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Application Number	
Filing Date	
First Named Inventor	Daniel E. Grupp
Art Unit	
Examiner Name	

Sheet	1	**of**	12	**Attorney Docket No:** 3771-0003-DC13

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](If known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		3708360	01/02/1973	WAKEFIELD, JR.; et al.	
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Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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		EP 0789388 A2	08/13/1997	AGENCY INDUSTRIAL SCIENCE AND TECHNOLOGY		
		WO 2002/043109 A2	05/30/2002	INFINEON TECHNOLOGIES AG; et al.		

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NON PATENT LITERATURE DOCUMENTS			
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-04-14
Name/Print	Tarek N. Fahmi	Registration Number	41402

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(71) Anmelder *(für alle Bestimmungsstaaten mit Ausnahme von US)*: **INFINEON TECHNOLOGIES AG** [DE/DE]; St.-Martin-Strasse 53, 81669 München (DE).

(72) Erfinder; und

(75) Erfinder/Anmelder *(nur für US)*: **HOFMANN, Franz** [DE/DE]; Herbergstrasse 25B, 80995 München (DE). **RISCH, Lothar** [DE/DE]; Tizianstr. 27, 85579 Neubiberg (DE). **ROESNER, Wolfgang** [DE/DE]; Sudetenstrasse 23, 85521 Ottobrunn (DE).

(74) Anwalt: **VIERING, JENTSCHURA & PARTNER**; Steinsdorfstr. 6, 80538 München (DE).

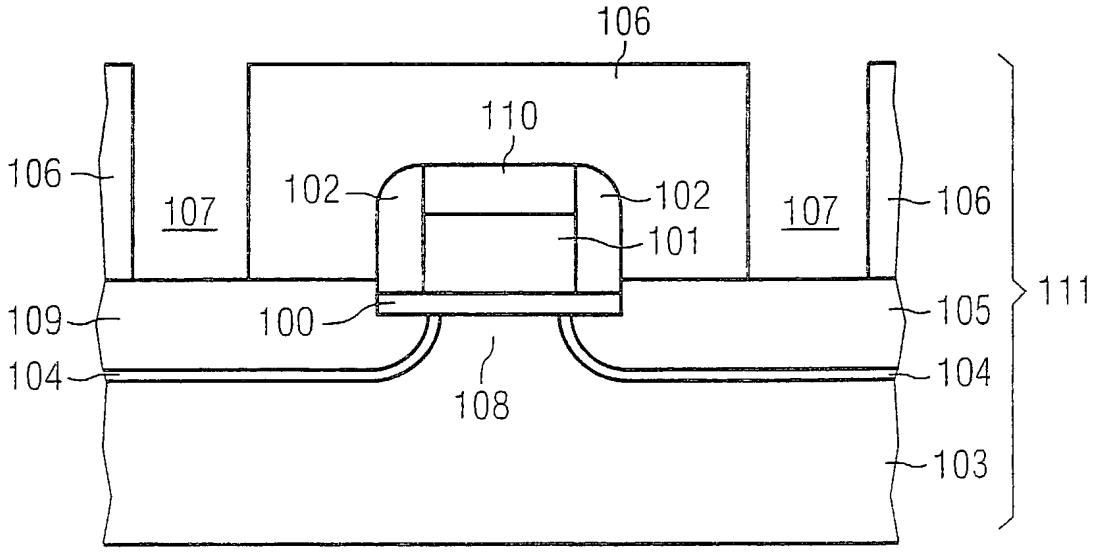
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[Fortsetzung auf der nächsten Seite]

(54) Title: METHOD FOR PRODUCING A PLANAR FIELD EFFECT TRANSISTOR AND A PLANAR FIELD EFFECT TRANSISTOR

(54) Bezeichnung: VERFAHREN ZUM HERSTELLEN EINES PLANAREN FELDEFFEKTTRANSISTORS UND PLANARER FELDEFFEKTTRANSISTOR



(57) Abstract: The invention relates to a planar field effect transistor comprising a barrier layer that lies adjacent to and/or below part of the gate region. Said barrier layer is configured between the source region and the channel region and/or between the drain region and the channel region in such a way that there is practically no diffusion of the doping atoms from the source region and the drain region into the channel region, but that electric charge carriers can tunnel through the barrier layer.

[Fortsetzung auf der nächsten Seite]

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GF Exhibit 1126 - 13/2248

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Zur Erklärung der Zweibuchstaben-Codes und der anderen Abkürzungen wird auf die Erklärungen ("Guidance Notes on Codes and Abbreviations") am Anfang jeder regulären Ausgabe der PCT-Gazette verwiesen.

(57) Zusammenfassung: Ein planarer Feldeffekttransistor weist eine Barriereschicht neben dem Gate-Bereich und/oder unter einem Teil des Gate-Bereichs auf, wobei die Barriereschicht zwischen dem Source-Bereich und dem Kanalbereich und/oder zwischen dem Drain-Bereich und dem Kanalbereich derart ausgestaltet ist, dass im wesentlichen kein Diffundieren der sich in dem Source-Bereich und dem Drain-Bereich befindlichen Dotieratome in den Kanalbereich erfolgen kann, jedoch ein Tunneln elektrischer Ladungsträger durch die Barriereschicht möglich ist.

Beschreibung

Verfahren zum Herstellen eines planaren Feldeffekttransistors und planarer Feldeffekttransistor

Die Erfindung betrifft ein Verfahren zum Herstellen eines planaren Feldeffekttransistors und einen planaren Feldeffekttransistor.

Ein Feldeffekttransistor ist aus [1] bekannt. Der Feldeffekttransistor aus [1] ist ein vertikaler Feldeffekttransistor, bei dem ein Gate-Bereich senkrecht zur Richtung des Elektronenflusses zwischen einem Source-Bereich und einem Drain-Bereich angeordnet ist. Der Feldeffekttransistor aus [1] weist einen Source-Bereich, einen Drain-Bereich, einen Gate-Bereich sowie einen Kanalbereich auf, wobei alle Bereiche aus Polysilizium hergestellt sind. Zwischen dem Source-Bereich und dem Kanalbereich ist eine erste elektrisch isolierende Schicht aus Nitrid (erste Tunnelbarriere) ausgebildet. Ferner ist zwischen dem Drain-Bereich und dem Kanalbereich eine zweite elektrisch isolierende Schicht aus Nitrid (zweite Tunnelbarriere) ausgebildet. Die erste elektrisch isolierende Schicht und die zweite elektrisch isolierende Schicht weisen jeweils eine Dicke von ungefähr 2 nm auf.

Häufig ist es insbesondere hinsichtlich der elektrischen Eigenschaften des Kanalbereichs wünschenswert, dass insbesondere der Kanalbereich aus monokristallinem Silizium hergestellt wird.

Die Ausbildung eines Kanalbereichs aus monokristallinem Silizium ist bei dem Herstellungsverfahren aus [1] nicht möglich, insbesondere da die Nitridschichten in dem Herstellungsverfahren aus [1] gemeinsam mit polykristallinem Silizium hergestellt werden können.

Weiterhin ist eine Übersicht über Oxynitride in [2] zu finden.

[3] beschreibt einen Feldeffekttransistor sowie ein Herstellungsverfahren zum Herstellen des Feldeffekttransistors, wobei die Source-/Drain-Bereiche als dotierte, monokristalline Siliziumbereiche ausgestaltet sind. Das Herstellungsverfahren gemäß [3] ist relativ aufwendig und somit teuer.

In [4] ist ferner ein planarer Feldeffekttransistor beschrieben mit einer Barriereschicht, wobei die Barriereschicht zwischen dem Source-Bereich und dem Kanalbereich und/oder zwischen dem Drain-Bereich und dem Kanalbereich derart ausgebildet ist, dass kein Tunneln elektrischer Ladungsträger durch die Barriereschicht in das Substrat möglich ist.

Somit liegt der Erfindung das Problem zugrunde, einen Feldeffekttransistor mit jeweils einer elektrisch isolierenden Schicht zwischen dem Source-Bereich und dem Kanalbereich bzw. dem Drain-Bereich und dem Kanalbereich anzugeben, bei dem der Kanalbereich aus monokristallinem Silizium hergestellt sein kann.

Das Problem wird gelöst durch ein Verfahrens zum Herstellen eines planaren Feldeffekttransistors und durch einen planaren Feldeffekttransistor mit den Merkmalen gemäß den unabhängigen Patentansprüchen.

Ein Verfahren zum Herstellen eines planaren Feldeffekttransistors weist folgende Schritte auf:

- Bilden einer isolierenden Schicht auf einem Substrat;
- Bilden eines Gate-Bereichs auf der isolierenden Schicht;
- Bilden mindestens eines Spacers auf der isolierenden Schicht;

- Bilden einer Barriereschicht neben der isolierenden Schicht und/oder unter einem Teil der isolierenden Schicht;
- Abscheiden eines Source-Bereichs auf der einen Seite des Gate-Bereichs und Abscheiden eines Drain-Bereichs auf der anderen Seite des Gate-Bereichs und eines Kanalbereichs unterhalb der isolierenden Schicht zwischen dem Source-Bereich und dem Drain-Bereich; und
- Bilden einer Barriereschicht zwischen dem Source-Bereich und dem Kanalbereich und/oder zwischen dem Drain-Bereich und dem Kanalbereich derart, dass im Wesentlichen kein Diffundieren der sich in dem Source-Bereich und dem Drain-Bereich befindlichen Dotier-Atome in den Kanalbereich erfolgen kann, jedoch ein Tunneln elektrischer Ladungsträger durch die Barriereschicht in den Kanalbereich und in das Substrat möglich ist.

Das Problem wird ferner gelöst durch einen planaren Feldeffekttransistor mit

- einem elektrisch leitenden Substrat,
- einem Drain-Bereich,
- einem Source-Bereich,
- einem Kanalbereich zwischen dem Drain-Bereich und dem Source-Bereich,
- einem Gate-Bereich auf der isolierenden Schicht, wobei auf der isolierenden Schicht mindestens ein Spacer angeordnet ist,
- einer isolierenden Schicht zwischen dem Gate-Bereich und dem Substrat
- einer Barriereschicht neben dem Gate-Bereich und/oder unter einem Teil des Gate-Bereichs,
- wobei die Barriereschicht zwischen dem Source-Bereich und dem Kanalbereich und/oder zwischen dem Drain-Bereich und dem Kanalbereich derart ausgestaltet ist, dass im wesentlichen kein Diffundieren der sich in dem Source-Bereich und dem Drain-Bereich befindlichen Dotieratome in den Kanalbereich erfolgen kann, jedoch ein Tunneln

elektrischer Ladungsträger durch die Barriereschicht in den Kanalbereich und in das Substrat möglich ist.

Bei dem planaren Feldeffekttransistor handelt es sich anschaulich um eine Modifikation eines bekannten planaren MOSFET (**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor), bei dem eine dünne Barriereschicht aus einem dielektrischen Material zwischen dem Source-Bereich bzw. Drain-Bereich und dem dazwischen liegenden Kanalbereich angeordnet ist.

Insbesondere aufgrund des Vorsehens eines planaren Feldeffekttransistors und der entsprechenden Vorgehensweise beim Herstellen des planaren Feldeffekttransistors wird es nunmehr erstmals möglich, den Kanalbereich aus monokristallinem Silizium herzustellen, was erhebliche Vorteile in den elektrischen Eigenschaften mit sich bringt. Insbesondere durch die Verwendung von monokristallinem Silizium in dem Kanalbereich wird die Beweglichkeit der elektrischen Ladungsträger in dem Kanalbereich im Vergleich zu einem Kanalbereich, der aus polykristallinem Silizium gebildet wird, um bis zu einem Faktor 100 und mehr verbessert.

Gemäß einer Ausgestaltung der Erfindung ist es somit vorgesehen, den Kanalbereich aus monokristallinem Silizium herzustellen.

Im Rahmen der Erfindung ist unter dem Ausdruck "dünn" eine Barriereschichtdicke von vorzugsweise weniger als ungefähr 2 nm zu verstehen, vorzugsweise von weniger als ungefähr 1 nm.

Gleichzeitig wird zusätzlich durch die Barriereschicht erreicht, dass die sich in den Source- und Drain-Bereichen befindlichen Dotieratome nicht aufgrund der zum Dotieren notwendigen Schritte bei hoher Temperatur in den dazwischenliegenden Kanalbereich des Substrats hinein

diffundieren. Ein solches Diffundieren in den Kanalbereich würde zu einem Verlaufen der Dotierprofile zwischen dem Kanalbereich und dem Source-Bereich bzw. Drain-Bereich und daher zu einer Verschlechterung der Steuerbarkeit des für die Schaltfähigkeit des Transistors unerlässlichen Kanalbereichs führen.

Des weiteren ermöglicht die planare Anordnung des erfindungsgemäßen planaren Feldeffekttransistors eine erhöhte Flexibilität hinsichtlich des Aufbaus des Feldeffekttransistors.

Beispielsweise ist es, wie untenstehend ausführlich beschrieben, möglich, je nach verwendetem Ätzverfahren die Barriereschicht

- nur neben der isolierenden Schicht des Gate-Komplexes,
- nur unter der isolierenden Schicht des Gate-Komplexes oder
- neben und unter der isolierenden Schicht des Gate-Komplexes

auszubilden.

Gegenüber dem in [1] beschriebenen, vertikalen Feldeffekttransistor mit Barriereschichten, bei dem es erforderlich ist, jede Schicht des Transistors mittels eines getrennten Verfahrensschrittes aufzubauen, ist es beispielsweise bei dem erfindungsgemäßen planaren Feldeffekttransistor möglich, mehrere Komponenten des Transistors, wie zum Beispiel Barriereschichten auf beiden Seiten der Isolierschicht sowie den Source-Bereich und den Drain-Bereich auf beiden Seiten der Isolierschicht gleichzeitig, beispielsweise durch ein einziges Abscheideverfahren, zu bilden. Dadurch wird gegenüber dem Stand der Technik ein hohes Maß an Gleichmäßigkeit hinsichtlich der Dicke und der genauen Zusammensetzung der erfindungsgemäßen Barriereschicht sowie des Source-Bereichs und des Drain-Bereichs gewährleistet.

Gemäß einer Weiterbildung der Erfindung ist es für den Fall, dass die Barriereschicht neben und unter einem Teil der isolierenden Schicht gebildet werden soll, vorgesehen, das Substrat vor dem Bilden der Barriereschicht neben und teilweise unter der isolierenden Schicht isotrop wegzuätzen.

Gemäß einer anderen Weiterbildung der Erfindung ist es für den Fall, dass die Barriereschicht nur unter einem Teil der isolierenden Schicht gebildet werden soll, vorgesehen, das Substrat vor dem Bilden der Barriereschicht neben und teilweise unter der isolierende Schicht isotrop wegzuätzen.

Die Barriereschicht wird vorzugsweise in einer Dicke von 1 nm oder weniger gebildet wird.

Der Spacer kann aus SiO_2 gebildet werden, beispielsweise mittels eines TEOS-, Silanoxid-, LTO-, SACVD-, HTO-, PECVD- oder eines Dep./Etch-Abscheideverfahrens.

Gemäß einer Ausgestaltung der Erfindung wird der Spacer in einer Dicke von höchstens 50 nm, vorzugsweise in einer Dicke von höchstens 10 nm, gebildet.

Gemäß einer Ausgestaltung der Erfindung wird die Barriereschicht aus einem dielektrischen Material gebildet, vorzugsweise aus einem Oxynitrid, beispielsweise einem in [2] beschriebenen Oxynitrid.

Gemäß einer weiteren Ausgestaltung der Erfindung wird die Barriereschicht aus SiO_2 oder Si_3N_4 gebildet.

Ausführungsbeispiele der Erfindung sind in den Figuren dargestellt und werden im Weiteren näher erläutert.

Es zeigen

Figuren 1a bis 1c einen Zeitablauf eines Herstellungsverfahrens gemäß einem ersten Ausführungsbeispiel der Erfindung,

Figur 2 eine schematische Darstellung eines zweiten Ausführungsbeispiels der Erfindung in fertiggestelltem Zustand, und

Figur 3 ein weiteres Ausführungsbeispiel der Erfindung in fertiggestelltem Zustand.

Fig.1a bis **Fig.1c** sind als Zeitablauf eines Herstellungsverfahrens eines erfindungsgemäßen planaren Feldeffekttransistors zu verstehen.

Wie in **Fig.1a** gezeigt ist, wird zunächst auf einem Substrat 103 eine isolierende Schicht 100 gebildet.

Das Substrat 103 besteht vorzugsweise aus einem für den Aufbau eines planaren Feldeffekttransistors geeigneten Material, bevorzugt aus monokristallinem Silizium.

Die isolierende Schicht 100, auch als Gate-Oxid (GOX) bezeichnet, besteht aus einem elektrisch isolierenden Material, wie beispielsweise Siliziumdioxid, und wird auf dem Substrat 103 beispielsweise durch einen für den Aufbau solcher planaren Feldeffekttransistoren bekannten Vorgang, wie beispielsweise durch thermische Oxidation gebildet.

Sodann wird der Gate-Bereich 101 als eine Schicht leitfähigen Materials, wie beispielsweise Polysilizium auf der isolierenden Schicht 100 gebildet. Das für diesen Zweck verwendete Silizium ist gemäß diesem Ausführungsbeispiel mit Phosphor dotiert.

Das Bilden des Gate-Bereichs 101 auf der isolierenden Schicht 100 erfolgt in bekannter Weise mit Hilfe von Photolithografie und anisotropem Reaktiven Ionenätzen.

Das Bilden des Gate-Bereichs 101 auf der isolierenden Schicht 100 erfolgt gemäß diesem Ausführungsbeispiel derart, dass eine Schicht aus Siliziumdioxid auf dem Substrat aufgebracht wird. Auf die Schicht aus Siliziumdioxid, die später die isolierende Schicht 100 bildet, wird eine Schicht aus Polysilizium aufgebracht, vorzugsweise mittels eines Abscheideverfahrens (CVD-Verfahrens) aus der Gasphase, vorzugsweise mittels eines Niederdruck-CVD-Verfahrens.

In einem weiteren Schritt wird die Polysiliziumschicht mit Phosphoratomen dotiert.

Ferner wird auf die Schicht aus Polysilizium in einem weiteren Prozessschritt eine TEOS-Schicht aufgebracht (TEOS: **T**etra-**E**thyl-**O**rtho-**S**ilicate).

Anschließend wird mittels Fotolithographie der spätere Gate-Bereich strukturiert.

Anschließend werden die TEOS-Schicht und die Schicht aus Polysilizium geätzt derart, dass ein Bereich oberhalb der isolierenden Schicht 100 übrig bleibt, so dass jeweils seitlich neben den nicht weggeätzten Teilen der TEOS-Schicht und der Schicht aus Polysilizium oberhalb der isolierenden Schicht 100 Raum gebildet wird für in weiteren Schritten gebildete Spacer.

In einem weiteren Schritt wird eine weitere TEOS-Schicht ganzflächig aufgebracht und die Spacer 102 gebildet, indem die TEOS-Schicht sowie die freigelegten Teile der isolierenden Schicht 100 ganzflächig anisotrop bis auf das Substrat 103 zurückgeätzt werden, so dass nur die Spacer 102 bestehen bleiben.

Der fertiggestellte Gate-Komplex 100-102 ist aus **Fig.1a** ersichtlich. Dieser wird durch die isolierenden Schicht 100, den Gate-Bereich 101 und den Spacer 102 gebildet.

Nach dem Bilden des fertiggestellten Gate-Komplexes 100-102 wird gemäß eines Ausführungsbeispiels des Verfahrens das Substrat 103 beidseitig dieses Gate-Komplexes 100-102 isotrop weggeätzt, so dass sowohl neben als auch unter einem Teil des Gate-Komplexes 100-102 ein Bereich des Substrats 103 ausgehöhlt wird.

Gemäß diesem Ausführungsbeispiel der Erfindung ist es vorgesehen, dass das Substrat 103 isotrop, d.h. nicht anisotrop weggeätzt wird. Auf diese Weise wird gewährleistet, dass es zu einer Unterätzung unterhalb eines Teils der isolierenden Schicht 100 kommt. Diese weggeätzten Aussparungen 110 beidseitig des Gate-Komplexes 100-102 werden letztendlich als der Source-Bereich bzw. der Drain-Bereich des fertiggestellten planaren Feldeffekttransistors 111 dienen.

Auf der sich durch das Wegätzen des Substrats 103 ergebende Oberfläche des Substrats 103 wird dann eine dünne, dielektrische Schicht 104 aufgebracht.

Diese dünne, dielektrische Schicht 104 dient als die eingangs erwähnte Barriereschicht, die im Wesentlichen kein Diffundieren der sich in dem Source-Bereich und dem Drain-Bereich befindlichen Dotieratome in das umgebende Substrat 103, und besonders in den dazwischen liegenden Kanalbereich 108 hinein zulässt, welche Barriereschicht jedoch ein Tunneln elektrischer Ladungsträger durch sich selbst ermöglicht.

Beispielsweise kann ein thermisches Oxid, ein Nitrid oder eine Kombination aus einem Oxid und einem Nitrid für die Barriereschicht 104 verwendet werden.

Bei dem Abscheiden des für die Barriereschicht 104 verwendeten Materials ist zu beachten, dass die Barriereschicht 104 in ihrem gesamten Verlauf in einer Dicke von 2 nm oder weniger, vorzugsweise sogar nur in einer Dicke von 1 nm oder weniger, gebildet werden sollte.

So wird bei der Barriereschicht 104 allgemein eine derartige Dicke gewährleistet, dass das Tunneln der Ladungsträger aus dem Source-Bereich und aus dem Drain-Bereich stattfinden kann, während jedoch kein Diffundieren der Dotierstoffe aus dem Source-Bereich und/oder Drain-Bereich in das Substrat 103 oder in den zwischen dem Source-Bereich und dem Drain-Bereich liegenden Kanalbereich 108 hinein erfolgt.

Fig.1c zeigt den planaren Feldeffekttransistor gemäß diesem Ausführungsbeispiel der Erfindung im fertiggestellten Zustand.

Oberhalb der in **Fig.1b** aufgebrachten Barriereschichten 104 beidseitig des Gate-Komplexes 100-102 sind aus **Fig.1c** zwei Bereiche 105, 109 ersichtlich, die den Source-Bereich 105 bzw. den Drain-Bereich 109 darstellen.

Diese Bereiche 105, 109 werden in bekannter Weise durch Abscheiden von Polysilizium, das in der Regel mit Arsenatomen dotiert ist, gebildet. Die Bereiche 105, 109 sind sehr hoch dotiert, d.h. in der Regel bis zu einer Dichte von 10^{21} As-Atome/cm^{-3}. Aufgrund dieser besonders hohen Dotierkonzentration könnte es sehr leicht zu einem unerwünschten Diffundieren dieser Dotieratome kommen, wenn es keine Barriereschicht 104 gäbe.

Mittels bekannter CMP-Verfahren (CMP = **C**hemical **M**echanical **P**olishing) wird sodann die mit Arsenatomen hochdotierte Polysilizium Schicht geebnet und somit für den nächsten Verfahrensschritt vorbereitet.

Oberhalb des gesamten planaren Feldeffekttransistors wird eine weitere elektrisch isolierende Schicht 106 abgeschieden. Die weitere isolierende Schicht 106 kann aus BPSG (**B**or **P**hosphor **S**ilikat **G**las) bestehen, das manchmal als Zwischenoxid, oder „ZOX" bezeichnet wird. In die weitere isolierende Schicht 106 werden sodann Kontaktlöcher 107 geätzt, die einen Kontakt zwischen der metallischen Leiterbahn und dem Source-Bereich bzw. dem Drain-Bereich 109 bei der anschließenden Metallisierung des planaren Feldeffekttransistors ermöglichen.

Das Ausführungsbeispiel des Verfahrens sowie des planaren Feldeffekttransistors 111, das in **Fig.1a** bis **Fig.1c** dargestellt ist, ergibt einen Feldeffekttransistor 111 wie in **Fig.1c** gezeigt, bei dem die Barriereschicht 104 sowohl neben als auch unter einem Teil der isolierenden Schicht 100 gebildet wird.

Im Gegensatz dazu zeigt **Fig.2** als ein weiteres Ausführungsbeispiel einen planaren Feldeffekttransistor 212 in fertiggestelltem Zustand, bei dem die Barriereschicht 204 lediglich unter einem Teil der isolierenden Schicht 200, d.h. nicht auch neben der isolierenden Schicht 200, gebildet ist.

Bei diesem Ausführungsbeispiel der Erfindung erfolgt der Aufbau des Gate-Komplexes, bestehend aus der isolierenden Schicht 200, dem Gate-Bereich 201 und dem Spacer 202, in analoger Weise wie für **Fig.1a** obenstehend beschrieben. Auch das Abscheiden des Materials für die Barriereschicht 204 erfolgt in analoger Weise wie für **Fig.1a** obenstehend beschrieben.

Der in **Fig.2** dargestellte planare Feldeffekttransistor 212 weist zwei Barrieren 204 sowie einen Source-Bereich 205 und einen Drain-Bereich 206 auf unterhalb der isolierenden Schicht 200 zwischen der isolierenden Schicht 200 und einer

planaren freigelegten Fläche 207. Jeweils eine der beiden Barrieren 204 ist zwischen dem Source-Bereich 205 und dem Kanalbereich 203 sowie zwischen dem Drain-Bereich 206 und dem Kanalbereich 203 angeordnet.

Gemäß diesem Ausführungsbeispiel werden die Barrieren 204 mittels einer thermischen Oxidation erzeugt, so dass die Barrieren 204 automatisch in der in **Fig.2** dargestellten Form entstehen, weil die planare freigelegte Fläche 207 schon aus dem vergrabenen Oxid des SOI-Ausgangsmaterials besteht.

Anschaulich entspricht diese Vorgehensweise dem Bilden eines Ausgangsmaterials eines SOI-Komplexes (**S**ilicon **O**n **I**nsulator).

So entsteht im fertiggestellten Zustand des planaren Feldeffekttransistors 212 eine Barriereschicht 204 lediglich zwischen dem Source-Bereich 206 und dem Kanalbereich 203 sowie zwischen dem Drain-Bereich 205 und dem Kanalbereich 203.

In anderen Worten ausgedrückt bedeutet dies, dass es in diesem Ausführungsbeispiel der Erfindung keine Barriereschicht 204 zwischen dem Source-Bereich 206 bzw. dem Drain-Bereich 205 und dem Substrat 209 gibt.

Es ist anzumerken, dass bei diesem Ausführungsbeispiel der Erfindung das Substrat 209 aus zwei unterteilten Abschnitten 207 und 208 besteht. Hierbei besteht der Substrat-Bereich 208 aus einem leitfähigen Material, wie beispielsweise Silizium, und der Substrat-Abschnitt 207 besteht vorzugsweise aus einem nicht leitfähigen Material, beispielsweise einem Oxid.

Die Beschaffenheit des Substrat-Abschnitts 207 als nicht leitfähiges Material verhindert, dass Dotieratome in dem Source-Bereich 205 bzw. dem Drain-Bereich 206 in das darunterliegende Material des Substrats 209 hinein diffundieren, und so den Kanalbereich 203 verunreinigen.

Im Gegensatz dazu wäre ein Diffundieren der Dotieratome in dem Source-Bereich 205 bzw. dem Drain-Bereich 206 in den dazwischen liegenden Kanalbereich 203 hinein ohne Barriereschicht 204 sehr wohl möglich, weshalb sich diese Barriereschicht 204 zwischen dem Source-Bereich 206 bzw. dem Drain-Bereich 205 und dem dazwischen liegenden Kanalbereich 203 befindet.

Der Aufbau des in **Fig.2** dreischichtig ausgestalteten Substrats 209 erfolgt in einfacher Weise vor dem Aufbau des Gate-Komplexes 200-202. Der Aufbau erfolgt ausgehend von einer Siliziumschicht 208, worauf eine nicht leitfähige isolierende Schicht 207 aufgebracht wird und schließlich durch das Aufbringen einer dritten Schicht aus Silizium auf der isolierenden Schicht 207. Nach dem Wegätzen bildet diese dritte Schicht dann den Kanalbereich 203.

Auf den Source-Bereich 205, dem Gate-Komplex 200-202 sowie dem Drain-Bereich 206 wird eine elektrisch isolierende Schicht 210, vorzugsweise aus Siliziumdioxid, aufgebracht, in die in einem weiteren Schritt Kontaktlöcher 211 für Leiterbahnen geätzt werden, die einen Kontakt zwischen der metallischen Leiterbahn und dem Source-Bereich bzw. dem Drain-Bereich 109 bei der anschließenden Metallisierung des planaren Feldeffekttransistors ermöglichen.

Fig.3 zeigt einen weiteren fertiggestellten, planaren Feldeffekttransistor, der mittels des erfindungsgemäßen Verfahrens ausgehend von dem noch nicht fertiggestellten Feldeffekttransistor, der in **Fig.1a** gezeigt ist, hergestellt wird.

Bei der Herstellung des planaren Feldeffekttransistors in **Fig.3** wird nach dem Aufbau des Gate-Komplexes 100-102 auf dem Substrat 103 in **Fig.1a** (entspricht Gate-Komplex 300-302 bzw. Substrat 307 in **Fig.3**) die Barriereschicht 304 direkt auf dem

Substrat 307 gebildet, ohne dass das Substrat 307 im Voraus weggeätzt wird. Die Barriereschicht 304 in **Fig.3** wird also ausschließlich neben, d.h. weder ausschließlich unter (vgl. **Fig.2**) noch unter und neben (vgl. **Fig.1c**) der Isolierschicht 300 gebildet. Der Source-Bereich 306 bzw. Drain-Bereich 305 des Feldeffekttransistors 309 in **Fig.3** kann also direkt auf der Barriereschicht abgeschieden werden, ohne dass es im Voraus eines weiteren Ätzverfahrens bedarf.

Es ist anzumerken, dass das in **Fig.3** gezeigte Ausführungsbeispiel des planaren Feldeffekttransistors 309 gemäß der Erfindung keinen Kanalbereich aufweist, welcher im Gegensatz zu den Ausführungsbeispielen in **Fig.1c** und in **Fig.2**, unmittelbar an der Barriereschicht 304 grenzt. Aus **Fig.3** ist ersichtlich, dass der Kanalbereich 308 beidseitig um den Abstand 303 von den jeweiligen Barriereschichten 304 entfernt angeordnet ist. Der Abstand 303 ergibt sich aus der Dicke des Spacers 302, der auf der isolierenden Schicht 300 gebildet ist. Die Bereiche 303 unterhalb der isolierenden Schicht 300 liegen außerhalb des durch den Gate-Bereich 301 erzeugten Feldes, so dass bei angelegter Gate-Spannung die Leitfähigkeit der Bereiche 303 gegenüber derjenigen des Kanalbereichs 308, der direkt in dem durch den Gate-Bereich 301 erzeugten Feld liegt, geringer ist.

Aus diesem Grund ist die Steuerbarkeit des planaren Feldeffekttransistors in **Fig.3** von dem Abstand 303 abhängig, wobei ein größerer Abstand 303 zu einer verschlechterten Steuerbarkeit des planaren Feldeffekttransistors 309 führt.

Bei dem Aufbau des planaren Feldeffekttransistors 309 in **Fig.3** ist also verfahrenstechnisch darauf zu achten, dass der auf der isolierenden Schicht 300 gebildete, nicht leitfähige Spacer 302 durch entsprechende Einstellung des zur Bildung dieses Spacers verwendeten Abscheideverfahrens möglichst dünn gebildet wird.

Bevorzugt wird der Spacer in einer Dicke von höchstens 10 nm gebildet, so dass die Abstände 303 klein genug sind, um eine Diffusion von Ladungsträgern durch die weniger gut leitfähigen Bereiche 303 des Substrats 307 beidseitig des Kanalbereichs 308 zu ermöglichen und daher eine gute Steuerbarkeit des planaren Feldeffekttransistors zu gewährleisten.

In diesem Dokument sind folgende Veröffentlichungen zitiert:

[1] T. Kisu, K. Nakazato, Silicon stacked transistor with source and drain tunnel barriers, Proceedings of the 29th European solid-state device research conference ESSDERC, S. 532, 1999.

[2] V.H.C. Watt et al, Ultra-Thin High Quality Oxynitride Formed by NH3 Nitridation and High Pressure O2 Re-oxidation, Proceedings of the 30th European Solid-State Device Research Conference (ESSDERC 2000), Cork, Ireland, 11. - 13. September 2000

[3] DE 42 12 861 C2

[4] US 6,091,076

Bezugszeichenliste

100	Isolierende Schicht
101	Gate-Bereich
102	Spacer
103	Substrat
104	Barriereschicht
105	Drain-/Source-Bereich
106	Isolierende Siliziumdioxidschicht
107	Kontaktlöcher für Leiterbahnen
108	Kanalbereich
109	Source-/Drain-Bereich
200	Isolierende Schicht
201	Gate-Bereich
202	Spacer
203	Kanalbereich
204	Barriereschicht
205	Drain-/Source-Bereich
206	Source-/Drain-Bereich
207	Isolierende Substratschicht
208	Leitende Substratschicht
209	Substrat
210	Isolierende Siliziumdioxidschicht
211	Kontaktlöcher für Leiterbahne
300	Isolierende Schicht
301	Gate-Bereich
302	Spacer
303	Abstand
304	Barriereschicht
305	Drain-/Source-Bereich
306	Source-/Drain-Bereich
307	Substrat
308	Kanalbereich

Patentansprüche

1. Verfahren zum Herstellen eines planaren Feldeffekttransistors,

- bei dem auf einem Substrat eine isolierende Schicht gebildet wird;
- bei dem auf der isolierenden Schicht ein Gate-Bereich gebildet wird;
- bei dem auf der isolierenden Schicht mindestens ein Spacer gebildet wird;
- bei dem neben der isolierenden Schicht und/oder unter einem Teil der isolierenden Schicht eine Barriereschicht gebildet wird;
- bei dem auf der einen Seite der isolierenden Schicht ein Source-Bereich abgeschieden wird und auf der anderen Seite der isolierenden Schicht ein Drain-Bereich abgeschieden wird und zwischen dem Source-Bereich und dem Drain-Bereich ein Kanalbereich unterhalb der isolierenden Schicht gebildet wird; und
- bei dem die Barriereschicht zwischen dem Source-Bereich und dem Kanalbereich und/oder zwischen dem Drain-Bereich und dem Kanalbereich derart gebildet wird, dass im wesentlichen kein Diffundieren der sich in dem Source-Bereich und dem Drain-Bereich befindlichen Dotieratome in den Kanalbereich erfolgen kann, jedoch ein Tunneln elektrischer Ladungsträger durch die Barriereschicht in den Kanalbereich und in das Substrat möglich ist.

2. Verfahren gemäß Anspruch 1,
bei dem für den Fall, dass die Barriereschicht neben und unter einem Teil der isolierenden Schicht gebildet werden soll, das Substrat vor dem Bilden der Barriereschicht neben und teilweise unter der isolierenden Schicht isotrop weggeätzt wird.

3. Verfahren gemäß Anspruch 1,

bei dem die Barriereschicht in einer Dicke von 2 nm oder weniger gebildet wird.

4. Verfahren gemäß einem der Ansprüche 1 bis 3, bei dem der Spacer aus SiO_2 gebildet wird, das mittels eines TEOS-, Silanoxid-, LTO-, SACVD-, HTO-, PECVD- oder Dep./Etch-Abscheideverfahrens gebildet wird.

5. Verfahren gemäß Anspruch 4, bei dem der Spacer in einer Dicke von höchstens 50 nm gebildet wird,

6. Verfahren gemäß einem der Ansprüche 1 bis 5, bei dem die Barriereschicht aus einem dielektrischen Material gebildet wird.

7. Verfahren gemäß Anspruch 6, bei dem die Barriereschicht aus einem Oxynitrid gebildet wird.

8. Verfahren gemäß Anspruch 6, bei dem die Barriereschicht aus SiO_2 oder Si_3N_4 gebildet wird.

9. Planarer Feldeffekttransistor, mit

- einem elektrisch leitenden Substrat,
- einem abgeschiedenen Drain-Bereich,
- einem abgeschiedenen Source-Bereich,
- einem Kanalbereich zwischen dem Drain-Bereich und dem Source-Bereich,
- einem Gate-Bereich auf der isolierenden Schicht, wobei auf dem Gate-Bereich und auf der isolierenden Schicht mindestens ein Spacer angeordnet ist,
- einer isolierenden Schicht zwischen dem Gate-Bereich und dem Substrat
- einer Barriereschicht neben dem Gate-Bereich und/oder unter einem Teil des Gate-Bereichs,

- wobei die Barriereschicht zwischen dem Source-Bereich und dem Kanalbereich und/oder zwischen dem Drain-Bereich und dem Kanalbereich derart ausgestaltet ist, dass im wesentlichen kein Diffundieren der sich in dem Source-Bereich und dem Drain-Bereich befindlichen Dotieratomen in den Kanalbereich erfolgen kann, jedoch ein Tunneln elektrischer Ladungsträger durch die Barriereschicht in den Kanalbereich und in das Substrat möglich ist.

10. Planarer Feldeffekttransistor gemäß Anspruch 9, bei dem die Barriereschicht dielektrisches Material aufweist.

11. Planarer Feldeffekttransistor gemäß Anspruch 9, bei dem die Barriereschicht Oxynitrid aufweist.

12. Planarer Feldeffekttransistor gemäß Anspruch 10, bei dem die Barriereschicht SiO_2 oder Si_3N_4 aufweist.

13. Planarer Feldeffekttransistor gemäß einem der Ansprüche 9 bis 12, bei dem die Dicke der Barriereschicht höchstens 2 nm beträgt.

14. Planarer Feldeffekttransistor gemäß einem der Ansprüche 9 bis 12, bei dem die Dicke der Barriereschicht höchstens 1 nm beträgt.

15. Planarer Feldeffekttransistor gemäß einem der Ansprüche 9 bis 14, bei dem der Spacer SiO_2 aufweist.

16. Planarer Feldeffekttransistor gemäß einem der Ansprüche 9 bis 15, bei dem die Barriereschicht neben dem Gate-Bereich liegt, wobei die Dicke des Spacers höchstens 50 nm beträgt.

FIG 1a

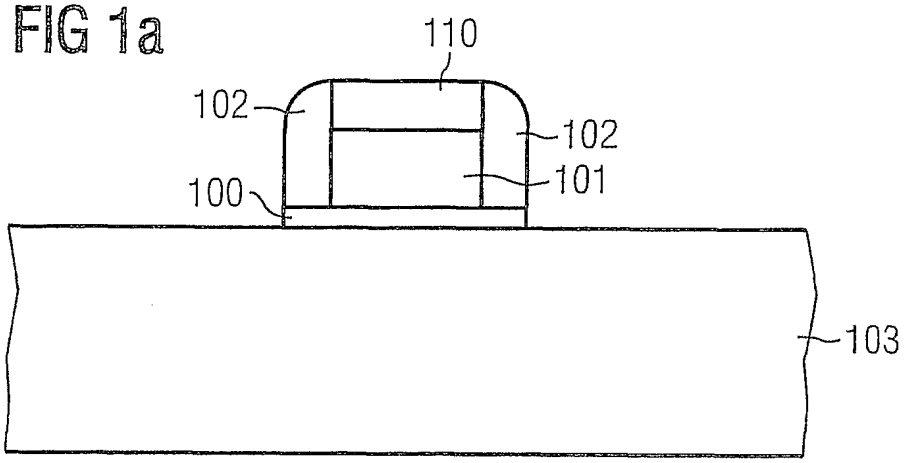


FIG 1b

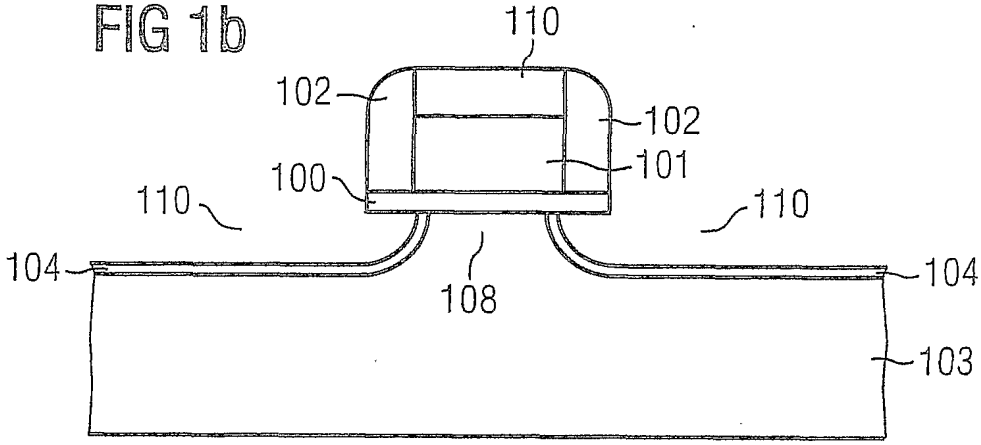


FIG 1c

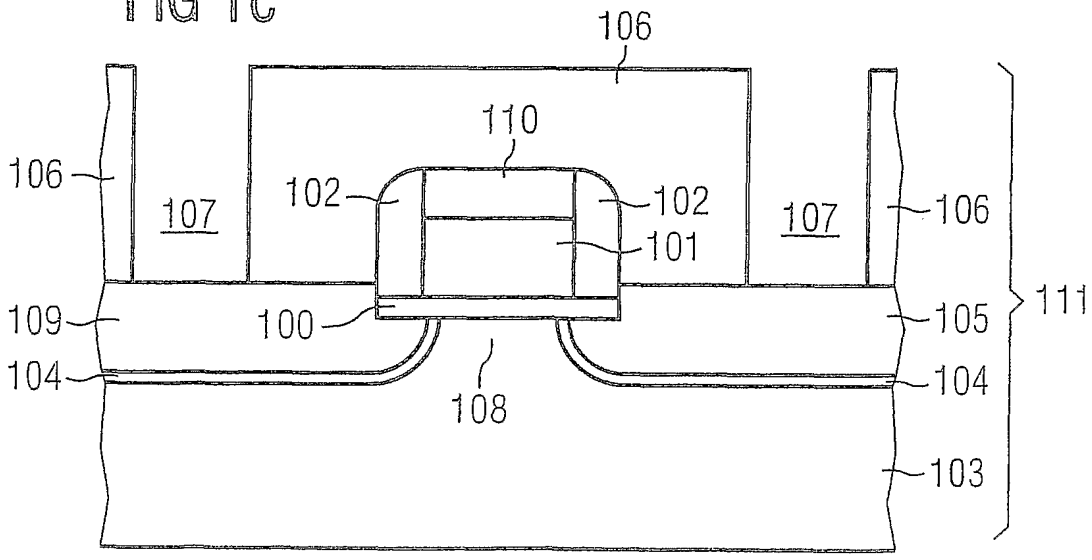


FIG 2

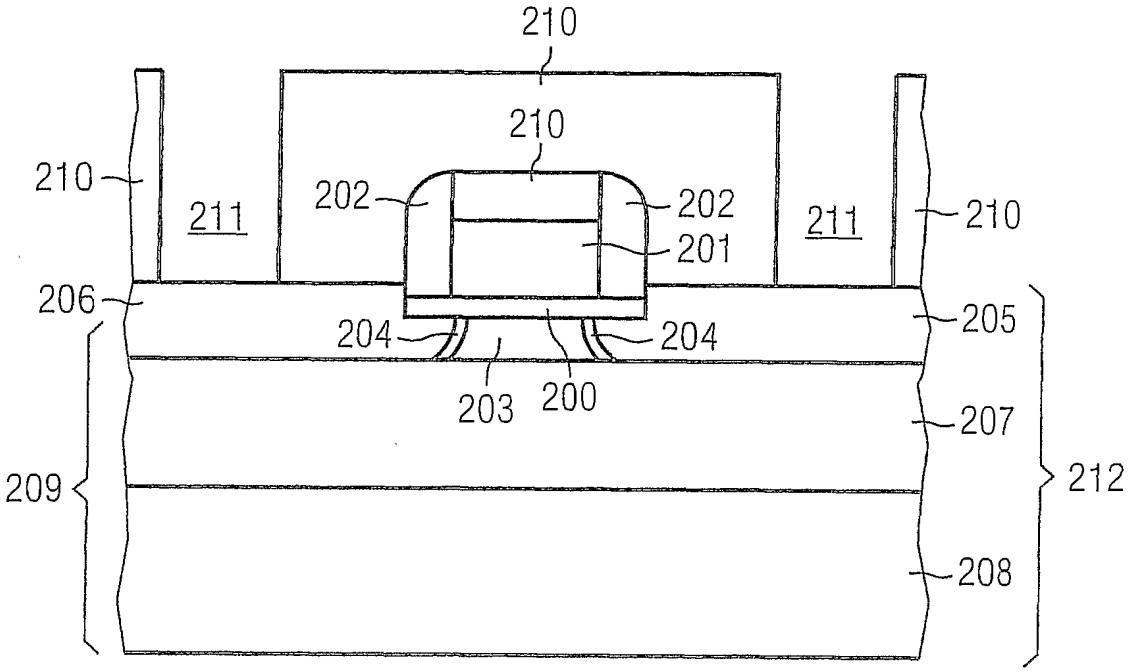
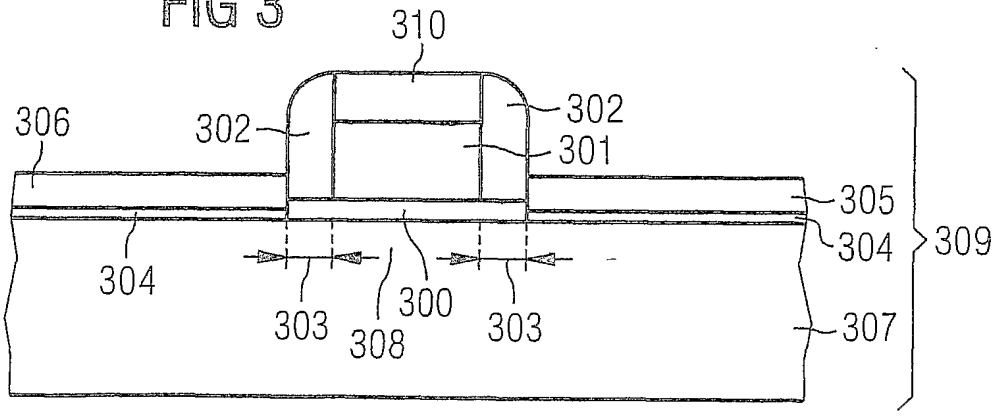

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FIG 3


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PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: TAREK FAHMI
TAREK N. FAHMI, APC
84 W. SANTA CLARA ST., SUITE 550
SAN JOSE, CA 95113

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 400037710017PCT	Date of mailing *(day month year)* 11 DEC 2012 **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2012/060893	International filing date *(day month year)* 18 October 2012
Applicant ACORN TECHNOLOGIES, INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 Telephone No. PCT OSP: 571-272-7774

Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: TAREK FAHMI
TAREK N. FAHMI, APC
84 W. SANTA CLARA ST., SUITE 550
SAN JOSE, CA 95113

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 400037710017PCT	Date of mailing *(day month year)* **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2012/060893	International filing date *(day month year)* 18 October 2012
Applicant ACORN TECHNOLOGIES, INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 Telephone No. PCT OSP: 571-272-7774

Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 400037710017PCT	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2012/060893	International filing date *(day/month/year)* 18 October 2012	(Earliest) Priority Date *(day/month/year)* 23 November 2011
Applicant ACORN TECHNOLOGIES, INC. *		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 4

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

GF Exhibit 1126 - 39/2248

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/060893

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/20 (2012.01)
USPC - 438/606
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/20, 21/28, 21/205, 21/285, 21/318, 21/762, 21/765, 33/28, 33/30 (2012.01)
USPC - 148/33.5; 257/14, E21.097, E21.54, E21.108, E21.546, 344, 407, 408, 412, 592, 929; 438/3, 424, 603-607

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent, Google Patents and Public AppFT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2005/0104137 A1 (FAULKNER et al) 19 May 2005 (19.05.2005) entire document	1, 3-12, 23-25, 27 --- 2, 13-22, 26, 28-30
Y	US 2011/0092047 A1 (GAINES et al) 21 April 2011 (21.04.2011) entire document	2, 22, 28-30
Y	US 4,843,029 A (JOYCE et al) 27 June 1989 (27.06.1989) entire document	13-21, 26

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 November 2012	11 DEC 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: 866-877-4883 5
TAREK N. FAHMI, APC
84 W. SANTA CLARA ST., SUITE 550
30 S. 17TH STREET
SAN JOSE, CA 95113

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	11 DEC 2012

Applicant's or agent's file reference	FOR FURTHER ACTION
400037710017PCT	See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2012/060893	18 October 2012	23 November 2011

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01L 21/20 (2012.01)
USPC - 438/606

Applicant ACORN TECHNOLOGIES, INC.

1. This opinion contains indications relating to the following items:

- [X] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [X] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	29 November 2012	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/060893

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

GF Exhibit 1126 - 42/2248

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/060893

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	2, 4-6, 12-23, 26-30	YES
	Claims	1, 3, 7-11, 24, 25	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-30	NO
Industrial applicability (IA)	Claims	1-30	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1, 3, 7-11, 24, and 25 lack novelty under PCT Article 33(2) as being anticipated by Faulkner et al.

Regarding claim 1, Faulkner et al. teach an electrical contact (semiconductor device or transistor, Claim 1; Paras. [0022]-[0027]), comprising a metal (metal layer 42, Para. [0077]; Figs. 2a-2d; Claims 1 and 6) and a group IV semiconductor (layer 26 may contain silicon, Figs. 2a-2d; Claim 1; Paras. [0073]-[0075]) separated by one of a monolayer of group V atoms, (ii) a monolayer of group III atoms, or (iii) one or more bi-layers, each bi-layer consisting of one monolayer of group V atoms and one monolayer of group III atom at an interface between the metal and the group IV semiconductor (layer 26 is separated from metal 42 by interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d), the atoms of the monolayer of group V or group III atoms or of each bi-layer of group V and group III atoms being in epitaxial alignment with a lattice structure of the semiconductor (the interfacial III-VI layered compound may be approximately epitaxially aligned with the underlying {111} semiconductor, Paras. [0024];[0027];[0031];[0062];[0067];[0076]).

Regarding claim 3, Faulkner et al. teach the contact of claim 1, wherein the metal comprises atoms of a different metallic element than the monolayer of group III metal atoms (the metal may comprise Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, Paras. [0063];[0077]).

Regarding claim 7, Faulkner et al. teach the contact of claim 1, wherein the group III atoms comprise any one or more of aluminum, gallium, indium, or alloys of aluminum, gallium and/or indium (elements from Groups IIIA-B include B, Al, Sc, Ga, Y, In, La, Tl and Ac, Para. [0023]).

Regarding claim 8, Faulkner et al. teach the contact of claim 1, wherein one monolayer of group III atoms is immediately adjacent the surface of the group IV semiconductor (layer 26 may contain silicon that is immediately adjacent interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0073]-[0076]; Figs. 2a-2d).

Regarding claim 9, Faulkner et al. teach the contact of claim 1, wherein one monolayer of group V atoms is immediately adjacent the surface of the group IV semiconductor (layer 26 may contain silicon that is immediately adjacent interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0073]-[0076]; Figs. 2a-2d).

Regarding claim 10, Faulkner et al. teach the contact of claim 1, wherein a surface of the group IV semiconductor at the interface is a {111} oriented surface or a {100} oriented surface (layer 26 may be a silicon containing {111} orientated surface, Figs. 2a-2d; Claim 1; Paras. [0073]-[0075]).

Regarding claim 11, Faulkner et al. teach the contact of claim 1, and a method of forming the contact (a method of forming a channel contact, Claim 13) by introducing at least the monolayer of group V atoms or the monolayer of group III atoms or the bi-layer of group V atoms and group III atoms at the interface between the metal (layer 26 is separated from metal 42 by interfacial layer 40, which may be a deposited monolayer or a bilayer of group III-VI compound, Claim 13; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d) and the group IV semiconductor (layer 26 may contain silicon, Figs. 2a-2d; Claim 13; Paras. [0073]-[0075]).

Regarding claim 24, Faulkner et al. teach the contact of claim 1, wherein one or more bi-layers of one monolayer of group V atoms and one monolayer of group III atoms are at the interface (layer 26 is separated from metal 42 by interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d) and each atomic layer of each bi-layer is in epitaxial alignment with one another and with the semiconductor lattice (the interfacial III-VI layered compound may be approximately epitaxially aligned with each other and the underlying {111} semiconductor, Paras. [0024];[0027];[0031];[0062];[0067];[0076]).

Regarding claim 25, Faulkner et al. teach an electrical contact (semiconductor device or transistor, Claim 1; Paras. [0022]-[0027]), comprising a metal (metal layer 42, Para. [0077]; Figs. 2a-2d; Claims 1 and 6) and a group IV semiconductor (layer 26 may contain silicon, Figs. 2a-2d; Claim 1; Paras. [0073]-[0075]) separated by ONE or both of a monolayer of epitaxially aligned group VI atoms (layer 26 is separated from metal 42 at the interface by epitaxially aligned interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d) and a monolayer of epitaxially aligned group II atoms at an interface between the metal and the semiconductor.

GF Exhibit 1126 - 43/2248

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Claims 4-6, 12, 23, and 27 lack an inventive step under PCT Article 33(3) as being obvious over Faulkner et al.

Regarding claim 4, Faulkner et al. teach the contact of claim 3, Faulkner et al. do not explicitly disclose wherein the metal comprises ruthenium, tantalum nitride or titanium nitride. However, Faulkner et al. teach the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]) and the use of metals, such as Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, (Paras. [0063];[0077]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a titanium compound as desired, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a metal of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Faulkner et al., Para. [0023]).

Regarding claim 5, Faulkner et al. teach the contact of claim 1, Faulkner et al. do not explicitly disclose wherein the group IV semiconductor comprises any of germanium, silicon, an alloy of silicon and germanium, an alloy of germanium and tin, an alloy of silicon with carbon, a compound of silicon and carbon, an alloy of germanium with carbon, a compound of germanium and carbon. However Faulkner et al. teaches the use of Group IV semiconductors in the interfacial layer as pure compounds or alloys of pure compounds (Para. [0023]) and that the semiconductor channel may contain Si, Ge, C; an alloy of Ge and Si; an alloy of Si and C; and an alloy of Ge and C; or an alloy of Ge, Si, and C (Claim 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a group IV metal or an alloy thereof, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a Group IV semiconductor in the interfacial layer as pure compounds or alloys of pure compounds (Faulkner et al., Para. [0023]).

Regarding claim 6, Faulkner et al. teach the contact of claim 1, Faulkner et al. do not explicitly disclose wherein the group V atoms comprise any one of nitrogen, phosphorus, arsenic and antimony; or a mixture of any two or more of nitrogen, phosphorus, arsenic and antimony atoms. However Faulkner et al. teaches the use of Group V semiconductors in the interfacial layer as pure compounds or alloys of pure compounds (Para. [0023]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a group V metal or an alloy thereof, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a Group III-VI semiconductor in the interfacial layer as pure compounds or alloys of pure compounds (Faulkner et al., Para. [0023]).

Regarding claim 12, Faulkner et al. teach the method of claim 11, wherein a oriented surface of the group IV semiconductor (Si surface of layer 26, Paras. [0075]-[0076]) is etched with a crystallographically selective etch (etched with an etch for selective crystallographic orientation, Paras. [0069]-[0076]) to reveal and expose multiple {111} oriented semiconductor crystal facets (exposing {111} surfaces, Paras. [0069]-[0076]); the at least monolayer of group V atoms is formed on the {111} facets (the interfacial III-VI monolayer compound may be formed on the {111} semiconductor with approximate epitaxial alignment with the underlying, Paras. [0024];[0027];[0031];[0062]; [0069]-[0076]). Faulkner et al. do not explicitly disclose a {110} oriented surface and that the monolayer of group III atoms is subsequently deposited on the monolayer of group V atoms. However, Faulkner et al. teach that other surface orientations are possible (Para. [0071]), depositing bilayers of atoms with an atom of one group, such as Group III, is deposited and then capped with an atom of another group, such as Group VI (Paras. [0058]-[0062]) and depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surfaces so as to be epitaxially aligned therewith(Claim 13; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to modify a {110} surface and the deposition steps by depositing a group III atom monolayer on a monolayer of group V atoms, since selection of a known material on the basis of its suitability for an intended use and any order of process steps which did not result in a new or unexpected result would involve only routine skill in the art. The motivation for doing so would be to deposit an ultra-thin layer of a III-VI monolayered layers on the {110} surface transformed to a {111} surface so as to be epitaxially aligned therewith (Claim 13; Paras. [0031]-[0032]; [0058]-[0062];[0076]; Figs. 2a-2d).

Regarding claim 23, Faulkner et al. teach the contact of claim 1, Faulkner et al. do not explicitly disclose wherein the metal is one of: a metal silicide, a nickel silicide, a composition NiSi, a platinum silicide, a barrier metal consisting of tantalum nitride or titanium nitride or ruthenium, or a ferromagnetic metal comprising one or more of nickel, cobalt, iron and/or gadolinium. However, Faulkner et al. teach the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]) and the use of metals, such as Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, (Paras. [0063];[0077]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a metal or metal nitride as desired, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a metal of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Faulkner et al., Para. [0023]).

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Supplemental Box

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Regarding claim 27, Faulkner et al. teach an electrical contact (semiconductor device or transistor, Claim 1; Paras. [0022]-[0027]), comprising a metal (metal layer 42, Para. [0077]; Figs. 2a-2d; Claims 1 and 6) and a group IV semiconductor (layer 26 may contain silicon, Figs. 2a-2d; Claim 1; Paras. [0073]-[0075]) separated by either a monolayer of epitaxially aligned group V atoms or a bi-layer consisting of the monolayer of epitaxially aligned group V atoms and a monolayer of group III atoms at an interface between the metal and the semiconductor (layer 26 is separated from metal 42 at the interface by epitaxially aligned interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d). Faulkner et al. do not explicitly disclose that the metal is ferromagnetic. However, Faulkner et al. teach the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]) and the use of metals, such as Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, (Paras. [0063];[0077]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a metal as desired, such as a ferromagnetic metal, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a metal of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Faulkner et al., Para. [0023]).

Claims 2, 22, and 28-30 lack an inventive step under PCT Article 33(3) as being obvious over Faulkner et al. in view of Gaines et al.

Regarding claim 2, Faulkner et al. teach the contact of claim 1, Faulkner et al. do not explicitly disclose wherein the metal comprises atoms of the same metallic element as the monolayer of group III metal atoms. However, Faulkner et al. teach the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]); and, Gaines et al. teach a semiconductor device with substrates of germanium, group III-V and group II-VI metals and deposition layers of buried stressor layers, active layers and sacrificial stressor layers on the substrate (Claim 1; Paras. [0004];[0019];[0031]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a metal with group III atoms. The motivation for doing so would be to select a metal of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Faulkner et al., Para. [0023]).

Regarding claim 22, Faulkner et al. teach the contact of claim 11, Faulkner et al. do not explicitly disclose wherein after forming the monolayer of group V atoms and the monolayer of group III atoms, further metal atoms are deposited on the group III atoms, the further atoms being of a same metallic element as the monolayer of group III atoms or atoms of a metal element different from the monolayer layer of group III atoms. However, Faulkner et al. teach depositing bilayers of atoms with an atom of one group, such as Group III, is deposited and then capped with an atom of another group, such as Group VI (Paras. [0058]-[0062]) and depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surfaces so as to be epitaxially aligned therewith (Claim 13; Paras. [0031]-[0032]; [0060]-[0062];[0076]; Figs. 2a-2d); and, Gaines et al. teach a multiple layer device (Paras. [0027]-[0030]; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit additional layers of any of the group III-VI elements as monolayers one on top another in the desired configuration, as taught by Gaines et al. The motivation for doing so would be to deposit the group III-VI elements in monolayers to desired thickness (Faulkner et al., Paras. [0020]-[0021]; [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d).

Regarding claim 28, Faulkner et al. teach a method of forming an electrical contact (a method of forming a channel contact, Claim 13), comprising depositing, on a surface of a group IV semiconductor, which has been prepared so as to include atoms of a first group V material near the surface (the interfacial III-VI monolayer compound may be formed on the prepared {111} semiconductor silicon surface with approximate epitaxial alignment with the underlying surface, Paras. [0024];[0027];[0031];[0062];[0069]-[0076]), the atoms of the group V material being epitaxially aligned with a lattice structure of the semiconductor (the interfacial III-VI layered compound may be approximately epitaxially aligned with the underlying {111} semiconductor, Paras. [0024];[0027];[0031];[0062];[0067];[0076]), and depositing a metal on the monolayer of the group V material (the metal is deposited on the monolayer or bi-layered interfacial layer, Paras. [0024];[0027];[0031];[0062];[0077]), there being formed between the atoms of the group V material dipoles (the metal is deposited on the interfacial interfacial III-VI layer, Paras. [0024];[0027];[0031];[0062];[0077]). Faulkner et al. do not explicitly disclose a monolayer of a second group V material and that the metal has image charges. However, Faulkner et al. teach depositing bilayers of atoms with an atom of one group, such as Group III, is deposited and then capped with an atom of another group, such as Group VI (Paras. [0058]-[0062]), depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surfaces so as to be epitaxially aligned therewith (Claim 13; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d) and that the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]) and the use of metals, such as Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, (Paras. [0063];[0077]); and, Gaines et al. teach a multiple layer device (Paras. [0027]-[0030]; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a metal that would exhibit the appropriate charge and to deposit additional layers of any of the group III-VI elements as monolayers one on top another in the desired configuration, as taught by Gaines et al. The motivation for doing so would be to deposit the group III-VI elements in monolayers to desired thickness with the appropriately selected metal (Faulkner et al., Paras. [0020]-[0023]; [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d).

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Supplemental Box

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Regarding claim 29, Faulkner et al. in view of Gaines et al. teach the contact of claim 28, Faulkner et al. do not explicitly disclose wherein the first group V material and the second group V material are the same group V material. However, Faulkner et al. teach depositing bilayers of atoms with an atom of one group, such as Group III, is deposited and then capped with an atom of another group, such as Group VI (Paras. [0058]-[0062]) and depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surfaces so as to be epitaxially aligned therewith (Claim 13; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d); and, Gaines et al. teach a multiple layer device (Paras. [0027]-[0030]; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit additional layers of any of the group III-VI elements as monolayers one on top another in the desired configuration, as taught by Gaines et al. The motivation for doing so would be to deposit the group III-VI elements in monolayers to desired thickness (Faulkner et al., Paras. [0020]-[0021]; [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d).

Regarding claim 30, Faulkner et al. in view of Gaines et al. teach the contact of claim 28, Faulkner et al. teach wherein the group IV semiconductor is prepared by depositing the first group V material on the semiconductor (the interfacial III-VI monolayer compound may be deposited on the prepared {111} semiconductor silicon surface with approximate epitaxial alignment with the underlying surface, Paras. [0024];[0027];[0031];[0062];[0069]-[0076]; Claim 13) at a sufficiently high temperature that atoms of the first group V material enter the semiconductor (the interfacial III-VI monolayer is deposited at a sufficiently high temperature so as to be epitaxially aligned with the semiconductor, Claim 13; Paras. [0024];[0027];[0031];[0062];[0069]-[0076]).

Claims 13-21 and 26 lack an inventive step under PCT Article 33(3) as being obvious over Faulkner et al. in view of Joyce et al.

Regarding claim 13, Faulkner et al. teach the method of claim 11, Faulkner et al. do not explicitly disclose wherein the monolayer of group V atoms is produced by way of a vapor deposition process that includes exposing the group IV semiconductor to a vapor flux of the group V atoms or a flux of homonuclear molecules of the group V element generated by thermally evaporating a source of the group V element, or by a chemical reaction. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach a method of manufacturing a semiconductor device with epitaxial growth of a group II-V material (Claim 1; Col. 9, Lines 51-65) with the deposition of a group V material by vapor flux (Col. 5, Line 3-Col. 7, Line 53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom by the processes taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as vapor flux (Joyce et al., Col. 5, Line 3-Col. 7, Line 53).

Regarding claim 14, Faulkner et al. in view of Joyce et al. teach the method of claim 13, Faulkner et al. do not explicitly disclose wherein the flux of group V atoms/molecules is either a flux of arsenic molecules of composition As4 or As2 and the molecular flux is created by thermal evaporation of an elemental arsenic source in a Knudsen cell. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the flux of group V atoms/molecules is either a flux of arsenic molecules of composition As4 or As2 (flux of As2 or As4 atoms, Col. 6, Line 30-Col. 7, Line 15) and the molecular flux is created by thermal evaporation of an elemental arsenic source in a Knudsen cell (the arsenic source is evaporated in a Knudsen cell, Col. 5, Line 3-Col. 7, Line 53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom by the processes taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as vapor flux in a Knudsen cell (Joyce et al., Col. 5, Line 3-Col. 7, Line 53).

Regarding claim 15, Faulkner et al. teach the method of claim 11, Faulkner et al. do not explicitly disclose wherein the group V element atoms are deposited on the semiconductor surface by decomposition of a vapor phase compound of the group V element. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the group V element atoms are deposited on the semiconductor surface by decomposition of a vapor phase compound of the group V element (elements, such as group V, are deposited on the surface by decomposition of the vapor phase, Col. 3, Lines 35-57; Col. 6, Line 30-Col. 7, Line 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom by the processes taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as decomposition vapor flux in a Knudsen cell (Joyce et al., Col. 3, Lines 35-57; Col. 5, Line 3-Col. 7, Line 53).

Regarding claim 16, Faulkner et al. in view of Joyce et al. teach the method of claim 15, Faulkner et al. do not explicitly disclose wherein the compound of the group V element is a hydride of the group V element, and the group V hydride gas comprises one of ammonia, phosphine, arsine, or stibine. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the compound of the group V element is a hydride of the group V element (group V compounds as hydrides, Col. 9, Line 66-Col. 10, Line 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom hydrides, as taught by Joyce et al., such as ammonia, phosphine, arsine, or stibine. The motivation for doing so would be to deposit the layers by known deposition processes, such as as group V metal hydrides (Joyce et al., Col. 9, Line 66-Col. 10, Line 7).

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Regarding claim 17, Faulkner et al. in view of Joyce et al. teach the method of claim 16, Faulkner et al. do not explicitly disclose wherein the group V hydride gas comprises arsine (AsH4) and the surface of the semiconductor is heated to a temperature in the range 675 °C to 725 °C. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach heating the substrate to a temperature for desired growth, such as 650 °C (Col. 6, Line 55-Col. 7, Line 15) and that group V material hydrides, such as As2 and As4, may be used (Col. 6, Line 55-Col. 7, Line 15; Col. 9, Line 66-Col. 10, Line 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom hydride at temperatures sufficient to heat the substrate for the desired growth, as taught by Joyce et al., such as a substrate at a temperature of 675 °C to 725 °C subjected to a group V hydride, such as AsH4. The motivation for doing so would be to deposit the layers by known deposition processes, such as through use of a group V metal hydride at sufficient substrate growth temperatures (Joyce et al., Col. 6, Line 55-Col. 7, Line 15; Col. 9, Line 66-Col. 10, Line 7).

Regarding claim 18, Faulkner et al. in view of Joyce et al. teach the method of claim 17, Faulkner et al. do not explicitly disclose wherein the semiconductor is silicon and prior to depositing the arsenic atoms, the silicon surface is heated to a sufficiently high temperature in hydrogen gas to remove any silicon oxide or other contamination. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the semiconductor is silicon (the semiconductor is silicon, Col. 9, Lines 51-65) and prior to depositing the arsenic atoms, the silicon surface is heated to a sufficiently high temperature (the substrate is heated to a sufficiently high temperature prior to depositing arsenic atoms, (Col. 6, Line 55-Col. 7, Line 53) in hydrogen gas to remove any silicon oxide or other contamination (in an atmosphere to remove volatile oxides and undesired impurities, Col. 6, Line 10-Col. 7, Line 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to heat the substrate in an atmosphere, such as hydrogen, to remove undesired impurities and volatile oxides, such as silicon oxide, as generally taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as through use of heating of the substrate to remove volatile oxides and impurities (Joyce et al., Col. 6, Line 10-Col. 7, Line 53).

Regarding claim 19, Faulkner et al. in view of Joyce et al. teach the method of claim 15, Faulkner et al. do not explicitly disclose wherein the compound of the group V element is a metalorganic compound of the group V element. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the compound of the group V element (group V metal, Col. 2, Lines 45-68) is a metalorganic compound of the group V element (metal organic compound of a group V metal, Col. 2, Lines 45-68; Claims 7 and 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to use a metal organic compound of a group V element, as taught by Joyce et al. The motivation for doing so would be to use a group V compound metal organic (Joyce et al., Col. 2, Lines 45-68).

Regarding claim 20, Faulkner et al. in view of Joyce et al. teach the method of claim 19, Faulkner et al. do not explicitly disclose wherein the metalorganic compound of the group V element comprises tertiary butyl arsine (TBA) and the surface of the semiconductor is heated to a temperature in the range 500 °C to 610 °C. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach the use of a group V metal organic (Col. 2, Lines 45-68; Claims 7 and 14) and heating the substrate to a temperature of 650 °C (Col. 6, Line 55-Col. 7, Line 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to use a metal organic compound of a group V element, as taught by Joyce et al., such as tertiary butyl arsine, and to heat the substrate to a sufficient temperature, such as 650 °C, as taught by Joyce et al. The motivation for doing so would be to use a specific group V compound metal organic and to heat the substrate to sufficient temperatures (Joyce et al., Col. 2, Lines 45-68; Col. 6, Line 55-Col. 7, Line 15).

Regarding claim 21, Faulkner et al. teach the method of claim 12, wherein the semiconductor is silicon (silicon semiconductor, Paras. [0042];[0073]) and prior to depositing the group V atoms (the interfacial III-VI monolayer compound may be formed on the {111} semiconductor with approximate epitaxial aligned with the underlying, Paras. [0024];[0027];[0031];[0062];[0069]-[0076]), the {111} oriented surface is cleaned in situ (Si surface of layer 26 is etched with an etch for selective crystallographic orientation to expose clean {111} surfaces, Paras. [0027];[0069]-[0076]) and the silicon is heated to a sufficiently high temperature to obtain a 7 X 7 reconstruction of the {111} silicon surface (annealed at a temperature sufficient to generate a 7X7 reconstruction of the {111} surfaces, Para. [0027]) after which the silicon is held at a temperature in the range of approximately 20 °C to 750 °C (the deposition is carried out a temperatures from 500 to 875 °C, Paras. [0062];[0076]). Faulkner et al. do not explicitly disclose that during exposure to a vapor flux of the group V atoms or a compound molecular vapor of the group V element. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach that during exposure to a vapor flux of the group V atoms or a compound molecular vapor of the group V element. (depositing by a vapor flux of group V atoms, Col. 5, Line 3-Col. 7, Line 53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom by the processes taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as vapor flux (Joyce et al., Col. 5, Line 3-Col. 7, Line 53).

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Regarding claim 26, Faulkner et al. in view of Joyce et al. teach the method of claim 19. Faulkner et al. further teach wherein the group VI atoms comprise any one or more of sulfur, selenium or tellurium (Group VIA elements include O, S, Se, Te and Po, Para. [0023]) and/or the group II atoms comprise zinc or cadmium, or an alloy of zinc and cadmium.

Claims 1-30 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.

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Search History:

Limited Classification Search

The Patent Analyst performed a limited classification search within the following US, IPC, ECLA, or F-Term classification areas:

U.S. Class/Subclass(es): 148/33.5; 257/14, E21.097, E21.54, E21.108, E21.546, 344, 407, 408, 412, 592, 929; 438/3, 424, 603-607

IPC (8) Class/Subclass(es): H01L 21/20, 21/28, 21/205, 21/285, 21/318, 21/762, 21/765, 33/28, 33/30 (2012.01)

See Global Search Results.

Global Patent Literature Text Search

The Patent Analyst performed the following global text search, which was not limited by classification but may or may not have been limited by other criteria:

MICROPATENT

47	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	257014
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
46	9 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
45	2397 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

44	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	257412
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
43	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	257408
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
42	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	257344
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
41	2 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	257407
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
40	2 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	1.80E+308
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

39	30 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	1.80E+308
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
38	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	1.80E+308
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
37	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	1.80E+308
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
36	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	1.80E+308
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
35	16 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	1.80E+308
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

34	2 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	1.80E+308
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
33	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	148DIG142
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
32	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	1480335
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
31	2 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	438607
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
30	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	438607
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

29	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	438605
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
28	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	438606
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
27	2 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	438606
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
26	5 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	438605
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
25	10 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	438604
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

24	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	438003
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
23	15 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	438003
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
22	3 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	438603
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
21	3 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current US Class	438424
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
20	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L003328
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

19	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L003330
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
18	21 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L003330
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
17	45 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L003328
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
16	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L002285
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
15	197 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L002120
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

14	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L0021765
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
13	24 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L0021318
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
12	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021318
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
11	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021765
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
10	2 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L002120
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

9	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021285
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
8	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021205
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
7	132 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L0021205
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
6	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021762
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
5	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L002128
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

4 56 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
	Current IPC-R	H01L002128
	Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
	Years	1836-2012
3 28 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
	Current IPC-R	H01L0021762
	Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
	Years	1836-2012
2 538 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride
	Current IPC-R	H01L0021762
	Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
	Years	1836-2012
1 702 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal
	Current IPC-R	H01L0021762
	Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
	Years	1836-2012

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1	2011/0092047	**11/28/2012**	Google Patents
485	semiconductor group V epitaxial layer metal nitride flux arsenic	**11/28/2012**	Google Patents
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Date search was completed: 29 November 2012

YLK/BT

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC13

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	75	75
UTILITY SEARCH FEE	2111	1	330	330
UTILITY EXAMINATION FEE	2311	1	380	380
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**785**

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

[0001] The present application is a CONTINUATION of U.S. Patent Application 16/506,022, filed July 9, 2019, which is a CONTINUATION of U.S. Patent Application 15/728,002, filed 10/9/2017, now U.S. Patent 10,388,748, which is a CONTINUATION of U.S. Patent Application No. 15/251,210, filed 8/30/2016, now U.S. Patent 9,812,542, which is a CONTINUATION of U.S. Patent Application No. 15/048,877, filed 2/19/2016, now U.S. Patent 9,905,691, which is a CONTINUATION of U.S. Patent Application No. 13/552,556, filed 7/18/2012, now U.S. Patent 9,425,277, which is a CONTINUATION of U.S. Patent Application No. 13/022,522, filed 2/7/2011, now U.S. Patent 8,431,469, which is a DIVISIONAL of U.S. Patent Application 12/197,996, filed 8/25/2008, now U.S. Patent 7,884,003, which is a DIVISIONAL of U.S. Patent Application 11/181,217, filed 7/13/2005, now U.S. Patent 7,462,860, which is a CONTINUATION of U.S. Patent Application 10/217,758, filed 8/12/2002, now U.S. Patent 7,084,423, all of which are hereby incorporated by reference.

FIELD OF THE INVENTION

[0002] The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with

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a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

[0004] Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at T=0) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\varphi_B = \varphi_M - \chi_S \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the electron affinity of the semiconductor.

[0005] Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

[0006] Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination. FIG. 1 shows a

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cross-section of an un-passivated silicon surface labeled 100. The particular silicon surface shown is an Si(100) 2×1 surface. As shown, the silicon atoms at the surface, such as atom 110, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond 120. These dangling bonds may be responsible for surface states that trap electrical charges.

[0007] Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

[0008] For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0009] Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band

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structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

[0010] One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

[0011] The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

[0012] The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the

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effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention.

[0013] Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately 10 Ω-μm^2. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

[0014] In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia (NH3), nitrogen (N2) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

[0015] A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

[0016] Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer

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configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0018] FIG. 1 shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

[0019] FIG. 2 illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

[0020] FIG. 3 shows an energy band diagram for a conventional metal-n-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

[0021] FIG. 4 illustrates band bending at a conventional metal-n-type semiconductor junction.

[0022] FIG. 5 shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

[0023] FIG. 6 shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

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[0024] FIGS. 7*a*, 7*b*, 7*c* and 7*d* show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

[0025] FIG. 8 shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0027] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0028] The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally

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near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

[0029] The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal-interface layer-semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

[0030] It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for n- and p-type semiconductors, respectively), the IV characteristic will be nearly symmetric, especially at low voltage. In this case, the term "forward bias" is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

[0031] It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a p-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an n-type semiconductor. These junctions are diodes, in that little current will flow if the n-type (p-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The

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low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

[0032] Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

[0033] In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

[0034] The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

[0035] I. Introduction and Definitions

[0036] The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some

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important energy scales, which are shown graphically in FIG. 2. The so-called vacuum level (E0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (ΦM) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

[0037] As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

[0038] Now consider a conventional junction between a metal and an n-type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S<\Phi_M$). An n-type semiconductor is one in which electrons are the majority charge carriers (in p-type semiconductors, holes are the majority charge carrier). As shown in FIG. 3, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor 310 to the metal 320 when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) 330 forms near the junction interface 340.

[0039] The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see FIG. 4). The band bending creates an energy barrier (discussed above) that blocks further transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a

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p-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-n-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-p-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

[0040] As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor—interface layer—metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

[0041] This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

[0042] II. Passivation of Semiconductor Surfaces

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[0043] A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

[0044] However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

[0045] Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

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[0046] These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing n- and p-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

[0047] FIG. 5 shows a semiconductor device 510 that contains a semiconductor 530 and an interface layer 520 formed on a surface 540 of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

[0048] The semiconductor 530 contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

[0049] The semiconductor 530 has a surface 540 that is passivated by the interface layer 520. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface 540. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to

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provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor 530 is operable to be electrically coupled with a first voltage associated with the semiconductor device 510 and to conduct electrical current 550 across the passivated surface 540.

[0050] The interface layer 520 is formed on the semiconductor 530 and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

[0051] Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer 520 may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

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[0052] Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface 540.

[0053] In some cases, passivation of the semiconductor surface 540 will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

[0054] III. Forming Interface Layers

[0055] Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

[0056] A. Hydrogen and Fluorine

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[0057] An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

[0058] It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

[0059] An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

[0060] B. Nitrogen

[0061] In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300° C. and about 750° C., which is lower than temperatures conventionally used for Rapid

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Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH_3) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

[0062] According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10−9 Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900° C. and about 1000° C., or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

[0063] Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in

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the vacuum chamber before removal, at a substantially elevated temperature between about 700° C. and 1000° C., or higher.

[0064] Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

[0065] Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

[0066] IV. Diodes Containing Passivated Semiconductor Surfaces

[0067] Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, conductor-semiconductor junction, and multi-material junction are all related and appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

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[0068] As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

[0069] FIG. 6 shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.

[0070] The conductor 630 contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys), and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

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[0071] Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

[0072] Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

[0073] A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

[0074] The semiconductor-interface layer-conductor configuration illustrated in FIG. 6 defines what the present inventors have chosen to call a "passivated Schottky barrier". The passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

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[0075] Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

[0076] To understand why thickness of the interface layer is important, refer briefly to FIG. 8 where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

[0077] Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

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[0078] One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer 620 is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

[0079] Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

[0080] According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

[0081] For example, to make large-barrier diodes, for an n-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a p-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an

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interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

[0082] The use of interface layer 620 thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer 620, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

[0083] The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

[0084] According to one embodiment of the present invention then, the interface layer 620 is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current

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to be transferred across the interface layer.

[0085] There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

[0086] FIG. 7*a*-7*d* show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_S of the semiconductor. In FIG. 7*a*, an unpassivated Schottky barrier 700 is shown. In this example, the Fermi level (E_F) of the metal 730 is pinned in the bandgap of the semiconductor 710. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

[0087] In FIG. 7*b*, the interface layer 720*b* is thick enough to passivate dangling bonds at the surface of the semiconductor 710, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in FIG. 7*c*, when the interface layer 720*c* is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in FIG. 7*d*, when the interface layer 720*d*

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is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately Φ_M=4.1 eV and the electron affinity for Si of approximately χ_S=4.05 eV.

[0088] V. Transistors Containing Passivated Semiconductor Surfaces

[0089] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Pat. No. 6,833,556, issued Dec. 21, 2004, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed Jan. 14, 2003 by the present inventors, and assigned to the assignee of the present invention.

[0090] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n+-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in FIG. 7*d*). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0091] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide—semiconductor junction a Schottky barrier is formed

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which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

[0092] Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

[0093] The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

[0094] In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

[0095] Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described

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herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

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ABSTRACT

An electrical device in which an interface layer is disposed in between and in contact with a conductor and a semiconductor.

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CLAIMS

What is claimed is:

1. An electrical junction, comprising:

a semiconductor substrate;

a metal electrical contact to said semiconductor substrate; and

a passivating dielectric tunnel barrier layer between said semiconductor substrate and said metal electrical contact,

said semiconductor substrate being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer is configured to increase a height of a Schottky barrier for electrons between the metal electrical contact and the semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween.

2. The electrical junction of claim 1, wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si.

3. The electrical junction of claim 2, wherein the metal electrical contact comprises a metal having a work function near or substantially equal to a conduction band edge of the semiconductor.

4. The electrical junction of claim 3, wherein the metal having a work function near or substantially equal to a conduction band edge of the semiconductor comprises one of: aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn).

5. The electrical junction of claim 3, wherein the semiconductor substrate is doped p-type proximate to the electrical contact.

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6. The electrical junction of claim 3, wherein the semiconductor substrate is undoped proximate to the electrical contact.

7. An electrical junction, comprising:

a semiconductor substrate;

a metal electrical contact to said semiconductor substrate;

and a passivating dielectric tunnel barrier layer between said semiconductor substrate and said metal electrical contact,

said semiconductor substrate being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer is configured to increase a height of a Schottky barrier for holes between the metal electrical contact and the semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween.

8. The electrical junction of claim 7, wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si.

9. The electrical junction of claim 8, wherein the metal electrical contact comprises a metal having a work function near or substantially equal to a valence band edge of the semiconductor.

10. The electrical junction of claim 9, wherein the metal having a work function near or substantially equal to a valence band edge of the semiconductor comprises one of: platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Go), or palladium (Pd).

11. The electrical junction of claim 9, wherein the semiconductor substrate is doped n-type proximate to the electrical contact.

12. The electrical junction of claim 9, wherein the semiconductor substrate is undoped proximate to the electrical contact.

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Electronic Acknowledgement Receipt

EFS ID:	39151392
Application Number:	16847878
International Application Number:	
Confirmation Number:	8164
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC13
Receipt Date:	14-APR-2020
Filing Date:	
Time Stamp:	12:15:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$785
RAM confirmation Number	E20204DC16068607
Deposit Account	
Authorized User	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	3771-0003-DC13_ADS.pdf	1226953 33389a2fcb383816b9ec6a8d4a08acff3336dc26	no	9
Warnings:					
Information:					
2	Drawings-only black and white line drawings	3771-0003-DC13_Figures.pdf	144859 2b898120e44a0f06e1fbb344198b0666cb77e4d4	no	6
Warnings:					
Information:					
3	Oath or Declaration filed	3771-0003-DC12_Exe_Dec-Assign.pdf	178410 078bd17088bd887245b4dd455f30cab8a1ee5b87	no	4
Warnings:					
Information:					
4	Transmittal Letter	3771-0003-DC13_IDS_Statement.pdf	85327 25367101ea0fc52e5260e3db7f621b5591324011	no	2
Warnings:					
Information:					
5	Information Disclosure Statement (IDS) Form (SB08)	3771-0003-DC13_IDS.pdf	372110 c871bb87d2c5d5dfae70427557393468beb47b56	no	12
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
6	Foreign Reference	WO2002043109.pdf	1003560 1ec77ec8cd0afd818aa046b493d790d5c996b8cd	no	24
Warnings:					

Information:					
7	Other Reference-Patent/App/Search documents	3771-0017-PCT_ISR_and_Written_Opinion_mailed_12-24-12.pdf	3198873 22114e67c86087fe4908dd6b6f93cf85a990ecbe	no	23
Warnings:					
Information:					
8	Non Patent Literature	MCKINLEY_1992.pdf	244430 1bf69ce766e60cdb6f9893a5e997cd92197ee3dc	no	4
Warnings:					
Information:					
9	Non Patent Literature	GB1409999-8_Exam_Rpt.pdf	224888 1895f36534674e20858d1b7bef94e14fd9cc12e3	no	5
Warnings:					
Information:					
10	Non Patent Literature	MCKINLEY_1990.pdf	644049 9ea15b3a80022e5a6c5d77afcd615cc45ead9057	no	5
Warnings:					
Information:					
11	Fee Worksheet (SB06)	fee-info.pdf	35110 bc5b161c2b81723924946c798c256c178e2e14a	no	2
Warnings:					
Information:					
12	Specification	e528ce79-815b-4001-95ba-0ca5901dc7c6.docx	40299 db0023a77286d8449a8b322d0421bf2b75d233b4c5b498160f30c68de72320b8541471f70f21e1e47863bc84947c433d44d45aa46db9a3d019cfaee25bc5017b	no	27
Warnings:					
Information:					
13	Specification	be3692ca-d5f5-4be3-978b-d86368551b27.pdf	302637 b51359c85ad8f2ec7fa85fef51c05604d41bafd1	no	27
Warnings:					
Information:					

14	Abstract	ee217216-098a-4e6f-a918-cb333f409d6a.docx	16749 62127bbd547d588f8f6519fc85a2d2def892cf55aeca47a6d36667c33155010e3c8a5e743fa3e7291cabf16283edabed06a0211c1d8cdb9668d9372a8f7ed74d	no	1
Warnings:					
Information:					
15	Abstract	990e9175-50f2-467b-bf49-4ee6a3c1aeeb.pdf	84833 37fe22282c7904b824be18d396af0a56f42fe507	no	1
Warnings:					
Information:					
16	Claims	1a99f9f2-2875-4d54-97a9-a424483f055d.docx	19876 3c51dc1210213ddc665de20bd0875843f72778eafc73f134a05c50cd5c13c5713341ac8f97e87c3fff4ddad789c1a1216770b48462270beb82fe9e2c79f72f85	no	-
Warnings:					
Information:					
17	Claims	614c21ba-5873-4462-9e4d-f334d32004f6.pdf	91283 b091598d1776e7073914608ca90c9ac3da655857	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	7914246		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Daniel	E.	Grupp	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Palo Alto	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	455 Cambridge Ave.		
Address 2			
City	Palo Alto	State/Province	CA
Postal Code	94306	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Daniel	J.	Connelly	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Redwood City	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	455 Cambridge Ave.		
Address 2			
City	Palo Alto	State/Province	CA
Postal Code	94306	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	27571		
Email Address	patents@ascendalaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS		
Attorney Docket Number	3771-0003-DC13	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	27571		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
	Continuation of	16506022	2019-07-09	

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16506022	Continuation of	15728002	2017-10-09	10388748	2019-08-20

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15728002	Continuation of	15251210	2016-08-30	9812542	2017-11-07

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15251210	Continuation of	15048877	2016-02-19	9905691	2018-02-27

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15048877	Continuation of	13552556	2012-07-18	9425277	2016-08-23

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13552556	Continuation of	13022522	2011-02-07	8431469	2013-04-30

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13022522	Division of	12197996	2008-08-25	7884003	2011-02-08

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12197996	Division of	11181217	2005-07-13	7462860	2008-12-09

Prior Application Status	Patented			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11181217	Continuation of	10217758	2002-08-12	7084423	2006-08-01

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

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Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Acorn Semi, LLC		
Mailing Address Information For Applicant:			
Address 1	455 Cambridge Ave.		
Address 2			
City	Palo Alto	**State/Province**	CA
Country	US	Postal Code	94306
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Tarek N. Fahmi/			Date (YYYY-MM-DD)	2020-04-14
First Name	Tarek	Last Name	Fahmi	Registration Number	41402

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

GF Exhibit 1126 - 104/2248

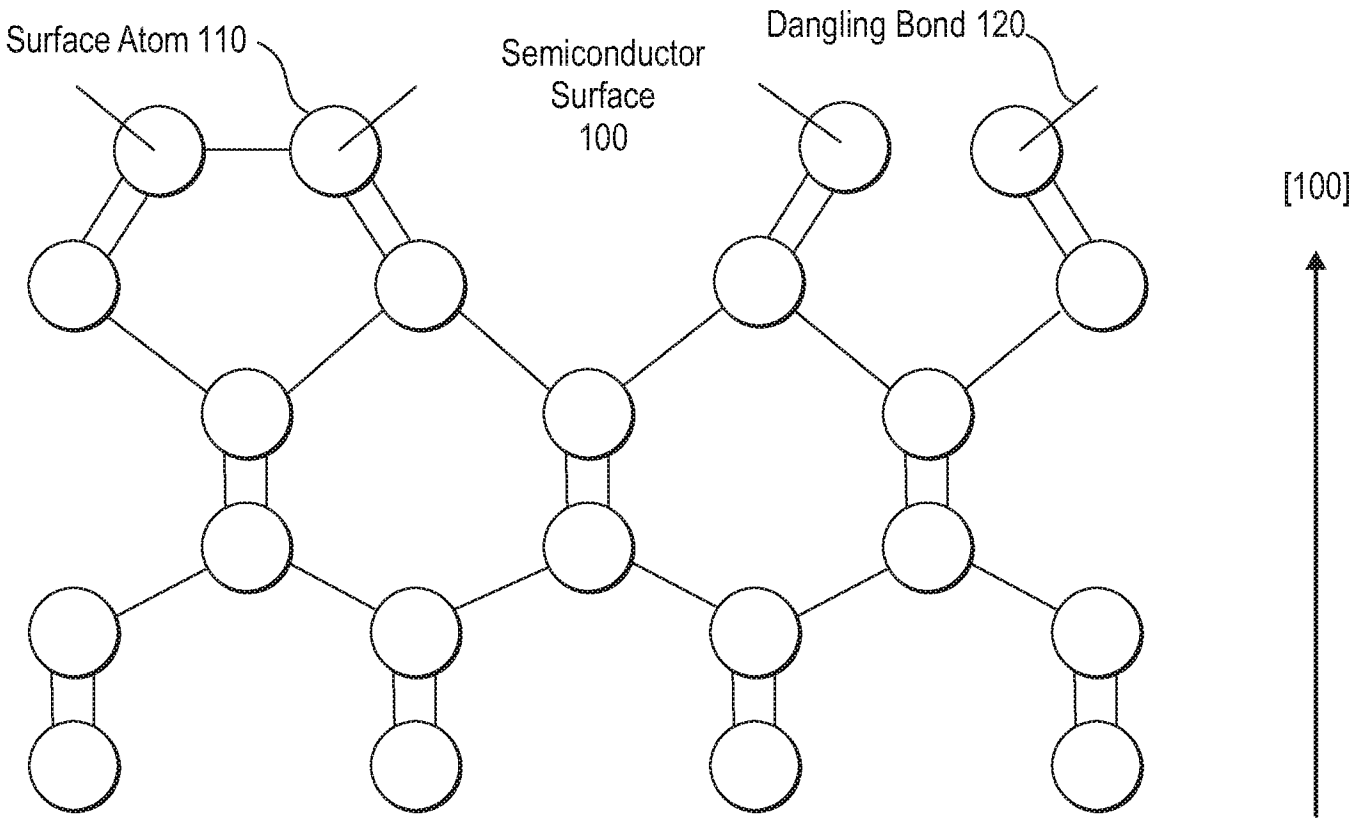


Fig. 1

GF Exhibit 1126 - 105/2248

Energy Scales for Metal - Semiconductor Junctions

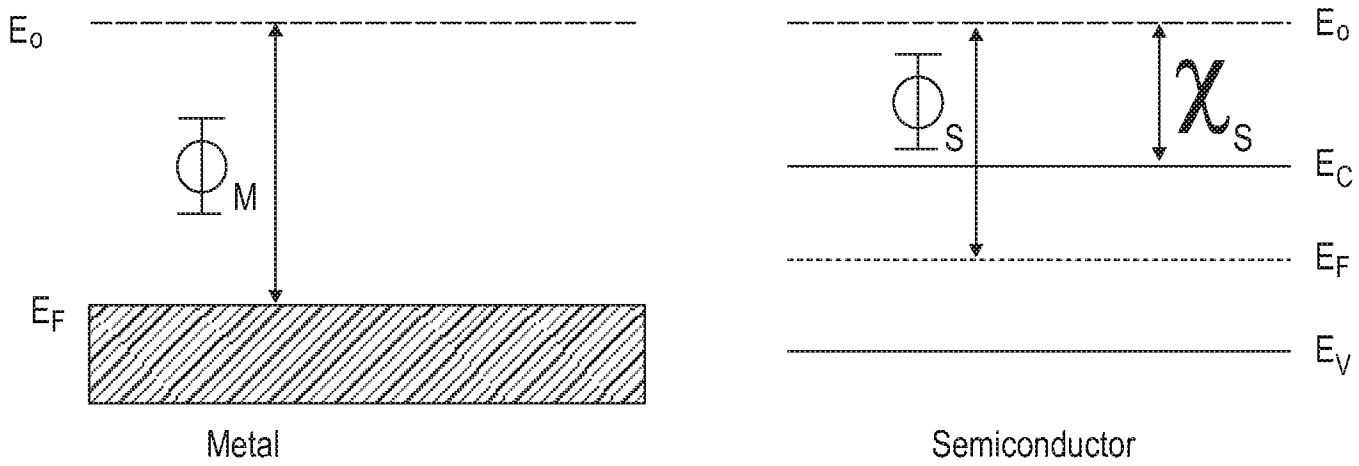


Fig. 2

GF Exhibit 1126 - 106/2248

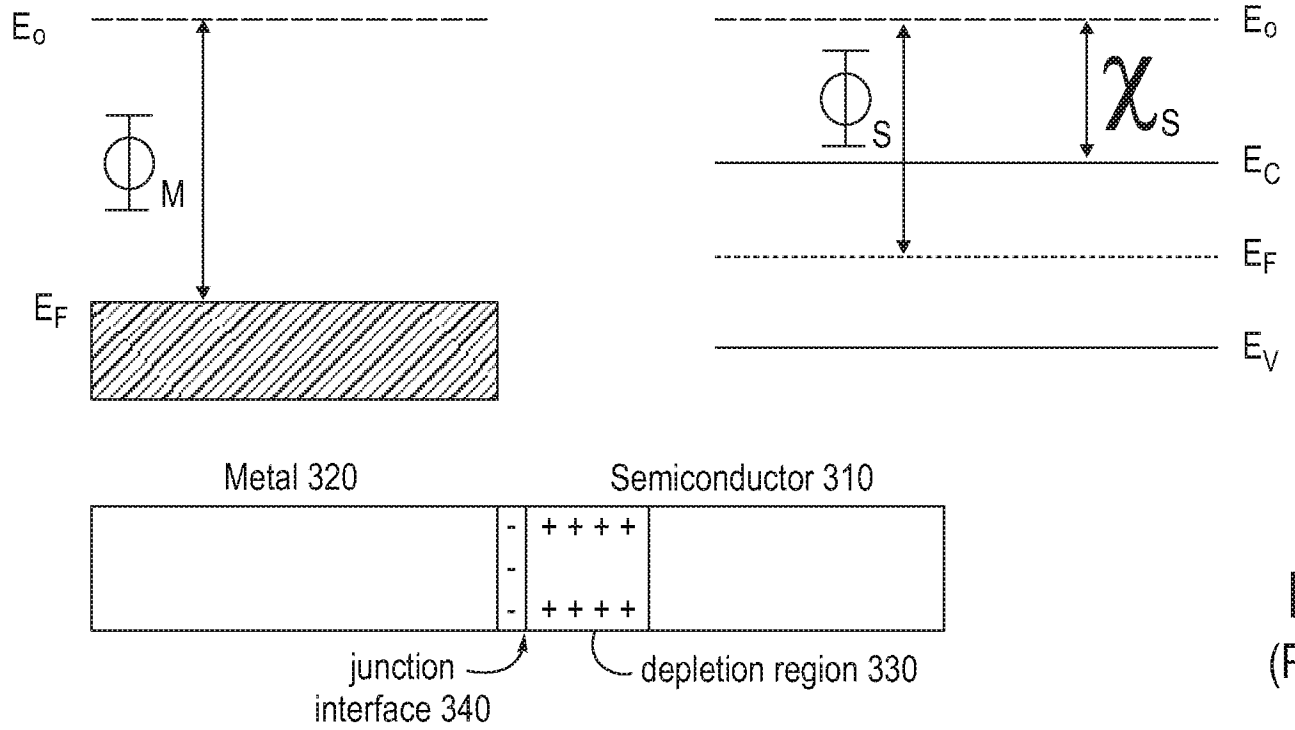


Fig. 3
(Prior Art)

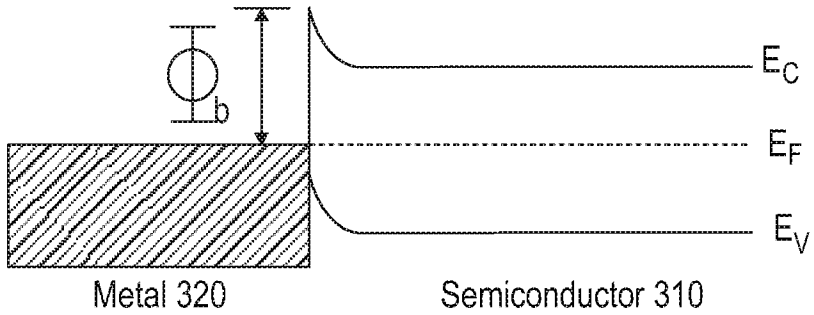


Fig. 4
(Prior Art)

GF Exhibit 1126 - 107/2248

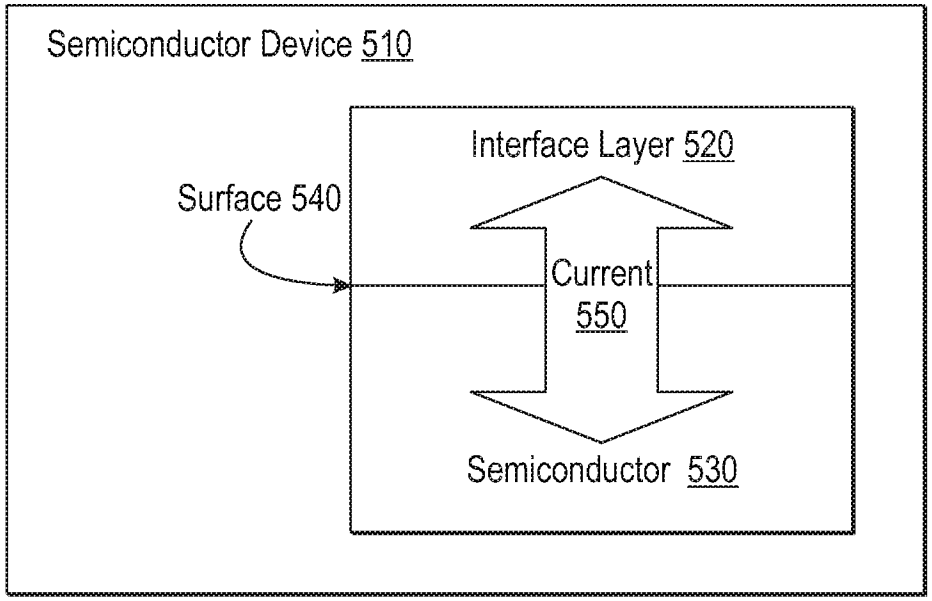


Fig. 5

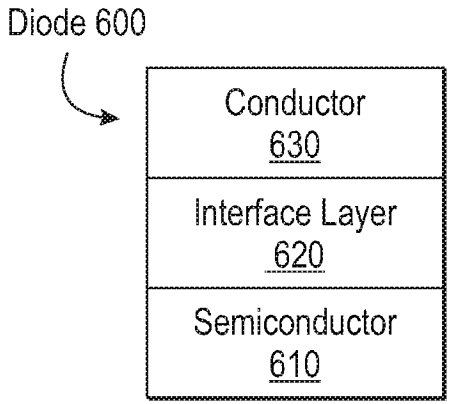


Fig.6

GF Exhibit 1126 - 108/2248

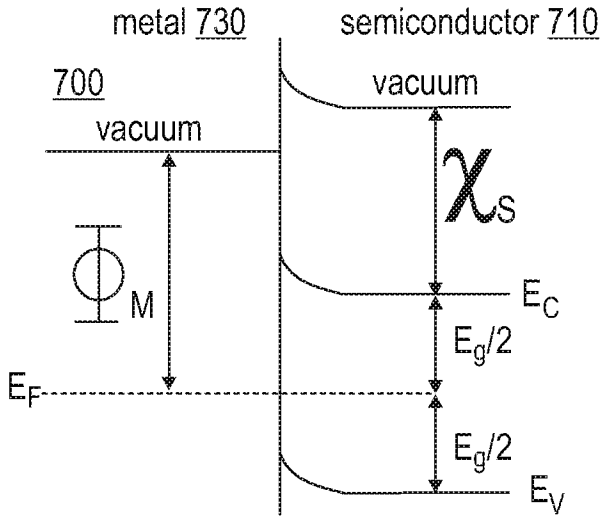


Fig. 7a

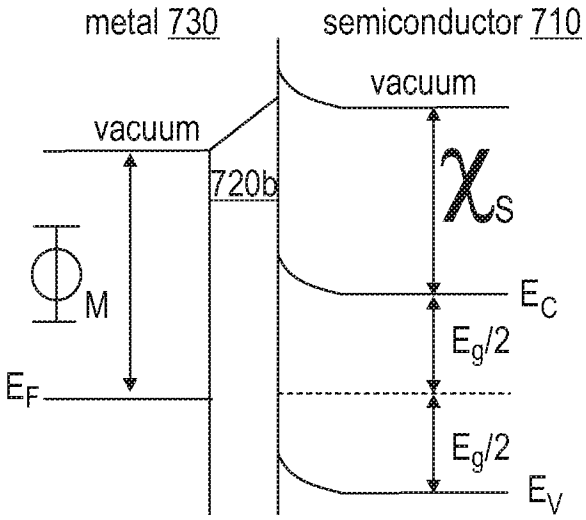


Fig. 7b

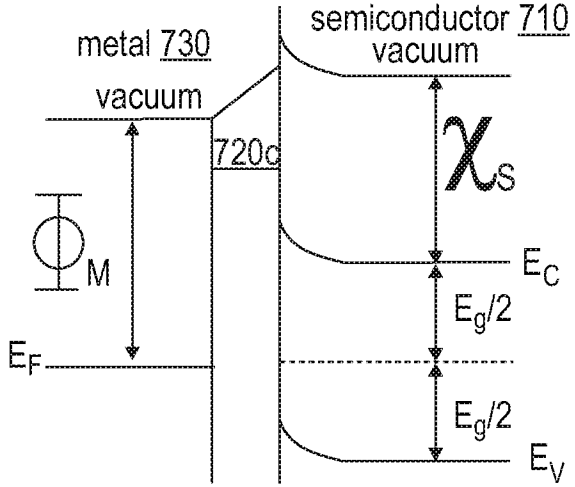


Fig. 7c

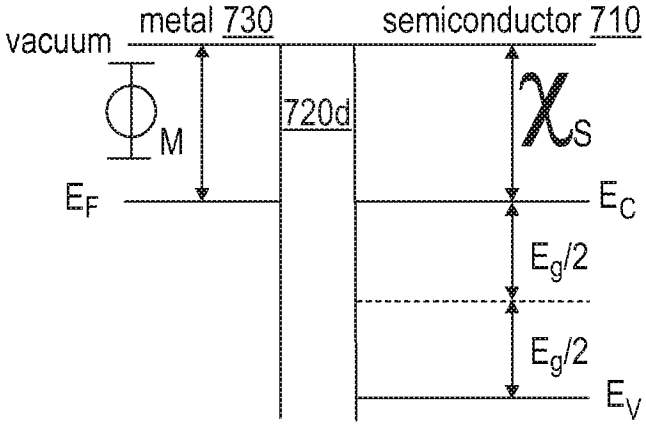


Fig. 7d

GF Exhibit 1126 - 109/2248

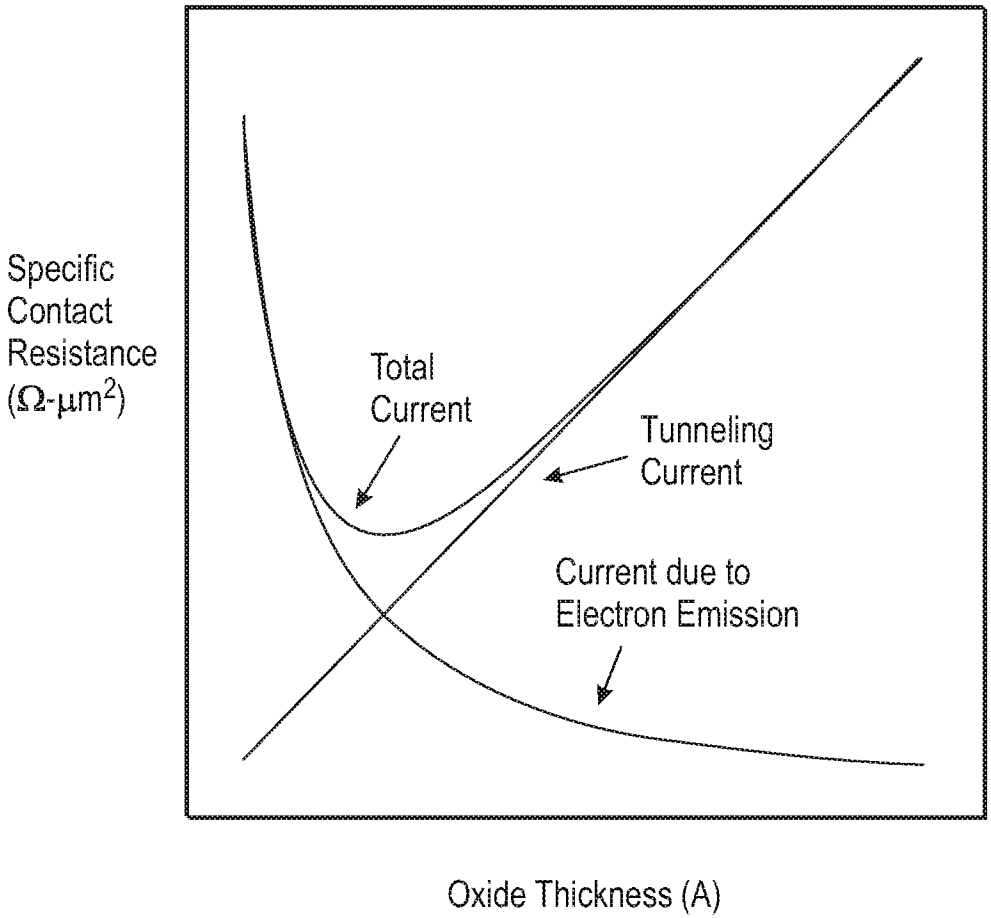


Fig. 8

GF Exhibit 1126 - 110/2248

Docket No.: 40003771-0003-473

Combined Declaration and Assignment for Utility and Design Patent Applications

DECLARATION

As a below named inventor, I hereby declare that:

I believe I am the original inventor or an original joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

Insert Title: **Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions**

the application of which is attached hereto unless the following is checked

☐ was filed on _____ as United States Application Number _____ and was filed on _____ as PCT International Application Number _____ and was amended on _____ (if applicable).

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under section 1001 of title 18 by fine or imprisonment of not more than 5 years, or both.

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the adequacy and receipt of which is hereby acknowledged by the undersigned inventor(s) (hereinafter ASSIGNOR) by

Insert Assignee(s) Name/Address:
Acorn Technologies, Inc.
330 Wilshire Boulevard, 2nd Floor
Santa Monica, CA 90401

(hereinafter ASSIGNEE), the undersigned ASSIGNOR hereby sells, assigns and transfers to ASSIGNEE the entire and exclusive right, title and interest to the above-identified application (e.g., provisional or non-provisional) and all Letters Patent of the United States to be obtained therefore on said application or any continuation, divisional, substitute, reissue , reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof for the full term or terms for which the same may be granted.

The ASSIGNOR agrees to execute all papers necessary in connection with the application and any continuation, divisional, reissue, reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof and also to execute separate assignments in connection with such applications as the ASSIGNEE may deem necessary or expedient.

The ASSIGNOR agrees to execute all papers necessary in connection with any interference, litigation, or other legal proceeding which may be declared concerning this application or any continuation, divisional, reissue or reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof or Letters Patent or reissue patent issued thereon and to cooperate with the ASSIGNEE in every way possible in obtaining and producing evidence and proceeding with such interference, litigation, or other legal proceeding.

The ASSIGNOR sells, assigns and transfers to said ASSIGNEE the entire and exclusive right, title and interest to the application(s) and the invention(s) disclosed therein for the United States of America and all countries foreign to the United States and do hereby authorize said ASSIGNEE to apply for patents therefore in its own name in countries where such procedure is proper and to claim the priority right under the International Convention and agrees to execute all papers

GF Exhibit 1126 - 111/2248

necessary in connection with applications for such patents and any continuation, divisional, substitute, reissue or reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof and also execute separate assignments in connection with such applications as the ASSIGNEE may deem necessary or expedient.

Hereby executed by the undersigned on the date opposite the undersigned name:

Legal Name of inventor ⇨ Daniel E. Grupp Date: 17 NOV 2012

Inventor's Signature ⇨ _____

Legal Name of inventor ⇨ Daniel J. Connelly Date: _____

Inventor's Signature ⇨ _____

GF Exhibit 1126 - 112/2248

Docket No.: 40003771-0003 - 473

Combined Declaration and Assignment for Utility and Design Patent Applications

DECLARATION

As a below named inventor, I hereby declare that:

I believe I am the original inventor or an original joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

Insert Title: **Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions**

the application of which is attached hereto unless the following is checked

☐ was filed on _____ as United States Application Number _____ and was filed on _____ as PCT International Application Number _____ and was amended on _____ (if applicable).

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under section 1001 of title 18 by fine or imprisonment of not more than 5 years, or both.

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the adequacy and receipt of which is hereby acknowledged by the undersigned inventor(s) (hereinafter ASSIGNOR) by

Insert Assignee(s) Name/Address:

Acorn Technologies, Inc.
330 Wilshire Boulevard, 2nd Floor
Santa Monica, CA 90401

(hereinafter ASSIGNEE), the undersigned ASSIGNOR hereby sells, assigns and transfers to ASSIGNEE the entire and exclusive right, title and interest to the above-identified application (e.g., provisional or non-provisional) and all Letters Patent of the United States to be obtained therefore on said application or any continuation, divisional, substitute, reissue , reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof for the full term or terms for which the same may be granted.

The ASSIGNOR agrees to execute all papers necessary in connection with the application and any continuation, divisional, reissue, reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof and also to execute separate assignments in connection with such applications as the ASSIGNEE may deem necessary or expedient.

The ASSIGNOR agrees to execute all papers necessary in connection with any interference, litigation, or other legal proceeding which may be declared concerning this application or any continuation, divisional, reissue or reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof or Letters Patent or reissue patent issued thereon and to cooperate with the ASSIGNEE in every way possible in obtaining and producing evidence and proceeding with such interference, litigation, or other legal proceeding.

The ASSIGNOR sells, assigns and transfers to said ASSIGNEE the entire and exclusive right, title and interest to the application(s) and the invention(s) disclosed therein for the United States of America and all countries foreign to the United States and do hereby authorize said ASSIGNEE to apply for patents therefore in its own name in countries where such procedure is proper and to claim the priority right under the International Convention and agrees to execute all papers

GF Exhibit 1126 - 113/2248

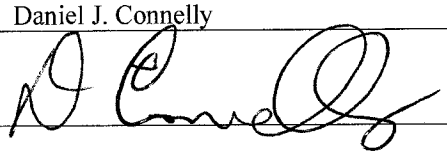
necessary in connection with applications for such patents and any continuation, divisional, substitute, reissue or reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof and also execute separate assignments in connection with such applications as the ASSIGNEE may deem necessary or expedient.

Hereby executed by the undersigned on the date opposite the undersigned name:

Legal Name of inventor ⇨ Daniel E. Grupp Date: _____

Inventor's Signature ⇨ _____

Legal Name of inventor ⇨ Daniel J. Connelly Date: 11 Oct 2012

Inventor's Signature ⇨ 

Legal Name of inventor ⇨ _____ Date: _____

Inventor's Signature ⇨ _____

Legal Name of inventor ⇨ _____ Date: _____

Inventor's Signature ⇨ _____

GF Exhibit 1126 - 114/2248

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Daniel E. Grupp

Application No.: Not Yet Assigned
Filed: Herewith

Examiner: Not Yet Assigned
Art Unit: Not Yet Assigned

Docket No.: 3771-0003-DC13

Customer No.: 27571

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g. copies of U.S. patents and U.S. published patent applications that need not be included and copies of Non Patent Literature documents that were previously provided in parent application nos. 13/552,556 filed 7/18/2012 and 13/022,522 filed 2/7/2011). This IDS and IDS Citation Form are being submitted before the mailing of a First Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account No. 50-5798.

Respectfully submitted,

Date: April 14, 2020

/Tarek N. Fahmi/
Tarek N. Fahmi, Reg. No. 41,402

ASCENDA LAW GROUP, PC
333 W. San Carlos St., Suite 200
San Jose, CA 95110-2730
(866) 877-4883

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/847,878

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	330		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	12 minus 20 =	*	x 50 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*	x 230 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	785		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/847,878	04/14/2020	2811	785	3771-0003-DC13	12	2

CONFIRMATION NO. 8164

FILING RECEIPT

27571
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

OC000000118409865

Date Mailed: 04/23/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

Applicant(s)

Acorn Semi, LLC, Palo Alto, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 16/506,022 07/09/2019
which is a CON of 15/728,002 10/09/2017 PAT 10388748
which is a CON of 15/251,210 08/30/2016 PAT 9812542
which is a CON of 15/048,877 02/19/2016 PAT 9905691
which is a CON of 13/552,556 07/18/2012 PAT 9425277
which is a CON of 13/022,522 02/07/2011 PAT 8431469
which is a DIV of 12/197,996 08/25/2008 PAT 7884003
which is a DIV of 11/181,217 07/13/2005 PAT 7462860
which is a CON of 10/217,758 08/12/2002 PAT 7084423

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

GF Exhibit 1126 - 118/2248

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/21/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/847,878**

Projected Publication Date: 07/30/2020

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign

patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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GF Exhibit 1126 - 120/2248

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GF Exhibit 1126 - 121/2248

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/847,878
Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	

Sheet	1	of	24	**Attorney Docket No:** 3771-0003-DC13

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2981877	1961-04-25	Noyce	
		3614548	1971-10-19	Inoue	
		3623925	1971-11-30	Jenkins, et al.	
		3719797	1973-03-06	Andrews, Jr., et al.	
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		3983264	1976-09-28	Schroen, et al.	
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		4960732	1990-10-02	Dixit, et al.	
		4961194	1990-10-02	Kuroda, et al.	

EXAMINER SIGNATURE **DATE CONSIDERED**

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Sheet	2	of	24	**Attorney Docket No:** 3771-0003-DC13

		5013685	1991-05-07	Chiu, et al.	
		5019530	1991-05-28	Kleinsasser, et al.	
		5021840	1991-06-04	Morris	
		5045502	1991-09-03	Lau, et al.	
		5086321	1992-02-04	Batey, et al.	
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		5238872	1993-08-24	Thalapaneni	
		5292677	1994-03-08	Dennison	
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		5355021	1994-10-11	Crouch, et al.	
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		5534449	1996-07-09	Dennison, et al.	
		5563448	1996-10-08	Lee, et al.	
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		5619057	1997-04-08	Komatsu	
		5654234	1997-08-05	Shih, et al.	
		5677553	1997-10-14	Yamamoto, et al.	
		5689125	1997-11-18	Vaccaro, et al.	
		5744817	1998-04-28	Shannon	
		5789312	1998-08-04	Buchanan, et al.	
		5793109	1998-08-11	Nakamura	

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Sheet	3	of	24	**Attorney Docket No:** 3771-0003-DC13

		5793788	1998-08-11	Inaba, et al.	
		5851912	1998-12-22	Liaw, et al.	
		5869364	1999-02-09	Nakano, et al.	
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		6274905	2001-08-14	Mo	
		6284557	2001-09-04	Yiu, et al.	
		6287946	2001-09-11	Micovic, et al.	
		6303942	2001-10-16	Farmer, II	
		6320238	2001-11-20	Kizilyalli, et al.	

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Examiner Name	

Sheet	4	of	24	**Attorney Docket No:** 3771-0003-DC13

		6346465	2002-02-12	Miura, et al.	
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		7863606	2011-01-04	Sung	
		9209261	2015-12-08	Grupp, et al.	

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Sheet	5	of	24	**Attorney Docket No:** 3771-0003-DC13

		20010030342	2001-10-18	Ohnishi, et al.	
		20010030352	2001-10-18	Ruf, et al.	
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		20040038467	2004-02-26	Darwish, et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		EP 0 042 066 A2	1981-12-23	IBM		

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Sheet	6	of	24	**Attorney Docket No:** 3771-0003-DC13

		EP 0 068 897 A2	1983-01-05	HITACHI LTD		
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		JP 2002-151428 A	2002-05-24	TOSHIBA CORP		X

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		JP 2002-184978 A	2002-06-28	TOSHIBA CORP		X
		JP 2002-217425 A	2002-08-02	SANKEN ELECTRIC CO LTD		X
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		JP H07-122519 A	1995-05-12	OMI TADAHIRO		X
		JP H07-263375 A	1995-10-13	TELEFUNKEN MICROELECTRON		X
		JP H08-64800 A	1996-03-08	HITACHI LTD		X
		JP H08-167693 A	1996-06-25	SHARP KK		X
		JP H09-289178 A	1997-11-04	MATSUSHITA ELECTRIC IND CO LTD		X
		JP H10-27847 A	1998-01-27	MITSUBISHI ELECTRIC CORP		X
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		JP H10-135452 A	1998-05-22	IBM		X
		JP H10-209445 A	1998-08-07	NEC CORP		X

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		KR 10-0197653 B1	1999-06-15	HYUNDAI ELECTRONICS IND		X
		KR 10-0290467 B1	2001-03-02	HYNIX SEMICONDUCTOR INC		X
		KR 92-002350 B1	1992-03-21	PANASONIC CORPORATION		X
		KR 1991-0006249 B1	1991-08-17	HITACHI, LTD.		X
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		KR 1994-0020550 A	1994-09-16	SAMSUNG ELECTRONICS CO., LTD.		X
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		KR 2000-0025576 A	2000-05-06	SAMSUNG ELECTRONICS CO LTD		X

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		SE 0875077 T3	2004-01-07	ABB RESEARCH LTD.		X
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		WO 01/63677 A1	2001-08-30	CENTRE NAT RECH SCIENT; et al.		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T2**
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Complete if Known	
Application Number	16/847,878
Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	

Sheet	21	of	24	**Attorney Docket No:** 3771-0003-DC13

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First Named Inventor	Daniel E. Grupp
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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-06-17
Name/Print	Tarek N. Fahmi	Registration Number	41,402

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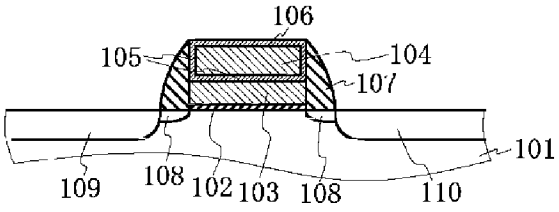
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(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号
(72)発明者　新村　俊樹
東京都港区芝五丁目７番１号　日本電気株式会社内
(72)発明者　松木　武雄
東京都港区芝五丁目７番１号　日本電気株式会社内
(74)代理人　100064621
弁理士　山川　政樹

(54)【発明の名称】　電界効果トランジスタおよびその製造方法

(57)【要約】
【課題】　電界効果トランジスタのゲート電極の材料に、トランジスタの特性を劣化させることなく銅を用いる。
【解決手段】　上部ゲート電極１０４は、下面と側面を覆うように窒化タンタルからなるバリア膜１０５が形成され、上面を覆うように窒化シリコンからなるバリア膜１０６が形成されている。



GF Exhibit 1126 - 146/2248

【特許請求の範囲】
【請求項１】　シリコン基板上にゲート絶縁膜を介して形成されたシリコンからなる下部ゲート電極と、
この下部ゲート電極上に形成された銅からなる上部ゲート電極と、
前記下部ゲート電極にチャネル部を駆動するに足りる電流が注入できる導電性を有して前記上部ゲート電極下面を覆うように形成された銅の拡散を阻止する第１のバリア膜と、
この第１のバリア膜に下端が接触して前記上部ゲート電極の両側面を覆うように形成された銅の拡散を阻止する第２のバリア膜と、
この第２のバリア膜に端部が接触して前記上部ゲート電極上面を覆うように形成された銅の拡散を阻止する第３のバリア膜と、
前記下部ゲート電極下の領域を挟むように前記シリコン基板に形成されたソース・ドレインとを備えたことを特徴とする電界効果トランジスタ。
【請求項２】　請求項１記載の電界効果トランジスタにおいて、
前記下部ゲート電極および上部ゲート電極側面に形成された側壁を備え、この側壁の一部で前記第２のバリア膜が構成されることを特徴とする電界効果トランジスタ。
【請求項３】　請求項１または２記載の電界効果トランジスタにおいて、
前記第３のバリア膜は絶縁材料から構成されたことを特徴とする電界効果トランジスタ。
【請求項４】　請求項３記載の電界効果トランジスタにおいて、
前記上部ゲート電極上面上を開放して前記シリコン基板上に形成された絶縁層を備え、
前記第３のバリア膜は前記絶縁層上に延在して形成されたことを特徴とする電界効果トランジスタ。
【請求項５】　請求項３または４記載の電界効果トランジスタにおいて、
前記第２，第３バリア膜は高融点金属もしくは高融点金属の窒化物から構成されていることを特徴とする電界効果トランジスタ。
【請求項６】　請求項１～５いずれか１項記載の電界効果トランジスタにおいて、
前記第１のバリア膜はトンネル電流が流れる厚さに形成された絶縁材料から構成されていることを特徴とする電界効果トランジスタ。
【請求項７】　請求項１記載の電界効果トランジスタにおいて、
前記第１，第２，および，第１のバリア膜は高融点金属もしくは高融点金属の窒化物から構成されていることを特徴とする電界効果トランジスタ。
【請求項８】　請求項２～６いずれか１項記載の電界効果トランジスタにおいて、
前記絶縁材料は、窒化シリコンもしくは窒化ボロンのいずれか１つから構成されたことを特徴とする電界効果トランジスタ。
【請求項９】　請求項１～８いずれか１項記載の電界効果トランジスタにおいて、
前記第１のバリア膜は２層以上の複数層からなる多層膜であることを特徴とする電界効果トランジスタ。
【請求項１０】　請求項１～８いずれか１項記載の電界効果トランジスタにおいて、
前記第１のバリア膜は、高融点金属からなる層または高融点金属シリサイドからなる層または高融点金属金属とシリコンと窒素との化合物からなる層もしくは高融点金属の窒化物からなる層のいずれかが組み合わされて複数層積層された多層膜であることを特徴とする電界効果トランジスタ。
【請求項１１】　請求項１０記載の電界効果トランジスタにおいて、
前記第１のバリア膜は、最下層が金属シリサイド層または高融点金属金属とシリコンと窒素との化合物からなる層から構成された多層膜であることを特徴とする電界効果トランジスタ。
【請求項１２】　請求項１１記載の電界効果トランジスタにおいて、
前記第１のバリア膜は、最下層が金属シリサイド層または高融点金属金属とシリコンと窒素との化合物からなる層から構成され、この金属シリサイドの層上に高融点金属の窒化物の層が配置された多層膜であることを特徴とする電界効果トランジスタ。
【請求項１３】　請求項１１記載の電界効果トランジスタにおいて、
前記第１のバリア膜は、最下層が金属シリサイド層または高融点金属金属とシリコンと窒素との化合物からなる層から構成され、この金属シリサイドの層または高融点金属金属とシリコンと窒素との化合物からなる層の上に高融点金属の窒化物の層が配置され、最上層が高融点金属から構成された多層膜であることを特徴とする電界効果トランジスタ。
【請求項１４】　請求項１～１３のいずれか１項に記載の電界効果トランジスタにおいて、
前記ソース・ドレイン表面の所定領域に高融点金属シリサイド膜が形成されていることを特徴とする電界効果トランジスタ。
【請求項１５】　シリコン基板上にゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、
前記下部ゲート電極上に犠牲パターンを形成する工程と、
前記下部ゲート電極および前記犠牲パターンをマスクとして前記シリコン基板の所定量域に不純物を導入するこ

とでソース・ドレインを形成する工程と、
前記下部ゲート電極および前記犠牲パターンを覆うように前記シリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、
前記第１の層間絶縁膜を除去して前記犠牲パターンの上面を露出させる工程と、
前記犠牲パターンを選択的に除去して前記下部ゲート電極上面を露出させて前記第１の層間絶縁膜の前記下部ゲート電極上部に溝を形成する工程と、
前記下部ゲート電極上面および前記溝側面を覆うように銅の拡散を阻止する導電性を有する第１，第２のバリア膜を形成する工程と、
前記溝内に前記第１，第２のバリア膜を介して銅からなる上部ゲート電極を形成して前記上部ゲート電極の底面および両側面が前記第１および第２のバリア膜に覆われた状態とする工程と、
前記上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項１６】　請求項１５記載の電界効果トランジスタの製造方法において、
前記犠牲パターンは、所定のエッチング処理条件において、シリコンおよび酸化シリコンより速くエッチングされる材料から構成することを特徴とする電界効果トランジスタの製造方法。
【請求項１７】　シリコン基板上にゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、
前記下部ゲート電極上にエッチングストッパー層を形成する工程と、
前記エッチングストッパー層上に犠牲パターンを形成する工程と、
前記下部ゲート電極および前記犠牲パターンをマスクとして前記シリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、
前記下部ゲート電極および前記犠牲パターンを覆うように前記シリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、
前記第１の層間絶縁膜を除去して前記犠牲パターンの上面を露出させる工程と、
前記犠牲パターンを選択的に除去して前記エッチングストッパー層上面を露出させる工程と、
前記エッチングストッパー層を除去して前記下部ゲート電極上面を露出させ前記下部ゲート電極上部に溝を形成する工程と、
前記下部ゲート電極上面および前記溝側面を覆うように銅の拡散を阻止する導電性を有する第１および第２のバリア膜を形成する工程と、
前記溝内に前記第１，第２のバリア膜を介して銅からなる上部ゲート電極を形成して前記上部ゲート電極の底面および両側面が前記第１および第２のバリア膜に覆われた状態とする工程と、
前記上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項１８】　シリコン基板上にゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、
前記下部ゲート電極上にエッチングストッパー層を形成する工程と、
前記エッチングストッパー層上に犠牲パターンを形成する工程と、
前記下部ゲート電極および前記犠牲パターンをマスクとして前記シリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、
前記下部ゲート電極および前記犠牲パターンを覆うように前記シリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、
前記第１の層間絶縁膜を選択的に除去して前記犠牲パターンの上面を露出させて前記下部ゲート電極上部に溝を形成する工程と、
前記犠牲パターンを選択的に除去して前記エッチングストッパー層上面を露出させる工程と、
前記エッチングストッパー層を除去して前記下部ゲート電極上面を露出させる工程と、
前記下部ゲート電極上面および前記溝側面を覆うように銅の拡散を阻止する導電性を有する第１および第２のバリア膜を形成する工程と、
前記溝内に前記第１，第２のバリア膜を介して銅からなる上部ゲート電極を形成して前記上部ゲート電極の底面および両側面が前記第１および第２のバリア膜に覆われた状態とする工程と、
前記上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項１９】　請求項１７または１８記載の電界効果トランジスタの製造方法において、
前記犠牲パターンは、所定のエッチング処理条件において、酸化シリコンより速くエッチングされる材料から構成することを特徴とする電界効果トランジスタの製造方法。
【請求項２０】　請求項１７～１９のいずれか１項に記載の電界効果トランジスタの製造方法において、
前記犠牲層，エッチングストッパー層，下部ゲート電極をハードマスクにより加工することを特徴とする電界効

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果トランジスタの製造方法。
【請求項２１】　請求項１７または１８に記載の電界効果トランジスタの製造方法において、
前記犠牲層，エッチングストッパー層，下部ゲート電極を酸化シリコンまたは窒化シリコンからなるハードマスクにより加工することを特徴とする電界効果トランジスタの製造方法。
【請求項２２】　請求項１５～２１のいずれか１項に記載の電界効果トランジスタの製造方法において、
前記下部ゲート電極上面が露出し、溝が形成された後、高融点金属膜を成膜する工程と、
この高融点金属膜上に高融点金属の窒化膜を成膜する工程と、
銅を成膜する工程と、
前記溝以外の領域の前記銅、前記高融点金属膜、前記高融点金属の窒化膜を除去し、前記銅からなる上部ゲート電極と前記高融点金属膜と前記高融点金属の窒化膜からなる第１および第２のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項２３】　請求項１５～２１のいずれか１項に記載の電界効果トランジスタの製造方法において、
前記下部ゲート電極上面が露出し、溝が形成された後、第１の高融点金属膜を成膜する工程と、
この第１の高融点金属膜上に高融点金属の窒化膜を成膜する工程と、
この高融点金属の窒化膜上に第２の高融点金属膜を成膜する工程と、
銅を成膜する工程と、
前記溝以外の領域の前記銅、前記第１の高融点金属膜、前記高融点金属の窒化膜，前記第２の高融点金属膜を除去し、前記銅からなる上部ゲート電極と前記第１の高融点金属膜，前記高融点金属の窒化膜，前記第２の高融点金属膜からなる第１および第２のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項２４】　請求項１５～２１のいずれか１項に記載の電界効果トランジスタの製造方法において、
前記下部ゲート電極上面が露出し、溝が形成された後、高融点金属とシリコンと窒素との化合物を成膜する工程と、
この高融点金属とシリコンと窒素との化合物の膜上に高融点金属の窒化膜を成膜する工程と、
前記上部ゲート電極となる銅を成膜する工程と、
前記溝以外の領域の前記銅、前記高融点金属膜、前記高融点金属膜の窒化膜を除去し、前記銅からなる上部ゲート電極と前記高融点金属膜と前記高融点金属の窒化膜からなる第１および第２のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項２５】　請求項１５～２１のいずれか１項に記載の電界効果トランジスタの製造方法において、
前記下部ゲート電極上面が露出し、溝が形成された後、高融点金属とシリコンと窒素との化合物を成膜する工程と、
この高融点金属とシリコンと窒素との化合物の膜上に高融点金属の窒化膜を成膜する工程と、
この高融点金属の窒化膜上に高融点金属膜を成膜する工程と、
前記上部ゲート電極となる銅を成膜する工程と、
前記溝以外の領域の前記銅、前記第１の高融点金属膜，前記高融点金属膜の窒化膜，前記第２の高融点金属膜を除去し、前記銅からなる上部ゲート電極と前記第１の高融点金属膜，前記高融点金属の窒化膜，前記第２の高融点金属膜からなる第１および第２のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項２６】　請求項２２または２３に記載の電界効果トランジスタの製造方法において、
前記下部ゲート電極に接して高融点金属の膜を成膜する工程と、
熱処理して前記下部ゲート電極に接する高融点金属の膜をシリサイド化して前記下部ゲート電極に接して高融点金属のシリサイド膜を形成し、前記第１のバリア膜の一部とする工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項２７】　シリコン基板上にゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、
前記下部ゲート電極上に犠牲パターンを形成する工程と、
前記下部ゲート電極および前記犠牲パターンをマスクとして前記シリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、
前記下部ゲート電極および前記犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、
前記下部ゲート電極および前記犠牲パターンを覆うように前記シリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、
前記第１の層間絶縁膜を除去して前記犠牲パターンの上面を露出させる工程と、
前記犠牲パターンを選択的に除去して前記下部ゲート電極上部に溝を形成する工程と、
前記下部ゲート電極上面を覆い両端が前記側壁に接触するように銅の拡散を阻止する導電性を有する第１のバリア膜を形成する工程と、
前記溝内に前記第１のバリア膜を介して銅からなる上部ゲート電極を形成して前記上部ゲート電極の底面が前記

第１のバリア膜に覆われて両側面が前記側壁からなる第２のバリア膜に覆われた状態とする工程と、
前記上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項２８】　シリコン基板上にゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、
前記下部ゲート電極上にエッチングストッパー層を形成する工程と、
前記エッチングストッパー層上に犠牲パターンを形成する工程と、
前記下部ゲート電極および前記犠牲パターンをマスクとして前記シリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、
前記下部ゲート電極，前記エッチングストッパー層，および，前記犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、
前記下部ゲート電極，前記エッチングストッパー層，および，前記犠牲パターンを覆うように前記シリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、
前記第１の層間絶縁膜を除去して前記犠牲パターンの上面を露出させる工程と、
前記犠牲パターンを選択的に除去して前記エッチングストッパー層上面を露出させる工程と、
前記エッチングストッパー層を除去して前記下部ゲート電極上部に溝を形成する工程と、
前記下部ゲート電極に密着して上面を覆い両端が前記側壁に接触するように銅の拡散を阻止する導電性を有する第１のバリア膜を形成する工程と、
前記溝内に前記第１のバリア膜を介して銅からなる上部ゲート電極を形成して前記上部ゲート電極の底面が前記第１のバリア膜に覆われて両側面が前記側壁からなる第２のバリア膜に覆われた状態とする工程と、
前記上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項２９】　シリコン基板上にゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、
前記下部ゲート電極上にエッチングストッパー層を形成する工程と、
前記エッチングストッパー層上に犠牲パターンを形成する工程と、
前記下部ゲート電極および前記犠牲パターンをマスクとして前記シリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、
前記下部ゲート電極，前記エッチングストッパー層，および，前記犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、
前記下部ゲート電極，前記エッチングストッパー層，および，前記犠牲パターンを覆うように前記シリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、
前記第１の層間絶縁膜を選択的に除去して前記犠牲パターンの上面を露出させて前記下部ゲート電極上部に溝を形成する工程と、
前記犠牲パターンを選択的に除去して前記エッチングストッパー層上面を露出させる工程と、
前記エッチングストッパー層を除去する工程と、
前記下部ゲート電極に密着して上面を覆い両端が前記側壁に接触するように銅の拡散を阻止する導電性を有する第１のバリア膜を形成する工程と、
前記溝内に前記第１のバリア膜を介して銅からなる上部ゲート電極を形成して前記上部ゲート電極の底面が前記第１のバリア膜に覆われて両側面が前記側壁からなる第２のバリア膜に覆われた状態とする工程と、
前記上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項３０】　請求項２８または２９に記載の電界効果トランジスタの製造方法において、
前記犠牲層，エッチングストッパー層，下部ゲート電極をハードマスクにより加工することを特徴とする電界効果トランジスタの製造方法。
【請求項３１】　請求項２８または２９に記載の電界効果トランジスタの製造方法において、
前記犠牲層，エッチングストッパー層，下部ゲート電極を酸化シリコンまたは窒化シリコンからなるハードマスクにより加工することを特徴とする電界効果トランジスタの製造方法。
【請求項３２】　請求項２７～３１いずれか１項に記載の電界効果トランジスタの製造方法において、
前記下部ゲート電極に接して高融点金属の膜を成膜する工程と、
熱処理して前記下部ゲート電極に接する高融点金属の膜をシリサイド化して前記下部ゲート電極に接して高融点金属のシリサイド膜を形成し、前記第１のバリア膜の一部とする工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。
【請求項３３】　請求項２７～３１のいずれか１項に記載の電界効果トランジスタの製造方法において、
前記下部ゲート電極に接して高融点金属膜を成膜する工程と、

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熱処理して前記下部ゲート電極に接する高融点金属窒化膜をシリコンに反応させて前記下部ゲート電極に接して高融点金属とシリコンと窒素との化合物膜を形成し、前記第１のバリア膜の一部とする工程とを少なくとも備えたことを特徴とする電界効果トランジスタの製造方法。

【請求項３４】　請求項１７～１９いずれか１項記載の電界効果トランジスタの製造方法において、
前記側壁がシリコン窒化物から構成されたことを特徴とする電界効果トランジスタの製造方法。

【請求項３５】　請求項１５～２１いずれか１項記載の電界効果トランジスタの製造方法において、
前記第１のバリア膜は前記下部ゲート電極上面をトンネル電流が流れる厚さまで窒化することで形成することを特徴とする電界効果トランジスタの製造方法。

【請求項３６】　請求項１５～３５いずれか１項に記載の電界効果トランジスタの製造方法において、
第１または第２のバリア膜は、前記溝底面に対して垂直の角度または垂直に近い角度で入射する粒子を多くした方法で成膜することを特徴とする電界効果トランジスタの製造方法。

【請求項３７】　請求項１５～３６いずれか１項に記載の電界効果トランジスタの製造方法において、
前記上部ゲート電極を形成する前に、前記ソース・ドレインの所定領域に高融点金属シリサイドが形成されることを特徴とする電界効果トランジスタの製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、シリコンと銅とを積層した構造のゲート電極を備えた電界効果トランジスタおよびその製造方法に関する。

【０００２】

【従来の技術】近年、ＬＳＩは高性能化，高集積化に向けてさらに微細化の研究が進められている。このような中で、微細化に伴い、電界効果トランジスタのゲート電極の低抵抗化が高性能化のために必要不可欠となっている。このため、ゲート電極材料に金属とポリシリコンとの２層構造を用いることが検討されている。そこで、電気抵抗が低いことや、加工性や化学的安定性が金・銀より優れていることなどにより、ポリシリコンと銅との２層構造によりゲート電極を構成することが提案されている。

【０００３】上記の従来の電界効果トランジスタについて説明すると、図１４に示すように、まず、シリコン基板１４０１上にゲート絶縁膜１４０２を介し、まず、ポリシリコンからなる下部ゲート電極１４０３を備えている。また、この下部ゲート電極１４０３上には、窒化チタンなどからなるバリア膜１４０４を介し、銅からなる上部ゲート電極１４０５を備えている。また、上部ゲート電極１４０５上には、窒化チタンなどからなるバリア膜１４０６を備えている。そして、下部ゲート電極１４０３と上部ゲート電極１４０５とで、トランジスタのゲート電極が構成されている。

【０００４】また、ゲート電極側面を覆うように、シリコン酸化物からなるサイドウォール１４０７が形成されている。また、サイドウォール１４０７下のシリコン基板１４０１には、低濃度不純物領域１４０８が形成されている。また、シリコン基板１４０１には、低濃度不純物領域１４０８を挟むように、ソース１４０９およびドレイン１４１０が形成されている。そして、上記の低濃度不純物領域１４０８，ソース１４０９およびドレイン１４１０，ゲート絶縁膜１４０２，および、下部ゲート電極１４０３および上部ゲート電極１４０５からなるゲート電極で、ＬＤＤ構造の電界効果トランジスタが構成されている。このＬＤＤ構造とすることで、単チャネル効果が抑制できるようになる。

【０００５】また、上記のトランジスタは、シリコン酸化物からなる層間絶縁膜１４１１で覆われ、層間絶縁膜１４１１上には、アルミニウムなどからなるゲート電極配線１４１２やソース電極配線１４１３が形成されている。ゲート電極配線１４１２は、層間絶縁膜１４１１に形成されたスルーホール内のプラグ１４１４により、上部ゲート電極１４０５にバリア膜１４０６を介して接続されている。なお、プラグ１４１４は、タングステンから構成され、プラグ１４１４の側面および底面には、窒化チタンなどからなるバリア膜１４１４ａが形成されている。

【０００６】また、ソース電極配線１４１３は、層間絶縁膜１４１１に形成されたコンタクトホール内のプラグ１４１５により、ソース１４０９に接続している。なお、このプラグ１４１５も、タングステンから構成され、側面および底面には窒化チタンなどからなるバリア膜１４１５ａが形成されている。また、ゲート電極配線１４１２およびソース電極配線１４１３上部にも、窒化チタンなどからなるバリア膜１４１２ａ，１４１３ａが形成されている。また、上記のゲート電極配線１４１２およびソース電極配線１４１３などの配線を覆うように、層間絶縁膜１４１１上には、保護絶縁膜１４１６が形成されている。

【０００７】

【発明が解決しようとする課題】以上示したように、さらなる低抵抗化のため、ポリシリコンと銅の２層構造によりゲート電極を構成する場合、銅からなる上部ゲート電極１４０５は、下面と上面とにバリア膜１４０４，１４０６を備え、下層のポリシリコンや上層の配線金属への銅の拡散を抑制するようにしている。しかしながら、銅は、シリコン酸化膜中も拡散するので、図１４の矢印の線で示すように、シリコン酸化物であるサイドウォール１４０７，層間絶縁膜１４１１中を拡散してしまう。そして、銅がシリコン基板１４０１方向に拡散すると、接合リーク電流の発生や、トランジスタのオン電流の低

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下、そして、しきい値の変動といった問題を起こしてしまう。また、銅が、上部の配線層方向に拡散すると、配線間リーク電流の発生という問題を起こしてしまう。

【０００８】本発明は、以上のような問題点を解消するためになされたものであり、電界効果トランジスタのゲート電極の材料に、トランジスタの特性を劣化させることなく銅を用いることができるようにすることを目的とする。

【０００９】

【課題を解決するための手段】本発明の電界効果トランジスタは、シリコン基板上にゲート絶縁膜を介して形成されたシリコンからなる下部ゲート電極と、この下部ゲート電極上に形成された銅からなる上部ゲート電極と、下部ゲート電極にチャネル部を駆動するに足りる電流が注入できる導電性を有して上部ゲート電極下面を覆うように形成された銅の拡散を阻止する第１のバリア膜と、この第１のバリア膜に下端が接触して上部ゲート電極の両側面を覆うように形成された銅の拡散を阻止する第２のバリア膜と、この第２のバリア膜に端部が接触して上部ゲート電極上面を覆うように形成された銅の拡散を阻止する第３のバリア膜と、下部ゲート電極下の領域を挟むようにシリコン基板に形成されたソース・ドレインとを備えたものである。この発明によれば、銅からなる上部ゲート電極は、電界効果トランジスタを構成する他の部分と第１，第２，および，第１のバリア膜を介して接触した状態に構成されている。

【００１０】上記の発明において、下部ゲート電極および上部ゲート電極側面に形成された側壁を備え、この側壁の一部で第２のバリア膜が構成される。上記の発明において、第３のバリア膜は絶縁材料から構成される。上記の発明において、上部ゲート電極上面上を開放してシリコン基板上に形成された絶縁層を備え、第３のバリア膜は絶縁層上に延在して形成される。上記の発明において、第１，第２バリア膜は高融点金属もしくは高融点金属の窒化物から構成される。上記の発明において、第１のバリア膜はトンネル電流が流れる厚さに形成された絶縁材料から構成される。前記の発明において、第１，第２，および，第３のバリア膜は高融点金属もしくは高融点金属の窒化物から構成される。上記の発明において、バリア膜は酸素を構成要素としない材料から構成される。上記の発明において、絶縁材料は、窒化シリコンもしくは窒化ボロンのいずれか１つから構成される。

【００１１】上記の発明において、第１のバリア膜は２層以上の複数層からなる多層膜である。上記の発明において、第１のバリア膜は、高融点金属からなる層または高融点金属シリサイドからなる層または高融点金属金属とシリコンと窒素との化合物からなる層もしくは高融点金属の窒化物からなる層のいずれかが組み合わされて複数層積層された多層膜である。上記の発明において、第１のバリア膜は、最下層が金属シリサイド層または高融点金属金属とシリコンと窒素との化合物からなる層から構成された多層膜である。上記の発明において、第１のバリア膜は、最下層が金属シリサイド層または高融点金属金属とシリコンと窒素との化合物からなる層から構成され、この金属シリサイドの層または高融点金属金属とシリコンと窒素との化合物からなる層の上に高融点金属の窒化物の層が配置された多層膜である。上記の発明において、第１のバリア膜は、最下層が金属シリサイド層または高融点金属金属とシリコンと窒素との化合物からなる層から構成され、この金属シリサイドの層または高融点金属金属とシリコンと窒素との化合物からなる層上に高融点金属の窒化物の層が配置され、最上層が高融点金属から構成された多層膜である。上記の発明において、ソース・ドレイン表面の所定領域に高融点金属シリサイド膜が形成される。

【００１２】また、本発明の電界効果トランジスタの製造方法は、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極および犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を除去して犠牲パターンの上面を露出させる工程と、犠牲パターンを選択的に除去して下部ゲート電極上面を露出させて第１の層間絶縁膜の下部ゲート電極上部に溝を形成する工程と、下部ゲート電極上面および溝側面を覆うように銅の拡散を阻止する導電性を有する第１，第２のバリア膜を形成する工程と、溝内に第１，第２のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面および両側面が第１および第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えるものである。この発明によれば、上部ゲート電極は、電界効果トランジスタを構成する他の部分と、第１～第３のバリア膜を介して接触した状態に作製される。上記の発明において、犠牲パターンは、所定のエッチング処理条件において、シリコンおよび酸化シリコンより速くエッチングされる材料から構成する。

【００１３】また、本発明の電界効果トランジスタの製造方法は、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上にエッチングストッパー層を形成する工程と、エッチングストッパー層上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極および犠牲パターンを覆うよ

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うにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を除去して犠牲パターンの上面を露出させる工程と、犠牲パターンを選択的に除去してエッチングストッパー層上面を露出させる工程と、エッチングストッパー層を除去して下部ゲート電極上面を露出させ下部ゲート電極上部に溝を形成する工程と、下部ゲート電極上面および溝側面を覆うように銅の拡散を阻止する導電性を有する第１および第２のバリア膜を形成する工程と、溝内に第１，第２のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面および両側面が第１および第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えたものである。この発明によれば、上部ゲート電極は、電界効果トランジスタを構成する多の部分と第１～第３のバリア膜を介して接触した状態に作製される。

【００１４】また、本発明の電界効果トランジスタの製造方法は、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上にエッチングストッパー層を形成する工程と、エッチングストッパー層上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極および犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を選択的に除去して犠牲パターンの上面を露出させて下部ゲート電極上部に溝を形成する工程と、犠牲パターンを選択的に除去してエッチングストッパー層上面を露出させる工程と、エッチングストッパー層を除去して下部ゲート電極上面を露出させる工程と、下部ゲート電極上面および溝側面を覆うように銅の拡散を阻止する導電性を有する第１および第２のバリア膜を形成する工程と、溝内に第１，第２のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面および両側面が第１および第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えるものである。この発明によれば、上部ゲート電極は、電界効果トランジスタを構成する多の部分と第１～第３のバリア膜を介して接触した状態に作製される。上記の発明において、犠牲パターンは、所定のエッチング処理条件において、酸化シリコンより速くエッチングされる材料から構成する。

【００１５】また、本発明の電界効果トランジスタの製造方法は、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極および犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、下部ゲート電極および犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を除去して犠牲パターンの上面を露出させる工程と、犠牲パターンを選択的に除去して下部ゲート電極上部に溝を形成する工程と、下部ゲート電極上面を覆い両端が側壁に接触するように銅の拡散を阻止する導電性を有する第１のバリア膜を形成する工程と、溝内に第１のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面が第１のバリア膜に覆われて両側面が側壁からなる第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えるものである。この発明によれば、上部ゲート電極は、電界効果トランジスタを構成する多の部分と第１～第３のバリア膜を介して接触した状態に作製される。また、第２のバリア膜は側壁で兼用される。

【００１６】また、本発明の電界効果トランジスタの製造方法は、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上にエッチングストッパー層を形成する工程と、エッチングストッパー層上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極，エッチングストッパー層，および，犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、下部ゲート電極，エッチングストッパー層，および，犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を除去して犠牲パターンの上面を露出させる工程と、犠牲パターンを選択的に除去してエッチングストッパー層上面を露出させる工程と、エッチングストッパー層を除去して下部ゲート電極上部に溝を形成する工程と、下部ゲート電極に密着して上面を覆い両端が側壁に接触するように銅の拡散を阻止する導電性を有する第１のバリア膜を形成する工程と、溝内に第１のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面が第１のバリア膜に覆われて両側面が側壁からなる第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えるものである。この発明によれば、上部ゲート電極は、電界効果トランジスタを構成する多の部分と第１～第３のバ

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リア膜を介して接触した状態に作製される。また、第2のバリア膜は側壁で兼用される。

【0017】また、本発明の電界効果トランジスタの製造方法は、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上にエッチングストッパー層を形成する工程と、エッチングストッパー層上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極，エッチングストッパー層，および，犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、下部ゲート電極，エッチングストッパー層，および，犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第1の層間絶縁膜を形成する工程と、第1の層間絶縁膜を選択的に除去して犠牲パターンの上面を露出させて下部ゲート電極上部に溝を形成する工程と、犠牲パターンを選択的に除去してエッチングストッパー層上面を露出させる工程と、エッチングストッパー層を除去する工程と、下部ゲート電極に密着して上面を覆い両端が側壁に接触するように銅の拡散を阻止する導電性を有する第1のバリア膜を形成する工程と、溝内に第1のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面が第1のバリア膜に覆われて両側面が側壁からなる第2のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第3のバリア膜を形成する工程とを少なくとも備えるものである。この発明によれば、上部ゲート電極は、電界効果トランジスタを構成する多の部分と第1～第3のバリア膜を介して接触した状態に作製される。また、第2のバリア膜は側壁で兼用される。

【0018】上記の発明において、側壁がシリコン窒化物から構成される。上記の発明において、第1のバリア膜は下部ゲート電極上面をトンネル電流が流れる厚さまで窒化する。上記の発明において、第1または第2のバリア膜は、溝底面に対して垂直の角度または垂直に近い角度で入射する粒子を多くした方法で成膜する。前記の発明において、下部ゲート電極上面が露出し、溝が形成された後、高融点金属膜を成膜する工程と、この高融点金属膜上に高融点金属の窒化膜を成膜する工程と、銅を成膜する工程と、溝以外の領域の銅、高融点金属膜、高融点金属の窒化膜を除去し、銅からなる上部ゲート電極と高融点金属膜と高融点金属の窒化膜からなる第1および第2のバリア膜を形成する工程とを少なくとも備える。前記の発明において、下部ゲート電極上面が露出し、溝が形成された後、第1の高融点金属膜を成膜する工程と、この第1の高融点金属膜上に高融点金属の窒化膜を成膜する工程と、この高融点金属の窒化膜上に第2の高融点金属膜を成膜する工程と、銅を成膜する工程と、溝以外の領域の銅、第1の高融点金属膜、高融点金属の窒化膜，第2の高融点金属膜を除去し、銅からなる上部ゲート電極と第1の高融点金属膜，高融点金属の窒化膜，第2の高融点金属膜からなる第1および第2のバリア膜を形成する工程とを少なくとも備える。

【0019】前記の発明において、下部ゲート電極に接して高融点金属の膜を成膜する工程と、熱処理して下部ゲート電極に接する高融点金属の膜をシリサイド化して下部ゲート電極に接して高融点金属のシリサイド膜を形成し、第1のバリア膜の一部とする工程とを少なくとも備える。前記の発明において、犠牲層，エッチングストッパー膜，下部ゲート電極をハードマスクにより加工する。前記の発明において、犠牲層，エッチングストッパー膜，下部ゲート電極を酸化シリコンまたは窒化シリコンからなるハードマスクにより加工する。前記の発明において、上部ゲート電極を形成する前にソース・ドレインの所定領域に高融点金属シリサイドを形成する。

【0020】上記の発明において、下部ゲート電極上面が露出し、溝が形成された後、高融点金属とシリコンと窒素との化合物を成膜する工程と、この高融点金属とシリコンと窒素との化合物の膜上に高融点金属の窒化膜を成膜する工程と、上部ゲート電極となる銅を成膜する工程と、溝以外の領域の銅、高融点金属膜、高融点金属膜の窒化膜を除去し、銅からなる上部ゲート電極と高融点金属膜と高融点金属の窒化膜からなる第1および第2のバリア膜を形成する工程とを少なくとも備える。上記の発明において、下部ゲート電極上面が露出し、溝が形成された後、高融点金属とシリコンと窒素との化合物を成膜する工程と、この高融点金属とシリコンと窒素との化合物の膜上に高融点金属の窒化膜を成膜する工程と、この高融点金属の窒化膜上に高融点金属膜を成膜する工程と、上部ゲート電極となる銅を成膜する工程と、溝以外の領域の銅、第1の高融点金属膜，高融点金属膜の窒化膜，第2の高融点金属膜を除去し、銅からなる上部ゲート電極と第1の高融点金属膜，高融点金属の窒化膜，第2の高融点金属膜からなる第1および第2のバリア膜を形成する工程とを少なくとも備える。上記の発明において、下部ゲート電極に接して高融点金属膜を成膜する工程と、熱処理して下部ゲート電極に接する高融点金属窒化膜をシリコンに反応させて下部ゲート電極に接して高融点金属とシリコンと窒素との化合物膜を形成し、第1のバリア膜の一部とする工程とを少なくとも備える。

【0021】

【発明の実施の形態】以下、本発明の実施の形態を図を参照して説明する。

実施の形態1

始めに、本発明の第1の実施の形態について説明する。図1は、実施の形態1における電界効果トランジスタの構成を示す断面図である。実施の形態1の電界効果トランジスタは、まず、シリコン基板101上に、ゲート絶

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縁膜１０２を介し、まず、ポリシリコンからなる下部ゲート電極１０３を備えている。また、下部ゲート電極１０３上には、銅からなる上部ゲート電極１０４を備えている。そして、上部ゲート電極１０４は、下面と側面を覆うように窒化タンタルからなるバリア膜（第１，第２のバリア膜）１０５が形成され、上面を覆うように窒化シリコンからなるバリア膜（第３のバリア膜）１０６が形成されているようにした。したがって、上部ゲート電極１０４は、バリア膜１０５，１０６により、筒状に覆われた状態となっている。そして、下部ゲート電極１０３と上部ゲート電極１０４とで、トランジスタのゲート電極が構成されている。

【００２２】また、ゲート電極側面を覆うように、シリコン酸化物からなるサイドウォール（側壁）１０７が形成されている。また、サイドウォール１０７下のシリコン基板１０１には、低濃度不純物領域１０８が形成されている。また、シリコン基板１０１には、低濃度不純物領域１０８を挟むように、ソース１０９およびドレイン１１０が形成されている。そして、上記の低濃度不純物領域１０８，ソース１０９およびドレイン１１０，ゲート絶縁膜１０２，および、下部ゲート電極１０３および上部ゲート電極１０４からなるゲート電極で、ＬＤＤ構造の電界効果トランジスタが構成されている。ＬＤＤ構造とすることで、単チャネル効果が抑制できるようになる。

【００２３】以上示したように、実施の形態１における電界効果トランジスタでは、ゲート電極をポリシリコンと銅とからなる積層構造となっているので、ゲート電極の低抵抗化がはかれている。そして、実施の形態１では、ゲート電極を構成する銅の部分を、上面と下面だけでなく、側面までバリア膜で覆うようにしたので、シリコン酸化膜を介した銅の拡散も抑制できるようになる。この結果、接合リーク電流の発生やトランジスタのオン電流の低下など、銅が拡散することによる問題が解消されることになる。

【００２４】次に、上述した実施の形態１の電界効果トランジスタの製造方法について説明する。まず、図２（ａ）に示すように、シリコン基板１０１上にドライ酸化により膜厚６ｎｍ程度に絶縁膜２０２を形成する。絶縁膜２０２はゲート絶縁膜となる。引き続いて、絶縁膜２０２上に低圧ＣＶＤ法により膜厚７０ｎｍ程度にポリシリコン膜２０３を形成し、この上に、やはり低圧ＣＶＤ法により膜厚１００ｎｍ程度に窒化シリコン膜２０４を形成する。

【００２５】次に、図２（ｂ）に示すように、レジストパターン２０５をマスクとしたドライエッチングにより、窒化シリコン膜２０４およびポリシリコン膜２０３を選択的に除去し、下部ゲート電極１０３および犠牲パターン２０４ａを形成する。次いで、レジストパターン２０５を除去した後、図２（ｃ）に示すように、犠牲パターン２０４ａおよび下部ゲート電極１０３をマスクとして選択的にイオン注入することで、低濃度不純物領域（ＬＤＤ）１０８を形成する。ここでは、Ａｓを注入エネルギー２０ｅＶでイオン注入し、注入量は3×10^{13}ｃｍ$^{-2}$程度とすればよい。

【００２６】次に、図２（ｄ）に示すように、全面にシリコン酸化膜２０６を形成する。これは、ＴＥＯＳを原料とした低圧ＣＶＤ法によりシリコン酸化物を堆積することで行えばよい。そして、垂直異方性を有している反応性イオンエッチング（ＲＩＥ）により、シリコン酸化膜２０６をエッチバックすることで、図３（ｅ）に示すように、下部ゲート電極１０３および犠牲パターン２０４ａの側面に、サイドウォール１０７を形成する。

【００２７】次に、図３（ｆ）に示すように、犠牲パターン２０４ａ，下部ゲート電極１０３，および，サイドウォール１０７をマスクとして選択的にイオン注入することで、ソース１０９およびドレイン１１０を形成する。ここでは、Ａｓを注入エネルギー３０ｅＶでイオン注入し、注入量は3×10^{15}ｃｍ$^{-2}$程度とすればよい。次に、オゾンとＴＥＯＳを原料としたＣＶＤにより、ボロンリンシリケートガラスを堆積し、図３（ｇ）に示すように、膜厚５００ｎｍ程度に下部層間絶縁膜２０９を形成する。

【００２８】次に、酸化膜の化学的機械的研磨（ＣＭＰ）により、下部層間絶縁膜２０９を平坦化研磨することで、図３（ｈ）に示すように、犠牲パターン２０４ａ上部を露出させる。次に、加熱したリン酸水溶液を用いたウエットエッチングにより、犠牲パターン２０４ａを選択的に除去し、図３（ｉ）に示すように、下部ゲート電極１０３上部にサイドウォール１０７および下部層間絶縁膜２０９に囲われた溝２１０を形成する。この熱リン酸によるウエットエッチングでは、シリコンや酸化シリコンはあまりエッチングされないので、窒化シリコンからなる犠牲パターン２０４ａを選択的に除去できる。

【００２９】ところで、上述した実施の形態１では、ＣＭＰにより下部層間絶縁膜２０９を除去することで、犠牲パターン２０４ａ上部を露出させるようにしたが、次に示す手法により犠牲パターン２０４ａ上部を露出させるようにしてもよい。例えば、ボロンシリケートガラスのようにリフローにより平坦化が可能な場合は、下部層間絶縁膜リフローして平坦化した後で、ドライエッチングなどにより除去することで犠牲パターン２０４ａ上部を露出させるようにしてもよい。この際に、ボロンシリケートガラス以外にも、ボロンとリンとを含有したシリケートガラス（ＢＰＳＧ）を、下部層間絶縁膜として使用することもできる。

【００３０】さらに、下部層間絶縁膜としてＳＯＧ（スピンオングラス）材料を用い、これを塗布することで平坦化した後、平坦化した塗布膜をドライエッチングなどによりエッチバックすることで犠牲パターン２０４ａ上

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部を露出させるようにしてもよい。ここで、CMP法やSOG材料を用いて平坦化した後エッチバックする手法を用いる場合は、特にシリケートガラスを用いずに、下部層間絶縁膜をCVD法などで成膜される通常のシリコン酸化膜や窒化シリコン膜とすることができる。

【0031】次に、図4（j）に示すように、上記の溝210の底部，側面を含む下部層間絶縁膜209上に窒化タンタル膜をスパッタ法により堆積し、膜厚10nm程度にTaN膜211を形成し、続いて、TaN膜211上に銅をスパッタにより堆積し、200nm程度のCu層212を形成する。次に、例えば、金属膜のCMPにより、Cu層212およびTaN膜211を研磨により除去することで、図4（k）に示すように、溝210内に窒化タンタルかなるバリア膜105に下面および側面を覆われた銅からなる上部ゲート電極104が形成された状態とし、加えて、上部ゲート電極104上部以外の下部層間絶縁膜209表面を露出させる。

【0032】次に、図4（l）に示すように、全面に窒化シリコンからなる膜厚10nm程度のバリア膜106を形成する。これは、プラズマCVD法により窒化シリコンを堆積することにより行えばよい。以上のことにより、ポリシリコンからなる下部ゲート電極103と、周囲をバリア膜105およびバリア膜106で覆われた銅からなる上部ゲート電極104とからなるゲート電極を備えた電界効果トランジスタが形成されたことになる。

【0033】なお、バリア膜106は、下部層間絶縁膜209上にまで延在して形成する必要はない。図1に示したように、バリア膜106により上部ゲート電極104の上面が覆われるだけの領域に、バリア膜106が形成されていても良い。この場合は、バリア膜106が下部層間絶縁膜209上に延在していないので、バリア膜106を例えば、バリア膜105と同一の導電性を有する窒化タンタルから構成するようにしても良い。

【0034】この後、図4（m）に示すように、バリア膜106上にボロンとリンが添加されたシリコン酸化物（BPSG）からなる層間絶縁膜111を、膜厚500nm程度に形成する。これは、例えば、酸素ガスとTEOSとを原料としたCVD法により形成すればよい。次に、図4（n）に示すように、コンタクトホール112およびスルーホール113を形成する。これは、公知のフォトリソグラフィグラフにより形成したレジストパターンをマスクとした、異方性ドライエッチングにより形成すればよい。なお、コンタクトホール112は、底面にシリコン基板101のソース109面が露出し、スルーホール113底面には、上部ゲート電極104の上面が露出している。

【0035】次に、図5（o）に示すように、コンタクトホール112，スルーホール113の側面および底面を含め、層間絶縁膜111上に窒化チタンとチタンとの2層構造のバリア膜114を形成する。これは、CVD法により形成し、膜厚は各々50nmおよび10nm程度とすればよい。引き続いて、図5（p）に示すように、バリア膜114上にタングステンからなるW膜115を、例えば、低圧CVD法により膜厚400nm程度に形成する。

【0036】次に、コンタクトホール112，スルーホール113が埋まった状態となる程度に、上記のW膜115をドライエッチングなどにより除去する。このことにより、プラグ112a，113aを形成した後（図5（q））、銅が1%程度のアルミニウム銅合金からなる合金膜115aを、スパッタ法により膜厚500nm程度に形成する。加えて、スパッタ法により、窒化チタンからなるバリア膜116を、膜厚30nm程度に形成する。そして、合金膜115aおよびバリア膜114，116をパターニングすれば、図5（r）に示すように、ソース電極配線117およびゲート電極配線118が形成できる。

【0037】以上示したように製造すれば、ソース・ドレインを形成した後で、銅からなる上部ゲート電極が形成される。すなわち、ソース・ドレイン形成のための高温の活性化熱処理の後で、上部ゲート電極が形成されることになるので、融点があまり高くない銅を用いて上部ゲート電極を構成することができる。なお、上記実施の形態1では、バリア膜（第1，第2のバリア膜）105として窒化タンタルを用いるようにしたが、これに限るものではなく、窒化チタン，窒化タングステン，窒化タンタル，窒化モリブデン，窒化チタンシリサイド，窒化タングステンシリサイドなどの窒化物（高融点金属とシリコンと窒素の化合物）や、タンタルやチタンタングステンなどの金属材料を用いるようにしてもよい。

【0038】ところで、上述したバリア膜（第1～第3のバリア膜）に、酸素を構成要素としない銅の拡散を阻止する機能を有する材料を用いるようにしてもよい。上部ゲート電極は銅から構成するので、このように酸素がなければ、銅の酸化を抑制することが可能となる。また、上部ゲート電極の下面に配置するバリア膜（第1のバリア膜）に、例えば、窒化シリコンなどを用いるようにしてもよい。すなわち、このバリア膜には、下部ゲート電極にチャネル部を駆動するに足りる電流が注入できる導電性があればよいので、窒化シリコンを用いても膜厚をトンネル電流が流れる程度としておけばよい。この場合、下部ゲート電極表面を例えば2nm程度窒化すれば、この窒化した部分でバリア膜を形成することができる。

【0039】また、上述した銅の上部ゲート電極の側面に配置されるバリア膜（第2のバリア膜）と下部ゲート電極との間に配置されるバリア膜（第1のバリア膜）は、2層以上の膜で構成された多層膜であってもよい。固体中の拡散においては、固体材料の界面または粒界（膜が多結晶の場合）に拡散種が析出する可能性が高

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い。このため、バリア膜を積層した多層膜することで、膜間の界面に微量に拡散する銅を捕獲し、拡散種の拡散をよりいっそう防止することが可能となる。この多層膜は、高融点金属，または高融点金属の複合膜とすると良い。例えば、Ｔａと窒化Ｔａとの複合膜とするとよい。熱的に安定な金属窒化物に銅などの金属は拡散しずらいため、バリア膜として高融点金属の窒化膜を用いることで点欠陥量も少なくなり、点欠陥を介した銅の拡散は抑制される。

【００４０】高融点金属シリサイドが、多層膜構造を有した第１のバリア膜の一部としてシリコンの下部ゲート電極に接して配置されることも、電界効果トランジスタの動作性能の向上に効果的である。シリサイドとシリコンとの界面では、ショットキーバリア形成が抑制されかつ接触抵抗が低減されるからである。多層膜の第１のバリア膜において、銅と接する膜を高融点金属とすることも、銅と第１のバリア膜との密着性向上には効果的である。高融点金属とシリコンと窒素の化合物が、多層膜構造を有した第１のバリア膜の一部としてシリコンの下部電極に接して配置されることも、デバイス製造歩留り向上に有効である。上記の化合物は、シリコンと密着性がよいからである。例えば、タングステンの窒化物をＣＶＤ法や反応性コリメートスパッタ法などで溝内に成膜し、５００℃程度の温度で熱処理することで、上記の化合物は形成できる。このとき、シリコンと高融点金属窒化物との反応で、上記の化合物は形成されるため、シリコンとの密着性は向上する。

【００４１】実施の形態２

次に、本発明の第２の実施の形態について説明する。まず、この実施の形態２の電界効果トランジスタの製造方法について説明する。はじめに、図６（ａ）に示すように、シリコン基板６０１上にドライ酸化により膜厚６ｎｍ程度にゲート絶縁膜６０２を形成する。引き続いて、ゲート絶縁膜６０２上に低圧ＣＶＤ法により膜厚５０ｎｍ程度にｎ形の不純物が導入されたポリシリコン膜７０３を形成し、この上に、ＣＶＤ法により膜厚１０ｎｍ程度に酸化シリコン膜７０４を形成する。加えて、この酸化シリコン膜７０４上に、ＣＶＤ法により膜厚１００～３００ｎｍ程度にポリシリコン膜７０５を形成する

【００４２】次に、図６（ｂ）に示すように、レジストパターン７０６をマスクとしたドライエッチングにより、ポリシリコン膜７０５，酸化シリコン膜７０４，および，ポリシリコン膜７０３を選択的に除去し、下部ゲート電極６０３，エッチングストッパー層７０４ａ，および，犠牲パターン７０５ａを形成する。次いで、レジストパターン７０６を除去した後、図６（ｃ）に示すように、犠牲パターン７０５ａおよび下部ゲート電極６０３をマスクとして選択的にイオン注入することで、低濃度不純物領域（ＬＤＤ）６０８を形成する。ここでは、Ａｓを注入エネルギー２０ｅＶでイオン注入し、この注入量は$1\times10^{13}cm^{-2}$程度とすればよい。

【００４３】次に、図６（ｄ）に示すように、全面にシリコン酸化膜７０７を形成する。これは、ＴＥＯＳを原料とした低圧ＣＶＤ法によりシリコン酸化物を堆積することで行えばよい。そして、垂直異方性を有している反応性イオンエッチング（ＲＩＥ）により、シリコン酸化膜７０７をエッチバックすることで、図６（ｅ）に示すように、下部ゲート電極６０３および犠牲パターン７０５ａの側面に、サイドウォール６０７を形成する。なお、このサイドウォール６０７は、窒化シリコンから構成するようにしてもよい。この場合も、酸化シリコンから形成する場合と同様に形成できる。

【００４４】次に、犠牲パターン７０５ａ，下部ゲート電極６０３，および，サイドウォール６０７をマスクとして選択的にイオン注入することで、ソース６０９およびドレイン６１０を形成する。ここでは、Ａｓを注入エネルギー３０ｅＶでイオン注入し、この注入量は$2\times10^{15}cm^{-2}$程度とすればよい。なお、イオン注入により形成した不純物導入領域は、例えば、窒素雰囲気で８００℃・１０分および１０００℃・１０秒の加熱処理を行い、欠陥の低減と不純物の活性化を行う。

【００４５】次に、オゾンとＴＥＯＳを原料としたＣＶＤにより、ボロンリンシリケートガラスを堆積し、これらを加熱してフローさせることで、図７（ｇ）に示すように、膜厚４００～６００ｎｍ程度に下部層間絶縁膜７０９を形成する。次に、例えば、酸化膜の化学的機械的研磨（ＣＭＰ）により下部層間絶縁膜７０９を所定膜厚除去し、図７（ｈ）に示すように、犠牲パターン７０５ａ上部を露出させる。次に、酸化膜との高選択性を持たせたリアクティブイオンエッチングにより犠牲パターン７０５ａを選択的に除去し、図７（ｉ）に示すように、下部ゲート電極６０３上部にサイドウォール６０７および下部層間絶縁膜７０９に囲われた溝７１０を形成する。

【００４６】続いて、図７（ｊ）に示すように、酸化シリコンと選択比のあるエッチング方法によりエッチングストッパー層７０４ａを除去し、溝７１０底部に下部ゲート電極６０３上面を露出させる。次に、図８（ｋ）に示すように、溝７１０の底部，側面を含む下部層間絶縁膜７０９上に窒化タンタル膜をスパッタ法により堆積し、膜厚１０ｎｍ程度にＴａＮ膜７１１を形成する。続いて、図８（ｌ）に示すように、ＴａＮ膜７１１上に銅をスパッタにより堆積し、加えて堆積した銅を加熱フローすることで、表面が平坦になった膜厚１００～５００ｎｍ程度のＣｕ層７１２を形成する。

【００４７】ここで、ＴａＮ膜７１１の代わりに、窒化チタン，タンタル，窒化タングステン，チタンタングステンなどの薄膜を用いるようにしても良い。また、Ｃｕ層６１２は、例えば電界メッキ法やＣＶＤ法により形成するようにしても良い。次に、例えば、金属膜のＣＭＰ

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により、Cu層712およびTaN膜711を除去することで、図8（m）に示すように、下面および側面が窒化タンタルかなるバリア膜605に覆われた、銅からなる上部ゲート電極604が形成された状態とし、加えて、上部ゲート電極604上以外の下部層間絶縁膜709表面を露出させる。なお、TaN膜711の代わりに、TaN／Ta、Ta／TaN／Ta膜など高融点金と高融点金属の窒化物の積層膜としてよい。

【0048】また、上記の積層膜の成膜方法にコリメートスパッタ法を用いることで、ゲート電極の層抵抗の低減と溝の幅が減少した場合の層抵抗の増加が抑制される。コリメートスパッタ法によれば、原料ターゲットからプラズマによりスパッタされた粒子で成膜にきよするものは、基板への入射角度はコリーメータにより垂直に近いものとなる。このため、溝内の側壁に成膜される膜厚は、溝底部に成膜される膜厚より薄くなる。バリア膜の材料の抵抗率が銅より高い場合、側面の膜厚が厚いと、この膜厚に比例して抵抗が増加する。また、溝の幅が減少した場合、層抵抗が増大する。したがって、上記のコリメートスパッタ法により、溝内の側壁に成膜される膜厚を薄くするようにした方がよい。同様の効果が、イオン化スパッタ法と呼ばれる方法によっても得られる。イオン化スパッタ法は、基板にかけたバイアスによりイオン化された原料粒子を基板に対して垂直に近い角度で入射し，入射した粒子を堆積して成膜する方法であり、やはり溝内の側壁に成膜される膜厚を薄くできる。

【0049】次に、図8（n）に示すように、全面に酸化チタンもしくは窒化シリコンからなる膜厚10～100nm程度のバリア膜606を形成する。これは、例えば反応性スパッタ法などにより成膜すればよい。以上のことにより、ポリシリコンからなる下部ゲート電極603と、周囲をバリア膜605およびバリア膜606で覆われた銅からなる上部ゲート電極604とからなるゲート電極を備えた電界効果トランジスタが形成されたことになる。なお、バリア膜606は、下部層間絶縁膜709上にまで延在して形成する必要はない。バリア膜606により上部ゲート電極604の上面が覆われるだけの領域に、バリア膜606が形成されていても良い。この場合は、バリア膜606が下部層間絶縁膜709上に延在していないので、バリア膜606を例えば、バリア膜605と同一の窒化タンタルから構成するようにしても良い。

【0050】この後、図8（o）に示すように、バリア膜606上にボロンとリンが添加されたシリコン酸化物（BPSG）からなる層間絶縁膜713を、膜厚100～500nm程度に形成する。これは、例えば、酸素ガスとTEOSとを原料としたCVD法により形成すればよい。次に、図9（p）に示すように、コンタクトホール612，613を形成する。これは、公知のフォトリソグラフィグラフにより形成したレジストパターンをマスクとした、異方性ドライエッチングにより形成すればよい。なお、コンタクトホール612は、底面にシリコン基板601のソース609面が露出し、コンタクトホール613は、底面にシリコン基板601のドレイン610面が露出し

【0051】そして、図9（q）に示すように、コンタクトホール612，613を介し、アルミニウムなどからなるソース電極配線616およびドレイン電極配線617形成すればよい。以上のことにより、実施の形態2においても、ゲート電極がポリシリコンと銅との積層構造となっているので、ゲート電極の低抵抗化がはかれている。そして、実施の形態2においても、ゲート電極を構成する銅の部分を、胴部分の上面と下面だけでなく、側面までバリア膜で覆うようにしたので、シリコン酸化膜を介した銅の拡散も抑制できるようになる。この結果、接合リーク電流の発生やトランジスタのオン電流の低下など、銅が拡散することによる問題が解消されることになる。

【0052】また、実施の形態2においても、ソース・ドレインを形成した後で、銅からなる上部ゲート電極が形成される。すなわち、ソース・ドレイン形成のための高温の活性化熱処理の後で、上部ゲート電極が形成されることになるので、融点があまり高くない銅を用いて上部ゲート電極を構成することができる。

【0053】ところで、サイドウォール（側壁）は、窒化シリコンから構成するようにしてもよい。窒化シリコンなどの銅の拡散を阻止できる材料からサイドウォールを形成した場合、サイドウォールを前述した上部ゲート電極側面に配置するバリア膜（第2のバリア膜）として用いることができる。この場合、新たに上部ゲート電極側面に配置するバリア膜を形成しなくてもすむ。すなわち、例えば、図4（j）に示したように、溝210の底部，側面を含む下部層間絶縁膜209上に窒化タンタル膜をスパッタ法により堆積せず、例えば、下部ゲート電極103上部を2nm程度窒化して第1のバリア膜とする。前述したように、2nm程度の膜厚の窒化シリコンならトンネル電流が流れるので、上部ゲート電極との導通に問題はない。

【0054】なお、このとき、下部ゲート電極103上部を窒化するのではなく、下部ゲート電極103上部に、銅の拡散を阻止できるほかの導電性を有する材料を形成するようにしてもよいことはいうまでもない。そして、上記の第1のバリア膜上に上部ゲート電極104を形成すれば、この上部ゲート電極104は下面および両側面が銅の拡散を阻止する窒化シリコンで覆われた状態とすることができる。この後、図4（l）以降の工程と同様にすれば、本発明による電界効果トランジスタを得ることができる。

【0055】また、サイドウォールを窒化シリコンなどのシリコン酸化物より所定のエッチング条件ではエッチ

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ングされにくいものとした場合、上部ゲート電極上への配線のコンタクトが容易となる。これは次に理由による。まず、上部ゲート電極上に形成される層間絶縁膜にコンタクトホールを形成し、このコンタクトホールを介して上部ゲート電極に配線を接続する。このコンタクトホール形成の時、シリコン酸化物からなる層間絶縁膜のエッチングでは窒化シリコンがほとんどエッチングされないため、コンタクトホール形成位置が少しずれても、サイドウォールがエッチングされないからである。

【００５６】ところで、上記では、図６（ｂ）に示すように、レジストパターン７０６をマスクとして下層を加工するようにしたが、これに限るものではなく、以下に説明するように、酸化シリコンからなるハードマスクを用いて加工するようにしてもよい。加えて、ハードマスクを用いることで、ソース・ドレイン領域に選択的に高融点金属のシリサイドを形成することができる。

【００５７】まず、図１０（ａ）に示すように、シリコン基板６０１上にドライ酸化により膜厚６ｎｍ程度にゲート絶縁膜６０２を形成する。引き続いて、ゲート絶縁膜６０２上に低圧ＣＶＤ法により膜厚５０ｎｍ程度にｎ形の不純物が導入されたポリシリコン膜７０３を形成し、この上に、ＣＶＤ法により膜厚１０ｎｍ程度に酸化シリコン膜７０４を形成し、この酸化シリコン膜７０４上に、ＣＶＤ法により膜厚１００～３００ｎｍ程度にポリシリコン膜７０５を形成する。加えて、ポリシリコン膜７０５ａ上に、酸化シリコン膜１００１を形成する。なお、この酸化シリコン膜は、窒化シリコン膜としてもよい。

【００５８】次に、ポリシリコン膜７０５，酸化シリコン膜７０４，および，ポリシリコン膜７０３，および酸化シリコン膜１００１を、図１０（ｂ）に示すように、レジストパターン７０６をマスクとしたドライエッチングにより選択的に除去し、下部ゲート電極６０３，エッチングストッパー層７０４ａ，および犠牲パターン７０５ａを形成するとともに、ハードマスク１００１ａを形成する。次いで、レジストパターン７０６を除去した後、図１０（ｃ）に示すように、ハードマスク１００１ａ，犠牲パターン７０５ａおよび下部ゲート電極６０３をマスクとして選択的にイオン注入することで、低濃度不純物領域（ＬＤＤ）６０８を形成する。ＬＤＤ６０８は、Ａｓを注入エネルギー２０ｅＶでイオン注入し、この注入量は1×10^{13}ｃｍ$^{-2}$程度とすればよい。

【００５９】次に、図１０（ｄ）に示すように、ＴＥＯＳを原料とした低圧ＣＶＤ法によりシリコン酸化物を堆積することで、全面にシリコン酸化膜７０７を形成する。そして、垂直異方性を有している反応性イオンエッチング（ＲＩＥ）により、シリコン酸化膜７０７をエッチバックすることで、図１０（ｅ）に示すように、下部ゲート電極６０３および犠牲パターン７０５ａの側面に、サイドウォール６０７を形成する。同時に、ゲート絶縁膜６０２の下部ゲート電極６０３とサイドウォール６０７で覆われていない領域を除去する。なお、上記のサイドウォール６０７は、窒化シリコンから構成するようにしてもよい。この場合も、酸化シリコンから形成する場合と同様に形成できる。

【００６０】次に、犠牲パターン７０５ａ，下部ゲート電極６０３，および，サイドウォール６０７加えてハードマスク１００１ａをマスクとして選択的にイオン注入することで、ソース６０９およびドレイン６１０を形成する。ここでも、Ａｓを注入エネルギー３０ｅＶでイオン注入し、この注入量は2×10^{15}ｃｍ$^{-2}$程度とすればよい。なお、イオン注入により形成した不純物導入領域は、例えば、窒素雰囲気で８００℃・１０分および１０００℃・１０秒の加熱処理を行い、欠陥の低減と不純物の活性化を行う。

【００６１】そして、ハードマスク１００１ａを用いるようにしたので、シリコンからなる犠牲パターン７０５ａ上にはシリサイドを形成することなく、ソース・ドレイン領域表面にシリサイドを自己整合的に形成することが可能となる。図１１（ｆ）に示すように、スパッタ法などにより、全域にコバルトを膜厚１０～２０ｎｍに成膜して高融点金属膜１００２を形成し、ＲＴＡ（Rapid Thermal Anneal）法で加熱し、下地シリコン（シリコン基板６０１）と高融点金属膜１００２を反応させ、図１１（ｇ）に示すように、ソース６０９，ドレイン６１０上に選択的にシリサイド１００３を形成する。このシリサイドを形成するための加熱温度は、６５０～７５０℃程度がよい。また、加熱するときの雰囲気は、窒素またはアルゴンのような不活性雰囲気がよい。

【００６２】シリサイドを形成した後、図１１（ｈ）に示すように、塩酸：過酸化水素水：水の混合水溶液を用いたウエットエッチングにより、下地シリコンと未反応のコバルトを選択的に除去する。窒素雰囲気で加熱した場合は、窒化したコバルトが生成されるため、この窒化したコバルトも塩酸：過酸化水素水：水の混合水溶液を用いたウエットエッチングにより選択的に除去する。この後、再度、ＲＴＡ法により７５０～８５０℃程度の温度で加熱することでシリサイドの低抵抗化が図れる。なお、高融点金属としては、コバルトのほかにチタン（１０～３０ｎｍ）を用いるようにしてもよい。チタンを用いる場合、シリサイド加工直後の余剰チタンまたは窒化チタンの除去には、アンモニア：過酸化水素水：水の混合水溶液によるウエットエッチングを用いればよい。

【００６３】ソース・ドレイン領域にシリサイドを選択的に形成したら、図７（ｇ）と同様に、膜厚４００～６００ｎｍ程度に下部層間絶縁膜７０９を形成し、この後、例えば、酸化膜の化学的機械的研磨（ＣＭＰ）により下部層間絶縁膜７０９を所定膜厚除去し、同時にハードマスも除去して犠牲パターン７０５ａ上部を露出させる。この後、図７（ｈ）～図９（ｑ）に示した工程と同

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様にすることで、図１１（ｉ）に示すように、図９（ｑ）に示した構成に加えて、シリサイド１００３が形成された状態が得られる。シリサイド１００３をソース６０９，ドレイン６１０に選択的に形成するようにしたので、ソース電極配線６１６およびドレイン電極配線６１７のコンタクト抵抗を低減することができる。

【００６４】なお、シリサイドの形成は、前述の実施の形態１の電界効果トランジスタに適用してもよい。例えば、図３（ｅ）に示したサイドウォール１０７の形成時に、ゲート絶縁膜１０２のソース・ドレインとなる領域上の部分を同時に除去すれば、シリコン基板１０１のソース・ドレインとなる表面が露出する。この後、図３（ｆ）と同様に、ソース１０９，ドレイン１１０を形成し、全域にコバルトやチタンなどの高融点金属の膜を形成すれば、図１１（ｆ）～図１１（ｈ）と同様に、ソース・ドレイン上に選択的にシリサイドを形成できる。実施の形態１では、犠牲パターン２０４ａは窒化シリコンから構成され、サイドウォール１０７は酸化シリコンから構成されているので、これら表面にはシリサイドが形成されない。このように、サイドウォール表面や犠牲膜表面が、高融点金属と反応しにくいものであれば、ソース・ドレイン上に選択的にシリサイドを形成することが容易に可能となる。

【００６５】次に、前述した再度ウオールを第２のバリア膜として用いる場合の電界効果トランジスタの製造方法に関して説明する。まず、図１２（ａ）に示すように、シリコン基板１０１上にドライ酸化により膜厚６ｎｍ程度に絶縁膜２０２を形成する。絶縁膜２０２はゲート絶縁膜となる。引き続いて、絶縁膜２０２上に低圧ＣＶＤ法により膜厚７０ｎｍ程度にポリシリコン膜２０３を形成した後、この場合では、ポリシリコン膜２０３上に窒化タンタル膜をスパッタ法により堆積し、膜厚１０ｎｍ程度にＴａＮ膜１２０１を形成する。そして、ＴａＮ膜１２０１上に４００℃程度の低温のＣＶＤ法またはプラズマＣＶＤ法により膜厚１００ｎｍ程度にポリシリコン膜７０５を形成する。

【００６６】次に、図１２（ｂ）に示すように、レジストパターン２０５をマスクとしたドライエッチングにより、ポリシリコン膜７０５，ＴａＮ膜１２０１，およびポリシリコン膜２０３を選択的に除去し、下部ゲート電極１０３および犠牲パターン７０５ａを形成するとともに、これらに挟まれたバリア膜（第１のバリア膜）１２０１ａを形成する。次いで、レジストパターン２０５を除去した後、図１２（ｃ）に示すように、犠牲パターン７０５および下部ゲート電極１０３をマスクとして選択的にイオン注入することで、低濃度不純物領域（ＬＤＤ）１０８を形成する。ここでも、Ａｓを注入エネルギー２０ｅＶでイオン注入し、注入量は$3\times10^{13}cm^{-2}$程度とすればよい。

【００６７】次に、図１２（ｄ）に示すように、全面にシリコン窒化膜２０６ａを形成する。そして、垂直異方性を有している反応性イオンエッチング（ＲＩＥ）により、シリコン窒化膜２０６ａをエッチバックすることで、図１２（ｅ）に示すように、下部ゲート電極１０３，バリア膜１２０１ａ、および犠牲パターン７０５ａの側面に、サイドウォール１０７ａを形成する。サイドウォール１０７ａは、シリコン窒化物から構成されるので、銅の拡散を抑制する第２のバリア膜として用いることができる。次に、図１２（ｆ）に示すように、犠牲パターン７０５ａ，下部ゲート電極１０３，および，サイドウォール１０７ａをマスクとして選択的にイオン注入することで、ソース１０９およびドレイン１１０を形成する。ソース１０９，ドレイン１１０の形成は、Ａｓを注入エネルギー３０ｅＶでイオン注入し、注入量は$3\times10^{15}cm^{-2}$程度とすればよい。

【００６８】次に、オゾンとＴＥＯＳを原料としたＣＶＤにより、ボロンリンシリケートガラスを堆積し、図１３（ｇ）に示すように、膜厚５００ｎｍ程度に下部層間絶縁膜２０９を形成する。次に、酸化膜の化学的機械的研磨（ＣＭＰ）により、下部層間絶縁膜２０９を平坦化研磨することで、図１３（ｈ）に示すように、犠牲パターン７０５ａ上部を露出させる。次に、ポリシリコンが選択的にエッチングされる条件で犠牲パターン７０５ａを選択的に除去し、図１３（ｉ）に示すように、上面がバリア膜１２０１ａで覆われた下部ゲート電極１０３上部にサイドウォール１０７ａおよび下部層間絶縁膜２０９に囲われた溝２１０を形成する。

【００６９】次に、図１３（ｊ）に示すように、上記の溝２１０の底部，側面を含む下部層間絶縁膜２０９（バリア膜１２０１ａ）上に銅をスパッタにより堆積し、膜厚２００ｎｍ程度のＣｕ層２１２を形成する。この後、例えば、金属膜のＣＭＰにより、Ｃｕ層２１２を研磨により除去するなど、前記の図４（ｋ）～図５（ｑ）と同様の処理を施すことで、図１３（ｒ）に示すように、サイドウォール１０７ａを第２のバリア膜とした電界効果トランジスタが形成できる。

【００７０】なお、ＴａＮ膜１２０１を形成した後、ポリシリコン膜を形成する前に、薄く酸化シリコン膜を形成することで、バリア膜（第１のバリア膜）１２０１ａと犠牲パターン７０５ａの間に酸化シリコンからなるエッチングストッパー層を設けるようにしてもよい。エッチングストッパー層を設けることで、上記の犠牲パターン７０５ａの選択除去が、より容易となる。なお、このエッチングストッパー層は、例えば弗酸溶液によるウエットエッチングで、バリア膜やサイドウォールに対して選択的に除去できる。この場合、下部層間絶縁膜２０９もある程度エッチングされる。以上説明したことにより、上部ゲート電極が下部ゲート電極と同一の幅に形成できるので、上部ゲート電極の幅が実施の形態１に比較して長くなり、上部ゲート電極の抵抗が低下する。

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【００７１】
【発明の効果】以上説明したように、本発明では、シリコン基板上にゲート絶縁膜を介して形成されたシリコンからなる下部ゲート電極と、この下部ゲート電極上に形成された銅からなる上部ゲート電極と、下部ゲート電極にチャネル部を駆動するに足りる電流が注入できる導電性を有して上部ゲート電極下面を覆うように形成された銅の拡散を阻止する第１のバリア膜と、この第１のバリア膜に下端が接触して上部ゲート電極の両側面を覆うように形成された銅の拡散を阻止する第２のバリア膜と、この第２のバリア膜に端部が接触して上部ゲート電極上面を覆うように形成された銅の拡散を阻止する第３のバリア膜と、下部ゲート電極下の領域を挟むようにシリコン基板に形成されたソース・ドレインとを備えるようにした。従って、上部ゲート電極は、電界効果トランジスタを構成する多の部分と第１～第３のバリア膜を介して接触した状態に構成されている。すなわち、上部ゲート電極からの銅の拡散がすべての方向に対して阻止できるようになる。この結果、この発明は、電界効果トランジスタのゲート電極の材料に、トランジスタの特性を劣化させることなく銅を用いることができるようになるという極めて優れた効果を有している。
【００７２】また、本発明では、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極および犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を除去して犠牲パターンの上面を露出させる工程と、犠牲パターンを選択的に除去して下部ゲート電極上面を露出させて第１の層間絶縁膜の下部ゲート電極上部に溝を形成する工程と、下部ゲート電極上面および溝側面を覆うように銅の拡散を阻止する導電性を有する第１，第２のバリア膜を形成する工程と、溝内に第１，第２のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面および両側面が第１および第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えるようにした。
【００７３】また、本発明では、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上にエッチングストッパー層を形成する工程と、エッチングストッパー層上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極および犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を選択的に除去して犠牲パターンの上面を露出させて下部ゲート電極上部に溝を形成する工程と、犠牲パターンを選択的に除去してエッチングストッパー層上面を露出させる工程と、エッチングストッパー層を除去して下部ゲート電極上面を露出させる工程と、下部ゲート電極上面および溝側面を覆うように銅の拡散を阻止する導電性を有する第１および第２のバリア膜を形成する工程と、溝内に第１，第２のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面および両側面が第１および第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えるようにした。
【００７４】以上のように製造するようにしたので、上部ゲート電極は、電界効果トランジスタを構成する多の部分と第１～第３のバリア膜を介して接触した状態に作製される。すなわち、上部ゲート電極からの銅の拡散がすべての方向に対して阻止できるようになる。この結果、この発明は、電界効果トランジスタのゲート電極の材料に、トランジスタの特性を劣化させることなく銅を用いることができるようになるという極めて優れた効果を有している。また、ソース・ドレインを形成した後で、銅からなる上部ゲート電極が形成されるので、ソース・ドレイン形成のための高温の活性化熱処理の後で、上部ゲート電極が形成されることになる。この結果、融点があまり高くない銅を用いて上部ゲート電極を構成することができる。
【００７５】また、本発明では、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極および犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、下部ゲート電極および犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を除去して犠牲パターンの上面を露出させる工程と、犠牲パターンを選択的に除去して下部ゲート電極上部に溝を形成する工程と、下部ゲート電極上面を覆い両端が側壁に接触するように銅の拡散を阻止する導電性を有する第１のバリア膜を形成する工程と、溝内に第１のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面が第１のバリア膜に覆われて両側面が側壁からなる第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも

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備えるようにした。

【００７６】また、本発明では、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上にエッチングストッパー層を形成する工程と、エッチングストッパー層上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極，エッチングストッパー層，および，犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、下部ゲート電極，エッチングストッパー層，および，犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を除去して犠牲パターンの上面を露出させる工程と、犠牲パターンを選択的に除去してエッチングストッパー層上面を露出させる工程と、エッチングストッパー層を除去して下部ゲート電極上部に溝を形成する工程と、下部ゲート電極に密着して上面を覆い両端が側壁に接触するように銅の拡散を阻止する導電性を有する第１のバリア膜を形成する工程と、溝内に第１のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面が第１のバリア膜に覆われて両側面が側壁からなる第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えるようにした。

【００７７】また、本発明では、シリコン基板上にゲート絶縁膜を形成する工程と、ゲート絶縁膜上にシリコンからなる下部ゲート電極を形成する工程と、下部ゲート電極上にエッチングストッパー層を形成する工程と、エッチングストッパー層上に犠牲パターンを形成する工程と、下部ゲート電極および犠牲パターンをマスクとしてシリコン基板の所定量域に不純物を導入することでソース・ドレインを形成する工程と、下部ゲート電極，エッチングストッパー層，および，犠牲パターンの両側面に銅の拡散を阻止する絶縁材料からなる側壁を形成する工程と、下部ゲート電極，エッチングストッパー層，および，犠牲パターンを覆うようにシリコン基板上にシリコン酸化物からなる第１の層間絶縁膜を形成する工程と、第１の層間絶縁膜を選択的に除去して犠牲パターンの上面を露出させて下部ゲート電極上部に溝を形成する工程と、犠牲パターンを選択的に除去してエッチングストッパー層上面を露出させる工程と、エッチングストッパー層を除去する工程と、下部ゲート電極に密着して上面を覆い両端が側壁に接触するように銅の拡散を阻止する導電性を有する第１のバリア膜を形成する工程と、溝内に第１のバリア膜を介して銅からなる上部ゲート電極を形成して上部ゲート電極の底面が第１のバリア膜に覆われて両側面が側壁からなる第２のバリア膜に覆われた状態とする工程と、上部ゲート電極の露出している上面を塞ぐように銅の拡散を阻止する第３のバリア膜を形成する工程とを少なくとも備えるようにした。

【００７８】以上のように製造するようにしたので、上部ゲート電極は、電界効果トランジスタを構成する多の部分と第１～第３のバリア膜を介して接触した状態に作製される。すなわち、上部ゲート電極からの銅の拡散がすべての方向に対して阻止できるようになる。この結果、この発明は、電界効果トランジスタのゲート電極の材料に、トランジスタの特性を劣化させることなく銅を用いることができるようになるという極めて優れた効果を有している。また、第２のバリア膜は側壁で兼用されるなるので、工程の簡略化が可能となる。また、ソース・ドレインを形成した後で、銅からなる上部ゲート電極が形成されるので、ソース・ドレイン形成のための高温の活性化熱処理の後で、上部ゲート電極が形成されることになる。この結果、融点があまり高くない銅を用いて上部ゲート電極を構成することができる。

【図面の簡単な説明】

【図１】　本発明の第１の実施の形態における電界効果トランジスタの構成を模式的に示す示す断面図である。

【図２】　実施の形態１における電界効果トランジスタの製造方法を説明するための工程図である。

【図３】　図２に続く、実施の形態１における電界効果トランジスタの製造方法を説明するための工程図である。

【図４】　図３に続く、実施の形態１における電界効果トランジスタの製造方法を説明するための工程図である。

【図５】　図４に続く、実施の形態１における電界効果トランジスタの製造方法を説明するための工程図である。

【図６】　本発明の第２の実施の形態における電界効果トランジスタの製造方法を説明するための工程図である。

【図７】　図６に続く、実施の形態２における電界効果トランジスタの製造方法を説明するための工程図である。

【図８】　図７に続く、実施の形態２における電界効果トランジスタの製造方法を説明するための工程図である。

【図９】　図８に続く、実施の形態２における電界効果トランジスタの製造方法を説明するための工程図である。

【図１０】　本発明の他の形態における電界効果トランジスタの製造方法を説明するための工程図である。

【図１１】　図１０に続く、本発明の他の形態における電界効果トランジスタの製造方法を説明するための工程図である。

【図１２】　本発明の他の形態における電界効果トラン

ジスタの製造方法を説明するための工程図である。

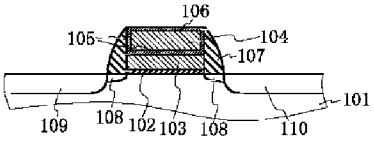
【図１３】　図１２に続く、本発明の他の形態における電界効果トランジスタの製造方法を説明するための工程図である。

【図１４】　従来よりある電界効果トランジスタの構成を示す断面図である。

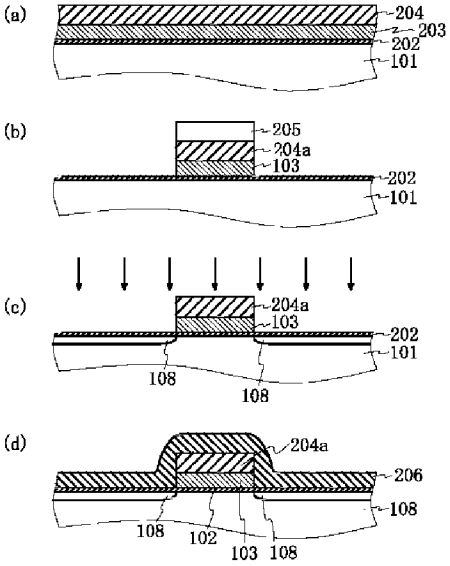
【符号の説明】

１０１…シリコン基板、１０２…ゲート絶縁膜、１０３…下部ゲート電極、１０４…上部ゲート電極、１０５…バリア膜（第１，第２のバリア膜）、１０６…バリア膜（第３のバリア膜）、１０７…サイドウォール、１０８…低濃度不純物領域、１０９…ソース、１１０…ドレイン。

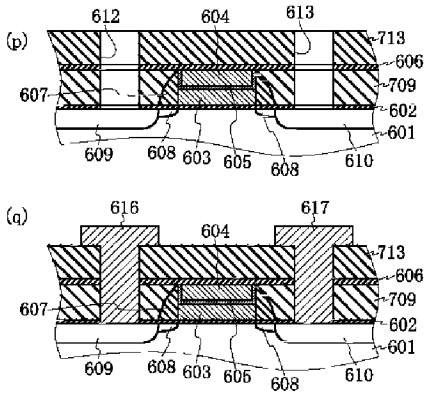
【図１】



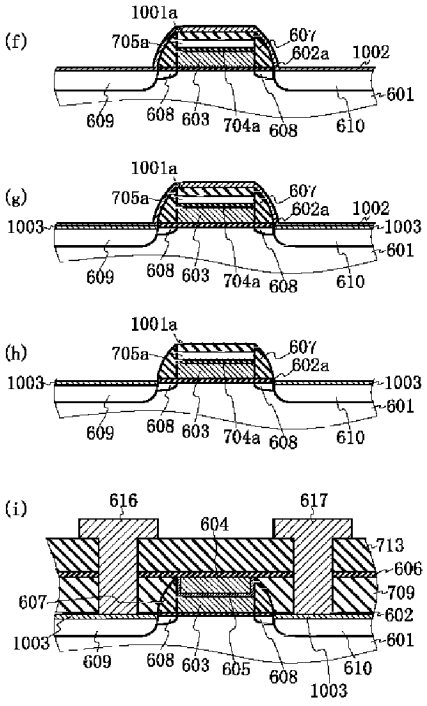
【図２】



【図９】

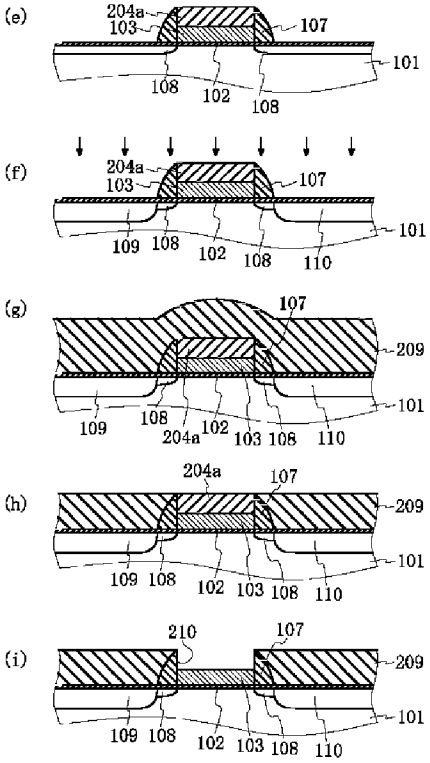


【図１１】

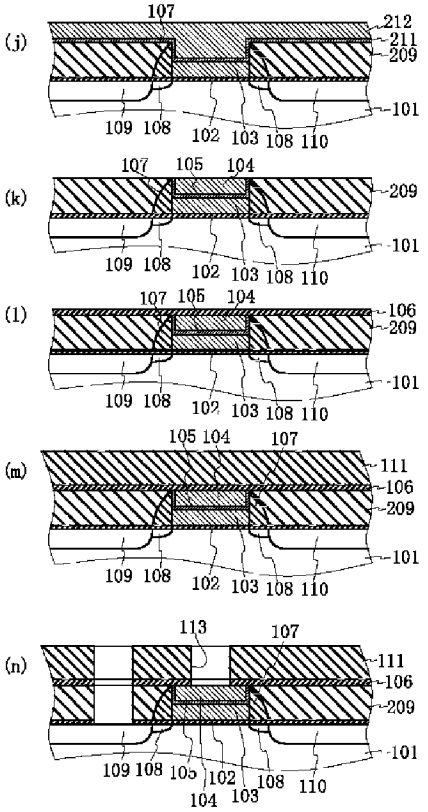


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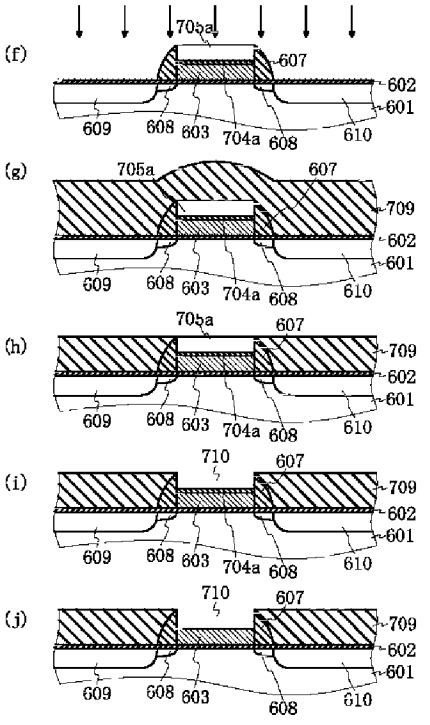
【図3】


(e)
204a
103
107
101
108
102
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(f)
204a
103
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108
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(g)
107
209
101
109
108
204a
102
103
108
110
(h)
204a
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(i)
210
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209
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110

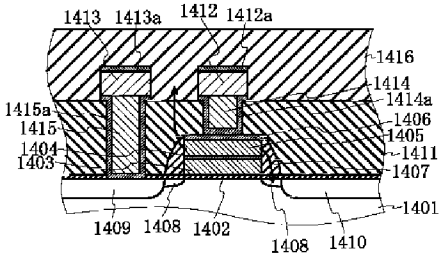
【図4】


(j)
107
212
211
209
101
109
108
102
103
108
110
(k)
107
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104
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101
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102
103
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110
(l)
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(m)
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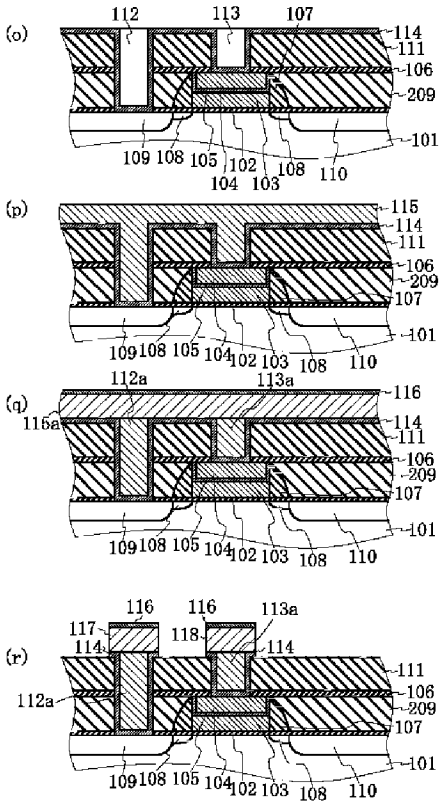
【図7】


(f)
705a
607
602
601
609
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603
704a
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610
(g)
705a
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709
602
601
609
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709
602
601
609
608
603
704a
608
610
(j)
710
607
709
602
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610

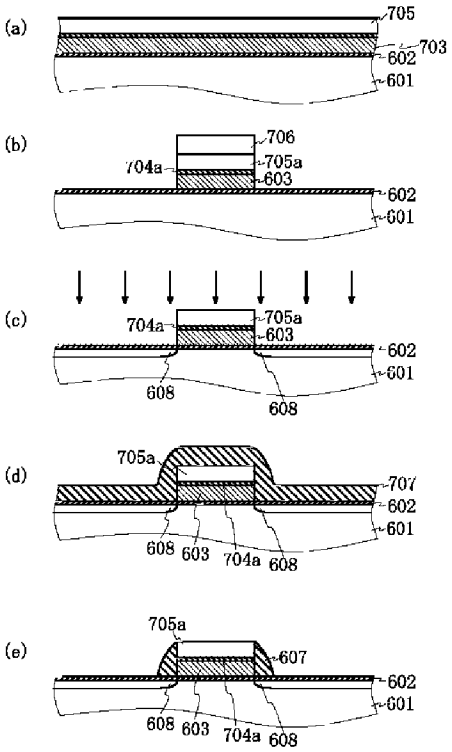
【図14】


1413
1413a
1412
1412a
1416
1414
1414a
1415a
1406
1415
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1404
1411
1403
1407
1401
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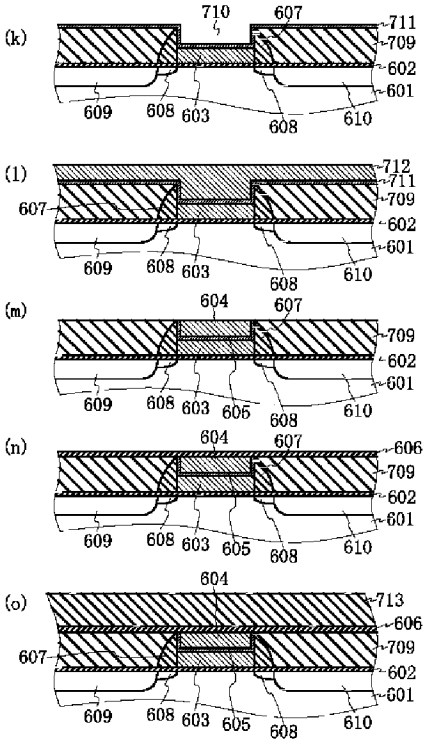
【図5】


(o)
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114
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104 103
(p)
115
114
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209
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101
109 108 105 104 102 103 108 110
(q)
112a
113a
116
115a
114
111
106
209
107
101
109 108 105 104 102 103 108 110
(r)
116
116
113a
117
118
114
114
111
112a
106
209
107
101
109 108 105 104 102 103 108 110

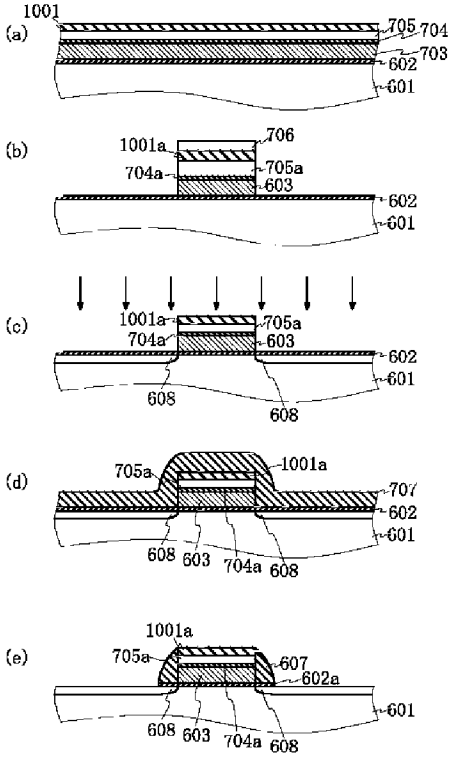
【図6】


(a)
705
703
602
601
(b)
706
704a
705a
603
602
601
(c)
704a
705a
603
602
601
608
608
(d)
705a
707
602
601
608 603 704a 608
(e)
705a
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608 603 704a 608

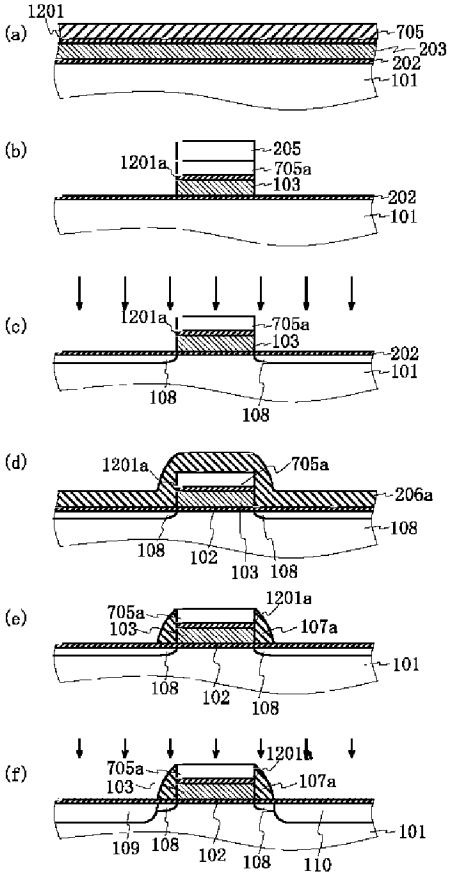
【図8】


(k)
710
607
711
709
602
601
609 608 603 608 610
(l)
712
711
709
607
602
601
609 608 603 608 610
(m)
604
607
709
602
601
609 608 603 605 608 610
(n)
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(o)
604
713
606
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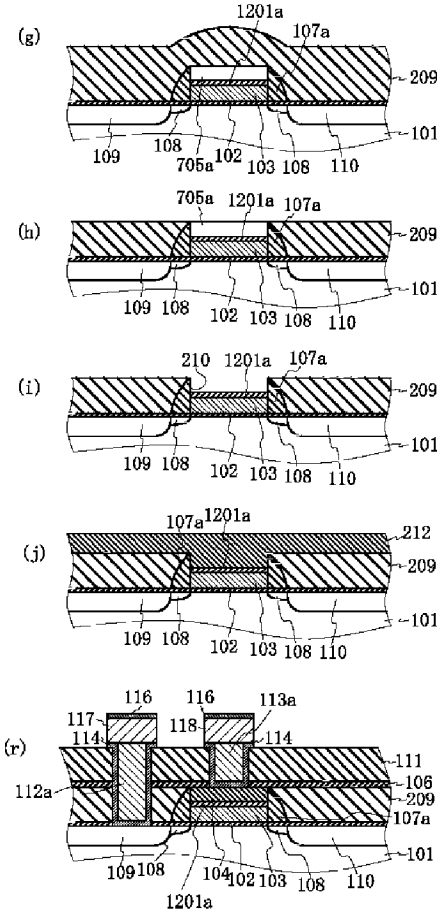
【図10】


(a)
1001
705
704
703
602
601
(b)
1001a
706
704a
705a
603
602
601
(c)
1001a
705a
704a
603
602
601
608
608
(d)
705a
1001a
707
602
601
608
603
704a
608
(e)
1001a
705a
607
602a
601
608
603
704a
608

【図12】


(a)
1201
705
203
202
101
(b)
1201a
205
705a
103
202
101
(c)
1201a
705a
103
202
101
108
108
(d)
1201a
705a
206a
108
108
102
103
108
(e)
705a
103
1201a
107a
101
108
102
108
(f)
705a
103
1201a
107a
101
109
108
102
108
110

【図13】


(g)
1201a
107a
209
101
109
108
705a
102
103
108
110
(h)
705a
1201a
107a
209
101
109
108
102
103
108
110
(i)
210
1201a
107a
209
101
109
108
102
103
108
110
(j)
107a
1201a
212
209
101
109
108
102
103
108
110
(r)
116
116
113a
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118
114
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107a
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JP2000228523A FIELD-EFFECT TRANSISTOR AND MANUFACTURE THEREOF

Applicants: NEC CORP

Inventors: MATSUKI TAKEO,NIIMURA TOSHIKI

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FIELD-EFFECT TRANSISTOR AND MANUFACTURE THEREOF

Abstract

PROBLEM TO BE SOLVED: To use copper for the material of a gate electrode without deterioration in characteristics of a transistor, by providing a first, second and third barrier films for an upper gate electrode to prevent diffusion of copper formed to respectively cover the lower, both and upper sides of the gate electrode. SOLUTION: A lower gate electrode 103 comprising polysilicon is provided on a silicon substrate 101 via a gate insulating film 102. An upper gate electrode 104 made of copper is provided on the lower gate electrode 103. Moreover, a barrier film 105 (a first and second barrier films) made of tantalum nitride is formed so as to cover the lower and side faces on the upper gate electrode and a barrier film 106 (a third barrier film) made of silicon nitride is formed to cover the upper face on the upper gate electrode 104. Accordingly, the upper gate electrode 104 is in a state which is covered with the barrier films 105, 106 like a cylinder. Thus, a gate electrode of a transistor is constituted by the lower gate electrode 103 and the upper gate electrode 104.

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DESCRIPTION JP2000228523

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a field effect transistor having a gate electrode having a structure in which silicon and copper are laminated and a method for manufacturing the same.

[0002]

2. Description of the Related Art In recent years, further miniaturization of LSI has been studied for higher performance and higher integration. Under such circumstances, along with the miniaturization, it is indispensable to reduce the resistance of the gate electrode of the field effect transistor for high performance. For this reason, the use of a two-layer structure of metal and polysilicon for the gate electrode material has been studied. Therefore, it has been proposed to configure the gate electrode with a two-layer structure of polysilicon and copper because of its low electric resistance and its workability and chemical stability superior to those of gold and silver.

[0003]

The conventional field effect transistor described above will be described. As shown in FIG. 14, a lower gate electrode 1403 made of polysilicon is provided on a silicon substrate 1401 via a gate insulating film 1402. Further, an upper gate electrode 1405 made of copper is provided on the

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lower gate electrode 1403 via a barrier film 1404 made of titanium nitride or the like. A barrier film 1406 made of titanium nitride or the like is provided on the upper gate electrode 1405. The lower gate electrode 1403 and the upper gate electrode 1405 form the gate electrode of the transistor.

[0004]

A sidewall 1407 made of silicon oxide is formed so as to cover the side surface of the gate electrode. Further, a low-concentration impurity region 1408 is formed in the silicon substrate 1401 below the sidewall 1407. A source 1409 and a drain 1410 are formed on the silicon substrate 1401 so as to sandwich the low concentration impurity region 1408. The low-concentration impurity region 1408, the source 1409 and the drain 1410, the gate insulating film 1402, and the gate electrode including the lower gate electrode 1403 and the upper gate electrode 1405 constitute a field effect transistor having an LDD structure. With this LDD structure, the single channel effect can be suppressed.

[0005]

Further, the above transistor is covered with an interlayer insulating film 1411 made of silicon oxide, and a gate electrode wiring 1412 and a source electrode wiring 1413 made of aluminum or the like are formed on the interlayer insulating film 1411. The gate electrode wiring 1412 is connected to the upper gate electrode 1405 via the barrier film 1406 by the plug 1414 in the through hole formed in the interlayer insulating film 1411. The plug 1414 is made of tungsten, and a barrier film 1414a made of titanium nitride or the like is formed on the side surface and the bottom surface of the plug 1414.

[0006]

Further, the source electrode wiring 1413 is connected to the source 1409 by a plug 1415 in a contact hole formed in the interlayer insulating film 1411. The plug 1415 is also made of tungsten, and a barrier film 1415a made of titanium nitride or the like is formed on the side surface and the bottom surface. Further, barrier films 1412a and 1413a made of titanium nitride or the like are also formed on the gate electrode wiring 1412 and the source electrode wiring 1413. Further, a protective insulating film 1416 is formed over the interlayer insulating film 1411 so as to cover the above-described wirings such as the gate electrode wiring 1412 and the

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source electrode wiring 1413.

[0007]

As described above, in order to further reduce the resistance, when the gate electrode is composed of a two-layer structure of polysilicon and copper, the upper gate electrode 1405 made of copper has a lower surface and an upper surface. In addition, barrier films 1404 and 1406 are provided to suppress the diffusion of copper into the lower polysilicon and the upper wiring metal. However, since copper also diffuses in the silicon oxide film, it diffuses in the sidewall 1407 and the interlayer insulating film 1411 which are silicon oxide, as shown by the arrow line in FIG. When copper diffuses in the direction of the silicon substrate 1401, problems such as generation of junction leakage current, reduction of on-current of the transistor, and fluctuation of threshold value occur. Further, if copper diffuses toward the upper wiring layer, there arises a problem of generation of inter-wiring leakage current.

[0008]
The present invention has been made to solve the above problems, and it is possible to use copper as a material of a gate electrode of a field effect transistor without deteriorating the characteristics of the transistor. To aim.

[0009]

A field effect transistor of the present invention comprises a lower gate electrode made of silicon formed on a silicon substrate via a gate insulating film, and copper formed on the lower gate electrode. An upper gate electrode, and a first barrier film having conductivity that allows injection of a sufficient current to drive the channel portion into the lower gate electrode and formed to cover the lower surface of the upper gate electrode to prevent diffusion of copper; The second barrier film is formed so as to cover the both side surfaces of the upper gate electrode so that the lower end of the first barrier film comes into contact with the second barrier film, and the second barrier film comes into contact with the end of the second barrier film. And a third barrier film formed so as to cover the upper surface of the upper gate electrode to prevent the diffusion of copper, and a source / drain formed on the silicon substrate so as to sandwich the region under the lower gate electrode. .

According to the present invention, the upper gate electrode made of copper is configured to be

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in contact with the other portion of the field effect transistor via the first, second, and first barrier films.

[0010]

In the above invention, a sidewall is formed on the side surfaces of the lower gate electrode and the upper gate electrode, and the second barrier film is formed by a part of the sidewall. In the above invention, the third barrier film is made of an insulating material. In the above invention, the upper surface of the upper gate electrode is opened, and the insulating layer is formed over the silicon substrate, and the third barrier film is formed to extend over the insulating layer. In the above invention, the first and second barrier films are made of a refractory metal or a refractory metal nitride. In the above invention, the first barrier film is made of an insulating material formed to have a thickness through which a tunnel current flows. In the above invention, the first, second, and third barrier films are made of a refractory metal or a refractory metal nitride. In the above invention, the barrier film is made of a material which does not contain oxygen as a constituent element. In the above invention, the insulating material is made of one of silicon nitride and boron nitride.

[0011]

In the above invention, the first barrier film is a multilayer film composed of a plurality of layers of two or more layers. In the above invention, the first barrier film is a layer made of a refractory metal, a layer made of a refractory metal silicide, a layer made of a compound of a refractory metal metal and silicon and nitrogen, or a nitride of a refractory metal. It is a multilayer film in which any one of the layers is combined and laminated in a plurality of layers. In the above invention, the first barrier film is a multilayer film in which the lowermost layer is a metal silicide layer or a layer made of a compound of a refractory metal metal, silicon, and nitrogen. In the above invention, in the first barrier film, the lowermost layer is composed of a metal silicide layer or a layer made of a compound of refractory metal metal and silicon and nitrogen. The metal silicide layer or refractory metal metal and silicon A multilayer film in which a layer of a refractory metal nitride is arranged on a layer made of a compound with nitrogen. In the above invention, in the first barrier film, the lowermost layer is composed of a metal silicide layer or a layer made of a compound of refractory metal metal and silicon and nitrogen. The metal silicide layer or refractory metal metal and silicon This is a multilayer film in which a layer of a refractory metal nitride is arranged on a layer made of a compound with nitrogen, and the uppermost layer is made of a refractory metal. In the above invention, the refractory metal silicide film is formed in a predetermined region on the surface of the source / drain.

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[0012]

In addition, the method of manufacturing a field effect transistor of the present invention includes a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and a sacrificial pattern on the lower gate electrode. Forming a source / drain by introducing impurities into a predetermined amount area of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask, and a step of forming a source / drain on the silicon substrate so as to cover the lower gate electrode and the sacrificial pattern. A step of forming a first interlayer insulating film made of silicon oxide, a step of removing the first interlayer insulating film to expose an upper surface of the sacrificial pattern, and a step of selectively removing the sacrificial pattern to form a lower gate electrode. Forming a groove on the upper part of the lower gate electrode of the first interlayer insulating film by exposing the upper surface, and first and second conductive materials that prevent diffusion of copper so as to cover the upper surface of the lower gate electrode and the side surface of the groove. Forming the barrier film, and forming an upper gate electrode made of copper in the groove through the first and second barrier films so that the bottom surface and both side surfaces of the upper gate electrode are the first and second barrier films. And a step of forming a third barrier film that blocks the diffusion of copper so as to cover the exposed upper surface of the upper gate electrode. According to the present invention, the upper gate electrode is formed in a state of being in contact with other portions forming the field effect transistor via the first to third barrier films. In the above invention, the sacrificial pattern is made of a material that is etched faster than silicon and silicon oxide under predetermined etching processing conditions.

[0013]

In addition, the method for manufacturing a field effect transistor of the present invention includes a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and an etching stopper on the lower gate electrode. A step of forming a layer, a step of forming a sacrificial pattern on the etching stopper layer, and a step of forming a source / drain by introducing an impurity into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask. Forming a first interlayer insulating film made of silicon oxide on the silicon substrate so as to cover the lower gate electrode and the sacrificial pattern, and removing the first interlayer insulating film to expose the upper surface of the sacrificial pattern. A step of selectively removing the sacrificial pattern to expose the upper surface of the etching

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stopper layer; a step of removing the etching stopper layer to expose the upper surface of the lower gate electrode to form a groove above the lower gate electrode; A step of forming first and second barrier films having conductivity so as to prevent diffusion of copper so as to cover the upper surface and the side surface of the groove, and an upper part made of copper in the groove via the first and second barrier films. Forming a gate electrode so that the bottom surface and both side surfaces of the upper gate electrode are covered with the first and second barrier films; and diffusing copper so as to cover the exposed upper surface of the upper gate electrode. And a step of forming a third barrier film for blocking. According to this invention, the upper gate electrode is formed in a state of being in contact with many portions forming the field effect transistor through the first to third barrier films.

[0014]

In addition, the method for manufacturing a field effect transistor of the present invention includes a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and an etching stopper on the lower gate electrode. A step of forming a layer, a step of forming a sacrificial pattern on the etching stopper layer, and a step of forming a source / drain by introducing an impurity into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask. A step of forming a first interlayer insulating film made of silicon oxide on the silicon substrate so as to cover the lower gate electrode and the sacrificial pattern, and selectively removing the first interlayer insulating film to expose the upper surface of the sacrificial pattern. Exposing and forming a groove above the lower gate electrode; selectively removing the sacrificial pattern to expose the upper surface of the etching stopper layer; and removing the etching stopper layer to expose the upper surface of the lower gate electrode. Forming a first and a second barrier film having conductivity to prevent the diffusion of copper so as to cover the upper surface of the lower gate electrode and the side surface of the groove, and through the first and second barrier films in the groove. Forming an upper gate electrode made of copper so that the bottom surface and both side surfaces of the upper gate electrode are covered with the first and second barrier films; and covering the exposed upper surface of the upper gate electrode. And a step of forming a third barrier film for preventing the diffusion of copper. According to this invention, the upper gate electrode is formed in a state of being in contact with many parts constituting the field effect transistor through the first to third barrier films. In the above invention, the sacrificial pattern is made of a material that is etched faster than silicon oxide under predetermined etching processing conditions.

[0015]

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In addition, the method of manufacturing a field effect transistor of the present invention includes a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and a sacrificial pattern on the lower gate electrode. And a step of forming a source / drain by introducing impurities into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask, and copper diffusion on both sides of the lower gate electrode and the sacrificial pattern. Forming a side wall made of an insulating material for preventing the above-mentioned process, forming a first interlayer insulating film made of silicon oxide on the silicon substrate so as to cover the lower gate electrode and the sacrificial pattern, and a first interlayer insulating film. Removing the film to expose the upper surface of the sacrificial pattern, selectively removing the sacrificial pattern to form a groove above the lower gate electrode, and covering the upper surface of the lower gate electrode so that both ends contact the sidewalls. A step of forming a conductive first barrier film for preventing diffusion of copper; and an upper gate electrode made of copper is formed in the groove through the first barrier film so that the bottom surface of the upper gate electrode is the first And a second barrier film having both side surfaces formed of sidewalls, and a third step of blocking the diffusion of copper so as to cover the exposed upper surface of the upper gate electrode. And a step of forming a barrier film. According to this invention, the upper gate electrode is formed in a state of being in contact with many parts constituting the field effect transistor through the first to third barrier films. The second barrier film is also used as the side wall.

[0016]

In addition, the method for manufacturing a field effect transistor of the present invention includes a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and an etching stopper on the lower gate electrode. A step of forming a layer, a step of forming a sacrificial pattern on the etching stopper layer, and a step of forming a source / drain by introducing an impurity into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask. A step of forming sidewalls made of an insulating material for preventing copper diffusion on both sides of the lower gate electrode, the etching stopper layer and the sacrificial pattern, and covering the lower gate electrode, the etching stopper layer and the sacrificial pattern. Forming a first interlayer insulating film of silicon oxide on the silicon substrate; removing the first interlayer insulating film to expose the upper surface of the sacrificial pattern; and selectively removing the sacrificial pattern. The step of exposing the upper surface of the etching stopper layer, the step of removing the etching stopper layer to form a groove in the upper part of the lower gate electrode, and the diffusion of copper so that both ends are in close contact with the upper surface and the sidewalls are in contact with each other.

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A step of forming a first barrier film having conductivity that blocks the above, and an upper gate electrode made of copper is formed in the groove through the first barrier film so that the bottom surface of the upper gate electrode is the first barrier film. And a third barrier film that blocks the diffusion of copper so as to cover the exposed upper surface of the upper gate electrode. And at least a forming step. According to this invention, the upper gate electrode is formed in a state of being in contact with many parts constituting the field effect transistor through the first to third barrier films. The second barrier film is also used as the side wall.

[0017]

In addition, the method for manufacturing a field effect transistor of the present invention includes a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and an etching stopper on the lower gate electrode. A step of forming a layer, a step of forming a sacrificial pattern on the etching stopper layer, and a step of forming a source / drain by introducing an impurity into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask. A step of forming a side wall made of an insulating material for preventing diffusion of copper on both sides of the lower gate electrode, the etching stopper layer, and the sacrificial pattern, and covering the lower gate electrode, the etching stopper layer, and the sacrificial pattern. Forming a first interlayer insulating film made of silicon oxide on a silicon substrate; and selectively removing the first interlayer insulating film to expose the upper surface of the sacrificial pattern to form a groove above the lower gate electrode. The step of selectively removing the sacrificial pattern to expose the upper surface of the etching stopper layer, the step of removing the etching stopper layer, and the step of closely adhering to the lower gate electrode and covering the upper surface so that both ends contact the sidewalls. A step of forming a conductive first barrier film for preventing diffusion of copper; and an upper gate electrode made of copper is formed in the groove through the first barrier film so that the bottom surface of the upper gate electrode is the first And a second barrier film having both side surfaces formed of sidewalls, and a third step of blocking the diffusion of copper so as to cover the exposed upper surface of the upper gate electrode. And a step of forming a barrier film. According to this invention, the upper gate electrode is formed in a state of being in contact with many parts constituting the field effect transistor through the first to third barrier films. The second barrier film is also used as the side wall.

[0018]

In the above invention, the sidewall is made of silicon nitride. In the above invention, the first

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barrier film nitrides the upper surface of the lower gate electrode to a thickness at which a tunnel current flows. In the above invention, the first or second barrier film is formed by a method of increasing the number of particles which are incident on the bottom surface of the groove at a vertical angle or an angle close to the vertical angle. In the above invention, a step of forming a refractory metal film after the upper surface of the lower gate electrode is exposed and a groove is formed, and a step of forming a refractory metal nitride film on the refractory metal film. The step of depositing copper, removing copper, the refractory metal film, and the nitride film of the refractory metal in regions other than the groove, and removing the upper gate electrode made of copper, the refractory metal film, and the nitride film of the refractory metal, And a step of forming the first and second barrier films. In the above invention, a step of forming a first refractory metal film after the upper surface of the lower gate electrode is exposed and a groove is formed, and a nitride film of refractory metal on the first refractory metal film. , A step of forming a second refractory metal film on the nitride film of the refractory metal, a step of forming copper, a copper in a region other than the groove, a first refractory metal The metal film, the refractory metal nitride film, and the second refractory metal film are removed, and the upper gate electrode made of copper and the first refractory metal film, the refractory metal nitride film, and the second refractory metal film are removed. And a step of forming first and second barrier films made of

[0019]

In the above invention, a step of forming a refractory metal film in contact with the lower gate electrode and a heat treatment to silicide the refractory metal film in contact with the lower gate electrode to contact the lower gate electrode with refractory metal film. Forming a silicide film and making it part of the first barrier film. In the above invention, the sacrifice layer, the etching stopper film, and the lower gate electrode are processed by a hard mask. In the above invention, the sacrifice layer, the etching stopper film, and the lower gate electrode are processed with a hard mask made of silicon oxide or silicon nitride. In the above invention, refractory metal silicide is formed in predetermined regions of the source / drain before forming the upper gate electrode.

[0020]

In the above invention, a step of forming a compound of a refractory metal, silicon and nitrogen after the upper surface of the lower gate electrode is exposed and a groove is formed, and a film of a compound of the refractory metal, silicon and nitrogen. A step of forming a nitride film of a refractory metal on top, a step of forming a copper film to be an upper gate electrode, and

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removing copper, a refractory metal film, and a nitride film of a refractory metal film in regions other than the groove. And at least a step of forming an upper gate electrode made of copper, a refractory metal film, and first and second barrier films made of a refractory metal nitride film. In the above invention, a step of forming a compound of a refractory metal, silicon and nitrogen after the upper surface of the lower gate electrode is exposed and a groove is formed, and a film of a compound of the refractory metal, silicon and nitrogen. A step of forming a refractory metal nitride film thereon, a step of forming a refractory metal film on the refractory metal nitride film, a step of forming copper to serve as an upper gate electrode, The copper, the first refractory metal film, the nitride film of the refractory metal film, and the second refractory metal film in the region 2) are removed, and the upper gate electrode and the first refractory metal film and refractory metal made of copper are removed. And forming a first barrier film and a second barrier film made of the second refractory metal film. In the above invention, a step of forming a refractory metal film in contact with the lower gate electrode and a heat treatment to react the refractory metal nitride film in contact with the lower gate electrode with silicon to contact the lower gate electrode with the refractory metal film. And a step of forming a compound film of silicon and nitrogen to form a part of the first barrier film.

[0021]

BEST MODE FOR CARRYING OUT THE INVENTION Embodiments of the present invention will be described below with reference to the drawings. First, the first embodiment of the present invention will be described. FIG. 1 is a sectional view showing the structure of the field effect transistor according to the first embodiment. The field-effect transistor according to the first embodiment first has a lower gate electrode 103 made of polysilicon on a silicon substrate 101 via a gate insulating film 102. An upper gate electrode 104 made of copper is provided on the lower gate electrode 103. In the upper gate electrode 104, a barrier film (first and second barrier films) 105 made of tantalum nitride is formed so as to cover the lower surface and side surfaces, and a barrier film made of silicon nitride (third barrier film) is formed so as to cover the upper surface. Barrier film) 106 is formed. Therefore, the upper gate electrode 104 is in a state of being covered with the barrier films 105 and 106 in a cylindrical shape. The lower gate electrode 103 and the upper gate electrode 104 form the gate electrode of the transistor.

[0022]

Further, a side wall (side wall) 107 made of silicon oxide is formed so as to cover the side surface of the gate electrode. Further, a low-concentration impurity region 108 is formed in the silicon substrate 101 below the sidewall 107. A source 109 and a drain 110 are formed on the silicon

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substrate 101 so as to sandwich the low concentration impurity region 108. Then, the low-concentration impurity region 108, the source 109 and the drain 110, the gate insulating film 102, and the gate electrode composed of the lower gate electrode 103 and the upper gate electrode 104 constitute a field effect transistor having an LDD structure. With the LDD structure, the single channel effect can be suppressed.

[0023]

As described above, in the field effect transistor according to the first embodiment, the gate electrode has the laminated structure made of polysilicon and copper, so that the resistance of the gate electrode is reduced. In the first embodiment, the copper portion forming the gate electrode is covered with the barrier film not only on the upper and lower surfaces but also on the side surfaces, so that the diffusion of copper through the silicon oxide film can be suppressed. Become. As a result, problems due to diffusion of copper, such as generation of junction leakage current and reduction of transistor on-current, are solved.

[0024]

Next, a method for manufacturing the field effect transistor according to the first embodiment described above will be described. First, as shown in FIG. 2A, an insulating film 202 having a film thickness of about 6 nm is formed on a silicon substrate 101 by dry oxidation. The insulating film 202 becomes a gate insulating film. Subsequently, a polysilicon film 203 having a film thickness of about 70 nm is formed on the insulating film 202 by the low pressure CVD method, and a silicon nitride film 204 having a film thickness of about 100 nm is also formed on the polysilicon film 203 by the low pressure CVD method.

[0025]

Next, as shown in FIG. 2B, the silicon nitride film 204 and the polysilicon film 203 are selectively removed by dry etching using the resist pattern 205 as a mask to form the lower gate electrode 103 and the sacrificial pattern 204a. To do. Next, after removing the resist pattern 205, as shown in FIG. 2C, the sacrificial pattern 204a and the lower gate electrode 103 are selectively ion-implanted to form a low-concentration impurity region (LDD) 108. To do. Here, As is ion-implanted with an implantation energy of 20 eV, and the implantation amount may be about $3 \times 10\ 13\ \mathrm{cm}\ -2$.

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[0026]

Next, as shown in FIG. 2D, a silicon oxide film 206 is formed on the entire surface. This may be performed by depositing silicon oxide by a low pressure CVD method using TEOS as a raw material. Then, by etching back the silicon oxide film 206 by reactive ion etching (RIE) having vertical anisotropy, as shown in FIG. 3E, the lower gate electrode 103 and the sacrificial pattern 204a are formed. Sidewalls 107 are formed on the side surfaces.

[0027]

Next, as shown in FIG. 3F, the source 109 and the drain 110 are formed by selectively ion-implanting the sacrificial pattern 204a, the lower gate electrode 103, and the sidewall 107 as a mask. Here, As may be ion-implanted at an implantation energy of 30 eV, and the implantation amount may be about 3×10 15 cm -2. Then, boron phosphorus silicate glass is deposited by CVD using ozone and TEOS as raw materials to form a lower interlayer insulating film 209 with a film thickness of about 500 nm as shown in FIG.

[0028]

Next, the lower interlayer insulating film 209 is planarized and polished by chemical mechanical polishing (CMP) of the oxide film to expose the upper portion of the sacrificial pattern 204a as shown in FIG. Next, the sacrificial pattern 204a is selectively removed by wet etching using a heated phosphoric acid aqueous solution, and as shown in FIG. 3I, the sidewall 107 and the lower interlayer insulating film 209 are formed on the lower gate electrode 103. Forming a groove 210 surrounded by. In this wet etching with hot phosphoric acid, since silicon and silicon oxide are not etched so much, the sacrificial pattern 204a made of silicon nitride can be selectively removed.

[0029]

By the way, in the above-described first embodiment, the upper portion of the sacrificial pattern 204a is exposed by removing the lower interlayer insulating film 209 by CMP, but the upper

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portion of the sacrificial pattern 204a is exposed by the following method. Good. For example, in the case where flattening is possible by reflow like boron silicate glass, the upper portion of the sacrificial pattern 204a may be exposed by removing it by dry etching or the like after the lower interlayer insulating film is reflowed and flattened. Good. At this time, in addition to boron silicate glass, silicate glass (BPSG) containing boron and phosphorus can be used as the lower interlayer insulating film.

[0030]

Further, an SOG (spin on glass) material is used as the lower interlayer insulating film, and is planarized by applying the material, and then the planarized application film is etched back by dry etching or the like to expose the upper portion of the sacrificial pattern 204a. You can Here, when the CMP method or the method of flattening using an SOG material and then etching back is used, the lower interlayer insulating film is formed by the CVD method or the like without using silicate glass. Or a silicon nitride film.

[0031]

Next, as shown in FIG. 4J, a tantalum nitride film is deposited on the lower interlayer insulating film 209 including the bottom and side surfaces of the groove 210 by a sputtering method to form a TaN film 211 with a film thickness of about 10 nm. Then, subsequently, copper is deposited on the TaN film 211 by sputtering to form a Cu layer 212 having a thickness of about 200 nm. Next, by removing the Cu layer 212 and the TaN film 211 by polishing, for example, by CMP of a metal film, as shown in FIG. The upper gate electrode 104 made of copper whose side surfaces are covered is formed, and in addition, the surface of the lower interlayer insulating film 209 other than the upper portion of the upper gate electrode 104 is exposed.

[0032]

Next, as shown in FIG. 4L, a barrier film 106 made of silicon nitride and having a film thickness of about 10 nm is formed on the entire surface. This may be performed by depositing silicon nitride by the plasma CVD method. As described above, the field effect transistor including the gate electrode composed of the lower gate electrode 103 made of polysilicon and the upper gate electrode 104 made of copper covered with the barrier film 105 and the barrier film 106 was formed. It will be.

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[0033]

Note that the barrier film 106 does not need to be formed to extend over the lower interlayer insulating film 209. As shown in FIG. 1, the barrier film 106 may be formed in a region where only the upper surface of the upper gate electrode 104 is covered with the barrier film 106. In this case, since the barrier film 106 does not extend onto the lower interlayer insulating film 209, the barrier film 106 may be made of, for example, tantalum nitride having the same conductivity as the barrier film 105.

[0034]

Thereafter, as shown in FIG. 4M, an interlayer insulating film 111 made of silicon oxide (BPSG) to which boron and phosphorus are added is formed on the barrier film 106 to have a film thickness of about 500 nm. This may be formed, for example, by a CVD method using oxygen gas and TEOS as raw materials. Next, as shown in FIG. 4N, the contact hole 112 and the through hole 113 are formed. This may be formed by anisotropic dry etching using a resist pattern formed by a known photolithography graph as a mask. The contact hole 112 has a bottom surface exposing the surface of the source substrate 109 of the silicon substrate 101, and a bottom surface of the through hole 113 exposing the upper surface of the upper gate electrode 104.

[0035]

Next, as shown in FIG. 5O, a barrier film 114 having a two-layer structure of titanium nitride and titanium is formed on the interlayer insulating film 111 including the side surfaces and bottom surfaces of the contact hole 112 and the through hole 113. This may be formed by the CVD method and the film thickness may be about 50 nm and 10 nm, respectively. Subsequently, as shown in FIG. 5P, a W film 115 made of tungsten is formed on the barrier film 114 to have a film thickness of about 400 nm by, for example, a low pressure CVD method.

[0036]

Next, the W film 115 is removed by dry etching or the like to the extent that the contact hole

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112 and the through hole 113 are filled. As a result, after forming the plugs 112a and 113a (FIG. 5 (q)), an alloy film 115a made of an aluminum-copper alloy with copper of about 1% is formed by sputtering to a thickness of about 500 nm. In addition, the barrier film 116 made of titanium nitride is formed to a thickness of about 30 nm by the sputtering method. Then, by patterning the alloy film 115a and the barrier films 114 and 116, the source electrode wiring 117 and the gate electrode wiring 118 can be formed as shown in FIG.

[0037]

When manufactured as described above, the upper gate electrode made of copper is formed after forming the source / drain. That is, since the upper gate electrode is formed after the high-temperature activation heat treatment for forming the source / drain, the upper gate electrode can be formed by using copper having a not so high melting point. Although tantalum nitride is used as the barrier film (first and second barrier films) 105 in the first embodiment, the invention is not limited to this, and titanium nitride, tungsten nitride, tantalum nitride, molybdenum nitride are not limited thereto. A nitride (a compound of refractory metal and silicon and nitrogen) such as titanium nitride silicide or tungsten nitride silicide, or a metal material such as tantalum or titanium tungsten may be used.

[0038]

By the way, for the barrier films (first to third barrier films) described above, a material having a function of preventing diffusion of copper, which does not contain oxygen as a constituent element, may be used. Since the upper gate electrode is made of copper, the oxidation of copper can be suppressed without oxygen in this way. Further, for example, silicon nitride may be used for the barrier film (first barrier film) arranged on the lower surface of the upper gate electrode. That is, since it is sufficient for the barrier film to have a conductivity capable of injecting a current sufficient for driving the channel portion into the lower gate electrode, the film thickness may be set so that a tunnel current flows even if silicon nitride is used. In this case, if the surface of the lower gate electrode is nitrided by, for example, about 2 nm, the barrier film can be formed in this nitrided portion.

[0039]

Further, the barrier film (first barrier film) arranged between the barrier film (second barrier

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film) arranged on the side surface of the above-mentioned copper upper gate electrode and the lower gate electrode has two or more layers. It may be a multilayer film composed of a film. When diffusing in a solid, there is a high possibility that the diffusing species will be deposited at the interface or grain boundary of the solid material (when the film is polycrystalline). Therefore, by forming a multilayer film in which barrier films are laminated, it is possible to capture a slight amount of copper that diffuses at the interface between the films and further prevent diffusion of diffusion species. The multilayer film is preferably a high melting point metal or a high melting point metal composite film. For example, a composite film of Ta and Ta nitride may be used. Since metals such as copper are less likely to diffuse into thermally stable metal nitrides, the use of a refractory metal nitride film as the barrier film also reduces the amount of point defects, and the diffusion of copper via point defects is suppressed. It

[0040]

Disposing the refractory metal silicide in contact with the silicon lower gate electrode as a part of the first barrier film having a multilayer film structure is also effective in improving the operating performance of the field effect transistor. This is because the Schottky barrier formation is suppressed and the contact resistance is reduced at the interface between the silicide and silicon. In the first barrier film of the multi-layer film, using a film having a high melting point as a film in contact with copper is also effective in improving the adhesion between the copper and the first barrier film. It is also effective to improve the device manufacturing yield that the compound of the refractory metal, silicon and nitrogen is arranged in contact with the lower electrode of silicon as a part of the first barrier film having the multilayer film structure. This is because the above compounds have good adhesion to silicon. For example, the above compound can be formed by forming a film of tungsten nitride in the groove by a CVD method, a reactive collimating sputtering method, or the like, and performing a heat treatment at a temperature of about 500 ° C. At this time, since the above compound is formed by the reaction between silicon and the refractory metal nitride, the adhesion with silicon is improved.

[0041]

Second Embodiment Next, a second embodiment of the present invention will be described. First, a method of manufacturing the field effect transistor of the second embodiment will be described. First, as shown in FIG. 6A, a gate insulating film 602 having a film thickness of about 6 nm is formed on a silicon substrate 601 by dry oxidation. Subsequently, a polysilicon film 703 in which an n-type impurity is introduced is formed to a film thickness of about 50 nm on the gate insulating film 602 by a low pressure CVD method, and a silicon oxide film 704 is formed

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thereon to a film thickness of about 10 nm by a CVD method. To form. In addition, a polysilicon film 705 having a film thickness of about 100 to 300 nm is formed on the silicon oxide film 704 by the CVD method.

[0042]

Next, as shown in FIG. 6B, the polysilicon film 705, the silicon oxide film 704, and the polysilicon film 703 are selectively removed by dry etching using the resist pattern 706 as a mask, and the lower gate electrode is formed. 603, an etching stopper layer 704a, and a sacrificial pattern 705a are formed. Next, after removing the resist pattern 706, as shown in FIG. 6C, the sacrificial pattern 705a and the lower gate electrode 603 are selectively ion-implanted to form a low-concentration impurity region (LDD) 608. To do. Here, As is ion-implanted with an implantation energy of 20 eV, and the implantation amount may be about 1 × 10 13 cm −2.

[0043]

Next, as shown in FIG. 6D, a silicon oxide film 707 is formed on the entire surface. This may be performed by depositing silicon oxide by a low pressure CVD method using TEOS as a raw material. Then, by etching back the silicon oxide film 707 by reactive ion etching (RIE) having vertical anisotropy, as shown in FIG. 6E, the lower gate electrode 603 and the sacrificial pattern 705a are formed. Sidewalls 607 are formed on the side surfaces. The sidewall 607 may be made of silicon nitride. In this case as well, it can be formed similarly to the case of forming from silicon oxide.

[0044]

Next, the source 609 and the drain 610 are formed by selectively ion-implanting the sacrificial pattern 705a, the lower gate electrode 603, and the sidewall 607 as a mask. Here, As is ion-implanted with an implantation energy of 30 eV, and the implantation amount may be about 2 × 10 15 cm −2. Note that the impurity introduction region formed by ion implantation is subjected to heat treatment at 800 ° C. for 10 minutes and 1000 ° C. for 10 seconds in a nitrogen atmosphere, for example, to reduce defects and activate impurities.

[0045]

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Next, boron phosphorus silicate glass is deposited by CVD using ozone and TEOS as raw materials, and these are heated and allowed to flow, so that the lower interlayer film is formed to a film thickness of about 400 to 600 nm as shown in FIG. 7 (g). An insulating film 709 is formed. Next, the lower interlayer insulating film 709 is removed by a predetermined thickness by, for example, chemical mechanical polishing (CMP) of the oxide film to expose the upper portion of the sacrificial pattern 705a as shown in FIG. Next, the sacrificial pattern 705a is selectively removed by reactive ion etching having a high selectivity with respect to the oxide film, and as shown in FIG. 7I, the sidewall 607 and the lower portion are formed above the lower gate electrode 603. A groove 710 surrounded by the interlayer insulating film 709 is formed.

[0046]

Subsequently, as shown in FIG. 7J, the etching stopper layer 704a is removed by an etching method having a selection ratio with silicon oxide, and the upper surface of the lower gate electrode 603 is exposed at the bottom of the groove 710. Next, as shown in FIG. 8K, a tantalum nitride film is deposited on the lower interlayer insulating film 709 including the bottom and side surfaces of the groove 710 by sputtering to form a TaN film 711 with a film thickness of about 10 nm. Subsequently, as shown in FIG. 8 (l), copper is deposited on the TaN film 711 by sputtering, and the deposited copper is heated and flowed to form a film having a flat surface with a thickness of about 100 to 500 nm. A Cu layer 712 is formed.

[0047]

Here, instead of the TaN film 711, a thin film of titanium nitride, tantalum, tungsten nitride, titanium tungsten, or the like may be used. Further, the Cu layer 612 may be formed by, for example, an electroplating method or a CVD method. Next, by removing the Cu layer 712 and the TaN film 711 by CMP of a metal film, for example, the lower surface and the side surface are covered with the barrier film 605 made of tantalum nitride, as shown in FIG. The upper gate electrode 604 made of copper is formed, and in addition, the surface of the lower interlayer insulating film 709 other than the upper gate electrode 604 is exposed. Instead of the TaN film 711, a laminated film of high melting point gold and high melting point metal nitride such as TaN / Ta or Ta / TaN / Ta film may be used.

[0048]

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Further, by using the collimating sputtering method as the above-described method for forming the laminated film, the layer resistance of the gate electrode is reduced and the layer resistance is prevented from increasing when the width of the groove is reduced. According to the collimate sputtering method, the particles sputtered by the plasma from the raw material target depending on the film formation have an angle of incidence on the substrate which is almost vertical due to the collimator. Therefore, the film thickness formed on the side wall in the groove is thinner than the film thickness formed on the bottom of the groove. When the resistivity of the material of the barrier film is higher than that of copper, if the film thickness on the side surface is large, the resistance increases in proportion to this film thickness. Also, when the width of the groove is reduced, the layer resistance is increased. Therefore, it is better to reduce the film thickness formed on the side wall in the groove by the above-mentioned collimating sputtering method. The same effect can be obtained by a method called ionization sputtering method. The ionization sputtering method is a method in which raw material particles ionized by a bias applied to the substrate are incident on the substrate at an angle close to vertical, and the incident particles are deposited to form a film, which is also formed on the sidewall of the groove. The film thickness can be reduced.

[0049]

Next, as shown in FIG. 8N, a barrier film 606 made of titanium oxide or silicon nitride and having a film thickness of about 10 to 100 nm is formed on the entire surface. This may be formed by, for example, a reactive sputtering method. As described above, the field effect transistor including the gate electrode composed of the lower gate electrode 603 made of polysilicon and the upper gate electrode 604 made of copper covered with the barrier film 605 and the barrier film 606 was formed. It will be. Note that the barrier film 606 does not need to be formed to extend over the lower interlayer insulating film 709. The barrier film 606 may be formed in a region where only the upper surface of the upper gate electrode 604 is covered with the barrier film 606. In this case, since the barrier film 606 does not extend on the lower interlayer insulating film 709, the barrier film 606 may be made of, for example, the same tantalum nitride as the barrier film 605.

[0050]

After that, as shown in FIG. 8O, an interlayer insulating film 713 made of silicon oxide (BPSG) to which boron and phosphorus are added is formed on the barrier film 606 to have a film

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thickness of about 100 to 500 nm. This may be formed, for example, by a CVD method using oxygen gas and TEOS as raw materials. Next, as shown in FIG. 9P, contact holes 612 and 613 are formed. This may be formed by anisotropic dry etching using a resist pattern formed by a known photolithography graph as a mask. The contact hole 612 exposes the source 609 surface of the silicon substrate 601 on the bottom surface, and the contact hole 613 exposes the drain 610 surface of the silicon substrate 601 on the bottom surface.

[0051]

Then, as shown in FIG. 9Q, the source electrode wiring 616 and the drain electrode wiring 617 made of aluminum or the like may be formed through the contact holes 612 and 613. As described above, also in the second embodiment, since the gate electrode has the laminated structure of polysilicon and copper, the resistance of the gate electrode is reduced. Further, also in the second embodiment, since the copper portion forming the gate electrode is covered not only with the upper and lower surfaces of the body portion but also with the side surfaces thereof, the diffusion of copper through the silicon oxide film is also prevented. Can be suppressed. As a result, problems due to diffusion of copper, such as generation of junction leakage current and reduction of transistor on-current, are solved.

[0052]

Further, also in the second embodiment, after forming the source / drain, the upper gate electrode made of copper is formed. That is, since the upper gate electrode is formed after the high-temperature activation heat treatment for forming the source / drain, the upper gate electrode can be formed by using copper having a not so high melting point.

[0053]

By the way, the sidewall may be made of silicon nitride. When the sidewall is formed of a material such as silicon nitride that can prevent diffusion of copper, the sidewall can be used as a barrier film (second barrier film) arranged on the side surface of the upper gate electrode. In this case, it is not necessary to newly form a barrier film to be arranged on the side surface of the upper gate electrode. That is, for example, as shown in FIG. 4J, a tantalum nitride film is not deposited on the lower interlayer insulating film 209 including the bottom and side surfaces of the groove 210 by a sputtering method. It is nitrided to some extent to form a first barrier film.

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As described above, since a tunnel current flows in the case of silicon nitride having a film thickness of about 2 nm, there is no problem in conduction with the upper gate electrode.

[0054]

At this time, it is needless to say that instead of nitriding the upper portion of the lower gate electrode 103, a material having other conductivity that can prevent diffusion of copper may be formed on the upper portion of the lower gate electrode 103. Absent. Then, by forming the upper gate electrode 104 on the first barrier film, the lower surface and both side surfaces of the upper gate electrode 104 can be covered with silicon nitride that prevents diffusion of copper. After this, the field effect transistor according to the present invention can be obtained by performing the same steps as those of FIG.

[0055]

Further, if the side wall is made less likely to be etched than silicon oxide such as silicon nitride under a predetermined etching condition, it becomes easy to contact the wiring on the upper gate electrode. This is due to the following reasons. First, a contact hole is formed in the interlayer insulating film formed on the upper gate electrode, and a wiring is connected to the upper gate electrode through this contact hole. This is because the silicon nitride is hardly etched by the etching of the interlayer insulating film made of silicon oxide at the time of forming the contact hole, so that the sidewall is not etched even if the contact hole forming position is slightly shifted.

[0056]

By the way, in the above, as shown in FIG. 6B, the lower layer is processed by using the resist pattern 706 as a mask, but the present invention is not limited to this, and as described below, a hard mask made of silicon oxide is used. You may make it process using. In addition, by using the hard mask, silicide of refractory metal can be selectively formed in the source / drain regions.

[0057]

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First, as shown in FIG. 10A, a gate insulating film 602 having a film thickness of about 6 nm is formed on a silicon substrate 601 by dry oxidation. Subsequently, a polysilicon film 703 in which an n-type impurity is introduced is formed to a film thickness of about 50 nm on the gate insulating film 602 by a low pressure CVD method, and a silicon oxide film 704 is formed thereon to a film thickness of about 10 nm by a CVD method. Then, a polysilicon film 705 having a film thickness of about 100 to 300 nm is formed on the silicon oxide film 704 by the CVD method. In addition, a silicon oxide film 1001 is formed on the polysilicon film 705a. Note that this silicon oxide film may be a silicon nitride film.

[0058]

Next, as shown in FIG. 10B, the polysilicon film 705, the silicon oxide film 704, the polysilicon film 703, and the silicon oxide film 1001 are selectively etched by dry etching using a resist pattern 706 as a mask. Then, the lower gate electrode 603, the etching stopper layer 704a, and the sacrificial pattern 705a are formed, and the hard mask 1001a is formed. Next, after removing the resist pattern 706, as shown in FIG. 10C, the low concentration impurity region (LDD) 608 is formed. The LDD 608 may be ion-implanted with As at an implantation energy of 20 eV, and the implantation amount may be about $1 \times 10\ 13\ \mathrm{cm}\ -2$.

[0059]

Next, as shown in FIG. 10D, a silicon oxide film 707 is formed on the entire surface by depositing silicon oxide by a low pressure CVD method using TEOS as a raw material. Then, the silicon oxide film 707 is etched back by reactive ion etching (RIE) having vertical anisotropy, so that the lower gate electrode 603 and the sacrificial pattern 705a are formed as shown in FIG. Sidewalls 607 are formed on the side surfaces. At the same time, a region of the gate insulating film 602 which is not covered with the lower gate electrode 603 and the sidewall 607 is removed. The sidewall 607 may be made of silicon nitride. In this case as well, it can be formed similarly to the case of forming from silicon oxide.

[0060]

Next, the source 609 and the drain 610 are formed by selectively ion-implanting the sacrificial pattern 705a, the lower gate electrode 603, and the sidewall 607 as well as the hard mask 1001a as a mask. Also here, As is ion-implanted with an implantation energy of 30 eV, and the

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implantation amount may be about 2 × 10 15 cm −2. Note that the impurity introduction region formed by ion implantation is subjected to heat treatment at 800 ° C. for 10 minutes and 1000 ° C. for 10 seconds in a nitrogen atmosphere, for example, to reduce defects and activate impurities.

[0061]

Further, since the hard mask 1001a is used, it is possible to form the silicide on the surface of the source / drain region in a self-aligned manner without forming the silicide on the sacrificial pattern 705a made of silicon. As shown in FIG. 11 (f), a refractory metal film 1002 is formed by depositing cobalt in a film thickness of 10 to 20 nm on the entire region by a sputtering method or the like, and heated by an RTA (Rapid Thermal Anneal) method to form a base. Silicon (silicon substrate 601) is reacted with the refractory metal film 1002 to selectively form a silicide 1003 on the source 609 and the drain 610 as shown in FIG. The heating temperature for forming this silicide is preferably about 650 to 750 ° C. The atmosphere for heating is preferably an inert atmosphere such as nitrogen or argon.

[0062]

After forming the silicide, as shown in FIG. 11H, the underlying silicon and unreacted cobalt are selectively removed by wet etching using a mixed aqueous solution of hydrochloric acid: hydrogen peroxide: water. When heated in a nitrogen atmosphere, nitrided cobalt is produced, so this nitrided cobalt is also selectively removed by wet etching using a mixed aqueous solution of hydrochloric acid: hydrogen peroxide: water. After that, the resistance of the silicide can be lowered by heating again at a temperature of about 750 to 850 ° C. by the RTA method. In addition to cobalt, titanium (10 to 30 nm) may be used as the refractory metal. When titanium is used, the excess titanium or titanium nitride immediately after the silicide processing may be removed by wet etching with a mixed aqueous solution of ammonia: hydrogen peroxide solution: water.

[0063]

After the silicide is selectively formed in the source / drain regions, the lower interlayer insulating film 709 is formed to have a film thickness of about 400 to 600 nm as in the case of FIG. The lower interlayer insulating film 709 is removed by a predetermined thickness by

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polishing (CMP), and at the same time, the hard mass is also removed to expose the upper portion of the sacrificial pattern 705a. Thereafter, by performing the same process as shown in FIGS. 7H to 9Q, as shown in FIG. 11I, in addition to the configuration shown in FIG. A state in which is formed is obtained. Since the silicide 1003 is selectively formed on the source 609 and the drain 610, the contact resistance of the source electrode wiring 616 and the drain electrode wiring 617 can be reduced.

[0064]

The formation of silicide may be applied to the field effect transistor of the first embodiment described above. For example, when the side wall 107 shown in FIG. 3E is formed, if the portions of the gate insulating film 102 on the regions to be the source / drain are simultaneously removed, the surface of the silicon substrate 101 to be the source / drain is exposed. .. After that, as in the case of FIG. 3F, if the source 109 and the drain 110 are formed and a film of a refractory metal such as cobalt or titanium is formed over the entire area, then FIG. 11F to FIG. Similarly, silicide can be selectively formed on the source / drain. In the first embodiment, since the sacrificial pattern 204a is made of silicon nitride and the sidewall 107 is made of silicon oxide, no silicide is formed on these surfaces. Thus, if the sidewall surface or the sacrificial film surface is hard to react with the refractory metal, it becomes possible to easily form the silicide selectively on the source / drain.

[0065]

Next, a method of manufacturing the field effect transistor when the above-mentioned wall is used again as the second barrier film will be described. First, as shown in FIG. 12A, an insulating film 202 having a film thickness of about 6 nm is formed on a silicon substrate 101 by dry oxidation. The insulating film 202 becomes a gate insulating film. Subsequently, a polysilicon film 203 having a film thickness of about 70 nm is formed on the insulating film 202 by a low pressure CVD method, and in this case, a tantalum nitride film is deposited on the polysilicon film 203 by a sputtering method to have a film thickness of about 10 nm. Then, a TaN film 1201 is formed. Then, a polysilicon film 705 having a thickness of about 100 nm is formed on the TaN film 1201 by a low temperature CVD method of about 400 ° C. or a plasma CVD method.

[0066]

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Next, as shown in FIG. 12B, the polysilicon film 705, the TaN film 1201, and the polysilicon film 203 are selectively removed by dry etching using the resist pattern 205 as a mask, and the lower gate electrode 103 and A sacrificial pattern 705a is formed, and a barrier film (first barrier film) 1201a sandwiched between them is formed. Next, after removing the resist pattern 205, as shown in FIG. 12C, the sacrificial pattern 705 and the lower gate electrode 103 are selectively ion-implanted to form a low-concentration impurity region (LDD) 108. To do. Also here, As may be ion-implanted with an implantation energy of 20 eV, and the implantation amount may be about $3 \times 10\ 13\ cm\ -2$.

[0067]

Next, as shown in FIG. 12D, a silicon nitride film 206a is formed on the entire surface. Then, by etching back the silicon nitride film 206a by reactive ion etching (RIE) having vertical anisotropy, as shown in FIG. 12E, the lower gate electrode 103, the barrier film 1201a, A sidewall 107a is formed on the side surface of the sacrificial pattern 705a. Since the sidewall 107a is made of silicon nitride, it can be used as a second barrier film that suppresses the diffusion of copper. Next, as shown in FIG. 12F, the source 109 and the drain 110 are formed by selectively implanting ions using the sacrificial pattern 705a, the lower gate electrode 103, and the sidewall 107a as a mask. To form the source 109 and the drain 110, As may be ion-implanted with an implantation energy of 30 eV, and the implantation amount may be about $3 \times 10\ 15\ cm\ -2$.

[0068]

Then, boron phosphorus silicate glass is deposited by CVD using ozone and TEOS as raw materials to form a lower interlayer insulating film 209 with a film thickness of about 500 nm as shown in FIG. Next, the lower interlayer insulating film 209 is planarized and polished by chemical mechanical polishing (CMP) of the oxide film to expose the upper portion of the sacrificial pattern 705a as shown in FIG. Next, the sacrificial pattern 705a is selectively removed under the condition that the polysilicon is selectively etched, and as shown in FIG. 13I, a side surface is formed above the lower gate electrode 103 whose upper surface is covered with the barrier film 1201a. A groove 210 surrounded by the wall 107a and the lower interlayer insulating film 209 is formed.

[0069]

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Next, as shown in FIG. 13J, copper is deposited on the lower interlayer insulating film 209 (barrier film 1201a) including the bottom and side surfaces of the groove 210 by sputtering to form a Cu layer 212 having a film thickness of about 200 nm. To form. After that, by performing the same processing as that of FIG. 4 (k) to FIG. 5 (q), such as removing the Cu layer 212 by polishing, for example, by CMP of the metal film, as shown in FIG. 13 (r). Thus, a field effect transistor using the sidewall 107a as the second barrier film can be formed.

[0070]

Note that a thin silicon oxide film is formed after the TaN film 1201 is formed and before the polysilicon film is formed, so that a silicon oxide film is formed between the barrier film (first barrier film) 1201a and the sacrificial pattern 705a. An etching stopper layer may be provided. By providing the etching stopper layer, the selective removal of the sacrificial pattern 705a becomes easier. The etching stopper layer can be selectively removed with respect to the barrier film and the sidewall by, for example, wet etching using a hydrofluoric acid solution. In this case, the lower interlayer insulating film 209 is also etched to some extent. As described above, since the upper gate electrode can be formed to have the same width as the lower gate electrode, the width of the upper gate electrode becomes longer than that in the first embodiment, and the resistance of the upper gate electrode is reduced.

[0071]

As described above, according to the present invention, the lower gate electrode made of silicon formed on the silicon substrate via the gate insulating film, and the upper gate made of copper formed on the lower gate electrode. An electrode, a first barrier film having conductivity that allows a sufficient current to drive the channel portion into the lower gate electrode, and formed to cover the lower surface of the upper gate electrode to prevent the diffusion of copper; A second barrier film formed to cover both side surfaces of the upper gate electrode so as to prevent the diffusion of copper, the second barrier film having a lower end in contact with the first barrier film, and an upper end in contact with the second barrier film. A third barrier film formed so as to cover the upper surface of the gate electrode to prevent the diffusion of copper, and a source / drain formed on the silicon substrate so as to sandwich the region under the lower gate electrode were provided. Therefore, the upper gate electrode is configured to be in contact with many portions forming the field effect transistor via the first to third barrier films. That is, the diffusion of copper from the upper gate electrode can be blocked in all directions. As a result, the present invention has an extremely excellent effect that copper can be used as the material of the gate electrode of the field effect transistor without deteriorating the characteristics of the

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transistor.

[0072]
Further, in the present invention, a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, a step of forming a sacrificial pattern on the lower gate electrode, a lower step A step of forming a source / drain by introducing an impurity into a predetermined amount region of the silicon substrate using the gate electrode and the sacrificial pattern as a mask, and a step of forming a silicon oxide film on the silicon substrate to cover the lower gate electrode and the sacrificial pattern. Forming the first interlayer insulating film, removing the first interlayer insulating film to expose the upper surface of the sacrificial pattern, and selectively removing the sacrificial pattern to expose the upper surface of the lower gate electrode. Forming a groove above the lower gate electrode of the interlayer insulating film, and forming conductive first and second barrier films that prevent copper diffusion so as to cover the upper surface of the lower gate electrode and the side surface of the groove. And an upper gate electrode made of copper is formed in the groove through the first and second barrier films so that the bottom surface and both side surfaces of the upper gate electrode are covered with the first and second barrier films. At least a step and a step of forming a third barrier film that blocks the diffusion of copper so as to cover the exposed upper surface of the upper gate electrode are provided.

[0073]
In the present invention, a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and a step of forming an etching stopper layer on the lower gate electrode, A step of forming a sacrificial pattern on the etching stopper layer, a step of forming a source / drain by introducing impurities into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask, a lower gate electrode and a sacrificial pattern Forming a first interlayer insulating film made of silicon oxide on the silicon substrate so as to cover the upper surface of the lower gate electrode by selectively removing the first interlayer insulating film to expose the upper surface of the sacrificial pattern. Forming a groove in the trench, selectively removing the sacrificial pattern to expose the upper surface of the etching stopper layer, removing the etching stopper layer to expose the upper surface of the lower gate electrode, A step of forming first and second conductive barrier films that prevent the diffusion of copper so as to cover the side surfaces, and an upper gate electrode made of copper in the trench via the first and second barrier films. A step of forming the bottom surface and both side surfaces of the upper gate electrode so as to be covered with the first and second barrier films, and a step of blocking diffusion of copper so as to cover the exposed upper surface of the upper gate electrode. And a step of forming a barrier film of No. 3 are provided.

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[0074]

Since it is manufactured as described above, the upper gate electrode is manufactured in a state of being in contact with many parts constituting the field effect transistor via the first to third barrier films.

That is, the diffusion of copper from the upper gate electrode can be blocked in all directions.

As a result, the present invention has an extremely excellent effect that copper can be used as the material of the gate electrode of the field effect transistor without deteriorating the characteristics of the transistor. Further, since the upper gate electrode made of copper is formed after forming the source / drain, the upper gate electrode is formed after the high temperature activation heat treatment for forming the source / drain. As a result, it is possible to form the upper gate electrode using copper whose melting point is not so high.

[0075]

Further, in the present invention, a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, a step of forming a sacrificial pattern on the lower gate electrode, a lower step A step of forming a source / drain by introducing an impurity into a predetermined amount area of a silicon substrate using the gate electrode and the sacrificial pattern as a mask, and an insulating material which prevents copper diffusion on both sides of the lower gate electrode and the sacrificial pattern. A step of forming a sidewall, a step of forming a first interlayer insulating film made of silicon oxide on a silicon substrate so as to cover the lower gate electrode and the sacrificial pattern, and a sacrificial pattern by removing the first interlayer insulating film. Exposing the upper surface of the lower gate electrode, selectively removing the sacrificial pattern to form a groove in the upper portion of the lower gate electrode, and conducting to prevent diffusion of copper so that both ends of the upper surface of the lower gate electrode are in contact with the sidewalls. A step of forming a first barrier film having a property, and an upper gate electrode made of copper is formed in the groove through the first barrier film so that a bottom surface of the upper gate electrode is covered with the first barrier film. A step in which both side surfaces are covered with a second barrier film composed of side walls; and a step in which a third barrier film is formed to block the diffusion of copper so as to block the exposed upper surface of the upper gate electrode. At least.

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[0076]
In the present invention, a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and a step of forming an etching stopper layer on the lower gate electrode, A step of forming a sacrificial pattern on the etching stopper layer, a step of forming a source / drain by introducing impurities into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask, a lower gate electrode, an etching stopper A step of forming a sidewall made of an insulating material on both sides of the layer and the sacrificial pattern, and a silicon oxide on the silicon substrate so as to cover the lower gate electrode, the etching stopper layer, and the sacrificial pattern. A step of forming a first interlayer insulating film made of, a step of removing the first interlayer insulating film to expose the upper surface of the sacrificial pattern, and a step of selectively removing the sacrificial pattern to expose the upper surface of the etching stopper layer. And a step of removing the etching stopper layer to form a groove on the upper part of the lower gate electrode, and having a conductivity that adheres to the lower gate electrode and covers the upper surface and prevents the diffusion of copper so that both ends contact the side walls. The step of forming the first barrier film and the step of forming an upper gate electrode made of copper in the groove through the first barrier film and covering the bottom surface of the upper gate electrode with the first barrier film The method further includes at least a step of covering with a second barrier film formed of a side wall, and a step of forming a third barrier film which blocks diffusion of copper so as to block the exposed upper surface of the upper gate electrode. I did it.

[0077]
In the present invention, a step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, and a step of forming an etching stopper layer on the lower gate electrode, A step of forming a sacrificial pattern on the etching stopper layer, a step of forming a source / drain by introducing impurities into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask, a lower gate electrode, an etching stopper A step of forming sidewalls made of an insulating material on both sides of the layer and the sacrificial pattern, and a silicon oxide on the silicon substrate so as to cover the lower gate electrode, the etching stopper layer, and the sacrificial pattern. A step of forming a first interlayer insulating film formed of, a step of selectively removing the first interlayer insulating film to expose the upper surface of the sacrificial pattern to form a groove on the upper part of the lower gate electrode, A step of selectively removing and exposing the upper surface of the etching stopper layer; a step of removing the etching stopper layer; and a step of adhering to the lower gate electrode to cover the upper surface and prevent diffusion of copper so that both ends contact the side walls. A step of forming a first barrier film having a property, and an upper gate electrode made of copper is formed in the groove through the first barrier film so that a bottom surface of the upper gate electrode is covered with the first barrier film. A step in which both side surfaces are covered

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with a second barrier film composed of side walls; and a step in which a third barrier film is formed to block the diffusion of copper so as to block the exposed upper surface of the upper gate electrode. At least.

[0078]

Since it is manufactured as described above, the upper gate electrode is manufactured in a state of being in contact with many parts constituting the field effect transistor via the first to third barrier films.

That is, the diffusion of copper from the upper gate electrode can be blocked in all directions.

As a result, the present invention has an extremely excellent effect that copper can be used as the material of the gate electrode of the field effect transistor without deteriorating the characteristics of the transistor.

Further, since the second barrier film is also used as the side wall, the process can be simplified. Further, since the upper gate electrode made of copper is formed after forming the source / drain, the upper gate electrode is formed after the high temperature activation heat treatment for forming the source / drain. As a result, it is possible to form the upper gate electrode using copper whose melting point is not so high.

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CLAIMS JP2000228523

1.
A lower gate electrode made of silicon formed on a silicon substrate through a gate insulating film, an upper gate electrode made of copper formed on the lower gate electrode, and a channel portion for driving the lower gate electrode are sufficient. A first barrier film having conductivity capable of injecting a current and blocking diffusion of copper formed so as to cover the lower surface of the upper gate electrode, and a lower end of the first barrier film contacts with the upper gate electrode. A second barrier film formed so as to cover both side surfaces of the electrode and for preventing diffusion of copper, and a copper film formed so as to cover an upper surface of the upper gate electrode by contacting an end portion of the second barrier film with the second barrier film. And a source / drain formed on the silicon substrate so as to sandwich the region under the lower gate electrode.

2.
The field effect transistor according to claim 1, further comprising a side wall formed on a side surface of the lower gate electrode and the upper gate electrode, and the second barrier film is formed by a part of the side wall. Transistor.

3.
3. The field effect transistor according to claim 1, wherein the third barrier film is made of an insulating material.

4.

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The field effect transistor according to claim 3, further comprising: an insulating layer formed on the silicon substrate by opening an upper surface of the upper gate electrode, wherein the third barrier film is formed to extend on the insulating layer. Field effect transistor characterized by having been made.

5.
The field effect transistor according to claim 3 or 4, wherein the second and third barrier films are made of a refractory metal or a refractory metal nitride.

6.
The field effect transistor according to any one of claims 1 to 5, wherein the first barrier film is made of an insulating material having a thickness through which a tunnel current flows.

7.
2. The field effect transistor according to claim 1, wherein the first, second, and first barrier films are made of a refractory metal or a refractory metal nitride.

8.
7. The field effect transistor according to claim 2, wherein the insulating material is composed of any one of silicon nitride and boron nitride.

9.
9. The field effect transistor according to claim 1, wherein the first barrier film is a multi-layer film composed of two or more layers.

10.
10. The field effect transistor according to claim 1, wherein the first barrier film is composed of a layer made of a refractory metal, a layer made of a refractory metal silicide, a refractory metal metal, silicon and nitrogen. A field-effect transistor, which is a multi-layered film in which a compound layer or a layer of a refractory metal nitride is combined and laminated in a plurality of layers.

11.
11. The field effect transistor according to claim 10, wherein the lowermost layer of the first

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barrier film is a metal silicide layer or a multilayer film composed of a layer made of a compound of a refractory metal metal and silicon and nitrogen. Characteristic field effect transistor.

12.

12. The field effect transistor according to claim 11, wherein the first barrier film has a lowermost layer composed of a metal silicide layer or a layer composed of a compound of a refractory metal metal and silicon and nitrogen. A field effect transistor, characterized in that it is a multilayer film in which a layer of a refractory metal nitride is arranged in the interior of the field effect transistor.

13.

12. The field effect transistor according to claim 11, wherein the first barrier film has a lowermost layer formed of a metal silicide layer or a layer formed of a compound of a refractory metal metal and silicon and nitrogen. A field effect characterized in that a layer of a refractory metal nitride is disposed on a layer composed of a refractory metal metal, a compound of silicon and nitrogen, and the uppermost layer is a multilayer film composed of a refractory metal. Transistor.

14.

14. The field effect transistor according to claim 1, wherein a refractory metal silicide film is formed in a predetermined region on the surface of the source / drain.

15.

Forming a gate insulating film on a silicon substrate, forming a lower gate electrode made of silicon on the gate insulating film, forming a sacrificial pattern on the lower gate electrode, and the lower gate electrode And a step of forming a source / drain by introducing impurities into a predetermined amount region of the silicon substrate using the sacrificial pattern as a mask, and silicon oxide on the silicon substrate so as to cover the lower gate electrode and the sacrificial pattern. Forming a first interlayer insulating film made of, exposing the upper surface of the sacrificial pattern by removing the first interlayer insulating film, and selectively removing the sacrificial pattern to form the lower gate electrode. A step of exposing a top surface of the first interlayer insulating film to form a groove above the lower gate electrode; and a step of covering the upper surface of the lower gate electrode and the side surface of the groove to prevent diffusion of copper. A step of forming first and second barrier films, and an upper gate electrode made of copper is formed in the groove through the first and second barrier films so that the bottom surface and both side surfaces of the upper gate electrode are At least the step of covering with the first and second barrier films and the step of forming a third barrier film that

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blocks the diffusion of copper so as to block the exposed upper surface of the upper gate electrode. A method for manufacturing a field effect transistor, comprising:

16.

16. The method of manufacturing a field effect transistor according to claim 15, wherein the sacrificial pattern is made of a material that is etched faster than silicon and silicon oxide under a predetermined etching treatment condition. ..

17.

A step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, a step of forming an etching stopper layer on the lower gate electrode, and the etching stopper. Forming a sacrificial pattern on the layer; forming a source / drain by introducing impurities into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask; Forming a first interlayer insulating film made of silicon oxide on the silicon substrate so as to cover the sacrificial pattern, and removing the first interlayer insulating film to expose an upper surface of the sacrificial pattern. Selectively removing the sacrificial pattern to expose the upper surface of the etching stopper layer, and removing the etching stopper layer to expose the upper surface of the lower gate electrode to form a groove above the lower gate electrode. Forming a first and a second barrier film having conductivity to prevent diffusion of copper so as to cover the upper surface of the lower gate electrode and the side surface of the groove, and the first and second barrier films in the groove. Forming an upper gate electrode made of copper through the film so that the bottom surface and both side surfaces of the upper gate electrode are covered with the first and second barrier films; and exposing the upper gate electrode. And a step of forming a third barrier film that blocks the diffusion of copper so as to block the upper surface of the field effect transistor.

18.

A step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, a step of forming an etching stopper layer on the lower gate electrode, and the etching stopper. Forming a sacrificial pattern on the layer; forming a source / drain by introducing impurities into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask; Forming a first interlayer insulating film made of silicon oxide on the silicon substrate so as to cover the sacrificial pattern, and selectively removing the first interlayer insulating film to expose an upper surface of the sacrificial pattern. Forming a groove in the upper part of the lower gate electrode, selectively removing the sacrificial pattern to expose the upper surface of the etching stopper layer, and removing the etching stopper layer to expose the upper surface of the lower gate

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electrode. Exposing, forming first and second barrier films having conductivity to prevent diffusion of copper so as to cover the upper surface of the lower gate electrode and the side surfaces of the groove, and the first and second barrier films in the groove. Forming an upper gate electrode made of copper through a second barrier film so that a bottom surface and both side surfaces of the upper gate electrode are covered with the first and second barrier films; and the upper gate. And a step of forming a third barrier film that blocks the diffusion of copper so as to block the exposed upper surface of the electrode.

19.

The method of manufacturing a field effect transistor according to claim 17 or 18, wherein the sacrificial pattern is made of a material that is etched faster than silicon oxide under a predetermined etching treatment condition. ..

20.

20. The method of manufacturing a field effect transistor according to claim 17, wherein the sacrifice layer, the etching stopper layer and the lower gate electrode are processed by a hard mask. ..

21.

19. The field effect transistor manufacturing method according to claim 17, wherein the sacrifice layer, the etching stopper layer and the lower gate electrode are processed by a hard mask made of silicon oxide or silicon nitride. Production method.

22.

A method of manufacturing a field effect transistor according to any one of claims 15 to 21, wherein a step of forming a refractory metal film after the upper surface of the lower gate electrode is exposed and a groove is formed, A step of forming a nitride film of a refractory metal on the refractory metal film, a step of forming a copper film, the copper in the region other than the groove, the refractory metal film, the nitride film of the refractory metal And a step of removing the upper gate electrode made of copper, the refractory metal film, and the first and second barrier films made of a nitride film of the refractory metal. Method of manufacturing transistor.

23.

22. The method for manufacturing a field effect transistor according to claim 15, wherein a step of forming a first refractory metal film after the upper surface of the lower gate electrode is

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exposed and a groove is formed. A step of forming a refractory metal nitride film on the first refractory metal film, a step of forming a second refractory metal film on the refractory metal nitride film, and copper. A step of forming a film and removing the copper, the first refractory metal film, the refractory metal nitride film, and the second refractory metal film in regions other than the groove, and forming an upper gate made of copper. At least a step of forming an electrode, the first refractory metal film, the nitride film of the refractory metal, and the first and second barrier films composed of the second refractory metal film. Of manufacturing a field effect transistor having the same.

24.

22. The method for manufacturing a field effect transistor according to claim 15, wherein after the upper surface of the lower gate electrode is exposed and a groove is formed, a compound of a refractory metal, silicon and nitrogen is formed. A step of forming a film, a step of forming a nitride film of a refractory metal on the film of the compound of a refractory metal, silicon and nitrogen, a step of forming a copper film to serve as the upper gate electrode, and a step other than the groove Removing the copper, the refractory metal film, and the nitride film of the refractory metal film in the region of, and forming the upper gate electrode made of copper, the refractory metal film, and the nitride film of the refractory metal, And a step of forming a second barrier film.

25.

22. The method for manufacturing a field effect transistor according to claim 15, wherein after the upper surface of the lower gate electrode is exposed and a groove is formed, a compound of a refractory metal, silicon and nitrogen is formed. A step of forming a film, a step of forming a nitride film of a refractory metal on the film of the compound of a refractory metal, silicon and nitrogen, and a film of a refractory metal film on the nitride film of a refractory metal A step of forming copper to be the upper gate electrode, the copper in a region other than the groove, the first refractory metal film, the nitride film of the refractory metal film, the second refractory metal The metal film is removed, and the upper gate electrode made of copper, the first refractory metal film, the refractory metal nitride film, and the first and second barrier films made of the second refractory metal film are removed. And a step of forming the field effect transistor.

26.

The method of manufacturing a field effect transistor according to claim 22 or 23, wherein a step of forming a refractory metal film in contact with the lower gate electrode, and a heat treatment process in which the refractory metal film is in contact with the lower gate electrode. And forming a silicide film of a refractory metal in contact with the lower gate electrode to form a

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silicide film of the refractory metal, and forming the silicide film as a part of the first barrier film.

27.

Forming a gate insulating film on a silicon substrate, forming a lower gate electrode made of silicon on the gate insulating film, forming a sacrificial pattern on the lower gate electrode, and the lower gate electrode And a step of forming a source / drain by introducing an impurity into a predetermined amount region of the silicon substrate using the sacrificial pattern as a mask, and an insulating material for preventing copper diffusion on both side surfaces of the lower gate electrode and the sacrificial pattern. Forming a side wall made of silicon oxide, forming a first interlayer insulating film made of silicon oxide on the silicon substrate so as to cover the lower gate electrode and the sacrificial pattern, and the first interlayer insulating film. To expose the upper surface of the sacrificial pattern, to selectively remove the sacrificial pattern to form a groove above the lower gate electrode, and to cover the upper surface of the lower gate electrode so that both ends are formed on the sidewall. Forming a first barrier film having conductivity to prevent diffusion of copper so as to make contact, and forming an upper gate electrode made of copper in the groove through the first barrier film to form the upper portion A step of making the bottom surface of the gate electrode covered with the first barrier film and both side surfaces covered with the second barrier film composed of the side wall, and closing the exposed upper surface of the upper gate electrode. And a step of forming a third barrier film for preventing the diffusion of copper, the method for manufacturing a field effect transistor.

28.

A step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, a step of forming an etching stopper layer on the lower gate electrode, and the etching stopper. A step of forming a sacrificial pattern on the layer, a step of forming a source / drain by introducing an impurity into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask, the lower gate electrode, A step of forming sidewalls made of an insulating material for preventing diffusion of copper on both side surfaces of the etching stopper layer and the sacrificial pattern, and covering the lower gate electrode, the etching stopper layer, and the sacrificial pattern. Forming a first interlayer insulating film of silicon oxide on the silicon substrate; removing the first interlayer insulating film to expose an upper surface of the sacrificial pattern; and selectively removing the sacrificial pattern. To expose the upper surface of the etching stopper layer, to remove the etching stopper layer to form a groove above the lower gate electrode, and to adhere to the lower gate electrode to cover the upper surface so that both ends are A step of forming a conductive first barrier film that blocks the diffusion of copper so as to come into contact with the side wall, and an upper gate electrode made of copper is formed in the groove through the first barrier film. The step of setting the bottom surface of the upper gate electrode to be covered with the first barrier film and the both side surfaces thereof to be

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covered with the second barrier film composed of the sidewalls; and the exposed upper surface of the upper gate electrode. And a step of forming a third barrier film that blocks the diffusion of copper so as to block the copper film.

29.

A step of forming a gate insulating film on a silicon substrate, a step of forming a lower gate electrode made of silicon on the gate insulating film, a step of forming an etching stopper layer on the lower gate electrode, and the etching stopper. A step of forming a sacrificial pattern on the layer, a step of forming a source / drain by introducing an impurity into a predetermined amount region of the silicon substrate using the lower gate electrode and the sacrificial pattern as a mask, the lower gate electrode, A step of forming sidewalls made of an insulating material for preventing diffusion of copper on both side surfaces of the etching stopper layer and the sacrificial pattern, and covering the lower gate electrode, the etching stopper layer, and the sacrificial pattern. Forming a first interlayer insulating film of silicon oxide on the silicon substrate; selectively removing the first interlayer insulating film to expose an upper surface of the sacrificial pattern to expose the upper portion of the lower gate electrode; A step of forming a groove in the substrate, a step of selectively removing the sacrificial pattern to expose the upper surface of the etching stopper layer, a step of removing the etching stopper layer, and a step of closely contacting the lower gate electrode to cover the upper surface. A step of forming a conductive first barrier film that blocks the diffusion of copper so that both ends are in contact with the side wall; and an upper gate electrode made of copper in the groove via the first barrier film. Forming a state in which the bottom surface of the upper gate electrode is covered with the first barrier film and both side surfaces of the upper gate electrode are covered with the second barrier film composed of the sidewalls; and exposing the upper gate electrode. And a step of forming a third barrier film that blocks the diffusion of copper so as to close the upper surface of the field effect transistor.

30.

30. The method of manufacturing a field effect transistor according to claim 28, wherein the sacrifice layer, the etching stopper layer, and the lower gate electrode are processed by a hard mask.

31.

30. The method of manufacturing a field effect transistor according to claim 28, wherein the sacrifice layer, the etching stopper layer, and the lower gate electrode are processed by a hard mask made of silicon oxide or silicon nitride. Production method.

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32.

32. The method of manufacturing a field effect transistor according to claim 27, wherein a step of forming a film of a refractory metal in contact with the lower gate electrode, and a step of heat treatment to contact the lower gate electrode. And a step of forming a refractory metal silicide film in contact with the lower gate electrode to form a refractory metal silicide film and forming the silicide film as a part of the first barrier film. Manufacturing method.

33.

32. The method for manufacturing a field effect transistor according to claim 27, wherein a step of depositing a refractory metal film in contact with the lower gate electrode and a heat treatment for contacting the lower gate electrode. At least forming a compound film of a refractory metal, silicon and nitrogen in contact with the lower gate electrode by reacting the melting point metal nitride film with silicon to form a part of the first barrier film. A method of manufacturing a field effect transistor, comprising:

34.

A method of manufacturing a field effect transistor according to any one of claims 17 to 19, wherein the sidewall is made of silicon nitride.

35.

22. The method of manufacturing a field effect transistor according to claim 15, wherein the first barrier film is formed by nitriding the upper surface of the lower gate electrode to a thickness at which a tunnel current flows. Method of manufacturing field effect transistor.

36.

The method for manufacturing a field effect transistor according to any one of claims 15 to 35, wherein the first or second barrier film is formed of particles which are incident on the bottom surface of the groove at a vertical angle or an angle close to the vertical angle. A method of manufacturing a field effect transistor, characterized in that the film is formed by an increased number of methods.

37.

37. The method of manufacturing a field effect transistor according to claim 15, wherein refractory metal silicide is formed in a predetermined region of the source / drain before forming the upper gate electrode. And a method of manufacturing a field effect transistor.

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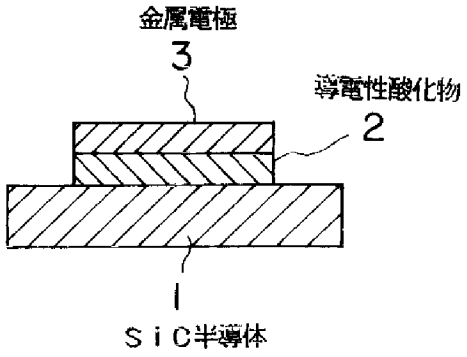
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(71)出願人　000001889
三洋電機株式会社
大阪府守口市京阪本通２丁目５番５号
(72)発明者　鈴木　誠二
大阪府守口市京阪本通２丁目５番５号　三洋電機株式会社内
(74)代理人　100076794
弁理士　安富　耕二　（外１名）

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(54)【発明の名称】　電極、ＳｉＣの電極及びＳｉＣデバイス

(57)【要約】
【課題】　ＳｉＣの電極において、高温アロイ処理、高キャリア濃度のイオン注入を必要とすることがなく、オーミック接触をとることができる電極構造を得る。
【解決手段】　ＳｉＣ１にＮｂドープチタン酸ストロンチウムなどの導電性酸化物２を介してＴｉ，Ａｌなどの金属電極３を設けてＳｉＣの電極を構成する。



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【特許請求の範囲】
【請求項１】　所定の導電型を有する半導体と、
該半導体上に形成された、該導電型と同じ導電型の導電性酸化物からなる電極と、からなる電極。
【請求項２】　請求項１記載の電極において、
前記半導体と、前記導電性酸化物とのバンドギャップが略等しい電極。
【請求項３】　所定の導電型のＳｉＣと、
該ＳｉＣに接触して形成された該導電型と同じ導電型の導電性酸化物からなる電極を備えるＳｉＣの電極。
【請求項４】　請求項３記載のＳｉＣの電極において、
前記導電性酸化物からなる電極は、
該酸化物からなる膜と、
該膜上に形成されてなる金属体とを有するＳｉＣの電極。
【請求項５】　請求項１乃至請求項４のいずれかに記載のＳｉＣの電極において、
前記導電性酸化物は、チタン酸ランタン，酸化レニウム，銅アルミ酸化物，銅ガリウム酸化物のいずれかであるＳｉＣの電極。
【請求項６】　請求項１乃至請求項４のいずれかに記載のＳｉＣの電極において、
前記導電性酸化物は、チタン酸ストロンチウム，酸化インジウムのいずれかであるＳｉＣの電極。
【請求項７】　請求項６記載のＳｉＣの電極において、
前記チタン酸ストロンチウムは、不純物として、Ｎｂ，Ｔａ，Ｌａのいずれかを含み、前記酸化インジウムについては、不純物としてＳｎを含むＳｉＣの電極。
【請求項８】　半導体としてＳｉＣを用いてなるＳｉＣデバイスにおいて、
請求項１乃至請求項７のいずれかに記載のＳｉＣの電極を用いたことを特徴とするＳｉＣデバイス。
【請求項９】　ＳｉＣ上に設けられたソース、及びドレインと、前記ＳｉＣ上の前記ソース、及びドレインの間に設けられたゲート電極と、前記ソース及びドレイン上に設けられた導電性酸化物からなる電極を備えてなるＳｉＣデバイス。
【請求項１０】　ｎ型ＳｉＣと、ｐ型ＳｉＣと、前記ｎ型ＳｉＣを挟んで設けられた第１、第２のｎ型導電性酸化物と、前記ｐ型ＳｉＣを挟んで設けられた第３、第４のｐ型導電性酸化物と、前記第２の導電性酸化物と前記第４の導電性酸化物を接続する第１金属電極と、前記第１の導電性酸化物に対して設けられる第２金属電極と、前記第３の導電性酸化物に対して設けられる第３金属電極とを備えてなるＳｉＣデバイス。
【請求項１１】　請求項１０記載のＳｉＣデバイスにおいて、
前記第１の導電性酸化物と前記第２金属電極との間、及び前記第２の導電性酸化物と前記第１金属電極との間、並びに前記第３の導電性酸化物と前記第３金属電極との間、及び前記第４の導電性酸化物と前記第１金属電極との間に、それぞれ各導電性酸化物とオーミック特性をもつ所定の金属を介在させてなるＳｉＣデバイス。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、ＳｉＣ（炭化珪素）の電極及びそれを用いたＳｉＣデバイスに関し、特に、ＳｉＣとオーミック接触を行うことができる電極、ＳｉＣの電極及びＳｉＣデバイスに関するものである。
【０００２】
【従来の技術】ＳｉＣ半導体は、現在一般的に使用されている他の半導体（例えばＳｉ）に比べ、融点、エネルギーギャップ、絶縁破壊電界、熱伝導率、飽和速度等の物性値が大きく、従って、熱的、化学的、機械的に安定であり、耐放射線特性にも優れている。
【０００３】ＳｉＣのオーミック性電極の形成については、従来より、例えば、ｐ型ＳｉＣについては、Ａｌ，Ａｌ／Ｔｉ積層膜，Ａｌ－Ｔｉ合金などを炭化珪素表面に蒸着した後、９００℃から１１００℃で高温アロイ処理を行うようにしたものが知られている。またｎ型ＳｉＣについては、Ｎｉ，Ｎｉ／Ｔｉ／Ｗ積層膜などをＳｉＣ表面に蒸着した後、高温アロイ処理を施すようにしたものが知られている。
【０００４】また、他の例としては、前記高温アロイ処理に加え、電極が接触する領域の炭化珪素に対して、不純物濃度を高くしておく（$10^{19}cm^{-3}$程度）ことによってより抵抗の低いオーミック接触を行うなどの方法が知られている。
【０００５】
【発明が解決しようとする課題】しかしながら、高温アロイ処理を必要とする場合は、ＳｉＣデバイスの製造において、耐熱性のある材料しか用いることができず、デバイス製造プロセスにおいて、材料に関する大きな制約を受けることとなる。また、高温アロイ処理中に電極材料の凝集が生じ、均一なオーミック性の電極を作成することが困難となる。
【０００６】一方、炭化珪素に対して不純物濃度の高い領域を形成するためには、イオン注入法が用いられるが、イオン注入により炭化珪素の結晶性を劣化させる。更に、ＳｉＣに表面処理を行う場合は、その処理が半導体デバイスの製造プロセスの効率化を妨げる。
【０００７】そこで、本発明は、高温アロイ処理、高キャリアのイオン注入を必要とすることなく、オーミック接触を得ることができる電極とこれを用いたＳｉＣデバイスを提供することを目的としている。
【０００８】
【課題を解決するための手段】上述した課題を解決するため、本発明に係る電極は、所定の導電型を有する半導体と、該半導体上に形成された、該導電型と同じ導電型の導電性酸化物からなる電極とからなるものである。ま

た、本発明に係る電極は、請求項１記載の電極において、半導体と、導電性酸化物とのバンドギャップが略等しいものである。

【０００９】又、本発明に係るＳｉＣの電極は、所定の導電型のＳｉＣと、該ＳｉＣに接触して形成された該導電型と同じ導電型の導電性酸化物からなる電極を備えたものである。

【００１０】図２に示されるように、例えば、$SrTiO_3$ に所定量のＮｂをドープしてなる$SrTiO_3$ のような導電性酸化物のバンド構造は、ＳｉＣと同様のワイドギャップ材料であるので、これら材料の接合では、連続的なバンドのつながりが想定され、金属と半導体との接触で生じるようなショットキー障壁は生じない。オーミック接触となる条件としては、図２中に示したΔＥの大きさで決まる。ΔＥは、ＳｉＣのフェルミ準位（キャリア濃度）Ｅｆの位置だけで定まる。

【００１１】ここで、例えば、ＳｉＣキャリア濃度$10^{16}cm^{-3}$に対して、Ｅｆは伝導帯の下端からエネルギー的に１３０ｍＶ下方に位置する。このとき、ΔＥ＝１３０ｍＶ（$10^{18}cm^{-3}$であれば僅かにΔＥ＝２０ｍＶ）となり、これはオーミック接触として扱ってよい量である。したがって、ＳｉＣが$10^{16}cm^{-3}$以上のドープ量であれば、オーミック接触が可能となり、本発明においては、ＳｉＣに対して高ドープする必要もなければ、高温アロイ処理も不要となる。

【００１２】また、本発明ＳｉＣの電極において、導電性酸化物からなる電極は、該酸化物からなる膜と、該膜上に形成されてなる金属体とを有するものである。

【００１３】ここで、酸化物からなる膜は、ＳｉＣとオーミック特性を有し、金属体は酸化物からなる膜とオーミック特性を有する。金属体は金属膜又は金属配線であってよい。電子デバイスにおいては、導電性酸化物自体は金などの配線接続用金属に比べて抵抗が大きい。従って、デバイスの導電性酸化物からなる電極に金などのリードを接続することが考えられる。導電性酸化物は、所定の金属、例えば、ＴｉやＡｌなどの金属と低抵抗な接続状態が得られる。従って、導電性酸化物に所定の金属を例えば配線接続用金属（或いは、ＴｉやＡｌなどの所定金属を介して更にリード用接続金属を設けてなる配線接続用金属）として設けた電極を構成すれば、他の回路（デバイス）への接続をそのまま低抵抗で行うことができる。なお、この場合、導電性酸化物は、ＳｉＣと低抵抗なオーミック接触がとれ、且つ金属（例えば配線接続用金属）と低抵抗なオーミック接触がとれれば良い最小限の間隔（または膜厚）、例えば５００Åに渡って設けられることが望ましい。

【００１４】なお、本発明に係るＳｉＣの電極において、前記導電性酸化物は、正規組成の酸化物であって、略１Ωｃｍ以下、例えば１～10^{-7}Ωｃｍの範囲の比抵抗を有する酸化物とすることができる。

【００１５】導電性酸化物には、正規組成につくったときに、最も伝導度が高くなるものがあり、金属的特性を示す物がある。このような酸化物によれば、不純物を注入することなく、電極構造として用いることが可能となる。なお、このような導電性酸化物には、実施の形態に説明しているものの他に、酸化チタン（ＴｉＯ），ランタンニッケル酸化物（$LaNiO_3$），ランタン銅酸化物（$LaCuO_3$），銅ルチニウム酸化物（$CuRuO_3$），ストロンチウムイリジウム酸化物（$SrIrO_3$），ストロンチウムクロム酸化物（$SrCrO_3$），リチウムチタン酸化物（$LiTi_2O_4$），酸化ルチニウム（RuO_2），酸化オスミウム（OsO_2），酸化イリジウム（IrO_2），酸化モリブデン（MoO_2），酸化タングステン（WO_2），酸化レニウム（ReO_2），酸化ロジウム（RhO_2），β酸化白金（βPtO_2），チタン酸ランタン（$LaTiO_3$），酸化ルテニウム（ReO_3），銅アルミ酸化物（$CuAlO_2$），銅ガリウム酸化物（$CuGaO_2$）のいずれかの酸化物としたものである。

【００１６】これら、酸化物は実施の形態にも説明されているように比抵抗が小さく、ＳｉＣ半導体と良好なオーミック接触をとることができる。なお、これら導電性酸化物のうち、ＳｉＣ半導体がｎ型の場合は、$LaTiO_3$ 若しくはReO_3 が用いられる。$LaTiO_3$ の比抵抗は10^{-5}Ωｃｍであり、ReO_3 の比抵抗は10^{-7}Ωｃｍである。一方、ＳｉＣ半導体がｐ型の場合は、$CuAlO_2$ 若しくは$CuGaO_2$ が用いられる。$CuAlO_2$ 及び$CuGaO_2$ の比抵抗は共に略１Ωｃｍである。

【００１７】また、本発明に係るＳｉＣの電極において、前記導電性酸化物は、正規組成の酸化物に不純物がドープされ、１Ωｃｍ以下、例えば１～10^{-7}Ωｃｍの範囲の比抵抗を有する酸化物とすることができる。

【００１８】導電性酸化物には、正規組成からずれることによって、酸素欠陥又は格子間イオンが生じて導電性を示すものがある。従って、導電性酸化物は、正規組成の絶縁性酸化物に、所定の不純物をドープすることによっても得られ、このような導電性酸化物を用いることによっても、ＳｉＣとのオーミック接触をとることができる。なお、このような導電性酸化物には、実施の形態に説明しているものの他に、酸化スズ（SnO_2），酸化インジウム（In_2O_3），酸化タリウム（Tl_2O_3），フッ素酸タリウム（ＴｌＯＦ）等がある。

【００１９】また、本発明に係るＳｉＣの電極において、前記正規組成の酸化物に不純物をドープすることにより、電極として用いられる酸化物は、$SrTiO_3$，In_2O_3 のいずれかの酸化物である。

【００２０】このような、酸化物は、所定の不純物のドープにより顕著な導電性が得られることが見出され、このような導電性酸化物を用いることによっても、ＳｉＣ

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とのオーミック接触をとることができる電極を得ることができる。

【0021】また、本発明に係るSiCの電極において、前記$SrTiO_3$は、不純物として、Nb，Ta，Laのいずれかを含み、前記In_2O_3については、不純物としてSnを含むものである。

【0022】実施の形態においても説明しているように、$SrTiO_3$には、Nb，Ta，Laのいずれかがドープされることにより、またIn_2O_3には、Snがドープされることにより、これら酸化物に導電性が生じ、SiCとのオーミック接触をとることができる。従って、このような導電性酸化物を用いることによりオーミック接触を有する電極を得ることができる。

【0023】また、本発明に係るSiCデバイスは、例えば図3乃至図8に示される電子デバイスのように、SiCの電極に請求項1乃至請求項7のいずれかに記載の電極を用いたものである。

【0024】このようなSiCデバイスは、高温アロイ処理やハイドープまたは特殊表面処理を施すことなくその電極を得ることができるので、製造プロセスが簡略化され、また、耐高温材料等の制約も緩和される。更に、半導体にSiCを用いているので、高温、放射線等の過酷な環境下にあっても、安定且つ信頼性ある動作が可能となる。

【0025】また、本発明に係るSiCデバイスは、例えば、MOSFETの電極において、高温アロイ処理やハイドープまたは特殊表面処理を施すことなくその電極（ソース、ドレイン電極）を得ることができるので、製造プロセスが簡略化され、また、耐高温材料等の制約も緩和される。更に、半導体がSiCにより構成されるので、高温、放射線等の過酷な環境下にあっても、安定且つ信頼性ある動作が可能となる。なお、ソース、ドレイン等が設けられるSiCは、SiC基板でもよく、SiC基板上にSiC膜が形成されたものでもよい。又、実施の形態においては、導電性酸化物上に配線接続用金属を備えている。

【0026】また、本発明に係るSiCデバイスは、例えば、熱電素子の電極において、高温アロイ処理やハイドープまたは特殊表面処理を施すことなくその電極を得ることができるので、製造プロセスが簡略化され、また、耐高温材料等の制約も緩和される。更に、半導体がSiCにより構成されるので、高温、放射線等の過酷な環境下にあっても、安定且つ信頼性ある動作が可能となる。

【0027】また、熱電素子の金属電極には熱伝導率の良さから一般に銅電極が使用される。そこで、このような銅と導電性酸化物との間に所定の金属（例えばTi，Al）を介在させることにより、SiCと銅電極間の低抵抗な電気接続を得ることができる。この所定の金属として、Al，Ti等が適用されている。

【0028】

【発明の実施の形態】以下、本発明の実施の形態を図面を用いて説明する。

実施の形態1．図1は実施の形態1を示す電極の断面側面図である。この電極は、SiC半導体1上に、導電性酸化物2を接触させて、更にその導電性酸化物2の上に金属電極3を接触させてなり、SiC半導体1と導電性酸化物2とがオーミック接触し、また導電性酸化物2と金属電極3とがオーミック接触する。

【0029】ここで、SiC半導体1がn型の場合は、導電性酸化物2には、正規組成の導電性酸化物として、$LaTiO_3$若しくはReO_3が用いられる。$LaTiO_3$の比抵抗は$10^{-5}\Omega cm$であり、ReO_3の比抵抗は$10^{-7}\Omega cm$である。

【0030】導電性酸化物2は、正規組成の絶縁性酸化物に、所定の不純物をドープすることによっても得られ、この場合は、例えば、Nb，Ta，Laのいずれかがドープされた$SrTiO_3$、或いは、SnがドープされたIn_2O_3が用いられる。

【0031】ここで、$SrTiO_3$への上記ドーパントのドープ量は、0．1～5atm%とされ、このときの比抵抗は$1\sim10^{-4}\Omega cm$である。また、Snへの上記ドーパントのドープ量は、5～10wt%とされ、このときの比抵抗は$10^{-4}\sim10^{-5}\Omega cm$である。

【0032】一方、SiC半導体1がp型の場合は、導電性酸化物2には、正規組成の導電性酸化物として、$CuAlO_2$若しくは$CuGaO_2$が用いられる。$CuAlO_2$及び$CuGaO_2$の比抵抗は共に略$1\Omega cm$である。

【0033】なお、p型のSiC半導体において、正規組成の絶縁性酸化物にドーパントをドープすることにより、導電性となるような酸化物は、現在のところ見出されていないが、このような酸化物が見出された場合も、ドープされてなるその導電性酸化物は本発明の導電性酸化物に含まれる。

【0034】絶縁性酸化物にドーパントをドープすることによって得られる導電性酸化物の製法は、スパッタ、レーザアブレーション、反応性共蒸着がある。例えば、スパッタにより$SrTiO_3$にNbをドープしてなる$SrTiO_3$（以下、Nb－$SrTiO_3$と記す）の製法は、ターゲットをNb－$SrTiO_3$、スパッタガスを$Ar+O_2$（10～50%），全圧0．01～1torrとして、500～700℃の成膜温度下において行われる。また、レーザアブレーションによるNb－$SrTiO_3$の製法は、ターゲットをNb－$SrTiO_3$、雰囲気ガスをO_2（0．01～1torr）として、500～700℃の成膜温度下において行われる。更に、反応性共蒸着によるNb－$SrTiO_3$の製法は、蒸発源をNb－$SrTiO_3$、雰囲気ガスをO_2（$10^{-6}\sim10^{-5}$torr）として、500～700℃の成膜温度下

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において行われる。

【００３５】図１において、導電性酸化物２に接触する金属材料としては、導電性酸化物と低抵抗のオーミック接触が得られる、ＴｉやＡｌが用いられる。なお、ｎ型のＳｉＣ半導体は、例えばＮを含む雰囲気におけるＣＶＤ法により成膜状のものが得られ、また昇華法によりバルク状のものが得られる。またｐ型のＳｉＣ半導体はＡｌ，Ｂのいずれかを含む雰囲気におけるＣＶＤ法により膜状のものが得られ、また昇華法によりバルク状のものが得られる。ＳｉＣのキャリア濃度は10^{16}ｃｍ$^{-3}$～10^{18}ｃｍ$^{-3}$とされる。

【００３６】図２は、上述した電極により得られる、Ｎｂ－ＳｒＴｉO_3 とｎ型ＳｉＣ半導体とのバンド構造を示している。図２に示されるように、導電性酸化物のバンド構造は、縮退半導体（フェルミ準位が伝導帯の中にある）構造をとる。縮退幅はキャリア濃度で決まり、また、酸化物の比抵抗値はキャリア濃度で決まるが、電極抵抗を小さくするためには、できるだけ高キャリア濃度であることが望まれる。

【００３７】導電性酸化物のバンド構造は、ＳｉＣと同様のワイドギャップ材料であるので、これら材料の接合

n-SiC（ドープ量10^{16}ｃｍ$^{-3}$以上）
導電性酸化物
Nb,Ta,Laのいずれかドープ$SrTiO_3$
SnドープIn_2O_3 (ITO)
$LaTiO_3$
ReO_3

【００４１】

p-SiC（ドープ量10^{16}ｃｍ$^{-3}$以上）
導電性酸化物
$CuAlO_2$
$CuGaO_2$

【００４２】実施の形態２．実施の形態２は、実施の形態１の電極を成膜ＳｉＣの薄膜電極として用いたＳｉＣデバイスの一例を示す。図３はｎチャネルＭＯＳＦＥＴ及びその製造方法を示す図である。このＭＯＳＦＥＴは、図３（ｈ）に示されるように、ｐ型ＳｉＣ基板１Ａ上に設けられたソース領域１Ｂ、及びドレイン領域１Ｃと、ＳｉＣ基板１上のソース、及びドレイン領域１Ｂ，１Ｃの間に設けられたゲート酸化膜５と、ソース及びドレイン領域１Ｂ、１Ｃ上に設けられた導電性酸化物膜２Ａ，２Ｂと、導電性酸化物膜２Ａ，２Ｂの上に設けられた配線接続用金属層３Ａ，３Ｂと、ゲート酸化膜５の上に設けられたゲート電極６とを備えてなる。

【００４３】ここで、導電性酸化物膜２Ａ，２Ｂと、これらの上に設けられた配線接続用金属層３Ａ、３Ｂは、それぞれソース及びドレイン電極を構成している。

【００４４】以下、このＭＯＳＦＥＴの製造方法を図３に従って説明する。図３（ａ）～（ｃ）はソースドレイン領域の形成工程を示すもので、まず、（ａ）に示されるように、ｐ型ＳｉＣ基板１Ａ上にイオン注入（ドープ）用マスク７を形成する。ここで、ｐ型ＳｉＣ基板１Ａとして、不純物としてＡｌを1×10^{15}－1×10^{18}ｃｍ$^{-3}$ドープしたＳｉＣ単結晶基板を使用した。マスク７は、ｐ型ＳｉＣ基板１Ａ上に１μｍの厚みのSiO_2膜をＣＶＤ法などで形成した後、フォトリソ工程、エッチング工程を経て得られるSiO_2 蒸着法により形成される。

では、連続的なバンドのつながりが想定され、金属と半導体との接触で生じるようなショットキー障壁は生じない。オーミック接触となる条件としては、図２中に示したΔＥの大きさで決まる。例えば、ΔＥ＝１ｅＶもある場合には、オーミック接触とは言えない。また、ΔＥは、ＳｉＣのフェルミ準位（キャリア濃度）Ｅｆの位置だけで定まる。

【００３８】ここで、例えば、ＳｉＣキャリア濃度10^{16}ｃｍ$^{-3}$に対して、Ｅｆは伝導帯の下端からエネルギー的に１３０ｍＶ下方に位置する。このとき、ΔＥ＝１３０ｍＶ（10^{18}ｃｍ$^{-3}$であれば僅かにΔＥ＝２０ｍＶ）となり、これはオーミック接触として扱ってよい量である。したがって、ＳｉＣが10^{16}ｃｍ$^{-3}$以上のドープ量であれば、オーミック接触が可能となり、本発明においては、ＳｉＣに対して高ドープする必要もなければ、高温アロイ処理も不要となる。

【００３９】なお、上述したｎ－ＳｉＣ及びｐ－ＳｉＣに対する導電性酸化物の種類、不純物、及びそのドープ量、それにより得られる比抵抗を以下に纏めておく。

【００４０】

【表１】

	ドープ量（比抵抗）
	0.01-1atm %(1－10^{-4}Ωcm)
	0.01-1wt%(10^{-4}－10^{-5}Ωcm)
	ドープなし (10^{-5}Ωｃｍ)
	ドープなし (10^{-7}Ωｃｍ)

【表２】

	ドープ量（比抵抗）
ドープなし	１Ωｃｍ
ドープなし	１Ωｃｍ

【００４５】次に、図３（ｂ）に示されるように、ｐ型ＳｉＣ基板１Ａ内にｎ型不純物領域１Ｂ、１Ｃをイオン注入法により形成する。ここで、注入不純物はＮまたはＰ、注入温度は５００～１０００℃、注入量は1×10^{18}-1×10^{21}ｃｍ$^{-3}$である。その後、エッチングによりマスク７を除去し、さらにｎ型不純物領域１Ｂ、１Ｃに注入された不純物がキャリアとして機能するように活性化させるためのアニール処理を、８００～１５００℃、真空または不活性ガス中において行い、図３（ｃ）に示されるように、ソース領域１Ｂおよびドレイン領域１Ｃ

を得る。

【0046】次に、図3（d）～（e）に示されるゲート酸化膜の形成を行う。まず、（d）において、p型SiC基板1Aを酸素雰囲気中、1200℃において酸化処理をして表面に膜厚500ÅのSiO$_2$膜5Aを形成する。そして、（e）のように、フォトリソ及びエッチング工程を経てソース領域1Bおよびドレイン領域1C上の酸化膜5Aを除去して、ゲート酸化膜5を得る。

【0047】次に、図3（f）～（h）に示されるソース、ドレイン、ゲート電極形成を行う。まず、p型SiC基板1A上に、厚み500Åの導電性酸化物をスパッタ法などで形成し、フォトリソ及びエッチング工程を経て、図3（f）に示されるように、ソース、ドレイン領域1B、1C上にコンタクト電極としての導電性酸化物2A、2Bを形成する。ここで、導電性酸化物としては、Nbを1atm%ドープしたSrTiO$_3$を使用した。

【0048】次に、p型SiC基板1A上に、厚み2000Åの配線層への接触層としてのAlまたはTiを真空蒸着法などで形成し、フォトリソ及びエッチング工程を経て図3（g）に示されるように、導電性酸化物膜2A、2B上に、配線接続用金属層3A、3Bを形成する。

【0049】最後に、p型SiC基板1A上に、厚み2000Åの多結晶Siをスパッタ法などで形成し、フォトリソ及びエッチング工程を経て、図3（h）に示されるように前記多結晶Siがゲート酸化膜5上にのみ存在するように、ゲート電極6を形成する。

【0050】このように、実施の形態2によるSiCデバイスは、SiCにオーミック接触する導電性酸化物膜（コンタクト電極）を介して配線層である金属電極層を接続するようにしたので、高温アロイ処理が不要となり、又、SiCに高キャリア層を設ける必要もなくなる。

【0051】実施の形態3．実施の形態3は、実施の形態1の電極をSiCバルクの電極として用いた電子デバイスの一例を示す。図4はSiCバルクを用いてなる熱電素子及びその製造方法を示す図である。この熱電素子は、図4（c）に示すように、n型SiC1Dを挟んで設けられたn型第1、第2導電性酸化物（2D-1，2D-2）と、p型SiC1Eを挟んで設けられたp型第3、第4導電性酸化物（2E-1，2E-2）と、n型導電性酸化物2D-2とp型導電性酸化物2E-2と金属膜3Dを介して接続する第1金属電極8と、n型導電性酸化物2D-1に金属膜3Eを介して接続された第2金属電極10と、p型導電性酸化物2E-1に金属膜3Eを介して接続された第3金属電極9とを備えてなる。

【0052】以下、この熱電素子の製造方法を図4に従って説明する。まず、（a）に示されるように、昇華法によって得られたp型SiC1Eの両側にp型導電性酸化物であるCuAlO$_2$（2E-1、2E-2）をスパッタ法などにより成膜する（厚み500Å）。また、n型SiC1Dの両側にn型導電性酸化物であるNbを1atm%ドープしたチタン酸ストロンチウム（2D-1，2D-2）をスパッタ法などにより成膜する（厚み500Å）。

【0053】次に、（b）に示されるように、それぞれ成膜された導電性酸化物（2D-1，2D-2，2E-1、2E-2）の膜上に接触金属膜3D、3Eとして、Al膜またはTi膜を真空蒸着法などで形成する（厚み10μm）。そして、（c）に示されるように、真空蒸着された接触金属膜3D，3D上に第1金属電極（銅電極）8をハンダ付けして掛け渡すとともに、接触金属膜3E，3E上に第2，第3金属電極（銅電極）9，10をそれぞれハンダ付けして取り付ける。

【0054】こうして製造された、熱電素子は金属電極（例えば銅電極）8～10とSiC半導体とのオーミック接触が簡単にとれ、又、接触金属層によりその抵抗を小さくできる。なお、金属電極に銅を用いるのは、銅は熱伝導性に優れ、熱電素子の電力／熱交換効率を高めることができるからである。

【0055】実施の形態4．図5はSiCを用いた電子デバイスの他の例としてnチャネル接合型電界効果トランジスタ（JFET）を示す断面図である。このJFETは、n型SiC1Fに対して対向する二つの面それぞれにp型領域1G，1Gを有し、これらの領域それぞれにp型導電性酸化物膜2F，2Fを介してゲート用のAl，Tiからなる配線接続用金属膜3F，3Fが設けられている。又、n型SiC1Fの他の対向する面上には、それぞれn型導電性酸化物膜2G、2Hを介してソース、及びドレイン用のAl，Tiからなる配線接続用金属膜3G，3Hが設けられている。

【0056】実施の形態5．図6はSiCを用いた電子デバイスの他の例としてnチャネル接合型電界効果トランジスタ（MESFET）を示す断面図である。このMESFETは、n型SiC1H上に例えばPt膜からなるショットキーゲート電極3Iが設けられ、その両側にn型導電性酸化物膜2I，2Jを介してそれぞれAl，Tiからなる配線接続用金属膜3J、3Kが設けられ、それぞれソース、ドレイン電極とされている。

【0057】実施の形態6．図7はSiCを用いた電子デバイスの他の例としてサイリスタを示す断面図である。このサイリスタは、図示左端より、SiCのp層1I、n層1J、p層1K、n層1Lが交互に設けられ、左端のp層1Iにp型導電性酸化物膜2Kを介してAl，Tiからなる配線接続用金属膜3Lが設けられてアノード電極が形成されている。また、右端のn層1Lにn型導電性酸化物膜2Lを介してAl，Tiからなる配線接続用金属膜3Mが設けられてカソード電極が形成されている。さらに、右端のn層1Lに隣接されるp層1

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Kにp型導電性酸化物膜２Mを介してＡｌ，Ｔｉからなる配線接続用金属膜３Ｎが設けられてゲート電極が形成されている。

【００５８】実施の形態7．図8はＳｉＣを用いた絶縁ゲートバイポーラトランジスタ（ＩＧＢＴ）であり、基板の上半分にｎ型ＳｉＣ１Mが形成され、下半分にｐ型ＳｉＣ１Ｎが形成されている。ｐ型ＳｉＣ１Ｎの下面にはｐ型導電性酸化物膜２Ｎを介してＡｌ，Ｔｉからなる配線接続用金属膜３Ｓが設けられてコレクタ電極が形成されている。ｎ型ＳｉＣ１Mの上面両側には、ｐ層１Ｐ，１Ｑが設けられ、それらの上にｎ型導電性酸化物膜２Ｑ，２Ｐを介して、Ａｌ，Ｔｉからなる配線接続用金属膜３Ｐ、３Ｑが設けられた電極が構成されている。これら電極のうち、左側の電極はエミッタ電極として使用され、右側の電極がゲート電圧制御端子として使用される。

【００５９】又、ｎ型ＳｉＣ１Mの上面にはゲート酸化膜５Ｂを介してＡｌ，Ｔｉからなる配線接続用金属膜３Ｒが設けられている。又、ｎ型導電性酸化物膜２Ｑ、２Ｐの基板側周辺部、及びゲート電極とエミッタ電極及びゲート電圧制御端子との間には、ｐ層１Ｐ，１Ｑの中にそれぞれ、ｎ層１Ｒ，１Ｓ及び１Ｔ，１Ｕが設けられている。

【００６０】以上のような電子デバイスでは、ＳｉＣを用いているので、絶縁破壊に優れ、大電力使用が可能であると共に、高温、放射線などの過酷な条件下においても、高い信頼性と安定性を維持し得る。

【００６１】

【発明の効果】以上に説明したように、本発明は、所定の導電型を有する半導体と、該半導体上に形成された該導電型と同じ導電型の導電性酸化物からなる電極とからなるので、高温アロイ処理、高キャリアのイオン注入を必要とすることがない電極、ＳｉＣの電極及びＳｉＣデバイスを得ることができるという効果を奏する。

【図面の簡単な説明】

【図１】本発明の実施の形態１における電極構造を示す断面図である。

【図２】ＳｉＣと導電性酸化物を接触させたときのバンド構造を示す図である。

【図３】実施の形態２を示す断面図である。

【図４】実施の形態３を示す断面図である。

【図５】実施の形態４を示す断面図である。

【図６】実施の形態５を示す断面図である。

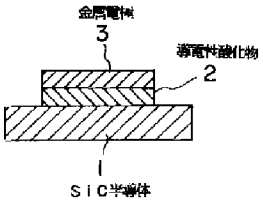
【図７】実施の形態６を示す断面図である。

【図８】実施の形態７を示す断面図である。

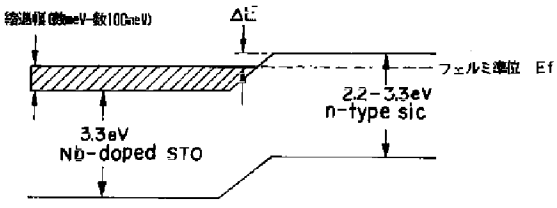
【符号の説明】

１　ＳｉＣ（炭化珪素）
１Ｂ　ソース領域
１Ｃ　ドレイン領域
１Ｄ　ｎ型ＳｉＣ
１Ｅ　ｐ型ＳｉＣ
２　導電性酸化物
２Ａ，２Ｂ　導電性酸化物膜
２Ｄ　Ｎｂドープチタン酸ストロンチウム
２Ｅ　$CuAlO_2$
３　金属電極
３Ａ，３Ｂ　配線接続用金属層
３Ｄ，３Ｅ　接触金属膜
５　ゲート酸化膜
８　第１金属電極（銅電極）
９，１０　第２，第３金属電極（銅電極）

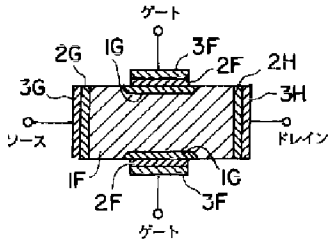
【図１】



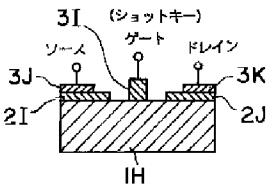
【図２】



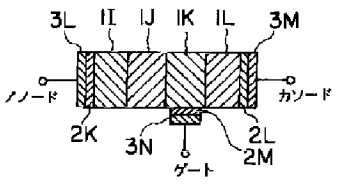
【図５】



【図６】

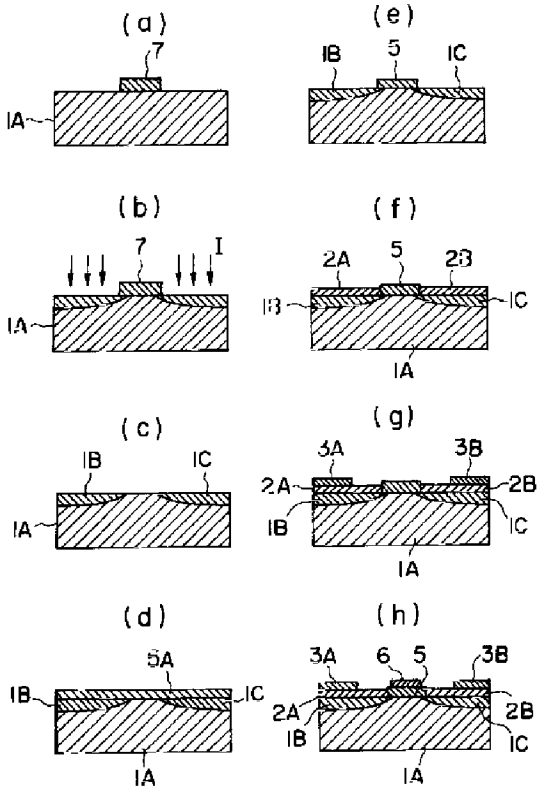


【図７】

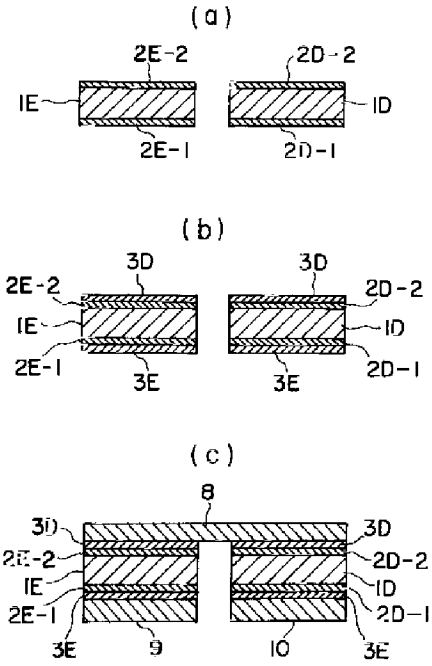


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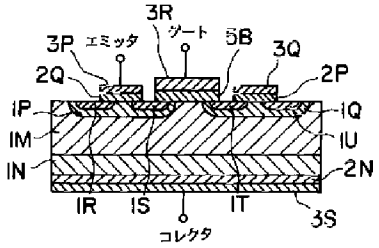
【図3】


(a)
7
1A
(b)
7
I
1A
(c)
1B
1C
1A
(d)
5A
1B
1C
1A
(e)
1B
5
1C
(f)
2A
5
2B
1B
1C
1A
(g)
3A
3B
2A
2B
1B
1C
1A
(h)
3A
6
5
3B
2A
2B
1B
1C
1A

【図4】


(a)
2E-2
2D-2
1E
1D
2E-1
2D-1
(b)
3D
3D
2E-2
2D-2
1E
1D
2E-1
2D-1
3E
3E
(c)
8
3D
3D
2E-2
2D-2
1E
1D
2E-1
2D-1
3E
9
10
3E

【図8】


3R
3P
エミッタ
ゲート
5B
3Q
2Q
2P
1P
1Q
1M
1U
1N
2N
1R
1S
1T
3S
コレクタ

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JP2000101064A ELECTRODE, SiC ELECTRODE, AND SiC DEVICE

Applicants: SANYO ELECTRIC CO

Inventors: SUZUKI SEIJI

Classifications:
IPC ***H01L21/28; H01L29/43;*** (IPC1-7): H01L29/43;

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ELECTRODE, SiC ELECTRODE, AND SiC DEVICE

Abstract

PROBLEM TO BE SOLVED: To realize an ohmic structure, without using a high-temperature alloy treatment and a high carrier ion implantation process by a method, wherein the ohmic contact structure is composed of a specified conductivity-type semiconductor and a conductive oxide electrode, which is of the same conductivity type as with the semiconductor formed on the semiconductor. SOLUTION: An electrode comes into ohmic contact with an SiC semiconductor 1 in a manner in which a conductive oxide 2 is brought into contact with the SiC semiconductor, and a metal electrode 3 is brought into contact with the conductive oxide 2, where the conductive oxide 2 comes into ohmic contact with the SiC semiconductor 1, and the metal electrode 3, coming into contact with the conductive oxide 2. Ti or Al that comes into ohmic contact with a conductive oxide an low in contact resistance, is used as a metal material that comes into contact with the conductive oxide 2. Furthermore, an N-type SiC semiconductor is formed film-like through a CVD method carried out in an N atmosphere, and a P-type SiC semiconductor is formed a film-like through a CVD method in an atmosphere that contains either Al or B.

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DESCRIPTION JP2000101064

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a SiC (silicon carbide) electrode and a SiC device using the same, and more particularly to an electrode capable of making ohmic contact with SiC, a SiC electrode and a SiC device. ..

[0002]

2. Description of the Related Art A SiC semiconductor has large physical properties such as a melting point, an energy gap, a dielectric breakdown electric field, a thermal conductivity, a saturation speed, etc. It is thermally, chemically and mechanically stable and has excellent radiation resistance.

[0003]

For forming an ohmic electrode of SiC, for example, for p-type SiC, Al, Al / Ti laminated film, Al—Ti alloy, etc. are vapor-deposited on the surface of silicon carbide, and then 900 ° C. to 1100 ° C. It is known that a high temperature alloy treatment is carried out.

As n-type SiC, it is known that Ni, Ni / Ti / W laminated film or the like is vapor-deposited on the SiC surface and then subjected to high temperature alloying treatment.

[0004]
Further, as another example, in addition to the high temperature alloying treatment, ohmic contact with lower resistance is performed by increasing the impurity concentration (about 10 @ 19 cm @ -3) with respect to the silicon carbide in the region where the electrode contacts. Methods such as are known.

[0005]

However, when high temperature alloying is required, only heat-resistant materials can be used in the manufacture of SiC devices, and there are great restrictions on materials in the device manufacturing process. It will be.

In addition, agglomeration of the electrode material occurs during the high temperature alloy treatment, which makes it difficult to form a uniform ohmic electrode.

[0006]

On the other hand, an ion implantation method is used to form a region having a high impurity concentration with respect to silicon carbide, but ion implantation deteriorates the crystallinity of silicon carbide. Furthermore, when surface-treating SiC, the treatment hinders the efficiency of the semiconductor device manufacturing process.

[0007]
Therefore, an object of the present invention is to provide an electrode that can obtain ohmic contact without the need for high temperature alloying treatment and high carrier ion implantation, and a SiC device using the electrode.

[0008]

In order to solve the above-mentioned problems, an electrode according to the present invention comprises a semiconductor having a predetermined conductivity type and a conductive material having the same conductivity type as the conductivity type formed on the semiconductor. And an electrode made of a conductive oxide.

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The electrode according to the present invention is the electrode according to claim 1, wherein the semiconductor and the conductive oxide have substantially the same band gap.

[0009]
Further, the SiC electrode according to the present invention includes an electrode made of a predetermined conductivity type SiC and a conductive oxide of the same conductivity type as the conductivity type formed in contact with the SiC.

[0010]

As shown in FIG. 2, for example, the band structure of a conductive oxide such as SrTiO3 obtained by doping SrTiO3 with a predetermined amount of Nb is a wide-gap material similar to SiC. , Continuous band connection is assumed, and the Schottky barrier that occurs when a metal contacts a semiconductor does not occur.

The condition for the ohmic contact is determined by the magnitude of ΔE shown in FIG. ΔE is determined only by the position of the Fermi level (carrier concentration) Ef of SiC.

[0011]

Here, for example, for a SiC carrier concentration of 10 16 cm −3, Ef is located energetically 130 mV below the lower end of the conduction band. At this time, ΔE = 130 mV (slightly ΔE = 20 mV for 10 18 cm −3), which is an amount that can be treated as ohmic contact. Therefore, if the doping amount of SiC is 10 @ 16 cm @ -3 or more, ohmic contact becomes possible, and in the present invention, it is not necessary to dope the SiC to a high degree and the high temperature alloying process is not necessary.

[0012]
Further, in the SiC electrode of the present invention, the electrode made of a conductive oxide has a film made of the oxide and a metal body formed on the film.

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[0013]

Here, the oxide film has an ohmic property with SiC, and the metal body has an ohmic property with the oxide film.

The metal body may be a metal film or a metal wiring. In an electronic device, the conductive oxide itself has a higher resistance than a metal for wiring connection such as gold. Therefore, it is conceivable to connect a lead such as gold to the electrode made of the conductive oxide of the device. The conductive oxide can obtain a low resistance connection state with a predetermined metal, for example, a metal such as Ti or Al. Therefore, the electrode may be formed by providing the conductive oxide with a predetermined metal as, for example, a wiring connection metal (or a wiring connection metal further provided with a lead connection metal via a predetermined metal such as Ti or Al). Therefore, it is possible to connect to other circuits (devices) with low resistance as it is. In this case, the conductive oxide has a minimum interval (or film thickness) that allows low ohmic contact with SiC and low ohmic contact with a metal (for example, a metal for wiring connection). For example, it is desirable that it is provided over 500 Å.

[0014]
In the SiC electrode according to the present invention, the conductive oxide may be an oxide having a regular composition and having a specific resistance of about 1 Ωcm or less, for example, 1-10 −7 Ωcm. it can.

[0015]

Some conductive oxides have the highest conductivity when made into a regular composition, and some have metallic properties.

Such an oxide can be used as an electrode structure without implanting impurities. In addition to the oxides described in the embodiments, such conductive oxides include titanium oxide (TiO), lanthanum nickel oxide (LaNiO3), lanthanum copper oxide (LaCuO3), and copper ruthenium oxide. (CuRuO3), strontium iridium oxide (SrIrO3), strontium chromium oxide (SrCrO3), lithium titanium oxide (LiTi2 O4), rutinium oxide (RuO2), osmium oxide (OsO2), iridium oxide (IrO2), molybdenum oxide (IrO2). MoO2), tungsten oxide (WO2), rhenium oxide (ReO2), rhodium oxide (RhO2), β platinum oxide (β PtO2), lanthanum titanate (LaTiO3), ruthenium oxide (ReO3), copper aluminum oxide (CuAlO2), copper It is any oxide of gallium oxide (CuGaO2).

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[0016]

As described in the embodiments, these oxides have low specific resistance and can make good ohmic contact with the SiC semiconductor. Of these conductive oxides, when the SiC semiconductor is n-type, LaTiO3 or ReO3 is used. LaTiO3 has a resistivity of 10 @ -5 .OMEGA.cm and ReO3 has a resistivity of 10 @ -7 .OMEGA.cm. On the other hand, when the SiC semiconductor is p-type, CuAlO2 or CuGaO2 is used. The specific resistances of CuAlO2 and CuGaO2 are both about 1 Ωcm.

[0017]
Further, in the SiC electrode according to the present invention, the conductive oxide is an oxide having a normal composition doped with impurities and having an resistivity of 1 Ωcm or less, for example, 1 to 10 −7 Ωcm. You can

[0018]

Some conductive oxides exhibit conductivity due to generation of oxygen defects or interstitial ions due to deviation from the normal composition.

Therefore, the conductive oxide can be obtained by doping an insulating oxide having a regular composition with a predetermined impurity, and by using such a conductive oxide, ohmic contact with SiC can be obtained. You can Examples of such conductive oxides include tin oxide (SnO2), indium oxide (In2 O3), thallium oxide (Tl2 O3), thallium fluoride (TlOF), etc. other than those described in the embodiments. There is.

[0019]
Further, in the SiC electrode according to the present invention, the oxide used as the electrode by doping the oxide having the normal composition with impurities is any one of SrTiO3 and In2O3.

[0020]
It has been found that such an oxide can obtain remarkable conductivity by doping with a

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predetermined impurity, and an ohmic contact with SiC can be obtained also by using such a conductive oxide. An electrode can be obtained.

[0021]
In the SiC electrode according to the present invention, the SrTiO3 contains any one of Nb, Ta and La as an impurity, and the In2O3 contains Sn as an impurity.

[0022]

As described in the embodiments, SrTiO 3 is doped with any of Nb, Ta, and La, and In 2 O 3 is doped with Sn, so that these oxides have conductivity. And the ohmic contact with SiC can be made.

Therefore, an electrode having ohmic contact can be obtained by using such a conductive oxide.

[0023]
Further, the SiC device according to the present invention uses the electrode according to any one of claims 1 to 7 as an electrode of SiC, such as the electronic device shown in FIGS. 3 to 8.

[0024]

In such a SiC device, the electrode can be obtained without performing high temperature alloying treatment, high doping, or special surface treatment, so that the manufacturing process is simplified and restrictions on high temperature resistant materials and the like are relaxed.

Furthermore, since SiC is used for the semiconductor, stable and reliable operation is possible even under a severe environment such as high temperature and radiation.

[0025]

Further, in the SiC device according to the present invention, for example, in the electrode of

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MOSFET, the electrode (source and drain electrodes) can be obtained without performing high temperature alloying treatment, high doping or special surface treatment, so that the manufacturing process is simplified. In addition, restrictions such as high temperature resistant materials are alleviated.

Furthermore, since the semiconductor is made of SiC, stable and reliable operation is possible even under a severe environment such as high temperature and radiation.

The SiC provided with the source, drain, etc. may be a SiC substrate or a SiC substrate on which a SiC film is formed. Further, in the embodiment, the wiring connecting metal is provided on the conductive oxide.

[0026]

Further, in the SiC device according to the present invention, for example, in an electrode of a thermoelectric element, the electrode can be obtained without performing high temperature alloy treatment, high doping or special surface treatment, so that the manufacturing process is simplified, and the resistance is improved. The restrictions on high temperature materials etc. are alleviated. Furthermore, since the semiconductor is made of SiC, stable and reliable operation is possible even under a severe environment such as high temperature and radiation.

[0027]

Moreover, a copper electrode is generally used for the metal electrode of the thermoelectric element because of its good thermal conductivity. Therefore, by interposing a predetermined metal (for example, Ti, Al) between the copper and the conductive oxide, a low resistance electrical connection between the SiC and the copper electrode can be obtained. Al, Ti or the like is applied as the predetermined metal.

[0028]

BEST MODE FOR CARRYING OUT THE INVENTION Embodiments of the present invention will be described below with reference to the drawings. Embodiment 1. FIG. 1 is a sectional side view of

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an electrode showing the first embodiment. This electrode is formed by contacting the conductive oxide 2 on the SiC semiconductor 1 and further contacting the metal electrode 3 on the conductive oxide 2, so that the SiC semiconductor 1 and the conductive oxide 2 are separated from each other. It makes ohmic contact, and the conductive oxide 2 and the metal electrode 3 make ohmic contact.

[0029]

Here, when the SiC semiconductor 1 is n-type, the conductive oxide 2 is LaTiO3 or ReO3 as a conductive oxide having a regular composition. LaTiO3 has a specific resistance of 10-5 Ωcm, and ReO3 has a specific resistance of 10-7 Ωcm.

[0030]
The conductive oxide 2 can also be obtained by doping an insulating oxide having a regular composition with a predetermined impurity. In this case, for example, SrTiO3 doped with any one of Nb, Ta, and La, or In2O3 doped with Sn is used.

[0031]

Here, the doping amount of the above dopant into SrTiO3 is set to 0.1 to 5 atm%, and the specific resistance at this time is 1 to 10 @ -4 .OMEGA.cm.

Further, the doping amount of the above-mentioned dopant into Sn is set to 5 to 10 wt%, and the specific resistance at this time is 10 −4 to 10 −5 Ωcm.

[0032]

On the other hand, when the SiC semiconductor 1 is p-type, for the conductive oxide 2, CuAlO2 or CuGaO2 is used as a conductive oxide having a regular composition. The specific resistances of CuAlO2 and CuGaO2 are both about 1 Ωcm.

[0033]

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It should be noted that, in the p-type SiC semiconductor, an oxide that becomes conductive by doping an insulating oxide having a regular composition with a dopant has not been found at present. When found, the doped conductive oxide is included in the conductive oxide of the present invention.

[0034]

The method for producing the conductive oxide obtained by doping the insulating oxide with a dopant includes sputtering, laser ablation, and reactive co-evaporation.

For example, a method of producing SrTiO3 (hereinafter referred to as Nb-SrTiO3) obtained by doping SrTiO3 with Nb by sputtering is as follows. Is performed at a film forming temperature of 500 to 700 ° C. The method for producing Nb-SrTiO3 by laser ablation is carried out at a film forming temperature of 500 to 700 DEG C. with Nb-SrTiO3 as a target and O2 (0.01 to 1 torr) as an atmospheric gas. Further, the method for producing Nb-SrTiO3 by reactive co-evaporation is carried out at a film forming temperature of 500 to 700 DEG C. with Nb-SrTiO3 as an evaporation source and O2 (10-6 to 10-5 torr) as an atmosphere gas.

[0035]

In FIG. 1, the metal material that contacts the conductive oxide 2 is Ti or Al, which allows ohmic contact with the conductive oxide with low resistance. The n-type SiC semiconductor can be obtained as a film-like one by a CVD method in an atmosphere containing N, and as a bulk one by a sublimation method. Further, the p-type SiC semiconductor can be obtained in a film form by the CVD method in an atmosphere containing either Al or B, and can be obtained in a bulk form by the sublimation method. The carrier concentration of SiC is 1016 cm-3 to 1018 cm-3.

[0036]

FIG. 2 shows a band structure of Nb-SrTiO3 and an n-type SiC semiconductor obtained by the electrode described above. As shown in FIG. 2, the band structure of the conductive oxide has a degenerate semiconductor (Fermi level is in the conduction band) structure. The degeneracy width is determined by the carrier concentration, and the specific resistance value of the oxide is determined by the carrier concentration. In order to reduce the electrode resistance, it is desired

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that the carrier concentration be as high as possible.

[0037]

Since the band structure of the conductive oxide is a wide-gap material similar to that of SiC, continuous band connection is assumed in the bonding of these materials, and a Schottky barrier such as that produced by contact between a metal and a semiconductor does not occur. Does not happen. The condition for the ohmic contact is determined by the magnitude of ΔE shown in FIG. For example, if there is $\Delta E = 1$ eV, ohmic contact cannot be said. Further, ΔE is determined only by the position of the Fermi level (carrier concentration) Ef of SiC.

[0038]

Here, for example, for a SiC carrier concentration of 10 16 cm -3, Ef is located energetically 130 mV below the lower end of the conduction band. At this time, $\Delta E = 130$ mV (slightly $\Delta E =$ 20 mV for 10 18 cm -3), which is an amount that can be treated as ohmic contact. Therefore, if the doping amount of SiC is 10 @ 16 cm @ -3 or more, ohmic contact becomes possible, and in the present invention, it is not necessary to dope the SiC to a high degree and the high temperature alloying process is not necessary.

[0039]
The types of conductive oxides, impurities, and their doping amounts for the above-mentioned n-SiC and p-SiC, and the specific resistance obtained thereby are summarized below.

[0040]
n-SiC (Doped amount 1016 cm-3 or more) Conductive oxide Doped amount (resistivity) Nb, Ta or La doped SrTiO3 0.01-1 atm% (1-10-4 Ωcm) Sn-doped In2O3 (ITO) 0.01- 1wt% (10-4-10-5Ωcm) LaTiO3 undoped (10-5Ωcm) ReO3 undoped (10-7Ωcm)

[0041]
p-SiC (Doped amount 1016 cm-3 or more) Conductive oxide Doped amount (specific resistance) CuAlO2 undoped 1Ωcm CuGaO2 undoped 1Ωcm

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[0042]

Embodiment 2.

The second embodiment shows an example of a SiC device using the electrode of the first embodiment as a thin film electrode of deposited SiC.

FIG. 3 is a diagram showing an n-channel MOSFET and its manufacturing method.

As shown in FIG. 3 (h), this MOSFET includes a source region 1B and a drain region 1C provided on a p-type SiC substrate 1A, and a source region 1B, 1C on the SiC substrate 1. Gate oxide film 5 provided on the conductive oxide film, conductive oxide films 2A and 2B provided on the source and drain regions 1B and 1C, and wiring connection metal provided on the conductive oxide films 2A and 2B. It comprises layers 3A and 3B and a gate electrode 6 provided on the gate oxide film 5.

[0043]
Here, the conductive oxide films 2A and 2B and the wiring connection metal layers 3A and 3B provided thereon constitute the source and drain electrodes, respectively.

[0044]

Hereinafter, a method of manufacturing this MOSFET will be described with reference to FIG.

3A to 3C show a step of forming the source / drain region. First, as shown in FIG. 3A, an ion implantation (doping) mask 7 is formed on the p-type SiC substrate 1A. .. Here, as the p-type SiC substrate 1A, a SiC single crystal substrate doped with 1 × 10 15 -1 × 10 18 cm -3 of Al as an impurity was used. The mask 7 is formed by a SiO2 vapor deposition method which is obtained by forming a 1 .mu.m thick SiO2 film on the p-type SiC substrate 1A by a CVD method and then performing a photolithography step and an etching step.

[0045]

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Next, as shown in FIG. 3B, n-type impurity regions 1B and 1C are formed in the p-type SiC substrate 1A by an implantation method. Here, the implantation impurity is N or P, the implantation temperature is 500 to 1000 ° C., and the implantation amount is 1 × 10 18 -1 × 10 21 cm -3. Thereafter, the mask 7 is removed by etching, and the annealing treatment for activating the impurities injected into the n-type impurity regions 1B and 1C so as to function as carriers is performed at 800 to 1500 ° C. in vacuum or inactive. This is performed in gas to obtain the source region 1B and the drain region 1C as shown in FIG.

[0046]

Next, the gate oxide film shown in FIGS. 3D to 3E is formed. First, in (d), the p-type SiC substrate 1A is oxidized in an oxygen atmosphere at 1200 ° C. to form a SiO 2 film 5A having a film thickness of 500 Å on the surface. Then, as shown in (e), the oxide film 5A on the source region 1B and the drain region 1C is removed through a photolithography and etching process to obtain the gate oxide film 5.

[0047]

Next, the source, drain, and gate electrodes shown in FIGS. 3F to 3H are formed. First, a conductive oxide having a thickness of 500 Å is formed on the p-type SiC substrate 1A by a sputtering method or the like, and is subjected to photolithography and etching steps, and then, as shown in FIG. 3 (f), source / drain regions 1B, 1C are formed. Conductive oxides 2A and 2B as contact electrodes are formed thereon. Here, as the conductive oxide, SrTiO3 doped with 1 atm% of Nb was used.

[0048]

Next, Al or Ti as a contact layer for the wiring layer having a thickness of 2000 Å is formed on the p-type SiC substrate 1A by a vacuum deposition method or the like, and is subjected to a photolithography and etching process, as shown in FIG. The wiring connection metal layers 3A and 3B are formed on the conductive oxide films 2A and 2B.

[0049]

Finally, polycrystalline Si having a thickness of 2000 Å is formed on the p-type SiC substrate 1A

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by a sputtering method or the like, and is subjected to a photolithography and etching process, and the polycrystalline Si is converted into a gate oxide film as shown in FIG. 3 (h). The gate electrode 6 is formed so that it exists only on the gate electrode 5.

[0050]

As described above, in the SiC device according to the second embodiment, the metal electrode layer, which is the wiring layer, is connected through the conductive oxide film (contact electrode) that makes ohmic contact with the SiC, so that high temperature alloying is not required. Also, it is not necessary to provide a high carrier layer on SiC.

[0051]

Embodiment 3.

The third embodiment shows an example of an electronic device using the electrode of the first embodiment as a SiC bulk electrode.

FIG. 4 is a diagram showing a thermoelectric element using a SiC bulk and a method for manufacturing the same.

As shown in FIG. 4 (c), this thermoelectric element includes p-type SiC 1E and n-type first and second conductive oxides (2D-1, 2D-2) provided with n-type SiC 1D sandwiched therebetween. The p-type third and fourth conductive oxides (2E-1, 2E-2), the n-type conductive oxide 2D-2, the p-type conductive oxide 2E-2, and the metal film 3D, which are provided so as to be sandwiched therebetween. The first metal electrode 8 connected via the second metal electrode 10 connected to the n-type conductive oxide 2D-1 via the metal film 3E, and the p-type conductive oxide 2E-1 connected to the metal film. And a third metal electrode 9 connected via 3E.

[0052]

Hereinafter, a method of manufacturing this thermoelectric element will be described with reference to FIG. First, as shown in (a), CuAlO2 (2E-1, 2E-2), which is a p-type conductive oxide, is formed on both sides of a p-type SiC1E obtained by a sublimation method by a sputtering

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method or the like (Thickness 500 Å). Further, strontium titanate (2D-1, 2D-2) doped with 1 atm% of Nb, which is an n-type conductive oxide, is formed on both sides of the n-type SiC 1D by a sputtering method or the like (thickness 500 Å).

[0053]

Next, as shown in (b), contact metal films 3D and 3E are formed on the films of the conductive oxides (2D-1, 2D-2, 2E-1, 2E-2) respectively formed as contact metal films 3D and 3E. An Al film or a Ti film is formed by a vacuum evaporation method or the like (thickness 10 μm). Then, as shown in (c), the first metal electrode (copper electrode) 8 is soldered and laid over the vacuum-deposited contact metal films 3D, 3D, and at the same time, the first metal electrodes (copper electrodes) 8 are formed on the contact metal films 3E, 3E. The second and third metal electrodes (copper electrodes) 9 and 10 are soldered and attached.

[0054]

In the thermoelectric element manufactured in this manner, ohmic contact between the metal electrodes (for example, copper electrodes) 8 to 10 and the SiC semiconductor can be easily obtained, and the contact metal layer can reduce the resistance. The reason why copper is used for the metal electrode is that copper has excellent thermal conductivity and can enhance the power / heat exchange efficiency of the thermoelectric element.

[0055]

Fourth Embodiment FIG. 5 is a sectional view showing an n-channel junction type field effect transistor (JFET) as another example of an electronic device using SiC. This JFET has p-type regions 1G and 1G on each of the two surfaces facing the n-type SiC 1F, and Al for gates is formed on these regions via p-type conductive oxide films 2F and 2F, respectively. Wiring connection metal films 3F and 3F made of Ti are provided. Further, on the other facing surface of the n-type SiC 1F, wiring connection metal films 3G and 3H made of Al and Ti for the source and drain are provided via the n-type conductive oxide films 2G and 2H, respectively. Has been.

[0056]

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Embodiment 5. FIG. 6 is a cross-sectional view showing an n-channel junction field effect transistor (MESFET) as another example of an electronic device using SiC. In this MESFET, a Schottky gate electrode 3I made of, for example, a Pt film is provided on the n-type SiC 1H, and wiring connection metal films made of Al and Ti are provided on both sides of the Schottky gate electrode 3I via the n-type conductive oxide films 2I and 2J. 3J and 3K are provided as a source electrode and a drain electrode, respectively.

[0057]

Sixth embodiment. FIG. 7 is a sectional view showing a thyristor as another example of the electronic device using SiC. In this thyristor, SiC p-layers 1I, n-layers 1J, p-layers 1K, and n-layers 1L are alternately provided from the left end in the drawing, and Al, p-type conductive oxide film 2K and Al A metal film 3L for wiring connection made of Ti is provided to form an anode electrode. Further, a metal film 3M for wiring connection made of Al and Ti is provided on the rightmost n layer 1L via the n-type conductive oxide film 2L to form a cathode electrode. Further, the p-layer 1K adjacent to the n-layer 1L at the right end is provided with the wiring connection metal film 3N made of Al and Ti via the p-type conductive oxide film 2M to form a gate electrode.

[0058]

Embodiment 7. FIG. 8 shows an insulated gate bipolar transistor (IGBT) using SiC, in which n-type SiC1M is formed in the upper half of the substrate and p-type SiC1N is formed in the lower half. On the lower surface of the p-type SiC 1N, a wiring connection metal film 3S made of Al and Ti is provided via a p-type conductive oxide film 2N to form a collector electrode. P layers 1P and 1Q are provided on both sides of the upper surface of the n-type SiC 1M, and wiring connection metal films 3P and 3Q made of Al and Ti are provided on the p layers 1P and 1Q via the n-type conductive oxide films 2Q and 2P. The electrodes provided are configured. Of these electrodes, the left electrode is used as an emitter electrode, and the right electrode is used as a gate voltage control terminal.

[0059]

Further, a metal film 3R for wiring connection made of Al and Ti is provided on the upper surface

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of the n-type SiC 1M via a gate oxide film 5B. In addition, the n-type conductive oxide films 2Q and 2P are surrounded by the substrate and between the gate electrode and the emitter electrode and the gate voltage control terminal in the p-layers 1P and 1Q, respectively. And 1T and 1U are provided.

[0060]
Since the electronic device as described above uses SiC, it has excellent dielectric breakdown, can use a large amount of power, and maintains high reliability and stability even under severe conditions such as high temperature and radiation. obtain.

[0061]
As described above, the present invention comprises a semiconductor having a predetermined conductivity type and an electrode formed on the semiconductor and made of a conductive oxide having the same conductivity type as the conductivity type. Therefore, it is possible to obtain an electrode, a SiC electrode and a SiC device that do not require high temperature alloying and high carrier ion implantation.

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CLAIMS JP2000101064

1.
An electrode comprising a semiconductor having a predetermined conductivity type and an electrode formed on the semiconductor and made of a conductive oxide having the same conductivity type as the conductivity type.

2.
The electrode according to claim 1, wherein the band gaps of the semiconductor and the conductive oxide are substantially equal to each other.

3.
An electrode of SiC, comprising an electrode made of SiC of a predetermined conductivity type and a conductive oxide of the same conductivity type as the conductivity type formed in contact with the SiC.

4.
The SiC electrode according to claim 3, wherein the electrode made of the conductive oxide has a film made of the oxide and a metal body formed on the film.

5.
The SiC electrode according to any one of claims 1 to 4, wherein the conductive oxide is lanthanum titanate, rhenium oxide, copper aluminum oxide, or copper gallium oxide.

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6.
The SiC electrode according to any one of claims 1 to 4, wherein the conductive oxide is either strontium titanate or indium oxide.

7.
The SiC electrode according to claim 6, wherein the strontium titanate contains any one of Nb, Ta, and La as an impurity, and the indium oxide contains Sn as an impurity.

8.
A SiC device using SiC as a semiconductor, wherein the SiC electrode according to any one of claims 1 to 7 is used.

9.
A source and a drain provided on the SiC, a gate electrode provided between the source and the drain on the SiC, and an electrode made of a conductive oxide provided on the source and the drain. SiC device.

10.
N-type SiC, p-type SiC, first and second n-type conductive oxides sandwiching the n-type SiC, and third and fourth sandwiching the p-type SiC A p-type conductive oxide, a first metal electrode for connecting the second conductive oxide and the fourth conductive oxide, and a second metal electrode provided for the first conductive oxide. A SiC device comprising a metal electrode and a third metal electrode provided for the third conductive oxide.

11.
11. The SiC device according to claim 10, wherein between the first conductive oxide and the second metal electrode, between the second conductive oxide and the first metal electrode, and the first conductive oxide. And a predetermined metal having ohmic characteristics with each conductive oxide between the third conductive metal oxide and the third metal electrode and between the fourth conductive oxide and the first metal electrode. A SiC device in which

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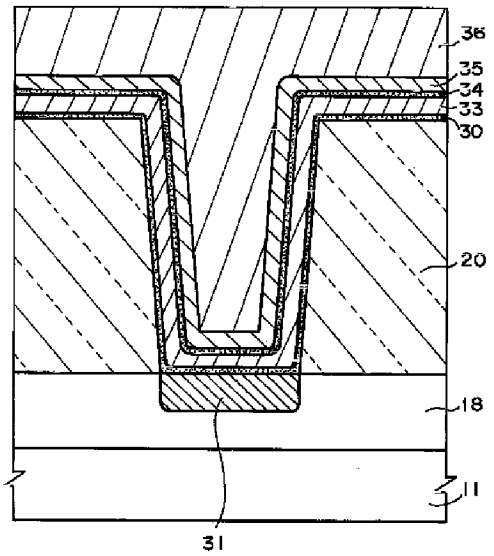
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(71)出願人　000002369
セイコーエプソン株式会社
東京都新宿区西新宿２丁目４番１号
(72)発明者　朝比奈　通雄
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内
(72)発明者　松本　和己
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内
(74)代理人　100090479
弁理士　井上　一　（外２名）

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(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【課題】　バリア性が優れたバリア層を有する半導体装置およびその製造方法を提供する。
【解決手段】　半導体装置は、素子を含む半導体基板１１、半導体基板１１の上に形成された層間絶縁層（シリコン酸化層，ＢＰＳＧ層）、層間絶縁層に形成されたスルーホール、層間絶縁層およびスルーホールの表面に形成されたバリア層、およびバリア層の上に形成された配線層４０を有する。バリア層は、該バリア層を構成する金属の酸化物からなる第１の金属酸化物層（酸化チタン層）３０、該バリア層を構成する金属の窒化物からなる金属窒化物層（窒化チタン層）３３、および該バリア層を構成する金属の酸化物からなる第２の金属酸化物層（酸化チタン層）３４を有する。



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【特許請求の範囲】
【請求項１】　素子を含む半導体基板、
前記半導体基板の上に形成された層間絶縁層、
前記層間絶縁層に形成されたスルーホール、
前記層間絶縁層および前記スルーホールの表面に形成されたバリア層、および前記バリア層の上に形成された配線層、を含み、
前記バリア層は、
該バリア層を構成する金属の酸化物からなる金属酸化物層、および該バリア層を構成する金属の窒化物からなる金属窒化物層を含む、半導体装置。
【請求項２】　請求項１において、
前記バリア層は、
該バリア層を構成する金属の酸化物からなる第１の金属酸化物層、
該バリア層を構成する金属の窒化物からなる金属窒化物層、および該バリア層を構成する金属の酸化物からなる第２の金属酸化物層、
を含む、半導体装置。
【請求項３】　請求項１または２において、
前記バリア層を構成するための金属は、チタン、コバルト、ルテニウム、モリブデン、ハフニウム、ニオブ、バナジウム、タンタルおよびタングステンから選択される少なくとも１種を含む、半導体装置。
【請求項４】　請求項１ないし３のいずれかにおいて、
前記バリア層を構成する第１および第２の金属酸化物層は、アモルファスをなす、半導体装置。
【請求項５】　請求項１ないし４のいずれかにおいて、
前記バリア層を構成する第１の金属酸化物層は、その膜厚が５～３０ｎｍである、半導体装置。
【請求項６】　請求項１ないし５のいずれかにおいて、
前記バリア層を構成する第２の金属酸化物層は、その膜厚が５～３０ｎｍである、半導体装置。
【請求項７】　請求項１ないし６のいずれかにおいて、
前記配線層は、アルミニウムあるいはアルミニウムを主成分とする合金からなる、半導体装置。
【請求項８】　素子を含む半導体基板の上に形成された層間絶縁層にスルーホールを形成する工程、
前記層間絶縁層および前記スルーホールの表面にバリア層を形成する工程、および前記バリア層の上に配線層を形成する工程、を含み、
前記バリア層を形成する工程は、以下の工程（ａ）～（ｄ）を含む、半導体装置の製造方法。
（ａ）前記バリア層を構成するための金属層を形成する工程、（ｂ）水素雰囲気中で熱処理することにより、前記金属層を水素合金化あるいは水素吸蔵化させる工程、（ｃ）酸素を含む雰囲気中で、前記金属層と酸素とを接触させる工程、および（ｄ）窒素雰囲気中で熱処理することにより、金属酸化物層および金属窒化物層を形成する工程。
【請求項９】　請求項８において、
前記バリア層は、
該バリア層を構成する金属の酸化物からなる第１の金属酸化物層、
該バリア層を構成する金属の窒化物からなる金属窒化物層、および該バリア層を構成する金属の酸化物からなる第２の金属酸化物層、
を含む、半導体装置の製造方法。
【請求項１０】　請求項８または９において、
前記工程（ｂ）において、前記熱処理は２００～８００℃で行われる、半導体装置の製造方法。
【請求項１１】　請求項８ないし１０のいずれかにおいて、
前記工程（ｃ）において、前記酸素を含む雰囲気は、少なくとも酸素が１０体積％含まれる、半導体装置の製造方法。
【請求項１２】　請求項８ないし１１のいずれかにおいて、
前記工程（ｄ）において、前記熱処理は６００～９００℃で行われる、半導体装置の製造方法。
【請求項１３】　請求項８ないし１２のいずれかにおいて、
前記工程（ｄ）において、前記窒素雰囲気は常圧状態である、半導体装置の製造方法。
【請求項１４】　請求項８ないし１３のいずれかにおいて、
前記バリア層を形成するための金属は、チタン、コバルト、ルテニウム、モリブデン、ハフニウム、ニオブ、バナジウム、タンタルおよびタングステンから選択される少なくとも１種を含む、半導体装置の製造方法。
【請求項１５】　請求項８ないし１４のいずれかにおいて、
前記バリア層を形成するための金属層は、その膜厚が５０～１５０ｎｍである、半導体装置の製造方法。
【請求項１６】　請求項８ないし１５のいずれかにおいて、
前記配線層は、アルミニウムあるいはアルミニウムを主成分とする合金からなる、半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置およびその製造方法に関し、特に微細化されたコンタクト部においてバリア性に優れた半導体装置およびその製造方法に関する。
【０００２】
【背景技術】ＬＳＩの素子の微細化、高密度化および多層化に伴い、微細でアスペクト比の大きいスルーホールでの配線材料の埋め込み技術が重要な課題となっている。従来、例えば、０．５μｍ以下の口径サイズおよびアスペクト比が２以上のコンタクト部においては、スル

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ーホールにタングステンプラグを挿入して、スルーホールを塞ぐとともに配線層のアルミニウムとシリコン基板のシリコンとの反応を防止している。しかし、このコンタクト構造では、タングステンの電気的抵抗が大きいこと、エレクトロマイグレーション耐性の劣化が生じやすいこと、および工程が複雑なことから生ずる歩留まりの低下などの問題がある。そこで、電気的抵抗が小さく、タングステンプラグのように複雑な埋め込み工程を必要としない、スルーホールへのアルミニウムの埋め込み技術の導入が検討されている。

【０００３】しかし、アルミニウムを用いたコンタクト部では、アルミニウムとシリコン基板のシリコンとの反応によるジャンクションリークの対策を完璧に行なう必要があり、バリア層のバリア性が高いことが要求される。

【０００４】バリア層としては、例えば、窒素雰囲気中での反応性スパッタ法で形成された、窒化チタンなどの高融点金属の窒化物層が用いられている。このようなバリア層は、以下のような問題を有している。

【０００５】① 窒素雰囲気中での反応性スパッタ法で形成された窒化チタン層は、カバレッジ性が不十分であることから、微細で高いアスペクト比のスルーホールの底部でのカバレッジが十分でないこと。

【０００６】② 窒素雰囲気中での反応性スパッタ法で形成された窒化チタン層は、膜のストレスが大きいため、マイクロクラックが生じやすく、その結果、配線材料のアルミニウムが拡散してジャンクションリークが発生しやすいこと。

【０００７】③ 窒素雰囲気中での反応性スパッタ法により形成された窒化チタン層は、柱状結晶のため、結晶粒界を介してアルミニウムが拡散してジャンクションリークが生じやすいこと。

【０００８】④ 柱状結晶の窒化チタン層の配向によりアルミニウム層の〈１１１〉配向が決定されるが、窒化チタンの結晶配向が必ずしも均一でないことからアルミニウム層の〈１１１〉配向の面方位の違いにより、アルミニウム層の表面荒れが生じ、このアルミニウム層のフォトリソグラフィーでのアライメントが困難となること。

【０００９】⑤ さらに、窒素雰囲気中での反応性スパッタ法により形成された窒化チタン層は、その膜ストレスのため成膜中に剥離を生ずることがあり、パーティクルを生じやすく、このパーティクルによるウエハ表面の汚染によりパーティクルショートが生じ、歩留まりの低下の原因となっていること。

【００１０】

【発明が解決しようとする課題】本発明の目的は、例えばハーフミクロン以下の微細なコンタクト部での導電材料の埋め込みが良好に行なわれ、かつジャンクションリークがなく高いバリア性を有する、半導体装置およびその製造方法を提供することにある。

【００１１】

【課題を解決するための手段】本発明に係る半導体装置は、素子を含む半導体基板、前記半導体基板の上に形成された層間絶縁層、前記層間絶縁層に形成されたスルーホール、前記層間絶縁層および前記スルーホールの表面に形成されたバリア層、および前記バリア層の上に形成された配線層、を含み、前記バリア層は、該バリア層を構成する金属の酸化物からなる金属酸化物層、および該バリア層を構成する金属の窒化物からなる金属窒化物層を含む。

【００１２】この半導体装置によれば、バリア層は、金属窒化物層に加え、金属酸化物層を含み、高い導電性を確保しながら優れたバリア性を有する。

【００１３】前記バリア層は、該バリア層を構成する金属の酸化物からなる第１の金属酸化物層、該バリア層を構成する金属の窒化物からなる金属窒化物層、および該バリア層を構成する金属の酸化物からなる第２の金属酸化物層、を含むことが望ましい。

【００１４】そして、前記バリア層を構成する第１および第２の金属酸化物層は、高いバリア性を得るために、アモルファスをなすことが望ましい。

【００１５】前記バリア層を構成する第１の金属酸化物層は、バリア性および導電性を考慮すると、その膜厚が５～３０ｎｍであることが望ましい。同様に、前記バリア層を構成する第２の金属酸化物層は、その膜厚が５～３０ｎｍであることが望ましい。これらの金属酸化物層は、連続していてもよく、あるいは不連続であってもよい。

【００１６】前記配線層は、アルミニウムあるいはアルミニウムを主成分とする合金からなることが望ましい。前記配線層の材料としては、これらのアルミニウムあるいはアルミニウム合金の他にも、銅、金、白金などを用いることができる。また、必要に応じて、スルーホールの埋込み材としてタングステンプラグを用いてもよい。

【００１７】本発明に係る半導体装置は、素子を含む半導体基板の上に形成された層間絶縁層にスルーホールを形成する工程、前記層間絶縁層および前記スルーホールの表面にバリア層を形成する工程、および前記バリア層の上に配線層を形成する工程、を含み、前記バリア層を形成する工程は、以下の工程（ａ）～（ｄ）を含む製造方法によって形成される。

（ａ）前記バリア層を構成するための金属層を形成する工程、（ｂ）水素雰囲気中で熱処理することにより、前記金属層を水素合金化あるいは水素吸蔵化させる工程、（ｃ）酸素を含む雰囲気中で、前記金属層と酸素とを接触させる工程、および（ｄ）窒素雰囲気中で熱処理することにより、金属酸化物層および金属窒化物層を形成する工程。

【００１８】この製造方法においては、前記バリア層は、金属酸化物層および金属窒化物層を含んで形成さ

れ、さらに詳細には、前記バリア層は、該バリア層を構成する金属の酸化物からなる第１の金属酸化物層、該バリア層を構成する金属の窒化物からなる金属窒化物層、および該バリア層を構成する金属の酸化物からなる第２の金属酸化物層、を含んで形成される。

【００１９】本発明の製造方法によれば、工程（ａ）においては、スパッタ法やＣＶＤ法などによって単一の金属層を形成し、その後工程（ｄ）で金属窒化物層を形成するので、例えばスパッタ法で直接金属窒化物層を形成する場合に比べて、密着性およびスルーホール底部でのカバレッジが良好な成膜ができる。また、工程（ａ）で金属層を形成した後、工程（ｂ）において、該金属層を水素合金化あるいは水素吸蔵化させることにより、その後の熱処理で半導体基板のシリコンと金属層の金属との反応がある程度抑制される。その結果、工程（ｄ）における金属の窒化反応および酸化反応が確実に行われ、金属窒化物層および金属酸化物層が形成される。そして、金属酸化物層が存在することにより、バリア層のバリア性が飛躍的に向上し、かつ、バリア層の導電性も確保されることが確認されている。

【００２０】前記金属酸化物層が金属窒化物層を介在させて第１および第２の２層で形成される理由は、必ずしも明らかではないが以下のように考えられる。つまり、工程（ａ）で形成される金属層に酸素が吸蔵されており、さらに工程（ｃ）で金属層と酸素とを接触させることにより、酸素が金属層の中および表面に導入される。そして、工程（ｂ）の熱処理で、第１の金属酸化物層の一部が形成され、工程（ｄ）の熱処理で、さらに第１の金属酸化物層の形成が進むとともに、金属窒化物層および第２の金属酸化物層が形成される。

【００２１】前記工程（ｂ）において、前記熱処理は、前記金属層を十分に水素合金化あるいは水素吸蔵化させるために、２００～８００℃で行われることが望ましい。また、水素雰囲気での水素の割合は、処理温度にも依存するが、１～１００％であることが望ましい。

【００２２】前記工程（ｃ）において、前記酸素を含む雰囲気は、少なくとも酸素が１０％、好ましくは１０～３０％含まれることが望ましい。この工程では、前記工程（ｂ）で水素合金化あるいは水素吸蔵化された金属層の表面に酸素が接触すればよい。

【００２３】前記工程（ｄ）において、前記熱処理は、水素が脱離し、かつ前記金属層の窒化と酸化が行われるために、６００～９００℃で行われることが望ましい。そして、前記工程（ｄ）では、雰囲気の圧力は特に限定されないが、常圧であることが望ましい。

【００２４】前記バリア層を形成するための金属は、バリア性および導電性を考慮すると、チタン、コバルト、ルテニウム、モリブデン、ハフニウム、ニオブ、バナジウム、タンタルおよびタングステンから選択される少なくとも１種を含むことが望ましい。

【００２５】前記バリア層を形成するための金属層は、その後の工程で形成される金属窒化物層および金属酸化物層の膜厚を考慮すると、その膜厚が５０～１５０ｎｍであることが望ましい。

【００２６】

【発明の実施の形態】図１～図６は、本発明に係る半導体装置の製造方法を示し、図７は半導体装置の一実施の形態を説明するための概略断面図である。

【００２７】以下に、半導体装置の製造方法の一例を示す。

【００２８】（素子の形成）まず、図１に示すように、一般的に用いられる方法によって、シリコン基板１１にＭＯＳ素子が形成される。具体的には、例えば、シリコン基板１１上に選択酸化によってフィールド絶縁層１２が形成され、アクティブ領域にゲート酸化層１３が形成される。チャネル注入により、しきい値電圧を調整した後、モノシラン（SiH_4）を熱分解して成長させたポリシリコン層１４の上にタングステンシリサイド層１５がスパッタされ、さらに所定パターンにエッチングすることにより、ゲート電極１９が形成される。

【００２９】次いで、リンをイオン注入することによりソース領域あるいはドレイン領域の低濃度不純物層１６が形成される。次いで、ゲート電極１９のサイドにシリコン酸化膜からなる側壁スペーサ１７が形成された後、ヒ素をイオン注入し、ハロゲンランプを用いたアニール処理によって不純物の活性化を行うことにより、ソース領域あるいはドレイン領域の高濃度不純物層１８が形成される。

【００３０】（層間絶縁層の形成）次に、図２に示すように、層間絶縁層２０のベース層として、まず、テトラエトキシラン（ＴＥＯＳ）と酸素とをプラズマ反応させることにより、膜厚１００～２００ｎｍのシリコン酸化層（図示せず）が形成される。このシリコン酸化層は、カスピングもなく、SiH_4から成長させた膜より絶縁性も高くフッ化水素の水溶液に対するエッチング速度も遅く、緻密な膜となる。

【００３１】次に、層間絶縁層２０の平坦化層として、前記シリコン酸化層上に、SiH_4あるいはＴＥＯＳなどのシラン化合物と、酸素やオゾン等と、リンおよびホウ素とを含むガスを気相反応させることにより、膜厚数百ｎｍ～１μｍ位のＢＰＳＧ層（図示せず）が形成される。その後、窒素雰囲気中で８００～９００℃のアニールを行い、高温フローによる平坦化を行う。なお、ＢＰＳＧ層の高温フローを行う代わりに、一般的に用いられるＳＯＧ膜を用いて平坦化を行うこともできる。

【００３２】さらに、前記ＢＰＳＧ層の代わりに、本出願の出願人による特許願（たとえば特願平９－３１４５１８号）に記載された、シリコン化合物と過酸化水素とを化学気相成長法によって反応させて形成されるシリコン酸化層を用いてもよい。このシリコン酸化層は、それ

自体で高い流動性を有し、優れた自己平坦化特性を有する。そのメカニズムは、シリコン化合物と過酸化水素とを化学気相成長法によって反応させると、気相中においてシラノールが形成され、このシラノールがウエハ表面に堆積することにより流動性のよい膜が形成されることによると考えられる。

【００３３】前記シリコン化合物としては、例えばモノシラン、ジシラン、SiH_2Cl_2、SiF_4などの無機シラン化合物、およびCH_3SiH_3、トリプロピルシラン、テトラエトキシシランなどの有機シラン化合物などを例示することができる。

【００３４】また、このシリコン酸化層の成膜工程は、前記シリコン化合物が無機シリコン化合物の場合には、０～２０℃の温度条件下で、前記シリコン化合物が有機シリコン化合物の場合には、１００～１５０℃の温度条件下で、減圧化学気相成長法によって行われることが望ましい。

【００３５】（スルーホールの形成）次いで、図２に示すように、CHF_3とCF_4とを主ガスとした反応性イオンエッチャーで層間絶縁層２０を構成するＢＰＳＧ層（平坦化層）およびシリコン酸化層（ベース層）を選択的に異方性エッチングすることにより、口径が０．２～０．５μｍ、アスペクト比が２～5のスルーホール２２が形成される。

【００３６】（バリア層の成膜）

（ａ）金属層の形成

まず、図3に示すように、ターゲットとウエハとの距離が１５０～３２０ｍｍの超ロングスロースパッタ装置で、層間絶縁層２０およびスルーホール２２の表面に膜厚５０～１５０ｎｍのチタン層２９を形成する。スルーホール２２の底部におけるチタン層２９の膜厚はおよそ１５～８０ｎｍであり、また、チタン層２９のスルーホール２２でのカバレッジも良好で、スルーホールの上部におけるせり出しもほとんどない。このように超ロングスロースパッタによってチタン層２９を形成することにり、スルーホール上部で、ウェッテイング層を構成する金属と埋込み層を構成するアルミニウムとが反応して、スルーホールを塞いでしまうピンチオフ現象を生じにくい。

【００３７】バリア層を形成するための金属としては、チタンの他に、コバルト、ルテニウム、モリブデン、ハフニウム、ニオブ、タンタル、タングステンなども用いることができる。

【００３８】（ｂ）水素雰囲気中での熱処理

次いで、１００％の水素雰囲気中で、２００～８００℃で、かつ２０～６０分にわたってウエハをアニール処理する。この工程で、チタン層２９は水素合金化あるいは水素吸蔵化される。すなわち、チタンの場合を例にとると、図４に示すように、例えば４００℃で２０分間のアニールにより、チタン層に１０原子％以上の水素が吸蔵され、TiH_X合金層３２が形成されるとともに、シリコン基板１１との境界領域ではチタンとシリコンとの反応が起こり、チタンシリサイド層３１が形成される。さらに、チタン層２９の最表面には、酸素が含まれる酸素リッチ層が形成される。

【００３９】この工程（ｂ）において、金属層を水素合金化あるいは水素吸蔵化させることにより、アニール処理で半導体基板のシリコンと金属層を構成するチタンとの反応がある程度抑制される。その結果、後の工程（ｄ）における金属の窒化反応および酸化反応が確実に行われ、金属窒化物層および金属酸化物層が形成される。

【００４０】（ｃ）次いで ウエハを酸素を含む雰囲気、例えば大気中に置くことより、TiH_X合金層３２と酸素とを接触させる。この工程により、TiH_X合金層３２の表面に酸素が吸着される。

【００４１】この工程では、ウエハを大気中に置く変わりに、酸素を１０～３０体積％の濃度で含む雰囲気中に存在させてもよい。

【００４２】（ｄ）次いで、常圧の窒素雰囲気中で、６００～８００℃で１０～６０秒にわたって、ランプアニールによる熱処理を行なうことにより、さらに金属の窒化とシリサイド化と酸化とを行なう。この工程では、TiH_X合金層３２中の水素はほとんど脱離し、図5に示すように、チタンと窒素との反応による窒化チタン層３３、チタンとシリコン基板１１のシリコンとの反応によるチタンシリサイド層３１とが形成される。これとともに、図7に拡大して示すように、チタンシリサイド層３１と窒化チタン層３３との境界領域に第１の酸化チタン層（第１の金属酸化物層）３０が、窒化チタン層３３の表面に第２の酸化チタン層（第２の金属酸化物層）３４が形成される。第１の酸化チタン層（第１の金属酸化物層）３０は、アモルファスの状態をなしていることが確認された。また、第２の酸化チタン層３４は、窒化チタン層３３の表面に不連続に形成され、やはりアモルファスの状態をなしていることが確認された。

【００４３】バリア層を構成する第１の酸化チタン層は、バリア性および導電性を考慮すると、その膜厚が５～３０ｎｍであることが望ましい。同様に、バリア層を構成する第２の酸化チタン層は、その膜厚が５～３０ｎｍであることが望ましい。

【００４４】これらの第１および第２の酸化チタン層３０，３４により、バリア層は優れたバリア機能を有する。また、第１および第２の酸化チタン層３０，３４の膜厚、ランプアニールの温度などが制御されることにより、バリア層における導電性も十分に確保される。

【００４５】以上の工程によって、バリア層は、少なくとも、第１の酸化チタン層３０、窒化チタン層３３および第２の酸化チタン層３４を有する。

【００４６】上記工程（ａ）～（ｄ）の後に、必要に応

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じて、酸素プラズマ処理を行うことができる。この酸素プラズマ処理は、0.1×10²～1.5×10²Paの圧力で酸素プラズマ中に10～100秒間さらし、次いで、450～700℃の窒素または水素雰囲気中で10～60分間にわたってアニール処理することにより行われる。この酸素プラズマ処理により、バリア層の窒化チタン層中に酸化チタンを島状に形成することができる。そして、この処理によりバリア層のバリア性をさらに向上させることができることを確認している。

【0047】また、バリア層中に酸化チタンを島状に形成する方法としては、少なくとも数百ppm～数%の酸素を含むランプアニール炉における400～800℃の熱処理によっても行うことができ、同様にバリア層のバリア性をさらに向上させることができる。

【0048】(脱ガス処理) 次に、脱ガス工程を含む熱処理ついて説明する。

【0049】まず、ランプチャンバで、1.5×10⁻⁴Pa以下のベース圧力、150～250℃の温度で30～60秒間のランプ加熱 (熱処理A) を施す。次いで、別のチャンバで1×10⁻¹～15×10⁻¹Paの圧力でアルゴンガスを導入し、300～550℃の温度で、30～120秒間の熱処理 (脱ガス工程；熱処理B) を行うことによって、脱ガス処理を行う。

【0050】この工程においては、まず、熱処理Aにおいて、主として、ウエハの裏面および側面を含むウエハ全体を加熱処理することにより、ウエハに付着している水分などを除去できる。

【0051】さらに、熱処理Bにおいて、主として、層間絶縁層20を構成するBPSG層などの平坦化層中のガス化成分 (酸素，水素，水，チッ素) を除去することができる。その結果、次工程のアルミニウム膜の形成時に、BPSG層からのガス化成分の発生が防止できる。

【0052】バリア層は数十原子%のガス化成分 (酸素，水素，水，チッ素) を固溶することから、バリア層の形成後に、層間絶縁層20中のガス化成分を除去することが、スルーホール内でのアルミニウム膜の成膜を良好に行う上で、極めて有効である。バリア層の下位の平坦化層中のガス化成分を十分に除去しておかないと、バリア層の形成時の温度 (通常、300℃以上) で、平坦化層中のガス化成分が放出され、このガスがバリア層中に取り込まれる。さらに、このガスがアルミニウム膜の成膜時にバリア層から離脱してバリア層とアルミニウム膜との界面に出てくるため、アルミニウム膜の密着性や流動性に悪影響を与えることがある。

【0053】(ウェッティング層の形成) さらに、必要に応じて、チタン、ニオブ、タングステンなどの金属を常温で20～50nmの膜厚で成膜し、ウェッティング層35を形成する。

【0054】(アルミニウム層の成膜前の熱処理およびウエハの冷却) まず、ウエハの冷却を行う前に、ランプチャンバ内において、1.5×10⁻⁴Pa以下のベース圧力、150～250℃の温度で30～60秒間の熱処理 (熱処理C) を行い、基板に付着した水などの物質を除去する。その後、アルミニウム層を成膜する前に、基板温度を100℃以下、好ましくは常温～50℃の温度に下げる。この冷却工程は、上記熱処理Cにより上昇した基板温度を下げるために重要なもので、例えば水冷機能を有するステージ上にウエハを載置して該ウエハ温度を所定温度まで下げる。

【0055】このようにウエハの冷却を行うことにより、第1のアルミニウム層を成膜する際に、層間絶縁層20およびバリア層、さらにウエハ全面から放出されるガス量を極力少なくすることができる。その結果、バリア層とアルミニウム層36との界面に吸着する、カバレッジ性や密着性に有害なガスの影響を防ぐことができる。

【0056】この冷却工程は、同一の構成のチャンバを複数有する、アルミニウム層を成膜するためのスパッタ装置を兼用して行われることが望ましい。例えばスパッタ装置内における水冷機能を有するステージ上に基板を載置して該基板温度を所定温度まで下げることが望ましい。

【0057】図9 (a) は、水冷機能を有するステージを含むスパッタ装置の一例の模式図を、図9 (b) は、ステージの一例の平面図を示す。

【0058】このスパッタ装置は、同一の構成のチャンバ50を複数備えたものである。チャンバ50内に、電極をかねるターゲット51およびステージをかねる電極52を有し、電極52上には冷却される基板 (ウエハ) Wが設置されるように構成されている。チャンバ50には、チャンバ内を減圧状態にするための排気手段60およびアルミニウムをスパッタリングする際にガスをチャンバ内に供給する第1のガス供給路53が設けられている。電極52は、ウエハWを電極52上に載置した際に、電極52とウエハWとの間に所定の空間が生じるように、具体的には図9 (b) のように、電極52の上面の外周部分に沿って、突起状の支持部52aが設けられている。さらに、電極52には、第2のガス供給路54が接続されている。そして、熱伝導媒体としてのガス、たとえばアルゴンガスは、第2のガス供給路54から、電極52とウエハWとの間の空間に供給される。また、電極52は、ウエハWを冷却するための冷却システムの役割も兼務している。電極52は、冷媒供給路56から供給される冷媒、たとえば水の還流により一定温度に調節される。電極52の上面は、たとえば図9 (b) に示すように、前記空間に均一にガスを供給させるため、所定のパターンで溝58が形成され、溝が交差する部分に第2のガス供給路54の吹き出し口54aが設けられている。

【0059】上記のスパッタ装置は、例えば以下のよう

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に動作して、ウエハを冷却する。

【0060】チャンバ50内を排気手段60により6×10^{-6}Pa以下の減圧状態として、電極52の支持部52a上にウエハWを載置する。電極52とウエハW間の熱伝導媒体としての役割を果たすガスを、第2のガス供給路54から、電極52とウエハWとの間の空間に導入し、該空間の圧力を600～1000Paに保ち、かつ、該空間からチャンバ内に漏出したガスを排気手段60で排気しながら、ウエハWを冷却する。

【0061】(アルミニウム層の成膜)まず、図6に示すように、200℃以下、より好ましくは30～100℃の温度で、0.2～1.0重量%の銅を含むアルミニウムを膜厚150～300nmでスパッタによって高速度で成膜し、第1のアルミニウム層36aが形成される。この成膜工程では、ターゲットとウエハとの距離は40～200mmに設定されることが望ましい。続いて、同一チャンバ内で基板温度350～460℃に加熱して、同様に銅を含むアルミニウムをスパッタにより低速度で成膜し、膜厚300～600nmの第2のアルミニウム層36bが形成される。この成膜工程では、ターゲットとウエハとの距離は40～200mmに設定されることが望ましい。ここで、アルミニウム層36の成膜において、「高速度」とは、成膜条件や製造されるデバイスの設計事項によって一概に規定できないが、おおよそ10nm/秒以上のスパッタ速度を意味し、「低速度」とは、おおよそ3nm/秒以下のスパッタ速度を意味する。

【0062】アルミニウムのスパッタは、前述のウエハの冷却の際に用いられた、図9に示すスパッタ装置内で行われることが望ましい。このように、減圧状態が保たれた同一の装置内で冷却工程およびアルミニウムの成膜の工程を行うことにより、基板の移動および設置の工程の減少が図られ、その結果、工程の簡便化および基板の汚染を防止することができる。

【0063】ここで、図9に示すスパッタ装置においては、第1のガス供給路53および第2のガス供給路54からは、いずれもアルゴンガスが供給される。そして、アルミニウム層の成膜時の温度は、第2のガス供給路54から供給されるガスによって制御されたウエハWの温度(基板温度)を意味する。

【0064】例えば、ウエハの温度制御は以下のように行われる。まず、ステージ52の温度は、予め、第2のアルミニウム層36bを形成するための温度(350～500℃)に設定されている。第1のアルミニウム層を形成する際には、第2のガス供給路54からのガスの供給はなく、基板温度はステージ52による加熱によって、徐々に上昇する。第2のアルミニウム層を形成する際には、第2のガス供給路54を介して加熱されたガスが供給されることによって基板温度は急激に上昇し、所定の温度で一定になるように制御される。

【0065】同一チャンバ内で第1のアルミニウム層36aおよび第2のアルミニウム層36bを連続的に成膜することにより、温度およびパワーの制御を厳密に行うことができ、従来よりも低温でかつ安定したアルミニウム層を効率よく形成することが可能となる。

【0066】前記第1のアルミニウム層36aの膜厚は、良好なステップカバレッジで連続層を形成することができること、並びに該アルミニウム層34より下層のバリア層および層間絶縁層20からのガス化成分の放出を抑制できることなどを考慮して、適正な範囲が選択され、例えば200～400nmが望ましい。また、第2のアルミニウム層36bは、スルーホールの大きさ並びにそのアスペクト比などによって決定され、例えばアスペクト比が3程度で口径が0.5μm以下のホールを埋めるためには、300～1000nmの膜厚が必要である。

【0067】(反射防止膜の成膜)さらに、別のスパッタチャンバで、スパッタにより窒化チタンを堆積することにより、膜厚30～80nmの反射防止膜37が形成される。その後、Cl_2とBCl_3のガスを主体とする異方性ドライエッチャーで前記バリア層、アルミニウム層36および反射防止膜37からなる堆積層を選択的にエッチングして、金属配線層40のパターニングを行う。

【0068】このようにして形成された金属配線層40では、アスペクト比が0.5～3で、口径が0.2～0.8μmのスルーホール内において、ボイドを発生させることなく良好なステップカバレッジでアルミニウムが埋め込まれることが確認された。

【0069】(実験例)

(a)透過型電子顕微鏡(TEM)による膜構造の解析

前述した方法によって図6および図7に示す構造のサンプルとしての半導体装置を形成し、コンタクト部を含む領域の断面の電子顕微鏡写真を撮影した。この実験で使用したサンプルは、以下のようにして形成されたものである。

【0070】まず、図1～図6に示すように、前述した方法で素子が形成されたシリコン基板11上に層間絶縁層20を形成した後、口径が0.3μm、アスペクト比4のスルーホールを形成した。続いて、ターゲットとウエハとの距離を300mmに設定した、超ロングスロースパッタ装置を用い、4×10^{-2}Pa、250℃の条件下で、チタンを70nmの膜厚で成膜した。このとき、スルーホールの底部には約25nmのチタン層が形成され、スルーホール上端におけるチタン層のせり出しもほとんどなかった。次いで 400℃で20分間にわたり、100%の水素雰囲気中でウエハをアニール処理した。その後、ウエハを大気中に置いた 次いで、常圧の窒素雰囲気中で、800℃で30秒間にわたってランプアニールを行った。次いで、常圧のアルゴンガス雰囲気中で、460℃で脱ガス処理を行い、さらにウェッティ

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ング層として１００ｎｍのチタン層を形成した。その後、ターゲットとウエハとの距離を３００ｍｍに設定したチャンバ内で、Ａｌ－Ｃｕ合金を常温で３００ｎｍの膜厚で形成した。続いて、ターゲットとウエハとの距離を１７０ｍｍに設定したチャンバ内で、Ａｌ－Ｃｕ合金を３００ｎｍの膜厚で形成した。さらに、反射防止膜として窒化チタン層を約３０ｎｍの膜厚で形成した。

【００７１】このようにして得られたサンプルの透過型電子顕微鏡により得られた写真をもとに得られた、コンタクト部の各膜の組成および膜厚は、およそ以下のようであった。

【００７２】

シリコン基板（Ｓｉ）	
チタンシリサイド層（$TiSi_2$）	７５ｎｍ
第１の酸化チタン層（TiO_2）	１０ｎｍ
窒化チタン層（Ti_2N）	２５ｎｍ
第２の酸化チタン層（TiO_2）	１０ｎｍ
アルミニウム－チタン層（Al_3Ti）	１５０ｎｍ
アルミニウム－銅層（Ａｌ－Ｃｕ）	

また、第１および第２の酸化チタン層は、アモルファス構造を有することが確認された。

【００７３】ウェッテング層を構成するチタンはアルミニウムと反応してAl_3Ti系の合金となり、この層上にアルミニウム（Ａｌ－Ｃｕ）膜が形成される。そして、バリア層は、Al_3Ti系の合金とも反応せず、安定で優れたバリア性と導電性を備えていることが確認された。

【００７４】（ｂ）オージェ電子分光法による解析

図８は、オージェ電子分光法による測定結果を示す。図８の横軸はスパッタ時間（分）を示し、縦軸はオージェ電子強度を示す。図８は、シリコン基板およびバリア層の領域を示している。図８から、シリコン基板とバリア層との境界領域に、およびバリア層の表面付近に、それぞれ酸素のピークＰ１およびＰ２が確認された。このことからも、第１のシリコン酸化層および第２のシリコン酸化層の存在が確認された。また、酸素のピークＰ１およびＰ２の間に窒化チタンのピークＰ３があることが確認された。

【００７５】（ｃ）バリア性

本発明のサンプルと、バリア層に酸化シリコン層が存在しない他は本発明のサンプルと同じ比較用サンプルとについて、サンプルに熱処理を施すことによるリーク特性について調べた。リーク特性は、サンプルを種々の条件でアニール処理し、コンタクト部でリーク電流が発生したときのアニール条件を求めた。

【００７６】その結果、本発明に係るサンプルでは、４５０℃で２時間にわたるアニール処理でもリーク電流の発生、およびアルミニウムがバリア層を突き抜けてシリコン基板に進入するスパイク現象の発生がなかった。これに対し、比較用サンプルにおいては、４５０℃で２時間のアニール処理でリーク電流の発生が確認された。

【００７７】このことから、本発明のサンプルは比較用サンプルに比べ、バリア性が格段に優れていることが確認された。

【００７８】このように、本発明の半導体装置によれば、バリア層に該バリア層を構成する金属酸化物層を含むことにより、バリア層の導電性を確保しながら優れたバリア性を有することが確認された。

【００７９】上記実施の形態では、バリア層と基板との接合部がバリア層－シリコン層の場合を説明したが、この接合部はシリコン層の代わりにチタンシリサイド層やコバルトシリサイド層のようなシリサイド層であってもよい。また、バリア層を形成するための金属層は、スパッタ法の代わりにＣＶＤ法で形成されてもよい。また、配線層は、アルミニウム合金の代わりに例えば銅を用いてもよい。特に、銅がメッキされた配線層では、配線層とバリア層との高い密着性およびバリア層の高いバリア性が要求され、バリア層として十分な材料が少ないが、本発明によればこのような銅の配線層にも適用できる。

【００８０】なお、上記実施の形態では、Ｎチャネル型ＭＯＳ素子を含む半導体装置について説明したが、Ｐチャネル型あるいはＣＭＯＳ型素子などを含む半導体装置にも適用することができる。

【図面の簡単な説明】

【図１】本発明の半導体装置の製造方法の一工程を模式的に示す断面図である。

【図２】図１に示す工程に引き続いて行なわれる半導体装置の製造方法の工程を模式的に示す断面図である。

【図３】図２に示す工程に引き続いて行なわれる半導体装置の製造方法の工程を模式的に示す断面図である。

【図４】図３に示す工程に引き続いて行なわれる半導体装置の製造方法の工程を模式的に示す断面図である。

【図５】図４に示す工程に引き続いて行なわれる半導体装置の製造方法の工程を模式的に記す断面図である。

【図６】図５に示す工程に引き続いて行なわれる半導体装置の製造方法の工程を模式的に示す断面図である。

【図７】本発明の半導体装置の要部を拡大して示す断面図である。

【図８】本発明の半導体装置のサンプルについて求めたＳＩＭＳの結果を示す図である。

【図９】（ａ）は、本発明の半導体の製造方法に用いられるスパッタ装置の一例を模式的に示す図であり、（ｂ）は、スパッタ装置のステージの一例を示す図であ

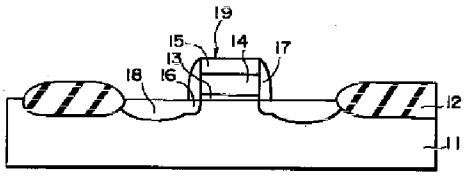
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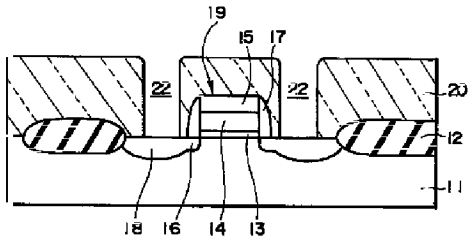
【符号の説明】

１１　シリコン基板
１２　フィールド絶縁層
１３　ゲート酸化層
１６　低濃度不純物層
１８　高濃度不純物層
１７　側壁スペーサ
１９　ゲート電極
２０　層間絶縁層
２２　スルーホール
３０　第１の金属酸化物層（酸化チタン層）
３１　金属シリサイド層（チタンシリサイド層）
３３　金属窒化物層（窒化チタン層）
３４　第２の金属酸化物層（酸化チタン層）
３６　アルミニウム層
３６ａ　第１のアルミニウム層
３６ｂ　第２のアルミニウム層
４０　金属配線層

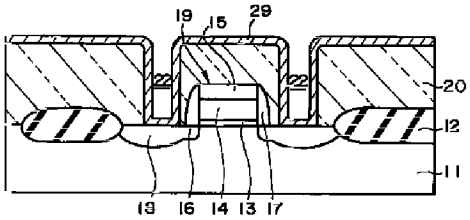
【図１】



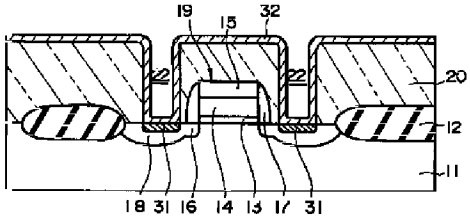
【図２】



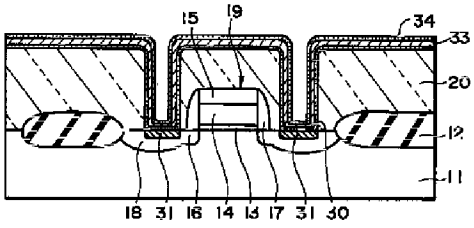
【図３】



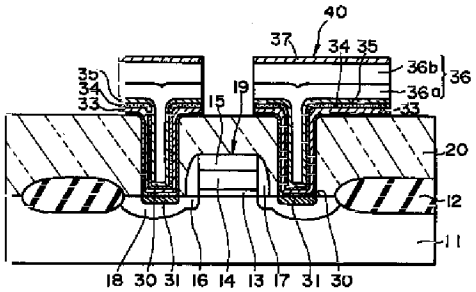
【図４】



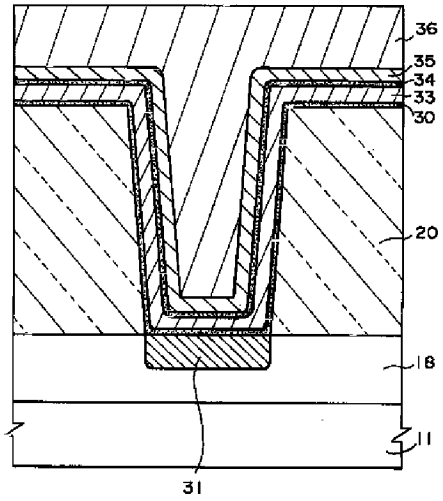
【図５】



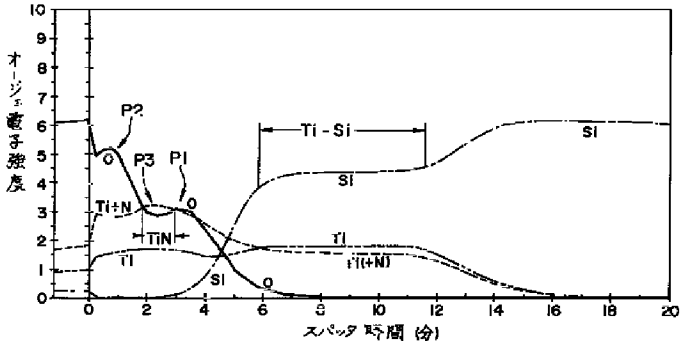
【図６】



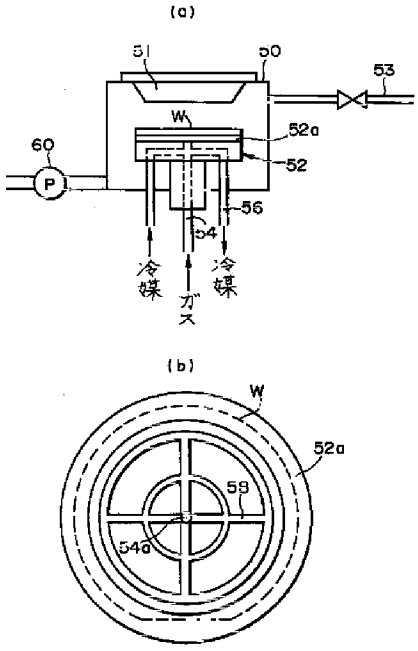
【図7】



【図8】



【図9】



フロントページの続き

(72)発明者　守屋　直弘
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内
(72)発明者　鈴木　英司
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内

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HH34 HH35 JJ01 JJ08 JJ09
JJ11 JJ15 JJ17 JJ18 JJ19
JJ20 JJ32 JJ33 JJ34 JJ35
KK01 KK25 KK26 KK27 KK28
KK29 KK30 LL07 MM08 MM13
NN06 NN07 PP06 PP15 PP18
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QQ13 QQ16 QQ37 QQ70 QQ73
QQ74 QQ75 QQ78 QQ82 QQ85
QQ88 QQ89 QQ91 RR04 RR09
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SS11 SS15 WW02 WW03 XX01
XX02 XX13

Espacenet

JP2000195954A SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Applicants: SEIKO EPSON CORP

Inventors: ASAHINA MICHIO,MATSUMOTO KAZUMI,MORIYA NAOHIRO,SUZUKI EIJI

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SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Abstract

PROBLEM TO BE SOLVED: To provide a semiconductor device which has a barrier layer superior in barrier property and its manufacture. SOLUTION: A semiconductor device has a semiconductor substrate 11 which includes an element, interlayer insulating layers (silicon oxide layer and a BPSG layer) made on the semiconductor substrate 11, a through-hole made in the interlayer insulating layer, a barrier layer made on the interlayer insulating layer and the through-hole, and a wiring layer made on the barrier layer. The barrier layer has a first metal oxide layer (titanium oxide layer) 30 consisting of the oxide of the metal constituting the barrier layer, a metal nitride layer (titanium nitride layer) 33 consisting of the nitride of the metal constituting the barrier layer, and a second metal oxide layer (titanium oxide layer) 34 which consists of the oxide of the metal constituting the barrier layer.

JP2000195954A SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

The EPO does not accept responsibility for the accuracy of data originating from authorities other than the EPO, nor does it guarantee that such data is complete, up-to-date or fit for specific purposes.

[0001] BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device and a manufacturing method thereof, and more particularly to a semiconductor device having excellent barrier properties in a miniaturized contact portion and a manufacturing method thereof.

[0002] 2. Description of the Related Art With the miniaturization, high density, and multi-layering of LSI elements, a technique for embedding a wiring material in a fine through hole having a high aspect ratio has become an important issue. Conventionally, for example, in a contact portion having an aperture size of 0.5 μm or less and an aspect ratio of 2 or more, a tungsten plug is inserted into the through hole to close the through hole and the reaction between aluminum of the wiring layer and silicon of the silicon substrate Is preventing. However, this contact structure has problems such as high electrical resistance of tungsten, easy deterioration of electromigration resistance, and reduced yield resulting from complicated processes. Therefore, introduction of a technique for embedding aluminum into a through hole, which has a low electrical resistance and does not require a complicated embedding process like a tungsten plug, has been studied.

[0003] However, in the contact portion using aluminum, it is necessary to completely take measures against junction leakage due to the reaction between aluminum and silicon of the silicon substrate, and the barrier layer is required to have high barrier properties.

[0004] As the barrier layer, for example, a nitride layer of a refractory metal such as titanium nitride formed by a reactive sputtering method in a nitrogen atmosphere is used. Such a barrier layer has the following problems.

[0005] The titanium nitride layer formed by reactive sputtering in a nitrogen atmosphere has insufficient coverage, so the coverage at the bottom of a fine and high aspect ratio through hole is not sufficient.

[0006] A titanium nitride layer formed by a reactive sputtering method in a nitrogen atmosphere is susceptible to microcracks because the film stress is large, and as a result, the aluminum of the wiring material diffuses and junction leakage is likely to occur.

[0007] Since the titanium nitride layer formed by reactive sputtering in a nitrogen atmosphere is a columnar crystal, aluminum is likely to diffuse through the grain boundary and cause junction leakage.

[0008] Although the <111> orientation of the aluminum layer is determined by the orientation of the columnar crystal titanium nitride layer, since the crystal orientation of the titanium nitride is not necessarily uniform, the difference in the plane orientation of the <111> orientation of the aluminum layer Surface roughening occurs and alignment of this aluminum layer by photolithography becomes difficult.

[0009] Furthermore, the titanium nitride layer formed by reactive sputtering in a nitrogen atmosphere may cause delamination during film formation due to the film stress, and it is easy to generate particles. A short circuit occurs, causing a decrease in yield.

[0010] SUMMARY OF THE INVENTION An object of the present invention is to provide a semiconductor device in which a conductive material is satisfactorily embedded in a fine contact portion of, for example, a half micron or less and has a high barrier property without junction leakage. It is in providing the manufacturing method.

[0011] A semiconductor device according to the present invention includes a semiconductor substrate including elements, an interlayer insulating layer formed on the semiconductor substrate, a through hole formed in the interlayer insulating layer, and the interlayer insulation. And a barrier layer formed on the surface of the through hole, and a wiring layer formed on the barrier layer, the barrier layer being a metal oxide composed of an oxide of a metal constituting the barrier layer And a metal nitride layer made of a metal nitride constituting the barrier layer.

[0012] According to this semiconductor device, the barrier layer includes a metal oxide layer in addition to the metal nitride layer, and has excellent barrier properties while ensuring high conductivity.

[0013] The barrier layer includes a first metal oxide layer made of a metal oxide constituting the barrier layer, a metal nitride layer made of a metal nitride constituting the barrier layer, and a metal constituting the barrier layer It is desirable to include a second metal oxide layer made of the above oxide.

[0014] The first and second metal oxide layers constituting the barrier layer are preferably amorphous in order to obtain high barrier properties.

[0015] The first metal oxide layer constituting the barrier layer preferably has a thickness of 5 to 30 nm in consideration of barrier properties and conductivity. Similarly, the thickness of the second metal oxide layer constituting the barrier layer is preferably 5 to 30 nm. These metal oxide layers may be continuous or discontinuous.

[0016] The wiring layer is preferably made of aluminum or an alloy containing aluminum as a main component. As a material for the wiring layer, copper, gold, platinum, or the like can be used in addition to the aluminum or aluminum alloy. Further, if necessary, a tungsten plug may be used as an embedding material for the through hole.

[0017] The semiconductor device according to the present invention includes a step of forming a through hole in an interlayer insulating layer formed on a semiconductor substrate including an element, a step of forming a barrier layer on the surface of the interlayer insulating layer and the through hole, and Forming a wiring layer on the barrier layer, and the step of forming the barrier layer is formed by a manufacturing method including the following steps (a) to (d). (A) forming a metal layer for forming the barrier layer; (b) heat-treating in a hydrogen atmosphere to hydrogenate or occlude the metal layer; and (c) contain oxygen. A step of bringing the metal layer into contact with oxygen in an atmosphere; and (d) a step of forming a metal oxide layer and a metal nitride layer by heat treatment in a nitrogen atmosphere.

[0018] In this manufacturing method, the barrier layer includes a metal oxide layer and a metal nitride layer, and more specifically, the barrier layer is a first oxide composed of a metal oxide constituting the barrier layer. And a second metal oxide layer comprising a metal oxide constituting the barrier layer, and a second metal oxide layer comprising the metal oxide constituting the barrier layer. .

[0019] According to the manufacturing method of the present invention, in the step (a), a single metal layer is formed by a sputtering method, a CVD method or the like, and then a metal nitride layer is formed in the step (d). As compared with the case where the metal nitride layer is directly formed, film formation with good adhesion and coverage at the bottom of the through hole can be performed. In addition, after forming the metal layer in the step (a), in the step (b), the metal layer is hydrogen alloyed or occluded, whereby the silicon of the semiconductor substrate and the metal of the metal layer are subjected to a subsequent heat treatment. The reaction is suppressed to some extent. As a result, the nitridation reaction and oxidation reaction of the metal in step (d) are performed reliably, and the metal nitride layer and the metal oxide layer are formed. It has been confirmed that the presence of the metal oxide layer dramatically improves the barrier property of the barrier layer and ensures the conductivity of the barrier layer.

[0020] The reason why the metal oxide layer is formed of the first and second layers with the metal nitride layer interposed is not necessarily clear, but is considered as follows. That is, oxygen is occluded in the metal layer formed in the step (a), and oxygen is introduced into and in the metal layer by bringing the metal layer and oxygen into contact in the step (c). Then, a part of the first metal oxide layer is formed by the heat treatment in the step (b), and the formation of the first metal oxide layer is further advanced by the heat treatment in the step (d). And a second metal oxide layer is formed.

[0021] In the step (b), the heat treatment is preferably performed at 200 to 800 ° C. in order to sufficiently form a hydrogen alloy or a hydrogen occlusion of the metal layer. Moreover, although the ratio of hydrogen in a hydrogen atmosphere is dependent also on process temperature, it is desirable that it is 1-100%.

[0022] In the step (c), it is desirable that the atmosphere containing oxygen contains at least 10%, preferably 10-30% of oxygen. In this step, oxygen may be in contact with the surface of the metal layer formed into a hydrogen alloy or occluded in the step (b).

[0023] In the step (d), the heat treatment is preferably performed at 600 to 900 ° C. in order to remove hydrogen and perform nitridation and oxidation of the metal layer. And in the said process (d), although the pressure of atmosphere is not specifically limited, It is desirable that it is a normal pressure.

[0024] The metal for forming the barrier layer preferably contains at least one selected from titanium, cobalt, ruthenium, molybdenum, hafnium, niobium, vanadium, tantalum, and tungsten in consideration of barrier properties and conductivity.

[0025] The metal layer for forming the barrier layer preferably has a thickness of 50 to 150 nm in consideration of the thickness of the metal nitride layer and metal oxide layer formed in the subsequent steps.

[0026] 1 to 6 show a method of manufacturing a semiconductor device according to the present invention, and FIG. 7 is a schematic cross-sectional view for explaining an embodiment of the semiconductor device.

[0027] Below, an example of the manufacturing method of a semiconductor device is shown.

[0028] (Formation of Element) First, as shown in FIG. 1, a MOS element is formed on the silicon substrate 11 by a generally used method. Specifically, for example, the field insulating layer 12 is formed on the silicon substrate 11 by selective oxidation, and the gate oxide layer 13 is formed in the active region. After adjusting the threshold voltage by channel implantation, a tungsten silicide layer 15 is sputtered on the polysilicon layer 14 grown by thermally decomposing monosilane (SiH 4), and further etched into a predetermined pattern to obtain a gate. An electrode 19 is formed.

[0029] Next, phosphorus is ion-implanted to form the low concentration impurity layer 16 in the source region or the drain region. Next, after a sidewall spacer 17 made of a silicon oxide film is formed on the side of the gate electrode 19, arsenic ions are implanted and impurities are activated by an annealing process using a halogen lamp to thereby form a source region or a drain region. The high concentration impurity layer 18 is formed.

[0030] (Formation of Interlayer Insulating Layer) Next, as shown in FIG. 2, as a base layer of the interlayer insulating layer 20, first, tetraethoxylane (TEOS) and oxygen are reacted with each other by plasma reaction so that the film thickness is 100 to 200 nm. A silicon oxide layer (not shown) is formed. This silicon oxide layer is dense and has no insulating property, is more insulating than a film grown from SiH4, and has a slower etching rate with respect to an aqueous solution of hydrogen fluoride.

[0031] Next, as a planarization layer of the interlayer insulating layer 20, a gas phase reaction is performed on the silicon oxide layer with a gas containing silane compound such as SiH4 or TEOS, oxygen, ozone, etc., and phosphorus and boron. A BPSG layer (not shown) having a film thickness of several hundred nm to 1 μm is formed. Thereafter, annealing is performed at 800 to 900 ° C. in a nitrogen atmosphere, and planarization is performed by high-temperature flow. In addition, instead of performing the high-temperature flow of the BPSG layer, planarization can be performed using a generally used SOG film.

[0032] Further, instead of the BPSG layer, a silicon compound and hydrogen peroxide described in a patent application (for example, Japanese Patent Application No. 9-314518) filed by the applicant of the present application are reacted by chemical vapor deposition. A silicon oxide layer may be used. This silicon oxide layer itself has high fluidity and excellent self-planarization characteristics. The mechanism is that when a silicon compound and hydrogen peroxide are reacted by chemical vapor deposition, silanol is formed in the gas phase, and this silanol is deposited on the wafer surface to form a highly fluid film. It is thought that.

[0033] Examples of the silicon compound include inorganic silane compounds such as monosilane, disilane, SiH2Cl2, and SiF4, and organic silane compounds such as CH3SiH3, tripropylsilane, and tetraethoxysilane.

[0034] Further, the silicon oxide layer forming step is performed at a temperature of 0 to 20 ° C. when the silicon compound is an inorganic silicon compound, and at 100 to 150 ° C. when the silicon compound is an organic silicon compound. It is desirable to carry out by a low pressure chemical vapor deposition method under the following temperature conditions.

[0035] (Formation of Through Hole) Next, as shown in FIG. 2, a BPSG layer (planarization layer) and a silicon oxide layer (base layer) constituting the interlayer insulating layer 20 with a reactive ion etcher mainly containing CHF3 and CF4.) Is selectively anisotropically etched to form a through hole 22 having a diameter of 0.2 to 0.5 μm and an aspect ratio of 2 to 5.

[0036] (Barrier layer formation) (a) Formation of metal layer First, as shown in FIG. 3, the distance between the target and the wafer is 150 to 320 mm, and the interlayer insulating layer 20 and the through-hole 22 are formed.

A titanium layer 29 having a thickness of 50 to 150 nm is formed on the surface. The thickness of the titanium layer 29 at the bottom of the through hole 22 is approximately 15 to 80 nm, the coverage of the titanium layer 29 at the through hole 22 is good, and there is almost no protrusion at the top of the through hole. In this way, the titanium layer 29 is formed by ultra-long throw sputtering, and the pinch-off in which the metal constituting the wetting layer reacts with the aluminum constituting the buried layer at the upper part of the through-hole to block the through-hole. Less likely to cause a phenomenon.

[0037] As a metal for forming the barrier layer, cobalt, ruthenium, molybdenum, hafnium, niobium, tantalum, tungsten, or the like can be used in addition to titanium.

[0038] (B) Heat treatment in a hydrogen atmosphere Next, the wafer is annealed in a 100% hydrogen atmosphere at 200 to 800 ° C. for 20 to 60 minutes. In this step, the titanium layer 29 is hydrogen alloyed or hydrogen occluded. That is, taking the case of titanium as an example, as shown in FIG. 4, by annealing for 20 minutes at 400 ° C., for example, 10 atomic% or more of hydrogen is occluded in the titanium layer, and the TiHX alloy layer 32 is formed. In the boundary region with the silicon substrate 11, the reaction between titanium and silicon occurs, and the titanium silicide layer 31 is formed. Further, an oxygen rich layer containing oxygen is formed on the outermost surface of the titanium layer 29.

[0039] In this step (b), the reaction between the silicon of the semiconductor substrate and titanium constituting the metal layer is suppressed to some extent by annealing the metal layer by hydrogen alloying or hydrogen occlusion. As a result, the nitridation reaction and oxidation reaction of the metal in the subsequent step (d) are performed reliably, and the metal nitride layer and the metal oxide layer are formed.

[0040] (C) Next, the TiHx alloy layer 32 and oxygen are brought into contact with each other by placing the wafer in an atmosphere containing oxygen, for example, in the air. By this step, oxygen is adsorbed on the surface of the TiHx alloy layer 32.

[0041] In this step, instead of placing the wafer in the atmosphere, it may be present in an atmosphere containing oxygen at a concentration of 10 to 30% by volume.

[0042] (D) Next, metal nitridation, silicidation, and oxidation are further performed by performing heat treatment by lamp annealing at 600 to 800 ° C. for 10 to 60 seconds in a nitrogen atmosphere at normal pressure. In this step, hydrogen in the TiHx alloy layer 32 is almost desorbed, and as shown in FIG. 5, a titanium nitride layer 33 due to the reaction between titanium and nitrogen, and a titanium silicide layer 31 due to the reaction between titanium and silicon on the silicon substrate 11. And are formed. At the same time, as shown in an enlarged view in FIG. 7, the first titanium oxide layer (first metal oxide layer) 30 is formed in the boundary region between the titanium silicide layer 31 and the titanium nitride layer 33. A second titanium oxide layer (second metal oxide layer) 34 is formed on the surface. It was confirmed that the first titanium oxide layer (first metal oxide layer) 30 was in an amorphous state. Further, it was confirmed that the second titanium oxide layer 34 was discontinuously formed on the surface of the titanium nitride layer 33 and was in an amorphous state.

[0043] The first titanium oxide layer constituting the barrier layer preferably has a thickness of 5 to 30 nm in consideration of barrier properties and conductivity. Similarly, the thickness of the second titanium oxide layer constituting the barrier layer is desirably 5 to 30 nm.

[0044] Due to the first and second titanium oxide layers 30 and 34, the barrier layer has an excellent barrier function. Further, by controlling the film thickness of the first and second titanium oxide layers 30 and 34, the temperature of lamp annealing, etc., the conductivity in the barrier layer is sufficiently ensured.

[0045] Through the above steps, the barrier layer includes at least the first titanium oxide layer 30, the titanium nitride layer 33, and the second titanium oxide layer.

[0046] After the steps (a) to (d), oxygen plasma treatment can be performed as necessary. This oxygen plasma treatment is performed in an oxygen plasma at a pressure of 0.1 × 10 2 to 1.5 × 10 2 Pa for 10 to 100 seconds, and then annealed in a nitrogen or hydrogen atmosphere at 450 to 700 ° C. for 10 to 60 minutes. Is done. By this oxygen plasma treatment, titanium oxide can be formed in an island shape in the titanium nitride layer of the barrier layer. It has been confirmed that the barrier property of the barrier layer can be further improved by this treatment.

[0047] In addition, as a method of forming titanium oxide in an island shape in the barrier layer, it can be performed by a heat treatment at 400 to 800 ° C. in a lamp annealing furnace containing at least several hundred ppm to several percent oxygen. The barrier property can be further improved.

[0048] (Degassing process) Next, the heat treatment including the degassing process will be described.

[0049] First, lamp heating (heat treatment A) is performed in a lamp chamber at a base pressure of 1.5×10^{-4} Pa or less and a temperature of 150 to 250 ° C. for 30 to 60 seconds. Next, argon gas is introduced at a pressure of 1×10^{-1} to 15×10^{-1} Pa in another chamber, and a heat treatment (degassing step; heat treatment B) is performed at a temperature of 300 to 550 ° C. for 30 to 120 seconds. Thus, degassing treatment is performed.

[0050] In this step, first, in the heat treatment A, moisture or the like adhering to the wafer can be removed mainly by heat-treating the entire wafer including the back and side surfaces of the wafer.

[0051] Further, in the heat treatment B, gasification components (oxygen, hydrogen, water, nitrogen) in the planarizing layer such as the BPSG layer constituting the interlayer insulating layer 20 can be mainly removed. As a result, generation of gasification components from the BPSG layer can be prevented during the formation of the aluminum film in the next step.

[0052] Since the barrier layer dissolves several tens atomic percent of gasified components (oxygen, hydrogen, water, nitrogen), it is possible to remove the gasified components in the interlayer insulating layer 20 after the formation of the barrier layer. It is extremely effective for forming an aluminum film in the hole satisfactorily. If the gasification component in the planarization layer below the barrier layer is not sufficiently removed, the gasification component in the planarization layer is released at the temperature at which the barrier layer is formed (usually 300 ° C. or higher). This gas is taken into the barrier layer. Furthermore, since this gas is detached from the barrier layer and formed at the interface between the barrier layer and the aluminum film when the aluminum film is formed, the adhesion and fluidity of the aluminum film may be adversely affected.

[0053] (Formation of Wetting Layer) Further, if necessary, a metal such as titanium, niobium or tungsten is formed at a film thickness of 20 to 50 nm at room temperature to form the wetting layer 35.

[0054] (Heat treatment and wafer cooling before forming aluminum layer) First, before cooling the wafer, in the lamp chamber, a base pressure of 1.5×10^{-4} Pa or less and a temperature of 150 to 250 ° C. A heat treatment for 60 seconds (heat treatment C) is performed to remove substances such as water adhering to the substrate. Thereafter, before forming the aluminum layer, the substrate temperature is lowered to 100 ° C. or lower, preferably from room temperature to 50 ° C. This cooling step is important for lowering the substrate temperature raised by the heat treatment C. For example, a wafer is placed on a stage having a water cooling function to lower the wafer temperature to a predetermined temperature.

[0055] By cooling the wafer in this way, when the first aluminum layer is formed, the amount of gas released from the interlayer insulating layer 20 and the barrier layer and from the entire wafer surface can be reduced as much as possible. As a result, it is possible to prevent the influence of gas that is adsorbed on the interface between the barrier layer and the aluminum layer 36 and is harmful to coverage and adhesion.

[0056] It is desirable that this cooling step be performed using a sputtering apparatus for forming an aluminum layer, which has a plurality of chambers having the same configuration. For example, it is desirable to place the substrate on a stage having a water cooling function in the sputtering apparatus and lower the substrate temperature to a predetermined temperature.

[0057] FIG. 9A shows a schematic diagram of an example of a sputtering apparatus including a stage having a water cooling function, and FIG. 9B shows a plan view of an example of the stage.

[0058] This sputtering apparatus includes a plurality of chambers 50 having the same configuration. The chamber 50 includes a target 51 serving as an electrode and an electrode 52 serving as a stage, and a substrate (wafer) W to be cooled is installed on the electrode 52. The chamber 50 is provided with an exhaust means 60 for reducing the pressure in the chamber and a first gas supply path 53 for supplying gas into the chamber when sputtering aluminum. The electrode 52 is formed so that a predetermined space is created between the electrode 52 and the wafer W when the wafer W is placed on the electrode 52, specifically, as shown in FIG. Protruding support portions 52a are provided along the outer peripheral portion of the upper surface. Further, a second gas supply path 54 is connected to the electrode 52. A gas as a heat conduction medium, for example, argon gas, is

supplied to the space between the electrode 52 and the wafer W from the second gas supply path 54. The electrode 52 also serves as a cooling system for cooling the wafer W. The electrode 52 is adjusted to a constant temperature by recirculation of a refrigerant, for example, water supplied from the refrigerant supply path 56. For example, as shown in FIG. 9B, the upper surface of the electrode 52 has a groove 58 formed in a predetermined pattern in order to supply gas uniformly to the space, and a second gas supply path at a portion where the groove intersects. 54 outlets 54a are provided.

[0059] The sputtering apparatus operates as follows, for example, to cool the wafer.

[0060] The inside of the chamber 50 is brought into a reduced pressure state of 6×10^{-6} Pa or less by the exhaust means 60, and the wafer W is placed on the support portion 52 a of the electrode 52. A gas serving as a heat transfer medium between the electrode 52 and the wafer W is introduced from the second gas supply path 54 into the space between the electrode 52 and the wafer W, and the pressure in the space is set to 600 to 1000 Pa. The wafer W is cooled while the gas leaked from the space into the chamber is exhausted by the exhaust means 60.

[0061] (Film Formation of Aluminum Layer) First, as shown in FIG. 6, aluminum containing 0.2 to 1.0% by weight of copper at a temperature of 200 ° C. or less, more preferably 30 to 100 ° C. A first aluminum layer 36a is formed by forming a film at a high speed by sputtering at 300 nm. In this film forming process, the distance between the target and the wafer is preferably set to 40 to 200 mm. Subsequently, the substrate temperature is heated to 350 to 460 ° C. in the same chamber, and aluminum containing copper is similarly formed at a low speed by sputtering to form a second aluminum layer 36b having a thickness of 300 to 600 nm. . In this film forming process, the distance between the target and the wafer is preferably set to 40 to 200 mm. Here, in the film formation of the aluminum layer 36, "high speed" cannot be generally defined by the film formation conditions or the design items of the device to be manufactured, but means a sputtering speed of about 10 nm / second or more, "Speed" means a sputtering speed of approximately 3 nm / second or less.

[0062] The aluminum sputtering is preferably performed in the sputtering apparatus shown in FIG. 9 used for cooling the wafer. In this way, by performing the cooling step and the aluminum film forming step in the same apparatus in which the reduced pressure state is maintained, the number of steps for moving and setting the substrate can be reduced. Contamination of the substrate can be prevented.

[0063] Here, in the sputtering apparatus shown in FIG. 9, argon gas is supplied from both the first gas supply path 53 and the second gas supply path 54. The temperature at the time of forming the aluminum layer means the temperature of the wafer W (substrate temperature) controlled by the gas supplied from the second gas supply path 54.

[0064] For example, the temperature control of the wafer is performed as follows. First, the temperature of the stage 52 is set in advance to a temperature (350 to 500 ° C.) for forming the second aluminum layer 36b. When forming the first aluminum layer, no gas is supplied from the second gas supply path 54, and the substrate temperature gradually rises due to heating by the stage 52. When the second aluminum layer is formed, the substrate temperature is rapidly increased by supplying the heated gas through the second gas supply path 54, and is controlled to be constant at a predetermined temperature. Is done.

[0065] By continuously forming the first aluminum layer 36a and the second aluminum layer 36b in the same chamber, the temperature and power can be strictly controlled, and the aluminum layer is stable at a lower temperature than in the past. Can be formed efficiently.

[0066] The film thickness of the first aluminum layer 36a is such that a continuous layer can be formed with good step coverage, and the release of gasification components from the barrier layer below the aluminum layer 34 and the interlayer insulating layer 20 is suppressed. Considering what can be done, an appropriate range is selected, for example, 200 to 400 nm is desirable. The second aluminum layer 36b is determined by the size of the through hole and the aspect ratio thereof. For example, in order to fill a hole having an aspect ratio of about 3 and a diameter of 0.5 μm or less, a film of 300 to 1000 nm is used. Thickness is necessary.

[0067] (Formation of Antireflection Film) Further, titanium nitride is deposited by sputtering in another sputtering chamber, whereby an antireflection film 37 having a thickness of 30 to 80 nm is formed. Thereafter, the metal wiring layer 40 is patterned by selectively etching the deposited layer composed of the barrier layer, the aluminum layer 36 and the antireflection film 37 with an anisotropic dry etcher mainly composed of Cl2 and BCl3 gases.

[0068] In the metal wiring layer 40 formed in this way, aluminum has good step coverage without generating voids in a through hole having an aspect ratio of 0.5 to 3 and a diameter of 0.2 to 0.8 μm. Has been confirmed to be embedded.

[0069] (Experimental example) (a) Analysis of film structure by transmission electron microscope (TEM) A semiconductor device as a sample having the structure shown in FIGS. 6 and 7 is formed by the above-described method, and electrons in a cross section of a region including a contact portion are formed. A photomicrograph was taken. The sample used in this experiment was formed as follows.

[0070] First, as shown in FIGS. 1 to 6, after the interlayer insulating layer 20 was formed on the silicon substrate 11 on which the elements were formed by the above-described method, a through hole having a diameter of 0.3 μm and an aspect ratio of 4 was formed. . Subsequently, titanium was formed to a thickness of 70 nm under the conditions of 4×10^{-2} Pa and 250 ° C. using an ultra long throw sputtering apparatus in which the distance between the target and the wafer was set to 300 mm. At this time, a titanium layer of about 25 nm was formed at the bottom of the through hole, and there was almost no protrusion of the titanium layer at the upper end of the through hole. The wafer was then annealed at 100 ° C. for 20 minutes in a 100% hydrogen atmosphere. Thereafter, the wafer was placed in the atmosphere. Next, lamp annealing was performed at 800 ° C. for 30 seconds in a normal pressure nitrogen atmosphere. Next, degassing treatment was performed at 460 ° C. in an atmospheric pressure argon gas atmosphere, and a titanium layer of 100 nm was formed as a wetting layer. Thereafter, an Al—Cu alloy was formed with a film thickness of 300 nm at room temperature in a chamber in which the distance between the target and the wafer was set to 300 mm. Subsequently, an Al—Cu alloy with a film thickness of 300 nm was formed in a chamber in which the distance between the target and the wafer was set to 170 mm. Further, a titanium nitride layer having a thickness of about 30 nm was formed as an antireflection film.

[0071] The composition and film thickness of each film of the contact portion obtained based on the photograph obtained by the transmission electron microscope of the sample thus obtained were as follows.

[0072] Silicon substrate (Si) Titanium silicide layer (TiSi2) 75 nm First titanium oxide layer (TiO2) 10 nm Titanium nitride layer (Ti2N) 25 nm Second titanium oxide layer (TiO2) 10 nm Aluminum-titanium layer (Al3Ti) 150 nm Aluminum-copper Layer (Al-Cu) Further, it was confirmed that the first and second titanium oxide layers have an amorphous structure.

[0073] Titanium constituting the wetting layer reacts with aluminum to form an Al3Ti alloy, and an aluminum (Al-Cu) film is formed on this layer. It was confirmed that the barrier layer did not react with the Al3Ti alloy and had stable and excellent barrier properties and conductivity.

[0074] (B) Analysis by Auger Electron Spectroscopy FIG. 8 shows the measurement results by Auger electron spectroscopy. The horizontal axis in FIG. 8 indicates the sputtering time (minutes), and the vertical axis indicates the Auger electron intensity. FIG. 8 shows the region of the silicon substrate and the barrier layer. From FIG. 8, oxygen peaks P1 and P2 were confirmed in the boundary region between the silicon substrate and the barrier layer and in the vicinity of the surface of the barrier layer, respectively. This also confirmed the presence of the first silicon oxide layer and the second silicon oxide layer. It was also confirmed that there was a titanium nitride peak P3 between the oxygen peaks P1 and P2.

[0075] (C) Barrier property The leakage characteristics of the sample of the present invention and the comparative sample that was the same as the sample of the present invention except that no silicon oxide layer was present in the barrier layer were examined. For the leak characteristics, the samples were annealed under various conditions, and the annealing conditions when a leak current occurred at the contact portion were determined.

[0076] As a result, in the sample according to the present invention, there was no occurrence of leakage current and no spike phenomenon in which aluminum penetrated the barrier layer and entered the silicon substrate even after annealing at 450 ° C. for 2 hours. On the other hand, in the comparative sample, generation of leakage current was confirmed by annealing at 450 ° C. for 2 hours.

[0077] From this, it was confirmed that the sample of the present invention has much better barrier properties than the comparative sample.

[0078] As described above, according to the semiconductor device of the present invention, it is confirmed that the barrier layer includes the metal oxide layer constituting the barrier layer, thereby having excellent barrier properties while ensuring the conductivity of the barrier layer. It was.

[0079] In the above embodiment, the description has been given of the case where the junction between the barrier layer and the substrate is the barrier layer-silicon layer, but this junction is a silicide layer such as a titanium silicide layer or a cobalt silicide layer instead of the silicon layer. May be. Further, the metal layer for forming the barrier layer may be formed by a CVD method instead of the sputtering method. Further, for example, copper may be used for the wiring layer instead of the aluminum alloy. In particular, in a wiring layer plated with copper, high adhesion between the wiring layer and the barrier layer and high barrier properties of the barrier layer are required, and there are few materials as a barrier layer. It can also be applied to copper wiring layers.

[0080] Although the semiconductor device including an N-channel MOS element has been described in the above embodiment, the present invention can also be applied to a semiconductor device including a P-channel type or a CMOS type element.

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CLAIMS JP2000195954

1.
A semiconductor substrate including an element, an interlayer insulating layer formed on the semiconductor substrate, a through hole formed in the interlayer insulating layer, a barrier layer formed on the surface of the interlayer insulating layer and the through hole, and the barrier A wiring layer formed on the barrier layer, wherein the barrier layer includes a metal oxide layer including an oxide of a metal forming the barrier layer, and a metal nitride including a nitride of a metal forming the barrier layer. A semiconductor device including a physical layer.

2.
2. The barrier layer according to claim 1, wherein the barrier layer is a first metal oxide layer formed of an oxide of a metal forming the barrier layer, a metal nitride layer formed of a nitride of a metal forming the barrier layer, and the barrier. A semiconductor device, comprising: a second metal oxide layer formed of a metal oxide forming the layer.

3.
The semiconductor device according to claim 1, wherein the metal forming the barrier layer includes at least one selected from titanium, cobalt, ruthenium, molybdenum, hafnium, niobium, vanadium, tantalum, and tungsten.

4.
The semiconductor device according to claim 1, wherein the first and second metal oxide layers forming the barrier layer are amorphous.

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5.
The semiconductor device according to claim 1, wherein the first metal oxide layer forming the barrier layer has a thickness of 5 to 30 nm.

6.
The semiconductor device according to claim 1, wherein the second metal oxide layer forming the barrier layer has a thickness of 5 to 30 nm.

7.
7. The semiconductor device according to claim 1, wherein the wiring layer is made of aluminum or an alloy containing aluminum as a main component.

8.

A step of forming a through hole in an interlayer insulating layer formed on a semiconductor substrate including an element, a step of forming a barrier layer on the surface of the interlayer insulating layer and the through hole, and a wiring layer on the barrier layer. A method of manufacturing a semiconductor device, including the step of forming, and the step of forming the barrier layer includes the following steps (a) to (d).

(A) a step of forming a metal layer for forming the barrier layer, (b) a step of heat-treating the metal layer in a hydrogen atmosphere to form a hydrogen alloy or hydrogen storage, (c) containing oxygen A step of contacting the metal layer with oxygen in an atmosphere, and (d) a step of forming a metal oxide layer and a metal nitride layer by heat treatment in a nitrogen atmosphere.

9.
9. The barrier layer according to claim 8, wherein the barrier layer is a first metal oxide layer formed of an oxide of a metal forming the barrier layer, a metal nitride layer formed of a nitride of a metal forming the barrier layer, and the barrier. A method of manufacturing a semiconductor device, comprising: a second metal oxide layer formed of a metal oxide forming a layer.

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10.

10. The method of manufacturing a semiconductor device according to claim 8, wherein in the step (b), the heat treatment is performed at 200 to 800 ° C.

11.

11. The method of manufacturing a semiconductor device according to claim 8, wherein in the step (c), the atmosphere containing oxygen contains at least 10% by volume of oxygen.

12.

12. The method of manufacturing a semiconductor device according to claim 8, wherein the heat treatment is performed at 600 to 900 ° C. in the step (d).

13.

13. The method for manufacturing a semiconductor device according to claim 8, wherein in the step (d), the nitrogen atmosphere is in a normal pressure state.

14.

14. The semiconductor according to claim 8, wherein the metal for forming the barrier layer includes at least one selected from titanium, cobalt, ruthenium, molybdenum, hafnium, niobium, vanadium, tantalum and tungsten. Device manufacturing method.

15.

15. The method of manufacturing a semiconductor device according to claim 8, wherein the metal layer for forming the barrier layer has a film thickness of 50 to 150 nm.

16.

16. The method of manufacturing a semiconductor device according to claim 8, wherein the wiring layer is made of aluminum or an alloy containing aluminum as a main component.

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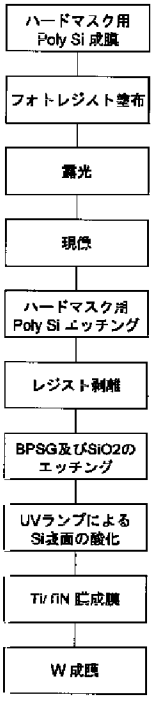
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(71)出願人　390040660
アプライド　マテリアルズ　インコーポレイテッド
ＡＰＰＬＩＥＤ　ＭＡＴＥＲＩＡＬＳ，ＩＮＣＯＲＰＯＲＡＴＥＤ
アメリカ合衆国　カリフォルニア州　95054　サンタ　クララ　バウアーズ　アベニュー　3050
(74)代理人　100088155
弁理士　長谷川　芳樹　（外２名）

最終頁に続く

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】
【課題】　絶縁層を介して半導体と配線との良好な接触を得る半導体製造方法。
【解決手段】　半導体層の上に絶縁層を形成し、絶縁層の一部を、半導体層の表面の一部が露出するまで除去して、半導体層の露出表面を底面とするコンタクトホールを形成し、半導体層の露出表面を加熱して、露出表面の上に半導体の酸化物の膜を形成し、コンタクトホールを金属で埋め込み更に金属が絶縁層の上を覆うように、金属を堆積する。



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【特許請求の範囲】
【請求項１】　半導体層の上に絶縁層を形成し、前記絶縁層の一部を、前記半導体層の表面の一部が露出するまで除去して、前記半導体層の露出表面を底面とするコンタクトホールを形成し、
前記半導体層の前記露出表面を加熱して、前記露出表面に該半導体の酸化物の膜を形成し、
前記コンタクトホールを金属で埋め込み更に金属が前記絶縁層の上を覆うように、金属を堆積する半導体装置の製造方法。
【請求項２】　前記露出表面の加熱が、紫外線ランプの照射により行われる請求項１に記載の半導体装置の製造方法。
【請求項３】　前記露出表面の加熱が、酸素（O_2）又はオゾン（O_3）の雰囲気下で行われる請求項１に記載の半導体装置の製造方法。
【請求項４】　前記露出表面の加熱が１秒間以上行われる請求項１に記載の半導体装置の製造方法。
【請求項５】　前記酸化物の膜の厚さが、０．１～１０ｎｍである請求項１に記載の半導体装置の製造方法。
【請求項６】　前記半導体がシリコンである請求項１～５のいずれかに記載の半導体装置の製造方法。
【請求項７】　前記半導体が、シリコンカーバイド（ＳｉＣ）とゲルマニウムとから成る群より選択される請求項１～５のいずれかに記載の半導体装置の製造方法。
【請求項８】　前記シリコンが、ドープシリコンである請求項６に記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体集積回路等を製造する半導体製造方法に関する。本発明は特に、多層の配線工程を含む半導体製造工程に適する。
【０００２】
【従来の技術】半導体集積回路や薄膜トランジスタ等の作製においては、半導体と絶縁体を交互に積層する構造が多用される。そして、このような積層構造において、絶縁層を介してその下にある半導体と電気的接触を取ろうとする場合は、絶縁層の一部を貫通するエッチングを行ってコンタクトホールを形成し、次いでコンタクトホールを金属膜で埋め込み、その後アニール処理を行う。この場合、一般には絶縁層の上にハードマスクを形成し、次いでエッチングにより所望の場所の絶縁層を除去してコンタクトホールを形成し、次いでコンタクトホールを金属膜で埋め込み、その後アニール処理を行う。
【０００３】金属膜によるコンタクトホールの埋め込みには、スパッタリングが主に使用されてきた。しかし、スパッタリングでは、金属粒子の飛来角の制御が難しく、アスペクト比の高いホールでは埋め込みが不良になる等の問題があった。
【０００４】
【発明が解決しようとする課題】この問題を解決するため、金属膜の成膜に化学気相堆積（ＣＶＤ）を用いようとする試みがある。しかし、ＣＶＤは真空中での成膜ではないため、金属膜の成膜に先立ち半導体表面には半導体の自然酸化物の膜が形成される。例えば、コンタクトホール表面に露出したシリコンの表面には、露出後金属膜形成前に自然シリコン酸化物の膜が形成されてしまう。このような自然酸化物が介在することにより、半導体と金属膜との電気的接触が損なわれるという問題が生じる。これを解決するため、真空中で表面の自然酸化膜を除去する工程を更に行う試みもなされているが、この除去工程において半導体表面にパーティクルが多数付着する等、別の問題が生じてしまう。また、自然酸化物の厚さは制御が困難であるため、接触部分の抵抗の制御が困難になる場合もある。
【０００５】また、金属（メタル）と接触させようとする半導体部分には、通常、リンや砒素等の不純物を導入して、その抵抗を下げているが、形成後の熱処理工程を行う際、半導体のごく表面の不純物の濃度が低下してしまうことがある。このような場合、十分な接触抵抗を得るために高温のアニールを行わなければならなくなるが、このような高温のアニールを行えば、半導体デバイスの性能が損なわれるおそれもある。
【０００６】
【課題を解決するための手段】本発明は、集積度の高い半導体デバイスの多層配線において、絶縁層を介して半導体と配線との良好な接触を得る半導体製造方法を提供することを目的とする。また、本発明は、余分な洗浄工程及びアニール工程を必要としない簡略化された工程により、高い生産性及び歩留まりを実現する半導体製造方法を提供することを目的とする。また、本発明は、比較的低抵抗な半導体に対して、アニール処理を経ずに良好な電気的接触を得ることができる半導体製造方法を提供することを目的とする。本発明の半導体装置の製造方法は、半導体層の上に絶縁層を形成し、絶縁層の一部を、半導体層の表面の一部が露出するまで除去して、半導体層の露出表面を底面とするコンタクトホールを形成し、半導体層の露出表面を加熱して、露出表面の上に半導体の酸化物の膜を形成し、コンタクトホールを金属で埋め込み更に金属が絶縁層の上を覆うように、金属を堆積することを特徴とする。
【０００７】
【発明の実施の形態】本発明に従った典型的な工程は、コンタクトホール形成後に、シリコン露出面を紫外線ランプ（ＵＶランプ）で加熱しシリコン露出面に薄いシリコン酸化膜の層を形成するステップを有している。ここでは、半導体にシリコンを用いる例を代表例として説明を進める。
【０００８】加熱により形成したシリコン酸化物は、自然酸化膜に比べて物理的な緊密性が高く、ポーラスでは

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ない。そのため、この加熱によるシリコン酸化膜の下のシリコンが更に自然酸化物を形成することは妨げられる。すなわち、加熱によりシリコン酸化物層の厚さを極く薄く形成するだけで、それ以上の酸化物の形成を妨げることができる。シリコン酸化物層の厚さは、加熱の時間や加熱に要するエネルギー等を制御することにより、デバイスの用途に応じて制御できる。

【０００９】ここで、以下の説明においては加熱によるシリコン酸化物と自然酸化物の区別のため、自然酸化物を指す場合は「自然酸化物」と明記することとし、その他の「シリコン酸化物」や「酸化膜」等の語には、特に明記した場合を除き自然酸化物を含まないこととする。

【００１０】なお、加熱により形成した酸化物膜の厚さに対しての電流と電圧の関係を、図３に示した。これは、J. Physics, D. Appl. Phys., 45, 9934 (1974), "Studies of tunnel MOS diodes, I, Interface effect in silicon schottky diodes"に記載されているものであり、ＭＩＳトンネルダイオードにおけるシリコン酸化物の厚みに対する電流及び電圧の変化を表すグラフである。シリコン酸化物の厚さｄをパラメータとして、縦軸が電流、横軸が電圧を表している。

【００１１】加熱により形成されるシリコン酸化物の厚さは、トンネル電流により十分低い抵抗を得るような厚さであればよい。具体的には、１～１００オングストローム（０．１～１０ｎｍ）程度あればよく、好ましくは１０～３０オングストローム（１～３ｎｍ）である。

【００１２】このように、本発明によれば、酸化物の厚さを適切な範囲に制御することができるため、アスペクト比の高いコンタクトホールホールに対して有用なＣＶＤにより金属膜を堆積する際、良好な接触抵抗を得ることが可能となる。

【００１３】ここで、加熱により形成したシリコン酸化物の表面は親水性になっており、疎水性のシリコン表面上に比べて微粒子等の付着物の除去性が高いことは一般によく知られている。従って、加熱によりシリコン酸化物膜を形成後そのままの状態で基板を保存しても、さほど問題は生じない。

【００１４】さらに、不純物濃度の低い半導体においては、直に金属を接触させるよりは、絶縁層を介して接触させた方が、より低抵抗な接触が得られる事が一般に知られている。半導体に金属を直に接触させた場合、半導体の表面には多数の界面準位が形成され、これが電気的な障壁となる。これに対し、良好な絶縁層を表面に設けることにより、この障壁は大幅に縮小される。このため、従来は、金属膜の堆積後、半導体基板の合金層を形成するアニール工程が必要となっていた。これに対し、本発明では、このようなアニール工程の必要がなくなる。また、前述のように、不純物をドープした半導体表面は熱を受けることにより表面の不純物が減少する問題があるが、本発明の方法を採用することにより、加熱は短時間で終了するため、不純物の偏析の問題が低減される。

【００１５】次に、プロセスの条件について説明する。

【００１６】シリコン表面の加熱処理には、取扱いの簡便性の点から、ＵＶランプによる加熱を用いることが好ましい。ＵＶランプは、加熱室（チャンバ）の中に設置されても、外に設置されてもよい。

【００１７】また、上述のＵＶランプによる加熱の他、ファーネス内での加熱、スチームによる加熱や、ＲＴＰ(rapid thermal processing)による加熱を用いてもよい。この中で、酸化物膜の表面が滑らかに得られるという点から、ＲＴＰによる加熱が好ましい。

【００１８】加熱中は、基板は酸素を有する雰囲気下に置かれる。この雰囲気は大気でもよいが、酸化反応を促進する点から、酸素（O_2）又はオゾン（O_3）の雰囲気が好ましい。特に、オゾン雰囲気においては、加熱により、酸化物の形成と同時に残留レジストのアッシングも行うことができる。また、酸素又はオゾンの雰囲気は、アルゴンやヘリウム等の不活性ガスや窒素ガス等の希釈ガスを含んでいてもよい。

【００１９】シリコン表面の加熱の時間は、十分な酸化物膜を形成するため、１秒以上、好ましくは５秒以上、更に好ましくは１０秒以上である。但し、この時間は、ＵＶランプの出力や基板とＵＶランプの距離等の操作条件に大きく依存する。また、デバイス自体に影響を与えない範囲であれば、加熱の時間を十分長くとっても問題ない。加熱中の圧力は、１０ミリトール以上、好ましくは１００ミリトール以上であり、大気圧の数倍以下～数十倍程度以下であればよい。

【００２０】本発明が適用可能な半導体は、上述のシリコンの他に、シリコンカーバイド（ＳｉＣ）及びゲルマニウム（Ｇｅ）を挙げることができる。

【００２１】また、半導体がシリコンである場合は、アモルファスシリコンであっても結晶性シリコンであってもよい。また、ノンドープシリコンであってもドープシリコンであってもよい。但し、金属との良好なコンタクトを形成する点から、多少ライトドープとすることが好ましい場合がある。

【００２２】なお、本発明の実施には、様々なタイプの半導体製造装置を用いることが可能である。中央に基板移送用チャンバを備えるクラスタツールタイプの半導体製造システムでもよいし、インラインタイプの半導体製造システムでもよい。

【００２３】

【実施例】以下、添付の図面を参照して、本発明の好ましい実施例について説明する。なお、図面中同一の符号には同一の要素が対応し、重複する説明は省略される。

【００２４】図１は、本発明に従った典型的な工程を示すフローチャートである。図２は、図１に示されるフローチャートに従って処理された半導体基板の断面図であ

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り、図１の工程に対応する基板の変化を示す。本実施例では、クラスタツールタイプの半導体製造システムを用いた。各プロセス間における基板の移送は、クラスタツールの中央部の移送チャンバを介して行われた。

【００２５】図２（ａ）に示すように、先ず、SiO_2層２及びＢＰＳＧ（ホウリン珪酸ガラス）層３が形成されたシリコン基板１に対し、ポリシリコン(Poly Si)のハードマスク４を成膜した。次いで、フォトレジストをハードマスク４の上に塗布し、露光、現像の後、ハードマスク用ポリシリコン４をエッチングし、コンタクトホール形成用のハードマスク４が形成された（図２（ｂ））。

【００２６】次に、フッ素系エッチャントガスを用いて、ＢＰＳＧ層３及びSiO_2層２のハードマスクで保護されない部分をエッチングして、コンタクトホール５を形成した（図２（ｃ））。このとき、コンタクトホール５の底部は、シリコン１が露出している。

【００２７】コンタクトホール５を形成した直後に、移送チャンバを介して真空を破らずに基板を加熱チャンバに移送した。加熱チャンバの内部には、ＵＶランプが設置されており、基板表面にＵＶを照射して表面を加熱できるようになっている。加熱チャンバ内をオゾン（O_3）雰囲気とし、移送されたコンタクトホール形成後の基板の表面をＵＶランプで１０秒程度加熱し、コンタクトホール５の底部のシリコン露出面に、厚さ３０オングストローム程度のシリコン酸化物膜６が形成された（図２（ｄ））。

【００２８】次いで、基板を下地層用のＣＶＤチャンバに移送し、下地層としてＴｉ／ＴｉＮ膜７を熱ＣＶＤにより形成した。次いで、基板をタングステン成膜用のＣＶＤチャンバに移送し、WF_6を原料にブランケットタングステン層８を堆積し、コンタクトホール５を埋め込んだ（図２（ｅ））。なお、本実施例では行わなかったが、ＢＰＳＧ層及びSiO_2層のエッチング工程の後、あるいはＵＶランプによる加熱工程の後、任意、洗浄工程を行ってもよい。また、Ｔｉ／ＴｉＮ膜の形成後に、下地層の濡れ性を高めるためアニールを行ってもよい。

【００２９】

【発明の効果】以上説明したように、本発明によれば、集積度の高い半導体デバイスの多層配線において、絶縁層を介して半導体と配線との良好な接触を得る半導体製造方法が提供される。また、本発明によれば、余分な洗浄工程及びアニール工程を必要としない簡略化された工程により、高い生産性及び歩留まりを実現する半導体製造方法が提供される。また、本発明によれば、比較的低抵抗な半導体に対して、アニール処理を経ずに良好な電気的接触を得ることができる半導体製造方法が提供される。

【図面の簡単な説明】

【図１】本発明の好ましい実施例におけるフローチャートである。

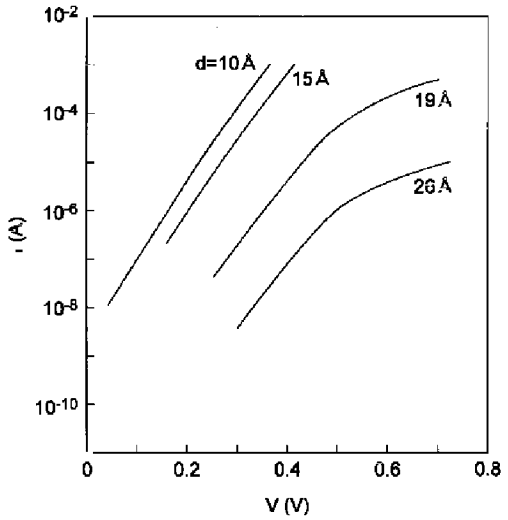
【図２】本発明の好ましい実施例に従って処理された基板の断面図である。

【図３】ＭＩＳトンネルダイオードにおけるシリコン酸化物の厚みに対する電流及び電圧の変化を表すグラフである。

【符号の説明】

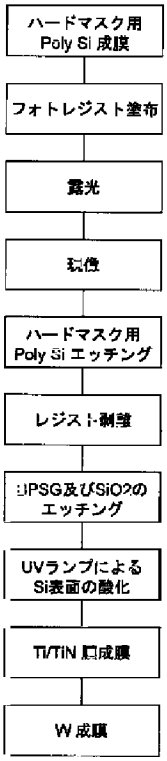
１…Ｓｉ基板、２…ＳｉＯ２、３…ＢＰＳＧ、４…ハードマスク、５…コンタクトホール、６…加熱によるシリコン酸化物層、７…Ｔｉ／ＴｉＮ、８…ブランケットタングステン。

【図３】

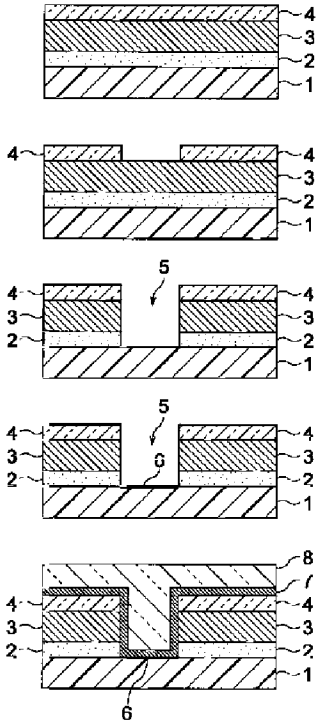


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【図1】



【図2】



フロントページの続き

(72)発明者　広瀬　満
千葉県成田市新泉14－３野毛平工業団地内
アプライド　マテリアルズ　ジャパン
株式会社内

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5F033 GG01 HH18 HH19 HH33 JJ18
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JP2000216241A MANUFACTURE OF SEMICONDUCTOR DEVICE

Applicants: APPLIED MATERIALS INC

Inventors: HIROSE MITSURU

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MANUFACTURE OF SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To provide a good contact between a semiconductor and a wiring by forming an insulating layer on a semiconductor layer, a part of which is removed to form a contact hole, which is filled with a metal, and depositing a metal so that the metal covers the insulating layer. SOLUTION: An SiO2 layer 2 and boron-phosphide silicon glass layer 3 are formed on a silicon substrate 1, and a hard mask 4 of polysilicon is film-formed on the boron-phosphide silicon glass layer 3. A photo-resist is applied on the hard mask 4 which is etched after exposure and development, forming the hard mask 4 for forming a contact hole. Then, such part of the boron-phosphide silicon glass layer 3 and SiO2 layer 2 which is not protected with the hard mask 4 is etched to form a contact hole 5. Over which, a silicon oxide film 6 and Ti/TiN film 7 are formed before a blanket tungsten layer 8 is deposited.

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DESCRIPTION JP2000216241

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor manufacturing method for manufacturing a semiconductor integrated circuit or the like. The present invention is particularly suitable for a semiconductor manufacturing process including a multilayer wiring process.

[0002]

2. Description of the Related Art In the fabrication of semiconductor integrated circuits, thin film transistors and the like, a structure in which semiconductors and insulators are alternately laminated is often used. Then, in such a laminated structure, when an attempt is made to make electrical contact with a semiconductor thereunder through an insulating layer, etching is performed through a part of the insulating layer to form a contact hole, and then a contact hole is formed. The holes are filled with a metal film, and then an annealing process is performed. In this case, generally, a hard mask is formed on the insulating layer, then the insulating layer at a desired place is removed by etching to form a contact hole, then the contact hole is filled with a metal film, and then an annealing treatment is performed.

[0003]

Sputtering has been mainly used for filling contact holes with a metal film. However, in the

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sputtering, it is difficult to control the flying angle of the metal particles, and there is a problem that the filling is defective in the hole having a high aspect ratio.

[0004]

In order to solve this problem, there is an attempt to use chemical vapor deposition (CVD) for forming a metal film. However, since CVD is not a film formation in a vacuum, a film of a natural oxide of a semiconductor is formed on the surface of a semiconductor prior to the formation of a metal film. For example, a natural silicon oxide film is formed on the surface of silicon exposed on the surface of the contact hole after the exposure and before the formation of the metal film. The interposition of such a natural oxide causes a problem that electrical contact between the semiconductor and the metal film is impaired. In order to solve this, an attempt has been made to further perform a step of removing the native oxide film on the surface in a vacuum, but in this removing step, another problem such as a large number of particles adhering to the semiconductor surface occurs. Further, since it is difficult to control the thickness of the natural oxide, it may be difficult to control the resistance of the contact portion.

[0005]

In addition, an impurity such as phosphorus or arsenic is usually introduced into a semiconductor portion to be brought into contact with a metal to reduce its resistance. The concentration of impurities on the surface may decrease. In such a case, it is necessary to perform high-temperature annealing to obtain sufficient contact resistance, but such high-temperature annealing may impair the performance of the semiconductor device.

[0006]

SUMMARY OF THE INVENTION It is an object of the present invention to provide a semiconductor manufacturing method for obtaining good contact between a semiconductor and a wiring through an insulating layer in a multilayer wiring of a semiconductor device having a high degree of integration. .. Another object of the present invention is to provide a semiconductor manufacturing method that realizes high productivity and yield by a simplified process that does not require extra cleaning process and annealing process. It is another object of the present invention to provide a semiconductor manufacturing method capable of obtaining good electrical contact to a semiconductor having a relatively low resistance without performing

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an annealing treatment. A method for manufacturing a semiconductor device of the present invention comprises forming an insulating layer on a semiconductor layer, removing a part of the insulating layer until a part of the surface of the semiconductor layer is exposed, and exposing the exposed surface of the semiconductor layer to a bottom surface. A contact hole is formed, and the exposed surface of the semiconductor layer is heated to form a semiconductor oxide film on the exposed surface. The contact hole is filled with metal, and further the metal covers the insulating layer. , Depositing a metal.

[0007]

BEST MODE FOR CARRYING OUT THE INVENTION A typical process according to the present invention is a step of heating a silicon exposed surface with an ultraviolet lamp (UV lamp) to form a thin silicon oxide film layer on the silicon exposed surface after forming a contact hole. have. Here, the description will proceed with a typical example of using silicon as a semiconductor.

[0008]

The silicon oxide formed by heating has higher physical tightness than a natural oxide film and is not porous. Therefore, the silicon under the silicon oxide film due to this heating is prevented from further forming a native oxide. That is, only by forming the silicon oxide layer to a very small thickness by heating, it is possible to prevent further formation of oxide. The thickness of the silicon oxide layer can be controlled according to the application of the device by controlling the heating time and the energy required for heating.

[0009]

Here, in the following description, in order to distinguish between a silicon oxide and a natural oxide by heating, when referring to a natural oxide, it is designated as "natural oxide", and other "silicon oxide" and "oxidation Unless otherwise specified, the word "membrane" and the like do not include a natural oxide.

[0010]

The relationship between current and voltage with respect to the thickness of the oxide film

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formed by heating is shown in FIG.

This is J. Physics, D. Appl. Phys., 45, 9934 (1974), "Studies of tunnel MOS diodes, I, Interface effect in silicon schottky diodes". Changes in current and voltage with respect to silicon oxide thickness in MIS tunnel diodes. It is a graph showing. With the thickness d of the silicon oxide as a parameter, the vertical axis represents current and the horizontal axis represents voltage.

[0011]

The thickness of the silicon oxide formed by heating may be such that a sufficiently low resistance is obtained by the tunnel current. Specifically, it may be about 1 to 100 Å (0.1 to 10 nm), preferably 10 to 30 Å (1 to 3 nm).

[0012]
As described above, according to the present invention, since the thickness of the oxide can be controlled within an appropriate range, it is possible to obtain a favorable result when depositing a metal film by CVD useful for a contact hole having a high aspect ratio. It is possible to obtain contact resistance.

[0013]

Here, it is generally well known that the surface of the silicon oxide formed by heating is hydrophilic, and that it has a higher removability of deposits such as fine particles than the hydrophobic silicon surface.

Therefore, even if the substrate is stored as it is after the silicon oxide film is formed by heating, no problem occurs.

[0014]

Further, in a semiconductor having a low impurity concentration, it is generally known that a contact having a lower resistance can be obtained by making contact with an insulating layer

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rather than by making a metal contact directly. When a metal is brought into direct contact with the semiconductor, a large number of interface states are formed on the surface of the semiconductor, and this serves as an electrical barrier. On the other hand, by providing a good insulating layer on the surface, this barrier is greatly reduced. Therefore, conventionally, an annealing step of forming an alloy layer of a semiconductor substrate has been required after the deposition of the metal film. In contrast, the present invention eliminates the need for such an annealing step. Further, as described above, the semiconductor surface doped with impurities has a problem that the impurities on the surface are reduced by receiving heat. However, by adopting the method of the present invention, the heating is completed in a short time. The problem of segregation of is reduced.

[0015]
Next, the process conditions will be described.

[0016]

For the heat treatment of the silicon surface, heating with a UV lamp is preferably used from the viewpoint of easy handling.

The UV lamp may be installed inside or outside the heating chamber (chamber).

[0017]

In addition to the heating by the UV lamp described above, heating in the furnace, heating by steam, or heating by RTP (rapid thermal processing) may be used. Among them, heating by RTP is preferable from the viewpoint that the surface of the oxide film can be obtained smoothly.

[0018]

During heating, the substrate is placed in an atmosphere containing oxygen. The atmosphere may be the air, but an oxygen (O2) or ozone (O3) atmosphere is preferable from the viewpoint of promoting the oxidation reaction. In particular, in an ozone atmosphere, the residual resist can be ashed simultaneously with the formation of the oxide by heating. Further, the atmosphere of

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oxygen or ozone may contain an inert gas such as argon or helium, or a diluent gas such as nitrogen gas.

[0019]

The heating time of the silicon surface is 1 second or longer, preferably 5 seconds or longer, and more preferably 10 seconds or longer in order to form a sufficient oxide film. However, this time largely depends on operating conditions such as the output of the UV lamp and the distance between the substrate and the UV lamp. Further, there is no problem even if the heating time is sufficiently long as long as it does not affect the device itself. The pressure during heating is 10 mTorr or more, preferably 100 mTorr or more, and may be several times or less to several tens times or less the atmospheric pressure.

[0020]
Semiconductors to which the present invention can be applied include silicon carbide (SiC) and germanium (Ge) in addition to the above-mentioned silicon.

[0021]

When the semiconductor is silicon, it may be amorphous silicon or crystalline silicon.

また、ノンドープシリコンであってもドープシリコンであってもよい。 However, it may be preferable to use light doping to some extent from the viewpoint of forming a good contact with a metal.

[0022]

It should be noted that various types of semiconductor manufacturing apparatuses can be used for implementing the present invention. It may be a cluster tool type semiconductor manufacturing system having a substrate transfer chamber in the center or an in-line type semiconductor manufacturing system.

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[0023]

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT A preferred embodiment of the present invention will be described below with reference to the accompanying drawings. In the drawings, the same elements correspond to the same reference numerals, and duplicate description will be omitted.

[0024]

FIG. 1 is a flow chart showing typical steps according to the present invention. FIG. 2 is a cross-sectional view of a semiconductor substrate processed according to the flowchart shown in FIG. 1, showing changes in the substrate corresponding to the steps of FIG. In this embodiment, a cluster tool type semiconductor manufacturing system was used. The transfer of substrates between each process was done via a transfer chamber in the center of the cluster tool.

[0025]

As shown in FIG. 2A, first, a hard mask 4 of polysilicon (Poly Si) was formed on the silicon substrate 1 on which the SiO2 layer 2 and the BPSG (borophosphosilicate glass) layer 3 were formed. Next, a photoresist was applied on the hard mask 4, and after exposure and development, the hard mask polysilicon 4 was etched to form a hard mask 4 for forming a contact hole (FIG. 2B).

[0026]

Next, a portion of the BPSG layer 3 and the SiO2 layer 2 which was not protected by the hard mask was etched using a fluorine-based etchant gas to form a contact hole 5 (FIG. 2C). At this time, the silicon 1 is exposed at the bottom of the contact hole 5.

[0027]

Immediately after forming the contact hole 5, the substrate was transferred to the heating

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chamber through the transfer chamber without breaking the vacuum. A UV lamp is installed inside the heating chamber so that the surface of the substrate can be irradiated with UV to heat the surface. The inside of the heating chamber is made into an ozone (O3) atmosphere, the surface of the transferred substrate after the formation of the contact hole is heated by a UV lamp for about 10 seconds, and the exposed silicon surface at the bottom of the contact hole 5 is made of silicon having a thickness of about 30 angstrom The oxide film 6 was formed (FIG.2 (d)).

[0028]

Next, the substrate was transferred to the CVD chamber for the underlayer, and the Ti / TiN film 7 was formed as the underlayer by thermal CVD. Then, the substrate was transferred to a CVD chamber for forming a tungsten film, a blanket tungsten layer 8 was deposited using WF6 as a raw material, and the contact hole 5 was embedded (FIG. 2 (e)). Although not performed in this embodiment, an optional cleaning process may be performed after the etching process of the BPSG layer and the SiO2 layer or the heating process using a UV lamp. In addition, after forming the Ti / TiN film, annealing may be performed to enhance the wettability of the underlayer.

[0029]

As described above, according to the present invention, there is provided a semiconductor manufacturing method for obtaining good contact between a semiconductor and a wiring through an insulating layer in a multilayer wiring of a semiconductor device having a high degree of integration. .. Further, according to the present invention, there is provided a semiconductor manufacturing method which realizes high productivity and yield by a simplified process which does not require extra cleaning process and annealing process. Further, according to the present invention, there is provided a semiconductor manufacturing method capable of obtaining good electrical contact to a semiconductor having a relatively low resistance without performing an annealing treatment.

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CLAIMS JP2000216241

1.
An insulating layer is formed on the semiconductor layer, a part of the insulating layer is removed until a part of the surface of the semiconductor layer is exposed, and a contact hole having the exposed surface of the semiconductor layer as a bottom surface is formed. Heating the exposed surface of the semiconductor layer to form a film of the oxide of the semiconductor on the exposed surface, filling the contact hole with a metal, and further removing the metal so that the metal covers the insulating layer. Method for manufacturing semiconductor device to be deposited.

2.
The method of manufacturing a semiconductor device according to claim 1, wherein the exposed surface is heated by irradiation of an ultraviolet lamp.

3.
The method for manufacturing a semiconductor device according to claim 1, wherein the heating of the exposed surface is performed in an atmosphere of oxygen (O2) or ozone (O3).

4.
The method for manufacturing a semiconductor device according to claim 1, wherein the exposed surface is heated for 1 second or longer.

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5.
The method of manufacturing a semiconductor device according to claim 1, wherein the oxide film has a thickness of 0.1 to 10 nm.

6.
The method for manufacturing a semiconductor device according to claim 1, wherein the semiconductor is silicon.

7.
The method for manufacturing a semiconductor device according to claim 1, wherein the semiconductor is selected from the group consisting of silicon carbide (SiC) and germanium.

8.
The method for manufacturing a semiconductor device according to claim 6, wherein the silicon is doped silicon.

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㊹発明の名称　化合物半導体装置の製造方法、化合物半導体装置及び電界効果トランジスタ

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㉗発明者　ジョン・バティ　アメリカ合衆国コネチカット州ダンバリイ、ブリタニア・ドライブ11番地
㉑出願人　インターナショナル・ビジネス・マシーンズ・コーポレーション　アメリカ合衆国10504、ニューヨーク州　アーモンク(番地なし)
㉔代理人　弁理士　山本　仁朗　外1名

最終頁に続く

明　細　書

1.発明の名称　化合物半導体装置の製造方法、化合物半導体装置及び電界効果トランジスタ

2.特許請求の範囲

(1)　安定した成長層を持ち配向度合の高い平滑な表面を有する化合物半導体層を形成する工程と、

前記化合物半導体層のピンニングを阻止し、前記表面上に次の工程で形成される絶縁材料の浸透を防ぐために十分な厚みを有するエピタキシャルかつ単結晶で連続的な単元素の半導体材料層を形成する工程と、

前記単元素半導体材料層上に絶縁物層を形成する工程と、

から成る低界面状態密度を有する化合物半導体装置の製造方法。

(2)　安定した成長層を持つ配向度合の高い平滑な表面を有するGaAs層をエピタキシャルに成長させる工程と、

上記GaAs表面上に、該表面のピンニングを阻止するエピタキシャルかつ単結晶で連続的なSi層をエピタキシャルに成長させる工程と、

上記Si層上にSiO_2層を堆積させる工程と、

から成る低界面状態密度を有する化合物半導体装置の製造方法。

(3)　エピタキシャルに成長した化合物半導体層と、

上記化合物半導体層に直接に接触し且つ電気的低リークの絶縁物層と、

から成る化合物半導体装置。

(4)　禁止帯幅全域を通じて移動される界面フェルミ準位を許容する状態密度を有するエピタキシャルに成長された化合物半導体層と、

電界効果トランジスタのゲート絶縁体として動作するに十分な厚みを有する、上記化合物半導体層上の電気的低リークの絶縁物層と、

上記化合物半導体層と上記絶縁物層間に配置されたエピタキシャルかつ単結晶で連続的な単元素半導体層と、

から成る化合物半導体装置。

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(5) 禁止帯幅全域を通じて移動される界面フエルミ準位を許容する状態密度を有するエピタキシヤルに成長したGaAs層と、

電解効果トランジスタのゲート絶縁体として動作するに十分な厚みを有する、上記GaAs層上の電気的低リークな絶縁物であるSiO_2層と、

上記GaAs層と上記SiO_2層間に配置され、該SiO_2層をGaAs層からへだてるのに十分な厚みを有するエピタキシヤルかつ単結晶かつ連続的なSi層と、

から成る化合物半導体装置。

(6) 禁止帯全域を通じて移動される界面フエルミ準位を許容する状態密度を有するエピタキシヤルに成長した化合物半導体層と、

上記化合物半導体層上に配置されたエピタキシヤルかつ、単結晶かつ連続的な単元素半導体層と、

上記単元素半導体層上の電気的低リークの絶縁物から成るゲート絶縁層と、

上記絶縁層の表面上に配置された導電性部材と、

上記化合物半導体内に形成され、上記ゲート絶縁層をはさんで互いに反対側に一定間隔を置いて設けられたソース領域及びドレイン領域と、

から成る電界効果トランジスタ。

3.発明の詳細な説明

A．産業上の利用分野

本発明は、金属酸化物半導体（ＭＯＳ）構造、特にGaAs等のような化合物半導体上のＭＯＳ構造に関するとともに、化合物半導体上にSiO_2等のようなゲート絶縁物を形成する方法に関する。

B．従来の技術

従来からGaAs上に金属酸化物半導体構造を実現する試みは成功していない。それは、誘出されたGaAs表面あるいは、ほとんどすべての材料との界面で、ほとんどいつも存在している界面の状態密度が非常に高いからである。このように界面の状態密度が高いと、GaAs界面でのフエルミ準位のピンニングが生じる。このフエルミ準位のピンニングは、非常に固く、そのことは、再現性のある金属半導体であるGaAsのＭＥＳＦＥＴデバイスの基本原理である。上記フエルミ準位は、エネルギーギヤップの大体中央、すなわち、表面でのエネルギー伝導帯とエネルギー価電子帯との間の中央位置に固定されている。

しかしながら、フエルミ準位がギヤップの中心からずれるような多くの応用が望まれる。そのために、従来、GaAs表面を化学的処理することを含む試みが為された。これらの試みとして次のものが挙げられる。

(i) 水と光で処理することによるGaの酸化物表面の形成と題するオフセイ（Offsey）他によるApplied Physics Letters No.48，475頁，1986年。

(ii) ナトリウム硫化物処理によるパッシベーションと題するサンドロフ（Sandroff）他によるApplied Physics Letters No.51，33頁，1987年。

(iii) GaAs上のGe又はSiの薄膜層は、違つたショットキ・バリアの高さになることが知られており、表面でのフエルミ準位の変更を示している（グラント（Grant）他著、Journal of Scientific Technology 5巻 No.4，1015頁，1987年）。

C．本発明が解決しようとする問題点

しかしながら、上記従来のものには、表面でのフエルミ準位の位置が禁止帯幅を通じて移動し得るということについては示されていなかつた。また、GaAs上にＭＯＳ構造を作成する場合、表面フエルミ準位は、ゲート電極に印加されるバイアス電圧によつて表面フエルミ準位が変えられるようにするため、固定されるべきでない。フエルミ準位の移動は、ゲート電極に印加されるバイアス電圧の極性に依存して反転モード又は蓄積モードでデバイスを動作させることができる。

更に、低リークゲート絶縁材料は、電荷キヤリヤのゲート制御を最大限行なうために必要である。しかしながら、フエルミ準位を固定しない従来技術のどれも、界面のフエルミ準位を再ピンニングすることなしに、処理表面上に低リーク絶縁材料を形成できなかつた。リークしやすい絶縁体を備えたＭＯＳキヤパシタ構造は、一般的に不十分なC

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－Ｖ特性を表わす。これは、チャネルと金属層が電荷を交換できるからである。そして、絶縁体がリークしやすいとき、フェルミ準位が固定されていないＧａＡｓ表面でさえ、ゲート電極によつて良好な電荷制御を示さない。

Ｄ．問題点を解決するための手段

本発明は、酸化物・化合物半導体装置と、低リーク絶縁体材料のみならず、フェルミ準位の固定されていない化合物半導体表面を備えた半導体装置の製造方法に関する。

ゲート漏れ電流は、プラズマＣＶＤによる高品質な酸化物によつて最小限にされる。ゲートリーク電流と界面状態密度は十分に低いので、フェルミ準位が固定されない化合物の半導体表面に応じて、半導体バンドギャップ全域、すなわち蓄積レベルから反転レベルまでの範囲を移動する。

本発明は、Ⅱ－Ⅵ族だけでなく、Ⅲ－Ⅴ族の化合物半導体で行なうことができる。

本発明は、化合物半導体であるＧａＡｓに関して以下に記述されているが、本発明は、特にⅢ－Ⅴ族の化合物材料に限定されない。

概略的に、本発明に係る半導体装置は、ＧａＡｓ基板、所定の膜厚を有するⅢ－Ⅴ族の種々なエピタキシャル層、特定の素子形成用の特定の成分のドーピング領域、界面単元素半導体層、及び半導体材料の絶縁層から構成されている。そして、複数の製造ステップを通じて形成されるゲート金属は、ベーシックＭＯＳデバイスを形成するために絶縁層上に配設される。単元素半導体材料は、シリコンとゲルマニウムから成るグループから選ぶことができ、そして上記絶縁層は、シリコン酸化物を含んでいる。

単体シリコンとSiO_2を含んでいる絶縁層から成る界面層を有する化合物半導体は、本発明の一実施例に過ぎない。半導体装置の製造方法では、（１００）の配向を有するＧａＡｓエピタキシャル層は、安定した成長層を持つ平滑な表面を形成する条件下で成長される。成長層は種々の構造、例えば、Ａｓで安定化されたＣ（２×８）成長層のような構造をとることができる。分子線エピタキシ（ＭＢＥ）による成長は、一般的に他の方法よりも、より平滑で良い配向の表面を形成する。

それから、Ｓｉのエピタキシャル層は、エピタキシャルＧａＡｓ上に形成される。Ｓｉ層は、ＧａＡｓエピタキシャル層上にその場で堆積される。その後、絶縁材料層は、Ｓｉ半導体層上に堆積され、そして、金属ゲートは、絶縁層上に堆積される。Ｓｉ層の膜厚は、絶縁材料がＧａＡｓエピタキシャル層に侵入するのを防いでＧａＡｓの酸化を防ぐことができるような厚さであれば十分である。Ｓｉ層が堆積された後、半導体装置は、ＭＢＥ装置から搬出され、SiO_2膜形成のために別の装置に搬入される。この搬送の間、たいへん薄い酸化膜がＳｉ層上に形成される。上記SiO_2層は、低温下で高品質の酸化膜を形成するプラズマＣＶＤ技術を使つて堆積される。

それから、半導体装置は、熱処理され、ゲート金属がＭＯＳデバイスを形成するために通常のデポジション技術によつて堆積される。あるいは、SiO_2層は、真空を破壊することなく、隣接するＣＶＤチャンバにＳｉ/ＧａＡｓ構造体を搬送することによつて、ＧａＡｓとＳｉの堆積物上にその場で堆積される。本発明の構造体は、電界の存在下において、界面フェルミ準位を禁止帯全域を通じて移動させるような状態密度を有するエキタキシャル成長した化合物半導体ＧａＡｓ層を含んでいる。また、漏れ電流の低い絶縁材料であるSiO_2層は、化合物半導体上に堆積し、そして、エピタキシャル層で、単結晶で、連続的な単元素Ｓｉ半導体層が化合物半導体層と絶縁物層との間に堆積される。更に、ゲート金属は、例えばＭＯＳキャパシタのようなＭＯＳデバイスをつくるために、絶縁物層上に設けられる。ソースとドレイン領域は、化合物半導体層で、従来から知られているイオン注入その他の技術によつて形成することができ、さらに、ＭＯＳＦＥＴを形成するためにゲートによつて分離される。

従つて、本発明は、ＧａＡｓのすぐれた移送特性だけでなく、SiO_2/Ｓｉ系のすぐれた電荷制御特性を保持するＧａＡｓ　ＭＯＳＦＥＴを提供する

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ものである。

E．実施例

第１図に示すように、本発明の構造１０は、GaAs基板１２と、平滑な表面を形成する成長条件下で分子線エピタキシによつて成長される３層以下の表面粗さを持つ（１００）方位の複数のGaAsエピタキシャル層１４を含んでいる。ＭＢＥ技術は、配向性が高く且つ平滑な表面を形成するのに好ましいけれども、エピタキシャル成長は、化学的蒸着方式でも行われる。エピタキシャル成長は、一般的に超高真空域内で行われる。GaAsの成長は、表面で安定化した成長層を形成させる条件下で終了する。ＭＢＥによるGaAsエピタキシャル成長は、Asで安定化されたＣ（２×８）の成長層をもたらす。他のⅢ－Ⅴ族の原子も表面上で陰イオンで安定化した成長層をもたらす。例えば、InP 系では、Pで安定化された成長層が形成される。Gaのような金属リッチな物質で安定化された成長層も存在するであろう。典型的な成長層の例は、Ｃ（４×４）、Ｃ（２×８）、Ｃ（８×２）、１×６及び４×６である。そして、これらはGa表面の濃度が増加する順にならべられている。これらの成長層は、例えばJ.of Vac. Sci. Tech．５巻４号１１３５頁，１９８７年７、８月号に示されるような種々な条件の下で形成してもよい。

Asで安定化したＣ（２×８）成長層が成長するとき、周囲のAs蒸気はAs源を閉じること及び／又は冷却することによつて減少させられる。その時、基板は、As Ｃ（2×8）成長層を維持できるように、３００℃～４００℃の範囲の温度に冷却される。表面の化学量論的組成は、表面の成長層に直接関係する。そして、この表面の化学量論的組成が構造の電気的特性に深い影響を与えると予想されている。

Si層１６は、エピタキシャル層１４を成長させるために使用される、同じ超高真空ＭＢＥ又はＣＶＤ装置を用いてエピタキシャル層１４の清浄な表面上に堆積される。そしてSi層１６は、低速度、例えば約0.1Å／secでエピタキシャル層１４上に堆積される。Si層１６の厚みは、いくつかの制約によつて決定される。最小の厚みは、GaAs表面を覆い、且つピンニングさせないために必要とされるSiの最小限の量によつて決定される。更に、その厚みは、後のSiO_2の堆積がGaAsに浸透して酸化させるのを防ぐのに十分なものでなければならない。Si層の最大の厚みは、Si内において電気的伝導現象が十分に行なわれることのないような厚みでなければならない。GaAsの移送特性はSiよりも優れているので、GaAs層内のチャネルにキャリヤを閉じ込めることが望ましい。Si層１６の厚みは、５Å～１００Åであり、特に１０Å～４０Åの間であつてもよい。

上述の堆積条件下では、Siの吸着原子は、著しい量が基板に混入することなく、エピタキシャル層を十分な時間をかけて形成する。Si層の成長中に観察される反射電子回折パターンは、基板のＣ（２×８）成長層が約５ÅのSiが堆積した後に取り除かれ、そして、Si層が単結晶であることを示す。数１０Åの範囲の層の厚さで、Si層も仮晶である。すなわち、Si層は、基板と同じ格子定数を持つように変質させられる。また、SiによるGaAs表面の非ピン止め効果の原因は完全には解明されていない。平滑に成長されたGaAs表面は、Si/GaAsの密着性をコントロールし、欠陥密度の低い急峻なヘテロ界面を形成する上できわめて重要である。フエルミ準位のピンニングを通常もたらすGaAsのダングリングボンドは飽和され、それによつて禁止帯中から界面状態が取り除かれている。

Si層１６が堆積された後、構造体はＭＢＥ装置から取り出され、SiO_2層１８の堆積を行うための他の装置内に搬入される。この構造体の搬送中、構造体の表面は大気にさらされる。Si表面層は、大変薄く且つ安定した酸化物を形成すること及びSi層と自然酸化物層は、GaAs表面上に保護層を形成することが期待されている。SiO_2層１８は、好ましくは堆積中に低い基板温度を利用して高品質の酸化物を形成するプラズマＣＶＤ技術により堆積される。SiO_2層は、基板温度が

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約３５０℃、堆積速度が約６０Å／minで３０Å～５００Åの厚みに堆積される。

プラズマＣＶＤにより形成される酸化物の質は、基板表面の粗さだけでなく、堆積前の基板表面上に存在する不純物に影響を受けやすいということが知られている。これら２つの要因は、ＵＨＶ条件下で成長され且つ大変平滑な表面を有するＭＢＥ層（Ｓｉ層１６）上に形成する場合には最小化される。上記プラズマＣＶＤ技術については、バテイ（Ｂａｔｅｙ）その他による次の論文により詳細に開示されている。

(i) プラズマＣＶＤによる高品質二酸化シリコン（SiO_2）の低温デポジションと題するバテイ（Ｂａｔｅｙ）その他による J. of Appl. phys. ６０巻９号，３１３６頁，１９８６年１１月１日。

(ii) 低い基板温度でデポされた非常に薄いSiO_2膜の電気的特性と題するＩＥＥＥ Elec. Dev. Lett. ＥＤＬ－８巻，４号，１４８頁、１９８７年４月。

他の実施例では，構造体のすべての層が真空状態を維持したまま堆積させられる。この方法では、Ｓｉ/ＧａＡｓ構造体は、エピタキシャル層の堆積中に存在する真空を破壊せずにＣＶＤチャンバーに搬送される。

SiO_2絶縁層は、その後ＣＶＤプロセスにより堆積させられる。本実施例では、自然酸化物の形成が避けられる。そして、すべての層のデポジションは大気中に存在する不純物にさらされることがないので大変清浄に行なわれる。SiO_2のデポジションにおいて、少なくとも最初に、一定量の酸化物が単元素シリコン層に拡散する。

上述のように、シリコン層１６の膜厚は、SiO_2のデポジションがエピタキシャルＧａＡｓ層１４に浸透して酸化させることのないように十分なものでなくてはならない。特に、Ｓｉ層１６は、SiO_2層のデポジション後、Ｓｉの薄膜層が最終的に残るように十分に厚くしている。しかしながら、Ｓｉ層１６の膜厚は、シリコン層１６全体がSiO_2のデポジションにより消耗されるように成長させることができる。したがつて、本発明は、ＧａＡｓエピタキシャル層１４上に形成されたSiO_2層１８を有する最終的な構造体を提供することができる。

第２図に示すヘテロ構造体１１は、かかる最終的な構造体の一例である。従つて、当該実施例では、Ｓｉ薄膜層１６は、SiO_2絶縁層１８がＧａＡｓエピタキシャル層１４に直接接触するように、シリコン層１６の十分な消耗が行なわれている間、ＧａＡｓの酸化を抑える。このとき各層は、１５分以上の時間、種々の不活性ガス雰囲気中で４００℃～７５０℃に加熱される。その後、ゲート金属が従来からある技術でデポジションされる。そして、ヘテロ構造体１０、１１は、追加の加熱処理を必要とする。

加熱処理は、標準シリコンＭＯＳ技術において行なわれるフオトリソグラフイ処理と非常に類似している。加熱処理は、界面状態密度を減少させるために必要である。

加熱処理されたＭＯＳキヤパシタの電気特性は、第３図及び第４図に示されている。

第３図に示された容量対電圧（Ｃ：Ｖ）特性は、反転層がＧａＡｓエピタキシャル層１４内に形成され、界面でのフエルミ準位がバンドギヤツプ全体を通して移動させられるということをはつきりと示している。第３図のキヤパシタは、タングステン・シリサイドから成るゲート金属で作られたものである。

基板は、窒素のプレデポジション工程で４５０℃で３０分間アニールされ、ＷＳｉが全面にデポジションされ、エツチングがゲートを形成するために施される。そして、フオーミングガス中で３０分間、４５０℃でポスト・メタルアニールするとデバイスが完成した。

第３図に示す擬似Ｃ－Ｖ曲線ａは、0.1Ｖ／Ｓで掃引され、高周波（１ＭＨｚ）曲線ｂとｃは、矢印で示される方向に0.5Ｖ／Ｓで掃引された。第３図に示したゲートキヤパシタンスは、酸化膜キヤパシタンスＣｏｘに等しいＣｍａｘに統一される。この例ではＣｏｘは４５ｐＦである。ヒステリシス特性、引き伸ばされた曲線形状、そして高低

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両周波数を示すC－V曲線間の大きなずれは、界面付近に遅い状態と速い状態が両方存在していることを示すものである。

第4図に示す電流対電圧特性は、ゲート金属（例えばAℓ）から酸化膜への電荷注入作用を示し、そして非常に高品質な酸化膜と非常に高品質な金属と酸化膜との界面を表わしている。曲線dはゲートに印加される負のバイアスに関し、曲線eは正のバイアスに関する。

本発明に従つて製造されたGaAs MOSFET13は、第5図に概略的に示されている。また、第1図に示されるように、層12、14、16を作成した後、ゲート20とゲート絶縁領域が典型的なプロセス技術で形成され、それにソース領域22及びドレイン領域24は、例えば、イオン注入技術によつて形成される。

更に1ボルトづつV_Gを変化させたときのI_D対V_{DS}のGaAs MOSFET特性が第6図に示されている。そして当該MOSFETにはタングステン・シリサイド・ゲートが設けられる。第6図に示された特性は空乏モードで操作する30ms／mmの相互コンダクタンス及び、8μmの長さのゲートを有するデバイスに関するものである。相互コンダクタンスは、完全なピンチオフを持つデバイスにおいては60ms／mmまで得られていた。

F．発明の効果

上述のように本発明によれば、優れた特性を有する化合物半導体装置を提供できる。

4.図面の簡単な説明

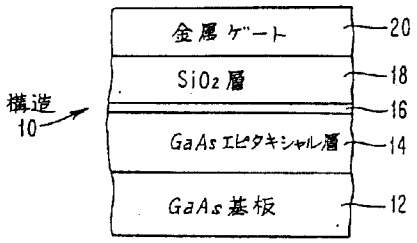
第1図は、本発明の実施例であるGaAs MOS構造を示す概略横断面図、第2図は、本発明の他の実施例であるGaAs MOS構造を示す概略横断面図、第3図及び第4図は、本発明に従つて形成したP型MOSキャパシタの容量対電圧及び電流対電圧の各特性を示すグラフ、第5図は、本発明の更に他の実施例であるMOSFETを示す概略横断面図、第6図は、本発明の第5図の実施例であるMOSFETのソースとドレインの特性を示すグラフである。

10、11……構造、12……GaAs基板、13……GaAs MOSFET、14……GaAsエピタキシャル層、16……Si層、18……SiO_2層、20……金属ゲート、22……ソース領域、24……ドレイン領域。

出願人　インターナショナル・ビジネス・マシーンズ・コーポレーション

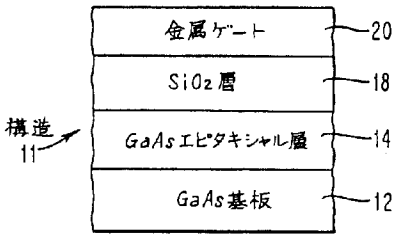
代理人　弁理士　山本仁朗（外1名）

FIG. 1



16…Si層

FIG. 2



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FIG. 3

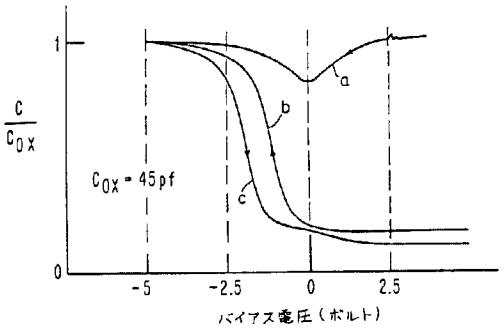


FIG. 5

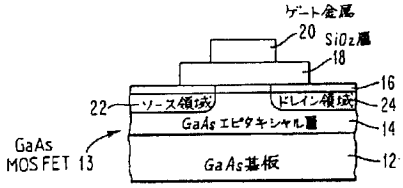


FIG. 4

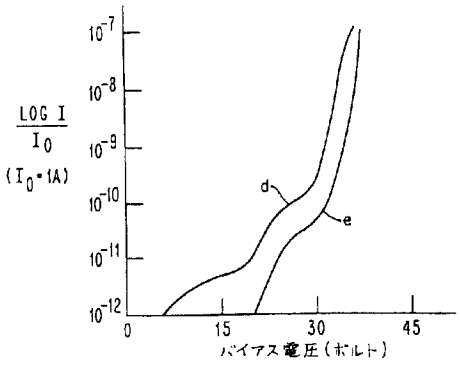
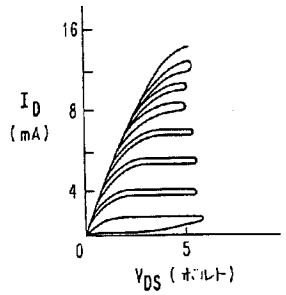


FIG. 6



第1頁の続き

⑤1Int. Cl.[5]	識別記号	庁内整理番号
H 01 L 21/205		7739−5F
21/31	C	6824−5F

⑦2発　明　者　サンデイプ・テワリ　アメリカ合衆国ニューヨーク州オシニング、パイネスブリッヂ・ロード791番地

⑦2発　明　者　ステイブン・ローレンズ・ライト　アメリカ合衆国ニューヨーク州ピークスキス、サウス・ヒル・ロード・ボックス218、アール・デイー1番地

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JPH0226073A MANUFACTURE OF COMPOUND SEMICONDUCTOR DEVICE, COMPOUND SEMICONDUCTOR DEVICE AND FIELD EFFECT TRANSISTOR

Applicants: IBM

Inventors: JIYON BATEI,SANDEIPU TEWARI,SUTEIBUN ROORENZU RAITO

Classifications:

IPC ***H01L21/203; H01L21/205; H01L21/28; H01L21/31; H01L21/314; H01L21/336; H01L29/267; H01L29/43; H01L29/78;*** (IPC1-7): H01L21/203; H01L21/31; H01L29/78; H01L29/784; H01L21/205;

CPC **H01L21/02274 (US); H01L21/28264 (EP); H01L21/314 (EP); H01L29/267 (EP); H01L29/432 (EP); H01L29/66522 (EP);** Y10S148/149 (EP); Y10S438/933 (EP); Y10S438/958 (EP);

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MANUFACTURE OF COMPOUND SEMICONDUCTOR DEVICE, COMPOUND SEMICONDUCTOR DEVICE AND FIELD EFFECT TRANSISTOR

Abstract

PURPOSE: To obtain superior characteristics by providing not only an oxide compd. semiconductor device and low leakage insulation material but a compd. semiconductor surface wherein the Fermi level is not fixed. CONSTITUTION: A structure 10 comprises a GaAs substrate 12 and GaAs epitaxial layer 14 grown by the molecular beam epitaxy under the growing condition for forming a smooth surface. After depositing an Si layer 16, the structure is taken out from an MBE device and SiO2 layer 18 is deposited. Such a structure involves an epitaxially grown compd. semiconductor GaAs layer 14 having a state density for moving the interface Fermi level over the entire inhibited band in the presence of an electric field, an SiO2 layer 8 made of a low leak current insulation material on the compd. semiconductor and a single crystal and single element type Si semiconductor epitaxial layer 16 deposited between the compd. semiconductor layer and insulator layer. Thus, a superior GaAs transfer characteristic and a superior SiO2 /Si type charge control characteristic are obtained.

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DESCRIPTION JPH0226073

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a metal oxide semiconductor (MOS) structure, particularly an MO8 structure on a compound semiconductor such as GaAs, and forming a gate insulator such as SiO2 on the compound semiconductor. Regarding the method. B. Conventional Technology Conventionally, attempts to realize a metal oxide semiconductor structure on GaAs have not been successful. This is because the density of states of the exposed GaAs surface or the interface with almost all the materials, which is almost always present, is very high. When the state density at the interface is high in this way, Fermi level pinning occurs at the GaAs interface. This Fermi level pinning is very hard, which is the basic principle of reproducible metal semiconductor GAS MESFET devices. The Fermi level is fixed at about the center of the energy gap, that is, at the center between the energy conduction band and the energy valence band on the surface. However, many applications are desired in which the Fermi level is offset from the center of the gap. To that end, attempts have heretofore been made to involve chemically treating the GaAs surface. These attempts include the following. (1) Applied Physics Letters No, 48 pp. 475, 1986, by Offsey et al., Entitled Ga oxide surface formation by treatment with water and light. (11) Applied Physics Letters No, Sandroff et al., Entitled Passivation by Sodium Sulfide Treatment, page 51, page 36, 1987. (It is known that the Go or Si thin film layer on i + D aa A S has different Schottky barrier heights, indicating a change of 7 engineering Lumi levels on the surface (ground (Grant) et al., Journalof 5cientific Technology 5 volumes No, 4. 1015, 1987). C0 Problems to be Solved by the Present Invention However, the above-mentioned prior art has not shown that the position of the Fermi level on the surface can move through the band gap. Further, when the MO8 structure is formed on GaAs, the surface Fermi level should not be fixed so that the surface Fermi level can be changed by the bias voltage applied to the gate electrode. The Fermi level shift can operate the device in either inversion mode or accumulation mode depending on the polarity of the bias voltage applied to

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the gate electrode.

In addition, a low leakage gate insulating material is needed for maximum gate control of charge carriers. However, none of the prior art techniques that fixed the Fermi level were able to form a low-leakage insulating material on the treated surface without re-pinning the Fermi level at the interface. MOS capacitor structures with leaky insulators exhibit C-V characteristics that are not sufficient for fishing. This is because the channel and the metal layer can exchange charges. And when the insulator leaks easily, even the GaAs surface where the Fermi level is not fixed does not show good charge control by the gate electrode. The present invention relates to an oxide / compound semiconductor device and a method for manufacturing a semiconductor device including not only a low-leakage insulator material but also a compound semiconductor surface in which the Fermi level is not fixed. .. Gate leakage current is minimized by high quality plasma CVD oxides. Since the gate leakage current and the interface state density are sufficiently low, they move in the entire semiconductor band gap, that is, in the range from the accumulation level to the inversion level according to the semiconductor surface of the compound in which the Fermi level is not fixed. The present invention can be carried out not only in the U- ■ group but also in the m-v group compound semiconductors. Although the present invention is described below with respect to GaAs which is a compound semiconductor, the present invention is not particularly limited to the compound materials of the groups (1)-(4). Schematically, a semiconductor device according to the present invention includes a GaAs substrate, various epitaxial layers of group-v having a predetermined film thickness, a doping region of a specific component for forming a specific device, an interface single element semiconductor layer, And an insulating layer of semiconductor material. Then, the gate metal formed through the plurality of manufacturing steps is disposed on the insulating layer to form a basic MOS device. The single element semiconductor material can be selected from the group consisting of silicon and germanium, and the insulating layer comprises silicon oxide. A compound semiconductor having an interface layer formed of an insulating layer containing elemental silicon and SiO2 is only one example of the present invention. In the method of manufacturing a semiconductor device, a GaAs epitaxial layer having an (ioo) orientation is grown under conditions that form a smooth surface having a stable growth layer. The growth layer can have various structures, such as a C (2 × 8) growth layer stabilized with As. Growth by molecular beam epitaxy (MBE) -forms a smoother and better oriented surface than other methods for fishing.

Then, an epitaxial layer of Si is formed on the epitaxial GaAs. The Si layer is deposited in situ on the GaAs epitaxial layer. Thereafter, a layer of insulating material is deposited on the Si semiconductor layer and a metal gate is deposited on the insulating layer. The film thickness of the Si layer is sufficient as long as it can prevent the insulating material from entering the GaAs epitaxial layer and prevent GaAs from being oxidized. After the Si layer is deposited, the semiconductor device is unloaded from the MBE device and loaded into another device to form a

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SiO2 film. During this transport, a very thin oxide film is formed on the Si layer. The SiO2 layer is deposited using a plasma CVD technique that forms a high quality oxide film at low temperatures. The semiconductor device is then heat treated and gate metal is deposited by conventional deposition techniques to form MOS devices. Alternatively, the Si 02 layer is deposited in situ on the Ga as and Si deposits by transporting the Si / GaAs structure to an adjacent CVD chamber without breaking the vacuum. The structure of the present invention includes an epitaxially grown compound semiconductor GaAs layer having a density of states that moves the interface Fermi level in the entire forbidden band in the presence of an electric field. Further, the SiO2 layer, which is an insulating material having a low leakage current, is deposited on the compound semiconductor, and an epitaxial layer, a single crystal, and a continuous single element Si semiconductor layer are formed between the compound semiconductor layer and the insulator layer. Be deposited on. In addition, gate metal is provided on the insulator layer to make MOS devices such as MOS capacitors. The source and drain regions are compound semiconductor layers that can be formed by conventional ion implantation or other techniques, and are separated by gates to form a MOSFET. Therefore, the present invention provides a GaAs MOSFET that retains not only excellent transfer characteristics of GaAs but also excellent charge control characteristics of SiO2 / Si system. E, Example As shown in FIG. 1, the structure 10 of the present invention has a GaAs substrate 12 and a surface roughness of 3 layers or less grown by molecular beam epitaxy under growth conditions that form a smooth surface. It includes a plurality of GaAs epitaxial layers 14 having a (1on) orientation. Although the MBE technique is preferred for forming highly oriented and smooth surfaces, epitaxial growth is also done by chemical vapor deposition.

Epitaxial growth is carried out in the ultra-high vacuum region for fishing. The growth of GaAs ends under conditions that form a surface-stabilized growth layer. GaAs epitaxial growth by MBE results in an As-stabilized growth layer of C (2X8). The other atoms of group (1)-(4) also bring about a growth layer stabilized by anions on the surface. For example, in the case of InP, the growth layer stabilized by P is formed. There will also be growth layers stabilized with metal rich materials such as Ga. Examples of typical growth layers are C (4X4), C (2X8), C (8X2), 1x6 and 4x6. Then, these are arranged in the order of increasing concentration on the Ga surface. These growth layers are, for example, J, of Vac, and Sci. It may be formed under various conditions as shown in Tech., Vol. 5, No. 4, page 1135, July, 1987 issue. When an As-stabilized C (2X8) growth layer is grown, ambient As vapor is reduced by closing and / or cooling the As source. At that time, the substrate is cooled to a temperature in the range of 600 ° C to 400 ° C so that the AsC (2X8) growth layer can be maintained. The stoichiometric composition of the surface is directly related to the growth layer on the surface. It is expected that the stoichiometric composition of this surface will have a profound effect on the electrical properties of the structure. The Si layer 16 is deposited on the clean surface of the epitaxial layer 14 using the same ultra high vacuum MBE or CVD equipment used to grow the epitaxial layer 14. Then, the Si layer 16 is deposited on the epitaxial layer 14 at a low rate of 2, for example, about 0.1 person /

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sec. The thickness of the Si layer 16 is determined by some constraints. The minimum thickness is determined by the minimum amount of Si needed to cover the GaAs surface and not spit pinning. Moreover, its thickness must be sufficient to prevent subsequent SiO2 deposition from penetrating and oxidizing GaAs. The maximum thickness of the Si layer must be such that electric conduction phenomenon does not sufficiently occur in Si. Since the transfer characteristics of GaAs are superior to those of Sl, it is desirable to confine carriers in the channel in the GaAs layer. The thickness of the S1 layer 16 is between 5 ^ and 100 ^, in particular between 1oX and 40 persons. Under the above-mentioned deposition conditions, the adsorbed atoms of Si form the epitaxial layer for a sufficient period of time without being contaminated into the substrate in a significant amount.

The backscattered electron diffraction pattern observed during the growth of the Si layer shows that the C (2X8) growth layer of the substrate was removed after about 5 Si was deposited and the Si layer was single crystal. .. With layer thicknesses in the range of a few tens, the Si layer is also returned. That is, the Si layer is altered to have the same lattice constant as the substrate. Further, the cause of the non-pinning effect of Si on the GaAs surface has not been completely clarified. The smooth-grown GaAs surface is extremely important in controlling the adhesion of Si / GaAs and forming a steep Peter interface with low defect density. The dangling bonds in GaAs, which normally result in Fermi level pinning, are saturated, thereby removing interface states from the forbidden band. After the Si layer 16 is deposited, the structure is removed from the MBE device and loaded into another device in the sump where the SiO2 layer 18 is deposited. During transport of this structure, the surface of the structure is exposed to the atmosphere. The Si surface layer is expected to form a very thin and stable oxide, and the Si layer and native oxide layer are expected to form a protective layer on the GaAs surface. The SiO2 layer 18 is preferably deposited by plasma CVD techniques that utilize low substrate temperatures during deposition to form high quality oxides. The Si O2 layer is deposited at a substrate temperature of about 650 ° C and a deposition rate of about 60 ^ / min in a thickness of 30 to 500A. It is known that the quality of oxides formed by plasma CVD is susceptible to not only the roughness of the substrate surface but also impurities existing on the substrate surface before deposition. These two factors are minimized when grown under UHV conditions and formed on one MBE layer (Si layer 16) with a very smooth surface. The plasma CVD technique is disclosed in detail in the following article by Patty et al. (1) J, of Appl by Patty and others entitled Low Temperature Deposition of High Quality Silicon Dioxide (Si O2) by Plasma CVD. physs, Vol. 60, No. 9, page 3136, November 1, 1986. (11) IEEE Elec entitled Electrical Characteristics of Very Thin SiO2 Film Devoted at Low Substrate Temperature. Dev, Lett, EDL-8, Vol. 4, No. 148, April 1987. In another embodiment, all layers of the structure are deposited while maintaining a vacuum. In this method, the Si / GAb structure is transferred to the CVD chamber without breaking the vacuum that exists during the deposition of the epitaxial layer.

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The 5102 insulating layer is then deposited by a CVD process. In this example, the formation of native oxide is avoided. And the deposition of all layers is very clean because it is not exposed to the impurities present in the atmosphere. At least initially in the deposition of SiO2, a certain amount of oxide diffuses into the single element silicon layer. As mentioned above, the thickness of the silicon layer 16 must be sufficient so that the SiO2 deposition does not penetrate into the epitaxial GaAa layer 14 and oxidize it. In particular, the Si layer 16 is sufficiently thick so that a thin film layer of Si will eventually remain after the deposition of the SiO 2 layer. However, the film thickness of the Si layer 16 can be grown so that the entire silicon layer 16 is consumed by the deposition of SiO 2. Therefore, the present invention can provide a final structure having the SiO 2 layer 18 formed on the GaAs epitaxial layer 14. The Peter structure 11 shown in FIG. 2 is an example of such a final structure. Therefore, in this embodiment, the Si thin film layer 16 suppresses the oxidation of GaAs while the silicon layer 16 is sufficiently consumed so that the Si O 2 insulating layer 18 is in direct contact with the GaAs epitaxial layer 14. .. At this time, each layer is heated to 400 ° C. to 750 ° C. in various inert gas atmospheres for 15 minutes or more. The gate metal is then deposited by conventional techniques. So, Peter structure 10.11 requires additional heat treatment. The heat treatment is very similar to the photolithography process performed in standard silicon MO8 technology. Heat treatment is necessary to reduce the interface state density. The electrical characteristics of the heat-treated MOS capacitor are shown in FIGS. 3 and 4. The capacitance-to-voltage (C: V) characteristic shown in FIG. 3 clearly shows that the inversion layer is formed in the GaAs epitaxial layer 14 and the Fermi level at the interface is moved throughout the bandgap. ing. The capacitor of FIG. 3 is made of a gate metal composed of tungsten silicide. The substrate is annealed at 450 ° C. for 30 minutes in a nitrogen predeposition process, WSi is blanket deposited and etching is applied to form the gate. Then, post metal annealing was performed at 450 ° C. for 60 minutes in the forming gas to complete the device.

The pseudo CV curve a shown in FIG. The frequency was swept at IV / S and the high frequency (IMHz) curve C was swept at 0.5 V / S in the direction indicated by the arrow. The gate capacitance shown in FIG. 6 is unified to Cmax equal to the oxide film capacitance Cox. In this example, Cox is 459F. The large shift between the CV curve showing the hysteresis characteristic, the stretched curve shape, and the high and low image frequencies indicates that both the slow state and the fast state exist near the interface. The current-voltage characteristic shown in FIG. 4 shows the charge injection action from the gate metal (for example, A4) to the oxide film, and the interface between the very high quality oxide film and the very high quality metal-oxide film is shown. It represents. Curve d relates to the negative bias applied to the gate and curve e relates to the positive bias. A GaAs MO8FET 13 manufactured according to the present invention is shown schematically in FIG. Also, as shown in FIG. 1, after forming the layer 12.14.16, the gate 20 and the gate insulating region are formed by a typical process technique, in which the source region 22 and the drain region 24 are, for example, It is formed by an ion implantation technique. Figure 6 shows the GaAs MOS FET characteristics of ID vs. vDs when changing vG by

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1 port. Then, the MO8FET is provided with a tungsten-base silicide gate. The characteristics shown in FIG. 6 relate to a device with a transconductance of 30 m5 / mm and a gate with a length of 8 μm operating in depletion mode. Transconductance was obtained up to 60 m5 / mm in devices with perfect pinch-off. F1 Effect of the Invention As described above, according to the present invention, a compound semiconductor device having excellent characteristics can be provided.

[0002]
Brief description of the drawings

[0003]

FIG. 1 is a schematic cross-sectional view showing a GaAs MO8 structure which is an embodiment of the present invention, and FIG. 2 is a schematic cross-sectional view showing a GaAa MO8 structure which is another embodiment of the present invention, FIG. FIG. 4 is a graph showing respective characteristics of capacitance-voltage and current-voltage of a P-type MOS capacitor formed according to the present invention, and FIG. 5 is a schematic cross-sectional view showing a MOSFET which is still another embodiment of the present invention. 6 and 6 are graphs showing the characteristics of the source and drain of the MOSFET according to the embodiment of FIG. 5 of the present invention.

10.11 ... ・ Structure, 12 --- GaAs substrate, i6 ...- Gafi, S MOSFET, 14-GaAs epitaxial layer, 16 ... Si layer, 18 ... SiO2 layer, 20 .... Metal gate, 22 ... Source region, 24 ... Drain region. FIG. 1 Applicant Inter-Digital Business Machine 〒 Ns Corp. Utan Agent Attorney Attorney Mt. Yamamoto Jin Aro (1 person outside) a 6 ... S; No 14 FIG, 2 FIG. F I G。 Bias voltage (this "I sheet") FIG. F I G。 VDS (re)

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1.

Forming a compound semiconductor layer having a smooth surface with a high degree of orientation, and preventing pinning of the compound semiconductor layer to prevent penetration of an insulating material formed on the surface in the next step. To form a continuous single-element semiconductor material layer that is epitaxial and single-crystal and has a sufficient thickness for the purpose of forming a low interface state density, and a step of forming an insulator layer on the single-element semiconductor material layer. A method for manufacturing a compound semiconductor device having the same. (2) A step of epitaxially growing a GaAs layer having a stable growth layer and a high degree of orientation and a smooth surface, and epitaxial and single crystal continuous Si on the GaAs surface for preventing pinning of the surface. A method of manufacturing a compound semiconductor device having a low interface state density, which comprises a step of epitaxially growing a layer and a step of depositing a SiO_2 layer on the Si layer. (3) A compound semiconductor device comprising an epitaxially grown compound semiconductor layer and an insulating layer which is in direct contact with the compound semiconductor layer and has an electrical low leak. (4) An epitaxially grown compound semiconductor layer having a density of states that allows an interface Fermi level to be moved throughout the bandgap, and a thickness sufficient to operate as a gate insulator of a field effect transistor. A compound semiconductor device comprising: an electrically low-leakage insulator layer on a compound semiconductor layer; and an epitaxial single-crystal continuous single-element semiconductor layer arranged between the compound semiconductor layer and the insulator layer. (5) Epitaxially grown GaAs layer having a density of states that allows an interface Fermi level to be moved over the entire band gap, and the GaAs layer having a thickness sufficient to operate as a gate insulator of a field effect transistor. The upper electrically low-leakage SiO_2 layer is disposed between the GaAs layer and the SiO_2 layer, and is epitaxial, single-crystal, and continuous with a thickness sufficient to extend the SiO_2 layer from the GaAs

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layer. Compound semiconductor device comprising a simple Si layer. (6) Epitaxially grown compound semiconductor layer having a density of states that allows an interface Fermi level to be moved throughout the forbidden band, and an epitaxial, single crystal, and continuous single element arranged on the compound semiconductor layer. A semiconductor layer, a gate insulating layer made of an electrically low-leakage insulator on the single-element semiconductor layer, a conductive member arranged on the surface of the insulating layer, and the gate formed in the compound semiconductor, A field effect transistor comprising a source region and a drain region which are provided on opposite sides of the insulating layer at regular intervals.

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(71)出願人　000005108
株式会社日立製作所
東京都千代田区神田駿河台四丁目６番地
(72)発明者　川瀬　大助
茨城県日立市大みか町七丁目１番１号　株式会社日立製作所日立研究所内
(72)発明者　大野　俊之
茨城県日立市大みか町七丁目１番１号　株式会社日立製作所日立研究所内
(72)発明者　小園　裕三
茨城県日立市大みか町七丁目１番１号　株式会社日立製作所日立研究所内
(74)代理人　弁理士　小川　勝男

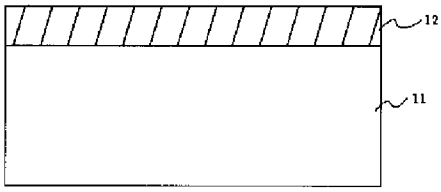
最終頁に続く

(54)【発明の名称】　炭化珪素半導体素子

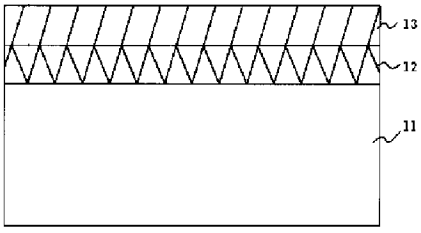
(57)【要約】
【目的】低コンタクト抵抗，炭化珪素半導体のオーム性電極を形成し、高電圧，大電流および高温において信頼性の高い炭化珪素半導体素子を得る。
【構成】炭化珪素単結晶上に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を積層してオーム性電極とした電極構造を持つ炭化珪素半導体素子。また、電極構造上に任意の金属層を積層してオーム性電極とした電極構造を持つ炭化珪素半導体素子。

図　1

(a)



(b)



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【特許請求の範囲】
【請求項１】炭化珪素単結晶に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を積層してオーム性電極としたことを特徴とする炭化珪素半導体素子。
【請求項２】炭化珪素単結晶に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層と任意の金属層を積層してオーム性電極としたことを特徴とする炭化珪素半導体素子。
【請求項３】$10^{18}/cm^3$ 以上の不純物濃度の炭化珪素単結晶上に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層と任意の金属層を積層してオーム性電極としたことを特徴とする炭化珪素半導体素子。
【請求項４】炭化珪素単結晶にＴｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中から少なくとも一種類の金属を含む金属珪化物、金属炭化物及び前記金属，珪素，炭素からなる複合化合物の複数種類を含む層と任意の一種類の金属層または合金層を積層したことを特徴とする炭化珪素半導体素子。
【請求項５】炭化珪素単結晶にＴｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中からの一種類の金属の合金をまたは一種類の金属の積層膜を積層した後に熱処理することにより合金／半導体界面に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を形成してオーム性電極としたことを特徴とする炭化珪素半導体素子。
【請求項６】炭化珪素単結晶にＴｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中からの一種類の金属の合金をまたは一種類の金属を積層後、その上に他金属層もしくは他金属合金層を積層した後に熱処理することにより合金／半導体界面に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を形成してオーム性電極としたことを特徴とする炭化珪素半導体素子。
【請求項７】炭化珪素単結晶表面にＴｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中からの一種類の金属をイオン注入した後に熱処理を行い金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を形成した後に一種類の金属を積層したことを特徴とする炭化珪素半導体素子。
【請求項８】請求項１，２，３，４，５，６または７において、前記炭化珪素半導体の電極構造上にＡｌまたはＡｕを積層した炭化珪素半導体素子。
【請求項９】請求項１から請求項８のいずれかに記載された電極構造を具備したダイオード。
【請求項１０】請求項１から請求項８のいずれかに記載された電極構造を具備したサイリスタ。
【請求項１１】請求項１から請求項８のいずれかに記載された電極構造を具備したトランジスタ。
【請求項１２】請求項１から請求項１１のいずれかに記載された半導体素子を具備した電気回路。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は炭化珪素半導体素子に関する。
【０００２】
【従来の技術】従来の炭化珪素(ＳｉＣ)半導体に形成するオーム性電極は、ｎ型ＳｉＣではニッケル（Ｎｉ），ｐ型半導体ではアルミニウム（Ａｌ）とシリコン（Ｓｉ）の共晶からなる各材料を真空蒸着した後に熱処理を行いオーム性接合を得ていた（J.Electrochem.Soc., vol. 135, p.359.）。ＳｉＣには多くの結晶系が存在し、結晶構造により２．２乃至３．３エレクトロンボルトの禁制帯幅を有する。また、ＳｉＣは、熱的，化学的及び機械的に極めて安定でワイドギャップ半導体としてはめずらしくｐ型及びｎ型共に安定に存在する材料である。従って、ＳｉＣ単結晶に外部回路と電気的接続するための電極を形成した素子は大電力用素子，高温動作素子，耐放射線素子，光電変換素子その他種々の電子技術分野への応用が期待される。
【０００３】
【発明が解決しようとする課題】ＳｉＣ半導体に上述のように電極を形成する場合、ｎ型ＳｉＣに対してはＮｉが用いられる。真空蒸着後の熱処理によりＳｉとＮｉとの化合物を生成することによりオーム性接合が形成できるが、ＣはＮｉに対して固溶量が少なく、またＣとＮｉは化合物を形成しない。このため、半導体／電極界面にＣが混入することによりコンタクト抵抗が高く半導体素子として使用することは困難である。また、Ｎｉ中はＣの拡散係数が小さく半導体／電極界面からＣを排出するために1100℃前後の高温が必要である。一方、ｐ型ＳｉＣに対してはオーム性電極としてＡｌおよびＡｌ合金が用いられる。ＡｌおよびＡｌ合金は熱処理の際の耐熱性に問題がある。また、熱処理中にＮｉ，ＡｌとＳｉＣとの膨張率の違いから電極の剥離が起こる。本発明は低コンタクト抵抗の信頼性の高いオーミック電極を実現し高電圧，大電流および高温において信頼性の高い炭化珪素半導体素子を提供することを目的とする。
【０００４】
【課題を解決するための手段】本発明は、ＳｉＣ単結晶上に低コンタクト抵抗かつ信頼性の高いオーム性電極を形成するために炭化珪素単結晶表面に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を積層または、炭化珪素単結晶表面に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層と任意の金属層を積層してオーム性電極としたものである。特に、高不純物濃度の炭化珪素単結晶上に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を積層

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してオーム性電極とすることによりコンタクト抵抗は低くなる。また、高不純物濃度の炭化珪素単結晶表面に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層と任意の金属層を積層しオーム性接合を得ても同様にコンタクト抵抗は低くなる。ここで用いる金属には、Ｔｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中から少なくとも一種類の金属を含む合金を選択することが適当である。Ｔｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中からの一種類の金属の合金、または一種類の金属の積層膜を炭化珪素単結晶上に積層した後に熱処理することにより合金／半導体界面に金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を形成することも可能である。また、熱処理の際の酸化防止のために前記金属の中から少なくとも一種類の金属からなる合金層上に酸化しにくいＡｕ，Ｐｔ，Ｐｄ，Ｎｉ，Ｃｕなどの金属、またはＴｉ－Ａｌ，Ｎｉ－Ａｌ系合金などを少なくとも一層積層後熱処理を行うことも有効である。また、外部回路との接続のためにオーム性電極上にＡｌ，Ａｕ，Ｃｕ，Ｎｉなどの低抵抗金属を積層することもある。また、炭化珪素単結晶表面にＴｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中からの一種類の金属をイオン注入した後に熱処理を行い金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を形成しオーミック電極を得ることも可能である。また、上記の低コンタクト抵抗を持つ電極構造を用いた炭化珪素半導体素子，半導体回路は高電圧，大電流および高温の使用において高信頼性を有する。

【０００５】

【作用】低抵抗である金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を炭化珪素単結晶上に形成しオーム性電極として用いることにより低いコンタクト抵抗が得られらた。また、金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を不純物濃度が10^{18}／cm^3 以上である高不純物濃度の炭化珪素単結晶上に積層することによりトンネル効果のために更に低コンタクト抵抗のオーム性接合が得られた。電極構造上に任意の一種類の金属を積層した場合も同様に低コンタクト抵抗のオーム性接合が得られた。これらの電極構造に用いる金属元素は珪化物，炭化物ともに安定相として存在するＴｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中から選択する。また、金属の中から少なくとも一種類の金属を用いた合金を炭化珪素単結晶上に積層した後に熱処理を加えることにより低抵抗である金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層を金属／半導体界面に形成することが可能ある。また、これらの、金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層は炭化珪素に熱膨張率が近いので熱処理の際に炭化珪素から剥がれることはない。また、高温での使用においても劣化することはない。以上の理由により金属を用いることにより熱処理により確実に低コンタクト抵抗のオーム性電極が得られる。また、Ｔｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗは活性な金属であるので熱処理の際に電極表面に高抵抗の酸化物層が形成されることがあるが、金属の少なくとも一種類の金属を含む合金を炭化珪素単結晶上に積層した上に酸化しにくいＡｕ，Ｐｔ，Ｐｄ，Ｎｉ，Ｃｕなどの金属、またはＴｉ－Ａｌ，Ｎｉ－Ａｌ系合金などを少なくとも一層キャップメタルとして積層後熱処理を行うことにより、電極表面の酸化を避けて確実に低コンタクト抵抗のオーム性電極が得られる。また、Ｔｉ，Ｖ，Ｃｒ，Ｚｒ，Ｎｂ，Ｍｏ，Ｈｆ，Ｔａ，Ｗの中からの一種類の金属をイオン注入にした後に熱処理を行うことにより金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層の形成が可能である。この際イオン注入条件を適当に選択し金属元素の打ち込み深さを制御することにより金属珪化物，金属炭化物及び金属，珪素，炭素からなる複合化合物の複数種類を含む層の厚さの制御が容易に実現できた。以上の手段により形成された炭化珪素半導体の電極構造上に電気抵抗の低いＡｌ，Ｃｕ，Ａｕ，Ｎｉなどを積層することにより外部回路と容易に接続可能であった。また、これらの低コンタクト抵抗の電極構造を有した炭化珪素半導体素子は高電圧，大電流用に適し、高い信頼性を示した。また、これらの半導体素子を用いた回路は高電圧，大電流制御において同様に優れた信頼性を示した。

【０００６】

【実施例】

（実施例１）図２は本発明の実施例の一つを示す。炭化珪素単結晶１１上にスパッタ法によりタングステン珪化物（ＷＳｉｘ），タングステン炭化物(ＷＣｙ)の混合相よりなる層２１を２００ｎｍ積層した後に10^{-8}Torrの真空雰囲気において１０００℃の熱処理を行った。このようにして得られた電極は図３に示すようにオーム性を示した。図４はｎ型ＳｉＣの不純物濃度(Ｎ)に対するコンタクト抵抗（Ｒｃ）を示している。特に、高不純物濃度域において低抵抗のオーム性接合が得られた。図５に示すようにＡｌ層５１を２００ｎｍタングステン珪化物，タングステン炭化物の混合相からなる層２１上に積層することによりＡｌワイヤ５２により容易に外部回路と接続が可能になった。

【０００７】（実施例２）図６（ａ）に示すように炭化珪素単結晶１１上に真空蒸着によりＴｉ層１３を２００ｎｍ積層した後に10^{-8}Torrの真空雰囲気において１０００℃の熱処理を行った。熱処理により図１（ｂ）に示すように炭化珪素単結晶１１，チタン珪化物（ＴｉＳｉｘ），チタン炭化物（ＴｉＣｙ）の混合相からなる層１２，Ｔｉ層１３の積層構造が得られた。図７に熱処理温

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度に対する接合のＩ－Ｖ特性を示す。図８に熱処理温度Ｔａによるコンタクト抵抗Ｒｃの変化を示す。高温での熱処理によりＴｉＳｉｘ，ＴｉＣｙの混合相からなる層１２が均質に形成されるために低コンタクト抵抗のオーム性電極が得られた。図９(ａ)に示すようにＳｉＣ単結晶１１上に真空蒸着によりＴｉ層１３を２００ｎｍ、白金Ｐｔ層９１を２００ｎｍ積層した後に10^{-8}Torrの真空雰囲気およびＡｒフロー中において熱処理を行った。各雰囲気でのコンタクト抵抗Ｒｃに電極自身の抵抗を加えた見かけのコンタクト抵抗Ｒｃ′の熱処理温度Ｔａに対する変化を図１０に示す。ＳｉＣにＴｉ層のみを積層した電極はＡｒフロー中においては電極表面の酸化のために高温でＲｃ′が増大する。一方、ＳｉＣ上のＴｉ層上にキャップメタルとしてＰｔ層を積層した電極は各雰囲気において低抵抗のオーム性電極が実現できた。

【０００８】（実施例３）図１１に示すように炭化珪素単結晶１１上にスパッタ法によりタングステン－銅（Ｗ－Ｃｕ）合金層１１１を２００ｎｍ積層した後に10^{-8}Torrの真空雰囲気において１０００℃の熱処理を行った。熱処理により図１２に示すようにＳｉＣ単結晶１１，ＷＳｉｘ，ＷｉＣｙの混合相からなる層２１，Ｗ－Ｃｕ合金層１１１の積層構造が得られた。この電極は低コンタクト抵抗のオーム性を示した。

【０００９】（実施例４）図１３に示すようにｎ型酸化珪素層１２１表面に１２００℃で熱処理をすることにより酸化膜１２２を形成した後に弗酸エッチングによりパターンを形成した。イオン注入により加速電圧４００ｋｅＶで窒素を注入した後に１６００℃の熱処理で回復を行い高不純物濃度であるn^+層１２３を形成した（図１４（ａ））。n^+層の不純物濃度は$10^{19}/cm^3$であった。真空蒸着によりチタン層１３を２００ｎｍ積層した後に１０００℃で熱処理を行い金属／高不純物濃度半導体界面にＴｉＳｉｘ，ＴｉＣｙの混合相からなる層１２が形成することにより低コンタクト抵抗のオーム性電極を選択的に得ることができた（図１４（ｂ））。

【００１０】（実施例５）図１３に示すようにイオン加速機によりチタンを加速電圧４００keV でＳｉＣ単結晶１１表面に打ち込んだ。10^{-8}Torrの真空雰囲気で１８００℃で熱処理することにより図１４（ａ）に示すようにＳｉＣ単結晶１１表面にＴｉＳｉｘ，ＴｉＣｙの混合相からなる層１２が形成される。この後にＡｌ層５１を２００ｎｍを積層することにより低コンタクト抵抗のオーム性電極が形成可能であった。また、図に示すようにＳｉＣ単結晶上に酸化雰囲気熱処理により酸化膜をマスクとして形成することにより選択的にオーム性電極の形成が可能である。

【００１１】（実施例６）図１７に本発明による電極構造を具備した炭化珪素ＭＯＳ型電界効果トランジスタの断面模式図を示す。酸化珪素層１２１には炭化珪素を１２００℃の酸化雰囲気で熱処理することにより形成した酸化珪素膜を用いた。また、ゲート電極１４２には他結晶炭化珪素を用いた。

【００１２】

【発明の効果】本発明によれば、炭化珪素単結晶上に金属硅化物，金属炭化物、または複合化合物を含む層を設けることにより低抵抗のオーム性電極が形成できた。また炭化珪素と電極との熱膨張率の差が小さいので低コンタクト抵抗の信頼性の高いオーム性電極を具備した高電圧，大電流および高温で信頼性の高い炭化珪素半導体素子を得ることがでる。

【図面の簡単な説明】

【図１】炭化珪素半導体の電極構造を示す断面図。

【図２】炭化珪素半導体の電極構造を示す断面図。

【図３】図１に示す炭化珪素半導体の電極構造のＩ－Ｖ特性図。

【図４】図１に示す炭化珪素半導体の電極構造の炭化珪素単結晶の不純物濃度に対するコンタクト抵抗の変化の説明図。

【図５】炭化珪素半導体のオーム性電極形成方法の説明図。

【図６】炭化珪素半導体のオーム性電極形成方法の説明図。

【図７】図６に示す炭化珪素半導体の電極構造のＩ－Ｖ特性の熱処理温度依存性の説明図。

【図８】図６に示す炭化珪素半導体の電極構造のコンタクト抵抗の熱処理温度依存性の説明図。

【図９】炭化珪素半導体のオーム性電極形成方法の説明図。

【図１０】図６，図９に示す炭化珪素半導体の電極構造の熱処理雰囲気による見かけのコンタクト抵抗の熱処理温度依存性の説明図。

【図１１】炭化珪素半導体のオーム性電極形成方法の説明図。

【図１２】炭化珪素半導体のオーム性電極形成方法の説明図。

【図１３】炭化珪素半導体のオーム性電極形成方法の説明図。

【図１４】炭化珪素半導体のオーム性電極形成方法の説明図。

【図１５】炭化珪素半導体のオーム性電極形成方法の説明図。

【図１６】炭化珪素半導体のオーム性電極形成方法の説明図。

【図１７】本発明による電極構造を具備した電解効果型トランジスタの断面図。

【符号の説明】

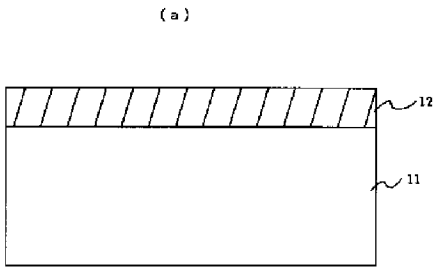
１１…炭化珪素単結晶、１２…チタン珪化物，チタン炭化物の混合相からなる層、１３…チタン層２１タングステン珪化物，タングステン炭化物の混合相よりなる層、５１…アルミ層、５２…アルミワイヤ、９１…白金層、

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１１１…タングステン－銅合金層、１２１…酸化珪素層、１３１…ｎ型炭化珪素単結晶、１３２…高濃度ｎ型炭化珪素単結晶、１４１…ｐ型炭化珪素単結晶、１４２…ゲート電極。

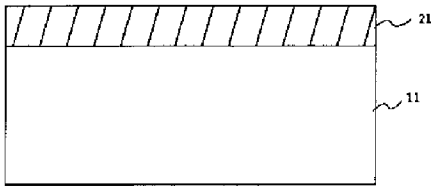
【図１】

図 1



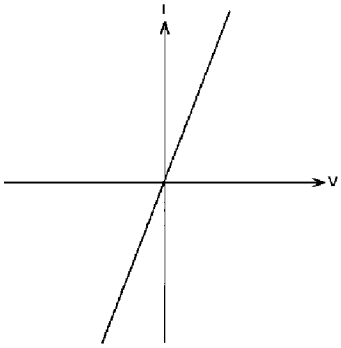
【図２】

図 2



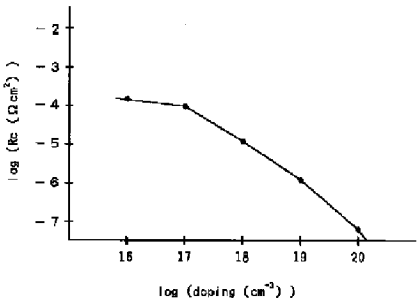
【図３】

図 3



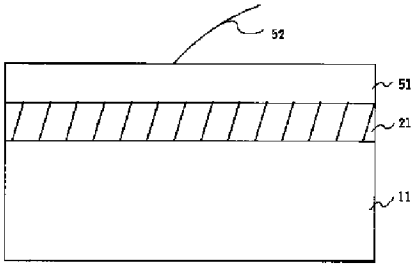
【図４】

図 4



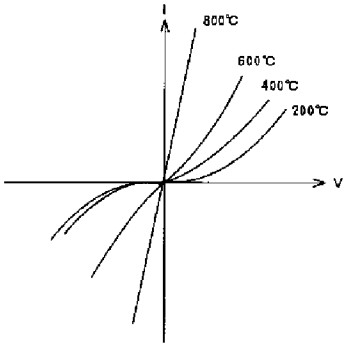
【図５】

図 5



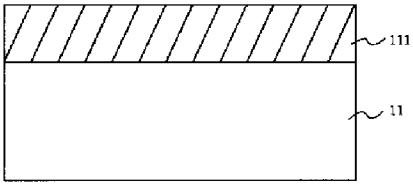
【図７】

図 7



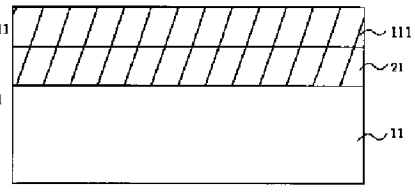
【図１１】

図 11



【図１２】

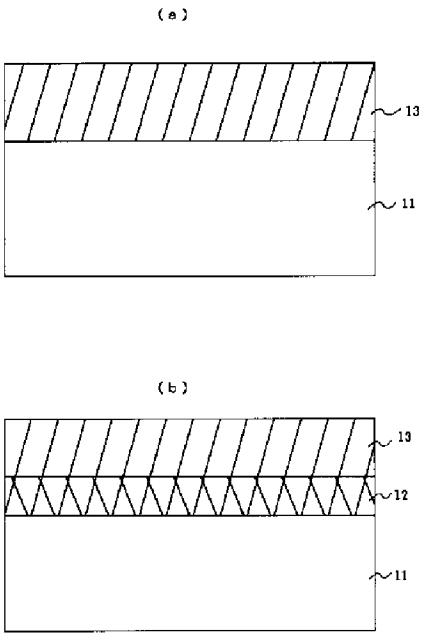
図 12



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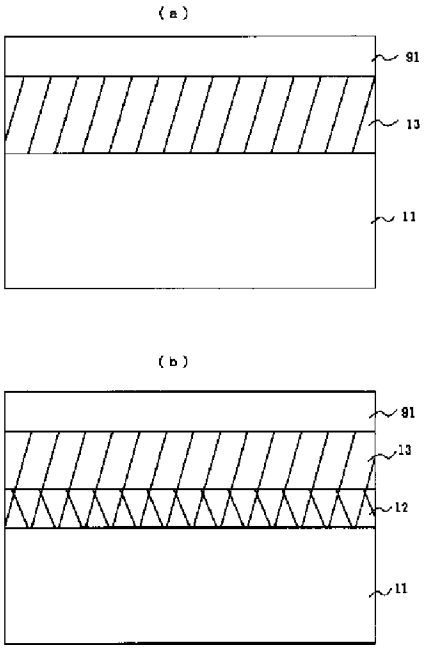
【図6】

図 6



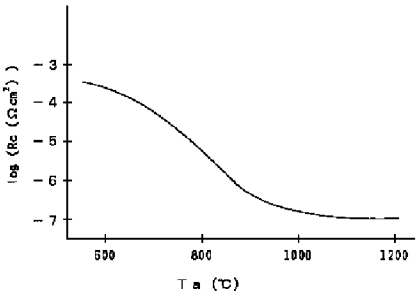
【図9】

図 9



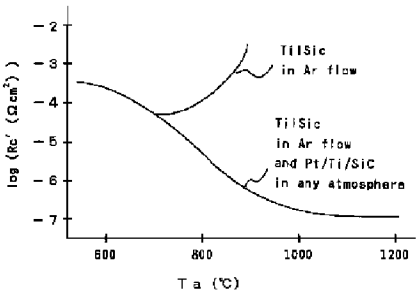
【図8】

図 8



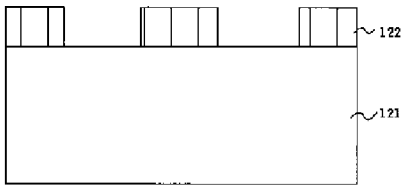
【図10】

図 10



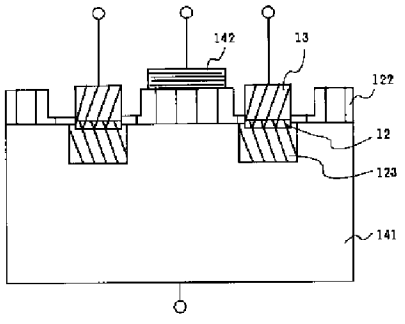
【図13】

図 13



【図17】

図 17

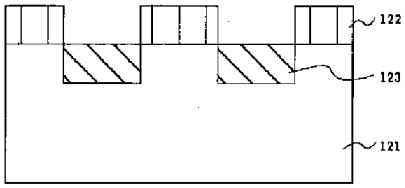


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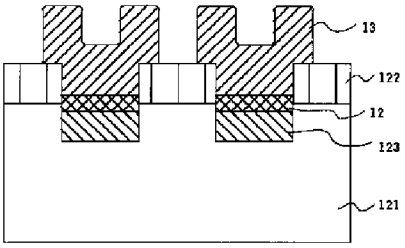
【図14】

図 14

(a)



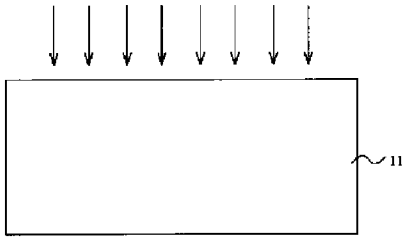
(b)



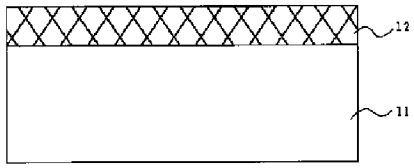
【図15】

図 15

(a)



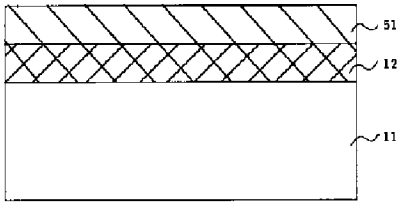
(b)



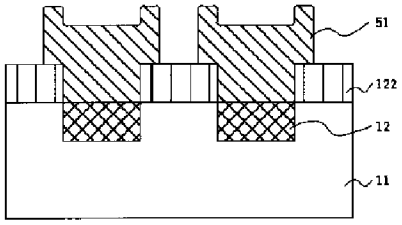
【図16】

図 16

(a)



(b)



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フロントページの続き

(72)発明者　八尾　勉
茨城県日立市大みか町七丁目１番１号　株
式会社日立製作所日立研究所内

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JPH0864800A SILICON CARBIDE SEMICONDUCTOR DEVICE

Applicants: HITACHI LTD

Inventors: KAWASE DAISUKE,KOZONO YUZO,ONO TOSHIYUKI,YAO TSUTOMU

Classifications:

IPC ***H01L21/203; H01L21/28; H01L29/43;*** (IPC1-7): H01L21/203; H01L21/28; H01L29/43;

CPC **H01L21/0485 (EP);**

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Publication: JPH0864800A·1996-03-08

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SILICON CARBIDE SEMICONDUCTOR DEVICE

Abstract

PURPOSE: To realize an ohmic electrode which has a low contact resistance and high reliability so as to obtain a silicon carbide semiconductor device which has a high operating voltage, large operating current, and is excellent in reliability by a method wherein a composite compound composed of low-resistance metal silicide, metal carbide, metal, silicon, and carbon is formed on a silicon carbide single crystal. CONSTITUTION: A mixed-phase layer 12 of titanium silicide and titanium carbide is formed on a silicon carbide single crystal 11, and furthermore a titanium layer 13 is laminated thereon to serve as an ohmic electrode. By this setup, an ohmic electrode of low contact resistance and high reliability can be obtained. Furthermore, as silicon carbide and the electrode have small thermal expansion coefficient, a silicon carbide semiconductor device which has a high operating voltage, large operating current, excellent in reliability at a high temperature, and equipped with an ohmic electrode of low contact resistance and high reliability can be obtained.

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DESCRIPTION JPH0864800

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a silicon carbide semiconductor device.

[0002]

A conventional ohmic electrode formed on a silicon carbide (SiC) semiconductor is a eutectic of nickel (Ni) for n-type SiC and aluminum (Al) and silicon (Si) for a p-type semiconductor. After vacuum deposition of each material, heat treatment was performed to obtain ohmic bonding (J. Electrochem. Soc., Vol. 135, p.359.). SiC has many crystal systems and has a band gap of 2.2 to 3.3 electron volts depending on the crystal structure. Further, SiC is a material that is extremely stable thermally, chemically and mechanically, is rare as a wide-gap semiconductor, and stably exists in both p-type and n-type. Therefore, an element in which an electrode for electrically connecting to an external circuit is formed on a SiC single crystal is expected to be applied to a large power element, a high temperature operation element, a radiation resistant element, a photoelectric conversion element and various other electronic technical fields. ..

[0003]

When forming an electrode on a SiC semiconductor as described above, Ni is used for n-type SiC. An ohmic bond can be formed by forming a compound of Si and Ni by heat treatment after

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vacuum vapor deposition, but C has a small solid solution amount with respect to Ni, and C and Ni do not form a compound. Therefore, since C is mixed in the semiconductor / electrode interface, the contact resistance is high and it is difficult to use it as a semiconductor element. Further, the diffusion coefficient of C in Ni is small, and a high temperature of about 1100 ° C. is required to discharge C from the semiconductor / electrode interface. On the other hand, for p-type SiC, Al and Al alloy are used as the ohmic electrode. Al and Al alloys have a problem in heat resistance during heat treatment. Further, during heat treatment, peeling of the electrode occurs due to the difference in expansion coefficient between Ni, Al and SiC. An object of the present invention is to provide a highly reliable ohmic electrode having a low contact resistance and to provide a highly reliable silicon carbide semiconductor device at high voltage, large current and high temperature.

[0004]

The present invention provides a metal silicide, a metal carbide and a metal silicide on the surface of a silicon carbide single crystal in order to form an ohmic electrode having low contact resistance and high reliability on a SiC single crystal. A layer containing a plurality of kinds of composite compounds composed of metal, silicon, and carbon is laminated, or a layer containing a plurality of kinds of composite compounds composed of metal silicide, metal carbide and metal, silicon, and carbon is formed on the surface of a silicon carbide single crystal. This is an ohmic electrode formed by laminating metal layers. In particular, the contact resistance is lowered by stacking a layer containing a plurality of kinds of metal silicides, metal carbides, and complex compounds composed of metal, silicon, and carbon on a silicon carbide single crystal having a high impurity concentration to form an ohmic electrode. .. Also, even if a layer containing a plurality of kinds of metal silicides, metal carbides and composite compounds composed of metal, silicon, and carbon and an arbitrary metal layer are laminated on the surface of a high-concentration silicon carbide single crystal, an ohmic bond is obtained. The contact resistance is low. As the metal used here, it is suitable to select an alloy containing at least one metal selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta and W. An alloy of one kind of metal selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta and W, or a laminated film of one kind of metal is laminated on the silicon carbide single crystal and then heat-treated. It is also possible to form a layer containing a plurality of kinds of a metal silicide, a metal carbide, and a composite compound composed of metal, silicon, and carbon at the alloy / semiconductor interface. Further, in order to prevent oxidation during heat treatment, a metal such as Au, Pt, Pd, Ni, Cu or the like which is hard to oxidize on the alloy layer made of at least one of the above metals, or Ti-Al, Ni- It is also effective to perform heat treatment after laminating at least one layer of Al-based alloy or the like. In addition, a low resistance metal such as Al, Au, Cu or Ni may be laminated on the ohmic electrode for connection with an external circuit. In addition, a metal silicide, a metal carbide and a metal are heat treated by ion-implanting one kind of metal selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta and W on the

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surface of the silicon carbide single crystal. It is also possible to obtain an ohmic electrode by forming a layer containing a plurality of kinds of composite compounds composed of silicon and carbon. Further, the silicon carbide semiconductor device and semiconductor circuit using the above electrode structure having a low contact resistance have high reliability in use at high voltage, large current and high temperature.

[0005]

A low contact is obtained by forming a layer containing a low resistance metal silicide, metal carbide and a plurality of kinds of composite compounds composed of metal, silicon and carbon on a silicon carbide single crystal and using it as an ohmic electrode. The resistance was obtained. Further, the tunnel effect is obtained by stacking a layer containing a plurality of kinds of metal silicide, metal carbide, and a complex compound of metal, silicon, and carbon on a high-impurity-concentration silicon carbide single crystal having an impurity concentration of 10 18 / cm 3 or more. Because of this, an ohmic contact with even lower contact resistance was obtained. In the case where any one kind of metal was laminated on the electrode structure, the ohmic contact with low contact resistance was similarly obtained. The metal element used for these electrode structures is selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta, and W, which exist as stable phases in both silicide and carbide. Further, a metal silicide, a metal carbide, and a composite compound of metal, silicon, and carbon, which have low resistance, are obtained by stacking an alloy using at least one kind of metal on a silicon carbide single crystal and then applying heat treatment. It is possible to form a layer containing a plurality of types of the above at the metal / semiconductor interface. Further, these layers containing a plurality of kinds of metal silicides, metal carbides, and composite compounds composed of metals, silicon, and carbon have a coefficient of thermal expansion close to that of silicon carbide, and therefore do not peel off from silicon carbide during heat treatment. Moreover, it does not deteriorate even when used at high temperatures. For the above reasons, by using a metal, an ohmic electrode having a low contact resistance can be surely obtained by heat treatment. Further, since Ti, V, Cr, Zr, Nb, Mo, Hf, Ta and W are active metals, a high resistance oxide layer may be formed on the electrode surface during heat treatment. An alloy containing at least one kind of metal is laminated on a silicon carbide single crystal, and a metal such as Au, Pt, Pd, Ni, Cu which is difficult to oxidize, or a Ti-Al, Ni-Al based alloy or the like is capped at least one layer. By performing a heat treatment after stacking as a metal, an ohmic electrode having a low contact resistance can be reliably obtained while avoiding oxidation of the electrode surface. In addition, a metal silicide, a metal carbide and a metal, silicon, carbon can be obtained by performing heat treatment after ion implantation of one kind of metal selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta and W. It is possible to form a layer containing a plurality of kinds of the composite compound consisting of. At this time, it is easy to control the thickness of the layer containing a plurality of kinds of metal silicides, metal carbides, and composite compounds of metal, silicon, and carbon by appropriately

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selecting the ion implantation conditions and controlling the implantation depth of the metal element. Was realized.

By stacking Al, Cu, Au, Ni or the like having a low electric resistance on the electrode structure of the silicon carbide semiconductor formed by the above means, it was possible to easily connect to an external circuit. In addition, these silicon carbide semiconductor devices having an electrode structure with low contact resistance are suitable for high voltage and large current, and have high reliability. In addition, circuits using these semiconductor devices also showed excellent reliability in high voltage and large current control.

[0006]

(Embodiment 1) FIG. 2 shows an embodiment of the present invention. A layer 21 made of a mixed phase of tungsten silicide (WSix) and tungsten carbide (WCy) having a thickness of 200 nm was laminated on the silicon carbide single crystal 11 by a sputtering method, and then heat treatment was performed at 1000 ° C. in a vacuum atmosphere of 10 −8 Torr. The electrode thus obtained exhibited ohmic properties as shown in FIG. FIG. 4 shows the contact resistance (Rc) with respect to the impurity concentration (N) of n-type SiC. In particular, a low resistance ohmic junction was obtained in the high impurity concentration region. As shown in FIG. 5, by stacking the Al layer 51 on the layer 21 composed of a mixed phase of 200 nm tungsten silicide and tungsten carbide, it became possible to easily connect to an external circuit by the Al wire 52.

[0007]

(Example 2) As shown in FIG. 6 (a), a Ti layer 13 having a thickness of 200 nm was deposited on a silicon carbide single crystal 11 by vacuum evaporation, and then heat treatment was performed at 1000 ° C. in a vacuum atmosphere of 10 −8 Torr. .. By the heat treatment, as shown in FIG. 1B, a laminated structure of a silicon carbide single crystal 11, a layer 12 composed of a mixed phase of titanium silicide (TiSix) and titanium carbide (TiCy), and a Ti layer 13 was obtained. FIG. 7 shows the IV characteristics of the junction with respect to the heat treatment temperature. FIG. 8 shows changes in the contact resistance Rc depending on the heat treatment temperature Ta. An ohmic electrode having a low contact resistance was obtained because the layer 12 composed of a mixed phase of TiSix and TiCy was uniformly formed by heat treatment at a high temperature. As shown in FIG. 9A, a Ti layer 13 having a thickness of 200 nm and a platinum Pt layer 91 having a thickness of 200 nm were laminated on the SiC single crystal

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11 by vacuum deposition, and then heat treatment was performed in a vacuum atmosphere of 10 −8 Torr and an Ar flow. FIG. 10 shows changes in the apparent contact resistance Rc′ obtained by adding the resistance of the electrode itself to the contact resistance Rc in each atmosphere with respect to the heat treatment temperature Ta. In the electrode in which only the Ti layer is laminated on SiC, Rc 'increases at high temperature due to oxidation of the electrode surface during Ar flow. On the other hand, an electrode in which a Pt layer as a cap metal was laminated on a Ti layer on SiC was able to realize an ohmic electrode with low resistance in each atmosphere.

[0008]

(Embodiment 3) As shown in FIG. 11, a tungsten-copper (W-Cu) alloy layer 111 having a thickness of 200 nm is formed on a silicon carbide single crystal 11 by a sputtering method, and then 1000 in a vacuum atmosphere of 10 -8 Torr. Heat treatment at ° C was performed. As a result of the heat treatment, as shown in FIG. 12, a laminated structure of a SiC single crystal 11, a layer 21 composed of a mixed phase of WSix and WiCy, and a W—Cu alloy layer 111 was obtained. This electrode exhibited low contact resistance and ohmic characteristics.

[0009]

Example 4 As shown in FIG. 13, the surface of the n-type silicon oxide layer 121 was heat-treated at 1200 ° C. to form an oxide film 122, and then a pattern was formed by etching with hydrofluoric acid. After implanting nitrogen at an accelerating voltage of 400 keV by ion implantation, recovery was performed by heat treatment at 1600 ° C. to form an n + layer 123 having a high impurity concentration (FIG. 14A). The impurity concentration of the n @ + layer was 10 @ 19 / cm @ 3. Select a low contact resistance ohmic electrode by stacking a titanium layer 13 to a thickness of 200 nm by vacuum vapor deposition and then performing heat treatment at 1000 ° C. to form a layer 12 composed of a mixed phase of TiSix and TiCy at the metal / high impurity concentration semiconductor interface. Could be obtained (FIG. 14 (b)).

[0010]

(Example 5) As shown in FIG. 13, titanium was implanted into the surface of the SiC single crystal 11 at an acceleration voltage of 400 keV by an ion accelerator. By heat treatment at 1800 ° C. in a vacuum atmosphere of 10 −8 Torr, a layer 12 composed of a mixed phase of TiSix and TiCy

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is formed on the surface of the SiC single crystal 11 as shown in FIG. 14A. After that, an Al layer 51 having a thickness of 200 nm was laminated to form an ohmic electrode having a low contact resistance. Further, as shown in the drawing, an ohmic electrode can be selectively formed by forming an oxide film on a SiC single crystal by heat treatment in an oxidizing atmosphere using the oxide film as a mask.

[0011]

(Embodiment 6) FIG. 17 shows a schematic sectional view of a silicon carbide MOS field effect transistor having an electrode structure according to the present invention. As the silicon oxide layer 121, a silicon oxide film formed by heat-treating silicon carbide in an oxidizing atmosphere at 1200 ° C. was used. Further, other crystalline silicon carbide was used for the gate electrode 142.

[0012]

According to the present invention, a low resistance ohmic electrode can be formed by providing a layer containing a metal silicide, a metal carbide or a composite compound on a silicon carbide single crystal. Further, since the difference in the coefficient of thermal expansion between silicon carbide and the electrode is small, it is possible to obtain a highly reliable silicon carbide semiconductor element equipped with a highly reliable ohmic electrode having a low contact resistance at high voltage, large current and high temperature. ..

[0013]
Brief description of the drawings

[0014]
1 is a cross-sectional view showing the electrode structure of the silicon carbide semiconductor.

[0015]
2 is a cross-sectional view showing the electrode structure of the silicon carbide semiconductor.

[0016]

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3 is an IV characteristic diagram of the electrode structure of the silicon carbide semiconductor shown in FIG.

[0017]
4 is an explanatory view of a change in contact resistance with respect to the impurity concentration of the silicon carbide single crystal of the electrode structure of the silicon carbide semiconductor shown in FIG.

[0018]
5 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0019]
6 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0020]
7 is an explanatory diagram of the heat treatment temperature dependence of the IV characteristics of the electrode structure of the silicon carbide semiconductor shown in FIG.

[0021]
8 is an explanatory diagram of heat treatment temperature dependence of the contact resistance of the electrode structure of the silicon carbide semiconductor shown in FIG.

[0022]
9 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0023]
10 is an explanatory view of the heat treatment temperature dependence of the apparent contact resistance depending on the heat treatment atmosphere of the electrode structure of the silicon carbide semiconductor shown in FIG. 6 and FIG. 9.

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[0024]
11 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0025]
12 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0026]
13 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0027]
14 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0028]
15 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0029]
16 is an explanatory view of a method for forming an ohmic electrode of a silicon carbide semiconductor.

[0030]
17 is a cross-sectional view of a field effect transistor having an electrode structure according to the present invention.

[0031]
Explanation of symbols

[0032]
11 ... Silicon carbide single crystal, 12 ... Layer composed of mixed phase of titanium silicide and

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titanium carbide, 13 ... Titanium layer 21 Layer composed of mixed phase of tungsten silicide and tungsten carbide, 51 ... Aluminum layer, 52 ... Aluminum wire, 91 ... Platinum layer, 111 ... Tungsten-copper alloy layer, 121 ... Silicon oxide layer, 131 ... N-type silicon carbide single crystal, 132 ... High concentration n-type silicon carbide single crystal, 141 ... P-type silicon carbide single crystal, 142 ... Gate electrode.

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CLAIMS JPH0864800

1.
A silicon carbide semiconductor device comprising an ohmic electrode formed by laminating a layer containing a plurality of kinds of a metal silicide, a metal carbide, and a composite compound composed of metal, silicon, and carbon on a silicon carbide single crystal.

2.
A silicon carbide semiconductor device characterized in that an ohmic electrode is formed by laminating a layer containing a plurality of kinds of metal silicides, metal carbides and composite compounds composed of metal, silicon and carbon on a silicon carbide single crystal and an arbitrary metal layer. .

3.
On a silicon carbide single crystal with an impurity concentration of 1018 / cm3 or more, a layer containing a plurality of kinds of metal silicides, metal carbides and complex compounds consisting of metal, silicon, and carbon and an arbitrary metal layer are laminated to form an ohmic electrode. A silicon carbide semiconductor device characterized by the above.

4.
A metal silicide containing at least one metal selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta, and W in a silicon carbide single crystal, a metal carbide, and a composite compound composed of the metal, silicon, and carbon. A silicon carbide semiconductor device comprising a layer containing a plurality of types and an arbitrary one type of metal layer or alloy layer.

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5.

An alloy of one kind of metal selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta and W or a laminated film of one kind of metal is laminated on the silicon carbide single crystal and then heat-treated. / A silicon carbide semiconductor device characterized in that an ohmic electrode is formed by forming a layer containing a plurality of kinds of a metal silicide, a metal carbide and a composite compound composed of metal, silicon and carbon on a semiconductor interface.

6.

An alloy of one kind of metal selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta and W is deposited on the silicon carbide single crystal, or after one kind of metal is laminated, another metal layer or another layer is formed thereon. It is characterized in that an ohmic electrode is formed by forming a layer containing a plurality of kinds of metal silicides, metal carbides, and complex compounds consisting of metal, silicon, and carbon at the alloy / semiconductor interface by stacking metal alloy layers and then heat-treating And a silicon carbide semiconductor device.

7.

One kind of metal selected from Ti, V, Cr, Zr, Nb, Mo, Hf, Ta and W is ion-implanted on the surface of the silicon carbide single crystal, and then heat treatment is performed to perform metal silicide, metal carbide and metal, silicon, A silicon carbide semiconductor device, comprising: forming a layer containing a plurality of kinds of composite compounds made of carbon and then laminating one kind of metal.

8.

The silicon carbide semiconductor element according to claim 1, 2, 3, 4, 5, 6 or 7, wherein Al or Au is laminated on the electrode structure of the silicon carbide semiconductor.

9.

A diode comprising the electrode structure according to any one of claims 1 to 8.

10.

A thyristor having the electrode structure according to any one of claims 1 to 8.

11.

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A transistor comprising the electrode structure according to any one of claims 1 to 8.

12.

An electric circuit comprising the semiconductor element according to any one of claims 1 to 11.

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⑲日本国特許庁(JP)　⑪特許出願公開

⑫公開特許公報(A)　平1−186672

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H 01 L 29/48		H−7638−5F	
29/80		M−8122−5F	

審査請求　未請求　請求項の数 1　(全3頁)

㊹発明の名称　ショットキー接合構造

㉑特　願　昭63−7179

㉒出　願　昭63(1988)1月14日

㉗発明者　廣瀬　和之　東京都港区芝5丁目33番1号　日本電気株式会社内

㉑出願人　日本電気株式会社　東京都港区芝5丁目33番1号

㉔代理人　弁理士　内原　晋

明細書

発明の名称　ショットキー接合構造

特許請求の範囲

(1)金属とⅢ−Ⅴ族化合物半導体ショットキー接合構造において、上記金属と上記半導体との間に、上記半導体との化学結合エネルギーの大きな別種金属が1／10〜30原子層の厚さだけ形成されていることを特徴とするショットキー接合構造。

発明の詳細な説明

(産業上の利用分野)

本発明は半導体のショットキー障壁高さが制御可能なショットキー接合構造に関するものである。

(従来の技術)

単一金属を半導体と接触させた時のショットキー障壁の高さは、理想的には金属の仕事関数と半導体の電子親和力との差によって与えられるとされていた[フィジクス・オブ・セミコンダクター・デバイス(Physics of SemiconductorDevices, 1969年,John Wiley R Sons,Inc.)]。従って任意の半導体に対してショットキー障壁の高さを変化させる為には、仕事関数の異なる金属と接触させればよいはずであった。しかし、半導体の種類によっては、仕事関数の異なる金属を接触させても、フェルミレベルが一定値に固定(ピニング)され、ショットキー障壁の高さを変化させることの不可能なものもあった。

産業上の利用価値の高いⅢ−Ⅴ族半導体はその顕著な例であった[フィジカル・レビュー・レターズ(Phy.Rev.Lett.)第22巻, 1969年, 第1433ページ]。

(発明が解決しようとする問題点)

ショットキー障壁の高さは、例えば整流特性を向上させる為には高い方が良く、接触抵抗を低減させる為には低い方が良い。さらにはショットキー障壁の高さは、トランジスターのしきい値電圧を決定する重要な要素である。従って前述のように利用価値の高いⅢ−Ⅴ族化合物半導体におい

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て、ショットキー障壁の高さが制御不可能であることは、デバイス設計の上で大きなハンディとなっていた。

本発明の目的は、半導体のショットキー障壁の高さが制御可能なショットキー接合構造を提供することにある。

（問題点を解決するための手段）

本発明は、金属とⅢ－Ⅴ族化合物半導体ショットキー接合構造において、上記金属と上記半導体との間に、上記半導体との化学結合エネルギーの大きな別種金属が１／10～30原子層の厚さだけ形成されていることを特徴とする。

（作用）

本発明者は、金属／Ⅲ－Ⅴ族化合物半導体界面ではフェルミレベルがピニングされるか否かは厚さ１原子層程度の金属を接触させた時に決定されること（ジャーナル・オブ・バキューム・サイエンス・アンド・テクノロジー（J. Vac. Sci. Technol.）第17巻、1980年，第1019ページ）、また金属の仕事関数は層厚が１層程度ではバルク状態の値に達せずに層厚が30層程度になって初めてバルク状態の値に安定すること（ジャーナル・オブ・バキューム・サイエンス・アンド・テクノロジー（J. Vac. Sci. Technol.）第16巻，1979年，第1137ページ）に注目した。

そして、Ⅲ－Ⅴ族化合物半導体と接触した時にフェルミレベルをピニングしない金属が唯一種でも存在すれば、その金属をⅢ－Ⅴ族化合物半導体に１／10～30原子層だけ接触させ、ひき続いて任意の金属を30原子層以上接触させれば、その時形成されるショットキー接合の障壁高さは前者の金属の仕事関数にはよらず、後者の金属の仕事関数によって決定されるものと考えられる。

例えばＧａＡｓに対してそのフェルミレベルをピニングしない金属を探し求めたところ、Ｓｂがそのような金属であることが報告されていた（ジャーナル・オブ・バキューム・サイエンス・アンド・テクノロジー（J. Vac. Sci. Technol.）第Ａ４巻，1986年，第958 ページ）。

そこで、第１図に示すように清浄なＧａＡｓ基板１の上にＳｂ２を１原子層形成し、それにひき続いて任意の金属３を30Ａ以上形成したところ、ＳｂとＧａＡｓとの間の強い化学結合が急峻で安定した界面を保証し、その結果フェルミレベルのピニングを引き起こす原因と考えられている半導体中の欠陥の発生や金属／半導体間の相互拡散が抑制され、ショットキー障壁は固定した値ではなく金属の仕事関数によって決定されることが判明した。この様な効果はＧａＡｓと強く化学結合する他の金属、例えばＤｙやＳｃにおいても見いだされた。

以下、本発明の実施例を説明する。

実施例１

金属ＳｂとＧａＡｓ半導体を用いて本発明のショットキー接合構造を形成し、ショットキー障壁高さの金属の仕事関数に対する依存性を検討したところ、ショットキー障壁高さを大きな幅で制御することができた。実験はｎ型ＧａＡｓ（110）基板を超高真空内でへき開し、その表面に室温でＳｂを分子線エピタキシャル成長法によって１／10原子厚でけ蒸着した。ひき続いてその上に金属として例えばＡｕ，Ｐｄ，Ａｌ，Ｔｉを 500Ａ蒸着した。そして作製した試料に電極を取り付けた後にＣ－Ｖ測定法により評価し、ショットキー障壁高さを決定した。その結果ショットキー障壁高さは、この４種の金属において各々の仕事関数の差を反映して、1500ｍｅＶも変化した。この値は従来の障壁高さの変動幅の30倍にも達した。

実施例２

金属ＳｃとＩｎＰ半導体を用いて本発明のショットキー接合構造を形成し、ショットキー障壁高さの金属の仕事関数に対する依存性を検討したところ、ショットキー障壁高さを大きな幅で制御することができた。実験はｎ型ＩｎＰ（110）基板を超高真空内でへき開し、その表面に室温でＳｃを分子線エピタキシャル成長法によって30原子層だけ蒸着した。ひき続いてその上に各種金属としてＡｕ，Ｐｄ，Ａｌ，Ｍｎを各々1000Ａ蒸着した。そして作製した試料に電極を取り付けた後にＣ－Ｖ測定法により評価し、ショットキー障壁高さを

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決定した。その結果ショットキー障壁高さは、この種の金属においてそれぞれの仕事関数の差を反映して、1020ｍｅＶも変化した。この値は従来の障壁高さの変動幅の12倍にも達した。

実施例３

金属ＤｙとＧａＡｓ半導体を用いて本発明のショットキー接合構造を形成し、ショットキー障壁高さを測定したところ、ショットキー障壁高さを従来の構造と較べて大きく変化させることができた。実験はｎ型ＧａＡｓ（100)基板上に、室温で分子線エピタキシャル成長法によってＤｙを３原子層だけ蒸着した。ひき続いてその上にＡｌを1000Ａ蒸着した。そして作製した試料に電極を取り付け後にＣ－Ｖ測定法により評価し、ショットキー障壁高さを決定した。その結果ショットキー障壁高さは、従来のＡｌＩｎＧａＡｓ構造の 750ｍｅＶと較べて 150ｍｅＶ減少しフェルミレベルがピンニングされていないことが分った。

本実施例においては分子線エピタキシャル成長により化学結合の大きな金属としてＳｂ，Ｓｃ，ＤｙをＩｎＰ及びＧａＡｓ上に成長させた場合を示したが、本発明の効果は成長方法や金属の種類によるものではない。清浄なⅢ－Ⅴ族基板上に前記基板との化学結合力が大きいものであれば良い。またⅢ－Ⅴ族化合物としてはＩｎＰやＧａＡｓに限るものではなくＩｎＧａＡｓ，ＩｎＧａＰなどにも適用できる。.

（発明の効果）

以上説明したように本発明はⅢ－Ⅴ族化合物半導体ショットキー接合において、金属をⅢ－Ⅴ族化合物半導体表面上に形成する前に、Ⅲ－Ⅴ族化合物半導体との化学結合エネルギーの大きな別種金属を１／10～30原子層の厚さだけⅢ－Ⅴ族化合物半導体上に形成することによって、ショットキー障壁高さを固定した値ではなく、金属の仕事関数によって制御可能なものとする効果がある。

図面の簡単な説明

第１図は本発明によるショットキー接合構造を示す構造図である。

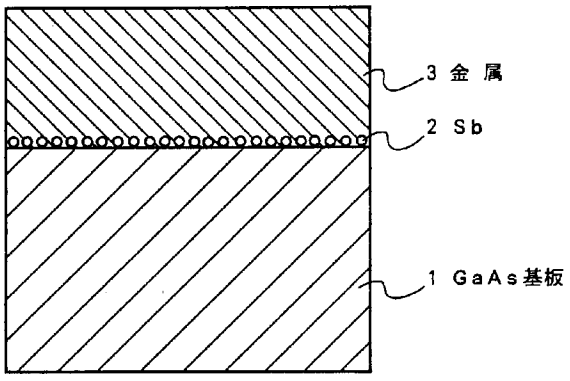
１…ＧａＡｓ

２…Ｓｂ

３…任意の金属

代理人　弁理士　内原　晋

第　１　図



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JPH01186672A SCHOTTKY JUNCTION STRUCTURE

Applicants: NEC CORP

Inventors: HIROSE KAZUYUKI

Classifications:
IPC ***H01L21/338; H01L29/47; H01L29/80; H01L29/812; H01L29/872;*** (IPC1-7): H01L29/48; H01L29/80;

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Published as: JPH01186672A

SCHOTTKY JUNCTION STRUCTURE

Abstract

PURPOSE:To make it possible to control the height of Schottky barrier by shaping a kind of metal having a large chemical combination energy with III-V compound semiconductor in a specified thickness before forming another kind of metal on the surface of III-V compound semiconductor. CONSTITUTION:Between metal 3 and III-V compound semiconductor 1, another kind of metal 2 having a large chemical combination energy with the semiconductor 1 is formed as thick as a 1/10-30atoms thick layer. Consequently, the strong chemical combination between the metal 2 and the semiconductor assures a sharp and stable interface. As a result, development of defects in the semiconductor 1 which is regarded to cause pinning of Fermi level is restrained and, therefore, the Schottky barrier is not a definite value but decided based on work function of the metal 2. The height of the Schottky barrier of the semiconductor 1 can be thereby controlled.

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DESCRIPTION JPH01186672

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a Schottky junction structure capable of controlling a semiconductor Schottky barrier height. (Prior Art) The height of the Schottky barrier when a single metal is brought into contact with a semiconductor is ideally given by the difference between the work function of the metal and the electron affinity of the semiconductor [Physics Of Semiconductor Devices (Physics of Sem1conductor Devices). 1969, John Wiley R5ons, Inc,)], so to change the height of the Schottky barrier for any semiconductor, it would have been necessary to contact it with a metal having a different work function. However, depending on the type of semiconductor, even if metals having different work functions are brought into contact with each other, the Fermi level is fixed (pinned) to a constant value, and it is impossible to change the height of the Schottky barrier. The IV group live conductor, which has a high industrial utility value, was a prominent example of this [Physical Review Letters (Phy, Rev, Lett), Volume 22, 1969, 1433 pages]. (Problems to be Solved by the Invention) The height of the Schottky barrier is preferably high in order to improve the rectifying characteristics, and low in order to reduce the contact resistance. Furthermore, the height of the Schottky barrier is an important factor that determines the threshold voltage of the transistor. Therefore, as described above, in the group V compound semiconductor having a high utility value, the fact that the height of the short key barrier is uncontrollable has been a great handicap in device design. An object of the present invention is to provide a Schottky junction structure in which the height of a semiconductor Schottky barrier can be controlled. (Means for Solving the Problems) In the present invention, in a metal- ■ -V compound semiconductor Schottky junction structure, another metal having a large chemical bond energy with the semiconductor is provided between the metal and the semiconductor. It is characterized in that it is formed by a thickness of 1/10 to 30 atomic layers. (Function) The inventor of the present invention determines whether or not the Fermi level is pinned at the metal / I [I-V group

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compound semiconductor interface] when a metal having a thickness of about 1 atomic layer is brought into contact (Journal Of Vacuum Science and Technology (J, Vac, Sci, Te-chnol,) Vol. 17, 1980, page 1019), and the work function of metals is in a bulk state when the layer thickness is 1 to about 1 degree. To reach the value in the bulk state only after the layer thickness reaches about 30 layers without reaching the value (Journal of Vacuum Science and Technology (J, Vac, Set, Technol) Vol. 16, 1979.

Attention was paid to page 1137). Then, if there is only one kind of metal that does not pin the Fermi level when it contacts with the (-V) compound semiconductor, the metal is contacted with the (-V) group compound semiconductor by 1/10 to 30 atomic layers, and then, continuously. It is considered that if any metal is brought into contact with 30 atomic layers or more, the barrier height of the Schottky junction formed at that time does not depend on the work function of the former metal but is determined by the work function of the latter metal. . For example, when searching for a metal that does not pin the Fermi level to GaAs, it was reported that sb was such a metal (Journal of Vacuum Science and Technology (J, Vac, Sci, (Technol,) Volume A4, 1986, page 958). Then, as shown in FIG. 1, one atomic layer of Sb2 was formed on a clean GaAs substrate 1, and subsequently, an arbitrary metal 3 of 30 A or more was formed. The strong chemical bond between sb and GaAs assures a steep and stable interface, and as a result suppresses the occurrence of defects in the semiconductor and the metal / semiconductor interdiffusion, which are considered to cause Fermi level pinning. And found that the Schottky barrier is determined by the work function of the metal, not a fixed value. Such an effect was also found in other metals that strongly chemically bond with GaAs, such as Dy and Sc. Hereinafter, the present invention will be described in detail. When the Schottky junction structure of the present invention was formed by using the supporting metal sb and the GaAs semiconductor, and the dependence of the Schottky barrier height on the work function of the metal was examined, the Schottky barrier height was wide. I was able to control it. In the experiment, an n-type GaAs (110) substrate was cleaved in an ultrahigh vacuum, and sb was vapor-deposited on the surface of the substrate at room temperature by a molecular beam epitaxial growth method with a 1/10 atomic thickness. Subsequently, metal such as Au, Pd, At, and Ti was vapor-deposited on the surface of the layer with 50 OA. After mounting the electrodes on the produced sample, the evaluation was made by the C- ■ measurement method to determine the Schottky barrier height. As a result, the Schottky barrier height also changed by 1500 meV, reflecting the difference in work functions of these four metals. This value reached 30 times the fluctuation width of the conventional barrier height. When the Schottky junction structure of the present invention was formed using the support metal Sc and InP semiconductor and the dependence of the Schottky barrier height on the work function of the metal was examined, the Schottky barrier height was controlled with a large width. We were able to.

In the experiment, an n-type InP (110) substrate was cleaved in an ultrahigh vacuum, and 30

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atomic layers of Sc was vapor-deposited on the surface of the substrate at room temperature by the molecular beam epitaxial growth method. Subsequently, various metals such as Au, Pd, AI, and Mn were vapor-deposited on each of them by 100 ports A. Then, after the electrodes were attached to the produced sample, the Schottky barrier height was determined by evaluation by the C-1 measurement method. As a result, the Schottky barrier height also changed by 1020 meV, reflecting the difference in work functions of these metals. This value reached 12 times the fluctuation width of the conventional barrier height. When the Schottky junction structure of the present invention was formed by using the support 1 metal 1) y and a GaAs semiconductor and the Schottky barrier height was measured, the Schottky barrier height was significantly changed as compared with the conventional structure. I was able to. In the experiment, three atomic layers of [) y were vapor-deposited on the n-type GaAs (100) substrate by the molecular beam epitaxial growth method at room temperature. Subsequently, 1000 A of AI was vapor-deposited thereon. Then, the electrodes were attached to the produced sample, which was later evaluated by the C-■ measurement method to determine the Schottky barrier height. As a result, it was found that the Schottky barrier height was reduced by 150 meV as compared with the conventional 75 Ime nGaAs laterally-equipped 75 R meV, and the Fermi level was not pinned. In this embodiment, Sb and Sc are used as the metal having a large chemical bond by the molecular beam epitaxial growth. The case where D and y are grown on InP and GaAs is shown, but the effect of the present invention does not depend on the growth method or the kind of metal. It is sufficient that the chemical bond strength with the above-mentioned substrate is large on a clean substrate. Further, (4) -V group compound is not limited to InP and GaAs (it can be applied to InGaAs, InGaP and the like. (Effect of the Invention) As described above, in the present invention, in the (1) -V group compound semiconductor Schottky junction, before the metal is formed on the (4) -V group compound semiconductor surface, it is chemically bonded to the II-V group compound semiconductor. By forming another metal having a large energy on the III-V group compound semiconductor by a thickness of 1/10 to 30 atomic layers, the Schottky barrier height can be controlled by the work function of the metal, not by a fixed value. There is an effect to do.

[0002]
Brief description of the drawings

[0003]

FIG. 1 is a structural diagram showing a Schottky junction structure according to the present invention.

1 ... GaAs2 ... sb3 ... arbitrary metal

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CLAIMS JPH01186672

1.
In the III-V compound semiconductor Schottky junction structure, another metal having a large chemical bond energy with the semiconductor is formed between the metal and the semiconductor in a thickness of 1/10 to 30 atomic layers. Schottky junction structure featuring.

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Complete if Known	
Application Number	16/847,878
Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	

Sheet	1	of	9	**Attorney Docket No:** 3771-0003-DC13

U.S. PATENT DOCUMENTS					
Examiner Initials*	**Cite No.[1]**	**Document Number** Number-Kind Code[2](if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of Cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		4845050	1989-07-04	Kim, et al.	
		6724088	2004-04-20	Jammy, et al.	
		7176483	2007-02-13	Grupp, et al.	
		9461167	2016-10-04	Grupp, et al.	
		9905691	2018-02-27	Grupp, et al.	
		10090395	2018-10-02	Grupp, et al.	
		20050093027	2005-05-05	Grupp; et al.	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T2**
		DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 79 pgs.	
		APPENDIX A1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	
		APPENDIX A2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 7 pgs.	

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Art Unit	2815
Examiner Name	

Sheet	2	of	9	**Attorney Docket No:** 3771-0003-DC13

		APPENDIX A3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 19 pgs.	
		APPENDIX A4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 21 pgs.	
		APPENDIX A6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	
		APPENDIX A7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 26 pgs.	
		APPENDIX A8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 28 pgs.	
		APPENDIX A10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 18 pgs.	
		APPENDIX B1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 41 pgs.	
		APPENDIX B2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 43 pgs.	

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Art Unit	2815
Examiner Name	

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		APPENDIX B3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 48 pgs.	
		APPENDIX B4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 48 pgs.	
		APPENDIX B5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 47 pgs.	
		APPENDIX B6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 32 pgs.	
		APPENDIX B7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 42 pgs.	
		APPENDIX B8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 41 pgs.	
		APPENDIX B10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 30 pgs.	
		APPENDIX C1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	

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Art Unit	2815
Examiner Name	

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		APPENDIX C2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	
		APPENDIX C3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 7 pgs.	
		APPENDIX C4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX C7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 4 pgs.	

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		APPENDIX D1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 16 pgs.	
		APPENDIX D2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 20 pgs.	
		APPENDIX D3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 14 pgs.	
		APPENDIX D4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 11 pgs.	
		APPENDIX D5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 16 pgs.	
		APPENDIX D6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 12 pgs.	
		APPENDIX D7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 22 pgs.	
		APPENDIX D8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	

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		APPENDIX D10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 21 pgs.	
		APPENDIX E1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
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		APPENDIX E10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX F1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 13 pgs.	
		APPENDIX F2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	
		APPENDIX F3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 11 pgs.	
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		APPENDIX F8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 17 pgs.	
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		De Bosscher, et al., The influence of silicide formation on the barrier height of Ti/Si MIS Schottky barriers, Semiconductor Sci., Tech., Vol. 1, 1986, pp. 376-382.	
		Defives, et al., Electrical behaviour and microstructural analysis of metal Schottky contacts on 4H-SiC, Microelec. Eng'g, Vol. 55, 2001, pp. 369-374.	
		Goodnick, et al., Effects of a thin SiO2 layer on the formation of metal-silicon contacts, Journal of Vacuum Sci. & Tech., Vol. 18, No. 3, Apr. 1981, pp. 949-954.	
		Schmidt, et al., Increased dependence of Schottky barrier height on metal work functions due to a thin-oxide layer, Journal of Vacuum Sci. & Tech., Vol. 6, No. 4, Jul./Aug. 1988, pp. 1436-1439.	
		Waldrop, et al., Schottky barrier height and interface chemistry of annealed metal contacts to alpha 6H-SiC: Crystal face dependence, Applied Physics Letters, Vol. 62, No. 21, May 24, 1993, pp. 2685-2687.	

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Attorney Docket No:	3771-0003-DC13

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☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-06-17
Name/Print	Tarek N. Fahmi	Registration Number	41,402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENDFEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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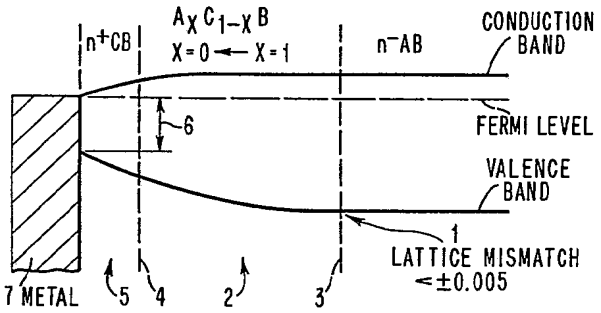
(71) Applicant: **International Business Machines Corporation, Armonk, N.Y. 10504 (US)**

(72) Inventor: **Woodall, Jerry McPherson, 336 Cherry Street, Bedford Hills New York 10507 (US)**

(74) Representative: **Hobbs, Francis John, IBM United Kingdom Patent Operations Hursley Park, Winchester Hants, SO21 2JN (GB)**

(54) Intermetallic semiconductor devices.

(57) An intermetallic semiconductor body (1) can be provided with an ohmic contact having a resistance of much less than 10^{-6} ohm cm^2 by introducing between the semiconductor body (1) and an external metal contact (7) an atomically compatible barrier-free graded layer (2, 5) of a semiconductor having at the interface with the external metal contact an energy gap width less than 0.5 electron volts. An ohmic contact for gallium arsenide can be provided by a graded region of indium gallium arsenide that decreases to indium arsenide at the interface with the external metal contact.



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INTERMETALLIC SEMICONDUCTOR DEVICES

This invention relates to intermetallic semiconductor devices.

A simple metal contact to a body of intermetallic semiconductor material exhibits a barrier to carrier flow which introduces resistance. Various ways of reducing the barrier to current flow at the surface of an intermetallic semiconductor have previously been proposed. One approach, exemplified by U.S. Patent No. 4,188,710 has been to reduce the barrier by the use of heavy doping at the surface of the device using materials such as germanium. Another approach is illustrated in U.S. Patent No. 3,984,261 wherein a substantially homogeneous layer of indium gallium arsenide is placed on a gallium arsenide semiconductor device. This structure, however, introduces another barrier which while smaller than the barrier at the surface still inhibits device performance.

The invention aims at providing a contact to intermetallic semiconductor material which substantially avoids any barrier to current flow.

A semiconductor device according to the invention, comprises a body of intermetallic semiconductor material provided with a contact, the contact comprising an external metallic layer and an intermediate region of semiconductor material atomically compatible with the body disposed between the metallic layer and the body, the device being characterised by the intermediate region having a graded composition such that the lattice and electron affinity of the intermediate region substantially match the lattice and electron affinity of the intermetallic semiconductor material at the interface between the intermediate region and the body and that there exists an energy gap of less than 0.5 electron volts at the interface between the intermediate region and the external metallic layer.

COMPLETE DOCUMENT

The invention will now be explained by way of example, with reference to the accompanying drawings, in which:-

FIG. 1 is an energy level diagram illustrating the conditions present in the low resistance ohmic contact of the invention;

FIG. 2 is a current-against-voltage graph illustrating the ohmic performance of the contact of the invention;

FIG. 3 is an energy level diagram illustrating the barrier to carrier flow present with intermetallic semiconductor metal contacts;

FIG. 4 is a current-against-voltage graph indicating the rectifying performance of the contact of FIG. 3;

FIG. 5 is an energy level diagram illustrating the effect of high doping at the interface of an intermetallic semiconductor metal contact;

FIG. 6 is a voltage-against-current graph indicating ohmic but high resistance performance of the contact of FIG. 5;

FIG. 7 is an energy level diagram illustrating a barrier present within an intermetallic device when the lattice constants of a semiconductor positioned between a metal contact and the intermetallic semiconductor are mismatched;

FIG. 8 is a current-against-voltage graph indicating rectifying performance of the contact of FIG. 7;

FIG. 9 is an energy level diagram illustrating a barrier present within an intermetallic device when lattice constants and electron affinities of a semiconductor positioned between a metal contact and the intermetallic semiconductor are matched and different respectively; and

FIG. 10 is a current-against-voltage graph of the contact of FIG. 9 indicating rectifying performance.

A low resistance ohmic contact to an intermetallic semiconductor can be provided by introducing between a metal external contact and the semiconductor an atomically compatible barrier-free semiconductor region with a graded band gap that decreases from the band gap of the intermetallic semiconductor to less than 0.5 electron volts at the interface with the metal external contact. An atomically compatible semiconductor will have an absolute fractional difference in lattice constants at the interface with the intermetallic semiconductor that is either no more than 0.005, or less than the amount necessary to cause misfit disclocation to form. The semiconductor will be atomically compatible with the intermetallic semiconductor if it can be doped to at least a level of $10^{19}/cm^3$ and there is an electron affinity difference between the intermetallic semiconductor and the semiconductor of the intermediate region at its interface with the intermetallic semiconductor that is not greater than 0.04 electron volts.

The ohmic contact structure comprises an external metal electrode separated from the body of an intermetallic semiconductor by an intermediate semiconductor region that serves to prevent barrier formation. In FIG. 1 the intermetallic semiconductor is designated 1 which may, for example, be a binary semiconductor designated AB, for example, the material gallium arsenide. The body 1 is shown as having an n-conductivity type. For illustration purposes the energy diagrams in the description will be drawn with n- as an example of one conductivity type, as is well known to those skilled in the art. The transition to the opposite conductivity type may readily be made.

An intermediate semiconductor region 2 is provided that, in essence, avoids a barrier at the surface where an external metal electrode is placed yet does not introduce an interface barrier where it joins the body 1.

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In accordance with the invention this is accomplished by providing a close lattice match and small electron affinity difference with the body 1, a small energy gap at the surface with the metal and a graded band gap in between. A graded region of a semiconductor is provided labelled 2. Where the body 1 is a binary semiconductor such as gallium arsenide, the semiconductor may be a ternary semiconductor such as GaInAs having two ingredients, A and B, in common with the binary semiconductor and may have the third ingredient C graded with respect to the first ingredient A such that the ingredient C is substantially absent, or in other words the material is GaAs, at the interface 3 with the body 1 thereby satisfying a barrier forming lattice mismatch requirement and the ingredient A is substantially absent, or in other words the material is InAs, at a line labelled 4.

In other words, on the other side of the line 4, in essence, the intermediate semiconductor will have become another binary semiconductor CB in a region labelled 5 and this semiconductor is such that the energy gap width 6 at an interface with the metal 7 is less than 0.5 electron volts and that it may be doped to at least $10^{19}/cm^3$.

It is necessary that the absolute fractional lattice mismatch between the atomically compatible semiconductor and the body 1 semiconductor at the interface 3 does not exceed 0.005, or the value which causes misfit disclocation to form. These conditions can be readily satisfied for a binary semiconductor by providing a ternary semiconductor with two elements in common and decreasing the extra element to zero at the interface. As the extra element increases and one of the common elements decreases, the valence band will rise because of the grading of the elements such that the energy gap 6 at the interface with the metal 7 will be the bandgap of the CB semiconductor 5, which for indium arsenide will be a gap 6 in the vicinity of 0.35 electron volts.

Referring to FIG. 2 a voltage-current graph of such a contact is shown. Since all barriers caused by surface carrier traps or states, or by carrier traps at the interface with the region 2 and the body 1 are avoided, the current-voltage characteristic will be a low resistance slope straight line labelled low resistance ohmic. The contact provides resistance values much less than 10^{-6} ohm cm.

In intermetallic semiconductors, that is, semiconductors wherein the crystal lattice is made up of periodically arranged atoms of more than one element such as the material gallium arsenide (GaAs), the surface is such that a barrier to current flow is present when a metal external electrode is applied. The presence of the barrier introduces resistance which can interfere with device performance in small signal devices such as Field Effect Transistors or in larger signal devices such as Laser devices.

An ideal ohmic contact may be considered to be one in which the resistance is as shown in Equation 1.

Equation 1: $$\rho_c = \left(\frac{\partial J}{\partial V}\right)^{-1} \quad \text{ohm cm}^2$$

where J = current density through contact at $V \tilde{\sim} 0$.

In order for the rate of change of current and voltage to remain constant, it will be necessary to avoid all non-linear barriers.

The first such non-linear barrier is of the Schottky type wherein a metal contact is placed on the surface of the semiconductor. Under these conditions, a barrier occurs due to a difference of work functions and electron affinities between the metal and the semiconductor.

Referring to FIG. 3 an energy level diagram is provided illustrating a metal contact and barrier on an intermetallic semiconductor. The barrier height is labelled ϕ_b and may be expressed for the ideal Schottky barrier contact in Equation 2.

Equation 2: $\phi_b = \phi_m - \chi$

where ϕ_b = barrier height

ϕ_m = work function of metal contact -

χ = electron affinity of the semiconductor which in turn is the energy to remove an electron from the bottom of the conduction band to vacuum with no kinetic energy.

Equation 2 will be valid when the density of surface states or carrier traps on the intermetallic semiconductor is small and the metal is inert with respect to the semiconductor. Under these conditions, ohmic contacts will occur when ϕ_m, the work function of the metal contact is less than or equal to χ the electron affinity of the semiconductor. In practice, however, this situation is rarely observed, especially for elemental and III-V compound intermetallic semiconductors. For example, in the material gallium arsenide, currently receiving considerable attention in the art, the barrier ϕ_b of FIG. 3 is nearly always observed to be 0.7 to 0.8 electron volts regardless of the metal used for the contact and its attendant ϕ_m. The constancy of the barrier ϕ_b (FIG. 3) of the gallium arsenide has been attributed to a large density of surface states on the gallium arsenide which operates to pin the barrier ϕ_b. The magnitude of the barrier ϕ_b has had serious detrimental effects since it introduces resistance.

At the present state of the art an evaporated gold contact on gallium arsenide which has been doped to less than or equal to 10^{18} still results in a rectifying contact as shown from the voltage-current graph of FIG. 4.

Efforts have taken place in the art that have improved the barrier situation through the use of alloyed contacts but these have some processing limitations. Referring to FIG. 5 an energy level diagram is shown illustrating an alloyed type of contact similar to the example set forth in U.S. Patent No. 4,188,710 wherein an alloyed contact such as gold-germanium has been employed.

Referring to FIG. 5 the barrier height ϕ_b is present but very heavy doping of the region immediately adjacent the metal contact for a short distance operates to produce a drop in both the conduction and valence band and to sharply narrow the barrier width labelled w. When the barrier width comes into a range for quantum mechanical tunnelling, the carriers no longer have to surmount the full barrier ϕ_b but rather tunnel through and consequently as illustrated in FIG. 6, the contact performance is ohmic. Even so, for the high doping levels of about 10^{19} achievable for GaAs, this type of contact still gives rise to contact resistance of $\geq 10^{-6}$ ohm cm^2 and the operating characteristic in FIG. 6 is labelled high resistance ohmic.

The processes available in the art to provide the heavily doped, narrow w region conditions for tunnelling require close control. The processing, with the attendant heat, introduces process problems that result in difficulty of reproducible results. The depletion width w is a function of doping and is exponentially related to the reciprocal of the doping density. This is a very sensitive parameter. Tunnelling dimensions for w are of the order of a few hundred angstroms but not only are precise times and temperatures required to form the contact but subsequent process

steps may interfere with the contact so that not only does the contact require extraordinary control to produce, but contact-to-contact parameters are seldom uniform and subsequent heat related processing may change the contact parameters.

A second problem occurs with the heavily doped type of contact of FIG. 5 in that the ϕ_b does introduce some contact resistance and where ϕ_b is greater than 0.5 electron volts, even though the rate of change of current with voltage would indicate a contact that is ohmic in nature, still some contact resistance will be present which may be significant in some signal situations. This is true even where the doping density is in the range of 10^{18} or 10^{19}.

It has been found that the best contact resistance for this type of contact is in the vicinity of about 10^{-6} ohm centimeters square. Thus, even though the heavily doped or alloy contact as illustrated in connection with FIG. 5 is an improvement over the situation of FIG. 3, the fact remains that it is necessary to lower ϕ_b to less than 0.5 electron volts. Especially for contacts to lightly doped or n- material where the doping level is less than 10^{17} it is necessary to keep ϕ_b less than 0.5 electron volts in order to provide full device performance flexibility.

Another approach to the contact resistance problem in the art has been the introduction of a semiconductor layer between the intermetallic semiconductor and the metal contact that operates to somewhat reduce the barrier ϕ_b. An illustration of this type of approach is shown in U.S. Patent No. 3,984,261 wherein a region of indium gallium arsenide (InGaAs) is applied on gallium arsenide (GaAs). In a structure of this type, however, an improvement at the barrier on the surface is offset as is illustrated in FIGS. 7 to 10, by the fact that a different barrier is introduced at the interface with the intermetallic semiconductor.

Referring to FIG. 7 an energy level diagram illustrates the type of contact wherein a lower bandgap semiconductor is inserted between the intermetallic semiconductor and the metal external contact. One barrier situation is caused by carrier traps or interface states at the interface of the two semiconductors.

In accordance with the invention this type of barrier is avoided by specifying a lattice match within an absolute fraction of 0.005.

FIG. 7 illustrates a situation in which the lower bandgap semiconductor lattice spacing is larger than that of the intermetallic semiconductor at the interface between the lower bandgap semiconductor and the intermetallic semiconductor. In this instance interface states are shown which operate as carrier traps and introduce a barrier such that the contact performs, as illustrated in the operating characteristic of FIG. 8, as a rectifier.

Referring next to FIG. 9 a condition for a second barrier situation is illustrated wherein the electron affinity of the lower bandgap semiconductor is smaller than that of the intermetallic semiconductor. In this type of situation there is no appreciable lattice mismatch and hence there are no appreciable interface states but a barrier to electron flow still occurs and the device operates as illustrated in FIG. 10 as a rectifier.

In both situations, the lower bandgap semiconductor reduces the barrier at the interface with the metal but another barrier is encountered at the interface of the semiconductors.

In accordance with the invention it has been found that the barrier situations of FIGS. 9 and 10 can be avoided for practical purposes by requiring that the fractional lattice mismatch not exceed 0.005 and that the conditions of the following Equations 4 and 5 be met.

Equation 4: $$\frac{\alpha_{ACB} - \alpha_{AB}}{\alpha_{AB}} > \pm 0.005$$

where α_{ACB} = lattice constant of the lower bandgap or ternary semiconductor; and

α_{AB} = lattice constant of the inter-metallic or binary semiconductor -

In accordance with the invention an electron affinity match is provided between the lower bandgap semiconductor and the inter-metallic semiconductor within 0.04 electron volts as expressed in Equation 5.

Equation 5: $\chi_{AB} - \chi_{AC} \leq 0.04$ eV

where χ is the electron affinity of the semiconductor which in turn is the energy to remove an electron from the bottom of the conduction band to vacuum with no kinetic energy.

In accordance with the invention by using a graded bandgap semiconductor, as illustrated in FIG. 1, lattice mismatches and other dislocations can be minimized.

Referring again to the energy diagram of FIG. 1. In a preferred embodiment an n-type layer 2 of the semiconductor ACB will be epitaxially grown by one of the techniques in the art of chemical vapour deposition (CVD) or molecular beam epitaxy (MBE) on an n-type body 1 AB semiconductor using for the AB semiconductor gallium arsenide and the ACB semiconductor $Ga_xIn_{1-x}As$ in which x varies to provide a graded composition from pure gallium arsenide at the interface 3 and

hence a perfect lattice and electron affinity match to pure indium arsenide at the interface 4 over a distance of approximately 2,000Å. In such a structure in the region 5 at the interface with the metal, the Fermi level is pinned in the conduction band at the n+ indium arsenide interface at an energy of 0.5 eV above the indium arsenide valence band. The energy gap for indium arsenide is approximately 0.35 electron volts. A gold metal contact 7 is evaporated or electroplated with no heating. The resulting structure in accordance with the invention produces an ohmic contact to n-type indium arsenide where the contact resistance is less than 5×10^{-7} ohm cm.

CLAIMS

1. A semiconductor device comprising a body (1) of intermetallic semiconductor material provided with a contact, the contact comprising an external metallic layer (7) and an intermediate region (2, 5) of semiconductor material atomically compatible with the body disposed between the metallic layer and the body, the device being characterised by the intermediate region having a graded composition such that the lattice and electron affinity of the intermediate region substantially match the lattice and electron affinity of the intermetallic semiconductor material at the interface between the intermediate region and the body and that there exists an energy gap of less than 0.5 electron volts at the interface between the intermediate region and the external metallic layer.

2. A device as claimed in claim 1, in which said intermediate region has at the interface with said body a fractional lattice match within 0.005.

3. A device as claimed in claim 1 or claim 2, in which said intermediate region has an electron affinity difference within 0.04 electron volts at its interface with said body.

4. A device as claimed in any of claims 1 to 3, in which the intermediate region is comprised of a ternary semiconductor material and said intermetallic semiconductor material is a compound of two of the elements in said ternary semiconductor material.

5. A device as claimed in claim 4, in which said intermetallic semiconductor material is gallium arsenide, and said ternary semiconductor material is gallium indium arsenide.

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6. A device as claimed in claim 5, in which the composition of said intermediate region is graded from being pure gallium arsenide at the interface with said body to being pure indium arsenide at the interface with the internal metallic layer.

FIG. 1

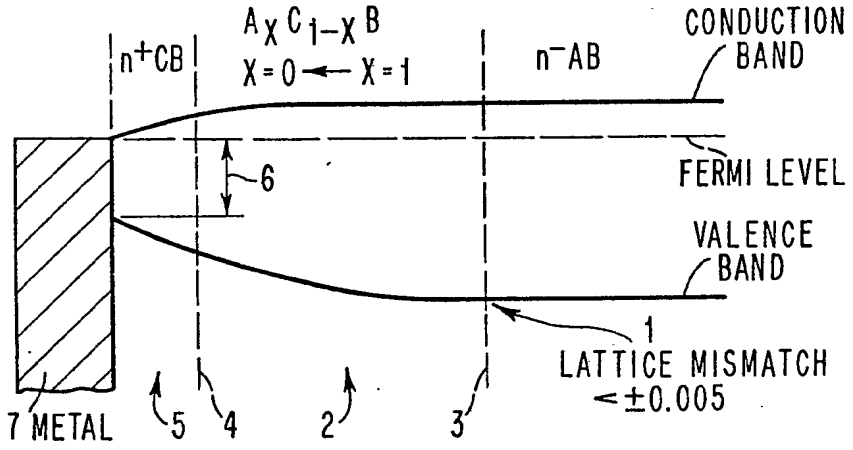


FIG. 2

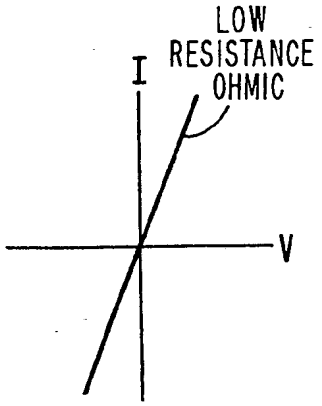


FIG. 3

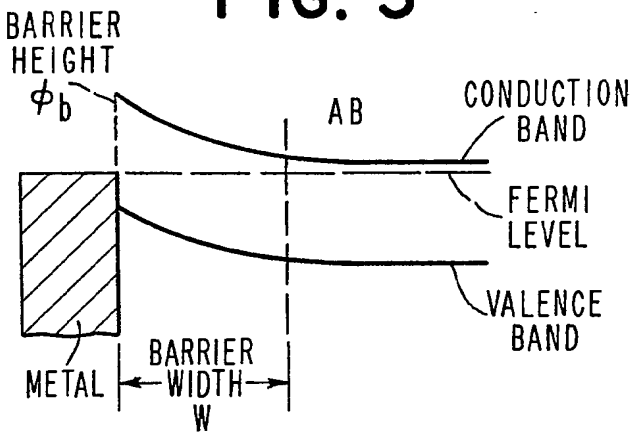


FIG. 4

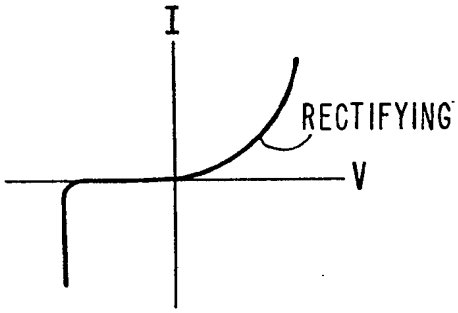


FIG. 5 PRIOR ART

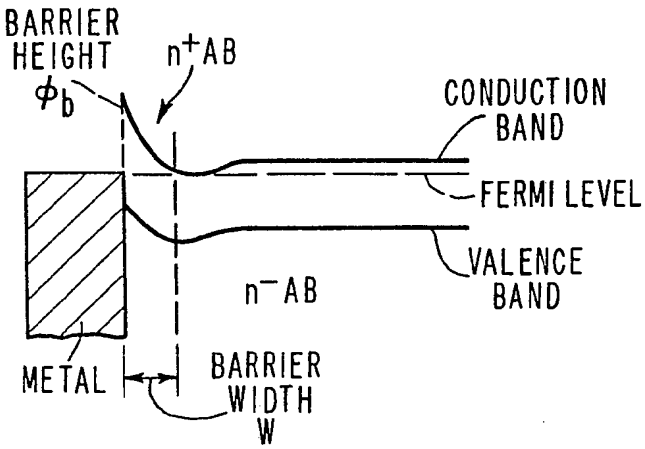


FIG. 6

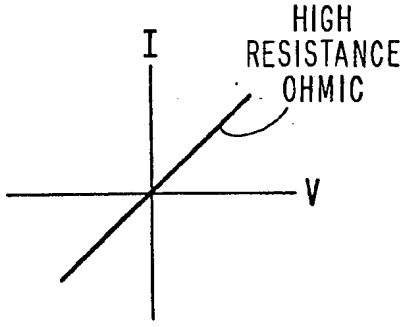


FIG. 7 PRIOR ART

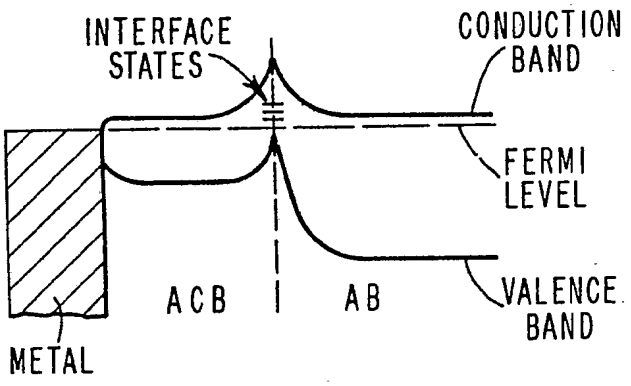


FIG. 8

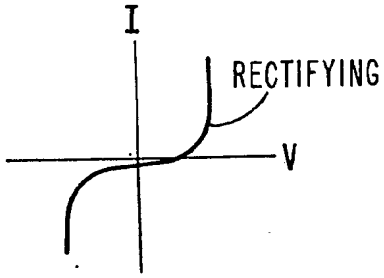


FIG. 9 PRIOR ART

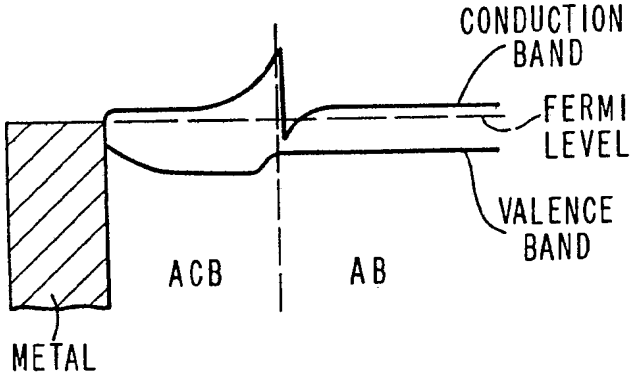
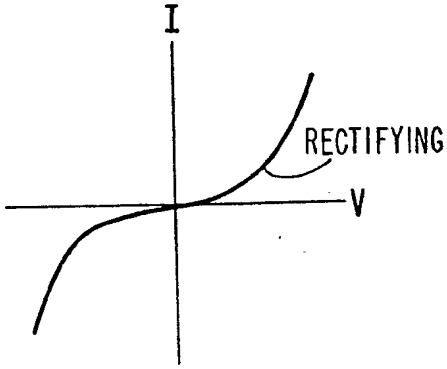


FIG. 10



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第2630279号

(45)発行日　平成９年(1997)７月16日　(24)登録日　平成９年(1997)４月18日

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29/872			29/48	Ｆ	
				Ｓ	

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(73)特許権者　000004237
日本電気株式会社
東京都港区芝五丁目７番１号

(72)発明者　小沼　和夫
東京都港区芝五丁目７番１号　日本電気株式会社内

(74)代理人　弁理士　加藤　朝道

審査官　近藤　幸浩

(56)参考文献　特開　平４－279068（ＪＰ，Ａ）
特開　昭63－200577（ＪＰ，Ａ）
特公　昭63－51546（ＪＰ，Ｂ２）

(54)【発明の名称】　ショットキー型光検出器およびその駆動方法

(57)【特許請求の範囲】

【請求項１】半導体基板と金属からなるショットキーダイオードを用いた光検出器において、前記半導体基板と前記金属との界面に近接して前記半導体基板中の空乏層が広がっている領域内に、前記半導体基板よりも誘電率の高い高誘電率層が形成されていることを特徴とするショットキー型光検出器。

【請求項２】前記半導体基板中のショットキーダイオード空乏層域内に、前記高誘電率層として、第２の半導体が形成されていることを特徴とする請求項１記載のショットキー型光検出器。

【請求項３】前記半導体基板中のショットキーダイオード空乏層域内に、前記高誘電率層として、絶縁体の極薄膜から形成されていることを特徴とする請求項１記載のショットキー型光検出器。

【請求項４】前記高誘電率層がチタンナイトライド（ＴｉＮ）からなることを特徴とする請求項１に記載のショットキー型光検出器。

【請求項５】半導体基板と金属からなるショットキーダイオードの空乏層域内に前記半導体よりも誘電率の高い高誘電率層を形成したショットキー型光検出器の駆動方法において、実効ショットキー障壁位置が、前記高誘電率層部分に位置するようにバイアス電圧を印加することを特徴とするショットキー型光検出器の駆動方法。

【請求項６】半導体基板と金属からなるショットキーダイオードの空乏層域内に前記半導体よりも誘電率の高い高誘電率層を形成したショットキー型光検出器の駆動方法において、前記ショットキー型光検出器を所定のバイアス電圧にリセットした後に直ちに浮動状態にし、所定時間後、再度リセットする際に電位を読み出すことを特

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徴とするショットキー型光検出器の駆動方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明はショットキーダイオードを用いた光検出器に関する。
【０００２】
【従来の技術】従来のショットキー型光検出器について図５を用いて説明する。図５（Ａ）は、ショットキー型光検出器の構成を示す図であり、参照文献（RCA Review vol.43 p569-587: H.Elabd and W.F.Kosonocky, “Theory and Measurements of photoresponse for Thin Film Pd_2Si and PtSi Infrared Schottky-Barrier Detectors with Optical Cavity”、アールシーエー　レビュー４３巻５６９頁～５８７頁：エラブド、及びコソノキー著、“光学共鳴構造を有するパラディウムシリサイドと白金シリサイドの薄膜によるショットキーバリア型赤外線検出器の光応答特性に関する理論と実際”、以後「参考文献１」という）で紹介されている。
【０００３】図５（Ａ）を参照して、ショットキー型光検出器は金属電極（１）としての白金シリサイド（ＰｔＳｉ）膜と半導体基板（２）としてのｐ型シリコン（ｐ－Ｓｉ）基板により構成されている。半導体基板（２）へのオーミックコンタクト（３）は模式的に示してある。
【０００４】半導体基板（２）としてのｐ型シリコン基板は比抵抗が３０～５０Ωｃｍである。
【０００５】図５（Ａ）に示すように、一般に、光（１００）は基板の裏面から入射させる。
【０００６】白金シリサイド（ＰｔＳｉ）のｐ型シリコン基板に対するショットキー障壁高さが約０．２２ｅＶであるため、この構成のショットキー型光検出器は、約５．６μｍの赤外線に感度を持つ赤外線検出器として用いることができる。
【０００７】従来、入射した光（赤外線）は、図５（Ｂ）に示されているように、白金シリサイド（ＰｔＳｉ）膜で吸収され、白金シリサイド内で生成したホットホールは、ＰｔＳｉ／ｐ－Ｓｉ界面で選択通過されるものと理解されていた。
【０００８】図５（Ｂ）では、通過するホットホールを符号２００で示し、反射されるホットホールを符号２０１で示している。図５（Ｂ）には、金属のフェルミレベル（４）、空乏層（５）、参考文献１に従ったポテンシャル（６）、および逆バイアス電圧（７）が示されている。
【０００９】この過程については、参照文献１で詳細に記載されている。選択通過されたホットホール２００は、ｐ型シリコン基板に流れ込み、信号として検出される。
【００１０】この理解の下に、ショットキー型赤外線イメージセンサが盛んに開発されて、例えば、100万画素の赤外線イメージセンサも試作されている［参考文献：T.Seto, A.Mori, R.Ishigaki, S.Itoh, N.Yutani, M.Kimata, N.Tubouchi, A.Akiyama, and T.Sasaki, ”Performance of IM-IRCCD imager with PtSi Schottky-barrier detectors”, proceeding of SPIE 2020, p404 (1993)、瀬戸　他、「ＰｔＳｉショットキーバリア検出器のＩＭ－ＩＲＣＣＤの性能」、エスピーアイイーのプロシーデング、２０２０巻４０４頁（１９９３年）］。
【００１１】しかし残念ながら、図５（Ｂ）に基づく理解は正確でない。
【００１２】すなわち、実際のショットキーダイオードにおいては、ホットホールは図５（Ｃ）に実線で示すポテンシャル（６′）を感じながら移動することになる。
【００１３】図５（Ｂ）と図５（Ｃ）の相違点は、鏡像力を考慮しているか、いないかの違いによる。ホットホールが実際に感じるポテンシャルは、図５（Ｃ）の点線ａ（図５（Ｂ）の実線に対応する）で示したポテンシャルに、図５（Ｃ）の破線ｂで示した鏡像力によるポテンシャル１／（16*π*ε*ｘ）を加えたものである。ここで、εは物質の誘電率であり、ｘは白金シリサイド（ＰｔＳｉ／ｐ－Ｓｉ）界面から半導体側への距離である。
【００１４】すなわち、図５（Ｃ）の実線で示すポテンシャル（６′）をホットホールは感じることになる。図５（Ｃ）において、実効ショットキー障壁高さ（「バリア高さ」ともいう）はΦb-effect、その位置（「バリア位置」ともいう）はx-effectとされる。
【００１５】光の吸収により白金シリサイド（ＰｔＳｉ）中で生成されたホットホールは、実効ショットキー障壁高さの位置に達して、一部が選択的に通過して、シリコン基板中に入り信号として検知される。
【００１６】
【発明が解決しようとする課題】このように実際には、白金シリサイド（ＰｔＳｉ）中で生成したホットホールは、白金シリサイド（ＰｔＳｉ）中の移動距離に加えて、バリア位置x-effectまでの移動を行なう。その際、ホットホールは移動中に格子散乱等によりその数が減少する。
【００１７】このため、ショットキー型光検出器の感度を向上させるには、生成したホットホールが、少ない移動距離でバリアに達すること、及び、バリア高さを低くすることが必要とされる。
【００１８】バリア高さを低くすることで、感度を向上させる従来例として、例えば特公昭６３－５１５４６号公報には、図６（Ａ）に示すように、白金シリサイド／ｐ型シリコン（ＰｔＳｉ／ｐ－Ｓｉ）ショットキーダイオードの界面部分に、ｐ型ドーパント（８）をイオン注入することにより、図６（Ａ）に示す構成をなし、図６（Ｂ）に示すようなポテンシャルを形成したものが開示されている。

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【００１９】この方法は、界面付近のドーパント濃度を高めることにより、空乏層幅を縮めてトンネル効果により実効バリア高さを低くするものである。
【００２０】しかしながら、実際には、図５（Ｃ）を参照して説明したように、鏡像効果を考慮したポテンシャルとして理解するべきであり、図５（Ｃ）と同様に、シリコン基板中の実効バリア位置までの距離が存在する。なお、図６について、鏡像効果を考慮したポテンシャルを示す図は省略する。
【００２１】すなわち、従来のショットキー型光検出器では、鏡像効果により、実効バリア位置が金属／半導体界面より半導体側内に入って位置することが全く考慮されていない。
【００２２】このため、金属／半導体界面より実効バリア位置までの移動の間にホットキャリア数が減少するという影響に対して、何等対策が施されていない。これは図５、図６で示した従来例に共通して言えることである。
【００２３】さらに、図６に示した従来例（特公昭６３－５１５４６号公報）では、トンネル効果により実効バリア高さを低下させているが、この方法では、熱励起された雑音信号分の検出も増加してしまうことになる。このため、ショットキーダイオード自身のＳ／Ｎの低下とともに、電荷量が増えることにより、ＣＣＤ等の信号転送素子の負担も増えてしまう。
【００２４】従って、生成したホットホールの減少を食い止めることが肝要である。
【００２５】本発明はこのような問題点に鑑みてなされたものであり、感度特性を向上したショットキー型光検出器を提供することを目的とする。
【００２６】
【課題を解決するための手段】前記目的を達成するため、本発明は、半導体基板と金属からなるショットキーダイオードを用いた光検出器において、前記半導体基板と前記金属の界面に近接して前記半導体基板中の空乏層が広がっている領域内に、前記半導体基板よりも誘電率の高い高誘電率層が形成されていることを特徴とするショットキー型光検出器を提供する。
【００２７】また、本発明のショットキー型光検出器においては、好ましくは前記半導体基板中のショットキーダイオード空乏層域内に、前記高誘電率層として、第２の半導体が形成されていることを特徴とする。
【００２８】さらに、本発明のショットキー型光検出器においては、好ましくは前記半導体基板中のショットキーダイオード空乏層域内に、前記高誘電率層として、絶縁体の極薄膜から形成されていることを特徴とする。
【００２９】本発明は、半導体基板と金属からなるショットキーダイオードの空乏層域内に前記半導体よりも誘電率の高い高誘電率層を形成したショットキー型光検出器の駆動方法において、実効ショットキー障壁位置が、前記高誘電率層部分に位置するようにバイアス電圧を印加することを特徴とするショットキー型光検出器の駆動方法を提供する。
【００３０】また、本発明は、半導体基板と金属からなるショットキーダイオードの空乏層域内に前記半導体よりも誘電率の高い高誘電率層を形成したショットキー型光検出器の駆動方法において、前記ショットキー型光検出器を所定のバイアス電圧にリセットした後に直ちに浮動状態にし、所定時間後、再度リセットする際に電位を読み出すことを特徴とするショットキー型光検出器の駆動方法を提供する。
【００３１】
【作用】金属と半導体基板とで構成されたショットキーダイオードにおいては、鏡像効果のためにシリコン（Ｓｉ）基板の奥に実効バリアが位置するのに対して、本発明によれば、空乏層が広がっている領域内に、半導体基板よりも誘電率が高い第２の半導層または絶縁層を形成することにより、実効バリア位置を界面近傍に近付けて、生成したホットキャリア数の減少を抑制するものである。
【００３２】本発明では、前記高誘電率層の形成によって、鏡像効果によるポテンシャルの傾向が急峻になることにより、鏡像効果とショットキーダイオード空乏層とのポテンシャルの和である実効ポテンシャルのバリア位置が界面に近づくことを利用している。
【００３３】
【実施例】図面を参照して、本発明の実施例を以下に説明する。
【００３４】
【実施例１】図１に、本発明の一実施例に係るショットキー型光検出器の構造を示す。図１を参照して、本実施例に係るショットキー型光検出器は、金属電極（１）としての白金シリサイド（ＰｔＳｉ）膜と、半導体基板（２）としてのｐ型シリコン（ｐ－Ｓｉ）基板により構成され、ＰｔＳｉ／ｐ－Ｓｉショットキーダイオードのｐ型シリコン基板中に、高誘電率材料（９）としてチタンナイトライド（ＴｉＮ）が形成されている。
【００３５】ホットホールの多重反射効果を考慮して、白金シリサイド（ＰｔＳｉ）膜は３ｎｍ、ｐ型Ｓｉ基板はボロンドープ３０～５０Ωｃｍを用いている。
【００３６】そして、裏面から光を入射できるようにｐ型シリコン基板は両面とも鏡面研磨してある。
【００３７】高誘電率材料であるチタンナイトライド（ＴｉＮ）は、ＰｔＳｉ／ｐ－Ｓｉ界面から略２ｎｍの位置から３ｎｍの位置までの１ｎｍの膜厚に形成されている（高誘電率材料（９）は、ショットキーダイオードの空乏層域内にある）。
【００３８】図２に、図１の構造のショットキー型光検出器のポテンシャルを示す。図２（Ａ）は図１の構成をそのまま描いたものである。図２（Ｂ）の実線は図２

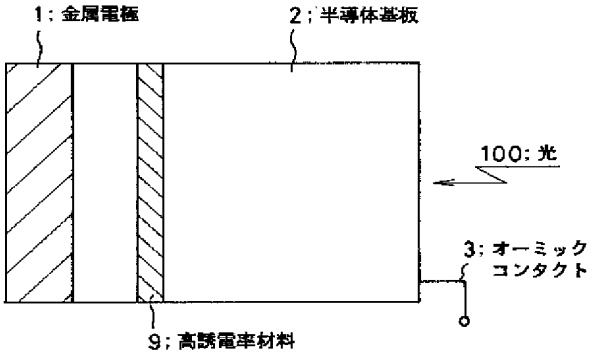
（Ａ）の構造によるポテンシャルを描いてある。
【００３９】ショットキーダイオードの印加電圧は、－５Ｖ（逆バイアス）としてある。図２（Ｂ）のこの実線は、ポアッソン方程式の解としてのショットキーダイオードのポテンシャルと、鏡像効果によるポテンシャルの和である。
【００４０】なお、図２（Ｂ）において、２つのポテンシャルの導出の際には、各深さにおける誘電率を考慮した１次元プロファイルモデルを用いている。
【００４１】結果として、実効バリア位置ｘ-effectは、ＰｔＳｉ／ｐ－Ｓｉ界面から３．０ｎｍとなる。高誘電率層（９）は１ｎｍの極薄膜であるため、ホットホールはトンネリングにより高誘電率層（９）を通過できる。
【００４２】比較のために、高誘導率層（９）を形成していない場合（従来例）のポテンシャルを、図２（Ｂ）に破線で示してある。従来例では実効バリア位置は約６．３ｎｍである。
【００４３】次に、図３を参照して、本発明の一実施例に係るショットキー型光検出器の駆動方法の例を示す。
【００４４】図３（Ａ）は、図１の構造のショットキー型光検出器に関して逆バイアス電圧５Ｖの条件のポテンシャルを示す図である。
【００４５】図３（Ｂ）は、逆バイアス電圧６Ｖの条件、図３（Ｃ）は、逆バイアス電圧７Ｖの条件のポテンシャルを示す図である。
【００４６】図３を参照して、逆バイアス電圧の値に応じて急激に実効バリア高さが低下することがわかる。そして、逆バイアス電圧の５～７Ｖという電圧値は、実効バリア位置が高誘電率膜内に位置する範囲の逆バイアスの条件とされる。
【００４７】このように、高誘電率膜の深さ方向範囲内に実効バリア位置が存在するように逆バイアス電圧を調整する駆動方法によって、小さな駆動電圧差によって実効ショットキー障壁高さを大きく変化させることができる。
【００４８】しかも、実効バリア位置が界面近傍に維持された状態であるため、生成したホットホールの減少が抑制できている。これにより、高い感度を維持しながらその範囲内で感度調整が容易に行える。
【００４９】高誘電率層（９）としては、シリコンの比誘電率（11.7）よりも高い比誘電率（静電的）を有するＧａＡｓ、ＩｎＳｂ等の化合物半導体あるいはＧｅ等を用いてもよい。
【００５０】
【実施例２】本発明のショットキー型光検出器の駆動方法の第２の実施例について説明する。
【００５１】本実施例に係る駆動方法は、図１に示した構造のショットキー型光検出器を逆バイアス電圧７Ｖにリセットした直後に浮動状態（フローティング状態）として、例えば３３ｍｓ（ミリ秒；走査期間）後に再度リセットする際に、電位を読み出すものである。
【００５２】図４に、この駆動方法の感度特性を示す。図４において、横軸は入射光量、縦軸は読み出し電位（信号電位）である。
【００５３】図３を参照して説明したとおり、逆バイアス電圧７Ｖにおける感度は高く、逆バイアス電圧に強く依存して感度が低下するため、低照度で高い感度を持ち、高照度では感度が抑制される。
【００５４】この傾向は、従来のショットキー光検出器においても同様に持ち合わせているが、図４中破線で示すように緩慢である。
【００５５】本実施例においては、図４中実線で示すように、低照度（照射光量小）で高感度を持ち（読み出し電位大）、高照度まで飽和しない感度特性は、自身の温度と放射赤外線との関係が対数に近い物理現象の検出には最適といえる。
【００５６】以上、本発明を上記実施例に即して説明したが、本発明は上記態様にのみ限定されず、本発明の原理に準ずる各種態様を含む。
【００５７】
【発明の効果】本発明（請求項１）のショットキー型光検出器によれば、金属／半導体界面から実効バリア位置までの移動における信号電荷担体の減少が抑制され、光検出器の高感度化を達成することができる。
【００５８】上記効果は請求項２～４に記載される本発明の好ましい態様によっても同様にして達成される。
【００５９】また、本発明のショットキー型光検出器の駆動方法（請求項５）によれば、金属／半導体界面から実効バリア位置までの移動における信号電荷（担体）の消滅を抑制するように逆バイアス電圧を印加することにより、光検出器の高感度化を達成することができる。
【００６０】さらに、本発明の駆動方法（請求項６）によれば、高誘電率膜の位置におけるポテンシャルの急激な変化を利用した駆動方法を用いることにより、低照度において高感度とされ、かつ大きなダイナミックレンジを有する検出器を実現できる。
【図面の簡単な説明】
【図１】本発明のショットキー型光検出器の実施例の構成を示す図である。
【図２】（Ａ）本発明の一実施例の構成を示す図である。
（Ｂ）本発明の一実施例のショットキー型光検出器のポテンシャルを示す図である。
【図３】本発明のショットキー型光検出器の駆動方法の第１の実施例のポテンシャルを示す図である。（Ａ）～（Ｃ）はバイアス電圧を可変とした場合のポテンシャルを示す図である。
【図４】本発明のショットキー型光検出器の駆動方法の第２の実施例の感度特性を示す図である。

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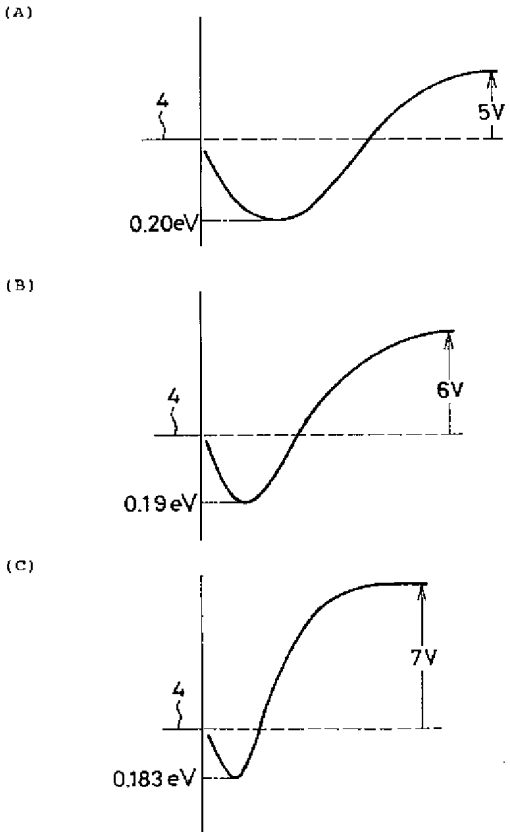
【図５】（Ａ）従来のショットキー型光検出器の構成を示す図である。
（Ｂ）図５（Ａ）の構成のポテンシャルを示す図である。
（Ｃ）鏡像効果を考慮したポテンシャルを示す図である。
【図６】（Ａ）従来のショットキー型光検出器の別の構成を示す図である。
（Ｂ）図６（Ａ）の構成のポテンシャルを示す図である。
【符号の説明】

１　金属電極
２　半導体基板
３　オーミックコンタクト
４　金属のフェルミレベル
５，５′，５″　空乏層
６，６′　ポテンシャル
７　逆バイアス電圧
８　p^+ドーパント
９　高誘電率材料（高誘電率層）
１００　光
２００～２０２　ホットホール

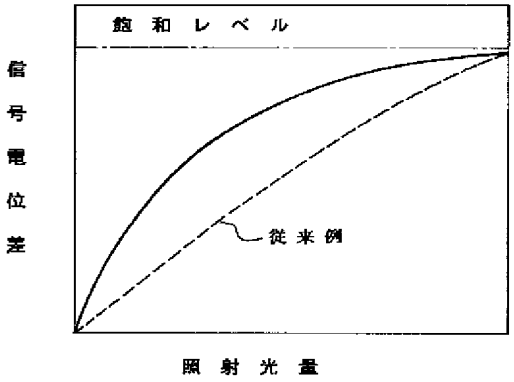
【図１】



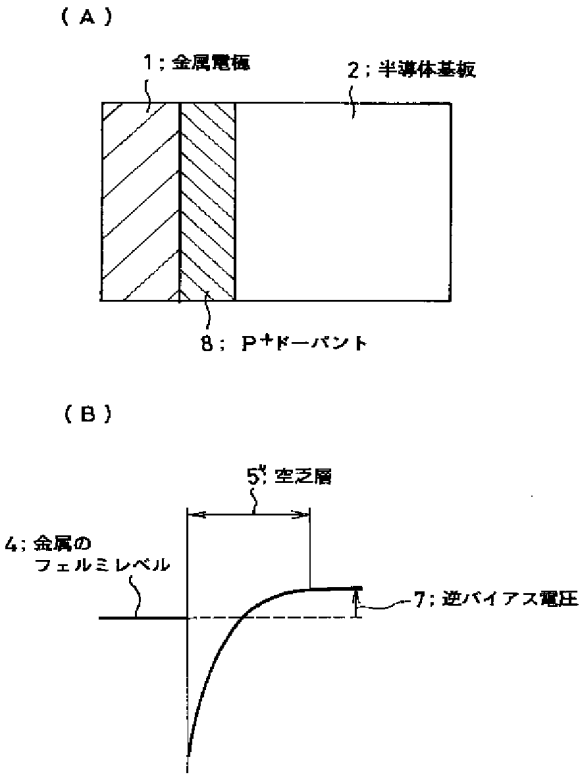
【図３】



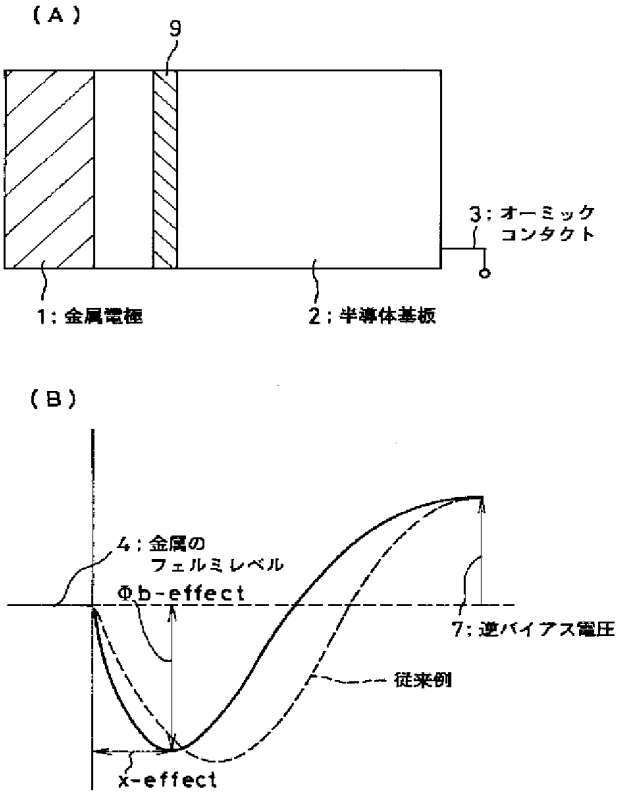
【図４】



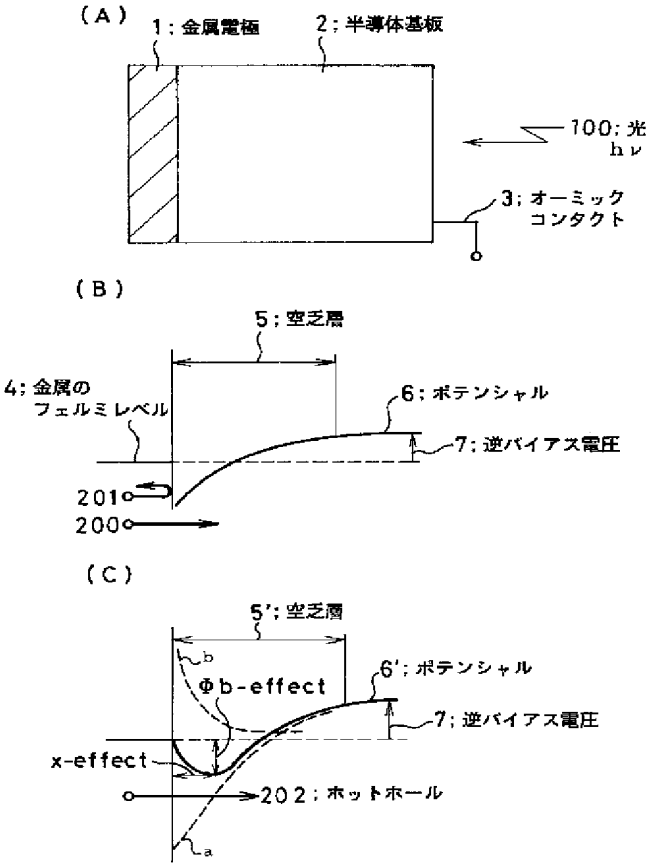
【図６】



【図２】


（Ａ）
9
3；オーミック
コンタクト
1；金属電極
2；半導体基板
（Ｂ）
4；金属の
フェルミレベル
Φb-effect
7；逆バイアス電圧
従来例
x-effect

【図５】


（Ａ）
1；金属電極
2；半導体基板
100；光
hν
3；オーミック
コンタクト
（Ｂ）
5；空乏層
4；金属の
フェルミレベル
6；ポテンシャル
7；逆バイアス電圧
201
200
（Ｃ）
5'；空乏層
b
Φb-effect
6'；ポテンシャル
7；逆バイアス電圧
x-effect
202；ホットホール
a

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JP2630279B2 SCHOTTKY TYPE PHOTODETECTOR AND ITS DRIVING METHOD

Applicants: NIPPON DENKI KK

Inventors: KONUMA KAZUO

Classifications:
IPC ***H01L29/47; H01L29/872; H01L31/108;*** (IPC1-7): H01L29/872; H01L31/108;

Priorities: JP27185594A 1994-10-12

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Publication: JP2630279B2·1997-07-16

Published as: **JPH08116084A;** JP2630279B2

SCHOTTKY TYPE PHOTODETECTOR AND ITS DRIVING METHOD

Abstract

PURPOSE: To restrain the decrease of signal charge carrier in the movement from the metal/semiconductor interface to the effective barrier position, and improve the sensitivity of a photodetector, by forming a high permittivity layer whose permittivity is higher than that of a substrate, in the substrate in the vicinity of the interface of the semiconductor substrate and metal. CONSTITUTION: The photodetector is constituted of a platinum silicide(PtSi) film as a metal electrode 1, and a P-type silicon(P-Si) substrate as a semiconductor substrate 2. In the P-Si substrate 2 of a PtSi/P-Si Schottky diode constituted of the metal electrode 1 and the semiconductor substrate 2, titanium nitride(TiN) as high permittivity material 9 whose permittivity is higher than that of the P-Si substrate 2 is formed. The TiN 9 is in the depletion layer of the Schottky diode. Thereby the decrease of signal charge carrier in the movement from the metal/semiconductor interface to the effective barrier position is restrained, and the sensitivity of a photodetector can be improved.

Schottky photodetector and driving method thereof

JP2630279B2
Japan

Find Prior Art Similar

Other languages: Japanese
Inventor: 和夫 小沼

Worldwide applications
1994 JP

Application JP6271855A events

1994-10-12	Application filed by 日本電気株式会社
1994-10-12	Priority to JP6271855A
1996-05-07	Publication of JPH08116084A
1997-07-16	Application granted
1997-07-16	Publication of JP2630279B2
2014-10-12	Anticipated expiration
Status	Expired - Lifetime

Info: Cited by (1), Legal events, Similar documents, Priority and Related Applications
External links: Espacenet, Global Dossier, Discuss

Claims (6)

Hide Dependent

(57) [Claims]

1. A photodetector using a Schottky diode composed of a semiconductor substrate and a metal, wherein a depletion layer in the semiconductor substrate is provided near an interface between the semiconductor substrate and the metal.
A Schottky-type photodetector, wherein a high-permittivity layer having a higher permittivity than the semiconductor substrate is formed in a region where the width of the semiconductor substrate extends .

2. The Schottky photodetector according to claim 1, wherein a second semiconductor is formed as the high dielectric constant layer in a Schottky diode depletion layer region in the semiconductor substrate. .

3. The Schottky-type photodetector according to claim 1, wherein the high dielectric constant layer is formed of an extremely thin insulating material in a Schottky diode depletion layer region in the semiconductor substrate. vessel.

4. The high dielectric constant layer is made of titanium nitride (T
The Schottky photodetector according to claim 1, wherein the photodetector comprises iN).

5. A method for driving a Schottky photodetector, wherein a high dielectric constant layer having a higher dielectric constant than the semiconductor is formed in a depletion layer region of a Schottky diode made of a semiconductor substrate and a metal. Wherein a bias voltage is applied such that the bias voltage is applied to the high dielectric constant layer portion.

6. A method for driving a Schottky photodetector, wherein a high dielectric constant layer having a higher dielectric constant than the semiconductor is formed in a depletion layer region of a Schottky diode made of a semiconductor substrate and a metal. A method for driving a Schottky photodetector, characterized in that a floating state is set immediately after resetting a detector to a predetermined bias voltage, and a potential is read out when resetting after a predetermined time.

Description

DETAILED DESCRIPTION OF THE INVENTION

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a photodetector using a Schottky diode.

[0002]

2. Description of the Related Art A conventional Schottky photodetector will be described with reference to FIG. FIG. 5A is a diagram showing a configuration of a Schottky-type photodetector.
vol.43 p569-587: H. Elabd and WF Kosonocky, "Theo
ry and Measurements of photoresponse for Thin Film
Pd_2 Si and PtSi Infrared Schottky-Barrier Detector
s with Optical Cavity, RCAA Review Vol. 43, pp. 569-587: Erabud and Kosonoki, "Theory on the Photoresponse Characteristics of Schottky Barrier Infrared Detectors Using Palladium Silicide and Platinum Silicide Thin Films with Optical Resonance Structure" And in fact ", hereinafter referred to as" Reference Document 1 ").

Referring to FIG. 5A, a Schottky photodetector has a platinum silicide (Pt) as a metal electrode (1).
Si) film and p-type silicon (p) as a semiconductor substrate (2)
-Si) substrate. Semiconductor substrate (2)
The ohmic contact (3) to is shown schematically.

The p-type silicon substrate as the semiconductor substrate (2) has a specific resistance of 30 to 50 Ωcm.

[0005] As shown in FIG.
00) is incident from the back surface of the substrate.

A Schottky barrier height of platinum silicide (PtSi) with respect to a p-type silicon substrate is about 0.22 eV.
Therefore, the Schottky photodetector having this configuration can be used as an infrared detector having sensitivity to infrared rays of about 5.6 μm.

Conventionally, the incident light (infrared ray) is shown in FIG.
As shown in (B), platinum silicide (PtS
i) It was understood that hot holes absorbed in the film and generated in platinum silicide were selectively passed at the PtSi / p-Si interface.

In FIG. 5B, the hot holes passing therethrough are indicated by reference numeral 200, and the hot holes that are reflected are indicated by reference numeral 20.
This is indicated by 1. FIG. 5B shows the Fermi level (4) of the metal, the depletion layer (5), the potential (6) according to Reference 1, and the reverse bias voltage (7).

This process is described in detail in Reference 1. Hot hole 200 that has been selectively passed
Flows into the p-type silicon substrate and is detected as a signal.

With this understanding, Schottky type infrared image sensors have been actively developed, and, for example, a 1 million pixel infrared image sensor has been prototyped [Reference:
T.Seto, A.Mori, R.Ishigaki, S.Itoh, N.Yutani, MK
imata, N. Tubouchi, A. Akiyama, and T. Sasaki, "Perfo
rmance of IM-IRCCD imager with PtSi Schottky-barri
er detectors ", proceeding of SPIE 2020, p404 (199
3), Seto et al., "Performance of IM-IRCCD of PtSi Schottky Barrier Detector," Proc. Of SPII, 2020, 404 (1993)].

Unfortunately, the understanding based on FIG. 5B is not accurate.

That is, in an actual Schottky diode, the hot hole moves while feeling the potential (6 ') shown by the solid line in FIG.

The difference between FIG. 5 (B) and FIG. 5 (C) depends on whether or not the image force is considered. The potential actually felt by the hot hole is the potential indicated by the dotted line a (corresponding to the solid line in FIG. 5B) of FIG. 5C, and the potential due to the image force indicated by the broken line b in FIG. 5C. This is obtained by adding a char 1 / (16 * π * ε * x). Here, ε is the dielectric constant of the substance, and x is the distance from the platinum silicide (PtSi / p-Si) interface to the semiconductor side.

That is, the hot hole feels the potential (6 ') shown by the solid line in FIG. In FIG. 5C, the effective Schottky barrier height (also called "barrier height") is Φb-effect, and its position (also called "barrier position") is x-effect.

By absorbing light, platinum silicide (PtS
The hot hole generated in i) reaches the position of the effective Schottky barrier height, and a part of the hot hole selectively passes into the silicon substrate and is detected as a signal.

[0016]

As described above, actually,
The hot holes generated in platinum silicide (PtSi) move to the barrier position x-effect in addition to the moving distance in platinum silicide (PtSi). At that time, the number of hot holes decreases due to lattice scattering or the like during movement.

For this reason, in order to improve the sensitivity of the Schottky photodetector, it is necessary that the generated hot holes reach the barrier within a short moving distance and that the height of the barrier is reduced.

As a conventional example in which the sensitivity is improved by lowering the barrier height, for example, Japanese Patent Publication No. Sho 63-51546 discloses, as shown in FIG.
By implanting a p-type dopant (8) into the interface of the p-type silicon (PtSi / p-Si) Schottky diode, the structure shown in FIG.
A device having a potential as shown in FIG.

In this method, the width of the depletion layer is reduced by increasing the dopant concentration near the interface, and the effective barrier height is reduced by the tunnel effect.

However, in practice, as described with reference to FIG. 5C, it should be understood as a potential in consideration of the mirror image effect, and as in FIG. There is a distance to the barrier position.
In FIG. 6, a diagram showing potentials in consideration of the mirror image effect is omitted.

That is, in the conventional Schottky photodetector, no consideration is given to the fact that the effective barrier position is located on the semiconductor side from the metal / semiconductor interface due to the mirror image effect.

For this reason, no measure is taken against the effect that the number of hot carriers decreases during the movement from the metal / semiconductor interface to the effective barrier position. This can be said in common with the conventional example shown in FIGS.

Further, a conventional example shown in FIG.
In JP-A-51546, the effective barrier height is reduced by the tunnel effect. However, in this method, the detection of the thermally excited noise signal also increases. For this reason, as the S / N of the Schottky diode itself decreases and the charge amount increases, the load on a signal transfer element such as a CCD also increases.

Therefore, it is important to prevent the generated hot holes from decreasing.

The present invention has been made in view of such a problem, and an object of the present invention is to provide a Schottky photodetector having improved sensitivity characteristics.

[0026]

In order to achieve the above object, the present invention provides a photodetector using a Schottky diode comprising a semiconductor substrate and a metal, wherein the photodetector is provided near an interface between the semiconductor substrate and the metal. Depletion layer in semiconductor substrate
Wherein a high dielectric constant layer having a higher dielectric constant than that of the semiconductor substrate is formed in a region where is spread .

In the Schottky photodetector according to the present invention, preferably, the high dielectric constant layer is formed in the Schottky diode depletion layer region in the semiconductor substrate.
Is formed.

Further, in the Schottky photodetector of the present invention, preferably, the high dielectric constant layer is formed of an extremely thin insulator as an insulator in a Schottky diode depletion layer region in the semiconductor substrate. It is characterized by.

The present invention relates to a method of driving a Schottky photodetector in which a high dielectric constant layer having a higher dielectric constant than the semiconductor is formed in a depletion layer region of a Schottky diode composed of a semiconductor substrate and a metal. The barrier position is
A method for driving a Schottky photodetector, characterized in that a bias voltage is applied so as to be located at the high dielectric layer portion.

The present invention also relates to a method for driving a Schottky photodetector in which a high dielectric constant layer having a higher dielectric constant than the semiconductor is formed in a depletion layer region of a Schottky diode comprising a semiconductor substrate and a metal. A method for driving a Schottky photodetector, characterized in that the Schottky photodetector is set in a floating state immediately after resetting to a predetermined bias voltage, and a potential is read out when resetting again after a predetermined time.

[0031]

In a Schottky diode composed of a metal and a semiconductor substrate, silicon (S) is used for a mirror image effect.
i) While the effective barrier is located at the back of the substrate, according to the present invention, the second semiconductor layer or the insulating layer having a higher dielectric constant than the semiconductor substrate is placed in the region where the depletion layer is spread. By forming, the effective barrier position is brought closer to the vicinity of the interface, and the decrease in the number of generated hot carriers is suppressed.

In the present invention, by forming the high dielectric constant layer, the tendency of the potential due to the mirror image effect becomes sharp, so that the barrier position of the effective potential, which is the sum of the mirror image effect and the potential of the Schottky diode depletion layer, is reduced. Utilizes approaching the interface.

[0033]

Embodiments of the present invention will be described below with reference to the drawings.

[0034]

Embodiment 1 FIG. 1 shows the structure of a Schottky photodetector according to an embodiment of the present invention. Referring to FIG. 1, a Schottky photodetector according to the present embodiment includes a platinum silicide (PtSi) film as a metal electrode (1) and a p-type silicon (p-Si) as a semiconductor substrate (2).
Titanium nitride (TiN) is formed as a high dielectric constant material (9) in a p-type silicon substrate of a PtSi / p-Si Schottky diode.

Considering the multiple reflection effect of hot holes,
The platinum silicide (PtSi) film uses 3 nm, and the p-type Si substrate uses boron-doped 30 to 50 Ωcm.

Then, p is set so that light can be incident from the back side.
The mold silicon substrate is mirror-polished on both sides.

Titanium nitride (TiN), which is a high dielectric constant material, is formed to a thickness of 1 nm from a position approximately 2 nm to 3 nm from the PtSi / p-Si interface (high dielectric constant material (9) is in the depletion region of the Schottky diode).

FIG. 2 shows the potential of the Schottky photodetector having the structure shown in FIG. FIG. 2A depicts the configuration of FIG. 1 as it is. The solid line in FIG.
The potential due to the structure of (A) is drawn.

The applied voltage of the Schottky diode is-
5 V (reverse bias). This solid line in FIG. 2B is the sum of the potential of the Schottky diode as a solution of the Poisson equation and the potential due to the mirror image effect.

In FIG. 2B, when deriving the two potentials, a one-dimensional profile model that takes into account the dielectric constant at each depth is used.

As a result, the effective barrier position x-effect
Is 3.0 nm from the PtSi / p-Si interface. Since the high dielectric layer (9) is a very thin film having a thickness of 1 nm, hot holes can pass through the high dielectric layer (9) by tunneling.

For comparison, the potential in the case where the high dielectric constant layer (9) is not formed (conventional example) is shown in FIG.
Are indicated by broken lines. In the conventional example, the effective barrier position is about 6.3 nm.

GF Exhibit 1126 - 355/2248

Next, an example of a method of driving a Schottky photodetector according to an embodiment of the present invention will be described with reference to FIG.

FIG. 3A is a diagram showing the potential of the Schottky photodetector having the structure shown in FIG. 1 under the condition of a reverse bias voltage of 5 V.

FIG. 3B is a diagram showing a potential under a condition of a reverse bias voltage of 6 V, and FIG. 3C is a diagram showing a potential under a condition of a reverse bias voltage of 7 V.

Referring to FIG. 3, it can be seen that the effective barrier height sharply decreases according to the value of the reverse bias voltage. The reverse bias voltage of 5 to 7 V is a condition for the reverse bias in a range where the effective barrier position is located in the high dielectric constant film.

As described above, the driving method of adjusting the reverse bias voltage so that the effective barrier position exists within the depth direction range of the high dielectric constant film greatly changes the effective Schottky barrier height with a small driving voltage difference. Can be done.

Further, since the effective barrier position is maintained in the vicinity of the interface, reduction of generated hot holes can be suppressed. Thereby, the sensitivity can be easily adjusted within the range while maintaining high sensitivity.

As the high dielectric constant layer (9), a compound semiconductor such as GaAs or InSb having a relative dielectric constant (electrostatic) higher than that of silicon (11.7) or Ge or the like may be used.

[0050]

Embodiment 2 A second embodiment of the method of driving a Schottky photodetector according to the present invention will be described.

In the driving method according to this embodiment, the Schottky photodetector having the structure shown in FIG. 1 is set to a floating state (floating state) immediately after resetting to a reverse bias voltage of 7 V, for example, 33 ms (millisecond; scanning). When resetting again after the period, the potential is read.

FIG. 4 shows the sensitivity characteristics of this driving method.
In FIG. 4, the horizontal axis is the amount of incident light, and the vertical axis is the read potential (signal potential).

As described with reference to FIG. 3, the sensitivity at a reverse bias voltage of 7 V is high, and the sensitivity is reduced strongly depending on the reverse bias voltage. Therefore, the sensitivity is high at low illuminance and the sensitivity is suppressed at high illuminance. Is done.

This tendency is similarly held in the conventional Schottky photodetector, but is slow as shown by the broken line in FIG.

In the present embodiment, as shown by the solid line in FIG. 4, the sensitivity characteristic is high at low illuminance (small irradiation light amount) (high readout potential) and does not saturate up to high illuminance. It can be said to be optimal for detecting physical phenomena whose relationship with infrared rays is close to logarithmic.

Although the present invention has been described with reference to the above embodiment, the present invention is not limited to the above embodiment but includes various embodiments according to the principle of the present invention.

[0057]

According to the Schottky photodetector of the present invention (claim 1), the decrease of the signal charge carriers in the movement from the metal / semiconductor interface to the effective barrier position is suppressed, and the photodetector has high sensitivity. Can be achieved.

The above-mentioned effects are similarly achieved by the preferred embodiments of the present invention.

According to the method of driving a Schottky photodetector of the present invention (claim 5), the disappearance of signal charges (carriers) during movement from the metal / semiconductor interface to the effective barrier position is suppressed. By applying a reverse bias voltage, high sensitivity of the photodetector can be achieved.

Further, according to the driving method of the present invention (claim 6), by using a driving method utilizing a sudden change in potential at the position of the high dielectric constant film, high sensitivity can be obtained at low illuminance, and A detector having a large dynamic range can be realized.

[Brief description of the drawings]

FIG. 1 is a diagram showing a configuration of an embodiment of a Schottky photodetector of the present invention.

FIG. 2A is a diagram showing a configuration of an embodiment of the present invention. (B) is a diagram showing the potential of the Schottky photodetector of one embodiment of the present invention.

FIG. 3 is a diagram showing the potential of the first embodiment of the driving method of the Schottky photodetector of the present invention. (A) ~
(C) is a diagram showing the potential when the bias voltage is variable.

FIG. 4 is a diagram showing sensitivity characteristics of a second embodiment of the driving method of the Schottky photodetector of the present invention.

FIG. 5A is a diagram showing a configuration of a conventional Schottky photodetector. (B) is a diagram showing the potential of the configuration of FIG. 5 (A). (C) is a diagram showing a potential in consideration of the mirror image effect.

FIG. 6A is a diagram showing another configuration of a conventional Schottky photodetector. FIG. 7B is a diagram showing the potential of the configuration of FIG.

[Description of Signs] 1 Metal electrode 2 Semiconductor substrate 3 Ohmic contact 4 Metallic Fermi level 5, 5 ', 5 "Depletion layer 6, 6' Potential 7 Reverse bias voltage 8 P^+ dopant 9 High dielectric constant material (High dielectric constant Layer) 100 light 200-202 hot hole

Cited By (1)

Publication number	Priority date	Publication date	Assignee	Title
Family To Family Citations				

GF Exhibit 1126 - 356/2248

FR2805395B1 *	2000-02-23	2002-05-10	Centre Nat Rech Scient	Mos transistor for high integration density circuits

* Cited by examiner, † Cited by third party, ‡ Family to family citation

Similar Documents

Publication	Publication Date	Title
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US10217889B2	2019-02-26	Clamped avalanche photodiode
US7009164B2	2006-03-07	Photoelectric converter method for driving photoelectric converter and system having photoelectric converter for image formation converted from radiation
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AU2005273818B2	2010-09-23	Semiconductor radiation detector with a modified internal gate structure
DE3104489C2	1991-01-31	
US7148551B2	2006-12-12	Semiconductor energy detector
US7723667B2	2010-05-25	Phototransistor with source layer between barrier layer and photosensitive semiconductor layer and a gate layer for controlling the barrier height of the barrier layer
JP4309574B2	2009-08-05	Photodiode and sensor array
US5317174A	1994-05-31	Bulk charge modulated device photocell
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CA1298389C	1992-03-31	High dynamic range charge-coupled device
US4731665A	1988-03-15	Image sensing apparatus with read-out of selected combinations of lines
JP2784020B2	1998-08-06	Schottky barrier photodiode with groove for infrared detection
US4198646A	1980-04-15	Monolithic imager for near-IR
Rosbeck et al.	1982	Background and temperature dependent current-voltage characteristics of HgCdTe photodiodes
US6815791B1	2004-11-09	Buried, fully depletable, high fill factor photodiodes
US4672455A	1987-06-09	Solid-state image-sensor having reverse-biased substrate and transfer registers

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
JP6271855A	1994-10-12	1994-10-12	Schottky photodetector and driving method thereof

Applications Claiming Priority (1)

Application	Filing date	Title
JP6271855A	1994-10-12	Schottky photodetector and driving method thereof

Legal Events

Date	Code	Title	Description
1997-03-04	A01	Written decision to grant a patent or to grant a registration (utility model)	**Free format text**: JAPANESE INTERMEDIATE CODE: A01 **Effective date**: 19970304

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	29/78				29/78	３０１Ｙ
	21/336					

審査請求　未請求　請求項の数17　ＯＬ　（全　８　頁）

(21)出願番号　特願平8－178829

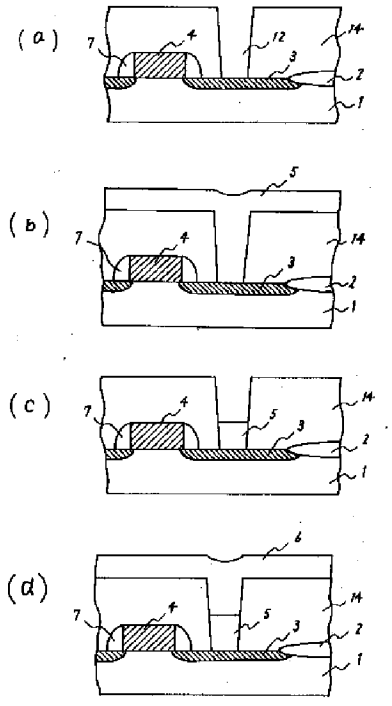
(22)出願日　平成８年(1996)７月９日

(71)出願人　000006013
三菱電機株式会社
東京都千代田区丸の内二丁目２番３号
(72)発明者　西岡　康隆
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　山川　聡
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　金本　恭三
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(74)代理人　弁理士　大岩　増雄

最終頁に続く

(54)【発明の名称】　集積化半導体素子

(57)【要約】
【課題】　従来の集積化半導体素子は、多結晶シリコン配線形成後の熱処理工程によって、前記多結晶シリコンの不純物が半導体基板へ拡散し、トランジスタの特性に悪影響を及ぼすという問題点があった。
【解決手段】　半導体基板上１に形成された電気的活性領域に対して電気的に接続された第一の多結晶シリコン５と、この第一の多結晶シリコン５上に形成された第二の多結晶シリコン６とを備え、第一の多結晶シリコン５と第二の多結晶シリコン６との不純物の種類及び濃度のいずれか一方または両方が異なるように形成する。



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【特許請求の範囲】
【請求項１】　半導体基板上に形成された電気的活性領域に対して、不純物を含有した多結晶シリコンを用いて電気的接続を行う集積化半導体素子において、前記多結晶シリコンと前記半導体基板との間に前記不純物が前記半導体基板への拡散を防止する不純物拡散防止層を形成したことを特徴とする集積化半導体素子。
【請求項２】　多結晶シリコン上に金属シリサイド化合物を形成したことを特徴とする請求項１記載の集積化半導体素子。
【請求項３】　半導体基板上に形成された電気的活性領域に対して電気的に接続された第一の多結晶シリコンと、この第一の多結晶シリコン上に形成された第二の多結晶シリコンとを備え、前記第一の多結晶シリコンと前記第二の多結晶シリコンとの不純物の種類及び濃度のいずれか一方または両方が異なることを特徴とする集積化半導体素子。
【請求項４】　第一の多結晶シリコンの不純物の濃度は、第二の多結晶シリコンの不純物の濃度よりも薄いことを特徴とする請求項３記載の集積化半導体素子。
【請求項５】　第一の多結晶シリコンは、不純物を含まない多結晶シリコンであることを特徴とする請求項３記載の集積化半導体素子。
【請求項６】　第一の多結晶シリコン及び第二の多結晶シリコンの不純物は、リン、ホウ素、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも１つであることを特徴とする請求項３から５のいずれか一項に記載の集積化半導体素子。
【請求項７】　第二の多結晶シリコン上に金属シリサイド化合物が形成されたことを特徴とする請求項３から６のいずれか一項に記載の集積化半導体素子。
【請求項８】　半導体基板上に形成された電気的活性領域に対して電気的に接続された第一の多結晶シリコンと、この第一の多結晶シリコン上に形成された金属シリサイド化合物とを備えたことを特徴とする集積化半導体素子。
【請求項９】　第一の多結晶シリコンと半導体基板との間に、第一の多結晶シリコン及び第二の多結晶シリコンの不純物が前記半導体基板への拡散を防止する不純物拡散防止層を形成したことを特徴とする請求項３から８のいずれか一項に記載の集積化半導体素子。
【請求項１０】　半導体基板上に形成された電気的活性領域に対して不純物を含有した多結晶シリコンを用いて電気的接続を行う半導体素子において、前記多結晶シリコンの含有する不純物の濃度を層状に連続的に変化させて形成することを特徴とする集積化半導体素子。
【請求項１１】　多結晶シリコンの下層から上層に向かって不純物の濃度が連続的に増加していることを特徴とする請求項１０記載の集積化半導体素子。
【請求項１２】　多結晶シリコン上に金属シリサイド化合物が形成されたことを特徴とする請求項１０または１１記載の集積化半導体素子。
【請求項１３】　多結晶シリコンと半導体基板との間に、前記多結晶シリコンの含有する不純物が前記半導体基板への拡散を防止する不純物拡散防止層を形成したことを特徴とする請求項１０から１２のいずれか一項に記載の集積化半導体素子。
【請求項１４】　多結晶シリコンに含有させる不純物は、リン、ホウ素、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも１つであることを特徴とする請求項１０から１３のいずれか一項に記載の集積化半導体素子。
【請求項１５】　不純物拡散防止層は、窒化チタン、酸化シリコン、窒化シリコンの少なくとも一つであることを特徴とする請求項１、９、１３のいずれか一項に記載の集積化半導体素子。
【請求項１６】　金属シリサイド化合物は、ニッケルシリサイド、コバルトシリサイド、タングステンシリサイド、チタンシリサイド、アルミニウムシリサイド、ルテニウムシリサイドの少なくとも一つであることを特徴とする請求項２、７、８、１２のいずれか一項に記載の集積化半導体素子。
【請求項１７】　半導体基板上に形成された電気的活性領域に対して不純物を含有した多結晶シリコンを用いて電気的接続を行う半導体素子において、前記多結晶シリコンの不純物は、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも一つであることを特徴とする集積化半導体素子。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は、活性な素子領域が二つ以上存在し、その活性な領域の間を電気的に接続する手段の一部又は全部に不純物を含有させた多結晶シリコンを用いた集積化半導体素子に関するものである。
【０００２】
【従来の技術】図９は、従来の集積化半導体素子を示す図であり、図において、１は半導体基板、２は素子分離、３はＭＯＳ型トランジスタのソース／ドレイン領域、４はゲート電極、７はサイドウォール、１３は不純物を含有させた多結晶シリコンを用いた配線、１４は層間絶縁膜である。また図１０は、図９の集積化半導体素子のソース／ドレイン領域３と多結晶シリコン１３との接続部を拡大した図である。図において、破線１１は多結晶シリコン１３の不純物の半導体基板１内への拡散範囲を示すものである。
【０００３】集積化半導体素子においては、通常、配線材料としてアルミニウムあるいはアルミニウムを含む合金が用いられるが、配線を形成したあとの工程では最高４５０℃の温度制限が生じ、熱を加える必要のある処理の工程や金属による汚染が問題となる工程を配線工程後

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に行うことができない。そのために、金属の配線を形成するまでに配線を形成する必要が生じた場合には、導電性を持つ不純物を含有させた多結晶シリコン１３を用いる。この不純物には一般的にはリンあるいはホウ素等が用いられる。また、このような配線は金属配線に比べると抵抗が高いため、抵抗を下げるために不純物が過飽和に近い濃度まで多結晶シリコン中に含有されており、例えばＴｉＳｉ２やＷＳｉ２等の金属シリサイドと多層構造にしてさらに抵抗を下げる方法が用いられることもある。

【０００４】

【発明が解決しようとする課題】従来の集積化半導体素子は以上のように構成されているので、図１０に示すように、多結晶シリコン配線形成後の熱処理工程によって、多結晶シリコン１３からシリコン基板１へ不純物が染み出す現象が生じていた。これは半導体基板１上に形成されたＭＯＳトランジスタのソースドレインを形成している接合の位置に対して、例えば破線１１の位置まで不純物が拡散するような結果を生じるため、ＭＯＳトランジスタの特性、例えばサブスレッショルド電圧（Ｖｔｈ）やソースドレイン耐圧（ＢＶｄｓ）を変動させることが従来から懸念されていた。さらに半導体素子の微細化が進むに連れてゲート電極４と多結晶シリコン１３の接続位置がますます短くなってきており、トランジスタ特性に与える影響がさらに大きくなるという問題点も有していた。

【０００５】この発明は上記のような問題点を解決するためになされたもので、多結晶シリコンから半導体基板への不純物の拡散を抑えることにより、ＭＯＳトランジスタ特性への影響を防止し、高性能な集積化半導体素子を得ることを目的とする。

【０００６】

【課題を解決するための手段】この発明に係る集積化半導体装置は、半導体基板上に形成された電気的活性領域に対して、不純物を含有した多結晶シリコンを用いて電気的接続を行う集積化半導体素子において、前記多結晶シリコンと前記半導体基板との間に前記不純物が前記半導体基板への拡散を防止する不純物拡散防止層を形成したものである。

【０００７】また、多結晶シリコン上に金属シリサイド化合物を形成したものである。

【０００８】また、半導体基板上に形成された電気的活性領域に対して電気的に接続された第一の多結晶シリコンと、この第一の多結晶シリコン上に形成された第二の多結晶シリコンとを備え、前記第一の多結晶シリコンと前記第二の多結晶シリコンとの不純物の種類及び濃度のいずれか一方または両方が異なるものである。

【０００９】また、第一の多結晶シリコンの不純物の濃度は、第二の多結晶シリコンの不純物の濃度よりも薄いものである。

【００１０】また、第一の多結晶シリコンは、不純物を含まない多結晶シリコンである。

【００１１】また、第一の多結晶シリコン及び第二の多結晶シリコンの不純物は、リン、ホウ素、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも１つである。

【００１２】また、第二の多結晶シリコン上に金属シリサイド化合物が形成されたものである。

【００１３】また、半導体基板上に形成された電気的活性領域に対して電気的に接続された第一の多結晶シリコンと、この第一の多結晶シリコン上に形成された金属シリサイド化合物とを備えたものである。

【００１４】また、第一の多結晶シリコンと半導体基板との間に、第一の多結晶シリコン及び第二の多結晶シリコンの不純物が前記半導体基板への拡散を防止する不純物拡散防止層を形成したものである。

【００１５】また、半導体基板上に形成された電気的活性領域に対して不純物を含有した多結晶シリコンを用いて電気的接続を行う半導体素子において、前記多結晶シリコンの含有する不純物の濃度を層状に連続的に変化させて形成するものである。

【００１６】また、多結晶シリコンの下層から上層に向かって不純物の濃度が連続的に増加しているものである。

【００１７】また、多結晶シリコン上に金属シリサイド化合物が形成されたものである。

【００１８】また、多結晶シリコンと半導体基板との間に、前記多結晶シリコンの含有する不純物が前記半導体基板への拡散を防止する不純物拡散防止層を形成したものである。

【００１９】また、多結晶シリコンに含有させる不純物は、リン、ホウ素、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも１つである。

【００２０】また、不純物拡散防止層は、窒化チタン、酸化シリコン、窒化シリコンの少なくとも一つである。

【００２１】また、金属シリサイド化合物は、ニッケルシリサイド、コバルトシリサイド、タングステンシリサイド、チタンシリサイド、アルミニウムシリサイド、ルテニウムシリサイドの少なくとも一つである。

【００２２】また、半導体基板上に形成された電気的活性領域に対して不純物を含有した多結晶シリコンを用いて電気的接続を行う半導体素子において、前記多結晶シリコンの不純物は、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも一つである。

【００２３】

【発明の実施の形態】

実施の形態１．以下、この発明の実施の一形態を図について説明する。図１はこの発明の実施の形態１による集積化半導体素子を示す断面図である。図において、１は半導体基板、２は素子分離、３はＭＯＳトランジスタの

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ソース／ドレイン領域、４はゲート電極、５は第一の多結晶シリコン、６は第二の多結晶シリコン、７はサイドウォール、１２は接続孔、１４は層間絶縁膜を示す。また図２は、図１の集積化半導体素子のソース／ドレイン領域３と多結晶シリコン５との接続部を拡大した図である。図において、破線１１ａは第一の多結晶シリコン５の不純物の半導体基板１内への拡散範囲を示すものである。

【００２４】以下、図１に沿って製作方法を説明する。半導体基板１上に従来の手法により素子分離２、ゲート電極４、ソースドレイン領域３を造り込み、層間絶縁膜１４を形成して配線層の接続孔１２をエッチングの手法で開孔する（図１ａ）。次にソースドレイン領域３の不純物濃度よりも十分薄い不純物濃度を持つ第一の多結晶シリコン５を成膜し（図１ｂ）、第一の多結晶シリコン５を全面エッチングして接続孔１２の内部に適当な厚さを残す（図１ｃ）。第一の多結晶シリコン５の厚さは、接続孔１２の深さにもよるが、おおむね２０ｎｍから５０ｎｍ程度が良好な特性を示す。続いてこの上部に第二の多結晶シリコン６を成膜し、所望の配線形状となるように写真製版、エッチングの工程を行う。なお、第一の多結晶シリコン５の不純物濃度は$1\times10^{15}cm^{-3}$から$1\times10^{17}cm^{-3}$程度に設定するのが望ましいが、これは第二の多結晶シリコン６とソース／ドレイン領域３の不純物濃度と比較して決定するのが望ましい。場合によっては不純物を含有させずに用いることもできる。また、第二の多結晶シリコン６はそのまま配線としても用いるため抵抗を低く抑える必要がある。よって不純物濃度は、第一の多結晶シリコン５の不純物濃度よりも濃い$1\times10^{20}cm^{-3}$から$1\times10^{21}cm^{-3}$程度に設定するのが望ましい。

【００２５】以上のように本実施の形態では、不純物濃度の濃い第二の多結晶シリコン６の直下に、不純物濃度の薄い第一の多結晶シリコン５形成したことを特徴としているため、図２の矢印に示すように、配線工程形成後の熱処理で第二の多結晶シリコン６からの不純物の拡散は第一の多結晶シリコン５を経由して進むため、結果として半導体基板１内を拡散する距離が小さくなる。一方、第一の多結晶シリコン５から半導体基板１内への不純物の拡散は、第一の多結晶シリコン５の不純物濃度がソースドレイン領域３の不純物濃度より十分薄いためほとんど無視することができ、不純物の拡散位置を実質的に１１ａの破線の位置まで抑えることができる。第一の多結晶シリコン５の不純物濃度が薄い場合、半導体基板１との接続部の抵抗の上昇が懸念されるが、第一の多結晶シリコン５の高さを２０ｎｍから５０ｎｍ程度に抑えることにより抵抗の上昇を最小限にすること、及び第二の多結晶シリコン６からの不純物の拡散により第一の多結晶シリコン５の不純物濃度は上昇するため、実際には成膜時よりも低抵抗となりほとんど無視できるようになる。さらに低抵抗にするためには第二の多結晶シリコン６の上層に、ニッケルシリサイド、コバルトシリサイド、タングステンシリサイド、チタンシリサイド、アルミニウムシリサイド、ルテニウムシリサイドの少なくとも一つからなる金属シリサイド層を張り合わせて一体化したいわゆるポリサイド構造にすることも可能である。

【００２６】実施の形態２．第一の多結晶シリコン５及び第二の多結晶シリコン６に含有させる不純物としては、Ｎ型ではリン、Ｐ型ではホウ素が一般的であるが、第一の多結晶シリコン５と第二の多結晶シリコン６の両方、または第二の多結晶シリコン６のみに、リンやホウ素よりも重い原子である、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも１つを用いることによってさらに大きな効果が得られる。即ち、重い原子を不純物に用いているため、半導体基板１内への不純物の拡散が遅くなる。特に、第一の多結晶シリコン５のみに含有させる場合、必ずしも第二の多結晶シリコン６より不純物濃度を薄くする必要がなく、場合によっては第二の多結晶シリコン６と同程度の不純物濃度でも問題とならない場合もある。

【００２７】実施の形態３．図３は、この発明の実施の形態３による集積化半導体素子を示す断面図である。図に示すように、第一の多結晶シリコン５の成膜したときの膜厚によっては接続孔１２の側面にも第一の多結晶シリコン５が形成される場合があるが、この場合でも、第二の多結晶シリコン６の不純物は第一の多結晶シリコン５の領域を経由して拡散するため、上記実施の形態１と同様の効果が得られる。

【００２８】実施の形態４．上記実施の形態１では、接続孔１２の内部に不純物濃度の薄い第一の多結晶シリコン５を埋め込んで形成したが、図４に示すように第二の多結晶シリコン６の直下に第二の多結晶シリコン６よりも不純物濃度の薄い第三の多結晶シリコン８を連続して成膜し、第二の多結晶シリコン６と第三の多結晶シリコン８とを同時に加工して第三の多結晶シリコン８も配線の一部に用いても同様の効果が得られる。この時にも第三の多結晶シリコン８による抵抗の上昇が懸念されるが、上記実施の形態１と同様の手法によりほとんど問題とはならない。

【００２９】また、上記実施の形態２と同様に、第二及び第三の多結晶シリコンあるいは第三の多結晶シリコン８のみに含有させる不純物として、リンやホウ素よりも重い原子に当たるヒ素やアンチモン、インジウムガリウムなどを用いることによってさらに大きな効果が得られる。特に、第三の多結晶シリコン８のみに含有させる場合は必ずしも第二の多結晶シリコン６よりも不純物濃度を薄くする必要があるわけではなく、場合によっては第二の多結晶シリコン６と同程度の不純物濃度でも問題とならない場合もある。また、さらに低抵抗にするためには、上記実施の形態１と同様に、第二の多結晶シリコン

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６上に金属シリサイド層を張り合わせて一体化したいわゆるポリサイド構造にすることも可能であることは言うまでもない。

【００３０】実施の形態５．上記実施の形態１では、接続孔１２の内部に不純物濃度の薄い第一の多結晶シリコン５を埋め込んで形成したが、図５に示すように、第一の多結晶シリコンの代りに不純物の拡散を阻止する導電性の不純物拡散防止層（以下、バリア層と呼ぶ）９を薄く形成しても同様の効果が得られる。この場合にはバリア層９の材料としては種々のものがあるが、金属系の材料としては窒化チタン、窒化シリコンが有り、その他絶縁体であるシリコン酸化膜（数Åから２０Å程度の膜厚）も、電子のトンネル効果によって導電性を持つためバリア層として用いることができる。このバリア層は上記実施の形態１から４の構造に併用しても当然有効である。

【００３１】実施の形態６．上記実施の形態４では、第二の多結晶シリコン６の直下に第二の多結晶シリコン６よりも不純物濃度の薄い第三の多結晶シリコン８を連続して成膜したが、図６に示すように、第二の多結晶シリコン６の成膜時に成膜開始から成膜終了まで連続的に不純物の濃度が濃くなるように成膜しても同様の効果が得られる。成膜開始の不純物濃度は、上記実施の形態１に示した第一の多結晶シリコン５と同じ程度かあるいは不純物無しの状態とし、最終的には上記実施の形態１に示した第二の多結晶シリコンと同じ程度の濃度にするのが望ましい。また、当然ながら上記実施の形態１のポリサイド構造や、上記実施の形態５のバリア層と併用しても有効であることは言うまでもない。

【００３２】実施の形態７．上記実施の形態４では、第二の多結晶シリコン６の直下に第二の多結晶シリコン６よりも不純物濃度の薄い第三の多結晶シリコン８を連続して成膜したが、図７に示すように第一及び第二の多結晶シリコンの成膜したときの各々の膜厚によっては、第二の多結晶シリコンの上層に形成したタングステンシリサイドなどの金属シリサイド層１５が接続孔１２内部に形成される場合もある。この場合でも上記実施の形態３と同様の効果が得られると共に、接続孔１２の抵抗が低減するという効果がある。当然ながら上記実施の形態５のバリア層と併用しても有効であることは言うまでもない。

【００３３】実施の形態８．上記実施の形態１では、不純物濃度の薄い第一の多結晶シリコン５の上に、不純物濃度の濃い第二の多結晶シリコン６を形成したが、図８に示すように第二の多結晶シリコン６の代わりに、ニッケルシリサイド、コバルトシリサイド、タングステンシリサイド、チタンシリサイド、アルミニウムシリサイド、ルテニウムシリサイドの少なくとも一つの金属シリサイドからなる金属シリサイド層１５を形成しても良い。この場合も上記実施の形態５のバリア層と併用することが可能である。

【００３４】

【発明の効果】以上のように請求項１記載の発明によれば、半導体基板上に形成された電気的活性領域に対して、不純物を含有した多結晶シリコンを用いて電気的接続を行う集積化半導体素子において、多結晶シリコンと半導体基板との間に不純物が半導体基板への拡散を防止する不純物拡散防止層を形成したので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００３５】また、請求項２記載の発明によれば、多結晶シリコン上に金属シリサイド化合物を形成したので、多結晶シリコンの不純物濃度を上げることなくさらに低抵抗にする効果が得られる。

【００３６】また、請求項３記載の発明によれば、半導体基板上に形成された電気的活性領域に対して電気的に接続された第一の多結晶シリコンと、この第一の多結晶シリコン上に形成された第二の多結晶シリコンとを備え、第一の多結晶シリコンと第二の多結晶シリコンとの不純物の種類及び濃度のいずれか一方または両方が異なるので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００３７】また、請求項４記載の発明によれば、第一の多結晶シリコンの不純物の濃度は、第二の多結晶シリコンの不純物の濃度よりも薄いので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００３８】また、請求項５記載の発明によれば、第一の多結晶シリコンは、不純物を含まない多結晶シリコンであるので、不純物が半導体基板へ拡散することはなく、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００３９】また、請求項６記載の発明によれば、第一の多結晶シリコン及び第二の多結晶シリコンの不純物は、リン、ホウ素、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも１つであるので、半導体基板への不純物の拡散をさらに抑制する効果が得られる。

【００４０】また、請求項７記載の発明によれば、第二の多結晶シリコン上に金属シリサイド化合物が形成されているので、多結晶シリコンの不純物濃度を上げることなくさらに低抵抗にする効果が得られる。

【００４１】また、請求項８記載の発明によれば、半導体基板上に形成された電気的活性領域に対して電気的に

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接続された第一の多結晶シリコンと、この第一の多結晶シリコン上に形成された金属シリサイド化合物とを備えたので、多結晶シリコンの不純物濃度を上げることなくさらに低抵抗にする効果が得られる。

【００４２】また、請求項９記載の発明によれば、第一の多結晶シリコンと半導体基板との間に、第一の多結晶シリコン及び第二の多結晶シリコンの不純物が半導体基板への拡散を防止する不純物拡散防止層を形成したので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００４３】また、請求項１０記載の発明によれば、半導体基板上に形成された電気的活性領域に対して不純物を含有した多結晶シリコンを用いて電気的接続を行う半導体素子において、多結晶シリコンの含有する不純物の濃度を層状に連続的に変化させて形成するので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００４４】また、請求項１１記載の発明によれば、多結晶シリコンの下層から上層に向かって不純物の濃度が連続的に増加しているので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００４５】また、請求項１２記載の発明によれば、多結晶シリコン上に金属シリサイド化合物が形成されているので、多結晶シリコンの不純物濃度を上げることなくさらに低抵抗にする効果が得られる。

【００４６】また、請求項１３記載の発明によれば、多結晶シリコンと半導体基板との間に、多結晶シリコンの含有する不純物が前記半導体基板への拡散を防止する不純物拡散防止層を形成したので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００４７】また、請求項１４記載の発明によれば、多結晶シリコンに含有させる不純物は、リン、ホウ素、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも１つであるので、半導体基板への不純物の拡散をさらに抑制する効果が得られる。

【００４８】また、請求項１５記載の発明によれば、不純物拡散防止層は、窒化チタン、酸化シリコン、窒化シリコンの少なくとも一つであるので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【００４９】また、請求項１６記載の発明によれば、金属シリサイド化合物は、ニッケルシリサイド、コバルトシリサイド、タングステンシリサイド、チタンシリサイド、アルミニウムシリサイド、ルテニウムシリサイドの少なくとも一つであるので、低抵抗にする効果が得られる。

【００５０】また、請求項１７記載の発明によれば、半導体基板上に形成された電気的活性領域に対して不純物を含有した多結晶シリコンを用いて電気的接続を行う半導体素子において、多結晶シリコンの不純物は、ヒ素、アンチモン、ビスマス、ガリウム、インジウム、タリウムの少なくとも一つであるので、多結晶シリコンの不純物が半導体基板へ拡散するのを効果的に抑制でき、ＭＯＳトランジスタなどの素子性能の劣化を生じない高性能な集積化半導体素子を製作できる効果が得られる。

【図面の簡単な説明】

【図１】　この発明の実施の形態１による集積化半導体素子を示す断面構造図である。

【図２】　この発明の実施の形態２による集積化半導体素子を示す断面構造図である。

【図３】　この発明の実施の形態３による集積化半導体素子を示す断面構造図である。

【図４】　この発明の実施の形態４による集積化半導体素子を示す断面構造図である。

【図５】　この発明の実施の形態５による集積化半導体素子を示す断面構造図である。

【図６】　この発明の実施の形態６による集積化半導体素子を示す断面構造図である。

【図７】　この発明の実施の形態７による集積化半導体素子を示す断面構造図である。

【図８】　この発明の実施の形態８による集積化半導体素子を示す断面構造図である。

【図９】　従来の集積化半導体素子を示す断面構造図である。

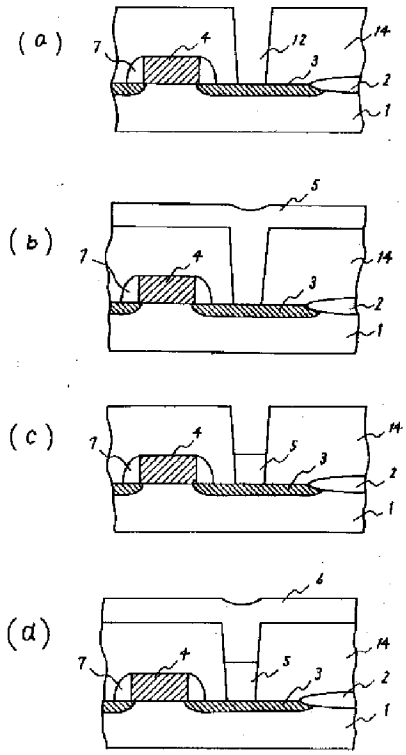
【図１０】　従来の集積化半導体素子を説明するための断面模式図である。

【符号の説明】

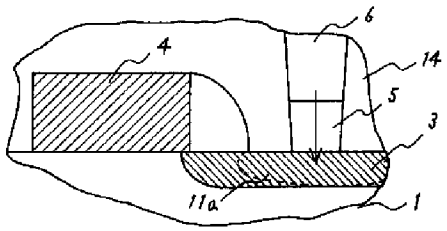
１　半導体基板、２　素子分離、３　ソース／ドレイン領域、４　ゲート電極、５　第一の多結晶シリコン、６　第二の多結晶シリコン、７　サイドウォール、８　第三の多結晶シリコン、９　不純物拡散防止（バリア）層、１０　不純物の濃度勾配を持つ多結晶シリコン、１１　多結晶シリコンから拡散した不純物の領域、１２　接続孔、１３　多結晶シリコン、１４　層間絶縁膜、１５　金属シリサイド層

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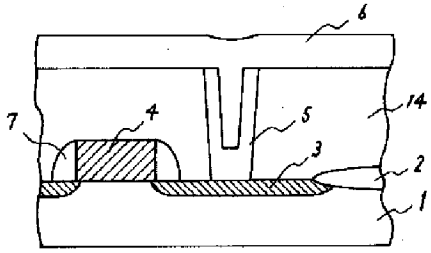
【図1】



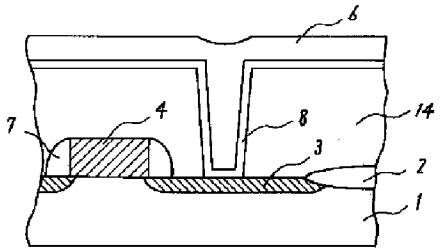
【図2】



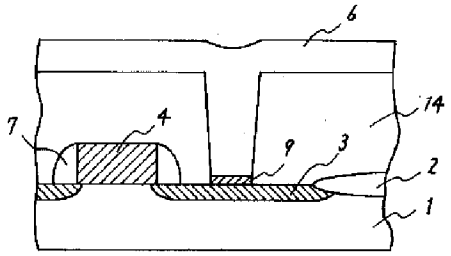
【図3】



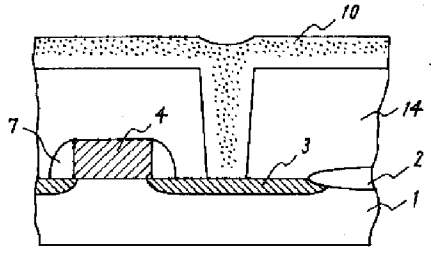
【図4】



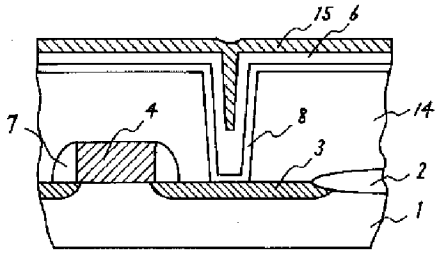
【図5】



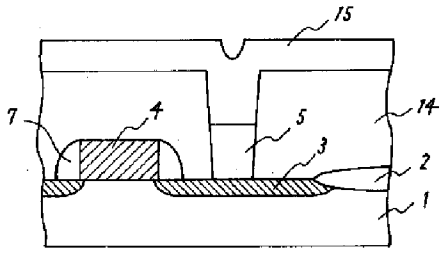
【図6】



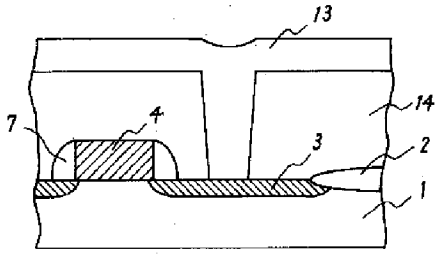
【図7】



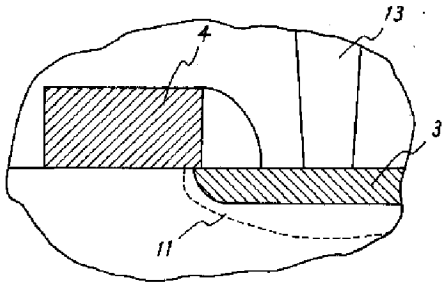
【図８】



【図９】



【図１０】



フロントページの続き

(72)発明者　阿部　雄次
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　徳田　安紀
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　須賀原　和之
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　大森　達夫
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内
(72)発明者　安村　賢二
東京都千代田区丸の内二丁目２番３号　三菱電機株式会社内

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JPH1027847A INTEGRATED SEMICONDUCTOR DEVICE

Applicants: MITSUBISHI ELECTRIC CORP

Inventors: ABE YUJI,KANEMOTO KYOZO,NISHIOKA YASUTAKA,OMORI TATSUO,SUGAHARA KAZUYUKI,TOKUDA YASUKI,YAMAKAWA SATOSHI,YASUMURA KENJI

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INTEGRATED SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To prevent deterioration in the device performance of a MOS transistor, etc., by a method wherein an impurity diffusion preventing layer, with which the diffusion of impurities into a semiconductor substrate is prevented, is formed between polycrystalline silicon and the semiconductor substrate. SOLUTION: In an integrated semiconductor device wherein an electric active region 3 formed on a semiconductor substrate 1 is electrically connected using impurity-containing polycrystalline silicon 6, an impurity diffusion preventing layer 5, which prevents the diffusion of impurities into the semiconductor substrate 1, is formed between the polycrystalline 6 and the semiconductor substrate 1. For example, a MOS transistor is formed on the semiconductor substrate 1, an interlayer insulating film 14 is formed and a contact hole 12 is opened. Then, the first polycrystalline silicon film 5, having the impurity density sufficiently lower than a source and drain region 3 is formed, and a suitable thickness of the film is left inside the contact hole 12 by etching the whole surface. Subsequently, the second polycrystalline silicon 6 is formed on over the contact hole 12, and an etching treatment is conducted so as to obtain the desired wiring form.

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DESCRIPTION JPH1027847

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to polycrystalline silicon in which two or more active element regions are present and impurities are contained in a part or all of means for electrically connecting the active regions. The present invention relates to the integrated semiconductor device used.

[0002]

2. Description of the Related Art FIG. 9 is a diagram showing a conventional integrated semiconductor device, in which 1 is a semiconductor substrate, 2 is element isolation, 3 is a source / drain region of a MOS transistor, 4 is a gate electrode, Reference numeral 7 is a sidewall, 13 is a wiring using polycrystalline silicon containing impurities, and 14 is an interlayer insulating film. Further, FIG. 10 is an enlarged view of a connecting portion between the source / drain region 3 and the polycrystalline silicon 13 of the integrated semiconductor device of FIG. In the figure, a broken line 11 indicates a diffusion range of impurities of the polycrystalline silicon 13 into the semiconductor substrate 1.

[0003]

In an integrated semiconductor device, aluminum or an alloy containing aluminum is usually used as a wiring material, but a temperature limitation of up to 450 ° C occurs in the process

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after forming the wiring, and a process step in which heat needs to be applied. It is not possible to perform a process in which metal contamination is a problem after the wiring process. Therefore, if it is necessary to form the wiring before the metal wiring is formed, the polycrystalline silicon 13 containing the conductive impurities is used. Phosphorus, boron or the like is generally used for this impurity. Further, since such a wiring has a higher resistance than a metal wiring, impurities are contained in polycrystalline silicon to a concentration close to supersaturation in order to reduce the resistance. For example, a metal silicide such as TiSi2 or WSi2 and a multi-layer structure are formed. Then, a method of further lowering the resistance may be used.

[0004]

Since the conventional integrated semiconductor device is constructed as described above, as shown in FIG. 10, the polycrystalline silicon 13 is converted into silicon by the heat treatment process after the polycrystalline silicon wiring is formed. The phenomenon in which impurities permeate the substrate 1 has occurred. This results in impurities diffusing to the position of the junction forming the source / drain of the MOS transistor formed on the semiconductor substrate 1, for example, to the position of the broken line 11, so that the characteristics of the MOS transistor, for example, It has been conventionally feared that the subthreshold voltage (Vth) and the source / drain breakdown voltage (BVds) are changed. Further, as the miniaturization of the semiconductor element progresses, the connection position between the gate electrode 4 and the polycrystalline silicon 13 is becoming shorter and shorter, and there is a problem that the influence on the transistor characteristics is further increased.

[0005]
The present invention has been made to solve the above problems, and suppresses the diffusion of impurities from polycrystalline silicon into a semiconductor substrate, thereby preventing the influence on the MOS transistor characteristics and achieving high-performance integration. The purpose is to obtain a semiconductor device.

[0006]
SUMMARY OF THE INVENTION An integrated semiconductor device according to the present invention is an integrated semiconductor device which is electrically connected to an electrically active region formed on a semiconductor substrate by using polycrystalline silicon containing impurities. In the semiconductor device, an impurity diffusion preventing layer for preventing the impurities from diffusing into the semiconductor substrate is formed between the polycrystalline silicon and the semiconductor substrate.

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[0007]
Also, a metal silicide compound is formed on polycrystalline silicon.

[0008]
In addition, the first polycrystalline silicon electrically connected to the electrically active region formed on the semiconductor substrate, and the second polycrystalline silicon formed on the first polycrystalline silicon The first polycrystalline silicon and the second polycrystalline silicon are different from each other in one or both of the type and concentration of impurities.

[0009]
The impurity concentration of the first polycrystalline silicon is lower than the impurity concentration of the second polycrystalline silicon.

[0010]
The first polycrystalline silicon is polycrystalline silicon containing no impurities.

[0011]
The impurities of the first polycrystalline silicon and the second polycrystalline silicon are at least one of phosphorus, boron, arsenic, antimony, bismuth, gallium, indium and thallium.

[0012]
Further, the metal silicide compound is formed on the second polycrystalline silicon.

[0013]
Further, a device including a first polycrystalline silicon electrically connected to an electrically active region formed on a semiconductor substrate and a metal silicide compound formed on the first polycrystalline silicon. Is.

[0014]
Further, an impurity diffusion preventing layer for preventing impurities of the first polycrystalline silicon and the second polycrystalline silicon from diffusing into the semiconductor substrate is formed between the first polycrystalline silicon and the

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semiconductor substrate. is there.

[0015]
Further, in a semiconductor element that electrically connects to an electrically active region formed on a semiconductor substrate using polycrystalline silicon containing impurities, the concentration of impurities contained in the polycrystalline silicon is continuously layered. It is formed by changing to.

[0016]
Further, the concentration of impurities continuously increases from the lower layer to the upper layer of polycrystalline silicon.

[0017]
In addition, a metal silicide compound is formed on polycrystalline silicon.

[0018]
Further, an impurity diffusion preventing layer for preventing impurities contained in the polycrystalline silicon from diffusing into the semiconductor substrate is formed between the polycrystalline silicon and the semiconductor substrate.

[0019]
The impurity contained in the polycrystalline silicon is at least one of phosphorus, boron, arsenic, antimony, bismuth, gallium, indium and thallium.

[0020]
The impurity diffusion prevention layer is at least one of titanium nitride, silicon oxide, and silicon nitride.

[0021]
The metal silicide compound is at least one of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, aluminum silicide, and ruthenium silicide.

[0022]

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Further, in a semiconductor element that electrically connects to an electrically active region formed on a semiconductor substrate using polycrystalline silicon containing impurities, the impurities of the polycrystalline silicon are arsenic, antimony, bismuth, and gallium. At least one of indium and thallium.

[0023]

BEST MODE FOR CARRYING OUT THE INVENTION Embodiment 1.

An embodiment of the present invention will be described below with reference to the drawings.

1 is a sectional view showing an integrated semiconductor device according to Embodiment 1 of the present invention.

In the figure, 1 is a semiconductor substrate, 2 is element isolation, 3 is a source / drain region of a MOS transistor, 4 is a gate electrode, 5 is first polycrystalline silicon, 6 is second polycrystalline silicon, and 7 is a sidewall. , 12 are connection holes, and 14 is an interlayer insulating film.

2 is an enlarged view of a connection portion between the source / drain region 3 and the polycrystalline silicon 5 of the integrated semiconductor device of FIG.

In the figure, a broken line 11a indicates a diffusion range of impurities of the first polycrystalline silicon 5 into the semiconductor substrate 1.

[0024]

The manufacturing method will be described below with reference to FIG.

The element isolation 2, the gate electrode 4, and the source / drain region 3 are formed on the semiconductor substrate 1 by the conventional method, the interlayer insulating film 14 is formed, and the connection hole 12 of the wiring layer is opened by the etching method (FIG.

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1a).).

Next, the first polycrystalline silicon 5 having an impurity concentration sufficiently lower than that of the source / drain region 3 is formed (FIG. 1b), and the first polycrystalline silicon 5 is entirely etched to form the inside of the contact hole 12. Leaving an appropriate thickness for the (Fig. 1c).

Although the thickness of the first polycrystalline silicon 5 depends on the depth of the connection hole 12, approximately 20 nm to 50 nm exhibits good characteristics.

Then, a second polycrystalline silicon 6 is formed on the upper portion of the film, and photolithography and etching steps are performed so as to obtain a desired wiring shape.

The impurity concentration of the first polycrystalline silicon 5 is preferably set to about 1 × 10 15 cm −3 to 1 × 10 17 cm −3, but this is the impurity concentration of the second polycrystalline silicon 6 and the source / drain regions 3. It is desirable to determine it by comparing with the concentration.

In some cases, it can be used without containing impurities.

Further, since the second polycrystalline silicon 6 is used as it is as a wiring, it is necessary to keep the resistance low.

Therefore, it is desirable to set the impurity concentration to about 1 × 10 20 cm −3 to 1 × 10 21 cm −3, which is higher than the impurity concentration of the first polycrystalline silicon 5.

[0025]

As described above, the present embodiment is characterized in that the first polycrystalline silicon 5 having a low impurity concentration is formed immediately below the second polycrystalline silicon 6 having a high impurity concentration. As shown in the figure, since the diffusion of impurities from the second polycrystalline silicon 6 proceeds via the first

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polycrystalline silicon 5 in the heat treatment after the formation of the wiring process, the diffusion distance in the semiconductor substrate 1 is small as a result. Become.

On the other hand, the diffusion of impurities from the first polycrystalline silicon 5 into the semiconductor substrate 1 can be almost ignored because the impurity concentration of the first polycrystalline silicon 5 is sufficiently lower than the impurity concentration of the source / drain region 3. The impurity diffusion position can be substantially suppressed to the position of the broken line 11a.

When the impurity concentration of the first polycrystalline silicon 5 is low, the resistance of the connection portion with the semiconductor substrate 1 may increase, but by suppressing the height of the first polycrystalline silicon 5 to about 20 nm to 50 nm, Since the impurity concentration of the first polycrystalline silicon 5 is increased by minimizing the increase in the resistance and by diffusing the impurities from the second polycrystalline silicon 6, the resistance is actually lower than that during film formation. You can almost ignore it.

To further reduce the resistance, a metal silicide layer made of at least one of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, aluminum silicide, and ruthenium silicide is attached to the upper layer of the second polycrystalline silicon 6 and integrated. It is also possible to use a so-called polycide structure.

[0026]

Embodiment 2.

As the impurities contained in the first polycrystalline silicon 5 and the second polycrystalline silicon 6, phosphorus is generally used in the N type and boron is generally used in the P type, but the first polycrystalline silicon 5 and the second polycrystalline silicon 5 are commonly used. By using at least one of arsenic, antimony, bismuth, gallium, indium, and thallium, which is an atom heavier than phosphorus or boron, for both the crystalline silicon 6 or only the second polycrystalline silicon 6, a larger effect can be obtained. can get.

That is, since heavy atoms are used as impurities, the diffusion of impurities into the semiconductor substrate 1 is delayed. In particular, when it is contained only in the first

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polycrystalline silicon 5, it is not always necessary to make the impurity concentration lower than that of the second polycrystalline silicon 6, and in some cases, even if the impurity concentration is similar to that of the second polycrystalline silicon 6. Sometimes it doesn't matter.

[0027]

Embodiment 3. 3 is a sectional view showing an integrated semiconductor device according to a third embodiment of the present invention. As shown in the figure, the first polycrystalline silicon 5 may be formed on the side surface of the connection hole 12 depending on the film thickness of the first polycrystalline silicon 5 when it is formed. Since the impurities of the second polycrystalline silicon 6 diffuse through the region of the first polycrystalline silicon 5, the same effect as that of the first embodiment can be obtained.

[0028]

Fourth Embodiment In the first embodiment described above, the first polycrystalline silicon 5 having a low impurity concentration is buried inside the connection hole 12, but as shown in FIG. 4, the second polycrystalline silicon 6 is formed immediately below the second polycrystalline silicon 6. A third polycrystal silicon 8 having an impurity concentration lower than that of the polycrystal silicon 6 is continuously formed, and the second polycrystal silicon 6 and the third polycrystal silicon 8 are simultaneously processed to form a third polycrystal silicon 8. The same effect can be obtained by using the crystalline silicon 8 as a part of the wiring. At this time as well, there is a concern that the resistance of the third polycrystalline silicon 8 may increase, but the method similar to that of the first embodiment causes almost no problem.

[0029]

Further, as in the second embodiment, as impurities to be contained only in the second and third polycrystalline silicon or the third polycrystalline silicon 8, arsenic, antimony, indium gallium, etc., which correspond to atoms heavier than phosphorus or boron, etc. By using, even greater effect can be obtained. In particular, when it is contained only in the third polycrystalline silicon 8, it is not always necessary to make the impurity concentration lower than that of the second polycrystalline silicon 6, and in some cases, it is almost the same as that of the second polycrystalline silicon 6. In some cases, the impurity concentration of does not matter. Further, in

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order to further reduce the resistance, it is possible to form a so-called polycide structure in which a metal silicide layer is bonded and integrated on the second polycrystalline silicon 6 as in the first embodiment. Needless to say.

[0030]

Embodiment 5. In the above-described first embodiment, the first polycrystalline silicon 5 having a low impurity concentration is formed inside the connection hole 12, but as shown in FIG. 5, diffusion of impurities is performed instead of the first polycrystalline silicon. The same effect can be obtained by forming a thin conductive impurity diffusion preventing layer (hereinafter referred to as a barrier layer) 9 that blocks the above. In this case, there are various kinds of materials for the barrier layer 9, but titanium nitride, silicon nitride are used as the metal-based material, and a silicon oxide film (film thickness of several Å to 20 Å) which is another insulator. Also, since it has conductivity due to the tunnel effect of electrons, it can be used as a barrier layer. This barrier layer is naturally effective when used in combination with the structures of the first to fourth embodiments.

[0031]

Sixth embodiment. In the above-described fourth embodiment, the third polycrystalline silicon 8 having a lower impurity concentration than the second polycrystalline silicon 6 is continuously formed immediately below the second polycrystalline silicon 6, but it is shown in FIG. As described above, when the second polycrystalline silicon 6 is formed, the same effect can be obtained even if the film is formed so that the concentration of impurities is continuously increased from the start to the end of the film formation. The impurity concentration at the start of film formation is about the same as that of the first polycrystalline silicon 5 shown in the first embodiment, or is in the state of no impurities, and finally the second polycrystalline silicon shown in the first embodiment is formed. It is desirable that the concentration be the same as that of crystalline silicon. Needless to say, the polycide structure according to the first embodiment and the barrier layer according to the fifth embodiment are also effective.

[0032]

Embodiment 7. In the above-described fourth embodiment, the third polycrystalline silicon 8 having a lower impurity concentration than the second polycrystalline silicon 6 is continuously

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formed immediately below the second polycrystalline silicon 6, but it is shown in FIG. As described above, the metal silicide layer 15 such as tungsten silicide formed on the upper layer of the second polycrystalline silicon is formed inside the contact hole 12 depending on the respective film thicknesses when the first and second polycrystalline silicon are formed. It may be done. Even in this case, the same effect as that of the third embodiment can be obtained, and the resistance of the connection hole 12 can be reduced. Of course, it goes without saying that the combination with the barrier layer of the fifth embodiment is also effective.

[0033]

Eighth embodiment. In the first embodiment, the second polycrystalline silicon 6 having a high impurity concentration is formed on the first polycrystalline silicon 5 having a low impurity concentration. However, as shown in FIG. Instead of 6, the metal silicide layer 15 made of at least one metal silicide of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, aluminum silicide, and ruthenium silicide may be formed. Also in this case, it is possible to use together with the barrier layer of the fifth embodiment.

[0034]
As described above, according to the first aspect of the present invention, the integrated structure for electrically connecting the electrically active region formed on the semiconductor substrate by using polycrystalline silicon containing impurities. In the semiconductor device, since the impurity diffusion preventing layer for preventing impurities from diffusing into the semiconductor substrate is formed between the polycrystalline silicon and the semiconductor substrate, it is possible to effectively prevent the impurities in the polycrystalline silicon from diffusing into the semiconductor substrate. It is possible to produce an effect that a high-performance integrated semiconductor device that can be suppressed and does not cause deterioration of device performance such as a MOS transistor can be manufactured.

[0035]
According to the second aspect of the invention, since the metal silicide compound is formed on the polycrystalline silicon, the effect of further lowering the resistance can be obtained without increasing the impurity concentration of the polycrystalline silicon.

[0036]
According to a third aspect of the present invention, the first polycrystalline silicon electrically connected to the electrically active region formed on the semiconductor substrate and the first

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polycrystalline silicon formed on the first polycrystalline silicon. Since the first polycrystalline silicon and the second polycrystalline silicon are different from each other in one or both of the types and concentrations of the impurities, the impurities of the polycrystalline silicon are different from each other. The effect of being able to manufacture a high-performance integrated semiconductor device that effectively suppresses the diffusion of the H.

[0037]
Further, according to the invention of claim 4, since the impurity concentration of the first polycrystalline silicon is lower than the impurity concentration of the second polycrystalline silicon, the impurity of the polycrystalline silicon diffuses into the semiconductor substrate. Can be effectively suppressed, and an effect can be obtained in which a high-performance integrated semiconductor device that does not cause deterioration of device performance such as a MOS transistor can be manufactured.

[0038]
According to the invention of claim 5, since the first polycrystalline silicon is polycrystalline silicon containing no impurities, the impurities do not diffuse into the semiconductor substrate, and the element performance of the MOS transistor or the like is deteriorated. It is possible to obtain an effect that a high-performance integrated semiconductor device that does not cause the above can be manufactured.

[0039]
According to the invention of claim 6, the impurities of the first polycrystalline silicon and the second polycrystalline silicon are at least one of phosphorus, boron, arsenic, antimony, bismuth, gallium, indium and thallium. Therefore, the effect of further suppressing the diffusion of impurities into the semiconductor substrate can be obtained.

[0040]
Further, according to the invention of claim 7, since the metal silicide compound is formed on the second polycrystalline silicon, the effect of further lowering the resistance can be obtained without increasing the impurity concentration of the polycrystalline silicon.

[0041]
According to the invention described in claim 8, the first polycrystalline silicon electrically connected to the electrically active region formed on the semiconductor substrate, and the first polycrystalline silicon formed on the first polycrystalline silicon. Since the metal silicide

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compound is provided, the effect of further lowering the resistance can be obtained without increasing the impurity concentration of polycrystalline silicon.

[0042]
According to the invention of claim 9, the impurities of the first polycrystalline silicon and the second polycrystalline silicon are prevented from diffusing into the semiconductor substrate between the first polycrystalline silicon and the semiconductor substrate. Since the impurity diffusion preventing layer is formed, it is possible to effectively prevent impurities of polycrystalline silicon from diffusing into the semiconductor substrate, and it is possible to manufacture a high-performance integrated semiconductor device that does not cause deterioration of device performance such as a MOS transistor. Is obtained.

[0043]
According to a tenth aspect of the invention, in a semiconductor element for electrically connecting to an electrically active region formed on a semiconductor substrate by using polycrystalline silicon containing impurities, the inclusion of polycrystalline silicon Since the concentration of the impurities to be formed is continuously changed in layers, it is possible to effectively prevent the impurities of the polycrystalline silicon from diffusing into the semiconductor substrate, and it is possible to achieve high performance without degrading the element performance such as the MOS transistor. The effect that an integrated semiconductor device can be manufactured is obtained.

[0044]
According to the eleventh aspect of the invention, since the concentration of impurities is continuously increased from the lower layer to the upper layer of polycrystalline silicon, it is effective to diffuse the impurities of polycrystalline silicon into the semiconductor substrate. Therefore, it is possible to obtain an effect that a high-performance integrated semiconductor device can be manufactured that does not cause deterioration of device performance such as a MOS transistor.

[0045]
According to the twelfth aspect of the invention, since the metal silicide compound is formed on the polycrystalline silicon, the effect of further lowering the resistance can be obtained without increasing the impurity concentration of the polycrystalline silicon.

[0046]

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Further, according to the invention of claim 13, an impurity diffusion preventing layer for preventing impurities contained in the polycrystalline silicon from diffusing into the semiconductor substrate is formed between the polycrystalline silicon and the semiconductor substrate. Diffusion of impurities of crystalline silicon into the semiconductor substrate can be effectively suppressed, and a high-performance integrated semiconductor device that does not cause deterioration of device performance such as a MOS transistor can be manufactured.

[0047]
Further, according to the invention of claim 14, the impurity contained in the polycrystalline silicon is at least one of phosphorus, boron, arsenic, antimony, bismuth, gallium, indium, and thallium. The effect of further suppressing diffusion is obtained.

[0048]
According to the fifteenth aspect of the present invention, since the impurity diffusion preventing layer is at least one of titanium nitride, silicon oxide, and silicon nitride, it is possible to effectively prevent the impurities of polycrystalline silicon from diffusing into the semiconductor substrate. It is possible to produce an effect that a high-performance integrated semiconductor device that can be suppressed and does not cause deterioration of device performance such as a MOS transistor can be manufactured.

[0049]
According to the sixteenth aspect of the present invention, the metal silicide compound is at least one of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, aluminum silicide, and ruthenium silicide. ..

[0050]
According to a seventeenth aspect of the present invention, in a semiconductor element for electrically connecting to an electrically active region formed on a semiconductor substrate by using polycrystalline silicon containing impurities, impurities of polycrystalline silicon are provided. Since arsenic is at least one of arsenic, antimony, bismuth, gallium, indium, and thallium, it is possible to effectively prevent impurities of polycrystalline silicon from diffusing into the semiconductor substrate, resulting in deterioration of device performance such as MOS transistors. The effect that a high-performance integrated semiconductor device having no high performance can be manufactured is obtained.

[0051]

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Brief description of the drawings

[0052]
1 is a sectional structural view showing an integrated semiconductor device according to a first embodiment of the present invention.

[0053]
2 is a sectional structural view showing an integrated semiconductor device according to a second embodiment of the present invention.

[0054]
3 is a sectional structural view showing an integrated semiconductor device according to a third embodiment of the present invention.

[0055]
4 is a sectional structural view showing an integrated semiconductor device according to a fourth embodiment of the present invention.

[0056]
5 is a sectional structural view showing an integrated semiconductor device according to a fifth embodiment of the present invention.

[0057]
6 is a sectional structural view showing an integrated semiconductor device according to a sixth embodiment of the present invention.

[0058]
7 is a sectional structural view showing an integrated semiconductor device according to a seventh embodiment of the present invention.

[0059]
8 is a sectional structural view showing an integrated semiconductor device according to an eighth embodiment of the present invention.

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[0060]
9 is a sectional structural view showing a conventional integrated semiconductor device.

[0061]
10 is a schematic sectional view for explaining a conventional integrated semiconductor device.

[0062]
Explanation of symbols

[0063]
DESCRIPTION OF SYMBOLS 1 semiconductor substrate, 2 element isolation, 3 source / drain regions, 4 gate electrodes, 5 first polycrystalline silicon, 6 second polycrystalline silicon, 7 sidewalls, 8 third polycrystalline silicon, 9 impurity diffusion prevention (Barrier) layer, 10 polycrystalline silicon having a concentration gradient of impurities, 11 impurity regions diffused from polycrystalline silicon, 12 contact holes, 13 polycrystalline silicon, 14 interlayer insulating film, 15 metal silicide layer

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CLAIMS JPH1027847

1.
In an integrated semiconductor device for electrically connecting an electrically active region formed on a semiconductor substrate by using polycrystalline silicon containing an impurity, the impurity is provided between the polycrystalline silicon and the semiconductor substrate. Forming an impurity diffusion preventing layer for preventing diffusion into the semiconductor substrate.

2.
2. The integrated semiconductor device according to claim 1, wherein a metal silicide compound is formed on polycrystalline silicon.

3.
A first polycrystalline silicon electrically connected to an electrically active region formed on a semiconductor substrate, and a second polycrystalline silicon formed on the first polycrystalline silicon, An integrated semiconductor device characterized in that the first polycrystalline silicon and the second polycrystalline silicon are different from each other in one or both of the types and concentrations of impurities.

4.
4. The integrated semiconductor device according to claim 3, wherein the impurity concentration of the first polycrystalline silicon is lower than the impurity concentration of the second polycrystalline silicon.

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5.

4. The integrated semiconductor device according to claim 3, wherein the first polycrystalline silicon is polycrystalline silicon containing no impurities.

6.

6. The impurity of the first polycrystalline silicon and the second polycrystalline silicon is at least one of phosphorus, boron, arsenic, antimony, bismuth, gallium, indium, and thallium. 2. The integrated semiconductor device according to item 1.

7.

7. The integrated semiconductor device according to claim 3, wherein a metal silicide compound is formed on the second polycrystalline silicon.

8.

A first polycrystalline silicon electrically connected to an electrically active region formed on a semiconductor substrate; and a metal silicide compound formed on the first polycrystalline silicon. Integrated semiconductor device.

9.

An impurity diffusion preventing layer for preventing impurities of the first polycrystalline silicon and the second polycrystalline silicon from diffusing into the semiconductor substrate is formed between the first polycrystalline silicon and the semiconductor substrate. The integrated semiconductor device according to any one of claims 3 to 8.

10.

In a semiconductor element for electrically connecting to an electrically active region formed on a semiconductor substrate using polycrystalline silicon containing impurities, the concentration of impurities contained in the polycrystalline silicon is continuously layered. An integrated semiconductor device characterized by being formed by being changed.

11.

11. The integrated semiconductor device according to claim 10, wherein the concentration of impurities continuously increases from the lower layer to the upper layer of polycrystalline

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silicon.

12.

12. The integrated semiconductor device according to claim 10, wherein a metal silicide compound is formed on polycrystalline silicon.

13.

13. An impurity diffusion preventing layer for preventing impurities contained in the polycrystalline silicon from diffusing into the semiconductor substrate, between the polycrystalline silicon and the semiconductor substrate. The integrated semiconductor device according to claim 1.

14.

14. The integrated device according to claim 10, wherein the impurity contained in the polycrystalline silicon is at least one of phosphorus, boron, arsenic, antimony, bismuth, gallium, indium and thallium. Semiconductor device.

15.

14. The integrated semiconductor device according to claim 1, wherein the impurity diffusion preventing layer is at least one of titanium nitride, silicon oxide, and silicon nitride.

16.

13. The metal silicide compound is at least one of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, aluminum silicide, and ruthenium silicide, according to claim 2, 7. Integrated semiconductor device.

17.

In a semiconductor element for electrically connecting to an electrically active region formed on a semiconductor substrate by using polycrystalline silicon containing an impurity, the impurity of the polycrystalline silicon is arsenic, antimony, bismuth, gallium, An integrated semiconductor device comprising at least one of indium and thallium.

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(71) Applicant: **SUMITOMO ELECTRIC INDUSTRIES, LTD.**
5-33, Kitahama 4-chome, Chuo-ku
Osaka-shi, Osaka 541(JP)

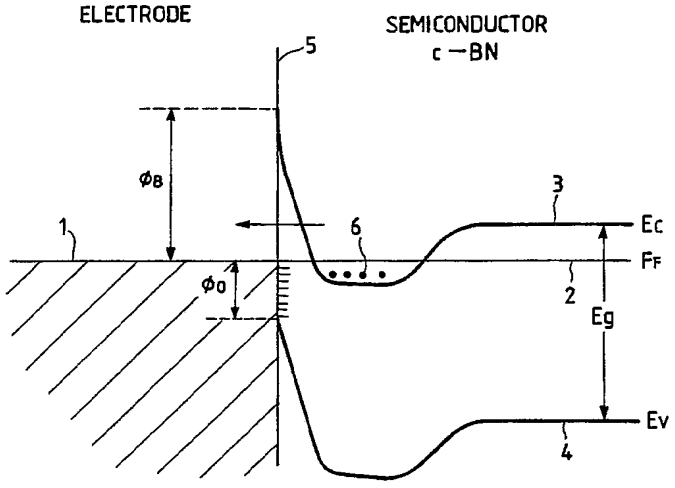
(72) Inventor: **Tomikawa, Tadashi, c/o Itami Works of Sumitomo**
Elec. Ind.,Ltd, 1-1, Koyakita 1-chome
Itami-shi, Hyogo(JP)
Inventor: **Kimoto, Tunenobu, c/o Itami Works of Sumitomo**
Elec. Ind.,Ltd, 1-1, Koyakita 1-chome
Itami-shi, Hyogo(JP)
Inventor: **Fujita, Nobuhiko, c/o Itami Works of Sumitomo**
Elec. Ind.,Ltd, 1-1, Koyakita 1-chome
Itami-shi, Hyogo(JP)

(74) Representative: **Patentanwälte Grünecker, Kinkeldey, Stockmair & Partner**
Maximilianstrasse 58
W-8000 München 22(DE)

(54) Ohmic contact electrodes for n-type semiconductor cubic boron nitride.

(57) An ohmic contact electrode formed on an n-type semiconductor cubic boron nitride by using a IVa metal; an alloy with a IVa metal; a metal with Si or S; an alloy with Si or S; a metal with B, Al, Ga, or In; an alloy with B, Al, Ga, or In; a Va metal; or an alloy with a Va metal.

FIG. 1



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BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to an ohmic contact electrode for an n-type semiconductor cubic boron nitride.

Description of Related Art

Attention has been given to a semiconductor cubic boron nitride as a new material for semiconductor devices such as diodes, transistors, sensors, and so on. Although an insulating cubic boron nitride is known broadly, that which is discussed here is a semiconductor cubic boron nitride having low resistivity.

A cubic boron nitride has a wide forbidden band width (7.0 eV) and a high heat-proof temperature (1300 ° C), and is chemically stable. Consequently, a semiconductor cubic boron nitride has been strongly expected to be an excellent material for environment-proof power devices, and blue light emission elements.

A cubic boron nitride does not naturally exist but can be formed through high-pressure synthesis. Further, recently, the formation of thin film through vapor phase synthesis has been reported.

A p-type cubic boron nitride can be obtained by doping beryllium (Be).

An n-type cubic boron nitride, on the other hand, can be obtained by doping sulfur (S) or silicon (Si). At present, a pn-junction diode is produced for trial by using a high-pressure synthetic method in such a manner that an n-type cubic boron nitride is continuously grown with a p-type cubic boron nitride as a seed crystal. The pn-junction diode which is produced has a diode characteristic under 650 ° C. Further, it has been reported that a pn-junction diode emits, by injection of minority carries, light from ultraviolet to blue centering around 340 nm.

A contact between a metal and a semiconductor is either a Schottky contact or an ohmic contact. The Schottky contact has a rectification property so that a current does not flow in a reverse direction. In the case of producing semiconductor devices, it is very important to form electrodes which can be formed by ohmic contact. The term "ohmic contact electrode" means an electrode in which the characteristic of a current flowing through the electrode and the characteristic of a voltage across the electrode are symmetrical forward and backward in accordance with the Ohm's law. Further, it is preferable that the contact resistance is reduced as much as possible. The term "contact resistance" is defined as a voltage to be applied so as to make a unit current flow through a unit contact surface. The unit of the contact resistance is $\Omega \cdot cm^2$.

There has not yet been found a superior electrode for an n-type cubic boron nitride. Although silver (Ag), silver paste, or the like is used as an electrode for an n-type cubic boron nitride ((1) R.H.Wentorf, Jr.: J. of Chem. Phys. Vol. 36 (1962) 1990; (2) 0. Mishima, etc.: Science Vol. 238 (1987) 181), there has been no report that an ohmic contact could be obtained.

The technique for forming ohmic contact is necessary and indispensable to produce semiconductor devices. Further, if an ohmic contact is obtained, it is desirable that the contact resistance in the ohmic contact portion be reduced as much as possible. The contact resistance of general electron devices is 10^{-2} $\Omega \cdot cm^2$ or less, and a smaller contact resistance of 10^{-4} $\Omega \cdot cm^2$ or less is required in high-speed and high-frequency devices.

If a formed contact is not an ohmic one but a Schottky one, carriers cannot be effectively injected into a produced device because of the existence of a Schottky barrier in the contact electrode portion even when the current is to be made to flow in the device. This results in low efficiency of carrier injection. Further, the voltage drop across the contact electrode portion is remarkably large because the resistance is larger at the contact electrode portion. Therefore, the effective voltage applied to the device ends up being small. As a result, the particularly desireable characteristics discussed above for the device cannot be obtained. Further, the generation of heat in the contact electrode portion is a large problem.

Accordingly, the formation of an ohmic contact electrode is necessary and indispensable in order to make it possible to utilize a semiconductor cubic boron nitride as a material for semiconductor devices.

An object of the present invention is therefore to form an ohmic contact electrode on an n-type semiconductor cubic boron nitride.

SUMMARY OF THE INVENTION

The ohmic contact electrode for an n-type semiconductor cubic boron nitride according to the present

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invention is an electrode formed on an n-type semiconductor cubic boron nitride so that an ohmic contact electrode can be obtained by using:

(1) a IVa-family metal which includes titanium (Ti), zirconium (Zr), and hafnium (Hf) or an alloy containing a IVa-family metal;

(2) a metal or alloy containing silicon (Si) or sulfur (S);

(3) a metal or alloy containing at least one of boron (B), aluminum (Al), gallium (Ga), and indium (In); or

(4) a Va-family metal which includes vanadium (V), niobium (Nb), and tantalum (Ta) or an alloy containing a Va-family metal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a band diagram in the case where a high concentration doped layer is formed in the vicinity of a metal/semiconductor interface when one of the following materials is applied to an n-type semiconductor cubic boron nitride:

(1) IVa-family metal or an alloy containing a IVa-family metal;

(2) a metal or alloy containing Si or S;

(3) a metal or alloy containing at least one of B, Al, Ga and In; or

(4) a Va-family metal or an alloy containing a Va-family metal.

Fig. 2 is a band diagram in the case where high-density localized states are formed in the vicinity of a metal/semiconductor interface when one of the following materials is applied to an n-type semiconductor cubic boron nitride:

(1) a IVa-family metal or an alloy containing a IVa-family metal;

(2) a metal or alloy containing at least one of B, Al, Ga and In; or

(3) a Va-family metal or an alloy containing a Va-family metal.

Fig. 3 is a plan showing an electrode pattern which was used in measuring the contact resistance between the semiconductor cubic boron nitride and the electrodes. In the drawing, hatched portions represent the electrodes:

1 Fermi-level of electrode;

2 Fermi-level of semiconductor;

3 lower end of conduction band of semiconductor;

4 upper end of valence band of semiconductor;

5 electrode/semiconductor interface.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to the present invention, an ohmic contact electrode can be obtained by coating an n-type cubic boron nitride with the following:

(1) A IVa-family metal (Ti, Zr, or Hf) or an alloy containing a IVa-family metal;

(2) A metal or alloy containing Si or S which is contained in a matrix material desirably selected from Cr, W, Mn, Co, Ni, Pt, Ag, Zn, WC, MnZn, Ni_2B, PtPd, AgAl, and so on;

(3) A metal or alloy containing at least one of B, Al, Ga and In; or

(4) A Va-family metal (V, Nb, or Ta) or an alloy containing a Va-family metal.

This technique has been found through repeated experiments. Although the reason is unclear why an ohmic contact is obtained by using the above mentioned metals or alloys, some possibilities can be considered.

IVa-family elements

When a IVa-family metal such as Ti, Zr, Hf, TiC, ZrNi, or the like, or an alloy containing a IVa-family metal is formed as an electrode on an n-type cubic boron nitride, the electrode constituent element/elements as well as boron and nitrogen are activated by the heating of a substrate at the time of electrode formation, radiation heat at the time of electrode evaporation, annealing after the electrode formation, etc., so that mutual diffusion is generated in an interface between the electrode and the semiconductor.

The IVa-family elements (Ti, Zr, and Hf), on the other hand, are also apt to react with boron and nitrogen so as to easily form a boride such as TiB_2, ZrB_2, HfB_2, etc. and a nitride such as TiN, ZrN, HfN, etc. This phenomenon is well known. Therefore, the mutual diffusion in the electrode constituent elements as well as boron and nitrogen is further accelerated. Moreover, a metal compound layer is formed in the

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electrode/semiconductor interface in which the mutual diffusion is generated, and the substantial electrode/semiconductor interface is shifted into a semiconductor layer so as to form a clean interface.

Further, there is a possibility that the IVa-family elements (Ti, Zr, and Hf) diffused into the cubic boron nitride become donors for the cubic boron nitride. There is a further possibility that holes or defects formed at places where boron and nitrogen have been removed by the diffusion become donors. As a result, an n-layer (n^+ layer) doped with high concentration is formed in the region where the mutual diffusion has been generated. Although the cubic boron nitride is of the n-type originally, it becomes of the n-type having a doping concentration considerably higher than the original mean doping concentration. The thickness of the barrier layer is reduced by the high-concentration doping so that the contact becomes ohmic by a tunneling current.

Si or S

Similarly, when a metal or alloy containing Si or S is formed as an electrode on an n-type cubic boron nitride, the Si or S contained in the electrode is activated by heating of a substrate at the time of electrode formation, radiation heat at the time of electrode evaporation, annealing after the electrode formation, etc., so that the Si or S gradually diffuses into the adjacent cubic boron nitride.

The Si or S acts as an effective donor in the cubic boron nitride. This phenomenon is well known. Therefore, in the region where Si or S has been diffused, an n-layer (n^+-layer) doped with high concentration is formed.

B, Al, Ga, or In

Similarly when a metal or alloy consisting of at least one of B, Al, Ga and In is formed as an electrode on an n-type cubic boron nitride, an electrode constituent element/elements as well as boron and nitrogen are activated by heating of a substrate at the time of electrode formation, radiation heat at the time of electrode evaporation, annealing after the electrode formation, etc., so that mutual diffusion is generated in an interface between the electrode and the semiconductor.

Such elements as Al, Ga, In, etc. easily react with nitrogen so as to easily form nitride such as AlN, GaN, InN, etc. This phenomenon is well known. Also in the case where an electrode includes B, of course, nitrogen diffuses into B. Further, Al easily forms boride such as AlB_2, etc. This is well known. Therefore, the mutual diffusion in the electrode constituent elements as well as boron and nitrogen is further accelerated. Moreover, a metal compound layer is formed in the electrode/semiconductor interface in which the mutual diffusion is generated, and the substantial electrode/semiconductor interface is shifted into a semiconductor layer so as to form a clean interface.

Va-family metal

Similarly, when a Va-family metal such as V, Nb, Ta, VC, Nb_3Al, or the like, or an alloy containing a Va-family metal is formed as an electrode on an n-type cubic boron nitride, an electrode constituent element/elements as well as boron and nitrogen are activated by heating of a substrate at the time of electrode formation, radiation heat at the time of electrode evaporation, annealing after the electrode formation, etc., so that mutual diffusion is generated in an interface between the electrode and the semiconductor.

The Va-family elements (V, Nb, and Ta) are also apt to react with boron and nitrogen so as to easily form a boride such as VB_2, NbB_2, TaB_2, etc. and a nitride such as VN, NbN, TaN, etc. This phenomenon is well known. Therefore, the mutual diffusion in the electrode constituent elements as well as B and N is further accelerated. Moreover, a metal compound layer is formed in the electrode/semiconductor interface in which the mutual diffusion is generated, and the substantial electrode/semiconductor interface is shifted into a semiconductor layer so as to form a clean interface.

Presently for all four types of coatings, there is the possibility that holes or defects formed at places where boron or nitrogen have been removed by the diffusion thereof into the electrode act as donors. In fact, in the case of GaN which is a III-V family compound and which is of the same kind as boron nitride, extreme n-type semiconductor characteristics are shown without any doping. This is, perhaps, because holes at which nitrogen has been removed act as donors.

As a result of mutual diffusion, an n-layer (n^+-layer) in which high concentration donor is formed in the region in the vicinity of the interface between the electrode and the cubic boron nitride. Although the cubic boron nitride is of the n-type originally, it becomes of the n-type having a donor concentration considerably

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higher than the original mean donor concentration. The thickness of the barrier layer is reduced by the high-concentration donor so that the contact becomes ohmic by a tunneling current.

In an ideal case, whether a metal/semiconductor contact becomes an ohmic one or a Schottky one is determined depending on the work function (ϕ_m) of the metal and the electron affinity (X_s) of the semiconductor. Here, the work function of a metal is energy required for drawing out electrons in Fermi-level to an infinite distance. The electron affinity of a semiconductor is energy required for drawing out electrons existing in the bottom of a conduction band to an infinite distance. In the case of an n-type semiconductor, the height (ϕ_B) of a barrier in a metal/semiconductor contact is expressed by the following equation.

$$\phi_B = \phi_m - X_s \quad (1)$$

The contact becomes therefore:

an ohmic one when $\phi_B < 0$; and

a Schottky one when $\phi_B > 0$.

Since ϕ_B represents the height of the barrier, electrons are checked by the barrier if the value of ϕ_B is positive so that the contact becomes a Schottky one, while if the value of ϕ_B is negative, there is no barrier so that the contact becomes an ohmic one. It seems, from the above equation, that an ohmic contact can be obtained if a metal having a low work function is selected to be an electrode.

In an actual metal/semiconductor contact, however, defects exist in a metal/semiconductor contact interface so as to form localized states (also called interface states, ϕ_0: interface level) in the vicinity of the center in a band gap. If a large number of defects exist, the Fermi-level of the semiconductor is pinned up to the level of ϕ_0. As a result, if the band gap of the semiconductor is represented by E_g, ϕ_B is expressed by the following equation, and hardly depends on the kind of metal at all.

$$\phi_B = E_g - \phi_0 \quad (2)$$

The ϕ is measured from the upper end of the valence band. This is because electrons from the metal can freely flow into the localized states to occupy the states so that the upper end of the localized states coincides with the Fermi plane of the metal and the Fermi level of the semiconductor coincides with the Fermi plane of the metal.

Since it is the case, of course, that $\phi_B > 0$, the metal/semiconductor contact becomes a Schottky one. This phenomenon is known as the pinning effect, and is remarkable particularly in the case of III-V family compound semiconductors. Further, ϕ_0 is about 1/3 - 1/2 times as large as E_g.

Also in the case of a cubic boron nitride, various kinds of interface defects may exist because it is not a single element material. Further, it is thought that a large number of interface defects exist which thereby cause the pinning effect because a cubic boron nitride crystal in the present circumstances is imperfect and has a large number of defects.

Fig. 1 is a band diagram of a Schottky contact between a metal and an n-type semiconductor. A Fermi-level 2 of the semiconductor is continued from a Fermi-level 1 of the outside metal. A conduction band and a valence band exist in the semiconductor. The reference numerals 3 and 4 designate the lower end of the conduction band and the upper end of the balance band respectively. Since the semiconductor is of the n-type, the lower end 3 of the conduction band is approximate to the Fermi-level 2. The Fermi-level is pinned up to the interface level ϕ_0 at a boundary 5, so that a barrier having a height of ϕ_B is formed. The band is extremely bent upward in the vicinity of the boundary 5 because the donor density is high at the boundary. Although electrons accumulate in a downward curved portion 6 in the conduction band, the electrons may fly into the metal because of the tunneling effect. Since all the donors at the metal/semiconductor boundary are donated electrons and have positive charges of e. The positive charges are substantially uniformly distributed in the vicinity of the boundary and therefore this portion becomes a depletion layer in which no electron exists. The thickness of this portion can be calculated as follows. The following equation is established by integrating the Gaussian expression relating to an electric field and electric charges.

$$d = [2 \cdot \epsilon_S \cdot \epsilon_0 \cdot (\phi_B - V)/(e \cdot N_d)]^{1/2} \quad (3)$$

d: depletion layer width

ϵ_S: specific inductive capacity of the semiconductor

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ϵ_0: dielectric constant in the vacuum
V: applied voltage
e: elementary electric charge
N_d: donor density in the semiconductor

Although ϕ_B is a potential having an energy dimension as before, ϕ_B is treated below as a value of voltage obtained by dividing the potential by the elementary electric charge e.

As seen from the equation (3), the depletion layer width d becomes smaller as the donor density in the semiconductor becomes higher. Since electrons easily pass through the thin depletion layer, the contact comes to have low resistance. This phenomenon will be described in more detail.

Being a tunneling current, a current I per unit area can be expressed as follows.

$$I = AT^2 \exp \{-2\int_0^d (8\pi^2 m_e U/h^2)^{1/2} dx\} \qquad (4)$$

in which U represents the potential of a conduction electron measured from the bottom of the conduction band.

U is expressed as follows as a function of x by integrating the Gaussian expression.

$$U = e(\phi_B - V)\{1-(x/d)\}^2 \qquad (5)$$

$$A = 4\pi em_e k^2/h^3 \qquad (6)$$

in which, me represents the effective mass of electrons in the semiconductor, h represents the Planck's constant, k represents the Boltzmann constant, and T represents the absolute temperature. In the case of free electrons, A is 120 A/cm^2K^2. If integration is made with respect to x,the following expression is obtained.

$$I = AT^2 \exp \{ - (\phi_B - V)/V_{00}\} \qquad (7)$$

in which

$$V_{00} = hNd^{1/2} / 4\pi (\epsilon_0 \epsilon_S m_e)^{1/2} \qquad (8)$$

Assuming that $Nd = 10^{21} cm^{-3}$, me represents the free electron mass, and $\epsilon_S = 1$, $\epsilon_0 = 1$, and $T = 300^\circ K$, then V_{00} is 0.56 V. Although the definition of ϕ_B has been described above, it is considered that if an n-type impurity is doped with high concentration, the ϕ_B itself decreases. This is because, as the localized states increase, ϕ_0 increases. E_g is 7 eV, while ϕ_B decreases to about 6-3 v. It is assumed that the concentration of doping is extremely large in the vicinity of the boundary. If $V_{00} = 0.5$ V, this contact can be regarded substantially as an ohmic one from the equation (6). This is the case provided that the direction of the voltage from the semiconductor side toward the metal electrode is defined to be positive.

Resistance (R_c) is obtained by partially differentiating the current with respect to the voltage on the assumption that $V = 0$. The R_C at this time is expressed by the following equation.

$$R_C = (V_{00}/AT^2)\exp(\phi_B/V_{00}) \qquad (9)$$

Assuming that $Nd = 10^{21} cm^{-3}$, the mass of free electrons is represented by m_e, $\epsilon_0 = 1$, and $T = 300^\circ K$, then $V_{00} = 0.56$ V. If the coefficient before exp. is included in exp., the following equation is obtained.

$$R_C = \exp \{(\phi_B/0.56) - 16.77) \qquad (10)$$

If $\phi_B = 6$ V, R_C becomes $10^{-3}\ \Omega \cdot cm^2$, while if $\phi_B = 7$ V, Rc becomes $10^{-2}\ \Omega \cdot cm^2$.

Assuming that $Nd = 10^{20} cm^{-3}$, then V00 becomes 0.18 V and the following equation is obtained.

$$R_C = \exp \{(\phi_B/0.18) - 17.91\} \qquad (11)$$

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If $\phi_B = 3V$, R_c is about 10^{-1} $\Omega \cdot cm^2$, while if $\phi_B = 2.5V$, Rc is about 10^{-2} $\Omega \cdot cm^2$.

Thus, if an n-type impurity is doped with high concentration, the depletion layer thickness d decreases. Further, there is such an effect that the localized state of the surface is increased by high concentration doping so that ϕ_0 increases and ϕ_B decreases. Although description has been made as to the case where ϕ_B is about 1/2 - 2/3 times as large as the band gap (7eV), it is considered that the ϕ_B may be further reduced.

Thus, the higher the donor density is made by high concentration doping, the more the thickness of the depletion layer decreases and the more ϕ_B decreases so as to make a tunneling current flow easily. Thus, it can be expected that the contact becomes ohmic. But the fact is not yet clearly understood. It may be that the localized state is transmitted by the tunnelling of electrons. Although such an effect can be expected by doping an impurity with high concentration, if the density of the impurity becomes so high, the result is rather undesirable because the resistance of the electrode increases. It is therefore believed that there exists a suitable range of the concentration.

Further, the following possibility is considered. That is, a boride layer and a nitride layer have been formed in a metal/semiconductor interface so that a large number of defects have been brought into the interface and the vicinity of the interface. If the localized states 7 of high density exist in the vicinity of the boundary 5 as shown in Fig. 2, electrons may move between the metal and the semiconductor through the states so that a current may flow between them. Since the higher the localized state density is, the more easily electrons move, which makes the contact resistance become low. Moreover, since the movement is performed bi-directionally, the contact becomes ohmic.

Other than those mechanisms described above, various mechanisms for obtaining an ohmic contact can be considered. They cannot be specified at the present time. An ohmic contact, however, can be obtained on an n-type cubic boron by forming an electrode according to the present invention.

Examples

The ohmic contact electrode according to the present invention will be described more in detail with reference to examples.

In order to inspect the kind of electrode material to which the electrode structure of the present invention was suitable, electrodes were produced from various materials and the ohmic property and contact resistance were evaluated.

Example 1

Ti, TiAl, TiB_2, TiC, TiCr, TiFe, TiN, TiNb, TiNi, TiSi, Zr, ZrAl, ZrB_2, ZrC, ZrN, ZrNb, ZrNi, ZrS_2, $ZrSi_2$, Hf, HfB_2, HfC, HfN, HfS_2, and $HfSi_2$ were formed, as the electrodes, according to the present invention, on a high-pressure synthesized Si-doped n-type cubic boron nitride, and the ohmic property and contact resistance of the thus formed electrodes were evaluated. The electrodes were formed at a substrate temperature of 400° C by vacuum evaporation or sputtering depending on the material.

At that time, an electrode pattern shown in Fig. 3 was formed on the cubic boron nitride by using a metal mask. The thickness of each of four electrodes was about 0.2 - 0.3 μm. The length was 0.8 mm and the width was 0.1 mm. They were arranged in parallel to each other at intervals of 0.1 mm, 0.2 mm, and 0.3 mm.

The current-voltage characteristic between arbitrary electrodes was measured in a voltage range of from -10V to +10V to thereby judge the ohmic property of the electrodes. With respect to the electrodes of which the ohmic characteristic has been measured, the contact resistance was measured by using a transmission line model on the basis of the resistance and electrode distance between two electrodes of the electrode pattern of Fig. 3.

Table 1 shows the summary of the results of applying one of the above metals to form an ohmic contact electrode.

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Table 1

Electrodes Containing IVa-Family Metal, Current-Voltage Characteristic, and Contact Resistance

Electrode (atom ratio)	Method of Formation	Current-voltage Characteristics	Contact Resistance ($\Omega \cdot cm^2$)
Ti	Vacuum evap.	Ohmic	2×10^{-1}
TiAl	Sputtering	Ohmic	3×10^{-1}
TiB_2	Sputtering	Ohmic	8×10^{-2}
TiC	Sputtering	Ohmic	1×10^{-1}
TiCr(80:20)	Sputtering	Ohmic	5×10^{-1}
TiFe	Sputtering	Ohmic	4×10^{-1}
TiN	Sputtering	Ohmic	7×10^{-2}
TiNb(66:34)	Sputtering	Ohmic	3×10^{-1}
TiNi(55:45)	Sputtering	Ohmic	7×10^{-1}
$TiSi_2$	Sputtering	Ohmic	4×10^{-2}
Zr	Vacuum evap.	Ohmic	1×10^{-1}
ZrAl(75:25)	Sputtering	Ohmic	3×10^{-1}
ZrB_2	Sputtering	Ohmic	7×10^{-2}
ZrC	Sputtering	Ohmic	9×10^{-2}
ZrN	Sputtering	Ohmic	6×10^{-2}
ZrNb(95:5)	Sputtering	Ohmic	5×10^{-1}
ZrNi	Sputtering	Ohmic	6×10^{-1}
ZrS_2	Sputtering	Ohmic	4×10^{-2}
$ZrSi_2$	Sputtering	Ohmic	5×10^{-2}
Hf	Vacuum evap.	Ohmic	8×10^{-2}
HfB_2	Sputtering	Ohmic	6×10^{-2}
HfC	Sputtering	Ohmic	2×10^{-1}
HfN	Sputtering	Ohmic	9×10^{-2}
HfS_2	Sputtering	Ohmic	6×10^{-2}
$HfSi_2$	Sputtering	Ohmic	4×10^{-2}

As seen in Table 1, IVa-family metals such as Ti, Zr, Hf, TiC, ZrNi, etc. and alloys containing a IVa-family metal were formed, as the electrodes, on an n-type cubic boron nitride, so that the ohmic characteristic could be obtained although the contact resistance was a value within a range from 10^{-2} to 10-1 $\Omega \cdot cm^2$.

Example 2

Si or S was added to Cr, W, Mn, Co, Ni, Pt, Ag, Zn, WC, MnZn, Ni_2B, PtPd, or AgAl. As the cubic boron nitride, a high-pressure composition was used. The electrodes were formed at a substrate temperature of 400 °C, and by the use of vacuum evaporation or sputtering depending on the material. As the

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electrode materials, used were those in which each of the Si-concentration and S-concentration was 0.1%-0.5%.

At that time, an electrode pattern shown in Fig. 3 was formed on the cubic boron nitride by using a metal mask. The thickness of each of four electrodes was about 0.5-0.3 μm. The length was 0.8 mm and the width was 0.1 mm. They were arranged in parallel to each other at intervals of 0.1 mm, 0.2 mm, and 0.3 mm. The current-voltage characteristic between arbitrary electrodes was measured in a voltage range of from -10V to +10V to thereby judge the ohmic property of the electrodes. With respect to the electrodes the ohmic characteristic of which has been measured, the contact resistance was measured by using a transmission line model on the basis of the resistance and electrode distance between two electrodes of the electrode pattern of Fig. 3.

The results of the above examples in which either Si or S were added with the above metals to form electrodes are summarized in Tables 2 and 3.

Table 2

Electrodes Containing Si, Current-Voltage Characteristic, and Contact Resistance

Electrode	Method of Formation	Current-Voltage Characteristic	Contact Resistance ($\Omega \cdot cm^2$)
CrSi	Vacuum evap.	Ohmic	1×10^{-1}
WSi	Vacuum evap.	Ohmic	4×10^{-2}
MnSi	Vacuum evap.	Ohmic	2×10^{-1}
CoSi	Vacuum evap.	Ohmic	6×10^{-2}
NiSi	Vacuum evap.	Ohmic	6×10^{-2}
PtSi	Vacuum evap.	Ohmic	7×10^{-2}
AgSi	Vacuum evap.	Ohmic	8×10^{-2}
ZnSi	Vacuum evap.	Ohmic	5×10^{-2}
WCSi	Sputtering	Ohmic	2×10^{-2}
MnZnSi	Sputtering	Ohmic	9×10^{-2}
Ni_2BSi	Sputtering	Ohmic	8×10^{-2}
PtPdSi	Sputtering	Ohmic	2×10^{-1}
AgAℓSi	Sputtering	Ohmic	9×10^{-2}

(Here, MSi does not mean that the element ratio of a metal or an alloy M to Si is 1:1 but means that a certain quantity of Si is contained in the metal or alloy M. That is, MSi does not mean a molecular formula with respect to Si.)

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Table 3

Electrodes Containing S, Current-Voltage Characteristic, and Contact Resistance

Electrode	Method of Formation	Current-Voltage Characteristic	Contact Resistance ($\Omega \cdot cm^2$)
CrS	Vacuum evap.	Ohmic	2×10^{-1}
WS	Vacuum evap.	Ohmic	2×10^{-2}
MnS	Vacuum evap.	Ohmic	9×10^{-2}
CoS	Vacuum evap.	Ohmic	7×10^{-2}
NiS	Vacuum evap.	Ohmic	1×10^{-1}
PtS	Vacuum evap.	Ohmic	8×10^{-2}
AgS	Vacuum evap.	Ohmic	6×10^{-2}
ZnS	Vacuum evap.	Ohmic	8×10^{-2}
WCS	Sputtering	Ohmic	2×10^{-2}
MnZnS	Sputtering	Ohmic	7×10^{-2}
Ni_2BS	Sputtering	Ohmic	6×10^{-2}
PtPdS	Sputtering	Ohmic	1×10^{-1}
AgAℓS	Sputtering	Ohmic	8×10^{-1}

(Here, MS does not mean that the atom ratio of a metal or an alloy M to S is 1:1 but means that a certain quantity of S is contained in the metal or alloy M. That is, MS does not mean a molecular formula with respect to S.)

Inspection was made on various metal materials and metal compounds, and as seen in Tables 2 and 3, the ohmic characteristic could be obtained with respect to all the material, although the contact resistance was a value within a range from 10^{-2} to 10^{-1} $\Omega \cdot cm^2$.

This fact makes reasonable the aforementioned estimation of the electron tunnel effect due to high concentration donor generation at the boundary between a metal and a semiconductor.

Example 3

When a metal or a metal compound containing Si or S is used as a material for the electrode, inspection was made to obtain a proper concentration of Si or S.

The electrodes were made from PtSi or PtS (this does not mean that the atomic ratio is 1:1 but means that a certain quantity of Si or S is contained in Pt) under the condition that the respective concentrations of Si and S were changed variously. The results of evaluation of the ohmic characteristic and contact resistance are shown in Tables 4 and 5.

As the cubic boron nitride, a high-pressure composition was used. The electrodes were formed through a vacuum evaporation method without heating the substrates and subjected to annealing in an atmosphere of N_2 + H_2 (H_2:10%) at 800 °C for 10 minutes.

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Table 4

Si Concentration, Current-Voltage Characteristic, and Contact Resistance

Si Concentration (PtSi)	Current-Voltage Characteristic	Contact Resistance ($\Omega \cdot cm^2$)
0.01%	Ohmic	2×10^{0}
0.1%	Ohmic	1×10^{-1}
1.5%	Ohmic	6×10^{-2}
1.0%	Ohmic	5×10^{-2}
5.0%	Ohmic	2×10^{-1}
10.0%	Ohmic	3×10^{-1}

Table 5

S Concentration, Current-Voltage Characteristic, and Contact Resistance

S Concentration (PtS)	Current-Voltage Characteristic	Contact Resistance ($\Omega \cdot cm^2$)
0.01%	Ohmic	1×10^{0}
0.1%	Ohmic	9×10^{-2}
0.5%	Ohmic	4×10^{-2}
1.0%	Ohmic	4×10^{-2}
5.0%	Ohmic	1×10^{-1}
10.0%	Ohmic	2×10^{-1}

From the Tables 4 and 5, it can be seen that the ohmic contact could be obtained over all the range of Si- or S-concentration, and that although the contact resistance decreased as the Si-or S-concentration increases, it reached the minimum at several % and then increased thereafter. Further, it is not desirable to make the Si- or S-concentration excessively high, because the resistance of the electrode per se becomes high. In practice, it suffices to select the Si- or S-concentration to be about 1 % by weight.

Example 4

B, AlB_2, CrB_2, SiB_4, WB, Al, AlCu, AlSi, Ga, GaIn, GaSn, GaZn, In, InMg, and InSn were formed, as the electrodes, according to the present invention, on a high-pressure synthesized Si-doped n-type cubic boron nitride, and the ohmic property of the thus formed electrodes was evaluated. In the case of low melting point metals and alloys such as Ga, In, GaIn, etc., after electrode materials were set at two positions on a cubic boron nitride, electrodes were formed through alloying treatment in an N_2 atmosphere at 400 ° C for five minutes. The current-voltage characteristic between those electrodes was measured in a voltage range

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of from -10V to +10V to thereby judge the ohmic property of the electrodes.

The other electrodes were formed by using a vacuum evaporation method or a sputtering method depending on the materials under the condition that the substrate temperature was kept at room temperature. After formation of the electrodes, annealing was made in an N_2 atmosphere at 400°C for 20 minutes. Further, in formation of the electrodes, an electrode pattern shown in Fig. 3 was formed on the cubic boron nitride by using a metal mask. The thickness of each of four electrodes was about 0.2-0.3 μm. The length was 0.8 mm and the width was 0.1 mm. They were arranged in parallel to each other at intervals of 0.1 mm, 0.2 mm, and 0.3 mm. With respect to the electrodes the ohmic characteristic of which has been measured, the contact resistance was measured by using a transmission line model on the basis of the resistance and electrode distance between two electrodes of the electrode pattern of Fig. 3.

Table 6 shows the summary of the results of the above examples.

Table 6

Electrodes Containing B, Al, Ga, or In; Current-Voltage Characteristic and Contact Resistance

Electrode (atom ratio)	Method of Formation	Current-Voltage Characteristic	Contact Resistance ($\Omega \cdot cm^2$)
B	Vacuum evap.	Ohmic	4×10^{-1}
AlB_2	Sputtering	Ohmic	9×10^{-2}
CrB_2	Sputtering	Ohmic	4×10^{-1}
SiB_4	Sputtering	Ohmic	5×10^{-2}
WB	Sputtering	Ohmic	3×10^{-1}
Al	Vacuum evap.	Ohmic	2×10^{-1}
AlCu	Sputtering	Ohmic	5×10^{-1}
AlSi	Sputtering	Ohmic	8×10^{-2}
Ga	Alloying	Ohmic	-
GaIn	Alloying	Ohmic	-
GaSn	Alloying	Ohmic	-
GaZn	Sputtering	Ohmic	6×10^{-1}
In	Alloying	Ohmic	-
InMg	Sputtering	Ohmic	7×10^{-1}
InSn	Alloying	Ohmic	-

As seen in Table 6, a metal or alloy consisting of at least one of the elements B, Al, Ga and In was formed, as an electrode, on an n-type cubic boron nitride, so that the ohmic characteristic could be obtained. The contact resistance of the electrode formed through vacuum evaporation or sputtering was within an order of 10^{-2} -10^{-1} $\Omega \cdot cm^2$.

Example 5

V, VB_2, VC, V_3Co, VaG_3, VN, VS, V_3Si, V_2Zr, Nb, Nb_3Al, NbB_2, NbC, Nb_3Ga, Nb_3Ge, NbN, NbS_2, $NbSi_2$, Ta, TaB_2, TaC, TaN, TaS_2, and $TaSi_2$ were formed, as the electrodes according to the present invention, on a high-pressure synthesized Si-doped n-type cubic boron nitride, and the ohmic property and

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contact resistance of the thus formed electrodes were evaluated. The electrodes were formed at a substrate temperature of 400 ° C by vacuum evaporation or sputtering depending on the material.

At that time, an electrode pattern shown in Fig. 3 was formed on the cubic boron nitride by using a metal mask. The thickness of each of four electrodes was about 0.2-0.3 μm. The length was 0.8 mm and the width was 0.1 mm. They were arranged in parallel to each other at intervals of 0.1 mm, 0.2 mm, and 0.3 mm. The current-voltage characteristic between arbitrary electrodes was measured in a voltage range of from -10V to +10V to thereby judge the ohmic property of the electrodes. With respect to the electrodes the ohmic characteristic of which has been measured, the contact resistance was measured by using a transmission line model on the basis of the resistance and electrode distance between two electrodes of the electrode pattern of Fig. 3.

Table 7 shows the summary of the results of the above example.

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Table 7

Electrodes Containing IVa-Family Metal, Current-Voltage Characteristic, and Contact Resistance

Electrode (atom ratio)	Method of Formation	Current-Voltage Characteristic	Contact Resistance ($\Omega \cdot cm^2$)
V	Vacuum evap.	Ohmic	3×10^{-1}
VB_2	Sputtering	Ohmic	9×10^{-2}
VC	Sputtering	Ohmic	1×10^{-1}
V_3Co	Sputtering	Ohmic	7×10^{-1}
V_3Ga	Sputtering	Ohmic	5×10^{-1}
VN	Sputtering	Ohmic	8×10^{-2}
VS	Sputtering	Ohmic	5×10^{-2}
V_3Si	Sputtering	Ohmic	6×10^{-2}
V_2Zr	Sputtering	Ohmic	2×10^{-1}
Nb	Vacuum evap.	Ohmic	3×10^{-1}
Nb_3Al	Sputtering	Ohmic	5×10^{-1}
NbB_2	Sputtering	Ohmic	8×10^{-2}
NbC	Sputtering	Ohmic	1×10^{-1}
Nb_3Ga	Sputtering	Ohmic	5×10^{-1}
Nb_3Ge	Sputtering	Ohmic	6×10^{-1}
NbN	Sputtering	Ohmic	9×10^{-2}
NbS_2	Sputtering	Ohmic	5×10^{-2}
$NbSi_2$	Sputtering	Ohmic	4×10^{-2}
Ta	Vacuum evap.	Ohmic	1×10^{-1}
TaB_2	Sputtering	Ohmic	8×10^{-2}
TaC	Sputtering	Ohmic	1×10^{-1}
TaN	Sputtering	Ohmic	9×10^{-2}
TaS_2	Sputtering	Ohmic	3×10^{-2}
$TaSi_2$	Sputtering	Ohmic	4×10^{-2}

As seen in Table 7, Va-family metals such as V, Nb, Ta, VC, Nb_3Al, etc. and alloys containing a Va-family metal were formed, as the electrodes, on an n-type cubic boron nitride, so that the ohmic characteristic could be obtained although the contact resistance was a value within a range from 10^{-2} to 10^{-1} $\Omega \cdot cm^2$.

It is effective to perform suitable annealing after formation of electrodes with the metals used in the above examples 1-5. Although the optimum values of the annealing temperature and time vary depending on the electrode material to be used, it is preferable to select the annealing temperature to be about 300 °C - 1800 °C.

Since oxidation of the electrode may progress at the time of annealing depending on the electrode

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material, it is desirable to perform the annealing in an inert gas, N_2 or H_2, or in a vacuum. Further, in the case where the temperature is as high as 1000 ° C or more, it is preferable to perform annealing in an inert gas, N_2 or H_2, or in a vacuum, similarly to the above case, because of the oxidization or hexagonal boron-nitriding of the cubic boron nitride progresses when O_2 is present.

Moreover, it is more effective to use a high temperature at the time of formation of the electrodes in place of annealing. It is desirable to select this temperature to be 300 ° C - 1800 ° C, although it depends on the electrode material. It is also more effective that a metal alloy of known dopant (Si, S, or the like) and a IVa-family element (Ti, Zr, or Hf) is formed, as the electrodes, on the n-type semiconductor cubic boron nitride. Moreover, if the electrodes according to the present invention and metal electrodes coated with Au, Ag, or the like having low resistance, are laminated to be a multilayer structure, the effect becomes more remarkable.

As described above, a IVa-family metal (Ti, Zr, or Hf) or an alloy containing a IVa-family metal; a metal or an alloy containing Si or S; a metal or alloy consisting of at least one of B, Al, Ga and In; or a Va-family metal or an alloy containing a Va-family metal is formed, as an electrode, on an n-type semiconductor cubic boron nitride, so that an ohmic contact can be obtained with respect to the n-type semiconductor boron nitride.

Since this technique is indispensable to produce semiconductor cubic boron nitride devices, it is effective in formation of all kinds of devices.

Claims

1. An ohmic contact electrode for an n-type semiconductor cubic boron nitride comprising at least one layer of a material selected from the group consisting of: a IVa metal; an alloy with a IVa metal; a metal with Si or S; an alloy with Si or S; a metal with B, Al, Ga, or In; an alloy with B, Al, Ga, or In; a Va metal; and an alloy with a Va metal.

2. An ohmic contact electrode according to claim 1 wherein said at least one layer comprises Ti, TiAl, TiB_2, TiC, TiCr, TiFe, TiN, TiNb, TiNi, TiSi, Zr, ZrAl, ZrB_2, ZrC, ZrN, ZrNb, ZrNi, ZrS_2, $ZrSi_2$, Hf, HfB_2, HfC, HfN, HfS_2, or $HfSi_2$.

3. An ohmic contact electrode according to claim 1 wherein said at least one layer comprises CrSi, WrSi, MnSi, CoSi, NiSi, PtSi, AgSi, ZnSi, WCSi, MnZnSi, Ni_2BSi, PtPdSi, or AgAlSi.

4. An ohmic contact electrode according to claim 3 wherein said at least one layer is approximately 1% Si by weight.

5. An ohmic contact electrode according to claim 1 wherein said at least one layer comprises CrS, WrS, MnS, CoS, NiS, ptS, AgS, ZnS, WCS, MnznS, Ni_2BS, PtPdS, or AgAlS.

6. An ohmic contact electrode according to claim 5 wherein said at least one layer is approximately 1% S by weight.

7. An ohmic contact electrode according to claim 1 wherein said at least one layer comprises B, AlB_2, CrB_2, SiB_4, WB, Al, AlCu, AlSi, Ga, GaIn, GaSn, GaZn, In, InMg, or InSn.

8. An ohmic contact electrode according to claim 1 wherein said at least one layer comprises V, VB_2, VC, V_3Co, V_3Ga, VN, VS, V_3Si, V_2Zr, Nb, NbB_2, NbC, Nb_3Ga, Nb_3Ge, NbN, NbS_2, $NbSi_2$, Ta, TaB_2, TaC, TaN, TaS_2, $TaSi_2$, or $HfSi_2$.

9. An ohmic contact electrode according to claim 1 wherein said electrode is a multilayer structure comprising at least one layer of a metal selected from the group consisting of Au and Ag.

10. A method of forming an ohmic contact electrode comprising coating an Si-doped n-type cubic boron nitride with at least one layer of a material according to claim 1 at a substrate temperature from 300 ° C to 1800 ° C by vacuum evaporation, sputtering or alloying.

11. A method of forming an ohmic contact electrode according to claim 10 wherein the coating step is at a substrate temperature of substantially 400 ° C and the coating step is followed by an annealing step

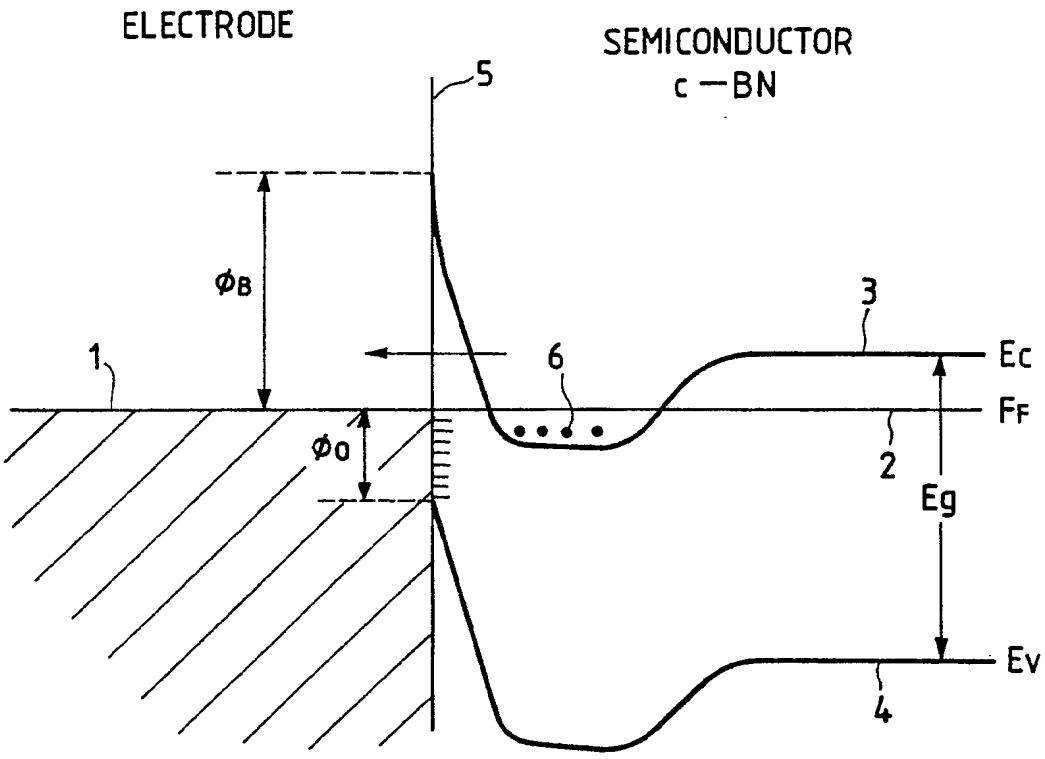
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wherein
the electrode is heated from 300 ° C to 1800 ° C in an atmosphere comprising an inert gas, N_2, H_2, or a vacuum.

12. A method of forming an ohmic contact electrode according to claim 10, wherein, after the coating step the Si-doped n-type cubic boron nitride is coated with at least one layer of a metal selected from the group consisting of Au and Ag.

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FIG. 1



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FIG. 2

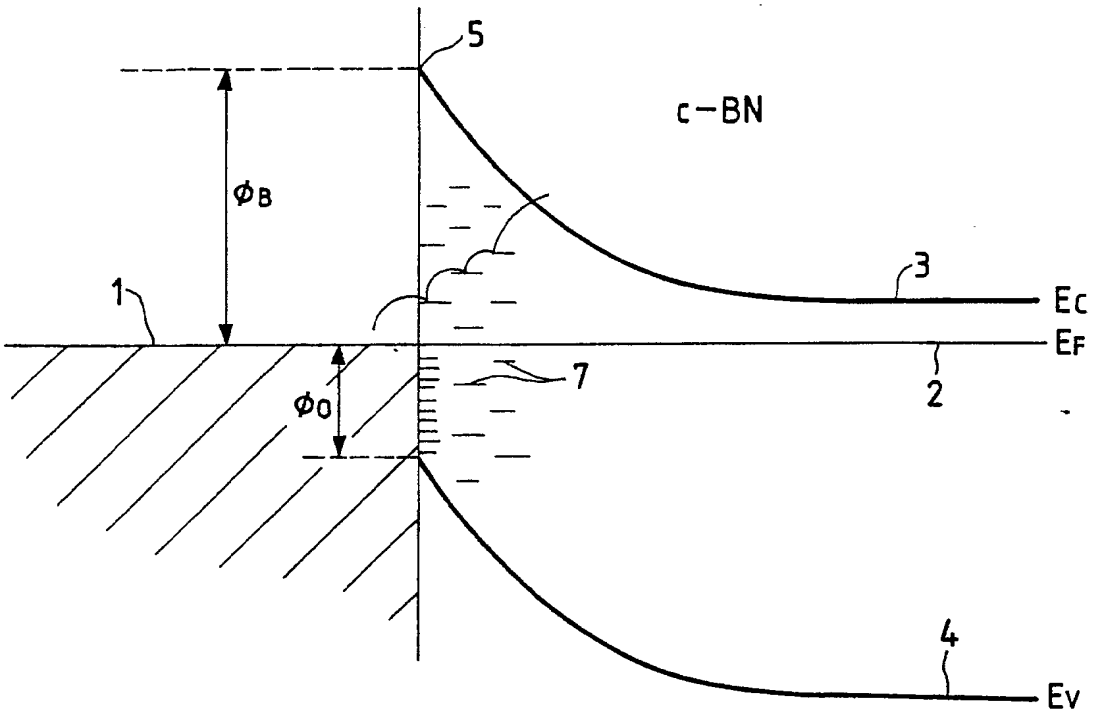
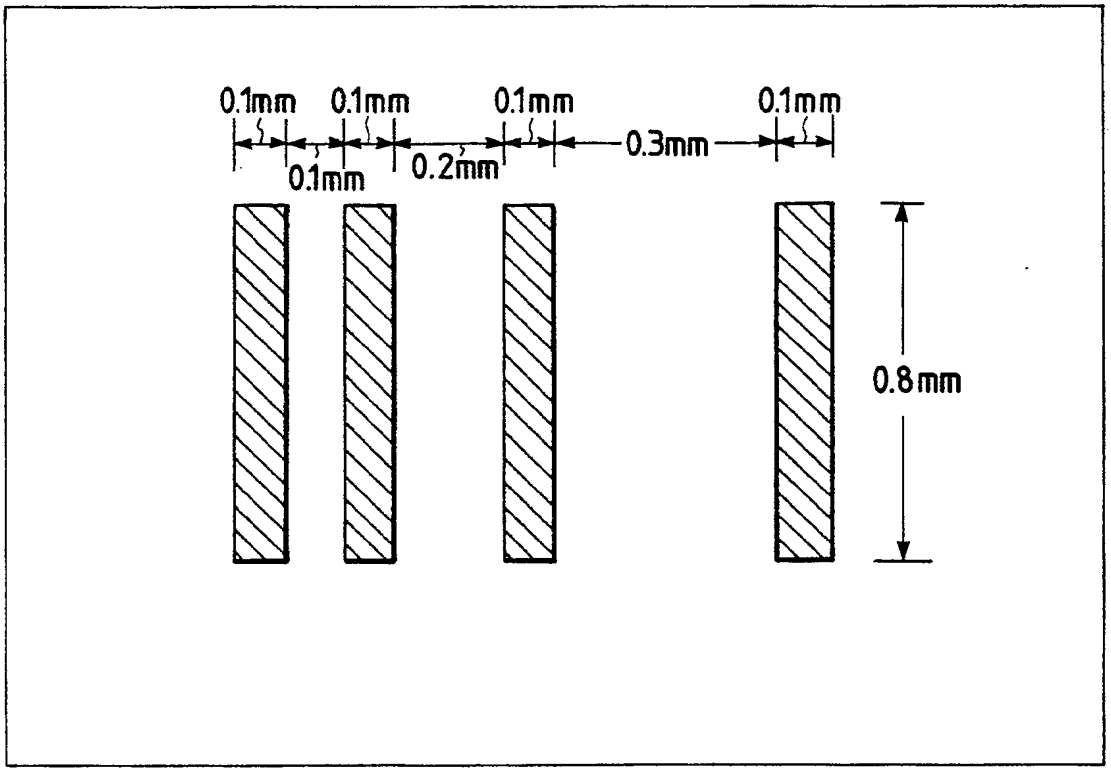


FIG. 3



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(60) **Références à d'autres documents nationaux apparentés :**

(71) **Demandeur(s) :** *STMICROELECTRONICS SA* *Société anonyme* — FR.

(72) **Inventeur(s) :** COLLARD EMMANUEL, DEFIVES DOMINIQUE et NOBLANC OLIVIER.

(73) **Titulaire(s) :**

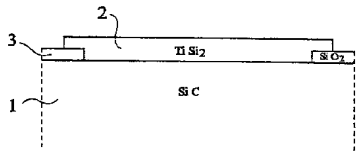
(74) **Mandataire(s) :** CABINET MICHEL DE BEAUMONT.

(54) PROCEDE DE REALISATION D'UN CONTACT SUR UN VARBURE DE SILICIUM.

(57) L'invention concerne un procédé de réalisation d'un contact ohmique sur un substrat de carbure de silicium, comprenant les étapes suivantes:

déposer sur le substrat (1) une couche (2) de siliciure de titane ($TiSi_2$),

recuire à une température de 500 à 800°C.



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PROCÉDÉ DE RÉALISATION D'UN CONTACT SUR DU CARBURE DE SILICIUM

La présente invention concerne la fabrication de composants semiconducteurs dans des substrats de carbure de silicium. Elle vise plus particulièrement la réalisation d'un contact présentant un comportement aussi proche que possible d'un comportement ohmique sur un substrat de carbure de silicium.

De façon classique, il est connu dans le domaine des semiconducteurs que, pour réaliser un contact ohmique entre une région semiconductrice et une métallisation, il faut que la concentration en dopants en surface de la région semiconductrice soit relativement élevée (supérieure à 10^{19} atomes/cm^3 dans le cas du silicium). Toutefois, dans le cas où le semiconducteur est du carbure de silicium, même pour des niveaux de dopage relativement élevés, le contact s'avère généralement ne pas être ohmique.

De plus, dans les composants à base de carbure de silicium, il n'est actuellement pas possible en pratique de réaliser des implantations et diffusions de dopants de type P dans des carbures de silicium de type N. Le dopant de type P couramment utilisé pour le carbure de silicium est de l'aluminium, et le dopant de type N est de l'azote. En effet, un recuit pour diffusion et implantation de dopant de type P nécessiterait une température de l'ordre de 1700°C, ce qui pose des problèmes technologiques aigus.

La demanderesse a proposé, dans le brevet français 2 764 117 du 30 mai 1997 (B3485), une structure de prise de contact ohmique sur un substrat de silicium faiblement dopé de type P. Cette structure est constituée d'une diode Schottky à très faible hauteur en direct, utilisée en inverse. Ce brevet préconise l'utilisation d'une couche de siliciure de platine formée par dépôt et recuit. On notera que ce brevet écarte explicitement l'utilisation d'un siliciure de titane.

Un objet de la présente invention est de réaliser une structure de contact utilisant une couche à faible barrière de Schottky comme contact ohmique ou quasi-ohmique sur un substrat de carbure de silicium.

Pour atteindre cet objet, la présente invention prévoit un procédé de réalisation d'un contact ohmique sur un substrat de carbure de silicium, comprenant les étapes suivantes :

déposer sur le substrat une couche de siliciure de titane ($TiSi_2$),

recuire à une température de 500 à 800°C.

Selon un mode de réalisation de la présente invention, la couche de $TiSi_2$ est obtenue par pulvérisation à partir d'une cible de $TiSi_2$.

La présente invention vise aussi un procédé de réalisation d'une diode Schottky, consistant à :

déposer sur une première face du substrat une couche propre à former avec ce substrat une jonction Schottky,

déposer sur une deuxième face de substrat une couche de $TiSi_2$,

recuire à une température de 500 à 800°C.

Selon un mode de réalisation de la présente invention, le procédé comprend une étape préliminaire de formation d'un oxyde et d'une ouverture dans cet oxyde.

Selon un mode de réalisation de la présente invention, la couche propre à former avec le substrat une diode Schottky est une couche de TiN.

Ces objets, caractéristiques et avantages de la présente invention, ainsi que d'autres de la présente invention seront exposés en détail dans la description suivante de modes de réalisation particuliers faite à titre non-limitatif en relation avec les figures jointes parmi lesquelles :

la figure 1 représente une vue en coupe schématique d'un contact quasi-ohmique selon la présente invention ;

la figure 2 représente une structure comprenant d'une part un contact quasi-ohmique, d'autre part un contact Schottky ; et

la figure 3 représente un exemple de structure de diode Schottky à contact ohmique en face arrière selon la présente invention.

Comme l'illustre la figure 1, la présente invention propose, pour réaliser un contact quasi-ohmique sur un substrat de carbure de silicium 1, de déposer sur ce substrat une couche 2 de siliciure de titane ($TiSi_2$). La zone de contact correspond éventuellement à une ouverture formée dans une couche d'oxyde de silicium 3.

Selon la présente invention, la couche 2 de $TiSi_2$ n'est pas une couche de siliciure formée à partir d'un dépôt de titane et d'un recuit, mais résulte d'un dépôt direct de siliciure de titane. Ce dépôt direct peut par exemple être réalisé par pulvérisation d'une cible de $TiSi_2$. Après ce dépôt, pour stabiliser la jonction, on procédera à un recuit, de préférence à une température de l'ordre de 500 à 800°C.

Ainsi, on constate que l'interface entre le $TiSi_2$ et le substrat de SiC constitue une barrière de Schottky de très faible hauteur en direct (< 0,5 V), dont la chute de tension inverse pour des valeurs faibles du courant est pratiquement nulle. Cette jonction Schottky utilisée en inverse, fournit donc un contact quasi-ohmique.

La figure 2 représente de façon très schématique la réalisation d'une diode Schottky en utilisant la présente invention. Le substrat 1 est un substrat de SiC. Sur la face infé-

rieure de ce substrat, on a formé une couche 2 de $TiSi_2$ de la façon décrite précédemment en relation avec la figure 1. Sur la face supérieure du substrat 1, on a formé une couche 5 destinée à former avec ce substrat un contact Schottky. Le substrat 1 est dopé de type N, par exemple à l'azote. La couche 5 est par exemple une couche de nitrure de titane (TiN) formant avec le substrat un contact Schottky ayant une tenue en tension inverse très élevée et présentant une barrière de tension en direct de l'ordre de 0,8 à 1 volt. Une telle barrière peut par exemple résulter du dépôt d'une couche d'un nitrure métallique tel que du TiN. De préférence, un recuit unique est effectué à une température de 500 à 800°C pendant quelques minutes pour stabiliser les jonctions entre le carbure de silicium et, d'une part, le TiN, d'autre part, le $TiSi_2$.

Une telle diode Schottky peut être polarisée en direct ou en inverse. Quand elle est polarisée en direct, la jonction entre les régions 5 et 1 présente une chute de tension de l'ordre du volt, et la jonction entre la région 1 et la couche de $TiSi_2$ est polarisée en inverse et présente une chute de tension pratiquement nulle. Quand la diode Schottky est polarisée en inverse, elle n'est normalement pas passante, la tension étant bloquée par la jonction entre les couches 5 et 1, jusqu'à des valeurs pouvant être supérieures à 1000 volts. En ce cas, peu importe la chute de tension (< 0,5 V) de la jonction en direct entre le substrat 1 de SiC et la couche 2 de $TiSi_2$ puisque la diode est normalement bloquée. Et, si jamais la diode est passante, cette chute de tension est totalement négligeable devant la chute de tension de l'autre jonction.

La figure 3 représente un exemple de réalisation pratique d'une diode Schottky. On retrouve le substrat de carbure de silicium 1, la couche de prise de contact 2 en $TiSi_2$ et le contact Schottky 5 en TiN déjà décrits en relation avec la figure 2.

Pour assurer une tenue en tension élevée en inverse de la jonction Schottky du côté de la face supérieure du substrat, on utilise par exemple une structure telle que représentée, qui

comprend une couche épitaxiée 11 de carbure de silicium dopé de type P, revêtue d'une couche isolante 12, couramment un oxyde de silicium. Ces deux couches sont ouvertes à l'emplacement où l'on veut établir un contact entre le substrat et la couche de TiN 5.

La périphérie supérieure du dispositif est creusée et revêtue d'une couche isolante 13, par exemple également en oxyde de silicium.

Sur la face supérieure, au-dessus de la couche de TiN, est déposée une métallisation 15, par exemple en aluminium, et, du côté de la face inférieure, sur la couche de $TiSi_2$, est déposée une métallisation 16, résultant par exemple de dépôts successifs de Ti, Ni, Au.

Bien entendu, la présente invention est susceptible de diverses variantes et le contact ohmique à base de $TiSi_2$ peut être utilisé dans de nombreuses structures sur carbure de silicium autres que celle qui a été représentée. Comme cela est représenté en figure 1, ce contact peut être localisé et n'être effectué qu'à l'intérieur d'une fenêtre formée dans une couche isolante.

Dans le cas où l'on utilise une structure de diode Schottky du type de celle représentée en figures 2 et 3, un avantage du contact en $TiSi_2$ selon la présente invention est qu'il nécessite un recuit du même ordre de grandeur (500 à 800°C) que la couche de TiN formant le contact de Schottky. Les deux recuits pourront donc être réalisés en une seule et même étape.

REVENDICATIONS

1. Procédé de réalisation d'un contact ohmique sur un substrat de carbure de silicium, caractérisé en ce qu'il comprend les étapes suivantes :

déposer sur le substrat (1) une couche (2) de siliciure de titane ($TiSi_2$),

recuire à une température de 500 à 800°C.

2. Procédé selon la revendication 1, caractérisé en ce que la couche de $TiSi_2$ est obtenue par pulvérisation à partir d'une cible de $TiSi_2$.

3. Procédé de réalisation d'une diode Schottky, caractérisé en ce qu'il consiste à :

déposer sur une première face du substrat une couche (5) propre à former avec ce substrat une jonction Schottky,

déposer sur une deuxième face de substrat une couche (2) de $TiSi_2$,

recuire à une température de 500 à 800°C.

4. Procédé selon la revendication 3, caractérisé en ce qu'il comprend une étape préliminaire de formation d'un oxyde et d'une ouverture dans cet oxyde.

5. Procédé selon la revendication 3, caractérisé en ce que la couche propre à former avec le substrat une diode Schottky est une couche de TiN.

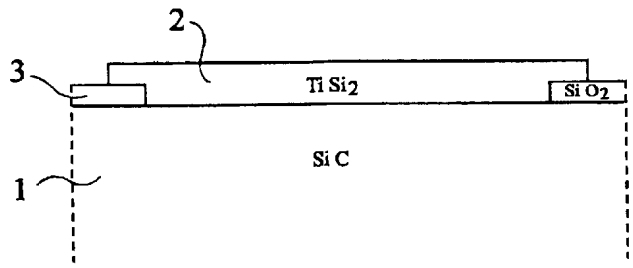


Fig 1

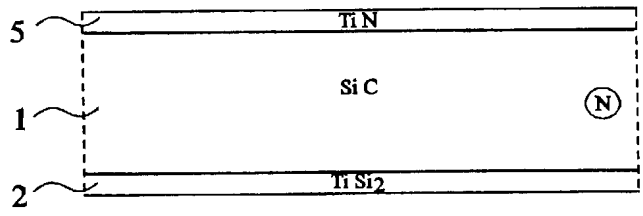


Fig 2

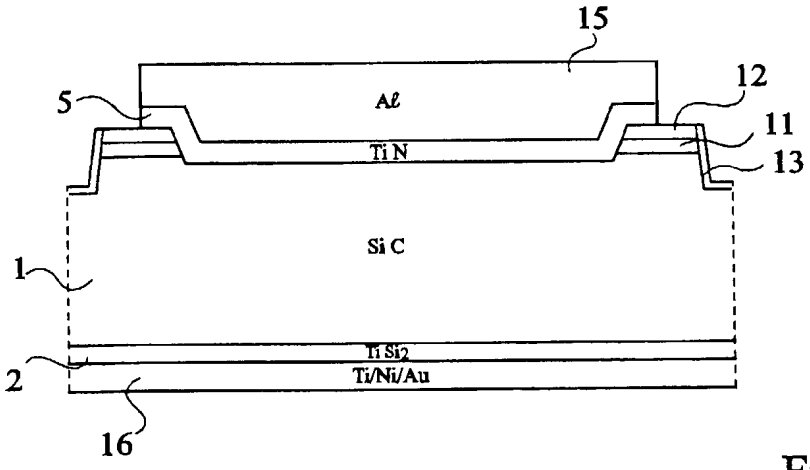


Fig 3

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RAPPORT DE RECHERCHE PRÉLIMINAIRE

établi sur la base des dernières revendications déposées avant le commencement de la recherche

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DOCUMENTS CONSIDÉRÉS COMME PERTINENTS		Revendication(s) concernée(s)	Classement attribué à l'invention par l'INPI
Categorie	Citation du document avec indication, en cas de besoin, des parties pertinentes		
X	GETTO, R. ET AL.: "Characterization of sputtered titanium silicide ohmic contacts on n-type 6H-silicon carbide" MATERIALS SCIENCE AND ENGINEERING B, vol. B61-B62, 30 juillet 1999 (1999-07-30), pages 270-274, XP001014599 Switzerland * le document en entier *	1,2	H01L29/45 H01L29/872
Y	---	3	
Y	KAKANAKOVA-GEORGIEVA A ET AL: "Characterization of ohmic and Schottky contacts on SiC" THIN SOLID FILMS, ELSEVIER-SEQUOIA S.A. LAUSANNE, CH, vol. 343-344, avril 1999 (1999-04), pages 637-641, XP004178442 ISSN: 0040-6090 * le document en entier *	3	

A	TANG S M ET AL: "TITANIUM SILICIDE OHMIC CONTACTS FOR HIGH TEMPERATURE S-SIC DEVICES" EXTENDED ABSTRACTS, ELECTROCHEMICAL SOCIETY. PRINCETON, NEW JERSEY, US, vol. 88-2, 21 septembre 1988 (1988-09-21), page 680 XP000050447 ISSN: 0160-4619 * le document en entier *	1-5	DOMAINES TECHNIQUES RECHERCHÉS (Int.CL.7) H01L

A	IQBAL CHAUDHRY, M. ET AL.: "A study of ohmic contacts on b-SiC" INTERNATIONAL JOURNAL OF ELECTRONICS, vol. 71, no. 3, 1991, pages 439-444, XP001015410 * le document en entier *	1-5	

Date d'achevement de la recherche	Examinateur
10 août 2001	Nesso, S

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DESCRIPTION FR2814856

The present invention relates to the manufacture of semiconductor components in silicon carbide substrates.

It relates more particularly to the production of a contact having a behavior as close as possible to an ohmic behavior on a silicon carbide substrate.

Conventionally, it is known in the field of semiconductors that, in order to achieve ohmic contact between a semiconductor region and a metallization, the concentration of dopants on the surface of the semiconductor region must be relatively high (greater than 1019 atoms / cm3 in the case of silicon). However, in the case where the semiconductor is silicon carbide, even for relatively high doping levels, the contact generally turns out not to be ohmic.

In addition, in components based on silicon carbide, it is currently not possible in practice to carry out implantations and diffusions of P-type dopants in N-type silicon carbides. The P-type dopant commonly used for silicon carbide is aluminum, and the N-type dopant is nitrogen. Indeed, annealing for diffusion and implantation of P-type dopant would require a temperature of the order of 1700oC, which poses acute technological problems.

The Applicant has proposed, in French Patent 2,764,117 of May 30, 1997 (B3485), an ohmic contact making structure on a lightly doped P-type silicon substrate.

This structure consists of a Schottky diode with very low height in direct, used in reverse. This

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patent recommends the use of a layer of platinum silicide formed by deposition and annealing. It will be noted that this patent explicitly excludes the use of a titanium silicide.

An object of the present invention is to provide a contact structure using a layer with a low Schottky barrier as an ohmic or quasi-ohmic contact on a silicon carbide substrate.

To achieve this object, the present invention provides a process for producing an ohmic contact on a silicon carbide substrate, comprising the following steps: depositing on the substrate a layer of titanium silicide (TiSi2), annealing at a temperature of 500 to 800 C.

According to an embodiment of the present invention, the TiSi2 layer is obtained by sputtering from a Tis2 target.

The present invention also relates to a method for producing a Schottky diode, consisting in: depositing on a first face of the substrate a layer capable of forming a Schottky junction with this substrate, depositing on a second face of substrate a layer of TiSi2, < img class = "EMIRef" id = "011734589-00020001" />

anneal at a temperature of 500 to 800OC.

According to an embodiment of the present invention, the method comprises a preliminary step of forming an oxide and an opening in this oxide.

According to an embodiment of the present invention, the layer capable of forming with the substrate a Schottky diode is a layer of TiN.

These objects, characteristics and advantages of the present invention, as well as others of the present invention will be explained in detail in the following description of particular embodiments given without limitation in relation to the attached figures, among which: the figure 1 shows a schematic sectional view of a quasi-ohmic contact according to the present invention; FIG. 2 represents a structure comprising on the one hand a quasi-ohmic contact, on the other hand a Schottky contact and FIG. 3 represents an example of a Schottky diode structure with ohmic contact on the rear face according to the present invention.

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As illustrated in FIG. 1, the present invention proposes, to make a quasi-ohmic contact on a substrate of silicon carbide 1, to deposit on this substrate a layer 2 of titanium silicide (TiSi2). The contact zone optionally corresponds to an opening formed in a layer of silicon oxide 3.

According to the present invention, the layer 2 of TiSi2 is not a silicide layer formed from a deposition of titanium and an annealing, but results from a direct deposition of titanium silicide. This direct deposition can for example be carried out by sputtering a TiSi2 target. After this deposition, to stabilize the junction, an annealing will be carried out, preferably at a temperature of the order of 500 to 8000C.

Thus, it can be seen that the interface between TiSi2 and the SiC substrate constitutes a Schottky barrier of very low direct height (<0.5 V), whose reverse voltage drop for low current values is practically zero . This Schottky junction used in reverse, therefore provides a quasi-ohmic contact.

FIG. 2 very schematically shows the production of a Schottky diode using the present invention. The substrate 1 is an SiC substrate. On the underside

lower of this substrate, a layer 2 of TiSi2 was formed in the manner described above in relation to FIG. 1. On the upper face of the substrate 1, a layer 5 has been formed intended to form a Schottky contact with this substrate. The substrate 1 is doped with type N, for example with nitrogen. Layer 5 is for example a layer of titanium nitride (TiN) forming with the substrate a Schottky contact having a very high reverse voltage withstand and having a live voltage barrier of the order of 0.8 to 1 volt. Such a barrier can for example result from the deposition of a layer of a metallic nitride such as TiN. Preferably, a single annealing is carried out at a temperature of 500 to 800 ° C. for a few minutes to stabilize the junctions between the silicon carbide and, on the one hand, the TiN, on the other hand, the TiSi2.

Such a Schottky diode can be forward or reverse biased. When it is forward biased, the junction between regions 5 and 1 shows a voltage drop in the order of a volt, and the junction between region 1 and the TiSi2 layer is reverse biased and shows a voltage drop practically nothing. When the Schottky diode is reverse biased, it is normally not conducting, the voltage being blocked by the junction between layers 5 and 1, up to values which can be greater than 1000 volts. In this case, it does not matter the voltage drop (<0.5 V) of the direct junction between the SiC substrate 1 and the layer 2 of TiSi2 since the diode is normally blocked.

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And, if the diode is always on, this voltage drop is completely negligible compared to the voltage drop of the other junction.

FIG. 3 represents a practical embodiment of a Schottky diode. We find the silicon carbide substrate 1, the contact-making layer 2 made of TiSi2 and the Schottky contact 5 made of TiN already described in relation to FIG. 2.

To ensure high voltage resistance opposite to the Schottky junction on the side of the upper face of the substrate, a structure as shown is used, for example.

comprises an epitaxial layer 11 of P-type doped silicon carbide, coated with an insulating layer 12, commonly a silicon oxide. These two layers are open at the location where it is desired to establish contact between the substrate and the TiN 5 layer.

The upper periphery of the device is hollowed out and coated with an insulating layer 13, for example also made of silicon oxide.

On the upper face, above the TiN layer, is deposited a metallization 15, for example of aluminum, and, on the side of the lower face, on the TiSi 2 layer, is deposited a metallization 16, resulting for example from successive deposits of Ti, Ni, Au.

Of course, the present invention is susceptible of various variants and the ohmic contact based on TiSi2 can be used in many structures on silicon carbide other than that which has been shown. As shown in FIG. 1, this contact can be located and only be carried out inside a window formed in an insulating layer.

In the case where a Schottky diode structure of the type shown in FIGS. 2 and 3 is used, an advantage of the TiSi2 contact according to the present invention is that it requires annealing of the same order of magnitude (500 to 800 ° C.) as the TiN layer forming the Schottky contact. The two anneals can therefore be carried out in one and the same step.

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CLAIMS FR2814856

CLAIMS

1.
Process for producing an ohmic contact on a silicon carbide substrate, characterized in that it comprises the following steps: depositing on the substrate (1) a layer (2) of titanium silicide (TiSi2), annealing with a temperature from 500 to 8000C.

2.
Method according to claim 1, characterized in that the TiSi2 layer is obtained by sputtering from a TiSi2 target.

3.
Method for producing a Schottky diode, characterized in that it consists in: depositing on a first face of the substrate a layer (5) suitable for forming with this substrate a Schottky junction, depositing on a second face of substrate a layer (2) of TiSi2, anneal at a temperature of 500 to 800OC.

4.
A method according to claim 3, characterized in that it comprises a preliminary step of forming an oxide and an opening in this oxide.

5.

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Method according to claim 3, characterized in that the layer capable of forming a Schottky diode with the substrate is a layer of TiN.

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(71) Applicant: **AGENCY OF INDUSTRIAL SCIENCE AND TECHNOLOGY**
Chiyoda-ku Tokyo (JP)

(72) Inventors:
- **Hara, Shiro**
  Tsukuba-shi, Ibaraki (JP)
- **Kajimura, Koji**
  Tsukuba-shi, Ibaraki (JP)
- **Okushi, Hideyo**
  Tsukuba-shi, Ibaraki (JP)
- **Teraji, Tokuyuki**
  Tsukuba-shi, Ibaraki (JP)

(74) Representative: **Beresford, Keith Denis Lewis**
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(54) Structure and fabrication method for schottky and ohmic electrodes onto semiconductor devices

(57) A novel electrode structure for Schottky electrodes and Ohmic electrodes and novel methods of fabricating electrodes by freely controlling electric characteristics of electrodes on semiconductors. Interface states density of a semiconductor (11) after deposition of an electrode metal (13, 14) is decreased by flattening the surface of the semiconductor on an atomic level to freely control the Schottky barrier height. The method can realize an ideal Ohmic electrode having a Schottky barrier height of substantially zero. The Schottky barrier height is varied freely by decreasing the interface level density and selecting work function of the electrode metal. The method can provide stable Schottky and Ohmic electrodes (13, 14) without need of heat treatment. Further, the method can provide Ohmic electrodes without high concentration doping.

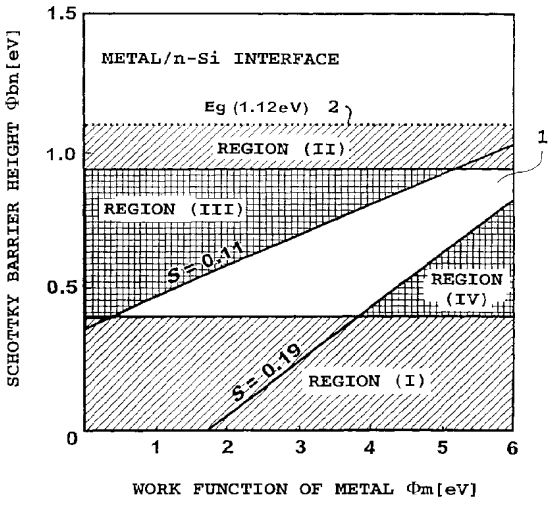


FIG.2

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Description

The present invention relates to an electrode provided on a semiconductor and a method for fabricating an electrode on a semiconductor. The present invention is applicable to various fields of industry which involve fabrication of electrodes on semiconductors. For example, the present invention can be applied to various semiconductor devices such as microprocessors, memories, power devices and the like.

In conventional fabrication methods of electrodes on semiconductors, rectifying potential barriers, i.e., Schottky barriers, which will appear on the interfaces between electrode metals and semiconductors, have been impossible to control their magnitude. Hence, it has been impossible to artificially control the rectifying properties and conductivities of all the electrodes including not only those semiconductor devices whose performance depends directly on the heights of Schottky barriers, such as Schottky diodes as typical examples, but also those electrodes in the semiconductor devices thus far fabricated. The Schottky barrier height and leakage current, which is an indicator of important performance of interface on the device, inconveniently vary to a greater extent depending on combination of metals and semiconductors as well as on the process in which the interface is formed. Conventionally, this problem has been solved empirically. That is, when a new semiconductor has been developed, a method for fabricating an electrode on the semiconductor has been investigated and developed for each metal one after another until a suitable one is obtained. In other words, going into detail, there have conventionally been developed unique fabrication methods for fabricating electrodes adapted for respective combinations of semiconductors and electrode metal materials. Because of having had to resort to empirical rule, methods for fabricating electrodes differ from institution to institution or from manufacturer to manufacturer. There has been established no fabrication method for fabricating electrodes which method can be uniformly applied to any or most of electrode metal/semiconductor combinations. Under the circumstances, development of electrodes has needed much human and monetary resources for investigation. In all the semiconductor device fabrication technology inclusive of technologies for fabricating integrated semiconductor devices such as VLSIs and the like, only the technology for forming electrodes has remained as a unit technology that is out of reach of successful efforts for free designing.

More specific explanation will be made as to how to fabricate electrodes for Schottky electrodes and Ohmic electrodes, respectively.

First, in the case of Schottky electrodes, it was almost impossible to control their Schottky barrier height and, hence there was no other way than accept such non-controlled values as they are. For example, silicon Schottky diodes have almost fixed barrier heights on the order of about 0.5 to about 0.7 eV. While use of different metals or application of heat to cause interface reaction will vary barrier height to some extent, the width of change in barrier height is at most about 0.2 eV. Thus, in Schottky devices, the Schottky barrier height, which is the most important indicator for the device characteristics, cannot be controlled freely.

In the case of Ohmic electrodes, a severer problem arises. That is, electrode fabrication inevitably results in the formation of a Schottky barrier whose interface usually shows rectifying resistance. As a result, formation of a conductive Ohmic electrode, which is contrary to the fabrication of an electrode having a rectifying resistance, requires in principle a very difficult technique. Practically, in fabrication of almost all of the Ohmic electrodes fabricators have presupposed presence of a Schottky barrier in the interface between the electrode metal and semiconductor and then taken a measure to allow a leakage current to flow in the barrier.

There have been known several methods for increasing a leakage current. For example, a method for fabricating a device in which impurity ions are doped to extremely increase the concentration of electrons or holes which contribute to conductivity in the vicinity of the surface of the semiconductor (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M.Murakami: Materials Science Reports, 5, 273 (1990), P.A. Barnes and A.Y. Cho, Appl. Phys. Lett, 33, 651 (1978), and T. Uemoto: Jpn. J. Appl. Phys., 34, L7 (995)). This reduces the width of the Schottky barrier, i.e., decreases the thickness of the depletion layer and, hence, a leakage current in the form of tunneling current, can be flown in the thin depletion layer. However, in the case of SiC, GaN and the like new semiconductor materials that are under development are usually difficult to dope with impurities at high concentrations so that electrodes having sufficiently low resistance cannot be obtained in most cases. The above-described method is not simple nor convenient in some cases since it requires an ion implanting apparatus or an electric oven for diffusing impurities in gaseous phases. Furthermore, the concentration of impurities has an upper limit at about $10^{20}cm^{-3}$. This automatically determines the minimum width of the depletion layer and, hence, sets technical limits to the interface resistance of an Ohmic electrode to be realized. Theoretically, this approach is unsuccessful in making the interface resistance of the Ohmic electrode to be zero. In addition, there may occur reflection of electrons or holes between the high concentration doped region and the low concentration doped substrate. This reflection of carriers increases the resistance of the electrode. From these, the interface resistance of an Ohmic electrode fabricated on a silicon substrate is limited to about $10^{-8}\ \Omega cm^2$ based on the technical restrictions as described above.

Another method for fabricating an Ohmic electrode is to heat the electrode to decrease its resistance (cf., e.g., E. H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M.

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Murakami: Materials Science Reports, 5, 273 (1990), H.C. Card: IEEE Trans. Electron Devices, ED-23, 538 (1976), T.C. Shen, G.B. Gao, and H. Morkoç: J. Vac. Sci. Technol., B10, 2113 (1992), N. Braslau, J.B. Gunn, and J.L. Staples: Solid-State Electronics, 10, 381 (1967), J. Appl. Phys., 77, 1317 (1967), and J. Crofton, P.G. McMullin, J.R. Williams, and M.J. Bozack: J. Appl. Phys., 77, 1317 (1995)). In this method, after the electrode metal is deposited, heat treatment is carried out so that there occurs interface chemical reaction between the metal and the semiconductor and metallization of the semiconductor proceeds in the vicinity of the interface. This induces impurity level or defect level in the depletion layer of the Schottky barrier. These levels generate leakage current. This method is simple and can be used in combination with high concentration doping. Because of the advantages, the method is used without fail in the conventional process of fabricating electrodes. However, interface reaction is complicated since it differs from a metal/semiconductor system to another and the mode of reaction varies widely depending on temperature and time of heat treatment. In some reaction systems, it is often the case that heating results in the formation of good Schottky barrier, which means heating does not always enhance Ohmicity (cf., e.g., S. Zaima, T. Yamauchi, Y. Koide, and Y. Yasuda: Appl. Surf. Sci., 70, 624 (1993)). This is a decisive defect of the above-described heating method.

Still another approach is to grow on a first semiconductor a crystal of a second semiconductor having a bandgap smaller than that of the first semiconductor so that the highest possible Schottky barrier height can be decreased to facilitate the formation of Ohmic contact (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M.Murakami: Materials Science Reports, 5, 273 (1990), and T.C. Shen, G.B. Gao, and H. Morkoç: J. Vac. Sci. Technol., B10, 2113 (1992)). This method involves heteroepitaxy of a semiconductor and, hence, its application is limited to semiconductor systems which allow heteroepitaxy.

Further, heteroepitaxy itself is a high technology which requires a complicated manufacturing process, which increases production costs. Therefore, the method is suited to a very limited range of semiconductor materials, more particularly, new semiconductor materials having wide bandgaps, such as GaN and the like, which are difficult to dope impurities with high concentration doping of impurities.

The above-described three methods use large process apparatus suitable for fabricating devices and thus are not simple. Accordingly, in early stages of research and development for evaluating electric properties of materials or developing various devices, simpler means such as scratching of semiconductor or the like is used (here, by the term "scratching" is meant to hurt the surface of a semiconductor with a diamond needle or the like to coarsen it (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988). On a coarse surface, a lot of structural defects are induced which increase leakage current. This method is quite inconvenient for making fine structures in the fabrication of semiconductor devices. In most cases, no good interface resistance can be obtained.

As described above, electrodes have been fabricated based on empirical rules. The primary reason for this is a lack of common or uniform understanding of the mechanism in forming a metal/semiconductor interface potential barrier. Uncontrollability of Schottky barriers and complexity of the mechanism of Ohmic contact formation which is attributable thereto would be due to the fact that Schottky barrier height is by nature fixed to a certain level. Fixation of Schottky barrier height of a semiconductor is equivalent to the fact that the Fermi level is fixed in the bandgap of the semiconductor on the metal/semiconductor interface. The fixation of Fermi level is usually referred to pinning of the Fermi level. The pinning of the Fermi level occurs as a result of generation of electron level in the bandgap of a semiconductor on the interface between the metal and the semiconductor. Carriers flow from bulk to the interface, i.e., electrons in the case of n-type semiconductor or holes in the case of p-type semiconductor flow from the bulk semiconductor to the interface and the carriers are trapped therein to create an electric double layer of the semiconductor bulk and the interface, i.e., a potential barrier or Schottky barrier.

Reviewing the development of Schottky barrier, in 1947, J. Bardeen stated that the interface level is caused by electronic level due to dangling bonds and the like existing on the surface of the semiconductor (cf. J. Bardeen: Phys. Rev., 71, 717 (1947)). Thereafter, however, in view of the impossibility of controlling the surface level density accurately by the technology available at that time, the leading view was that surface level density was uncontrollable and intrinsic to the material concerned, and interface electron level embedded in a solid should be an essential electron level that was more difficult to control than the surface level. The belief that pinning was intrinsic to materials and cannot be controlled artificially has led to a theory of MIGS (Metal-induced Gap States) which explains a cause of generation of interface levels (cf. V. Heine: Phys. Rev., 138, A1689 (1965)). According to this theory, interface levels are induced when a metal approaches toward the semiconductor. Since 1965 when V. Heine proposed it, the MIGS theory has been leading to date. The MIGS theory has inhibited research of a technology which controls the height of Schottky barrier. In fact, regardless of theories, there have been unavailable high technologies that can control interface level density in actual semiconductor devices.

Concerning numerical consideration of pinning, the work which referred to Schottky barrier for the first time was by W. Schottky (cf. W. Schottky: Naturwissenschaften, 26, 843 (1938) and N.F. Mott: Proc. Camb. Philos. Soc., 34, 568 (1938)). According to Schottky, the Schottky barrier height, φbn, of a n-type semiconductor is given by the following equation (1):

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$$\varphi bn=\varphi m-\chi S+C \quad (1)$$

wherein φm is a work function of the metal, χS is electron affinity of the semiconductor, C is a constant no greater than several meV. On the other hand, the Schottky barrier height of a p-type semiconductor in a pinning-free state is given by the following equation (2):

$$\varphi bp=Eg-(\varphi m-\chi S+C) \quad (2)$$

wherein Eg is a bandgap.

The equations (1) and (2) are called Schottky models. However, no interface has been realized that meets these equations. The actual interface is expressed by the following equation (3):

$$\varphi bn=S(\varphi m-\chi S)+C \quad (3)$$

wherein S is a coefficient which indicates a dependence of φbn on φm and $0 \leq S \leq 1$.

When S=0, φbn is constant and the interface is pinned strongly. This state is called a Bardeen barrier. On the contrary, when S=1, the equation (3) is the same as the equation (3) and represents a pinning-free interface according to the Schottky-Mott model. Actual interfaces fall between the both states. Heretofore, the S factor has been believed to be a physical property specific to the material concerned and, hence, beyond control.

Table 1 below summarizes values of S factor and maximum and minimum values of Schottky barrier height of representative semiconductors.

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Table 1

PINNING RATIOS S OF VARIOUS KNOWN SEMICONDUCTORS AND RANGE OF SCHOTTKY BARRIER HEIGHT

SEMI-CONDUCTOR	S FACTOR	INTERCEPT PARAMETER	MINIMUM SCHOTTKY BARRIER HEIGHT [eV]	MAXIMUM SCHOTTKY BARRIER HEIGHT [eV]
Ge	$0.18 \geq S \geq 0.05$[1]	$-0.23 \leq C_2 \leq 0.11$[1]		
Si(001)	$0.19 \geq S \geq 0.11$[1]	$-0.34 \leq C_2 \leq 0.35$[1]	0.37 ($GdSi_2$/$HoSi_2$)[2]	0.94 ($IrSi_3$)[3]
GaAs(001)	$0.22 \geq S \geq 0.06$[1]	$-0.40 \leq C_2 \leq 0.075$[1]	0.62 (Mg)[4]	0.96 (Cu)[4]
GaP	$0.21 \geq S \geq 0.07$[1]	$0.45 \leq C_2 \leq 0.80$[1]		
InP	$0.37 \geq S \geq 0.24$[1]	$-1.00 \leq C_2 \leq 0.81$[1]		
ZnS	$0.66 \geq S \geq 0.21$[1]	$-1.63 \leq C_2 \leq 0.91$[1]		
ZnSe	$0.24 \geq S \geq 0.17$[1]	$-0.25 \leq C_2 \leq 0.57$[1]		
6H-SiC(0001)	$0.25 \geq S \geq 0.23^{5-10}$	$-3.5 \leq C_2 \leq 0.15^{5-10}$	0.73 (Ti)[6]	1.37 (Au)[5]

1. B.L. Sharma and S.C. Gupta, Solid State Technology, 23(6), 90 (1980).
2. K.N. Tu, R.D. Thompson, and B.Y.Tsaur, Appl. Phys. Lett. 38, 626(1981).
3. C.S. Petersson, et al., J. Appl. Phys., 50, 3357 (1979).
4. J.R. Waldrop, J. Vac. Sci. Technol., B2, 445 (1984).
5. J.R. Waldrop, et al., J. Appl. Phys., 72, 4757 (1992).
6. J.R. Waldrop, et al., Appl. Phys. Lett., 62, 2685 (1993).
7. L.M. Porter, et al., Mat. Res. Soc. Symp. Proc., 287, 471 (1993).
8. L.M. Porter, et al., J. Mat. Res., 10, 26 (1995).
9. L.M. Porter, et al., J. Mat. Res., 10, 668 (1995).
10. L.M. Porter, et al., M. Mat. Res. 10, 2336 (1995).

Fig. 1 is a graphical presentation of the data in Table 1, plotting Schottky barrier height (φbn [eV]) against work function of a metal (φm [eV]) taking as an example of an n-type Si(001) semiconductor substrate. Fig. 1 shows that the Schottky barrier height was limited within a certain range for various metals. In Fig. 1, reference numeral 1 denotes an area representing the range in which the Schottky barrier heights of conventionally fabricated metal/n-Si interfaces fall and 2 denotes a line which represents an absolute upper limit of the Schottky barrier height of metal/n-Si interfaces corresponding to the bandgap Eg=1.12 eV. With different metals, there are always upper and lower limits of the Schottky

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barrier heights.

Consequently, it has heretofore been impossible to freely control the Schottky height of metal/semiconductor interfaces.

The present invention is directed to overcoming the problem of uncontrollability of the Schottky barrier height between an electrode metal and a semiconductor, which problem has been an important subject since a transistor was invented.

Also, the present invention is aimed at solving the scientific and technological problem of uncontrollability of Ohmic electrodes, which has heretofore been considered a different problem from the uncontrollability of Schottky barrier height.

Further, the present invention is intended to provide a systematic technology which can control both Schottky electrodes and Ohmic electrodes, that have been treated separately one from another, based on a single principle that allows understanding them consistently. More specifically, the present invention is directed to overcoming the problem of uncontrollability of pinning of Fermi level of the interface of metal/semiconductor that has been impossible to control conventionally.

Therefore, an object of the present invention is to provide a method for fabricating Schottky electrode or Ohmic electrode formed at the interface between an electrode metal/semiconductor, which enables freely controlling electric properties of the electrode formed on the semiconductor.

Another object of the present invention is to provide an electrode structure comprising an electrode having a controlled Schottky barrier height of the interface between the electrode metal and the semiconductor.

According to a first aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

decreasing a surface states density of the surface of the semiconductor.

According to a second aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

controlling a Schottky barrier height of a rectifying Schottky electrode formed on the surface of the semiconductor.

Here, the control of the Schottky barrier height of the Schottky electrode may be carried out by controlling flatness of an electrode metal/semiconductor interface.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling a step density on an atomic level of an electrode metal/semiconductor interface.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling selecting a work function of the metal.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling the Schottky barrier height of the Schottky electrode under conditions without giving thermal hysteresis.

According to a third aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

fabricating a Schottky electrode from a metal having a high work function, and fabricating an Ohmic electrode from a metal having a low work function, for an n-type semiconductor, or

fabricating a Schottky electrode form a metal having a low work function and an Ohmic electrode from a metal having a high work function, for a p-type semiconductor.

Here, the method may further comprise the step of heating.

According to a fourth aspect of the present invention, there is provided a method of fabricating an Ohmic electrode, comprising the step of: forming flat electrode metal/semiconductor interface on an atomic level.

According to a fifth aspect of the present invention, there is provided a method of fabricating an Ohmic electrode, comprising the step of: forming an electrode metal/semiconductor interface having a low step density on an atomic level.

According to a sixth aspect of the present invention, there is provided a method of fabricating an electrode, comprising the step of:

fabricating an Ohmic electrode as described above in a highly integrated electronic device.

Here, the semiconductor may be made of a semiconductor selected from the group consisting of Si and SiC.

The electrode metal may be selected from the group consisting of Al, Au, Mo and Ti.

According to a seventh aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor having an interface portion which is flat on an atomic level.

According to an eighth aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor having a Schottky barrier height which is impossible to realize by conventional method.

According to a ninth aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor containing no high concentration impurity.

According to a tenth aspect of the present invention, there is provide an Ohmic electrode structure having a Schottky barrier height which is substantially zero.

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Here, the semiconductor may be made of a semiconductor selected from the group consisting of Si and SiC.

The electrode metal may be selected from the group consisting of Al, Au, Mo and Ti.

According to an eleventh aspect of the present invention, there is provided a method of fabricating an electrode, comprising the step of:

oxidizing a surface layer of silicon or silicon carbide on a surface of a semiconductor and removing the resulting oxide film.

Here, the oxidizing of the silicon or silicon carbide may be carried out by heating the silicon or silicon carbide in an oxidative gaseous atmosphere.

Removing the oxide film may be carried out by reacting the oxide film with a reducing liquid or gas.

The silicon or silicon carbide may be n-type silicon or n-type silicon carbide, and wherein the electrode metal is a metal having a work function lower than that of noble metals.

The silicon carbide may be p-type silicon carbide, and wherein the electrode material is a noble metal or a metal having a work function of a level substantially equal to that of noble metals.

The electrode material may be titanium (Ti).

The electrode material may be aluminum (Al).

The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of the embodiment thereof taken in conjunction with the accompanying drawings.

Fig. 1 is a graph plotting Schottky barrier height of a Schottky electrode fabricated on an n-type Si(001) substrate by a conventional method against the work function of the electrode metal;

Fig. 2 is a graph illustrating regions representing Schottky barrier heights realized by the fabrication method of the present invention;

Fig. 3 is a graph illustrating current-voltage characteristics of Ti electrodes on SiC according to examples of the present invention;

Fig. 4 is a graph illustrating current-voltage characteristics of a Ti electrode on SiC which has been subjected to a conventional treatment with 5% hydrofluoric acid;

Fig. 5 is a graph illustrating current-voltage characteristics of an Al electrode on SiC according to the present invention;

Fig. 6 is a graph illustrating current-voltage characteristics of Al electrodes on SiC according to the present invention;

Fig. 7 is a graph illustrating current-voltage characteristics of an Al electrode on Si(111) which has been subjected to a conventional treatment with 5% hydrofluoric acid;

Fig. 8A is a sketch prepared based on an optical micrograph of the surface of a Ti electrode fabricated by the fabrication method according to EXAMPLE 4 of the present invention;

Fig. 8B is a schematic cross sectional view showing the Ti electrode illustrated in Fig. 8A;

Fig. 9A is a sketch prepared based on an optical micrograph of the surface of an Ni electrode fabricated by a conventional fabrication method;

Fig. 9B is a schematic cross sectional view showing the Ti electrode illustrated in Fig. 9A;

Fig. 10 is a graph illustrating logarithmic current-voltage characteristics of Au electrodes on 6H-SiC(0001) substrates according to EXAMPLE 7 of the present invention;

Fig. 11 is a graph plotting Schottky barrier height of electrode metals fabricated on 6H-SiC(0001) substrates against the work function of the electrode metals; and

Fig. 12 is a graph illustrating new areas for Schottky barrier heights of electrode metals fabricated on 6H-SiC(0001) substrates using the techniques of the present invention.

In order to solve the problem of uncontrollability of Schottky barrier height, it is only necessary to decrease the interface states density of the interface between an electrode metal and a semiconductor on which the electrode metal layer is formed. According to the present invention, a decrease in the interface states density is realized by decreasing the surface states density of the semiconductor before deposition of a metal thereon. The decrease in the surface states density can be realized primarily by flattening the surface of a semiconductor on an atomic level.

Flattening of the surface of a semiconductor results in a decrease in an atomic step density which generates dangling bond density which is a cause of surface states and in an amount of unstable atoms adsorbed on the surface of the semiconductor. According to the present invention, it has been found for the first time that flattening of the surface of a semiconductor on an atomic level decreases the surface states density of the semiconductor and that a decrease in the surface states density is effective for decreasing the interface states density of the electrode metal/semiconductor structure.

Recently, the technology of flattening the surface of semiconductors on an atomic level has developed rapidly and a variety of methods have been proposed. The present invention uses the newest known atomic level surface flattening

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technologies to demonstrate the above effect. However, the present invention should not be construed as being limited to specific atomic level surface flattening techniques. There have been known several important techniques for flattening surfaces of semiconductors on an atomic level, all of which have been proved useful in decreasing interface level density according to the present invention.

The present invention is based on a principle contrary to the conventional method in which particularly in the case of Ohmic contact, the desired Ohmic contact has been realized by intentionally decreasing ideality of interface, i.e., abruptness of structural connection.

Description will be made on how to flatten the surface of a semiconductor on an atomic level. An example of such a method is to set up conditions of oxidation appropriately so that oxidation can proceed flat on an atomic level, thus making the surface of the semiconductor after etching more flattened than the original surface.

Another method is a treatment with dilute hydrofluoric acid adjusted to have an appropriate pH. The pH of the solution can be rendered alkaline with ammonia water. Such a solution has an activity of flattening the surface of a semiconductor on an atomic level by means of a weak etching action of a lot of OH groups contained in the solution. Similarly, a semiconductor may be immersed in boiling water. This method can flatten the surface of a semiconductor on an atomic level by means of a weak etching action of deionized water.

High temperature heat treatment in hydrogen gas is also effective for flattening the surface of a semiconductor. Homoepitaxial growth can accelerate surface migration of atoms at relatively low growth rates to flatten the surface of crystal growth. As the last example, a method utilizing electromigration can also be used for flattening the surface of a semiconductor on an atomic level. Electromigration is a phenomenon in which upon application of electric current to a sample, surface atoms will migrate in a direction the same as or opposite to the direction in which electric current flows. Use of this method semiconductor surfaces can be flattened depending on the conditions. The present invention is not limited to the above-described specific methods. Instead, any method that can flatten semiconductor surfaces on an atomic level may be used similarly and will be effective for decreasing interface levels.

Hereinbelow, the idea of flattening semiconductor surfaces on an atomic level will be described in more detail. To be flat on an atomic level means existence of wide flat terraces when viewed on an atomic level. This directly indicates that an atomic step density is low in the surface concerned. Atoms at a step generally have more dangling bonds than atoms on a terrace. While the dangling bonds on a terrace will disappear after the formation of an interface with a metal due to bonding with the metal, the dangling bonds at a step will not disappear completely because of the step or difference in height as high as the thickness of one atomic layer. Therefore, after the formation of an interface, a main cause of generation of interface states is dangling bonds at steps. In other words, a decrease in a step density will result in a decrease in an interface level density. Hence, in order to decrease an interface states density, it is sufficient to flatten the surface of a semiconductor so that its step density can be decreased. Thus, even if the surface is not flattened when viewed on a scale on the order of micrometers, existence of wide terraces in more minute regions will suffice for decreasing interface states. Therefore, electrode structures with an interface having wide terraces on an atomic level, even though they have uneven or rough surfaces when viewed in a broader region, will cause a decrease in surface states density and, hence, fall within the scope of the present invention as defined below in appended claims.

If the interface states density is reduced enough by one of the above-described methods, the pinning of Fermi level will disappear. On such a pinning-free interface, what determines its potential barrier is merely a difference between respective Fermi levels, i.e., a difference between respective work functions, of the metal and the semiconductor. In this case, Schottky-Mott model expressed by equations (1) and (2) above is followed. Therefore, in the case of an n-type semiconductor, use of a metal having a high work function results in the formation of a Schottky barrier while use of a metal having a low work function gives rise to an Ohmic contact. To control the Schottky barrier height, it is only necessary to select an appropriate metal with regard to work function. For p-type semiconductors, the same idea as that for n-type semiconductors can be applied except that relationship of the magnitudes of the work functions should be reversed.

According to the present invention, the Schottky barrier height of a semiconductor can be expanded to a minimum value of 0 eV (cf. Fig. 2, region (I)) and a maximum value equivalent to the bandgap (cf. Fig. 2, region (II)).

Also, controlling the degree of pinning will in effect vary the Schottky height and, hence, controlling interface level density will enable the Schottky barrier height even when the same metal is used. That pinning can be controlled means that the Schottky barrier height can be controlled at will for each metal. As a result, the region where the Schottky barrier height can be controlled is expanded to regions (III) and (IV) in Fig. 2.

As described above, the present invention has made it possible to expand the region where the Schottky barrier height can appear from region (1) to regions (I) to (IV) in Fig. 2. Therefore, for a given metal, electrodes having the Schottky barrier heights within one of the regions (I) to (IV) also fall within the scope of the present invention. The present invention is generally applicable and operable regardless of the kind of metal and for all n-type and p-type semiconductor substrates, can be set up the regions (I) to (IV) as illustrated in Fig. 2 according to the present invention. Table 1 above indicates the Schottky barrier height regions of the present invention for representative semiconductor materials.

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Another important feature of the present invention is that control of Schottky/Ohmic property can be performed without heat treatment. However, if heat treatment is carried out after the deposition of electrode metals, still a flat interface can be obtained since originally a flat surface on an atomic level is provided, an interface reaction between the metal and the semiconductor occurs uniformly in the interface therebetween. Therefore, the present invention is also effective to electrodes which are subjected to heat treatment.

While not intended to be bound thereto, the present invention can be applied suitably to fabrication of electrodes on silicon carbide (SiC). While SiC is a material with which p- and n-type semiconductors can be used with ease, they have various excellent physical properties such as large a large bandgap. The present invention will be explained further taking SiC as an example. Since in the present invention, processes are used that do not involve heat treatment, no appreciable interface chemical reaction does occur between the metal and the semiconductor. Therefore, the resulting interface receives the conditions of the surface of the semiconductor without any change, and the interface has electrical characteristics which depend on structural and chemical properties of the surface of SiC before the deposition of the electrode metal. In other words, control of the conditions of the surface of SiC makes it possible to control electric properties freely.

When no treatment is performed on the surface of SiC, a natural oxide film is formed thereon. Also, a lot of water and/or impurity atoms are adsorbed on the SiC surface. Further, in the case of as ground surfaces, there are near the surface a lot of impurity atoms contaminating or defects induced upon grinding. Such conditions depend strongly on the process by which the SiC surface is fabricated so that the resulting surface does not always have the same surface atomic conditions and surface electronic state and then unstable.

In the present invention, a method is used which depends strongly on the conditions of surface atoms as described above. Therefore, such an unstable surface layer must be removed. For this purpose, SiC is oxidized and then the resulting oxide film is removed. The oxidation and removal of the oxide film may be performed simultaneously.

As a specific example of oxidation method for oxidizing silicon carbide (SiC), there can be used a method in which SiC is heated in an oxidizing gas atmosphere. The oxidation can be carried out at a heating temperature within the range of usually 800 to 1,250°C, preferably 950 to 1,150°C.

Concerning the selection of metals for use as an electrode material, a lot of metal materials with which Ohmic electrodes have not been realized by the conventional high temperature heat treatment can be used for forming Ohmic electrodes according to surface condition controlling technique in the fabrication method for fabricating electrodes on SiC according to the present invention. Properly speaking, a theoretical approach for realizing an Ohmic contact for n-type semiconductors is to use metal materials having a low work function. However, conventionally, Ohmic contacts were obtained by coarsening or roughening the interface by means of high temperature heat treatment to provide the interface with a non-ideal (non-uniform) structure and metal materials having a high work function which are difficult to oxidize were used in order to prevent the high temperature oxidation. On the contrary, in the present invention, heat treatment does not have to be done so that the interface is abrupt enough to be ideal one and then it is possible to realize an Ohmic contact for those metal materials which do not have high work function naturally. Here, metals which do not have high work functions are those metal materials composed mainly of elements other than noble metals (Ni, Pd, Pt, Cu, Ag, and Au) having high work functions, such as Ni which has been used conventionally. More specifically, a wide variety of metals can be used, including, for example, Mg, Ca, Sr, Ba, Sc, Y, La, Ti, Zr, Hf, V, Nb, Ta, Cr, Mn, Re, Fe, Al, Ga, In, Tl and the like. Among these, those metals having not so high an oxidizing capability, e.g., Ti and Al, are preferred.

In order to realize Ohmic contacts with p-type semiconductors, theoretically, metal materials having high work functions should be used. Conventionally, however, Ohmic contacts were formed by addition of impurities in high concentrations and, hence, aluminum (Al) has been used as an electrode metal because it can serve as a p-type impurity. However, Al has a low work function and is not suited as a metal for p-type metals. In the present invention, metals having high work functions are used. More specifically, metals which can be used for p-type semiconductors for forming Ohmic contacts include noble metals such as Ni, Pd, Pt, Cu, Ag, and Al and metals having approximately the same work function as the noble metals, such as Co, Rh, Ir, Ru, Os, and Re.

In the case of n-type SiC, if heat treatment is required after the formation of electrodes, a metal which is resistant to oxidation and has a high work function can be deposited on the above-described electrode metals having low work functions to prevent oxidation of the electrode portions. Similar effects can be obtained by depositing two or more metals having low work functions on a metal forming a metal semiconductor interface. Therefore, if heating is needed or desired, the above-described effect of the present invention cannot be deteriorated. What is important in the present invention is to use a metal having a low work function for an n-type SiC and a metal having a high work function for a p-type SiC. Practically, metals are divided into low and high work function metals when they have work functions up to 4.5 eV or higher than 4.5 eV. However, 4.5 eV is not a strict threshold value. This is because when a metal is deposited on SiC at ambient (room) temperature, e.g., about 20°C, mutual diffusion of the atoms constituting the metal and the atoms constituting the SiC semiconductor may occur on the metal/semiconductor interface and effective work function alters, if the metal used is highly reactive. So, 4.5 eV is to be understood to be a practical standard for classifying

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metals.

More specifically, the present invention comprises an oxidation process using an oxidative gas. Usually, a sample is placed in an oxidative atmosphere in an apparatus which enables heating of the sample, such as electric oven, and the sample is heated at a temperature within the range of 800 to 1,250°C. With this treatment, the surface of the sample becomes insulating due to formation of an oxide film thereon and a sufficient electric contact is not achieved. Then, the oxide film is removed with a reducing liquid or gas. It is often the case that the atoms on the surface of SiC are arranged or accumulate in a manner different from that the atoms in the bulk of the SiC. The oxidation process in an oxidative gaseous atmosphere is meant to oxidize such a denatured surface layer and make the surface layer ready to be removed by a liquid process including dissolving the surface oxide layer with a reducing liquid to remove it, or gaseous process involving reducing the surface oxide layer with a reducing gas to convert the oxide layer to a semiconductor of non-oxidized state.

In conventional processes for fabricating electrodes, immersion or dipping of a semiconductor in a dilute hydrofluoric acid has been conducted to remove spontaneous oxide film on the surface of SiC. However, no intentional or artificial oxidation of SiC has been performed so that the unstable surface layer has not been removed completely, thus failing to provide stable Ohmic contacts.

According to the present invention, development of Schottky and Ohmic electrodes, which has heretofore been made relying on experience or empirical rules, can be made in a shorter time than before since the present invention is based on a systematized knowledge. Thus, efforts for the development of electrodes can be minimized. The method for fabricating electrodes according to the present invention does not need heat treatment, which makes a great increase in stability of the electrode structure as compared with the conventional method in which heat treatment is essential. Further, In the case of fabricating Ohmic electrodes, conventional methods use doping semiconductors with impurities in high concentrations. In the present invention, however, high concentration doping is unnecessary so that Ohmic electrodes can be fabricated simply and conveniently. In contrast to the conventional methods in which leakage current in the Schottky barrier is used, the method for fabricating electrodes according to the present invention can reduce the Schottky barrier height to zero so that high performance Ohmic electrodes having theoretically no interface resistance that has not been achieved conventionally.

According to the present invention, Schottky barrier heights, that have been almost impossible to control by conventional methods, can be controlled freely by controlling interface level density and selecting work function of metals.

In practicing the present invention, it is only necessary to make the surface of a semiconductor as flat as possible on an atomic level. There are various kinds of known techniques for flattening the surface of a semiconductor on an atomic level and all such techniques can be used in the present invention. Therefore, there is no technical difficulty in practicing the present invention and the present invention can be applied to various metals and semiconductors simply and conveniently.

Hereinafter, the present invention will be described in greater detail by examples with reference to the attached drawings. However, the present invention should not be construed as being limited thereto.

EXAMPLE 1 Confirmation of Ohmic Property (SiC-Ti Structure)

In the instant example, vacuum sublimated n-type 6H-SiC was used as a semiconductor substrate immediately after it was ground. The substrate had a carrier density of about $1x10^{17}$ cm^{-3}. At this carrier density, usually, the semiconductor was not metallic and it was difficult to produce an Ohmic contact. The substrate was cleaned using methanol and trichloroethylene, and then placed in an electric oven filled with an oxygen gas atmosphere and oxidized at 300 °C for 30 minutes, followed by 800°C for 10 minutes. Thus an oxide film of about 5 nm thick was formed. The substrate was dipped in 5% hydrofluoric acid to remove the oxide film.

On the thus-obtained SiC substrate was deposited titanium (Ti), which is a representative high melting metal and has a low work function. The work function of Ti was 4.4 eV, which is by 0.9 eV lower than Ni, which has conventionally been used as an Ohmic electrode and has a work function of 5.3 eV. The SiC substrate used was not heated previously. The thickness of deposited film was about 500 nm. Deposition was not carried out on the entire surface of the semiconductor but through a metal mask formed with a round hole of 0.30 mm in diameter for subsequent electrical measurements.

Fig. 3 is a graph illustrating current-voltage (I-V) characteristics of the sample taken out of the vacuum apparatus (cf. line 3a). As apparent from Fig. 3, the line 3a is a straight line. Lack of nonlinearity as shown by the straight line 3a in Fig. 3 clearly indicates that the electrode obtained is Ohmic, that is, current is proportional to voltage. The interface resistance of the resulting electrode was $6.7x10^{-2}$ Ωcm^2. The electrode made of a SiC material having a low carrier density as low as $2x10^{17}$ cm^{-3} had an Ohmic contact which had theoretically the lowest resistance.

An electrode structure was fabricated in the same manner as in EXAMPLE 1 except that no oxidative etching was conducted but only dipping in 5% hydrofluoric acid was performed (COMPARATIVE EXAMPLE 1). The comparative electrode structure showed no Ohmic property but exhibited Schottky property (Fig. 4). In Fig. 4, curves 4a and 4b

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show normal and reverse direction leakage currents, respectively.

EXAMPLE 2 Confirmation of Ohmic Property (SiC-Al structure)

Next, an electrode structure was fabricated in the same manner as in EXAMPLE 1 except that instead of Ti was used aluminum (Al), which is a non-transient, low melting metal and belonging to the group (III) of the periodic table. In this case, too, was obtained an Ohmic contact similar to that fabricated in EXAMPLE 1. The work function of Al is 4.3 eV. Fig. 5 shows current-voltage characteristics of the aluminum electrode fabricated under the same conditions as the Ti electrode. Similarly to EXAMPLE 1, a line 5 representing the current-voltage characteristics of the Al electrode showed linearity and the interface resistance was about $1.4 \times 10^{-2}\ \Omega cm^2$. The electrode made of a SiC material having a low carrier density as low as $2 \times 10^{17}\ cm^{-3}$ had an Ohmic contact which had theoretically the lowest resistance.

What is common between EXAMPLE 1 and EXAMPLE 2 is that the both metals used have work functions by about 1 eV lower than those of noble metals used as electrode metal for SiC in the conventional methods. The both metals tested here exhibited effects which attain the objects of the present invention.

EXAMPLE 3 Confirmation of Ohmic Property (Si-Al structure)

The instant example is to show that the present invention is applicable to Si substrates and also realize Ohmic contacts. As a semiconductor substrate was used an n-type Si substrate having a carrier density of $7 \times 10^{16}\ cm^{-3}$. The substrate was cleaned using methanol and trichloroethylene, and then placed in an electric oven filled with an oxygen gas atmosphere and oxidized at 300°C for 30 minutes, followed by 800°C for 10 minutes. Thus an oxide film of about 50 nm thick was formed. The substrate was dipped in 5% hydrofluoric acid to remove the oxide film. The substrate thus obtained was dipped in hot water to make the surface of the semiconductor substrate flat on an atomic level. Thereafter, aluminum was deposited on the surface as an electrode metal. Fig. 6 illustrates current-voltage characteristics of the resulting electrode structure. A line 6a, which is a straight line, represents the sample with 5% hydrofluoric acid treatment. A line 6b, which is also a straight line, represents the sample with hot water treatment after 5% hydrofluoric acid treatment. A line 6c, which is also a straight line, represents the sample with 5% hydrofluoric acid treatment followed by hot water treatment. Here, by the term "hot water treatment" is meant a treatment with heated deionized water at a temperature below 100°C. From Fig. 6, it is apparent that the electrode fabricated according to the present invention has an Ohmic contact having a good linearity of current-voltage characteristics (the line 6c). Heretofore, as illustrated in Fig. 1, no metal could provide an Ohmic contact for Si substrates without high concentration doping. In fact, a comparative sample having an Si(111) substrate which did not subjected to high concentration doping and having a carrier density of $7 \times 10^{16}\ cm^{-3}$ (COMPARATIVE EXAMPLE 2) gave a Schottky barrier whose φbn was 0.69 eV after receiving the same 5% hydrofluoric acid treatment as in the instant example (Fig. 7). In Fig. 7, curves 7a and 7b denote current flows in normal and reverse directions, respectively. Comparing the lines 6a to 6c in Fig. 6, it is observed that according as flattening processes are added or flatness increases, current increases and contact resistance decreases. In the instant example (the line 6c in Fig. 6), the doping concentration was $7 \times 10^{16}\ cm^{-3}$, at which the width of the depletion layer is sufficiently thick and no tunneling will occur theoretically. Therefore, the Ohmic property observed in the sample of the instant example is considered to be attributable to a sufficiently decreased Schottky barrier.

EXAMPLE 4 Structural Uniformity of Electrode Structure

A Ti electrode was fabricated in the same manner as in EXAMPLE 1. Fig. 8A is an illustrative view prepared based on an optical micrograph of the surface of the Ti electrode. Fig. 8B is an expanded schematic cross sectional view showing the Ti electrode shown in Fig. 8A. As COMPARATIVE EXAMPLE 3, was prepared an Ni electrode by a conventional heat treatment method. The Ni electrode fabricated by cleaning using methanol and trichloroethylene, the same n-type SiC substrate as used in EXAMPLE 1, depositing Ni thereon by vapor deposition and then heating the substrate at 1,000°C for 60 minutes. Fig. 9A is an illustrative view prepared based on an optical micrograph of the surface of the Ni electrode. Fig. 9B is an expanded schematic cross sectional view showing the Ni electrode shown in Fig. 8A. In Figs. 8A and 9A, reference numeral 11 denotes an SiC substrate, 12 is an outline contour line of the electrode, 13 is an Ni electrode, and 14 is a Ti electrode. The both Ni and Ti electrodes were in the form of a disk of 0.3 mm in diameter. From Figs. 8A, 8B, 9A and 9B, it is apparent that the Ti electrode fabricated on SiC fabricated without heat treatment in accordance with the present invention has a high flatness in surface. The Ni electrode 13 shown in Fig. 9A has a rough surface, clearly lacking structural uniformity. In contrast, in the Ti electrode 14 of the present invention, no region is observed where surface conditions are different, and the area inside a contour line 12 of the electrode 14 is uniform in appearance and highly flat, thus presenting excellent structure for Ohmic structure. The electrode fabricated according to the method of the present invention (Fig. 8B) had a surface with an unevenness (X1) of 5 nm or

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less. On the contrary, the electrode fabricated by the conventional method (Fig. 9B) had a surface with an unevenness (X2) of about 200 nm. This clearly indicates that the electrode fabricated by the method of the present invention had a surface flatness much superior to the electrode fabricated by the conventional method.

EXAMPLE 5 Dependence on Atomic Level Flattening Treatment - Epitaxial Growth

The same SiC substrate immediately after grinding as used in EXAMPLE 1 was dipped in boiling water (100°C) for 10 minutes. On the other hand, a sample was prepared by homoepitaxially growing SiC on the same SiC substrate after grinding as used in EXAMPLE 1. The sample was dipped in boiling water (100°C) for 10 minutes. Then, difference in current-voltage characteristics between the epitaxial SiC substrate and the SiC substrate immediately after grinding were examined. In the case of the epitaxial SiC substrate, an expectation will be made that flattening in surface proceeds sufficiently so that the interface level density decreases and as a result, the Schottky barrier height decreased and Ohmic property increases. In fact, the SiC substrate immediately after grinding had an interface resistance of 1.2×10^{-2} Ωcm^2 (the line 3c in Fig. 3) while the epitaxial SiC substrate had an improved interface resistance of 6×10^{-3} Ωcm^2 (the line 3d in Fig. 3). From this it follows that epitaxial growth is effective for flattening on an atomic level the surface of a semiconductor and for decreasing interface level density of the semiconductor.

EXAMPLE 6 Dependence on Atomic Level Flattening Treatment - pH Adjusted Dilute Hydrofluoric Acid Treatment

An oxidized/etched substrate having a current-voltage characteristics represented by the line 3a in Fig. 3 as used in EXAMPLE 1 was dipped in a pH adjusted dilute hydrofluoric acid for 10 minutes. Then, a metal was deposited on the surface of the thus obtained substrate. In Fig. 3, the line 3b represents the current-voltage characteristics of the electrode sample. In this case, the dilute hydrofluoric acid was adjusted to pH 10. Comparison of the line 3b with the line 3a shows that the interface resistance is improved to 1.5×10^{-2} Ωcm^2. As demonstrated in the instant example, pH adjusted dilute hydrofluoric acid treatment is also effective in decreasing interface level density.

EXAMPLE 7 Fabrication of a Schottky Electrode Showing Less Leakage

Fig. 10 illustrates current-voltage characteristics of gold (Au) electrode on 6H-SiC(0001) face. Lines 10a, 10b and 10c show normal direction leakage currents and 10a', 10b' and 10c' show reverse direction leakage currents. In the case of SiC surface with usual 5% hydrofluoric acid treatment, the reverse direction leakage current was on the order of 10^{-7} A/cm^2 (line 10a'). When oxidation/etching treatment was conducted, the reverse direction leakage current was decreased to 10^{-19} A/cm^2 or less (line 10b'), thus showing a drastically improvement in leakage characteristics by 12 digits. Furthermore, with additional boiling water treatment, the reverse direction leakage current was further improved by 2 digits to 10^{-21} A/cm^2 (line 10c'). This indicates that oxidation/etching treatment and boiling water treatment which accelerate flattening of the surface of the semiconductor weaken the pinning of the Schottky barrier. To note, in the instant example, the electrode itself was subjected to no heat treatment. Therefore, the instant example clearly shows that high quality Schottky electrode can be fabricated without heat treatment of the electrode.

EXAMPLE 8 Control of Pinning and Schottky Barrier Height

Fig. 11 illustrate Schottky barrier height for various metals deposited on 6H-SiC(0001) face. The horizontal axis indicates work function of the metal. In the case of usual pretreatment with 5% hydrofluoric acid, the Schottky barrier height does not substantially depend on the work function of the metal and S factor which indicates an inclination of the line is about 0.2 (line 11a). Then, atomic level flattening of SiC was conducted by oxidation/etching treatment, S=0.8 was obtained, which indicates almost pinning free state (line 11b). Further, boiling water treatment gives rise to S=1.0, which indicates no pinning is observed (line 11c). Thus, the present invention realized pinning free state for those semiconductors which inherently show pinning. As a result, the Schottky barrier height can be freely changed merely by changing the work function of the metal as illustrated in Fig. 11 clearly. When the same metal is used, change in the process of atomic level flattening of the surface of the semiconductor results in varied Schottky barrier height. Note that for Ti electrodes, Schottky barrier heights were theoretically estimated from contact resistance values.

Fig. 12 illustrates Schottky barrier heights of Schottky electrodes fabricated on 6H-SC(0001) substrates by the conventional method and by the methods of the examples of the present invention. For strict comparison, conventional electrodes were fabricated on clean surfaces and I-V characteristics values measured at room temperature were used. The data of the conventional electrodes exist in the region (0). Ti, Mo and Au electrodes subjected to oxidation/etching treatment and boiling water treatment according to the present invention are plotted in regions (I), (IV) and (II), respectively. The data show that the present invention made it possible to realize Schottky barrier heights beyond the lower limit (region (I)) and beyond the upper limit (region (II) that were impossible to achieve by the conventional method.

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The Mo electrode plotted in region (IV) gives the same Schottky barrier height as that of the conventional Ti electrode having lower work function. This means that to give a certain Schottky barrier height, those metals that were considered inappropriate in view of pinning action can be used in the method of the present invention.

As described above, Schottky barrier height of semiconductors can be freely controlled according to the present invention.

Table 2 summarizes the results of examples and Comparative examples above.

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Table 2

	Substrate	Electrode Metal	Treatment	Figure	Interface Resistance ($10^{-2}\Omega cm^2$)	Reverse Direction Leakage Current (A/cm^2)	Surface Unevenness (nm)
Ex. 1	SiC	Ti	A+B	Fig. 3 Line (a)	6.7		
C.Ex.1	SiC	Ti	B	Fig. 4			
Ex. 2	SiC	Al	A+B	Fig. 5	1.4		
Ex. 3	Si	Al	A+B	Fig. 6 Line (a)			
	Si	Al	B+C	Fig. 6 Line (b)			
	Si	Al	A+B+C	Fig. 6 Line (c)			
C.Ex.2	Si	Al	B	Fig. 7			
Ex. 4	SiC	Ti	A+B	Fig. 8A, Fig. 8B			5≥
C.Ex.3	SiC	Ni	Cleaning* Heating 1,000°C	Fig. 9A, Fig. 9B			200

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Table 2 (Continued)

	Substrate	Electrode Metal	Treatment	Figure	Interface Resistance ($10^{-2}\Omega cm^2$)	Reverse Direction Leakage Current (A/cm^2)	Surface Unevenness (nm)
Ex. 5	SiC (Bulk)	Ti	A+B+C	Fig. 3 Line (c)	1.2		
	SiC-SiC (Epitaxial)	Ti	A+B+C	Fig. 3 Line (d)	0.6		
Ex. 6	SiC	Ti	A+B'	Fig. 3 Line (b)	1.5		
Ex. 7	6H-SiC (0001)	Au	A+B	Fig. 10		10^{-19}	
	6H-SiC (0001)	Au	A+B+C	Fig. 10		10^{-21}	
C.Ex.4	6H-SiC (0001)	Au	B	Fig. 10		10^{-7}	
Ex. 8	6H-SiC (0001)	Ti, Mo, Ni	A+B+C	Fig. 11			

*: with methanol and trichloroethylene

The present invention has been described in detail with respect to an embodiment, and it will now be apparent

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from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and it is the intention, therefore, in the appended claims to cover all such changes and modifications as fall within the true spirit of the invention.

Claims

1. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
   decreasing a surface states density of said surface of said semiconductor.

2. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
   controlling a Schottky barrier height of a rectifying Schottky electrode formed on said surface of said semiconductor.

3. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling flatness of an electrode metal/semiconductor interface.

4. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling a step density on an atomic level of an electrode metal/semiconductor interface.

5. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling selecting a work function of the metal.

6. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling the Schottky barrier height of the Schottky electrode under conditions without giving thermal hysteresis.

7. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:

   fabricating a Schottky electrode from a metal having a high work function, and fabricating an Ohmic electrode from a metal having a low work function, for an n-type semiconductor, or
   fabricating a Schottky electrode form a metal having a low work function and an Ohmic electrode from a metal having a high work function, for a p-type semiconductor.

8. The method as claimed in any one of claims 2 to 7, characterized by further comprising the step of heating.

9. A method of fabricating an Ohmic electrode, characterized by comprising the step of: forming flat electrode metal/semiconductor interface on an atomic level.

10. A method of fabricating an Ohmic electrode, characterized by comprising the step of: forming an electrode metal/semiconductor interface having a low step density on an atomic level.

11. A method of fabricating an electrode,
    characterized by comprising the step of:
    fabricating an Ohmic electrode as claimed in any one of claim 1 to 10 in a highly integrated electronic device.

12. The method as claimed in any one of claims 1 to 11, characterized in that said semiconductor is made of a semiconductor selected from the group consisting of Si and SiC.

13. The method as claimed in any one of claims 1 to 12, characterized in that said electrode metal is selected from the group consisting of Al, Au, Mo and Ti.

14. A Schottky electrode structure provided on a semiconductor characterized by having an interface portion which is flat on an atomic level.

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15. A Schottky electrode structure provided on a semiconductor characterized by having a Schottky barrier height which is impossible to realize by conventional method.

16. An Ohmic electrode structure provided on a semiconductor characterized by containing no high concentration impurity.

17. An Ohmic electrode structure characterized by having a Schottky barrier height which is substantially zero.

18. The electrode structure as claimed in any one of claims 14 to 17, characterized in that said semiconductor is made of a semiconductor selected from the group consisting of Si and SiC.

19. The electrode structure as claimed in any one of claims 14 to 17, characterized in that said electrode metal is selected from the group consisting of Al, Au, Mo and Ti.

20. A method of fabricating an electrode,
characterized by comprising the step of:
oxidizing a surface layer of silicon or silicon carbide and removing the resulting oxide film.

21. The method as claimed in claim 20, characterized in that said oxidizing of the silicon or silicon carbide is carried out by heating the silicon or silicon carbide in an oxidative gaseous atmosphere.

22. The method as claimed in claim 20, characterized in that said removing the oxide film is carried out by reacting the oxide film with a reducing liquid or gas.

23. The method as claimed in any one of claims 20 to 22, characterized in that said silicon or silicon carbide is n-type silicon or n-type silicon carbide, and wherein said electrode metal is a metal having a work function lower than that of noble metals.

24. The method as claimed in any one of claims 20 to 22, characterized in that said silicon carbide is p-type silicon carbide, and wherein said electrode material is a noble metal or a metal having a work function of a level substantially equal to that of noble metals.

25. The method as claimed in claim 23, characterized in that said electrode material is titanium (Ti).

26. The method as claimed in claim 23, characterized in that said electrode material is aluminum (Al).

27. A method of producing a Schottky diode or other semiconductor device having electrodes which includes fabricating electrodes by any method or combination of methods as claimed in any of claims 9 to 13 or 20 to 26 or which includes fabricating electrodes by patterning or fabricating in a pattern a layer of electrode metal produced by any method claimed in claims 1 to 8.

28. A semiconductor device having at least two metal electrodes formed on a semiconductor surface and wherein the flatness of the semiconductor surface is different at each interface with said two respective metal electrodes.

29. A device according to claim 28 wherein the electrodes are ohmic and Schottky electrodes respectively, and the interfaces therewith are atomically flat and other than atomically flat respectively.

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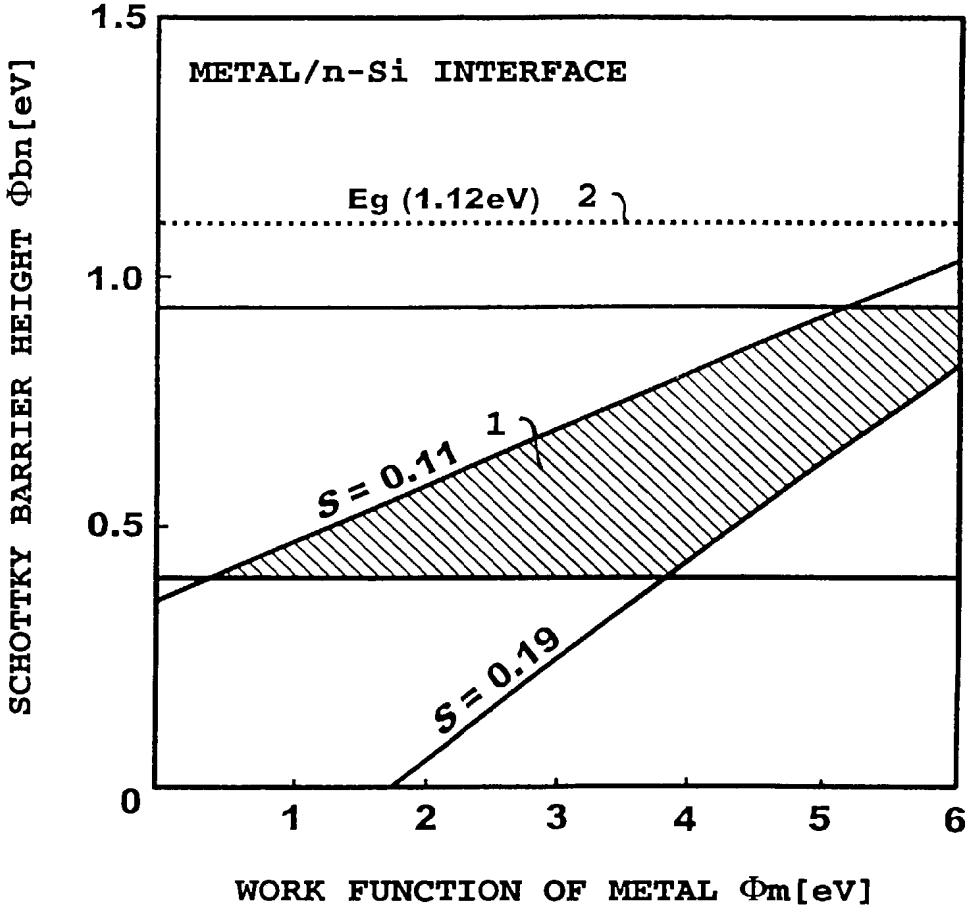


FIG. 1
(PRIOR ART)

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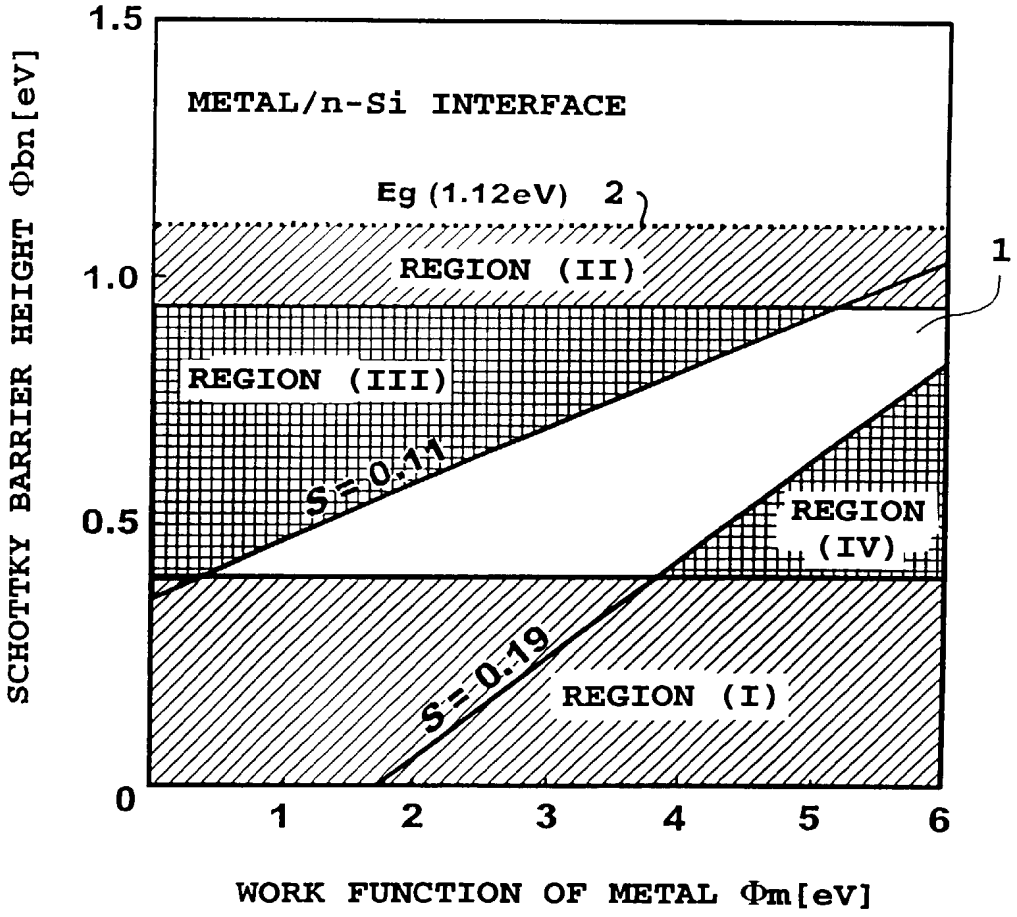


FIG.2

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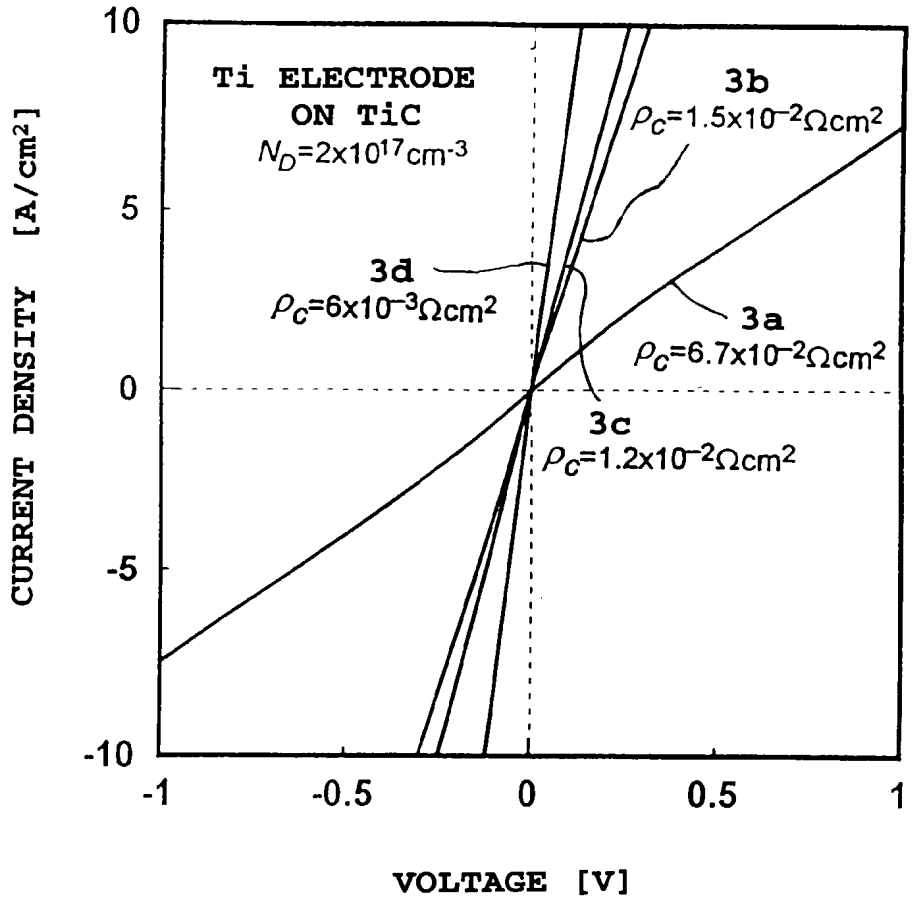


FIG.3

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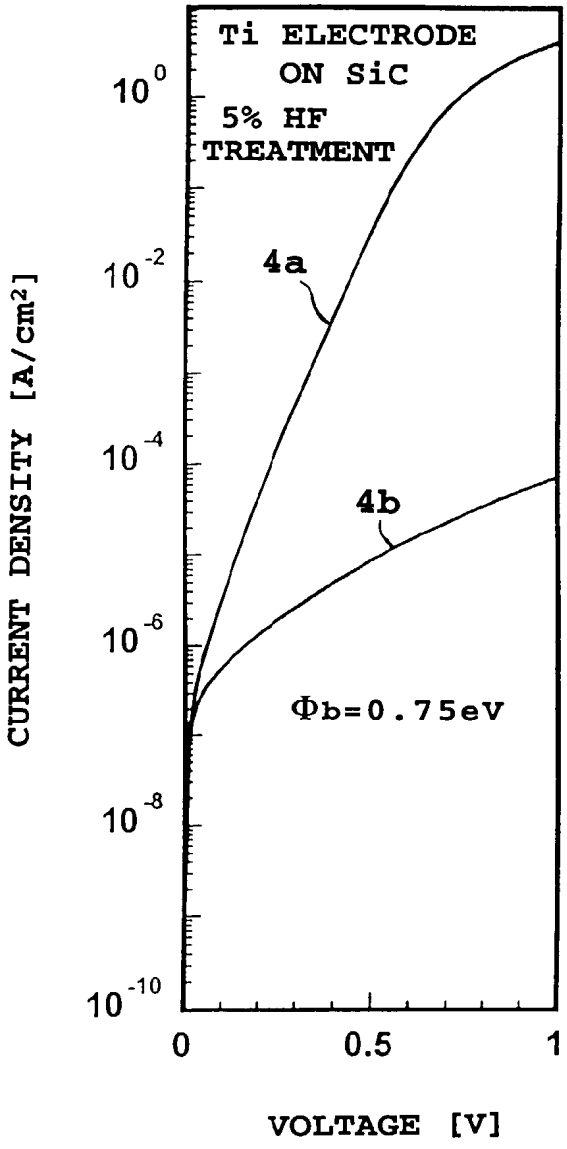


FIG.4

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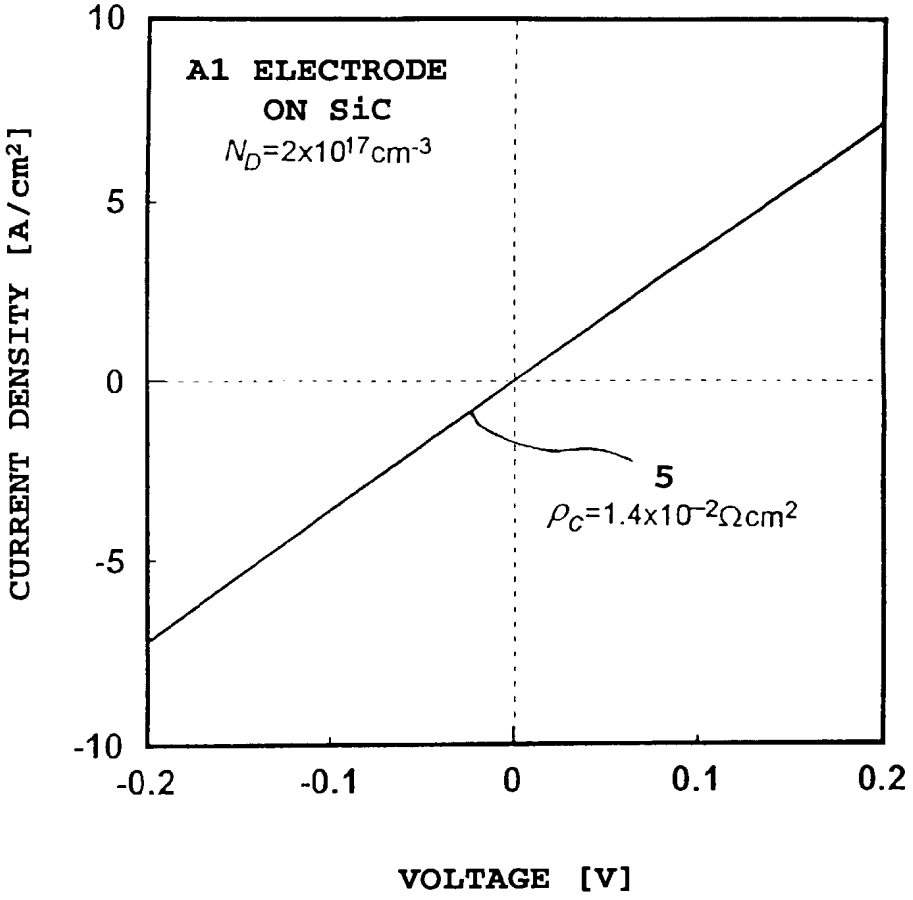


FIG.5

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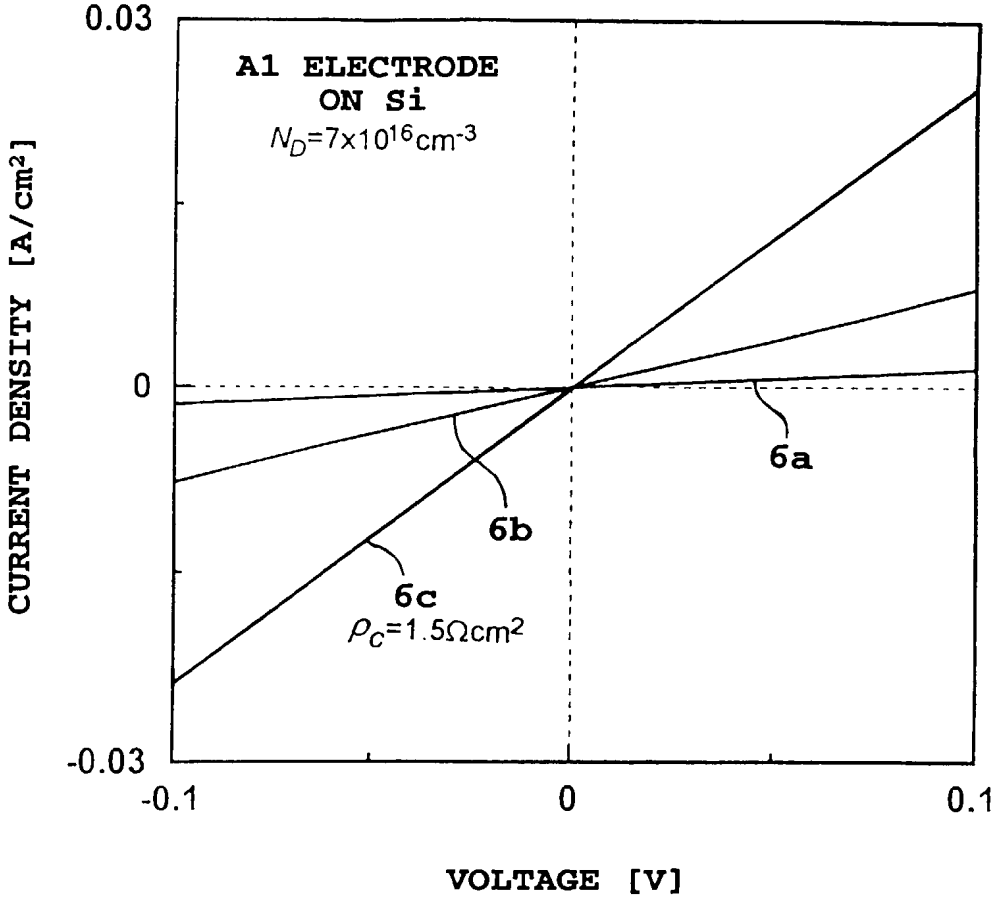


FIG.6

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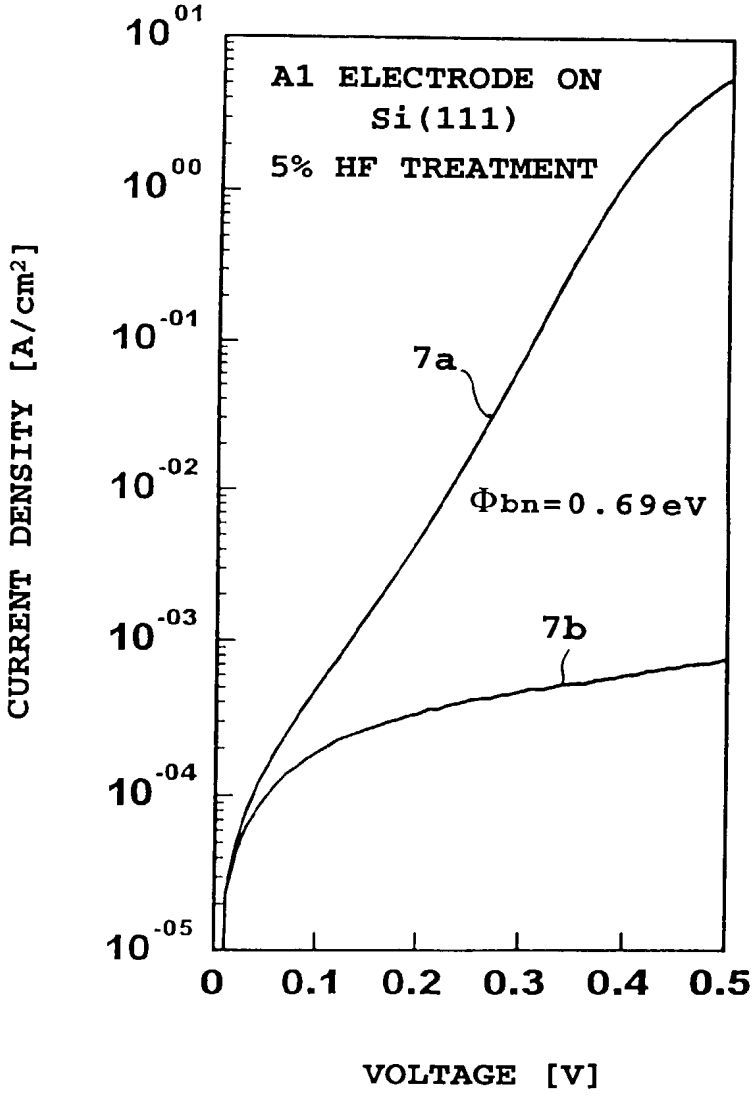


FIG.7

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FIG.8A

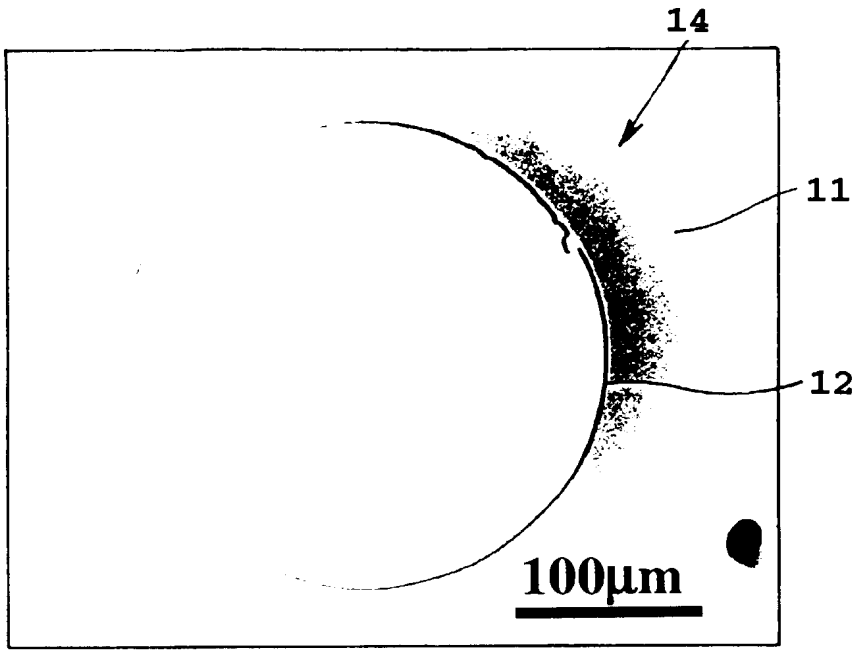
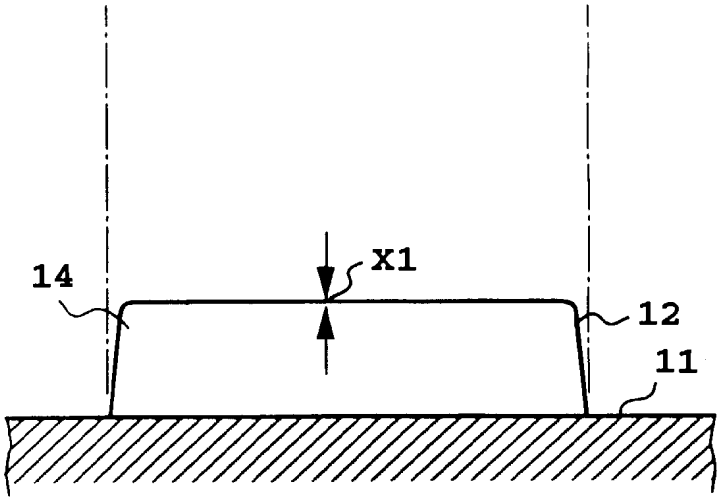


FIG.8B



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FIG.9A

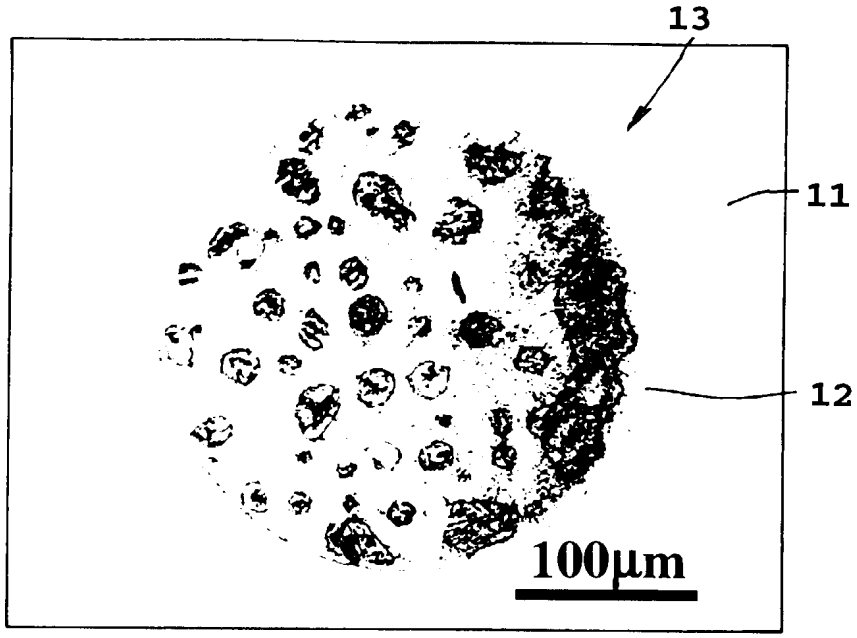
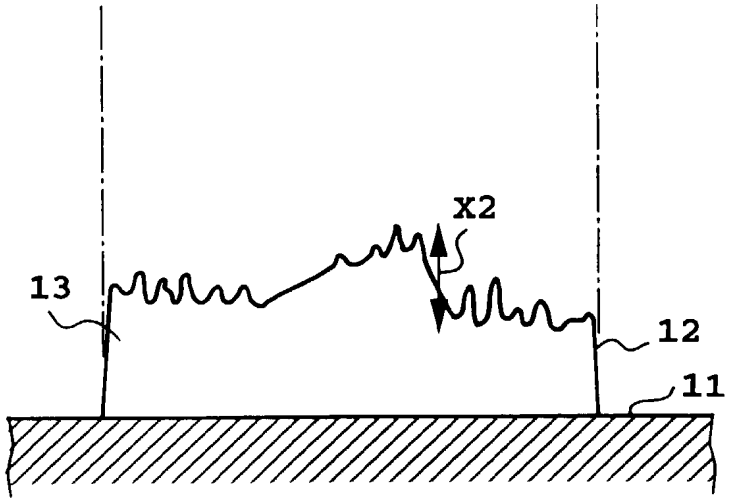


FIG.9B



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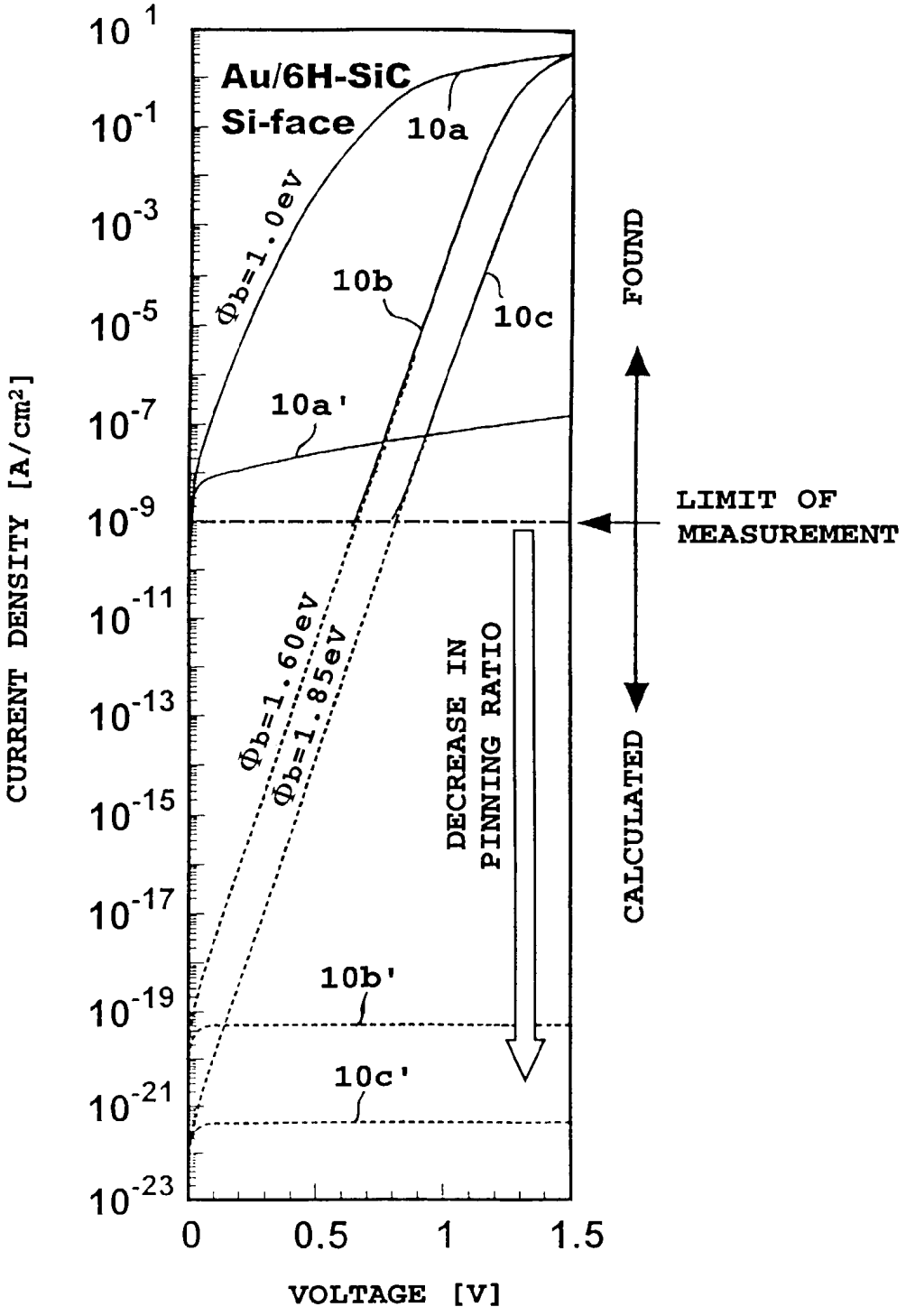


FIG.10

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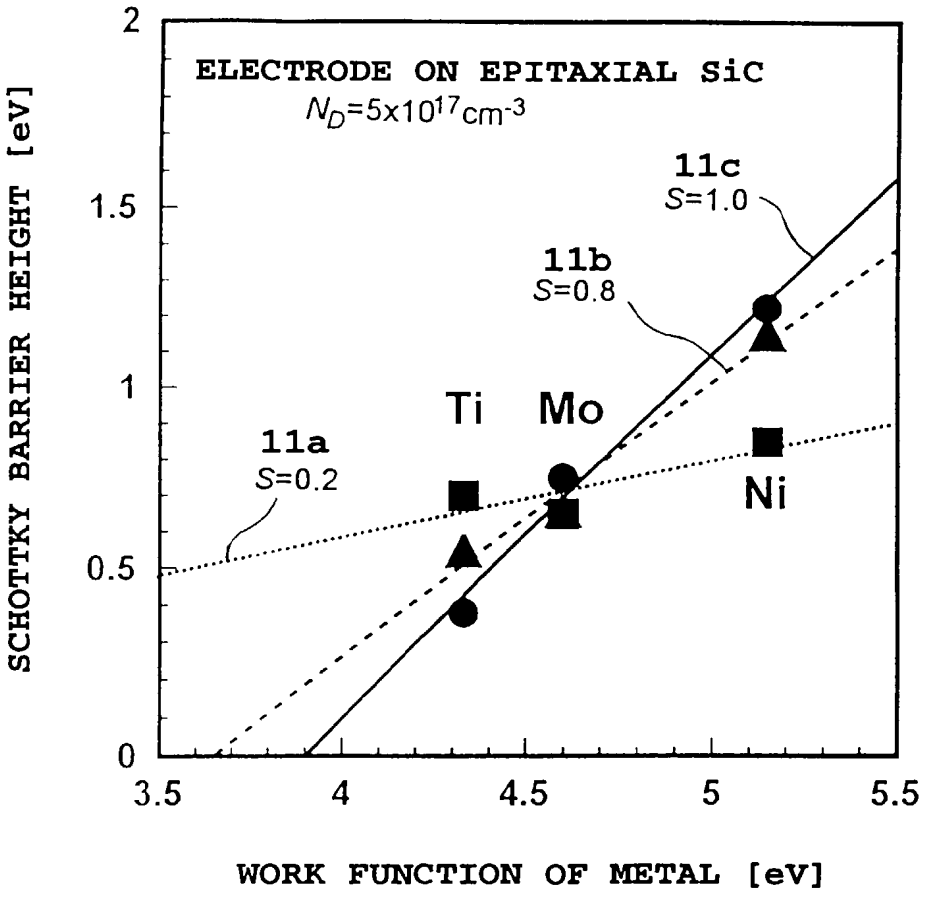


FIG.11

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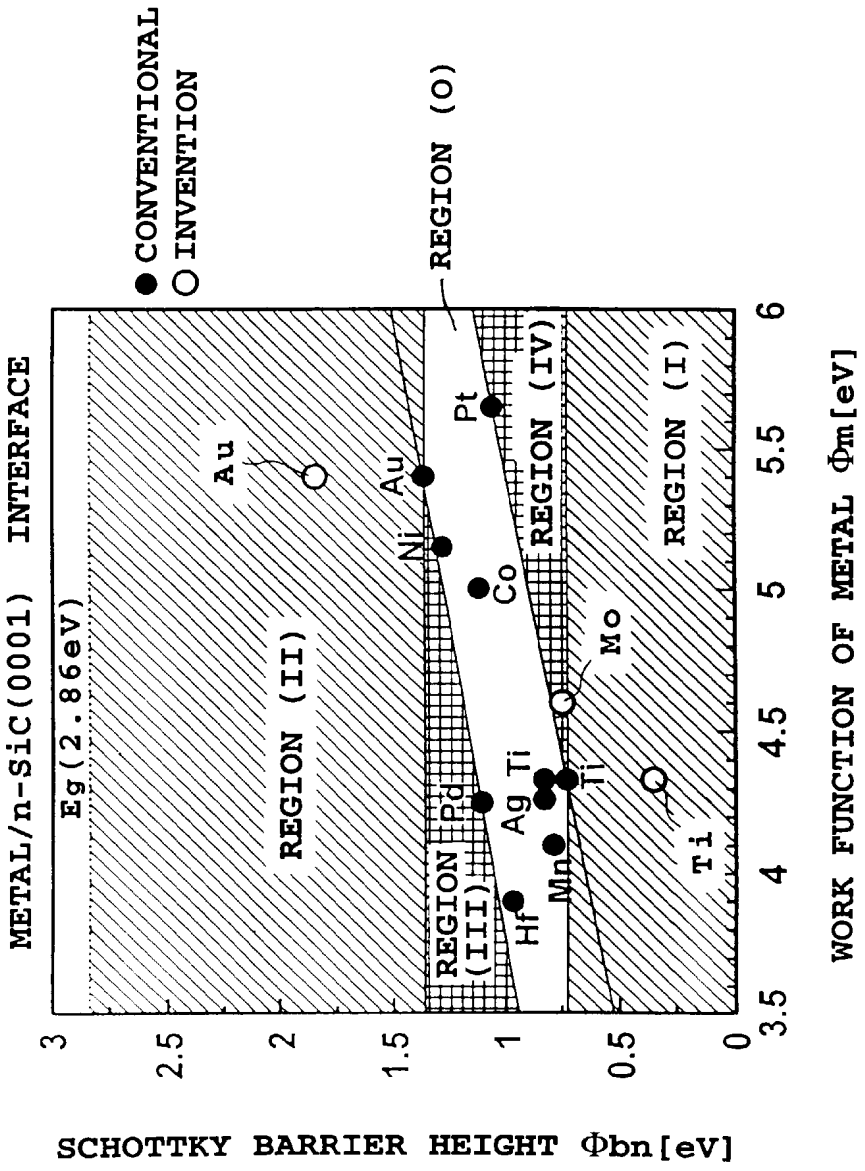


FIG.12

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(51)Int.Cl.[7]	識別記号	ＦＩ	
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21/3205		21/88	Ｒ
21/768		21/90	Ｃ

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(73)特許権者　000002185
ソニー株式会社
東京都品川区北品川６丁目７番35号
(72)発明者　角　博文
東京都品川区北品川６丁目７番35号　ソニー株式会社内
(74)代理人　100090376
弁理士　山口　邦夫　(外１名)

審査官　長谷山　健

最終頁に続く

(54)【発明の名称】　接続孔埋め込み形成方法

(57)【特許請求の範囲】

【請求項１】　シリコン基板の上方全面に形成された層間絶縁膜をパターニングして形成した接続孔に配線材料を埋め込む、接続孔埋め込み形成方法であって、
前記層間絶縁膜をパターニングして接続孔を形成した後に、前記接続孔にシリサイドを形成するための金属を、前記シリコン基板と前記シリサイドを形成するための金属とが反応する温度で堆積する工程を含むことを特徴とする接続孔埋め込み形成方法。

【請求項２】　前記シリサイドを形成するための金属が遷移金属であることを特徴とする請求項１に記載の接続孔埋め込み形成方法。

【請求項３】　前記遷移金属がコバルトであることを特徴とする請求項２に記載の接続孔埋め込み形成方法。

【請求項４】　シリコン基板の上方全面に形成された層間絶縁膜をパターニングして形成した接続孔に配線材料を埋め込む、接続孔埋め込み形成方法であって、
前記層間絶縁膜をパターニングして接続孔を形成した後に、前記接続孔にシリサイドを形成するための金属を、前記シリコン基板と前記シリサイドを形成するための金属とが反応する温度で堆積する工程と、
前記シリコン基板と反応していない金属を除去する工程と、
前記金属とシリコン基板との反応物質を安定化させるために高温熱処理を行う工程と、
前記接続孔内に前記シリサイドを形成するための金属を、前記シリコン基板と、前記シリサイドを形成するための金属とが反応する温度で堆積する工程を含むことを特徴とする接続孔埋め込み形成方法。

【請求項５】　シリコン基板の上方全面に形成された層

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間絶縁膜をパターニングして形成した接続孔に配線材料を埋め込む、接続孔埋め込み形成方法であって、
前記層間絶縁膜をパターニングして接続孔を形成した後に、該接続孔の底部に薄い酸化膜を形成する工程と、
前記接続孔にシリサイドを形成するための金属を、前記シリコン基板と前記シリサイドを形成するための金属とが反応する温度で堆積する工程を含むことを特徴とする接続孔埋め込み形成方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、半導体装置の製造方法に係り、特に微細接続孔埋め込み方法に関するものである。

【０００２】

【従来の技術】近年メモリー素子における集積度の大容量化につれ、素子の微細化が進んでいる。このために接続孔においても微細化の為に、接続孔へのメタル埋め込み技術が困難を増している。

【０００３】素子との接続を可能とするためには配線として用いているアルミニウム（Ａｌ）等の配線材料を埋め込む必要がある。その方法として、近年高温スパッタによりＡｌ埋め込み技術が注目されている。本方法は、シリコン（Ｓｉ）基板を数百度に高温加熱した状態でＡｌ合金をスパッタ成膜することにより、Ａｌをリフローさせ、Ａｌを接続孔内に充填し、かつ平坦化する技術である。この場合、Ａｌの下地として例えばＴｉなどのＡｌと反応し易い材料を用いると、成膜中のＡｌと下地Ｔｉとの界面反応の進行により、両者の間の濡れ性がよくなり、Ａｌが拡がった良好な埋め込みが行えることが知られている。

【０００４】上記接続孔内に、Ａｌを埋め込むにはＡｌと下地との良好な埋め込み特性、およびＡｌのシリコン基板への突き抜けの防止などが要求される。

【０００５】これらの要求に対して、従来以下に述べる様なＡｌの成膜構造がとられていた。

【０００６】（１）Ａｌの成膜構造がＡｌ／ＴｉＯＮ／Ｔｉ
これら三層は枚様式マルチチャンバースパッタ装置により真空中で連続成膜される。

【０００７】（２）Ａｌの成膜構造がＡｌ／Ｔｉ／ＴｉＯＮ／Ｔｉ
（３）Ａｌの成膜構造がＡｌ／Ｔｉ／ＴｉＮ／Ｔｉ
（４）ソース／ドレイン全面にＳＡＬＩＣＩＤＥ（Self aligned silicide）
でＳＩＴＯＸ（Silicidation through oxicide）－ＴｉＳｉ$_2$を形成した後に、その上層に層間絶縁膜および接続孔を形成しＡｌを成膜する。

【０００８】これらの従来の接続孔の埋め込み技術のうち（４）の場合についてＭＯＳトランジスタの製造を例にとり、以下に説明する。

【０００９】図９および図１０はＭＯＳトランジスタ製造工程断面図である。

【００１０】以下工程順に説明する。

【００１１】（１）図９（ａ）に示す様にシリコン基板１に素子間分離のためのフィールド酸化膜２を形成する。

【００１２】（２）ゲート酸化を行い多結晶シリコン及びＷＳｉ$_2$を堆積し、パターニングを行うと図９（ｂ）に示す様にゲート酸化膜４およびゲート電極３が形成される。次にＬＤＤ（Lightly doped drain）イオン注入を行い、ＬＤＤ拡散層５を形成する。

【００１３】（３）シリコン基板１の全面に酸化膜を形成した後に、全面エッチバックを行い、図９（ｃ）に示す様にサイドウォール１８を形成する。

【００１４】次にソース／ドレイン領域を形成するために図９（ｃ）に示す様にシリコン基板１の全面にイオン注入６を行い、図１０（ａ）に示す様に拡散層８を形成する。

【００１５】（４）シリコン基板１の全面に薄い酸化膜を形成する。

【００１６】次にＴｉを全面に堆積した後に、熱処理でソースおよびドレイン領域上に図１０（ａ）に示す様にＳＩＴＯＸ－ＴｉＳｉ$_2$２１を形成する。

【００１７】次に酸化膜上の未反応のＴｉを選択的にエッチングする。

【００１８】（５）シリコン基板１の上方全面に層間絶縁膜を形成し、レジストパターニングを行い、ドライエッチングにより、図１０（ｂ）に示す様に層間絶縁膜７ａおよび接続孔１５を形成する。

【００１９】（６）Ｔｉ１３を全面に堆積した後に、Ａｌを全面に形成する。

【００２０】次にレジストパターニングを行い、ドライエッチングにより図１０（ｃ）に示す様に、Ａｌ配線１２を形成する。

【００２１】

【発明が解決しようとする課題】しかしながら、上記従来のいずれの接続孔埋め込み技術にも以下の様な問題があった。

【００２２】（１）Ａｌの成膜構造がＡｌ／ＴｉＯＮ／Ｔｉの場合
ＡｌとＴｉＯＮとがお互いに反応しにくく、両者の濡れ性が悪くＡｌの埋め込み特性が極端に悪くなる。

【００２３】（２）Ａｌの成膜構造がＡｌ／Ｔｉ／ＴｉＯＮ／Ｔｉの場合
ＡｌがＴｉＯＮの上に直接接触する（１）の場合よりも埋め込み特性が改善されるが、Ｔｉ単層の場合程には改善されない。それはＡｌ成膜時シリコン基板が数百度に加熱された際にＴｉＯＮ中の酸素は上層Ｔｉ膜中に拡散し、とりわけＴｉ膜の薄い接続孔側壁の下部等ではＴｉ表面にまでこの酸素が達し、この部分のＴｉが酸化さ

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れ、Ａｌとの反応が劣下し、埋め込み特性が悪くなるからである。

【００２４】（３）Ａｌの成膜構造がＡｌ／Ｔｉ／ＴｉＮ／Ｔｉの場合

ＡｌのバリアメタルとしてＴｉＯＮの代わりにＴｉＮを用いると埋め込み不良の問題は解決されるが、ＴｉＮはＴｉＯＮに比べてＡｌのバリア性が不十分であり、高温スパッタもしくはＡｌシンター等の加熱プロセスによりＡｌの突き抜けが起こる。

【００２５】（４）ソース／ドレイン全面にＳＡＬＩＣＩＤＥでＳＩＴＯＸ－ＴｉＳｉ$_2$２１を形成するため、図１０（ａ）に示した様に、このＳＩＴＯＸ－ＴｉＳｉ$_2$２１がフィールド酸化膜２に接触してしまう。しかしＴｉＳｉ$_2$にはテンシルのストレスがあり、そのためにフィールド酸化膜２のエッジ部のシリコン基板１に結晶欠陥を誘発してしまい、シリコン拡散層では接合リークを通常より１桁増大させる。

【００２６】そこで本発明は、アルミニウム等の電極材料に対し、バリア特性を有して、しかも埋め込み特性の良好な接続孔埋め込み形成方法を提供することを目的とする。

【００２７】

【課題を解決するための手段】上記課題は本発明によれば、シリコン基板の上方全面に形成された層間絶縁膜をパターニングして形成した接続孔に配線材料を埋め込む、接続孔埋め込み形成方法であって、前記層間絶縁膜をパターニングして接続孔を形成した後に、前記接続孔にシリサイドを形成するための金属を、前記シリコン基板と前記シリサイドを形成するための金属とが反応する温度で堆積する工程を含むことを特徴とする接続孔埋め込み形成方法によって解決される。

【００２８】また上記課題は本発明によれば、前記金属が遷移金属であることを特徴とする接続孔埋め込み形成方法によって好適に解決される。更に上記遷移金属がコバルトであることを特徴とする埋め込み形成方法によって好適に解決される。

【００２９】また上記課題は本発明によれば、シリコン基板の上方全面に形成された層間絶縁膜をパターニングして形成した接続孔に配線材料を埋め込む、接続孔埋め込み形成方法であって、前記層間絶縁膜をパターニングして接続孔を形成した後に、前記接続孔にシリサイドを形成するための金属を、前記シリコン基板と前記シリサイドを形成するための金属とが反応する温度で堆積する工程と、前記シリコン基板と反応していない金属を除去する工程と、前記金属とシリコン基板との反応物質を安定化させるために高温熱処理を行う工程と、前記接続孔内に前記シリサイドを形成するための金属を、前記シリコン基板とシリサイドを形成するための金属と反応する温度で堆積する工程を含むことを特徴とする接続孔埋め込み形成方法によって解決される。

【００３０】また上記課題は本発明によれば、シリコン基板の上方全面に形成された層間絶縁膜をパターニングして形成した接続孔に配線材料を埋め込む、接続孔埋め込み形成方法であって、前記層間絶縁膜をパターニングして接続孔を形成した後に、該接続孔の底部に薄い酸化膜を形成する工程と、前記接続孔にシリサイドと形成するための金属を、前記シリコン基板と前記シリサイドを形成するための金属とが反応する温度で堆積する工程を含むことを特徴とする接続孔埋め込み形成方法によって解決される。

【００３１】また上記課題は本発明によれば、前記酸化膜をシリコン酸化膜またはシリコン酸化窒化膜とし、その膜厚を１０ｎｍ以下とし、前記シリサイドを形成するための金属をチタンとし、前記接続孔内に金属を堆積する温度を６００℃以上で堆積することを特徴とする接続孔埋め込み形成方法によって好適に解決される。

【００３２】

【００３３】

【作用】本発明によれば、図８に示す様に層間絶縁膜をパターニングして接続孔１５を形成した後に、この接続孔１５にシリコン基板１とシリサイドを形成するための金属の堆積を、シリコン基板１とこの金属とが反応する温度で行うことにより、金属原子はシリコン（Ｓｉ）と反応しようとするためにシリコン方向に活発に拡散し、Ｓｉと反応してシリサイドを形成することが出来る。その結果、金属の堆積表面においては、この金属原子の拡散により平坦な面を形成し、接続孔１５の底部のシリコン基板１とのカバレージを向上させることが出来る。しかもシリサイドを接続孔１５の底部のみに形成しているので、フィールド酸化膜のエッジ部のシリコンの結晶欠陥を防止することが出来る。

【００３４】また本発明によれば、上記金属を遷移金属とすると、この遷移金属が、シリコンと反応するため拡散する主な原子（move spieces）となるので、遷移金属は接続孔１５内で拡散がより活発になり、接続孔１５内における金属堆積表面を好適に平坦化させることが出来る。

【００３５】また本発明によれば、図４（ｂ）に示す様に接続孔１５内に金属を、シリコン基板１と金属とが反応する温度で堆積すると、シリコン基板１とこの金属との反応物質（シリサイド）の上層に、未反応の金属が堆積するので、この未反応の金属のみを選択的に除去することが出来る。その結果、接続孔１５の堆積表面をより平坦化することが出来る。また、未反応金属のみを除去した後更に、高温処理を行うことにより上記シリサイドを安定化することが出来る。

【００３６】更に、この平坦なシリサイド上に上記金属をシリコン基板１と反応する温度で接続孔１５内に堆積させることにより、堆積した金属が活発に拡散しシリコンと反応するので堆積表面を好適に平坦化することが出

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来る。

【００３７】本発明によれば、図２（ｃ）に示す様に接続孔１５の底部に薄い酸化膜９を形成した後に、図３（ａ）に示す接続孔１５内に金属を、シリコン基板１と金属とが反応する温度で堆積することにより、酸化膜、金属、シリコンとの反応物質であるＳＩＴＯＸ（Silicidation through oxicide）－シリサイドを形成することが出来る。この反応物質はアルミニウム等の電極形成時のバリア性を有し、しかもシート抵抗の低い好適な電極の下地を形成する。

【００３８】また本発明によれば、上記薄い酸化膜をシリコン酸化膜あるいはシリコン酸化窒化膜とし、堆積する金属をチタン（Ｔｉ）とすることにより、ＳＩＴＯＸ－ＴｉＳｉ$_2$が形成される。このＳＩＴＯＸ－ＴｉＳｉ$_2$はシート抵抗は１０Ω以下の低抵抗で、しかも５００℃の温度までアルミニウムに対してバリア性を有し、好適な電極の下地材料を形成する。

【００３９】また本発明によれば、図５（ｂ）に示す様に接続孔１５の底部及び側壁部にシリコン窒化膜（ＳｉＮ）１４を形成した後に、接続孔１５内に金属の堆積をシリコン基板１と金属とが反応する温度で行う際に、接続孔の側壁部において、金属とシリコンの酸化膜である層間絶縁膜７ａとの間にはシリコン窒化膜１４が介在しているので金属の酸化を減少させることが出来る。その結果、アルミニウム等の電極との埋め込み特性を向上させることが出来る。

【００４０】

【実施例】以下本発明による実施例を図面に基づいて詳細に説明する。

【００４１】図１～図３は本発明による第１実施例を示すＭＯＳトランジスタ製造工程断面図である。

【００４２】以下、第１実施例を工程順に説明する。

【００４３】（１）図１（ａ）に示す様にシリコン基板１に素子間分離のためのフィールド酸化膜２を形成する。

【００４４】（２）ゲート用の酸化を行う。

条件　ガス　H_2／O_2＝６／４リットル／分，温度　８５０℃，膜厚　１６ｎｍ次に多結晶シリコンを全面に堆積する。

条件　ガス　SiH_4／PH_3／H_2＝５００／０．３５／５０ｓｃｃｍ，温度　５８０℃，圧力　７９．８Ｐａ，膜厚　２００ｎｍ

次にＷＳｉ$_2$を全面に堆積する。

条件　WF_6／SiH_4／Ｈｅ＝１０／１０００／３６０ｓｃｃｍ，温度　３６０℃，圧力　２６．６Ｐａ，膜厚　１００ｎｍ

次にレジストパターニングを行いドライエッチングでゲート配線部を形成する。

条件　ガス　$C_2Cl_3F_3$／SF_6＝６５／５ｓｃｃｍ，圧力　１．３３Ｐａ，マイクロ波パワー　１００Ｗ,ＲＦパワー　１００Ｗ

このようにして図１（ｂ）に示す様にゲート酸化膜４、ゲート電極３を形成する。

【００４５】次にＬＤＤイオン（ＡｓまたはBF_2）注入を行い、ＬＤＤ拡散層５を形成する。

【００４６】（３）シリコン基板１の全面に酸化膜を形成した後に、全面エッチバックを行い、図１（ｃ）に示す様にサイドウォール１８を形成する。

【００４７】次にソース／ドレイン領域を形成するために図１（ｃ）に示す様にシリコン基板１の全面にイオン注入６を行い、図２（ａ）に示す様に拡散層８を形成する。

ＮＭＯＳの場合、Ａｓ　５０ＫｅＶ，５ｅ１５／ｃｍ^2、ＰＭＯＳの場合、BF_2　２０ＫｅＶ，３ｅ１５／ｃｍ^{2}の条件で行う。

【００４８】（４）図２（ａ）に示す様にシリコン基板１の全面に層間絶縁膜７を形成する。

条件　ガス流量　SiH_4／O_2／N_2＝２５０／２５０／１００ｓｃｃｍ，温度　４２０℃，圧力　１３．３Ｐａ，膜厚　５００ｎｍ

さらに１１００℃１０秒の活性化アニールを行う。

【００４９】（５）レジストパターニングを行い、ドライエッチでパターニングし図２（ｂ）に示す様に接続孔１５を形成する。

条件　ガス　C_4F_8＝５０ｓｃｃｍ，ＲＦパワー　１２００Ｗ，圧力　２Ｐａ

【００５０】（６）図２（ｃ）に示す様に接続孔１５の底部に薄い酸化膜９を形成する。

条件　ガス　H_2O／O_2＝１．５／６　１／ｍｉｎ，　温度　８５０℃，膜厚　３ｎｍ

【００５１】（７）図３（ａ）に示す様に接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＴｉ１０を形成する。この時シリコン基板１の温度を６００℃程度にまで上昇させる。

Ｔｉスパッタ条件例　Ａｒ＝４０ｓｃｃｍ，圧力　０．０４Ｐａ，スパッタパワー　１ＫＷ，膜厚　３０ｎｍ

これによりスパッタリングする金属原子は下地Ｓｉと次々に反応するため接続孔１５内に拡散する。原子は接続孔１５内に流動するためにＴｉ１０のカバレージもオーバーハング形状にならず、接続孔１５に均一に形成できる。

【００５２】さらに、接続孔１５内のＳｉと接しているＴｉ１０はシリサイドを形成しているために接続孔１５内のシート抵抗は１０Ω以下の低抵抗を保つ。その後のＡｌ配線とのコンタクト抵抗も１０Ω以下の低抵抗となる。さらに形成するシリサイドはＳＩＴＯＸ－ＴｉＳｉ

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$_2$１１であるので、５００℃の温度までＡｌに対してバリヤ性を有する。

Ａｌスパッタ条件例　Ａｒ流量　４０ｓｃｃｍ，圧力　０．０４Ｐａ，
スパッタパワーＤＣ　１ＫＷ，膜厚　５００ｎｍ

次にレジストパターニングを行い、上記Ａｌのドライエッチングを行い、図３（ｂ）に示す様にしてＡｌ配線１

条件例は、ＲＦ印加型ＥＣＲエッチャーを使用、
ガス流量　BCl_3／Cl_2＝６０／９０ｓｃｃｍ，マイクロ波パワー
１００Ｗ，ＲＦパワー　５０Ｗ，圧力　２１．３Ｐａ

上記工程を経て本第１実施例によるＭＯＳトランジスタが製造される。

【００５４】図４は第２実施例を示すＭＯＳトランジスタ製造後半工程断面図である。

【００５５】本実施例は第１実施例で示した図３（ａ）の工程における、ＳＩＴＯＸ－ＴｉSi_2の形成時の未反応Ｔｉを選択的に除去する。その後に安定したＴｉSi_2を形成するために９００℃程度の高温アニールを施す。そしてＡｌ配線を埋め込むために新たにＴｉを堆積

Ｔｉスパッタ条件例　Ａｒ＝４０ｓｃｃｍ，圧力　０．０４Ｐａ，
ＲＦバイアス　５０Ｗ，スパッタパワー　１ＫＷ，
膜厚　３０ｎｍ

これによってスパッタリングする金属原子は下地Ｓｉと次々に反応するために接続孔１５内に拡散する。原子は接続孔１５内に流動するために接続孔１５の底部に均一にＴｉ原子を供給できる。結果として、安定した膜厚のＴｉシリサイドを形成できる。

【００５８】（８）図４（ｂ）に示す様に層間絶縁膜７ａおよびＳＩＴＯＸ－Ｔｉ$Si_2$１１上の未反応のＴｉ１０を選択的にエッチングする。

条件例　NH_4OH：H_2O_2：H_2O＝１：２：２溶液に１０分間浸す。

【００５９】次に安定したＴｉSi_2を形成するために９００℃，３０秒程度の熱処理を行う。

Ｔｉスパッタ条件例　Ａｒ＝４０ｓｃｃｍ，圧力　０．０４Ｐａ，
ＲＦバイアス　５０Ｗ，スパッタパワー　１ＫＷ，
膜厚　３０ｎｍ

次に接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＡｌを形成する。

Ａｌスパッタ条件例　Ａｒ流量　４０ｓｃｃｍ，圧力　０．０４Ｐａ，
スパッタパワーＤＣ　１ＫＷ，膜厚　５００ｎｍ

次にレジストパターニングを行い、上記Ａｌのドライエッチングを行い図４（ｃ）に示す様にしてＡｌ配線１２

条件例は、ＲＦ印加型ＥＣＲエッチャーを使用、
ガス流量　BCl_3／Cl_2＝６０／９０ｓｃｃｍ，
マイクロ波パワー　１０００Ｗ，ＲＦパワー　５０Ｗ，
圧力　２１．３Ｐａ

上記工程を経て本第２実施例によるＭＯＳトランジスタが製造される。

【００６２】次に図５および図６は第３実施例を示すＭＯＳトランジスタ製造後半工程断面図である。

【００６３】本実施例は接続孔側部のSiO_2上にＳｉ

【００５３】（８）接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＡｌを形成する。

２を形成する。

【００５６】本実施例は、まず第１実施例で示した（１）～（６）の工程を経てシリコン基板１に層間絶縁膜をパターニングし接続孔１５およびこの接続孔１５の表面に薄い酸化膜を形成する。

【００５７】（７）図４（ａ）に示す様に接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＴｉ１０を形成する。この時シリコン基板１の温度を６００℃程度まで上昇させる。

【００６０】接続孔１５内はシリサイドを形成しているために接続孔１５内のシート抵抗は１０Ω以下の低抵抗を保つ。その後のＡｌ配線とのコンタクト抵抗も１０Ω以下の低抵抗となる。さらに形成するシリサイドはＳＩＴＯＸ－Ｔｉ$Si_2$１１であるので、５００℃の温度までＡｌに対してバリヤ性を有する。

【００６１】（９）図４（ｃ）に示す様に接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＴｉ１３を形成する。この場合もあらかじめ形成したＴｉSi_2を通して、ＴｉとＳｉを反応させることによりＴｉのカバレージを稼ぐため、Ｔｉ成膜時に６００℃程度の加熱しながら堆積を行う。

１の全面にＡｌを形成する。

を形成する。

Ｎを形成させることにより、その後成膜するＴｉの酸化を抑える方法である。以下本実施例の工程を説明する。

【００６４】本実施例は、まず第１実施例で示した（１）～（５）までの工程を経てシリコン基板１上に層間絶縁膜をパターニングし接続孔１５を形成する。

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【００６５】（６）図５（ａ）に示す様に接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＳｉＮ１４を形成する。

条件例　ガス　SiH_4／NH_3／N_2＝１８０／５００／７２０ｓｃｃｍ，
温度　２５０℃，圧力　４０Ｐａ，膜厚　１００ｎｍ

【００６６】（７）図５（ｂ）に示す様にＳｉＮ１４をエッチバックして層間絶縁膜７ａの側壁にＳｉＮ１４ａを形成する。次にＳｉＮ１４ａを有した接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＴｉ１０を形成する。

条件例　ガス　CHF_3＝５０ｓｃｃｍ，ＲＦパワー　１５０Ｗ，圧力　２Ｐａ
Ｔｉスパッタ条件例　Ａｒ流量　４０ｓｃｃｍ，圧力　０．０４Ｐａ，
スパッタパワーＤＣ　１ＫＷ，膜厚　５００ｎｍ

【００６７】（８）図５（ｃ）に示す様に未反応Ｔｉを選択的にエッチする。

条件例　NH_4OH：H_2O_2：H_2O＝１：２：２溶液に１０分間浸す。

【００６８】その後、安定したＴｉSi_2を形成するために９００℃，３０秒程度の熱処理を加える。

【００６９】（９）図６に示す様に接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＴｉ１３を堆積させる。この場合もあらかじめ形成したＴｉSi_2を通して、ＴｉとＳｉを反応させることによりＴｉのカバレージを稼ぐため、Ｔｉ成膜時に６００℃程度の加熱をしながら堆積を行う。

Ｔｉスパッタ条件例　Ａｒ＝４０ｓｃｃｍ，圧力　０．０４Ｐａ，
ＲＦバイアス　５０Ｗ，スパッタパワー　１ＫＷ，
膜厚　３０ｎｍ

次に接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＡｌを形成する。次にレジストパターニングを行い、次いでメタル配線膜のドライエッチを行いＡｌ配線１２を作りトランジスタを形成する。

条件例は、ＲＦ印加型ＥＣＲエッチャーを使用、
ガス流量　BCl_3／Cl_2＝６０／９０ｓｃｃｍ，
マイクロ波パワー　１０００Ｗ，ＲＦパワー　５０Ｗ，
圧力　２１．３Ｐａ

上記工程を経て本実施例によるＭＯＳトランジスタが製造される。

【００７０】次にレジストパターニングを行い、次いでメタル配線膜のドライエッチを行いＡｌ配線１２を作りトランジスタを形成する。条件例は、ＲＦ印加型ＥＣＲエッチャーを使用、ガス流量　BCl_3／Cl_2＝６０／９０ｓｃｃｍ，マイクロ波パワー　１０００Ｗ，ＲＦパワー　５０Ｗ，圧力　２１．３Ｐａ

上記工程を経て本実施例によるＭＯＳトランジスタが製造される。

【００７１】次に図７は本発明による第４実施例を示すＭＯＳトランジスタ製造後半工程断面図である。

【００７２】本実施例は、Ｓｉと反応するための拡散する主な原子（move spieces）が金属である場合を示す。（Ｔｉの場合は move speicesがＳｉである。）接続孔内のカバレージを積極的に向上させるためにはスパッタリングする原子の拡散を接続孔内へより活発に生じさせる必要がある。Ｓｉとの反応の move spieces がスパッタリングする金属原子であれば接続孔の金属は流動し易くなる。

【００７３】その例として反応の move spieces が金属である物質は，Ｃｏ，Ｎｉ，Ｐｄ等の遷移金属のシリサイドが考えられる。

【００７４】Ｃｏを例とした工程を以下に説明する。

【００７５】本実施例は、まず第１実施例で示した（１）～（４）までの工程を経て図７（ａ）に示す様にシリコン基板１上に層間絶縁膜７ａおよび接続孔１５を形成する。

【００７６】（５）図７（ｂ）に示す様に接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＣｏ１６を形成する。この時シリコン基板１の温度を６００℃程度まで加熱する。

Ｃｏスパッタ条件例　Ａｒ＝４０ｓｃｃｍ，圧力　０．０４Ｐａ，
ＲＦバイアス　５０Ｗ，温度　６００℃，
スパッタパワー　１ＫＷ，膜厚　３０ｎｍ

図７（ｂ）に示す様に接続孔１５の底部にＣｏシリサイドＣｏ$Si_2$１７が形成される。またＣｏは接続孔１５の側壁部にもオーバーハング形状にはならず、カバレージ良く形成される。

【００７７】（６）接続孔１５の底部及び側壁部を含む、シリコン基板１の全面にＡｌを高温スパッタで形成する。

Ａｌスパッタ条件例　Ａｒ流量　４０ｓｃｃｍ，圧力　０．０４Ｐａ，
温度　５００℃，スパッタパワーＤＣ　１ＫＷ，

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膜厚５００ｎｍ

この時、接続孔１５内に均一にＣｏが堆積しているために、Ａｌは Ｃｏと反応しながら接続孔１５の底部から上方へ均一に埋め込んで行く。従って接続孔１５の完全平坦化を可能となる。

【００７８】次にレジストパターニングを行い、次いでメタル配線膜のドライエッチを行い図７（ｃ）に示す様にＡｌ配線１２を作りトランジスタを形成する。条件例は、ＲＦ印加型ＥＣＲエッチャーを使用、ガス流量 BCl_3／Cl_2＝６０／９０ｓｃｃｍ，マイクロ波パワー １０００Ｗ，ＲＦパワー ５０Ｗ，圧力 ２１．３Ｐａ 上記工程を経て本実施例によるＭＯＳトランジスタが製造される。

【００７９】尚、本発明は、本実施例に限定するものではなく、本目的が達成できれば他の物質、方法を用いても良い。

【００８０】例えば、Ａｌの替りにＡｌ合金、もしくはＡｌ以外のＣｕ，Ａｇ，Ｗ，Ｍｏ等の金属、Ａｌとの反応物質であるＴｉの替りに、Ｗ，Ｍｏ等の高融点金属，貴金属、遷移金属、半導体物質を用いても良い。

【００８１】

【発明の効果】以上説明した様に、本発明によれば、Ｔｉ等の金属を接続孔の底部の下地シリコン基板と反応させながら堆積させるので、Ｔｉ等の拡散が活発に起こり接続孔内のカバレージを改善することが出来、しかもフィールド酸化膜のエッジ部の接合リークの問題点を解決することが出来る。

【００８２】また高温Ａｌを埋め込むために必要な下地物質（Ｔｉ等）が接続孔内に均一に形成されるために、埋め込む高温Ａｌを均一に形成されるために、埋め込む高温Ａｌを均一に埋め込むことが出来る。

【００８３】また接続孔内に安定した厚さのＴｉ等を堆積することが出来るので、接続孔内のみにＴｉ等のシリサイドを安定して形成することが出来る。

【００８４】またＡｌとの接続部のＳＩＴＯＸ－シリサイド（例えば$TiSi_2$）は酸化物がＡｌに対してバリア性を有し、バリアメタルとして働きしかも、低抵抗なシート抵抗を維持することが出来る。

【図面の簡単な説明】

【図１】第１実施例を示すＭＯＳトランジスタ製造前半工程断面図である。

【図２】第１実施例を示すＭＯＳトランジスタ製造中半工程断面図である。

【図３】第１実施例を示すＭＯＳトランジスタ製造後半工程断面図である。

【図４】第２実施例を示すＭＯＳトランジスタ製造後半工程断面図である。

【図５】第３実施例を示すＭＯＳトランジスタ製造後半工程断面図（その１）である。

【図６】第３実施例を示すＭＯＳトランジスタ製造後半工程断面図（その２）である。

【図７】第４実施例を示すＭＯＳトランジスタ製造後半工程断面図である。

【図８】本発明による埋め込み効果のメカニズムを説明する断面図である。

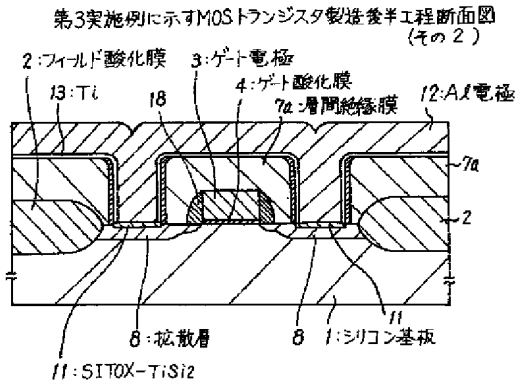
【図９】従来例を示すＭＯＳトランジスタ製造前半工程断面図である。

【図１０】従来例を示すＭＯＳトランジスタ製造後半工程断面図である。

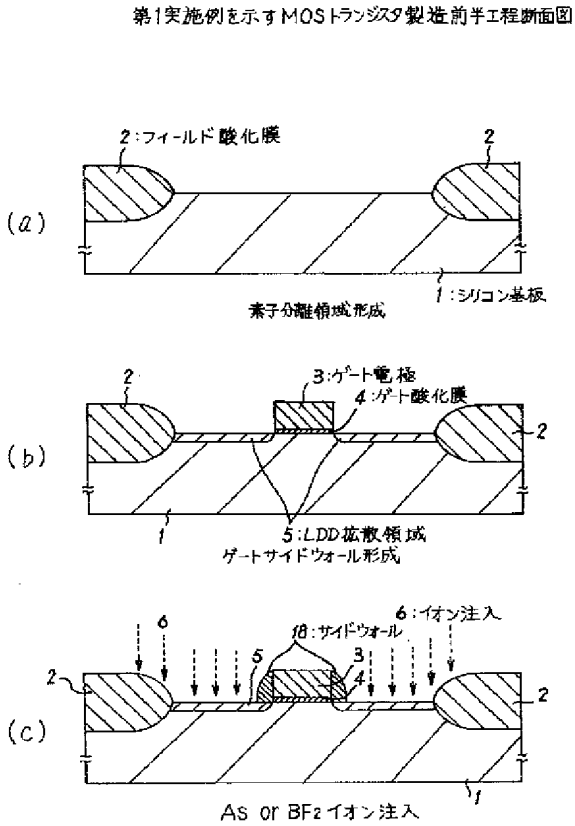
【符号の説明】

１　シリコン基板
２　フィールド酸化膜
３　ゲート電極
４　ゲート酸化膜
５　ＬＤＤ拡散領域
６　イオン注入（Ａｓ ｏｒ BF_2）
７　層間膜
８　拡散層
９　酸化膜
１０，１３　Ｔｉ
１１，２１　ＳＩＴＯＸ－$TiSi_2$
１２　Ａｌ配線
１４，１４ａ　シリコン窒化膜（ＳｉＮ）
１５　接続孔
１６　Ｃｏ
１７　$CoSi_2$
１８　サイドウォール

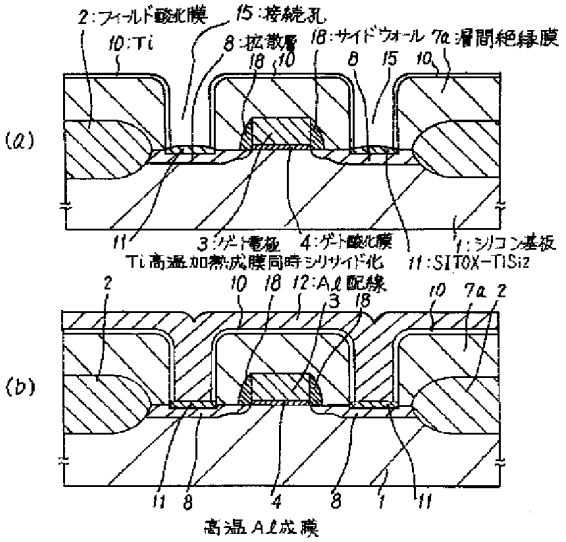
【図６】


第3実施例に示すMOSトランジスタ製造後半工程断面図
（その２）
2:フィールド酸化膜
13:Ti
18
3:ゲート電極
4:ゲート酸化膜
7a:層間絶縁膜
12:Al電極
7a
2
8:拡散層
8
1:シリコン基板
11
11:SITOX-TiSi2
高温Ti+高温Al成膜

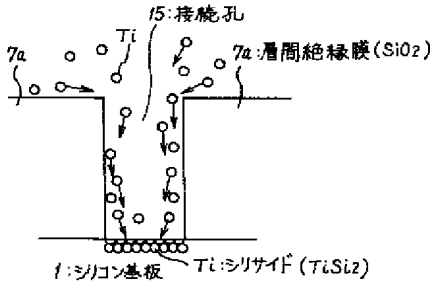
【図１】


第1実施例を示すMOSトランジスタ製造前半工程断面図
(a)
2:フィールド酸化膜
2
1:シリコン基板
素子分離領域形成
(b)
2
3:ゲート電極
4:ゲート酸化膜
2
1
5:LDD拡散領域
ゲートサイドウォール形成
(c)
6
6:イオン注入
18:サイドウォール
5
3
4
2
2
1
As or BF2 イオン注入

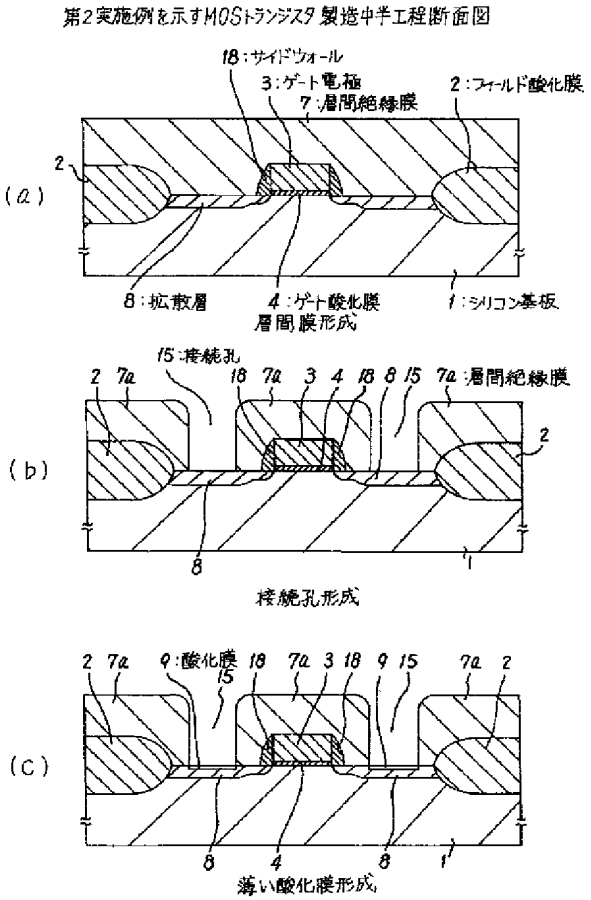
【図３】


実施例を示すMOSトランジスタ製造後半工程断面図
(a)
2:フィールド酸化膜
15:接続孔
10:Ti
8:拡散層
18:サイドウォール
7a:層間絶縁膜
18
10
8
15
10
11
3:ゲート電極
4:ゲート酸化膜
1:シリコン基板
Ti高温加熱成膜同時シリサイド化
11:SITOX-TiSi2
(b)
2
10
18
12:Al配線
3
18
10
7a
2
11
8
4
8
1
11
高温Al成膜

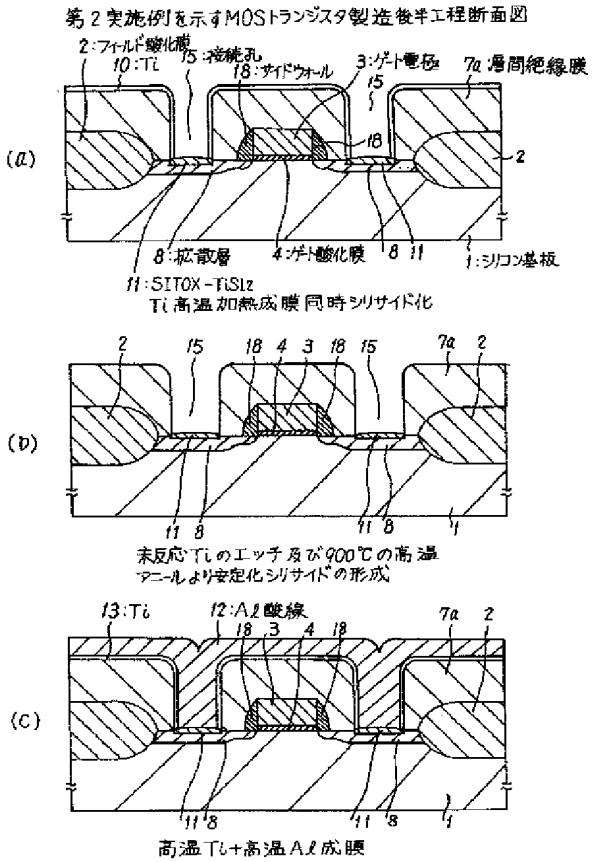
【図８】


本発明によるメカニズムを説明するための模式図
15:接続孔
Ti
7a
7a:層間絶縁膜(SiO2)
1:シリコン基板
Ti:シリサイド(TiSi2)
TiはSiと反応しようとするため
Si方向に拡散する.(基板温度600℃以上)

【図２】

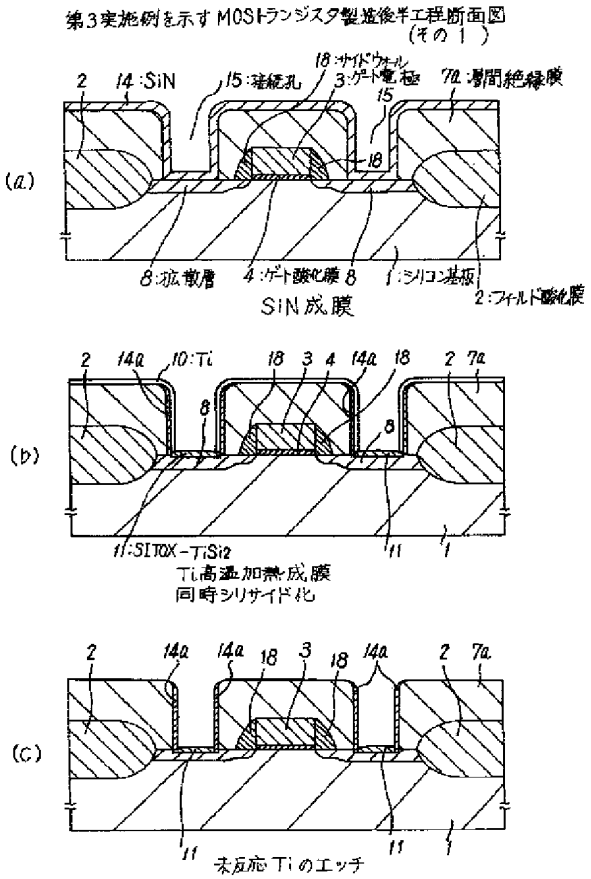


【図４】

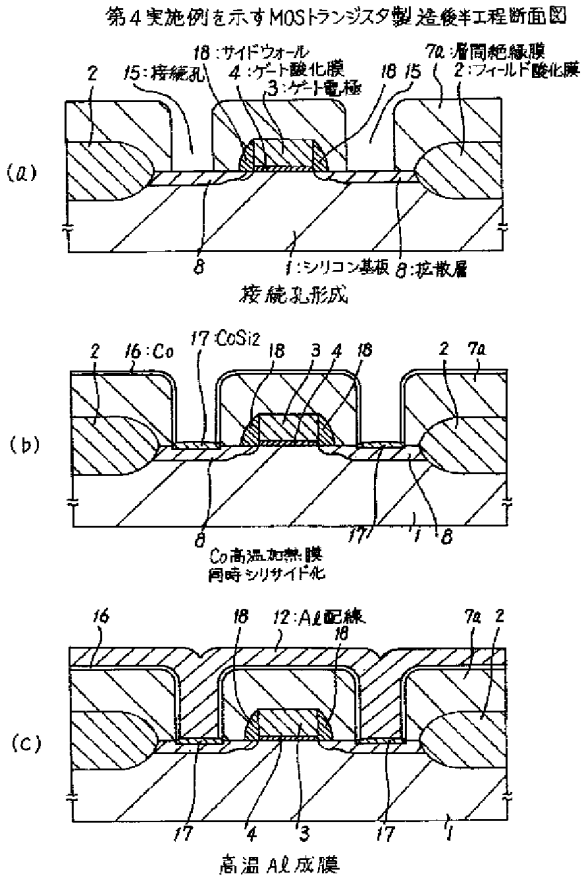


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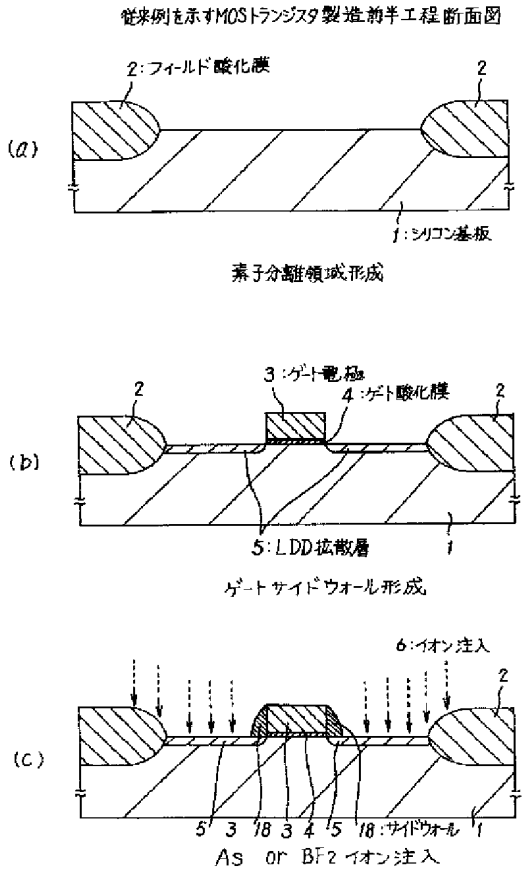
【図５】


第3実施例を示すMOSトランジスタ製造後半工程断面図
（その１）
(a)
2
14:SiN
15:接続孔
18:サイドウォール
3:ゲート電極
7a:層間絶縁膜
8:拡散層
4:ゲート酸化膜
1:シリコン基板
2:フィールド酸化膜
SiN成膜
(b)
14a
10:Ti
11:SiTiOX-TiSi2
Ti高温加熱成膜
同時シリサイド化
(c)
未反応Tiのエッチ

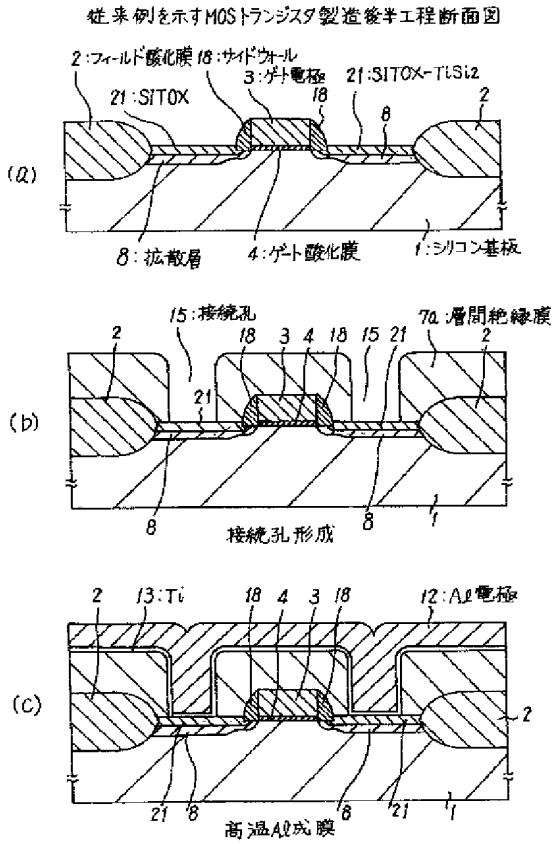
【図７】


第4実施例を示すMOSトランジスタ製造後半工程断面図
(a)
2
15:接続孔
18:サイドウォール
4:ゲート酸化膜
3:ゲート電極
7a:層間絶縁膜
2:フィールド酸化膜
8
1:シリコン基板
8:拡散層
接続孔形成
(b)
16:Co
17:CoSi2
Co高温加熱膜
同時シリサイド化
(c)
16
18
12:Al配線
7a
17
4
3
高温Al成膜

【図９】



【図１０】



フロントページの続き

(58)調査した分野(Int.Cl.⁷，ＤＢ名)
H01L　21/28 - 21/288
H01L　21/44 - 21/445
H01L　29/40 - 29/43
H01L　29/47
H01L　29/872
H01L　21/3205
H01L　21/3213
H01L　21/768

Espacenet

JP3208599B2

Applicants: SONY CORP

Inventors: SUMI HIROBUMI

Classifications:

IPC ***H01L21/28; H01L21/3205; H01L21/336; H01L21/768; H01L23/52; H01L23/522; H01L29/78;***
(IPC1-7): H01L21/28; H01L21/3205; H01L21/768;

Priorities: JP13698892A 1992-05-28

Application: JP3208599B2·1992-05-28

Publication: JP3208599B2·2001-09-17

Published as: **JPH05335330A;** JP3208599B2

Abstract

PURPOSE:To provide a embedding formation method of a connection hole having a good barrier characteristic against electrode materials, such as alminum, and also good embedding characteristic. CONSTITUTION:Relating to embedding-formation of connection holes where wiring material is embedded in connection holes 15 formed by patterning the inter-layer insulation film 7a formed an the entire upper surface of a silicon substrate 1, the process in which the inter-layer insulation film is patterned for formating the connection holes 15, and then the metal for forming silicide in the connection hole 15 is deposited at the temperature at which the silicon substrate 1 and the metal react with each other is included.

Connection hole filling method

JP3208599B2
Japan

Find Prior Art Similar

Other languages: Japanese
Inventor: 博文 桑

Worldwide applications
1992 JP

Application JP13698892A events

1992-05-28	Application filed by ソニー株式会社
1992-05-28	Priority to JP13698892A
1993-12-17	Publication of JPH05335330A
2001-09-17	Application granted
2001-09-17	Publication of JP3208599B2
2012-05-28	Anticipated expiration
Status	Expired - Fee Related

Info: Cited by (1), Legal events, Similar documents, Priority and Related Applications
External links: Espacenet, Global Dossier, Discuss

Claims (5)

Hide Dependent

(57) [Claims]

1. A method for burying a connection material, wherein a wiring material is buried in a connection hole formed by patterning an interlayer insulating film formed over the entire surface of a silicon substrate, wherein the connection hole is formed by patterning the interlayer insulating film. After forming, a metal for forming a silicide in the connection hole,
A method for burying a connection hole, comprising, depositing at a temperature at which the silicon substrate and a metal for forming the silicide react.

2. The method according to claim 1, wherein the metal for forming the silicide is a transition metal.

3. The method according to claim 2, wherein the transition metal is cobalt.

4. A method for burying a wiring material in a connection hole formed by patterning an interlayer insulating film formed over the entire surface of a silicon substrate, wherein the connection hole is formed by patterning the interlayer insulating film. After forming, a metal for forming a silicide in the connection hole,
Depositing at a temperature at which the silicon substrate reacts with a metal for forming the silicide; removing metal not reacting with the silicon substrate, stabilizing a reactant between the metal and the silicon substrate. Performing a high-temperature heat treatment for depositing the metal for forming the silicide in the connection hole at a temperature at which the silicon substrate and the metal for forming the silicide react with each other. A method for forming a buried connection hole.

5. A method for burying a connection material, wherein a wiring material is buried in a connection hole formed by patterning an interlayer insulating film formed over the entire surface of a silicon substrate, wherein the connection hole is formed by patterning the interlayer insulating film. Forming a thin oxide film at the bottom of the contact hole after forming the contact hole; and a temperature at which the metal for forming silicide in the contact hole reacts with the silicon substrate and the metal for forming the silicide. A step of depositing a contact hole.

Description

DETAILED DESCRIPTION OF THE INVENTION

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a method for manufacturing a semiconductor device, and more particularly to

a method for filling a fine connection hole.

[0002]

2. Description of the Related Art In recent years, as the degree of integration in memory devices has increased, the miniaturization of devices has been progressing. For this reason, the technique of embedding metal in the connection hole is increasing in difficulty for miniaturization of the connection hole.

In order to enable connection with an element, it is necessary to embed a wiring material such as aluminum (Al) used for wiring. As a method therefor, an Al embedding technique by high-temperature sputtering has recently attracted attention. The method is
While heating a silicon (Si) substrate to a high temperature of several hundred degrees,
This is a technique in which Al is reflowed by sputter-depositing an Al-alloy, Al is filled in connection holes, and flattened. In this case, for example, A such as Ti
When a material that easily reacts with Al is used, Al during film formation and the base T
It is known that due to the progress of the interfacial reaction with i, the wettability between the two is improved, and good embedding with Al spreading can be performed.

In order to bury Al in the connection hole, Al
Good embedding characteristics between the substrate and the base, prevention of penetration of Al into the silicon substrate, and the like are required.

[0005] To meet these requirements, an Al film-forming structure as described below has conventionally been adopted.

(1) The film formation structure of Al is Al / TiON /
Ti These three layers are continuously formed in a vacuum using a single-wafer multi-chamber sputtering apparatus.

(2) The film structure of Al is Al / Ti / Ti
ON / Ti (3) A film structure of Al is made of Al / Ti / TiN / Ti (4) SALICIDE (Self
SITOX (Silicidation through oxicide) -Ti
After forming Si_2 , an interlayer insulating film and a connection hole are formed thereon, and Al is formed.

[0008] Of these conventional connection hole filling techniques, the case (4) will be described below, taking the manufacture of a MOS transistor as an example.

FIG. 9 and FIG. 10 are sectional views of a MOS transistor manufacturing process.

The process will be described below in the order of steps.

(1) As shown in FIG. 9A, a field oxide film 2 for element isolation is formed on a silicon substrate 1.

(2) Polycrystalline silicon and WSi_2 are deposited by performing gate oxidation and patterning is performed, as shown in FIG.
A gate oxide film 4 and a gate electrode 3 are formed as shown in FIG. Next, LDD (Lightly doped drain) ion implantation is performed to form an LDD diffusion layer 5.

(3) After an oxide film is formed on the entire surface of the silicon substrate 1, the entire surface is etched back to form a sidewall 18 as shown in FIG. 9 (c).

Next, ion implantation 6 is performed on the entire surface of the silicon substrate 1 as shown in FIG. 9C to form source / drain regions, and a diffusion layer 8 is formed as shown in FIG. 10A. .

(4) A thin oxide film is formed on the entire surface of the silicon substrate 1.

Next, after Ti is deposited on the entire surface, SITOX-$TiSi_2$ 21 is formed on the source and drain regions by heat treatment as shown in FIG.

Next, unreacted Ti on the oxide film is selectively etched.

(5) An interlayer insulating film is formed on the entire upper surface of the silicon substrate 1, resist patterning is performed, and dry etching is performed to form an interlayer insulating film 7 as shown in FIG.
a and the connection hole 15 are formed.

(6) After depositing Ti13 on the entire surface,
1 is formed on the entire surface.

Next, resist patterning is performed, and Al wiring 1 is formed by dry etching as shown in FIG.
Form 2.

[0021]

However, any of the above-described conventional connection hole filling techniques has the following problems.

(1) The film structure of Al is Al / TiON /
In the case of Ti, Al and TiON hardly react with each other, the wettability of both is poor, and the embedding property of Al is extremely deteriorated.

(2) Al film structure is Al / Ti / Ti
In the case of ON / Ti The embedding characteristics are improved as compared with the case of (1) in which Al directly contacts TiON, but not as much as in the case of a Ti single layer. It is because oxygen in TiON diffuses into the upper Ti film when the silicon substrate is heated to several hundred degrees during Al film formation.
This is because the oxygen reaches the surface, the Ti in this portion is oxidized, the reaction with Al deteriorates, and the embedding characteristics deteriorate.

(3) The film structure of Al is Al / Ti / Ti
In the case of N / Ti Using TiN instead of TiON as an Al barrier metal solves the problem of poor embedding, but TiN has insufficient Al barrier properties compared to TiON, and high-temperature sputtering or Al sintering The heating process causes penetration of Al.

(4) SALIC over the entire source / drain
In order to form SITOX-$TiSi_2$ 21 by IDE,
As shown in FIG. 10A, this SITOX-$TiSi_2$ 21 will be in contact with the field oxide film 2. However, $TiSi_2$ has a tensile stress, which induces crystal defects in the silicon substrate 1 at the edge of the field oxide film 2, and increases junction leakage by one digit in the silicon diffusion layer.

SUMMARY OF THE INVENTION It is an object of the present invention to provide a method for burying a contact hole having an electrode material such as aluminum and having a good burying property.

[0027]

According to the present invention, there is provided a connection hole filling method for filling a connection material formed by patterning an interlayer insulating film formed over the entire surface of a silicon substrate with a wiring material. After patterning the interlayer insulating film to form a connection hole, a metal for forming a silicide in the connection hole is deposited at a temperature at which the silicon substrate and the metal for forming the silicide react. This problem is solved by a method for forming a buried connection hole, which comprises the step of:

Further, according to the present invention, the above-mentioned object is suitably solved by a method for forming a buried contact hole, wherein the metal is a transition metal. Further, the above problem is suitably solved by a burying method in which the transition metal is cobalt.

According to the present invention, there is also provided a method for burying a connection hole, wherein a wiring material is buried in a connection hole formed by patterning an interlayer insulating film formed over the entire surface of a silicon substrate. After patterning an insulating film to form a connection hole, depositing a metal for forming silicide in the connection hole at a temperature at which the silicon substrate and the metal for forming the silicide react with each other, Removing a metal that has not reacted with the silicon substrate, performing a high-temperature heat treatment to stabilize a reactant between the metal and the silicon substrate, and forming a metal for forming the silicide in the connection hole. Depositing at a temperature that reacts with a metal for forming silicide with the silicon substrate. It is solved Te

According to the present invention, there is also provided a method for burying a connection hole, wherein a wiring material is buried in a connection hole formed by patterning an interlayer insulating film formed over the entire surface of a silicon substrate. After forming a connection hole by patterning an insulating film, a step of forming a thin oxide film on the bottom of the connection hole, and forming a metal for forming silicide in the connection hole and forming the metal on the silicon substrate and the silicide And a step of depositing the contact hole at a temperature at which the metal reacts with the metal.

According to the present invention, the oxide film is a silicon oxide film or a silicon oxynitride film, the thickness of which is 10 nm or less, the metal for forming the silicide is titanium, and the connection hole is formed. The method is preferably achieved by a method for forming a buried contact hole, wherein a metal is deposited at a temperature of 600 ° C. or more.

[0032]

[0033]

According to the present invention, as shown in FIG. 8, after the interlayer insulating film is patterned to form a connection hole 15, a metal for forming a silicide with the silicon substrate 1 is deposited in the connection hole 15. By performing at a temperature at which the silicon substrate 1 and the metal react, the metal atoms actively diffuse in the silicon direction in an attempt to react with silicon (Si),
It can react with Si to form silicide. As a result, a flat surface is formed on the metal deposition surface by the diffusion of the metal atoms, and the coverage of the bottom of the connection hole 15 with the silicon substrate 1 can be improved. Moreover, since the silicide is formed only at the bottom of the connection hole 15, crystal defects of silicon at the edge of the field oxide film can be prevented.

According to the present invention, if the above-mentioned metal is a transition metal, the transition metal becomes a main atom (move spieces) which reacts with silicon and diffuses. And the metal deposition surface in the connection hole 15 can be suitably flattened.

According to the present invention, when a metal is deposited in the connection hole 15 at a temperature at which the silicon substrate 1 reacts with the metal, as shown in FIG. Since unreacted metal is deposited on the upper layer of the substance (silicide), only the unreacted metal can be selectively removed. As a result, the deposition surface of the connection hole 15 can be further flattened. In addition, the silicide can be stabilized by performing a high-temperature treatment after removing only the unreacted metal.

Further, by depositing the metal on the flat silicide in the connection hole 15 at a temperature at which the metal reacts with the silicon substrate 1, the deposited metal actively diffuses and reacts with silicon. It can be flattened.

According to the present invention, after forming a thin oxide film 9 on the bottom of the connection hole 15 as shown in FIG.
By depositing a metal at a temperature at which the silicon substrate 1 reacts with the metal in the connection hole 15 shown in FIG.
SITOX (Silici) which is a reactant with metal and silicon
dation through oxicide)-silicide can be formed. This reactant has a barrier property when an electrode such as aluminum is formed, and forms a suitable electrode base having a low sheet resistance.

According to the present invention, the thin oxide film is a silicon oxide film or a silicon oxynitride film, and the metal to be deposited is titanium (Ti).
-$TiSi_2$ is formed. This SITOX-$TiSi_2$
Has a low sheet resistance of 10Ω or less and is 500 ° C
It has a barrier property against aluminum up to the temperature of, and forms a suitable electrode base material.

[0039] According to the invention, the bottom and the silicon nitride film on the side wall of the connection hole 15 as shown in FIG. 5 (b) (Si
N) After the formation of 14, when the metal is deposited in the connection hole 15 at a temperature at which the silicon substrate 1 reacts with the metal, an interlayer insulating film which is an oxide film of metal and silicon is formed on the side wall of the connection hole 7a, the silicon nitride film 14 is interposed therebetween, so that metal oxidation can be reduced. As a result, it is possible to improve the characteristics of embedding with an electrode such as aluminum.

[0040]

DESCRIPTION OF THE PREFERRED EMBODIMENTS Embodiments according to the present invention will be described below in detail with reference to the drawings.

FIGS. 1 to 3 are sectional views showing the steps of manufacturing a MOS transistor according to a first embodiment of the present invention.

Hereinafter, the first embodiment will be described in the order of steps.

(1) As shown in FIG. 1A, a field oxide film 2 for element isolation is formed on a silicon substrate 1.

(2) Oxidation for the gate is performed. Conditions Gas $_{H2/O2=6/4}$ l / min, temperature 8
Next, polycrystalline silicon is deposited on the entire surface at 50 ° C. and a thickness of 16 nm. Condition Gas SiH_4 / PH_3 / H_2 = 500 / 0.35
/ 50sccm, temperature 580 ° C, pressure 79.8Pa,

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Next, WSi_2 is deposited on the entire surface. Conditions WF_6 / SiH_4 / He = 10/1000/360
sccm, temperature 360 ° C, pressure 26.6 Pa, film thickness
Next, resist patterning is performed, and a gate wiring portion is formed by dry etching. Conditions Gas $C_2Cl_3F_3$ / SF_6 = 65/5 sccm,
Pressure 1.33Pa, microwave power 100W, RF
Power 100 W In this manner, as shown in FIG.
The gate electrode 3 is formed.

Next, LDD ions (As or BF_2) are implanted to form an LDD diffusion layer 5.

(3) After an oxide film is formed on the entire surface of the silicon substrate 1, the entire surface is etched back to form a sidewall 18 as shown in FIG. 1 (c).

Next, in order to form source / drain regions, ion implantation 6 is performed on the entire surface of the silicon substrate 1 as shown in FIG. 1C, and a diffusion layer 8 is formed as shown in FIG. 2A. . In the case of NMOS, As 50 KeV, 5e15 / cm^2 ,
In the case of PMOS, BF_2 20 KeV, 3e15 / cm^2
It is performed under the following conditions.

(4) As shown in FIG. 2A, an interlayer insulating film 7 is formed on the entire surface of the silicon substrate 1. Conditions Gas flow rate SiH_4 / O_2 / N_2 = 250/250
/ 100sccm, temperature 420 ° C, pressure 13.3P
a, Film thickness: 500 nm Further, activation annealing is performed at 1100 ° C. for 10 seconds.

(5) Perform resist patterning and pattern by dry etching to form connection holes 15 as shown in FIG. 2B. Conditions Gas C_4F_8 = 50 sccm, RF power 120
0W, pressure 2Pa

[0050] (5) of the connection hole 15 as shown in FIG. 2 (c)
A thin oxide film 9 is formed on the bottom . Conditions Gas H_2O / O_2 = 1.5 / 6 1 / min, temperature 850 ° C., film thickness 3 nm

[0051] (7) of the connection hole 15 as shown in FIG. 3 (a)
Ti1 is formed on the entire surface of the silicon substrate 1 including the bottom and side walls.
0 is formed. At this time, the temperature of the silicon substrate 1 is set to 600 ° C.
To about a degree. Example of Ti sputtering conditions: Ar = 40 sccm, pressure: 0.04 Pa, sputtering power: 1 kW, film thickness: 30 nm As a result, metal atoms to be sputtered diffuse into the connection hole 15 because they react with the underlying Si one after another. Since the atoms flow into the connection hole 15, the coverage of the Ti 10 does not become an overhang shape and can be uniformly formed in the connection hole 15.

Further, since Ti 10 in contact with Si in the connection hole 15 forms silicide, the connection hole 15
The sheet resistance inside is kept as low as 100 or less. Subsequent contact resistance with the Al wiring also becomes a low resistance of 100 or less. Further, the silicide to be formed is SITOX-TiSi
Since $_2$ 11, with a barrier against Al to a temperature of 500 ° C..

(6) Including the bottom and side walls of the connection hole 15
First, Al is formed on the entire surface of the silicon substrate 1 . Example of Al sputtering conditions Ar flow rate 40 sccm, pressure 0.04 Pa, sputtering power DC 1 KW, film thickness 500 nm Next, resist patterning was performed, and the above-mentioned Al dry etching was performed, and as shown in FIG.
Form 2 An example of the condition is to use an RF application type ECR etcher, a gas flow rate of BCl_3 / Cl_2 = 60/90 sccm, a microwave power of 100 W, an RF power of 50 W, and a pressure of 21.3 Pa. Manufactured.

FIG. 4 is a sectional view showing the second half of the process of manufacturing a MOS transistor according to the second embodiment.

This embodiment is different from the first embodiment shown in FIG.
Unreacted Ti at the time of forming SITOX-$TiSi_2$ in the step ($_1$) is selectively removed. After that, stable TiS
High temperature annealing at about 900 ° C. is performed to form i_2 . Then, Ti is newly deposited to bury the Al wiring. The steps will be described below.

In this embodiment, the interlayer insulating film is patterned on the silicon substrate 1 through the steps (1) to (6) shown in the first embodiment, and the connection hole 15 and the surface of the connection hole 15 are thinly oxidized. Form a film.

[0057] (7) 4 of the contact hole 15 as shown in (a)
Ti1 is formed on the entire surface of the silicon substrate 1 including the bottom and side walls.
0 is formed. At this time, the temperature of the silicon substrate 1 is set to 600 ° C.
Raise to the extent. Example of Ti sputtering conditions: Ar = 40 sccm, pressure: 0.04 Pa, RF bias: 50 W, sputtering power: 1 kW, film thickness: 30 nm As a result, metal atoms to be sputtered diffuse into the connection holes 15 because they react with the underlying Si one after another. Since the atoms flow into the connection hole 15, Ti atoms can be uniformly supplied to the bottom of the connection hole 15. As a result, a Ti silicide having a stable film thickness can be formed.

(8) As shown in FIG. 4B, the interlayer insulating film 7
a and unreacted Ti on SITOX-$TiSi_2$ 11
10 is selectively etched. Condition example: Immerse in a solution of NH_4OH: H_2O_2 : H_2O = 1: 2: 2 for 10 minutes.

Next, a heat treatment is performed at 900 ° C. for about 30 seconds to form stable $TiSi_2$.

Since silicide is formed in the connection hole 15, the sheet resistance in the connection hole 15 maintains a low resistance of 100 or less. Subsequent contact resistance with Al wiring is also 100.
The following low resistance is obtained. The silicide to be formed is SI
Since it is TOX-$TiSi_2$ 11, it has a barrier property against Al up to a temperature of 500 ° C.

[0061] (9) 4 of the contact hole 15 as shown in (c)
Ti1 is formed on the entire surface of the silicon substrate 1 including the bottom and side walls.
Form 3 In this case, too, the preformed TiSi
In order to increase the coverage of Ti by reacting Ti and Si through Step $_2$, deposition is performed while heating at about 600 ° C. during Ti film formation. Example of Ti

sputtering conditions: Ar = 40 sccm, pressure: 0.04 Pa, RF bias: 50 W, sputtering power: 1 kW, film thickness: 30 nm Next , the silicon substrate including the bottom and side wall of the connection hole 15
1 is formed on the entire surface of the substrate 1 . Example of Al sputtering conditions: Ar flow rate 40 sccm, pressure 0.04 Pa, sputtering power DC 1 kW, film thickness 500 nm Next, resist patterning is performed, and dry etching of the Al is performed, and the Al wiring 12 is formed as shown in FIG.
To form An example of the condition is to use an RF application type ECR etcher, a gas flow rate of BCl_3 / Cl_2 = 60/90 sccm, a microwave power of 1000 W, an RF power of 50 W, and a pressure of 21.3 Pa. Manufactured.

FIGS. 5 and 6 show a third embodiment of the present invention.
FIG. 10 is a sectional view of the latter half of the process of manufacturing the OS transistor.

In the present embodiment, Si is formed on SiO_2 on the side of the connection hole.
This is a method in which the formation of N suppresses the oxidation of Ti to be formed later. Hereinafter, the steps of this embodiment will be described.

In this embodiment, first, through the steps (1) to (5) shown in the first embodiment, the interlayer insulating film is patterned on the silicon substrate 1 to form the connection holes 15.

[0065] (6) 5 of the contact hole 15 as shown in (a)
SiN is applied to the entire surface of the silicon substrate 1 including the bottom and side walls.
14 is formed. Conditional example gas SiH_4 / NH_3 / N_2 = 180/500/720 sccm, temperature 250 ° C., pressure 40 Pa, film thickness 100 nm

(7) As shown in FIG. 5B, the SiN 14 is etched back to form a SiN 14a on the side wall of the interlayer insulating film 7a.
To form Next, the bottom of the connection hole 15 having the SiN 14a
Ti10 on the entire surface of the silicon substrate 1 including the portion and the side wall portion.
To form Condition example gas CHF_3 = 50 sccm, RF power 150 W, pressure 2 Pa Ti sputtering condition example Ar flow rate 40 sccm, pressure 0.04 Pa, sputtering power DC 1 KW, film thickness 500 nm

(8) As shown in FIG. 5C, unreacted Ti is selectively etched. Condition example: immerse in a solution of NH_4OH: H_2O_2 : H_2O = 1: 2: 2 for 10 minutes.

Thereafter, a heat treatment is applied at 900 ° C. for about 30 seconds to form stable $TiSi_2$.

[0069] (9) the bottom of the contact hole 15 as shown in FIG. 6
Ti13 is deposited on the entire surface of the silicon substrate 1 including the sidewalls and the sidewalls . Also in this case, in order to increase the coverage of Ti by reacting Ti and Si through $TiSi_2$ formed in advance, deposition is performed while heating at about 600 ° C. during Ti film formation. Example of Ti sputtering conditions:
Ar = 40 sccm, pressure: 0.04 Pa, RF bias: 50 W, sputtering power: 1 kW, film thickness: 30 nm Next , the silicon substrate including the bottom and side wall of the connection hole 15
1 is formed on the entire surface of the substrate 1 . Next, resist patterning is performed, and then dry etching of the metal wiring
A wiring 12 is formed to form a transistor. An example of the condition is to use an RF application type ECR etcher, a gas flow rate of BCl_3 / Cl_2 = 60/90 sccm, a microwave power of 1000 W, an RF power of 50 W, and a pressure of 21.3 Pa. The MOS transistor according to this embodiment is manufactured through the above steps. You.

Next, resist patterning is performed, and then dry etching of the metal wiring film is performed to form an Al wiring 12 and form a transistor. Condition example is RF applied ECR
Using an etcher, gas flow rate BCl_3 / Cl_2 = 60 /
90 sccm, microwave power 1000 W, RF power 50 W, pressure 21.3 Pa Through the above steps, the MOS transistor according to the present embodiment is manufactured.

FIG. 7 is a sectional view showing the latter half of the process of manufacturing a MOS transistor according to a fourth embodiment of the present invention.

This embodiment shows a case where the main diffusing atoms (move spieces) for reacting with Si are metal.
(In the case of Ti, the move speices are Si.) In order to positively improve the coverage in the connection hole, it is necessary to cause diffusion of atoms to be sputtered more actively into the connection hole. If the move spieces of the reaction with Si are metal atoms to be sputtered, the metal in the connection hole will flow more easily.

As an example, a substance in which the move spieces of the reaction are metals may be a silicide of a transition metal such as Co, Ni or Pd.

A process using Co as an example will be described below.

In this embodiment, first, through the steps (1) to (4) shown in the first embodiment, the interlayer insulating film 7a and the connection holes 15 are formed on the silicon substrate 1 as shown in FIG. To form

[0076] (5) 7 of the contact hole 15 as shown in (b)
Co1 is coated on the entire surface of the silicon substrate 1 including the bottom and side walls.
6 is formed. At this time, the temperature of the silicon substrate 1 is set to 500 ° C.
Heat to a degree. Example of Co sputtering conditions Ar = 40 sccm, pressure 0.04 Pa, RF bias 50 W, temperature 600 ° C., sputtering power 1 kW, film thickness 30 nm
As shown in FIG. 7B, Co silicide $CoSi_2$ 17 is provided at the bottom of the connection hole 15. It is formed. Co is the connection hole 15
Is not formed in an overhang shape on the side wall portion, but is formed with good coverage.

(6) Including the bottom and side walls of the connection hole 15
First, Al is formed on the entire surface of the silicon substrate 1 by high-temperature sputtering. Example of Al sputtering conditions Ar flow rate 40 sccm, pressure 0.04 Pa, temperature 500 ° C., sputtering power DC 1 KW, film thickness 500 nm At this time, since Co is uniformly deposited in the connection hole 15, Al reacts with Co.
While from the bottom of the connection hole 15
Embed evenly toward the end . Therefore, the connection hole 15 can be completely flattened.

Next, resist patterning is performed, and then dry etching of the metal wiring film is performed to form an Al wiring 12 as shown in FIG. 7C to form a transistor. The condition example uses the RF application type ECR etcher, gas flow rate B
Cl_3 / Cl_2 = 60/90 sccm, microwave power 1000 W, RF power 50 W, pressure 21.3 Pa Through the above steps, the MOS transistor according to the present embodiment is manufactured.

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The present invention is not limited to the present embodiment, and other substances and methods may be used as long as the object can be achieved.

For example, instead of Al, an Al alloy or a metal other than Al, such as Cu, Ag, W, or Mo, or a high melting point metal, such as W or Mo, instead of Ti, which is a reactant with Al.
Noble metals, transition metals, and semiconductor materials may be used.

[0081]

As described above, according to the present invention, T
Since the metal such as i is deposited while reacting with the underlying silicon substrate at the bottom of the connection hole, Ti and the like are actively diffused, the coverage in the connection hole can be improved, and the edge of the field oxide film is joined. The problem of the leak can be solved.

Since the base material (Ti or the like) necessary for embedding high-temperature Al is uniformly formed in the connection hole,
Since the high-temperature Al to be embedded is uniformly formed, the high-temperature Al to be embedded can be uniformly embedded.

Further, since a stable thickness of Ti or the like can be deposited in the connection hole, silicide such as Ti can be stably formed only in the connection hole.

The oxide of SITOX-silicide (eg, $TiSi_2$) at the connection portion with Al has a barrier property against Al, works as a barrier metal, and can maintain a low sheet resistance.

[Brief description of the drawings]

FIG. 1 is a sectional view showing a first half of a process of manufacturing a MOS transistor according to a first embodiment.

FIG. 2 is a cross-sectional view showing a half-step during manufacturing of a MOS transistor, showing a first embodiment;

FIG. 3 is a sectional view showing a second half of the process of manufacturing the MOS transistor, showing the first embodiment;

FIG. 4 is a sectional view showing a second half of a process of manufacturing a MOS transistor according to a second embodiment;

FIG. 5 is a sectional view (part 1) of a second half of the process of manufacturing a MOS transistor according to the third embodiment;

FIG. 6 is a sectional view (part 2) of the latter half of the process of manufacturing the MOS transistor, showing the third embodiment;

FIG. 7 is a sectional view of the latter half of the process of manufacturing a MOS transistor, showing a fourth embodiment;

FIG. 8 is a cross-sectional view illustrating a mechanism of an embedding effect according to the present invention.

FIG. 9 is a sectional view of a first half of a process of manufacturing a MOS transistor showing a conventional example.

FIG. 10 is a sectional view showing the latter half of the process of manufacturing a MOS transistor, showing a conventional example.

[Explanation of symbols]

Reference Signs List 1 silicon substrate 2 field oxide film 3 gate electrode 4 gate oxide film 5 LDD diffusion region 6 ion implantation (As or BF_2) 7 interlayer film 8 diffusion layer 9 oxide film 10, 13 Ti 11, 21 SITOX-$TiSi_2$ 12 Al wiring 14, 14a Silicon nitride film (SiN) 15 Connection hole 16 Co 17 $CoSi_2$ 18 Side wall

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(Int.Cl. [7], DB name) H01L 21/28-21/288 H01L 21/44-21/445 H01L 29/40-29/43 H01L 29 / 47 H01L 29/872 H01L 21/3205 H01L 21/3213 H01L 21/768

Cited By (1)

Publication number	Priority date	Publication date	Assignee	Title
Family To Family Citations				
JP2007116186A *	2006-12-04	2007-05-10	Renesas Technology Corp	Semiconductor device and method of manufacturing same

* Cited by examiner, † Cited by third party, ‡ Family to family citation

Similar Documents

Publication	Publication Date	Title
US4558507A	1985-12-17	Method of manufacturing semiconductor device
US5856237A	1999-01-05	insitu formation of TiSi2/TiN bi-layer structures using self-aligned nitridation treatment on underlying CVD-TiSi2 layer
US6013569A	2000-01-11	One step salicide process without bridging
US5874342A	1999-02-23	Process for forming MOS device in integrated circuit structure using cobalt silicide contacts as implantation media
US5989988A	1999-11-23	Semiconductor device and method of manufacturing the same
US5346836A	1994-09-13	Process for forming low resistance contacts between silicide areas and upper level polysilicon interconnects
JP2857006B2	1999-02-10	Self-aligned cobalt silicide on MOS integrated circuits.
US5668065A	1997-09-16	Process for simultaneous formation of silicide-based self-aligned contacts and local interconnects

US7078777B2	2006-07-18	Semiconductor device having a low-resistance gate electrode
KR100350358B1	2002-08-28	Method of manufacturing semiconductor device and semiconductor device
KR100302894B1	2001-11-07	integrated circuit structure with dual thickness cobalt silicide layers and method for its manufacture
US6693025B2	2004-02-17	Local interconnect structures for integrated circuits and methods for making the same
US6562718B1	2003-05-13	Process for forming fully silicided gates
US5770507A	1998-06-23	Method for forming a gate-side air-gap structure in a salicide process
US6521519B2	2003-02-18	MIS transistor and manufacturing method thereof
US5656546A	1997-08-12	Self-aligned tin formation by N2+ implantation during two-step annealing Ti-salicidation
US5767004A	1998-06-16	Method for forming a low impurity diffusion polysilicon layer
US6410429B1	2002-06-25	Method for fabricating void-free epitaxial-CoSi2 with ultra-shallow junctions
US6153485A	2000-11-28	Salicide formation on narrow poly lines by pulling back of spacer
KR100397913B1	2003-12-18	Local silicidation methods to form shallow source / drain junctions
JP4748408B2	2011-08-17	Method for forming metal silicide layer of semiconductor device
US5550084A	1996-08-27	Integrated circuit fabrication using a metal silicide having a sputterdeposited metal nitride layer
US5834846A	1998-11-10	Semiconductor device with contact structure and method of manufacturing the same
US20010046765A1	2001-11-29	Method for producing a barrier layer in an electronic component and method for producing an electronic component with a barrier layer
EP1509947B1	2006-03-22	Nickel silicide with reduced interface roughness

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
JP13698892A	1992-05-28	1992-05-28	Connection hole filling method

Applications Claiming Priority (1)

Application	Filing date	Title
JP13698892A	1992-05-28	Connection hole filling method

Legal Events

Date	Code	Title	Description
2004-07-13	LAPS	Cancellation because of no payment of annual fees	

Concepts

machine-extracted

Download Filter table

Name	Image	Sections	Count	Query match
hole materials		title,claims,description	99	0.000
silicon		claims,description	67	0.000
silicon	Si	claims,description	65	0.000
silicon		claims,description	65	0.000
metal		claims,description	62	0.000

metals	claims,description	62	0.000
substrates	claims,description	60	0.000
silicides	claims,description	34	0.000
silicide(4-)	claims,description	32	0.000
Si^{4}			
interlayers	claims,description	22	0.000
patterning	claims,description	22	0.000
materials	claims,description	14	0.000
deposition	claims,description	11	0.000
cobalt	claims,description	10	0.000
heat treatment	claims,description	9	0.000
transition metals	claims,description	8	0.000
transition metals	claims,description	8	0.000
reactants	claims,description	5	0.000
cobalt	claims,description	3	0.000
cobalt	claims,description	2	0.000
Co			
stabilizing	claims	1	0.000

Show all concepts from the description section

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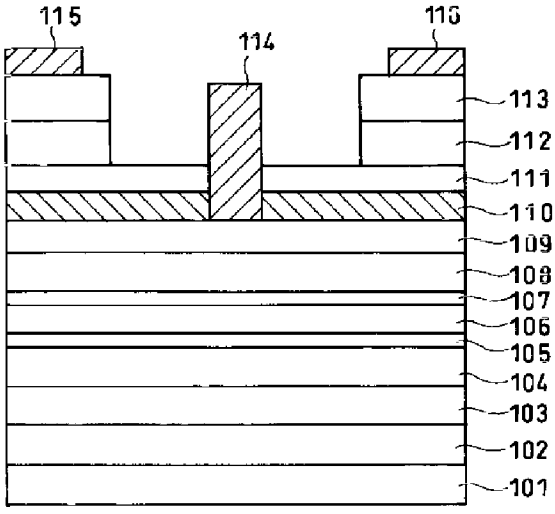
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(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号
(72)発明者　加藤　武彦
東京都港区芝五丁目７番１号　日本電気株式会社内
(74)代理人　100088812
弁理士　▲柳▼川　信

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(54)【発明の名称】　電界効果トランジスタ及びその製造方法

(57)【要約】
【課題】　キャップ層からチャネル層へのコンタクト抵抗を低減すること。
【解決手段】　電子供給層（ショットキ層）１０８上部にショットキゲートコンタクト層１０９を介して超格子層１１０を積層する。これによりＧａＡｓ埋め込み層１１１との界面で起こるコンダクションバンドの曲がりが小さくなり、この部分におけるシート抵抗が低減される。又、ゲートショットキ直下においてはゲートリセス形成時に超格子層１１０層は削れているためショットキ層形成に効いてくるφＢは$Al_{0.2}$ $Ga_{0.8}$ Ａｓの値をとる。以上の結果、０．１Ω・ｍｍオン抵抗が低減される。



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【特許請求の範囲】

【請求項１】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第２のＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含むことを特徴とする電界効果トランジスタ。

【請求項２】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＧａＡｓ層、第２のＡｌＧａＡｓ層、第３のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第２、第３のＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記ＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含むことを特徴とする電界効果トランジスタ。

【請求項３】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第２ＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記ＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含み、かつ前記第２ＡｌＧａＡｓ層はＡｌ組成比が前記キャップ層から前記ＧａＡｓ層方向に順次高くなる傾斜構造に形成されることを特徴とする電界効果トランジスタ。

【請求項４】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、第２のＡｌＧａＡｓ層、ＧａＡｓ層、第３のＡｌＧａＡｓ層、第４のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第３、第４のＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記第２のＡｌＧａＡｓ層及びＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含むことを特徴とする電界効果トランジスタ。

【請求項５】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層、第３のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第２、第３のＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含むことを特徴とする電界効果トランジスタ。

【請求項６】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、第２のＡｌＧａＡｓ層、ＧａＡｓ層、第３のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第３のＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記第１、第２のＡｌＧａＡｓ層及びＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含み、かつ前記第３のＡｌＧａＡｓ層はＡｌ組成比が前記キャップ層から前記ＧａＡｓ層方向に順次高くなる傾斜構造に形成されることを特徴とする電界効果トランジスタ。

【請求項７】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第２のＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含み、かつ前記第２のＡｌＧａＡｓ層はＡｌ組成比が前記キャップ層から前記ＧａＡｓ層方向に順次高くなる傾斜構造に形成されることを特徴とする電界効果トランジスタ。

【請求項８】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層する第１ステップと、この第１ステップの次に前記第２のＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記第２のリセス内にゲート電極を設ける第４ステップとを含むことを特徴とする電界効果トランジスタの製造方法。

【請求項９】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＧａＡｓ層、第２のＡｌＧａＡｓ層、第３のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層する第１ステップと、この第１ステップの次に前記第２、第３のＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記Ｇａ

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Ａｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記２のリセス内にゲート電極を設ける第４ステップとを含むことを特徴とする電界効果トランジスタの製造方法。

【請求項１０】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層する第１ステップと、この第１ステップの次に前記第２ＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記ＧａＡｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記第２のリセス内にゲート電極を設ける第４ステップとを含み、かつ前記第２ＡｌＧａＡｓ層はＡｌ組成比が前記キャップ層から前記ＧａＡｓ層方向に順次高くなる傾斜構造に形成されることを特徴とする電界効果トランジスタの製造方法。

【請求項１１】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、第２のＡｌＧａＡｓ層、ＧａＡｓ層、第３のＡｌＧａＡｓ層、第４のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層する第１ステップと、この第１ステップの次に前記第３、第４のＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記第２のＡｌＧａＡｓ層及びＧａＡｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記第２のリセス内にゲート電極を設ける第４ステップとを含むことを特徴とする電界効果トランジスタの製造方法。

【請求項１２】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層、第３のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層する第１ステップと、この第１ステップの次に前記第２、第３のＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記第２のリセス内にゲート電極を設ける第４ステップとを含むことを特徴とする電界効果トランジスタの製造方法。

【請求項１３】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、第２のＡｌＧａＡｓ層、ＧａＡｓ層、第３のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層第１ステップと、この第１ステップの次に前記第３のＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記第１、第２のＡｌＧａＡｓ層及びＧａＡｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記第２のリセス内にゲート電極を設ける第４ステップとを含み、かつ前記第３のＡｌＧａＡｓ層はＡｌ組成比が前記キャップ層から前記ＧａＡｓ層方向に順次高くなる傾斜構造に形成されることを特徴とする電界効果トランジスタの製造方法。

【請求項１４】　ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層する第１ステップと、この第１ステップの次に前記第２のＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記第２のリセス内にゲート電極を設ける第４ステップとを含み、かつ前記第２のＡｌＧａＡｓ層はＡｌ組成比が前記キャップ層から前記ＧａＡｓ層方向に順次高くなる傾斜構造に形成されることを特徴とする電界効果トランジスタの製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は電界効果トランジスタ（Ｆｉｅｌｄ　Ｅｆｆｅｃｔ　Ｔｒａｎｓｉｓｔｏｒ；「ＦＥＴ」）及びその製造方法に関し、特にヘテロ接合の電界効果トランジスタ及びその製造方法に関する。

【０００２】

【従来の技術】この種の従来の技術の一例が「電子情報通信学会１９９６年エレクトロニクスソサエティ大会公園論文集２：吉田直人、片山秀昭、井上晃、林一夫、中本隆博、浅田智之、采女豊、谷野憲之、山内真秀著，８０頁１８行目及び図１，発行年月日１９９６年８月３０日」に開示されている。

【０００３】ＧａＡｓＦＥＴは高周波素子として広く一般に使用されている。特にその高出力素子においてはソース抵抗低減やゲート耐圧確保のため、多段リセス構造が採用されている。

【０００４】なお、「リセス構造」とはソースとドレイン領域にマスクを施し、ゲート近辺をエッチングにより堀込んだ構造をいい、「多段リセス構造」とは複数段に堀込んだ構造をいう。

【０００５】そのような多段リセス構造は例えば、ＧａＡｓ／ＡｌＧａＡｓ積層構造の選択エッチングを用いて形成される。図１８は従来の電界効果トランジスタの断面図である。図１８中の８０１は半絶縁性ＧａＡｓ基

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板、８０２は膜厚４００nmのＧａＡｓバッファ層、８０３はアンドープ$Al_{0.2}Ga_{0.8}As$バッファー層、８０４はＳｉドープ$Al_{0.2}Ga_{0.8}As$電子供給層、８０５はアンドープ$Al_{0.2}Ga_{0.8}As$スペーサー層、８０６はアンドープ$In_{0.2}Ga_{0.8}As$チャネル層、８０７はアンドープ$Al_{0.2}Ga_{0.8}As$スペーサー層、８０８はＳｉドープ$Al_{0.2}Ga_{0.8}As$電子供給層、８０９はアンドープ$Al_{0.2}Ga_{0.8}As$ゲートコンタクト層、８１０はＧａＡｓゲート埋め込み層、８１１はＳｉドープ$Al_{0.2}Ga_{0.8}As$ワイドリセスストッパ層、８１２はＳｉドープＧａＡｓキャップ層、８１３はゲート電極、８１４はソース電極、８１５はドレイン電極である。

【０００６】このようなリセス構造は、まず、第１リセス（ワイドリセス）部８２１が開口したマスク（不図示）を形成し、ＡｌＧａＡｓ層８１１をワイドリセスストッパとしてＧａＡｓ層８１２を選択エッチングする。次に第２リセス（ゲートリセス）部８２２が開口したマスク（不図示）を形成しＡｌＧａＡｓ層８０９をゲートリセスストッパ層としてＧａＡｓ層８１０を選択エッチングすることにより形成する。

【０００７】この図１８中に従来構造を有するＦＥＴの各部分に生じる分布常数的な電気抵抗を模式的に示す。Ｒ１はオーミック電極（ソース電極８１４及びドレイン電極８１５）からキャップ層８１２へのコンタクト抵抗、Ｒ２はキャップ層８１２からチャネル層８０６へのコンタクト抵抗、Ｒ３はゲート８１３の下のシート抵抗である。そして、ＦＥＴのオン抵抗はソース電極８１４からドレイン電極８１５までの全抵抗である。

【０００８】他の１の文献「１９９６年ＩＥＥＥ　ＧａＡｓ　ＩＣ　Ｓｙｍｐｏｓｉｕｍ頁１１９」に載っているように低いオン抵抗は低電圧動作において高出力、高効率を得るために重要である。

【０００９】なお、この種の従来技術の他の例が特開平９－１０２６００号公報及び特許第２６２６２１３号公報に開示されている。

【００１０】

【発明が解決しようとする課題】しかし、従来の技術ではキャップ層からチャネル層へのコンタクト抵抗Ｒ２が高いという欠点があった。その理由は、多段リセス構造を形成するために用いているＡｌＧａＡｓストッパ層のポテンシャルバリアが高く、キャップ層からチャネル層へのトンネル確率が小さいためである。しかし、選択エッチングのストッパ層として用いているためこの層を薄くすることは難しい。

【００１１】そこで本発明の目的はキャップ層からチャネル層へのコンタクト抵抗を低減することが可能な電界効果トランジスタ及びその製造方法を提供することにある。

【００１２】

【課題を解決するための手段】前記課題を解決するために本発明は、ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第２のＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含んで電界効果トランジスタを構成したことを特徴とする。

【００１３】又、本発明による他の発明は、ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層する第１ステップと、この第１ステップの次に前記第２のＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記第２のリセス内にゲート電極を設ける第４ステップとを含んで電界効果トランジスタの製造方法を構成したことを特徴とする。

【００１４】本発明及び本発明による他の発明によれば、第１のＡｌＧａＡｓ層の上部にＡｌＧａＡｓ／ＧａＡｓ超格子層を積層したため、コンタクト抵抗を低減することが可能となる。

【００１５】

【発明の実施の形態】以下、本発明の実施の形態について添付図面を参照しながら説明する。まず、第１の実施の形態から説明する。第１の実施の形態は請求項１及び８の発明に関するものである。

【００１６】図１は本発明の第１の実施の形態の構成を示す断面図、図２～図４は同形態の製造過程における断面図、図５は同形態の製造工程を示すフローチャートである。以下、図１～図５を参照して第１の実施の形態について説明する。

【００１７】まず、半絶縁性ＧａＡｓ基板１０１上に、膜厚４００nmのＧａＡｓバッファ層１０２、膜厚１００nmのアンドープ$Al_{0.2}Ga_{0.8}As$バッファー層１０３、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚４nmの$Al_{0.2}Ga_{0.8}As$電子供給層１０４、膜厚２nmのアンドープ$Al_{0.2}Ga_{0.8}As$スペーサ層１０５、膜厚１５nmのアンドープ$In_{0.2}Ga_{0.8}As$チャネル層１０６、膜厚２nmのアンドープ$Al_{0.2}Ga_{0.8}As$スペーサ層１０７、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚９nmの$Al_{0.2}Ga_{0.8}As$

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電子供給層108、膜厚17nmのアンドープ$Al_{0.2}Ga_{0.8}As$ショットキゲートコンタクト層109、$Al_{0.2}Ga_{0.8}As$（0.5nm）／GaAs（0.5nm）×3周期の超格子層110、膜厚30nmのアンドープGaAs埋め込み層111、Siを$4\times10^{18}cm^{-3}$ドープした膜厚6nmの$Al_{0.2}Ga_{0.8}As$ワイドリセスストッパ層112、Siを$4\times10^{18}cm^{-3}$ドープした膜厚100nmのGaAsキャップ層113を順次分子線成長法又は有機金属気相成長法によりエピタキシャル成長する（S1）。図2はエピタキシャル成長後の構造を示している。

【0018】次に、図3に示すように作成したウエハ上にワイドリセス部が開口したマスク901を形成し（S2）、$Al_{0.2}Ga_{0.8}As$ワイドリセスストッパ層112をストッパ層に用いてGaAsキャップ層113を選択的にエッチングする（S3）。このような選択エッチングはECRエッチング装置又はRIE装置を用い、ハロゲン元素として塩素のみを含んだ塩化ガスとフッ素のみを含んだフッ化物ガスとの混合ガス（例えば$BCl_3 + SF_6$ 等）を導入したドライエッチングにより可能である。

【0019】そのマスクを除去後、図4に示すように新たにゲートリセス部が開口したマスク902を形成し（S4）、$Al_{0.2}Ga_{0.8}As$ゲートコンタクト層109をストッパ層に用いてGaAsゲート埋込み層110、$Al_{0.2}Ga_{0.8}As$（0.5nm）／GaAs（0.5nm）×3周期の超格子層110を選択的にエッチングする（S5）。

【0020】次に、エッチングの結果露出した$Al_{0.2}Ga_{0.8}As$ゲートコンタクト層109の露出部109aにゲート電極114を形成し（S6）、AuGeを蒸着リフトオフ及びアロイ（例えば400℃／min）を行い、オーミック電極としてソース電極115及びドレイン電極116を形成する（S7）。

【0021】第1の実施の形態の構造によれば、ソースドレイン間ではポテンシャルバリアとして効いてくるAlGaAsショットキ層108上部にAlGaAs／GaAs超格子層110が積層されていることによりGaAs埋め込み層111との界面で起こるコンダクションバンドの曲がりが小さくなり、この部分におけるシート抵抗が低減される。又、ゲートショットキ直下においてはゲートリセス形成時にAlGaAs／GaAs超格子層110層は削れているためショットキ層形成に効いてくるφB（ショットキ障壁高さ；単位エレクトロンボルト，以下同様）は$Al_{0.2}Ga_{0.8}As$の値をとる。以上の結果、0.1Ω・mmオン抵抗が低減される。

【0022】次に、第2の実施の形態について説明する。第2の実施の形態は請求項2及び9の発明に関するものである。

【0023】図6は本発明の第2の実施の形態の構成を示す断面図、図7は同形態の製造工程を示すフローチャートである。なお、以後の実施の形態において同形態の製造過程における断面図は図示を省略する。以下、図6及び図7を参照して第2の実施の形態について説明する。

【0024】半絶縁性GaAs基板201上に、膜厚400nmのGaAsバッファ層202、膜厚100nmのアンドープ$Al_{0.2}Ga_{0.8}As$バッファー層203、Siを$4\times10^{18}cm^{-3}$ドープした膜厚4nmの$Al_{0.2}Ga_{0.8}As$電子供給層204、膜厚2nmのアンドープ$Al_{0.2}Ga_{0.8}As$スペーサ層205、膜厚15nmのアンドープ$In_{0.2}Ga_{0.8}As$チャネル層206、膜厚2nmのアンドープ$Al_{0.2}Ga_{0.8}As$スペーサ層207、Siを$4\times10^{18}cm^{-3}$ドープした膜厚9nmの$Al_{0.2}Ga_{0.8}As$電子供給層208、膜厚17nmのアンドープ$Al_{0.2}Ga_{0.8}As$ショットキゲートコンタクト層209、膜厚30nmのアンドープGaAs埋め込み層210、Siを$4\times10^{18}cm^{-3}$ドープした膜厚3nmの$Al_{0.2}Ga_{0.8}As$ワイドリセスストッパ層211、Siを$4\times10^{18}cm^{-3}$ドープした膜厚3nmの$Al_{0.1}Ga_{0.9}As$層212、Siを$4\times10^{18}cm^{-3}$ドープした膜厚100nmのGaAsキャップ層213を順次分子線成長法又は有機金属気相成長法によりエピタキシャル成長する（S11）。

【0025】作成したウェハ上にワイドリセスが開口したマスクを形成し（S12）、$Al_{0.2}Ga_{0.8}As$ワイドリセスストッパ層211をストッパ層に用いて$Al_{0.1}Ga_{0.9}As$層212、GaAsキャップ層213層を選択的にエッチングする（S13）。

【0026】このような選択エッチングはECRエッチング装置又はRIE装置を用い、ハロゲン元素として塩素のみを含んだ塩化ガスとフッ素のみを含んだフッ化物ガスとの混合ガス（例えば$BCl_3 + SF_6$ 等）を導入したドライエッチングにより可能である。

【0027】そのマスクを除去後、新たにゲートリセス部が開口したマスクを形成し（S14）、$Al_{0.2}Ga_{0.8}As$ゲートコンタクト層209をストッパ層に用いてGaAsゲート埋め込み層210を選択的にエッチングする（S15）。表面に露出したゲートコンタクト層209上にゲート電極214を形成する（S16）。次にAuGeを蒸着リフトオフ及びアロイ（例えば400℃／min）を行い、オーミック電極として、ソース電極215及びドレイン電極216を形成する（S17）。

【0028】第2の実施の形態の構造によれば、AlGaAsワイドリセスストッパ層が二段構造になっている（211層と212層）ことによりこの部分におけるシート抵抗が低減される。以上の結果、0.05Ω・mmオン抵抗が低減される。

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【００２９】次に、第３の実施の形態について説明する。第３の実施の形態は請求項３及び１０の発明に関するものである。

【００３０】図８は本発明の第３の実施の形態の構成を示す断面図、図９は同形態の製造工程を示すフローチャートである。以下、図８及び図９を参照して第３の実施の形態について説明する。

【００３１】半絶縁性ＧａＡｓ基板３０１上に、膜厚４００ｎｍのＧａＡｓバッファ層３０２、膜厚１００ｎｍのアンドープ$Al_{0.2}Ga_{0.8}As$バッファー層３０３、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚４ｎｍの$Al_{0.2}Ga_{0.8}As$電子供給層３０４、膜厚２ｎｍのアンドープ$Al_{0.2}Ga_{0.8}As$スペーサ層３０５、膜厚１５ｎｍのアンドープ$In_{0.2}Ga_{0.8}As$チャネル層３０６、膜厚２ｎｍのアンドープ$Al_{0.2}Ga_{0.8}As$スペーサ層３０７、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚９ｎｍの$Al_{0.2}Ga_{0.8}As$電子供給層３０８、膜厚１７ｎｍのアンドープ$Al_{0.2}Ga_{0.8}As$ショットキゲートコンタクト層３０９、膜厚３０ｎｍのアンドープＧａＡｓ埋め込み層３１０、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚３ｎｍの$Al_{0.2}Ga_{0.8}As$層３１１、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚０．５ｎｍの$Al_{0.18}Ga_{0.82}As$層３１２、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚０．５ｎｍの$Al_{0.15}Ga_{0.85}As$層３１３、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚０．５ｎｍの$Al_{0.12}Ga_{0.88}As$層３１４、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚０．５ｎｍの$Al_{0.09}Ga_{0.91}As$層３１５、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚０．５ｎｍの$Al_{0.06}Ga_{0.94}As$層３１６、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚０．５ｎｍの$Al_{0.03}Ga_{0.97}As$層３１７、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚１００ｎｍのＧａＡｓキャップ層３１８を順次分子線成長法又は有機金属気相成長法によりエピタキシャル成長する（Ｓ２１）。

【００３２】作成したウェハ上にワイドリセスが開口したマスクを形成し（Ｓ２２）、$Al_{0.2}Ga_{0.8}As$ワイドリセスストッパ層３１１をストッパ層に用いてＡｌＧａＡｓ層３１２～３１７、ＧａＡｓキャップ層３１３層を選択的にエッチングする（Ｓ２３）。

【００３３】このような選択エッチングはＥＣＲエッチング装置又はＲＩＥ装置を用い、ハロゲン元素として塩素のみを含んだ塩化ガスとフッ素のみを含んだフッ化物ガスとの混合ガス（例えば$BCl_3 + SF_6$等）を導入したドライエッチングにより可能である。

【００３４】そのマスクを除去後、新たにゲートリセス部が開口したマスクを形成し（Ｓ２４）、$Al_{0.2}Ga_{0.8}As$ゲートコンタクト層３０９をストッパ層に用いてＧａＡｓゲート埋め込み層３１０を選択的にエッチングする（Ｓ２５）。

【００３５】表面に露出したゲートコンタクト層３０９上にゲート電極３１９を形成する（Ｓ２６）。次にＡｕＧｅを蒸着リフトオフ及びアロイ（例えば４００℃／ｍｉｎ）を行い、オーミック電極として、ソース電極３２０及びドレイン電極３２１を形成する（Ｓ２７）。

【００３６】第３の実施の形態の構造によれば、ＡｌＧａＡｓワイドリセスストッパ層が二段構造になっている（３１１層と３１２～３１７層）ことによりこの部分におけるシート抵抗が低減される。以上の結果、０．０５Ω・ｍｍオン抵抗が低減される。

【００３７】次に、第４の実施の形態について説明する。第４の実施の形態は請求項４及び１１の発明に関するものである。

【００３８】図１０は本発明の第４の実施の形態の構成を示す断面図、図１１は同形態の製造工程を示すフローチャートである。以下、図１０及び図１１を参照して第４の実施の形態について説明する。

【００３９】半絶縁性ＧａＡｓ基板４０１上に、膜厚４００ｎｍのＧａＡｓバッファ層４０２、膜厚１００ｎｍのアンドープ$Al_{0.2}Ga_{0.8}As$バッファー層４０３、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚４ｎｍの$Al_{0.2}Ga_{0.8}As$電子供給層４０４、膜厚２ｎｍのアンドープ$Al_{0.2}Ga_{0.8}As$スペーサ層４０５、膜厚１５ｎｍのアンドープ$In_{0.2}Ga_{0.8}As$チャネル層４０６、膜厚２ｎｍのアンドープ$Al_{0.2}Ga_{0.8}As$スペーサ層４０７、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚９ｎｍの$Al_{0.2}Ga_{0.8}As$電子供給層４０８、膜厚１７ｎｍのアンドープ$Al_{0.2}Ga_{0.8}As$ショットキゲートコンタクト層４０９、膜厚３ｎｍのアンドープ$Al_{0.1}Ga_{0.9}As$層４１０、膜厚３０ｎｍのアンドープＧａＡｓ埋め込み層４１１、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚６ｎｍのＳｉを$4\times10^{18}cm^{-3}$ドープした膜厚３ｎｍの$Al_{0.2}Ga_{0.8}As$ワイドリセスストッパ層４１２、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚３ｎｍの$Al_{0.1}Ga_{0.9}AsAs$層４１３、Ｓｉを$4\times10^{18}cm^{-3}$ドープした膜厚１００ｎｍのＧａＡｓキャップ層４１４を順次分子線成長法又は有機金属気相成長法によりエピタキシャル成長する（Ｓ３１）。

【００４０】作成したウェハ上にワイドリセスが開口したマスクを形成し（Ｓ３２）、$Al_{0.2}Ga_{0.8}As$ワイドリセスストッパ層４１２をストッパ層に用いてＧａＡｓキャップ層４１４層、ＡｌＧａＡｓ４１３層を選択的にエッチングする（Ｓ３３）。

【００４１】このような選択エッチングはＥＣＲエッチング装置又はＲＩＥ装置を用い、ハロゲン元素として塩素のみを含んだ塩化ガスとフッ素のみを含んだフッ化物ガスとの混合ガス（例えば$BCl_3 + SF_6$等）を導入したドライエッチングにより可能である。

【００４２】そのマスクを除去後、新たにゲートリセス部が開口したマスクを形成し（Ｓ３４）、$Al_{0.2}Ga_{0.8}As$

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$Ga_{0.8}$ Asゲートコンタクト層409をストッパ層に用いてGaAsゲート埋め込み層411、$Al_{0.1}$ $Ga_{0.9}$ As層410を選択的にエッチングする（S35）。

【0043】表面に露出したゲートコンタクト層409上にゲート電極415を形成する（S36）。次にAuGeを蒸着リフトオフ及びアロイ（例えば400℃／min）を行い、オーミック電極として、ソース電極416及びドレイン電極417を形成する（S37）。

【0044】第4の実施の形態の構造によれば、ソースドレイン間ではポテンシャルバリアとして効いてくるAlGaAsショットキ層が二段構造になっている（412層と413層）ことによりこの部分におけるシート抵抗が低減される。又、ゲートショットキ直下においてはゲートリセス形成時にショットキ層410層は削れているためショットキ層形成に効いてくるφBは$Al_{0.2}$ $Ga_{0.8}$ Asの値をとる。以上の結果、0.15Ω・mmオン抵抗が低減される。

【0045】次に、第5の実施の形態について説明する。第5の実施の形態は請求項5及び12の発明に関するものである。

【0046】図12は本発明の第5の実施の形態の構成を示す断面図、図13は同形態の製造工程を示すフローチャートである。以下、図12及び図13を参照して第5の実施の形態について説明する。

【0047】半絶縁性GaAs基板501上に、膜厚400nmのGaAsバッファ層502、膜厚100nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asバッファー層503、Siを$4\times10^{18}cm^{-3}$ドープした膜厚4nmの$Al_{0.2}$ $Ga_{0.8}$ As電子供給層504、膜厚2nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asスペーサ層505、膜厚15nmのアンドープ$In_{0.2}$ $Ga_{0.8}$ Asチャネル層506、膜厚2nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asスペーサ層507、Siを$4\times10^{18}cm^{-3}$ドープした膜厚9nmの$Al_{0.2}$ $Ga_{0.8}$ As電子供給層508、膜厚17nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asショットキゲートコンタクト層509、$Al_{0.2}$ $Ga_{0.8}$ As（0.5nm）／GaAs（0.5nm）×3周期の超格子層510、膜厚30nmのアンドープGaAs埋め込み層511、Siを$4\times10^{18}cm^{-3}$ドープした膜厚6nmのSiを$4\times10^{18}cm^{-3}$ドープした膜厚3nmの$Al_{0.2}$ $Ga_{0.8}$ Asワイドリセスストッパ層512、Siを$4\times10^{18}cm^{-3}$ドープした膜厚3nmの$Al_{0.1}$ $Ga_{0.9}$ As層513、Siを$4\times10^{18}cm^{-3}$ドープした膜厚100nmのGaAsキャップ層514を順次分子線成長法又は有機金属気相成長法によりエピタキシャル成長する（S41）。

【0048】作成したウェハ上にワイドリセスが開口したマスクを形成し（S42）、$Al_{0.2}$ $Ga_{0.8}$ Asワイドリセスストッパ層512をストッパ層に用いてGaAsキャップ層514層、AlGaAs層513を選択的にエッチングする（S43）。

【0049】このような選択エッチングはECRエッチング装置又はRIE装置を用い、ハロゲン元素として塩素のみを含んだ塩化ガスとフッ素のみを含んだフッ化物ガスとの混合ガス（例えばBCl_3 + SF_6 等）を導入したドライエッチングにより可能である。

【0050】そのマスクを除去後、新たにゲートリセス部が開口したマスクを形成し（S44）、$Al_{0.2}$ $Ga_{0.8}$ Asゲートコンタクト層509をストッパ層に用いてGaAsゲート埋め込み層511、$Al_{0.2}$ $Ga_{0.8}$ As（0.5nm）／GaAs（0.5nm）×3周期の超格子層510を選択的にエッチングする（S45）。

【0051】表面に露出したゲートコンタクト層509上にゲート電極515を形成する（S46）。次にAuGeを蒸着リフトオフ及びアロイ（例えば400℃／min）を行い、オーミック電極として、ソース電極516及びドレイン電極517を形成する（S47）。

【0052】第5の実施の形態の構造によれば、ソースドレイン間ではポテンシャルバリアとして効いてくるAlGaAsショットキ層が二段構造になっている（512層と513層）ことによりこの部分におけるシート抵抗が低減される。又、ゲートショットキ直下においてはゲートリセス形成時にAlGaAs層510層は削れているためショットキ層形成に効いてくるφBは$Al_{0.2}$ $Ga_{0.8}$ Asの値をとる。以上の結果、0.15Ω・mmオン抵抗が低減される。

【0053】次に、第6の実施の形態について説明する。第6の実施の形態は請求項6及び13の発明に関するものである。

【0054】図14は本発明の第6の実施の形態の構成を示す断面図、図15は同形態の製造工程を示すフローチャートである。以下、図14及び図15を参照して第6の実施の形態について説明する。

【0055】半絶縁性GaAs基板601上に、膜厚400nmのGaAsバッファ層602、膜厚100nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asバッファー層603、Siを$4\times10^{18}cm^{-3}$ドープした膜厚4nmの$Al_{0.2}$ $Ga_{0.8}$ As電子供給層604、膜厚2nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asスペーサ層605、膜厚15nmのアンドープ$In_{0.2}$ $Ga_{0.8}$ Asチャネル層606、膜厚2nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asスペーサ層607、Siを$4\times10^{18}cm^{-3}$ドープした膜厚9nmの$Al_{0.2}$ $Ga_{0.8}$ As電子供給層608、膜厚17nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asショットキゲートコンタクト層609、膜厚3nmのアンドープ$Al_{0.1}$ $Ga_{0.9}$ As層610、膜厚30nmのアンドープGaAs埋め込み層611、Siを$4\times10^{18}cm^{-3}$ドープした膜厚3nmのAl

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$_{0.2}$ $Ga_{0.8}$ As層612、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.18}Ga_{0.82}As$層613、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.15}Ga_{0.85}As$層614、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.12}Ga_{0.88}As$層615、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.09}Ga_{0.91}As$層616、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.06}Ga_{0.94}As$層617、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.03}Ga_{0.97}As$層618、Siを$4\times10^{18}cm^{-3}$ドープした膜厚100nmのGaAsキャップ層619を順次分子線成長法又は有機金属気相成長法によりエピタキシャル成長する（S51）。

【0056】作成したウェハ上にワイドリセスが開口したマスクを形成し（S52）、$Al_{0.2}$ $Ga_{0.8}$ Asワイドリセスストッパ層612をストッパ層に用いてGaAsキャップ層614層、AlGaAs層613～618を選択的にエッチングする（S53）。

【0057】このような選択エッチングはECRエッチング装置又はRIE装置を用い、ハロゲン元素として塩素のみを含んだ塩化ガスとフッ素のみを含んだフッ化物ガスとの混合ガス（例えばBCl_3 + SF_6 等）を導入したドライエッチングにより可能である。

【0058】そのマスクを除去後、新たにゲートリセス部が開口したマスクを形成し（S54）、$Al_{0.2}$ $Ga_{0.8}$ Asゲートコンタクト層609をストッパ層に用いてGaAsゲート埋め込み層611、$Al_{0.1}$ $Ga_{0.9}$ As層610を選択的にエッチングする（S55）。

【0059】表面に露出したゲートコンタクト層609上にゲート電極620を形成する（S56）。次にAuGeを蒸着リフトオフ及びアロイ（例えば400℃/min）を行い、オーミック電極として、ソース電極621及びドレイン電極622を形成する（S57）。

【0060】第6の実施の形態の構造によれば、ソースドレイン間ではポテンシャルバリアとして効いてくるAlGaAsショットキ層が二段構造になっている（612層と613～618層）ことによりこの部分におけるシート抵抗が低減される。又、ゲートショットキ直下においてはゲートリセス形成時にAlGaAs層610層は削れているためショットキ層形成に効いてくるϕBは$Al_{0.2}$ $Ga_{0.8}$ Asの値をとる。以上の結果、0.15Ω·mmオン抵抗が低減される。

【0061】次に、第7の実施の形態について説明する。第7の実施の形態は請求項7及び14の発明に関するものである。

【0062】図16は本発明の第7の実施の形態の構成を示す断面図、図17は同形態の製造工程を示すフローチャートである。以下、図16及び図17を参照して第7の実施の形態について説明する。

【0063】半絶縁性GaAs基板701上に、膜厚400nmのGaAsバッファ層702、膜厚100nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asバッファー層703、Siを$4\times10^{18}cm^{-3}$ドープした膜厚4nmの$Al_{0.2}$ $Ga_{0.8}$ As電子供給層704、膜厚2nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asスペーサ層705、膜厚15nmのアンドープ$In_{0.2}$ $Ga_{0.8}$ Asチャネル層706、膜厚2nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asスペーサ層707、Siを$4\times10^{18}cm^{-3}$ドープした膜厚9nmの$Al_{0.2}$ $Ga_{0.8}$ As電子供給層708、膜厚17nmのアンドープ$Al_{0.2}$ $Ga_{0.8}$ Asショットキゲートコンタクト層709、$Al_{0.2}$ $Ga_{0.8}$ As（0.5nm）/GaAs（0.5nm）×3周期の超格子層710、膜厚30nmのアンドープGaAs埋め込み層711、Siを$4\times10^{18}cm^{-3}$ドープした膜厚3nmの$Al_{0.2}$ $Ga_{0.8}$ As層712、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.18}Ga_{0.82}As$層713、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.15}Ga_{0.85}As$層714、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.12}Ga_{0.88}As$層715、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.09}Ga_{0.91}As$層716、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.06}Ga_{0.94}As$層717、Siを$4\times10^{18}cm^{-3}$ドープした膜厚0.5nmの$Al_{0.03}Ga_{0.97}As$層718、Siを$4\times10^{18}cm^{-3}$ドープした膜厚100nmのGaAsキャップ層719を順次分子線成長法又は有機金属気相成長法によりエピタキシャル成長する（S61）。

【0064】作成したウェハ上にワイドリセスが開口したマスクを形成し（S62）、$Al_{0.2}$ $Ga_{0.8}$ Asワイドリセスストッパ層712をストッパ層に用いてGaAsキャップ層714、AlGaAs層713～718を選択的にエッチングする（S63）。

【0065】このような選択エッチングはECRエッチング装置又はRIE装置を用い、ハロゲン元素として塩素のみを含んだ塩化ガスとフッ素のみを含んだフッ化物ガスとの混合ガス（例えばBCl_3 + SF_6 等）を導入したドライエッチングにより可能である。

【0066】そのマスクを除去後、新たにゲートリセス部が開口したマスクを形成し（S64）、$Al_{0.2}$ $Ga_{0.8}$ Asゲートコンタクト層709をストッパ層に用いてGaAsゲート埋め込み層711、$Al_{0.2}$ $Ga_{0.8}$ As（0.5nm）/GaAs（0.5nm）×3周期の超格子層710を選択的にエッチングする（S65）。

【0067】表面に露出したゲートコンタクト層709上にゲート電極720を形成する（S66）。次にAuGeを蒸着リフトオフ及びアロイ（例えば400℃/min）を行い、オーミック電極として、ソース電極72

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１及びドレイン電極７２２を形成する（Ｓ６７）。

【００６８】第７の実施の形態の構造によれば、ソースドレイン間ではポテンシャルバリアとして効いてくるＡｌＧａＡｓショットキ層が二段構造になっている（７１２層と７１３～７１８層）ことによりこの部分におけるシート抵抗が低減される。又、ゲートショットキ直下においてはセカンドリセス形成時にＡｌＧａＡｓ層７１０層は削れているためショットキ層形成に効いてくるφＢは$Al_{0.2}$ $Ga_{0.8}As$の値をとる。以上の結果、０．１５Ω・ｍｍオン抵抗が低減される。

【００６９】

【発明の効果】本発明によれば、ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層してなり、さらに前記第２のＡｌＧａＡｓ層及びキャップ層中に形成される第１のリセスと、この第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に形成される第２のリセスと、この第２のリセス内に設けられるゲート電極とを含んで電界効果トランジスタを構成したため、第１のＡｌＧａＡｓ層の上部にＡｌＧａＡｓ／ＧａＡｓ超格子層が積層されることになり、これによりコンタクト抵抗を低減することが可能となる。

【００７０】又、本発明による他の発明によれば、ＩｎＧａＡｓ又はＧａＡｓで構成されるチャネル層、第１のＡｌＧａＡｓ層、ＡｌＧａＡｓ／ＧａＡｓ超格子層、ＧａＡｓ層、第２のＡｌＧａＡｓ層及びオーミック電極用のＩｎＧａＡｓ又はＧａＡｓで構成されるキャップ層を順次積層する第１ステップと、この第１ステップの次に前記第２のＡｌＧａＡｓ層及びキャップ層中に第１のリセスを形成する第２ステップと、この第２ステップの次に前記第１のリセスの中でかつ前記ＡｌＧａＡｓ／ＧａＡｓ超格子層及びＧａＡｓ層中に第２のリセスを形成する第３ステップと、この第３ステップの次に前記第２のリセス内にゲート電極を設ける第４ステップとを含んで電界効果トランジスタの製造方法を構成したため、第１のＡｌＧａＡｓ層の上部にＡｌＧａＡｓ／ＧａＡｓ超格子層が積層されることになり、これによりコンタクト抵抗を低減することが可能となる。

【００７１】さらに具体的に説明すると、本発明によれば、第１に従来構造のようにショットキバリア層のＡｌＧａＡｓの組成一定ではなく上記のように間に超格子層を設けることによりポテンシャルバリアが下がりチャネル・ゲート間のコンタクト抵抗を０．１Ω・ｍｍ低減することができる。またこのときゲート電極はＡｌ組成の高い部分にもうけられているため高いφＢを保つことができる。このことにより本発明の構造では高い逆耐圧を保ったまま、電界効果トランジスタの高出力動作、高効率動作が可能となる。

【００７２】第２に、従来構造のようにワイドリセスストッパ層のＡｌＧａＡｓの組成一定ではなく二段構造にすることによりポテンシャルバリアが下がりチャネルゲート間のコンタクト抵抗を０．０５Ω・ｍｍ低減することができる。このことにより電界効果トランジスタの高出力動作、高効率動作が可能となる。

【００７３】第３に、従来構造のようにワイドリセスストッパ層のＡｌＧａＡｓの組成一定ではなく上記のように傾斜Ａｌ組成構造にすることによりポテンシャルバリアが下がりチャネルゲート間のコンタクト抵抗を０．０５Ω・ｍｍ低減することができる。このことにより電界効果トランジスタの高出力動作、高効率動作が可能となる。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態の構成を示す断面図である。

【図２】同形態の製造過程における断面図である。

【図３】同形態の製造過程における断面図である。

【図４】同形態の製造過程における断面図である。

【図５】同形態の製造工程を示すフローチャートである。

【図６】本発明の第２の実施の形態の構成を示す断面図である。

【図７】同形態の製造工程を示すフローチャートである。

【図８】本発明の第３の実施の形態の構成を示す断面図である。

【図９】同形態の製造工程を示すフローチャートである。

【図１０】本発明の第４の実施の形態の構成を示す断面図である。

【図１１】同形態の製造工程を示すフローチャートである。

【図１２】本発明の第５の実施の形態の構成を示す断面図である。

【図１３】同形態の製造工程を示すフローチャートである。

【図１４】本発明の第６の実施の形態の構成を示す断面図である。

【図１５】同形態の製造工程を示すフローチャートである。

【図１６】本発明の第７の実施の形態の構成を示す断面図である。

【図１７】同形態の製造工程を示すフローチャートである。

【図１８】従来の電界効果トランジスタの断面図である。

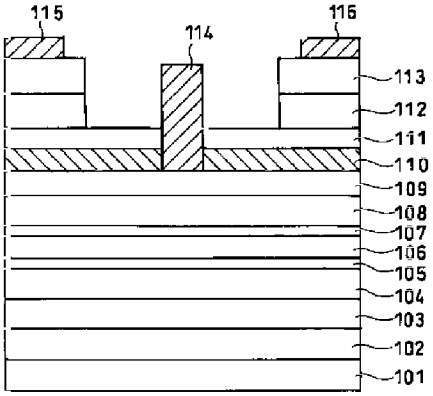
【符号の説明】

１０１　基板

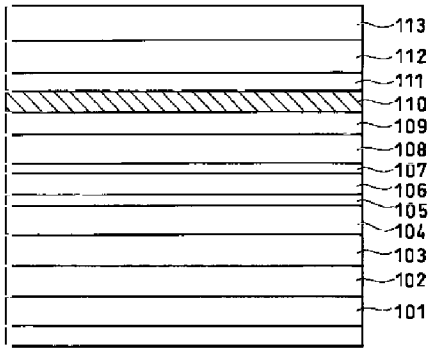
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１０２，１０３　バッファ層
１０４，１０８　電子供給層
１０５，１０７　スペーサ層
１０６　チャネル層
１０９　ショットキゲートコンタクト層
１１０　超格子層
１１１　アンドープＧａＡｓ埋め込み層
１１２　ワイドリセスストッパ層
１１３　キャップ層
１１４　ゲート電極
１１５　ソース電極
１１６　ドレイン電極
２１２　ＡｌＧａＡｓ層
３１２〜３１７　ＡｌＧａＡｓ層
４１０　ＡｌＧａＡｓ層

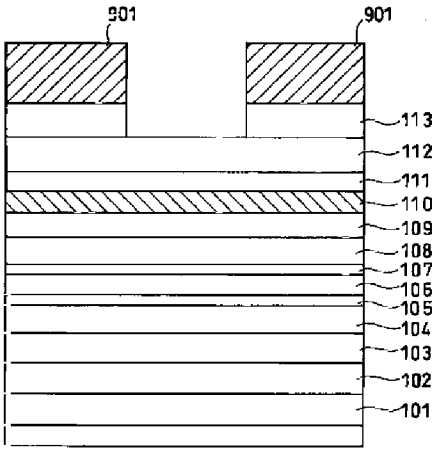
【図１】



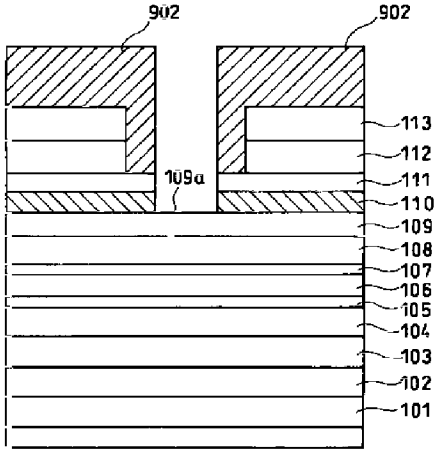
【図２】



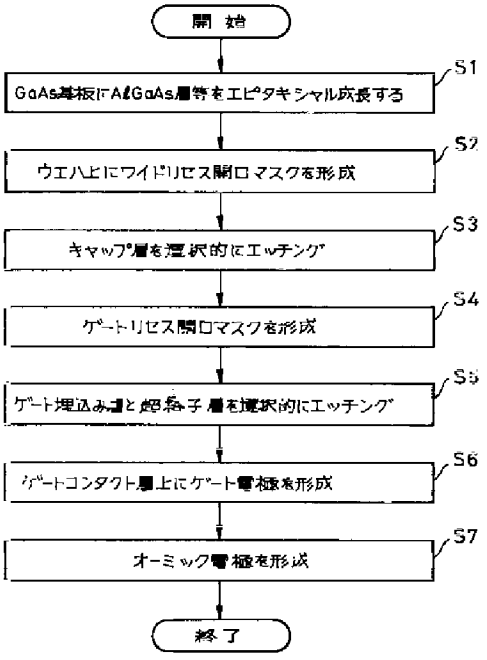
【図３】



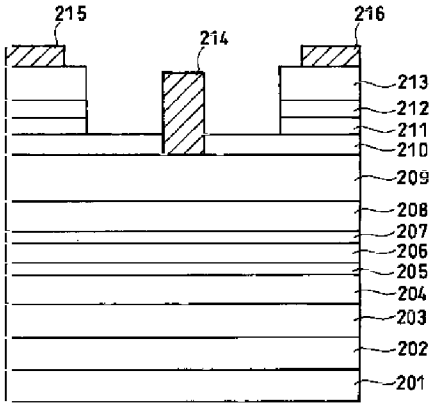
【図４】



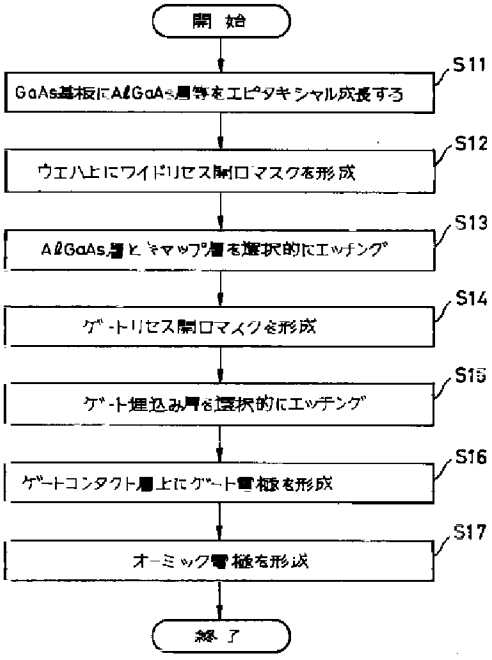
【図5】



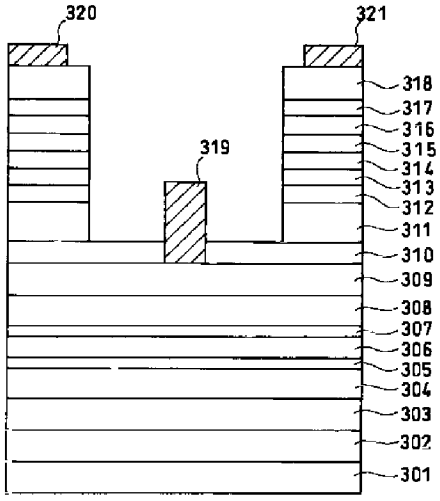
【図6】



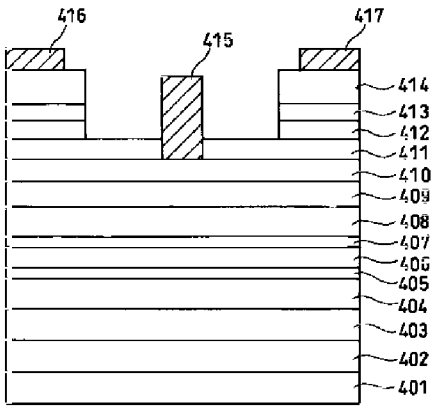
【図7】



【図8】

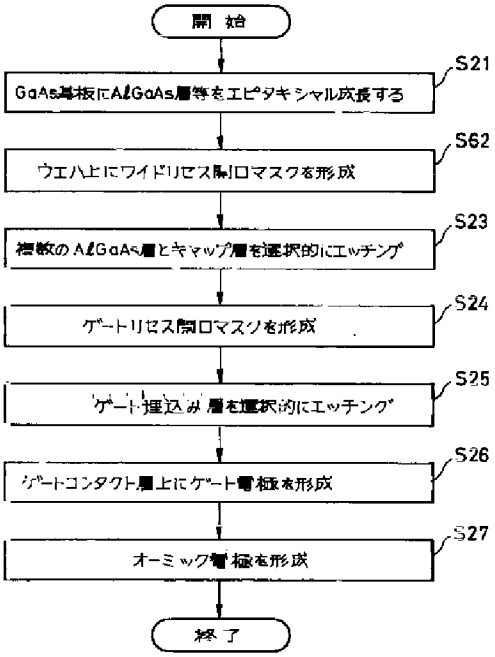


【図10】

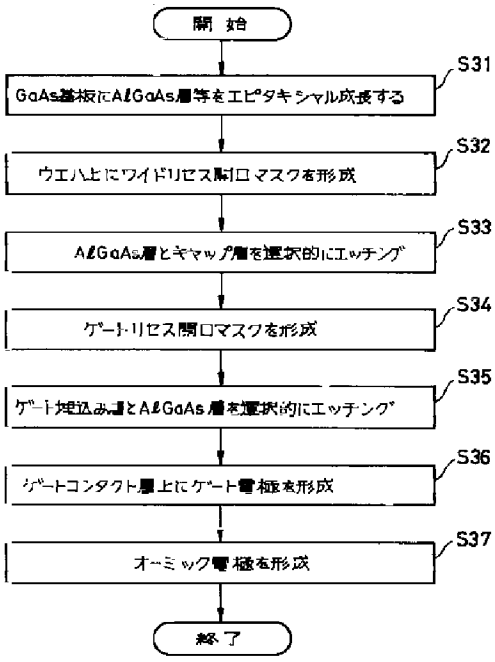


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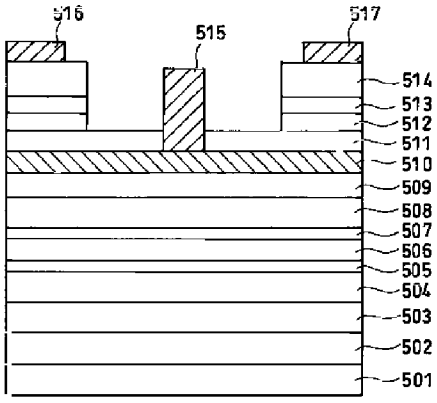
【図9】



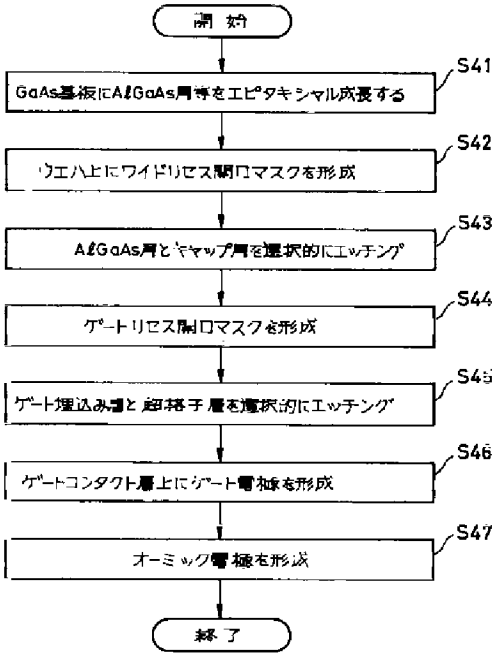
【図11】



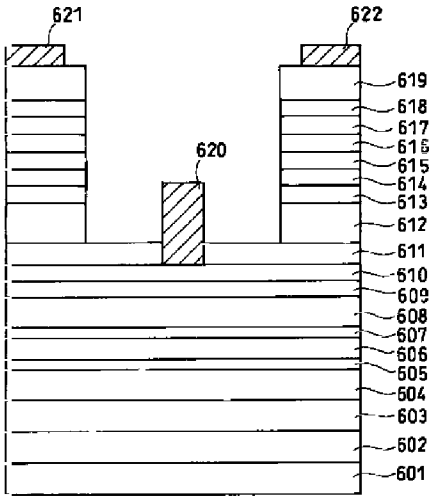
【図12】



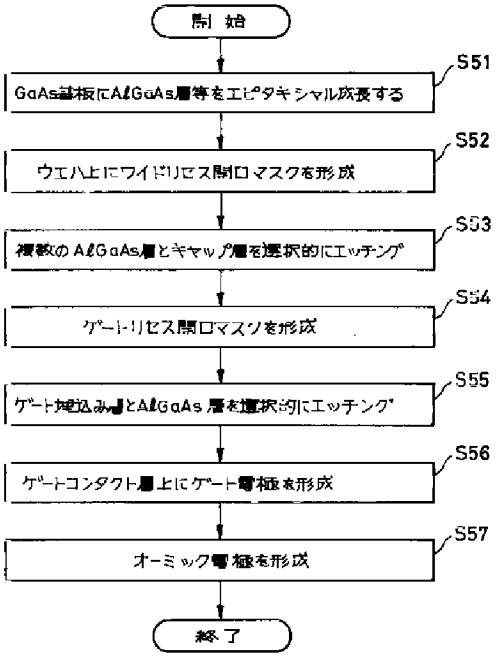
【図13】



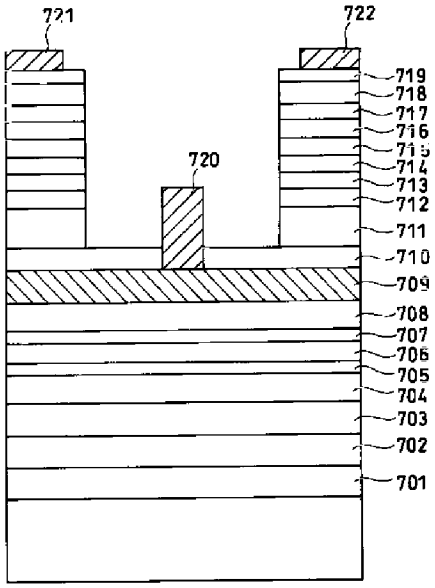
【図14】



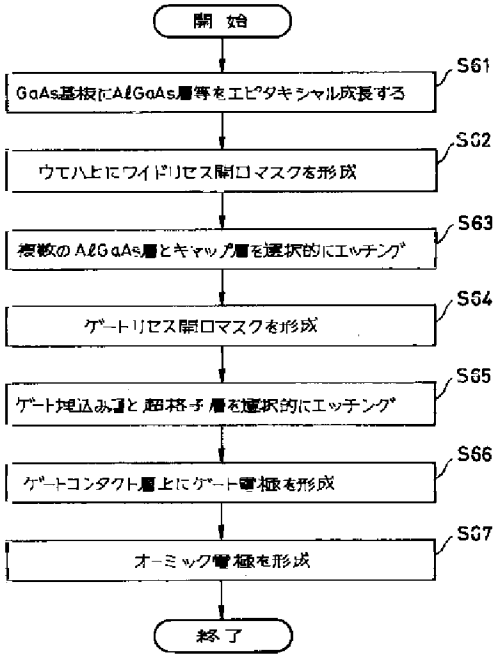
【図15】



【図16】

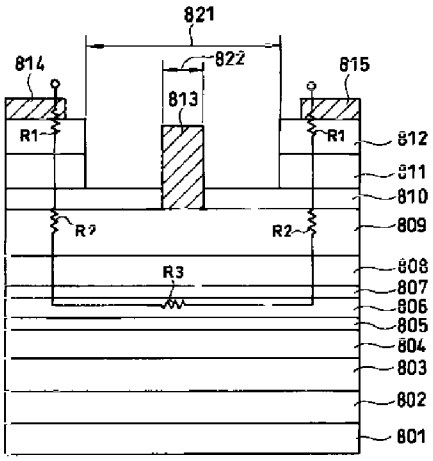


【図17】



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【図18】


821
822
814
815
813
R1
R1
812
811
810
R2
R2
809
R3
808
807
806
805
804
803
802
801

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JP2000236086A FIELD-EFFECT TRANSISTOR AND ITS MANUFACTURING METHOD

Applicants: NEC CORP

Inventors: KATO TAKEHIKO

Classifications:
IPC ***H01L21/338; H01L29/778; H01L29/812;*** (IPC1-7): H01L21/338; H01L29/778; H01L29/812;

Priorities: JP3797999A 1999-02-17

Application: JP2000236086A·1999-02-17

Publication: JP2000236086A·2000-08-29

Published as: JP2000236086A;**JP3223903B2**

FIELD-EFFECT TRANSISTOR AND ITS MANUFACTURING METHOD

Abstract

PROBLEM TO BE SOLVED: To reduce contact resistance of a field-effect transistor extending from cap layer to a channel layer. SOLUTION: A superlattice layer 110 is laminated onto the upper part of an electronic supply layer (Schottky layer) via a Schottky gate contact layer 109, thus reducing the bending of a conduction band which is generated on an interface to a GaAs embedded layer 111, and hence reducing sheet resistance at the part. Also, since the superlattice layer 110 is scraped when a gate recess is formed, ϕB (the height of the Schottky barrier in units of electron volt) that becomes effective on the formation of the Schottky layer is set to Al0.2Ga0.8 As, thus reducing the on-resistance by 0.1 Ωmm.

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DESCRIPTION JP2000236086

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a field effect transistor (“FET”) and a manufacturing method thereof, and more particularly to a heterojunction field effect transistor and a manufacturing method thereof.

[0002]
2. Description of the Related Art An example of this type of conventional technology is "The Institute of Electronics, Information and Communication Engineers, 1996 Electronics Society Conference Park Collection 2: Naoto Yoshida, Hideaki Katayama, Akira Inoue, Kazuo Hayashi, Takahiro Nakamoto, Tomoyuki Asada, Yutaka Kasume. , Noriyuki Yano, Masahide Yamauchi, page 80, line 18 and FIG. 1, date of publication August 30, 1996 ” .

[0003]

GaAs FETs are widely used as high frequency devices.

In particular, in the high output device, a multi-step recess structure is adopted in order to reduce the source resistance and ensure the gate breakdown voltage.

[0004]

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The "recess structure" refers to a structure in which the source and drain regions are masked and the vicinity of the gate is dug by etching, and the "multi-step recess structure" is a structure in which a plurality of steps are dug.

[0005]

Such a multi-step recess structure is formed by using, for example, selective etching of a GaAs / AlGaAs laminated structure.

FIG. 18 is a sectional view of a conventional field effect transistor. In FIG. 18, 801 is a semi-insulating GaAs substrate, 802 is a 400 nm thick GaAs buffer layer, 803 is an undoped Al0.2 Ga0.8 As buffer layer, 804 is a Si-doped Al0.2 Ga0.8 As electron supply layer, 805 is an undoped Al0.2 Ga0.8 As spacer layer, 806 is an undoped In0.2 Ga0.8 As channel layer, 807 is an undoped Al0.2 Ga0.8 As spacer layer, and 808 is Si-doped Al0.2 Ga0.8 As electrons. Supply layer, 809 undoped Al0.2 Ga0.8 As gate contact layer, 810 GaAs gate buried layer, 811 Si-doped Al0.2 Ga0.8 As wide recess stopper layer, 812 Si-doped GaAs cap layer, 813 A gate electrode, 814 is a source electrode, and 815 is a drain electrode.

[0006]

In such a recess structure, first, a mask (not shown) in which the first recess (wide recess) portion 821 is opened is formed, and the GaAs layer 812 is selectively etched using the AlGaAs layer 811 as a wide recess stopper. Next, a mask (not shown) having an opening in the second recess (gate recess) portion 822 is formed, and the GaAs layer 810 is selectively etched using the AlGaAs layer 809 as a gate recess stopper layer.

[0007]

FIG. 18 schematically shows the distributed constant electrical resistance generated in each part of the FET having the conventional structure. R1 is a contact resistance from the ohmic electrode (source electrode 814 and drain electrode 815) to the cap layer 812, R2 is a contact resistance from the cap layer 812 to the channel layer 806, and R3 is a sheet resistance below the gate 813. The ON resistance of the FET is the total resistance from the source electrode 814 to the drain electrode 815.

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[0008]
Low on-resistance is important for obtaining high output and high efficiency in low voltage operation, as described in another document “1996 IEEE GaAs IC Symposium page 119”.

[0009]
Other examples of this type of prior art are disclosed in Japanese Patent Application Laid-Open No. 9-102600 and Japanese Patent No. 2626213.

[0010]

However, the conventional technique has a drawback that the contact resistance R2 from the cap layer to the channel layer is high.

The reason is that the AlGaAs stopper layer used for forming the multi-step recess structure has a high potential barrier and the tunnel probability from the cap layer to the channel layer is small.

However, it is difficult to thin this layer because it is used as a stopper layer for selective etching.

[0011]
Therefore, an object of the present invention is to provide a field effect transistor capable of reducing the contact resistance from the cap layer to the channel layer and a method for manufacturing the same.

[0012]
In order to solve the above problems, the present invention provides a channel layer made of InGaAs or GaAs, a first AlGaAs layer, an AlGaAs / GaAs superlattice layer, a GaAs layer, and a second AlGaAs. Layer and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated, and further, a first recess formed in the second AlGaAs layer and the cap layer, and the first recess A field effect transistor is configured to include a second recess formed in the AlGaAs / GaAs superlattice layer and the GaAs layer, and a gate electrode provided in the second recess.

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[0013]
Another invention according to the present invention is a channel layer composed of InGaAs or GaAs, a first AlGaAs layer, an AlGaAs / GaAs superlattice layer, a GaAs layer, a second AlGaAs layer and InGaAs or GaAs for an ohmic electrode. A first step of sequentially laminating the cap layers to be formed, a second step of forming the first recess in the second AlGaAs layer and the cap layer after the first step, and a step of following the second step. A third step of forming a second recess in the first recess and in the AlGaAs / GaAs superlattice layer and the GaAs layer, and a gate electrode in the second recess after the third step. And a fourth step of providing a field effect transistor.

[0014]
According to the present invention and another invention according to the present invention, since the AlGaAs / GaAs superlattice layer is laminated on the first AlGaAs layer, the contact resistance can be reduced.

[0015]

BEST MODE FOR CARRYING OUT THE INVENTION Embodiments of the present invention will be described below with reference to the accompanying drawings.

First, the first embodiment will be described.

The first embodiment relates to the inventions of claims 1 and 8.

[0016]

1 is a sectional view showing a configuration of a first embodiment of the present invention, FIGS. 2 to 4 are sectional views in a manufacturing process of the same embodiment, and FIG. 5 is a flowchart showing a manufacturing process of the same embodiment.

Hereinafter, the first embodiment will be described with reference to FIGS. 1 to 5.

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[0017]

First, on a semi-insulating GaAs substrate 101, a GaAs buffer layer 102 having a film thickness of 400 nm, an undoped Al0.2 Ga0.8 As buffer layer 103 having a film thickness of 100 nm, and an Al0 film having a film thickness of 4 nm doped with Si 4 × 10 18 cm −3. .2 Ga0.8 As electron supply layer 104, 2 nm thick undoped Al0.2 Ga0.8 As spacer layer 105, 15 nm thick undoped In0.2 Ga0.8 As channel layer 106, 2 nm thick undoped Al0. 2 Ga0.8 As spacer layer 107, Al0.2 Ga0.8 As electron supply layer 108 having a film thickness of 9 nm doped with Si at 4 × 10 18 cm −3, undoped Al0.2 Ga0.8 As Schottky gate contact layer having a film thickness of 17 nm 109, Al0.2 Ga0.8 As (0.5 nm) / GaAs (0.5 nm) × 3 periods superlattice layer 110, 30 nm thick undoped GaAs buried layer 111, Si 4 × 10 18 cm −3 doped film An Al 0.2 Ga 0.8 As wide recess stopper layer 112 having a thickness of 6 nm and a GaAs cap layer 113 having a thickness of 100 nm doped with Si of 4 × 10 18 cm −3 are epitaxially grown sequentially by a molecular beam growth method or a metal organic chemical vapor deposition method (S1).

FIG. 2 shows the structure after epitaxial growth.

[0018]

Next, a mask 901 having wide recesses opened is formed on the wafer formed as shown in FIG. 3 (S2), and the GaAs cap layer 113 is formed by using the Al0.2 Ga0.8 As wide recess stopper layer 112 as a stopper layer. Are selectively etched (S3). Such selective etching uses an ECR etching device or an RIE device, and dry etching using a mixed gas (for example, BCl3 + SF6) of a chlorine gas containing only chlorine as a halogen element and a fluoride gas containing only fluorine. Is possible.

[0019]

After removing the mask, as shown in FIG. 4, a new mask 902 having an opening in the gate recess portion is formed (S4), and the GaAs gate buried layer 110 is formed by using the Al0.2Ga0.8As gate contact layer 109 as a stopper layer. , Al0.2 Ga0.8 As (0.5 nm) / GaAs (0.5 nm) × 3 periods superlattice layer 110 is selectively etched (S5).

[0020]

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Next, the gate electrode 114 is formed on the exposed portion 109a of the Al0.2Ga0.8As gate contact layer 109 exposed as a result of etching (S6), and AuGe is deposited by lift-off and alloying (for example, 400 ° C./min). Then, the source electrode 115 and the drain electrode 116 are formed as ohmic electrodes (S7).

[0021]

According to the structure of the first embodiment, since the AlGaAs / GaAs superlattice layer 110 is laminated on the AlGaAs Schottky layer 108 which functions as a potential barrier between the source and drain, the interface with the GaAs buried layer 111 is formed. The bending of the conduction band that occurs is reduced, and the sheet resistance in this portion is reduced.

Further, immediately below the gate Schottky, since the AlGaAs / GaAs superlattice layer 110 layer is shaved at the time of forming the gate recess, ϕB (Schottky barrier height; unit electron volt, the same applies hereinafter) that is effective in forming the Schottky layer is Al0.2 Ga0. Take a value of 8 As.

As a result, the on resistance of 0.1 $\Omega \cdot$ mm is reduced.

[0022]

Next, a second embodiment will be described. The second embodiment relates to the inventions of claims 2 and 9.

[0023]

FIG. 6 is a sectional view showing the configuration of the second embodiment of the present invention, and FIG. 7 is a flowchart showing the manufacturing process of the same embodiment. It should be noted that in the following embodiments, cross-sectional views in the manufacturing process of the same embodiment are not shown. The second embodiment will be described below with reference to FIGS. 6 and 7.

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[0024]
On a semi-insulating GaAs substrate 201, a GaAs buffer layer 202 having a film thickness of 400 nm, an undoped Al0.2 Ga0.8 As buffer layer 203 having a film thickness of 100 nm, and an Al0.2 film having a film thickness of 4 nm doped with Si 4 × 10 18 cm −3. Ga0.8 As electron supply layer 204, 2 nm-thick undoped Al0.2 Ga0.8 As spacer layer 205, 15 nm-thick undoped In0.2 Ga0.8 As channel layer 206, 2 nm-thick undoped Al0.2 Ga0 .8 As spacer layer 207, Al0.2 Ga0.8 As electron supply layer 208 with a thickness of 9 nm doped with Si at 4 × 10 18 cm -3, undoped Al0.2 Ga0.8 Schottky gate contact layer 209 with a thickness of 17 nm, film An undoped GaAs buried layer 210 having a thickness of 30 nm, an Al0.2 Ga0.8 As wide recess stopper layer 211 having a film thickness of 3 nm doped with Si of 4 × 10 18 cm −3, and an Al0. A 1 Ga0.9 As layer 212 and a 100 nm thick GaAs cap layer 213 doped with Si of 4 × 10 18 cm −3 are epitaxially grown sequentially by the molecular beam growth method or the metal organic chemical vapor deposition method (S11).

[0025]
A mask with an open wide recess is formed on the created wafer (S12), and an Al0.2 Ga0.8 As wide recess stopper layer 211 is used as a stopper layer to form an Al0.1 Ga0.9 As layer 212 and a GaAs cap layer 213 layer. Are selectively etched (S13).

[0026]
Such selective etching uses an ECR etching device or an RIE device, and dry etching using a mixed gas (for example, BCl3 + SF6) of a chlorine gas containing only chlorine as a halogen element and a fluoride gas containing only fluorine. Is possible.

[0027]

After removing the mask, a new mask having a gate recess opened is formed (S14), and the GaAs gate buried layer 210 is selectively etched by using the Al0.2Ga0.8As gate contact layer 209 as a stopper layer (S15).

A gate electrode 214 is formed on the gate contact layer 209 exposed on the surface (S16).

Next, AuGe is subjected to vapor deposition lift-off and alloying (for example, 400 ° C./min) to form a source electrode 215 and a drain electrode 216 as ohmic electrodes (S17).

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[0028]

According to the structure of the second embodiment, the AlGaAs wide recess stopper layer has a two-step structure (211 layers and 212 layers), so that the sheet resistance in this portion is reduced.

As a result, the on resistance of 0.05 Ω · mm is reduced.

[0029]

Next, a third embodiment will be described. The third embodiment relates to the inventions of claims 3 and 10.

[0030]

FIG. 8 is a sectional view showing the configuration of the third embodiment of the present invention, and FIG. 9 is a flow chart showing the manufacturing process of the same embodiment. Hereinafter, the third embodiment will be described with reference to FIGS. 8 and 9.

[0031]

On a semi-insulating GaAs substrate 301, a GaAs buffer layer 302 having a film thickness of 400 nm, an undoped Al0.2 Ga0.8 As buffer layer 303 having a film thickness of 100 nm, and an Al0.2 film having a film thickness of 4 nm doped with Si 4 × 10 18 cm −3. Ga0.8 As electron supply layer 304, 2 nm thick undoped Al0.2 Ga0.8 As spacer layer 305, 15 nm thick undoped In0.2 Ga0.8 As channel layer 306, 2 nm thick undoped Al0.2 Ga0 .8 As spacer layer 307, Si 4 × 10 18 cm −3 doped 9 nm thick Al 0.2 Ga 0.8 As electron supply layer 308, 17 nm thick undoped Al 0.2 Ga 0.8 As Schottky gate contact layer 309, An undoped GaAs buried layer 310 having a film thickness of 30 nm, an Al0.2 Ga0.8 As layer 311 having a film thickness of 3 nm doped with Si at 4 × 10 18 cm −3, and an Al 0 .5 film having a film thickness of 0.5 nm doped with Si at 4 × 10 18 cm −3. 18 Ga 0.82 As layer 312, Si 0.14 Ga cm-0.85 As layer 313 with a thickness of 0.5 nm, and Si 4 x 10 18 cm -3 doped Si 0.14 Ga 0.85 As layer 313 with a 0.5 nm film thickness Al 0.12

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Ga 0.88 As layer 314, Si 4 × 10 18 cm -3 doped 0.5 nm thick Al0.09Ga0.91As layer 315, Si 4 × 10 18 cm -3 doped 0.5 nm thick Al0.06Ga 0.94As layer 316, Si An Al0.03Ga0.97As layer 317 having a film thickness of 4 × 10 18 cm −3 and a thickness of 0.5 nm, and a GaAs cap layer 318 having a film thickness of 100 nm and having a film thickness of 4 × 10 18 cm −3 and having a thickness of 100 nm are sequentially grown by molecular beam growth or metal organic chemical vapor deposition. Is epitaxially grown by the method (S21).

[0032]
A mask having wide recesses is formed on the formed wafer (S22), and Al0.2 Ga0.8 As wide recess stopper layer 311 is used as a stopper layer to selectively form AlGaAs layers 312 to 317 and a GaAs cap layer 313 layer. Etching is performed (S23).

[0033]
Such selective etching uses an ECR etching apparatus or an RIE apparatus, and dry etching in which a mixed gas (for example, BCl3 + SF6 etc.) of a chlorine gas containing only chlorine as a halogen element and a fluoride gas containing only fluorine is introduced. Is possible.

[0034]
After removing the mask, a new mask having a gate recess opened is formed (S24), and the GaAs gate buried layer 310 is selectively etched by using the Al0.2Ga0.8As gate contact layer 309 as a stopper layer (S25).

[0035]

A gate electrode 319 is formed on the gate contact layer 309 exposed on the surface (S26).

Next, AuGe is subjected to vapor deposition lift-off and alloying (for example, 400 ° C./min) to form a source electrode 320 and a drain electrode 321 as ohmic electrodes (S27).

[0036]

According to the structure of the third embodiment, the AlGaAs wide recess stopper layer has a two-step structure (311 layer and 312 to 317 layer), so that the sheet resistance in this portion is

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reduced.

As a result, the on resistance of 0.05 Ω · mm is reduced.

[0037]

Next, a fourth embodiment will be described.

The fourth embodiment relates to the inventions of claims 4 and 11.

[0038]

FIG. 10 is a sectional view showing the configuration of the fourth embodiment of the present invention, and FIG. 11 is a flow chart showing the manufacturing process of the same embodiment.

Hereinafter, the fourth embodiment will be described with reference to FIGS. 10 and 11.

[0039]

On a semi-insulating GaAs substrate 401, a GaAs buffer layer 402 having a film thickness of 400 nm, an undoped Al0.2 Ga0.8 As buffer layer 403 having a film thickness of 100 nm, and an Al0.2 film having a film thickness of 4 nm doped with Si at 4 × 10 18 cm −3. Ga0.8 As electron supply layer 404, 2 nm thick undoped Al0.2 Ga0.8 As spacer layer 405, 15 nm thick undoped In0.2 Ga0.8 As channel layer 406, 2 nm thick undoped Al0.2 Ga0 .8 As spacer layer 407, Al0.2 Ga0.8 As electron supply layer 408 having a film thickness of 9 nm doped with Si at 4 × 10 18 cm -3, undoped Al0.2 Ga0.8 As Schottky gate contact layer 409 having a film thickness of 17 nm, Undoped Al0.1 Ga0.9 As layer 410 having a film thickness of 3 nm, undoped GaAs buried layer 411 having a film thickness of 30 nm, Si having a thickness of 4 × 10 18 cm −3, and having a film thickness of 6 nm, Si having a thickness of 4 × 10 18 cm − 3 Al 0.2 Ga 0.8 As wide recess stopper layer 412, Si 4 × 10 18 cm −3 doped 3 nm thick Al 0.1 Ga 0.9 AsAs layer 413, Si 4 × 10 18 cm − 3 doped 100 nm thick GaAs The cap layer 414 is sequentially epitaxially grown by the molecular beam growth method or the metal organic chemical vapor deposition method (S31).

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[0040]
A mask having wide recesses is formed on the formed wafer (S32), and the GaAs cap layer 414 layer and the AlGaAs 413 layer are selectively etched by using the Al0.2 Ga0.8 As wide recess stopper layer 412 as a stopper layer (S33).

[0041]
Such selective etching uses an ECR etching apparatus or an RIE apparatus, and dry etching in which a mixed gas (for example, BCl3 + SF6 etc.) of a chlorine gas containing only chlorine as a halogen element and a fluoride gas containing only fluorine is introduced. Is possible.

[0042]
After removing the mask, a new mask having an opening in the gate recess is formed (S34), and the Al0.2Ga0.8As gate contact layer 409 is used as a stopper layer to form the GaAs gate buried layer 411 and Al0.1Ga0.9. The As layer 410 is selectively etched (S35).

[0043]

A gate electrode 415 is formed on the gate contact layer 409 exposed on the surface (S36).

Then, AuGe is subjected to vapor deposition lift-off and alloying (for example, 400 ° C./min) to form a source electrode 416 and a drain electrode 417 as ohmic electrodes (S37).

[0044]

According to the structure of the fourth embodiment, the AlGaAs Schottky layer that acts as a potential barrier between the source and the drain has a two-step structure (412 layer and 413 layer), so that the sheet resistance in this portion is reduced. It

Further, immediately below the gate Schottky, since the Schottky layer 410 is scraped at the time of forming the gate recess, ϕB effective for forming the Schottky layer has a value of Al0.2 Ga0.8 As.

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As a result, the on-resistance of 0.15Ω · mm is reduced.

[0045]

Next, a fifth embodiment will be described.

The fifth embodiment relates to the inventions of claims 5 and 12.

[0046]

FIG. 12 is a sectional view showing the structure of the fifth embodiment of the present invention, and FIG. 13 is a flow chart showing the manufacturing process of the same embodiment. The fifth embodiment will be described below with reference to FIGS. 12 and 13.

[0047]

On a semi-insulating GaAs substrate 501, a GaAs buffer layer 502 having a film thickness of 400 nm, an undoped Al0.2 Ga0.8 As buffer layer 503 having a film thickness of 100 nm, and an Al0.2 film having a film thickness of 4 nm doped with Si at 4 × 10 18 cm −3. Ga0.8 As electron supply layer 504, 2 nm thick undoped Al0.2 Ga0.8 As spacer layer 505, 15 nm thick undoped In0.2 Ga0.8 As channel layer 506, 2 nm thick undoped Al0.2 Ga0 .8 As spacer layer 507, Si 4 × 10 18 cm -3 doped 9 nm thick Al0.2 Ga0.8 As electron supply layer 508, 17 nm thick undoped Al0.2 Ga0.8 As Schottky gate contact layer 509, Al0.2 Ga0.8 As (0.5 nm) / GaAs (0.5 nm) × 3 period superlattice layer 510, 30 nm thick undoped GaAs buried layer 511, Si 4 × 10 18 cm −3 thickness 6 nm 3 nm thick Al0.2 Ga0.8 As wide recess stopper layer 512 doped with 4 × 10 18 cm −3 of Si, and 3 nm thick Al0.1 Ga0.9 As layer 513 doped with 4 × 10 18 cm −3 Si, A 100 nm-thick GaAs cap layer 514 doped with Si at 4 × 10 18 cm −3 is epitaxially grown sequentially by a molecular beam growth method or a metal organic chemical vapor deposition method (S41).

[0048]

A mask having wide recesses is formed on the formed wafer (S42), and the GaAs cap layer 514 layer and the AlGaAs layer 513 are selectively etched by using the Al0.2 Ga0.8 As wide recess

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stopper layer 512 as a stopper layer. (S43).

[0049]
Such selective etching uses an ECR etching apparatus or an RIE apparatus, and dry etching in which a mixed gas (for example, BCl3 + SF6 etc.) of a chlorine gas containing only chlorine as a halogen element and a fluoride gas containing only fluorine is introduced. Is possible.

[0050]
After removing the mask, a new mask having an opening in the gate recess is formed (S44), and the Al0.2Ga0.8 As gate contact layer 509 is used as the stopper layer to form the GaAs gate buried layer 511 and the Al0.2Ga0.8 layer. The superlattice layer 510 of As (0.5 nm) / GaAs (0.5 nm) × 3 periods is selectively etched (S45).

[0051]

A gate electrode 515 is formed on the gate contact layer 509 exposed on the surface (S46).

Next, AuGe is subjected to vapor deposition lift-off and alloying (for example, 400 ° C./min) to form a source electrode 516 and a drain electrode 517 as ohmic electrodes (S47).

[0052]

According to the structure of the fifth embodiment, the AlGaAs Schottky layer that acts as a potential barrier between the source and the drain has a two-stage structure (512 layers and 513 layers), so that the sheet resistance in this portion is reduced. It

Further, immediately below the gate Schottky, since the AlGaAs layer 510 layer is scraped at the time of forming the gate recess, ϕB which is effective in forming the Schottky layer has a value of Al0.2Ga0.8As.

As a result, the on-resistance of 0.15Ω · mm is reduced.

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[0053]

Next, a sixth embodiment will be described.

The sixth embodiment relates to the inventions of claims 6 and 13.

[0054]

FIG. 14 is a sectional view showing the configuration of the sixth embodiment of the present invention, and FIG. 15 is a flow chart showing the manufacturing process of the same embodiment. The sixth embodiment will be described below with reference to FIGS. 14 and 15.

[0055]

On a semi-insulating GaAs substrate 601, a GaAs buffer layer 602 having a film thickness of 400 nm, an undoped Al0.2 Ga0.8 As buffer layer 603 having a film thickness of 100 nm, and an Al0.2 film having a film thickness of 4 nm doped with Si at 4 × 10 18 cm −3. Ga0.8 As electron supply layer 604, 2 nm thick undoped Al0.2 Ga0.8 As spacer layer 605, 15 nm thick undoped In0.2 Ga0.8 As channel layer 606, 2 nm thick undoped Al0.2 Ga0 .8 As spacer layer 607, 9 nm thick Al0.2 Ga0.8 As electron supply layer 608 doped with 4 × 10 18 cm −3 of Si, 17 nm thick undoped Al0.2 Ga0.8 As Schottky gate contact layer 609, An undoped Al0.1 Ga0.9 As layer 610 having a film thickness of 3 nm, an undoped GaAs buried layer 611 having a film thickness of 30 nm, an Al0.2 Ga0.8 As layer 612 having a film thickness of 3 nm doped with Si of 4 × 10 18 cm −3, and a Si film are formed. 4 × 10 18 cm -3 doped Al 0.18 Ga 0.82 As layer 613 with a film thickness of 0.5 nm, Si 4 × 10 18 cm -3 doped 0.5 nm Al 0.15 Ga 0.85 As layer 614, Si 4 × 10 18 cm- 3 Al-doped 0.5-nm thick Al0.12Ga0.88As layer 615, Si-doped 4 × 10 18 cm −3 0.5-nm thick Al0.09Ga 0.91As layer 616, Si-doped 4 × 10 18 cm −3 film Al0.06Ga0.94As layer 617 having a thickness of 0.5 nm, Al0.03Ga0.97As layer 618 having a film thickness of 0.5 nm doped with Si at 4 × 10 18 cm −3, and GaAs having a film thickness of 100 nm doped with Si at 4 × 10 18 cm −3 The cap layer 619 is sequentially epitaxially grown by the molecular beam growth method or the metal organic chemical vapor deposition method (S51).

[0056]

A mask having wide recesses is formed on the created wafer (S52), and the Al0.2Ga0.8As wide recess stopper layer 612 is used as a stopper layer to selectively form the GaAs cap layer 614

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layer and the AlGaAs layers 613 to 618. Etching (S53).

[0057]
Such selective etching uses an ECR etching device or an RIE device, and dry etching using a mixed gas (for example, BCl3 + SF6) of a chlorine gas containing only chlorine as a halogen element and a fluoride gas containing only fluorine. Is possible.

[0058]
After removing the mask, a new mask having an opening in the gate recess is formed (S54), and the Al0.2Ga0.8As gate contact layer 609 is used as a stopper layer to form the GaAs gate buried layer 611 and Al0.1Ga0.9. The As layer 610 is selectively etched (S55).

[0059]

A gate electrode 620 is formed on the gate contact layer 609 exposed on the surface (S56).

Next, AuGe is subjected to vapor deposition lift-off and alloying (for example, 400 ° C./min) to form a source electrode 621 and a drain electrode 622 as ohmic electrodes (S57).

[0060]

According to the structure of the sixth embodiment, the AlGaAs Schottky layer, which acts as a potential barrier between the source and the drain, has a two-step structure (612 layers and 613 to 618 layers). Will be reduced.

Further, immediately below the gate Schottky, since the AlGaAs layer 610 layer is scraped at the time of forming the gate recess, ϕB which is effective in forming the Schottky layer has a value of Al0.2Ga0.8As.

As a result, the on-resistance of 0.15Ω · mm is reduced.

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[0061]

Next, a seventh embodiment will be described.

The seventh embodiment relates to the inventions of claims 7 and 14.

[0062]

FIG. 16 is a sectional view showing the configuration of the seventh embodiment of the present invention, and FIG. 17 is a flow chart showing the manufacturing process of the same embodiment. The seventh embodiment will be described below with reference to FIGS. 16 and 17.

[0063]

On a semi-insulating GaAs substrate 701, a GaAs buffer layer 702 having a thickness of 400 nm, an undoped Al0.2 Ga0.8 As buffer layer 703 having a thickness of 100 nm, and an Al0.2 having a thickness of 4 nm doped with Si at 4 × 10 18 cm −3. Ga0.8 As electron supply layer 704, 2 nm thick undoped Al0.2 Ga0.8 As spacer layer 705, 15 nm thick undoped In0.2 Ga0.8 As channel layer 706, 2 nm thick undoped Al0.2 Ga0 .8 As spacer layer 707, Si 0.24 cm.sup.3 cm @ -3 doped 9 nm thick Al0.2 Ga0.8 As electron supply layer 708, 17 nm thick undoped Al0.2 Ga0.8 As Schottky gate contact layer 709, Al0.2 Ga0.8 As (0.5 nm) / GaAs (0.5 nm) × 3 period superlattice layer 710, 30 nm thick undoped GaAs buried layer 711, Si 4 × 10 18 cm −3 thick 3 nm thick Al 0.2 Ga 0.8 As layer 712, Si 4 × 10 18 cm -3 doped 0.5 nm thick Al 0.18 Ga 0.82 As layer 713, Si 4 × 10 18 cm -3 doped 0.5 nm thick Al 0 .15 Ga0.85As layer 714, Si 4 × 10 18 cm -3 doped 0.5 nm thick Al0.12Ga 0.88As layer 715, Si 4 × 10 18 cm -3 doped 0.5 nm thick Al0.09Ga 0.91As Layer 716, Si 4 × 10 18 cm -3 doped 0.5 nm thick Al0.06Ga0.94As layer 717, Si 4 × 10 18 cm -3 doped 0.5 nm thick Al0.03Ga 0.97As layer 718, Si Then, a GaAs cap layer 719 having a thickness of 100 nm doped with 4 × 10 18 cm -3 is sequentially epitaxially grown by a molecular beam growth method or a metal organic chemical vapor deposition method (S61).

[0064]

A mask with an open wide recess is formed on the created wafer (S62), and the GaAs cap layer 714 and the AlGaAs layers 713 to 718 are selectively etched using the Al0.2 Ga0.8 As wide recess stopper layer 712 as a stopper layer. (S63).

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[0065]
Such selective etching uses an ECR etching device or an RIE device, and dry etching using a mixed gas (for example, BCl3 + SF6) of a chlorine gas containing only chlorine as a halogen element and a fluoride gas containing only fluorine Is possible.

[0066]
After removing the mask, a new mask having an opening in the gate recess is formed (S64), and the Al0.2 Ga0.8 As gate contact layer 709 is used as a stopper layer to form the GaAs gate buried layer 711 and Al0.2 Ga0.8. The superlattice layer 710 of As (0.5 nm) / GaAs (0.5 nm) × 3 periods is selectively etched (S65).

[0067]

A gate electrode 720 is formed on the gate contact layer 709 exposed on the surface (S66).

Next, AuGe is subjected to vapor deposition lift-off and alloying (for example, 400 ° C./min) to form a source electrode 721 and a drain electrode 722 as ohmic electrodes (S67).

[0068]

According to the structure of the seventh embodiment, the AlGaAs Schottky layer, which acts as a potential barrier between the source and the drain, has a two-stage structure (712 layers and 713 to 718 layers). Will be reduced.

Further, just under the gate Schottky, since the AlGaAs layer 710 layer is scraped at the time of forming the second recess, ϕB which is effective in forming the Schottky layer has a value of Al0.2Ga0.8As.

As a result, the on-resistance of 0.15Ω · mm is reduced.

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[0069]
According to the present invention, the channel layer made of InGaAs or GaAs, the first AlGaAs layer, the AlGaAs / GaAs superlattice layer, the GaAs layer, the second AlGaAs layer and the InGaAs or GaAs for the ohmic electrode. And a first recess formed in the second AlGaAs layer and the cap layer, and the AlGaAs / GaAs superlattice layer in the first recess. And the second recess formed in the GaAs layer and the gate electrode provided in the second recess constitute the field effect transistor, so that the AlGaAs / GaAs superlattice layer is formed on the first AlGaAs layer. Will be laminated, and this makes it possible to reduce the contact resistance.

[0070]
According to another invention of the present invention, a channel layer composed of InGaAs or GaAs, a first AlGaAs layer, an AlGaAs / GaAs superlattice layer, a GaAs layer, a second AlGaAs layer and InGaAs for an ohmic electrode or A first step of sequentially stacking a cap layer made of GaAs, a second step of forming a first recess in the second AlGaAs layer and the cap layer, and a second step of the first step. And a third step of forming a second recess in the first recess and in the AlGaAs / GaAs superlattice layer and the GaAs layer, and in the second recess after the third step. Since the method for manufacturing a field effect transistor is configured including the fourth step of providing the gate electrode, the AlGaAs / GaAs superlattice layer is stacked on the first AlGaAs layer, thereby reducing the contact resistance. It becomes possible.

[0071]

More specifically, according to the present invention, firstly, the potential barrier is lowered by providing the superlattice layer between the Schottky barrier layers not having a constant composition of AlGaAs as in the conventional structure. The contact resistance between the gates can be reduced by 0.1 $\Omega \cdot$ mm.

Further, at this time, since the gate electrode is provided in the portion having a high Al composition, a high ϕB can be maintained.

As a result, the structure of the present invention enables high-output operation and high-efficiency operation of the field effect transistor while maintaining a high reverse breakdown voltage.

[0072]

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Secondly, the potential barrier is lowered and the contact resistance between the channel gates can be reduced by 0.05Ω · mm by adopting a two-step structure instead of the AlGaAs of the wide recess stopper layer having a constant composition as in the conventional structure.

This enables high-output operation and high-efficiency operation of the field effect transistor.

[0073]

Thirdly, the potential barrier is lowered and the contact resistance between the channel gates is reduced by 0.05 Ω · mm by adopting the graded Al composition structure as described above, instead of the AlGaAs composition of the wide recess stopper layer being constant as in the conventional structure. be able to. This enables high-power operation and high-efficiency operation of the field effect transistor.

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CLAIMS JP2000236086

1.
A channel layer made of InGaAs or GaAs, a first AlGaAs layer, an AlGaAs / GaAs superlattice layer, a GaAs layer, a second AlGaAs layer and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated. And a first recess formed in the second AlGaAs layer and the cap layer, and a second recess formed in the first recess and in the AlGaAs / GaAs superlattice layer and the GaAs layer. A field effect transistor comprising a recess and a gate electrode provided in the second recess.

2.
A channel layer made of InGaAs or GaAs, a first AlGaAs layer, a GaAs layer, a second AlGaAs layer, a third AlGaAs layer, and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated. A first recess formed in the second and third AlGaAs layers and the cap layer, a second recess formed in the first recess and in the GaAs layer, and a second recess formed in the GaAs layer. And a gate electrode provided in the recess of the second field effect transistor.

3.
A channel layer made of InGaAs or GaAs, a first AlGaAs layer, a GaAs layer, a second AlGaAs layer, and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated, and the second AlGaAs layer is further formed. And a first recess formed in the cap layer, a second recess formed in the first recess and in the GaAs layer, and a gate electrode formed in the second recess. A field effect transistor including the second AlGaAs layer, wherein the second AlGaAs layer is formed in a graded structure in which the Al composition ratio is gradually

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increased from the cap layer toward the GaAs layer.

4.

Channel layer composed of InGaAs or GaAs, first AlGaAs layer, second AlGaAs layer, GaAs layer, third AlGaAs layer, fourth AlGaAs layer and cap layer composed of InGaAs or GaAs for ohmic electrode A first recess formed in the third and fourth AlGaAs layers and the cap layer, and in the first recess and in the second AlGaAs layer and the GaAs layer. A field effect transistor, comprising: a second recess formed in the second recess; and a gate electrode provided in the second recess.

5.

Channel layer composed of InGaAs or GaAs, first AlGaAs layer, AlGaAs / GaAs superlattice layer, GaAs layer, second AlGaAs layer, third AlGaAs layer and cap composed of InGaAs or GaAs for ohmic electrode A first recess formed in the second and third AlGaAs layers and the cap layer, and the AlGaAs / GaAs superlattice layer and the GaAs in the first recess. A field effect transistor comprising a second recess formed in a layer and a gate electrode provided in the second recess.

6.

A channel layer made of InGaAs or GaAs, a first AlGaAs layer, a second AlGaAs layer, a GaAs layer, a third AlGaAs layer, and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated. A first recess formed in the third AlGaAs layer and the cap layer, and a second recess formed in the first recess and in the first and second AlGaAs layers and the GaAs layer. And a gate electrode provided in the second recess, and the third AlGaAs layer is formed in a graded structure in which the Al composition ratio is gradually increased from the cap layer toward the GaAs layer. Field-effect transistor characterized by.

7.

A channel layer made of InGaAs or GaAs, a first AlGaAs layer, an AlGaAs / GaAs superlattice layer, a GaAs layer, a second AlGaAs layer and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated. And a first recess formed in the second AlGaAs layer and the cap layer, and a second recess formed in the first recess and in the AlGaAs / GaAs superlattice layer and the GaAs layer. The second AlGaAs layer includes a recess and a gate electrode provided in the second recess, and the second AlGaAs layer has a graded structure in which an Al composition ratio is gradually increased from the cap layer toward the GaAs layer. Characteristic field effect transistor.

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8.

A channel layer composed of InGaAs or GaAs, a first AlGaAs layer, an AlGaAs / GaAs superlattice layer, a GaAs layer, a second AlGaAs layer, and a cap layer composed of InGaAs or GaAs for ohmic electrodes are sequentially laminated. A step of forming a first recess in the second AlGaAs layer and the cap layer after the first step, and in the first recess after the second step; and Including a third step of forming a second recess in the AlGaAs / GaAs superlattice layer and the GaAs layer, and a fourth step of providing a gate electrode in the second recess after the third step. A method for manufacturing a characteristic field effect transistor.

9.

A first layer in which a channel layer made of InGaAs or GaAs, a first AlGaAs layer, a GaAs layer, a second AlGaAs layer, a third AlGaAs layer and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated. A step of forming a first recess in the second and third AlGaAs layers and the cap layer after the first step, and a step of forming the first recess in the first recess after the second step. And a third step of forming a second recess in the GaAs layer, and a fourth step of providing a gate electrode in the second recess after the third step. Manufacturing method.

10.

A first step of sequentially laminating a channel layer made of InGaAs or GaAs, a first AlGaAs layer, a GaAs layer, a second AlGaAs layer and a cap layer made of InGaAs or GaAs for ohmic electrodes, and A second step of forming a first recess in the second AlGaAs layer and the cap layer after one step, and a second step in the first recess and in the GaAs layer after the second step; The method further includes a third step of forming a recess, and a fourth step of providing a gate electrode in the second recess after the third step, and the second AlGaAs layer has an Al composition ratio from the cap layer to the GaAs. A method of manufacturing a field-effect transistor, wherein the field-effect transistor is formed in a graded structure that gradually increases in a layer direction.

11.

A channel layer made of InGaAs or GaAs, a first AlGaAs layer, a second AlGaAs layer, a GaAs layer, a third AlGaAs layer, a fourth AlGaAs layer and a cap made of InGaAs or GaAs for an ohmic electrode. A first step of sequentially stacking layers, a second step of forming a first recess in the third and fourth AlGaAs layers and a cap layer after the first step, and a step of second step after the second step. A third step of forming a second recess in the first recess and in the second AlGaAs layer and the GaAs layer, and providing a gate electrode in the second recess after the third step. A method of manufacturing a field effect transistor, comprising: a fourth step.

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12.

A channel layer made of InGaAs or GaAs, a first AlGaAs layer, an AlGaAs / GaAs superlattice layer, a GaAs layer, a second AlGaAs layer, a third AlGaAs layer and InGaAs or GaAs for an ohmic electrode A first step of sequentially depositing a cap layer, a second step of forming a first recess in the second and third AlGaAs layers and the cap layer after the first step, and a step of following the second step. A third step of forming a second recess in the first recess and in the AlGaAs / GaAs superlattice layer and the GaAs layer, and a gate electrode in the second recess after the third step. And a fourth step of providing the method.

13.

A channel layer made of InGaAs or GaAs, a first AlGaAs layer, a second AlGaAs layer, a GaAs layer, a third AlGaAs layer and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated. A second step of forming a first recess in the third AlGaAs layer and the cap layer after the first step, and in the first recess after the second step and A third step of forming a second recess in the first and second AlGaAs layers and the GaAs layer, and a fourth step of providing a gate electrode in the second recess after the third step, The method of manufacturing a field effect transistor, wherein the third AlGaAs layer is formed in a graded structure in which an Al composition ratio gradually increases from the cap layer toward the GaAs layer.

14.

A channel layer made of InGaAs or GaAs, a first AlGaAs layer, an AlGaAs / GaAs superlattice layer, a GaAs layer, a second AlGaAs layer and a cap layer made of InGaAs or GaAs for ohmic electrodes are sequentially laminated. A first step, a second step of forming a first recess in the second AlGaAs layer and the cap layer after the first step, and a step of forming the first recess in the first recess after the second step. And a third step of forming a second recess in the AlGaAs / GaAs superlattice layer and the GaAs layer, and a fourth step of providing a gate electrode in the second recess after the third step, The method of manufacturing a field effect transistor, wherein the second AlGaAs layer is formed in a graded structure in which an Al composition ratio is gradually increased from the cap layer toward the GaAs layer.

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(71) Applicant: N.V. Philips' Gloeilampenfabrieken
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

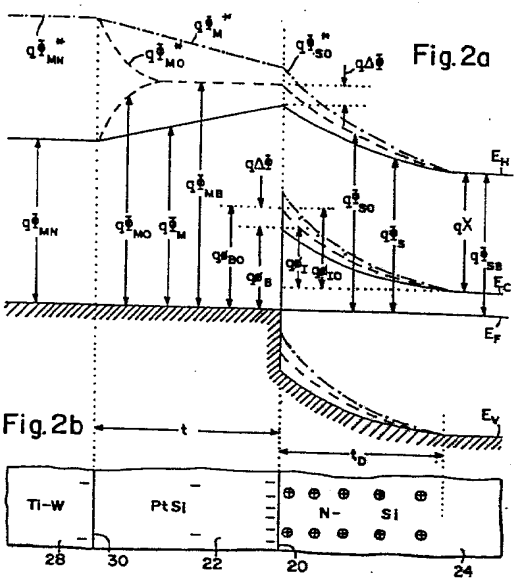
(72) Inventor: Ellwanger, Russell Craig
c/o INT. OCTROOIBUREAU B.V. Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(72) Inventor: Robbins, Arthur Allen
c/o INT. OCTROOIBUREAU B.V. Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(74) Representative: Voorrips, Hugo Carel et al,
INTERNATIONAAL OCTROOIBUREAU B.V. Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(54) **A semiconductor device comprising at least one Schottkytype rectifier having controllable barrier height and method of manufacturing such devices.**

(57) A semiconductor device comprises a Schottky-type diode which has a conductor-to-semiconductor barrier height ϕ_B that is controlled by adjusting the thickness of a metal silicide layer (22) which forms a rectifying junction (20) with an N-type semiconductor (24). The silicide layer is typically platinum silicide whose thickness is on the order of 100 angstroms. In fabricating one version of the diode, a metallic layer (70) consisting of two or more metals such as platinum and nickel is deposited on an N-type silicon semiconductor (68) and heated to create a metal silicide layer (72) consisting of a lower layer (62) and an upper layer (74) of different average composition. A portion of the upper layer is then removed, allowing ϕ_B to be adjusted suitably. In particular the device contains a pair of Schottky-type diodes of different conductor-to-semiconductor barrier height ϕ_B. For at least one of the diodes, ϕ_B is controlled by adjusting the thickness of a metal silicide layer (78A, 78B or 78C) which forms a rectifying junction (76A, 76B or 76C) with an N-type semiconductor (170).



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A semiconductor device comprising at least one Schottky-type rectifier having controllable barrier height and method for manufacturing such devices.

The invention relates to a semiconductor device comprising at least one Schottky type rectifier in which a semiconductor body has an N-type semiconductive region, a metal silicide layer adjoins the N-type region to define a rectifying junction at an interface therebetween, and a conductive non-silicide layer ohmically adjoins the silicide layer across from the junction.

Such a semiconductor device is known from U.S. Patent 3855612.

The invention also relates to a method of manufacturing such devices.

The junction between a metal and an N-type semiconductor may be either rectifying or ohmic--i.e., non-rectifying--depending on the characteristics of the materials in the metal-semiconductor system. As pointed out by R. Muller et al in Device Electronics for Integrated Circuits (John Wiley and Sons: New York), 1977, the work function distinguishes a rectifying junction from an ohmic junction. The work function is a measure of the average energy needed to raise an electron from the Fermi energy level to an energy level at which the electron is just free of the influence of the system. If the work function of the metal is greater than that of the semiconductor when the materials are not interacting, a rectifying junction is formed when they interact.

For the rectifying junction, a charge depletion region consisting of bound positive charges exists on the semiconductor side of the interface. In an idealized system, the electrons associated with the bound positive charges are situated in the metal right next to the interface--i.e., no more than several monolayers into the metal. This sets up an induced electric field directed

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across the depletion region toward the interface where the field essentially ends. As a result, a built-in voltage ϕ_I whose magnitude depends on the N-type dopant concentration in the semiconductor exists across the depletion region. The built-in voltage represents an energy barrier $q\phi_I$ that electrons in the semiconductor conduction band must overcome to cross the interface and enter the metal. q is the electronic charge. This energy barrier can be reduced by applying an external voltage that is positive with respect to the semiconductor. As the applied voltage is increased, a point is eventually reached at which electrons flow freely from the semiconductor to the metal. ϕ_I is thus indicative of the conductive forward voltage drop ϕ_{SH} across the rectifying junction. However, ϕ_I is often difficult to measure directly.

A parameter more readily ascertainable from the current/voltage characteristics of the system is the Schottky barrier height, represented as ϕ_B in electrostatic potential units or as $q\phi_B$ in energy units, that electrons in the metal at the Fermi level must overcome to cross the interface and enter the semiconductor. Because ϕ_B is greater than ϕ_I and is not affected to any significant degree by the applied voltage in the idealized system, very few electrons in the metal can enter the semiconductor. ϕ_B is also linearly related to ϕ_I and therefore provides a direct measure of ϕ_{SH}.

Numerous types of metal-semiconductor rectifying elements, generally referred to as Schootky diodes, have been considered. The oldest Schottky diodes utilize aluminium as the metal and doped silicon as the N-type semiconductor. These basic Al-Si diodes are manufactured relatively easily. However, they degrade relatively fast as the aluminium intermixes with the silicon.

In view of this problem, other materials have been sandwiched between the aluminium and silicon in more recent Schottky diodes. In one of the principal arrangements, a diode is formed on a semiconductor body

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which has an appropriately doped N-type semiconductive region. A layer of a metal silicide adjoins the N-type region to define a rectifying junction at the interface between the N-type region and the silicide layer. The junction is still referred to as a metal-semiconductor or Schottky junction since metal silicides have been conventionally thought to be metallic in nature. The silicide is typically platinum silicide whose $q\phi_B$ with N-type silicon is 0.79 - 0.83 electron volt (eV) depending on the dopant concentration. As, for example, described by W. Rosvold in U.S. Patent 3,855,612, nickel is often included with platinum in the silicide layer. The nickel reduces the junction $q\phi_B$ since the nickel $q\phi_B$ is about 0.63 - 0.67 eV with N-type silicon.

The thickness of the silicide layer is typically on the order of 1,00 nm and is no less than about 50 nm in any known prior art Schottky diode having a conductive non-silicide layer adjoining the silicide layer across from the Schottky junction. This thickness is employed because of the conventional belief that this much silicide is needed to make the silicide layer stable and to avoid continuity defects such as pinholes in it.

A conductive non-silicide layer typically consisting of a barrier metal such as tungsten or titanium-tungsten ohmically adjoins the silicide layer across from the rectifying junction. The barrier metal substantially prevents the materials on either side of it from diffusing through it to the other side. Also, the barrier metal does not diffuse into the silicide. Finally, an aluminium layer normally overlies the barrier metal.

While known Pt-based silicide Schottky diodes perform well without significant junction degradation, they are relatively expensive because of the high cost of platinum. In a Schottky diode whose silicide layer is constituted with two or more metals, controlling the ratio of these metals to one another in the depositon target employed in forming the metallic layer later con-

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verted to silicide is also difficult. It is desirable to have a less expensive silicide Schottky-diode whose ϕ_B can be varied so as to appropriately tailor ϕ_{SH} more simply than in the prior art.

In some integrated circuits, this silicide Schottky diode is used with other Schottky diodes of different ϕ_B. In one such semiconductor structure particularly used for an STL gate, each high-ϕ_B Schottky clamping diode is a PtSi diode of the above type normally formed by reacting platinum with silicon along a surface of a silicon semiconductor. Each low-ϕ_B Schottky output diode is a true metal-semiconductor diode typically created by depositing a metal or metal alloy such as Ti-W on the silicon semiconductor. No silicide layer lies between the silicon and Ti-W.

Only one additional masking step is typically needed to fabricate this structure compared to a structure whose Schottky diodes all have the same ϕ_B. However, because the low-ϕ_B diodes are directly created by metal deposition, their rectifying junctions are not as clean as those of the reaction-created high-ϕ_B silicide diodes. This can lead to manufacturing difficulty and early failure.

J. Bindell et al describe another way for achieving a semiconductor structure with Schottky diodes of different ϕ_B in "Ion-Implanted Low-Barrier PtSi Schottky-Barrier Diodes," IEEE Transactions on Electron Devices, Vol. ED-27, No. 2, Feb. 1979, pp. 420 - 425.

In manufacturing the structure of Bindell et al, an N-type impurity is first implanted into the second region. This raises its net N-type concentration above that in the first region. An approximate 50-nm Pt layer is then deposited on an exposed surface of each region. The resultant structure is suitably heated to cause the platinum to react with silicon along the exposed surface and form the PtSi layers. Any deposited platinum that has not been converted to PtSi is appropriately re-

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moved. A layer of Ti-Pt-Au is then deposited on the resultant structure including on the PtSi layers across from the rectifying junctions and is suitably etched to form the non-silicide layers.

In manufacturing an implanted structure such as that of Bindell et al, only one additional masking step is normally required in comparison with a single-ϕ_B structure. However, there are different breakdown voltages between the different types of diodes. This is often undesirable because it places additional limitations on circuit design.

In short, prior art structures containing Schottky diodes of different ϕ_B generally are difficult to manufacture, have reliability problems, and/or unduly limit system design.

In accordance with a first aspect of the invention, a semiconductor device comprising at least one Schottky type rectifier in which a semiconductor body has an N-type semiconductive region, a metal silicide layer adjoins the N-type region to define a rectifying junction at an interface therebetween, and a conductive non-silicide layer ohmically adjoins the silicide layer across from the junction is characterized in that the silicide layer is sufficiently thin that the actual conductor-to-semiconductor barrier height ϕ_B at the junction does not substantially equal the intrinsic conductor-to-semiconductor barrier height ϕ_{BO} at an interface between material which is the same as that of the N-type region along the junction and material which is the same as that of the silicide layer along the junction and has the same average composition as the silicide layer. The intrinsic barrier height ϕ_{BO} is the barrier height that would exist if the silicide layer were effectively of infinite thickness.

More particularly, the absolute value of $(\phi_{BO} - \phi_N)/(\phi_{BO} - \phi_{BN})$ is at least 15% and preferably at least 25%. ϕ_{BN} is the conductor-to-semiconductor barrier

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height at an interface between material which is the same as the N-type region along the junction and material which is the same as the non-silicide layer.

The invention is based on the discovery that a silicide constituted with a metal such as platinum and/or nickel appears capable of sustaining a small electric field in somewhat the manner that an electric field exists across a conventional semiconductor PN junction. By making the silicide layer thin enough, a self-induced electric field originating in the charge depletion region of the N-type region penetrates through the silicide layer and into the non-silicide layer. Because of this field penetration into the non-silicide layer, the work function of the silicide layer "mixes" with the work function of the non-silicide layer. As a result, ϕ_B differs from ϕ_{BO} which is the barrier height for prior art Schottky diodes.

Typically, fabrication of the present rectifier only involves depositing less metal for the silicide layer than in the prior art. Consequently, ϕ_B can be readily adjusted here without going through difficult-to-control deposition target composition changes used to vary the forward voltage drop in some previous Schottky diodes.

For a preferred embodiment of the invention in which the silicide layer comprises PtSi, its thickness is in the range of 1,5 - 25 nm. Optimally, the PtSi is 6 - 8 nm thick, while the non-silicide layer consists of tungsten or titanium-tungsten as a barrier metal. In this case, work-function mixing makes $q\phi_B$ about 0.74 eV which is about 0.07 eV less than $q\phi_{BO}$ of the comparable prior art Schottky diodes which utilize 50 nm or more of PtSi. The 0.74-eV $q\phi_B$ is quite adequate for many semiconductor applications and is achieved with a small fraction of the platinum employed in comparable prior art PtSi Schottky diodes.

In an important variation where two or more selected metals are used in the silicide layer, it is the

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remainder of an original metal silicide layer of greater thickness. Because of this difference, ϕ_{BO} is taken with respect to material which has the same average composition as the original silicide layer since its average composition generally differs from that of the (remaining) silicide layer. This occurs because the silicide layer consists of two or more generally distinct layers. One of these adjoins the N-type region, while another overlies the first and has a different average composition.

In fabricating a diode according to this variation, a metallic layer composed of the selected metals is deposited on an exposed surface of an N-type silicon semiconductive region in a semiconductor body. The resultant structure is heated to a suitable temperature to form the original silicide by reaction of the metallic layer with solicon along the surface. The metals and dopant concentration of the N-type region are so selected that the interface between the silicide layer and the remainder of the N-type region is a rectifying junction. Next, a non-insubstantial portion of the thickness of the original silicide layer is removed across from the junction so as to establish the desired ϕ_B. Subsequently, a non-silicide layer normally consisting of a barrier metal is formed on the (remaining) silicide layer. A layer of a suitable conductor such as aluminium can then be deposited on the non-silicide layer.

In accordance with a second aspect of the invention, the semiconductor device comprises a semiconductor body having a first N-type semiconductive region and a second N-type semiconductive region (which may be continuous with each other). A first metal silicide layer adjoins the first N-type region to define a first rectifying Schottky junction. A second metal silicide layer adjoins the second N-type region to define a second rectifying Schottky junction whose actual conductor-to-semiconductor barrier height ϕ_{B2} differs from the actual conductor-to-semiconductor barrier height ϕ_{B1} at the

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first junction. A conductive non-silicide layer ohmically adjoins the second silicide layer across from the second junction. The second silicide layer is sufficiently thin that ϕ_{B2} does not substantially equal the intrinsic conductor-to-semiconductor barrier height ϕ_{B20} at an interface between material which is the same as that of the second region along the second junction and material which is the same as that of a second silicide layer along the second junction and has the same average composition as the second silicide layer. The intrinsic barrier height ϕ_{B20} is the barrier height that would exist if the second silicide layer were effectively of infinite thickness.

More particularly, the absolute value of $(\phi_{B20} - \phi_{B2})/(\phi_{B20} - \phi_{BN2})$ is at least 15% and preferably at least 25%. ϕ_{BN2} is the conductor-to-semiconductor barrier height at an interface between material which is the same as the second N-type region along the second junction and material which is the same as the non-silicide layer.

While the nature of the first rectifying junction may be conventional, it may also follow the teachings of the invention. In this case, a further conductive non-silicide layer ohmically adjoins the first silicide layer across from the first junction. The first silicide layer is sufficiently thin that ϕ_{B1} does not substantially equal the intrinsic barrier height ϕ_{B10} defined for the first junction in the same manner as ϕ_{B20} is defined. Likewise, the absolute value of $(\phi_{B10} - \phi_{B1})/(\phi_{B10} - \phi_{BN1})$ is at least 15% where ϕ_{BN1} is defined for the further non-silicide layer in the same manner as ϕ_{BN2} is defined.

The silicide layers normally consist of the same metal silicide but at different thicknesses.

In fabricating the present structure, the metal silicide layers are first formed along the N-type regions to define the rectifying junctions. Where the regions consist of silicon, this is normally performed in two sets

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of similar steps. In the first set of steps, a first metallic layer composed of the metal(s) in the first silicide layer is deposited on a surface of the first N-type region exposed as the result of a masking step. The structure is then suitably heated to cause the first metallic layer to react with adjacent silicon. In the second set of steps, a second metallic layer composed of the metal(s) in the second silicide layer is likewise deposited on a surface of the second region exposed as the result of another masking step. The structure is then suitably heated to cause the second metallic layer to react with acjacent silicon.

The second set of steps is preferably performed after the first set of steps. In this case, a portion of the second metallic layer is also deposited on the metal silicide previously created along the first N-type region. This portion is converted to metal silicide during the subsequent heating step. As a result, the first silicide layer is thicker than the second silicide layer.

The non-silicide layer is subsequently formed on the second silicide layer. The further non-silicide layer is preferably formed on the first silicide layer at the same time and with the same material.

Compared to a structure whose Schottky diodes all have the same ϕ_B, only one additional masking step is needed to fabricate the present structure. This is achieved without any significant loss in reliability. Consequently, the present structure is generally simpler and is more reliable than the above prior art structures likewise manufactured with only one additional masking step.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional side view of a semiconductor structure containing a Schottky-type rectifier according to the invention.

Figs. 2a and 2b are an energy diagram and an associated structural schematic, respectively, useful in

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understanding the rectifier of Fig. 1.

Figs. 3 and 4 are graphs for the variation of ϕ_B and $\left| (\phi_{BO} - \phi_B)/(\phi_{BO} - \phi_{BN}) \right|$, respectively, with silicide thickness in a PtSi Schottky-type diode.

Fig. 5 is a particl cross-sectional side view of a structure containing a particular embodiment of the rectifier of Fig. 1.

Figs. 6a, 6b, 6c and 6d are cross-sectional side views representing steps in a manufacturing process leading to the structure of Fig. 5.

Fig. 7 is a partial cross-sectional side view of a semiconductor structure containing Schottky-type diodes having different barrier heights in accordance with the invention.

Fig. 8 is a circuit diagram corresponding to the structure of Fig. 7.

Figs. 9a, 9b, 9c and 9d are cross-sectional side views representing steps in a process for manufacturing the structure of Fig. 7.

Like reference symbols are employed in the drawings and in the description of the preferred embodiments to represent the same or very similar item or items.

Referring to the drawings, Fig. 1 illustrates a side view of a semiconductor structure containing a Schottky-type rectifier whose actual conductor-to-semiconductor barrier height ϕ_B at its rectifying junction 20 is readily controllable. Junction 20 is located at the interface between a metal silicide layer 22 and an N-semiconductive region 24 in a monocrystalline silicon semiconductor body 26 of an integrated circuit.

The thickness t of silicide layer 22 is at least 15 angstroms. To avoid pinholes and other such continuity defects in layer 22, t is preferably at least 50 angstroms. Layer 22 consists of silicon chemically combined with a metal such as platinum or nickel or with two or more such metals. In a preferred embodiment, layer 22 is PtSi for

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which thickness t is no more than 25 nm and is desirably no more than 10 nm. t is optimally 6 - 8 nm in this embodiment.

N- region 24 has a substantially uniform net N-type dopant concentration of no more than about 2×10^{17} atoms/cm^3 (corresponding to a resistivity of 0.05 ohm-cm). This assures that junction 20 is indeed rectifying (rather than ohmic). The optimum net N-type dopant concentration in N- region 24 is about 9.8×10^{15} atoms/cm^3 (corresponding to a resistivity of about 0.3 ohm-cm).

An electrically conductive non-silicide layer 28 consisting of a metal such as tungsten or titanium-tungsten which acts substantially as a diffusion barrier to silicon and aluminium at 520° C or less ohmically adjoins silicide layer 22 along an interface 30. Optimally, layer 28 consists of about 1,00 nm of Ti-W alloyed in the proportions of 85 % tungsten to 15 % titanium. The Schottky barrier height $q\phi_{BN}$ at an interface between Ti-W in the foregoing proportions and N-type monocrystalline silicon at the optimum dopant concentration above is abput 0.65 eV.

In the optimal embodiment described above for which the thickness t of the PtSi in layer 22 is 6 - 8 nm, it is so thin that the forward voltage drop ϕ_{SH} across junction 20 is about 350 mV at a junction current I of 10 /ua and a diode temperature T of about 25° C. ϕ_B is calculated as a function of ϕ_{SH} from the relationship

$$I = R^{**}AT^2 e^{-q\phi_B/kT}(e^{q\phi_{SH}/nkT} - i)$$

In this relationship, R^{**} is Richardson's constant, k is Boltzmann's constant, and n is the ideality factor. A is the interfacial area of junction 20. In the present case, A is about 4.6×10^{-6} cm^2, and n is about 1.04. Accordingly, $q\phi_B$ is about 0.74 eV. Furthermore, $q\phi_B$ can be reduced to about 0.72 eV by decreasing t to 5 nm or raised to about 0.76 eV by increasing t to 10 nm.

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For purposes of comparison, the intrinsic Schottky barrier height ϕ_{BO} means the conductor-to-semiconductor barrier height for a reference diode whose rectifying junction is at the interface of an N-type region and a reference silicide layer of effectively infinite thickness--i.e., on the order of 1 00 nm. This N-type region is defined as being compositionally the same as N- region 24 along junction 22. Similarly, the reference silicide layer is defined as being composed of the same material as that of silicide layer 22 along junction 20. The reference silicide layer is also defined as having the same average composition as layer 22. The reference diode is thus basically the comparable prior art silicide Schottky diode.

If the reference diode is the same as the optimal diode described above except for the difference in PtSi thickness, $q\phi_{BO}$ is about 0.81 eV. This contrasts sharply with the actual 0.74-eV value for $q\phi_B$. The comparison parameter $\left| (\phi_{BO} - \phi_B)/(\phi_{BO} - \phi_{BN}) \right|$, which is a measure of the difference between the present rectifier and the reference diode, is then 44 %.

Returning to Fig. 1, a layer 32 of a material suitable for electrically interconnecting non-silicide layer 28 with other elements of the integrated circuit lies on the top of layer 28. Layer 32 is preferably a highly conductive metal, optimally aluminium with about 1 % copper having a thickness of 1,1 /um. Alternatively, layer 32 could consist of doped polycrystalline silicon or doped amorphous silicon.

In body 26, a P- substrate region 34 underlies N-region 24. A highly doped N+ buried region 36 lies along the interface 38 between regions 24 and 34. Buried region 36 extends about 6 microns below interface 38 and slightly above it as well. N- region 24, which extends about 3,7 /um upward from interface 38 to the upper surface 40 of body 26, is basically an active semiconductor region laterally isolated from other such semiconductor regions by

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a deep annular highly doped P+ region 42 laterally surrounding N- region 24 and extending downward about 5,00 nm below interface 38. A shallow annular highly doped P+ region 44 underlies the portion of layer 22 outside the lateral boundary of junction 20 and extends laterally outward beyond the side edge of layer 22. P+ layer 44, which extends downward about 1,2 /um below surface 40, is a guard ring for reducing leakage currents. A patterned electrically insulating layer 46 of silicon dioxide whose thickness is 3,50 - 4,00 nm overlies isolation region 42, parts of N- region 24, and the part of guard ring 44 extending laterally outward beyond the side edge of layer 22.

In addition, Fig. 1 illustrates an ohmic electrical contact to N- region 24. This contact consists of a highly doped N+ region 48, a metal silicide layer 50, and an electrically conductive non-silicide layer 52. N+ region 48 extends downward from surface 40 about 1,2 /um into body 26. Silicide layer 50 downwardly adjoins N+ region 48 at a junction 54. Non-silicide layer 52 ohmically adjoins silicide layer 50 at its upper surface. Also shown is an electrically conductive layer 56 lying on the top of non-silicide layer 52. Layers 50, 52 and 56 preferably consist of the same respective materials and have the same respective thicknesses as layers 22, 28 and 32. The net N-type dopant concentration in N+ region 48 along interface 54 is about 5×10^{21} atom/cm^3 (corresponding to a sheet resistance of about 10 ohms/square). As a result, interface 54 is an ohmic junction. During operation, electrons travel from the contact through N- region 24 to buried region 36 and then along it to a location below silicide layer 22 where they pass back through region 24 and across junction 20.

In fabricating the structure of Fig. 1, the starting material is a boron-doped P- monocrystalline silicon semiconductor substrate having a resistivity of 7-21 ohm-cm. Arsenic is selectively diffused into the top

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surface of the substrate at the general location for N+ region 36. After exposing surface 38, an arsenic-doped N- epitaxial layer having a resistivity of about 0.3 ohm-cm is grown on the top of the substrate. During this and subsequent processing steps, the arsenic suitably redistributes to form buried N+ region 36 at a sheet resistance of 10-12 ohms/square.

A layer of silicon dioxide is thermally grown along the top of the structure. After opening a suitable window through this oxide layer, boron is diffused in through this window to form isolation region 42 at a sheet resistance of about 5 ohms/square. A layer of silicon dioxide is thermally grown to close this window. After opening another suitable window through the resulting oxide layer, boron is again diffused to form guard ring 44 at a sheet resistance of about 200 ohms/square. The steps of oxide growth, new window opening, and diffusion are then repeated with phosphorus to form N+ region 48. Another layer of silicon dioxide is thermally grown to close the window for N+ region 48. Layer 46 is the resultant oxide layer.

Windows are now opened through oxide layer 46 at the sites for the diode and the contact. The structure is suitably cleaned, after which an in situ sputter etch is performed with argon ions to remove any silicon dioxide in the diode and contact windows.

A layer of platinum having a thickness of about 3,5 nm is deposited according to conventional sputtering techniques on the top surface of the structure including the surface of the silicon exposed through the windows in oxide layer 46. The structure is then sintered for 20 minutes at 450° C in an environment of dry nitrogen with 1% hydrogen to cause the platinum to react with silicon along the exposed surfaces at both windows so as to form layers 22 and 50 of PtSi. In this reaction, each unit of Si thickness reacts with about one unit of Pt thickness to form about two units of PtSi thickness. Any platinum

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that has not reacted to form PtSi is then removed by etching with hot aqua regia. A 1 00 nm layer of Ti-W at the above proportions is deposited according to conventional sputtering techniques on the top of the structure and suitably etched with hydrogen peroxide to define layers 28 and 52. In a similar manner, a layer of aluminium with about 1 % copper is deposited on the top of the resultant structure and suitably patterned by etching with sulfuric/phosphoric acid to create layers 32 and 56. The structure is then finished in a conventional manner.

As described above, ϕ_B at junction 20 differs from ϕ_{BO} by a non-insubstantial amount. This difference is believed to arise because the self-induced electric field directed across the depletion region in N- region 24 toward junction 20 penetrates through the entire thickness t of silicide layer 22 and into non-silicide layer 28. The self-induced field terminates next to interface 30-- i.e., no more than several monolayers into layer 28. The further field penetration through silicide layer 22 is thought to occur because the silicide in layer 22 is partially semiconductive in nature.

Figs. 2a and 2b which respectively show an energy diagram and an associated schematic side view of a slice through N- region 24, silicide layer 22, and non-silicide layer 28 facilitate the qualitative understanding of the device physics leading to this phenomenon. To simplify the explanation, Figs. 2a and 2b represent the case in which no external voltage is applied across the diode. The solid lines in Fig. 2a denote actual energy variations in the present diode for the case, as above, where ϕ_{BN} for the material of non-silicide layer 28 is less than ϕ_{BO} and where the composition of silicide layer 22 is uniform across its thickness (as with PtSi). The dashed lines in Fig. 2a denote the corresponding energy variations for the reference diode whose silicide layer thickness is effectively infinite.

The circled "+" signs in the N- region 24 of

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Fig. 2b represent the bound positive charges of the depletion region whose width (thickness) is denoted as t_D. The "-" signs in layers 22 and 28 represent the electrons associated with the bound positive charges for achieving overall charge neutrality. These "-" signs are divided into one part along junction 20 for inducing the basic electric field across the depletion region and another part located in layers 22 and 28 away from junction 20 for inducing the field portion that penetrates through silicide layer 22.

The work function is generally denoted as in electrostatic potential units or as q in energy units. ϕ_{SB} and ϕ_{MB} are the bulk values of the N-type semiconductor and the metal silicide, respectively, when they are not interacting (i.e., there is no silicide-semiconductor rectifying junction). ϕ_{SB} exists in the N-type semiconductor outside its charge depletion region. In order for rectification to occur, ϕ_{MB} exceeds ϕ_{SB}. Also, the work function ϕ_{MN} of non-silicide layer 28 (or the corresponding non-silicide layer in the reference diode) is less than ϕ_{MB} (since ϕ_{BN} is less than ϕ_{BO} here).

With these considerations in mind, a good starting place is the Fermi energy E_F which is constant in a Schottky-type diode in the absence of an applied voltage. The sum of E_F and the work function at any point in the diode is the energy E_H at which an electron is just free of the influence of the diode. Although E_H varies, it is continuous across any conductor-semiconductor interface or any conductor-conductor interface.

Looking first at the reference diode, the intrinsic work function ϕ_{SO} of its N-type region thereby increases from ϕ_{SB} outside the depletion region to a maximum at its rectifying junction as progressively more energy is needed to raise an electron to E_H. Since E_F is constant and E_H is continuous, ϕ_{SO} meets the intrinsic work function ϕ_{MO} of the silicide layer of the reference diode at its rectifying junction. At that point, ϕ_{MO} equals ϕ_{MB}.

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Near the interface between the silicide and non-silicide layers in the reference diode, ϕ_{MO} drops down to ϕ_{MN}.

In the diode of Fig. 1, the actual work function ϕ_S for N-region 24 similarly rises from ϕ_{SB} outside the depletion region to a maximum at junction 20 where ϕ_S meets the actual work function ϕ_M for silicide layer 22. Likewise, ϕ_M meets ϕ_{MN} at junction 30. The important difference between the reference diode and the rectifier of Fig. 1 is that ϕ_M is always less than ϕ_{MB} because of the electric-field penetration into non-silicide layer 28. This generally lowers ϕ_M as ϕ_{MO} mixes with lower-valued ϕ_{MN}. Accordingly, the value of ϕ_M at junction 20 is lower than ϕ_{MO} at the rectifying junction of the reference diode by an amount $\Delta\phi$.

The difference $\Delta\phi$ is reflected down as the difference between ϕ_{BO} and ϕ_B. This occurs because the difference qX between E_H and the lowest energy E_C in the semiconductor conduction band is constant from point to point. As E_H rises across the depletion region, E_C rises in the same manner. The change in E_C is the actual built-in semiconductor-to-conductor energy barrier $q\phi_I$ which is thereby $q\Delta\phi$ less than the intrinsic built-in semiconductor-to-conductor energy barrier $q\phi_{IO}$. Similarly, $q\phi_B$ is the difference between E_F and E_C at junction 20. Consequently, ϕ_{BO} exceeds ϕ_B by $\Delta\phi$.

Alternatively, ϕ_{MN} for non-silicide layer 28 might exceed ϕ_{MO}. ϕ_B would then exceed ϕ_{BO}. The dot-and-dash lines in Fig. 2a represent the actual energy variations for this complementary case, each of the relevant parameters being denoted with an "*". That is, the parameters ϕ_{MN}^*, ϕ_M^*, ϕ_{MO}^*, and ϕ_S for the complementary case correspond respectively to ϕ_{MN}, ϕ_M, ϕ_{MO}, and ϕ_S. In the complementary case, the basic device physics is largely the same as in the main case except that the various differences are reversed in sign. Accordingly, no further explanation is necessary here.

For a pair of conductors, the difference between

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their work functions is representative of the difference between their barrier heights with the same semiconductor. In particular, the difference between ϕ_{MO} and ϕ_{MN} is representative of the difference between ϕ_{BO} and ϕ_{BN}. The parameter $\left| (\phi_{BO} - \phi_B)/(\phi_{BO} - \phi_{BN}) \right|$, hereafter usually referred to as $\mathcal{E}$, is therefore indicative of the amount of work function mixing in the present diode.

Fig. 3 is a graph showing the experimental variation of ϕ_B with silicide thickness t for the PtSi diode. The end points on this curve are ϕ_{BO} when t is effectively infinite--i.e., about 1 00 nm-- and ϕ_{BN} when t is zero--i.e., N- region 24 directly adjoins non-silicide layer 28. Fig. 4 is a graph showing the corresponding curve for the variation of $\mathcal{E}$ with t.

Some statistical variation does exist in the data shown. In addition, there is some difficulty in ascertaining t because of limitations in the measurement apparatus/technique. Allowing for statistical variation and measurement accuracy, it is nonetheless clear that ϕ_B is significantly different from ϕ_{BO} when t is about 30. nm or less. This corresponds to the range beginning at point 58 in Fig. 4 where $\mathcal{E}$ is at least 15 %. More particularly, the curve starts to bend sharply near the point 60 at which $\mathcal{E}$ is about 25 %. The range for greater than 25 % is even more preferred since ϕ_B can vary greatly within this range for small changes in t.

Turning to Fig. 5, it illustrates an embodiment of the diode of Fig. 1 in which layer 22 is a silicide of nickel and platinum divided generally into a pair of layers 62 and 64. Lower layer 62 adjoins N- region 24 along interface 20 and consists of $Ni_YPt_{1-Y}Si$ where Y is variable between 0 and 1. Upper layer 64 adjoins non-silicide layer 28 along interface 30 and consists of $Ni_ZPt_{1-z}Si$ where Z is variable between 0 and Y. Accordingly, lower layer 62 is Ni-rich compared to upper layer 64. In the embodiment shown, Y is about 0.9, and Z is about 0.25. Non-silicide layer 28 again consists of Ti-W in

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the above proportions.

As stated above, the intrinsic barrier height ϕ_{BO} for the reference diode is defined with respect to a silicide layer having the same average composition as layer 22. This is important here because it takes into account the compositional difference between layers 62 and 64.

Layer 22 in the rectifier of Fig. 5 is preferably the remainder of an original silicide layer of greater thickness. In this case, ϕ_{BO} is defined with respect to a reference silicide layer which is the same as the original silicide layer along junction 20 and has the same average composition as the original silicide layer.

In the specific embodiment of Fig. 5, $q\phi_B$ is about 0.74 eV if the original silicide layer is formed to a thickness of about 1 00 nm in the manner described below. This value is approximately the appropriate $q\phi_{BO}$. The thickness t_L of lower layer 62 is slightly under 50 nm. Depending on the thickness t_U selected for upper layer 64, $q\phi_B$ can be adjusted to as low as 0.66 eV, this minimum arising when t_U is zero. Again, the effect is clear when $\mathcal{E}$ is 15% or more.

The ability to control ϕ_B by making upper layer 64 sufficiently thin is believed to occur because of electric-field penetration through silicide layer 22 into non-silicide layer 28. Although there are slight differences in the work-function mixing because layer 22 is divided into layers 62 and 64 of different average composition, the device physics is basically the same as described for Figs. 2a and 2b.

Figs. 6a, 6b, 6c and 6d illustrate steps in a method for fabricating the particular rectifier shown in Fig. 5. In this method, silicon semiconductor body 26 is initially processed in the manner described above for the rectifier of Fig. 1 up through the creation of the windows for the diode and the electrical contact (not shown here) down to the exposed silicon surfaces 66 of the N-portion

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68 remaining from the original epitaxial layer. At this point, the structure appears as shown in Fig. 6a in which N- region 68 downwardly adjoins buried region 36. Body 26 preferably also includes doped regions 42, 44 and 48 at this point as shown in Fig. 1 but not illustrated here. In the following steps, layers 50, 52 and 56 for the contact are preferably formed at the same time, with the same materials, and to the same thicknesses as layers 22, 28 and 32, respectively. To simplify the discussion, no further reference is made to the contact.

A metallic layer 70 of Ni-Pt in the proportions of 60 % nickel to 40 % platinum is now deposited according to conventional sputtering techniques to a thickness of about 50 nm on surface 66 as depicted in Fig. 6b. The structure is sintered for 20 minutes at 500° C in an environment of dry nitrogen with 1% hydrogen to cause the nickel and platinum to react with silicon along surface 66 and form an original silicide layer 72 which adjoins the remainder 24 of N- region 68 along interface 20 as shown in Fig. 6c. The resulting thickness of silicide layer 72 is about 1 00 nm, while its average composition is $Ni_{.6}Pt_{.4}Si$. During this sintering step, silicide layer 72 actually forms as lower silicide layer 62 and an original upper silicide layer 74. The average composition of lower layer 62 is about $Ni_{.9}Pt_{.1}Si$. The average composition of upper layer 74 is about $Ni_{.25}Pt_{.75}Si$. Any Ni-Pt that has not reacted to form silicide is then removed by etching with room-temperature aqua regia.

A portion of the thickness of upper layer 74 is removed by milling with argon ions so as to leave silicide layer 22 of which upper portion 64 is the remainder of original upper layer 74 as shown in Fig. 6d. A 1 00 nm layer of Ti-W at the above proportions is deposited according to conventional sputtering techniques on the top of the structure and suitably etched with hydrogen peroxide to define non-silicide layer 28 as shown in Fig. 5. In a similar manner, a layer of aluminium

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with about 1 % copper is deposited on the top of the structure and suitably patterned by etching with sulfuric/phosphoric acid to create layer 32. As indicated above, lower layer 62 is so thin that removal of the portion of original upper 74 enables ϕ_B to be reduced from about 0.74 eV when upper layer 74 is intact to about 0.66 eV when upper layer 74 is entirely gone.

The rectifier of Fig. 1 is particularly suitable for semiconductor structures containing Schottky-type diodes of different ϕ_B. Fig. 7 illustrates a side view of such a structure employable in an STL portion of an integrated circuit. Fig. 8 is the corresponding circuit diagram.

The structure centers around an NPN bipolar transistor Q whose N+ emitter 162 receives a supply voltage V_{EE} preferably at ground reference (0 volt) and whose P-base 164 receives a digital input signal V_I. Base 164 is also coupled through an input resistor R_I (not shown in Fig. 7) to another supply voltage V_{CC} which is preferably 2,5 volts. The collector of transistor Q is connected to the cathode of a Schottky-type diode S1 whose anode is connected to base 164. In addition to providing a direct digital output signal V_O, the collector is also connected to the cathodes of three substantially identical Schottky-type diodes S2A, S2B and S2C whose anodes provide further output digital signals V_{OA}, V_{OB} and V_{OC}, respectively. The actual conductor-to-semiconductor barrier height ϕ_{B1} for diode S1 exceeds the actual conductor-to-semiconductor barrier height ϕ_{B2} for any of diodes S2A, S2B and S2C. Consequently, the conductive forward voltage drop ϕ_{SH1} for diode S1 exceeds the conductive forward voltage drop ϕ_{SH2} for diode S2A, S2B, or S2C.

The rectifying junction 166 for diode S1 is at the interface between a metal silicide layer 168 and an underlying N- semiconductive region 170 in a monocrystalline silicon semiconductor body 172. Silicide layer 168 also extends laterally away from N- region 170 in such a

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manner as to downwardly adjoin P- region 164 at an ohmic junction 174. The rectifying junctions 76A, 76B and 76C for diodes S2A, S2B and S2C, respectively, lie at the interfaces between N- region 170 and metal silicide layers 78A, 78B and 78C, respectively.

Region 170 has a substantially uniform net N-type dopant concentration of no more than about 2×10^{17} atoms/cm^3 (corresponding to a resistivity of 0.05 ohm-cm). This assures that junctions 166, 76A, 76B and 76C are actually rectifying junctions. The optimum net N-type dopant concentration in region 24 is about 9.8×10^{15} atom/cm^3 (corresponding to a resistivity of about 0.3 ohm-cm).

While any of the metal silicides described above might be used in layers 168, 78A, 78B and 78C, the preferred silicide is PtSi. The thickness t_1 of layer 166 is 1 00 - 1 10 nm (or more). Accordingly, $q\phi_{B1}$ is about 0.81 eV. This is the corresponding intrinsic Schottky barrier height $q\phi_{B10}$. ϕ_{SH1} is then 430 mV at a junction current of 10 /ua. As in Fig. 1, the thickness t_2 of each silicide layer 78A, 78B or 78C is at least 1,5 nm and is preferably at least 5 nm. t_2 is no more than 10 nm and is optimally 5 - 6 nm. As a result, ϕ_{B2} depends on the material across from junctions 76A, 76B and 76C because of penetration of the self-induced electric fields entirely through layers 78A, 78B and 78C.

Electrically conductive non-silicide layers 80A, 80B and 80C consisting of about 1,00 nm of Ti-W alloyed in proportions of 85 % tungsten to 15 % titanium adjoin silicide layers 78A, 78B and 78C, respectively, along their upper surfaces. The Schottky barrier height $q\phi_{BN2}$ at an interface between Ti-W in the foregoing proportions and N-type monocrystalline silicon at the optimum dopant concentration above is about 0,65 eV. As a consequence, $q\phi_{B2}$ is about 0.72 eV at the optimum value of t_2, while ϕ_{SH2} is 340 mV at a junction current of 10 /uA. $q\phi_{B2}$ is thus significantly different from the intrinsic Schottky

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barrier height $q\phi_{B20}$ of 0.81 eV. The comparison parameter $\left| (\phi_{B20} - \phi_{B2})/(\phi_{B20} - \phi_{BN2}) \right|$ is about 56 % in this case. More generally, $\left| (\phi_{B20} - \phi_{B2})/(\phi_{B20} - \phi_{B2N}) \right|$ is at least 15 % and more preferably at least 25% as discussed for Fig. 4.

In the present case, ϕ_{B10} equals ϕ_{B20} since the net N-type dopant concentration along junctions 166, 76A, 76B and 76C in N- region 170 is the same and since silicide layers 168, 78A, 78B and 78C consist of PtSi -- i.e., they have the same average composition as well as the same composition along junctions 166, 76A, 76B and 76C. If this were not the case, ϕ_{B10} would generally not equal ϕ_{B20}.

Another 1 00 nm non-silicide layer 82 consisting of Ti-W alloyed in the foregoing proportions adjoins silicide layer 168 along its upper surface. The Schottky barrier height ϕ_{BN1} at an interface between Ti-W so alloyed and N-type monocrystalline silicon at the same dopant concentration as region 170 along interface 166 then equals ϕ_{BN2}.

If the dopant concentration in region 170 along interface 166 differed from that in region 170 along interfaces 78A, 78B and 78C, ϕ_{BN1} would not generally equal ϕ_{BN2}. This is also true if non-silicide layer 82 consists of a different material than that of non-silicide layers 80A, 80B and 80C.

Layers 84A, 84B and 84C consisting of a material suitable for electrically interconnecting non-silicide layers 80A, 80B and 80C, respectively, with other elements of the integrated circuit lie on the tops of layers 80A, 80B and 80C. Likewise, a layer 86 of the same material lies on the top of non-silicide layer 82. Layers 84A, 86B, 84C and 86 are preferably a highly conductive metal, optimally aluminium with about 1 % copper having a thickness of about 1,1 /um. Alternatively, they could consist of doped polycrystalline silicon or doped amorphous silicon.

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A P- substrate region 88 in body 172 underlies N- region 170. A highly doped N+ buried region 90 lies along the interface 92 between regions 170 and 88. Buried region 90, which extends about 6 microns below interface 92 and slightly above it as well, provides a conductive path for electrons travelling between parts of the structure. N-region 170, which extends about 3,7 /um upwards from interface 92 to the upper surface 94 of body 172, is basically an active semiconductive region laterally isolated from other such semiconductor regions by a deep annular highly doped P+ region 96 laterally surrounding region 170 and extending downwards about 5 00 nm below interface 92. N- region 170 laterally and upwardly surrounds P- region 164 which extends downward about 1,2 /um below surface 94. Similarly, P- region 164 laterally and upwardly encloses N+ region 162 along surface 94. The final semiconductive region in body 172 is a highly doped N+ region 98 laterally and upwardly enclosed by N- region 170. In combination, N-type regions 170, 90 and 98 form the collector for transistor Q. N+ regions 162 and 98 both extend about 1,0 /um downward from surface 94.

A patterned electrically insulating layer 100 of silicon dioxide whose thickness is 3 50 - 4 00 nm overlies body 172 along surface 94 except at the locations of silicide layers 168, 78A, 78B and 78C and at the locations of silicide layers 102 and 104 which ohmically adjoin N+ regions 162 and 98, respectively. Layers 102 and 104 preferably consist of PtSi having the same thickness as layers 78A, 78B and 78C. Layers 106 and 108 consisting of 1 00 nm of Ti-W in the above proportions lie on the top surfaces of silicide layers 102 and 104, respectively. Finally, layers 110 and 112 having the same thickness as layers 84A, 84B, 84C and 86 and consisting of the same highly conductive material lie on the tops of non-silicide layers 106 and 108, respectively.

Figs. 9a, 9b, 9c and 9d illustrate steps in a method for fabricating the structure of Fig. 8. Conven-

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tional masking, etching and cleaning techniques which are largely not further referred to in order to simplify the discussion are employed in creating the various doped regions and overlying layers. In many of the diffusion steps, the respective impurities could alternatively be introduced by ion implantation.

The starting material is a boron-doped P-monocrystalline silicon semiconductor substrate having a resistivity of about 7-21 ohm-cm. Arsenic is selectively diffused into the top surface of the substrate at the general location for N+ region 90. After exposing surface 92, an arsenic doped N- epitaxial layer having a resistivity of about 0.3 ohm-cm is grown on the top of the substrate. During this and subsequent processing steps, the arsenic suitably redistributes to form buried region 90 at a sheet resistance of 10-12 ohms/square.

A layer of silicon dioxide is thermally grown along the top of the structure. After opening a suitable window through this oxide layer, boron is diffused in through this window to form isolation region 96 at a sheet resistance of 5 ohms/square. A layer of silicon dioxide is thermally grown to close this window. After opening another window at the general location for P- region 164, boron is again diffused in to form a P- region having a sheet resistance of 200 ohms/square. Another layer of silicon dioxide is thermally grown to close this last window. After opening suitable windows through the now resulting oxide layer, phosphorus is diffused in to form N+ regions 162 and 98 at a sheet resistance of 10 ohms/square. Yet another layer of silicon dioxide is thermally grown to close the windows for regions 162 and 98. Layer 100 is the resultant oxide layer. At this point, the structure appears as in Fig. 9a. N- region 170 is the remainder of the original epitaxial layer that has not been further operated on, while base 164 is the remainder of the original diffused P- region excluding emitter 162.

In a first set of diode fabrication steps, a

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photoresist mask is employed in opening a window through oxide layer 100 at the site for diode S1. This window also overlies part of P- region 164. The structure is wet precleaned, after which an in situ sputter etch is performed with argon ions to move any silicon dioxide in the window for diode S1. This exposes silicon surface portion 114 of surface 94.

A metallic layer 116 of platinum having a thickness of about 50 nm is now deposited according to conventional sputtering techniques on the top of the structure including on surface 114 as depicted in Fig. 9b. The structure is sintered for 20 minutes at 450° C in a wet nitrogen environment to cause the platinum to react with silicon along surface 114 and form a PtSi layer 118 having a thickness of about 1 00 nm. In converting platinum to PtSi in steps such as this one, each unit of Si thickness reacts with about one unit Pt thickness to form about two units of PtSi thickness. Any platinum that has not reacted to form PtSi is removed by etching with hot aqua regia.

In a second set of diode fabrication steps, another photoresist mask is utilized in opening windows through oxide layer 100 at the sites for diodes S2A, S2B, and S2C and also above N+ regions 162 and 98. The structure is again wet precleaned, after which another in situ sputter etch is performed with argon ions to remove any silicon dioxide in the windows for diodes S2A, S2B and S2C and N+ regions 162 and 98. This respectively exposes surface portions 120A, 120B, 120C, 122 and 124 of surface 94.

A metallic layer 126 of platinum having a thickness of 2,5 - 3 nm is deposited according to conventional sputtering techniques on the top of the structure including on surfaces 120A, 120B, 120C, 122 and 124 as shown in Fig. 9c. In this deposition, a portion of metallic layer 126 is also deposited on the top of PtSi layer 118. The structure is sintered forten minutes at 450°C in a dry

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nitrogen environment to cause the platinum to react with silicon along surfaces 120A, 120B, 120C, 122 and 124 so as to form silicide layers 78A, 78B, 78C, 102 and 104. During this heating step, the portion of metallic layer 126 on PtSi layer 118 likewise reacts with adjacent silicon to convert layer 118 into silicide layer 168 which is 5 - 6 nm thicker. Any platinum that has not reacted to form PtSi is again removed by etching with hot aqua regia.

A 1 00 nm layer of Ti-W at the above proportions is deposited according to conventional sputtering techniques on the top of the structure and suitably etched with hydrogen peroxide to define layers 80A, 80B, 80C, 82, 106 and 108 as illustrated in Fig. 9d. In a similar manner, a layer of aluminium with about 1 % copper is deposited on the top of the structure and suitably patterned by etching with nitric/phosphoric/acetic acid to create layers 84A, 84B, 84C, 110 and 112 as shown in Fig. 7. The structure is then finished in a conventional manner.

In the structure of Fig. 7, fabricated as shown in Figs. 9a - 9d, ϕ_{B1} was chosen to equal ϕ_{B10}. In other structures which utilize the diode of Fig. 1, the silicide layer corresponding to layer 168 for diode S1 might be sufficiently thin that ϕ_{B1} does not substantially equal ϕ_{B10}. In this case, $\left| (\phi_{B10} - \phi_{B1})/(\phi_{B10} - \phi_{BN1}) \right|$ is again preferably not less than 15 % and even more preferably not less than 25 %.

While the invention has been described with reference to particular embodiments, this description is solely for the purpose of illustration and is not to be constructed as limiting the scope of the invention claimed below. For example, the non-silicide layer might consist of appropriately doped silicon or some other material that is not a barrier metal. Furthermore, in presence of two or more Schottky rectifiers the compositions of their non-silicide layers might differ even though their silicide

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layers consist of the same material. The compositions of the silicide layers might differ as long as at least one of them is so thin that ϕ_B is not substantially the same as ϕ_{BO} for that one. Thus, various modifications, changes, and applications may be made by those skilled in the art without departing from the true scope and spirit of the invention as defined by the appended claims.

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CLAIM

1. A semiconductor device comprising at least one Schottky type rectifier in which a semiconductor body has an N-type semiconductive region, a metal silicide layer adjoins the N-type region to define a rectifying junction at an interface therebetween, and a conductive non-silicide layer ohmically adjoins the silicide layer across from the junction, characterized in that the silicide layer is sufficiently thin that the actual conductor-to-semiconductor barrier height ϕ_B at the junction does not substantially equal the intrinsic conductor-to-semiconductor barrier height ϕ_{BO} at an interface between material which is the same as that of the N-type region along the junction and material which is the same as that of the silicide layer along the junction and has the same average composition as the silicide layer.

2. A semiconductor device as in Claim 1 characterized in that the absolute value of $(\phi_{BO} - \phi_B)/(\phi_{BO} - \phi_{BN})$ is not less than 0.15 where ϕ_{BN} is the conductor-to-semiconductor barrier height at an interference between material which is the same as that of the N-type region along the junction and material which is the same as that of the non-silicide layer.

3. A semiconductor device as in Claim 2 characterized in that the absolute value of $(\phi_{BO} - \phi_B)/(\phi_{BO} - \phi_{BN})$ is not less than 0.25.

4. A semiconductor device as in Claim 3 characterized in that a self-induced electric field penetrates through the entire thickness of the silicide layer and into the non-silicide layer.

5. A semiconductor device as in Claim 4 characterized in that the N-type region is substantially doped silicon and that the non-silicide layer is a metal layer.

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6. A semiconductor device as in Claim 2 wherein the silicide layer comprises PtSi, characterized in that the thickness t of the silicide layer is in the range of 1,5 - 25 nm.

7. A semiconductor device as in Claim 6 characterized in that t is at least 5 nm.

8. A semiconductor device as in Claim 7 characterized in that the N-type region is substantially doped silicon and that the non-silicide layer is a metal layer which acts substantially as a diffusion barrier to silicon and aluminium at a temperature not greater than 520° C.

9. A semiconductor device as in Claim 2 characterized in that the silicide layer comprises a first layer adjoining the N-type region and a second layer overlying the first layer across from the junction and having a different average composition than the first layer.

10. A semiconductor device as in Claim 9 characterized in that the average composition of the first layer is substantially $Ni_YPt_{1-Y}Si$ where Y is variable between 0 and 1 and that the average composition of the second layer is substantially $Ni_ZPt_{1-Z}Si$ where Z is variable between 0 and Y.

11. A semiconductor device as in any of Claims 1 - 10 characterized in that said metal silicide layer is constituted with at least two selected metals and in that said silicide layer is the remainder of an original metal silicide layer of greater thickness.

12. A semiconductor device comprising a second rectifier as in any of Claims 1 - 11 with a second N-type semiconductor region, a second silicide layer, a second rectifying junction and a second non-silicide layer and having an actual conductor-to-semiconductor barrier height ϕ_{B2} and an intrinsic barrier height ϕ_{B20}, characterized in that the device comprises in addition a first rectifier with a first N-type semiconductor region and a first metal silicide layer adjoining the first region to define a first rectifying junction having an actual conductor-to-

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semiconductor barrier height ϕ_{B1} different from ϕ_{B2}.

13. A semiconductor device as in Claim 12, characterized in that a further conductive non-silicide layer ohmically adjoins the first silicide layer across from the first junction, and in that the first silicide layer is sufficiently thin that ϕ_{B1} does not substantially equal the intrinsic conductor-semiconductor barrier height ϕ_{B10} at an interface between material which is the same as that of first region and material which is the same as that of the first silicide layer along the first junction and has the same average composition as the first silicide layer.

14. A semiconductor device as in Claim 13 characterized in that the absolute value of $(\phi_{B10} - \phi_{B1})/(\phi_{B10} - \phi_{BN1})$ is not less than 0.15 where ϕ_{BN1} is the conductor-to-semiconductor barrier height at an interface between material which is the same as that of the first region along the first junction and material which is the same as that of the further non-silicide layer.

15. A semiconductor device as in Claim 14, characterized in that the N-type regions are continuous with each other and have substantially the same net N-type dopant concentration along the junctions, and in that the silicide layers have substantially the same composition along the junctions and substantially the same average composition, whereby ϕ_{B10} equals ϕ_{B20}.

16. A semiconductor device as in Claim 15 characterized in that the non-silicide layers comprise the same material, whereby ϕ_{BN1} equals ϕ_{BN2}.

17. A semiconductor device as in any of Claims 12-16 characterized in that the silicide layers comprise the same metal silicide at different thicknesses.

18. A semiconductor device as in Claim 17 wherein a further conductive non-silicide layer ohmically adjoins the first silicide layer across from the first junction, characterized in that the non-silicide layers are metal layers of the same composition.

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19. A method of forming a semiconductor device as in any of Claims 1 - 18 characterized in that a metallic layer composed of at least two selected metals is deposited on an exposed surface of an N-type silicon semiconductive region in a semiconductor body after which the body and the metallic layer are heated to a suitable temperature to cause the metals to react with silicon along the surface and form an original metal silicide layer which adjoins the remainder of the N-type region along an interface therebetween, the metals and impurity dopant concentration of the N-type region being so selected that the interface is a rectifying junction, and comprising the step of removing a non-insubstantial portion of the thickness of the silicide layer across from the junction so as to leave a remaining metal silicide layer.

20. A method as in Claim 19, characterized by the step of forming a conductive non-silicide layer on the remaining silicide layer.

21. A method as in Claim 20 characterized in that the silicide layer forms as at least a first layer adjoining the remainder of the N-type region and an original second layer overlying the first layer across from the junction and having a different average composition than the first layer, that the step of removing involves removal of at least a part of the thickness of the original second layer, and that the first layer is sufficiently thin that removal of the part enables the actual conductor-to-semiconductor barrier height ϕ_B at the junction to be controlled depending on the degree of removal.

22. A method as in Claim 21 characterized in that the absolute value of $(\phi_{BO} - \phi_B)/(\phi_{BO} - \phi_{BN})$ is not less than 0.15 where ϕ_{BO} is the intrinsic conductor-to-semiconductor barrier height at an interface between material which is the same as that of the N-type region along the junction and material which is the same as that of the ori-

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ginal silicide layer along the junction and has the same average composition as the original silicide layer and where ϕ_{BN} is the conductor-to-semiconductor barrier height at an interface between material which is the same as that of the N-type region along the junction and material which is the same as that of the non-silicide layer.

23. A method as in Claim 22 characterized in that the average composition of the first layer is substantially $Ni_YPt_{1-Y}Si$ where Y is variable between 0 and 1 and that the average composition of the second layer is substantially $Ni_ZPt_{1-Z}Si$ where Z is variable between 0 and Y.

24. A method as in Claim 19 for manufacturing a semiconductor device as in Claim 12, characterized in that a first silicide layer is formed by depositing a first metallic layer composed of the metal material of the first silicide layer on an exposed surface of a first N-type silicon region after which the body and the first metallic layer are heated suitably to cause it to react with silicon of the first region, and in that the step of forming a second silicide layer involves timewise separately performing the steps of: depositing a second metallic layer composed of the metal material of the second silicide layer on an exposed surface of a second N-type silicon region; and subsequently heating the body and the second metallic layer suitably to cause it to react with silicon of the second region.

25. A method as in Claim 24 characterized in that the step of depositing the second metallic layer is performed after the step of heating the body and the first metallic layer and includes depositing a portion of the second metallic layer on the resulting metal silicide along the first region and that the step of heating the body and the second metallic layer includes heating the portion to cause it to react with silicon of the first region.

26. A method as in Claim 25 characterized in that the metallic layers are deposited at different thicknesses

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of the same material.

27. A method as in Claim 26 wherein a further conductive non-silicide layer is ohmically formed on the first silicide layer across from the first junction, characterized in that the non-silicide layers are formed of the same material at the same time.

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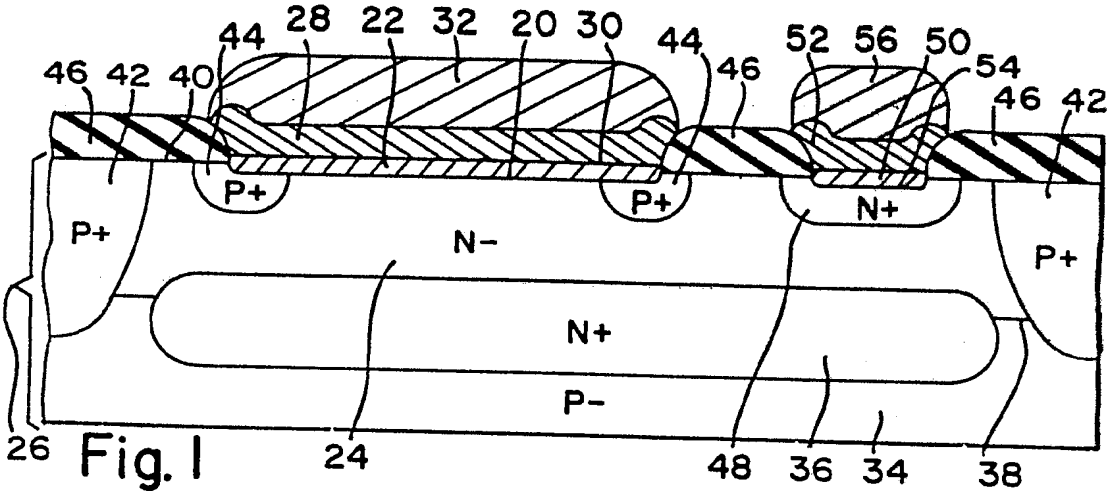


Fig. 1

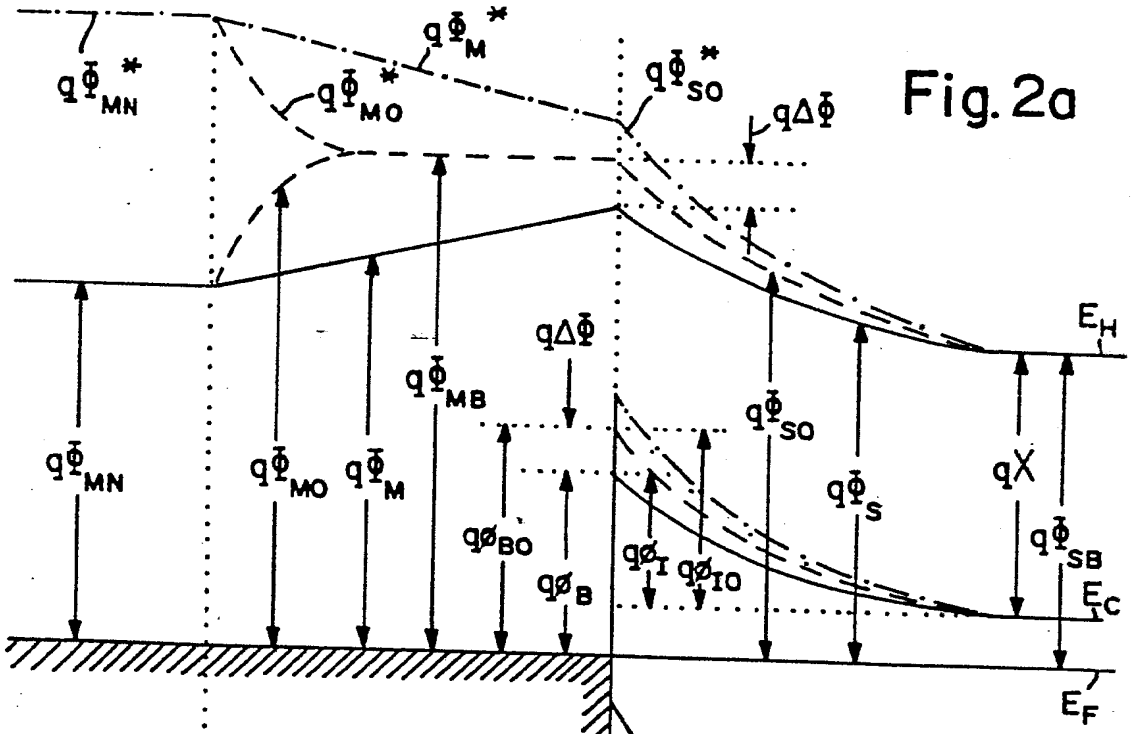


Fig. 2a

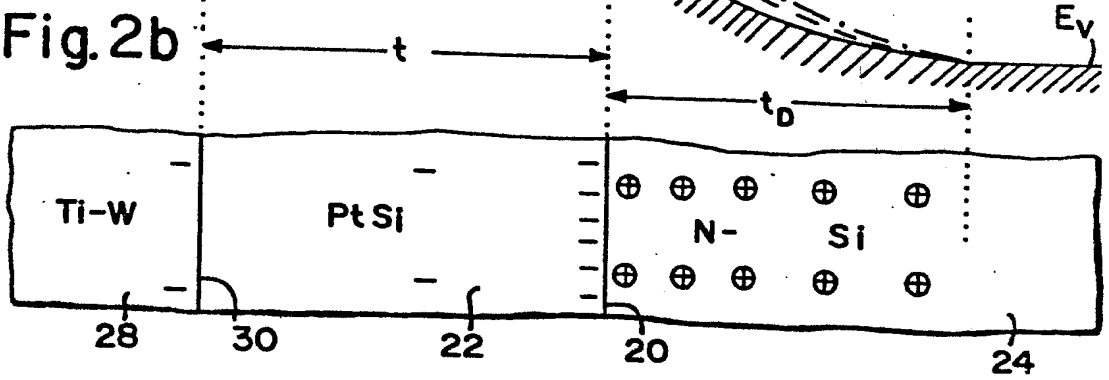


Fig. 2b

Fig. 3

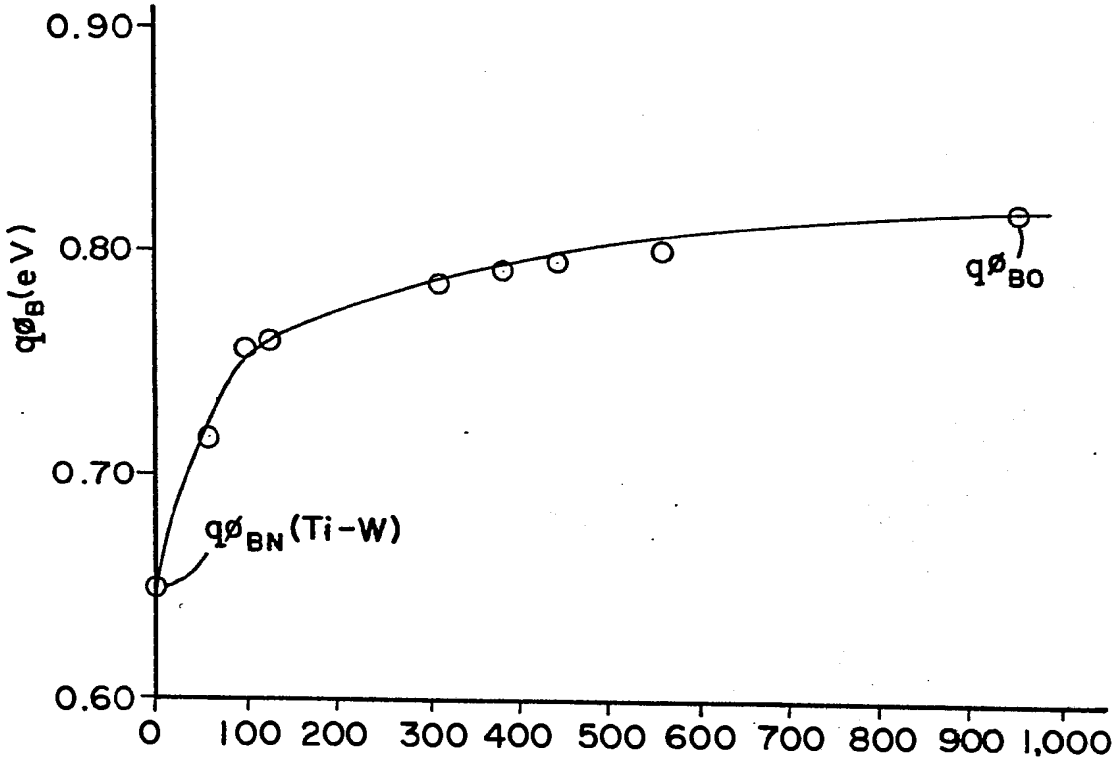
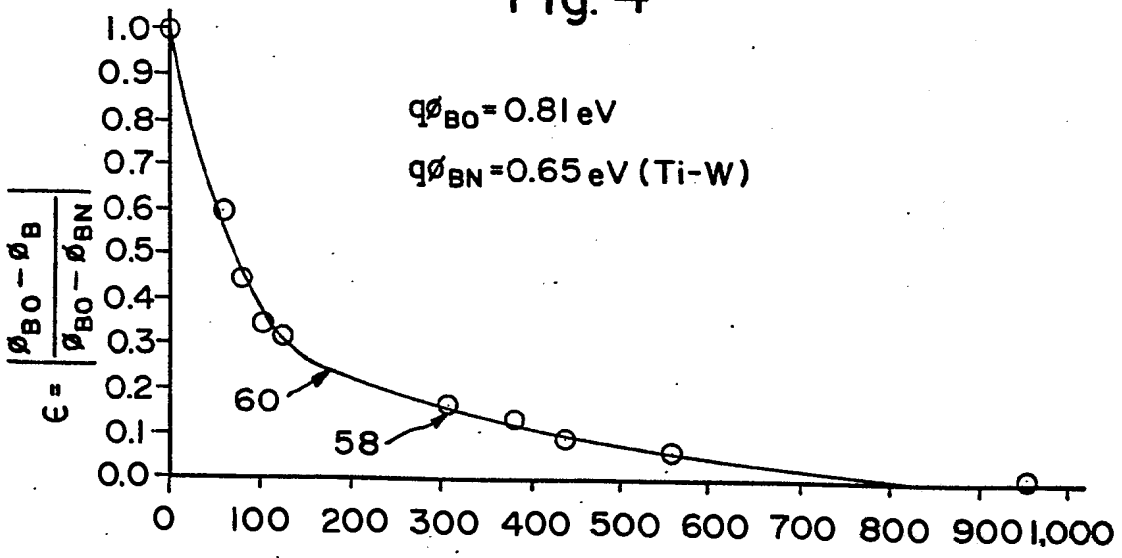


Fig. 4



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Fig. 5

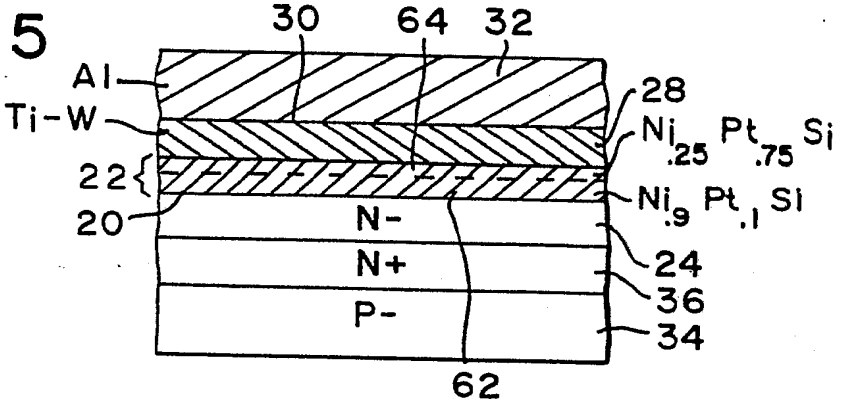


Fig. 6a

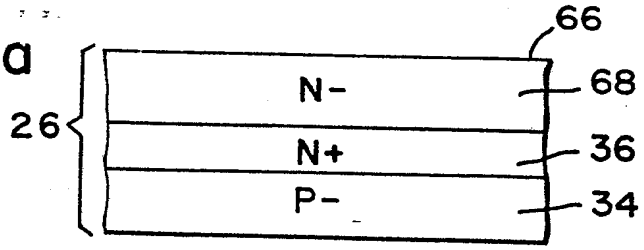


Fig. 6b

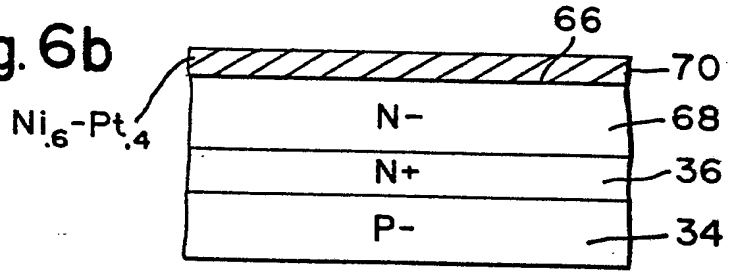


Fig. 6c

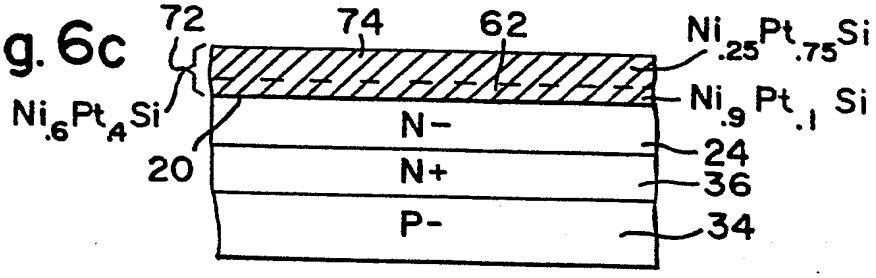
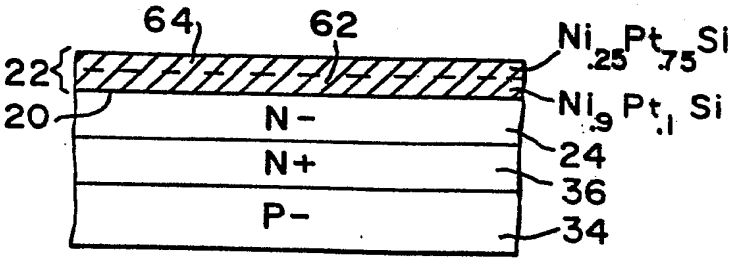


Fig. 6d



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Fig.7

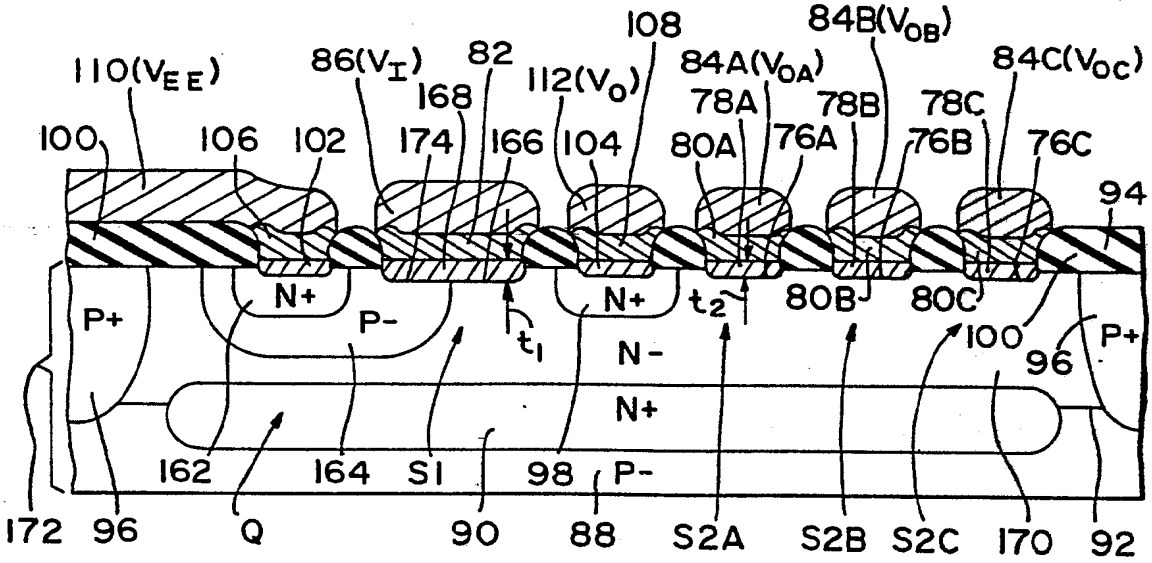
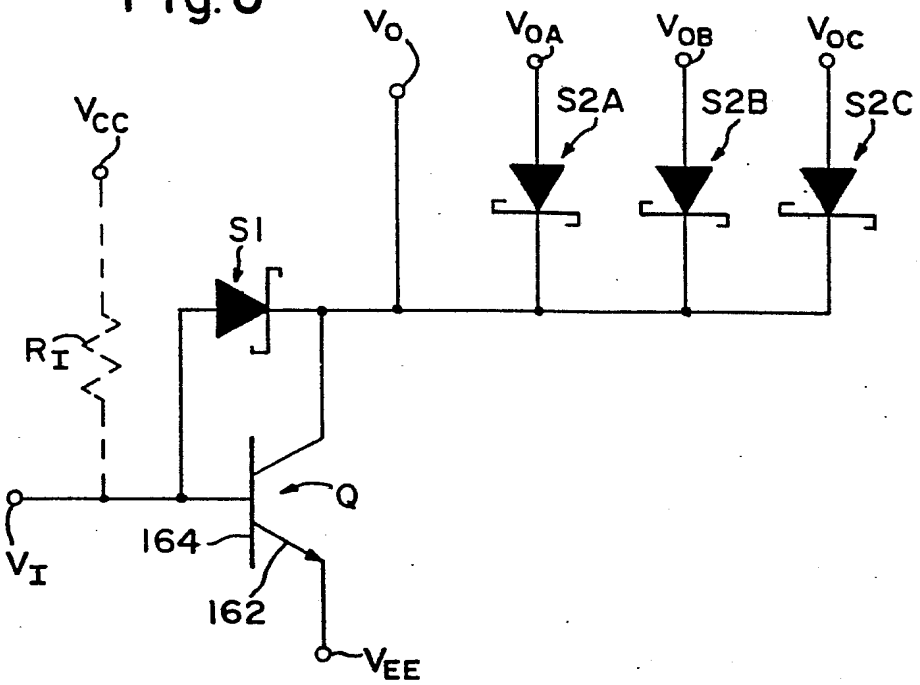


Fig.8



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Fig.9a

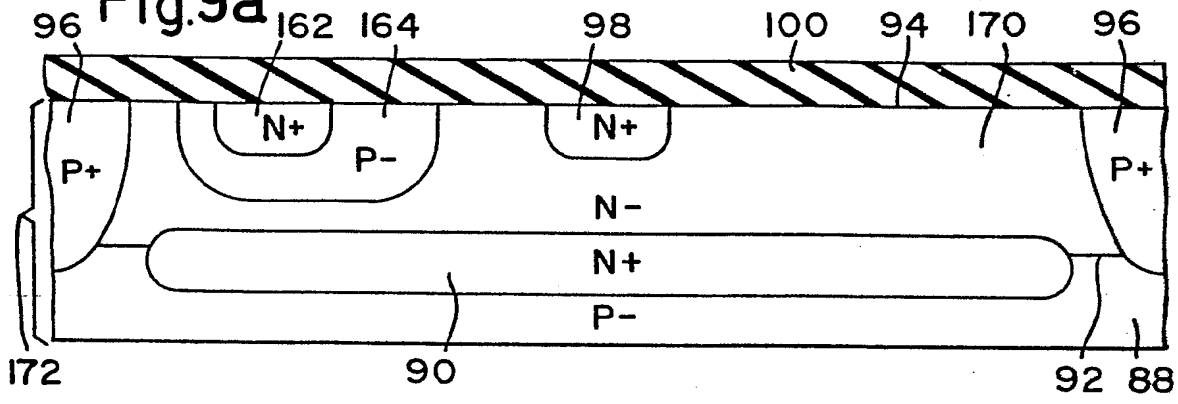


Fig.9b

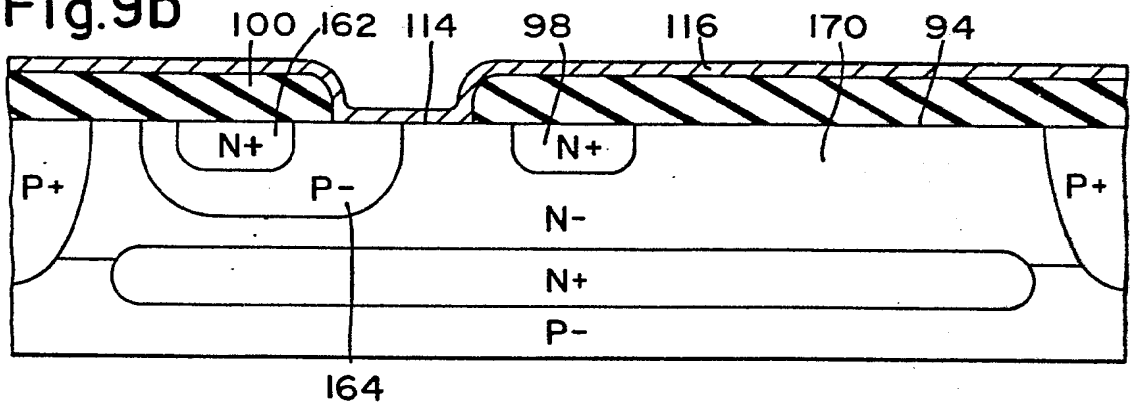


Fig.9c

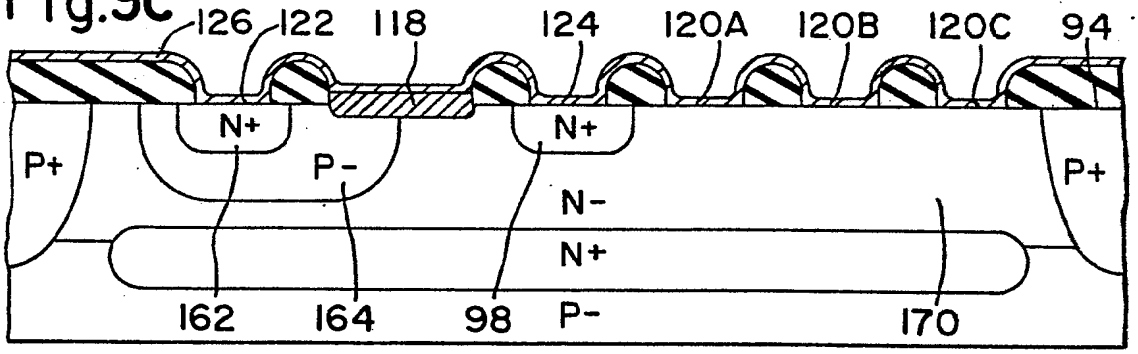
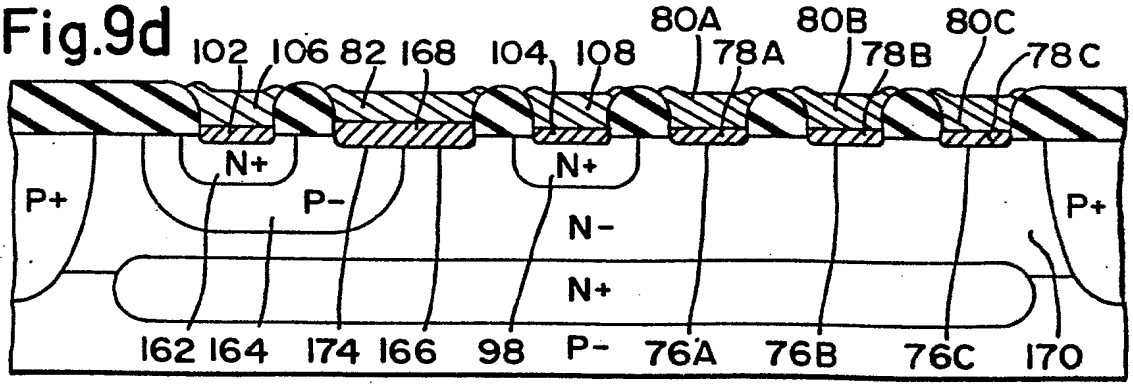


Fig.9d



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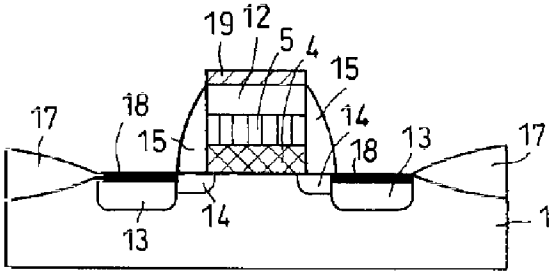
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(71)出願人　000003078
株式会社東芝
東京都港区芝浦一丁目１番１号
(72)発明者　小山　正人
神奈川県横浜市磯子区新杉田町８番地　株式会社東芝横浜事業所内
(72)発明者　西山　彰
神奈川県横浜市磯子区新杉田町８番地　株式会社東芝横浜事業所内
(74)代理人　100081732
弁理士　大胡　典夫　（外２名）

最終頁に続く

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】
【課題】チタン酸化物を直接シリコン基板上に形成する方法では、シリコンとチタン酸化物とが反応することで、SiO_2を主とする界面反応層が厚さ２ｎｍ以上形成されることにより、絶縁膜容量が実用できない水準にまで低下するという問題がある。
【解決手段】シリコン基板１と、前記シリコン基板１上に形成されたチタン及びシリコンを含む酸化物からなるバッファ層４と、前記バッファ層４上に形成されたチタン酸化物からなるゲート絶縁膜５と、前記ゲート絶縁膜５上に形成されたゲート電極１２と、前記シリコン基板１中の前記ゲート絶縁膜５下に形成されたチャネル領域と、前記シリコン基板１中に離間して形成され、それらの間にチャネル領域を位置する用にして設けられたソース領域及びドレイン領域とを具備し、前記バッファ層４は、膜厚２ｎｍ以下、チタン原子の原子濃度が１％以上８％以下であることを特徴とする半導体装置。



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【特許請求の範囲】
【請求項１】シリコン基板と、
前記シリコン基板上に形成されたチタン及びシリコンを含む酸化物からなるバッファ層と、
前記バッファ層上に形成されたチタン酸化物からなるゲート絶縁膜と、
前記ゲート絶縁膜上に形成されたゲート電極と、
前記シリコン基板中の前記ゲート絶縁膜下に形成されたチャネル領域と、
前記シリコン基板中に離間して形成され、それらの間に前記チャネル領域を位置するようにして設けられたソース領域及びドレイン領域とを具備し、
前記バッファ層は、膜厚２ｎｍ以下、チタンの原子濃度が１％以上８％以下であることを特徴とする半導体装置。
【請求項２】前記バッファ層と前記シリコン基板との間に、膜厚１ｎｍ以下のSiO_2層が形成されていることを特徴とする請求項１記載の半導体装置。
【請求項３】シリコン基板表面に形成された酸化膜を剥離する工程と、
チタン酸化物をターゲットとし、酸素流量が０ｓｃｃｍ以上１．２ｓｃｃｍ以下の条件で、スパッタリングすることにより、前記シリコン基板上に、チタン及びシリコンを含む酸化物からなり、膜厚２ｎｍ以下、チタンの原子濃度が１％以上８％以下であるバッファ層を形成する工程と、
チタン酸化物をターゲットとし、酸素流量が１０ｓｃｃｍ以上の条件で、スパッタリングすることにより、前記バッファ層上に、チタン酸化物からなるゲート絶縁膜を形成する工程とを具備することを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置及びその製造方法に関する。特にチタン酸化物をゲート絶縁膜として用いた電界効果トランジスタとその製造方法に関する。
【０００２】
【従来の技術】ゲート長が０．１μｍ以下となる電界効果トランジスタの世代では、ゲート絶縁膜がSiO_2換算膜厚で１．５ｎｍ以下で駆動する性能が要求されている。従来どおりゲート絶縁膜にSiO_2を用いると、厚さが１．５ｎｍ以下であるのでトンネル電流が主となるリーク電流が多くなる問題がある。このリーク電流は、比較的消費電力が高くても高速性を求めるロジック回路ですら無視できないほど高く、リーク電流を防止し消費電力を低下することが課題となっている。
【０００３】そこで、SiO_2よりも比誘電率の大きな高誘電体材料をゲート絶縁膜として利用し、駆動性能を維持しつつ物理的なゲート膜厚を厚くすることでトンネル電流を阻止し、消費電力を低下する技術の研究開発が盛んに行われている。
【０００４】高誘電体材料として検討されている材料としてTiO_2、Ta_2O_5、ZrO_2、HfO_2、La_2O_3等の金属酸化物がある。これらの金属酸化物のうちで最も比誘電率が高いのはTiO_2(チタン酸化物)である。チタン酸化物は、ＤＲＡＭ等のキャパシタの誘電材料としてＬＳＩで常用されてきた実績もあり、チタン酸化物を電界効果トランジスタのゲート絶縁膜として用いる研究開発が盛んになされている。
【０００５】しかしながらチタン酸化物はシリコンと反応性が高く、チタン酸化物をシリコン基板上に堆積する過程で、チタン酸化物膜とシリコン基板との界面に主にSiO_2からなる界面反応層が２ｎｍ以上形成されるという問題がある。
【０００６】このSiO_2を主とする界面反応層は、比誘電率がSiO_2なみに低いため、チタン酸化物膜と界面反応層とが積層された絶縁膜では、その電気的容量値がほとんど界面反応層の容量値で決定されてしまうという問題がある。また、このSiO_2を主とする界面層は厚さが２ｎｍ以上必然的に形成されてしまうために、ゲート絶縁膜としてSiO_2換算での要求される膜厚１．５ｎｍ以下を達成できないという問題もある。
【０００７】そこで、この界面反応層を形成しないように、ＳｉＯＮやＳｉＮ等の窒素を含む薄膜を、予めシリコン基板上に形成しておき、この窒素を含む薄膜上にチタン酸化物を成膜することが試みられている。しかしながらこの方法では、SiO_2を主とする界面反応層を抑制することはできるが、窒素を含む薄膜の性質によってゲート絶縁膜とシリコン基板との界面特性が大きく異なる結果をもたらす。例えば、ゲート絶縁膜とシリコン基板との界面付近に存在する窒素によって電気的特性が劣化する場合がある。具体的には、窒素原子による固定電荷に代表される余剰電荷、界面準位などの起源となる欠陥が多数界面に発生し、デバイス特性を劣化させてしまう。
【０００８】
【発明が解決しようとする課題】上述したように、チタン酸化物を直接シリコン基板上に形成する方法では、シリコンとチタン酸化物とが反応することで、SiO_2を主とする界面反応層が厚さ２ｎｍ以上形成されることにより、絶縁膜容量が実用できない水準にまで低下するという問題がある。
【０００９】また、窒素を含む薄膜をバッファ層として、この界面反応層を抑制する試みがなされているが、こんどは窒素による界面特性の劣化が著しく未だ実用にはいたっていない。
【００１０】本発明は、上記問題点を解決するためになされたもので、高品質な界面特性を実現し、かつSiO_2換算で１．５ｎｍ以下の性能を有する高い絶縁膜容量

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の実現及びトンネル電流の抑制とを両立する半導体装置を提供することを目的とする。

【００１１】また、本発明は、このようなゲート絶縁膜をシリコン基板上に形成することができる半導体装置の製造方法を提供することを目的とする。

【００１２】

【課題を解決するための手段】上記目的を達成するために、本発明は、シリコン基板と、前記シリコン基板上に形成されたチタン及びシリコンを含む酸化物からなるバッファ層と、前記バッファ層上に形成されたチタン酸化物からなるゲート絶縁膜と、前記ゲート絶縁膜上に形成されたゲート電極と、前記シリコン基板中の前記ゲート絶縁膜下に形成されたチャネル領域と、前記シリコン基板中に離間して形成され、それらの間に前記チャネル領域を位置するようにして設けられたソース領域及びドレイン領域とを具備し、前記バッファ層は、膜厚２ｎｍ以下、チタンの原子濃度が１％以上８％以下であることを特徴とする半導体装置。

【００１３】また、前記バッファ層と前記シリコン基板との間に、膜厚１ｎｍ以下のSiO_2層が形成されていてもよい。

【００１４】前記バッファ層は、若干の窒素を含有しても良い。

【００１５】また、本発明は、シリコン基板表面に形成された酸化膜を剥離する工程と、チタン酸化物をターゲットとし、酸素流量が０ｓｃｃｍ以上１．２ｓｃｃｍ以下の条件で、スパッタリングすることにより、前記シリコン基板上に、チタン及びシリコンを含む酸化物からなり、膜厚２ｎｍ以下、チタンの原子濃度が１％以上８％以下であるバッファ層を形成する工程と、チタン酸化物をターゲットとし、酸素流量が１０ｓｃｃｍ以上の条件で、スパッタリングすることにより、前記バッファ層上に、チタン酸化物からなるゲート絶縁膜を形成する工程とを具備することを特徴とする半導体装置の製造方法を提供する。

【００１６】本発明では、SiO_2を主とする界面反応層を抑制するためにチタン酸化物を形成する前に、予めシリコン基板上にチタン原子、シリコン原子及び酸素原子からなるバッファ層を形成している。そして絶縁膜容量の値を著しく劣化させること無く、さらにシリコン基板との界面特性を高品質に保持するために、バッファ層の構成原料の比及びその膜厚を種々研究した結果、膜厚が２ｎｍ以下で、その構成元素がチタン及びシリコンを含む酸化物からなり、さらにそのチタンの原子濃度を１％以上８％以下にすることで上記目的を達成できることを見出した。

【００１７】このときのバッファ層は少なくとも０．５ｎｍの膜厚であればよい。また、原子濃度とはその膜中に存在する全ての原子数に対して、その膜中を構成する原子の割合を表す。

【００１８】

【発明の実施の形態】以下本発明の好ましい実施形態について図面を用いて詳細に説明する。

【００１９】先ず、本発明の実施形態を説明するに先立って、従来技術の問題点を見出すために、チタン酸化物膜をシリコン基板上に直接成膜してみた。

【００２０】図1に、従来のＣＶＤ（ケミカルベイパーディポジッション）法により、シリコン基板上にチタン酸化膜を成膜したときの概念図を示す。

【００２１】先ず、図１（ａ）に示すように、予め自然酸化膜を除去したシリコン基板１を用意する。そしてこのシリコン基板１表面上に、チタンを含む有機金属ガス等のチタン原料ガス２及び酸素ガス３をシリコン基板1上に供給する。

【００２２】すると図１（ｂ）に示すように、このＣＶＤによる成膜方法では、シリコン基板１とチタン酸化物膜５の界面にはSiO_2を主成分とする界面反応層４が厚さ約２ｎｍできてしまう。

【００２３】また、図2に、従来のチタンをターゲットとしたスパッタリング法により、シリコン基板上にチタン酸化膜を成膜した時の概念図を示す。

【００２４】この方法では、先ず、図２（ａ）に示すように、予め自然酸化膜を除去したシリコン基板１を用意する。そしてこのシリコン基板１表面上に、チタンターゲット６に励起されたアルゴン７を照射して、酸素雰囲気８中にてＴｉ－Ｏ及びＴｉを供給する。

【００２５】すると図2(b)に示すように、このスパッタリングによる成膜法でも、シリコン基板１とチタン酸化物膜５の界面にはSiO_2を主成分とする界面反応層４が厚さ約２ｎｍできてしまうことがわかった。

【００２６】これらの従来の成膜法に共通しているのは、シリコン基板１上にチタン酸化物が形成される初期の段階に、シリコン表面が多量の酸素に晒されていることである。このことは、化学的に活性なシリコン基板１の表面にチタンよりも酸素を多量に供給してしまうことであり、低誘電率なSiO_2を主とする界面反応層４を厚さ２ｎｍ以上成膜してしまう原因となる。従来は、チタン酸化物のバルク特性を高めるために成膜時に酸素ガスの供給量を過剰する傾向があった。これは一般にチタン酸化物は酸素原子が抜けやすいためで、酸素ガスの供給を過剰にしなければ組成比がストイキオメトリにならないためである。

【００２７】しかしながらこのとき生じる界面反応層は、少なくとも厚さが２ｎｍとなり、さらにSiO_2を主成分とすることから比誘電率は４程度と低くなり絶縁膜容量が低下してしまう。

【００２８】本発明者らは以上の考察より、最初に酸素ガスの供給量を少なくし或いは全く供給せず、ターゲットとしてチタン酸化膜を用いてチタン酸化膜からなるバッファ層をシリコン基板上に形成する。そしてこのバッ

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ファ層上に改めて酸素ガスを十分供給する雰囲気中にて、チタン酸化物をターゲットとしてスパッタリングによりチタン酸化物からなるゲート絶縁膜を形成する。こうすることでSiO_2を主とする界面反応層の形成を防げることを見出した。

【００２９】図３に、本発明のチタン酸化膜からなるゲート絶縁膜の成膜方法を説明する概念図を示す。

【００３０】先ず、図３（ａ）に示すように、予め自然酸化膜が除去されたシリコン基板１を用意する。このシリコン基板１の表面上に、チタン酸化物からなるターゲット９に活性化されたアルゴン７を照射しスパッタリングする。こうすることでシリコン基板１上にＴｉ－ＯやＴｉが供給される。このときの酸素供給量は極力少なくするか或いは供給を全くしないようにする。しかしながらターゲットをチタン酸化物としたので、このチタン酸化物から酸素８が蒸発しシリコン基板１の表面に供給される。

【００３１】こうして図３（ｂ）に示すように、シリコン基板１上にチタン及びシリコンを含む酸化物からなるバッファ層１０が形成される。この反応はチタン酸化物の成膜とシリコン基板１表面の酸化が同時に進行する形となり、バッファ層１０にはチタン及びシリコンと酸素が混在することになる。

【００３２】次に、図３（ｃ）に示すように、酸素ガス８を十分に供給し、チタン酸化物ターゲット９に励起したアルゴン７を照射し、バッファ層１０上にＴｉ－Ｏ及びＴｉを供給する。このときの反応は酸素ガス８が十分に供給されているので、チタン原子と酸素原子はストイキオメトリに近く非常に電気的特性の優れたチタン酸化物を形成できる。図３（ｄ）は、これによりチタン酸化物からなるゲート絶縁膜１１がバッファ層１０上に形成された図である。

【００３３】このようにバッファ層を形成するときのプロセスを酸素の供給を少ないかゼロにし、ゲート絶縁膜を形成するときのプロセスを十分な酸素供給の条件で行う２段階プロセスとすることで、バルク特性に優れたチタン酸化物と比誘電率が高いチタン及びシリコンを含む酸化物からなるバッファ層を実現できる。

【００３４】図４は、バッファ層の組成分析結果を示す図である。

【００３５】図４に示すように、バッファ層にはチタン原子、シリコン原子及び酸素原子が含まれることが分かる。上述したようにチタンを含有していることでこのバッファ層はSiO_2よりも誘電率が高くなる。

【００３６】次に、図５にバッファ層の比誘電率を縦軸、バッファ層中のチタンの原子濃度を横軸にとったグラフを示す。

【００３７】図５から分かるように、$TiSi_xO_y$膜中のチタンの原子濃度が高くなると$TiSi_xO_y$膜の誘電率は高くなる。しかしチタン原子の含有量が高くなりすぎると、チタンがTiO_2とSiO_2とに相分離し、チタン酸化物の結晶化、それに伴うリーク電流が増大する問題がある。またSiO_2が相分離することにより比誘電率が低下する問題もある。このTiO_2とSiO_2との相分離はチタンの原子濃度が８％を越える辺りから顕在化することが分かった。そこで本発明ではチタン及びシリコンを含む酸化物からなるバッファ層のうち、チタンの原子濃度を８％以下と規定した。

【００３８】また、図５から分かるように、チタンの原子濃度が低すぎると比誘電率が下がり、チタンの原子濃度が１％よりも低いと比誘電率が５よりも低くなる。このことはバッファ層の膜厚を例えば膜厚２ｎｍとすると、SiO_2換算膜厚が１．６ｎｍとなり、０．１μｍ世代のスペックであるSiO_2換算膜厚が１．５ｎｍを満たすことができない。そこで本発明ではチタンの原子濃度を１％以上と規定した。このときのバッファ層の膜厚は２ｎｍ以下としなければならない。本発明の方法では、バッファ層をスパッタ法により形成しているので膜厚の制御は容易にできる。本発明者らの実験では、バッファ層の膜厚を１．５ｎｍ以下にすることも可能となっている。バッファ層の膜厚としては、次のチタン酸化物成膜時にSiO_2界面層が発生しない程度であればよく０．５ｎｍ以上であれば良い。ただし０．１ｎｍ以下のSiO_2であればSiO_2換算膜厚としても十分に薄いので界面層として生じても問題ない。

【００３９】またこれらの考察より$TiSi_xO_y$からなるバッファ層は、チタン原子の原子濃度が２％以上４％以下であることが好ましい。本発明に係るバッファ層は微視的に見るとTiO_2とSiO_2の混合物となっていることが好ましい。また、バッファ層において、シリコンは原子濃度で２０％以上４０％以下、より好ましくは２５％以上３５％以下である。また酸素の原子濃度は６５％以上７０％以下であることがシリコン基板とバッファ層の界面特性と絶縁膜容量の向上を両立させるためには好ましい。

【００４０】また、バッファ層に例えば$1\times10^{20}/cm^3$以下程度の窒素原子が混在しても差し支えない。

【００４１】本発明では、バッファ層の形成時にチタン酸化物成膜初期に酸素流量を抑制することは、バッファ層の膜厚を２ｎｍ以下にする効果もある。具体的には酸素を完全に排除することでバッファ層を１．５ｎｍ以下にまで薄くできる。

【００４２】本発明では、バッファ層を形成するときの酸素の供給量を０ｓｃｃｍ以上、２ｓｃｃｍ以下としＴｉとＯの比がストイキオメトリ（TiO_2）になるよりも十分に低くなるようにしている。ここでバッファ層の厚さやチタン原子の原子濃度、比誘電率はこの酸素供給量によって大きく影響を受ける。比誘電率を高くしてバッファ層の絶縁膜容量を高くするためには、酸素は完全に除去することが好ましい。一方チタンの原子濃度が高

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くなると若干のリーク電流が流れるため、リーク電流の低さを優先させるためには、若干の酸素を流すことが良い。

【００４３】以上詳述したような方法によって、バッファ層をシリコン基板上に形成したあと、チタン酸化物のバルク特性を高めるのに最適な、酸素大量に供給しながらスパッタする方法を用いると良いてゲート絶縁膜を形成すればよい。

【００４４】図６に、シリコン基板上に、$TiSi_xO_y$からなるバッファ層、このバッファ層上に形成されたチタン酸化物膜を示す。

【００４５】図６に示すように、バッファ層のチタンの原子濃度が２％以上８％以下、好ましくは４％以下、膜厚が２ｎｍ以下となれば理想的な界面特性を得ることができる。

【００４６】図８は、上述した本発明の方法を用いてゲート絶縁膜を形成した電界効果トランジスタの断面図である。

【００４７】図７に示すように、この電界効果トランジスタは、シリコン基板１と、シリコン基板１上に形成されバッファ層４と、バッファ層４上に形成された多結晶シリコン等からなるゲート絶縁膜５と、ゲート絶縁膜上に形成されたゲート電極１２とを具備している。

【００４８】バッファ層４は、チタン及びシリコンを含む酸化物から構成され、チタンの原子濃度が１％以上８％以下、膜厚が２ｎｍ以下となるように形成されている。ゲート絶縁膜５は、チタン酸化膜で構成されている。

【００４９】バッファ層４／ゲート絶縁膜５／ゲート電極１２の積層構造の側壁には、シリコン酸化物或いはシリコン窒化物等からなるゲート側壁１５が形成されている。シリコン基板１中のゲート絶縁膜５下の位置には、チャネル領域が形成されている。このチャネル領域を挟む位置には高濃度に不純物を拡散した深い拡散領域１３及び浅い拡散領域１４が形成され、ソース領域／ドレイン領域を構成している。符号１７は素子分離領域である。また、符号１８は、深い拡散領域１３上に形成されたサリサイド、符号１９は、ゲート電極１２上に形成されたサリサイドである。

【００５０】次に、図８を参照して、図７に示す電界効果トランジスタの製造方法について説明する。

【００５１】先ず、図８（ａ）に示すように、シリコン基板１上の所定の位置に、通常の工程によりシリコン酸化物等からなる素子分離領域１７を形成する。次に、シリコン基板１上の自然酸化膜を希ＨＦ溶液処理により剥離し、シリコン表面を水素終端する。この工程は、Ｓｉ表面に余分な酸化膜を形成させないために極めて重要である。

【００５２】次に、図８（ｂ）に示すように、シリコン基板１上に、チタン原子、シリコン原子及び酸素原子から構成されるバッファ層１７を形成する。この工程は、図３（ａ）（ｂ）で説明したスパッタ法を用いた。

【００５３】具体的には、TiO_2をターゲットとして用い、ＲＦスパッタリングにより励起したアルゴンをターゲットに照射して堆積した。この時のガス流量条件は、Ａｒガスを２０ｓｃｃｍとし、酸素流量を０ｓｃｃｍから１．２ｓｃｃｍまでの範囲で違う条件でバッファ層を形成した。この工程により、膜厚１．３ｎｍ（酸素が０ｓｃｃｍの条件）～１．８ｎｍ（酸素が１．２ｓｃｃｍの条件）のバッファ層を形成した。当然のことながら、素子分離領域１７上にはＴｉＯｘ（ｘ＜２）が堆積する。

【００５４】次に、図８（ｃ）に示すように、全面に高誘電率なチタン酸化物膜７を堆積する。この工程は、図３（ｃ）（ｄ）で説明したスパッタ法を用いた。

【００５５】具体的には、TiO_2をターゲットとして用い、ＲＦスパッタリングにより励起したアルゴンをターゲットに照射し堆積した。この時のガス流量条件は、Ａｒガスを１０ｓｃｃｍとし、酸素ガスを１０ｓｃｃｍとした。これは組成比がストイキオメトリに近く非常に電気的特性の優れたチタン酸化物を堆積するための条件である。このときのチタン酸化物４の膜厚は、リーク電流のことを考慮して１ｎｍ以上であることが好ましい。

【００５６】これらのスパッタ工程は、同じ装置内で、ガス流量条件だけを変更して連続して行った。こうすることで真空が破られることはなく、厳密に管理されたガス雰囲気中において、バッファ層４及びゲート絶縁膜７を形成できる。このことは絶縁膜に対する汚染（炭素、酸素、窒素など）を排除して絶縁膜の特性を向上させるうえで大変重要である。

【００５７】次に、図８（ｄ）に示すように、通常の工程によりＴｉＮ、ポリシリコンなどのゲート電極材料を堆積し、エッチングによって加工しゲート電極１２を形成する。次に、ゲート電極１２をマスクとし、不純物をイオン注入することによって浅い拡散領域１４を形成する。次に、全体に酸化シリコン或いは窒化シリコンを堆積し異方性エッチングすることによって、バッファ層４／ゲート絶縁膜５／ゲート電極１２の側面にゲート側壁５を形成する。次に、ゲート電極１２及びゲート側壁１５をマスクとし、不純物をイオン注入することによって深い拡散領域１３を形成する。このときの不純物の加速電圧は浅い拡散領域１４よりも高くすれば良い。これらの不純物注入は、ゲート電極１２中にも同時に行われる。次に、浅い拡散領域１４及び深い拡散領域１３及びゲート電極１２に注入した不純物イオンを活性化のための熱処理を行う。

【００５８】この熱処理温度は、ゲート電極１２に用いる材料に依存して若干変化し、典型的には９００℃～１０５０℃程度の熱処理が必要である。この条件で熱処理した場合のシリコン基板１／ＴｉＳｉＯバッファ層４／

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チタン酸化物ゲート絶縁膜５ゲート電極１２の積層構造の断面図を図９に示す。図９（ａ）は、熱処理前、図９（ｂ）は熱処理後を示す。

【００５９】チタン酸化物膜５は平坦性を保っていて、Ｔｉ－Ｓｉ－Ｏバッファ層４は（ａ）熱処理前と、（ｂ）熱処理後とほとんど膜厚が変化しない。つまりチタン酸化膜５における凝集の問題は無く、バッファ層４の再成長による容量低下の問題もほぼ無視できる。

【００６０】このように、本発明の積層絶縁膜構造は従来のＣＭＯＳ工程に十分対応できる耐熱性を有している。

【００６１】次に、Ｃｏを蒸着して熱処理することによって、図７に示すように深い拡散領域１３上にサリサイド１８、ゲート電極１２上にサリサイド１９を形成することによって、前述した電界効果トランジスタを形成できる。

【００６２】図１０は、このようにして作成した（ａ）電界効果トランジスタ及び酸化シリコンをゲート絶縁膜として用いた電界効果トランジスタのゲート電圧とソースドレイン電流の電気的特性を示した図である。

【００６３】本発明の電界効果トランジスタの特性（ａ）は、界面特性の指標であるＳファクタ（ドレイン電流の１桁変化に対するゲート電圧の変化量）が、シリコン酸化膜をゲート絶縁膜として用いた電界効果トランジスタの特性（ｂ）とほぼ同程度であり、高品質な界面特性を示していることが分かる。

【００６４】

【発明の効果】以上詳述したように本発明によれば、高品質な界面特性を実現し、かつSiO_2換算で１．５ｎｍ以下の性能を有する高い絶縁膜容量の実現及びトンネル電流の抑制とを両立する半導体装置を提供することができる。

【００６５】また、本発明は、このようなゲート絶縁膜をシリコン基板上に形成することができる半導体装置の製造方法を提供することができる。

【図面の簡単な説明】

【図１】　ＣＶＤによりシリコン基板上にチタン酸化物膜を堆積する工程を示す図。

【図２】　反応性スパッタによりシリコン基板上にチタン酸化物膜を堆積する工程を示す図。

【図３】　本発明に係る方法によりシリコン基板上にバッファ層及びチタン酸化物膜をこの順に堆積する工程を示す図。

【図４】　本発明に係る方法により堆積したバッファ層の元素分析結果を示す図。

【図５】　本発明に係る方法により堆積したバッファ膜の比誘電率とＴｉ原子の原子濃度の関係を示す実験結果を示す図。

【図６】　本発明に係る方法により堆積したシリコン基板／ＴｉＳｉＯバッファ層／チタン酸化物膜の断面図。

【図７】　本発明に係る電界効果トランジスタの断面図。

【図８】　本発明に係る電界効果トランジスタの製造工程を説明するための図であり、図８（ａ）（ｂ）（ｃ）（ｄ）は各工程における断面図。

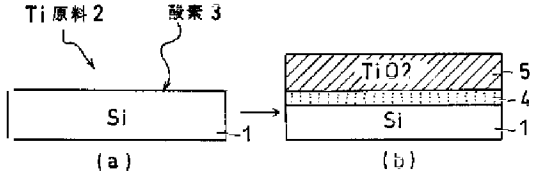
【図９】　本発明のシリコン基板／バッファ層／チタン酸化膜ゲート絶縁膜／ゲート電極における積層構造の熱処理前後の断面図であり、図９（ａ）は熱処理前、図９（ｂ）は熱処理後のもの。

【図１０】　本発明に係る電界効果トランジスタ及びシリコン酸化物をゲート絶縁膜に用いた電界効果トランジスタの電圧電流特性図。

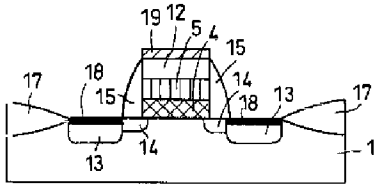
【符号の説明】

１・・・シリコン基板
２・・・チタン原料
３・・・酸素原料
４・・・SiO_2を主とする界面反応層
５・・・チタン酸化膜
６・・・チタンターゲット
７・・・アルゴン
８・・・酸素
９・・・チタン酸化物ターゲット
１０・・・バッファ層
１１・・・チタン酸化物膜
１２・・・ゲート電極
１３・・・深い拡散領域
１４・・・浅い拡散領域
１５・・・ゲート側壁
１６・・・TiO_2
１７・・・素子分離領域
１８・・・サリサイド
１９・・・サリサイド

【図１】

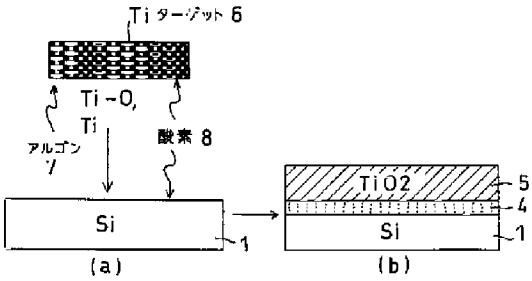


【図７】

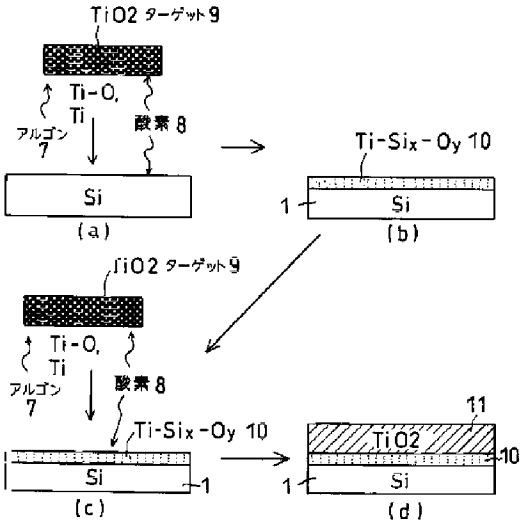


GF Exhibit 1126 - 551/2248

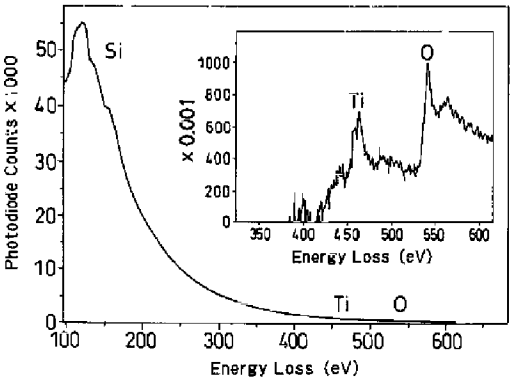
【図2】


Ti ターゲット 6
Ti-O,
Ti
アルゴン 7
酸素 8
Si
1
(a)
TiO2
5
4
Si
1
(b)

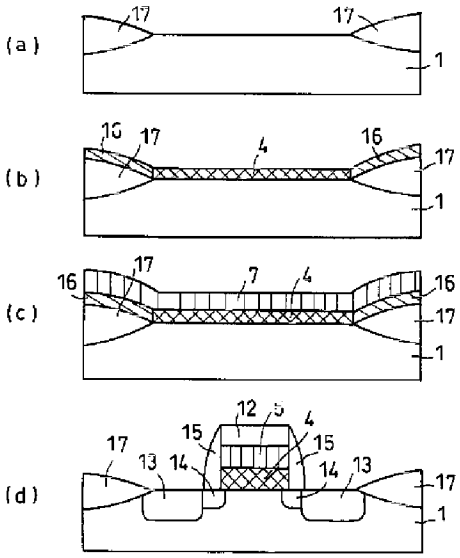
【図3】


TiO2 ターゲット 9
Ti-O,
Ti
アルゴン 7
酸素 8
Si
(a)
Ti-Six-Oy 10
Si
1
(b)
TiO2 ターゲット 9
Ti-O,
Ti
アルゴン 7
酸素 8
Ti-Six-Oy 10
Si
1
(c)
11
TiO2
10
Si
1
(d)

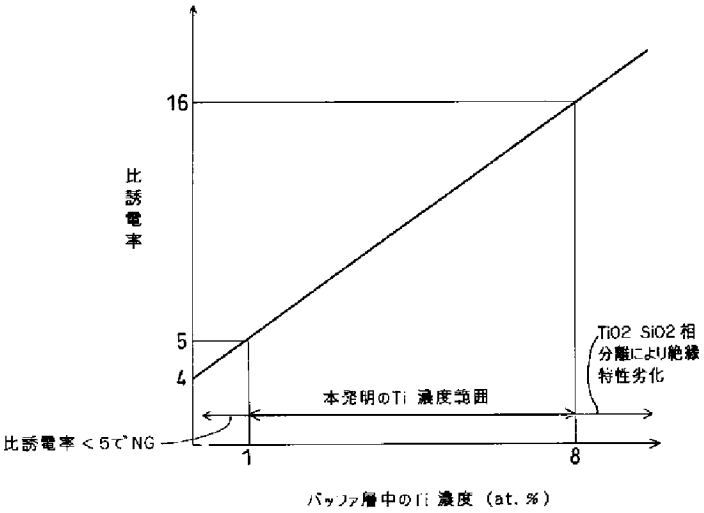
【図4】


Photodiode Counts x 1000
Si
Ti
O
x 0.001
Energy Loss (eV)
Energy Loss (eV)

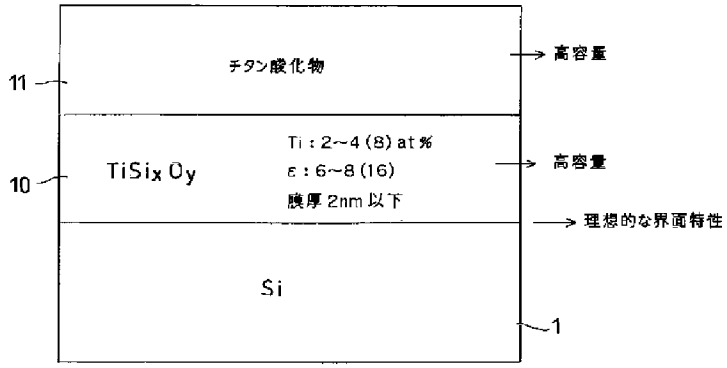
【図8】


(a)
17
17
1
(b)
16
17
4
16
17
1
(c)
16
17
7
4
16
17
1
(d)
12
5
4
15
15
17
13
14
14
13
17
1

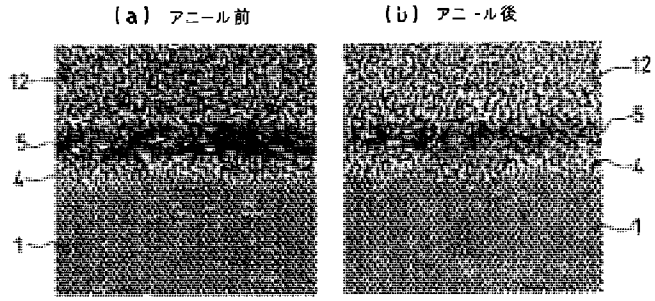
【図5】


比誘電率
16
5
4
Ti02 SiO2 相分離により絶縁特性劣化
本発明のTi 濃度範囲
比誘電率 < 5で NG
1
8
バッファ層中のTi 濃度 (at. %)

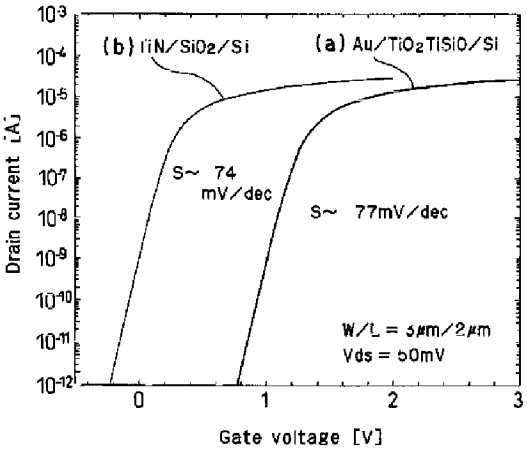
【図6】



【図9】



【図10】



フロントページの続き

Fターム(参考) 4K029 AA06 BA46 BA48 BB02 BD01
CA05 DC05 EA01 EA04
5F040 DA00 DA02 DB03 EC04 EC07
EC13 ED01 ED03 FA05 FA07
FB04 FC19
5F058 BA20 BC04 BF12 BF14 BJ01

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JP2002184978A SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Applicants: TOSHIBA CORP

Inventors: KOYAMA MASATO,NISHIYAMA AKIRA

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SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

Abstract

PROBLEM TO BE SOLVED: To prevent an insulation film capacity from decreasing to an unpractical level, resulted from an interface reaction layer having SiO2 as a main component with a thickness of 2 nm or more formed by reacting silicon and titanium oxide in a method of forming titanium oxide directly on a silicon substrate. SOLUTION: A semiconductor device comprising a silicon substrate 1, a buffer layer 4 which is formed on the silicon substrate 1 and is made of oxide containing titanium and silicon, a gate insulating film 5 which is formed on the buffer layer 4 and is made of titanium oxide, a gate electrode 12 which is formed on the gate insulating film 5, a channel region formed under the gate insulating film 5 in the silicon substrate 1, and a source region and a drain region which are separately formed in the silicon substrate 1 and has the channel region. The buffer layer 4 characteristically has a thickness of 2 nm or less, and an atomic percentage of titanium atoms is 1 to 8%.

JP2002184978A SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

The EPO does not accept responsibility for the accuracy of data originating from authorities other than the EPO, nor does it guarantee that such data is complete, up-to-date or fit for specific purposes.

[0001] BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device and a method for manufacturing the same. In particular, the present invention relates to a field effect transistor using titanium oxide as a gate insulating film and a manufacturing method thereof.

[0002] 2. Description of the Related Art In the generation of field effect transistors in which the gate length is 0.1 μm or less, the gate insulating film is required to be driven with a SiO 2 equivalent film thickness of 1.5 nm or less. When SiO2 is used for the gate insulating film as in the conventional case, the thickness is 1.5 nm or less, and there is a problem that the leakage current mainly including the tunnel current increases. This leakage current is so high that even a logic circuit that requires high speed even if power consumption is relatively high cannot be ignored, and it is a problem to prevent leakage current and reduce power consumption.

[0003] Therefore, a high dielectric material having a relative dielectric constant larger than that of SiO2 is used as the gate insulating film, and the tunnel current is prevented and the power consumption is reduced by increasing the physical gate film thickness while maintaining the driving performance. Research and development of technology is actively conducted.

[0004] There are metal oxides such as TiO 2, Ta 2 O 5, ZrO 2, HfO 2, La 2 O 3, etc. that have been studied as high dielectric materials. Among these metal oxides, TiO2 (titanium oxide) has the highest relative dielectric constant. Titanium oxide has a track record of being used in LSI as a dielectric material for capacitors such as DRAMs, and research and development using titanium oxide as a gate insulating film of a field effect transistor has been actively conducted.

[0005] However, titanium oxide is highly reactive with silicon, and in the process of depositing titanium oxide on a silicon substrate, an interface reaction layer mainly composed of SiO2 is formed at 2 nm or more at the interface between the titanium oxide film and the silicon substrate. There is a problem.

[0006] This interfacial reaction layer mainly composed of SiO2 has a dielectric constant as low as that of SiO2. Therefore, in an insulating film in which a titanium oxide film and an interfacial reaction layer are laminated, the electric capacity value thereof is almost the same as that of the interfacial reaction layer. There is a problem that it is determined by the value. Further, since the interface layer mainly composed of SiO2 is inevitably formed with a thickness of 2 nm or more, there is a problem that a required film thickness of 1.5 nm or less in terms of SiO2 cannot be achieved as a gate insulating film. .

[0007] Therefore, in order not to form the interface reaction layer, a thin film containing nitrogen such as SiON or SiN is formed in advance on a silicon substrate, and a titanium oxide film is formed on the thin film containing nitrogen. It has been. However, this method can suppress the interface reaction layer mainly composed of SiO2, but brings about a result that the interface characteristics between the gate insulating film and the silicon substrate are greatly different depending on the properties of the thin film containing nitrogen. For example, the electrical characteristics may be deteriorated by nitrogen existing near the interface between the gate insulating film and the silicon substrate. Specifically, a large number of defects, such as surplus charges represented by fixed charges caused by nitrogen atoms and interface states, are generated at the interface, thereby deteriorating device characteristics.

[0008] As described above, in the method of directly forming titanium oxide on a silicon substrate, the interface reaction layer mainly composed of SiO2 is thickened by the reaction between silicon and titanium oxide. When the thickness is 2 nm or more, there is a problem that the insulating film capacitance is lowered to a level where it cannot be used.

[0009] In addition, attempts have been made to suppress this interfacial reaction layer using a nitrogen-containing thin film as a buffer layer, but this time, the interface characteristics are significantly deteriorated by nitrogen and have not yet been put into practical use.

[0010] The present invention has been made to solve the above-mentioned problems, and realizes a high quality interfacial characteristic and realizes a high insulating film capacity having a performance of 1.5 nm or less in

terms of SiO 2 and suppresses a tunnel current. An object of the present invention is to provide a semiconductor device that satisfies both requirements.

[0011] It is another object of the present invention to provide a method of manufacturing a semiconductor device that can form such a gate insulating film on a silicon substrate.

[0012] In order to achieve the above object, the present invention provides a silicon substrate, a buffer layer formed on the silicon substrate and made of an oxide containing titanium and silicon, and on the buffer layer. A gate insulating film made of titanium oxide formed on the gate insulating film, a gate electrode formed on the gate insulating film, a channel region formed under the gate insulating film in the silicon substrate, and the silicon substrate. A source region and a drain region which are formed so as to be spaced apart from each other and the channel region is positioned between them; the buffer layer has a film thickness of 2 nm or less and an atomic concentration of titanium of 1% or more A semiconductor device characterized by being 8% or less.

[0013] An SiO 2 layer having a thickness of 1 nm or less may be formed between the buffer layer and the silicon substrate.

[0014] The buffer layer may contain some nitrogen.

[0015] In addition, the present invention provides a step of peeling an oxide film formed on the surface of a silicon substrate and sputtering on the silicon substrate by using titanium oxide as a target and sputtering under a condition where an oxygen flow rate is 0 sccm or more and 1.2 sccm or less. And a step of forming a buffer layer made of an oxide containing titanium and silicon and having a film thickness of 2 nm or less and an atomic concentration of titanium of 1% or more and 8% or less, and a titanium oxide as a target and an oxygen flow rate of 10 sccm or more. And a step of forming a gate insulating film made of titanium oxide on the buffer layer by sputtering under the above conditions. A method for manufacturing a semiconductor device is provided.

[0016] In the present invention, before the titanium oxide is formed in order to suppress the interface reaction layer mainly composed of SiO2, a buffer layer made of titanium atoms, silicon atoms and oxygen atoms is previously formed on the silicon substrate. Then, in order to maintain the interface characteristics with the silicon substrate with high quality without significantly degrading the value of the insulating film capacitance, the ratio of the constituent materials of the buffer layer and the film thickness thereof were variously studied. In the following, it has been found that the above-mentioned object can be achieved by making the constituent element of an oxide containing titanium and silicon, and further by making the atomic concentration of titanium 1% or more and 8% or less.

[0017] The buffer layer at this time may have a thickness of at least 0.5 nm. The atomic concentration represents the proportion of atoms constituting the film with respect to the total number of atoms present in the film.

[0018] DESCRIPTION OF THE PREFERRED EMBODIMENTS Preferred embodiments of the present invention will be described below in detail with reference to the drawings.

[0019] First, prior to describing the embodiments of the present invention, a titanium oxide film was directly formed on a silicon substrate in order to find out the problems of the prior art.

[0020] FIG. 1 shows a conceptual diagram when a titanium oxide film is formed on a silicon substrate by a conventional CVD (Chemical Vapor Deposition) method.

[0021] First, as shown in FIG. 1A, a silicon substrate 1 from which a natural oxide film has been removed in advance is prepared. Then, a titanium source gas 2 such as an organic metal gas containing titanium and an oxygen gas 3 are supplied onto the silicon substrate 1 surface.

[0022] Then, as shown in FIG. 1B, in this film forming method by CVD, an interface reaction layer 4 mainly composed of SiO 2 can be formed at a thickness of about 2 nm at the interface between the silicon substrate 1 and the titanium oxide film 5. .

[0023] FIG. 2 shows a conceptual diagram when a titanium oxide film is formed on a silicon substrate by a conventional sputtering method using titanium as a target.

[0024] In this method, first, as shown in FIG. 2A, a silicon substrate 1 from which a natural oxide film has been removed in advance is prepared. Then, the surface of the silicon substrate 1 is irradiated with argon 7 excited by the titanium target 6 to supply Ti—O and Ti in an oxygen atmosphere 8.

[0025] Then, as shown in FIG. 2B, even with this film formation method by sputtering, an interface reaction layer 4 mainly composed of SiO 2 can be formed to a thickness of about 2 nm at the interface between the silicon substrate 1 and the titanium oxide film 5. I understood it.

[0026] What is common to these conventional film formation methods is that the silicon surface is exposed to a large amount of oxygen at the initial stage when titanium oxide is formed on the silicon substrate 1. This means that a larger amount of oxygen than titanium is supplied to the surface of the chemically active silicon substrate 1, and the interface reaction layer 4 mainly composed of low dielectric constant SiO2 is formed to a thickness of 2 nm or more. It will cause. Conventionally, there has been a tendency to excessively supply oxygen gas during film formation in order to improve the bulk characteristics of titanium oxide. This is because titanium oxide is generally free of oxygen atoms, and the composition ratio cannot be stoichiometric unless oxygen gas is supplied excessively.

[0027] However, the interface reaction layer generated at this time has a thickness of at least 2 nm, and since SiO2 is the main component, the relative dielectric constant is as low as about 4 and the insulating film capacity is reduced.

[0028] Based on the above considerations, the inventors of the present invention first form a buffer layer made of a titanium oxide film on a silicon substrate by using a titanium oxide film as a target without reducing or supplying oxygen gas at all. Then, a gate insulating film made of titanium oxide is formed on the buffer layer by sputtering using titanium oxide as a target in an atmosphere in which oxygen gas is sufficiently supplied. By doing so, it was found that the formation of an interface reaction layer mainly composed of SiO 2 can be prevented.

[0029] FIG. 3 is a conceptual diagram illustrating a method for forming a gate insulating film made of a titanium oxide film according to the present invention.

[0030] First, as shown in FIG. 3A, a silicon substrate 1 from which a natural oxide film has been removed in advance is prepared. On the surface of the silicon substrate 1, the activated argon 7 is irradiated onto the target 9 made of titanium oxide and sputtered. By doing so, Ti—O or Ti is supplied onto the silicon substrate 1. At this time, the amount of oxygen supplied is minimized or not supplied at all. However, since the target is titanium oxide, oxygen 8 is evaporated from the titanium oxide and supplied to the surface of the silicon substrate 1.

[0031] Thus, as shown in FIG. 3B, the buffer layer 10 made of an oxide containing titanium and silicon is formed on the silicon substrate 1. This reaction is such that the formation of titanium oxide and the oxidation of the surface of the silicon substrate 1 proceed simultaneously, and the buffer layer 10 contains a mixture of titanium, silicon, and oxygen.

[0032] Next, as shown in FIG. 3C, the oxygen gas 8 is sufficiently supplied, and the titanium oxide target 9 is irradiated with the excited argon 7 to supply Ti—O and Ti onto the buffer layer 10. Since the oxygen gas 8 is sufficiently supplied in the reaction at this time, titanium atoms and oxygen atoms are close to stoichiometry and can form a titanium oxide having very excellent electrical characteristics. FIG. 3D is a view in which the gate insulating film 11 made of titanium oxide is formed on the buffer layer 10.

[0033] In this way, the process for forming the buffer layer is reduced to zero or zero, and the process for forming the gate insulating film is a two-stage process in which sufficient oxygen is supplied, so that the bulk characteristics are improved. A buffer layer made of an excellent titanium oxide and an oxide containing titanium and silicon having a high relative dielectric constant can be realized.

[0034] FIG. 4 is a diagram illustrating a composition analysis result of the buffer layer.

[0035] As shown in FIG. 4, it can be seen that the buffer layer contains titanium atoms, silicon atoms, and oxygen atoms. As described above, the buffer layer has a dielectric constant higher than that of SiO 2 by containing titanium.

[0036] Next, FIG. 5 shows a graph in which the relative dielectric constant of the buffer layer is plotted on the vertical axis and the atomic concentration of titanium in the buffer layer is plotted on the horizontal axis.

[0037] As can be seen from FIG. 5, the dielectric constant of the TiSixOy film increases as the atomic concentration of titanium in the TiSixOy film increases. However, if the content of titanium atoms becomes too high, titanium is phase-separated into TiO 2 and SiO 2, and there is a problem that the crystallization of titanium oxide and the accompanying leakage current increase. Further, there is a problem that the relative dielectric constant is lowered by the phase separation of SiO2. It has been found that the phase separation between TiO2 and SiO2 becomes apparent when the atomic concentration of titanium exceeds 8%. Therefore, in the present invention, in the buffer layer made of an oxide containing titanium and silicon, the atomic concentration of titanium is defined as 8% or less.

[0038] Further, as can be seen from FIG. 5, the relative dielectric constant decreases when the atomic concentration of titanium is too low, and the relative dielectric constant is lower than 5 when the atomic concentration of titanium is lower than 1%. For example, if the film thickness of the buffer layer is 2 nm, for example, the SiO2 equivalent film thickness is 1.6 nm, and the SiO2 equivalent film thickness that is the specification of the 0.1 μm generation cannot satisfy 1.5 nm. Therefore, in the present invention, the atomic concentration of titanium is specified to be 1% or more. At this time, the thickness of the buffer layer must be 2 nm or less. In the method of the present invention, since the buffer layer is formed by sputtering, the film thickness can be easily controlled. In the experiments by the present inventors, it is possible to make the thickness of the buffer layer 1.5 nm or less. The thickness of the buffer layer may be such that no SiO2 interface layer is generated during the next titanium oxide film formation, and may be 0.5 nm or more. However, if SiO2 is 0.1 nm or less, the SiO2 equivalent film thickness is sufficiently thin, so there is no problem even if it occurs as an interface layer.

[0039] From these considerations, the buffer layer made of TiSixOy preferably has an atomic concentration of titanium atoms of 2% or more and 4% or less. The buffer layer according to the present invention is preferably a mixture of TiO 2 and SiO 2 when viewed microscopically. In the buffer layer, silicon has an atomic concentration of 20% to 40%, more preferably 25% to 35%. The atomic concentration of oxygen is preferably 65% or more and 70% or less in order to achieve both the interface characteristics between the silicon substrate and the buffer layer and the improvement of the insulating film capacity.

[0040] Further, for example, nitrogen atoms of about 1 × 10 20 / cm 3 or less may be mixed in the buffer layer.

[0041] In the present invention, when the buffer layer is formed, suppressing the oxygen flow rate at the beginning of the titanium oxide film formation also has the effect of reducing the thickness of the buffer layer to 2 nm or less. Specifically, the buffer layer can be thinned to 1.5 nm or less by completely eliminating oxygen.

[0042] In the present invention, the amount of oxygen supplied when forming the buffer layer is set to 0 sccm or more and 2 sccm or less so that the ratio of Ti and O is sufficiently lower than that of stoichiometry (TiO 2). Here, the thickness of the buffer layer, the atomic concentration of titanium atoms, and the relative dielectric constant are greatly influenced by the oxygen supply amount. In order to increase the dielectric constant and increase the insulating film capacity of the buffer layer, it is preferable to completely remove oxygen. On the other hand, since a slight leakage current flows when the atomic concentration of titanium increases, it is preferable to flow a small amount of oxygen in order to give priority to a low leakage current.

[0043] After forming the buffer layer on the silicon substrate by the method described in detail above, it is preferable to use a method of sputtering while supplying a large amount of oxygen, which is optimal for enhancing the bulk characteristics of titanium oxide. May be formed.

[0044] FIG. 6 shows a buffer layer made of TiSixOy on a silicon substrate and a titanium oxide film formed on the buffer layer.

[0045] As shown in FIG. 6, ideal interface characteristics can be obtained if the atomic concentration of titanium in the buffer layer is 2% or more and 8% or less, preferably 4% or less and the film thickness is 2 nm or less.

[0046] FIG. 8 is a cross-sectional view of a field effect transistor in which a gate insulating film is formed using the method of the present invention described above.

[0047] As shown in FIG. 7, the field effect transistor includes a silicon substrate 1, a buffer layer 4 formed on the silicon substrate 1, a gate insulating film 5 made of polycrystalline silicon or the like formed on the buffer layer 4, And a gate electrode 12 formed on the gate insulating film.

[0048] The buffer layer 4 is made of an oxide containing titanium and silicon, and is formed so that the atomic concentration of titanium is 1% to 8% and the film thickness is 2 nm or less. The gate insulating film 5 is composed of a titanium oxide film.

[0049] Gate sidewalls 15 made of silicon oxide, silicon nitride, or the like are formed on the sidewalls of the stacked structure of the buffer layer 4 / gate insulating film 5 / gate electrode 12. A channel region is formed at a position below the gate insulating film 5 in the silicon substrate 1. A deep diffusion region 13 and a shallow diffusion region 14 in which impurities are diffused at a high concentration are formed at positions sandwiching the channel region, thereby constituting a source region / drain region. Reference numeral 17 denotes an element isolation region. Reference numeral 18 denotes a salicide formed on the deep diffusion region 13, and reference numeral 19 denotes a salicide formed on the gate electrode 12.

[0050] Next, a method for manufacturing the field effect transistor shown in FIG. 7 will be described with reference to FIG.

[0051] First, as shown in FIG. 8A, an element isolation region 17 made of silicon oxide or the like is formed at a predetermined position on the silicon substrate 1 by a normal process. Next, the natural oxide film on the silicon substrate 1 is peeled off by dilute HF solution treatment, and the silicon surface is terminated with hydrogen. This step is extremely important in order not to form an extra oxide film on the Si surface.

[0052] Next, as shown in FIG. 8B, a buffer layer 17 composed of titanium atoms, silicon atoms, and oxygen atoms is formed on the silicon substrate 1. In this step, the sputtering method described in FIGS. 3A and 3B was used.

[0053] Specifically, TiO 2 was used as a target, and the target was deposited by irradiating argon excited by RF sputtering. The gas flow conditions at this time were such that Ar gas was 20 sccm and the oxygen flow rate was different in the range from 0 sccm to 1.2 sccm. By this step, a buffer layer having a film thickness of 1.3 nm (conditions where oxygen is 0 sccm) to 1.8 nm (conditions where oxygen is 1.2 sccm) was formed. As a matter of course, TiOx (x <2) is deposited on the element isolation region 17.

[0054] Next, as shown in FIG. 8C, a titanium oxide film 7 having a high dielectric constant is deposited on the entire surface. In this step, the sputtering method described in FIGS. 3C and 3D was used.

[0055] Specifically, TiO2 was used as a target, and the target was irradiated with argon excited by RF sputtering and deposited. The gas flow rate conditions at this time were 10 sccm for Ar gas and 10 sccm for oxygen gas. This is a condition for depositing titanium oxide having a compositional ratio close to stoichiometry and excellent in electrical characteristics. At this time, the thickness of the titanium oxide 4 is preferably 1 nm or more in consideration of leakage current.

[0056] These sputtering processes were continuously performed in the same apparatus while changing only the gas flow rate conditions. By doing so, the vacuum is not broken, and the buffer layer 4 and the gate insulating film 7 can be formed in a strictly controlled gas atmosphere. This is very important in improving the characteristics of the insulating film by eliminating contamination (carbon, oxygen, nitrogen, etc.) to the insulating film.

[0057] Next, as shown in FIG. 8D, a gate electrode material such as TiN or polysilicon is deposited by a normal process and processed by etching to form the gate electrode 12. Next, the shallow diffusion region 14 is formed by ion implantation of impurities using the gate electrode 12 as a mask. Next, silicon oxide or silicon nitride is deposited on the entire surface and anisotropically etched to form gate sidewalls 5 on the side surfaces of buffer layer 4 / gate insulating film 5 / gate electrode 12. Next, the deep diffusion region 13 is formed by ion implantation of impurities using the gate electrode 12 and the gate sidewall 15 as a mask. The acceleration voltage of the impurity at this time may be higher than that of the shallow diffusion region 14. These impurity implantations are simultaneously performed in the gate electrode 12. Next, heat treatment for activating the impurity ions implanted into the shallow diffusion region 14, the deep diffusion region 13, and the gate electrode 12 is performed.

[0058] This heat treatment temperature varies slightly depending on the material used for the gate electrode 12 and typically requires a heat treatment of about 900 ° C. to 1050 ° C. FIG. 9 shows a cross-sectional view of the laminated structure of the silicon substrate 1 / TiSiO buffer layer 4 / titanium oxide gate insulating film 5 gate electrode 12 when heat-treated under these conditions. FIG. 9A shows before heat treatment, and FIG. 9B shows after heat treatment.

[0059] The titanium oxide film 5 maintains flatness, and the thickness of the Ti—Si—O buffer layer 4 hardly changes between (a) before heat treatment and (b) after heat treatment. That is, there is no problem of aggregation in the titanium oxide film 5, and the problem of capacity reduction due to regrowth of the buffer layer 4 can be almost ignored.

[0060] Thus, the laminated insulating film structure of the present invention has heat resistance that can sufficiently cope with the conventional CMOS process.

[0061] Next, by depositing Co and performing heat treatment, the above-described field effect transistor can be formed by forming the salicide 18 on the deep diffusion region 13 and the salicide 19 on the gate electrode 12 as shown in FIG.

[0062] FIG. 10 is a diagram showing the electrical characteristics of the gate voltage and the source / drain current of the field effect transistor and the field effect transistor using silicon oxide as a gate insulating film thus prepared.

[0063] The field effect transistor of the present invention has a characteristic (a) in which the S factor (the amount of change in the gate voltage with respect to a single digit change in the drain current), which is an index of the interface characteristics, uses a silicon oxide film as the gate insulating film. It can be seen that the characteristic (b) is substantially the same as that of FIG.

[0064] As described in detail above, according to the present invention, it is possible to realize high quality interfacial characteristics and to realize a high insulating film capacity having a performance of 1.5 nm or less in terms of SiO2 and to suppress tunnel current. It is possible to provide a semiconductor device that satisfies both requirements.

[0065] In addition, the present invention can provide a method for manufacturing a semiconductor device in which such a gate insulating film can be formed on a silicon substrate.

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CLAIMS JP2002184978

1.
A silicon substrate, a buffer layer made of an oxide containing titanium and silicon formed on the silicon substrate, a gate insulating film made of titanium oxide formed on the buffer layer, and formed on the gate insulating film And the channel region formed under the gate insulating film in the silicon substrate, and the channel region formed in the silicon substrate so as to be separated from each other, and the channel region is located between them. And a source region and a drain region, wherein the buffer layer has a film thickness of 2 nm or less and an atomic concentration of titanium of 1% or more and 8% or less.

2.
2. The semiconductor device according to claim 1, wherein a SiO2 layer having a film thickness of 1 nm or less is formed between the buffer layer and the silicon substrate.

3.
A step of peeling off the oxide film formed on the surface of the silicon substrate, and sputtering titanium oxide with a target of titanium oxide under the condition that the oxygen flow rate is 0 sccm or more and 1.2 sccm or less to deposit titanium and silicon on the silicon substrate. A step of forming a buffer layer made of an oxide containing a film having a film thickness of 2 nm or less and an atomic concentration of titanium of 1% or more and 8% or less; and sputtering using a titanium oxide target at an oxygen flow rate of 10 sccm or more. Accordingly, a step of forming a gate insulating film made of titanium oxide on the buffer layer is provided.

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(71)出願人　999999999
日本電気株式会社
東京都港区芝５丁目７番１号

(72)発明者　廣瀬　和之
東京都港区芝５丁目33番１号　日本電気株式会社内

(74)代理人　弁理士　岩佐　義幸

審査官　松本　邦夫

(54)【発明の名称】　ショットキー接合構造

【特許請求の範囲】

【請求項１】金属とIII－Ｖ族化合物半導体とのショットキー接合構造において、上記金属と上記半導体との間に、上記半導体と接触した時に上記半導体のフェルミレベルをピニングしない別種金属が1/10～30原子層の厚さだけ形成されていることを特徴とするショットキー接合構造。

【発明の詳細な説明】

〔産業上の利用分野〕

本発明は半導体のショットキー障壁高さが制御可能なショットキー接合構造に関するものである。

〔従来の技術〕

単一金属を半導体と接触させた時のショットキー障壁の高さは、理想的には金属の仕事関数と半導体の電子親和力との差によって与えられるとされていた〔フィジクス・オブ・セミコンダクター・デバイス(Physics of Semiconductor Devices,1969年, John Wiley R Sons,Inc.)〕。従って任意の半導体に対してショットキー障壁の高さを変化させる為には、仕事関数の異なる金属と接触させればよいはずであった。しかし、半導体の種類によっては、仕事関数の異なる金属を接触させても、フェルミレベルが一定値に固定（ピニング）され、ショットキー障壁の高さを変化させることの不可能なものもあった。

産業上の利用価値の高いIII－Ｖ族半導体はその顕著な例であった〔フィジカル・レビュー・レターズ（Phy. Rev. Lett.）第22巻, 1969年, 第1433ページ〕。

〔発明が解決しようとする問題点〕

ショットキー障壁の高さは、例えば整流特性を向上させる為には高い方が良く、接触抵抗を低減させる為には低

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い方が良い。さらにはショットキー障壁の高さは、トランジスターのしきい値電圧を決定する重要な要素である。従って前述のように利用価値の高いIII－V族化合物半導体において、ショットキー障壁の高さが制御不可能であることは、デバイス設計の上で大きなハンディとなっていた。

本発明の目的は、半導体のショットキー障壁の高さが制御可能なショットキー接合構造を提供することにある。

〔問題点を解決するための手段〕

本発明は、金属とIII－V族化合物半導体とのショットキー接合構造において、上記金属と上記半導体との間に、上記半導体と接触した時に上記半導体のフェルミレベルをピニングしない別種金属が1/10～30原子層の厚さだけ形成されていることを特徴とする。

〔作用〕

本発明者は、金属／III－V族化合物半導体界面ではフェルミレベルがピニングされるか否かは厚さ１原子層程度の金属を接触させた時に決定されること〔ジャーナル・オブ・バキューム・サイエンス・アンド・テクノロジー（J. Vac. Sci. Technol.）第17巻，1980年，第1019ページ〕、また金属の仕事関数は層厚が１層程度ではバルク状態の値に達せずに層厚が30層程度になって初めてバルク状態の値に安定すること〔ジャーナル・オブ・バキューム・サイエンス・アンド・テクノロジー（J. Vac. Sci. Technol.）第16巻，1979年，第1137ページ〕に注目した。

そして、III－V族化合物半導体と接触した時にフェルミレベルをピニングしない金属が唯一種でも存在すれば、その金属をIII－V族化合物半導体に1/10～30原子層だけ接触させ、ひき続いて任意の金属を30原子層以上接触させれば、その時形成されるショットキー接合の障壁高さは後者の金属の仕事関数によって決定されるものと考えた。

例えばＧａＡｓに対してそのフェルミレベルをピニングしない金属を探し求めたところ、Ｓｂがそのような金属であることが報告されていた〔ジャーナル・オブ・バキューム・サイエンス・アンド・テクノロジー（J. Vac. Sci. Technol.）第Ａ４巻，1986年，第958ページ〕。

そこで、第１図に示すように清浄なＣａＡｓ基板１の上にＳｂ２を１原子層形成し、それにひき続いて任意の金属３を30Å以上形成したところ、ＳｂとＧａＡｓとの間の強い化学結合が急峻で安定した界面を保証し、その結果フェルミレベルのピニングを引き起こす原因と考えられている半導体中の欠陥の発生や金属／半導体間の相互拡散が抑制され、ショットキー障壁は固定した値ではなく金属の仕事関数によって決定されることが判明した。

〔実施例〕

以下、本発明の実施例を説明する。

実施例１

金属ＳｂとＧａＡｓ半導体を用いて本発明のショットキー接合構造を形成し、ショットキー障壁高さの金属の仕事関数に対する依存性を検討したところ、ショットキー障壁高さを大きな幅で制御することができた。実験はｎ型ＧａＡｓ（１１０）基板を超高真空内でへき開し、その表面に室温でＳｂを分子線エピタキシャル成長法によって1/10原子厚だけ蒸着した。ひき続いてその上に各種金属（Ａｕ，Ｐｄ，Ａｌ，Ｔｉ）を各々500Å蒸着した。そして作製した試料に電極を取り付けた後にＣ－Ｖ測定法により評価し、ショットキー障壁高さを決定した。その結果ショットキー障壁高さは、この４種の金属においてその仕事関数の差を反映して、1500ｍｅＶも変化した。この値は従来の障壁高さの変動幅の30倍にも達した。

実施例２

金属ＳｃとＩｎＰ半導体を用いて本発明のショットキー接合構造を形成し、ショットキー障壁高さの金属の仕事関数に対する依存性を検討したところ、ショットキー障壁高さを大きな幅で制御することができた。実験はｎ型ＩｎＰ（１１０）基板を超高真空内でへき開し、その表面に室温でＳｃを分子線エピタキシャル成長法によって30原子層だけ蒸着した。ひき続いてその上に各種金属（Ａｕ，Ｐｄ，Ａｌ，Ｍｎ）を各々1000Å蒸着した。そして作製した試料に電極を取り付けた後にＣ－Ｖ測定法により評価し、ショットキー障壁高さを決定した。その結果ショットキー障壁高さは、この種の金属においてその仕事関数の差を反映して、1020ｍｅＶも変化した。この値は従来の障壁高さの変動幅の12倍にも達した。

〔発明の効果〕

以上説明したように本発明はIII－V族化合物半導体ショットキー接合において、金属をIII－V族化合物半導体表面上に形成する前に、III－V族化合物半導体との化学結合エネルギーの大きな別種金属を1/10～30原子層の厚さだけIII－V族化合物半導体上に形成することによって、ショットキー障壁高さを固定した値ではなく、金属の仕事関数によって制御可能なものとする効果がある。

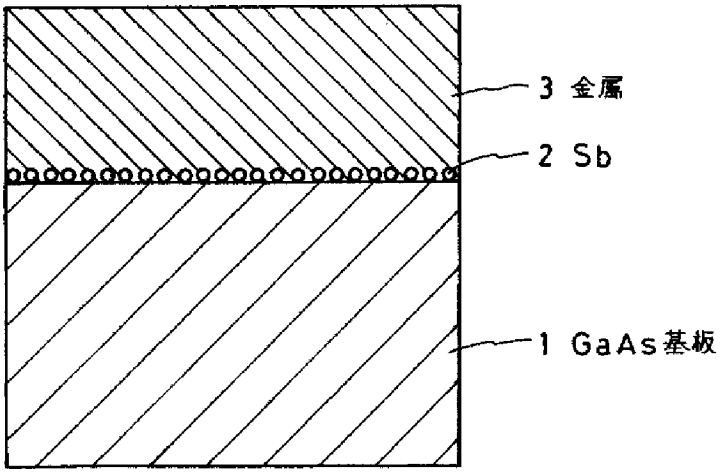
【図面の簡単な説明】

第１図は本発明によるショットキー接合構造を示す構造図である。

１…ＧａＡｓ
２…Ｓｂ
３…任意の金属

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【第１図】



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JPH065737B2 SCHOTTKY JUNCTION STRUCTURE

Applicants: NIPPON ELECTRIC CO

Inventors: HIROSE KAZUYUKI

Classifications:
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SCHOTTKY JUNCTION STRUCTURE

Abstract

PURPOSE:To make it possible to control the height of a Schottky barrier, by forming another kind of metal which has high chemical bonding energy with a semiconductor between a metal and the semiconductor by the thickness of 1/10-30 atomic layers. CONSTITUTION:Another kind of metal 2, which has high chemical bonding energy with a semiconductor 1, is formed between a metal 3 and the semiconductor 1 by the thickness of 1/10-30 atomic layers. The strong chemical bonding between the metal 2 and the semiconductor 1 insures a steep, stable interface. As a result, the occurrence of defects in the semiconductor, which are considered to cause pinning Fermi levels and mutual diffusion between the metal 3 and the semiconductor 1, are suppressed. A Schottky barrier depends on not a fixed value, but a work function of the metal. Thus the height of the Schottky barrier can be controlled.

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DESCRIPTION JPH065737

[0001]
FIELD OF THE INVENTION The present invention relates to a Schottky junction structure in which the height of a semiconductor Schottky barrier can be controlled. [Prior Art] The height of a Schottky barrier when a single metal is brought into contact with a semiconductor is ideally given by the difference between the work function of the metal and the electron affinity of the semiconductor [Physics Of Semiconductor Devices (Physics of Semiconductor Devices, 1969, John Wiley R Sons, Inc.)]. Therefore, in order to change the height of the Schottky barrier for an arbitrary semiconductor, it should have been brought into contact with metals having different work functions. However, depending on the type of semiconductor, even if metals having different work functions are brought into contact with each other, the Fermi level is fixed (pinned) to a constant value, and it is impossible to change the height of the Schottky barrier. III-V semiconductors, which have high utility value in industry, were a prominent example [Physical Review Letters (Phy. Rev. Lett.), Vol. 22, 1969, p. 1433]. [Problems to be Solved by the Invention] The height of the Schottky barrier is preferably high in order to improve the rectifying characteristics, and low in order to reduce the contact resistance. Furthermore, the height of the Schottky barrier is an important factor that determines the threshold voltage of the transistor. Therefore, as described above, the uncontrollable height of the Schottky barrier in the III-V group compound semiconductor, which has a high utility value, is a great handicap in device design. An object of the present invention is to provide a Schottky junction structure in which the height of a semiconductor Schottky barrier can be controlled. [Means for Solving the Problems] The present invention provides a Fermi of the semiconductor in the Schottky junction structure of the metal and the group III-V compound semiconductor, when the metal and the semiconductor are in contact with each other. It is characterized in that another kind of metal that does not pin the level is formed in a thickness of 1/10 to 30 atomic layers. [Function] The present inventor has determined that the Fermi level is pinned at the metal / III-V group compound semiconductor

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interface when a metal having a thickness of about one atomic layer is brought into contact [Journal of. Vacuum Science and Technology (J. Vac. Sci. Technol.) Vol. 17, 1980, p. 1019], and the work function of metal does not reach the value in the bulk state when the layer thickness is about 1 layer, and stabilizes to the value in the bulk state only when the layer thickness reaches about 30 layers. What to do [Journal of Vacuum Science and Technology (J. Vac.

Sci. Technol.) Volume 16, 1979, p. 1137]. Then, if there is only one kind of metal that does not pin the Fermi level when it comes into contact with the III-V group compound semiconductor, the metal is brought into contact with the III-V group compound semiconductor for only 1/10 to 30 atomic layers, and then continues. It was considered that the barrier height of the Schottky junction formed at that time by contacting any metal over 30 atomic layers is determined by the work function of the latter metal. For example, when searching for a metal that does not pin the Fermi level to GaAs, it was reported that Sb is such a metal [Journal of Vacuum Science and Technology (J. Vac. Sci. Technol.) Volume A4, 1986, p. 958]. Therefore, as shown in FIG. 1, one atomic layer of Sb2 was formed on a clean CaAs substrate 1, and then an arbitrary metal 3 of 30 Å or more was formed. As a result, a strong chemical bond between Sb and GaAs was formed. Guarantees a steep and stable interface, and as a result suppresses the generation of defects in the semiconductor and the metal / semiconductor interdiffusion, which are considered to be the cause of Fermi level pinning, and the Schottky barrier is fixed at a fixed value. It was found that it was determined by the work function of the metal. [Examples] Examples of the present invention will be described below. Example 1 When the Schottky junction structure of the present invention was formed using metal Sb and a GaAs semiconductor and the dependence of the Schottky barrier height on the work function of the metal was examined, the Schottky barrier height was controlled with a large width. We were able to. In the experiment, an n-type GaAs (110) substrate was cleaved in an ultrahigh vacuum, and Sb was vapor-deposited on the surface thereof at room temperature by a molecular beam epitaxial growth method by a 1/10 atomic thickness. Subsequently, various metals (Au, Pd, Al, Ti) were vapor-deposited on the respective layers to a thickness of 500 Å. Then, after the electrodes were attached to the produced sample, the evaluation was made by the CV measurement method to determine the Schottky barrier height. As a result, the Schottky barrier height changed 1500 meV, reflecting the difference in the work functions of the four metals. This value has reached 30 times the fluctuation range of the conventional barrier height. Example 2 When the Schottky junction structure of the present invention was formed using metal Sc and InP semiconductor and the dependence of the Schottky barrier height on the work function of the metal was examined, the Schottky barrier height was controlled with a large width. We were able to.

In the experiment, an n-type InP (110) substrate was cleaved in an ultrahigh vacuum, and Sc was deposited on its surface at room temperature by a molecular beam epitaxial growth method in an amount of 30 atomic layers. Subsequently, various metals (Au, Pd, Al, Mn) were vapor-deposited

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on each of the thicknesses of 1000 Å. Then, after the electrodes were attached to the produced sample, the Schottky barrier height was determined by evaluation by the CV measurement method. As a result, the Schottky barrier height also changed by 1020 meV, reflecting the difference in its work function in this kind of metal. This value reaches 12 times the fluctuation range of the conventional barrier height. As described above, in the present invention, in the III-V group compound semiconductor Schottky junction, the metal is chemically bonded to the III-V group compound semiconductor before the metal is formed on the surface of the III-V group compound semiconductor. By forming another metal having a large energy in the thickness of 1/10 to 30 atomic layers on the III-V group compound semiconductor, the Schottky barrier height can be controlled not by a fixed value but by the work function of the metal. There is an effect to do.

[0002]
Brief description of the drawings

[0003]

FIG. 1 is a structural diagram showing a Schottky junction structure according to the present invention.

1 ... GaAs2 ... Sb3 ... Arbitrary metal

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CLAIMS JPH065737

1.

In a Schottky junction structure of a metal and a III-V compound semiconductor, 1/10 to 30 atomic layers of another metal that does not pin the Fermi level of the semiconductor when contacted with the semiconductor is provided between the metal and the semiconductor. Schottky junction structure characterized by being formed only in the thickness of

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			３０１Ｄ	
21/768		21/90	Ｂ	
29/78			Ｄ	
		29/78	３０１Ｃ	

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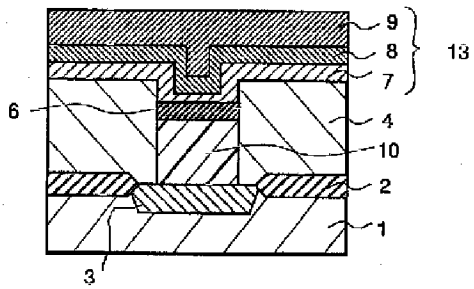
(71)出願人　000005108
株式会社日立製作所
東京都千代田区神田駿河台四丁目６番地
(72)発明者　轟原　ひろみ
茨城県土浦市神立町502番地　株式会社日立製作所機械研究所内
(72)発明者　三浦　英生
茨城県土浦市神立町502番地　株式会社日立製作所機械研究所内
(74)代理人　100075096
弁理士　作田　康夫

最終頁に続く

(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【課題】コンタクトホール内部の、シリコンとチタンシリサイド膜との接続界面に断線が生じることなく、低抵抗のコンタクトを有する半導体装置およびその製造方法を提供する。
【解決手段】電気配線用金属１３と半導体素子が形成された単結晶シリコン基板１あるいは多結晶シリコン１０が絶縁膜中に形成されたコンタクトホール５の内部あるいは底部においてチタンシリサイド膜６を介して接続されている半導体装置において、チタンシリサイド膜厚を２０ｎｍ以上７５ｎｍ以下とする。

図３



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【特許請求の範囲】
【請求項１】絶縁膜に設けたコンタクトホールの内部でシリコンと電気配線用金属とがチタンシリサイド膜を介して接続されている半導体装置において、前記チタンシリサイド膜の膜厚が２０ｎｍ以上７５ｎｍ以下であることを特徴とする半導体装置。
【請求項２】シリコン基板上の絶縁膜に設けたコンタクトホールの内部で前記シリコン基板と電気配線用金属とがチタンシリサイド膜を介して接続されている半導体装置において、前記チタンシリサイド膜の膜厚が２０ｎｍ以上７５ｎｍ以下であることを特徴とする半導体装置。
【請求項３】シリコン基板上の絶縁膜に設けたコンタクトホールの内部で前記シリコン基板と電気配線用金属とがチタンシリサイド膜を介して接続されている半導体装置において、前記シリコン基板と前記絶縁膜の界面と、前記シリコン基板とチタンシリサイドの界面との面間距離が、１８ｎｍ以上６９ｎｍ以下であることを特徴とする半導体装置。
【請求項４】シリコン基板上の絶縁膜に設けたコンタクトホールの内部で前記シリコン基板の上に堆積させた多結晶シリコンと電気配線用金属とがチタンシリサイド膜を介して接続されている半導体装置において、前記チタンシリサイド膜の膜厚が２０ｎｍ以上７５ｎｍ以下であることを特徴とする半導体装置。
【請求項５】単結晶シリコン基板と、この単結晶シリコン基板に形成されたゲート電極が多結晶シリコンであるＭＯＳトランジスタと、前記単結晶シリコン基板の前記ＭＯＳトランジスタが形成された面に形成された絶縁膜とを備え、前記絶縁膜に設けたコンタクトホールの内部で前記ゲート電極と電気配線用金属とがチタンシリサイド膜を介して接続されている半導体装置において、前記チタンシリサイド膜の膜厚が２０ｎｍ以上７５ｎｍ以下であることを特徴とする半導体装置。
【請求項６】前記電気配線用金属の前記チタンシリサイド膜と接する面がチタンであることを特徴とする請求項１乃至５のいずれか記載の半導体装置。
【請求項７】前記コンタクトホールの穴径が０．４μｍ以下であることを特徴とする請求項１乃至６のいずれか記載の半導体装置。
【請求項８】シリコン基板上に絶縁膜を設け、この絶縁膜にコンタクトホールを開き、このコンタクトホールの内部で前記シリコン基板に接するようにチタン膜を堆積させた後、前記チタン膜と前記シリコンとを熱処理して、前記チタン膜の膜厚８ｎｍ以上３０ｎｍ以下をシリサイド反応させることを特徴とする半導体装置の製造方法。
【請求項９】シリコン基板上に絶縁膜を設け、この絶縁膜にコンタクトホールを開き、このコンタクトホール内部に多結晶シリコンを埋め込み、このコンタクトホールの内部で前記多結晶シリコンに接するようにチタン膜を堆積させた後、前記チタン膜と前記シリコンとを熱処理して、前記チタン膜の膜厚８ｎｍ以上３０ｎｍ以下をシリサイド反応させることを特徴とする半導体装置の製造方法。
【請求項１０】シリコン基板上に絶縁膜を設け、この絶縁膜にコンタクトホールを開き、このコンタクトホールの内部で前記シリコン基板に接するようにチタン膜を膜厚８ｎｍ以上３０ｎｍ以下堆積させた後、前記チタン膜と前記シリコンとを熱処理して、前記チタン膜の全てをシリサイド反応させることを特徴とする半導体装置の製造方法。
【請求項１１】前記コンタクトホールの穴径が０．４μｍ以下であることを特徴とする請求項７乃至９のいずれか記載の半導体装置の製造方法。
【請求項１２】チタンシリサイド膜を形成する熱処理温度が、６５０℃以上であることを特徴とする請求項７乃至１０のいずれか記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は半導体装置およびその製造方法に関し、とくに半導体基板上に堆積された絶縁膜に形成されたコンタクトホール内部におけるシリサイドコンタクト構造に関する。
【０００２】
【従来の技術】近年、半導体装置の高集積化、微細化にともなって、高速動作のために金属配線と半導体接続部分のコンタクト抵抗の低減が望まれている。
【０００３】シリコン基板表面と金属配線とを電気的に接続するコンタクト部の抵抗を低減させる従来技術としては、例えば、特開平０７－７８８２１号公報（以下、公知例という）に、シリコン基板上と積層金属配線との間にチタンシリサイド膜を形成したものが記載されている。
【０００４】
【発明が解決しようとする課題】しかし、チタンシリサイド膜は膜厚が厚いほど、また、コンタクトホールの穴径が小さいほど剥離しやすく、半導体装置の高集積化、微細化の支障になっている。
【０００５】シリコンと金属との界面にシリサイド膜を形成することによって低いコンタクト抵抗を得るためには、形成されるチタンシリサイド（特にＴｉＳｉ２：ダイシリサイド）の膜厚がある程度必要である。しかし、チタンシリサイドは、チタン膜を堆積させたシリコンを熱処理することによって形成されるため、膜の体積変化によって膜内部に応力が発生する。
【０００６】そして、この膜内部の応力によりチタンシリサイド膜とシリコンとの界面近傍の界面に発生する応力が高くなる。この界面に発生する平均応力は、コンタクトホールの穴径が小さいほど、また、チタンシリサイド層の膜厚が厚い程高くなり、チタンシリサイド膜の剥

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離の原因になっていることを実験及び解析により解明した。

【０００７】本発明の目的は、コンタクトホールにおけるシリコンとチタンシリサイド膜との接続界面において、チタンシリサイド膜が剥離しない半導体装置を提供することにある。

【０００８】本発明の他の目的は、コンタクトホールにおけるシリコンとチタンシリサイド膜との接続界面において、チタンシリサイド膜が剥離しない半導体装置の製造方法を提供することである。

【０００９】

【課題を解決するための手段】上記の目的は、絶縁膜に設けたコンタクトホールの内部でシリコンと電気配線用金属とがチタンシリサイド膜を介して接続されている半導体装置において、前記チタンシリサイド膜の膜厚を２０～７５ｎｍとすることにより達成される。

【００１０】また、上記の他の目的は、シリコン基板上に絶縁膜を設け、この絶縁膜にコンタクトホールを開き、このコンタクトホールの内部で前記シリコン基板に接するようにチタン膜を堆積させた後、前記チタン膜と前記シリコンとを熱処理して、前記チタン膜の膜厚８～３０ｎｍをシリサイド反応させることにより達成される。

【００１１】本発明によれば、コンタクトホールにおけるシリコンとチタンシリサイド膜との接続界面において、チタンシリサイド膜が剥離しない半導体装置が提供される。また、コンタクトホールにおけるシリコンとチタンシリサイド膜との接続界面において、チタンシリサイド膜が剥離しない半導体装置の製造方法が提供される。

【００１２】ここで、チタン膜とは、チタン以外の成分を含有した金属膜も含んでいる。

【００１３】

【発明の実施の形態】以下、本発明の実施の形態について図を参照して説明する。

【００１４】まず、本発明における第１の実施形態である半導体装置のコンタクト構造断面図及びその製造方法をそれぞれ図１、７に示す。

【００１５】本実施形態の半導体装置のコンタクト構造は、図１に示すように、シリコン基板１と、このシリコン基板１表面に形成された絶縁膜４とを備え、絶縁膜に設けたコンタクトホールの内部でシリコン基板１に設けた素子形成領域３と電気配線用金属１３とがチタンシリサイド膜６を介して接続されたものである。

【００１６】この半導体装置のコンタクト構造断面は、図7に示す製造方法により製造される。すなわち、

（１）シリコン基板１上に素子分離領域２、および素子形成領域３を形成する。

【００１７】（２）素子形成領域３に素子を形成した後に、シリコン基板１上面に絶縁膜４を形成する。そして、絶縁膜４にコンタクトホール５を設ける。

【００１８】（３）絶縁膜４上面、コンタクトホール５内部の絶縁膜４側壁、およびコンタクトホール５底面の素子形成領域３上面に接するように、チタン膜７を８ｎｍ以上堆積する。

【００１９】（４）チタン膜７を８ｎｍ以上堆積したシリコン基板１を熱処理することにより、チタン膜７と素子形成領域３のシリコンとをシリサイド反応させ、界面にチタンシリサイド膜６を形成する。

【００２０】このとき、チタン膜７の膜厚８～３０ｎｍがシリサイド反応するように熱処理条件を設定する。

【００２１】なお、理由は後で述べるが、シリサイド反応をさせるためには、熱処理温度は少なくとも６５０℃以上であることが必要であり、さらに８００℃以上であることが好ましい。また、この温度は、シリコンに導入されている不純物の拡散を防止させるために１０００℃以下であることが好ましい。

【００２２】チタン膜７の膜厚の８～３０ｎｍをシリサイド反応させることによりチタンシリサイド膜６の膜厚は２０～７５ｎｍとなる。これは、理論的に、チタン膜厚１に対して、厚さ約２．３のシリコンが消費され、膜厚約２．５のチタンシリサイドが形成されるからである。

【００２３】次に図１４乃至図１７を参照して、本実施形態の半導体装置のコンタクト構造の作用効果を説明する。

【００２４】図１４シリサイド反応によるシリコン界面変化のメカニズムを示す模式図である。図１４に示すように、シリコン２１上にチタン膜２２を堆積させ、熱処理により、前記シリコン２１とチタン膜２２とを反応させ、チタンシリサイド膜６を形成した場合、理論的に、チタン膜厚１に対して、厚さ約２．３のシリコンが消費され、膜厚約２．５のチタンシリサイドが形成される。したがって、シリコン２１とチタン２２とのシリサイド反応による体積変化（体積収縮）及び密度変化により、形成されるチタンシリサイド膜とシリコン基板との界面２４の位置は、絶縁膜とシリコン基板との界面２３の位置に比べ２．３（反応に消費したチタンとの膜厚比）だけシリコン側に低くなる。

【００２５】また、このシリサイド反応による体積変化（体積収縮）及び密度変化により、チタンシリサイド膜の内部には応力が発生する。

【００２６】図１５はシリサイド反応にともなう膜内部の応力を示すグラフである。なお、応力値は実験における測定値である。

【００２７】図１５から解るように熱処理温度が５５０℃以上で膜の内部応力が急激に増加する。これは、５５０℃以上でシリサイド反応によるものであり、膜内部には最大で１０００ＭＰａの引張り応力が発生することが実験的に明らかである。

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【００２８】また、図１６は、図１５より求められた発生応力の最大値１０００ＭＰａと、コンタクト構造を考慮し、有限要素法によって、チタンシリサイドとシリコンとの界面に発生する平均応力（せん断応力）を解析した結果である。図１６から解るように、穴径が一定の場合、チタンシリサイド膜の膜厚増加に伴い界面に発生する平均応力は増加し、また、チタンシリサイド膜の膜厚が一定の場合には、コンタクトホールの小径化に伴い界面に発生する平均応力は増加する。

【００２９】ここで得られた解析結果と不良発生の実験データとの対比から、断線が発生する臨界応力は２８０ＭＰａと決定される。チタンシリサイド膜の剥離を生じさせないためには、界面に発生する平均応力を断線臨界応力値以下になるように設計することが不可欠である。すなわち、チタンシリサイドの膜厚を７５ｎｍ以下にすれば、コンタクトホールの穴径に関わらず界面に発生する平均応力を断線臨界応力値以下にすることができる。なお、コンタクトホールの孔径が０．４μｍより大きい場合は、チタンシリサイドの膜厚を７５ｎｍ以下にしなくても界面に発生する平均応力を断線臨界応力値以下することができるが、コンタクトホールの穴径が０．４μｍ以下の場合、チタンシリサイドの膜厚が７５ｎｍより厚くなると、チタンシリサイド膜が剥離する可能性がある。したがって、穴径が０．４μｍ以下のコンタクトホールにおいては、チタンシリサイド膜の剥離を防止するため、チタンシリサイド膜の膜厚を７５ｎｍ以下にする必要がある。

【００３０】図１７は、以上の結果を検証するため、穴径０．４μｍのコンタクトを試作し、断線不良率（チタンシリサイド膜の剥離）とチタンシリサイド膜の膜厚との関係を検討した結果を示している。チタンシリサイド膜厚が７５ｎｍまでは、不良が発生しないが、チタンシリサイド膜厚が７５ｎｍを超えると不良は急激に増加することが明らかである。このことからも、コンタクト内部において、チタン膜７とシリコンとのシリサイド反応によりチタンシリサイド膜６を形成する場合、シリコンとチタンシリサイド膜との界面における、チタンシリサイド膜の断線不良を防止するためには、チタンシリサイド膜厚を７５ｎｍ以下にしなければならないことが解る。

【００３１】さて、チタンシリサイド膜のコンタクト抵抗は実験によりチタンシリサイド膜の膜厚が２０ｎｍ以下で上昇することが確認されているため、チタンシリサイド膜の膜厚は２０ｎｍ以上とする必要がある。

【００３２】つまり、低コンタクト抵抗、かつ、剥離が生じることの無い、安定なコンタクトを形成するためには、チタンシリサイド膜厚が２０～７５ｎｍでなければならない。

【００３３】本実施形態では、図１に示すように、シリサイド反応に使用されなかったチタン膜７が窒化チタン膜とチタンシリサイド膜との間に存在している。

【００３４】このように、窒化チタン膜とチタンシリサイド膜との間にチタン膜７を存在させると、窒化チタン膜とチタンシリサイド膜とを直接積層するよりも、窒化チタン膜の膜内応力が低減され、窒化チタン膜の剥離強度を高めることができる。

【００３５】なお、窒化チタン膜とチタンシリサイド膜との間にチタン層７を存在させるためには、チタン層７の膜厚をシリサイド反応させる膜厚以上とし、熱処理時に熱処理温度及び熱処理時間を制御してチタンシリサイド膜の膜厚が２０～７５ｎｍとなるように制御する必要がある。

【００３６】図１に示した本実施形態の半導体装置のコンタクト構造断面図では、コンタクトホール５内部において、コンタクトホール底面の素子形成領域３と電気配線用金属膜１３との境界に、チタンシリサイド膜６が形成されている。チタンシリサイド膜６の上面には、電気配線用金属膜１３として、チタン膜７、窒化チタン膜８、タングステン膜９が積層されている。また、絶縁膜４上面にはチタン膜７、窒化チタン膜８、タングステン膜９が積層されている。

【００３７】しかし、チタン膜７は必ずしも存在する必要はなく、直接窒化チタン膜８が接していても構わない。また、窒化チタン膜８および、タングステン膜９はこれに限定されるものではなく、電気配線用金属膜１３としては、たとえば、金属チタン、窒化チタン、タングステンのほかにアルミニウム合金、モリブデンシリサイド、タングステンシリサイド、あるいはこれら複数の材料からなる積層構造からなるものがある。さらに他の導電性膜、絶縁膜であってもよい。また、異種材料の積層構造でなくともよい。

【００３８】次に、本発明における第２の実施形態である半導体装置のコンタクト構造断面図及びその製造方法をそれぞれ図２、８に示す。

【００３９】図２は本実施形態である半導体装置のコンタクト構造断面図、図８はその半導体装置の製造工程の一部を示す横断面図である。

【００４０】この半導体装置のコンタクト構造断面は図８に示す製造方法により製造される。すなわち、

（１）シリコン基板１上に素子分離領域２、および素子形成領域３を形成する。

【００４１】（２）素子形成領域３に素子を形成した後に、その上面に絶縁膜４を形成する。そして、絶縁膜４にコンタクトホール５を形成する。

【００４２】（３）絶縁膜４上面、コンタクトホール５内部の絶縁膜側壁、およびコンタクトホール５底面の素子形成領域３上面に接するように、チタン膜７を８～３０ｎｍ堆積する。

【００４３】（４）チタン膜７を８～３０ｎｍ堆積したシリコン基板１を熱処理することにより、チタン膜７と

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素子形成領域3のシリコンとをシリサイド反応させ、界面にチタンシリサイド膜6を形成する。

【0044】なお、シリサイド反応をさせるためには、熱処理温度は少なくとも650℃以上であることが必要であり、さらに800℃以上であることが好ましい。また、この温度は、シリコンに導入されている不純物の拡散を防止させるために1000℃以下であることが好ましい。

【0045】本実施形態では、図8に示すように、チタン膜7の全てがチタンシリサイド膜となっている。

【0046】このように、チタン膜7の全てをシリサイド反応させる場合は、チタンシリサイド膜の膜厚は、チタン膜7の膜厚により決定されるため、チタンシリサイド膜の膜厚制御を容易に行うことができる。

【0047】なお、この場合、窒化チタン膜とチタンシリサイド膜とが直接積層されるため、窒化チタン膜とチタンシリサイド膜との間にチタン膜7が存在する場合に較べて窒化チタン膜の膜内応力が高まる。

【0048】本発明における第3の実施形態である半導体装置のコンタクト構造断面図及びその製造方法をそれぞれ図3、9に示す。

【0049】本実施形態の半導体装置のコンタクト構造断面は図9に示す製造方法により製造される。すなわち、

(1) シリコン基板1上に素子分離領域2、および素子形成領域3を形成する。前記素子形成領域3に素子を形成した後に、その上面に絶縁膜4が形成されている。この絶縁膜は例えば酸化シリコンからなる。絶縁膜には、素子形成領域との導通を得るため、穴径が0.4μm以下のコンタクトホール5が形成される。

【0050】(2) 絶縁膜4上面、コンタクトホール5内部の絶縁膜側壁およびコンタクトホール底面の素子形成領域3上面に接するように、例えばCVD(Chemical Vapor Deposition;化学気相成長法)により多結晶シリコン膜10が堆積され、コンタクトホール5内部は前記多結晶シリコン10によって埋められる。その後、絶縁膜4上面に堆積した多結晶シリコン膜はエッチングなどによって除去される。

【0051】(3) 絶縁膜4上面、コンタクトホール5内部の絶縁膜側壁およびコンタクトホール底面の多結晶シリコン膜10上面に接するように、チタン膜7を8nm以上堆積する。

【0052】(4) その後、熱処理によってチタン膜7と多結晶シリコン膜10とのシリサイド反応により、界面にチタンシリサイド膜6が形成される。このとき反応させるチタン膜7の膜厚は8～30nmである。これによって、熱処理により形成されるチタンシリサイド膜6の膜厚は、20～75nmとなる。なお、シリサイドを形成するための熱処理温度は、少なくとも650℃以上であり、800℃以上であることが好ましい。また、この温度は、シリコンに導入されている不純物の拡散を防止させるために1000℃以下であることが好ましい。

【0053】本実施形態では、上記(2)の示したように、絶縁膜4上面およびコンタクトホール5内部の絶縁膜側壁、コンタクトホール底面の素子形成領域3上面に接するように、多結晶シリコン膜10を堆積させるという工程が必要になるが、コンタクトホール5内部が多結晶シリコン10によって埋められることにより、コンタクトホール5の深さが浅くなり、次工程である、チタン膜7の堆積が容易になる。

【0054】コンタクトホールの小径化に伴いコンタクトホールのアスペクト比(深さ/直径)は増加する傾向にあり、従来から用いられてきたスパッタリング法では、コンタクトホールの側面と底面に十分な厚さの配線用金属を被覆させることが困難になる。

【0055】しかし、段差被覆性に優れたCVD技術によってコンタクトホール内に多結晶シリコンを埋め込み、コンタクトホールの深さを浅くすることにより、容易にチタン膜をコンタクトホールの側面と底面に8nm以上堆積させることができる。

【0056】また、本実施形態では、図3に示すように、シリサイド反応に使用されなかったチタン膜7が窒化チタン膜とチタンシリサイド膜との間に存在している。

【0057】このように、窒化チタン膜とチタンシリサイド膜との間にチタン膜7が存在させる、窒化チタン膜とチタンシリサイド膜とを直接積層するよりも、窒化チタン膜の膜内応力が低減され、窒化チタン膜の剥離強度を高めることができる。

【0058】なお、窒化チタン膜とチタンシリサイド膜との間にチタン層7を存在させるためには、チタン層7の膜厚をシリサイド反応させる膜厚以上とし、熱処理時に熱処理温度及び熱処理時間を制御してチタンシリサイド膜の膜厚が20～75nmとなるように制御する必要がある。

【0059】本実施形態の半導体装置は、コンタクトホール内部において、シリコン基板1に直接堆積した多結晶シリコン10と電気配線用金属膜13との界面にチタンシリサイド膜6が形成されている。チタンシリサイド膜の上面には、電気配線用金属膜13として、チタン膜7、窒化チタン膜8、タングステン膜9が積層されている。また、前記絶縁膜4上面にはチタン膜7、窒化チタン膜8、タングステン膜9が積層されている。チタン膜7は必ずしも残留している必要はなく、絶縁膜4上に直接窒化チタン膜8が接していても構わない。また、前記窒化チタン膜8および、前記タングステン膜9はこれに限定されるものではなく、第一の実施例に示したように他の導電性膜、絶縁膜であってもよい。また、異種材料の積層構造でなくともよい。

【0060】本発明における第4の実施形態である半導

体装置のコンタクト構造断面図及びその製造方法をそれぞれ図４、１０に示す。

【００６１】本実施形態の半導体装置のコンタクト構造は、図１０に示す製造方法により製造される。すなわち、

（１）シリコン基板１上に素子分離領域２、および素子形成領域３を形成する。前記素子形成領域３に素子を形成した後に、その上面に絶縁膜４が形成されている。この絶縁膜は例えば酸化シリコンからなる。絶縁膜には、素子形成領域との導通を得るため、コンタクトホール５が形成される。

【００６２】（２）絶縁膜４上面およびコンタクトホール５内部の絶縁膜側壁、コンタクトホール底面の素子形成領域３上面に接するように、例えばＣＶＤ（Ｃｈｅｍｉｃａｌ　Ｖａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ；化学気相成長法）により多結晶シリコン膜１０が堆積され、コンタクトホール５内部は前記多結晶シリコン１０によって埋められる。その後、絶縁膜４上面に堆積した多結晶シリコン膜はエッチングなどによって除去される。

【００６３】（３）絶縁膜４上面、コンタクトホール５内部の絶縁膜側壁、およびコンタクトホール５底面の素子形成領域３上面に接するように、チタン膜７を８～３０ｎｍ堆積する。

【００６４】（４）チタン膜７を８～３０ｎｍ堆積したシリコン基板１を熱処理することにより、チタン膜７と素子形成領域３のシリコンとをシリサイド反応させ、界面にチタンシリサイド膜６を形成する。

【００６５】なお、シリサイドを形成するための熱処理温度は、少なくとも６５０℃以上であり、８００℃以上であることが好ましい。また、この温度は、シリコンに導入されている不純物の拡散を防止させるために１０００℃以下であることが好ましい。

【００６６】本実施形態では、上記（２）の示したように、絶縁膜４上面およびコンタクトホール５内部の絶縁膜側壁、コンタクトホール底面の素子形成領域３上面に接するように、多結晶シリコン膜１０を堆積させるという工程が必要になるが、コンタクトホール５内部が多結晶シリコン１０によって埋められることにより、コンタクトホール５の深さが浅くなり、次工程である、チタン膜７の堆積が容易になる。

【００６７】コンタクトホールの小径化に伴いコンタクトホールのアスペクト比（深さ／直径）は増加する傾向にあり、従来から用いられてきたスパッタリング法では、コンタクトホールの側面と底面に十分な厚さの配線用金属を被覆させることが困難になる。

【００６８】しかし、段差被覆性に優れたＣＶＤ技術によってコンタクトホール内に多結晶シリコンを埋め込み、コンタクトホールの深さを浅くすることにより、容易にチタン膜をコンタクトホールの側面と底面に８ｎｍ以上堆積させることができる。

【００６９】また、本実施形態では、図４に示すように、チタン膜７の全てがチタンシリサイド膜となっている。

【００７０】このように、チタン膜７の全てをシリサイド反応させる場合は、チタンシリサイド膜の膜厚は、チタン膜７の膜厚により決定されるため、チタンシリサイド膜の膜厚制御を容易に行うことができる。

【００７１】なお、この場合、窒化チタン膜とチタンシリサイド膜とが直接積層されるため、窒化チタン膜とチタンシリサイド膜との間にチタン膜７が存在する場合に較べて窒化チタン膜の膜内応力が高まる。

【００７２】本実施形態の半導体装置のコンタクト部は、コンタクトホール５内部において、シリコン基板１に直接堆積した多結晶シリコン１０と電気配線用金属膜１３との界面にチタンシリサイド膜６が形成されている。前記チタンシリサイド膜の上面には、電気配線用金属膜１３として、窒化チタン膜８、タングステン膜９が積層されている。また、前記絶縁膜４上面にはチタン膜７、窒化チタン膜８、タングステン膜９が積層されている。チタン膜７は必ずしも残留している必要はなく、絶縁膜４上に直接窒化チタン膜８が接していても構わない。また、前記窒化チタン膜８および、前記タングステン膜９はこれに限定されるものではなく、他の導電性膜、絶縁膜であってもよい。また、異種材料の積層構造でなくともよい。

【００７３】本発明における第５の実施形態であるＭＯＳ（Ｍｅｔａｌ　Ｏｘｉｄｅ　Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）トランジスタのゲート電極コンダクト構造断面図及びその製造方法をそれぞれ図５、１２に示す。

【００７４】本実施形態の半導体装置のコンタクト構造は図１２に示す製造方法により製造される。すなわち、（１）シリコン基板１上の素子形成領域３に約１５ｎｍの厚さのシリコン酸化膜１１を形成する。前記シリコン酸化膜１１上にＣＶＤ（Ｃｈｅｍｉｃａｌ　Ｖａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ；化学気相成長法）により多結晶シリコン膜を形成し、フォトリソグラフィー法でレジストパターンを形成し、それをマスクにしてドライエッチング法により多結晶シリコン膜とシリコン酸化膜をパターン化して多結晶シリコンゲート電極１２を形成する。

【００７５】（２）シリコン基板１上面およびゲート電極１２上面一面に絶縁膜４を堆積し、ゲート電極１２との導通をとるためにゲート電極に達するようにコンタクトホール５が開孔される。

【００７６】（３）前記絶縁膜４上面、および、前記コンタクトホール５内部においてゲート電極１２と接するようにチタン膜７が堆積される。

【００７７】（４）その後、熱処理によってチタン膜７とゲート電極１２のシリコンとのシリサイド反応により、界面にチタンシリサイド膜６が形成される。このと

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き反応させるチタン膜7の膜厚は8～30nmである。なお、シリサイドを形成するための熱処理温度は、少なくとも650℃以上であり、800℃以上であることが好ましい。また、この温度は、シリコンに導入されている不純物の拡散を防止させるために1000℃以下であることが好ましい。

【0078】本実施形態では、図5に示すように、シリサイド反応に使用されなかったチタン膜7が窒化チタン膜とチタンシリサイド膜との間に存在している。

【0079】このように、窒化チタン膜とチタンシリサイド膜との間にチタン膜7を存在させると、窒化チタン膜とチタンシリサイド膜とを直接積層するよりも、窒化チタン膜の膜内応力が低減され、窒化チタン膜の剥離強度を高めることができる。

【0080】なお、窒化チタン膜とチタンシリサイド膜との間にチタン層7を存在させるためには、チタン層7の膜厚をシリサイド反応させる膜厚以上とし、熱処理時に熱処理温度及び熱処理時間を制御してチタンシリサイド膜の膜厚が20～75nmとなるように制御する必要がある。

【0081】本実施形態の半導体装置のコンタクト部は、コンタクトホール5内部において、電気配線用金属膜13と多結晶シリコンからなるゲート電極12との界面にチタンシリサイド膜6が形成されている。図5および図12では、チタンシリサイド膜6の上面に電気配線用金属膜13として未反応のチタン膜7、窒化チタン8が積層されている場合を示した。しかし、ゲート電極12上面に8～30nmのチタン膜7を堆積し、前記チタン膜すべてを消費するようにチタンシリサイド膜6を形成し、チタンシリサイド膜6上面にチタン膜7が残留していなくてもよい。また、絶縁膜4上に直接窒化チタン膜8が接していても構わない。前記窒化チタン膜8はこれに限定されるものではなく、他の導電性膜、絶縁膜であってもよい。また、異種材料の積層構造でなくともよい。

【0082】本発明における第6の実施形態であるMOSトランジスタのゲート電極コンタクト構造断面図及びその製造方法をそれぞれ図6、13に示す。

【0083】本実施形態の半導体装置のコンタクト構造は、図13に示す製造方法により製造される。すなわち、

(1) シリコン基板1上の素子形成領域3に約15nmの厚さのシリコン酸化膜11を形成する。前記シリコン酸化膜11上にCVD(Chemical Vapor Deposition;化学気相成長法)により多結晶シリコン膜を形成し、フォトリソグラフィー法でレジストパターンを形成し、それをマスクにしてドライエッチング法により多結晶シリコン膜とシリコン酸化膜をパターン化して多結晶シリコンゲート電極12を形成する。

【0084】(2) シリコン基板1上面およびゲート電極12上面一面に絶縁膜4を堆積し、ゲート電極12との導通をとるためにゲート電極に達するようにコンタクトホール5が開孔される。絶縁膜4上面およびコンタクトホール5内部の絶縁膜側壁、コンタクトホール底面のゲート電極12上面に接するように、例えばCVDにより多結晶シリコン膜10が堆積され、コンタクトホール5内部は前記多結晶シリコン10によって埋められる。その後、絶縁膜4上面に堆積した多結晶シリコン膜はエッチングなどによって除去される。

【0085】(3) 前記絶縁膜4上面、および、多結晶シリコン膜10上面一面にチタン膜7が堆積される。

【0086】(4) その後、熱処理によってチタン膜7と多結晶シリコン10とのシリサイド反応により、界面にチタンシリサイド膜6が形成される。このとき反応させるチタン膜7の膜厚は8～30nmである。なお、シリサイドを形成するための熱処理温度は、少なくとも650℃以上であり、800℃以上であることが好ましい。また、この温度は、シリコンに導入されている不純物の拡散を防止させるために1000℃以下であることが好ましい。

【0087】本実施形態では、上記(2)の示したように、絶縁膜4上面およびコンタクトホール5内部の絶縁膜側壁、コンタクトホール底面の素子形成領域3上面に接するように、多結晶シリコン膜10を堆積させるという工程が必要になるが、コンタクトホール5内部が多結晶シリコン10によって埋められることにより、コンタクトホール5の深さが浅くなり、次工程である、チタン膜7の堆積が容易になる。

【0088】コンタクトホールの小径化に伴いコンタクトホールのアスペクト比(深さ/直径)は増加する傾向にあり、従来から用いられてきたスパッタリング法では、コンタクトホールの側面と底面に十分な厚さの配線用金属を被覆させることが困難になる。

【0089】しかし、段差被覆性に優れたCVD技術によってコンタクトホール内に多結晶シリコンを埋め込み、コンタクトホールの深さを浅くすることにより、容易にチタン膜をコンタクトホールの側面と底面に8nm以上堆積させることができる。

【0090】また、本実施形態では、図3に示すように、シリサイド反応に使用されなかったチタン膜7が窒化チタン膜とチタンシリサイド膜との間に存在している。

【0091】このように、窒化チタン膜とチタンシリサイド膜との間にチタン膜7が存在する場合、窒化チタン膜とチタンシリサイド膜とを直接積層するよりも、窒化チタン膜の膜内応力が低減され、窒化チタン膜の剥離強度を高めることができる。

【0092】なお、窒化チタン膜とチタンシリサイド膜との間にチタン層7を存在させるためには、チタン層7

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の膜厚をシリサイド反応させる膜厚以上とし、熱処理時に熱処理温度及び熱処理時間を制御してチタンシリサイド膜の膜厚が２０～７５ｎｍとなるように制御する必要がある。

【００９３】本実施形態の半導体装置のコンタクト部は、コンタクトホール５内部において、ゲート電極１２に接するように埋め込まれた多結晶シリコン１０と電気配線用金属膜１３との界面にチタンシリサイド膜６が形成されている。図６および図１３では、チタンシリサイド膜６の上面に電気配線用金属膜１３として、未反応のチタン膜７、窒化チタン膜８が積層している場合を示した。しかし、ゲート電極１２上面に８～３０ｎｍのチタン膜７を堆積し、前記チタン膜すべてを消費するようにチタンシリサイド膜６を形成し、チタンシリサイド膜６上面にチタン膜７が残留していなくてもよい。また、絶縁膜４上に直接窒化チタン膜８が接していても構わない。前記窒化チタン膜８はこれに限定されるものではなく、第一の実施例に示したように、他の導電性膜、絶縁膜であってもよい。また、異種材料の積層構造でなくともよい。前記チタンシリサイド膜６の膜厚は、２０～７５ｎｍである。

【００９４】以上の全ての実施形態における製造工程において、チタンシリサイド膜の形成は、単結晶シリコン基板１あるいは多結晶シリコン１０に接するようにチタン膜７を堆積する工程の後、熱処理によりチタンシリサイド膜６を形成する工程がある場合について説明した。しかし、各実施形態において説明した製造工程はこれに限定されるものではなく、図１１に示すような製造工程であってもよい。すなわち、

（１）シリコン基板１上に素子分離領域２、および素子形成領域３を形成する。

【００９５】（２）前記素子形成領域３に素子を形成した後に、その上面に絶縁膜４が形成されている。この絶縁膜は例えば酸化シリコンからなる。絶縁膜には、素子形成領域との導通を得るため、コンタクトホール５が形成される。

【００９６】（３）絶縁膜４上面およびコンタクトホール５内部の絶縁膜側壁、コンタクトホール底面の素子形成領域３上面に接するように、チタン膜７が堆積される。さらに前記チタン膜７の上面に窒化チタン膜８、タングステン膜９を積層させる。前記窒化チタン膜８および、前記タングステン膜９はこれに限定されるものではなく、他の導電性膜、絶縁膜であってもよい。

【００９７】（４）その後、熱処理によってチタン膜７と素子形成領域３のシリコンとのシリサイド反応により、界面にチタンシリサイド膜６が形成される。このとき反応させるチタン膜７の膜厚は８～３０ｎｍである。これによって、熱処理により形成されるチタンシリサイド膜６の膜厚は、２０～７５ｎｍとなる。なお、シリサイドを形成するための熱処理温度は、少なくとも６５０℃以上であり、８００℃以上であることが好ましい。また、この温度は、シリコンに導入されている不純物の拡散を防止させるために１０００℃以下であることが好ましい。

【００９８】形成するチタンシリサイド膜６の膜厚を２０～７５ｎｍとすることにより、シリコンとチタンとの接触抵抗値が低減でき、かつ、シリコンとチタンシリサイド膜との界面に発生する界面に発生する平均応力を断線発生臨界応力値以下にすることができ、チタンシリサイド膜の剥離が生じない良好なコンタクトとなる。

【００９９】図１１では、チタンシリサイド膜６の上面に電気配線用金属膜１３として、未反応のチタン膜７、窒化チタン膜８、タングステン膜９が積層している場合を示した。しかし、シリコン基板１上の素子形成領域３に接するように８～３０ｎｍのチタン膜７を堆積し、前記チタン膜すべてを消費するようにチタンシリサイド膜６を形成し、チタンシリサイド膜６上面にチタン膜７が残留していなくてもよい。また、絶縁膜４上に直接窒化チタン膜８が接していても構わない。前記窒化チタン膜８、タングステン膜９はこれに限定されるものではなく、他の導電性膜、絶縁膜であってもよい。また、異種材料の積層構造でなくともよい。前記チタンシリサイド膜６の膜厚は、２０～７５ｎｍである。

【０１００】

【発明の効果】本発明によれば、絶縁膜に設けたコンタクトホールの内部でシリコンと電気配線用金属とがチタンシリサイド膜を介して接続されている半導体装置において、前記チタンシリサイド膜の膜厚が２０ｎｍ以上７５ｎｍ以下とすることにより、シリコンと金属配線との接触抵抗を低減でき、シリコンとチタンシリサイドとの界面において断線の生じる心配のない、良好なコンタクトを形成することができる。

【図面の簡単な説明】

【図１】本発明における第１の実施形態である半導体装置のコンタクト構造を示す断面図である。

【図２】本発明における第２の実施形態である半導体装置のコンタクト構造を示す断面図である。

【図３】本発明における第３の実施形態である半導体装置のコンタクト構造を示す断面図である。

【図４】本発明における第４の実施形態である半導体装置のコンタクト構造を示す断面図である。

【図５】本発明における第５の実施形態であるＭＯＳトランジスタのゲート電極コンタクト構造を示す断面図である。

【図６】本発明における第６の実施例であるＭＯＳトランジスタのゲート電極コンタクト構造を示す断面図である。

【図７】本発明における第１の実施形態である半導体装置の製造工程の一部を示す断面図である。

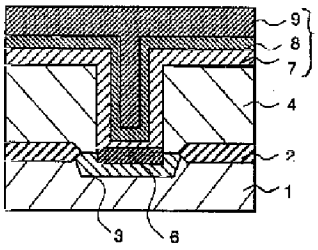
【図８】本発明における第２の実施形態である半導体装

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置の製造工程の一部を示す断面図である。
【図９】本発明における第３の実施形態である半導体装置の製造工程の一部を示す断面図である。
【図１０】本発明における第４の実施形態である半導体装置の製造工程の一部を示す断面図である。
【図１１】本発明における第５の実施形態である半導体装置の製造工程の一部を示す断面図である。
【図１２】本発明における第６の実施形態であるＭＯＳトランジスタの製造工程の一部を示す断面図である。
【図１３】本発明における第７の実施形態であるＭＯＳトランジスタの製造工程の一部を示す断面図である。
【図１４】シリサイド反応によるシリコン界面変化のメカニズムを示す模式図である。
【図１５】シリサイド反応にともなう膜内部の応力を示すグラフである。
【図１６】シリコン膜とチタンシリサイド膜の界面に発生する平均応力とチタン膜厚およびコンタクトホール穴径との関係を示すグラフである。
【図１７】コンタクトホール穴径０．４μｍの場合における、断線不良率（チタンシリサイド膜剥離）とチタンシリサイド膜厚の関係を示すグラフである。
【符号の説明】
１…シリコン基板、２…素子分離領域、３…素子形成領域、４…絶縁膜、５…コンタクトホール、６…チタンシリサイド膜、７…チタン膜、８…窒化チタン膜、９…タングステン膜、１０…多結晶シリコン、１１…シリコン酸化膜、１２…ゲート電極、１３…電気配線用金属膜、２１…シリコン、２２…チタン膜、２３…初期のシリコン／チタン界面、２４…チタンシリサイド／シリコン界面。

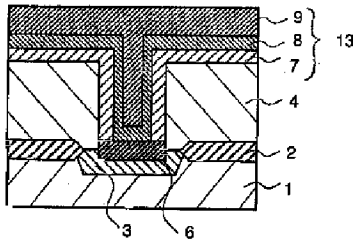
【図１】

図1



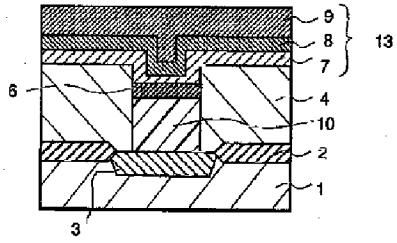
【図２】

図2



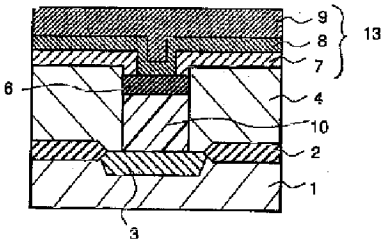
【図３】

図3



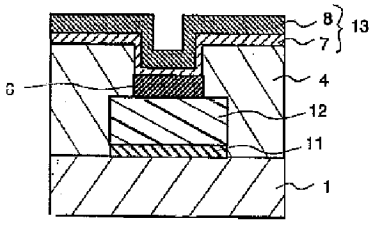
【図４】

図4



【図５】

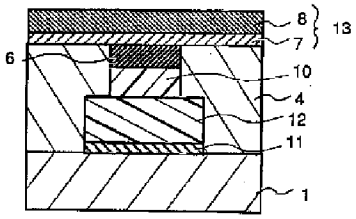
図5



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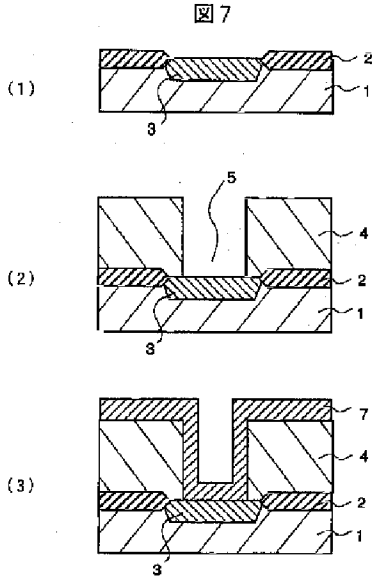
【図6】

図6



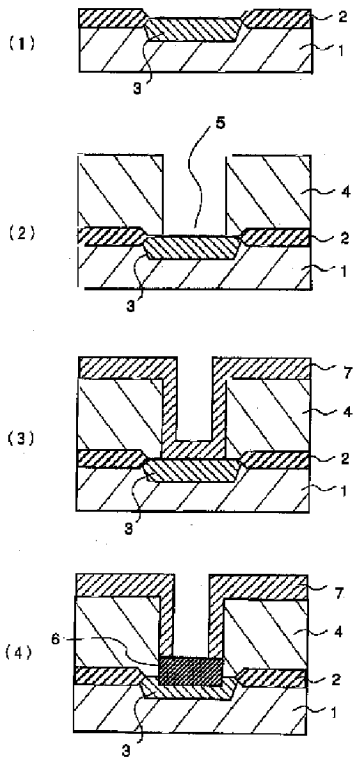
【図7】

図7



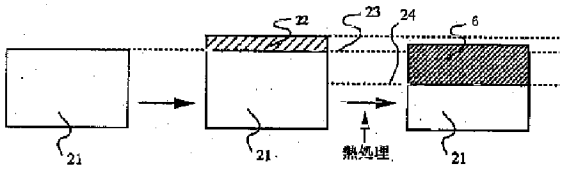
【図8】

図8



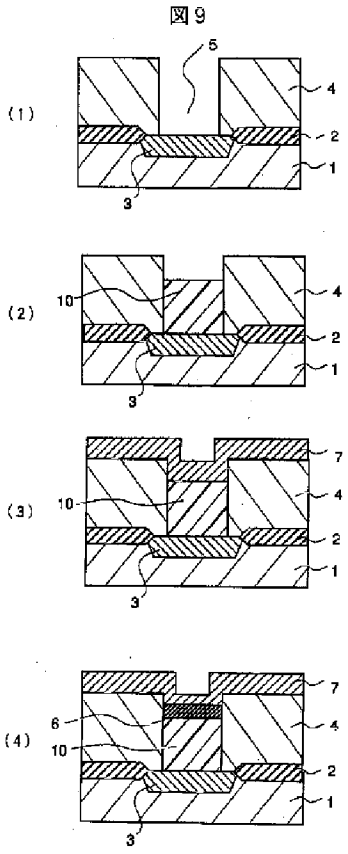
【図14】

図14



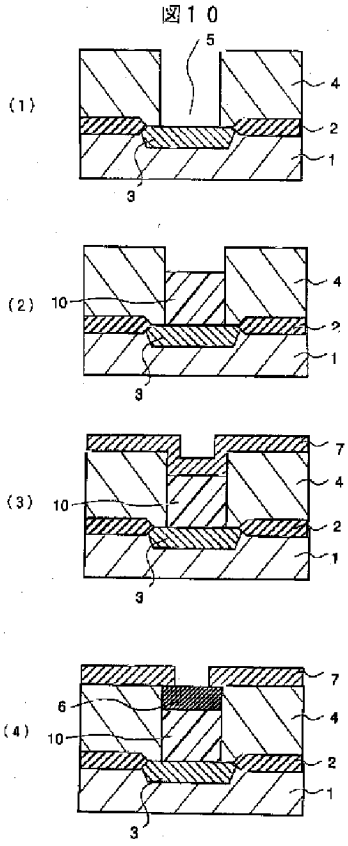
【図9】

図9



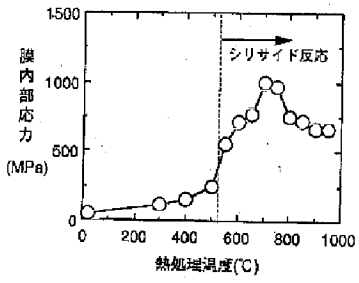
【図10】

図10



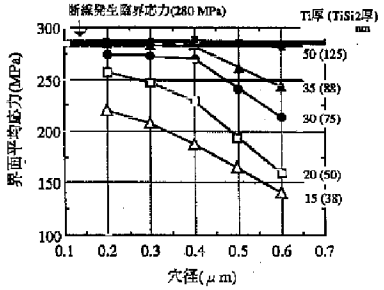
【図15】

図15



【図16】

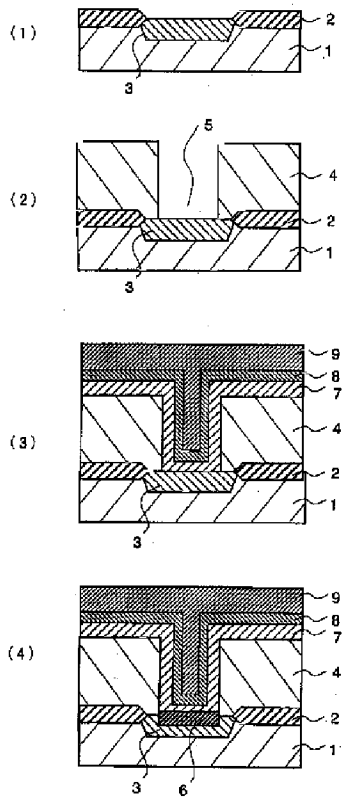
図16



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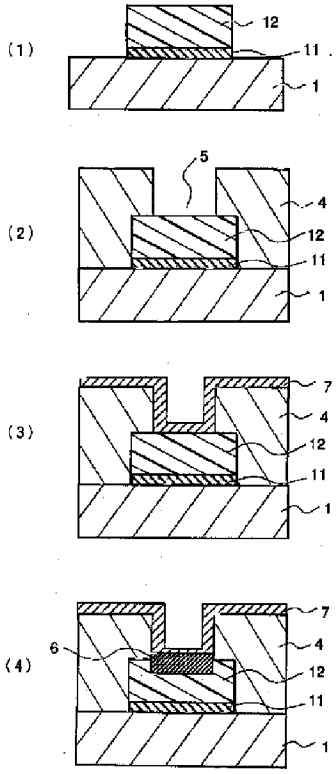
【図11】

図11



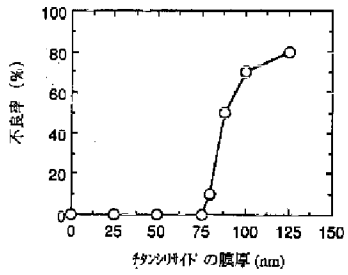
【図12】

図12



【図17】

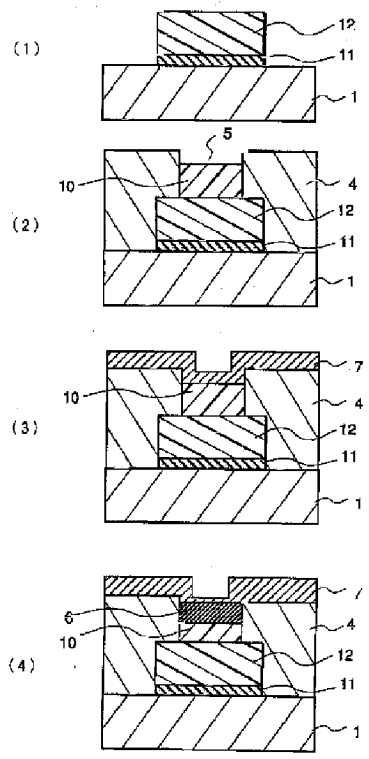
図17



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【図13】

図13



フロントページの続き

(72)発明者　鈴樹　正恭
東京都小平市上水本町五丁目20番1号　株式会社日立製作所半導体事業部内

(72)発明者　西原　晋治
東京都小平市上水本町五丁目20番1号　株式会社日立製作所半導体事業部内

(72)発明者　池田　修二
東京都小平市上水本町五丁目20番1号　株式会社日立製作所半導体事業部内

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JP2001223180A SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Applicants: HITACHI LTD

Inventors: GOHARA HIROMI,IKEDA SHUJI,MIURA HIDEO,NISHIHARA SHINJI,SUZUKI MASAYASU

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SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Abstract

PROBLEM TO BE SOLVED: To provide a semiconductor device wherein contact of low resistance is obtained without generating disconnection on a connection interface between silicon and a titanium silicide film in a contact hole, and a manufacturing method of the device. SOLUTION: A semiconductor device is connected via the titanium silicide film 6 at the inside or a bottom part of the contact hole 5 wherein a single crystal silicon substrate 1 on which metal 13 for electric wiring and a semiconductor element are formed or polycrystalline silicon 10 is formed in an insulating film. In this semiconductor device, thickness of the titanium silicide film is set at least 20 nm and at most 75 nm.

JP2001223180A SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

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The wording below is an initial machine translation of the original publication. To apply more advanced translation technology, use Patent Translate.

[0001] BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device and a method of manufacturing the same, and more particularly to a silicide contact structure inside a contact hole formed in an insulating film deposited on a semiconductor substrate.

[0002] 2. Description of the Related Art In recent years, with the high integration and miniaturization of semiconductor devices, it is desired to reduce the contact resistance between a metal wiring and a semiconductor connection portion for high-speed operation.

[0003] As a conventional technique for reducing the resistance of a contact portion that electrically connects the surface of a silicon substrate and a metal wiring, for example, Japanese Patent Laid-Open No. 07-78821 (hereinafter referred to as a known example) discloses a method for forming a silicon substrate and a laminated metal wiring. And a titanium silicide film formed between the two.

[0004] However, as the thickness of the titanium silicide film increases and the hole diameter of the contact hole decreases, the titanium silicide film is more easily peeled off, which hinders high integration and miniaturization of semiconductor devices. .

[0005] In order to obtain a low contact resistance by forming a silicide film at the interface between silicon and metal, a film thickness of titanium silicide (particularly TiSi2: disilicide) to be formed is required to some extent. However, since titanium silicide is formed by heat-treating silicon on which a titanium film is deposited, stress is generated inside the film due to the volume change of the film.

[0006] The stress generated at the interface near the interface between the titanium silicide film and silicon is increased by the stress inside the film. The average stress generated at this interface increases as the hole diameter of the contact hole decreases and the thickness of the titanium silicide layer increases, and it has been elucidated by experiments and analyzes that it causes peeling of the titanium silicide film. did.

[0007] An object of the present invention is to provide a semiconductor device in which a titanium silicide film does not peel off at a connection interface between silicon and a titanium silicide film in a contact hole.

[0008] Another object of the present invention is to provide a method of manufacturing a semiconductor device in which a titanium silicide film does not peel off at a connection interface between silicon and a titanium silicide film in a contact hole.

[0009] The object of the present invention is to provide a semiconductor device in which silicon and an electric wiring metal are connected via a titanium silicide film inside a contact hole provided in the insulating film. This is achieved by setting the film thickness to 20 to 75 nm.

[0010] Another object of the present invention is to provide an insulating film on a silicon substrate, open a contact hole in the insulating film, deposit a titanium film in contact with the silicon substrate inside the contact hole, and then form the titanium film. This is achieved by heat-treating the film and the silicon to cause a silicide reaction of the titanium film with a thickness of 8 to 30 nm.

[0011] According to the present invention, a semiconductor device is provided in which the titanium silicide film does not peel off at the connection interface between silicon and the titanium silicide film in the contact hole. In addition, a method for manufacturing a semiconductor device is provided in which the titanium silicide film does not peel off at the connection interface between silicon and the titanium silicide film in the contact hole.

[0012] Here, the titanium film includes a metal film containing a component other than titanium.

[0013] DESCRIPTION OF THE PREFERRED EMBODIMENTS Embodiments of the present invention will be described below with reference to the drawings.

[0014] First, a cross-sectional view of a contact structure of a semiconductor device according to a first embodiment of the present invention and a manufacturing method thereof are shown in FIGS.

[0015] As shown in FIG. 1, the contact structure of the semiconductor device of the present embodiment includes a silicon substrate 1 and an insulating film 4 formed on the surface of the silicon substrate 1, and silicon is formed inside a contact hole provided in the insulating film. The element forming region 3 provided on the substrate 1 and the electric wiring metal 13 are connected via the titanium silicide film 6.

[0016] The cross section of the contact structure of this semiconductor device is manufactured by the manufacturing method shown in FIG. (1) An element isolation region 2 and an element formation region 3 are formed on a silicon substrate 1.

[0017] (2) After the elements are formed in the element formation region 3, the insulating film 4 is formed on the upper surface of the silicon substrate 1. Then, a contact hole 5 is provided in the insulating film 4.

[0018] (3) The titanium film 7 is deposited to a thickness of 8 nm or more so as to be in contact with the upper surface of the insulating film 4, the side wall of the insulating film 4 inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole 5.

[0019] (4) By heat-treating the silicon substrate 1 on which the titanium film 7 is deposited with a thickness of 8 nm or more, the titanium film 7 and the silicon in the element forming region 3 are silicided to form the titanium silicide film 6 at the interface.

[0020] At this time, the heat treatment conditions are set so that the titanium film 7 has a thickness of 8 to 30 nm and undergoes a silicide reaction.

[0021] Although the reason will be described later, in order to cause the silicide reaction, the heat treatment temperature needs to be at least 650 ° C. or higher, and more preferably 800 ° C. or higher. Further, this temperature is preferably 1000 ° C. or lower in order to prevent diffusion of impurities introduced into silicon.

[0022] When the titanium film 7 having a thickness of 8 to 30 nm is subjected to a silicide reaction, the titanium silicide film 6 has a thickness of 20 to 75 nm. This is because, theoretically, silicon with a thickness of about 2.3 is consumed for titanium film thickness 1, and titanium silicide with a film thickness of about 2.5 is formed.

[0023] Next, operations and effects of the contact structure of the semiconductor device of this embodiment will be described with reference to FIGS.

[0024] 14 is a schematic diagram showing the mechanism of the silicon interface change due to the silicide reaction. As shown in FIG. 14, when the titanium film 22 is deposited on the silicon 21 and the silicon 21 and the titanium film 22 are reacted by heat treatment to form the titanium silicide film 6, theoretically, the titanium film thickness 1 On the other hand, silicon with a thickness of about 2.3 is consumed, and titanium silicide with a thickness of about 2.5 is formed. Therefore, the position of the interface 24 between the formed titanium silicide film and the silicon substrate due to the volume change (volume shrinkage) and density change due to the silicide reaction between the silicon 21 and the titanium 22 is the position of the interface 23 between the insulating film and the silicon substrate. Compared to the position, the distance is lowered to the silicon side by 2.3 (ratio of film thickness with titanium consumed for reaction).

[0025] Further, stress is generated inside the titanium silicide film due to volume change (volume shrinkage) and density change due to the silicide reaction.

[0026] FIG. 15 is a graph showing the stress inside the film due to the silicide reaction. The stress value is a measured value in the experiment.

[0027] As can be seen from FIG. 15, when the heat treatment temperature is 550 ° C. or higher, the internal stress of the film rapidly increases. This is due to the silicidation above 550 ° C., and it is experimentally clear that a maximum tensile stress of 1000 MPa is generated inside the film.

[0028] Further, FIG. 16 analyzed the average stress (shear stress) generated at the interface between titanium silicide and silicon by the finite element method in consideration of the maximum value of 1000 MPa of the generated stress obtained from FIG. 15 and the contact structure. It is a result. As can be seen from FIG. 16, when the hole diameter is constant, the average stress generated at the interface increases as the thickness of the titanium silicide film increases, and when the thickness of the titanium silicide film is constant, the contact hole As the diameter decreases, the average stress generated at the interface increases.

[0029] From the comparison between the analysis result obtained here and the experimental data indicating the occurrence of defects, the critical stress at which disconnection occurs is determined to be 280 MPa. In order not to cause peeling of the titanium silicide film, it is essential to design the average stress generated at the interface to be equal to or lower than the disconnection critical stress value. That is, if the thickness of the titanium silicide is 75 nm or less, the average stress generated at the interface can be made equal to or less than the disconnection critical stress value regardless of the hole diameter of the contact hole. In addition, when the hole diameter of the contact hole is larger than 0.4 μm, the average stress generated at the interface can be made not more than the disconnection critical stress value even if the film thickness of titanium silicide is not made 75 nm or less. Is 0.4 μm or less, the titanium silicide film may be peeled off when the thickness of the titanium silicide is more than 75 nm. Therefore, in a contact hole having a hole diameter of 0.4 μm or less, the thickness of the titanium silicide film needs to be 75 nm or less in order to prevent peeling of the titanium silicide film.

[0030] FIG. 17 shows the result of examining the relationship between the disconnection failure rate (peeling of the titanium silicide film) and the film thickness of the titanium silicide film, in order to verify the above results, by fabricating a contact with a hole diameter of 0.4 μm. Yes. It is apparent that defects do not occur until the titanium silicide film thickness is 75 nm, but the defects rapidly increase when the titanium silicide film thickness exceeds 75 nm. For this reason, when the titanium silicide film 6 is formed in the contact by the silicide reaction between the titanium film 7 and silicon, in order to prevent the disconnection defect of the titanium silicide film at the interface between the silicon and the titanium silicide film. It can be seen that the titanium silicide film thickness must be 75 nm or less.

[0031] Since the contact resistance of the titanium silicide film has been confirmed by experiment to increase when the thickness of the titanium silicide film is 20 nm or less, the thickness of the titanium silicide film needs to be 20 nm or more.

[0032] That is, in order to form a stable contact with low contact resistance and no peeling, the titanium silicide film thickness must be 20 to 75 nm.

[0033] In the present embodiment, as shown in FIG. 1, the titanium film 7 that has not been used for the silicide reaction exists between the titanium nitride film and the titanium silicide film.

[0034] As described above, when the titanium film 7 exists between the titanium nitride film and the titanium silicide film, the in-film stress of the titanium nitride film is reduced and the nitridation is performed as compared with the case where the titanium nitride film and the titanium silicide film are directly laminated. The peel strength of the titanium film can be increased.

[0035] In order for the titanium layer 7 to be present between the titanium nitride film and the titanium silicide film, the thickness of the titanium layer 7 is set to be equal to or larger than the thickness of the silicide reaction, and the heat treatment temperature and the heat treatment time are controlled during the heat treatment. It is necessary to control the thickness of the silicide film to be 20 to 75 nm.

[0036] In the cross-sectional view of the contact structure of the semiconductor device according to the present embodiment shown in FIG. 1, a titanium silicide film 6 is formed in the contact hole 5 at the boundary between the element formation region 3 on the bottom surface of the contact hole and the metal film 13 for electric wiring. Has been. On the upper surface of the titanium silicide film 6, a titanium film 7, a titanium nitride film 8, and a tungsten film 9 are laminated as a metal film 13 for electrical wiring. A titanium film 7, a titanium nitride film 8, and a tungsten film 9 are stacked on the upper surface of the insulating film 4.

[0037] However, the titanium film 7 is not necessarily present, and the titanium nitride film 8 may be in direct contact. Further, the titanium nitride film 8 and the tungsten film 9 are not limited to this, and examples of the metal film 13 for electric wiring include an aluminum alloy, molybdenum silicide, tungsten silicide in addition to metal titanium, titanium nitride, and tungsten. Alternatively, there is a layered structure composed of a

plurality of these materials. Furthermore, other conductive films and insulating films may be used. Further, the laminated structure of different materials is not necessary.

[0038] Next, a cross-sectional view of a contact structure of a semiconductor device according to the second embodiment of the present invention and a manufacturing method thereof are shown in FIGS.

[0039] FIG. 2 is a cross-sectional view of the contact structure of the semiconductor device according to the present embodiment, and FIG. 8 is a cross-sectional view showing a part of the manufacturing process of the semiconductor device.

[0040] The cross section of the contact structure of this semiconductor device is manufactured by the manufacturing method shown in FIG. (1) An element isolation region 2 and an element formation region 3 are formed on a silicon substrate 1.

[0041] (2) After an element is formed in the element formation region 3, an insulating film 4 is formed on the upper surface thereof. Then, contact holes 5 are formed in the insulating film 4.

[0042] (3) The titanium film 7 is deposited to 8 to 30 nm so as to be in contact with the upper surface of the insulating film 4, the insulating film side wall inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole 5.

[0043] (4) The silicon substrate 1 on which the titanium film 7 is deposited by 8 to 30 nm is heat-treated to cause a silicide reaction between the titanium film 7 and the silicon in the element formation region 3 to form a titanium silicide film 6 at the interface.

[0044] In order to cause a silicide reaction, the heat treatment temperature needs to be at least 650 ° C. or higher, and more preferably 800 ° C. or higher. Further, this temperature is preferably 1000 ° C. or lower in order to prevent diffusion of impurities introduced into silicon.

[0045] In the present embodiment, as shown in FIG. 8, all of the titanium film 7 is a titanium silicide film.

[0046] As described above, when the silicide reaction of all of the titanium film 7 is performed, the film thickness of the titanium silicide film is determined by the film thickness of the titanium film 7, so that the film thickness control of the titanium silicide film can be easily performed. .

[0047] In this case, since the titanium nitride film and the titanium silicide film are directly laminated, the in-film stress of the titanium nitride film is increased as compared with the case where the titanium film 7 exists between the titanium nitride film and the titanium silicide film. .

[0048] FIGS. 3 and 9 show a cross-sectional view of a contact structure of a semiconductor device according to a third embodiment of the present invention and a manufacturing method thereof, respectively.

[0049] The contact structure cross section of the semiconductor device of this embodiment is manufactured by the manufacturing method shown in FIG. (1) An element isolation region 2 and an element formation region 3 are formed on a silicon substrate 1. After the element is formed in the element formation region 3, an insulating film 4 is formed on the upper surface thereof. This insulating film is made of, for example, silicon oxide. A contact hole 5 having a hole diameter of 0.4 μm or less is formed in the insulating film in order to obtain conduction with the element formation region.

[0050] (2) The polycrystalline silicon film 10 is formed by, for example, CVD (Chemical Vapor Deposition) so as to be in contact with the upper surface of the insulating film 4, the insulating film side wall inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole. Is deposited, and the inside of the contact hole 5 is filled with the polycrystalline silicon 10. Thereafter, the polycrystalline silicon film deposited on the upper surface of the insulating film 4 is removed by etching or the like.

[0051] (3) A titanium film 7 is deposited to a thickness of 8 nm or more so as to be in contact with the upper surface of the insulating film 4, the insulating film sidewall inside the contact hole 5, and the upper surface of the polycrystalline silicon film 10 at the bottom of the contact hole.

[0052] (4) Thereafter, a titanium silicide film 6 is formed at the interface by a silicide reaction between the titanium film 7 and the polycrystalline silicon film 10 by heat treatment. The thickness of the titanium film 7 to be reacted at this time is 8 to 30 nm. As a result, the thickness of the titanium silicide film 6 formed by the heat treatment becomes 20 to 75 nm. Note that the heat treatment temperature for forming silicide is at least 650 ° C. or higher, and preferably 800 ° C. or higher. Further, this temperature is preferably 1000 ° C. or lower in order to prevent diffusion of impurities introduced into silicon.

[0053] In the present embodiment, as shown in (2) above, the polycrystalline silicon film 10 is deposited so as to be in contact with the upper surface of the insulating film 4, the sidewall of the insulating film inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole. However, the contact hole 5 is filled with the polycrystalline silicon 10, so that the depth of the contact hole 5 becomes shallow and the deposition of the titanium film 7, which is the next process, becomes easy.

[0054] As the contact hole diameter decreases, the aspect ratio (depth / diameter) of the contact hole tends to increase. With the sputtering method that has been used in the past, the wiring metal has a sufficient thickness on the side and bottom surfaces of the contact hole. It becomes difficult to coat.

[0055] However, it is possible to easily deposit a titanium film of 8 nm or more on the side and bottom surfaces of the contact hole by embedding polycrystalline silicon in the contact hole by a CVD technique having excellent step coverage and reducing the depth of the contact hole. it can.

[0056] In the present embodiment, as shown in FIG. 3, the titanium film 7 that has not been used for the silicide reaction exists between the titanium nitride film and the titanium silicide film.

[0057] In this way, the in-film stress of the titanium nitride film is reduced compared to the case where the titanium film 7 is present between the titanium nitride film and the titanium silicide film, and the titanium nitride film and the titanium silicide film are directly laminated. The peel strength of the film can be increased.

[0058] In order for the titanium layer 7 to be present between the titanium nitride film and the titanium silicide film, the thickness of the titanium layer 7 is set to be equal to or larger than the thickness of the silicide reaction, and the heat treatment temperature and the heat treatment time are controlled during the heat treatment. It is necessary to control the thickness of the silicide film to be 20 to 75 nm.

[0059] In the semiconductor device of this embodiment, a titanium silicide film 6 is formed at the interface between the polycrystalline silicon 10 deposited directly on the silicon substrate 1 and the electric wiring metal film 13 inside the contact hole. On the upper surface of the titanium silicide film, a titanium film 7, a titanium nitride film 8, and a tungsten film 9 are laminated as a metal film 13 for electric wiring. Further, a titanium film 7, a titanium nitride film 8, and a tungsten film 9 are laminated on the upper surface of the insulating film 4. The titanium film 7 does not necessarily remain, and the titanium nitride film 8 may be in direct contact with the insulating film 4. Further, the titanium nitride film 8 and the tungsten film 9 are not limited to this, and may be other conductive films and insulating films as shown in the first embodiment. Further, the laminated structure of different materials is not necessary.

[0060] FIGS. 4 and 10 show a cross-sectional view of a contact structure of a semiconductor device according to a fourth embodiment of the present invention and a manufacturing method thereof, respectively.

[0061] The contact structure of the semiconductor device of this embodiment is manufactured by the manufacturing method shown in FIG. (1) An element isolation region 2 and an element formation region 3 are formed on a silicon substrate 1. After the element is formed in the element formation region 3, an insulating film 4 is formed on the upper surface thereof. This insulating film is made of, for example, silicon oxide. A contact hole 5 is formed in the insulating film in order to obtain conduction with the element formation region.

[0062] (2) The polycrystalline silicon film 10 is formed by, for example, CVD (Chemical Vapor Deposition) so as to be in contact with the upper surface of the insulating film 4, the sidewall of the insulating film inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole. Is deposited, and the inside of the contact hole 5 is filled with the polycrystalline silicon 10. Thereafter, the polycrystalline silicon film deposited on the upper surface of the insulating film 4 is removed by etching or the like.

[0063] (3) The titanium film 7 is deposited to 8 to 30 nm so as to be in contact with the upper surface of the insulating film 4, the insulating film side wall inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole 5.

[0064] (4) The silicon substrate 1 on which the titanium film 7 is deposited by 8 to 30 nm is heat-treated to cause a silicide reaction between the titanium film 7 and the silicon in the element formation region 3 to form a titanium silicide film 6 at the interface.

[0065] Note that the heat treatment temperature for forming silicide is at least 650 ° C. or higher, and preferably 800 ° C. or higher. Further, this temperature is preferably 1000 ° C. or lower in order to prevent diffusion of impurities introduced into silicon.

[0066] In the present embodiment, as shown in (2) above, the polycrystalline silicon film 10 is deposited so as to be in contact with the upper surface of the insulating film 4, the sidewall of the insulating film inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole. However, the contact hole 5 is filled with the polycrystalline silicon 10, so that the depth of the contact hole 5 becomes shallow and the deposition of the titanium film 7, which is the next process, becomes easy.

[0067] As the contact hole diameter decreases, the aspect ratio (depth / diameter) of the contact hole tends to increase. With the sputtering method that has been used in the past, the wiring metal has a sufficient thickness on the side and bottom surfaces of the contact hole. It becomes difficult to coat.

[0068] However, it is possible to easily deposit a titanium film of 8 nm or more on the side and bottom surfaces of the contact hole by embedding polycrystalline silicon in the contact hole by a CVD technique having excellent step coverage and reducing the depth of the contact hole. it can.

[0069] In the present embodiment, as shown in FIG. 4, all of the titanium film 7 is a titanium silicide film.

[0070] As described above, when the silicide reaction of all of the titanium film 7 is performed, the film thickness of the titanium silicide film is determined by the film thickness of the titanium film 7, so that the film thickness control of the titanium silicide film can be easily performed. .

[0071] In this case, since the titanium nitride film and the titanium silicide film are directly laminated, the in-film stress of the titanium nitride film is increased as compared with the case where the titanium film 7 exists between the titanium nitride film and the titanium silicide film. .

[0072] In the contact portion of the semiconductor device of this embodiment, a titanium silicide film 6 is formed at the interface between the polycrystalline silicon 10 deposited directly on the silicon substrate 1 and the metal film 13 for electric wiring inside the contact hole 5. On the upper surface of the titanium silicide film, a titanium nitride film 8 and a tungsten film 9 are laminated as a metal film 13 for electric wiring. Further, a titanium film 7, a titanium nitride film 8, and a tungsten film 9 are laminated on the upper surface of the insulating film 4. The titanium film 7 does not necessarily remain, and the titanium nitride film 8 may be in direct contact with the insulating film 4. The titanium nitride film 8 and the tungsten film 9 are not limited to this, and may be other conductive films or insulating films. Further, the laminated structure of different materials is not necessary.

[0073] 5 and 12 show a sectional view of a gate electrode conduct structure of a MOS (Metal Oxide Semiconductor) transistor according to a fifth embodiment of the present invention and a manufacturing method thereof, respectively.

[0074] The contact structure of the semiconductor device of this embodiment is manufactured by the manufacturing method shown in FIG. That is, (1) a silicon oxide film 11 having a thickness of about 15 nm is formed in the element formation region 3 on the silicon substrate 1. A polycrystalline silicon film is formed on the silicon oxide film 11 by CVD (Chemical Vapor Deposition), a resist pattern is formed by photolithography, and a polycrystalline silicon film is formed by dry etching using the resist pattern as a mask. The polycrystalline silicon gate electrode 12 is formed by patterning the film and the silicon oxide film.

[0075] (2) The insulating film 4 is deposited on the upper surface of the silicon substrate 1 and the upper surface of the gate electrode 12, and a contact hole 5 is opened so as to reach the gate electrode in order to establish conduction with the gate electrode 12.

[0076] (3) The titanium film 7 is deposited so as to be in contact with the gate electrode 12 on the upper surface of the insulating film 4 and inside the contact hole 5.

[0077] (4) Thereafter, a titanium silicide film 6 is formed at the interface by a silicide reaction between the titanium film 7 and the silicon of the gate electrode 12 by heat treatment. The thickness of the titanium film 7 to be reacted at this time is 8 to 30 nm. Note that the heat treatment temperature for forming silicide is at least 650 ° C. or higher, and preferably 800 ° C. or higher. Further, this temperature is preferably 1000 ° C. or lower in order to prevent diffusion of impurities introduced into silicon.

[0078] In the present embodiment, as shown in FIG. 5, the titanium film 7 that has not been used for the silicide reaction exists between the titanium nitride film and the titanium silicide film.

[0079] As described above, when the titanium film 7 exists between the titanium nitride film and the titanium silicide film, the in-film stress of the titanium nitride film is reduced and the nitridation is performed as compared with the case where the titanium nitride film and the titanium silicide film are directly laminated. The peel strength of the titanium film can be increased.

[0080] In order for the titanium layer 7 to be present between the titanium nitride film and the titanium silicide film, the thickness of the titanium layer 7 is set to be equal to or larger than the thickness of the silicide reaction, and the heat treatment temperature and the heat treatment time are controlled during the heat treatment. It is necessary to control the thickness of the silicide film to be 20 to 75 nm.

[0081] In the contact portion of the semiconductor device of this embodiment, a titanium silicide film 6 is formed in the contact hole 5 at the interface between the metal film 13 for electrical wiring and the gate electrode 12 made of polycrystalline silicon. 5 and 12 show the case where an unreacted titanium film 7 and titanium nitride 8 are stacked on the upper surface of the titanium silicide film 6 as the metal film 13 for electrical wiring. However, the titanium film 7 having a thickness of 8 to 30 nm is deposited on the upper surface of the gate electrode 12, the titanium silicide film 6 is formed so as to consume all of the titanium film, and the titanium film 7 does not remain on the upper surface of the titanium silicide film 6. Also good. Further, the titanium nitride film 8 may be in direct contact with the insulating film 4. The titanium nitride film 8 is not limited to this, and may be another conductive film or an insulating film. Further, the laminated structure of different materials is not necessary.

[0082] FIGS. 6 and 13 show a sectional view of a gate electrode contact structure of a MOS transistor according to a sixth embodiment of the present invention and a manufacturing method thereof, respectively.

[0083] The contact structure of the semiconductor device of this embodiment is manufactured by the manufacturing method shown in FIG. That is, (1) a silicon oxide film 11 having a thickness of about 15 nm is formed in the element formation region 3 on the silicon substrate 1. A polycrystalline silicon film is formed on the silicon oxide film 11 by CVD (Chemical Vapor Deposition), a resist pattern is formed by photolithography, and a polycrystalline silicon film is formed by dry etching using the resist pattern as a mask. The polycrystalline silicon gate electrode 12 is formed by patterning the film and the silicon oxide film.

[0084] (2) The insulating film 4 is deposited on the upper surface of the silicon substrate 1 and the upper surface of the gate electrode 12, and a contact hole 5 is opened so as to reach the gate electrode in order to establish conduction with the gate electrode 12. A polycrystalline silicon film 10 is deposited by, for example, CVD so as to be in contact with the upper surface of the insulating film 4, the sidewall of the insulating film inside the contact hole 5, and the upper surface of the gate electrode 12 at the bottom of the contact hole. Buried. Thereafter, the polycrystalline silicon film deposited on the upper surface of the insulating film 4 is removed by etching or the like.

[0085] (3) A titanium film 7 is deposited on the upper surface of the insulating film 4 and the entire upper surface of the polycrystalline silicon film 10.

[0086] (4) Thereafter, a titanium silicide film 6 is formed at the interface by a silicide reaction between the titanium film 7 and the polycrystalline silicon 10 by heat treatment. The thickness of the titanium film 7 to be reacted at this time is 8 to 30 nm. Note that the heat treatment temperature for forming silicide is at least 650 ° C. or higher, and preferably 800 ° C. or higher. Further, this temperature is preferably 1000 ° C. or lower in order to prevent diffusion of impurities introduced into silicon.

[0087] In the present embodiment, as shown in (2) above, the polycrystalline silicon film 10 is deposited so as to be in contact with the upper surface of the insulating film 4, the sidewall of the insulating film inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole. However, the contact hole 5 is filled with the polycrystalline silicon 10, so that the depth of the contact hole 5 becomes shallow and the deposition of the titanium film 7, which is the next process, becomes easy.

[0088] As the contact hole diameter decreases, the aspect ratio (depth / diameter) of the contact hole tends to increase. With the sputtering method that has been used in the past, the wiring metal has a sufficient thickness on the side and bottom surfaces of the contact hole. It becomes difficult to coat.

[0089] However, it is possible to easily deposit a titanium film of 8 nm or more on the side and bottom surfaces of the contact hole by embedding polycrystalline silicon in the contact hole by a CVD technique having excellent step coverage and reducing the depth of the contact hole. it can.

[0090] In the present embodiment, as shown in FIG. 3, the titanium film 7 that has not been used for the silicide reaction exists between the titanium nitride film and the titanium silicide film.

[0091] Thus, when the titanium film 7 exists between the titanium nitride film and the titanium silicide film, the in-film stress of the titanium nitride film is reduced and the nitridation is performed as compared with the case where the titanium nitride film and the titanium silicide film are directly laminated. The peel strength of the titanium film can be increased.

[0092] In order for the titanium layer 7 to be present between the titanium nitride film and the titanium silicide film, the thickness of the titanium layer 7 is set to be equal to or larger than the thickness of the silicide reaction, and the heat treatment temperature and the heat treatment time are controlled during the heat treatment. It is necessary to control the thickness of the silicide film to be 20 to 75 nm.

[0093] In the contact portion of the semiconductor device of the present embodiment, a titanium silicide film 6 is formed at the interface between the polycrystalline silicon 10 embedded in contact with the gate electrode 12 and the metal film 13 for electric wiring inside the contact hole 5. Yes. 6 and 13 show a case where an unreacted titanium film 7 and a titanium nitride film 8 are stacked on the upper surface of the titanium silicide film 6 as the metal film 13 for electric wiring. However, the titanium film 7 having a thickness of 8 to 30 nm is deposited on the upper surface of the gate electrode 12, the titanium silicide film 6 is formed so as to consume all of the titanium film, and the titanium film 7 does not remain on the upper surface of the titanium silicide film 6. Also good. Further, the titanium nitride film 8 may be in direct contact with the insulating film 4. The titanium nitride film 8 is not limited to this, and may be other conductive film or insulating film as shown in the first embodiment. Further, the laminated structure of different materials is not necessary. The thickness of the titanium silicide film 6 is 20 to 75 nm.

[0094] In the manufacturing steps in all the embodiments described above, the titanium silicide film is formed by the heat treatment after the step of depositing the titanium film 7 so as to be in contact with the single crystal silicon substrate 1 or the polycrystalline silicon 10. The case where there is a process to perform has been described. However, the manufacturing process described in each embodiment is not limited to this, and may be a manufacturing process as shown in FIG. (1) An element isolation region 2 and an element formation region 3 are formed on a silicon substrate 1.

[0095] (2) After the element is formed in the element forming region 3, the insulating film 4 is formed on the upper surface thereof. This insulating film is made of, for example, silicon oxide. A contact hole 5 is formed in the insulating film in order to obtain conduction with the element formation region.

[0096] (3) The titanium film 7 is deposited so as to be in contact with the upper surface of the insulating film 4, the sidewall of the insulating film inside the contact hole 5, and the upper surface of the element formation region 3 at the bottom of the contact hole. Further, a titanium nitride film 8 and a tungsten film 9 are laminated on the upper surface of the titanium film 7. The titanium nitride film 8 and the tungsten film 9 are not limited to this, and may be other conductive films or insulating films.

[0097] (4) Thereafter, a titanium silicide film 6 is formed at the interface by a silicide reaction between the titanium film 7 and silicon in the element formation region 3 by heat treatment. The thickness of the titanium film 7 to be reacted at this time is 8 to 30 nm. As a result, the thickness of the titanium silicide film 6 formed by

the heat treatment becomes 20 to 75 nm. Note that the heat treatment temperature for forming silicide is at least 650 ° C. or higher, and preferably 800 ° C. or higher. Further, this temperature is preferably 1000 ° C. or lower in order to prevent diffusion of impurities introduced into silicon.

[0098] By setting the thickness of the titanium silicide film 6 to be formed to 20 to 75 nm, the contact resistance value between silicon and titanium can be reduced, and the average stress generated at the interface between the silicon and titanium silicide film can be reduced. It is possible to make the disconnection occurrence critical stress value or less, and a good contact is obtained in which the titanium silicide film does not peel off.

[0099] FIG. 11 shows the case where an unreacted titanium film 7, titanium nitride film 8, and tungsten film 9 are stacked as the metal film 13 for electrical wiring on the upper surface of the titanium silicide film 6. However, a titanium film 7 having a thickness of 8 to 30 nm is deposited so as to be in contact with the element formation region 3 on the silicon substrate 1, a titanium silicide film 6 is formed so as to consume all of the titanium film, and titanium titanium is formed on the titanium silicide film 6. The film 7 may not remain. Further, the titanium nitride film 8 may be in direct contact with the insulating film 4. The titanium nitride film 8 and the tungsten film 9 are not limited to this, and may be other conductive films or insulating films. Further, the laminated structure of different materials is not necessary. The thickness of the titanium silicide film 6 is 20 to 75 nm.

[0100] According to the present invention, in a semiconductor device in which silicon and an electric wiring metal are connected via a titanium silicide film inside a contact hole provided in the insulating film, the thickness of the titanium silicide film is increased. By setting the thickness to 20 nm or more and 75 nm or less, the contact resistance between silicon and the metal wiring can be reduced, and a good contact without fear of disconnection at the interface between silicon and titanium silicide can be formed.

[0101] Brief Description of Drawings

[0102] 1 is a cross-sectional view showing a contact structure of a semiconductor device according to a first embodiment of the present invention.

[0103] 2 is a cross-sectional view showing a contact structure of a semiconductor device according to a second embodiment of the present invention.

[0104] 3 is a cross-sectional view showing a contact structure of a semiconductor device according to a third embodiment of the present invention.

[0105] 4 is a cross-sectional view showing a contact structure of a semiconductor device according to a fourth embodiment of the present invention.

[0106] 5 is a cross-sectional view showing a gate electrode contact structure of a MOS transistor according to a fifth embodiment of the present invention.

[0107] 6 is a cross-sectional view showing a gate electrode contact structure of a MOS transistor according to a sixth embodiment of the present invention.

[0108] 7 is a cross-sectional view showing a part of the manufacturing process of the semiconductor device according to the first embodiment of the present invention.

[0109] 8 is a cross-sectional view showing a part of the manufacturing process of the semiconductor device according to the second embodiment of the present invention.

[0110] 9 is a cross-sectional view showing a part of the manufacturing process of the semiconductor device according to the third embodiment of the present invention.

[0111] 10 is a cross-sectional view showing a part of the manufacturing process of the semiconductor device according to the fourth embodiment of the present invention.

[0112] 11 is a cross-sectional view showing a part of the manufacturing process of the semiconductor device according to the fifth embodiment of the present invention.

[0113] 12 is a cross-sectional view showing a part of the manufacturing process of the MOS transistor according to the sixth embodiment of the present invention.

[0114] 13 is a cross-sectional view showing a part of the manufacturing process of the MOS transistor according to the seventh embodiment of the present invention.

[0115] 14 is a schematic diagram showing the mechanism of the silicon interface change due to the silicide reaction.

[0116] 15 is a graph showing the stress in the film accompanying the silicide reaction.

[0117] 16 is a graph showing the relationship between the average stress generated at the interface between the silicon film and the titanium silicide film, the titanium film thickness, and the contact hole hole diameter.

[0118] 17 is a graph showing the relationship between the disconnection failure rate (titanium silicide film peeling) and the titanium silicide film thickness when the contact hole hole diameter is 0.4 μm.

[0119] Explanation of symbols

[0120] DESCRIPTION OF SYMBOLS 1 ... Silicon substrate, 2 ... Element isolation region, 3 ... Element formation area, 4 ... Insulating film, 5 ... Contact hole, 6 ... Titanium silicide film, 7 ... Titanium film, 8 ... Titanium nitride film, 9 ... Tungsten film, 10 ... polycrystalline silicon, 11 ... silicon oxide film, 12 ... gate electrode, 13 ... metal film for electrical wiring, 21 ... silicon, 22 ... titanium film, 23 ... initial silicon / titanium interface, 24 ... titanium silicide / silicon interface.

JP2001223180A SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

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The wording below is an initial machine translation of the original publication. To apply more advanced translation technology, use Patent Translate.

1. In a semiconductor device in which silicon and a metal for electric wiring are connected via a titanium silicide film inside a contact hole provided in the insulating film, the thickness of the titanium silicide film is 20 nm to 75 nm. Semiconductor device.

2. In a semiconductor device in which the silicon substrate and an electric wiring metal are connected via a titanium silicide film inside a contact hole provided in an insulating film on the silicon substrate, the thickness of the titanium silicide film is 20 nm or more and 75 nm or less. A semiconductor device characterized by the above.

3. In the semiconductor device in which the silicon substrate and the metal for electric wiring are connected via a titanium silicide film inside a contact hole provided in the insulating film on the silicon substrate, the interface between the silicon substrate and the insulating film, A semiconductor device, wherein a distance between surfaces of a silicon substrate and an interface between titanium silicide is 18 nm or more and 69 nm or less.

4. In the semiconductor device in which the polycrystalline silicon deposited on the silicon substrate inside the contact hole provided in the insulating film on the silicon substrate and the metal for electric wiring are connected via the titanium silicide film, the titanium silicide A semiconductor device having a film thickness of 20 nm to 75 nm.

5. A single crystal silicon substrate, a MOS transistor whose gate electrode formed on the single crystal silicon substrate is polycrystalline silicon, and an insulating film formed on the surface of the single crystal silicon substrate on which the MOS transistor is formed. In the semiconductor device in which the gate electrode and the metal for electric wiring are connected through the titanium silicide film inside the contact hole provided in the insulating film, the thickness of the titanium silicide film is 20 nm or more and 75 nm or less. A semiconductor device.

6. The semiconductor device according to claim 1, wherein a surface of the metal for electric wiring that is in contact with the titanium silicide film is titanium.

7. The semiconductor device according to claim 1, wherein a diameter of the contact hole is 0.4 μm or less.

8. An insulating film is provided on the silicon substrate, a contact hole is opened in the insulating film, a titanium film is deposited so as to be in contact with the silicon substrate inside the contact hole, and then the titanium film and the silicon are heat-treated. A method for manufacturing a semiconductor device, comprising subjecting a titanium film to a silicide reaction with a thickness of 8 nm to 30 nm.

9. After an insulating film is provided on the silicon substrate, a contact hole is opened in the insulating film, polycrystalline silicon is buried inside the contact hole, and a titanium film is deposited so as to contact the polycrystalline silicon inside the contact hole. A method of manufacturing a semiconductor device, wherein the titanium film and the silicon are heat-treated to cause a silicide reaction between a thickness of 8 nm and 30 nm of the titanium film.

10. An insulating film is provided on a silicon substrate, a contact hole is opened in the insulating film, and a titanium film is deposited in a thickness of 8 nm to 30 nm so as to be in contact with the silicon substrate inside the contact hole. A method of manufacturing a semiconductor device, wherein the silicon is heat-treated to cause a silicidation of all of the titanium film.

11. The method of manufacturing a semiconductor device according to claim 7, wherein the diameter of the contact hole is 0.4 .mu.m or less.

12. The method of manufacturing a semiconductor device according to claim 7, wherein a heat treatment temperature for forming the titanium silicide film is 650.degree. C. or more.

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　平3−29355

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		8624−5F　H 01 L 27/10　325 C	

審査請求　未請求　請求項の数 1　（全3頁）

㊹発明の名称　半導体装置

㉑特　願　平1−163101
㉒出　願　平1(1989)6月26日

㉗発明者　米田　清　大阪府守口市京阪本通2丁目18番地　三洋電機株式会社内
㉗発明者　辻村　和俊　大阪府守口市京阪本通2丁目18番地　三洋電機株式会社内
㉑出願人　三洋電機株式会社　大阪府守口市京阪本通2丁目18番地
㉔代理人　弁理士　西野　卓嗣　外2名

明　細　書

1. 発明の名称　半導体装置

2. 特許請求の範囲

（1）下層導電体膜、誘電体膜及び上層導電体膜を順次積層して形成したキャパシタを有する半導体装置において、上記誘電体膜は、上記下層導電体膜上に、チタン窒化膜、チタン酸化膜及びシリコン酸化膜を順次積層したものであることを特徴とする半導体装置。

3. 発明の詳細な説明

（イ）産業上の利用分野

本発明は、下層導電体膜、誘電体膜及び上層導電体膜を順次積層して形成したキャパシタを有する半導体装置に関する。

（ロ）従来の技術

従来、ダイナミックメモリ等、その回路中にキャパシタを有する半導体装置において、例えばプレーナ型メモリセルの場合、誘電体膜としては、シリコン基板を熱酸化したシリコン酸化膜を用いてきた。

しかしながら、キャパシタ容量は次式で表わされるため、

$Cs = \varepsilon i \cdot S / tox$

（εi：誘電率、S：キャパシタ面積、tox：誘電体膜厚）高集積化、高密度化のために小面積にて必要なキャパシタ容量を確保するには同一構造のセルの場合、誘電体膜厚toxを小さくする必要がある。しかし絶縁耐圧の点から、上記シリコン熱酸化膜の極薄化にも限度がある。そのため、トレンチキャパシタやスタックトキャパシタなどのようにキャパシタ構造を3次元化することにより小面積のセルにおいても、電極の面積を大きくしてキャパシタ容量を確保している。しかし、それでも電極の面積が6～7μm^2では、キャパシタ容量を30fF以上確保するためのシリコン酸化膜の膜厚として、7～8□□必要とする。

このような極薄膜では絶縁耐圧不足や、更には膜厚制御の困難性等、多くの問題がある。

そのため近年では、シリコン酸化膜の代わりに

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シリコン酸化膜とシリコン窒化膜との組み合せが用いられ始めており（１９８８年９月号日経マイクロデバイス第６５頁）、更には高誘電体膜として、タンタル酸化膜が提案されている。

(ハ) 発明が解決しようとする課題

しかしながら、前述のシリコン酸化膜とシリコン窒化膜との組み合せでは誘電率が７となり、シリコン酸化膜の誘電率（３～４）の２倍程度であるため、さらに高集積化・高密度化を進める上で効果は少ない。一方、タンタル酸化膜については誘電率が２０と大きいものの、リーク電流が多いなどまだまだ問題点が多い。

従って、本発明は、斯る諸問題を解決したキャパシタ構造を提供するものである。

(ニ) 課題を解決するための手段

本発明は、半導体装置内のキャパシタの誘電体膜として、下層導電体膜上にチタン窒化膜、チタン酸化膜及びシリコン酸化膜を順次積層し、これら３層からなる絶縁膜体積体を用いることを特徴とする。

(ホ) 作　用

上記３層構造の誘電体膜を用いることで、絶縁耐圧が高まり、かつリーク電流が小さくなる。又斯る誘電体膜は１００程度の非常に高い誘電率を有するチタン酸化膜を含んでいるので十分な容量を実現できる。

(ヘ) 実施例

本発明をスタックトキャパシタ構造に適用した実施例につき、図面を参照し、製造工程順に説明する。

第１図にて、(1)はシリコン基板、(2)(2)は夫々、ソース、ドレインとなる拡散領域、(3)はシリコン酸化膜、(4)は、拡散領域(2)(2)と共にＭＯＳトランジスタを構成する多結晶シリコンからなるゲート配線、(5)は他のＭＯＳトランジスタにおける同様のゲート配線、(6)は多結晶シリコンからなる、キャパシタの下層導電体膜である。斯る構成は従来のものと同様である。

第２図にて、(7)はチタン窒化膜（ＴｉＮ）、(8)はチタン酸化膜（TiO_2）である。前者の膜(7)はＴｉターゲットを用い、アルゴンガスと窒素ガスとの混合下でスパッタリングを行うことにより形成され、その膜厚は約５０㎚である。後者の膜(8)は、上記のスパッタリング条件において、窒素ガスの代りに酸素ガスを用いることにより得られ、その膜厚は約５０㎚である。

第３図にて、C_2F_6ガスを用いたＲＩＥエッチングにより、チタン窒化膜(7)及びチタン酸化膜(8)の不要部分が除去される。

第４図にて、(9)はシリコン酸化膜（SiO_2）であり、斯る膜は、ジクロルシランガスと亜酸化窒素ガスを減圧下で反応させることにより得られ、その膜厚は２００㎚である。

第５図にて、第３図の場合と同様にして、シリコン酸化膜(9)の不要部分が除去される。本工程において、チタン窒化膜(7)、チタン酸化膜(8)及びシリコン酸化膜(9)からなるキャパシタ用誘電体膜(10)が形成されたことになる。

第６図にて、(11)は多結晶シリコンからなる上層導電体膜であり、これ自体は従来のものと同様である。

以上により、下層導電体(6)、誘電体膜(10)及び上層導電体(11)からなるキャパシタが得られ、その後、必要に応じて、斯るキャパシタの上に絶縁膜を介して多層配線が施される。

上記実施例において形成されたキャパシタは、８μm^2程度の微小面積において、３.３Ｖの電源電圧下でもキャパシタ容量１２０ｆＦを確保でき、更にリーク電流も５MV/cmの電界下で、良好な値$3.5\times10^{-9}A/cm^2$を得られた。

上記実施例において、下層導電体膜(6)として、$TiSi_2$やWSi_2等のシリサイドを用いることにより、電気抵抗の低減、更には付着強度の向上を図ることができる。

(ト) 発明の効果

本発明半導体装置のキャパシタ構造によれば、小面積かつ比較的厚い膜で大きなキャパシタ容量が得られ、その結果、集積度の向上や、半導装置製造プロセス上、各種膜厚制御の容易化が図れる。

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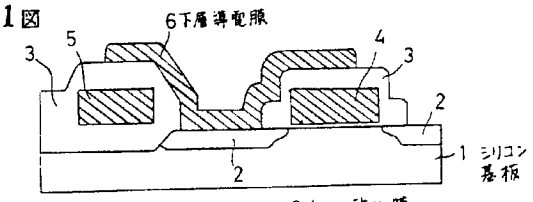
4. 図面の簡単な説明

第1図乃至第6図は本発明実施例を説明するための製造工程別断面図である。

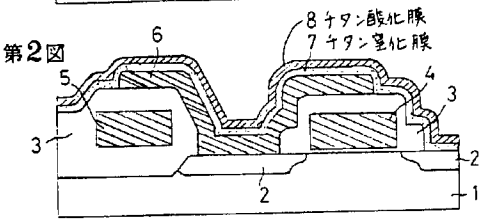
出願人　三洋電機株式会社

代理人　弁理士　西野卓嗣（外2名）

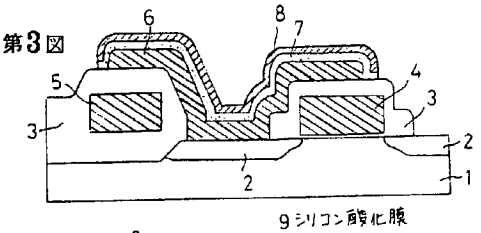
第1図



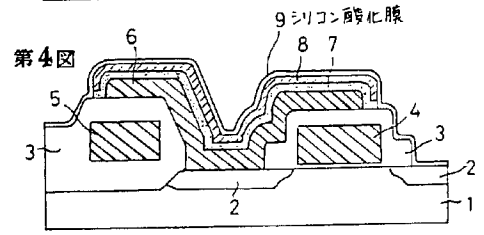
第2図



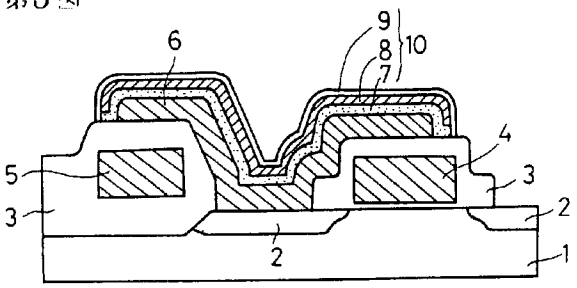
第3図



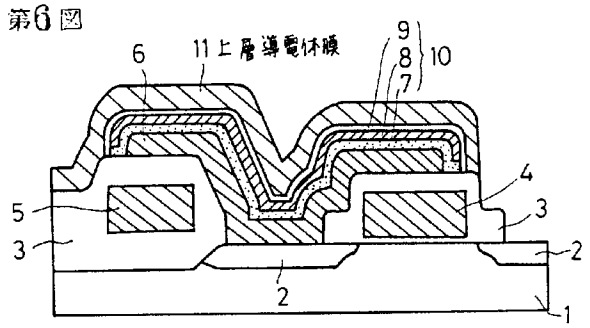
第4図



第5図



第6図



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JPH0329355A SEMICONDUCTOR DEVICE

Applicants: SANYO ELECTRIC CO

Inventors: TSUJIMURA KAZUTOSHI,YONEDA KIYOSHI

Classifications:
IPC ***H01L21/822; H01L21/8242; H01L27/04; H01L27/10; H01L27/108;*** (IPC1-7): H01L27/04; H01L27/108;

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SEMICONDUCTOR DEVICE

Abstract

PURPOSE:To realize a high integration and a high density by a method wherein, as a dielectric film for a capacitor, a titanium nitride film, a titanium oxide film and a silicon oxide film are laminated one after another on a lower-layer conductor film and an insulating-film laminated body composed of these three layers is used. CONSTITUTION:The following are provided: a silicon substrate 1; diffusion regions 2, 2 to be used as a source and a drain; a silicon oxide film 3; a gate interconnection 4 composed of polycrystalline silicon; a gate interconnection 5 in another MOS transistor; and a lower-layer conductive film 6 of a capacitor. In addition, the following are formed: a titanium nitride film 7; a titanium oxide film 8; a silicon oxide film 9; and an upper-layer conductor film 11 composed of polycrystalline silicon. A dielectric film 10 for capacitor use is formed of the titanium nitride film 7, the titanium oxide film 8 and the silicon oxide film 9. A capacitor composed of the lower-layer conductor film 6, the dielectric film 10 and the upper-layer conductor film 11 can be obtained. Thereby, a large capacitance can be obtained in a small area and by a comparatively thick film; the integration scale can be enhanced and a high density can be realized.

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DESCRIPTION JPH0329355

[0001]

(A) Field of Industrial Application The present invention relates to a semiconductor device having a capacitor formed by sequentially laminating a lower conductor film, a dielectric film and an upper conductor film. (B) Conventional Technology Conventionally, in a semiconductor device having a capacitor in its circuit such as a dynamic memory, for example, in the case of a planar type memory cell, a silicon oxide film obtained by thermally oxidizing a silicon substrate has been used as a dielectric film. . However, since the capacitance of the capacitor is expressed by the following formula, Cs = ε i−S / tox (ε 1: dielectric constant, S: capacitor area, tox: dielectric film thickness) is increased to 4 AWt and a small area is required for high density. In the case of cells having the same structure, it is necessary to reduce the dielectric film thickness tox in order to secure the required capacitor capacity. However, from the viewpoint of withstand voltage, there is a limit to the ultrathinning of the silicon thermal oxide film. Therefore, by making the capacitor structure three-dimensional such as a trench capacitor or a stacked capacitor, the area of the electrode is increased to secure the capacitor capacitance even in a cell having a small area. However, even if the area of the electrode is 6 to 7 μm2, the film thickness of the silicon oxide film for securing the capacitor capacitance of 30 fF or more requires 7 to 8 nm. Such an ultrathin film has many problems such as insufficient dielectric strength and difficulty in controlling the film thickness. Therefore, in recent years, a combination of a silicon oxide film and a silicon nitride film has begun to be used instead of the silicon oxide film (September 1988, Nikkei Microdevices, page 65), and as a high dielectric film, a tantalum oxide film is used. Has been proposed. (C) Problems to be Solved by the Invention However, the above-mentioned combination of the silicon oxide film and the silicon nitride film has a dielectric constant of 7, which is about twice the dielectric constant (3-4) of the silicon oxide film. Further ?: 5 There is little effect in promoting integration and high density. On the other hand, the tantalum oxide film has a large dielectric constant of 20, but still has many problems such as a large leak current.

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Therefore, the present invention provides a capacitor structure that solves these problems. (2) Means for Solving the Problems In the present invention, as a dielectric film of a capacitor in a semiconductor device, a titanium nitride film, a titanium oxide film and a silicon oxide film are sequentially laminated on a lower conductor film, and these three layers are formed. It is characterized by using an insulating film volume consisting of. (E) Action By using the dielectric film having the three-layer structure, the dielectric strength is increased and the leak current is reduced. Further, since such a dielectric film contains a titanium oxide film having a very high dielectric constant of about 100, a sufficient capacity can be realized.

(V) Example An example in which the present invention is applied to a stacked cavitator structure will be described in the order of manufacturing steps with reference to the drawings. In FIG. 1, (1) is a silicon substrate, (2) (2+ is diffusion regions to be the source and drain, respectively, (3) is a silicon oxide film, (4) is diffusion region +2 1 (2)) Also, a gate wiring made of polycrystalline silicon that constitutes a MOS transistor, {5} is a similar gate wiring in another MOS transistor, and (6) is a lower conductor film of a capacitor made of polycrystalline silicon. Such elliptical command is similar to the conventional one. In FIG. 2, (7) is a titanium nitride film (TiN), and (8) is a titanium oxide WA (T i O 2). The former JI5! (7) is formed by using a Ti target and performing sputtering in a mixture of argon gas and nitrogen gas, and the film thickness thereof is about 500 squares. The latter film (8) is obtained by using oxygen gas instead of nitrogen gas under the above-mentioned sputtering conditions, and its film thickness is about 50 glm. In FIG. 3, unnecessary portions of the titanium nitride II 51 (7) and the titanium oxide film {8} are removed by RIE etching using C2F6 gas. In FIG. 4, (9) is a silicon oxide film (SiO2>), which is obtained by reacting dichlorosilane gas with nitrous oxide gas under reduced pressure, and its film thickness is 20 am. . In FIG. 5, as in the case of FIG. 3, silicon oxide 119! (The unnecessary portion of 91 is removed. In this step, titanium nitride JI5I (71, titanium oxide film (8) and silicon oxide Jl !! (9) The capacitor dielectric fi (10) is formed. In FIG. 6, (11) is an upper conductor film made of polycrystalline silicon, which is the same as the conventional one. As described above, a capacitor composed of the lower conductor (6), the dielectric film (10) and the upper conductor (Ill) is obtained, and then, if necessary, a multilayer wiring is formed on the capacitor via an insulating film. Given. The capacitor formed in the above embodiment can secure a capacitor capacity of 120 fF even under a power supply voltage of 3.3 in a small area of about 8 μm2, and the leakage current is excellent under an electric field of 5 M '// cm. A value of 3.5X10-'^ / cm "was obtained. In the above embodiment, by using a silicide such as TiSi2 or WSi2 as the lower conductor 115H6), it is possible to reduce the electric resistance and further improve the adhesion strength.

(G) Effect of the Invention According to the capacitor structure of the semiconductor device of the present invention, a large capacitor capacitance can be obtained with a small area and a relatively thick film, and as a result, various films can be obtained in the IAWt degree

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improvement and the semiconductor device manufacturing process. The thickness control can be localized. 4.

[0002]
Brief description of the drawings

[0003]
1 to 6 are cross-sectional views by manufacturing process for explaining an embodiment of the present invention.

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CLAIMS JPH0329355

1.
In a semiconductor device having a capacitor formed by sequentially laminating an electric film, a dielectric film and an upper conductive film, the dielectric film is formed by depositing a titanium nitride film, a titanium oxide film and a silicon oxide film on the lower conductive film. A semiconductor device comprising a stack of films in sequence.

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21/336		29/78	３０１Ｐ
29/78			

請求項の数６(全　６　頁)

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(73)特許権者　000004237
日本電気株式会社
東京都港区芝五丁目７番１号
(72)発明者　三浦　喜直
東京都港区芝五丁目７番１号　日本電気株式会社内
(72)発明者　石田　宏一
東京都港区芝五丁目７番１号　日本電気株式会社内
(74)代理人　100088328
弁理士　金田　暢之　(外２名)
審査官　長谷山　健

(56)参考文献　特開　平10－335265（ＪＰ，Ａ）

最終頁に続く

(54)【発明の名称】　半導体装置及びその製造方法

(57)【特許請求の範囲】

【請求項１】　シリサイド化固相反応での拡散種がＮｉ，Ｖ，Ｐｔ及びＰｄからなる群から選択される１種の金属原子であるシリサイドがＳｉ基板上に直接形成されてオーミックコンタクトを形成する半導体装置の製造方法において、Ｓｉ基板上に厚さ０．５～１．５ｎｍの窒化シリコン膜を形成する工程、前記拡散種の金属原子の薄膜を堆積する工程、及び熱処理によって拡散層にのみ前記金属原子のシリサイドを形成する工程とを有することを特徴とする、半導体装置の製造方法。

【請求項２】　シリサイド化固相反応での拡散種がＮｉであり、熱処理よって拡散層にのみエピタキシャルＮｉ$Ｓｉ_2$が形成されることを特徴とする、請求項１に記載の半導体装置の製造方法。

【請求項３】　シリサイド化固相反応での拡散種がＮｉ，Ｖ，Ｐｔ及びＰｄからなる群から選択される１種の金属原子であるシリサイドがＳｉ基板上に直接形成されてオーミックコンタクトを形成する半導体装置において、該シリサイドがＳｉ基板上に厚さ０．５～１．５ｎｍの窒化シリコン膜を形成した後に、該窒化シリコン膜上に堆積された前記拡散種の金属原子の薄膜から前記窒化シリコン膜を通して熱拡散により拡散した金属原子とのシリサイド化固相反応によるものであることを特徴とする半導体装置。

【請求項４】　シリサイド化固相反応での拡散種がＮｉであり、熱処理によって拡散層にのみエピタキシャルＮｉ$Ｓｉ_2$が形成されていることを特徴とする請求項３に記載の半導体装置。

【請求項５】　シリサイド化固相反応での拡散種がＮｉ，Ｖ，Ｐｔ及びＰｄからなる群から選択される１種の

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金属原子であるシリサイドがＳｉ基板上に直接形成されてオーミックコンタクトを形成する半導体装置において、該シリサイドがＳｉ基板上に厚さ０．５～１．５ｎｍの窒化シリコン膜を形成した後に、該窒化シリコン膜上に堆積された前記拡散種の金属原子の薄膜から前記窒化シリコン膜を通して熱拡散により拡散した金属原子とのシリサイド化固相反応によるものであり、前記形成されたシリサイド上に窒化シリコン膜が残留していることを特徴とする半導体装置。

【請求項６】　前記拡散種となる金属原子がＮｉであり、形成されるシリサイドがエピタキシャル$NiSi_2$である請求項５に記載の半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置の製造方法において、Ｓｉ基板上にシリサイド電極を形成する方法及び該方法により製造される半導体装置の構造に関するものである。

【０００２】

【従来の技術】近年のデバイスの集積化に伴い、短チャネル効果を抑制するため、コンタクトの接合深さを浅くする必要性が増大している。このため、今まで以上に急峻かつ均一なコンタクト界面構造を形成することが、必須の課題となっている。また、自己整合型のコンタクトを形成することを目的として、ＴｉやＣｏなどのシリサイドを形成する金属が導入されてきた。しかしながら、ほとんどの金属の場合、シリサイド化の固相反応が不均一で、針状の金属結晶を形成したり、拡散層の結晶構造を乱すことによって、リーク電流が発生しやすくなるという問題があった。また、シリサイド自体が、コンタクト配線を構成する主たる金属であるＡｌと反応しやすく、特に粒界が多いシリサイド膜の場合には、６００℃以上のデバイス製造プロセスに耐える構造とするために、バリア膜を必要としていた。

【０００３】シリサイドが不均一に進行する理由の一つは、組成や結晶構造が異なる様々なシリサイドが存在することである。シリサイドを形成するほとんどの金属の場合、比較的低温でのシリサイド化反応では、生成自由エネルギーが比較的小さく、Ｓｉ組成の少ないシリサイド相が形成されるのに対し、比較的高温では、生成自由エネルギーが大きく、Ｓｉ組成の多い安定なシリサイド相に置き換わっていく。したがって、プロセス中のシリサイド化のための熱処理工程では、シリサイド結晶の核形成密度や、熱処理温度の上昇速度などに依存して、不均一なシリサイド薄膜が形成されてしまう。

【０００４】一方、均一なシリサイド形成としては、Ｓｉ（１１１）面上のＣｏ薄膜を熱処理することによって得られる、エピタキシャル$CoSi_2$膜の例がある。エピタキシャル膜が得られるのは、Ｓｉと$CoSi_2$が類似の結晶構造とほぼ同じ格子定数を持つこと、その（１１）界面がエネルギー的に安定であること、などによる。このようなエピタキシャル膜では粒界がほとんど存在せず、これを用いてコンタクトを形成すれば、熱処理による構造の変化が少ない、信頼性の極めて高いコンタクトが形成できる。

【０００５】しかし、半導体デバイスに通常用いられるＳｉ（１００）基板上にコンタクトを形成する場合には、固相反応の初期にＣｏＳｉなどの生成自由エネルギーの小さいシリサイド相ができるため、一様なエピタキシャル膜を得るのは難しい。そこで、Ｓｉ（１００）基板の場合には、Ｃｏ／Ｓｉ界面にＴｉ薄膜又はSiO_x薄膜をはさむことにより、熱処理初期でのＣｏ拡散及び固相反応を抑えて、Ｓｉ（１００）界面にエピタキシャル$CoSi_2$を形成する方法が提案されている。ところが、前者のＴｉ薄膜の場合には、膜厚の均一性が不十分であり（1991年、アプライド・フィジックス・レターズ、第58巻、1308ページ（Applied PhysicsLetters, vol. 58, p. 1308 (1991)）、後者のSiO_x薄膜の場合には、実用的なシリサイド膜厚が得られていなかった（1996年、アプライド・フィジックス・レターズ、第68巻、3461ページ（Applied Physics Letters, vol. 68, p. 3461(1996)）。

【０００６】

【発明が解決しようとする課題】第一の問題点は、Ｓｉ基板上に直接金属を堆積して、引き続く熱処理でシリサイド電極を形成する方法では、コンタクト面内で均一なシリサイド層が形成できないため、接合深さが５０ｎｍ以下の浅い接合を、信頼性を保ちながら形成することが難しいという点である。

【０００７】第二の問題点は、電極配線を構成する主たる金属であるＡｌがシリサイドと反応しやすく、バリア膜を必要とするため、コンタクト製造プロセスが複雑になるという点である。

【０００８】したがって、本発明の目的は、高速化デバイスに適したコンタクト構造を、高いバリア性・高いリーク電流耐性を維持しながら実現し、簡便なセルフアラインプロセスによって、高速・高集積な半導体装置を提供することにある。

【０００９】

【課題を解決するための手段】本発明のコンタクト構造の製造方法では、シリコン基板上のコンタクト開口部に、シリコンの直接窒化プロセスを用いて、窒化シリコン（SiN_x）薄膜を形成し、続いてＮｉ，Ｖ，Ｐｔ及びＰｄなどの、シリサイド化固相反応での拡散種が金属原子であるような金属を薄膜状に堆積し、熱処理工程によってコンタクト開口部にのみ、熱力学的に最も安定なシリサイド相のみからなるシリサイド電極を形成するものである。

【００１０】すなわち本発明は、シリサイド化固相反応での拡散種がＮｉ，Ｖ，Ｐｔ及びＰｄからなる群から選

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択される１種の金属原子であるシリサイドがＳｉ基板上に直接形成されてオーミックコンタクトを形成する半導体装置の製造方法において、Ｓｉ基板上に厚さ０．５～１．５ｎｍの窒化シリコン膜を形成する工程、前記拡散種の金属原子の薄膜を堆積する工程、及び熱処理によって拡散層にのみシリサイドを形成する工程とを有することを特徴とする、半導体装置の製造方法であり、更に該製造方法により製造される半導体装置の構造である。特に前記拡散種がＮｉであり、形成されるシリサイドがエピタキシャル$NiSi_2$である。また本発明は、シリサイド化固相反応での拡散種が金属原子であるシリサイドがＳｉ基板上に直接形成されてオーミックコンタクトを形成する半導体装置において、該シリサイドがＳｉ基板上に厚さ０．５～１．５ｎｍの窒化シリコン膜を形成した後に、該窒化シリコン膜上に堆積された前記拡散種の金属原子の薄膜から前記窒化シリコン膜を通して熱拡散により拡散した金属原子とのシリサイド化固相反応によるものであり、前記形成されたシリサイド上に窒化シリコン膜が残留していることを特徴とする半導体装置である。

【００１１】

【発明の実施の形態】シリサイド化固相反応での拡散種が金属原子であるシリサイドを形成する際に、前記拡散種の金属原子の薄膜と、Ｓｉ基板との間に、薄い窒化シリコン（SiN_x）膜をはさむことにより、熱処理初期におけ該金属原子の拡散を抑制し、十分な温度に達して初めて、生成自由エネルギーの最も大きいシリサイド相を生成させるようにすることができる。窒化シリコン膜としては、０．５～１．５ｎｍ、好ましくは０．５～１．０ｎｍ程度に形成するのが望ましい。０．５ｎｍ未満では厚さをコントロールすることが難しく、１．５ｎｍを超えると、拡散が遅くなりすぎて実用的ではない場合もある。また上記拡散種の金属の例としては、Ｎｉ、Ｖ、Ｐｔ、Ｐｄ、（参考例としてＣｏ）などがあるが、いずれも窒化物の生成自由エネルギーが小さく、SiN_x膜とほとんど反応しないため、膜厚換算で１０ｎｍ以上の該金属が拡散してもＳｉNx膜の構造は維持される。したがって、あらかじめSiN_x膜上に適当な膜厚の該金属薄膜を堆積しておけば、上記のような固相反応の後、該金属のシリサイド膜上にSiN_x膜が残留し、該残留したSiN_x膜が更にその上に堆積される主たる配線金属に対するバリア膜として働く。一方、シリサイド固相反応での拡散種がＳｉ原子であるような金属（Ｔｉ，Ｗ，Ｔａ，Ｍｏなど）の場合には、Ｓｉ基板との間に薄い窒化シリコン（ＳｉNx）層をはさんで熱処理を行っても、シリサイド層はSiN_x層より上方に形成されるため、低抵抗で良好なコンタクトは形成できない。

【００１２】特に、前記金属原子としてＣｏを用いた場合には、前述のように、$CoSi_2$とＳｉは、類似の結晶構造とほぼ同じ格子定数を有するため、$CoSi_2$膜とＳｉ基板との間にエピタキシャル関係が得られる。また、SiN_x膜中のＣｏ拡散速度は、金属中のそれに比べて極めて遅いため、中間層にＴｉ金属を用いた従来法の場合に比べて、一様で欠陥の少ない$CoSi_2$膜が得られるという利点がある。

【００１３】

【実施例】以下、実施例を参照して本発明を更に具体的に説明するが、本発明はこれらの実施例のみに限定されるものではない。

【００１４】実施例１（参考例）

本発明の実施の形態について図１を用いて詳細に説明する。図１は、本発明のコバルトシリサイド層を含む積層構造について、その形成方法の各工程を示す断面図である。

【００１５】清浄なＳｉ（１００）基板を、プラズマＣＶＤチャンバー内に搬送し、基板温度を３００℃に保ちながら、アンモニアガス雰囲気でプラズマを生成することにより、Ｓｉ基板１を直接窒化する。このような窒化法により得られる窒化シリコン膜２は、厚さがおよそ１ｎｍで、組成が化学量論比であるSi_3N_4に近いことが、Ｘ線光電子分光から確認できる。この表面に厚さ１５ｎｍのＣｏ薄膜３をスパッタ法により堆積する（図１（ａ））。続いてＡｒガス雰囲気中で、７５０℃、３０分の熱処理を行うことにより、表面のＣｏ薄膜３は完全にシリサイド化する。結晶性を断面透過電子顕微鏡を用いて高分解能で観察すると、基板のＳｉ結晶に格子整合して、（１００）方位に揃った$CoSi_2$結晶層４が観測される。界面は１～２原子層のレベルで平坦であり、膜厚も約２０ｎｍとほぼ均一である。最表面には、厚さ１～２ｎｍのアモルファス状の領域５が観測されるが、Ｘ線光電子分光による分析から、主にＳｉの窒化物からなる薄膜であることが確認できる（図１（ｂ））。この試料の表面上に、Ａｌ膜６を５０ｎｍ堆積した試料を作製し（図１（ｃ））、窒素雰囲気中での熱処理（５５０℃，６０分）を行っても、Ａｌ膜６と$CoSi_2$結晶層４との界面層の厚さが若干増加するものの、界面の平坦さは保たれ、$CoSi_2$上の窒化シリコン層５が界面反応を抑制する働きがあることが確認される。

【００１６】実施例２

本発明の他の実施形態について、図２を用いて詳細に説明する。図２は、本発明のニッケルシリサイド層を含むコンタクト構造について、その形成方法の各工程を示す一部断面図である。

【００１７】抵抗率が１０Ωｃｍのｎ，ｐ両タイプのＳｉ（１００）基板１を、厚さ３００ｎｍのSiO_2膜７で被覆し、直径１００ｍｍの円形の開口部を形成する。次に、この試料を真空槽中に搬送して基板温度を５００℃に保ち、高温フィラメントを通過させた窒素ガスビーム（原子状窒素を含む）を表面に照射する。このとき、開口部底面のＳｉ表面には厚さ１．０ｎｍの窒化膜２

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が、酸化膜７上にはＳｉＯＮ膜８が形成される。ここで、Ｓｉ上の窒化膜は化学量論比より窒素の含有量が少なく、組成がＳｉ：Ｎ＝１：１であるような膜である。同じ真空槽中で基板温度を５０℃に下げ、ＥＢガンを用いて平均膜厚２０ｎｍのＮｉ薄膜９を堆積する（図２（ａ））。次に、Ａｒ雰囲気中でRapid Thermal Annealing（ＲＴＡ）法により、７５０℃，３０秒の条件で急速加熱処理を施す。このとき、開口部底面のＮｉが消費されてＳｉとＮを主成分とする薄膜５の下に均一な厚さの$NiSi_2$層１０が形成される（図２（ｂ））。このシリサイド層１０は、基板の結晶構造を引き継いで（１００）配向となり、Ｓｉと$NiSi_2$の格子定数が非常に近いことから、界面は$CoSi_2$の場合と同様、エピタキシャル界面となる。ところどころに長さ１～２ｎｍの（１１１）面のファセットが存在する以外は、（１００）面に平行なフラット界面となる。ＳｉＮ膜を形成しないＳｉ／Ｎｉ界面に対して上記熱処理を行った場合には、界面は（１１１）面のファセットで覆われることから、ＳｉＮ膜をＳｉ／Ｎｉ界面にはさむという本発明が、フラット$NiSi_2$／Ｓｉ界面を得る上で顕著な効果を奏することが検証される。図２（ｂ）のコンタクト構造を有する基板を、塩酸を主成分とする酸混合液中で洗浄することにより、未反応のＮｉ層９を除去した後、厚さ２００ｎｍのＡｌ膜６を堆積して、リソグラフィープロセスにより、各コンタクトにそれぞれコンタクトパッドを形成する（図２（ｃ））。

【００１８】このようなコンタクトは、ショットキー接合ダイオードになっており、Ｉ－Ｖ法により障壁高さを測定できる。ｎ，ｐ基板の試料に対して、温度７７Ｋで測定した典型的な障壁高さはそれぞれ、０．４０ｅＶ，０．６５ｅＶとなった。両者の和が、Ｓｉのバンドギャップ１．１ｅＶに近いことから、コンタクト内の障壁高さ分布がほぼ均一であることが証明される。通常のＮｉSi_2／ｎ－Ｓｉでの障壁高さが約０．７ｅＶであるのに比べると、ｎ基板での障壁高さが著しく低い。このことは、ｎ基板への極めて低抵抗なオーミックコンタクトが本発明の手法によって実現できることを示している。

【００１９】実施例３

図３（ａ）～（ｄ）は、本発明の参考例としてのコバルトシリサイドコンタクトを含むＭＯＳ型トランジスタについて、その形成方法の各工程を示す、一部断面図である。図３（ａ）に示すように、半導体基板１上に素子分離領域１１を形成し、熱酸化によってゲート酸化膜１２を形成する。次いで、多結晶シリコンを堆積してパターニング工程により、多結晶シリコンゲート１３を形成する。ここで、低濃度のイオン注入で拡散層１４を形成した後、全面への酸化膜堆積とそれに引き続く異方性エッチングでサイドウォール１５を形成する。更に高濃度のイオン注入した後に熱処理を行って拡散層１４を形成することにより、ＬＤＤ構造となる。

【００２０】次に、コンタクト底部の自然酸化膜を希フッ酸で除去した後、基板をプラズマＣＶＤチャンバー内に搬送し、基板温度を３００℃に保ちながら、アンモニアガス雰囲気でプラズマを生成することにより、基板表面を窒化する。このとき、コンタクト底面のＳｉ表面には厚さ１．０ｎｍのＳｉＮ膜２で覆われ、このときフィールド酸化膜表面も窒化されて、ごく薄い酸窒化膜（ＳｉＯＮ）８となる。続いて、スパッタ法を用いて、試料全面に厚さ３０ｎｍのＣｏ薄膜３をスパッタする（図３（ｂ））。なお、図３（ｂ）では酸窒化膜８を模式的に示しているが、後に続く図３（ｃ）、（ｄ）では省略する。

【００２１】ここで、前記ＲＴＡ法により、７５０℃，６０秒の急速熱処理を行う。コンタクト部では、表面のＣｏが基板Ｓｉ中に拡散して、均一な厚さ（１５ｎｍ）の$CoSi_2$層４を形成する。ＳｉＮ層の存在によってコバルトの供給速度が抑えられているため、シリサイドは基板の結晶配向を反映した安定な結晶構造をとり、界面は原子オーダーで急峻かつ平坦で、Ｓｉ（１００）／$CoSi_2$（１００）のエピタキシャル関係が実現する。この時点で、ＳｉとＮを主成分とする薄膜５は$CoSi_2$層の直上に存在し、更にその上には未反応のＣｏ層３が残留している（図３（ｃ））。また、フィールド酸化膜をはじめとする、シリコン酸化膜上ではＣｏ層３はほぼそのまま残留している。

【００２２】次に、未反応のＣｏを除去するため、（硫酸）：（硝酸）：（リン酸）：（酢酸）＝１：１：４：４の混合溶液を用いて５０℃でエッチングを行う。以上の処理により、拡散層上に自己整合的に$CoSi_2$コンタクトを形成することができる（図３（ｄ））。

【００２３】電気特性を評価するため、同様の方法で得られたコンタクトにＡｌ配線を施し、$1\times1\ \mu m^2$のコンタクトが２０００個連なったコンタクトチェーンパターンを作製した。平均コンタクト抵抗は$1\times10^{-7}\ \Omega cm^2$程度であり、十分低い値が得られた。また水素雰囲気中で、５００℃，３０分の熱処理を行って電気測定を行ったが、抵抗はほとんど上昇せず、リーク電流も発生しなかった。

【００２４】本実施例では、参考例として、金属としてＣｏを用いた場合を説明したが、他の金属、例えばＮｉ，Ｖ，Ｐｔ，Ｐｄなどを用いても、安定なシリサイド相からなる一様な厚さコンタクトを形成することができる。これらの金属はいずれも、シリサイド化固相反応での拡散種となる金属であり、窒化物の生成自由エネルギーが比較的小さいためＳｉＮ膜との反応性が低いという特徴がある。

【００２５】また、Ｓｉ基板の窒化のプロセスには、アンモニアガスプラズマにさらす方法以外に、ＥＣＲで活性化したアンモニアガスや窒素ガスのビーム照射など、反応性の高い窒素原子に基板をさらす方法によっても同

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様の効果が得られる。

【００２６】

【発明の効果】第一の効果は、半導体装置の信頼性の向上が図られることである。その理由は、コンタクト面内で均一な厚さのシリサイド層がコンタクト界面に形成されるため、半導体装置の高性能化のために接合深さを５０ｎｍ以下に浅くしても、シリサイド化に伴う構造の乱れが局所的に接合界面にまで及ぶということがなく、リーク電流が発生しにくいためである。

【００２７】第二の効果は、半導体装置の製造工程を簡素化できることである。その理由は、シリサイド層の形成と同時に、シリサイド上に薄いSiN_x層が残留し、この層がコンタクトを構成する主たる金属であるＡｌやＷに対するバリア膜となるからである。

【図面の簡単な説明】

【図１】本発明のコバルトシリサイド層を含む積層構造について、その形成方法の各工程を示す断面図である。

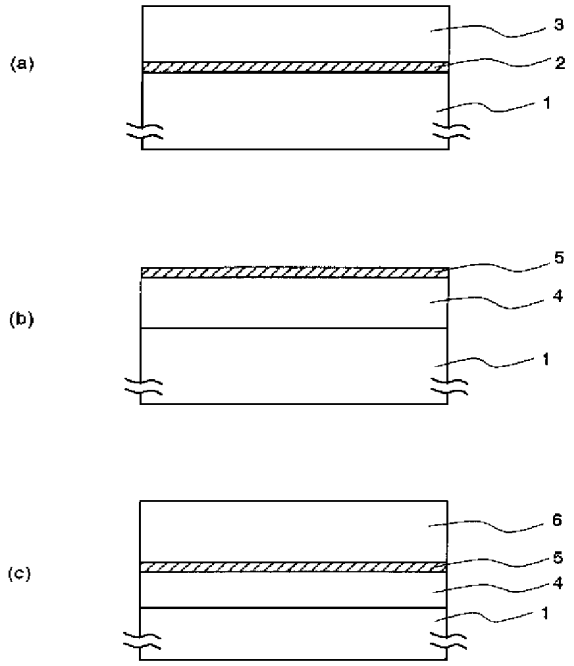
【図２】本発明のニッケルシリサイド層を含むコンタクト構造について、その形成方法の各工程を示す一部断面図である。

【図３】本発明のコバルトシリサイドコンタクトを含むＭＯＳ型トランジスタについて、その形成方法の各工程を示す、一部断面図である。

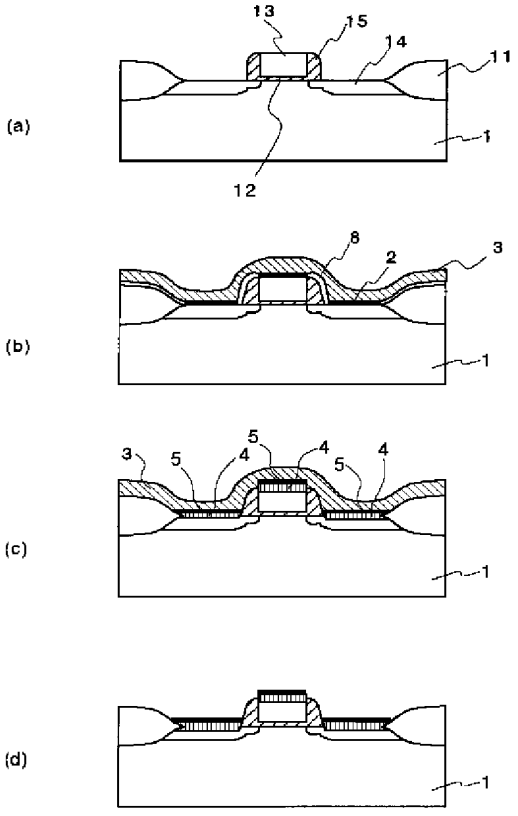
【符号の説明】

１　Ｓｉ（１００）半導体基板
２　シリコン窒化膜
３　Ｃｏ膜
４　$CoSi_2$膜
５　ＳｉとＮを主成分とする膜
６　Ａｌ膜
７　SiO_2層間膜
８　ＳｉＯＮ膜
９　Ｎｉ膜
１０　$NiSi_2$膜
１１　素子分離領域
１２　ゲート酸化膜
１３　多結晶シリコンゲート
１４　拡散層

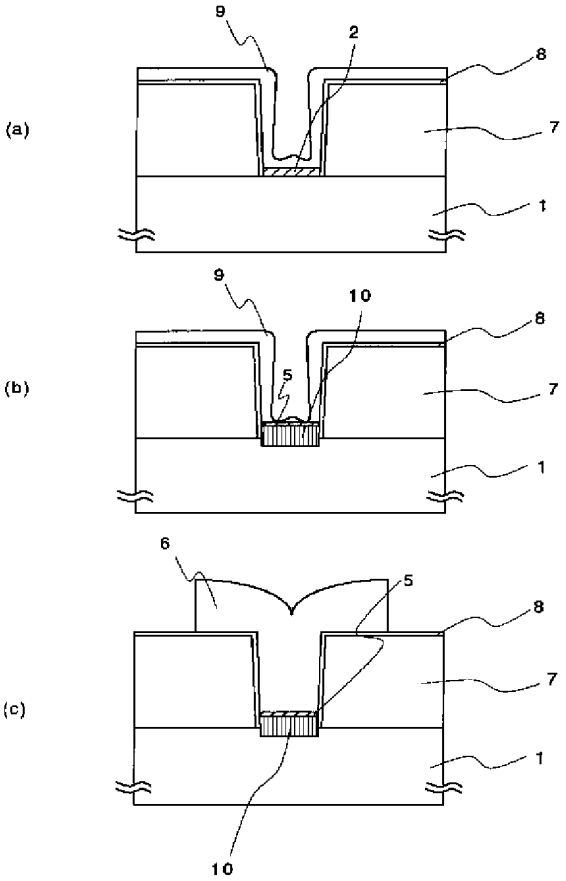
【図１】



【図３】



【図２】



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(58)調査した分野(Int.Cl.⁷，ＤＢ名)

H01L　21/28 - 21/288
H01L　21/44 - 21/445
H01L　29/40 - 29/43
H01L　29/47
H01L　29/872

Espacenet

JP3191728B2 SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Applicants: NEC CORP

Inventors: ISHIDA KOICHI,MIURA YOSHINAO

Classifications:

IPC ***H01L21/28; H01L21/285; H01L21/336; H01L21/768; H01L29/78;*** (IPC1-7): H01L21/28; H01L21/336; H01L29/78;

CPC **H01L21/28518 (EP); H01L21/28537 (EP); H01L21/76814 (EP); H01L21/76831 (EP); H01L21/76877 (EP);**

Priorities: JP16608797A 1997-06-23

Application: JP3191728B2·1997-06-23

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SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Abstract

PROBLEM TO BE SOLVED: To provide a semiconductor device having a silicide contact of a uniform thickness which is formed on a Si substrate with a large and constant generation of free energy. SOLUTION: When a semiconductor device in which an ohmic contact is formed by forming silicide directly on a Si substrate with atoms of metal as diffusion seeds for silicidation solid phase reaction in this method, first, a silicon nitride film 2 which is 0.5-1.5 nm thick is formed on a Si substrate 1. Then, a thin film of atoms of metal as above-mentioned diffusion seeds is deposited. After that, silicide 4 is formed only on the diffusion layer by heat treatment.

Semiconductor device and manufacturing method thereof

Classifications

H01L21/28518 Deposition of conductive or insulating materials for electrodes conducting electric current from a gas or vapour, e.g. condensation of conductive layers on semiconductor bodies comprising elements of Group IV of the Periodic System the conductive layers comprising silicides

View 4 more classifications

JP3191728B2

Japan

Find Prior Art Similar

Other languages: Japanese

Inventor: 嘉嘉 三浦, 宏一 石田

Worldwide applications

1997 JP 2000 US

Application JP16608797A events

1997-06-23	Application filed by 日本電気株式会社
1997-06-23	Priority to JP16608797A
1999-01-22	Publication of JPH11168053A
2001-07-23	Application granted
2001-07-23	Publication of JP3191728B2
2017-06-23	Anticipated expiration
Status	Expired - Lifetime

Info: Patent citations (14), Cited by (18), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (6)

Hide Dependent

(57) [Claims]

1. The method according to claim 1, wherein the diffusion species in the silicidation solid phase reaction is N.
In a method of manufacturing a semiconductor device in which silicide, which is one kind of metal atom selected from the group consisting of i, V, Pt, and Pd, is formed directly on a Si substrate to form an ohmic contact, A step of forming a silicon nitride film having a thickness of 1.5 to 1.5 nm, a step of depositing a thin film of the metal atom of the diffusion type, and a step of forming a silicide of the metal atom only in the diffusion layer by heat treatment. A method for manufacturing a semiconductor device.

2. The method according to claim 1, wherein the diffusion species in the silicidation solid phase reaction is Ni.
And epitaxial heat treatment only for the diffusion layer by heat treatment.
The method according to claim 1, wherein Si_2 is formed.

3. The method according to claim 1, wherein the diffusion species in the silicidation solid phase reaction is N.
In a semiconductor device in which silicide, which is one kind of metal atom selected from the group consisting of i, V, Pt and Pd, is directly formed on a Si substrate to form an ohmic contact, the silicide has a thickness of 0 on the Si substrate. 0.5-1.5n
m, after forming a silicon nitride film of m by a silicidation solid-phase reaction with metal atoms diffused by thermal diffusion from the thin film of the metal atoms of the diffusion species deposited on the silicon nitride film through the silicon nitride film. A semiconductor device, comprising:

4. The method according to claim 1, wherein the diffusion species in the silicidation solid phase reaction is Ni.
And only the epitaxial N
4. The semiconductor device according to claim 3, wherein iSi_2 is formed.

5. The method according to claim 1, wherein the diffusion species in the silicidation solid phase reaction is N.
In a semiconductor device in which silicide, which is one kind of metal atom selected from the group consisting of i, V, Pt and Pd, is directly formed on a Si substrate to form an ohmic contact, the silicide is formed on the Si substrate. 0.5 to 1.5n thick
m, after forming a silicon nitride film of m by a silicidation solid-phase reaction with metal atoms diffused by thermal diffusion from the thin film of the metal atoms of the diffusion species deposited on the silicon nitride film through the silicon nitride film. Wherein a silicon nitride film remains on the formed silicide.

6. The metal atom serving as the diffusion species is Ni.
And the silicide formed is epitaxial $NiSi_2$
6. The semiconductor device according to claim 5, wherein

Description

DETAILED DESCRIPTION OF THE INVENTION

[0001]

The present invention relates to a method for forming a silicide electrode on a Si substrate and a structure of a semiconductor device manufactured by the method in a method for manufacturing a semiconductor device.

[0002]

2. Description of the Related Art With the recent integration of devices, the need to reduce the junction depth of contacts has been increasing in order to suppress the short channel effect. Therefore, it is essential to form a steep and uniform contact interface structure more than ever. Further, for the purpose of forming a self-aligned contact, a metal for forming a silicide such as Ti or Co has been introduced. However,
In the case of most metals, there is a problem that a solid-state reaction of silicidation is not uniform, and a needle-like metal crystal is formed or a crystal structure of a diffusion layer is disturbed, so that a leak current is easily generated. Further, the silicide itself easily reacts with Al which is a main metal constituting the contact wiring. In order to have a structure that can withstand the above device manufacturing process, a barrier film is required.

One of the reasons why the silicide proceeds unevenly is that various silicides having different compositions and different crystal structures exist. In the case of most metals that form silicide, the silicidation reaction at a relatively low temperature results in a relatively small free energy of formation and a silicide phase with a small Si composition, whereas at a relatively high temperature, the free energy of formation is relatively low. is replaced by a stable silicide phase having a large Si composition. Therefore, in the heat treatment step for silicidation during the process, a non-uniform silicide thin film is formed depending on the nucleation density of the silicide crystal, the rate of increase in the heat treatment temperature, and the like.

On the other hand, in order to form a uniform silicide, S
There is an example of an epitaxial $CoSi_2$ film obtained by heat-treating a Co thin film on the i (111) plane. An epitaxial film is obtained because Si and $CoSi_2$ have almost the same lattice constant as a similar crystal structure.
11) The interface is energetically stable. In such an epitaxial film, there is almost no grain boundary, and if a contact is formed using this, a highly reliable contact with little structural change due to heat treatment can be formed.

However, when a contact is formed on a Si (100) substrate usually used for a semiconductor device, a uniform silicide phase having a low free energy of formation, such as CoSi, is formed at an early stage of a solid-phase reaction. It is difficult to get a film. Therefore, in the case of a Si (100) substrate, a Ti thin film or SiO_x is formed at the Co / Si interface.
There has been proposed a method of forming epitaxial $CoSi_2$ at the Si (100) interface by sandwiching a thin film to suppress Co diffusion and a solid phase reaction at an early stage of heat treatment. However, in the case of the former Ti thin film, the uniformity of the film thickness is insufficient (1991, Applied Physics Letters, Vol. 58, p. 1308 (Applied Physics Letters, vo
l. 58, p. 1308 (1991)), in the case of the latter SiO_x thin film, a practical silicide film thickness was not obtained (1996, Applied Physics Letters, No. 68).
Volume, p. 3461 (Applied Physics Letters, vol. 68,
p. 3461 (1996)).

[0006]

The first problem is that Si
In a method in which a metal is directly deposited on a substrate and a silicide electrode is formed by a subsequent heat treatment, a uniform silicide layer cannot be formed in the contact surface.
The point is that it is difficult to form the following shallow junction while maintaining reliability.

The second problem is that Al, which is a main metal constituting the electrode wiring, easily reacts with silicide and requires a barrier film, which complicates the contact manufacturing process.

Therefore, an object of the present invention is to realize a contact structure suitable for a high-speed device while maintaining high barrier properties and high leakage current resistance, and to realize a high-speed and highly integrated semiconductor device by a simple self-alignment process. Is to provide.

[0009]

According to a method of manufacturing a contact structure of the present invention, a silicon nitride (SiN_x) thin film is formed in a contact opening on a silicon substrate by using a direct nitridation process of silicon. Ni, V, Pt and
Such as fine Pd, a metal such as diffusing species in silicidation solid phase reaction is a metal atom is deposited as a thin film, only the contact opening by a heat treatment step, only the most thermodynamically stable silicide phases is formed.

That is, according to the present invention, the silicide, in which the diffusion species in the silicidation solid phase reaction is one kind of metal atom selected from the group consisting of Ni, V, Pt and Pd, is formed directly on the Si substrate, In a method of manufacturing a semiconductor device for forming a contact, a thickness of 0.5 to
Manufacturing a semiconductor device, comprising: forming a 1.5-nm silicon nitride film, depositing a thin film of metal atoms of the diffusion type, and forming silicide only in the diffusion layer by heat treatment. And a structure of a semiconductor device manufactured by the manufacturing method. In particular the diffusing species is Ni, silicide formed is epitaxial $NiSi_2$. The present invention also provides a semiconductor device in which a silicide in which a diffusion species in a silicidation solid phase reaction is a metal atom is directly formed on a Si substrate to form an ohmic contact, wherein the silicide has a thickness of 0.5 mm on the Si substrate. After forming a silicon nitride film having a thickness of about 1.5 nm, a silicidation solid-phase reaction with a metal atom diffused by thermal diffusion from the thin film of the metal atom of the diffusion type deposited on the silicon nitride film through the silicon nitride film Wherein the silicon nitride film remains on the formed silicide.

[0011]

DESCRIPTION OF THE PREFERRED EMBODIMENTS In forming a silicide in which a diffusion species in a silicidation solid phase reaction is a metal atom, a thin silicon nitride (SiN) film is provided between a thin film of the metal atom of the diffusion species and a Si substrate. $_x$) By sandwiching the film, the diffusion of the metal

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atoms can be suppressed in the early stage of the heat treatment, and the silicide phase having the largest free energy of formation can be generated only when the temperature reaches a sufficient temperature. As a silicon nitride film, 0.5 to 1.5 nm, preferably 0.5 to 1.5 nm
It is desirable to form it to about 1.0 nm. If the thickness is less than 0.5 nm, it is difficult to control the thickness.
If m is exceeded, diffusion may be too slow to be practical. Examples of the diffusion metal include Ni,
V, Pt, Pd, (Co for reference), etc.
In each case, the free energy of formation of nitride is small, and SiN
Since it hardly reacts with the x film, the structure of the SiNx film is maintained even if the metal having a thickness of 10 nm or more is diffused. Therefore, if depositing the metal thin film of suitable thickness on the previously the SiN_x film, after the solid-phase reaction as described above, the SiN_x film on the silicide film of the metal may remain,
The remaining SiN_x film functions as a barrier film for a main wiring metal further deposited thereon. On the other hand, for a metal (T
(i, W, Ta, Mo, etc.), the silicide layer is formed above the SiN_x layer even if heat treatment is performed with a thin silicon nitride (SiN x) layer interposed between the Si substrate and the Si substrate. A good contact cannot be formed with low resistance.

[0012] Particularly, when using Co as the metal atom, as described above, $CoSi_2$ and Si, because it has almost the same lattice constant similar to the crystal structure, between the $CoSi_2$ film and the Si substrate To obtain an epitaxial relationship. Further, since the Co diffusion rate in the SiN_x film is extremely slow as compared with that in the metal, a $CoSi_2$ film with less defects and uniformity can be obtained as compared with the conventional method using Ti metal for the intermediate layer. There is an advantage.

[0013]

EXAMPLES Hereinafter, the present invention will be described more specifically with reference to examples, but the present invention is not limited to only these examples.

Embodiment 1(Reference example) An embodiment of the present invention will be described in detail with reference to FIG.
You. FIG. 1 shows a laminate including a cobalt silicide layer of the present invention.
FIG. 4 is a cross-sectional view showing each step of a method for forming the structure.
You.

A clean Si (100) substrate is treated with plasma C
The substrate is transported into the VD chamber, and plasma is generated in an ammonia gas atmosphere while maintaining the substrate temperature at 300 ° C., thereby directly nitriding the Si substrate 1. The silicon nitride film 2 obtained by such a nitriding method has a thickness of about 1
It can be confirmed by X-ray photoelectron spectroscopy that the composition in nm is close to the stoichiometric ratio of Si_3N_4. Thickness 1 on this surface
A 5 nm Co thin film 3 is deposited by a sputtering method (FIG. 1).
(A)). Subsequently, at 750 ° C. and 30 ° C. in an Ar gas atmosphere.
By performing the heat treatment for minutes, the Co thin film 3 on the surface is completely silicided. When the crystallinity is observed at a high resolution using a cross-sectional transmission electron microscope, a $CoSi_2$ crystal layer 4 that is lattice-matched to the Si crystal of the substrate and aligned in the (100) direction is observed. The interface is flat at the level of one to two atomic layers,
The film thickness is also approximately uniform at about 20 nm. On the outermost surface, an amorphous region 5 having a thickness of 1 to 2 nm is observed,
From analysis by X-ray photoelectron spectroscopy, it can be confirmed that the thin film is mainly composed of Si nitride (FIG. 1B). A sample in which an Al film 6 was deposited to a thickness of 50 nm on the surface of this sample was prepared (FIG. 1C), and a heat treatment (550) in a nitrogen atmosphere was performed.
(° C., 60 minutes), although the thickness of the interface layer between the Al film 6 and the $CoSi_2$ crystal layer 4 slightly increases, the flatness of the interface is maintained, and the silicon nitride layer 5 on $CoSi_2$ it is confirmed that it has a function of suppressing the reaction.

Embodiment 2 Another embodiment of the present invention will be described in detail with reference to FIG. FIG. 2 is a partial cross-sectional view showing each step of a method for forming a contact structure including a nickel silicide layer of the present invention.

Both n and p type S having a resistivity of 10 Ωcm
An i (100) substrate 1 is coated with a SiO_2 film 7 having a thickness of 300 nm.
To form a circular opening having a diameter of 100 mm.
Next, the sample is transferred into a vacuum chamber and the substrate temperature is set to 500.
The surface is irradiated with a nitrogen gas beam (including atomic nitrogen) passed through a high-temperature filament while maintaining the temperature. At this time,
A 1.0 nm thick nitride film 2 is formed on the Si surface at the bottom of the opening.
However, an SiON film 8 is formed on the oxide film 7. Here, the nitride film on Si is a film whose nitrogen content is smaller than the stoichiometric ratio and whose composition is Si: N = 1: 1.
The substrate temperature was lowered to 50 ° C. in the same vacuum chamber, and a Ni thin film 9 having an average film thickness of 20 nm was deposited using an EB gun (FIG. 2).
(A)). Next, Rapid Thermal Anneal in Ar atmosphere
A rapid heating treatment is performed by ing (RTA) at 750 ° C. for 30 seconds. At this time, Ni on the bottom surface of the opening is consumed, and a $NiSi_2$ layer 10 having a uniform thickness is formed under the thin film 5 containing Si and N as main components (FIG. 2B). This silicide layer 10 inherits the crystal structure of the substrate (1
00) and the lattice constants of Si and $NiSi_2$ are very close, so that the interface is an epitaxial interface as in the case of $CoSi_2$. Somewhere 1-2 nm in length
(10) except that a facet of the (111) plane of
0) It becomes a flat interface parallel to the plane. When the above heat treatment is performed on the Si / Ni interface where no SiN film is formed, the interface is covered with facets of the (111) plane. It is verified that a remarkable effect is obtained in obtaining the $NiSi_2$ / Si interface. After removing the unreacted Ni layer 9 by washing the substrate having the contact structure of FIG. 2B in an acid mixture containing hydrochloric acid as a main component,
An Al film 6 having a thickness of 200 nm is deposited, and a contact pad is formed on each contact by a lithography process (FIG. 2C).

Such a contact is a Schottky junction diode, and the height of the barrier can be measured by the IV method. Typical barrier heights measured at 77K for the n and p substrate samples are 0.40 eV,
It became 0.65 eV. Since the sum of the two is close to the band gap of Si of 1.1 eV, it is proved that the barrier height distribution in the contact is substantially uniform. Normal Ni
The barrier height on the n-substrate is significantly lower than the barrier height on Si_2 / n-Si of about 0.7 eV. This indicates that an ohmic contact with extremely low

resistance to the n-substrate can be realized by the method of the present invention.

Embodiment 3 FIGS. 3A to 3D show steps of a method of forming a MOS transistor including a cobalt silicide contact as a reference example of the present invention. It is sectional drawing. As shown in FIG. 3A, an element isolation region 11 is formed on a semiconductor substrate 1, and a gate oxide film 12 is formed by thermal oxidation.
To form Next, polycrystalline silicon is deposited and a polycrystalline silicon gate 13 is formed by a patterning process. Here, after the diffusion layer 14 is formed by low-concentration ion implantation, a sidewall 15 is formed by depositing an oxide film on the entire surface and subsequently performing anisotropic etching. Further, a heat treatment is performed after high-concentration ion implantation to form the diffusion layer 14, whereby an LDD structure is obtained.

Next, after removing the natural oxide film at the bottom of the contact with dilute hydrofluoric acid, the substrate is transferred into a plasma CVD chamber, and plasma is generated in an ammonia gas atmosphere while maintaining the substrate temperature at 300 ° C. Then, the substrate surface is nitrided. At this time, the Si surface on the bottom surface of the contact is covered with a SiN film 2 having a thickness of 1.0 nm. At this time, the surface of the field oxide film is also nitrided, and a very thin oxynitride film (S
iON) 8. Subsequently, a 30 nm-thick Co thin film 3 is sputtered on the entire surface of the sample by using a sputtering method (FIG. 3).
(B)). Although FIG. 3B schematically shows the oxynitride film 8, it is omitted in the subsequent FIGS. 3C and 3D.

Here, at 750.degree.
A rapid heat treatment for 60 seconds is performed. In the contact portion, Co on the surface diffuses into the substrate Si to form a uniform thickness (15 nm).
To form a $CoSi_2$ layer 4. Since the supply rate of cobalt is suppressed by the presence of the SiN layer, the silicide has a stable crystal structure reflecting the crystal orientation of the substrate, the interface is steep and flat in the atomic order, and the Si (100) /
An epitaxial relationship of $CoSi_2$ (100) is realized. At this point, the thin film 5 containing Si and N as main components is Co
Exists directly on the Si_2 layer, and further unreacted Co
The layer 3 remains (FIG. 3C). In addition, a Co layer 3 is formed on the silicon oxide film including the field oxide film.
Remains almost intact.

Next, to remove unreacted Co, (sulfuric acid) :(nitric acid) :(phosphoric acid) :(acetic acid) = 1: 1: 4:
Etching is performed at 50 ° C. using the mixed solution of No. 4. With the above processing, a $CoSi_2$ contact can be formed on the diffusion layer in a self-aligned manner (FIG. 3D).

In order to evaluate the electrical characteristics, Al contacts were formed on the contacts obtained in the same manner, and a contact chain pattern in which 2000 1 × 1 μm^2 contacts were formed was prepared. Average contact resistance is 1×10^{-7} Ωc
m^2, and a sufficiently low value was obtained. In addition, electrical measurement was performed by performing a heat treatment at 500 ° C. for 30 minutes in a hydrogen atmosphere. As a result, the resistance hardly increased and no leak current occurred.

In this embodiment, as a reference example,
Although the case where Co is used has been described , other metals such as N
Even if i, V, Pt, Pd, or the like is used, a uniform thickness contact made of a stable silicide phase can be formed. Each of these metals is a metal that becomes a diffusion species in the silicidation solid-phase reaction, and has a characteristic that the reactivity with the SiN film is low because the free energy of formation of nitride is relatively small.

In the process of nitriding the Si substrate, in addition to the method of exposing to the ammonia gas plasma, a beam irradiation of ammonia gas or nitrogen gas activated by ECR may be used.
A similar effect can be obtained by exposing the substrate to highly reactive nitrogen atoms.

[0026]

The first effect is that the reliability of the semiconductor device is improved. The reason is that a silicide layer having a uniform thickness is formed at the contact interface within the contact surface.
This is because even if the thickness is reduced to 0 nm or less, the disorder of the structure due to silicidation does not locally reach the junction interface, and a leak current hardly occurs.

The second effect is that the manufacturing process of the semiconductor device can be simplified. The reason is that, simultaneously with the formation of the silicide layer, a thin SiN_x layer remains on the silicide,
This is because this layer becomes a barrier film for Al and W which are the main metals constituting the contact.

[Brief description of the drawings]

FIG. 1 is a cross-sectional view showing each step of a method for forming a laminated structure including a cobalt silicide layer of the present invention.

FIG. 2 is a partial cross-sectional view showing each step of a method for forming a contact structure including a nickel silicide layer of the present invention.

FIG. 3 is a partial cross-sectional view showing each step of a method for forming a MOS transistor including a cobalt silicide contact of the present invention.

[Explanation of symbols]

DESCRIPTION OF SYMBOLS 1 Si (100) semiconductor substrate 2 Silicon nitride film 3 Co film 4 $CoSi_2$ film 5 Film containing Si and N as main components 6 Al film 7 SiO_2 interlayer film 8 SiON film 9 Ni film 10 $NiSi_2$ film 11 Element isolation region 12 gate oxide film 13 polycrystalline silicon gate 14 diffusion layer

----------続き Continued on the front page (58) Field surveyed
(Int.Cl. ^{7} , DB name) H01L 21/28-21/288 H01L 21/44-21/445 H01L 29/40-29/43 H01L 29 / 47 H01L 29/872

Patent Citations (14)

Publication number	Priority date	Publication date	Assignee	Title

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Family To Family Citations				
US4707197A	1984-08-02	1987-11-17	American Telephone And Telegraph Company, At&T Bell Laboratories	Method of producing a silicide/Si heteroepitaxial structure, and articles produced by the method
EP0183995B1	1984-11-02	1989-08-16	Hitachi, Ltd.	Semiconductor device having a polycrystalline silicon interconnection layer and method for its manufacture
US4814294A	1987-07-30	1989-03-21	Allied-Signal Inc.	Method of growing cobalt silicide films by chemical vapor deposition
JPH02162722A *	1988-12-16	1990-06-22	Nippon Telegr & Teleph Corp <Ntt>	Manufacture of semiconductor device
US5323053A	1992-05-28	1994-06-21	At&T Bell Laboratories	Semiconductor devices using epitaxial silicides on (111) surfaces etched in (100) silicon substrates
JP3262676B2	1993-06-25	2002-03-04	株式会社リコー	Semiconductor device
US5652180A *	1993-06-28	1997-07-29	Kawasaki Steel Corporation	Method of manufacturing semiconductor device with contact structure
US5430328A	1994-05-31	1995-07-04	United Microelectronics Corporation	Process for self-align contact
JP2586345B2 *	1994-10-14	1997-02-26	日本電気株式会社	Semiconductor device comprising cobalt silicide film and method of manufacturing the device
JPH098297A	1995-06-26	1997-01-10	Mitsubishi Electric Corp	Semiconductor device, manufacture thereof and field-effect transistor
US5861340A	1996-02-15	1999-01-19	Intel Corporation	Method of forming a polycide film
JPH10335265A	1997-05-27	1998-12-18	Sony Corp	Manufacture of semiconductor device
US5973372A	1997-12-06	1999-10-26	Omid-Zohoor; Farrokh	Silicided shallow junction transistor formation and structure with high and low breakdown voltages
US6229216B1 *	1998-03-24	2001-05-08	Rohm Co., Ltd.	Semiconductor device and method of manufacturing the same

* Cited by examiner, † Cited by third party

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Publication number	Priority date	Publication date	Assignee	Title
Family To Family Citations				
US7037371B1 *	1999-10-04	2006-05-02	Matsushita Electric Industrial Co., Ltd.	Method for fabricating semiconductor device
US6989854B2 *	2000-11-29	2006-05-10	Chartered Semiconductor Manufacturing, Inc.	Method and apparatus for performing nickel salicidation
US6468900B1 *	2000-12-06	2002-10-22	Advanced Micro Devices, Inc.	Dual layer nickel deposition using a cobalt barrier to reduce surface roughness at silicide/junction interface
US6730616B2 *	2001-09-24	2004-05-04	Texas Instruments Incorporated	Versatile plasma processing system for producing oxidation resistant barriers
SG120865A1 *	2002-04-03	2006-04-26	Univ Singapore	Method of forming epitaxial metal silicide for a semiconductor device
JP2005530344A *	2002-06-12	2005-10-06	アプライドマテリアルズインコーポレイテッド Applied Materials, Incorporated	A method to improve nitrogen profile in plasma nitrided gate dielectric layers
US7067439B2 *	2002-06-14	2006-06-27	Applied Materials, Inc.	ALD metal oxide deposition process using direct oxidation
US6878624B1 *	2003-09-30	2005-04-12	International Business Machines Corporation	Pre-anneal of CoSi, to prevent formation of amorphous layer between Ti-O-N and CoSi
US8119210B2 *	2004-05-21	2012-02-21	Applied Materials, Inc.	Formation of a silicon oxynitride layer on a high-k dielectric material
JP5116003B2 *	2006-02-27	2013-01-09	セイコーエプソン株式会社	Method for forming silicide and method for manufacturing semiconductor device
US7678710B2	2006-03-09	2010-03-16	Applied Materials, Inc.	Method and apparatus for fabricating a high dielectric constant transistor gate using a low energy plasma system
US7833938B2 *	2006-03-09	2010-11-23	Applied Materials, Inc.	Method of fabricating a high dielectric constant transistor gate using a low energy plasma apparatus

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JP6398744B2 *	2015-01-23	2018-10-03	三菱電機株式会社	Manufacturing method of substrate for semiconductor device
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* Cited by examiner, † Cited by third party, ‡ Family to family citation

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US5736461A	1998-04-07	Self-aligned cobalt silicide on MOS integrated circuits
US5324974A	1994-06-28	Nitride capped MOSFET for integrated circuits
JP2921889B2	1999-07-19	Method for manufacturing semiconductor device
DE19950708C2	2002-10-02	Process for forming self-aligning cobalt silicide layers with locally different layer thicknesses
US6620719B1	2003-09-16	Method of forming ohmic contacts using a self doping layer for thin-film transistors
US6255702B1	2001-07-03	Semiconductor device having junction depths for reducing short channel effect
JP3393731B2	2003-04-07	Semiconductor device and method of forming the same
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JP2978736B2	1999-11-15	Method for manufacturing semiconductor device
JP3600399B2	2004-12-15	Fabrication process for devices with thin layers of cobalt silicide
DE19505947B4	2006-04-06	Semiconductor device with improved barrier metal layer in an electrode or wiring layer
US7015126B2	2006-03-21	Method of forming silicided gate structure
US5767004A	1998-06-16	Method for forming a low impurity diffusion polysilicon layer
US6952040B2	2005-10-04	Transistor structure and method of fabrication
US7111959B2	2006-10-03	Method of forming metal/high-k gate stacks with high mobility
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KR100204083B1	1999-06-15	Tasin oxygen diffusion barrier in multilayer structure
US6800543B2	2004-10-05	Semiconductor device having a low-resistance gate electrode
JP5511889B2	2014-06-04	Method for forming a semiconductor structure including a TiC film
US6228779B1	2001-05-08	Ultra thin oxynitride and nitride/oxide stacked gate dielectrics fabricated by high pressure technology

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
JP16608797A	1997-06-23	1997-06-23	Semiconductor device and manufacturing method thereof

Applications Claiming Priority (2)

Application	Filing date	Title
JP16608797A	1997-06-23	Semiconductor device and manufacturing method thereof
US09/598,502	2000-06-22	Semiconductor device with silicide contact structure and fabrication method thereof

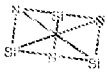
Legal Events

Date	Code	Title	Description
2008-05-07	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20090525 **Year of fee payment**: 8
2009-05-07	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20100525 **Year of fee payment**: 9
2010-05-11	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20110525 **Year of fee payment**: 10
2010-07-01	S111	Request for change of ownership or part of ownership	**Free format text**: JAPANESE INTERMEDIATE CODE: R313113
2010-07-09	R371	Transfer withdrawn	**Free format text**: JAPANESE INTERMEDIATE CODE: R371
2010-07-09	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20110525 **Year of fee payment**: 10
2010-07-16	S111	Request for change of ownership or part of ownership	**Free format text**: JAPANESE INTERMEDIATE CODE: R313113
2010-07-16	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20110525 **Year of fee payment**: 10
2010-07-27	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20110525 **Year of fee payment**: 10
2010-07-27	R350	Written notification of registration of transfer	**Free format text**: JAPANESE INTERMEDIATE CODE: R350
2011-04-12	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20120525 **Year of fee payment**: 11
2012-03-29	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20120525 **Year of fee payment**: 11
2012-04-03	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20130525 **Year of fee payment**: 12
2013-03-12	FPAY	Renewal fee payment (event date is renewal date of database)	**Free format text**: PAYMENT UNTIL: 20140525 **Year of fee payment**: 13
2015-09-10	S531	Written request for registration of change of domicile	**Free format text**: JAPANESE INTERMEDIATE CODE: R313531
2015-09-18	R350	Written notification of registration of transfer	**Free format text**: JAPANESE INTERMEDIATE CODE: R350
2017-06-23	EXPY	Cancellation because of completion of term	

Concepts

machine-extracted

Download Filter table

Name	Image	Sections	Count	Query match
semiconductor		title,claims,description	20	0.000
manufacturing process		title,description	5	0.000
films		claims,description	68	0.000
silicides		claims,description	45	0.000
silicide(4-)	Si^{-4}	claims,description	44	0.000
metal		claims,description	40	0.000
metals		claims,description	40	0.000
substrates		claims,description	39	0.000
Si3N4		claims,description	34	0.000
Silicon nitride		claims,description	34	0.000
layers		claims,description	34	0.000
thin films		claims,description	22	0.000
atoms		claims,description	20	0.000
heat treatment		claims,description	20	0.000
solid phase reaction		claims,description	17	0.000
nickel		claims,description	13	0.000
deposition		claims,description	4	0.000

Show all concepts from the description section

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(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号
特開2000－174261
（P2000－174261A）
(43)公開日　平成12年６月23日(2000.6.23)

(51)Int.Cl.[7]	識別記号	ＦＩ		テーマコード（参考）
Ｈ０１Ｌ　29/778		Ｈ０１Ｌ　29/80	Ｈ	５Ｆ００３
21/338		29/72		５Ｆ０４０
29/812		29/78	３０１Ｂ	５Ｆ１０２
21/331				
29/73				

審査請求　未請求　請求項の数７　ＯＬ　（全 13 頁）　最終頁に続く

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(71)出願人　000005223
富士通株式会社
神奈川県川崎市中原区上小田中４丁目１番１号

(72)発明者　高橋　剛
神奈川県川崎市中原区上小田中４丁目１番１号　富士通株式会社内

(72)発明者　岡本　直哉
神奈川県川崎市中原区上小田中４丁目１番１号　富士通株式会社内

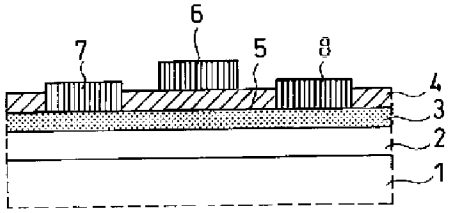
(74)代理人　100072833
弁理士　柏谷　昭司　（外２名）

最終頁に続く

(54)【発明の名称】　化合物半導体装置

(57)【要約】
【課題】　化合物半導体装置に関し、化合物半導体におけるピンニング効果の解除、界面準位密度の低減、及び、オーミック抵抗の低減を簡単な製造装置構成によって行う。
【解決手段】　化合物半導体層２の表面を、２原子層以上の厚さの少なくともＧａＳを含む層３で覆うとともに、少なくともＧａＳを含む層３の少なくも一部をＧａＮ層４で覆う。

本発明の原理的構成の説明図



１：半絶縁性化合物半導体基板
２：化合物半導体層
３：少なくともＧａＳを含む層
４：ＧａＮ層
５：ゲート絶縁膜
６：ゲート電極
７：ソース電極
８：ドレイン電極

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【特許請求の範囲】
【請求項１】　化合物半導体層の表面を、２原子層以上の厚さの少なくともＧａＳを含む層で覆うと共に、前記少なくともＧａＳを含む層の少なくとも一部をＧａＮ層で覆ったことを特徴とする化合物半導体層。
【請求項２】　上記ＧａＮ層を、少なくともＧａＳを含む層でさらに被覆したことを特徴とする請求項１記載の化合物半導体装置。
【請求項３】　上記ＧａＮ層を、少なくともＧａＳを含む層でさらに被覆すると共に、前記少なくともＧａＳを含む層の表面をＧａＮ層でさらに被覆したことを特徴とする請求項１記載の化合物半導体装置。
【請求項４】　上記少なくともＧａＳを含む層に接する化合物半導体層が、III-V族化合物半導体層であることを特徴とする請求項１乃至３のいずれか１項に記載の化合物半導体装置。
【請求項５】　少なくとも一つのオーミック電極を、上記化合物半導体層に接する少なくともＧａＳを含む層に接するように設けたことを特徴とする請求項１乃至４のいずれか１項に記載の化合物半導体装置。
【請求項６】　少なくとも一つのオーミック電極を、上記化合物半導体層に接する少なくともＧａＳを含む層を覆うＧａＮ層に接するように設けたことを特徴とする請求項１乃至４のいずれか１項に記載の化合物半導体装置。
【請求項７】　上記ＧａＮ層の内の最上層の表面に非オーミック電極を設けて、金属－絶縁体－半導体構造を構成したことを特徴とする請求項５または６に記載の化合物半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は化合物半導体装置に関するものであり、特に、化合物半導体ＭＩＳＦＥＴ等における界面準位密度を低減させるとともに、コンタクト抵抗を低減するための界面保護膜の構成に特徴のある化合物半導体装置に関するものである。
【０００２】
【従来の技術】ＭＥＳＦＥＴ（ショットキーバリアゲートＦＥＴ）やＨＥＭＴ（高電子移動度トランジスタ）等の化合物半導体電界効果型トランジスタやＨＢＴ（ヘテロ接合バイポーラトランジスタ）等の化合物半導体装置は、高周波動作素子として用いられており、高周波応用の一つとして、例えば、携帯電話基地局の送信用パワー増幅器に用いる高出力ＦＥＴや、携帯電話用のマイクロ波やミリ波での増幅器があり、さらには、光通信用の信号処理回路等に応用が期待される。
【０００３】しかし、化合物半導体装置においては、Ｓｉに対するSiO_2膜のような界面準位密度の低い絶縁膜界面を形成することが困難であった。例えば、ＧａＡｓに対する絶縁膜としてはＳｉＮ、SiO_2、或いは、Ga_2O_3等の絶縁膜が検討されたが、ＧａＡｓにはピンニング（ｐｉｎｎｉｎｇ）を引き起こす独特の界面準位が存在するので、界面準位密度を低減することが困難であり、そのため、ＧａＡｓ等のIII-V族化合物半導体においてはＭＩＳＦＥＴは実用化されず、ＭＥＳＦＥＴやＨＥＭＴ構造で界面の問題を回避してきた。なお、化合物半導体における通常の界面準位密度は、10^{13}～$10^{14}eV^{-1}cm^{-2}$程度である。
【０００４】ここで、図７（ａ）を参照して、ＧａＡｓにおけるピンニング効果を説明する。
図７（ａ）参照
図７（ａ）は、金属とｎ型ＧａＡｓとを接合させた場合のバンドダイヤグラムであり、ＧａＡｓに対しどの様な金属を接合させた場合にも、詳細な因果関係は判明していないものの、ピンニング効果により金属の種類によらない一定のバンドベンディングがあり、それによってバリアハイトは一定になって半導体／金属界面に整流特性が生じ、ｎ型ＧａＡｓへのオーミックコンタクトの抵抗が高くなる傾向がある。
【０００５】この様なピンニング効果を改善するために、ＧａＡｓの表面を$(NH_4)_2S_x$やNa_2Sの溶液中で処理してＧａＡｓ表面のダングリング・ボンドをＳ（硫黄）により終端処理（ターミネート）することや（必要ならば、特開平４－１９９５１８号公報参照）、或いは、ＧａＡｓ表面をH_2Sガスによって処理し、ＧａＡｓ表面のダングリング・ボンドをＳによりターミネートすること（必要ならば、特開平２－１７０４１７号公報参照）が知られている。
【０００６】この様に、ＧａＡｓ表面のダングリング・ボンドをＳによりターミネートすることによって形成されたＧａ－Ｓ結合によって表面が安定化され、ＰＬ（フォトルミネッセンス）強度の増加や、バリアハイトの金属仕事関数依存性がもたらされることになるので、この事情を図７（ｂ）を参照して説明する。
【０００７】図７（ｂ）参照
図７（ｂ）は、ｎ型ＧａＡｓの表面をＳによってターミネートしたのち、金属を接合させた場合のバンドダイヤグラムであり、ターミネートにより形成されたＧａＳの存在によりｎ型ＧａＡｓ表面のピンニングが解除されるため、金属の仕事関数を反映したショットキーバリアが形成され、バリアハイトが低くなる金属、例えば、Ｔｉを選択するとｎ型ＧａＡｓ表面におけるバンドベンディングが小さくなり、金属とｎ型ＧａＡｓとがＧａＳにおけるトンネル電流を介してオーミックに接続されることになる。
【０００８】しかし、この様なＳによるターミネートにより形成されたＧａＳ層は１原子層（モノレーヤ）と極端に薄い膜であるため、Ｓ処理により安定化した表面をそのまま安定に保持することが困難であるという問題がある。例えば、Ｓ処理を施したＧａＡｓ表面に、表面保

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護膜としてＳｉＮ膜やSiO_2膜を堆積させた場合、ＰＬ強度が著しく減少して、ピンニングを解除する効果が減少してしまうという問題がある。

【０００９】また、Ｓ処理を施したＧａＡｓの表面に金属を堆積させてオーミック電極を形成する場合、熱処理に伴って金属とＧａＡｓとが反応してショットキー特性が急激に変化して、オーミック電極の形成と同時にピンニングを解除する効果が減少してしまうという問題がある。

【００１０】この様な、Ｓ処理における安定性、特に、熱的安定性を改善するために、本発明者等は、ターシャリブチルガリウムサルファキュベン〔$((t-Bu)GaS)_4$〕の昇華により形成した３０ｎｍ程度の厚いアモルファスＧａＳ層をゲート絶縁膜として用いることによってＧａＡｓ表面のピンニングを解除し、化合物半導体ＭＩＳＦＥＴを構成することを提案している（必要ならば、特開平１０－９８１８５号公報参照）。なお、ＧａＳ層はＧａＡｓとの格子不整を緩和するためにアモルファス状としているが、ＧａＳを結晶化させた場合には、組成比が１：１の立方晶系の構造をとる。

【００１１】さらに、本発明者等は、この様な厚いＧａＳ層によるピンニングの解除をオーミック電極の形成のために用いることも提案しているので（必要ならば、特願平９－３５１６３３号参照）、この様な改良型ＭＩＳＦＥＴを図８を参照して説明する。

【００１２】図８（ａ）参照

図８（ａ）は、従来の改良型ＭＩＳＦＥＴの断面図であり、まず、半絶縁性ＧａＡｓ基板６１上に、ＭＯＶＰＥ法（有機金属気相成長法）を用いてＣ（炭素）濃度が$3\times10^{15}cm^{-3}$で厚さが３００ｎｍ（＝３０００Å）のp^-型ＧａＡｓチャネル層６２をエピタキシャル成長させたのち、固体原料であるターシャリブチルガリウムサルファキュベンを真空中で昇華させることによって、厚さ５ｎｍ～２０ｎｍのＧａＳ層６３を堆積させ、次いで、プラズマ励起型ＣＶＤ法によって厚さ５０ｎｍのＳｉＮ層６４を堆積させる。

【００１３】次いで、レジストパターン（図示せず）をマスクとして、バッファードフッ酸を用いてエッチングを行って露出するＳｉＮ層６４を選択的に除去してソース・ドレイン電極を形成するための開口部を形成したのち、レジストパターンを除去し、次いで、新たなレジストパターン（図示せず）を用いたリフトオフ法によって、Ｔｉ／Ｐｔ／Ａｕ層からなるゲート電極６６、ソース電極６７、及び、ドレイン電極６８を形成することによって化合物半導体ＭＩＳＦＥＴの基本構造が完成する。なお、この場合のゲート絶縁膜６５は、ＧａＳ層６３とＳｉＮ層６４との２層構造となる。

【００１４】この様な改良型ＭＩＳＦＥＴにおいては、モノレーヤに比べてかなり厚いＧａＳ層を介してソース電極６７及びドレイン電極６８を設けているので、p^-型ＧａＡｓチャネル層６２の表面におけるピンニング効果が解除されたままとなり、その結果、低抵抗のオーミックコンタクトを形成することができる。

【００１５】この場合のコンタクト抵抗率のＧａＳの膜厚依存性は既に上記の特願平９－３５１６３３号において開示しているが、改めて、この事情を図８（ｂ）を参照して説明する。

図８（ｂ）参照

図８（ｂ）は、ＧａＡｓ上にＧａＳ層の膜厚を変えてＴｉ電極を形成したのち、３００℃において１０分熱処理した場合のコンタクト抵抗率（$\Omega\cdot cm^2$）を測定した結果を示す図であり、膜厚が０Åの高抵抗のショットキーバリアから、準ショットキーバリア（ｓｃｈｏｔｔｋｙ　ｌｉｋｅ）を経て、１５０Å（＝１５ｎｍ）程度における抵抗率が最低になり、膜厚が２０ｎｍ程度で再び準ショットキーバリアとなり、それ以上では、高抵抗の絶縁膜となる。したがって、ＧａＳ層の膜厚を適宜選択することによって、絶縁膜としても、コンタクト抵抗を低減するための膜としても使用できるものである。なお、この場合のＧａＳ層の膜厚は、堆積時の膜厚であり、熱処理によりＴｉと反応した反応層がＴｉ電極側に形成されて、実際の膜厚はこの数値よりも低減しているものと考えられる。

【００１６】

【発明が解決しようとする課題】しかし、特開平１０－９８１８５号公報において開示されているＭＩＳＦＥＴの様に、ＧａＳ層のみによってゲート絶縁膜を構成した場合、ゲート絶縁膜となるＧａＳ層を薄くすると、ＧａＳ層の絶縁耐圧が低いためにＭＩＳ構造部において大きなリーク電流が流れるという問題がある。

【００１７】また、図８（ａ）に示した改良型ＭＩＳＦＥＴにおいては、オーミック電極を形成するための熱処理工程において、ＧａＳ層と金属電極との反応が進行してオーミックの特性が最も良くなる膜厚に応じた熱処理時間範囲があり、反応しすぎると特性が悪化するという問題があるので、ＧａＳ層を絶縁膜及びコンタクト抵抗を低減するための膜として同時に用いた場合には、ＧａＳ層の膜厚については、絶縁膜用とコンタクト抵抗の低減用とは、互いにトレードオフの関係になり、採用する膜厚が問題となり、さらに、熱処理時間にも問題があるので、プロセスの自由度が制限されるという問題がある。

【００１８】さらに、図８（ａ）に示した改良型ＭＩＳＦＥＴにおいては、ＧａＳ層とＳｉＮ層とを堆積させるための成長装置が全く異なるため、製造装置構成が複雑化し、それに伴って製造工程数が増加するので、スループットが低下するという問題がある。

【００１９】したがって、本発明は、化合物半導体におけるピンニング効果の解除、界面準位密度の低減、及び、オーミック抵抗の低減を簡単な製造装置構成によっ

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て行うことを目的とする。

【0020】

【課題を解決するための手段】図1は本発明の原理的構成の説明図であり、この図1を参照して本発明における課題を解決するための手段を説明する。

図1参照

（1）本発明は、化合物半導体装置において、化合物半導体層2の表面を、2原子層以上の厚さの少なくともGaSを含む層3で覆うと共に、少なくともGaSを含む層3の少なくとも一部をGaN層4で覆ったことを特徴とする。

【0021】この様に、化合物半導体層2の表面を少なくともGaSを含む層3で覆うことによって界面準位密度を低減するとともにピンニングを解除し、且つ、その膜厚を2原子層以上の厚さにすることによって、熱的安定性を高めることができるとともに、図8（b）から明らかなようにコンタクト抵抗を低減することができる。なお、「少なくともGaSを含む層3」とは、GaS層自体、AlGaS層或いはGaSSe層等のIII-VI族化合物半導体層、或いは、これらに他の金属元素が混入した層を意味する。

【0022】さらに、この少なくともGaSを含む層3をSiN層の代わりにGaN層4で覆うことによって製造装置を共通化することができ、それによって製造工程が簡素化してスループットが向上する。特に、半絶縁性化合物半導体基板1上に化合物半導体層2を成長させる場合、化合物半導体層2、少なくともGaSを含む層3、及び、GaN層4を同じ製造装置を用いて製造することができる。

【0023】また、この少なくともGaSを含む層3をGaN層4で覆うことによって、プラズマアッシング工程等における少なくともGaSを含む層3の剥離を防止することができるとともに、オーミック電極を設ける場合に、少なくともGaSを含む層3の膜厚を最適範囲に制御することが容易になる。

【0024】（2）また、本発明は、上記（1）において、GaN層4を少なくともGaSを含む層でさらに被覆したことを特徴とする。

【0025】一般に、GaN層4を少なくともGaSを含む層3上に厚く堆積させることは容易ではないので、GaN層4の上に少なくともGaSを含む層をさらに設けることによって、全体の厚さを厚くすることができ、それによって、絶縁耐圧を高めることができる。

【0026】（3）また、本発明は、上記（1）において、GaN層4を少なくともGaSを含む層でさらに被覆すると共に、少なくともGaSを含む層の表面をGaN層でさらに被覆したことを特徴とする。

【0027】この様に、最上層をGaN層にすることによって、プラズマアッシング工程等における剥離等の少なくともGaSを含む層のプロセス不安定性を改善することができる。

【0028】（4）また、本発明は、上記（1）乃至（3）のいずれかにおいて、少なくともGaSを含む層3に接する化合物半導体層2が、III-V族化合物半導体層であることを特徴とする。

【0029】この様に、少なくともGaSを含む層3のS（硫黄）により表面のダングリング・ボンドをターミネートさせる対象の化合物半導体としては、界面準位密度の低減が困難な$In_xAl_yGa_{1-x-y}As_wP_{1-w}$やナイトライド系化合物半導体等のIII-V族化合物半導体が好適である。

【0030】（5）また、本発明は、上記（1）乃至（4）のいずれかにおいて、少なくとも一つのオーミック電極を、化合物半導体層2に接する少なくともGaSを含む層3に接するように設けたことを特徴とする。

【0031】この様に、表面を被覆するGaN層4を除去して露出した少なくともGaSを含む層3の表面にソース電極7及びドレイン電極8等のオーミック電極を設けることによって、少なくともGaSを含む層3の膜厚を堆積時の条件で精度良く制御することができるので、コンタクト抵抗を再現性良く低減することができる。なお、HBT等に適用する場合には、例えば、ベース電極のみを少なくともGaSを含む層3の表面に設け、エミッタ電極或いはコレクタ電極は化合物半導体層2の表面に直接設けても良い。

【0032】（6）また、本発明は、上記（1）乃至（4）のいずれかにおいて、少なくとも一つのオーミック電極を、化合物半導体層2に接する少なくともGaSを含む層3を覆うGaN層4に接するように設けたことを特徴とする。

【0033】上述の様に、GaN層4の厚さは一般に薄いので、GaN層4の表面に電極を設けても、トンネル電流を介して電極と化合物半導体層2がオーミックに接続され、それによって、コンタクトホールの形成工程を必要としないので製造工程数を削減することができる。

【0034】（7）また、本発明は、上記（5）または（6）において、GaN層4の内の最上層の表面に非オーミック電極を設けて金属－絶縁体－半導体構造を構成したことを特徴とする。

【0035】この様に、少なくともGaSを含む層3とGaN層4の積層構造を用いることにより、低抵抗のソース電極7及びドレイン電極8等のオーミック電極と、界面準位密度が低く且つ絶縁耐圧に優れた金属－絶縁体－半導体構造（MIS構造）を同時に構成することができるので、MIS型化合物半導体装置の実現が可能になる。なお、この場合のゲート絶縁膜5は、少なくともGaSを含む層3とGaN層4の積層構造膜となる。

【0036】

【発明の実施の形態】ここで、図2を参照して、本発明の第1の実施の形態のMISFETの製造工程を説明す

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る。
図2（ａ）参照
まず、半絶縁性ＧａＡｓ基板１１上に、ＭＯＶＰＥ法を用いて、厚さが、例えば、３００ｎｍで、炭素濃度が、例えば、$3\times10^{15}cm^{-3}$のチャネル層となるｐ$^-$型ＧａＡｓ層１２を成長させたのち、チャンバー内に収納した固体原料であるターシャリブチルガリウムサルファキュベンを、３５０～５００℃、例えば、３５０℃の基板温度において昇華させることによって、厚さが、２原子層～２０ｎｍ、例えば、１０ｎｍのアモルファス状態のＧａＳ層１３成長させる。
【００３７】引き続いて、同じチャンバー内で、基板温度を４００～４５０℃、例えば、４００℃とした状態で、ＴＥＧａ（トリエチルガリウム）を０．２５ｓｃｃｍ、及び、３５０Ｗの高周波電力によって励起した窒素ラジカルを１ｓｃｃｍ流すことによって、ＧａＳ層１３上に、厚さが、０．５～５ｎｍ、例えば、５ｎｍのＧａＮ層１４を成長させる。なお、この場合のＧａＮ層１４の成長速度は、約２０～４０ｎｍ／時である。
【００３８】図2（ｂ）参照
次いで、ソース・ドレイン領域に対応する開口部１６を設けたレジストパターン１５をマスクとしてホットH_3PO_4を用いたウェット・エッチングを施すことによって、ＧａＮ層１４を選択的に除去してＧａＳ層１３を露出させる。
【００３９】図2（ｃ）参照
次いで、レジストパターン１５を除去したのち、ゲート電極及びソース・ドレイン電極に対応する開口部を有する新たなレジストパターン１７を設け、全面に、厚さが、例えば、１０ｎｍのＴｉ膜、厚さが、例えば、３０ｎｍのＰｔ膜、及び、厚さが、例えば、３００ｎｍのＡｕ膜を順次堆積させることによってＴｉ／Ｐｔ／Ａｕ層１８を堆積させる。
【００４０】図2（ｄ）参照
次いで、レジストパターン１７を除去することによって、レジストパターン１７上に堆積したＴｉ／Ｐｔ／Ａｕ層１８をリフトオフすることによって、ゲート電極２０、ソース電極２１、及び、ドレイン電極２２を形成する。なお、この場合のゲート絶縁膜１９は、ＧａＳ層１３とＧａＮ層１４との積層構造となる。
【００４１】この第１の実施の形態のＭＩＳＦＥＴにおいては、ｐ$^-$型ＧａＡｓ層１２に接するようにＧａＳ層１３を設けているので、ＧａＳ層１３によるターミネート効果により界面準位密度を$10^{11}eV^{-1}cm^{-2}$以下にすることができ、それによって、ｐ$^-$型ＧａＡｓ層１２の表面に反転層、即ち、ｎ型のチャネル層が形成される。
【００４２】また、ゲート絶縁膜１９は、ＧａＳ層１３とＧａＮ層１４との２層構造で構成されるので、ＧａＳ層１３の絶縁耐圧の低さをワイドギャップのＧａＮ層１４によって補うことができ、ゲート絶縁耐圧を高め、リーク電流を低減することができる。
【００４３】なお、この場合のＧａＮ層１４の作用は、上述の図８（ａ）に示したＳｉＮ層６４と同様であるが、ＧａＮ層１４は、ＳｉＮ層６４と異なりＧａＳ層１３と同じチャンバー内で一連の工程として堆積することができるので、製造装置が簡素化され、また、製造装置間を移動させる場合の清浄化工程等が不要になるのでスループットが向上する。
【００４４】また、ソース電極２１及びドレイン電極２２は、厚さが、例えば、１０ｎｍのＧａＳ層１３を介して設けているので、ピンニング効果が解除されてコンタクト抵抗率の低いオーミック電極として形成することができる。なお、この場合のＧａＳ層１３の膜厚は、成膜時の膜厚で決まるので、コンタクト抵抗率を図８（ｂ）に示した最適範囲に精度良く制御することができ、それによって、化合物半導体ＭＩＳＦＥＴを再現性良く製造することができる。
【００４５】次に、図３を参照して、本発明の第２の実施の形態のＭＩＳＦＥＴを説明する。なお、図３（ａ）は、オーミック電極をＧａＳ層上に設けた場合の断面図であり、また、図３（ｂ）は、オーミック電極をＧａＮ層を介して設けた場合の断面図である。
図3（ａ）参照
まず、上記の第１の実施の形態と全く同様に、半絶縁性ＧａＡｓ基板１１上に、ＭＯＶＰＥ法を用いて、厚さが、例えば、３００ｎｍで、炭素濃度が、例えば、$3\times10^{15}cm^{-3}$のチャネル層となるｐ$^-$型ＧａＡｓ層１２を成長させたのち、チャンバー内に収納したターシャリブチルガリウムサルファキュベンを、３５０～５００℃、例えば、３５０℃の基板温度において昇華させることによって、厚さが、２原子層～２０ｎｍ、例えば、１０ｎｍのアモルファス状態のＧａＳ層１３成長させる。
【００４６】引き続いて、同じチャンバー内で、基板温度を４００～４５０℃、例えば、４００℃とした状態で、ＴＥＧａを０．２５ｓｃｃｍ、及び、３５０Ｗの高周波電力によって励起した窒素ラジカルを１ｓｃｃｍ流すことによって、ＧａＳ層１３上に、厚さが、０．５～５ｎｍ、例えば、２ｎｍのＧａＮ層２３を成長させる。
【００４７】引き続いて、同じチャンバー内で、ターシャリブチルガリウムサルファキュベンを、３５０～５００℃、例えば、３５０℃の基板温度において昇華させることによって、厚さが、２原子層～２０ｎｍ、例えば、１０ｎｍのアモルファス状態のＧａＳ層２４成長させる。
【００４８】次いで、ソース・ドレイン領域に対応する開口部を設けたレジストパターン（図示せず）をマスクとしてH_3PO_4＋ＨＣｌの混合液を用いたウェット・エッチングを施すことによって、ＧａＳ層２４を選択的に除去してＧａＮ層２３を露出させ、次いで、ホットＨ

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$_3PO_4$ を用いたウェット・エッチングを施すことによって、ＧａＮ層２３を選択的に除去してＧａＳ層１３を露出させる。

【００４９】以降は上記の第１の実施の形態と全く同様に、レジストパターンを除去したのち、ゲート電極及びソース・ドレイン電極に対応する開口部を有する新たなレジストパターンを設け、全面に、厚さが、例えば、１０ｎｍのＴｉ膜、厚さが、例えば、３０ｎｍのＰｔ膜、及び、厚さが、例えば、３００ｎｍのＡｕ膜を順次堆積させることによってＴｉ／Ｐｔ／Ａｕ層を堆積させ、次いで、レジストパターンを除去して、レジストパターン上に堆積したＴｉ／Ｐｔ／Ａｕ層をリフトオフすることによって、ゲート電極２０、ソース電極２１、及び、ドレイン電極２２を形成する。なお、この場合のゲート絶縁膜２５は、ＧａＳ層１３／ＧａＮ層２３／ＧａＳ層２４の積層構造となる。

【００５０】この第２の実施の形態のＭＩＳＦＥＴの素子特性は上記の第１の実施の形態と基本的に同様であるが、比較的低温におけるＧａＮ層の堆積工程において、上記の第１の実施の形態のＧａＮ層１３のように、厚く堆積させることは一般には容易ではないので、ＧａＮ層２３を薄くする代わりに、ＧａＳ層の総計の厚さを厚くしてゲート絶縁耐圧を高めたものである。

【００５１】この場合、ＧａＳ層１３を２０ｎｍとしてＧａＳ層２４を省略することも考えられるが、その場合には、ソース・ドレイン領域におけるＧａＳ層２４厚さが厚くなりすぎコンタクト抵抗率が高くなりすぎるが、この第２の実施の形態においては薄いＧａＮ層２３をエッチングストッパー的に用いているので、コンタクト抵抗率を図８（ｂ）に示した最適範囲に精度良く制御することができ、それによって、化合物半導体ＭＩＳＦＥＴを再現性良く製造することができる。

【００５２】図３（ｂ）参照

図３（ｂ）に示すＭＩＳＦＥＴは図３（ａ）の変形例であり、成膜工程は図３（ａ）の場合と同様であるので説明を省略するが、ソース・ドレイン領域に対応する開口部を形成する際に、ＧａＳ層２４のみを除去するだけで、薄いＧａＮ層２３をそのまま残しておき、ＧａＮ層２３の表面にソース電極２１及びドレイン電極２２を設けたものである。

【００５３】この場合、ＧａＮ層２３は２ｎｍ程度と非常に薄いので、トンネル電流を介してソース電極２１及びドレイン電極２２とｐ$^-$ 型ＧａＡｓ層１２とがオーミックに接続されることになる。この様な構成を採用することによって、ＧａＮ層２３のエッチング工程が不要となるので、製造工程数を削減することができ、スループットが向上することになる。

【００５４】次に、図４を参照して、本発明の第３の実施の形態のＭＩＳＦＥＴを説明する。なお、図４（ａ）は、オーミック電極をＧａＳ層上に設けた場合の断面図であり、また、図４（ｂ）は、オーミック電極をＧａＮ層を介して設けた場合の断面図である。

図４（ａ）参照

まず、上記の第１の実施の形態と全く同様に、半絶縁性ＧａＡｓ基板１１上に、ＭＯＶＰＥ法を用いて、厚さが、例えば、３００ｎｍで、炭素濃度が、例えば、$3\times10^{15}cm^{-3}$のチャネル層となるｐ$^-$ 型ＧａＡｓ層１２を成長させたのち、チャンバー内に収納したターシャリブチルガリウムサルファキュベンを、３５０～５００℃、例えば、３５０℃の基板温度において昇華させることによって、厚さが、２原子層～２０ｎｍ、例えば、１０ｎｍのアモルファス状態のＧａＳ層１３成長させる。

【００５５】引き続いて、同じチャンバー内で、基板温度を４００～４５０℃、例えば、４００℃とした状態で、ＴＥＧａを０．２５ｓｃｃｍ、及び、３５０Ｗの高周波電力によって励起した窒素ラジカルを１ｓｃｃｍ流すことによって、ＧａＳ層１３上に、厚さが、０．５～５ｎｍ、例えば、２ｎｍのＧａＮ層２３を成長させる。

【００５６】引き続いて、同じチャンバー内で、ターシャリブチルガリウムサルファキュベンを、３５０～５００℃、例えば、３５０℃の基板温度において昇華させることによって、厚さが、２原子層～２０ｎｍ、例えば、１０ｎｍのアモルファス状態のＧａＳ層２４成長させたのち、引き続いて、同じチャンバー内で、基板温度を４００～４５０℃、例えば、４００℃とした状態で、ＴＥＧａを０．２５ｓｃｃｍ、及び、３５０Ｗの高周波電力によって励起した窒素ラジカルを１ｓｃｃｍ流すことによって、ＧａＳ層２４上に、厚さが、０．５～５ｎｍ、例えば、２ｎｍのＧａＮ層２６を成長させる。

【００５７】次いで、ソース・ドレイン領域に対応する開口部を設けたレジストパターン（図示せず）をマスクとしてホットH_3PO_4 を用いたウェット・エッチングを施すことによって、ＧａＮ層２６を選択的に除去してＧａＳ層２４を露出させたのち、H_3PO_4 ＋ＨＣｌの混合液を用いたウェット・エッチングを施すことによって、ＧａＳ層２４を選択的に除去してＧａＮ層２３を露出させ、次いで、再び、ホットH_3PO_4 を用いたウェット・エッチングを施すことによって、ＧａＮ層２３を選択的に除去してＧａＳ層１３を露出させる。

【００５８】以降は上記の第１の実施の形態と全く同様に、レジストパターンを除去したのち、ゲート電極及びソース・ドレイン電極に対応する開口部を有する新たなレジストパターンを設け、全面に、厚さが、例えば、１０ｎｍのＴｉ膜、厚さが、例えば、３０ｎｍのＰｔ膜、及び、厚さが、例えば、３００ｎｍのＡｕ膜を順次堆積させることによってＴｉ／Ｐｔ／Ａｕ層を堆積させ、次いで、レジストパターンを除去して、レジストパターン上に堆積したＴｉ／Ｐｔ／Ａｕ層をリフトオフすることによって、ゲート電極２０、ソース電極２１、及び、ドレイン電極２２を形成する。なお、この場合のゲート絶

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縁膜27は、GaS層13／GaN層23／GaS層24／GaN層26の積層構造となる。

【0059】この第3の実施の形態のMISFETの素子特性は上記の第2の実施の形態と基本的に同様であるが、レジストパターンを除去するプラズマアッシング工程等において、GaS層24が剥離しやすい等のプロセス不安定性があるので、最上層にGaN層26を設けておくことによってプロセス安定性が向上する。また、GaN層26を設けることによって、ゲートの絶縁耐圧はさらに向上する。

【0060】また、この第3の実施の形態においても、下層のGaN層23をエッチングストッパー的に用いているので、コンタクト抵抗率を図8（b）に示した最適範囲に精度良く制御することができ、それによって、化合物半導体MISFETを再現性良く製造することができる。

【0061】図4（b）参照

図4（b）に示したMISFETは図4（a）の変形例で、図3（b）のMISFETに対応するものであり、成膜工程は図4（a）の場合と同様であるので説明を省略するが、ソース・ドレイン領域に対応する開口部を形成する際に、GaN層26及びGaS層24を除去するだけで、薄いGaN層23をそのまま残しておき、GaN層23の表面にソース電極21及びドレイン電極22を設けたものである。

【0062】この場合にも、GaN層23は2nm程度と非常に薄いので、トンネル電流を介してソース電極21及びドレイン電極22とp⁻型GaAs層12とがオーミックに接続されることになる。この様な構成を採用することによって、GaN層23のエッチング工程が不要となるので、製造工程数を削減することができ、スループットが向上することになる。

【0063】次に、図5を参照して、本発明の第4の実施の形態のHEMTを説明する。なお、図5（a）は、オーミック電極をGaS層上に設けた場合のHEMTの断面図であり、また、図5（b）は、オーミック電極をGaN層を介して設けた場合のHEMTの断面図である。

図5（a）参照

まず、半絶縁性GaAs基板31上に、MOVPE法を用いて、TEGa（トリエチルガリウム）、AsH_3、及び、キャリアガスとしてのH_2を流して厚さが、例えば、500nmのアンドープのi型GaAsバッファ層32を成長させたのち、TMIn（トリメチルインジウム）を加えて、厚さが、例えば、14nmで、In組成比が0.2のノン・ドープのi型InGaAsチャネル層32を堆積させ、次いで、AsH_3をPH_3に切り替えるとともに、不純物源としてSiH_4を加えて、例えば、厚さが25nmで、Si濃度が$2\times10^{18}cm^{-3}$で、In組成比が0.49のn型InGaPキャリア供給層33を成長させ、次いで、TMInの供給を停止するとともに、PH_3を再びAsH_3に替えて厚さが、例えば、70nmで、Si濃度が、例えば、$5\times10^{18}cm^{-3}$のn⁺型GaAsコンタクト層35を堆積させる。

【0064】次いで、n⁺型GaAsコンタクト層35を$H_3PO_4+H_2O_2+H_2O$の混合液を用いたウェット・エッチングによりソース・ドレイン領域に対応するようにパターニングしてゲートリセス部を形成したのち、GaS堆積用チャンバー内に収容し、チャンバー内においてターシャリブチルガリウムサルファキュベンを、350～500℃、例えば、350℃の基板温度において昇華させることによって、厚さが、2原子層～20nm、例えば、10nmのアモルファス状態のGaS層36成長させ、引き続いて、同じチャンバー内で、基板温度を400～450℃、例えば、400℃とした状態で、TEGaを0.25sccm、及び、350Wの高周波電力によって励起した窒素ラジカルを1sccm流すことによって、GaS層36上に、厚さが、0.5～5nm、例えば、2nmのGaN層37を成長させる。

【0065】次いで、ゲート形成用の開口部を設けたレジストパターン（図示せず）をマスクとしてホットH_3PO_4を用いたウェット・エッチングを施すことによってGaN層37を選択的除去したのち、H_3PO_4とHClの混合液を用いたウェット・エッチングを施すことによってGaS層36を選択的に除去する。

【0066】次いで、レジストパターンを除去したのち、ソース・ドレイン領域に対応する開口部を有する新たなレジストパターン（図示せず）をマスクとしてホットH_3PO_4を用いたウェット・エッチングを施すことによってGaN層37を選択的除去したのち、全面に厚さが、例えば、500nmのAl膜を蒸着し、レジストパターンとともにリフトオフすることによってソース電極39及びドレイン電極40を形成する。

【0067】次いで、レジストパターンを除去したのち、ゲート電極形成用の開口部を設けた新たなレジストパターン（図示せず）を設け、全面に厚さが、例えば、500nmのAl膜を蒸着し、レジストパターンとともにリフトオフしてゲート電極38を形成することによってHEMTの基本構成が完成する。

【0068】この本発明の第4の実施の形態のHEMTにおいては、n型InGaPキャリア供給層34の表面の内、ゲート電極38と接する部分を除いたチャネル領域をGaS層36で被覆しているので、n型InGaPキャリア供給層34の表面のダングリング・ボンドをSでターミネートして安定化することができ、それによって界面準位密度が低減するのでHEMTの動作を安定化することができる。

【0069】この場合も、10nm程度の膜厚のGaS

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層３６を介してソース電極３９及びドレイン電極４０を設けているので、ソース電極３９及びドレイン電極４０を低抵抗のオーミック電極とすることができる。

【００７０】また、この第４の実施の形態において、ＧａＳ層３６の表面はＧａＮ層３７で被覆されているので、レジストパターンを除去するためにプラズマアッシングを行う際に、ＧａＳ層３６が剥離することがなく、プロセス安定性が向上する。

【００７１】図５（ｂ）参照

図５（ｂ）に示すＨＥＭＴは図５（ａ）の変形例であり、成膜工程は図５（ａ）の場合と同様であるので説明を省略するが、薄いＧａＮ層３７を介してソース電極３９及びドレイン電極４０を設けたもので、ゲート形成用の開口部を設けるだけで良いので、エッチング工程を少なくすることができ、スループットが向上する。

【００７２】また、この場合には、ゲート電極３８、ソース電極３９、及び、ドレイン電極４０を一度の成膜工程及びリフトオフ工程によって形成することができるので、製造工程をさらに少なくすることができる。なお、ＧａＮ層３７は２ｎｍ程度と非常に薄いので、トンネル電流を介してソース電極３９及びドレイン電極４０とn^+型ＧａＡｓコンタクト層３５とがオーミックに接続されることになる。

【００７３】次に、図６を参照して、本発明の第５の実施の形態のＨＢＴを説明する。なお、図６（ａ）は、オーミック電極をＧａＳ層上に設けた場合のＨＢＴの断面図であり、また、図６（ｂ）は、オーミック電極をＧａＮ層を介して設けた場合のＨＢＴの断面図である。

図６（ａ）参照

まず、半絶縁性ＧａＡｓ基板４１上に、ＭＯＶＰＥ法を用いて、ＴＥＧａ、AsH_3、不純物源としてSiH_4、及び、キャリアガスとしてのH_2を流して、例えば、厚さが５００ｎｍで、Ｓｉ濃度が$3\times10^{18}cm^{-3}$のn^+型ＧａＡｓサブコレクタ層４２、及び、例えば、厚さが４５０ｎｍで、Ｓｉ濃度が$3\times10^{16}cm^{-3}$のｎ型ＧａＡｓコレクタ層４３を順次堆積させる。

【００７４】次いで、SiH_4をCBr_4に切り替えて、例えば、厚さが７０ｎｍで、Ｃ濃度が$4\times10^{19}cm^{-3}$のp^+型ＧａＡｓベース層４４を堆積させたのち、CBr_4を再びSiH_4に切り替えるとともに、AsH_3をPH_3に切り替え、ＴＭＩｎを供給して、例えば、厚さが５０ｎｍで、Ｓｉ濃度が$3\times10^{17}cm^{-3}$で、Ｉｎ組成比が０．４９のｎ型ＩｎＧａＰエミッタ層４５を堆積させ、次いで、ＴＭＩｎの供給を停止するとともに、PH_3をAsH_3に切り替えて、例えば、厚さが２００ｎｍのn^+型ＧａＡｓエミッタキャップ層４６を堆積させる。なお、n^+型ＧａＡｓエミッタキャップ層４６は、ｎ型ＩｎＧａＰエミッタ層４５側の１５０ｎｍの厚さの部分のＳｉ濃度は$3\times10^{17}cm^{-3}$であり、残りの上側の５０ｎｍの厚さの部分のＳｉ濃度は$3\times10^{18}cm^{-3}$である。

【００７５】次いで、メサエッチングを施すことによって、n^+型ＧａＡｓエミッタキャップ層４６及びｎ型ＩｎＧａＰエミッタ層４５からなるエミッタメサを形成し、次いで、再びメサエッチングを行うことによって、p^+型ＧａＡｓベース層４４及びｎ型ＧａＡｓコレクタ層４３からなるベースメサを形成する。このメサエッチング工程において、ＧａＡｓ層のエッチングには、$H_3PO_4+H_2O_2+H_2O$の混合液を用い、ＩｎＧａＰのエッチングには、H_3PO_4とＨＣｌの混合液を用いる

なお、このＨＢＴを集積化する場合には、素子分離を行うために半絶縁性ＧａＡｓ基板４１に達するメサエッチングを行ってコレクタメサを形成する。

【００７６】次いで、基板をＧａＳ堆積用チャンバー内に収容し、チャンバー内においてターシャリブチルガリウムサルファキュベンを、３５０～５００℃、例えば、３５０℃の基板温度において昇華させることによって、厚さが、２原子層～２０ｎｍ、例えば、１０ｎｍのアモルファス状態のＧａＳ層４７成長させ、引き続いて、同じチャンバー内で、基板温度を４００～４５０℃、例えば、４００℃とした状態で、ＴＥＧａを０．２５ｓｃｃｍ、及び、３５０Ｗの高周波電力によって励起した窒素ラジカルを１ｓｃｃｍ流すことによって、ＧａＳ層４７上に、厚さが、０．５～５ｎｍ、例えば、２ｎｍのＧａＮ層４８を成長させる。

【００７７】次いで、ベース電極形成用の開口部を設けたレジストパターン（図示せず）をマスクとしてホットH_3PO_4を用いたウェット・エッチングを施すことによってＧａＮ層４８を選択的除去したのち、全面に厚さが２０ｎｍのＰｔ膜及び１５０ｎｍのＡｕ膜を順次堆積させ、レジストパターンとともに除去することによって、ベース電極５０を形成する。

【００７８】次いで、レジストパターンを除去したのち、エミッタ電極及びコレクタ電極形成用の開口部を有する新たなレジストパターン（図示せず）を設け、このレジストパターンをマスクとしてホットH_3PO_4を用いたウェット・エッチングを施すことによってＧａＮ層４８を選択的除去したのち、全面に厚さが、例えば、厚さが１０ｎｍＴｉ膜、厚さが３０ｎｍＰｔ膜、及び、厚さが３００ｎｍのＡｕ膜を順次蒸着し、レジストパターンとともにリフトオフしてエミッタ電極４９及びドレイン電極５１を形成することによってＨＢＴの基本構成が完成する。

【００７９】この本発明の第５の実施の形態のＨＢＴにおいては、p^+型ＧａＡｓベース層４４の露出表面及びｎ型ＩｎＧａＰエミッタ層４５の側面がＧａＳ層４７によって覆われているので、ベース－エミッタ間のｐｎ接合近傍の領域がＳによってターミネートされて界面準位密度が低減し、それによって、ｐｎ接合領域における表

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面再結合が抑制されるので電流利得を大きくすることができる。

【００８０】また、この場合も、１０ｎｍ程度の膜厚のＧａＳ層３６を介してエミッタ電極４９、ベース電極５０、及び、コレクタ電極５１を設けているので、エミッタ電極４９、ベース電極５０、及び、コレクタ電極５１を低抵抗のオーミック電極とすることができる。

【００８１】また、この第５の実施の形態においても、ＧａＳ層４７の表面はＧａＮ層４８で被覆されているので、レジストパターンを除去するためのプラズマアッシング工程において、ＧａＳ層４７が剥離することがなく、プロセス安定性が向上する。

【００８２】図６（ｂ）参照

図６（ｂ）に示すＨＢＴは図６（ａ）の変形例であり、成膜工程は図６（ａ）の場合と同様であるので説明を省略するが、薄いＧａＮ層４８を介してエミッタ電極４９、ベース電極５０、及び、コレクタ電極５１を設けたもので、ＧａＮ層４８を除去する必要がないので、エッチング工程を少なくすることができ、スループットが向上する。なお、ＧａＮ層４８は２ｎｍ程度と非常に薄いので、トンネル電流によってエミッタ電極４９、ベース電極５０、及び、コレクタ電極５１がオーミック電極となる。

【００８３】以上、本発明の各実施の形態を説明してきたが、本発明は各実施の形態に記載された構成に限られるものでなく、各種の変更が可能である。例えば、上記の第１乃至第３の実施の形態においては、半絶縁性ＧａＡｓ基板１１を出発材料とし、この上にp^-型ＧａＡｓ層１２、ＧａＳ層１３、及び、ＧａＮ層１３，２３等を一連の成長工程によって成膜しているが、半絶縁性ＧａＡｓ基板１１上にp^-型ＧａＡｓ層１２を成長させたエピタキシャルウェハを出発材料としても良いものである。

【００８４】この様な、エピタキシャルウェハを用いる場合には、ＧａＳ堆積用チャンバー内において、トリスジメチルアミノアルシンを用いて、例えば、５００℃の基板温度で１０分間処理を行うことによって、エピタキシャルウェハの表面の自然酸化膜を除去し、引き続いて、ＨＣｌガスを用いて、例えば、５００℃の基板温度で処理を行うことによって、p^-型ＧａＡｓ層１２の表面を数原子層程度エッチングして、表面を清浄化したのち、ＧａＳ層１３等の堆積を行えば良い。

【００８５】また、この様なクリーニング工程は、上記の第４及び第５の実施の形態における、半導体層のエッチング工程後に行うＧａＳ層３６，４７の成膜工程の前にも行うことが望ましく、第４の実施の形態においては、ｎ型ＩｎＧａＰキャリア供給層３４の表面も数原子層除去することになる。

【００８６】また、上記の第１乃至第３の実施の形態においては、ＧａＳ層１３上に、或いは、ＧａＮ層２３を介してソース電極２１及びドレイン電極２２を設けているが、ＧａＳ層１３も選択的に除去し、ゲート電極２０とは別個の工程で、２０ｎｍのＡｕ・Ｇｅ膜／５ｎｍのＮｉ膜／３００ｎｍのＡｕ膜からなる三層構造膜等のアロイ系のオーミック電極を形成しても良いものであり、上記の第５の実施の形態のエミッタ電極４９及びコレクタ電極５１の場合も全く同様である。

【００８７】また、上記の第４の実施の形態においてはＨＥＭＴとして説明しているが、ｉ型ＩｎＧａＡｓチャネル層３３をｎ型ＩｎＧａＡｓチャネル層に置き換えることによってＭＥＳＦＥＴとして動作させることが可能になり、本発明は、この様なＭＥＳＦＥＴも対象とするものである。

【００８８】また、上記の各実施の形態においては、ＧａＳ層をターシャリブチルガリウムサルファキュベンを用いて成膜しているが、ターシャリブチルガリウムサルファキュベンに限られるものではなく、$2[(tBu)_2Ga(\mu-SH)]_2$を用いても良いものである。

【００８９】また、上記の各実施の形態においては、ピンニング効果の発現が著しいＧａＡｓの表面安定化を主目的としているが、上記の第４及び第５の実施の形態の様にＩｎＧａＰの表面安定化にも寄与するものであり、ピンニング効果の解除には直接関係がなくとも、Ｓによって表面のダングリング・ボンドをターミネートすることにより界面準位密度を低減することができるので、素子特性の向上に寄与することができるものであり、したがって、$In_xAl_yGa_{1-x-y}As_wP_{1-w}$や$In_xAl_yGa_{1-x-y}As_wN_{1-w}$で表される他のIII-V族化合物半導体の表面安定化にも用いることができるものである。

【００９０】また、上記の各実施の形態においては、表面安定化を行う層をＧａＳ層として説明しているが、純粋なＧａＳ層に限られるものではなく、ＡｌＧａＳやＧａＳＳｅ等のIII-Ⅵ族化合物半導体でも良く、また、オーミック電極との固相拡散反応によって金属成分がドープまたは合金化されたＧａＳ層等でも良い。

【００９１】また、上記の各実施の形態においては、ＧａＳ層を絶縁体として捉え、トンネル電流によって実効的にオーミック化するとしているが、必ずしも、純粋に絶縁性である必要はなく、上述のオーミック電極との固相拡散反応によって金属成分がドープされることによって多少の導電性を有していてもかまわないものである。

【００９２】また、上記の各実施の形態におけるＧａＳ層の厚さとしては、２原子層～２０ｎｍとしているが、熱的安定性を増すためには、５ｎｍ以上の膜厚であることがより望ましく、また、ＧａＳ層を除去してオーミック電極を形成する場合には、ＧａＳ層は純粋に絶縁体として作用するものであるので、２０ｎｍ以上の膜厚でも良いのである。

【００９３】

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【発明の効果】本発明によれば、ＧａＡｓ等の化合物半導体層の表面を少なくとも２原子層以上の厚さのＧａＳ層とＧａＮ層の２層構造膜で覆っているので、化合物半導体層の表面をその後の熱処理工程においても変化しないように安定化することができ、且つ、ＧａＮ層を用いることによって製造装置を共通化することができ、さらに、ＧａＳ層上に或いはＧａＮ層を介してオーミック電極を設けているので、オーミック電極のコンタクト抵抗を低減することができるとともに、エッチング工程を削減することができるので、化合物半導体装置の高性能化及び低コスト化に寄与するところが大きい。

【００９４】特に、化合物半導体層としてＧａＡｓ層を用いた場合には、ピンニング効果を解除することができるとともに、良好な反転層を形成することができるので、化合物半導体ＭＩＳＦＥＴの実用化に寄与するところが大きい。

【図面の簡単な説明】

【図１】本発明の原理的構成の説明図である。

【図２】本発明の第１の実施の形態のＭＩＳＦＥＴの製造工程の説明図である。

【図３】本発明の第２の実施の形態のＭＩＳＦＥＴの断面図である。

【図４】本発明の第３の実施の形態のＭＩＳＦＥＴの断面図である。

【図５】本発明の第４の実施の形態のＨＥＭＴの断面図である。

【図６】本発明の第５の実施の形態のＨＢＴの断面図である。

【図７】ＧａＡｓにおけるピンニング効果とその防止法の説明図である。

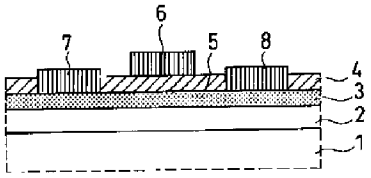
【図８】従来の改良型ＭＩＳＦＥＴの構造とコンタクト抵抗率の説明図である。

【符号の説明】

１　半絶縁性化合物半導体基板
２　化合物半導体層
３　少なくともＧａＳを含む層
４　ＧａＮ層
５　ゲート絶縁膜
６　ゲート電極
７　ソース電極
８　ドレイン電極
１１　半絶縁性ＧａＡｓ基板
１２　p^- 型ＧａＡｓ層
１３　ＧａＳ層
１４　ＧａＮ層
１５　レジストパターン
１６　開口部
１７　レジストパターン
１８　Ｔｉ／Ｐｔ／Ａｕ層
１９　ゲート絶縁膜
２０　ゲート電極
２１　ソース電極
２２　ドレイン電極
２３　ＧａＮ層
２４　ＧａＳ層
２５　ゲート絶縁膜
２６　ＧａＮ層
２７　ゲート絶縁膜
３１　半絶縁性ＧａＡｓ基板
３２　ｉ型ＧａＡｓバッファ層
３３　ｉ型ＩｎＧａＡｓチャネル層
３４　ｎ型ＩｎＧａＰキャリア供給層
３５　n^+ 型ＧａＡｓコンタクト層
３６　ＧａＳ層
３７　ＧａＮ層
３８　ゲート電極
３９　ソース電極
４０　ドレイン電極
４１　半絶縁性ＧａＡｓ基板
４２　n^+ 型ＧａＡｓサブコレクタ層
４３　ｎ型ＧａＡｓコレクタ層
４４　p^+ 型ＧａＡｓベース層
４５　ｎ型ＩｎＧａＰエミッタ層
４６　n^+ 型ＧａＡｓエミッタキャップ層
４７　ＧａＳ層
４８　ＧａＮ層
４９　エミッタ電極
５０　ベース電極
５１　コレクタ電極
６１　半絶縁性ＧａＡｓ基板
６２　p^- 型ＧａＡｓチャネル層
６３　ＧａＳ層
６４　ＳｉＮ層
６５　ゲート絶縁膜
６６　ゲート電極
６７　ソース電極
６８　ドレイン電極

【図1】

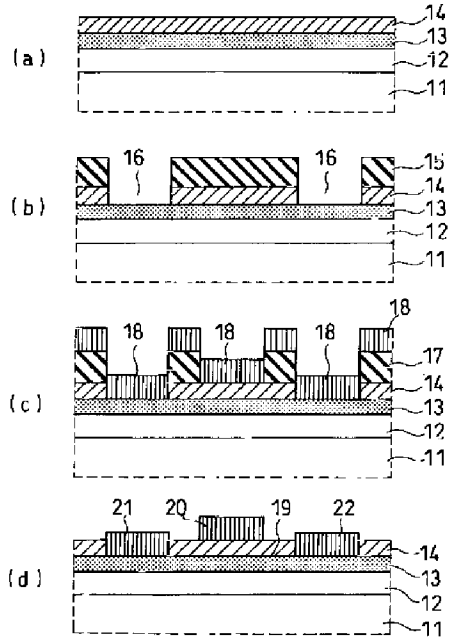
本発明の原理的構成の説明図



1：半絶縁性化合物半導体基板
2：化合物半導体層
3：少なくともＧａＳを含む層
4：ＧａＮ層
5：ゲート絶縁膜
6：ゲート電極
7：ソース電極
8：ドレイン電極

【図2】

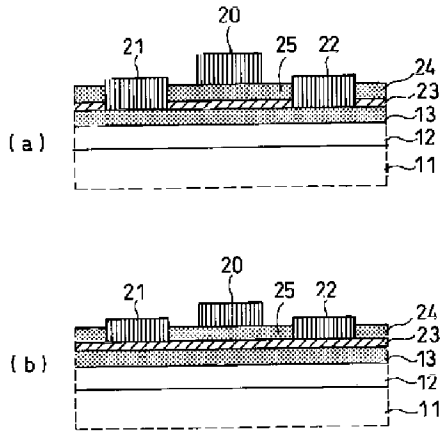
本発明の第１の実施の形態のＭＩＳＦＥＴの製造工程の説明図



11：半絶縁性ＧａＡｓ基板
12：p⁻型ＧａＡｓ層
13：ＧａＳ層
14：ＧａＮ層
15：レジストパターン
16：開口部
17：レジストパターン
18：Ｔｉ／Ｐｔ／Ａｕ層
19：ゲート絶縁膜
20：ゲート電極
21：ソース電極
22：ドレイン電極

【図3】

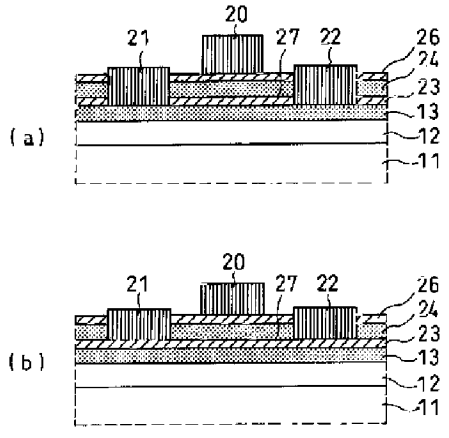
本発明の第２の実施の形態のＭＩＳＦＥＴの断面図



11：半絶縁性ＧａＡｓ基板
12：p⁻型ＧａＡｓ層
13：ＧａＳ層
20：ゲート電極
21：ソース電極
22：ドレイン電極
23：ＧａＮ層
24：ＧａＳ層
25：ゲート絶縁膜

【図4】

本発明の第３の実施の形態のＭＩＳＦＥＴの断面図

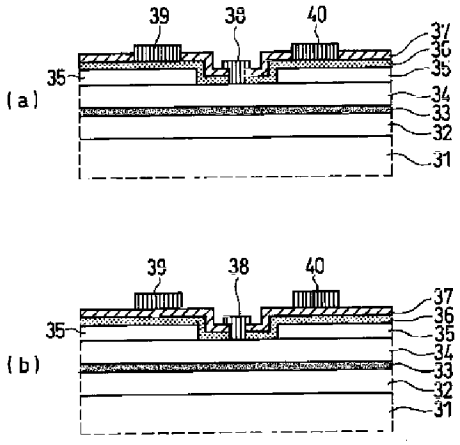


11：半絶縁性ＧａＡｓ基板
12：p⁻型ＧａＡｓ層
13：ＧａＳ層
20：ゲート電極
21：ソース電極
22：ドレイン電極
23：ＧａＮ層
24：ＧａＳ層
26：ＧａＮ層
27：ゲート絶縁膜

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【図5】

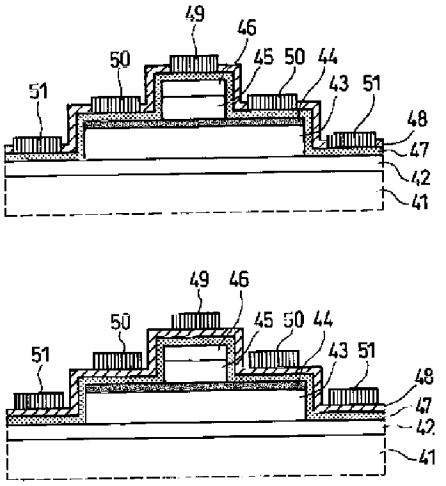
本発明の第４の実施の形態のＨＥＭＴの断面図



３１：半絶縁性ＧａＡｓ基板
３２：ｉ型ＧａＡｓバッファ層
３３：ｉ型ＩｎＧａＡｓチャネル層
３４：ｎ型ＩｎＧａＰキャリア供給層
３５：n^+型ＧａＡｓコンタクト層
３６：ＧａＳ層
３７：ＧａＮ層
３８：ゲート電極
３９：ソース電極
４０：ドレイン電極

【図6】

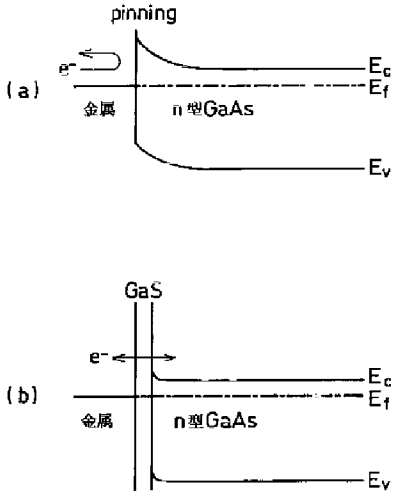
本発明の第５の実施の形態のＨＢＴの断面図



４１：半絶縁性ＧａＡｓ基板
４２：n^+型ＧａＡｓサブコレクタ層
４３：ｎ型ＧａＡｓコレクタ層
４４：p^+型ＧａＡｓベース層
４５：ｎ型ＩｎＧａＰエミッタ層
４６：n^+型ＧａＡｓエミッタキャップ層
４７：ＧａＳ層
４８：ＧａＮ層
４９：エミッタ電極
５０：ベース電極
５１：コレクタ電極

【図7】

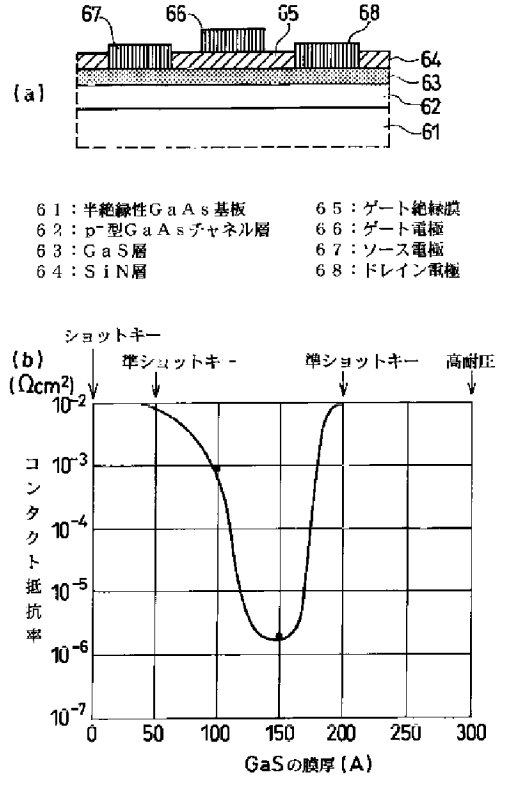
ＧａＡｓにおけるピンニング効果とその防止法の説明図



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【図8】

従来の改良型ＭＩＳＦＥＴの構造とコンタクト抵抗率の説明図



６１：半絶縁性ＧａＡｓ基板
６２：p⁻型ＧａＡｓチャネル層
６３：ＧａＳ層
６４：ＳｉＮ層
６５：ゲート絶縁膜
６６：ゲート電極
６７：ソース電極
６８：ドレイン電極

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ED02 ED03 FC05 FC25
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GJ05 GK05 GL04 GL05 GM04
GN05 GQ01 GS02 GT03 HC01
HC19

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JP2000174261A COMPOUND SEMICONDUCTOR DEVICE

Applicants: FUJITSU LTD

Inventors: OKAMOTO NAOYA,TAKAHASHI TAKESHI

Classifications:

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CPC H01L29/2003 (EP);

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Application: JP2000174261A·1998-12-02

Publication: JP2000174261A·2000-06-23

Published as: JP2000174261A;**JP4228250B2**

COMPOUND SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To cancel the pinning effect and reduce the interface level density and the Ohmic resistance by covering the surface of a compd. semiconductor layer with a GaS-contg. layer thicker than a diatomic layer and covering a part thereof with GaN. SOLUTION: The surface of a compd. semiconductor layer 2 is covered with a layer 3 contg. at least GaS to reduce the interface level density and cancel the pinning, and its film thickness is set to be larger than a diatomic layer to raise the thermal stability and reduce the contact resistance. The layer 3 may be a III-VI compd. semiconductor layer such as a GaS layer, AlGaS layer, and GaSSe layer or a layer contg. a metal element added to them. The layer 3 may be covered with a GaN layer 4, instead of SiN layer, thereby making the manufacturing apparatus commonly usable. This simplifies the manufacturing process and improves the throughput. For esp. growing the compd. semiconductor layer 2 on a semi-insulative compd. semiconductor substrate 1, this layer 2, the layer 3 contg. at least GaS and the GaN layer 4 can be formed by the same manufacturing apparatus.

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DESCRIPTION JP2000174261

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a compound semiconductor device, and is particularly characterized by the structure of an interface protective film for reducing the interface state density and the contact resistance of a compound semiconductor MISFET or the like. The present invention relates to a compound semiconductor device.

[0002]

2. Description of the Related Art Compound semiconductor field effect transistors such as MESFETs (Schottky barrier gate FETs) and HEMTs (high electron mobility transistors) and compound semiconductor devices such as HBTs (heterojunction bipolar transistors) are used as high frequency operating elements. As one of the high frequency applications, there are, for example, high-power FETs used for power amplifiers for transmission of mobile phone base stations, microwave and millimeter wave amplifiers for mobile phones, and further for optical communication. It is expected to be applied to the signal processing circuit, etc.

[0003]

However, in the compound semiconductor device, it has been difficult to form an insulating film interface having a low interface state density such as a SiO2 film with respect to Si.

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For example, as an insulating film for GaAs, an insulating film such as SiN, SiO2, or Ga2 O3 has been studied. However, since GaAs has a unique interface state that causes pinning, the interface state density is Since it is difficult to reduce the amount, MISFETs have not been put to practical use in III-V group compound semiconductors such as GaAs, and interface problems have been avoided in MESFETs and HEMT structures. The normal interface state density in the compound semiconductor is about 1013 to 1014 eV-1 cm-2.

[0004]

Here, the pinning effect in GaAs will be described with reference to FIG. Reference is made to FIG. 7A. FIG. 7A is a band diagram when a metal and n-type GaAs are bonded, and no matter what kind of metal is bonded to GaAs, a detailed causal relationship is shown. Although it has not been clarified, there is a certain band bending that does not depend on the type of metal due to the pinning effect, which results in a constant barrier height and rectification characteristics at the semiconductor / metal interface, and the resistance of ohmic contact to n-type GaAs is increased. Tends to be higher.

[0005]
In order to improve such pinning effect, the GaAs surface is treated in a solution of (NH4) 2Sx or Na2S to terminate the dangling bond on the GaAs surface with S (sulfur). Alternatively (see JP-A-4-199518, if necessary), or the GaAs surface is treated with H2 S gas, and dangling bonds on the GaAs surface are terminated with S (if necessary, JP-A-2-1995). 170417) are known.

[0006]
In this way, the surface is stabilized by the Ga-S bond formed by terminating the dangling bond on the GaAs surface with S, and the PL (photoluminescence) intensity is increased and the barrier height depends on the metal work function. This situation will be described with reference to FIG. 7B.

[0007]
See FIG. 7B. FIG. 7B is a band diagram in the case where the surface of n-type GaAs is terminated by S and then a metal is joined, and the presence of GaS formed by the termination causes the surface of the n-type GaAs to be , The Schottky barrier that reflects the work function of the metal is formed, and when a metal having a low barrier height, for example, Ti, is selected, band bending on the surface of the n-type GaAs is reduced, and the metal and the n-type GaAs are reduced. And will be ohmic-connected via the tunnel current in GaS.

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[0008]

However, since the GaS layer formed by terminating with S is an extremely thin film of one atomic layer (monolayer), it is difficult to keep the surface stabilized by the S treatment as it is. There is.

For example, when a SiN film or a SiO2 film is deposited as a surface protection film on the S-treated GaAs surface, there is a problem that the PL intensity is significantly reduced and the effect of releasing pinning is reduced.

[0009]
When a metal is deposited on the surface of S-treated GaAs to form an ohmic electrode, the metal and GaAs react with the heat treatment to rapidly change the Schottky characteristics, resulting in the formation of the ohmic electrode. At the same time, there is a problem that the effect of canceling pinning decreases.

[0010]

In order to improve such stability in S treatment, particularly thermal stability, the present inventors have formed by sublimation of tert-butyl gallium sulfacuben [[(t-Bu) GaS) 4]. It has been proposed that the pinning of the GaAs surface be released by using a thick amorphous GaS layer having a thickness of about 30 nm as a gate insulating film to form a compound semiconductor MISFET (if necessary, see Japanese Patent Laid-Open No. 10-98185). ..

Although the GaS layer is made amorphous in order to relax lattice mismatch with GaAs, when GaS is crystallized, it has a cubic crystal structure with a composition ratio of 1: 1.

[0011]
Furthermore, since the present inventors have proposed that such pinning cancellation by a thick GaS layer is used for forming an ohmic electrode (see Japanese Patent Application No. 9-351633, if necessary). Such an improved MISFET will be described with reference to FIG.

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[0012]
Reference is made to FIG. 8A. FIG. 8A is a cross-sectional view of a conventional improved MISFET. First, C () is formed on the semi-insulating GaAs substrate 61 by MOVPE method (metal organic chemical vapor deposition method). After epitaxially growing a p-type GaAs channel layer 62 having a carbon concentration of 3 × 10 15 cm −3 and a thickness of 300 nm (=3000 Å), sublimate tert-butyl gallium sulfacuben, which is a solid raw material, in a vacuum. To deposit a GaS layer 63 having a thickness of 5 nm to 20 nm, and then depositing a SiN layer 64 having a thickness of 50 nm by a plasma enhanced CVD method.

[0013]

Then, using the resist pattern (not shown) as a mask, etching is performed using buffered hydrofluoric acid to selectively remove the exposed SiN layer 64 to form openings for forming source / drain electrodes. After that, the resist pattern is removed, and then a gate electrode 66, a source electrode 67, and a drain electrode 68 made of a Ti / Pt / Au layer are formed by a lift-off method using a new resist pattern (not shown). This completes the basic structure of the compound semiconductor MISFET.

The gate insulating film 65 in this case has a two-layer structure of the GaS layer 63 and the SiN layer 64.

[0014]
In such an improved MISFET, since the source electrode 67 and the drain electrode 68 are provided through the GaS layer which is considerably thicker than that of the monolayer, the pinning effect on the surface of the p--type GaAs channel layer 62 is canceled. As a result, a low resistance ohmic contact can be formed.

[0015]

The dependence of the contact resistivity on the GaS film thickness in this case has already been disclosed in the above-mentioned Japanese Patent Application No. 9-351633, but this situation will be described again with reference to FIG.

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See FIG. 8 (b). FIG. 8 (b) shows the contact resistivity (Ω · cm2) when a Ti electrode is formed on GaAs by changing the film thickness of the GaS layer and then heat-treated at 300 ° C. for 10 minutes. It is a figure which shows the measurement result, and a resistivity becomes about 150 Å (= 15 nm) minimum from a high-resistance Schottky barrier with a film thickness of 0 Å, through a quasi-Schottky barrier, and the film thickness is It becomes a quasi-Schottky barrier again at about 20 nm, and becomes a high resistance insulating film at more than 20 nm.

Therefore, by appropriately selecting the film thickness of the GaS layer, it can be used as both an insulating film and a film for reducing contact resistance.

The film thickness of the GaS layer in this case is the film thickness at the time of deposition, and a reaction layer that has reacted with Ti by heat treatment is formed on the Ti electrode side, and the actual film thickness is smaller than this value. Thought to be a thing.

[0016]
However, when the gate insulating film is composed of only the GaS layer like the MISFET disclosed in Japanese Patent Application Laid-Open No. 10-98185, if the GaS layer to be the gate insulating film is thinned. , The low breakdown voltage of the GaS layer causes a problem that a large leak current flows in the MIS structure portion.

[0017]
In addition, in the improved MISFET shown in FIG. 8A, in the heat treatment process for forming the ohmic electrode, the reaction between the GaS layer and the metal electrode progresses and the ohmic characteristics are maximized. There is a range of heat treatment time depending on the thickness, and there is a problem that the characteristics deteriorate when the reaction is excessive. Therefore, when the GaS layer is used as an insulating film and a film for reducing the contact resistance at the same time, the film of the GaS layer is formed. Regarding the thickness, there is a trade-off relationship between the insulating film and the contact resistance reduction, the film thickness to be adopted becomes a problem, and the heat treatment time also has a problem, so that the process flexibility is limited. There is a problem that

[0018]
Further, in the improved MISFET shown in FIG. 8A, the growth apparatus for depositing the GaS layer and the SiN layer is completely different, which complicates the manufacturing apparatus configuration and accordingly increases the number of manufacturing steps. Therefore, there is a problem that the throughput is reduced.

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[0019]
Therefore, it is an object of the present invention to cancel the pinning effect in a compound semiconductor, reduce the interface state density, and reduce the ohmic resistance with a simple manufacturing apparatus configuration.

[0020]

FIG. 1 is an explanatory view of the principle configuration of the present invention, and the means for solving the problems in the present invention will be described with reference to FIG.

(1) According to the present invention, in the compound semiconductor device, the surface of the compound semiconductor layer 2 is covered with the layer 3 containing at least GaS and having a thickness of 2 atomic layers or more, and at least a part of the layer 3 containing at least GaS is made of GaN. It is characterized by being covered with layer 4.

[0021]

Thus, by covering the surface of the compound semiconductor layer 2 with the layer 3 containing at least GaS, the interface state density is reduced, pinning is released, and the film thickness is made equal to or more than two atomic layers. By this, the thermal stability can be enhanced, and the contact resistance can be reduced as is apparent from FIG.

The "layer 3 containing at least GaS" means a GaS layer itself, a III-VI group compound semiconductor layer such as an AlGaS layer or a GaSSe layer, or a layer in which other metal elements are mixed.

[0022]

Further, by covering the layer 3 containing at least GaS with the GaN layer 4 instead of the SiN layer, the manufacturing apparatus can be made common, which simplifies the manufacturing process and improves the throughput.

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In particular, when growing the compound semiconductor layer 2 on the semi-insulating compound semiconductor substrate 1, the compound semiconductor layer 2, the layer 3 containing at least GaS, and the GaN layer 4 can be manufactured using the same manufacturing apparatus.

[0023]
Further, by covering the layer 3 containing at least GaS with the GaN layer 4, peeling of the layer 3 containing at least GaS in the plasma ashing process or the like can be prevented, and when the ohmic electrode is provided, at least GaS is contained. It becomes easy to control the film thickness of the layer 3 within the optimum range.

[0024]
(2) Further, the present invention is characterized in that, in the above (1), the GaN layer 4 is further covered with a layer containing at least GaS.

[0025]
In general, it is not easy to deposit the GaN layer 4 thickly on the layer 3 containing at least GaS, so that it is possible to increase the total thickness by further providing a layer containing at least GaS on the GaN layer 4. Therefore, the withstand voltage can be increased.

[0026]
(3) Further, the present invention is characterized in that, in the above (1), the GaN layer 4 is further covered with a layer containing at least GaS, and the surface of the layer containing at least GaS is further covered with a GaN layer.

[0027]
As described above, by using the GaN layer as the uppermost layer, it is possible to improve process instability of the layer containing at least GaS, such as peeling in the plasma ashing step or the like.

[0028]
(4) Further, in any one of the above (1) to (3), the present invention is characterized in that the compound semiconductor layer 2 in contact with the layer 3 containing at least GaS is a III-V

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group compound semiconductor layer. ..

[0029]
In this way, as a compound semiconductor targeted for terminating dangling bonds on the surface by S (sulfur) of the layer 3 containing at least GaS, Inx Aly Ga1-xy Asw P1-W is difficult to reduce the interface state density. Group III-V compound semiconductors such as and nitride compound semiconductors are suitable.

[0030]
(5) Further, the present invention is characterized in that in any one of the above (1) to (4), at least one ohmic electrode is provided so as to be in contact with at least the GaS-containing layer 3 in contact with the compound semiconductor layer 2. And

[0031]

In this way, by providing the ohmic electrodes such as the source electrode 7 and the drain electrode 8 on the surface of the layer 3 containing at least GaS exposed by removing the GaN layer 4 covering the surface, the film of the layer 3 containing at least GaS is formed. Since the thickness can be accurately controlled under the conditions at the time of deposition, the contact resistance can be reduced with good reproducibility.

When applied to an HBT or the like, for example, only the base electrode may be provided on the surface of the layer 3 containing at least GaS, and the emitter electrode or the collector electrode may be directly provided on the surface of the compound semiconductor layer 2.

[0032]
(6) Further, according to the present invention, in any one of the above (1) to (4), at least one ohmic electrode is in contact with the GaN layer 4 covering the layer 3 containing at least GaS in contact with the compound semiconductor layer 2. It is characterized by being provided.

[0033]
As described above, since the GaN layer 4 is generally thin, even if an electrode is provided on the surface of the GaN layer 4, the electrode and the compound semiconductor layer 2 are ohmic-connected via the tunnel current, whereby the contact hole is formed. The number of

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manufacturing steps can be reduced because the forming step of No. 1 is not required.

[0034]
(7) Further, the present invention is characterized in that, in the above (5) or (6), a non-ohmic electrode is provided on the surface of the uppermost layer of the GaN layer 4 to form a metal-insulator-semiconductor structure. To do.

[0035]

As described above, by using the laminated structure of the layer 3 containing at least GaS and the GaN layer 4, the ohmic electrodes such as the source electrode 7 and the drain electrode 8 having a low resistance, the interface state density is low, and the withstand voltage is excellent. Since the metal-insulator-semiconductor structure (MIS structure) can be formed at the same time, the MIS type compound semiconductor device can be realized.

The gate insulating film 5 in this case is a laminated structure film of the layer 3 containing at least GaS and the GaN layer 4.

[0036]

BEST MODE FOR CARRYING OUT THE INVENTION Here, a manufacturing process of a MISFET according to a first embodiment of the present invention will be described with reference to FIG.

Referring to FIG. 2A, first, on the semi-insulating GaAs substrate 11, a p- layer which becomes a channel layer having a thickness of, for example, 300 nm and a carbon concentration of, for example, $3 \times 10\ 15\ cm\ -3$ is formed by using the MOVPE method. After the type GaAs layer 12 is grown, the solid raw material tert-butylgallium sulfacuben is sublimated at a substrate temperature of 350 to 500 ° C., for example, 350 ° C. However, the GaS layer 13 in an amorphous state having a thickness of 2 atomic layers to 20 nm, for example, 10 nm is grown.

[0037]

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Subsequently, in the same chamber, TEGa (triethylgallium) at 0.25 sccm and nitrogen radicals excited by 350 W of high frequency power at 1 sccm were used at a substrate temperature of 400 to 450 ° C., for example, 400 ° C. By flowing, the GaN layer 14 having a thickness of 0.5 to 5 nm, for example, 5 nm is grown on the GaS layer 13.

The growth rate of the GaN layer 14 in this case is about 20 to 40 nm / hour.

[0038]
2B, the GaN layer 14 is selectively removed by wet etching using hot H3 PO4 using the resist pattern 15 having the openings 16 corresponding to the source / drain regions as a mask. To expose the GaS layer 13.

[0039]
2C, after removing the resist pattern 15, a new resist pattern 17 having openings corresponding to the gate electrode and the source / drain electrodes is provided, and a Ti film having a thickness of, for example, 10 nm is formed on the entire surface. A Ti / Pt / Au layer 18 is deposited by sequentially depositing a film, a Pt film with a thickness of eg 30 nm and an Au film with a thickness of eg 300 nm.

[0040]

Next, by removing the resist pattern 17 to lift off the Ti / Pt / Au layer 18 deposited on the resist pattern 17, the gate electrode 20, the source electrode 21, and the drain electrode 22 are referred to. To form.

The gate insulating film 19 in this case has a laminated structure of the GaS layer 13 and the GaN layer 14.

[0041]
In the MISFET according to the first embodiment, the GaS layer 13 is provided so as to be in contact with the p-type GaAs layer 12, so that the interface state density is reduced to 10 11 eV - 1 cm -2 or less by the termination effect of the GaS layer 13. It is possible to form an inversion layer, that is, an n-type channel layer on the surface of the p-type GaAs layer 12.

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[0042]
Further, since the gate insulating film 19 has a two-layer structure of the GaS layer 13 and the GaN layer 14, the low withstand voltage of the GaS layer 13 can be compensated by the wide-gap GaN layer 14, and the gate insulating film 19 can be insulated. The breakdown voltage can be increased and the leak current can be reduced.

[0043]
The action of the GaN layer 14 in this case is the same as that of the SiN layer 64 shown in FIG. 8A, but the GaN layer 14 is different from the SiN layer 64 in that the GaS layer 13 is continuously operated in the same chamber. Since it can be deposited as a step of, the manufacturing apparatus can be simplified, and a cleaning step or the like when moving between manufacturing apparatuses is not necessary, so that the throughput is improved.

[0044]

Further, since the source electrode 21 and the drain electrode 22 are provided via the GaS layer 13 having a thickness of, for example, 10 nm, the pinning effect can be released and the ohmic electrode having a low contact resistivity can be formed.

Since the film thickness of the GaS layer 13 in this case is determined by the film thickness at the time of film formation, the contact resistivity can be accurately controlled within the optimum range shown in FIG. The semiconductor MISFET can be manufactured with good reproducibility.

[0045]

Next, a MISFET according to a second embodiment of the present invention will be described with reference to FIG.

3A is a cross-sectional view when the ohmic electrode is provided on the GaS layer, and FIG. 3B is a cross-sectional view when the ohmic electrode is provided via the GaN layer. ..

Referring to FIG. 3A, the MOVPE method is used on the semi-insulating GaAs substrate 11 in

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exactly the same manner as in the first embodiment, and the thickness is, for example, 300 nm and the carbon concentration is, for example, 300 nm. After growing the p-type GaAs layer 12 serving as a channel layer of 3 × 10 15 cm -3, the tertiary butyl gallium sulfacuben stored in the chamber is added to the substrate at 350 to 500 ° C, for example, 350 ° C. By sublimation at a temperature, the GaS layer 13 in an amorphous state having a thickness of 2 atomic layers to 20 nm, for example, 10 nm is grown.

[0046]
Subsequently, in the same chamber, at a substrate temperature of 400 to 450 ° C., for example, at 400 ° C., 0.25 sccm of TEGa and 1 sccm of nitrogen radicals excited by high-frequency power of 350 W are caused to flow, A GaN layer 23 having a thickness of 0.5 to 5 nm, for example, 2 nm, is grown on the GaS layer 13.

[0047]
Subsequently, in the same chamber, tert-butyl gallium sulfacuben is sublimed at a substrate temperature of 350 to 500 ° C., for example 350 ° C. to give a thickness of 2 atomic layers to 20 nm, for example 10 nm. The GaS layer 24 in the amorphous state is grown.

[0048]
Then, the GaS layer 24 is selectively removed by performing wet etching using a mixed solution of H3 PO4 + HCl using a resist pattern (not shown) having openings corresponding to the source / drain regions as a mask. To expose the GaN layer 23, and then wet etching using hot H3 PO4 is performed to selectively remove the GaN layer 23 to expose the GaS layer 13.

[0049]

After that, just as in the first embodiment, after removing the resist pattern, a new resist pattern having openings corresponding to the gate electrode and the source / drain electrodes is provided, and the entire surface has a thickness of For example, a Ti / Pt / Au layer is deposited by sequentially depositing a Ti film of 10 nm, a Pt film of 30 nm in thickness, and an Au film of 300 nm in thickness, and then a resist pattern. Is removed and the Ti / Pt / Au layer deposited on the resist pattern is lifted off to form the gate electrode 20, the source electrode 21, and the drain electrode 22.

In this case, the gate insulating film 25 has a laminated structure of GaS layer 13 / GaN layer 23

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/ GaS layer 24.

[0050]
The device characteristics of the MISFET of the second embodiment are basically the same as those of the first embodiment described above, but in the process of depositing the GaN layer at a relatively low temperature, the device characteristics of the first embodiment described above are obtained. Since it is generally not easy to deposit a thick layer like the GaN layer 13, instead of thinning the GaN layer 23, the total thickness of the GaS layer is made thicker to increase the gate breakdown voltage.

[0051]
In this case, it is conceivable that the GaS layer 13 is set to 20 nm and the GaS layer 24 is omitted. In that case, the thickness of the GaS layer 24 in the source / drain regions becomes too thick and the contact resistivity becomes too high. Since the thin GaN layer 23 is used as an etching stopper in the second embodiment, the contact resistivity can be accurately controlled within the optimum range shown in FIG. The MISFET can be manufactured with good reproducibility.

[0052]
Refer to FIG. 3 (b) The MISFET shown in FIG. 3 (b) is a modification of FIG. 3 (a), and the film forming process is the same as in the case of FIG. 3 (a). When the opening corresponding to the drain region is formed, only the GaS layer 24 is removed, the thin GaN layer 23 is left as it is, and the source electrode 21 and the drain electrode 22 are provided on the surface of the GaN layer 23. Is.

[0053]

In this case, since the GaN layer 23 is very thin, about 2 nm, the source electrode 21 and the drain electrode 22 and the p-type GaAs layer 12 are ohmic-connected via the tunnel current.

By adopting such a configuration, the step of etching the GaN layer 23 is unnecessary, so that the number of manufacturing steps can be reduced and the throughput can be improved.

[0054]

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Next, a MISFET according to a third embodiment of the present invention will be described with reference to FIG.

4A is a cross-sectional view when the ohmic electrode is provided on the GaS layer, and FIG. 4B is a cross-sectional view when the ohmic electrode is provided via the GaN layer. ..

Referring to FIG. 4A, the MOVPE method is used on the semi-insulating GaAs substrate 11 in exactly the same manner as in the first embodiment, and the thickness is, for example, 300 nm and the carbon concentration is, for example, 300 nm. After growing the p-type GaAs layer 12 serving as a channel layer of 3 × 10 15 cm -3, the tertiary butyl gallium sulfacuben stored in the chamber is added to the substrate at 350 to 500 ° C, for example, 350 ° C. By sublimation at a temperature, the GaS layer 13 in an amorphous state having a thickness of 2 atomic layers to 20 nm, for example, 10 nm is grown.

[0055]
Subsequently, in the same chamber, at a substrate temperature of 400 to 450 ° C., for example, at 400 ° C., 0.25 sccm of TEGa and 1 sccm of nitrogen radicals excited by high-frequency power of 350 W are caused to flow, A GaN layer 23 having a thickness of 0.5 to 5 nm, for example, 2 nm, is grown on the GaS layer 13.

[0056]
Subsequently, in the same chamber, tert-butyl gallium sulfacuben is sublimed at a substrate temperature of 350 to 500 ° C., for example 350 ° C. to give a thickness of 2 atomic layers to 20 nm, for example 10 nm. After growing the GaS layer 24 in the amorphous state, the TEGa of 0.25 sccm and the high frequency of 350 W are continuously generated in the same chamber at a substrate temperature of 400 to 450 ° C, for example, 400 ° C. By flowing nitrogen radicals excited by electric power at 1 sccm, the GaN layer 26 having a thickness of 0.5 to 5 nm, for example, 2 nm is grown on the GaS layer 24.

[0057]
Then, the GaN layer 26 is selectively removed by performing wet etching using hot H3 PO4 using a resist pattern (not shown) having openings corresponding to the source / drain regions as a mask. After exposing 24, the GaS layer 24 is selectively removed to expose the GaN layer 23 by wet etching using a mixture of H3 PO4 + HCl, and then hot H3 PO4 is used again. The wet

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etching is performed to selectively remove the GaN layer 23 to expose the GaS layer 13.

[0058]

After that, just as in the first embodiment, after removing the resist pattern, a new resist pattern having openings corresponding to the gate electrode and the source / drain electrodes is provided, and the entire surface has a thickness of For example, a Ti / Pt / Au layer is deposited by sequentially depositing a Ti film of 10 nm, a Pt film of 30 nm in thickness, and an Au film of 300 nm in thickness, and then a resist pattern. Is removed and the Ti / Pt / Au layer deposited on the resist pattern is lifted off to form the gate electrode 20, the source electrode 21, and the drain electrode 22.

In this case, the gate insulating film 27 has a laminated structure of GaS layer 13 / GaN layer 23 / GaS layer 24 / GaN layer 26.

[0059]

The device characteristics of the MISFET of the third embodiment are basically the same as those of the second embodiment, but the GaS layer 24 is easily peeled off in the plasma ashing process for removing the resist pattern. Since there is process instability, providing the GaN layer 26 as the uppermost layer improves the process stability.

Further, by providing the GaN layer 26, the withstand voltage of the gate is further improved.

[0060]

Further, also in the third embodiment, since the lower GaN layer 23 is used as an etching stopper, the contact resistivity can be accurately controlled within the optimum range shown in FIG. 8B. Thereby, the compound semiconductor MISFET can be manufactured with good reproducibility.

[0061]

Refer to FIG. 4 (b) The MISFET shown in FIG. 4 (b) is a modification of FIG. 4 (a) and corresponds to the MISFET of FIG. 3 (b). Although the description is omitted because it is similar to the case,

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the thin GaN layer 23 is left as it is, only by removing the GaN layer 26 and the GaS layer 24 when forming the openings corresponding to the source / drain regions. A source electrode 21 and a drain electrode 22 are provided on the surface of the GaN layer 23.

[0062]

Also in this case, since the GaN layer 23 is very thin, about 2 nm, the source electrode 21 and the drain electrode 22 and the p-type GaAs layer 12 are ohmic-connected via the tunnel current.

By adopting such a configuration, the step of etching the GaN layer 23 is unnecessary, so that the number of manufacturing steps can be reduced and the throughput can be improved.

[0063]

Next, a HEMT according to a fourth embodiment of the present invention will be described with reference to FIG.

5A is a cross-sectional view of the HEMT when the ohmic electrode is provided on the GaS layer, and FIG. 5B is a HEMT when the ohmic electrode is provided via the GaN layer. FIG.

5 (a). First, on the semi-insulating GaAs substrate 31, TEGa (triethylgallium), AsH3, and H2 as a carrier gas are caused to flow on the semi-insulating GaAs substrate 31 by using an undoped layer having a thickness of, for example, 500 nm. After growing the i-type GaAs buffer layer 32, the TMIn (trimethylindium) is added to form a non-doped i-type InGaAs channel layer 32 having a thickness of, for example, 14 nm and an In composition ratio of 0.2. Then, AsH3 is switched to PH3 and SiH4 is added as an impurity source. For example, an n-type InGaP carrier having a thickness of 25 nm, a Si concentration of 2 × 10 18 cm -3, and an In composition ratio of 0.49 is deposited. The supply layer 33 is grown, then the supply of TMIn is stopped, PH3 is replaced with AsH3 again, and the thickness is, for example, 70 nm, and the Si concentration is, for example, 5 × 10 18 cm -3, n + type GaAs contact. Deposit layer 35.

[0064]

Next, the n + type GaAs contact layer 35 is patterned by wet etching using a mixed solution of H3

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PO4 + H2 O2 + H2 O so as to correspond to the source / drain regions to form a gate recess, and then in the GaS deposition chamber. And subliming tert-butyl gallium sulfacuben in the chamber at a substrate temperature of 350 to 500 ° C., for example 350 ° C. to give a thickness of 2 atomic layers to 20 nm, for example 10 nm. The GaS layer 36 in an amorphous state is grown, and subsequently, TEGa is excited by high frequency power of 0.25 sccm and 350 W in the same chamber at a substrate temperature of 400 to 450 ° C., for example, 400 ° C. By flowing the nitrogen radicals described above at 1 sccm, the GaN layer 37 having a thickness of 0.5 to 5 nm, for example, 2 nm is grown on the GaS layer 36.

[0065]
Then, the GaN layer 37 is selectively removed by performing wet etching using hot H3 PO4 using a resist pattern (not shown) having an opening for forming a gate as a mask, and then mixing H3 PO4 and HCl. The GaS layer 36 is selectively removed by performing wet etching using a liquid.

[0066]
Next, after removing the resist pattern, the GaN layer 37 is selectively etched by performing wet etching using hot H3PO4 with a new resist pattern (not shown) having openings corresponding to the source / drain regions as a mask. After the removal, the source electrode 39 and the drain electrode 40 are formed by vapor-depositing an Al film having a thickness of, for example, 500 nm and lifting off together with the resist pattern.

[0067]
Then, after removing the resist pattern, a new resist pattern (not shown) having an opening for forming a gate electrode is provided, and an Al film having a thickness of, for example, 500 nm is vapor-deposited on the entire surface to form a resist pattern together with the resist pattern. The basic structure of the HEMT is completed by lifting off and forming the gate electrode 38.

[0068]
In the HEMT according to the fourth embodiment of the present invention, since the channel region of the surface of the n-type InGaP carrier supply layer 34 except the portion in contact with the gate electrode 38 is covered with the GaS layer 36, n The dangling bond on the surface of the type InGaP carrier supply layer 34 can be terminated by S to be stabilized, and the interface state density can be reduced thereby, so that the operation of the HEMT can be stabilized.

[0069]

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Also in this case, since the source electrode 39 and the drain electrode 40 are provided through the GaS layer 36 having a film thickness of about 10 nm, the source electrode 39 and the drain electrode 40 can be low resistance ohmic electrodes.

[0070]
In addition, in the fourth embodiment, since the surface of the GaS layer 36 is covered with the GaN layer 37, the GaS layer 36 does not peel off when plasma ashing is performed to remove the resist pattern. , Process stability is improved.

[0071]
Refer to FIG. 5 (b) The HEMT shown in FIG. 5 (b) is a modification of FIG. 5 (a), and the film forming process is the same as in the case of FIG. 5 (a). Since the source electrode 39 and the drain electrode 40 are provided through the layer 37 and only the opening for forming the gate is required to be provided, the number of etching steps can be reduced and throughput can be improved.

[0072]

Further, in this case, since the gate electrode 38, the source electrode 39, and the drain electrode 40 can be formed by one film forming step and lift-off step, the number of manufacturing steps can be further reduced.

Since the GaN layer 37 is as thin as about 2 nm, the source electrode 39 and the drain electrode 40 and the n + -type GaAs contact layer 35 are ohmic-connected via the tunnel current.

[0073]

Next, an HBT according to a fifth embodiment of the present invention will be described with reference to FIG.

6A is a cross-sectional view of the HBT when the ohmic electrode is provided on the GaS layer, and FIG. 6B is the HBT when the ohmic electrode is provided via the GaN layer. FIG.

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See FIG. 6A. First, on the semi-insulating GaAs substrate 41, TEGa, AsH3, SiH4 as an impurity source, and H2 as a carrier gas are caused to flow by MOVPE method. , An n + -type GaAs subcollector layer 42 having a Si concentration of 3 × 10 18 cm −3, and an n-type GaAs collector layer 43 having a thickness of 450 nm and a Si concentration of 3 × 10 16 cm −3 are sequentially deposited.

[0074]

Then, SiH4 is switched to CBr4, for example, a p + type GaAs base layer 44 having a thickness of 70 nm and a C concentration of 4 × 10 19 cm -3 is deposited, and then CBr4 is switched to SiH4 again and AsH3 is changed to PH3. Then, TMIn is supplied to deposit an n-type InGaP emitter layer 45 having a thickness of 50 nm, a Si concentration of 3 × 10 17 cm −3, and an In composition ratio of 0.49, and then TMIn is supplied. Is stopped and PH3 is switched to AsH3 to deposit an n + type GaAs emitter cap layer 46 having a thickness of 200 nm, for example.

The n + type GaAs emitter cap layer 46 has a Si concentration of 3 × 10 17 cm −3 at a portion having a thickness of 150 nm on the n type InGaP emitter layer 45 side, and the remaining Si portion having a thickness of 50 nm on the upper side. The concentration is 3 × 10 18 cm -3.

[0075]

Next, mesa etching is performed to form an emitter mesa composed of the n + type GaAs emitter cap layer 46 and the n type InGaP emitter layer 45, and then mesa etching is performed again to form the p + type GaAs base layer 44 and n. A base mesa composed of the type GaAs collector layer 43 is formed.

In this mesa etching step, a mixed solution of H3 PO4 + H2 O2 + H2 O is used for etching the GaAs layer, and a mixed solution of H3 PO4 and HCl is used for etching InGaP. In the case of integrating this HBT, , Mesa etching is performed to reach the semi-insulating GaAs substrate 41 for element isolation to form a collector mesa.

[0076]

The substrate is then housed in a GaS deposition chamber and tert-butyl gallium sulfacuben is

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sublimed in the chamber at a substrate temperature of 350-500 ° C, for example 350 ° C, to give a thickness of 2 Amorphous GaS layer 47 having an atomic layer of 20 nm, for example, 10 nm is grown, and subsequently, TEGa is 0.25 sccm in the same chamber at a substrate temperature of 400 to 450 ° C, for example, 400 ° C. , And a nitrogen radical excited by a high-frequency power of 350 W is caused to flow at 1 sccm to grow a GaN layer 48 having a thickness of 0.5 to 5 nm, for example, 2 nm on the GaS layer 47.

[0077]
Then, the GaN layer 48 is selectively removed by performing wet etching using hot H3 PO4 using a resist pattern (not shown) provided with an opening for forming a base electrode as a mask, and then the entire surface is reduced in thickness. A 20 nm Pt film and a 150 nm Au film are sequentially deposited and removed together with the resist pattern to form the base electrode 50.

[0078]
Then, after removing the resist pattern, a new resist pattern (not shown) having openings for forming an emitter electrode and a collector electrode is provided, and wet etching using hot H3 PO4 is performed using this resist pattern as a mask. Then, after selectively removing the GaN layer 48, a Ti film having a thickness of 10 nm, a Pt film having a thickness of 30 nm, and an Au film having a thickness of 300 nm are sequentially deposited on the entire surface, and lift-off is performed together with the resist pattern. Then, the emitter electrode 49 and the drain electrode 51 are formed to complete the basic structure of the HBT.

[0079]
In the HBT according to the fifth embodiment of the present invention, the exposed surface of the p + -type GaAs base layer 44 and the side surface of the n-type InGaP emitter layer 45 are covered with the GaS layer 47, so that there is a gap between the base and the emitter. The region near the pn junction is terminated by S to reduce the interface state density, and thereby surface recombination in the pn junction region is suppressed, so that the current gain can be increased.

[0080]
Also in this case, since the emitter electrode 49, the base electrode 50, and the collector electrode 51 are provided via the GaS layer 36 having a film thickness of about 10 nm, the emitter electrode 49, the base electrode 50, and the collector electrode 51 are also provided. Can be a low resistance ohmic electrode.

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[0081]
Further, also in the fifth embodiment, since the surface of the GaS layer 47 is covered with the GaN layer 48, the GaS layer 47 is not peeled off in the plasma ashing step for removing the resist pattern, Process stability is improved.

[0082]

Reference is made to FIG. 6B. The HBT shown in FIG. 6B is a modification of FIG. 6A, and the film forming process is the same as in the case of FIG. Since the emitter electrode 49, the base electrode 50, and the collector electrode 51 are provided via the layer 48, it is not necessary to remove the GaN layer 48, so that the etching process can be reduced and the throughput is improved.

Since the GaN layer 48 is very thin, about 2 nm, the emitter electrode 49, the base electrode 50, and the collector electrode 51 become ohmic electrodes due to the tunnel current.

[0083]

Although the respective embodiments of the present invention have been described above, the present invention is not limited to the configurations described in the respective embodiments, and various modifications can be made.

For example, in the above-described first to third embodiments, the semi-insulating GaAs substrate 11 is used as a starting material, and the p $^{-}$ -type GaAs layer 12, the GaS layer 13, and the GaN layers 13 and 23 are provided on the starting material. Although the film is formed by a series of growth steps, an epitaxial wafer in which the p-type GaAs layer 12 is grown on the semi-insulating GaAs substrate 11 may be used as a starting material.

[0084]
When such an epitaxial wafer is used, the surface of the epitaxial wafer is naturally treated by performing treatment with trisdimethylaminoarsine in the GaS deposition chamber at a substrate temperature of, for example, 500 ° C. for 10 minutes. The oxide film is removed, and subsequently, by using HCl gas, for example, at a substrate temperature of 500 ° C., the surface

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of the p--type GaAs layer 12 is etched by several atomic layers to clean the surface. After conversion, the GaS layer 13 and the like may be deposited.

[0085]
In addition, it is desirable that such a cleaning step be performed before the film forming step of the GaS layers 36 and 47 performed after the semiconductor layer etching step in the fourth and fifth embodiments. In the embodiment, the surface of the n-type InGaP carrier supply layer 34 is also removed by several atomic layers.

[0086]
Further, in the first to third embodiments described above, the source electrode 21 and the drain electrode 22 are provided on the GaS layer 13 or via the GaN layer 23, but the GaS layer 13 is also selectively. An alloy type ohmic electrode such as a three-layer structure film composed of a 20 nm Au.Ge film / 5 nm Ni film / 300 nm Au film may be formed in a separate step from the gate electrode 20. The same applies to the case of the emitter electrode 49 and the collector electrode 51 of the fifth embodiment described above.

[0087]
Further, in the above-described fourth embodiment, the HEMT is described, but by replacing the i-type InGaAs channel layer 33 with an n-type InGaAs channel layer, it becomes possible to operate as a MESFET, and the present invention is Such MESFET is also targeted.

[0088]
Further, in each of the above-described embodiments, the GaS layer is formed by using tert-butyl gallium sulfacuben, but the present invention is not limited to tert-butyl gallium sulfacuben, and 2 [(tBu) 2 Ga (μ-SH)] 2 may be used.

[0089]
Further, in each of the above-described embodiments, the main purpose is to stabilize the surface of GaAs in which the pinning effect is remarkably exhibited. However, as in the fourth and fifth embodiments described above, it is also possible to stabilize the surface of InGaP. Even if the pinning effect is not directly canceled, the interface state density can be reduced by terminating the surface dangling bond with S, which contributes to the improvement of the device characteristics. Therefore, it can also be used for the surface stabilization of other III-V group compound semiconductors represented by Inx Aly Ga1-xy Asw P1-W and Inx Aly Ga1-xy Asw N1-w. It is a thing.

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[0090]
Further, in each of the above-described embodiments, the layer for surface stabilization is described as a GaS layer, but the layer is not limited to a pure GaS layer, and a III-VI group compound semiconductor such as AlGaS or GaSSe may be used. Alternatively, a GaS layer or the like in which a metal component is doped or alloyed by a solid phase diffusion reaction with an ohmic electrode may be used.

[0091]
Further, in each of the above-described embodiments, the GaS layer is regarded as an insulator and effectively ohmicized by the tunnel current. However, it does not necessarily have to be purely insulative, and the GaS layer is not necessarily insulative. The metal component may be doped by the solid phase diffusion reaction so that it may have some conductivity.

[0092]
Further, the thickness of the GaS layer in each of the above-described embodiments is set to 2 atomic layers to 20 nm, but it is more preferable that the thickness is 5 nm or more in order to increase thermal stability. When the GaS layer is removed to form the ohmic electrode, the GaS layer acts purely as an insulator, so that the film thickness may be 20 nm or more.

[0093]
According to the present invention, the surface of the compound semiconductor layer such as GaAs is covered with the two-layer structure film of GaS layer and GaN layer having a thickness of at least two atomic layers. Can be stabilized so as not to change even in the subsequent heat treatment step, and the manufacturing apparatus can be shared by using the GaN layer. Furthermore, the ohmic electrode can be formed on the GaS layer or via the GaN layer. Since it is possible to reduce the contact resistance of the ohmic electrode and to reduce the etching process, it greatly contributes to high performance and low cost of the compound semiconductor device.

[0094]
In particular, when the GaAs layer is used as the compound semiconductor layer, the pinning effect can be canceled and a good inversion layer can be formed, which greatly contributes to the practical application of the compound semiconductor MISFET.

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CLAIMS JP2000174261

1.
A compound semiconductor layer, wherein the surface of the compound semiconductor layer is covered with a layer containing at least GaS and having a thickness of two atomic layers or more, and at least a part of the layer containing at least GaS is covered with a GaN layer.

2.
The compound semiconductor device according to claim 1, wherein the GaN layer is further covered with a layer containing at least GaS.

3.
2. The compound semiconductor device according to claim 1, wherein the GaN layer is further covered with a layer containing at least GaS, and the surface of the layer containing at least GaS is further covered with a GaN layer.

4.
4. The compound semiconductor device according to claim 1, wherein the compound semiconductor layer in contact with the layer containing at least GaS is a III-V group compound semiconductor layer.

5.
5. The compound semiconductor device according to claim 1, wherein at least one ohmic

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electrode is provided so as to be in contact with a layer containing at least GaS in contact with the compound semiconductor layer.

6.

5. The compound semiconductor device according to claim 1, wherein at least one ohmic electrode is provided so as to be in contact with a GaN layer that covers at least a layer containing GaS that is in contact with the compound semiconductor layer.

7.

The compound semiconductor device according to claim 5 or 6, wherein a non-ohmic electrode is provided on the surface of the uppermost layer of the GaN layers to form a metal-insulator-semiconductor structure.

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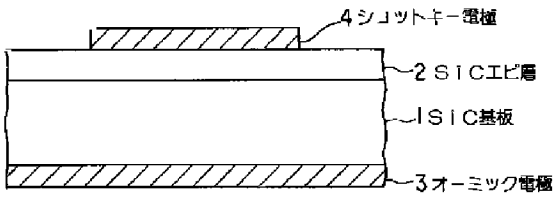
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(71)出願人　000003078
株式会社東芝
神奈川県川崎市幸区堀川町72番地
(72)発明者　滝川　修
神奈川県川崎市幸区小向東芝町１番地　株式会社東芝研究開発センター内
(74)代理人　100058479
弁理士　鈴江　武彦　（外６名）

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(54)【発明の名称】　半導体装置

(57)【要約】
【課題】　ＳｉＣとショットキー電極との反応を抑制してリーク電流の低減をはかる。
【解決手段】　ＳｉＣ１、２と電極との間でショットキー接合が形成された半導体装置において、ショットキー電極４として鉄、ルテニウム、オスミウム、イリジウム、ロジウム又はこれらの合金を用いる。



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【特許請求の範囲】
【請求項１】ＳｉＣと電極との間でショットキー接合が形成された半導体装置において、前記電極として鉄、ルテニウム、オスミウム、イリジウム、ロジウム又はこれらの中から選択された少なくとも２以上の金属の合金を用いることを特徴とする半導体装置。
【請求項２】ＳｉＣと電極との間でショットキー接合が形成された半導体装置において、前記電極としてIII a族の第１の金属と仕事関数が３．９ｅＶ以上の第２の金属との合金を用いることを特徴とする半導体装置。
【請求項３】前記第１の金属としてスカンジウム（Ｓｃ）、前記第２の金属としてIVa族の金属を用いることを特徴とする請求項２に記載の半導体装置。
【請求項４】ＳｉＣと電極との間でショットキー接合が形成された半導体装置において、前記電極としてIVa族どうしの合金を用いることを特徴とする半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、炭化珪素（ＳｉＣ）を用いた半導体装置に関する。
【０００２】
【従来の技術】金属と半導体を接触させたショットキー電極を用いる構造のショットキーダイオードは、半導体中の少数キャリアを使用しないので高速スイッチングができるという特徴がある。しかしながら、シリコンを用いたショットキーダイオードは耐圧が低いという問題がある。これに対して、ＳｉＣを用いたショットキーダイオードは耐圧が高いという特徴を有している。また、ＳｉＣを用いたショットキーダイオードは高温でも動作できることから、大電流が流れるような用途に対して、冷却手段なし或いは小さな冷却装置を用いるだけでよい。
【０００３】ショットキー電極としては例えばチタン（Ｔｉ）等が用いられるが、チタンは高温で熱処理するとＳｉＣと反応し、逆バイアス時のリーク電流が増加するという問題がある。また、デバイスとしてはショットキー電極の他にオーミック電極を形成する必要がある。オーミック電極としては通常ニッケルが用いられるが、良好なオーミック性を生じさせるためには数１００度の温度で熱処理を行う必要がある。このときの熱処理によって、ショットキー電極に前述したようなリーク電流の増加が生じる。オーミック電極を形成した後に熱処理を行い、その後にショットキー電極を形成する方法も考えられるが、この場合にはアニール雰囲気中の不純物によって表面が汚染され、逆にリーク電流が増大するという現象が生じる。
【０００４】一方、ショットキーダイオードを動作させる際には、オン抵抗を下げてオン電流が多くなるようにすることが好ましい。この場合、半導体と金属との間の電位障壁、いわゆるバリアハイトが低いことが要求される。ショットキー電極としてＴｉを用いた場合、バリアハイトは約１ｅＶ程度である。しかし、大電流を得るためにはさらにバリアハイトを下げることが望ましい。
【０００５】
【発明が解決しようとする課題】このように、ショットキー電極として例えばチタンを用いる場合、高温で熱処理を行うことによりチタンがＳｉＣと反応し、逆バイアス時のリーク電流が増加するいう問題があった。
【０００６】また、ショットキーダイオードのオン電流を増加させるためには、半導体と金属との間のバリアハイトを低くすることが必要であるが、ショットキー電極としてＴｉを用いた場合のバリアハイトは１ｅＶ程度であり、必ずしも満足できるものではなかった。
【０００７】本発明は上記従来の課題に対してなされたものであり、ＳｉＣと電極との間でショットキー接合が形成された半導体装置において、ＳｉＣと電極との反応を抑制してリーク電流を低減することを第１の目的とし、半導体と電極との間のバリアハイトを低くしてオン電流を増大させることを第２の目的としている。
【０００８】
【課題を解決するための手段】本発明は、ＳｉＣと電極との間でショットキー接合が形成された半導体装置において、前記電極として鉄、ルテニウム、オスミウム、イリジウム、ロジウム又はこれらの中から選択された少なくとも２以上の金属の合金を用いることを特徴とする。
【０００９】前記金属はＳｉＣとの反応が少なく、これらの金属をショットキー電極として用いることにより、高温で熱処理を行っても逆バイアス時のリーク電流の増加を抑えることができる。
【００１０】また、本発明は、ＳｉＣと電極との間でショットキー接合が形成された半導体装置において、前記電極としてIII a族（ＳｃやＹ、或いはＬａ等のランタン系、アクチニウム系）の第１の金属と仕事関数が３．９ｅＶ以上の第２の金属との合金を用いることを特徴とする。
【００１１】前記第１の金属としてはＳｃ、前記第２の金属としてはIVa族（Ｔｉ、Ｚｒ、Ｈｆ）の金属を用いることが好ましい。このように、III a族の金属（Ｓｃ等は仕事関数が３．５ｅＶ以下）と仕事関数が３．９ｅＶ以上の金属との合金をショットキー電極として用いることにより、ＳｉＣ（例えば、結晶構造が４Ｈのものでは電子親和力が３．７ｅＶ程度）とのショットキー接合のバリアハイトを低くすることが可能となり、オン電流を増加させることが可能となる。
【００１２】また、本発明は、ＳｉＣと電極との間でショットキー接合が形成された半導体装置において、前記電極としてIVa族（Ｔｉ、Ｚｒ、Ｈｆ）どうしの合金を用いることを特徴とする。
【００１３】このように、IVa族どうしの合金をショットキー電極として用いた場合にも、ＳｉＣとのショットキー接合のバリアハイトを低くすることが可能であり、

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オン電流を増加させることが可能となる。

【0014】

【発明の実施の形態】以下、本発明の実施形態を図面を参照して説明する。

（実施形態1）以下のようにして図1に示すようなショットキーダイオードを作製し、作製したショットキーダイオードの評価等を行った。

【0015】まず、不純物濃度10^{18}／cm^3のn型伝導を示すSiC基板1（厚さ0.2mm）に、不純物濃度5×10^{15}／cm^3のn型SiC層（SiCエピタキシャル層2）10μmをエピタキシャル成長させた基板を準備した。この基板をアンモニア水と過酸化水素水の混合溶液に浸漬し、さらに希ふっ酸水溶液に浸漬するなどして洗浄を行った後、エピタキシャル層2側にショットキー電極4としてFeを1μmの厚さで蒸着した。また、SiC基板1の裏面にオーミック電極3としてNiを1μmの厚さで蒸着した。その後、レジスト塗布、露光、現像、エッチングといったパターニングプロセスを行い、直径0.1mmのFe電極（ショットキー電極4）を形成した。また、比較例として、ショットキー電極としてTiを形成したサンプルも作製した。

【0016】上記のようにして作製した両試料をアルゴン雰囲気中、700℃で熱処理し、ダイオードの逆方向のリーク電流を測定した。その結果、電圧−100Vにおけるリーク電流は、ショットキー電極としてTiを用いた場合は約10^{-4}（A）であったが、Feの場合は10^{-6}（A）以下と小さかった。なお、オーミック電極は、上記熱処理によってほぼオーミック特性を示した。

【0017】ショットキー電極の界面を調べるため、Ti及びFeをそれぞれ10nmの厚さで蒸着したSiC基板を700℃で熱処理し、X線回析を行った。Tiの場合はシリサイドのピークが見られたが、Feではシリサイドはほとんど見られなかった。

【0018】このように、FeとSiCとの反応が少ないことがリーク電流の小さい理由と考えられる。すなわち、Feはシリサイドの生成熱がSiCの生成熱と同程度かそれよりも大きく、SiC中のシリコンと反応してシリサイドを形成するよりも金属として存在するほうが安定である。したがって、熱処理によってSiCと反応しにくいため、リーク電流の増加を抑制することができると考えられる。

【0019】Feを10nmの厚さで形成し、アニールした後にFe上にAlを1μm蒸着した試料についても、上記と同様にリーク電流は小さかった。また、鉄の代わりにルテニウム、オスミウム、イリジウム及びロジウムを用いた試料についても、上記と同様にリーク電流は小さかった。

【0020】（実施形態2）ショットキー電極の種類を換えて、第1の実施形態と同様に図1に示すようなショットキーダイオードを作製し、作製したショットキーダイオードの評価等を行った。

【0021】本実施形態では、ショットキー電極としてTiシリサイド、具体的にはTi_3Si，TiSi及び$TiSi_2$を形成した。形成方法としては、TiとSiをそれぞれ蒸発源とし、Eガン蒸着装置で両者を同時に蒸発させるようにした。このときの基板温度は250℃とした。

【0022】作製した試料に対して、第1の実施形態と同様に熱処理を行った後リーク電流を測定した。その結果、Ti_3Siの場合には10^{-5}（A）台のリーク電流であったが、TiSiでは4×10^{-6}（A）、$TiSi_2$では2×10^{-6}（A）のリーク電流であった。また、界面のX線回析を第1の実施形態と同様に行った。その結果、Ti_3Siでは同定不能なピークが見られたが、それ以外のものではそれぞれのシリサイド以外のピークは見られなかった。Ti_3Siの場合にはリーク電流が若干高くSiCとの反応が若干あるとも考えられるが、他の試料では良好な特性が得られている。なお、シリサイドはアニールによって結晶性が向上しており、これも特性向上に寄与していると考えられる。

【0023】また、Tiシリサイドを100nmの厚さで形成し、その上にTiを1μm形成した場合も、上記と同様にリーク電流を低下することができた。この場合は、Tiシリサイドが厚い場合に比べて、熱処理による密着力の低下を抑制することができた。また、Tiシリサイドの厚さが20nmでも効果が見られた。

【0024】また、Ti以外の金属のシリサイドをショットキー電極に用いて同様に熱処理を行った場合にもリーク電流の増加が少なく、リーク電流は10^{-5}（A）以下であった。

【0025】金属シリサイドをMSi_x（Mは金属）とすると、xの値が1の近傍でシリサイドの生成エネルギーが最低となる。そのため、所定の割合でSiが含まれたシリサイドでは、SiCのSiを奪ってxのより大きな化合物になるよりも、そのままの状態でいるほうが熱的に安定といえる。したがって、シリサイドを用いることにより、熱処理によってSiCと反応しにくくなり、リーク電流の増加を抑制することができると考えられる。

【0026】なお、シリサイドを形成する金属Mとしては、仕事関数が5.2以下のものがSiCに対するバリアの高さが小さく、オン抵抗を下げることができる。金属MとしてはTi以外に、La，Zr，Hf，V，Nb，Ta，Cr，Mo，W，Mn，Re，Ni，Ru，Pd，Lu，Fe，Os，Ir，Co，Rh，Ptがあげられる。また、SiC中のSiとの反応を抑制する観点から、金属シリサイドMSi_x中のSiの割合は所定以上、具体的にはxが0.3以上、さらに好ましくは1以上とすることが好ましい。

【0027】以上、第1及び第2の実施形態について説

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明したが、ショットキー電極としての厚さは１０ｎｍ程度以上が好ましく、また、平面抵抗を下げる或いはボンディング性を向上させるために、実施例中でも説明したように他の金属を積層しても良い。

【００２８】なお、第１及び第２の実施形態ではショットキーダイオードについて説明したが、ＭＥＳＦＥＴなどの他の半導体装置のショットキー電極として用いることも可能である。

【００２９】（実施形態３）以下のようにして図１に示すようなショットキーダイオードを作製し、作製したショットキーダイオードの評価等を行った。

【００３０】まず、不純物濃度10^{18}／ｃｍ^{3}のｎ型伝導を示すＳｉＣ基板１（厚さ０．２ｍｍ）に、不純物濃度5×10^{15}／ｃｍ^{3}のｎ型ＳｉＣ層（ＳｉＣエピタキシャル層２）１０μｍをエピタキシャル成長させた基板を準備した。通常の洗浄方法によって洗浄した後、乾燥酸素中１２００℃で酸化膜を形成した。その後、エピタキシャル層２側をレジストで保護し、反対側の層の酸化膜をふっ酸で溶解した。レジストを除去した後に洗浄を行い、ＳｉＣ基板１の裏面にオーミック電極３としてＮｉを１μｍの厚さで蒸着した。さらに、９５０℃でアニールを行い、オーミック性を確保した。その後、エピタキシャル層２側の酸化膜を溶解してエピタキシャル層２の表面を露出させた。

【００３１】次に、上記の工程を行った基板を蒸着装置にセットし、ショットキー電極となる金属材料を蒸着した。このとき、第１の金属としてＳｃ、第２の金属としてＨｆ或いはＺｒを選び、第１の金属及び第２の金属を同時に蒸着した。基板温度は２００℃とし、両金属の固溶体を形成しやすくさせた。試料としては、Ｓｃ：Ｈｆ或いはＳｃ：Ｚｒの比を、３：２、１：１、９：１としたものを作製した。その後、パターニングを行って直径１００μｍのショットキー電極４を形成した。パターニング後、アルゴン雰囲気中で３００℃、１時間のアニールを行った。

【００３２】第１の金属として用いるＳｃは、シリサイドやカーバイドを形成しやすくＳｉＣに対して十分な密着力が得られるが、仕事関数が小さいのでＳｉＣと接合したときにショットキーバリアを形成することができない。そこで、仕事関数がＳｃよりも大きくかつＳｃと固溶体を形成しやすいＨｆやＺｒを用い、固溶体の仕事関数を増加させることで、ＳｉＣに対し低バリアハイトのショットキーダイオードを形成するようにした。

【００３３】以上のようにして作製したサンプルに対して、電圧と容量の関係からビルトイン電圧を求めバリアハイトを求めた。なお、比較例としてＴｉをショットキー電極としたものも同様に作製し、バリアハイトを求めた。その結果、Ｔｉの場合は０．９ｅＶのバリアハイトであったが、本実施形態の場合には各試料とも０．２～０．８ｅＶの範囲内であった。ばらつきは見られたが、どちらかというとＳｃの割合が少ないほうがバリアハイトの値が大きい傾向であった。

【００３４】また、電極のＸ線回析を行ったところ、本実施形態の試料は単一相であった。また、混合相電極にありがちなアニールにおける相分離などに起因するはがれ等の現象は見られなかった。

【００３５】なお、通常の洗浄、蒸着工程で電極を形成すると界面に薄い酸化膜が形成されやすく、その影響で大きなバリアハイトが観測される場合がある。そこで、界面を清浄化させるために、蒸着前にイオンボンバードメント等を行ったところ、安定した界面を得ることができた。以下、具体的に説明する。

【００３６】ＲＦコイルを備えた蒸着装置にＨｅやＡｒ等の不活性ガス或いは水素や炭化水素等の還元性ガスを微量導入してプラズマを生成し、このプラズマに対して１００Ｖ程度以下の直流電圧を印加してＳｉＣ基板表面に衝突させた。このようなイオンボンバードメント処理を行った後にショットキー電極を形成したもののバリアハイトを評価した。３００℃のアニールを行った後において、イオンボンバードメント処理無しのものはバリアハイトに±０．２ｅＶ程度のばらつきがあったが、イオンボンバードメント処理を行ったものは±０．１ｅＶ以内とばらつきが改善された。

【００３７】また、水素ガスを導入した減圧状態で６００℃の熱処理を行い、その後２００℃でショットキー電極となる金属材料を蒸着した場合も、やはりバリアハイトのばらつきは±０．１ｅＶ以内であった。

【００３８】（実施形態４）第１の金属としてＨｆを、第二の金属としてＴｉを用い、両金属の固溶体をショットキー電極として、第３の実施形態と同様にショットキーダイオードを作製した。Ｈｆ／Ｔｉの比率は９から０．１とした。その結果、バリアハイトは０．３から０．７ｅＶまで連続的に変化させることができた。また、第１の実施形態と同様、電極はがれはなかった。

【００３９】なお、ＺｒとＨｆやＴｉとで固溶体を形成することも有効であり、上述したＨｆ－Ｔｉの他にも、Ｈｆ－Ｚｒ或いはＺｒ－Ｔｉの固溶体を用いることにより、Ｔｉよりも仕事関数を下げることができ、バリアハイトの低いショットキー接合を得ることが可能である。

【００４０】（実施形態５）第１の金属としてＬａを、第２の金属としてＡｌを用い、これらを基板温度２００℃で同時に蒸着して、La_3Al、$LaAl_2$をショットキー電極として用いた２種類のショットキーダイオードを第３の実施形態と同様に作製した。また、比較例として、Ｌａをショットキー電極とした試料も作製した。

【００４１】測定の結果、ＳｉＣとのショットキー接合のバリアハイトは、La_3Alでは０．４ｅＶ、$LaAl_2$では０．６ｅＶであった。また電極に$LaAl_2$を用いた試料に対してアニールを行った。逆方向に１００Ｖの電圧を印加した場合、３００℃のアニールでは１０

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$^{-4}$（Ａ）のリーク電流であったが、８００℃のアニールでは10^{-6}（Ａ）に低下した。なお、電極にＬａのみを用いた試料では８００℃でのアニールによって電極が凝集してしまったが、電極に$LaAl_2$を用いた試料では形状に特に変化は見られなかった。

（実施形態６）第１の金属としてＳｃ、Ｙ或いはランタン系のＬａ，Ｃｅ，Ｇｄ，Ｎｄを用い、第２の金属としてＲｕ，Ａｇ，Ｃｏ，Ｚｎ，Ｃｄ，Ｈｇ，Ｇａ，Ｉｎ，Ｔｌ，Ｓｎ，Ｐｂ，Ｓｂ，Ｂｉ，Ｐｔ，Ａｕを用い、第１の金属／第２の金属の比率が０．３～３の合金をショットキー電極とした。作製方法は第３の実施形態と同様であり、また同様にバリアハイトを評価した。

【００４２】その結果、バリアハイトは０．３～０．８ｅＶの範囲内であった。なお、第２の金属中に不純物元素が１％程度含まれていてもバリアハイトには大きな影響はなかった。また、第２の金属としてＲｕ，Ａｇ，Ｃｏ，Ｚｎ，Ｃｄ，Ｈｇ，Ｇａ，Ｉｎ，Ｔｌ，Ｓｎ，Ｐｂ，Ｓｂ，Ｂｉ，Ｐｔ，Ａｕを用いた場合には、７００℃でアニールを行っても電極に変化はなく耐熱性が得られた。

【００４３】以上本発明の各実施形態を説明したが、本発明はこれらの実施形態に限定されるものではなく、その趣旨を逸脱しない範囲内において種々変形して実施することが可能である。

【００４４】

【発明の効果】本発明では、ＳｉＣとの間でショットキー接合を形成する電極材料に所定の金属を用いることにより、高温の熱処理を行ってもリーク電流の少ない優れた半導体素子を得ることができる。

【００４５】また、本発明では、ＳｉＣとの間でショットキー接合を形成する電極材料に所定の金属の合金を用いることにより、ショットキー接合のバリアハイトを低くすることができ、オン電流の多い優れた半導体素子を得ることができる。

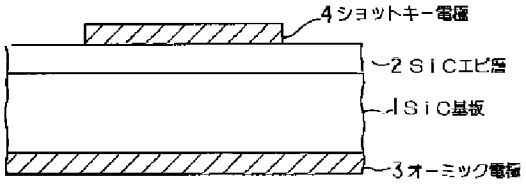
【図面の簡単な説明】

【図１】本発明の実施形態に係るショットキーダイオードの構成例を示した図。

【符号の説明】

1…ＳｉＣ基板
2…ＳｉＣエピタキシャル層
3…オーミック電極
4…ショットキー電極

【図１】



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JP2000101100A SEMICONDUCTOR DEVICE

Applicants: TOSHIBA CORP

Inventors: TAKIGAWA OSAMU

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SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To restrain an electrode from acting on an SiC board so as to lessen a leakage current by a method, where the electrode is formed of an element such as iron, ruthenium, osmium, iridium, or rhodium or alloy of two or more metals selected from among them. SOLUTION: An N-type SiC layer 2 is grown epitaxially on an N-conductivity type SiC board 1, the SiC board 1 is cleaned, and then Fe is evaporated as a Schottky electrode 4 on the epitaxial layer 2 on the SiC board 1. Ni is evaporated as an ohmic electrode 3 on the rear of the SiC board 1. An Fe electrode is formed through a patterning process. Ruthenium, osmium, iridium, or rhodium may also be used in place of iron. As a result, an electrode is made hardly reacting with SiC, and a leakage current can be restrained from increasing.

JP2000101100A SEMICONDUCTOR DEVICE

The EPO does not accept responsibility for the accuracy of data originating from authorities other than the EPO, nor does it guarantee that such data is complete, up-to-date or fit for specific purposes.

[0001] BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device using silicon carbide (SiC).

[0002] 2. Description of the Related Art A Schottky diode having a structure using a Schottky electrode in which a metal and a semiconductor are in contact has a feature that it can perform high-speed switching because it does not use minority carriers in the semiconductor. However, the Schottky diode using silicon has a problem that the breakdown voltage is low. On the other hand, a Schottky diode using SiC has a feature that the breakdown voltage is high. In addition, since a Schottky diode using SiC can operate at a high temperature, there is no need for a cooling means or only a small cooling device for applications where a large current flows.

[0003] For example, titanium (Ti) or the like is used as the Schottky electrode. However, when titanium is heat-treated at a high temperature, it reacts with SiC, and there is a problem that leakage current at the time of reverse bias increases. Further, as a device, it is necessary to form an ohmic electrode in addition to the Schottky electrode. Nickel is usually used as the ohmic electrode, but it is necessary to perform heat treatment at a temperature of several hundred degrees in order to produce good ohmic properties. The heat treatment at this time causes an increase in leakage current as described above in the Schottky electrode. A method is also conceivable in which heat treatment is performed after the ohmic electrode is formed, and then the Schottky electrode is formed. In this case, however, the surface is contaminated by impurities in the annealing atmosphere, and the phenomenon that the leakage current increases conversely occurs. .

[0004] On the other hand, when operating the Schottky diode, it is preferable to reduce the on-resistance to increase the on-current. In this case, the potential barrier between the semiconductor and the metal, that is, a so-called barrier height is required to be low. When Ti is used as the Schottky electrode, the barrier height is about 1 eV. However, it is desirable to further lower the barrier height in order to obtain a large current.

[0005] As described above, for example, when titanium is used as the Schottky electrode, there is a problem that the titanium reacts with SiC by heat treatment at a high temperature, and the leakage current at the time of reverse bias increases. It was.

[0006] Further, in order to increase the on-current of the Schottky diode, it is necessary to lower the barrier height between the semiconductor and the metal, but the barrier height when Ti is used as the Schottky electrode is about 1 eV, It was not always satisfactory.

[0007] The present invention has been made to solve the above-described conventional problems, and in a semiconductor device in which a Schottky junction is formed between SiC and an electrode, a reaction between SiC and the electrode is suppressed to reduce a leakage current. The first object is to lower the barrier height between the semiconductor and the electrode and increase the on-current.

[0008] According to the present invention, in a semiconductor device in which a Schottky junction is formed between SiC and an electrode, the electrode is selected from iron, ruthenium, osmium, iridium, rhodium or these. In addition, an alloy of at least two metals is used.

[0009] The metal has little reaction with SiC, and by using these metals as Schottky electrodes, an increase in leakage current during reverse bias can be suppressed even when heat treatment is performed at a high temperature.

[0010] Further, according to the present invention, in the semiconductor device in which a Schottky junction is formed between SiC and an electrode, the first metal of group IIIa (lanthanum-based or actinium-based such as Sc, Y, or La) is used as the electrode. And an alloy with a second metal having a work function of 3.9 eV or more.

[0011] It is preferable to use Sc as the first metal and a Group IVa (Ti, Zr, Hf) metal as the second metal. Thus, by using an alloy of a group IIIa metal (Sc or the like having a work function of 3.5 eV or less) and a metal having a work function of 3.9 eV or more as a Schottky electrode, SiC (for example, having a crystal structure

of In the case of 4H, the barrier height of the Schottky junction having an electron affinity of about 3.7 eV can be lowered, and the on-current can be increased.

[0012] Further, the present invention is characterized in that in a semiconductor device in which a Schottky junction is formed between SiC and an electrode, an alloy of IVa group (Ti, Zr, Hf) is used as the electrode.

[0013] Thus, even when an IVa group alloy is used as the Schottky electrode, the barrier height of the Schottky junction with SiC can be lowered, and the on-current can be increased.

[0014] DESCRIPTION OF THE PREFERRED EMBODIMENTS Embodiments of the present invention will be described below with reference to the drawings. (Embodiment 1) A Schottky diode as shown in FIG. 1 was manufactured as follows, and the manufactured Schottky diode was evaluated.

[0015] First, a substrate obtained by epitaxially growing an n-type SiC layer (SiC epitaxial layer 2) of 10 μm with an impurity concentration of 5 × 10 15 / cm 3 on an SiC substrate 1 (thickness 0.2 mm) having an n-type conductivity of 10 18 / cm 3 of impurity concentration. Got ready. This substrate is immersed in a mixed solution of ammonia water and hydrogen peroxide solution, and further cleaned by immersing it in a dilute hydrofluoric acid aqueous solution, and then Fe is used as a Schottky electrode 4 on the epitaxial layer 2 side to a thickness of 1 μm. Vapor deposited. Moreover, Ni was vapor-deposited on the back surface of the SiC substrate 1 as an ohmic electrode 3 with a thickness of 1 μm. Thereafter, a patterning process such as resist coating, exposure, development, and etching was performed to form an Fe electrode (Schottky electrode 4) having a diameter of 0.1 mm. As a comparative example, a sample in which Ti was formed as a Schottky electrode was also produced.

[0016] Both samples prepared as described above were heat-treated at 700 ° C. in an argon atmosphere, and the reverse leakage current of the diode was measured. As a result, the leakage current at a voltage of −100 V was about 10 −4 (A) when Ti was used as the Schottky electrode, but was as small as 10 −6 (A) or less in the case of Fe. The ohmic electrode exhibited almost ohmic characteristics by the heat treatment.

[0017] In order to examine the interface of the Schottky electrode, an SiC substrate on which Ti and Fe were deposited to a thickness of 10 nm was heat-treated at 700 ° C., and X-ray diffraction was performed. In the case of Ti, a silicide peak was observed, but in the case of Fe, almost no silicide was observed.

[0018] Thus, it is considered that the reason for the small leakage current is that the reaction between Fe and SiC is small. That is, Fe has a heat of formation of silicide equal to or greater than that of SiC, and is more stable when present as a metal than reacts with silicon in SiC to form silicide. Therefore, it is considered that it is difficult to react with SiC by heat treatment, so that an increase in leakage current can be suppressed.

[0019] The leakage current was also small for the sample in which Fe was formed to a thickness of 10 nm, annealed, and 1 μm of Al was deposited on Fe, as described above. In addition, the leakage current was small for the sample using ruthenium, osmium, iridium and rhodium instead of iron as well.

[0020] (Embodiment 2) A Schottky diode as shown in FIG. 1 was fabricated in the same manner as in the first embodiment by changing the type of Schottky electrode, and the fabricated Schottky diode was evaluated.

[0021] In this embodiment, Ti silicide, specifically, Ti3Si, TiSi, and TiSi2 are formed as the Schottky electrode. As a forming method, Ti and Si were used as evaporation sources, respectively, and both were evaporated at the same time by an E gun deposition apparatus. The substrate temperature at this time was 250 ° C.

[0022] The manufactured sample was heat-treated in the same manner as in the first embodiment, and then the leakage current was measured. As a result, in the case of Ti3 Si, the leakage current was in the order of 10 @ -5 (A), but in TiSi, it was 4 * 10 <-6> (A), and in TiSi2 it was 2 * 10 <-6> (A). It was. Further, X-ray diffraction of the interface was performed in the same manner as in the first embodiment. As a result, peaks that could not be identified were observed with Ti3 Si, but peaks other than the respective silicide were not observed with the others. In the case of Ti3 Si, the leakage current is slightly high, and it is considered that there is a slight reaction with SiC, but other samples have good characteristics. Note that the crystallinity of silicide is improved by annealing, which is considered to contribute to the improvement of characteristics.

[0023] Further, when Ti silicide was formed with a thickness of 100 nm and Ti was formed thereon with a thickness of 1 μm, the leakage current could be reduced as described above. In this case, compared with the case

where Ti silicide is thick, the fall of the adhesive force by heat processing was suppressed. The effect was also seen when the thickness of the Ti silicide was 20 nm.

[0024] Further, when heat treatment was similarly performed using a metal silicide other than Ti for the Schottky electrode, the increase in the leakage current was small, and the leakage current was 10 −5 (A) or less.

[0025] When the metal silicide is MSix (M is a metal), the generation energy of the silicide is lowest when the value of x is near 1. Therefore, it can be said that a silicide containing Si at a predetermined ratio is more thermally stable in the state as it is, rather than depriving SiC of Si to become a compound having a larger x. Therefore, it is considered that by using silicide, it becomes difficult to react with SiC by heat treatment, and an increase in leakage current can be suppressed.

[0026] As the metal M that forms silicide, a metal having a work function of 5.2 or less has a small barrier height against SiC, and can reduce the on-resistance. In addition to Ti, the metal M includes La, Zr, Hf, V, Nb, Ta, Cr, Mo, W, Mn, Re, Ni, Ru, Pd, Lu, Fe, Os, Ir, Co, Rh, and Pt. can give. Further, from the viewpoint of suppressing the reaction with Si in SiC, the ratio of Si in the metal silicide MSix is preferably a predetermined value or more, specifically, x is 0.3 or more, more preferably 1 or more.

[0027] Although the first and second embodiments have been described above, the thickness as the Schottky electrode is preferably about 10 nm or more, and as described in the examples in order to reduce the planar resistance or improve the bondability. Other metals may be laminated on the substrate.

[0028] Although the Schottky diode has been described in the first and second embodiments, it can be used as a Schottky electrode of another semiconductor device such as MESFET.

[0029] (Embodiment 3) A Schottky diode as shown in FIG. 1 was manufactured as follows, and the manufactured Schottky diode was evaluated.

[0030] First, a substrate obtained by epitaxially growing an n-type SiC layer (SiC epitaxial layer 2) of 10 μm with an impurity concentration of 5 × 10 15 / cm 3 on an SiC substrate 1 (thickness 0.2 mm) having an n-type conductivity of 10 18 / cm 3 of impurity concentration. Got ready. After cleaning by a normal cleaning method, an oxide film was formed at 1200 ° C. in dry oxygen. Thereafter, the epitaxial layer 2 side was protected with a resist, and the oxide film on the opposite side was dissolved with hydrofluoric acid. After removing the resist, cleaning was performed, and Ni was deposited as an ohmic electrode 3 on the back surface of the SiC substrate 1 to a thickness of 1 μm. Furthermore, annealing was performed at 950 ° C. to ensure ohmic properties. Thereafter, the oxide film on the epitaxial layer 2 side was dissolved to expose the surface of the epitaxial layer 2.

[0031] Next, the substrate subjected to the above steps was set in a vapor deposition apparatus, and a metal material to be a Schottky electrode was vapor deposited. At this time, Sc was selected as the first metal and Hf or Zr was selected as the second metal, and the first metal and the second metal were vapor-deposited simultaneously. The substrate temperature was 200 ° C. to facilitate the formation of a solid solution of both metals. Samples were prepared with Sc: Hf or Sc: Zr ratios of 3: 2, 1: 1, 9: 1. Thereafter, patterning was performed to form a Schottky electrode 4 having a diameter of 100 μm. After patterning, annealing was performed in an argon atmosphere at 300 ° C. for 1 hour.

[0032] Sc used as the first metal is easy to form silicide and carbide and can provide sufficient adhesion to SiC. However, since it has a low work function, it cannot form a Schottky barrier when bonded to SiC. Therefore, by using Hf or Zr, which has a work function larger than Sc and easily forms a solid solution with Sc, and increases the work function of the solid solution, a Schottky diode having a low barrier height with respect to SiC is formed.

[0033] For the sample produced as described above, the built-in voltage was determined from the relationship between voltage and capacity, and the barrier height was determined. As a comparative example, a Ti-Schottky electrode was prepared in the same manner, and the barrier height was obtained. As a result, in the case of Ti, the barrier height was 0.9 eV, but in the case of this embodiment, each sample was in the range of 0.2 to 0.8 eV. Although variation was observed, the barrier height value tended to be larger when the Sc ratio was smaller.

[0034] Moreover, when the X-ray diffraction of the electrode was performed, the sample of this embodiment was a single phase. Also, no phenomenon such as peeling due to phase separation in annealing, which is often found in mixed phase electrodes, was observed.

[0035] When an electrode is formed by a normal cleaning and vapor deposition process, a thin oxide film is easily formed at the interface, and a large barrier height may be observed due to the influence. Then, in order to clean the interface, ion bombardment or the like was performed before vapor deposition, and a stable interface could be obtained. This will be specifically described below.

[0036] A small amount of an inert gas such as He or Ar or a reducing gas such as hydrogen or hydrocarbon is introduced into a deposition apparatus equipped with an RF coil to generate plasma, and a DC voltage of about 100 V or less is applied to the plasma. And collided with the SiC substrate surface. The barrier height of the Schottky electrode formed after such ion bombardment treatment was evaluated. After annealing at 300 ° C, those without ion bombardment treatment had a variation of about ± 0.2 eV in barrier height, but those with ion bombardment treatment were improved within ± 0.1 eV. It was done.

[0037] In addition, when a heat treatment at 600 ° C. was performed in a reduced pressure state in which hydrogen gas was introduced, and then a metal material serving as a Schottky electrode was deposited at 200 ° C., the variation in barrier height was still within ± 0.1 eV.

[0038] (Embodiment 4) A Schottky diode was fabricated in the same manner as in the third embodiment, using Hf as the first metal, Ti as the second metal, and using a solid solution of both metals as the Schottky electrode. The ratio of Hf / Ti was 9 to 0.1. As a result, the barrier height could be continuously changed from 0.3 to 0.7 eV. Further, as in the first embodiment, no electrode peeling occurred.

[0039] It is also effective to form a solid solution with Zr, Hf, and Ti. In addition to the above-mentioned Hf-Ti, the work function is lowered than Ti by using a solid solution of Hf-Zr or Zr-Ti. Therefore, it is possible to obtain a Schottky junction with a low barrier height.

[0040] (Embodiment 5) Two types of Schottky using La as the first metal and Al as the second metal, which are simultaneously deposited at a substrate temperature of 200 ° C., and using La 3 Al and LaAl 2 as Schottky electrodes A diode was fabricated in the same manner as in the third embodiment. As a comparative example, a sample using La as a Schottky electrode was also produced.

[0041] As a result of the measurement, the barrier height of the Schottky junction with SiC was 0.4 eV for La3 Al and 0.6 eV for LaAl2. Also, annealing was performed on a sample using LaAl2 as an electrode. When a voltage of 100 V was applied in the reverse direction, the leakage current was 10 −4 (A) in the 300 ° C. annealing, but decreased to 10 −6 (A) in the 800 ° C. annealing. In the sample using only La for the electrode, the electrode was aggregated by annealing at 800 ° C., but in the sample using LaAl 2 as the electrode, no particular change was observed in the shape. (Embodiment 6) Sc, Y or lanthanum-based La, Ce, Gd, Nd is used as the first metal, and Ru, Ag, Co, Zn, Cd, Hg, Ga, In, Tl, as the second metal. Sn, Pb, Sb, Bi, Pt, and Au were used, and an alloy having a first metal / second metal ratio of 0.3 to 3 was used as a Schottky electrode. The manufacturing method is the same as that of the third embodiment, and the barrier height was similarly evaluated.

[0042] As a result, the barrier height was in the range of 0.3 to 0.8 eV. In addition, even if about 2% of the impurity element was contained in the second metal, the barrier height was not greatly affected. Further, when Ru, Ag, Co, Zn, Cd, Hg, Ga, In, Tl, Sn, Pb, Sb, Bi, Pt, or Au is used as the second metal, annealing is performed at 700 ° C. There was no change in the electrode, and heat resistance was obtained.

[0043] Although the embodiments of the present invention have been described above, the present invention is not limited to these embodiments, and various modifications can be made without departing from the spirit of the present invention.

[0044] According to the present invention, by using a predetermined metal as an electrode material for forming a Schottky junction with SiC, it is possible to obtain an excellent semiconductor element having a small leakage current even when a high temperature heat treatment is performed. it can.

[0045] Further, in the present invention, by using a predetermined metal alloy as an electrode material for forming a Schottky junction with SiC, the barrier height of the Schottky junction can be lowered, and an excellent semiconductor device having a large on-current Can be obtained.

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CLAIMS JP2000101100

1.
In a semiconductor device having a Schottky junction formed between SiC and an electrode, iron, ruthenium, osmium, iridium, rhodium, or an alloy of at least two metals selected from these is used as the electrode. Semiconductor device.

2.
In a semiconductor device in which a Schottky junction is formed between SiC and an electrode, an alloy of a first metal of Group IIIa and a second metal having a work function of 3.9 eV or more is used as the electrode. Semiconductor device.

3.
The semiconductor device according to claim 2, wherein scandium (Sc) is used as the first metal, and a group IVa metal is used as the second metal.

4.
A semiconductor device in which a Schottky junction is formed between SiC and an electrode, wherein an alloy of IVa group is used as the electrode.

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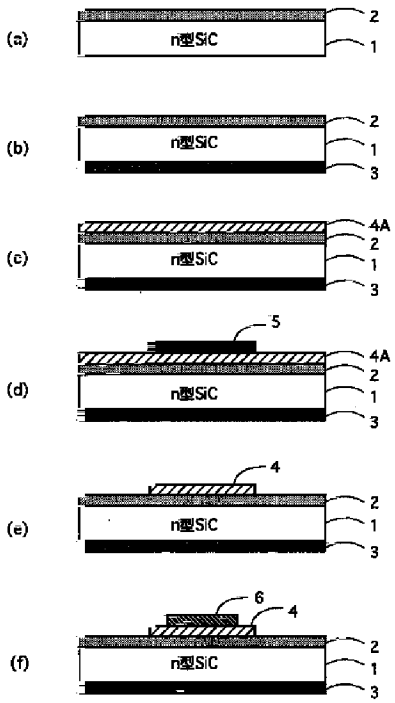
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(71)出願人　000191238
新日本無線株式会社
東京都中央区日本橋横山町３番10号
(72)発明者　新井　学
埼玉県上福岡市福岡２丁目１番１号　新日本無線株式会社川越製作所内
(72)発明者　木村　親夫
埼玉県上福岡市福岡２丁目１番１号　新日本無線株式会社川越製作所内
(74)代理人　100083194
弁理士　長尾　常明

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(54)【発明の名称】　ショットキーダイオードおよびその製造方法

(57)【要約】
【課題】　同じ電流を流すのに要する順方向電圧を低下させたショットキーダイオードを提供すること。
【解決手段】　シリコンカーバイド基板１の上に形成したエピタキシャル層２の上面に、ショットキー電極として酸化ルテニウム４を形成した。シリコンカーバイド基板１の裏面にはNi層のオーミック電極を形成した。



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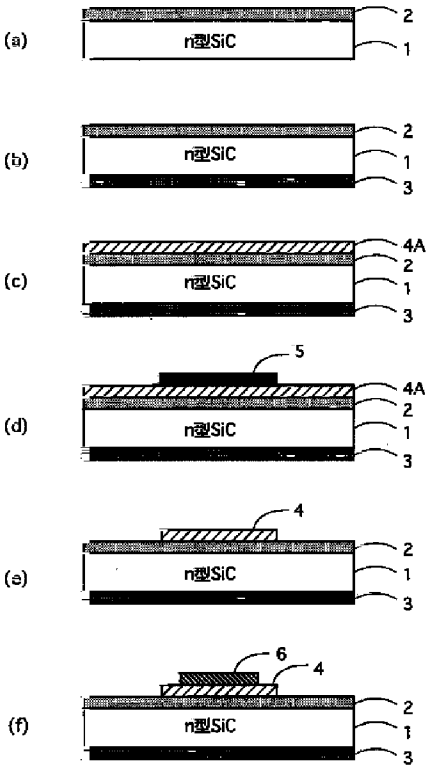
【特許請求の範囲】
【請求項１】シリコンカーバイド基板の活性層の面上にショットキー電極として酸化ルテニウム膜を形成してなることを特徴とするショットキーダイオード。
【請求項２】前記酸化ルテニウム膜の上面に金又はアルミニウムからなるパッド電極を形成してなることを特徴とする請求項１に記載のショットキーダイオード。
【請求項３】前記シリコンカーバイド基板の前記酸化ルテニウム膜が形成された面と反対側の面にオーミック電極を形成してなることを特徴とする請求項１又は２に記載のショットキーダイオード。
【請求項４】シリコンカーバイド基板の活性層の面上に、反応スパッタ法、蒸着法又はゾル・ゲル法により酸化ルテニウム膜を形成する工程と、
前記酸化ルテニウム膜をエッチングして所定の形状の電極に形成する工程と、
を含むことを特徴とするショットキーダイオードの製造方法。
【請求項５】前記酸化ルテニウム膜を形成する工程よりも後に、前記酸化ルテニウム膜の上に金又はアルミニウムのパッド電極を形成する工程を設けたことを特徴とする請求項４に記載のショットキーダイオードの製造方法。
【請求項６】前記酸化ルテニウム膜を形成する工程よりも前に、前記シリコンカーバイド基板の裏面にオーミック電極を形成する工程を設けたことを特徴とする請求項４又は５に記載のショットキーダイオードの製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、SiC（シリコンカーバイド）を基板として使用したショットキーダイオードおよびその製造方法に関するものである。
【０００２】
【従来の技術】半導体装置の電極材料の選択には、その半導体の種類やその電極に求められる特性（半導体との密着性、耐熱性、ワイヤボンディング容易性等のデバイスやプロセス上の要求）を十分に考慮する必要がある。この金属材料は大別すると、(1)半導体構成元素の全てと安定な化合物を形成するもの、(2)半導体構成元素の一部とのみ化合物を形成するもの、(3)高融点金属、に分類される。
【０００３】まず、(1)の金属材料は、GaAs（ガリウム砒素）等の化合物半導体と一様に固溶反応する。よく知られている半導体装置として、電極材料にPt（プラチナ）を使用したPt/GaAsがある。この半導体装置では、200℃以上の熱処理により多結晶のPtAs、PtGaが形成される。この場合の接合界面は、シャープ（界面が明確）で耐熱性もよく、更に固相反応とともにGaAs表面の酸化物や汚れが除去されるので、表面処理に特別の注意を払わなくても、n因子（ショットキーダイオードの特性を表すもので、n値ともいう。）の良好なショットキー電極が得られる。ただ、この金属材料とV族元素との化合物は一般に比抵抗が大きいため、比抵抗の小さな金属で上面を覆い回路全体の抵抗を低下させる必要がある。
【０００４】(2)の金属材料は、一般に半導体とは反応し難い。例えば、III－Vの化合物半導体に対しては、蒸気圧の高いV族としか化合物を形成しない金属が特に反応し難く、耐熱性や信頼性に優れている。一例として、GaAsのゲート電極として多く用いられるAlがある。一方、III族とのみ反応する系では、V族元素の蒸気圧が大きいため電極表面から飛散し易く、金属とIII族の化合物生成エネルギーが小さくても、半導体との反応が進行する。Au/GaAsの反応がそれである。
【０００５】(3)の金属材料は、W（タングステン）、Mo（モリブデン）等では化合物半導体との反応速度が小さいため、耐熱性が良好である。
【０００６】ところで、化合物半導体材料として、SiC基板が市販されるようになり、そのデバイスの研究が盛に行われている。このSiCは、Si（シリコン）に比べて３倍もの熱伝導率を持ち、約２倍もの飽和電子ドリフト速度を持ち、さらに六方晶の６H－SiCでは禁制帯幅が3.09 eVもの大きな値に達する。
【０００７】このため、絶縁破壊電圧はSiに比べて１０倍程度も高く、動作可能な温度は500℃にも達し、しかもその導電型をｐ型にもｎ型にも制御できることから、高温動作デバイス、大電力デバイス、耐放射線デバイス等のように厳しい環境下で動作させる素材として期待されてきた。
【０００８】このようなSiCの結晶上に安定なオーミック電極が形成できるかについて、SiCは前記したように広い禁制帯幅と高い化学的安定性を有するところから、合金化には比較的高温が必要になるが、n型SiCへのオーミック接合では、種々の金属が試されている。
【０００９】例えば、ドーピング濃度が$5\times10^{18}cm^{-3}$のSiC基板にNi（ニッケル）電極を被着させた例では、$10^{-5}\Omega\cdot cm^2$台のコンタクト抵抗率が得られており、更に高いドーピング濃度のSiC基板に対しては$10^{-6}\Omega\cdot cm^2$台と、素子の用途によってはすでに実用化できる程度の低い抵抗率が得られている（C.Aranodo,etc.,Ins.Phys.Conf.Ser.142,P.577,1996）。
【００１０】
【発明が解決しようとする課題】ところが、SiCの結晶上に良好なショットキー電極が形成できるかについては、NiやTi（チタン）が試みられているものの、いずれもショットキー障壁が1.3eV、0.85 eVと大きく、同じ電流を流すのに要する順方向電圧が高くなるという問題がある。
【００１１】本発明の目的は、順方向電圧が低いショットキー半導体装置及びその製造方法を提供することである。

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【0012】
【課題を解決するための手段】上記課題を解決するための第1の発明のショットキーダイオードは、シリコンカーバイド基板の活性層の面上にショットキー電極として酸化ルテニウム膜を形成して構成した。
【0013】第2の発明は、第1の発明において、前記酸化ルテニウム膜の上面に金又はアルミニウムからなるパッド電極を形成して構成した。
【0014】第3の発明は、第1又は第2の発明において、前記シリコンカーバイド基板の前記酸化ルテニウム膜が形成された面と反対側の面にオーミック電極を形成して構成した。
【0015】第4の発明のショットキーダイオードの製造方法は、シリコンカーバイド基板の活性層の面上に、反応スパッタ法、蒸着法又はゾル・ゲル法により酸化ルテニウム膜を形成する工程と、前記酸化ルテニウム膜をエッチングして所定の形状の電極に形成する工程とを含むよう構成した。
【0016】第5の発明は、第4の発明において、前記酸化ルテニウム膜を形成する工程よりも後に、前記酸化ルテニウム膜の上に金又はアルミニウムのパッド電極を形成する工程を設けた。
【0017】第6の発明は、第4又は第5の発明において、前記酸化ルテニウム膜を形成する工程よりも前に、前記シリコンカーバイド基板の裏面にオーミック電極を形成する工程を設けた。
【0018】
【発明の実施の形態】図1は本発明の実施の形態のショットキー半導体装置の製造工程を示す図である。本実施形態では、まず図1の(a)にあるように、高濃度（例えば、$5\times10^{18}cm^{-3}$）に不純物がドープされたn型のSiC基板1の上面に、N（窒素）を不純物として$3.5\times10^{18}cm^{-3}$だけ添付したエピタキシャル層2を膜厚13μmだけ予め成長させた基板を用意する。
【0019】次に、図1の(b)にあるように、基板1の裏面にNi層3を真空蒸着法により所定膜厚だけ堆積させ、950℃の温度で2分間の熱処理を行う。これにより、Ni層3は、SiC基板1との界面が合金化されて、$10^{-5}\Omega\cdot cm^2$台のコンタクト抵抗率のオーミック電極として機能するようになる。
【0020】次に、図1の(c)にあるように、酸化ルテニウム（RuO_2）膜4Aを反応性スパッタ法により形成する。この反応性スパッタ法は、ルテニウムをターゲットとして、スパッタ用のAr（アルゴン）と酸化用のO_2（酸素）供給して行う。このときの条件は、その圧力を例えば12 m Torrとし、ガス流量はAr/O_2が15/45 sccmになるような条件で成長を行い、これにより約200 nmの酸化ルテニウム膜4Aを形成する。
【0021】次に、図1の(d)にあるように、酸化ルテニウム膜4Aに対して塗布したレジスト5のパターニングを周知の写真蝕刻法により行い、このレジスト5をマスクとして、RIE（リアクティブ・イオン・エッチング）により酸化ルテニウム膜4Aのエッチングを行って、図1の(e)にあるように、酸化ルテニウム電極4としての形状に形成する。酸化ルテニウムはCF_4ガスでエッチング可能であり、圧力が0.04 Torr、CF_4の流量が40 sccm、高周波電力が250 Wのとき、エッチングレートが12 nm/minで加工される。
【0022】最後に、配線を接続するため等のパッドとなるAu（金）又はAl（アルミニウム）の電極6を真空蒸着法により形成する。この低抵抗のパッド電極6により回路全体の抵抗も低下する。
【0023】以上のようにして形成したショットキーダイオードは、ショットキー障壁の高さが0.5 eVであり、順方向のオン抵抗が4 mΩ・cm^2を実現できた。
【0024】ここに形成した酸化ルテニウムは、その電気抵抗率が室温で$4\times10^{-5}\Omega\cdot cm$と白金の$1\times10^{-5}\Omega\cdot cm$とほぼ同じであり、またこの酸化ルテニウムは800℃まで分解せず安定である。
【0025】なお、ここではルテニウムをターゲットとし酸素を供給して反応性スパッタ法により酸化ルテニウム膜を生成する場合について説明したが、酸化ルテニウムをターゲットにしてスパッタを行うこともできる。この場合でも酸素を供給する反応性スパッタが好ましい。また、酸化ルテニウム電極は、その酸化ルテニウムを蒸発させて堆積させる真空蒸着法により形成することもできるが、この場合も酸素を供給することが好ましい。さらに、酸化ルテニウム電極は、ゾル・ゲル法（酸化ルテニウムをゾルやゲル化してエピタキシャル膜2の上に塗布しその後に乾燥・焼結させて電極とする方法）により形成することもできる（S.Saito,etc.,Jpn.J.Appl.Phy.31,1991 p.135）。
【0026】
【発明の効果】以上から本発明によれば、ショットキーダイオードに同じ電流を流すのに要する順方向電圧をNiやTiをショットキー電極に使用した場合に比べて大幅に低減することができる利点がある。
【図面の簡単な説明】
【図1】　本発明のショットキーダイオードの製造方法の説明図である。
【符号の説明】
1：高濃度不純物添加のSiC基板
2：エピタキシャル層（活性層）
3：Ni層（オーミック電極）
4A：酸化ルテニウム膜
4：酸化ルテニウムショットキー電極
5：レジスト
6：パッド電極

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【図1】


(a)
n型SiC
2
1
(b)
n型SiC
2
1
3
(c)
n型SiC
4A
2
1
3
(d)
n型SiC
5
4A
2
1
3
(e)
n型SiC
4
2
1
3
(f)
n型SiC
6
4
2
1
3

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JP2000299479A SCHOTTKY DIODE AND MANUFACTURE THEREOF

Applicants: NEW JAPAN RADIO CO LTD

Inventors: ARAI MANABU,KIMURA CHIKAO

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SCHOTTKY DIODE AND MANUFACTURE THEREOF

Abstract

PROBLEM TO BE SOLVED: To obtain a Schottky semiconductor device having a lower forward voltage by forming a ruthenium oxide film as a Schottky electrode on the surface of active layer on a silicon carbide substrate. SOLUTION: An epitaxial layer 2 that is an active layer to which N is added as impurity is grown on the surface of an n-type SiC substrate 1 where impurity is doped to a high concentration. Next, an Ni layer 3 is deposited only in the predetermined thickness with a vacuum evaporation method at the rear surface of the substrate 1. Consequently, the Ni layer 3 functions as an ohmic electrode because the interface with SiC substrate 1 is alloyed. Next, an ruthenium oxide film 4A is formed with the reactive sputtering method. A resist 5 coated to the ruthenium oxide 4A is patterned and etching is then executed using such resist 5 to form a ruthenium oxide electrode 4. As a result, the forward voltage can be lowered than that when Ni and Ti are used as the Schottky electrode.

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DESCRIPTION JP2000299479

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a Schottky diode using SiC (silicon carbide) as a substrate and a method for manufacturing the same.

[0002]

2. Description of the Related Art In selecting an electrode material for a semiconductor device, the type of the semiconductor and the characteristics required for the electrode (adhesion with the semiconductor, heat resistance, easiness of wire bonding, etc. in the device and process) are selected. It needs to be considered carefully. This metal material is roughly classified into (1) those that form stable compounds with all of the semiconductor constituent elements, (2) those that form compounds only with some of the semiconductor constituent elements, and (3) refractory metals. being classified.

[0003]

First, the metal material (1) uniformly undergoes solid solution reaction with a compound semiconductor such as GaAs (gallium arsenide). A well-known semiconductor device is Pt / GaAs that uses Pt (platinum) as an electrode material. In this semiconductor device, polycrystalline PtAs and PtGa are formed by heat treatment at 200 ° C. or higher. In this case, the bonding

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interface is sharp (the interface is clear) and has good heat resistance, and since the oxides and dirt on the GaAs surface are removed along with the solid-phase reaction, n Factor (represents the characteristics of the Schottky diode and is also called the n value.) Good Schottky electrode can be obtained. However, since the compound of the metal material and the group V element generally has a large specific resistance, it is necessary to cover the upper surface with a metal having a small specific resistance to reduce the resistance of the entire circuit.

[0004]
(2)

In general, the metal materials described above are difficult to react with semiconductors. For example, with respect to III-V compound semiconductors, a metal that forms a compound only with a group V having a high vapor pressure is particularly difficult to react, and is excellent in heat resistance and reliability. One example is Al, which is often used as the gate electrode of GaAs. On the other hand, in a system that reacts only with the group III element, the vapor pressure of the group V element is large, so that the element easily scatters from the electrode surface, and the reaction with the semiconductor proceeds even if the metal and group III compound formation energy is small. That is the reaction of Au / GaAs.

[0005]
(3)The metallic material of W (tungsten), Mo (molybdenum) or the like has a low reaction rate with the compound semiconductor, and thus has good heat resistance.

[0006]

Meanwhile, as a compound semiconductor material, a SiC substrate has come to be marketed, and research on the device has been actively conducted.

This SiC has a thermal conductivity three times that of Si (silicon) and a saturation electron drift velocity about twice that of Si (Si), and the band gap of hexagonal 6H-SiC reaches as large as 3.09 eV. ..

[0007]
For this reason, the breakdown voltage is about 10 times higher than that of Si, the operable

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temperature reaches 500 ° C, and its conductivity type can be controlled to p-type or n-type. It has been expected as a material that can be operated in severe environments such as high power devices and radiation resistant devices.

[0008]
Regarding the formation of stable ohmic electrodes on such SiC crystals, since SiC has a wide band gap and high chemical stability as described above, relatively high temperature is required for alloying. However, various metals have been tried in ohmic contact with n-type SiC.

[0009]

For example, in a case where a Ni (nickel) electrode is deposited on a SiC substrate with a doping concentration of 5 × 10 18 cm −3, a contact resistivity of 10 −5 Ω · cm 2 is obtained, and a SiC substrate with a higher doping concentration is obtained. However, the resistivity is as low as 10-6 Ω · cm2, which is low enough for practical use depending on the application of the device (C. Aranodo, etc., Ins.

Phys.

Conf. Ser. 142, P. 577, 1996).

[0010]
However, as to whether a good Schottky electrode can be formed on a SiC crystal, although Ni and Ti (titanium) have been tried, both have a Schottky barrier of 1.3 eV, The problem is that it is as large as 0.85 eV and the forward voltage required to pass the same current becomes high.

[0011]
An object of the present invention is to provide a Schottky semiconductor device having a low forward voltage and a manufacturing method thereof.

[0012]
The Schottky diode of the first invention for solving the above problems is constituted by forming a ruthenium oxide film as a Schottky electrode on the surface of an active layer of a silicon

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carbide substrate.

[0013]
According to a second aspect of the present invention, in the first aspect, a pad electrode made of gold or aluminum is formed on the upper surface of the ruthenium oxide film.

[0014]
A third invention is the first or second invention, wherein an ohmic electrode is formed on the surface of the silicon carbide substrate opposite to the surface on which the ruthenium oxide film is formed.

[0015]
A method of manufacturing a Schottky diode according to a fourth aspect of the present invention comprises a step of forming a ruthenium oxide film on a surface of an active layer of a silicon carbide substrate by a reactive sputtering method, a vapor deposition method or a sol-gel method, and the ruthenium oxide film. And a step of forming an electrode having a predetermined shape by etching.

[0016]
In a fifth aspect of the present invention, the step of forming a pad electrode of gold or aluminum on the ruthenium oxide film is provided after the step of forming the ruthenium oxide film in the fourth aspect.

[0017]
In a sixth aspect of the invention, in the fourth or fifth aspect of the invention, a step of forming an ohmic electrode on the back surface of the silicon carbide substrate is provided before the step of forming the ruthenium oxide film.

[0018]

1 is a diagram showing a manufacturing process of a Schottky semiconductor device according to an embodiment of the present invention.

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In this embodiment, first, as shown in FIG. 1A, N (nitrogen) is added as an impurity to the upper surface of the n-type SiC substrate 1 which is highly doped (for example, 5 × 10 18 cm −3) with impurities. As the substrate, a substrate is prepared in which the epitaxial layer 2 attached to 3.5 × 10 18 cm −3 is grown to a thickness of 13 μm in advance.

[0019]

Next, as shown in FIG. 1B, a Ni layer 3 is deposited on the back surface of the substrate 1 by a vacuum deposition method to a predetermined thickness, and heat treatment is performed at a temperature of 950 ° C. for 2 minutes.

As a result, the Ni layer 3 is alloyed at the interface with the SiC substrate 1 and functions as an ohmic electrode having a contact resistivity of 10 −5 Ω · cm 2.

[0020]

Next, as shown in FIG. 1C, a ruthenium oxide (RuO2) film 4A is formed by a reactive sputtering method.

This reactive sputtering method is performed by supplying ruthenium as a target and supplying Ar (argon) for sputtering and O2 (oxygen) for oxidation.

The conditions at this time are such that the pressure is, for example, 12 m Torr, and the gas flow rate is such that Ar / O2 is 15/45 sccm, whereby the ruthenium oxide film 4A of about 200 nm is formed.

[0021]

Next, as shown in FIG. 1D, patterning of the resist 5 applied to the ruthenium oxide film 4A is performed by a well-known photo-etching method, and the RIE (reactive ion. Etching) is performed to etch the ruthenium oxide film 4A to form a ruthenium oxide electrode 4 as shown in FIG.

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Ruthenium oxide can be etched with CF4 gas, and when the pressure is 0.04 Torr, the flow rate of CF4 is 40 sccm, and the high frequency power is 250 W, the etching rate is 12 nm / min.

[0022]

Finally, an electrode 6 of Au (gold) or Al (aluminum), which serves as a pad for connecting wiring, is formed by a vacuum evaporation method.

This low resistance pad electrode 6 also reduces the resistance of the entire circuit.

[0023]
The Schottky diode formed as described above has a Schottky barrier height of 0.5 eV and an on-resistance in the forward direction of 4 mΩ · cm 2.

[0024]
The ruthenium oxide formed here has an electrical resistivity of 4×10^{-5} Ω · cm at room temperature and about 1×10^{-5} Ω · cm of platinum, and this ruthenium oxide does not decompose up to 800 ° C. It is stable.

[0025]

Although the case where ruthenium is used as a target and oxygen is supplied to form a ruthenium oxide film by a reactive sputtering method has been described here, it is also possible to perform sputtering using ruthenium oxide as a target.

Even in this case, reactive sputtering for supplying oxygen is preferable.

Further, the ruthenium oxide electrode can be formed by a vacuum vapor deposition method in which the ruthenium oxide is evaporated and deposited, but in this case also, it is preferable to supply oxygen.

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Further, the ruthenium oxide electrode can also be formed by a sol-gel method (a method in which ruthenium oxide is sol or gelled and applied on the epitaxial film 2 and then dried and sintered to form an electrode). Saito, etc., Jpn.

J.Appl. Phy. 31, 1991 p.135).

[0026]

As described above, according to the present invention, the forward voltage required to pass the same current through the Schottky diode can be significantly reduced as compared with the case where Ni or Ti is used for the Schottky electrode. There is.

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CLAIMS JP2000299479

1.
A Schottky diode characterized in that a ruthenium oxide film is formed as a Schottky electrode on the surface of an active layer of a silicon carbide substrate.

2.
The Schottky diode according to claim 1, wherein a pad electrode made of gold or aluminum is formed on an upper surface of the ruthenium oxide film.

3.
3. The Schottky diode according to claim 1, wherein an ohmic electrode is formed on the surface of the silicon carbide substrate opposite to the surface on which the ruthenium oxide film is formed.

4.
A step of forming a ruthenium oxide film by a reactive sputtering method, a vapor deposition method or a sol-gel method on the surface of the active layer of the silicon carbide substrate; and a step of etching the ruthenium oxide film to form an electrode having a predetermined shape. A method of manufacturing a Schottky diode, comprising:

5.
The method of manufacturing a Schottky diode according to claim 4, further comprising a step of

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forming a pad electrode of gold or aluminum on the ruthenium oxide film after the step of forming the ruthenium oxide film.

6.

6. The method of manufacturing a Schottky diode according to claim 4, further comprising a step of forming an ohmic electrode on the back surface of the silicon carbide substrate before the step of forming the ruthenium oxide film.

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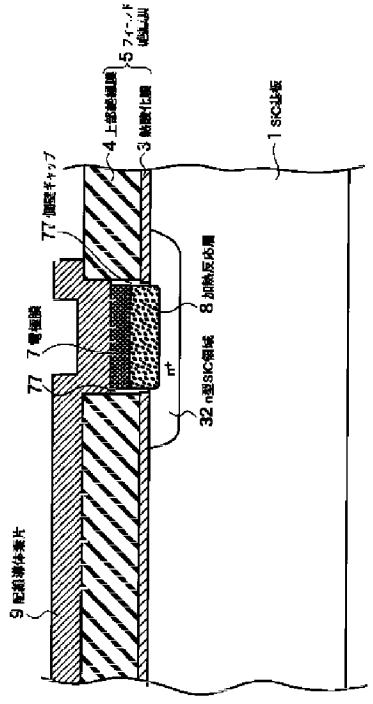
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(71)出願人　301021533
独立行政法人産業技術総合研究所
東京都千代田区霞が関１－３－１
(74)上記１名の復代理人　100083806
弁理士　三好　秀和　（外８名）
(71)出願人　000003997
日産自動車株式会社
神奈川県横浜市神奈川区宝町２番地
(74)上記１名の代理人　100083806
弁理士　三好　秀和　（外８名）
(72)発明者　大串　秀世
茨城県つくば市梅園１丁目１番４　工業技術院電子技術総合研究所内

最終頁に続く

(54)【発明の名称】　オーミック電極構造体、その製造方法、半導体装置及び半導体装置の製造方法

(57)【要約】
【課題】　$10^{-7}\Omega cm^2$台程度の低いコンタクト抵抗を有する微細且つ信頼性の高いオーミック電極構造体を提供する。
【解決手段】　ＳｉＣ基板１、ＳｉＣ基板１の表面に形成されたｎ型ＳｉＣ領域３２、ＳｉＣ基板１の上に載置されたフィールド絶縁膜５、フィールド絶縁膜５中にｎ型ＳｉＣ領域３２を露出するように開口された開口部の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７を隔てて配置された電極膜７、電極膜７とｎ型ＳｉＣ領域３２の間に配置された加熱反応層８、フィールド絶縁膜５の開口部の内部において、電極膜７の表面に接し、且つフィールド絶縁膜５の上部にまで伸延された配線導体素片９とから構成されている。側壁ギャップ７７を構成している一定の間隙は、フィールド絶縁膜５の厚みより小さい値に制御されている。



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【特許請求の範囲】
【請求項１】　炭化珪素（ＳｉＣ）基板と、
前記ＳｉＣ基板の表面に選択的に形成されたｎ型ＳｉＣ領域と、
前記ＳｉＣ基板の上に載置されたフィールド絶縁膜と、
前記フィールド絶縁膜中に前記ｎ型ＳｉＣ領域の表面を露出するように開口された開口部の内部において、前記フィールド絶縁膜から一定の間隙を隔てて配置された電極膜と、
前記開口部の内部において、前記フィールド絶縁膜から前記一定の間隙を隔て、且つ前記電極膜と前記ｎ型ＳｉＣ領域の間に配置された加熱反応層と、
前記開口部の内部において前記電極膜の表面に接し、且つ前記フィールド絶縁膜の上部にまで伸延された配線導体素片とからなることを特徴とするオーミック電極構造体。
【請求項２】　前記一定の間隙は、前記フィールド絶縁膜の厚みより小なることを特徴とする請求項１記載のオーミック電極構造体。
【請求項３】　前記フィールド絶縁膜は、
ＳｉＣの熱酸化膜と、
該熱酸化膜とは組成若しくは密度の異なる絶縁膜からなる上部絶縁膜との積層絶縁膜からなることを特徴とする請求項１又は２記載のオーミック電極構造体。
【請求項４】　前記上部絶縁膜の絶縁破壊電界強度は、前記熱酸化膜の絶縁破壊電界強度よりも低いことを特徴とする請求項１～３のいずれか１項記載のオーミック電極構造体。
【請求項５】　前記上部絶縁膜の緩衝フッ酸溶液によるエッチング速度が、前記熱酸化膜の前記緩衝フッ酸溶液によるエッチング速度よりも速いことを特徴とする請求項１～４のいずれか１項記載のオーミック電極構造体。
【請求項６】　炭化珪素（ＳｉＣ）基板の表面の少なくとも一部に高不純物密度を有するｎ型ＳｉＣ領域を形成する工程と、
前記ＳｉＣ基板の表面を洗浄する工程と、
前記ＳｉＣ基板の表面をフィールド絶縁膜で被覆する工程と、
前記フィールド絶縁膜の上部に前記フィールド絶縁膜とはエッチング速度の異なるマスク材を形成する工程と、
前記マスク材に窓部を設け、マスクパターンを形成する工程と、
該マスクパターンを用い、前記フィールド絶縁膜を前記ｎ型ＳｉＣ領域の表面が露出するまでエッチングし開口部を形成する工程と、
前記ｎ型ＳｉＣ領域の表面が露出後、更に前記フィールド絶縁膜をオーバーエッチングし、前記窓部近傍の前記マスク材の下部にアンダーカット部を形成する工程と、
前記マスク材の上部及び前記開口部の内部の前記ｎ型ＳｉＣ領域の表面に、第１の導体膜を堆積する工程と、
前記マスク材を除去することにより、前記前記開口部の内部の前記ｎ型ＳｉＣ領域の表面に、前記フィールド絶縁膜とは一定の間隙を隔て、前記第１の導体膜の素片を残留させる工程と、
非酸化性雰囲気中において、前記ＳｉＣ基板を熱処理し、前記第１の導体膜の素片と前記ｎ型ＳｉＣ領域との間に加熱反応層を生成する工程とを有することを特徴とするオーミック電極構造体の製造方法。
【請求項７】　前記フィールド絶縁膜で被覆する工程は、
熱酸化により、前記ＳｉＣ基板の表面に熱酸化膜を成長する工程と、
該熱酸化膜の上部に、熱酸化以外の方法で、絶縁膜を堆積する工程とからなることを特徴とする請求項６記載のオーミック電極構造体の製造方法。
【請求項８】　前記フィールド絶縁膜で被覆する工程は、
熱酸化以外の方法で、前記ＳｉＣ基板の表面に酸素透過性絶縁膜を堆積する工程と、
該酸素透過性絶縁膜の堆積後に、熱酸化により、前記ＳｉＣ基板の表面と前記酸素透過性絶縁膜との界面に、熱酸化膜を成長する工程とからなることを特徴とする請求項６記載のオーミック電極構造体の製造方法。
【請求項９】　前記マスク材を形成する工程は、フォトレジストを塗布する工程であることを特徴とする請求項６～８のいずれか１項記載のオーミック電極構造体の製造方法。
【請求項１０】前記フィールド絶縁膜に開口部を形成する工程において、前記ｎ型ＳｉＣ領域の表面が露出するに直前のステップは、ウェットエッチングと超純水によるリンスで完結されることを特徴とする請求項９記載のオーミック電極構造体の製造方法。
【請求項１１】　前記第１の導体膜の厚みは、前記ｎ型ＳｉＣ領域の厚みの１／２より薄いことを特徴とする請求項６～１０のいずれか１項記載のオーミック電極構造体の製造方法。
【請求項１２】　前記加熱反応層を生成する工程は、酸素（O_2）及び水（H_2O）の分圧が共に1×10^{-3}Ｐａ～1×10^{-10}Ｐａの非酸化性雰囲気中において、前記ＳｉＣ基板を熱処理することを特徴とする請求項６～１１のいずれか１項記載のオーミック電極構造体の製造方法。
【請求項１３】　前記第１の導体膜の素片に接し、且つ、前記フィールド絶縁膜の開口部を被覆するように、前記フィールド絶縁膜の上部に第２の導体膜を形成する工程を更に有することを特徴とする請求項６～１１のいずれか１項記載のオーミック電極構造体の製造方法。
【請求項１４】　前記第２の導体膜を形成する直前に、前記第１の導体膜の素片の表面に生成された酸化膜或いは付着したハイドロ・カーボンを除去する工程を付加し

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たことを特徴とする請求項１３記載のオーミック電極構造体の製造方法。
【請求項１５】　炭化珪素（ＳｉＣ）基板と、
前記ＳｉＣ基板の表面に選択的に形成されたｎ型ＳｉＣ領域からなる主電極領域と、
前記ＳｉＣ基板の上に載置されたフィールド絶縁膜と、
前記フィールド絶縁膜中に前記主電極領域の表面を露出するように開口された開口部の内部において、前記フィールド絶縁膜から一定の間隙を隔てて配置された電極膜と、
前記開口部の内部において、前記フィールド絶縁膜から前記一定の間隙を隔て、且つ前記電極膜と前記主電極領域の間に配置された加熱反応層と、
前記開口部の内部において前記電極膜の表面に接し、且つ前記フィールド絶縁膜の上部にまで伸延された主電極配線とからなることを特徴とする半導体装置。
【請求項１６】　前記一定の間隙は、前記フィールド絶縁膜の厚みより小なることを特徴とする請求項１５記載の半導体装置。
【請求項１７】　炭化珪素（ＳｉＣ）基板の表面の少なくとも一部に高不純物密度のｎ型ＳｉＣ領域からなる主電極領域を形成する工程と、
前記ＳｉＣ基板の表面を洗浄する工程と、
前記ＳｉＣ基板の表面をフィールド絶縁膜で被覆する工程と、
前記フィールド絶縁膜の上部に前記フィールド絶縁膜とはエッチング速度の異なるマスク材を形成する工程と、
前記マスク材に窓部を設け、マスクパターンを形成する工程と、
該マスクパターンを用い、前記フィールド絶縁膜を前記主電極領域の表面が露出するまでエッチングし開口部を形成する工程と、
前記主電極領域の表面が露出後、更に前記フィールド絶縁膜をオーバーエッチングし、前記窓部近傍の前記マスク材の下部にアンダーカット部を形成する工程と、
前記マスク材の上部及び前記開口部の内部の前記主電極領域の表面に、第１の導体膜を堆積する工程と、
前記マスク材を除去することにより、前記前記開口部の内部の前記主電極領域の表面に、前記フィールド絶縁膜とは一定の間隙を隔て、前記第１の導体膜の素片を残留させる工程と、
非酸化性雰囲気中において、前記ＳｉＣ基板を熱処理し、前記第１の導体膜の素片と前記主電極領域との加熱反応層を生成する工程とを有することを特徴とする半導体装置の製造方法。
【請求項１８】　前記フィールド絶縁膜で被覆する工程は、
熱酸化により、前記ＳｉＣ基板の表面に熱酸化膜を成長する工程と、
該熱酸化膜の上部に、熱酸化以外の方法で、絶縁膜を堆積する工程とからなることを特徴とする請求項１７記載の半導体装置の製造方法。
【請求項１９】　前記熱酸化膜を成長する工程の後に、前記熱酸化膜の上部に、ゲート電極を形成する工程を更に有することを特徴とする請求項１８記載の半導体装置の製造方法。
【請求項２０】　前記第１の導体膜の厚みは、前記主電極領域の厚みの１／２より薄いことを特徴とする請求項１７～１９のいずれか１項記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、炭化珪素（ＳｉＣ）基板を使用した半導体装置、及び半導体装置の製造方法に係り、更に、このＳｉＣ半導体装置に利用されるｎ型ＳｉＣ領域に対するオーミック電極構造体及びその製造方法に関するものである。
【０００２】
【従来の技術】ＳｉＣは、ｐｎ接合の形成が可能で、珪素（Ｓｉ）や砒化ガリウム（ＧａＡｓ）等の他の半導体材料に比べて禁制帯幅Ｅｇが広く３Ｃ－ＳｉＣで２．２３ｅＶ、６Ｈ－ＳｉＣで２．９３ｅＶ、４Ｈ－ＳｉＣで３．２６ｅＶ程度の値が報告されている。また、ＳｉＣは、熱的、化学的、機械的に安定で、耐放射線性にも優れているので、発光素子や高周波デバイスは勿論のこと、高温、大電力、放射線照射等の過酷な条件で、高い信頼性と安定性を示す電力用半導体装置（パワーデバイス）として様々な産業分野での適用が期待されている。
【０００３】特に、ＳｉＣを用いた高耐圧のＭＯＳＦＥＴは、Ｓｉを用いたパワーデバイスよりもオン抵抗が低いことが報告されている。また、ＳｉＣを用いたショットキーダイオードの順方向降下電圧が低くなることが報告されている。良く知られているように、パワーデバイスのオン抵抗とスイッチング速度とは、トレード・オフ関係にある。しかし、ＳｉＣを用いたパワーデバイスによれば、低オン抵抗化と高速スイッチング速度化が同時に達成出来る可能性がある。
【０００４】このＳｉＣを用いたパワーデバイスの低オン抵抗化には、オーミック・コンタクトに対するコンタクト抵抗ρｃの低減が重要な要素である。特に、低オン抵抗化のためには、パワーデバイスの主電極領域を細分化し、高密度にＳｉＣ基板上に配列する方法も採用される。このような、微細寸法化されたパワーデバイスの低オン抵抗化には、微細な開口部（コンタクト・ウィンドウ）の内部において、低いコンタクト抵抗ρｃを得ることが極めて重要となってくる。また、パワーデバイスの高速スイッチング速度化のためにも、ＳｉＣ領域に対するオーミック・コンタクトのコンタクト抵抗ρｃは大きな問題である。
【０００５】ＳｉＣ青色発光素子が既に実用化され量産

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されているのとは対称的に、パワーデバイス、高周波デバイスとしてのＳｉＣの応用は甚だ遅れている。この原因の一つは、これらデバイスの構造及び作製プロセスに適合した実用的な低抵抗のオーミック・コンタクトを形成する技術が未だに確立されていないからである。

【０００６】ｎ型ＳｉＣに低抵抗オーミック・コンタクトを形成する方法として広く活用されている従来技術は、ニッケル（Ｎｉ）、タングステン（Ｗ）、チタン（Ｔｉ）のような電極膜をｎ型ＳｉＣに被着させて形成したオーミック電極構造体を８００℃～１２００℃の高温で熱処理する方法である。なかでもＮｉを用いたオーミック・コンタクトでは$10^{-6}\Omega\cdot cm^2$台の実用的なコンタクト抵抗値ρcが得られており、極めて有望なオーミック・コンタクトである。

【０００７】図２４はパワーデバイスや高周波デバイスなどで使用されるＮｉ膜を用いたオーミック電極構造体の構造（以下において、「第１の従来技術」という。）を簡略化して示したものである。単結晶ＳｉＣ基板１の表面に高不純物密度のｎ型ＳｉＣ領域３２が形成されている。この単結晶ＳｉＣ基板１の表面には、更に熱酸化膜３及び上部絶縁膜４からなるフィールド絶縁膜５が形成されている。このフィールド絶縁膜５を貫通し、ｎ型ＳｉＣ領域３２の表面を露出するように、開口部が配置されている。フィールド絶縁膜５の開口部の内部には、ｎ型ＳｉＣ領域３２の表面に接した加熱反応層８と、この加熱反応層８の上部の電極膜（Ｎｉ膜素片）４７が配置されている。加熱反応層８は、Ｎｉ膜を全面蒸着し、フォトリソグラフィとエッチングを用いて、図２４に示す形状に、パターニングした後、熱処理することにより形成される。即ち、電極膜（Ｎｉ膜素片）４７を設けたＳｉＣ基板１を、１０００℃～１２００℃で高温処理することにより、Ｎｉ－Ｓｉ－Ｃが混合した導電性の加熱反応層８が形成される。電極膜（Ｎｉ膜素片）４７の上部には、フィールド絶縁膜５の上部に延伸するように配線導体素片９が配置されている。

【０００８】第１の従来技術は、後述するような問題点を有している。そこで、この第１の従来技術の問題を解決するため、特開平８－６４８０１号公報では、イオン注入で形成したｎ型ＳｉＣ領域３２に対するオーミック電極の形成法を開示している（以下において、「第２の従来技術」という。）。第２の従来技術に記載の方法は、

（イ）図２５（ａ）に示すように第１金属膜（Ｎｉ膜）４２をＳｉ酸化膜（フィールド絶縁膜）４３と隔絶するように開口部内に配置する；

（ロ）その後、高温熱処理を実施し、図２５（ｂ）に示すようにオーミック接触片４５を生成する；

（ハ）最後に、図２５（ｃ）に示すように、オーミック接触片４５及び露出したｎ型ＳｉＣ領域３２の表面に対して、第２金属膜を接続する、という手順による方法である。

【０００９】

【発明が解決しようとする課題】先ず、図２４に示す第１の従来技術によるｎ型ＳｉＣ領域３２に対するオーミック電極構造体にあっては、

１）Ｎｉ膜４７とフィールド絶縁膜５の接着力が弱く、しばしば蒸着後にＮｉ膜４７が剥落するため、製造歩留まりが悪い；

２）Ｎｉ膜４７との接触面にあるフィールド絶縁膜（SiO_2膜）５が、高温熱処理でＮｉ膜４７と反応し（還元され）、SiO_2膜５が浸食され、薄くなる。SiO_2膜５が、もともと薄い場合は、SiO_2膜５の絶縁性が損なわれ、はなはだしい場合は、SiO_2膜５が貫通する；

３）Ｎｉ－ＳｉＣ－SiO_2が共存し、３元系の反応が生じる加熱反応層８の外縁コーナ部S_1，S_2直下においては、高温熱処理により、寄生のショットキー接合が形成され、水平方向の電流の流れを阻害する；

４）高温熱処理で電極膜（Ｎｉ膜素片）４７の表面が激しく荒れ、表面モホロジーが低下する。このため、フォトリソグラフィ工程用のアライメント・マークが、同様なＮｉ膜４７を有する構造であれば、その形成が困難となる。従って、後続の工程において高精度なフォトリソグラフィならびにエッチングが出来ない；

５）高温熱処理で電極膜（Ｎｉ膜素片）４７表面に、ＮｉＯやSiO_2等の酸化膜やハイドロ・カーボンが生じ、電極膜（Ｎｉ膜素片）４７と配線導体素片９間のコンタクト抵抗が実質的に、上昇するという問題があった。

【００１０】第２の従来技術では、この第１の従来技術の問題点のうち、２）と３）の問題を解決する方法である。即ち、オーミック接触片４５がＳｉ酸化膜（フィールド絶縁膜）４３と隔絶しており、露出したｎ型ＳｉＣ領域３２の表面に接している第２金属膜は、熱処理しないので、第１の従来技術のＮｉ－ＳｉＣ－SiO_2の共存に起因した寄生のショットキー接合が形成されないという特徴を有する。

【００１１】しかし、第２の従来技術は、図２５（ａ）に示す開口部内に、第１金属膜（Ｎｉ膜）４２をＳｉ酸化膜（フィールド絶縁膜）４３と隔絶してパターニングする具体的な方法がなんら開示されていない。通例、このような場合、用いられる方法は、ＳｉＣ基板１全面にＮｉ膜を全面蒸着し、フォトリソグラフィとＮｉのエッチングを用いて、開口部の内部に選択的に第１金属膜（Ｎｉ膜）４２を配設する方法である。しかし、第２の従来技術とこの方法の組み合わせでは基本的に１）、４）、５）の問題を解決することは出来ない。

【００１２】更に、第１金属膜（Ｎｉ膜）４２のパターニング工法において独立したフォトリソグラフィ工程を用いているために、露光装置（マスクアライナー）の合

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わせ精度及び第１金属膜（Ｎｉ膜）４２のエッチング加工精度を考慮すると、オーミック接触片４５とＳｉ酸化膜（フィールド絶縁膜）４３の開口部側壁との間隔のトレランスを十分大きくとらなければならないという問題がある。これは、集積密度が高く、微細なオーミック電極構造体の製作を困難にするという問題に結びつく。ひいては、デバイス寸法やチップ面積が増大する、半導体装置の生産コスト（チップ単価）が上昇するという問題に連鎖する。

【００１３】本発明はこのような従来のｎ型ＳｉＣ領域に対するオーミック電極構造体、及びこれを用いた半導体装置の問題点をそれぞれ、或いは、同時に解決するためになされたものである。

【００１４】具体的には、本発明は、$10^{-7}\Omega cm^2$台程度の実用的なコンタクト抵抗を有するｎ型ＳｉＣ領域に対する微細なオーミック電極構造体の新規な構造を提供することを目的とする。

【００１５】本発明の他の目的は、表面金属配線（配線導体素片）とフィールド絶縁膜の接着力が良好で、信頼性の高いオーミック電極構造体の新規な構造を提供することである。

【００１６】本発明の更に他の目的は、フィールド絶縁膜の絶縁性が維持出来、高耐圧、低リーク電流のオーミック電極構造体の新規な構造を提供することである。

【００１７】本発明の更に他の目的は、オーミック電極の外縁部に寄生ショットキー接合が存在しないオーミック電極構造体の新規な構造を提供することである。

【００１８】本発明の更に他の目的は、電極膜の表面モホロジーが良好なオーミック電極構造体の新規な構造を提供することである。

【００１９】本発明の更に他の目的は、微細な寸法精度を有したオーミック電極構造体を提供することである。

【００２０】本発明の更に他の目的は、導体膜堆積後に表面金属配線の剥落等の不良が抑制され、製造歩留まりの高いオーミック電極構造体の製造方法を提供することである。

【００２１】本発明の更に他の目的は、オーミック電極の母材となる導体膜とフィールド絶縁膜との浸食反応（還元反応）が有効に回避出来るオーミック電極構造体の製造方法を提供することである。

【００２２】本発明の更に他の目的は、オーミック電極の母材となる導体膜、ＳｉＣ及びフィールド絶縁膜との３元系の反応が回避されるオーミック電極構造体の製造方法を提供することである。

【００２３】本発明の更に他の目的は、高温熱処理を経た後でも、電極膜の表面モホロジーが良好なオーミック電極構造体の製造方法を提供することである。

【００２４】本発明の更に他の目的は、フォトリソグラフィ工程用のアライメント・マークの形態に影響を与えず、後続の工程において高精度なフォトリソグラフィならびにエッチングを容易にするなオーミック電極構造体の製造方法を提供することである。

【００２５】本発明の更に他の目的は、高温熱処理を経た後でも、電極膜の表面に、酸化膜やハイドロ・カーボンが生じず、電極膜と配線導体素片間のコンタクト抵抗を低く維持出来るオーミック電極構造体の製造方法を提供することである。

【００２６】本発明の更に他の目的は、フォトリソグラフィ工程における露光装置の合わせ精度及びエッチング加工精度に影響されずに、電極膜（オーミック接触片）とフィールド絶縁膜の開口部側壁との間隔を十分に微細化することが可能なオーミック電極構造体の製造方法を提供することである。

【００２７】本発明の更に他の目的は、微細な寸法精度を有したオーミック電極構造体が簡単に製造出来るオーミック電極構造体の製造方法を提供することである。

【００２８】本発明の更に他の目的は、高耐圧且つ高速動作可能な半導体装置を提供することである。

【００２９】本発明の更に他の目的は、オン抵抗が低く、且つ高速スイッチング可能な半導体装置を提供することである。

【００３０】本発明の更に他の目的は、チップ占有面積が小さく、チップ単価が低く、且つ信頼性の高い半導体装置を提供することである。

【００３１】本発明の更に他の目的は、表面金属配線の剥落等の不良が抑制され、製造歩留まりの高い半導体装置の製造方法を提供することである。

【００３２】本発明の更に他の目的は、オーミック電極の母材となる導体膜とフィールド絶縁膜との高温熱処理での浸食反応（還元反応）が有効に回避出来、且つ導体膜、ＳｉＣ及びフィールド絶縁膜との３元系の反応をも回避出来る半導体装置の製造方法を提供することである。

【００３３】本発明の更に他の目的は、高温熱処理を経た後でも、電極膜の表面モホロジーが良好で、フォトリソグラフィ工程用のアライメント・マークの形態に影響を与えず、後続の工程において高精度なフォトリソグラフィならびにエッチングが可能な半導体装置の製造方法を提供することである。

【００３４】本発明の更に他の目的は、高温熱処理を経た後でも、電極膜の表面に、酸化膜やハイドロ・カーボンが生じず、電極膜と配線導体素片間のコンタクト抵抗を低く維持出来る半導体装置の製造方法を提供することである。

【００３５】本発明の更に他の目的は、電極膜（オーミック接触片）とフィールド絶縁膜の開口部側壁との間隔を十分に微細化し、微細な寸法精度を有したオーミック電極構造体が簡単に製造出来る半導体装置の製造方法を提供することである。

【００３６】本発明の更に他の目的は、チップ面積の縮

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小が可能で、チップ単価が低く出来る半導体装置の製造方法を提供することである。

【００３７】

【課題を解決するための手段】上記目的を達成するために、請求項１記載の発明は、（イ）ＳｉＣ基板と、（ロ）ＳｉＣ基板の表面に選択的に形成されたｎ型ＳｉＣ領域と、（ハ）ＳｉＣ基板の上に載置されたフィールド絶縁膜と、（ニ）フィールド絶縁膜中にｎ型ＳｉＣ領域の表面を露出するように開口された開口部（コンタクト・ウィンドウ）の内部において、フィールド絶縁膜から一定の間隙を隔てて配置された電極膜と、（ホ）フィールド絶縁膜の開口部の内部において、フィールド絶縁膜から一定の間隙を隔て、且つ電極膜とｎ型ＳｉＣ領域の間に配置された加熱反応層と、（ヘ）フィールド絶縁膜の開口部の内部において、電極膜の表面に接し、且つフィールド絶縁膜の上部にまで伸延された配線導体素片とからなるオーミック電極構造体であることを要旨とする。請求項１記載の発明によれば、電極膜及び加熱反応層が共に、フィールド絶縁膜の開口部の内部において、フィールド絶縁膜から一定の間隙を隔て配置されているので、電極膜及び加熱反応層を構成する金属材料が、フィールド絶縁膜と反応することが防止出来る。更に、加熱反応層の底部外縁部における金属－ＳｉＣ－SiO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来る。

【００３８】なお、請求項１に規定する「ＳｉＣ基板の表面に選択的に形成されたｎ型ＳｉＣ領域」は、ＳｉＣ基板の表面に、直接ｎ型ＳｉＣ領域が形成される場合のみに限定されないことは勿論である。例えば、ＳｉＣ基板の表面の一部に、ｎ型ＳｉＣ領域よりも平面上の面積の大きい他の半導体領域をウェル形状に配置し、そのウェル形状の半導体領域の内部の位置において、本発明のｎ型ＳｉＣ領域が形成されていても良い。或いは、ＳｉＣ基板の表面の全面に他の半導体領域をエピタキシャル成長し、そのエピタキシャル成長した他の半導体領域の表面の一部において、本発明のｎ型ＳｉＣ領域を形成するような場合も許容される。このように、請求項１記載に係る発明においては、ｎ型ＳｉＣ領域が他の半導体領域を介して、間接的に形成される場合を許容することに留意すべきである。

【００３９】請求項２記載の発明は、請求項１記載のオーミック電極構造体において、一定の間隙は、フィールド絶縁膜の厚みより小なることを要旨とする。

【００４０】請求項３記載の発明は、請求項１又は２記載のオーミック電極構造体において、フィールド絶縁膜は、ＳｉＣの熱酸化膜と、この熱酸化膜とは組成若しくは密度の異なる絶縁膜からなる上部絶縁膜との積層絶縁膜からなることを要旨とする。

【００４１】請求項４記載の発明は、請求項１～３のいずれか１項記載のオーミック電極構造体において、上部絶縁膜の絶縁破壊電界強度は、熱酸化膜の絶縁破壊電界強度よりも低いことを要旨とする。

【００４２】請求項５記載の発明は、請求項１～４のいずれか１項記載のオーミック電極構造体において、上部絶縁膜の緩衝フッ酸溶液（ＢＨＦ溶液）によるエッチング速度が、熱酸化膜の緩衝フッ酸溶液によるエッチング速度よりも速いことを要旨とする。「ＢＨＦ溶液」とは、フッ化アンモニウム（NH_4F）：フッ酸（ＨＦ）＝７：１の溶液からなる当業者周知のシリコン酸化膜（SiO_2膜）のエッチング液（エッチャント）である。

【００４３】請求項６記載の発明は、（イ）ＳｉＣ基板の表面の少なくとも一部に高不純物密度を有するｎ型ＳｉＣ領域を形成する工程と、（ロ）ＳｉＣ基板の表面を洗浄する工程と、（ハ）ＳｉＣ基板の表面をフィールド絶縁膜で被覆する工程と、（ニ）フィールド絶縁膜の上部にフィールド絶縁膜とはエッチング速度の異なるマスク材を形成する工程と、（ホ）マスク材に窓部を設け、マスクパターンを形成する工程と、（ヘ）このマスクパターンを用い、フィールド絶縁膜をｎ型ＳｉＣ領域の表面が露出するまでエッチングし開口部を形成する工程と、（ト）ｎ型ＳｉＣ領域の表面が露出後、更にフィールド絶縁膜をオーバーエッチングし、窓部近傍のマスク材の下部にアンダーカット部を形成する工程と、（チ）マスク材の上部及び開口部の内部のｎ型ＳｉＣ領域の表面に、第１の導体膜を堆積する工程と、（リ）マスク材を除去することにより、開口部の内部のｎ型ＳｉＣ領域の表面に、フィールド絶縁膜とは一定の間隙を隔て、第１の導体膜の素片を残留させる工程と、（ヌ）非酸化性雰囲気中において、ＳｉＣ基板を熱処理し、第１の導体膜の素片とｎ型ＳｉＣ領域との間に加熱反応層を生成する工程とを有するオーミック電極構造体の製造方法であることを要旨とする。請求項６記載の発明によれば、フィールド絶縁膜の「オーバーエッチング（スライト・エッチング）」のエッチング量の制御により、窓部近傍のマスク材の下部に形成されるアンダーカット部の深さが制御出来る。また、このアンダーカット部の深さにより、第１の導体膜の素片とフィールド絶縁膜との一定の間隙を自己整合的に決定出来る。請求項１と同様に、請求項６に規定する「ＳｉＣ基板の表面の少なくとも一部に高不純物密度を有するｎ型ＳｉＣ領域を形成する工程」は、ＳｉＣ基板の表面に、直接ｎ型ＳｉＣ領域を形成する場合のみに限定されない。例えば、ＳｉＣ基板の表面の一部に他の半導体領域をウェル形状に形成し、そのウェル形状の半導体領域の内部にｎ型ＳｉＣ領域を形成しても良い。或いは、ＳｉＣ基板の表面の全面に他の半導体領域をエピタキシャル成長し、そのエピタキシャル成長した半導体領域の表面の一部にｎ型ＳｉＣ領域を形成するような工程も許容される。

【００４４】請求項７記載の発明は、請求項６記載のオーミック電極構造体の製造方法において、フィールド絶

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縁膜で被覆する工程は、熱酸化により、ＳｉＣ基板の表面に熱酸化膜を成長する工程と、この熱酸化膜の上部に、熱酸化以外の方法で、絶縁膜を堆積する工程とからなることを要旨とする。

【００４５】請求項８記載の発明は、請求項６記載のオーミック電極構造体の製造方法において、フィールド絶縁膜で被覆する工程は、熱酸化以外の方法で、ＳｉＣ基板の表面に酸素透過性絶縁膜を堆積する工程と、この酸素透過性絶縁膜の堆積後に、熱酸化により、ＳｉＣ基板の表面と酸素透過性絶縁膜との界面に、熱酸化膜を成長する工程とからなることを要旨とする。

【００４６】請求項９記載の発明は、請求項６～８のいずれか１項記載のオーミック電極構造体の製造方法において、マスク材を形成する工程は、フォトレジストを塗布する工程であることを要旨とする。

【００４７】請求項１０記載の発明は、請求項９記載のオーミック電極構造体の製造方法が、フィールド絶縁膜に開口部を形成する工程において、ｎ型ＳｉＣ領域の表面が露出するに直前のステップは、ウェットエッチングと超純水によるリンスで完結されることを要旨とする。

【００４８】請求項１１記載の発明は、請求項６～１０のいずれか１項記載のオーミック電極構造体の製造方法において、第１の導体膜の厚みは、ｎ型ＳｉＣ領域の厚みの１／２より薄いことを要旨とする。請求項１１記載の発明によれば、加熱反応層を形成する前の第１の導体膜の素片の厚みが、その下部にあるｎ型ＳｉＣ領域の厚みの１／２より薄くなるように、予め設定されているので、ＳｉＣ基板の熱処理により、仮に第１の導体膜の素片が完全に加熱反応層に転化したとしても、ｎ型ＳｉＣ領域が消失することはない。

【００４９】請求項１２記載の発明は、請求項６～１１のいずれか１項記載のオーミック電極構造体の製造方法において、加熱反応層を生成する工程は、酸素（O_2）及び水（H_2O）の分圧が共に1×10^{-3}Ｐａ～1×10^{-10}Ｐａの非酸化性雰囲気中でＳｉＣ基板を熱処理することを要旨とする。請求項１２記載の発明によれば、酸素及び水の分圧が共に1×10^{-3}Ｐａ～1×10^{-10}Ｐａに制御された非酸化性雰囲気中で熱処理して、加熱反応層を生成しているので、加熱反応層生成のための高温熱処理で、第１の導体膜の素片の表面に酸化膜が生じることを防止出来る。

【００５０】請求項１３記載の発明は、請求項６～１１のいずれか１項記載のオーミック電極構造体の製造方法において、第１の導体膜の素片に接し、且つ、フィールド絶縁膜の開口部を被覆するように、フィールド絶縁膜の上部に第２の導体膜を形成する工程を更に有することを要旨とする。

【００５１】請求項１４記載の発明は、請求項１３記載のオーミック電極構造体の製造方法において、第２の導体膜を形成する直前に、第１の導体膜の素片の表面に生成された酸化膜或いは付着したハイドロ・カーボンを除去する工程を付加したことを要旨とする。

【００５２】請求項１５記載の発明は、（イ）ＳｉＣ基板と、（ロ）ＳｉＣ基板の表面に選択的に形成されたｎ型ＳｉＣ領域からなる主電極領域と、（ハ）ＳｉＣ基板の上に載置されたフィールド絶縁膜と、（ニ）フィールド絶縁膜中に主電極領域の表面を露出するように開口された開口部の内部において、フィールド絶縁膜から一定の間隙を隔てて配置された電極膜と、（ホ）フィールド絶縁膜の開口部の内部において、フィールド絶縁膜から一定の間隙を隔て、且つ電極膜と主電極領域の間に配置された加熱反応層と、（ヘ）フィールド絶縁膜の開口部の内部において、電極膜の表面に接し、且つフィールド絶縁膜の上部にまで伸延された主電極配線とからなる半導体装置であることを要旨とする。請求項１５記載の発明において、「主電極領域」とは半導体装置の主電流の通路の両端にそれぞれ位置し、互いに対向した半導体領域の少なくとも一方である。請求項１５記載の発明によれば、主電極領域に対するオーミック電極を構成する電極膜及び加熱反応層が共に、フィールド絶縁膜の開口部の内部において、フィールド絶縁膜から一定の間隙を隔て配置されているので、電極膜及び加熱反応層を構成する金属材料が、フィールド絶縁膜と反応することが防止出来る。更に、オーミック電極の底部外縁部における金属－ＳｉＣ－SiO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来る。請求項１において説明したように、請求項１５に規定する「ＳｉＣ基板の表面に選択的に形成されたｎ型ＳｉＣ領域からなる主電極領域」は、ＳｉＣ基板の表面に、直接ｎ型ＳｉＣ領域からなる主電極領域が形成される場合のみに限定されない。例えば、ＳｉＣ基板の表面の一部に他の半導体領域をウェル形状に配置し、そのウェル形状の半導体領域の内部に主電極領域が形成されていても良い。或いは、ＳｉＣ基板の表面の全面に他の半導体領域をエピタキシャル成長し、そのエピタキシャル成長した半導体領域の表面の一部に主電極領域を形成するような場合も許容される。

【００５３】請求項１６記載の発明は、請求項１５記載の半導体装置において、一定の間隙は、フィールド絶縁膜の厚みより小なることを要旨とする。

【００５４】請求項１７記載の発明は、（イ）ＳｉＣ基板の表面の少なくとも一部に高不純物密度のｎ型ＳｉＣ領域からなる主電極領域を形成する工程と、（ロ）ＳｉＣ基板の表面を洗浄する工程と、（ハ）ＳｉＣ基板の表面をフィールド絶縁膜で被覆する工程と、（ニ）フィールド絶縁膜の上部にフィールド絶縁膜とはエッチング速度の異なるマスク材を形成する工程と、（ホ）マスク材に窓部を設け、マスクパターンを形成する工程と、（ヘ）このマスクパターンを用い、フィールド絶縁膜を主電極領域の表面が露出するまでエッチングし開口部を

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形成する工程と、（ト）主電極領域の表面が露出後、更にフィールド絶縁膜をオーバーエッチングし、窓部近傍のマスク材の下部にアンダーカット部を形成する工程と、（チ）マスク材の上部及び開口部の内部の主電極領域の表面に、第１の導体膜を堆積する工程と、（リ）マスク材を除去することにより、開口部の内部の主電極領域の表面に、フィールド絶縁膜とは一定の間隙を隔て、第１の導体膜の素片を残留させる工程と、（ヌ）非酸化性雰囲気中において、ＳｉＣ基板を熱処理し、第１の導体膜の素片と主電極領域との加熱反応層を生成する工程とを有する半導体装置の製造方法であることを要旨とする。請求項１７記載の発明の「主電極領域」とは、請求項１５記載の発明で定義したように、半導体装置の主電流の通路の両端に位置する半導体領域である。請求項１７記載の発明によれば、半導体装置の主電極領域に対するオーミック電極を形成する際に、フィールド絶縁膜のオーバーエッチング（スライト・エッチング）のエッチング量の制御により、窓部近傍のマスク材の下部に形成されるアンダーカット部の深さが制御出来る。また、このアンダーカット部の深さにより、第１の導体膜の素片とフィールド絶縁膜との一定の間隙を自己整合的に決定出来る。請求項１５と同様に、請求項１７に規定する「ＳｉＣ基板の表面の少なくとも一部に高不純物密度のｎ型ＳｉＣ領域からなる主電極領域を形成する工程」は、ＳｉＣ基板の表面に、直接ｎ型ＳｉＣ領域からなる主電極領域を形成する場合のみに限定されない。例えば、ＳｉＣ基板の表面の一部に、他の半導体領域をウェル形状に形成し、そのウェル形状の半導体領域の内部に主電極領域を形成しても良い。或いは、ＳｉＣ基板の表面の全面に他の半導体領域をエピタキシャル成長し、その半導体領域の表面の一部に主電極領域を形成するような工程でも良い。

【００５５】請求項１８記載の発明は、請求項１７記載の半導体装置の製造方法において、フィールド絶縁膜で被覆する工程は、熱酸化により、ＳｉＣ基板の表面に熱酸化膜を成長する工程と、この熱酸化膜の上部に、熱酸化以外の方法で、絶縁膜を堆積する工程とからなることを要旨とする。

【００５６】請求項１９記載の発明は、請求項１８記載の半導体装置の製造方法において、熱酸化膜を成長する工程の後に、熱酸化膜の上部に、ゲート電極を形成する工程を更に有することを要旨とする。

【００５７】請求項２０記載の発明は、請求項１７～１９のいずれか１項記載の半導体装置の製造方法において、第１の導体膜の厚みは、主電極領域の厚みの１／２より薄いことを要旨とする。

【００５８】

【発明の効果】請求項１記載の発明によれば、電極膜及び加熱反応層を構成する金属材料が、フィールド絶縁膜と反応することが防止され、金属材料との接触面にあるフィールド絶縁膜が高温熱処理で還元（浸食）されることがないので、フィールド絶縁膜の絶縁性が維持出来る。また、電極膜を構成する金属材料がフィールド絶縁膜に接していないので、電極膜とフィールド絶縁膜の接着力が弱いという問題は、本来的に存在しない。このため、製造プロセス終了後に電極膜が剥落することはなく、製造歩留まりが高くなる。更に、加熱反応層の底部外縁部における金属－ＳｉＣ－SiO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来るので、低いコンタクト抵抗が達成出来る。また、寄生のショットキー接合の生成に伴うｎ型ＳｉＣ領域の水平方向の電流の流れの阻害もない。

【００５９】請求項２記載の発明によれば、電極膜及び加熱反応層の周縁部と開口部側壁との間の間隙を、フィールド絶縁膜の厚みより小さい微細寸法としたため、オーミック電極構造体の占有面積を小さく出来る。

【００６０】請求項３記載の発明によれば、フィールド絶縁膜の下部に、ＳｉＣの酸化膜を有している。ＳｉＣの熱酸化膜は、Ｓｉの熱酸化膜に近いシリコン酸化膜（SiO_2膜）であり、ＳｉＣとの界面準位が少なく、高い絶縁破壊電界強度が維持出来る。また、熱酸化膜とは組成若しくは密度の異なる絶縁膜からなる上部絶縁膜と熱酸化膜との積層構造にしているので、熱酸化膜の厚さを薄く設定できる。このため、過剰な熱酸化による表面モホロジーの低下もない。表面モホロジーが良好であるため、良好な金属・半導体接合が保証できる。従って、界面準位に起因した寄生トランジスタの生成が抑制され、信頼性の高いフィールド絶縁膜の開口部に、低いコンタクト抵抗のオーミック電極構造体を構成出来る。

【００６１】ＳｉＣの熱酸化膜の絶縁破壊電界強度は、厚さ１０ｎｍで１４ＭＶ／ｃｍ程度である。熱酸化以外の方法で形成したSiO_2膜の絶縁破壊電界強度は、この値よりも小さい。即ち、請求項４記載に係る発明によれば、ＳｉＣの熱酸化膜以外の種々の絶縁膜を、ＳｉＣの熱酸化膜の上部に形成して、半導体装置の仕様として要求される耐圧を確保しつつ、低い界面準位と良好な表面モホロジーを有したフィールド絶縁膜の開口部に、オーミック電極構造体を構成出来る。

【００６２】上記のように、ＳｉＣの熱酸化膜は、Ｓｉ熱酸化膜に近いSiO_2膜であるので、ＢＨＦ溶液に対するエッチング速度は１００ｎｍ／分程度である。これに比し、ＣＶＤで堆積したSiO_2膜に対するエッチング速度は１．５倍から３倍位高い。即ち、請求項５記載に係る発明によれば、ＳｉＣの熱酸化膜以外の種々のSiO_2膜を、ＳｉＣの熱酸化膜の上部に形成しているので、要求される耐圧、低い界面準位、表面の安定性、良好な表面モホロジーを有したフィールド絶縁膜の開口部に、所望のオーミック電極構造体を構成出来る。また、ＢＨＦ溶液に対するエッチング速度の相違を利用して、種々の半導体プロセスを採用出来るので、多様なオーミ

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ック電極構造体を構成出来る。

【００６３】請求項６記載の発明によれば、フィールド絶縁膜に対するオーバーエッチングのエッチング時間の制御により、窓部近傍のマスク材の下部に形成されるアンダーカット部の深さが制御出来るので、寸法制御が容易である。また、このアンダーカット部の深さにより、第１の導体膜の素片とフィールド絶縁膜との一定の間隙を自己整合的に決定出来るので、第１の導体膜の素片とフィールド絶縁膜との一定の間隙を制御するためのフォトリソグラフィ工程は不要である。このため、電極膜となる第１の導体膜の素片とフィールド絶縁膜の開口部側壁との間隔を十分に小さく出来、占有面積の小さく、微細寸法を有したオーミック電極構造体を製造出来る。更に、フォトリソグラフィ工程が省略出来るため、工程数が減少し、製造歩留まりが高くなる。更に、請求項６記載の発明は、標準的なＳｉ半導体デバイス製造方法が適用可能なので、容易且つ信頼性が高い。更に、第１の導体膜の素片が、フィールド絶縁膜と反応することが防止出来るので、第１の導体膜の素片を構成する金属材料との接触面にあるフィールド絶縁膜が高温熱処理で還元（浸食）されることがなく、フィールド絶縁膜の絶縁性が維持出来る。また、第１の導体膜の素片を構成する金属材料がフィールド絶縁膜に接していないので、第１の導体膜の素片から生成された電極膜とフィールド絶縁膜の接着力が弱いという問題は、本来的に存在しない。このため、プロセス終了後に電極膜が剥落することはなく、製造歩留まりが高くなる。更に、加熱反応層を生成する工程において、第１の導体膜の素片の底部外縁部における金属－ＳｉＣ－SiO_2の３元系の共存する状態が存在しないので、３元系の反応による寄生のショットキー接合の生成も回避出来、低いコンタクト抵抗が達成出来る。また、寄生のショットキー接合の生成に伴うｎ型ＳｉＣ領域の水平方向の電流の流れの阻害もない。

【００６４】請求項７記載の発明によれば、ＳｉＣ基板表面にフィールド絶縁膜を形成する工程は、ＳｉＣ表面を薄く熱酸化させた後、熱酸化膜の上部に、熱酸化以外の方法で厚い絶縁膜を堆積することによって達成しているので、ＳｉＣの表面モホロジーを、過度な熱酸化により荒らすことない。また、熱酸化以外の方法は、ＣＶＤ法やスパッタリング法等の周知の物理的或いは化学的手段が採用可能であるが、これらの、熱酸化以外の方法に固有な自然酸化膜やハイドロ・カーボンのＳｉＣ界面（表面）への生成を、熱酸化により効果的に除去、若しくは抑制出来る。つまり、加熱反応層の形成の障害となるＳｉＣ表面の自然酸化膜とハイドロカーボンを除去することが可能であるので、$10^{-7}\Omega cm^2$台程度の低いコンタクト抵抗が簡単に実現出来る。

【００６５】請求項８記載の発明によれば、熱酸化以外の方法でＳｉＣ基板の表面に酸素透過性絶縁膜を堆積する工程を先に行い、この酸素透過性絶縁膜の堆積後に、熱酸化によりＳｉＣ基板の表面と酸素透過性絶縁膜との界面に熱酸化膜を成長して、フィールド絶縁膜を形成している。この場合も、請求項７記載に係る発明と同様に、過度の熱酸化によるＳｉＣ基板の表面モホロジーの劣化を抑制することが出来る。また、ＣＶＤ法やスパッタリング法等の周知の物理的或いは化学的手段に固有な自然酸化膜やハイドロ・カーボンの生成を、熱酸化膜の生成により効果的に除去、若しくは抑制出来る。このため、加熱反応層とｎ型ＳｉＣ領域との界面のモホロジーが良好となり、均一且つ均質な加熱反応層を生成出来る。従って、$10^{-7}\Omega cm^2$台程度の低いコンタクト抵抗ρcを簡単に得ることが出来る。

【００６６】請求項９記載の発明によれば、半導体製造プロセスで周知のフォトレジストを使うことが出来るので、フォトリソグラフィ工程で簡単に、フィールド絶縁膜に開口部を形成するためのマスクパターンを形成出来る。更に、このマスクパターンをそのまま用いて、フォトレジストの上部に第１の導体膜を堆積すれば、その後、フォトレジストを剥離剤等で簡単に除去出来るので、リフトオフ工程も簡単に実施出来る。

【００６７】請求項１０記載に係る発明によれば、フィールド絶縁膜中に設ける開口部（凹部）の底面がｎ型ＳｉＣ領域の表面に到達する最終ステップが、ウェット・エッチングと超純水によるリンスで完結されるので、ドライ・エッチングの反応生成物であるハイドロ・カーボンのｎ型ＳｉＣ領域の表面への再付着や、過剰なプラズマエネルギによるエッチング損傷が防止出来る。このため、開口部に露出したｎ型ＳｉＣ領域の表面の汚染やｎ型ＳｉＣ領域の表面の粗面化が有効に防止出来る。加えて、ドライ・エッチングが使用出来るため、微細な開口部寸法を有したオーミック・コンタクトが形成出来る。このため、半導体集積回路の高集積密度化や、電力用半導体装置のオン抵抗の低減等に好適なオーミック電極構造体の製造が可能になる。

【００６８】請求項１１記載の発明によれば、加熱反応層を形成する前の第１の導体膜の素片の厚みが制御されているので、仮に第１の導体膜の素片が完全に加熱反応層に転化したとしても、ｎ型ＳｉＣ領域が消失したり、加熱反応層がｎ型ＳｉＣ領域を突き抜けることが確実に防止出来る。従って、ｎ型ＳｉＣ領域の消失に伴うコンタクト抵抗の急増や、ｎ型ＳｉＣ領域の突き抜けに伴うリーク電流の増大を有効に防止出来る。更に、加熱反応層形成のためのＳｉＣ基板の熱処理工程のプロセス・マージンが十分に取れ、十分な熱処理が可能で、より低いコンタクト抵抗の実現を可能にする。

【００６９】請求項１２記載の発明によれば、酸素及び水の分圧が制御された非酸化性雰囲気中で熱処理し、加熱反応層を生成しているので、加熱反応層生成のための高温熱処理で第１の導体膜の素片の表面に酸化膜が生じることを防止出来る。このため、第１の導体膜の素片か

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ら構成された電極膜と、この電極膜に接続される上層の第２の導体膜との間のコンタクト抵抗が低減出来る。更に、酸素及び水の分圧が制御された非酸化性雰囲気中で熱処理することにより、高温熱処理中に、酸素或いは酸素含有雰囲気が原因で起こる第１の導体膜の素片の表面の荒れが防止出来る。このため、同様な工程と構造で形成されるアライメント・マークの表面モホロジーも良好であるので、後続の工程において高精度なフォトリソグラフィならびにエッチングが可能となる。

【００７０】請求項１３記載の発明によれば、第１の導体膜の素片に接し、且つ、フィールド絶縁膜の開口部を被覆するように第２の導体膜を配設し、これにより配線導体素片を形成出来るので、現実の半導体装置の電極構造に対応したオーミック電極構造体を簡単に製造出来る。また、第２の導体膜に対しては、高温の熱処理が不要であるので、第２の導体膜を構成する材料との接触面にあるフィールド絶縁膜が高温熱処理で還元（浸食）されることがないので、フィールド絶縁膜の絶縁性が維持出来る。

【００７１】請求項１４記載の発明によれば、仮に、高温熱処理で第１の導体膜の素片の表面に酸化膜が生成され場合や、ハイドロ・カーボンが付着した場合であっても、これらの酸化膜やハイドロ・カーボンを有効に除去出来る。このため、第１の導体膜の素片の表面の酸化膜やハイドロ・カーボンに起因した第１の導体膜の素片と第２の導体膜コンタクト抵抗の上昇を回避出来る。

【００７２】請求項１５記載の発明によれば、半導体装置の主電極領域に対するオーミック電極において、オーミック電極の電極膜及び加熱反応層を構成する金属材料が、フィールド絶縁膜と反応しない構造になっているので、金属材料との接触面にあるフィールド絶縁膜が高温熱処理で還元（浸食）されることがない。このため、半導体装置の主電極領域の周辺に形成されたフィールド絶縁膜の高い絶縁性が維持出来、リーク電流も低減出来る。また、電極膜を構成する金属材料がフィールド絶縁膜に接していないので、オーミック電極の電極膜とフィールド絶縁膜の接着力が弱いという問題は、本来的に存在しない。このため、半導体装置の製造プロセス終了後にオーミック電極の電極膜が剥落することはなく、半導体装置の製造歩留まりが高くなる。更に、オーミック電極の底部外縁部における金属－ＳｉＣ－SiO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来るので、低いコンタクト抵抗のオーミック電極が達成出来る。また、寄生のショットキー接合の生成に伴う主電極領域中の水平方向の電流の流れの阻害もない。この結果、高耐圧で且つ高速に動作可能な半導体装置が実現出来る。特に、電力用半導体装置においては、低いオン抵抗と高速なスイッチングを同時に達成出来る。

【００７３】請求項１６記載の発明によれば、電極膜及び加熱反応層の周縁部と開口部側壁との間の間隙を、フィールド絶縁膜の厚みより小さい微細寸法としたため、主電極領域に対するオーミック電極の占有面積を小さく出来、半導体装置の集積密度を向上出来る。特に、微細な構造のオーミック電極を多数配列することにより、電力用半導体装置の低いオン抵抗と高速なスイッチングを同時に達成出来る。

【００７４】請求項１７記載の発明によれば、半導体装置の主電極領域に対するオーミック電極を形成するためのコンタクトホールを形成する際に、フィールド絶縁膜に対するオーバーエッチングのエッチング時間の制御により、窓部近傍のマスク材の下部に形成されるアンダーカット部の深さが制御出来るので、寸法制御が容易である。また、このアンダーカット部の深さにより、オーミック電極を形成するための第１の導体膜の素片とフィールド絶縁膜との一定の間隙を自己整合的に決定出来るので、オーミック電極とフィールド絶縁膜との一定の間隙を制御するためのフォトリソグラフィ工程は不要である。このため、オーミック電極となる第１の導体膜の素片とフィールド絶縁膜の開口部側壁との間隔を十分に小さく出来、占有面積の小さく、微細寸法を有したオーミック電極を配置出来る。更に、フォトリソグラフィ工程が省略出来るため、半導体装置の主電極領域に対するオーミック電極形成に係わる工程数が減少し、半導体装置の製造歩留まりが高くなる。更に、請求項１７記載の発明は、標準的なＳｉ半導体デバイス製造方法が適用可能なので、容易且つ信頼性が高い。更に、第１の導体膜の素片が、フィールド絶縁膜と反応することが防止出来るので、第１の導体膜の素片を構成する金属材料との接触面にあるフィールド絶縁膜が高温熱処理で還元（浸食）されることがなく、フィールド絶縁膜の絶縁性が維持出来る。また、オーミック電極を構成する金属材料がフィールド絶縁膜に接していないので、第１の導体膜の素片から生成されたオーミック電極とフィールド絶縁膜の接着力が弱いという問題は、本来的に存在しない。このため、プロセス終了後にオーミック電極が剥落することはなく、製造歩留まりが高くなる。更に、オーミック電極の加熱反応層を生成する工程において、オーミック電極の底部外縁部における金属－ＳｉＣ－SiO_2の３元系の共存する状態が存在しないので、３元系の反応による寄生のショットキー接合の生成も回避出来、低いコンタクト抵抗が達成出来る。また、寄生のショットキー接合の生成に伴う主電極領域の水平方向の電流の流れの阻害もない良好な特性の半導体装置が簡単に製造出来る。また、請求項１７記載態に係るオーミック電極構造体の製造方法は、いわゆる「リフトオフ法」を用いてパターニングしているので、どのような種類の第１の導体膜でもパターニング出来る特徴を有する。

【００７５】請求項１８記載の発明によれば、ＳｉＣ基板表面にフィールド絶縁膜を形成する工程は、ＳｉＣ表面を薄く熱酸化させた後、熱酸化膜の上部に、熱酸化以

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外の方法で厚い絶縁膜を堆積することによって達成しているので、ＳｉＣの表面モホロジーを、過度な熱酸化により荒らすことない。また、熱酸化以外の方法は、ＣＶＤ法やスパッタリング法等の周知の物理的或いは化学的手段が採用可能であるが、これらの、熱酸化以外の方法に固有な自然酸化膜やハイドロ・カーボンのＳｉＣ界面（表面）への生成を、熱酸化により効果的に除去、若しくは抑制出来る。つまり、加熱反応層の形成の障害となるＳｉＣ表面の自然酸化膜とハイドロカーボンを除去することが可能であるので、$10^{-7}\Omega cm^2$台程度の低いコンタクト抵抗のオーミック電極を有した半導体装置が簡単に実現出来る。

【００７６】請求項１９記載の発明によれば、界面準位の少ない熱酸化膜の上部に、ゲート電極を形成しているので、ゲート閾値制御が容易で、高速・高耐圧の半導体装置を簡単に製造可能である。

【００７７】請求項２０記載の発明によれば、オーミック電極の加熱反応層を形成する前の第１の導体膜の素片の厚みが制御されているので、仮に第１の導体膜の素片が完全に加熱反応層に転化したとしても、主電極領域が消失したり、加熱反応層が主電極領域を突き抜けることが確実に防止出来る。従って、主電極領域の消失に伴うコンタクト抵抗の急増や、主電極領域の突き抜けに伴うリーク電流の増大を有効に防止出来る。更に、オーミック電極の加熱反応層形成のためのＳｉＣ基板の熱処理工程のプロセス・マージンが十分に取れ、十分な熱処理が可能で、非常に低いコンタクト抵抗のオーミック電極を有した半導体装置が実現出来る。

【００７８】

【発明の実施の形態】次に、図面を参照して、本発明の第１乃至第３の実施の形態を説明する。以下の図面の記載において、同一又は類似の部分には同一又は類似の符号を付している。但し、図面は模式的なものであり、厚みと平面寸法との関係、各層の厚みの比率等は現実のものとは異なることに留意すべきである。従って、具体的な厚みや寸法は以下の説明を参酌して判断すべきものである。また図面相互間においても互いの寸法の関係や比率が異なる部分が含まれていることは勿論である。

【００７９】（第１の実施形態）図１に示すように、本発明の第１の実施の形態に係るオーミック電極構造体は、ＳｉＣ基板１、ＳｉＣ基板１の表面に選択的に形成されたｎ型ＳｉＣ領域３２、ＳｉＣ基板１の上に載置されたフィールド絶縁膜５、フィールド絶縁膜５中にｎ型ＳｉＣ領域３２の表面を露出するように開口された開口部（コンタクト・ウィンドウ）の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７を隔てて配置された電極膜７、フィールド絶縁膜５の開口部の内部において、フィールド絶縁膜５から側壁ギャップ７７を隔て、且つ電極膜７とｎ型ＳｉＣ領域３２の間に配置された加熱反応層８、フィールド絶縁膜５の開口部の内部において、電極膜７の表面に接し、且つフィールド絶縁膜５の上部にまで伸延された配線導体素片９とから構成されている。電極膜７とｎ型ＳｉＣ領域３２との間に埋設されている加熱反応層８は、ｎ型ＳｉＣ領域３２と電極膜７の母材である第１の導体膜との加熱反応によって形成された層である。側壁ギャップ７７を構成している一定の間隙は、フィールド絶縁膜５の厚みより小さい値に制御されている。

【００８０】ｎ型ＳｉＣ領域３２は、高い表面電子密度を有する。例えば、ｎ型ＳｉＣ領域３２の表面電子密度は少なくとも$1\times10^{18}/cm^3$～$2\times10^{21}/cm^3$、好ましくは$1\times10^{19}/cm^3$～$8\times10^{20}/cm^3$である。ＳｉＣ基板１の導電型は本オーミック電極構造体を利用する半導体装置によって異なる。例えば、ＭＯＳＦＥＴならｐ型、ＭＥＳＦＥＴやショットキーバリヤダイオードならｎ型等のように設計仕様に応じて選べばよい。

【００８１】電極膜７の母材である第１の導体膜はＮｉのほかチタン（Ｔｉ）、クロム（Ｃｒ）、タンタル（Ｔａ）、タングステン（Ｗ）、モリブデン（Ｍｏ）などの１、又は１以上の金属から選ばれた、金属膜、合金膜、化合物膜、或いはこれらの複合膜や積層膜から構成されている。この電極膜７の厚みはｎ型ＳｉＣ領域３２の拡散深さの概ね１／２未満の値であることが望ましい。

【００８２】電極膜７には、他の部位のオーミック電極と結線するための第２の導体膜からなる配線導体素片９が接続されている。配線導体素片９は、フィールド絶縁膜５の開口部を被覆するように配置される。配線導体素片９は図１に示すオーミック・コンタクトを他の部位と結線する配線部材であり、半導体装置の主電極配線として機能する。パワーデバイスにおいては、複数のユニットセルを多数ＳｉＣ基板１の上に、蜂の巣状や、マトリクス状等にして配置し電流容量を確保している。また、オン電圧を低くするための設計仕様により、各主電極領域を細分化し、ＳｉＣ基板１の上に高密度に配列する場合もある。従って、このような場合は、複数に分割されたユニットセルの各主電極領域を統合する配線として配線導体素片９が機能する。この配線導体素片９には、周知のアルミニウム（Ａｌ）、アルミニウム・シリコン（Ａｌ－Ｓｉ）共晶、アルミニウム・銅・シリコン（Ａｌ－Ｃｕ－Ｓｉ）共晶、銅（Ｃｕ）、チタン・タングステン（Ｔｉ－Ｗ）合金などが用いられる。

【００８３】フィールド絶縁膜５は、ＳｉＣ基板１の熱酸化膜３と、この熱酸化膜３とは組成若しくは密度の異なる絶縁膜からなる上部絶縁膜４との積層絶縁膜から構成されている。第１の実施の形態に係るオーミック電極構造体において、「熱酸化膜３とは組成の異なる絶縁膜」とは、ＰＳＧ（りん珪酸ガラス）膜、ＢＳＧ（硼珪酸ガラス）、ＢＰＳＧ（硼りん珪酸ガラス）或いはSi_3N_4膜等の絶縁膜の意である。また、「熱酸化膜３とは

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密度の異なる絶縁膜」とは、熱酸化膜以外の方法で堆積したＳｉO_2膜等の絶縁膜の意である。例えば、ＣＶＤ法、スパッタリング法、真空蒸着法等の、化学的若しくは物理的堆積方法によるＳｉO_2膜が該当する。図１に示すＳｉＣの熱酸化膜３は、Ｓｉ熱酸化膜よりは劣るが、Ｓｉ熱酸化膜に近いＳｉO_2膜である。熱酸化膜とその他の方法で堆積したＳｉO_2膜とでは密度が違うので断面を高分解能ＳＥＭ観察すると境界が見える。

【００８４】そして、Ｓｉ熱酸化膜に近いＳｉＣの熱酸化膜３の絶縁破壊電界強度は、厚さ１０ｎｍで１４ＭＶ／ｃｍ程度である。一方、熱酸化以外の方法で形成したＳｉO_2膜の絶縁破壊電界強度は、この値よりも小さい。例えば、ＣＶＤで堆積したＳｉO_2膜の絶縁破壊電界強度は、同じ厚さ１０ｎｍで６ＭＶ／ｃｍ程度であるので、絶縁破壊電界強度を測定すれば、明瞭にＳｉＣの熱酸化膜３と上部絶縁膜４とは識別可能である。

【００８５】また、ＳｉＣの熱酸化膜３は、Ｓｉ熱酸化膜に近いＳｉO_2膜であるので、ＢＨＦ溶液に対するエッチング速度は１００ｎｍ／分程度である。これに比し、ＣＶＤで堆積したＳｉO_2膜に対するエッチング速度は１．５倍から３倍位高い。従って、ＢＨＦ溶液に対するエッチング速度を測定すれば、明瞭にＳｉＣの熱酸化膜３と上部絶縁膜４とは識別可能である。

【００８６】ミクロには、ＣＶＤで堆積したＳｉO_2膜中には、ＳｉＣの熱酸化膜３より水素やカーボン結合が多く、Ｓｉ－Ｏ－Ｓｉ結合距離がＳｉＣの熱酸化膜３より長いので、赤外線吸収スペクトルやラマン分光によっても、明瞭にＳｉＣの熱酸化膜３と上部絶縁膜４とは識別可能である。

【００８７】図１に示すようなＳｉＣの熱酸化膜以外の種々のＳｉO_2膜等の上部絶縁膜４を、ＳｉＣの熱酸化膜３の上部に形成した積層構造を採用すれば、半導体装置の仕様として要求される界面準位、耐圧や表面の安定性を確保しつつ、ＳｉＣの表面モホロジーを良好に維持出来る。

【００８８】熱酸化膜３の厚さは２～５０ｎｍであることが望ましい。特に、５～２０ｎｍの範囲の熱酸化膜３の厚さが望ましい。熱酸化膜３の厚さが、５ｎｍより薄い場合は表面研磨やイオン注入法で生じたＳｉＣ基板１表面の損傷領域を除去する効果ならびに表面の異物を除去する効果が乏しくなる。一方、熱酸化膜３の厚さが、５０ｎｍより厚い場合は過度な熱酸化によりＳｉＣ基板１表面が次第に荒れ、表面モホロジーが低下するという問題がある。このため、コンタクト抵抗ρcの低減には上記範囲の熱酸化膜３の厚さが有益な効果をもたらす。

【００８９】熱酸化膜３の厚さと上部絶縁膜４の厚さとを合計したフィールド絶縁膜５の総厚は、１００ｎｍ～３μｍであることが望ましい。特に、３００ｎｍ以上であることが望ましい。また、高耐圧の電力用半導体装置であれば、８００ｎｍ以上にすれば良い。但し、フィールド絶縁膜５があまり厚くなると、クラック等が発生するので、３μｍ以上は好ましくない。また、電極膜７及び加熱反応層８の周縁部と開口部側壁との間の間隙（側壁ギャップ）７７は、フィールド絶縁膜５の厚み程度に制御できるので、微細寸法化には、フィールド絶縁膜５があまり厚いのは好ましくない。即ち、微細寸法化を考慮した場合には、１．５μｍ程度が、フィールド絶縁膜５の厚さの実用的な上限である。

【００９０】図１に示すように、第１の実施の形態に係るオーミック電極構造体によれば、電極膜７及び加熱反応層８が共に、フィールド絶縁膜５の開口部の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７を隔て配置されているので、電極膜７及び加熱反応層８を構成する金属材料が、フィールド絶縁膜５と反応することが防止出来る。従って、金属材料との接触面にあるフィールド絶縁膜５が高温熱処理で還元（浸食）されることがないので、フィールド絶縁膜５の絶縁性が維持出来る。また、電極膜７を構成する金属材料がフィールド絶縁膜５に接していないので、電極膜７とフィールド絶縁膜５の接着力が弱いという問題は、本来的に存在しない。このため、製造プロセス終了後に電極膜７が剥落することはなく、製造歩留まりが高くなる。更に、加熱反応層８の底部外縁部における金属－ＳｉＣ－ＳｉO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来るので、低いコンタクト抵抗が達成出来る。また、寄生のショットキー接合の生成に伴うｎ型ＳｉＣ領域３２の水平方向の電流の流れの阻害もない。

【００９１】更に、第１の実施の形態に係るオーミック電極構造体によれば、電極膜７及び加熱反応層８の周縁部と開口部側壁との間の間隙（側壁ギャップ）７７を、フィールド絶縁膜５の厚みより小さい微細寸法に出来るので、オーミック電極構造体の占有面積を小さく出来る。

【００９２】次に、図２～図４に示す工程断面図（その１～その３）を参照しながら本発明の第１の実施の形態に係るオーミック電極構造体の製造工程を説明する。

【００９３】（イ）先ず、厚さ約１．５μｍのＳｉO_2膜３３を、ＣＶＤ法で４Ｈ－ＳｉＣ基板１の表面全面に堆積し、その上にフォトレジスト３４をスピンコートする。そして、図２（ａ）に示すように、ｎ型ＳｉＣ領域形成予定領域の上に堆積したＳｉO_2膜３３を周知のフォトリソグラフィ法とウェット・エッチング技術で選択的に除去し、イオン注入マスク膜３３を形成する。

【００９４】（ロ）そして、図２（ｂ）に示すように、イオン注入マスク膜３３の上に、再びＣＶＤ法で薄いＳｉO_2膜からなるイオン注入スルー膜３５を全面に堆積する。イオン注入スルー膜３５は、後述のイオン注入時の射影飛程（深さ）R_pを調節するための膜である。後述の$^{31}P^+$（りんイオン）の注入条件では、イオン注入

スルー膜３５の厚みは２０～２５ｎｍである。イオン注入スルー膜３５を堆積した後、ＳｉＣ基板１全面に$^{31}P^{+}$，$^{14}N^{+}$（窒素イオン）や$^{75}As^{+}$（ヒ素イオン）などのｎ型不純物イオンを、少なくともＳｉＣ基板１の表面の不純物密度が$1\times10^{20}/cm^{3}$以上になり、且つ、ＳｉＣ基板１の結晶性を損なわないようにイオン注入する。このｎ型不純物イオンの注入は、５００℃に加熱したＳｉＣ基板１に、ドーズ量Φ／加速エネルギーE_{AC}を変えながら多段に注入することが好ましい。例えば、$^{31}P^{+}$を、ＳｉＣ基板１に多段イオン注入する場合のドーズ量Φ／加速エネルギーE_{AC}条件は、以下の通りである：

第１イオン注入$\Phi=5\times10^{14}cm^{-2}/E_{AC}=40KeV$；

第２イオン注入$\Phi=5\times10^{14}cm^{-2}/E_{AC}=70KeV$；

第３イオン注入$\Phi=1\times10^{15}cm^{-2}/E_{AC}=100KeV$；

第４イオン注入$\Phi=1\times10^{15}cm^{-2}/E_{AC}=150KeV$；

第５イオン注入$\Phi=2\times10^{15}cm^{-2}/E_{AC}=200KeV$；

第６イオン注入$\Phi=2\times10^{15}cm^{-2}/E_{AC}=250KeV$。

【００９５】（ハ）６段の多段イオン注入が終了したところで、イオン注入マスク膜３３とイオン注入スルー膜３５をフッ酸（ＨＦ）で全面除去する。そして、常圧Ａｒ雰囲気で１７００℃１分の急速加熱処理を行うと、イオン注入された$^{31}P^{+}$が活性化されて、図２（ｃ）に示すように、高不純物密度を有するｎ型ＳｉＣ領域３２が選択的に形成される。上記イオン注入条件と活性化熱処理条件で生成されるｎ型ＳｉＣ領域３２の拡散深さはおよそ３５０ｎｍである。

【００９６】（ニ）そして、シリコン（Ｓｉ）プロセスで周知のＲＣＡ洗浄法等の所定の洗浄法を用いて、ＳｉＣ基板１を十分清浄化する。ＲＣＡ洗浄法は、$H_2O_2+NH_4OH$混合液（ＳＣ－１）とH_2O_2＋ＨＣｌ混合液（ＳＣ－２）による浸漬処理を組み合わせ行う伝統的な半導体ＳｉＣ基板１の洗浄法である。そして、図３（ｄ）に示すように、十分清浄化されたＳｉＣ基板１の表面を、１０００℃から１１５０℃において乾燥酸素雰囲気で熱酸化し、表面に厚さ５～４０ｎｍ熱酸化膜３を成長する。なお、乾燥酸素雰囲気の代わりに、水蒸気を用いてもかまわない。乾燥酸素中、熱処理温度１１５０℃で３時間熱酸化すれば、３５～４０ｎｍの熱酸化膜３が得られる。水蒸気を用いたウェット雰囲気中、１１５０℃で２時間熱酸化すれば、３０～３５ｎｍの熱酸化膜３が得られる。水蒸気を用いたウェット雰囲気の熱酸化の場合は、その後アルゴン（Ａｒ）中で１１５０℃、３０分程度アニールすることが好ましい。熱酸化膜３を２０ｎｍ以下にするためには、酸化温度を下げる若しくは、酸化時間を短縮すれば良い。

【００９７】（ホ）次に、図３（ｅ）に示すように、熱酸化膜３の上に、常圧ＣＶＤ法で４００ｎｍのＰＳＧからなる上部絶縁膜４を堆積し、２層構造からなるフィールド絶縁膜５を形成する。熱酸化膜３の厚さと上部絶縁膜４の厚さとを合計したフィールド絶縁膜５の総厚を、１００ｎｍ～６００ｎｍ程度にすることが望ましい。

【００９８】（ヘ）次に、フィールド酸絶縁膜５の表面に、本発明の「マスク材」として、厚さ１～２μｍのフォトレジスト２２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、マスク材（フォトレジスト）２２を選択的に露光し、現像することによって開口部６に対応する部分のフォトレジスト２２を除去し窓部を形成する。続いて、このフォトレジスト２２のマスクパターンをエッチングマスクとして用い、ＳｉＣ基板１をＢＨＦ溶液に浸漬しウェット・エッチングすることで、図３（ｆ）に示すように、フィールド絶縁膜５に開口部６を形成する。微細な開口部６を形成する時は、ガスプラズマを用いたドライ・エッチングが好ましい。例えば、CHF_3やC_2F_6などをエッチャントとした反応性イオンエッチング（ＲＩＥ）法や電子サイクロトロン共鳴イオンエッチング（ＥＣＲイオンエッチング）等の種々のドライ・エッチングを使用することが出来る。この場合、最初にドライ・エッチングを行い、フィールド絶縁膜５を数１０ｎｍ残したところで、ウェット・エッチングに切り換えるようにする。開口部６をドライ・エッチングで、最後まで貫通させると、

１）ＳｉＣ基板１の表面が過剰なプラズマエネルギによるプラズマ損傷で荒れる、

２）エッチング反応で生成した反応生成物であるハイドロ・カーボンがＳｉＣ基板１の表面に再付着し、表面を汚染する

という弊害が起こり、後述の加熱反応層の均一生成に大きな障害になる。更に、コンタクト抵抗ρcを劇的に増加させる結果となるので好ましくない。ウェットエッチング単独で開口する場合でも、ドライエッチングとウェットエッチングの組み合わせで開口する場合でも、両者に共通し、本発明の根幹に係わる極めて重要な形成上のポイントはウェット・エッチング又はドライ・エッチングをやや過剰に行い（オーバーエッチングを行い）、フィールド絶縁膜５の開口部６がフォトレジストの開口部より大きくなり、アンダーカット部が生じるようにするということである。例えば、エッチングモニタ部の目視により（色の変化により）、ｎ型ＳｉＣ領域３２の表面の露出が確認された後、更に所定の時間オーバーエッチングを追加すればよい。オーバーエッチング量の制御は、エッチング液の組成、液温を厳密に制御し、エッチング時間をコントロールすればよい。このようなコント

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ロールを行うことにより、アンダーカット部の深さは、フィールド絶縁膜５の厚み（１００ｎｍ～６００ｎｍ）程度であれば、容易に制御可能である。或いは、所望のエッチング厚のエッチングモニタを別途用意し、このエッチングモニタのジャスト・エッチを確認してエッチングを終了するようにすれば、１００ｎｍ以下の制御も可能である。エッチング液に界面活性剤等を加えても良い。更に、精密なアンダーカット部の深さを制御するためには、気相反応を利用したエッチング（ガスエッチング）を用いても良い。第１の実施形態では、本発明の「マスク材」としてフォトレジスト２２を用いているが、このオーバーエッチング時に、エッチングされない材料であれば、フォトレジスト２２以外の材料を本発明の「マスク材」として採用可能である。即ち、本発明の「マスク材」は、フィールド絶縁膜５とはエッチング速度の異なる材料で構成されているれば良い。なお、図３（ｆ）には、熱酸化膜３と上部絶縁膜４のエッチング速度の差による側壁部の段差を誇張して示しているが、アンダーカット部の深さが薄い限り、現実にはエッチング深さの差は顕著ではない。

【００９９】（ト）その後、エッチングマスクとしてのフォトレジスト２２を残存した状態で、ＢＨＦ溶液を超純水で完全に濯ぎ落とした（リンスした）後、乾燥する。そして、レジストマスク２２が被着した状態のＳｉＣ基板１を、真空蒸着装置のチャンバー中に速やかに据え付け、直ちに真空排気する。コンタクト・ウィンドウ開口エッチングから真空排気までの大気中放置時間は、コンタクト抵抗ρcの大小をする極めて重要な因子である。大気中放置時間が長いと、開口部のＳｉＣ基板１の表面に自然酸化膜が生成されたり、望まぬ異物が付着する。このため、後述の加熱反応層の均一生成に大きな障害となり、ひいてはコンタクト抵抗ρcを劇的に増加させるので、５分以内の短時間で行う。そして、真空蒸着装置のチャンバーをターボ分子ポンプ、クライオポンプ等で、1.3×10^{-5} Ｐａ未満の圧力まで真空排気し、図４（ｇ）に示すように、ＳｉＣ基板１の表面に第１の導体膜としての第１の導体膜１７を蒸着する。第１の導体膜１７としては、例えば、Ｎｉ膜を電子ビーム（ＥＢ）蒸着すれば良い。図４（ｇ）に示すように、開口部の側壁に第１の導体膜（Ｎｉ系電極膜）１７が付着しないようにするためには、オリフィス等を用いて、蒸着ビームの指向性を向上させて行えば良い。この時、上述のように、フィールド絶縁膜５の開口部６はフォトレジスト・マスクの開口部より大きくなるように形成されているため、開口部底部に蒸着される第１の導体膜の素片（以下において「第１の導体素片２７」という。）はこの若干小さいフォトレジスト・マスクの開口部の形状に正確に転写される。こうして、第１の導体素片２７の周縁部とフィールド絶縁膜５の開口部側壁との間には、距離が一定で、且つ微細寸法の蒸着制限領域が形成される。この微細な蒸着制限領域は、上述したアンダーカット部の深さで決定されるので、開口エッチングのオーバーエッチング時間で精密にコントロール出来る。第１の導体膜１７の厚みはその下部にあるｎ型ＳｉＣ領域３２の拡散深さの１／２より薄く設定する。

【０１００】（チ）第１の導体膜（Ｎｉ膜）１７の真空蒸着後、ＳｉＣ基板１を真空蒸着装置のチャンバーから取り出す。続いて、リフトオフ法を用いて、図４（ｈ）に示すように、開口部の内部のみに第１の導体素片２７が選択的に埋設された基板構造を得る。即ち、ＳｉＣ基板１をアセトンなどの有機溶剤或いは専用のフォトレジスト剥離液に浸漬させ、ＳｉＣ基板１表面に残されているフォトレジスト２２を完全に除去すると、フォトレジスト２２の上に被着した第１の導体膜（Ｎｉ膜）１７もフォトレジスト２２と共に除かれるので、図４（ｈ）に示すように、開口部の内部のみに第１の導体素片２７が選択的に残存する。この結果、第１の導体素片２７の周縁部とフィールド絶縁膜５の開口部側壁との間には、蒸着制限領域に対応した微細寸法の側壁ギャップ７７が自己整合的に形成される。

【０１０１】（リ）しかる後、ＳｉＣ基板１を７００℃～１０５０℃の非酸化性雰囲気で短時間（数分程度）の熱処理を施すと、図４（ｉ）に示すように、第１の導体素片２７とＳｉＣ基板１が相互に反応して、両者の界面領域に加熱反応層８が生成され、加熱反応層とｎ型ＳｉＣ領域３２との間で優れたオーミック特性が実現される。数分程度の短時間の熱処理を行うためには、赤外線（ＩＲ）ランプ加熱を用いれば良い。ここで「非酸化性雰囲気」とは酸素（O_2）や水（H_2O）等の酸素を含む化合物の気体を含まない雰囲気のことである。具体的には、超高純度アルゴン（Ａｒ）や超高純度窒素（N_2）などの超高純度不活性ガス雰囲気、或いは、高真空等が、「非酸化性雰囲気」として好適である。これら熱処理雰囲気に酸素が僅かでも含まれると、熱処理で表面に金属の酸化物（＝絶縁物）が生じたり、加熱反応層の形成が阻害されたりするので、酸素及び水の分圧の制御に関しては、厳重なる管理が必要である。具体的には、熱処理雰囲気に含まれる酸素及び水の分圧は少なくとも、1×10^{-3} Ｐａ～1×10^{-10} Ｐａ程度、望ましくは、$1.\times10^{-5}$ Ｐａ～1×10^{-10} Ｐａ程度であることが望ましい。超高純度不活性ガス雰囲気中で熱処理する場合は、ガス配管のベーキングやリークの点検の他に、脱酸素装置やガス純化装置の採用等の厳重なる管理が必要である。また、高真空中で熱処理する場合は、厳密には1×10^{-8} Ｐａ程度の真空中でも金属の表面が酸化するので、クライオパネル等を併用して、酸素及び水の分圧を1×10^{-8} Ｐａ～1×10^{-10} Ｐａ程度に制御して、超高真空下で熱処理をすることが好ましい。例えば、第１の導体膜１７としてＮｉ膜を用いた場合は、熱処理により、ニッケルシリサイド（ＮｉＳ

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i_{1-X}，ＮｉＳｉ$_2$）とカーボン（Ｃ）等からなる加熱反応層８が、第１の導体素片２７の底部（下部）に生成される。加熱反応層８にならなかった上部の未反応の第１の導体素片２７は電極膜７になる。現実には、電極膜７は、未反応のＮｉにニッケルシリサイド（Ｎｉ$_2$Ｓｉ）が拡散した状態になる。第１の導体膜を蒸着する工程で第１の導体膜の厚みをその下部にあるｎ型ＳｉＣ領域３２の厚みの１／２より薄く設定したのは、第１の導体素片２７が加熱処理で完全に加熱反応層８に転化した場合であっても、ｎ型ＳｉＣ領域３２が下部に残されるよう保証するためである。高不純物密度ｎ型ＳｉＣ領域３２が完全に消失すると、コンタクト抵抗が急増する深刻な事態となる。第１の導体膜の厚みの条件はこの事態を回避するために規定されている。

【０１０２】（ヌ）加熱反応層８の形成後に、図１に示すように、ＳｉＣ基板１全面にＡｌ等の第２の導体膜を蒸着する。そして、フォトリソグラフィ法とＲＩＥ等のエッチング技術でパターニングして、図１に示すような配線導体素片９を形成すれば、第１の実施の形態に係るオーミック電極構造体が完成する。なお、パターニングの際のエッチャント（＝エッチング液或いはエッチングガス）がＮｉ系電極膜７を侵す時は、第２の導体膜は必ずＮｉ系電極膜７を覆うように配設する構成とすれば良い。

【０１０３】なお、熱反応層９を形成する工程で第１の導体膜からなる電極膜７の表面に意図せず第１の導体膜の酸化物が形成されたり、例えば、ハイドロ・カーボン等の高抵抗性の汚染物が付着する場合には、第２の導体膜を成膜する前に、これら、異物を除去する工程が付加される。この目的に適合した基板処理として、ドライ処理ならＡｒイオンによるスパッタエッチが有効である。或いは、酸素プラズマへの暴露によるハイドロ・カーボンの除去工程の後に、燐酸（H_3PO_4）：硝酸（HNO_3）：酢酸（CH_3COOH）混合溶液への浸漬により、第１の導体膜等の酸化膜除去し、純水リンスし、乾燥するという一連のウェット処理工程を用いることが出来る。

【０１０４】第１の実施の形態に係るオーミック電極構造体の製造方法によれば、フィールド絶縁膜５に対するオーバーエッチングのエッチング時間の制御により、窓部近傍のマスク材の下部に形成されるアンダーカット部の深さが制御出来るので、寸法制御が容易である。また、このアンダーカット部の深さにより、第１の導体素片２７とフィールド絶縁膜５との一定の間隙（側壁ギャップ）７７を自己整合的に決定出来る。つまり、第１の導体素片２７の電極パターンがフィールド絶縁膜５に設けられた開口パターンの側壁の位置に対して、自己整合的に形成出来るという利点がある。言いかえると、フォトリソグラフィ工程で第１の導体素片２７パターニングするのではないので、フィールド絶縁膜５の端部に対して、極限の精度で、第１の導体素片２７の端部の位置を合わせられる利点がある。「極限の精度」とは、オーバーエッチングの方法を選べば、ナノメータ・レベル、更には分子層単位の精度でアンダーカットの深さが制御可能と言う意味である。例えば、超高真空に排気可能な真空チャンバー中で、表面反応を利用した気相エッチング等の採用をすれば、分子層単位のエッチングが可能である。従って、電極膜７となる第１の導体素片２７とフィールド絶縁膜５の開口部側壁との間隔を十分に小さく出来、占有面積の小さく、微細寸法を有したオーミック電極構造体を製造出来る。

【０１０５】第１の実施の形態に係るオーミック電極構造体の製造方法によれば、第１の導体素片２７とフィールド絶縁膜５との一定の間隙（側壁ギャップ）７７を制御するためのフォトリソグラフィ工程は不要である。つまり、フィールド絶縁膜５の開口部６形成工程から第１の導体素片２７の形成に至る一連の工程において、フォトリソグラフィが１回で済み、プロセスが簡素化される利点がある。工程数が減少すれば、製造歩留まりが高くなり、従来例に対し製造原価の低減として有効に作用する。更に、標準的なＳｉ半導体デバイス製造方法が適用可能なので、容易且つ信頼性が高いオーミック電極構造体の製造方法が提供出来る。

【０１０６】また、第１の実施の形態に係るオーミック電極構造体の製造方法によれば、どのような種類、構造の第１の導体膜１７でもパターニングすることが可能である。この利点が特に活かされるのは、

ａ）第１の導体膜１７に実用的なエッチング速度のエッチャントが存在しないとき、

ｂ）酸素や水分、或いは、エッチャントに第１の導体膜１７が著しく反応するとき、

ｃ）第１の導体膜１７が多層構造になっていてエッチングが煩雑になるとき、である。

【０１０７】更に、第１の実施の形態に係るオーミック電極構造体の製造方法によれば、第１の導体素片２７が、フィールド絶縁膜５と反応することが防止出来るので、第１の導体素片２７を構成する金属材料との接触面にあるフィールド絶縁膜５が高温熱処理で還元（浸食）されることがなく、フィールド絶縁膜５の絶縁性が維持出来る。また、第１の導体素片２７を構成する金属材料がフィールド絶縁膜５に接していないので、第１の導体素片２７から生成された電極膜７とフィールド絶縁膜５の接着力が弱いという問題は、本来的に存在しない。このため、プロセス終了後に電極膜７が剥落することはなく、製造歩留まりが高くなる。更に、加熱反応層８を生成する工程において、第１の導体素片２７の底部外縁部における金属－ＳｉＣ－SiO_2の３元系の共存する状態が存在しないので、３元系の反応による寄生のショットキー接合の生成も回避出来、低いコンタクト抵抗が達成出来る。また、寄生のショットキー接合の生成に伴う

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n型ＳｉＣ領域３２の水平方向の電流の流れの阻害もない。

【０１０８】このような構成で作製したn型ＳｉＣ領域３２に対するオーミック電極構造体が実用的コンタクト抵抗を示すか確かめるために、コンタクト抵抗の評価にしばしば用いられる線型伝送線路モデル（リニアＴＬＭ）評価法のコンタクト群を作製した。このリニアＴＬＭ評価法においては、SiO_2膜からなる素子分離領域に囲まれた長方形のn型ＳｉＣ領域の内部に、電極パターン（コンタクト・パターン）を横一列に並べたコンタクト群を用いる。n型ＳｉＣ領域の短辺の長さは、２０８μmである。即ち、長方形のn型ＳｉＣ領域の長辺方向に沿って、この長方形とは長辺方向が直交する小さな長方形からなる複数の電極パターンを１次元配列したコンタクト群のパターンを用意する。この小さな長方形の長辺の長さ（オーミック・コンタクト幅）は２００μmで、短辺の長さは、１００μmである。ここで、コンタクト群のパターンは、小さな長方形パターンからなるコンタクト（金属・半導体接合）の相互の間隔（コンタクト間隔）を順に変化させながら、n型ＳｉＣ領域の長辺方向に沿って横一列に配列される。即ち、コンタクト間隔Ｌは$L=6, 10, 15, 20, 25, 30\mu m$と順に変化させる。リニアＴＬＭ評価法とは、このコンタクト群における隣接する２つのコンタクト間の電流－電圧特性から抵抗を求め、抵抗をコンタクト間隔の関数として整理し、これを直線近似して数式処理を行い、最終的に精密なコンタクト抵抗ρcを求める方法である。

【０１０９】評価した試料の主な構成は次の通りである。使用したＳｉＣ基板１は高抵抗のｐ型ホモエピタキシャル膜を有する（０００１）面の４Ｈ－ＳｉＣ基板である。このホモエピタキシャル４Ｈ－ＳｉＣ基板の表面は、Ｓｉ面である。このホモエピタキシャル４Ｈ－ＳｉＣ基板に、高不純物密度のn型ＳｉＣ領域３２が、上述した方法で、イオン注入され、活性化熱処理され形成されたものである。n型ＳｉＣ領域３の拡散深さは３５０ｎｍで、不純物密度は$2.7\times10^{20}\ cm^{3}$である。熱処理前の第１の導体膜１７は１５０ｎｍ厚のＮｉで、フィールド絶縁膜５の熱酸化膜３は１１００℃ドライ酸化膜（１０ｎｍ厚）、上部絶縁膜４は常圧ＣＶＤで成膜したSiO_2膜（４００ｎｍ厚）である。加熱反応層８の熱処理温度は１０００℃、熱処理時間は５分、熱処理雰囲気は高純度Ａｒ雰囲気である。第２の導体膜からなる配線導体素片９は厚さ１μmのＡｌ膜素片である。

【０１１０】図５はコンタクト間隔をパラメータにして、隣接する電極間の電流－電圧特性を示している。原点を通る直線が得られていることから、ＴＬＭを構成するすべての電極でオーミック・コンタクトが得られていることが分かる。図５の直線の傾きから求めたオーミック・コンタクト電極間の抵抗と距離の関係をプロットすると図６のようになる。データはバラツキが少なく、１直線上にプロットされている。この直線近似から、コンタクト抵抗$\rho c=8.6\times10^{-7}\ \Omega cm^{2}$と非常に優れた値が得られる。図５には、比較のため、加熱反応層８を、熱処理温度は９００℃とし、他の条件を熱処理温度１０００℃の場合と同じにした結果も示すが、コンタクト抵抗$\rho c=4.0\times10^{-6}\ \Omega cm^{2}$であり、加熱反応層８の生成が、熱処理温度１０００℃の場合に比し、少し不十分であると考えられる。

【０１１１】なお、４Ｈ－ＳｉＣ基板１ではなく、禁制帯幅が相対的に狭く、電子親和力の小さな６Ｈ－ＳｉＣ基板１（Ｓｉ面）を用いて同様の評価を行った場合には$\rho c=4.3\times10^{-7}\ \Omega cm^{2}$の更に小さなコンタクト抵抗が実現される。

【０１１２】他の条件を同じにして、第１の導体膜として、Ｎｉの替わりに厚み１００ｎｍのチタン（Ｔｉ）を用いた場合には$\rho c=1.2\times10^{-6}\ \Omega cm^{2}$のコンタクト抵抗が得られる。第１の導体膜として、厚み１５０ｎｍのタングステン（Ｗ）を用いた場合には$5.5\times10^{-6}\ \Omega cm^{2}$のコンタクト抵抗が得られる。

【０１１３】図７は、ノマルスキー干渉顕微鏡によるフィールド絶縁膜５中に開口されたコンタクト・ウィンドウ内に埋め込まれた電極膜７の表面モホロジーをスケッチした模式図である。電極膜７の平面寸法は、２０μm×２０μmであり、フィールド絶縁膜５の開口部側壁と電極膜７との間には、自己整合的に形成された微細寸法の側壁ギャップ７７が観察出来る。図７（ａ）は、熱処理なしの場合の、Ｎｉ膜からなる電極膜７の表面の模式図であり、良好な表面モホロジーが観察出来る。一方、図７（ｂ）及び図７（ｃ）は、それぞれ、９００℃及び１０００℃で熱処理した場合の、電極膜７の表面をスケッチした模式図であり、若干の表面状態の変化が認められるものの良好な表面モホロジーであると判断出来る。

【０１１４】図８は、１０００℃で熱処理した本発明の第１の実施形態に係るオーミック電極構造体の断面ＴＥＭ像をスケッチした模式図である。ＴＥＭ観察は、［１１２０］方向に、３００ＫｅＶの加速電圧の電子線を照射して行った。熱処理前のＮｉ／ＳｉＣ界面が熱処理後に、約１７０ｎｍ程度ＳｉＣ基板方向に移動している。加熱反応層８とn型ＳｉＣ領域３２との界面には、界面の平坦性に優れた良好な表面モホロジーが観察出来る。

【０１１５】図９は、$^{4}He^{+}$を加速電圧３ＭｅＶで入射角０°照射した場合の散乱角１５７°におけるラザフォード後方散乱分析により求めた第１の実施形態に係るオーミック電極構造体の厚み方向の組成の変化を示す図である。最上層には、配線導体素片９としてのＡｌ膜が観察出来る。配線導体素片９の下部には、厚さ約１００ｎｍの電極膜７が認められる。電極膜７は、Ｎｉ、ニッケルシリサイド（Ni_2Si）及びカーボン（Ｃ）の固溶体であると推定される。電極膜７の下には、厚さ約３００ｎｍの加熱反応層８が認められる。加熱反応層８

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は、厚さ約１００ｎｍのニッケルシリサイド（$NiSi_{1-x}$）層と、この層の下に連続して位置する厚さ厚さ約２００ｎｍのニッケルシリサイド（$NiSi_2$）とカーボン（Ｃ）の固溶体層から構成されていると推定される。

【０１１６】（第２の実施形態）図１３は、本発明の第２の実施の形態に係るオーミック電極構造体の要部断面図である。本構造はリセス型ゲート構造を有するＭＥＳＦＥＴ、ＭＯＳＦＥＴなどで用いられるメサ形状をした高不純物密度ｎ型ＳｉＣエピタキシャル領域にオーミック電極構造体を形成する例である。

【０１１７】本発明の第２の実施の形態に係るオーミック電極構造体においては、所望のＳｉＣ基板１の表面に、メサ形状の高不純物密度のｎ型ＳｉＣ領域２が形成されている。ｎ型ＳｉＣ領域２の表面電子密度は少なくとも$1\times10^{18}/cm^3$～$2\times10^{21}/cm^3$、好ましくは$1\times10^{19}/cm^3$～$8\times10^{20}/cm^3$である。このような高不純物密度のｎ型ＳｉＣ領域２は、窒素をその場で添加した気相エピタキシャル成長法等によるホモ・エピタキシャル成長で形成しても良いし、第１の実施の形態と同様に、$^{31}P^+$，$^{14}N^+$や$^{75}As^+$などのｎ型不純物イオンの注入と、その後の活性化熱処理で形成しても良い。ＳｉＣ基板１の導電型は、第２の実施の形態に係るオーミック電極構造体を利用する半導体装置によって異なるのでここでは規定しない。図１３において図１と同じ番号を付した部位は、図１と同じ要素であり、冗長を避けるために説明を簡略化或いは省略する。

【０１１８】図１３に示すように、第２の実施の形態に係るオーミック電極構造体によれば、電極膜７及び加熱反応層８が共に、フィールド絶縁膜５の開口部の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７を隔て配置されているので、電極膜７及び加熱反応層８を構成する金属材料が、フィールド絶縁膜５と反応することが防止出来る。従って、金属材料との接触面にあるフィールド絶縁膜５が高温熱処理で還元（浸食）されることがないので、フィールド絶縁膜５の絶縁性が維持出来る。また、電極膜７を構成する金属材料がフィールド絶縁膜５に接していないので、電極膜７とフィールド絶縁膜５の接着力が弱いという問題は、本来的に存在しない。このため、製造プロセス終了後に電極膜７が剥落することはなく、製造歩留まりが高くなる。更に、加熱反応層８の底部外縁部における金属－ＳｉＣ－SiO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来るので、低いコンタクト抵抗が達成出来る。また、寄生のショットキー接合の生成に伴うｎ型ＳｉＣ領域２の水平方向の電流の流れの阻害もない。

【０１１９】更に、第２の実施の形態に係るオーミック電極構造体によれば、電極膜７及び加熱反応層８の周縁部と開口部側壁との間の間隙（側壁ギャップ）７７を、フィールド絶縁膜５の厚みより小さい微細寸法に出来るので、オーミック電極構造体の占有面積を小さく出来る。

【０１２０】次に図１４～図１６に示す工程断面図（その１～その３）を参照しながら、本発明の第２の実施の形態に係るオーミック電極構造体の製造工程を説明する。

【０１２１】（イ）先ず、（０００１）面、８°オフの４Ｈ－ＳｉＣ基板１のＳｉ面表面に、$1\times10^{19}/cm^3$以上の高不純物密度のｎ型不純物としてのＮ（窒素）を添加した厚さ数１００ｎｍのｎ型エピタキシャル成長層（ｎ型ＳｉＣ領域）２０をエピタキシャル成長する。続いて、このｎ型エピタキシャル成長層（ｎ型ＳｉＣ領域）２０の上に、厚さ２０ｎｍのシリコン酸化膜（SiO_2膜）からなるプロテクト酸化膜をＣＶＤ法で堆積する。このプロテクト酸化膜の上に、更に、２００ｎｍ厚のＡｌ膜を蒸着する。このＡｌ膜／SiO_2膜を、周知のフォトリソグラフィ法とＲＩＥ法等のエッチング技術で、図１４（ａ）に示すように、ｎ型ＳｉＣ領域２に対応するＡｌ膜／SiO_2膜からなるエッチングマスク２１を形成する。

【０１２２】（ロ）次に、Ａｌ膜／SiO_2膜からなるエッチングマスク２１を使用し、SF_6とO_2をエッチャントガスとしたＲＩＥ法で、図１４（ｂ）に示すように、不要なエピタキシャル層を除く。更に、その後、エッチングマスク２１の上部のＡｌを硫酸（H_2SO_4）と過酸化水素（H_2O_2）の混合液で取り除き、続いて、その下のプロテクト酸化膜をＢＨＦ溶液で除いて、素子分離されたメサ構造のｎ型ＳｉＣ領域２を形成する。

【０１２３】（ハ）この後は、第１の実施の形態の図３（ｄ）以降の工程と、実質的に同様である。即ち、ＲＣＡ洗浄法等の所定の洗浄法を用いて、ＳｉＣ基板１を十分清浄化する。そして、図１４（ｃ）に示すように、十分清浄化されたＳｉＣ基板１の表面を、１０００℃から１１５０℃において乾燥酸素雰囲気で熱酸化し、表面に厚さ５～４０ｎｍ熱酸化膜３を成長する。次に、図１５（ｄ）に示すように、熱酸化膜３の上に、常圧ＣＶＤ法でSiO_2膜からなる上部絶縁膜４を堆積し、２層構造からなるフィールド絶縁膜５を形成する。熱酸化膜３の厚さと上部絶縁膜４の厚さとを合計したフィールド絶縁膜５の総厚を、１００ｎｍ～６００ｎｍ程度にすることが望ましい。

【０１２４】（ニ）次にフィールド酸絶縁膜５の表面に、本発明のマスク材として、厚さ１～２μｍのフォトレジスト２２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト２２を選択的に露光し、現像することによって開口部６に対応する部分のマスク材（フォトレジスト）２２を除去し、窓部を形成する。続いて、このフォトレジスト２２のマスクパターンをエッチングマスクとして用

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い、ＳｉＣ基板１をＢＨＦ溶液に浸漬し、ウェット・エッチングすることで、図１５（ｅ）に示すように、フィールド絶縁膜５に開口部６を形成する。微細な開口部６を形成する時は、ガスプラズマを用いたドライ・エッチングが好ましい。この場合、最初にドライ・エッチングを行い、フィールド絶縁膜５を数１０ｎｍ残したところで、ウェット・エッチングに切り換えるようにする。第１の実施の形態で説明したように、ウェットエッチング単独で開口する場合でも、ドライエッチングとウェットエッチングの組み合わせで開口する場合でも、ウェット・エッチング又はドライ・エッチングをやや過剰に行い、フィールド絶縁膜５の開口部６がフォトレジストの開口部より大きくなり、アンダーカット部が生じるようにする。第１の実施の形態と同様に、エッチングモニタ部の目視により、ｎ型ＳｉＣ領域２の表面の露出が確認された後、更に所定の時間オーバーエッチングを追加すればよい。第２の実施形態では、本発明の「マスク材」としてフォトレジスト２２を用いているが、このオーバーエッチング時に、エッチングされない材料であれば、フォトレジスト２２以外の材料を本発明の「マスク材」として採用可能であることは勿論である。

【０１２５】（ホ）その後、エッチングマスクとしてのフォトレジスト２２を残存した状態で、ＢＨＦ溶液を超純水で完全に濯ぎ落とした（リンスした）後、乾燥する。そして、レジストマスク２２が被着した状態のＳｉＣ基板１を、真空蒸着装置のチャンバー中に速やかに据え付け、直ちに真空排気する。コンタクト・ウィンドウ開口エッチングから真空排気までの大気中放置時間は、コンタクト抵抗ρｃの大小をする極めて重要な因子であることは、第１の実施の形態で説明した通りである。従って、大気に露出されている時間は、５分以内の出来るだけ短時間にする。そして、真空蒸着装置のチャンバーをターボ分子ポンプ、クライオポンプ等で、１．３×１０$^{-5}$Ｐａ未満の圧力まで真空排気し、図１５（ｆ）に示すように、ＳｉＣ基板１の表面に第１の導体膜１７を蒸着する。第１の導体膜１７としては、例えば、Ｎｉ膜を蒸着すれば良い。図１５（ｆ）に示すように、開口部の側壁に第１の導体膜（Ｎｉ膜）１７が付着しないようにするためには、オリフィス等の指向性制御手段を用いて、蒸着ビームの指向性を向上させて行えば良い。この時、上述のように、フィールド絶縁膜５の開口部６はフォトレジスト・マスクの開口部より大きくなるようにアンダーカット部が形成されているため、開口部底部に蒸着される第１の導体素片２７は、アンダーカット部の形状に正確に転写される。こうして、第１の導体素片２７の周縁部とフィールド絶縁膜５の開口部側壁との間には、距離が一定で、且つ微細寸法の蒸着制限領域（側壁ギャップ）７７が発生する。この微細な側壁ギャップ７７は、開口エッチングのオーバーエッチング時間で精密にコントロール出来る。微細な側壁ギャップ７７はフィールド絶縁膜５の厚み（１００ｎｍ～６００ｎｍ）程度まで狭めて形成出来る。第１の導体膜１７の厚みは、その下部にあるｎ型ＳｉＣ領域２の拡散深さの１／２より薄く設定する。

【０１２６】（ヘ）第１の導体膜（Ｎｉ膜）１７の真空蒸着後、ＳｉＣ基板１を真空蒸着装置のチャンバーから取り出す。続いて、リフトオフ法を用いて、図１６（ｇ）に示すように、開口部の内部のみにＮｉ系電極膜７が選択的に埋設された基板構造を得る。即ち、フォトレジスト２２を完全に除去すると、フォトレジスト２２の上に被着した第１の導体膜（Ｎｉ膜）１７もフォトレジスト２２と共に除かれるので、図１６（ｇ）に示すように、開口部の内部のみに第１の導体素片２７が選択的に残存する。この結果、第１の導体素片２７の周縁部とフィールド絶縁膜５の開口部側壁との間には、微細寸法の側壁ギャップ７７が自己整合的に形成される。

【０１２７】（ト）しかる後、ＳｉＣ基板１を７００℃～１０５０℃の非酸化性雰囲気で、短時間（数分程度）の熱処理を施すと、図１６（ｈ）に示すように、第１の導体素片２７とＳｉＣ基板１が相互に反応して、両者の界面領域に加熱反応層８が生成され、加熱反応層とｎ型ＳｉＣとの間で優れたオーミック特性が実現される。数分程度の短時間の熱処理を行うためには、ＩＲランプ加熱を用いれば良い。ここで「非酸化性雰囲気」とは、第１の実施の形態で説明したように、酸素（O_2）や水（H_2O）等の酸素を含む化合物の気体を含まない雰囲気のことである。厳密には、酸素及び水の分圧を１×１０$^{-8}$Ｐａ～１×１０$^{-10}$Ｐａ程度に制御して、熱処理をすることが好ましい。第１の導体膜の厚みを、その下部にあるｎ型ＳｉＣ領域２の厚みの１／２より薄く設定しておくことにより、第１の導体素片２７が加熱処理で完全に加熱反応層８に転化した場合であっても、ｎ型ＳｉＣ領域２が下部に残されるよう保証される。

【０１２８】（チ）加熱反応層８の形成後に、図１６（ｉ）に示すように、ＳｉＣ基板１全面にＡｌ等の第２の導体膜１９を蒸着する。そして、フォトリソグラフィ法とＲＩＥ等のエッチング技術でパターニングして、図１３に示すような配線導体素片９を形成すれば、本発明の第２の実施の形態に係るオーミック電極構造体が完成する。なお、パターニングの際のエッチャント（＝エッチング液或いはエッチングガス）が電極膜７を侵す時は、第２の導体膜１９は必ず電極膜７を覆うように配設する構成とすれば良い。

【０１２９】このような構成で作製したｎ型ＳｉＣ領域２に対するオーミック電極構造体が実用的コンタクト抵抗を示すか確かめるために、第１の実施の形態と同様な、コンタクト間隔が、Ｌ＝６，１０，１５，２０，２５，３０μｍのリニアＴＬＭコンタクト群を作製した。オーミック・コンタクトの電極をなす長方形の長辺（コンタクト幅）及び短辺の長さは、第１の実施の形態と同

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様にそれぞれ２００μｍ、１００μｍである。

【０１３０】評価した試料の主な構成は次の通りである。リニアＴＬＭコンタクト群は、高抵抗のｐ型４Ｈ－ＳｉＣ基板の上に、エピタキシャル成長させた厚み８００ｎｍ、電子密度１．５×10^{19}／cm^2のｎ型ＳｉＣ領域に形成した。第１の導体膜は５０ｎｍ厚のＮｉ膜、フィールド絶縁膜５の熱酸化膜３は１１００℃ドライ酸化膜（１０ｎｍ厚）、上部絶縁膜４は常圧ＣＶＤで成膜したSiO_2膜（４００ｎｍ厚）である。加熱反応層８の熱処理温度及び熱処理時間、熱処理雰囲気はそれぞれ１０００℃、２分、高純度Ａｒ雰囲気である。第２の導体膜からなる配線導体素片９は厚さ１μｍのＡｌ膜である。

【０１３１】第１の実施形態と同様にＴＬＭ法で評価したところ、コンタクト抵抗ρｃ＝３．３×10^{-6}Ωｃm^2が得られた。高不純物密度エピタキシャル膜でｎ型ＳｉＣ層を形成する替わりに、第１の実施形態と同じ$^{31}P^+$イオン注入と活性化熱処理（条件同一）でｎ型ＳｉＣ層を形成した場合には、他の条件が同じなら、第１の実施形態のＮｉを用いたオーミック電極構造体と誤差の範囲で等しいコンタクト抵抗７．４×10^{-7}Ωｃm^2が得られる。

【０１３２】図１０は、第１の導体膜１７としてのＮｉ膜の厚さを変えた場合の、Ｎｉ膜の厚さ（膜厚）と表面モホロジーとの関係を示す図である。図１０に示した観察においては、加熱反応層８の熱処理条件は、熱処理温度は１０００℃で、熱処理時間は２分である。熱処理雰囲気は高純度Ａｒ雰囲気である。図１０（ａ）は、Ｎｉ膜の膜厚が２００ｎｍで熱処理前の試料の表面モホロジーをスケッチした図である。図１０（ｂ）は、このＮｉ膜の膜厚が２００ｎｍの試料の熱処理後の表面モホロジーをスケッチした図であるが、Ｎｉ膜の膜厚が２００ｎｍでは、表面モホロジーの低下が認められる。図１０（ｃ）は、Ｎｉ膜の膜厚が１００ｎｍの試料に対して、熱処理した場合の表面モホロジーで、膜厚２００ｎｍに比すれば良好であるが、未だ若干の表面モホロジーの低下が認められる。図１０（ｄ）及び図１０（ｅ）は、それぞれ、Ｎｉ膜の膜厚が５０ｎｍ及び２０ｎｍの場合の試料の熱処理後の表面モホロジーで、膜厚５０ｎｍ以下にすれば、フォトリソグラフィ工程等の製造プロセスに対応可能な良好な表面モホロジーが得られることが分かる。

【０１３３】図１１は、第１の導体膜１７としてのＮｉ膜の厚さを変えた場合の、Ｎｉ膜の厚さとオーミック電極構造体のコンタクト抵抗との関係を示す図である。Ｎｉ膜の膜厚が２００ｎｍ及び１００ｎｍではほぼ同程度のコンタクト抵抗である。Ｎｉ膜の膜厚５０ｎｍの場合は、膜厚が２００ｎｍ及び１００ｎｍの場合より低いコンタクト抵抗が得られることが分かる。Ｎｉ膜の膜厚５０ｎｍの試料の熱処理後の表面モホロジーが良好なことを反映していると考えられる。但し、Ｎｉ膜の膜厚２０ｎｍの場合の試料では、コンタクト抵抗の増大が認められる。加熱反応層８の厚さが不十分と思われる。従って、膜厚５０ｎｍの場合が、最もコンタクト抵抗が低いことになる。

【０１３４】図１２は、本発明の第２の実施形態に係るオーミック電極構造体の不純物密度とコンタクト抵抗との関係を、従来技術の結果と共に示す図である。エピタキシャル成長により得られた不純物密度１．５×$10^{19}$$cm^3$のｎ型ＳｉＣ領域に対して、従来のいずれの結果よりも低いコンタクト抵抗ρｃ＝３．３×10^{-7}Ωcm^2の値が得られることが分かる。イオン注入により得られた不純物密度１．５×$10^{20}$$cm^3$のｎ型ＳｉＣ領域に対しても、従来のいずれの結果よりも低いコンタクト抵抗ρｃ＝８．６×10^{-7}Ωcm^2の値が得られることが分かる。このように第２の実施の形態に係るオーミック電極構造体は、従来と同等、或いはそれよりも低い実用的なコンタクト抵抗を、簡単に実現出来る。

【０１３５】（第３の実施形態）本発明の「半導体装置」としては、例えばダイオード、絶縁ゲート型バイポーラトランジスタ（ＩＧＢＴ）、電界効果トランジスタ（ＦＥＴ）、静電誘導トランジスタ（ＳＩＴ）、バイポーラトランジスタ（ＢＪＴ）、静電誘導サイリスタ（ＳＩサイリスタ）、ＧＴＯサイリスタ等の種々の半導体電子デバイスに適用可能である。

【０１３６】一般に半導体電子デバイスは、第１主電極領域、第２主電極領域及び制御電極を有する。第１主電極領域と第２主電極領域との間に主電流の通路が形成される。この主電流は、制御電極に印加される電圧又は電流で制御される。従って、「第１主電極領域」とは、例えば、ＢＪＴやＩＧＢＴにおいては、エミッタ領域又はコレクタ領域のいずれか一方、ＭＯＳＦＥＴやＭＯＳＳＩＴ等の絶縁ゲート型トランジスタ（ＩＧＴ）においては、ソース領域又はドレイン領域のいずれか一方を意味する。「第２主電極領域」とは、ＢＪＴやＩＧＢＴにおいては上記第１主電極領域とはならないエミッタ領域又はコレクタ領域のいずれか一方、ＩＧＴにおいては上記第１主電極領域とはならないソース領域又はドレイン領域のいずれか一方を意味する。即ち、第１主電極領域が、エミッタ領域であれば、第２主電極領域はコレクタ領域であり、第１主電極領域がソース領域であれば、第２主電極領域はドレイン領域である。また、「制御電極」とはＩＧＢＴ及びＩＧＴのゲート電極を意味することは勿論である。また、ダイオード等の制御電極を有しないＳｉＣ半導体装置でも、同様に、第１主電極領域及び第２主電極領域が定義される。

【０１３７】図１７は、本発明の第３の実施の形態に係る半導体装置としての横型ＭＯＳＦＥＴの要部断面図である。第３の実施の形態に係る半導体装置（横型ＭＯＳＦＥＴ）は、ｐ型ＳｉＣ基板１１を用いて構成され、こ

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のｐ型ＳｉＣ基板１１の表面に選択的に形成されたｎ型ＳｉＣ領域２ｓからなる第１の主電極領域（ソース領域）２ｓ、及びｎ型ＳｉＣ領域２ｓからなる第２の主電極領域（ドレイン領域）２ｄとを有している。更に、ｐ型ＳｉＣ基板１１の上には、ゲート酸化膜３が配置されている。ソース領域２ｓとドレイン領域２ｄとの間のゲート酸化膜３の上部には、ゲート電極６３が配置されている。そして、ゲート電極６３の上部及びゲート電極６３が配置されていないゲート酸化膜３の上部には、上部絶縁膜４が形成されている。ゲート酸化膜３と上部絶縁膜４とで、フィールド絶縁膜５が構成されている。

【０１３８】フィールド絶縁膜５中には、ソース領域２ｓの表面を露出するように開口された開口部、ドレイン領域２ｄの表面を露出するように開口された開口部が形成されている。それぞれの開口部の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７ｓ、７７ｄを隔てて、ソース電極膜７ｓ及びドレイン電極膜７ｄが配置されている。更に、フィールド絶縁膜５のソース領域２ｓの上部の開口部の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７ｓを隔て、且つソース電極膜７ｓとソース領域２ｓの間には、加熱反応層８ｓが配置され、ドレイン領域２ｄの上部の開口部の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７ｄを隔て、且つドレイン電極膜７ｄとドレイン領域２ｄの間には加熱反応層８ｄが配置されている。第３の実施の形態に係る半導体装置は、更に、ソース領域２ｓの上部の開口部の内部において、ソース電極膜７ｓの表面に接し、且つフィールド絶縁膜５の上部にまで伸延された第１の主電極配線（ソース配線）９ｓと、ドレイン領域２ｄの上部の開口部の内部において、ドレイン電極膜７ｄの表面に接し、且つフィールド絶縁膜５の上部にまで伸延された第２の主電極配線（ドレイン配線）９ｄとを有している。

【０１３９】なお、半導体装置の設計により、各主電極領域２ｓ、２ｄに配線導体素片（主電極配線）９ｓ、９ｄを介してそれぞれ接続されるボンディングパッド（図示省略）を、フィールド絶縁膜５の上に形成しても良い。ゲート電極６３も同様に、配線導体素片を介してボンディングパッドが接続される。そして、これらの配線導体素片及びボンディングパッドの上部には、酸化膜（SiO_2）、ＰＳＧ膜、ＢＰＳＧ膜、窒化膜（Si_3N_4）、或いはポリイミド膜等からなるパッシベーション膜を形成しても良い。そして、パッシベーション膜の一部に複数の電極層を露出するように複数の開口部（窓部）を設け、ボンディングを可能にすることが出来る。

【０１４０】第３の実施の形態に係る半導体装置によれば、ソース領域２ｓに対するオーミック電極において、ソース電極膜７ｓ及び加熱反応層８ｓを構成する金属材料が、フィールド絶縁膜５と反応しない構造になっている。同様に、ドレイン領域２ｄに対するオーミック電極において、ドレイン電極膜７ｄ及び加熱反応層８ｄを構成する金属材料が、フィールド絶縁膜５と反応しない構造になっている。このため、ソース電極膜７ｓ及びドレイン電極膜７ｄを構成する金属材料との接触面にあるフィールド絶縁膜５が高温熱処理で還元（浸食）されることがない。従って、半導体装置のソース領域２ｓ及びドレイン領域２ｄの周辺に形成されたフィールド絶縁膜５の高い絶縁性が維持出来、リーク電流も低減出来る。

【０１４１】また、ソース電極膜７ｓ及びドレイン電極膜７ｄを構成する金属材料がフィールド絶縁膜５に接していないので、ソース電極膜７ｓ又はドレイン電極膜７ｄとフィールド絶縁膜５の接着力が弱いという問題は、本来的に存在しない。このため、半導体装置の製造プロセス終了後にソース電極膜７ｓ又はドレイン電極膜７ｄが剥落することはなく、半導体装置の製造歩留まりが高くなる。

【０１４２】更に、オーミック電極の底部外縁部における金属－ＳｉＣ－SiO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来るので、低いコンタクト抵抗のオーミック電極が、ソース領域２ｓ又はドレイン領域２ｄに対して形成出来る。また、寄生のショットキー接合の生成に伴うソース領域２ｓ又はドレイン領域２ｄ中の水平方向の電流の流れの阻害もない。この結果、高耐圧で且つ高速に動作可能な半導体装置が実現出来る。特に、電力用半導体装置においては、低いオン抵抗と高速なスイッチングを同時に達成出来る。

【０１４３】特に、ソース電極膜７ｓ及び加熱反応層８ｓの周縁部と開口部側壁との間の側壁ギャップ７７ｓ、及びドレイン電極膜７ｄ及び加熱反応層８ｄの周縁部と開口部側壁との間の側壁ギャップ７７ｄを、フィールド絶縁膜５の厚みより小さい微細寸法と出来るため、ソース領域２ｓ及びドレイン領域２ｄに対するオーミック電極の占有面積を小さく出来、半導体装置の集積密度を向上出来る。

【０１４４】次に図１８～図２０に示す工程断面図（その１～その３）を参照しながら、本発明の第３の実施の形態に係る半導体装置（横型ＭＯＳＦＥＴ）の製造工程を説明する。

【０１４５】（イ）先ず図１４（ａ）から図１４（ｃ）と同様な工程で、８° オフのｐ型４Ｈ－ＳｉＣ基板１１のＳｉ面の表面に、厚さ数１００ｎｍの$1\times10^{19}/cm^3$以上の高不純物密度のｎ型ＳｉＣ領域を、エピタキシャル成長する。そして、エピタキシャル成長を選択的にエッチングすることにより、互いに対向したメサ形状のｎ型ＳｉＣ領域からなるソース領域２ｓ及びドレイン領域２ｄを形成する。即ち、ＳｉＣ基板１１の表面の異なる２つの場所に、互いに一定距離離間して、凸部形状のソース領域２ｓ及びドレイン領域２を形成する。平面図を省略しているが、ソース領域２ｓ及びドレイン領域２は、互いの長辺を平行にした２つの矩形（長方形）の

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パターンとして配列される。集積回路の場合であれば、ソース領域２ｓ及びドレイン領域２を構成する２つの矩形（長方形）のパターンの領域の外側には、素子分離領域が形成される。更に、デバイスの仕様に応じてチャネルストップのイオン注入工程を加えても良く、パワーデバイスならば、ガードリング領域等の形成工程を加えても良い。素子分離領域形成後、周知のＲＣＡ洗浄法等の所定の洗浄法を用いて、ＳｉＣ基板１１を十分清浄化し、図１８（ａ）に示すように、ＳｉＣ基板１１の表面に、厚さ３５～４０ｎｍのゲート酸化膜としての熱酸化膜３を成長する。乾燥酸素中、雰囲気１１５０℃で３時間熱酸化すれば、３５～４０ｎｍの熱酸化膜（ゲート酸化膜）３が得られる。素子分離領域は、トレンチにＣＶＤ法等で堆積した絶縁膜を埋め込む等の方法で、形成すれば良い。ゲート酸化膜３の厚さを、５～２０ｎｍとした場合は、ゲート酸化膜３の上に、更に、厚さ３５～８０ｎｍのシリコン窒化膜（Si_3N_4膜）を常圧ＣＶＤ法で形成し、いわゆるＮＯ膜でゲート絶縁膜を形成しても良い。

【０１４６】（ロ）ゲート酸化膜（ゲート絶縁膜）３の形成後、必要に応じて閾値制御のイオン注入を行う（ゲート酸化膜３の形成前に、閾値制御のイオン注入を行っても良い。）。その後、図１８（ｂ）に示すように、タングステン（Ｗ）、チタン（Ｔｉ）、モリブデン（Ｍｏ）等の高融点金属、或いは、これらのシリサイド（WSi_2，$TiSi_2$，$MoSi_2$）等のゲート電極材料６１を、ゲート酸化膜３の上の全面に、スパッタリング法、真空蒸着法、ＣＶＤ法等で堆積する。そして、ゲート電極材料６１の表面に厚さ１～２μｍのフォトレジスト６２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト６２を選択的に露光し、現像することによって図１８（ｃ）に示すように、ゲート電極６３に対応する部分のフォトレジスト６２のみを選択的に残存させる。更に、フォトレジスト６２をエッチングマスクとして用い、図１８（ｃ）に示すように、ＲＩＥ法とを用いて、ゲート電極材料６１をパターニングし、ソース領域２ｓとドレイン領域２ｄとの間のゲート酸化膜（ゲート絶縁膜）３の上にゲート電極６３を形成する。

【０１４７】（ハ）そして、図１９（ｄ）に示すように、ゲート電極６３の形成後、フォトレジスト６２を除去し、更に、ＲＣＡ洗浄法等でＳｉＣ基板１１の表面を清浄化する。十分清浄化されたゲート電極６３及びゲート酸化膜３の上に、常圧ＣＶＤ法でSiO_2膜からなる上部絶縁膜４を堆積する。この結果、ゲート電極６３以外の領域においては、２層構造からなるフィールド絶縁膜５が形成される。ゲート酸化膜３の厚さと上部絶縁膜４の厚さとを合計したフィールド絶縁膜５の総厚を、１００ｎｍ～６００ｎｍ程度にすることが望ましい。

【０１４８】（ニ）次にフィールド酸絶縁膜５の表面に、本発明の「マスク材」としての厚さ１～２μｍのフォトレジスト２２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、マスク材（フォトレジスト）２２を選択的に露光し、現像することによって開口部６ｓ及び６ｄに対応する部分のフォトレジスト２２を除去し窓部を形成する。続いて、このフォトレジスト２２のマスクパターンをエッチングマスクとして用い、ＳｉＣ基板１１をＢＨＦ溶液に浸漬し、ウェット・エッチングすることで、図１９（ｅ）に示すように、フィールド絶縁膜５に開口部６ｓ及び６ｄを形成する。微細な開口部６ｓ及び６ｄを形成する時は、ガスプラズマを用いたドライ・エッチングが好ましい。例えば、CHF_3やC_2F_6などをエッチャントとしたＲＩＥ法やＥＣＲイオンエッチング等の種々のドライ・エッチングを使用することが出来る。この場合、最初にドライ・エッチングを行い、フィールド絶縁膜５を数１０ｎｍ残したところで、ウェット・エッチングに切り換えるようにする。第１の実施の形態で説明したように、ウェットエッチング単独で、開口部６ｓ及び６ｄを開口する場合でも、ドライエッチングとウェットエッチングの組み合わせで開口する場合でも、ウェット・エッチング又はドライ・エッチングをやや過剰に行い、フィールド絶縁膜５の開口部６ｓ及び６ｄがフォトレジストの開口部より大きくなり、それぞれアンダーカット部が生じるようにする。第１及び第２の実施の形態と同様に、エッチングモニタ部の目視により、ソース領域２ｓとドレイン領域２ｄの表面の露出が確認された後、更に所定の時間オーバーエッチングを追加すればよい。第３の実施形態では、本発明の「マスク材」としてフォトレジスト２２を用いているが、このオーバーエッチング時に、エッチングされない材料であれば、フォトレジスト２２以外の材料を本発明の「マスク材」として採用可能である。

【０１４９】（ホ）その後、エッチングマスクとしてのフォトレジスト２２を残存した状態で、ＢＨＦ溶液を超純水で完全に濯ぎ落とした（リンスした）後、乾燥する。そして、レジストマスク２２が被着した状態のＳｉＣ基板１１を、真空蒸着装置のチャンバー中に速やかに据え付け、直ちに真空排気する。即ち、ＳｉＣ基板１１の表面が大気に露出される時間は、５分以内の可能な限り短時間で行う。そして、真空蒸着装置のチャンバーをターボ分子ポンプ、クライオポンプ等で、1.3×10^{-5}Ｐａ未満の圧力まで真空排気し、図１９（ｆ）に示すように、ＳｉＣ基板１１の表面に第１の導体膜１７を蒸着する。第１の導体膜１７としては、例えばＮｉ膜を用いる。なお、図１９（ｆ）に示すように、開口部６ｓ及び６ｄの側壁に第１の導体膜１７が付着しないようにするためには、オリフィス等を用いて、蒸着ビームの指向性を向上させて行えば良い。この時、図１９（ｆ）に示すように、フィールド絶縁膜５の開口部はフォトレジスト・マスク２２の開口部より大きくなるようにアンダ

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ーカット部が形成されているため、開口部底部に蒸着される第１の導体膜１７ｓ及び１７ｄは、アンダーカット部の形状に正確に転写される。こうして、第１の導体膜１７ｓ及び１７ｄの周縁部とフィールド絶縁膜５の開口部の側壁との間には、距離が一定で、且つ微細寸法の蒸着制限領域（側壁ギャップ）７７ｓ及び７７ｄが発生する。この微細な側壁ギャップ７７ｓ及び７７ｄは、開口部エッチングのオーバーエッチング時間で精密にコントロール出来る。第１の導体膜１７（１７ｓ及び１７ｄ）の厚みは、その下部にあるソース領域２ｓ及びドレイン領域２ｄの拡散深さの１／２より薄く設定する。

【０１５０】（ヘ）第１の導体膜１７の真空蒸着後、ＳｉＣ基板１１を真空蒸着装置のチャンバーから取り出す。続いて、リフトオフ法を用いて、図２０（ｇ）に示すように、それぞれの開口部の内部のみに第１の導体素片２７ｓ及び２７ｄが選択的に埋設される。この結果、それぞれの第１の導体素片２７ｓ及び２７ｄの周縁部とフィールド絶縁膜５の開口部側壁との間には、微細寸法の側壁ギャップ７７ｓ及び７７ｄが自己整合的に形成される。

【０１５１】（ト）しかる後、ＳｉＣ基板１１を７００℃～１０５０℃の非酸化性雰囲気で、短時間（数分程度）の熱処理を施すと、図２０（ｈ）に示すように、第１の導体素片２７ｓ及び２７ｄとＳｉＣ基板１１が相互に反応して、両者の界面領域に加熱反応層８ｓ及び８ｄが生成され、加熱反応層８ｓとソース領域２ｓとの間、及び加熱反応層８ｄとドレイン領域２ｄとの間で、それぞれ優れたオーミック特性が実現される。「非酸化性雰囲気」としての酸素及び水の分圧の制御に関しては、厳重なる管理が必要で、熱処理雰囲気に含まれる酸素及び水の分圧は少なくとも、1×10^{-3} Ｐａ～1×10^{-10} Ｐａ程度、望ましくは、$1.\times10^{-5}$ Ｐａ～1×10^{-10} Ｐａ程度に設定する。

【０１５２】（チ）加熱反応層８ｓ及び８ｄの形成後に、図２０（ｉ）に示すように、ＳｉＣ基板１１全面にＡｌ等の第２の導体膜１９を蒸着する。そして、フォトリソグラフィ法とＲＩＥ等のエッチング技術で、ソース配線９ｓ及びドレイン配線９ｄを パターニングすれば、本発明の第３の実施の形態に係るＭＯＳＦＥＴが完成する（図１７参照。）。

【０１５３】第３の実施の形態に係る半導体装置の製造方法によれば、ソース領域２ｓ及びドレイン領域２ｄに対するオーミック電極を形成するためのコンタクトホールを形成する際に、フィールド絶縁膜５に対するオーバーエッチングのエッチング時間の制御により、窓部近傍のマスク材の下部に形成されるアンダーカット部の深さが制御出来るので、寸法制御が容易である。また、このアンダーカット部の深さにより、オーミック電極を形成するための第１の導体素片２７とフィールド絶縁膜５との一定の間隙（側壁ギャップ）７７ｓ，７７ｄを自己整合的に決定出来るので、オーミック電極とフィールド絶縁膜５との一定の間隙（側壁ギャップ）７７ｓ，７７ｄを制御するためのフォトリソグラフィ工程は不要である。このため、オーミック電極となる第１の導体素片２７とフィールド絶縁膜５の開口部側壁との間隔を十分に小さく出来、占有面積の小さく、微細寸法を有したオーミック電極を配置出来る。

【０１５４】更に、フォトリソグラフィ工程が省略出来るため、半導体装置のソース領域２ｓ及びドレイン領域２ｄに対するオーミック電極形成に係わる工程数が減少し、半導体装置の製造歩留まりが高くなる。更に、第３の実施の形態に係る半導体装置は、標準的なＳｉ半導体デバイス製造方法が適用可能なので、容易且つ信頼性が高い。

【０１５５】更に、第１の導体素片２７が、フィールド絶縁膜５と反応することが防止出来るので、第１の導体素片２７を構成する金属材料との接触面にあるフィールド絶縁膜５が高温熱処理で還元（浸食）されることがなく、フィールド絶縁膜５の絶縁性が維持出来る。また、オーミック電極を構成する金属材料がフィールド絶縁膜５に接していないので、第１の導体素片２７から生成されたオーミック電極とフィールド絶縁膜５の接着力が弱いという問題は、本来的に存在しない。このため、プロセス終了後にオーミック電極が剥落することはなく、製造歩留まりが高くなる。

【０１５６】更に、オーミック電極の加熱反応層８ｓを生成する工程において、オーミック電極の底部外縁部における金属－ＳｉＣ－SiO_2の３元系の共存する状態が存在しないので、３元系の反応による寄生のショットキー接合の生成も回避出来、低いコンタクト抵抗が達成出来る。また、寄生のショットキー接合の生成に伴うソース領域２ｓ及びドレイン領域２ｄの水平方向の電流の流れの阻害もないので、良好な特性の半導体装置が簡単に製造出来る。

【０１５７】（その他の実施の形態）上記のように、本発明は第１乃至第３の実施の形態によって記載したが、この開示の一部をなす論述及び図面はこの発明を限定するものであると理解すべきではない。この開示から当業者には様々な代替実施の形態、実施例及び運用技術が明らかとなろう。

【０１５８】例えば、既に述べた第３の実施の形態の説明においては、リセスゲート構造の横型ＭＯＳＦＥＴに付いて説明したが、図２１に示すような平面ゲート構造の横型ＭＯＳＦＥＴでもかまわない。第３の実施の形態と同様に、ｐ型ＳｉＣ基板１１を用いて構成されているが、図１７とは異なり、ｐ型ＳｉＣ基板１１の表面は同一レベルの平面で構成されている。即ち、ｎ型ＳｉＣ領域からなる第１の主電極領域（ソース領域）２ｓ及び第２の主電極領域（ドレイン領域）２ｄの表面のレベルと、ゲート酸化膜３が配置されているソース領域２ｓと

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ドレイン領域２ｄとの間のｐ型ＳｉＣ基板１１の表面とは同一レベルである。この平面ゲート構造のゲート酸化膜３の上部には、ゲート電極６３が配置されている。そして、ゲート電極６３の上部及びゲート電極６３が配置されていないゲート酸化膜３の上部には、上部絶縁膜４が形成され、ゲート酸化膜３と上部絶縁膜４とで、フィールド絶縁膜５が構成されている。他は、図１７と同様なので、重複した説明を省略する。

【０１５９】図２１に示した、他の実施の形態に係る半導体装置においても、ソース領域２ｓに対するオーミック電極において、ソース電極膜７ｓ及び加熱反応層８ｓを構成する金属材料が、フィールド絶縁膜５と反応せず、ドレイン領域２ｄに対するオーミック電極において、ドレイン電極膜７ｄ及び加熱反応層８ｄを構成する金属材料が、フィールド絶縁膜５と反応しない構造になっている。このため、ソース電極膜７ｓ及びドレイン電極膜７ｄを構成する金属材料との接触面にあるフィールド絶縁膜５が高温熱処理で還元（浸食）されることがない。更に、オーミック電極の底部外縁部における金属－ＳｉＣ－SiO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来るので、低いコンタクト抵抗のオーミック電極が、ソース領域２ｓ又はドレイン領域２ｄに対して形成出来る。

【０１６０】リセスゲート構造や平面ゲート構造の横型ＭＯＳＦＥＴ以外にも、縦型のＭＯＳＦＥＴでも良い。またＵ溝やＶ溝にゲート酸化膜とゲート電極を構成した縦型のＭＯＳＦＥＴでも良い。更に、埋め込みドレイン領域を有するＭＯＳＦＥＴでも良い。埋め込みドレイン領域を有するＭＯＳＦＥＴにおいては、シンカー領域を用いて、埋め込みドレイン領域から電流を引き出すがこの場合オン抵抗の増大が懸念される。しかしながら、本発明の適用により、微細な構造のシンカー領域とこれに接続されるオーミック電極を多数配列することにより、低いオン抵抗と高速なスイッチングを同時に達成出来る。２重拡散構造のｐチャネルのパワーＭＯＳＦＥＴでは、ドリフト領域として機能するｎ型ＳｉＣ基板（或いはν型ＳｉＣ基板若しくはｉ型ＳｉＣ基板）の表面に、ドレイン領域（主電極領域）としての高不純物密度のｎ型ＳｉＣ領域を形成可能である。この場合、ソース領域としての他のｎ型ＳｉＣ領域が、ｎ型ＳｉＣ基板の表面に形成されたｐボディ領域に形成される。

【０１６１】同様に、ｎ型ＳｉＣ基板（或いはν型ＳｉＣ基板）の表面にドレイン領域としてのｎ型ＳｉＣ領域と、ソース領域してのｎ型ＳｉＣ領域を形成し、ソース領域とドレイン領域２の間のｎ型ＳｉＣ基板（或いはν型ＳｉＣ基板）の表面に、ショットキー電極を構成すれば、ＭＥＳＦＥＴが実現出来る。

【０１６２】更に、第３の実施の形態の説明の冒頭で説明したように、ＦＥＴ以外に、本発明の「半導体装置」として、ダイオード、ＩＧＢＴ、ＳＩＴ、ＢＪＴ、ＳＩサイリスタ、ＧＴＯサイリスタ等の種々の半導体電子デバイスに適用可能である。例えば、ｎｐｎ型バイポーラトランジスタであれば、コレクタ領域となる低不純物密度のｎ型（若しくはν型）ＳｉＣ基板の表面に、ｐ型ＳｉＣ領域からなるベース領域をウェル形状に形成し、このベース領域の平面上の内部の位置において、主電極領域（エミッタ領域）としての高不純物密度のｎ型ＳｉＣ領域を形成しても良い。この場合、コレクタ領域となる低不純物密度のｎ型ＳｉＣ基板の代わりに真性半導体（ｉ型）のＳｉＣ基板を用い、ｉ型ＳｉＣ基板の裏面（若しくは表面の一部）に、高不純物密度のｎ型ＳｉＣ領域からなるコレクタ領域を形成しても良い。

【０１６３】ＧＴＯサイリスタ等のサイリスタであれば、ｎベース領域となるｎ型ＳｉＣ基板の表面の一部又は全面に、ｐ型ＳｉＣ領域からなるｐベース領域を形成し、このｐベース領域の内部に、カソード領域（主電極領域）としての高不純物密度のｎ型ＳｉＣ領域をエピタキシャル成長により形成することが可能である。この場合、ｎベース領域となるｎ型ＳｉＣ基板の裏面には、アノード領域としてのｐ型ＳｉＣ領域が形成される。

【０１６４】一方、ｎチャネルの接合型ＦＥＴや接合型ＳＩＴでは、チャネル領域として機能するｎ型ＳｉＣ基板（或いはn^-型（ν型）ＳｉＣ基板、若しくはｉ型ＳｉＣ基板）の表面に、ソース領域（主電極領域）としての高不純物密度のｎ型ＳｉＣ領域を形成可能である。図２２は、切り込みゲート型のＳＩＴの模式的な断面図である。図２２においては、チャネル領域として機能するｎ型ＳｉＣ基板１２の表面に、ソース領域（第１の主電極領域）としての高不純物密度のｎ型ＳｉＣ領域８７が形成され、ｎ型ＳｉＣ基板１２の裏面に、ドレイン領域（第２の主電極領域）としての高不純物密度のｎ型ＳｉＣ領域８１が形成されている。そして、ソース領域８７及びドレイン領域８１間を流れる主電流を制御するために、ｎ型ＳｉＣ基板１２の表面に設けられたゲート溝部の底部にｐ型ＳｉＣ領域８４からなるゲート領域が形成されている。ゲート領域８４には、ゲート加熱反応層８５を介してゲート電極膜８６が接続されている。ゲート電極膜８６には、Ａｌ－Ｔｉ系電極膜が使用可能である。例えば、Ｔｉ（５０ｎｍ厚）／Ａｌ（３００ｎｍ厚）積層膜を用いればよい。そして、ゲート電極膜８６には、Ａｌ、Ａｌ－Ｓｉ、Ａｌ－Ｃｕ－Ｓｉ、Ｃｕ、Ｔｉ－Ｗ等のゲート配線９２が接続されている。ドレイン領域８１には、ドレイン加熱反応層８２を介して、ドレイン電極８３が形成されている。

【０１６５】図２２に示す接合型ＳＩＴでは、ｎ型ＳｉＣ基板１２の表面に選択的に形成されたｎ型ＳｉＣ領域８７からなるソース領域８７を囲んで、ｎ型ＳｉＣ基板１２の上にフィールド絶縁膜５が載置されたている。フィールド絶縁膜５は、熱酸化膜３と、熱酸化膜以外の絶縁膜である上部絶縁膜４とから構成されている。そし

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て、フィールド絶縁膜５中にソース領域８７の表面を露出するように開口された開口部の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７を隔てて配置されたソース電極膜９７、フィールド絶縁膜５の開口部の内部において、フィールド絶縁膜５から一定の間隙（側壁ギャップ）７７を隔て、且つソース電極膜９７とソース領域８７の間に配置されたソース加熱反応層９８、フィールド絶縁膜５の開口部の内部において、ソース電極膜９７の表面に接し、且つフィールド絶縁膜５の上部にまで伸延された第１の主電極配線（ソース配線）９１とを有している。

【０１６６】図２２に示すソース領域８７及びドレイン領域８１間のポテンシャルと、ゲート領域８４に印加されるゲート電圧によるチャネル中のポテンシャルの２次元空間における鞍部点であるポテンシャルの高さが、ドレイン領域８１に印加されるドレイン電圧及びゲート領域８４に印加されるゲート電圧で制御され、主電流が制御される。ＳＩＴの電流・電圧特性は真空管の三極管特性と同様な指数関数則に従った特性を示す。図２２に示す接合型ＳＩＴによれば、ソース領域８７に対するオーミック電極において、ソース電極膜９７及び加熱反応層９８を構成する金属材料が、フィールド絶縁膜５と反応しない構造になっているので、金属材料との接触面にあるフィールド絶縁膜５が高温熱処理で還元（浸食）されることがない。このため、接合型ＳＩＴのソース領域８７の周辺に形成されたフィールド絶縁膜５の高い絶縁性が維持出来、リーク電流も低減出来る。また、ソース電極膜９７を構成する金属材料がフィールド絶縁膜５に接していないので、ソース電極膜９７とフィールド絶縁膜５の接着力が弱いという問題は、本来的に存在しない。このため、接合型ＳＩＴの製造プロセス終了後にソース電極膜９７が剥落することはなく、接合型ＳＩＴの製造歩留まりが高くなる。更に、オーミック電極の底部外縁部における金属－ＳｉＣ－SiO_2の３元系共存反応による寄生のショットキー接合の生成も回避出来るので、低いコンタクト抵抗のオーミック電極が達成出来る。この結果、高耐圧で且つ高速に動作可能な接合型ＳＩＴが実現出来る図２２に示す接合型ＳＩＴにおいて、ドレイン領域としての高不純物密度のｎ型ＳｉＣ領域８１の代わりに、アノード領域としての高不純物密度のｐ型ＳｉＣ領域を形成すれば、ｎチャネルのＳＩサイリスタとなる。この場合、ソース領域としての高不純物密度のｎ型ＳｉＣ領域８７は、カソード領域として機能する。

【０１６７】ｎチャネルのＩＧＢＴでは、ドリフト領域として機能するｎ型ＳｉＣ基板（或いはν型ＳｉＣ基板）の表面（若しくは裏面）に、コレクタ領域としての高不純物密度のｎ型ＳｉＣ領域を形成可能である。この場合、エミッタ領域としての他のｎ型ＳｉＣ領域が、ｎ型（或いはν型）ＳｉＣ基板のコレクタ領域とは異なる位置の表面に形成されたｐボディ領域の内部に形成される。本発明のオーミック電極構造体は、これら種々の半導体電子デバイスの主電極領域としての高不純物密度のｎ型ＳｉＣ領域に適用可能である。上記の第１乃至第３の実施の形態の製造プロセスにおいては、フィールド絶縁膜５の要素である熱酸化膜３は上部絶縁膜４形成の直前に形成する構成となっているが、図２３の工程断面図に示すように、熱酸化膜の形成を上部絶縁膜４形成の直後にする構成としても、ほぼ同様な効果が得られる。

【０１６８】（イ）例えば、第１の実施の形態で説明した方法と全く同様の方法で、ＳｉＣ基板１の表面にｎ型ＳｉＣ領域３２を形成する。そして、ＲＣＡ洗浄法等のＳｉＣ基板１洗浄法を用いて、ＳｉＣ基板１を十分清浄化する。この後、ＳｉＣ基板１の上に、図２３（ａ）に示すように、常圧ＣＶＤ法でSiO_2膜等の酸素透過性絶縁膜４４を堆積する。

【０１６９】（ロ）酸素透過性絶縁膜４４を堆積後、図２３（ｂ）に示すように、乾燥酸素雰囲気で熱処理し、ＳｉＣ基板１の表面を熱酸化し、酸素透過性絶縁膜４４とＳｉＣ基板１との界面に熱酸化膜３を成長する。第１の実施の形態と同様に、熱酸化膜３の厚さは５０ｎｍ未満、好ましくは５～２０ｎｍが望ましい。この結果、熱酸化膜３の上に、酸素透過性絶縁膜（SiO_2膜）４４からなる上部絶縁膜４が位置し、２層構造からなるフィールド絶縁膜５が形成される。

【０１７０】（ハ）この後は、第１の実施の形態で説明した図３（ｆ）以下に示す方法と全く同様の工程を進めることが可能である。即ち、図２３（ｃ）に示すように、フィールド酸絶縁膜５の表面に厚さ１～２μｍのフォトレジスト２２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト２２を選択的に露光し、現像することによって開口部６に対応する部分のフォトレジスト２２を除去する。続いて、このフォトレジスト２２のパターンをエッチングマスクとして用い、ウェット・エッチングすることで、図２３（ｃ）に示すように、フィールド絶縁膜５に開口部６を形成する。このとき、第１の実施の形態で説明したように、ｎ型ＳｉＣ領域３２の表面の露出が確認されたジャストエッチングの後、更に所定のアンダーカット部の深さが得られるまで、オーバーエッチングを追加する。この後の説明は、重複するので省略する。

【０１７１】図２３に示す方法を用いても、$10^{-7}\Omega cm^2$台程度の実用的なコンタクト抵抗ρｃを達成することが可能である。このように、本発明はここでは記載していない様々な実施の形態等を含むことは勿論である。従って、本発明の技術的範囲は上記の説明から妥当な特許請求の範囲に係る発明特定事項によってのみ定められるものである。

【図面の簡単な説明】

【図１】本発明の第１の実施形態に係るオーミック電極構造体の構成を示す要部断面図である。

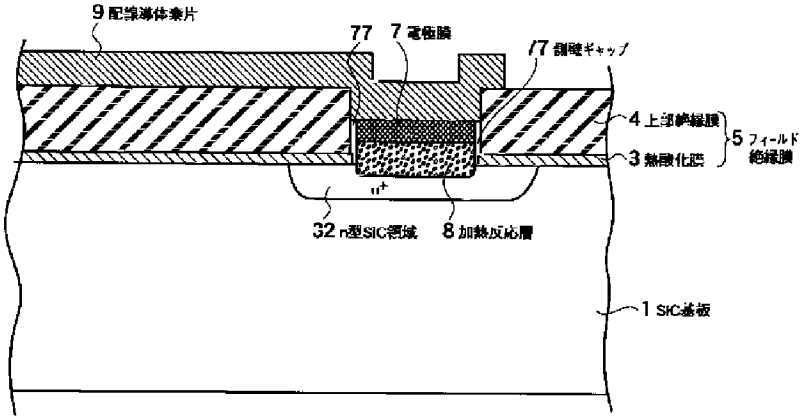
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【図２】本発明の第１の実施形態に係るオーミック電極構造体の製造工程を説明するための工程断面図（その１）である。
【図３】本発明の第１の実施形態に係るオーミック電極構造体の製造工程を説明するための工程断面図（その２）である。
【図４】本発明の第１の実施形態に係るオーミック電極構造体の製造工程を説明するための工程断面図（その３）である。
【図５】本発明の第１の実施形態に係るオーミック電極構造体を説明するためのＴＬＭコンタクト群の電流－電圧特性である。
【図６】本発明の第１の実施形態に係るオーミック電極構造体を説明するためのＴＬＭコンタクト群のＴＬＭ特性を示す図である。
【図７】ノマルスキー干渉顕微鏡によるコンタクト・ウィンドウ内の表面モホロジーの観察結果を示す図である。
【図８】本発明の第１の実施形態に係るオーミック電極構造体の断面ＴＥＭ像をスケッチした図である。
【図９】ラザフォード後方散乱分析により求めた本発明の第１の実施形態に係るオーミック電極構造体の厚み方向の組成の変化を示す図である。
【図１０】本発明の第２の実施形態に係るオーミック電極構造体の厚さと表面モホロジーとの関係を示す図である。
【図１１】本発明の第２の実施形態に係るオーミック電極構造体の電極の厚さとコンタクト抵抗との関係を示す図である。
【図１２】本発明の第２の実施形態に係るオーミック電極構造体の不純物密度とコンタクト抵抗との関係を、従来技術の結果と共に示す図である。
【図１３】本発明の第２の実施形態に係るオーミック電極構造体の構成を示す要部断面図である。
【図１４】本発明の第２の実施形態に係るオーミック電極構造体の製造工程を説明するための工程断面図（その１）である。
【図１５】本発明の第２の実施形態に係るオーミック電極構造体の製造工程を説明するための工程断面図（その２）である。
【図１６】本発明の第２の実施形態に係るオーミック電極構造体の製造工程を説明するための工程断面図（その３）である。
【図１７】本発明の第３の実施形態に係る半導体装置（横型ＭＯＳＦＥＴ）の構成を示す要部断面図である。
【図１８】　本発明の第３の実施形態に係る半導体装置（横型ＭＯＳＦＥＴ）の製造工程を説明するための工程断面図（その１）である。
【図１９】本発明の第３の実施形態に係る半導体装置の製造工程を説明するための工程断面図（その２）である。
【図２０】本発明の第３の実施形態に係る半導体装置の製造工程を説明するための工程断面図（その３）である。
【図２１】本発明の他の実施形態に係る半導体装置（横型ＭＯＳＦＥＴ）の構成を示す要部断面図である。
【図２２】本発明の更に他の実施形態に係る半導体装置（接合型ＳＩＴ）の構成を示す要部断面図である。
【図２３】本発明の更に他の実施形態に係るオーミック電極構造体の製造工程を説明するための工程断面図の一部である。
【図２４】第１の従来技術に係るオーミック電極構造の構成を示す要部断面図である。
【図２５】第２の従来技術に係るオーミック電極構造の構成を示す要部断面図である。
【符号の説明】
１，１１，１２　ＳｉＣ基板
２，３２　ｎ型ＳｉＣ領域
２ｓ　第１の主電極領域（ソース領域）
２ｄ　第２の主電極領域（ドレイン領域）
３　熱酸化膜（ゲート酸化膜）
４　上部絶縁膜
５　フィールド絶縁膜
６　フィールド絶縁膜の開口部
７，４７　電極膜
７ｓ　ソース電極膜
７ｄ　ドレイン電極膜
８，８ｓ，８ｄ　加熱反応層
９　配線導体素片
９ｓ　第１の主電極配線（ソース配線）
９ｄ　第２の主電極配線（ドレイン配線）
１７，１７ｓ，１７ｄ　第１の導体膜
２７，２７ｓ，２７ｄ　第１の導体素片（第１の導体膜の素片）
１９　第２の導体膜
２０　エピタキシャル成長層
２１　エッチングマスク
２２，２３、３４、６２　フォトレジスト
３３　イオン注入マスク
３５　イオン注入スルー膜
４２　第１金属膜（Ｎｉ膜）
４３　Ｓｉ酸化膜（フィールド絶縁膜）
４４　酸素透過性絶縁膜
４５　オーミック接触片
６１　ゲート電極材料
６３　ゲート電極
７７，７７ｓ，７７ｄ　間隙
８１　ドレイン領域（第２の主電極領域）
８２　ドレイン加熱反応層
８３　ドレイン電極

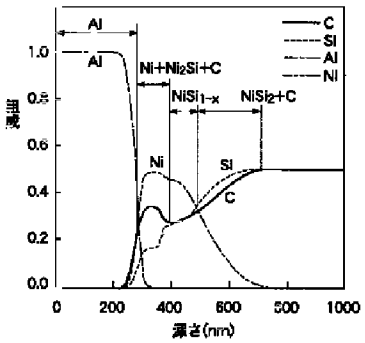
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８４　ゲート領域
８５　ゲート加熱反応層
８６　ゲート電極膜
８７　ソース領域（第１の主電極領域）
９１　第１の主電極配線（ソース配線）
９２　ゲート配線
９７　ソース電極膜
９８　ソース加熱反応層

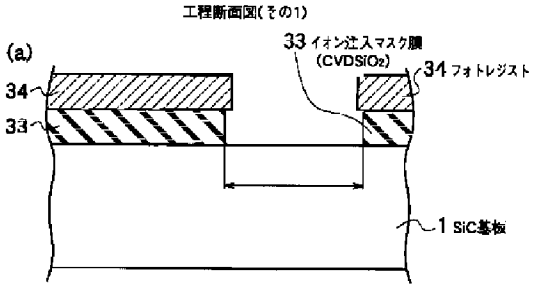
【図１】



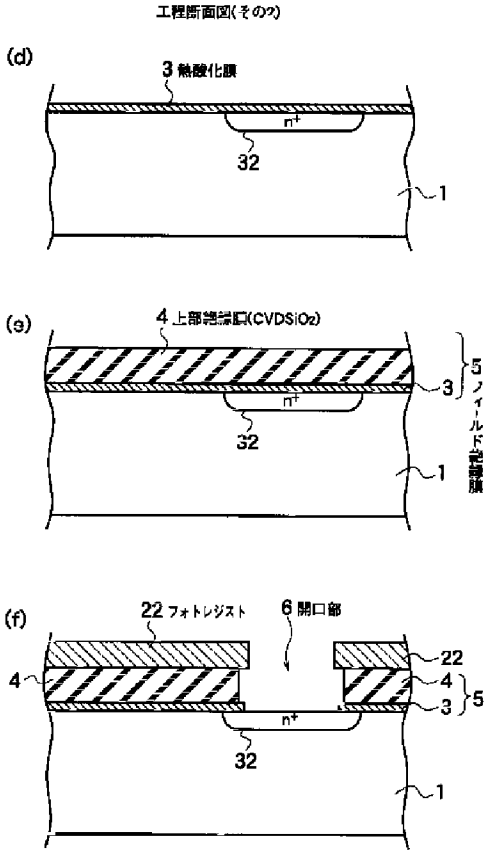
【図９】



【図２】

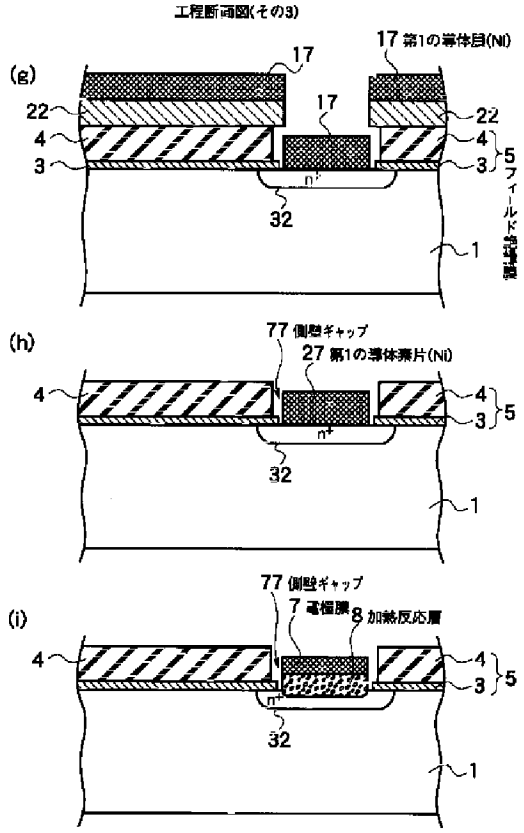


【図３】

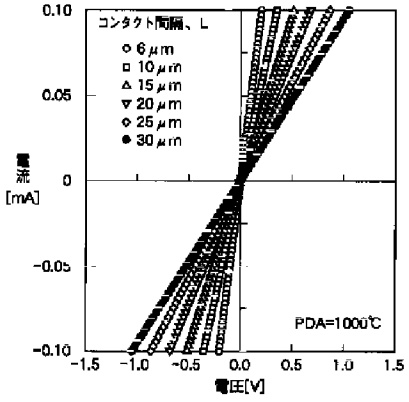


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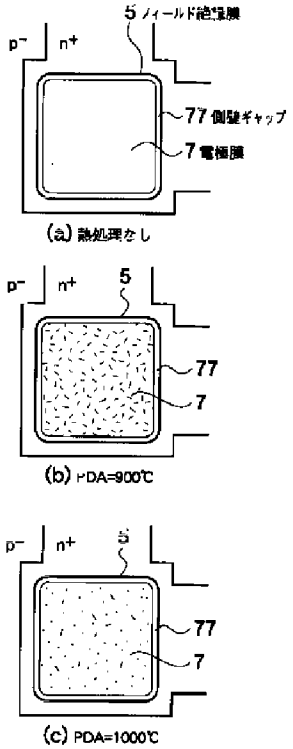
【図4】



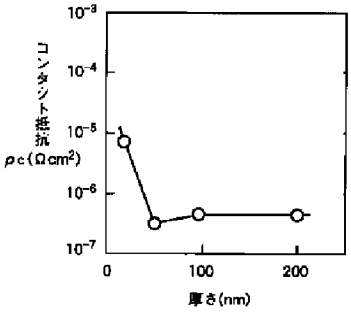
【図5】



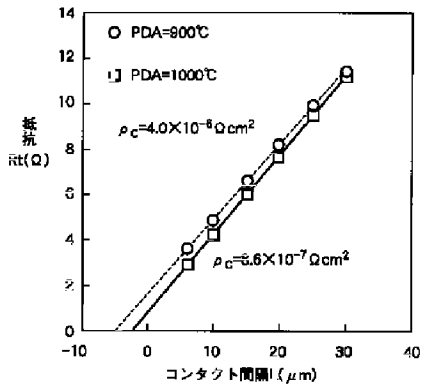
【図7】



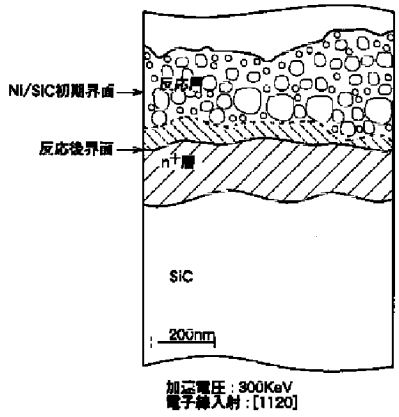
【図11】



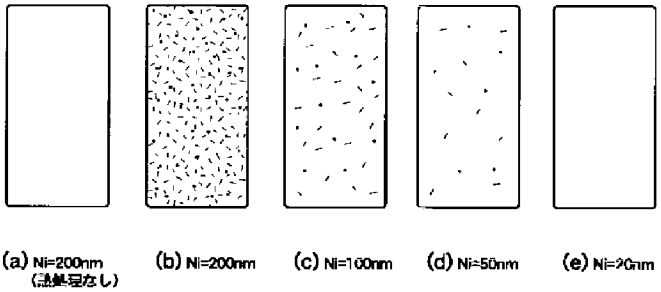
【図6】



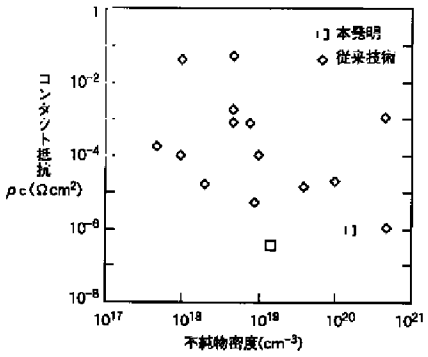
【図8】



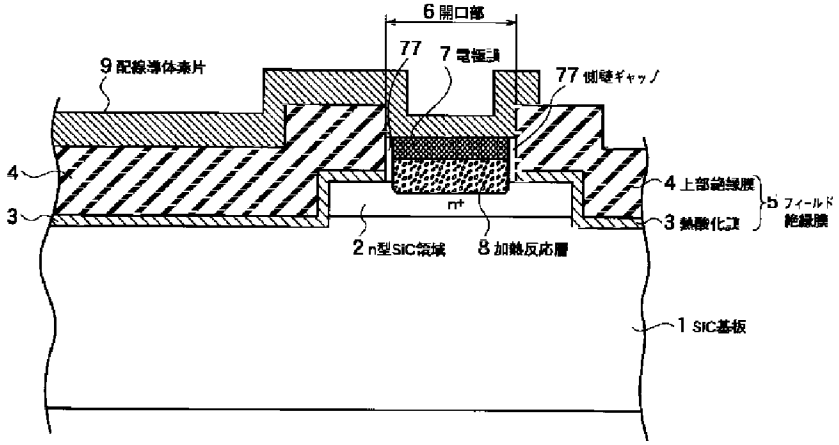
【図10】



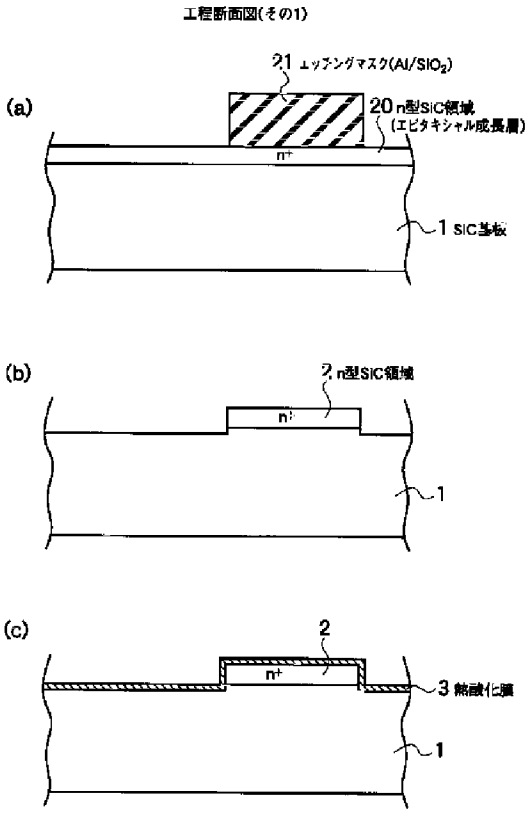
【図12】



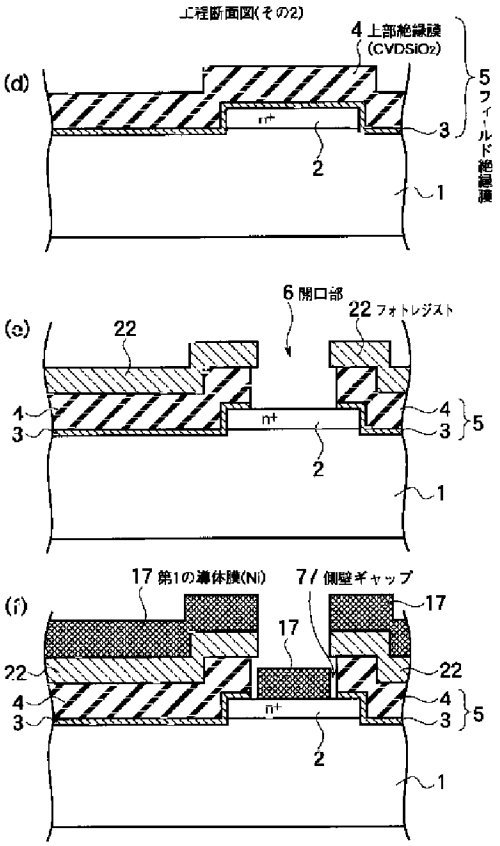
【図13】



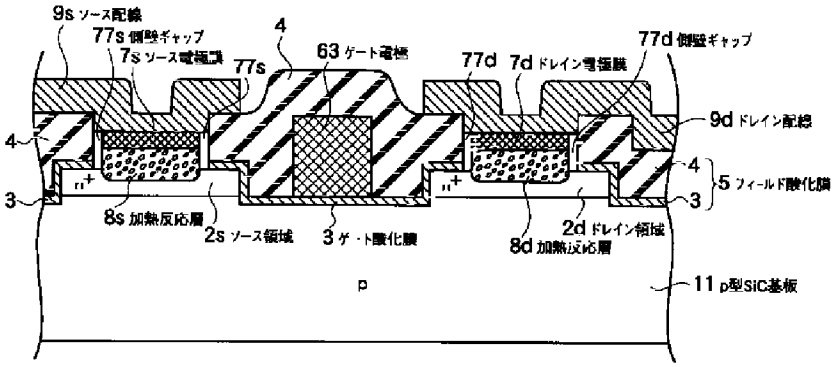
【図14】


工程断面図(その1)
(a)
21 エッチングマスク(Al/SiO2)
20 n型SiC領域
(エピタキシャル成長層)
n+
1 SiC基板
(b)
2 n型SiC領域
n+
1
(c)
2
n+
3 熱酸化膜
1

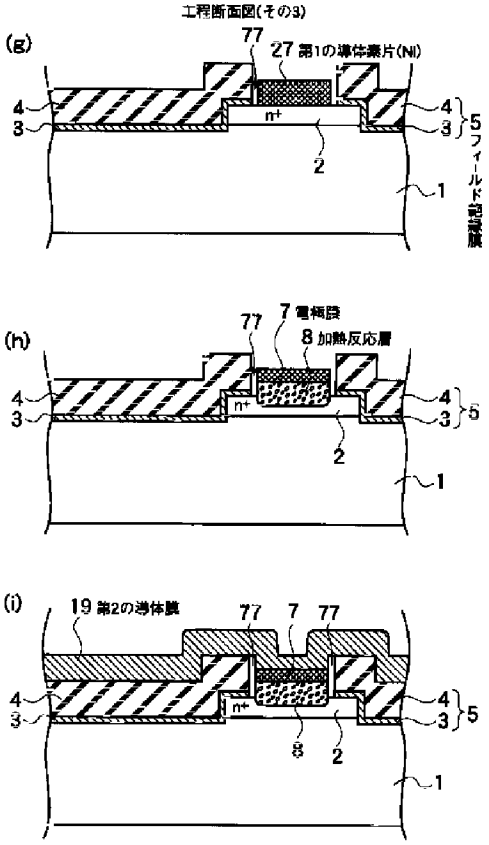
【図15】


工程断面図(その2)
(d)
4 上部絶縁膜
(CVDSiO2)
5 フィールド絶縁膜
n+
3
2
1
(e)
6 開口部
22 フォトレジスト
22
4
3
n+
4
3
5
2
1
(f)
17 第1の導体膜(Ni)
7 側壁ギャップ
17
17
22
22
4
3
n+
4
3
5
2
1

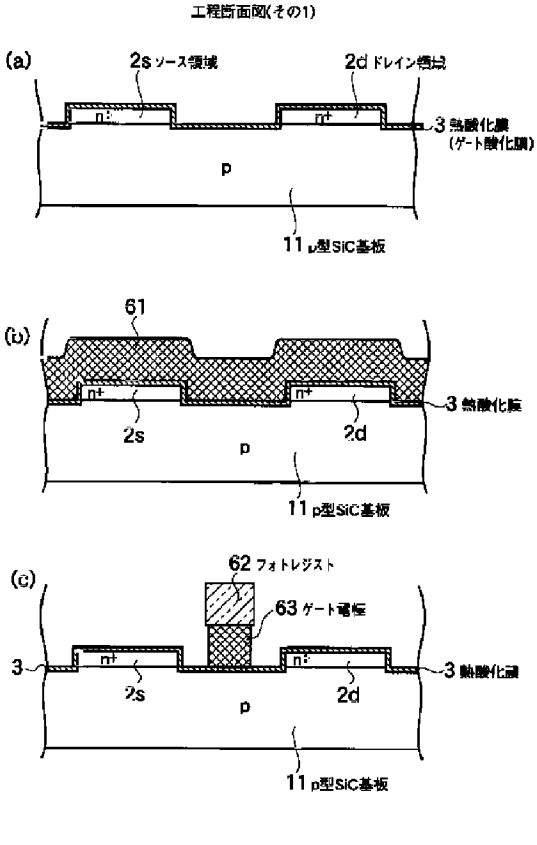
【図17】


9s ソース配線
77s 側壁ギャップ
7s ソース電極膜
77s
4
63 ゲート電極
77d
7d ドレイン電極膜
77d 側壁ギャップ
9d ドレイン配線
4
3
n+
n+
4
5 フィールド酸化膜
3
8s 加熱反応層
2s ソース領域
3 ゲート酸化膜
2d ドレイン領域
8d 加熱反応層
p
11 p型SiC基板

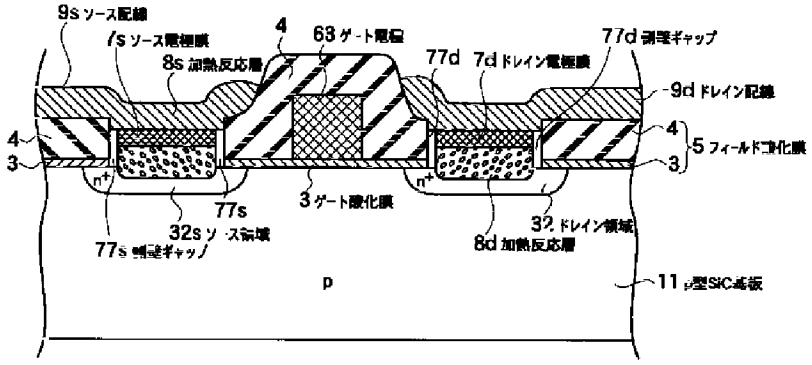
【図16】



【図18】

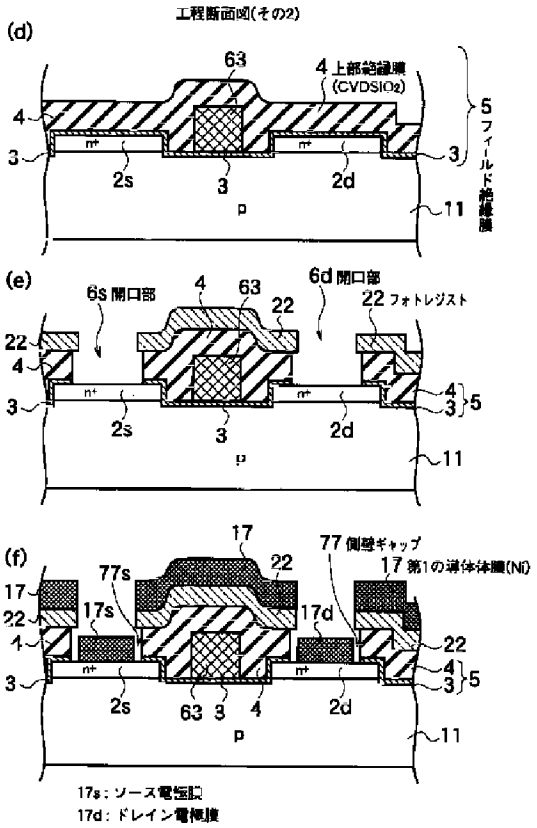


【図21】

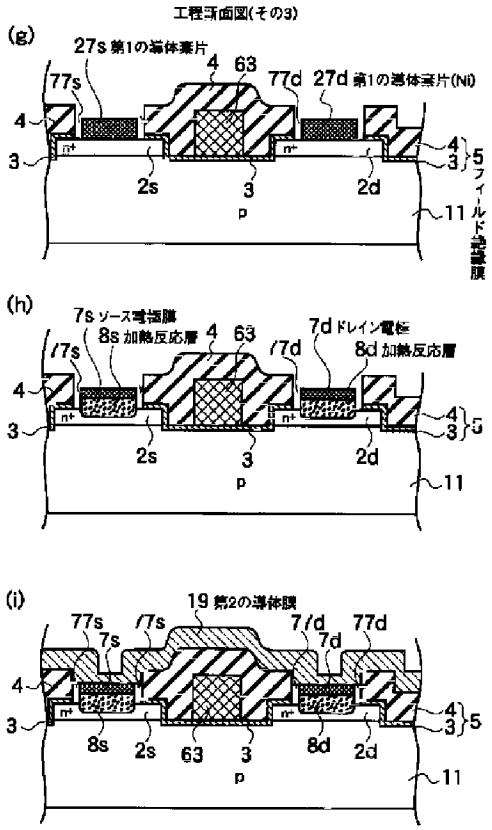


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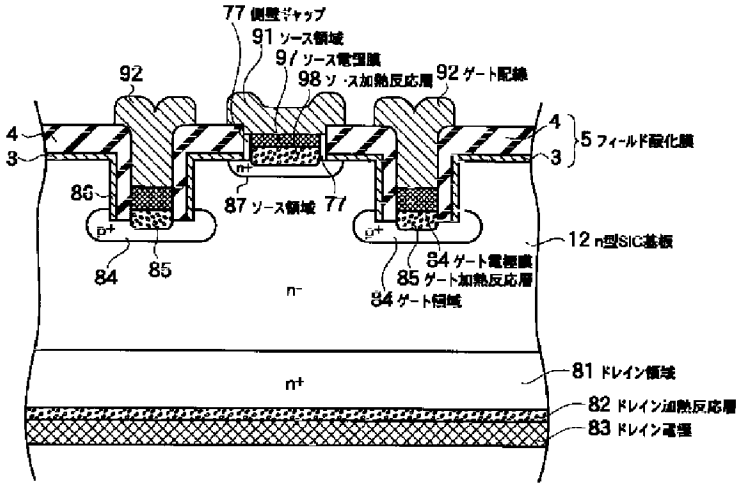
【図19】


工程断面図(その2)
(d)
63
4 上部絶縁膜 (CVDSiO2)
5 フィールド絶縁膜
4
3
n+
2s
3
2d
p
11
(e)
6s 開口部
6d 開口部
22 フォトレジスト
22
(f)
17
77 側壁ギャップ
17 第1の導体体膜(Ni)
77s
17s
17d
63
17s：ソース電極膜
17d：ドレイン電極膜

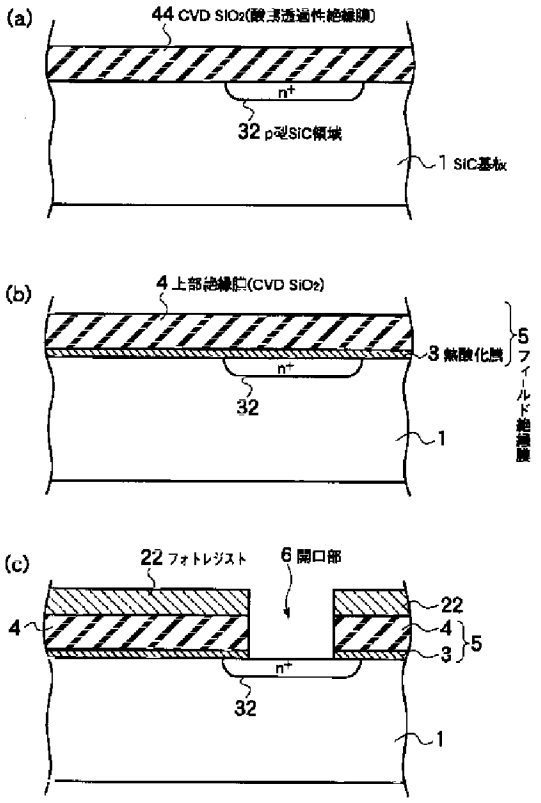
【図20】


工程断面図(その3)
(g)
27s 第1の導体薄片
27d 第1の導体薄片(Ni)
77s
77d
(h)
7s ソース電極膜
8s 加熱反応層
7d ドレイン電極
8d 加熱反応層
(i)
19 第2の導体膜
7s
7d
8s
8d

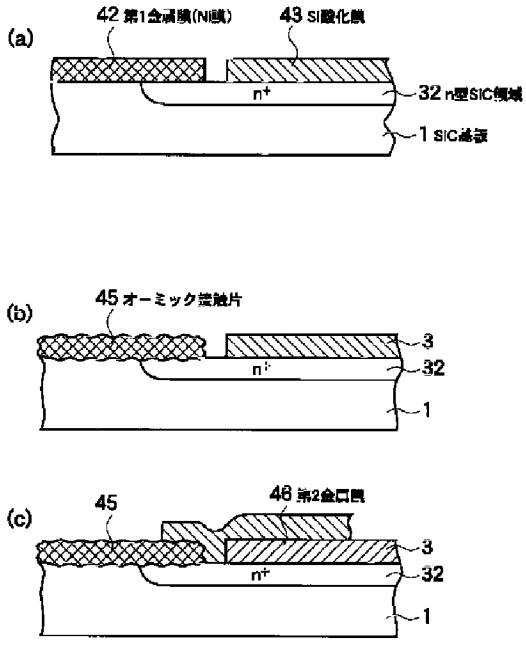
【図22】


77 側壁ギャップ
91 ソース領域
97 ソース電極膜
98 ソース加熱反応層
92
92 ゲート配線
4
3
5 フィールド酸化膜
86
87 ソース領域
77
p+
84
85
12 n型SiC基板
84 ゲート電極膜
85 ゲート加熱反応層
84 ゲート領域
n-
n+
81 ドレイン領域
82 ドレイン加熱反応層
83 ドレイン電極

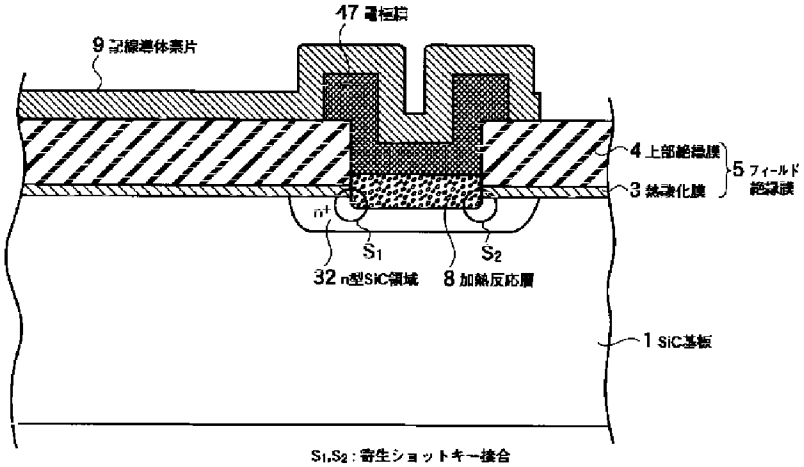
【図23】



【図25】



【図24】



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	21/336			３０１Ｐ
	29/78	６５２	29/80	F
	21/338			V
	29/812		29/91	A
	29/80			
	21/329			

(72)発明者　谷本　智
神奈川県横浜市神奈川区宝町２番地　日産自動車株式会社内

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5F102 FB01 GB04 GC08 GC09 GD01 GD04 GJ02 GR01 GR04 GS04 GV07 HC07 HC11 HC15 HC21

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JP2002093742A OHMIC ELECTRODE STRUCTURE, ITS MANUFACTURING METHOD, SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SEMICONDUCTOR DEVICE

Applicants: NAT INST OF ADV IND & TECHNOL,NISSAN MOTOR

Inventors: OGUSHI HIDEYO,TANIMOTO SATOSHI

Classifications:

IPC ***H01L21/28; H01L21/329; H01L21/331; H01L21/336; H01L21/338; H01L29/12; H01L29/73; H01L29/74; H01L29/744; H01L29/78; H01L29/80; H01L29/812;*** (IPC1-7): H01L21/28; H01L21/329; H01L21/331; H01L21/336; H01L21/338; H01L29/73; H01L29/74; H01L29/744; H01L29/78; H01L29/80; H01L29/812;

CPC **H01L21/0485 (EP);**

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Publication: JP2002093742A·2002-03-29

Published as: JP2002093742A;**JP4671314B2**

OHMIC ELECTRODE STRUCTURE, ITS MANUFACTURING METHOD, SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To provide a fine and highly reliable ohmic electrode structure, having a low contact resistance of on the order of 10-7 Ωcm2. SOLUTION: A structure comprises an SiC substrate 1, an n-type SiC region 32 formed in a surface of the SiC substrate 1, a field insulating film 5 mounted on the SiC substrate 1, an electrode film 7 spaced a fixed clearance (sidewall gap) 77 apart from the field insulating film 5 inside an opening part which is opened to expose the n-type SiC region 32 in the field insulating film 5, a heating reaction layer 8 disposed between the electrode film 7 and the n-type SiC region 32 and a wiring conductor piece 9, which is in contact with the surface of the electrode layer 7 and extended up to the upper part of the field insulating film 5 inside an opening part of the field insulating film 5. The fixed clearance constituting the sidewall gap 77 is controlled to a value, which is smaller than the thickness of the field insulating film 5.

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DESCRIPTION JP2002093742

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device using a silicon carbide (SiC) substrate and a method for manufacturing the semiconductor device, and further to an n-type SiC region used in this SiC semiconductor device. The present invention relates to an ohmic electrode structure and a manufacturing method thereof.

[0002]

2. Description of the Related Art SiC is capable of forming a pn junction and has a wider forbidden band width Eg than other semiconductor materials such as silicon (Si) and gallium arsenide (GaAs). Values of about 2.93 eV for 23 eV and 6 H-SiC and about 3.26 eV for 4 H-SiC have been reported. Further, since SiC is thermally, chemically and mechanically stable and has excellent radiation resistance, it can be used not only for light emitting devices and high frequency devices, but also under severe conditions such as high temperature, high power, and radiation irradiation. As a power semiconductor device (power device) showing high reliability and stability, it is expected to be applied in various industrial fields.

[0003]

In particular, it has been reported that a high breakdown voltage MOSFET using SiC has a lower

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on-resistance than a power device using Si. It has also been reported that the Schottky diode using SiC has a low forward voltage drop. As is well known, there is a trade-off relationship between the ON resistance of a power device and the switching speed. However, according to the power device using SiC, there is a possibility that low ON resistance and high switching speed can be achieved at the same time.

[0004]

In order to reduce the on-resistance of this power device using SiC, the reduction of the contact resistance ρ c with respect to the ohmic contact is an important factor. In particular, in order to reduce the on-resistance, a method of subdividing the main electrode region of the power device and arranging it on the SiC substrate with high density is also adopted. In order to reduce the ON resistance of such a finely sized power device, it is extremely important to obtain a low contact resistance ρ c inside the fine opening (contact window). Further, the contact resistance ρ c of the ohmic contact with respect to the SiC region is a big problem in order to increase the switching speed of the power device.

[0005]

Contrary to the fact that the SiC blue light emitting element has already been put into practical use and mass-produced, the application of SiC as a power device and a high frequency device has been greatly delayed. One of the causes of this is that the technology for forming a practical low resistance ohmic contact suitable for the structure and manufacturing process of these devices has not been established yet.

[0006]

A conventional technique widely used as a method for forming a low resistance ohmic contact on n-type SiC is to use an electrode film such as nickel (Ni), tungsten (W) or titanium (Ti) on n-type SiC. It is a method of heat-treating the deposited ohmic electrode structure at a high temperature of 800 ° C to 1200 ° C. In particular, the ohmic contact using Ni has a practical contact resistance value ρ c of the order of $10^{-6}\ \Omega \cdot \mathrm{cm}^2$ and is an extremely promising ohmic contact.

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[0007]

FIG. 24 shows the structure of an ohmic electrode structure using a Ni film used in power devices, high frequency devices, etc. (hereinafter referred to as "first conventional technology").) Is simplified and shown. An n-type SiC region 32 having a high impurity density is formed on the surface of single crystal SiC substrate 1. A field insulating film 5 including a thermal oxide film 3 and an upper insulating film 4 is further formed on the surface of the single crystal SiC substrate 1. An opening is arranged so as to penetrate the field insulating film 5 and expose the surface of the n-type SiC region 32. Inside the opening of the field insulating film 5, a heating reaction layer 8 in contact with the surface of the n-type SiC region 32 and an electrode film (Ni film element) 47 on the heating reaction layer 8 are arranged. . The heating reaction layer 8 is formed by depositing a Ni film on the entire surface, patterning it into the shape shown in FIG. 24 by using photolithography and etching, and then performing heat treatment. That is, the SiC substrate 1 provided with the electrode film (Ni film element) 47 is subjected to a high temperature treatment at 1000 ° C. to 1200 ° C. to form the conductive heating reaction layer 8 mixed with Ni—Si—C. To be done. On the upper part of the electrode film (Ni film element) 47, the wiring conductor element 9 is arranged so as to extend to the upper part of the field insulating film 5.

[0008]

The first conventional technique has the following problems. Therefore, in order to solve the problem of the first conventional technique, Japanese Unexamined Patent Publication No. 8-64801 discloses a method of forming an ohmic electrode for the n-type SiC region 32 formed by ion implantation (hereinafter, referred to as " The second prior art ".). In the method described in the second conventional technique, (a) the first metal film (Ni film) 42 is formed in the opening so as to be isolated from the Si oxide film (field insulating film) 43 as shown in FIG. (B) After that, high-temperature heat treatment is performed to generate ohmic contact pieces 45 as shown in FIG. 25 (b); (c) Finally, ohmic contact pieces as shown in FIG. 25 (c). This is a method according to the procedure of connecting the second metal film to the surfaces of 45 and the exposed n-type SiC region 32.

[0009]

First, in the ohmic electrode structure for the n-type SiC region 32 according to the first conventional technique shown in FIG. 24, 1) the Ni film 47 and the field insulating film 5 are formed. Since the adhesion is weak and the Ni film 47 often peels off after vapor deposition, the

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manufacturing yield is poor; 2) The field insulating film (SiO 2 film) 5 on the contact surface with the Ni film 47 reacts with the Ni film 47 by high temperature heat treatment. (Reduced), the SiO 2 film 5 is eroded and thinned. When the SiO2 film 5 is originally thin, the insulation property of the SiO2 film 5 is impaired, and when the SiO2 film 5 is extremely thin, the SiO2 film 5 penetrates; Immediately below the outer edge corners S1 and S2 of the reaction layer 8, a high-temperature heat treatment forms a parasitic Schottky junction, which impedes horizontal current flow; 4) High-temperature heat treatment causes an electrode film (Ni film element) The surface of 47 is severely roughened, and the surface morphology deteriorates. Therefore, if the alignment mark for the photolithography process has a similar Ni film 47 structure, its formation becomes difficult. Therefore, high-precision photolithography and etching cannot be performed in the subsequent steps; 5) An oxide film such as NiO or SiO2 or hydro carbon is generated on the surface of the electrode film (Ni film element) 47 by high temperature heat treatment, and the electrode film There is a problem that the contact resistance between the (Ni film element) 47 and the wiring conductor element 9 is substantially increased.

[0010]

The second prior art is a method for solving the problems 2) and 3) of the problems of the first prior art. That is, the ohmic contact piece 45 is isolated from the Si oxide film (field insulating film) 43, and the second metal film in contact with the exposed surface of the n-type SiC region 32 is not subjected to the heat treatment. The characteristic feature is that a parasitic Schottky junction due to the coexistence of Ni-SiC-SiO2 is not formed.

[0011]

However, in the second conventional technique, the first metal film (Ni film) 42 is separated from the Si oxide film (field insulating film) 43 and patterned in the opening shown in FIG. No such method is disclosed. Generally, in such a case, the method used is to deposit a Ni film on the entire surface of the SiC substrate 1 and use photolithography and etching of Ni to selectively deposit the first metal film (Ni film) inside the opening. This is a method of disposing 42. However, the combination of the second conventional technique and this method cannot basically solve the problems 1), 4), and 5).

[0012]

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Furthermore, since an independent photolithography process is used in the patterning method of the first metal film (Ni film) 42, the alignment accuracy of the exposure apparatus (mask aligner) and the first metal film (Ni film) 42 Considering the etching processing accuracy, there is a problem that the tolerance of the distance between the ohmic contact piece 45 and the side wall of the opening of the Si oxide film (field insulating film) 43 must be sufficiently large. This leads to a problem that it is difficult to manufacture a fine ohmic electrode structure having a high integration density. As a result, the problem is that the device size and the chip area increase, and the production cost (chip unit price) of the semiconductor device increases.

[0013]
The present invention has been made to solve the problems of the conventional ohmic electrode structure for the n-type SiC region and the semiconductor device using the same, or simultaneously.

[0014]
Specifically, an object of the present invention is to provide a novel structure of a fine ohmic electrode structure for an n-type SiC region having a practical contact resistance of about 10^{-7} Ωcm 2.

[0015]
Another object of the present invention is to provide a novel structure of an ohmic electrode structure which has good adhesion between the surface metal wiring (wiring conductor element) and the field insulating film and has high reliability.

[0016]
Still another object of the present invention is to provide a novel structure of an ohmic electrode structure which can maintain the insulating property of a field insulating film and has a high breakdown voltage and a low leakage current.

[0017]
Still another object of the present invention is to provide a novel structure of the ohmic electrode structure in which the parasitic Schottky junction does not exist on the outer edge of the ohmic electrode.

[0018]

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Still another object of the present invention is to provide a novel structure of an ohmic electrode structure having a good surface morphology of the electrode film.

[0019]
Still another object of the present invention is to provide an ohmic electrode structure having fine dimensional accuracy.

[0020]
Still another object of the present invention is to provide a method for manufacturing an ohmic electrode structure in which defects such as peeling of surface metal wiring after deposition of a conductor film are suppressed and the manufacturing yield is high.

[0021]
Still another object of the present invention is to provide a method for manufacturing an ohmic electrode structure capable of effectively avoiding an erosion reaction (reduction reaction) between a conductor film serving as a base material of an ohmic electrode and a field insulating film. is there.

[0022]
Still another object of the present invention is to provide a method of manufacturing an ohmic electrode structure in which a reaction of a ternary system with a conductor film serving as a base material of an ohmic electrode, SiC and a field insulating film is avoided. is there.

[0023]
Still another object of the present invention is to provide a method for producing an ohmic electrode structure in which the surface morphology of the electrode film is good even after the high temperature heat treatment.

[0024]
Still another object of the present invention is to manufacture an ohmic electrode structure which does not affect the shape of the alignment mark for the photolithography process and facilitates highly accurate photolithography and etching in the subsequent process. Is to provide a method.

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[0025]
Still another object of the present invention is to maintain a low contact resistance between the electrode film and the wiring conductor element without causing oxide film or hydrocarbon on the surface of the electrode film even after the high temperature heat treatment. A method of manufacturing an ohmic electrode structure is provided.

[0026]
Still another object of the present invention is to set the distance between the electrode film (ohmic contact piece) and the side wall of the opening of the field insulating film without being affected by the alignment accuracy and etching processing accuracy of the exposure apparatus in the photolithography process. An object of the present invention is to provide a method for manufacturing an ohmic electrode structure that can be sufficiently miniaturized.

[0027]
Still another object of the present invention is to provide a method of manufacturing an ohmic electrode structure which can easily manufacture an ohmic electrode structure having fine dimensional accuracy.

[0028]
Still another object of the present invention is to provide a semiconductor device having a high breakdown voltage and capable of operating at high speed.

[0029]
Still another object of the present invention is to provide a semiconductor device having a low on-resistance and capable of high-speed switching.

[0030]
Still another object of the present invention is to provide a semiconductor device which has a small chip occupying area, a low chip unit price, and high reliability.

[0031]
Still another object of the present invention is to provide a method of manufacturing a semiconductor device in which defects such as peeling of surface metal wiring are suppressed and the manufacturing yield is high.

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[0032]
Still another object of the present invention is to effectively prevent the erosion reaction (reduction reaction) between the conductor film, which is the base material of the ohmic electrode, and the field insulating film during the high temperature heat treatment, and to prevent the conductor film, SiC and the field. It is an object of the present invention to provide a method for manufacturing a semiconductor device which can avoid a reaction of a ternary system with an insulating film.

[0033]
Still another object of the present invention is that even after the high temperature heat treatment, the surface morphology of the electrode film is good, the shape of the alignment mark for the photolithography process is not affected, and the accuracy of the subsequent process is high. It is to provide a method for manufacturing a semiconductor device capable of various photolithography and etching.

[0034]
Still another object of the present invention is to maintain a low contact resistance between the electrode film and the wiring conductor element without causing an oxide film or hydrocarbon on the surface of the electrode film even after the high temperature heat treatment. A method of manufacturing a semiconductor device is provided.

[0035]
Still another object of the present invention is to make the space between the electrode film (ohmic contact piece) and the side wall of the opening of the field insulating film sufficiently fine, and to easily form an ohmic electrode structure having fine dimensional accuracy. A method of manufacturing a semiconductor device that can be manufactured.

[0036]
Still another object of the present invention is to provide a method of manufacturing a semiconductor device which can reduce the chip area and can reduce the unit cost of the chip.

[0037]

In order to achieve the above object, the invention according to claim 1 is characterized in that

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(a) an SiC substrate and (b) n selectively formed on the surface of the SiC substrate. -Type SiC region, (c) a field insulating film placed on a SiC substrate, and (d) an opening (contact window) opened to expose the surface of the n-type SiC region in the field insulating film.) Inside the field insulating film with a certain gap, and (e) inside the opening of the field insulating film, with a certain gap from the field insulating film and n. A heating reaction layer disposed between the type SiC regions, and (f) a wiring conductor piece that is in contact with the surface of the electrode film inside the opening of the field insulating film and extends to the upper part of the field insulating film. The gist is that it is an ohmic electrode structure made of.

According to the invention of claim 1, both the electrode film and the heating reaction layer are arranged inside the opening of the field insulating film with a certain gap from the field insulating film. It is possible to prevent the metal material forming the above from reacting with the field insulating film.

Further, it is possible to avoid the formation of parasitic Schottky junction due to the ternary coexistence reaction of metal-SiC-SiO2 at the bottom outer edge of the heating reaction layer.

[0038]

The "n-type SiC region selectively formed on the surface of the SiC substrate" defined in claim 1 is not limited to the case where the n-type SiC region is directly formed on the surface of the SiC substrate. Of course.

For example, another semiconductor region having a plane area larger than that of the n-type SiC region is arranged in a well shape on a part of the surface of the SiC substrate, and at the position inside the well-shaped semiconductor region, n of the present invention is formed. A type SiC region may be formed.

Alternatively, the case where another semiconductor region is epitaxially grown on the entire surface of the SiC substrate and the n-type SiC region of the present invention is formed on a part of the surface of the other epitaxially grown semiconductor region is allowed.

As described above, it should be noted that the invention according to claim 1 allows the case where the n-type SiC region is indirectly formed via another semiconductor region.

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[0039]
The invention according to claim 2 is, in the ohmic electrode structure according to claim 1, characterized in that the constant gap is smaller than the thickness of the field insulating film.

[0040]
According to a third aspect of the present invention, in the ohmic electrode structure according to the first or second aspect, the field insulating film includes a thermal oxide film of SiC and an insulating film having a composition or a density different from that of the thermal oxide film. The gist is that it is composed of a laminated insulating film with an upper insulating film that is

[0041]
According to a fourth aspect of the present invention, in the ohmic electrode structure according to any one of the first to third aspects, the dielectric breakdown electric field strength of the upper insulating film is lower than the dielectric breakdown electric field strength of the thermal oxide film. That is the summary.

[0042]

According to a fifth aspect of the present invention, in the ohmic electrode structure according to any one of the first to fourth aspects, the etching rate of the upper insulating film by the buffered hydrofluoric acid solution (BHF solution) is higher than that of the thermal oxide film. The gist is that the etching rate is faster than that of the buffered hydrofluoric acid solution.

The "BHF solution" is an etching solution (etchant) for a silicon oxide film (SiO2 film) known to those skilled in the art, which is composed of a solution of ammonium fluoride (NH4F): hydrofluoric acid (HF) = 7: 1.

[0043]

According to a sixth aspect of the invention, (a) a step of forming an n-type SiC region having a high impurity density on at least a part of the surface of the SiC substrate, and (b) a step of cleaning the surface of the SiC substrate. , (C) a step of covering the surface of the SiC substrate

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with a field insulating film, (d) a step of forming a mask material having an etching rate different from that of the field insulating film on the field insulating film, and (e) a mask material. A step of forming a window portion and forming a mask pattern; (f) a step of etching the field insulating film using the mask pattern until the surface of the n-type SiC region is exposed to form an opening portion; After the surface of the type SiC region is exposed, the field insulating film is further over-etched to form an undercut portion under the mask material in the vicinity of the window, and (h) n in the upper portion of the mask material and inside the opening. A step of depositing the first conductor film on the surface of the n-type SiC region, and (i) removing the mask material, so that a constant gap from the field insulating film is formed on the surface of the n-type SiC region inside the opening. Between the first conductive film element and the n-type SiC region by heat-treating the SiC substrate in a step of leaving the first conductive film element in a non-oxidizing atmosphere. The gist is a method for manufacturing an ohmic electrode structure including a step of forming a heating reaction layer.

According to the invention of claim 6, the depth of the undercut portion formed under the mask material in the vicinity of the window portion is controlled by controlling the etching amount of "over etching (slight etching)" of the field insulating film. I can.

Further, the depth of the undercut portion can determine a constant gap between the element of the first conductor film and the field insulating film in a self-aligned manner.

Similar to claim 1, the “step of forming an n-type SiC region having a high impurity density on at least a part of the surface of the SiC substrate” defined in claim 6 is performed directly on the surface of the SiC substrate. It is not limited only to the case of forming.

For example, another semiconductor region may be formed in a well shape on a part of the surface of the SiC substrate, and the n-type SiC region may be formed inside the well-shaped semiconductor region.

Alternatively, a step of epitaxially growing another semiconductor region on the entire surface of the SiC substrate and forming an n-type SiC region on a part of the surface of the epitaxially grown semiconductor region is also allowed.

[0044]
According to a seventh aspect of the invention, in the method of manufacturing an ohmic

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electrode structure according to the sixth aspect, the step of covering with the field insulating film is a step of growing a thermal oxide film on the surface of the SiC substrate by thermal oxidation. And a step of depositing an insulating film on the thermal oxide film by a method other than thermal oxidation.

[0045]
According to an eighth aspect of the present invention, in the method for manufacturing an ohmic electrode structure according to the sixth aspect, the step of covering with the field insulating film is a method other than thermal oxidation, and the surface of the SiC substrate is covered with an oxygen-permeable insulating material. It is characterized by comprising a step of depositing a film and a step of growing a thermal oxide film on the interface between the surface of the SiC substrate and the oxygen permeable insulating film by thermal oxidation after the deposition of the oxygen permeable insulating film. To do.

[0046]
According to a ninth aspect of the present invention, in the method of manufacturing an ohmic electrode structure according to any one of the sixth to eighth aspects, the step of forming the mask material is a step of applying a photoresist. Use as a summary.

[0047]
According to a tenth aspect of the invention, in the method of manufacturing the ohmic electrode structure according to the ninth aspect, in the step of forming the opening in the field insulating film, a step immediately before the surface of the n-type SiC region is exposed. Is to be completed by wet etching and rinsing with ultrapure water.

[0048]

The invention according to claim 11 is the method for manufacturing an ohmic electrode structure according to any one of claims 6 to 10, wherein the thickness of the first conductor film is 1 / th of the thickness of the n-type SiC region. The point is that it is thinner than 2.

According to the eleventh aspect of the present invention, the thickness of the element of the first conductor film before forming the heating reaction layer is less than 1/2 of the thickness of the n-type SiC region below the element. Since it is set in advance, even if the element of the first conductor film is completely converted into the heating reaction layer by the heat treatment of

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the SiC substrate, the n-type SiC region does not disappear.

[0049]

According to the twelfth aspect of the present invention, in the method for producing an ohmic electrode structure according to any one of the sixth to eleventh aspects, the step of forming the heated reaction layer includes oxygen (O2) and water (H2O). The gist is that the SiC substrate is heat-treated in a non-oxidizing atmosphere having a partial pressure of 1×10^{-3} Pa to 1×10^{-10} Pa.

According to the invention of claim 12, heat treatment is performed in a non-oxidizing atmosphere in which the partial pressures of oxygen and water are both controlled to 1×10^{-3} Pa to 1×10^{-10} Pa to form a heated reaction layer. Therefore, it is possible to prevent the oxide film from being formed on the surface of the element of the first conductor film by the high temperature heat treatment for forming the heating reaction layer.

[0050]

According to a thirteenth aspect of the present invention, in the method of manufacturing an ohmic electrode structure according to any one of the sixth to eleventh aspects, the element of the first conductor film is in contact with the opening of the field insulating film. The gist further includes the step of forming a second conductor film on the field insulating film so as to cover the portion.

[0051]

According to a fourteenth aspect of the present invention, in the method for manufacturing an ohmic electrode structure according to the thirteenth aspect, the ohmic electrode structure is formed on the surface of the element of the first conductor film immediately before forming the second conductor film. The gist is that a step of removing the oxide film or the attached hydro carbon is added.

[0052]

According to a fifteenth aspect of the present invention, (a) a SiC substrate, (b) a main electrode region consisting of an n-type SiC region selectively formed on the surface of the SiC substrate,

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and (c) a SiC substrate. And (d) inside the field insulating film and the opening formed in the field insulating film so as to expose the surface of the main electrode region. (E) Inside the opening of the (f) field insulating film, a heating reaction layer disposed at a constant gap from the field insulating film and between the electrode film and the main electrode region, and (f) field insulating The gist of the present invention is to provide a semiconductor device including a main electrode wiring which is in contact with a surface of an electrode film and extends to an upper portion of a field insulating film inside an opening of the film.

In the invention of claim 15, the “main electrode region” is at least one of semiconductor regions located at both ends of the main current path of the semiconductor device and facing each other.

According to the invention of claim 15, both the electrode film and the heating reaction layer forming the ohmic electrode with respect to the main electrode region are arranged inside the opening of the field insulating film with a certain gap from the field insulating film. Therefore, the metal material forming the electrode film and the heating reaction layer can be prevented from reacting with the field insulating film.

Further, it is possible to avoid the formation of parasitic Schottky junction due to the ternary coexistence reaction of metal-SiC-SiO2 at the bottom outer edge of the ohmic electrode.

As described in claim 1, the “main electrode region composed of the n-type SiC region selectively formed on the surface of the SiC substrate” defined in claim 15 is the n-type SiC region directly on the surface of the SiC substrate. It is not limited to the case where the main electrode region made of is formed.

For example, another semiconductor region may be arranged in a well shape on a part of the surface of the SiC substrate, and the main electrode region may be formed inside the well-shaped semiconductor region.

Alternatively, the case where another semiconductor region is epitaxially grown on the entire surface of the SiC substrate and the main electrode region is formed on a part of the surface of the epitaxially grown semiconductor region is also allowed.

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[0053]
According to a sixteenth aspect of the present invention, in the semiconductor device according to the fifteenth aspect, the constant gap is smaller than the thickness of the field insulating film.

[0054]

According to a seventeenth aspect of the invention, (a) a step of forming a main electrode region composed of a high impurity density n-type SiC region on at least a part of the surface of the SiC substrate; A step of cleaning, (c) a step of covering the surface of the SiC substrate with a field insulating film, (d) a step of forming a mask material having an etching rate different from that of the field insulating film on the field insulating film,) A step of forming a window portion on the mask material to form a mask pattern, and (f) a step of etching the field insulating film using the mask pattern until the surface of the main electrode region is exposed to form an opening portion, G) After the surface of the main electrode region is exposed, the field insulating film is further over-etched to form an undercut portion under the mask material near the window, and (h) the upper portion of the mask material and the inside of the opening. The step of depositing the first conductor film on the surface of the main electrode region of (1), and (i) the removal of the mask material allows the surface of the main electrode region inside the opening to have a constant gap with the field insulating film. And a heating reaction layer of the first conductor film segment and the main electrode region by heat-treating the SiC substrate in a non-oxidizing atmosphere. The method is a method for manufacturing a semiconductor device, the method including the steps of:

The "main electrode region" of the invention of claim 17 is, as defined in the invention of claim 15, a semiconductor region located at both ends of the main current path of the semiconductor device.

According to the seventeenth aspect of the present invention, when the ohmic electrode for the main electrode region of the semiconductor device is formed, by controlling the etching amount of over-etching (slight etching) of the field insulating film, the mask material near the window portion The depth of the undercut portion formed at the bottom can be controlled.

Further, the depth of the undercut portion can determine a constant gap between the element of the first conductor film and the field insulating film in a self-aligned manner.

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Similarly to claim 15, the “step of forming a main electrode region made of an n-type SiC region having a high impurity density on at least a part of the surface of the SiC substrate” defined in claim 17 is performed directly on the surface of the SiC substrate. The present invention is not limited to the case of forming the main electrode region including the n-type SiC region.

For example, another semiconductor region may be formed in a well shape on a part of the surface of the SiC substrate, and the main electrode region may be formed inside the well-shaped semiconductor region.

Alternatively, a step of epitaxially growing another semiconductor region on the entire surface of the SiC substrate and forming a main electrode region on a part of the surface of the semiconductor region may be used.

[0055]
According to an eighteenth aspect of the present invention, in the method of manufacturing a semiconductor device according to the seventeenth aspect, the step of covering with the field insulating film comprises a step of growing a thermal oxide film on the surface of the SiC substrate by thermal oxidation. The gist is that it comprises a step of depositing an insulating film on the thermal oxide film by a method other than thermal oxidation.

[0056]
The invention according to claim 19 is the method for manufacturing a semiconductor device according to claim 18, further comprising a step of forming a gate electrode on the thermal oxide film after the step of growing the thermal oxide film. Is the gist.

[0057]
According to a twentieth aspect of the invention, in the method of manufacturing a semiconductor device according to any one of the seventeenth to nineteenth aspects, the thickness of the first conductor film is smaller than ½ of the thickness of the main electrode region. That is the summary.

[0058]

According to the first aspect of the invention, the metal material forming the electrode film and

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the heating reaction layer is prevented from reacting with the field insulating film, and is present on the contact surface with the metal material. Since the field insulating film is not reduced (eroded) by the high temperature heat treatment, the insulating property of the field insulating film can be maintained.

Further, since the metal material forming the electrode film is not in contact with the field insulating film, the problem that the adhesive force between the electrode film and the field insulating film is weak does not originally exist.

Therefore, the electrode film is not peeled off after the manufacturing process is completed, and the manufacturing yield is increased.

Further, it is possible to avoid the formation of parasitic Schottky junction due to the ternary coexistence reaction of metal-SiC-SiO2 at the outer peripheral portion of the bottom of the heating reaction layer, so that a low contact resistance can be achieved.

Further, there is no hindrance to the horizontal current flow in the n-type SiC region due to the formation of the parasitic Schottky junction.

[0059]
According to the second aspect of the present invention, the gap between the peripheral edge of the electrode film and the heating reaction layer and the side wall of the opening is set to a fine dimension smaller than the thickness of the field insulating film. The occupied area can be reduced.

[0060]

According to the third aspect of the present invention, the SiC oxide film is provided under the field insulating film.

The thermal oxide film of SiC is a silicon oxide film (SiO2 film) close to the thermal oxide film of Si, has few interface states with SiC, and can maintain high dielectric breakdown field strength.

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Further, since the thermal oxide film has a laminated structure of an upper insulating film made of an insulating film having a different composition or density and a thermal oxide film, the thickness of the thermal oxide film can be set thin.

Therefore, there is no reduction in surface morphology due to excessive thermal oxidation.

Good surface morphology ensures good metal-semiconductor bonding.

Therefore, generation of a parasitic transistor due to the interface state is suppressed, and an ohmic electrode structure having a low contact resistance can be formed in the highly reliable opening of the field insulating film.

[0061]

The dielectric breakdown field strength of the thermal oxide film of SiC is about 14 MV / cm at a thickness of 10 nm.

The dielectric breakdown field strength of the SiO2 film formed by a method other than thermal oxidation is smaller than this value.

That is, according to the invention of claim 4, various insulating films other than the thermal oxide film of SiC are formed on the thermal oxide film of SiC to secure the breakdown voltage required for the specifications of the semiconductor device. At the same time, the ohmic electrode structure can be formed in the opening of the field insulating film having a low interface state and a good surface morphology.

[0062]

As described above, since the SiC thermal oxide film is a SiO2 film close to the Si thermal oxide film, the etching rate for the BHF solution is about 100 nm / min.

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In comparison, the etching rate for the SiO2 film deposited by CVD is 1.5 to 3 times higher.

That is, according to the invention described in claim 5, since various SiO2 films other than the thermal oxide film of SiC are formed on the thermal oxide film of SiC, the required breakdown voltage, low interface state, A desired ohmic electrode structure can be formed in the opening of the field insulating film having surface stability and good surface morphology. Further, since various semiconductor processes can be adopted by utilizing the difference in etching rate with respect to the BHF solution, various ohmic electrode structures can be constructed.

[0063]

According to the sixth aspect of the invention, the depth of the undercut portion formed under the mask material in the vicinity of the window portion can be controlled by controlling the etching time for overetching the field insulating film. Easy to control. Further, since the constant gap between the element of the first conductor film and the field insulating film can be determined in a self-aligned manner by the depth of the undercut portion, the element of the first conductor film and the field insulating film can be separated from each other. No photolithography step is needed to control the constant gap of the. Therefore, the distance between the elemental piece of the first conductor film serving as the electrode film and the side wall of the opening of the field insulating film can be made sufficiently small, and an ohmic electrode structure having a small occupied area and a fine dimension can be manufactured. Further, since the photolithography process can be omitted, the number of processes is reduced and the manufacturing yield is increased. Furthermore, the invention according to claim 6 is easy and highly reliable because a standard Si semiconductor device manufacturing method can be applied. Further, since it is possible to prevent the element of the first conductor film from reacting with the field insulating film, the field insulating film on the contact surface with the metal material forming the element of the first conductor film is subjected to the high temperature heat treatment. The insulating property of the field insulating film can be maintained without being reduced (eroded). Further, since the metal material forming the first conductor film element is not in contact with the field insulating film, the adhesive force between the electrode film generated from the first conductor film element and the field insulating film is weak. Does not exist by nature. Therefore, the electrode film is not peeled off after the process is completed, and the manufacturing yield is increased. Furthermore, in the step of generating the heating reaction layer, there is no state in which the ternary system of metal-SiC-SiO2 coexists at the bottom outer edge portion of the element of the first conductor film, and therefore, the parasitic state due to the reaction of the ternary system does Generation of Schottky junction can be avoided and low contact resistance can be achieved. Further, there is no hindrance to the

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horizontal current flow in the n-type SiC region due to the formation of the parasitic Schottky junction.

[0064]

According to the invention of claim 7, in the step of forming the field insulating film on the surface of the SiC substrate, the surface of the SiC is thinly thermally oxidized, and then the upper portion of the thermal oxide film is thickened by a method other than thermal oxidation. Since it is achieved by depositing an insulating film, the surface morphology of SiC is not damaged by excessive thermal oxidation. In addition to the thermal oxidation, well-known physical or chemical means such as a CVD method or a sputtering method can be adopted. However, a natural oxide film or hydrocarbons unique to these methods other than the thermal oxidation can be used. Generation at the SiC interface (surface) can be effectively removed or suppressed by thermal oxidation. That is, since it is possible to remove the natural oxide film on the SiC surface and the hydrocarbons which hinder the formation of the heating reaction layer, it is possible to easily realize a contact resistance as low as about $10^{-7}\ \Omega\mathrm{cm}^2$.

[0065]

According to the invention described in claim 8, the step of depositing the oxygen permeable insulating film on the surface of the SiC substrate by a method other than thermal oxidation is performed first, and after the oxygen permeable insulating film is deposited, thermal oxidation is performed. Thus, a thermal oxide film is grown on the interface between the surface of the SiC substrate and the oxygen permeable insulating film to form a field insulating film. Also in this case, similarly to the invention according to claim 7, deterioration of the surface morphology of the SiC substrate due to excessive thermal oxidation can be suppressed. Further, the formation of a natural oxide film or hydro carbon unique to well-known physical or chemical means such as a CVD method or a sputtering method can be effectively removed or suppressed by the formation of a thermal oxide film. Therefore, the morphology of the interface between the heated reaction layer and the n-type SiC region is improved, and a uniform and homogeneous heated reaction layer can be generated. Therefore, it is possible to easily obtain a contact resistance ρc as low as about $10^{-7}\ \Omega\mathrm{cm}^2$.

[0066]

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According to the invention described in claim 9, since a well-known photoresist can be used in the semiconductor manufacturing process, a mask pattern for forming an opening in the field insulating film can be easily formed in the photolithography process. I can. Further, by using this mask pattern as it is, if the first conductor film is deposited on the photoresist, the photoresist can be easily removed by a peeling agent or the like, so that the lift-off process can be easily performed.

[0067]

According to the tenth aspect of the invention, the final step in which the bottom of the opening (recess) provided in the field insulating film reaches the surface of the n-type SiC region is the wet etching and the rinse with ultrapure water. As a result, it is possible to prevent re-adhesion of hydrocarbon, which is a reaction product of dry etching, to the surface of the n-type SiC region and etching damage due to excessive plasma energy. Therefore, contamination of the surface of the n-type SiC region exposed in the opening and roughening of the surface of the n-type SiC region can be effectively prevented. In addition, since dry etching can be used, an ohmic contact having a fine opening size can be formed. Therefore, it is possible to manufacture the ohmic electrode structure suitable for increasing the integration density of the semiconductor integrated circuit and reducing the on-resistance of the power semiconductor device.

[0068]

According to the eleventh aspect of the present invention, since the thickness of the elemental piece of the first conductor film before the formation of the heating reaction layer is controlled, the elemental piece of the first conductor film is completely removed. Even if it is converted into the heating reaction layer, it is possible to reliably prevent the n-type SiC region from disappearing and the heating reaction layer from penetrating the n-type SiC region. Therefore, it is possible to effectively prevent a sudden increase in contact resistance due to disappearance of the n-type SiC region and an increase in leak current due to penetration of the n-type SiC region. Further, the process margin of the heat treatment step of the SiC substrate for forming the heating reaction layer can be sufficiently secured, sufficient heat treatment can be performed, and lower contact resistance can be realized.

[0069]

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According to the twelfth aspect of the present invention, since the heating reaction layer is formed by heat treatment in a non-oxidizing atmosphere in which the partial pressures of oxygen and water are controlled, a high temperature for forming the heating reaction layer is obtained. It is possible to prevent an oxide film from being formed on the surface of the element of the first conductor film by the heat treatment. Therefore, it is possible to reduce the contact resistance between the electrode film formed of the pieces of the first conductor film and the upper second conductor film connected to the electrode film. Furthermore, by heat-treating in a non-oxidizing atmosphere in which the partial pressure of oxygen and water is controlled, during the high-temperature heat treatment, the roughness of the surface of the segment of the first conductor film caused by the oxygen or the oxygen-containing atmosphere is caused. It can be prevented. For this reason, since the surface morphology of the alignment mark formed by the similar process and structure is also good, highly accurate photolithography and etching can be performed in the subsequent process.

[0070]

According to the thirteenth aspect of the present invention, the second conductor film is arranged so as to contact the element of the first conductor film and cover the opening of the field insulating film. Since the conductor pieces can be formed, the ohmic electrode structure corresponding to the actual electrode structure of the semiconductor device can be easily manufactured. Further, since the high temperature heat treatment is not necessary for the second conductor film, the field insulating film on the contact surface with the material forming the second conductor film is reduced (eroded) by the high temperature heat treatment. Since it does not exist, the insulating property of the field insulating film can be maintained.

[0071]

According to the fourteenth aspect of the present invention, even if an oxide film is formed on the surface of the first conductor film element by the high temperature heat treatment or hydro carbon is attached, these Can effectively remove the oxide film and hydro carbon. For this reason, it is possible to avoid an increase in contact resistance between the first conductor film element and the second conductor film element due to the oxide film on the surface of the first conductor film element or hydrocarbon.

[0072]

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According to the fifteenth aspect of the invention, in the ohmic electrode for the main electrode region of the semiconductor device, the metal material forming the electrode film of the ohmic electrode and the heating reaction layer does not react with the field insulating film. Therefore, the field insulating film on the contact surface with the metal material is not reduced (eroded) by the high temperature heat treatment. Therefore, the high insulation of the field insulating film formed around the main electrode region of the semiconductor device can be maintained, and the leak current can be reduced. Further, since the metal material forming the electrode film is not in contact with the field insulating film, the problem that the adhesive force between the electrode film of the ohmic electrode and the field insulating film is weak does not originally exist. Therefore, the electrode film of the ohmic electrode is not peeled off after the manufacturing process of the semiconductor device is completed, and the manufacturing yield of the semiconductor device is increased. Furthermore, the formation of parasitic Schottky junction due to the ternary coexistence reaction of metal-SiC-SiO2 at the outer peripheral portion of the bottom of the ohmic electrode can be avoided, so that an ohmic electrode with low contact resistance can be achieved. Further, there is no hindrance to the flow of current in the horizontal direction in the main electrode region due to the formation of the parasitic Schottky junction. As a result, a semiconductor device having a high breakdown voltage and capable of operating at high speed can be realized. Particularly, in a power semiconductor device, low on-resistance and high-speed switching can be achieved at the same time.

[0073]

According to the sixteenth aspect of the present invention, the gap between the peripheral edge of the electrode film and the heating reaction layer and the side wall of the opening is set to a fine dimension smaller than the thickness of the field insulating film. The area occupied by the electrodes can be reduced, and the integration density of semiconductor devices can be improved. In particular, by arranging a large number of ohmic electrodes having a fine structure, it is possible to simultaneously achieve low on-resistance and high-speed switching of the power semiconductor device.

[0074]

According to the seventeenth aspect of the invention, when the contact hole for forming the ohmic electrode for the main electrode region of the semiconductor device is formed, the window portion is controlled by controlling the etching time for over-etching the field insulating film. Since the depth of the undercut portion formed under the neighboring mask material can be

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controlled, dimensional control is easy. Further, the depth of the undercut portion can determine the constant gap between the field insulating film and the element of the first conductor film for forming the ohmic electrode in a self-aligned manner. There is no need for a photolithography process to control a constant gap between and. Therefore, the distance between the element of the first conductor film, which serves as the ohmic electrode, and the side wall of the opening of the field insulating film can be made sufficiently small, and the ohmic electrode having a small occupied area and fine dimensions can be arranged. Furthermore, since the photolithography step can be omitted, the number of steps involved in forming the ohmic electrode for the main electrode region of the semiconductor device is reduced, and the manufacturing yield of the semiconductor device is increased. Furthermore, the invention according to claim 17 is easy and highly reliable because a standard Si semiconductor device manufacturing method can be applied. Further, since it is possible to prevent the element of the first conductor film from reacting with the field insulating film, the field insulating film on the contact surface with the metal material forming the element of the first conductor film is subjected to the high temperature heat treatment. The insulating property of the field insulating film can be maintained without being reduced (eroded). Further, since the metal material forming the ohmic electrode is not in contact with the field insulating film, there is an inherent problem that the adhesive force between the ohmic electrode and the field insulating film generated from the element of the first conductor film is weak. do not do. For this reason, the ohmic electrode is not peeled off after the process is completed, and the manufacturing yield is increased. Further, in the step of forming the heated reaction layer of the ohmic electrode, since there is no coexisting state of the metal-SiC-SiO2 ternary system at the bottom outer edge portion of the ohmic electrode, parasitic Schottky junction due to reaction of the ternary system is present. It is also possible to avoid the generation of, and low contact resistance can be achieved. Further, it is possible to easily manufacture a semiconductor device having good characteristics, which does not hinder the horizontal current flow in the main electrode region due to the formation of the parasitic Schottky junction. Further, since the ohmic electrode structure manufacturing method according to the seventeenth aspect uses the so-called “lift-off method” for patterning, it has a feature that any kind of first conductor film can be patterned.

[0075]

According to the eighteenth aspect of the present invention, in the step of forming the field insulating film on the surface of the SiC substrate, the surface of the SiC is thinly thermally oxidized, and then the upper portion of the thermal oxide film is thickened by a method other than thermal oxidation. Since it is achieved by depositing an insulating film, the surface morphology of SiC is not damaged by excessive thermal oxidation. In addition to the thermal oxidation, well-known physical or chemical means such as a CVD method or a sputtering method can be adopted. However, a natural oxide film or hydrocarbons unique to these methods other

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than the thermal oxidation can be used. Generation at the SiC interface (surface) can be effectively removed or suppressed by thermal oxidation. In other words, since it is possible to remove the natural oxide film on the SiC surface and the hydrocarbons which hinder the formation of the heating reaction layer, a semiconductor device having an ohmic electrode with a low contact resistance of about $10^{-7}\ \Omega\text{cm}^2$ can be easily formed. Can be realized.

[0076]
According to the nineteenth aspect of the invention, since the gate electrode is formed on the thermal oxide film having a small number of interface states, the gate threshold value control is easy, and a high-speed and high-breakdown-voltage semiconductor device is simple. Can be manufactured.

[0077]

According to the twentieth aspect of the invention, since the thickness of the piece of the first conductor film before the formation of the heating reaction layer of the ohmic electrode is controlled, the piece of the first conductor film is temporarily assumed. However, even if it is completely converted into the heating reaction layer, it is possible to reliably prevent the main electrode region from disappearing and the heating reaction layer from penetrating the main electrode region.

Therefore, it is possible to effectively prevent a sudden increase in contact resistance due to the disappearance of the main electrode region and an increase in leak current due to penetration of the main electrode region. Furthermore, a semiconductor device having an ohmic electrode with a very low contact resistance can be realized because a sufficient process margin can be secured in the heat treatment step of the SiC substrate for forming the heated reaction layer of the ohmic electrode, sufficient heat treatment is possible.

[0078]

DESCRIPTION OF THE PREFERRED EMBODIMENTS Next, first to third embodiments of the present invention will be described with reference to the drawings. In the following description of the drawings, the same or similar reference numerals are given to the same or similar parts. However, it should be noted that the drawings are schematic and the relationship between the thickness and the plane dimension, the thickness ratio of each layer, and the like are different

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from the actual ones. Therefore, specific thicknesses and dimensions should be determined in consideration of the following description. Further, it is needless to say that the drawings include portions having different dimensional relationships and ratios.

[0079]

(First Embodiment) As shown in FIG. 1, the ohmic electrode structure according to the first embodiment of the present invention is selectively formed on the surfaces of the SiC substrate 1 and the SiC substrate 1. The n-type SiC region 32, the field insulating film 5 placed on the SiC substrate 1, and the opening (contact window) opened to expose the surface of the n-type SiC region 32 in the field insulating film 5. Inside the opening of the electrode film 7 and the field insulating film 5, which are arranged inside the field insulating film 5 with a constant gap (side wall gap) 77, the side wall gap 77 is separated from the field insulating film 5 and the electrode The heating reaction layer 8 disposed between the film 7 and the n-type SiC region 32 was in contact with the surface of the electrode film 7 inside the opening of the field insulating film 5, and extended to the upper part of the field insulating film 5. It is composed of a wiring conductor element 9. The heating reaction layer 8 embedded between the electrode film 7 and the n-type SiC region 32 was formed by a heating reaction between the n-type SiC region 32 and the first conductor film that is the base material of the electrode film 7. It is a layer. The constant gap forming the side wall gap 77 is controlled to a value smaller than the thickness of the field insulating film 5.

[0080]

The n-type SiC region 32 has a high surface electron density. For example, the surface electron density of the n-type SiC region 32 is at least 1 × 1018 / cm3 to 2 × 1021 / cm3, preferably 1 × 1019 / cm3 to 8 × 1020 / cm3. The conductivity type of the SiC substrate 1 differs depending on the semiconductor device using the present ohmic electrode structure. For example, p-type for MOSFET and n-type for MESFET or Schottky barrier diode may be selected according to the design specifications.

[0081]

The first conductor film, which is the base material of the electrode film 7, is not only Ni but also titanium (Ti), chromium (Cr), tantalum (Ta), tungsten (W), molybdenum (Mo), etc. 1, or 1. It is

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composed of a metal film, an alloy film, a compound film, or a composite film or a laminated film thereof selected from the above metals. It is desirable that the thickness of this electrode film 7 be a value less than approximately 1/2 of the diffusion depth of the n-type SiC region 32.

[0082]

To the electrode film 7, a wiring conductor piece 9 made of a second conductor film for connecting to an ohmic electrode at another portion is connected. The wiring conductor piece 9 is arranged so as to cover the opening of the field insulating film 5. The wiring conductor piece 9 is a wiring member that connects the ohmic contact shown in FIG. 1 to another portion, and functions as a main electrode wiring of the semiconductor device. In the power device, a plurality of unit cells are arranged on the SiC substrate 1 in a honeycomb shape, a matrix shape or the like to secure a current capacity. In addition, each main electrode region may be subdivided and arranged on the SiC substrate 1 at a high density depending on the design specifications for lowering the ON voltage. Therefore, in such a case, the wiring conductor piece 9 functions as a wiring that integrates the respective main electrode regions of the unit cells divided into a plurality. The wiring conductor piece 9 includes well-known aluminum (Al), aluminum-silicon (Al-Si) eutectic, aluminum-copper-silicon (Al-Cu-Si) eutectic, copper (Cu), titanium-tungsten. A (Ti-W) alloy or the like is used.

[0083]

The field insulating film 5 is composed of a laminated insulating film of a thermal oxide film 3 of the SiC substrate 1 and an upper insulating film 4 made of an insulating film having a composition or density different from that of the thermal oxide film 3. In the ohmic electrode structure according to the first embodiment, the "insulating film having a composition different from that of the thermal oxide film 3" means PSG (phosphosilicate glass) film, BSG (borosilicate glass), BPSG (borophosphosilicate). It means an insulating film such as glass) or a Si3N4 film. The "insulating film having a density different from that of the thermal oxide film 3" means an insulating film such as a SiO2 film deposited by a method other than the thermal oxide film. For example, a SiO2 film formed by a chemical or physical deposition method such as a CVD method, a sputtering method, or a vacuum deposition method is applicable. The SiC thermal oxide film 3 shown in FIG. 1 is a SiO2 film that is inferior to the Si thermal oxide film but is close to the Si thermal oxide film. Since the thermal oxide film and the SiO2 film deposited by another method have different densities, the boundaries can be seen by observing the cross section with high resolution SEM.

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[0084]

The dielectric breakdown field strength of the SiC thermal oxide film 3 close to the Si thermal oxide film is about 14 MV / cm at a thickness of 10 nm. On the other hand, the dielectric breakdown field strength of the SiO2 film formed by a method other than thermal oxidation is smaller than this value. For example, the insulation breakdown electric field strength of the SiO2 film deposited by CVD is about 6 MV / cm at the same thickness of 10 nm. Therefore, if the insulation breakdown electric field strength is measured, the thermal oxide film 3 of SiC and the upper insulation film 4 can be clearly seen. Can be distinguished from.

[0085]

Further, since the SiC thermal oxide film 3 is a SiO2 film close to the Si thermal oxide film, the etching rate for the BHF solution is about 100 nm / min. In comparison, the etching rate for the SiO2 film deposited by CVD is 1.5 to 3 times higher. Therefore, the thermal oxide film 3 of SiC and the upper insulating film 4 can be clearly distinguished by measuring the etching rate for the BHF solution.

[0086]

Microscopically, since there are more hydrogen and carbon bonds in the SiO2 film deposited by CVD than the thermal oxide film 3 of SiC and the Si--O--Si bond distance is longer than that of the thermal oxide film 3 of SiC, infrared rays are used. The thermal oxide film 3 of SiC and the upper insulating film 4 can be clearly distinguished by the absorption spectrum and Raman spectroscopy.

[0087]

If a laminated structure in which an upper insulating film 4 such as various SiO 2 films other than the SiC thermal oxide film as shown in FIG. The surface morphology of SiC can be favorably maintained while securing the interface state, withstand voltage, and surface stability required as.

[0088]

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The thickness of the thermal oxide film 3 is preferably 2 to 50 nm.

Particularly, the thickness of the thermal oxide film 3 in the range of 5 to 20 nm is desirable.

If the thickness of the thermal oxide film 3 is thinner than 5 nm, the effect of removing the damaged region on the surface of the SiC substrate 1 caused by the surface polishing or the ion implantation method and the effect of removing the foreign matter on the surface become poor. On the other hand, when the thickness of the thermal oxide film 3 is thicker than 50 nm, there is a problem that the surface of the SiC substrate 1 is gradually roughened due to excessive thermal oxidation and the surface morphology is deteriorated. Therefore, in order to reduce the contact resistance ρc, the thickness of the thermal oxide film 3 within the above range brings a beneficial effect.

[0089]

The total thickness of the field insulating film 5, which is the sum of the thickness of the thermal oxide film 3 and the thickness of the upper insulating film 4, is preferably 100 nm to 3 μm. Particularly, it is desirable that the thickness is 300 nm or more. Further, if it is a high breakdown voltage power semiconductor device, it may be set to 800 nm or more. However, if the field insulating film 5 becomes too thick, cracks and the like will occur, so 3 μm or more is not preferable. Further, the gap (side wall gap) 77 between the peripheral edge of the electrode film 7 and the heating reaction layer 8 and the side wall of the opening can be controlled to about the thickness of the field insulating film 5. It is not preferable that 5 is too thick. That is, considering the miniaturization, about 1.5 μm is a practical upper limit of the thickness of the field insulating film 5.

[0090]

As shown in FIG. 1, according to the ohmic electrode structure of the first embodiment, both the electrode film 7 and the heating reaction layer 8 are subjected to field insulation inside the opening of the field insulation film 5. The metal material forming the electrode film 7 and the heating reaction layer 8 can be prevented from reacting with the field insulating film 5 because they are arranged with a constant gap (side wall gap) 77 from the film 5. Therefore, since the field insulating film 5 on the contact surface with the metal material is not reduced (eroded) by the high temperature heat treatment, the insulating property of the field insulating film 5 can be

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maintained. Further, since the metal material forming the electrode film 7 is not in contact with the field insulating film 5, the problem that the adhesive force between the electrode film 7 and the field insulating film 5 is weak does not originally exist. Therefore, the electrode film 7 is not peeled off after the manufacturing process is completed, and the manufacturing yield is increased. Furthermore, since it is possible to avoid the formation of parasitic Schottky junction due to the ternary coexistence reaction of metal-SiC-SiO2 in the outer peripheral portion of the bottom of the heating reaction layer 8, a low contact resistance can be achieved. Further, there is no hindrance to the horizontal current flow in the n-type SiC region 32 due to the formation of the parasitic Schottky junction.

[0091]
Further, according to the ohmic electrode structure according to the first embodiment, the gap (side wall gap) 77 between the peripheral portions of the electrode film 7 and the heating reaction layer 8 and the side wall of the opening is formed by field insulation. Since the size can be made smaller than the thickness of the film 5, the area occupied by the ohmic electrode structure can be reduced.

[0092]
Next, the manufacturing process of the ohmic electrode structure according to the first embodiment of the present invention will be described with reference to the process cross-sectional views (Nos. 1 to 3) shown in FIGS.

[0093]

(A) First, a SiO 2 film 33 having a thickness of about 1.5 μm is deposited on the entire surface of the 4H—SiC substrate 1 by the CVD method, and a photoresist 34 is spin-coated on it.

Then, as shown in FIG. 2A, the SiO2 film 33 deposited on the n-type SiC region formation-scheduled region is selectively removed by the well-known photolithography method and wet etching technique, and the ion implantation mask film 33 is formed. To form.

[0094]

(B) Then, as shown in FIG. 2B, the ion implantation through film 35 made of a thin SiO 2 film is

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again deposited on the entire surface of the ion implantation mask film 33 by the CVD method.

The ion implantation through film 35 is a film for adjusting a projection range (depth) Rp at the time of ion implantation described later. Under the implantation condition of 31P + (phosphorus ion) described later, the thickness of the ion implantation through film 35 is 20 to 25 nm. After depositing the ion implantation through film 35, n-type impurity ions such as 31P +, 14N + (nitrogen ions) and 75As + (arsenic ions) are deposited on the entire surface of the SiC substrate 1 so that the impurity density of at least the surface of the SiC substrate 1 is 1 × 10 20 /. Ion implantation is performed so that the crystallinity of the SiC substrate 1 is not impaired and the cm3 or more. It is preferable that the n-type impurity ions are implanted in multiple steps into the SiC substrate 1 heated to 500 ° C. while changing the dose amount Φ / acceleration energy EAC. For example, the dose amount Φ / acceleration energy EAC conditions in the case of multi-stage ion implantation of 31P + into the SiC substrate 1 are as follows: first ion implantation Φ = 5 × 10 14 cm −2 / EAC = 40 KeV; second ion Implantation Φ = 5 × 1014 cm −2 / EAC = 70 KeV; Third ion implantation Φ = 1 × 1015 cm −2 / EAC = 100 KeV; Fourth ion implantation Φ = 1 × 1015 cm −2 / EAC = 150 KeV; Fifth ion implantation Φ = 2 × 1015 cm-2 / EAC = 200 KeV; sixth ion implantation Φ = 2 × 1015 cm-2 / EAC = 250 KeV.

[0095]

(C) When the 6-step multi-step ion implantation is completed, the ion implantation mask film 33 and the ion implantation through film 35 are entirely removed with hydrofluoric acid (HF). Then, when rapid heat treatment at 1700 ° C. for 1 minute is performed in an atmospheric pressure Ar atmosphere, the ion-implanted 31P + is activated, and as shown in FIG. 2C, the n-type SiC region 32 having a high impurity density Are selectively formed. The diffusion depth of the n-type SiC region 32 generated under the ion implantation conditions and the activation heat treatment conditions is about 350 nm.

[0096]

(D) Then, the SiC substrate 1 is sufficiently cleaned by using a predetermined cleaning method such as the RCA cleaning method well known in the silicon (Si) process. The RCA cleaning method is a conventional cleaning method of the semiconductor SiC substrate 1 in which the immersion treatment with the H2O2 + NH4OH mixed solution (SC-1) and the H2O2 + HCl mixed solution (SC-2) is combined. Then, as shown in FIG. 3D, the surface of the sufficiently cleaned SiC substrate 1 is thermally oxidized in a dry oxygen atmosphere at 1000 ° C. to 1150 ° C., and a

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thermal oxide film having a thickness of 5 to 40 nm is formed on the surface. Grow three. Note that steam may be used instead of the dry oxygen atmosphere. By thermal oxidation in dry oxygen at a heat treatment temperature of 1150 ° C. for 3 hours, a thermal oxide film 3 having a thickness of 35 to 40 nm is obtained. Thermal oxidation at 1150 ° C. for 2 hours in a wet atmosphere using water vapor gives a thermal oxide film 3 of 30 to 35 nm. In the case of thermal oxidation in a wet atmosphere using water vapor, it is preferable to anneal in argon (Ar) at 1150 ° C. for about 30 minutes thereafter. In order to reduce the thermal oxide film 3 to 20 nm or less, the oxidation temperature may be lowered or the oxidation time may be shortened.

[0097]

(E) Next, as shown in FIG. 3E, an upper insulating film 4 made of PSG of 400 nm is deposited on the thermal oxide film 3 by the atmospheric pressure CVD method to form a two-layer structure. The field insulating film 5 is formed. It is desirable that the total thickness of the field insulating film 5, which is the sum of the thickness of the thermal oxide film 3 and the thickness of the upper insulating film 4, be about 100 nm to 600 nm.

[0098]

(F) Next, a photoresist 22 having a thickness of 1 to 2 μm is applied on the surface of the field acid insulating film 5 as a "mask material" of the present invention by using a spinner. Then, by using a predetermined photomask (reticle), the mask material (photoresist) 22 is selectively exposed and developed to remove the photoresist 22 in a portion corresponding to the opening 6 to form a window portion. Subsequently, using the mask pattern of the photoresist 22 as an etching mask, the SiC substrate 1 is dipped in a BHF solution and wet-etched to form an opening 6 in the field insulating film 5 as shown in FIG. To form. When forming the fine openings 6, dry etching using gas plasma is preferable. For example, various dry etching methods such as reactive ion etching (RIE) method using CHF3 or C2F6 as an etchant and electron cyclotron resonance ion etching (ECR ion etching) can be used. In this case, dry etching is first performed, and after leaving the field insulating film 5 of several tens of nm, switching to wet etching is performed. When the opening 6 is penetrated to the end by dry etching, 1) the surface of the SiC substrate 1 is roughened by plasma damage due to excessive plasma energy, and 2) hydrocarbon which is a reaction product generated by the etching reaction is SiC. The problem of redeposition on the surface of the substrate 1 and contamination of the surface occurs, which is a major obstacle to the uniform formation of a heating reaction layer described later. Further, it results in a dramatic increase in contact resistance ρc, which is not preferable. Whether the opening is performed by the wet etching alone or the combination of the dry etching and the wet etching is

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common to both, the extremely important formation point related to the basis of the present invention is that the wet etching or the dry etching is a little. This is done excessively (over-etching) so that the opening 6 of the field insulating film 5 becomes larger than the opening of the photoresist, resulting in an undercut portion. For example, after the exposure of the surface of the n-type SiC region 32 is confirmed by visual inspection of the etching monitor portion (due to a change in color), overetching may be added for a predetermined time. The amount of over-etching may be controlled by strictly controlling the composition of the etching solution and the solution temperature, and controlling the etching time. By performing such control, the depth of the undercut portion can be easily controlled as long as it is about the thickness (100 nm to 600 nm) of the field insulating film 5.

Alternatively, if an etching monitor having a desired etching thickness is separately prepared and the just etching of the etching monitor is confirmed to finish the etching, the control of 100 nm or less is possible. A surfactant or the like may be added to the etching liquid. Further, in order to precisely control the depth of the undercut portion, etching using gas phase reaction (gas etching) may be used. In the first embodiment, the photoresist 22 is used as the "mask material" of the present invention. However, if the material is not etched during this over-etching, a material other than the photoresist 22 is used as the "mask material" of the present invention. Can be adopted as. That is, the "mask material" of the present invention may be made of a material having an etching rate different from that of the field insulating film 5. Although FIG. 3 (f) exaggerates the steps of the side wall portion due to the difference in etching rate between the thermal oxide film 3 and the upper insulating film 4, as long as the depth of the undercut portion is thin, it is actually shown. The difference in etching depth is not significant.

[0099]

(G) Then, with the photoresist 22 as an etching mask remaining, the BHF solution is completely rinsed (rinsed) with ultrapure water and then dried. Then, the SiC substrate 1 with the resist mask 22 adhered thereon is immediately installed in the chamber of the vacuum vapor deposition apparatus, and immediately evacuated. The time left in the atmosphere from contact window opening etching to evacuation is an extremely important factor for increasing or decreasing the contact resistance ρ c. When left in the air for a long time, a natural oxide film is formed on the surface of the SiC substrate 1 in the opening, or unwanted foreign matter is attached. For this reason, it will be a great obstacle to the uniform formation of a heating reaction layer described later, and the contact resistance ρ c will be dramatically increased. Then, the chamber of the vacuum vapor deposition apparatus is evacuated to a pressure of less than 1.3×10^{-5} Pa by using a turbo molecular pump, a cryopump, etc., and a first surface is formed on the surface of the SiC substrate 1 as shown in FIG. The first conductor film 17 as the conductor

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film of is vapor-deposited. As the first conductor film 17, for example, a Ni film may be electron beam (EB) evaporated. As shown in FIG. 4G, in order to prevent the first conductor film (Ni-based electrode film) 17 from adhering to the side wall of the opening, an orifice or the like is used to improve the directivity of the vapor deposition beam. Let's do it. At this time, as described above, since the opening 6 of the field insulating film 5 is formed to be larger than the opening of the photoresist mask, the first conductive film segment deposited on the bottom of the opening. (Hereinafter, referred to as "first conductor element 27".) Is accurately transferred to the shape of this slightly smaller photoresist mask opening. In this way, a vapor deposition limiting region having a constant distance and a fine dimension is formed between the peripheral edge of the first conductor element 27 and the side wall of the opening of the field insulating film 5. This fine vapor deposition limited area is determined by the depth of the above-mentioned undercut portion, so that it can be precisely controlled by the overetching time of the opening etching. The thickness of the first conductor film 17 is set to be smaller than 1/2 of the diffusion depth of the n-type SiC region 32 located therebelow.

[0100]

(H) After vacuum deposition of the first conductor film (Ni film) 17, the SiC substrate 1 is taken out of the chamber of the vacuum deposition apparatus. Subsequently, a lift-off method is used to obtain a substrate structure in which the first conductor element piece 27 is selectively embedded only inside the opening as shown in FIG. That is, when the SiC substrate 1 is immersed in an organic solvent such as acetone or a dedicated photoresist stripping solution to completely remove the photoresist 22 remaining on the surface of the SiC substrate 1, the first photoresist 22 deposited on the photoresist 22 is removed. Since the first conductor film (Ni film) 17 is also removed together with the photoresist 22, the first conductor piece 27 selectively remains only inside the opening as shown in FIG. 4 (h). As a result, a side wall gap 77 having a fine dimension corresponding to the vapor deposition limited region is formed in a self-aligned manner between the peripheral edge of the first conductor element 27 and the side wall of the opening of the field insulating film 5.

[0101]

(I) After that, when the SiC substrate 1 is subjected to a heat treatment in a non-oxidizing atmosphere at 700 ° C. to 1050 ° C. for a short time (about several minutes), as shown in FIG. The conductor piece 27 of No. 1 and the SiC substrate 1 react with each other to generate the heating reaction layer 8 in the interface region between them, and excellent ohmic characteristics are realized between the heating reaction layer and the n-type SiC region 32. It

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Infrared (IR) lamp heating may be used to perform heat treatment for a short time of about several minutes. Here, the "non-oxidizing atmosphere" is an atmosphere containing no gas of a compound containing oxygen such as oxygen (O2) or water (H2O). Specifically, an ultrahigh-purity inert gas atmosphere such as ultrahigh-purity argon (Ar) or ultrahigh-purity nitrogen (N2), high vacuum, or the like is suitable as the "non-oxidizing atmosphere". If even a small amount of oxygen is contained in these heat treatment atmospheres, metal oxides (= insulators) will be generated on the surface by heat treatment, or the formation of a heating reaction layer will be hindered. Requires strict control. Specifically, the partial pressure of oxygen and water contained in the heat treatment atmosphere is at least about 1 × 10 −3 Pa to 1 × 10 −10 Pa, preferably 1. It is desirable that the pressure is about 10-5 Pa to 1 * 10-10 Pa. When heat treatment is performed in an ultra-high purity inert gas atmosphere, strict control is required such as the use of a deoxidizer or a gas purifier, in addition to baking of gas pipes and inspection of leaks. When heat treatment is performed in a high vacuum, the surface of the metal is oxidized even in a vacuum of about 1 × 10 −8 Pa. Therefore, a partial pressure of oxygen and water is 1 × 10 − by using a cryopanel or the like together. It is preferable to control the heat treatment at about 8 Pa to 1 × 10 −10 Pa and perform the heat treatment under an ultrahigh vacuum. For example, when a Ni film is used as the first conductor film 17, the heat reaction layer 8 composed of nickel silicide (NiSi1-X, NiSi2) and carbon (C) is heat-treated by the heat treatment to form the first conductor element 27. Is generated at the bottom (bottom) of the. The unreacted first conductor piece 27 that has not become the heating reaction layer 8 becomes the electrode film 7. In reality, the electrode film 7 is in a state in which nickel silicide (Ni2Si) is diffused into unreacted Ni. In the step of depositing the first conductor film, the thickness of the first conductor film is set to be smaller than ½ of the thickness of the n-type SiC region 32 located therebelow because the first conductor piece 27 is heat-treated. This is to ensure that the n-type SiC region 32 remains in the lower portion even when it is completely converted into the heated reaction layer 8 in step 1.

When the high-impurity-density n-type SiC region 32 disappears completely, the contact resistance rapidly increases, which is a serious situation. The condition for the thickness of the first conductor film is specified to avoid this situation.

[0102]

(V) After the heating reaction layer 8 is formed, as shown in FIG. 1, a second conductor film such as Al is deposited on the entire surface of the SiC substrate 1. Then, patterning is performed by a photolithography method and an etching technique such as RIE to form the wiring conductor piece 9 as shown in FIG. 1, whereby the ohmic electrode structure according to the first embodiment is completed. When the etchant (= etching liquid or etching gas) during patterning

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attacks the Ni-based electrode film 7, the second conductor film may be arranged so as to cover the Ni-based electrode film 7. ..

[0103]

In the step of forming the heat-reactive layer 9, the oxide of the first conductor film is unintentionally formed on the surface of the electrode film 7 made of the first conductor film. When highly resistive contaminants are attached, a step of removing these foreign substances is added before forming the second conductor film. As a substrate treatment suitable for this purpose, sputter etching using Ar ions is effective for dry treatment. Alternatively, the oxide film such as the first conductor film is removed by immersion in a mixed solution of phosphoric acid (H3PO4): nitric acid (HNO3): acetic acid (CH3COOH) after the step of removing hydrocarbons by exposure to oxygen plasma. A series of wet treatment steps of rinsing with pure water and drying can be used.

[0104]

According to the method of manufacturing the ohmic electrode structure of the first embodiment, the undercut formed under the mask material near the window is controlled by controlling the etching time for overetching the field insulating film 5. Since the depth of the part can be controlled, the size control is easy. In addition, a constant gap (side wall gap) 77 between the first conductor element 27 and the field insulating film 5 can be determined in a self-aligned manner by the depth of the undercut portion. That is, there is an advantage that the electrode pattern of the first conductor element 27 can be formed in a self-aligned manner with respect to the position of the side wall of the opening pattern provided in the field insulating film 5. In other words, since the patterning of the first conductor element 27 is not performed in the photolithography step, the position of the end of the first conductor element 27 is positioned with the utmost precision with respect to the edge of the field insulating film 5. There is an advantage that can be combined. The term "extreme precision" means that if an overetching method is selected, the depth of the undercut can be controlled at the nanometer level, and also at the precision of the molecular layer unit. For example, in a vacuum chamber that can be evacuated to an ultra-high vacuum, if vapor phase etching or the like utilizing surface reaction is adopted, etching can be performed in molecular layer units. Therefore, the distance between the first conductor element 27 serving as the electrode film 7 and the side wall of the opening of the field insulating film 5 can be made sufficiently small, and an ohmic electrode structure having a small occupied area and a fine dimension can be manufactured.

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[0105]

According to the method of manufacturing the ohmic electrode structure of the first embodiment, the photo for controlling the constant gap (side wall gap) 77 between the first conductor element 27 and the field insulating film 5 is used. No lithographic step is required. That is, in a series of steps from the step of forming the opening 6 of the field insulating film 5 to the step of forming the first conductor element 27, photolithography is required only once, and there is an advantage that the process is simplified. If the number of steps is reduced, the production yield is increased, which effectively acts as a reduction in production cost as compared with the conventional example. Furthermore, since a standard Si semiconductor device manufacturing method can be applied, it is possible to provide an easy and highly reliable manufacturing method for the ohmic electrode structure.

[0106]

According to the method of manufacturing the ohmic electrode structure of the first embodiment, it is possible to pattern the first conductor film 17 of any kind and structure. This advantage is particularly utilized when a) when the first conductor film 17 does not have an etchant having a practical etching rate, b) when the first conductor film 17 significantly reacts with oxygen, water, or an etchant. At this time, c) when the first conductor film 17 has a multi-layer structure and etching becomes complicated.

[0107]

Further, according to the method of manufacturing the ohmic electrode structure of the first embodiment, it is possible to prevent the first conductor element 27 from reacting with the field insulating film 5, so that the first conductor The field insulating film 5 on the contact surface with the metal material forming the element 27 is not reduced (eroded) by the high temperature heat treatment, and the insulating property of the field insulating film 5 can be maintained. Further, since the metal material forming the first conductor element 27 is not in contact with the field insulating film 5, the adhesive force between the electrode film 7 generated from the first conductor element 27 and the field insulating film 5 is weak. The problem does not exist by nature. Therefore, the electrode film 7 is not peeled off after the process is completed, and the manufacturing yield is increased. Furthermore, in the step of producing the heating reaction layer 8, there is no state in which the ternary system of metal-SiC-SiO2 coexists in the outer

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peripheral portion of the bottom of the first conductor element 27, so that there is no parasitic state due to the reaction of the ternary system. Generation of Schottky junction can be avoided and low contact resistance can be achieved. Further, there is no hindrance to the horizontal current flow in the n-type SiC region 32 due to the formation of the parasitic Schottky junction.

[0108]

In order to confirm whether the ohmic electrode structure for the n-type SiC region 32 manufactured with such a structure exhibits a practical contact resistance, a linear transmission line model (linear TLM) evaluation method often used for evaluating the contact resistance. A contact group was prepared. In this linear TLM evaluation method, a contact group in which electrode patterns (contact patterns) are arranged in a horizontal line inside a rectangular n-type SiC region surrounded by an element isolation region made of a SiO2 film is used. The length of the short side of the n-type SiC region is 208 μm. That is, along the long side direction of the rectangular n-type SiC region, there is prepared a contact group pattern in which a plurality of electrode patterns each of which is a small rectangle whose long side direction is orthogonal to this rectangle are one-dimensionally arranged. The long side (ohmic contact width) of this small rectangle is 200 μm, and the short side is 100 μm. Here, the pattern of the contact group is arranged in a horizontal row along the long side direction of the n-type SiC region while sequentially changing the mutual intervals (contact intervals) of the contacts (metal-semiconductor junction) each having a small rectangular pattern. To be done. That is, the contact distance L is sequentially changed to L = 6, 10, 15, 20, 25, 30 μm. In the linear TLM evaluation method, the resistance is obtained from the current-voltage characteristics between two adjacent contacts in this contact group, the resistance is arranged as a function of the contact interval, and this is linearly approximated to perform mathematical processing, and finally This is a method for obtaining a precise contact resistance ρc.

[0109]

The main constitutions of the evaluated samples are as follows. The SiC substrate 1 used is a (0001) plane 4H-SiC substrate having a high resistance p-type homoepitaxial film. The surface of this homoepitaxial 4H-SiC substrate is a Si surface. The n-type SiC region 32 having a high impurity density is formed on this homoepitaxial 4H-SiC substrate by ion implantation and activation heat treatment by the method described above. N-type SiC region 3 has a diffusion depth of 350 nm and an impurity density of 2.7 × 1020 cm3. The first conductor film 17 before heat treatment is Ni having a thickness of 150 nm, the thermal oxide film 3 of the field insulating film 5 is a 1100 ° C. dry oxide film (10 nm thick), and the upper insulating film 4 is SiO 2

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formed by atmospheric pressure CVD. It is a film (400 nm thick). The heat treatment temperature of the heating reaction layer 8 is 1000 ° C., the heat treatment time is 5 minutes, and the heat treatment atmosphere is a high-purity Ar atmosphere. The wiring conductor piece 9 made of the second conductor film is an Al film piece having a thickness of 1 μm.

[0110]

FIG. 5 shows current-voltage characteristics between adjacent electrodes using the contact distance as a parameter. Since the straight line passing through the origin is obtained, it can be seen that ohmic contacts are obtained at all the electrodes forming the TLM. FIG. 6 is a plot of the relationship between the resistance between the ohmic contact electrodes and the distance obtained from the slope of the straight line in FIG. The data has little variation and is plotted on one straight line. From this linear approximation, a contact resistance $\rho c = 8.6 \times 10^{-7}$ Ωcm 2 which is a very excellent value can be obtained. For comparison, FIG. 5 also shows the results obtained when the heat treatment temperature of the heated reaction layer 8 was 900 ° C. and other conditions were the same as the case of the heat treatment temperature of 1000 ° C., but the contact resistance $\rho c = 4.0$. It is $\times 10^{-6}$ Ωcm 2, and it is considered that the formation of the heating reaction layer 8 is slightly insufficient as compared with the case where the heat treatment temperature is 1000 ° C.

[0111]
When the same evaluation is performed using the 6H-SiC substrate 1 (Si surface) having a relatively narrow band gap and a small electron affinity, instead of the 4H-SiC substrate 1, $\rho c =$ 4. An even smaller contact resistance of 0.3×10^{-7} Ωcm 2 is realized.

[0112]

When the other conditions are the same and titanium (Ti) having a thickness of 100 nm is used as the first conductor film instead of Ni, a contact resistance of $\rho c = 1.2 \times 10^{-6}$ Ωcm 2 is obtained. ..

When tungsten (W) having a thickness of 150 nm is used as the first conductor film, a contact resistance of 5.5×10^{-6} Ωcm 2 is obtained.

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[0113]

FIG. 7 is a schematic diagram sketching the surface morphology of the electrode film 7 embedded in the contact window opened in the field insulating film 5 by the Nomarski interference microscope. The plane dimension of the electrode film 7 is 20 μm × 20 μm, and a minute side wall gap 77 formed in a self-aligned manner can be observed between the side wall of the opening of the field insulating film 5 and the electrode film 7. FIG. 7A is a schematic view of the surface of the electrode film 7 made of a Ni film without heat treatment, and good surface morphology can be observed. On the other hand, FIGS. 7 (b) and 7 (c) are schematic views sketching the surface of the electrode film 7 when heat-treated at 900 ° C. and 1000 ° C., respectively, in which slight changes in the surface state are observed. Although it is recognized, it can be judged that the surface morphology is good.

[0114]

FIG. 8 is a schematic diagram sketching a cross-sectional TEM image of the ohmic electrode structure according to the first embodiment of the present invention which is heat-treated at 1000 ° C. The TEM observation was performed by irradiating an electron beam with an acceleration voltage of 300 KeV in the [1120] direction. The Ni / SiC interface before the heat treatment has moved to the SiC substrate direction by about 170 nm after the heat treatment. At the interface between the heated reaction layer 8 and the n-type SiC region 32, good surface morphology having excellent interface flatness can be observed.

[0115]

FIG. 9 shows the composition in the thickness direction of the ohmic electrode structure according to the first embodiment obtained by Rutherford backscattering analysis at a scattering angle of 157 ° when 4 He + was irradiated with an accelerating voltage of 3 MeV and an incident angle of 0 ° . It is a figure which shows change. An Al film as the wiring conductor piece 9 can be observed in the uppermost layer. An electrode film 7 having a thickness of about 100 nm is recognized below the wiring conductor piece 9. The electrode film 7 is presumed to be a solid solution of Ni, nickel silicide (Ni2Si) and carbon (C). A heating reaction layer 8 having a thickness of about 300 nm is recognized under the electrode film 7. The heating reaction layer 8 is composed of a nickel silicide (NiSi1-X) layer having a thickness of about 100 nm and a solid solution of nickel silicide (NiSi2) and carbon (C) having a thickness of about 200 nm which are continuously located under the layer. Presumed to be composed of layers.

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[0116]

(Second Embodiment) FIG. 13 is a cross-sectional view of essential parts of an ohmic electrode structure according to a second embodiment of the present invention. This structure is an example in which an ohmic electrode structure is formed in a mesa-shaped high impurity density n-type SiC epitaxial region used in a MESFET or MOSFET having a recessed gate structure.

[0117]

In the ohmic electrode structure according to the second embodiment of the present invention, a mesa-shaped n-type SiC region 2 having a high impurity density is formed on the surface of a desired SiC substrate 1. The surface electron density of the n-type SiC region 2 is at least 1 × 1018 / cm3 to 2 × 1021 / cm3, preferably 1 × 1019 / cm3 to 8 × 1020 / cm3. The n-type SiC region 2 having such a high impurity density may be formed by homo-epitaxial growth by a vapor phase epitaxial growth method or the like in which nitrogen is added in-situ, or 3 iP +, It may be formed by implanting n-type impurity ions such as 14N + or 75As + and then performing activation heat treatment. The conductivity type of SiC substrate 1 differs depending on the semiconductor device using the ohmic electrode structure according to the second embodiment, and is not specified here. In FIG. 13, the parts denoted by the same numbers as in FIG. 1 are the same elements as in FIG. 1, and the description thereof will be simplified or omitted to avoid redundancy.

[0118]

As shown in FIG. 13, according to the ohmic electrode structure according to the second embodiment, both the electrode film 7 and the heating reaction layer 8 are subjected to the field insulation inside the opening of the field insulation film 5. The metal material forming the electrode film 7 and the heating reaction layer 8 can be prevented from reacting with the field insulating film 5 because they are arranged with a constant gap (side wall gap) 77 from the film 5. Therefore, since the field insulating film 5 on the contact surface with the metal material is not reduced (eroded) by the high temperature heat treatment, the insulating property of the field insulating film 5 can be maintained. Moreover, since the metal material forming the electrode film 7 is not in contact with the field insulating film 5, the problem that the adhesive force between the electrode film 7 and the field insulating film 5 is weak does not inherently exist.

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Therefore, the electrode film 7 is not peeled off after the manufacturing process is completed, and the manufacturing yield is increased. Furthermore, since it is possible to avoid the formation of parasitic Schottky junction due to the ternary coexistence reaction of metal-SiC-SiO2 in the outer peripheral portion of the bottom of the heating reaction layer 8, a low contact resistance can be achieved. Further, there is no hindrance to the horizontal current flow in the n-type SiC region 2 due to the formation of the parasitic Schottky junction.

[0119]

Furthermore, according to the ohmic electrode structure of the second embodiment, the gap (side wall gap) 77 between the peripheral edge of the electrode film 7 and the heating reaction layer 8 and the side wall of the opening is formed by field insulation. Since the size can be made smaller than the thickness of the film 5, the area occupied by the ohmic electrode structure can be reduced.

[0120]

Next, the manufacturing process of the ohmic electrode structure according to the second embodiment of the present invention will be described with reference to the process cross-sectional views (No. 1 to No. 3) shown in FIGS.

[0121]

(A) First, N (nitrogen) as an n-type impurity having a high impurity density of 1×10^{19} / cm 3 or more is added to the Si surface of the (0001) surface, 8 ° off 4H—SiC substrate 1. The n-type epitaxial growth layer (n-type SiC region) 20 having a thickness of several 100 nm is epitaxially grown.

Then, a protective oxide film made of a silicon oxide film (SiO2 film) having a thickness of 20 nm is deposited on the n-type epitaxial growth layer (n-type SiC region) 20 by the CVD method.

An Al film having a thickness of 200 nm is further vapor-deposited on the protect oxide film. This Al film / SiO2 film is etched by a well-known etching technique such as a photolithography method and an RIE method, as shown in FIG. 14A, to form an etching mask 21 made of an Al film / SiO2 film corresponding to the n-type SiC region 2. To form.

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[0122]

(B) Next, as shown in FIG. 14B, an unnecessary epitaxial layer is formed by the RIE method using the etching mask 21 made of Al film / SiO 2 film and SF 6 and O 2 as etchant gas. except. Further, thereafter, Al on the etching mask 21 is removed by a mixed solution of sulfuric acid (H2SO4) and hydrogen peroxide (H2O2), and subsequently, a protective oxide film thereunder is removed by a BHF solution to separate the mesa isolated from the element. An n-type SiC region 2 having a structure is formed.

[0123]

(C) Subsequent steps are substantially the same as the steps of FIG. 3 (d) onward of the first embodiment. That is, the SiC substrate 1 is sufficiently cleaned by using a predetermined cleaning method such as the RCA cleaning method. Then, as shown in FIG. 14C, the surface of the sufficiently cleaned SiC substrate 1 is thermally oxidized in a dry oxygen atmosphere at 1000 ° C. to 1150 ° C., and a thermal oxide film having a thickness of 5 to 40 nm is formed on the surface. Grow three. Next, as shown in FIG. 15D, an upper insulating film 4 made of a SiO2 film is deposited on the thermal oxide film 3 by an atmospheric pressure CVD method to form a field insulating film 5 having a two-layer structure. .. It is desirable that the total thickness of the field insulating film 5, which is the sum of the thickness of the thermal oxide film 3 and the thickness of the upper insulating film 4, be about 100 nm to 600 nm.

[0124]

(D) Next, a photoresist 22 having a thickness of 1 to 2 μm is applied as a mask material of the present invention on the surface of the field acid insulating film 5 using a spinner. Then, by using a predetermined photomask (reticle), the photoresist 22 is selectively exposed and developed to remove the mask material (photoresist) 22 in a portion corresponding to the opening 6 to form a window portion. .. Then, using the mask pattern of the photoresist 22 as an etching mask, the SiC substrate 1 is dipped in a BHF solution and wet-etched to form an opening in the field insulating film 5 as shown in FIG. 6 is formed. When forming the fine openings 6, dry etching using gas plasma is preferable. In this case, dry etching is first performed, and after leaving the field insulating film 5 of several tens of nm, switching to wet etching is performed. As described in the first embodiment, the wet etching or the dry etching is performed slightly excessively regardless of whether the wet etching is performed alone or the dry etching and the wet etching are performed. The opening 6 of 5 is larger than the opening of the photoresist so that an undercut

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portion is formed. Similar to the first embodiment, after the exposure of the surface of the n-type SiC region 2 is confirmed by visual inspection of the etching monitor portion, overetching may be added for a predetermined time. In the second embodiment, the photoresist 22 is used as the "mask material" of the present invention. However, if the material is not etched during this over-etching, a material other than the photoresist 22 is used as the "mask material" of the present invention. Of course, it can be adopted as.

[0125]

(E) Then, with the photoresist 22 as the etching mask remaining, the BHF solution is completely rinsed (rinsed) with ultrapure water, and then dried. Then, the SiC substrate 1 with the resist mask 22 adhered thereon is immediately installed in the chamber of the vacuum vapor deposition apparatus, and immediately evacuated. As described in the first embodiment, the time left in the atmosphere from the etching of the contact window opening to evacuation is an extremely important factor for increasing or decreasing the contact resistance ρ c. Therefore, the exposure time to the atmosphere should be as short as possible within 5 minutes. Then, the chamber of the vacuum vapor deposition apparatus is evacuated to a pressure of less than 1.3×10^{-5} Pa by using a turbo molecular pump, a cryopump, etc., and the first surface of the SiC substrate 1 is removed as shown in FIG. The conductor film 17 is deposited. As the first conductor film 17, for example, a Ni film may be deposited. As shown in FIG. 15F, in order to prevent the first conductor film (Ni film) 17 from adhering to the side wall of the opening, a directivity control means such as an orifice is used to direct the vapor deposition beam. It is good to improve the property. At this time, as described above, since the undercut portion is formed so that the opening portion 6 of the field insulating film 5 is larger than the opening portion of the photoresist mask, the first conductor deposited on the bottom portion of the opening portion. The element piece 27 is accurately transferred to the shape of the undercut portion. In this way, a vapor deposition limiting region (side wall gap) 77 having a constant distance and a fine dimension is generated between the peripheral edge of the first conductor element 27 and the side wall of the opening of the field insulating film 5. The minute sidewall gap 77 can be precisely controlled by the over-etching time of the opening etching. The minute sidewall gap 77 can be formed by narrowing it to the thickness of the field insulating film 5 (100 nm to 600 nm). The thickness of the first conductor film 17 is set to be smaller than ½ of the diffusion depth of the n-type SiC region 2 located therebelow.

[0126]

(F) After vacuum deposition of the first conductor film (Ni film) 17, the SiC substrate 1 is taken

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out from the chamber of the vacuum deposition apparatus. Subsequently, a lift-off method is used to obtain a substrate structure in which the Ni-based electrode film 7 is selectively embedded only inside the opening as shown in FIG. That is, when the photoresist 22 is completely removed, the first conductor film (Ni film) 17 deposited on the photoresist 22 is also removed together with the photoresist 22. Therefore, as shown in FIG. The first conductor element piece 27 selectively remains only inside the portion. As a result, a fine side wall gap 77 is formed in a self-aligned manner between the peripheral edge of the first conductor element 27 and the side wall of the opening of the field insulating film 5.

[0127]

(G) Then, when the SiC substrate 1 is heat-treated in a non-oxidizing atmosphere at 700 ° C. to 1050 ° C. for a short time (about several minutes), as shown in FIG. The first conductor element 27 and the SiC substrate 1 react with each other to generate the heated reaction layer 8 in the interface region between them, and an excellent ohmic characteristic is realized between the heated reaction layer and the n-type SiC. .. In order to perform heat treatment for a short time of about several minutes, IR lamp heating may be used. Here, the "non-oxidizing atmosphere" is an atmosphere containing no gas of a compound containing oxygen such as oxygen (O2) or water (H2O) as described in the first embodiment. Strictly speaking, it is preferable to control the partial pressure of oxygen and water to about 1×10^{-8} Pa to 1×10^{-10} Pa and perform the heat treatment. By setting the thickness of the first conductor film to be less than ½ of the thickness of the n-type SiC region 2 located therebelow, the first conductor piece 27 is completely heated by the heat treatment and the reaction layer 8 is heated. It is ensured that the n-type SiC region 2 remains underneath even when it is converted to.

[0128]

(H) After the heating reaction layer 8 is formed, as shown in FIG. 16I, a second conductor film 19 such as Al is deposited on the entire surface of the SiC substrate 1. Then, patterning is performed by a photolithography method and an etching technique such as RIE to form the wiring conductor piece 9 as shown in FIG. 13, whereby the ohmic electrode structure according to the second embodiment of the present invention is completed. .. When the etchant (= etching liquid or etching gas) at the time of patterning attacks the electrode film 7, the second conductor film 19 may be arranged so as to cover the electrode film 7 without fail.

[0129]

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In order to confirm whether the ohmic electrode structure with respect to the n-type SiC region 2 manufactured with such a structure exhibits a practical contact resistance, the contact interval is L = 6, which is the same as in the first embodiment. A linear TLM contact group of 10, 15, 20, 25, 30 μm was prepared. The long side (contact width) and the short side of the rectangle forming the electrode of the ohmic contact are 200 μm and 100 μm, respectively, as in the first embodiment.

[0130]

The main constitutions of the evaluated samples are as follows. The linear TLM contact group was formed on an n-type SiC region having a thickness of 800 nm and an electron density of 1.5 $\times$ 10 19 / cm 2 epitaxially grown on a high-resistance p-type 4H—SiC substrate. The first conductor film is a 50 nm thick Ni film, the thermal oxide film 3 of the field insulating film 5 is a 1100 ° C. dry oxide film (10 nm thick), and the upper insulating film 4 is a SiO2 film (400 nm thick) formed by atmospheric pressure CVD.). The heat treatment temperature, heat treatment time, and heat treatment atmosphere of the heating reaction layer 8 are 1000 ° C. and 2 minutes, respectively, and a high-purity Ar atmosphere is used. The wiring conductor piece 9 made of the second conductor film is an Al film having a thickness of 1 μm.

[0131]

When evaluated by the TLM method as in the first embodiment, a contact resistance ρc = 3.3 $\times$ 10 -6 Ωcm 2 was obtained. When the n-type SiC layer is formed by the same 31P + ion implantation and activation heat treatment (same condition) as in the first embodiment, instead of forming the n-type SiC layer by the high impurity density epitaxial film, other conditions are If they are the same, a contact resistance of 7.4 $\times$ 10 -7 Ωcm 2 that is equal to the ohmic electrode structure using Ni of the first embodiment within the error range is obtained.

[0132]

FIG. 10 is a diagram showing the relationship between the thickness (film thickness) of the Ni film and the surface morphology when the thickness of the Ni film as the first conductor film 17 is changed. In the observation shown in FIG. 10, the heat treatment conditions for the heat

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reaction layer 8 are a heat treatment temperature of 1000 ° C. and a heat treatment time of 2 minutes. The heat treatment atmosphere is a high purity Ar atmosphere. FIG. 10A is a sketch of the surface morphology of the sample before heat treatment with the Ni film having a thickness of 200 nm. FIG. 10B is a sketch of the surface morphology of the sample having a Ni film thickness of 200 nm after the heat treatment. When the Ni film thickness is 200 nm, a decrease in the surface morphology is observed. FIG. 10C shows the surface morphology of a sample having a Ni film thickness of 100 nm when heat-treated, which is better than the film thickness of 200 nm, but a slight decrease in the surface morphology is still observed. .. FIG. 10D and FIG. 10E are surface morphology after heat treatment of the sample when the film thickness of the Ni film is 50 nm and 20 nm, respectively. It can be seen that a good surface morphology that can be applied to the process is obtained.

[0133]

FIG. 11 is a diagram showing the relationship between the thickness of the Ni film as the first conductor film 17 and the contact resistance of the ohmic electrode structure when the thickness of the Ni film is changed. When the film thickness of the Ni film is 200 nm and 100 nm, the contact resistance is almost the same. It can be seen that when the Ni film thickness is 50 nm, a lower contact resistance is obtained than when the Ni film thickness is 200 nm and 100 nm. It is considered that this reflects that the surface morphology of the sample having a Ni film thickness of 50 nm after heat treatment is good. However, an increase in contact resistance is observed in the sample having a Ni film thickness of 20 nm. It seems that the thickness of the heating reaction layer 8 is insufficient. Therefore, the contact resistance is lowest when the film thickness is 50 nm.

[0134]

FIG. 12 is a diagram showing the relationship between the impurity density and the contact resistance of the ohmic electrode structure according to the second embodiment of the present invention, together with the result of the prior art. It can be seen that the contact resistance $\rho c = 3.3 \times 10^{-7}$ Ωcm 2 lower than any of the conventional results can be obtained for the n-type SiC region having the impurity density of 1.5×10^{19} cm 3 obtained by the epitaxial growth. It can be seen that a contact resistance $\rho c = 8.6 \times 10^{-7}$ Ωcm 2 lower than any of the conventional results can be obtained even for the n-type SiC region having an impurity density of 1.5×10^{20} cm 3 obtained by ion implantation. .. As described above, the ohmic electrode structure according to the second embodiment can easily realize a practical contact resistance equal to or lower than the conventional one.

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[0135]
(Third Embodiment) As the "semiconductor device" of the present invention, for example, a diode, an insulated gate bipolar transistor (IGBT), a field effect transistor (FET), a static induction transistor (SIT), a bipolar transistor (It is applicable to various semiconductor electronic devices such as BJT), electrostatic induction thyristor (SI thyristor), and GTO thyristor.

[0136]

Generally, a semiconductor electronic device has a first main electrode region, a second main electrode region and a control electrode.

A main current path is formed between the first main electrode region and the second main electrode region. This main current is controlled by the voltage or current applied to the control electrode. Therefore, the "first main electrode region" means, for example, either the emitter region or the collector region in BJT or IGBT, and the source region or drain region in the insulated gate transistor (IGT) such as MOSFET or MOSSIT. Means either one of The "second main electrode region" means either an emitter region or a collector region that does not become the first main electrode region in the BJT or the IGBT, and a source region or drain that does not become the first main electrode region in the IGT. Means either one of the areas. That is, if the first main electrode region is the emitter region, the second main electrode region is the collector region, and if the first main electrode region is the source region, the second main electrode region is the drain region. Further, it goes without saying that the “control electrode” means the IGBT and the gate electrode of the IGT. Also, in a SiC semiconductor device that does not have a control electrode such as a diode, the first main electrode region and the second main electrode region are similarly defined.

[0137]

FIG. 17 is a cross-sectional view of essential parts of a lateral MOSFET as a semiconductor device according to the third embodiment of the present invention. The semiconductor device (lateral MOSFET) according to the third embodiment is configured by using a p-type SiC substrate 11, and includes an n-type SiC region 2s selectively formed on the surface of the p-type SiC substrate 11. It has one main electrode region (source region) 2s and a second main electrode region (drain region) 2d composed of an n-type SiC region 2s. Further, the gate oxide film 3 is arranged

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on the p-type SiC substrate 11. A gate electrode 63 is arranged on the gate oxide film 3 between the source region 2s and the drain region 2d. An upper insulating film 4 is formed on the gate electrode 63 and on the gate oxide film 3 where the gate electrode 63 is not arranged. The gate oxide film 3 and the upper insulating film 4 form a field insulating film 5.

[0138]

In field insulating film 5, an opening is formed so as to expose the surface of source region 2s, and an opening is formed so as to expose the surface of drain region 2d. Inside each of the openings, the source electrode film 7s and the drain electrode film 7d are arranged with constant gaps (side wall gaps) 77s and 77d from the field insulating film 5. Further, inside the opening above the source region 2s of the field insulating film 5, a constant gap (side wall gap) 77s is separated from the field insulating film 5 and heating is performed between the source electrode film 7s and the source region 2s. The reaction layer 8s is disposed, and a heating reaction is performed between the drain electrode film 7d and the drain region 2d with a constant gap (side wall gap) 77d from the field insulating film 5 inside the opening above the drain region 2d. The layer 8d is arranged. The semiconductor device according to the third embodiment further includes a first portion which is in contact with the surface of the source electrode film 7s and extends to the upper portion of the field insulating film 5 inside the opening above the source region 2s. Inside the main electrode wiring (source wiring) 9s and the opening in the upper part of the drain region 2d, the second main electrode wiring which is in contact with the surface of the drain electrode film 7d and extends to the upper part of the field insulating film 5 (Drain wiring) 9d.

[0139]

Depending on the design of the semiconductor device, the bonding pads (not shown) connected to the respective main electrode regions 2s and 2d through the wiring conductor pieces (main electrode wiring) 9s and 9d are connected to the field insulating film 5. It may be formed on. Similarly, the gate electrode 63 is also connected to the bonding pad via the wiring conductor element. Then, a passivation film made of an oxide film (SiO2), a PSG film, a BPSG film, a nitride film (Si3N4), a polyimide film, or the like may be formed on the wiring conductor pieces and the bonding pads. Then, a plurality of openings (window portions) may be provided in a part of the passivation film so as to expose the plurality of electrode layers, so that bonding can be performed.

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[0140]

According to the semiconductor device of the third embodiment, the ohmic electrode for the source region 2s has a structure in which the metal material forming the source electrode film 7s and the heating reaction layer 8s does not react with the field insulating film 5. Is becoming Similarly, in the ohmic electrode for the drain region 2d, the metal material forming the drain electrode film 7d and the heating reaction layer 8d does not react with the field insulating film 5. Therefore, the field insulating film 5 on the contact surface with the metal material forming the source electrode film 7s and the drain electrode film 7d is not reduced (eroded) by the high temperature heat treatment. Therefore, the high insulating property of the field insulating film 5 formed around the source region 2s and the drain region 2d of the semiconductor device can be maintained, and the leak current can be reduced.

[0141]

Further, since the metal material forming the source electrode film 7s and the drain electrode film 7d is not in contact with the field insulating film 5, the adhesive force between the source electrode film 7s or the drain electrode film 7d and the field insulating film 5 is weak. The problem does not exist by nature. Therefore, the source electrode film 7s or the drain electrode film 7d is not peeled off after the manufacturing process of the semiconductor device is completed, and the manufacturing yield of the semiconductor device is increased.

[0142]

Furthermore, since it is possible to avoid the formation of parasitic Schottky junction due to the ternary coexistence reaction of metal-SiC-SiO2 at the outer peripheral portion of the bottom of the ohmic electrode, the ohmic electrode having a low contact resistance can be used as the source region 2s or the drain region. It can be formed for 2d. Further, there is no obstruction of the horizontal current flow in the source region 2s or the drain region 2d due to the formation of the parasitic Schottky junction. As a result, a semiconductor device having a high breakdown voltage and capable of operating at high speed can be realized. Particularly, in a power semiconductor device, low on-resistance and high-speed switching can be achieved at the same time.

[0143]

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Particularly, the side wall gap 77s between the peripheral edge of the source electrode film 7s and the heating reaction layer 8s and the side wall of the opening, and the side wall gap 77s between the peripheral edge of the drain electrode film 7d and the heating reaction layer 8d and the side wall of the opening. Since the side wall gap 77d can be made smaller than the thickness of the field insulating film 5, the area occupied by the ohmic electrode with respect to the source region 2s and the drain region 2d can be reduced and the integration density of the semiconductor device can be improved.

[0144]
Next, the manufacturing process of the semiconductor device (lateral MOSFET) according to the third embodiment of the present invention will be described with reference to the process cross-sectional views (No. 1 to No. 3) shown in FIGS. ..

[0145]

(A) First, in a step similar to that shown in FIGS. 14A to 14C, 1 × 10 19 with a thickness of several hundreds nm is formed on the surface of the Si surface of the 8 ° -off p-type 4H-SiC substrate 11. An n-type SiC region having a high impurity density of / cm3 or more is epitaxially grown.

Then, by selectively etching the epitaxial growth, the source region 2s and the drain region 2d made of the mesa-shaped n-type SiC regions facing each other are formed.

That is, the source region 2s and the drain region 2 having a convex shape are formed at two different locations on the surface of the SiC substrate 11 with a certain distance therebetween. Although the plan view is omitted, the source region 2s and the drain region 2 are arranged as a pattern of two rectangles (rectangles) whose long sides are parallel to each other. In the case of an integrated circuit, an element isolation region is formed outside the two rectangular (rectangular) pattern regions forming the source region 2s and the drain region 2. Further, a channel stop ion implantation step may be added depending on the device specifications, and in the case of a power device, a guard ring region forming step may be added. After the element isolation region is formed, the SiC substrate 11 is sufficiently cleaned by using a predetermined cleaning method such as a well-known RCA cleaning method, and as shown in FIG. A thermal oxide film 3 as a 40 nm gate oxide film is grown. Thermal oxidation in dry oxygen in an atmosphere of 1150 ° C. for 3 hours gives a thermal oxide film (gate oxide film) 3 having a thickness of 35 to 40 nm. The element isolation region may be formed by a method of filling the

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trench with an insulating film deposited by the CVD method or the like. When the thickness of the gate oxide film 3 is set to 5 to 20 nm, a silicon nitride film (Si3N4 film) having a thickness of 35 to 80 nm is further formed on the gate oxide film 3 by the atmospheric pressure CVD method. The gate insulating film may be formed of an NO film.

[0146]

(B) After the gate oxide film (gate insulating film) 3 is formed, threshold control ion implantation is performed as necessary (threshold control ion implantation may be performed before the gate oxide film 3 is formed. ..). Then, as shown in FIG. 18B, a refractory metal such as tungsten (W), titanium (Ti), and molybdenum (Mo), or a gate electrode material 61 such as silicide (WSi2, TiSi2, MoSi2) thereof. Is deposited on the entire surface of the gate oxide film 3 by a sputtering method, a vacuum evaporation method, a CVD method or the like. Then, a photoresist 62 having a thickness of 1 to 2 μm is applied to the surface of the gate electrode material 61 using a spinner. Then, by selectively exposing and developing the photoresist 62 using a predetermined photomask (reticle), as shown in FIG. 18C, only the portion of the photoresist 62 corresponding to the gate electrode 63 is selected. To remain. Further, using the photoresist 62 as an etching mask, as shown in FIG. 18C, the gate electrode material 61 is patterned by RIE and the gate oxide film between the source region 2s and the drain region 2d. A gate electrode 63 is formed on the (gate insulating film) 3.

[0147]

(C) Then, as shown in FIG. 19D, the photoresist 62 is removed after the gate electrode 63 is formed, and the surface of the SiC substrate 11 is cleaned by an RCA cleaning method or the like. An upper insulating film 4 made of a SiO2 film is deposited on the gate electrode 63 and the gate oxide film 3 which are sufficiently cleaned by an atmospheric pressure CVD method. As a result, in the region other than the gate electrode 63, the field insulating film 5 having a two-layer structure is formed. It is desirable that the total thickness of the field insulating film 5, which is the sum of the thickness of the gate oxide film 3 and the thickness of the upper insulating film 4, be about 100 nm to 600 nm.

[0148]

(D) Next, a photoresist 22 having a thickness of 1 to 2 μm as the “mask material” of the

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present invention is applied to the surface of the field acid insulating film 5 using a spinner. Then, by using a predetermined photomask (reticle), the mask material (photoresist) 22 is selectively exposed and developed to remove the photoresist 22 in the portions corresponding to the openings 6s and 6d to form a window portion. To do. Then, using the mask pattern of the photoresist 22 as an etching mask, the SiC substrate 11 is dipped in a BHF solution and wet-etched to form an opening in the field insulating film 5 as shown in FIG. 6s and 6d are formed. When forming the fine openings 6s and 6d, dry etching using gas plasma is preferable. For example, various dry etching methods such as RIE method and ECR ion etching using CHF3 or C2F6 as an etchant can be used. In this case, dry etching is first performed, and after leaving the field insulating film 5 of several tens of nm, switching to wet etching is performed. As described in the first embodiment, the wet etching or the dry etching is slightly performed regardless of whether the openings 6s and 6d are opened by the wet etching alone or by the combination of the dry etching and the wet etching. This is excessively performed so that the openings 6s and 6d of the field insulating film 5 become larger than the openings of the photoresist, and undercut portions are generated. Similar to the first and second embodiments, after the exposure of the surface of the source region 2s and the drain region 2d is confirmed by visual inspection of the etching monitor portion, overetching may be further added for a predetermined time. In the third embodiment, the photoresist 22 is used as the “mask material” of the present invention. However, if the material is not etched during this over-etching, a material other than the photoresist 22 is used as the “mask material” of the present invention. Can be adopted as.

[0149]

(E) Then, with the photoresist 22 as the etching mask remaining, the BHF solution is completely rinsed (rinsed) with ultrapure water, and then dried. Then, the SiC substrate 11 with the resist mask 22 adhered thereon is immediately installed in the chamber of the vacuum vapor deposition apparatus, and immediately evacuated. That is, the time for exposing the surface of the SiC substrate 11 to the atmosphere is as short as possible within 5 minutes. Then, the chamber of the vacuum vapor deposition apparatus is evacuated to a pressure of less than 1.3×10^{-5} Pa by using a turbo molecular pump, a cryopump, etc., and the first surface of the SiC substrate 11 is removed as shown in FIG. The conductor film 17 is deposited. For example, a Ni film is used as the first conductor film 17. As shown in FIG. 19 (f), in order to prevent the first conductor film 17 from adhering to the side walls of the openings 6s and 6d, an orifice or the like is used to improve the directivity of the vapor deposition beam. You can do it. At this time, as shown in FIG. 19F, since the undercut portion is formed so that the opening portion of the field insulating film 5 is larger than the opening portion of the photoresist mask 22, it is vapor-deposited on the bottom portion of the opening portion. The first conductor films 17s and 17d are accurately transferred to the shape of the undercut portion. Thus, the vapor deposition limiting regions (sidewall gaps) 77s and 77d having a constant distance and having a constant

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distance are generated between the peripheral portions of the first conductor films 17s and 17d and the side walls of the opening of the field insulating film 5. To do. The minute sidewall gaps 77s and 77d can be precisely controlled by the over-etching time of the opening etching. The thickness of the first conductor film 17 (17s and 17d) is set to be thinner than 1/2 of the diffusion depth of the source region 2s and the drain region 2d located therebelow.

[0150]

(F) After vacuum deposition of the first conductor film 17, the SiC substrate 11 is taken out of the chamber of the vacuum deposition apparatus. Subsequently, the lift-off method is used to selectively bury the first conductor pieces 27s and 27d only inside the respective openings, as shown in FIG. As a result, fine side wall gaps 77s and 77d are formed in a self-aligned manner between the peripheral portions of the first conductor pieces 27s and 27d and the side walls of the opening of the field insulating film 5.

[0151]

(G) Then, when the SiC substrate 11 is heat-treated in a non-oxidizing atmosphere at 700 ° C. to 1050 ° C. for a short time (about several minutes), as shown in FIG. The first conductor pieces 27s and 27d and the SiC substrate 11 react with each other to generate heating reaction layers 8s and 8d in the interface region between them, and between the heating reaction layer 8s and the source region 2s and heating reaction. Excellent ohmic characteristics are realized between the layer 8d and the drain region 2d. Strict control is required for controlling the partial pressure of oxygen and water as a “non-oxidizing atmosphere”, and the partial pressure of oxygen and water contained in the heat treatment atmosphere is at least 1 × 10 −3 Pa to 1 × 10 −. About 10 Pa, preferably 1. It is set to approximately 10-5 Pa to 1 × 10-10 Pa.

[0152]

(H) After forming the heated reaction layers 8s and 8d, as shown in FIG. 20I, a second conductor film 19 of Al or the like is deposited on the entire surface of the SiC substrate 11. Then, the source wiring 9s and the drain wiring 9d are patterned by a photolithography method and an etching technique such as RIE, thereby completing the MOSFET according to the third embodiment of the present invention (see FIG. 17).

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[0153]

According to the method of manufacturing a semiconductor device of the third embodiment, overetching of the field insulating film 5 is performed when forming contact holes for forming ohmic electrodes for the source region 2s and the drain region 2d. By controlling the etching time, the depth of the undercut portion formed under the mask material in the vicinity of the window can be controlled, which facilitates dimensional control. Further, the depths of the undercut portions allow the constant gaps (side wall gaps) 77s and 77d between the first conductor element 27 and the field insulating film 5 for forming the ohmic electrode to be determined in a self-aligned manner. The photolithography process for controlling the constant gaps (side wall gaps) 77s and 77d between the ohmic electrode and the field insulating film 5 is unnecessary. Therefore, the distance between the first conductor element 27 serving as an ohmic electrode and the side wall of the opening of the field insulating film 5 can be made sufficiently small, and the ohmic electrode having a small occupied area and a fine dimension can be arranged.

[0154]

Further, since the photolithography step can be omitted, the number of steps involved in forming the ohmic electrode for the source region 2s and the drain region 2d of the semiconductor device is reduced, and the manufacturing yield of the semiconductor device is increased. Furthermore, the semiconductor device according to the third embodiment can be applied with the standard Si semiconductor device manufacturing method, and is therefore easy and highly reliable.

[0155]

Furthermore, the first conductor element 27 can be prevented from reacting with the field insulating film 5, so that the field insulating film 5 on the contact surface with the metal material forming the first conductor element 27 can be prevented. The insulating property of the field insulating film 5 can be maintained without being reduced (eroded) by the high temperature heat treatment. Further, since the metal material forming the ohmic electrode is not in contact with the field insulating film 5, the problem that the adhesive force between the ohmic electrode generated from the first conductor element 27 and the field insulating film 5 is weak is originally caused. not exist. For this reason, the ohmic electrode is not peeled off after the process is completed, and the manufacturing yield is increased.

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[0156]

Further, in the step of forming the heated reaction layer 8s of the ohmic electrode, since there is no coexisting state of the ternary system of metal-SiC-SiO2 at the outer peripheral portion of the bottom of the ohmic electrode, there is no parasitic due to the reaction of the ternary system. The generation of Schottky junction can be avoided, and low contact resistance can be achieved. Further, since there is no obstruction of the horizontal current flow in the source region 2s and the drain region 2d due to the formation of the parasitic Schottky junction, a semiconductor device having good characteristics can be easily manufactured.

[0157]

(Other Embodiments) As described above, the present invention has been described by the first to third embodiments, but the description and drawings forming a part of this disclosure limit the present invention. Should not be understood to be. From this disclosure, various alternative embodiments, examples, and operation techniques will be apparent to those skilled in the art.

[0158]

For example, in the above description of the third embodiment, a lateral MOSFET having a recess gate structure has been described, but a lateral MOSFET having a planar gate structure as shown in FIG. 21 may be used. Similar to the third embodiment, the p-type SiC substrate 11 is used, but unlike in FIG. 17, the surface of the p-type SiC substrate 11 is formed of a flat surface at the same level. That is, the surface levels of the first main electrode region (source region) 2s and the second main electrode region (drain region) 2d, which are n-type SiC regions, and the source region 2s where the gate oxide film 3 is arranged. The surface of the p-type SiC substrate 11 between the drain region 2d and the drain region 2d is at the same level. A gate electrode 63 is arranged on the gate oxide film 3 having the planar gate structure. Then, an upper insulating film 4 is formed on the gate electrode 63 and on the gate oxide film 3 where the gate electrode 63 is not arranged, and the field insulating film 5 is formed by the gate oxide film 3 and the upper insulating film 4. It is configured. Others are the same as those in FIG. 17, and thus redundant description will be omitted.

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[0159]

Also in the semiconductor device according to another embodiment shown in FIG. 21, in the ohmic electrode for the source region 2s, the metal material forming the source electrode film 7s and the heating reaction layer 8s is the same as the field insulating film 5. In the ohmic electrode with respect to the drain region 2d, the metal material forming the drain electrode film 7d and the heating reaction layer 8d does not react and does not react with the field insulating film 5. Therefore, the field insulating film 5 on the contact surface with the metal material forming the source electrode film 7s and the drain electrode film 7d is not reduced (eroded) by the high temperature heat treatment. Further, generation of a parasitic Schottky junction due to a ternary coexistence reaction of metal-SiC-SiO2 at the outer peripheral portion of the bottom of the ohmic electrode can be avoided. Can be formed.

[0160]

Besides the lateral MOSFET having the recess gate structure or the planar gate structure, a vertical MOSFET may be used. Further, a vertical MOSFET in which a gate oxide film and a gate electrode are formed in the U groove or V groove may be used. Further, a MOSFET having a buried drain region may be used. In a MOSFET having a buried drain region, a sinker region is used to draw a current from the buried drain region, but in this case there is a concern that the on-resistance will increase. However, by applying the present invention, a low on-resistance and high-speed switching can be achieved at the same time by arranging a large number of fine structure sinker regions and ohmic electrodes connected thereto. In a p-channel power MOSFET having a double diffusion structure, a drain region (main electrode region) with a high impurity density is formed on the surface of an n-type SiC substrate (or ν -type SiC substrate or i-type SiC substrate) that functions as a drift region. An n-type SiC region can be formed. In this case, another n-type SiC region as the source region is formed in the p-body region formed on the surface of the n-type SiC substrate.

[0161]

Similarly, an n-type SiC region as a drain region and an n-type SiC region as a source region are formed on the surface of an n-type SiC substrate (or ν -type SiC substrate), and the source region and the drain region 2 are formed. If a Schottky electrode is formed on the surface of the n-type SiC substrate (or ν -type SiC substrate) in between, a MESFET can be realized.

[0162]

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Further, as described at the beginning of the description of the third embodiment, in addition to the FET, various "semiconductor devices" such as diodes, IGBTs, SITs, BJTs, SI thyristors, GTO thyristors, etc. can be used as the "semiconductor device" of the present invention. It is applicable to the semiconductor electronic device of.

For example, in the case of an npn-type bipolar transistor, a base region composed of a p-type SiC region is formed in a well shape on the surface of an n-type (or ν -type) SiC substrate having a low impurity density which serves as a collector region, and the base region of this base region is formed. An n-type SiC region having a high impurity density may be formed as a main electrode region (emitter region) at an inner position on the plane. In this case, an intrinsic semiconductor (i-type) SiC substrate is used in place of the low-impurity-density n-type SiC substrate serving as the collector region, and the high-impurity-density n-type SiC substrate is formed on the back surface (or part of the front surface) of the i-type SiC substrate. A collector region composed of a type SiC region may be formed.

[0163]

In the case of a thyristor such as a GTO thyristor, a p base region made of a p type SiC region is formed on a part or the whole surface of an n type SiC substrate to be an n base region, and inside the p base region. It is possible to form an n-type SiC region having a high impurity density as a cathode region (main electrode region) by epitaxial growth. In this case, a p-type SiC region as an anode region is formed on the back surface of the n-type SiC substrate to be the n-base region.

[0164]

On the other hand, in the n-channel junction type FET or the junction type SIT, the source region is formed on the surface of the n-type SiC substrate (or n-type (ν type) SiC substrate or i-type SiC substrate) that functions as a channel region. It is possible to form an n-type SiC region having a high impurity density as (main electrode region). FIG. 22 is a schematic sectional view of a cut gate type SIT. In FIG. 22, a high impurity density n-type SiC region 87 as a source region (first main electrode region) is formed on the surface of the n-type SiC substrate 12 functioning as a channel region. An n-type SiC region 81 having a high impurity density is formed as a drain region (second main electrode region) on the back surface. Then, in order to control the main

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current flowing between the source region 87 and the drain region 81, a gate region formed of the p-type SiC region 84 is formed at the bottom of the gate groove provided on the surface of the n-type SiC substrate 12. .. A gate electrode film 86 is connected to the gate region 84 via a gate heating reaction layer 85. An Al—Ti based electrode film can be used for the gate electrode film 86. For example, a Ti (50 nm thick) / Al (300 nm thick) laminated film may be used. The gate electrode film 86 is connected to the gate wiring 92 made of Al, Al-Si, Al-Cu-Si, Cu, Ti-W, or the like. A drain electrode 83 is formed in the drain region 81 via a drain heating reaction layer 82.

[0165]

In the junction type SIT shown in FIG. 22, the field region is formed on the n-type SiC substrate 12 by surrounding the source region 87 formed of the n-type SiC region 87 selectively formed on the surface of the n-type SiC substrate 12. The membrane 5 is mounted. The field insulating film 5 is composed of a thermal oxide film 3 and an upper insulating film 4 which is an insulating film other than the thermal oxide film. Then, inside the opening formed in the field insulating film 5 so as to expose the surface of the source region 87, the source electrode film 97 is arranged with a certain gap (side wall gap) 77 from the field insulating film 5. In the inside of the opening of the field insulating film 5, a source heating reaction layer 98, which is arranged with a certain gap (side wall gap) 77 from the field insulating film 5 and between the source electrode film 97 and the source region 87, Inside the opening of the insulating film 5, there is provided a first main electrode wiring (source wiring) 91 that is in contact with the surface of the source electrode film 97 and extends to the upper portion of the field insulating film 5.

[0166]

The potential between the source region 87 and the drain region 81 shown in FIG. 22 and the potential at the saddle point in the two-dimensional space of the potential in the channel due to the gate voltage applied to the gate region 84 is the height of the drain region. The main current is controlled by controlling the drain voltage applied to 81 and the gate voltage applied to the gate region 84. The current / voltage characteristics of SIT show characteristics according to the same exponential function law as the triode characteristics of vacuum tubes. According to the junction type SIT shown in FIG. 22, in the ohmic electrode for the source region 87, the metal material forming the source electrode film 97 and the heating reaction layer 98 has a structure that does not react with the field insulating film 5. The field insulating film 5 on the contact surface with the material is not reduced (eroded) by the high temperature heat treatment. Therefore, the high insulating property of the field insulating film 5 formed around the source

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region 87 of the junction type SIT can be maintained, and the leak current can be reduced. In addition, since the metal material forming the source electrode film 97 is not in contact with the field insulating film 5, the problem that the adhesive force between the source electrode film 97 and the field insulating film 5 is weak does not originally exist. Therefore, the source electrode film 97 is not peeled off after the manufacturing process of the junction type SIT is completed, and the manufacturing yield of the junction type SIT is increased. Furthermore, the formation of parasitic Schottky junction due to the ternary coexistence reaction of metal-SiC-SiO2 at the outer peripheral portion of the bottom of the ohmic electrode can be avoided, so that an ohmic electrode with low contact resistance can be achieved. As a result, in the junction type SIT shown in FIG. 22 capable of realizing a junction type SIT having a high breakdown voltage and capable of operating at high speed, instead of the n type SiC region 81 having a high impurity density as a drain region, a high impurity as an anode region is used. If a p-type SiC region having a high density is formed, it becomes an n-channel SI thyristor. In this case, the high impurity density n-type SiC region 87 as the source region functions as the cathode region.

[0167]

In the n-channel IGBT, an n-type SiC region having a high impurity density as a collector region can be formed on the front surface (or the back surface) of the n-type SiC substrate (or ν -type SiC substrate) that functions as a drift region. .. In this case, another n-type SiC region as the emitter region is formed inside the p-body region formed on the surface of the n-type (or ν -type) SiC substrate at a position different from the collector region. The ohmic electrode structure of the present invention can be applied to an n-type SiC region having a high impurity density as a main electrode region of these various semiconductor electronic devices. In the manufacturing processes of the first to third embodiments described above, the thermal oxide film 3 which is an element of the field insulating film 5 is formed immediately before the upper insulating film 4 is formed. As shown in the process cross-sectional views, substantially the same effect can be obtained even if the thermal oxide film is formed immediately after the upper insulating film 4 is formed.

[0168]

(A) For example, the n-type SiC region 32 is formed on the surface of the SiC substrate 1 by exactly the same method as that described in the first embodiment. Then, the SiC substrate 1 is cleaned sufficiently by using the SiC substrate 1 cleaning method such as the RCA cleaning method. Thereafter, as shown in FIG. 23A, an oxygen permeable insulating film 44 such as a SiO2 film is deposited on the SiC substrate 1 by the atmospheric pressure CVD method.

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[0169]

(B) After depositing the oxygen permeable insulating film 44, as shown in FIG. 23B, heat treatment is performed in a dry oxygen atmosphere to thermally oxidize the surface of the SiC substrate 1 to form the oxygen permeable insulating film 44. A thermal oxide film 3 is grown on the interface with the SiC substrate 1. Similar to the first embodiment, the thickness of the thermal oxide film 3 is less than 50 nm, preferably 5 to 20 nm. As a result, the upper insulating film 4 made of the oxygen permeable insulating film (SiO2 film) 44 is located on the thermal oxide film 3, and the field insulating film 5 having a two-layer structure is formed.

[0170]

(C) After that, it is possible to proceed with the same steps as the method shown in FIG. 3 (f) and subsequent figures described in the first embodiment. That is, as shown in FIG. 23C, a photoresist 22 having a thickness of 1 to 2 μm is applied to the surface of the field acid insulating film 5 using a spinner. Then, using a predetermined photomask (reticle), the photoresist 22 is selectively exposed and developed to remove the photoresist 22 in the portion corresponding to the opening 6. Subsequently, using the pattern of the photoresist 22 as an etching mask, wet etching is performed to form an opening 6 in the field insulating film 5 as shown in FIG. At this time, as described in the first embodiment, after just etching in which the exposure of the surface of the n-type SiC region 32 is confirmed, overetching is further performed until a predetermined undercut portion depth is obtained. to add. The subsequent description will be omitted because it is redundant.

[0171]

Using the method shown in FIG. 23, it is possible to achieve a practical contact resistance ρc of the order of 10^{-7} Ωcm 2. As described above, needless to say, the present invention includes various embodiments and the like not described here. Therefore, the technical scope of the present invention is defined only by the matters specifying the invention according to the scope of claims reasonable from the above description.

[0172]

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Brief description of the drawings

[0173]
<Figure 1> It is the principal part cross section diagram which shows the constitution of the ohmic electrode structure which relates to the 1st execution form of this invention.

[0174]
2 is a process cross-sectional view (No. 1) for explaining the manufacturing process of the ohmic electrode structure according to the first embodiment of the present invention.

[0175]
3 is a process cross-sectional view (No. 2) for explaining the manufacturing process of the ohmic electrode structure according to the first embodiment of the present invention.

[0176]
4 is a process cross-sectional view (No. 3) for explaining the manufacturing process of the ohmic electrode structure according to the first embodiment of the present invention.

[0177]
5 is a current-voltage characteristic of the TLM contact group for explaining the ohmic electrode structure according to the first embodiment of the present invention.

[0178]
<Figure 6> It is the figure which shows the TLM characteristic of the TLM contact group in order to explain the ohmic electrode structure which relates to the 1st execution form of this invention.

[0179]
7 is a diagram showing the observation results of the surface morphology in the contact window by Nomarski interference microscope.

[0180]
8 is a diagram sketching a cross-sectional TEM image of the ohmic electrode structure according

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to the first embodiment of the present invention.

[0181]
9 is a diagram showing the change in composition in the thickness direction of the ohmic electrode structure according to the first embodiment of the present invention obtained by Rutherford backscattering analysis.

[0182]
10 is a diagram showing the relationship between the thickness and surface morphology of the ohmic electrode structure according to a second embodiment of the present invention.

[0183]
<Figure 11> It is the figure which shows the relationship of electrode thickness and contact resistance of the ohmic electrode structure which relates to the 2nd execution form of this invention.

[0184]
<Figure 12> It is the figure which shows the relationship of the impurity density and contact resistance of the ohmic electrode structure which relates to the 2nd execution form of this invention with the result of former technology.

[0185]
<Drawing 13> The principal part cross section diagram which shows the constitution of the ohmic electrode structure which relates to the 2nd execution form of this invention.

[0186]
14 is a process sectional view (1) for explaining a manufacturing process of the ohmic electrode structure according to the second embodiment of the present invention.

[0187]
FIG. 15 is a process sectional view (2) for explaining a manufacturing process of the ohmic electrode structure according to the second embodiment of the present invention.

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[0188]
16 is a process cross-sectional view (No. 3) for explaining the manufacturing process of the ohmic electrode structure according to the second embodiment of the present invention.

[0189]
17 is a cross-sectional view of a main portion showing the configuration of a semiconductor device (lateral MOSFET) according to a third embodiment of the present invention.

[0190]
18 is a process cross-sectional view (No. 1) for explaining the manufacturing process of the semiconductor device (lateral MOSFET) according to the third embodiment of the present invention.

[0191]
19 is a process cross-sectional view (No. 2) for explaining the manufacturing process of the semiconductor device according to the third embodiment of the present invention.

[0192]
20 is a process sectional view (3) for explaining the manufacturing process of the semiconductor device according to the third embodiment of the present invention.

[0193]
21 is a cross-sectional view of a main portion showing the configuration of a semiconductor device (lateral MOSFET) according to another embodiment of the present invention.

[0194]
<Figure 22> It is the principal part cross section diagram which shows the constitution of the semiconductor device (junction type SIT) which relates to other execution form of this invention.

[0195]
23 is a part of a process cross-sectional view for explaining a manufacturing process of an ohmic electrode structure according to still another embodiment of the present invention.

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[0196]
24 is a cross-sectional view of a main part showing the configuration of the ohmic electrode structure according to the first conventional technology.

[0197]
25 is a cross-sectional view of a main part showing the configuration of the ohmic electrode structure according to the second conventional technology.

[0198]
Explanation of symbols

[0199]
1, 11 and 12 SiC substrate 2, 32 n-type SiC region 2s First main electrode region (source region) 2d Second main electrode region (drain region) 3 Thermal oxide film (gate oxide film) 4 Upper insulating film 5 Field insulating film 6 Field insulating film opening 7,47 Electrode film 7s Source electrode film 7d Drain electrode film 8, 8s, 8d Heat reaction layer 9 Wiring conductor element 9s First main electrode wiring (source wiring) 9d Second Main electrode wiring (drain wiring) 17, 17s, 17d First conductor film 27, 27s, 27d First conductor piece (first conductor film piece) 19 Second conductor film 20 Epitaxial growth layer 21 Etching Masks 22, 23, 34, 62 Photoresist 33 Ion implantation mask 35 Ion implantation through film 42 First metal film (Ni film) 43 Si oxide film (field insulating film) 44 Oxygen permeable insulating film 45 Ohmic contact piece 61 Gate electrode Material 63 Gate electrodes 77, 77s, 77d Gap 81 Drain region (second main electrode region) 82 Drain heating reaction layer 83 Drain electrode 84 Gate region 85 Gate heating reaction layer 86 Gate electrode film 87 Source region (first main electrode Region 91 first main electrode wiring (source wiring) 92 gate wiring 97 source electrode film 98 source heating reaction layer

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CLAIMS JP2002093742

1.
A silicon carbide (SiC) substrate, an n-type SiC region selectively formed on the surface of the SiC substrate, a field insulating film mounted on the SiC substrate, and the n-type in the field insulating film. An electrode film disposed with a constant gap from the field insulating film inside the opening opened to expose the surface of the SiC region, and the constant inside the opening from the field insulating film. And a heating reaction layer disposed between the electrode film and the n-type SiC region, extending in contact with the surface of the electrode film inside the opening and extending to the upper part of the field insulating film. An ohmic electrode structure, comprising:

2.
The ohmic electrode structure according to claim 1, wherein the predetermined gap is smaller than a thickness of the field insulating film.

3.
3. The field insulating film is composed of a laminated insulating film of a thermal oxide film of SiC and an upper insulating film made of an insulating film having a composition or density different from that of the thermal oxide film. Ohmic electrode structure.

4.
4. The ohmic electrode structure according to claim 1, wherein the dielectric breakdown electric field strength of the upper insulating film is lower than the dielectric breakdown electric field

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strength of the thermal oxide film.

5.

5. The ohmic electrode structure according to claim 1, wherein an etching rate of the upper insulating film with the buffer hydrofluoric acid solution is higher than an etching rate of the thermal oxide film with the buffer hydrofluoric acid solution. body.

6.

Forming an n-type SiC region having a high impurity density on at least a part of the surface of the silicon carbide (SiC) substrate; cleaning the surface of the SiC substrate; and covering the surface of the SiC substrate with a field insulating film. And a step of forming a mask material having an etching rate different from that of the field insulating film on the field insulating film, a step of providing a window portion in the mask material to form a mask pattern, and the mask pattern A step of etching the field insulating film until the surface of the n-type SiC region is exposed to form an opening, and after the surface of the n-type SiC region is exposed, the field insulating film is further over-etched, Forming an undercut portion under the mask material near the window portion, and depositing a first conductor film on the surface of the n-type SiC region in the upper portion of the mask material and inside the opening. By removing the mask material, the elemental pieces of the first conductor film are left on the surface of the n-type SiC region inside the opening with a certain gap from the field insulating film. And a step of heat-treating the SiC substrate in a non-oxidizing atmosphere to generate a heated reaction layer between the segment of the first conductor film and the n-type SiC region. Method for manufacturing ohmic electrode structure.

7.

The step of covering with the field insulating film includes a step of growing a thermal oxide film on the surface of the SiC substrate by thermal oxidation, and a step of depositing an insulating film on the thermal oxide film by a method other than thermal oxidation. The method for manufacturing an ohmic electrode structure according to claim 6, comprising:

8.

In the step of covering with the field insulating film, a step other than thermal oxidation is used to deposit an oxygen permeable insulating film on the surface of the SiC substrate, and after the oxygen permeable insulating film is deposited, thermal oxidation is performed to form the SiC The method for manufacturing an ohmic electrode structure according to claim 6, comprising a step of growing a thermal oxide film on an interface between the surface of the substrate and the oxygen-permeable insulating film.

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9.
The method of manufacturing an ohmic electrode structure according to claim 6, wherein the step of forming the mask material is a step of applying a photoresist.

10.
10. The step of forming an opening in the field insulating film, wherein the step immediately before exposing the surface of the n-type SiC region is completed by wet etching and rinsing with ultrapure water. A method for manufacturing the described ohmic electrode structure.

11.
11. The method for manufacturing an ohmic electrode structure according to claim 6, wherein the thickness of the first conductor film is less than 1/2 of the thickness of the n-type SiC region.

12.
In the step of forming the heated reaction layer, the SiC substrate is heat-treated in a non-oxidizing atmosphere in which the partial pressures of oxygen (O2) and water (H2O) are both 1 $\times$ 10 $-$3 Pa to 1 $\times$ 10 $-$10 Pa. The method for manufacturing an ohmic electrode structure according to any one of claims 6 to 11, characterized in that.

13.
The method further comprises the step of forming a second conductor film on the field insulating film so as to contact the element of the first conductor film and cover the opening of the field insulating film. The method for manufacturing an ohmic electrode structure according to any one of claims 6 to 11.

14.
10. A step of removing an oxide film formed on the surface of the segment of the first conductor film or attached hydrocarbons immediately before the formation of the second conductor film is added. 13. The method for manufacturing the ohmic electrode structure according to 13.

15.
A silicon carbide (SiC) substrate, a main electrode region composed of an n-type SiC region selectively formed on the surface of the SiC substrate, a field insulating film mounted on the SiC

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substrate, and the field insulating film. In the inside of the opening opened so as to expose the surface of the main electrode region in the film, the electrode film disposed with a certain gap from the field insulating film, and in the inside of the opening, the field A heating reaction layer disposed at a certain distance from the insulating film and between the electrode film and the main electrode region, in contact with the surface of the electrode film inside the opening, and in the field insulating film. A semiconductor device comprising a main electrode wiring extended to an upper portion.

16.

16. The semiconductor device according to claim 15, wherein the constant gap is smaller than the thickness of the field insulating film.

17.

A step of forming a main electrode region composed of an n-type SiC region having a high impurity density on at least a part of a surface of a silicon carbide (SiC) substrate, a step of cleaning the surface of the SiC substrate, A step of covering with a field insulating film, a step of forming a mask material having an etching rate different from that of the field insulating film on the field insulating film, a step of forming a window portion in the mask material, and forming a mask pattern. A step of etching the field insulating film using the mask pattern until the surface of the main electrode region is exposed to form an opening; and after the surface of the main electrode region is exposed, the field insulating film is further overetched. Then, a step of forming an undercut portion in the lower portion of the mask material near the window portion, and depositing a first conductor film on the upper surface of the mask material and the surface of the main electrode region inside the opening portion. The step of removing the mask material leaves the first conductive film segment on the surface of the main electrode region inside the opening with a constant gap from the field insulating film. And a step of heat-treating the SiC substrate in a non-oxidizing atmosphere to generate a heated reaction layer of the segment of the first conductor film and the main electrode region. Device manufacturing method.

18.

The step of covering with the field insulating film includes a step of growing a thermal oxide film on the surface of the SiC substrate by thermal oxidation, and an insulating film is deposited on the thermal oxide film by a method other than thermal oxidation. 18. The method for manufacturing a semiconductor device according to claim 17, further comprising:

19.

19. The method of manufacturing a semiconductor device according to claim 18, further

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comprising the step of forming a gate electrode on the thermal oxide film after the step of growing the thermal oxide film.

20.

20. The method of manufacturing a semiconductor device according to claim 17, wherein the thickness of the first conductor film is less than 1/2 of the thickness of the main electrode region.

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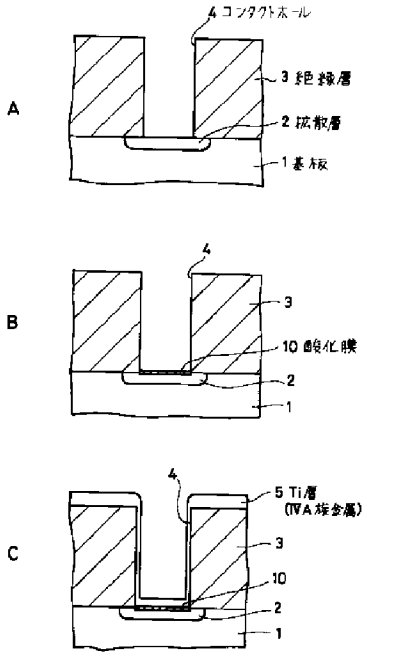
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(71)出願人　000002185
ソニー株式会社
東京都品川区北品川６丁目７番35号
(72)発明者　宮本　孝章
東京都品川区北品川６丁目７番35号　ソニー株式会社内
(72)発明者　角　博文
東京都品川区北品川６丁目７番35号　ソニー株式会社内
(74)代理人　弁理士　松隈　秀盛

(54)【発明の名称】　メタルプラグの形成方法

(57)【要約】
【目的】　ＴｉをＳｉ上にＣＶＤ法によりＣｌを含む材料ガスを用いて成膜する際に、ＣｌのＳｉへの浸食を回避して、リーク電流の低減化をはかる。
【構成】　半導体層上に開口したコンタクトホールに配線層を埋込むメタルプラグの形成方法において、その一例の製造工程図を図１Ａ～Ｃ及び図２Ａ～Ｃに示すように、コンタクトホール３の底部に薄い酸化膜１０を形成した後、ＣＶＤ法によりこのコンタクトホール３内にⅣＡ族金属即ちＴｉ、Ｚｒ又はＨｆの例えばＴｉ層５を堆積して、配線層を被着形成する。



本発明メタルプラグの形成方法の一例の工程（その１）

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【特許請求の範囲】
【請求項１】　半導体層上に開口したコンタクトホールに配線層を埋込むメタルプラグの形成方法において、上記コンタクトホールの底部に薄い酸化膜を形成した後、化学気相成長法により上記コンタクトホール内にIVA族金属を堆積して、配線層を被着形成することを特徴とするメタルプラグの形成方法。
【請求項２】　半導体層上に開口したコンタクトホールに配線層を埋込むメタルプラグの形成方法において、上記コンタクトホールの底部に薄い酸化膜を形成した後、化学気相成長法により上記コンタクトホール内にIVA族金属シリサイドを堆積して、配線層を被着形成することを特徴とするメタルプラグの形成方法。
【請求項３】　上記IVA族金属を電子サイクロトロン共鳴プラズマによる化学気相成長法により形成することを特徴とする上記請求項１に記載のメタルプラグの形成方法。
【請求項４】　上記IVA族金属シリサイドを熱化学気相成長法により形成することを特徴とする上記請求項２に記載のメタルプラグの形成方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、各種半導体装置の半導体層上の配線層との接続部におけるメタルプラグの形成方法に係わる。
【０００２】
【従来の技術】超ＬＳＩなどの高密度の半導体装置においてはコンタクトホールの微細化が進められており、この微細コンタクトホールにＡｌ等の配線層を埋込む技術としては、高温におけるＡｌの流動性を利用した高温Ａｌスパッタ法とか、スパッタ法よりカバレッジが優れたＣＶＤ（化学気相成長）法によってＡｌより高温耐熱性を有するＷ（タングステン）をコンタクトホール内を含んで全面的に被着するいわゆるＢＬＫ（ブランケット）－Ｗ　ＣＶＤ法等が現在多く利用されている。
【０００３】このような高温Ａｌスパッタ法やＢＬＫ－Ｗ　ＣＶＤ法のいずれのプロセスを用いる場合においても、整流性のない低抵抗の半導体－金属接合（オーミックプロセス）を形成することが必要である。このため上述の高温Ａｌスパッタ法ＢＬＫ－Ｗ　ＣＶＤ法の両プロセスにおいて、半導体層と配線層との間に高融点金属の中でも比較的低いコンタクト抵抗を有し、シリコン酸化膜を還元できるチタンＴｉを形成する方法が採られている。
【０００４】チタンは、その酸化物がシリコン酸化物に比し生成自由エネルギーが低く即ちチタン酸化物を形成した方が安定であるため、上述したようにシリコン酸化物を還元し得る能力を有するが、チタン膜厚が薄い場合やシリコン酸化膜が厚い場合はチタンはシリコン酸化物を還元することができず、低オーミックコンタクト抵抗を得ることができない（例えば第38回春季応用物理学会講演会予稿集p.691 ）。
【０００５】またチタンは通常スパッタ法により堆積されているため、高アスペクト比の微細コンタクトホール内に被着しようとすると、コンタクトホールの底部において拡散層上の自然シリコン酸化膜を還元し得るに充分なチタン膜厚が得られず、低コンタクト抵抗が得られないという問題がある。
【０００６】
【発明が解決しようとする課題】このため、コンタクトホール内にチタンをスパッタ法によらずに、化学気相成長法により被着形成することが試みられている。例えばＥＣＲ（電子サイクロトロン共鳴）プラズマＣＶＤ法や熱ＣＶＤ法、ＭＯＣＶＤ（有機金属による化学気相成長）法など多くの方法によりチタンを成膜することが試みられているが、ＭＯＣＶＤ法ではチタン単体を成膜できる適当な有機材料がみつかっていないこと、熱ＣＶＤ法では１０００℃程度以上の高温を必要とするため、ＬＳＩの製造には適用しにくいなどの問題がある。
【０００７】そこで現状では、ＥＣＲプラズマによって$TiCl_4$の解離を促進させることを利用した$TiCl_4+H_2$系のＥＣＲプラズマＣＶＤ法によるＴｉ成膜と、$TiCl_4+SiH_4$系熱ＣＶＤ法による$TiSi_2$成膜が行われている。
【０００８】しかしながらこれらの方法では、$TiCl_4$ソースを利用しているため、$TiCl_4$中のＣｌや或いは生成されるＨＣｌが例えばコンタクトホール底部のシリコン拡散層を浸食する問題がある（例えば"Extended Abstracts of 1991 Inter-national Conference on Solid State Devices and Materials,Yokohama,1991,pp210-212"）。
【０００９】例えば図５に示すように、Ｓｉ等より成る基板１上に拡散層２を形成し、厚いSiO_2等より成る絶縁層３を被着して拡散層２に達する深さのコンタクトホール４を開口した後上述の例えば$TiCl_4+H_2$系のＥＣＲプラズマＣＶＤ法によりＴｉ層５を被着すると、拡散層２のＳｉがＨＣｌに削られて矢印ｔで示すようにＴｉが浸食して拡散層２と基板１の間の接合破壊が生じ、リーク電流が増大する恐れがある。
【００１０】本発明は、このようなＳｉ拡散層の浸食が生じないようにＴｉ等のバリアメタルを形成し得るメタルプラグの形成方法を提供するものである。
【００１１】
【課題を解決するための手段】本発明は、半導体層上に開口したコンタクトホールに配線層を埋込むメタルプラグの形成方法において、その一例の製造工程図を図１Ａ～Ｃに示すように、コンタクトホール３の底部に薄い酸化膜１０を形成した後、ＣＶＤ法によりこのコンタクトホール３内に、Ｔｉ、Ｚｒ又はＨｆのIVA族金属、例えばＴｉ層５を堆積して、配線層を被着形成する。

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【００１２】また他の本発明は、半導体層上に開口したコンタクトホールに配線層を埋込むメタルプラグの形成方法において、図４Ａ～Ｃにその一例の製造工程図を示すように、コンタクトホール３の底部に薄い酸化膜１０を形成した後、ＣＶＤ法によりコンタクトホール３内にＴｉＳｉ$_x$、ＺｒＳｉ$_x$又はＨｆＳｉ$_x$のIVA族金属シリサイド、例えばＴｉＳｉ$_X$層８を堆積して、配線層を被着形成する。

【００１３】また本発明は、上述の図１Ａ～Ｃに示すメタルプラグの形成方法において、上述のIVA族金属例えばＴｉ層５をＥＣＲプラズマＣＶＤ法により形成する。

【００１４】更にまた本発明は、上述の図４Ａ～Ｃに示すメタルプラグの形成方法において、上述のIVA族金属シリサイド例えばＴｉＳｉ$_X$層８を熱ＣＶＤ法により形成する。

【００１５】

【作用】上述したように、本発明メタルプラグの形成方法は、コンタクトホール３の底部に薄い酸化膜を形成した後、この上にIVA族金属又はIVA族金属シリサイドをＣＶＤ法により成膜するものであり、成膜中にＣｌによって浸食されにくい酸化膜を薄く形成しておくことによってＳｉの浸食を回避して、リーク電流を低減化し得るものである。

【００１６】また、IVA族金属即ちＴｉ、Ｚｒ及びＨｆがＳｉ酸化膜の還元能力を有するため、その後の熱処理により酸化膜が還元されて耐熱性に優れたシリサイドを形成することができて、低コンタクト抵抗でカバレッジの優れたメタルプラグを形成することができる。

【００１７】更にまた、IVA族金属の成膜方法としてＥＣＲプラズマＣＶＤ法、IVA族金属シリサイドの成膜方法として熱ＣＶＤ法を採ることによって、微細な形状のコンタクトホール内においても埋め込み性良く所望の膜厚をもって形成することができ、この下の拡散層上の自然酸化膜を十分還元することができ、良好なコンタクト抵抗を得ることができる。

【００１８】

【実施例】以下本発明実施例を図面を参照して詳細に説明する。各例共に、Ｓｉ基板等より成る半導体層上に不純物拡散層を設け、この上に配線層を接続する場合を示す。

【００１９】実施例１

この例においては、Ｔｉ層をＥＣＲプラズマＣＶＤ法により形成する際に、予め薄い酸化膜を被着しておく場合で、先ず図１Ａに示すように、Ｓｉ等より成る基板１上の所定位置に不純物等を注入して拡散層２を形成する。そしてこの後SiO_2等の絶縁層３をＣＶＤ法等により厚く堆積し、拡散層２上に達する深さでその径が０．４μｍ～０．６μｍ程度の微細なコンタクトホール４を開口する。

【００２０】次に図１Ｂに示すように、熱酸化等によりコンタクトホール４の底部即ち拡散層２の上部に厚さ３～５ｎｍ程度の薄いSiO_2酸化膜１０を形成する。この酸化条件としては、例えば酸素流量を１０１／ｍｉｎ、基板温度を８５０℃、処理時間を５～１０ｍｉｎとして形成することができる。

【００２１】そして図１Ｃに示すように、この上を覆って全面的にIVA族金属の例えばＴｉ層５をＣＶＤ法により被着する。この場合$TiCl_4+H_2$系によるＥＣＲプラズマＣＶＤ法により厚さ３０ｎｍ程度として堆積する。ＥＣＲプラズマＣＶＤの条件は、基板温度を４２０℃～５４０℃、マイクロ波パワーを２．８ｋＷ、$TiCl_4$、H_2の流量をそれぞれ１０ｓｃｃｍ、５０ｓｃｃｍとし、Ａｒの流量を４３ｓｃｃｍとした。

【００２２】Ｓｉ－Ｓｉ原子間の結合エネルギーは７６ｋｃａｌ／ｍｏｌであり、Ｓｉ－Ｃｌ間の結合エネルギーは７７ｋｃａｌ／ｍｏｌであるため、前述したように、従来の方法による場合はＴｉ成膜材料の$TiCl_4$中のＣｌによって下地Ｓｉ拡散層が容易に浸食されてしまう。これに対し、Ｓｉ－Ｏ間の結合エネルギーは１９２ｋｃａｌ／ｍｏｌと比較的高く、本発明によればこのように安定なSiO_2膜を予め形成しておくため、Ｃｌにより下地Ｓｉが浸食されることなく拡散層－基板間の接合が破壊されることを確実に回避できる。

【００２３】そしてこの後図２Ａに示すように、ＥＣＲプラズマＣＶＤ法にてＴｉＮ層６を厚さ例えば７０ｎｍとして全面的に堆積する。この場合基板温度を４２０℃～５４０℃、マイクロ波パワーを２．８ｋＷとし、$TiCl_4$，N_2，H_2，Ａｒの各流量をそれぞれ１０，１５，５０，４３ｓｃｃｍとした。

【００２４】この後、２段階のアニールを行って図２Ｂに示すようにコンタクトホール４の底部にてＴｉと下地Ｓｉ拡散層をSiO_2酸化膜を介して反応させ、ＴｉＳｉ$_x$（チタンシリサイド）等のシリサイド１１を形成する。この場合、第１のアニールはＡｒ雰囲気中で基板温度を６５０℃、３０秒間行い、第２のアニールをN_2中で９００℃、３０秒間行った。このように第２のアニール処理において窒素を導入することによってコンタクトホール４の側壁部及び絶縁層３上のＴｉ層は窒化され、コンタクトホール４内のシリサイド１１上を含めて全面的にＴｉＮ層１６が形成される。

【００２５】尚、上述したようにＴｉ等のIVA族金属は、Ｓｉ酸化物を形成するよりも金属酸化物を形成した方が安定であるためＳｉ酸化物を還元することができる。そして上述したように３～５ｎｍ程度の薄い酸化膜を介してアニールを施すことによって高温耐熱性に優れたシリサイド膜を形成することができることが、例えば本出願人の出願に係る特開平３－３８８２３号公開公報、又は特開平４－３４９２６号公開公報等おいて示されている。本発明においては特にこの酸化膜１０の上にＣＶＤ法によってIVA族金属またはIVA族金属シリサイ

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ドを形成することにより、高アスペクト比のコンタクトホールにおいても良好に成膜することができる。

【００２６】そして更に、図２Ｃに示すように例えばＢＬＫ－ＷをＣＶＤ法により埋込み形成して配線層７を形成し、メタルプラグを構成する。この場合、堆積条件としては例えば基板温度４５０℃、圧力1×10^{4} Ｐａ、WF_6 の流量を９５ｓｃｃｍ、H_2 の流量を５５０ｓｃｃｍとした。

【００２７】また、このＢＬＫ－Ｗを用いずに、例えば高温Ａｌスパッタ法により図３に示すようにＡｌより成る配線層７を形成することもできる。図３において、図１及び図２に対応する部分には同一符号を付して重複説明を省略する。この場合はＴｉＮ層１６の表面に自然発生的に形成される自然酸化膜を逆スパッタにてエッチング除去した後、Ａｌとの濡れ性を良好にするためのＴｉ層１７とＡｌより成る配線層７とを、大気開放することなく順次連続堆積することによって、埋込みを良好に行うことができる。上述の逆スパッタ条件としては、ＲＦ電圧を１０００Ｖ、基板温度２００℃、Ａｒの流量を５０ｓｃｃｍ、圧力０．５Ｐａとして行い、またＴｉ層１７のスパッタ条件としてはＤＣ４ｋＷ、基板温度１５０℃、Ａｒ流量１００ｓｃｃｍ、圧力０．５Ｐａとし、更にＡｌスパッタ条件を基板温度４８０℃～５００℃、Ａｒ流量を１００ｓｃｃｍ、圧力０．５Ｐａとして行った。

【００２８】このように、コンタクトホール４内にSiO_2 酸化膜１０を薄く形成した後、ＴｉをＥＣＲプラズマＣＶＤ法等により形成することによって、微細なコンタクトホール４内においても良好な密着性をもってメタルプラグを形成することができる。

【００２９】実施例２

次に、本発明による他の実施例を図４Ａ～Ｃを参照して説明する。この例においては熱ＣＶＤ法により$TiSi_x$ を形成する場合に、予め薄い酸化膜を形成する方法を適用したものである。

【００３０】先ず図４Ａに示すように、Ｓｉ等より成る基板１上に拡散層２を形成した後、厚くSiO_2 等の絶縁層３を形成して、０．４μｍ～０．６μｍ程度の微細なコンタクトホール４をフォトリソグラフィ等の適用により開口する。そして上述の実施例と同様に、即ち熱酸化等によりコンタクトホール４の底部即ち拡散層２の上部に厚さ３～５ｎｍ程度の薄いSiO_2 酸化膜１０を形成する。この酸化条件としては、例えば酸素流量を１０ｌ／ｍｉｎ、基板温度を８５０℃、処理時間を５～１０ｍｉｎとして形成することができる。

【００３１】そしてこの後、図４Ｂに示すように、全面的にIVA族金属シリサイドの例えば$TiSi_x$ 層８を、$TiCl_4+SiH_4$ 系熱ＣＶＤ法により被着形成する。このとき、$TiSi_x$ をＴｉリッチな組成とし、即ちＳｉのＴｉに対する組成比を２．０より小さい１．０～１．８の例えば１．８程度とし、堆積条件としては、基板温度を５００℃以上の例えば７００℃程度とし、SiH_4 の$TiCl_4$ に対する流量比SiH_4 ／$TiCl_4$ を５～１０とした。

【００３２】通常このようにシリコン基体上等に$TiSi_x$ を成膜する場合は、ストレスを抑制するためにＳｉリッチな組成とし、Ｓｉの組成比ｘは２．６程度とされるが、本発明においては、$TiSi_x$ の下層のSiO_2 酸化膜１０を十分還元することができるように、Ｓｉ組成比を１．８程度以下とするものである。尚、Ｓｉ組成比を１．０以上とするのは、組成比が１．０未満のときは熱ＣＶＤ法による成膜を行いにくくことによる。尚、$TiSi_x$ は例えばＥＣＲプラズマＣＶＤ法により成膜することもできる。

【００３３】このように$TiSi_x$ をＴｉリッチな組成として被着した後シリサイド化することによって酸化膜１０中のＳｉを完全に反応させることができ、耐熱性に優れた良好なシリサイド１１を形成することができると共に、実施例１において説明したと同様に、薄い酸化膜１０を予め形成しておくことによって、$TiSi_x$ 成膜の際のＣｌによるＳｉの浸食を抑制することができる。

【００３４】そしてこの後NH_3 雰囲気中において基板温度９００℃、３０秒間のアニールを行う。このとき、$TiSi_x$ （ｘ＝１．０～１．８）と下地Ｓｉ拡散層２とがSiO_2 酸化膜１０を介して反応し、図４Ｃに示すように、コンタクトホール４の底部に厚いシリサイド１１が形成される。このシリサイド１１即ち$TiSi_x$ は、化学式通りのいわゆるストイキオメトリーなｘ＝２．０の組成となる。また$TiSi_x$ 層８の表面は窒化され、薄いＴｉＮ層９が形成される。

【００３５】そしてこの後、上述の実施例１と同様に、ＢＬＫ－Ｗまたは高温Ａｌスパッタ法等により配線層を形成して、微細なコンタクトホール４内においても良好な密着性をもってメタルプラグを形成することができる。

【００３６】尚、上述の各例においては半導体装置の拡散層上にコンタクトホールを設ける場合について説明したが、その他ポリシリコンゲート上の接続部などの種々のメタルプラグ形成の際に本発明を適用し得ることはいうまでもない。また、上述の各例においてはＴｉを用いてメタルプラグを形成したが、その他IVA族金属のＺｒ、Ｈｆを用いた場合も同様の効果を得ることができる。更に、その形成方法としても上述の各方法に限定されることなく、温度、反応ガス流量等において種々の変形変更をなし得ることはいうまでもない。

【００３７】

【発明の効果】上述したように、本発明方法によれば予めSiO_2 酸化膜を形成した後、Ｔｉ又は$TiSi_x$ をＣＶＤ法により成膜することによって、成膜材料に含まれるＣｌによってＳｉが浸食されることを回避でき、カ

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バレッジに優れ、低リーク電流のメタルプラグを形成することができる。特に、ＴｉまたはＴｉＳｉ$_X$を成膜した後アニールを施してSiO_2酸化膜をシリサイド化することにより、コンタクト抵抗の低減化をはかることができる。

【００３８】また、特にＴｉＳｉを形成する場合にＴｉリッチな組成とすることによって、確実に酸化膜を還元させてシリサイド化することができ、低コンタクトで耐熱性に優れたメタルプラグを形成することができる。

【図面の簡単な説明】

【図１】本発明メタルプラグの形成方法の一例の製造工程図である。

【図２】本発明メタルプラグの形成方法の一例の製造工程図である。

【図３】本発明メタルプラグの形成方法の他の例の一製造工程図である。

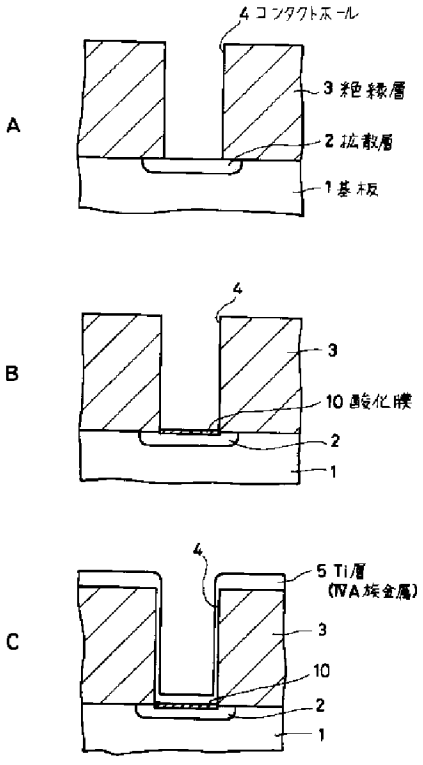
【図４】本発明メタルプラグの形成方法の他の例の製造工程図である。

【図５】従来のメタルプラグの形成方法の一製造工程図である。

【符号の説明】

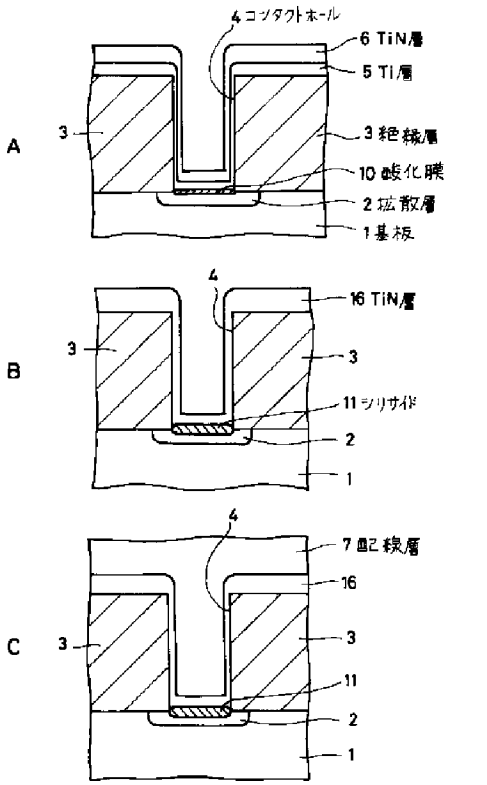
１　基板
２　拡散層
３　絶縁層
４　コンタクトホール
５　Ｔｉ層
６　ＴｉＮ層
７　配線層
１０　酸化膜
１１　シリサイド

【図１】



本発明メタルプラグの形成方法の一例の工程(その1)

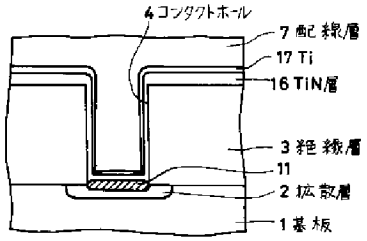
【図２】



本発明メタルプラグの形成方法の一例の工程図(その2)

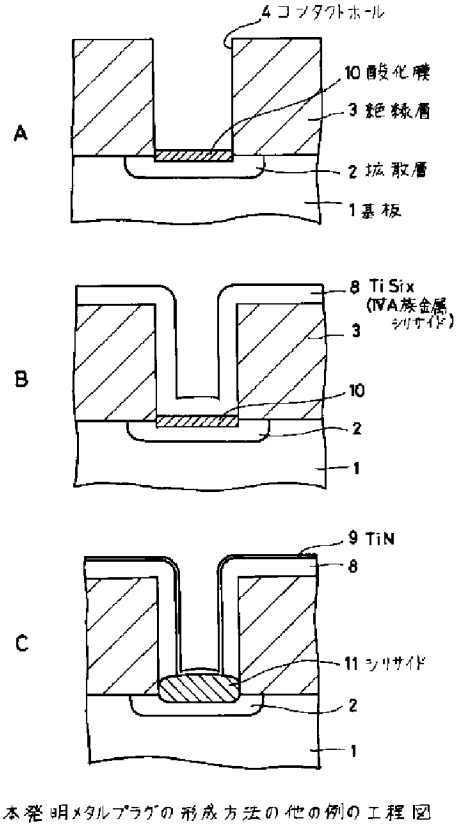
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【図3】



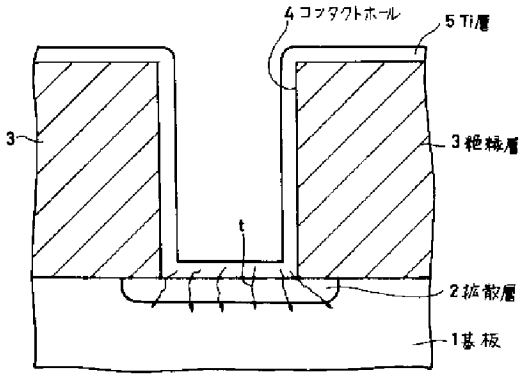
本発明メタルプラグの形成方法の他の例の一工程図

【図4】



本発明メタルプラグの形成方法の他の例の工程図

【図5】



従来のメタルプラグの形成方法の一工程図

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JPH0653165A METHOD OF FORMING METAL PLUG

Applicants: SONY CORP

Inventors: MIYAMOTO TAKAAKI,SUMI HIROBUMI

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Published as: JPH0653165A

METHOD OF FORMING METAL PLUG

Abstract

PURPOSE:To provide a metal plug in which leakage current is decreased by preventing chromium from entering silicon in the process for depositing titanium on silicon using a source gas that contains chromium.
CONSTITUTION:A method of forming a metal plug to lay an interconnection in a contact hole opened in a semiconductor layer comprises the steps of depositing a thin oxide 10 on the bottom of a contact hole 4; and depositing a group IVA metal 5, such as Ti, Zr or Hf, in the contact hole by CVD to form an interconnection.

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DESCRIPTION JPH0653165

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a method for forming a metal plug in a connection portion of a semiconductor layer of various semiconductor devices with a wiring layer.

[0002]
2. Description of the Related Art In high density semiconductor devices such as VLSI, contact holes are being miniaturized. A technique for burying a wiring layer such as Al in the fine contact holes is to improve the fluidity of Al at high temperature. A high-temperature Al sputtering method using Al, or a CVD (chemical vapor deposition) method having better coverage than the sputtering method is used to deposit W (tungsten), which has a higher temperature heat resistance than Al, over the entire surface including the contact hole. The BLK (blanket) -W CVD method and the like are currently widely used.

[0003]

It is necessary to form a low-resistance semiconductor-metal junction (ohmic process) having no rectifying property in any of the processes of the high temperature Al sputtering method and the BLK-W CVD method.

Therefore, in both of the above-described high temperature Al sputtering method BLK-W CVD

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method, titanium Ti which has a relatively low contact resistance among the refractory metals and can reduce the silicon oxide film is used between the semiconductor layer and the wiring layer. The method of forming is adopted.

[0004]
Titanium has a lower free energy of formation than that of silicon oxide, that is, it is more stable when titanium oxide is formed. Therefore, titanium has the ability to reduce silicon oxide as described above. When the thickness is thin or the silicon oxide film is thick, titanium cannot reduce silicon oxide, and low ohmic contact resistance cannot be obtained (for example, the 38th JSAP Spring Meeting of Applied Physics Proceedings p.691).).

[0005]
In addition, since titanium is usually deposited by the sputtering method, if an attempt is made to deposit it in a fine contact hole with a high aspect ratio, a titanium film sufficient to reduce the natural silicon oxide film on the diffusion layer at the bottom of the contact hole. There is a problem that the thickness cannot be obtained and the low contact resistance cannot be obtained.

[0006]

Therefore, it has been attempted to deposit titanium in the contact hole by the chemical vapor deposition method instead of the sputtering method.

For example, titanium has been tried to be formed into a film by many methods such as ECR (electron cyclotron resonance) plasma CVD method, thermal CVD method, MOCVD (chemical vapor deposition by metal organic) method. There is a problem that a suitable organic material capable of forming a film is not found, and the thermal CVD method requires a high temperature of about 1000 ° C. or higher, which makes it difficult to apply to the manufacture of LSI.

[0007]
Therefore, at present, Ti film formation by a TiCl4 + H2 system ECR plasma CVD method utilizing promotion of dissociation of TiCl4 by ECR plasma and TiSi2 film formation by a TiCl4 + SiH4 system thermal CVD method are performed.

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[0008]
However, since these methods use a TiCl4 source, there is a problem that Cl in TiCl4 or generated HCl corrodes the silicon diffusion layer at the bottom of the contact hole (for example, "Extended Abstracts of 1991 Inter-national"). Conference on Solid State Devices and Materials, Yokohama, 1991, pp210-212 ").

[0009]
For example, as shown in FIG. 5, a diffusion layer 2 is formed on a substrate 1 made of Si or the like, an insulating layer 3 made of thick SiO2 or the like is deposited, and a contact hole 4 having a depth reaching the diffusion layer 2 is opened. After that, when the Ti layer 5 is deposited by the above-mentioned TiCl4 + H2 system ECR plasma CVD method, Si of the diffusion layer 2 is scraped off by HCl and Ti is eroded as shown by an arrow t, so that the diffusion layer 2 and the substrate 1 There is a risk of junction breakdown between them and an increase in leak current.

[0010]
The present invention provides a method for forming a metal plug capable of forming a barrier metal such as Ti so that such erosion of the Si diffusion layer does not occur.

[0011]
According to the present invention, in a method of forming a metal plug in which a wiring layer is embedded in a contact hole opened on a semiconductor layer, an example of manufacturing process charts thereof is shown in FIGS. After forming a thin oxide film 10 on the bottom of the contact hole 3, a group IVA metal of Ti, Zr, or Hf, for example, a Ti layer 5 is deposited in the contact hole 3 by a CVD method, and a wiring layer is deposited. To do.

[0012]
Still another aspect of the present invention is a method of forming a metal plug in which a wiring layer is embedded in a contact hole opened on a semiconductor layer, and a metal plug is formed on the bottom of the contact hole 3 as shown in FIGS. After forming the thin oxide film 10, a group IVA metal silicide of TiSix, ZrSix or HfSix, for example, a TiSix layer 8 is deposited in the contact hole 3 by the CVD method to form a wiring layer.

[0013]
Further, according to the present invention, in the method of forming a metal plug shown in FIGS.

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[0014]
Furthermore, the present invention is the method for forming a metal plug shown in FIGS. 4A to 4C, in which the above-mentioned group IVA metal silicide, for example, TiSiX layer 8 is formed by a thermal CVD method.

[0015]
As described above, according to the method of forming a metal plug of the present invention, a thin oxide film is formed on the bottom of the contact hole 3, and then a group IVA metal or a group IVA metal silicide is formed thereon by a CVD method. Therefore, by forming a thin oxide film that is not easily eroded by Cl during film formation, erosion of Si can be avoided and leak current can be reduced.

[0016]
In addition, since the group IVA metal, that is, Ti, Zr, and Hf has the reducing ability of the Si oxide film, the oxide film is reduced by the subsequent heat treatment, and silicide having excellent heat resistance can be formed, resulting in low contact resistance. A metal plug having excellent coverage can be formed.

[0017]
Furthermore, by adopting the ECR plasma CVD method as the film forming method of the group IVA metal and the thermal CVD method as the film forming method of the group IVA metal silicide, it is possible to obtain a desired film thickness with good embedding even in a contact hole having a fine shape. It can be formed, and the natural oxide film on the diffusion layer therebelow can be sufficiently reduced, and good contact resistance can be obtained.

[0018]

Embodiments of the present invention will now be described in detail with reference to the drawings.

In each example, a case is shown in which an impurity diffusion layer is provided on a semiconductor layer made of a Si substrate or the like, and a wiring layer is connected thereon.

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[0019]

Example 1 In this example, a thin oxide film is deposited in advance when the Ti layer is formed by the ECR plasma CVD method. First, as shown in FIG. 1A, on a substrate 1 made of Si or the like. Impurities and the like are implanted at predetermined positions to form the diffusion layer 2.

After that, an insulating layer 3 of SiO2 or the like is thickly deposited by a CVD method or the like, and a fine contact hole 4 having a diameter of about 0.4 .mu.m to 0.6 .mu.m is opened at a depth reaching the diffusion layer 2.

[0020]

Next, as shown in FIG. 1B, a thin SiO2 oxide film 10 having a thickness of about 3 to 5 nm is formed on the bottom of the contact hole 4, that is, the upper portion of the diffusion layer 2 by thermal oxidation or the like.

As the oxidizing conditions, for example, the oxygen flow rate can be 10 l / min, the substrate temperature can be 850 ° C., and the processing time can be 5 to 10 min.

[0021]

Then, as shown in FIG. 1C, an IVA group metal, for example, a Ti layer 5 is deposited over the entire surface by a CVD method.

In this case, the thickness is about 30 nm and deposited by the ECR plasma CVD method using TiCl4 + H2 system.

The ECR plasma CVD conditions were a substrate temperature of 420 ° C. to 540 ° C., a microwave power of 2.8 kW, TiCl4 and H2 flow rates of 10 sccm and 50 sccm, respectively, and an Ar flow rate of 43 sccm.

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[0022]

Since the bond energy between Si-Si atoms is 76 kcal / mol and the bond energy between Si-Cl is 77 kcal / mol, as described above, according to the conventional method, Cl in TiCl4 of the Ti film forming material is used. As a result, the underlying Si diffusion layer is easily eroded.

On the other hand, the bond energy between Si and O is relatively high at 192 kcal / mol. According to the present invention, since such a stable SiO2 film is formed in advance, the underlying Si is not corroded by Cl. It is possible to surely avoid breaking the junction between the diffusion layer and the substrate.

[0023]

Then, as shown in FIG. 2A, a TiN layer 6 is deposited over the entire surface by ECR plasma CVD to a thickness of, for example, 70 nm.

In this case, the substrate temperature was 420 ° C. to 540 ° C., the microwave power was 2.8 kW, and the flow rates of TiCl4, N2, H2, and Ar were 10, 15, 50, and 43 sccm, respectively.

[0024]

After that, two-stage annealing is performed to react Ti with the underlying Si diffusion layer through the SiO2 oxide film at the bottom of the contact hole 4 to form a silicide 11 such as TiSix (titanium silicide). To do.

In this case, the first annealing was performed in Ar atmosphere at a substrate temperature of 650 ° C. for 30 seconds, and the second annealing was performed in N 2 at 900 ° C. for 30 seconds.

Thus, by introducing nitrogen in the second annealing treatment, the Ti layer on the side wall of the contact hole 4 and the insulating layer 3 is nitrided, and the TiN layer 16 is entirely covered

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including the silicide 11 in the contact hole 4. Is formed.

[0025]

As described above, the group IVA metal such as Ti is more stable when the metal oxide is formed than when the Si oxide is formed, and thus the Si oxide can be reduced.

As described above, it is possible to form a silicide film having excellent high temperature heat resistance by annealing through a thin oxide film having a thickness of about 3 to 5 nm, for example, Japanese Patent Application Laid-Open No. 3-38823 of the present applicant. Japanese Patent Laid-Open Publication No. 4-34926, etc.

In the present invention, particularly, by forming a group IVA metal or a group IVA metal silicide on the oxide film 10 by the CVD method, a good film can be formed even in a contact hole having a high aspect ratio.

[0026]

Further, as shown in FIG. 2C, for example, BLK-W is buried and formed by a CVD method to form a wiring layer 7 to form a metal plug.

In this case, the deposition conditions were, for example, a substrate temperature of 450 ° C., a pressure of 1 × 10 4 Pa, a flow rate of WF 6 of 95 sccm, and a flow rate of H 2 of 550 sccm.

[0027]

Alternatively, the wiring layer 7 made of Al may be formed as shown in FIG. 3 by using, for example, a high temperature Al sputtering method without using the BLK-W. In FIG. 3, parts corresponding to those in FIGS. 1 and 2 are denoted by the same reference numerals, and redundant description will be omitted. In this case, the natural oxide film formed spontaneously on the surface of the TiN layer 16 is removed by etching by reverse sputtering, and then the Ti layer 17 and the wiring layer 7 made of Al for improving the wettability with Al. By sequentially

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depositing and without sequentially exposing them to the atmosphere, the embedding can be satisfactorily performed. The reverse sputtering conditions are as follows: the RF voltage is 1000 V, the substrate temperature is 200 ° C., the flow rate of Ar is 50 sccm, and the pressure is 0.5 Pa. The sputtering conditions for the Ti layer 17 are DC 4 kW, substrate temperature 150 ° C., and Ar. The flow rate was 100 sccm, the pressure was 0.5 Pa, the Al sputtering conditions were a substrate temperature of 480 ° C. to 500 ° C., the Ar flow rate was 100 sccm, and the pressure was 0.5 Pa.

[0028]

As described above, after the SiO2 oxide film 10 is thinly formed in the contact hole 4, Ti is formed by the ECR plasma CVD method or the like to form a metal plug with good adhesion even in the fine contact hole 4. be able to.

[0029]

Second Embodiment Next, another embodiment according to the present invention will be described with reference to FIGS.

In this example, when TiSix is formed by the thermal CVD method, a method of forming a thin oxide film in advance is applied.

[0030]

First, as shown in FIG. 4A, after forming a diffusion layer 2 on a substrate 1 made of Si or the like, a thick insulating layer 3 such as SiO2 is formed, and a fine contact hole 4 of about 0.4 .mu.m to 0.6 .mu.m is formed. Are opened by applying photolithography or the like. Then, similarly to the above-described embodiment, that is, by thermal oxidation or the like, a thin SiO2 oxide film 10 having a thickness of about 3 to 5 nm is formed on the bottom of the contact hole 4, that is, on the diffusion layer 2. As the oxidizing conditions, for example, the oxygen flow rate can be 10 l / min, the substrate temperature can be 850 ° C., and the processing time can be 5 to 10 min.

[0031]

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After that, as shown in FIG. 4B, a TiSix layer 8 of a group IVA metal silicide is formed on the entire surface by TiCl4 + SiH4 system thermal CVD. At this time, TiSix has a Ti-rich composition, that is, the composition ratio of Si to Ti is set to 1.0 to 1.8 which is smaller than 2.0, for example, about 1.8, and the deposition temperature is set to a substrate temperature of 500 ° C. For example, the temperature is set to about 700 ° C. and the flow ratio of SiH4 to TiCl4 is set to 5 to 10 (SiH4 / TiCl4).

[0032]

Usually, when forming a TiSiX film on a silicon substrate in this way, the composition is Si-rich in order to suppress stress, and the Si composition ratio x is set to about 2.6. The Si composition ratio is set to about 1.8 or less so that the lower SiO2 oxide film 10 can be sufficiently reduced. The reason why the Si composition ratio is set to 1.0 or more is that when the composition ratio is less than 1.0, film formation is performed by the thermal CVD method. Incidentally, TiSix can also be formed by, for example, the ECR plasma CVD method.

[0033]

Thus, by depositing TiSix in a Ti-rich composition and then siliciding, Si in the oxide film 10 can be completely reacted, and a good silicide 11 having excellent heat resistance can be formed. As in the first embodiment, by forming the thin oxide film 10 in advance, it is possible to suppress the erosion of Si by Cl during the TiSiX film formation.

[0034]

Then, after that, annealing is performed for 30 seconds at a substrate temperature of 900 ° C. in an NH3 atmosphere.

At this time, TiSiX (x = 1.0 to 1.8) reacts with the underlying Si diffusion layer 2 through the SiO2 oxide film 10, and a thick silicide 11 is formed at the bottom of the contact hole 4 as shown in FIG. 4C. It is formed. This silicide 11, that is, TiSix, has a so-called stoichiometric x = 2.0 composition according to the chemical formula. The surface of the TiSix layer 8 is nitrided and a thin TiN layer 9 is formed.

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[0035]
Then, after this, similarly to the first embodiment, a wiring layer is formed by BLK-W or a high temperature Al sputtering method or the like, and a metal plug can be formed with good adhesion even in the fine contact hole 4. it can.

[0036]

In each of the above-mentioned examples, the case where the contact hole is provided on the diffusion layer of the semiconductor device has been described, but the present invention can be applied to the formation of various metal plugs such as the connection portion on the polysilicon gate. Needless to say.

Further, in each of the above-mentioned examples, the metal plug is formed by using Ti, but the same effect can be obtained when using other group IVA metals Zr and Hf. Further, the forming method is not limited to the above-mentioned methods, and it goes without saying that various modifications and changes can be made in temperature, reaction gas flow rate and the like.

[0037]

As described above, according to the method of the present invention, after the SiO2 oxide film is formed in advance, Ti or TiSiX is formed by the CVD method, so that Si contained in the film forming material erodes Si. That is, it is possible to form a metal plug having excellent coverage and low leakage current. In particular, the contact resistance can be reduced by forming a film of Ti or TiSix and then annealing it to silicide the SiO2 oxide film.

[0038]
Further, particularly when TiSi is formed, the composition rich in Ti can surely reduce the oxide film to silicidize and form a metal plug having low contact and excellent heat resistance.

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CLAIMS JPH0653165

1.
In a method of forming a metal plug in which a wiring layer is embedded in a contact hole opened on a semiconductor layer, a thin oxide film is formed on the bottom of the contact hole, and then a group IVA metal is deposited in the contact hole by chemical vapor deposition. A method for forming a metal plug, which comprises depositing and depositing a wiring layer.

2.
In a method of forming a metal plug in which a wiring layer is buried in a contact hole opened on a semiconductor layer, a thin oxide film is formed on the bottom of the contact hole, and then a chemical vapor deposition method is used to deposit a group IVA metal silicide in the contact hole. And depositing a wiring layer to form a metal plug.

3.
The method for forming a metal plug according to claim 1, wherein the Group IVA metal is formed by a chemical vapor deposition method using electron cyclotron resonance plasma.

4.
The method for forming a metal plug according to claim 2, wherein the group IVA metal silicide is formed by a thermochemical vapor deposition method.

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21/265		29/165		５Ｆ００３
29/165		29/78	６５２Ｔ	５Ｆ００５
21/331			６５２Ｍ	５Ｆ０４１
29/73		33/00	Ｅ	５Ｆ１０２

審査請求　未請求　請求項の数21　ＯＬ　（全 31 頁）　最終頁に続く

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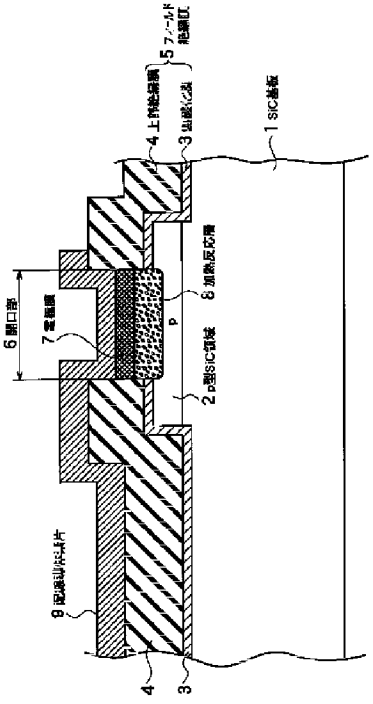
（出願人による申告）国等の委託研究の成果に係わる特許出願（平成12年度新エネルギー・産業技術総合開発機構「超低損失電力素子技術開発　基盤技術開発」に係わる委託研究、産業再生特別措置法第30条の適用を受けるもの）

(71)出願人　301021533
独立行政法人産業技術総合研究所
東京都千代田区霞が関１－３－１
(74)上記１名の復代理人　100083806
弁理士　三好　秀和　（外８名）
(71)出願人　000003997
日産自動車株式会社
神奈川県横浜市神奈川区宝町２番地
(74)上記１名の代理人　100083806
弁理士　三好　秀和　（外８名）
(72)発明者　大串　秀世
茨城県つくば市梅園１丁目１番４　工業技術院電子技術総合研究所内

最終頁に続く

(54)【発明の名称】　オーミック電極構造体、その製造方法、及びオーミック電極を用いた半導体装置

(57)【要約】
【課題】　微細なコンタクト・ウインドウの内部において、ｐ型ＳｉＣ領域への低いコンタクト抵抗ρｃを実現する。
【解決手段】　ＳｉＣ基板１、ＳｉＣ基板１の表面に形成されたｐ型ＳｉＣ領域２、このｐ型ＳｉＣ領域２の表面に形成された加熱反応層８、ＳｉＣ基板１とｐ型ＳｉＣ領域２との界面を覆う熱酸化膜３、熱酸化膜３の表面に配置された上部絶縁膜４、加熱反応層８の上部に配置された電極膜７とを有する。電極膜７には、配線導体素片９が接続されている。加熱反応層８は、ｐ型ＳｉＣ領域２の表面から上方に突出して形成されている。熱酸化膜３は、加熱反応層８が貫通する開口部を有し、且つＳｉＣ基板１とｐ型ＳｉＣ領域２との界面を覆うように、ＳｉＣ基板１の表面に接して配置されている。上部絶縁膜４は、熱酸化膜３とは組成若しくは密度の異なる絶縁膜である。



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【特許請求の範囲】
【請求項１】　炭化珪素（ＳｉＣ）基板と、
該ＳｉＣ基板の表面に選択的に形成されたｐ型ＳｉＣ領域と、
該ｐ型ＳｉＣ領域の表面の一部から内部に進入し、且つ該ｐ型ＳｉＣ領域の表面から上方に突出して形成された加熱反応層と、
該加熱反応層が貫通する第１の開口部を有し、前記ＳｉＣ基板と前記ｐ型ＳｉＣ領域の表面に接して配置された熱酸化膜と、
該熱酸化膜とは組成若しくは密度の異なる絶縁膜であって、前記第１の開口部に連続した第２の開口部を有し、且つ前記熱酸化膜の表面に配置された上部絶縁膜と、
該上部絶縁膜の前記第２の開口部において、前記加熱反応層の上部に配置されたＡｌ及びＴｉの少なくとも一方を含む金属からなる電極膜とからなることを特徴とするオーミック電極構造体。
【請求項２】　前記電極膜は、下部のチタン・シリコン（Ｔｉ－Ｓｉ）合金膜と上部のチタン（Ｔｉ）膜とからなる積層膜、下部のアルミニウム・シリコン（Ａｌ－Ｓｉ）合金膜と上部のアルミニウム（Ａｌ）膜とからなる積層膜、及び下部のアルミニウム・チタン・シリコン（Ａｌ－Ｔｉ－Ｓｉ）合金膜と上部のアルミニウム・チタン（Ａｌ－Ｔｉ）合金膜とからなる積層膜からなるグループの内の少なくとも一つの積層膜を含む金属膜であることを特徴とする請求項１記載のオーミック電極構造体。
【請求項３】　前記加熱反応層は、金属の炭化物と金属シリコン（Ｓｉ）とを含む固溶体であることを特徴とする請求項１又は２記載のオーミック電極構造体。
【請求項４】　前記上部絶縁膜の絶縁破壊電界強度は、前記熱酸化膜の絶縁破壊電界強よりも低いことを特徴とする請求項１～３のいずれか１項記載のオーミック電極構造体。
【請求項５】　前記上部絶縁膜の緩衝フッ酸溶液によるエッチング速度が、前記熱酸化膜の前記緩衝フッ酸溶液によるエッチング速度よりも速いことを特徴とする請求項１～４のいずれか１項記載のオーミック電極構造体。
【請求項６】　前記ｐ型ＳｉＣ領域の表面キャリア密度は、1×10^{18}／ｃｍ^3～5×10^{21}／ｃｍ^{3}であることを特徴とする請求項１～５のいずれか１項記載のオーミック電極構造体。
【請求項７】　前記熱酸化膜の厚さは２～５０ｎｍであることを特徴とする請求項１～６のいずれか１項記載のオーミック電極構造体。
【請求項８】　前記熱酸化膜の厚さと前記上部絶縁膜の厚さとを合計した値は、１００ｎｍ～３μｍであることを特徴とする請求項１～７のいずれか１項記載のオーミック電極構造体。
【請求項９】　前記電極膜の最上部の位置が、前記第２の開口部の内部に存在することを特徴とする請求項１～８のいずれか１項記載のオーミック電極構造体。
【請求項１０】　炭化珪素（ＳｉＣ）基板の表面の少なくとも一部に高不純物密度を有するｐ型ＳｉＣ領域を形成する工程と、
前記ＳｉＣ基板の表面を洗浄する工程と、
前記ＳｉＣ基板の表面をフィールド絶縁膜で被覆する工程と、
前記ｐ型ＳｉＣ領域の少なくとも一部を露出するように、前記フィールド絶縁膜に開口部を形成する工程と、
前記開口部の内部にＡｌ－Ｔｉ系電極膜を配設する工程と、
酸素（O_2）及び水（H_2O）の分圧が共に1×10^{-3}Ｐａ～1×10^{-10}Ｐａの非酸化性雰囲気中において、前記ＳｉＣ基板を熱処理し、前記Ａｌ－Ｔｉ系電極膜と前記ＳｉＣ基板との加熱反応層を生成する工程とを有することを特徴とするオーミック電極構造体の製造方法。
【請求項１１】　前記フィールド絶縁膜で被覆する工程は、
熱酸化により、前記ＳｉＣ基板の表面に熱酸化膜を成長する工程と、
該熱酸化膜の上部に、熱酸化以外の方法で、絶縁膜を堆積する工程とからなることを特徴とする請求項１０記載のオーミック電極構造体の製造方法。
【請求項１２】　前記フィールド絶縁膜で被覆する工程は、
熱酸化以外の方法で、前記ＳｉＣ基板の表面に酸素透過性絶縁膜を堆積する工程と、
該酸素透過性絶縁膜の堆積後に、熱酸化により、前記ＳｉＣ基板の表面と前記酸素透過性絶縁膜との界面に、熱酸化膜を成長する工程とからなることを特徴とする請求項１０記載のオーミック電極構造体の製造方法。
【請求項１３】　炭化珪素（ＳｉＣ）基板の表面の少なくとも一部に高不純物密度を有するｐ型ＳｉＣ領域を形成する工程と、
前記ＳｉＣ基板の表面を洗浄する工程と、
熱酸化以外の方法で、前記ＳｉＣ基板の表面に酸素透過性絶縁膜を堆積する工程と、
前記ｐ型ＳｉＣ領域の一部を選択的に露出するように、前記酸素透過性絶縁膜に開口部を形成する工程と、
該開口部を形成する工程後に、熱酸化により、該開口部に露出した前記ＳｉＣ基板の表面、及び前記ＳｉＣ基板の表面と前記酸素透過性絶縁膜との界面に、熱酸化膜を成長する工程と、
前記開口部に成長した前記熱酸化膜を除去する工程と、
前記熱酸化膜が除去された前記開口部の内部に、アルミニウム・チタン（Ａｌ－Ｔｉ）系電極膜を配設する工程と、
非酸化性雰囲気中において、前記ＳｉＣ基板を熱処理し

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前記Ａｌ－Ｔｉ系電極膜と前記ＳｉＣ基板との加熱反応層を生成する工程とを有することを特徴とするオーミック電極構造体の製造方法。

【請求項１４】　前記加熱反応層を生成する工程は、酸素（O_2）及び水（H_2O）の分圧が共に1×10^{-3}Ｐａ～1×10^{-10}Ｐａである雰囲気中で実施されることを特徴とする請求項１３記載のオーミック電極構造体の製造方法。

【請求項１５】前記Ａｌ－Ｔｉ系電極膜を配設する工程は、

アルミニウム（Ａｌ）層の上にチタン（Ｔｉ）層を堆積する工程、

Ｔｉ層の上にＡｌ層を堆積する工程、

アルミニウム・チタン（Ａｌ－Ｔｉ）合金膜を堆積する工程からなるグループの内の少なくとも一つの工程を含むことを特徴とする請求項１０～１４のいずれか１項記載のオーミック電極構造体の製造方法。

【請求項１６】　前記開口部を形成する工程は、

フォトリソグラフィ法により、前記フィールド絶縁膜の上部にエッチングマスクを形成する工程と、

該エッチングマスクを用いて、前記ｐ型ＳｉＣ領域の少なくとも一部の上部に前記フィールド絶縁膜が残留するように、前記フィールド絶縁膜の一部をドライ・エッチングで除去する工程と、

残留した前記フィールド絶縁膜をウェット・エッチングで除去し、前記ｐ型ＳｉＣ領域の少なくとも一部を露出する工程と、

超純水によるリンスで、露出した前記ｐ型ＳｉＣ領域を清浄化する工程とからなることを特徴とする請求項１０～１２のいずれか１項記載のオーミック電極構造体の製造方法。

【請求項１７】　前記Ａｌ－Ｔｉ系電極膜を配設する工程は、

前記エッチングマスクが、前記フィールド絶縁膜の上部に残留した状態で、前記Ａｌ－Ｔｉ系電極膜を前記エッチングマスクの上部及び前記開口部を含む全面に堆積する工程と、

該全面に堆積する工程の後、前記エッチングマスクを除去することにより、前記Ａｌ－Ｔｉ系電極膜を前記開口部の内部にのみ選択的に残留させる工程とからなることを特徴とする請求項１６記載のオーミック電極構造体の製造方法。

【請求項１８】　前記開口部を形成する工程は、

フォトリソグラフィ法により、前記酸素透過性絶縁膜の上部にエッチングマスクを形成する工程と、

該エッチングマスクを用いて、前記ｐ型ＳｉＣ領域の少なくとも一部の上部に前記酸素透過性絶縁膜が残留するように、前記酸素透過性絶縁膜の一部を除去する工程と、

残留した前記酸素透過性絶縁膜をウェット・エッチングで除去し、前記ｐ型ＳｉＣ領域の少なくとも一部を露出する工程と、

超純水によるリンスで、露出した前記ｐ型ＳｉＣ領域を清浄化する工程とからなることを特徴とする請求項１３又は１４記載のオーミック電極構造体の製造方法。

【請求項１９】炭化珪素（ＳｉＣ）基板と、

該ＳｉＣ基板の表面に選択的に形成された主電極領域として機能するｐ型ＳｉＣ領域と、

該ｐ型ＳｉＣ領域の表面の一部から内部に進入し、且つ該ｐ型ＳｉＣ領域の表面から上方に突出して形成された加熱反応層と、

該加熱反応層が貫通する第１の開口部を有し、前記ＳｉＣ基板と前記ｐ型ＳｉＣ領域の表面に接して配置された熱酸化膜と、

該熱酸化膜とは組成若しくは密度の異なる絶縁膜であって、前記第１の開口部に連続した第２の開口部を有し、且つ前記熱酸化膜の表面に配置された上部絶縁膜と、

該上部絶縁膜の前記第２の開口部において、前記加熱反応層の上部に配置されたＡｌ及びＴｉの少なくとも一方を含む金属からなる電極膜と、

該電極膜に接続される主電極配線とからなることを特徴とする半導体装置。

【請求項２０】　前記電極膜は、下部のチタン・シリコン（Ｔｉ－Ｓｉ）合金膜と上部のチタン（Ｔｉ）膜とからなる積層膜、下部のアルミニウム・シリコン（Ａｌ－Ｓｉ）合金膜と上部のアルミニウム（Ａｌ）膜とからなる積層膜、及び下部のアルミニウム・チタン・シリコン（Ａｌ－Ｔｉ－Ｓｉ）合金膜と上部のアルミニウム・チタン（Ａｌ－Ｔｉ）合金膜とからなる積層膜からなるグループの内の少なくとも一つの積層膜を含む金属膜であることを特徴とする請求項１９記載の半導体装置。

【請求項２１】　前記加熱反応層は、金属の炭化物と金属シリコン（Ｓｉ）とを含む固溶体であることを特徴とする請求項１９又は２０記載の半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、炭化珪素（ＳｉＣ）基板を使用した半導体装置に係り、更には、このＳｉＣ半導体装置に利用されるｐ型ＳｉＣ領域に対するオーミック電極構造体及びその製造方法に関するものである。

【０００２】

【従来の技術】ＳｉＣは、ｐｎ接合の形成が可能で、珪素（Ｓｉ）や砒化ガリウム（ＧａＡｓ）等の他の現在広く実用化されている半導体材料に比べて禁制帯幅Ｅｇが広く３Ｃ－ＳｉＣで２．２３ｅＶ、６Ｈ－ＳｉＣで２．９３ｅＶ、４Ｈ－ＳｉＣで３．２６ｅＶ程度の値が報告されている。また、ＳｉＣは、熱的、化学的、機械的に安定で、耐放射線性にも優れているので、発光素子や高周波デバイスは勿論のこと、高温、大電力、放射線照射

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等の過酷な条件で、高い信頼性と安定性を示す電力用半導体装置（パワーデバイス）として様々な産業分野での適用が期待されている。

【０００３】特に、ＳｉＣを用いた高耐圧のＭＯＳＦＥＴは、Ｓｉを用いたパワーデバイスよりもオン抵抗が低いことが報告されている。また、ショットキーダイオードの順方向降下電圧が低くなることが報告されている。良く知られているように、パワーデバイスのオン抵抗とスイッチング速度とは、トレード・オフ関係にある。しかし、ＳｉＣを用いたパワーデバイスによれば、低オン抵抗化と高速スイッチング速度化が同時に達成できる可能性がある。

【０００４】このＳｉＣを用いたパワーデバイスの低オン抵抗化には、オーミック・コンタクトに対するコンタクト抵抗ρｃの低減が重要な要素である。特に、低オン抵抗化のためには、パワーデバイスの主電極領域を細分化し、高密度にＳｉＣ基板上に配列する方法も採用される。このような、微細寸法化されたパワーデバイスの低オン抵抗化には、微細な開口部（コンタクト・ウインドウ）の内部において、低いコンタクト抵抗ρｃを得ることが極めて重要となってくる。また、パワーデバイスの高速スイッチング速度化のためにも、ｐ型ＳｉＣ領域に対するオーミック・コンタクトのコンタクト抵抗ρｃは大きな問題である。

【０００５】ＳｉＣ青色発光素子がすでに実用化され量産されているのとは対称的に、パワーデバイス、高周波デバイスとしてのＳｉＣの応用は甚だ遅れている。この原因の一つは、これらデバイスの構造及び作製プロセスに適合した実用的な低抵抗のオーミック・コンタクトを形成する技術がいまだに確立されていないからである。ＳｉＣチップのほぼ全面に形成されたオーミック・コンタクト面に対して均一に電流が流れるＳｉＣ青色発光素子に対して、電導チャネルに近接する微細なコンタクト・ウインドウ中のオーミック・コンタクトを介して主電流が流れる半導体電子デバイス（半導体装置）では、コンタクト抵抗ρｃの低減が極めて重要である。即ち、オーミック・コンタクトが形成された局所的な領域に集中して主電流が流れるパワーデバイスや高周波デバイスでは、桁違いに低いコンタクト抵抗ρｃが、デバイス特性の高性能化に対して求められているからである。

【０００６】具体例を挙げて説明すると、ＳｉＣ青色発光素子のｐ型ＳｉＣエピタキシャル層に低抵抗オーミック・コンタクトを形成する方法として利用されている従来技術として特許第２９１１１２２号公報に記載された方法がある（以下において「第１の従来技術」という。）」。この第１の従来技術は、ウェット・エッチングにより表面処理したｐ型ＳｉＣ表面上に、ＳｉＣよりも強く酸素と反応する金属、例えばＴｉ薄膜電極を、真空蒸着法を用いて５０ｎｍ程度成膜し、続いて、この上にＡｌ－Ｔｉ系電極膜を成膜した後、斯かる積層基板を、８００～１０００℃、例えば９５０℃で５分程度熱処理するもので、ＳｉＣ表面の自然酸化膜に妨げられることなく基板のどの地点でも均一なオーミック・コンタクトを形成することが出来る。

【０００７】しかしながら、第１の従来技術は、電極層のオーミック性が完全なものではなかった。例えば、電極層間の電流－電圧特性を厳密に測定すると、電流－電圧特性を示す線は曲線となり、そのオーミック性は不完全なものであることが、特開平７－１６１６５８号公報の中で指摘されている。このような構成のオーミック・コンタクトは電流密度が高くなると大きな寄生抵抗を生むことになるので、パワーデバイスや高周波デバイスなどの半導体電子デバイスへの使用には適さない。

【０００８】半導体電子デバイス用として広範囲に検討されている従来技術はｐ型ＳｉＣ領域の表面にＡｌを含む金属膜を高温で熱処理して、オーミック・コンタクトとする方法（以下において「第２の従来技術」という。）である。中でも、クロフトンら（アプライド・フィジックス・レターズ：Applied Physics Letters, 第６２巻、第３８４頁(１９９８年)）は、６Ｈ－ＳｉＣ基板の表面にエピタキシャル成長により、高不純物密度にドープしたｐ型ＳｉＣ層の上に、Ａｌ－Ｔｉ合金膜を堆積し、その後、熱処理を施す方法で、ρｃ＝１．５×１０$^{-5}$Ωｃｍ^{2}のオーミック・コンタクトが得られることを報告している。クロフトンらは、Ａｌ－Ｔｉ合金膜のパターニングにリフトオフ法を用いている。クロフトンらの方法は、概略以下のような工程である。即ち、

（イ）先ず、フォトリソグラフィ法に形成した第１のフォトレジストをマスクとして、フィールド絶縁膜としての酸化膜を緩衝フッ酸（ＢＨＦ）溶液でエッチングし、開口部（コンタクト・ウインドウ）を形成する。フィールド絶縁膜のエッチング後、第１のフォトレジストを除去する。

【０００９】（ロ）その後、第２のフォトレジストをコンタクト・ウインドウを含む前面に塗布している。そして、フォトリソグラフィ法により、第２のフォトレジストをパターニングし、ｐ型ＳｉＣ層の表面を露出するように開口部を形成する。

【００１０】（ハ）その後、ｐ型ＳｉＣ層の表面を洗浄した後、全面に厚さ３００ｎｍ～５００ｎｍのＡｌ－Ｔｉ合金膜をスパッタリング法で成膜する。続いて、第２のフォトレジストをアセトンで溶解することによって、不要なＡｌ－Ｔｉ合金膜を第２のフォトレジストと共に除去して、Ａｌ－Ｔｉ合金膜をパターニングする。

【００１１】（ニ）そして、熱処理温度１０００℃において、アルゴン雰囲気で５分間熱処理する。

【００１２】

【発明が解決しようとする課題】しかしながら、上記の第１の従来技術のオーミック・コンタクトの構造ならびに作製プロセスは、平坦なＳｉＣ基板の表面にｐ型Ｓｉ

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Ｃオーミック・コンタクトを形成するという極めて単純化された構成をしている。このため、フィールド絶縁膜やゲート電極などその他の構造物が周辺に置かれる現実のデバイスの製作に適用するには具体性に欠けるという問題がある。そもそも第１の従来技術では電極パターニングの具体的方法がなんら開示されていないから、適用は困難である。

【００１３】また、第２の従来技術に開示されたオーミック・コンタクトを、トランジスタやダイオード等の実際の半導体電子デバイスに適用する場合は、クロフトンの得たρｃでも十分とは言い難く、より一層の低抵抗化が希求されている。そもそも、クロフトンが提示したリフトオフ法は、現像した時にフィールド絶縁膜の開口部にフォトレジストが残りやすく、これが低抵抗化の妨げになる。また、フォトレジストの残滓等は、コンタクト抵抗ρｃのばらつきの原因となる。

【００１４】本発明は第１及び第２の従来技術のｐ型ＳｉＣへのオーミック・コンタクトの問題を同時に解決するためになされたものであり、半導体電子デバイスに要求される$10^{-6}\Omega cm^2$台或いはこれ以下のコンタクト抵抗ρｃを有するオーミック電極構造体を提供することである。

【００１５】本発明の他の目的は、現実のデバイス構造に採用可能な微細な開口部（コンタクト・ウインドウ）の内部において、低いコンタクト抵抗ρｃを得ることが出来る単純化な構造のオーミック電極構造体を提供することである。

【００１６】本発明の更に他の目的は、高耐圧が要求される各種パワーデバイスに採用可能なフィールド絶縁膜の構造を維持しつつ、低いコンタクト抵抗ρｃを得ることが出来るオーミック電極構造体を提供することである。

【００１７】本発明の更に他の目的は、半導体電子デバイスに要求される$10^{-6}\Omega cm^2$台或いはこれ以下のコンタクト抵抗ρｃを有するオーミック電極構造体の製造方法を提供することである。

【００１８】本発明の更に他の目的は、現実のデバイス構造に採用可能な微細な開口部の内部において、低いコンタクト抵抗ρｃを簡単に得ることが出来るオーミック電極構造体の製造方法を提供することである。

【００１９】本発明の更に他の目的は、高耐圧が要求される各種パワーデバイスに採用可能なフィールド絶縁膜を形成すると共に、低いコンタクト抵抗ρｃが得られるオーミック電極構造体の製造方法を提供することである。

【００２０】本発明の更に他の目的は、微細な開口部の内部において、低いコンタクト抵抗ρｃを有し、高速・高周波動作可能な半導体装置を提供することである。

【００２１】本発明の更に他の目的は、オン電圧が低く、高速動作可能で、しかも動作電圧を高くすることが可能な半導体装置を提供することである。

【００２２】

【課題を解決するための手段】発明者らが鋭意、検討・考察した結果によれば、Ａｌ－Ｔｉ系電極膜とｐ型ＳｉＣ領域との間のオーミック・コンタクトにおいて、コンタクト抵抗ρｃを増大させる原因は

１）加熱反応層とｐ型ＳｉＣその接触によって必然的に出来るショットキー障壁の存在；

２）面内で不均一、不均質な加熱反応層の形成；

３）加熱反応層形成に際してＡｌ－Ｔｉ系電極膜表面に形成される金属酸化物である。

【００２３】上述した第１の従来技術が実用性に乏しかったのは、実際のデバイス構造とかけ離れて、平坦なＳｉＣ基板の表面にコンタクトを形成する構成になっていたためである。しかし実際の半導体電子デバイスでは、微細な開口部の内部においてショットキー障壁を低減化し、均一且つ均質な加熱反応層を生成する必要がある。以下に述べる本発明は、実際のデバイス構造の多くに適用されているフィールド絶縁膜の開口部に設けたｐ型ＳｉＣオーミック電極構造体において、上記コンタクト抵抗ρｃを高くしている３原因を解消するための手段を提供するものである。

【００２４】上記課題を解決するために、請求項１記載に係る発明は、（イ）ＳｉＣ基板と、（ロ）このＳｉＣ基板の表面に選択的に形成されたｐ型ＳｉＣ領域と、（ハ）このｐ型ＳｉＣ領域の表面の一部から内部に進入し、且つこのｐ型ＳｉＣ領域の表面から上方に突出して形成された加熱反応層と、（ニ）この加熱反応層が貫通する第１の開口部を有し、ＳｉＣ基板とｐ型ＳｉＣ領域の表面に接して配置された熱酸化膜と、（ホ）この熱酸化膜とは組成若しくは密度の異なる絶縁膜であって、第１の開口部に連続した第２の開口部を有し、且つ熱酸化膜の表面に配置された上部絶縁膜と、（ヘ）この上部絶縁膜の第２の開口部において、加熱反応層の上部に配置されたＡｌ及びＴｉの少なくとも一方を含む金属からなる電極膜とからなるオーミック電極構造体であることを要旨とする。後述するオーミック電極構造体の製造方法とも関連する事項であるが、このような、オーミック電極構造体の構造を採用することにより、清浄な金属／半導体接合界面が得られる。このため、金属／半導体接合におけるショットキー障壁が低く、且つ、界面のモホロジーが良好となる。

【００２５】なお、請求項１に規定する「ＳｉＣ基板の表面に選択的に形成されたｐ型ＳｉＣ領域」は、ＳｉＣ基板の表面に、直接ｐ型ＳｉＣ領域が形成される場合のみに限定されないことは勿論である。例えば、ＳｉＣ基板１の表面の一部に、ｐ型ＳｉＣ領域よりも平面上の面積の大きい他の半導体領域をウェル形状に配置し、そのウェル形状の半導体領域の内部の位置において、ｐ型ＳｉＣ領域が形成されていても良い。或いは、ＳｉＣ基板

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の表面の全面に他の半導体領域をエピタキシャル成長し、そのエピタキシャル成長した他の半導体領域の表面の一部において、ｐ型ＳｉＣ領域を形成するような場合も許容される。このように、請求項１記載に係る発明においては、ｐ型ＳｉＣ領域が他の半導体領域を介して、間接的に形成される場合を許容することに留意すべきである。

【００２６】請求項２記載に係る発明は、請求項１記載に係るオーミック電極構造体において、電極膜は、（ｉ）下部のＴｉ－Ｓｉ合金膜と上部のＴｉ膜とからなる積層膜、（ii）下部のＡｌ－Ｓｉ合金膜と上部のＡｌ膜とからなる積層膜、及び（iii）下部のＡｌ－Ｔｉ－Ｓｉ合金膜と上部のＡｌ－Ｔｉ合金膜とからなる積層膜からなるグループの内の少なくとも一つの積層膜を含む金属膜であることを要旨とする。後述するように、本発明は、（ｉ）Ａｌ層の上にＴｉ層を堆積したＡｌ／Ｔｉ積層膜、（ii）Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜、（iii）Ａｌ－Ｔｉ合金膜をｐ型ＳｉＣ領域との反応させ、加熱反応層を形成することにより、ショットキー障壁を極めて低く、且つ障壁の厚さを薄く出来る。また、加熱反応層が均一に生成される。請求項２記載に規定する電極膜の構造は、この加熱反応層の生成後の、未反応の金属層及び加熱反応層を拡散してきた金属Ｓｉとの化合部からなる積層構造である。即ち、（ｉ）Ａｌ層の上にＴｉ層を堆積したＡｌ／Ｔｉ積層膜においては、主に熱処理前の下層のＡｌ層が熱処理により加熱反応層となる。このとき、熱処理前の上層のＴｉ層の下部には、加熱反応層を拡散してきた金属Ｓｉとの反応により、Ｔｉ－Ｓｉ合金膜が生成される。この生成されたＴｉ－Ｓｉ合金膜と上部の未反応のＴｉ膜とからなる積層膜で請求項２記載に係る構造の電極膜を構成することになる。

【００２７】（ii）Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜においては、主に熱処理前のＴｉ層が熱処理により加熱反応層となり、熱処理前の上層のＡｌ層が、請求項２記載に係る構造の電極膜になる。この場合、電極膜は下部に、加熱反応層を拡散してきた金属Ｓｉとの反応によりＡｌ－Ｓｉ合金膜が生成され、上部に未反応のＡｌ膜が残留する。

【００２８】（iii）Ａｌ－Ｔｉ合金膜においては、主に熱処理前の下部のＡｌ－Ｔｉ合金膜が熱処理により加熱反応層となり、熱処理前の最上部には未反応のＡｌ－Ｔｉ合金膜が残るが、加熱反応層との境界部には、加熱反応層を拡散してきた金属Ｓｉとの反応によりＡｌ－Ｔｉ－Ｓｉ合金膜が生成される。このＡｌ－Ｔｉ－Ｓｉ合金膜／未反応のＡｌ－Ｔｉ合金膜とからなる積層構造が、請求項２記載に係る構造の電極膜を構成することになる。

【００２９】請求項３記載に係る発明は、請求項１又は２記載に係るオーミック電極構造体において加熱反応層は、金属の炭化物と金属シリコンとを含む固溶体であることを要旨とする。上述したＡｌ／Ｔｉ積層膜、Ｔｉ／Ａｌ積層膜、Ａｌ－Ｔｉ合金膜等のＡｌ－Ｔｉ系の金属とＳｉＣとは、種々の珪素化物（シリサイド）や炭化物（カーバイド）を含む合金を生成することが可能である。しかし、本発明者らの多くの実験結果によれば、これらの内、金属の炭化物と金属シリコンとを含む固溶体からなる加熱反応層が、金属／半導体接合におけるショットキー障壁が極めて低くなり、且つ、界面のモホロジーが良好で、加熱反応層が均一に生成されることが見いだされたのである。

【００３０】請求項４記載に係る発明は、請求項１～３のいずれか１項記載に係るオーミック電極構造体において、上部絶縁膜の絶縁破壊電界強度は、熱酸化膜の絶縁破壊電界強よりも低いことを要旨とする。

【００３１】請求項５記載に係る発明は、請求項１～４のいずれか１項記載に係るオーミック電極構造体において、上部絶縁膜のＢＨＦ溶液によるエッチング速度が、熱酸化膜のＢＨＦ溶液によるエッチング速度よりも速いことを要旨とする。「ＢＨＦ溶液」とは、周知のように、フッ化アンモニウム（NH_4F）：フッ酸（ＨＦ）＝７：１の溶液からなるシリコン酸化膜（SiO_2膜)のエッチング液（エッチャント）である。

【００３２】請求項６記載に係る発明は、請求項１～５のいずれか１項記載に係るオーミック電極構造体において、ｐ型ＳｉＣ領域の表面キャリア密度は、1×10^{18}／cm^3～5×10^{21}／cm^3であることを要旨とする。

【００３３】請求項７記載に係る発明は、請求項１～６のいずれか１項記載に係るオーミック電極構造体において、熱酸化膜の厚さは２～５０ｎｍであることを要旨とする。

【００３４】請求項８記載に係る発明は、請求項１～７のいずれか１項記載に係るオーミック電極構造体において、熱酸化膜の厚さと上部絶縁膜の厚さとを合計した値は、１００ｎｍ～３μｍであることを要旨とする。

【００３５】請求項９記載に係る発明は、請求項１～８のいずれか１項記載に係るオーミック電極構造体において、電極膜の最上部の位置が、第２の開口部の内部に存在することを要旨とする。

【００３６】請求項１０記載に係る発明は、（イ）ＳｉＣ基板の表面の少なくとも一部に高不純物密度を有するｐ型ＳｉＣ領域を形成する工程と、（ロ）ＳｉＣ基板の表面を洗浄する工程と、（ハ）ＳｉＣ基板の表面をフィールド絶縁膜で被覆する工程と、（ニ）ｐ型ＳｉＣ領域の少なくとも一部を露出するように、フィールド絶縁膜に開口部を形成する工程と、（ホ）開口部の内部にＡｌ－Ｔｉ系電極膜を配設する工程と、（ヘ）酸素及び水の分圧が共に1×10^{-3} Ｐａ～1×10^{-10} Ｐａの非酸化性雰囲気中において、ＳｉＣ基板を熱処理しＡｌ－Ｔｉ系電極膜とＳｉＣ基板との加熱反応層を生成する工程

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とを有するオーミック電極構造体の製造方法であることを要旨とする。

【００３７】なお、請求項１と同様に、請求項１０に規定する「ＳｉＣ基板の表面の少なくとも一部に高不純物密度を有するｐ型ＳｉＣ領域を形成する工程」は、ＳｉＣ基板の表面に、直接ｐ型ＳｉＣ領域を形成する場合のみに限定されないことは勿論である。例えば、ＳｉＣ基板１の表面の一部に、ｐ型ＳｉＣ領域よりも平面上の面積の大きい他の半導体領域をウェル形状に配置し、そのウェル形状の半導体領域の内部の位置において、ｐ型ＳｉＣ領域を形成しても良い。或いは、ＳｉＣ基板の表面の全面に他の半導体領域をエピタキシャル成長し、そのエピタキシャル成長した他の半導体領域の表面の一部において、ｐ型ＳｉＣ領域を形成するような場合も許容される。このように、請求項１０記載に係る発明においては、ｐ型ＳｉＣ領域を、他の半導体領域を介して、間接的に形成する場合をも許容することに留意すべきである。

【００３８】請求項１１記載に係る発明は、請求項１０記載に係るオーミック電極構造体の製造方法においてフィールド絶縁膜で被覆する工程は、熱酸化により、ＳｉＣ基板の表面に熱酸化膜を成長する工程と、この熱酸化膜の上部に、熱酸化以外の方法で、絶縁膜を堆積する工程とからなることを要旨とする。

【００３９】請求項１２記載に係る発明は、請求項１０記載に係るオーミック電極構造体の製造方法において、フィールド絶縁膜で被覆する工程は、熱酸化以外の方法で、ＳｉＣ基板の表面に酸素透過性絶縁膜を堆積する工程と、この酸素透過性絶縁膜の堆積後に、熱酸化により、ＳｉＣ基板の表面と酸素透過性絶縁膜との界面に、熱酸化膜を成長する工程とからなることを要旨とする。即ち、酸素透過性絶縁膜を介して、雰囲気の酸素が、ＳｉＣ基板の表面に到達し、ＳｉＣ基板の表面と酸素透過性絶縁膜との界面にSiO_2膜を形成し、フィールド絶縁膜を実現することが出来る。

【００４０】請求項１３記載に係る発明は、（イ）ＳｉＣ基板の表面の少なくとも一部に高不純物密度を有するｐ型ＳｉＣ領域を形成する工程と、（ロ）ＳｉＣ基板の表面を洗浄する工程と、（ハ）熱酸化以外の方法で、ＳｉＣ基板の表面に酸素透過性絶縁膜を堆積する工程と、（ニ）ｐ型ＳｉＣ領域の一部を選択的に露出するように、酸素透過性絶縁膜に開口部を形成する工程と、（ホ）この開口部を形成する工程後に、熱酸化により、この開口部に露出したＳｉＣ基板の表面、及びＳｉＣ基板の表面と酸素透過性絶縁膜との界面に、熱酸化膜を成長する工程と、（ヘ）開口部に成長した熱酸化膜を除去する工程と、（ト）熱酸化膜が除去された開口部の内部に、Ａｌ－Ｔｉ系電極膜を配設する工程と、（チ）非酸化性雰囲気中において、ＳｉＣ基板を熱処理しＡｌ－Ｔｉ系電極膜とＳｉＣ基板との加熱反応層を生成する工程とを有するオーミック電極構造体の製造方法であることを要旨とする。

【００４１】請求項１４記載に係る発明は、請求項１３記載に係るオーミック電極構造体の製造方法において、加熱反応層を生成する工程は、酸素及び水の分圧が共に1×10^{-3}Ｐａ～1×10^{-10}Ｐａである雰囲気中で実施されることを要旨とする。

【００４２】請求項１５記載に係る発明は、請求項１０～１４のいずれか１項記載に係るオーミック電極構造体の製造方法において、Ａｌ－Ｔｉ系電極膜を配設する工程は、（ｉ）Ａｌ層の上にＴｉ層を堆積する工程、（ｉｉ）Ｔｉ層の上にＡｌ層を堆積する工程、（iii）Ａｌ－Ｔｉ合金膜を堆積する工程からなるグループの内の少なくとも一つの工程を含むことを要旨とする。

【００４３】請求項１６記載に係る発明は、請求項１０～１２のいずれか１項記載に係るオーミック電極構造体の製造方法において、開口部を形成する工程は（ａ）フォトリソグラフィ法により、フィールド絶縁膜の上部にエッチングマスクを形成する工程と、（ｂ）このエッチングマスクを用いて、ｐ型ＳｉＣ領域の少なくとも一部の上部にフィールド絶縁膜が残留するように、フィールド絶縁膜の一部をドライ・エッチングで除去する工程と、（ｃ）残留したフィールド絶縁膜をウェット・エッチングで除去し、ｐ型ＳｉＣ領域の少なくとも一部を露出する工程と、（ｄ）超純水によるリンスで、露出したｐ型ＳｉＣ領域を清浄化する工程とからなることを要旨とする。

【００４４】請求項１７記載に係る発明は、請求項１６記載に係るオーミック電極構造体の製造方法において、Ａｌ－Ｔｉ系電極膜を配設する工程は、エッチングマスクが、フィールド絶縁膜の上部に残留した状態で、Ａｌ－Ｔｉ系電極膜をエッチングマスクの上部及び開口部を含む全面に堆積する工程と、この全面に堆積する工程の後、エッチングマスクを除去することにより、Ａｌ－Ｔｉ系電極膜を開口部の内部にのみ選択的に残留させる工程とからなることを要旨とする。

【００４５】請求項１８記載に係る発明は、請求項１３又は１４記載に係るオーミック電極構造体の製造方法において開口部を形成する工程は、（ａ）フォトリソグラフィ法により、酸素透過性絶縁膜の上部にエッチングマスクを形成する工程と、（ｂ）このエッチングマスクを用いて、ｐ型ＳｉＣ領域の少なくとも一部の上部に酸素透過性絶縁膜が残留するように、酸素透過性絶縁膜の一部を除去する工程と、（ｃ）残留した酸素透過性絶縁膜をウェット・エッチングで除去し、ｐ型ＳｉＣ領域の少なくとも一部を露出する工程と、（ｄ）超純水によるリンスで、露出したｐ型ＳｉＣ領域を清浄化する工程とからなることを要旨とする。

【００４６】請求項１９記載に係る発明は、（イ）ＳｉＣ基板と、（ロ）このＳｉＣ基板の表面に選択的に形成

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された主電極領域として機能するｐ型ＳｉＣ領域と、（ハ）このｐ型ＳｉＣ領域の表面の一部から内部に進入し、且つこのｐ型ＳｉＣ領域の表面から上方に突出して形成された加熱反応層と、（ニ）この加熱反応層が貫通する第１の開口部を有し、ＳｉＣ基板とｐ型ＳｉＣ領域の表面に接して配置された熱酸化膜と、（ホ）この熱酸化膜とは組成若しくは密度の異なる絶縁膜であって、第１の開口部に連続した第２の開口部を有し、且つ熱酸化膜の表面に配置された上部絶縁膜と、（ヘ）この上部絶縁膜の第２の開口部において、加熱反応層の上部に配置されたＡｌ及びＴｉの少なくとも一方を含む金属からなる電極膜と、（ト）この電極膜に接続される主電極配線とからなる半導体装置であることを要旨とする。

【００４７】ここで、「ＳｉＣ基板の表面に選択的に形成された主電極領域として機能するｐ型ＳｉＣ領域」は、ＳｉＣ基板の表面に、直接ｐ型ＳｉＣ領域が形成される場合のみに限定されないことは勿論である。例えば、ＳｉＣ基板１の表面の一部に、主電極領域（ｐ型ＳｉＣ領域）よりも面積の大きい他の半導体領域をウェル形状に配置し、そのウェル形状の半導体領域の内部の位置において、主電極領域（ｐ型ＳｉＣ領域）が形成されていても良い。例えば、バイポーラトランジスタのベース領域や、パワーＭＯＳＦＥＴ等のボディ領域中に形成された主電極領域（ｐ型ＳｉＣ領域）でも構わない。或いは、ＳｉＣ基板の表面の全面に他の半導体領域をエピタキシャル成長し、そのエピタキシャル成長した他の半導体領域の表面の一部において、主電極領域（ｐ型ＳｉＣ領域）を形成するような場合も許容される。このように、請求項１９記載に係る発明においては、主電極領域（ｐ型ＳｉＣ領域）が他の半導体領域を介して、間接的に、ＳｉＣ基板の表面に形成される場合を許容することに留意すべきである。

【００４８】請求項２０記載に係る発明は、請求項１９に係る半導体装置において、電極膜が、下部のチタン・シリコン（Ｔｉ－Ｓｉ）合金膜と上部のチタン（Ｔｉ）膜とからなる積層膜、下部のアルミニウム・シリコン（Ａｌ－Ｓｉ）合金膜と上部のアルミニウム（Ａｌ）膜とからなる積層膜、及び下部のアルミニウム・チタン・シリコン（Ａｌ－Ｔｉ－Ｓｉ）合金膜と上部のアルミニウム・チタン（Ａｌ－Ｔｉ）合金膜とからなる積層膜からなるグループの内の少なくとも一つの積層膜を含む金属膜であることを要旨とする。

【００４９】請求項２１記載に係る発明は、請求項１９又は２０記載に係る半導体装置において、加熱反応層が、金属の炭化物と金属シリコン（Ｓｉ）とを含む固溶体であることを要旨とする。

【００５０】

【発明の効果】請求項１記載に係る発明によれば、ＳｉＣ基板の表面を熱酸化して形成された熱酸化膜と熱酸化膜とは組成若しくは密度の異なる絶縁膜との積層構造で、比較的厚いフィールド絶縁膜が形成出来る。このため、高耐圧が要求される各種パワーデバイスにおいて、従来知られていたコンタクト抵抗ρcよりも１桁程度低い$10^{-6}\Omega cm^2$台、或いはこれ以下のコンタクト抵抗ρcが実現され、表面配線がｐ型ＳｉＣ領域に接続される種々の半導体電子デバイスの高周波化、高性能化が可能となる。特に、実際のデバイス構造に採用可能な微細な開口部（コンタクト・ウインドウ）の内部において、低いコンタクト抵抗ρcを得ることが出来る。

【００５１】請求項２記載に規定する材料を金属膜として用いることにより、ショットキー障壁が低く、且つその障壁の厚さが薄い金属／半導体接合出来る。また、加熱反応層が均一に生成される。このため、請求項２記載に係る発明によれば、ｐ型ＳｉＣ領域に対するコンタクト抵抗ρcが極めて低いオーミック電極構造体が得られる。

【００５２】請求項３記載に係る発明によれば、金属の炭化物と金属シリコンとを含む固溶体からなる加熱反応層を選択しているので、金属／半導体接合におけるショットキー障壁が極めて低く、且つ、界面のモホロジーが良好で、加熱反応層が均一に形成出来る。このため、ｐ型ＳｉＣ領域に対するコンタクト抵抗ρcが極めて低いオーミック電極構造体が得られる。

【００５３】ＳｉＣの熱酸化膜は、Ｓｉ熱酸化膜よりは劣るが、Ｓｉ熱酸化膜に近いシリコン酸化膜（SiO_2膜）である。従って、ＳｉＣの熱酸化膜の絶縁破壊電界強度は、厚さ１０ｎｍで１４ＭＶ／ｃｍ程度である。熱酸化以外の方法で形成したSiO_2膜の絶縁破壊電界強度は、この値よりも小さい。即ち、請求項４記載に係る発明によれば、ＳｉＣの熱酸化膜以外の種々の絶縁膜を、ＳｉＣの熱酸化膜の上部に形成して、半導体装置の仕様として要求される耐圧を確保しつつ、ＳｉＣの表面モホロジーを良好に維持出来る。

【００５４】上記のように、ＳｉＣの熱酸化膜は、Ｓｉ熱酸化膜に近いSiO_2膜であるので、ＢＨＦ溶液に対するエッチング速度は１００ｎｍ／分程度である。これに比し、ＣＶＤで堆積したSiO_2膜に対するエッチング速度は１１．５倍から３倍位高い。即ち、請求項５記載に係る発明によれば、ＳｉＣの熱酸化膜以外の種々のSiO_2膜を、ＳｉＣの熱酸化膜の上部に形成して、半導体装置の仕様として要求される耐圧や表面の安定性を確保しつつ、ＳｉＣの表面モホロジーを良好に維持出来る。また、ＢＨＦ溶液に対するエッチング速度の相違を利用して、種々の半導体プロセスを採用出来る。

【００５５】請求項６記載に係る発明によれば、ｐ型ＳｉＣ領域の表面キャリア密度が、1×10^{18}／cm^3～5×10^{21}／cm^3の高不純物密度であるので、ｐ型ＳｉＣ領域と加熱反応層との間に生じるショットキー障壁の厚さが薄くなり、トンネル効果によって伝導正孔が容易に流れるようになる。このため、低いコンタクト抵抗

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ρｃが得られる。

【００５６】請求項７の発明によれば、熱酸化膜の厚さを２～５０ｎｍの値に最適化しているので、ｐ型ＳｉＣ領域の表面に生成されやすい炭化水素化合物及び自然酸化膜を可能な限り除く効果を維持しつつ、過剰な熱酸化による基板粗面化を防止することが出来る。このため、ｐ型ＳｉＣ領域と加熱反応層の界面が平坦である。また、加熱反応層が均一且つ均質であるので、ショットキー障壁の高さが低減され、コンタクト抵抗ρｃが低くなる。

【００５７】請求項８記載に係る発明によれば、熱酸化膜の厚さと上部絶縁膜の厚さとを合計した値を、１００ｎｍ～３μｍとしたため、熱酸化膜の下部のＳｉＣ基板と上部絶縁膜の上部の配線とで形成される寄生ＭＯＳトランジスタによるリーク電流が抑制され、高い耐圧を有した電力用半導体デバイスが提供出来る。

【００５８】請求項９記載に係る発明によれば、電極膜の最上部の位置が、第２の開口部の内部に存在し、第２の開口部周辺の上部絶縁膜を重畳することが無い。このため、加熱反応層を形成する時、Ａｌが溶融しても、Ａｌは第２の開口部の窪地に閉じこめられるので、融解Ａｌが周辺の上部絶縁膜の表面に流れ出し、配線ショートを起こす心配が無い。この結果、製造歩留まりが向上する。

【００５９】請求項１０記載に係る発明によれば、フィールド絶縁膜を形成する直前から、開口部の内部にＡｌ－Ｔｉ系電極膜を配設するまでの工程は、開口部のＳｉＣ露出表面にフォトレジストを一度も塗布することなく進行出来る。従って、加熱反応層を形成する前のＡｌ－Ｔｉ系電極膜とＳｉＣとの界面へのフォトレジストに起因するハイドロ・カーボンの付着が完全に回避出来、清浄な界面が容易に得られる。このため、加熱反応層とＳｉＣとの界面のショットキー障壁が極めて低く、且つ、薄くなる。また、界面のモホロジーが良好で、加熱反応層が均一に生成される。更に、酸素及び水の分圧が共に1×10^{-3} Ｐａ～1×10^{-10} Ｐａの非酸化性雰囲気中で熱処理し、加熱反応層を生成しているので、熱処理中にＡｌ－Ｔｉ系電極膜の表面に生成される酸化アルミニウム（Al_2O_3）や酸化チタン（TiO_2）等の金属酸化膜が、顕著に抑制され、表面の金属酸化膜によるコンタクト抵抗ρｃの増大が大きく低減出来る。この結果、従来のコンタクト抵抗ρｃよりも１桁程度低い$10^{-6}\Omega cm^2$台、若しくはこれ以下のコンタクト抵抗ρｃが得られる。しかも、このオーミック電極構造体は、フィールド絶縁膜中の開口部に設けられるので、現実の半導体電子デバイスに適した構造である。

【００６０】請求項１１記載に係る発明によれば、ＳｉＣ基板の表面にフィールド絶縁膜を形成する工程は、熱酸化膜を成長する工程と、この熱酸化膜の上部に熱酸化以外の方法で絶縁膜を堆積する工程とから構成しているので、過度の熱酸化によるＳｉＣ基板の表面モホロジーの劣化を抑制することが出来る。また、熱酸化以外の方法は、ＣＶＤ法やスパッタリング法等の周知の物理的或いは化学的手段が採用可能であるが、これらの、熱酸化以外の方法に固有な自然酸化膜やハイドロ・カーボンの生成を熱酸化膜により効果的に除去、若しくは抑制出来る。このため、加熱反応層とｐ型ＳｉＣ領域との界面のモホロジーが良好となり、均一且つ均質な加熱反応層を生成出来る。従って、上述した$10^{-6}\Omega cm^2$台、若しくはこれ以下のコンタクト抵抗ρｃを簡単に得ることが出来る。

【００６１】請求項１２記載に係る発明によれば、熱酸化以外の方法でＳｉＣ基板の表面に酸素透過性絶縁膜を堆積する工程を先に行い、この酸素透過性絶縁膜の堆積後に、熱酸化によりＳｉＣ基板の表面と酸素透過性絶縁膜との界面に熱酸化膜を成長して、フィールド絶縁膜を形成している。この場合も、請求項１１記載に係る発明と同様に、過度の熱酸化によるＳｉＣ基板の表面モホロジーの劣化を抑制することが出来る。また、ＣＶＤ法やスパッタリング法等の周知の物理的或いは化学的手段に固有な自然酸化膜やハイドロ・カーボンの生成を、熱酸化膜の生成により効果的に除去、若しくは抑制出来る。このため、加熱反応層とｐ型ＳｉＣ領域との界面のモホロジーが良好となり、均一且つ均質な加熱反応層を生成出来る。従って、$10^{-6}\Omega cm^2$台、若しくはこれ以下の低いコンタクト抵抗ρｃを簡単に得ることが出来る。

【００６２】請求項１３記載に係る発明においては、先に、熱酸化以外の方法でＳｉＣ基板の表面に酸素透過性絶縁膜からなる「暫定フィールド絶縁膜」を形成し、この暫定フィールド絶縁膜に開口部（いわゆるコンタクト・ウインドウ）を形成し、この開口部に露出したＳｉＣ基板の表面に熱酸化膜を成長し、その後、この熱酸化膜を除去しているので、ｐ型ＳｉＣ領域の表面を清浄化出来る。更に、請求項１１及び１２記載に係る発明と同様に、暫定フィールド絶縁膜を形成する直前から、開口部の内部にＡｌ－Ｔｉ系電極膜を配設するまでの工程は、開口部のＳｉＣ露出表面にフォトレジストを一度も塗布することなく進行出来る。従って、加熱反応層を形成する前のＡｌ－Ｔｉ系電極膜とＳｉＣとの界面へのフォトレジストに起因するハイドロ・カーボンの付着が完全に回避出来、清浄な界面が容易に得られる。このため、加熱反応層とＳｉＣとの界面のショットキー障壁が極めて低く、且つ、薄くなる。更に、後からの熱酸化により、ＳｉＣ基板の表面と酸素透過性絶縁膜との界面に、薄い熱酸化膜が形成されるので、請求項１１及び１２記載に係る発明と同様に、高耐圧化が可能になると同時に過度の熱酸化によるＳｉＣ基板の表面モホロジーの劣化を抑制することが出来る。また、熱酸化以外の物理的或いは化学的手段に固有な自然酸化膜やハイドロ・カーボンの生成を、熱酸化膜の生成により効果的に除去出来る。こ

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のため、加熱反応層とｐ型ＳｉＣ領域との界面のモホロジーが良好となり、均一且つ均質な加熱反応層を生成出来る。従って、$10^{-6}\Omega cm^2$台、若しくはこれ以下の低いコンタクト抵抗ρｃを簡単に得ることが出来る。

【００６３】請求項１４記載に係る発明によれば、酸素及び水の分圧が共に1×10^{-3}Ｐａ～1×10^{-10}Ｐａの非酸化性雰囲気中で熱処理し、加熱反応層を生成しているので、熱処理中にＡｌ－Ｔｉ系電極膜の表面に生成されるAl_2O_3やTiO_2等の金属酸化膜が、顕著に抑制され、表面の金属酸化膜によるコンタクト抵抗ρｃの増大が大きく低減出来る。

【００６４】請求項１５記載に規定する（ｉ）Ａｌ層の上にＴｉ層を堆積したＡｌ／Ｔｉ積層膜、（ii）Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜、（iii）Ａｌ－Ｔｉ合金膜は、いずれもｐ型ＳｉＣ領域との反応により、ｐ型ＳｉＣ領域との界面のモホロジーが良好でかつショットキー障壁が極めて低い加熱反応層が形成出来る。従って、請求項１５記載に係る発明によれば、従来のコンタクト抵抗ρｃよりも１桁程度低い$10^{-6}\Omega cm^2$台、若しくはこれ以下のコンタクト抵抗ρｃが得られる。

【００６５】請求項１６記載に係る発明によれば、開口部がｐ型ＳｉＣ領域に到達する最終ステップが、ウェット・エッチングと超純水によるリンスで完結されるので、ドライ・エッチングの反応生成物であるハイドロ・カーボンのｐ型ＳｉＣ基板の表面への再付着や、過剰なプラズマエネルギによるエッチング損傷が防止出来る。このため、ｐ型ＳｉＣ基板の表面の汚染や基板表面の粗面化が有効に防止出来る。加えて、ドライ・エッチングが使用出来るため、微細なオーミック・コンタクトが形成出来るので、半導体集積回路の高集積密度化や、電力用半導体装置のオン抵抗の低減等の高性能化が可能になる。

【００６６】請求項１７記載に係る発明によれば、開口部（コンタクト・ウインドウ）を開口に用いたエッチングマスクを、Ａｌ－Ｔｉ系電極膜をパターニングするためのリフトオフ工程用のマスクとして兼用出来る。即ち、コンタクト・ウインドウ開口工程とＡｌ－Ｔｉ系電極膜のパターニング工程用のフォトリソグラフィ工程を一度で行え、半導体装置の製造プロセスが簡略化される。このため、半導体装置の製造歩留まりの向上、生産性の向上、更には製造コストの低減化が容易になる。

【００６７】請求項１８記載に係る発明によれば、酸素透過性絶縁膜にｐ型ＳｉＣ領域に到達する開口部を設ける最終ステップが、ウェット・エッチングと超純水によるリンスで完結されるので、ドライ・エッチングの反応生成物であるハイドロ・カーボンのｐ型ＳｉＣ基板の表面への再付着や、過剰なプラズマエネルギによるエッチング損傷が防止出来る。このため、請求項１６記載に係る発明と同様に、ｐ型ＳｉＣ基板の表面の汚染や基板表面の粗面化が有効に防止出来る。加えて、ドライ・エッチングが使用出来るため、微細なオーミック・コンタクトが形成出来、半導体集積回路の高集積密度化や、電力用半導体装置のオン抵抗の低減等の高性能化が可能になる。

【００６８】請求項１９記載に係る発明によれば、ＳｉＣ基板の表面を熱酸化して形成された熱酸化膜と熱酸化膜とは組成若しくは密度の異なる絶縁膜との積層構造で、安定性に優れた比較的厚いフィールド絶縁膜が形成出来る。このため、定格動作電圧の高い各種パワーデバイスにおいて、従来知られていたコンタクト抵抗ρｃよりも１桁程度低いコンタクト抵抗ρｃが実現される。このため、半導体電子デバイスの高周波化、高性能化が可能となる。特に、実際のデバイス構造に採用可能な微細な開口部（コンタクト・ウインドウ）の内部において、主電極領域に対する低いコンタクト抵抗ρｃを得ることが出来る。従って、微細なコンタクト・ウインドウを多数・高密度に配置することにより、低オン電圧・高速動作可能な半導体パワーデバイスが実現出来る。

【００６９】請求項２０記載に規定する材料を金属膜として用いることにより、ショットキー障壁が低く、且つその障壁の厚さが薄い金属／半導体接合出来る。また、加熱反応層が均一に生成される。このため、請求項２０記載に係る発明によれば、ｐ型ＳｉＣ領域からなる主電極領域に対するコンタクト抵抗ρｃが極めて低くなり、種々の半導体電子デバイスの高周波化、高性能化が可能となる。

【００７０】請求項２１記載に係る発明によれば、金属の炭化物と金属シリコンとを含む固溶体からなる加熱反応層を選択しているので、金属／半導体接合におけるショットキー障壁が極めて低くなる。しかも、界面のモホロジーが良好で、加熱反応層が均一に形成出来る。このため、主電極領域に対するコンタクト抵抗ρｃが極めて低くなり、種々の半導体電子デバイスの高周波化、高性能化が可能となる。

【００７１】

【発明の実施の形態】次に、図面を参照して、本発明の第１乃至第３の実施の形態を説明する。以下の図面の記載において、同一又は類似の部分には同一又は類似の符号を付している。但し、図面は模式的なものであり、厚さと平面寸法との関係、各層の厚さの比率等は現実のものとは異なることに留意すべきである。従って、具体的な厚さや寸法は以下の説明を参酌して判断すべきものである。また図面相互間においても互いの寸法の関係や比率が異なる部分が含まれていることは勿論である。

【００７２】（第１の実施の形態）図１に示すように、本発明の第１の実施の形態に係るオーミック電極構造体は、ＳｉＣ基板１、ＳｉＣ基板１の表面に選択的に形成されたｐ型ＳｉＣ領域２、このｐ型ＳｉＣ領域２の表面の一部に形成された加熱反応層８、ＳｉＣ基板１とｐ型

ＳｉＣ領域２との界面を覆う熱酸化膜３、熱酸化膜３の表面に配置された上部絶縁膜４、加熱反応層８の上部に配置された電極膜７とを少なくとも有する。ｐ型ＳｉＣ領域２は、半導体装置、特に半導体電子デバイスの主電極領域として機能する。

【００７３】一般に半導体電子デバイスは、第１主電極領域、第２主電極領域及び制御電極を有する。「第１主電極領域」とは、ＩＧＢＴにおいてエミッタ領域又はコレクタ領域のいずれか一方、パワーＭＯＳＦＥＴやパワーＭＯＳＳＩＴ等の電力用絶縁ゲート型トランジスタ（パワーＩＧＴ）においては、ソース領域又はドレイン領域のいずれか一方を意味する。「第２主電極領域」とは、ＩＧＢＴにおいては上記第１主電極領域とはならないエミッタ領域又はコレクタ領域のいずれか一方、パワーＩＧＴにおいては上記第１主電極領域とはならないソース領域又はドレイン領域のいずれか一方を意味する。即ち、第１主電極領域が、エミッタ領域であれば、第２主電極領域はコレクタ領域であり、第１主電極領域がソース領域であれば、第２主電極領域はドレイン領域である。また、「制御電極」とはＩＧＢＴ及びパワーＩＧＴのゲート電極を意味することは勿論である。本発明においては、第１主電極領域及び第２主電極領域のいずれか一方を、単に「主電極領域」と呼ぶ。また、ダイオード等の制御電極を有しないＳｉＣ半導体装置でも、同様に、第１主電極領域及び第２主電極領域が定義される。本発明においては、この場合も、第１主電極領域及び第２主電極領域のいずれか一方を、単に「主電極領域」と呼ぶ。更に、パワーＩＣ等の半導体集積回路においては、３つ以上の主電極領域が定義可能であるが、これらの複数の少なくとも一つは、本発明の「主電極領域」である。

【００７４】熱酸化膜３と、上部絶縁膜４との積層構造により、フィールド絶縁膜５を構成している。更に、電極膜７に電気的に接続するように、フィールド絶縁膜５の上には、配線導体素片９が形成されている。配線導体素片９は図１に示すオーミック・コンタクトを他の部位と結線する配線部材であり、半導体装置の主電極配線として機能する。パワーデバイスにおいては、複数のユニットセルを多数ＳｉＣ基板１の上に、蜂の巣状や、マトリクス状等にして配置し電流容量を確保している。また、オン電圧を低くするための設計仕様により、各主電極領域を細分化し、ＳｉＣ基板１の上に高密度に配列する場合もある。従って、このような場合は、複数に分割されたユニットセルの各主電極領域を統合する配線として配線導体素片９が機能する。この配線導体素片９には、周知のアルミニウム（Ａｌ）、アルミニウム・シリコン（Ａｌ－Ｓｉ）共晶、アルミニウム・銅・シリコン（Ａｌ－Ｃｕ－Ｓｉ）共晶、銅（Ｃｕ）、チタン・タングステン（Ｔｉ－Ｗ）合金などが用いられる。

【００７５】ＳｉＣ基板１の導電型や不純物密度は、本発明のオーミック電極構造体を利用する半導体装置によって異なる。更に、ＳｉＣ基板１の表面の一部に、ｐ型ＳｉＣ領域２よりも平面上の面積の大きい他の半導体領域をウェル形状に配置し、そのウェル形状の他の半導体領域の平面上の内部の位置において、エピタキシャル成長した高不純物密度のｐ型ＳｉＣ領域２を凸部として形成し、このｐ型ＳｉＣ領域２を主電極領域として用いても良い。或いは、ＳｉＣ基板１の表面の全面に他の半導体領域をエピタキシャル成長し、そのエピタキシャル成長した他の半導体領域の表面の一部において、更に連続エピタキシャル成長した高不純物密度のｐ型ＳｉＣ領域２をメサエッチング等により凸部として形成し、このｐ型ＳｉＣ領域２を主電極領域として用いても良い。

【００７６】例えば、ｐｎｐ型バイポーラトランジスタであれば、コレクタ領域となる低不純物密度のｐ型（若しくはπ型）ＳｉＣ基板１の表面に、ｎ型ＳｉＣ領域からなるベース領域をウェル形状に形成し、このベース領域の平面上の内部の位置において、主電極領域（エミッタ領域）としての高不純物密度のｐ型ＳｉＣ領域２を凸部として形成しても良い。この場合、コレクタ領域となる低不純物密度のｐ型ＳｉＣ基板１の代わりに真性半導体（ｉ型）のＳｉＣ基板１を用い、ｉ型ＳｉＣ基板１の裏面（若しくは表面の一部）に、高不純物密度のｐ型ＳｉＣ領域からなるコレクタ領域を形成しても良い。

【００７７】ＧＴＯサイリスタ等のサイリスタであれば、ｐベース領域となるｐ型ＳｉＣ基板１の表面の一部又は全面に、ｎ型ＳｉＣ領域からなるｎベース領域を形成し、このｎベース領域の内部に、アノード領域（主電極領域）としての高不純物密度のｐ型ＳｉＣ領域２をエピタキシャル成長により、凸部形状に形成することが可能である。この場合、ｐベース領域となるｐ型ＳｉＣ基板１の裏面には、カソード領域としてのｎ型ＳｉＣ領域が形成される。

【００７８】一方、ｎチャネルの接合型ＦＥＴや接合型ＳＩＴでは、チャネル領域として機能するｎ型ＳｉＣ基板（或いはν型ＳｉＣ基板若しくはｉ型ＳｉＣ基板）１の表面に、ソース領域（主電極領域）としての高不純物密度のｐ型ＳｉＣ領域２を凸部形状に形成可能である。また、ｎチャネルのＳＩサイリスタでは、チャネル領域として機能するｎ型ＳｉＣ基板（或いはν型ＳｉＣ基板若しくはｉ型ＳｉＣ基板）１の表面に、アノード領域としての高不純物密度のｐ型ＳｉＣ領域２を凸部形状に形成可能である。

【００７９】ｐチャネルのパワーＩＧＴでは、ｎ型チャネル領域として機能するｎ型ＳｉＣ基板（或いはπ型ＳｉＣ基板）１の表面に、ドレイン領域（主電極領域）としての高不純物密度のｐ型ＳｉＣ領域２を凸部形状に形成可能である。この場合、ｎ型ＳｉＣ基板（或いはπ型ＳｉＣ基板）１の表面の他の場所に、ドレイン領域２に対向して、ソース領域（他の主電極領域）としての高不

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純物密度のｐ型ＳｉＣ領域が凸部形状に形成される。そして、ソース領域とドレイン領域２の間のｎ型ＳｉＣ基板（或いはπ型ＳｉＣ基板）１の表面にゲート酸化膜が形成され、このゲート酸化膜の上に、ゲート電極が形成される。ゲート電極としては、タングステン（Ｗ）、チタン（Ｔｉ）、モリブデン（Ｍｏ）等の高融点金属、これらのシリサイド（WSi_2，$TiSi_2$，$MoSi_2$）等が使用可能である。或いは、２重拡散構造のｐチャネルのパワーＩＧＴでは、ドリフト領域として機能するｐ型ＳｉＣ基板（或いはπ型ＳｉＣ基板若しくはｉ型ＳｉＣ基板）１の表面に、ドレイン領域（主電極領域）としての高不純物密度のｐ型ＳｉＣ領域２を凸部形状に形成可能である。この場合、ソース領域としての他のｐ型ＳｉＣ領域が、ｐ型ＳｉＣ基板１の表面に形成されたｎボディ領域に形成される。同様に、ｎ型ＳｉＣ基板（或いはπ型ＳｉＣ基板）１の表面にドレイン領域としてのｐ型ＳｉＣ領域２と、ソース領域してのｐ型ＳｉＣ領域を凸部形状に形成し、ソース領域とドレイン領域２の間のｎ型ＳｉＣ基板（或いはπ型ＳｉＣ基板）１の表面に、ショットキー電極を構成すれば、ＭＥＳＦＥＴが実現出来る。

【００８０】ｎチャネルのＩＧＢＴでは、ドリフト領域として機能するｎ型ＳｉＣ基板（或いはν型ＳｉＣ基板）１の表面に、コレクタ領域としての高不純物密度のｐ型ＳｉＣ領域２を凸部形状に形成可能である。この場合、エミッタ領域としての他のｎ型ＳｉＣ領域が、ｎ型（或いはν型）ＳｉＣ基板１の表面に形成されたｐボディ領域に形成される。本発明の第１の実施の形態に係るオーミック電極構造体は、これら種々の半導体電子デバイスの主電極領域としての高不純物密度のｐ型ＳｉＣ領域２に適用可能である。加熱反応層８は、ｐ型ＳｉＣ領域２の表面の一部から内部に進入すると同時に、ｐ型ＳｉＣ領域２の表面から上方に突出して形成されている。熱酸化膜３は、加熱反応層８が貫通する第１の開口部を有し、且つＳｉＣ基板１とｐ型ＳｉＣ領域２との界面を覆うように、ＳｉＣ基板１とｐ型ＳｉＣ領域２の表面に接して配置されている。上部絶縁膜４は、熱酸化膜３とは組成若しくは密度の異なる絶縁膜であって、第１の開口部に連続した第２の開口部を有している。図１に示すように、電極膜７の最上部の位置は、第２の開口部の内部に存在する。第１及び第２の開口部は共通の開口部６を構成している。

【００８１】本発明の第１の実施の形態に係るオーミック電極構造体において、「熱酸化膜３とは組成の異なる絶縁膜」とは、ＰＳＧ（りん珪酸ガラス）膜、ＢＳＧ（硼珪酸ガラス）、ＢＰＳＧ（硼りん珪酸ガラス）或いはSi_3N_4膜等の絶縁膜の意である。また、「熱酸化膜３とは密度の異なる絶縁膜」とは、熱酸化膜以外の方法で堆積したSiO_2膜等の絶縁膜の意である。例えば、ＣＶＤ法、スパッタリング法、真空蒸着法等の、化学的若しくは物理的堆積方法によるSiO_2膜が該当する。図１に示すＳｉＣの熱酸化膜３は、Ｓｉ熱酸化膜よりは劣るが、Ｓｉ熱酸化膜に近いSiO_2膜である。熱酸化膜とその他の方法で堆積したSiO_2膜とでは密度が違うので断面を高分解能ＳＥＭ観察すると境界が見える。

【００８２】そして、Ｓｉ熱酸化膜に近いＳｉＣの熱酸化膜３の絶縁破壊電界強度は、厚さ１０ｎｍで１４ＭＶ／ｃｍ程度である。一方、熱酸化以外の方法で形成したSiO_2膜の絶縁破壊電界強度は、この値よりも小さい。例えば、ＣＶＤで堆積したSiO_2膜の絶縁破壊電界強度は、同じ厚さ１０ｎｍで６ＭＶ／ｃｍ程度であるので、絶縁破壊電界強度を測定すれば、明瞭にＳｉＣの熱酸化膜３と上部絶縁膜４とは識別可能である。

【００８３】また、ＳｉＣの熱酸化膜３は、Ｓｉ熱酸化膜に近いSiO_2膜であるので、ＢＨＦ溶液に対するエッチング速度は１００ｎｍ／分程度である。これに比し、ＣＶＤで堆積したSiO_2膜に対するエッチング速度は１．５倍から３倍位高い。従って、ＢＨＦ溶液に対するエッチング速度を測定すれば、明瞭にＳｉＣの熱酸化膜３と上部絶縁膜４とは識別可能である。

【００８４】ミクロには、ＣＶＤで堆積したSiO_2膜中には、ＳｉＣの熱酸化膜３より水素やカーボン結合が多く、Ｓｉ－Ｏ－Ｓｉ結合距離がＳｉＣの熱酸化膜３より長いので、赤外線吸収スペクトルやラマン分光によっても、明瞭にＳｉＣの熱酸化膜３と上部絶縁膜４とは識別可能である。

【００８５】図１に示すようなＳｉＣの熱酸化膜以外の種々のSiO_2膜等の上部絶縁膜４を、ＳｉＣの熱酸化膜３の上部に形成した積層構造を採用すれば、半導体装置の仕様として要求される耐圧や表面の安定性を確保しつつ、ＳｉＣの表面モホロジーを良好に維持出来る。

【００８６】熱酸化膜３の厚さは２～５０ｎｍであることが望ましい。特に、５～２０ｎｍの範囲の熱酸化膜３の厚さが望ましい。熱酸化膜３の厚さが、５ｎｍより薄い場合は表面研磨やイオン注入法で生じたＳｉＣ基板１表面の損傷領域を除去する効果ならびに表面の異物を除去する効果が乏しくなる。一方、熱酸化膜３の厚さが、５０ｎｍより厚い場合は過度な熱酸化によりＳｉＣ基板１表面が次第に荒れ、表面モホロジーが低下するという問題がある。このため、コンタクト抵抗ρcの低減には上記範囲の熱酸化膜３の厚さが有益な効果をもたらす。

【００８７】熱酸化膜３の厚さと上部絶縁膜４の厚さとを合計したフィールド絶縁膜５の総厚は、１００ｎｍ～３μｍであることが望ましい。特に、３００ｎｍ以上であることが望ましい。また、高耐圧の電力用半導体装置であれば、８００ｎｍ以上にすれば良い。但し、フィールド絶縁膜５があまり厚くなると、クラック等が発生するので、３μｍ以上は好ましくない。

【００８８】図１に示す電極膜７は、上部絶縁膜４の第２の開口部において、加熱反応層８の上部に配置された

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Ａｌ及びＴｉの少なくとも一方を含む金属から構成されている。この「Ａｌ及びＴｉの少なくとも一方を含む金属からなる電極膜７」は、（ｉ）下部のＴｉ－Ｓｉ合金膜と上部のＴｉ膜とからなる積層膜、（ii）下部のＡｌ－Ｓｉ合金膜と上部のＡｌ膜とからなる積層膜、及び（iii）下部のＡｌ－Ｔｉ－Ｓｉ合金膜と上部のＡｌ－Ｔｉ合金膜とからなる積層膜のいずれかであることが好ましい。

【００８９】後述するように、本発明は、（ｉ）Ａｌ層の上にＴｉ層を堆積したＡｌ／Ｔｉ積層膜、（ii）Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜、（iii）Ａｌ－Ｔｉ合金膜をｐ型ＳｉＣ領域２との反応させ、加熱反応層８を形成することにより、ショットキー障壁を極めて低く、且つ障壁の厚さを薄くしている。このことに由来して、図１に示す電極膜７は、この加熱反応層８の生成後の、未反応の金属層及び加熱反応層８を拡散してきた金属Ｓｉとの化合部からなる積層構造である。即ち、（ｉ）Ａｌ層の上にＴｉ層を堆積したＡｌ／Ｔｉ積層膜においては、熱処理前の下層のＡｌ層が熱処理により加熱反応層８となる。このとき、熱処理前の上層のＴｉ層においては、加熱反応層を拡散してきた金属Ｓｉとの反応により下部にＴｉ－Ｓｉ合金膜が生成される。この下部のＴｉ－Ｓｉ合金膜と上部の未反応のＴｉ膜とからなる積層膜で、電極膜７を構成することになる。

【００９０】（ii）Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜においては、熱処理前のＴｉ層が熱処理により加熱反応層８となる。一方、熱処理前のＡｌ層においては、加熱反応層を拡散してきた金属Ｓｉとの反応により下部にＡｌ－Ｓｉ合金膜が生成され、上部に未反応のＡｌ膜が残留する。

【００９１】（iii）Ａｌ－Ｔｉ合金膜においては、熱処理前の下部のＡｌ－Ｔｉ合金膜が熱処理により加熱反応層８となり、熱処理前の最上部には未反応のＡｌ－Ｔｉ合金膜が残る。そして、加熱反応層８との境界部には、加熱反応層を拡散してきた金属Ｓｉとの反応によりＡｌ－Ｔｉ－Ｓｉ合金膜が生成される。

【００９２】図２は、Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜を、１０００℃で２分間熱処理した後において、オージェ電子分光（ＡＥＳ）法を用いて、オーミック電極構造体の深さ方向の組成を分析した結果を示す図である。ＡＥＳ測定時のスパッタリングによるエッチング速度は、SiO_2換算で１３ｎｍ／分である。図２に示すように、最も表面側には、配線導体素片９としてのＡｌが存在する。配線導体素片９の下には、酸素（Ｏ）を含むＡｌと、その下のＳｉを含むＡｌとからなる電極膜７が存在する。電極膜７の厚さは、スパッタリングによるエッチング速度を考慮すると３１２ｎｍである。電極膜７の下には、厚さ３６７ｎｍの加熱反応層８が存在する。加熱反応層８は、炭素（Ｃ）及びＳｉを含むＴｉ層である。加熱反応層８の下が、ＳｉＣ基板１である。

【００９３】C_{KLL}，Al_{KLL}，Si_{LVV}を用いたターゲット・ファクター・アナリシス（ＴＦＡ）により、各元素の化学状態を判断すると、Ｃについては、化学状態が２成分に分けられ、表面側の成分はＴｉの分布と重なる。図示を省略したピーク形状からも、これは、加熱反応層８におけるＴｉの炭化物（ＴｉＣ）であると推定される。一方、深い方の成分はＳｉＣ基板１のＳｉＣに起因した成分であると推定される。

【００９４】Ａｌについても化学状態は、２成分に分けられ、図示を省略したピーク形状からも金属成分と酸化物成分の存在が推定される。それぞれの成分のプロファイルで、酸化物のプロファイルは、Ｏのプロファイルと良く一致している。

【００９５】Ｓｉについては、２成分乃至３成分に分けられる。プロファイルの分割時は、２成分のフィッティングの方が良好なので、ここで２成分系で考察する。図示を省略したピーク形状からは、金属成分と炭化物成分の存在が推定される。金属成分のプロファイルについては、表面側は、Al_{KLL}のＡｌ金属成分のプロファイルと良く一致する。ＴｉＣ層に対応する内部領域では、Ａｌ金属成分のプロファイルとの間に乖離が認められる。そこで、図示を省略したスペクトルの形状から化学状態を判断すると、Ａｌ金属成分と対応するスペクトルとの差が認められない。従って、金属成分であると判断される。このことから、加熱反応層８のＴｉＣ層では、Ｓｉが金属状態で存在すると推定される。

【００９６】また、Ｔｉ層以降で認められる成分は、Ｃ（ＳｉＣ）のプロファイルと良く一致し、ピーク形状からもＳｉＣ基板１のＳｉＣであると推定される。

【００９７】このように、ＡＥＳ測定によれば、Ｔｉ／Ａｌ積層膜を、１０００℃で２分間熱処理した場合には、加熱反応層８は、金属の炭化物（ＴｉＣ）と金属シリコンとを含む固溶体であることが推定出来る。Ａｌ／Ｔｉ積層膜を、熱処理した場合には、加熱反応層８は、ＡｌＣと金属シリコンとを含む固溶体となっていると推定される。この金属の炭化物と金属シリコンとを含む固溶体からなる加熱反応層８が、金属／半導体接合におけるショットキー障壁を極めて低くし、且つ、界面のモホロジーを良好にし、結果として、加熱反応層８を均一に生成出来ると判断される。

【００９８】Ｔｉ／Ａｌ積層膜或いはＡｌ／Ｔｉ積層膜の一要素のＡｌ膜はＳｉ半導体電子デバイスの配線で多用されているＡｌ－Ｓｉ共晶膜に替えることも出来る。

【００９９】図１に示すように、ＳｉＣ基板１の表面に、高い表面キャリア（ホール）密度を有するｐ型ＳｉＣ領域２が形成されている。ｐ型ＳｉＣ領域２は、ｐ型エピタキシャル膜をメサ状に残した領域２である。ｐ型ＳｉＣ領域２の表面キャリア密度は1×10^{18}／ｃｍ^3～5×10^{21}／ｃｍ^{3}であることが望ましい。より、好

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ましくは1×10^{18}／cm^3以上の表面キャリア密度が望ましい。

【0100】なお、半導体装置の設計により、各主電極領域及び制御電極に配線導体素片（主電極配線）9を介して接続される複数のボンディングパッドを、フィールド絶縁膜5の上に形成しても良い。そしてこの配線導体素片（主電極配線）9及びボンディングパッドの上部には、酸化膜（SiO_2）、PSG膜、BPSG膜、窒化膜（Si_3N_4）、或いはポリイミド膜等からなるパッシベーション膜を形成しても良い。そして、パッシベーション膜の一部に複数の電極層を露出するように複数の開口部（窓部）を設け、ボンディングを可能にすることが出来る。

【0101】次に図3～図5に示す工程断面図（その1～その3）を参照しながら、本発明の第1の実施の形態に係るオーミック電極構造体の製造工程を説明する。

【0102】（イ）先ず図3（a）に示すように、8°オフの4H－SiC基板1のSi面表面に、1×10^{19}／cm^3以上の高不純物密度のp型不純物（Al）を添加した厚さ数100nmのp型エピタキシャル成長層（p型SiC領域）20をエピタキシャル成長する。続いて、このp型エピタキシャル成長層（p型SiC領域）20の上に、厚さ1．2μmのシリコン酸化膜（SiO_2膜）をCVD法で堆積し、周知のフォトリソグラフィ法と反応性イオンエッチング（RIE）法等のエッチング技術で、p型SiC領域2に対応するエッチングマスク21を形成する。

【0103】（ロ）次に、SiO_2膜からなるエッチングマスク21を使用し、SF_6とO_2をエッチャントガスとしたRIE法で、図3（b）に示すように、不要なエピタキシャル層を除く。更に、その後、SiO_2膜からなるエッチングマスク21をフッ酸（HF）で全面除去して、素子分離されたメサ構造のp型SiC領域22を形成する。なお、p型SiC領域22が、パワーIGTのドレイン領域として機能する場合は、SiC基板1の表面の他の場所に、同様な手法で（ドレイン領域2の形成と同時に）、ドレイン領域2に対向して、ソース領域としてのp型SiC領域が凸部形状に形成される。この場合、SiC基板1としては、n型SiC基板、或いはπ型SiC基板を選べば良い。

【0104】（ハ）そして、シリコン（Si）プロセスで周知のRCA洗浄法等の所定の洗浄法を用いて、SiC基板1を十分清浄化する。RCA洗浄法は、H_2O_2＋NH_4OH混合液（SC－1）とH_2O_2＋HC1混合液（SC－2）による浸漬処理を組み合わせ行う伝統的な半導体SiC基板1の洗浄法である。そして、図3（c）に示すように、十分清浄化されたSiC基板1の表面を、1000℃から1150℃において乾燥酸素雰囲気で熱酸化し、表面に厚さ5～40nm熱酸化膜3を成長する。なお、乾燥酸素雰囲気の代わりに、水蒸気を用いてもかまわない。乾燥酸素中、雰囲気1150℃で3時間熱酸化すれば、35～40nmの熱酸化膜3が得られる。水蒸気を用いたウェット雰囲気中、1150℃で2時間熱酸化すれば、30～35nmの熱酸化膜3が得られる。水蒸気を用いたウェット雰囲気の熱酸化の場合は、その後アルゴン（Ar）中で1150℃、30分程度アニールすることが好ましい。熱酸化膜3を20nm以下にするためには、酸化温度を下げる若しくは、酸化時間を短縮すれば良い。パワーIGTの製造工程として考えるならば、ソース領域とドレイン領域2の間のSiC基板1の表面に形成される熱酸化膜3をゲート酸化膜として使用することも可能である。

【0105】（ニ）次に、図4（d）に示すように、熱酸化膜3の上に、常圧CVD法でSiO_2膜からなる上部絶縁膜4を堆積し、2層構造からなるフィールド絶縁膜5を形成する。熱酸化膜3の厚さと上部絶縁膜4の厚さとを合計したフィールド絶縁膜5の総厚を、600nm～1．5μm程度にすることが望ましい。仮に、パワーIGTの製造工程として考えるならば、上部絶縁膜4の堆積前に、ゲート電極の形成をしておけば良い。即ち、熱酸化膜3の形成後、W、Ti、Mo等の高融点金属、或いは、これらのシリサイド（WSi_2，$TiSi_2$，$MoSi_2$）等のゲート電極材料を、熱酸化膜3の上に、スパッタリング法、真空蒸着法、CVD法等で堆積する。そして、フォトリソグラフィ法とRIE法とを用いて、ゲート電極材料をパターニングし、ソース領域とドレイン領域2の間のゲート酸化膜3の上にゲート電極を形成すれば良い。そして、ゲート電極形成後、RCA洗浄法等でSiC基板1を清浄化する。十分清浄化されたゲート電極及び熱酸化膜3の上に、常圧CVD法でSiO_2膜からなる上部絶縁膜4を堆積し、2層構造からなるフィールド絶縁膜5を形成する。

【0106】（ホ）次にフィールド酸絶縁膜5の表面に厚さ1～2μmのフォトレジスト22をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト22を選択的に露光し、現像することによって開口部6に対応する部分のフォトレジスト22を除去する。続いて、このフォトレジスト22のパターンをエッチングマスクとして用い、SiC基板1をBHF溶液に浸漬し、ウェット・エッチングすることで、図4（e）に示すように、フィールド絶縁膜5に開口部6を形成する。微細な開口部6を形成する時は、ガスプラズマを用いたドライ・エッチングが好ましい。例えば、CHF_3やC_2F_6などをエッチャントとしたRIE法や電子サイクロトロン共鳴イオンエッチング（ECRイオンエッチング）等の種々のドライ・エッチングを使用することが出来る。この場合、最初にドライ・エッチングを行い、フィールド絶縁膜5を数10nm残したところで、ウェット・エッチングに切り換えるようにする。開口部6をドライ・エッチングで、最後ま

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で貫通させると、
１）ＳｉＣ基板１の表面が過剰なプラズマエネルギによるプラズマ損傷で荒れる、
２）エッチング反応で生成した反応生成物であるハイドロ・カーボンがＳｉＣ基板１の表面に再付着し、表面を汚染する
という弊害が起こり、後述の加熱反応層の均一生成に大きな障害になる。更には、コンタクト抵抗ρｃを劇的に増加させる結果となるので好ましくない。
【０１０７】（ヘ）その後、エッチングマスクとしてのフォトレジスト２２を残存した状態で、ＢＨＦ溶液を超純水で完全に濯ぎ落とした（リンスした）後、乾燥する。そして、レジストマスク２２が被着した状態のＳｉＣ基板１を、真空蒸着装置のチャンバー中に速やかに据え付け、直ちに真空排気する。コンタクト・ウインドウ開口エッチングから真空排気までの大気中放置時間は、コンタクト抵抗ρｃの大小をする極めて重要な因子である。大気中放置時間が長いと、開口部のＳｉＣ基板１の表面に自然酸化膜が生成されたり、望まぬ異物が付着する。このため、後述の加熱反応層の均一生成に大きな障害となり、ひいてはコンタクト抵抗ρｃを劇的に増加させるので、５分以内の短時間で行う。そして、真空蒸着装置のチャンバーをターボ分子ポンプ、クライオポンプ等で、１．３×10^{-5}Ｐａ未満の圧力まで真空排気し、図４（ｆ）に示すように、ＳｉＣ基板１の表面にＡｌ－Ｔｉ系電極膜１７を蒸着する。図４（ｆ）に示すように、開口部の側壁にＡｌ－Ｔｉ系電極膜１７が付着しないようにするためには、オリフィス等を用いて、蒸着ビームの指向性を向上させて行えば良い。
【０１０８】（ト）Ａｌ－Ｔｉ系電極膜１７の真空蒸着後、ＳｉＣ基板１を真空蒸着装置のチャンバーから取り出す。続いて、リフトオフ法を用いて、図５（ｇ）に示すように、開口部のみにＡｌ－Ｔｉ系電極膜７が選択的に埋設された基板構造を得る。即ち、ＳｉＣ基板１をアセトンなどの有機溶剤或いは専用のフォトレジスト剥離液に浸漬させ、ＳｉＣ基板１表面に残されているフォトレジスト２２を完全に除去すると、フォトレジスト２２の上に被着したＡｌ－Ｔｉ系電極膜１７もフォトレジスト２２とともに除かれるので、図５（ｇ）に示すように、開口部のみにＡｌ－Ｔｉ系電極膜２７が選択的に残存する。
【０１０９】（チ）しかる後、ＳｉＣ基板１を７００℃～１０５０℃の非酸化性雰囲気で、短時間（数分程度）の熱処理を施すと、図５（ｇ）に示すように、Ａｌ－Ｔｉ系電極膜２７とＳｉＣ基板１が相互に反応して、両者の界面領域に加熱反応層８が生成され、加熱反応層とｐ型ＳｉＣとの間で優れたオーミック特性が実現される。数分程度の短時間の熱処理を行うためには、赤外線（ＩＲ）ランプ加熱を用いれば良い。ここで「非酸化性雰囲気」とは酸素（O_2）や水（H_2O）等の酸素を含む化合物の気体を含まない雰囲気のことである。具体的には、超高純度アルゴン（Ａｒ）や超高純度窒素（N_2）などの超高純度不活性ガス雰囲気、或いは、高真空等が、「非酸化性雰囲気」として好適である。これら熱処理雰囲気に酸素が僅かでも含まれると、熱処理で表面にＡｌやＴｉの酸化物（＝絶縁物）が生じたり、加熱反応層の形成が阻害されたりするので、酸素及び水の分圧の制御に関しては、厳重なる管理が必要である。具体的には、熱処理雰囲気に含まれる酸素及び水の分圧は少なくとも、１×10^{-3}Ｐａ～１×10^{-10}Ｐａ程度、望ましくは、１．×10^{-5}Ｐａ～１×10^{-10}Ｐａ程度であることが望ましい。超高純度不活性ガス雰囲気中で熱処理する場合は、ガス配管のベーキングやリークの点検の他に、脱酸素装置やガス純化装置の採用等の厳重なる管理が必要である。また、高真空中で熱処理する場合は、ＡｌやＴｉはゲッタリング作用があり、厳密には１×10^{-8}Ｐａ程度の真空中でも表面が酸化するので、クライオパネル等を併用して、酸素及び水の分圧を１×10^{-8}Ｐａ～１×10^{-10}Ｐａ程度に制御して、超高真空下で熱処理をすることが好ましい。Ａｌ－Ｔｉ系電極膜２７として、Ａｌ層の上にＴｉ層を堆積したＡｌ／Ｔｉ積層膜においては、熱処理前の下層のＡｌ層が熱処理により加熱反応層８となる。このとき、熱処理前のＴｉ層は、下部にＴｉ－Ｓｉ合金膜が生成され、このＴｉ－Ｓｉ合金膜と上部の未反応のＴｉ膜との積層膜からなる電極膜７が加熱反応層８の上に生成される。Ａｌ－Ｔｉ系電極膜２７として、Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜においては、熱処理前のＴｉ層が熱処理により加熱反応層８となり、熱処理前のＡｌ層は、下部にＡｌ－Ｓｉ合金膜が生成され上部に未反応のＡｌ膜が残留するので、Ａｌ－Ｓｉ／Ａｌ層からなる電極膜７が加熱反応層８の上に生成される。Ａｌ－Ｔｉ系電極膜２７としてＡｌ－Ｔｉ合金膜を用いた場合には、熱処理前の下部のＡｌ－Ｔｉ合金膜が熱処理により加熱反応層８となり、熱処理前の最上部には未反応のＡｌ－Ｔｉ合金膜が残る。また、加熱反応層８との境界部には、Ａｌ－Ｔｉ－Ｓｉ合金膜が生成されるので、Ａｌ－Ｔｉ－Ｓｉ／Ａｌ－Ｔｉ層からなる電極膜７が加熱反応層８の上に生成される。熱反応層８としては、金属の炭化物と金属シリコンとを含む固溶体が形成される。
【０１１０】（リ）加熱反応層８の形成後に、図５（ｉ）に示すように、ＳｉＣ基板１１全面にＡｌ等の導体膜１９を蒸着する。そして、フォトリソグラフィ法とＲＩＥ等のエッチング技術でパターニングして、図１に示すような配線導体素片９を形成すれば、本発明の第１の実施の形態に係るオーミック電極構造体が完成する。この配線導体素片９が、ドレイン電極配線（主電極配線）であれば、同様に、ドレイン領域２に対向して配置されたソース領域に対しても、ソース電極配線（主電極配線が接続され、パワーＩＧＴが完成する（ソース電極

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側のオーミック電極も、ドレイン電極側と全く同一工程で、同時に形成可能である。）。なお、パターニングの際のエッチャント（＝エッチング液或いはエッチングガス）がＡｌ－Ｔｉ系電極膜７を侵す時は、Ａｌ等の導体膜１９は必ずＡｌ－Ｔｉ系電極膜７を覆うように配設する構成とすれば良い。

【０１１１】本発明の第１の実施の形態に係るオーミック電極構造体の効果を厳密に評価するために、線型伝送線路モデル（リニアＴＬＭ）評価法を用いて、コンタクト抵抗ρcを測定した。リニアＴＬＭ評価法においては、先ず、長方形の素子分離領域（ここではｎ型領域）の長辺方向に、コンタクト間隔を変化させながら、方形のコンタクトを横一列に並べた構造のリニアＴＬＭコンタクト群を用意する。そして、隣接する２つのコンタクト間の電流－電圧特性から抵抗を求める。リニアＴＬＭ評価法では、この抵抗をコンタクト間隔の関数として整理し、これを直線近似して数式処理を行い、最終的に厳密なコンタクト抵抗ρcを求める。

【０１１２】評価した試料の構成は次の通りである。ｐ型エピタキシャル層の厚さと不純物密度はそれぞれ８００ｎｍ、$1.2\times10^{19}/cm^3$（Ａｌドープ）である。Ａｌ－Ｔｉ系電極膜７はＴｉ（５０ｎｍ厚）／Ａｌ（３００ｎｍ厚）積層膜で構成されている。フィールド絶縁膜５を構成する熱酸化膜３は、１１００℃ドライ酸化膜（１０ｎｍ厚）で、その上の上部絶縁膜４は、常圧ＣＶＤで成膜したSiO_2膜（４００ｎｍ厚）である。加熱反応層８を形成するための熱処理温度及び熱処理時間、熱処理雰囲気はそれぞれ１０００℃、５分、純Ａｒ雰囲気である。ＴＬＭパターンを構成するコンタクト群のコンタクト幅及び長さはそれぞれ２００μｍ，１００μｍ、コンタクト間隔Ｌ＝６，１０，１５，２０，２５，３０μｍである。

【０１１３】図６はコンタクト間隔をパラメータにして、隣接するコンタクト電極間の電流－電圧特性を示している。原点を通る直線が得られていることから、ＴＬＭパターンを構成するすべての電極でオーミック・コンタクトが得られているのが判る。図６の直線の傾きから求めたコンタクト電極間の抵抗と距離の関係をプロットすると図７のようになる。データはバラツキの少ない１直線近似され、ＴＬＭ法によりコンタクト抵抗$\rho c=9.5\times10^{-7}\Omega cm^2$が得られる。他の条件を同じにして、Ｔｉ／Ａｌ積層電極膜の替わりに、Ａｌ（１５０ｎｍ厚）／Ｔｉ（１５ｎｍ厚）積層電極膜を用いた場合には$\rho c=7.0\times10^{-6}\Omega cm^2$が得られる。また、Ａｌ－Ｔｉ合金を用いた場合は、$\rho c=9.0\times10^{-6}\Omega cm^2$が得られる。

【０１１４】本発明の第１の実施の形態に係るオーミック電極構造体の製造方法において、熱処理温度は、９００℃以上が好ましい。上記のＴｉ／Ａｌ積層電極膜からなるＴＬＭパターンを用いたコンタクト抵抗ρcの測定によれば、熱処理温度７００℃では、$\rho c=1.2\times10^{-2}\Omega cm^2$、熱処理温度８００℃では、$\rho c=1.3\times10^{-3}\Omega cm^2$、熱処理温度９００℃では、$\rho c=4.3\times10^{-6}\Omega cm^2$であり、熱処理温度１０００℃では、上述したように、$\rho c=9.5\times10^{-7}\Omega cm^2$が得られたからである。

【０１１５】また、上記のＴｉ／Ａｌ積層電極膜を用いたコンタクト抵抗ρcの測定において、Ａｌの膜厚を３００ｎｍと一定にして、Ｔｉを１０ｎｍ，２０ｎｍ、５０ｎｍ，１００ｎｍと振ってみたときのコンタクト抵抗ρcは１００ｎｍが最も低く、５０ｎｍで一桁上昇（悪化）し、２０ｎｍ，１０ｎｍと緩やかに高くなる。従って、Ｔｉの膜厚は、５０ｎｍ以上が好ましい。より好ましくは、１００ｎｍ～３００ｎｍの値を選ぶと良い。

【０１１６】このように本発明の第１の実施の形態に係るオーミック電極構造体は、$10^{-6}\Omega cm^2$台或いはこれ以下の実用的なコンタクト抵抗ρcを達成している。この結果、ｐ型ＳｉＣに対するオーミック・コンタクトにおけるコンタクト抵抗ρcが高い、或いは単純化された構成で現実のＳｉＣ電子デバイスの製造に適用出来ない、というＳｉＣ電子デバイスの従来技術における問題点を解決している。

【０１１７】（第２の実施の形態）図８に示す本発明の第２の実施の形態に係るオーミック電極構造体の特徴は、ＳｉＣ基板１に選択的なイオン注入法でｐ型ＳｉＣ領域３２を構成した点である。即ち、本発明の第２の実施の形態に係るオーミック電極構造体は、ＳｉＣ基板１、ＳｉＣ基板１の表面に選択的に形成されたｐ型ＳｉＣ領域３２、このｐ型ＳｉＣ領域３２の表面の一部に形成された加熱反応層８、ＳｉＣ基板１とｐ型ＳｉＣ領域３２との界面を覆う熱酸化膜３、熱酸化膜３の表面に配置された上部絶縁膜４、加熱反応層８の上部に配置された電極膜７とを少なくとも有する。ｐ型ＳｉＣ領域３２は、半導体装置、特に半導体電子デバイスの主電極領域として機能する。

【０１１８】熱酸化膜３と、上部絶縁膜４との積層構造により、フィールド絶縁膜５を構成している。更に、電極膜７に電気的に接続するように、フィールド絶縁膜５の上には、配線導体素片９が形成されている。配線導体素片９は図８に示すオーミック・コンタクトを他の部位と結線する配線部材であり、半導体装置の主電極配線として機能する。従って、設計にもよるが、配線導体素片９は所定のボンディングパッドにまで接続される主電極配線でも良い。この配線導体素片９には、周知のＡｌ、Ａｌ－Ｓｉ共晶、Ａｌ－Ｃｕ－Ｓｉ共晶、Ｃｕ、Ｔｉ－Ｗ合金などが用いられる。

【０１１９】加熱反応層８は、ｐ型ＳｉＣ領域３２の表面の一部から内部に進入すると同時に、ｐ型ＳｉＣ領域３２の表面から上方に突出して形成されている。熱酸化膜３は、加熱反応層８が貫通する第１の開口部を有し、

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且つＳｉＣ基板１とｐ型ＳｉＣ領域３２との界面を覆うように、ＳｉＣ基板１とｐ型ＳｉＣ領域３２の表面に接して配置されている。上部絶縁膜４は、熱酸化膜３とは組成若しくは密度の異なる絶縁膜であって、第１の開口部に連続した第２の開口部を有している。図８に示すように、電極膜７の最上部の位置は、第２の開口部の内部に存在する。第１及び第２の開口部は共通の開口部６を構成している。

【０１２０】本発明の第１の実施の形態で定義したように、第２の実施の形態に係るオーミック電極構造体において、「熱酸化膜３とは組成の異なる絶縁膜」とは、ＰＳＧ膜、ＢＳＧ、ＢＰＳＧ或いはSi_3N_4膜等の絶縁膜の意である。また、「熱酸化膜３とは密度の異なる絶縁膜」とは、熱酸化膜以外の方法、例えば、ＣＶＤ法、スパッタリング法、真空蒸着法等で堆積したSiO_2膜等の絶縁膜が該当する。図８に示すＳｉＣの熱酸化膜３は、Ｓｉ熱酸化膜よりは劣るが、Ｓｉ熱酸化膜に近いSiO_2膜である。熱酸化膜とその他の方法で堆積したSiO_2膜とでは密度が違うので断面を高分解能ＳＥＭ観察すると境界が見える。また、ＳｉＣの熱酸化膜３と上部絶縁膜４とは、絶縁破壊電界強度、ＢＨＦ溶液に対するエッチング速度、赤外線吸収スペクトルやラマン分光スペクトルを測定すれば、明瞭に識別可能である。

【０１２１】熱酸化膜３の厚さは２～５０ｎｍであることが望ましい。特に、５～２０ｎｍの範囲の熱酸化膜３の厚さが望ましい。第１の実施の形態で説明したように熱酸化膜３の厚さが、５ｎｍより薄い場合は表面研磨やイオン注入法で生じたＳｉＣ基板１表面の損傷領域を除去する効果ならびに表面の異物を除去する効果が乏しくなる。一方、熱酸化膜３の厚さが、５０ｎｍより厚い場合は過度な熱酸化によりＳｉＣ基板１表面が次第に荒れ、表面モホロジーが低下するからである。

【０１２２】熱酸化膜３の厚さと上部絶縁膜４の厚さとを合計したフィールド絶縁膜５の総厚は、１００ｎｍ～３μｍであることが望ましい。特に、３００ｎｍ以上であることが望ましい。また、高耐圧の電力用半導体装置であれば、８００ｎｍ以上にすれば良い。但し、フィールド絶縁膜５があまり厚くなると、クラック等が発生するので、３μｍ以上は好ましくない。

【０１２３】図８に示すようなＳｉＣの熱酸化膜以外の種々のSiO_2膜等の上部絶縁膜４を、ＳｉＣの熱酸化膜３の上部に形成した積層構造を採用すれば、半導体装置の仕様として要求される耐圧や表面の安定性を確保しつつ、ＳｉＣの表面モホロジーを良好に維持出来る。

【０１２４】図８に示す電極膜７は、上部絶縁膜４の第２の開口部において、加熱反応層８の上部に配置されたＡｌ及びＴｉの少なくとも一方を含む金属から構成されている。第１の実施の形態で説明したように、この「Ａｌ及びＴｉの少なくとも一方を含む金属からなる電極膜７」は、下部のＴｉ－Ｓｉ合金膜と上部のＴｉ膜とからなる積層膜、下部のＡｌ－Ｓｉ合金膜と上部のＡｌ膜とからなる積層膜、及び下部のＡｌ－Ｔｉ－Ｓｉ合金膜と上部のＡｌ－Ｔｉ合金膜とからなる積層膜のいずれかであることが好ましい。また、熱反応層８は、金属の炭化物と金属シリコンとを含む固溶体であることが好ましい。この金属の炭化物と金属シリコンとを含む固溶体からなる加熱反応層８が、金属／半導体接合におけるショットキー障壁を極めて低くし、且つ、界面のモホロジーを良好にし、結果として、加熱反応層８を均一に生成出来ると判断される。Ｔｉ／Ａｌ積層膜或いはＡｌ／Ｔｉ積層膜の一要素のＡｌ膜はＳｉ半導体電子デバイスの配線で多用されているＡｌ－Ｓｉ共晶膜等に替えることも出来る。

【０１２５】図８に示すように、ＳｉＣ基板１の表面に、高い表面キャリア（ホール）密度を有するｐ型ＳｉＣ領域３２が形成されている。イオン注入法は、第１の実施の形態に係るエピタキシャルｐ型ＳｉＣ領域２の場合よりも高不純物密度のｐ型ＳｉＣ領域３２が形成出来るのが利点である。ｐ型ＳｉＣ領域３２の表面キャリア密度（表面正孔密度）は少なくとも$1\times10^{17}/cm^3$以上、好ましくは$1\times10^{18}/cm^3$以上であることが望ましい。

【０１２６】ＳｉＣ基板１の導電型や不純物密度は、本発明の第２の実施の形態に係るオーミック電極構造体を利用する半導体装置の設計仕様によって異なる。更に、ＳｉＣ基板１の表面に、ｐ型ＳｉＣ領域３２よりも平面面積の大きく、拡散深さの深い他の半導体領域をウェル形状に配置し、その内部の表面にｐ型ＳｉＣ領域３２を形成しても良い。例えば、ｐｎｐ型バイポーラトランジスタであれば、コレクタ領域となるｐ型ＳｉＣ基板１の表面に、ｎ型ＳｉＣ領域からなるベース領域を形成し、このベース領域の内部に、エミッタ領域としてのｐ型ＳｉＣ領域３２を形成しても良い。この場合、コレクタ領域となる低不純物密度のｐ型ＳｉＣ基板１の代わりに真性半導体（ｉ型）のＳｉＣ基板１を用い、ｉ型ＳｉＣ基板１の裏面（若しくは表面の一部）に高不純物密度のｐ型ＳｉＣ領域からなるコレクタ領域を形成しても良い。

【０１２７】ＧＴＯサイリスタ等のサイリスタであれば、ｐベース領域となるｐ型ＳｉＣ基板１の表面に、ｎ型ＳｉＣ領域からなるｎベース領域を形成し、このｎベース領域の内部に、アノード領域としてのｐ型ＳｉＣ領域３２を形成可能である。この場合、ｐベース領域となるｐ型ＳｉＣ基板１の裏面には、カソード領域としてのｎ型ＳｉＣ領域が形成される。一方、ｎチャネルの接合型ＦＥＴや接合型ＳＩＴでは、チャネル領域として機能するｎ型ＳｉＣ基板１の表面に、ソース領域としてのｐ型ＳｉＣ領域３２を形成可能である。また、ｎチャネルのＳＩサイリスタでは、チャネル領域として機能するｎ型ＳｉＣ基板１の表面に、アノード領域としてのｐ型ＳｉＣ領域３２を形成可能である。

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【０１２８】ｐチャネルのパワーＩＧＴでは、ドリフト領域として機能するｐ型ＳｉＣ基板１の表面に、ドレイン領域としてのｐ型ＳｉＣ領域３２を形成可能である。この場合、ソース領域としてのｐ型ＳｉＣ領域３２が、ｐ型ＳｉＣ基板１の表面に形成されたｎボディ領域に形成される。ｎチャネルのＩＧＢＴでは、ドリフト領域として機能するｎ型ＳｉＣ基板（或いはν型ＳｉＣ基板）１の表面に、コレクタ領域としての高不純物密度のｐ型ＳｉＣ領域３２を形成可能である。この場合、エミッタ領域としての他のｎ型ＳｉＣ領域が、ｎ型（或いはν型）ＳｉＣ基板１の表面に形成されたｐボディ領域に形成される。本発明の第２の実施の形態に係るオーミック電極構造体は、これら種々の半導体電子デバイスの主電極領域として機能するｐ型ＳｉＣ領域３２に適用可能である。

【０１２９】次に、図９～図１１に示す工程断面図（その１～その３）を参照しながら本発明の第２の実施の形態に係るオーミック電極構造体の製造工程を説明する。

【０１３０】（イ）先ず、厚さ約１．５μｍのSiO_2膜３３を、ＣＶＤ法で４Ｈ－ＳｉＣ基板１の表面全面に堆積し、その上にフォトレジスト３４をスピンコートする。そして、図９（ａ）に示すように、ｐ型ＳｉＣ領域形成予定領域の上に堆積したSiO_2膜３３を周知のフォトリソグラフィ法とウェット・エッチング技術で選択的に除去し、イオン注入マスク膜３３を形成する。

【０１３１】（ロ）そして、図９（ｂ）に示すように、イオン注入マスク膜３３の上に、再びＣＶＤ法で薄いSiO_2膜からなるイオン注入スルー膜３５を全面に堆積する。イオン注入スルー膜３５は、後述のイオン注入時の射影飛程（深さ）R_pを調節するための膜である。イオン注入スルー膜３５を堆積した後、ＳｉＣ基板１全面に$^{27}Al^+$や$^{11}B^+$（ホウ素）などのｐ型不純物イオンを、少なくともＳｉＣ基板１の表面の不純物密度が$1\times10^{20}/cm^3$以上になり、且つ、ＳｉＣ基板１の結晶性を損なわないようにイオン注入する。ｐ型不純物イオンとしての$^{27}Al^+$を、ＳｉＣ基板１にイオン注入する場合の条件の一例を示すと、７５０℃に加熱したＳｉＣ基板１に、次のようにドーズ量Φ／加速エネルギーE_{AC}を変えながら多段注入する：

第１イオン注入$\Phi=0.9\times10^{15}cm^{-2}/E_{AC}=30KeV$；

第２イオン注入$\Phi=51.2\times10^{15}cm^{-2}/E_{AC}=60KeV$；

第３イオン注入$\Phi=1.5\times10^{15}cm^{-2}/E_{AC}=100KeV$；

第４イオン注入$\Phi=2.4\times10^{15}cm^{-2}/E_{AC}=150KeV$；

第５イオン注入$\Phi=3.0\times10^{15}cm^{-2}/E_{AC}=190KeV$。

【０１３２】（ハ）５段の多段イオン注入が終了したところで、イオン注入マスク膜３３とイオン注入スルー膜３５をフッ酸（ＨＦ）で全面除去する。そして、常圧Ａｒ雰囲気で１７００℃１分の急速加熱処理を行うと、イオン注入された$^{27}Al^+$が活性化されて、図９（ｃ）に示すように、高不純物密度を有するｐ型ＳｉＣ領域３２が選択的に形成される。

【０１３３】（ニ）ここから後の工程は、第１の実施の形態の製造工程で説明した図３（ｃ）以下の工程とほぼ同様である。即ち、ＲＣＡ洗浄法等のＳｉＣ基板１洗浄法を用いて、ＳｉＣ基板１を十分清浄化する。そして、図１０（ｄ）に示すように、十分清浄化されたＳｉＣ基板１の表面を、乾燥酸素雰囲気で熱酸化し、表面に、厚さ５～２０ｎｍの熱酸化膜３を成長する。

【０１３４】（ホ）次に、図１０（ｅ）に示すように、熱酸化膜３の上に、常圧ＣＶＤ法でSiO_2膜からなる上部絶縁膜４を堆積し、２層構造からなるフィールド絶縁膜５を形成する。

【０１３５】（ヘ）次にフィールド酸絶縁膜５の表面に厚さ１～２μｍのフォトレジスト２２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト２２を選択的に露光し、現像することによって開口部６に対応する部分のフォトレジスト２２を除去する。続いて、このフォトレジスト２２のパターンをエッチングマスクとして用い、ＳｉＣ基板１をＢＨＦ溶液に浸漬しウェット・エッチングすることで、図１０（ｆ）に示すように、フィールド絶縁膜５に開口部６を形成する。

【０１３６】（ト）その後、エッチングマスクとしてのフォトレジスト２２を残存した状態で、超純水で完全にリンスした後、乾燥する。そして、レジストマスク２２が被着した状態のＳｉＣ基板１を、真空蒸着装置のチャンバー中に据え付け、直ちに真空排気する。そして、真空蒸着装置のチャンバーをターボ分子ポンプ、クライオポンプ等で、1.3×10^{-5}Ｐａ未満の圧力まで真空排気し、図１１（ｇ）に示すように、ＳｉＣ基板１の表面にＡｌ－Ｔｉ系電極膜１７を蒸着する。

【０１３７】（チ）Ａｌ－Ｔｉ系電極膜１７の真空蒸着後、ＳｉＣ基板１を真空蒸着装置のチャンバーから取り出す。続いて、リフトオフ法を用いて、図１１（ｈ）に示すように、開口部のみにＡｌ－Ｔｉ系電極膜７が選択的に埋設された基板構造を得る。即ち、フォトレジスト２２を完全に除去すると、図１１（ｈ）に示すように、開口部のみにＡｌ－Ｔｉ系電極膜７が選択的に残存する。

【０１３８】（リ）しかる後、ＳｉＣ基板１を７００℃～１０５０℃の非酸化性雰囲気で短時間（数分程度）の熱処理を施すと、図１１（ｉ）に示すように、Ａｌ－Ｔｉ系電極膜とＳｉＣ基板１が相互に反応して、両者の界面領域に加熱反応層８が生成される。この際、熱処理雰囲気に含まれる酸素及び水の分圧は少なくとも、１×１

10^{-3}Ｐａ～1×10^{-10}Ｐａ程度に制御する。この結果、加熱反応層８とｐ型ＳｉＣ領域３２との間で優れたオーミック特性が実現される。Ａｌ－Ｔｉ系電極膜２７として、Ａｌ層の上にＴｉ層を堆積したＡｌ／Ｔｉ積層膜においては、熱処理前の下層のＡｌ層が熱処理により加熱反応層８となる。このとき、熱処理前のＴｉ層は、下部にＴｉ－Ｓｉ合金膜が生成され、このＴｉ－Ｓｉ合金膜と上部の未反応のＴｉ膜との積層膜からなる電極膜７が加熱反応層８の上に生成される。Ａｌ－Ｔｉ系電極膜２７として、Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜においては、熱処理前のＴｉ層が熱処理により加熱反応層８となり、熱処理前のＡｌ層は、下部にＡｌ－Ｓｉ合金膜が生成され、上部に未反応のＡｌ膜が残留するので、Ａｌ－Ｓｉ／Ａｌ層からなる電極膜７が加熱反応層８の上に生成される。Ａｌ－Ｔｉ系電極膜２７としてＡｌ－Ｔｉ合金膜を用いた場合には、熱処理前の下部のＡｌ－Ｔｉ合金膜が熱処理により加熱反応層８となり、熱処理前の最上部には未反応のＡｌ－Ｔｉ合金膜が残る。また、加熱反応層８との境界部には、Ａｌ－Ｔｉ－Ｓｉ合金膜が生成されるので、Ａｌ－Ｔｉ－Ｓｉ／Ａｌ－Ｔｉ層からなる電極膜７が加熱反応層８の上に生成される。熱反応層８としては、金属の炭化物と金属シリコンとを含む固溶体が形成される。加熱反応層８の形成後に、第１の実施の形態で説明した図５（ｉ）と同様に、ＳｉＣ基板１１全面にＡｌ等の導体膜１９を蒸着する。そして、フォトリソグラフィ法とＲＩＥ等のエッチング技術でパターニングして、図８に示すような配線導体素片９を形成すれば、本発明の第２の実施の形態に係るオーミック電極構造体が完成する。

【０１３９】本発明の第２の実施の形態に係るオーミック電極構造体の効果を精密に評価するために、第１の実施の形態と同様なリニアＴＬＭコンタクト群を作製した。評価した試料の構成は次の通りである。ｐ型ＳｉＣ領域３２（＝イオン注入層）の不純物Ａｌのドーピング密度は加熱反応層８と接する付近で3×10^{20}／cm^3である。他の条件は、第１の実施の形態に係るオーミック電極構造体と同じである。即ち、Ａｌ－Ｔｉ系電極膜７はＴｉ（５０ｎｍ厚）／Ａｌ（３００ｎｍ厚）積層膜とし、フィールド絶縁膜５の熱酸化膜３は１１００℃ドライ酸化膜（１０ｎｍ厚）、上部絶縁膜４は常圧ＣＶＤで成膜したSiO_2膜（４００ｎｍ厚）である。加熱反応層８を形成するための熱処理温度及び熱処理時間、熱処理雰囲気はそれぞれ１０００℃、５分、純Ａｒ雰囲気であった。

【０１４０】ＴＬＭ法により得られたコンタクト抵抗ρcは$\rho c=4.3\times10^{-7}\Omega cm^2$であった。第１の実施の形態より低い値が得られたのは、高ドーズ量のイオン注入と効果的な活性化アニールで、高不純物密度が得られたためと考えられる。つまり、高不純物密度ｐ型ＳｉＣ領域３２の存在により、加熱反応層８とｐ型ＳｉＣ領域３２界面のショットキー障壁がより薄くなったためと考えられる。他の条件を同じにして、このＴｉ／Ａｌ積層電極膜の替わりに、Ａｌ－Ｔｉ合金膜（４００ｎｍ厚、Ｔｉ：１０％含有）でｐ型オーミック・コンタクトを形成するとＴｉ／Ａｌ積層電極膜より数倍高いものの、従来技術に比べれば低い$\rho c=1.2\times10^{-6}\Omega cm^2$が得られる。

【０１４１】このように本発明の第２の実施の形態に係るオーミック電極構造体によれば、$10^{-6}\Omega cm^2$台或いはこれ以下の実用的なコンタクト抵抗ρcを達成出来る。この結果、実際のデバイス構造に採用可能な微細な開口部（コンタクト・ウインドウ）の内部において、低いコンタクト抵抗ρcを得ることが出来、単純化された構成で、高性能なＳｉＣ電子デバイスを簡単に製造出来る。

【０１４２】（第３の実施の形態）図１２に示す本発明の第３の実施の形態に係るオーミック電極構造体は、電極膜４７の平面寸法が開口部より大きく、フィールド絶縁膜５に重畳するように配設している点が、第１及び第２の実施の形態に係るオーミック電極構造体とは異なる。

【０１４３】ｐ型ＳｉＣ領域３２は第１の実施の形態のような高不純物密度のｐ型エピタキシャル成長層からなるＳｉＣ領域で構成してもいいし、第２の実施の形態のような選択イオン注入領域で構成しても良い。ここではイオン注入法で形成する例で説明する。第１及び第２の実施の形態と同様に、ｐ型ＳｉＣ領域３２は、半導体装置、特に半導体電子デバイスの主電極領域として機能する。

【０１４４】図１２に示すように、本発明の第３の実施の形態に係るオーミック電極構造体は、ＳｉＣ基板１、ＳｉＣ基板１の表面に選択的に形成されたｐ型ＳｉＣ領域３２、このｐ型ＳｉＣ領域３２の表面の一部に形成された加熱反応層８、ＳｉＣ基板１とｐ型ＳｉＣ領域３２との界面を覆う熱酸化膜３、熱酸化膜３の表面に配置された上部絶縁膜４、加熱反応層８の上部に配置された電極膜４７とを少なくとも有する。熱酸化膜３と、上部絶縁膜４との積層構造により、フィールド絶縁膜５を構成している。熱酸化膜３は、加熱反応層８が貫通する第１の開口部を有し、且つＳｉＣ基板１とｐ型ＳｉＣ領域３２との界面を覆うように、ＳｉＣ基板１とｐ型ＳｉＣ領域３２の表面に接して配置されている。上部絶縁膜４は、熱酸化膜３とは組成若しくは密度の異なる絶縁膜であって、第１の開口部に連続した第２の開口部を有している。

【０１４５】加熱反応層８は、ｐ型ＳｉＣ領域３２の表面の一部から内部に進入すると同時に、ｐ型ＳｉＣ領域３２の表面から上方に突出して形成されている。そして、加熱反応層８の上部に配設された電極膜４７が、第２の開口部から伸延し、第２の開口部の周辺に位置する

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フィールド絶縁膜５の上部に重畳している。つまり、Ａ電極膜４７は、第２の開口部を完全に封じるように、第２の開口部よりも大きな平面パターンで形成されている。更に、第２の開口部を完全に封じた電極膜４７に電気的に接続するように、配線導体素片９が形成されている。配線導体素片９は、半導体装置の主電極配線として機能する。従って、設計にもよるが、配線導体素片９は所定のボンディングパッドにまで接続される主電極配線でも良い。この配線導体素片９は、フィールド絶縁膜５の上にＡｌ、Ａｌ－Ｓｉ共晶、Ａｌ－Ｃｕ－Ｓｉ共晶、Ｃｕ、Ｔｉ－Ｗ合金等の導電性材料で形成されている。

【０１４６】図１２に示す電極膜４７は、下部のＡｌ－Ｓｉ合金膜と上部の未反応のＡｌ膜とからなる積層膜である。ＡＥＳ測定によれば、Ｔｉ／Ａｌ積層膜を、１００℃で２分間熱処理した場合には、加熱反応層８は、ＴｉＣと金属シリコンとを含む固溶体であることが推定出来る。このＴｉＣと金属シリコンとを含む固溶体からなる加熱反応層８が、金属／半導体接合におけるショットキー障壁を極めて低くし、且つ、界面のモホロジーを良好にし、結果として、加熱反応層８を均一に生成出来ると判断される。熱処理前に堆積されるＴｉ／Ａｌ積層膜の上層のＡｌ膜を、Ｓｉ半導体電子デバイスの配線で多用されているＡｌ－Ｓｉ共晶膜に替えることも出来る。この場合は、電極膜４７は、下部のＡｌ－Ｓｉ合金膜と上部の未反応のＡｌ－Ｓｉ合金膜とからなり、Ｓｉの組成に分布を有した合金膜となる。

【０１４７】なお、Ａｌは６６０℃以上の高温にすると融解し、フィールド絶縁膜５との密着性及び濡れ性が著しく低下するので、第３の実施の形態において、フィールド絶縁膜５の周縁部に、直接Ａｌ層が接触するＡｌ／Ｔｉ積層電極は、加熱反応層８形成用の原料となる電極材料としては適さない。

【０１４８】本発明の第１の実施の形態で定義したように、第３の実施の形態に係るオーミック電極構造体において、「熱酸化膜３とは組成の異なる絶縁膜」とは、ＰＳＧ膜、ＢＳＧ、ＢＰＳＧ或いはSi_3N_4膜等の絶縁膜の意である。また、「熱酸化膜３とは密度の異なる絶縁膜」とは、熱酸化膜以外の方法、例えば、ＣＶＤ法、スパッタリング法、真空蒸着法等で堆積したSiO_2膜等の絶縁膜が該当する。熱酸化膜３の厚みは２～５０ｎｍであることが望ましい。特に、５～２０ｎｍの範囲の熱酸化膜３の厚みが望ましい。第１の実施の形態で説明したように熱酸化膜３の厚みが、５ｎｍより薄い場合は表面研磨やイオン注入法で生じたＳｉＣ基板１表面の損傷領域を除去する効果ならびに表面の異物を除去する効果が乏しくなる。一方、熱酸化膜３の厚みが、５０ｎｍより厚い場合は過度な熱酸化によりＳｉＣ基板１表面が次第に荒れ、表面モホロジーが低下するからである。熱酸化膜３の厚みと上部絶縁膜４の厚みとを合計したフィールド絶縁膜５の総厚は、１００ｎｍ～３μｍであることが望ましい。特に、３００ｎｍ以上であることが望ましい。また、高耐圧の電力用半導体装置であれば、８００ｎｍ以上にすれば良い。但し、フィールド絶縁膜５があまり厚くなると、クラック等が発生するので、３μｍ以上は好ましくない。

【０１４９】図１２に示すようなＳｉＣの熱酸化膜以外の種々のSiO_2膜等の上部絶縁膜４を、ＳｉＣの熱酸化膜３の上部に形成した積層構造を採用すれば、半導体装置の仕様として要求される耐圧や表面の安定性を確保しつつ、ＳｉＣの表面モホロジーを良好に維持出来る。

【０１５０】ｐ型ＳｉＣ領域３２の表面正孔密度は、少なくとも1×10^{17}／cm^3以上、好ましくは1×10^{18}／cm^3以上であることが望ましい。ＳｉＣ基板１の導電型や不純物密度は第３の実施の形態に係るオーミック電極構造体を利用する半導体装置によって異なる。例えば、第２の実施の形態に係るオーミック電極構造体の適用例と同様に、種々の半導体電子デバイスの主電極領域として機能するｐ型ＳｉＣ領域３２を、その設計に適合して選ばれた導電型及び不純物密度を有するＳｉＣ基板１の上に（直接若しくは他の半導体領域を介して）形成可能である。従って、ＳｉＣ基板１の導電型や不純物密度は、ここでは規定しない。

【０１５１】次に図１３及び図１４に示す工程断面図（その１及びその２）を参照しながら本発明の第３の実施の形態に係るオーミック電極構造体の製造工程を説明する。

【０１５２】（イ）第２の実施の形態で説明した方法と全く同様に、フォトリソグラフィ法及びイオン注入法等を用いて、ｐ型ＳｉＣ領域３２を、４Ｈ－ＳｉＣ基板１の表面に選択的に形成する。即ち、ＳｉＣ基板１の表面に、ＡｌイオンＸはＢイオンなどのｐ型不純物イオンを注入して、熱処理により活性化し、ｐ型ＳｉＣ領域３２を形成する。そして、第２の実施の形態の製造工程で説明した図１０（ｄ）以下の工程とほぼ同様に、十分清浄化されたＳｉＣ基板１の表面を、乾燥酸素雰囲気で熱酸化し、表面に熱酸化膜３を成長する。次に、図１３（ａ）に示すように、熱酸化膜３の上に、常圧ＣＶＤ法でSiO_2膜からなる上部絶縁膜４を堆積し、２層構造からなるフィールド絶縁膜５を形成する。

【０１５３】（ロ）次にフィールド酸絶縁膜５の表面に厚さ１～２μｍのフォトレジスト２２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト２２を選択的に露光し、現像することによって開口部６に対応する部分のフォトレジスト２２を除去する。続いて、このフォトレジスト２２のパターンをエッチングマスクとして用い、ＳｉＣ基板１をＢＨＦ溶液に浸漬しウェット・エッチングすることで、図１３（ｂ）に示すように、フィールド絶縁膜５に開口部６を形成する。

【０１５４】（ハ）その後、アセトン又は専用のフォト

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レジスト剥離液を用いてエッチングに使用したフォトレジスト２２を剥離する。続いて、ＳｉＣ基板１をＢＨＦ溶液に約１０秒浸漬し、フィールド絶縁膜５を僅かにエッチングすることによって、フィールド絶縁膜５に付着したフォトレジスト２２の残滓を完全に除去する。フィールド絶縁膜５に残ったフォトレジスト２２の残滓は、フィールド絶縁膜５に重畳するように配設する電極膜４７（又は１７，５７）のフィールド絶縁膜５に対する付着力を著しく低下させるので、この工程は欠かせない。ＢＨＦ溶液を超純水で完全に濯ぎ落とし、乾燥したＳｉＣ基板１を速やかに、蒸着装置のチャンバーの中に据え付け、直ちに真空排気する。所定の到達圧力が得られたら、開口部６の内部及びフィールド絶縁膜５の表面全面に、図１３（ｃ）に示すように、Ａｌ－Ｔｉ系電極膜１７として、５０ｎｍ厚のＴｉ層、及びこの上の３００ｎｍ厚のＡｌ層からなるＴｉ／Ａｌ積層膜を蒸着する。開口部６におけるステップカバレージを向上させるため、第１及び第２の実施の形態とは異なり、斜め蒸着法を採用することが好ましい。

【０１５５】（ニ）Ａｌ－Ｔｉ系電極膜１７としてのＴｉ／Ａｌ積層膜の真空蒸着後、ＳｉＣ基板１を真空蒸着装置のチャンバーから取り出す。続いて、Ａｌ－Ｔｉ系電極膜（Ｔｉ／Ａｌ積層膜）１７の表面に、厚さ１～２μｍのフォトレジスト２３をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト２３を選択的に露光し、現像することによって、図１４（ｄ）に示すように、開口部とその周縁部のフィールド絶縁膜５の一部の上部にのみ、選択的にフォトレジスト２３を残存させる。

【０１５６】（ホ）続いて、このフォトレジスト２３のパターンをエッチングマスクとして図１４（ｅ）に示すように、開口部とその周縁部のフィールド絶縁膜５の上部の一部にのみ、Ａｌ－Ｔｉ系電極膜５７を残して、他の部分のＡｌ－Ｔｉ系電極膜１７は除去する。エッチングはウェット・エッチングでもドライ・エッチングでも構わない。ウェット・エッチングのエッチャントとして燐酸（H_3PO_4）：硝酸（HNO_3）：酢酸（CH_3COOH）混合液を用いることが出来る。ドライ・エッチングのエッチャント・ガスとしては塩素（Cl_2）：３臭化ホウ素（BBr_3）混合ガスを用いることが出来る。エッチングが終了したら専用のフォトレジスト剥離液に浸漬させ、濯いで乾燥させる。乾燥後、酸素プラズマ灰化装置にかけ、続いて、Ａｒスパッタエッチャにかけ、フォトレジストの灰化で生じたＡｌ－Ｔｉ系電極膜５７の表面の酸化膜を完全に除去する。

【０１５７】（ヘ）しかる後、ＳｉＣ基板１を７００℃～１０５０℃の非酸化性雰囲気で短時間（数分程度）の熱処理を施すと、図１４（ｆ）に示すように、Ａｌ－Ｔｉ系電極膜５７とｐ型ＳｉＣ領域３２が相互に反応して、両者の界面領域に加熱反応層８が生成される。この際、熱処理雰囲気に含まれる酸素及び水の分圧は少なくとも、1×10^{-3} Ｐａ～1×10^{-10} Ｐａ程度に制御する。この結果、加熱反応層８とｐ型ＳｉＣ領域３２との間で優れたオーミック特性が実現される。Ａｌ－Ｔｉ系電極膜５７として、Ｔｉ層の上にＡｌ層を堆積したＴｉ／Ａｌ積層膜においては、主に、熱処理前のＴｉ層が熱処理により加熱反応層８となる。一方、熱処理前のＡｌ層は、下部にＡｌ－Ｓｉ合金膜が生成され、上部に未反応のＡｌ膜が残留するので、Ａｌ－Ｓｉ／Ａｌ層からなる電極膜７が加熱反応層８の上に生成される。熱反応層８としては、金属の炭化物と金属シリコンとを含む固溶体が形成される。

【０１５８】（ト）最後に、第１及び第２の実施の形と同様に、ＳｉＣ基板１の全面にＡｌ等の導体膜を蒸着して、フォトリソグラフィ法とエッチング法でパターニングして配線導体素片９を形成し、図１２に示すｐ型ＳｉＣ領域３２に対するオーミック電極構造体が完成する。なお、配線パターニングのエッチャント（＝エッチング液或いはエッチングガス）が電極膜４７を侵す時は、配線導体素片９は必ず電極膜４７を覆うように配設する構成とする。

【０１５９】本発明の第３の実施の形態に係るオーミック電極構造体の効果を精密に評価するために、リニアＴＬＭコンタクト群を作製した。ｐ型ＳｉＣ領域３２（＝イオン注入層）の不純物Ａｌのドーピング密度は加熱反応層８と接する付近で3×10^{20}／cm^3である。フィールド絶縁膜５を構成している熱酸化膜３は１１００℃ドライ酸化膜（１０ｎｍ厚）、上部絶縁膜４は常圧ＣＶＤで成膜したSiO_2膜（４００ｎｍ厚）である。加熱反応層８を形成するための熱処理温度及び熱処理時間、熱処理雰囲気はそれぞれ１０００℃、５分、純Ａｒ雰囲気であった。

【０１６０】ＴＬＭ法により得られたコンタクト抵抗ρｃはρｃ＝6.4×10^{-7}Ωcm^2と第２の実施の形態のＴｉ／Ａｌ積層電極の場合とほぼ同じ値が得られた。

【０１６１】（その他の実施の形態）上記のように、本発明は第１乃至第３の実施の形態によって記載したが、この開示の一部をなす論述及び図面はこの発明を限定するものであると理解すべきではない。この開示から当業者には様々な代替実施の形態、実施例及び運用技術が明らかとなろう。

【０１６２】上記の第１乃至第３の実施の形態の製造プロセスにおいては、フィールド絶縁膜５の要素である熱酸化膜３は上部絶縁膜４形成の直前に形成する構成となっているが、図１５の工程断面図に示すように、熱酸化膜の形成を上部絶縁膜４形成の直後にする構成としても、ほぼ同様な効果が得られる。

【０１６３】（イ）例えば、第２の実施の形態で説明した方法と全く同様の方法で、ＳｉＣ基板１の表面にｐ型ＳｉＣ領域３２を形成する。そして、ＲＣＡ洗浄法等の

ＳｉＣ基板１洗浄法を用いて、ＳｉＣ基板１を十分清浄化する。この後、ＳｉＣ基板１の上に、図１５（ａ）に示すように、常圧ＣＶＤ法でSiO_2膜等の酸素透過性絶縁膜４４を堆積する。

【０１６４】（ロ）酸素透過性絶縁膜４４を堆積後、図１５（ｂ）に示すように、乾燥酸素雰囲気で熱処理し、ＳｉＣ基板１の表面を熱酸化し、酸素透過性絶縁膜４４とＳｉＣ基板１との界面に熱酸化膜３を成長する。第１の実施の形態と同様に、熱酸化膜３の厚さは５０ｎｍ未満、好ましくは５～２０ｎｍが望ましい。この結果、熱酸化膜３の上に、酸素透過性絶縁膜（SiO_2膜）４４からなる上部絶縁膜４が位置し、２層構造からなるフィールド絶縁膜５が形成される。

【０１６５】（ハ）この後は、第２の実施の形態で説明した図１０（ｆ）以下に示す方法と全く同様の工程を進めることが可能である。即ち、図１５（ｃ）に示すように、フィールド酸絶縁膜５の表面に厚さ１～２μｍのフォトレジスト２２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト２２を選択的に露光し、現像することによって開口部６に対応する部分のフォトレジスト２２を除去する。続いて、このフォトレジスト２２のパターンをエッチングマスクとして用い、ウェット・エッチングすることで、図１５（ｃ）に示すように、フィールド絶縁膜５に開口部６を形成する。この後の説明は、重複するので省略する。

【０１６６】図１５に示す方法を用いても、$10^{-6}\Omega cm^2$台或いはこれ以下の実用的なコンタクト抵抗ρcを達成することが可能である。

【０１６７】更に、図１６及び図１７の工程断面図（その１及びその２）に示すように、熱酸化膜の形成を開口部形成の直後に実施しても良い。

【０１６８】（イ）例えば、第２の実施の形態で説明した方法と全く同様の方法で、ＳｉＣ基板１の表面にｐ型ＳｉＣ領域３２を形成する。そして、ＳｉＣ基板１を十分清浄化後、ＳｉＣ基板１の上に、図１６（ａ）に示すように、常圧ＣＶＤ法でSiO_2膜等の酸素透過性絶縁膜４４を堆積する。

【０１６９】（ロ）次に酸素透過性絶縁膜４４の表面に厚さ１～２μｍのフォトレジスト２２をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト２２を選択的に露光し、現像することによって開口部６に対応する部分のフォトレジスト２２を除去する。続いて、このフォトレジスト２２のパターンをエッチングマスクとして用い、酸素透過性絶縁膜４４をウェット・エッチングすることで、図１６（ｂ）に示すように、酸素透過性絶縁膜４４に開口部６を形成する。

【０１７０】（ハ）開口部６の形成後、アセトン又は専用のフォトレジスト剥離液を用いて、酸素透過性絶縁膜４４のエッチングに使用したフォトレジスト２２を剥離する。続いて、ＳｉＣ基板１をＢＨＦ溶液に約１０秒浸漬し、酸素透過性絶縁膜４４を僅かにエッチングすることによって、酸素透過性絶縁膜４４に付着したフォトレジスト２２の残滓を完全に除去する。更に、ＲＣＡ洗浄法等のＳｉＣ基板１洗浄法を用いて、開口部６の内部に露出したＳｉＣ基板１の表面を十分清浄化する。そして、図１６（ｃ）に示すように、乾燥酸素雰囲気で熱酸化し、開口部６の内部に露出したＳｉＣ基板１の表面、及び酸素透過性絶縁膜４４とＳｉＣ基板１との界面に熱酸化膜３を成長する。開口部６の内部に露出したＳｉＣ基板１の表面の酸化速度は、酸素透過性絶縁膜４４とＳｉＣ基板１との界面における酸化速度よりも速いので、開口部６の内部に露出したＳｉＣ基板１の表面の方が厚い熱酸化膜が形成される。酸素透過性絶縁膜４４とＳｉＣ基板１との界面における熱酸化膜３の厚さは５０ｎｍ未満、好ましくは５～２０ｎｍが望ましい。５ｎｍより薄い場合は表面研磨やイオン注入法で生じたＳｉＣ基板１表面の損傷領域を除去する効果ならびに表面の異物を除去する効果が乏しく、５０ｎｍより厚い場合は過度な熱酸化によりＳｉＣ基板１表面が次第に荒れるからである。

【０１７１】（ニ）その後、ＢＨＦ溶液で全面エッチングして、図１７（ｄ）に示すように、開口部６の内部に露出したＳｉＣ基板１の表面の熱酸化膜３を、自己整合的に除く。

【０１７２】（ホ）乾燥させたＳｉＣ基板１を速やかに、蒸着装置のチャンバーの中に据え付け、直ちに真空排気する。所定の到達圧力が得られたら、開口部６の内部及びフィールド絶縁膜５の表面全面に、図１７（ｅ）に示すように、斜め蒸着法でＡｌ－Ｔｉ系電極膜１７を蒸着する。

【０１７３】（ヘ）Ａｌ－Ｔｉ系電極膜１７の真空蒸着後、ＳｉＣ基板１を真空蒸着装置のチャンバーから取り出す。続いて、Ａｌ－Ｔｉ系電極膜１７の表面に厚さ１～２μｍのフォトレジスト２３をスピンナーを用いて塗布する。そして、所定のフォトマスク（レティクル）を用い、フォトレジスト２３を選択的に露光し、現像することによって、開口部とその周縁部のフィールド絶縁膜５に重畳する一部にのみ、選択的にフォトレジスト２３を残存させる。続いて、このフォトレジスト２３のパターンをエッチングマスクとして図１７（ｆ）に示すように、開口部とその周縁部のフィールド絶縁膜５の上部の一部にのみ、Ａｌ－Ｔｉ系電極膜５７を残して、他の部分のＡｌ－Ｔｉ系電極膜１７は除去する。

【０１７４】（ト）しかる後、第３の実施の形態で説明した、図１４（ｆ）以下の方法と全く同様に、ＳｉＣ基板１を７００℃～１０５０℃の非酸化性雰囲気で短時間（数分程度）の熱処理を施し、Ａｌ－Ｔｉ系電極膜５７とｐ型ＳｉＣ領域３２が相互に反応して、両者の界面領

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域に加熱反応層８を生成する。この後の工程の説明は、第３の実施の形態の説明と重複するので省略する。

【０１７５】図１６及び図１７に示す方法を用いても、$10^{-6}\Omega cm^2$台或いはこれ以下の実用的なコンタクト抵抗ρcを達成することが可能である。

【０１７６】また、以上において、パワーデバイス等の半導体電子デバイスに付いて主に記載したが、本発明は発光ダイオードや半導体レーザ等の半導体発光デバイスやこれを用いた光集積回路等に適用可能なことは勿論である。

【０１７７】このように、本発明はここでは記載していない様々な実施の形態等を含むことは勿論である。従って、本発明の技術的範囲は上記の説明から妥当な特許請求の範囲に係る発明特定事項によってのみ定められるものである。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態に係るオーミック電極構造体の構成を示す要部断面図である。

【図２】オージェ電子分光（ＡＥＳ）法を用いて、本発明の第１の実施の形態に係るオーミック電極構造体の深さ方向の組成を分析した結果を示す図である。

【図３】本発明の第１の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その１）である。

【図４】本発明の第１の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その２）である。

【図５】本発明の第１の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その３）である。

【図６】本発明の第１の実施の形態に係るオーミック電極構造体に基づくＴＬＭコンタクト群の電流－電圧特性を示す図である。

【図７】本発明の第１の実施の形態に係るオーミック電極構造体に基づくＴＬＭコンタクト群のＴＬＭ特性を示す図である。

【図８】本発明の第２の実施の形態に係るオーミック電極構造体の構成を示す要部断面図である。

【図９】本発明の第２の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その１）である。

【図１０】本発明の第２の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その２）である。

【図１１】本発明の第２の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その３）である。

【図１２】本発明の第３の実施の形態に係るオーミック電極構造体の構成を示す要部断面図である。

【図１３】本発明の第３の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その１）である。

【図１４】本発明の第３の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その２）である。

【図１５】本発明の他の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図である。

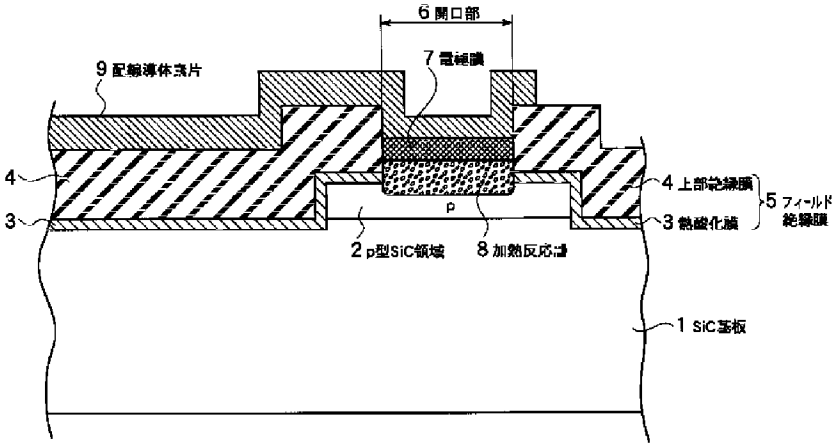
【図１６】本発明の更に他の実施の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その１）である。

【図１７】本発明の更に他の形態に係るオーミック電極構造体の製造工程を示す工程断面図（その２）である。

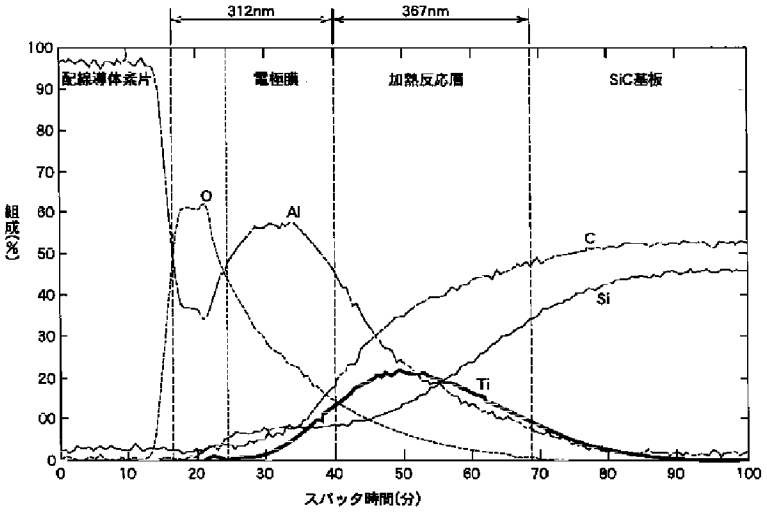
【符号の説明】

１　ＳｉＣ基板１
２，３２　ｐ型ＳｉＣ領域
３　熱酸化膜
４　上部絶縁膜
５　フィールド絶縁膜
６　フィールド絶縁膜の開口部
７，４７　電極膜
８　加熱反応層８
９　配線導体素片
１７，２７，５７　Ａｌ－Ｔｉ系電極膜
１９　Ａｌ膜
２０　エピタキシャル成長層
２１　エッチングマスク
２２，２３、３４　フォトレジスト
３３　イオン注入マスク
３５　イオン注入スルー膜
４４　酸素透過性絶縁膜

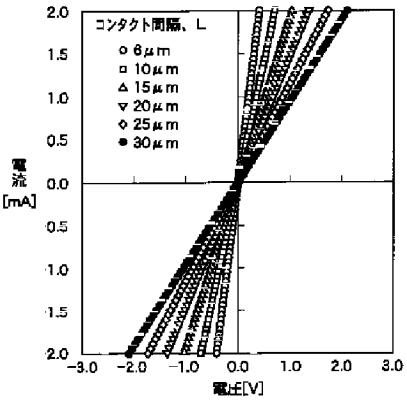
【図1】


6 開口部
7 電極膜
9 配線導体薄片
4
3
4 上部絶縁膜
5 フィールド絶縁膜
3 熱酸化膜
p
2 p型SiC領域
8 加熱反応層
1 SiC基板

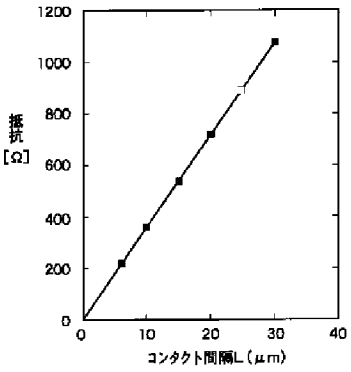
【図2】


312nm
367nm
配線導体薄片
電極膜
加熱反応層
SiC基板
O
Al
C
Si
Ti
組成(%)
スパッタ時間(分)

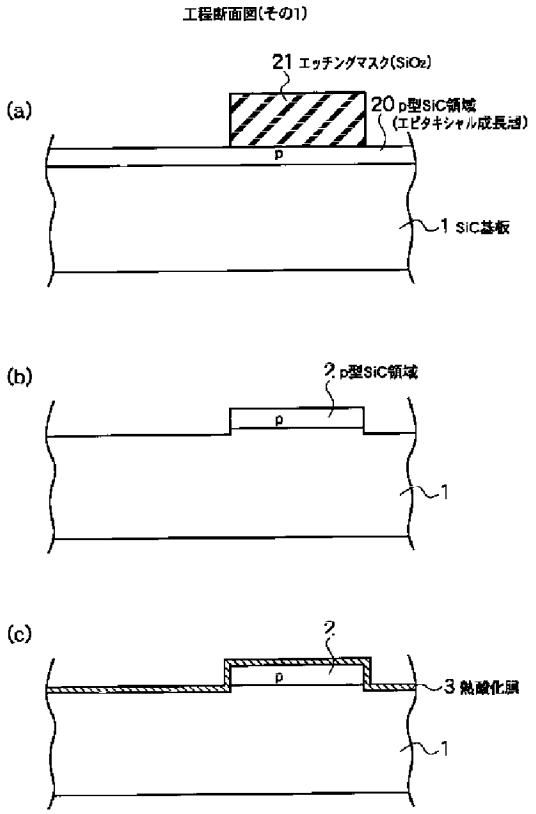
【図6】


コンタクト間隔、L
6μm
10μm
15μm
20μm
25μm
30μm
電流[mA]
電圧[V]

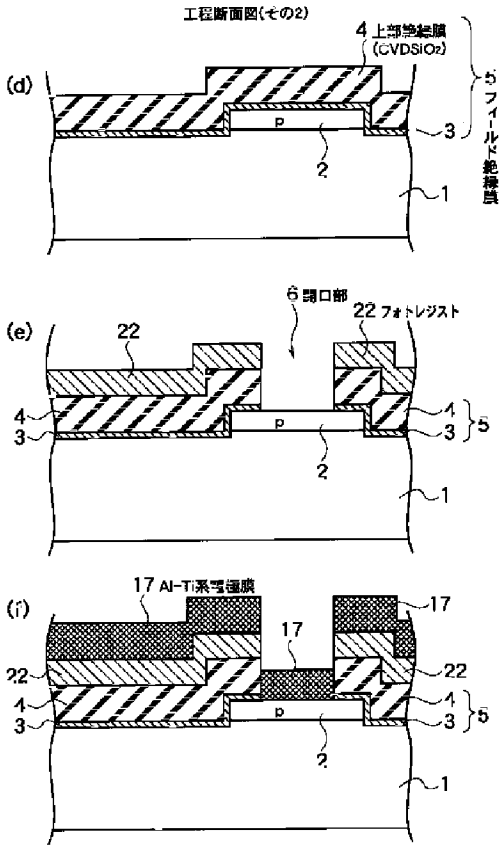
【図7】


抵抗[Ω]
コンタクト間隔L(μm)

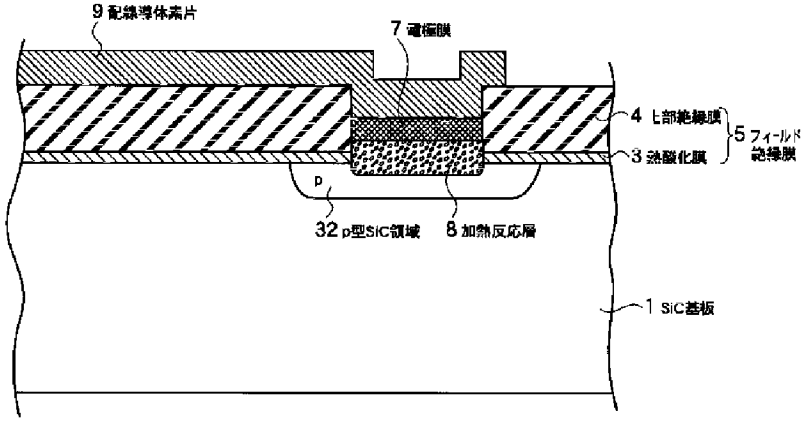
【図3】


工程断面図(その1)
(a)
21 エッチングマスク(SiO2)
20 p型SiC領域
(エピタキシャル成長法)
p
1 SiC基板
(b)
2 p型SiC領域
p
1
(c)
2
p
3 熱酸化膜
1

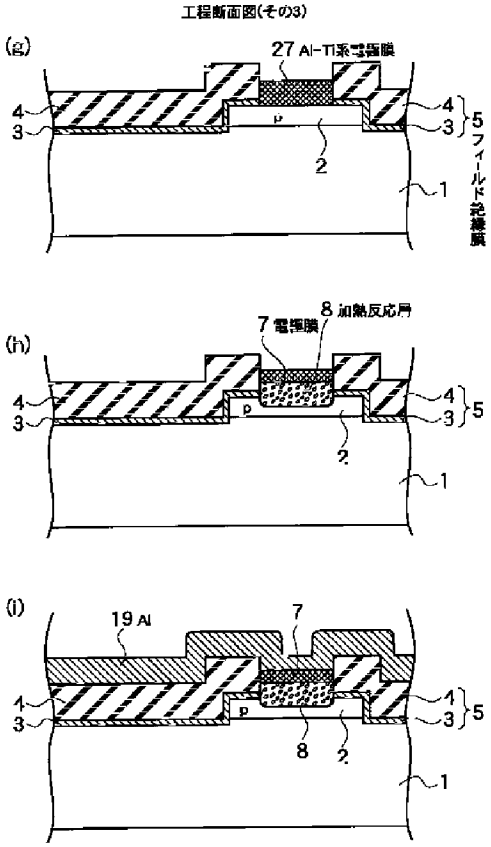
【図4】


工程断面図(その2)
(d)
4 上部絶縁膜
(CVDSiO2)
5 フィールド絶縁膜
p
3
2
1
(e)
6 開口部
22 フォトレジスト
22
4
3
p
2
1
5
(f)
17 Al-Ti系電極膜
17
22
4
3
p
2
1
5

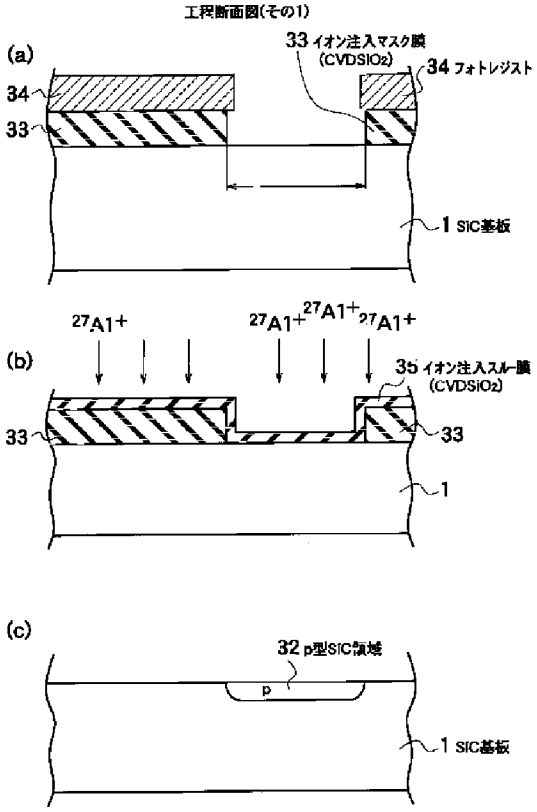
【図8】


9 配線導体素片
7 電極膜
4 上部絶縁膜
5 フィールド絶縁膜
3 熱酸化膜
p
32 p型SiC領域
8 加熱反応層
1 SiC基板

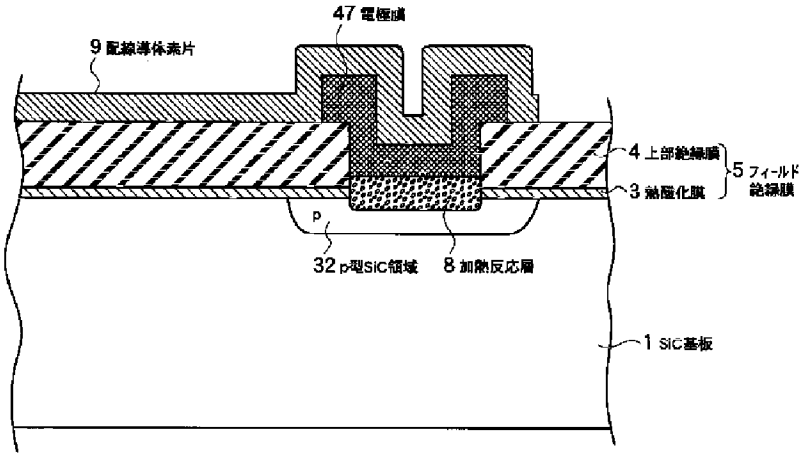
【図5】


工程断面図(その3)
(g)
27 Al-Ti系電極膜
4
3
5
フィールド絶縁膜
2
1
(h)
8 加熱反応層
7 電極膜
(i)
19 Al
7
8
2

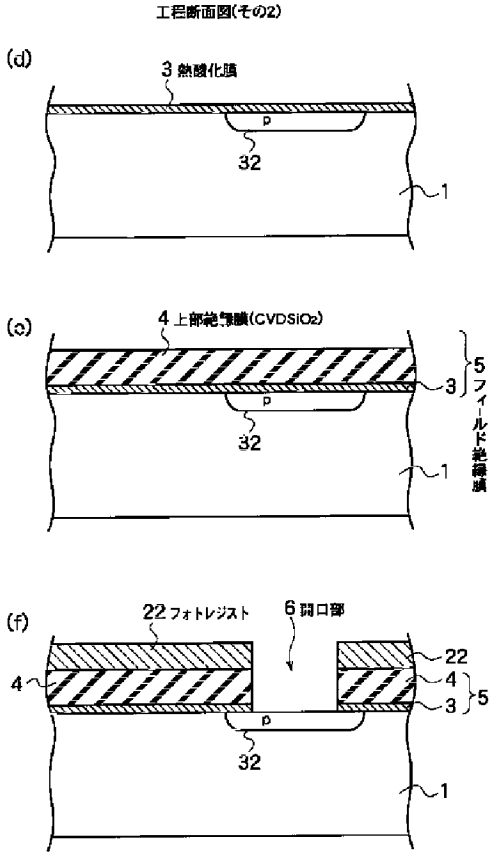
【図9】


工程断面図(その1)
(a)
33 イオン注入マスク膜
(CVDSiO2)
34 フォトレジスト
34
33
1 SiC基板
(b)
27Al+
27Al+ 27Al+ 27Al+
35 イオン注入スルー膜
(CVDSiO2)
(c)
32 p型SiC領域
1 SiC基板

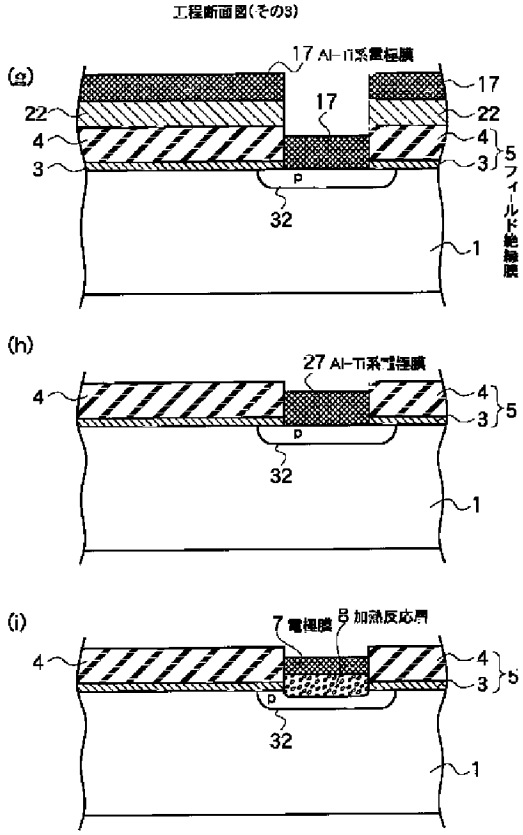
【図12】


47 電極膜
9 配線導体素片
4 上部絶縁膜
3 熱酸化膜
5 フィールド絶縁膜
32 p型SiC領域
8 加熱反応層
1 SiC基板

【図１０】

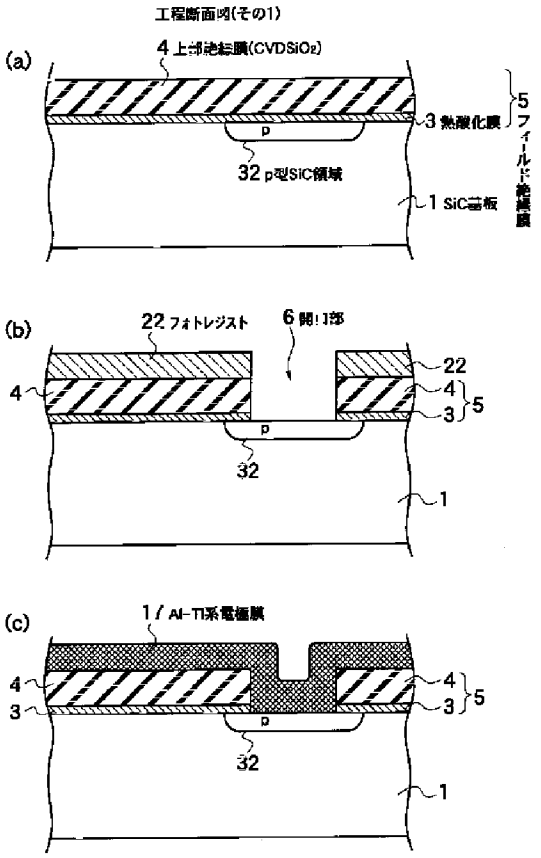


【図１１】

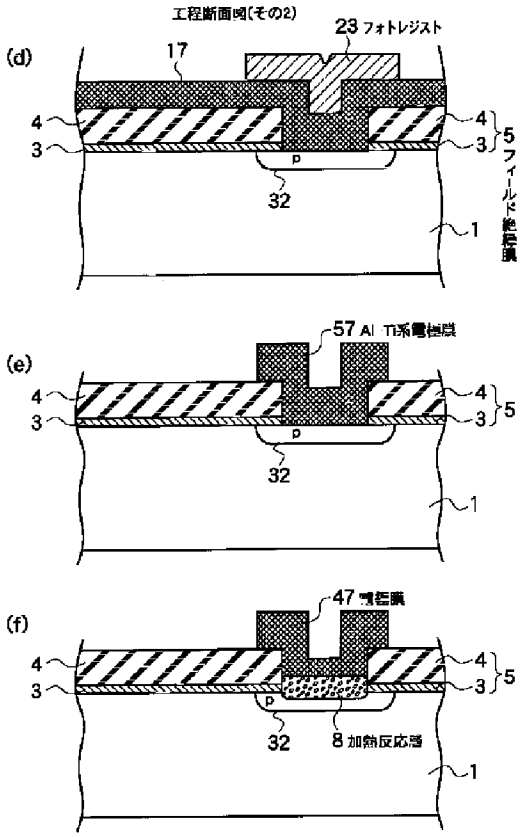


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【図13】

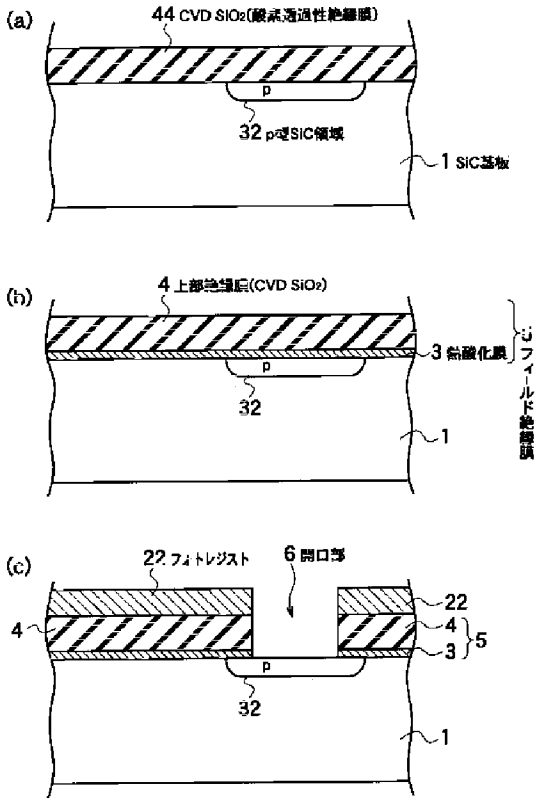


【図14】

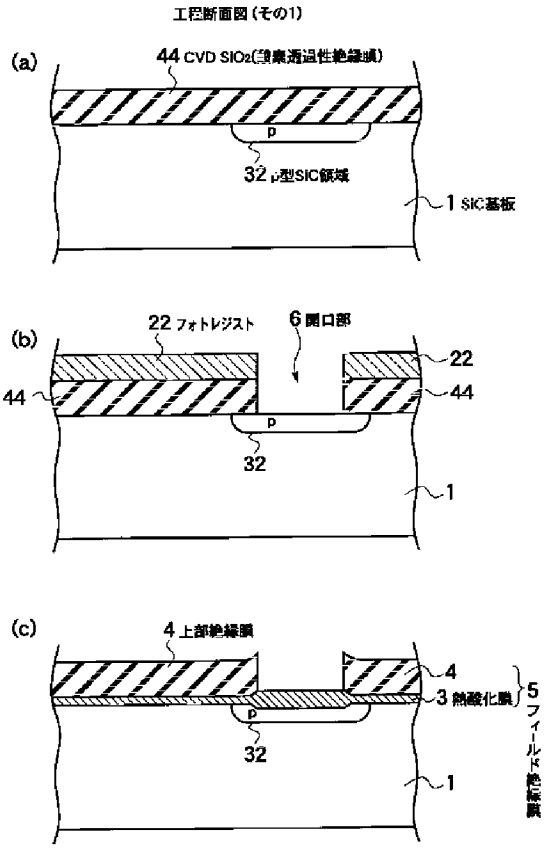


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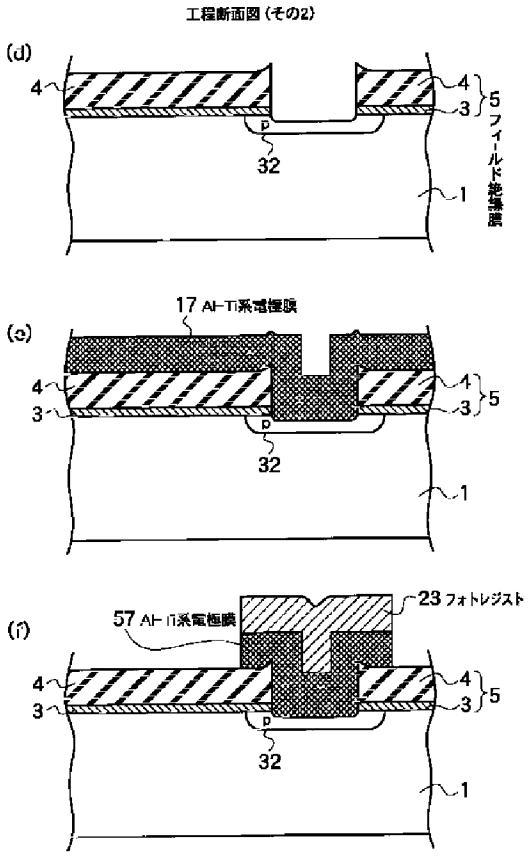
【図15】


(a)
44 CVD SiO2(酸素透過性絶縁膜)
p
32 p型SiC領域
1 SiC基板
(b)
4 上部絶縁層(CVD SiO2)
3 熱酸化膜
5 フィールド絶縁膜
p
32
1
(c)
22 フォトレジスト
6 開口部
22
4
4
3
5
p
32
1

【図16】


工程断面図（その1）
(a)
44 CVD SiO2(酸素透過性絶縁膜)
p
32 p型SiC領域
1 SiC基板
(b)
22 フォトレジスト
6 開口部
22
44
44
p
32
1
(c)
4 上部絶縁膜
4
3 熱酸化膜
5 フィールド絶縁膜
p
32
1

【図１７】



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	29/808			29/91	F
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	33/00				

(72)発明者　谷本　智
神奈川県横浜市神奈川区宝町２番地　日産
自動車株式会社内

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DD68 DD78 DD83 FF13 GG06
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BH07 BH08 BH18 BH99 BJ93
BM01 BP31 BZ01 BZ02 BZ03
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5F041 AA24 CA33 CA73 CA82 CA83
CA84 CA87 CA92 CA98
5F102 GB01 GC01 GD04 GJ02 GL02
GS01 GS02

Espacenet

JP2002075909A OHMIC ELECTRODE STRUCTURE, ITS MANUFACTURING METHOD, AND SEMICONDUCTOR DEVICE USING OHMIC ELECTRODE

Applicants: NAT INST OF ADV IND & TECHNOL,NISSAN MOTOR

Inventors: OGUSHI HIDEYO,TANIMOTO SATOSHI

Classifications:

IPC ***H01L21/265; H01L21/28; H01L21/331; H01L21/336; H01L21/337; H01L29/12; H01L29/165; H01L29/73; H01L29/744; H01L29/78; H01L29/808; H01L29/861; H01L33/12; H01L33/34; H01L33/40; H01L33/44;*** (IPC1-7): H01L21/265; H01L21/28; H01L21/331; H01L21/336; H01L21/337; H01L29/165; H01L29/73; H01L29/744; H01L29/78; H01L29/808; H01L29/861; H01L33/00;

CPC **H01L21/0485 (EP);**

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Application: JP2002075909A·2000-09-01

Publication: JP2002075909A·2002-03-15

Published as: JP2002075909A;**JP4179492B2**

OHMIC ELECTRODE STRUCTURE, ITS MANUFACTURING METHOD, AND SEMICONDUCTOR DEVICE USING OHMIC ELECTRODE

Abstract

PROBLEM TO BE SOLVED: To enable a p-type SiC region in a fine contact window to have a low contact resistance ρc. SOLUTION: An ohmic electrode structure has an SiC substrate 1, p-type SiC area 2 formed on the surface of the substrate 1, thermally reacted layer 8 formed on the surface of the area 2, thermally oxidized film 3 covering the interface between the substrate 1 and area 2, upper insulating film 4 arranged on the surface of the oxidized film 3, and electrode film 7 arranged on the reacted layer 8. The electrode film 7 is connected with a blank wiring conductor chip 9. The reacted layer 8 is upwardly protruded from the surface of the SiC area 2. The oxidized film 3 has an opening through which the reacted layer 8 is passed and is arranged in contact with the surface of the substrate 1 so as to cover the interface between the substrate 1 and area 2. The upper insulating film 4 has a composition or density which is different from that of the thermally oxidized layer 3.

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DESCRIPTION JP2002075909

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device using a silicon carbide (SiC) substrate, and further to an ohmic electrode structure for a p-type SiC region used in this SiC semiconductor device and the same. The present invention relates to a manufacturing method.

[0002]

2. Description of the Related Art SiC is capable of forming a pn junction, and has a bandgap Eg which is larger than that of other widely used semiconductor materials such as silicon (Si) and gallium arsenide (GaAs). Widely reported values are 2.23 eV for 3C-SiC, 2.93 eV for 6H-SiC, and 3.26 eV for 4H-SiC. Further, since SiC is thermally, chemically and mechanically stable and has excellent radiation resistance, it can be used not only for light emitting devices and high frequency devices, but also under severe conditions such as high temperature, high power, and radiation irradiation. As a power semiconductor device (power device) showing high reliability and stability, it is expected to be applied in various industrial fields.

[0003]

In particular, it has been reported that a high breakdown voltage MOSFET using SiC has a lower on-resistance than a power device using Si. Further, it has been reported that the forward drop

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voltage of the Schottky diode becomes low. As is well known, there is a trade-off relationship between the ON resistance of a power device and the switching speed. However, according to the power device using SiC, there is a possibility that low ON resistance and high switching speed can be achieved at the same time.

[0004]

In order to reduce the on-resistance of this power device using SiC, the reduction of the contact resistance ρ c with respect to the ohmic contact is an important factor. In particular, in order to reduce the on-resistance, a method of subdividing the main electrode region of the power device and arranging it on the SiC substrate with high density is also adopted. In order to reduce the ON resistance of such a finely sized power device, it is extremely important to obtain a low contact resistance ρ c inside the fine opening (contact window). Further, the contact resistance ρ c of the ohmic contact with respect to the p-type SiC region is also a big problem in order to increase the switching speed of power devices.

[0005]

In contrast to the fact that the SiC blue light emitting element has already been put to practical use and mass-produced, the application of SiC as a power device or a high frequency device has been far behind. One of the reasons for this is that the technology for forming a practical low resistance ohmic contact suitable for the structure and manufacturing process of these devices has not been established yet. For a SiC blue light-emitting element in which a current flows evenly over the ohmic contact surface formed on almost the entire surface of the SiC chip, the main current flows through the ohmic contact in the fine contact window close to the conduction channel. In a flowing semiconductor electronic device (semiconductor device), it is extremely important to reduce the contact resistance ρ c. That is, in a power device or a high frequency device in which a main current flows concentratedly in a local region where an ohmic contact is formed, an order of magnitude lower contact resistance ρ c is required to improve device characteristics. Because.

[0006]

Explaining with a specific example, a method described in Japanese Patent No. 2911122 is used as a prior art utilized as a method for forming a low resistance ohmic contact in a p-type SiC

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epitaxial layer of a SiC blue light emitting device. Yes (hereinafter, referred to as "first conventional technology"). " In this first conventional technique, a metal, such as a Ti thin film electrode, which reacts more strongly with oxygen than SiC, such as a Ti thin film electrode, is formed on a p-type SiC surface that has been surface treated by wet etching to a film thickness of about 50 nm, Then, after forming an Al-Ti-based electrode film on this, the laminated substrate is heat-treated at 800 to 1000 ° C, for example, 950 ° C for about 5 minutes to form a natural oxide film on the SiC surface. A uniform ohmic contact can be formed at any point on the substrate without interruption.

[0007]

However, in the first prior art, the ohmic property of the electrode layer was not perfect. For example, it is pointed out in Japanese Patent Laid-Open No. 161658/1995 that the line showing the current-voltage characteristic becomes a curve when the current-voltage characteristic between the electrode layers is strictly measured, and the ohmic property thereof is incomplete. Has been done. The ohmic contact having such a structure causes a large parasitic resistance when the current density becomes high, and is not suitable for use in a semiconductor electronic device such as a power device or a high frequency device.

[0008]

The prior art, which has been extensively studied for semiconductor electronic devices, is a method in which a metal film containing Al is heat-treated at a high temperature on the surface of a p-type SiC region to form an ohmic contact (hereinafter referred to as “second conventional method”). Technology.）である。 Among them, Crofton et al. (Applied Physics Letters, Vol. 62, p. 384 (1998)) describe a p-type SiC layer doped with high impurity density by epitaxial growth on the surface of a 6H-SiC substrate. It is reported that an ohmic contact of $\rho c = 1.5 \times 10^{-5}$ Ωcm 2 can be obtained by a method of depositing an Al-Ti alloy film on the above and then subjecting it to heat treatment. Crofton et al. Use the lift-off method for patterning the Al-Ti alloy film. The method of Crofton et al. Is roughly as follows. That is, (a) First, using the first photoresist formed by photolithography as a mask, the oxide film as the field insulating film is etched with a buffer hydrofluoric acid (BHF) solution to form an opening (contact window). To do. After etching the field insulating film, the first photoresist is removed.

[0009]

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(B) Then, a second photoresist is applied to the front surface including the contact window. Then, the second photoresist is patterned by photolithography to form an opening so as to expose the surface of the p-type SiC layer.

[0010]

(C) After that, after cleaning the surface of the p-type SiC layer, an Al-Ti alloy film having a thickness of 300 nm to 500 nm is formed on the entire surface by sputtering. Then, the second photoresist is dissolved with acetone to remove the unnecessary Al—Ti alloy film together with the second photoresist, and the Al—Ti alloy film is patterned.

[0011]

(D) At a heat treatment temperature of 1000 ° C., heat treatment is performed for 5 minutes in an argon atmosphere.

[0012]

[0012] However, the above-mentioned first prior art ohmic contact structure and manufacturing process are extremely difficult to form a p-type SiC ohmic contact on the surface of a flat SiC substrate. It has a simplified structure.

For this reason, there is a problem that it is not specific enough to be applied to the production of an actual device around which other structures such as a field insulating film and a gate electrode are placed. In the first place, the first prior art does not disclose any specific method for electrode patterning, so that it is difficult to apply it.

[0013]

Further, when the ohmic contact disclosed in the second prior art is applied to an actual semiconductor electronic device such as a transistor or a diode, it is difficult to say that the ρ c obtained by Crofton is sufficient. There is a demand for lower resistance. In the first place, the lift-off method proposed by Crofton tends to leave a photoresist in the opening of the field

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insulating film during development, which hinders reduction of resistance. Further, the residue of the photoresist and the like cause variations in the contact resistance ρ c.

[0014]
The present invention has been made to solve the problems of ohmic contacts to p-type SiC of the first and second prior arts at the same time, and it is 10-6 Ωcm 2 or less required for semiconductor electronic devices. It is to provide an ohmic electrode structure having the following contact resistance ρ c.

[0015]
Another object of the present invention is to provide a simple ohmic electrode structure capable of obtaining a low contact resistance ρ c inside a fine opening (contact window) which can be used in an actual device structure. Is to provide.

[0016]
Still another object of the present invention is to provide an ohmic electrode structure capable of obtaining a low contact resistance ρ c while maintaining the structure of a field insulating film applicable to various power devices which are required to have a high breakdown voltage. It is to be.

[0017]
Still another object of the present invention is to provide a method of manufacturing an ohmic electrode structure having a contact resistance ρ c of 10^{-6} Ωcm 2 or less, which is required for semiconductor electronic devices.

[0018]
Still another object of the present invention is to provide a method of manufacturing an ohmic electrode structure capable of easily obtaining a low contact resistance ρ c inside a fine opening which can be adopted in an actual device structure. Is.

[0019]
Still another object of the present invention is to provide a method for manufacturing an ohmic electrode structure capable of forming a field insulating film that can be used in various power devices that are required to have a high breakdown voltage and obtaining a low contact resistance ρ c. That is.

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[0020]
Still another object of the present invention is to provide a semiconductor device having a low contact resistance ρ c inside a fine opening and capable of operating at high speed and high frequency.

[0021]
Still another object of the present invention is to provide a semiconductor device which has a low on-voltage, can operate at high speed, and can increase the operating voltage.

[0022]
According to the results of the inventors' earnest study and consideration, the contact resistance ρ c in the ohmic contact between the Al--Ti based electrode film and the p-type SiC region is shown. The causes of increasing the temperature are 1) the existence of a Schottky barrier that is inevitably formed by the contact between the heated reaction layer and p-type SiC; 2) the formation of a non-uniform or inhomogeneous heated reaction layer in the plane; 3) the formation of the heated reaction layer At this time, it is a metal oxide formed on the surface of the Al-Ti based electrode film.

[0023]

The above-mentioned first conventional technique is not practical because the contact is formed on the surface of a flat SiC substrate, which is far from the actual device structure.

However, in an actual semiconductor electronic device, it is necessary to reduce the Schottky barrier inside the minute opening and generate a uniform and homogeneous heated reaction layer.

The present invention described below eliminates the three causes for increasing the contact resistance ρ c in the p-type SiC ohmic electrode structure provided in the opening of the field insulating film, which is applied to many actual device structures. It provides a means for

[0024]

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In order to solve the above-mentioned problems, the invention according to claim 1 provides: (a) a SiC substrate; and (b) a p-type SiC region selectively formed on the surface of the SiC substrate.) A heating reaction layer formed by penetrating inside from a part of the surface of the p-type SiC region and projecting upward from the surface of the p-type SiC region; and (d) a first through which the heating reaction layer penetrates. A thermal oxide film which has an opening of, and which is disposed in contact with the surface of the SiC substrate and the p-type SiC region; and (e) an insulating film having a composition or density different from that of the thermal oxide film. An upper insulating film having a second opening continuous to the opening and arranged on the surface of the thermal oxide film; and (f) a second opening of the upper insulating film, which is located above the heating reaction layer. The gist is that it is an ohmic electrode structure composed of an electrode film made of a metal containing at least one of Al and Ti arranged.

Although it is a matter related to a method of manufacturing an ohmic electrode structure described later, a clean metal / semiconductor bonding interface can be obtained by adopting such a structure of the ohmic electrode structure.

Therefore, the Schottky barrier in the metal / semiconductor junction is low, and the morphology of the interface is good.

[0025]

The "p-type SiC region selectively formed on the surface of the SiC substrate" defined in claim 1 is not limited to the case where the p-type SiC region is directly formed on the surface of the SiC substrate. Of course.

For example, another semiconductor region having a plane area larger than that of the p-type SiC region is arranged in a well shape on a part of the surface of the SiC substrate 1 , and the p-type SiC is formed at a position inside the well-shaped semiconductor region. A region may be formed.

Alternatively, a case where another semiconductor region is epitaxially grown on the entire surface of the SiC substrate and a p-type SiC region is formed on a part of the surface of the

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other epitaxially grown semiconductor region is allowed.

As described above, it should be noted that the invention according to claim 1 permits the case where the p-type SiC region is indirectly formed via another semiconductor region.

[0026]

According to a second aspect of the invention, in the ohmic electrode structure according to the first aspect, the electrode film is (i) a laminated film including a lower Ti--Si alloy film and an upper Ti film, ii) a laminated film composed of a lower Al—Si alloy film and an upper Al film, and (iii) a laminated film composed of a lower Al—Ti—Si alloy film and an upper Al—Ti alloy film. The gist is that it is a metal film including at least one of the laminated films.

As will be described later, the present invention relates to (i) an Al / Ti laminated film in which a Ti layer is deposited on an Al layer, (ii) a Ti / Al laminated film in which an Al layer is deposited on a Ti layer, (iii) By making the Al—Ti alloy film react with the p-type SiC region to form the heating reaction layer, the Schottky barrier can be made extremely low and the thickness of the barrier can be made thin.

In addition, the heated reaction layer is uniformly formed. The structure of the electrode film defined in claim 2 is a laminated structure including an unreacted metal layer after the formation of the heating reaction layer and a compound portion with metal Si diffused in the heating reaction layer. That is, (i) in the Al / Ti laminated film in which the Ti layer is deposited on the Al layer, the lower Al layer before the heat treatment is mainly the heat reaction layer by the heat treatment. At this time, a Ti—Si alloy film is formed below the upper Ti layer before the heat treatment by the reaction with the metal Si that has diffused in the heating reaction layer. The electrode film having the structure according to the second aspect is constituted by the laminated film including the generated Ti—Si alloy film and the unreacted Ti film on the upper portion.

[0027]

(Ii) In a Ti / Al laminated film in which an Al layer is deposited on a Ti layer, the Ti layer before the heat treatment mainly becomes a heat reaction layer by the heat treatment, and the upper Al layer before the heat treatment is The electrode film has a structure according to 2. In this case,

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an Al-Si alloy film is formed in the lower part of the electrode film by the reaction with the metal Si diffused in the heating reaction layer, and an unreacted Al film remains in the upper part.

[0028]

(Iii) In the Al-Ti alloy film, mainly the lower Al-Ti alloy film before the heat treatment becomes a heat reaction layer by the heat treatment, and the unreacted Al-Ti alloy film is present at the top before the heat treatment. Although remaining, an Al-Ti-Si alloy film is formed at the boundary with the heating reaction layer due to the reaction with metallic Si diffused in the heating reaction layer. The laminated structure composed of this Al-Ti-Si alloy film / unreacted Al-Ti alloy film constitutes the electrode film having the structure according to the second aspect.

[0029]

The invention according to claim 3 is characterized in that, in the ohmic electrode structure according to claim 1 or 2, the heating reaction layer is a solid solution containing metal carbide and metal silicon. The Al-Ti-based metal such as the Al / Ti laminated film, the Ti / Al laminated film, and the Al-Ti alloy film described above and SiC form alloys containing various silicides (carbides) or carbides (carbides). It is possible. However, according to many experimental results of the present inventors, among these, the heated reaction layer made of a solid solution containing metal carbide and metal silicon has a very low Schottky barrier at the metal / semiconductor junction, and It was found that the morphology of the interface was good and the heated reaction layer was uniformly formed.

[0030]
According to a fourth aspect of the present invention, in the ohmic electrode structure according to any one of the first to third aspects, the dielectric breakdown electric field strength of the upper insulating film is higher than that of the thermal oxide film. The point is that it is also low.

[0031]

According to a fifth aspect of the present invention, in the ohmic electrode structure according to any one of the first to fourth aspects, the etching rate of the upper insulating film with the BHF solution is higher than that of the thermal oxide film with the BHF solution. The point is that it is

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faster than speed.

As is well known, the "BHF solution" is an etching solution (etchant) for a silicon oxide film (SiO2 film) made of a solution of ammonium fluoride (NH4F): hydrofluoric acid (HF) = 7: 1.

[0032]
The invention according to claim 6 is the ohmic electrode structure according to any one of claims 1 to 5, wherein the surface carrier density of the p-type SiC region is 1 × 10 18 / cm 3 to 5 × 10 21 The summary is / cm3.

[0033]
The invention according to claim 7 is summarized in that, in the ohmic electrode structure according to any one of claims 1 to 6, the thickness of the thermal oxide film is 2 to 50 nm.

[0034]
The invention according to claim 8 is the ohmic electrode structure according to any one of claims 1 to 7, wherein the sum of the thickness of the thermal oxide film and the thickness of the upper insulating film is 100 nm. The gist is that it is 3 μm.

[0035]
According to a ninth aspect of the present invention, in the ohmic electrode structure according to any one of the first to eighth aspects, the uppermost position of the electrode film exists inside the second opening. That is the summary.

[0036]
The invention according to claim 10 is: (a) a step of forming a p-type SiC region having a high impurity density on at least a part of the surface of the SiC substrate; and (b) a step of cleaning the surface of the SiC substrate. (C) a step of covering the surface of the SiC substrate with a field insulating film, and (d) a step of forming an opening in the field insulating film so as to expose at least a part of the p-type SiC region,) A step of disposing an Al-Ti-based electrode film inside the opening, and (f) SiC in a non-oxidizing atmosphere with a partial pressure of oxygen and water of 1 × 10 −3 Pa to 1 × 10 −10 Pa. It is a gist of the present invention to provide a method for manufacturing an ohmic electrode structure, which includes a step of heat-treating a substrate to generate a heated reaction layer of an Al-Ti based electrode film and a SiC substrate.

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[0037]

As in the case of claim 1, the “step of forming a p-type SiC region having a high impurity density on at least a part of the surface of the SiC substrate” defined in claim 10 is performed on the surface of the SiC substrate. Of course, it is not limited to the case of directly forming the p-type SiC region.

For example, another semiconductor region having a plane area larger than that of the p-type SiC region is arranged in a well shape on a part of the surface of the SiC substrate 1, and the p-type SiC is formed at a position inside the well-shaped semiconductor region. A region may be formed.

Alternatively, a case where another semiconductor region is epitaxially grown on the entire surface of the SiC substrate and a p-type SiC region is formed on a part of the surface of the other epitaxially grown semiconductor region is allowed.

Thus, it should be noted that the invention according to claim 10 allows the p-type SiC region to be indirectly formed through another semiconductor region.

[0038]

According to the eleventh aspect of the invention, in the method of manufacturing the ohmic electrode structure according to the tenth aspect, the step of covering with the field insulating film grows a thermal oxide film on the surface of the SiC substrate by thermal oxidation. The gist of the invention is that it comprises a step and a step of depositing an insulating film on the thermal oxide film by a method other than thermal oxidation.

[0039]

According to a twelfth aspect of the present invention, in the method of manufacturing an ohmic electrode structure according to the tenth aspect, the step of covering with the field insulating film is a method other than thermal oxidation, and oxygen permeation is performed on the surface of the SiC substrate. A step of depositing a conductive insulating film and a step of growing a thermal oxide film on the interface between the surface of the SiC substrate and the

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oxygen permeable insulating film by thermal oxidation after the deposition of the oxygen permeable insulating film. Use as a summary.

That is, oxygen in the atmosphere reaches the surface of the SiC substrate via the oxygen permeable insulating film, and a SiO2 film is formed at the interface between the surface of the SiC substrate and the oxygen permeable insulating film to realize a field insulating film. You can

[0040]
The invention according to claim 13 is: (a) a step of forming a p-type SiC region having a high impurity density on at least a part of the surface of the SiC substrate; and (b) a step of cleaning the surface of the SiC substrate. And (c) a step of depositing an oxygen permeable insulating film on the surface of the SiC substrate by a method other than thermal oxidation, and (d) oxygen permeability so that a part of the p-type SiC region is selectively exposed. After the step of forming the opening in the insulating film and (e) the step of forming the opening, the surface of the SiC substrate exposed in the opening by thermal oxidation, and the surface of the SiC substrate and the oxygen-permeable insulating film. A step of growing a thermal oxide film on the interface of (4), a step of (f) removing the thermal oxide film grown in the opening, and (g) an Al-Ti system inside the opening from which the thermal oxide film has been removed. An ohmic electrode structure including: a step of disposing an electrode film; and (h) a step of heat-treating a SiC substrate in a non-oxidizing atmosphere to generate a heated reaction layer of the Al—Ti based electrode film and the SiC substrate. The gist is that it is a manufacturing method.

[0041]
According to a fourteenth aspect of the present invention, in the method of manufacturing an ohmic electrode structure according to the thirteenth aspect, in the step of forming the heating reaction layer, the partial pressures of oxygen and water are both 1×10^{-3} Pa The gist is that it is carried out in an atmosphere of 1×10^{-10} Pa.

[0042]
According to a fifteenth aspect of the present invention, in the method of manufacturing an ohmic electrode structure according to any one of the tenth to fourteenth aspects, the step of disposing the Al--Ti based electrode film includes (i) At least one step from the group consisting of depositing a Ti layer on the Al layer, (ii) depositing an Al layer on the Ti layer, and (iii) depositing an Al-Ti alloy film The main point is to include.

[0043]

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According to a sixteenth aspect of the present invention, in the method of manufacturing an ohmic electrode structure according to any one of the tenth to twelfth aspects, the step of forming the opening is performed by (a) photolithography method. A step of forming an etching mask on the insulating film, and (b) using the etching mask, a part of the field insulating film is formed so that the field insulating film remains on at least a part of the p-type SiC region. A step of removing by dry etching, (c) a step of removing remaining field insulating film by wet etching to expose at least a part of the p-type SiC region, and (d) exposure by rinsing with ultrapure water The gist is that it comprises a step of cleaning the p-type SiC region.

[0044]
According to a seventeenth aspect of the present invention, in the method of manufacturing an ohmic electrode structure according to the sixteenth aspect, in the step of disposing the Al--Ti based electrode film, the etching mask is provided on the field insulating film. In the remaining state, a step of depositing the Al—Ti based electrode film on the entire surface including the upper portion and the opening of the etching mask, and after the step of depositing on the entire surface, the etching mask is removed to remove the Al—Ti based electrode film. The gist is that it comprises a step of selectively leaving the film only inside the opening.

[0045]
According to an eighteenth aspect of the present invention, in the method of manufacturing an ohmic electrode structure according to the thirteenth or fourteenth aspect, the step of forming the opening includes (a) a photolithography method for forming an oxygen permeable insulating film. A step of forming an etching mask on the upper part, and (b) using this etching mask, a part of the oxygen permeable insulating film is formed so that the oxygen permeable insulating film remains on at least a part of the p-type SiC region. And (c) removing the residual oxygen-permeable insulating film by wet etching to expose at least a part of the p-type SiC region, and (d) exposing with a rinse with ultrapure water. The gist is that it comprises a step of cleaning the p-type SiC region.

[0046]
The invention according to claim 19 is: (a) a SiC substrate; (b) a p-type SiC region which functions as a main electrode region selectively formed on the surface of the SiC substrate; A heating reaction layer formed to penetrate inside from a part of the surface of the p-type SiC region and project upward from the surface of the p-type SiC region, and (d) a first opening through which the heating reaction layer penetrates. A thermal oxide film having a portion and being in contact with the surface of the SiC substrate and the p-type SiC region, and (e) an insulating film having a composition or density different from that of the thermal oxide film. An upper insulating film having a continuous second opening on the surface of the thermal oxide film, and (f) a second

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opening of the upper insulating film, which is arranged on the heating reaction layer. Another feature of the present invention is that the semiconductor device includes an electrode film made of a metal containing at least one of Al and Ti, and (g) a main electrode wiring connected to the electrode film.

[0047]

Here, the "p-type SiC region functioning as a main electrode region selectively formed on the surface of the SiC substrate" means only when the p-type SiC region is directly formed on the surface of the SiC substrate. Of course, it is not limited.

For example, another semiconductor region having an area larger than that of the main electrode region (p-type SiC region) is arranged in a well shape on a part of the surface of the SiC substrate 1, and the main semiconductor is formed at a position inside the well-shaped semiconductor region. An electrode region (p-type SiC region) may be formed.

For example, it may be a base region of a bipolar transistor or a main electrode region (p-type SiC region) formed in a body region such as a power MOSFET.

Alternatively, the case where another semiconductor region is epitaxially grown on the entire surface of the SiC substrate and the main electrode region (p-type SiC region) is formed on a part of the surface of the other epitaxially grown semiconductor region is also allowed. .

As described above, the invention according to claim 19 allows the case where the main electrode region (p-type SiC region) is indirectly formed on the surface of the SiC substrate through the other semiconductor region. It should be noted.

[0048]
According to a twentieth aspect of the invention, in the semiconductor device according to the nineteenth aspect, the electrode film is a laminated film including a lower titanium-silicon (Ti-Si) alloy film and an upper titanium (Ti) film. A laminated film including a lower aluminum-silicon (Al-Si) alloy film and an upper aluminum (Al) film, and a lower aluminum-titanium-silicon (Al-Ti-Si) alloy film and an upper aluminum-titanium film The gist is that it is a metal film including at least one laminated film in the group consisting of laminated films composed of an (Al—Ti) alloy

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film.

[0049]
The invention according to claim 21 is the semiconductor device according to claim 19 or 20, wherein the heating reaction layer is a solid solution containing a metal carbide and metal silicon (Si).

[0050]

According to the invention of claim 1, a thermal oxide film formed by thermally oxidizing the surface of a SiC substrate and an insulating film having a different composition or density from the thermal oxide film are laminated. Due to the structure, a relatively thick field insulating film can be formed.

Therefore, in various power devices that are required to have a high breakdown voltage, a contact resistance ρ c of 10^{-6} Ωcm 2 or lower, which is about one digit lower than the conventionally known contact resistance ρ c, is realized, and the surface wiring is p-type SiC. It is possible to increase the frequency and performance of various semiconductor electronic devices connected to the area.

In particular, a low contact resistance ρ c can be obtained inside a fine opening (contact window) that can be used in an actual device structure.

[0051]

By using the material defined in claim 2 as the metal film, a metal / semiconductor junction having a low Schottky barrier and a thin barrier can be formed.

In addition, the heated reaction layer is uniformly formed.

Therefore, according to the invention of claim 2, an ohmic electrode structure having an extremely low contact resistance ρ c with respect to the p-type SiC region can be obtained.

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[0052]

According to the third aspect of the invention, since the heating reaction layer made of a solid solution containing metal carbide and metal silicon is selected, the Schottky barrier at the metal / semiconductor junction is extremely low, and The interface morphology is good and the heated reaction layer can be formed uniformly.

Therefore, an ohmic electrode structure having an extremely low contact resistance ρ c with respect to the p-type SiC region can be obtained.

[0053]

The thermal oxide film of SiC is a silicon oxide film (SiO2 film) which is inferior to the Si thermal oxide film but is close to the Si thermal oxide film.

Therefore, the dielectric breakdown field strength of the thermal oxide film of SiC is about 14 MV / cm at a thickness of 10 nm.

The dielectric breakdown field strength of the SiO2 film formed by a method other than thermal oxidation is smaller than this value. That is, according to the invention of claim 4, various insulating films other than the thermal oxide film of SiC are formed on the thermal oxide film of SiC to secure the breakdown voltage required for the specifications of the semiconductor device. At the same time, the surface morphology of SiC can be favorably maintained.

[0054]

As described above, since the SiC thermal oxide film is a SiO2 film close to the Si thermal oxide film, the etching rate for the BHF solution is about 100 nm / min. On the other hand, the etching rate for the SiO2 film deposited by CVD is 11.5 to 3 times higher. That is, according to the invention described in claim 5, various SiO2 films other than the thermal oxide film of SiC are formed on the thermal oxide film of SiC, and the withstand voltage and surface The surface

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morphology of SiC can be favorably maintained while ensuring stability. Further, various semiconductor processes can be adopted by utilizing the difference in etching rate with respect to the BHF solution.

[0055]

According to the sixth aspect of the invention, the surface carrier density of the p-type SiC region is a high impurity density of 1 × 10 18 / cm 3 to 5 × 10 21 / cm 3, so that the p-type SiC region and the heating reaction The thickness of the Schottky barrier generated between the layer and the layer becomes thin, and conduction holes easily flow due to the tunnel effect. Therefore, a low contact resistance ρ c is obtained.

[0056]

According to the invention of claim 7, since the thickness of the thermal oxide film is optimized to a value of 2 to 50 nm, a hydrocarbon compound and a natural oxide film which are easily formed on the surface of the p-type SiC region are possible. It is possible to prevent roughening of the substrate due to excessive thermal oxidation while maintaining the removal effect as much as possible. Therefore, the interface between the p-type SiC region and the heating reaction layer is flat. Moreover, since the heated reaction layer is uniform and homogeneous, the height of the Schottky barrier is reduced, and the contact resistance ρ c is reduced.

[0057]
According to the invention of claim 8, the total value of the thickness of the thermal oxide film and the thickness of the upper insulating film is 100 nm to 3 μ m. Therefore, the SiC substrate below the thermal oxide film and the upper insulating film are formed. It is possible to provide a power semiconductor device having a high withstand voltage, in which a leak current due to a parasitic MOS transistor formed with the wiring above is suppressed.

[0058]

According to the invention of claim 9, the uppermost position of the electrode film exists inside the second opening, and the upper insulating film around the second opening does not overlap. .

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Therefore, when forming the heating reaction layer, even if Al is melted, Al is confined in the depression of the second opening, so that the molten Al flows out to the surface of the surrounding upper insulating film, which may cause a wiring short circuit. There is no. As a result, the manufacturing yield is improved.

[0059]

According to the tenth aspect of the invention, the steps from immediately before forming the field insulating film to arranging the Al--Ti based electrode film inside the opening are performed on the exposed SiC surface of the opening. It can proceed without applying photoresist once. Therefore, it is possible to completely avoid the adhesion of hydrocarbons due to the photoresist to the interface between the Al—Ti based electrode film and SiC before forming the heated reaction layer, and a clean interface can be easily obtained. Therefore, the Schottky barrier at the interface between the heated reaction layer and SiC is extremely low and thin. Moreover, the morphology of the interface is good, and the heated reaction layer is uniformly formed. Furthermore, since a heat reaction layer is formed by heat treatment in a non-oxidizing atmosphere in which the partial pressures of oxygen and water are both 1×10^{-3} Pa to 1×10^{-10} Pa, the Al—Ti based electrode film is formed during the heat treatment. The metal oxide film such as aluminum oxide (Al2O3) or titanium oxide (TiO2) formed on the surface of the is significantly suppressed, and the increase in contact resistance ρ c due to the metal oxide film on the surface can be greatly reduced. As a result, a contact resistance ρ c of 10^{-6} Ωcm 2 or lower, which is lower than the conventional contact resistance ρ c by about one digit, can be obtained. Moreover, since this ohmic electrode structure is provided in the opening in the field insulating film, it is a structure suitable for an actual semiconductor electronic device.

[0060]

According to the invention described in claim 11, the step of forming the field insulating film on the surface of the SiC substrate is performed by a step of growing a thermal oxide film and a method other than thermal oxidation on the thermal oxide film. Since it is composed of the step of depositing the insulating film, it is possible to suppress deterioration of the surface morphology of the SiC substrate due to excessive thermal oxidation. In addition to the thermal oxidation, well-known physical or chemical means such as a CVD method or a sputtering method can be adopted. However, a natural oxide film or hydrocarbons unique to these methods other than the thermal oxidation can be used. The generation can be effectively removed or suppressed by the thermal oxide film. Therefore, the morphology of the interface between the heating

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reaction layer and the p-type SiC region becomes good, and a uniform and homogeneous heating reaction layer can be generated. Therefore, it is possible to easily obtain the above-mentioned contact resistance ρ c of 10^{-6} Ωcm 2 or less.

[0061]

According to the twelfth aspect of the present invention, the step of depositing the oxygen permeable insulating film on the surface of the SiC substrate by a method other than thermal oxidation is performed first, and after the oxygen permeable insulating film is deposited, thermal treatment is performed. A thermal oxide film is grown on the interface between the surface of the SiC substrate and the oxygen permeable insulating film by oxidation to form a field insulating film. Also in this case, similarly to the invention according to claim 11, deterioration of the surface morphology of the SiC substrate due to excessive thermal oxidation can be suppressed. Further, the formation of a natural oxide film or hydro carbon unique to well-known physical or chemical means such as a CVD method or a sputtering method can be effectively removed or suppressed by the formation of a thermal oxide film. Therefore, the morphology of the interface between the heated reaction layer and the p-type SiC region becomes good, and a uniform and homogeneous heated reaction layer can be generated. Therefore, a low contact resistance ρ c of 10^{-6} Ωcm 2 or less can be easily obtained.

[0062]

In the invention according to claim 13, first, a "temporary field insulating film" made of an oxygen permeable insulating film is formed on the surface of the SiC substrate by a method other than thermal oxidation, and this temporary field insulating film is formed. Since an opening (so-called contact window) is formed, a thermal oxide film is grown on the surface of the SiC substrate exposed in this opening, and then this thermal oxide film is removed, the surface of the p-type SiC region is removed. Can be cleaned. Further, similarly to the inventions according to claims 11 and 12, the steps from immediately before forming the provisional field insulating film to arranging the Al-Ti based electrode film inside the opening are performed by exposing the SiC of the opening. It can proceed without applying photoresist to the surface even once. Therefore, it is possible to completely avoid the adhesion of hydrocarbons due to the photoresist to the interface between the Al—Ti based electrode film and SiC before forming the heated reaction layer, and a clean interface can be easily obtained. Therefore, the Schottky barrier at the interface between the heated reaction layer and SiC is extremely low and thin. Furthermore, since a thin thermal oxide film is formed at the interface between the surface of the SiC substrate and the oxygen-permeable insulating film by the subsequent thermal oxidation, a high breakdown

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voltage is achieved as in the invention according to claims 11 and 12. At the same time, the deterioration of the surface morphology of the SiC substrate due to excessive thermal oxidation can be suppressed. Further, the formation of a natural oxide film or hydrocarbons, which is inherent in physical or chemical means other than thermal oxidation, can be effectively removed by the formation of a thermal oxide film. Therefore, the morphology of the interface between the heating reaction layer and the p-type SiC region becomes good, and a uniform and homogeneous heating reaction layer can be generated. Therefore, a low contact resistance ρ c of 10^{-6} Ωcm 2 or less can be easily obtained.

[0063]
According to the fourteenth aspect of the invention, heat treatment is performed in a non-oxidizing atmosphere in which the partial pressures of oxygen and water are both 1×10^{-3} Pa to 1×10^{-10} Pa to form a heated reaction layer. Therefore, the metal oxide film such as Al2O3 or TiO2 generated on the surface of the Al-Ti-based electrode film during the heat treatment is remarkably suppressed, and the increase of the contact resistance ρ c due to the metal oxide film on the surface can be greatly reduced.

[0064]

(I) An Al / Ti laminated film having a Ti layer deposited on an Al layer, (ii) a Ti / Al laminated film having an Al layer deposited on a Ti layer, and (iii)) Each of the Al-Ti alloy films can form a heated reaction layer having a good morphology at the interface with the p-type SiC region and an extremely low Schottky barrier by the reaction with the p-type SiC region.

Therefore, according to the invention of claim 15, a contact resistance ρ c of 10^{-6} Ωcm 2 or less, which is lower than the conventional contact resistance ρ c by about one digit, can be obtained.

[0065]

According to the sixteenth aspect of the present invention, since the final step of the opening reaching the p-type SiC region is completed by wet etching and rinsing with ultrapure water, a reaction product of dry etching is obtained. It is possible to prevent re-adhesion of the hydro carbon to the surface of the p-type SiC substrate and etching damage due to excessive plasma energy. Therefore, it is possible to effectively prevent contamination of the surface of the p-type

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SiC substrate and roughening of the substrate surface. In addition, since dry etching can be used, a fine ohmic contact can be formed, so that high integration density of a semiconductor integrated circuit and high performance such as reduction of on-resistance of a power semiconductor device are possible.

[0066]

According to the seventeenth aspect of the present invention, the etching mask using the opening (contact window) as the opening can also be used as the mask for the lift-off process for patterning the Al—Ti based electrode film. That is, the contact window opening step and the photolithography step for patterning the Al—Ti based electrode film can be performed at one time, and the manufacturing process of the semiconductor device is simplified. Therefore, it is easy to improve the manufacturing yield of semiconductor devices, improve the productivity, and further reduce the manufacturing cost.

[0067]

According to the eighteenth aspect of the present invention, the final step of forming the opening reaching the p-type SiC region in the oxygen-permeable insulating film is completed by wet etching and rinsing with ultrapure water. It is possible to prevent re-adhesion of hydro carbon, which is a reaction product of dry etching, to the surface of the p-type SiC substrate and etching damage due to excessive plasma energy. Therefore, similarly to the invention according to claim 16, contamination of the surface of the p-type SiC substrate and roughening of the substrate surface can be effectively prevented. In addition, since dry etching can be used, fine ohmic contacts can be formed, and high performance such as high integration density of semiconductor integrated circuits and reduction of on-resistance of power semiconductor devices can be achieved.

[0068]

According to the nineteenth aspect of the present invention, the stability is provided by the laminated structure of the thermal oxide film formed by thermally oxidizing the surface of the SiC substrate and the insulating film having a different composition or density from the thermal oxide film. It is possible to form a relatively thick field insulating film excellent in heat resistance. Therefore, in various power devices having a high rated operating voltage, a contact resistance

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ρc that is about one digit lower than the conventionally known contact resistance ρc is realized. Therefore, it is possible to increase the frequency and performance of the semiconductor electronic device. In particular, a low contact resistance ρc with respect to the main electrode region can be obtained inside the fine opening (contact window) that can be adopted in the actual device structure. Therefore, by arranging a large number of fine contact windows at high density, a semiconductor power device capable of low on-voltage and high-speed operation can be realized.

[0069]

By using the material defined in claim 20 as the metal film, a metal / semiconductor junction having a low Schottky barrier and a thin barrier can be formed. In addition, the heated reaction layer is uniformly formed. Therefore, according to the invention of claim 20, the contact resistance ρc with respect to the main electrode region formed of the p-type SiC region becomes extremely low, and it becomes possible to increase the frequency and performance of various semiconductor electronic devices.

[0070]

According to the twenty-first aspect of the invention, since the heating reaction layer made of the solid solution containing the metal carbide and the metal silicon is selected, the Schottky barrier at the metal / semiconductor junction becomes extremely low. Moreover, the morphology of the interface is good, and the heated reaction layer can be formed uniformly. Therefore, the contact resistance ρc with respect to the main electrode region becomes extremely low, and it becomes possible to increase the frequency and performance of various semiconductor electronic devices.

[0071]

Next, first to third embodiments of the present invention will be described with reference to the drawings. In the following description of the drawings, the same or similar reference numerals are given to the same or similar parts. However, it should be noted that the drawings are schematic and the relationship between the thickness and the plane dimension, the thickness ratio of each layer, and the like are different from the actual ones. Therefore, specific thicknesses and dimensions should be determined in consideration of the following description. Further, it is needless to say that the drawings include portions having different dimensional relationships and

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ratios.

[0072]

(First Embodiment) As shown in FIG. 1, an ohmic electrode structure according to a first embodiment of the present invention is selectively formed on the surfaces of a SiC substrate 1 and a SiC substrate 1. P-type SiC region 2, heat reaction layer 8 formed on a part of the surface of p-type SiC region 2, thermal oxide film 3 covering the interface between SiC substrate 1 and p-type SiC region 2, thermal oxide film 3 At least the upper insulating film 4 arranged on the surface of the electrode and the electrode film 7 arranged on the heating reaction layer 8. The p-type SiC region 2 functions as a main electrode region of a semiconductor device, especially a semiconductor electronic device.

[0073]

Generally, a semiconductor electronic device has a first main electrode region, a second main electrode region and a control electrode. The "first main electrode region" means either the emitter region or the collector region in the IGBT, and the source region or the drain region in the power insulated gate transistor (power IGT) such as the power MOSFET or the power MOSSIT. Means one side. The "second main electrode region" means either an emitter region or a collector region that does not become the first main electrode region in the IGBT, and a source region or a drain region that does not become the first main electrode region in the power IGT. Means either one of That is, if the first main electrode region is the emitter region, the second main electrode region is the collector region, and if the first main electrode region is the source region, the second main electrode region is the drain region. Further, it goes without saying that the “control electrode” means the gate electrodes of the IGBT and the power IGT. In the present invention, either one of the first main electrode region and the second main electrode region is simply referred to as "main electrode region". Also, in a SiC semiconductor device that does not have a control electrode such as a diode, the first main electrode region and the second main electrode region are similarly defined. In the present invention, also in this case, either one of the first main electrode region and the second main electrode region is simply referred to as “main electrode region”. Furthermore, in a semiconductor integrated circuit such as a power IC, three or more main electrode regions can be defined, but at least one of the plurality is the "main electrode region" of the present invention.

[0074]

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The field insulating film 5 is composed of a laminated structure of the thermal oxide film 3 and the upper insulating film 4. Further, a wiring conductor piece 9 is formed on the field insulating film 5 so as to be electrically connected to the electrode film 7. The wiring conductor piece 9 is a wiring member that connects the ohmic contact shown in FIG. 1 to another portion, and functions as a main electrode wiring of the semiconductor device. In the power device, a plurality of unit cells are arranged on the SiC substrate 1 in a honeycomb shape, a matrix shape or the like to secure a current capacity. In addition, each main electrode region may be subdivided and arranged on the SiC substrate 1 at a high density depending on the design specifications for lowering the ON voltage. Therefore, in such a case, the wiring conductor piece 9 functions as a wiring that integrates the respective main electrode regions of the unit cells divided into a plurality. The wiring conductor piece 9 includes well-known aluminum (Al), aluminum-silicon (Al-Si) eutectic, aluminum-copper-silicon (Al-Cu-Si) eutectic, copper (Cu), titanium-tungsten. A (Ti-W) alloy or the like is used.

[0075]

The conductivity type and the impurity density of the SiC substrate 1 differ depending on the semiconductor device using the ohmic electrode structure of the present invention. Further, another semiconductor region having a plane area larger than that of the p-type SiC region 2 is arranged in a well shape on a part of the surface of the SiC substrate 1, and the inside of the well shape of the other semiconductor area on the plane is arranged. At the position, the epitaxially grown p-type SiC region 2 of high impurity density may be formed as a convex portion, and this p-type SiC region 2 may be used as the main electrode region. Alternatively, another semiconductor region is epitaxially grown on the entire surface of the SiC substrate 1, and a part of the surface of the other epitaxially grown semiconductor region is further subjected to continuous epitaxial growth by high-impurity-density p-type SiC region 2 by mesa etching or the like. You may form as a convex part and use this p-type SiC area ¦ region 2 as a main electrode area ¦ region.

[0076]

For example, in the case of a pnp-type bipolar transistor, a base region made of an n-type SiC region is formed in a well shape on the surface of a low-impurity-density p-type (or π -type) SiC substrate 1 serving as a collector region. A p-type SiC region 2 having a high impurity density as a main electrode region (emitter region) may be formed as a convex portion at a position inside

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the plane of the base region. In this case, an intrinsic semiconductor (i-type) SiC substrate 1 is used in place of the low-impurity-density p-type SiC substrate 1 serving as the collector region, and the rear surface (or part of the front surface) of the i-type SiC substrate 1 is filled with high impurities You may form the collector region which consists of a p-type SiC region of high density.

[0077]

In the case of a thyristor such as a GTO thyristor, an n base region made of an n type SiC region is formed on a part or the whole surface of the p type SiC substrate 1 which becomes a p base region, and the inside of this n base region is formed. In addition, it is possible to form the p-type SiC region 2 having a high impurity density as an anode region (main electrode region) into a convex shape by epitaxial growth. In this case, an n-type SiC region as a cathode region is formed on the back surface of the p-type SiC substrate 1 that serves as the p base region.

[0078]

On the other hand, in the n-channel junction type FET or junction type SIT, the source region (main electrode region) is formed on the surface of the n-type SiC substrate (or ν -type SiC substrate or i-type SiC substrate) 1 functioning as the channel region. It is possible to form the p-type SiC region 2 having a high impurity density as a convex shape. Further, in an n-channel SI thyristor, a high impurity density p-type SiC region 2 as an anode region is projected on the surface of an n-type SiC substrate (or ν -type SiC substrate or i-type SiC substrate) 1 functioning as a channel region. It can be formed in a partial shape.

[0079]

In the p-channel power IGT, on the surface of the n-type SiC substrate (or π -type SiC substrate) 1 functioning as an n-type channel region, a p-type SiC region having a high impurity density as a drain region (main electrode region) is formed. 2 can be formed in a convex shape. In this case, a p-type SiC region having a high impurity density as a source region (other main electrode region) is formed on another surface of the n-type SiC substrate (or π -type SiC substrate) 1 so as to face the drain region 2. Are formed in a convex shape. Then, a gate oxide film is formed on the surface of the n-type SiC substrate (or π -type SiC substrate) 1 between the source region and the drain region 2, and a gate electrode is formed on the gate oxide film. As the gate electrode, a

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refractory metal such as tungsten (W), titanium (Ti), or molybdenum (Mo), a silicide (WSi2, TiSi2, MoSi2) thereof, or the like can be used. Alternatively, in a p-channel power IGT having a double diffusion structure, a high drain region (main electrode region) is formed on the surface of the p-type SiC substrate (or π -type SiC substrate or i-type SiC substrate) 1 that functions as a drift region. It is possible to form the p-type SiC region 2 having an impurity density in a convex shape. In this case, another p-type SiC region as a source region is formed in the n-body region formed on the surface of p-type SiC substrate 1. Similarly, a p-type SiC region 2 as a drain region and a p-type SiC region as a source region are formed in a convex shape on the surface of an n-type SiC substrate (or a π -type SiC substrate) 1, and the source region and the drain are formed. A MESFET can be realized by forming a Schottky electrode on the surface of the n-type SiC substrate (or π -type SiC substrate) 1 between the regions 2.

[0080]

In an n-channel IGBT, a high impurity density p-type SiC region 2 as a collector region can be formed in a convex shape on the surface of an n-type SiC substrate (or ν -type SiC substrate) 1 functioning as a drift region. Is. In this case, another n-type SiC region as the emitter region is formed in the p-body region formed on the surface of the n-type (or ν -type) SiC substrate 1. The ohmic electrode structure according to the first embodiment of the present invention can be applied to the high impurity density p-type SiC region 2 as the main electrode region of these various semiconductor electronic devices. The heating reaction layer 8 is formed so as to enter the inside from a part of the surface of the p-type SiC region 2 and at the same time project upward from the surface of the p-type SiC region 2. Thermal oxide film 3 has a first opening through which heated reaction layer 8 penetrates, and covers SiC substrate 1 and p-type SiC region 2 so as to cover the interface between SiC substrate 1 and p-type SiC region 2. It is placed in contact with the surface. The upper insulating film 4 is an insulating film having a composition or density different from that of the thermal oxide film 3, and has a second opening continuous with the first opening. As shown in FIG. 1, the uppermost position of the electrode film 7 exists inside the second opening. The first and second openings form a common opening 6.

[0081]

In the ohmic electrode structure according to the first embodiment of the present invention, "insulating film having a composition different from that of the thermal oxide film 3" means PSG (phosphosilicate glass) film, BSG (borosilicate glass). , BPSG (borophosphosilicate glass) or Si3N4 film. The "insulating film having a density different from that of the thermal oxide film 3" means an insulating film such as a SiO2 film deposited by a method other than the thermal oxide film.

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For example, a SiO2 film formed by a chemical or physical deposition method such as a CVD method, a sputtering method, or a vacuum deposition method is applicable. The SiC thermal oxide film 3 shown in FIG. 1 is a SiO2 film that is inferior to the Si thermal oxide film but is close to the Si thermal oxide film. Since the thermal oxide film and the SiO2 film deposited by another method have different densities, the boundaries can be seen by observing the cross section with high resolution SEM.

[0082]

The dielectric breakdown field strength of the SiC thermal oxide film 3 close to the Si thermal oxide film is about 14 MV / cm at a thickness of 10 nm. On the other hand, the dielectric breakdown field strength of the SiO2 film formed by a method other than thermal oxidation is smaller than this value. For example, the insulation breakdown electric field strength of the SiO2 film deposited by CVD is about 6 MV / cm at the same thickness of 10 nm. Therefore, if the insulation breakdown electric field strength is measured, the thermal oxide film 3 of SiC and the upper insulation film 4 can be clearly seen. Can be distinguished from.

[0083]

Further, since the SiC thermal oxide film 3 is a SiO2 film close to the Si thermal oxide film, the etching rate for the BHF solution is about 100 nm / min. In comparison, the etching rate for the SiO2 film deposited by CVD is 1.5 to 3 times higher. Therefore, the thermal oxide film 3 of SiC and the upper insulating film 4 can be clearly distinguished by measuring the etching rate for the BHF solution.

[0084]

Microscopically, since there are more hydrogen and carbon bonds in the SiO2 film deposited by CVD than the SiC thermal oxide film 3 and the Si--O--Si bond distance is longer than that of the SiC thermal oxide film 3, infrared rays are used. The thermal oxide film 3 of SiC and the upper insulating film 4 can be clearly distinguished by the absorption spectrum and Raman spectroscopy.

[0085]

If a laminated structure in which an upper insulating film 4 such as various SiO 2 films other than the thermal oxide film of SiC as shown in FIG. 1 is formed on the thermal oxide film 3 of SiC

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is adopted, the specifications of the semiconductor device can be improved. The surface morphology of SiC can be favorably maintained while ensuring the pressure resistance and surface stability required as.

[0086]

The thickness of the thermal oxide film 3 is preferably 2 to 50 nm.

Particularly, the thickness of the thermal oxide film 3 in the range of 5 to 20 nm is desirable.

If the thickness of the thermal oxide film 3 is thinner than 5 nm, the effect of removing the damaged region on the surface of the SiC substrate 1 caused by the surface polishing or the ion implantation method and the effect of removing the foreign matter on the surface become poor. On the other hand, when the thickness of the thermal oxide film 3 is thicker than 50 nm, there is a problem that the surface of the SiC substrate 1 is gradually roughened due to excessive thermal oxidation and the surface morphology is deteriorated. Therefore, in order to reduce the contact resistance ρc, the thickness of the thermal oxide film 3 within the above range brings a beneficial effect.

[0087]

The total thickness of the field insulating film 5, which is the sum of the thickness of the thermal oxide film 3 and the thickness of the upper insulating film 4, is preferably 100 nm to 3 μm. Particularly, it is desirable that the thickness is 300 nm or more. Further, if it is a high breakdown voltage power semiconductor device, it may be set to 800 nm or more. However, if the field insulating film 5 becomes too thick, cracks and the like will occur, so 3 μm or more is not preferable.

[0088]

The electrode film 7 shown in FIG. 1 is made of a metal containing at least one of Al and Ti, which is disposed above the heating reaction layer 8 in the second opening of the upper insulating film 4. The "electrode film 7 made of a metal containing at least one of Al and Ti" is

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(i) a laminated film composed of a lower Ti—Si alloy film and an upper Ti film, and (ii) a lower Al—Si alloy film. It is preferable that it is either a laminated film made of Al and an upper Al film, or (iii) a laminated film made of a lower Al—Ti—Si alloy film and an upper Al—Ti alloy film.

[0089]

As will be described later, according to the present invention, (i) an Al / Ti laminated film in which a Ti layer is deposited on an Al layer, (ii) a Ti / Al laminated film in which an Al layer is deposited on a Ti layer, (Iii) The Al—Ti alloy film is caused to react with the p-type SiC region 2 to form the heating reaction layer 8, whereby the Schottky barrier is extremely low and the barrier thickness is thin. Due to this, the electrode film 7 shown in FIG. 1 has a laminated structure composed of the unreacted metal layer after the formation of the heating reaction layer 8 and the compound portion with the metal Si diffused in the heating reaction layer 8. Is. That is, (i) in the Al / Ti laminated film in which the Ti layer is deposited on the Al layer, the lower Al layer before the heat treatment becomes the heating reaction layer 8 by the heat treatment. At this time, in the upper Ti layer before the heat treatment, a Ti—Si alloy film is formed in the lower portion by the reaction with the metallic Si that has diffused in the heating reaction layer. The electrode film 7 is composed of a laminated film including the lower Ti—Si alloy film and the upper unreacted Ti film.

[0090]

(Ii) In the Ti / Al laminated film in which the Al layer is deposited on the Ti layer, the Ti layer before the heat treatment becomes the heating reaction layer 8 by the heat treatment. On the other hand, in the Al layer before the heat treatment, an Al—Si alloy film is formed in the lower part by the reaction with the metal Si diffused in the heating reaction layer, and an unreacted Al film remains in the upper part.

[0091]

(Iii) In the Al—Ti alloy film, the lower Al—Ti alloy film before the heat treatment becomes the heat reaction layer 8 by the heat treatment, and the unreacted Al—Ti alloy film remains at the uppermost portion before the heat treatment. .. Then, at the boundary with the heating reaction layer 8, an Al—Ti—Si alloy film is generated by the reaction with the metal Si that has diffused in the heating reaction layer.

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[0092]

FIG. 2 shows that after a Ti / Al laminated film in which an Al layer is deposited on a Ti layer is heat-treated at 1000 ° C. for 2 minutes, the ohmic electrode structure is formed by Auger electron spectroscopy (AES) method. It is a figure which shows the result of having analyzed the composition of the depth direction of. The etching rate by sputtering during AES measurement is 13 nm / min in terms of SiO2. As shown in FIG. 2, Al as the wiring conductor element 9 exists on the outermost surface side. Below the wiring conductor piece 9, there is an electrode film 7 made of Al containing oxygen (O) and Al below it containing Si. The thickness of the electrode film 7 is 312 nm in consideration of the etching rate by sputtering. Below the electrode film 7, there is a heating reaction layer 8 having a thickness of 367 nm. The heating reaction layer 8 is a Ti layer containing carbon (C) and Si. Below the heating reaction layer 8 is the SiC substrate 1.

[0093]

When the chemical state of each element was judged by target factor analysis (TFA) using CKLL, AlKLL, SiLVV, the chemical state of C was divided into two components, and the component on the surface side was Ti. Overlap with the distribution. From the peak shape (not shown), it is estimated that this is a carbide of Ti (TiC) in the heated reaction layer 8. On the other hand, the deeper component is presumed to be the component caused by the SiC of the SiC substrate 1.

[0094]

The chemical state of Al is also divided into two components, and the existence of a metal component and an oxide component is estimated from the peak shape not shown. In the profile of each component, the profile of oxide is in good agreement with the profile of O.

[0095]

Si is divided into two or three components. Since the fitting of two components is better when dividing the profile, a two-component system will be considered here. The presence of metal components and carbide components is estimated from the peak shapes not shown. Regarding

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the profile of the metal component, the surface side agrees well with the profile of the Al metal component of AlKLL. In the internal region corresponding to the TiC layer, a deviation is recognized from the profile of the Al metal component. Therefore, when the chemical state is judged from the shape of the spectrum (not shown), no difference is observed between the Al metal component and the corresponding spectrum. Therefore, it is determined to be a metal component. From this, it is estimated that Si exists in the metallic state in the TiC layer of the heating reaction layer 8.

[0096]
Further, the components found after the Ti layer are in good agreement with the profile of C (SiC), and the peak shape is presumed to be SiC of the SiC substrate 1.

[0097]

As described above, according to the AES measurement, when the Ti / Al laminated film is heat-treated at 1000 ° C. for 2 minutes, the heating reaction layer 8 contains metal carbide (TiC) and metal silicon. It can be presumed to be a solid solution.

When the Al / Ti laminated film is heat-treated, the heating reaction layer 8 is presumed to be a solid solution containing AlC and metallic silicon. The heated reaction layer 8 made of a solid solution containing the metal carbide and the metal silicon makes the Schottky barrier in the metal / semiconductor junction extremely low, and improves the morphology of the interface, and as a result, makes the heated reaction layer 8 uniform. It is determined that it can be generated.

[0098]
The Ti / Al laminated film or the Al film as one element of the Al / Ti laminated film can be replaced with an Al—Si eutectic film which is widely used for wiring of Si semiconductor electronic devices.

[0099]

As shown in FIG. 1, p-type SiC region 2 having a high surface carrier (hole) density is formed on the surface of SiC substrate 1.

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The p-type SiC region 2 is a region 2 in which the p-type epitaxial film is left in a mesa shape. The surface carrier density of p-type SiC region 2 is preferably 1 × 10 18 / cm 3 to 5 × 10 21 / cm 3. More preferably, a surface carrier density of 1 × 10 18 / cm 3 or more is desirable.

[0100]

Depending on the design of the semiconductor device, a plurality of bonding pads connected to each main electrode region and control electrode via wiring conductor pieces (main electrode wiring) 9 are formed on the field insulating film 5. May be. A passivation film made of an oxide film (SiO2), a PSG film, a BPSG film, a nitride film (Si3N4), a polyimide film or the like is formed on the wiring conductor element (main electrode wiring) 9 and the bonding pad. Is also good. Then, a plurality of openings (window portions) may be provided in a part of the passivation film so as to expose the plurality of electrode layers, so that bonding can be performed.

[0101]
Next, the manufacturing process of the ohmic electrode structure according to the first embodiment of the present invention will be described with reference to the process cross-sectional views (No. 1 to No. 3) shown in FIGS.

[0102]

(A) First, as shown in FIG. 3A, a p-type impurity (Al) having a high impurity density of 1 × 10 19 / cm 3 or more is applied to the Si surface of the 8 ° -off 4H-SiC substrate 1. The added p-type epitaxial growth layer (p-type SiC region) 20 having a thickness of several 100 nm is epitaxially grown.

Then, a 1.2 μm thick silicon oxide film (SiO 2 film) is deposited on the p-type epitaxial growth layer (p-type SiC region) 20 by the CVD method, and the well-known photolithography method and reactive ion etching (An etching mask 21 corresponding to the p-type SiC region 2 is formed by an etching technique such as the RIE method.

[0103]

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(B) Next, using the etching mask 21 made of the SiO2 film, the unnecessary epitaxial layer is removed by the RIE method using SF6 and O2 as the etchant gas, as shown in FIG. 3 (b). Further, thereafter, the etching mask 21 made of a SiO2 film is entirely removed with hydrofluoric acid (HF) to form a p-type SiC region 22 having a mesa structure separated from each other. When the p-type SiC region 22 functions as a drain region of the power IGT, the p-type SiC region 22 faces the drain region 2 in another place on the surface of the SiC substrate 1 by the same method (at the same time when the drain region 2 is formed). Then, the p-type SiC region as the source region is formed in a convex shape. In this case, an n-type SiC substrate or a π -type SiC substrate may be selected as the SiC substrate 1.

[0104]

(C) Then, the SiC substrate 1 is sufficiently cleaned using a predetermined cleaning method such as the RCA cleaning method well known in the silicon (Si) process. The RCA cleaning method is a conventional cleaning method of the semiconductor SiC substrate 1 in which the immersion treatment with the H2O2 + NH4OH mixed solution (SC-1) and the H2O2 + HCl mixed solution (SC-2) is combined. Then, as shown in FIG. 3C, the surface of the sufficiently cleaned SiC substrate 1 is thermally oxidized in a dry oxygen atmosphere at 1000 ° C. to 1150 ° C., and a thermal oxide film having a thickness of 5 to 40 nm is formed on the surface. Grow three. Note that steam may be used instead of the dry oxygen atmosphere. Thermal oxidation in dry oxygen in an atmosphere of 1150 ° C. for 3 hours gives a thermal oxide film 3 having a thickness of 35 to 40 nm. Thermal oxidation at 1150 ° C. for 2 hours in a wet atmosphere using water vapor gives a thermal oxide film 3 of 30 to 35 nm. In the case of thermal oxidation in a wet atmosphere using water vapor, it is preferable to anneal in argon (Ar) at 1150 ° C. for about 30 minutes thereafter. In order to reduce the thermal oxide film 3 to 20 nm or less, the oxidation temperature may be lowered or the oxidation time may be shortened. Considering as a manufacturing process of the power IGT, the thermal oxide film 3 formed on the surface of the SiC substrate 1 between the source region and the drain region 2 can be used as a gate oxide film.

[0105]

(D) Next, as shown in FIG. 4D, an upper insulating film 4 made of a SiO 2 film is deposited on the thermal oxide film 3 by an atmospheric pressure CVD method to form a field having a two-layer structure. The insulating film 5 is formed. It is desirable that the total thickness of the field

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insulating film 5, which is the sum of the thickness of the thermal oxide film 3 and the thickness of the upper insulating film 4, be about 600 nm to 1.5 μm. If it is considered as a manufacturing process of the power IGT, the gate electrode may be formed before the upper insulating film 4 is deposited. That is, after forming the thermal oxide film 3, a refractory metal such as W, Ti, or Mo, or a gate electrode material such as a silicide (WSi2, TiSi2, MoSi2) thereof is deposited on the thermal oxide film 3 by a sputtering method. , A vacuum evaporation method, a CVD method or the like. Then, the gate electrode material may be patterned by using the photolithography method and the RIE method to form the gate electrode on the gate oxide film 3 between the source region and the drain region 2. After forming the gate electrode, the SiC substrate 1 is cleaned by the RCA cleaning method or the like. An upper insulating film 4 made of a SiO2 film is deposited on the sufficiently cleaned gate electrode and the thermal oxide film 3 by an atmospheric pressure CVD method to form a field insulating film 5 having a two-layer structure.

[0106]

(E) Next, a photoresist 22 having a thickness of 1 to 2 μm is applied on the surface of the field acid insulating film 5 by using a spinner. Then, using a predetermined photomask (reticle), the photoresist 22 is selectively exposed and developed to remove the photoresist 22 in the portion corresponding to the opening 6. Subsequently, using the pattern of the photoresist 22 as an etching mask, the SiC substrate 1 is dipped in a BHF solution and wet-etched to form an opening 6 in the field insulating film 5 as shown in FIG. To form. When forming the fine openings 6, dry etching using gas plasma is preferable. For example, various dry etching methods such as RIE method using CHF3 or C2F6 as an etchant and electron cyclotron resonance ion etching (ECR ion etching) can be used. In this case, dry etching is first performed, and after leaving the field insulating film 5 of several tens of nm, switching to wet etching is performed. When the opening 6 is penetrated to the end by dry etching, 1) the surface of the SiC substrate 1 is roughened by plasma damage due to excessive plasma energy, and 2) hydrocarbon which is a reaction product generated by the etching reaction is SiC. The problem of redeposition on the surface of the substrate 1 and contamination of the surface occurs, which is a major obstacle to the uniform formation of a heating reaction layer described later. Furthermore, it results in a dramatic increase in the contact resistance ρc, which is not preferable.

[0107]

(F) After that, with the photoresist 22 as the etching mask remaining, the BHF solution is completely rinsed (rinsed) with ultrapure water and then dried. Then, the SiC substrate 1 with the resist mask 22 adhered thereon is immediately installed in the chamber of the vacuum vapor

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deposition apparatus, and immediately evacuated. The time left in the atmosphere from contact window opening etching to vacuum evacuation is a very important factor for increasing or decreasing the contact resistance ρc. When left in the air for a long time, a natural oxide film is formed on the surface of the SiC substrate 1 in the opening, or unwanted foreign matter is attached. For this reason, it will be a great obstacle to the uniform formation of a heating reaction layer described later, and the contact resistance ρc will be dramatically increased. Then, the chamber of the vacuum vapor deposition apparatus is evacuated to a pressure of less than 1.3×10^{-5} Pa with a turbo molecular pump, a cryopump, etc., and Al— is formed on the surface of the SiC substrate 1 as shown in FIG. The Ti-based electrode film 17 is deposited. As shown in FIG. 4F, in order to prevent the Al—Ti based electrode film 17 from adhering to the side wall of the opening, the directivity of the vapor deposition beam may be improved by using an orifice or the like. ..

[0108]

(G) After the vacuum deposition of the Al—Ti system electrode film 17, the SiC substrate 1 is taken out from the chamber of the vacuum deposition apparatus. Then, a lift-off method is used to obtain a substrate structure in which the Al—Ti based electrode film 7 is selectively embedded only in the opening as shown in FIG. That is, when the SiC substrate 1 is dipped in an organic solvent such as acetone or a dedicated photoresist stripping solution to completely remove the photoresist 22 left on the surface of the SiC substrate 1, the Al deposited on the photoresist 22 is removed. Since the —Ti-based electrode film 17 is also removed together with the photoresist 22, the Al—Ti-based electrode film 27 selectively remains only in the opening as shown in FIG.

[0109]

(H) Then, when the SiC substrate 1 is heat-treated in a non-oxidizing atmosphere at 700 ° C. to 1050 ° C. for a short time (about several minutes), as shown in FIG. The Al—Ti-based electrode film 27 and the SiC substrate 1 react with each other to generate a heated reaction layer 8 in the interface region between them, and excellent ohmic characteristics are realized between the heated reaction layer and p-type SiC. .. Infrared (IR) lamp heating may be used to perform heat treatment for a short time of about several minutes. Here, the "non-oxidizing atmosphere" is an atmosphere containing no gas of a compound containing oxygen such as oxygen (O2) or water (H2O). Specifically, an ultrahigh-purity inert gas atmosphere such as ultrahigh-purity argon (Ar) or ultrahigh-purity nitrogen (N2), high vacuum, or the like is suitable as the "non-oxidizing atmosphere". If even a small amount of oxygen is contained in these heat treatment atmospheres, oxides of Al and Ti (= insulators) are generated on the surface by heat treatment, or formation of

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a heated reaction layer is hindered. Regarding control, strict management is required. Specifically, the partial pressure of oxygen and water contained in the heat treatment atmosphere is at least about 1 × 10 −3 Pa to 1 × 10 −10 Pa, preferably 1. It is desirable that the pressure is about 10-5 Pa to 1 * 10-10 Pa. When heat treatment is performed in an ultra-high purity inert gas atmosphere, strict control is required such as the use of a deoxidizer or a gas purifier, in addition to baking of gas pipes and inspection of leaks. Further, when heat treatment is performed in a high vacuum, Al and Ti have a gettering action, and strictly speaking, the surface oxidizes even in a vacuum of about 1 × 10 −8 Pa. It is preferable to control the partial pressure of 1 × 10 −8 Pa to 1 × 10 −10 Pa and perform the heat treatment under ultrahigh vacuum. In the Al / Ti laminated film in which a Ti layer is deposited on the Al layer as the Al-Ti based electrode film 27, the lower Al layer before the heat treatment becomes the heat reaction layer 8 by the heat treatment. At this time, a Ti—Si alloy film is formed in the lower portion of the Ti layer before the heat treatment, and the electrode film 7 made of a laminated film of the Ti—Si alloy film and the unreacted Ti film in the upper portion is the heating reaction layer 8. Generated on. In the Ti / Al laminated film in which an Al layer is deposited on the Ti layer as the Al—Ti-based electrode film 27, the Ti layer before the heat treatment becomes the heating reaction layer 8 by the heat treatment, and the Al layer before the heat treatment is at the bottom. Since the Al—Si alloy film is formed and the unreacted Al film remains on the upper portion, the electrode film 7 composed of the Al—Si / Al layer is formed on the heating reaction layer 8.

When an Al—Ti alloy film is used as the Al—Ti-based electrode film 27, the lower Al—Ti alloy film before the heat treatment becomes the heat reaction layer 8 by the heat treatment, and unreacted Al is present at the top before the heat treatment. -Ti alloy film remains. Further, since the Al—Ti—Si alloy film is formed at the boundary with the heating reaction layer 8, the electrode film 7 composed of the Al—Ti—Si / Al—Ti layer is formed on the heating reaction layer 8. To be done. As the thermal reaction layer 8, a solid solution containing metal carbide and metal silicon is formed.

[0110]

(I) After the heating reaction layer 8 is formed, a conductor film 19 of Al or the like is deposited on the entire surface of the SiC substrate 11 as shown in FIG. 5 (i). Then, patterning is performed by a photolithography method and an etching technique such as RIE to form the wiring conductor piece 9 as shown in FIG. 1, whereby the ohmic electrode structure according to the first embodiment of the present invention is completed. .. If the wiring conductor piece 9 is a drain electrode wiring (main electrode wiring), similarly, the source electrode wiring (main electrode wiring is connected to the source region arranged opposite to the drain region 2). A

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power IGT is completed (the ohmic electrode on the source electrode side can be formed at the same time in the same process as the drain electrode side). When the etchant (= etching solution or etching gas) during patterning attacks the Al—Ti based electrode film 7, the conductor film 19 such as Al is arranged so as to cover the Al—Ti based electrode film 7. It may be configured.

[0111]

In order to strictly evaluate the effect of the ohmic electrode structure according to the first embodiment of the present invention, the contact resistance ρ c was measured using the linear transmission line model (linear TLM) evaluation method. In the linear TLM evaluation method, first, a linear TLM contact group having a structure in which rectangular contacts are arranged in a horizontal row while changing the contact spacing in the long side direction of a rectangular element isolation region (here, an n-type region) prepare. Then, the resistance is obtained from the current-voltage characteristics between two adjacent contacts. In the linear TLM evaluation method, this resistance is arranged as a function of the contact distance, and this is linearly approximated to perform mathematical processing to finally obtain a strict contact resistance ρ c.

[0112]

The configurations of the evaluated samples are as follows. The thickness and the impurity density of the p-type epitaxial layer are 800 nm and 1.2×10^{19} / cm 3 (Al-doped), respectively. The Al-Ti based electrode film 7 is composed of a Ti (50 nm thick) / Al (300 nm thick) laminated film. The thermal oxide film 3 forming the field insulating film 5 is a 1100 ° C. dry oxide film (10 nm thick), and the upper insulating film 4 thereon is a SiO2 film (400 nm thick) formed by atmospheric pressure CVD. The heat treatment temperature and heat treatment time and the heat treatment atmosphere for forming the heating reaction layer 8 are 1000 ° C. and 5 minutes, respectively, and a pure Ar atmosphere is used. The contact widths and lengths of the contact groups constituting the TLM pattern are 200 μ m and 100 μ m, respectively, and the contact intervals L = 6, 10, 15, 20, 25, 30 μ m.

[0113]

FIG. 6 shows current-voltage characteristics between adjacent contact electrodes with the contact spacing as a parameter. Since the straight line passing through the origin is obtained, it can be

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seen that ohmic contacts are obtained at all the electrodes forming the TLM pattern. FIG. 7 is a plot of the relationship between the resistance between the contact electrodes and the distance obtained from the slope of the straight line in FIG. The data is approximated by one straight line with little variation, and the contact resistance $\rho c = 9.5 \times 10^{-7}\ \Omega cm^2$ is obtained by the TLM method. When other conditions are the same and an Al (150 nm thick) / Ti (15 nm thick) laminated electrode film is used instead of the Ti / Al laminated electrode film, $\rho c = 7.0 \times 10^{-6}\ \Omega cm^2$ is obtained. .. When Al-Ti alloy is used, .rho.c = 9.0.times.10 @ -6 .OMEGA.cm @ 2 is obtained.

[0114]

In the method of manufacturing the ohmic electrode structure according to the first embodiment of the present invention, the heat treatment temperature is preferably 900 ° C or higher. According to the measurement of the contact resistance ρc using the TLM pattern composed of the Ti / Al laminated electrode film, $\rho c = 1.2 \times 10^{-2}\ \Omega cm^2$ at the heat treatment temperature of 700 ° C. and $\rho c =$ at the heat treatment temperature of 800 ° C. At $1.3 \times 10^{-3}\ \Omega cm^2$ and heat treatment temperature of 900 ° C., $\rho c = 4.3 \times 10^{-6}\ \Omega cm^2$, and at heat treatment temperature of 1000 ° C., $\rho c = 9.5 \times 10^{-7}\ \Omega cm^2$ was obtained as described above. Because it was done.

[0115]

Further, in the measurement of the contact resistance ρc using the above Ti / Al laminated electrode film, the contact was obtained when Ti was shaken at 10 nm, 20 nm, 50 nm and 100 nm while keeping the Al film thickness constant at 300 nm. The resistance ρc is the lowest at 100 nm, increases (deteriorates) by one digit at 50 nm, and gradually increases to 20 nm and 10 nm. Therefore, the film thickness of Ti is preferably 50 nm or more. More preferably, a value of 100 nm to 300 nm should be selected.

[0116]

As described above, the ohmic electrode structure according to the first embodiment of the present invention achieves a practical contact resistance ρc of $10^{-6}\ \Omega cm^2$ or less. As a result, the problem in the prior art of the SiC electronic device that the contact resistance ρc in the ohmic contact with the p-type SiC is high, or that the simplified configuration cannot be applied

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to the actual production of the SiC electronic device, is solved. There is.

[0117]

(Second Embodiment) The feature of the ohmic electrode structure according to the second embodiment of the present invention shown in FIG. 8 is that the p-type SiC region 32 is formed in the SiC substrate 1 by a selective ion implantation method. It is the point that constituted. That is, in the ohmic electrode structure according to the second embodiment of the present invention, the SiC substrate 1, the p-type SiC region 32 selectively formed on the surface of the SiC substrate 1, and the surface of the p-type SiC region 32 are formed. Of the partially formed heating reaction layer 8, the thermal oxide film 3 covering the interface between the SiC substrate 1 and the p-type SiC region 32, the upper insulating film 4 disposed on the surface of the thermal oxide film 3, and the heating reaction layer 8. It has at least the electrode film 7 disposed on the upper part. The p-type SiC region 32 functions as a main electrode region of a semiconductor device, especially a semiconductor electronic device.

[0118]

The field insulating film 5 is composed of a laminated structure of the thermal oxide film 3 and the upper insulating film 4. Further, a wiring conductor piece 9 is formed on the field insulating film 5 so as to be electrically connected to the electrode film 7. The wiring conductor piece 9 is a wiring member that connects the ohmic contact shown in FIG. 8 to another portion, and functions as a main electrode wiring of the semiconductor device. Therefore, although depending on the design, the wiring conductor piece 9 may be a main electrode wiring connected to a predetermined bonding pad. For the wiring conductor piece 9, well-known Al, Al-Si eutectic, Al-Cu-Si eutectic, Cu, Ti-W alloy, or the like is used.

[0119]

The heating reaction layer 8 is formed so as to enter the inside from a part of the surface of the p-type SiC region 32 and at the same time project upward from the surface of the p-type SiC region 32. Thermal oxide film 3 has a first opening through which heat reaction layer 8 penetrates, and covers SiC substrate 1 and p-type SiC region 32 so as to cover the interface between SiC substrate 1 and p-type SiC region 32. It is placed in contact with the surface. The upper insulating film 4 is an insulating film having a composition or density different from that

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of the thermal oxide film 3, and has a second opening continuous with the first opening. As shown in FIG. 8, the uppermost position of the electrode film 7 exists inside the second opening. The first and second openings form a common opening 6.

[0120]

As defined in the first embodiment of the present invention, in the ohmic electrode structure according to the second embodiment, the "insulating film having a composition different from that of the thermal oxide film 3" means the PSG film. , BSG, BPSG or Si3N4 film. The "insulating film having a density different from that of the thermal oxide film 3" corresponds to an insulating film such as a SiO2 film deposited by a method other than the thermal oxide film, for example, a CVD method, a sputtering method, a vacuum vapor deposition method or the like. The thermal oxide film 3 of SiC shown in FIG. 8 is a SiO2 film which is inferior to the thermal oxide film of Si but is close to the thermal oxide film of Si. Since the thermal oxide film and the SiO2 film deposited by another method have different densities, the boundaries can be seen by observing the cross section with high resolution SEM. Further, the thermal oxide film 3 of SiC and the upper insulating film 4 can be clearly distinguished by measuring the dielectric breakdown field strength, the etching rate with respect to the BHF solution, the infrared absorption spectrum, and the Raman spectrum.

[0121]

The thickness of the thermal oxide film 3 is preferably 2 to 50 nm. Particularly, the thickness of the thermal oxide film 3 in the range of 5 to 20 nm is desirable. As described in the first embodiment, when the thickness of the thermal oxide film 3 is thinner than 5 nm, the effect of removing the damaged region on the surface of the SiC substrate 1 caused by the surface polishing or the ion implantation method and the foreign matter on the surface are removed. The removal effect becomes poor. On the other hand, if the thickness of the thermal oxide film 3 is thicker than 50 nm, the surface of the SiC substrate 1 is gradually roughened due to excessive thermal oxidation, and the surface morphology is reduced.

[0122]

The total thickness of the field insulating film 5, which is the sum of the thickness of the thermal oxide film 3 and the thickness of the upper insulating film 4, is preferably 100 nm to 3 μm.

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Particularly, it is desirable that the thickness is 300 nm or more. Further, if it is a high breakdown voltage power semiconductor device, it may be set to 800 nm or more. However, if the field insulating film 5 becomes too thick, cracks and the like will occur, so 3 μm or more is not preferable.

[0123]
If the laminated structure in which the upper insulating film 4 such as various SiO 2 films other than the thermal oxide film of SiC as shown in FIG. 8 is formed on the thermal oxide film 3 of SiC, the semiconductor device specifications can be improved. The surface morphology of SiC can be favorably maintained while ensuring the pressure resistance and surface stability required as.

[0124]

The electrode film 7 shown in FIG. 8 is made of a metal containing at least one of Al and Ti, which is disposed above the heating reaction layer 8 in the second opening of the upper insulating film 4.

As described in the first embodiment, the "electrode film 7 made of a metal containing at least one of Al and Ti" is a laminated film made of a lower Ti—Si alloy film and an upper Ti film. Is preferably a laminated film formed of the Al—Si alloy film and the upper Al film, or a laminated film formed of the lower Al—Ti—Si alloy film and the upper Al—Ti alloy film. The thermal reaction layer 8 is preferably a solid solution containing metal carbide and metal silicon. The heated reaction layer 8 made of a solid solution containing the metal carbide and the metal silicon makes the Schottky barrier in the metal / semiconductor junction extremely low, and improves the morphology of the interface, and as a result, makes the heated reaction layer 8 uniform. It is determined that it can be generated. The Al film which is one element of the Ti / Al laminated film or the Al / Ti laminated film can be replaced with an Al—Si eutectic film which is often used for wiring of Si semiconductor electronic devices.

[0125]

As shown in FIG. 8, p-type SiC region 32 having a high surface carrier (hole) density is formed on the surface of SiC substrate 1. The ion implantation method is advantageous in that the p-type SiC region 32 having a higher impurity density can be formed than in the case of the epitaxial p-type SiC region 2 according to the first embodiment. It is desirable that the surface carrier

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density (surface hole density) of the p-type SiC region 32 is at least 1 × 10 17 / cm 3 or more, preferably 1 × 10 18 / cm 3 or more.

[0126]

The conductivity type and impurity density of SiC substrate 1 differ depending on the design specifications of the semiconductor device using the ohmic electrode structure according to the second embodiment of the present invention. Further, another semiconductor region having a plane area larger than that of the p-type SiC region 32 and a deep diffusion depth is arranged in a well shape on the surface of the SiC substrate 1, and the p-type SiC region 32 is formed on the inner surface thereof. May be. For example, in the case of a pnp-type bipolar transistor, a base region made of an n-type SiC region is formed on the surface of a p-type SiC substrate 1 which is a collector region, and a p-type SiC region as an emitter region is formed inside this base region. 32 may be formed. In this case, an intrinsic semiconductor (i-type) SiC substrate 1 is used in place of the low-impurity-density p-type SiC substrate 1 serving as the collector region, and the rear surface (or part of the front surface) of the i-type SiC substrate 1 has a high impurity density. You may form the collector region which consists of p-type SiC region of.

[0127]

In the case of a thyristor such as a GTO thyristor, an n base region composed of an n type SiC region is formed on the surface of the p type SiC substrate 1 serving as ap base region, and an anode region is formed inside the n base region. The p-type SiC region 32 can be formed. In this case, an n-type SiC region as a cathode region is formed on the back surface of the p-type SiC substrate 1 that serves as the p base region. On the other hand, in the n-channel junction type FET or the junction type SIT, the p-type SiC region 32 as the source region can be formed on the surface of the n-type SiC substrate 1 functioning as the channel region. Further, in the n-channel SI thyristor, the p-type SiC region 32 as the anode region can be formed on the surface of the n-type SiC substrate 1 functioning as the channel region.

[0128]

In the p-channel power IGT, the p-type SiC region 32 as the drain region can be formed on the surface of the p-type SiC substrate 1 functioning as the drift region. In this case, p-type SiC region 32 as the source region is formed in the n-body region formed on the surface of p-type

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SiC substrate 1. In an n-channel IGBT, a high impurity density p-type SiC region 32 as a collector region can be formed on the surface of an n-type SiC substrate (or ν -type SiC substrate) 1 that functions as a drift region. In this case, another n-type SiC region as the emitter region is formed in the p-body region formed on the surface of the n-type (or ν -type) SiC substrate 1. The ohmic electrode structure according to the second embodiment of the present invention can be applied to the p-type SiC region 32 that functions as the main electrode region of these various semiconductor electronic devices.

[0129]

Next, the manufacturing process of the ohmic electrode structure according to the second embodiment of the present invention will be described with reference to the process cross-sectional views (No. 1 to No. 3) shown in FIGS.

[0130]

(A) First, a SiO 2 film 33 having a thickness of about 1.5 μm is deposited on the entire surface of the 4H—SiC substrate 1 by the CVD method, and a photoresist 34 is spin-coated thereon.

Then, as shown in FIG. 9A, the SiO2 film 33 deposited on the p-type SiC region formation planned region is selectively removed by the well-known photolithography method and wet etching technique, and the ion implantation mask film 33 is formed. To form.

[0131]

(B) Then, as shown in FIG. 9B, the ion implantation through film 35 made of a thin SiO 2 film is again deposited on the entire surface of the ion implantation mask film 33 by the CVD method. The ion implantation through film 35 is a film for adjusting a projection range (depth) Rp at the time of ion implantation described later. After depositing the ion implantation through film 35, p-type impurity ions such as 27Al + and 11B + (boron) are formed on the entire surface of the SiC substrate 1 so that the impurity density of at least the surface of the SiC substrate 1 becomes 1 $\times$ 10 20 / cm 3 or more, and Ions are implanted so as not to impair the crystallinity of the SiC substrate 1. An example of conditions for ion-implanting 27Al + as p-type impurity ions into the SiC substrate 1 is as follows. In the SiC substrate 1 heated to 750 ° C., the dose Φ / acceleration energy EAC is changed as follows. Multi-stage implantation: First ion implantation Φ = 0.9 $\times$ 10 15 cm -2 / EAC = 30 KeV; Second ion implantation Φ = 51.2 $\times$ 10 15 cm -2 / EAC = 60 KeV;

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Third ion implantation Φ = 1.5 × 1015 cm-2 / EAC = 100 KeV; 4th ion implantation Φ = 2.4 × 10 15 cm-2 / EAC = 150 KeV; 5th ion implantation Φ = 3.0 × 10 15 cm-2 / EAC = 190 KeV.

[0132]

(C) When the 5-step multi-step ion implantation is completed, the ion implantation mask film 33 and the ion implantation through film 35 are entirely removed with hydrofluoric acid (HF). Then, when rapid heat treatment at 1700 ° C. for 1 minute is performed in an atmospheric pressure Ar atmosphere, the ion-implanted 27Al + is activated, and as shown in FIG. 9C, the p-type SiC region 32 having a high impurity density is formed. Are selectively formed.

[0133]

(D) The subsequent steps are almost the same as the steps shown in FIG. 3C and subsequent figures described in the manufacturing steps of the first embodiment. That is, the SiC substrate 1 is sufficiently cleaned by using the SiC substrate 1 cleaning method such as the RCA cleaning method. Then, as shown in FIG. 10D, the surface of the sufficiently cleaned SiC substrate 1 is thermally oxidized in a dry oxygen atmosphere, and a thermal oxide film 3 having a thickness of 5 to 20 nm is grown on the surface.

[0134]

(E) Next, as shown in FIG. 10E, an upper insulating film 4 made of a SiO 2 film is deposited on the thermal oxide film 3 by the atmospheric pressure CVD method to form a field having a two-layer structure. The insulating film 5 is formed.

[0135]

(F) Next, a photoresist 22 having a thickness of 1 to 2 μm is applied on the surface of the field acid insulating film 5 using a spinner.

Then, using a predetermined photomask (reticle), the photoresist 22 is selectively exposed and developed to remove the photoresist 22 in the portion corresponding to the opening 6. Then, using the pattern of the photoresist 22 as an etching mask, the SiC substrate 1 is dipped in a BHF

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solution and wet-etched to form an opening 6 in the field insulating film 5 as shown in FIG. Form.

[0136]

(G) Then, with the photoresist 22 as an etching mask remaining, it is rinsed completely with ultrapure water and then dried. Then, the SiC substrate 1 with the resist mask 22 adhered is installed in the chamber of the vacuum vapor deposition apparatus and immediately evacuated. Then, the chamber of the vacuum vapor deposition apparatus is evacuated to a pressure of less than 1.3×10^{-5} Pa with a turbo molecular pump, a cryopump, etc., and Al— is formed on the surface of the SiC substrate 1 as shown in FIG. The Ti-based electrode film 17 is deposited.

[0137]

(H) After vacuum deposition of the Al—Ti system electrode film 17, the SiC substrate 1 is taken out from the chamber of the vacuum deposition apparatus. Subsequently, a lift-off method is used to obtain a substrate structure in which the Al—Ti based electrode film 7 is selectively embedded only in the opening as shown in FIG. That is, when the photoresist 22 is completely removed, as shown in FIG. 11H, the Al—Ti based electrode film 7 selectively remains only in the opening.

[0138]

(I) After that, when the SiC substrate 1 is heat-treated in a non-oxidizing atmosphere at 700 ° C. to 1050 ° C. for a short time (several minutes), as shown in FIG. The —Ti-based electrode film and the SiC substrate 1 react with each other to form the heated reaction layer 8 in the interface region between them. At this time, the partial pressure of oxygen and water contained in the heat treatment atmosphere is controlled to be at least about 1×10^{-3} Pa to 1×10^{-10} Pa. As a result, excellent ohmic characteristics are realized between the heating reaction layer 8 and the p-type SiC region 32. In the Al / Ti laminated film in which a Ti layer is deposited on the Al layer as the Al-Ti based electrode film 27, the lower Al layer before the heat treatment becomes the heat reaction layer 8 by the heat treatment. At this time, a Ti—Si alloy film is formed in the lower portion of the Ti layer before the heat treatment, and the electrode film 7 made of a laminated film of the Ti—Si alloy film and the unreacted Ti film in the upper portion is the heating reaction layer 8. Generated on. In the Ti / Al laminated film in which an Al layer is deposited on the Ti

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layer as the Al—Ti-based electrode film 27, the Ti layer before the heat treatment becomes the heating reaction layer 8 by the heat treatment, and the Al layer before the heat treatment is at the bottom. Since an Al-Si alloy film is formed and an unreacted Al film remains on the upper portion, the electrode film 7 made of an Al-Si / Al layer is formed on the heating reaction layer 8. When an Al—Ti alloy film is used as the Al—Ti-based electrode film 27, the lower Al—Ti alloy film before the heat treatment becomes the heat reaction layer 8 by the heat treatment, and unreacted Al is present at the top before the heat treatment. -Ti alloy film remains. Further, since the Al—Ti—Si alloy film is formed at the boundary with the heating reaction layer 8, the electrode film 7 composed of the Al—Ti—Si / Al—Ti layer is formed on the heating reaction layer 8. To be done. As the thermal reaction layer 8, a solid solution containing metal carbide and metal silicon is formed. After forming the heating reaction layer 8, a conductor film 19 such as Al is vapor-deposited on the entire surface of the SiC substrate 11 as in the case of FIG. 5I described in the first embodiment. Then, patterning is performed by a photolithography method and an etching technique such as RIE to form the wiring conductor piece 9 as shown in FIG. 8, whereby the ohmic electrode structure according to the second embodiment of the present invention is completed. ..

[0139]

In order to precisely evaluate the effect of the ohmic electrode structure according to the second embodiment of the present invention, a linear TLM contact group similar to that of the first embodiment was produced. The structure of the evaluated sample is as follows. The doping density of the impurity Al in the p-type SiC region 32 (= ion-implanted layer) is $3 \times 10\ 20$ / cm 3 near the contact with the heating reaction layer 8. Other conditions are the same as those of the ohmic electrode structure according to the first embodiment. That is, the Al-Ti-based electrode film 7 is a Ti (50 nm thick) / Al (300 nm thick) laminated film, the thermal oxide film 3 of the field insulating film 5 is a 1100 ° C. dry oxide film (10 nm thick), and the upper insulating film 4 is formed. Is a SiO2 film (400 nm thick) formed by atmospheric pressure CVD. The heat treatment temperature and heat treatment time for forming the heated reaction layer 8 and the heat treatment atmosphere were 1000 ° C. and 5 minutes, respectively, and a pure Ar atmosphere was used.

[0140]

The contact resistance ρ c obtained by the TLM method was $\rho c = 4.3 \times 10 -7\ \Omega cm\ 2$. It is considered that the reason why the value lower than that in the first embodiment is obtained is that the high impurity density is obtained by the high dose ion implantation and the effective

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activation annealing. That is, it is considered that the existence of the high impurity density p-type SiC region 32 made the Schottky barrier at the interface between the heating reaction layer 8 and the p-type SiC region 32 thinner. If the p-type ohmic contact is formed with an Al-Ti alloy film (400 nm thickness, containing Ti: 10%) instead of this Ti / Al laminated electrode film under the same conditions other than the Ti / Al laminated electrode film, Although several times higher, $\rho c = 1.2 \times 10^{-6}$ Ωcm 2 is obtained which is lower than that of the prior art.

[0141]

As described above, according to the ohmic electrode structure of the second embodiment of the present invention, a practical contact resistance ρc of 10^{-6} Ωcm 2 or less can be achieved. As a result, a low contact resistance ρc can be obtained inside the fine opening (contact window) that can be adopted in the actual device structure, and a high-performance SiC electronic device can be easily realized with a simplified configuration. Can be manufactured.

[0142]
(Third Embodiment) In the ohmic electrode structure according to the third embodiment of the present invention shown in FIG. 12, the planar dimension of the electrode film 47 is larger than that of the opening, and the ohmic electrode structure is superposed on the field insulating film 5. The difference from the ohmic electrode structures according to the first and second embodiments is that the ohmic electrode structures according to the first and second embodiments are arranged.

[0143]

The p-type SiC region 32 may be composed of a SiC region formed of a p-type epitaxial growth layer having a high impurity density as in the first embodiment, or selective ion implantation as in the second embodiment. It may be composed of regions.

Here, an example of forming by the ion implantation method will be described. Similar to the first and second embodiments, the p-type SiC region 32 functions as a main electrode region of a semiconductor device, especially a semiconductor electronic device.

[0144]

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As shown in FIG. 12, the ohmic electrode structure according to the third embodiment of the present invention includes a SiC substrate 1, a p-type SiC region 32 selectively formed on the surface of the SiC substrate 1, and a p-type SiC region 32. The heat reaction layer 8 formed on a part of the surface of the p-type SiC region 32, the thermal oxide film 3 covering the interface between the SiC substrate 1 and the p-type SiC region 32, and the upper insulation disposed on the surface of the thermal oxide film 3. At least the film 4 and the electrode film 47 arranged on the heating reaction layer 8. The field insulating film 5 is composed of a laminated structure of the thermal oxide film 3 and the upper insulating film 4. Thermal oxide film 3 has a first opening through which heat reaction layer 8 penetrates, and covers SiC substrate 1 and p-type SiC region 32 so as to cover the interface between SiC substrate 1 and p-type SiC region 32. It is placed in contact with the surface. The upper insulating film 4 is an insulating film having a composition or density different from that of the thermal oxide film 3, and has a second opening continuous with the first opening.

[0145]

The heated reaction layer 8 is formed so as to enter the inside from a part of the surface of the p-type SiC region 32 and at the same time project upward from the surface of the p-type SiC region 32. Then, the electrode film 47 disposed on the heating reaction layer 8 extends from the second opening and overlaps the field insulating film 5 located around the second opening. That is, the A electrode film 47 is formed in a plane pattern larger than the second opening so as to completely seal the second opening. Further, the wiring conductor element 9 is formed so as to be electrically connected to the electrode film 47 which completely seals the second opening. The wiring conductor piece 9 functions as a main electrode wiring of the semiconductor device. Therefore, although depending on the design, the wiring conductor piece 9 may be a main electrode wiring connected to a predetermined bonding pad. The wiring conductor piece 9 is formed on the field insulating film 5 with a conductive material such as Al, Al—Si eutectic, Al—Cu—Si eutectic, Cu, and Ti—W alloy.

[0146]

The electrode film 47 shown in FIG. 12 is a laminated film composed of a lower Al—Si alloy film and an upper unreacted Al film. According to the AES measurement, when the Ti / Al laminated film is heat-treated at 1000 ° C. for 2 minutes, it can be estimated that the heating reaction layer 8 is a solid solution containing TiC and metallic silicon. The heating reaction layer 8 made

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of a solid solution containing TiC and metallic silicon makes the Schottky barrier in the metal / semiconductor junction extremely low and improves the morphology of the interface. As a result, the heating reaction layer 8 is uniformly formed. It is judged that it can be done. The Al film as the upper layer of the Ti / Al laminated film deposited before the heat treatment can be replaced with an Al—Si eutectic film which is often used for wiring of Si semiconductor electronic devices. In this case, the electrode film 47 is composed of a lower Al—Si alloy film and an upper unreacted Al—Si alloy film, and is an alloy film having a distribution of Si composition.

[0147]

It should be noted that Al is melted at a high temperature of 660 ° C. or higher, and the adhesiveness and wettability with the field insulating film 5 are significantly deteriorated. Therefore, in the third embodiment, the peripheral portion of the field insulating film 5 is In addition, the Al / Ti laminated electrode in direct contact with the Al layer is not suitable as an electrode material which is a raw material for forming the heating reaction layer 8.

[0148]

As defined in the first embodiment of the present invention, in the ohmic electrode structure according to the third embodiment, the "insulating film having a composition different from that of the thermal oxide film 3" means the PSG film. , BSG, BPSG or Si3N4 film.

The "insulating film having a density different from that of the thermal oxide film 3" corresponds to an insulating film such as a SiO2 film deposited by a method other than the thermal oxide film, for example, a CVD method, a sputtering method, a vacuum vapor deposition method or the like. The thickness of the thermal oxide film 3 is preferably 2 to 50 nm. Particularly, the thickness of the thermal oxide film 3 in the range of 5 to 20 nm is desirable. As described in the first embodiment, when the thickness of the thermal oxide film 3 is thinner than 5 nm, the effect of removing the damaged region on the surface of the SiC substrate 1 caused by the surface polishing or the ion implantation method and the removal of foreign matter on the surface are removed. The effect of doing is poor. On the other hand, if the thickness of the thermal oxide film 3 is thicker than 50 nm, the surface of the SiC substrate 1 is gradually roughened due to excessive thermal oxidation, and the surface morphology is reduced. The total thickness of the field insulating film 5, which is the sum of the thickness of the thermal oxide film 3 and the thickness of the upper insulating film 4, is preferably 100 nm to 3 μm. Particularly, it is desirable that the thickness is 300 nm or more. Further, if it is a high breakdown voltage power semiconductor device, it may be set to 800 nm or more. However, if the field insulating film 5 becomes too thick, cracks and the like will occur, so 3 μm or more is not preferable.

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[0149]
If a laminated structure in which an upper insulating film 4 such as various SiO 2 films other than the SiC thermal oxide film as shown in FIG. 12 is formed on the SiC thermal oxide film 3 is adopted, the semiconductor device specifications can be improved. The surface morphology of SiC can be favorably maintained while ensuring the pressure resistance and surface stability required as.

[0150]

It is desirable that the surface hole density of the p-type SiC region 32 is at least 1 × 10 17 / cm 3 or more, preferably 1 × 10 18 / cm 3 or more.

The conductivity type and the impurity density of the SiC substrate 1 differ depending on the semiconductor device using the ohmic electrode structure according to the third embodiment. For example, as in the application example of the ohmic electrode structure according to the second embodiment, the p-type SiC region 32 functioning as the main electrode region of various semiconductor electronic devices is selected as a conductive material selected according to its design. It can be formed (directly or via another semiconductor region) on the SiC substrate 1 having the mold and the impurity density. Therefore, the conductivity type and the impurity density of the SiC substrate 1 are not specified here.

[0151]
Next, the manufacturing process of the ohmic electrode structure according to the third embodiment of the present invention will be described with reference to the process sectional views (No. 1 and No. 2) shown in FIGS.

[0152]

(A) The p-type SiC region 32 is selectively formed on the surface of the 4H—SiC substrate 1 by using the photolithography method, the ion implantation method, or the like, just as in the method described in the second embodiment. To form.

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That is, p-type impurity ions such as Al ions or B ions are implanted into the surface of the SiC substrate 1 and activated by heat treatment to form the p-type SiC region 32. Then, the surface of the sufficiently cleaned SiC substrate 1 is thermally oxidized in a dry oxygen atmosphere to heat the surface almost in the same manner as the steps of FIG. 10D and subsequent steps described in the manufacturing process of the second embodiment. The oxide film 3 is grown. Next, as shown in FIG. 13A, an upper insulating film 4 made of a SiO2 film is deposited on the thermal oxide film 3 by an atmospheric pressure CVD method to form a field insulating film 5 having a two-layer structure. ..

[0153]

(B) Next, a photoresist 22 having a thickness of 1 to 2 μm is applied to the surface of the field acid insulating film 5 using a spinner. Then, using a predetermined photomask (reticle), the photoresist 22 is selectively exposed and developed to remove the photoresist 22 in the portion corresponding to the opening 6. Subsequently, using the pattern of the photoresist 22 as an etching mask, the SiC substrate 1 is dipped in a BHF solution and wet-etched to form an opening 6 in the field insulating film 5 as shown in FIG. 13B. Form.

[0154]

(C) After that, the photoresist 22 used for etching is stripped using acetone or a dedicated photoresist stripping solution. Then, the SiC substrate 1 is dipped in a BHF solution for about 10 seconds to slightly etch the field insulating film 5 to completely remove the residue of the photoresist 22 attached to the field insulating film 5. The residue of the photoresist 22 remaining on the field insulating film 5 significantly reduces the adhesion of the electrode film 47 (or 17, 57) arranged so as to overlap the field insulating film 5 to the field insulating film 5. The process is essential. The BHF solution is completely rinsed with ultrapure water, and the dried SiC substrate 1 is immediately installed in the chamber of the vapor deposition apparatus and immediately evacuated. When a predetermined ultimate pressure is obtained, a 50 nm-thick Ti layer is formed as an Al—Ti-based electrode film 17 on the inside of the opening 6 and the entire surface of the field insulating film 5, as shown in FIG. 13C. A Ti / Al laminated film consisting of an Al layer having a thickness of 300 nm is vapor-deposited thereon. In order to improve the step coverage in the opening 6, unlike the first and second embodiments, it is preferable to adopt the oblique vapor deposition method.

[0155]

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(D) After vacuum deposition of the Ti / Al laminated film as the Al—Ti system electrode film 17, the SiC substrate 1 is taken out from the chamber of the vacuum deposition apparatus. Subsequently, a photoresist 23 having a thickness of 1 to 2 μm is applied to the surface of the Al—Ti based electrode film (Ti / Al laminated film) 17 using a spinner. Then, by selectively exposing and developing the photoresist 23 using a predetermined photomask (reticle), as shown in FIG. 14D, one portion of the field insulating film 5 in the opening and the peripheral portion thereof is formed. The photoresist 23 is selectively left only on the upper part of the portion.

[0156]

(E) Next, using the pattern of the photoresist 23 as an etching mask, as shown in FIG. 14E, Al-- The Ti-based electrode film 57 is left and the other portions of the Al-Ti-based electrode film 17 are removed. The etching may be wet etching or dry etching. A mixed solution of phosphoric acid (H3PO4): nitric acid (HNO3): acetic acid (CH3COOH) can be used as an etchant for wet etching. As an etchant gas for dry etching, a mixed gas of chlorine (Cl2): boron bromide (BBr3) can be used. After the etching is completed, it is immersed in a dedicated photoresist stripping solution, rinsed and dried. After drying, it is subjected to an oxygen plasma ashing device and then to an Ar sputter etcher to completely remove the oxide film on the surface of the Al—Ti based electrode film 57 generated by the ashing of the photoresist.

[0157]

(F) Then, when the SiC substrate 1 is heat-treated in a non-oxidizing atmosphere at 700 ° C. to 1050 ° C. for a short time (about several minutes), as shown in FIG. The —Ti-based electrode film 57 and the p-type SiC region 32 react with each other to form the heated reaction layer 8 in the interface region between the two. At this time, the partial pressure of oxygen and water contained in the heat treatment atmosphere is controlled to be at least about 1×10^{-3} Pa to 1×10^{-10} Pa. As a result, excellent ohmic characteristics are realized between the heating reaction layer 8 and the p-type SiC region 32. In the Ti / Al laminated film in which an Al layer is deposited on the Ti layer as the Al—Ti-based electrode film 57, the Ti layer before the heat treatment mainly becomes the heating reaction layer 8 by the heat treatment. On the other hand, in the Al layer before the heat treatment, an Al—Si alloy film is formed in the lower portion and an unreacted Al film remains in the upper portion, so that the electrode film 7 made of the Al—Si / Al layer is formed on the heating reaction layer 8. Is generated. As the thermal reaction layer 8, a solid solution containing metal carbide and metal silicon is formed.

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[0158]

(G) Finally, as in the first and second embodiments, a conductor film of Al or the like is deposited on the entire surface of the SiC substrate 1 and patterned by photolithography and etching to form a wiring conductor. The element piece 9 is formed, and the ohmic electrode structure for the p-type SiC region 32 shown in FIG. 12 is completed. When the etchant (= etching liquid or etching gas) for patterning the wiring invades the electrode film 47, the wiring conductor element 9 is arranged so as to cover the electrode film 47 without fail.

[0159]

In order to precisely evaluate the effect of the ohmic electrode structure according to the third embodiment of the present invention, a linear TLM contact group was produced. The doping density of the impurity Al in the p-type SiC region 32 (= ion-implanted layer) is 3×10^{20} / cm 3 near the contact with the heating reaction layer 8. The thermal oxide film 3 forming the field insulating film 5 is a 1100 ° C. dry oxide film (10 nm thick), and the upper insulating film 4 is a SiO2 film (400 nm thick) formed by atmospheric pressure CVD. The heat treatment temperature and heat treatment time for forming the heated reaction layer 8 and the heat treatment atmosphere were 1000 ° C. and 5 minutes, respectively, and a pure Ar atmosphere was used.

[0160]

The contact resistance ρc obtained by the TLM method was $\rho c = 6.4 \times 10^{-7}$ Ωcm 2, which was almost the same value as that of the Ti / Al laminated electrode of the second embodiment.

[0161]

(Other Embodiments) As described above, the present invention has been described by the first to third embodiments, but the description and drawings forming a part of this disclosure limit the present invention. Should not be understood to be.

From this disclosure, various alternative embodiments, examples, and operation techniques will be apparent to those skilled in the art.

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[0162]
In the manufacturing processes of the above-described first to third embodiments, the thermal oxide film 3 which is an element of the field insulating film 5 is formed immediately before the upper insulating film 4 is formed. As shown in the process cross-sectional view of FIG. 15, even if the thermal oxide film is formed immediately after the formation of the upper insulating film 4, substantially the same effect can be obtained.

[0163]

(A) For example, the p-type SiC region 32 is formed on the surface of the SiC substrate 1 by the same method as the method described in the second embodiment.

Then, the SiC substrate 1 is cleaned sufficiently by using the SiC substrate 1 cleaning method such as the RCA cleaning method. Thereafter, as shown in FIG. 15A, an oxygen permeable insulating film 44 such as a SiO2 film is deposited on the SiC substrate 1 by the atmospheric pressure CVD method.

[0164]

(B) After depositing the oxygen permeable insulating film 44, as shown in FIG. 15B, heat treatment is performed in a dry oxygen atmosphere to thermally oxidize the surface of the SiC substrate 1 to form the oxygen permeable insulating film 44. A thermal oxide film 3 is grown on the interface with the SiC substrate 1. Similar to the first embodiment, the thickness of the thermal oxide film 3 is less than 50 nm, preferably 5 to 20 nm. As a result, the upper insulating film 4 made of the oxygen permeable insulating film (SiO2 film) 44 is located on the thermal oxide film 3, and the field insulating film 5 having a two-layer structure is formed.

[0165]

(C) After that, it is possible to proceed with the same steps as the method shown in FIG. 10 (f) and subsequent figures described in the second embodiment. That is, as shown in FIG. 15C, a photoresist 22 having a thickness of 1 to 2 μm is applied to the surface of the field acid

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insulating film 5 using a spinner. Then, using a predetermined photomask (reticle), the photoresist 22 is selectively exposed and developed to remove the photoresist 22 in the portion corresponding to the opening 6. Subsequently, using the pattern of the photoresist 22 as an etching mask, wet etching is performed to form an opening 6 in the field insulating film 5 as shown in FIG. 15C. The subsequent description will be omitted because it is redundant.

[0166]
By using the method shown in FIG. 15, it is possible to achieve a practical contact resistance ρ c of 10^{-6} Ωcm 2 or less.

[0167]
Further, as shown in the process cross-sectional views (No. 1 and No. 2) of FIGS. 16 and 17, the thermal oxide film may be formed immediately after the opening is formed.

[0168]

(A) For example, the p-type SiC region 32 is formed on the surface of the SiC substrate 1 by the same method as the method described in the second embodiment.

Then, after the SiC substrate 1 is sufficiently cleaned, an oxygen permeable insulating film 44 such as a SiO2 film is deposited on the SiC substrate 1 by the atmospheric pressure CVD method as shown in FIG. 16 (a).

[0169]

(B) Next, a photoresist 22 having a thickness of 1 to 2 μm is applied to the surface of the oxygen permeable insulating film 44 using a spinner.

Then, using a predetermined photomask (reticle), the photoresist 22 is selectively exposed and developed to remove the photoresist 22 in the portion corresponding to the opening 6. Subsequently, by using the pattern of the photoresist 22 as an etching mask, the oxygen permeable insulating film 44 is wet-etched to form the opening 6 in the oxygen permeable insulating film 44 as shown in FIG. 16B. Form.

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[0170]

(C) After the opening 6 is formed, the photoresist 22 used for etching the oxygen permeable insulating film 44 is removed using acetone or a dedicated photoresist removing solution. Subsequently, the SiC substrate 1 is dipped in a BHF solution for about 10 seconds to slightly etch the oxygen permeable insulating film 44, thereby completely removing the residue of the photoresist 22 attached to the oxygen permeable insulating film 44. Further, the surface of the SiC substrate 1 exposed inside the opening 6 is sufficiently cleaned by using the SiC substrate 1 cleaning method such as the RCA cleaning method. Then, as shown in FIG. 16C, thermal oxidation is performed in a dry oxygen atmosphere, and the surface of the SiC substrate 1 exposed inside the opening 6 and the interface between the oxygen permeable insulating film 44 and the SiC substrate 1 are heated. The oxide film 3 is grown. Since the oxidation rate of the surface of the SiC substrate 1 exposed inside the opening 6 is higher than the oxidation rate at the interface between the oxygen permeable insulating film 44 and the SiC substrate 1, the SiC substrate 1 exposed inside the opening 6 A thermal oxide film having a thicker surface is formed. The thickness of the thermal oxide film 3 at the interface between the oxygen permeable insulating film 44 and the SiC substrate 1 is less than 50 nm, preferably 5 to 20 nm. When the thickness is less than 5 nm, the effect of removing the damaged region on the surface of the SiC substrate 1 caused by surface polishing or ion implantation and the effect of removing foreign matter on the surface are poor, and when the thickness is more than 50 nm, the surface of the SiC substrate 1 is excessively oxidized due to excessive thermal oxidation. Is gradually getting rough.

[0171]

(D) Then, the entire surface is etched with a BHF solution, and the thermal oxide film 3 on the surface of the SiC substrate 1 exposed inside the opening 6 is self-aligned as shown in FIG. except.

[0172]

(E) The dried SiC substrate 1 is immediately installed in the chamber of the vapor deposition apparatus and immediately evacuated.

When a predetermined ultimate pressure is obtained, an Al—Ti based electrode film 17 is vapor-

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deposited on the inside of the opening 6 and the entire surface of the field insulating film 5 by the oblique vapor deposition method, as shown in FIG.

[0173]

(F) After vacuum deposition of the Al—Ti system electrode film 17, the SiC substrate 1 is taken out from the chamber of the vacuum deposition apparatus. Then, a photoresist 23 having a thickness of 1 to 2 μm is applied to the surface of the Al—Ti based electrode film 17 using a spinner. Then, by using a predetermined photomask (reticle), the photoresist 23 is selectively exposed and developed, so that only a part of the opening and the peripheral portion thereof overlapping the field insulating film 5 is selectively exposed. The resist 23 is left. Then, using the pattern of the photoresist 23 as an etching mask, as shown in FIG. 17F, the Al—Ti based electrode film 57 is formed only on the opening and a part of the upper portion of the field insulating film 5 at the peripheral portion thereof. The remaining portion of the Al—Ti based electrode film 17 is removed.

[0174]

(G) Thereafter, the SiC substrate 1 was subjected to a short-time treatment in a non-oxidizing atmosphere of 700 ° C. to 1050 ° C., exactly as in the method of FIG. 14 (f) and subsequent steps described in the third embodiment. A heat treatment is performed for a time (about several minutes), the Al—Ti based electrode film 57 and the p-type SiC region 32 react with each other, and the heated reaction layer 8 is formed in the interface region between the two. The description of the subsequent steps will be omitted because it overlaps with the description of the third embodiment.

[0175]

Using the method shown in FIGS. 16 and 17, it is possible to achieve a practical contact resistance ρc of 10^{-6} Ωcm 2 or less.

[0176]

In the above, the semiconductor electronic devices such as power devices have been mainly described, but the present invention is applicable to semiconductor light emitting devices such as light emitting diodes and semiconductor lasers, and optical integrated circuits using the same. Of course.

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[0177]

As described above, it goes without saying that the present invention includes various embodiments and the like not described here.

Therefore, the technical scope of the present invention is defined only by the matters specifying the invention according to the scope of claims reasonable from the above description.

[0178]
Brief description of the drawings

[0179]
<Figure 1> It is the principal part cross section diagram which shows the constitution of the ohmic electrode structure which relates to the form of 1st execution of this invention.

[0180]
2 is a diagram showing the results of analyzing the composition in the depth direction of the ohmic electrode structure according to the first embodiment of the present invention using the Auger electron spectroscopy (AES) method.

[0181]
<Figure 3> It is the process cross section diagram (1) which shows the manufacturing process of the ohmic electrode structure which relates to the form of 1st execution of this invention.

[0182]
<Figure 4> Process step drawing which shows the manufacturing process of the ohmic electrode structure which relates to the form of 1st execution of this invention (the 2).

[0183]
5 is a process cross-sectional view (3) showing the manufacturing process of the ohmic electrode structure according to the first embodiment of the present invention.

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[0184]
6 is a diagram showing the current-voltage characteristics of the TLM contact group based on the ohmic electrode structure according to the first embodiment of the present invention.

[0185]
7 is a diagram showing TLM characteristics of the TLM contact group based on the ohmic electrode structure according to the first embodiment of the present invention.

[0186]
<Figure 8> It is the principal part cross section diagram which shows the constitution of the ohmic electrode structure which relates to the 2nd execution form of this invention.

[0187]
9 is a process sectional view (1) showing a manufacturing process of the ohmic electrode structure according to the second embodiment of the present invention.

[0188]
10 is a process cross-sectional view (No. 2) showing a manufacturing process of the ohmic electrode structure according to the second embodiment of the present invention.

[0189]
11 is a process cross-sectional view (3) showing a manufacturing process of the ohmic electrode structure according to the second embodiment of the present invention.

[0190]
<Figure 12> It is the principal part cross section diagram which shows the constitution of the ohmic electrode structure which relates to the 3rd execution form of this invention.

[0191]
13 is a process cross-sectional view (1) showing a manufacturing process of the ohmic electrode structure according to the third embodiment of the present invention.

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[0192]
14 is a process sectional view (2) showing a manufacturing process of the ohmic electrode structure according to the third embodiment of the present invention.

[0193]
15 is a process cross-sectional view showing a manufacturing process of the ohmic electrode structure according to another embodiment of the present invention.

[0194]
<Figure 16> Process sectional drawing which shows the manufacturing process of the ohmic electrode structure which relates to the other execution form of this invention (part 1).

[0195]
17 is a process cross-sectional view (No. 2) showing a manufacturing process of the ohmic electrode structure according to still another embodiment of the present invention.

[0196]
Explanation of symbols

[0197]
1 SiC substrate 12, 32 p-type SiC region 3 thermal oxide film 4 upper insulating film 5 field insulating film 6 field insulating film opening 7,47 electrode film 8 heating reaction layer 89 wiring conductor element 17, 27, 57 Al- Ti-based electrode film 19 Al film 20 Epitaxial growth layer 21 Etching masks 22, 23, 34 Photoresist 33 Ion implantation mask 35 Ion implantation through film 44 Oxygen permeable insulating film

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CLAIMS JP2002075909

1.
A silicon carbide (SiC) substrate, a p-type SiC region selectively formed on the surface of the SiC substrate, a part of the surface of the p-type SiC region, and a surface of the p-type SiC region A thermal reaction layer formed so as to project upward from the thermal reaction layer, and a thermal oxide film having a first opening through which the thermal reaction layer penetrates and disposed in contact with the surfaces of the SiC substrate and the p-type SiC region. An upper insulating film which is an insulating film having a composition or density different from that of the thermal oxide film, which has a second opening continuous with the first opening, and which is arranged on the surface of the thermal oxide film. And an electrode film made of a metal containing at least one of Al and Ti, which is disposed on the heating reaction layer in the second opening of the upper insulating film. .

2.
The electrode film is a laminated film composed of a lower titanium-silicon (Ti-Si) alloy film and an upper titanium (Ti) film, a lower aluminum-silicon (Al-Si) alloy film and an upper aluminum (Al) film. At least one of a group consisting of a laminated film made of a film and a laminated film made of an aluminum-titanium-silicon (Al-Ti-Si) alloy film at the bottom and an aluminum-titanium (Al-Ti) alloy film at the top. The ohmic electrode structure according to claim 1, which is a metal film including two stacked films.

3.
The ohmic electrode structure according to claim 1, wherein the heated reaction layer is a solid solution containing metal carbide and metal silicon (Si).

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4.

4. The ohmic electrode structure according to claim 1, wherein the dielectric breakdown electric field strength of the upper insulating film is lower than the dielectric breakdown electric field strength of the thermal oxide film.

5.

5. The ohmic electrode structure according to claim 1, wherein an etching rate of the upper insulating film with the buffer hydrofluoric acid solution is higher than an etching rate of the thermal oxide film with the buffer hydrofluoric acid solution. body.

6.

The ohmic electrode structure according to claim 1, wherein the surface carrier density of the p-type SiC region is 1 × 10 18 / cm 3 to 5 × 10 21 / cm 3.

7.

The ohmic electrode structure according to claim 1, wherein the thermal oxide film has a thickness of 2 to 50 nm.

8.

The ohmic electrode structure according to claim 1, wherein a total value of the thickness of the thermal oxide film and the thickness of the upper insulating film is 100 nm to 3 μm.

9.

The ohmic electrode structure according to any one of claims 1 to 8, wherein a position of an uppermost portion of the electrode film is present inside the second opening.

10.

A step of forming a p-type SiC region having a high impurity density on at least a part of a surface of a silicon carbide (SiC) substrate, a step of cleaning the surface of the SiC substrate, and a field insulating film on the surface of the SiC substrate. A step of covering, a step of forming an opening in the field insulating film so as to expose at least a part of the p-type SiC region, and a step of disposing an Al-Ti based electrode film inside the opening. And in the non-oxidizing atmosphere in which the partial pressures of oxygen (O2) and water (H2O) are both 1 × 10 −3

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Pa to 1 × 10 −10 Pa, the SiC substrate is heat treated to form the Al—Ti based electrode film. And a step of forming a heated reaction layer with the SiC substrate, the method for manufacturing an ohmic electrode structure.

11.

The step of covering with the field insulating film includes a step of growing a thermal oxide film on the surface of the SiC substrate by thermal oxidation, and an insulating film is deposited on the thermal oxide film by a method other than thermal oxidation. The method for manufacturing an ohmic electrode structure according to claim 10, comprising the steps of:

12.

In the step of covering with the field insulating film, a step other than thermal oxidation is used to deposit an oxygen permeable insulating film on the surface of the SiC substrate, and after the oxygen permeable insulating film is deposited, thermal oxidation The method of manufacturing an ohmic electrode structure according to claim 10, comprising a step of growing a thermal oxide film on an interface between the surface of the SiC substrate and the oxygen-permeable insulating film.

13.

A step of forming a p-type SiC region having a high impurity density on at least a part of a surface of a silicon carbide (SiC) substrate, a step of cleaning the surface of the SiC substrate, and a method other than thermal oxidation for the SiC substrate. A step of depositing an oxygen permeable insulating film on the surface of the substrate, a step of forming an opening in the oxygen permeable insulating film so as to selectively expose a portion of the p-type SiC region, and the opening. After the step of forming, a step of growing a thermal oxide film on the surface of the SiC substrate exposed in the opening by thermal oxidation and on the interface between the surface of the SiC substrate and the oxygen-permeable insulating film, and the opening. Removing the thermal oxide film grown on the inner surface, disposing an aluminum-titanium (Al-Ti) based electrode film inside the opening from which the thermal oxide film has been removed, and non-oxidizing property. A method of manufacturing an ohmic electrode structure, comprising: a step of heat-treating the SiC substrate in an atmosphere to generate a heated reaction layer of the Al-Ti based electrode film and the SiC substrate.

14.

10. The method for producing a heated reaction layer is performed in an atmosphere in which the partial pressures of oxygen (O2) and water (H2O) are both 1 × 10 −3 Pa to 1 × 10 −10 Pa. Item 14. A method for manufacturing an ohmic electrode structure according to item 13.

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15.

The step of disposing the Al--Ti system electrode film includes the steps of depositing a titanium (Ti) layer on an aluminum (Al) layer, depositing an Al layer on a Ti layer, and aluminum-titanium (Al) layer. The method for manufacturing an ohmic electrode structure according to any one of claims 10 to 14, comprising at least one step selected from the group consisting of the step of depositing a -Ti) alloy film.

16.

The step of forming the opening may include a step of forming an etching mask on the field insulating film by a photolithography method, and the step of forming the opening on at least a part of the p-type SiC region using the etching mask. A step of removing part of the field insulating film by dry etching so that the field insulating film remains; and a step of removing the remaining field insulating film by wet etching to remove at least part of the p-type SiC region. The manufacturing of an ohmic electrode structure according to any one of claims 10 to 12, comprising a step of exposing and a step of cleaning the exposed p-type SiC region with a rinse with ultrapure water. Method.

17.

In the step of disposing the Al-Ti based electrode film, the Al-Ti based electrode film is formed on the upper portion of the etching mask and the opening while the etching mask remains on the upper portion of the field insulating film. Including the step of depositing on the entire surface including the above, and the step of selectively leaving the Al—Ti based electrode film only inside the opening by removing the etching mask after the step of depositing on the entire surface. The method for manufacturing an ohmic electrode structure according to claim 16, wherein.

18.

The step of forming the opening includes a step of forming an etching mask on the oxygen permeable insulating film by a photolithography method, and an upper portion of at least a part of the p-type SiC region using the etching mask. A step of removing a part of the oxygen permeable insulating film so that the oxygen permeable insulating film remains on the p-type SiC region. 15. The method for manufacturing an ohmic electrode structure according to claim 13 or 14, comprising a step of exposing at least a part and a step of cleaning the exposed p-type SiC region by rinsing with ultrapure water. .

19.

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A silicon carbide (SiC) substrate, a p-type SiC region functioning as a main electrode region selectively formed on the surface of the SiC substrate, and a part of the surface of the p-type SiC region that penetrates into the interior and The heating reaction layer is formed so as to project upward from the surface of the p-type SiC region, and the first opening through which the heating reaction layer penetrates, and is in contact with the surfaces of the SiC substrate and the p-type SiC region. The disposed thermal oxide film is an insulating film having a composition or density different from that of the thermal oxide film, has a second opening continuous with the first opening, and has a surface of the thermal oxide film. An upper insulating film disposed in the upper insulating film, an electrode film made of a metal containing at least one of Al and Ti disposed above the heating reaction layer in the second opening of the upper insulating film, and the electrode film. A semiconductor device comprising: a main electrode wiring connected to the.

20.

The electrode film is a laminated film composed of a lower titanium-silicon (Ti-Si) alloy film and an upper titanium (Ti) film, a lower aluminum-silicon (Al-Si) alloy film and an upper aluminum (Al) film.) Film, and at least a group consisting of a laminated film composed of a lower aluminum-titanium-silicon (Al-Ti-Si) alloy film and an upper aluminum-titanium (Al-Ti) alloy film. 20. The semiconductor device according to claim 19, which is a metal film including one laminated film.

21.

21. The semiconductor device according to claim 19, wherein the heated reaction layer is a solid solution containing metal carbide and metal silicon (Si).

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⑤4発明の名称　半導体装置およびその製造方法

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⑦2発明者　清水　俊行　東京都港区芝5丁目33番1号　日本電気株式会社内
⑦1出願人　日本電気株式会社　東京都港区芝5丁目7番1号
⑦4代理人　弁理士　内原　晋

明　細　書

発明の名称

半導体装置およびその製造方法

特許請求の範囲

1．半導体基板上に設けられた層間絶縁膜と、この層間絶縁膜に設けられたコンタクト穴と、このコンタクト穴の側壁面に設けられた導体膜または半導体膜と、導体膜または半導体膜が設けられた前記コンタクト穴内に埋設された高融点金属層とを含むことを特徴とする半導体装置。

2．半導体基板上に層間絶縁膜を形成する工程と、前記層間絶縁膜にコンタクト穴を形成する工程と、このコンタクト穴の側壁面を覆う導体膜または半導体膜を形成する工程と、側壁面に導体膜または半導体膜が形成された前記コンタクト穴に高融点金属層を埋設する工程とを含むことを特徴とする半導体装置の製造方法．

発明の詳細な説明

〔産業上の利用分野〕

本発明は半導体装置およびその製造方法に関し、特に配線等の導体層を低抵抗で接続するコンタクト穴内の電極およびその形成方法に関する．

〔従来の技術〕

半導体基板、特にシリコン基板上に形成される集積回路は高密度化、高集積化の一途を辿り、特にＭＯＳ型スタティックメモリ装置では集積度が１Ｍビットから４Ｍビットへと進もうとしている。この様な装置の高集積化においては、チップのコストと歩留りの観点から、一素子当りの占有面積を低減することが最も有効な方法である．

ＭＯＳ型スタティックメモリにおける１ＭビットＲＡＭでは、１セル当たりの占有面積が４０〜５０μm^2であったのに対し、４ＭビットＲＡＭでは１５〜２５μm^2であることが要請される．

１セル当たりの占有面積の低減に伴い、配線層と配線層を電気的につなぐコンタクト穴の占有面積も小さくすることが必要であり、このコンタク

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ト穴の微細化に伴いコンタクト抵抗の上昇が問題となる。即ち、メモリ装置の様な集積回路装置では、高集積化と共に高速度化が要求され、動作速度には各種容量成分と共に、配線及びコンタクト抵抗の上昇が大きく悪影響を及ぼすからである。従ってコンタクト穴は微細になってもコンタクト抵抗は低いことが要求される。

高速化が要求される一方、低消費電力であることも要求されるので、半導体集積回路ではＣＭＯＳ化が一段と進みつつある。従ってＣＭＯＳ化に対応する工程の少ない導体層間の接続方法も同時に要求されるところである。

これらの二者の要請を同時に満たす導体層間の接続方法として第３図に示す様に、選択的にコンタクト穴内に接続用の電極として高融点金属を埋設する技術が検討されている。

即ち、シリコン基板１に形成されたＮ型拡散層２と上部のアルミニウム配線８とを接続するために層間絶縁膜３にコンタクト穴４を開口し、タングステン７等の金属を、シリコン基板又は、配線層上のみに選択的に成長する化学気相成長技術を用い、コンタクト穴４内のみに選択的に埋設する方法である。

この方法は、低抵抗で導体層間を接続できるばかりでなく、層間の平坦化も同時に行なえるので、微細化，高密度化，高集積化する集積回路の導体層間の接続技術として極めて有効である。

又ＣＭＯＳ型集積回路においても、Ｎ型およびＰ型の不純物拡散層も同じ工程で接続することも可能になるため、工程を減少させることができ、コストの低減、歩留りの向上の点でも極めて有効な手段である。

〔発明が解決しようとする課題〕

しかし、上述した従来の高融点金属を埋設する導体層間の接続方法では、コンタクト穴側壁の絶縁膜と高融点金属の接着性が悪く、コンタクト穴に接続用の電極として埋設した高融点金属がはがれて抜けてしまい、良好な導体層間の接続が損なわれてしまうという問題があった。

この原因は特にコンタクト穴内壁の二酸化ケイ素と埋設した金属との間に化合物が生成しないことが主な原因であると思われる。例えばタングステンと二酸化ケイ素の熱膨張係数は、タングステンでは４．５×１０$^{-6}$Ｔ$^{-1}$であるのに対し、二酸化ケイ素では０．４×１０$^{-6}$Ｔ$^{-1}$であるので、化学結合の弱いこれら物質間では熱工程を加えることにより更にはがれやすくなるという問題点もあった。

本発明の目的は、この様なコンタクト穴内に埋設した高融点金属のはがれや抜け落ちることを防止した信頼性および歩留りの高い半導体装置の製造方法を提供することにある。

〔課題を解決するための手段〕

本発明の半導体装置は、半導体基板上に設けられた層間絶縁膜と、この層間絶縁膜に設けられたコンタクト穴と、このコンタクト穴の側壁面に設けられた導体膜または半導体膜と、導体膜または半導体膜が設けられた前記コンタクト穴内に埋設された高融点金属層とを含んで構成される。

また本発明の半導体装置の製造方法は、半導体基板上に層間絶縁膜を形成する工程と、前記層間絶縁膜にコンタクト穴を形成する工程と、このコンタクト穴の側壁面を覆う導体膜または半導体膜を形成する工程と、側壁面に導体膜または半導体膜が形成された前記コンタクト穴に高融点金属層を埋設する工程とを含んで構成される。

〔実施例〕

次に、本発明について図面を参照して説明する。

第１図（ａ）～（ｅ）は本発明の第１の実施例を説明するための工程順に示した半導体チップの断面図である。

まず、第１図（ａ）に示すように、半導体基板１上にＮ型拡散層２を形成したのち全面にＳｉＯからなる層間絶縁膜３を形成する。次に衆知のリソグラフィー工程と反応性イオンエッチング法等により、Ｎ型拡散層２上の層間絶縁膜３にコンタクト穴４を形成する。

次に第１図（ｂ）に示すように、コンタクト穴４の側壁面を覆うポリシリコン膜５を形成する。

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形成する物質は、層間絶縁膜と密着性の良いものであればよく、タングステンシリサイドを用いても良い。

ポリシリコン膜5の形成方法はスパッタリング方を用いても良いし化学気相成長法等を用いても良い。膜厚はコンタクト穴4を埋設しない100～2000Å程度形成する。このポリシリコン膜5には、イオン注入や拡散等の方法により不純物をドープしておいても良い。次に、ポリシリコン膜5をエッチバックし、層間絶縁膜3上のポリシリコン膜5を除去し、コンタクト穴4の側壁面のにのみポリシリコン膜5を残す。

次に第1図（c）に示すように、イオン注入法又は拡散法によりコンタクト穴4の底部に高濃度不純物を導入しN⁺型拡散層6を形成する。不純物の濃度は10^{20}～$8\times10^{21}cm^{-3}$程度が望ましい。不純物濃度が高い程、コンタクト穴内に形成する高融点金属とシリコン基板上に形成されるN⁺型拡散層6のショットキー障壁による抵抗が低下するからである。

N⁺型拡散層の濃度が$10^{21}cm^{-3}$以上であれば接触抵抗は$10^{-7}\Omega\cdot cm^2$以下にできる。この際コンタクト穴4の側壁面に形成されているポリシリコン膜5にも不純物がドープされるのが望ましい。

次に第1図（d）に示すように、化学気相成長法によりコンタクト穴4内に電極として高融点金属であるタングステン層7を選択的に成長し、コンタクト穴4を埋設する。コンタクト穴4内はポリシリコン膜5及びシリコン基板1の単結晶シリコンが露出しているので、タングステン層7はコンタクト穴4内で全てシリコンと接しており、層間絶縁膜3と接触するよりも接着強度が強くなりかつ、抵抗も低減される。

次に第1図（e）に示すように、上部配線としてアルミニウム配線8を形成する。

このように第1の実施例によれば、タングステン層7からなる電極はポリシリコン膜5を介して層間絶縁膜3と良好に接着されているため、はがれて抜けることはなくなる。

第2図（a）～（e）は本発明の第2の実施例を説明するための半導体チップの断面図である。

まず第2図（a）に示すように、半導体基板1上にN型拡散層2を形成し、次でPt又はTi等の金属を形成したのち熱処理を加えて自己整合的にN型拡散層2上に金属シリサイド層9を形成する。

N型拡散層2は、金属シリサイド層9を形成した後に金属シリサイド層9中に不純物をイオン注入等の方法で導入し、高不純物濃度となった金属シリサイド層9から熱処理によりシリコン基板1に不純物を拡散させ、N型拡散層2を形成しても良い。

次に第2図（b）に示すように、第1の実施例と同様に操作し、コンタクト穴4の側壁面にポリシリコン膜5を形成する。

ポリシリコン膜の反応性イオンエッチングにCF_4等のガスを用いた場合のエッチング速度は、金属シリサイドの3～10倍であるので、コンタクト穴4の側壁面にポリシリコン膜5を残す工程に於いて、コンタクト穴4底部の金属シリサイド層9を残すことが出来るため、コンタクト内部では金属シリサイド層9と高融点金属の接触となり、第1の実施例よりも更に抵抗が低下し、1／20～1／5程度に抵抗値が下がる利点もある。

次に第2図（c）に示すように、イオン注入法等により金属シリサイド層9中にN型不純物をドープする。濃度は10^{20}～$10^{22}cm^{-3}$あれば良い次で熱処理を行ない金属シリサイド層9からシリコン基板へ不純物を拡散させ、N⁺型拡散層6を形成する。この工程は前記ポリシリコン膜5のエッチバックの際、十分に金属シリサイド層9が残存していれば省いてもよい。

次に第2図（d）に示すように、コンタクト穴4内に電極としての高融点金属を選択的に成長させる。高融点金属としてはタングステン層7を用いる。

次に第2図（e）に示すように、上部配線としてアルミニウム配線8を形成する。

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尚、上記実施例においては拡散層と配線層とをタングステン層からなる電極を用いて接続する場合について説明したが、これに限定されるものではなく、拡散層間または配線層間の接続であってもよい。また、高融点金属としてタングステンを用いたが、モリブデン等他の金属であってもよい。

〔発明の効果〕

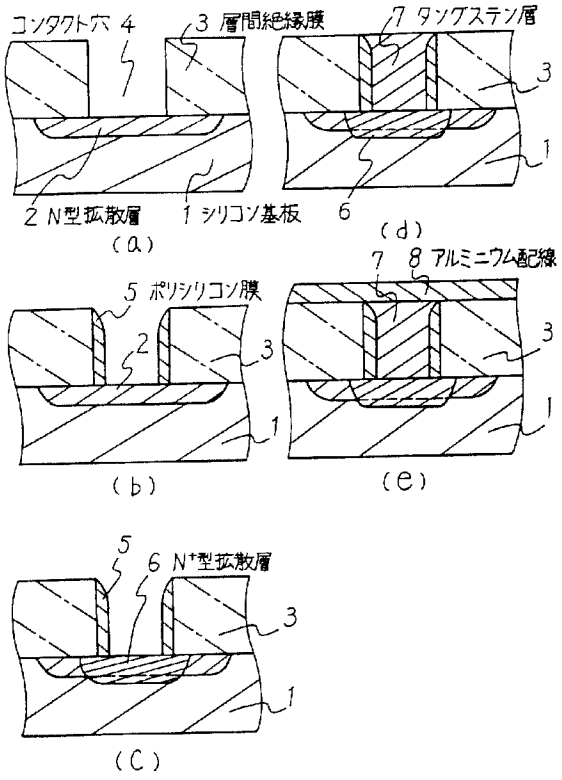
以上説明したように本発明は、コンタクト穴の側壁面に、埋没する高融点金属と接着強度の強い導体膜または半導体膜を形成することにより、信頼性および歩留りの高い半導体装置が得られるという効果がある。

図面の簡単な説明

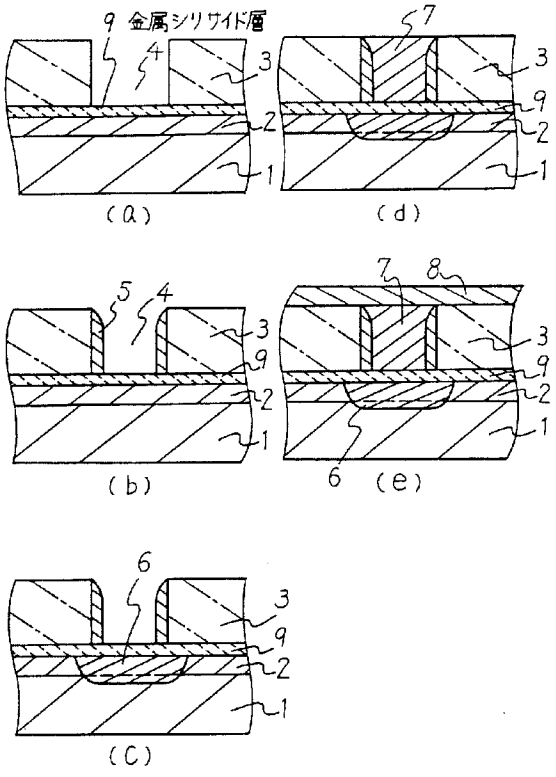
第1図及び第2図は本発明の第1及び第2の実施例を説明するための半導体チップの断面図、第3図は従来例を説明するための半導体チップの断面図である。

1…シリコン基板、2…N型拡散層、3…層間絶縁膜、4…コンタクト穴、5…ポリシリコン膜、6…N^+型拡散層、7…タングステン層、8…アルミニウム配線、9…金属シリサイド層。

代理人　弁理士　内原　晋

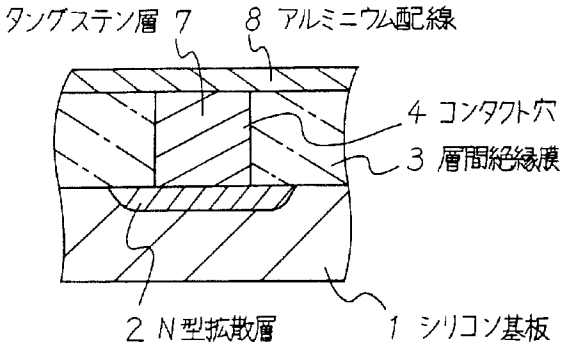


第1図



第2図

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第3図

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JPH03191518A SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

Applicants: NEC CORP

Inventors: SHIMIZU TOSHIYUKI

Classifications:
IPC ***H01L21/28; H01L21/3205; H01L21/768;*** (IPC1-7): H01L21/28; H01L21/3205; H01L21/90;

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SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

Abstract

PURPOSE:To prevent a high melting point metal buried in a contact hole from being released to fall off by a method wherein the high melting point metal layer is buried in the contact hole on whose sidewall a conductor film or a semiconductor film is formed. CONSTITUTION:An interlayer insulating film 3 is formed on a semiconductor substrate 1 and then a contact hole 4 is made in the interlayer insulating film 3. A conductor film or a semiconductor film covering the sidewall of the contact hole 4 is formed and then a tungsten layer 7 as a high melting point metal to be an electrode is selectively deposited by chemical vapor deposition process in the contact hole 4 so as to be buried therein. At this time, since the contact hole 4 is exposed to the single crystal silicon of the polysilicon film 5 and the silicon substrate 1, the tungsten layer 7 is entirely in contact with the silicon in the contact hole 4 so that the bonding strength may be increased while lowering the resistance in comparison with the contact with the interlayer insulating film 3. Through these procedures, a high melting point metal buried in the contact hole 4 as a connecting electrode can be prevented from being released to fall off.

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DESCRIPTION JPH03191518

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device and a method for manufacturing the same, and more particularly to an electrode in a contact hole for connecting conductor layers such as wiring with low resistance and a method for forming the same. [Prior Art] The density of integrated circuits formed on a semiconductor substrate, particularly a silicon substrate, is becoming higher and higher, and especially, the integration degree of MO9 type sub-type tattoo memory device is changed from 1 Mbit to 4 Mbit. Trying to proceed! ／X ろ。 In high integration of such a device, the most effective method is to reduce the occupied area per element from the viewpoint of the cost and yield of the chip yl. The occupied area per cell is 40 to 50 μm 2 in the 1M Bi 7) RAM in the MO3 type static memory, while it is required to be 15 to 25 μm 2 in the 4M and y) RAM. With the reduction of the occupied area per cell), it is necessary to reduce the occupied area of the contact hole that electrically connects the wiring layer and the wiring layer, and the contact resistance increases with the miniaturization of the contact 6. It becomes a problem. That is, in an integrated circuit device such as a memory device, higher integration and higher speed are required, and the operating speed is greatly adversely affected by various capacitance components and increases in wiring and contact resistance. Therefore, the contact resistance is required to be low even if the contact hole becomes fine. While high speed is required and low power consumption is also required, CMO8 is being further promoted in semiconductor integrated circuits. Therefore, a method for connecting between conductor layers, which has a small number of steps corresponding to CMO3 conversion, is being demanded at the same time. As a method of connecting conductor layers that simultaneously satisfy the requirements of these three parties, as shown in FIG. 3, a technique of selectively burying a refractory metal as an electrode for connection in a contact hole is being studied. That is, in order to connect the N-type diffusion layer 2 formed on the silicon substrate 1 and the upper aluminum wiring 8, a contact

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hole 4 is opened in the interlayer insulating film 3 and a metal such as tungsten 7 is added to the silicon substrate or the wiring. This is a method of selectively burying only in the contact hole 4 by using a chemical vapor deposition technique that selectively grows only on the layer. This method is not only capable of connecting conductor layers with low resistance but also planarizing the layers at the same time, which is extremely effective as a technique for connecting conductor layers of an integrated circuit that is miniaturized, densified, and highly integrated. . Also in the CMO3 type O3 circuit, since it is possible to connect the N type and P type impurity diffusion layers in the same step, the number of steps can be reduced, which is extremely effective in terms of cost reduction and yield improvement. It is a means.

[Problems to be Solved by the Invention] However, in the above-described conventional method for connecting the conductor layers in which the refractory metal is buried, the adhesiveness between the insulating film on the sidewall of the contact hole and the refractory metal is poor, and the connection to the contact hole There has been a problem that the refractory metal embedded as an electrode is peeled off and is removed, and a good connection between conductor layers is impaired. The main cause seems to be that no compound is formed between the silicon dioxide on the inner wall of the contact hole and the buried metal. For example, the coefficient of thermal expansion of tungsten and silicon dioxide is 4, 5 x 10-6T-1 for tungsten, whereas it is 0, 4 x 10-6T-1 for silicon dioxide, so these substances with weak chemical bonds In the meantime, there is a problem that the peeling is further facilitated by adding a heat step. An object of the present invention is to provide a method of manufacturing a semiconductor device having high reliability and high yield, which prevents the high melting point metal embedded in such a contact hole from peeling off or falling off. [Means for Solving the Problem] A semiconductor device of the present invention is provided with an interlayer insulating film provided on a semiconductor substrate, a contact hole provided in the interlayer insulating film, and a sidewall surface of the contact hole. It is configured to include a conductor film or a semiconductor film, and a refractory metal layer embedded in the contact hole provided with the conductor film or the semiconductor film. A method of manufacturing a semiconductor device according to the present invention includes a step of forming an interlayer insulating film on a semiconductor substrate, a step of forming a contact hole in the interlayer insulating film, and a conductor film or a semiconductor film covering a side wall surface of the contact hole. And a step of burying a refractory metal layer in the contact hole in which the conductor film or the semiconductor film is formed on the side wall surface. EXAMPLES Next, the present invention will be described with reference to the drawings. 1A to 1E are cross-sectional views of a semiconductor chip shown in the order of steps for explaining a first embodiment of the present invention. First, as shown in FIG. 1A, an N-type diffusion layer 2 is formed on a semiconductor substrate 1, and then an interlayer insulating film 3 made of SiO 2 is formed on the entire surface. Next, a contact hole 4 is formed in the interlayer insulating film 3 on the N-type diffusion layer 2 by a well-known lithography process and a reactive ion etching method. Next, as shown in FIG. 1B, a polysilicon film 5 covering the side wall surface of the contact hole 4 is formed. Any

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material may be used as long as it has good adhesion to the interlayer insulating film, and tungsten silicide may be used. As a method for forming the polysilicon M5, a sputtering method or a chemical vapor deposition method may be used.

The film thickness is about 100 to 2000 people without burying the contact holes 4. The polysilicon film 5 may be doped with impurities by a method such as ion implantation or diffusion. Next, the polysilicon film 5 is etched back, the polysilicon film 5 on the interlayer insulating film 3 is removed, and the polysilicon film 5 is left only on the side wall surface of the contact hole 4. Next, as shown in FIG. 1C, a high-concentration impurity is introduced into the bottom of the contact hole 4 by an ion implantation method or a diffusion method to form an N + type diffusion layer 6. It is desirable that the concentration of impurities is approximately 1024 to 8 x 1.021011-3. This is because the higher the impurity concentration, the lower the resistance due to the Schottky barrier of the refractory metal formed in the contact hole and the N "type diffusion layer 6 formed on the silicon substrate. If the N + type diffusion layer concentration is 1021 cm 4 or more, the contact resistance can be 10 −7 Ω · cT 112 or less. At this time, it is desirable that the polysilicon film 5 formed on the side wall surface of the contact hole 4 is also doped with impurities. Next, as shown in FIG. 1 (d), a tungsten layer 7 which is a refractory metal as an electrode is selectively grown in the contact hole 4 by chemical vapor deposition to fill the contact hole 4. Since the polysilicon film 5 and the single-crystal silicon of the silicon substrate 1 are exposed in the contact hole 4, the tungsten layer 7 is entirely in contact with the silicon in the contact hole 4 and is more bonded than the interlayer insulating film 3. The strength is increased and the resistance is reduced. Next, as shown in FIG. 1E, an aluminum wiring 8 is formed as an upper wiring. As described above, according to the first embodiment, since the electrode made of the tungsten layer 7 is well adhered to the interlayer insulating film 3 via the polysilicon film 5, it does not peel off. FIGS. 2A to 2E are sectional views of a semiconductor chip for explaining the second embodiment of the present invention. First, as shown in FIG. 2 (a), an N type diffusion layer 2 is formed on a semiconductor substrate 1, and then a metal such as pt or 1 i is formed, and then heat treatment is performed to self-align the N type. A metal silicide layer 9 is formed on the diffusion layer 2. In the N-type diffusion layer 2, after the metal silicide layer 9 is formed, impurities are introduced into the metal silicide layer 9 by a method such as ion implantation, and the silicon silicide layer 9 having a high impurity concentration is subjected to a heat treatment to remove impurities in the silicon substrate 1. May be diffused to form the N-type diffusion layer 2. Next, as shown in FIG. 2B, the same operation as in the first embodiment is performed to form the polysilicon film 5 on the side wall surface of the contact hole 4.

The etching rate when a gas such as CF4 is used for reactive ion etching of the polysilicon film is 3 to 10 times that of metal silicide, so that in the step of leaving the polysilicon film 5 on the side wall surface of the contact hole 4. Since the metal silicide layer 9 at the bottom of the contact

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hole 4 can be left, the metal silicide layer 9 is in contact with the refractory metal inside the contact, and the resistance is further reduced as compared with the first embodiment. There is also an advantage that the resistance value is lowered to some extent. Next, as shown in FIG. 2C, the metal silicide layer 9 is doped with N-type impurities by an ion implantation method or the like. Concentration is lQ20-IQ22co! Then, heat treatment is performed next to diffuse the impurities into the silicon substrate from the metal silicide layer 9 to form the N + type diffusion layer 6. This step may be omitted as long as the metal silicide layer 9 remains in the — — portion during the etching back of the polysilicon film 5. Next, as shown in FIG. 2D, a refractory metal as an electrode is selectively grown in the contact hole 4. The tungsten layer 7 is used as the refractory metal. Next, as shown in FIG. 2E, an aluminum wiring 8 is formed as an upper wiring. In the above embodiment, the case where the diffusion layer and the wiring layer are connected by using the electrode made of the tungsten layer has been described, but the present invention is not limited to this, and the connection between the diffusion layers or the wiring layers is also possible. Good. Further, although tungsten is used as the refractory metal, it may be a metal such as molybdenum. [Effects of the Invention] As described above, the present invention forms a semiconductor film having high reliability and yield by forming a conductor film or a semiconductor film having a high adhesive strength with a buried refractory metal on the side wall surface of a contact hole. There is an effect that is obtained.

[0002]
Brief description of the drawings

[0003]

1 and 2 are sectional views of a semiconductor chip for explaining the first and second embodiments of the present invention, and FIG. 3 is a sectional view of a semiconductor chip for explaining a conventional example.

l ... Silicon substrate, 2 ... N type diffusion layer, 3 ... Interlayer insulating film, 4 ... Contact hole, 5 ... Polysilicon film, 6 ... N ″ type diffusion layer 7 ... Tungsten layer, 8 ... Aluminum wiring, 9 ... Metal silicide layer.

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CLAIMS JPH03191518

1.
An interlayer insulating film provided on a plate, a contact hole provided in the interlayer insulating film, a conductor film or a semiconductor film provided on a side wall surface of the contact hole, and a conductor film or a semiconductor film provided with the contact hole. A semiconductor device comprising a refractory metal layer embedded in a contact hole. 2. A step of forming an interlayer insulating film on a semiconductor substrate, a step of forming a contact hole in the interlayer insulating film, a step of forming a conductor film or a semiconductor film covering a sidewall surface of the contact hole, and a sidewall surface. Embedding a refractory metal layer in the contact hole in which a conductor film or a semiconductor film is formed.

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21/90	A	7353－4M	
		7353－4M　H 01 L 21/88	K

審査請求　未請求　請求項の数 1　（全4頁）

⑭発明の名称　半導体装置の製造方法

⑳特　願　平2－331714
㉒出　願　平2(1990)11月29日

㉗発明者　江口　芳和　長野県諏訪市大和3丁目3番5号　セイコーエプソン株式会社内
㉑出願人　セイコーエプソン株式会社　東京都新宿区西新宿2丁目4番1号
㉔代理人　弁理士　鈴木　喜三郎　外1名

明細書

1．発明の名称

半導体装置の製造方法

2．特許請求の範囲

半導体基板の上方に層間絶縁膜を形成する工程、

前記層間絶縁膜を窓開けしてコンタクトホールを形成する工程、

前記コンタクトホールの内面及び前記層間絶縁膜上に前記コンタクトホールの半径より大きい膜厚のタングステン層を化学気相成長法により堆積する工程、

前記タングステン層を全面エッチバックし、膜厚を５００Ａ程度にする工程、

前記タングステン層上にアルミ合金層を堆積する工程、

前記アルミ合金層の上方に、予め配線となるように設計された領域に形成されたフォトレジストをマスクとして前記アルミ合金層と、前記タングステン層をエッチングして、配線を形成する工程、よりなることを特徴とする半導体装置の製造方法。

3．発明の詳細な説明

［産業上の利用分野］

本発明は、半導体装置における配線の形成方法に関する。

［従来の技術］

従来の半導体の製造方法では、第２図に示すように、半導体基板２０１上に層間絶縁膜２０２を堆積した後、コンタクトホール２０３を開孔し、下地金属層であるチタン層２０４（１００Ａ）と窒化チタン層２０５（５００Ａ）を連続して堆積する。そして、前記コンタクトホール２０３内部と前記層間絶縁膜２０２上にタングステン層２０６を化学気相成長法により堆積する。この後、前記タングステン層２０６を全面エッチバックし、コンタクトホール２０３内部にのみタングステン層２０６を残した後、アルミ合金２０７層を堆積

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し、フォトリソ技術及び、エッチング技術により、所望のパターンにパターニングしていた。

［発明が解決しようとする課題］

しかしながら、前述の従来技術では全面エッチバックにより層間絶縁膜２０２上のタングステン層２０６を除去してしまうので、層間絶縁膜２０２とアルミ合金２０７が直接接触する領域ができ、ここでアルミ合金２０７へシリコン原子が拡散してノジュールを形成し、アルミ合金からなる配線層２０７が断線してしまうことがあった。

そこで、本発明はこの様な課題を解決するもので、その目的とするところは、層間絶縁膜上のタングステンを５００Å残すように全面エッチバックを行い、アルミ合金と層間絶縁膜とが直接接触しないようにしてアルミ合金におけるノジュール発生を抑制することにより、高信頼性を有する配線を持つ半導体装置の製造方法を提供するところにある。

［課題を解決するための手段］

本発明は、半導体基板の上方に層間絶縁膜を形成する工程、

前記層間絶縁膜を窓開けしてコンタクトホールを形成する工程、

前記コンタクトホールの内面及び前記層間絶縁膜上に、前記コンタクトホールの半径より大きい膜厚のタングステン層を化学気相成長法により堆積する工程、

前記タングステン層を全面エッチバックし、膜厚を５００Å程度にする工程、

前記タングステン層上にアルミ合金層を堆積する工程、

前記アルミ合金層の上方に、予め配線となるように設計された領域に形成されたフォトレジストをマスクとして前記アルミ合金層と、前記タングステン層をエッチングして、配線を形成する工程、よりなることを特徴とする。

［実施例］

次に本発明の実施例にかかる半導体装置の製造方法を、その工程断面図である第１図（ａ）～（ｆ）を参照して説明する。

まず、第１図に示す如く、シリコン基板１０１の表面には拡散層等の半導体領域（図示せず）が形成されており、これらの半導体領域とシリコン基板１０１の表面側に形成される電極配線層とを絶縁分離するために、シリコン基板１０１の表面上には厚さ５０００Å前後のシリコン酸化膜１０２たる層間絶縁膜が化学気相成長法により形成される。シリコン酸化膜１０２のコンタクト予定領域１０１ａに対応する部分には、エッチングによりコンタクトホール１０３が形成され、その底面でシリコン基板１０１のコンタクト予定領域１０１ａは窓開けされた状態になる。

次に、第１図（ｂ）に示す如く、コンタクトホール１０３の内面及びシリコン酸化膜１０２の表面上には、シリコン基板１０１のコンタクト予定領域１０１ａに直接接続され、そのコンタクト抵抗を低下させるためのコンタクト金属層たる厚さ１５０Åのチタン層１０４、このチタン層１０４と後述するコンタクト埋め込み層１０６との密着性を向上するため、これら２層の間に介在する密着用金属層たる厚さ５００Åの窒化チタン層１０５が順次スパッタ法により堆積される。ここで、チタン層１０４はコンタクトホール１０３の底面でコンタクト領域１０１ａと接触している。一方、窒化チタン層１０５の表面上には、第１図（ｃ）に示す如く、ウェハ全面にわたってタングステン層１０６を形成する。タングステン層１０６の膜厚は、コンタクトホール１０３の直径の半分以上となる。例えば、コンタクトホール１０３の直径が０．５μｍならば、タングステン層１０６の膜厚は少なくとも２５００Åとなる。これだけの膜厚を堆積すれば、コンタクトホール１０３の内部はタングステン層１０６で充満される。又、タングステン層１０６の下は前述のＴｉＮ層１０５があるので密着性は十分確保される。

次に、第１図（ｄ）に示すごとく、タングステン層１０６を全面エッチバックし、タングステン

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層１０６のシリコン酸化膜１０２上における膜厚を５００Å程度に減少させる。このことによって、チタン層１０４、ＴｉＮ層１０５、タングステン層１０６、後述するアルミ合金層１０７からなる配線層の厚さを減少させることが可能となり、この配線層の上方に堆積する膜の被覆性が良好なものとなる。逆に、シリコン酸化膜１０２上のタングステン層１０６を全て除去せずに、５００Å程度残すことにより、タングステン層１０６をバリアメタルとして用いることができ、後述するアルミ合金層１０７中にシリコン酸化膜中のシリコン原子が拡散することによるノジュールの発生を抑制することができる。

次に、第１図（ｅ）に示すようにアルミ合金１０７を５０００Åスパッタリング法により堆積する。アルミ合金層１０７の下層はバリアメタルとなるタングステン層１０６があるため、シリコン基板１０１やシリコン１０２とアルミ合金層１０７との相互拡散は防止される。又、配線層の最終的な膜厚は約６０００Åとなり、配線の上方に堆積される膜の被覆性は、タングステン膜１０６を全くエッチバックしない場合に比べて大きく向上する。

次に第１図（ｆ）に示す如く、フォトリソ技術及びエッチング技術を用いて、チタン層１０５、ＴｉＮ層１０５、タングステン層１０６、アルミ合金層１０７を所望のパターンにパターニングする。以上で配線が完成する。

［発明の効果］

以上述べた本発明に従って形成された配線は、タングステン層によって、コンタクトホール内は充満され、十分な段差被覆性を有している。又、層間絶縁膜上にタングステン層を残すことにより、アルミ合金と層間絶縁膜との反応を抑制しており、高い信頼性を持っている。更に、タングステン層を堆積してから全面エッチバックすることにより配線層の厚さを抑えており、この配線層の上方の膜、例えばパシベーション膜などの被覆性を改良する効果も有する。

4．図面の簡単な説明

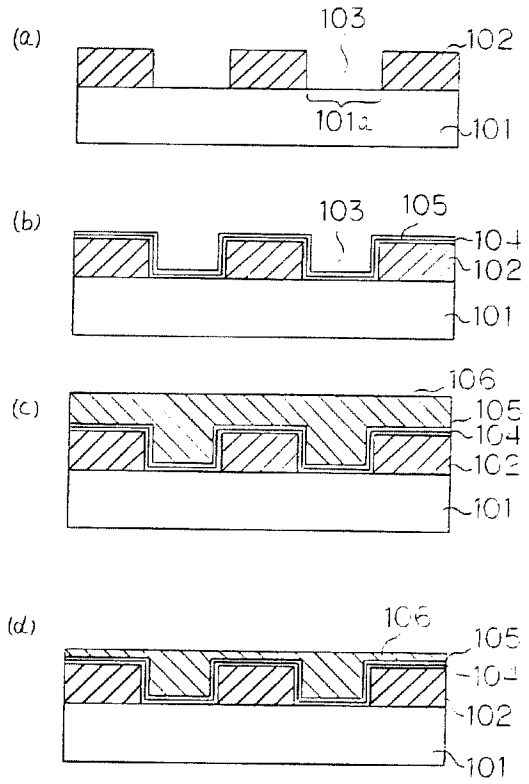
第１図（ａ）～（ｆ）は、本発明の半導体装置の製造方法を示す工程断面図。

第２図（ａ）～（ｄ）は、従来の半導体装置の製造方法を示す工程断面図。

１０１、２０１　半導体基板
１０１ａ　コンタクト予定領域
１０２、２０２　シリコン酸化膜
１０３、２０３　コンタクトホール
１０４、２０４　チタン層
１０５、２０５　窒化チタン層
１０６、２０６　タングステン層
１０７、２０７　アルミ合金層

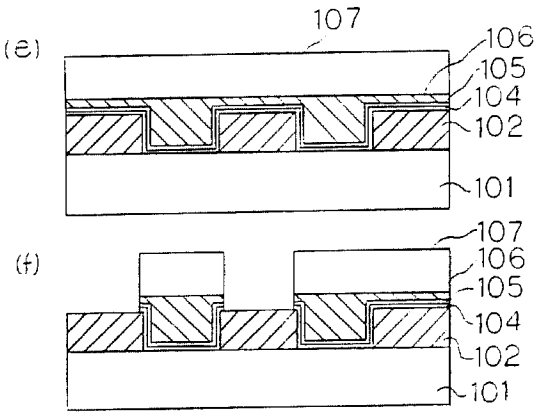
以上

出願人　セイコーエプソン株式会社
代理人　弁理士　鈴木喜三郎（他１名）

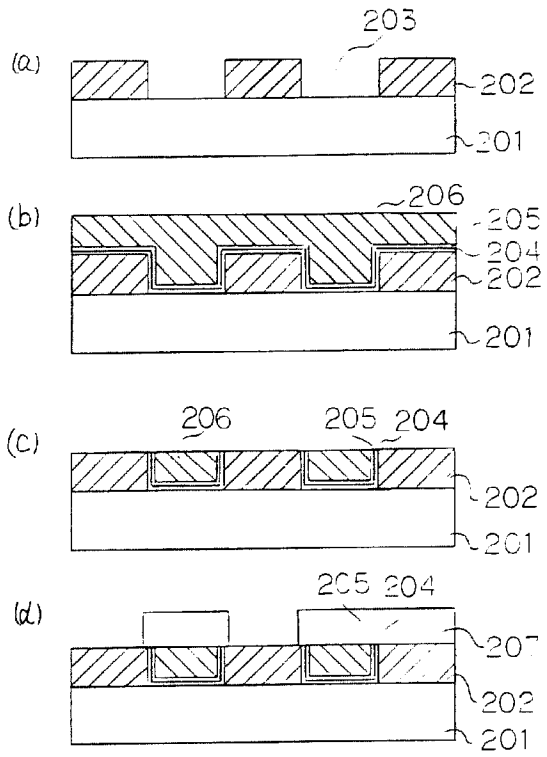


第１図

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第 1 図



第 2 図

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JPH04199628A MANUFACTURE OF SEMICONDUCTOR DEVICE

Applicants: SEIKO EPSON CORP

Inventors: EGUCHI YOSHIKAZU

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IPC ***H01L21/3205; H01L21/768;*** (IPC1-7): H01L21/3205; H01L21/90;

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MANUFACTURE OF SEMICONDUCTOR DEVICE

Abstract

PURPOSE:To enable the title semiconductor device having wirings in high reliability to be manufactured by a method wherein the whole surface of a tungsten layer on an interlayer insulating film is etched back to be left in thickness of about 500Angstrom so that an Al alloy and the layer insulating film may not be brought into direct contact with each other so as to avoid the growth of nodules in the Al alloy. CONSTITUTION:A layer insulating film to be a silicon oxide film 102 is formed on the surface of a silicon substrate 101 and then contact holes 103 are made in the film 102. Next, a titanium layer 104 and a titanium nitride layer 105 to be directly connected to a prospective contact region 101a and to lower the contact resistance are successively deposited on the inner surface of the contact holes 103 and on the surface of the silicon oxide film 102. Next, a tungsten layer 106 is formed extending over the whole wafer surface on the surface of a titanium nitride layer 105 and the whole surface of the tungsten layer 106 is etched back to reduce the film thickness to about 500Angstrom on the silicon oxide film 102. Through these procedures, the tungsten layer 106 used as a barrier metal to avoid the growth of modules thereby enabling the wirings in high reliability to be made.

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DESCRIPTION JPH04199628

[0001]

TECHNICAL FIELD The present invention relates to a method for forming wiring in a semiconductor device. [Prior Art] In a conventional semiconductor manufacturing method, as shown in FIG. 2, after an interlayer insulating film 202 is deposited on a semiconductor substrate 201, a contact hole 203 is opened to form a titanium layer as a base metal layer. 204 (100 people) and titanium nitride layer 205 (500 people) are continuously deposited. Then, a tungsten layer 206 is deposited on the inside of the contact hole 203 and on the interlayer insulating M2O2 by a chemical vapor deposition method. After that, the tungsten layer 206 is entirely etched back, leaving the tungsten layer 206 only inside the contact hole 203, and then an aluminum alloy 207 layer is deposited and patterned into a desired pattern by a photolithography technique and an etching technique. Was there. [Problems to be Solved by the Invention] However, in the above-described conventional technique, since the tungsten layer 206 on the interglossal insulating film 202 is removed by the entire surface etchback, the area where the interlayer insulating film 202 and the aluminum alloy 207 are in direct contact with each other is In some cases, however, silicon atoms diffuse into the aluminum alloy 207 to form nodules, and the wiring layer 207 made of the aluminum alloy may be broken. Therefore, the present invention solves such a problem. The purpose of the present invention is to perform an overall etch back so as to leave 500 tungsten on the glabella insulation film and to directly contact the aluminum alloy with the interlayer insulation film. Therefore, it is an object of the present invention to provide a method of manufacturing a semiconductor device having highly reliable wiring by suppressing the generation of nodules in an aluminum alloy. [Means for Solving the Problems] The present invention provides a step of forming an interlayer insulating film above a semiconductor substrate, a step of forming a contact hole by opening a window of the interlayer insulating film, an inner surface of the contact hole and the interlayer. A step of depositing a tungsten layer having a thickness larger than the radius of the contact hole on the

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insulating film by chemical vapor deposition, a step of etching back the whole tungsten layer to a thickness of about 500 Å, A step of depositing an aluminum alloy layer, above the aluminum alloy layer, by etching the aluminum alloy layer and the tungsten layer using a photoresist formed in a region designed to be wiring in advance as a mask, And a step of forming wiring. [Embodiment] Next, a method of manufacturing a semiconductor device according to an embodiment of the present invention will be described with reference to FIGS.

First, as shown in FIG. 1, semiconductor regions (not shown) such as diffusion layers are formed on the surface of the silicon substrate 101, and electrode wirings formed on these semiconductor regions and the surface side of the silicon substrate 101. In order to insulate the layers from each other, an intergrowth insulating film having a thickness of about 5,000 and covering the silicon oxide film 10 is formed on the surface of the silicon substrate 101 by a chemical vapor deposition method. A contact hole 103 is formed by etching in a portion of the silicon oxide film 102 corresponding to the contact planned region 101a, and the contact planned region 101a of the silicon substrate 101 is opened at its bottom surface. Next, as shown in FIG. 1B, the inner surface of the contact hole 103 and the surface of the silicon oxide film 102 are directly connected to the planned contact region 101a of the silicon substrate 101 to reduce the contact resistance thereof. A titanium layer 104 having a thickness of 150 contact metal layers, and a contact metal layer having a thickness of 500 persons interposed between these titanium layers 104 and a contact embedding layer 106 described later in order to improve adhesion. Titanium nitride layer 1-5 is sequentially deposited by sputtering. Here, the titanium layer 104 is in contact with the contact area m101a on the bottom surface of the contact hole 103. On the other hand, a tungsten layer 106 is formed on the entire surface of the wafer on the surface of the titanium nitride layer 105, as shown in FIG. The film thickness of the tungsten layer 106 is more than half the diameter of the contact hole 103. For example, the diameter of the contact hole 103 is 0. If the thickness is 5 μm, the film thickness of the tungsten layer 108 is at least 250 OA. By depositing such a thickness, the inside of the contact hole 103 is filled with the tungsten layer 106. Further, since the TiN layer 105 described above is provided under the tungsten layer 106, sufficient adhesion is secured. Next, as shown in FIG. 1D, the tungsten layer 106 is entirely etched back to reduce the film thickness of the tungsten layer 106 on the silicon oxide film 102 to about 500. This makes it possible to reduce the thickness of the wiring layer composed of the titanium layer 104, the TiN layer 105, the tungsten layer 106, and the aluminum alloy layer 107 described later, and the coverage of the film deposited above this wiring layer can be improved. It will be good. On the contrary, the tungsten layer 106 on the silicon oxide film 102 can be used as a barrier metal by not leaving the tungsten layer 106 on the silicon oxide film 102 and leaving about 500 octaves. The generation of nodules due to the diffusion of silicon atoms can be suppressed.

Next, as shown in FIG. 1 (e), an aluminum alloy 107 is deposited by the 500OA sputtering

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method. Since the lower layer of the aluminum alloy layer 107 has the tungsten layer 106 serving as a barrier metal, mutual diffusion between the silicon substrate 101 or silicon 102 and the aluminum alloy layer 107 is prevented. Further, the final film thickness of the wiring layer is about 6000, and the coverage of the film deposited above the wiring is tungsten 11! This is a significant improvement over the case where 106 is not etched back at all. Next, as shown in FIG. 1F, the titanium layer 105, the TiN layer 105, the tungsten layer 106, and the aluminum alloy layer 107 are patterned into a desired pattern by using a photolithography technique and an etching technique. The wiring is completed as described above. [Advantages of the Invention] In the wiring formed according to the present invention described above, the contact hole is filled with the tungsten layer and has sufficient step coverage. Further, by leaving the tungsten layer on the interlayer insulating film, the reaction between the aluminum alloy and the interlayer insulating film is suppressed, which has high reliability. Furthermore, the thickness of the wiring layer is suppressed by depositing the tungsten layer and then etching back the entire surface, which also has the effect of improving the coverage of the film above this wiring layer, such as passivation.

[0002]
Brief description of the drawings

[0003]

1A to 1F are process cross-sectional views showing a method for manufacturing a semiconductor device of the present invention.

2A to 2D are process cross-sectional views showing a conventional method for manufacturing a semiconductor device. 101.201 Semiconductor substrate 101a, planned contact area 102.202, silicon oxide film 103.203, contact hole 104.204, titanium layer 105.205, titanium nitride layer 106.206, tungsten layer 107.207, aluminum alloy layer or above Applicant Seiko Epson Corporation People Patent Attorney Kizo Suzuki (1 person) ji, No Q

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CLAIMS JPH04199628

1.

A step of forming an interlayer insulating film above, a step of forming a contact hole by opening the interlayer insulating film, and a tungsten layer having a thickness larger than a radius of the contact hole on an inner surface of the contact hole and the interlayer insulating film. By a chemical vapor deposition method, a step of etching back the tungsten layer to a thickness of about 500 Å, a step of depositing an aluminum alloy layer on the tungsten layer, and a step above the aluminum alloy layer, Manufacturing a semiconductor device, which comprises: forming a wiring by etching the aluminum alloy layer and the tungsten layer using a photoresist formed in a region designed to be a wiring as a mask. Method.

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審査請求　未請求　請求項の数 5　(全6頁)

⑤4発明の名称　ショットキー電極を有する半導体装置の製造方法

⑳特　願　平2−73338
㉒出　願　平2(1990)3月26日

⑦2発明者　渕上　伸隆　東京都小平市上水本町5丁目20番1号　日立超エル・エス・アイ・エンジニアリング株式会社内

⑦2発明者　小田　浩人　東京都小平市上水本町5丁目20番1号　日立超エル・エス・アイ・エンジニアリング株式会社内

⑦1出願人　株式会社日立製作所　東京都千代田区神田駿河台4丁目6番地

⑦1出願人　日立超エル・エス・アイ・エンジニアリング株式会社　東京都小平市上水本町5丁目20番1号

⑦4代理人　弁理士　小川　勝男　外1名

最終頁に続く

明　細　書

1．発明の名称

ショットキー電極を有する半導体装置の製造方法

2．特許請求の範囲

1．半導体基板上に高融点金属シリサイドから成る第1の層を直接形成する工程、該第1の層上に高融点金属から成る第2の層を直接または高融点金属を含む層を介して形成する工程、該第2の層上に高融点金属シリサイド、高融点金属窒化物およびシリコンから成る群から選ばれた少なくとも1種から成る第3の層を直接形成する工程、該第3の層上にレジスト膜を直接形成する工程、該レジスト膜をパターニングする工程、および該パターニングされたレジスト膜をマスクとして上記第1の層および該層上に積層された層をエッチングしてショットキー電極を形成することを特徴とするショットキー電極を有する半導体装置の製造方法。

2．上記高融点金属を含む層は、高融点金属層および高融点金属シリサイド層をこの順序に積層した層の組を少なくとも1組有している特許請求の範囲第1項記載のショットキー電極を有する半導体装置の製造方法。

3．上記ショットキー電極形成後、上記第3の層の一部または全部を除去する工程を有する特許請求の範囲第1項又は第2項記載のショットキー電極を有する半導体装置の製造方法。

4．半導体基板上に高融点金属シリサイドから成る第1の層を直接形成する工程、該第1の層上に高融点金属から成る第2の層を直接または高融点金属を含む層を介して形成する工程、該第2の層上にシリコンから成る第3の層を直接形成する工程、該第3の層上に第1のレジスト膜を直接形成する工程、該第1のレジスト膜をパターニングする工程、および該パターニングされた第1のレジスト膜をマスクとして上記第3の層をエッチングすると共に上記第3の層形成時に上記第2の層と上記第3の層の界面に形成された上記第2の層の構成材料のシリサイド層

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を露出する工程、該エッチングにより残った上記第３の層および該層に連続した部分の上記第２の層の構成材料のシリサイド層を、少なくとも一端が上記第３の層で終端するように第３のレジスト膜で被覆する工程、およびに該第２のレジスト膜をマスクとして上記第１の層および該層上に形成された層をドライエッチングしてショットキー電極形状と成す工程を有し、該ドライエッチング工程において上記第３の層で終端した部分のショットキー電極の側面はその断面の上記半導体基板側の角度が鋭角である如くに加工されたテーパ部を有することを特徴とするショットキー電極を有する半導体装置の製造方法。

５．上記ショットキー電極は電界効果トランジスタのゲート電極であり、上記ドライエッチング工程の後上記第３の層を除去する工程および上記電界効果トランジスタのゲート電極とソース電極の間が露出した状態で該両電極間に導電体膜を被着し該両電極間を電気的に接続する工程を有する特許請求の範囲第４項記載のショットキー電極を有する半導体装置の製造方法。

３．発明の詳細な説明

〔産業上の利用分野〕

本発明はショットキー電極を有する半導体装置の製造方法に関する。

〔従来の技術〕

高融点金属やその硅化物をショットキー電極として用いるＧａＡｓ　ＭＥＳＦＥＴ（Metal Semiconductor Field Effect Transistor）において、熱安定性に優れ、かつ半導体基板との密着性が良好なタングステン・シリサイド等の高融点金属シリサイドを１層目に用い、その上に金融タングステン等の高融点金属層を重ねて、ゲート抵抗を低減する技術が特開昭６１－２１４４８１号公報において知られている。

〔発明が解決しようとする課題〕

ＧａＡｓ　ＭＥＳＦＥＴのゲート電極として重ね膜ゲート（下層はＷＳｉₓ膜、上層は金属タングステン膜）を用いた場合、レジストの剥離が生じ易くゲート形成の歩留まりの低下を招く問題があった。

本発明の目的は、高融点金属をショットキーゲート電極材料として用いた場合に生じるレジストとの密着性の低下を防止することにある。

〔課題を解決するための手段〕

上記目的は、半導体基板上に高融点金属のシリサイドから成る第１の層を直接形成してショットキー接合を形成する工程、該第１の層上に高融点金属から成る第２の層を直接又は高融点金属を含む層を介して形成する工程、該第２の層上に高融点金属のシリサイド、高融点金属の窒化物及びシリコンから成る群から選ばれた少なくとも１つの材料から成る第３の層を直接形成する工程、該第３の層上にレジスト膜を直接形成する工程、該レジスト膜をパターニングする工程、及び該パターニングされたレジスト膜をマスクとして上記第１の層および該層上に形成された層をエッチングしてショットキー電極を形成することにより達成できる。

〔作用〕

本発明においては、ゲート電極の最下層（第１の層）として高融点金属シリサイドを用いるので半導体界面で良好なショットキー接合を形成することが可能となる。また、第２の層として高融点金属を用いるのでゲートの低抵抗化が可能となる。さらに、最上層としてレジストとの密着性の良い第３の層を形成するのでレジストの剥れを防止できる。

ゲート電極に配線層を接続する場合、第３の層を除去して第２の層に直接配線層を接続すると接触抵抗を低減できる。

〔実施例〕

以下、本発明を実施例により説明する。

実施例ではＧａＡｓ　ＭＥＳＦＥＴのゲート電極として用いる場合について説明するが、ＩｎＰ、ＩｎＧａＡｓ、ＩｎＡℓＡｓ等の他の化合物半導体及びシリコン等の単元素半導体に使用することが可能であり、ショットキー・ダイオード、ＩＧＦＥＴ（Insulated Gate FET）等のゲート電

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極として用いることも可能である。

実施例．1

本発明の実施例1を第1図及び第2図に従い説明する。

半絶縁性GaAs基板1に、ドナー不純物としてSi⁺イオンを打込み、アニールを行なって導電層2を形成する。その上にWSiₓ膜3を100nm、W膜4を200nm、WSiₓ膜5を10nm重ねて被着する。WSiₓ3，5の被着は焼結体のWsSi₂ターゲットをAr⁺イオンでスパッタリングすることで行い、スパッタリング中のArガスの圧力を9mtorr、パワーを直流で0.35kwとする時WSiₓ膜の組成Xは0.22、膜内応力は引張り方向に3×10⁹dyne／cm²であった。

W膜4の被着はWターゲットのスパッタリングで行い、Arガスの圧力は5mtorr、パワーは直流で0.36kwとする。この時W膜の膜内応力は、GaAs基板に対しては圧縮方向に7×10⁹dyne／cm²を示すが、実際はWSiₓ膜上に被着する為、WSiₓとの界面で応力が散逸してしまい、WSiₓ膜3とW膜4の合計の応力はGaAs基板に対してはほとんど零となる。最上層のWSiₓ膜5の応力は薄い為、ほとんど無視できる。WSiₓはWよりもホトレジストに対する密着性がよいので、最上層のWSiₓ膜5上にホトレジスト6を塗布すればレジスト剥離はほとんど起きない為、従来のW／WSiₓの2層構造のゲートの場合よりも歩留りが向上する。

ホトレジスト6のパターニングを行った後、反応性イオンエッチングでWSiₓ膜5、W膜4、WSiₓ膜3を加工して、ゲート電極を形成する。

本実施例で形成したゲート電極のシート抵抗は、約0.9Ω／□であり、単層のWSiₓゲート（約7Ω／□）の場合の約1／8である。加工後のゲート金属の断面形状を第1図に示す。

次に、ホトレジスト6を除去した後、ソースとドレインのオーミック電極を形成し（図示せず）、層間絶縁膜10を被覆し、配線11を行うことで本実施例は完成する。

配線金属（Au）11と最上層WSiₓ膜5との接触抵抗はコンタクト穴を1×1μm²の正方形とした場合で3～5Ωある。しかし、コンタクト穴の部分で最上層WSiₓ膜5を除去し、配線金属と中間層W膜4とを接触させた場合の接触抵抗は0.6～0.8Ωに低減できる為、ゲートの寄生抵抗を2～4Ω減らすことが可能となる。この場合の断面構造を第2図に示す。

実施例．2

実施例1では第3の層である最上層のWSiₓ膜5の膜厚を5～10nmに設定したが、それよりも厚くした場合についてゲート電極の断面形状を第3図に示す。最上層のWSiₓ膜5の厚さは50nmである。

CHF_3、CF_4、NF_3ガス等を用いるドライエッチ工程では、WSiₓのエッチングレートはWよりも2～4倍大きい為、中間層のW膜4をエッチングする最中に最上層のWSiₓ層5は側面からのサイドエッチが生じ、サイドエッチ部分からW層4が露出する。この結果、中間層のW膜4の断面形状は台形となる。最下層のWSiₓ膜3の加工中はエッチングガスから生成したポリマーが側面に付着する為、最上層のWSiₓ膜5に比べてエッチングが遅く、サイドエッチは僅かである。

本実施例のゲート電極は、実施例1の場合に比べゲート抵抗が若干大きくなる欠点はあるもののゲート電極に層間絶縁膜を被着した時の平坦性が向上する利点がある。

実施例．3

本発明の実施例を第4図に示す。ドライエッチ工程においてWSiₓのエッチングレートはWより大きい為、WSiₓ層とW層とを200nmずつ重ねた2層構造では下段のWSiₓ層に大きなサイドエッチが生じる。そこで、本実施例では、WSiₓ層3とW層4の厚さを各100nmとして、これを2回繰り返して4層構造とし、更に最上層に数nmの厚さのWSiₓ層5を被着する。この場合、WSiₓ層3を薄くしたので、この層のサイドエッチ量が減り、ゲート電極の断面形状

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は矩形に近づく。

実施例．4

実施例1～3では最上層5に最下層3と同じWSi_xを用いた。この理由はスパッタリングのターゲットをW_5Si_3からWに、そして再びW_5Si_3に切り換えることで最下層3、中間層4、最上層5を連続的に形成できる利点がある為である。

しかし、最上層5はWSi_xN_y、或いはWN_xを用いることも可能であり、W_5Si_3又はWのターゲットを窒化雰囲気中でスパッタリングさせることで形成できる。この場合、WSi_xN_y、WH_xはAℓ配線やゲート電極中のWに対するバリヤメタルとして作用し、コンタクト穴でのエレクトロマイグレーションを抑え、集積回路の信頼性向上と製品寿命の延長を図ることができる。

最上層5の材料には、この他$TaSi_x$、$MoSi_x$、$TiSi_x$、$IrSi_x$等の他の硅化物、或いはWN_x、TaN_x、等の窒化物、WB_6、TaB_6等の硼化物やWC、SiC、TiC等の炭化物、或いはSi等を用いることも可能である。

実施例．5

集積回路の負荷FETでは、ゲート電極とソース側のオーミック電極とを直接接続させることでセル面積を小さくすることができる。この場合、断面形状が矩形のゲート電極では側端の角の部分でオーミック電極が断線する不良が発生する。この問題を解決する方法として、ゲート電極のソース側端部となる領域のゲート電極材の最上層としてSi膜を形成し、ゲート電極形成時のドライエッチングにより上記Si膜がサイドエッチされることを利用して、ゲート電極のソース側端をテーパ状に加工することにより段差被覆性を向上させる方法が特開平1－187876号公報において知られている。

また、Siは本発明の目的も達成できるので本発明と上記従来技術を組み合せることが可能である。

実施例5として、この組合せをインバータ回路を有する集積回路に適用した例を示す。第5図はその断面図であり、第6図（a）乃至第6図（e）は負荷FET部分の製造工程図である。

半絶縁性基板1に、駆動FET、負荷FETの能動層2を形成し、DC（直流）スパッタリングでWSi_x層3、W層4を100、200nm被着し、更にRF（高周波）スパッタリングでSi層7を50nm被着する。この時、W層4とSi層7の界面にはスパッタのミキシングと拡散とによってWSi_x層5が形成される（第6図（a））。このWSi_x層5の厚さはSi層7を被着する際のRFパワーを大きくすることで1～2nmにできるが、赤外線ランプによる加熱で更に厚くすることも可能である。次に、負荷FETのゲート電極を形成する領域のうちソース側のみにSi層7を残し、他の領域のSi層7を除去する。その後、ホトレジスト6を1μm塗布し、ゲート電極のパターニングを行う（第6図(b)）。

ホトレジスト6をマスクにドライエッチングを行い、ゲート電極を加工する。この時、SiのエッチングレートはWより1桁大きい為、W層4をエッチングする間にSi層7は側面からのサイドエッチが進行する。この結果、W層4はSi層7を残した部分ではテーパ状に加工される。この時の負荷FETの断面構造を第6図（c）に示す。

本工程において、負荷FETのゲート電極では、ホトレジスト6の下面は上記のようにSi又はWSi_xに接しており、また、駆動FETのゲート電極では、ホトレジスト6の下面はWSi_xに接しているので、本工程中にホトレジスト6が剥離することはない。

次に、ホトレジスト6を除去した後、イオン打込みで高濃度導電層（n^+層）9を形成し、さらにSiO_2膜12をCVD（化学気相成長）法で約300nm被着した後800℃15分の活性化アニールでn^+層9の活性化を行う。つづいて、有機レジスト膜13を約1μm塗布した後、これをマスクとしてオーミック電極形成領域および負荷FETのゲートとソースとの配線領域のSiO_2膜12およびSi層7を除去する。次に、オーミック金属（AuGe）8を厚さ0.2μm蒸着す

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る（第６図(ｄ)）。

次に、有機レジスト膜１３およびSiO_2膜１２を除去して（ソフトオフ法）オーミック電極が形成される。この時の負荷ＦＥＴの断面構造を第６図（ｅ）に示す。ソース側のオーミック電極８はゲート電極と直接接続しており、ドレイン側に比べて占有面積は小さくできる。

この時のインバータ回路の断面図は第５図のようになっている。この後、層間絶縁膜を被着し、配線工程を行うことで積積回路は完成する（図示せず）。

〔発明の効果〕

本発明によってタングステンを用いた低抵抗のゲート電極を形成する際に生じるホトレジストの剥離がなくなり、集積回路の歩留り向上を図れる効果がある。

又、最上層に高融点金属窒化物、或いは高融点金属の硅化物と窒化物の混合体を用いることで配線金属やゲート電極中のタングステンが外方拡散するのを抑え、エレクトロマイグレーション寿命（ＥＭ寿命）を延ばす効果がある。

更に、最上層にＳｉ等のエッチング速度の大きい材料を選ぶことで、ゲート電極の側端にテーパを設けて段差被覆性を向上できる効果がある。この効果は負荷ＦＥＴでのゲート・ソース直接接続によってセル面積縮小を図った集積回路における歩留り向上に有効である。

４．図面の簡単な説明

第１図は本発明の重ねゲートを用いた実施例１のＭＥＳＦＥＴの断面図、第２図は実施例１の配線後の断面構造図、第３図は最上層のWSi_x膜を厚くした実施例２の断面構造図、第４図は４層構造の重ねゲートに本発明を適用した実施例３の断面構造図。

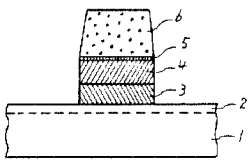
第５図は負荷ＦＥＴのソース側のオーミック電極とゲート電極とを直接接続する為に、ゲート電極のソース側をテーパ状に加工する方法について示した実施例５の断面構造図、第６図（ａ）乃至第６図（ｅ）は実施例５の負荷ＦＥＴの部分のプロセス工程図である。

符号の説明

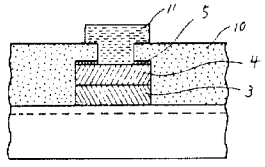
１…半絶縁性基板、２…導電層、３，５…高融点金属硅化物、又は窒化物、４…高融点金属、６…ホトレジスト、７…シリコン、８…オーミック金属、９…n^+層、１０…層間絶縁膜、１１…配線金属。

代理人弁理士　小　川　勝　男

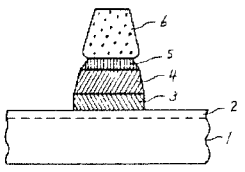
第１図



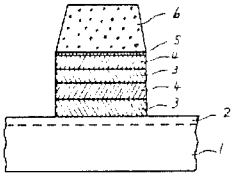
第２図



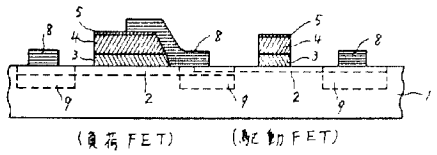
第３図



第４図



第５図

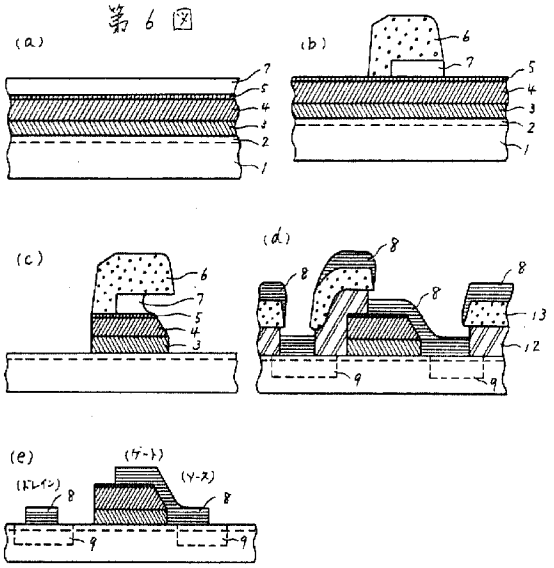


（負荷FET）　（駆動FET）

1…半絶縁性基板　2…導電層
3，5…高融点金属硅化物　又は窒化物
4…高融点金属　6…ホトレジスト
7…シリコン　8…オーミック金属　9…n⁺層
10…層間絶縁膜　11…配線金属

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第6図



1… 半絶縁性基板　2… 導電層
3, 5 … 高融点金属硅化物　又は 窒化物
4… 高融点金属　6… ホトレジスト
7… シリコン　8… オーミック金属　9… n⁺層
10 …層間絶縁膜　11… 配線金属　12… SiO_2
13…ホトレジスト

第1頁の続き

⑫発明者　重田　淳二　東京都国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内
⑫発明者　今村　慶憲　東京都国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内

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JPH03274735A MANUFACTURE OF SEMICONDUCTOR DEVICE WITH SCHOTTKY ELECTRODE

Applicants: HITACHI LTD,HITACHI VLSI ENG

Inventors: FUCHIGAMI NOBUTAKA,IMAMURA YOSHINORI,ODA HIROTO,SHIGETA JUNJI

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MANUFACTURE OF SEMICONDUCTOR DEVICE WITH SCHOTTKY ELECTRODE

Abstract

PURPOSE:To prevent the lowering of adhesive properties with a resist by forming a Schottky junction by forming a first layer composed of the silicide of a high melting point metal onto a semiconductor substrate, shaping a second layer consisting of the high melting-point metal onto the first layer, forming a third layer made up of the silicide, etc., of the high melting-point metal and forming a Schottky electrode. CONSTITUTION:Si<+> ions are implanted into a semi-insulating GaAs substrate 1 as donor impurities, and a conductive layer 2 is formed through annealing. A WSix film 3, a W film 4 and a WSix film 5 are superposed and applied successively onto the conductive layer 2. Since WSix has adhesive properties with a photo-resist better than W, the resist is hardly peeled when the photo-resist 6 is applied onto the WSix film 5 as an uppermost layer, thus improving yield. The photo-resist 6 is patterned, and the WSix film 5, the W film 4 and the WSix film 3 are machined through reactive ion etching, thus shaping a gate electrode. The photo resist 6 is removed, the ohmic electrodes of a source and a drain are formed and the electrodes and the conductive layer 2 are coated with an inter-layer insulating film 10, and a semiconductor device is completed through wiring 11.

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DESCRIPTION JPH03274735

[0001]
TECHNICAL FIELD The present invention relates to a method of manufacturing a semiconductor device having a Schottky electrode. [Prior Art] In a GaAs MESFET (Metal Semiconductor Field Effect Transistor) that uses a refractory metal or its silicide as a Schottky electrode, it has excellent thermal stability and high adhesion to the semiconductor substrate, such as tungsten silicide. Japanese Patent Application Laid-Open No. 61-214481 discloses a technique for reducing the gate resistance by using a melting point metal silicide as the first layer and superposing a high melting point metal layer such as financial tungsten on the first layer. [Problems to be Solved by the Invention] When a stacked film gate (a lower layer is a WSix film and an upper layer is a metal tungsten film) is used as a gate electrode of a GaAs MESFET, the resist is easily peeled off and the yield of gate formation is reduced. There was a problem that caused. An object of the present invention is to prevent a decrease in adhesion to a resist that occurs when a refractory metal is used as a Schottky gate electrode material. [Means for Solving the Problems] The above-mentioned object is to form a Schottky junction by directly forming a first layer made of a refractory metal silicide on a semiconductor substrate, and to obtain a high melting point on the first layer. A step of forming a second layer made of a metal directly or through a layer containing a refractory metal, and selected from the group consisting of refractory metal silicide, refractory metal nitride and silicon. Directly forming a third layer made of at least one material, directly forming a resist film on the third layer, patterning the resist film, and masking the patterned resist film The etching can be performed by etching the first layer and the layer formed on the layer to form a Schottky electrode. [Operation] In the present invention, since the refractory metal silicide is used as the lowermost layer (first layer) of the gate electrode, it is possible to form a good Schottky junction at the semiconductor interface. Further, since the refractory metal is used as the second layer, the resistance of the gate can be reduced. Further, since the third layer having good adhesion to the resist is formed as the

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uppermost layer, the resist can be prevented from peeling off. When connecting the wiring layer to the gate electrode, the contact resistance can be reduced by removing the third layer and directly connecting the wiring layer to the second layer. [Examples] Hereinafter, the present invention will be described with reference to Examples. In the example, the case of using as a gate electrode of GaAs MESFET is explained, but it can be used for other compound semiconductors such as InP, InGaAs, InAQAs and single element semiconductors such as silicon, and Schottky. -It is also possible to use it as a gate electrode for diodes, IGFT (Insulated Gate FET), etc.

First Embodiment A first embodiment of the present invention will be described with reference to FIGS. Si + ions are implanted into the semi-insulating GaAs substrate 1 as a donor impurity and annealed to form the conductive layer 2. 1100 n of W S i x film 3, 200 nm of W film 4 and 10 nm of WSix film 5 are deposited on top of this. The deposition of WSi, 3, 5 is performed by sputtering a W5Si3 target of a sintered body with Ar ″ ions, and when the pressure of Ar gas during sputtering is 9 mtorr and the power is 0.35 kw DC, W S i The set Ifxx of the x film was 0.22, and the stress in the film was 3 × 10 ” dyne / d in the tensile direction. The deposition of W114 is performed by sputtering a W target, the pressure of Ar gas is 5 mtorr, and the power is 0.36 kw in DC. At this time, the in-film stress of the W film shows 7 × 10'dyne / al in the compression direction with respect to the GaAs substrate, but since it actually adheres on the W S i x film, the stress is dissipated at any interface of WSIX. Therefore, the total stress of the W S i x film 3 and the W film 4 is almost zero for the GaAs substrate. Since the stress of the uppermost W S i x film 5 is thin, it can be ignored almost entirely. Since W S ix has better adhesion to photoresist than W, if photoresist 6 is applied on the top W S i x film S, resist peeling will hardly occur, so that the conventional W / W S i x The yield is improved as compared with the case of the two-layer structure gate. After patterning the photoresist 6, the WS ion film 5, W film 4, and WSix film 3 are processed by reactive ion etching to form a gate electrode. The sheet resistance of the gate electrode embodying this example is about 0.9 Ω / port and about 178 in the case of a single-layer W S i x gate (about 7 Ω / port). The cross-sectional shape of the processed gate metal is shown in FIG. Next, after removing the photoresist 6, the ohmic electrodes of the source and drain are not shown in detail), the interlayer insulating film 10 is covered, and the wiring 11 is provided to complete the present embodiment. The contact resistance between the wiring metal (Au) 11 and the uppermost layer W S i X film 5 is 3 to 5 Ω when the contact hole is a square of 1 × 1 μm 2. However, since the contact resistance when the uppermost layer WSix film 5 is removed at the contact hole and the wiring metal and the intermediate layer W film 4 are brought into contact with each other can be reduced to 0.6 to 0.8Ω, the parasitic resistance of the gate is reduced. Can be reduced by 2 to 4Ω.

The sectional structure in this case is shown in FIG. In Example 2 and Example 1, the uppermost layer W S i! Although the film thickness of the film 5 is set to 5 to 10 nm, the cross-sectional

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shape of the gate electrode when the film thickness is made thicker than that is shown in FIG. The thickness of the uppermost W S i X film 5 is 50 nm. In the dry etching process using CHF3, CF4, NF, gas, etc., since the etching rate of WSix is 2 to 4 times higher than W, the WS layer of the uppermost layer is etched while etching the W layer 4 of the intermediate layer. Side etching of the IX layer 5 occurs from the side surface, and the W layer 4 is exposed from the side-etched portion. As a result, the cross-sectional shape of the intermediate W film 4 becomes a trapezoid. During the processing of the bottom layer WS ix film 3, the polymer generated from the etching gas adheres to the side surface, so etching is slower than the top layer WS ix film 5, and side etching is slight. The gate electrode of the present embodiment has the disadvantage that the gate resistance is slightly higher than that of the first embodiment, but has the advantage of improving the flatness when the glabella insulating film is applied to the gate electrode. Embodiment 3 Embodiment of the present invention is shown in FIG. Since the etching rate of W S i X is higher than W in the dry etching process, a large side etch occurs on the lower "JJ S i x layer" in the two-layer structure in which the W S i x layer and the W layer are overlapped by 200 nm. Therefore, in the present embodiment, the thicknesses of the W S i X layer 3 and the W layer 4 are set to 1100 n each, and this is repeated twice to form a four-layer structure, and the top layer has a W S i x of several nm. The layer 5 is applied. In this case, since the wsix layer 3 is thinned, the side etching amount of this layer is reduced, and the cross-sectional shape of the gate electrode approaches a rectangle. In Examples 4 and 1 to 3, WS x * was used for the uppermost layer 5 as in the lowermost layer 3. The reason for this is that there is an advantage that the lowermost layer 3, the intermediate layer 4, and the uppermost layer 5 can be continuously formed by switching the sputtering target from WsSlx to W and again to W3Si. However, the top layer 5 is W S i X N y, or WN. Can also be used, and can be formed by sputtering a W, Si 3 or W target in a nitriding atmosphere. In this case, WSLxNy and WH act as a barrier metal against W in the Afl wiring and the gate electrode, suppress electromigration in the contact holes, and improve the reliability of the integrated circuit and extend the product life. ..

As the material of the uppermost layer 5, other suicides such as TaSix, MoSix, TiSix, and Irsix, or nitrides such as WN, TaNx, WB, TaB, and the like, WC, It is also possible to use carbides such as SiC and TiC, or Si. In the load FET of the fifth embodiment, the cell area can be reduced by directly connecting the gate electrode and the ohmic electrode on the source side. In this case, in the gate electrode having a rectangular cross-section, the ohmic electrode is broken at the corner of the side edge. As a method of solving this problem, the Si film is formed as the uppermost layer of the gate electrode material in the region which is the end portion on the source side of the gate electrode, and the Si film is side-etched by dry etching when forming the gate electrode. Japanese Patent Application Laid-Open No. 1-187876 discloses a method of improving the step coverage by processing the end of the gate electrode on the source side into a taper shape. Further, since Si can also achieve the object of the present invention, it is possible to combine the present invention with the above-mentioned conventional techniques. Example 5 shows an example in which this combination is applied to an integrated circuit having an inverter circuit.

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FIG. 5 is a sectional view thereof, and FIGS. 6 (a) to 6 (e) are manufacturing process diagrams of the load FET portion. The active layer 2 of the drive FET and the load FET is formed on the semi-insulating substrate 1, and the W S x layer 3 and the W layer 4 are applied by DC (direct current) sputtering at 1 o ○, 200 nm, and further RF (high frequency) A Si layer 7 of 50 nm is deposited by sputtering. At this time, at the interface between the W, Ii4 and the Si layer 7, the WSix layer 5 is formed by the mixing and diffusion of the sputter (Fig. 6 (a)). The thickness of this W S i x layer 5 can be set to 1 to 2 nm by increasing the RF power when depositing S i f @ 7, but it can be made even thicker by heating with an infrared lamp. Next, the Si layer 7 is left only on the source side in the region forming the gate electrode of the load FET, and Sif @ 7 in other regions is removed. After that, a photoresist 6 is applied to a thickness of 1 μm and a gate electrode is patterned (FIG. 6B). Tri-etching is performed using the photoresist 6 as a mask to process the gate electrode. At this time, since the etching rate of Si is an order of magnitude higher than W, side etching of Si Nl 7 proceeds from the side while etching the W layer 4. As a result, the W layer 4 is processed into a tapered shape in the portion where the S i M 7 remains.

The sectional structure of the load FET at this time is shown in FIG. 6 (c). In this process, in the gate electrode of the load FET, the lower surface of the photoresist 6 is in contact with Si or WSIX as described above, and in the gate electrode of the opening FET, the lower surface of the photoresist 6 is WSxx. Since they are in contact with each other, the photoresist 6 does not peel off during this step. Next, after removing the photoresist 6, the high-concentration conductive layer (n ″ Fg) 9 was formed by ion implantation, and further, about 300 nm was deposited by the Si 2 film 12 total 12 total 12D chemical vapor deposition) method. After that, the n + layer 9 is activated by activation annealing at 800 ° C. for 15 minutes. Then, after applying the organic resist film 13 by about 1 μm, Sin of the wiring region between the ohmic electrode formation region and the gate and the source of the load FET is used as a mask. The film 12 and the Si layer 7 are removed. Next, ohmic metal (AuGe) 8 is vapor-deposited to a thickness of 0.2 μm (FIG. 6 (d)). Next, the organic resist film 13 and the Si ○ 2 film 12 are removed (soft-off method) to form an ohmic electrode. The sectional structure of the load FET at this time is shown in FIG. The ohmic electrode 8 on the source side is directly connected to the gate electrode, and the occupied area can be made smaller than that on the drain side. A sectional view of the inverter circuit at this time is as shown in FIG. Thereafter, a one-layer insulating film is deposited and a wiring process is performed to complete the product circuit (not shown). [Advantages of the Invention] According to the present invention, the peeling of the photoresist that occurs when forming a low resistance gate electrode using tungsten is eliminated, and the yield of integrated circuits can be improved. Further, by using a refractory metal nitride or a mixture of a refractory metal silicide and a nitride in the uppermost layer, it is possible to suppress the outward diffusion of tungsten in the wiring metal and the gate electrode and to prevent the electromigration life (EM). It has the effect of extending the life). Furthermore, by selecting a material having a high etching rate such as Si for the uppermost layer, there is an effect that the side edge of the gate electrode is tapered and the step coverage can be improved. This effect is effective in improving the yield in an

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integrated circuit in which the cell area is reduced by directly connecting the gate and source of the load FET.

[0002]
Brief description of the drawings

[0003]

FIG. 1 is a cross-sectional view of a MESFET of Example 1 using a stacked gate of the present invention, FIG. 2 is a cross-sectional structure diagram of Example 1 after wiring, and FIG. 3 is a top W Six film FIG. 4 is a sectional structural view of Embodiment 2 described above, and FIG. 4 is a sectional structural view of Embodiment 3 in which the present invention is applied to a stacked gate having a four-layer structure.

FIG. 5 is a sectional structural view of Embodiment 5 showing a method of processing the source side of the gate electrode into a tapered shape in order to directly connect the ohmic electrode on the source side of the load FET and the gate electrode, FIG. 6 (6A to 6E are process step diagrams of the load FET portion of the fifth embodiment. DESCRIPTION OF SYMBOLS 1 ... Semi-insulating substrate, 2 ... Conductive layer, 3, 5 ... Refractory metal silicide or nitride, 4 ... Refractory metal, 6 ... Photoresist, 7 ... ..Silicon, 8 ... Ohmic metal, 9 ... n + layer, 10 ... Interlayer insulating film, 11 ... Wiring metal.

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CLAIMS JPH03274735

1.
A step of directly forming a first layer made of a refractory metal silicide on a plate, and a step of forming a second layer made of a refractory metal on the first layer directly or through a layer containing a refractory metal A step of directly forming a third layer of at least one selected from the group consisting of refractory metal silicides, refractory metal nitrides and silicon on the second layer, resist on the third layer Forming a film directly, patterning the resist film, and etching the first layer and a layer laminated on the first film using the patterned resist film as a mask to form a Schottky electrode And a method of manufacturing a semiconductor device having a Schottky electrode. 2. The Schottky electrode according to claim 1, wherein the layer containing a refractory metal has at least one set of layers in which a refractory metal layer and a refractory metal silicide layer are laminated in this order. A method for manufacturing a semiconductor device having the following. 3. The method for manufacturing a semiconductor device having a Schottky electrode according to claim 1 or 2, further comprising a step of removing a part or all of the third layer after forming the Schottky electrode. 4. A step of directly forming a first layer made of a refractory metal silicide on a semiconductor substrate, and a second layer made of a refractory metal on the first layer directly or through a layer containing a refractory metal. Forming step, directly forming a third layer made of silicon on the second layer, directly forming a first resist film on the third layer, patterning the first resist film And the step of etching the third layer using the patterned first resist film as a mask and forming the third layer at the interface between the second layer and the third layer at the time of forming the third layer. The step of exposing the silicide layer of the constituent material of the second layer, the silicide layer of the constituent material of the second layer in a portion continuous with the third layer and the layer left by the etching, A step of coating with a third resist film so as to terminate at the third layer, and, by using the second resist film as a mask, dry etching the first layer and the layer formed on the layer to perform a shot. A step of forming a key electrode

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shape, and the side surface of the Schottky electrode in the portion terminated by the third layer in the dry etching step is processed so that the angle of its cross section on the semiconductor substrate side is an acute angle. And a semiconductor device having a Schottky electrode. 5. The Schottky electrode is a gate electrode of a field effect transistor, and the Schottky electrode is used in a step of removing the third layer after the dry etching step and in a state where a portion between the gate electrode and the source electrode of the field effect transistor is exposed. The method for manufacturing a semiconductor device having a Schottky electrode according to claim 4, further comprising a step of depositing a conductor film between both electrodes and electrically connecting the both electrodes.

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(71)出願人　000005108
株式会社日立製作所
東京都千代田区神田駿河台四丁目６番地

(72)発明者　飯島　晋平
東京都小平市上水本町五丁目20番１号　株式会社日立製作所半導体事業部内

(72)発明者　菅原　安浩
東京都小平市上水本町五丁目20番１号　株式会社日立製作所半導体事業部内

(72)発明者　浅野　勇
東京都青梅市今井2326番地　株式会社日立製作所デバイス開発センタ内

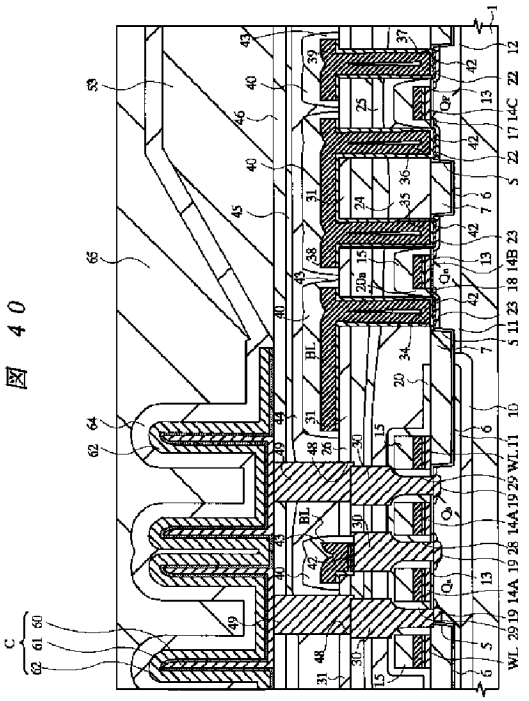
(74)代理人　弁理士　筒井　大和

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(54)【発明の名称】　半導体集積回路装置およびその製造方法

(57)【要約】
【課題】　メモリセルアレイ領域と周辺回路領域との間に段差を生じない技術を提供する。
【解決手段】　下部電極６０の形成のために用いた酸化シリコン膜５３を周辺回路領域に残存させ、容量絶縁膜６１、上部電極６２を形成し、ＣＶＤ法による酸化シリコン膜６４を堆積した後、厚膜のＳＯＧ膜６５を塗布して表面を平坦化する。

図４０



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【特許請求の範囲】
【請求項１】　メモリセル選択用ＭＩＳＦＥＴと、前記メモリセル選択用ＭＩＳＦＥＴに直列に接続され、上方に開孔部を有する筒形の下部電極、少なくとも前記下部電極の前記筒形の内面に接して形成された容量絶縁膜および前記容量絶縁膜を介し少なくとも前記下部電極の前記筒形の内面に対向して形成された上部電極を備えた情報蓄積用容量素子とでメモリセルを構成し、前記メモリセルが配置されたメモリセルアレイ領域と、前記メモリセルアレイ領域の周辺の周辺回路領域とを有する半導体集積回路装置の製造方法であって、（ａ）半導体基板の主面の前記メモリセルアレイ領域に前記メモリセル選択用ＭＩＳＦＥＴおよび前記半導体基板の主面の前記周辺回路領域に周辺回路のＭＩＳＦＥＴを形成した後、前記メモリセル選択用ＭＩＳＦＥＴおよび周辺回路のＭＩＳＦＥＴの上部に、前記下部電極の高さに相当する膜厚の第１絶縁膜を堆積する工程、（ｂ）前記メモリセル選択用ＭＩＳＦＥＴの上部の前記第１絶縁膜を開孔して溝を形成する工程、（ｃ）前記溝の内部を含む前記第１絶縁膜の上部に、前記溝が埋まらない膜厚で前記下部電極の一部となる第１導電膜を堆積する工程、（ｄ）前記溝内に形成された前記第１導電膜の凹部を充填する第２絶縁膜を形成し、前記第１絶縁膜の上部の前記第１導電膜を露出する工程、（ｅ）前記第１導電膜をエッチングし、前記溝の内部のみに前記第１導電膜を残す工程、（ｆ）前記凹部を充填する前記第２絶縁膜を除去し、前記下部電極を形成する工程、（ｇ）前記下部電極の表面に前記容量絶縁膜を形成する工程、（ｈ）前記容量絶縁膜上に第２導電膜を堆積し、前記第２導電膜をパターニングして前記上部電極を形成する工程、を含むことを特徴とする半導体集積回路装置の製造方法。
【請求項２】　請求項１記載の半導体集積回路装置の製造方法であって、
前記（ｆ）工程の後、前記第１絶縁膜の上層部分を除去し、前記下部電極の上部にかかる一部分を露出する工程、および前記（ｈ）工程の後、前記半導体基板の全面に第３絶縁膜を形成し、表面を平坦化する工程、を含むことを特徴とする半導体集積回路装置の製造方法。
【請求項３】　請求項２記載の半導体集積回路装置の製造方法であって、
その上層部分が除去された前記第１絶縁膜の前記周辺回路領域に接続孔を開口し、前記第２導電膜の堆積と同時に前記接続孔を埋め込み、前記第２導電膜のパターニングと同時に前記周辺回路領域の前記第２導電膜をパターニングしてプラグまたは配線を形成することを特徴とする半導体集積回路装置の製造方法。
【請求項４】　請求項１記載の半導体集積回路装置の製造方法であって、
前記（ｅ）工程の後、前記周辺回路領域の前記第１絶縁膜を被覆するフォトレジスト膜を形成する工程、前記（ｆ）工程において、前記第２絶縁膜の除去を前記フォトレジスト膜をマスクとした湿式エッチング法による前記メモリセルアレイ領域の前記第１絶縁膜の除去と同時に行い、前記周辺回路領域に前記第１絶縁膜の一部を残存させつつ上方に開孔部を有する筒形の前記下部電極を形成する工程、および、前記（ｈ）工程の後、前記半導体基板の全面に第３絶縁膜を形成し表面を平坦化する工程、を含むことを特徴とする半導体集積回路装置の製造方法。
【請求項５】　請求項４記載の半導体集積回路装置の製造方法であって、
前記第１絶縁膜の堆積前に前記第１絶縁膜および第２絶縁膜とはエッチング速度の相違する第４絶縁膜を前記半導体基板の全面に堆積し、前記下部電極が形成された後に前記メモリセルアレイ領域の前記第４絶縁膜をエッチングして除去する工程を含むことを特徴とする半導体集積回路装置の製造方法。
【請求項６】　メモリセル選択用ＭＩＳＦＥＴと、前記メモリセル選択用ＭＩＳＦＥＴに直列に接続され、上方に開孔部を有する筒形の下部電極、前記下部電極の表面に形成された容量絶縁膜および前記容量絶縁膜を介し前記下部電極に対向して形成された上部電極を備えた情報蓄積用容量素子とでメモリセルを構成し、前記メモリセルが配置されたメモリセルアレイ領域と、前記メモリセルアレイ領域の周辺の周辺回路領域とを有する半導体集積回路装置の製造方法であって、（ａ）半導体基板の主面に前記メモリセル選択用ＭＩＳＦＥＴを形成し、次いでその上部に情報蓄積用容量素子を形成する工程、
（ｂ）前記半導体基板の主面上に、前記情報蓄積用容量素子の高さに相当する寸法以上の膜厚で第１絶縁膜を堆積する工程、（ｃ）前記周辺回路領域の前記第１絶縁膜を被覆するフォトレジスト膜を形成した後、前記フォトレジスト膜をマスクとして湿式エッチング法により前記メモリセルアレイ領域の前記第１絶縁膜を除去する工程、（ｄ）前記半導体基板の全面に第３絶縁膜を形成し、表面を平坦化する工程、を含むことを特徴とする半導体集積回路装置の製造方法。
【請求項７】　請求項２～６記載のいずれかの半導体集積回路装置の製造方法であって、
前記第３絶縁膜の表面を平坦化する工程は、ＳＯＧ膜の塗布による第１の工程、または前記情報蓄積用容量素子の高さに相当する寸法以上の膜厚で気相成長法により堆積された絶縁膜をＣＭＰ法によりエッチングする第２の工程、のいずれかの工程であることを特徴とする半導体集積回路装置の製造方法。
【請求項８】　請求項１～７記載のいずれかの記載の半導体集積回路装置の製造方法であって、
前記第２導電膜の堆積を、前記下部電極の筒形状により形成された凹部を埋め込むように行い、その表面を平坦化することを特徴とする半導体集積回路装置の製造方

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法。
【請求項９】　メモリセル選択用ＭＩＳＦＥＴと、前記メモリセル選択用ＭＩＳＦＥＴに直列に接続され、上方に開孔部を有する筒形の下部電極、少なくとも前記下部電極の前記筒形の内面に接して形成された容量絶縁膜および前記容量絶縁膜を介し少なくとも前記下部電極の前記筒形の内面に対向して形成された上部電極を備えた情報蓄積用容量素子とでメモリセルを構成し、前記メモリセルが配置されたメモリセルアレイ領域と、前記メモリセルアレイ領域の周辺の周辺回路領域とを有する半導体集積回路装置であって、
前記情報蓄積用容量素子の高さに相当する膜厚の絶縁膜を前記周辺回路領域に有し、前記メモリセルアレイ領域と前記周辺回路領域との間の段差を解消した第１の構成、
前記情報蓄積用容量素子を構成する前記下部電極により生ずる凹部を、前記情報蓄積用容量素子を構成する前記上部電極により埋め込んだ第２の構成、
前記情報蓄積用容量素子が前記メモリセル選択用ＭＩＳＦＥＴの上部に形成され、前記情報蓄積用容量素子が、前記下部電極と前記メモリセル選択用ＭＩＳＦＥＴとを接続するプラグの一部からなる円柱電極、および、その外周に形成され容量絶縁膜を介して形成された同心円筒電極を含む円筒形容量素子と一体に形成されている第３の構成、
のいずれかの構成を有することを特徴とする半導体集積回路装置。
【請求項１０】　メモリセル選択用ＭＩＳＦＥＴと、前記メモリセル選択用ＭＩＳＦＥＴに直列に接続され、下部電極、前記下部電極に接して形成された容量絶縁膜、および前記容量絶縁膜を介し前記下部電極に対向して形成された上部電極を備えた情報蓄積用容量素子とを含むメモリセルを有する半導体集積回路装置であって、
前記下部電極および前記上部電極の双方が少なくとも窒化チタンを含む導電材からなり、前記容量絶縁膜が少なくとも多結晶酸化タンタルを含む絶縁膜からなることを特徴とする半導体集積回路装置。
【請求項１１】　請求項１０記載の半導体集積回路装置であって、
前記メモリセル選択用ＭＩＳＦＥＴと前記下部電極とを接続するプラグが窒化チタンを主成分とする導電材からなることを特徴とする半導体集積回路装置。
【請求項１２】　請求項１０または１１記載の半導体集積回路装置であって、
前記下部電極と前記容量絶縁膜との界面には１０nm以下の膜厚の酸化チタン膜が形成されていることを特徴とする半導体集積回路装置。
【請求項１３】　メモリセル選択用ＭＩＳＦＥＴと、前記メモリセル選択用ＭＩＳＦＥＴに直列に接続され、下部電極、前記下部電極に接して形成された容量絶縁膜、および前記容量絶縁膜を介し前記下部電極に対向して形成された上部電極を備えた情報蓄積用容量素子とを含むメモリセルを有する半導体集積回路装置の製造方法であって、（ａ）ＣＶＤ法により前記下部電極となる窒化チタン膜を堆積し、その窒化チタン膜を非酸化性雰囲気で熱処理する工程、（ｂ）ＣＶＤ法により酸化タンタル膜を堆積し、非酸化性雰囲気で熱処理して前記酸化タンタル膜を結晶化して多結晶酸化タンタル膜に変換する工程、（ｃ）前記多結晶酸化タンタル膜を酸化性雰囲気で熱処理し、前記多結晶酸化タンタル膜を改質すると同時に前記窒化チタン膜と前記多結晶酸化タンタル膜との界面に酸化チタンを形成する工程、（ｄ）ＣＶＤ法により前記上部電極となる窒化チタン膜を堆積する工程、を含むことを特徴とする半導体集積回路装置の製造方法。
【請求項１４】　請求項１３記載の半導体集積回路装置の製造方法であって、
前記（ａ）工程の後に、前記窒化チタン膜の表面に酸化チタン膜を形成する工程を含むことを特徴とする半導体集積回路装置の製造方法。
【請求項１５】　メモリセル選択用ＭＩＳＦＥＴと、前記メモリセル選択用ＭＩＳＦＥＴに直列に接続され、下部電極、前記下部電極に接して形成された容量絶縁膜、および前記容量絶縁膜を介し前記下部電極に対向して形成された上部電極を備えた情報蓄積用容量素子とを含むメモリセルを有する半導体集積回路装置の製造方法であって、
前記メモリセル選択用ＭＩＳＦＥＴと前記下部電極とを接続するプラグの一部を、前記メモリセル選択用ＭＩＳＦＥＴの上部に配置されるビット線と同時に形成することを特徴とする半導体集積回路装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体集積回路装置およびその製造技術に関し、特に、ＤＲＡＭ（Dynamic Random Access Memory）の蓄積容量の増大とそれに伴って生じるメモリセルアレイ領域と周辺回路領域との段差の緩和に適用して有効な技術に関するものである。
【０００２】
【従来の技術】ＤＲＡＭのメモリセルは、半導体基板の主面上にマトリクス状に配置された複数のワード線と複数のビット線との交点に配置され、１個のメモリセル選択用ＭＩＳＦＥＴ(Metal Insulator Semiconductor Field Effect Transistor) とこれに直列に接続された１個の情報蓄積用容量素子（キャパシタ）とで構成されている。メモリセル選択用ＭＩＳＦＥＴは、周囲を素子分離領域で囲まれた活性領域に形成され、主としてゲート酸化膜、ワード線と一体に構成されたゲート電極およびソース、ドレインを構成する一対の半導体領域で構成されている。ビット線は、メモリセル選択用ＭＩＳＦＥＴの上部に配置され、その延在方向に隣接する２個のメモリ

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セル選択用ＭＩＳＦＥＴによって共有されるソース、ドレインの一方と電気的に接続されている。情報蓄積用容量素子は、同じくメモリセル選択用ＭＩＳＦＥＴの上部に配置され、上記ソース、ドレインの他方と電気的に接続されている。

【０００３】特開平７－７０８４号公報は、ビット線の上部に情報蓄積用容量素子を配置するキャパシタ・オーバー・ビットライン(Capacitor Over Bitline)構造のＤＲＡＭを開示している。この公報に記載されたＤＲＡＭは、メモリセルの微細化に伴う情報蓄積用容量素子の蓄積電荷量（Ｃs)の減少を補うために、ビット線の上部に配置した情報蓄積用容量素子の下部電極（蓄積電極）を円筒状に加工することによってその表面積を増やし、その上部に容量絶縁膜と上部電極（プレート電極）とを形成している。

【０００４】しかしながら、ＣＯＢ構造を有するメモリセルにおいては、メモリセルアレイ領域に形成されるキャパシタの半導体記憶装置としての動作信頼度を確保する必要上、装置の集積度が向上しセル面積が縮小しても相当の立体化が必須となっている。このような立体化されたキャパシタを形成した後に層間絶縁膜を形成した場合には、メモリセルアレイ領域と周辺回路領域の間にキャパシタの高さに相当する分だけの段差が生じてしまう。

【０００５】このような段差は、ＤＲＡＭの集積度が増すに従い、一定のキャパシタ容量を確保する必要があり、益々高くなる方向にある。また、ＤＲＡＭの集積度向上の要求から、フォトリソグラフィの露光精度の向上が要求され、そのような要求を満足するために許容される焦点深度の値が益々厳しいものとなる。このような段差の増大、およびフォトリソグラフイにおける露光焦点の余裕の減少から、前記層間絶縁膜上に形成される配線層の形成が困難になるという問題がある。

【０００６】上記フォトリソグラフィにおける加工性の低下は、前記段差の緩和により対処することが可能であるが、このような段差を緩和することができる技術として以下のような技術が知られている。

【０００７】たとえば、特開平４－１０６５１号公報、あるいは、特開平７－７０８４号公報に記載されているような技術が知られている。この技術を簡単に説明すれば以下のとおりである。すなわち、上記公報に記載の技術は、メモリセルアレイ領域と周辺回路領域との間に、キャパシタの下部電極（ストレージノード）と同時に形成される立壁（周壁）あるいはチャネルを形成するものである。

【０００８】このような立壁あるいはチャネルを有するＤＲＡＭは以下のようにして形成される。まず、ＤＲＡＭの選択ＭＩＳＦＥＴおよび周辺回路のＭＩＳＦＥＴを所定の方法で形成後、層間絶縁膜を介してビット線を形成し、さらにビット線を覆う層間絶縁膜を形成する。次に、立体化されたキャパシタの高さに相当する膜厚の絶縁膜を堆積後、キャパシタの下部電極が形成される領域の前記絶縁膜に孔を形成すると同時に、メモリセルアレイ領域と周辺回路領域との境界領域に立壁（周壁）あるいはチャネルを形成するための溝を形成する。その後、全面に導電膜を堆積し、前記絶縁膜上の導電膜のみを除去する。さらに前記絶縁膜を除去すれば前記孔内の前記導電膜が立体化されたキャパシタの下部電極となり、前記溝内の前記導電膜が立壁もしくはチャネルとして形成される。このキャパシタの下部電極および立壁もしくはチャネルを形成する際に除去する絶縁膜を周辺回路領域にのみ残存させればメモリセルアレイ領域と周辺回路領域との間に段差が形成されず、キャパシタ上に堆積する層間絶縁膜が平坦化されることとなる。このような周辺回路領域にのみ残存させる絶縁膜の形成にはレジストマスクを用いる方法、あるいは前記導電膜をマスクとする方法が前記公報に開示されている。すなわち前記公報に開示されている技術は、立壁もしくはチャネルを存在させることにより、前記マスクの形成端部を単一または複数の立壁またはチャネルが形成された領域内で任意の位置とすることができ、フォトリソグラフィのマージンを増加してマスクの形成を容易に行うことができるとするものである。

【０００９】また、たとえば、平成５年１０月２６日、工業調査会発行、「やさしいＵＬＳＩ技術」、ｐ１５５～ｐ１６４に記載されているように、ＳＯＧ（Spin On Glass ）膜あるいは低融点ガラスの塗布および溶融による塗布法、ガラスフローによる熱処理法、ＣＶＤ（Chemical Vapor Deposition ）の表面反応メカニズムを適用して自己平坦化させる方法等が知られ、たとえば、特開平７－１２２６５４号公報には、ＢＰＳＧ（Boron-doped Phospho-Silicate Glass）膜のリフローによる平坦化とスピンオングラス膜（ＳＯＧ膜）による平坦化とを組み合わせて段差の低減を図る技術が開示されている。

【００１０】さらに、たとえば、平成８年５月１日、工業調査会発行、「電子材料」１９９６年５月号、ｐ２２～ｐ２７に記載されているように、フォトレジスト犠牲膜、ＳＯＧ膜あるいは自己平坦化ＣＶＤ膜の堆積とエッチバック法とを組み合わせた方法およびＣＭＰ（Chemical Mechanical Polishing ）法が知られている。

【００１１】

【発明が解決しようとする課題】しかし、前記した従来技術では以下のような問題があった。

【００１２】すなわち、特開平４－１０６５１号公報、あるいは、特開平７－７０８４号公報に記載されているような技術では、メモリセルアレイ領域と周辺回路領域との間に、立壁あるいはチャネルを形成するため、立壁あるいはチャネルを形成するための領域を占有し、チップサイズを大きくしてしまうという問題がある。

【００１３】また、ＳＯＧ膜あるいは低融点ガラスの塗

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布および溶融による塗布法では、微細な凹凸を埋め込む（平坦化）することはできても、周辺回路領域のように広い面積の凹部を埋め込むことはできず、前記のような段差の緩和には顕著な効果を期待できない。

【００１４】また、ガラスフローによる熱処理法、たとえばＢＰＳＧのリフロー膜では、高い温度の熱処理が必要となり、今後の高集積化されたＤＲＡＭにおいてゲート、プラグあるいはキャパシタの材料としてメタル系材料が用いられることを考慮すれば、そのような高温プロセスを採用することによるメタル系材料の好ましくない反応が生じ、ＤＲＡＭの性能を向上できない恐れがある。

【００１５】また、ＣＶＤの表面反応メカニズムを適用して自己平坦化させる方法では、プロセスが複雑となり、安定な工程の実現という観点から好ましくない。

【００１６】また、ＢＰＳＧ膜のリフローによる平坦化とスピンオングラス膜（ＳＯＧ膜）による平坦化とを組み合わせて段差の低減を図る技術では、上記した高温プロセスの採用によるデメリットを解消することはできない。

【００１７】また、フォトレジスト犠牲膜、ＳＯＧ膜あるいは自己平坦化ＣＶＤ膜の堆積とエッチバック法とを組み合わせた方法、あるいはＣＭＰ法では、ともに工程が複雑となり、好ましくない。

【００１８】本発明の目的は、立体化キャパシタを形成してもメモリセルアレイ領域と周辺回路領域との間に段差を生じない技術を提供することにある。

【００１９】また、本発明の目的は、立体化キャパシタの形成によるメモリセルアレイ領域と周辺回路領域との間の段差を解消する技術を提供し、フォトリソグラフィの困難性を解消することにある。

【００２０】また、本発明の目的は、立体化キャパシタの形成によるメモリセルアレイ領域と周辺回路領域との間の段差を解消する技術を提供し、その上層に形成される配線層の断線あるいはパターニングの不良による短絡を防止することにある。

【００２１】また、本発明の目的は、キャパシタの容量確保、および高い信頼度をともに実現した半導体集積回路装置を提供することにある。

【００２２】また、本発明の目的は、立体化キャパシタが高くなることによる製造工程途中でのキャパシタ電極の倒壊を防止する技術を提供し、半導体集積回路装置の製造歩留まりを向上することにある。

【００２３】また、本発明の目的は、高い蓄積容量値を有する立体化キャパシタを提供し、立体化キャパシタの高さを低減してキャパシタの容量確保、および高い信頼度をともに実現した半導体集積回路装置を提供することにある。

【００２４】また、本発明の目的は、メモリセルアレイ領域と周辺回路領域との間の段差を解消することにより深くなる周辺回路領域の接続孔のアスペクト比を緩和し、周辺回路領域の接続孔の加工を容易にする技術を提供することにある。

【００２５】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【００２６】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、次のとおりである。

【００２７】（１）本発明の半導体集積回路装置の製造方法は、メモリセル選択用ＭＩＳＦＥＴと、メモリセル選択用ＭＩＳＦＥＴに直列に接続され、上方に開孔部を有する筒形の下部電極、少なくとも下部電極の筒形の内面に接して形成された容量絶縁膜および容量絶縁膜を介し少なくとも下部電極の筒形の内面に対向して形成された上部電極を備えた情報蓄積用容量素子とでメモリセルを構成し、メモリセルが配置されたメモリセルアレイ領域と、メモリセルアレイ領域の周辺の周辺回路領域とを有する半導体集積回路装置の製造方法であって、（ａ）半導体基板の主面のメモリセルアレイ領域にメモリセル選択用ＭＩＳＦＥＴおよび半導体基板の主面の周辺回路領域に周辺回路のＭＩＳＦＥＴを形成した後、メモリセル選択用ＭＩＳＦＥＴおよび周辺回路のＭＩＳＦＥＴの上部に、下部電極の高さに相当する膜厚の第１絶縁膜を堆積する工程、（ｂ）メモリセル選択用ＭＩＳＦＥＴの上部の第１絶縁膜を開孔して溝を形成する工程、（ｃ）溝の内部を含む第１絶縁膜の上部に、溝が埋まらない膜厚で下部電極の一部となる第１導電膜を堆積する工程、（ｄ）溝内に形成された第１導電膜の凹部を充填する第２絶縁膜を形成し、第１絶縁膜の上部の第１導電膜を露出する工程、（ｅ）第１導電膜をエッチングし、溝の内部のみに第１導電膜を残す工程、（ｆ）凹部を充填する第２絶縁膜を除去し、下部電極を形成する工程、（ｇ）下部電極の表面に容量絶縁膜を形成する工程、（ｈ）容量絶縁膜上に第２導電膜を堆積し、第２導電膜をパターニングして上部電極を形成する工程を含むものである。

【００２８】このような半導体集積回路装置の製造方法によれば、情報蓄積用容量素子の形成のために堆積した第１絶縁膜を周辺回路領域に残すため、メモリセルアレイ領域と周辺回路領域との間に段差を形成することがない。その結果、その後の工程でのフォトリソグラフィのマージンを増加し、接続孔の開口等を安定に加工して更なる微細化に対応することが可能となる。

【００２９】（２）また、本発明の半導体集積回路装置の製造方法は、（１）記載の半導体集積回路装置の製造方法の（ｆ）工程の後、第１絶縁膜の上層部分を除去し、下部電極の上部にかかる一部分を露出する工程、および（ｈ）工程の後、半導体基板の全面に第３絶縁膜を形成し、表面を平坦化する工程を含むものである。

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【００３０】このような半導体集積回路装置の製造方法によれば、下部電極の上部にかかる一部分を露出するため、下部電極の下部には、第１絶縁膜が残存する。このため、第１絶縁膜が下部電極の機械的な補強部材として作用し、下部電極の高さが高くなっても容易に倒壊せず、安定に下部電極を形成することができる。この結果、情報蓄積用容量素子を高くして蓄積電荷量を多くすることができる。

【００３１】（３）なお、前記（２）記載の半導体集積回路装置の製造方法において、その上層部分が除去された第１絶縁膜の周辺回路領域に接続孔を開口し、第２導電膜の堆積と同時に接続孔を埋め込み、第２導電膜のパターニングと同時に周辺回路領域の第２導電膜をパターニングしてプラグまたは配線を形成することもできる。

【００３２】このような半導体集積回路装置の製造方法によれば、残存した第１絶縁膜の高さおよび上部電極の膜厚に相当する高さのプラグあるいは配線を形成するため、たとえばプラグを形成した場合には、周辺回路領域の接続孔の深さを緩和して接続孔の加工の難易度を下げることができる。これは、周辺回路領域に絶縁膜を残存しまたは絶縁膜を形成してメモリセルアレイ領域との段差を解消した場合には、相対的に周辺回路領域の絶縁膜の膜厚が大きくなり、周辺回路領域に接続孔の開口が困難となるが、その困難性を緩和することに寄与する。

【００３３】（４）また、本発明の半導体集積回路装置の製造方法は、（１）記載の半導体集積回路装置の製造方法の（ｅ）工程の後、周辺回路領域の第１絶縁膜を被覆するフォトレジスト膜を形成する工程、（ｆ）工程の第２絶縁膜の除去をフォトレジスト膜をマスクとした湿式エッチング法によるメモリセルアレイ領域の第１絶縁膜の除去と同時に行い、周辺回路領域に第１絶縁膜の一部を残存させつつ上方に開孔部を有する筒形の下部電極を形成する工程、および（ｈ）工程の後、半導体基板の全面に第３絶縁膜を形成し表面を平坦化する工程を含むものである。

【００３４】このような半導体集積回路装置の製造方法によれば、周辺回路領域に第１絶縁膜を残存させるため、メモリセルアレイ領域と周辺回路領域との間に段差を形成することがなく、その後の工程でのフォトリソグラフィのマージンを増加し、接続孔の開口等を安定に加工して更なる微細化に対応することが可能となる。また、湿式エッチング法によりメモリセルアレイ領域の第１絶縁膜の除去を行うため、上方に開口を有する筒形の下部電極が形成され、下部電極の表面積を増加して蓄積電荷量を増加することができる。

【００３５】（５）なお、（４）記載の半導体集積回路装置の製造方法において、第１絶縁膜の堆積前に第１絶縁膜および第２絶縁膜とはエッチング速度の相違する第４絶縁膜を半導体基板の全面に堆積し、下部電極が形成された後にメモリセルアレイ領域の第４絶縁膜をエッチングして除去する工程を含むこともできる。

【００３６】このような半導体集積回路装置の製造方法によれば、第４絶縁膜が形成されていた領域（メモリセル選択用ＭＩＳＦＥＴとを接続するプラグの一部）をも容量素子として機能させることができ、その電荷蓄積量を増加させることができる。なお、このようにして形成された情報蓄積用容量素子は、下部電極とメモリセル選択用ＭＩＳＦＥＴとを接続するプラグの一部からなる円柱電極、および、その外周に形成され容量絶縁膜を介して形成された同心円筒電極を含む円筒形容量素子としてその上方に形成される上方に開口を有する筒形の容量素子と一体に形成されることとなる。

【００３７】（６）本発明の半導体集積回路装置の製造方法は、メモリセル選択用ＭＩＳＦＥＴと、そのメモリセル選択用ＭＩＳＦＥＴに直列に接続され、上方に開孔部を有する筒形の下部電極、下部電極の表面に形成された容量絶縁膜および容量絶縁膜を介し下部電極に対向して形成された上部電極を備えた情報蓄積用容量素子とでメモリセルを構成し、メモリセルが配置されたメモリセルアレイ領域と、メモリセルアレイ領域の周辺の周辺回路領域とを有する半導体集積回路装置の製造方法であって、（ａ）半導体基板の主面にメモリセル選択用ＭＩＳＦＥＴを形成し、次いでその上部に情報蓄積用容量素子を形成する工程、（ｂ）半導体基板の主面上に、情報蓄積用容量素子の高さに相当する寸法以上の膜厚で第１絶縁膜を堆積する工程、（ｃ）周辺回路領域の第１絶縁膜を被覆するフォトレジスト膜を形成した後、フォトレジスト膜をマスクとして湿式エッチング法によりメモリセルアレイ領域の第１絶縁膜を除去する工程、（ｄ）半導体基板の全面に第３絶縁膜を形成し、表面を平坦化する工程を含むものである。

【００３８】このような半導体集積回路装置の製造方法によれば、周辺回路領域にのみ第１絶縁膜を形成するため、メモリセルアレイ領域と周辺回路領域との間の段差を解消し、その後の工程でのフォトリソグラフィのマージンを増加し、接続孔の開口等を安定に加工して更なる微細化に対応することが可能となる。

【００３９】（７）また、本発明の半導体集積回路装置の製造方法は、前記（２）～（６）記載のいずれかの半導体集積回路装置の製造方法において、第３絶縁膜の表面を平坦化する工程を、ＳＯＧ膜の塗布による平坦化工程とするものである。

【００４０】または、第３絶縁膜の表面を平坦化する工程を、情報蓄積用容量素子の高さに相当する寸法以上の膜厚で気相成長法により堆積された絶縁膜をＣＭＰ法によりエッチングする平坦化工程とするものである。

【００４１】このような半導体集積回路装置の製造方法によれば、周辺回路領域とメモリセルアレイ領域との間の湿式エッチングによる溝（凹部）を埋め込んで、ほぼ完全に平坦化することが可能である。特にＳＯＧ膜の塗

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布による方法では、工程が簡便であり製造を容易にすることができる。

【００４２】（８）また、本発明の半導体集積回路装置の製造方法は、前記（１）～（７）記載のいずれかの記載の半導体集積回路装置の製造方法において、第２導電膜の堆積を下部電極の筒形状により形成された凹部を埋め込むように行い、その表面を平坦化するものである。

【００４３】このような半導体集積回路装置の製造方法によれば、第２導電膜の表面に凹部が形成されず、仮に凹部を形成した場合に、その凹部を埋め込む絶縁膜の凹部の底部に発生するであろうボイド等の発生を防止し、半導体集積回路装置の信頼性を向上することができる。半導体集積回路装置が微細化され、情報蓄積用容量素子が微細化された場合には、第２導電膜の表面の凹部も相当に小さなものとなり、ボイド等の発生が起きやすくなる状況にあり、本発明は、今後の微細化傾向を考慮した場合特に有効である。

【００４４】（９）本発明の半導体集積回路装置は、メモリセル選択用ＭＩＳＦＥＴと、メモリセル選択用ＭＩＳＦＥＴに直列に接続され、上方に開孔部を有する筒形の下部電極、少なくとも下部電極の筒形の内面に接して形成された容量絶縁膜および容量絶縁膜を介し少なくとも下部電極の筒形の内面に対向して形成された上部電極を備えた情報蓄積用容量素子とでメモリセルを構成し、メモリセルが配置されたメモリセルアレイ領域と、メモリセルアレイ領域の周辺の周辺回路領域とを有する半導体集積回路装置であって、情報蓄積用容量素子の高さに相当する膜厚の絶縁膜を周辺回路領域に有し、メモリセルアレイ領域と周辺回路領域との間の段差を解消したものである。

【００４５】また、前記半導体集積回路装置であって、情報蓄積用容量素子を構成する下部電極により生じる凹部を、情報蓄積用容量素子を構成する上部電極により埋め込んだものである。

【００４６】また、前記半導体集積回路装置であって、情報蓄積用容量素子がメモリセル選択用ＭＩＳＦＥＴの上部に形成され、情報蓄積用容量素子が、下部電極とメモリセル選択用ＭＩＳＦＥＴとを接続するプラグの一部からなる円柱電極、および、その外周に形成され容量絶縁膜を介して形成された同心円筒電極を含む円筒形容量素子と一体に形成されているものである。

【００４７】このような半導体集積回路装置は、前記した（１）～（８）の製造方法により製造することが可能である。

【００４８】（１０）本発明の半導体集積回路装置は、メモリセル選択用ＭＩＳＦＥＴと、メモリセル選択用ＭＩＳＦＥＴに直列に接続され、下部電極、下部電極に接して形成された容量絶縁膜、および容量絶縁膜を介し下部電極に対向して形成された上部電極を備えた情報蓄積用容量素子とを含むメモリセルを有する半導体集積回路装置であって、下部電極および上部電極の双方が少なくとも窒化チタンを含む導電材からなり、容量絶縁膜が少なくとも多結晶酸化タンタルを含む絶縁膜からなるものである。

【００４９】このような半導体集積回路装置によれば、下部電極および上部電極の双方が少なくとも窒化チタンを含む導電材からなり、容量絶縁膜が少なくとも多結晶酸化タンタルを含む絶縁膜からなるため、蓄積電荷量の増加を図ることが可能となる。すなわち、多結晶酸化タンタルは高誘電率材料であり、また、下部電極の窒化チタンの酸化物は導電体であり、仮にシリコン材料を下部電極に用いた場合のようにシリコン酸化膜の生成による容量絶縁膜の実質的な膜厚の増加がなく、シリコン酸化膜の生成を防止するシリコン窒化膜の形成を必要としないためである。

【００５０】（１１）また、前記（１０）記載の半導体集積回路装置において、メモリセル選択用ＭＩＳＦＥＴと下部電極とを接続するプラグを窒化チタンを主成分とする導電材とすることができる。

【００５１】このような半導体集積回路装置によれば、プラグを低抵抗化して半導体集積回路装置の応答速度（メモリの読み出し、書き込み速度）を向上することができる。なお、プラグの主成分を下部電極材料である窒化チタンと同一にするため、その親和性を向上することも可能となる。

【００５２】（１２）なお、前記（１０）または（１１）記載の半導体集積回路装置において、下部電極と容量絶縁膜との界面には１０nm以下の膜厚の酸化チタン膜を形成することができる。

【００５３】このような酸化チタン膜は、容量絶縁膜である酸化タンタル膜の酸素雰囲気による熱処理により生成する場合と、酸化タンタル膜の堆積前にあらかじめ形成しておく場合の２種類がある。いずれにしろ酸化チタン膜は導電膜であり、容量絶縁膜の膜厚の増加には関係なく、容量値を増加して蓄積電荷量を増加することができる。

【００５４】（１３）本発明の半導体集積回路装置の製造方法は、メモリセル選択用ＭＩＳＦＥＴと、メモリセル選択用ＭＩＳＦＥＴに直列に接続され、下部電極、下部電極に接して形成された容量絶縁膜、および容量絶縁膜を介し下部電極に対向して形成された上部電極を備えた情報蓄積用容量素子とを含むメモリセルを有する半導体集積回路装置の製造方法であって、（ａ）ＣＶＤ法により下部電極となる窒化チタン膜を堆積し、その窒化チタン膜を非酸化性雰囲気で熱処理する工程、（ｂ）ＣＶＤ法により酸化タンタル膜を堆積し、非酸化性雰囲気で熱処理して酸化タンタル膜を結晶化して多結晶酸化タンタル膜に変換する工程、（ｃ）多結晶酸化タンタル膜を酸化性雰囲気で熱処理し、多結晶酸化タンタル膜を改質すると同時に窒化チタン膜と多結晶酸化タンタル膜との

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界面に酸化チタンを形成する工程、（ｄ）ＣＶＤ法により上部電極となる窒化チタン膜を堆積する工程を含むものである。

【００５５】このような半導体集積回路装置の製造方法によれば、前記した（１０）～（１２）の半導体集積回路装置を製造することができる。

【００５６】（１４）また、前記（１３）記載の半導体集積回路装置の製造方法において、（ａ）工程の後に、窒化チタン膜の表面に酸化チタン膜を形成する工程を含むことができる。

【００５７】このような半導体集積回路装置の製造方法によれば、酸化タンタル膜の堆積前に窒化チタンの酸化膜をあらかじめ形成しているため、多結晶酸化タンタル膜の酸化性雰囲気での熱処理により多結晶酸化タンタル膜を改質する工程において酸素の侵入を抑制することができる。仮に、窒化チタンの酸化物を形成しない場合には、窒化チタン膜と多結晶酸化タンタル膜との界面に形成される酸化チタン膜の体積が大きくなり、多結晶酸化タンタル膜に応力を与えてその絶縁性を阻害することが考えられるが、本発明の場合はそのような不具合を抑制することができる。

【００５８】（１５）本発明の半導体集積回路装置の製造方法は、メモリセル選択用ＭＩＳＦＥＴと、メモリセル選択用ＭＩＳＦＥＴに直列に接続され、下部電極、下部電極に接して形成された容量絶縁膜、および容量絶縁膜を介し下部電極に対向して形成された上部電極を備えた情報蓄積用容量素子とを含むメモリセルを有する半導体集積回路装置の製造方法であって、メモリセル選択用ＭＩＳＦＥＴと下部電極とを接続するプラグの一部を、メモリセル選択用ＭＩＳＦＥＴの上部に配置されるビット線と同時に形成するものである。

【００５９】このような半導体集積回路装置の製造方法によれば、ビット線の形成工程によりプラグを形成して工程を簡略化することができる。

【００６０】

【発明の実施の形態】以下、本発明の実施の形態を図面に基づいて詳細に説明する。なお、実施の形態を説明するための全図において、同一の機能を有する部材には同一の符号を付し、その繰り返しの説明は省略する。

【００６１】（実施の形態１）図１は、本実施の形態のＤＲＡＭを形成した半導体チップの全体平面図である。図示のように、単結晶シリコンからなる半導体チップ１Ａの主面には、Ｘ方向（半導体チップ１Ａの長辺方向）およびＹ方向（半導体チップ１Ａの短辺方向）に沿って多数のメモリアレイＭＡＲＹがマトリクス状に配置されている。Ｘ方向に沿って互いに隣接するメモリアレイＭＡＲＹの間にはセンスアンプＳＡが配置されている。半導体チップ１Ａの主面の中央部には、ワードドライバＷＤ、データ線選択回路などの制御回路や、入出力回路、ボンディングパッドなどが配置されている。

【００６２】図２は、上記ＤＲＡＭの等価回路図である。図示のように、このＤＲＡＭのメモリアレイ（ＭＡＲＹ）は、マトリクス状に配置された複数のワード線ＷＬ（ＷＬｎ-１ 、ＷＬｎ 、ＷＬｎ+１ …）と複数のビット線ＢＬおよびそれらの交点に配置された複数のメモリセル（ＭＣ）により構成されている。１ビットの情報を記憶する１個のメモリセルは、１個の情報蓄積用容量素子Ｃとこれに直列に接続された１個のメモリセル選択用ＭＩＳＦＥＴＱｓとで構成されている。メモリセル選択用ＭＩＳＦＥＴＱｓのソース、ドレインの一方は、情報蓄積用容量素子Ｃと電気的に接続され、他方はビット線ＢＬと電気的に接続されている。ワード線ＷＬの一端は、ワードドライバＷＤに接続され、ビット線ＢＬの一端は、センスアンプＳＡに接続されている。

【００６３】次に、本実施の形態のＤＲＡＭの製造方法を図３～図４１を用いて工程順に説明する。

【００６４】まず、図３に示すように、ｐ型で比抵抗が１０Ωcm程度の半導体基板１を８５０℃程度でウェット酸化してその表面に膜厚１０nm程度の薄い酸化シリコン膜２を形成した後、この酸化シリコン膜２の上部にＣＶＤ（Chemical Vapor Deposition ）法で膜厚１４０nm程度の窒化シリコン膜３を堆積する。酸化シリコン膜２は、後の工程で素子分離溝の内部に埋め込まれる酸化シリコン膜をシンタリング（焼き締め）するときなどに基板に加わるストレスを緩和するために形成される。窒化シリコン膜３は酸化されにくい性質を持つので、その下部（活性領域）の基板表面の酸化を防止するマスクとして利用される。

【００６５】次に、図４に示すように、フォトレジスト膜４をマスクにして窒化シリコン膜３、酸化シリコン膜２および半導体基板１をドライエッチングすることにより、素子分離領域の半導体基板１に深さ３００～４００nm程度の溝５ａを形成する。溝５ａを形成するには、フォトレジスト膜４をマスクにして窒化シリコン膜３をドライエッチングし、次いでフォトレジスト膜４を除去した後、窒化シリコン膜３をマスクにして酸化シリコン膜２および半導体基板１をドライエッチングしてもよい。

【００６６】次に、フォトレジスト膜４を除去した後、図５に示すように、前記のエッチングによって溝５ａの内壁に生じたダメージ層を除去するために、半導体基板１を８５０～９００℃程度でウェット酸化して溝５ａの内壁に膜厚１０nm程度の薄い酸化シリコン膜６を形成する。

【００６７】次に、図６に示すように、半導体基板１上に膜厚３００～４００nm程度の酸化シリコン膜７を堆積した後、半導体基板１を１０００℃程度でドライ酸化することにより、溝５ａに埋め込まれた酸化シリコン膜７の膜質を改善するためのシンタリング（焼き締め）を行う。酸化シリコン膜７は、例えばオゾン（O_3 ）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いた

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プラズマＣＶＤ法で堆積する。

【００６８】次に、図７に示すように、酸化シリコン膜７の上部にＣＶＤ法で膜厚１４０nm程度の窒化シリコン膜８を堆積した後、図８に示すように、フォトレジスト膜９をマスクにして窒化シリコン膜８をドライエッチングすることにより、メモリアレイと周辺回路との境界部のような相対的に広い面積の溝５ａの上部のみに窒化シリコン膜８を残す。溝５ａの上部に残った窒化シリコン膜８は、次の工程で酸化シリコン膜７をＣＭＰ法で研磨して平坦化する際に、相対的に広い面積の溝５ａの内部の酸化シリコン膜７が相対的に狭い面積の溝５ａの内部の酸化シリコン膜７に比べて深く研磨される現象（ディッシング；dishing ）を防止するために形成される。

【００６９】次に、フォトレジスト膜９を除去した後、図９に示すように、窒化シリコン膜３、８をストッパに用いたＣＭＰ法で酸化シリコン膜７を研磨して溝５ａの内部に残すことにより、素子分離溝５を形成する。

【００７０】次に、熱リン酸を用いたウェットエッチングで窒化シリコン膜３、８を除去した後、図１０に示すように、メモリセルを形成する領域（メモリアレイ）の半導体基板１にｎ型不純物、例えばＰ（リン）をイオン打ち込みしてｎ型半導体領域１０を形成し、メモリアレイと周辺回路の一部（ｎチャネル型ＭＩＳＦＥＴを形成する領域）にｐ型不純物、例えばＢ（ホウ素）をイオン打ち込みしてｐ型ウエル１１を形成し、周辺回路の他の一部（ｐチャネル型ＭＩＳＦＥＴを形成する領域）にｎ型不純物、例えばＰ（リン）をイオン打ち込みしてｎ型ウエル１２を形成する。また、このイオン打ち込みに続いて、ＭＩＳＦＥＴのしきい値電圧を調整するための不純物、例えばBF_2(フッ化ホウ素）をｐ型ウエル１１およびｎ型ウエル１２にイオン打ち込みする。ｎ型半導体領域１０は、入出力回路などから半導体基板１を通じてメモリアレイのｐ型ウエル１１にノイズが侵入するのを防止するために形成される。

【００７１】次に、ｐ型ウエル１１およびｎ型ウエル１２の各表面の酸化シリコン膜２をＨＦ（フッ酸）系の洗浄液を使って除去した後、半導体基板１を８５０℃程度でウェット酸化してｐ型ウエル１１およびｎ型ウエル１２の各表面に膜厚７nm程度の清浄なゲート酸化膜１３を形成する。

【００７２】特に限定はされないが、上記ゲート酸化膜１３を形成した後、半導体基板１をＮＯ（酸化窒素）雰囲気中またはN_2O（亜酸化窒素）雰囲気中で熱処理することによって、ゲート酸化膜１３と半導体基板１との界面に窒素を偏析させてもよい（酸窒化処理）。ゲート酸化膜１３が7nm程度まで薄くなると、半導体基板１との熱膨張係数差に起因して両者の界面に生じる歪みが顕在化し、ホットキャリアの発生を誘発する。半導体基板１との界面に偏析した窒素はこの歪みを緩和するので、上記の酸窒化処理は、極薄ゲート酸化膜１３の信頼性を向上できる。

【００７３】次に、図１１に示すように、ゲート酸化膜１３の上部にゲート電極１４Ａ、１４Ｂ、１４Ｃを形成する。ゲート電極１４Ａは、メモリセル選択用ＭＩＳＦＥＴの一部を構成し、活性領域以外の領域ではワード線ＷＬとして使用される。このゲート電極１４Ａ（ワード線ＷＬ）の幅、すなわちゲート長は、メモリセル選択用ＭＩＳＦＥＴの短チャネル効果を抑制して、しきい値電圧を一定値以上に確保できる許容範囲内の最小寸法（例えば0.２４μm程度）で構成される。また、隣接するゲート電極１４Ａ（ワード線ＷＬ）同士の間隔は、フォトリソグラフィの解像限界で決まる最小寸法（例えば0.２２μｍ）で構成される。ゲート電極１４ＢおよびゲートＭＩＳＦＥＴおよびｐチャネル型ＭＩＳＦＥＴの各一部を構成する。

【００７４】ゲート電極１４Ａ（ワード線ＷＬ）およびゲート電極１４Ｂ、１４Ｃは、例えばＰ（リン）などのｎ型不純物がドープされた膜厚７０nm程度の多結晶シリコン膜を半導体基板１上にＣＶＤ法で堆積し、次いでその上部に膜厚５０nm程度のＷＮ（タングステンナイトライド）膜と膜厚１００nm程度のＷ膜とをスパッタリング法で堆積し、さらにその上部に膜厚１５０nm程度の窒化シリコン膜１５をＣＶＤ法で堆積した後、フォトレジスト膜１６をマスクにしてこれらの膜をパターニングすることにより形成する。ＷＮ膜は、高温熱処理時にＷ膜と多結晶シリコン膜とが反応して両者の界面に高抵抗のシリサイド層が形成されるのを防止するバリア層として機能する。バリア層は、ＷＮ膜の他、ＴｉＮ（チタンナイトライド）膜などを使用することもできる。

【００７５】ゲート電極１４Ａ（ワード線ＷＬ）の一部を低抵抗の金属（Ｗ）で構成した場合には、そのシート抵抗を２～2.５Ω／□程度にまで低減できるので、ワード線遅延を低減することができる。また、ゲート電極１４（ワード線ＷＬ）をＡｌ配線などで裏打ちしなくともワード線遅延を低減できるので、メモリセルの上部に形成される配線層の数を１層減らすことができる。

【００７６】次に、フォトレジスト膜１６を除去した後、フッ酸などのエッチング液を使って、半導体基板１の表面に残ったドライエッチング残渣やフォトレジスト残渣などを除去する。このウェットエッチングを行うと、ゲート電極１４Ａ（ワード線ＷＬ）およびゲート電極１４Ｂ、１４Ｃの下部以外の領域のゲート酸化膜１３が削られると同時に、ゲート側壁下部のゲート酸化膜１３も等方的にエッチングされてアンダーカットが生じるため、そのままではゲート酸化膜１３の耐圧が低下する。そこで、半導体基板１を９００℃程度でウェット酸化することによって、削れたゲート酸化膜１３の膜質を改善する。

【００７７】次に、図１２に示すように、ｎ型ウエル１２にｐ型不純物、例えばＢ（ホウ素）をイオン打ち込み

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してゲート電極１４Ｃの両側のｎ型ウエル１２にp^-型半導体領域１７を形成する。また、ｐ型ウエル１１にｎ型不純物、例えばＰ（リン）をイオン打ち込みしてゲート電極１４Ｂの両側のｐ型ウエル１１にn^-型半導体領域１８を形成し、ゲート電極１４Ａの両側のｐ型ウエル１１にｎ型半導体領域１９を形成する。これにより、メモリアレイにメモリセル選択用ＭＩＳＦＥＴＱｓが形成される。

【００７８】次に、図１３に示すように、半導体基板１上にＣＶＤ法で膜厚５０～１００㎚程度の窒化シリコン膜２０を堆積した後、図１４に示すように、メモリアレイの窒化シリコン膜２０をフォトレジスト膜２１で覆い、周辺回路の窒化シリコン膜２０を異方性エッチングすることにより、ゲート電極１４Ｂ、１４Ｃの側壁にサイドウォールスペーサ２０ａを形成する。このエッチングは、ゲート酸化膜１３や素子分離溝５に埋め込まれた酸化シリコン膜７の削れ量を最少とするために、酸化シリコン膜に対する窒化シリコン膜２０のエッチングレートが大きくなるようなエッチングガスを使用して行う。また、ゲート電極１４Ｂ、１４Ｃ上の窒化シリコン膜１５の削れ量を最少とするために、オーバーエッチング量を必要最小限にとどめるようにする。

【００７９】次に、フォトレジスト膜２１を除去した後、図１５に示すように、周辺回路領域のｎ型ウエル１２にｐ型不純物、例えばＢ（ホウ素）をイオン打ち込みしてｐチャネル型ＭＩＳＦＥＴのp^+型半導体領域２２（ソース、ドレイン）を形成し、周辺回路領域のｐ型ウエル１１にｎ型不純物、例えばＡｓ（ヒ素）をイオン打ち込みしてｎチャネル型ＭＩＳＦＥＴのn^+型半導体領域２３（ソース、ドレイン）を形成する。これにより、周辺回路領域にＬＤＤ(Lightly Doped Drain) 構造を備えたｐチャネル型ＭＩＳＦＥＴＱｐおよびｎチャネル型ＭＩＳＦＥＴＱｎが形成される。

【００８０】次に、図１６に示すように、半導体基板１上に膜厚３００㎚程度のＳＯＧ（スピンオングラス）膜２４をスピン塗布した後、半導体基板１を８００℃、１分程度熱処理してＳＯＧ膜２４をシンタリング（焼き締め）する。

【００８１】次に、図１７に示すように、ＳＯＧ膜２４の上部に膜厚６００㎚程度の酸化シリコン膜２５を堆積した後、この酸化シリコン膜２５をＣＭＰ法で研磨してその表面を平坦化する。酸化シリコン膜２５は、例えばオゾン（O_3）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いたプラズマＣＶＤ法で堆積する。

【００８２】このように、本実施の形態では、ゲート電極１４Ａ（ワード線ＷＬ）およびゲート電極１４Ｂ、１４Ｃの上部にリフロー性が高いＳＯＧ膜２４を塗布し、さらにその上部に堆積した酸化シリコン膜２５をＣＭＰ法で平坦化する。これにより、ゲート電極１４Ａ（ワード線ＷＬ）同士の微細な隙間のギャップフィル性が向上すると共に、ゲート電極１４Ａ（ワード線ＷＬ）およびゲート電極１４Ｂ、１４Ｃの上部の絶縁膜の平坦化を実現することができる。

【００８３】次に、図１８に示すように、酸化シリコン膜２５の上部に膜厚１００㎚程度の酸化シリコン膜２６を堆積する。この酸化シリコン膜２６は、ＣＭＰ法で研磨されたときに生じた前記酸化シリコン膜２５の表面の微細な傷を補修するために堆積する。酸化シリコン膜２６は、例えばオゾン（O_3）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いたプラズマＣＶＤ法で堆積する。酸化シリコン膜２５の上部には、上記酸化シリコン膜２６に代えてＰＳＧ(Phospho Silicate Glass)膜などを堆積してもよい。

【００８４】次に、図１９に示すように、フォトレジスト膜２７をマスクにしたドライエッチングでメモリセル選択用ＭＩＳＦＥＴＱｓのｎ型半導体領域１９（ソース、ドレイン）の上部の酸化シリコン膜２６、２５およびＳＯＧ膜２４を除去する。このエッチングは、窒化シリコン膜２０に対する酸化シリコン膜２６、２５およびＳＯＧ膜２４のエッチングレートが大きくなるような条件で行い、ｎ型半導体領域１９や素子分離溝５の上部を覆っている窒化シリコン膜２０が完全には除去されないようにする。

【００８５】なお、図１９における酸化シリコン膜２６およびレジスト膜２７の表面は、図１８に示すような周辺回路領域における酸化シリコン膜２５表面に沿って落ち込み（段差）形状を成している。図１９はその形状を省略している。

【００８６】続いて、図２０に示すように、上記フォトレジスト膜２７をマスクにしたドライエッチングでメモリセル選択用ＭＩＳＦＥＴＱｓのｎ型半導体領域１９（ソース、ドレイン）の上部の窒化シリコン膜２０とゲート酸化膜１３とを除去することにより、ｎ型半導体領域１９（ソース、ドレイン）の一方の上部にコンタクトホール２８を形成し、他方の上部にコンタクトホール２９を形成する。

【００８７】このエッチングは、酸化シリコン膜（ゲート酸化膜１３および素子分離溝５内の酸化シリコン膜７）に対する窒化シリコン膜１５のエッチングレートが大きくなるような条件で行い、ｎ型半導体領域１９や素子分離溝５が深く削れないようにする。また、このエッチングは、窒化シリコン膜２０が異方的にエッチングされるような条件で行い、ゲート電極１４Ａ（ワード線ＷＬ）の側壁に窒化シリコン膜２０が残るようにする。これにより、フォトリソグラフィの解像限界以下の微細な径を有するコンタクトホール２８、２９がゲート電極１４Ａ（ワード線ＷＬ）に対して自己整合で形成される。コンタクトホール２８、２９をゲート電極１４Ａ（ワード線ＷＬ）に対して自己整合で形成するには、あらかじめ窒化シリコン膜２０を異方性エッチングしてゲート電

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極１４Ａ（ワード線ＷＬ）の側壁にサイドウォールスペーサを形成しておいてもよい。

【００８８】次に、フォトレジスト膜２７を除去した後、フッ酸＋フッ化アンモニウム混液などのエッチング液を使って、コンタクトホール２８、２９の底部に露出した基板表面のドライエッチング残渣やフォトレジスト残渣などを除去する。その際、コンタクトホール２８、２９の側壁に露出したＳＯＧ膜２４もエッチング液に曝されるが、ＳＯＧ膜２４は、前述した８００℃程度のシンタリングによってフッ酸系のエッチング液に対するエッチングレートが低減されているので、このウェットエッチング処理によってコンタクトホール２８、２９の側壁が大きくアンダーカットされることはない。これにより、次の工程でコンタクトホール２８、２９の内部に埋め込まれるプラグ同士のショートを確実に防止することができる。

【００８９】次に、図２１に示すように、コンタクトホール２８、２９の内部にプラグ３０を形成する。プラグ３０は、酸化シリコン膜２６の上部にｎ型不純物（例えばＰ（リン））をドープした多結晶シリコン膜をＣＶＤ法で堆積した後、この多結晶シリコン膜をＣＭＰ法で研磨してコンタクトホール２８、２９の内部に残すことにより形成する。

【００９０】次に、図２２に示すように、酸化シリコン膜２６の上部に膜厚２００㎚程度の酸化シリコン膜３１を堆積した後、半導体基板１を８００℃程度で熱処理する。酸化シリコン膜３１は、例えばオゾン（O_3）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いたプラズマＣＶＤ法で堆積する。この熱処理によって、プラグ３０を構成する多結晶シリコン膜中のｎ型不純物がコンタクトホール２８、２９の底部からメモリセル選択用ＭＩＳＦＥＴＱｓのｎ型半導体領域１９（ソース、ドレイン）に拡散し、ｎ型半導体領域１９が低抵抗化される。

【００９１】次に、図２３に示すように、フォトレジスト膜３２をマスクにしたドライエッチングで前記コンタクトホール２８の上部の酸化シリコン膜３１を除去してプラグ３０の表面を露出させる。次に、フォトレジスト膜３２を除去した後、図２４に示すように、フォトレジスト膜３３をマスクにしたドライエッチングで周辺回路領域の酸化シリコン膜３１、２６、２５、ＳＯＧ膜２４およびゲート酸化膜１３を除去することにより、ｎチャネル型ＭＩＳＦＥＴＱｎのn^+型半導体領域２３（ソース、ドレイン）の上部にコンタクトホール３４、３５を形成し、ｐチャネル型ＭＩＳＦＥＴＱｐのp^+型半導体領域２２（ソース、ドレイン）の上部にコンタクトホール３６、３７を形成する。

【００９２】次に、フォトレジスト膜３３を除去した後、図２５に示すように、酸化シリコン膜３１の上部にビット線ＢＬおよび周辺回路の第１層配線３８、３９を形成する。ビット線ＢＬおよび第１層配線３８、３９を形成するには、まず酸化シリコン膜３１の上部に膜厚５０㎚程度のＴｉ膜をスパッタリング法で堆積し、半導体基板１を８００℃程度で熱処理する。次いで、Ｔｉ膜の上部に膜厚５０㎚程度のＴｉＮ膜をスパッタリング法で堆積し、さらにその上部に膜厚１５０㎚程度のW膜と膜厚２００㎚程度の窒化シリコン膜４０とをＣＶＤ法で堆積した後、フォトレジスト膜４１をマスクにしてこれらの膜をパターニングする。

【００９３】酸化シリコン膜３１の上部にＴｉ膜を堆積した後、半導体基板１を８００℃程度で熱処理することにより、Ｔｉ膜と下地Ｓｉとが反応し、ｎチャネル型ＭＩＳＦＥＴＱｎのn^+型半導体領域２３（ソース、ドレイン）の表面とｐチャネル型ＭＩＳＦＥＴＱｐのp^+型半導体領域２２（ソース、ドレイン）の表面とプラグ３０の表面とに低抵抗のＴｉＳｉ２（チタンシリサイド）層４２が形成される。これにより、n^+型半導体領域２３、p^+型半導体領域２２およびプラグ３０に接続される配線（ビット線ＢＬ、第１層配線３８、３９）のコンタクト抵抗を低減することができる。また、ビット線ＢＬをW膜／ＴｉＮ膜／Ｔｉ膜で構成することにより、そのシート抵抗を２Ω／□以下にまで低減できるので、情報の読み出し速度および書き込み速度を向上させることができると共に、ビット線ＢＬと周辺回路の第１層配線３８、３９とを一つの工程で同時に形成することができるので、ＤＲＡＭの製造工程を短縮することができる。さらに、周辺回路の第１層配線（３８、３９）をビット線ＢＬと同層の配線で構成した場合には、第１層配線をメモリセルの上層のＡｌ配線で構成する場合に比べて周辺回路のＭＩＳＦＥＴ（ｎチャネル型ＭＩＳＦＥＴＱｎ、ｐチャネル型ＭＩＳＦＥＴＱｐ）と第１層配線とを接続するコンタクトホール（３４～３７）のアスペクト比が低減されるため、第１層配線の接続信頼性が向上する。

【００９４】ビット線ＢＬは、隣接するビット線ＢＬとの間に形成される寄生容量をできるだけ低減して情報の読み出し速度および書き込み速度を向上させるために、その間隔がその幅よりも長くなるように形成する。ビット線ＢＬの間隔は例えば0.２４μｍ程度とし、その幅は例えば0.２２μｍ程度とする。

【００９５】次に、フォトレジスト膜４１を除去した後、図２６に示すように、ビット線ＢＬの側壁と第１層配線３８、３９の側壁とにサイドウォールスペーサ４３を形成する。サイドウォールスペーサ４３は、ビット線ＢＬおよび第１層配線３８、３９の上部にＣＶＤ法で窒化シリコン膜を堆積した後、この窒化シリコン膜を異方性エッチングして形成する。

【００９６】次に、図２７に示すように、ビット線ＢＬおよび第１層配線３８、３９の上部に膜厚３００㎚程度のＳＯＧ膜４４をスピン塗布する。次いで、半導体基板

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１を８００℃、１分程度熱処理してＳＯＧ膜４４をシンタリング（焼き締め）する。

【００９７】ＳＯＧ膜４４は、ＢＰＳＧ膜に比べてリフロー性が高く、微細な配線間のギャップフィル性に優れているので、フォトリソグラフィの解像限界程度まで微細化されたビット線ＢＬ同士の隙間を良好に埋め込むことができる。また、ＳＯＧ膜４４は、ＢＰＳＧ膜で必要とされる高温、長時間の熱処理を行わなくとも高いリフロー性が得られるため、ビット線ＢＬの下層に形成されたメモリセル選択用ＭＩＳＦＥＴＱｓのソース、ドレインや周辺回路のＭＩＳＦＥＴ（ｎチャネル型ＭＩＳＦＥＴＱｎ、ｐチャネル型ＭＩＳＦＥＴＱｐ）のソース、ドレインに含まれる不純物の熱拡散を抑制して浅接合化を図ることができる。さらに、ゲート電極１４Ａ（ワード線ＷＬ）およびゲート電極１４Ｂ、１４Ｃを構成するメタル（Ｗ膜）の劣化を抑制できるので、ＤＲＡＭのメモリセルおよび周辺回路を構成するＭＩＳＦＥＴの高性能化を実現することができる。また、ビット線ＢＬおよび第１層配線３８、３９を構成するＴｉ膜、ＴｉＮ膜、Ｗ膜の劣化を抑制して配線抵抗の低減を図ることができる。

【００９８】次に、図２８に示すように、ＳＯＧ膜４４の上部に膜厚６００㎚程度の酸化シリコン膜４５を堆積した後、この酸化シリコン膜４５をＣＭＰ法で研磨してその表面を平坦化する。酸化シリコン膜４５は、例えばオゾン（O_3）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いたプラズマＣＶＤ法で堆積する。

【００９９】このように、本実施の形態では、ビット線ＢＬおよび第１層配線３８、３９の上部に成膜直後でも平坦性が良好なＳＯＧ膜４４を塗布し、さらにその上部に堆積した酸化シリコン膜４５をＣＭＰ法で平坦化する。これにより、ビット線ＢＬ同士の微細な隙間のギャップフィル性が向上すると共に、ビット線ＢＬおよび第１層配線３８、３９の上部の絶縁膜の平坦化を実現することができる。また、高温・長時間の熱処理を行わないため、メモリセルおよび周辺回路を構成するＭＩＳＦＥＴの特性劣化を防止して高性能化を実現することができると共に、ビット線ＢＬおよび第１層配線３８、３９の低抵抗化を図ることができる。

【０１００】なお、酸化シリコン膜４５の上部に膜厚１００㎚程度の酸化シリコン膜を堆積してもよい。この酸化シリコン膜は、ＣＭＰ法で研磨されたときに生じた前記酸化シリコン膜の表面の微細な傷を補修することができる。このような酸化シリコン膜は、例えばオゾン（O_3）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いたプラズマＣＶＤ法で堆積することができる。

【０１０１】次に、図２９に示すように、酸化シリコン膜４５の上部に膜厚５０㎚程度の窒化シリコン膜４６を堆積する。この窒化シリコン膜４６は、後述する情報蓄積用容量素子の下部電極を形成する工程で下部電極の間の酸化シリコン膜をエッチングする際のエッチングストッパとして使用される。したがって、窒化シリコン膜４６は、後に説明する下部電極の間の酸化シリコン膜のエッチング速度よりもエッチング速度の遅い窒化シリコン材料で構成されている。

【０１０２】次に、図３０に示すように、フォトレジスト膜４７をマスクにしたドライエッチングでコンタクトホール２９の上部の窒化シリコン膜４６、酸化シリコン膜４５、ＳＯＧ膜４４および酸化シリコン膜３１を除去してプラグ３０の表面に達するスルーホール４８を形成する。このエッチングは、窒化シリコン膜４６を窒化シリコンがエッチングされる条件でエッチングした後、酸化シリコン膜４５、３１およびＳＯＧ膜４４に対する窒化シリコン膜のエッチングレートが小さくなるような条件で行い、スルーホール４８とビット線ＢＬの合わせずれが生じた場合でも、ビット線ＢＬの上部の窒化シリコン膜４０やサイドウォールスペーサ４３が深く削れないようにする。これにより、スルーホール４８がビット線ＢＬに対して自己整合で形成される。

【０１０３】次に、フォトレジスト膜４７を除去した後、フッ酸＋フッ化アンモニウム混液などのエッチング液を使って、スルーホール４８の底部に露出したプラグ３０の表面のドライエッチング残渣やフォトレジスト残渣などを除去する。その際、スルーホール４８の側壁に露出したＳＯＧ膜４４もエッチング液に曝されるが、ＳＯＧ膜４４は、前記８００℃程度のシンタリングによってフッ酸系のエッチング液に対するエッチングレートが低減されているので、このウェットエッチング処理によってスルーホール４８の側壁が大きくアンダーカットされることはない。これにより、次の工程でスルーホール４８の内部に埋め込まれるプラグとビット線ＢＬとのショートを確実に防止することができる。また、プラグとビット線ＢＬとを十分に離間させることができるので、ビット線ＢＬの寄生容量の増加を抑制することができる。

【０１０４】次に、図３１に示すように、スルーホール４８の内部にプラグ４９を形成する。プラグ４９は、窒化シリコン膜４６の上部にｎ型不純物（例えばＰ（リン））をドープした多結晶シリコン膜をＣＶＤ法で堆積した後、この多結晶シリコン膜をエッチバックしてスルーホール４８の内部に残すことにより形成する。

【０１０５】次に、図３２に示すように、窒化シリコン膜４６の上部に膜厚0.５μｍ程度の酸化シリコン膜５３を堆積した後、フォトレジスト膜５４をマスクにしたドライエッチングで酸化シリコン膜５３を除去することにより、プラグ４９を埋め込んだスルーホール４８の上部に溝５５を形成する。酸化シリコン膜５３は、例えばオゾン（O_3）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いたプラズマＣＶＤ法で堆積する。

【０１０６】次に、フォトレジスト膜５４を除去した

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後、図３３に示すように、酸化シリコン膜５３の上部にｎ型不純物（例えばＰ（リン））をドープした膜厚５０nm程度の多結晶シリコン膜５６をＣＶＤ法で堆積する。この多結晶シリコン膜５６は、情報蓄積用容量素子の下部電極材料として使用される。

【０１０７】次に、図３４に示すように、多結晶シリコン膜５６の上部に溝５５を埋め込むに十分な膜厚（例えば0.４μm程度）の酸化シリコン膜５７をたとえばＣＶＤ法で形成した後、図３５に示すように、酸化シリコン膜５７をたとえばドライエッチング法を用いてエッチバックし溝５５内にのみ酸化シリコン膜５７を残存させ、さらに酸化シリコン膜５３の上部の多結晶シリコン膜５６をエッチバックすることにより、溝５５の内側（内壁および底部）に多結晶シリコン膜５６を残す。

【０１０８】次に、図３６に示すように、周辺回路領域の酸化シリコン膜５３を覆うフォトレジスト膜５８を形成する。このフォトレジスト膜５８は、メモリセルアレイ領域の最外端に位置する情報蓄積用容量素子の下部電極となる多結晶シリコン膜５６から５μm程度離れていても問題はない。このため、フォトレジスト膜５８を形成するために高度なフォトリソグラフィの技術は必要ではない。これにより製造工程の負荷を低減して製造方法を簡略化できる。

【０１０９】次に、図３７に示すように、表面が露出している領域の酸化シリコン膜５３および酸化シリコン膜５７を湿式エッチングにより除去する。湿式エッチングは、たとえばフッ酸（ＨＦ）とフッ化アンモニウム（NH_4F）の1対２０混合液に浸漬して行ない、下地の窒化シリコン膜４６が露出するまで行うことができる。

【０１１０】この表面が露出している領域の酸化シリコン膜５３および酸化シリコン膜５７の除去にはドライエッチング法を用いることもできるが、酸化シリコン膜５３のエッチング端部を傾斜面にするためには等方的にエッチングが進行する湿式エッチングの方が都合が良い。また、窒化シリコン膜４６および多結晶シリコン膜５６とのエッチングの選択性を確保できる点においても湿式エッチングの方が都合が良い。

【０１１１】このようにして多結晶シリコン膜５６からなる下部電極６０を形成する。なお、周辺回路領域には酸化シリコン膜５３が残存しているので、後に説明する平坦化を容易に行うことができる。

【０１１２】なお、本実施の形態ではフォトレジスト膜５８を例示しているが、これに限られるものではない。

【０１１３】次に、フォトレジスト膜５８を除去し、次いで下部電極６０を構成する多結晶シリコン膜（５６）の酸化を防止するために、半導体基板１をアンモニア雰囲気中、８００℃程度で熱処理して多結晶シリコン膜（５６）の表面を窒化して膜厚1.５nm程度の窒化シリコン膜（図示せず）を形成した後、図３８に示すように、半導体基板１の全面に膜厚１０nm程度のTa_2O_5（酸化タンタル）膜６１をＣＶＤ法で堆積し、次いで半導体基板１を８００℃程度で熱処理してTa_2O_5膜６１の改質処理を行う。このTa_2O_5膜６１は、情報蓄積用容量素子の容量絶縁膜材料として使用される。

【０１１４】次に、図３９に示すように、Ta_2O_5膜６１の上部にたとえばＣＶＤ法で膜厚５０nm程度のＴｉＮ膜６２を堆積した後、フォトレジスト膜６３をマスクにしたドライエッチングでＴｉＮ膜６２およびTa_2O_5膜６１をパターニングすることにより、ＴｉＮ膜６２からなる上部電極と、Ta_2O_5膜６１からなる容量絶縁膜と、多結晶シリコン膜５６からなる下部電極６０とで構成される情報蓄積用容量素子Ｃを形成する。これにより、メモリセル選択用ＭＩＳＦＥＴＱｓとこれに直列に接続された情報蓄積用容量素子Ｃとで構成されるＤＲＡＭのメモリセルが完成する。

【０１１５】次に、フォトレジスト膜６３を除去した後、図４０に示すように、情報蓄積用容量素子Ｃの上部に膜厚４０nm程度の酸化シリコン膜６４を堆積する。酸化シリコン膜６４は、例えばオゾン（O_3）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いたプラズマＣＶＤ法で堆積する。

【０１１６】その後、厚く形成してもヒビ割れの生じない厚膜のＳＯＧ膜６５を回転塗付法により形成して表面を平坦化する。この厚膜に塗付可能なＳＯＧ膜については、一例が特願平３－２４５４９９号公報に述べられており、例えば東京応化社製の商品名タイプ８を用いることができる。

【０１１７】次に、図４１に示すように、フォトレジスト膜をマスクにしたドライエッチングで周辺回路の第１層配線３８の上部のＳＯＧ膜６５、酸化シリコン膜６４、５３、窒化シリコン膜４６、酸化シリコン膜４５、ＳＯＧ膜４４および窒化シリコン膜４０を除去することにより、スルーホール６６ａを形成する。また、同様に上部電極であるＴｉＮ膜６２の上部のＳＯＧ膜６５、酸化シリコン膜６４を除去することにより、スルーホール６６ｂを形成する。その後、スルーホール６６ａ、６６ｂの内部にプラグ６７を形成し、続いてＳＯＧ膜６５の上部に第２層配線６８を形成する。プラグ６７は、ＳＯＧ膜６５の上部にスパッタリング法で膜厚１００nm程度のＴｉＮ膜を堆積し、さらにその上部にＣＶＤ法で膜厚５００nm程度のW膜を堆積した後、これらの膜をエッチバックしてスルーホール６６ａ、６６ｂの内部に残すことにより形成する。第２層配線６８は、ＳＯＧ膜６５の上部にスパッタリング法で膜厚５０nm程度のＴｉＮ膜、膜厚５００nm程度のＡｌ（アルミニウム）膜、膜厚５０nm程度のＴｉ膜を堆積した後、フォトレジスト膜をマスクにしたドライエッチングでこれらの膜をパターニングして形成する。

【０１１８】その後、層間絶縁膜を介して第３層配線を形成し、その上部に酸化シリコン膜と窒化シリコン膜と

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で構成されたパッシベーション膜を堆積するが、その図示は省略する。以上の工程により、本実施の形態のＤＲＡＭが略完成する。

【０１１９】なお、第３層配線およびそれに接続するプラグは第２層配線の場合と同様に形成することができ、層間絶縁膜は、例えば膜厚３００nm程度の酸化シリコン膜、膜厚４００nm程度のＳＯＧ膜および膜厚３００nm程度の酸化シリコン膜で構成できる。酸化シリコン膜は、例えばオゾン（O_3）とテトラエトキシシラン（ＴＥＯＳ）とをソースガスに用いたプラズマＣＶＤ法で堆積できる。

【０１２０】本実施の形態によれば、情報蓄積用容量素子を形成した後に表面の平坦化が可能となり、従来、メモリセルアレイ領域と周辺回路領域に段差があった場合、フォトリソグラフィ工程における露光焦点深度の余裕度が減少してパターン形成が困難となる問題を解消できる、この結果、下部電極６０の高さを高くして容量の増加を図ることができる。

【０１２１】なお、本実施の形態ではビット線ＢＬを金属を含む積層膜で構成して、シリコン基板等とのコンタクトの耐熱性が乏しくなっても容量絶縁膜６１に酸化タンタル膜６１ｃを用いているので熱処理の低温化が可能となり、コンタクト部分での導通不良を回避できる利点がある。

【０１２２】（実施の形態２）図４２は、本実施の形態のＤＲＡＭの一例を示した断面図である。本実施の形態のＤＲＡＭは、容量絶縁膜６１および上部電極６２の一部がプラグ４９の上部の周辺にも配置されたものである。これにより蓄積電荷量の増加を図ることができる。つまりプラグ４９の上部を下部電極６０に接続された円柱電極とし、その回りに配置された同心円筒電極として上部電極６２を配置して、円柱形容量素子と、上部に開口を有する筒形容量素子とを一体に形成して情報蓄積用容量素子とするものである。

【０１２３】本実施の形態のＤＲＡＭの製造方法は、実施の形態１における図３７の工程までは同一である。

【０１２４】この後、図４３に示すように、窒化シリコン膜４６をたとえば熱リン酸による湿式エッチング法によりエッチングする。このとき、酸化シリコン膜はエッチングされない。そのため、酸化シリコン膜５３が一種のマスクとして作用し、周辺回路領域の窒化シリコン膜４６の全てがエッチングされることを防止できる。

【０１２５】その後、図４４に示すように、実施の形態１と同様に、容量絶縁膜６１、上部電極６２を形成する。

【０１２６】その後の工程は実施の形態１と同様であるため説明を省略する。このようにして本実施の形態のＤＲＡＭがほぼ完成する。

【０１２７】（実施の形態３）本実施の形態では、情報蓄積用容量素子の形成後にＳＯＧ膜で表面を平坦化する、より効果的な方法について図４５を用いて説明する。

【０１２８】情報蓄積用容量素子の形成後に厚膜のＳＯＧ膜を形成する場合に以下のような問題が生じることがある。すなわち、実施の形態１における下部電極６０は上方に開口を有する筒形の形状を有するものであり、この形状を反映して上部電極６２の表面にも凹部が形成される。この凹部に厚膜のＳＯＧ膜６５を塗布して表面の平坦化を図る訳であるが、厚膜のＳＯＧ膜６５は、回転塗布法によって形成され、情報蓄積用容量素子を形成することによって表面に生じる凹凸が大きくなる。すなわち溝の幅が狭く且つ深くなると溝の内部を完全に充填することができなくなる場合がある。このような場合、溝の中央部、底部あるいは側面にボイドを生じ、これらのボイドは、後の工程で受ける熱処理により膨張して厚膜のＳＯＧ膜６５を破壊する場合があり好ましくない。なお、実施の形態１で説明した、メモリセルアレイ領域と周辺回路領域の境界領域に生じる溝（凹部）には幅に余裕があるためこのような問題は発生しない。

【０１２９】そこで、本実施の形態では以下の方法によりボイドの発生を回避する。図４５は、本実施の形態の製造方法の一例を示す断面図である。

【０１３０】すなわち、情報蓄積用容量素子の上部電極６９を溝が埋るように形成し、ＳＯＧを形成する前に予めメモリセルアレイ領域を上部電極６９自体で平坦化する。この上部電極による平坦化は、メモリセルアレイ領域内に規則的に配置されている情報蓄積用容量素子の間隔のうち最も長い部分の半分以上の膜厚を有する上部電極材料をＣＶＤ法により堆積することにより達成できる。上部電極材料には、四塩化チタンとアンモニアを原料として生成する窒化チタンや周知の多結晶シリコンなどを用いることができる。

【０１３１】本実施の形態によれば情報蓄積用容量素子を形成することによって生じる溝を情報蓄積用容量素子の一構成要素となる上部電極６９自体で充填することができるので、狭くて深い溝をＳＯＧで充填する場合に発生するボイド等によるＤＲＡＭの信頼性の低下を回避できる。

【０１３２】（実施の形態４）本実施の形態では、情報蓄積用容量素子の下部電極に金属もしくは金属化合物を用いる場合のプラグの構成について図４６を用いて説明する。

【０１３３】図４６は、実施の形態４のＤＲＡＭを示した断面図である。本実施の形態では、実施の形態１のプラグ３０の代わりに、ビット線ＢＬと同時に形成される金属プラグ７０が形成されている。また、本実施の形態では、下部電極６０の下部に形成されるプラグ４９も金属プラグとすることができる。さらに下部電極６０も金属膜で形成することができる。金属プラグ、金属膜の材質としては窒化チタン、あるいは窒化チタンとタングス

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テンを例示できる。

【０１３４】本実施の形態のＤＲＡＭの製造方法は、実施の形態１における図２０のコンタクトホール２８、２９の開口までは同一である。次に、実施の形態１におけるプラグ３０を形成することなく、ビット線ＢＬを形成する。なお、このとき周辺回路のコンタクトホール３４、３５、３６、３７をあらかじめ開口しておくことは実施の形態１と同様である。

【０１３５】このようにして、金属プラグ７０がビット線ＢＬおよび第１層配線３８と同時に形成できる。

【０１３６】その後、実施の形態１の図３０までの工程は同一であり、図３１において形成されるプラグ４９の代わりに窒化チタンからなる金属プラグ７１を形成する。

【０１３７】さらに、実施の形態１の図３３における多結晶シリコン膜５６の代わりに窒化チタン膜を堆積し、実施の形態１と同様の工程により窒化チタンからなる下部電極７２を形成する。その他の工程は実施の形態１と同様である。

【０１３８】本実施の形態によれば、情報蓄積用容量素子の下部電極７２を窒化チタンで構成しているので、下地の金属プラグ７１を金属もしくは金属化合物で構成することが可能となり、シリコンで構成する場合に比べ低抵抗化でき、プラグの一部をビット線と同じ工程で形成できる利点がある。

【０１３９】（実施の形態５）本実施の形態では、情報蓄積用容量素子の下部電極を島形に形成する場合の表面の平坦化方法について図４７～図５１を用いて説明する。図４７～図５１は、実施の形態５の製造方法をその工程順に説明した一部断面図である。

【０１４０】本実施の形態の製造方法は、実施の形態１の図３１までの工程については同様である。なお、図３１におけるプラグ４９は、本実施の形態では窒化チタンからなる金属プラグ７１とする。金属プラグ７１は、全面に窒化チタン膜をスルーホール４８が埋まる程度の膜厚でＣＶＤ法により堆積した後、堆積膜厚分だけエッチング除去する周知の方法により形成できる。

【０１４１】次に、図４７に示すように、膜厚５００nmのタングステン膜をスパッタ法により全面に形成した後、パターニングされたフォトレジスト膜７３を所定の位置に形成し、ドライエッチング法により前記タングステン膜を加工して下部電極７４を形成する。

【０１４２】次に、図４８に示すように、フォトレジスト膜７３を除去した後、容量絶縁膜として厚さ１５nmの酸化タンタル膜（図示せず）をＣＶＤ法により形成し熱処理を施した後、下部電極の間が埋るように窒化チタン膜を全面に形成し、周辺回路領域の窒化チタン膜を周知のリソグラフイとドライエッチング法により除去し、上部電極７５を形成する。

【０１４３】次に、図４９に示すように、厚さ５００nmの酸化シリコン膜７６をＣＶＤ法により全面に形成する。酸化シリコン膜７６は、たとえばオゾンとＴＥＯＳを原料としたＣＶＤ法により形成することができる。

【０１４４】次に、図５０に示すように、周辺回路領域にフォトレジスト膜７７を形成し、それをマスクとしてメモリセルアレイ領域の酸化シリコン膜７６をたとえばフッ酸溶液によりエッチング除去する。このように湿式エッチングによりエッチングすることの効果は、実施の形態１で説明した場合と同様である。

【０１４５】次に、図５１に示すように、フォトレジスト膜７７を除去した後、厚さ５０nmの酸化シリコン膜７８を半導体基板１の全面に形成し、厚膜のＳＯＧ膜７９を塗布し形成して全面を平坦化する。酸化シリコン膜７８および厚膜のＳＯＧ膜７９は、実施の形態１における酸化シリコン膜６４および厚膜のＳＯＧ膜６５と同様である。

【０１４６】その後の工程は、実施の形態１と同様である。

【０１４７】本実施の形態によれば、情報蓄積用容量素子の下部電極７４が島形であっても表面の平坦化を達成することができる。その結果、フォトリソグラフィの制約を解消でき、島形の下部電極７４の高さを高くして所望の蓄積電荷量を確保できる。

【０１４８】なお、本実施の形態では、図５１においてメモリセルアレイ領域と周辺回路領域との間の凹部を厚膜のＳＯＧ膜７９を塗布することにより平坦化する例を示したが、図５２および図５３に示すように、フォトレジスト膜７７を除去した後、厚さ７００nmの酸化シリコン膜８０をＣＶＤ法により形成し（図５２）、その後、酸化シリコン膜８０の表面をＣＭＰ法により研磨して平坦化を行ってもよい（図５３）。なお、酸化シリコン膜８０は、島形の下部電極７４の高さより厚くなるように設定する。その後の工程は実施の形態１と同様に行うことができる。

【０１４９】なお、本実施の形態では島形の下部電極７４にタングステンを用いた例を示したが、これに限定されるものではなく窒化チタンやその他の金属あるいは金属化合物であってもよい。また、形成方法についてもスパッタ法に限定されるものではなくＣＶＤ法であってもよい。

【０１５０】（実施の形態６）本実施の形態では、情報蓄積用容量素子の形成方法について図５４～図５５を用いて説明する。図５４および図５５は上部に開口を有する筒形の情報蓄積用容量素子の一例を示す断面図である。

【０１５１】本実施の形態のＤＲＡＭは、実施の形態１におけるＤＲＡＭと情報蓄積用容量素子の部分を除きほぼ同一である。従って、その同一の部分についての説明は省略する。

【０１５２】図５４（ａ）は、窒化シリコン膜４６に形

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成した、窒化チタンからなる金属プラグ８１上に上部に開口を有する筒形の下部電極となる窒化チタン膜８２を形成し、その表面を酸化して酸化チタン膜８３を形成した状態を示している。金属プラグ８１および窒化チタン膜８２の形成は、前記した実施の形態の金属プラグ７１および窒化チタンからなる下部電極７２と同様である。

【０１５３】図５４（ｂ）は、さらに酸化タンタル膜８４を形成した状態を示している。

【０１５４】上部に開口を有する筒形の情報蓄積用容量素子を実現する上で重要な点は、上部に開口を有する筒形の下部電極の作成方法にある。すでに実施の形態１で説明したように、下部電極６０を円筒形に形成する場合、まず母材となる酸化シリコン膜５３に溝５５を形成し、その溝５５の側壁及び底部に下部電極材料を残存させることにより形成する。この時、下部電極材料の段差被覆性の良否が上部に開口を有する筒形の下部電極６０の実現の可否を左右する。すなわち、段差被覆性が悪いと溝５５の底部領域の膜厚が薄くなってしまい母材をエッチング除去した際に下部電極６０が倒壊してしまい、その形成が困難となる。従って、上部に開口を有する筒形の下部電極の実現には電極材料堆積時の段差被覆性が良いことが必須条件である。このような特性を有する電極材料としては四塩化チタンとアンモニアを原料としてＣＶＤ法により生成する窒化チタン膜を例示することができる。

【０１５５】したがって本実施の形態では窒化チタン膜８２による下部電極を形成する。以下に製造方法を説明する。

【０１５６】窒化チタン膜８２の形成後、７５０℃の窒素雰囲気中で３分熱処理を行う。この熱処理は、窒化チタンの再結晶化を促進させることを目的としており、後で行なう酸化タンタル膜に対する熱処理温度より高い温度で実施することが望ましい。その後、窒化チタン膜８２の表面に厚さ５㎚の酸化チタン膜８３を形成する。

【０１５７】次に、誘電体として厚さ１５㎚の酸化タンタル膜８４をＣＶＤ法により形成する。その後、７２５℃のアルゴン雰囲気中で３分熱処理し、酸化タンタルを結晶化させる。さらに４００℃のオゾン雰囲気中で５分熱処理し、酸化タンタルの酸化改質を行なう。この後、実施の形態１と同様に窒化チタン膜を形成し上部電極を形成して情報蓄積用容量素子を構成することができる。

【０１５８】図５５は、下部電極となる窒化チタン膜の表面に酸化チタン膜を形成する処理を酸化タンタル膜の形成後に行なう手順を示している。

【０１５９】窒化チタン膜８５で上部に開口を有する筒形の下部電極を形成した後、窒素雰囲気中で７５０℃、３分間の熱処理を施し、厚さ１５㎚の酸化タンタル膜８６を堆積する。

【０１６０】次に、７２５℃のアルゴン雰囲気中で３分間熱処理し、酸化タンタル膜８６を結晶化させた後、４００℃のオゾン雰囲気中で熱処理した。このとき酸化タンタル膜８６の改質と同時に下地の窒化チタン膜８５の表面に厚さ３～５㎚の酸化チタン膜８７が形成されるように熱処理時間を制御できる。この後、前記同様の上部電極を形成し情報蓄積用容量素子を構成することができる。

【０１６１】図５６は、上記した方法で得られた情報蓄積用容量素子の特性の一例を示している。半導体記憶装置に用いる情報蓄積用容量素子に要求される重要な特性の一つに実効膜厚がある。実効膜厚は、容量絶縁膜の材料の如何に係らず二酸化シリコンからなることを仮定して、その情報蓄積用容量素子の有する容量から得られる電気的膜厚を示す。実効膜厚が薄いほど大きな容量が得られることになる。

【０１６２】図５６は、酸化タンタルをアルゴン雰囲気中で熱処理した時の熱処理温度（横軸）と実効膜厚（縦軸）の関係を示している。図中Ａは酸化タンタルの物理的膜厚が２０㎚の場合を、Ｂは１０㎚の場合を各々示している。いずれの場合も熱処理温度が高くなるのに伴なって実効膜厚が薄くなっている。７２５℃では、Ｂの場合で実効膜厚が0.９㎚を示している。これは、例えば従来の情報蓄積用容量素子における実効膜厚が３㎚で、そのときに必要な円筒電極の高さが６００㎚であったとすると、実効膜厚0.９㎚では円筒電極の高さを約２００㎚まで低くできることを意味しており、半導体記憶装置としての製造工程の構築において極めて大きな利点となる。すなわち、情報蓄積用容量素子の高さを低減して製造工程における加工の難易度を低減することが可能となる。

【０１６３】本実施の形態によれば、下部電極としてにＣＶＤ法で形成する窒化チタン膜８２、８５を用いているので上方に開口を有する筒形の下部電極の形成が容易となり、かつ窒化チタンはシリコンを含有していないため、その上層に酸化タンタル膜８４、８６が形成された状態で熱処理を行っても、誘電率の低い二酸化シリコンが生成されることがない。このため実効膜厚を薄くでき、大きな容量を得ることができる。

【０１６４】（実施の形態７）本実施の形態では情報蓄積用容量素子の高さが高くなった時に生じる情報蓄積用容量素子の倒壊防止方法について図５７および図５８を用いて説明する。

【０１６５】図５７および図５８は、本実施の形態の製造方法をその工程順に説明した一部断面図である。

【０１６６】本実施の形態の製造方法は、実施の形態１の図３１までの工程については同様である。

【０１６７】次に、図５７に示すように、窒化シリコン膜４６の所定の領域に埋込まれた金属プラグ７１に接続するように酸化シリコン５３に溝５５を形成した後、前記した窒化チタン膜８８を前面に形成し、溝５５内を有機物８９で充填する。有機物８９としては、フォトレジ

ストもしくはポリイミドイソインドロキュナゾリンジオンの如きポリイミド樹脂を例示できる。

【０１６８】次に、図５８に示すように、酸化シリコン５３上に露出している窒化チタン膜８８を除去し、溝５５内にのみ窒化チタン膜８８を残存させる。また、溝５５内を充填した有機物８９をも除去した後、前記した実施の形態と同様に酸化タンタルからなる容量絶縁膜（図示せず）を形成し、上部電極として窒化チタン膜９０を形成し、情報蓄積用容量素子を形成する。

【０１６９】その後、実施の形態１と同様に層間絶縁膜を形成し、実施の形態１と同様のプラグ６７および第２層配線６８を形成することができる。なお、本実施の形態では、メモリセルアレイ領域と周辺回路領域との間には凹部が形成されないため、層間絶縁膜の一部にＳＯＧ膜を用いる必要はない。

【０１７０】本実施の形態によれば、上部に開口を有する筒形の下部電極を形成するために用いた母材である酸化シリコン膜５３を除去せずに、支えとしてそのまま残すため、下部電極である窒化チタン膜８８が倒壊することがない。また、メモリセルアレイ領域と周辺回路領域の境界に生じる段差は、上部電極である窒化チタン膜９０の膜厚分でせいぜい１００㎚であり、上層配線を形成するためのフォトリソグラフィにおいては、ほとんど問題にならない。さらに、支えとして母材を残すので情報蓄積用容量素子が相対的に細くなっても倒壊することがないので高さを高くして容量の拡大を図ることができる。

【０１７１】（実施の形態８）本実施の形態では、情報蓄積用容量素子の高さを高くしてなおかつ容量の増大を図ることができる方法について図５９～図６３を用いて説明する。

【０１７２】図５９～図６３は、本実施の形態の製造方法をその工程順に説明した一部断面図である。

【０１７３】本実施の形態の製造方法は、実施の形態７の下部電極である窒化チタン膜８８の形成までは同様である（図５９）。

【０１７４】その後、図６０に示すように、母材として用いた酸化シリコン膜５３を元の厚さの３割程度残るようにエッチングして除去する。さらに前記した容量絶縁膜の形成方法に基き酸化タンタル膜（図示せず）を形成して熱処理を施した。その状態で周辺回路領域の所定の位置に、リソグラフイとドライエッチングを用いて接続孔９１を設け、フォトレジスト膜を除去した後窒化チタン膜を全面に形成して情報蓄積用容量素子の上部電極９０と周辺回路のプラグ９２を同時に形成する。

【０１７５】次に、図６１に示すように、厚さ５０㎚程度の窒化シリコン膜９３を全面に形成し、先に除去した酸化シリコン膜５３の除去膜厚分の膜厚を有する新たな酸化シリコン膜９４をＣＶＤ法により半導体基板１の全面に堆積する。

【０１７６】その後、実施の形態１と同様にフォトレジスト膜９５を形成しメモリセルアレイ領域の酸化シリコン膜９４を除去する。

【０１７７】次に、図６２に示すように、フォトレジスト膜９５を除去した後、ＳＯＧ膜９６を形成して表面を平坦化する。ＳＯＧ膜９６の形成は実施の形態１の厚膜のＳＯＧ膜６５の形成と同様にできる。

【０１７８】最後に、厚さ１００㎚の酸化シリコン膜９７をＣＶＤ法により形成した後、所定の領域にスルーホール９８を形成して、プラグ９９を形成し、第２層配線１００を形成する。スルーホール９８、プラグ９９および第２層配線１００の形成は、実施の形態１と同様に行うことができる。

【０１７９】本実施の形態によれば、情報蓄積用容量素子の底部領域にのみ母材となる絶縁膜を残すことにより、母材が残った情報蓄積用容量素子の底部領域は溝形情報蓄積用容量素子となり、母材が除去された上部領域は上部に開口を有する筒形の情報蓄積用容量素子として構成できるので、情報蓄積用容量素子の高さを高くしても倒壊を防止しつつ、且つ容量の増大を図ることができる効果がある。また、周辺回路領域のプラグ９２を上部電極９０と同じ工程で形成できるので、スルーホール９８の深さを浅くすることができドライエッチングをより容易に行うことができる効果もある。

【０１８０】以上、本発明者によってなされた発明を発明の実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることは言うまでもない。

【０１８１】たとえば、前記実施の形態では、下部電極として多結晶シリコン膜を用いた例を示したが、図６４に示すような表面に半球状シリコン１０１を有する下部電極としてもよい。この場合、下部電極の高さを減じて工程を容易にすることができ、あるいは蓄積電荷量を増加させることができる。

【０１８２】

【発明の効果】本願において開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば以下のとおりである。

【０１８３】（１）立体化キャパシタを形成してもメモリセルアレイ領域と周辺回路領域との間に段差を生じない技術を提供できる。

【０１８４】（２）立体化キャパシタの形成によるメモリセルアレイ領域と周辺回路領域との間の段差を解消する技術を提供し、フォトリソグラフィの困難性を解消することができる。

【０１８５】（３）立体化キャパシタの形成によるメモリセルアレイ領域と周辺回路領域との間の段差を解消する技術を提供し、その上層に形成される配線層の断線あるいはパターニングの不良による短絡を防止できる。

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【０１８６】（４）キャパシタの容量確保、および高い信頼度をともに実現した半導体集積回路装置を提供できる。

【０１８７】（５）立体化キャパシタが高くなることによる製造工程途中でのキャパシタ電極の倒壊を防止する技術を提供し、半導体集積回路装置の製造歩留まりを向上できる。

【０１８８】（６）高い蓄積容量値を有する立体化キャパシタを提供し、立体化キャパシタの高さを低減してキャパシタの容量確保、および高い信頼度をともに実現した半導体集積回路装置を提供できる。

【０１８９】（７）メモリセルアレイ領域と周辺回路領域との間の段差を解消することにより、より深くなる周辺回路領域の接続孔のアスペクト比を緩和し、周辺回路領域の接続孔の加工を容易にすることができる。

【０１９０】（８）上下電極が段差被覆性に優れた窒化チタンからなり、誘電体も段差被覆性に優れた酸化タンタルからなる組み合わせで情報蓄積用容量素子を構成しているので、電極の高さを制約することなく情報蓄積用容量素子を実現できる。

【０１９１】（９）半導体記憶装置の集積度が向上し個々のメモリセルに許容される平面的面積が縮小されても、情報蓄積用容量素子の高さを高くすることにより容量の確保を図ることが可能で、信頼性の高い半導体記憶装置を提供できる。

【図面の簡単な説明】

【図１】本発明の一実施の形態であるＤＲＡＭを形成した半導体チップの全体平面図である。

【図２】本発明の実施の形態１であるＤＲＡＭの等価回路図である。

【図３】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図４】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図５】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図６】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図７】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図８】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図９】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１０】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１１】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１２】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１３】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１４】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１５】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１６】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１７】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１８】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図１９】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２０】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２１】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２２】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２３】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２４】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２５】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２６】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２７】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２８】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図２９】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図３０】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図３１】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図３２】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図３３】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図３４】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図３５】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図３６】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

【図３７】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。

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【図３８】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。
【図３９】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。
【図４０】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。
【図４１】本発明の実施の形態１であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。
【図４２】本発明の実施の形態２であるＤＲＡＭを示す半導体基板の要部断面図である。
【図４３】本発明の実施の形態２であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。
【図４４】本発明の実施の形態２であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。
【図４５】本発明の実施の形態３であるＤＲＡＭの製造方法を示す半導体基板の要部断面図である。
【図４６】本発明の実施の形態４であるＤＲＡＭを示す半導体基板の要部断面図である。
【図４７】本発明の実施の形態５であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図４８】本発明の実施の形態５であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図４９】本発明の実施の形態５であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５０】本発明の実施の形態５であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５１】本発明の実施の形態５であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５２】本発明の実施の形態５であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５３】本発明の実施の形態５であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５４】（ａ）および（ｂ）は、本発明の実施の形態６であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５５】（ａ）および（ｂ）は、本発明の実施の形態６であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５６】本発明の実施の形態６のＤＲＡＭの情報蓄積用容量素子を構成する容量絶縁膜の性能を示すグラフである。
【図５７】本発明の実施の形態７であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５８】本発明の実施の形態７であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図５９】本発明の実施の形態８であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図６０】本発明の実施の形態８であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図６１】本発明の実施の形態８であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図６２】本発明の実施の形態８であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図６３】本発明の実施の形態８であるＤＲＡＭの製造方法を示す半導体基板の一部断面図である。
【図６４】情報蓄積用容量素子を構成する下部電極の一例を示す部分拡大断面図である。
【符号の説明】
１　半導体基板
１Ａ　半導体チップ
２　酸化シリコン膜
３　窒化シリコン膜
４　フォトレジスト膜
５　素子分離溝
５ａ　溝
６　薄い酸化シリコン膜
７　酸化シリコン膜
８　窒化シリコン膜
９　フォトレジスト膜
１０　ｎ型半導体領域
１１　ｐ型ウエル
１２　ｎ型ウエル
１３　ゲート酸化膜
１４　ゲート電極
１４Ａ　ゲート電極
１４Ｂ　ゲート電極
１４Ｃ　ゲート電極
１５　窒化シリコン膜
１６　フォトレジスト膜
１７　p^- 型半導体領域
１８　n^- 型半導体領域
１９　ｎ型半導体領域
２０　窒化シリコン膜
２０ａ　サイドウォールスペーサ
２１　フォトレジスト膜
２２　p^+ 型半導体領域
２３　n^+ 型半導体領域
２４　ＳＯＧ膜
２５　酸化シリコン膜
２６　酸化シリコン膜
２７　フォトレジスト膜
２８　コンタクトホール
２９　コンタクトホール
３０　プラグ
３１　酸化シリコン膜
３２　フォトレジスト膜
３３　フォトレジスト膜
３４　コンタクトホール
３５　コンタクトホール
３６　コンタクトホール

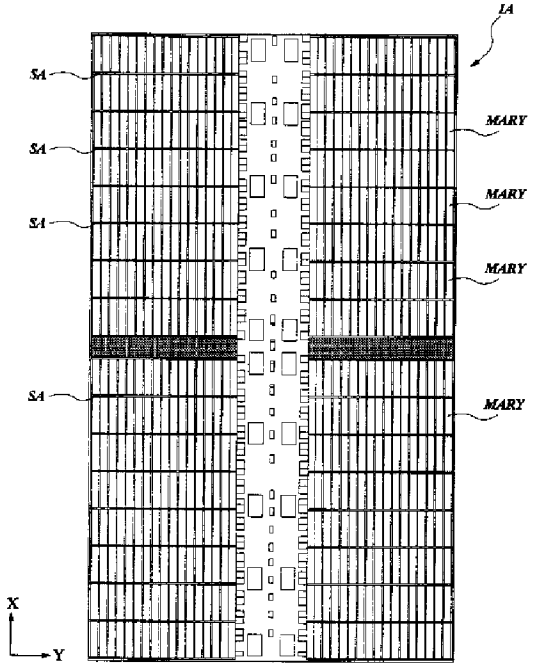
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３７　コンタクトホール
３８　第１層配線
４０　窒化シリコン膜
４１　フォトレジスト膜
４２　酸化シリコン膜
４３　サイドウォールスペーサ
４４　ＳＯＧ膜
４５　酸化シリコン膜
４６　窒化シリコン膜
４７　フォトレジスト膜
４８　スルーホール
４９　プラグ
５３　酸化シリコン膜
５４　フォトレジスト膜
５５　溝
５６　多結晶シリコン膜
５７　酸化シリコン膜
５８　フォトレジスト膜
６０　下部電極（Ta_2O_5 膜）
６１　容量絶縁膜（酸化タンタル膜）
６２　ＴｉＮ膜（上部電極）
６３　フォトレジスト膜
６４　酸化シリコン膜
６５　ＳＯＧ膜
６６ａ、６６ｂ　スルーホール
６７　プラグ
６８　第２層配線
６９　第２層配線
７０　金属プラグ
７１　金属プラグ
７２　下部電極
７３　フォトレジスト膜
７４　下部電極
７５　上部電極
７６　酸化シリコン膜
７７　フォトレジスト膜
７８　酸化シリコン膜
７９　ＳＯＧ膜
８０　酸化シリコン膜
８１　金属プラグ
８２　窒化チタン膜
８３　酸化チタン膜
８４　酸化タンタル膜
８５　窒化チタン膜
８６　酸化タンタル膜
８７　酸化チタン膜
８８　窒化チタン膜
８９　有機物
９０　上部電極（窒化チタン膜）
９１　接続孔
９２　プラグ
９３　窒化シリコン膜
９４　酸化シリコン膜
９５　フォトレジスト膜
９６　ＳＯＧ膜
９７　酸化シリコン膜
９８　スルーホール
９９　プラグ
１００　第２層配線
１０１　半球状シリコン
ＢＬ　ビット線
Ｃ　情報蓄積用容量素子
ＭＡＲＹ　メモリアレイ
Ｑｎ　ｎチャネル型ＭＩＳＦＥＴ
Ｑｐ　ｐチャネル型ＭＩＳＦＥＴ
Ｑｓ　メモリセル選択用ＭＩＳＦＥＴ
ＳＡ　センスアンプ
ＷＤ　ワードドライバ

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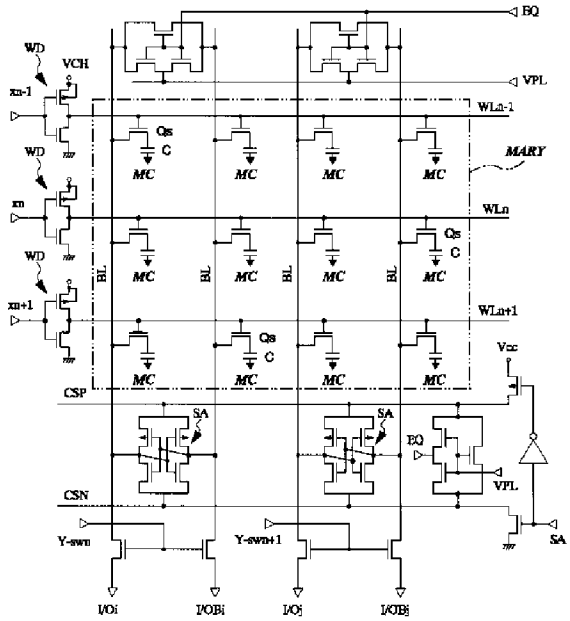
【図1】

図　1



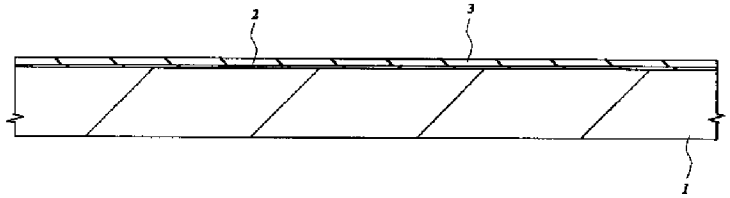
【図2】

図　2



【図3】

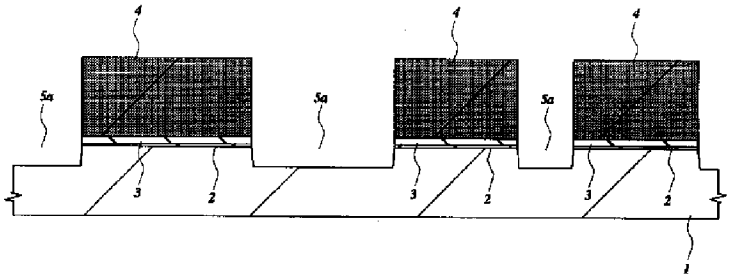
図　3



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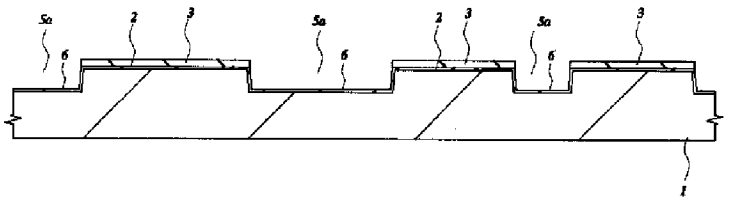
【図４】

図　4



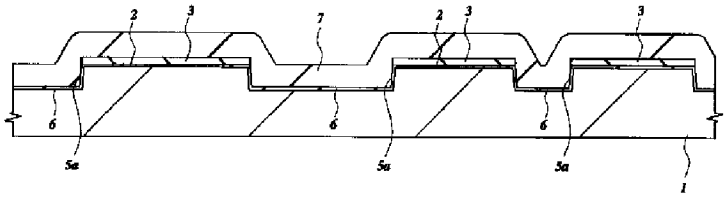
【図５】

図　5



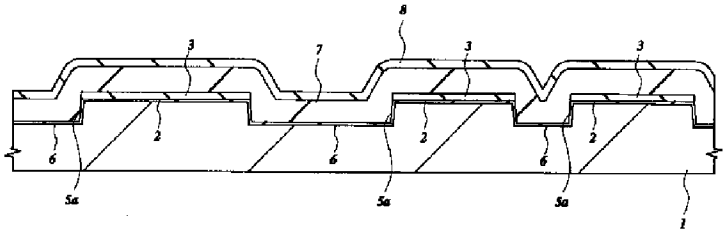
【図６】

図　6



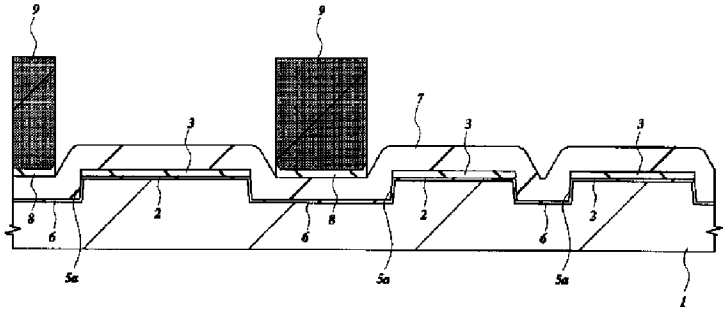
【図７】

図　7



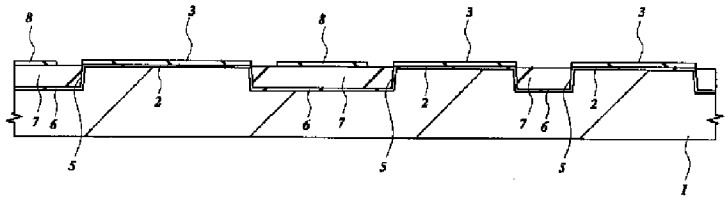
【図8】

図 8



【図9】

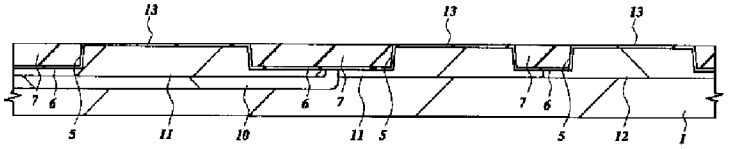
図 9



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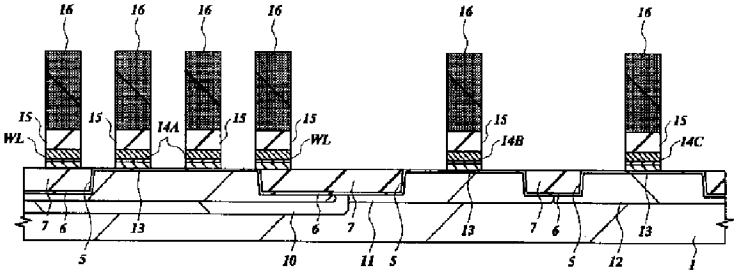
【図１０】

図　10



【図１１】

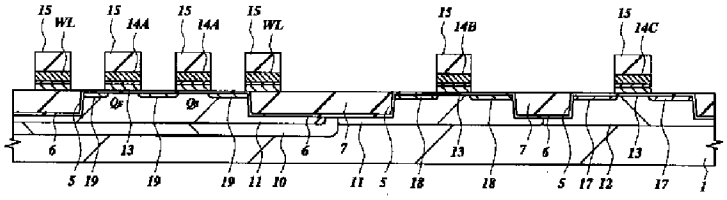
図　11



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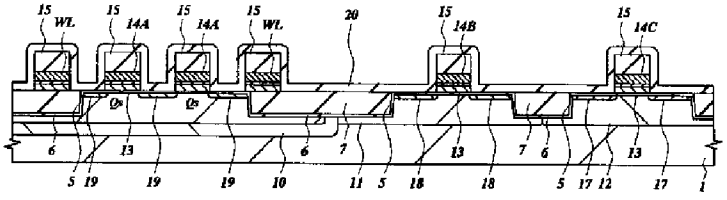
【図１２】

図　12



【図１３】

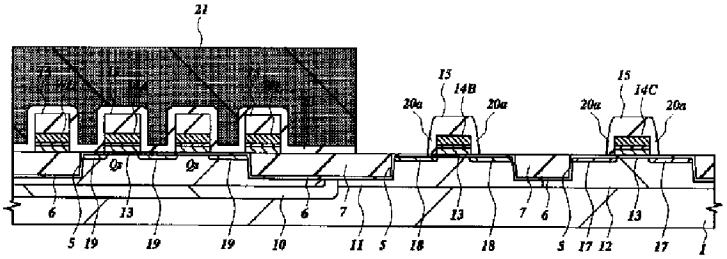
図　13



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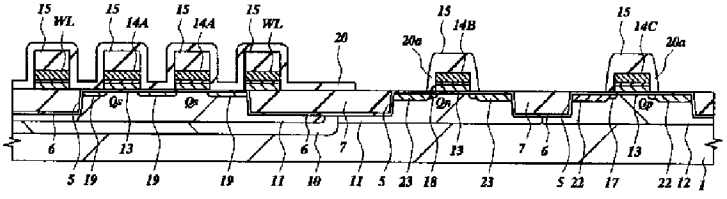
【図１４】

図　14



【図１５】

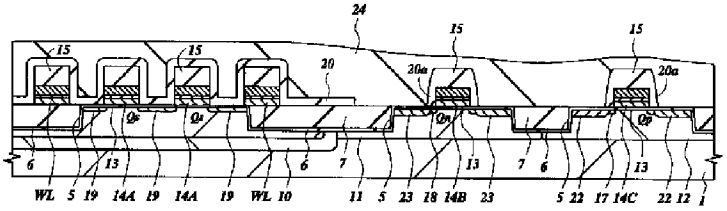
図　15



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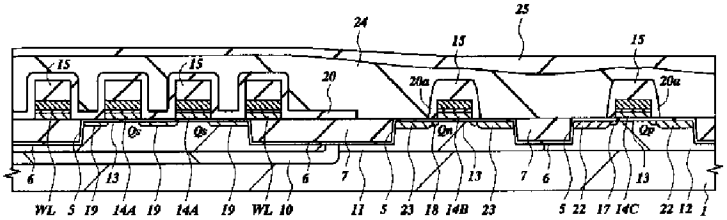
【図１６】

図 16



【図１７】

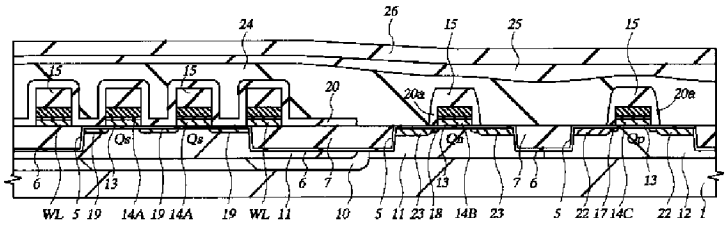
図 17



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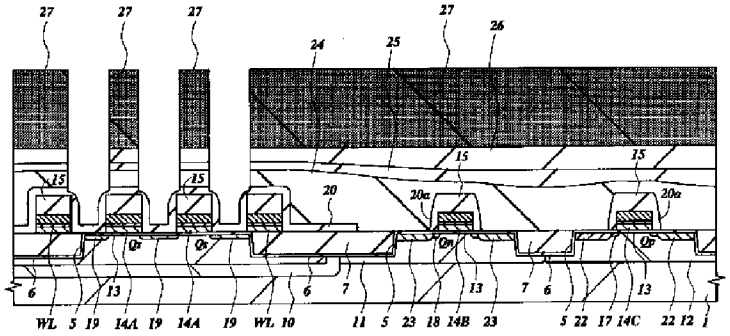
【図１８】

図　18



【図１９】

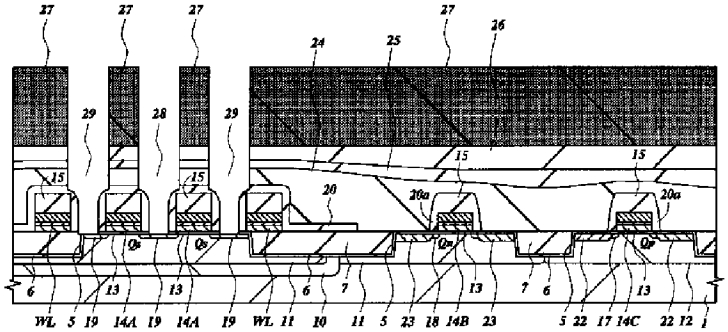
図　19



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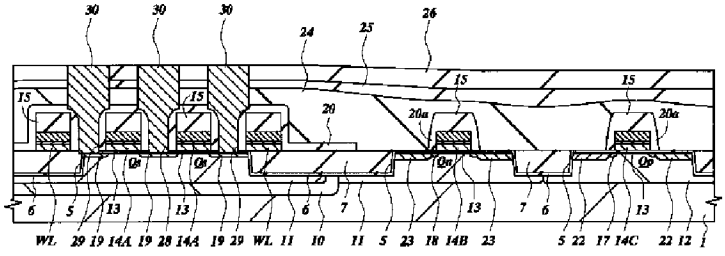
【図２０】

図　20



【図２１】

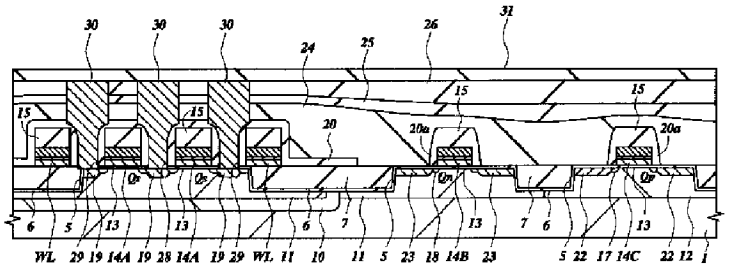
図　21



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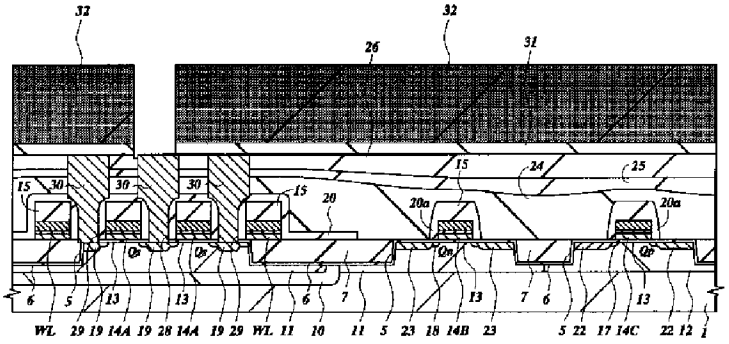
【図２２】

図　22



【図２３】

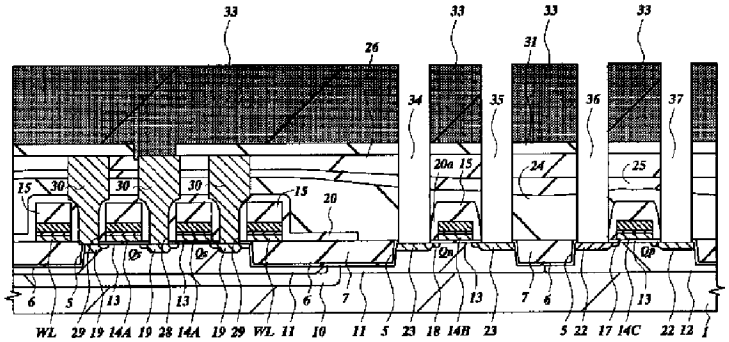
図　23



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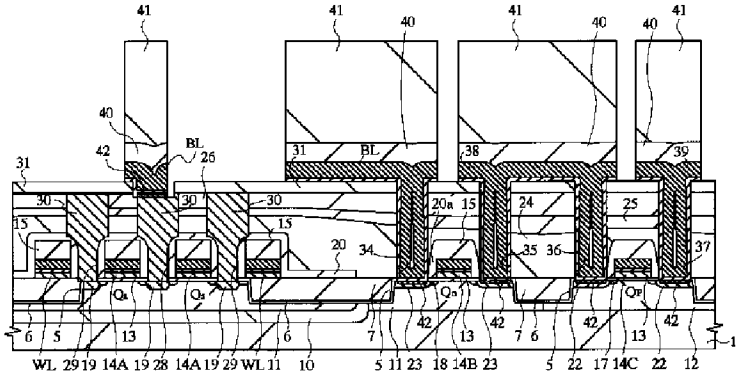
【図２４】

図　24



【図２５】

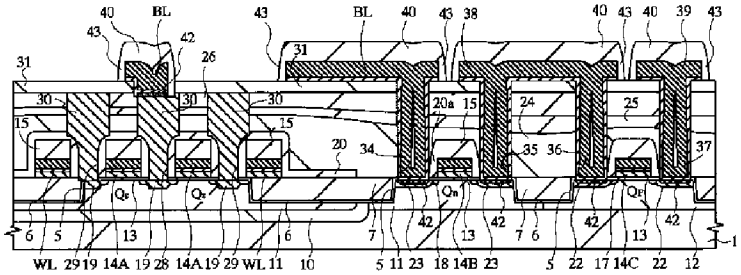
図　25



GF Exhibit 1126 - 968/2248

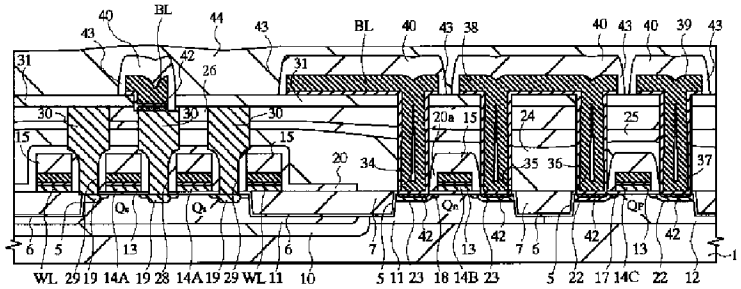
【図２６】

図　26



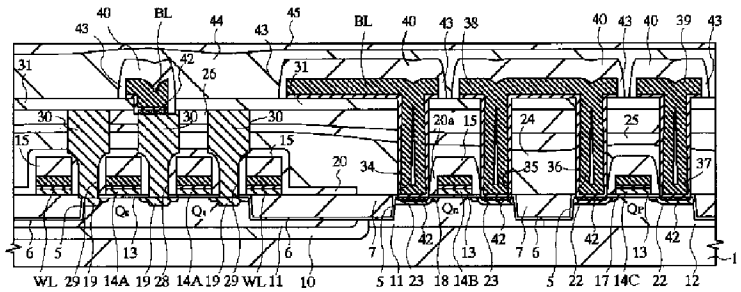
【図２７】

図　27



【図２８】

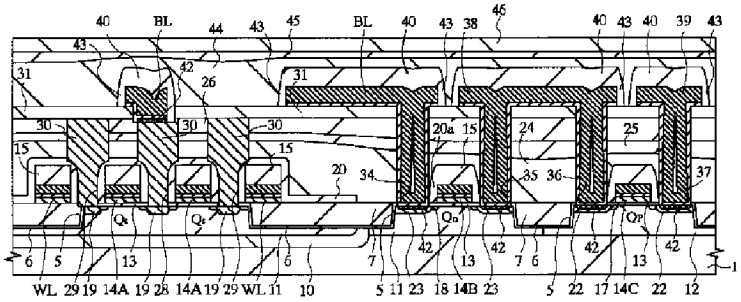
図　28



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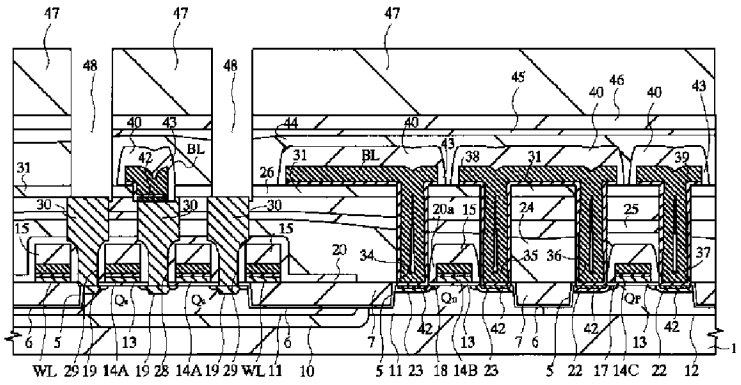
【図２９】

図　29



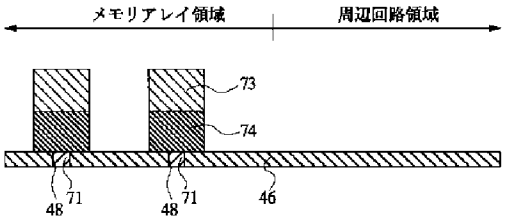
【図３０】

図　30



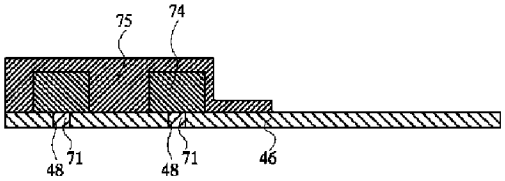
【図４７】

図　47



【図４８】

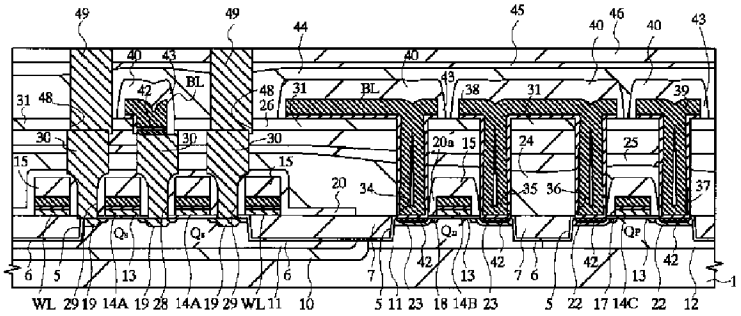
図　48



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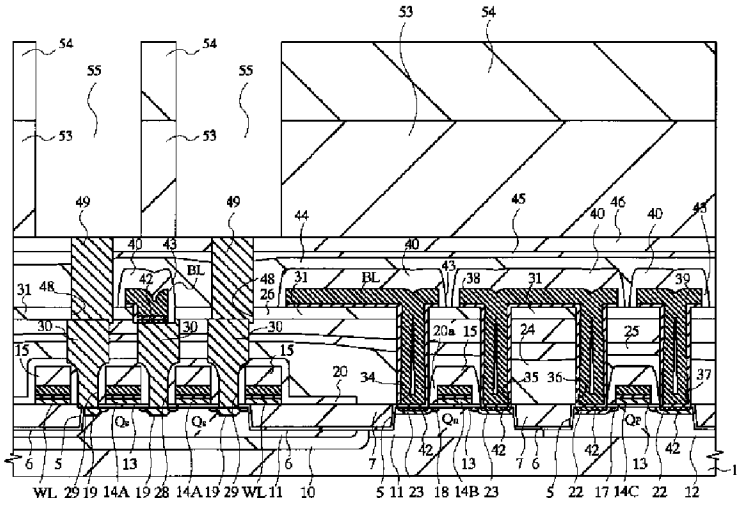
【図３１】

図 31



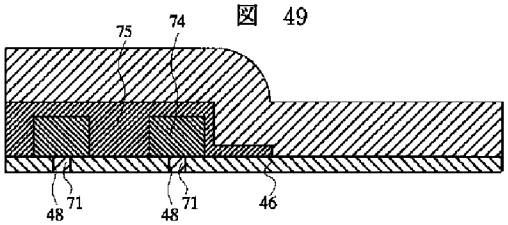
【図３２】

図 32



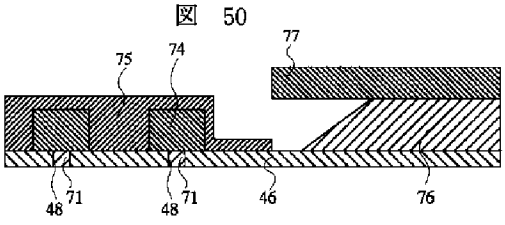
【図４９】

図 49



【図５０】

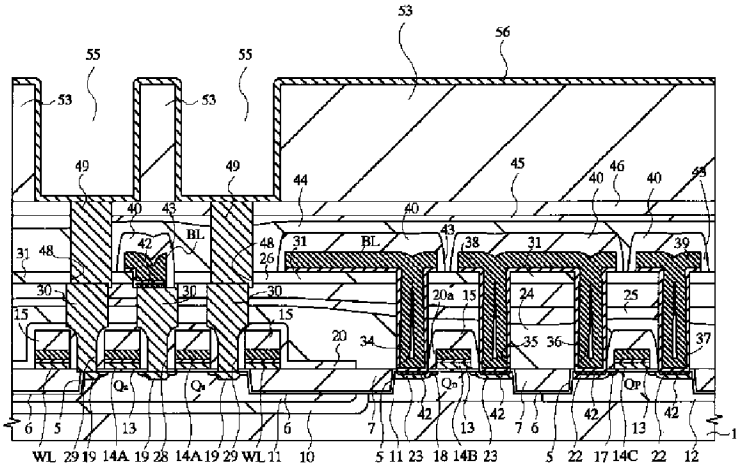
図 50



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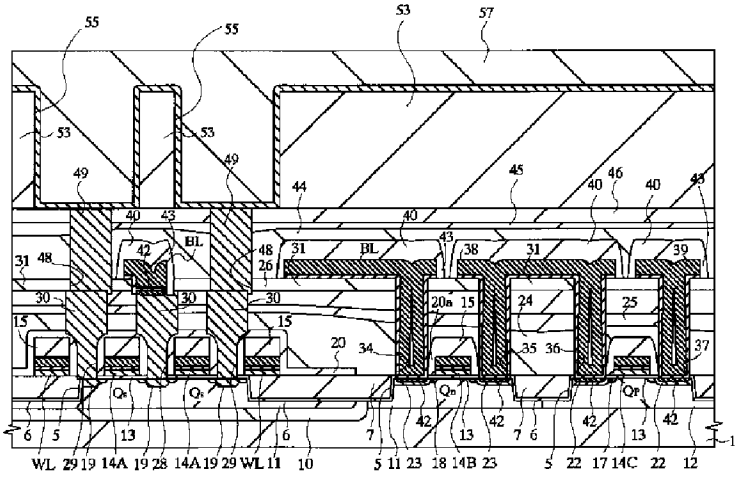
【図３３】

図　３３



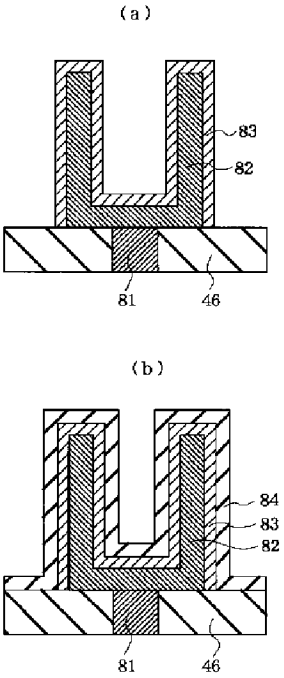
【図３４】

図　３４



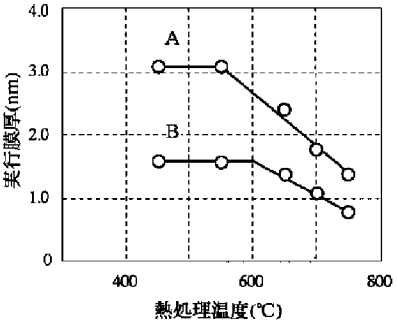
【図５４】

図　５４



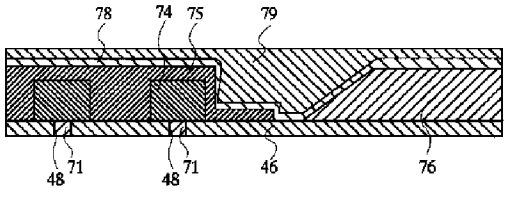
【図５６】

図　５６



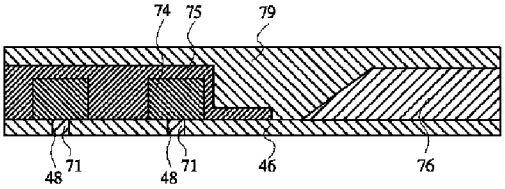
【図５１】

図　５１



【図５３】

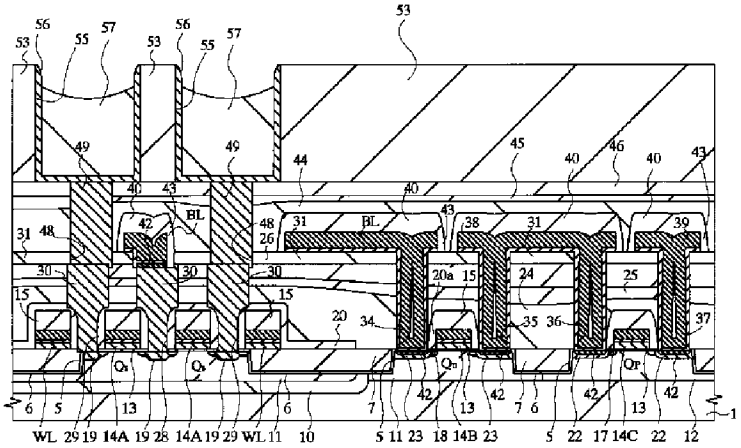
図　５３



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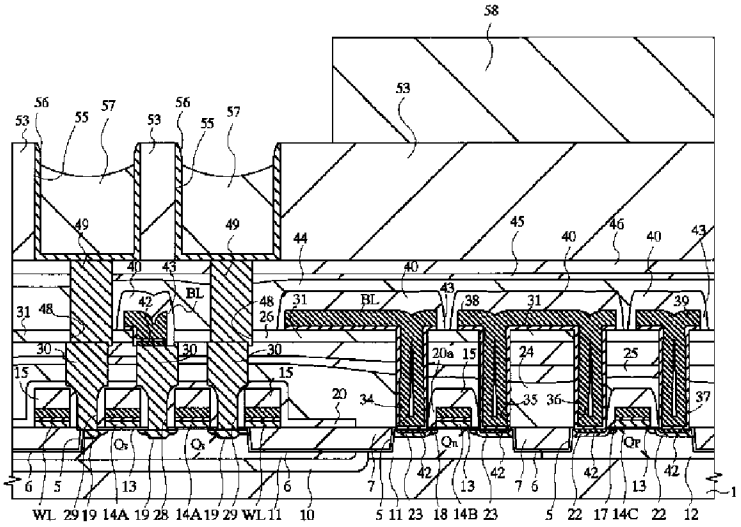
【図３５】

図 35



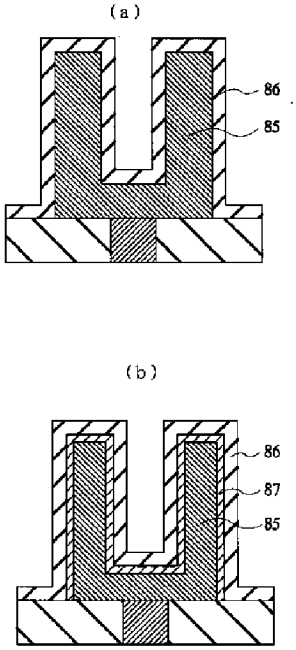
【図３６】

図 36



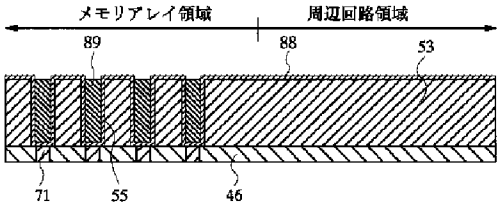
【図５５】

図 55



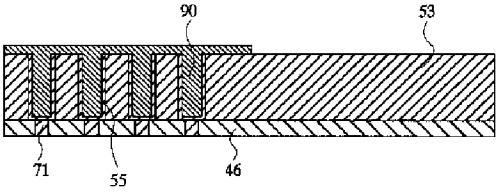
【図５７】

図 57



【図５８】

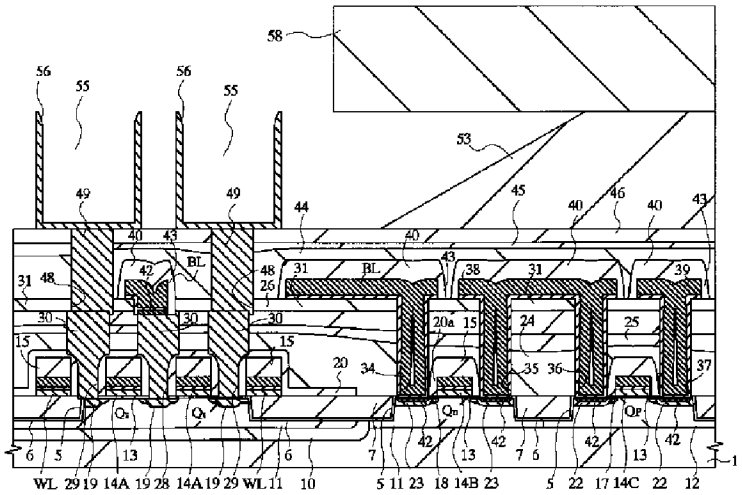
図 58



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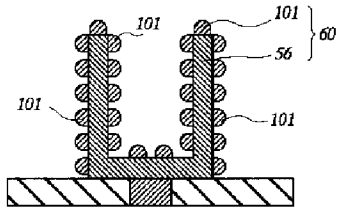
【図３７】

図 37



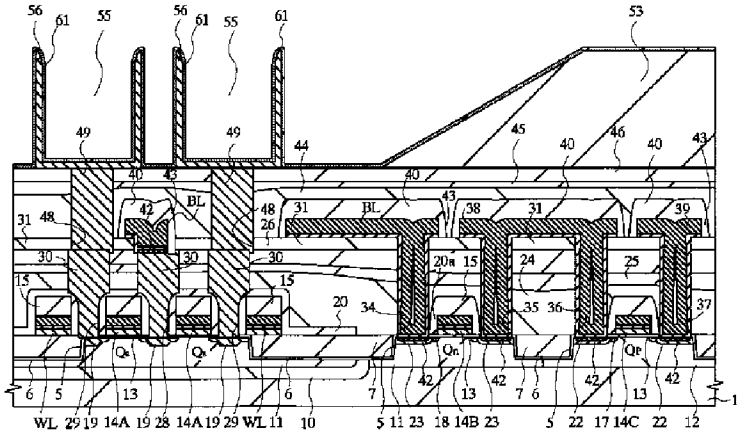
【図６４】

図 64



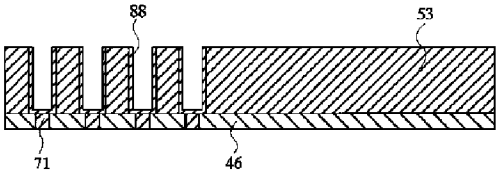
【図３８】

図 38



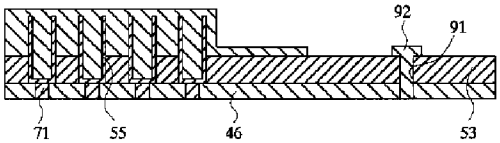
【図５９】

図 59



【図６０】

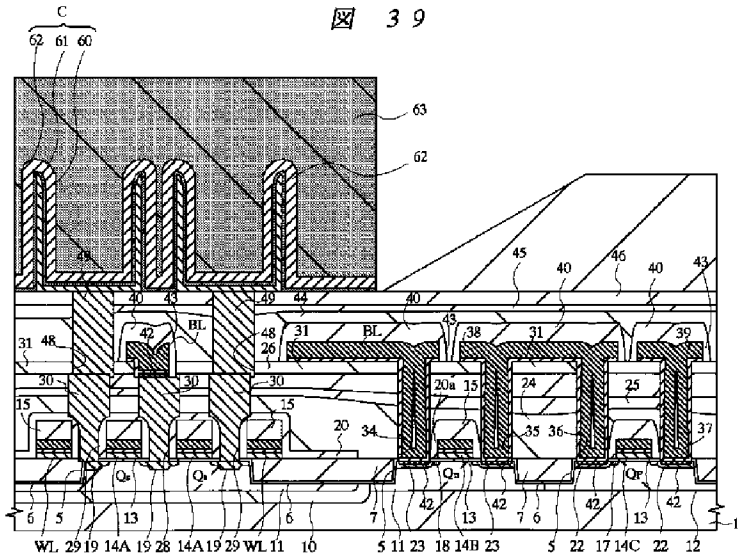
図 60



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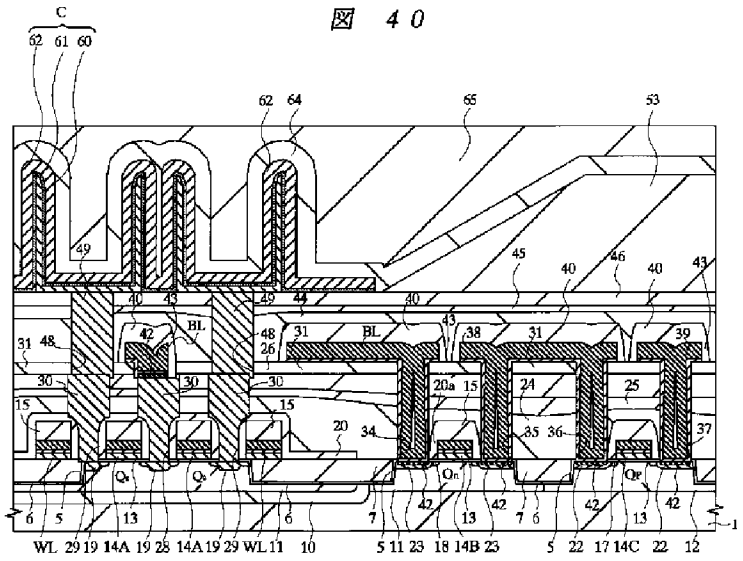
【図３９】

図　３９



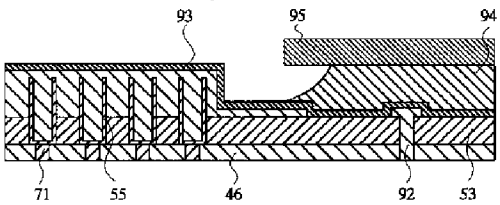
【図４０】

図　４０



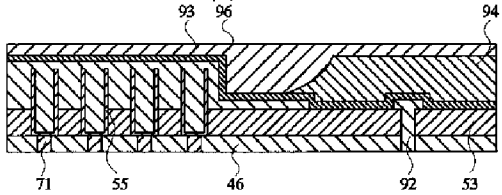
【図６１】

図　61



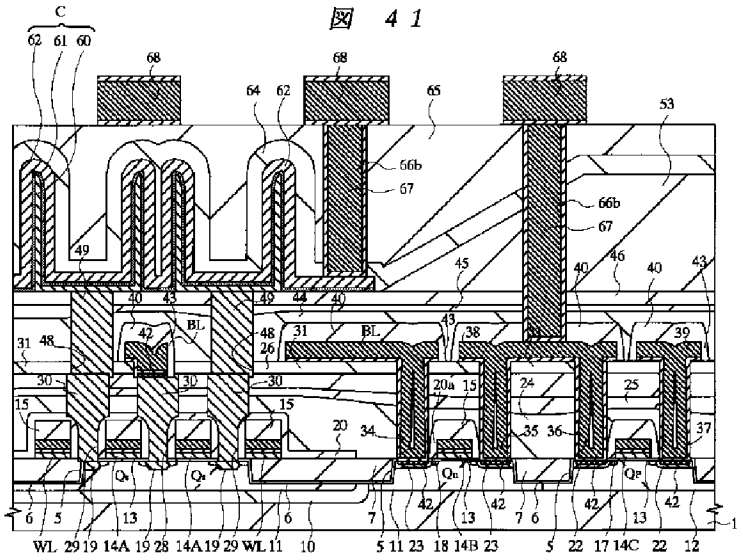
【図６２】

図　62



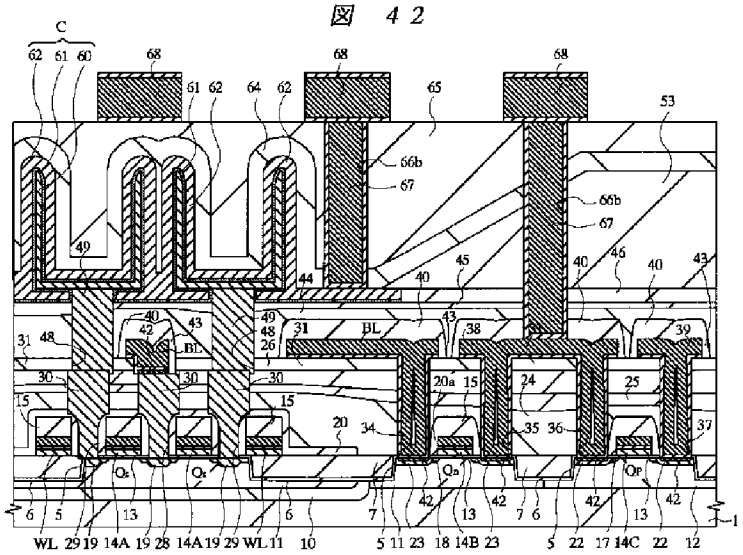
【図４１】

図　４１



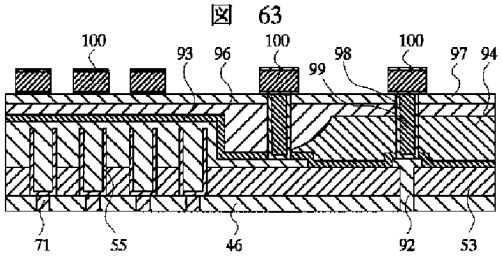
【図４２】

図　４２



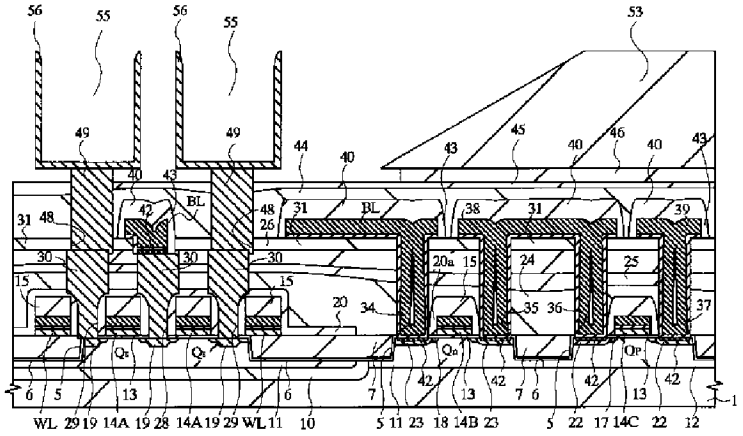
【図６３】

図　６３



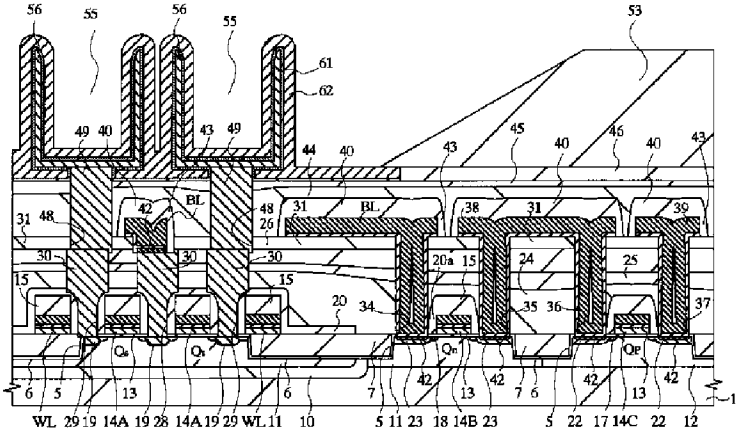
【図４３】

図　４３



【図４４】

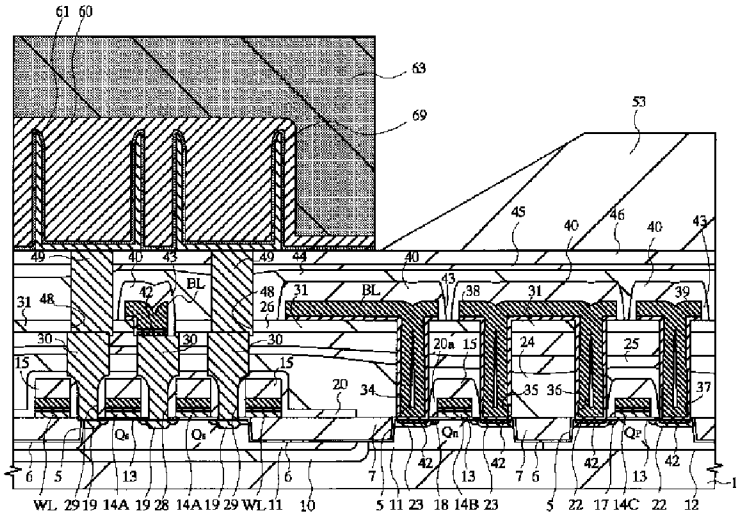
図　４４



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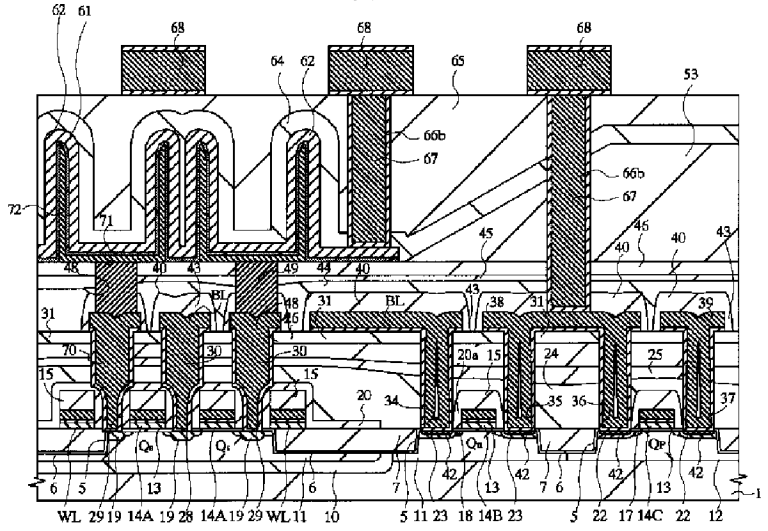
【図４５】

図　45



【図４６】

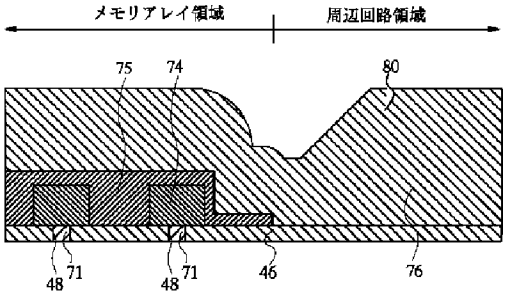
図　46



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【図５２】

図　52



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(72)発明者　金井　美鈴
東京都小平市上水本町五丁目20番１号　株
式会社日立製作所半導体事業部内

GF Exhibit 1126 - 979/2248

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JPH1126713A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURE THEREOF

Applicants: HITACHI LTD

Inventors: ASANO ISAMU,IIJIMA SHINPEI,KANAI MISUZU,SUGAWARA YASUHIRO

Classifications:
IPC ***H01L21/8242; H01L27/108;*** (IPC1-7): H01L21/8242; H01L27/108;

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Published as: JPH1126713A

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURE THEREOF

Abstract

PROBLEM TO BE SOLVED: To prevent the occurrence of the step difference between a memory array region and a surrounding circuit region, by forming an insulating film on a memory-cell selecting MISFET and the like, forming a groove in the insulating film, forming a conducting film in the groove or the like, etching the conducting film, and forming a lower electrode so that the conducting film remains only in the groove and so on. SOLUTION: On a memory-cell selecting MISFET and a surrounding circuit region, a silicon oxide film 45, a silicon nitride film 46, a silicon oxide film 53 are deposited. A groove is formed at the upper part of a through hole 48. Polycrystal silicon is formed in the groove. Then, a photoresist film covering the silicon oxide film 53 is formed in the surrounding circuit region. Then, the silicon oxide 53 and the like are etched, and a slant surface is formed. Thereafter, a lower electrode 60 is formed from polycrystalline silicon 56. Then, a Ta2 O3 film 61 and a TiN film 62 are formed, and an information storing capacitor element C, which is constituted of the lower electrode 60, is formed by patterning and the like. Then, a silicon oxide film 64 is deposited. An SOG film 65 is formed, and the surface is flattened.

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DESCRIPTION JPH1126713

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor integrated circuit device and a manufacturing technique thereof, and more particularly to an increase in storage capacity of a DRAM (Dynamic Random Access Memory) and a step difference between a memory cell array region and a peripheral circuit region which is generated in association therewith. It is related to the effective technology applied to the mitigation of.

[0002]

2. Description of the Related Art A memory cell of a DRAM is arranged at an intersection of a plurality of word lines and a plurality of bit lines arranged in a matrix on the main surface of a semiconductor substrate, and one memory cell selecting MISFET (Metal). Insulator Semiconductor Field Effect Transistor) and one information storage capacitive element (capacitor) connected in series with the Insulator Semiconductor Field Effect Transistor. The memory cell selection MISFET is formed in an active region surrounded by an element isolation region, and is mainly composed of a gate oxide film, a gate electrode integrally formed with a word line, and a pair of semiconductor regions forming a source and a drain. Has been done. The bit line is arranged above the memory cell selecting MISFET and is electrically connected to one of a source and a drain shared by two memory cell selecting MISFETs adjacent in the extending direction. The information storage capacitive element is similarly arranged above the memory cell selection MISFET and is electrically connected to the other of the source and the drain.

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[0003]

Japanese Unexamined Patent Publication No. 7-7084 discloses a DRAM having a Capacitor Over Bitline structure in which an information storage capacitive element is arranged above a bit line. In the DRAM described in this publication, in order to compensate for the decrease in the stored charge amount (Cs) of the information storage capacitive element due to the miniaturization of the memory cell, the lower electrode of the information storage capacitive element arranged above the bit line. By processing the (storage electrode) into a cylindrical shape, its surface area is increased, and the capacitive insulating film and the upper electrode (plate electrode) are formed on the upper surface thereof.

[0004]

However, in the memory cell having the COB structure, it is necessary to secure the operational reliability of the capacitor formed in the memory cell array region as a semiconductor memory device, and therefore, even if the integration degree of the device is improved and the cell area is reduced, it is considerable. Three-dimensionalization is essential. When the interlayer insulating film is formed after forming such a three-dimensional capacitor, a step corresponding to the height of the capacitor is generated between the memory cell array region and the peripheral circuit region.

[0005]

Such a step tends to become higher and higher as it is necessary to secure a certain capacitor capacity as the integration degree of DRAM increases. Further, due to the demand for higher integration of DRAM, higher exposure accuracy for photolithography is required, and the depth of focus allowed to satisfy such demand becomes more severe. There is a problem that it is difficult to form a wiring layer formed on the interlayer insulating film due to such an increase in the step and a decrease in the exposure focus margin in photolithography.

[0006]

The workability deterioration in the photolithography can be dealt with by mitigating the step, and the following techniques are known as techniques capable of mitigating such a step.

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[0007]

For example, the technique described in Japanese Patent Application Laid-Open No. 4-10651 or Japanese Patent Application Laid-Open No. 7-7084 is known.

A brief description of this technique is as follows. That is, the technique described in the above publication forms a standing wall (peripheral wall) or a channel formed simultaneously with the lower electrode (storage node) of the capacitor between the memory cell array region and the peripheral circuit region.

[0008]

A DRAM having such a standing wall or channel is formed as follows. First, after forming the selective MISFET of the DRAM and the MISFET of the peripheral circuit by a predetermined method, a bit line is formed through the interlayer insulating film, and further an interlayer insulating film covering the bit line is formed. Next, after depositing an insulating film having a film thickness corresponding to the height of the three-dimensional capacitor, holes are formed in the insulating film in the region where the lower electrode of the capacitor is formed, and at the same time, the memory cell array region and the peripheral circuit region are formed. A groove for forming a standing wall (peripheral wall) or a channel is formed in the boundary region with the. After that, a conductive film is deposited on the entire surface and only the conductive film on the insulating film is removed. Further, if the insulating film is removed, the conductive film in the hole becomes a lower electrode of a three-dimensional capacitor, and the conductive film in the groove is formed as a standing wall or a channel. If the insulating film to be removed when forming the lower electrode and the standing wall or channel of this capacitor is left only in the peripheral circuit region, a step is not formed between the memory cell array region and the peripheral circuit region and is deposited on the capacitor. The interlayer insulating film is flattened. The above publication discloses a method of using a resist mask or a method of using the conductive film as a mask for forming an insulating film which remains only in the peripheral circuit region. That is, in the technique disclosed in the above-mentioned publication, the formation end portion of the mask can be set at an arbitrary position within a region where a single wall or a plurality of vertical walls or channels are formed by allowing the vertical walls or channels to exist. It is supposed that the mask can be easily formed by increasing the margin of photolithography.

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[0009]
Further, for example, as described in “Easy ULSI Technology”, p155-p164, issued by Industrial Research Society on October 26, 1993, by coating and melting SOG (Spin On Glass) film or low melting point glass. A coating method, a heat treatment method using a glass flow, a method of applying a surface reaction mechanism of CVD (Chemical Vapor Deposition) to self-planarize, and the like are known. For example, Japanese Patent Laid-Open No. 7-122654 discloses BPSG (Boron-doped). There is disclosed a technique for reducing the step difference by combining the planarization by reflow of a Phospho-Silicate Glass) film and the planarization by a spin-on-glass film (SOG film).

[0010]
Further, for example, as described in May 22, 1996, Industrial Research Committee, "Electronic Materials", May 1996, p22 to p27, a photoresist sacrificial film, an SOG film, or a self-planarizing CVD. A method combining a film deposition and an etch back method and a CMP (Chemical Mechanical Polishing) method are known.

[0011]
However, the above-mentioned conventional technique has the following problems.

[0012]
That is, in the technique disclosed in Japanese Patent Application Laid-Open No. 4-10651 or Japanese Patent Application Laid-Open No. 7-7084, a standing wall or a channel is formed between the memory cell array region and the peripheral circuit region. Alternatively, there is a problem that the area for forming the channel is occupied and the chip size is increased.

[0013]
Further, in the coating method by coating and melting the SOG film or the low melting point glass, fine irregularities can be embedded (flattened), but recesses having a large area such as the peripheral circuit region cannot be embedded. No significant effect can be expected for the relief of the above steps.

[0014]
Further, a heat treatment method using a glass flow, for example, a reflow film of BPSG requires a high temperature heat treatment, and it should be taken into consideration that a metal-based material will be used as a material for a gate, a plug or a capacitor in a highly integrated DRAM in the future. If such a high temperature process is adopted, an unfavorable reaction of the metal-

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based material may occur, and the performance of the DRAM may not be improved.

[0015]
In addition, the method of applying the surface reaction mechanism of CVD for self-planarization is not preferable from the viewpoint of realizing a stable process because the process becomes complicated.

[0016]
Further, the technique for reducing the step difference by combining the flattening of the BPSG film by reflow and the flattening by the spin-on-glass film (SOG film) cannot eliminate the disadvantages due to the adoption of the high temperature process.

[0017]
Further, the method in which the deposition of the photoresist sacrificial film, the SOG film or the self-planarizing CVD film and the etch back method are combined, or the CMP method is not preferable because the steps are both complicated.

[0018]
An object of the present invention is to provide a technique in which a step is not formed between the memory cell array region and the peripheral circuit region even when the three-dimensional capacitor is formed.

[0019]
Another object of the present invention is to provide a technique for eliminating a step between the memory cell array region and the peripheral circuit region due to the formation of a three-dimensional capacitor, and to eliminate the difficulty of photolithography.

[0020]
Further, an object of the present invention is to provide a technique for eliminating a step between the memory cell array region and the peripheral circuit region due to the formation of a three-dimensional capacitor, and a short circuit due to a disconnection or a defective patterning of a wiring layer formed thereabove. Is to prevent.

[0021]

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It is another object of the present invention to provide a semiconductor integrated circuit device which realizes both high capacitance and high capacitance.

[0022]
Another object of the present invention is to provide a technique for preventing the capacitor electrodes from collapsing during the manufacturing process due to an increase in the height of the three-dimensional capacitor, and to improve the manufacturing yield of the semiconductor integrated circuit device.

[0023]
Another object of the present invention is to provide a three-dimensional capacitor having a high storage capacitance value, to reduce the height of the three-dimensional capacitor, to secure the capacitance of the capacitor, and to provide a semiconductor integrated circuit device with high reliability. To do.

[0024]
Another object of the present invention is to ease the aspect ratio of the connection hole in the peripheral circuit region, which is deepened by eliminating the step between the memory cell array region and the peripheral circuit region, and facilitate processing of the connection hole in the peripheral circuit region. To provide the technology to.

[0025]
The above and other objects and novel features of the present invention will be apparent from the description of this specification and the accompanying drawings.

[0026]
The typical ones of the inventions disclosed in this application will be briefly described as follows.

[0027]
(1) A method for manufacturing a semiconductor integrated circuit device according to the present invention includes: a memory cell selecting MISFET; and a cylindrical lower electrode that is connected in series with the memory cell selecting MISFET and has an opening at the top, at least the lower electrode. A memory cell is configured with a capacitive insulating film formed in contact with the inner surface of the cylindrical shape and an information storage capacitive

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element having at least an upper electrode formed opposite to the inner surface of the lower electrode through the capacitive insulating film. A method of manufacturing a semiconductor integrated circuit device having a memory cell array region in which memory cells are arranged and a peripheral circuit region around the memory cell array region, comprising: (a) a memory cell array region on a main surface of a semiconductor substrate; After the MISFET for cell selection and the MISFET for the peripheral circuit are formed in the peripheral circuit region of the main surface of the semiconductor substrate, the MISFET for memory cell selection and the MISFET for the peripheral circuit are formed on the upper surface of the first electrode having a film thickness corresponding to the height of the lower electrode. 1 step of depositing an insulating film, (b) a step of forming a groove by opening a first insulating film above the MISFET for memory cell selection, (c) an upper part of the first insulating film including the inside of the groove, A step of depositing a first conductive film which becomes a part of the lower electrode with a film thickness that does not fill the groove, (d) a second insulating film which fills the concave portion of the first conductive film formed in the groove, Exposing the first conductive film above the first insulating film, (e) etching the first conductive film to leave the first conductive film only inside the groove, (f) second insulating film filling the recess Is removed to form a lower electrode, (g) a step of forming a capacitive insulating film on the surface of the lower electrode, (h) a second conductive film is deposited on the capacitive insulating film, and the second conductive film is patterned. And a step of forming an upper electrode.

[0028]

According to such a method of manufacturing a semiconductor integrated circuit device, since the first insulating film deposited for forming the information storage capacitive element is left in the peripheral circuit region, a step is formed between the memory cell array region and the peripheral circuit region. Is not formed.

As a result, it is possible to increase the margin of photolithography in the subsequent steps and to stably process the opening of the connection hole and the like to cope with further miniaturization.

[0029]

(2) In the method for manufacturing a semiconductor integrated circuit device according to the present invention, after the step (f) of the method for manufacturing a semiconductor integrated circuit device according to (1), the upper layer portion of the first insulating film is removed and the lower electrode is formed. After the step of exposing a part of the upper part of the substrate and the step (h), a step of forming a third insulating film on the entire surface of the

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semiconductor substrate and flattening the surface is included.

[0030]

According to such a method of manufacturing a semiconductor integrated circuit device, a part of the upper part of the lower electrode is exposed, so that the first insulating film remains under the lower electrode.

For this reason, the first insulating film acts as a mechanical reinforcing member for the lower electrode, does not easily collapse even if the height of the lower electrode becomes high, and the lower electrode can be stably formed.

As a result, it is possible to increase the information storage capacitive element and increase the accumulated charge amount.

[0031]
(3) In the method of manufacturing a semiconductor integrated circuit device according to (2), a connection hole is opened in the peripheral circuit region of the first insulating film from which an upper layer portion is removed, and at the same time as the deposition of the second conductive film. A plug or a wiring may be formed by filling the connection hole and patterning the second conductive film in the peripheral circuit region at the same time as patterning the second conductive film.

[0032]

According to such a method of manufacturing a semiconductor integrated circuit device, since the plug or the wiring having a height corresponding to the height of the remaining first insulating film and the film thickness of the upper electrode is formed, for example, when the plug is formed, Can relax the depth of the connection hole in the peripheral circuit region and reduce the difficulty of processing the connection hole.

This is because when the insulating film remains in the peripheral circuit region or an insulating film is formed to eliminate the step difference from the memory cell array region, the insulating

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film in the peripheral circuit region has a relatively large film thickness. Although it becomes difficult to open the connection hole in the region, it contributes to alleviating the difficulty.

[0033]
(4) Further, in the method for manufacturing a semiconductor integrated circuit device of the present invention, after the step (e) of the method for manufacturing a semiconductor integrated circuit device according to (1), a photoresist for covering the first insulating film in the peripheral circuit region is provided. The step of forming a film and the removal of the second insulating film in the step (f) are performed simultaneously with the removal of the first insulating film in the memory cell array region by the wet etching method using the photoresist film as a mask, and the first insulating film is formed in the peripheral circuit region. After the step of forming a cylindrical lower electrode having an opening above while leaving a part of the film and step (h), a third insulating film is formed on the entire surface of the semiconductor substrate and the surface is flattened. It includes a process.

[0034]

According to such a method of manufacturing a semiconductor integrated circuit device, since the first insulating film is left in the peripheral circuit region, a step is not formed between the memory cell array region and the peripheral circuit region, and the subsequent process is performed. It is possible to increase the margin of the photolithography and stably process the opening of the connection hole or the like to cope with further miniaturization.

Further, since the first insulating film in the memory cell array region is removed by the wet etching method, a cylindrical lower electrode having an opening above is formed, and the surface area of the lower electrode can be increased to increase the accumulated charge amount. it can.

[0035]
(5) In the method for manufacturing a semiconductor integrated circuit device according to (4), the fourth insulating film having a different etching rate from the first insulating film and the second insulating film is formed on the semiconductor substrate before the deposition of the first insulating film. The method may include a step of depositing on the entire surface of, and etching and removing the fourth insulating film in the memory cell array region after the lower electrode is formed.

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[0036]

According to such a method for manufacturing a semiconductor integrated circuit device, the region in which the fourth insulating film was formed (a part of the plug connecting the MISFET for memory cell selection) can also be made to function as a capacitive element, The charge storage amount can be increased.

The information storage capacitive element formed in this manner has a cylindrical electrode formed of a part of a plug connecting the lower electrode and the memory cell selection MISFET and a capacitive insulating film formed on the outer periphery thereof. As a cylindrical capacitive element including the formed concentric cylindrical electrode, it is integrally formed with a cylindrical capacitive element having an opening above the cylindrical capacitive element.

[0037]

(6) A method of manufacturing a semiconductor integrated circuit device according to the present invention comprises a memory cell selecting MISFET and a cylindrical lower electrode and a lower electrode which are connected in series to the memory cell selecting MISFET and have an opening above. A memory cell array region in which a memory cell is formed by a capacitive insulating film formed on the surface and an information storage capacitive element having an upper electrode formed facing the lower electrode via the capacitive insulating film, and in which the memory cell is arranged. And a peripheral circuit region around the memory cell array region, comprising: (a) forming a memory cell selecting MISFET on a main surface of a semiconductor substrate; A step of forming a capacitive element, (b) a step of depositing a first insulating film on the main surface of a semiconductor substrate with a film thickness equal to or larger than the height corresponding to the height of the information storage capacitive element, (c) a peripheral circuit region Forming a photoresist film covering the first insulating film, and removing the first insulating film in the memory cell array region by a wet etching method using the photoresist film as a mask, (d) a third insulating film on the entire surface of the semiconductor substrate. It includes a step of forming a film and flattening the surface.

[0038]

According to such a method for manufacturing a semiconductor integrated circuit device, since the first insulating film is formed only in the peripheral circuit region, the step between the memory cell array region and the peripheral circuit region is eliminated, and the photolithography in the subsequent process is performed. It is possible to increase the margin of lithography and to stably process the opening of the connection hole or the like to cope with further miniaturization.

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[0039]
(7) The method for manufacturing a semiconductor integrated circuit device according to the present invention is the method for manufacturing a semiconductor integrated circuit device according to any one of (2) to (6), wherein the surface of the third insulating film is flattened. Is a flattening step by applying an SOG film.

[0040]
Alternatively, the step of flattening the surface of the third insulating film may be performed by flattening the insulating film deposited by vapor phase epitaxy with a film thickness equal to or greater than the height of the information storage capacitive element by CMP. It is a process.

[0041]

According to such a method of manufacturing a semiconductor integrated circuit device, it is possible to fill a groove (concave portion) between the peripheral circuit region and the memory cell array region by wet etching to achieve almost complete planarization.

Particularly, in the method of applying the SOG film, the steps are simple and the manufacturing can be facilitated.

[0042]
(8) Further, in the method for manufacturing a semiconductor integrated circuit device of the present invention, in the method for manufacturing a semiconductor integrated circuit device according to any one of (1) to (7), the second conductive film is deposited on the lower electrode. The surface is flattened by burying the recess formed by the cylindrical shape.

[0043]

According to such a method for manufacturing a semiconductor integrated circuit device, no recess is formed on the surface of the second conductive film, and if a recess is formed, it will occur at the bottom of the recess of the insulating film filling the recess. It is possible to prevent the occurrence of wax voids and improve the reliability of the semiconductor integrated circuit

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device.

When the semiconductor integrated circuit device is miniaturized and the information storage capacitive element is miniaturized, the recesses on the surface of the second conductive film are also considerably small, and voids and the like are likely to occur. The present invention is particularly effective in consideration of future miniaturization trends.

[0044]
(9) A semiconductor integrated circuit device according to the present invention comprises a memory cell selecting MISFET and a cylindrical lower electrode which is connected in series with the memory cell selecting MISFET and has an opening portion above, and at least a lower electrode having a cylindrical shape. A memory cell is constituted by a capacitive insulating film formed in contact with the inner surface and an information storage capacitive element having at least an upper electrode formed so as to face the cylindrical inner surface of the lower electrode via the capacitive insulating film. A semiconductor integrated circuit device having a memory cell array region in which cells are arranged and a peripheral circuit region around the memory cell array region, wherein an insulating film having a film thickness corresponding to the height of an information storage capacitive element is formed in the peripheral circuit region. In addition, the step difference between the memory cell array region and the peripheral circuit region is eliminated.

[0045]
Further, in the semiconductor integrated circuit device, the recess formed by the lower electrode forming the information storage capacitive element is filled with the upper electrode forming the information storage capacitive element.

[0046]
In the semiconductor integrated circuit device, the information storage capacitive element is formed above the memory cell selection MISFET, and the information storage capacitive element is one of plugs connecting the lower electrode and the memory cell selection MISFET. It is integrally formed with a cylindrical capacitive element including a cylindrical electrode composed of a portion and a concentric cylindrical electrode formed on the outer periphery of the cylindrical electrode via a capacitive insulating film.

[0047]
Such a semiconductor integrated circuit device can be manufactured by the manufacturing

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methods (1) to (8) described above.

[0048]
(10) The semiconductor integrated circuit device of the present invention includes a memory cell selecting MISFET, a memory cell selecting MISFET connected in series, a lower electrode, a capacitor insulating film formed in contact with the lower electrode, and a capacitor insulating film. What is claimed is: 1. A semiconductor integrated circuit device having a memory cell including an information storage capacitive element having an upper electrode formed opposite to a lower electrode with a conductive material in which both the lower electrode and the upper electrode include at least titanium nitride The capacitive insulating film is made of an insulating film containing at least polycrystalline tantalum oxide.

[0049]

According to such a semiconductor integrated circuit device, both the lower electrode and the upper electrode are made of a conductive material containing at least titanium nitride, and the capacitive insulating film is made of an insulating film containing at least polycrystalline tantalum oxide. It is possible to increase.

That is, polycrystalline tantalum oxide is a material with a high dielectric constant, and the oxide of titanium nitride of the lower electrode is a conductor, and the capacitance due to the formation of a silicon oxide film, as if a silicon material was used for the lower electrode. This is because there is no substantial increase in the film thickness of the insulating film and it is not necessary to form the silicon nitride film that prevents the formation of the silicon oxide film.

[0050]
(11) Further, in the semiconductor integrated circuit device according to (10), the plug connecting the MISFET for memory cell selection and the lower electrode can be made of a conductive material containing titanium nitride as a main component.

[0051]

According to such a semiconductor integrated circuit device, it is possible to reduce the resistance of the plug and improve the response speed (reading and writing speed of the

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memory) of the semiconductor integrated circuit device.

Since the main component of the plug is the same as titanium nitride, which is the material of the lower electrode, its affinity can be improved.

[0052]
(12) In the semiconductor integrated circuit device according to (10) or (11), a titanium oxide film having a thickness of 10 nm or less can be formed at the interface between the lower electrode and the capacitive insulating film.

[0053]

There are two types of such a titanium oxide film, that is, a tantalum oxide film that is a capacitive insulating film is formed by heat treatment in an oxygen atmosphere, and a titanium oxide film is formed in advance before the deposition of the tantalum oxide film.

In any case, the titanium oxide film is a conductive film and can increase the capacitance value and increase the amount of accumulated charges regardless of the increase in the film thickness of the capacitance insulating film.

[0054]
(13) A method of manufacturing a semiconductor integrated circuit device according to the present invention includes a memory cell selection MISFET, a memory cell selection MISFET connected in series, a lower electrode, a capacitor insulating film formed in contact with the lower electrode, and a capacitor. A method of manufacturing a semiconductor integrated circuit device having a memory cell including an information storage capacitive element having an upper electrode formed opposite to a lower electrode via an insulating film, comprising: (a) a lower electrode by a CVD method; A titanium nitride film is deposited, and the titanium nitride film is heat-treated in a non-oxidizing atmosphere. (B) A tantalum oxide film is deposited by a CVD method and heat-treated in a non-oxidizing atmosphere to crystallize the tantalum oxide film. The step of converting into a polycrystalline tantalum oxide film, (c) heat treating the polycrystalline tantalum oxide film in an oxidizing atmosphere to modify the polycrystalline tantalum oxide film and at the same time oxidize the interface between the titanium nitride film and the polycrystalline tantalum oxide film. It includes a step of forming titanium and (d) a step of depositing a titanium nitride film to be an upper electrode by a CVD method.

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[0055]
According to such a method of manufacturing a semiconductor integrated circuit device, the semiconductor integrated circuit devices of (10) to (12) described above can be manufactured.

[0056]
(14) Further, the method of manufacturing a semiconductor integrated circuit device according to (13) above may include a step of forming a titanium oxide film on the surface of the titanium nitride film after the step (a).

[0057]

According to such a method for manufacturing a semiconductor integrated circuit device, since the oxide film of titanium nitride is formed in advance before the deposition of the tantalum oxide film, the polycrystalline tantalum oxide film is heat-treated in an oxidizing atmosphere so that the polycrystalline oxide film is oxidized. Invasion of oxygen can be suppressed in the step of modifying the tantalum film.

If the oxide of titanium nitride is not formed, the volume of the titanium oxide film formed at the interface between the titanium nitride film and the polycrystalline tantalum oxide film increases, and stress is applied to the polycrystalline tantalum oxide film to Although it may be considered that the insulating property is hindered, such a problem can be suppressed in the case of the present invention.

[0058]
(15) A method of manufacturing a semiconductor integrated circuit device according to the present invention includes a memory cell selecting MISFET, a memory cell selecting MISFET connected in series, a lower electrode, a capacitor insulating film formed in contact with the lower electrode, and a capacitor. A method for manufacturing a semiconductor integrated circuit device having a memory cell including an information storage capacitive element having an upper electrode formed opposite to a lower electrode via an insulating film, comprising: a memory cell selecting MISFET and a lower electrode. Is formed at the same time as the bit line arranged above the memory cell selecting MISFET.

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[0059]
According to such a method of manufacturing a semiconductor integrated circuit device, the plug can be formed by the step of forming the bit line to simplify the step.

[0060]

BEST MODE FOR CARRYING OUT THE INVENTION Embodiments of the present invention will be described in detail below with reference to the drawings.

In all the drawings for explaining the embodiments, members having the same function are designated by the same reference numeral, and the repeated description thereof will be omitted.

[0061]

(Embodiment 1) FIG. 1 is an overall plan view of a semiconductor chip in which a DRAM of the present embodiment is formed.

As shown in the figure, on the main surface of the semiconductor chip 1A made of single crystal silicon, a large number of memory arrays MARY are arranged along the X direction (long side direction of the semiconductor chip 1A) and the Y direction (short side direction of the semiconductor chip 1A). Are arranged in a matrix.

A sense amplifier SA is arranged between the memory arrays MARY adjacent to each other along the X direction.

At the center of the main surface of the semiconductor chip 1A, a word driver WD, a control circuit such as a data line selection circuit, an input / output circuit, and a bonding pad are arranged.

[0062]

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FIG. 2 is an equivalent circuit diagram of the DRAM.

As shown in the figure, this DRAM memory array (MARY) has a plurality of word lines WL (WLn-1, WLn, WLn + 1 ...) Arranged in a matrix and a plurality of bit lines BL and their intersections. It is configured by a plurality of memory cells (MC) that are formed.

One memory cell for storing 1-bit information is composed of one information storage capacitive element C and one memory cell selecting MISFETQs connected in series with this.

One of a source and a drain of the memory cell selection MISFET Qs is electrically connected to the information storage capacitive element C, and the other is electrically connected to the bit line BL.

One end of the word line WL is connected to the word driver WD, and one end of the bit line BL is connected to the sense amplifier SA.

[0063]
Next, a method of manufacturing the DRAM of this embodiment will be described in the order of steps with reference to FIGS.

[0064]

First, as shown in FIG. 3, a p-type semiconductor substrate 1 having a specific resistance of about 10 Ωcm is wet-oxidized at about 850 ° C. to form a thin silicon oxide film 2 having a thickness of about 10 nm on the surface thereof. A silicon nitride film 3 having a thickness of about 140 nm is deposited on the silicon oxide film 2 by a CVD (Chemical Vapor Deposition) method.

The silicon oxide film 2 is formed to relieve stress applied to the substrate when sintering (baking) the silicon oxide film embedded in the element isolation trench in a later step.

Since the silicon nitride film 3 has a property of being hard to be oxidized, it is used as a mask for preventing the oxidation of the substrate surface below it (active region).

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[0065]

Next, as shown in FIG. 4, the silicon nitride film 3, the silicon oxide film 2 and the semiconductor substrate 1 are dry-etched using the photoresist film 4 as a mask, so that the depth of the semiconductor substrate 1 in the element isolation region is reduced to 300 to 300 nm. A groove 5a of about 400 nm is formed.

To form the groove 5a, the silicon nitride film 3 is dry-etched using the photoresist film 4 as a mask, the photoresist film 4 is removed, and then the silicon nitride film 3 is used as a mask to form the silicon oxide film 2 and the semiconductor substrate. 1 may be dry-etched.

[0066]

Next, after removing the photoresist film 4, as shown in FIG. 5, the semiconductor substrate 1 is wet at about 850 to 900 ° C. in order to remove the damage layer generated on the inner wall of the groove 5a by the etching. By oxidation, a thin silicon oxide film 6 having a film thickness of about 10 nm is formed on the inner wall of the groove 5a.

[0067]

Next, as shown in FIG. 6, after depositing a silicon oxide film 7 having a film thickness of about 300 to 400 nm on the semiconductor substrate 1, the semiconductor substrate 1 is dry-oxidized at about 1000 ° C. to be embedded in the groove 5a. Sintering is performed to improve the film quality of the silicon oxide film 7 thus formed.

The silicon oxide film 7 is deposited by a plasma CVD method using ozone (O3) and tetraethoxysilane (TEOS) as source gases, for example.

[0068]

Next, as shown in FIG. 7, after depositing a silicon nitride film 8 having a film thickness of about 140 nm on the silicon oxide film 7 by a CVD method, as shown in FIG. By dry etching the silicon

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film 8, the silicon nitride film 8 is left only on the upper portion of the groove 5a having a relatively large area such as the boundary between the memory array and the peripheral circuit.

The silicon nitride film 8 remaining on the upper portion of the groove 5a has a relatively large area inside the groove 5a when the silicon oxide film 7 is planarized by polishing the silicon oxide film 7 by the CMP method in the next step. It is formed in order to prevent a phenomenon (dishing) of being deeply polished as compared with the silicon oxide film 7 inside the groove 5a having a relatively narrow area.

[0069]

Next, after removing the photoresist film 9, as shown in FIG. 9, the silicon oxide film 7 is polished by the CMP method using the silicon nitride films 3 and 8 as stoppers and left inside the groove 5a. The element isolation groove 5 is formed.

[0070]

Next, after the silicon nitride films 3 and 8 are removed by wet etching using hot phosphoric acid, as shown in FIG. 10, the semiconductor substrate 1 in the region (memory array) where the memory cell is formed has n-type impurities, for example, P (phosphorus) is ion-implanted to form the n-type semiconductor region 10, and p-type impurities such as B (boron) are ion-implanted into a part of the memory array and the peripheral circuit (region where the n-channel type MISFET is formed). Then, a p-type well 11 is formed, and an n-type impurity, for example, P (phosphorus) is ion-implanted into another part of the peripheral circuit (a region for forming a p-channel type MISFET) to form the n-type well 12.

Further, following this ion implantation, an impurity for adjusting the threshold voltage of the MISFET, for example, BF2 (boron fluoride) is ion-implanted into the p-type well 11 and the n-type well 12.

The n-type semiconductor region 10 is formed to prevent noise from entering the p-type well 11 of the memory array from the input / output circuit or the like through the semiconductor substrate 1.

[0071]

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Next, the silicon oxide film 2 on each surface of the p-type well 11 and the n-type well 12 is removed using a HF (hydrofluoric acid) -based cleaning solution, and the semiconductor substrate 1 is wet-oxidized at about 850 ° C. A clean gate oxide film 13 having a film thickness of about 7 nm is formed on each surface of the well 11 and the n-well 12.

[0072]

Although not particularly limited, after the gate oxide film 13 is formed, the semiconductor substrate 1 is heat-treated in an NO (nitrogen oxide) atmosphere or an N 2 O (nitrous oxide) atmosphere to form the gate oxide film 13 and the semiconductor substrate. Nitrogen may be segregated at the interface with 1 (oxynitriding treatment).

When the gate oxide film 13 is thinned to about 7 nm, the strain generated at the interface between the semiconductor substrate 1 and the semiconductor substrate 1 becomes apparent and induces the generation of hot carriers.

Nitrogen segregated at the interface with the semiconductor substrate 1 alleviates this strain, so the above oxynitriding treatment can improve the reliability of the ultrathin gate oxide film 13.

[0073]

Next, as shown in FIG. 11, gate electrodes 14A, 14B, and 14C are formed on the gate oxide film 13.

The gate electrode 14A constitutes a part of the memory cell selecting MISFET, and is used as the word line WL in a region other than the active region.

The width of the gate electrode 14A (word line WL), that is, the gate length, is a minimum dimension within an allowable range (for example, a threshold value) in which the short channel effect of the memory cell selection MISFET can be suppressed and the threshold voltage can be secured at a certain value or more (for example, About 0.24 μm).

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Further, the interval between the adjacent gate electrodes 14A (word lines WL) is constituted by the minimum dimension (for example, 0.22 μm) determined by the resolution limit of photolithography.

The gate electrode 14B and the gate electrode 14C form a part of each of the n-channel type MISFET and the p-channel type MISFET of the peripheral circuit.

[0074]

As the gate electrode 14A (word line WL) and the gate electrodes 14B and 14C, a polycrystalline silicon film having a film thickness of about 70 nm doped with an n-type impurity such as P (phosphorus) is deposited on the semiconductor substrate 1 by the CVD method. Then, a WN (tungsten nitride) film having a film thickness of about 50 nm and a W film having a film thickness of about 100 nm are deposited on the upper portion thereof by a sputtering method, and a silicon nitride film 15 having a thickness of about 150 nm is further formed on the upper portion thereof by a CVD method. After the deposition, the photoresist film 16 is used as a mask to pattern these films.

The WN film functions as a barrier layer that prevents the W film and the polycrystalline silicon film from reacting with each other during high temperature heat treatment to form a silicide layer of high resistance at the interface between the two films.

As the barrier layer, a TiN (titanium nitride) film or the like can be used instead of the WN film.

[0075]

When a part of the gate electrode 14A (word line WL) is made of a low resistance metal (W), its sheet resistance can be reduced to about 2 to 2.5 Ω / □, so that the word line delay is reduced. be able to.

Further, since the word line delay can be reduced without lining the gate electrode 14 (word line WL) with Al wiring or the like, the number of wiring layers formed above the memory cell can be reduced by one layer.

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[0076]

Next, after removing the photoresist film 16, the dry etching residue and the photoresist residue remaining on the surface of the semiconductor substrate 1 are removed using an etching solution such as hydrofluoric acid.

When this wet etching is performed, the gate oxide film 13 in regions other than the lower portion of the gate electrode 14A (word line WL) and the gate electrodes 14B and 14C is removed, and at the same time, the gate oxide film 13 below the gate sidewall is isotropically. Since etching causes an undercut, the breakdown voltage of the gate oxide film 13 decreases as it is.

Therefore, the quality of the scraped gate oxide film 13 is improved by wet-oxidizing the semiconductor substrate 1 at about 900 ° C.

[0077]

Next, as shown in FIG. 12, p-type impurities such as B (boron) are ion-implanted into the n-type well 12 to form p-type semiconductor regions 17 in the n-type well 12 on both sides of the gate electrode 14C.

Further, an n-type impurity such as P (phosphorus) is ion-implanted into the p-type well 11 to form n-type semiconductor regions 18 in the p-type well 11 on both sides of the gate electrode 14B, and p-type on both sides of the gate electrode 14A. An n-type semiconductor region 19 is formed in the well 11.

As a result, the memory cell selecting MISFET Qs is formed in the memory array.

[0078]

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Next, as shown in FIG. 13, after depositing a silicon nitride film 20 having a film thickness of about 50 to 100 nm on the semiconductor substrate 1 by the CVD method, as shown in FIG. Sidewall spacers 20a are formed on the sidewalls of the gate electrodes 14B and 14C by covering the resist film 21 and anisotropically etching the silicon nitride film 20 of the peripheral circuit.

This etching uses an etching gas that increases the etching rate of the silicon nitride film 20 with respect to the silicon oxide film in order to minimize the amount of abrasion of the silicon oxide film 7 embedded in the gate oxide film 13 and the element isolation trench 5. Do using.

Further, in order to minimize the amount of abrasion of the silicon nitride film 15 on the gate electrodes 14B and 14C, the over-etching amount is kept to a necessary minimum.

[0079]

Next, after removing the photoresist film 21, as shown in FIG. 15, p-type impurities such as B (boron) are ion-implanted into the n-type well 12 in the peripheral circuit region to p-type p-channel MISFET. A semiconductor region 22 (source, drain) is formed, and an n-type impurity, such as As (arsenic), is ion-implanted into the p-type well 11 in the peripheral circuit region to form an n + -type semiconductor region 23 (source, drain) of an n-channel MISFET.) Is formed.

As a result, the p-channel type MISFET Qp and the n-channel type MISFET Qn having the LDD (Lightly Doped Drain) structure are formed in the peripheral circuit region.

[0080]

Next, as shown in FIG. 16, after the SOG (spin on glass) film 24 having a film thickness of about 300 nm is spin-coated on the semiconductor substrate 1, the semiconductor substrate 1 is heat-treated at 800 ° C. for about 1 minute to perform the SOG film 24. Are sintered.

[0081]

Next, as shown in FIG. 17, after depositing a silicon oxide film 25 with a film thickness of about 600 nm on the SOG film 24, the silicon oxide film 25 is polished by the CMP method to planarize its surface.

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The silicon oxide film 25 is deposited by the plasma CVD method using ozone (O3) and tetraethoxysilane (TEOS) as source gas, for example.

[0082]

As described above, in the present embodiment, the SOG film 24 having a high reflow property is applied to the upper portion of the gate electrode 14A (word line WL) and the gate electrodes 14B and 14C, and the silicon oxide film 25 deposited on the upper portion is subjected to CMP. Method to flatten.

As a result, the gap fill property of a fine gap between the gate electrodes 14A (word lines WL) is improved, and the insulating film above the gate electrodes 14A (word lines WL) and the gate electrodes 14B and 14C is flattened. be able to.

[0083]

Next, as shown in FIG. 18, a silicon oxide film 26 having a film thickness of about 100 nm is deposited on the silicon oxide film 25. The silicon oxide film 26 is deposited in order to repair fine scratches on the surface of the silicon oxide film 25 that are produced when the silicon oxide film 25 is polished by the CMP method. The silicon oxide film 26 is deposited by plasma CVD using, for example, ozone (O3) and tetraethoxysilane (TEOS) as source gases. Instead of the silicon oxide film 26, a PSG (Phospho Silicate Glass) film or the like may be deposited on the silicon oxide film 25.

[0084]

Next, as shown in FIG. 19, by dry etching using the photoresist film 27 as a mask, the silicon oxide films 26 and 25 and the SOG film 24 above the n-type semiconductor region 19 (source, drain) of the memory cell selecting MISFET Qs are dry-etched. To remove. This etching is performed under conditions such that the etching rates of the silicon oxide films 26 and 25 and the SOG film 24 with respect to the silicon nitride film 20 are large, and the silicon nitride film covering the n-type semiconductor region 19 and the upper portion of the element isolation

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trench 5 is etched. Make sure 20 is not completely removed.

[0085]

Note that the surfaces of the silicon oxide film 26 and the resist film 27 in FIG. 19 have a depression (step) shape along the surface of the silicon oxide film 25 in the peripheral circuit region as shown in FIG. FIG. 19 omits the shape.

[0086]
Then, as shown in FIG. 20, by dry etching using the photoresist film 27 as a mask, the silicon nitride film 20 and the gate oxide film 13 above the n-type semiconductor region 19 (source, drain) of the MISFET Qs for memory cell selection. By removing and, a contact hole 28 is formed in one upper part of the n-type semiconductor region 19 (source, drain), and a contact hole 29 is formed in the other upper part.

[0087]

This etching is performed under conditions such that the etching rate of the silicon nitride film 15 with respect to the silicon oxide film (the gate oxide film 13 and the silicon oxide film 7 in the element isolation trench 5) becomes large, and the n-type semiconductor region 19 and the element isolation trench are etched. Make sure not to sharpen 5 deeply.

Further, this etching is performed under the condition that the silicon nitride film 20 is anisotropically etched so that the silicon nitride film 20 remains on the side wall of the gate electrode 14A (word line WL). As a result, the contact holes 28 and 29 having a fine diameter less than the resolution limit of photolithography are formed in self alignment with the gate electrode 14A (word line WL). In order to form the contact holes 28 and 29 in self-alignment with the gate electrode 14A (word line WL), the silicon nitride film 20 is anisotropically etched in advance to form a sidewall on the side wall of the gate electrode 14A (word line WL). Spacers may be formed in advance.

[0088]

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Next, after removing the photoresist film 27, dry etching residues and photoresist residues on the substrate surface exposed at the bottoms of the contact holes 28 and 29 are removed by using an etching solution such as a hydrofluoric acid + ammonium fluoride mixed solution. To do. At that time, the SOG film 24 exposed on the sidewalls of the contact holes 28 and 29 is also exposed to the etching solution, but the SOG film 24 has an etching rate with respect to the hydrofluoric acid-based etching solution due to the sintering at about 800 ° C. described above. Since it is reduced, the sidewalls of the contact holes 28 and 29 are not largely undercut by this wet etching process. As a result, it is possible to reliably prevent a short circuit between the plugs embedded in the contact holes 28 and 29 in the next step.

[0089]

Next, as shown in FIG. 21, a plug 30 is formed inside the contact holes 28 and 29. For the plug 30, a polycrystalline silicon film doped with an n-type impurity (for example, P (phosphorus)) is deposited on the silicon oxide film 26 by the CVD method, and then the polycrystalline silicon film is polished by the CMP method to form a contact hole. It is formed by leaving the inside of 28 and 29.

[0090]

Next, as shown in FIG. 22, after depositing a silicon oxide film 31 with a film thickness of about 200 nm on the silicon oxide film 26, the semiconductor substrate 1 is heat-treated at about 800 ° C. The silicon oxide film 31 is deposited by the plasma CVD method using ozone (O3) and tetraethoxysilane (TEOS) as source gas, for example. By this heat treatment, the n-type impurities in the polycrystalline silicon film forming the plug 30 are diffused from the bottoms of the contact holes 28, 29 to the n-type semiconductor region 19 (source, drain) of the memory cell selecting MISFET Qs, and the n-type semiconductor is formed. The region 19 has a low resistance.

[0091]

Next, as shown in FIG. 23, the silicon oxide film 31 above the contact hole 28 is removed by dry etching using the photoresist film 32 as a mask to expose the surface of the plug 30. Next, after removing the photoresist film 32, as shown in FIG. 24, the silicon oxide films 31, 26, 25, the SOG film 24 and the gate oxide film in the peripheral circuit region are dry-etched by using the

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photoresist film 33 as a mask. By removing 13, the contact holes 34 and 35 are formed above the n + type semiconductor region 23 (source and drain) of the n channel MISFET Qn, and the p + type semiconductor region 22 (source and drain) of the p channel MISFET Qp is formed.), Contact holes 36 and 37 are formed.

[0092]

Next, after removing the photoresist film 33, as shown in FIG. 25, the bit line BL and the first layer wirings 38 and 39 of the peripheral circuit are formed on the silicon oxide film 31. To form the bit line BL and the first layer wirings 38 and 39, first, a Ti film having a film thickness of about 50 nm is deposited on the silicon oxide film 31 by a sputtering method, and the semiconductor substrate 1 is heat-treated at about 800 ° C. .. Then, a TiN film having a thickness of about 50 nm is deposited on the Ti film by a sputtering method, and a W film having a thickness of about 150 nm and a silicon nitride film 40 having a thickness of about 200 nm are further deposited on the TiN film by a CVD method. The photoresist film 41 is used as a mask to pattern these films.

[0093]

After depositing a Ti film on the silicon oxide film 31, the semiconductor substrate 1 is heat-treated at about 800 ° C., whereby the Ti film reacts with the underlying Si, and the n + -type semiconductor region 23 (of the n-channel type MISFET Qn) is formed. A low resistance TiSi2 (titanium silicide) layer 42 is formed on the surfaces of the source and drain, the p + type semiconductor region 22 (source and drain) of the p-channel MISFET Qp, and the surface of the plug 30. As a result, the contact resistance of the wiring (bit line BL, first layer wirings 38, 39) connected to the n + type semiconductor region 23, the p + type semiconductor region 22 and the plug 30 can be reduced. Further, since the bit line BL is formed of the W film / TiN film / Ti film, the sheet resistance thereof can be reduced to 2Ω / □ or less, so that the reading speed and the writing speed of information can be improved and the bit speed can be improved. Since the line BL and the first layer wirings 38 and 39 of the peripheral circuit can be simultaneously formed in one process, the manufacturing process of the DRAM can be shortened. Further, when the first-layer wirings (38, 39) of the peripheral circuit are formed by wirings in the same layer as the bit line BL, the peripheral wirings are more peripheral than when formed by Al wirings in the upper layer of the memory cell. Since the aspect ratio of the contact holes (34 to 37) connecting the MISFETs (n-channel type MISFETQn, p-channel type MISFETQp) of the circuit and the first layer wiring is reduced, the connection reliability of the first layer wiring is improved. ..

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[0094]

The bit lines BL are formed such that their intervals are longer than their widths in order to reduce the parasitic capacitance formed between the bit lines BL and the adjacent bit lines BL as much as possible to improve the information reading speed and information writing speed. .. The interval between the bit lines BL is, eg, about 0.24 μm, and the width thereof is, eg, about 0.22 μm.

[0095]

Next, after removing the photoresist film 41, as shown in FIG. 26, sidewall spacers 43 are formed on the sidewalls of the bit lines BL and the sidewalls of the first layer wirings 38 and 39. The sidewall spacer 43 is formed by depositing a silicon nitride film on the bit line BL and the first layer wirings 38 and 39 by the CVD method, and then anisotropically etching the silicon nitride film.

[0096]

Next, as shown in FIG. 27, an SOG film 44 having a film thickness of about 300 nm is spin-coated on the bit line BL and the first layer wirings 38 and 39. Next, the semiconductor substrate 1 is heat-treated at 800 ° C. for about 1 minute to sinter the SOG film 44.

[0097]

The SOG film 44 has a higher reflow property than the BPSG film and an excellent gap fill property between fine wirings, so that the gap between the bit lines BLs fined to the resolution limit of photolithography can be favorably formed. Can be embedded. Further, since the SOG film 44 can obtain a high reflow property without the high temperature and long time heat treatment required for the BPSG film, the source and drain of the memory cell selecting MISFET Qs formed in the lower layer of the bit line BL. It is possible to suppress the thermal diffusion of impurities contained in the sources and drains of the MISFETs (n-channel type MISFETQn, p-channel type MISFETQp) of the peripheral circuits and the peripheral circuits, thereby achieving a shallow junction. Further, since deterioration of the metal (W film) forming the gate electrode 14A (word

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line WL) and the gate electrodes 14B and 14C can be suppressed, high performance of the MISFET forming the DRAM memory cell and the peripheral circuit can be realized. You can In addition, it is possible to suppress the deterioration of the Ti film, the TiN film, and the W film that form the bit line BL and the first layer wirings 38 and 39, and reduce the wiring resistance.

[0098]

Next, as shown in FIG. 28, after depositing a silicon oxide film 45 having a film thickness of about 600 nm on the SOG film 44, the silicon oxide film 45 is polished by the CMP method to planarize its surface. The silicon oxide film 45 is deposited by a plasma CVD method using ozone (O3) and tetraethoxysilane (TEOS) as source gases, for example.

[0099]

As described above, in the present embodiment, the SOG film 44 having good flatness is applied to the upper part of the bit line BL and the first layer wirings 38 and 39 even after the film formation, and the silicon oxide film 45 deposited on the upper part thereof. Is flattened by the CMP method. As a result, the gap fill property of the minute gap between the bit lines BL is improved, and the insulating film above the bit lines BL and the first layer wirings 38 and 39 can be flattened. Further, since heat treatment at high temperature for a long time is not performed, it is possible to prevent deterioration of the characteristics of the MISFETs constituting the memory cell and the peripheral circuit and realize high performance, and at the same time, the bit line BL and the first layer wiring 38, It is possible to reduce the resistance of 39.

[0100]

A silicon oxide film having a film thickness of about 100 nm may be deposited on the silicon oxide film 45. This silicon oxide film can repair fine scratches on the surface of the silicon oxide film that are generated when the silicon oxide film is polished by the CMP method. Such a silicon oxide film can be deposited by a plasma CVD method using ozone (O3) and tetraethoxysilane (TEOS) as source gases, for example.

[0101]

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Next, as shown in FIG. 29, a silicon nitride film 46 having a film thickness of about 50 nm is deposited on the silicon oxide film 45. This silicon nitride film 46 is used as an etching stopper when etching the silicon oxide film between the lower electrodes in the step of forming the lower electrodes of the information storage capacitive element described later. Therefore, the silicon nitride film 46 is made of a silicon nitride material having an etching rate slower than the etching rate of the silicon oxide film between the lower electrodes described later.

[0102]

Next, as shown in FIG. 30, the silicon nitride film 46, the silicon oxide film 45, the SOG film 44 and the silicon oxide film 31 above the contact hole 29 are removed by dry etching using the photoresist film 47 as a mask to remove the plug. A through hole 48 reaching the surface of 30 is formed. This etching is performed under the condition that the etching rate of the silicon nitride film with respect to the silicon oxide films 45 and 31 and the SOG film 44 is reduced after etching the silicon nitride film 46 under the condition that silicon nitride is etched. Even if there is a misalignment between the bit line BL and the bit line BL, the silicon nitride film 40 and the sidewall spacer 43 above the bit line BL are prevented from being deeply shaved. As a result, the through hole 48 is formed in self alignment with the bit line BL.

[0103]

Next, after removing the photoresist film 47, a dry etching residue or a photoresist residue on the surface of the plug 30 exposed at the bottom of the through hole 48 is removed by using an etching solution such as a mixed solution of hydrofluoric acid and ammonium fluoride. To do. At that time, the SOG film 44 exposed on the side wall of the through hole 48 is also exposed to the etching solution, but the SOG film 44 has a reduced etching rate for the hydrofluoric acid-based etching solution due to the sintering at about 800 ° C. Therefore, the sidewall of the through hole 48 is not largely undercut by this wet etching process. As a result, it is possible to reliably prevent a short circuit between the plug embedded in the through hole 48 and the bit line BL in the next step. Moreover, since the plug and the bit line BL can be sufficiently separated from each other, an increase in the parasitic capacitance of the bit line BL can be suppressed.

[0104]

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Next, as shown in FIG. 31, a plug 49 is formed inside the through hole 48. For the plug 49, a polycrystalline silicon film doped with an n-type impurity (for example, P (phosphorus)) is deposited on the silicon nitride film 46 by a CVD method, and then the polycrystalline silicon film is etched back to form a through hole 48. It is formed by leaving it inside.

[0105]

Next, as shown in FIG. 32, after depositing a silicon oxide film 53 having a film thickness of about 0.5 μm on the silicon nitride film 46, the silicon oxide film 53 is removed by dry etching using the photoresist film 54 as a mask. By doing so, a groove 55 is formed above the through hole 48 in which the plug 49 is embedded. The silicon oxide film 53 is deposited by the plasma CVD method using ozone (O3) and tetraethoxysilane (TEOS) as source gases, for example.

[0106]

Next, after removing the photoresist film 54, as shown in FIG. 33, a polycrystalline silicon film 56 having a film thickness of about 50 nm doped with an n-type impurity (for example, P (phosphorus)) is formed on the silicon oxide film 53. It is deposited by the CVD method. This polycrystalline silicon film 56 is used as a lower electrode material of the information storage capacitive element.

[0107]

Next, as shown in FIG. 34, a silicon oxide film 57 having a film thickness (for example, about 0.4 μm) sufficient to fill the trench 55 is formed on the polycrystalline silicon film 56 by, for example, the CVD method, and then, as shown in FIG. As shown in FIG. 5, the silicon oxide film 57 is etched back by using, for example, a dry etching method to leave the silicon oxide film 57 only in the groove 55, and further, the polycrystalline silicon film 56 on the silicon oxide film 53 is etched back. Thus, the polycrystalline silicon film 56 is left inside the groove 55 (inner wall and bottom).

[0108]

Next, as shown in FIG. 36, a photoresist film 58 covering the silicon oxide film 53 in the peripheral circuit region is formed.

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There is no problem even if the photoresist film 58 is separated from the polycrystalline silicon film 56, which is the lower electrode of the information storage capacitor located at the outermost end of the memory cell array region, by about 5 μm. Therefore, a sophisticated photolithography technique is not required to form the photoresist film 58. This can reduce the load of the manufacturing process and simplify the manufacturing method.

[0109]

Next, as shown in FIG. 37, the silicon oxide film 53 and the silicon oxide film 57 in the region where the surface is exposed are removed by wet etching. The wet etching can be carried out, for example, by immersing it in a mixed solution of hydrofluoric acid (HF) and ammonium fluoride (NH4 F) in a ratio of 1:20, until the underlying silicon nitride film 46 is exposed.

[0110]

A dry etching method can be used to remove the silicon oxide film 53 and the silicon oxide film 57 in the region where the surface is exposed. However, in order to make the etching end portion of the silicon oxide film 53 an inclined surface, an isotropic method is used. It is more convenient to use wet etching in which the etching progresses. In addition, wet etching is more convenient in terms of ensuring etching selectivity with respect to the silicon nitride film 46 and the polycrystalline silicon film 56.

[0111]

Thus, the lower electrode 60 made of the polycrystalline silicon film 56 is formed. Since the silicon oxide film 53 remains in the peripheral circuit region, planarization described later can be easily performed.

[0112]
Although the photoresist film 58 is illustrated in the present embodiment, the present invention is not limited to this.

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[0113]

Next, the photoresist film 58 is removed, and then, in order to prevent the polycrystalline silicon film (56) forming the lower electrode 60 from being oxidized, the semiconductor substrate 1 is subjected to a heat treatment at about 800 ° C. in an ammonia atmosphere, and is then subjected to a heat treatment. After nitriding the surface of the crystalline silicon film (56) to form a silicon nitride film (not shown) having a film thickness of about 1.5 nm, as shown in FIG. A Ta2 O5 (tantalum oxide) film 61 is deposited by the CVD method, and then the semiconductor substrate 1 is heat-treated at about 800 ° C. to modify the Ta2 O5 film 61.

This Ta2 O5 film 61 is used as a material for the capacitive insulating film of the information storage capacitive element.

[0114]

Next, as shown in FIG. 39, a TiN film 62 having a film thickness of about 50 nm is deposited on the Ta2 O5 film 61 by, for example, the CVD method, and then the TiN film 62 and the Ta2 film 62 and Ta2 are dry-etched using the photoresist film 63 as a mask. By patterning the O5 film 61, an information storage capacitive element C including an upper electrode made of a TiN film 62, a capacitive insulating film made of a Ta2 O5 film 61, and a lower electrode 60 made of a polycrystalline silicon film 56 is formed. To form. As a result, a DRAM memory cell including the memory cell selection MISFET Qs and the information storage capacitive element C connected in series with the MISFET Qs is completed.

[0115]

Next, after removing the photoresist film 63, as shown in FIG. 40, a silicon oxide film 64 having a film thickness of about 40 nm is deposited on the information storage capacitive element C. The silicon oxide film 64 is deposited by a plasma CVD method using ozone (O3) and tetraethoxysilane (TEOS) as source gases, for example.

[0116]

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After that, a thick SOG film 65 which is not cracked even if formed thick is formed by a spin coating method to flatten the surface. An example of the SOG film that can be applied to this thick film is described in Japanese Patent Application No. 3-245499, and for example, a trade name type 8 manufactured by Tokyo Ohka Co., Ltd. can be used.

[0117]

Next, as shown in FIG. 41, the SOG film 65, the silicon oxide films 64 and 53, the silicon nitride film 46, and the silicon oxide film on the first layer wiring 38 of the peripheral circuit are dry-etched by using the photoresist film as a mask. By removing 45, the SOG film 44 and the silicon nitride film 40, a through hole 66a is formed. Similarly, the through hole 66b is formed by removing the SOG film 65 and the silicon oxide film 64 above the TiN film 62 which is the upper electrode. After that, the plug 67 is formed inside the through holes 66 a and 66 b, and then the second layer wiring 68 is formed on the SOG film 65. For the plug 67, a TiN film having a film thickness of about 100 nm is deposited on the SOG film 65 by a sputtering method, a W film having a film thickness of about 500 nm is further deposited on the TiN film by a sputtering method, and then these films are etched back. And is left inside the through holes 66a and 66b. The second layer wiring 68 is formed by depositing a TiN film having a film thickness of about 50 nm, an Al (aluminum) film having a film thickness of about 500 nm, and a Ti film having a film thickness of about 50 nm on the SOG film 65 by a sputtering method, and then forming a photoresist film. These films are formed by patterning these films by dry etching using as a mask.

[0118]

After that, a third-layer wiring is formed via an interlayer insulating film, and a passivation film composed of a silicon oxide film and a silicon nitride film is deposited on the third-layer wiring, but the illustration thereof is omitted. Through the above steps, the DRAM of this embodiment is almost completed.

[0119]

The third-layer wiring and the plug connected thereto can be formed in the same manner as the second-layer wiring, and the interlayer insulating film is, for example, a silicon oxide film with a

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thickness of about 300 nm, an SOG film with a thickness of about 400 nm, and It can be composed of a silicon oxide film having a film thickness of about 300 nm. The silicon oxide film can be deposited, for example, by a plasma CVD method using ozone (O3) and tetraethoxysilane (TEOS) as source gases.

[0120]
According to the present embodiment, the surface can be flattened after the information storage capacitive element is formed. Conventionally, when there is a step between the memory cell array region and the peripheral circuit region, the exposure depth of focus margin in the photolithography process can be increased. It is possible to solve the problem that pattern formation becomes difficult due to a decrease in the degree of the pattern. As a result, it is possible to increase the height of the lower electrode 60 and increase the capacitance.

[0121]
In this embodiment, the bit line BL is made of a laminated film containing a metal, and the tantalum oxide film 61c is used as the capacitor insulating film 61 even if the heat resistance of the contact with the silicon substrate becomes poor. It is possible to lower the temperature, and there is an advantage that conduction failure at the contact portion can be avoided.

[0122]

(Embodiment 2) FIG. 42 is a sectional view showing an example of a DRAM of the present embodiment.

In the DRAM of the present embodiment, a part of the capacitance insulating film 61 and the upper electrode 62 is also arranged around the upper portion of the plug 49.

As a result, the amount of accumulated charge can be increased. That is, the upper part of the plug 49 is a cylindrical electrode connected to the lower electrode 60, and the upper electrode 62 is arranged as a concentric cylindrical electrode arranged around the lower electrode 60 to form a cylindrical capacitive element and a cylindrical capacitive element having an opening at the top. And are integrally formed as an information storage capacitive element.

[0123]

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The method of manufacturing the DRAM of the present embodiment is the same up to the step of FIG. 37 in the first embodiment.

[0124]

After that, as shown in FIG. 43, the silicon nitride film 46 is etched by a wet etching method using hot phosphoric acid, for example.

At this time, the silicon oxide film is not etched. Therefore, the silicon oxide film 53 acts as a kind of mask, and it is possible to prevent the entire silicon nitride film 46 in the peripheral circuit region from being etched.

[0125]
After that, as shown in FIG. 44, the capacitive insulating film 61 and the upper electrode 62 are formed as in the first embodiment.

[0126]

Since the subsequent steps are the same as those in the first embodiment, the description thereof will be omitted.

In this way, the DRAM of this embodiment is almost completed.

[0127]
(Embodiment 3) In this embodiment, a more effective method of planarizing the surface with an SOG film after formation of the information storage capacitor will be described with reference to FIG.

[0128]

The following problems may occur when the thick SOG film is formed after the information

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storage capacitive element is formed.

That is, the lower electrode 60 in the first embodiment has a cylindrical shape having an opening upward, and a recess is also formed on the surface of the upper electrode 62 reflecting this shape. The thick SOG film 65 is applied to the recesses to planarize the surface. The thick SOG film 65 is formed by the spin coating method, and the surface is formed by forming the information storage capacitive element. The unevenness that occurs on the surface becomes large. That is, if the width of the groove is narrow and deep, it may not be possible to completely fill the inside of the groove. In such a case, voids are generated in the central portion, the bottom portion, or the side surface of the groove, and these voids may expand due to the heat treatment received in a later step and destroy the thick SOG film 65, which is not preferable. Such a problem does not occur because the groove (recess) formed in the boundary region between the memory cell array region and the peripheral circuit region described in the first embodiment has a sufficient width.

[0129]

Therefore, in the present embodiment, the occurrence of voids is avoided by the following method. FIG. 45 is a cross-sectional view showing an example of the manufacturing method of the present embodiment.

[0130]

That is, the upper electrode 69 of the information storage capacitive element is formed so as to fill the groove, and the memory cell array region is previously flattened by the upper electrode 69 itself before forming the SOG. The flattening by the upper electrode is performed by depositing an upper electrode material having a film thickness of half or more of the longest portion of the intervals of the information storage capacitive elements regularly arranged in the memory cell array region by the CVD method. Can be achieved by As the upper electrode material, titanium nitride produced from titanium tetrachloride and ammonia as a raw material, known polycrystalline silicon, or the like can be used.

[0131]

According to the present embodiment, the groove formed by forming the information storage capacitive element can be filled with the upper electrode 69 itself which is one component of the

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information storage capacitive element, so that the narrow and deep groove is formed by SOG. It is possible to avoid a decrease in the reliability of the DRAM due to voids or the like that occur when filling.

[0132]
Embodiment Mode 4 In this embodiment mode, a structure of a plug in the case where a metal or a metal compound is used for a lower electrode of an information storage capacitor is described with reference to FIG.

[0133]

FIG. 46 is a sectional view showing the DRAM of the fourth embodiment.

In the present embodiment, a metal plug 70 formed at the same time as the bit line BL is formed instead of the plug 30 of the first embodiment.

Further, in the present embodiment, the plug 49 formed below the lower electrode 60 can also be a metal plug. Further, the lower electrode 60 can also be formed of a metal film. Examples of the material for the metal plug and the metal film include titanium nitride, or titanium nitride and tungsten.

[0134]

The method of manufacturing the DRAM of the present embodiment is the same up to the opening of contact holes 28 and 29 of FIG. 20 in the first embodiment. Next, the bit line BL is formed without forming the plug 30 in the first embodiment. Note that, at this time, the contact holes 34, 35, 36, 37 of the peripheral circuit are previously opened as in the first embodiment.

[0135]
In this way, the metal plug 70 can be formed simultaneously with the bit line BL and the first layer wiring 38.

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[0136]
After that, the steps up to FIG. 30 of the first embodiment are the same, and a metal plug 71 made of titanium nitride is formed instead of the plug 49 formed in FIG.

[0137]

Further, a titanium nitride film is deposited instead of the polycrystalline silicon film 56 in FIG. 33 of the first embodiment, and the lower electrode 72 made of titanium nitride is formed by the same process as in the first embodiment.

Other steps are the same as those in the first embodiment.

[0138]
According to the present embodiment, since the lower electrode 72 of the information storage capacitive element is made of titanium nitride, the underlying metal plug 71 can be made of a metal or a metal compound. Compared with the above, the resistance can be reduced, and there is an advantage that a part of the plug can be formed in the same process as the bit line.

[0139]

(Embodiment 5) In this embodiment, a method of flattening the surface when the lower electrode of the information storage capacitor is formed in an island shape will be described with reference to FIGS. 47 to 51.

47 to 51 are partial cross-sectional views illustrating the manufacturing method according to the fifth embodiment in the order of steps thereof.

[0140]

The manufacturing method of the present embodiment is the same in the steps up to FIG. 31 of the first embodiment.

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Note that the plug 49 in FIG. 31 is a metal plug 71 made of titanium nitride in the present embodiment. The metal plug 71 can be formed by a well-known method in which a titanium nitride film is deposited on the entire surface by a CVD method to a thickness that fills the through hole 48, and then etched and removed by the deposited film thickness.

[0141]
Next, as shown in FIG. 47, a tungsten film having a thickness of 500 nm is formed on the entire surface by a sputtering method, a patterned photoresist film 73 is formed at a predetermined position, and the tungsten film is processed by a dry etching method. Then, the lower electrode 74 is formed.

[0142]
Next, as shown in FIG. 48, after removing the photoresist film 73, a tantalum oxide film (not shown) having a thickness of 15 nm is formed as a capacitive insulating film by the CVD method and heat treatment is performed. A titanium nitride film is formed on the entire surface so as to fill the gap, and the titanium nitride film in the peripheral circuit region is removed by well-known lithography and dry etching to form an upper electrode 75.

[0143]

Next, as shown in FIG. 49, a silicon oxide film 76 having a thickness of 500 nm is formed on the entire surface by the CVD method.

The silicon oxide film 76 can be formed by, for example, a CVD method using ozone and TEOS as raw materials.

[0144]

Next, as shown in FIG. 50, a photoresist film 77 is formed in the peripheral circuit region, and the silicon oxide film 76 in the memory cell array region is removed by etching with a hydrofluoric acid solution using the photoresist film 77 as a mask.

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The effect of the wet etching is similar to that of the case described in the first embodiment.

[0145]

Next, as shown in FIG. 51, after removing the photoresist film 77, a silicon oxide film 78 having a thickness of 50 nm is formed on the entire surface of the semiconductor substrate 1, and a thick SOG film 79 is applied to form the entire surface. Flatten. The silicon oxide film 78 and the thick SOG film 79 are similar to the silicon oxide film 64 and the thick SOG film 65 in the first embodiment.

[0146]
The subsequent steps are the same as those in the first embodiment.

[0147]

According to the present embodiment, even if the lower electrode 74 of the information storage capacitive element has an island shape, the surface can be flattened.

As a result, the restrictions of photolithography can be eliminated, and the height of the island-shaped lower electrode 74 can be increased to secure a desired amount of accumulated charges.

[0148]

In the present embodiment, an example in which the concave portion between the memory cell array region and the peripheral circuit region is flattened by applying the thick SOG film 79 in FIG. 51 is shown, but FIGS. As shown, after removing the photoresist film 77, a 700 nm-thickness silicon oxide film 80 is formed by the CVD method (FIG. 52), and then the surface of the silicon oxide film 80 is polished by the CMP method to be planarized. You may go (Fig. 53). The silicon oxide film 80 is set to be thicker than the height of the island-shaped lower electrode 74. Subsequent steps can be performed in the same manner as in Embodiment 1.

[0149]

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In the present embodiment, an example in which tungsten is used for the island-shaped lower electrode 74 is shown, but the present invention is not limited to this, and titanium nitride or another metal or metal compound may be used. Further, the forming method is not limited to the sputtering method and may be the CVD method.

[0150]

(Embodiment 6) In this embodiment, a method for forming an information storage capacitor is described with reference to FIGS. 54 and 55 are cross-sectional views showing an example of a cylindrical information storage capacitive element having an opening at the top.

[0151]

The DRAM of the present embodiment is almost the same as the DRAM of the first embodiment except for the information storage capacitor element. Therefore, the description of the same parts will be omitted.

[0152]

In FIG. 54A, a titanium nitride film 82 to be a cylindrical lower electrode having an opening at the top is formed on a metal plug 81 made of titanium nitride formed on the silicon nitride film 46, and the surface thereof is oxidized. The state where the titanium oxide film 83 is formed is shown. The formation of the metal plug 81 and the titanium nitride film 82 is similar to that of the metal plug 71 and the lower electrode 72 made of titanium nitride in the above-described embodiments.

[0153]

FIG. 54B shows a state in which the tantalum oxide film 84 is further formed.

[0154]

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An important point in realizing a cylindrical information storage capacitor element having an opening in the upper part is a method of forming a cylindrical lower electrode having an opening in the upper part.

As already described in the first embodiment, when forming the lower electrode 60 in a cylindrical shape, first, the groove 55 is formed in the silicon oxide film 53 as the base material, and the lower electrode material is formed on the side wall and the bottom of the groove 55. It is formed by leaving it. At this time, whether or not the step coverage of the lower electrode material is good determines whether or not the cylindrical lower electrode 60 having an opening at the top can be realized. That is, if the step coverage is poor, the film thickness of the bottom region of the groove 55 becomes thin, and the lower electrode 60 collapses when the base material is removed by etching, which makes its formation difficult. Therefore, in order to realize a cylindrical lower electrode having an opening in the upper portion, good step coverage during electrode material deposition is an essential condition. An example of the electrode material having such characteristics is a titanium nitride film formed by a CVD method using titanium tetrachloride and ammonia as raw materials.

[0155]

Therefore, in the present embodiment, the lower electrode made of the titanium nitride film 82 is formed. The manufacturing method will be described below.

[0156]

After forming the titanium nitride film 82, heat treatment is performed for 3 minutes in a nitrogen atmosphere at 750 ° C. This heat treatment is intended to promote recrystallization of titanium nitride, and is preferably performed at a temperature higher than the heat treatment temperature for the tantalum oxide film to be performed later. Then, a titanium oxide film 83 having a thickness of 5 nm is formed on the surface of the titanium nitride film 82.

[0157]

Next, a tantalum oxide film 84 having a thickness of 15 nm is formed as a dielectric by the CVD

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method. Then, heat treatment is performed for 3 minutes in an argon atmosphere at 725 ° C. to crystallize tantalum oxide. Further, heat treatment is performed in an ozone atmosphere at 400 ° C. for 5 minutes to oxidize and modify tantalum oxide. After that, similarly to the first embodiment, a titanium nitride film is formed and an upper electrode is formed to form an information storage capacitive element.

[0158]

FIG. 55 shows a procedure of performing the process of forming the titanium oxide film on the surface of the titanium nitride film to be the lower electrode after forming the tantalum oxide film.

[0159]

After forming a cylindrical lower electrode having an opening at the top with the titanium nitride film 85, heat treatment is performed in a nitrogen atmosphere at 750 ° C. for 3 minutes to deposit a tantalum oxide film 86 having a thickness of 15 nm.

[0160]

Next, heat treatment was performed for 3 minutes in an argon atmosphere at 725 ° C. to crystallize the tantalum oxide film 86, and then heat treatment was performed in an ozone atmosphere at 400 ° C.

At this time, the heat treatment time can be controlled so that the titanium oxide film 86 having a thickness of 3 to 5 nm is formed on the surface of the underlying titanium nitride film 85 simultaneously with the modification of the tantalum oxide film 86.

After that, an upper electrode similar to the above may be formed to form an information storage capacitive element.

[0161]

FIG. 56 shows an example of characteristics of the information storage capacitive element obtained by the above method. An effective film thickness is one of the important characteristics

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required for an information storage capacitive element used in a semiconductor memory device. The effective film thickness is an electric film thickness obtained from the capacitance of the information storage capacitor, assuming that it is made of silicon dioxide regardless of the material of the capacitor insulating film. The smaller the effective film thickness, the larger the capacity obtained.

[0162]

FIG. 56 shows the relationship between the heat treatment temperature (horizontal axis) and the effective film thickness (vertical axis) when tantalum oxide is heat-treated in an argon atmosphere. In the figure, A shows the case where the physical film thickness of tantalum oxide is 20 nm, and B shows the case where it is 10 nm. In either case, the effective film thickness becomes smaller as the heat treatment temperature becomes higher. At 725 ° C, in case of B, the effective film thickness is 0.9 nm. For example, if the effective thickness of the conventional information storage capacitor is 3 nm and the required height of the cylindrical electrode is 600 nm, the effective thickness of the cylindrical electrode is about 0.9 nm. This means that it can be lowered to 200 nm, which is an extremely great advantage in constructing a manufacturing process as a semiconductor memory device. That is, it is possible to reduce the height of the information storage capacitive element and reduce the difficulty of processing in the manufacturing process.

[0163]

According to the present embodiment, since titanium nitride films 82 and 85 formed by the CVD method are used as the lower electrodes, it is easy to form a cylindrical lower electrode having an opening at the top, and titanium nitride is formed of silicon. Since it is not contained, even if the heat treatment is performed with the tantalum oxide films 84 and 86 formed thereon, silicon dioxide having a low dielectric constant is not generated. Therefore, the effective film thickness can be reduced and a large capacity can be obtained.

[0164]

(Embodiment 7) In this embodiment, a method for preventing the information storage capacitive element from collapsing when the height of the information storage capacitive element is increased will be described with reference to FIGS. 57 and 58.

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[0165]
57 and 58 are partial cross-sectional views describing the manufacturing method of the present embodiment in the order of steps thereof.

[0166]
The manufacturing method of the present embodiment is the same in the steps up to FIG. 31 of the first embodiment.

[0167]

Next, as shown in FIG. 57, after forming a groove 55 in the silicon oxide 53 so as to connect to the metal plug 71 buried in a predetermined region of the silicon nitride film 46, the titanium nitride film 88 is fronted. Then, the groove 55 is filled with the organic substance 89.

As the organic material 89, a photoresist or a polyimide resin such as polyimide isoindolocunazolinedione can be exemplified.

[0168]

Next, as shown in FIG. 58, the titanium nitride film 88 exposed on the silicon oxide 53 is removed, and the titanium nitride film 88 remains only in the trench 55.

Further, after removing the organic substance 89 filling the groove 55, a capacitive insulating film (not shown) made of tantalum oxide is formed as in the above-described embodiment, and a titanium nitride film 90 is formed as an upper electrode. , Forming an information storage capacitive element.

[0169]

After that, an interlayer insulating film can be formed similarly to the first embodiment, and the plug 67 and the second layer wiring 68 similar to those of the first embodiment can be formed.

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In this embodiment, since the recess is not formed between the memory cell array region and the peripheral circuit region, it is not necessary to use the SOG film as a part of the interlayer insulating film.

[0170]

According to this embodiment, the silicon oxide film 53, which is the base material used to form the cylindrical lower electrode having an opening in the upper portion, is not removed but left as it is as a support. The titanium film 88 does not collapse. Further, the step generated at the boundary between the memory cell array region and the peripheral circuit region is 100 nm at most due to the film thickness of the titanium nitride film 90 which is the upper electrode, and poses no problem in photolithography for forming the upper layer wiring. . Further, since the base material is left as a support, even if the information storage capacitive element becomes relatively thin, it does not collapse, so that it is possible to increase the height and expand the capacity.

[0171]
(Embodiment 8) In this embodiment, a method of increasing the height of the information storage capacitive element and increasing the capacitance will be described with reference to FIGS. 59 to 63.

[0172]
59 to 63 are partial cross-sectional views explaining the manufacturing method of the present embodiment in the order of steps thereof.

[0173]
The manufacturing method of the present embodiment is the same until the formation of the titanium nitride film 88 which is the lower electrode of the seventh embodiment (FIG. 59).

[0174]

After that, as shown in FIG. 60, the silicon oxide film 53 used as the base material is etched and removed so that about 30% of the original thickness remains.

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Further, a tantalum oxide film (not shown) was formed on the basis of the above method of forming the capacitive insulating film, and heat treatment was performed.

In that state, a connection hole 91 is provided at a predetermined position in the peripheral circuit region by using lithography and dry etching, and after removing the photoresist film, a titanium nitride film is formed on the entire surface to form an upper electrode of the information storage capacitor element. 90 and the peripheral circuit plug 92 are formed simultaneously.

[0175]
Next, as shown in FIG. 61, a silicon nitride film 93 having a thickness of about 50 nm is formed on the entire surface, and a new silicon oxide film 94 having a film thickness corresponding to the removed film thickness of the silicon oxide film 53 previously removed is formed. It is deposited on the entire surface of the semiconductor substrate 1 by the CVD method.

[0176]
Then, a photoresist film 95 is formed as in the first embodiment, and the silicon oxide film 94 in the memory cell array region is removed.

[0177]

Next, as shown in FIG. 62, after removing the photoresist film 95, an SOG film 96 is formed to planarize the surface.

The SOG film 96 can be formed in the same manner as the thick SOG film 65 of the first embodiment.

[0178]

Finally, a 100-nm-thick silicon oxide film 97 is formed by a CVD method, then a through hole 98 is formed in a predetermined region, a plug 99 is formed, and a second layer wiring 100 is

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formed.

The through hole 98, the plug 99 and the second layer wiring 100 can be formed in the same manner as in the first embodiment.

[0179]

According to the present embodiment, by leaving the insulating film serving as the base material only in the bottom area of the information storage capacitive element, the bottom area of the information storage capacitive element in which the base material remains is a groove type information storage capacitive element. Since the upper region from which the base material has been removed can be configured as a cylindrical information storage capacitive element having an opening in the upper portion, it is possible to prevent collapse even if the height of the information storage capacitive element is increased, and There is an effect that it can increase.

Further, since the plug 92 in the peripheral circuit region can be formed in the same step as the upper electrode 90, there is an effect that the depth of the through hole 98 can be reduced and dry etching can be performed more easily.

[0180]
Although the invention made by the present inventor has been specifically described based on the embodiments of the present invention, the present invention is not limited to the embodiments and various modifications can be made without departing from the scope of the invention. Needless to say.

[0181]

For example, in the above-described embodiment, an example in which a polycrystalline silicon film is used as the lower electrode has been shown, but a lower electrode having hemispherical silicon 101 on the surface as shown in FIG. 64 may be used.

In this case, the height of the lower electrode can be reduced to facilitate the process, or the amount of accumulated charge can be increased.

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[0182]
The effects obtained by the typical ones of the inventions disclosed in the present application will be briefly described as follows.

[0183]
(1) It is possible to provide a technique in which a step is not generated between the memory cell array region and the peripheral circuit region even when the three-dimensional capacitor is formed.

[0184]
(2) A technique for eliminating a step between the memory cell array region and the peripheral circuit region due to the formation of the three-dimensional capacitor can be provided, and the difficulty of photolithography can be eliminated.

[0185]
(3) A technique for eliminating a step between the memory cell array region and the peripheral circuit region due to the formation of the three-dimensional capacitor can be provided, and a wiring layer formed thereabove or a short circuit due to defective patterning can be prevented.

[0186]
(4) It is possible to provide a semiconductor integrated circuit device that achieves both high capacitance and high capacitance.

[0187]
(5) It is possible to provide a technique for preventing the collapse of the capacitor electrode during the manufacturing process due to the increase in the height of the three-dimensional capacitor, and improve the manufacturing yield of the semiconductor integrated circuit device.

[0188]
(6) It is possible to provide a three-dimensional capacitor having a high storage capacitance value, reduce the height of the three-dimensional capacitor, secure the capacitance of the capacitor, and provide a semiconductor integrated circuit device that achieves high reliability.

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[0189]
(7) By eliminating the step between the memory cell array region and the peripheral circuit region, the aspect ratio of the connection hole in the deeper peripheral circuit region is relaxed, and the processing of the connection hole in the peripheral circuit region is facilitated. You can

[0190]
(8) Since the upper and lower electrodes are made of titanium nitride having excellent step coverage, and the dielectric is also made of tantalum oxide having excellent step coverage, the information storage capacitive element is configured, so that the height of the electrodes is restricted. It is possible to realize an information storage capacitive element without doing so.

[0191]
(9) Even if the degree of integration of the semiconductor memory device is improved and the planar area allowed for each memory cell is reduced, it is possible to secure the capacity by increasing the height of the information storage capacitor element. Therefore, a highly reliable semiconductor memory device can be provided.

[0192]
Brief description of the drawings

[0193]
1 is an overall plan view of a semiconductor chip forming a DRAM according to an embodiment of the present invention.

[0194]
2 is an equivalent circuit diagram of the DRAM according to the first embodiment of the present invention.

[0195]
3 is a cross-sectional view of a main portion of a semiconductor substrate showing a method of manufacturing a DRAM according to the first embodiment of the present invention.

[0196]

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<Figure 4> It is the principal part cross section diagram of the semiconductor substrate which shows the manufacturing method of the DRAM which is the form 1 of execution of this invention.

[0197]
5 is a cross-sectional view of a main portion of a semiconductor substrate showing a method of manufacturing a DRAM which is Embodiment 1 of the present invention.

[0198]
6 is a cross-sectional view of a main portion of a semiconductor substrate showing a method of manufacturing a DRAM according to the first embodiment of the present invention.

[0199]
7 is a cross-sectional view of a main portion of a semiconductor substrate showing a method of manufacturing a DRAM according to the first embodiment of the present invention.

[0200]
<Figure 8> It is the principal part cross section diagram of the semiconductor substrate which shows the manufacturing method of the DRAM which is the form 1 of execution of this invention.

[0201]
9 is a cross-sectional view of a main portion of a semiconductor substrate showing a method of manufacturing a DRAM which is Embodiment 1 of the present invention.

[0202]
10 is a cross-sectional view of a main portion of a semiconductor substrate showing a method of manufacturing a DRAM which is Embodiment 1 of the present invention.

[0203]
<Drawing 11> The principal part cross section of the semiconductor substrate which shows the manufacturing method of the DRAM which is the form 1 of execution of this invention.

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[0204]
<Drawing 12> The principal part cross section of the semiconductor substrate which shows the manufacturing method of the DRAM which is the form 1 of execution of this invention.

[0205]
FIG. 13 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0206]
14 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0207]
FIG. 15 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0208]
16 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0209]
FIG. 17 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0210]
<Figure 18> It is the principal part cross section diagram of the semiconductor substrate which shows the manufacturing method of the DRAM which is the form 1 of execution of this invention.

[0211]
<Drawing 19> The principal part cross section of the semiconductor substrate which shows the manufacturing method of the DRAM which is the form 1 of execution of this invention.

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[0212]
20 is a cross-sectional view of a main portion of a semiconductor substrate showing a method of manufacturing a DRAM which is Embodiment 1 of the present invention.

[0213]
<Figure 21> It is the principal part cross section diagram of the semiconductor substrate which shows the manufacturing method of the DRAM which is the form 1 of execution of this invention.

[0214]
FIG. 22 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0215]
FIG. 23 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0216]
24 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0217]
25 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0218]
26 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0219]
27 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

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[0220]
28 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0221]
29 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0222]
30 is a cross-sectional view of a main portion of a semiconductor substrate showing a method of manufacturing a DRAM which is Embodiment 1 of the present invention.

[0223]
31 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0224]
32 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0225]
33 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0226]
34 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0227]
35 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0228]

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36 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0229]
FIG. 37 is a main-portion cross-sectional view of the semiconductor substrate, showing the method of manufacturing the DRAM which is the first embodiment of the present invention.

[0230]
38 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0231]
39 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0232]
40 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0233]
41 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the first embodiment of the present invention.

[0234]
42 is a fragmentary cross-sectional view of a semiconductor substrate showing a DRAM that is Embodiment 2 of the present invention.

[0235]
43 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the second embodiment of the present invention.

[0236]
44 is a fragmentary cross-sectional view of the semiconductor substrate showing the method of

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manufacturing the DRAM according to the second embodiment of the present invention.

[0237]
45 is a fragmentary cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to a third embodiment of the present invention.

[0238]
46 is a fragmentary cross-sectional view of a semiconductor substrate showing a DRAM that is Embodiment 4 of the present invention.

[0239]
47 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to a fifth embodiment of the present invention.

[0240]
48 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to a fifth embodiment of the present invention.

[0241]
49 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to a fifth embodiment of the present invention.

[0242]
50 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to a fifth embodiment of the present invention.

[0243]
51 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to a fifth embodiment of the present invention.

[0244]
FIG. 52 is a partial cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the fifth embodiment of the present invention.

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[0245]
53 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to a fifth embodiment of the present invention.

[0246]
54A and 54B are partial cross-sectional views of a semiconductor substrate showing a method of manufacturing a DRAM according to a sixth embodiment of the present invention.

[0247]
55 (a) and 55 (b) are partial cross-sectional views of a semiconductor substrate showing a method of manufacturing a DRAM according to a sixth embodiment of the present invention.

[0248]
56 is a graph showing the performance of the capacitive insulating film forming the information storage capacitive element of the DRAM of the sixth embodiment of the present invention.

[0249]
57 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to a seventh embodiment of the present invention.

[0250]
FIG. 58 is a partial cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the seventh embodiment of the present invention.

[0251]
59 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to an eighth embodiment of the present invention.

[0252]
60 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to an eighth embodiment of the present invention.

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[0253]
61 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to an eighth embodiment of the present invention.

[0254]
62 is a partial cross-sectional view of the semiconductor substrate showing the method of manufacturing the DRAM according to the eighth embodiment of the present invention.

[0255]
63 is a partial cross-sectional view of a semiconductor substrate showing a method of manufacturing a DRAM according to an eighth embodiment of the present invention.

[0256]
64 is a partial enlarged cross-sectional view showing an example of a lower electrode constituting the information storage capacitive element.

[0257]
Explanation of symbols

[0258]
1 semiconductor substrate 1A semiconductor chip 2 silicon oxide film 3 silicon nitride film 4 photoresist film 5 element isolation groove 5a groove 6 thin silicon oxide film 7 silicon oxide film 8 silicon nitride film 9 photoresist film 10 n-type semiconductor region 11 p-type well 12 n-type well 13 gate oxide film 14 gate electrode 14A gate electrode 14B gate electrode 14C gate electrode 15 silicon nitride film 16 photoresist film 17 p- type semiconductor region 18 n- type semiconductor region 19 n type semiconductor region 20 silicon nitride film 20a Sidewall spacer 21 Photoresist film 22 p + type semiconductor region 23 n + type semiconductor region 24 SOG film 25 Silicon oxide film 26 Silicon oxide film 27 Photoresist film 28 Contact hole 29 Contact hole 30 Plug 31 Silicon oxide film 32 Photoresist film 33 photoresist film 34 contact hole 35 contact hole 36 contact hole 37 contact hole 38 first layer wiring 40 silicon nitride film 41 photoresist film 42 silicon oxide film 43 sidewall spacer 44 SOG film 45 silicon oxide film 46 silicon nitride film 47 photo Resist film 48 Through hole 49 Plug 53 Silicon oxide film 54 Photoresist film 55 Groove 56 Polycrystalline silicon film 57 Silicon oxide film 58 Photoresist film 60 Lower electrode (Ta2O5 film) 61 Capacitive insulating film (tantalum oxide film) 62 TiN film (Upper electrode) 63 Photoresist film 64 Silicon oxide film 65 SOG films 66a, 66b Through

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hole 67 Plug 68 Second layer wiring 69 Second layer wiring 70 Metal plug 71 Metal plug 72 Lower electrode 73 Photoresist film 74 Lower electrode 75 Upper part Electrode 76 Silicon oxide film 77 Photoresist film 78 Silicon oxide film 79 SOG film 80 Silicon oxide film 81 Metal plug 82 Titanium nitride film 83 Titanium oxide film 84 Tantalum oxide film 85 Titanium nitride film 86 Tantalum oxide film 87 Titanium oxide film 88 Titanium nitride Film 89 Organic matter 90 Upper electrode (titanium nitride film) 91 Connection hole 92 Plug 93 Silicon nitride film 94 Silicon oxide film 95 Photoresist film 96 SOG film 97 Silicon oxide film 98 Through hole 99 Plug 100 Second layer wiring 101 Hemispherical silicon BL Bit line C Information storage capacitor MA RY memory array Qn n-channel type MISFET Qp p-channel type MISFET Qs MISFETSA for memory cell selection SA sense amplifier WD word driver

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1.

A memory cell selection MISFET and a cylindrical lower electrode which is connected in series with the memory cell selection MISFET and has an opening portion above, and capacitive insulation formed in contact with at least the cylindrical inner surface of the lower electrode. A memory cell is formed by a film and an information storage capacitive element having an upper electrode formed to face at least the cylindrical inner surface of the lower electrode through the capacitive insulating film, and the memory cell is arranged. A method of manufacturing a semiconductor integrated circuit device having a memory cell array region and a peripheral circuit region around the memory cell array region, comprising: (a) adding the memory cell selecting MISFET and the memory cell selecting MISFET to the memory cell array region on a main surface of a semiconductor substrate. After forming a peripheral circuit MISFET in the peripheral circuit region of the main surface of the semiconductor substrate, a first film having a film thickness corresponding to the height of the lower electrode is formed on the memory cell selecting MISFET and the peripheral circuit MISFET. Depositing an insulating film, (b) forming a groove by opening the first insulating film above the memory cell selection MISFET, and (c) forming the first insulating film including the inside of the groove. A step of depositing a first conductive film which becomes a part of the lower electrode in a film thickness that does not fill the groove on the upper part, and (d) a second conductive film which fills the concave part of the first conductive film formed in the groove Forming an insulating film and exposing the first conductive film above the first insulating film; (e) etching the first conductive film to leave the first conductive film only inside the groove. , (F) removing the second insulating film filling the recess to form the lower electrode, (g) forming the capacitive insulating film on the surface of the lower electrode, (h) the capacitive insulating And a step of depositing a second conductive film on the film and patterning the second conductive film to form the upper electrode.

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2.

2. The method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein after the step (f), the upper layer portion of the first insulating film is removed to expose a part of the upper portion of the lower electrode, A method of manufacturing a semiconductor integrated circuit device, comprising the step of: after the step (h), forming a third insulating film on the entire surface of the semiconductor substrate and flattening the surface.

3.

3. The method of manufacturing a semiconductor integrated circuit device according to claim 2, wherein a connection hole is opened in the peripheral circuit region of the first insulating film from which an upper layer portion is removed, and the second conductive film is deposited at the same time. A method of manufacturing a semiconductor integrated circuit device, comprising: filling a connection hole, and patterning the second conductive film in the peripheral circuit region at the same time as patterning the second conductive film to form a plug or a wiring.

4.

2. The method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein after the step (e), a step of forming a photoresist film covering the first insulating film in the peripheral circuit region, the step (f). In the above step, the second insulating film is removed simultaneously with the removal of the first insulating film in the memory cell array region by a wet etching method using the photoresist film as a mask, and the first insulating film is formed in the peripheral circuit region. Forming the cylindrical lower electrode having an opening portion while leaving the remaining portion, and after the step (h), a third insulating film is formed on the entire surface of the semiconductor substrate to flatten the surface. A method of manufacturing a semiconductor integrated circuit device, comprising:

5.

The method for manufacturing a semiconductor integrated circuit device according to claim 4, wherein the fourth insulating film having an etching rate different from that of the first insulating film and the second insulating film is formed on the semiconductor substrate before depositing the first insulating film. And a step of etching the fourth insulating film in the memory cell array region to remove the lower electrode after the lower electrode is formed.

6.

A memory cell selection MISFET, a cylindrical lower electrode connected in series to the memory cell selection MISFET and having an opening at an upper portion, a capacitive insulating film

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formed on the surface of the lower electrode, and the capacitive insulating film. A memory cell is formed by an information storage capacitive element having an upper electrode formed to face the lower electrode via a memory cell array region in which the memory cell is arranged, and a peripheral circuit around the memory cell array region. A method of manufacturing a semiconductor integrated circuit device having a region, the method comprising: (a) forming the memory cell selecting MISFET on a main surface of a semiconductor substrate and then forming an information storage capacitor element on the upper surface thereof;) Depositing a first insulating film on the main surface of the semiconductor substrate with a film thickness equal to or greater than the height of the information storage capacitive element, (c) the first insulating film in the peripheral circuit region. Forming a photoresist film covering the photoresist, and then removing the first insulating film in the memory cell array region by a wet etching method using the photoresist film as a mask, (d) a third insulating film over the entire surface of the semiconductor substrate. And a step of flattening the surface of the semiconductor integrated circuit device.

7.

7. The method for manufacturing a semiconductor integrated circuit device according to claim 2, wherein the step of planarizing the surface of the third insulating film is the first step of applying an SOG film, or the information storage. The semiconductor integrated circuit, which is a second step of etching by CMP an insulating film deposited by vapor phase epitaxy with a film thickness equal to or greater than the height of a capacitor element. Device manufacturing method.

8.

The method for manufacturing a semiconductor integrated circuit device according to claim 1, wherein the second conductive film is deposited so as to fill a recess formed by the tubular shape of the lower electrode, A method for manufacturing a semiconductor integrated circuit device, which comprises flattening a surface.

9.

A memory cell selection MISFET and a cylindrical lower electrode which is connected in series with the memory cell selection MISFET and has an opening portion above, and capacitive insulation formed in contact with at least the cylindrical inner surface of the lower electrode. A memory cell is formed by a film and an information storage capacitive element having an upper electrode formed to face at least the cylindrical inner surface of the lower electrode through the capacitive insulating film, and the memory cell is arranged. A semiconductor integrated circuit device having a memory cell array region and a peripheral circuit region around the memory cell array region, wherein an insulating film having a film thickness corresponding to the height of the information storage capacitive element is provided in the peripheral circuit region. Then, the

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first structure in which the step between the memory cell array region and the peripheral circuit region is eliminated, and the concave portion formed by the lower electrode forming the information storing capacitive element constitutes the information storing capacitive element. In a second configuration in which the upper electrode is embedded, the information storage capacitive element is formed on the memory cell selection MISFET, and the information storage capacitive element includes the lower electrode and the memory cell selection MISFET. Any one of a cylindrical electrode formed of a part of a plug to be connected, and a third structure integrally formed with a cylindrical capacitive element including a concentric cylindrical electrode formed on the outer periphery of the plug through a capacitive insulating film. A semiconductor integrated circuit device having the above configuration.

10.

A memory cell selecting MISFET, a memory cell selecting MISFET connected in series, a lower electrode, a capacitance insulating film formed in contact with the lower electrode, and a lower electrode facing the lower electrode via the capacitance insulating film. What is claimed is: 1. A semiconductor integrated circuit device having a memory cell including an information storage capacitive element having an upper electrode formed, wherein both the lower electrode and the upper electrode are made of a conductive material containing at least titanium nitride. A semiconductor integrated circuit device, wherein the insulating film comprises an insulating film containing at least polycrystalline tantalum oxide.

11.

11. The semiconductor integrated circuit device according to claim 10, wherein a plug connecting said memory cell selecting MISFET and said lower electrode is made of a conductive material containing titanium nitride as a main component. ..

12.

12. The semiconductor integrated circuit device according to claim 10, wherein a titanium oxide film having a thickness of 10 nm or less is formed at an interface between the lower electrode and the capacitive insulating film. Circuit device.

13.

A memory cell selecting MISFET, a memory cell selecting MISFET connected in series, a lower electrode, a capacitance insulating film formed in contact with the lower electrode, and a lower electrode facing the lower electrode via the capacitance insulating film. A method for manufacturing a semiconductor integrated circuit device having a memory cell including an information storage capacitor having an upper electrode formed therein, comprising: (a)

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depositing a titanium nitride film to be the lower electrode by a CVD method, A step of heat-treating the titanium nitride film in a non-oxidizing atmosphere, (b) depositing a tantalum oxide film by a CVD method and heat-treating in a non-oxidizing atmosphere to crystallize the tantalum oxide film to convert it into a polycrystalline tantalum oxide film. Step (c) heat-treating the polycrystalline tantalum oxide film in an oxidizing atmosphere to modify the polycrystalline tantalum oxide film and simultaneously form titanium oxide at the interface between the titanium nitride film and the polycrystalline tantalum oxide film. A method of manufacturing a semiconductor integrated circuit device, comprising the steps of: (d) depositing a titanium nitride film to be the upper electrode by a CVD method.

14.

14. The method for manufacturing a semiconductor integrated circuit device according to claim 13, further comprising a step of forming a titanium oxide film on the surface of the titanium nitride film after the step (a). Manufacturing method.

15.

A memory cell selecting MISFET, a memory cell selecting MISFET connected in series, a lower electrode, a capacitance insulating film formed in contact with the lower electrode, and a lower electrode facing the lower electrode via the capacitance insulating film. A method of manufacturing a semiconductor integrated circuit device having a memory cell including an information storage capacitive element having a formed upper electrode, wherein a part of a plug connecting the memory cell selection MISFET and the lower electrode is formed. A method for manufacturing a semiconductor integrated circuit device, wherein the bit line is formed at the same time as the memory cell selecting MISFET.

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(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

(72) Inventor: Ito, Takashi
408, Noborito Tama-ku
Kawasaki-shi Kanagawa 214(JP)

(72) Inventor: Horie, Hiroshi
Tanabeso 202 1-4, Katsuse
Ebina-shi Kanagawa 243-04(JP)

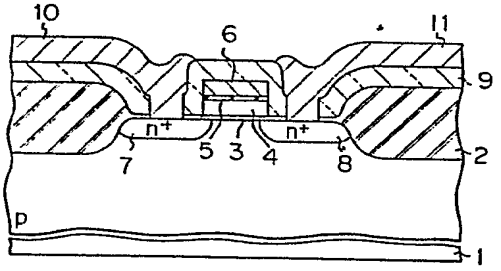
(72) Inventor: Sugii, Toshihiro
Dai 2 Yamato Haitsu 305 312, Shukugawara
Tama-ku Kawasaki-shi Kanagawa 214(JP)

(74) Representative: Fane, Christopher Robin King et al,
HASELTINE LAKE & CO. Hazlitt House 28 Southampton
Buildings Chancery Lane
London, WC2A 1AT(GB)

(54) **Wiring layers in semiconductor devices.**

(57) A semiconductor device has an electrode wiring layer including a first conductive layer (4) extending over an active region of the device, and a second conductive layer (6) spaced from the first conductive layer by a barrier layer (5) used for reaction prevention. The barrier layer consists of an insulating film having a thickness thin enough for flow of a tunnel current. In this way a wiring layer can be produced satsifactorily such as to have lower resistivity than an otherwise comparable prior wiring layer.

Fig. 4



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WIRING LAYERS IN SEMICONDUCTOR DEVICES

The present invention relates to wiring layers in a semiconductor device.

Polycrystalline silicon is often used as the material of electrodes or wiring in the production of a semiconductor device, particularly, an integrated circuit (IC). Since polycrystalline silicon is a semiconductor, it has a high resistivity compared to a metal. To lower the resistivity, impurities such as phosphorous, arsenic, boron, or the like are doped in the polycrystalline silicon. These have not, however, managed to reduce the resistivity to the desired level. The still high resistivity of the polycrystalline silicon therefore causes delays in signal propagation.

Recently, to solve this problem, use has been proposed of a high melting point metal, for example, molybdenum or tungsten, or a silicide thereof. Materials such as molybdenum or tungsten, however, are not very suited to production processes of semiconductor devices such as IC's. For example, when molybdenum or tungsten is deposited on a thin silicon dioxide film and heat-treated at a high temperature, the high melting point metal locally reacts with the silicon dioxide and significantly reduces the breakdown voltage of the silicon dioxide film. Further, when a high concentration doped semiconductor contacts molybdenum or tungsten, the contact resistance is remarkably increased.

Unexamined Japanese Patent Publication (Kokai) No. 56-79450 (filed on December 30, 1979) discloses an electrode or wiring in a semiconductor device formed by placing or burying molybdenum or tungsten at a part of a polycrystalline silicon layer, but the electrode or wiring can still suffer from the problems such as are mentioned above.

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According to one aspect of the present invention there is provided a semiconductor device including an electrode wiring layer consisting of an upper conductive layer and, interspaced with a barrier layer used for reaction prevention, a lower conductive layer contacting an active region; the said barrier layer consisting of an insulating film having a thickness thin enough for the flow of a tunnel current.

An embodiment of the present invention can be made so as to provide a semiconductor device having improved signal propagation.

In a semiconductor device embodying the present invention an electrode or wiring can be produced so as to have a low contact resistance at the interface with the polycrystalline silicon film.

Reference will now be made, by way of example, to the accompanying drawings, wherein:

Figures 1 to 4 show cross-sectional views illustrating a production process for a semiconductor device embodying the present invention;

Figure 5 is a histogram;

Figures 6 to 8 show graphs;

Figures 9A and 9B show I-V characteristics in a conventional polycrystalline silicon gate and in a gate in an embodiment of the present invention, respectively;

Figure 10 shows a cross-sectional view illustrating an ohmic contact electrode in an embodiment of the present invention; and

Figure 11 shows a cross-sectional view illustrating a rectifying contact electrode in an embodiment of the present invention.

Embodiments of the present invention will now be described with reference to the drawings.

Figures 1 to 4 are cross-sectional views illustrating a production process for an embodiment according to the present invention.

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The embodiment is described using a metal-insulator-semiconductor (MIS) field-effect-semiconductor device.

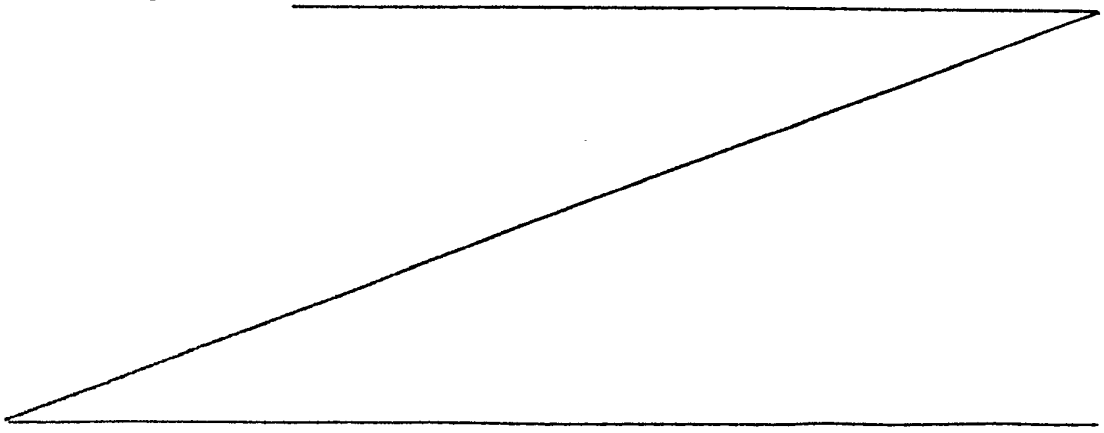
As shown in Figure 1, a p-type silicon semiconductor substrate 1 has formed thereon a field insulating film 2, consisting of silicon dioxide, by a selective thermal oxidation process. A gate insulating film 3 is formed by a thermal oxidation process on the surface of an active region of the substrate 1.

As shown in Figure 2, a polycrystalline silicon film 4, having a thickness of about 0.1 μm, is formed by a chemical vapor deposition (CVD) process. Phosphorus ions are doped in a high concentration, for example, $10^{20}/cm^3$ or more, into the polycrystalline silicon film 4 by a vapor diffusion process, ion implanting process, or the like.

The surface of the polycrystalline silicon film 4 then has formed thereon a silicon nitride film 5, having a thickness of about 20 Å (2 nm), by heat treatment for five minutes at a temperature of 700°C in an atmosphere of pure ammonia gas.

The silicon nitride film 5 may also be formed by a CVD process using, for example, mono-silane (SiH_4) and ammonia (NH_3) gas or by a nitriding process using energy of ammonia plasma or light irradiation.

This thickness of the silicon nitride film 5 may be from 10 to 50 Å (1 to 5 nm), allowing the flow of a tunnel current



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upon application of voltage to the silicon nitride film 5 during operation of the semiconductor device.

The silicon nitride film 5 has formed on it, for example, a molybdenum film having a thickness of about 0.3 μm by a well known sputtering process or CVD process. After that, heat treatment is carried out at a temperature of, for example, about 1000°C to increase the density of the molybdenum film 6 and thus reduce the resistivity of the molybdenum.

During the heat treatment, the silicon nitride film 5 acts as a barrier preventing the polycrystalline silicon film 4 from reacting with the molybdenum film 6, thereby maintaining the low resistivity.

When no silicon nitride film 5 is formed between the polycrystalline silicon film 4 and the molybdenum film 6, molybdenum reacts with the polycrystalline silicon to form molybdenum silicide. Molybdenum has a sheet resistivity of 0.3 Ω/□, while molybdenum silicide has a sheet resistivity of 3 Ω/□. Since impurities doped into the polycrystalline silicon film 4 are not absorbed into the molybdenum film 6 due to the presence of the silicon nitride film 5, the threshold voltage in a gate electrode of an MIS field-effect semiconductor device embodying the present invention can be maintained at substantially the same level as in a conventional silicon gate of an MIS field-effect semiconductor device.

After forming the molybdenum film, as shown in Fig. 3, the molybdenum film 6, silicon nitride film 5, and the polycrystalline silicon film 4 are patterned by reactive ion etching using a conventional lithographic technique to form a two-layer gate electrode consisting of a molybdenum film and a polycrystalline silicon film. After that, required wiring is formed as necessary.

An shown in Fig. 4, arsenic ions (As^+) are then injected into the obtained structure by ion implantation, while the ion implanted structure is heat-treated so

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that an n^+ type source region 7 and an n^+ type drain region 8 are formed in the p-type silicon semiconductor substrate 1.

A phospho-silicate glass (PSG) film 9 is formed on the obtained structure. The PSG film 9 is patterned by a conventional lithographic technique to form electrode contact windows. Aluminum film is formed on the entire surface of the obtained structure by, for example, a spattering process. The aluminum is patterned by a conventional lithographic technique to form a source electrode 10 and a drain electrode 11. Well-known techniques are applied to the thus obtained structure to form the MIS field effect semiconductor device.

Figure 5 is a histogram illustrating the dielectric strength between a gate electrode and a semiconductor substrate in an embodiment of the present invention.

In Fig. 5, the region designated by reference numeral 12 relates to an MIS field-effect semiconductor device embodying the present invention. In this case, the thickness of the gate insulating film 3 is 200 Å (20 nm). The dielectric strength is 16V to 20V, which is a satisfactory value. The sheet resistivity of the two-layer gate electrode is about 0.5 Ω/□.

On the other hand, the region designated by reference numeral 13 relates to an MIS field-effect semiconductor device which has no silicon nitride film 5 between the polycrystalline silicon film 4 and the molybdenum film 6. In this case, the dielectric strength is remarkably decreased and the sheet resistance becomes about 5 Ω/□.

In the above embodiments, phosphorous ions were doped into the polycrystalline silicon. However, impurities such as boron ions or arsenic ions may also be used. Such impurities may be injected into the silicon substrate from above the molybdenum film 6 because the polycrystalline silicon film acts as a mask.

Further, in the above embodiments, molybdenum was

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used as the high melting point metal. However, other high melting point metals, such as molybdenum silicide or tungsten (W), chromium (Cr), titanium (Ti), zirconium (Zr), hafnium (Hf), platinum (Pt), palladium (Pd), nickel (Ni), cobalt (Co), iridium (Ir), tantalum (Ta), or silicides thereof may also be used.

Additionally, in an embodiment of the present invention, a silicon nitride film acting as a barrier layer is placed between the polycrystalline silicon film and the film consisting of the high melting point metal or silicide thereof. However, the barrier layer is so thin that it has only a small effect on the electrical properties and allows a tunnel current to flow therein.

The electrical properties of an embodiment of the invention are illustrated in Figs. 6 to 9B.

Figure 6 is a graph illustrating the relationship between the threshold voltage and effective channel length.

In Fig. 6, "poly Si gate" shows prior art data, and "MTP gate" shows data of an embodiment of the invention. "MTP" means "molybdenum tunnel nitride polycrystalline silicon".

As shown in Fig. 6, the threshold voltage of an embodiment of the invention is substantially the same as that of the prior art. "Tox" means gate oxide. "Vd" means drain voltage.

Figure 7 is a graph illustrating the relationship between sheet resistance and annealing temperature in an embodiment of the present invention. As shown in Fig. 7, the sheet resistance (Rs) is decreased as the annealing temperature is increased. Although the data is not illustrated in Fig. 7, the sheet resistance in the prior art is increased as the annealing temperature is increased, because of the reaction of the molybdenum or other metal with the silicon dioxide, as explained above.

Figure 8 is a graph illustrating the relationship between gate voltage (Vg) and the ratio (C/C_{ox}) of

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capacitance of an oxide (C_{ox}) to the capacitance of an MOS diode embodying the present invention. As shown in Fig. 8, the same curve is followed when the gate voltage is increased and the gate voltage is continuously decreased. Thus, no charge-up phenomenon can be seen between the polycrystalline silicon and molybdenum layers.

Figures 9A and 9B show I-V characteristics in a conventional polycrystalline silicon gate and in a gate (MTP) in an embodiment of the invention, respectively. As shown in Figs. 9A and 9B, the I-V characteristics of the prior art and the present embodiment are substantially the same. The data in Figs. 9A and 9B was obtained using a structure having a tunnel oxide thickness of 25 nm, effective channel length (L_{eff}) of 1.3 μm, and effective channel width (W_{eff}) of 10 μm.

An embodiment of the invention is preferably concerned with an ohmic contact electrode as shown in Fig. 10 and/or a rectifying contact electrode as shown in Fig. 11.

In Fig. 10, the polycrystalline silicon film 4 is contacted with the silicon substrate in ohmic contact.

In Fig. 11, the polycrystalline silicon film 4 doped, for example, with p^+ type impurities is contacted with the silicon substrate 1 having, for example, n region 9 in rectifying contact.

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CLAIMS:

1. A semiconductor device having an electrode wiring layer extending over a main surface of the semiconductor body of the device, characterised in that the wiring layer comprises a first conductive layer (4) sandwiched between the said main surface and a second conductive layer (6), there being interposed between the first and second conductive layers a barrier layer (5) for preventing the occurence of a reaction between the first and second conductive layers during formation of the latter, the said barrier layer being sufficiently thin to permit the flow of tunnel current therethrough when the device is in use.

2. A device as claimed in Claim 1, wherein the first conductive layer (4) extends over a gate insulating film which separates the first conductive layer from the said main surface at a gate region of the device.

3. A semiconductor device with an electrode wiring layer including:

a first, lower conductive layer contacting an active region; and

a second, upper conductive layer interspaced from the first layer by a barrier layer used for reaction prevention;

said barrier layer consisting of an insulating film having a thickness thin enough for flow of a tunnel current.

4. A semiconductor device as claimed in Claim 3, wherein said active region is a gate insulating film region in a gate portion of an MIS semiconductor device.

5. A semiconductor device as claimed in any preceding claim, wherein the said barrier layer consists of a silicon nitride film.

6. A semiconductor device as claimed in any preceding claim, wherein the said first conductive layer consists of polycrystalline silicon and the said second conductive layer consists of a high melting point metal or a

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silicide thereof.

7. A semiconductor device as claimed in Claim 6, wherein the said barrier layer comprises a direct nitride film of a surface region of the first conductive layer.

8. A semiconductor device as claimed in Claim 3, wherein said active region consists of a semiconductor region on which an ohmic electrode is arranged and said first conductive layer is in ohmic contact with the active layer.

9. A semiconductor device as claimed in Claim 3, wherein said active region consists of a semiconductor region on which a rectifying electrode is arranged and said first conductive layer is in rectifying contact with the active region.

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Fig. 1

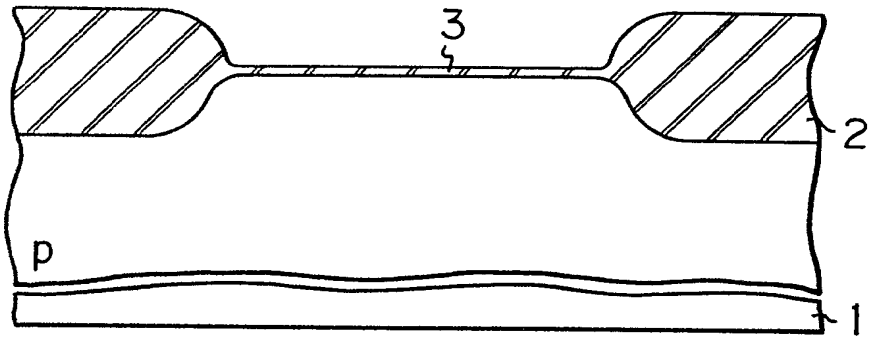
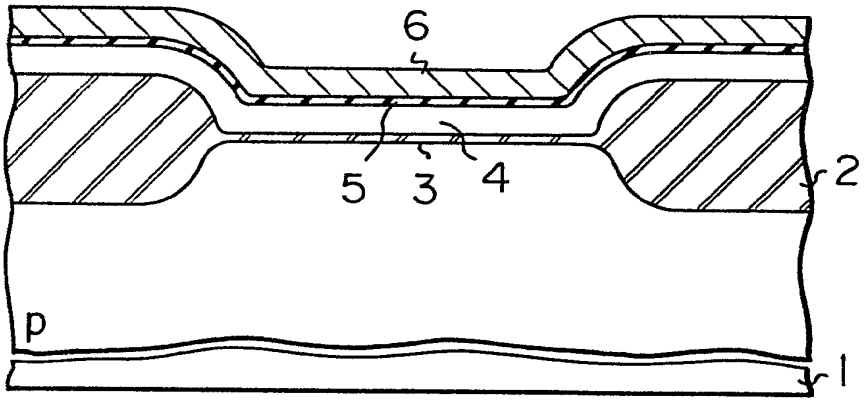


Fig. 2



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Fig. 3

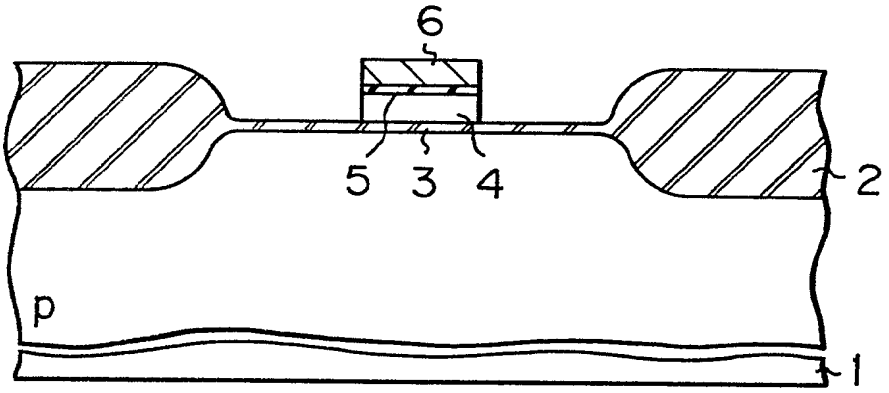
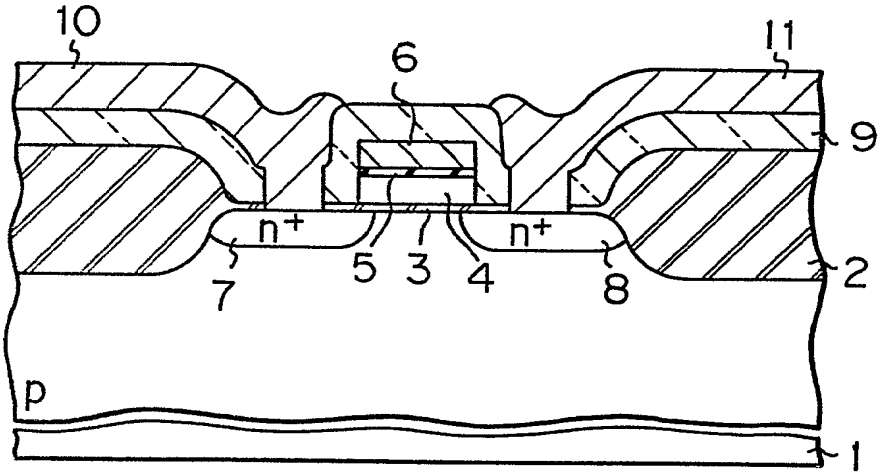
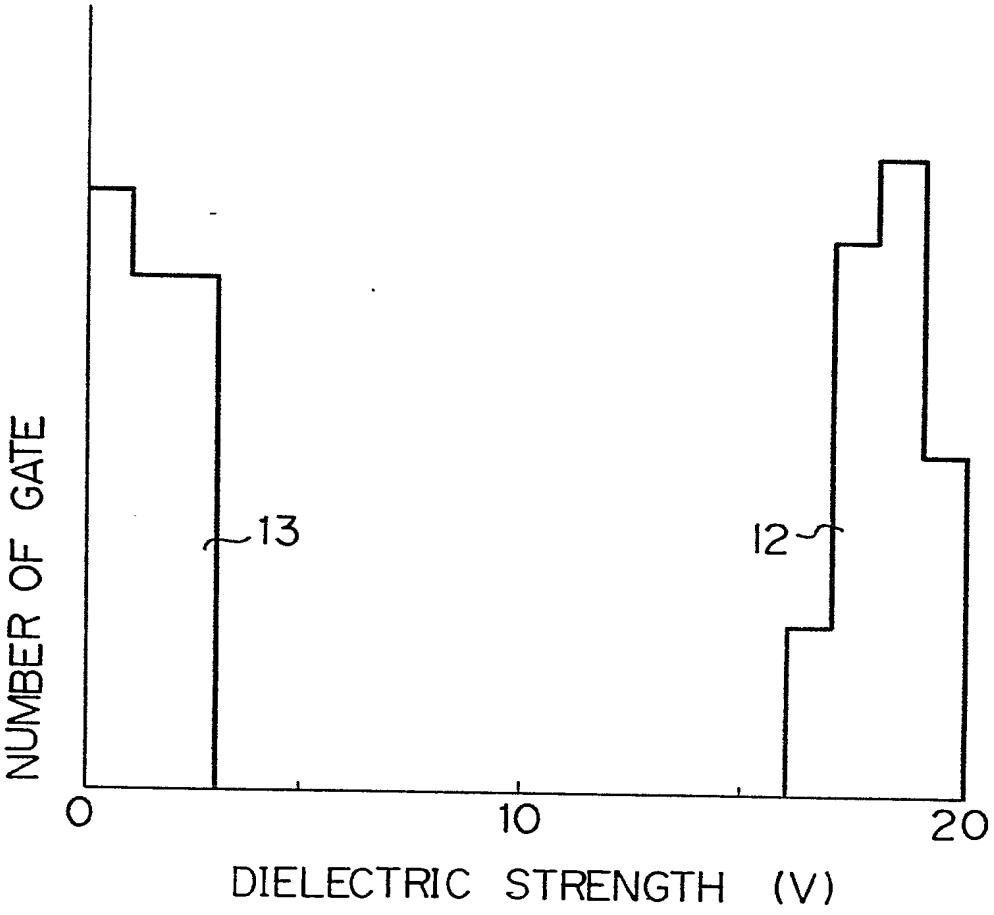


Fig. 4



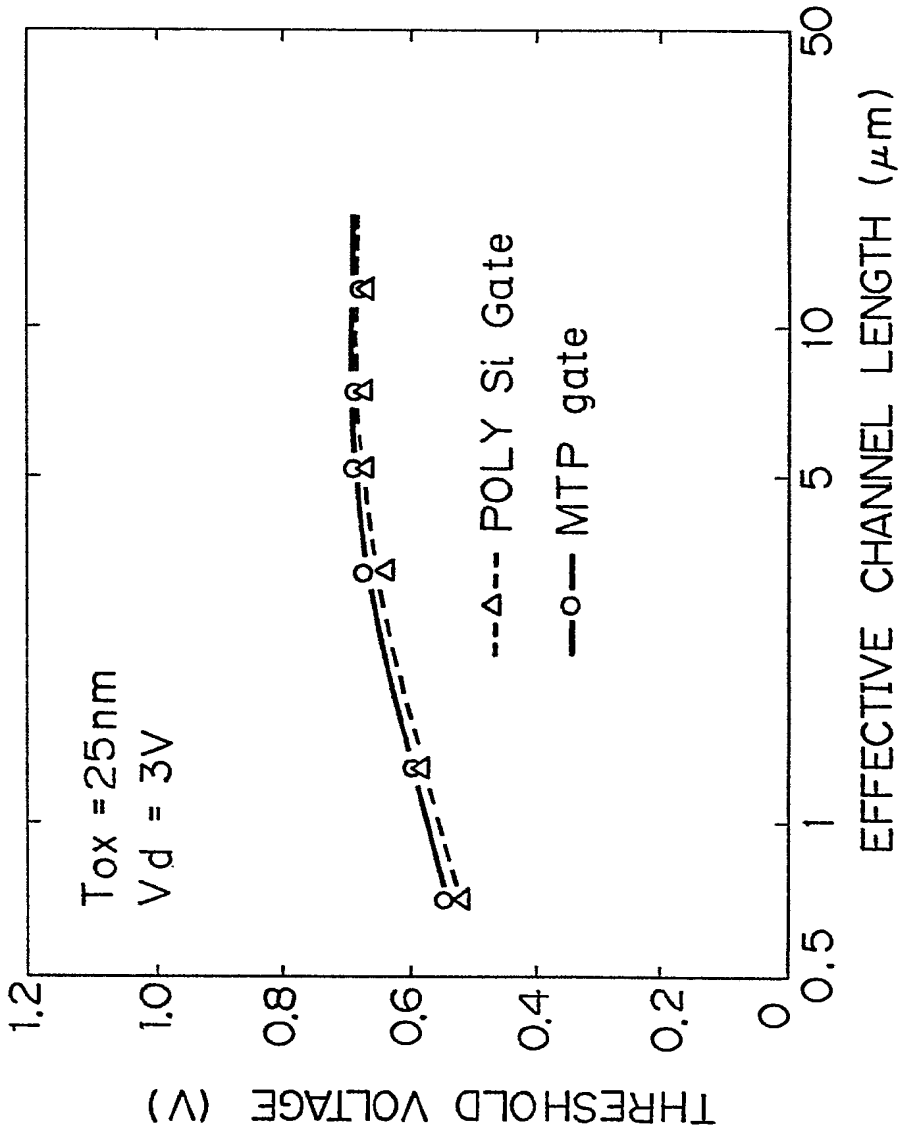
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Fig. 5



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Fig. 6



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Fig. 7

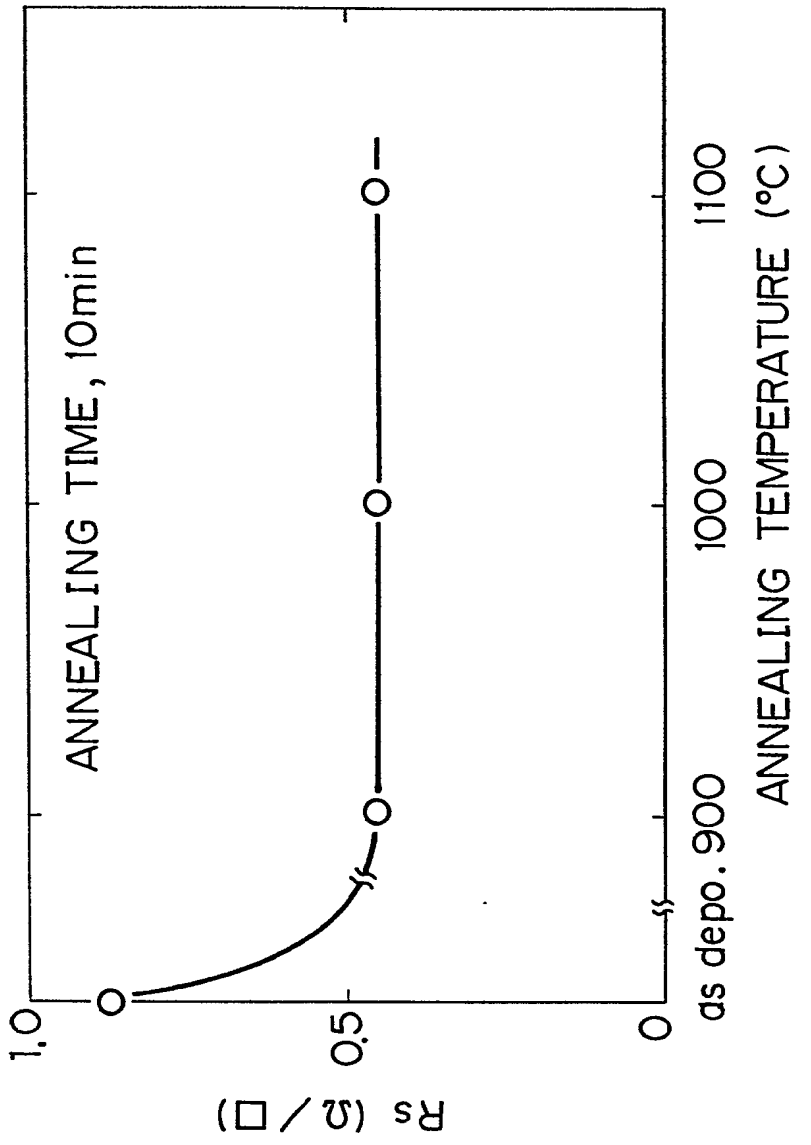
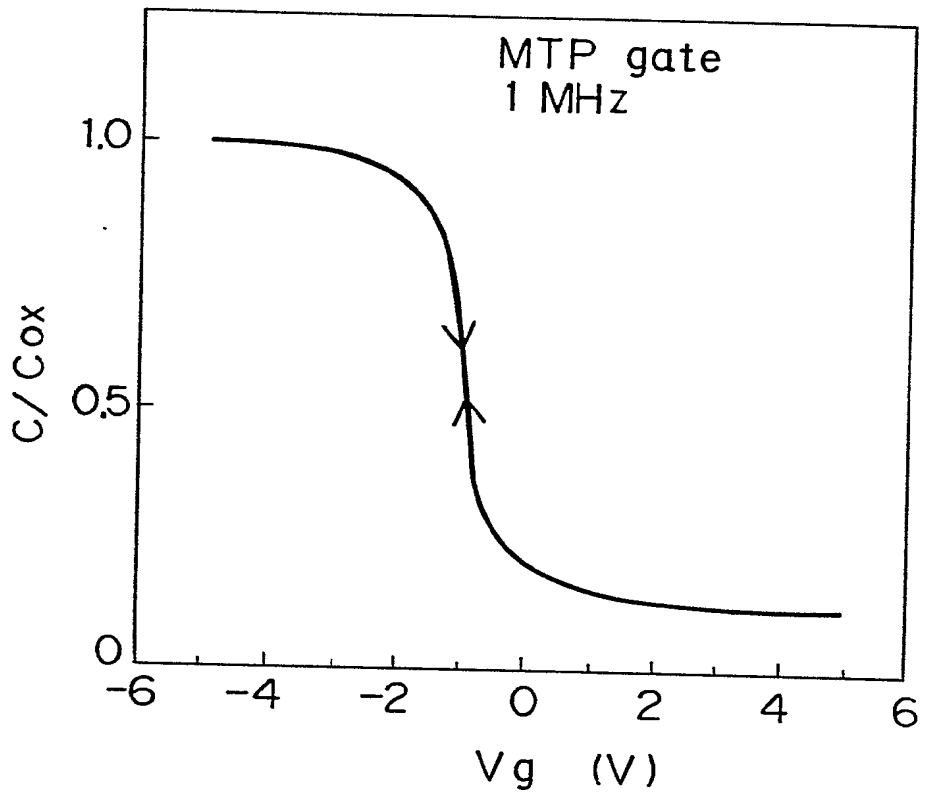
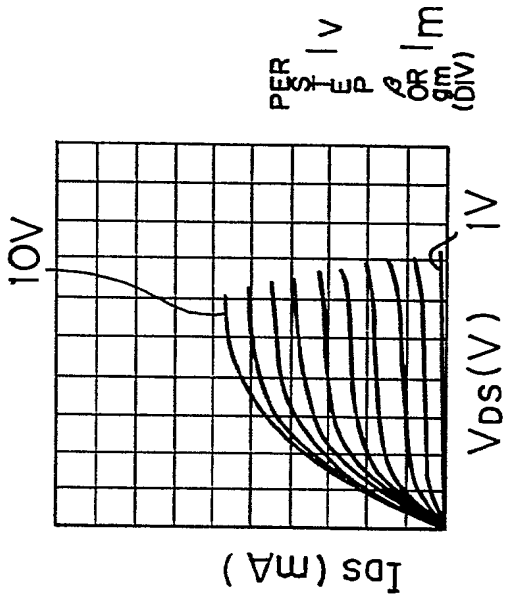

ANNEALING TIME, 10min
Rs (Ω/□)
1.0
0.5
0
as depo.
900
1000
1100
ANNEALING TEMPERATURE (°C)

Fig. 8



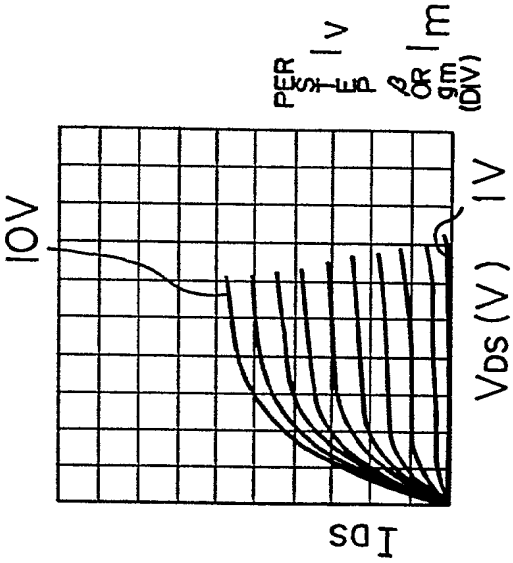
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Fig. 9A



POLY SiGATE

Fig. 9B



MTP GATE

Tox = 25nm L_{eff} = 1.3 μm W_{eff} = 10 μm

I-V CHARACTERISTICS

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Fig. 10

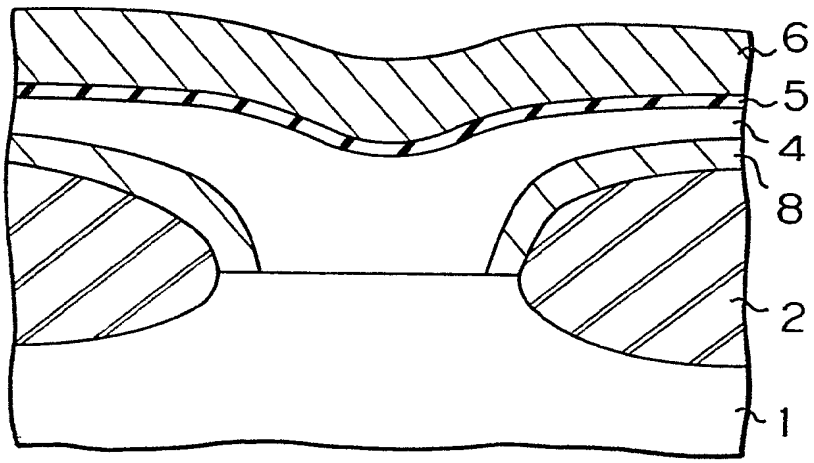
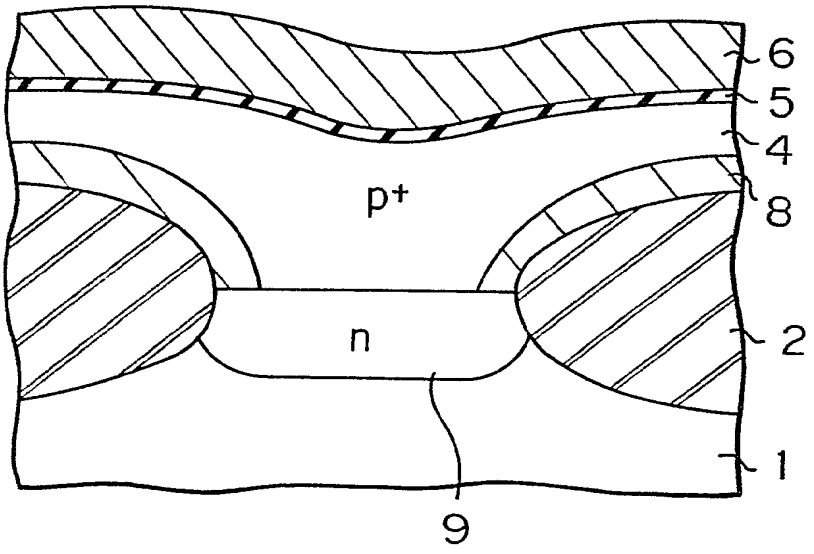


Fig. 11



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European Patent Office

EUROPEAN SEARCH REPORT

0168125
. Application number

EP 85 30 1892

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl 4)
A	US-A-4 141 022 (SIGG et al.) * Column 4, line 28 - column 5, line 25 *	1-4,8	H 01 L 29/40 H 01 L 23/52
A	PATENT ABSTRACTS OF JAPAN, vol. 6, no. 251, 10th December 1982, page (E-147) (1129); & JP-A-57-149751 (NIPPON DENKI) 16-09-1982	1-4,6	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 2, July 1979, New York, USA; T.M. REITH "Diffusion barrier process", page 558	1,9	
A	APPLIED PHYSICS LETTERS, vol. 32, no. 5, 1st March 1978, New York, USA; T. ITO "Thermally grown silicon nitride films for high-perfomance MNS devices", pages 330-331	7	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L 23/52 H 01 L 29/40

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	12-06-1985	GIBBS C.S.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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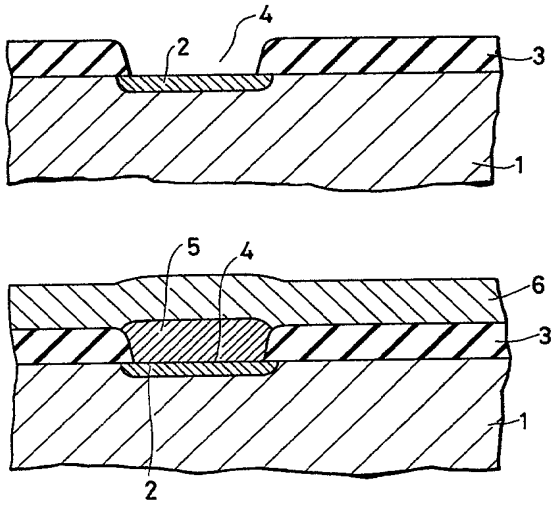
(71) Applicant: **Hitachi, Ltd., 5-1, Marunouchi 1-chome, Chiyoda-ku Tokyo 100 (JP)**

(72) Inventor: **Sugaki, Shojiro, 2-32-D302 Koyasu-cho, Hachioji-shi Tokyo (JP)**
Inventor: **Ogirima, Masahiko, 2-1-23 Nakai Shinjuku-ku, Tokyo (JP)**
Inventor: **Yamamoto, Naoki, 1-10-20 Shiba, Kawaguchi-shi Saitama-ken (JP)**

(74) Representative: **Paget, Hugh Charles Edward et al, MEWBURN ELLIS & CO. 2/3 Cursitor Street, London EC4A 1BQ (GB)**

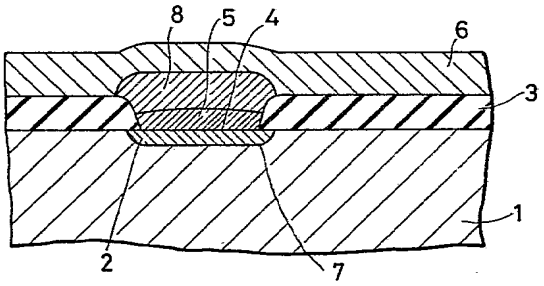
(54) **A method of forming an electrode of a semiconductor device.**

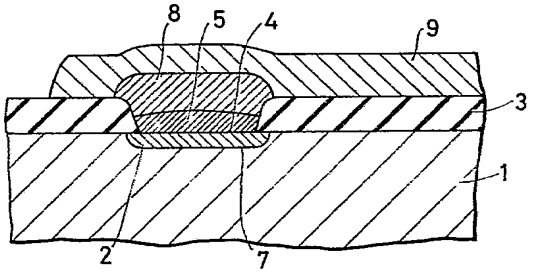
(57) To form an electrode in a semiconductor device, after a silicon layer (5) is selectively grown on that part of a silicon substrate surface on which the electrode is to be formed, the silicon layer (5) is reacted with a refractory metal (6) so as to form the electrode as a metal silicide layer (8). In this way, the problem of a metal layer ruining a pn-junction (7) in the substrate is avoided, and a device of high packaging density can be formed.



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"A method of forming an electrode of a semiconductor device"

The present invention relates to a method of forming an electrode of a semiconductor device, and more particularly (but not exclusively) to the formation of an electrode on a silicon wafer.

As is well known, the electrodes of various semiconductor devices are principally formed by using an Al alloy as the electrode material or by producing metal silicide directly on a silicon substrate.

The use of Al alloy as the electrode material has the merit that the process is simple and that manufacture is easy. Since, however, the Al alloy is readily alloyed with Si at the low temperature of about 500°C, Al penetrates into the Si substrate by the solid-phase diffusion reaction between Si and Al. If there is a thin diffusion layer in the Si substrate the Al which has penetrated into it passes through the diffusion layer easily, resulting in the disadvantages that junction shorting occurs and that the heat resistance is conspicuously low.

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The method of forming an electrode by forming metal silicide directly on the Si substrate, gives better heat resistance than the method using Al alloy. However, the metal silicide is formed by the solid phase reaction between a metal and the Si substrate, so that when it is intended to form a thick metal silicide layer, the lower part of the metal silicide extends into the Si substrate so that the interface between the silicide and the corresponding part of the Si substrate lies within the original Si substrate. Within the Si substrate, regions having opposite conductivity type to that of the Si substrate are usually formed. Therefore, when the Si-silicide interface is formed within the Si substrate, there is a risk that a junction is ruined by the metal silicide, so that the thickness of the metal silicide cannot be very large.

In order to solve this problem, there has been proposed a method in which a polycrystalline Si film heavily doped with an impurity is formed on the Si substrate in advance, and a metal film is deposited on the Si film to react with it, to form the metal silicide. This polycrystalline Si film can prevent spoiling of the junction within the substrate. Since, however the polycrystalline Si film needs to

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be formed in parts which are contact holes formed by a photoetching process, this method is unsuitable for the formation of a semiconductor device of high packaging density having a very fine structure.

Objects of the present invention are therefore to provide a method of forming the electrode of a semiconductor device which can ensure sufficient heat resistance of the electrode, which can avoid the risk of ruining a junction within a substrate and which can also be applied to the manufacture of an integrated circuit of high packaging density.

The present invention is set out in the claims. In the invention, a Si layer is formed on that selected part of the surface of a Si substrate on which an electrode is to be formed, and a metal film is deposited onto the Si layer so as to form metal silicide.

An embodiment of the invention will now be described by way of example with reference to the accompanying drawing, in which

Figures 1a to 1d are processing flow diagrams illustrative of the embodiment of the invention.

As shown in Figure 1a, an impurity-doped layer 2 is formed in the surface region of a single-crystal Si substrate by a well-known method such as thermal diffusion or ion implantation.

Using a well-known process such as thermal oxidation or chemical vapor deposition (CVD), a SiO_2 film 3 is deposited on the whole surface of the Si substrate. Thereafter, the part of the SiO_2 film overlying the impurity-doped layer 2 is selectively removed by the well-known photoetching process so as to form a contact hole 4.

In this example, the deposition of the SiO_2 film 3 and the formation of the contact hole 4 were carried out after the impurity-doped layer 2 had been formed. The impurity-doped layer 2 however may be formed after the deposition of the SiO_2 film 3 and the formation of the contact hole 4.

As shown in Figure 1b, using the well-known vapor epitaxial growth technique which employs $SiCl_4$ and H_2, a Si epitaxial layer 5 is selectively grown on the exposed surface of the Si substrate 1. Thereafter, a refractory metal film 6 of Mo, Ta, Ti, W or the like is deposited on the whole surface of the resultant substrate. Two or more such metals may be used jointly, or an alloy consisting of two or more such metals.

Subsequently, a heat treatment is conducted at about 500°C or above in a non-oxidizing atmosphere, so that a solid phase reaction takes place between the metal layer 6 and the Si layer 5, to form a metal

silicide layer 8 as shown in Figure 1c.

The temperature of this heat treatment should preferably be in the range 500°C - 1000°C. At below about 500°C, the metal silicide is difficult to form, and at above about 1000°C, the impurity-doped layer 2 spreads due to thermal diffusion and the pn-junction 7 deepens. The growth rate of the metal silicide depends greatly upon the atmosphere of the heat treatment. For example, the growth rate of the metal silicide is markedly higher in a hydrogen atmosphere than in a nitrogen atmosphere.

The thickness of the metal silicide layer 8 can be controlled to a desired value by control of the conditions of the heat treatment. In an example in which the heat treatment was conducted at 700°C in the hydrogen atmosphere for 1 hour, a tungsten silicide layer 8 about 500nm thick was obtained.

Even if the entire Si layer 5 reacts with the metal film 6, it is only necessary that the silicide film 8 produced does not pierce the impurity-doped layer 2 to destroy the junction 7. Therefore, when the thickness of the Si epitaxial layer 5 is made sufficiently great beforehand (roughly, greater than the thickness of the metal silicide layer to be formed), the formation of the metal silicide layer 8 can be

performed with a sufficient tolerance.

More specifically, when the Si epitaxial layer 5 is formed so as to be somewhat thick in advance, this layer 5 is not fully reacted in the formation of the metal silicide but is left unreacted to some degree as illustrated in Figure 1c. There is then no fear that the pn-junction 7 will be spoilt by the layer 8, and a contact having a high reliability can be formed very easily.

In the embodiment shown, the Si epitaxial layer 5 is formed on the impurity-doped layer 2. Since, however, the present invention requires only the formation of the metal silicide through the reaction with the refractory metal, it is possible to employ, instead of an Si epitaxial layer, a polycrystalline silicon layer or an amorphous silicon layer. It is difficult, however, to form an amorphous silicon layer on the selected part of the impurity-doped layer 2 without using a mask or the like. In contrast, an Si epitaxial or a polycrystalline silicon layer can be selectively grown on the impurity-doped layer 2 and these two are therefore favoured in practice.

After the metal silicide layer 8 has been formed, the refractory metal film 6 is etched and removed. The unreacted refractory metal film 6 can

be selectively etched and removed by employing an etchant whose etching rate for the metal is sufficiently greater than that of the metal silicide.

For example, if Mo is the refractory metal, the Mo film only is selectively removed with the Mo silicide layer left behind if a phosphoric acid-based solution is used as the etchant. If W is the refractory metal to form W silicide, the W film only is selectively removed with the W silicide layer left behind when a hydrogen peroxide liquid is used as the etchant.

Next a wiring metal film, e.g. of Al, is deposited on the whole surface of the resultant substrate and then its unnecessary parts are removed by photo-etching. A wiring layer 9 which is electrically connected with the metal silicide layer 8 is thus formed as shown in Figure 1d.

The metal silicide layer formed in the present invention can be used as the contact electrode for the impurity-doped layer within the Si substrate, for the electrode of a Schottky diode, etc. When using the metal silicide layer as the electrode of the Schottky diode, it is desirable to react the entire Si epitaxial layer with the metal silicide and to hold the metal silicide layer in direct contact with the silicon semiconductor substrate.

In the illustrated embodiment, the metal silicide layer is formed, the refractory metal layer is thereafter removed, and then the wiring layer of Al or the like is deposited so as to form the wiring. The present invention is not restricted to this order of method steps. By processing the unreacted refractory metal layer into a desired shape by photoetching, it can be used as the wiring in a variety of semiconductor devices, as the gate electrode of a MOS field effect transistor, etc. When employing the refractory metal in these ways, the metal silicide layer can be formed at the contact hole by heat treatment after the refractory metal has been processed into the desired shape by photoetching.

Since the metal silicide layer formed in the present invention can typically endure heat treatment at temperatures up to about 1,200°C, there is no risk of ruining the electrode if temperatures of various heat treatments which are conducted after the formation of the electrode are below about 1,100°C, and almost all the ordinary silicon processes can be performed without hindrance.

When wiring is formed from the unreacted part of the refractory metal used for forming the metal silicide, the heat resistance is excellent,

and the specific resistance is as low as at most $2 \times 10^{-5} \Omega \cdot cm$. Such wiring is therefore very suitable for various semiconductor integrated circuits.

In addition, according to the present invention, Si is selectively grown on the contact hole and is reacted with the refractory metal. Therefore, the metal silicide layer is formed in a self-aligning manner, and the method can be very easily applied to the formation of a large-scale integrated circuit having a very fine structure.

CLAIMS

1. A method of forming an electrode of a semiconductor device wherein a Si layer (5) is formed on a semiconductor substrate (1) and a metal layer (6) is formed on the Si layer to react therewith to form metal silicide electrode (8), characterized by the steps of:

(A) forming an insulating film (3) onto a surface of the semiconductor substrate (1) in a manner which exposes that part of the said surface on which the electrode is to be formed,

(B) selectively growing the Si layer (5) on the exposed surface of said semiconductor substrate (1),

(C) depositing a refractory metal layer (6) as said metal layer so as to cover at least said Si layer (5), and

(D) heating the resultant substrate to react said Si layer (5), and said refractory metal layer (6) to form a metal silicide layer (8).

2. A method according to claim 1 wherein after step (D) the following steps are performed:

(E) removing an unreacted part of said refractory metal layer (6) to expose a surface of said metal silicide layer (8), and

(F) forming a wiring layer (9) connected to said metal silicide layer (8).

3. A method according to claim 1 wherein after the step (D), the following step is performed:

(E') removing a predetermined part or parts of the unreacted part of said refractory metal layer (6) so as to form a wiring layer.

4. A method according to any one of claims 1 to 3, wherein said silicon layer (5) is a Si epitaxial layer, a polycrystalline Si layer or an amorphous Si layer.

5. A method according to any one of claims 1 to 4 wherein the refractory metal is at least one of Mo, Ta, Ti and W.

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FIG. 1a

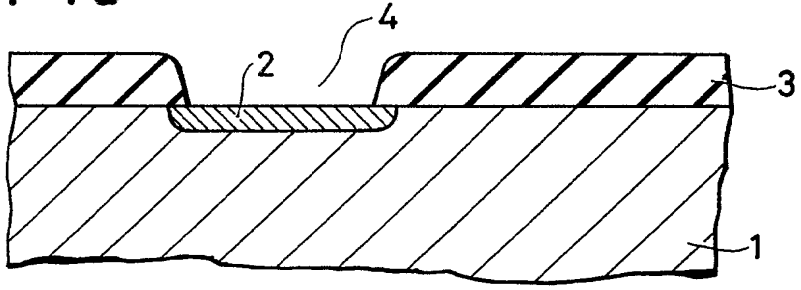


FIG. 1b

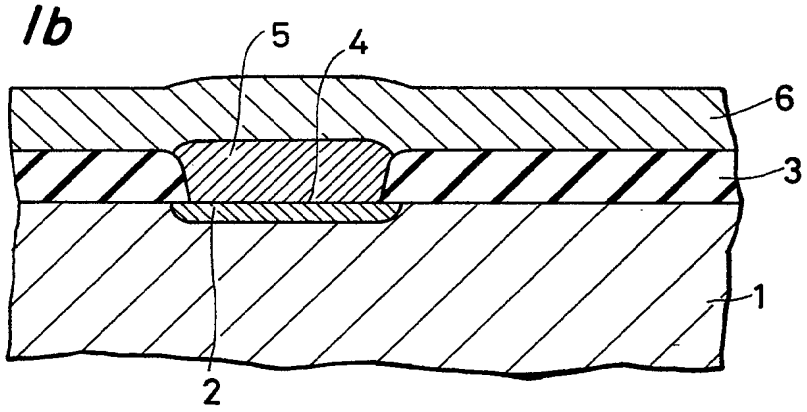


FIG. 1c

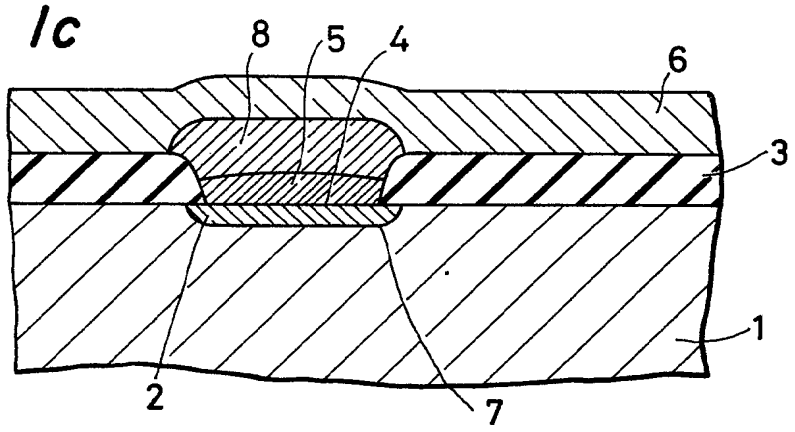
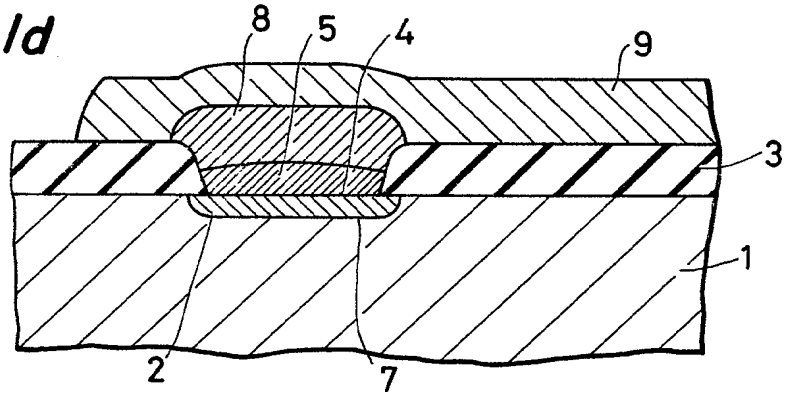


FIG. 1d



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PATENT SPECIFICATION (11) 1 222 594

DRAWINGS ATTACHED

1 222 594

(21) Application No. 53865/68 (22) Filed 13 Nov. 1968
(31) Convention Application No. 686 984 (32) Filed 30 Nov. 1967 in
(33) United States of America (US)
(45) Complete Specification published 17 Feb. 1971
(51) International Classification H 01 l 3/12
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H1K 211 217 312 353 358 413 415 41Y 422 441 459 469 490 515 523 524 52Y 530 53X 53Y 54Y 563 574 578 579 581 583 615 618 61Y 629 62Y
C7F 1V1 2Z2 4X 6D1A3

(72) Inventors WILLIAM MANOS PORTNOY and HAYDEN MARTIN LEEDY, Jr.

(54) TITANIUM-SILICON RECTIFYING JUNCTION

(71) We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to semiconductors and more particularly to metal-semiconductor rectifying junctions.

Rectifying junctions formed by intimately contacting certain metals with certain semiconductors are finding wide spread applications in devices for high frequency electronic circuits. The metals most commonly used in the electronic industry today to make metal-semiconductors rectifying junctions are molybdenum and aluminum. One such application for a metal-semiconductor rectifying junction is in a Schottky-barrier diode used as the diode in an X-band mixer circuit for microwave application. Such a mixer diode requires a low series resistance and a low forward voltage. Although molybdenum-silicon diodes are widely used for this purpose, better circuit performance could be achieved with lower series resistance and lower forward voltage than is obtainable with these diodes.

Accordingly, an object of this invention is a metal-semiconductor junction with low series resistance and low forward voltage.

According to the present invention there is provided a semiconductor device comprising titanium in contact with silicon, said contact forming a rectifying junction.

The invention may best be understood by reference to the following detailed description when read in conjunction with the accompanying drawing wherein:

FIGURE 1 is a pictorial view, partly in section, illustrating a diode using titanium to make both rectifying and ohmic contacts to a silicon substrate.

FIGURE 2 is a pictorial view, partly in section, illustrating a conventional evaporator used to deposit the titanium for the contacts shown in FIGURE 1.

FIGURE 3 is a graph, illustrating the forward current versus forward voltage of a typical titanium-silicon rectifying junction compared to a comparable molybdenum-silicon rectifying junction.

Briefly, the invention involves a titanium-silicon rectifying junction formed by the intimate contact of titanium to silicon. When titanium is placed in contact with a silicon surface, the titanium reacts with the thin layer of silicon oxide of approximately 50 Å in thickness that is always found on an otherwise clean surface of a silicon substrate. By reacting with and absorbing the oxygen from this thin layer of silicon oxide, a more intimate metal to semiconductor contact is achieved than is possible with less reactive metals, such as molybdenum, resulting in almost zero series resistance. The titanium-silicon rectifying junction has good forward and reverse characteristics, with a reverse break-down voltage of about 2 volts at 100 microamperes, and a forward voltage of about 0.2 volt at 1 milliampere as compared to the reverse break down voltage of about 10 to 15 volts at 100 microamperes and a forward voltage of about 0.5 volt at 1 milliampere for a molybdenum-silicon rectifying junction. Both the low series resistance and low forward voltage of the titanium-silicon rectifying junction are an advantage in a diode, especially when the junction is used for a mixer diode in an X-band microwave circuit.

Referring now to the FIGURES of the drawing, there is illustrated in FIGURE 1 a Shottky-barrier diode 10. Only one method of fabricating the diode 10 is described for illustrative purposes and is not meant to limit the invention in any way.

[*Price 25p*]

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The N++ type regions 1 and the N type region 2 in the N+ type silicon substrate 3 are formed by conventional epitaxial deposition and diffusion methods.

As the first step in the formation of the diode 10, a thin layer of silicon oxide 6 is formed on the surface of the N+ type silicon substrate 3 having a resistivity of about 0.008 to 0.015 ohm-cm to a thickness of about 4,000 Å by any conventional method, such as thermal growth or pyrolytic deposition. An opening 7 is formed in the silicon oxide layer 6 by conventional photolithographic and etch methods to expose a portion of the substrate 3. The opening 7 is filled with N type silicon material 2 having a resistivity of about 0.025-3 ohm-cm, (between 1 to 2 ohm-cm being the preferred resistivity) by conventional epitaxial deposition methods. A second silicon oxide layer 8 is deposited pyrolitically on the first silicon oxide layer 6 and the N type material 2 to a thickness of about 8,000 Å followed by formation of the apertures 9 by conventional photolithographic and etch methods in both silicon oxide layers 6 and 8 to expose portions of the substrate 3. By using conventional diffusion methods, an N type impurity is diffused into the portion of the substrate surface exposed by the apertures 9 to form the N++ type regions 1 having resistivities of less than about 0.005 ohm-cm. By conventional photolithographic and etch methods, the apertures 9 are reopened to remove the layer of oxide formed during the diffusion operation and the opening 11 is formed to expose the region 2.

During the fabrication of all silicon devices there is formed a thin layer of silicon oxide of approximately 50 Å on the surface of the silicon. This layer of silicon oxide is impossible to prevent whenever a silicon surface is exposed to an air ambient, even at room temperature. The necessary precautions of excluding air during the subsequent steps of device fabrication until the contacts are formed is practiced only in the formation of laboratory devices. Such precautions are not practical and are not followed during the fabrication of commercial devices. Therefore, there exists a thin layer of silicon oxide between any metal contact and a silicon surface of any commercial silicon device. Silicon oxide, being an electrical insulator, forms a layer having electrical resistance between the metal contact and the silicon substrate. Titanium, however, on contact with an oxide surface, has the characteristic of absorbing oxygen from the oxide so that when a layer of titanium is applied on the surface of a silicon substrate with an intermediate layer of silicon oxide, the titanium reacts with the oxygen of the silicon oxide to form titanium oxide. In turn, titanium oxide breaks down with the oxygen diffusing into the mass of the titanium metal. Since the amount of titanium metal is so great compared to the amount of oxygen absorbed the resistivity of the titanium metal is unaffected by the absorption of the oxygen. It is possible, therefore, when using titanium as a contact material, either ohmic or rectifying, to form an almost zero series resistance contact.

To form a layer of titanium on the substrate 3 of FIGURE 1 the substrate 3 is placed on a support in a conventional evaporator 20 as shown in FIGURE 2. A charge 21 of titanium is placed inside a tungsten coil 22 that is connected to two electrical contacts 23 which are in turn connected to a power supply (not shown) located outside the evaporator. A vacuum of approximately 5×10^{-7} millimeters of mercury is pulled on the evaporator 20. The tungsten coil 22 is heated by the outside power source until the titanium charge 21 reaches a temperature of approximately 2400°C, at which temperature the titanium evaporates and deposits on the silicon substrate 3. During the evaporation of the titanium the silicon substrate 3 remains approximately at room temperature. The evaporation of the titanium is continued by maintaining the temperature of the charge 21 at about 2400°C for a period of time sufficient to deposit a layer of titanium on the surface of the silicon substrate 3 of sufficient thickness to have low electrical resistance. After the desired thickness of titanium is obtained the tungsten coil 21 is cooled and the evaporator is returned to atmospheric pressure to allow the titanium covered substrate 3 to be removed from the evaporator.

The titanium layer is covered with a photoresistive material, such as KMER, manufactured by Eastman Kodak Company, Rochester, New York, and patterned by exposure to a pattern of light. The unpolymerized portions of the KMER are remvoed to expose the surface of the titanium layer except the portions required to form the rectifying and ohmic contacts 5 and 4, respectively, as shown in FIGURE 1. The exposed portions of the surface of the titanium layer and the layer of KMER are subjected to a wet chemical etch, including as its constituents, water, hydrochloric acid and nitric acid, for a period of time sufficient to form the contacts 4 making ohmic connections to the N++ type regions 1 and the contact 5 making a rectifying connection to the N type region 2. Although it is not shown in FIGURE 1, a top layer of metal, such as gold or aluminum, can be formed by conventional methods on the contacts 4 and 5 to facilitate subsequent ball bonding of lead wires to the contacts. Electrical connections are made to the diode 10

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by bonding gold wires, for example, to the contacts 4 and 5 if the diode is an individual device or the contacts 4 and 5 are extended to make electrical connections to the remainder of the circuit if the diode is a component of a monolithic integrated circuit.

Although a diode was described to illustrate one typical use of the titanium-silicon rectifying junction, it is obvious that other configurations and devices can be made using the titanium-silicon rectifying junction. For example, a diode could be formed with the titanium-silicon rectifying junction on one side of a silicon substrate with the ohmic contact being made to the opposite side of the substrate. In addition, the rectifying junction of the invention can be used as one junction of a transistor.

The titanium-silicon rectifying junction has excellent forward and reverse characteristics. The reverse breakdown voltage is about 2 volts at 100 microamperes which compares favorably with a comparable molybdenum-silicon rectifying junction having a reverse breakdown voltage of about 10 to 15 volts at 100 microamperes. The forward characteristics of a titanium-silicon rectifying junction are shown in FIGURE 3 as compared to a molybdenum-silicon rectifying junction. The forward current I_f is shown as the ordinate and the forward voltage V_f is shown as the abcissa of the graph. The I_f of curve 30 resulting from test data taken on the titanium-silicon diode fabricated as shown in FIGURE 1 increases from zero to about 1 milliamphere as the V_f is increased from zero to about 0.2 volt. The I_f of curve 31 resulting from test data taken on a comparable molybdenum-silicon diode does not increase from zero to about 1 milliamphere until V_f is increased from zero to about 0.5 volt. The V_f of curve 30 at 10 milli-amperes is about 0.3 volt as compared to a V_f of curve 31 of about 0.8 volt at 10 milliamperes. The improved forward characteristic of the titanium-silicon diode represented by the curve 30 as compared to the molybdenum-silicon diode as represented by the curve 31 is clearly shown by comparing their respective junction resistances, or the slopes of the curves. The junction resistance R_j of the curve 30 at about 10 milliamperes is from 4 to about 6 ohms. The junction resistance R_j of the curve 31 at about 10 milliamperes is about 7 to about 10 ohms. The reason for the difference in the series resistance of the titanium-silicon diode versus the molybdenum-silicon diode is not clearly understood. It is believed, however, to be somewhat related to the work factor of titanium, molybdenum and silicon, the work factor being defined as the energy required to move an electron from the Fermi level of a material.

The combination of low series resistance, resulting from the removal of the silicon oxide layer formed at the titanium-silicon interface and low forward voltage results in a rectifying junction that is ideal for a mixer diode to be used at microwave frequencies as well as for a general purpose diode.

WHAT WE CLAIM IS:—

1. A semiconductor device, comprising: titanium in contact with silicon, said contact forming a rectifying junction.

2. A semiconductor device, comprising: a layer of titanium in physical and electrical contact with the surface of a silicon substrate, said contact forming a rectifying junction between said layer of titanium and said surface of said silicon substrate.

3. A device as defined in Claim 2, including an N type region extending into said silicon substrate from a portion of said surface of said silicon substrate beneath said layer of titanium, said N type region having a resistivity from about 0.025 to 3 ohm-cm.

4. A device as defined in Claim 2 or 3, including one electrical connection to said layer of titanium and another electrical connection to said silicon substrate.

5. A Schottky-barrier diode, comprising:
(a) a silicon substrate,
(b) a layer of titanium on one surface of said silicon substrate, said layer of titanium and said silicon substrate forming a rectifying junction therebetween, and
(c) one ohmic contact to said silicon substrate and another ohmic connection to said layer of titanium.

6. A diode as defined in Claim 5, including an N type region having a resistivity from about 0.025 to 3 ohm-cm extending into said silicon substrate beneath a portion of said layer of titanium and an N++ type region having a resistivity of less than about 0.005 ohm-cm extending into said silicon substrate beneath a portion of said one ohmic contact.

7. A diode as defined in Claim 5 or 6, including a layer of gold or aluminum on said layer of titanium.

8. A diode as defined in Claim 6 wherein said one ohmic contact is titanium.

9. A semiconductor device substantially as herein described with reference to Figure 1 of the accompanying drawings.

ABEL & IMRAY,
Chartered Patent Agents,
Northumberland House,
303—306 High Holborn,
London, WC1V 7LH

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1222594 COMPLETE SPECIFICATION
1 SHEET *This drawing is a reproduction of the Original on a reduced scale*

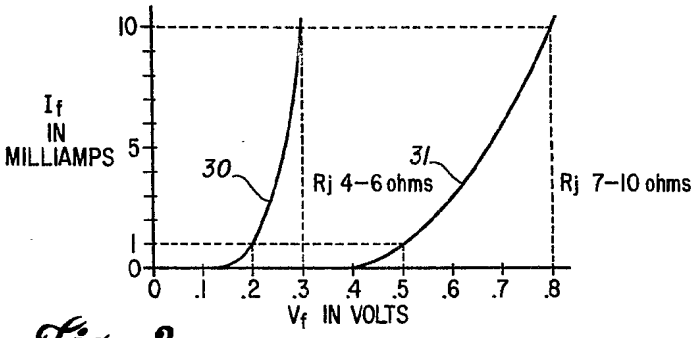


Fig. 3

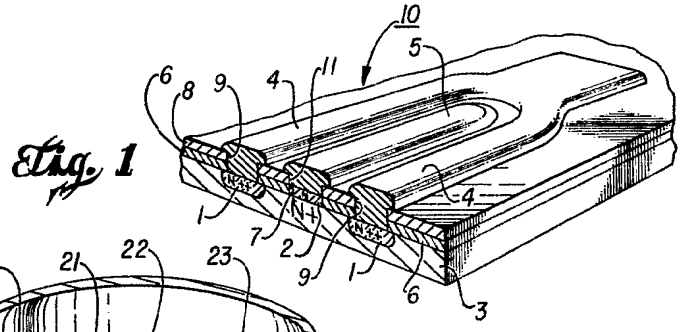


Fig. 1

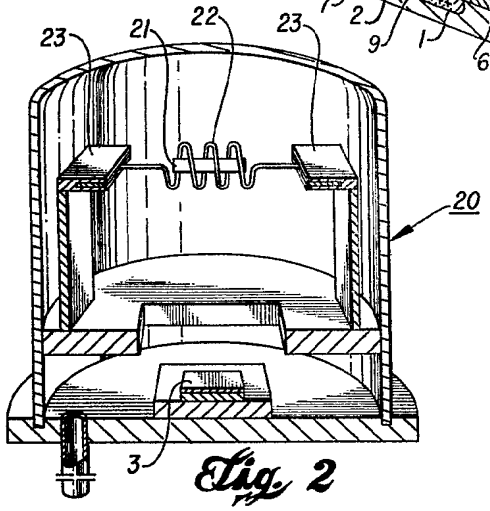


Fig. 2

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特開2002－217425
（P2002－217425A）
(43)公開日　平成14年８月２日(2002.8.2)

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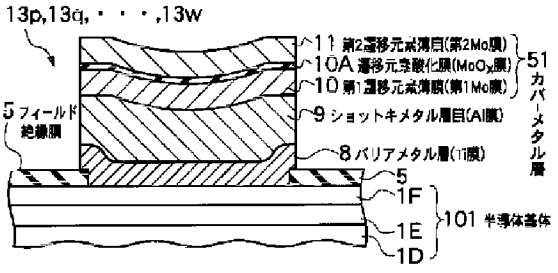
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(71)出願人　000106276
サンケン電気株式会社
埼玉県新座市北野３丁目６番３号
(72)発明者　後藤　博一
埼玉県新座市北野３丁目６番３号　サンケン電気株式会社内
(74)代理人　100083806
弁理士　三好　秀和　（外８名）

最終頁に続く

(54)【発明の名称】　半導体装置用電極、半導体装置及びその製造方法

(57)【要約】
【課題】　緩衝フッ酸溶液及びアルカリ系現像液により腐食を防止出来るゲート電極、及びこのゲート電極を有した半導体装置を提供する。
【解決手段】　半導体基体１０１の上に、順次、Ｔｉ膜８、Ａｌ膜９、第１Ｍｏ膜１０、遷移元素酸化膜（MoO_x膜）１０Ａ、第２Ｍｏ膜１１を積層してゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗを構成している。第１Ｍｏ膜１０／MoO_x膜１０Ａ／第２Ｍｏ膜１１の積層構造膜を、Ａｌ膜９上に形成することにより、ゲート電極の緩衝フッ酸溶液及びアルカリ系現像液による腐食を防止出来る。又、第１Ｍｏ膜１０／MoO_x膜１０Ａ／第２Ｍｏ膜１１の積層構造膜は、下地層のＡｌ原子が表面側へ拡散しにくく、積層構造膜の上の表面配線層等のＡｕが下地のＡｌ膜へ拡散することを有効に抑制する。



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【特許請求の範囲】
【請求項１】　半導体基体の上に形成されるバリアメタル層と、
前記バリアメタル層の上に配置されたアルミニウム（Ａ１）膜と、
該アルミニウム膜の上に配置された６Ａ族遷移元素及び該６Ａ族遷移元素の酸化膜との複合膜からなるカバーメタル層とからなることを特徴とする半導体装置用電極。
【請求項２】　前記カバーメタル層は、前記６Ａ族遷移元素からなる第１遷移元素薄膜、該第１遷移元素薄膜の上部の前記酸化膜、及び前記酸化膜の上部の第２遷移元素薄膜とから構成されていることを特徴とする請求項１記載の半導体装置用電極。
【請求項３】　前記第１遷移元素薄膜の膜厚は、１５ｎｍ～１００ｎｍであることを特徴とする請求項２に記載の半導体装置用電極。
【請求項４】　前記酸化膜の膜厚は、０．７ｎｍ～１０ｎｍであることを特徴とする請求項２又は請求項３に記載の半導体装置用電極。
【請求項５】　前記第２遷移元素薄膜の膜厚は、１５ｎｍ～１００ｎｍであることを特徴とする請求項２～４のいずれか１項記載の半導体装置用電極。
【請求項６】　前記６Ａ族の遷移元素は、モリブデン（Ｍｏ）であることを特徴とする請求項１～５のいずれか１項記載の半導体装置用電極。
【請求項７】　半導体基体と、
該半導体基体の表面に配置されたフィールド絶縁膜と、
前記半導体基体の素子主動作領域に設けられた前記フィールド絶縁膜の開口部において、前記半導体基体の上に形成されたバリアメタル層と、
前記バリアメタル層の上に配置されたアルミニウム（Ａ１）膜と、
該アルミニウム膜の上に配置された６Ａ族遷移元素及び該６Ａ族遷移元素の酸化膜との複合膜からなるカバーメタル層とからなるゲート電極を備えることを特徴とする半導体装置。
【請求項８】　前記半導体装置は前記素子主動作領域に隣接して設けられた外部回路接続領域を更に有し、
前記ゲート電極は前記外部回路接続領域に設けられた前記フィールド絶縁膜の上部にまで延長形成され、該外部回路接続領域において前記ゲート電極と同一の積層構造を有するゲートパッド下地層を構成していることを特徴とする請求項７記載の半導体装置。
【請求項９】　前記フィールド絶縁膜の上部に配置された層間絶縁膜と、
前記ゲートパッド下地層の表面に設けられた前記層間絶縁膜の開口部において、前記ゲートパッド下地層に接続される外部回路接続用金属配線層を更に有することを特徴とする請求項８記載の半導体装置。
【請求項１０】　前記カバーメタル層は、前記６Ａ族遷移元素からなる第１遷移元素薄膜、該第１遷移元素薄膜の上部の前記酸化膜、及び前記酸化膜の上部の第２遷移元素薄膜とから構成されていることを特徴とする請求項７～９のいずれか１項記載の半導体装置。
【請求項１１】　前記第１遷移元素薄膜の膜厚は、１５ｎｍ～１００ｎｍであることを特徴とする請求項１０に記載の半導体装置。
【請求項１２】　前記酸化膜の膜厚は、０．７ｎｍ～１０ｎｍであることを特徴とする請求項７～１１のいずれか１項記載の半導体装置。
【請求項１３】　前記第２遷移元素薄膜の膜厚は、１５ｎｍ～１００ｎｍであることを特徴とする請求項１０又は１１記載の半導体装置。
【請求項１４】　前記６Ａ族の遷移元素は、モリブデン（Ｍｏ）であることを特徴とする請求項７～１３のいずれか１項記載の半導体装置。
【請求項１５】　半導体基体の表面にフィールド絶縁膜を形成する工程と、
前記フィールド絶縁膜の一部を選択的に除去し、前記半導体基体が露出する開口部を形成する工程と、
前記開口部の底部に露出した半導体基体の上部及び前記フィールド絶縁膜の上部にバリアメタル層を堆積する工程と、
前記バリアメタル層の上にアルミニウム（Ａ１）膜を堆積する工程と、
前記アルミニウム膜の上に、６Ａ族遷移元素及び該６Ａ族遷移元素酸化膜との複合膜からなるカバーメタル層を形成する工程と、
前記カバーメタル層、前記アルミニウム膜及び前記バリアメタル層を選択的に除去し、前記開口部の内部に前記バリアメタル層、前記アルミニウム膜及び前記カバーメタル層とからなるゲート電極を形成する工程とを備えることを特徴とする半導体装置の製造方法。
【請求項１６】　前記カバーメタル層は、前記アルミニウム膜の上に第１モリブデン（Ｍｏ）膜を堆積した後、該第１モリブデン膜の表面を酸化処理して前記６Ａ族遷移元素酸化膜を形成し、その後前記６Ａ族遷移元素酸化膜の上に第２モリブデン膜を堆積層して形成することを特徴とする請求項１５に記載の半導体装置の製造方法。
【請求項１７】　前記カバーメタル層の上に層間絶縁膜を堆積する工程と、
該層間絶縁膜の上に第１レジストを塗布する工程と、
該第１レジストの一部を選択的に露光する工程と、
前記露光後の第１レジストを現像する工程と、
前記露光する工程及び現像する工程により形成されたエッチングマスクを用いて、前記層間絶縁膜を緩衝フッ酸溶液で、前記カバーメタル層の表面が露出するまでエッチングする工程とを更に有することを特徴とする請求項１５又は１６記載の半導体装置の製造方法。
【請求項１８】　前記第１レジストを除去する工程と、

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前記エッチングする工程液により形成された前記層間絶縁膜の開口部の底部に露出した前記カバーメタル層及び前記層間絶縁膜の上に第２レジストを塗布する工程と、該第２レジストの一部を選択的に露光する工程と、前記露光後の第２レジストをアルカリ系現像液で現像する工程とを更に有することを特徴とする請求項１７記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体装置用電極、半導体装置及びその製造方法に係り、特に、高電子移動度トランジスタ（ＨＥＭＴ）やショットキ・バリア型電界効果トランジスタ（ＭＥＳＦＥＴ）などの半導体装置に用いるショットキ・ゲート電極の新規な構造及びその製造方法に関するものである。

【０００２】

【従来の技術】ＭＥＳＦＥＴやＨＥＭＴなどの電界効果トランジスタ（ＦＥＴ）のショットキ・ゲート電極は、主にチタン（Ｔｉ）／アルミニウム（Ａｌ）積層膜で形成されている。又、ボンディングパッド形成領域を備えるＦＥＴでは、図２４及び図２５に示すようにゲート電極からボンディングパッド形成領域のフィールド絶縁膜８５の上に延長されたゲートパッド下地層（Ｔｉ／Ａｌパッド下地層）３２の表面は、酸化膜（SiO_x）や窒化膜（SiN_x）などの層間絶縁膜８１で覆われている。ゲート電極とゲートパッド下地層とは同一構造で一体で形成され、素子主動作領域においては、ゲート電極を構成するＴｉ層は、半導体基体１０３に直接接触している。ゲートパッド下地層を、外部の回路と電気的接続するためには、図２４に示すように、ゲートパッド下地層３２の上部の層間絶縁膜８１を選択的に除去し（窓部を開口し）、この窓部を用いて図２５に示すように金（Ａｕ）の薄膜をパターニングしたゲート・ボンディングパッド３４Ａを用意しておく必要がある。層間絶縁膜８１の選択的除去には、レジスト３９からなるエッチングマスクを用いる。そして、このゲート・ボンディングパッド３４Ａに、Ａｕ線等のボンディンワイヤが接続され、パッケージの外部との電気的接続が可能になる。

【０００３】これらのＦＥＴの製造では、エッチングが困難なＡｕの薄膜のパターニングには、いわゆる「リフトオフ法」が用いられている。即ち、ゲートパッド下地層３２の場合であれば、図２４で形成した層間絶縁膜８１の窓部（開口部）に対し、図２５に示すように、更にオーバーハング形状に新たなレジスト３３をパターニングし、Ａｕの薄膜（配線材料）３４を蒸着する。そして、その後レジスト３３を除去することにより、Ａｕからなるゲート・ボンディングパッド３４Ａのパターンを形成する。

【０００４】

【発明が解決しようとする課題】しかし、図２４に示すように、ゲートパッド下地層３２の上部の層間絶縁膜８１に窓明けする際に、酸化膜（SiO_x）８１のエッチング液として用いる緩衝フッ酸溶液で、下層のＴｉ／Ａｌ層３２が腐食されてしまうという問題点がある。

【０００５】又、図２５に示す断面形状の構造において、ゲート・ボンディングパッド３４Ａのパターニングにリフトオフ法を用いる場合には、リフトオフ用マスクを形成する際に、レジスト現像液がアルカリ溶液であるためレジスト現像時にゲートパッド下地層（Ｔｉ／Ａｌ層）３２が更に腐食されてしまう虞れがあった。

【０００６】このように、従来のＦＥＴでは、ゲート電極（Ｔｉ／Ａｌ）が腐食されてしまうため、この上に形成されるゲート・ボンディングパッド３４Ａとの接触が悪くなり、ゲート・ボンディングパッド３４Ａにおける接触抵抗が大きくなってしまうという問題点があった。このように接触抵抗が大きくなると、ＦＥＴの特性が悪化する。

【０００７】このような問題に対して、図２６に示すように、ゲート電極としてＴｉ膜３８／Ａｌ膜３５／Ｍｏ膜３６の積層膜からなる電極を用いることが提案されている。図２６は、素子主動作領域におけるゲート電極の構造を示し、ゲート電極の最下層のＴｉ膜３８は半導体基体１０４に直接接触している。図２６の構造も、図２４及び図２５と同様に、ゲート電極からボンディングパッド形成領域のフィールド絶縁膜８５の上に延長されたゲートパッド下地層を有する。そして、このゲートパッド下地層の表面は層間絶縁膜で覆われている。即ち、この場合もゲート電極とゲートパッド下地層とは同一構造で一体で形成されている。しかしながら、モリブデン（Ｍｏ）膜単層ではＡｌ原子の拡散防止効果が小さく、図２６に示すようにＡｌ原子がＭｏ膜３６の表面に拡散してしまうため、やはり酸化膜（SiO_x）のエッチング液やポジレジスト現像液によって腐食されてしまう。又、図２７に示すように、Ｍｏ膜３６の膜厚を厚くすればエッチング液やポジレジスト現像液による腐食は防げるが、膜厚が厚すぎると応力により、Ｍｏ膜３６の「膜剥がれ３７」が発生し易くなり、電気特性に悪影響を及ぼす虞れがある。

【０００８】本発明は上記課題を解決するためになされたものである。そこで、本発明の目的は、エッチング液やレジスト現像液により腐食されるのが有効に抑制され、所望の幾何学的形状及び電気的特性が得られる半導体装置用電極を提供することである。

【０００９】本発明の他の目的は、ゲート電極とこれに接続される配線電極との接触抵抗を小さく抑えた電気的特性の良好な半導体装置を提供することにある。

【００１０】本発明の更に他の目的は、ゲート電極がエッチング液及びレジスト現像液により腐食されるのを防止出来る半導体装置の製造方法を提供することを目的としている。

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【００１１】
【課題を解決するための手段】上記課題を解決するために、本発明の第１の特徴は、半導体基体の上に形成されるバリアメタル層、このバリアメタル層の上に配置されたＡｌ膜、このＡｌ膜の上に配置された特定の材料からなるカバーメタル層とからなる半導体装置用電極としたことを要旨とする。ここで、「特定の材料からなるカバーメタル層」とは、６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜からなるカバーメタル層という意味である。「６Ａ族遷移元素」とは、周知のようにクロム（Ｃｒ）、モリブデン（Ｍｏ）、タングステン（Ｗ）、ウラン（Ｕ）である。但し、ウラン（Ｕ）は放射性元素であるので実用的ではない。具体的には、６Ａ族の遷移元素としてはＭｏ又はＣｒが好ましい。「バリアメタル層」としてはチタン（Ｔｉ）、チタン・タングステン（ＴｉＷ）、窒化チタン（ＴｉＮ）、或いはメタルシリサイド等が使用可能である。「半導体装置用電極」とは、例えばダイオード、電界効果トランジスタ（ＦＥＴ）、静電誘導トランジスタ（ＳＩＴ）等の個別半導体素子、及びこれらからなる半導体集積回路に用いられる種々の電極を意味する。特に、ショットキダイオード、ＨＥＭＴ，ＭＥＳＦＥＴ，ＭＥＳＳＩＴ等のショットキ電極に好適である。この「ショットキ電極」には、素子主動作領域に位置する活性な制御電極だけでなく、これら活性な制御電極から延長形成された制御電極取り出し部、或いはボンディングパッド等の外部回路接続用金属配線層に接続するための下地層等が含まれる。
【００１２】本発明の第１の特徴に係る半導体装置用電極の最上層の６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜は、酸化膜（SiO_x）のウェットエッチングに用いる緩衝フッ酸（バッファフッ酸）溶液に対してエッチング耐性を有する。緩衝フッ酸溶液は、フッ酸（ＨＦ）：フッ化アンモニウム（NH_4F）＝１：１０若しくは１：７程度の組成で用いられる。このため、最上層のカバーメタル層は、絶縁膜をエッチングして電極膜を露出させる場合に、緩衝フッ酸溶液によりカバーメタル層の下地のＡｌ膜にコロージョンやアフターコロージョンなどの腐食が起こるのを防止することが出来る。
【００１３】又、６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜は、アルカリ系のレジスト現像液（以下において「アルカリ系現像液」と言う。）に対してエッチング耐性を有する。このため、リフトオフ法を用いてカバーメタル層の上にボンディングパッド等の外部回路接続用金属配線層としての配線部材を形成する場合に、アルカリ系現像液でカバーメタル層が腐食されるのを防止する作用がある。
【００１４】更に、カバーメタル層を構成する６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜は、カバーメタル層の下地のＡｌ膜からのＡｌ原子が拡散しにくいため、バリア層としての機能を果たす。６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜は、６Ａ族遷移元素のみからなる金属単層膜に比較して原子が拡散されにくく、Ａｌ膜側に向けて６Ａ族遷移元素が拡散したり、Ａｌ膜を通過して半導体基体の表面と反応することもない。このように、半導体基体の表面と６Ａ族の遷移元素とが反応することがないため、半導体装置の電気的特性や結晶学的（金属学的）特性を劣化させることがない。加えて、６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜は、その上にＡｕからなる表面配線層若しくは層間配線層を形成する場合も、Ａｕが下地のＡｌ膜や、更に半導体基体側へ拡散することを抑制する作用を有する。このため、本発明においては、半導体装置の電気的特性や結晶学的（金属学的）特性が変化してしまうことを防止することが出来る。
【００１５】具体的には、カバーメタル層は、６Ａ族遷移元素からなる第１遷移元素薄膜、この第１遷移元素薄膜の上部の６Ａ族遷移元素の酸化膜、及び６Ａ族遷移元素の酸化膜の上部の第２遷移元素薄膜とから構成することが好ましい。カバーメタル層の拡散防止作用は、６Ａ族遷移元素のみからなる金属層に比較して、第１及び第２遷移元素薄膜間に６Ａ族遷移元素の酸化膜が介在されている積層構造の方が大きいからである。又、第１及び第２遷移元素薄膜間に６Ａ族遷移元素の酸化膜が形成されることによって、実質的な６Ａ族遷移元素薄膜の膜厚を稼ぐと共に、第１遷移元素薄膜及び第２遷移元素薄膜膜間の密着性が劣化することも防止することが出来る。
【００１６】この場合、第１遷移元素薄膜の膜厚は１５ｎｍ～１００ｎｍ、６Ａ族遷移元素の酸化膜の膜厚は０．７ｎｍ～１０ｎｍ、第２遷移元素薄膜の膜厚は、１５ｎｍ～１００ｎｍ程度に設定すれば良い。このような膜厚の範囲に設定することにより、膜剥がれを抑制し、且つ拡散防止の効果を維持出来る。
【００１７】６Ａ族の遷移元素としてＭｏ及びＣｒが好ましいことは、前述したが、この内特にＭｏが好ましい。６Ａ族遷移元素がＭｏの場合は、６Ａ族遷移元素の酸化膜は、MoO_2やMoO_3等のモリブデン酸化膜（MoO_x）となる。Ｍｏ及びMoO_xの複合膜（Ｍｏ積層構造膜）は、緩衝フッ酸溶液に対して高いエッチング耐性を有する。このため、カバーメタル層としてのＭｏ積層構造膜は、絶縁膜をエッチングして電極膜を露出させる場合に、緩衝フッ酸溶液によりＭｏ積層構造膜の下地のＡｌ膜にコロージョンやアフターコロージョンなどの腐食が起こるのを防止出来る。特に、Ｍｏ積層構造膜は、アルカリ系現像液に対してエッチング耐性を有し、且つ下地層のＡｌ原子が拡散しにくいため、Ａｌの拡散バリア層として有効に機能する。更に、Ｍｏ積層構造膜は、その上にＡｕからなる表面配線層等を形成する場合も、Ａｕが下地のＡｌ膜や半導体基体側へ拡散することを有効に抑制する。

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【００１８】本発明の第２の特徴は、半導体基体、この半導体基体の表面に配置されたフィールド絶縁膜、フィールド絶縁膜の開口部において半導体基体の上に形成されたバリアメタル層、バリアメタル層の上に配置されたＡｌ膜、このＡｌ膜の上に配置されたカバーメタル層とからなるゲート電極を備える半導体装置としたことを要旨とする。バリアメタル層の配置される「フィールド絶縁膜の開口部」は、半導体基体の素子主動作領域の一部若しくは全部に設けられている。「素子主動作領域」とは、平面パターン上、いわゆる「活性領域」若しくは「デバイス領域」と呼ばれる半導体能動素子の主電流が制御される領域である。例えば、この「素子主動作領域」にはＦＥＴのソース領域及びドレイン領域が配置され、ソース領域とドレイン領域の間を流れる主電流が、制御電極（ゲート電極）により制御される。集積回路においては、素子主動作領域の周りを素子分離領域が囲み、隣接する他の素子主動作領域との電気的な干渉を防止している。フィールド絶縁膜の開口部の端部（内周部）が素子主動作領域と素子分離領域との境界近傍に位置するようにしても良い。「カバーメタル層」は、第１の特徴で述べたように、６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜から構成される。この６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜の作用や機能等は、第１の特徴で述べたとおりである。「バリアメタル層」としては、第１の特徴で述べたＴｉ、ＴｉＷ、ＴｉＮ等が使用可能である。

【００１９】なお、本発明の第２の特徴において、素子主動作領域に隣接して設けられた外部回路接続領域を更に有し、ゲート電極は外部回路接続領域に設けられたフィールド絶縁膜の上部にまで延長形成され、この外部回路接続領域においてゲート電極と同一の積層構造を有するゲートパッド下地層を構成していることが好ましい。言い換えれば、本発明の第２の特徴に係る「ゲート電極」には、素子主動作領域に位置する活性な制御電極だけでなく、これら活性な制御電極から延長形成された制御電極取り出し部や外部回路接続用金属配線層に接続するための下地層等が含まれることになる。ここで、「外部回路接続領域」にはボンディングパッドを配置するための領域の他に、集積回路においては、他の素子主動作領域に接続するための層間配線層や表面配線層を配置するための領域が含まれ、素子分離領域の上部を外部回路接続領域に用いることが可能である。つまり、「ゲートパッド下地層」とは、この外部回路との接続を可能にするための比較的広い面積を有した「活性な制御電極」に金属学的に接続される同一の積層構造を有する金属層を意味することになる。

【００２０】したがって、本発明の第２の特徴において、フィールド絶縁膜の上部に配置された層間絶縁膜、及びゲートパッド下地層の表面に設けられた層間絶縁膜の開口部において、ゲートパッド下地層に接続される外部回路接続用金属配線層を更に有することが好ましい。上述の説明から分かるように、「外部回路接続用金属配線層」にはボンディングパッドの他に、集積回路における他の素子主動作領域に接続するための層間配線層や表面配線層が含まれる。

【００２１】本発明の第２の特徴に係る半導体装置のゲート電極の最上層の６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜は、緩衝フッ酸溶液に対してエッチング耐性を有する。このため、最上層のカバーメタル層は、フィールド絶縁膜の上部に配置された層間絶縁膜を、緩衝フッ酸溶液でエッチングしてゲートパッド下地層を露出させる場合に、緩衝フッ酸溶液によりカバーメタル層の下地のＡｌ膜にコロージョンやアフターコロージョンなどの腐食が起こるのを防止することが出来る。

【００２２】又、６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜は、アルカリ系現像液に対してエッチング耐性を有する。このため、リフトオフ法を用いてゲートパッド下地層の上に外部回路接続用金属配線層を形成する場合に、アルカリ系現像液でゲートパッド下地層が腐食されるのを防止する作用がある。６Ａ族遷移元素及びこの６Ａ族遷移元素の酸化膜との複合膜は、その上にＡｕからなる外部回路接続用金属配線層を形成する場合も、Ａｕがゲートパッド下地層を構成するＡｌ膜へ拡散することを抑制する作用を有する。このため、本発明においては、半導体装置の電気的特性や結晶学的（金属学的）特性が変化してしまうことを防止することが出来る。

【００２３】本発明の第３の特徴は、（イ）半導体基体の表面にフィールド絶縁膜を形成する工程、（ロ）このフィールド絶縁膜の一部を選択的に除去し、半導体基体が露出する開口部を形成する工程、（ハ）開口部の底部に露出した半導体基体の上部及びフィールド絶縁膜の上部にバリアメタル層を堆積する工程、（ニ）バリアメタル層の上にＡｌ膜を堆積する工程、（ホ）Ａｌ膜の上に、６Ａ族遷移元素及びこの６Ａ族遷移元素酸化膜との複合膜からなるカバーメタル層を形成する工程、（ヘ）カバーメタル層、Ａｌ膜及びバリアメタル層を選択的に除去し、開口部の内部にバリアメタル層、Ａｌ膜及びカバーメタル層とからなるゲート電極を形成する工程とを備える半導体装置の製造方法としたことを要旨とする。（ロ）のフィールド絶縁膜の一部を選択的に除去する工程と（ハ）のバリアメタル層を堆積する工程の間に、他の電極を形成する工程等が含まれていてもかまわない。

【００２４】６Ａ族遷移元素及びこの６Ａ族遷移元素酸化膜との複合膜からなるカバーメタル層は、アルカリ系現像液及び緩衝フッ酸溶液に対してエッチング耐性を有する。したがって、本発明の第３の特徴に係る半導体装置の製造方法において、（ａ）カバーメタル層の上に層間絶縁膜を堆積する工程、（ｂ）この層間絶縁膜の上に

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レジストを塗布する工程、（ｃ）このレジストの一部を選択的に露光する工程、（ｄ）露光後のレジストを現像する工程、（ｅ）これら一連の露光する工程及び現像する工程により形成されたエッチングマスクを用いて層間絶縁膜を緩衝フッ酸溶液でカバーメタル層の表面が露出するまでエッチングする工程とを更に有するようにした場合、緩衝フッ酸溶液によりカバーメタル層がエッチングされることを防止し、更にその下のＡ１膜が腐食されるのを回避することが出来る。特に、Ａ１膜にコロージョンやアフターコロージョンなどの腐食が起こるのを、有効に防止する。

【００２５】更に、引き続き、（ｆ）第１レジストを除去する工程、（ｇ）エッチングする工程液により形成された層間絶縁膜の開口部の底部に露出したカバーメタル層及び層間絶縁膜の上に第２レジストを塗布する工程、（ｈ）この第２レジストの一部を選択的に露光する工程、（ｉ）露光後の第２レジストをアルカリ系現像液で現像する工程とを更に有するようにしても、アルカリ系現像液でカバーメタル層がエッチングされることは回避される。このため、リフトオフ法を用いてカバーメタル層の上にボンディングパッドや表面配線層等の外部回路接続用金属配線層を形成する場合に、アルカリ系現像液でカバーメタル層が腐食されるのを防止し、更にその下のＡ１膜が腐食されるのが有効に防止される。

【００２６】本発明の第３の特徴に係る半導体装置の製造方法において、カバーメタル層を形成する工程は、Ａ１膜の上に第１Ｍｏ膜を堆積した後、この第１Ｍｏ膜の表面を酸化処理して６Ａ族遷移元素酸化膜（MoO_2やMoO_3等のモリブデン酸化膜）を形成し、その後６Ａ族遷移元素酸化膜の上に第２Ｍｏ膜を堆積層して形成することが好ましい。この酸化処理は、蒸着装置の蒸着チャンバー若しくは、蒸着チャンバーにゲートバルブ等を介して接続された酸化処理用チャンバー中において、第１Ｍｏ膜の表面を酸素雰囲気中に晒すことで容易に行うことが出来る。第１Ｍｏ膜／モリブデン酸化膜／第２Ｍｏ膜からなるＭｏ積層構造膜は、下地層のＡｌが拡散しにくいため、バリア層としての機能を果たす。第１Ｍｏ膜／モリブデン酸化膜／第２Ｍｏ膜からなるＭｏ積層構造膜は、その上に例えばＡｕからなる層間配線層を形成する場合も、Ａｕ原子が下地のＡｌ膜や半導体基体に拡散することを抑制する作用を有する。又、第１Ｍｏ膜／モリブデン酸化膜／第２Ｍｏ膜からなるＭｏ積層構造膜は、各層間の密着性が劣化することを防止し、成膜効率を向上することが出来る。

【００２７】

【発明の実施の形態】次に、図面を参照して、本発明の半導体装置としてＨＥＭＴ及びＭＥＳＦＥＴを例示し説明する。即ち、本発明の第１の実施の形態において本発明の半導体装置としてＨＥＭＴの構造及びその製造方法を説明し、第２の実施の形態においては、本発明の半導体装置としてＭＥＳＦＥＴの構造及びその製造方法について説明する。但し、図面は模式的なものであり、各材料層の厚みや膜厚比率等は現実のものとは異なることに留意すべきである。したがって、具体的な厚みや寸法は以下の説明を参酌して判断すべきものである。又、図面相互間においても互いの寸法の関係や比率が異なる部分が含まれていることは勿論である。

【００２８】（第１の実施の形態）本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）２０１は、図３に示すようなショットキゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗを有している。即ち、ＨＥＭＴ２０１のショットキゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗは、図３に示すように、半導体基体１０１、この半導体基体１０１の表面に配置されたフィールド絶縁膜５、フィールド絶縁膜５の開口部において半導体基体１０１の上に形成されたバリアメタル層８、バリアメタル層８の上に配置されたＡｌ膜９、このＡｌ膜９の上に配置されたカバーメタル層５１とを少なくとも備える。なお、フィールド絶縁膜５は、図３のようにショットキゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗに隣接して配置されていなくても良い。例えば、フィールド絶縁膜５の開口部の端部（内周部）が素子主動作領域と素子分離領域との境界近傍に位置するようにして、フィールド絶縁膜５の開口部の内部に他の構造が含まれていてもかまわない。

【００２９】図３において、カバーメタル層５１は、６Ａ族遷移元素からなる第１遷移元素薄膜１０、この第１遷移元素薄膜１０の上部の６Ａ族遷移元素の酸化膜（以下において「遷移元素酸化膜」と言う。）１０Ａ、及び遷移元素酸化膜１０Ａの上部の第２遷移元素薄膜１１とから構成されている。図３に示すように、第１遷移元素薄膜１０と第２遷移元素薄膜１１と間に遷移元素酸化膜１０Ａが介在されている積層構造とすることにより、カバーメタル層５１の拡散防止作用が、６Ａ族遷移元素のみからなる金属層に比較して大きくなる。「拡散防止作用」とは、カバーメタル層５１の下地のＡｌ膜９が、カバーメタル層５１を拡散して上に抜けるのを防止する作用、及びカバーメタル層５１の上に積層された金属の元素がカバーメタル層５１を下に抜けてカバーメタル層５１の下地のＡｌ膜９に到達するのを防ぐ作用を言う。

又、図３に示すように、第１遷移元素薄膜１０及び第２遷移元素薄膜１１間に遷移元素酸化膜１０Ａが形成されることによって、実質的な６Ａ族遷移元素薄膜の膜厚を稼ぐと共に、第１遷移元素薄膜１０及び第２遷移元素薄膜１１膜間の密着性が劣化することも防止することが出来る。

【００３０】この場合、第１遷移元素薄膜１０の膜厚は１５ｎｍ～１００ｎｍ、遷移元素酸化膜１０Ａの膜厚は０．７ｎｍ～１０ｎｍ、第２遷移元素薄膜１１の膜厚は、１５ｎｍ～１００ｎｍ程度に設定すれば良い。この

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ような膜厚の範囲に設定することにより、膜剥がれを抑制し、且つ拡散防止作用（拡散バリア効果）を高く維持出来る。

【００３１】６Ａ族の遷移元素としてＭｏ及びＣｒが好ましく、特にＭｏが好ましい。６Ａ族遷移元素がＭｏの場合は、図３における遷移元素酸化膜１０Ａは、MoO_2やMoO_3等のモリブデン酸化膜（MoO_x）１０Ａとなる。Ｍｏ及びMoO_xの複合膜（Ｍｏ積層構造膜）は、緩衝フッ酸溶液に対して高いエッチング耐性を有する。このため、カバーメタル層５１としてのＭｏ積層構造膜は、絶縁膜をエッチングして電極膜を露出させる場合に、緩衝フッ酸溶液によりＭｏ積層構造膜の下地のＡｌ膜９にコロージョンやアフターコロージョンなどの腐食が起こるのを防止出来る。又、Ｍｏ積層構造膜は、アルカリ系現像液に対してエッチング耐性を有し、且つ下地層１６のＡｌ原子が拡散しにくいため、バリア層として有効に機能する。図３では、具体的に、半導体基体１０１の上に、順次、バリアメタル膜としてのＴｉ膜８、Ａｌ膜９、第１遷移元素薄膜としての第１Ｍｏ膜１０、遷移元素酸化膜としてのMoO_x膜１０Ａ、第２遷移元素薄膜としての第２Ｍｏ膜を積層している。そして、Ｔｉ膜８の膜厚を５ｎｍ程度、Ａｌ膜９の膜厚を５００ｎｍ程度、第１Ｍｏ膜１０、第２Ｍｏ膜１１のそれぞれの膜厚を１５ｎｍ～１００ｎｍ程度に設定している。又、遷移元素酸化膜１０Ａは、第１Ｍｏ膜１０の表面を短時間で酸化処理した０．７ｎｍ～１０ｎｍ程度のMoO_x（ｘ＞０）からなる極薄い膜である。１０ｎｍ程度以上のMoO_x膜１０Ａは、ゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗの抵抗の増大の問題や、第２Ｍｏ膜１１とMoO_x膜１０Ａとの密着性の問題が生じるので好ましくない。又、０．７ｎｍ以下では、Ａｌの拡散バリアとして十分機能しない。これらの点を考慮すると、MoO_x膜１０Ａの厚さは１ｎｍ～７ｎｍ程度がより好ましい。特に直接トンネル伝導が支配的になる４ｎｍ以下が好ましい。MoO_xとしては、MoO_2或いはMoO_3が好ましい。

【００３２】バリアメタル層８の配置されるフィールド絶縁膜５の開口部は、図１に示すような半導体基体１０１の素子主動作領域に設けられている。素子主動作領域とは、平面パターン上、いわゆる活性領域若しくはデバイス領域と呼ばれる半導体能動素子の主電流が制御される領域であり、図１では素子主動作領域用台状部２に配置されている。図１に示す半導体基体１０１の一方の主面側に、この素子主動作領域用台状部２と共に、素子主動作領域用台状部２の一方に位置する２つのソースパッド用台状部３ａ，３ｂ、素子主動作領域用台状部２の他方に位置する１つのドレインパッド用台状部４とを有している。素子主動作領域用台状部２の両側の縁には、それぞれ複数の食い込み溝２Ａが、互いに対向して形成されている。食い込み溝２Ａは、入り江の形状で沿面距離を長くして、高耐圧を得るための溝であり、目的によっては省略出来る。そして、図２に示すように、この素子主動作領域にはＦＥＴの複数のソース領域６１ａ，６１ｂ，　　，６１ｄ及び複数のドレイン領域６２ｅ，６２ｆ，　　，６２ｉが配置され、互いに対向する複数のソース領域６１ａ，６１ｂ，　　，６１ｄと複数のドレイン領域６２ｅ，６２ｆ，　　，６２ｉの間を流れる主電流が、それぞれに対応した制御電極（ゲート電極）１３ｐ，１３ｑ，１３ｒ，　　，１３ｗにより制御される。

【００３３】図１に示すように、素子主動作領域用台状部２に隣接して設けられた外部回路接続領域を更に有し、ゲート電極は外部回路接続領域に設けられたフィールド絶縁膜５の上部にまで延長形成され、この外部回路接続領域においてゲート電極と同一の積層構造を有するゲートパッド下地層１６を構成している（図１２の断面図参照。）。図１では、外部回路接続領域にはゲート・ボンディングパッド１９ＧＰが配置されているが、集積回路等の場合においては、他の素子主動作領域に接続するための層間配線層や表面配線層を配置しても良い。つまり、図１に示したゲートパッド下地層１６は、種々の外部回路との接続を可能にするための比較的広い面積を有した金属層であり、活性な制御電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗに金属学的に接続され、同一の積層構造を有する。

【００３４】半導体基体１０１は、図２に示すように、例えば半絶縁性半導体基板（半絶縁性ＧａＡｓ基板）１Ａの上に、順次、厚さ３００～５００ｎｍのｎ型ＧａＡｓからなるバッファ層１Ｂ、厚さ１５～５５ｎｍのn^-型ＩｎＧａＡｓからなるチャネル層１Ｃ、厚さ２～５ｎｍのn^-型ＡｌＧａＡｓからなるスペーサ層１Ｄ、厚さ３～１５ｎｍのｎ型ＡｌＧａＡｓからなる電子供給層１Ｅ、厚さ１０～２５ｎｍのｎ型ＡｌＧａＡｓからなるショットキ層（ショットキコンタクト層）１Ｆとを積層して構成されている。n^-型チャネル層１Ｃ及びn^-型スペーサ層１Ｄは故意には不純物が添加されていない、いわゆる「アンドープ層」である。そして、ｎ型ショットキ層１Ｆの上には複数のn^+型ソース領域（n^+型オーミックコンタクト領域）６１ａ，６１ｂ，　　，６１ｄ及び複数のn^+型ドレイン領域（n^+型オーミックコンタクト領域）６２ｅ，６２ｆ，　　，６２ｉがパターニングされて配置されている。ソース領域６１ａ，６１ｂ，　　，６１ｄ及びドレイン領域６２ｅ，６２ｆ，　　，６２ｉは、それぞれ、厚さ５～１０ｎｍのn^+型ＩｎＧａＡｓ、若しくはn^+型ＧａＡｓで構成されている。n^-型ＩｎＧａＡｓからなるチャネル層１Ｃとn^-型ＡｌＧａＡｓからなるスペーサ層１Ｄとの間でヘテロ接合が形成されている。そして、電子供給層１Ｅから電子が供給されｎ型チャネル層１Ｃのn^-型スペーサ層１Ｄとの界面近傍に２次元電子ガスが形成される。

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【００３５】素子主動作領域用台状部２における複数のソース領域（オーミックコンタクト領域）６１ａ，６１ｂ，　　，６１ｄの上には図２に示すように、複数のソース電極７Ｓがそれぞれ配置されている。又、複数のドレイン領域（オーミックコンタクト領域）６２ｅ，６２ｆ，　　，６２ｉの上には、複数のドレイン電極７Ｄがそれぞれ配置されている。複数のドレイン電極７Ｄ及び複数のソース電極７Ｓは、互いに平行且つ交互に配置されている。

【００３６】又、対をなすそれぞれのソース電極７Ｓとドレイン電極７Ｄとの間のソース電極７Ｓ近傍には、それぞれゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗが形成されている。即ち、１組のソース領域６１ａ、ゲート電極１３ｐ，ドレイン領域６２ｅで第１のユニットセルを構成している。又、１組のソース領域６１ａ、ゲート電極１３ｑ，ドレイン領域６２ｆで第２のユニットセルを、１組のソース領域６１ｂ、ゲート電極１３ｒ，ドレイン領域６２ｆで第３のユニットセルを構成している。このようにユニットセルが複数個並列接続されてマルチチャネル構造のＨＥＭＴ２０１を構成している。

【００３７】又、ソースパッド用台状部３ａ，３ｂ、ドレインパッド用台状部４の上には、ソース電極７Ｓ、ドレイン電極７Ｄと同一工程で形成されたソースパッド下地層（図示省略）、ドレインパッド下地層（図示省略）が形成されている（図８には、ソースパッド下地層７ＳＰａ，７ＳＰｂ、ドレインパッド下地層７ＤＰ、ゲートパッド下地層７ＧＰが示されている。）。ソース電極７Ｓとソースパッド下地層とは、層間絶縁膜２１に形成された窓部（開口部）を介して金（Ａｕ）からなるソース配線１９Ｓで連結されている。又、ドレイン電極７Ｄとドレインパッド下地層とは、層間絶縁膜２１に形成された窓部（開口部）を介してＡｕからなるドレイン配線１９Ｄで連結されている。図示を省略したソースパッド下地層の上には、図１に示すように、Ａｕからなるソース・ボンディングパッド１９ＳＰａ，１９ＳＰｂが形成され、図示を省略したドレインパッド下地層の上には、Ａｕからなるドレイン・ボンディングパッド１９ＤＰが形成されている。ソース・ボンディングパッド１９ＳＰａ，１９ＳＰｂはソース配線１９Ｓと一体で形成され、ドレイン・ボンディングパッド１９ＤＰはドレイン配線１９Ｄと一体で形成されている。図示を省略したソースパッド下地層とドレインパッド下地層の間には、ゲートパッド下地層１６が配置され、ゲートパッド下地層１６の上には、ゲート・ボンディングパッド１９ＧＰが形成されている。そして、図２に示すように、このような構造のＨＥＭＴ２０１の層間絶縁膜２１、ソース配線１９Ｓ及びドレイン配線１９Ｄを覆うように全面にパッシベーション膜２２が形成されている。

【００３８】又、本発明の第１の実施の形態に係るＨＥＭＴ２０１では、図１に示すように、ゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗの他に、このゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗに直列に繋がった形態のゲートライン１４、１５及びゲートパッド下地層１６が形成されている。なお、ゲートライン１４は、ソース電極７Ｓの両側に位置するゲート電極１３ｐ，１３ｑ；１３ｒ，１３ｓ；　　；１３ｖ，１３ｗをドレインパッド用台状部４側で連結するように形成されている。又、比較的幅の広いゲートライン１５は、ドレイン電極７Ｄの両側に位置するゲート電極１３ｐ，１３ｑ；１３ｒ，１３ｓ；　　；１３ｖ，１３ｗをソースパッド用台状部３ａ，３ｂ側で連結するように形成されている。又、ゲートパッド下地層１６は、２つのソースパッド用台状部３ａ，３ｂの間に位置するように形成されるものであり、中央に位置するドレイン電極７Ｄの両側に位置するゲート電極１３ｐ；１３ｑ，１３ｒ；１３ｓ，１３ｔ；　　；１３ｕ，１３ｖ；１３ｗをソースパッド用台状部３ａ，３ｂ側で連結している。

【００３９】このような構成のＨＥＭＴ２０１では、図３に示すようなゲート電極１３の構造をしているので、ゲート電極１３を構成するＡｌ膜９が、上層の第１Ｍｏ膜１０、遷移元素酸化膜（MoO_x膜）１０Ａ、第２Ｍｏ膜１１の積層構造膜で保護される。したがって、以下に説明する製造工程において、アルカリ系現像液や酸化膜エッチング液などより腐食されることがなく、ゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗの特性の劣化が抑制され、高い製造歩留まりと信頼性を達成出来る。又、ゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗは、第１Ｍｏ膜１０、遷移元素酸化膜（MoO_x膜）１０Ａ、第２Ｍｏ膜１１からなる積層構造膜を採用しているので、Ａｌが拡散しにくく、逆にＭｏがＡｌ膜９を通過してショットキ層１Ｆと反応することもない。このため、半導体基体１０１と良好なショットキ特性を有する。この点からＨＥＭＴ２０１の高い変換コンダクタンスｇｍが得られ、高周波特性を向上させることが出来る。

【００４０】図４～図１５を用いて本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）２０１の製造方法について説明する。

【００４１】（１）先ず、半絶縁性ＧａＡｓ基板１Ａの上に、順次、厚さ３００～５００ｎｍのｎ型ＧａＡｓからなるバッファ層１Ｂ、厚さ１５～５５ｎｍのn^-型ＩｎＧａＡｓからなるチャネル層１Ｃ、厚さ２～５ｎｍのn^-型ＡｌＧａＡｓからなるスペーサ層１Ｄ、厚さ３～１５ｎｍのｎ型ＡｌＧａＡｓからなる電子供給層１Ｅ、厚さ１０～２５ｎｍのｎ型ＡｌＧａＡｓからなるショットキ層１Ｆ、厚さ５～１０ｎｍのn^+型ＩｎＧａＡｓからなるオーミックコンタクト層１Ｇを連続的にエピタキシャル成長し、半導体基体１０１を得る。例えば、減圧有機金属気相成長（ＭＯＣＶＤ）装置のサセプタに、厚

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さ２５０μｍ～４５０μｍ程度の厚さの半絶縁性ＧａＡｓ基板１Ａを搭載し、このＧａＡｓ基板上に、順次、バッファ層１Ｂ、チャネル層１Ｃ、スペーサ層１Ｄ、電子供給層１Ｅ、ショットキ層１Ｆ、オーミックコンタクト層１Ｇを連続的に気相エピタキシャル成長する。具体的には、例えば、圧力５０Ｐａ～２００Ｐａにおいて、基板温度５５０℃～７００℃で、ＴＥＧ（トリエチルガリウム）とAsH_3（アルシン）を導入しｎ型ＧａＡｓからなるバッファ層１Ｂを成長する。更に、ＴＭＩｎ（トリメチルインジウム）の導入を加えn^-型ＩｎＧａＡｓからなるチャネル層１Ｃを成長する。そして、ＴＭＩｎの導入を止め、代わりにＴＭＡ（トリメチルアルミニウム）を導入して、n^-型ＡｌＧａＡｓからなるスペーサ層１Ｄ、ｎ型ＡｌＧａＡｓからなるｎ型電子供給層１Ｅ及びｎ型ＡｌＧａＡｓからなるｎ型ショットキ層１Ｆを成長する。更に、ＴＭＡの導入を止め代わりにＴＭＩｎを導入してn^+型ＩｎＧａＡｓからなるオーミックコンタクト層１Ｇを成長する。ｎ型電子供給層１Ｅ、ｎ型ショットキ層１Ｆ及びn^+型ＩｎＧａＡｓからなるオーミックコンタクト層１Ｇの成長に際しては、ｎ型のドーパントガスとしてはSiH_4（モノシラン）、Si_2H_6（ジシラン）、或いはＤＥＳｅ（ジエチルセレン）、ＤＥＴｅ（ジエチルテルル）等を用いれば良い。連続的な気相エピタキシャル成長が終了したら、減圧ＭＯＣＶＤ装置から半導体基体１０１を取り出す。なお、ＭＯＣＶＤ法以外に、分子線エピタキシ（ＭＢＥ）法、化学ビームエピタキシ（ＣＢＥ）法、分子層エピタキシ（ＭＬＥ）法等によって連続的にエピタキシャル成長しても良い。

【００４２】（２）減圧ＭＯＣＶＤ装置から取り出された半導体基体１０１の全面にレジスト（図示省略）を塗布し、フォトリソグラフィー技術により露光・現像を行ってレジストのパターニングを行い、メサエッチング用マスクを形成する。このメサエッチング用マスクを用い、図４及び図５に示すように、半導体基体１０１の一方の主面側に、両側縁に複数の食い込み溝２Ａが形成された素子主動作領域用台状部２、素子主動作領域用台状部２の一方に位置する接続パッド形成領域としての２つのソースパッド用台状部３ａ，３ｂ、素子主動作領域用台状部２の他方に位置する接続パッド形成領域としての１つのドレインパッド用台状部４とをメサエッチング工程により形成する。

【００４３】（３）次に、全面にレジスト（図示省略）を塗布し、フォトリソグラフィー技術により露光・現像を行ってレジストのパターニングを行い、リセスエッチング用マスクを形成する。このリセスエッチング用マスクを用い、反応性イオンエッチング（ＲＩＥ）により、ソース／ドレイン領域として必要な場所のみにオーミックコンタクト層１Ｇを残留させ、これ以外の部分のオーミックコンタクト層１Ｇを選択的に除去する。これにより複数のソース領域（オーミックコンタクト領域）６１ａ，６１ｂ，　　，６１ｄ及び複数のドレイン領域（オーミックコンタクト領域）６２ｅ，６２ｆ，　　，６２ｉが形成される。ＲＩＥは、ショットキ層１Ｆが露出するまで行い、ゲート電極形成予定部分に凹部（リセス）を形成する。このリセスエッチング工程により、凹部に囲まれた凸部として、ソース領域６１ａ，６１ｂ，　　，６１ｄ及びドレイン領域６２ｅ，６２ｆ，　　，６２ｉが、それぞれ複数個形成される。ソース領域６１ａ，６１ｂ，　　，６１ｄ及びドレイン領域６２ｅ，６２ｆ，　　，６２ｉは、平面図上では、複数のストライプ形状のパターンとして、並列に形成される。そして、リセスエッチング工程の終了後に、レジストを除去し、ＣＶＤ法等により、図６に示すように、半導体基体１０１の一方の主面側にSiO_xからなるフィールド絶縁膜５を全面に堆積させる。

【００４４】（４）次に、再び、全面に新たなレジスト（図示省略）を塗布し、フォトリソグラフィー技術により露光・現像を行ってレジストのパターニングを行い、オーミックコンタクト開口マスクを形成する。このオーミックコンタクト開口マスクを用い、ＲＩＥにより、ソース領域（オーミックコンタクト領域）６１ａ，６１ｂ，　　，６１ｄ及びドレイン領域（オーミックコンタクト領域）６２ｅ，６２ｆ，　　，６２ｉ上のフィールド絶縁膜５を選択的に除去する。この後、このオーミックコンタクト開口マスクを除去し、更に別のレジスト６を全面に塗布する（なお、ソースパッド用台状部３ａ，３ｂ及びドレインパッド用台状部４の構造を素子主動作領域と同一にする場合は、オーミックコンタクト開口マスクを残留させ、これをレジスト６とする。）。そして、フォトリソグラフィー技術によりレジストのパターニングを行い、複数のオーミックメタル部（ソース電極／ドレイン電極）、ソースパッド下地層、ドレインパッド下地層に対応した部分に開口を有するリフトオフ用マスク６を形成する。このリフトオフ用マスク６を介して、図７に示すように、全面に例えばＡｕ系の金属膜７を堆積させる。そして、レジスト（リフトオフ用マスク）６を剥離すれば、複数のソース領域（オーミックコンタクト領域）６１ａ，６１ｂ，　　，６１ｄ及びドレイン領域（オーミックコンタクト領域）６２ｅ，６２ｆ，　　，６２ｉの上方に、それぞれ対応する複数のソース電極７Ｓとドレイン電極７Ｄが残留する。同様にフィールド絶縁膜５の上に、ソースパッド下地層７ＳＰａ，７ＳＰｂ、ドレインパッド下地層７ＤＰの金属膜が残留する。こうして、図８の平面図に示すように、複数のソース電極７Ｓとドレイン電極７Ｄ、ソースパッド下地層７ＳＰａ，７ＳＰｂ、ドレインパッド下地層７ＤＰとがパターニングされる。

【００４５】（５）その後、図９に示すようにＴｉ／Ａｌ／Ｍｏ／MoO_x／Ｍｏの多層膜からなるゲート電極

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13p，13q，13r，　　，13wを形成する。このTi／Al／Mo／MoO_x／Moゲート電極13p，13q，13r，　　，13wの形成方法については、図16～図21を用いて後述する。この結果、図10の平面図に示すように、直列に繋がったTi／Al／Mo／MoO_x／Moの多層膜からなるゲート電極13p，13q，13r，　　，13w、ゲートライン14、15及びゲートパッド下地層16を形成する。なお、ゲートライン14は、ソース電極7Sの両側に位置するゲート電極13p，13q；13r，13s；　　；13v，13wを、ドレインパッド用台状部4側で、互いに連結するように形成されている。又、比較的幅の広いゲートライン15は、ドレイン電極7Dの両側に位置するゲート電極13p，13q；13r，13s；　　；13v，13wを、それぞれソースパッド用台状部3a，3b側で互いに連結するように形成されている。又、ゲートパッド下地層16は、2つのソースパッド用台状部3a，3bの間に位置するように形成されている。ゲートパッド下地層16は、中央に位置するドレイン電極7Dの両側のゲート電極13p，13q；13r，13s；　　；13v，13wを、ソースパッド用台状部3a，3b側で連結している。

【0046】（6）次に、図11に示すように、CVD法を用いて、全面にSiO_xからなる層間絶縁膜21を堆積させる。なお、図11は、図10のA－A断面に相当する断面図である。そして、層間絶縁膜21の上にレジスト17を全面に塗布し、フォトリソグラフィー技術を用いて、露光・現像を行って、図12に示すようなコンタクトホール開口マスク17を形成する。コンタクトホール開口マスク17は、ソース電極7S、ドレイン電極7D、ソースパッド下地層7SPa，7SPb、ドレインパッド下地層7DP、及びゲートパッド下地層16の上の層間絶縁膜21を開口し、コンタクト用窓部を形成するためのレジスト17からなるマスクパターンである。

【0047】（7）次に、レジスト17からなるコンタクトホール開口マスクを用いて、酸化膜エッチング液により層間絶縁膜21をエッチングして、ドレインパッドコンタクトホール31DP、ドレイン電極コンタクトホール31D、ゲートパッドコンタクトホール31GPを開口する。酸化膜エッチング液は、HF：NH_4F＝1：10からなる緩衝フッ酸溶液を用いる。Al膜は、緩衝フッ酸溶液でエッチングされるが、本発明では、ゲート電極13p，13q，13r，　　，13wを構成するAl膜が、上層のMo膜／モリブデン酸化膜（MoO_x）／Mo膜の積層構造膜で保護されるため、Ti／Al／Mo／MoO_x／Moゲート電極13p，13q，13r，　　，13wが緩衝フッ酸溶液より腐食されることはない。なお、図12の断面上には現れていないが、図13の平面図には、更に、ソースパッドコンタクトホール31SP、ソース電極コンタクトホール31Sが、一点鎖線で示されている。図12は、図13のB－B方向に沿った断面図であり、図12に対応して、図13にも、ドレインパッドコンタクトホール31DP、ドレイン電極コンタクトホール31D、ゲートパッドコンタクトホール31GPが一点鎖線で示されている。その後、コンタクトホール開口マスクとして用いたレジスト17を剥離する。

【0048】（8）そして、露出したTi／Al／Mo／MoO_x／Moゲート電極13p，13q，13r，　　，13wの表面及びその周辺の層間絶縁膜21を含んで、半導体基体101の表面の全面に新たなレジスト18を塗布する。そして、このレジスト18に対し、フォトリソグラフィー技術によりマスク合わせ（露光）及び現像を行ってレジスト18のパターニングを行い、リフトオフ用マスク18を形成する。このリフトオフ用マスク18のパターニングにアルカリ系現像液を用いても、このアルカリ系現像液により、Ti／Al／Mo／MoO_x／Moゲート電極13p，13q，13r，　　，13wの表面が腐食されることはない。ゲート電極13p，13q，13r，　　，13wを構成するAl膜が、上層のMo膜／モリブデン酸化膜（MoO_x）／Mo膜の積層構造膜で保護されているからである。リフトオフ用マスク18は、図13に示したソース電極コンタクトホール31S、ドレイン電極コンタクトホール31D、ソースパッドコンタクトホール31SP、ドレインパッドコンタクトホール31DP、ゲートパッドコンタクトホール31GPの寸法よりも、マスク合わせ余裕分広い面積を有したパターンである。更に、ソース電極コンタクトホール31Sとソースパッドコンタクトホール31SPとを接続するソース配線19Sのパターン、及びドレイン電極コンタクトホール31Dとドレインパッドコンタクトホール31DPとを接続するドレイン配線19Dのパターンが含まれている。ソース配線19Sのパターン及びドレイン配線19Dのパターンは、ソース電極コンタクトホール31S、ドレイン電極コンタクトホール31Dの線幅よりも、マスク合わせ余裕分広い線幅を有した、交差指（インター・ディジタル）状に噛み合った櫛形のパターンを形成する。リフトオフ工程用マスク18は、図14に示すようなオーバーハング形状を形成する。オーバーハング形状は、レジスト18の膜厚、露光条件、現像条件、ポストベーク条件、キュア条件等を制御して形成する。

【0049】（9）このリフトオフ用マスク17を介して、半導体基体101の一方の主面側に、図14に示すように、Auの蒸着を行う。レジスト17の開口内の底部とレジスト17上とに、Au膜19は分離される。そして、リフトオフ用マスクとしてのレジスト17を剥離、即ち、リフトオフを行えば、レジスト17とその上のAu膜19が除去される。この結果、図15及び図1

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に示すように、ソース電極７Ｓの上にはソース電極７Ｓとソースパッド下地層７ＳＰａ，７ＳＰｂを連結するソース配線１９Ｓが形成される。又、ドレイン電極７Ｄの上には、ドレイン電極７Ｄとドレインパッド下地層７ＤＰとを連結するドレイン配線１９Ｄが形成される。ソース配線１９Ｓ及びドレイン配線１９Ｄは、それぞれ複数本平行に配置され、互いに交差指状に噛み合った櫛形のパターンが形成する。又、図１に示すように、それぞれのパッド下地層７ＳＰａ，７ＳＰｂ、７ＤＰ、７ＧＰの上には、Ａｕからなるソース・ボンディングパッド１９ＳＰａ，１９ＳＰｂ、ドレイン・ボンディングパッド１９ＤＰ、ゲート・ボンディングパッド１９ＧＰが形成される。

【００５０】（１０）そして、図２に示すように、全面にパッシベーション膜（保護膜）２２を形成する。パッシベーション膜２２は、酸化膜（SiO_2）、ＰＳＧ膜、ＢＰＳＧ膜、窒化膜（Si_3N_4）、或いはポリイミド膜等の絶縁膜により形成すれば良い。更に、Ａｕからなるソース・ボンディングパッド１９ＳＰａ，１９ＳＰｂ、ドレイン・ボンディングパッド１９ＤＰ、ゲート・ボンディングパッド１９ＧＰの上部のパッシベーション膜２２を除去し、直径３０μｍ乃至２００μｍの金（Ａｕ）線若しくはアルミニウム（Ａｌ）線からなるボンディングワイヤが接続可能なような窓部を設ければ、本発明の半導体装置としてのＨＥＭＴ２０１が完成する。

【００５１】ここで、本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）２０１に用いるＴｉ／Ａｌ／Ｍｏ／MoO_x／Ｍｏゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗの形成方法について、図１６～図２１を用いて説明する。

【００５２】（イ）ソース電極７Ｓとドレイン電極７Ｄの形成後、先ず、全面に新たなレジスト（図示省略）を塗布する。そして、フォトリソグラフィー技術により露光・現像を行ってレジストのパターニングを行い、ゲート電極用開口開口マスクを形成する。このゲート電極用開口マスクを用い、ＲＩＥにより、ソース電極７Ｓの近傍のフィールド絶縁膜５を選択的に除去する。即ち、互いに対向するソース電極７Ｓとドレイン電極７Ｄとの間のフィールド絶縁膜５に、図１６に示すように、ゲート電極用開口５Ａを形成して、ショットキ層１Ｆの表面を露出させる（図１６は、図９の部分的な拡大図であり、図１６ではソース電極７Ｓとドレイン電極７Ｄは図示領域よりはみ出した位置に存在する。）。なお、ソース電極７Ｓとドレイン電極７Ｄ形成時に、互いに対向するソース電極７Ｓとドレイン電極７Ｄとの間のフィールド絶縁膜５を除去しておけば、この段階でのフォトリソグラフィー技術及びＲＩＥによるフィールド絶縁膜５の選択的除去の工程は不要である。

【００５３】（ロ）そして、例えばマルチソースの電子ビーム（ＥＢ）蒸着装置の蒸着チャンバーの内部の試料台に、半導体基体１０１を収納する。この蒸着チャンバーの内部には、Ｔｉ蒸着用、Ａｌ蒸着用、Ｍｏ蒸着用の各ＥＢガンが備えられている。この蒸着チャンバーを、内部の圧力が1.3×10^{-5}Ｐａ～1.2×10^{-8}Ｐａ程度の所定の蒸着圧力（バックグランド圧力）に到達するまで真空排気する。そして、先ず、図１６に示すように、全面にＴｉ膜８を膜厚が５ｎｍ程度になるように蒸着する。その後、ＥＢガンを切り替え、図１７に示すように、Ｔｉ膜８に連続してＡｌ膜９を膜厚５００ｎｍ程度になるように蒸着する。再びＥＢガンを切り替え、図１８に示すように、Ａｌ膜９の上に、６Ａ族の遷移元素からなる金属膜としての第１Ｍｏ膜１０を、膜厚が１５ｎｍ～１００ｎｍの範囲になるよう蒸着する。Ｍｏ蒸着用のＥＢガンを停止し、蒸着装置のベルジャー内にニードルバルブ等を介して、酸素（又は空気）を導入し、圧力を例えば1.3×10^{-3}Ｐａ～1.2×10^{-2}Ｐａに設定する。この酸化圧力で、５分程度放置して、図１９に示すように、第１Ｍｏ膜１０の表面に厚さ０．７ｎｍ～１０ｎｍ程度の極薄い酸化膜（モリブデン酸化膜：MoO_x）１０Ａを形成する。この際、赤外線ランプ（ＩＲ）ランプ）で、半導体基体１０１の温度を２００℃～３５０℃に制御する。その後、酸素（又は空気）の導入を止め、蒸着チャンバーの圧力が1.3×10^{-5}Ｐａ～1.2×10^{-8}Ｐａになるまで再度真空排気する。所定の蒸着圧力になれば、Ｍｏ蒸着用のＥＢガンを再び用い、遷移元素酸化膜（MoO_x膜）１０Ａの上に第２Ｍｏ膜１１を膜厚が１５ｎｍ～１００ｎｍの範囲になるよう蒸着する。このように、Ｔｉ膜８、Ａｌ膜９、第１Ｍｏ膜１０、第２Ｍｏ膜１１は、マルチソースのＥＢ蒸着装置を用いて連続的に堆積する。特に、蒸着室（蒸着チャンバー）とゲートバルブを介して接続した小型の酸化室（酸化チャンバー）を設け、この間を磁力等を利用した搬送機構で搬送可能にしたマルチチャンバー構成にすれば、第１Ｍｏ膜１０、遷移元素酸化膜（MoO_x膜）１０Ａ、第２Ｍｏ膜１１の連続形成が短時間で可能となり、生産性も向上する。この場合は、酸化時の圧力を１００ｋＰａ～１Ｐａ程度にしても良い。

【００５４】（ハ）次に、マルチソースのＥＢ蒸着装置のベルジャー内から、半導体基体１０１を取り出し、第２Ｍｏ膜１１の上にレジスト１２を全面に塗布する。フォトリソグラフィー技術により露光・現像を行って、レジストのパターニングを行い、ゲート電極形成マスクを形成する。ゲート電極形成マスクには、ゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗ、ゲートライン１４、１５及びゲートパッド１６を形成するための開口部がマスクとなるレジスト１２を加工する。その後、図２１に示すように、レジスト１２をゲート電極形成マスクとしてＲＩＥによりエッチングを行って、積層されたＴｉ膜８、Ａｌ膜９、第１Ｍｏ膜１０、モリブデン酸化膜

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（MoO_x）10A、第2Mo膜11をパターニングする。この結果、図10の平面図に示すように直列に繋がった形態のゲート電極13p，13q，13r，，13w、ゲートライン14、15及びゲートパッド下地層16を形成する。

【0055】（第2の実施の形態）本発明の半導体装置としては、第1の実施の形態で説明したHEMTに限定されるものではない。例えば、第2の実施の形態で説明するMESFETでもかまわない。

【0056】第2の実施の形態に係るMESFET202は、第1の実施の形態のHEMT201で説明した半導体基体101の内で、スペーサ層1D、電子供給層1E、ショットキ層1Fが省略された構造に相当する。即ち、図22に示すように、半絶縁性GaAs基板1Aの上に、順次、厚さ300～500nmのn型GaAsからなるバッファ層1B、厚さ200～500nmのn^-型GaAsからなる能動層（チャネル層）1K及び能動層1Kの上に配置された複数のソース領域61a，61b，，61d及び複数のドレイン領域62e，62f，，62iとから半導体基体102が構成されている。複数のソース領域61a，61b，，61d及び複数のドレイン領域62e，62f，，62iは、それぞれ厚さ5～10nmのn^+型GaAsからなるオーミックコンタクト層である。対をなすそれぞれのソース電極7Sとドレイン電極7Dとの間には、それぞれゲート電極13p，13q，13r，，13wが形成されている。互いに対向する複数のソース領域61a，61b，，61dと複数のドレイン領域62e，62f，，62iの間を流れる主電流が、それぞれに対応した制御電極（ゲート電極）13p，13q，13r，，13wにより制御される。複数のソース領域（オーミックコンタクト領域）61a，61b，，61dの上には図22に示すように、複数のソース電極7Sがそれぞれ配置されている。又、複数のドレイン領域（オーミックコンタクト領域）62e，62f，，62iの上には、複数のドレイン電極7Dがそれぞれ配置されている。複数のドレイン電極7D及び複数のソース電極7Sは、互いに平行且つ交互に配置されている。ソース電極7Sは、層間絶縁膜21の開口部を介して、その上層のソース配線19Sに、ドレイン電極7Dはその上層のドレイン配線19Dに接続されている。そして、図22に示すように、このような構造のMESFET202の層間絶縁膜21、ソース配線19S及びドレイン配線19Dを覆うように全面にパッシベーション膜22が形成されている。

【0057】第2の実施の形態に係るMESFET202の平面図は、図1に示すHEMT201と同一でかまわないので、図示を省略する。即ち、MESFET202は、図1と同様に、素子主動作領域用台状部2とこの素子主動作領域用台状部2に隣接して設けられた外部回路接続領域を更に有し、ゲート電極は外部回路接続領域に設けられたフィールド絶縁膜5の上部にまで延長形成され、この外部回路接続領域においてゲート電極と同一の積層構造を有するゲートパッド下地層16を構成している。ゲートパッド下地層16の上にはゲート・ボンディングパッド19GPが形成されている。素子主動作領域用台状部2の表面では、図1と同様に、ソース配線19Sとドレイン配線19Dとがインター・ディジタル状に形成されている。

【0058】第2の実施の形態に係る半導体装置（MESFET）202の素子主動作領域のユニットセルの構造の拡大した断面図を図23に示す。図23では、ソース領域61a、ゲート電極13q，ドレイン領域62fの1組からユニットセルを構成していることを示している。ソース領域61aは、この左側において、1組のソース領域61a、ゲート電極13p，ドレイン領域62eで他のユニットセルを構成している。又、図23では図示を省略したドレイン領域62fの右側では、1組のソース領域61b、ゲート電極13r，ドレイン領域62fで更に他のユニットセルを構成している（図22参照）。こうして、図22に示すようにユニットセルが複数個並列接続されてマルチチャネル構造のMESFET202を構成している。

【0059】図23では、MESFET20の1つのショットキゲート電極13qの構造を示す。他のゲート電極13p，13r，，13wも全く同一の断面構造であることは勿論である。即ち、ショットキゲート電極13qは、半導体基体1、この半導体基体1の表面に配置されたフィールド絶縁膜5、フィールド絶縁膜5の開口部において半導体基体1の上に形成されたバリアメタル層8、バリアメタル層8の上に配置されたA1膜9、このA1膜9の上に配置されたカバーメタル層51とを少なくとも備える。なお、図23において、ソース電極7Sとドレイン電極7Dとの間のフィールド絶縁膜5は省略可能である。例えば、フィールド絶縁膜5は、その開口部が素子主動作領域のほぼ全面を露出するように構成されていてもかまわない。つまり、フィールド絶縁膜5が素子分離領域の素子分離絶縁膜を兼ねる構造でも良い。フィールド絶縁膜5が素子分離領域の素子分離絶縁膜を兼ねる場合は、フィールド絶縁膜5の開口部の内部に複数のソース電極7S及びドレイン電極7Dが配置される。即ち、複数のソース電極7S及びドレイン電極7Dの形成時に、既に対向するソース電極7Sとドレイン極7Dとの間のフィールド絶縁膜5が除去されている構造でもかまわない。

【0060】図23において、カバーメタル層51は、第1の実施の形態と同様に6A族遷移元素からなる第1遷移元素薄膜10、この第1遷移元素薄膜10の上部の遷移元素酸化膜10A、及び遷移元素酸化膜10Aの上部の第2遷移元素薄膜11とから構成されている。第1

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の実施の形態で説明したように、第１遷移元素薄膜１０と第２遷移元素薄膜１１と間に遷移元素酸化膜１０Ａが介在されている積層構造とすることにより、カバーメタル層５１の拡散防止作用が、６Ａ族遷移元素のみからなる金属層に比較して大きくなる。第１遷移元素薄膜１０及び第２遷移元素薄膜１１間に遷移元素酸化膜１０Ａが形成されることによって、実質的な６Ａ族遷移元素薄膜の膜厚を稼ぐと共に、第１遷移元素薄膜１０及び第２遷移元素薄膜１１膜間の密着性が劣化することも防止することが出来る。

【００６１】第１の実施の形態で説明したように、第１遷移元素薄膜１０の膜厚は１５ｎｍ～１００ｎｍ、遷移元素酸化膜１０Ａの膜厚は０．７ｎｍ～１０ｎｍ、第２遷移元素薄膜１１の膜厚は、１５ｎｍ～１００ｎｍ程度に設定すれば良い。このような膜厚の範囲に設定することにより、膜剥がれを抑制し、且つ拡散防止作用（拡散バリア効果）を高く維持出来る。６Ａ族の遷移元素としてＭｏが好ましく、この場合は、図２３における遷移元素酸化膜１０Ａは、モリブデン酸化膜（MoO_x）１０Ａとなる。Ｍｏ及びMoO_xの複合膜（Ｍｏ積層構造膜）は、緩衝フッ酸溶液及びアルカリ系現像液に対してエッチング耐性を有し、且つ下地層１６のＡｌ原子が拡散しにくいため、拡散バリア層として有効に機能する。図２３では、半導体基体１の上に、順次、バリアメタル膜としてのＴｉ膜８、Ａｌ膜９、第１遷移元素薄膜としての第１Ｍｏ膜１０、遷移元素酸化膜としてのMoO_x膜１０Ａ、第２遷移元素薄膜としての第２Ｍｏ膜を積層している。

【００６２】本発明の第２の実施の形態に係るＭＥＳＦＥＴ２０２の製造方法は、基本的に図４～図１５に示したＨＥＭＴ２０１の場合と同様である。

【００６３】（１）先ず、半絶縁性ＧａＡｓ基板１Ａの上に、順次、厚さ３００～５００ｎｍのｎ型ＧａＡｓからなるバッファ層１Ｂ、厚さ２００～５００ｎｍのn^-型ＧａＡｓからなる能動層１Ｋ、厚さ５～１０ｎｍのn^+型ＧａＡｓからなるオーミックコンタクト層（図示省略）を連続的にエピタキシャル成長し、半導体基体１０２を得る。この半導体基体１０２の全面にレジスト（図示省略）を塗布し、フォトリソグラフィー技術により露光・現像を行ってレジストのパターニングを行い、メサエッチング用マスクを形成する。このメサエッチング用マスクを用い、図４及び図５に示すように、半導体基体１０２の一方の主面側に、両側縁に複数の食い込み溝２Ａが形成された素子主動作領域用台状部２、素子主動作領域用台状部２の一方に位置する接続パッド形成領域としての２つのソースパッド用台状部３ａ，３ｂ、素子主動作領域用台状部２の他方に位置する接続パッド形成領域としての１つのドレインパッド用台状部４とをメサエッチング工程により形成する。

【００６４】（２）次に、全面にレジスト（図示省略）を塗布し、フォトリソグラフィー技術により露光・現像を行ってレジストのパターニングを行い、リセスエッチング用マスクを形成する。このリセスエッチング用マスクを用い、反応性イオンエッチング（ＲＩＥ）により、ソース／ドレイン領域として必要な場所のみにオーミックコンタクト層を残留させ、これ以外の部分のオーミックコンタクト層１Ｇを選択的に除去し能動層１Ｋを露出させる。これにより複数のソース領域（オーミックコンタクト領域）６１ａ，６１ｂ，　　，６１ｄ及び複数のドレイン領域（オーミックコンタクト領域）６２ｅ，６２ｆ，　　，６２ｉが形成される。ＲＩＥは、能動層１Ｋが露出するまで行い、ゲート電極形成予定部分に凹部（リセス）を形成する。このリセスエッチング工程により、凹部に囲まれた凸部として、ソース領域６１ａ，６１ｂ，　　，６１ｄ及びドレイン領域６２ｅ，６２ｆ，　　，６２ｉが、それぞれ複数個形成される。そして、リセスエッチング工程の終了後に、レジストを除去し、ＣＶＤ法等により、図６に示すように、能動層１Ｋの表面にSiO_xからなるフィールド絶縁膜５を全面に堆積させる。

【００６５】この後の工程は、半導体基体１０２の断面構造が半導体基体１０１とは異なることを考慮すれば、第１の実施の形態に係るＨＥＭＴ２０１の製造方法と全く同一であるので、重複した記載を省略する。このような製造方法で製造したＭＥＳＦＥＴ２０２では、図２３に示すようなゲート電極１３の構造をしているので、ゲート電極１３を構成するＡｌ膜９が、上層の第１Ｍｏ膜１０、遷移元素酸化膜（MoO_x膜）１０Ａ、第２Ｍｏ膜１１の積層構造膜で保護される。したがって、製造工程の途中において、アルカリ系現像液や酸化膜エッチング液などより腐食されることがなく、ゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗの特性の劣化が抑制され、高い製造歩留まりと信頼性を達成出来る。又、ゲート電極１３ｐ，１３ｑ，１３ｒ，　　，１３ｗは、第１Ｍｏ膜１０、遷移元素酸化膜（MoO_x膜）１０Ａ、第２Ｍｏ膜１１からなる積層構造膜を採用しているので、Ａｌが拡散しにくく、逆にＭｏがＡｌ膜９を通過してショットキ層１Ｆと反応することもない。このため、半導体基体１と良好なショットキ特性を有する。このため、ＭＥＳＦＥＴ２０２の高い変換コンダクタンスｇｍが得られ、高周波特性を向上させることが出来る。

【００６６】（その他の実施の形態）上記の本発明の第１及び第２の実施の形態の開示の一部をなす論述及び図面はこの発明を限定するものであると理解すべきではない。この開示から当業者には様々な代替実施の形態、実施例及び運用技術が明らかとなろう。

【００６７】例えば、第１及び第２の実施の形態では、６Ａ族遷移元素として、Ｍｏを例示したが、Ｍｏ以外にも周知のようにＣｒ、Ｗ等が使用可能である。６Ａ族遷移元素としてＣｒを使用する場合は、カバーメタル層と

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して第１Ｃｒ膜／CrO_x／第２Ｃｒ膜から構成することが好ましい。また、第１遷移元素薄膜と第２遷移元素薄膜とを互いに異なる６Ａ族遷移元素で構成しても良い。例えば、Ｃｒ膜／MoO_x／Ｍｏ膜、Ｃｒ膜／CrO_x／Ｍｏ膜、Ｍｏ膜／MoO_x／Ｃｒ膜、Ｍｏ膜／CrO_x／Ｃｒ膜、Ｗ膜／WO_x／Ｍｏ膜、Ｗ膜／MoO_x／Ｍｏ膜等の構造でもかまわない。

【００６８】第１及び第２の実施の形態では、バリアメタル層８としてＴｉを例示したが、Ｔｉ以外に、ＴｉＷ、ＴｉＮ、或いはメタルシリサイド等が使用可能である。

【００６９】又、第１の実施の形態で説明したＨＥＭＴは種々の構造があり、第１の実施の形態に開示されたＨＥＭＴにこの発明を限定するものではない。例えば、半絶縁性ＧａＡｓ基板の上に、ｎ型ＧａＡｓからなるバッファ層を介して、厚さ３～１５ｎｍのｎ型ＡｌＧａＡｓからなる電子供給層、厚さ２～５ｎｍのn^-型ＡｌＧａＡｓからなるスペーサ層、厚さ１５～５５ｎｍのn^-型ＧａＡｓからなるチャネル層、厚さ１０～２５ｎｍのｎ型ＧａＡｓからなるショットキ層とを積層して構成した逆構造のＨＥＭＴでも良い。更にこれらを組み合わせた第１電子供給層（下層電子供給層）と第２電子供給層（上層電子供給層）とを有するＨＥＭＴでも良い。されている。半絶縁性ＧａＡｓ基板の代わりに半絶縁性ＩｎＰ基板を用いても良く、ＡｌＧａＡｓ／ＩｎＧａＡｓ、ＡｌＧａＡｓ／ＧａＡｓヘテロ接合以外のＡｌＩｎＡｓ／ＩｎＧａＡｓ、Ｓｉ／ＳｉＧｅ等のヘテロ接合を用いたＨＥＭＴでもかまわない。

【００７０】本発明の第１及び第２の実施の形態においては、素子主動作領域を図１に示すように素子主動作領域用台状部２に設け、外部回路接続領域を素子主動作領域用台状部２とは別の台状部若しくは、台状部と台状部の間の凹部底部に設けた構造を示した。しかし、半導体基体の表面を平坦としプロトン照射による素子分離領域を設け、この素子分離領域の表面を外部回路接続領域として用いても良い。又、Ｕ溝及びＵ溝に埋め込まれた素子分離絶縁膜で素子分離領域を設け、この素子分離領域の表面を外部回路接続領域として用いても良い。

【００７１】又、本発明の半導体装置としては、第１の実施の形態で説明したＨＥＭＴ、或いは第２の実施の形態で説明するＭＥＳＦＥＴに限定されるものではない。例えば、ショットキダイオード、ショットキゲート型ＳＩＴ、ショットキゲート型サイリスタ等の個別半導体素子、或いはこれらからなる半導体集積回路でも良いことは勿論である。更に、化合物半導体を基礎とした半導体装置に限定されず、Ｓｉ等の単元素半導体でもかまわない。

【００７２】更に、第１の実施の形態の説明においては、ゲート・ボンディングパッド１９ＧＰをはじめとして、ソース配線１９Ｓ、ドレイン配線１９Ｄなどをリフトオフ法にて形成したが、これに限定されるものではなく、通常のレジストパターニングとエッチング技術を用いた手法を用いても良い。

【００７３】化学量論的組成のシリコン窒化膜（Si_3N_4）は、緩衝フッ酸溶液ではエッチングされない。しかし、非化学量論的組成のシリコン窒化膜（SiN_x）、或いは酸素を含むシリコン酸化窒化膜（SiO_xN_y）の内には、緩衝フッ酸溶液でエッチングされるものがある。また、リンガラス（ＰＳＧ）等の不純物を含む酸化膜も緩衝フッ酸溶液でエッチング可能である。したがって、本発明の層間絶縁膜は酸化膜（SiO_x）のみに限定されるものではなく、緩衝フッ酸溶液でエッチング可能なすべての絶縁膜が対象となる。

【００７４】このように、本発明はここでは記載していない様々な実施の形態等を含むことは勿論である。したがって、本発明の技術的範囲は上記の説明から妥当な特許請求の範囲に係る発明特定事項によってのみ定められるものである。

【００７５】

【発明の効果】本発明によれば、電極膜の最上層のカバーメタル層が緩衝フッ酸溶液に対してエッチング耐性を有するため、絶縁膜を開口して電極膜を露出させる場合に、エッチング工程によりショットキメタル層（Ａｌ）にコロージョンやアフターコロージョンなどの腐食を防止する効果がある。

【００７６】本発明によれば、電極膜の最上層のカバーメタル層は、アルカリ系現像液に対してエッチング耐性を有するため、リフトオフ法を用いてカバーメタル層の上に接続パッドや層間配線部材を形成する場合に、アルカリ系現像液でショットキメタル層としてのＡｌ膜が腐食されるのを防止出来る。

【００７７】又、本発明によれば、カバーメタル層の構造を所定の構造に設定することにより、膜剥がれを抑制することが出来る。又、Ａｌ膜とカバーメタル層とが反応することもなく、半導体層とショットキ接合をなすゲート電極の特性を劣化させることを防止出来る。

【００７８】更に、本発明によれば、Ａｌ膜にコロージョンやアフターコロージョンなどの腐食が発生するのを防止出来る製造方法を提供することが出来る。そして、ショットキ特性の良好なゲート電極を備えた半導体装置を効率よく製造することが出来る。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）を示す平面図である。

【図２】図１のＣ－Ｃ断面図である。

【図３】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）のゲート電極の構造を示す模式的な断面図である。

【図４】本発明に係る半導体装置（ＨＥＭＴ）の製造方法の本発明の第１の実施の形態における製造工程を示す

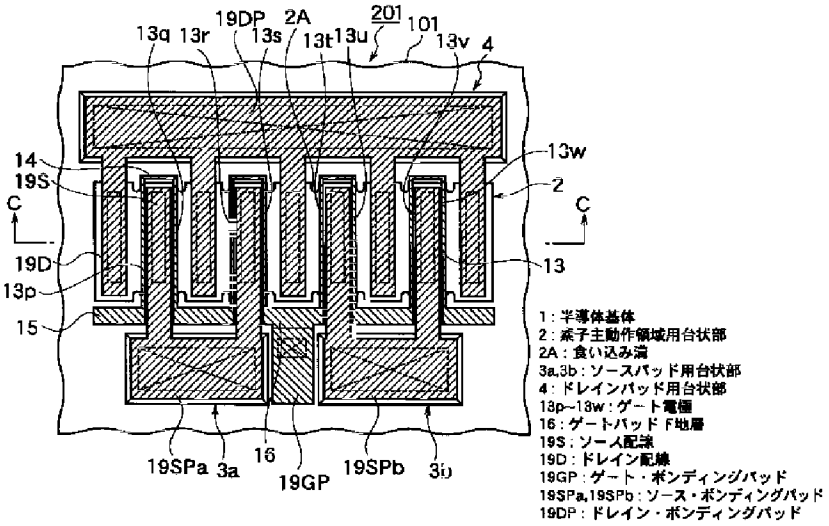
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平面図である。
【図５】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す斜視図である。
【図６】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す断面図である。
【図７】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す断面図である。
【図８】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す平面図である。
【図９】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す断面図である。
【図１０】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す平面図である。
【図１１】図１０のＡ－Ａ断面図である。
【図１２】図１３のＢ－Ｂ断面図である。
【図１３】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す平面図である。
【図１４】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す断面図である。
【図１５】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）の製造工程を示す断面図である。
【図１６】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）のゲート電極の形成工程を示す要部断面図である。
【図１７】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）のゲート電極の形成工程を示す要部断面図である。
【図１８】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）のゲート電極の形成工程を示す要部断面図である。
【図１９】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）のゲート電極の形成工程を示す要部断面図である。
【図２０】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）のゲート電極の形成工程を示す要部断面図である。
【図２１】本発明の第１の実施の形態に係る半導体装置（ＨＥＭＴ）のゲート電極の形成工程を示す要部断面図である。
【図２２】本発明の第２の実施の形態に係る半導体装置（ＭＥＳＦＥＴ）の模式的な断面図である。
【図２３】本発明の第２の実施の形態に係る半導体装置（ＭＥＳＦＥＴ）のゲート電極の構造を示す模式的な断面図である。
【図２４】従来の半導体装置のゲート電極の形成工程を示す要部断面図である。
【図２５】従来の半導体装置のゲート電極の形成工程を示す要部断面図である。
【図２６】従来の半導体装置のゲート電極のＡｌ拡散を説明する断面説明図である。
【図２７】従来の半導体装置のゲート電極における膜剥がれを示す断面説明図である。
【符号の説明】
１Ａ　半導体基板（半絶縁性ＧａＡｓ基板）
１Ｂ　バッファ層（ｎ型ＧａＡｓ）
１Ｃ　チャネル層（n^-型ＩｎＧａＡｓ）
１Ｄ　スペーサ層（n^-型ＡｌＧａＡｓ）
１Ｅ　電子供給層（ｎ型ＡｌＧａＡｓ）
１Ｆ　ショットキ層（ｎ型ＡｌＧａＡｓ）
１Ｇ　オーミックコンタクト層（n^+型ＩｎＧａＡｓ）
１Ｋ　能動層（n^-型ＧａＡｓ）
２　素子主動作領域用台状部
２Ａ　食い込み溝
３ａ，３ｂ　ソースパッド用台状部
４　ドレインパッド用台状部
５，８５　フィールド絶縁膜
６，１８，３３，３９　レジスト
７Ｓ　ソース電極
７ＳＰａ，７ＳＰｂ　ソースパッド下地層
７Ｄ　ドレイン電極
７ＤＰ　ドレインパッド下地層
８　バリアメタル層（Ｔｉ膜）
９　ショットキメタル層（Ａｌ膜）
１０　第１遷移元素薄膜（第１Ｍｏ膜）
１０Ａ　遷移元素酸化膜（MoO_x膜）
１１　第２遷移元素薄膜（第２Ｍｏ膜）
１３ｐ，１３ｑ，１３ｒ，　，１３ｗ　ゲート電極
１４、１５　ゲート配線
１６，３２　ゲートパッド下地層
１９Ｓ　ソース配線
１９ＳＰａ，１９ＳＰｂ　ソース・ボンディングパッド
１９Ｄ　ドレイン配線
１９ＤＰ　ドレイン・ボンディングパッド
１９ＧＰ，３４Ａ　ゲート・ボンディングパッド
２１，８１　層間絶縁膜
２１Ａ　開口
３１ＳＰ　ソースパッドコンタクトホール
３１Ｓ　ソース電極コンタクトホール
３１ＤＰ　ドレインパッドコンタクトホール
３１Ｄ　ドレイン電極コンタクトホール
３１ＧＰ　ゲートパッドコンタクトホール
３４　Ａｕの薄膜（配線材料）３５　Ａｌ膜
３６　Ｍｏ膜
３７　膜剥がれ
３８　Ｔｉ膜
５１　カバーメタル層
６１ａ，６１ｂ，　，６１ｄ　ソース領域
６２ｅ，６２ｆ，　，６２ｉ　ドレイン領域
１０１，１０２，１０３，１０４　半導体基体
２０１　ＨＥＭＴ

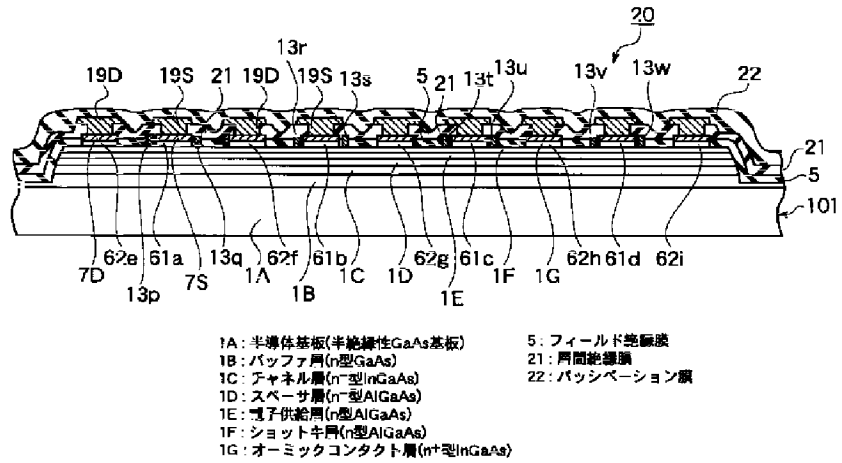
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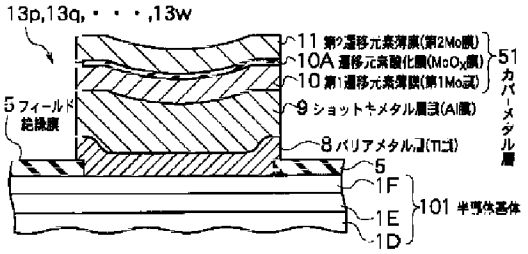
【図1】



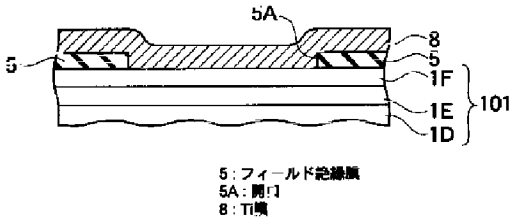
【図2】



【図3】

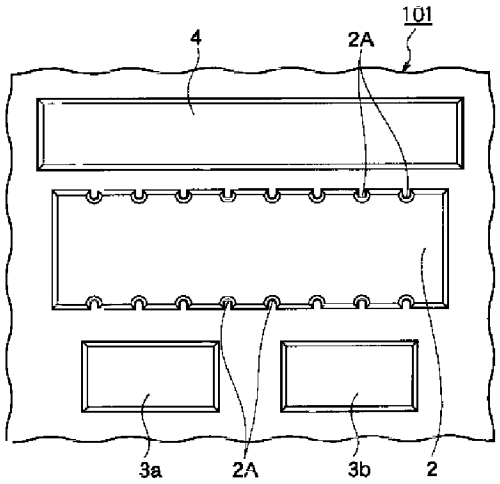


【図16】



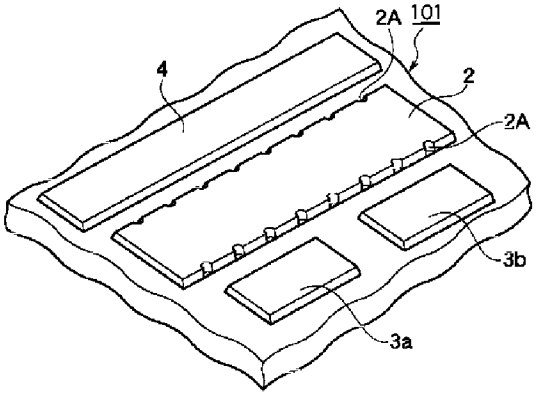
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【図4】



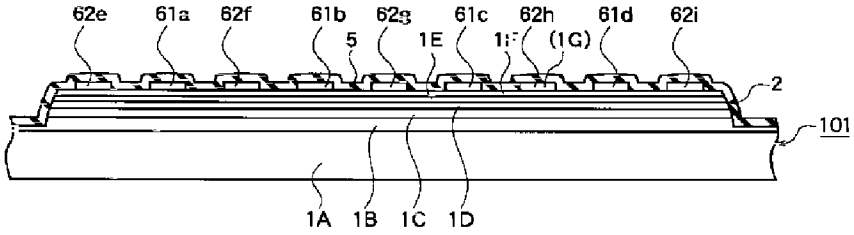
101：半導体基体
2：素子主動作領域用台状部分
3a,3b：ソースパッド用台状部分
4：ドレインパッド用台状部分

【図5】



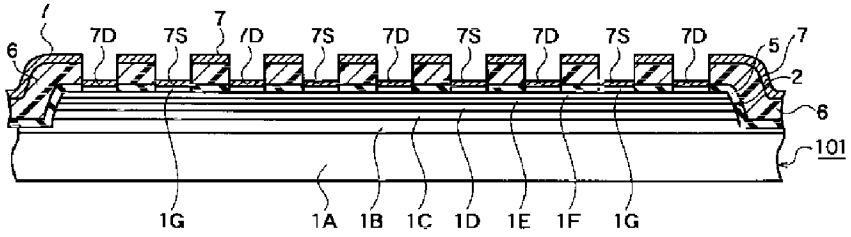
101：半導体基体
2：素子主動作領域用台状部
3a,3b：ソースパッド用台状部
4：ドレインパッド用台状部

【図6】



1A：半導体基板(半絶縁性GaAs基板)
1B：バッファ層(n型GaAs)
1C：チャネル層(n⁻型InGaAs)
1D：スペーサ層(n⁻型AlGaAs)
1E：電子供給層(n型AlGaAs)
1F：ショットキ層(n型AlGaAs)
1G：オーミックコンタクト層(n⁺型InGaAs)
2：素子主動作領域用台状部
5：フィールド絶縁膜
101：半導体基体

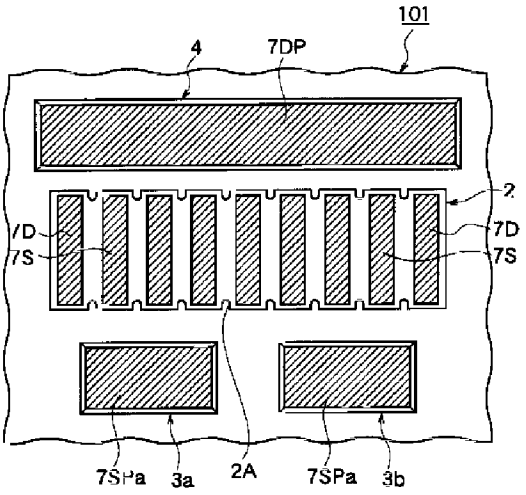
【図7】



6：レジスト
7S：ソース電極
7D：ドレイン電極

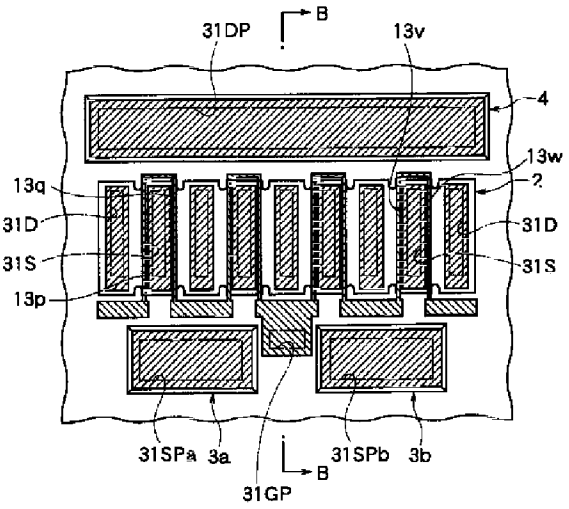
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【図8】

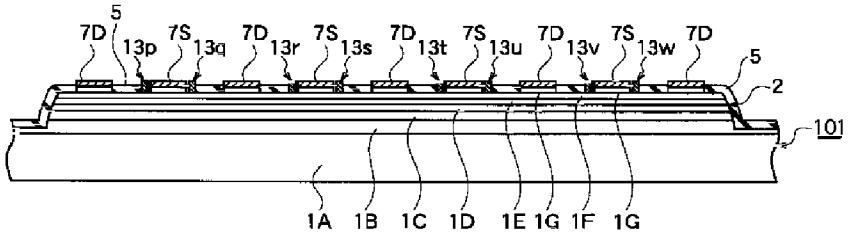


7S：ソース電極
7D：ドレイン電極
7SPa,7SPb：ソースパッド下地層
7DP：ドレインパッド下地層

【図13】

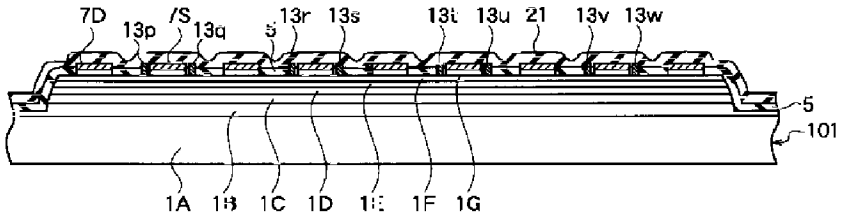


【図9】



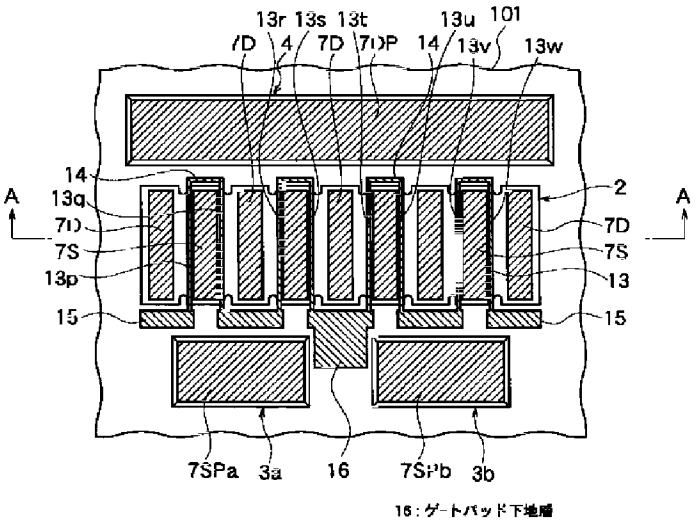
5：フィールド絶縁膜
7S：ソース電極
7D：ドレイン電極
13：ゲート電極

【図11】

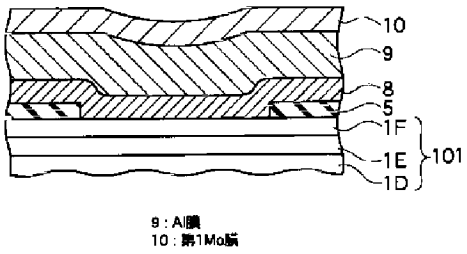


21：層間絶縁膜

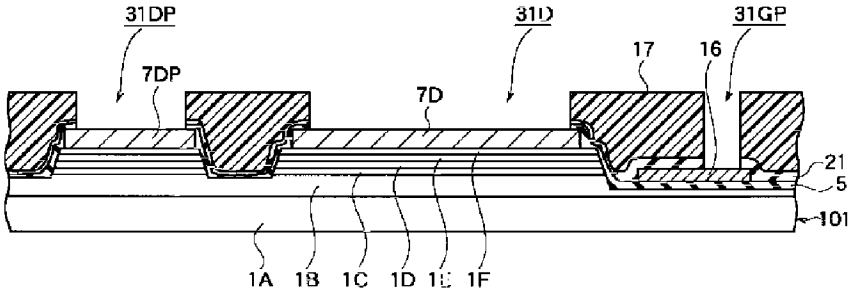
【図10】



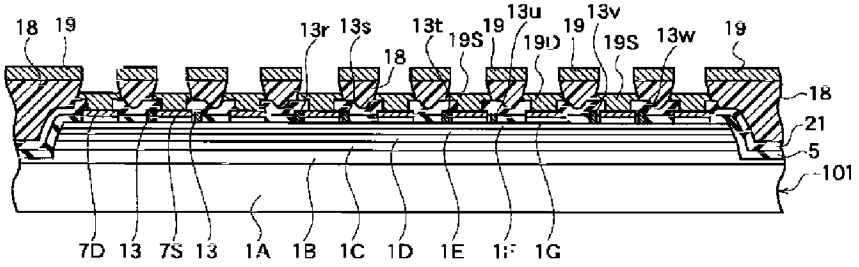
【図18】



【図12】

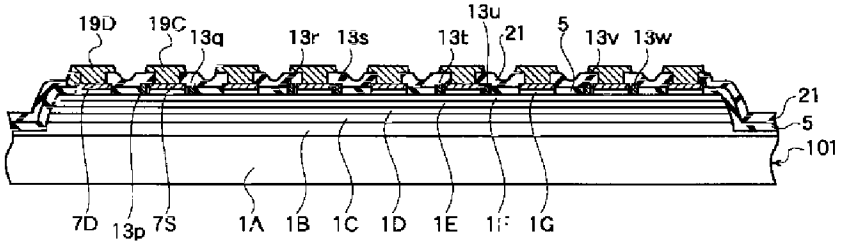


【図14】

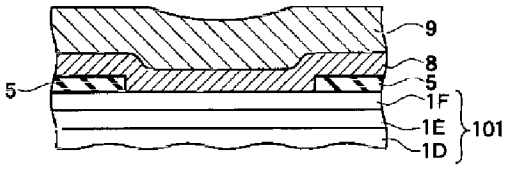


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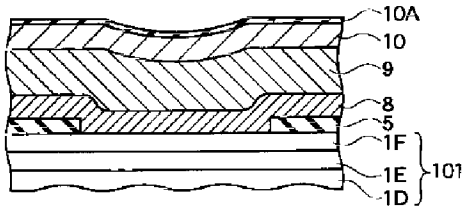
【図15】



【図17】

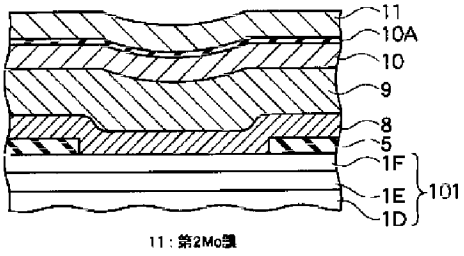


【図19】



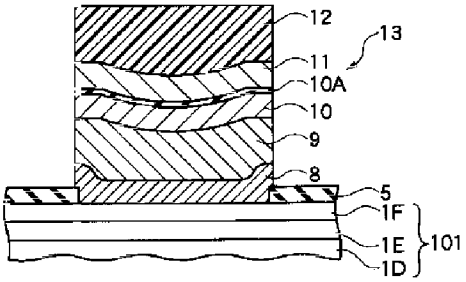
10A：Mo酸化膜(MoO_X膜)

【図20】

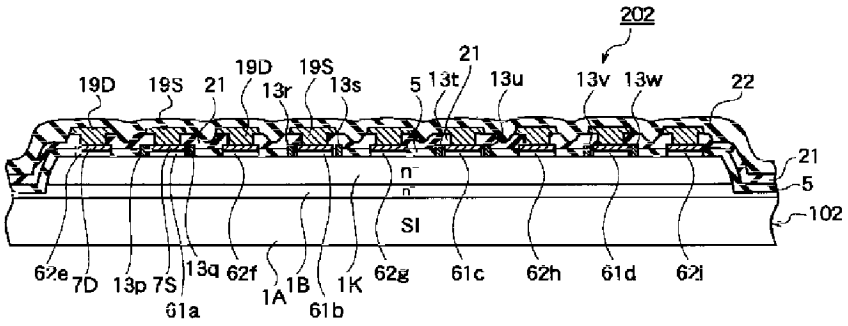


11：第2Mo膜

【図21】



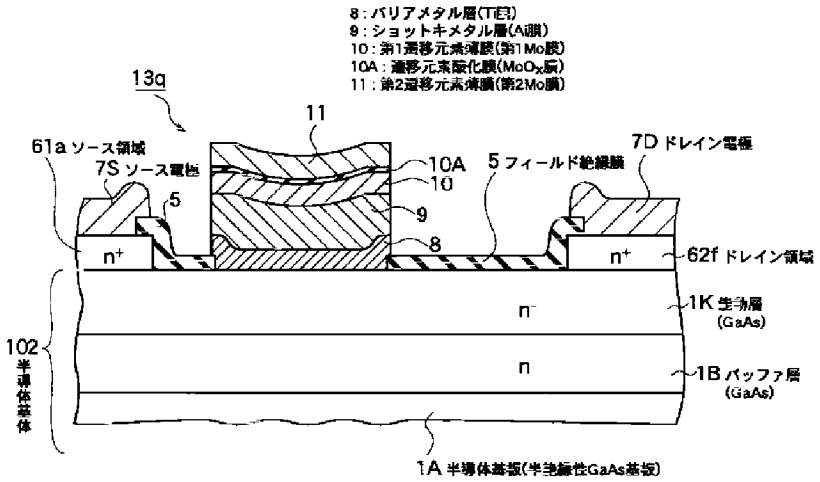
【図22】



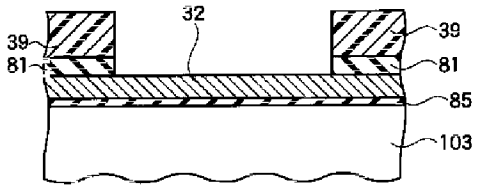
1A：半導体基板(半絶縁性GaAs基板)
1B：バッファ層(n型GaAs)
1K：能動層(n^-型GaAs)
5：フィールド絶縁膜
20：電界効果トランジスタ
21：層間絶縁膜
22：パッシベーション膜

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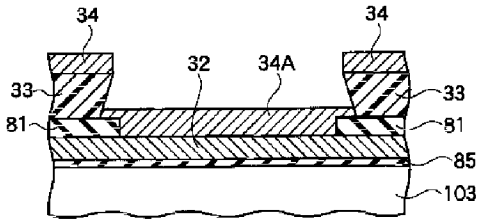
【図23】



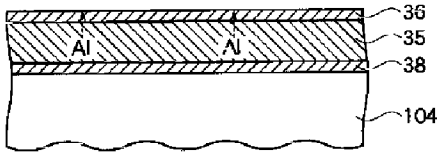
【図24】



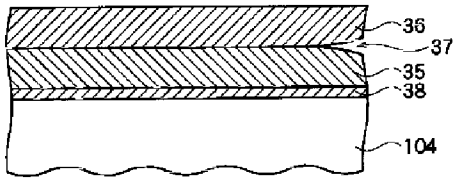
【図25】



【図26】



【図27】



フロントページの続き

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H01L 29/812			

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GM05 GM06 GM08 GN04 GN05
GQ01 GQ03 GR04 GT00 GT02
GT03 GV03 GV07 GV08 HC01
HC19

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JP2002217425A ELECTRODE FOR SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Applicants: SANKEN ELECTRIC CO LTD

Inventors: GOTO HIROICHI

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(IPC1-7): H01L21/28; H01L21/338; H01L29/74; H01L29/778; H01L29/812; H01L29/872;

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ELECTRODE FOR SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Abstract

PROBLEM TO BE SOLVED: To provide a gate electrode, that can prevent corrosion due to buffer fluoric acid solution and alkaline-based developer, and to provide a semiconductor device having the gate electrode. SOLUTION: There are successively laminated a Ti film 8, an Al film 9, a first Mo film 10, a transition element oxide film (MoOx film) 10A, and a second Mo film 11 on a semiconductor substrate 101 for composing the gate electrodes 13p, 13q, 13r,..., and 13w. The laminated structure film on the first Mo, MoOx, and second Mo films 10, 10A, and 11 is formed on the Al film 9, thus preventing corrosion, due to buffered fluoric acid solution and alkaline-based developer in the gate electrode. In the laminated structure film of the first Mo, MoOx, and second Mo films 10, 10A and 11, an Al atom in a foundation layer cannot be easily diffused to the surface side, and the diffusion of Au, such as a surface wiring layer on the lamination structure film to the Al film of foundation, is restrained effectively.

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DESCRIPTION JP2002217425

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device electrode, a semiconductor device and a manufacturing method thereof, and more particularly to a semiconductor device such as a high electron mobility transistor (HEMT) and a Schottky barrier field effect transistor (MESFET). The present invention relates to a novel structure of a Schottky gate electrode used and a method of manufacturing the same.

[0002]

2. Description of the Related Art The Schottky gate electrode of a field effect transistor (FET) such as MESFET or HEMT is mainly formed of a titanium (Ti) / aluminum (Al) laminated film. Further, in the FET having the bonding pad formation region, as shown in FIGS. 24 and 25, the gate pad underlayer (Ti / Al pad underlayer) extended from the gate electrode onto the field insulating film 85 in the bonding pad formation region. The surface of 32 is covered with an interlayer insulating film 81 such as an oxide film (SiOx) or a nitride film (SiNx). The gate electrode and the gate pad base layer are integrally formed with the same structure, and the Ti layer forming the gate electrode is in direct contact with the semiconductor substrate 103 in the element main operation region. In order to electrically connect the gate pad base layer to an external circuit, as shown in FIG. 24, the interlayer insulating film 81 on the gate pad base layer 32 is selectively removed (a window is opened). It is necessary to prepare a gate bonding pad 34A in which a thin film of gold (Au) is patterned using this window portion as shown in FIG. An etching mask made of the resist 39 is used for the selective removal of the interlayer insulating film 81. Then, a bonder wire such as an Au wire is connected to the gate bonding pad 34A to

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enable electrical connection with the outside of the package.

[0003]

In the manufacture of these FETs, the so-called "lift-off method" is used for patterning a Au thin film that is difficult to etch. That is, in the case of the gate pad base layer 32, a new resist 33 is further patterned in an overhang shape with respect to the window (opening) of the interlayer insulating film 81 formed in FIG. 24. Then, an Au thin film (wiring material) 34 is deposited. After that, the resist 33 is removed to form a pattern of the gate bonding pad 34A made of Au.

[0004]
However, as shown in FIG. 24, a buffer pad used as an etching solution for the oxide film (SiOx) 81 when a window is opened in the interlayer insulating film 81 above the gate pad base layer 32. There is a problem that the lower Ti / Al layer 32 is corroded by the acid solution.

[0005]
Further, in the structure having the cross-sectional shape shown in FIG. 25, when the lift-off method is used for patterning the gate bonding pad 34A, the resist developing solution is an alkaline solution when the lift-off mask is formed, and thus the gate is used during the resist development. The pad underlayer (Ti / Al layer) 32 may be further corroded.

[0006]

As described above, in the conventional FET, since the gate electrode (Ti / Al) is corroded, the contact with the gate bonding pad 34A formed on the gate electrode is deteriorated, and the contact resistance at the gate bonding pad 34A is reduced. There was a problem that it would grow.

When the contact resistance increases in this way, the characteristics of the FET deteriorate.

[0007]

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To solve such a problem, as shown in FIG. 26, it has been proposed to use an electrode composed of a laminated film of Ti film 38 / Al film 35 / Mo film 36 as a gate electrode.

FIG. 26 shows the structure of the gate electrode in the device main operation region, and the Ti film 38 at the lowermost layer of the gate electrode is in direct contact with the semiconductor substrate 104. The structure of FIG. 26 also has a gate pad base layer extending from the gate electrode onto the field insulating film 85 in the bonding pad formation region, similarly to FIGS. 24 and 25. The surface of this gate pad base layer is covered with an interlayer insulating film. That is, also in this case, the gate electrode and the gate pad base layer are integrally formed with the same structure. However, the molybdenum (Mo) film single layer has a small effect of preventing diffusion of Al atoms, and Al atoms diffuse to the surface of the Mo film 36 as shown in FIG. Corroded by the positive resist developer. Also, as shown in FIG. 27, if the film thickness of the Mo film 36 is increased, the corrosion due to the etching solution or the positive resist developer can be prevented, but if the film thickness is too large, the stress causes the “film peeling 37” of the Mo film 36. Is likely to occur, which may adversely affect the electrical characteristics.

[0008]

The present invention has been made to solve the above problems. Therefore, an object of the present invention is to provide an electrode for a semiconductor device in which corrosion by an etching solution or a resist developing solution is effectively suppressed and a desired geometrical shape and electric characteristics can be obtained.

[0009]
Another object of the present invention is to provide a semiconductor device having good electrical characteristics in which the contact resistance between a gate electrode and a wiring electrode connected to the gate electrode is suppressed small.

[0010]
Still another object of the present invention is to provide a method for manufacturing a semiconductor device capable of preventing the gate electrode from being corroded by an etching solution and a resist developing solution.

[0011]

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In order to solve the above problems, a first feature of the present invention is to provide a barrier metal layer formed on a semiconductor substrate and an Al film arranged on the barrier metal layer. The gist is that the semiconductor device electrode is composed of a cover metal layer made of a specific material and arranged on the Al film.

Here, the “cover metal layer made of a specific material” means a cover metal layer made of a composite film of a 6A group transition element and an oxide film of the 6A group transition element.

As is well known, the “6A group transition element” is chromium (Cr), molybdenum (Mo), tungsten (W), or uranium (U). However, uranium (U) is a radioactive element and is not practical. Specifically, Mo or Cr is preferable as the 6A group transition element. As the “barrier metal layer”, titanium (Ti), titanium / tungsten (TiW), titanium nitride (TiN), metal silicide, or the like can be used. The "electrode for semiconductor device" means, for example, a diode, a field effect transistor (FET), an individual semiconductor element such as a static induction transistor (SIT), and various electrodes used in a semiconductor integrated circuit including these. In particular, it is suitable for a Schottky electrode such as a Schottky diode, HEMT, MESFET, MESSIT. This "Schottky electrode" includes not only active control electrodes located in the main operation region of the device, but also control electrode lead-out portions formed by extension from these active control electrodes, or metal wiring layers for external circuit connection such as bonding pads. An underlayer and the like for connecting to the.

[0012]

The composite film of the 6A group transition element and the oxide film of the 6A group transition element in the uppermost layer of the electrode for a semiconductor device according to the first feature of the present invention is a buffer hydrofluoric acid used for wet etching of an oxide film (SiOx) (It has etching resistance to a buffer hydrofluoric acid) solution. The buffered hydrofluoric acid solution is used with a composition of hydrofluoric acid (HF): ammonium fluoride (NH4F) = 1: 10 or 1: 7. Therefore, when the insulating film is etched to expose the electrode film, the cover metal layer of the uppermost layer is prevented from corrosion such as corrosion and after-corrosion of the Al film underlying the cover metal layer due to the buffer hydrofluoric acid solution. It can be prevented.

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[0013]

Further, the composite film of the 6A group transition element and the oxide film of the 6A group transition element is referred to as an alkaline resist developing solution (hereinafter referred to as "alkaline developing solution").) Has etching resistance. Therefore, when forming a wiring member as a metal wiring layer for external circuit connection such as a bonding pad on the cover metal layer using the lift-off method, it is possible to prevent the cover metal layer from being corroded by the alkaline developer. There is an action.

[0014]

Further, the composite film of the 6A group transition element and the oxide film of the 6A group transition element forming the cover metal layer functions as a barrier layer because Al atoms from the underlying Al film of the cover metal layer do not easily diffuse. Fulfill. In the composite film of the 6A group transition element and the oxide film of the 6A group transition element, atoms are less likely to diffuse as compared with the metal single layer film composed of only the 6A group transition element, and the 6A group transition element is directed toward the Al film side. Does not diffuse or react with the surface of the semiconductor substrate through the Al film. In this way, since the surface of the semiconductor substrate does not react with the 6A group transition element, the electrical characteristics and crystallographic (metallurgical) characteristics of the semiconductor device are not deteriorated. In addition, the composite film of the 6A-group transition element and the oxide film of the 6A-group transition element, when the surface wiring layer or the interlayer wiring layer made of Au is formed on the composite film, Au is an underlying Al film or further It has an effect of suppressing diffusion to the semiconductor substrate side. Therefore, in the present invention, it is possible to prevent the electrical characteristics and crystallographic (metallurgical) characteristics of the semiconductor device from changing.

[0015]

Specifically, the cover metal layer includes a first transition element thin film made of a 6A group transition element, a 6A group transition element oxide film on the first transition element thin film, and a 6A group transition element oxide film on the 6A group transition element oxide film. It is preferably composed of a second transition element thin film. As for the diffusion preventing action of the cover metal layer, the laminated structure in which the oxide film of the 6A group transition element is interposed between the first and second transition element thin films is

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more effective than the metal layer made of only the 6A group transition element. Because it is big. Further, since the oxide film of the 6A group transition element is formed between the first and second transition element thin films, the film thickness of the 6A group transition element thin film is substantially increased, and the first transition element thin film and the second transition element thin film are formed. It is also possible to prevent the adhesion between the elemental thin films from deteriorating.

[0016]

In this case, the film thickness of the first transition element thin film is set to 15 nm to 100 nm, the film thickness of the 6A group transition element oxide film is set to 0.7 nm to 10 nm, and the film thickness of the second transition element thin film is set to about 15 nm to 100 nm. Good. By setting the thickness within such a range, film peeling can be suppressed and the diffusion preventing effect can be maintained.

[0017]

As described above, Mo and Cr are preferable as the 6A group transition element, but Mo is particularly preferable among them. When the 6A group transition element is Mo, the oxide film of the 6A group transition element is a molybdenum oxide film (MoOx) such as MoO2 or MoO3. The composite film of Mo and MoOx (Mo laminated structure film) has high etching resistance to the buffered hydrofluoric acid solution. Therefore, when the insulating film is etched to expose the electrode film, the Mo laminated structure film as the cover metal layer is corroded by corrosion or after-corrosion of the Al film underlying the Mo laminated structure film by the buffered hydrofluoric acid solution. Can be prevented. In particular, the Mo laminated structure film has etching resistance to an alkaline developing solution, and since Al atoms in the underlayer are difficult to diffuse, it effectively functions as an Al diffusion barrier layer. Further, the Mo laminated structure film effectively suppresses the diffusion of Au to the underlying Al film or the semiconductor substrate side even when the surface wiring layer made of Au or the like is formed thereon.

[0018]

A second feature of the present invention is to provide a semiconductor substrate, a field insulating film arranged on the surface of the semiconductor substrate, a barrier metal layer

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formed on the semiconductor substrate in the opening of the field insulating film, and a barrier metal layer on the barrier metal layer. The gist is that the semiconductor device is provided with a gate electrode composed of an Al film arranged and a cover metal layer arranged on the Al film. The "opening of the field insulating film" in which the barrier metal layer is arranged is provided in a part or all of the element main operation region of the semiconductor substrate. The "element main operation area" is an area where a main current of the semiconductor active element is so-called "active area" or "device area" is controlled on the plane pattern. For example, the source region and the drain region of the FET are arranged in this "element main operation region", and the main current flowing between the source region and the drain region is controlled by the control electrode (gate electrode). In an integrated circuit, an element isolation region surrounds the element main operation region to prevent electrical interference with another adjacent element main operation region. The end portion (inner peripheral portion) of the opening of the field insulating film may be located near the boundary between the element main operation region and the element isolation region. As described in the first feature, the "cover metal layer" is composed of a composite film of a 6A group transition element and an oxide film of this 6A group transition element. The operation and function of the 6A group transition element and the composite film of the 6A group transition element and the oxide film are as described in the first feature. As the "barrier metal layer", Ti, TiW, TiN or the like described in the first feature can be used.

[0019]

In the second aspect of the present invention, the device further has an external circuit connection region provided adjacent to the element main operation region, and the gate electrode extends to an upper portion of the field insulating film provided in the external circuit connection region. It is preferable that the formed gate pad base layer has the same laminated structure as the gate electrode in the external circuit connection region. In other words, the "gate electrode" according to the second feature of the present invention includes not only the active control electrodes located in the device main operation region, but also the control electrode lead-out portions and the external parts formed by extension from these active control electrodes. A base layer and the like for connecting to the metal wiring layer for circuit connection are included. Here, in the "external circuit connection region", in addition to the region for arranging the bonding pad, in the integrated circuit, for arranging the interlayer wiring layer and the surface wiring layer for connecting to other element main operation regions. Region is included, and the upper portion of the element isolation region can be used as the external circuit connection region. That is, the “gate pad underlayer” has the same laminated structure that is metallurgically connected to the “active control electrode” having a relatively large area for enabling connection with this external circuit. It means a metal layer.

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[0020]

Therefore, according to the second aspect of the present invention, the gate insulating layer is formed on the upper surface of the field insulating film and the opening of the interlayer insulating film formed on the surface of the gate pad underlying layer. It is preferable to further include a metal wiring layer for external circuit connection. As can be seen from the above description, the “external circuit connecting metal wiring layer” includes, in addition to the bonding pad, an interlayer wiring layer and a surface wiring layer for connecting to other element main operation regions in the integrated circuit.

[0021]

The uppermost 6A group transition element of the gate electrode of the semiconductor device according to the second aspect of the present invention and the composite film of the 6A group transition element and the oxide film have etching resistance to the buffered hydrofluoric acid solution. Therefore, the uppermost cover metal layer is a cover metal layer formed by the buffer hydrofluoric acid solution when the interlayer insulating film disposed on the field insulating film is etched with the buffer hydrofluoric acid solution to expose the gate pad base layer. It is possible to prevent corrosion such as corrosion and after-corrosion of the Al film underlying the layer.

[0022]

Further, the 6A group transition element and the composite film of the 6A group transition element and the oxide film have etching resistance to an alkaline developing solution. Therefore, when the metal wiring layer for external circuit connection is formed on the gate pad underlayer using the lift-off method, it has an effect of preventing the gate pad underlayer from being corroded by the alkaline developer. Even when a metal wiring layer for connecting an external circuit made of Au is formed on the composite film of the 6A-group transition element and the oxide film of the 6A-group transition element, Au is converted to the Al film forming the gate pad underlayer. It has the effect of suppressing diffusion. Therefore, in the present invention, it is possible to prevent the electrical characteristics and crystallographic (metallurgical) characteristics of the semiconductor device from changing.

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[0023]

A third feature of the present invention is (a) a step of forming a field insulating film on the surface of the semiconductor substrate, and (b) a part of the field insulating film is selectively removed to form an opening for exposing the semiconductor substrate. A step of forming, (c) a step of depositing a barrier metal layer on the upper part of the semiconductor substrate and the upper part of the field insulating film exposed at the bottom of the opening, (d) a step of depositing an Al film on the barrier metal layer, (E) A step of forming a cover metal layer made of a 6A group transition element and a composite film of the 6A group transition element oxide film on the Al film, (F) a cover metal layer, an Al film and a barrier metal layer are selectively formed. And a step of forming a gate electrode composed of a barrier metal layer, an Al film, and a cover metal layer inside the opening. Between the step (b) of selectively removing a part of the field insulating film and the step (c) of depositing the barrier metal layer, a step of forming another electrode may be included.

[0024]

The cover metal layer composed of a 6A group transition element and a composite film of the 6A group transition element oxide film has etching resistance to an alkaline developer and a buffered hydrofluoric acid solution. Therefore, in the method of manufacturing a semiconductor device according to the third aspect of the present invention, (a) a step of depositing an interlayer insulating film on the cover metal layer, and (b) a step of applying a resist on the interlayer insulating film. , (C) a step of selectively exposing a part of this resist, (d) a step of developing the resist after exposure, (e) an etching mask formed by the series of these exposing and developing steps And the step of etching the interlayer insulating film with a buffered hydrofluoric acid solution until the surface of the cover metal layer is exposed, the cover metal layer is prevented from being etched by the buffered hydrofluoric acid solution. Corrosion of the underlying Al film can be avoided. In particular, it effectively prevents corrosion such as corrosion and after-corrosion of the Al film.

[0025]

Further, subsequently, (f) the step of removing the first resist, (g) the step of etching, and the second resist on the cover metal layer and the interlayer insulating film exposed at the bottom of the opening of the interlayer insulating film formed by the solution. And (h) selectively exposing part of the second resist, and (i) developing the second resist after exposure with an alkaline

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developer, The etching of the cover metal layer with the alkaline developer is avoided. Therefore, when forming a metal wiring layer for external circuit connection such as a bonding pad or surface wiring layer on the cover metal layer by using the lift-off method, it is possible to prevent the cover metal layer from being corroded by the alkaline developer. In addition, the Al film thereunder is effectively prevented from being corroded.

[0026]

In the method of manufacturing a semiconductor device according to the third aspect of the present invention, in the step of forming the cover metal layer, after depositing the first Mo film on the Al film, the surface of the first Mo film is oxidized to form 6A. It is preferable to form a group transition element oxide film (a molybdenum oxide film such as MoO2 or MoO3) and then deposit a second Mo film on the group 6A transition element oxide film. This oxidation treatment can be easily performed by exposing the surface of the first Mo film to an oxygen atmosphere in the vapor deposition chamber of the vapor deposition apparatus or an oxidation treatment chamber connected to the vapor deposition chamber via a gate valve or the like. .. The Mo laminated structure film composed of the first Mo film / molybdenum oxide film / second Mo film serves as a barrier layer because Al of the underlayer is difficult to diffuse. In the Mo laminated structure film composed of the first Mo film / molybdenum oxide film / second Mo film, even when an interlayer wiring layer made of, for example, Au is formed on the Mo laminated structure film, Au atoms are prevented from diffusing into the underlying Al film or the semiconductor substrate. Has a suppressing effect. Further, the Mo laminated structure film composed of the first Mo film / molybdenum oxide film / second Mo film can prevent the adhesion between the layers from being deteriorated and improve the film forming efficiency.

[0027]

BEST MODE FOR CARRYING OUT THE INVENTION Next, HEMTs and MESFETs will be exemplified and described as semiconductor devices of the present invention with reference to the drawings. That is, the structure of the HEMT as the semiconductor device of the present invention and the manufacturing method thereof will be described in the first embodiment of the present invention, and the structure of the MESFET as the semiconductor device of the present invention and the manufacturing method thereof will be described in the second embodiment. The method will be described. However, it should be noted that the drawings are schematic and that the thicknesses and film thickness ratios of the respective material layers are different from the actual ones. Therefore, specific thicknesses and dimensions should be determined in consideration of the following description. Further, it is needless to say that the drawings include

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portions in which dimensional relationships and ratios are different from each other.

[0028]

(First Embodiment) A semiconductor device (HEMT) 201 according to the first embodiment of the present invention includes Schottky gate electrodes 13p, 13q, 13r, ..., 13w as shown in FIG. Have That is, the Schottky gate electrodes 13p, 13q, 13r, ..., 13w of the HEMT 201 have the semiconductor substrate 101, the field insulating film 5 disposed on the surface of the semiconductor substrate 101, and the field insulating film as shown in FIG. The barrier metal layer 8 formed on the semiconductor substrate 101 in the opening of the film 5, the Al film 9 arranged on the barrier metal layer 8, and the cover metal layer 51 arranged on the Al film 9 are formed. Provide at least. The field insulating film 5 may not be arranged adjacent to the Schottky gate electrodes 13p, 13q, 13r, ..., 13w as shown in FIG. For example, the end portion (inner peripheral portion) of the opening of the field insulating film 5 is located near the boundary between the element main operation region and the element isolation region, and another structure is formed inside the opening of the field insulating film 5. May be included.

[0029]

In FIG. 3, the cover metal layer 51 is a first transition element thin film 10 made of a 6A group transition element, and an oxide film of the 6A group transition element on the first transition element thin film 10 (hereinafter referred to as “transition element oxide film”). To tell.) 10A and the second transition element thin film 11 on the transition element oxide film 10A. As shown in FIG. 3, by adopting a laminated structure in which the transition element oxide film 10A is interposed between the first transition element thin film 10 and the second transition element thin film 11, the diffusion preventing action of the cover metal layer 51 is It becomes larger than that of a metal layer composed only of a 6A group transition element. The “diffusion preventing effect” is an effect of preventing the Al film 9 underlying the cover metal layer 51 from diffusing through the cover metal layer 51 and slipping upward, and a function of a metal laminated on the cover metal layer 51. This is an action of preventing an element from passing through the cover metal layer 51 downward and reaching the underlying Al film 9 of the cover metal layer 51. Further, as shown in FIG. 3, by forming the transition element oxide film 10A between the first transition element thin film 10 and the second transition element thin film 11, the substantial thickness of the 6A group transition element thin film is obtained. It is also possible to prevent the adhesion between the first transition element thin film 10 and the second transition element thin film 11 from being deteriorated.

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[0030]

In this case, the first transition element thin film 10 has a thickness of 15 nm to 100 nm, the transition element oxide film 10A has a thickness of 0.7 nm to 10 nm, and the second transition element thin film 11 has a thickness of about 15 nm to 100 nm. Good. By setting the thickness within such a range, film peeling can be suppressed and the diffusion preventing effect (diffusion barrier effect) can be maintained high.

[0031]

Mo and Cr are preferable as the 6A group transition element, and Mo is particularly preferable. When the 6A group transition element is Mo, the transition element oxide film 10A in FIG. 3 is a molybdenum oxide film (MoOx) 10A such as MoO2 or MoO3. The composite film of Mo and MoOx (Mo laminated structure film) has high etching resistance to the buffer hydrofluoric acid solution. Therefore, the Mo laminated structure film as the cover metal layer 51 may be corroded or after-corroded on the Al film 9 underlying the Mo laminated structure film by the buffered hydrofluoric acid solution when the insulating film is etched to expose the electrode film. It can prevent the corrosion of. Further, the Mo laminated structure film has etching resistance to an alkaline developing solution, and since Al atoms in the underlayer 16 are less likely to diffuse, it effectively functions as a barrier layer. In FIG. 3, specifically, on the semiconductor substrate 101, a Ti film 8 as an barrier metal film, an Al film 9, a first Mo film 10 as a first transition element thin film, and a MoOx film as a transition element oxide film are sequentially formed. 10A, a second Mo film as a second transition element thin film is laminated. The film thickness of the Ti film 8 is set to about 5 nm, the film thickness of the Al film 9 is set to about 500 nm, and the film thickness of each of the first Mo film 10 and the second Mo film 11 is set to about 15 nm to 100 nm. The transition element oxide film 10A is an extremely thin film made of MoOx (x> 0) of about 0.7 nm to 10 nm obtained by oxidizing the surface of the first Mo film 10 for a short time. The MoOx film 10A having a thickness of about 10 nm or more is preferable because it causes a problem of increase in resistance of the gate electrodes 13p, 13q, 13r, ..., 13w and a problem of adhesion between the second Mo film 11 and the MoOx film 10A. Absent. Further, if the thickness is 0.7 nm or less, it does not sufficiently function as a diffusion barrier of Al. Considering these points, the thickness of the MoOx film 10A is more preferably about 1 nm to 7 nm. In particular, it is preferably 4 nm or less where direct tunnel conduction becomes dominant. MoOx is preferably MoO2 or MoO3.

[0032]

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The opening of the field insulating film 5 in which the barrier metal layer 8 is arranged is provided in the element main operation region of the semiconductor substrate 101 as shown in FIG. The element main operation area is an area where a main current of a semiconductor active element, which is a so-called active area or device area, is controlled on a plane pattern, and is arranged in the element main operation area trapezoidal portion 2 in FIG. .. On the one main surface side of the semiconductor substrate 101 shown in FIG. 1, together with the device main operating region trapezoidal part 2, two source pad trapezoidal parts 3a located in one of the device main operating region trapezoidal parts 2 are provided. , 3b, and one trapezoidal portion 4 for drain pad located on the other side of the trapezoidal portion 2 for element main operation region. A plurality of biting grooves 2A are formed on both edges of the element main operating region trapezoidal portion 2 so as to face each other. The bite groove 2A is a groove for increasing the creepage distance in the shape of a cove to obtain a high withstand voltage, and can be omitted depending on the purpose. Then, as shown in FIG. 2, a plurality of source regions 61a, 61b, ..., 61d and a plurality of drain regions 62e, 62f ,. , 61d and a plurality of drain regions 62e, 62f, ..., 62i facing each other, the main currents flowing between the source regions 61a, 61b ,. Controlled by electrodes (gate electrodes) 13p, 13q, 13r, ..., 13w.

[0033]

As shown in FIG. 1, it further has an external circuit connection region provided adjacent to the device main operation region trapezoidal portion 2, and the gate electrode is provided above the field insulating film 5 provided in the external circuit connection region. The gate pad base layer 16 is formed to extend to the external circuit connection region and has the same laminated structure as the gate electrode (see the sectional view of FIG. 12). In FIG. 1, the gate bonding pad 19GP is arranged in the external circuit connection region, but in the case of an integrated circuit or the like, an interlayer wiring layer or a surface wiring layer for connecting to another element main operation region is arranged. You may. That is, the gate pad base layer 16 shown in FIG. 1 is a metal layer having a relatively large area for enabling connection with various external circuits, and the active control electrodes 13p, 13q, 13r ,. .., 13w are metallurgically connected and have the same laminated structure.

[0034]

As shown in FIG. 2, the semiconductor substrate 101 includes, for example, a buffer layer 1B of n-type GaAs having a thickness of 300 to 500 nm and a thickness of 15 on a semi-insulating

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semiconductor substrate (semi-insulating GaAs substrate) 1A. A channel layer 1C made of n-type InGaAs having a thickness of 55 nm, a spacer layer 1D made of n-type AlGaAs having a thickness of 2-5 nm, an electron supply layer 1E made of n-type AlGaAs having a thickness of 3-15 nm, and a thickness of 10 to 25 nm. And a Schottky layer (Schottky contact layer) 1F made of n-type AlGaAs. The n-type channel layer 1C and the n-type spacer layer 1D are so-called "andove layers" in which impurities are not intentionally added. A plurality of n + type source regions (n + type ohmic contact regions) 61a, 61b, ..., 61d and a plurality of n + type drain regions (n + type ohmic contact regions) 62e are formed on the n type Schottky layer 1F. , 62f, ..., 62i are patterned and arranged. , 61d and drain regions 62e, 62f, ..., 62i are each made of n + type InGaAs or n + type GaAs having a thickness of 5 to 10 nm. . A heterojunction is formed between the channel layer 1C made of n-type InGaAs and the spacer layer 1D made of n-type AlGaAs. Then, electrons are supplied from the electron supply layer 1E and a two-dimensional electron gas is formed near the interface between the n-type channel layer 1C and the n-type spacer layer 1D.

[0035]

As shown in FIG. 2, a plurality of source electrodes 7S are respectively arranged on the plurality of source regions (ohmic contact regions) 61a, 61b, ..., 61d in the device main operating region trapezoidal portion 2. ing. A plurality of drain electrodes 7D are arranged on the plurality of drain regions (ohmic contact regions) 62e, 62f, ..., 62i, respectively. The plurality of drain electrodes 7D and the plurality of source electrodes 7S are arranged in parallel with each other and alternately.

[0036]

Gate electrodes 13p, 13q, 13r, ..., 13w are formed in the vicinity of the source electrode 7S between the source electrode 7S and the drain electrode 7D forming a pair. That is, one set of source region 61a, gate electrode 13p, and drain region 62e constitutes a first unit cell. The set of the source region 61a, the gate electrode 13q, and the drain region 62f constitutes a second unit cell, and the set of the source region 61b, the gate electrode 13r, and the drain region 62f constitutes a third unit cell. In this way, a plurality of unit cells are connected in parallel to form a HEMT 201 having a multi-channel structure.

[0037]

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Further, on the source pad trapezoidal portions 3a and 3b and the drain pad trapezoidal portion 4, a source pad base layer (not shown) and a drain pad lower layer formed in the same process as the source electrode 7S and the drain electrode 7D. A ground layer (not shown) is formed (FIG. 8 shows the source pad base layers 7SPa and 7SPb, the drain pad base layer 7DP, and the gate pad base layer 7GP). The source electrode 7S and the source pad base layer are connected by a source wiring 19S made of gold (Au) through a window (opening) formed in the interlayer insulating film 21. Further, the drain electrode 7D and the drain pad base layer are connected by a drain wiring 19D made of Au through a window (opening) formed in the interlayer insulating film 21. As shown in FIG. 1, source bonding pads 19SPa and 19SPb made of Au are formed on the source pad underlayer (not shown), and Au is formed on the drain pad underlayer (not shown). A drain / bonding pad 19DP is formed. The source bonding pads 19SPa and 19SPb are formed integrally with the source wiring 19S, and the drain bonding pad 19DP is formed integrally with the drain wiring 19D. A gate pad underlayer 16 is disposed between the source pad underlayer and the drain pad underlayer (not shown), and a gate bonding pad 19GP is formed on the gate pad underlayer 16. Then, as shown in FIG. 2, a passivation film 22 is formed on the entire surface so as to cover the interlayer insulating film 21, the source wiring 19S and the drain wiring 19D of the HEMT 201 having such a structure.

[0038]

Further, in the HEMT 201 according to the first embodiment of the present invention, as shown in FIG. 1, in addition to the gate electrodes 13p, 13q, 13r, ..., 13w, the gate electrodes 13p, 13q, 13r are also included. The gate lines 14 and 15 and the gate pad base layer 16 which are connected in series with 13w are formed. The gate line 14 is formed so as to connect the gate electrodes 13p, 13q; 13r, 13s; ... 13v, 13w located on both sides of the source electrode 7S on the drain pad trapezoidal portion 4 side. ing. In addition, the gate line 15 having a relatively wide width includes the gate electrodes 13p, 13q; 13r, 13s; ..; 13v, 13w located on both sides of the drain electrode 7D on the source pad trapezoidal portions 3a, 3b side. Are formed so as to be connected with each other. The gate pad base layer 16 is formed so as to be located between the two source pad trapezoidal portions 3a and 3b, and the gate electrodes 13p located on both sides of the drain electrode 7D located at the center; 13q, 13r; 13s, 13t; ...; 13u, 13v; 13w are connected on the source pad trapezoidal portions 3a, 3b side.

[0039]

Since the HEMT 201 having such a structure has the structure of the gate electrode 13 as shown in FIG. 3, the Al film 9 forming the gate electrode 13 includes the upper first Mo film 10 and the

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transition element oxide film (MoOx film).) 10A, protected by the laminated structure film of the second Mo film 11. Therefore, in the manufacturing process described below, the deterioration of the characteristics of the gate electrodes 13p, 13q, 13r, ..., 13w is suppressed without being corroded by an alkaline developing solution or an oxide film etching solution. , High manufacturing yield and reliability can be achieved. Further, since the gate electrodes 13p, 13q, 13r, ..., 13w employ a laminated structure film composed of the first Mo film 10, the transition element oxide film (MoOx film) 10A, and the second Mo film 11, Al hardly diffuses, and on the contrary, Mo does not pass through the Al film 9 and react with the Schottky layer 1F. Therefore, it has good Schottky characteristics with the semiconductor substrate 101. From this point, the high conversion conductance gm of the HEMT 201 can be obtained, and the high frequency characteristics can be improved.

[0040]
A method of manufacturing the semiconductor device (HEMT) 201 according to the first embodiment of the present invention will be described with reference to FIGS.

[0041]

(1) First, on a semi-insulating GaAs substrate 1A, a buffer layer 1B made of n-type GaAs having a thickness of 300 to 500 nm, a channel layer 1C made of n-type InGaAs having a thickness of 15 to 55 nm, and a thickness in order. Spacer layer 1D made of n-type AlGaAs having a thickness of 2 to 5 nm, electron supply layer 1E made of n type AlGaAs having a thickness of 3 to 15 nm, Schottky layer 1F made of n type AlGaAs having a thickness of 10 to 25 nm, thickness 5 to 10 nm The ohmic contact layer 1G made of n + type InGaAs is continuously epitaxially grown to obtain the semiconductor substrate 101.

For example, a semi-insulating GaAs substrate 1A having a thickness of about 250 μm to 450 μm is mounted on a susceptor of a low pressure metal organic chemical vapor deposition (MOCVD) apparatus, and a buffer layer 1B and a channel layer are sequentially formed on the GaAs substrate. 1C, the spacer layer 1D, the electron supply layer 1E, the Schottky layer 1F, and the ohmic contact layer 1G are continuously vapor-phase epitaxially grown. Specifically, for example, at a pressure of 50 Pa to 200 Pa, at a substrate temperature of 550 ° C. to 700 ° C., TEG (triethylgallium) and AsH3 (arsine) are introduced to grow the buffer layer 1B made of n-type GaAs. Further, TMIn (trimethylindium) is introduced to grow a channel layer 1C made of n-type InGaAs. Then, the introduction of TMIn is stopped, TMA (trimethylaluminum) is introduced instead, and the spacer layer 1D made of n-type AlGaAs, the n-type electron supply layer 1E made of n-type AlGaAs and the n-type Schottky made of n-type AlGaAs. Grow layer 1F. Further,

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instead of stopping the introduction of TMA, TMIn is introduced to grow an ohmic contact layer 1G made of n + type InGaAs. In growing the n-type electron supply layer 1E, the n-type Schottky layer 1F, and the ohmic contact layer 1G made of n + -type InGaAs, SiH4 (monosilane), Si2H6 (disilane), or DESe (diethyl selenium) is used as the n-type dopant gas. , DETe (diethyl tellurium) or the like may be used. After the continuous vapor phase epitaxial growth is completed, the semiconductor substrate 101 is taken out from the low pressure MOCVD apparatus. In addition to the MOCVD method, continuous epitaxial growth may be performed by a molecular beam epitaxy (MBE) method, a chemical beam epitaxy (CBE) method, a molecular layer epitaxy (MLE) method, or the like.

[0042]

(2) A resist (not shown) is applied to the entire surface of the semiconductor substrate 101 taken out from the low pressure MOCVD apparatus, and exposure / development is performed by the photolithography technique to pattern the resist to form a mesa etching mask. Using this mesa etching mask, as shown in FIGS. 4 and 5, the trapezoidal portion 2 for the element main operation region in which a plurality of bite grooves 2A are formed at both side edges on one main surface side of the semiconductor substrate 101. , Two source pad trapezoids 3a and 3b as connection pad formation regions located on one of the element main operation region trapezoids 2, and connection pad formation on the other of the element main operation region trapezoids 2 One drain pad platform 4 as a region is formed by a mesa etching process.

[0043]

(3) Next, a resist (not shown) is applied on the entire surface, exposure and development are performed by a photolithography technique to pattern the resist, and a recess etching mask is formed. By using this recess etching mask, the ohmic contact layer 1G is left only in the necessary places as the source / drain regions by reactive ion etching (RIE), and the ohmic contact layer 1G in other portions is selectively removed. .. As a result, a plurality of source regions (ohmic contact regions) 61a, 61b, ..., 61d and a plurality of drain regions (ohmic contact regions) 62e, 62f ,. The RIE is performed until the Schottky layer 1F is exposed to form a recess (recess) in the portion where the gate electrode is to be formed. By this recess etching step, a plurality of source regions 61a, 61b, ..., 61d and drain regions 62e, 62f ,. .. , 61d and drain regions 62e, 62f, ..., 62i are formed in parallel as a plurality of stripe-shaped patterns in a plan view. After the recess etching process is completed, the resist is removed, and the field insulating film 5 made of SiOx is deposited on the entire main surface of the semiconductor substrate 101 by the CVD method or the like, as shown in FIG.

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[0044]

(4) Next, a new resist (not shown) is applied on the entire surface again, and exposure and development are performed by the photolithography technique to pattern the resist to form an ohmic contact opening mask. By using this ohmic contact opening mask, the source regions (ohmic contact regions) 61a, 61b, ..., 61d and the drain regions (ohmic contact regions) 62e, 62f „. The field insulating film 5 is selectively removed. After that, the ohmic contact opening mask is removed, and another resist 6 is applied to the entire surface (note that the structure of the source pad trapezoidal portions 3a and 3b and the drain pad trapezoidal portion 4 is referred to as an element main operating region). If they are the same, the ohmic contact opening mask is left, and this is used as the resist 6.). Then, the resist is patterned by a photolithography technique to form a lift-off mask 6 having openings in a plurality of ohmic metal portions (source electrodes / drain electrodes), source pad underlayers, and drain pad underlayers. As shown in FIG. 7, an Au-based metal film 7 is deposited on the entire surface through the lift-off mask 6. Then, if the resist (lift-off mask) 6 is peeled off, a plurality of source regions (ohmic contact regions) 61a, 61b, ..., 61d and drain regions (ohmic contact regions) 62e, 62f „. A plurality of corresponding source electrodes 7S and drain electrodes 7D remain above .. Similarly, the metal films of the source pad base layers 7SPa and 7SPb and the drain pad base layer 7DP remain on the field insulating film 5. In this way, as shown in the plan view of FIG. 8, the plurality of source electrodes 7S and drain electrodes 7D, source pad base layers 7SPa and 7SPb, and drain pad base layer 7DP are patterned.

[0045]

(5) Thereafter, as shown in FIG. 9, gate electrodes 13p, 13q, 13r, ..., 13w made of a multilayer film of Ti / Al / Mo / MoOx / Mo are formed. A method of forming the Ti / Al / Mo / MoOx / Mo gate electrodes 13p, 13q, 13r, ..., 13w will be described later with reference to FIGS. As a result, as shown in the plan view of FIG. 10, the gate electrodes 13p, 13q, 13r, ..., 13w and the gate line 14 formed of Ti / Al / Mo / MoOx / Mo multilayer films connected in series are formed. , 15 and the gate pad base layer 16 are formed. The gate line 14 connects the gate electrodes 13p, 13q; 13r, 13s; 13V, 13w located on both sides of the source electrode 7S to each other on the drain pad trapezoidal portion 4 side. Is formed in. In addition, the gate line 15 having a relatively wide width includes the gate electrodes 13p, 13q; 13r, 13s ;. It is formed so as to be connected to each other on the 3b side. The gate pad base layer 16 is formed so as to be located between the two source pad trapezoidal portions 3a and 3b. The gate pad underlayer 16 connects the gate electrodes 13p, 13q; 13r, 13s; ... 13v, 13w on both sides of the drain electrode 7D located at the

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center on the side of the source pad trapezoidal portions 3a, 3b. is doing.

[0046]

(6) Next, as shown in FIG. 11, an interlayer insulating film 21 made of SiOx is deposited on the entire surface by the CVD method. Note that FIG. 11 is a cross-sectional view corresponding to the AA cross section of FIG. 10. Then, a resist 17 is applied over the entire surface of the interlayer insulating film 21, and exposed and developed by using a photolithography technique to form a contact hole opening mask 17 as shown in FIG. The contact hole opening mask 17 opens the interlayer insulating film 21 on the source electrode 7S, the drain electrode 7D, the source pad base layers 7SPa and 7SPb, the drain pad base layer 7DP, and the gate pad base layer 16, and the contact window portion. It is a mask pattern made of a resist 17 for forming a.

[0047]

(7) Next, using the contact hole opening mask made of the resist 17, the interlayer insulating film 21 is etched with an oxide film etching solution to form the drain pad contact hole 31DP, the drain electrode contact hole 31D, and the gate pad contact hole 31GP. Open. As the oxide film etching solution, a buffered hydrofluoric acid solution containing HF: NH4F = 1: 10 is used. Although the Al film is etched with a buffered hydrofluoric acid solution, in the present invention, the Al film forming the gate electrodes 13p, 13q, 13r, ..., 13w is an upper Mo film / molybdenum oxide film (MoOx).) / Mo film is protected by the laminated structure film so that the Ti / Al / Mo / MoOx / Mo gate electrodes 13p, 13q, 13r, ..., 13w are not corroded by the buffered hydrofluoric acid solution. .. Although not appearing on the cross section of FIG. 12, the source pad contact hole 31SP and the source electrode contact hole 31S are further shown by a one-dot chain line in the plan view of FIG. 12 is a cross-sectional view taken along the line BB of FIG. 13, and corresponding to FIG. 12, the drain pad contact hole 31DP, the drain electrode contact hole 31D, and the gate pad contact hole 31GP are also one point in FIG. It is shown with a dashed line. Then, the resist 17 used as the contact hole opening mask is removed.

[0048]

(8) Then, the surface of the semiconductor substrate 101 including the exposed surface of the Ti / Al / Mo / MoOx / Mo gate electrodes 13p, 13q, 13r ,. A new resist 18 is applied to the entire surface of the. Then, the resist 18 is subjected to mask alignment (exposure) and development by

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a photolithography technique to pattern the resist 18 to form a lift-off mask 18. Even if an alkaline developing solution is used for patterning the lift-off mask 18, the surface of the Ti / Al / Mo / MoOx / Mo gate electrodes 13p, 13q, 13r, ... Is not corroded. This is because the Al films forming the gate electrodes 13p, 13q, 13r, ..., 13w are protected by the upper layer Mo film / molybdenum oxide film (MoOx) / Mo film laminated structure film. The lift-off mask 18 is wider than the dimensions of the source electrode contact hole 31S, the drain electrode contact hole 31D, the source pad contact hole 31SP, the drain pad contact hole 31DP, and the gate pad contact hole 31GP shown in FIG. It is a pattern having an area. Further, a pattern of the source wiring 19S connecting the source electrode contact hole 31S and the source pad contact hole 31SP and a pattern of the drain wiring 19D connecting the drain electrode contact hole 31D and the drain pad contact hole 31DP are included. The pattern of the source wiring 19S and the pattern of the drain wiring 19D have a line width wider than the line widths of the source electrode contact hole 31S and the drain electrode contact hole 31D by the mask alignment margin, and have an interdigital (inter-digital) shape. Form an interdigitated comb pattern. The lift-off process mask 18 has an overhang shape as shown in FIG. The overhang shape is formed by controlling the film thickness of the resist 18, exposure conditions, development conditions, post-baking conditions, curing conditions and the like.

[0049]

(9) Au is vapor-deposited on one main surface side of the semiconductor substrate 101 through the lift-off mask 17, as shown in FIG. The Au film 19 is separated on the bottom of the resist 17 in the opening and on the resist 17. Then, the resist 17 as a lift-off mask is peeled off, that is, lift-off is performed, so that the resist 17 and the Au film 19 thereon are removed. As a result, as shown in FIGS. 15 and 1, a source wiring 19S connecting the source electrode 7S and the source pad base layers 7SPa and 7SPb is formed on the source electrode 7S. A drain wiring 19D that connects the drain electrode 7D and the drain pad base layer 7DP is formed on the drain electrode 7D. A plurality of the source wirings 19S and the drain wirings 19D are arranged in parallel with each other, and a comb-shaped pattern in which they interdigitate with each other is formed. Further, as shown in FIG. 1, source bonding pads 19SPa, 19SPb, drain bonding pad 19DP, and gate bonding pad 19GP made of Au are formed on the respective pad underlayers 7SPa, 7SPb, 7DP, 7GP. To be done.

[0050]

(10) Then, as shown in FIG. 2, a passivation film (protective film) 22 is formed on the entire surface. The passivation film 22 may be formed of an insulating film such as an oxide film (SiO2),

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a PSG film, a BPSG film, a nitride film (Si3N4), or a polyimide film. Further, the passivation film 22 on the source bonding pads 19SPa and 19SPb, the drain bonding pad 19DP, and the gate bonding pad 19GP made of Au is removed, and a gold (Au) wire or an aluminum (Al) wire having a diameter of 30 μm to 200 μm is removed. The HEMT 201 as the semiconductor device of the present invention is completed by providing the window portion to which the bonding wire made of is connectable.

[0051]
Here, a method of forming the Ti / Al / Mo / MoOx / Mo gate electrodes 13p, 13q, 13r, ..., 13w used in the semiconductor device (HEMT) 201 according to the first embodiment of the present invention will be described. , FIG. 16 to FIG. 21.

[0052]

(A) After forming the source electrode 7S and the drain electrode 7D, first, a new resist (not shown) is applied on the entire surface.

Then, exposure / development is performed by photolithography technique to pattern the resist to form an opening mask for gate electrode openings. Using this gate electrode opening mask, the field insulating film 5 near the source electrode 7S is selectively removed by RIE. That is, as shown in FIG. 16, a gate electrode opening 5A is formed in the field insulating film 5 between the source electrode 7S and the drain electrode 7D facing each other to expose the surface of the Schottky layer 1F (FIG. 16). 9 is a partially enlarged view of FIG. 9, and in FIG. 16, the source electrode 7S and the drain electrode 7D are present at positions protruding from the illustrated region). When the source electrode 7S and the drain electrode 7D are formed, if the field insulating film 5 between the source electrode 7S and the drain electrode 7D facing each other is removed, the field insulating film at this stage can be formed by the photolithography technique and RIE. The step of selective removal of 5 is unnecessary.

[0053]

(B) Then, for example, the semiconductor substrate 101 is housed in the sample stage inside the vapor deposition chamber of the multi-source electron beam (EB) vapor deposition apparatus. Inside this vapor deposition chamber, EB guns for Ti vapor deposition, Al vapor deposition, and Mo vapor deposition are provided. The vapor deposition chamber is evacuated until the internal

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pressure reaches a predetermined vapor deposition pressure (background pressure) of about 1.3 × 10 −5 Pa to 1.2 × 10 −8 Pa. Then, first, as shown in FIG. 16, a Ti film 8 is vapor-deposited on the entire surface to a film thickness of about 5 nm. After that, the EB gun is switched, and as shown in FIG. 17, the Al film 9 is vapor-deposited so as to be continuous with the Ti film 8 so as to have a thickness of about 500 nm. The EB gun is switched again, and as shown in FIG. 18, a first Mo film 10 as a metal film made of a 6A group transition element is vapor-deposited on the Al film 9 so that the film thickness is in the range of 15 nm to 100 nm. . The EB gun for Mo vapor deposition is stopped, oxygen (or air) is introduced into the bell jar of the vapor deposition apparatus through a needle valve, etc., and the pressure is, for example, 1.3 × 10 −3 Pa to 1.2 × 10 −2 Pa. Set to. By leaving for about 5 minutes under this oxidizing pressure, as shown in FIG. 19, an extremely thin oxide film (molybdenum oxide film: MoOx) 10A having a thickness of about 0.7 nm to 10 nm is formed on the surface of the first Mo film 10. . At this time, the temperature of the semiconductor substrate 101 is controlled at 200 ° C. to 350 ° C. by an infrared lamp (IR) lamp. Then, the introduction of oxygen (or air) is stopped, and the chamber is evacuated again until the pressure in the vapor deposition chamber reaches 1.3 × 10 −5 Pa to 1.2 × 10 −8 Pa. When the predetermined deposition pressure is reached, the EB gun for vapor deposition of Mo is used again to deposit the second Mo film 11 on the transition element oxide film (MoOx film) 10A so that the film thickness is in the range of 15 nm to 100 nm. As described above, the Ti film 8, the Al film 9, the first Mo film 10, and the second Mo film 11 are continuously deposited using a multi-source EB vapor deposition device. In particular, if a small-sized oxidation chamber (oxidation chamber) connected to the deposition chamber (deposition chamber) through a gate valve is provided, and a multi-chamber configuration capable of being transported by a transport mechanism utilizing magnetic force or the like is used, the first Mo The film 10, the transition element oxide film (MoOx film) 10A, and the second Mo film 11 can be continuously formed in a short time, and the productivity is also improved. In this case, the pressure during oxidation may be about 100 kPa to 1 Pa.

[0054]

(C) Next, the semiconductor substrate 101 is taken out from the bell jar of the multi-source EB vapor deposition apparatus, and the resist 12 is applied on the entire surface of the second Mo film 11. Exposure and development are performed by a photolithography technique to pattern the resist, thereby forming a gate electrode formation mask. .., 13w, gate lines 14 and 15, and openings for forming the gate pads 16 are used as a mask for the gate electrode formation mask. After that, as shown in FIG. 21, etching is performed by RIE using the resist 12 as a gate electrode forming mask to stack the Ti film 8, the Al film 9, the first Mo film 10, the molybdenum oxide film (MoOx) 10A, and the second Mo film. The film 11 is patterned. As a result, as shown in the plan view of FIG. 10, gate electrodes 13p, 13q, 13r, ..., 13w, gate lines 14 and 15 and a gate pad base layer 16 which are connected in series are formed.

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[0055]

(Second Embodiment) The semiconductor device of the present invention is not limited to the HEMT described in the first embodiment. For example, the MESFET described in the second embodiment may be used.

[0056]

The MESFET 202 according to the second embodiment corresponds to the structure in which the spacer layer 1D, the electron supply layer 1E, and the Schottky layer 1F are omitted in the semiconductor substrate 101 described in the HEMT 201 according to the first embodiment. That is, as shown in FIG. 22, a buffer layer 1B made of n-type GaAs having a thickness of 300 to 500 nm and an active layer made of n-type GaAs having a thickness of 200 to 500 nm are sequentially formed on a semi-insulating GaAs substrate 1A. , 61d and a plurality of drain regions 62e, 62f, ..., 62i arranged on the (channel layer) 1K and the active layer 1K, and a semiconductor substrate. 102 is configured. , 61d and drain regions 62e, 62f, ..., 62i are ohmic contact layers made of n + type GaAs having a thickness of 5 to 10 nm. . Gate electrodes 13p, 13q, 13r, ..., 13w are formed between each pair of source electrode 7S and drain electrode 7D. , 61d and a plurality of drain regions 62e, 62f, ..., 62i facing each other, the main currents flowing between the control regions (gates) , Electrodes 13p, 13q, 13r, ..., 13w. A plurality of source electrodes 7S are arranged on the plurality of source regions (ohmic contact regions) 61a, 61b, ..., 61d, respectively, as shown in FIG. A plurality of drain electrodes 7D are arranged on the plurality of drain regions (ohmic contact regions) 62e, 62f, ..., 62i, respectively. The plurality of drain electrodes 7D and the plurality of source electrodes 7S are arranged in parallel with each other and alternately. The source electrode 7S is connected to the source wiring 19S in the upper layer thereof through the opening of the interlayer insulating film 21, and the drain electrode 7D is connected to the drain wiring 19D in the upper layer thereof. Then, as shown in FIG. 22, a passivation film 22 is formed on the entire surface so as to cover the interlayer insulating film 21, the source wiring 19S and the drain wiring 19D of the MESFET 202 having such a structure.

[0057]

The plan view of the MESFET 202 according to the second embodiment may be the same as the HEMT 201 shown in FIG. That is, the MESFET 202 further has a device main operation region

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trapezoidal portion 2 and an external circuit connection region provided adjacent to the device main operation region trapezoidal portion 2 as in FIG. The gate pad base layer 16 is formed to extend over the field insulating film 5 provided in the external circuit connection region and has the same laminated structure as the gate electrode in the external circuit connection region. A gate bonding pad 19GP is formed on the gate pad base layer 16. On the surface of the trapezoidal portion 2 for the main element operation region, the source wiring 19S and the drain wiring 19D are formed in an inter-digital form, as in FIG.

[0058]

FIG. 23 shows an enlarged cross-sectional view of the structure of the unit cell in the element main operation region of the semiconductor device (MESFET) 202 according to the second embodiment. FIG. 23 shows that a unit cell is composed of one set of the source region 61a, the gate electrode 13q, and the drain region 62f. On the left side of the source region 61a, a pair of source region 61a, gate electrode 13p, and drain region 62e form another unit cell. On the right side of the drain region 62f (not shown in FIG. 23), a set of source region 61b, the gate electrode 13r, and the drain region 62f constitute yet another unit cell (see FIG. 22). Thus, as shown in FIG. 22, a plurality of unit cells are connected in parallel to form a MESFET 202 having a multi-channel structure.

[0059]

FIG. 23 shows the structure of one Schottky gate electrode 13q of the MESFET 20. Of course, the other gate electrodes 13p, 13r, ..., 13w have the same sectional structure. That is, the Schottky gate electrode 13q is composed of the semiconductor substrate 1, the field insulating film 5 arranged on the surface of the semiconductor substrate 1, the barrier metal layer 8 formed on the semiconductor substrate 1 in the opening of the field insulating film 5, and the barrier. At least an Al film 9 arranged on the metal layer 8 and a cover metal layer 51 arranged on the Al film 9 are provided. 23, the field insulating film 5 between the source electrode 7S and the drain electrode 7D can be omitted. For example, the field insulating film 5 may be configured so that its opening exposes almost the entire surface of the element main operation region. That is, the field insulating film 5 may also serve as a device isolation insulating film in the device isolation region. When the field insulating film 5 also serves as the element isolation insulating film in the element isolation region, a plurality of source electrodes 7S and drain electrodes 7D are arranged inside the openings of the field insulating film 5. That is, the field insulating film 5 between the source electrode 7S and the drain electrode 7D that face each other may be removed when the plurality of source electrodes 7S and drain electrodes 7D are formed.

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[0060]

In FIG. 23, the cover metal layer 51 includes a first transition element thin film 10 made of a 6A group transition element, a transition element oxide film 10A above the first transition element thin film 10, and a transition, as in the first embodiment. It is composed of the second transition element thin film 11 on the element oxide film 10A. As described in the first embodiment, the cover metal layer 51 has the laminated structure in which the transition element oxide film 10A is interposed between the first transition element thin film 10 and the second transition element thin film 11. The diffusion preventing effect is greater than that of the metal layer composed only of the 6A group transition element. By forming the transition element oxide film 10A between the first transition element thin film 10 and the second transition element thin film 11, a substantial film thickness of the 6A group transition element thin film is obtained, and the first transition element thin film 10 and the first transition element thin film 10A are formed. It is also possible to prevent the adhesion between the two transition element thin films 11 from deteriorating.

[0061]

As described in the first embodiment, the film thickness of the first transition element thin film 10 is 15 nm to 100 nm, the film thickness of the transition element oxide film 10A is 0.7 nm to 10 nm, and the film thickness of the second transition element thin film 11. Is about 15 nm to 100 nm. By setting the thickness within such a range, film peeling can be suppressed and the diffusion preventing effect (diffusion barrier effect) can be maintained high. Mo is preferable as the 6A group transition element, and in this case, the transition element oxide film 10A in FIG. 23 is a molybdenum oxide film (MoOx) 10A. The composite film of Mo and MoOx (Mo laminated structure film) is effective as a diffusion barrier layer because it has etching resistance to a buffered hydrofluoric acid solution and an alkaline developing solution, and Al atoms of the underlayer 16 are difficult to diffuse. To function. In FIG. 23, on the semiconductor substrate 1, a Ti film 8 as a barrier metal film, an Al film 9, a first Mo film 10 as a first transition element thin film, a MoOx film 10A as a transition element oxide film, and a second film are sequentially formed. A second Mo film as a transition element thin film is laminated.

[0062]

The method of manufacturing the MESFET 202 according to the second embodiment of the present invention is basically the same as that of the HEMT 201 shown in FIGS. 4 to 15.

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[0063]

(1) First, on a semi-insulating GaAs substrate 1A, a buffer layer 1B made of n-type GaAs having a thickness of 300 to 500 nm, an active layer 1K made of n-type GaAs having a thickness of 200 to 500 nm, and a thickness in order. An ohmic contact layer (not shown) made of n + type GaAs having a thickness of 5 to 10 nm is continuously epitaxially grown to obtain a semiconductor substrate 102.

A resist (not shown) is applied to the entire surface of the semiconductor substrate 102, and exposure and development are performed by a photolithography technique to pattern the resist, thereby forming a mesa etching mask. Using this mesa etching mask, as shown in FIGS. 4 and 5, the trapezoidal portion 2 for the element main operation region in which a plurality of bite grooves 2A are formed at both side edges on one main surface side of the semiconductor substrate 102. , Two source pad trapezoids 3a and 3b as connection pad formation regions located on one of the element main operation region trapezoids 2, and connection pad formation on the other of the element main operation region trapezoids 2 One drain pad platform 4 as a region is formed by a mesa etching process.

[0064]

(2) Next, a resist (not shown) is applied over the entire surface, and exposure / development is performed by a photolithography technique to pattern the resist, thereby forming a recess etching mask. By using this recess etching mask, the ohmic contact layer is left only in the necessary portions as the source / drain regions by reactive ion etching (RIE), and the ohmic contact layer 1G in the other portions is selectively removed and activated. Expose layer 1K. As a result, a plurality of source regions (ohmic contact regions) 61a, 61b, ..., 61d and a plurality of drain regions (ohmic contact regions) 62e, 62f ,. The RIE is performed until the active layer 1K is exposed to form a recess (recess) in the portion where the gate electrode is to be formed. By this recess etching step, a plurality of source regions 61a, 61b, ..., 61d and drain regions 62e, 62f ,. .. After the recess etching process is completed, the resist is removed, and the field insulating film 5 made of SiOx is deposited on the entire surface of the active layer 1K by the CVD method or the like, as shown in FIG.

[0065]

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Since the subsequent steps are exactly the same as the method for manufacturing the HEMT 201 according to the first embodiment, considering that the cross-sectional structure of the semiconductor substrate 102 is different from that of the semiconductor substrate 101, duplicate description will be omitted. .. Since the MESFET 202 manufactured by such a manufacturing method has the structure of the gate electrode 13 as shown in FIG. 23, the Al film 9 forming the gate electrode 13 includes the upper first Mo film 10 and the transition element oxide film. (MoOx film) 10A and the second Mo film 11 are protected by a laminated structure film. Therefore, during the manufacturing process, the characteristics of the gate electrodes 13p, 13q, 13r, ..., 13w are suppressed from being corroded by an alkaline developing solution, an oxide film etching solution, or the like, which is high. Manufacturing yield and reliability can be achieved. Further, since the gate electrodes 13p, 13q, 13r, ..., 13w employ a laminated structure film composed of the first Mo film 10, the transition element oxide film (MoOx film) 10A, and the second Mo film 11, Al hardly diffuses, and on the contrary, Mo does not pass through the Al film 9 and react with the Schottky layer 1F. Therefore, it has good Schottky characteristics with the semiconductor substrate 1. Therefore, a high conversion conductance gm of the MESFET 202 can be obtained, and high frequency characteristics can be improved.

[0066]

(Other Embodiments) It should not be understood that the description and drawings forming part of the disclosure of the first and second embodiments of the present invention described above limit the present invention. From this disclosure, various alternative embodiments, examples, and operation techniques will be apparent to those skilled in the art.

[0067]

For example, in the first and second embodiments, Mo is exemplified as the 6A group transition element, but Cr, W and the like can be used as well known in addition to Mo. When Cr is used as the 6A group transition element, the cover metal layer is preferably composed of a first Cr film / CrOx / second Cr film. Further, the first transition element thin film and the second transition element thin film may be composed of different 6A group transition elements. For example, Cr film / MoOx / Mo film, Cr film / CrOx / Mo film, Mo film / MoOx / Cr film, Mo film / CrOx / Cr film, W film / WOx / Mo film, W film / MoOx / Mo film, etc. The structure of does not matter.

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[0068]
Although Ti is illustrated as the barrier metal layer 8 in the first and second embodiments, TiW, TiN, metal silicide, or the like can be used instead of Ti.

[0069]

Further, the HEMT described in the first embodiment has various structures, and the invention is not limited to the HEMT disclosed in the first embodiment.

For example, on a semi-insulating GaAs substrate, an electron supply layer made of n-type AlGaAs having a thickness of 3 to 15 nm and a spacer made of n-type AlGaAs having a thickness of 2 to 5 nm via a buffer layer made of n-type GaAs. The reverse structure HEMT may be formed by laminating a layer, a channel layer made of n-type GaAs having a thickness of 15 to 55 nm, and a Schottky layer made of n type GaAs having a thickness of 10 to 25 nm. Further, a HEMT having a first electron supply layer (lower layer electron supply layer) and a second electron supply layer (upper layer electron supply layer) obtained by combining these may be used. されている。 A semi-insulating InP substrate may be used instead of the semi-insulating GaAs substrate, and a HEMT using a hetero junction such as AlInAs / InGaAs or Si / SiGe other than the AlGaAs / InGaAs or AlGaAs / GaAs hetero junction may be used.

[0070]

In the first and second embodiments of the present invention, the element main operating region is provided in the element main operating region trapezoidal portion 2 as shown in FIG. 1, and the external circuit connection region is provided in the element main operating region trapezoid. The structure provided on the trapezoid different from the part 2 or on the bottom of the recess between the trapezoids is shown. However, the surface of the semiconductor substrate may be flattened to provide an element isolation region by proton irradiation, and the surface of the element isolation region may be used as an external circuit connection region. It is also possible to provide an element isolation region with a U groove and an element isolation insulating film embedded in the U groove, and use the surface of this element isolation region as an external circuit connection region.

[0071]

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Further, the semiconductor device of the present invention is not limited to the HEMT described in the first embodiment or the MESFET described in the second embodiment. For example, individual semiconductor elements such as Schottky diodes, Schottky gate type SITs, Schottky gate type thyristors, etc., or semiconductor integrated circuits composed of these may be used. Furthermore, the semiconductor device is not limited to a semiconductor device based on a compound semiconductor, and a single element semiconductor such as Si may be used.

[0072]

Further, in the description of the first embodiment, the gate bonding pad 19GP, the source wiring 19S, the drain wiring 19D, and the like are formed by the lift-off method, but the present invention is not limited to this, and a normal method is used. A method using resist patterning and etching technology may be used.

[0073]

The stoichiometric silicon nitride film (Si_3N_4) is not etched by the buffered hydrofluoric acid solution.

However, some silicon nitride films (SiNx) having a non-stoichiometric composition or silicon oxynitride films (SiOxNy) containing oxygen are etched with a buffered hydrofluoric acid solution. Further, an oxide film containing impurities such as phosphorus glass (PSG) can also be etched with the buffer hydrofluoric acid solution. Therefore, the interlayer insulating film of the present invention is not limited to the oxide film (SiOx) only, and all insulating films that can be etched with a buffered hydrofluoric acid solution are targeted.

[0074]

As described above, needless to say, the present invention includes various embodiments and the like not described here. Therefore, the technical scope of the present invention is defined only by the matters specifying the invention according to the scope of claims appropriate from the above description.

[0075]

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According to the present invention, since the uppermost cover metal layer of the electrode film has etching resistance to the buffer hydrofluoric acid solution, the etching process is performed when the insulating film is opened to expose the electrode film. Thus, the Schottky metal layer (Al) has an effect of preventing corrosion such as corrosion and after-corrosion.

[0076]
According to the present invention, since the uppermost cover metal layer of the electrode film has etching resistance to the alkaline developing solution, the connection pad and the interlayer wiring member are formed on the cover metal layer by the lift-off method. In this case, it is possible to prevent the Al film as the Schottky metal layer from being corroded by the alkaline developer.

[0077]

Further, according to the present invention, film peeling can be suppressed by setting the structure of the cover metal layer to a predetermined structure.

Further, the Al film and the cover metal layer do not react with each other, and it is possible to prevent the characteristics of the gate electrode that forms a Schottky junction with the semiconductor layer from being deteriorated.

[0078]

Furthermore, according to the present invention, it is possible to provide a manufacturing method capable of preventing the occurrence of corrosion such as corrosion and after-corrosion in the Al film.

Then, it is possible to efficiently manufacture a semiconductor device having a gate electrode having good Schottky characteristics.

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CLAIMS JP2002217425

1.
A barrier metal layer formed on a semiconductor substrate, an aluminum (Al) film arranged on the barrier metal layer, a group 6A transition element arranged on the aluminum film, and a group 6A transition element An electrode for a semiconductor device, comprising a cover metal layer made of a composite film with an oxide film.

2.
The cover metal layer is composed of a first transition element thin film made of the 6A group transition element, the oxide film above the first transition element thin film, and a second transition element thin film above the oxide film. The electrode for a semiconductor device according to claim 1, wherein the electrode is for a semiconductor device.

3.
The film thickness of the said 1st transition element thin film is 15 nm-100 nm, The electrode for semiconductor devices of Claim 2 characterized by the above-mentioned.

4.
The film thickness of the said oxide film is 0.7 nm-10 nm, The electrode for semiconductor devices of Claim 2 or Claim 3 characterized by the above-mentioned.

5.

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The film thickness of the said 2nd transition element thin film is 15 nm-100 nm, The electrode for semiconductor devices of any one of Claims 2-4 characterized by the above-mentioned.

6.

The electrode for a semiconductor device according to any one of claims 1 to 5, wherein the transition element of the 6A group is molybdenum (Mo).

7.

A semiconductor substrate, a field insulating film arranged on the surface of the semiconductor substrate, and a barrier metal formed on the semiconductor substrate in an opening of the field insulating film provided in an element main operation region of the semiconductor substrate. Layer, a cover metal composed of an aluminum (Al) film arranged on the barrier metal layer, and a composite film of a group 6A transition element and an oxide film of the group 6A transition element arranged on the aluminum film A semiconductor device comprising a gate electrode composed of a layer.

8.

The semiconductor device further has an external circuit connection region provided adjacent to the element main operation region, the gate electrode is extended to an upper portion of the field insulating film provided in the external circuit connection region, 8. The semiconductor device according to claim 7, wherein a gate pad underlayer having the same laminated structure as the gate electrode is formed in the external circuit connection region.

9.

An interlayer insulating film disposed on the field insulating film, and an external circuit connecting metal wire connected to the gate pad underlying layer at an opening of the interlayer insulating film provided on the surface of the gate pad underlying layer. 9. The semiconductor device according to claim 8, further comprising a layer.

10.

The cover metal layer includes a first transition element thin film made of the 6A group transition element, the oxide film on the first transition element thin film, and the second transition element thin film on the oxide film. The semiconductor device according to claim 7, wherein the semiconductor device is a semiconductor device.

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11.

11. The semiconductor device according to claim 10, wherein the first transition element thin film has a thickness of 15 nm to 100 nm.

12.

12. The semiconductor device according to claim 7, wherein the oxide film has a thickness of 0.7 nm to 10 nm.

13.

12. The semiconductor device according to claim 10, wherein the film thickness of the second transition element thin film is 15 nm to 100 nm.

14.

14. The semiconductor device according to claim 7, wherein the 6A group transition element is molybdenum (Mo).

15.

A step of forming a field insulating film on a surface of a semiconductor substrate, a step of selectively removing a part of the field insulating film to form an opening for exposing the semiconductor substrate, and a step of exposing the bottom of the opening. A barrier metal layer on the upper part of the semiconductor substrate and the field insulating film, an aluminum (Al) film on the barrier metal layer, and a group 6A transition on the aluminum film. A step of forming a cover metal layer formed of a composite film of an element and the 6A group transition element oxide film, and selectively removing the cover metal layer, the aluminum film, and the barrier metal layer to form inside the opening. And a step of forming a gate electrode composed of the barrier metal layer, the aluminum film, and the cover metal layer.

16.

For the cover metal layer, after depositing a first molybdenum (Mo) film on the aluminum film, the surface of the first molybdenum film is oxidized to form the Group 6A transition element oxide film, and thereafter, The method of manufacturing a semiconductor device according to claim 15, wherein a second molybdenum film is formed by depositing a second molybdenum film on the Group 6A transition element oxide film.

17.

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A step of depositing an interlayer insulating film on the cover metal layer, a step of applying a first resist on the interlayer insulating film, a step of selectively exposing a part of the first resist, The surface of the cover metal layer is exposed to the interlayer insulating film with a buffered hydrofluoric acid solution using the step of developing the first resist after exposure and the etching mask formed by the steps of exposing and developing. 17. The method of manufacturing a semiconductor device according to claim 15, further comprising the step of etching up to.

18.

A step of removing the first resist and a step of applying a second resist on the cover metal layer and the interlayer insulating film exposed at the bottom of the opening of the interlayer insulating film formed by the etching process liquid. 18. The semiconductor according to claim 17, further comprising: a step, a step of selectively exposing a part of the second resist, and a step of developing the exposed second resist with an alkaline developing solution. Device manufacturing method.

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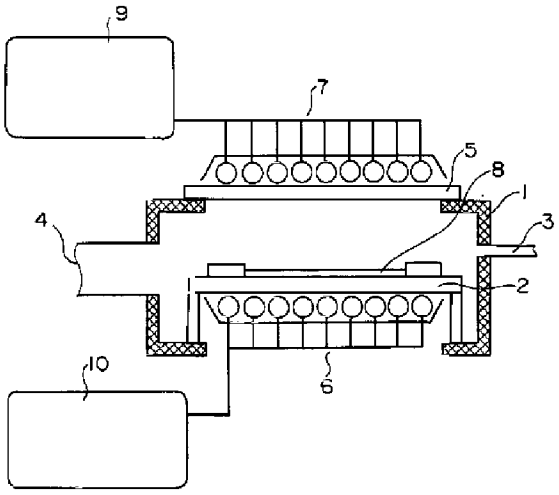
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(71)出願人　000003078
株式会社東芝
東京都港区芝浦一丁目１番１号
(72)発明者　伊藤　貴之
神奈川県横浜市磯子区新杉田町８番地　株式会社東芝横浜事業所内
(72)発明者　飯沼　俊彦
神奈川県横浜市磯子区新杉田町８番地　株式会社東芝横浜事業所内
(74)代理人　100091629
弁理士　竹村　壽

最終頁に続く

(54)【発明の名称】　熱処理方法及び半導体装置の製造方法

(57)【要約】
【課題】　４００℃程度の低温で良質な強誘電体膜を形成すること、低温でコンタクト性の高いコンタクト部を形成すること、低温で急速にシリサイド形成を行うことなどを実施するための熱処理方法を提供する。
【解決手段】　少なくとも２種類以上のランプを備え、第１のランプ（ハロゲンランプなど）６を点灯して試料（シリコンウェーハ）８を加熱し、一定の温度に達したところで第２のランプ（フラッシュランプ）７を点灯し、試料の温度をさらに上昇させ所望の温度に到達せしめる。即ち、点灯時間の異なる少なくとも２種類以上のランプを用いて加熱する工程を具備する。本発明は、コンタクトプロセスのサーマルバジェットの低減化を目的に発光波長分布と照射時間が異なる第１の加熱源と第２の加熱源とを組み合わせ、配線や電極と半導体基板や導電体膜とのコンタクト部等を高速反応させてコンタクト抵抗を低抵抗化させる。



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【特許請求の範囲】
【請求項１】　試料を加熱処理する際に、点灯時間の異なる少なくとも２種類以上のランプを用いて加熱する工程を具備し、前記試料を加熱処理する際に、第１の種類のランプを点灯し、続いて、前記第１の種類のランプの点灯中にフラッシュランプからなる第２の種類のランプを点灯して試料を加熱することを特徴とする熱処理方法。
【請求項２】　半導体基板上に絶縁膜を形成し、この絶縁膜に前記半導体基板もしくはこの半導体基板上に形成された導電体膜を露出させるコンタクト孔を形成する工程と、
前記コンタクト孔から露出している半導体基板表面もしくは前記導電体膜に接続する配線もしくは導電性電極を堆積させてコンタクト部を形成する工程と、
前記半導体基板を熱処理することにより前記半導体基板表面もしくは前記導電体膜と前記配線もしくは前記導電性電極との前記コンタクト部のコンタクト性を向上させる工程とを備え、
前記半導体基板を熱処理する工程において、発光波長分布及び照射時間の異なる２つの加熱源を用い、第１の加熱源を照射し、照射中もしくは照射停止後熱処理温度が低下する前に第２の加熱源を前記第１の加熱源の照射時間よりも短い時間照射することを特徴とする半導体装置の製造方法。
【請求項３】　前記配線もしくは導電性電極は、前記半導体基板表面もしくは前記導電体膜の表面に形成される酸化膜を還元できる金属膜であることを特徴とする請求項２に記載の半導体装置の製造方法。
【請求項４】　前記酸化膜を還元できる金属膜は、酸化膜形成時と下地である前記半導体基板もしくは前記導電体膜を構成する元素との化合物形成時を併せた生成熱が、前記半導体基板表面もしくは前記導電体膜の表面に形成される酸化膜の生成熱より負に大きいことを特徴とする請求項３に記載の半導体装置の製造方法。
【請求項５】　前記酸化膜を還元できる金属膜にはシリコンが５～２０原子％含有されていることを特徴とする請求項４に記載の半導体装置の製造方法。
【請求項６】　前記加熱源は、発光波長が赤外領域にある前記第１の加熱源と、それより短波長側にある発光波長を有する第２の加熱源からなることを特徴とする請求項３乃至請求項５に記載の半導体装置の製造方法。
【請求項７】　前記第２の加熱源は、発光波長領域の少なくとも一部が紫外領域にあることを特徴とする請求項６に記載の半導体装置の製造方法。
【請求項８】　前記第２の加熱源は、フラッシュランプであることを特徴とする請求項６に記載の半導体装置の製造方法。
【請求項９】　前記第１の加熱源による前記半導体基板の温度は、前記絶縁膜、前記導電体膜、前記配線及び前記導電性電極の特性劣化の誘発しない温度より低く、前記第２の加熱源は、低負荷内でコンタクト部の反応が促進する照射エネルギー密度に設定されることを特徴とする請求項２乃至請求項８のいずれかに記載の半導体装置の製造方法。
【請求項１０】　半導体素子が形成された半導体基板上に層間絶縁膜を介して少なくとも１層のアルミニウム配線を形成する工程と、
前記アルミニウム配線上に層間絶縁膜を介して、下部電極、強誘電体膜、上部電極を順次スパッタリング法により堆積させる工程と、
前記半導体基板を熱処理することにより前記強誘電体膜を結晶化して前記下部電極、前記強誘電体膜及び前記上部電極からなるキャパシタを形成する工程とを備え、
前記半導体基板を熱処理する工程において、点灯時間の異なる少なくとも２種類以上のランプを用い、第１の種類のランプを点灯し、点灯中もしくは消灯後熱処理温度が低下する前に第２の種類のランプであるフラッシュランプを前記第１の種類のランプの点灯時間よりも短い時間点灯することを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は、半導体の製造装置及び半導体の製造プロセスに関し、特に、強誘電体膜を結晶化するため、もしくはコンタクト部のコンタクト特性を向上させる熱処理装置と熱処理方法及び半導体装置の製造方法に関するものである。
【０００２】
【従来の技術】近年、強誘電体メモリ（ＦｅｒｒｏｅｌｅｃｔｒｉｃＲＡＭ）が注目されている。ＤＲＡＭと略同等の応答速度を持ち、且つ記憶が消えない不揮発性という特徴を持つためである。その特徴は、汎用メモリはもとよりロジックデバイスと混載するシステムＬＳＩでいかんなく発揮されるものとして期待を集めている。強誘電体メモリ素子の断面を図１６に示す。図から明らかなように、下から順に、トランジスタ、強誘電体キャパシタ、配線が形成されている。この強誘電体メモリ素子においてキャパシタの下部電極１０１は、プレート線を兼ねており、強誘電体膜１０２を挟んで上部電極１０３は、ビット線に接続されている。製造プロセスは、当然のことながら、最初にトランジスタが作成され、次に、強誘電体キャパシタが形成される。そして、接続孔が開孔されてＡｌ－Ｃｕ配線が形成される。接続孔内の接続配線は、タングステン（Ｗ）が用いられる。
【０００３】強誘電体メモリを製造する場合の困難さの一つは、強誘電体がプロセス損傷を受け易いということである。多層配線を形成するためのドライエッチングやスパッタリングを行った際に、プラズマ中の荷電粒子の影響を受け、さらに、これらのプロセスが減圧下で行われるのでチタン酸ジルコン酸鉛ＰＺＴ（Ｐｂ（Ti_x・

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Zr_{1-x}) O_3) やタンタル酸ストロンチウムビスマスSBT (Sr_2 BiTaO_9) などの強誘電体中に酸素が脱離し、強誘電性を著しく損ってしまう。このような多層配線形成工程のプロセスダメージを避けるための一つの工夫として、例えば、特開平11-317500号公報には、多層配線を先に形成し、その上に強誘電体キャパシタを作成する方法が提案されている。多層配線を先に形成し、その上に強誘電体キャパシタを形成するのであるから、当然のことながら強誘電体は、配線形成工程のプロセスダメージを受けることはない。このプロセスの問題点は、強誘電体であるPZTやSBTの結晶化温度が、アルミニウム配線の耐える温度（450℃）よりも高いという点にある。PZTの結晶化温度は、低くても550℃であり、一方、SBTの場合は少なくとも650℃を要する。このような温度に加熱するとアルミニウムが溶融し、配線が分断するなどの問題が発生する。

【0004】このような問題を避けるために、例えば、熱処理温度が450℃程度のCVD(Chemical Vapour Deposition)で形成するプロセスが研究されているが、低温では、良質の強誘電体性能が実現されていない。強誘電体としての充分な性能を得るためには、やはり高い温度で充分に結晶化させる必要がある。加熱される時間が非常に短ければ、温度は高くてもアルミニウムは変質して溶融することはない。例えば、500℃の場合、数秒以内であれば、アルミニウムは変質しない。したがって、RTP (Rapid Thermal Process)も一つの手段となり得るが、現在のRTPで、例えば、650℃に加熱した場合、450℃以上に到達している時間が長いため、アルミニウムに変質が起きてしまう。このように現在では、高温を要する結晶化とアルミニウムが変質しない温度以下でのプロセスという狭間に挟まれて、解が見つからない状況である。

【0005】また、現在トランジスタの高性能化を進める上でゲート絶縁膜が薄膜化されるに及んでゲート電極空乏化という問題が顕在化している。ゲート電極空乏層の存在により寄生容量が増大してしまうので非常に薄いゲート絶縁膜を形成したとしても実効的な酸化膜厚が厚くなってしまう。これを解決するためには、メタルゲート電極もしくは高誘電率ゲート絶縁膜を用いることが極めて有効である。しかし、メタルゲートや高誘電体膜が直面する問題点の一つにコンタクトプロセスの低温化がある。通常、Si基板の表面上には自然酸化膜が存在しているため、それが障壁層となって金属とのコンタクトをとるのが難しい。近年、半導体装置のコンタクト部の形成方法は、層間絶縁膜にパターニングされ開口されたコンタクト孔に電極あるいは電極の下地層として金属導電性の膜を堆積させ、その後赤外加熱炉で550℃1時間以上の熱処理が行われてきた。この熱処理の目的は、電極と半導体基板界面の自然酸化膜を還元して低抵抗オーミックコンタクトの形成を行うことである。

【0006】しかし、従来の熱処理条件はサーマルバジェットが大きく、抵抗率の低い金属であるAlは融点が低いために、また高誘電体材料であるTa_2 O_5 は結晶化に伴いゲートリーク電流が増大するために、各々ゲート電極やゲート絶縁膜として用いるには十分ではない。また、素子特性の更なる高性能化への実現のためには低誘電率材料を層間絶縁膜に用いる必要があるが、従来の熱工程では密度の低下に伴い力学的強度が減少したり吸湿性が増加したりするため、トランジスタへの適用が困難になる。但しコンタクト部形成の熱処理温度を500℃以下にまで低温化するとコンタクト抵抗及び半導体基板面内でのバラツキが共に増大することが判明している。これは、500℃以下の熱処理ではシリコン基板表面上の自然酸化膜を十分に還元することができないるためである。

【0007】

【発明が解決しようとする課題】以上のように、現在トランジスタの高性能化を進める上でゲート絶縁膜が薄膜化されるに及んでゲート電極空乏化という問題が顕在化している。そして、前述の低サーマルバジェットでコンタクト部を形成するという問題があった。さらに多層配線上に強誘電体キャパシタを形成する方法は、多層配線のダメージを避けることが出来るが、上述のようにアルミニウムが変質しない温度で強誘電体を結晶化しなければならないという制約がある。本発明は、このような事情によりなされたものであり、400℃程度の低温で良質な強誘電体膜を形成すること、低温でコンタクト性の高いコンタクト部を形成すること、低温で急速にシリサイド形成を行うことなどを実施するための熱処理方法及びこの熱処理方法を利用した半導体装置の製造方法を提供する。

【0008】

【課題を解決するための手段】本発明は、少なくとも2種類以上のランプを備え、まず、第1のランプを点灯して試料を加熱し、一定の温度に達したところで第2のランプを点灯し、試料の温度をさらに上昇させ所望の温度に到達せしめることを特徴としている。従来のRTPの場合、所望の温度まで一種類のランプで加熱する。例えば、熱処理温度を700℃とすると、700℃まで1種類のランプで加熱する。標準的なRTPの性能である50℃／秒で昇温したとすると、700℃に到達するまでに14秒、処理時間をゼロとして直ちに降温するとしても降温に20秒以上を要するため、トータルの熱処理時間は30秒を越える。試料が半導体基板であり、この上にアルミニウム配線が形成され、その上に層間絶縁膜を介して形成された強誘電体膜を結晶化により熱処理する場合において、アルミニウムにとって危険温度である450℃以上に加熱される時間は、10秒以上に及ぶことになり、アルミニウム配線の溶解に至ることになる。ア

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ルミニウムは、４５０℃で加熱を続けても１時間は変質しない。５００℃では１０～１５秒程度は、加熱を続けることができる。５５０℃では5～6秒程度は、加熱を続けることができる。

【０００９】さらに、６００℃では、大体1～2秒で変質する。アルミニウムは、６６０℃で溶融する。しかし、溶融温度より低い温度でも加熱時間を上記のような範囲を越えると、変質する。このような変質とはアルミニウム配線におけるアルミニウム粒が成長してヒロックが生じる状態をいう。第1のランプを用いて予備加熱を行うことが必要な理由は、以下の通りである。すなわち、第2のランプで加える熱エネルギーには、ある程度の制限が加わる。照射時間の非常に短いフラッシュランプだけで試料表面を加熱しようとすると、場合よっては、大きな熱エネルギーが必要になることがある。そのような場合、狙いどおり強誘電体を結晶化できたとしても、印可されたエネルギーが下層に伝導し、そして、トータルのエネルギー量が多いためにアルミニウムの温度が上昇するという問題が起こる。第2のランプで投入される熱エネルギーは、強誘電体だけが加熱され、且つ結晶化に必要な程度に加熱されるように調整されなければならない。そのために、ある程度まで予備加熱しておくことが意味を持つのである。

【００１０】図１０は、ランプエネルギーと強誘電体膜の熱処理による温度の照射されるランプのエネルギー依存性を示す特性図である。図に示すように、強誘電体膜は、所定の温度になると結晶化が始まり、さらに高い温度Ｔになると分解する。そしてそれぞれに対応した必要エネルギーが図に示したエネルギー曲線から求まる。結晶化に必要なエネルギーは、エネルギー幅ｄの間にある。図１１は、本発明を実施するに際して結晶化温度と熱処理時間との関係を示す特性図である。本発明では、第1のランプで強誘電体膜を所定の温度（Ｔ１又はＴ２）に予備加熱しておき、次に、短時間で昇温させることができる第2のランプで、例えば、１０００分の1秒程度の短時間のうちに結晶化温度（Ｔｃ）にまで温度を上げる。第2のランプが与えるエネルギー量は、予備加熱の温度に依存している。第2のランプのエネルギー量を少なく（例えば、Ｅ２）したいときは、予備加熱温度を高く（例えば、Ｔ２）し、予備加熱時間を短くする（例えば、ｔ２）と良い。フラッシュランプを第2のランプとして用いた場合において、エネルギー量を２７ジュール（Ｊ）／ｃｍ^2 以下に設定すれば、強誘電体膜の下層に形成されたアルミニウム配線が溶融し破損しない。例えば、ＰＺＴ強誘電体膜を結晶化する場合において、予備加熱温度を４００℃に設定すると、フラッシュランプのエネルギーは、１０Ｊ／ｃｍ^2 以上で結晶化する。

【００１１】予備加熱を５５０℃に設定すると、フラッシュランプのエネルギーが7～8Ｊ／ｃｍ^2 で結晶化する。このように予備加熱温度が高い場合は、第１ランプの予備加熱温度を１秒以下にすることができる。ランプを用いず、試料台中にヒーターを埋め込み、このヒーターを用いて予備加熱を行うことも可能である。しかし、この場合、加熱されたヒーター上に試料を載置する関係上、本来の結晶化が起こる時間を挟んで前後の予備加熱時間は、数１０秒に及ぶことになる。予備加熱温度がアルミニウムにとって問題のない温度であれば、この方法も可能である。しかし、第2のランプで印可する熱エネルギーの大きさによっては、５００℃程度の予備加熱しなければならないことも起こりうる。その場合、アルミニウムの変質を考えると、予備加熱時間を秒単位に短縮しなければならない。そのために予備加熱をランプで行うことが必要となるのである。ランプで予備加熱を行う方法が様々なケースに対応できるという幅広い応用性を持つのである。

【００１２】また、本発明は、コンタクトプロセスのサーマルバジェットの低減化を目的に、発光波長分布と照射時間が異なる第１の加熱源と第２の加熱源とを組み合わせることを特徴としている。配線や電極と半導体基板や導電体膜とのコンタクト部を高速反応させることによりコンタクト抵抗の低抵抗化が実現される。また、発光波長分布及び照射時間が異なる第１の加熱源と第２の加熱源を組み合わせてシリサイド形成を行うことを特徴としている。低温かつ急速にシリサイド形成を行うことができるため、耐熱性の低いメタルゲートや高誘電率ゲート絶縁膜、低誘電率層間絶縁膜などの新材料をトランジスタに適用できることが容易になり、素子特性の高性能化が実現できる。すなわち、本発明の熱処理方法は、試料を加熱処理する際に、点灯時間の異なる少なくとも２種類以上のランプを用いて加熱する工程を具備し、前記試料を加熱処理する際に、第１の種類のランプを点灯し、続いて、前記第１の種類のランプの点灯中にフラッシュランプからなる第２の種類のランプを点灯して試料を加熱することを特徴としている。

【００１３】本発明の半導体装置の製造方法は、半導体基板上に絶縁膜を形成し、この絶縁膜に前記半導体基板もしくはこの半導体基板上に形成された導電体膜を露出させるコンタクト孔を形成する工程と、前記コンタクト孔から露出している半導体基板表面もしくは前記導電体膜に接続する配線もしくは導電性電極を堆積させてコンタクト部を形成する工程と、前記半導体基板を熱処理することにより前記半導体基板表面もしくは前記導電体膜と前記配線もしくは前記導電性電極との前記コンタクト部のコンタクト性を向上させる工程とを備え、前記半導体基板を熱処理する工程において、発光波長分布及び照射時間の異なる２つの加熱源を用い、第１の加熱源を照射し、照射中もしくは照射停止後熱処理温度が低下する前に第２の加熱源を前記第１の加熱源の照射時間よりも短い時間照射することを特徴としている。前記配線もし

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くは導電性電極は、前記半導体基板表面もしくは前記導電体膜の表面に形成される酸化膜を還元できる金属膜でも良い。前記酸化膜を還元できる金属膜は、酸化膜形成時と下地である前記半導体基板もしくは前記導電体膜を構成する元素との化合物形成時を併せた生成熱が、前記半導体基板表面もしくは前記導電体膜の表面に形成される酸化膜の生成熱より負に大きいようにしても良い。

【００１４】前記酸化膜を還元できる金属膜にはシリコンが５～２０ｗｔ％含有されているようにしても良い。前記加熱源は、発光波長が赤外領域にある前記第１の加熱源と、それより短波長側にある発光波長を有する第２の加熱源からなるようにしても良い。前記第２の加熱源は、発光波長領域の少なくとも一部が紫外領域にあっても良い。前記第２の加熱源は、フラッシュランプであってもよい。前記第１の加熱源による前記半導体基板の温度は、前記絶縁膜、前記導電体膜、前記配線及び前記導電性電極の特性劣化の誘発しない温度より低く、前記第２の加熱源は、低負荷内でコンタクト部の反応が促進する照射エネルギー密度に設定されるようにしても良い。

【００１５】また、本発明の半導体装置の製造方法は、半導体素子が形成された半導体基板上に層間絶縁膜を介して少なくとも１層のアルミニウム配線を形成する工程と、前記アルミニウム配線上に層間絶縁膜を介して、下部電極、強誘電体膜、上部電極を順次スパッタリング法により堆積させる工程と、前記半導体基板を熱処理することにより前記強誘電体膜を結晶化して前記下部電極、前記強誘電体膜及び前記上部電極からなるキャパシタを形成する工程とを備え、前記半導体基板を熱処理する工程において、点灯時間の異なる少なくとも２種類以上のランプを用い、第１の種類のランプを点灯し、点灯中もしくは消灯後熱処理温度が低下する前に第２の種類のランプであるフラッシュランプを前記第１の種類のランプの点灯時間よりも短い時間点灯することを特徴としている。本発明の製造方法により形成された半導体装置は、半導体基板と、前記半導体基板に形成されたソース／ドレイン領域と、前記半導体基板上に形成され、少なくとも前記ソース／ドレイン領域の対向する領域間上に形成されたゲート絶縁膜と、前記ゲート絶縁膜上に形成されたゲート電極と、少なくとも前記ソース／ドレイン領域表面に形成されたコバルトシリサイド表面層とを備えたことを特徴としている。

【００１６】

【発明の実施の形態】以下、図面を参照して発明の実施の形態を説明する。まず、図９に示す概略断面図を参照して本発明の熱処理装置を説明する。この熱処理装置は、アルミニウムからなる試料チャンバー１を有し、この試料チャンバー１内部には、試料を載置する試料台２、ガスを導入するガス導入口３、排気する排気口４、光を導入するための上部の石英窓５、試料を予備加熱するための棒状のランプ（第１のランプ）６、フラッシュランプ（第２のランプ）７を備えている。棒状ランプ６は、３ｋＷのタングステンハロゲンランプで１６本、試料８の下に設置され、試料８を下から加熱する。一方、フラッシュランプ７は、同様に棒状のランプであり、１５本が試料８の上に設置され、試料８を上から加熱する。両ランプは、いずれもそれぞれ専用の電源９、１０に接続されている。ランプ点灯のタイミング、点灯時間及びフラッシュランプの点灯回数は、マイコンによって制御されるように構成されている。前記２種類のランプは、棒状のランプであることが本質的ではなく、ランプの分野でシングルエンドと呼ばれる一方向に外部端子が２つ設けられたタイプのランプでも同様の効果を期待することができる。

【００１７】次に、図１及び図２を参照して第１の実施例を説明する。図１は、半導体基板と配線とのコンタクト部の形成方法を説明する製造工程断面図である。まず、図１（ａ）に図示するように、単結晶シリコン基板４１にＣＶＤ(Chemical Vapor Deposition) 法で２００ｎｍのSiO_2 膜４２を堆積させる。次に、図１（ｂ）に図示するように、SiO_2 膜４２をパターニングして、０．３μｍ×０．３μｍのコンタクト孔４３を開口する。次に、SiO_2 膜４２をマスクとしてシリコン半導体基板４１にボロン（Ｂ）を加速エネルギー１０ｋｅＶ、ドーズ$5\times10^{15}cm^{-2}$でイオン注入する。これにより、図１（ｃ）に図示するように、イオン注入層４４が形成される。ここで、シリコン半導体基板４１の表面には、ｐ型層形成不純物に限らず、Ｐ、Ａｓ等のイオン注入によるｎ型導電層が形成されても良い。この後、赤外ランプ加熱炉（ＲＴＡ）の窒素雰囲気中で１０００℃１０秒の熱処理を行う。これにより、図１（ｄ）に示すように、イオン注入層４４の結晶回復が行われると共に不純物の活性化が行われて、イオン注入層４４は、ソース／ドレイン領域などに用いられるｐ型不純物拡散領域４７になる。次に、この不純物拡散領域４７上も含めてシリコン半導体基板４１上に膜厚３０ｎｍ以下の金属膜４５を堆積させる。金属膜４５としてはシリコン半導体基板上の自然酸化膜を還元できる金属、例えば、Ｔｉが望ましい。

【００１８】これに適した金属として、他にはIIIa、IVａ、Va族の高融点金属が挙げられる。この後、シリコン半導体基板１を窒素雰囲気中で赤外加熱炉内で４００℃に加熱し、加熱中にエネルギー密度１０Ｊ／cm^{-2}、パルス幅１ｍｓｅｃを有するＸｅフラッシュランプを１パルス照射させる。これにより、金属膜５と下地シリコン半導体基板４１とのオーミックコンタクトが形成された。次に、図１（ｅ）に図示するように、抵抗率の低い金属膜４６、例えば、Ａｌを膜厚４００ｎｍ程度堆積させてから、コンタクト孔４３に合わせてパターニングして電極４８を形成する。なお、本発明における半導体装置のコンタクト部形成における赤外加熱炉の熱処理条件

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は、５００℃以上の温度で長時間処理されることのないように設定される。上述の方法によって形成したこの実施例のサンプルＳ１において、Ａｌ電極と不純物拡散層間のコンタクト抵抗を実測したところ、１．３×10^{-7} Ωｃｍ^2 であった。

【００１９】実施例におけるコンタクト抵抗の低減効果を調べるために、フラッシュランプの照射を行わずに、４００℃の基板加熱のみを行い、図１（ｅ）と同じ構造のサンプルＳ２を比較例として形成する。比較例のサンプルＳ２のコンタクト抵抗を実測したところ、５．３×10^{-4} Ωｃｍ^2 であった。さらに、従来の赤外加熱炉のみの熱処理条件５５０℃、９０分で作製された図１（ｅ）と同じ構造のサンプルＳ３のコンタクト抵抗を実測したところ、２．５×10^{-7} Ωｃｍ^2 であった。上述の結果から、実施例のサンプルＳ１では、比較例サンプルＳ２に比べてコンタクト抵抗が著しく低下しており、従来例のサンプルＳ３と比べても低下していることが分かる。

【００２０】次に、実施例のサンプルＳ１、比較例のサンプルＳ２及び従来例のサンプルＳ３において、金属配線とシリコン半導体基板とのコンタクト部の元素の拡散挙動及び反応形態の様子をオージェ分光分析により調べる。その結果を図２に示す。図２は、本発明、比較例び従来の半導体装置のコンタクト部の反応形態においてフラッシュランプの効果を説明する組成図であり、縦軸が元素の組成比（ａｔｏｍ％）、横軸がＡｒイオンスパッタリング時間（分）を表わしている。即ち、横軸は深さ方向に対応している。図２（ａ）が実施例サンプルＳ１、図２（ｂ）が比較例サンプルＳ２、図２（ｃ）が従来例サンプルＳ３である。ここでは、さらにコンタクト抵抗を下げる方法としてシリコン半導体基板表面上に導電体膜$CoSi_2$ 層を設けており、金属膜ＴｉとＣｏＳｉ$_2$ 層との反応形態の様子が示されている。

【００２１】図２に示されるように、比較例のサンプルＳ２では、Ｔｉ／$CoSi_2$ 界面に酸素が検出されており、$CoSi_2$ 上に絶縁体の自然酸化膜（SiO_2 、ＣｏＯ）が存在していることが分かる。一方、実施例サンプルＳ１及び従来例サンプルＳ３では、$CoSi_2$ 上に自然酸化膜は検出されず、金属膜Ｔｉにより還元されていることが分かる。さらには、Ｔｉと下地シリコン半導体基板との相互拡散が生じており、Ｔｉシリサイド層を形成していることが判明した。ちなみに、比較例サンプルＳ２では、熱処理時間を９０分以上続けても、Ｔｉシリサイド層の形成を確認することはできなかった。以上の結果から、シリコン半導体基板表面上に存在する自然酸化膜の還元反応と金属膜によるシリサイド層の形成が、低抵抗コンタクト形成の鍵を握ると考えられる。低温熱処理ではシリコン半導体基板表面の自然酸化膜を金属膜であるＴｉが還元しきれずに、Ｔｉシリサイド層の形成が抑制されていたためコンタクト抵抗を下げることができなかったと考えられる。この実施例におけるＸｅフラッシュランプの効果は、熱以外に光エネルギーをも利用することにより、赤外加熱炉では到達することのできないエネルギーを極短時間で得ることができたため、金属膜と下地シリコン半導体基板との高速反応が可能となり、低サーマルバジェットでコンタクト抵抗の低減化が実現できたものである。

【００２２】本発明は、上記実施例に限られるものではない。半導体装置のコンタクト部を形成するための２つの加熱源は、発光波長が赤外領域にある加熱源とそれよりも短波長側で発光波長の少なくとも一部が紫外領域にあれば良く、例えば、Ａｒ、N_2 、エキシマ等のレーザや水素ランプを適用することも可能である。

【００２３】次に、図３乃至図５を参照して第２の実施例を説明する。図３は、比較例サンプルＳ４のコンタクト部の反応形態においてフラッシュランプの効果を説明する組成図であり、縦軸が元素の組成比（ａｔｏｍ％）、横軸がＡｒイオンスパッタリング時間（分）を表わしている。即ち横軸は深さ方向に対応している。前述の第１の実施例にしたがって半導体装置を製造する。但し、この実施例における金属配線とシリコン半導体基板とのコンタクト部を形成するための熱処理条件は、基板温度を１００～４８０℃、Ｘｅフラッシュランプの照射エネルギー密度を５～２５Ｊ／ｃｍ^2 の範囲内に設定する。即ち、この実施例では、第１の加熱源による基板温度は高融点金属膜、ここではＴｉ層が熱処理中の雰囲気からの影響を受けずに素子特性としての劣化を誘発しない温度を条件とし、第２の加熱源では光源本体の低負荷内でコンタクト部の反応が促進できる照射エネルギーに設定している。実施例におけるコンタクト部の反応効果を調べるために、基板温度を５００℃に設定し、Ｘｅフラッシュランプの照射エネルギー密度を１０Ｊ／ｃｍ^2 に設定したサンプルＳ４を比較例として作製する。

【００２４】比較例のサンプルＳ４のＡｌ電極と不純物拡散層間のコンタクト抵抗を実測したところ７．２×10^{-3} Ωｃｍ^2 であった。上述の結果から、比較例サンプルＳ４は、第１の実施例のサンプルＳ１と比べてコンタクト抵抗が却って増大してしまうことが分かった。図３（ａ）は、比較例のサンプルＳ４について、オージェ分光分析からコンタクト部の反応形態の様子を調べた結果を示している。比較例サンプルＳ４ではＴｉ層に相当量の酸素が取り込まれており、最表面に約１５ｎｍ程度のＴｉ酸化膜が存在しているばかりか、Ｔｉシリサイド層の膜厚も減少してしまっていることが分かる。このことは、基板温度が高くなるほど雰囲気の影響を受け易くなり、基板表面側から侵入してくる酸素量が増加することによりＴｉシリサイド層の成長率が制限されてしまうことを示唆している。すなわち、比較例サンプルＳ４では、金属膜Ｔｉが酸化されて絶縁体となってしまったことと、ＴｉシリサイドのＳｉ成長が抑制されてしまったこと

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とで、コンタクト抵抗が増大したものと考察される。

【００２５】そこで、シリコン半導体基板の基板温度を室温にした状態で、Ｘｅフラッシュランプ（照射エネルギー：１０Ｊ／ｃｍ^2）のみで、図１（ｅ）に図示する構造のサンプルＳ５を作製する。この時のサンプルＳ５のコンタクト抵抗は、３．１×１０$^{-5}$Ωｃｍ^{2}であり、実施例サンプルと比べると著しく高いものであった。図３（ｂ）にはサンプルＳ５について、オージェ分光分析からコンタクト部の反応形態の様子を調べた結果を示している。以上の結果から、Ｔｉ層の酸化反応を阻止するために、第１の加熱源による基板温度を低く設定し過ぎても、第２の加熱源であるＸｅフラッシュランプのみでは、低抵抗コンタクトの形成は困難であることが分かる。Ｘｅフラッシュランプ照射のみで金属シリサイド層を形成するには、３０Ｊ／ｃｍ^{2}以上の照射エネルギー密度が必要になってくると予想されるが、照射エネルギー密度が大きくなるほど、金属シリサイドの生成量を制御することが困難となり、またフラッシュランプ負荷の面から考えても実用的とはいえない。

【００２６】図４は、低サーマルバジェットでコンタクト部にＴｉシリサイド層を形成し、低抵抗オーミックコンタクトを形成するために必要な第１の加熱源による基板温度と、第２の加熱源によるＸｅフラッシュランプ（パルス幅１ｍｓｅｃ時）の照射エネルギー密度との関係を示すものである。図中、斜線で示された領域は、Ｘｅフラッシュランプの寿命を考慮した範囲内で５×１０$^{-7}$Ωｃｍ^{2}以下の低抵抗コンタクトを形成することができる条件を示している。４８０℃付近までは基板温度を増加させるほど、低エネルギー密度のフラッシュ照射で、５×１０$^{-7}$Ωｃｍ^{2}以下の低抵抗コンタクトが得られることが分かる。図５は、Ｘｅフラッシュランプを１０回照射させた場合を図示したものである。照射回数を増加させると５×１０$^{-7}$Ωｃｍ^{2}以下の低抵抗コンタクトの得られる条件が低温、低照射エネルギー側へ広がることが分かる。以上から、金属配線とシリコン半導体基板とのコンタクト部を形成するための熱処理条件は、基板温度を１００～４８０℃、Ｘｅフラッシュランプの照射エネルギー密度を５～２５Ｊ／ｃｍ^{2}の範囲内に設定するのが適当である。

【００２７】次に、図６を参照して第３の実施例について説明する。この実施例では、第１の実施例にしたがって半導体装置を製造する。ただし、この実施例における金属配線とシリコン半導体基板とのコンタクト部を形成するための電極下地層として、５～２０％のＳｉが添加された金属導電性膜を堆積させる。Ｔｉ－１０％Ｓｉの金属導電性膜をコンタクト底に堆積させ、その後、シリコン半導体基板の基板温度４００℃でＸｅフラッシュランプをエネルギー密度１０Ｊ／ｃｍ^{2}で１パルス照射させて、図１（ｅ）に図示する構造のサンプルＳ６を作製する。即ち、本発明による特徴は、高融点金属膜をコンタクト底に堆積する前に、コンタクト界面で金属シリサイド層を形成するためのＳｉを予め高融点金属膜内に含有させておくことにより熱工程に伴う下地基板であるシリコン半導体基板のシリコン表面側への前方拡散量を抑制し、シリサイデーション反応を抑制することで接合リーク電流の低減化を図ることにある。

【００２８】この実施例におけるサンプルＳ６の接合リーク電流の低減効果を調べるために、コンタクトプロセスの熱工程は実施例のサンプルＳ６と同じであるが、Ｓｉ未添加の金属膜Ｔｉを電極下地層としたサンプルＳ１を用いて、比較実験を行う。実施例のサンプルＳ６において、逆方向バイアス電圧５Ｖ印加時の接合リーク電流を実測したところ３．５×１０$^{-9}$Ａ／ｃｍ^{2}であった。また、Ａｌ電極と不純物拡散層間のコンタクト抵抗は、３．６×１０$^{-7}$Ωｃｍ^{2}であった。一方、比較例のサンプルＳ１（第１の実施例では実施例サンプル）において、接合リーク電流を実測したところ、５．１×１０$^{-7}$Ａ／ｃｍ^2（コンタクト抵抗：１．３×１０$^{-7}$Ωｃｍ^2）であった。さらに、第２の加熱源を使わずに第１の加熱源のみで５５０℃、９０分の熱処理を行った従来例サンプルＳ３の接合リーク電流は２．６×１０$^{-9}$Ａ／ｃｍ^2（コンタクト抵抗：２．５×１０$^{-7}$Ωｃｍ^2）であった。これより、実施例サンプルＳ６の接合リーク電流は、従来例サンプルＳ３と同レベルのリーク電流が得られており、また比較例のサンプルＳ１と比べた場合にはコンタクト抵抗の上昇は見られるものの接合リーク電流は２桁近くも低くなり、極めて効果的に改善できることが分かる。

【００２９】第２の加熱源を組み合わせるコンタクト部の形成方法は、金属シリサイド層を厚く形成できることでコンタクト抵抗の低減化には著しい効果が見られたものの、その反面、下地シリコン半導体基板の金属膜側への前方拡散量が多く、シリコン半導体基板内に空孔ができてしまい、その空孔が逆バイアス印加時に空乏層中に含まれてしまうために接合リーク電流の増大を招いていたと考えられる。そこで、金属膜堆積前にＳｉを予め添加させておくことで、熱処理に伴う下地シリコン半導体基板からのＳｉの拡散量を抑制し、シリサイデーション反応を制御しつつ金属シリサイド層を形成することができたために接合リーク電流の改善に至ったと考察される。図６は、基板温度４００℃でＸｅフラッシュランプを照射エネルギー密度１０Ｊ／ｃｍ^{2}で１パルス照射した時のＴｉ中に添加されるＳｉの量に対するコンタクト抵抗と接合リーク電流（５Ｖ印加時）の関係を示す特性図である。Ｓｉの添加量が増えるほどコンタクト抵抗は上昇するが、接合リーク電流が小さくなることが分かる。コンタクト抵抗と接合リーク電流の両面からスペックを満たすことのできるＳｉ添加量の範囲は、５～２０％であることが示されている。

【００３０】以上、金属配線とシリコン半導体基板との

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良好なコンタクト特性を有するコンタクト部を形成するための電極下地層としての金属導電性膜に5～20%のSiを添加することが有効であることが分かる。次に、図7及び図8を参照して第4の実施例を説明する。この実施例ではロジック素子の不純物拡散領域と接続プラグとのコンタクト部の製造に本発明を適用する。p型シリコン半導体基板51の素子分離領域（STI）53に囲まれた素子領域にMOSトランジスタが形成されている。MOSトランジスタは、ソース／ドレイン領域を構成するn型不純物拡散領域57と、この不純物拡散領域57間の上に形成されたシリコン酸化膜からなるゲート絶縁膜54と、ゲート絶縁膜54上に形成されたポリシリコンなどからなり、側壁絶縁膜により保護されたゲート電極50が形成されている。ゲート電極50、不純物拡散領域57の表面にはコバルトシリサイド（$CoSi_2$）層55が形成され低抵抗化されている。半導体基板51の表面にはプラズマCVDにより形成されたシリコン窒化膜56が形成されている。シリコン窒化膜56の上にはBPSG膜及びその上のTEOS膜からなる層間絶縁膜52が形成されている。

【0031】層間絶縁膜52の表面は、平坦化され、TiN／Tiバリアメタル層とこのバリアメタル層に挟まれたAl－Cu金属膜から構成された金属配線59が形成されている。この金属配線59とMOSトランジスタのゲート電極50及び不純物拡散領域57は、層間絶縁膜52に形成されたコンタクト孔に埋め込まれた接続プラグ58により電気的に接続されている。接続プラグ58は、コンタクト孔の内壁に形成されたTiN／Tiバリアメタル層とこのバリアメタル層に包まれたタングステン（W）から構成されている。この接続プラグ58は、シリサイド層55に接続される。図7に示すA領域にそのコンタクト部が示される。シリサイド層は、ゲート電極50のポリシリコン上及び不純物拡散領域57上にコバルト膜をスパッタリング等により堆積させ、加熱処理してシリサイド化することにより形成される。しかし、A領域に示すコンタクト構造は、SiO_2 及びCoO層が形成されているので、高抵抗になっている（図8（a））。そこで、通常は、接続プラグのバリアメタル層を形成してから550℃、90分の条件でアニールしてSiO_2 及びCoO層を消失させ、低抵抗化させている（図8（b））。この実施例ではこのような条件でアニールを行わず、半導体基板を赤外線加熱により400℃で加熱し、加熱中にエネルギー密度10J／cm_2、パルス幅1msecを有するXeフラッシュランプを1照射させる。これにより、400℃の低温でありながら、従来と同じ、図8（b）に示すA領域の構造が得られる。

【0032】次に、図12乃至図14を参照して第5の実施例を説明する。図12は、1トランジスタ・1キャパシタ構成の強誘電体メモリセルの等価回路を示しており、これは、DRAMセルの等価回路と同じ回路接続を有する。図13は、FRAMが形成された半導体基板の断面図である。従来のFRAMが形成された半導体基板は、トランジスタの上に強誘電体キャパシタ、その上に多層配線が形成された構造であるが、この実施例では、加熱処理する試料としてトランジスタの上に多層配線が形成され、多層配線の上に強誘電体キャパシタが形成された構造の半導体基板を用いる。図14は、本発明が適用されるFRAM構造の半導体装置の製造工程を説明するフローチャートである。まず、ウェーハにメモリなどに用いられるMOSトランジスタを形成し（1）、次に、層間絶縁膜を介してアルミニウムもしくはアルミニウムを主成分とする金属配線を多層構造に形成する（2）。その後、層間絶縁膜を介して強誘電体膜を有するキャパシタを形成する（3）。この半導体装置は、図16に示すFRAM構造のものに比較してキャパシタの位置が上下入れ代わっていることに特徴がある。

【0033】Cはペロブスカイト構造を有する強誘電体を電極間絶縁膜に用いた情報記録用のキャパシタ、Qはこのキャパシタに直列に接続されている電荷転送用MOSトランジスタ、WLはこのMOSトランジスタのゲートに接続されているワード線、BLはMOSトランジスタのソース／ドレイン領域の一方に接続されているビット線PLは、上記キャパシタの一端（プレート）に接続されているプレート線、VPLはプレート線電圧である。図13は、強誘電体特性のある強誘電体膜を有するキャパシタを具備したFRAMの断面図である。p型シリコン半導体などからなる半導体基板20にはLOCOS法によるSiO_2 から構成された素子分離領域が形成されている。半導体基板20の表面領域にはソース／ドレイン領域として用いられるn型不純物拡散領域21が形成されている。ソース／ドレイン領域間の上にはゲート酸化膜（SiO_2）22を介してゲート電極23が形成されている。ワード線（WL）に繋がるゲート電極23は、ポリシリコン膜とポリシリコン膜上のタングステンシリサイド膜などからなり、上面はシリコン窒化膜により保護されている。半導体基板20は、ゲート電極23を覆うように減圧CVD法により形成された層間絶縁膜として用いられるBPSG(Born Phospharus Silicate Glass)膜からなる第1の絶縁膜241により被覆されている。第1の絶縁膜241は、CMP(Chemical Mechanical Polishing) などにより研磨されて平坦化される。

【0034】第1の層間絶縁膜241にはバリアメタル層を介在させたアルミニウムなどの金属配線251が埋め込み形成されている。第1の層間絶縁膜241上には、それぞれ第2乃至第4の金属配線252～254が埋め込み形成されたシリコン酸化膜などからなる第2乃至第4の層間絶縁膜242～244が形成され、第4の層間絶縁膜244上には第5の層間絶縁膜245が堆積

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されている。第5の層間絶縁膜245の上には、強誘電体キャパシタCが形成されている。キャパシタCは、層間絶縁膜245に接触し、下部電極301、強誘電体特性を有するPZTなどの強誘電体膜302及びプレート線（PL）に繋がる上部電極303が順次堆積された積層体から構成されている。第1乃至第5の層間絶縁膜241～245にはコンタクト孔が形成され、そこにタングステンなどの接続プラグ27が埋め込み形成され、接続プラグ27は、下部電極301とMOSトランジスタQのソース／ドレイン領域の一方とを電気的に接続している。ソース／ドレイン領域の他方は、ビット線（BL）（図示しない）に繋がっている。

【0035】下部電極301は、層間絶縁膜245に接触するTi膜及びTi膜の上に形成されたPt膜から構成されている。上部電極303は、Pt膜から構成されている。キャパシタCを被覆するように層間絶縁膜245上に絶縁膜28が形成されている絶縁膜28は、TEOS膜（SiO_2 膜）などからなる。絶縁膜28は、CMPなどにより平坦化される。絶縁膜28にはエッチングによりコンタクト孔及び配線溝が形成され、そこにアルミニウムなどの金属配線（PL）29が埋め込み形成される。以上、説明したFRAMにおいてキャパシタ強誘電体膜は、本発明の結晶化方法を適用して形成される。すなわち、PZTやSROPなどの強誘電体膜をアモルファス状態で成膜させ、その後に熱処理により結晶化してキャパシタ誘電体として用いる膜が形成される。

【0036】次に、図15を参照して第6の実施例を説明する。図15は、強誘電体膜を誘電体とするキャパシタが形成された半導体基板の断面図である。p型（100）シリコン半導体基板31を加熱炉に入れ酸素雰囲気中で850℃に加熱し、膜厚100nmの熱酸化膜32を形成する。この上に、アルゴンガスを用いるスパッタリングによってアルミニウム（Al）膜33を膜厚400nm程度堆積する。この上に、SiH_4 とN_2O ガスを用いるプラズマCVD法によりシリコン酸化膜34を膜厚500nm程度堆積する。この半導体基板31上に、さらに、スパッタリングによって金属チタン（Ti）膜35と白金（Pt）36を、それぞれ30nmと100nmの膜厚で堆積する。次に、再びスパッタリング装置を用いて、チタン酸ジルコン酸鉛（$PbZr_xTi_{1-x}O_3$ 、以下、PZTという）膜37を膜厚150nm程度堆積する。このときのスパッタリングに用いたガスは、アルゴンガスで、スパッタリング中の基板温度は、室温とする。

【0037】この半導体基板31を図9に示す加熱処理装置に入れ、酸素を導入しながら、結晶化を行う。この工程は、まず、半導体基板31を予備加熱するために下からのタングステンハロゲンランプ（第1のランプ）6に3kWを投入し、1秒間に80℃の速度で昇温した。昇温開始から5秒後400℃の到達した時点でフラッシュランプ（第2のランプ）7を1回だけ点灯し、その直後にタングステンハロゲンランプ6を消灯した。フラッシュランプ7の点灯時間は、1．3msecであり、そのエネルギーは、12J／cm^2 である。このように本発明を実施した半導体基板をX線回析で分析したところ、フラッシュランプ6を照射しなかった試料（半導体基板）ではPZTが結晶化していなかったのに対し、フラッシュランプを照射した試料ではペロブスカイト相に結晶化していることが確認された。同時に下地のアルミニウム膜33の状態を顕微鏡と走査型電子顕微鏡で調べたが、全く変化が認められず、アルミニウム膜33を変化させることなくPZT膜37を結晶化させることが可能であることが明らかになった。タングステンハロゲンランプ7による予備加熱温度を400℃に固定し、PZT膜の結晶化に要するフラッシュランプ8の出力を調べたところ、10J／cm^2 以上では結晶化が起こることが判明した。

【0038】また、逆に予備加熱温度をパラメーターとしてアルミニウム膜33を変化させることなくPZT膜37を結晶化させることが出来る範囲を調べると、予備加熱時間を1秒以内にすれば550℃程度まで加熱してもアルミニウム膜33に変化が起こらないことが確認できた。この半導体基板31上に再びPt膜38をアルゴンガスを用いるスパッタリングにより形成した。膜厚は、150nmとした。この試料の分極特性を測定したところ、残留分極値が30μC／cm2あり、通常のRTAで結晶化したPZT膜に比較して何ら遜色がないことが明らかになった。2種類のランプを同時に点灯すると、それだけ電力を消費する。消費電力の削減を目痣して、例えば、タングステンハロゲンランプ6を点灯し、消灯した瞬間にフラッシュランプ7を点灯することも可能である。この場合、数10kWの電力を消費するタングステンハロゲンランプ6を消灯した後であるが、消灯直後のために半導体基板31の温度はまだ保たれている。したがって、ランプ点灯のための電極が一つで済み、同時に消費電力の削減を計ることが可能となる。

【0039】強誘電体膜は、PZT膜に限らずSBT（$SrBiTa_2O_9$），BTO（$BaTiO_3$）など多くの材料が存在するが、本発明を実施することによりアルミニウム膜に変化を起こすことなく、これらの膜を結晶化させることが可能であることはいうまでもない。本発明は、半導体基板上に形成された強誘電体膜の結晶化方法に限るものではなく、チタン酸ストロンチウム（$SrTiO_3$ 、STOと略）、チタン酸ストロンチウム・バリウム（$Ba_xSr_{1-x}TiO_3$ ）の結晶化、Ta_2O_5 の結晶化などの下地に与える熱エネルギーを抑制しなければならないプロセスに幅広く応用することが可能である。

【0040】

【発明の効果】本発明によれば、半導体装置のコンタク

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ト部の製造を低温で且つ急速に制御性良く行うことができ、その結果メタルゲート電極や高誘電率ゲート絶縁膜、低誘電率層間絶縁膜に見られる耐熱性の低い新材料を半導体装置に容易に適用できるようになり素子特性の高性能化が実現可能になる。また、本発明を用いることによって、アルミニウム配線に熱的損傷を与えることなく、その上に強誘電体キャパシタを形成することができる。アルミニウム配線は何層形成されていても、その上で強誘電体キャパシタを形成することが可能になる。

【図面の簡単な説明】

【図１】本発明の半導体装置におけるコンタクト部の製造工程を示す断面図。

【図２】本発明及び比較例のサンプルにおけるコンタクト部の反応形態においてフラッシュランプの効果を示す組成図。

【図３】本発明及び比較例のサンプルにおけるコンタクト部の反応形態において基板温度の効果を示す組成図。

【図４】フラッシュランプを１回照射した時の低抵抗コンタクトを形成するために必要な基板温度とフラッシュランプの照射エネルギー密度との関係を示す特性図。

【図５】フラッシュランプを１０回照射した時の低抵抗コンタクトを形成するために必要な基板温度とフラッシュランプの照射エネルギー密度との関係を示す特性図。

【図６】下地金属膜に対するＳｉの添加量とコンタクト抵抗及び接合リーク電流との関係を示す特性図。

【図７】本発明のロジック素子が形成されたシリコン半導体基板の断面図。

【図８】図７のＡ領域の構造を示す断面図。

【図９】本発明の熱処理装置の概略断面図。

【図１０】本発明を説明するランプエネルギーと強誘電体膜の熱処理による温度の照射されるランプのエネルギー依存性を示す特性図。

【図１１】本発明を説明する結晶化温度と熱処理時間との関係を示す特性図。

【図１２】１トランジスタ・１キャパシタ構成の強誘電体メモリセルの等価回路図。

【図１３】本発明のＦＲＡＭが形成された半導体基板の断面図。

【図１４】本発明に適用されるＦＲＡＭ構造の半導体装置の製造工程図。

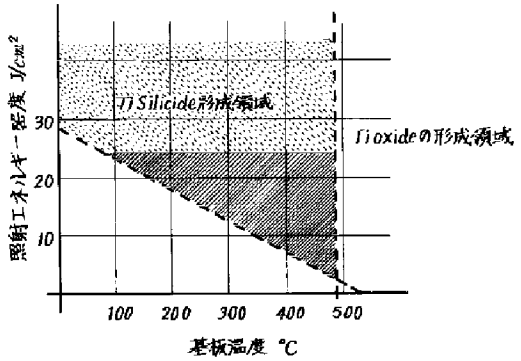
【図１５】本発明の強誘電体膜を誘電体とするキャパシタが形成された半導体基板の断面図。

【図１６】従来のＦＲＡＭ素子の断面図。

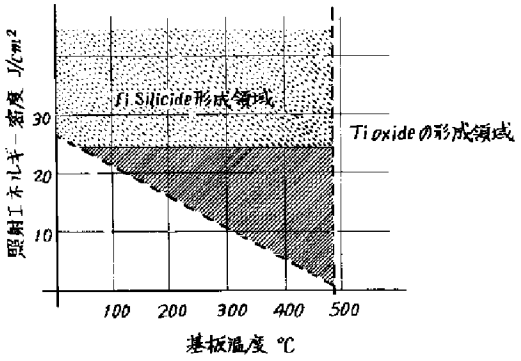
【符号の説明】

１・・・試料チャンバー、　２・・・試料台、　３・・・ガス導入口、４・・・排気口、　５・・・石英窓、６・・・第1のランプ（タングステンハロゲンランプ）、７・・・第2のランプ（フラッシュランプ）、８・・・試料、　９、１０・・・電源、　２０、３１・・・シリコン基板、２１、４７、５７・・・不純物拡散領域、　２２・・・ゲート酸化膜、２３、５０・・・ゲート電極、　２７・・・接続プラグ、２８・・・絶縁膜、　２９、２５１～２５４・・・金属配線、３２・・・熱酸化膜、　３３・・・アルミニウム膜、３４・・・シリコン酸化膜、　３５・・・金属チタン膜、３６・・・白金膜、　３７・・・チタン酸ジルコン酸鉛膜、４１、５１・・・シリコン半導体基板、　４２・・・SiO_2 膜、４３・・・コンタクト孔、　４４・・・イオン注入層、４５・・・金属膜、　４６・・・抵抗率の低い金属膜、４８・・・電極、　５２、２４１～２４５・・・層間絶縁膜、５３・・・素子分離領域、　５４・・・ゲート絶縁膜、５５・・・シリサイド層、　５６・・・シリコン窒化膜、５８・・・接続プラグ、　５９・・・金属配線、１０１、３０１・・・下部電極、　１０２、３０２・・・強誘電体膜、１０３、３０３・・・上部電極、　２４１～２４５・・・層間絶縁膜。

【図４】

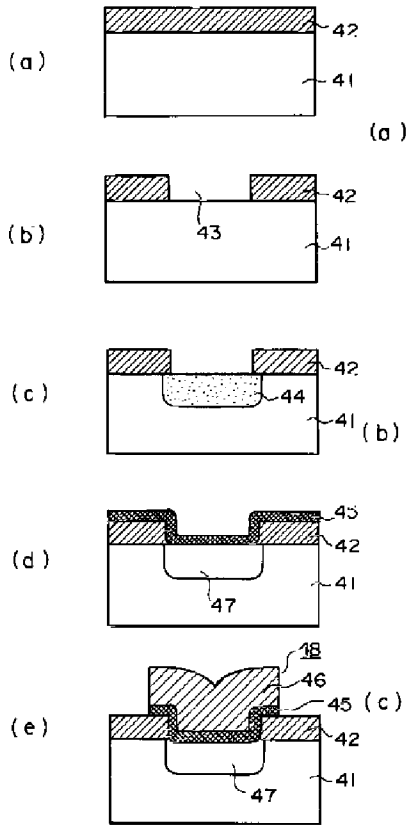


【図５】

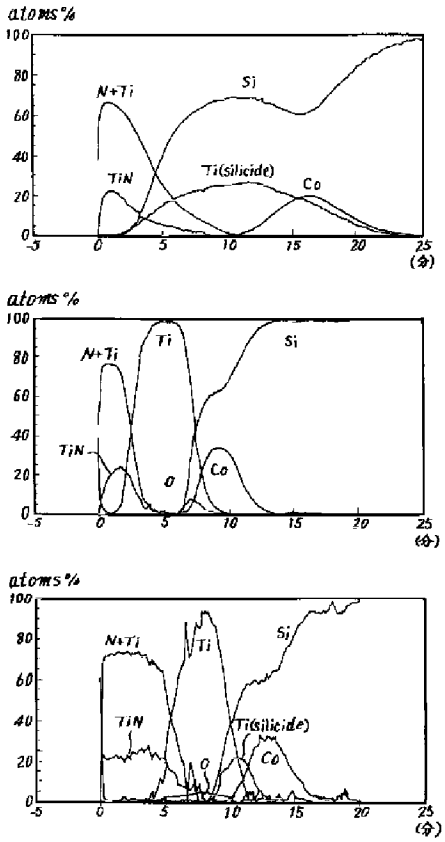


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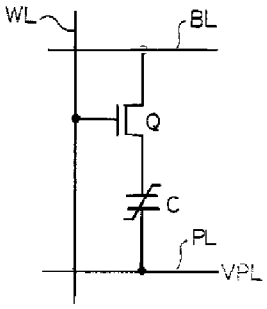
【図1】



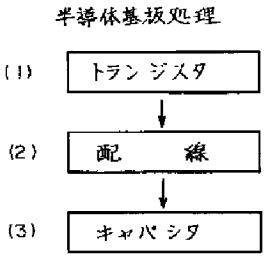
【図2】



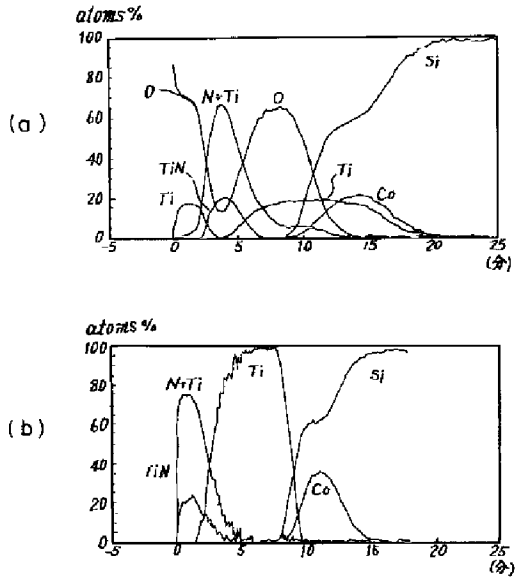
【図12】



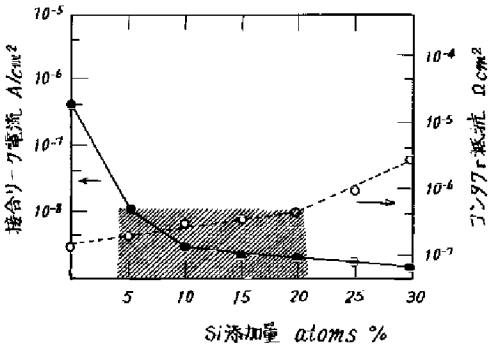
【図14】



【図3】

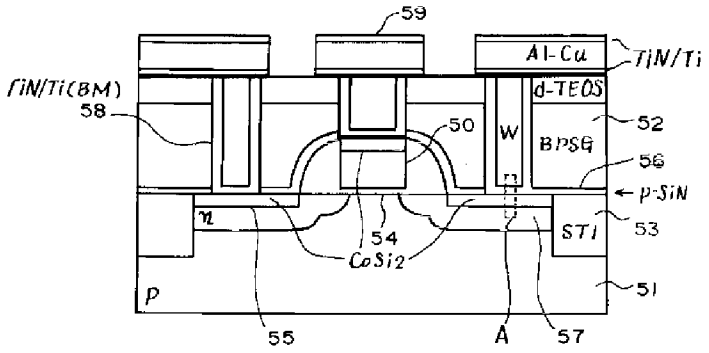


【図6】

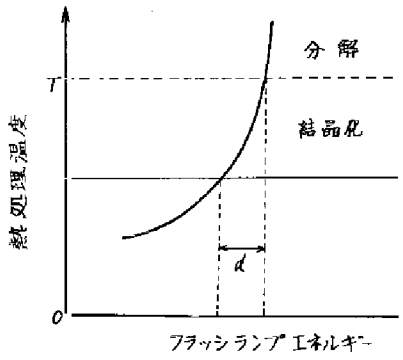


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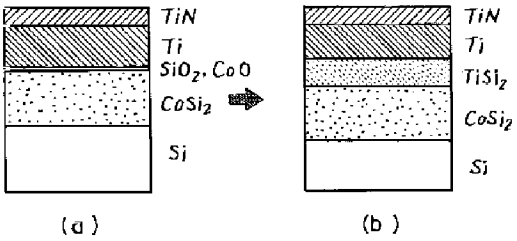
【図7】



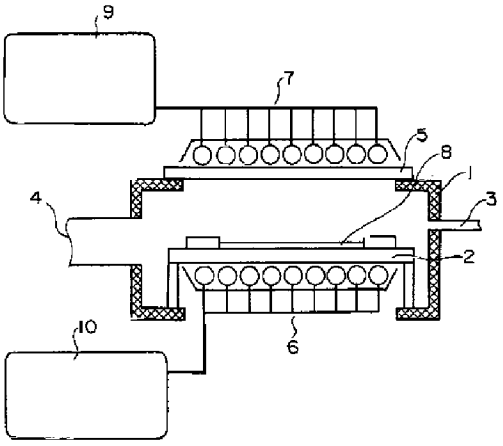
【図10】



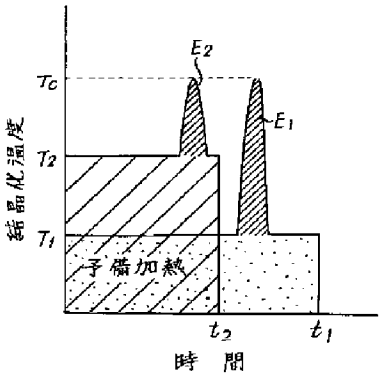
【図8】



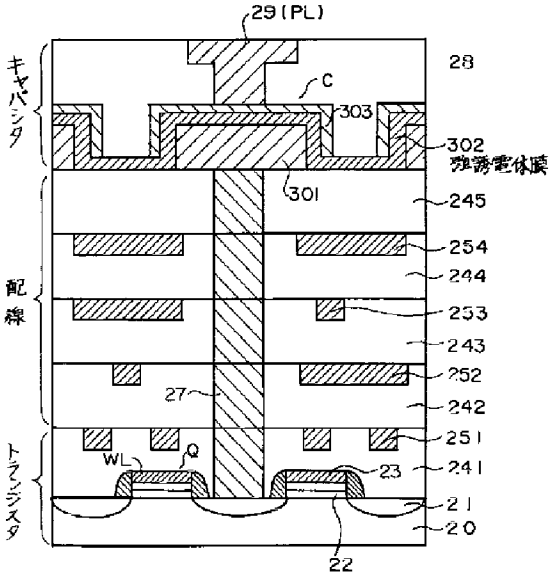
【図9】



【図11】

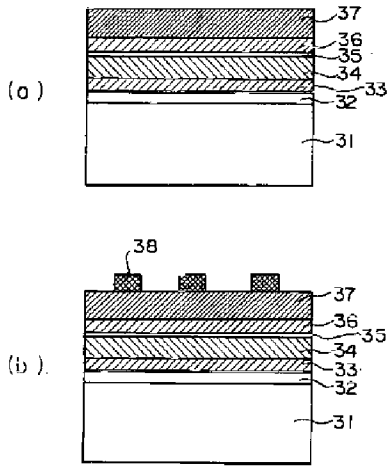


【図13】

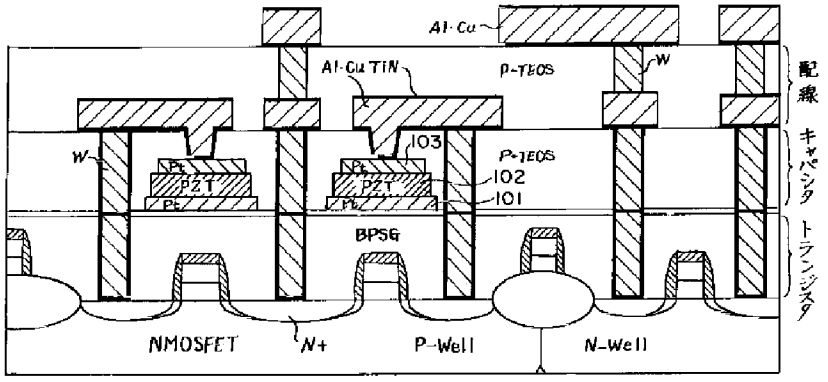


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【図15】



【図16】



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(72)発明者 須黒 恭一
神奈川県横浜市磯子区新杉田町8番地 株式会社東芝横浜事業所内
(72)発明者 有門 経敏
神奈川県横浜市磯子区新杉田町8番地 株式会社東芝横浜事業所内
(72)発明者 飯塚 佳男
神奈川県川崎市幸区小向東芝町1番地 株式会社東芝マイクロエレクトロニクスセンター内

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QQ73 QQ82 RR04 RR06 RR15
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JP2002151428A METHOD FOR HEAT TREATMENT AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Applicants: TOSHIBA CORP

Inventors: ARIKADO TSUNETOSHI,IINUMA TOSHIHIKO,IIZUKA YOSHIO,ITO TAKAYUKI,SUGURO KYOICHI

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Application: JP2002151428A·2000-11-13

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METHOD FOR HEAT TREATMENT AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To provide a method for heat treatment for implementing the formation of a high-quality ferroelectric film at a low temperature, such as 400 deg.C or about, the formation of a contact section having a high contactability at a low temperature, the formation of silicide rapidly at a low temperature, or the like. SOLUTION: This method for heat treatment comprises at least two kinds of lamps. The first lamp (halogen lamp or the like) 6 is lighted up to heat a sample (silicon wafer) 8. When the sample reaches a specified temperature, the second lamp (flash lamp) 7 is lighted up to further increase the temperature of the sample until the sample reaches a desired temperature. That is, this method for heat treatment comprises a process of heating the sample using at least two kinds of lamps which are lighted up at different times. In this method, a first source of heat and a second source of heat different in light emission wavelength distribution and radiation time are combined for the purpose of reducing a thermal budget in a contact process, so as to make interconnections, contact sections between electrodes and a semiconductor substrate or a conductor film, or the like rapidly react to reduce a contact resistance.

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DESCRIPTION JP2002151428

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor manufacturing apparatus and a semiconductor manufacturing process, and more particularly to a heat treatment apparatus and a heat treatment method for crystallizing a ferroelectric film or improving contact characteristics of a contact portion, and a semiconductor. The present invention relates to a method of manufacturing a device.

[0002]

2. Description of the Related Art In recent years, a ferroelectric memory (Ferroelectric RAM) has attracted attention. This is because it has a response speed almost equal to that of a DRAM and has a non-volatile characteristic that the memory is not erased. The characteristics are expected to be exhibited not only in general-purpose memories but also in system LSIs mounted together with logic devices. A cross section of the ferroelectric memory element is shown in FIG. As is clear from the figure, a transistor, a ferroelectric capacitor, and a wiring are formed in order from the bottom. In this ferroelectric memory element, the lower electrode 101 of the capacitor also serves as a plate line, and the upper electrode 103 is connected to the bit line with the ferroelectric film 102 interposed therebetween. The manufacturing process is, of course, such that the transistor is first made and then the ferroelectric capacitor is formed. Then, the connection hole is opened and an Al-Cu wiring is formed. Tungsten (W) is used for the connection wiring in the connection hole.

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[0003]

One of the difficulties in manufacturing a ferroelectric memory is that the ferroelectric is susceptible to process damage. When dry etching or sputtering is performed to form a multi-layer wiring, it is affected by charged particles in the plasma, and since these processes are performed under reduced pressure, lead zirconate titanate PZT (Pb (Tix. Oxygen is desorbed in the ferroelectric substance such as Zr1-x) O3) or strontium bismuth tantalate SBT (Sr2 BiTaO9), and the ferroelectricity is significantly impaired. As one contrivance for avoiding such a process damage in the multilayer wiring forming process, for example, in Japanese Patent Laid-Open No. 11-317500, a method of forming a multilayer wiring first and forming a ferroelectric capacitor on it is disclosed. Is proposed. Since the multilayer wiring is formed first and the ferroelectric capacitor is formed thereon, the ferroelectric is naturally not damaged by the process of the wiring forming process. The problem with this process is that the crystallization temperature of PZT or SBT, which is a ferroelectric substance, is higher than the temperature (450 ° C.) that aluminum wiring can withstand. The crystallization temperature of PZT is at least 550 ° C, while that of SBT requires at least 650 ° C. When heated to such a temperature, aluminum is melted and a problem such as disconnection of wiring occurs.

[0004]

In order to avoid such a problem, for example, a process of forming by CVD (Chemical Vapor Deposition) at a heat treatment temperature of about 450 ° C. has been studied, but a good ferroelectric performance is not realized at a low temperature. .. In order to obtain sufficient performance as a ferroelectric substance, it is still necessary to sufficiently crystallize at a high temperature. If the heating time is very short, the aluminum will not deteriorate and melt even if the temperature is high. For example, at 500 ° C, the aluminum does not deteriorate within a few seconds. Therefore, although RTP (Rapid Thermal Process) can be one of the means, if the current RTP is heated to, for example, 650 ° C, it takes a long time to reach 450 ° C or higher, so that the quality of aluminum changes. Will end up. Thus, at present, the solution cannot be found because of the gap between the crystallization that requires high temperature and the process below the temperature at which aluminum does not deteriorate.

[0005]

In addition, as the performance of a transistor is improved, the problem of depletion of the gate electrode is becoming apparent as the gate insulating film is thinned. Since the parasitic

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capacitance increases due to the presence of the gate electrode depletion layer, the effective oxide film thickness increases even if a very thin gate insulating film is formed. In order to solve this, it is extremely effective to use a metal gate electrode or a high dielectric constant gate insulating film. However, one of the problems faced by metal gates and high dielectric films is the lowering of the contact process temperature. Usually, since a natural oxide film exists on the surface of the Si substrate, it becomes a barrier layer and it is difficult to make contact with the metal. In recent years, a method of forming a contact portion of a semiconductor device is performed by depositing a metal conductive film as an electrode or an underlayer of the electrode in a contact hole which is patterned and opened in an interlayer insulating film, and then in an infrared heating furnace at 550 ° C. for 1 hour. The above heat treatment has been performed. The purpose of this heat treatment is to reduce the natural oxide film at the interface between the electrode and the semiconductor substrate to form a low resistance ohmic contact.

[0006]

However, conventional heat treatment conditions have a large thermal budget, Al, which is a metal having a low resistivity, has a low melting point, and Ta2O5, which is a high dielectric material, has an increased gate leakage current due to crystallization. It is not sufficient to be used as a gate electrode or a gate insulating film, respectively. In order to realize higher performance of the device characteristics, it is necessary to use a low dielectric constant material for the interlayer insulating film, but in the conventional thermal process, the mechanical strength and moisture absorption decrease with the decrease in density. Therefore, it becomes difficult to apply it to a transistor. However, it has been found that when the heat treatment temperature for forming the contact portion is lowered to 500 ° C. or less, both the contact resistance and the variation within the semiconductor substrate surface increase. This is because the natural oxide film on the surface of the silicon substrate cannot be sufficiently reduced by the heat treatment at 500 ° C. or less.

[0007]

As described above, as the performance of a transistor is improved, the problem of depletion of the gate electrode is becoming apparent as the gate insulating film is made thinner. Then, there is a problem that the contact portion is formed by the above-mentioned low thermal budget. Further, the method of forming the ferroelectric capacitor on the multi-layer wiring can avoid damage to the multi-layer wiring, but has a limitation that the ferroelectric must be crystallized at a temperature at which aluminum does not deteriorate as described above. The present invention has been made in view of the above circumstances, and is to form a good-quality ferroelectric

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film at a low temperature of about 400 ° C., to form a contact portion having a high contact property at a low temperature, and to rapidly form a contact portion at a low temperature. Provided are a heat treatment method for performing silicide formation and the like, and a semiconductor device manufacturing method using the heat treatment method.

[0008]

The present invention comprises at least two or more kinds of lamps. First, the first lamp is turned on to heat the sample, and when the temperature reaches a certain level, the second lamp is turned on. However, the temperature of the sample is further raised to reach a desired temperature. In the case of the conventional RTP, one kind of lamp heats up to a desired temperature. For example, if the heat treatment temperature is 700 ° C, heating is performed up to 700 ° C with one type of lamp. Assuming that the temperature is raised at a standard RTP performance of 50 ° C./sec, it takes 14 seconds to reach 700 ° C. Even if the treatment time is set to zero and the temperature is immediately lowered, it takes 20 seconds or more to lower the temperature. The total heat treatment time is over 30 seconds. When the sample is a semiconductor substrate, aluminum wiring is formed on it, and the ferroelectric film formed via the interlayer insulating film is heat-treated by crystallization, 450 ° C, which is a dangerous temperature for aluminum, is used. The time for heating above reaches 10 seconds or more, and the aluminum wiring is melted. Aluminum does not deteriorate for 1 hour even if it is heated at 450 ° C. At 500 ° C, heating can be continued for about 10 to 15 seconds. At 550 ° C, heating can be continued for about 5 to 6 seconds.

[0009]

Furthermore, at 600 ° C, the quality changes in 1-2 seconds. Aluminum melts at 660 ° C. However, even if the temperature is lower than the melting temperature, if the heating time exceeds the above-mentioned range, the quality is deteriorated. Such alteration refers to a state in which aluminum particles in the aluminum wiring grow to cause hillocks. The reason why it is necessary to perform the preheating using the first lamp is as follows. That is, the thermal energy applied by the second lamp is limited to some extent. In some cases, a large amount of heat energy may be required to heat the sample surface with only a flash lamp having a very short irradiation time. In such a case, even if the ferroelectric substance can be crystallized as intended, the applied energy is conducted to the lower layer, and since the total amount of energy is large, the temperature of aluminum rises. The thermal energy input at the second lamp must be adjusted so that only the ferroelectric is heated and to the extent necessary for crystallization. Therefore, it is important to preheat to some extent.

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[0010]

FIG. 10 is a characteristic diagram showing the energy dependence of the lamp to be irradiated with the lamp energy and the temperature due to the heat treatment of the ferroelectric film. As shown in the figure, the ferroelectric film begins to crystallize at a predetermined temperature and decomposes at a higher temperature T. Then, the required energy corresponding to each is obtained from the energy curve shown in the figure. The energy required for crystallization lies within the energy width d. FIG. 11 is a characteristic diagram showing the relationship between the crystallization temperature and the heat treatment time when carrying out the present invention. In the present invention, the ferroelectric film is preheated to a predetermined temperature (T1 or T2) by the first lamp, and then the second lamp capable of raising the temperature in a short time, for example, 1000 The temperature is raised to the crystallization temperature (Tc) within a short time of about one second. The amount of energy provided by the second lamp depends on the preheating temperature. When it is desired to reduce the energy amount of the second lamp (for example, E2), it is preferable to increase the preheating temperature (for example, T2) and shorten the preheating time (for example, t2). When the flash lamp is used as the second lamp and the energy amount is set to 27 joules (J) / cm2 or less, the aluminum wiring formed in the lower layer of the ferroelectric film is not melted and damaged. For example, in the case of crystallizing a PZT ferroelectric film, if the preheating temperature is set to 400 ° C, the energy of the flash lamp is crystallized at 10 J / cm 2 or more.

[0011]

When the preheating is set at 550 ° C, the flash lamp is crystallized at an energy of 7 to 8 J / cm 2. When the preheating temperature is high as described above, the preheating temperature of the first lamp can be set to 1 second or less. It is also possible to embed a heater in the sample stage without using a lamp and perform preheating using this heater. However, in this case, since the sample is placed on the heated heater, the pre-heating time before and after the original crystallization takes several tens of seconds. This method is also possible as long as the preheating temperature is a temperature at which aluminum has no problem. However, depending on the amount of heat energy applied by the second lamp, preheating at about 500 ° C. may be necessary. In that case, considering the deterioration of aluminum, the preheating time must be shortened to seconds. Therefore, it is necessary to perform preheating with a lamp. The method of preheating with a lamp has a wide range of applicability in that it can be used in various cases.

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[0012]

Further, the present invention is characterized in that a first heating source and a second heating source having different emission wavelength distributions and irradiation times are combined for the purpose of reducing the thermal budget of the contact process. The contact resistance can be reduced by rapidly reacting the contact portion between the wiring or electrode and the semiconductor substrate or the conductor film. Further, it is characterized in that a silicide is formed by combining a first heating source and a second heating source having different emission wavelength distributions and irradiation times. Since silicide formation can be performed rapidly at low temperature, it is easy to apply new materials such as metal gates with low heat resistance, high-dielectric-constant gate insulating films, and low-dielectric-constant interlayer insulating films to transistors. Higher performance can be realized. That is, the heat treatment method of the present invention comprises a step of heating at least two types of lamps having different lighting times when heat-treating the sample, and the first type when heat-treating the sample. The lamp is turned on, and subsequently, the lamp of the second type, which is a flash lamp, is turned on to heat the sample while the lamp of the first type is turned on.

[0013]

A method of manufacturing a semiconductor device according to the present invention includes a step of forming an insulating film on a semiconductor substrate, and forming a contact hole in the insulating film to expose the semiconductor substrate or a conductor film formed on the semiconductor substrate, A step of depositing a wiring or a conductive electrode connected to the semiconductor substrate surface exposed from the contact hole or the conductor film to form a contact portion; and heat treating the semiconductor substrate to form the semiconductor substrate surface or the A step of improving the contact property of the contact portion between the conductor film and the wiring or the conductive electrode, and in the step of heat-treating the semiconductor substrate, two heating sources having different emission wavelength distributions and irradiation times are used. The first heating source is irradiated, and the second heating source is irradiated for a time shorter than the irradiation time of the first heating source before the heat treatment temperature is lowered during the irradiation or after the irradiation is stopped. The wiring or the conductive electrode may be a metal film capable of reducing an oxide film formed on the surface of the semiconductor substrate or the surface of the conductor film. The metal film capable of reducing the oxide film is generated by heat generated during the formation of the oxide film and at the time of forming a compound with an element forming the semiconductor substrate or the conductor film as a base, the surface of the semiconductor

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substrate or the conductor. The heat of formation of the oxide film formed on the surface of the film may be negatively larger.

[0014]

The metal film capable of reducing the oxide film may contain 5 to 20 wt% of silicon. The heating source may include the first heating source having an emission wavelength in the infrared region and a second heating source having an emission wavelength on a shorter wavelength side. At least a part of the emission wavelength range of the second heating source may be in the ultraviolet range. The second heating source may be a flash lamp. The temperature of the semiconductor substrate by the first heating source is lower than the temperature at which characteristic deterioration of the insulating film, the conductor film, the wiring, and the conductive electrode is not induced, and the second heating source has a low load. The irradiation energy density may be set so that the reaction of the contact portion is promoted therein.

[0015]

Further, a method of manufacturing a semiconductor device of the present invention comprises a step of forming at least one layer of aluminum wiring on a semiconductor substrate having a semiconductor element formed thereon via an interlayer insulating film, and a step of forming an interlayer insulating film on the aluminum wiring. Then, a step of sequentially depositing a lower electrode, a ferroelectric film and an upper electrode by a sputtering method, and heat treating the semiconductor substrate to crystallize the ferroelectric film to form the lower electrode, the ferroelectric film and the A step of forming a capacitor composed of an upper electrode, wherein in the step of heat treating the semiconductor substrate, at least two kinds of lamps having different lighting times are used, and the first kind of lamp is lit It is characterized in that the flash lamp, which is the second type of lamp, is lit for a shorter time than the lighting time of the first type of lamp before the heat treatment temperature is lowered. A semiconductor device formed by the manufacturing method of the present invention includes a semiconductor substrate, a source / drain region formed in the semiconductor substrate, and a semiconductor device formed on the semiconductor substrate, at least between regions facing the source / drain region. A gate insulating film formed on the gate insulating film, a gate electrode formed on the gate insulating film, and a cobalt silicide surface layer formed on at least the surface of the source / drain region.

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[0016]

BEST MODE FOR CARRYING OUT THE INVENTION Embodiments of the present invention will be described below with reference to the drawings. First, the heat treatment apparatus of the present invention will be described with reference to the schematic sectional view shown in FIG. This heat treatment apparatus has a sample chamber 1 made of aluminum. Inside the sample chamber 1, a sample table 2 on which a sample is placed, a gas inlet 3 for introducing a gas, an exhaust port 4 for exhausting gas, and an inlet for light are introduced. A quartz window 5 at the top for heating, a rod-shaped lamp (first lamp) 6 for preheating the sample, and a flash lamp (second lamp) 7 are provided. Sixteen rod-shaped lamps 6 are 3 kW tungsten halogen lamps and are installed under the sample 8 to heat the sample 8 from below. On the other hand, the flash lamp 7 is also a rod-shaped lamp, and 15 lamps are installed on the sample 8 to heat the sample 8 from above. Both of the lamps are connected to dedicated power supplies 9 and 10, respectively. The timing of lighting the lamp, the lighting time, and the number of times the flash lamp is lit are configured to be controlled by the microcomputer. It is not essential that the two types of lamps are rod-shaped lamps, and the same effect can be expected in a type of lamp that is provided with two external terminals in one direction, which is called a single end in the field of lamps. it can.

[0017]

Next, a first embodiment will be described with reference to FIGS. 1A to 1D are cross-sectional views of a manufacturing process illustrating a method of forming a contact portion between a semiconductor substrate and a wiring. First, as shown in FIG. 1A, a 200 nm SiO2 film 42 is deposited on a single crystal silicon substrate 41 by a CVD (Chemical Vapor Deposition) method. Next, as shown in FIG. 1B, the SiO2 film 42 is patterned to form contact holes 43 of 0.3 .mu.m.times.0.3 .mu.m. Then, using the SiO2 film 42 as a mask, boron (B) is ion-implanted into the silicon semiconductor substrate 41 at an acceleration energy of 10 keV and a dose of 5.times.10@15 cm @ -2. As a result, as shown in FIG. 1C, the ion implantation layer 44 is formed. Here, not only the p-type layer forming impurities but also an n-type conductive layer formed by ion implantation of P, As, etc. may be formed on the surface of the silicon semiconductor substrate 41. Then, heat treatment is performed at 1000 ° C. for 10 seconds in a nitrogen atmosphere of an infrared lamp heating furnace (RTA). As a result, as shown in FIG. 1D, the ion implantation layer 44 is crystallized and the impurities are activated, so that the ion implantation layer 44 is a p-type impurity used for the source / drain regions. It becomes the diffusion region 47. Next, a metal film 45 having a thickness of 30 nm or less is deposited on the silicon semiconductor substrate 41 including the impurity diffusion region 47. As the metal film 45, a metal capable of reducing the natural oxide film on the silicon semiconductor substrate, for

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example, Ti is desirable.

[0018]

Other suitable metals for this include IIIa, IVa, and Va refractory metals. Then, the silicon semiconductor substrate 1 is heated to 400 ° C. in an infrared heating furnace in a nitrogen atmosphere, and one pulse of an Xe flash lamp having an energy density of 10 J / cm −2 and a pulse width of 1 msec is irradiated during the heating. As a result, ohmic contact was formed between the metal film 5 and the underlying silicon semiconductor substrate 41. Next, as shown in FIG. 1E, a metal film 46 having a low resistivity, for example, Al is deposited to a film thickness of about 400 nm, and then patterned according to the contact hole 43 to form an electrode 48. The heat treatment conditions of the infrared heating furnace for forming the contact portion of the semiconductor device according to the present invention are set so as not to be treated at a temperature of 500 ° C. or higher for a long time. The contact resistance between the Al electrode and the impurity diffusion layer of the sample S1 of this example formed by the above method was measured and found to be 1.3 × 10 −7 Ωcm 2.

[0019]

In order to investigate the effect of reducing the contact resistance in the example, only the substrate heating at 400 ° C. is performed without irradiating the flash lamp, and the sample S2 having the same structure as in FIG. 1E is formed as a comparative example. When the contact resistance of the sample S2 of the comparative example was measured, it was 5.3.times.10@-4 .OMEGA.cm @ 2. Furthermore, when the contact resistance of the sample S3 having the same structure as that shown in FIG. 1 (e), which was produced under the heat treatment condition of 550 ° C. for 90 minutes only in the conventional infrared heating furnace, was measured, it was 2.5 × 10 −7 Ωcm 2. It was From the above results, it can be seen that the contact resistance of the sample S1 of the example is significantly lower than that of the sample S2 of the comparative example, and is lower than that of the sample S3 of the conventional example.

[0020]

Next, in the sample S1 of the example, the sample S2 of the comparative example, and the sample S3 of the conventional example, the diffusion behavior and reaction morphology of the element in the contact portion between the metal wiring and the silicon semiconductor substrate are

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examined by Auger spectroscopy. The result is shown in FIG. FIG. 2 is a composition diagram for explaining the effect of the flash lamp in the reaction mode of the contact portion of the semiconductor device of the present invention, the comparative example, and the conventional semiconductor device, in which the vertical axis represents the composition ratio of elements (atom%) and the horizontal axis represents Ar ions. It represents the sputtering time (minutes). That is, the horizontal axis corresponds to the depth direction. 2A shows an example sample S1, FIG. 2B shows a comparative example sample S2, and FIG. 2C shows a conventional example sample S3. Here, as a method of further lowering the contact resistance, a conductor film CoSi2 layer is provided on the surface of the silicon semiconductor substrate, and the state of reaction between the metal film Ti and the CoSi2 layer is shown.

[0021]

As shown in FIG. 2, in the sample S2 of the comparative example, oxygen was detected at the Ti / CoSi2 interface, and it was found that a natural oxide film (SiO2, CoO) of an insulator was present on CoSi2. On the other hand, in the sample S1 of the example and the sample S3 of the conventional example, it can be seen that the natural oxide film was not detected on the CoSi2 and was reduced by the metal film Ti. Further, it was found that mutual diffusion of Ti and the underlying silicon semiconductor substrate occurred, forming a Ti silicide layer. By the way, in the comparative sample S2, it was not possible to confirm the formation of the Ti silicide layer even when the heat treatment time was continued for 90 minutes or longer. From the above results, it is considered that the reduction reaction of the natural oxide film existing on the surface of the silicon semiconductor substrate and the formation of the silicide layer by the metal film hold the key to the formation of the low resistance contact. It is considered that the contact resistance could not be reduced because the low-temperature heat treatment did not completely reduce the natural oxide film on the surface of the silicon semiconductor substrate by Ti, which was the metal film, and the formation of the Ti silicide layer was suppressed. The effect of the Xe flash lamp in this example is that the energy which cannot be reached by the infrared heating furnace can be obtained in an extremely short time by utilizing not only heat but also light energy, so that the metal film and the underlying silicon are used. High-speed reaction with the semiconductor substrate is possible, and contact resistance can be reduced with a low thermal budget.

[0022]

The present invention is not limited to the above embodiment. For the two heating sources for forming the contact portion of the semiconductor device, it is sufficient if the heating source has

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an emission wavelength in the infrared region and at least a part of the emission wavelength in the ultraviolet region on the shorter wavelength side than that. It is also possible to apply a laser such as Ar, N2 or excimer, or a hydrogen lamp.

[0023]

Next, a second embodiment will be described with reference to FIGS. FIG. 3 is a composition diagram for explaining the effect of the flash lamp in the reaction mode of the contact portion of the comparative sample S4, in which the vertical axis represents the composition ratio of elements (atom%) and the horizontal axis represents the Ar ion sputtering time (minutes). It represents. That is, the horizontal axis corresponds to the depth direction. A semiconductor device is manufactured according to the first embodiment described above. However, the heat treatment conditions for forming the contact portion between the metal wiring and the silicon semiconductor substrate in this embodiment are that the substrate temperature is 100 to 480 ° C. and the irradiation energy density of the Xe flash lamp is 5 to 25 J / cm 2. Set to. That is, in this embodiment, the substrate temperature by the first heating source is set to a temperature at which the refractory metal film, here the Ti layer, is not affected by the atmosphere during the heat treatment and does not induce deterioration as element characteristics, In the second heating source, the irradiation energy is set so that the reaction of the contact portion can be promoted within the low load of the light source body. In order to investigate the reaction effect of the contact portion in the example, a sample S4 in which the substrate temperature was set to 500 ° C. and the irradiation energy density of the Xe flash lamp was set to 10 J / cm 2 was prepared as a comparative example.

[0024]

The contact resistance between the Al electrode and the impurity diffusion layer of the sample S4 of the comparative example was actually measured and found to be 7.2×10^{-3} Ωcm 2. From the above results, it was found that the contact resistance of the comparative sample S4 increased rather than the contact resistance of the sample S1 of the first embodiment. FIG. 3A shows the result of examining the reaction morphology of the contact portion from Auger spectroscopic analysis for the sample S4 of the comparative example. In the comparative sample S4, a considerable amount of oxygen was taken into the Ti layer, not only the Ti oxide film of about 15 nm was present on the outermost surface, but also the thickness of the Ti silicide layer was reduced. I understand. This suggests that the higher the substrate temperature, the more easily it is affected by the atmosphere, and the amount of oxygen invading from the substrate surface side increases, so that the growth rate of the Ti silicide layer is limited. That is, it is

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considered that in the comparative sample S4, the contact resistance was increased due to the fact that the metal film Ti was oxidized to become an insulator and the growth of Ti silicide was suppressed.

[0025]

Therefore, with the substrate temperature of the silicon semiconductor substrate kept at room temperature, a sample S5 having the structure shown in FIG. 1 (e) is produced using only a Xe flash lamp (irradiation energy: 10 J / cm2). The contact resistance of the sample S5 at this time was 3.1.times.10@-5 .OMEGA.cm @ 2, which was remarkably higher than that of the sample of the example. FIG. 3B shows the result of examining the reaction morphology of the contact portion from Auger spectroscopic analysis for sample S5. From the above results, in order to prevent the oxidation reaction of the Ti layer, even if the substrate temperature by the first heating source is set too low, only the Xe flash lamp which is the second heating source forms a low resistance contact. Turns out to be difficult. It is expected that an irradiation energy density of 30 J / cm 2 or more will be required to form a metal silicide layer only by Xe flash lamp irradiation. However, as the irradiation energy density increases, the amount of metal silicide produced is controlled. However, it is not practical from the viewpoint of flash lamp load.

[0026]

FIG. 4 shows the substrate temperature by the first heating source and the Xe flash lamp (pulse by the second heating source) necessary for forming a Ti silicide layer at the contact portion with a low thermal budget and forming a low resistance ohmic contact. It shows the relationship with the irradiation energy density (when the width is 1 msec). In the figure, the shaded region shows the conditions under which a low resistance contact of 5×10^{-7} Ωcm 2 or less can be formed within the range in which the life of the Xe flash lamp is taken into consideration. It can be seen that as the substrate temperature is increased up to around 480 ° C., a low resistance contact of 5×10^{-7} Ωcm 2 or less can be obtained by flash irradiation with low energy density. FIG. 5 illustrates a case where the Xe flash lamp is irradiated 10 times. It is understood that the conditions under which a low resistance contact of 5×10^{-7} Ωcm 2 or less can be obtained expands to low temperature and low irradiation energy side when the number of irradiation is increased. From the above, the heat treatment conditions for forming the contact portion between the metal wiring and the silicon semiconductor substrate are set such that the substrate temperature is 100 to 480 ° C. and the irradiation energy density of the Xe flash lamp is within the range of 5 to 25 J / cm 2. Is appropriate.

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[0027]

Next, a third embodiment will be described with reference to FIG. In this embodiment, a semiconductor device is manufactured according to the first embodiment. However, as the electrode underlayer for forming the contact portion between the metal wiring and the silicon semiconductor substrate in this embodiment, a metal conductive film to which 5 to 20% of Si is added is deposited. A metal conductive film of Ti-10% Si was deposited on the contact bottom, and then a Xe flash lamp was irradiated with one pulse at an energy density of 10 J / cm 2 at a substrate temperature of a silicon semiconductor substrate of 400 ° C., as shown in FIG. A sample S6 having the structure shown in FIG. That is, the feature of the present invention is that, before depositing the refractory metal film on the contact bottom, Si for forming the metal silicide layer at the contact interface is contained in advance in the refractory metal film to prevent the heat treatment. It is intended to reduce the junction leakage current by suppressing the forward diffusion amount to the silicon surface side of the silicon semiconductor substrate which is the underlying substrate and suppressing the silicidation reaction.

[0028]

In order to investigate the effect of reducing the junction leakage current of the sample S6 in this example, the thermal process of the contact process was the same as that of the sample S6 of the example, but the sample S1 in which the metal film Ti without Si was used as the electrode underlayer was used. A comparative experiment is performed using. In the sample S6 of the example, the junction leak current when a reverse bias voltage of 5 V was applied was measured and found to be 3.5 × 10 −9 A / cm 2. The contact resistance between the Al electrode and the impurity diffusion layer was 3.6 × 10 -7 Ωcm 2. On the other hand, in the sample S1 of the comparative example (the example sample in the first example), the junction leak current was measured and found to be 5.1 × 10 −7 A / cm 2 (contact resistance: 1.3 × 10 −7 Ωcm 2). there were. Further, the junction leakage current of the conventional sample S3, which was subjected to the heat treatment at 550 ° C. for 90 minutes without using the second heating source, was 2.6 × 10 −9 A / cm 2 (contact resistance : 2.5 × 10 −7 Ωcm 2). From this, the junction leak current of the example sample S6 is the same as that of the conventional sample S3, and an increase in contact resistance is observed when compared with the sample S1 of the comparative example, but the junction leak current is increased. It can be seen that the leak current is reduced by almost two digits and can be improved very effectively.

[0029]

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The method of forming the contact portion in which the second heating source is combined has a remarkable effect in reducing the contact resistance due to the fact that the metal silicide layer can be formed thick, but on the other hand, the method of forming the contact portion on the metal film side of the underlying silicon semiconductor substrate is improved. It is considered that since the amount of forward diffusion was large and vacancies were formed in the silicon semiconductor substrate, and the vacancies were included in the depletion layer when the reverse bias was applied, the junction leak current was increased. Therefore, by adding Si in advance before depositing the metal film, the amount of diffusion of Si from the underlying silicon semiconductor substrate due to the heat treatment can be suppressed, and the metal silicide layer can be formed while controlling the silicidation reaction. It is considered that the junction leakage current was improved because of this. FIG. 6 shows the relationship between the contact resistance and the junction leakage current (when 5 V is applied) with respect to the amount of Si added to Ti when the Xe flash lamp is irradiated with one pulse at an irradiation energy density of 10 J / cm 2 at a substrate temperature of 400 ° C. It is a characteristic view showing. It can be seen that the contact resistance increases as the amount of Si added increases, but the junction leakage current decreases. It is shown that the range of the amount of Si added that can satisfy the specifications from both aspects of contact resistance and junction leakage current is 5 to 20%.

[0030]

As described above, it is effective to add 5 to 20% of Si to the metal conductive film as the electrode underlayer for forming the contact portion having the good contact property between the metal wiring and the silicon semiconductor substrate. .. Next, a fourth embodiment will be described with reference to FIGS. 7 and 8. In this embodiment, the present invention is applied to the manufacture of the contact portion between the impurity diffusion region of the logic element and the connection plug. A MOS transistor is formed in the element region surrounded by the element isolation region (STI) 53 of the p-type silicon semiconductor substrate 51. The MOS transistor is formed on an n-type impurity diffusion region 57 forming a source / drain region, a gate insulating film 54 made of a silicon oxide film formed between the impurity diffusion regions 57, and the gate insulating film 54. A gate electrode 50 made of polysilicon or the like and protected by the sidewall insulating film is formed. A cobalt silicide (CoSi2) layer 55 is formed on the surfaces of the gate electrode 50 and the impurity diffusion region 57 to reduce the resistance. A silicon nitride film 56 formed by plasma CVD is formed on the surface of the semiconductor substrate 51. An interlayer insulating film 52 made of a BPSG film and a TEOS film thereon is formed on the silicon nitride film 56.

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[0031]

The surface of the interlayer insulating film 52 is flattened, and a metal wiring 59 composed of a TiN / Ti barrier metal layer and an Al—Cu metal film sandwiched between the barrier metal layers is formed. The metal wiring 59, the gate electrode 50 of the MOS transistor, and the impurity diffusion region 57 are electrically connected by the connection plug 58 embedded in the contact hole formed in the interlayer insulating film 52. The connection plug 58 is composed of a TiN / Ti barrier metal layer formed on the inner wall of the contact hole and tungsten (W) wrapped in this barrier metal layer. The connection plug 58 is connected to the silicide layer 55. The contact portion is shown in the area A shown in FIG. The silicide layer is formed by depositing a cobalt film on the polysilicon of the gate electrode 50 and on the impurity diffusion region 57 by sputtering or the like, and heat-treating it to silicify it. However, the contact structure shown in the region A has a high resistance because the SiO2 and CoO layers are formed (FIG. 8 (a)). Therefore, normally, after forming the barrier metal layer of the connection plug, it is annealed at 550 ° C. for 90 minutes to eliminate the SiO 2 and CoO layers to reduce the resistance (FIG. 8B). In this embodiment, the semiconductor substrate is heated at 400 ° C. by infrared heating without annealing under such conditions, and one Xe flash lamp having an energy density of 10 J / cm 2 and a pulse width of 1 msec is irradiated during the heating. As a result, the structure of the area A shown in FIG. 8B, which is the same as the conventional structure, can be obtained at a low temperature of 400 ° C.

[0032]

Next, a fifth embodiment will be described with reference to FIGS. FIG. 12 shows an equivalent circuit of a ferroelectric memory cell having a one-transistor / one-capacitor configuration, which has the same circuit connection as the equivalent circuit of a DRAM cell. FIG. 13 is a cross-sectional view of the semiconductor substrate on which the FRAM is formed. The conventional semiconductor substrate on which the FRAM is formed has a structure in which the ferroelectric capacitor is formed on the transistor and the multilayer wiring is formed thereon. In this embodiment, the multilayer wiring is formed on the transistor as a sample to be heat-treated. Is used, and a semiconductor substrate having a structure in which a ferroelectric capacitor is formed on a multilayer wiring is used. FIG. 14 is a flow chart for explaining a manufacturing process of a semiconductor device having an FRAM structure to which the present invention is applied. First, a MOS transistor used for a memory or the like is formed on a wafer (1), and then aluminum or metal wiring containing aluminum as a main component is formed in a multilayer structure with an interlayer insulating film interposed (2). Then, a capacitor having a ferroelectric film is formed via an interlayer insulating film (3). This semiconductor device is characterized in

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that the positions of the capacitors are vertically interchanged as compared with those of the FRAM structure shown in FIG.

[0033]

C is a capacitor for information recording using a ferroelectric having a perovskite structure as an interelectrode insulating film, Q is a charge transfer MOS transistor connected in series to this capacitor, and WL is connected to the gate of this MOS transistor. Is a word line, BL is a bit line PL connected to one of source / drain regions of a MOS transistor, a plate line is connected to one end (plate) of the capacitor, and VPL is a plate line voltage. FIG. 13 is a cross-sectional view of an FRAM including a capacitor having a ferroelectric film having a ferroelectric characteristic. On a semiconductor substrate 20 made of a p-type silicon semiconductor or the like, an element isolation region made of SiO2 is formed by the LOCOS method. N-type impurity diffusion regions 21 used as source / drain regions are formed in the surface region of the semiconductor substrate 20. A gate electrode 23 is formed above the source / drain region via a gate oxide film (SiO2) 22. The gate electrode 23 connected to the word line (WL) is composed of a polysilicon film and a tungsten silicide film on the polysilicon film, and the upper surface is protected by the silicon nitride film. The semiconductor substrate 20 is covered with a first insulating film 241 made of a BPSG (Born Phospharus Silicate Glass) film used as an interlayer insulating film formed by the low pressure CVD method so as to cover the gate electrode 23. The first insulating film 241 is polished and planarized by CMP (Chemical Mechanical Polishing) or the like.

[0034]

In the first interlayer insulating film 241, a metal wiring 251 such as aluminum with a barrier metal layer interposed is embedded and formed. Second to fourth interlayer insulating films 242 to 244 are formed on the first interlayer insulating film 241. The second to fourth interlayer insulating films 242 to 244 are formed of silicon oxide films in which the second to fourth metal wirings 252 to 254 are embedded. A fifth interlayer insulating film 245 is deposited on the fourth interlayer insulating film 244. A ferroelectric capacitor C is formed on the fifth interlayer insulating film 245. The capacitor C is composed of a laminated body which is in contact with the interlayer insulating film 245 and in which a lower electrode 301, a ferroelectric film 302 such as PZT having ferroelectric characteristics, and an upper electrode 303 connected to a plate line (PL) are sequentially deposited. Has been done. Contact holes are formed in the first to fifth interlayer insulating films 241 to 245, and a connection plug 27 made of tungsten or the like is embedded therein. The connection plug 27 includes the lower electrode 301 and the source / drain regions of the MOS transistor Q. Is electrically connected to one side. The other of the

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source / drain regions is connected to a bit line (BL) (not shown).

[0035]

The lower electrode 301 is composed of a Ti film in contact with the interlayer insulating film 245 and a Pt film formed on the Ti film. The upper electrode 303 is composed of a Pt film. The insulating film 28 in which the insulating film 28 is formed on the interlayer insulating film 245 so as to cover the capacitor C is made of a TEOS film (SiO2 film) or the like. The insulating film 28 is planarized by CMP or the like. A contact hole and a wiring groove are formed in the insulating film 28 by etching, and a metal wiring (PL) 29 such as aluminum is embedded therein. In the FRAM described above, the capacitor ferroelectric film is formed by applying the crystallization method of the present invention. That is, a ferroelectric film such as PZT or SROP is formed in an amorphous state, and then it is crystallized by heat treatment to form a film used as a capacitor dielectric.

[0036]

Next, a sixth embodiment will be described with reference to FIG. FIG. 15 is a cross-sectional view of a semiconductor substrate on which a capacitor having a ferroelectric film as a dielectric is formed. The p-type (100) silicon semiconductor substrate 31 is put in a heating furnace and heated to 850 ° C. in an oxygen atmosphere to form a thermal oxide film 32 having a film thickness of 100 nm. An aluminum (Al) film 33 having a thickness of about 400 nm is deposited thereon by sputtering using argon gas. A silicon oxide film 34 having a thickness of about 500 nm is deposited on this by a plasma CVD method using SiH4 and N2 O gas. On this semiconductor substrate 31, a metallic titanium (Ti) film 35 and a platinum (Pt) 36 are further deposited by sputtering to have film thicknesses of 30 nm and 100 nm, respectively. Next, using a sputtering apparatus again, a lead zirconate titanate (PbZrx Ti1-x O3, hereinafter referred to as PZT) film 37 is deposited to a film thickness of about 150 nm. The gas used for sputtering at this time is argon gas, and the substrate temperature during sputtering is room temperature.

[0037]

This semiconductor substrate 31 is put into the heat treatment apparatus shown in FIG. 9 and crystallized while introducing oxygen. In this step, first, 3 kW was put into the tungsten halogen lamp (first lamp) 6 from below in order to preheat the semiconductor substrate 31, and the

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temperature was raised at a rate of 80 ° C. for 1 second. The flash lamp (second lamp) 7 was turned on only once when the temperature reached 400 ° C. 5 seconds after the start of the temperature rise, and immediately thereafter, the tungsten halogen lamp 6 was turned off. The lighting time of the flash lamp 7 is 1.3 msec, and its energy is 12 J / cm @ 2. When the semiconductor substrate of the present invention was analyzed by X-ray diffraction as described above, PZT was not crystallized in the sample (semiconductor substrate) which was not irradiated with the flash lamp 6, whereas it was irradiated with the flash lamp. It was confirmed that the sample was crystallized in the perovskite phase. At the same time, the state of the underlying aluminum film 33 was examined by a microscope and a scanning electron microscope, but no change was observed, and it was revealed that the PZT film 37 can be crystallized without changing the aluminum film 33. Became. When the preheating temperature by the tungsten halogen lamp 7 was fixed at 400 ° C. and the output of the flash lamp 8 required for crystallization of the PZT film was examined, it was found that crystallization occurred at 10 J / cm 2 or more.

[0038]

On the contrary, when examining the range in which the PZT film 37 can be crystallized without changing the aluminum film 33 using the preheating temperature as a parameter, heating to about 550 ° C. is possible if the preheating time is within 1 second. However, it was confirmed that the aluminum film 33 did not change. The Pt film 38 was again formed on the semiconductor substrate 31 by sputtering using argon gas. The film thickness was 150 nm. When the polarization characteristics of this sample were measured, it was revealed that the residual polarization value was 30 μC / cm 2, which was comparable to the PZT film crystallized by ordinary RTA. When two kinds of lamps are turned on at the same time, the power is consumed accordingly. It is also possible to turn on the tungsten halogen lamp 6 and turn on the flash lamp 7 at the moment when the lamp is turned off in order to reduce the power consumption. In this case, although the tungsten halogen lamp 6 consuming a few tens of kW of power is turned off, the temperature of the semiconductor substrate 31 is still maintained immediately after the light is turned off. Therefore, only one electrode is required for lighting the lamp, and at the same time, it is possible to reduce power consumption.

[0039]

The ferroelectric film is not limited to the PZT film, but many materials such as SBT (SrBiTa2 O9) and BTO (BaTiO3) exist, but by implementing the present invention, these films can be formed without changing the aluminum film. It goes without saying that it is possible to crystallize. The

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present invention is not limited to the method of crystallizing a ferroelectric film formed on a semiconductor substrate, but includes strontium titanate (SrTiO3, STO) and strontium barium titanate (Bax Sr1-x TiO3) crystals. It can be applied to a wide range of processes such as crystallization, crystallization of Ta2 O5, and the like, in which the heat energy applied to the base must be suppressed.

[0040]

According to the present invention, the contact portion of a semiconductor device can be manufactured rapidly at low temperature with good controllability, and as a result, a metal gate electrode, a high dielectric constant gate insulating film, and a low dielectric constant interlayer insulating film can be manufactured. New materials with low heat resistance, which are found in films, can be easily applied to semiconductor devices, and high performance of element characteristics can be realized. Further, by using the present invention, a ferroelectric capacitor can be formed on the aluminum wiring without causing thermal damage to the aluminum wiring. It is possible to form a ferroelectric capacitor on any number of aluminum wiring layers formed.

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1.
When heat-treating the sample, a step of heating using at least two types of lamps having different lighting times is provided, and when the sample is heat-treated, the first type of lamp is lit, and then, A heat treatment method comprising heating a sample by lighting a second type of lamp, which is a flash lamp, while the first type of lamp is lighting.

2.
Forming an insulating film on a semiconductor substrate and forming a contact hole in the insulating film to expose the semiconductor substrate or a conductor film formed on the semiconductor substrate; and a semiconductor substrate exposed from the contact hole A step of depositing a wiring or a conductive electrode connected to the surface or the conductive film to form a contact portion; and heat treating the semiconductor substrate to form the semiconductor substrate surface or the conductive film and the wiring or the conductive A step of improving the contact property of the contact portion with an electrode, and in the step of heat-treating the semiconductor substrate, two heating sources having different emission wavelength distributions and irradiation times are used, and the first heating source is irradiated, A method for manufacturing a semiconductor device, comprising irradiating a second heating source for a time shorter than an irradiation time of the first heating source before the heat treatment temperature is lowered during irradiation or after the irradiation is stopped.

3.
The method of manufacturing a semiconductor device according to claim 2, wherein the wiring or the conductive electrode is a metal film capable of reducing an oxide film formed on the

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surface of the semiconductor substrate or the surface of the conductor film.

4.

In the metal film capable of reducing the oxide film, the heat generated during the formation of the oxide film and the formation of a compound with an element constituting the semiconductor substrate or the conductor film, which is a base, is generated on the surface of the semiconductor substrate or the conductor. 4. The method of manufacturing a semiconductor device according to claim 3, wherein the heat of formation of the oxide film formed on the surface of the film is larger than the heat of formation.

5.

The method for manufacturing a semiconductor device according to claim 4, wherein the metal film capable of reducing the oxide film contains 5 to 20 atomic% of silicon.

6.

The heating source comprises the first heating source having an emission wavelength in an infrared region and a second heating source having an emission wavelength on a shorter wavelength side than the first heating source. 5. The method for manufacturing a semiconductor device according to item 5.

7.

7. The method for manufacturing a semiconductor device according to claim 6, wherein at least a part of the emission wavelength range of the second heating source is in the ultraviolet range.

8.

7. The method of manufacturing a semiconductor device according to claim 6, wherein the second heating source is a flash lamp.

9.

The temperature of the semiconductor substrate by the first heating source is lower than the temperature at which characteristic deterioration of the insulating film, the conductor film, the wiring, and the conductive electrode is not induced, and the second heating source has a low load. 9. The method for manufacturing a semiconductor device according to claim 2, wherein the irradiation energy density is set so as to accelerate the reaction of the contact portion.

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10.

A step of forming at least one layer of aluminum wiring on a semiconductor substrate on which a semiconductor element is formed via an interlayer insulating film, and a lower electrode, a ferroelectric film, an upper portion on the aluminum wiring via the interlayer insulating film. A step of sequentially depositing electrodes by a sputtering method, and a step of heat treating the semiconductor substrate to crystallize the ferroelectric film to form a capacitor composed of the lower electrode, the ferroelectric film and the upper electrode. In the step of heat-treating the semiconductor substrate, at least two kinds of lamps having different lighting times are used, the first kind of lamp is lit, and the second kind is lit during lighting or after being turned off before the heat treatment temperature decreases. The method of manufacturing a semiconductor device, wherein the flash lamp, which is the lamp, is lit for a shorter time than the lighting time of the lamp of the first type.

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(71)出願人　000005108
株式会社日立製作所
東京都千代田区神田駿河台四丁目６番地

(71)出願人　000233169
株式会社日立マイコンシステム
東京都小平市上水本町５丁目22番１号

(72)発明者　鈴樹　正恭
東京都小平市上水本町５丁目20番１号　株式会社日立製作所武蔵工場内

(72)発明者　竹田　敏文
東京都小平市上水本町５丁目20番１号　株式会社日立製作所武蔵工場内

(74)代理人　弁理士　筒井　大和

最終頁に続く

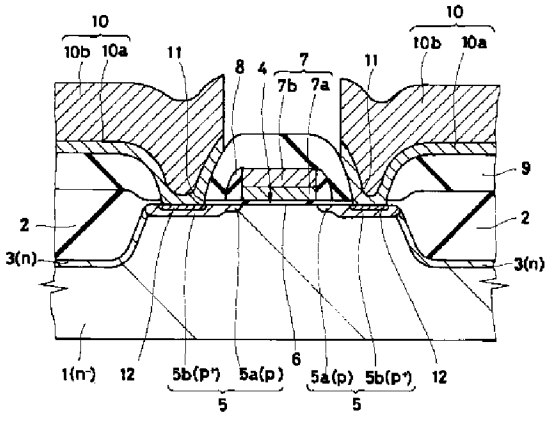
(54)【発明の名称】　半導体集積回路装置およびその製造方法

(57)【要約】

【目的】　半導体集積回路装置を構成する配線の下地金属膜と半導体基板との接触抵抗を低減する。

【構成】　半導体集積回路装置を構成する配線１０の下地金属膜１０ａと、半導体基板１上の半導体層５との接触部に、下地金属膜１０ａと半導体基板１との各々の構成原子が化合されてなり、かつ、半導体基板１に対してエピタキシャルとなるシリサイド層１２を設けた。

図１



１：半導体基板　１０：配線
４：ｐチャネルＭＯＳ・ＦＥＴ　１０ａ：下地金属膜
５：半導体層　１２：シリサイド層（化合物層）
９：層間絶縁膜

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【特許請求の範囲】
【請求項１】　半導体基板上の絶縁膜上に下地金属膜と導体膜とを下層から順に積層してなる配線を設けるとともに、前記下地金属膜と前記半導体基板との接触部に、下地金属膜および半導体基板の各々の構成原子が化合されてなり、かつ、前記半導体基板に対してエピタキシャルである化合物層を設けたことを特徴とする半導体集積回路装置。
【請求項２】　前記下地金属膜が、チタンタングステンであることを特徴とする請求項１記載の半導体集積回路装置。
【請求項３】　前記接触部を、ＭＩＳ・ＦＥＴのソース・ドレイン形成用の半導体層またはショットキバリヤダイオードのショットキ接触形成用の半導体層に形成したことを特徴とする請求項１または２記載の半導体集積回路装置。
【請求項４】　半導体基板上の絶縁膜に半導体基板に達する接続孔を形成する工程と、前記接続孔の形成された絶縁膜上に配線形成用の下地金属膜を堆積する工程と、前記半導体基板に対してアニールを施し、前記下地金属膜と前記半導体基板との接触部において下地金属膜と半導体基板との各々の構成原子を化合させ、半導体基板に対してエピタキシャルとなる化合物層を形成し、前記下地金属膜と半導体基板とを電気的に接続する工程とを有することを特徴とする半導体集積回路装置の製造方法。
【請求項５】　前記下地金属膜と半導体基板との接続と同時に、前記化合物層と半導体基板との接触部にショットキ接触部を形成することを特徴とする請求項４記載の半導体集積回路装置の製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、半導体集積回路装置およびその製造技術に関し、特に、半導体集積回路装置を構成する配線と、半導体基板との接続技術に関するものである。
【０００２】
【従来の技術】半導体集積回路装置の配線材料には、アルミニウム（Ａｌ）またはその合金が使用されている。Ａｌは、抵抗率が低い、シリコン（Ｓｉ）に形成されたp^+形またはn^+形の半導体層との接触抵抗が低い、成膜・加工が容易である等、半導体集積回路装置の配線材料として用いるのに優れた性質を有するからである。
【０００３】しかし、単層Ａｌ配線では、半導体集積回路装置における配線や接続孔等の微細化に伴い、エレクトロマイグレーション・ストレスマイグレーションに起因する配線断線不良やＡｌ配線側にＳｉが析出することに起因するＡｌ配線と半導体基板との接触抵抗の増大等、配線の信頼性上の問題が顕著となってきた。
【０００４】そこで、近年は、Ａｌ配線の下層に、例えばチタンタングステン（ＴｉＷ）、窒化チタン（ＴｉＮ）、タングステン（Ｗ）またはモリブデン（Ｍｏ）等からなる下地金属膜を設けることにより、配線断線不良やＳｉの析出等を防ぎ、配線の信頼性を確保する傾向にある。
【０００５】ところが、下地金属膜を、Ｓｉ基板と直接接触させると、接触抵抗、特に、ｐチャネルＭＯＳ・ＦＥＴ（以下、単にｐＭＯＳという）等のソース・ドレイン領域を形成するｐ形半導体層に直接接触させた場合の接触部における接触抵抗が高くなるという問題がある。
【０００６】その解決方法として、接触面積を増大させることが考えられるが、その場合、半導体集積回路装置の微細化傾向に反する。また、ｐ形半導体層の不純物濃度を高めに設定することも考えられるが、その場合、短チャネル効果等、ｐＭＯＳの特性を劣化させる問題が生じ、ｐＭＯＳの微細化を阻害する。
【０００７】そこで、そのような問題を招くことなく、下地金属膜とｐ形半導体層との接触抵抗を低くする方法として、下地金属膜と、ｐ形半導体層との間に、例えばプラチナシリサイド（ＰｔＳｉ）層等のような低抵抗のシリサイド層を介在させる方法が提案されている。この方法は、例えば次のようにする。
【０００８】まず、Ｓｉ基板主面上の絶縁膜に、ｐ形半導体層の露出する接続孔を形成した後、Ｓｉ基板上にＰｔ膜を堆積する。続いて、Ｓｉ基板に対して熱処理を施し、Ｐｔ膜とｐ形半導体層との接触部において、ＰｔとＳｉとを反応させて、その接触部にＰｔＳｉ層を形成した後、Ｐｔ膜を王水によって除去する。この時、接続孔内のｐ形半導体層上にはＰｔＳｉ層が残存する。その後、Ｓｉ基板上に、下地金属膜およびＡｌ合金膜を順に堆積した後、それらの積層膜をフォトリソグラフィ技術によってパターンニングして二層構造の配線を形成する。
【０００９】なお、Ａｌ配線の下層に下地金属膜を設ける従来技術については、例えば日刊工業新聞社、昭和６２年９月２９日発行、「ＣＭＯＳデバイスハンドブック」Ｐ３３２～Ｐ３３３に記載があり、Ａｌ配線の下層にバリヤメタルを設ける必要性等について説明されている。
【００１０】
【発明が解決しようとする課題】ところで、配線を構成する下地金属膜と、半導体基板のｐ形半導体層との接触部に、ＰｔＳｉ層等のような低抵抗のシリサイド層を設ける上記従来の技術は、半導体集積回路装置の微細化に反しないし、また、半導体層の不純物濃度を高くしなくとも良いので、短チャネル効果等も発生せず、素子の微細化を促進させることが可能であるが、Ｐｔ膜を堆積する工程やＰｔ膜を除去する工程が必要となるので、半導体集積回路装置の製造工程数が増大する上、その工程が複雑となる問題があることを本発明者は見い出した。
【００１１】本発明は上記課題に着目してなされたもの

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であり、その目的は、半導体集積回路装置の製造工程の増大や複雑化を招くことなく、配線を構成する下地金属膜と、半導体基板との接触抵抗を低くすることのできる技術を提供することにある。

【００１２】本発明の前記ならびにその他の目的と新規な特徴は、明細書の記述および添付図面から明らかになるであろう。

【００１３】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、以下のとおりである。

【００１４】すなわち、請求項１記載の発明は、半導体基板上の絶縁膜上に下地金属膜と導体膜とを下層から順に積層してなる配線を設けるとともに、前記下地金属膜と前記半導体基板との接触部に、下地金属膜および半導体基板の各々の構成原子が化合されてなり、かつ、前記半導体基板に対してエピタキシャルである化合物層を設けた半導体集積回路装置構造とするものである。

【００１５】請求項４記載の発明は、半導体基板上の絶縁膜に半導体基板に達する接続孔を形成する工程と、前記接続孔の形成された絶縁膜上に配線形成用の下地金属膜を堆積する工程と、前記半導体基板に対してアニールを施し、前記下地金属膜と前記半導体基板との接触部において、下地金属膜と半導体基板との各々の構成原子を化合させ、半導体基板に対してエピタキシャルとなる化合物層を形成し、前記下地金属膜と半導体基板とを電気的に接続する工程とを有する半導体集積回路装置の製造方法とするものである。

【００１６】

【作用】上記した請求項１記載の発明によれば、例えば配線を構成する下地金属膜と、半導体基板の半導体層との仕事関数差を小さくすることができるので、配線とｐ形半導体層との接触抵抗を低くすることが可能となる。

【００１７】このため、例えばｐＭＯＳのソース・ドレイン領域を構成するｐ形半導体層の不純物濃度を従来よりも低くすることができるので、ｐＭＯＳの短チャネル効果を抑制でき、ｐＭＯＳの微細化を促進させることが可能となる。

【００１８】上記した請求項４記載の発明によれば、例えば前記したＰｔ膜を堆積する工程やＰｔ膜を除去する工程等が必要なくなるので、半導体集積回路装置の製造工程数を低減できる上、その工程の簡略化が可能となる。

【００１９】

【実施例１】図１は本発明の一実施例である半導体集積回路装置の要部断面図、図２～図４は図１の半導体集積回路装置の製造工程中における要部断面図、図５は配線－半導体基板間の接触抵抗とアニール温度との関係を示すグラフ図である。

【００２０】本実施例１の半導体集積回路装置は、例えばＣＭＯＳ（Complimentary MOS)回路によって構成されている。本実施例１の半導体集積回路装置のｐＭＯＳ部分を図１に示す。

【００２１】半導体基板１は、例えばn^-形Ｓｉ単結晶からなり、その主面上の非活性領域には、例えばSiO_2からなるフィールド絶縁膜２が形成されている。なお、フィールド絶縁膜２の下層には、チャネルストッパ層３が形成されている。チャネルストッパ層３には、例えばｎ形不純物であるリンが導入されている。

【００２２】半導体基板１の主面において、フィールド絶縁膜２に囲まれた活性領域には、例えばｐＭＯＳ４が形成されている。すなわち、ｐＭＯＳ４は、その周囲が、フィールド絶縁膜２によって規定されている。

【００２３】ｐＭＯＳ４は、半導体基板１の上部に形成された半導体層５，５と、半導体層５，５間の上方に形成されたゲート絶縁膜６と、ゲート絶縁膜６上に形成されたゲート電極７とを有している。

【００２４】半導体層５は、例えばｐ形不純物であるホウ素等が導入されてなり、例えばｐ形半導体層５ａとp^+形半導体層５ｂとから構成されている。すなわち、本実施例１においては、ｐＭＯＳ４は、ＬＤＤ（Lightly Doped Drain)構造を有している。

【００２５】ゲート絶縁膜６は、例えばSiO_2からなる。ゲート電極７は、例えば二層の導体膜７ａ，７ｂが下層から順に積層されて構成されている。導体膜７ａは、例えばドープトポリシリコンからなる。また、導体膜７ｂは、例えばタングステンシリサイド（WSi_2)からなる。

【００２６】なお、ゲート電極７の側壁には、スペーサ８が形成されている。スペーサ８は、上記ＬＤＤ構造を形成するための絶縁膜であり、例えばSiO_2からなる。

【００２７】半導体基板１上には、層間絶縁膜９が堆積されている。層間絶縁膜９は、例えばSiO_2からなり、その上には、配線１０が形成されている。

【００２８】配線１０は、下地金属膜１０ａと、導体膜１０ｂとが下層から順に積層されてなり、その下地金属膜１０ａの一部が層間絶縁膜９に穿孔された接続孔１１を通じて半導体層５と電気的に接続されている。

【００２９】そして、本実施例１においては、下地金属膜１０ａと、半導体層５との接触部に、下地金属膜１０ａと半導体層５との各々の構成原子が化合されてなり、かつ、半導体基板１に対してエピタキシャルとなるシリサイド層（化合物層）１２が形成されている。

【００３０】すなわち、本実施例１の半導体集積回路装置においては、下地金属膜１０ａと半導体層５との接触部に、シリサイド層１２を設けたことにより、下地金属膜１０ａと半導体層５との仕事関数差を小さくすることができるので、下地金属膜１０ａと半導体層５との接触抵抗を低くすることが可能な構造になっている。

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【００３１】下地金属膜１０ａは、例えば３０ａｔｍ％程度のチタン（Ｔｉ）を含むＴｉＷからなり、その厚さは、例えば１５０ｎｍ程度である。

【００３２】ただし、下地金属膜１０ａのＴｉの量は、３０ａｔｍ％に限定されるものではなく種々変更可能であり、例えば１５ａｔｍ％以上、６０ａｔｍ％以下の範囲が好ましい。これは、次のような発明者の研究結果による。

【００３３】すなわち、例えば下地金属膜１０ａに含まれるＴｉの量を１５ａｔｍ％以下とした場合、下地金属膜１０ａと半導体層５との接触部にはエピタキシャルなシリサイド層が充分形成されず、下地金属膜１０ａと半導体層５との接触抵抗も余り低くならなかった。

【００３４】一方、下地金属膜１０ａと半導体層５との接触抵抗が充分低下した場合において、下地金属膜１０ａを除去し、シリサイド層１２をエックス線マイクロアナライザーで分析したところ、ＴｉとＷとのモル比は、約６対４であった。

【００３５】ＴｉとＷとの組成比は、同一のスパッターゲットを用いてもスパッタリング装置の違い等により若干異なるが、上記の分析結果から６０ａｔｍ％程度以下のＴｉを含むＴｉＷならばシリサイド層１２を半導体基板１に対してエピタキシャルとすることができると判明した。

【００３６】ただし、下地金属膜１０ａは、ＴｉＷに限定されるものではなく種々変更可能であり、例えばＴａＷ、ＴｉＴａ等でも良い。

【００３７】導体膜１０ｂは、例えばＡｌまたはＡｌ－Ｓｉ－銅（Ｃｕ）合金からなり、その厚さは、例えば４００ｎｍ程度である。

【００３８】シリサイド層１２は、例えばＴｉ、ＷおよびＳｉの化合物からなり、その厚さは、例えば３ｎｍ程度である。

【００３９】なお、図示はしないが、配線１０および層間絶縁膜９上には、表面保護膜が堆積されている。表面保護膜は、例えばプラズマＣＶＤ法によって堆積されたSiO_2からなる絶縁膜と、同じくプラズマＣＶＤ法等によって堆積された窒化ケイ素（Si_3N_4）からなる絶縁膜とが下層から順に積層されて構成されている。

【００４０】次に、本実施例１の半導体集積回路装置の製造方法を図２～図５により説明する。なお、本実施例１においては、説明を簡単にするため、ｎチャネルＭＯＳの製造工程部分は説明を省略する。

【００４１】まず、図２に示すように、例えばn^-形Ｓｉ単結晶からなる半導体基板１の主面における非活性領域を選択的に酸化し、その領域にフィールド絶縁膜２を形成する。この際、同時に、フィールド絶縁膜２の下層にｎ形のチャネルストッパ層３を形成する。

【００４２】続いて、半導体基板１の主面において、フィールド絶縁膜２により周囲を規定された活性領域を酸化し、その領域にゲート絶縁膜６を形成する。

【００４３】その後、半導体基板１上にドープトポリシリコンからなる導体膜およびWSi_2からなる導体膜を堆積した後、それらの導体膜をフォトリソグラフィ技術によってパターンニングしてゲート電極７を形成する。

【００４４】次いで、ゲート電極７をマスクとして、半導体基板１に、例えばｐ形不純物であるホウ素等を軽くイオン打ち込みして、ｐ形半導体層５ａを形成する。

【００４５】続いて、半導体基板１上に図示しない絶縁膜を堆積した後、その絶縁膜をエッチバックして、ゲート電極７の側壁にスペーサ８を形成する。

【００４６】その後、半導体基板１の全面に薄い酸化膜を形成した後、ゲート電極７およびスペーサ８をマスクとして、半導体基板１に、例えばｐ形不純物であるホウ素等をイオン打ち込みして、p^+形半導体層５ｂを形成する。このようにして、半導体基板１上にｐＭＯＳ４を形成する。

【００４７】次いで、図３に示すように、半導体基板１上に、例えばSiO_2からなる層間絶縁膜９をＣＶＤ法等によって堆積した後、フォトリソグラフィ技術によって層間絶縁膜９に、半導体層５に達する接続孔１１を穿孔する。

【００４８】続いて、半導体基板１上に、例えば下地金属膜１０ａ（図１参照）を形成するためのＴｉＷからなる金属膜$10a_1$をスパッタリング法等によって堆積する。

【００４９】この時の金属膜$10a_1$のＴｉの量は、上記した理由により、例えば３０ａｔｍ％程度である。また、金属膜$10a_1$の厚さは、例えば１５０ｎｍ程度である。

【００５０】その後、半導体基板１を通常の炉体（図示せず）内に収容して、例えば窒素雰囲気で６５０℃のアニールを３０分間施し、金属膜$10a_1$のＴｉＷと、半導体層５のＳｉとを化合させて、図４に示すように、金属膜$10a_1$と半導体層５との接触部にシリサイド層１２を形成する。

【００５１】すなわち、本実施例１においては、下地金属膜１０ａと半導体層５との接触部にＰｔＳｉ膜を形成する従来技術のようなＰｔ膜を堆積する工程やＰｔ膜を除去する工程が不要となるので、半導体集積回路装置の製造工程を低減できる上、その工程の簡略化が可能となる。

【００５２】また、アニールによって形成されたシリサイド層１２は、半導体基板１に対してエピタキシャルであり、かつ、厚さ３ｎｍ程度の薄い層であった。このため、シリサイド層１２を形成する際の化学反応等に伴う体積変化による半導体基板１や半導体層５への応力が小さくてすみ、その応力に起因する接合リークの増加等も観測されず、ｐＭＯＳ４において良好な電気的特性が示された。

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【００５３】さらに、アニールしたことにより、アニールを行わなかった場合に比べて導体膜１０ｂ（図１参照）の抵抗が低くなり、配線１０の抵抗を低くすることができた。これは、アニールをしたことにより、金属膜$10a_1$の表面に反応性の低いＴｉの酸化物等が偏析されたため、この後、金属膜$10a_1$上に堆積するＡｌからなる導体膜１０ｂと金属膜$10a_1$の反応が抑制された結果、Ａｌからなる導体膜１０ｂ本来の導電率が確保されたためと想定される。

【００５４】ただし、アニール温度は、６５０℃に限定されるものではなく種々変更可能であり、例えば５５０℃～７５０℃、理想的には、例えば６００℃以上、７００℃以下の範囲が好ましい。

【００５５】下地金属膜１０ａおよび半導体層５の接触部の接触抵抗と、アニール温度との関係を図５に示す。図５に示すように、下地金属膜１０ａと半導体層５との接触抵抗が大幅に低下するのは、ほぼ６００℃以上であることが判る。

【００５６】しかし、本発明者の研究によれば、アニール温度を７５０℃以上とすると、シリサイド層１２に直径数十ｎｍ程度の不均一な結晶粒が観測された。この場合の試料の断面を透過電子顕微鏡等によって観測した結果、接続孔１１の周辺のp^+形半導体層５ｂに強い歪が観測され、それが原因でp^+半導体層５と半導体基板１との接合部が破壊されることが判明した。

【００５７】さらに、本発明者の研究によれば、アニール温度が６００℃の場合と７００℃の場合との各々の試料のシリサイド層を、各々のアニール処理後に下地金属膜を除去して、光電子分光法等によって調査したところ、それらの場合のシリサイド層は、上述のアニール温度が６５０℃の場合の良好なシリサイド層１２とほぼ同一の表面状態となることが判明した。

【００５８】したがって、アニールの方法等によっても変わると想定されるので、一概には規定できないが、少なくともアニール温度が、例えば６００℃～７００℃程度の範囲であれば、半導体基板１に対してエピタキシャルとなる良好なシリサイド層１２が形成される。

【００５９】アニール処理によってシリサイド層１２を形成した後、金属膜$10a_1$上に、例えばＡｌ－Ｓｉ－Ｃｕ合金からなる導体膜（図示せず）を堆積した後、その導体膜および金属膜$10a_1$をフォトリソグラフィ技術によってパターンニングして図１に示した配線１０を形成する。

【００６０】その後、図示はしないが、配線１０および層間絶縁膜９上に、例えばプラズマＣＶＤ法等によってSiO_2膜およびSi_3N_4膜を堆積し、半導体基板１上に表面保護膜を形成する。

【００６１】このように本実施例１によれば、以下の効果を得ることが可能となる。

【００６２】(1).配線１０を構成する下地金属膜１０ａと、ｐＭＯＳ４を構成する半導体層５との接触部に、半導体基板１に対してエピタキシャルとなるシリサイド層１２を設けたことにより、下地金属膜１０ａと半導体層５との仕事関数差を小さくすることができるので、下地金属膜１０ａと半導体層５との接触抵抗を低くすることが可能となる。

【００６３】(2).上記(1)により、p^+形半導体層５ｂの不純物濃度を従来よりも低くすることができるので、ｐＭＯＳ４の短チャネル効果を抑制することができ、ｐＭＯＳ４の微細化を促進させることが可能となる。したがって、半導体集積回路装置の素子集積度の向上を図ることが可能となる。

【００６４】(3).シリサイド層１２をアニールによって形成することにより、下地金属膜１０ａと半導体層５との接触部にＰｔＳｉ膜を形成する従来技術の場合のようなＰｔ膜を堆積する工程やＰｔ膜を除去する工程が不要となるので、その従来技術の場合よりも半導体集積回路装置の製造工程を低減できる上、その工程の簡素化が可能となる。

【００６５】(4).下地金属膜１０ａを、例えば１５ａｔｍ%以上、６０ａｔｍ%以下、理想的には、３０ａｔｍ%のＴｉを含むＴｉＷによって構成するとともに、アニール温度を、例えば５５０℃～７５０℃、理想的には６００℃以上、７００℃以下の範囲としてアニールすることにより、例えば３ｎｍ程度の非常に薄く、かつ、半導体基板１に対してエピタキシャルとなるシリサイド層１２を形成することが可能となる。

【００６６】(5).上記(4)により、シリサイド層１２を形成する際の化学反応等に伴う体積変化による半導体基板１や半導体層５への応力が小さくてすみ、その応力に起因する接合リークの増加等も観測されず、ｐＭＯＳ４において良好な電気的特性を得ることが可能となる。

【００６７】

【実施例２】図６～図１０は本発明の他の実施例である半導体集積回路装置の製造工程中における半導体基板の要部断面図、図１１は半導体集積回路装置の製造工程の要部の工程図、図１２は接続孔における配線とp^+形半導体層とのコンタクト抵抗のアニール温度依存性を示すグラフ図、図１３は接合リーク電流のアニール温度依存性を示すグラフ図、図１４（ａ）はショットキバリヤダイオードの順方向の電流電圧特性を示すグラフ図、図１４（ｂ）はショットキバリヤダイオードの逆方向の電流電圧特性を示すグラフ図、図１５はＳＥＭによって観測されたポストアニール後のシリサイド層の断面図、図１６はＴＥＭによって観測されたアニール後の下地金属膜と半導体基板との界面の断面図、図１７はシリサイド層のＸ線回折スペクトルを示すグラフ図、図１８（ａ）～（ｃ）はシリサイド層のＥＳＣＡスペクトルを示すグラフ図、図１９は下地金属膜のシリサイデーションのモデルを示す説明図である。

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【００６８】本実施例２の半導体集積回路装置の製造方法は、例えば同一の半導体基板上にＣＭＯＳ回路およびショットキバリヤダイオード（Shyottoky Barrier Diode：以下、ＳＢＤと略す）を有する半導体集積回路装置の製造方法である。以下、本実施例２の半導体集積回路装置の製造方法を図６～図１１によって説明する。

【００６９】図６に示す半導体基板１は、例えばｐ形のＳｉ単結晶からなる抵抗率１０Ω ｃｍの（１００）基板である。

【００７０】まず、このような半導体基板１に対して、ＬＯＣＯＳ法等によりフィールド絶縁膜２を形成した後、ｐＭＯＳ形成領域ＰおよびＳＢＤ形成領域Ｓに、例えばｎ形不純物であるリン（Ｐ）をイオン注入してｎウェル１３ｎを形成する。なお、図６のＮは、ｎＭＯＳ形成領域を示している。

【００７１】続いて、図７に示すように、ｎＭＯＳ形成領域Ｎに、例えばｐ形不純物であるボロン（Ｂ）をイオン注入してｐウェル１３ｐを形成する。

【００７２】その後、図８に示すように、ゲート電極７を形成した後、ｐＭＯＳ形成領域Ｐには、例えばボロンを、ｎＭＯＳ形成領域Ｎには、例えばリンをイオン注入し、ソース、ドレインを構成するp^+形半導体層５ｃ，５ｃおよびn^+形半導体層５ｄ，５ｄを形成する。

【００７３】次いで、図９に示すように、半導体基板１上に絶縁膜１４を形成した後、その絶縁膜１４にp^+半導体層５ｃ、n^+半導体層５ｄおよびＳＢＤ形成領域Ｓにおけるｎウエル１３ｎに達するそれぞれ接続孔１１ａ～１１ｃを開孔する。

【００７４】続いて、半導体基板１上に、例えばＴｉＷからなる下地金属膜１０ａをデポした後、シリサイデーションする。これにより、前記実施例１と同様に、下地金属膜１０ａと、p^+形半導体層、n^+形半導体層およびｎウエル１３ｎとの間に、図９には図示しないシリサイド層（化合物層）が形成される。シリサイデーションについては後述する。

【００７５】その後、図１０に示すように、例えばＡｌＣｕＳｉ、ＴｉＷを順にデポし、例えばＴｉＷ／ＡｌＣｕＳｉ／ＴｉＷからなる配線１０を形成する。これにより、ｎＭＯＳ形成領域ＮにｎチャネルＭＯＳ・ＦＥＴ１５を形成し、ｐＭＯＳ形成領域ＰにｐＭＯＳ４を形成し、ショットキバリヤダイオード（ＳＢＤ）形成領域Ｓにショットキバリヤダイオード（ＳＢＤ）１６を形成する。

【００７６】図１１に、例えば本実施例２のＴｉＷシリサイデーションのプロセスフローを示す。

【００７７】接続孔１１（図９，図１０参照）をドライエッチング法等によって形成した後（工程１０１）、ウエットの前処理を行ない（工程１０２）、その後、例えばＴｉＷをスパッタリング法により半導体基板１上に形成する（工程１０３）。

【００７８】スパッタは、例えば通常のＤＣスパッタ装置（図示せず）を用い、ターゲットには、例えば１０ｗｔ％Ｔｉ－Ｗターゲットを用いた。その後、一般的な横型炉体（図示せず）を用い、例えばN_2雰囲気で、５００～８００℃で３０分間アニールした（工程１０４）。

【００７９】最後に、例えばＡｌＣｕＳｉ、ＴｉＷを、例えばスパッタリング法で順に形成し、配線１０を形成した（工程１０５，１０６）。

【００８０】次に、このようにして形成された半導体集積回路装置の評価項目と評価方法について説明する。

【００８１】電気特性は、コンタクト抵抗、接合リーク電流およびＳＢＤ特性を測定した。

【００８２】コンタクト抵抗は、例えばケルビン法を用いて0.６μｍ×0.６μｍ程度のコンタクトホールを測定した。接合リーク電流は、例えば３５，０００μm^2の大面積ｐ／ｎ接合を用い、逆方向電流を測定した。ＳＢＤ特性は、例えば面積６００μm^2のＳＢＤを作製し、順方向特性と逆方向特性を測定した。

【００８３】シリサイデーションの物理的現象を明らかにするため、シリサイド層の断面を走査型電子顕微鏡（ＳＥＭ）、透過型電子顕微鏡（ＴＥＭ）によって観察した。

【００８４】また、ＴｉＷ／Ｓｉ界面に関しては、Ｘ線光電子分光法（ＥＳＣＡ）、Ｘ線回折（ＸＲＤ）による分析を行った。

【００８５】次に、その評価による半導体集積回路装置の電気的特性について説明する。

【００８６】コンタクト抵抗のアニール温度依存性を図１２に示す。p^+形半導体層（p^+Ｓｉ）に対するコンタクト抵抗は、アニール無しでは約６００Ωと高いのに対し、アニール温度を高くするにつれて抵抗は低くなり、例えば６５０℃以上では１００Ω以下の値が得られる。なお、n^+形半導体層（n^+ Ｓｉ）に対するコンタクト抵抗はアニール無しでも約５０Ωと十分低く、アニールしてもほとんど変化は見られない。

【００８７】接合リーク電流のアニール温度依存性を図１３に示す。リーク電流は、n^+／ｐ接合、p^+／ｎ接合のいずれの場合にも、７００℃程度まではアニール無しの場合と同等で小さいが、７５０℃以上のアニールで急激な増加が見られる。

【００８８】以上の結果より、コンタクト抵抗が十分低く、かつ、接合リーク電流が増加しない６５０℃程度のアニールを標準条件とし、以下この条件で作製したサンプルに対し、測定を行った。

【００８９】その場合のＳＢＤ特性の測定結果の例を図１４（ａ），（ｂ）に示す。図１４（ａ）には順方向特性、図１４（ｂ）には逆方向特性の結果を示す。ＳＢＤの順方向電流は、熱電子放出理論によれば、次式のように表される（Ｓ．Ｍ．Sze, Physics of Semiconductor Devices, 2nd ed.（Wiley, New York, １９８

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１））。

【００９０】

Ｊ＝Ｊｓ［ｅｘｐ（ｑＶ／ｎｋＴ）－１］

Ｊｓ＝Ａ* Ｔ2 ｅｘｐ（－ｑφＢ／ｋＴ）

ここで、ｑは素電荷、ｋはボルツマン（Boltzmann）定数、Ｔは絶対温度、Ａ* は有効リチャードソン（Richardson)定数、φＢはバリアハイトである。ｎは理想値からの補正係数であり、理想的にはｎ＝１である。

【００９１】図１４（ａ）より、例えばφＢ＝0.６１ｅＶ、ｎ＝1.０３が得られた。φＢ＝0.６１ｅＶは、ＴｉＳｉ$_2$ のφＢ＝0.６０ｅＶとＷＳｉ$_2$ のφＢ＝0.６５ｅＶの間の値である（Ｓ．Ｍ．Ｓze，Physics of Semiconductor Devices，2nd ed.(Wiley，New York，１９８１））。また、ｎ＝1.０３は理想値に近く、良好なＳＢＤ特性であることが判る。

【００９２】次に、例えば７００～８００℃でアニールした接続孔部の断面ＳＥＭ写真を図１５に示す。半導体基板の断面を研磨した後、例えばＨＦ：HNO_3 ：CH_3COOH混合液に浸漬して拡散層（n^+ 半導体層）をエッチングし、観察した。

【００９３】例えば８００℃ではシリサイド層が、拡散層の厚さ以上に成長し、そのため接合リーク電流が増加したことが判る。一方、例えば７５０℃以下では、明確なシリサイド層の形成は観察されない。

【００９４】また、例えば６５０℃、３０分のアニールを施した時のＴｉＷ／Ｓｉ界面の断面ＴＥＭ写真を図１６に示す。半導体基板１とＴｉＷからなる下地金属膜１０ａとの間に厚さ約４～５ｎｍのシリサイド層１２がエピタキシャルに形成されており、その格子面間隔は約0.３９ｎｍである。

【００９５】これは、ＷＳｉ$_2$ （００２）の0.３９１ｎｍ（Ｆ．ｄ’Heurle,et al.，Ｊ.Appl.Phys.，Ｖol.５１，ｐ．５９７６（１９８０）、S.Murarka,et al.,Ｊ．Appl.Phys.，Ｖol.５２，ｐ．７４５０（１９８１））もしくは$Ti_3W_2Si_{10}$（１００）の0.３９９ｎｍ（Ｆ．Nova,et al.，Ｊ．Appl.Phys.，Ｖo1.54,ｐ．２４３４（１９８３）、Ｊ．Ｍ．Harris,et al.，Ｊ．Electrochem.Soc.,Ｖol.１２３，ｐ．１２０（１９７６））に近い。

【００９６】次に、シリサイド層のＸＲＤスペクトルを図１７に示す。例えばＴｉＷシリサイデーション後、例えばH_2O_2 で表面のＴｉＷを除去し、Ｃｕ　ｋαを用いて測定した。

【００９７】例えば６５０℃ではシリサイデーションに起因する明確なピークは観察されないが、例えば７００℃で$2\theta=22°$ に（$Ti_{1-X}W_X$）Si_2 の僅かなピークが観察される。さらに、例えば７５０℃以上では（$Ti_{1-X}W_X$）Si_2 、WSi_2 の強いピークが観察され、厚い（$Ti_{1-X}W_X$）Si_2 とWSi_2 の混晶が形成されていることが判る。

【００９８】次に、例えばH_2O_2 でＴｉＷを除去した後の半導体基板表面のＥＳＣＡスペクトルを図１８（ａ）～（ｃ）に示す。例えば５００℃～７５０℃までのアニール温度に対して、例えばＳｉ（２ｐ）、Ｔｉ（２ｐ）、Ｗ（４ｆ）のスペクトルの変化を示している。

【００９９】まず、図１８（ａ）のＳｉ（２ｐ）のスペクトルに注目すると、Ｓｉ（ｍｅｔａｌ）ピークとＳｉ（ｏｘｉｄｅ）ピークとの結合エネルギー差（化学シフト）が、例えば５５０℃以下では４．４０ｅＶであるのに対し、例えば６００℃以上では4.２４ｅＶと、0.１６ｅＶ小さくなっている。この結果は、例えば６００℃以上でシリサイドが生じたことを示している。

【０１００】また、図１８（ｂ），（ｃ）のＴｉ（２ｐ）とＷ（４ｆ）のスペクトルについては、例えば５５０℃まではいずれもｏｘｉｄｅのピークだけが観察されるのに対し、例えば６００℃以上ではｍｅｔａｌとｏｘｉｄｅのピークが観察される。これは、例えば６００℃以上でＴｉとＷのシリサイド層ができていることを示唆している。なお、ｏｘｉｄｅのピークが観察されたのは、空気中での酸化の他に、H_2O_2 でＴｉＷを除去したために酸化されたためである。

【０１０１】次に、例えばＴｉＷシリサイデーションのモデルを図１９に示す。半導体基板１にＴｉＷからなる下地金属膜１０ａを形成した後、例えば６００℃以上の温度でアニールすることにより、下地金属膜１０ａと半導体基板１との間にシリサイド層１２が形成される。

【０１０２】ＴＥＭ、ＥＳＣＡの結果より、例えば６００～７００℃の範囲ではＴｉ、Ｗ、Ｓｉの３元合金（$Ti_{1-X}W_X$）Si_2 がエピタキシャルに形成されていることが判った。このシリサイド層１２の形成により、コンタクト抵抗は低減される。

【０１０３】Ｓ．Ｅ．Babcockらは、５００～９００℃のアニールでは、ＴｉリッチのＴｉＷの場合にはＴｉＷ／Ｓｉ界面に２５ｎｍの$TiSi_2$ が形成されるが、ＷリッチのＴｉＷの場合には７５０℃以上で厚い（$Ti_{1-X}W_X$）Si_2 またはWSi_2 のみが形成されることを報告している（Ｓ．Ｅ．Babcock,et al.，Ｊ．Appl.Phys.，Ｖol．５３，ｐ．６８９８（１９８２）、Ｓ．Ｅ．Babcock,et al.，Ｊ．Appl.Phys.，Ｖol．５９，ｐ．１５９９（１９８６））。

【０１０４】これは、彼らの分析手段がＸＲＤとＲＢＳであったため、４ｎｍ程度の非常に薄い（$Ti_{1-X}W_X$）Si_2 シリサイド層を観察できなかったためと考える。なお、大西らは、ＴｉＷのランプアニール（ＲＴＡ）により、ＴｉＷ／Ｓｉ界面に$TiSi_2$ が形成されることを報告している（大西茂夫，他，ＥＣＳ日本支部第２回シンポジウム《ＵＬＳＩにおけるＡｌ配線技術に関する諸問題》ｐ．５０（１９８９））。

【０１０５】さらに、７５０℃以上のアニールでは、シ

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リサイド層は多結晶の（Ti_{1-X} Wx）Si_2 とWSi_2 の混晶となり、急激に厚膜化する。そして、この厚いシリサイド層１７が拡散層を突き抜けて、接合リーク電流の増加を生じる。

【０１０６】ＴｉＷ／ＳｉとＷ／Ｓｉとのアニールによるシリサイデーションの差異を既に報告している（Ｍ．Ｓｕｚｕｋｉ,ｅｔ ａｌ．，１９９１　ＳＳＤＭ　ｐ．２１３（１９９１））が、上述したように、ＴｉＷ／Ｓｉにおいては（Ti_{1-x} W_x ）Si_2 のエピタキシャル層が形成されるの対し、Ｗ／Ｓｉではエピ成長せず、多結晶ＷSi_2 が形成されるため、低い温度で接合リークが発生し、プロセスウインドウが狭くなる。すなわち、ＴｉＷシリサイデーションは、Ｗに比べて、微細なＵＬＳＩに適したプロセスである。

【０１０７】このように本実施例２によれば、半導体基板１上に堆積されたＴｉＷのシリサイデーションにより、低いコンタクト抵抗と良好なＳＢＤ特性を同時に得ることが可能となる。

【０１０８】この結果、例えば0.６μｍの接続孔１１ｂにおいて、p^+ 形半導体層５ｃに対しても、例えば１００Ω以下の低いコンタクト抵抗とすることが可能となる。また、例えばバリアハイトφＢ＝0.６１ｅＶのＳＢＤを得ることが可能となる。

【０１０９】特に、ＴｉＷのシリサイデーションの際に、例えば６００～７００℃のアニールによりＴｉＷ／Ｓｉ界面に3元合金（Ti_{1-X} W_X ）Si_2 がエピタキシャルに形成され、これにより、コンタクト抵抗を低減することができ、かつ、良好なＳＢＤ特性を得ることが可能となる。

【０１１０】また、シリサイド層１２をアニールによって形成することにより、前記実施例１と同様、下地金属膜１０ａと半導体層との接触部にＰｔＳｉ膜を形成する従来技術の場合のようなＰｔ膜を堆積する工程やＰｔ膜を除去する工程が不要となるので、その従来技術の場合よりも半導体集積回路装置の製造工程を低減できる上、その工程の簡素化が可能となる。

【０１１１】以上、本発明者によってなされた発明を実施例に基づき具体的に説明したが、本発明は前記実施例１，２に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

【０１１２】例えば前記実施例１，２においては、配線を、ＴｉＷからなる下地金属膜上にＡｌ等からなる導体膜を積層して構成した場合について説明したが、これに限定されるものではなく、例えば下地金属膜としてＴｉＭｏ，ＴｉＴａ，ＺｒＷ，ＺｒＭｏ，ＺｒＴａ，ＨｆＷ，ＨｆＭｏ，ＨｆＴａを用いてもよい。これは、ＩＶａ族のＴｉ，Ｚｒ，Ｈｆは金属／Ｓｉ界面のSiO_2 を還元できるので界面反応を均一に起こす働きをし、Ｔａ，Ｗ，ＭｏはＩＶａ族金属に比べシリサイド化のの速度が遅く、薄いシリサイド層しか形成しない。そして、シリサイド層は薄いため格子歪が大きくてもＳｉ上に安定に存在できるためである。

【０１１３】また、例えば配線を、下地金属膜上にW膜を積層して構成しても良い。これらの場合は、配線をパターンニングした後に、シリサイド層を形成するためのアニールを行うようにしても良い。

【０１１４】また、前記実施例１，２においては、シリサイド層を形成するためのアニールを炉体内で行う場合について説明したが、これに限定されるものでなく、例えばランプラニール法を用いても良い。ランプアニールに際しては、処理室内の雰囲気を、例えば窒素雰囲気またはアンモニア雰囲気とする。

【０１１５】ランプアニールを用いた場合、アニール処理時間を１分間程度に短縮することが可能となる。また、この場合は、例えば７５０℃でアニールしても薄いシリサイド層が形成され、接合リークの増加は観測されなかった。

【０１１６】ランプアニールに際して、窒素雰囲気とした場合は、ＴｉＷ等からなる下地金属膜の表面に酸化Ｔｉが析出するため、アニールを行わなかった場合に比べて配線抵抗を低減することができた。

【０１１７】また、ランプアニールに際して、アンモニア雰囲気とした場合は、ＴｉＷ等からなる下地金属膜の表面にＴｉＮや窒化タングステン等が形成され、窒素雰囲気中でアニールした場合よりもＡｌからなる導体膜との反応性を低くすることができ、配線抵抗を低減できた。

【０１１８】以上の説明では主として本発明者によってなされた発明をその背景となった利用分野であるＣＭＯＳ回路によって構成された半導体集積回路装置に適用した場合について説明したが、これに限定されず種々適用可能であり、例えばバイポーラトランジスタによって構成された半導体集積回路装置やＢｉＣ－ＭＯＳ（Ｂｉｐｏｌａｒ ＣＭＯＳ）によって構成された半導体集積回路装置等、他の半導体集積回路装置に適用することも可能である。

【０１１９】

【発明の効果】本願において開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、下記のとおりである。

【０１２０】(1).すなわち、請求項１記載の発明によれば、例えば配線を構成する下地金属膜と、半導体基板のｐ形半導体層との仕事関数差を小さくすることができるので、配線とｐ形半導体層との接触抵抗を低くすることが可能となる。このため、例えばｐＭＯＳのソース・ドレイン領域を構成するｐ形半導体層の不純物濃度を低くすることができるので、ｐＭＯＳの短チャネル効果を抑制でき、ｐＭＯＳの微細化を促進させることが可能となる。したがって、半導体集積回路装置の素子集積度を向上させることが可能となる。

【０１２１】(2).請求項４記載の発明によれば、例えば

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前記したＰｔ膜を堆積する工程やＰｔ膜を除去する工程等が必要なくなるので、半導体集積回路装置の製造工程数を低減できる上、その工程の簡略化が可能となる。すなわち、半導体集積回路装置の製造工程の増大や複雑化を招くことなく、配線と半導体基板との接触抵抗を低くすることが可能となる。

【図面の簡単な説明】

【図１】図１は本発明の一実施例である半導体集積回路装置の要部断面図である。

【図２】図１の半導体集積回路装置の製造工程中における要部断面図である。

【図３】図１の半導体集積回路装置の製造工程中における要部断面図である。

【図４】図１の半導体集積回路装置の製造工程中における要部断面図である。

【図５】配線－半導体基板間の接触抵抗とアニール温度との関係を示すグラフ図である。

【図６】本発明の他の実施例である半導体集積回路装置の製造工程中における半導体基板の要部断面図である。

【図７】図６に続く半導体集積回路装置の製造工程中における半導体基板の要部断面図である。

【図８】図７に続く半導体集積回路装置の製造工程中における半導体基板の要部断面図である。

【図９】図８に続く半導体集積回路装置の製造工程中における半導体基板の要部断面図である。

【図１０】図９に続く半導体集積回路装置の製造工程中における半導体基板の要部断面図である。

【図１１】半導体集積回路装置の製造工程の要部の工程図である。

【図１２】接続孔における配線とp^+形半導体層とのコンタクト抵抗のアニール温度依存性を示すグラフ図である。

【図１３】接合リーク電流のアニール温度依存性を示すグラフ図である。

【図１４】（ａ）は、ショットキバリヤダイオードの順方向の電流電圧特性を示すグラフ図、（ｂ）はショットキバリヤダイオードの逆方向の電流電圧特性を示すグラフ図である。

【図１５】ＳＥＭによって観測されたアニール後のシリサイド層の断面図である。

【図１６】ＴＥＭによって観測されたアニール後の下地金属膜と半導体基板との界面の断面図である。

【図１７】シリサイド層のＸ線回折スペクトルを示すグラフ図である。

【図１８】（ａ）～（ｃ）は、シリサイド層のＥＳＣＡスペクトルを示すグラフ図である。

【図１９】下地金属膜のシリサイデーションのモデルを示す説明図である。

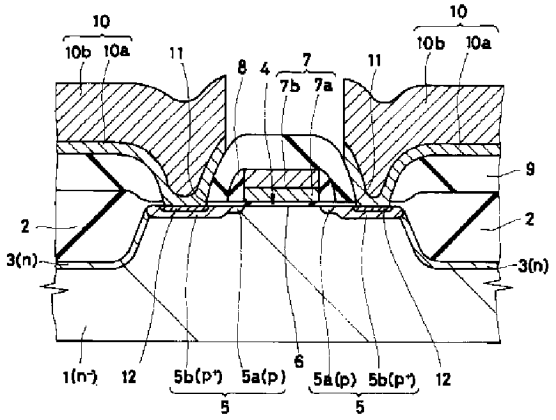
【符号の説明】

１　半導体基板
２　フィールド絶縁膜
３　チャネルストッパ層
４　ｐチャネルＭＯＳ・ＦＥＴ
５　半導体層
５ａ　ｐ形半導体層
５ｂ　p^+形半導体層
５ｃ　p^+形半導体層
５ｄ　n^+形半導体層
６　ゲート絶縁膜
７　ゲート電極
７ａ　導体膜
７ｂ　導体膜
８　スペーサ
９　層間絶縁膜
１０　配線
１０ａ　下地金属膜
$10a_1$　金属膜
１０ｂ　導体膜
１１　接続孔
１１ａ　接続孔
１１ｂ　接続孔
１１ｃ　接続孔
１２　シリサイド層（化合物層）
１３ｎ　ｎウエル
１３ｐ　ｐウエル
１４　絶縁膜
１５　ｎチャネルＭＯＳ・ＦＥＴ
１６　ショットキバリヤダイオード
１７　シリサイド層
Ｐ　ｐＭＯＳ形成領域
Ｎ　ｎＭＯＳ形成領域
Ｓ　ショットキバリヤダイオード形成領域

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【図1】

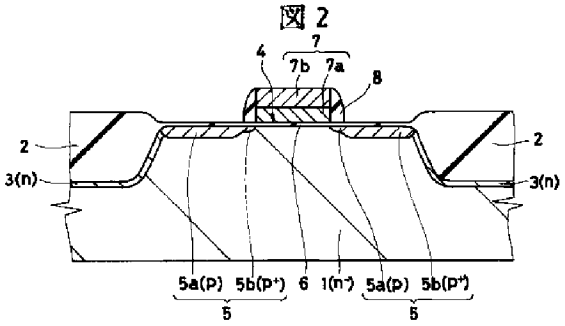
図 1



1：半導体基板　　10：配線
4：pチャネルMOS・FET　10a：下地金属膜
5：半導体層　　12：シリサイド層（化合物層）
9：層間絶縁膜

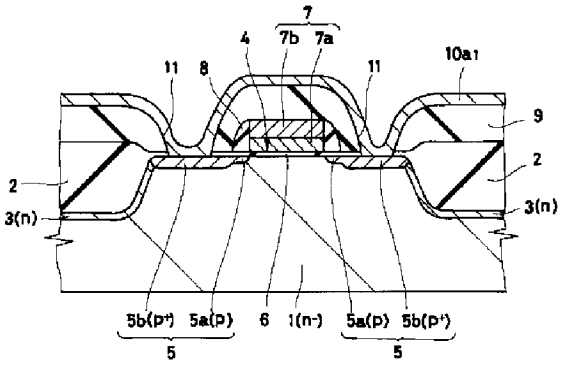
【図2】

図 2



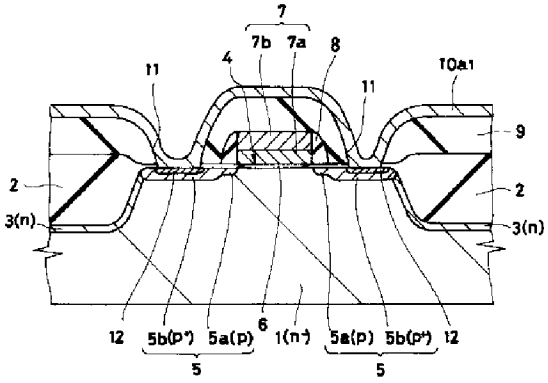
【図3】

図 3



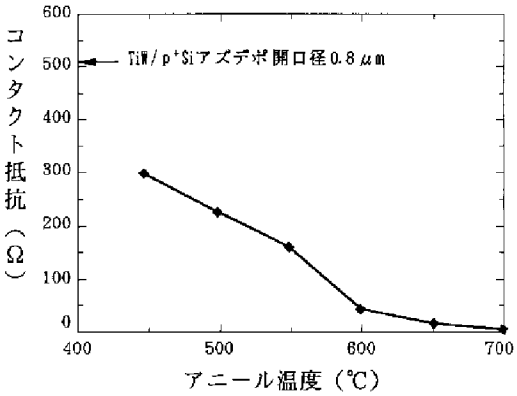
【図4】

図 4



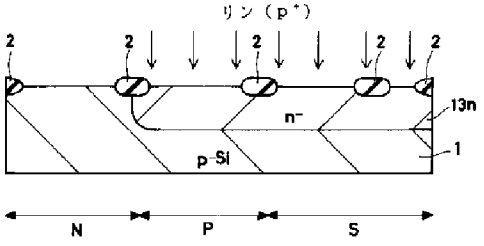
【図5】

図 5



【図6】

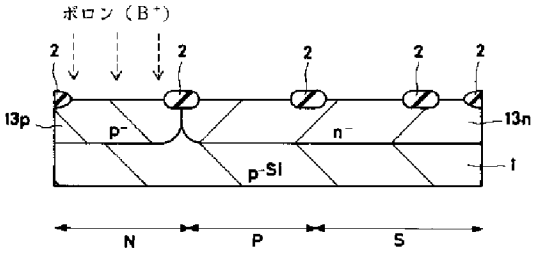
図 6



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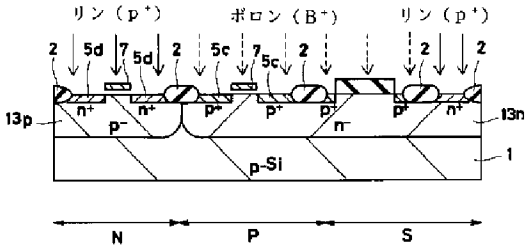
【図7】

図 7



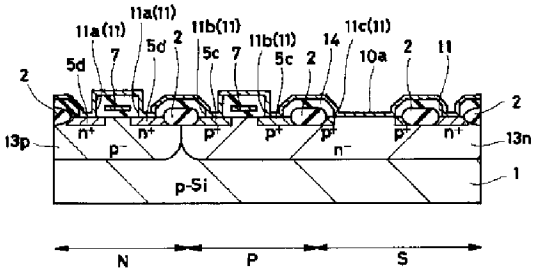
【図8】

図 8



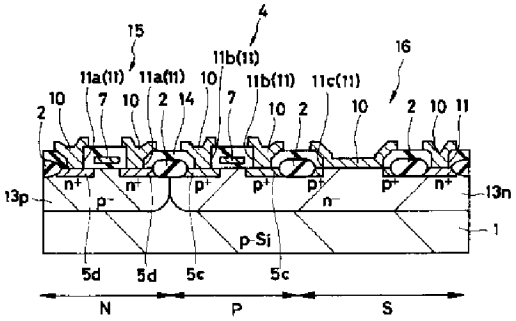
【図9】

図 9



【図10】

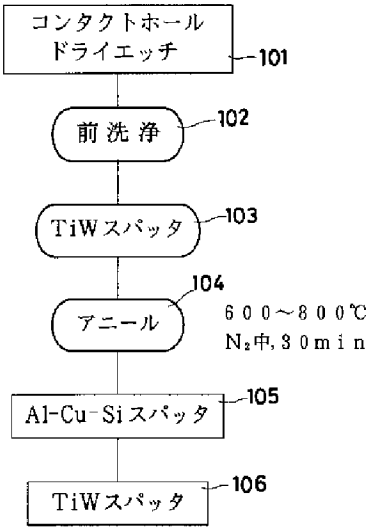
図10



16：ショットキバリヤダイオード

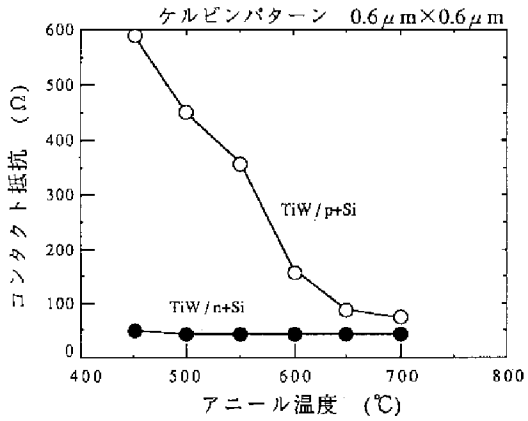
【図11】

図11



【図12】

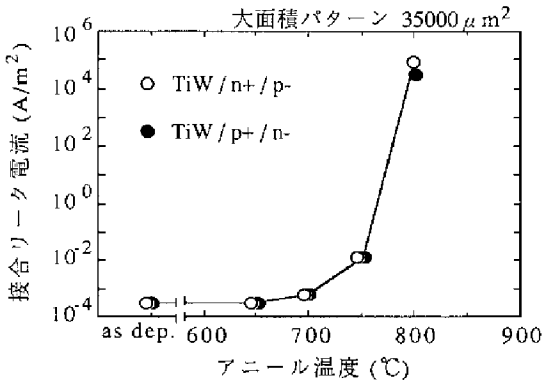
図12



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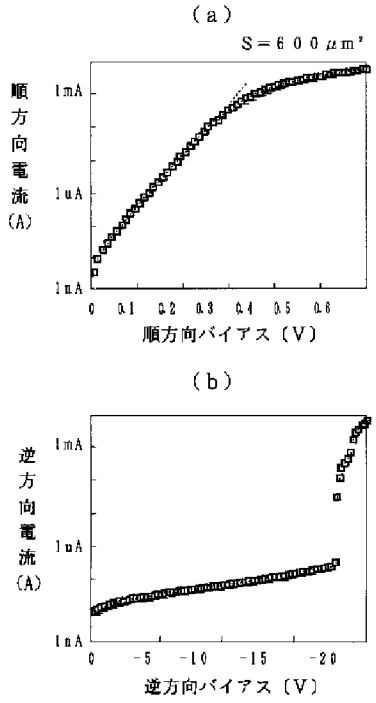
【図１３】

図 13



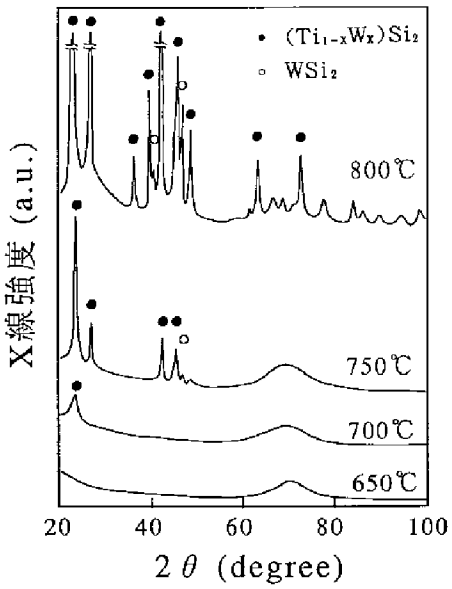
【図１４】

図 14



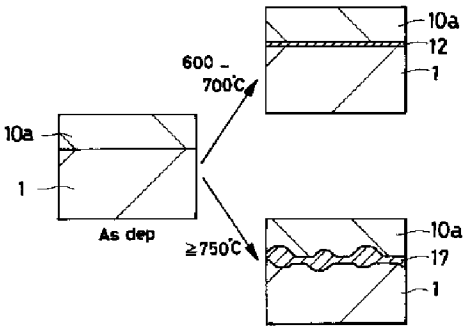
【図１７】

図 17



【図１９】

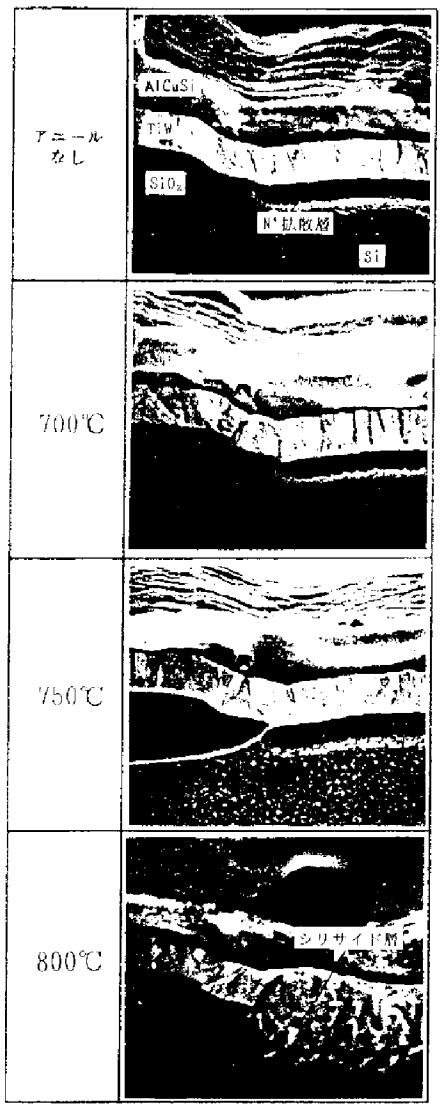
図 19



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【図１５】

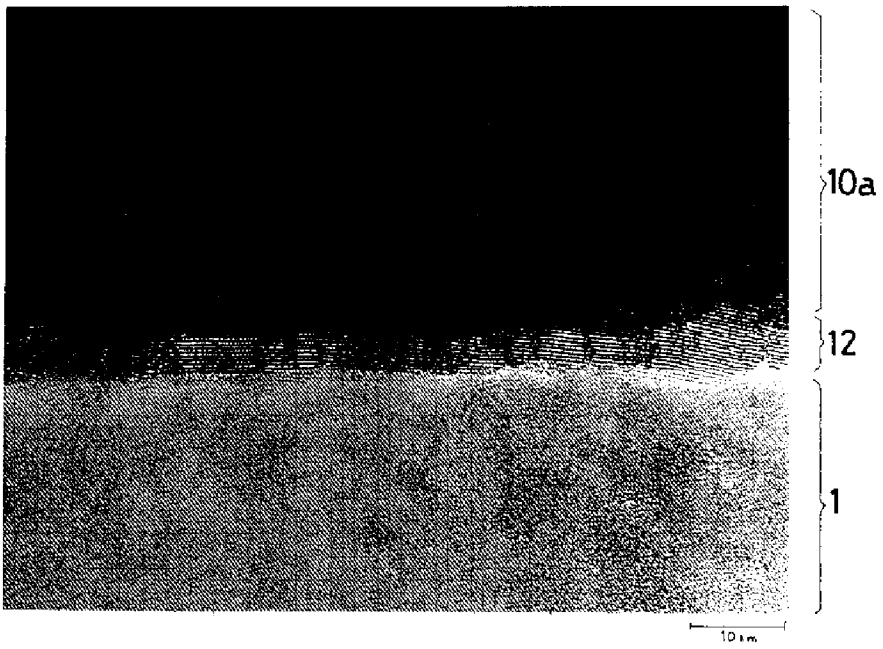
図 15



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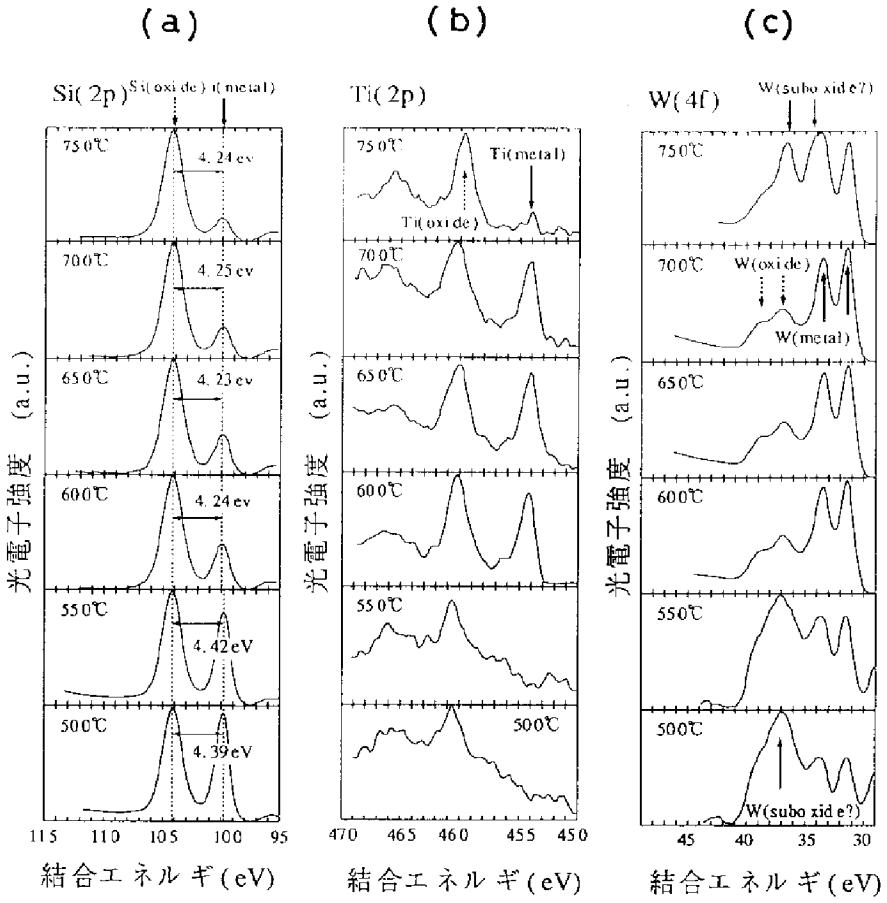
【図16】

図16



【図18】

図 18



フロントページの続き

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(72)発明者　岡　保志
東京都小平市上水本町５丁目22番１号　株式会社日立マイコンシステム内

(72)発明者　吉田　安子
東京都小平市上水本町５丁目20番１号　株式会社日立製作所武蔵工場内

(72)発明者　春田　亮
東京都小平市上水本町５丁目20番１号　株式会社日立製作所武蔵工場内

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JPH0661177A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURE THEREOF

Applicants: HITACHI LTD,HITACHI MICOM SYST KK

Inventors: HARUTA AKIRA,OKA YASUSHI,SUZUKI MASAYASU,TAKEDA TOSHIFUMI,YOSHIDA YASUKO

Classifications:

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CPC H01L2924/0002 (EP);

C-sets **H01L2924/0002, H01L2924/00 (EP);**

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SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURE THEREOF

Abstract

PURPOSE:To lessen a base metal film of a wiring which forms a semiconductor integrated circuit device and a semiconductor substrate in contact resistance between them. CONSTITUTION:A silicide layer 12 which is made of combined material composed of the component atoms of a base metal film 10a and a semiconductor substrate 1 and epitaxial to the semiconductor substrate 1 is provided to a contact surface between the base metal film 10a of a wiring 10 which forms a semiconductor integrated circuit device and a semiconductor layer 5 located on the semiconductor substrate 1.

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DESCRIPTION JPH0661177

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor integrated circuit device and a manufacturing technique thereof, and more particularly to a connection technique between a wiring forming the semiconductor integrated circuit device and a semiconductor substrate.

[0002]

2. Description of the Related Art Aluminum (Al) or its alloy is used as a wiring material of a semiconductor integrated circuit device. Al has a low resistivity, a low contact resistance with a p + type or n + type semiconductor layer formed on silicon (Si), and is easy to form and process. It is a wiring material for semiconductor integrated circuit devices. This is because it has excellent properties for use as.

[0003]
However, in the case of a single-layer Al wiring, a wiring disconnection defect caused by electromigration / stress migration or Si wiring deposited on the Al wiring side is accompanied by the miniaturization of the wiring or the connection hole in the semiconductor integrated circuit device. The problem of reliability of wiring has become remarkable, such as an increase in contact resistance with the semiconductor substrate.

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[0004]
Therefore, in recent years, by providing a base metal film made of, for example, titanium tungsten (TiW), titanium nitride (TiN), tungsten (W), molybdenum (Mo) or the like under the Al wiring, wiring disconnection defects and Si There is a tendency to prevent deposition and secure the reliability of wiring.

[0005]
However, when the underlying metal film was brought into direct contact with the Si substrate, it was brought into direct contact with the contact resistance, in particular, the p-type semiconductor layer forming the source / drain regions of the p-channel MOS • FET (hereinafter simply referred to as pMOS). In this case, there is a problem that the contact resistance at the contact portion becomes high.

[0006]

A possible solution is to increase the contact area, but in that case, it is against the tendency of miniaturization of the semiconductor integrated circuit device.

Further, it is conceivable to set the impurity concentration of the p-type semiconductor layer to a higher value, but in that case, there arises a problem of degrading the characteristics of the pMOS such as a short channel effect, which hinders miniaturization of the pMOS.

[0007]

Therefore, as a method of reducing the contact resistance between the underlying metal film and the p-type semiconductor layer without causing such a problem, for example, a platinum silicide (PtSi) layer is provided between the underlying metal film and the p-type semiconductor layer. There has been proposed a method of interposing a silicide layer having a low resistance such as the above.

This method is as follows, for example.

[0008]

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First, after forming a connection hole where the p-type semiconductor layer is exposed in the insulating film on the main surface of the Si substrate, a Pt film is deposited on the Si substrate.

Subsequently, the Si substrate is heat-treated to react Pt with Si at the contact portion between the Pt film and the p-type semiconductor layer to form a PtSi layer at the contact portion. Remove by. At this time, the PtSi layer remains on the p-type semiconductor layer in the connection hole. Then, a base metal film and an Al alloy film are sequentially deposited on the Si substrate, and then the laminated film thereof is patterned by a photolithography technique to form a wiring having a two-layer structure.

[0009]
The conventional technique of forming a base metal film in the lower layer of the Al wiring is described in, for example, "CMOS Device Handbook" P332 to P333, published by Nikkan Kogyo Shimbun Co., Ltd. on September 29, 1987. The necessity of providing barrier metal and the like are explained.

[0010]
By the way, a conventional low-resistance silicide layer such as a PtSi layer is provided at a contact portion between a base metal film forming a wiring and a p-type semiconductor layer of a semiconductor substrate. Does not conflict with the miniaturization of the semiconductor integrated circuit device, and since it is not necessary to increase the impurity concentration of the semiconductor layer, the short channel effect or the like does not occur, and the miniaturization of the element can be promoted. However, the present inventor has found that the steps of depositing the Pt film and the step of removing the Pt film are required, and thus the number of manufacturing steps of the semiconductor integrated circuit device is increased and the steps are complicated. It was

[0011]
The present invention has been made in view of the above problems, and an object thereof is to contact a base metal film forming a wiring with a semiconductor substrate without increasing or complicating a manufacturing process of a semiconductor integrated circuit device. It is to provide a technique capable of reducing resistance.

[0012]

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The above and other objects and novel features of the present invention will be apparent from the description of the specification and the accompanying drawings.

[0013]
The typical ones of the inventions disclosed in the present application will be briefly described as follows.

[0014]
That is, the invention according to claim 1 provides a wiring formed by sequentially laminating a base metal film and a conductor film on an insulating film on a semiconductor substrate from the lower layer, and a contact portion between the base metal film and the semiconductor substrate. In the semiconductor integrated circuit device structure, the base metal film and the constituent atoms of the semiconductor substrate are combined with each other, and a compound layer that is epitaxial is provided on the semiconductor substrate.

[0015]
According to a fourth aspect of the present invention, a step of forming a connection hole reaching the semiconductor substrate in an insulating film on the semiconductor substrate, and a step of depositing a base metal film for forming a wiring on the insulating film in which the connection hole is formed. A compound that is annealed to the semiconductor substrate and combines the constituent atoms of the base metal film and the semiconductor substrate at a contact portion between the base metal film and the semiconductor substrate to form an epitaxial film on the semiconductor substrate. A method of manufacturing a semiconductor integrated circuit device, comprising the steps of forming a layer and electrically connecting the underlying metal film and the semiconductor substrate.

[0016]
According to the invention described in claim 1, since the work function difference between the underlying metal film forming the wiring and the semiconductor layer of the semiconductor substrate can be reduced, the wiring and the p-type semiconductor layer are formed. It is possible to reduce the contact resistance of the.

[0017]
For this reason, for example, the impurity concentration of the p-type semiconductor layer forming the source / drain region of the pMOS can be made lower than before, so that the short channel effect of the pMOS can be suppressed and miniaturization of the pMOS can be promoted.

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Becomes

[0018]
According to the invention described in claim 4, for example, the step of depositing the Pt film, the step of removing the Pt film, and the like are not necessary, so that the number of manufacturing steps of the semiconductor integrated circuit device can be reduced and It is possible to simplify.

[0019]
Embodiment 1 FIG. 1 is a cross-sectional view of an essential part of a semiconductor integrated circuit device according to an embodiment of the present invention, and FIGS. 2 to 4 are cross-sectional views of an essential part of a semiconductor integrated circuit device shown in FIG. 5 is a graph showing the relationship between the contact resistance between the wiring and the semiconductor substrate and the annealing temperature.

[0020]

The semiconductor integrated circuit device according to the first embodiment is composed of, for example, a CMOS (Complimentary MOS) circuit.

FIG. 1 shows the pMOS portion of the semiconductor integrated circuit device of the first embodiment.

[0021]

The semiconductor substrate 1 is made of, for example, n-type Si single crystal, and the field insulating film 2 made of, for example, SiO2 is formed in the inactive region on the main surface thereof.

A channel stopper layer 3 is formed below the field insulating film 2.

Phosphorus, which is an n-type impurity, is introduced into the channel stopper layer 3.

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[0022]

On the main surface of the semiconductor substrate 1, for example, a pMOS 4 is formed in the active region surrounded by the field insulating film 2.

That is, the periphery of the pMOS 4 is defined by the field insulating film 2.

[0023]
The pMOS 4 includes semiconductor layers 5 and 5 formed on the semiconductor substrate 1, a gate insulating film 6 formed between the semiconductor layers 5 and 5, and a gate electrode 7 formed on the gate insulating film 6. have.

[0024]

The semiconductor layer 5 is formed by introducing, for example, boron, which is a p-type impurity, and is composed of, for example, a p-type semiconductor layer 5a and a p + -type semiconductor layer 5b.

That is, in the first embodiment, the pMOS 4 has an LDD (Lightly Doped Drain) structure.

[0025]

The gate insulating film 6 is made of, for example, SiO2.

The gate electrode 7 is formed by stacking, for example, two layers of conductor films 7a and 7b in order from the lower layer.

The conductor film 7a is made of, for example, doped polysilicon.

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The conductor film 7b is made of, for example, tungsten silicide (WSi2).

[0026]

A spacer 8 is formed on the side wall of the gate electrode 7.

The spacer 8 is an insulating film for forming the LDD structure and is made of, for example, SiO2.

[0027]

An interlayer insulating film 9 is deposited on the semiconductor substrate 1.

The interlayer insulating film 9 is made of, for example, SiO2, and the wiring 10 is formed thereon.

[0028]
The wiring 10 is formed by laminating a base metal film 10a and a conductor film 10b in order from the lower layer, and a part of the base metal film 10a is electrically connected to the semiconductor layer 5 through a connection hole 11 formed in the interlayer insulating film 9. It is connected to the.

[0029]
In the first embodiment, the constituent atoms of the base metal film 10a and the semiconductor layer 5 are combined at the contact portion between the base metal film 10a and the semiconductor layer 5, and the semiconductor substrate 1 is formed. On the other hand, a silicide layer (compound layer) 12 that becomes epitaxial is formed.

[0030]
That is, in the semiconductor integrated circuit device according to the first embodiment, the work function difference between the base metal film 10a and the semiconductor layer 5 is

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caused by providing the silicide layer 12 at the contact portion between the base metal film 10a and the semiconductor layer 5. Therefore, the contact resistance between the underlying metal film 10a and the semiconductor layer 5 can be reduced.

[0031]
The base metal film 10a is made of TiW containing titanium (Ti) in an amount of about 30 atm%, and has a thickness of about 150 nm, for example.

[0032]

However, the amount of Ti of the underlying metal film 10a is not limited to 30 atm% and can be variously changed, and for example, a range of 15 atm% or more and 60 atm% or less is preferable.

This is based on the following research results of the inventor.

[0033]
That is, for example, when the amount of Ti contained in the base metal film 10a is set to 15 atm% or less, the epitaxial silicide layer is not sufficiently formed at the contact portion between the base metal film 10a and the semiconductor layer 5, and the base metal film 10a is not formed. The contact resistance with the semiconductor layer 5 was not so low.

[0034]
On the other hand, when the contact resistance between the underlying metal film 10a and the semiconductor layer 5 is sufficiently reduced, the underlying metal film 10a is removed and the silicide layer 12 is analyzed by an X-ray microanalyzer. As a result, the molar ratio of Ti and W is It was about 6 to 4.

[0035]
Although the composition ratio of Ti and W is slightly different even if the same sputtering target is used due to the difference in the sputtering apparatus and the like, from the above analysis results, if TiW containing Ti of about 60 atm% or less is used, the silicide layer 12 is formed on the semiconductor substrate 1. It turned out that it can be made epitaxial.

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[0036]
However, the underlying metal film 10a is not limited to TiW and can be variously changed, and may be TaW, TiTa, or the like.

[0037]
The conductor film 10b is made of, for example, Al or Al-Si-copper (Cu) alloy and has a thickness of, for example, about 400 nm.

[0038]
The silicide layer 12 is made of, for example, a compound of Ti, W and Si, and its thickness is, for example, about 3 nm.

[0039]

Although not shown, a surface protective film is deposited on the wiring 10 and the interlayer insulating film 9.

The surface protection film is composed of, for example, an insulating film made of SiO2 deposited by a plasma CVD method and an insulating film made of silicon nitride (Si3 N4) deposited by a plasma CVD method in this order from the lower layer. There is.

[0040]

Next, a method of manufacturing the semiconductor integrated circuit device according to the first embodiment will be described with reference to FIGS.

In the first embodiment, the description of the manufacturing process of the n-channel MOS is omitted to simplify the description.

[0041]

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First, as shown in FIG. 2, the non-active region on the main surface of the semiconductor substrate 1 made of, for example, n-type Si single crystal is selectively oxidized to form the field insulating film 2 in that region.

At this time, at the same time, the n-type channel stopper layer 3 is formed under the field insulating film 2.

[0042]
Subsequently, on the main surface of the semiconductor substrate 1, the active region whose periphery is defined by the field insulating film 2 is oxidized, and the gate insulating film 6 is formed in that region.

[0043]
After that, a conductor film made of doped polysilicon and a conductor film made of WSi2 are deposited on the semiconductor substrate 1, and then the conductor films are patterned by a photolithography technique to form a gate electrode 7.

[0044]
Next, using the gate electrode 7 as a mask, the semiconductor substrate 1 is lightly ion-implanted with, for example, p-type impurity such as boron, to form the p-type semiconductor layer 5a.

[0045]
Subsequently, after depositing an insulating film (not shown) on the semiconductor substrate 1, the insulating film is etched back to form the spacer 8 on the side wall of the gate electrode 7.

[0046]

After that, a thin oxide film is formed on the entire surface of the semiconductor substrate 1, and then the semiconductor substrate 1 is ion-implanted with, for example, p-type impurities such as boron by using the gate electrode 7 and the spacer 8 as a mask to form a p + -type semiconductor layer. 5b is formed.

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In this way, the pMOS 4 is formed on the semiconductor substrate 1.

[0047]
Next, as shown in FIG. 3, an interlayer insulating film 9 made of, for example, SiO2 is deposited on the semiconductor substrate 1 by the CVD method or the like, and then the interlayer insulating film 9 is formed in the interlayer insulating film 9 by the photolithography technique to reach the semiconductor layer 5. Perforate.

[0048]
Then, a metal film 10a1 made of TiW for forming the base metal film 10a (see FIG. 1) is deposited on the semiconductor substrate 1 by a sputtering method or the like.

[0049]

The amount of Ti in the metal film 10a1 at this time is, for example, about 30 atm% for the reason described above.

The thickness of the metal film 10a1 is, for example, about 150 nm.

[0050]
Then, the semiconductor substrate 1 is housed in an ordinary furnace body (not shown), and annealed at 650 ° C. for 30 minutes in a nitrogen atmosphere, for example, to combine the TiW of the metal film 10a1 with the Si of the semiconductor layer 5. Then, as shown in FIG. 4, a silicide layer 12 is formed at the contact portion between the metal film 10a1 and the semiconductor layer 5.

[0051]
That is, in the first embodiment, the step of depositing the Pt film and the step of removing the Pt film as in the conventional technique of forming the PtSi film at the contact portion between the base metal film 10a and the semiconductor layer 5 are unnecessary. In addition, the manufacturing process of the semiconductor integrated circuit device can be reduced and the process can be simplified.

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[0052]

The silicide layer 12 formed by annealing was epitaxial with respect to the semiconductor substrate 1 and was a thin layer having a thickness of about 3 nm.

Therefore, the stress on the semiconductor substrate 1 and the semiconductor layer 5 due to the volume change accompanying the chemical reaction when forming the silicide layer 12 can be small, and an increase in junction leak due to the stress is not observed, and the pMOS 4 Showed good electrical characteristics.

[0053]

Furthermore, by annealing, the resistance of the conductor film 10b (see FIG. 1) becomes lower than that in the case where annealing is not performed, and the resistance of the wiring 10 can be lowered.

This is because the low-reactive Ti oxide or the like is segregated on the surface of the metal film 10a1 due to the annealing, so that the conductor film 10b made of Al and the metal film 10a1 deposited on the metal film 10a1 thereafter are separated. It is assumed that as a result of suppressing the reaction, the original conductivity of the conductor film 10b made of Al was secured.

[0054]

However, the annealing temperature is not limited to 650 ° C and can be changed variously, for example, 550 ° C to 750 ° C, ideally, for example, a range of 600 ° C or more and 700 ° C or less is preferable. ..

[0055]

FIG. 5 shows the relationship between the contact resistance of the base metal film 10a and the contact portion of the semiconductor layer 5 and the annealing temperature.

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As shown in FIG. 5, it can be seen that the contact resistance between the underlying metal film 10a and the semiconductor layer 5 significantly decreases at about 600 ° C. or higher.

[0056]

However, according to the research by the present inventor, when the annealing temperature is set to 750 ° C. or higher, nonuniform crystal grains having a diameter of several tens nm are observed in the silicide layer 12.

As a result of observing the cross section of the sample in this case with a transmission electron microscope or the like, strong strain is observed in the p + -type semiconductor layer 5b around the connection hole 11, which causes the p + -type semiconductor layer 5 and the semiconductor substrate 1 to be separated from each other. It was found that the joint was destroyed.

[0057]

Further, according to the research conducted by the present inventor, the silicide layer of each sample when the annealing temperature is 600 ° C. and 700 ° C. is removed, and the underlying metal film is removed after each annealing process to perform photoelectron spectroscopy. As a result of investigation by a method or the like, it was found that the silicide layer in that case has substantially the same surface state as the good silicide layer 12 when the annealing temperature is 650 ° C.

[0058]

Therefore, since it is assumed that the temperature varies depending on the annealing method and the like, it cannot be specified unconditionally, but if the annealing temperature is at least in the range of, for example, 600 ° C. to 700 ° C. A good silicide layer 12 is formed.

[0059]

After the silicide layer 12 is formed by the annealing process, a conductor film (not shown) made of, for example, an Al--Si--Cu alloy is deposited on the metal film 10a1 and then the conductor film and the metal film 10a1 are formed by photolithography. The wiring 10 shown in FIG. 1 is formed by patterning.

[0060]

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Thereafter, although not shown, a SiO2 film and a Si3 N4 film are deposited on the wiring 10 and the interlayer insulating film 9 by, for example, a plasma CVD method or the like to form a surface protective film on the semiconductor substrate 1.

[0061]
As described above, according to the first embodiment, the following effects can be obtained.

[0062]
(1)

.

By providing the silicide layer 12 that becomes epitaxial with respect to the semiconductor substrate 1 at the contact portion between the base metal film 10a forming the wiring 10 and the semiconductor layer 5 forming the pMOS 4, the base metal film 10a and the semiconductor layer 5 are formed. Since it is possible to reduce the work function difference between the semiconductor layer 5 and the base metal film 10a, it is possible to reduce the contact resistance between the underlying metal film 10a and the semiconductor layer 5.

[0063]
(2)

.

By the above (1), the impurity concentration of the p + -type semiconductor layer 5b can be made lower than before, so that the short channel effect of the pMOS 4 can be suppressed and the miniaturization of the pMOS 4 can be promoted. ..

Therefore, it is possible to improve the degree of element integration of the semiconductor integrated circuit device.

[0064]

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(3)

.

By forming the silicide layer 12 by annealing, a step of depositing a Pt film or a step of removing the Pt film as in the case of the conventional technique of forming a PtSi film at the contact portion between the base metal film 10a and the semiconductor layer 5 is performed. Since it is unnecessary, the manufacturing process of the semiconductor integrated circuit device can be reduced as compared with the case of the conventional technique, and the process can be simplified.

[0065]
(4)

.

The base metal film 10a is made of, for example, TiW containing Ti of 15 atm% or more and 60 atm% or less, ideally 30 atm%, and the annealing temperature is, for example, 550 ° C. to 750 ° C., ideally 600 ° C. By annealing in the range of ° C to 700 ° C, it is possible to form a very thin silicide layer 12 of, for example, about 3 nm, which is epitaxial with respect to the semiconductor substrate 1.

[0066]
(5)

.

By the above (4), the stress on the semiconductor substrate 1 and the semiconductor layer 5 due to the volume change accompanying the chemical reaction when forming the silicide layer 12 can be small, and the increase in the junction leak due to the stress is also observed. Therefore, it is possible to obtain good electrical characteristics in the pMOS4.

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[0067]

[Embodiment 2] FIGS. 6 to 10 are cross-sectional views of essential parts of a semiconductor substrate during a manufacturing process of a semiconductor integrated circuit device according to another embodiment of the present invention, and FIG. FIG. 12 is a graph showing the annealing temperature dependence of the contact resistance between the wiring and the p + type semiconductor layer in the contact hole, FIG. 13 is a graph showing the annealing temperature dependence of the junction leakage current, and FIG. a) is a graph showing a forward current-voltage characteristic of the Schottky barrier diode, FIG. 14B is a graph showing a reverse current-voltage characteristic of the Schottky barrier diode, and FIG. 15 is a graph showing post-annealing observed by SEM. 16 is a cross-sectional view of the silicide layer, FIG. 16 is a cross-sectional view of the interface between the underlying metal film after annealing and the semiconductor substrate observed by TEM, FIG. 17 is a graph showing an X-ray diffraction spectrum of the silicide layer, and FIG.) To (c) are graphs showing the ESCA spectrum of the silicide layer, and FIG. 19 is an explanatory view showing a model of silicidation of the underlying metal film.

[0068]

The method for manufacturing the semiconductor integrated circuit device according to the second embodiment is, for example, a method for manufacturing a semiconductor integrated circuit device having a CMOS circuit and a Schottky barrier diode (hereinafter abbreviated as SBD) on the same semiconductor substrate.

Hereinafter, a method of manufacturing the semiconductor integrated circuit device according to the second embodiment will be described with reference to FIGS.

[0069]

The semiconductor substrate 1 shown in FIG. 6 is a (100) substrate made of, for example, p-type Si single crystal and having a resistivity of 10 Ω · cm.

[0070]

First, after the field insulating film 2 is formed on the semiconductor substrate 1 by the LOCOS method or the like, phosphorus (P), which is an n-type impurity, is ion-implanted into the pMOS formation region P and the SBD formation region S. To form the n-well 13n.

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Note that N in FIG. 6 indicates an nMOS formation region.

[0071]
Subsequently, as shown in FIG. 7, for example, boron (B) which is a p-type impurity is ion-implanted into the nMOS formation region N to form a p-well 13p.

[0072]
Thereafter, as shown in FIG. 8, after the gate electrode 7 is formed, for example, boron is ion-implanted in the pMOS formation region P and phosphorus is ion-implanted in the nMOS formation region N to form p + forming the source and drain. The semiconductor layers 5c and 5c and the n + semiconductor layers 5d and 5d are formed.

[0073]
Next, as shown in FIG. 9, after forming the insulating film 14 on the semiconductor substrate 1, the insulating film 14 reaches the p + semiconductor layer 5c, the n + semiconductor layer 5d, and the n well 13n in the SBD formation region S, respectively. The connection holes 11a to 11c are opened.

[0074]

Subsequently, a base metal film 10a made of, for example, TiW is deposited on the semiconductor substrate 1, and then silicidation is performed.

As a result, a silicide layer (compound layer) not shown in FIG. 9 is formed between the underlying metal film 10a and the p + type semiconductor layer, the n + type semiconductor layer and the n well 13n, as in the first embodiment. It is formed.

The silicidation will be described later.

[0075]

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After that, as shown in FIG. 10, for example, AlCuSi and TiW are sequentially deposited to form the wiring 10 made of, for example, TiW / AlCuSi / TiW.

As a result, the n-channel MOS • FET 15 is formed in the nMOS formation region N, the pMOS 4 is formed in the pMOS formation region P, and the Schottky barrier diode (SBD) 16 is formed in the Schottky barrier diode (SBD) formation region S.

[0076]
FIG. 11 shows a process flow of TiW silicidation of Example 2, for example.

[0077]
After the connection hole 11 (see FIGS. 9 and 10) is formed by the dry etching method or the like (step 101), a wet pretreatment is performed (step 102), and then, for example, TiW is formed on the semiconductor substrate 1 by the sputtering method. (Step 103).

[0078]

For sputtering, for example, a normal DC sputtering device (not shown) was used, and for the target, for example, a 10 wt% Ti-W target was used.

Then, using a general horizontal furnace body (not shown), for example, in an N2 atmosphere, annealing was performed at 500 to 800 DEG C. for 30 minutes (step 104).

[0079]
Finally, for example, AlCuSi and TiW were sequentially formed by, for example, a sputtering method to form the wiring 10 (steps 105 and 106).

[0080]
Next, evaluation items and evaluation methods of the semiconductor integrated circuit device thus formed will be described.

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[0081]
As the electrical characteristics, contact resistance, junction leak current and SBD characteristics were measured.

[0082]

For the contact resistance, for example, a Kelvin method was used to measure a contact hole of about 0.6 μm × 0.6 μm.

For the junction leak current, a reverse current was measured using a large-area p / n junction of, for example, 35,000 μm 2.

As for the SBD characteristics, for example, an SBD having an area of 600 .mu.m.sup.2 was produced, and the forward characteristics and the backward characteristics were measured.

[0083]
In order to clarify the physical phenomenon of silicidation, the cross section of the silicide layer was observed with a scanning electron microscope (SEM) and a transmission electron microscope (TEM).

[0084]
The TiW / Si interface was analyzed by X-ray photoelectron spectroscopy (ESCA) and X-ray diffraction (XRD).

[0085]
Next, the electrical characteristics of the semiconductor integrated circuit device based on the evaluation will be described.

[0086]

FIG. 12 shows the annealing temperature dependence of the contact resistance.

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The contact resistance with respect to the p + type semiconductor layer (p + Si) is as high as about 600Ω without annealing, but the resistance becomes lower as the annealing temperature is increased, and for example, a value of 100Ω or less is obtained at 650 ° C or higher. ..

The contact resistance with respect to the n + type semiconductor layer (n + Si) is as low as about 50Ω without annealing, and there is almost no change even after annealing.

[0087]

FIG. 13 shows the annealing temperature dependence of the junction leakage current.

Leakage current is as small as up to 700 ° C without annealing in both n + / p junction and p + / n junction, but a sharp increase is seen after annealing at 750 ° C or higher. Be done.

[0088]
From the above results, the annealing was performed at about 650 ° C. where the contact resistance was sufficiently low and the junction leakage current did not increase, and the measurement was performed on the samples manufactured under these conditions.

[0089]

An example of the measurement result of the SBD characteristic in that case is shown in FIGS.

FIG. 14A shows the result of the forward characteristic and FIG. 14B shows the result of the backward characteristic.

According to thermionic emission theory, the forward current of the SBD is expressed by the following equation (SM Sze, Physics of Semiconductor Devices, 2nd ed.

(Wiley, New York, 1981)).

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[0090]

J = Js [exp (qV / nkT) -1] Js = A * T2 exp (-q ϕ B / kT) where q is elementary charge, k is Boltzmann constant, T is absolute temperature, and A * is effective. Richardson constant, ϕ B is the barrier height.

n is a correction coefficient from an ideal value, and ideally n = 1.

[0091]

From FIG. 14A, for example, ϕ B = 0.61 eV and n = 1.03 were obtained.

ϕ B = 0.61 eV is a value between ϕ B = 0.60 eV of TiSi2 and ϕ B = 0.65 eV of WSi2 (SM Sze, Physics of Semiconductor Devices, 2nd ed.

(Wiley, New York, 1981)).

Further, it can be seen that n = 1.03 is close to the ideal value and has a good SBD characteristic.

[0092]

Next, FIG. 15 shows a cross-sectional SEM photograph of the connection hole portion annealed at 700 to 800 ° C., for example.

After polishing the cross section of the semiconductor substrate, the diffusion layer (n @ + semiconductor layer) was etched by immersing in a HF: HNO3: CH3 COOH mixed solution and observed.

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[0093]

For example, it can be seen that at 800 ° C., the silicide layer grows beyond the thickness of the diffusion layer, which increases the junction leakage current.

On the other hand, at, for example, 750 ° C. or lower, no clear formation of the silicide layer is observed.

[0094]

Further, FIG. 16 shows a TEM photograph of a cross section of the TiW / Si interface when annealing is performed at 650 ° C. for 30 minutes.

A silicide layer 12 having a thickness of about 4 to 5 nm is epitaxially formed between the semiconductor substrate 1 and the underlying metal film 10a made of TiW, and the lattice plane spacing thereof is about 0.39 nm.

[0095]

This is due to WSi2 (002) 0.391 nm (F. d'Heurle, et al., J. Appl.

Phys., Vol. 51, p.

5976 (1980), S. Murarka, et al., J. Appl.

Phys., Vol. 52, p. 7450 (1981)) or Ti3 W2 Si10 (100) at 0.399 nm (F. Nova, et al., J. Appl. Phys., Vol.54, p. 2434 (1983), JM Harris, et al., J. Electrochem. Soc., Vol. 123, p. 120 (1976)).

[0096]

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Next, FIG. 17 shows the XRD spectrum of the silicide layer. For example, after TiW silicidation, TiW on the surface was removed with, for example, H 2 O 2, and measurement was performed using Cu k α .

[0097]

For example, at 650 ° C., no clear peak due to silicidation is observed, but at 700 ° C., a slight peak of (Ti1-x Wx) Si2 is observed at 2 θ =22 ° . Further, for example, at 750 ° C. or higher, strong peaks of (Ti1-x Wx) Si2 and WSi2 are observed, and it is understood that a thick mixed crystal of (Ti1-x Wx) Si2 and WSi2 is formed.

[0098]

Next, ESCA spectra of the surface of the semiconductor substrate after removing TiW with, for example, H2 O2 are shown in FIGS. For example, changes in the spectra of Si (2p), Ti (2p), and W (4f) are shown with respect to the annealing temperature of 500 ° C to 750 ° C.

[0099]

First, focusing on the spectrum of Si (2p) in FIG. 18A, the binding energy difference (chemical shift) between the Si (metal) peak and the Si (oxide) peak is 4.40 eV at 550 ° C. or lower, for example. On the other hand, for example, at 600 ° C. or higher, it is 4.24 eV, which is smaller than 0.16 eV. This result indicates that silicide was generated at 600 ° C. or higher, for example.

[0100]

In the spectra of Ti (2p) and W (4f) of FIGS. 18 (b) and (c), only the peak of oxide is observed up to 550 ° C., while the peak of 600 ° C. is observed. Above, the peaks of metal and oxide are observed. This suggests that a silicide layer of Ti and W is formed at 600 ° C or higher, for example. The oxide peak was observed not only because of oxidation in air but also because the TiW was removed by H2O2.

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[0101]

Next, for example, a model of TiW silicidation is shown in FIG. After the base metal film 10a made of TiW is formed on the semiconductor substrate 1, the silicide layer 12 is formed between the base metal film 10a and the semiconductor substrate 1 by annealing, for example, at a temperature of 600 ° C. or higher.

[0102]

From the results of TEM and ESCA, it was found that the ternary alloy of Ti, W and Si (Ti1-xWx) Si2 was epitaxially formed in the range of 600 to 700 ° C. The formation of the silicide layer 12 reduces the contact resistance.

[0103]

S. E. Babcock et al., When annealing at 500 to 900 ° C, 25 nm of TiSi2 was formed at the TiW / Si interface in the case of Ti-rich TiW, but at 750 ° C in the case of W-rich TiW. It is reported that only thick (Ti1-x Wx) Si2 or WSi2 is formed by the above (SE Babcock, et al., J. Appl. Phys., Vol. 53, p. 6898 (1982), S. E. Babcock, et al., J. Appl. Phys., Vol. 59, p. １５９９（１９８６））。

[0104]

This is probably because their analysis means were XRD and RBS, and therefore a very thin (Ti1-xWx) Si2 silicide layer of about 4 nm could not be observed. Onishi et al. Reported that TiSi2 was formed at the TiW / Si interface by TiW lamp annealing (RTA) (Shigeo Onishi, et al., 2nd Symposium of ECS Japan Chapter, Al wiring technology in ULSI). Problems >> p. ５０（１９８９））。

[0105]

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Further, in the case of annealing at 750 ° C. or higher, the silicide layer becomes a mixed crystal of polycrystalline (Ti1-x Wx) Si2 and WSi2, and the film is rapidly thickened. Then, this thick silicide layer 17 penetrates through the diffusion layer, causing an increase in junction leak current.

[0106]

The difference in silicidation due to annealing of TiW / Si and W / Si has already been reported (M. Suzuki, et al., 1991 SSDM p. 213 (1991)), as described above, an epitaxial layer of (Ti1-x Wx) Si2 is formed in TiW / Si, whereas an epitaxial growth is not formed in W / Si and polycrystalline WSi2 is formed. Therefore, a junction leak occurs at a low temperature and the process window becomes narrow. That is, TiW silicidation is a process suitable for fine ULSI as compared with W.

[0107]
As described above, according to the second embodiment, the silicidation of TiW deposited on the semiconductor substrate 1 makes it possible to simultaneously obtain a low contact resistance and a good SBD characteristic.

[0108]

As a result, in the connection hole 11b of, for example, 0.6 μm, a low contact resistance of, for example, 100Ω or less can be obtained even for the p + type semiconductor layer 5c.

Further, for example, it becomes possible to obtain the SBD having the barrier height $\phi B = 0.61$ eV.

[0109]
In particular, at the time of silicidation of TiW, a ternary alloy (Ti1-xWx) Si2 is epitaxially formed at the TiW / Si interface by annealing at 600 to 700 ° C, thereby reducing the contact resistance. And it is possible to obtain good SBD characteristics.

[0110]
Further, by forming the silicide layer 12 by annealing, similarly to the first embodiment, a step of

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depositing a Pt film as in the case of the prior art in which a PtSi film is formed at the contact portion between the base metal film 10a and the semiconductor layer. Since the process of removing the Pt film and the Pt film is not required, the manufacturing process of the semiconductor integrated circuit device can be reduced and the process can be simplified as compared with the conventional technique.

[0111]
Although the invention made by the inventor has been specifically described based on the embodiments, the invention is not limited to the first and second embodiments, and various modifications can be made without departing from the scope of the invention. Needless to say.

[0112]

For example, in the first and second embodiments, the case where the wiring is configured by laminating the conductor film made of Al or the like on the base metal film made of TiW has been described. TiMo, TiTa, ZrW, ZrMo, ZrTa, HfW, HfMo, HfTa may be used as the metal film.

This is because Ti, Zr, and Hf of IVa group can reduce the SiO2 at the metal / Si interface, and thus work uniformly to cause the interfacial reaction, and Ta, W, and Mo have a slower rate of silicidation than the IVa group metal. , Only a thin silicide layer is formed.

Further, since the silicide layer is thin, it can exist stably on Si even if the lattice strain is large.

[0113]

Further, for example, the wiring may be formed by stacking a W film on the base metal film.

In these cases, after patterning the wiring, annealing for forming a silicide layer may be performed.

[0114]

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Further, in the first and second embodiments, the case where the annealing for forming the silicide layer is performed in the furnace has been described, but the present invention is not limited to this, and, for example, a ramp ranier method may be used. At the time of lamp annealing, the atmosphere in the processing chamber is, for example, a nitrogen atmosphere or an ammonia atmosphere.

[0115]

When lamp annealing is used, the annealing time can be shortened to about 1 minute. Further, in this case, a thin silicide layer was formed even if annealing was performed at, for example, 750 ° C., and no increase in junction leak was observed.

[0116]
In the lamp anneal, when a nitrogen atmosphere was used, Ti oxide was deposited on the surface of the underlying metal film made of TiW or the like, so that the wiring resistance could be reduced as compared with the case where the annealing was not performed.

[0117]
Further, when the lamp annealing is performed in an ammonia atmosphere, TiN, tungsten nitride, or the like is formed on the surface of the underlying metal film made of TiW, etc., and the reactivity with the conductor film made of Al is higher than that in the case of annealing in a nitrogen atmosphere. And the wiring resistance was reduced.

[0118]
In the above description, the case where the invention made by the present inventor is mainly applied to the semiconductor integrated circuit device configured by the CMOS circuit which is the field of application of the background has been described, but the invention is not limited to this and various applications are possible. However, the present invention can be applied to other semiconductor integrated circuit devices such as a semiconductor integrated circuit device formed of a bipolar transistor and a semiconductor integrated circuit device formed of BiC-MOS (Bipolar CMOS).

[0119]
The effects obtained by the typical ones of the inventions disclosed in this application will be

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briefly described as follows.

[0120]
(1)

.

That is, according to the first aspect of the invention, the work function difference between the underlying metal film forming the wiring and the p-type semiconductor layer of the semiconductor substrate can be reduced, so that the wiring and the p-type semiconductor layer are separated from each other. It is possible to reduce the contact resistance.

Therefore, for example, the impurity concentration of the p-type semiconductor layer forming the source / drain region of the pMOS can be reduced, so that the short channel effect of the pMOS can be suppressed and the miniaturization of the pMOS can be promoted.

Therefore, the degree of element integration of the semiconductor integrated circuit device can be improved.

[0121]
(2)

.

According to the invention of claim 4, for example, the step of depositing the Pt film, the step of removing the Pt film, and the like are not necessary, so that the number of manufacturing steps of the semiconductor integrated circuit device can be reduced and the steps are simplified. Is possible. That is, it is possible to reduce the contact resistance between the wiring and the semiconductor substrate without increasing or complicating the manufacturing process of the semiconductor integrated circuit device.

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CLAIMS JPH0661177

1.
A wiring is formed by laminating a base metal film and a conductor film in order from the lower layer on an insulating film on a semiconductor substrate, and each of the base metal film and the semiconductor substrate is provided at a contact portion between the base metal film and the semiconductor substrate. 2. A semiconductor integrated circuit device comprising a compound layer, which is formed by combining the constituent atoms of the above, and is epitaxial with respect to the semiconductor substrate.

2.
2. The semiconductor integrated circuit device according to claim 1, wherein the underlying metal film is titanium tungsten.

3.
3. The semiconductor integrated circuit device according to claim 1, wherein the contact portion is formed in a semiconductor layer for forming a source / drain of a MIS • FET or a semiconductor layer for forming a Schottky contact of a Schottky barrier diode.

4.
A step of forming a connection hole reaching the semiconductor substrate in an insulating film on the semiconductor substrate; a step of depositing a base metal film for forming a wiring on the insulating film in which the connection hole is formed; and an annealing process for the semiconductor substrate. And forming a compound layer that becomes epitaxial with respect to

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the semiconductor substrate by combining respective constituent atoms of the base metal film and the semiconductor substrate at a contact portion between the base metal film and the semiconductor substrate. And a step of electrically connecting the semiconductor substrate to a semiconductor substrate.

5.

5. The method of manufacturing a semiconductor integrated circuit device according to claim 4, wherein a Schottky contact portion is formed at a contact portion between the compound layer and the semiconductor substrate at the same time when the base metal film and the semiconductor substrate are connected.

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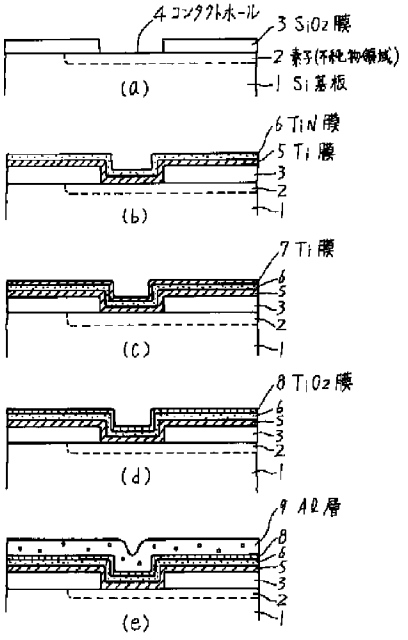
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(71)出願人　000005223
富士通株式会社
神奈川県川崎市中原区上小田中1015番地
(71)出願人　000237617
富士通ヴイエルエスアイ株式会社
愛知県春日井市高蔵寺町２丁目1844番２
(72)発明者　千藤　俊彦
愛知県春日井市高蔵寺町二丁目1844番２
富士通ヴイエルエスアイ株式会社内
(74)代理人　弁理士　井桁　貞一

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】
【目的】　半導体装置及びその製造方法に関し，半導体基板と配線層の反応を阻止しかつコンタクト不良を防止するバリア層を有する半導体装置及びその製造方法を目的とする。
【構成】　素子の形成された半導体基板１上に絶縁膜３を形成し，絶縁膜３にコンタクトホール４を形成する工程と，コンタクトホール４内に半導体基板１に接続する第１のチタン膜５，窒化チタン膜６，第２のチタン膜７による導体多層膜５，６，７を形成する工程と，第２のチタン膜７を全部あるいは一部酸化して酸化チタン膜８を形成する工程と，酸化チタン膜８上に配線層９を形成する工程とを有するように構成する。

実施例を示す工程順断面図



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1

【特許請求の範囲】

【請求項1】　半導体基板(1) と，該半導体基板(1) 上に形成された配線層(9) と，該半導体基板(1) と該配線層(9) に接して介在するバリア層(5, 6, 8) とを有する半導体装置であって，該バリア層(5, 6, 8) はチタン膜(5)，窒化チタン膜(6)，酸化チタン膜(8)による三層構造を含み，前記酸化チタン膜(8) は前記半導体基板(1) と前記配線層(9) 間の電気的導通を保ちかつ両者間の化学的反応を阻止する厚さを有することを特徴とする半導体装置。

【請求項2】　前記半導体基板(1) はＳｉ基板であり，前記配線層(9) はＡｌ層或いはＡｌを主成分とする合金層であることを特徴とする請求項1記載の半導体装置。

【請求項3】　素子の形成された半導体基板(1) 上に絶縁膜(3) を形成し，該絶縁膜(3) にコンタクトホール(4) を形成する工程と，該コンタクトホール(4) 内に該半導体基板(1) に接続する第1のチタン膜(5)，窒化チタン膜(6)，第2のチタン膜(7) による導体多層膜(5, 6, 7) を形成する工程と，該第2のチタン膜(7) を全部あるいは一部酸化して酸化チタン膜(8) を形成する工程と，該酸化チタン膜(8) 上に配線層(9) を形成する工程とを有することを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体装置及びその製造方法に係り，特に，半導体基板上にバリア層を介して配線層の形成された半導体装置及びその製造方法に関する。

【０００２】半導体基板に形成された多数の素子上に，通常，層間絶縁膜を介してＡｌ等の配線層を形成する。配線層は層間絶縁膜に形成さたコンタクトホール内で半導体基板と接続する。

【０００３】ところで，Ｓｉ基板に形成される素子の微細化，デバイスの高集積化に伴い，配線層のＡｌが基板のＳｉと反応し，接合破壊を起こすといった問題の発生することがある。

【０００４】そのため，近年ではＡｌ配線層とＳｉ基板間の反応を防止するため，スルーホール内にバリア層を設けている。

【０００５】

【従来の技術】図2(a) ～(d) は従来例を示す工程順断面図である。以下，これらの図を参照しながら，従来例について説明する。

【０００６】図2(a) 参照

素子（不純物領域）２の形成されたＳｉ基板１に，層間絶縁膜としてSiO_2 膜３を形成し，そのSiO_2 膜３に素子２を露出するコンタクトホール４を形成する。

【０００７】図2(b) 参照

スパッタ法により全面にチタン（Ｔｉ）膜５及び窒化チタン（ＴｉＮ）膜６をこの順に形成する。

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【０００８】図2(c) 参照

この基板を加熱炉に入れ，酸素と窒素を含む雰囲気中で450 ℃，３０分程度の加熱を行うことにより，ＴｉＮ膜６の表面に酸化窒化チタン（ＴｉＮＯ）膜10を形成する。

【０００９】図2(d) 参照

ＴｉＮＯ膜10上に配線層としてＡｌ層９を形成する。Ｔｉ膜５，ＴｉＮ膜６はいわゆるバリア層を形成し，Ａｌ層９とＳｉ基板１の電気的導通を保ち，かつＡｌ層９のＡｌとＳｉ基板１のＳｉが反応するのを防ぐ作用をもつものであるが，ＡｌとＳｉの反応を防止する機能が十分でないため，ＴｉＮＯ膜10を形成してその機能を向上することが行われている。

【００１０】しかし，そのようにしても，その後の加熱を含む工程を経て半導体装置が完成した時，バリア層としての機能が失われることがある。図３は従来の問題点を示す断面図である。

【００１１】Ａｌ層９形成後の工程では，Ａｌが融解しない温度で各種の加熱が行われるがその加熱工程において，バリア層が十分機能せずに，コンタクトホール部でＳｉ基板１のＳｉが配線層９に溶け込み，逆に配線層９からＡｌがバリア層を通してＳｉ基板１に侵入してアロイスパイク11を形成し，コンタクト不良を引き起こすとともに，不純物領域２を突き抜けて接合破壊を引き起こすことがある。

【００１２】デバイスの高集積化とともに不純物領域２はますます薄く形成される方向にあるから，アロイスパイク11の発生は深刻な問題となる。バリア層としての効果をあげるため，加熱炉内の温度，時間，雰囲気を制御してバリア性の高いＴｉＮＯ膜10を形成しようとしても，なかなか品質が安定せず思うようにバリア層としての効果をあげることができない。

【００１３】

【発明が解決しようとする課題】本発明は上記の問題に鑑み，よりバリア性が高くかつ安定に形成できるバリア層を有する半導体装置及びその製造方法を提供しようとするものである。

【００１４】

【課題を解決するための手段】図1(a) ～(e) は実施例を示す工程順断面図である。上記課題は，半導体基板１と，該半導体基板１上に形成された配線層９と，該半導体基板１と該配線層９に接して介在するバリア層５，６，８とを有する半導体装置であって，該バリア層５，６，８はチタン膜５，窒化チタン膜６，酸化チタン膜８による三層構造を含み，前記酸化チタン膜８は前記半導体基板１と前記配線層９間の電気的導通を保ちかつ両者間の化学的反応を阻止する厚さを有する半導体装置によって解決される。

【００１５】また，前記半導体基板１はＳｉ基板であり，前記配線層９はＡｌ層或いはＡｌを主成分とする合

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金層である半導体装置によって解決される。また，素子の形成された半導体基板１上に絶縁膜３を形成し，該絶縁膜３にコンタクトホール４を形成する工程と，該コンタクトホール４内に該半導体基板１に接続する第１のチタン膜５，窒化チタン膜６，第２のチタン膜７による導体多層膜５，６，７を形成する工程と，該第２のチタン膜７を全部あるいは一部酸化して酸化チタン膜８を形成する工程と，該酸化チタン膜８上に配線層９を形成する工程とを有する半導体装置の製造方法によって解決される。

【００１６】

【作用】酸化チタン膜８は酸化窒化チタン（ＴｉＮＯ）膜に比べてバリア性が高く，しかも容易に安定した品質が得られる。

【００１７】また，酸化チタン膜８は半導体基板１と配線層９間の電気的導通を保ちかつ両者間の化学的反応を阻止する作用を兼ね備える厚さに形成することができる。また，半導体基板１がＳｉ基板であり，配線層９がＡｌ層或いはＡｌを主成分とする合金層である半導体装置に酸化チタン膜８を含むバリア層を形成する時，その効果が大きい。

【００１８】また，酸化チタン膜８は，まずチタン膜７を形成し，その表面を酸化するようにすれば，例えば，酸素を含む雰囲気で高温高速加熱を行うことにより，容易にかつ安定に形成することができる。

【００１９】このような酸化チタン膜８を存在させることにより，アロイスパイクの発生を無くして接合破壊を防止し，かつコンタクト不良を防止することができる。

【００２０】

【実施例】図１(a) ～(e) は実施例を示す工程順断面図であり，以下，これらの図を参照しながら実施例について説明する。

【００２１】図１(a) 参照

素子（不純物領域）２の形成されたＳｉ基板１に，層間絶縁膜としてＣＶＤ法による厚さ0.8 ～１μmのＳｉO_2 膜３を形成し，そのＳｉO_2 膜３に素子２を露出するコンタクトホール４を形成する。

【００２２】図１(b) 参照

スパッタ法により，全面に厚さ数百～千Åの第１のチタン（Ｔｉ）膜５，厚さ数百～千Åの窒化チタン（ＴｉＮ）膜６をこの順に堆積する。ここまでは従来例と同様である。

【００２３】図１(c) 参照

スパッタ法により，全面に厚さが，例えば100 Åの第２のチタン（Ｔｉ）膜７を堆積する。

【００２４】図１(d) 参照

この基板を高温高速加熱（Rapid Thermal Anneal）装置に入れ，酸素と窒素の混合雰囲気中で，800 ～950 ℃，２０～３０秒の加熱により，第２のＴｉ膜７を酸化して酸化チタン（ＴｉO_2 ）膜８に変質させる。

【００２５】また，あらかじめ第２のＴｉ膜７を200 ～300 Åの厚さに形成しておき，酸素と窒素の混合雰囲気中で高温高速加熱することにより第２のＴｉ膜７の表面を酸化し，厚さが数十～百Å程度のＴｉO_2 膜８を形成し，その下に第２のＴｉ膜７に接続する極く薄いＴｉＮＯ膜を形成するようにしてもよい。

【００２６】図１(e) 参照

ＴｉO_2 膜８上にスパッタ法により配線層として，例えば厚さ１μmのＡｌ層９を形成する。

【００２７】このようにして形成されたＴｉ膜５，ＴｉＮ膜６，ＴｉO_2 膜８，ＴｉＮＯ膜は，いわゆるバリア層となり，Ａｌ層９とＳｉ基板１の電気的導通を保ち，かつＡｌ層９のＡｌとＳｉ基板１のＳｉが反応するのを防ぐ作用を持ち，この後の加熱を含む工程を経て半導体装置を完成した時，アロイスパイクの発生は見られなかった。

【００２８】ＴｉO_2 膜８の厚さは数十～200 Åが最適で，500 Å以上になるとＡｌとＳｉが反応するのを防ぐ作用は大きくなるものの，電気的導通性が減少して望ましくない。

【００２９】また，実施例では配線層９としてＡｌ層を用いる例について説明したが，例えば少量のＳｉや少量のＳｉ，Ｃｕ等を含む合金層を用いることもできる。なお，本発明によれば，Ｓｉ基板１のＳｉと第１のＴｉ膜５のＴｉが反応してチタンシリサイド層が不可避的に形成されるが，本発明にとっては実質的に問題はない。

【００３０】

【発明の効果】以上説明したように，本発明によれば，半導体基板１のＳｉと配線層９のＡｌが反応してアロイスパイクを生じることにより接合破壊を起こすことが防止され，かつ半導体基板１と配線層９のコンタクト不良も防止されるという顕著な効果を奏することができる。

【００３１】本発明は，半導体装置の高密度化に寄与するものである。

【図面の簡単な説明】

【図１】(a) ～(e) は実施例を示す工程順断面図である。

【図２】(a) ～(d) は従来例を示す工程順断面図である。

【図３】従来の問題点を示す断面図である。

【符号の説明】

１は半導体基板であってＳｉ基板
２は素子であって不純物領域
３は絶縁膜であってＳｉO_2 膜
４はコンタクトホール
５はバリア層でありＴｉ膜であって第１のＴｉ膜
６はバリア層であってＴｉＮ膜
７はバリア層でありＴｉ膜であって第２のＴｉ膜
８はバリア層であってＴｉO_2 膜
９は配線層であってＡｌ層

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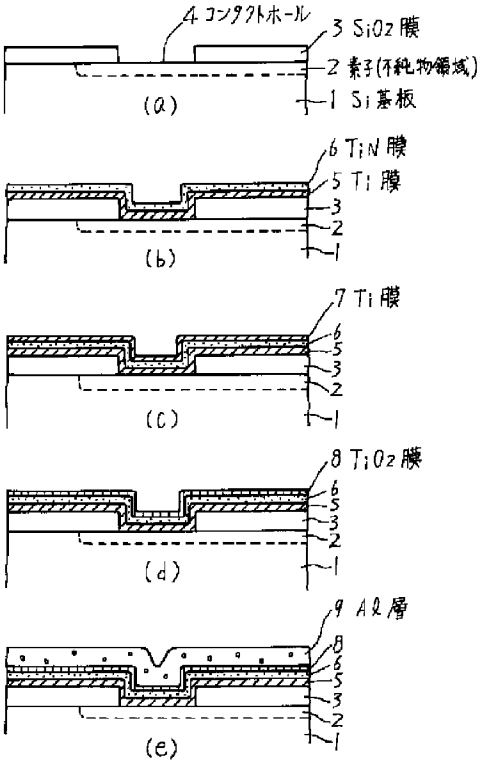
10はバリア層であってＴｉＮＯ膜

6

11はアロイスパイク

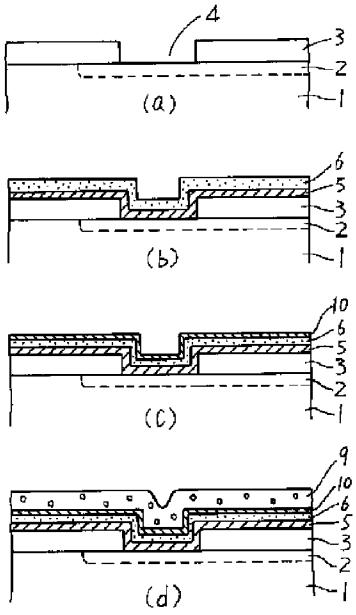
【図１】

実施例を示す工程順断面図



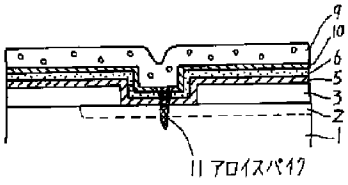
【図２】

従来例を示す工程順断面図



【図３】

従来の問題点を示す断面図



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JPH04284668A SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

Applicants: FUJITSU LTD,FUJITSU VLSI LTD

Inventors: CHITO TOSHIHIKO

Classifications:

IPC ***H01L21/28; H01L21/3205; H01L21/768; H01L23/52; H01L23/522; H01L29/43;*** (IPC1-7): H01L21/3205; H01L21/90; H01L29/46;

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SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

Abstract

PURPOSE:To manufacture a semiconductor device by a method wherein a semiconductor substrate is prevented from reacting with a wiring layer and a burrier layer for preventing a contact failure from being generated is provided. CONSTITUTION:A semiconductor device is constituted in such a way as to have a process wherein an insulating film (an SiO2 film) 3 is formed on a semiconductor Si substrate 1 with an element (an impurity region) 2 formed therein and a contact hole 4 is formed in the film 3, a process wherein conductor multilayer films 5, 6 and 7 consisting of a first titanium(Ti) film 5 which is connected to the substrate 1, a titanium nitride(TiN) film 6 and a second titanium(Ti) film 7 are formed in the hole 4, a process wherein the film 7 is all or partially oxidized to form a titanium oxide(TiO2) film 8 and a process for forming a wiring layer (an Al layer) 9 on the film 8.

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DESCRIPTION JPH04284668

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device and a manufacturing method thereof, and more particularly to a semiconductor device having a wiring layer formed on a semiconductor substrate with a barrier layer interposed therebetween and a manufacturing method thereof.

[0002]

A wiring layer of Al or the like is usually formed on a large number of elements formed on a semiconductor substrate via an interlayer insulating film. The wiring layer is connected to the semiconductor substrate in the contact hole formed in the interlayer insulating film.

[0003]
Incidentally, with the miniaturization of elements formed on a Si substrate and the high integration of devices, there is a problem that Al in the wiring layer reacts with Si in the substrate to cause a junction breakdown.

[0004]
Therefore, in recent years, a barrier layer is provided in the through hole in order to prevent a reaction between the Al wiring layer and the Si substrate.

[0005]

[Prior Art] FIGS. 2A to 2D are sectional views in order of steps showing a conventional example.

A conventional example will be described below with reference to these drawings.

[0006]
2A, a SiO2 film 3 is formed as an interlayer insulating film on a Si substrate 1 on which a reference element (impurity region) 2 is formed, and a contact hole 4 exposing the element 2 is formed on the SiO2 film 3. To do.

[0007]
As shown in FIG. 2 (b), a titanium (Ti) film 5 and a titanium nitride (TiN) film 6 are formed in this order on the entire surface by a sputtering method.

[0008]
See FIG. 2 (c). This substrate is placed in a heating furnace and heated at 450 ° C. for about 30 minutes in an atmosphere containing oxygen and nitrogen, whereby titanium oxynitride (TiNO) is formed on the surface of the TiN film 6.) Form the film 10.

[0009]

The Al layer 9 is formed as a wiring layer on the TiNO film 10 shown in FIG. 2 (d).

The Ti film 5 and the TiN film 6 form a so-called barrier layer, have an action of maintaining electrical conduction between the Al layer 9 and the Si substrate 1, and a function of preventing Al of the Al layer 9 and Si of the Si substrate 1 from reacting with each other. However, since the function of preventing the reaction between Al and Si is not sufficient, the TiNO film 10 is formed to improve the function.

[0010]

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However, even in such a case, the function as the barrier layer may be lost when the semiconductor device is completed through the subsequent steps including heating.

FIG. 3 is a sectional view showing a conventional problem.

[0011]
In the step after the Al layer 9 is formed, various kinds of heating are performed at a temperature at which Al does not melt, but in the heating step, the barrier layer does not function sufficiently and Si of the Si substrate 1 is wired in the contact hole portion. When it dissolves in the layer 9, conversely Al from the wiring layer 9 penetrates into the Si substrate 1 through the barrier layer to form an alloy spike 11, causing contact failure and penetrating the impurity region 2 to cause junction breakdown.

[0012]

The generation of the alloy spike 11 becomes a serious problem because the impurity region 2 tends to be formed thinner as the device becomes highly integrated.

In order to improve the effect as a barrier layer, even if the temperature, time, and atmosphere in the heating furnace are controlled to form the TiNO film 10 having a high barrier property, the quality is not stable and the effect as a barrier layer is not expected. I can't give it.

[0013]
In view of the above problems, the present invention is to provide a semiconductor device having a barrier layer having a higher barrier property and capable of being stably formed, and a method for manufacturing the same.

[0014]

[Means for Solving the Problems] FIGS. 1A to 1E are sectional views in order of steps showing an embodiment.

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The above-mentioned problem is a semiconductor device having a semiconductor substrate 1, a wiring layer 9 formed on the semiconductor substrate 1, and barrier layers 5, 6, 8 interposed in contact with the semiconductor substrate 1 and the wiring layer 9. The barrier layers 5, 6 and 8 include a three-layer structure including a titanium film 5, a titanium nitride film 6 and a titanium oxide film 8. The titanium oxide film 8 serves as an electrical conductor between the semiconductor substrate 1 and the wiring layer 9. This is solved by a semiconductor device having a thickness that maintains the electrical continuity and prevents the chemical reaction between the two.

[0015]

The semiconductor substrate 1 is a Si substrate, and the wiring layer 9 is an Al layer or an alloy layer containing Al as a main component.

In addition, the step of forming the insulating film 3 on the semiconductor substrate 1 on which the element is formed and forming the contact hole 4 in the insulating film 3, and the first titanium connecting to the semiconductor substrate 1 in the contact hole 4. A step of forming the conductor multilayer films 5, 6, 7 by the film 5, the titanium nitride film 6, and the second titanium film 7, and the titanium oxide film 8 is formed by completely or partially oxidizing the second titanium film 7. And a step of forming a wiring layer 9 on the titanium oxide film 8 to solve the problem.

[0016]

The titanium oxide film 8 has a higher barrier property than the titanium oxynitride (TiNO) film, and moreover, stable quality can be easily obtained.

[0017]

Further, the titanium oxide film 8 can be formed to have a thickness that maintains the electrical continuity between the semiconductor substrate 1 and the wiring layer 9 and prevents the chemical reaction between the two.

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Further, when the barrier layer including the titanium oxide film 8 is formed in the semiconductor device in which the semiconductor substrate 1 is the Si substrate and the wiring layer 9 is the Al layer or the alloy layer containing Al as a main component, the effect is great.

[0018]
The titanium oxide film 8 can be easily and stably formed by first forming the titanium film 7 and oxidizing the surface thereof, for example, by performing high-temperature high-speed heating in an atmosphere containing oxygen. can do.

[0019]
The presence of such a titanium oxide film 8 can prevent the occurrence of alloy spikes, prevent the junction from breaking, and prevent the contact failure.

[0020]
[Examples] FIGS. 1 (a) to 1 (e) are cross-sectional views in order of steps showing an example, and an example will be described below with reference to these drawings.

[0021]
1A, a SiO 2 film 3 having a thickness of 0.8 to 1 μm is formed as an interlayer insulating film by a CVD method on a Si substrate 1 on which a reference element (impurity region) 2 is formed, and the SiO 2 film 3 is formed. A contact hole 4 exposing the element 2 is formed in the substrate.

[0022]

Referring to FIG. 1B, a first titanium (Ti) film 5 having a thickness of several hundred to 1,000 Å and a titanium nitride (TiN) film 6 having a thickness of several hundred to 1,000 Å are formed on the entire surface by a sputtering method. Deposit in order.

The process up to this point is the same as in the conventional example.

[0023]
A second titanium (Ti) film 7 having a thickness of, for example, 100 Å is deposited on the entire

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surface by the reference sputtering method shown in FIG. 1 (c).

[0024]
See FIG. 1 (d). This substrate is put in a high-temperature high-speed heating (Rapid Thermal Anneal) device and heated in a mixed atmosphere of oxygen and nitrogen at 800 to 950 ° C. for 20 to 30 seconds to obtain a second temperature. The Ti film 7 is oxidized and transformed into a titanium oxide (TiO2) film 8.

[0025]
Further, the second Ti film 7 is formed in advance to a thickness of 200 to 300 Å, and the surface of the second Ti film 7 is oxidized by heating at high temperature and high speed in a mixed atmosphere of oxygen and nitrogen. However, a TiO 2 film 8 having a thickness of about several tens to 100 Å may be formed, and an extremely thin TiNO film connected to the second Ti film 7 may be formed thereunder.

[0026]
On the TiO2 film 8 shown in FIG. 1 (e), an Al layer 9 having a thickness of 1 μm, for example, is formed as a wiring layer by a sputtering method.

[0027]
The Ti film 5, the TiN film 6, the TiO2 film 8 and the TiNO film thus formed serve as so-called barrier layers, maintain the electrical continuity between the Al layer 9 and the Si substrate 1, and prevent the Al layer 9 from forming. It has an action of preventing Al from reacting with Si of the Si substrate 1, and when the semiconductor device was completed through the subsequent steps including heating, no alloy spike was observed.

[0028]
The thickness of the TiO 2 film 8 is optimally several tens to 200 Å, and if it is 500 Å or more, the action of preventing the reaction between Al and Si is increased, but the electrical conductivity is reduced, which is not desirable.

[0029]

Further, in the embodiment, the example in which the Al layer is used as the wiring layer 9 has

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been described, but it is also possible to use, for example, a small amount of Si or an alloy layer containing a small amount of Si, Cu or the like.

According to the present invention, Si of the Si substrate 1 and Ti of the first Ti film 5 react to form a titanium silicide layer inevitably, but there is substantially no problem for the present invention.

[0030]
As described above, according to the present invention, it is possible to prevent the junction breakdown due to the alloy spike caused by the reaction between Si of the semiconductor substrate 1 and Al of the wiring layer 9. In addition, it is possible to achieve a remarkable effect of preventing contact failure between the semiconductor substrate 1 and the wiring layer 9.

[0031]
The present invention contributes to increasing the density of semiconductor devices.

[0032]
Brief description of the drawings

[0033]
1 (a) to 1 (e) are process sectional views showing an embodiment.

[0034]
2A to 2D are cross-sectional views in order of steps showing a conventional example.

[0035]
3 is a cross-sectional view showing a conventional problem.

[0036]
Explanation of symbols

[0037]

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Reference numeral 1 is a semiconductor substrate, Si substrate 2 is an element, impurity region 3 is an insulating film, SiO 2 film 4 is a contact hole 5 is a barrier layer, and a Ti film is the first Ti film 6 is a barrier layer. The TiN film 7 is a barrier layer and a Ti film, the second Ti film 8 is a barrier layer, the TiO2 film 9 is a wiring layer, the Al layer 10 is a barrier layer, and the TiNO film 11 is Alloy spike

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1.
A semiconductor substrate (1), a wiring layer (9) formed on the semiconductor substrate (1), and barrier layers (5, 6, 6) interposed in contact with the semiconductor substrate (1) and the wiring layer (9) 8) A semiconductor device having: the barrier layer (5, 6, 8) including a three-layer structure of a titanium film (5), a titanium nitride film (6), and a titanium oxide film (8), and the oxidation A semiconductor device characterized in that the titanium film (8) has a thickness that maintains electrical continuity between the semiconductor substrate (1) and the wiring layer (9) and prevents a chemical reaction between the two.

2.
2. The semiconductor device according to claim 1, wherein the semiconductor substrate (1) is a Si substrate, and the wiring layer (9) is an Al layer or an alloy layer containing Al as a main component.

3.
A step of forming an insulating film (3) on the semiconductor substrate (1) on which the element is formed and forming a contact hole (4) in the insulating film (3), and the semiconductor substrate in the contact hole (4) A step of forming a conductor multilayer film (5, 6, 7) consisting of a first titanium film (5), a titanium nitride film (6) and a second titanium film (7) connected to (1), and the second Characterized in that it has a step of forming a titanium oxide film (8) by oxidizing all or part of the titanium film (7) of No. 1 and a step of forming a wiring layer (9) on the titanium oxide film (8). And a method for manufacturing a semiconductor device.

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(71)出願人　390040660
アプライド　マテリアルズ　インコーポレイテッド
ＡＰＰＬＩＥＤ　ＭＡＴＥＲＩＡＬＳ，ＩＮＣＯＲＰＯＲＡＴＥＤ
アメリカ合衆国　カリフォルニア州　95054　サンタ　クララ　バウアーズ　アベニュー　3050

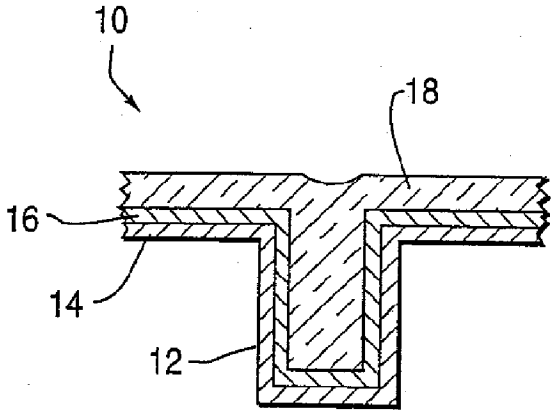
(72)発明者　ゴングダ　ヤオ
アメリカ合衆国，カリフォルニア州，　ミルピタス，　ミルモント　ドライヴ　1775

(74)代理人　弁理士　長谷川　芳樹　（外４名）

最終頁に続く

(54)【発明の名称】　アルミニウム接触用チタニウム・アルミナイド湿潤層

(57)【要約】
改良されたアルミニウム・コンタクト並びに開口部中にチタニウム・アルミナイド湿潤層を堆積すること及びその上にアルミニウム層を堆積することを含むそれを基板中の開口部中に形成する方法。チタニウム・アルミナイド湿潤層は、制御された厚さを有する。



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【特許請求の範囲】
【請求項１】ａ）開口部の底部及び側壁をカバーするためコリメータを通じてチタニウム・アルミナイドの層をスパッタ堆積すること、及び
ｂ）その上にアルミニウムの層をスパッタ堆積することを順に行う基板中の開口部中にアルミニウム・コンタクト層を堆積する方法。
【請求項２】ｘが１－３であって、ＴｉＡｌ$_x$がＴｉＡｌ$_x$ターゲットからスパッタされる請求項１の方法。
【請求項３】ＴｉＡｌ$_x$が約５０－５００オングストロームの深さまでスパッタされる請求項２の方法。
【請求項４】ｘが約３である請求項２の方法。
【請求項５】アルミニウムが約５００－５５０℃の温度においてＴｉＡｌ$_x$層上にスパッタ堆積される請求項２の方法。
【請求項６】アルミニウムが前記開口部を充たすためＴｉＡｌ$_x$層上に約３５０－４００℃の第１温度においてスパッタ堆積され、次いで約５００－５５０℃の第２温度においてスパッタされる請求項２の方法。
【請求項７】開口部中の第１層として、チタニウム窒化物が約５０－２００オングストロームの厚さにスパッタ堆積される請求項１の方法。
【請求項８】基板を真空下に維持する間、チタニウム窒化物が第１物理的気相堆積チャンバ中でスパッタされ、チタニウム・アルミナイドが第２物理的気相堆積チャンバ中でスパッタされ、及びアルミニウムが第３物理的気相堆積チャンバ中でスパッタされる請求項７の方法。
【請求項９】約５０－２００オングストロームの厚さのチタニウム窒化物の第１層、５０－５００オングストロームの制御された厚さを有するチタニウム・アルミナイド（ＴｉＡｌ$_x$，ｘは１－３）の第２層、及びアルミニウムの第３プレーナ化された層を含むアルミニウム・コンタクト。
【請求項１０】ｘが約３である請求項９のアルミニウム・コンタクト。
【発明の詳細な説明】
【０００１】本発明は、改良されたアルミニウム・コンタクト(contact)に関する。特に、本発明はプレーナ化された(planarized)アルミニウム・コンタクト及びその製造方法に関する。
【０００２】
【発明の背景】半導体装置用のアルミニウム・コンタクトの製造において、シリコン・ウェハはトランジスタ及びその類似物用のソース及びドレーン領域を提供するためにドープされ得る。１つの集積回路層を他のものと連結するために、開口部(openings)はアルミニウムあるいは銅、又は少量の銅を含むアルミニウム合金のような導電性金属が堆積される誘電体層(dielectric layer)中に造られる。このようなコンタクト開口部の製造においていくつかの試みがある。アルミニウムのような導電性金属がシリコン（珪素）に隣接して堆積されると、引き続く高い温度処理は、アルミニウムと珪素が反応して金属珪化物を形成させる。アルミニウム珪化物もまた導電性であり、アルミニウムと珪素の接合間で「スパイキング(spiking)」を引き起こす。
【０００３】このスパイキングを避けるためアルミニウム堆積に先だってコンタクト開口部中に、チタニウム窒化物層のようなバリヤ層を堆積することは容認できる実施であった。しかし、チタニウム窒化物はアルミニウムより高いシート抵抗(sheet resistance)を有し、このためチタニウム窒化物の薄い層のみがコンタクトのシート抵抗率(sheet resistivity)に反対方向に作用することなく耐えることができる。さらに、チタニウム窒化物は上に重なるアルミニウム層を十分に湿潤せず、このためチタニウム窒化物とその上に重なるアルミニウム、すなわちチタニウム窒化物からのアルミニウム離層との間の接着性の問題を引き起こす。デウェッティング(dewetting)現象を除去するためチタニウム窒化物バリヤ層上にチタニウム湿潤層を堆積することを含み、種々の方法がチタニウム窒化物とアルミニウムの間の湿潤性(wettability)を改良するために試みられてきた。
【０００４】しかし、引き続く処理の間、アルミニウムとチタニウムは約４００℃と同様な低い温度で反応し、チタニウムとアルミニウムの境界面においてチタニウム・トリアルミナイド（ＴｉＡｌ$_3$）領域を形成し、この領域がアルミニウムに比べて比較的に高いシート抵抗率を有し、このことがアルミニウム・フィルムの導電性を下げ及びこのために装置能力を下げる。さらに、チタニウムはこの反応の間その上に堆積したアルミニウムの一部を消費し、さらにアルミニウム・フィルムの導電性を下げる。たとえば、５００Åのチタニウムでラインされた(lined)アルミニウムで充填されたコンタクト開口部に関して、ＴｉＡｌ$_3$を形成するそれらの間の反応は約１５００Åのアルミニウムを消費する。またさらに、アルミニウムがコンタクト中に堆積されるに従い、厚いチタニウム・トリアルミナイド層の形成は、特に小開口幅のコンタクトに関して、コンタクト開口部の早期の閉塞を引き起こし、コンタクト中に空隙の形成を引き起こす。
【０００５】このように、開口部中でチタニウム窒化物上にアルミニウム・コンタクトを形成する改良された方法が求められてきた。
【０００６】
【発明の要約】我々は、湿潤層としてコンタクト開口部中に、制御された厚さを有するチタニウム・アルミナイド(aluminide)（ＴｉＡｌ$_x$，ｘは１－３）の層をスパッタ堆積(sputter depositing)することによって、引き続くアルミニウム処理の間、チタニウムが湿潤層として使用される場合よりも３０－６０パーセント少ないコンタクト中のアルミニウムが消費されることを見いだした。

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結果として、アルミニウム・コンタクトのコンタクトシート抵抗は、より予想可能であってより低いものである。同様のコンタクトシート抵抗率を得るためにより少ないアルミニウムが堆積する必要があり、その上に重なるアルミニウム層のプレーナ化は、アルミニウムとチタニウムの間の反応が非常に低下するため改良される。

【０００７】本発明のコンタクトは、乾燥エッチング(dry etch)技術と両立でき、物理的気相堆積(physical vapor deposition)チャンバ中で容易にスパッタ堆積され、相互に連結させる物質の存在を両立させるシート抵抗率を有する。

【０００８】

〔発明の詳細な説明〕図１は、本発明のコンタクトの一例である。その中に開口部１２を有する珪素層１０は、チタニウム窒化物のようなバリヤ材料の第１層１４及びその上に$TiAl_x$の湿潤層１６を含む。その後、開口部１２は、アルミニウム１８で充たされる。

【０００９】本発明の方法によれば、ｘが１－３である$TiAl_x$の層は、３７．８重量％のアルミニウムを含もの、あるいはアルミニウム：チタニウムが約３：５の比である$TiAl_x$ターゲットからのスパッタリングによって珪素ウェハ又は誘電体フィルム層などの基板中に、好ましくはコリメータを通じて、バイア(via)あるいはコンタクト開口部などのアパーチャ(aperture)中に堆積される。この方法において、$TiAl_x$の均質な層は、アパーチャの側壁上と同様に底部上にも堆積され、アパーチャは２：１より高いアスペクト比を有することができる。この$TiAl_x$層は、それが上に堆積されるとき、引き続いて堆積され上に重なるアルミニウム層を湿潤する。さらに、一部のアルミニウム、たとえば３０パーセントは、既に$TiAl_x$湿潤層中に存在しているので、引き続く処理の間その上に堆積したアルミニウム・コンタクト層と湿潤層の間で、湿潤層がチタニウム単独のときより少ない反応が起きる。アルミニウム層のより少量が湿潤層によって消費されるので、引き続く高温度処理はアルミニウム層に非常に少なく作用し、金属ライン(line)シート抵抗における増大を防止しアルミニウム層中の空隙の形成を防止する。

【００１０】チタニウム、チタニウム窒化物、チタニウム・アルミナイド及びアルミニウムは図２に示されるようにＰＶＤチャンバ中にスパッタ堆積され得る。

【００１１】図２を参照すると、スパッタリング・チャンバ２０は、ＤＣ電力源２３と基板支持２４に連結される所望のターゲット２２を含む。ターゲット２２は、堆積される材料によって、チタニウム、チタニウム・アルミナイド又はアルミニウムからなるものであり得る。コリメータ２６は、ターゲット２２と基板支持２４の間に取り付けられている。ＲＦ電力源２８は、基板支持２４に連結されている。ガス入口マニホールド３０は、アルゴンあるいは窒素のような種々のガスをチャンバ中に制御可能に通過することを許す。処理の間、基板３２は、基板支持２４上に取り付けられる。

【００１２】典型的なアルミニウム・コンタクトの調製は、以下に記述されている。薄いチタニウム窒化物層は、たとえば５０－２００Åの厚さのものは、アパーチャ中で最初に堆積される。この層は、チャンバ中窒素ガスの存在下でチタニウム・ターゲットをスパッタすることにより形成することができる。チタニウム窒化物層は、必要であれば既知の方法でアニールされ(annealed)、又は酸素を詰め込まれてもよい。

【００１３】チタニウム・アルミナイドの堆積を実行するために、その中でアルミニウム・コンタクトが形成される複数の露出した開口部を有する基板が提供される。基板３２を基板支持２４上に取り付けた後、アルゴンの流れがチャンバ中で開始され、チタニウム・アルミナイドが基板３２上のチタニウム・アルミナイド・ターゲット２２からスパッタされる。コリメータ２６を通じてスパッタリングすることによって、$TiAl_3$の層は、露出した開口部の底部上に堆積されることに加えて側壁上に堆積され、より高いアスペクト比を有する開口部が充填され得る。

【００１４】以下の例において、その上に熱的(thermal)酸化珪素の層を有する珪素層中のコンタクト開口部は、標準的写真製版(photolithographic)技術を用いて造られた。コンタクト開口部は、サイズすなわち直径で０．６、０．８、及び１．０ミクロンと変えらて製造され、１．２ミクロンの深さであった。

【００１５】制御－湿潤層としてのスパッタされたチタニウム

種々の厚さのチタニウムの層は、２：１のアスペクト比を有する（１．２ミクロンの深さ）直径０．６ミクロンのコンタクト開口部中に堆積された。チタニウムは、１：１のアスペクト比のコリメータを使用しスパッタ堆積された。アルミニウムは、チタニウム層上にスパッタ堆積された。測定は、アルミニウム充填(fill)とプレーナ化に関して行われた。アルミニウムの堆積はまた変えられ、ホット・アルミニウム堆積（５１０－５５０℃）、コールド／ホット・アルミニウム堆積（最初の温度が約４００℃で引き続く温度上昇で約５００－５５０℃まで）、及び堆積の間ターゲットの適用される電力が含まれた。図３（ａ）から３（ｄ）の全てのデータは、０．６ミクロン直径の開口部を使用して測定された。

【００１６】図３（ａ）は、ホット・アルミニウム堆積に関するコンタクト充填のパーセントを示す。パーセント充填は、最適温度が約５３０℃で、約６５－９６％の変化をする。

【００１７】図３（ｂ）は、パーセント・コンタクト充填対アルミニウム堆積の温度のグラフであり、これが３０００Åのコールド・アルミニウム及び５０００Åのホット・アルミニウムを殆どコンタクト充填のロスなしで

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堆積するよう変化することができるが、最適充填が２０００Åのアルミニウム・コールド（４００℃）及び６０００Åのアルミニウム・ホット（５３０℃）の堆積によって達成されることを示す。

【００１８】図３（ｃ）は、パーセント・コンタクト充填対ホット・アルミニウム堆積の間の電力のグラフであり、低電力におけるアルミニウムの堆積が好適であることを示す。

【００１９】湿潤性及びパーセント・コンタクト充填に関してチタニウムの最適な厚さは、図３（ｄ）中に示されるように、約４００Åである。壁範囲(wall coverage)が低く、２：１のアスペクト比の開口部の底部において約１４パーセントのみであるので、チタニウム層に関する最小厚さは、約５０－６０Åである。約５５０Åのより高いチタニウム層厚さにおいて、開口部の頂部において形成される張出部(overhang)は、開口部中へのアルミニウムのリフロー(reflow)を防止する。

【００２０】図４（ａ）は、４００Åのチタニウムで及びその後コールド／ホット・プロセスによって堆積されたアルミニウムで充填されたコンタクトの断面の顕微鏡写真である。

【００２１】図４（ｂ）は、図４（ａ）のコンタクトのＴＥＭ分析の顕微鏡写真である。約２０００Å厚さの$TiAl_3$の層が測定された。

【００２２】実施例１－湿潤層としてのスパッタされた$TiAl_x$

コントロール(Control)の中におけるようにコンタクト開口部中に$TiAl_3$の層のスパッタ堆積後、アルミニウムは、コンタクト開口部中に１：１アスペクト比のコリメータを使用してスパッタ堆積された。

【００２３】得られたフィルムのラザフォード後方散乱(Rutherford Backscattering)分析は、約３．５：１のＡｉ：Ｔｉ比又は７７．８％のアルミニウムと２２．２％のチタニウムを含む合金が堆積されたことを示した。$TiAl_3$の抵抗率(resistivity)は、１５８．$TiAl_3$の形成を確認する９６μｏｈｍｓ－ｃｍであった。スパッタされた$TiAl_3$層のシート抵抗均一性は、約２．２６６パーセント、１シグマ(sigma)であった。

【００２４】その後、アルミニウムは、ホット及びコールド／ホット・プロセスの両方を使用して$TiAl_3$層の上に堆積された。

【００２５】図５は、ホット堆積及びホット／コールド堆積方法の両方によって堆積されたアルミニウムに関し、上に重ねられるアルミニウム層のパーセント充填対$TiAl_3$層のオングストロームでの厚さのグラフである。ホット・アルミニウム堆積が、$TiAl_3$の任意のフィルム厚さにおいて優れた充填を与えることは明らかである。コールド／ホット・プロセスを使用してアルミニウムを堆積するとき、最適パーセント充填は、$TiAl_3$のフィルムが少なくとも１０００Åの厚さで堆積されるまで得られない。

【００２６】図６は、ホット・プロセスを使用して堆積された４００Åの$TiAl_3$と８０００Åのアルミニウムによる直径０．６ミクロンのコンタクト開口部の優れた充填を示す。

【００２７】図７は、$TiAl_3$層とアルミニウムの間の境界面のＴＥＭ分析の顕微鏡写真である。

【００２８】上記のプロセスは、２つのスパッタ堆積チャンバのみを必要とし、第１は$TiAl_x$合金をスパッタ堆積すること及び第２はその上にアルミニウムをスパッタ堆積することである。好適な複数チャンバ堆積システムは、本願明細書に参考として組み入れられる米国特許第４，９５１，６０１号中にＭａｙｄａｎらによって開示されており、図８中に略図的に示されている。

【００２９】図８は、本プロセスの堆積及び処理の工程の全てが実施可能である好適な堆積システムを示す。このシステムは、高真空基板移動チャンバに連結した複数の処理真空チャンバを含む。処理チャンバの各々は、同時に単一のウェハを処理するが、複数のウェハは種々のチャンバ中で平行(parellel)処理によってシステム中に収容される。図８のシステム８００は、システム中への基板の装填及び取り外しに関し、２つの独立に操作されるロード・ロック・チャンバ(load lock chambers)８１０Ａ及び８１０Ｂを含む。基板は、ロード・ロック・チャンバ８１０Ａから、種々の連結された処理チャンバへの基板の移動のためのロボット８１３を含む基板移動チャンバ８１２中に移動される。たとえば、予備清浄チャンバ８１６は、空気に晒された珪素基板から天然の酸化層を除去するために基板をスパッタ清浄あるいはプラズマ清浄することに使用することができる。その後基板は、種々の処理チャンバに移動することができる。たとえば、チタニウム窒化物層はチャンバ８２０中で堆積することができ、チタニウム・アルミナイド層はチャンバ８２２中で堆積することができ、アルミニウム層はチャンバ８２６中で堆積することができる。その後、被覆された基板は、システム８００から移動のためロード・ロック・チャンバ８１０Ｂに移動される。

【００３０】加熱あるいはアニーリング及びその類似の目的で、追加的処理チャンバは、システム８００に追加することができる。

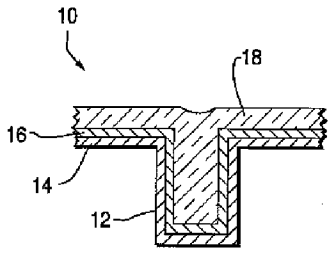
【００３１】１：１のアスペクト比のコリメータを使用して、２．９１Å／ｋｗの堆積速度が達成される。

【００３２】アルミニウム・コンタクトを形成する好ましい方法において、チタニウム窒化物の約５０－２００Å厚さの第１層が開口部中でスパッタ堆積され、通常の方法で酸素中でアニールされる。基板は、チタニウム・アルミナイドのターゲットを包含するチャンバに移動され、約５０－５００Å厚さの$TiAl_x$層がアルゴン・ガス及びチャンバ中のコリメータを使用して堆積される。

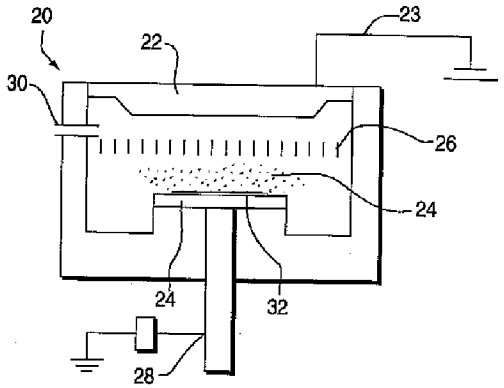
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【００３３】その後、基板は、アルミニウムの堆積のために他のスパッタリング・チャンバに移動される。
【００３４】ホット・アルミニウム・プロセスにおいて、基板支持は約５００℃又はそれ以上の温度まで加熱される。
【００３５】コールド／ホット・プロセスを使用して、数千オングストロームの厚さのアルミニウムの第１堆積は３５０－４００℃でなされ、その後基板支持は約５５０℃まで加熱され、堆積は所望のアルミニウムの厚さまで継続される。アルミニウムの最初のコールド堆積は、チタニウム・アルミナイドとアルミニウム層との間の良好な湿潤を確実にする。堆積の間の温度をアルミニウムの流れ点(flow point)を超える温度まで、たとえば約５５０℃まで上昇することによって、アルミニウムは、アルミニウム層中の空隙の形成を除去しながら、堆積されるときのように流動する。加熱されたアルゴンはまた、基板の温度を急速に上昇させるためにウェハ支持を通って通過させることもできる。
【００３６】約３５００Åのアルミニウムのみが、所望のシート抵抗を得るためにコンタクトを充填するために必要とされる。引き続く高温度処理の間アルミニウムとチタニウムの間で殆ど反応は起こらないので、コンタクトの抵抗は低いままである。
【００３７】コンタクトの抵抗の安定性は、装置の操作の間アルムニウム・ラインの電子移動効果(electron migration effects)を防止することにおいて、他の利点を有する。アルミニウムがチタニウムとの反応によって消費されるときのように、アルミニウムシート抵抗が時間に対して増大する場合、電流密度は増加し、アルミニウムライン中の電子移動も増大し、このことはアルミニウム・ライン中における破壊を導き得る。
【００３８】本発明は、特定の具体例によって記述されたきたが、材料、反応条件、及びそれに類似するものにおける種々の変形は、この技術分野において当業者によってなし得るものであり、これらが本願明細書中に含まれるものであることを意味する。
【００３９】
【図面の簡単な説明】
【図１】　本発明のコンタクトの断面図である。
【図２】　本発明のプロセスにおいて使用される材料が堆積することができるスパッタリング・チャンバの略図である。
【図３】　（ａ）は、ホット・アルミニウム堆積に関するパーセント・コンタクト充填対温度のグラフである。（ｂ）は、パーセント・コンタクト充填対ホット／コールド・アルミニウム堆積のグラフである。（ｃ）は、アルミニウム堆積の間のパーセント・コンタクト充填対電力のグラフである。（ｄ）は、パーセント・コンタクト充填対チタニウム厚さのグラフである。
【図４】　（ａ）は、チタニウム湿潤層を使用して製造されたコンタクトの断面のＳＥＭ写真である。（ｂ）は、チタニウム・アルミナイド層の形成を示す、チタニウム湿潤層を使用して製造されたコンタクトの断面のＴＥＭ写真である。
【図５】　ホット・アルミニウム堆積及びコールド／ホット・アルミニウム堆積の両方に関するパーセント・アルミニウム充填対チタニウム・アルミナイド厚さのグラフである。
【図６】　湿潤層としてチタニウム・アルミナイドを使用して製造されたコンタクトの断面のＳＥＭ写真である。
【図７】　湿潤層としてチタニウム・アルミナイドを使用して製造されたコンタクトの断面のＴＥＭ写真である。
【図８】　本発明を実施するために有用な複数チャンバ真空堆積システムの平面図である。

【図１】

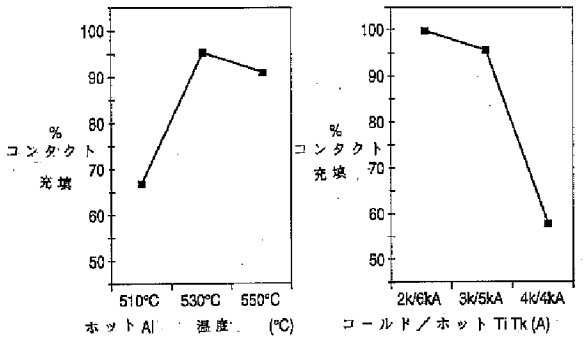


【図２】

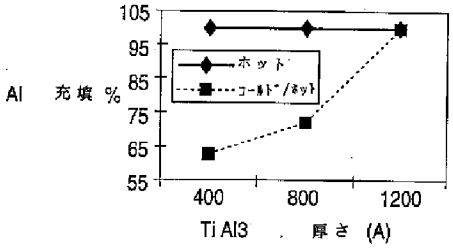


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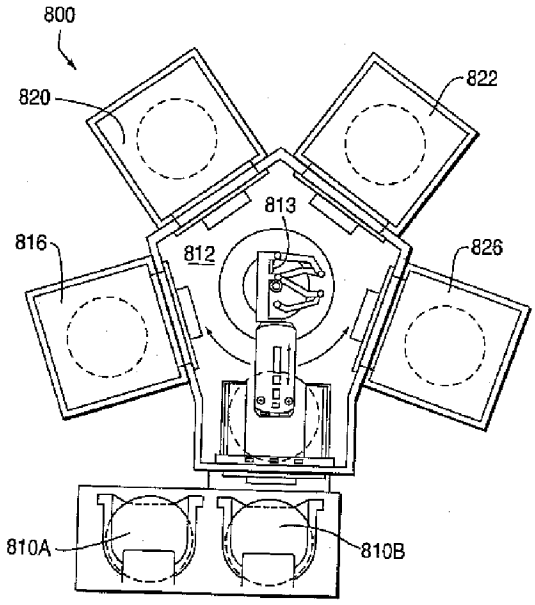
【図3】

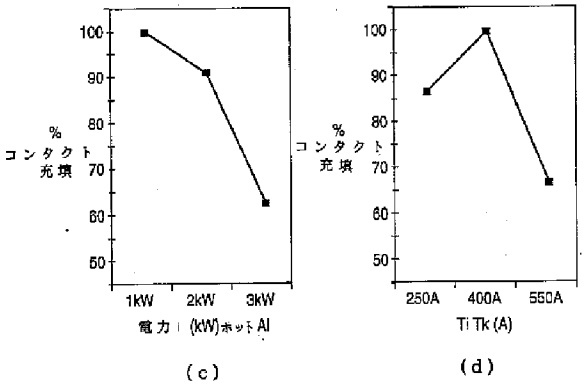


【図5】



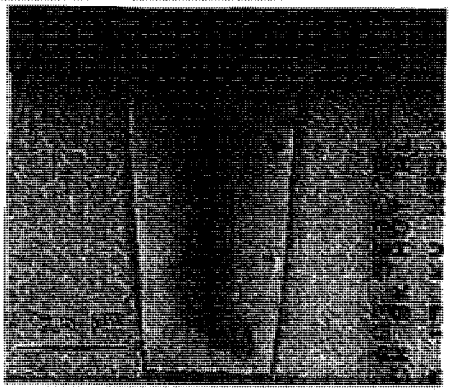
【図8】





【図6】

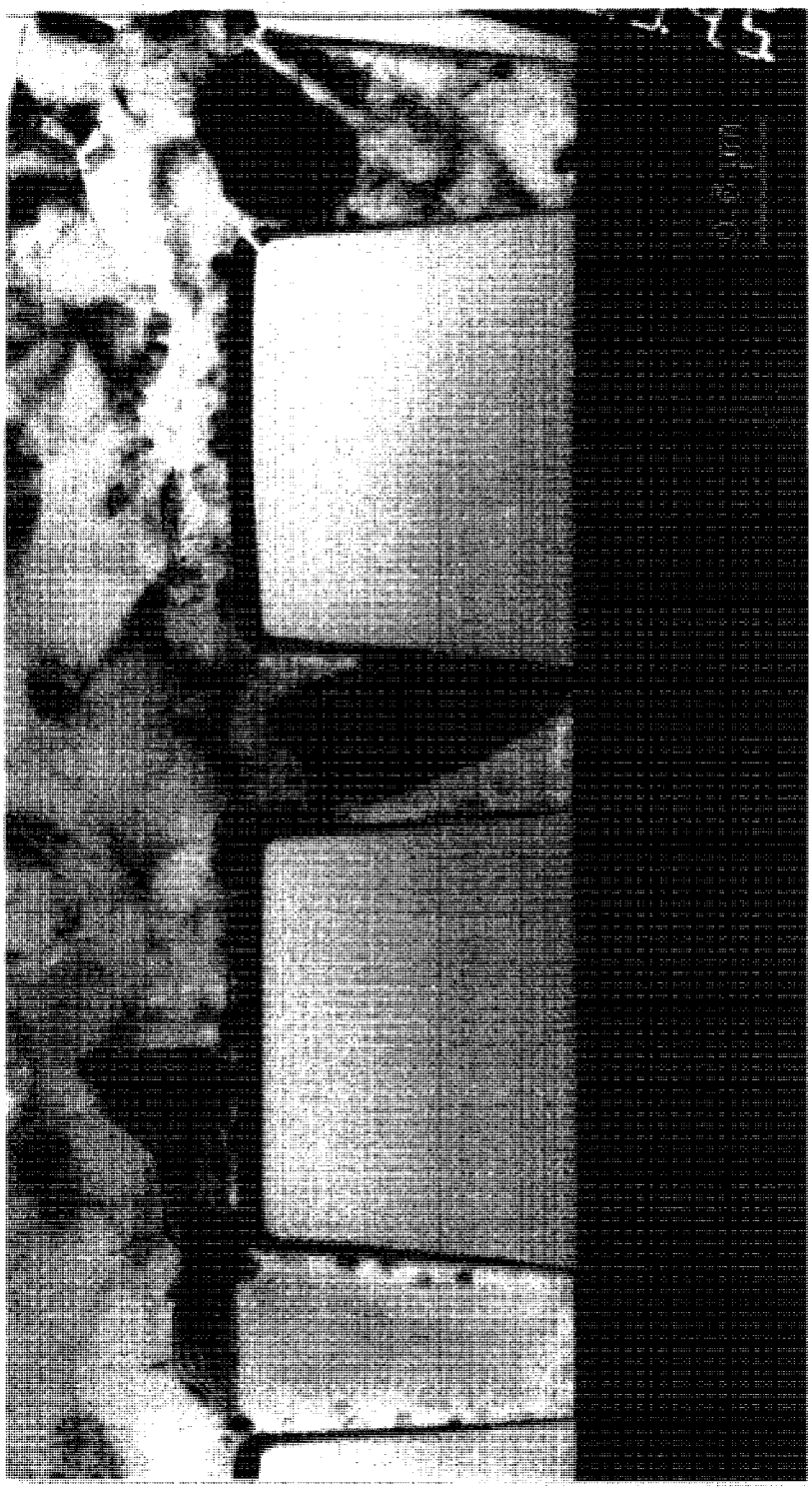
図面代用写真



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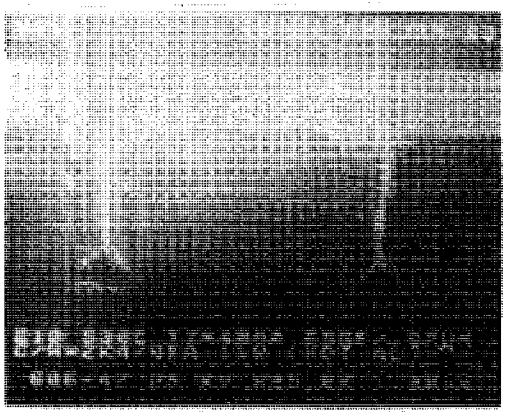
【図７】

図面代用写真



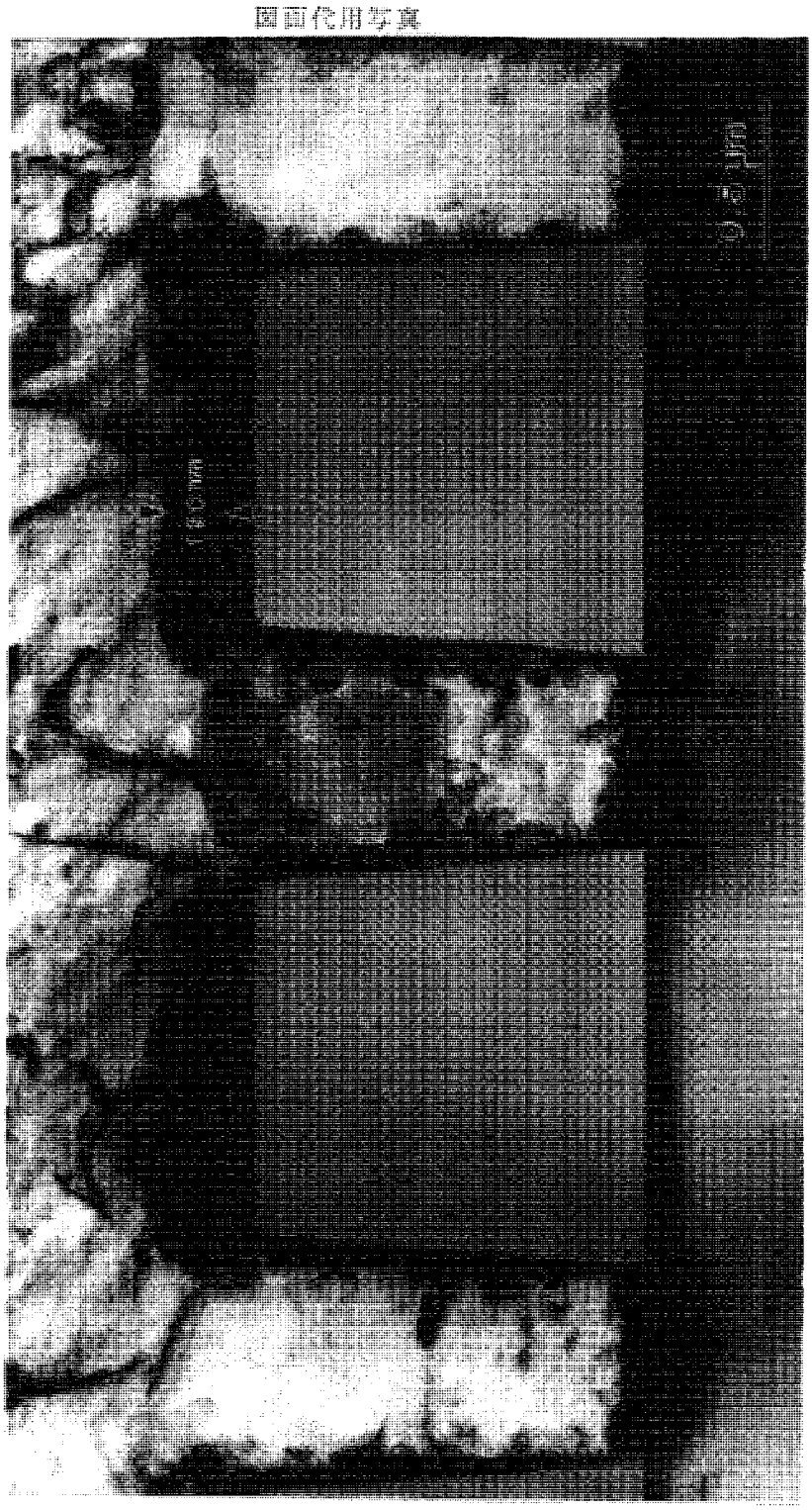
【図4】

図面代用写真



（a）

【図４】

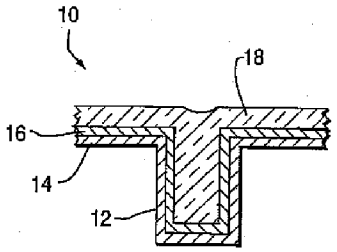


【手続補正書】
【提出日】平成９年６月５日
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】００２０
【補正方法】変更
【補正内容】
【００２０】図4は、４００　のチタニウムで及びその後コールド／ホット・プロセスによって堆積されたアルミニウムで充填されたコンタクトの断面の顕微鏡写真である。
【手続補正２】
【補正対象書類名】明細書
【補正対象項目名】００２１
【補正方法】変更
【補正内容】
【００２１】図5は、図4のコンタクトのＴＥＭ分析の顕微鏡写真である。約２０００　厚さのＴｉＡｌ$_3$の層が測定された。
【手続補正３】
【補正対象書類名】明細書
【補正対象項目名】００２５
【補正方法】変更
【補正内容】
【００２５】図6は、ホット堆積及びホット／コールド堆積方法の両方によって堆積されたアルミニウムに関し、上に重ねられるアルミニウム層のパーセント充填対ＴｉＡｌ$_3$層のオングストロームでの厚さのグラフである。ホット・アルミニウム堆積が、ＴｉＡｌ$_3$の任意のフィルム厚さにおいて優れた充填を与えることは明らかである。コールド／ホット・プロセスを使用してアルミニウムを堆積するとき、最適パーセント充填は、ＴｉＡｌ$_3$のフィルムが少なくとも１０００　の厚さで堆積されるまで得られない。
【手続補正４】
【補正対象書類名】明細書
【補正対象項目名】００２６
【補正方法】変更
【補正内容】
【００２６】図7は、ホット・プロセスを使用して堆積された４００　のＴｉＡｌ$_3$と８０００　のアルミニウムによる直径０．６ミクロンのコンタクト開口部の優れた充填を示す。
【手続補正５】
【補正対象書類名】明細書
【補正対象項目名】００２７
【補正方法】変更
【補正内容】
【００２７】図8は、ＴｉＡｌ$_3$層とアルミニウムの間の境界面のＴＥＭ分析の顕微鏡写真である。
【手続補正６】
【補正対象書類名】明細書
【補正対象項目名】００２８
【補正方法】変更
【補正内容】
【００２８】上記のプロセスは、２つのスパッタ堆積チャンバのみを必要とし、第１はＴｉＡｌ$_x$合金をスパッタ堆積すること及び第２はその上にアルミニウムをスパッタ堆積することである。好適な複数チャンバ堆積システムは、本願明細書に参考として組み入れられる米国特許第４，９５１，６０１号中にＭａｙｄａｎらによって開示されており、図９中に略図的に示されている。
【手続補正７】
【補正対象書類名】明細書
【補正対象項目名】００２９
【補正方法】変更
【補正内容】
【００２９】図9は、本プロセスの堆積及び処理の工程の全てが実施可能である好適な堆積システムを示す。このシステムは、高真空基板移動チャンバに連結した複数の処理真空チャンバを含む。処理チャンバの各々は、同時に単一のウェハを処理するが、複数のウェハは種々のチャンバ中で平行（ｐａｒｅｌｌｅｌ）処理によってシステム中に収容される。図９のシステム８００は、システム中への基板の装填及び取り外しに関し、２つの独立に操作されるロード・ロック・チャンバ（ｌｏａｄ　ｌｏｃｋ　ｃｈａｍｂｅｒｓ）８１０A及び８１０Ｂを含む。基板は、ロード・ロック・チャンバ８１０Aから、種々の連結された処理チャンバへの基板の移動のためのロボット８１３を含む基板移動チャンバ８１２中に移動される。たとえば、予備清浄チャンバ８１６は、空気に晒された珪素基板から天然の酸化層を除去するために基板をスパッタ清浄あるいはプラズマ清浄することに使用することができる。その後基板は、種々の処理チャンバに移動することができる。たとえば、チタニウム窒化物層はチャンバ８２０中で堆積することができ、チタニウム・アルミナイド層はチャンバ８２２中で堆積することができ、アルミニウム層はチャンバ８２６中で堆積することができる。その後、被覆された基板は、システム８００から移動のためロード・ロック・チャンバ８１０Ｂに移動される。

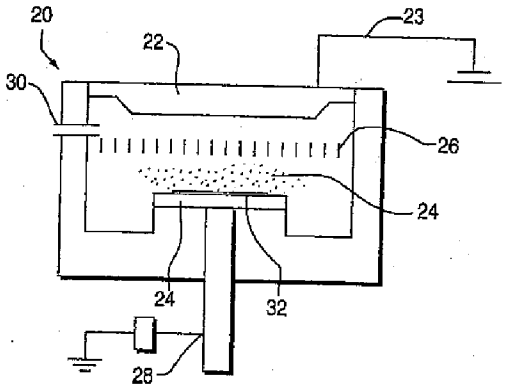
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【手続補正書】
【提出日】平成９年９月４日
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】図面の簡単な説明
【補正方法】変更
【補正内容】
【図面の簡単な説明】
【図１】　本発明のコンタクトの断面図である。
【図２】　本発明のプロセスにおいて使用される材料が堆積することができるスパッタリング・チャンバの略図である。
【図３】　（ａ）は、ホット・アルミニウム堆積に関するパーセント・コンタクト充填対温度のグラフである。（ｂ）は、パーセント・コンタクト充填対ホット／コールド・アルミニウム堆積のグラフである。（ｃ）は、アルミニウム堆積の間のパーセント・コンタクト充填対電力のグラフである。（ｄ）は、パーセント・コンタクト充填対チタニウム厚さのグラフである。
【図４】　チタニウム湿潤層を使用して製造されたコンタクトの断面のＳＥＭ写真である。
【図５】　チタニウム・アルミナイド層の形成を示す、チタニウム湿潤層を使用して製造されたコンタクトの断面のＴＥＭ写真である。
【図６】　ホット・アルミニウム堆積及びコールド／ホット・アルミニウム堆積の両方に関するパーセント・アルミニウム充填対チタニウム・アルミナイド厚さのグラフである。
【図７】　湿潤層としてチタニウム・アルミナイドを使用して製造されたコンタクトの断面のＳＥＭ写真である。
【図８】　湿潤層としてチタニウム・アルミナイドを使用して製造されたコンタクトの断面のＴＥＭ写真である。
【図９】　本発明を実施するために有用な複数チャンバ真空堆積システムの平面図である。
【手続補正２】
【補正対象書類名】図面
【補正対象項目名】全図
【補正方法】変更
【補正内容】

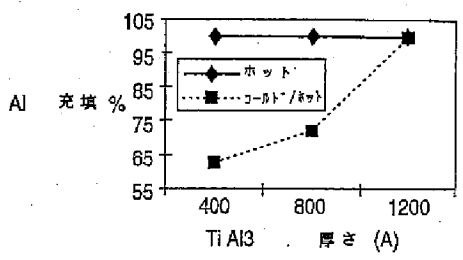
【図１】



【図２】

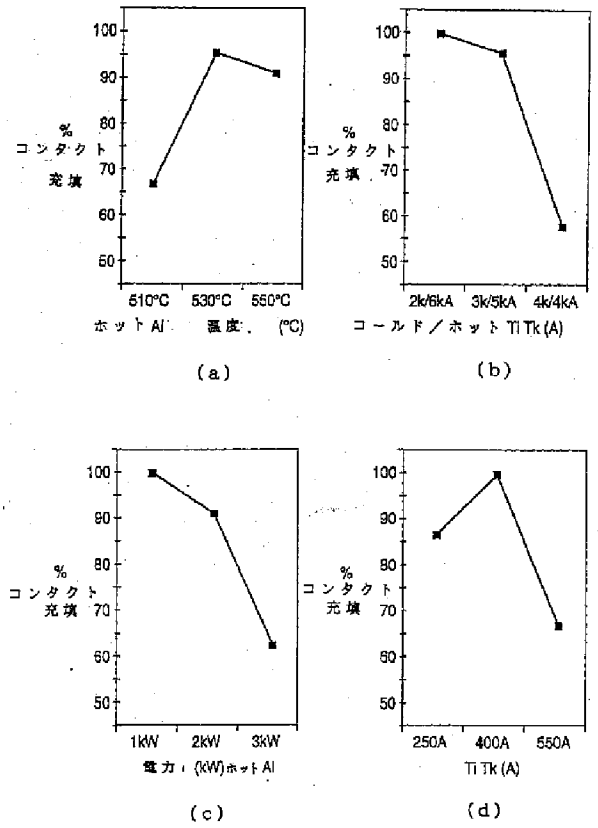


【図６】



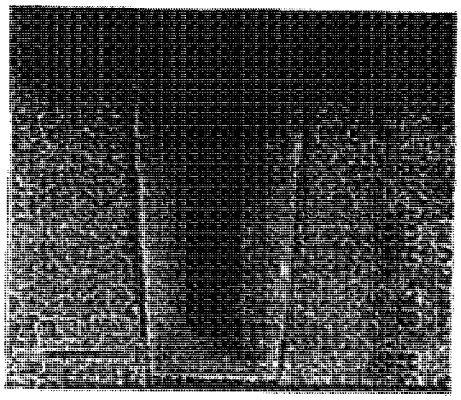
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【図3】



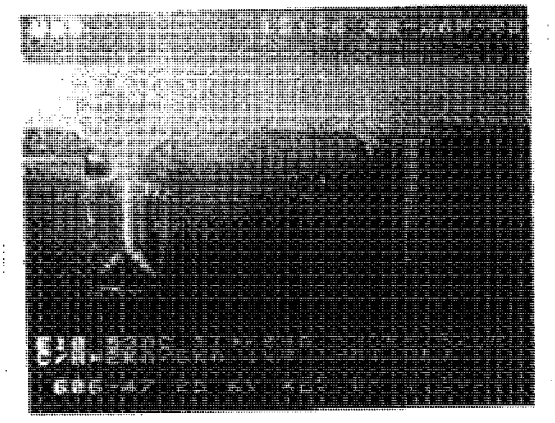
【図7】

図面代用写真

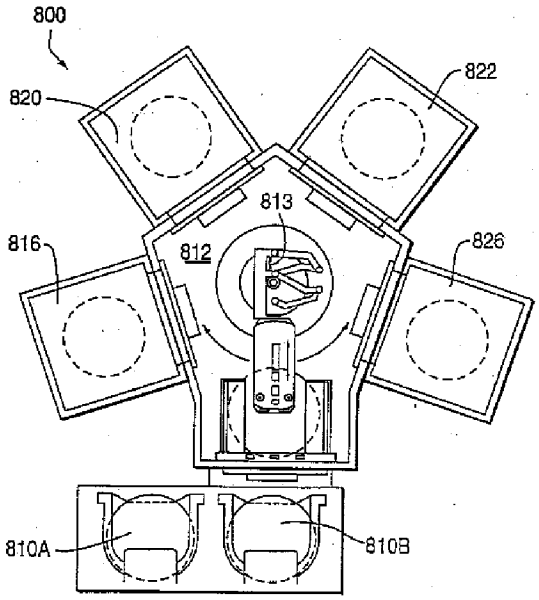


【図4】

図面代用写真



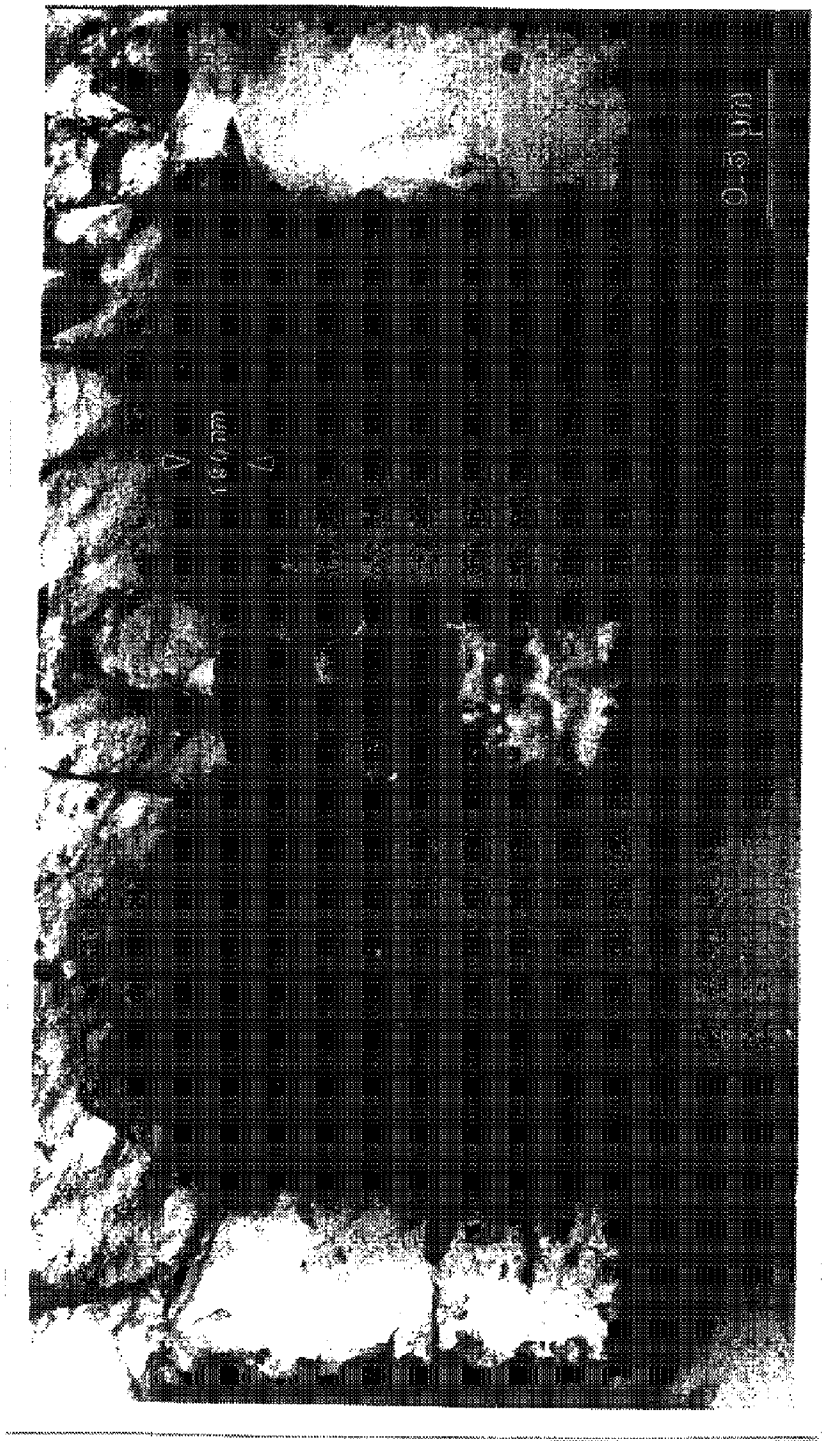
【図9】



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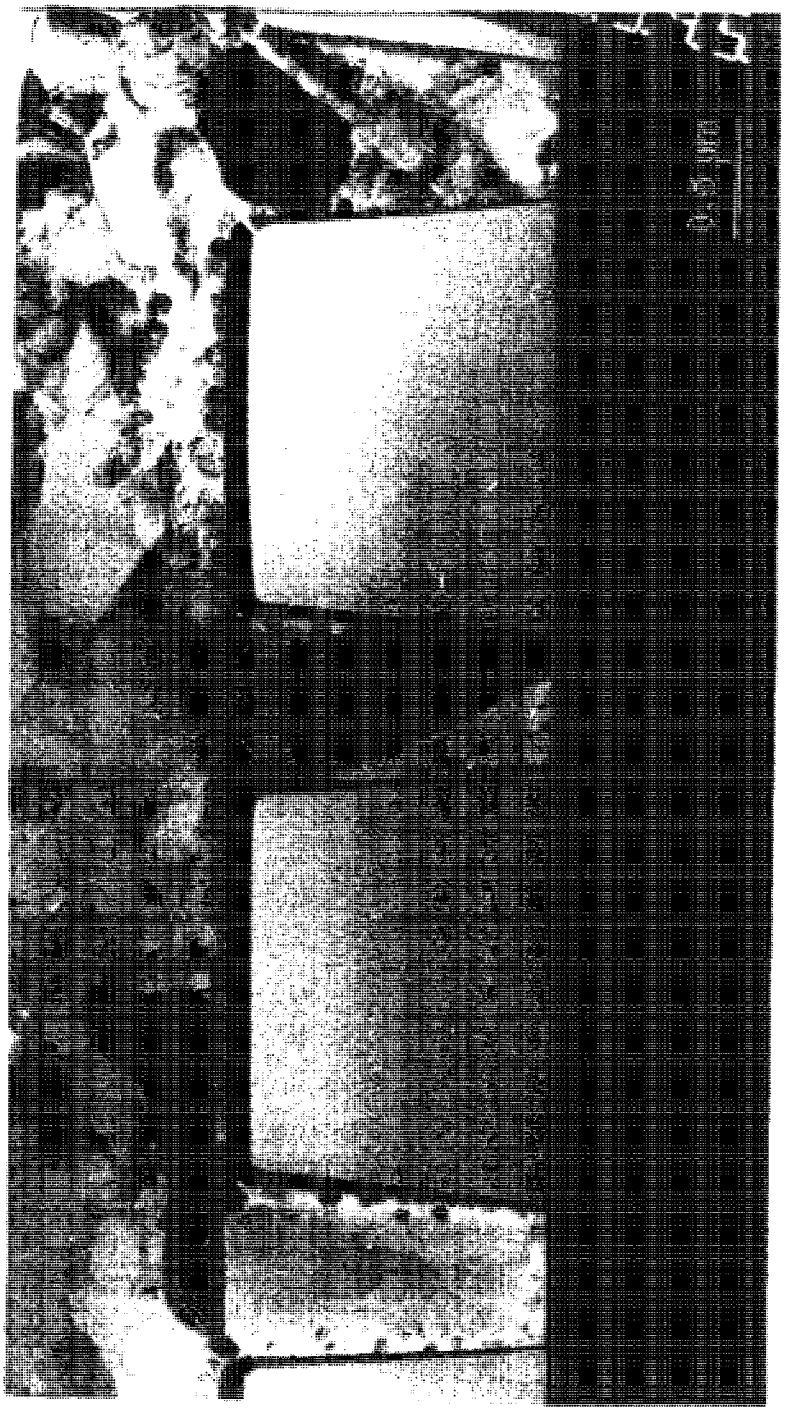
【図5】

図面代用写真



【図8】

図面代用写真



フロントページの続き

(72)発明者　ジェン　シュー
アメリカ合衆国，　カリフォルニア州，
フォスター　シティー，　ハドソン　ベイ
ストリート　279

(72)発明者　ホア　キュー
アメリカ合衆国，　カリフォルニア州，
サニーヴェール，　ウェスト　オリーヴ
215

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【外国語明細書】

1. Title of Invention

TITANIUM ALUMINIDE WETTING LAYER FOR ALUMINUM CONTACTS

2. Claims

1. A method of depositing an aluminum contact layer into an opening in a substrate comprising in sequence,

a) sputter depositing a layer of titanium aluminide through a collimator to cover the bottom and sidewalls of the opening; and

b) sputter depositing a layer of aluminum thereover.

2. A method according to claim 1 wherein $TiAl_x$ is sputtered from a $TiAl_x$ target wherein x is 1-3.

3. A method according to claim 2 wherein $TiAl_x$ is sputtered to a depth of about 50-500 angstroms.

4. A method according to claim 2 wherein x is about 3.

5. A method according to claim 2 wherein aluminum is sputter deposited over the $TiAl_x$ layer at a temperature of about 500-550°C.

6. A method according to claim 2 wherein aluminum is sputter deposited over the $TiAl_x$ layer at a first temperature of about 350-400°C and then sputtered at a second temperature of about 500-550°C to fill said opening.

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7. A method according to claim 1 wherein titanium nitride is sputter deposited as a first layer in the opening to a thickness of about 50-200 angstroms.

8. A method according to claim 7 wherein titanium nitride is sputtered in a first physical vapor deposition chamber, titanium aluminide is sputtered in a second physical vapor deposition chamber and aluminum is sputtered in a third physical vapor deposition chamber while maintaining the substrate under vacuum.

9. An aluminum contact comprising a first layer of titanium nitride about 50-200 angstroms thick, a second layer of titanium aluminide ($TiAl_x$) wherein x is 1-3 having a controlled thickness of 50-500 angstroms, and a third planarized layer of aluminum.

10. An aluminum contact according to claim 9 wherein x is about 3.

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3. Detailed Description of Invention

This invention relates to improved aluminum contacts. More particularly, this invention relates to improved planarized aluminum contacts and method of making them.

BACKGROUND OF THE DISCLOSURE

In the manufacture of aluminum contacts for semiconductor devices, a silicon wafer may be doped to provide source and drain areas for transistors and the like. These areas are then covered with a dielectric such as silicon oxide. In order to connect one integrated circuit layer with another, openings are made in the dielectric layer into which a conductive metal layer, such as aluminum or copper, or aluminum alloys containing minor amounts of copper, is deposited. There are several challenges in making such contact openings. When a conductive metal such as aluminum is deposited adjacent to silicon, subsequent elevated temperature processing causes the aluminum and silicon to react to form a metal silicide. Aluminum silicide is also conductive, leading to "spiking" between the aluminum and the silicon junction.

Thus it has been acceptable practice to deposit a barrier layer, such as a titanium nitride layer, into the contact opening prior to aluminum deposition to prevent this spiking. However, titanium nitride has a higher sheet resistance than aluminum, and thus only a thin layer of titanium nitride can be tolerated without adversely affecting the sheet resistivity of

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the contact. Further, titanium nitride does not wet an overlying aluminum layer well, which leads to adhesion problems between the titanium nitride and the overlying aluminum, i.e., the aluminum delaminates from the titanium nitride. Various methods have been tried to improve the wettability between titanium nitride and aluminum, including depositing a titanium wetting layer over the titanium nitride barrier layer to eliminate the dewetting phenomenon.

However, during subsequent processing, aluminum and titanium react at temperatures as low as about 400°C to form a titanium trialuminide ($TiAl_3$) region at the interface of the titanium and aluminum, which region has a relatively high sheet resistivity as compared to aluminum, and thus will degrade the conductivity of the aluminum film and thus device performance. Additionally, the titanium consumes some of the aluminum deposited thereon during this reaction, further degrading the conductivity of the aluminum film. For example, for a contact opening lined with 500Å of titanium and filled with aluminum, reaction between them to form $TiAl_3$ consumes about 1500Å of aluminum. Still further, formation of a thick titanium trialuminide layer as the aluminum is being deposited in the contact can cause premature closure of the contact openings, particularly for small aperture width contacts, leading to the formation of voids in the contacts.

Thus an improved method of forming aluminum contacts over

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titanium nitride in an opening has been sought.

SUMMARY OF THE INVENTION

We have found that by sputter depositing a layer of titanium aluminide ($TiAl_x$), wherein x is 1-3, having a controlled thickness, into a contact opening as a wetting layer, from 30-60 percent less of the aluminum in the contact is consumed during subsequent processing of the aluminum than when titanium is used as a wetting layer. As a result, the contact sheet resistance of the aluminum contact is both more predictable and lower. Less aluminum needs to be deposited to obtain the same contact sheet resistivity; and planarization of the overlying aluminum layer is improved because the reaction between aluminum and titanium has been greatly reduced..

The contacts of the invention are compatible with dry etch techniques, are readily sputter deposited in a physical vapor deposition (PVD) chamber, and have a sheet resistivity compatible with existing interconnect materials.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 is an illustration of a contact of the invention. A silicon layer 10 having an opening 12 therein includes a first layer 14 of a barrier material such as titanium nitride,

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and a wetting layer 16 of $TiAl_x$ thereover. The opening 12 is then filled with aluminum 18.

According to the method of the invention, a layer of $TiAl_x$ wherein x is 1-3, is deposited in an aperture such as a via or contact opening, in a substrate such as a silicon wafer or a dielectric film layer by sputtering from a $TiAl_x$ target such as one containing 37.2% by weight of aluminum, or a ratio of aluminum:titanium of about 3:5, preferably through a collimator. In this manner, a uniform layer of $TiAl_x$ will be deposited on the sidewalls as well as on the bottom of the aperture, which aperture can have an aspect ratio higher than 2:1. This $TiAl_x$ layer wets the subsequently deposited overlying aluminum layer when it is deposited thereover. Further, since some aluminum, e.g., about 30 percent, is already present in the $TiAl_x$ wetting layer, less reaction will occur between the aluminum contact layer deposited thereon and the wetting layer during subsequent processing than when the wetting layer is titanium alone. Since less of the aluminum layer is consumed by the wetting layer, subsequent high temperature processing will affect the aluminum layer much less, preventing an increase in the metal line sheet resistance and preventing void formation in the aluminum layer.

Titanium, titanium nitride, titanium aluminide and aluminum can be sputter deposited in a PVD chamber as shown in Fig. 2.

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Referring to Fig. 2, a sputtering chamber 20 includes a desired target 22 connected to a DC power source 23 and a substrate support 24. The target 22 can be of titanium, titanium aluminide or aluminum, depending on the material to be deposited. A collimator 26 is mounted between the target 22 and the substrate support 24. A source of RF power 28 is connected to the substrate support 24. A gas inlet manifold 30 permits various gases, such as argon or nitrogen, to be controllably passed into the chamber. During processing, a substrate 32 is mounted on the substrate support 24.

The preparation of a typical aluminum contact is described hereinbelow. A thin titanium nitride layer, e.g., from about 50-200Å thick, is first deposited in the aperture. This layer can be formed by sputtering a titanium target in the presence of nitrogen gas in the chamber. The titanium nitride layer may be annealed or stuffed with oxygen in known manner if desired.

To carry out the titanium aluminide deposition, a substrate is provided having a plurality of exposed openings in which aluminum contacts are to be formed. After mounting the substrate 32 onto the substrate support 24, a flow of argon is started in the chamber, whereupon titanium aluminide is sputtered from the titanium aluminide target 22 onto the substrate 32. By sputtering through the collimator 26, a layer of $TiAl_3$ is deposited on the sidewalls in addition to being

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deposited on the bottom of the exposed openings, and openings having higher aspect ratios can be filled.

In the following example, contact openings in a silicon layer having a layer of thermal silicon oxide thereon were made using standard photolithographic techniques. The contact openings varied in size, i.e., 0.6, 0.8 and 1.0 micron in diameter and were 1.2 microns deep.

Control - Sputtered Titanium as a Wetting Layer

Layers of titanium of various thickness were deposited in contact openings 0.6 micron in diameter having a 2:1 aspect ratio (1.2 micron deep). The titanium was sputter deposited using a 1:1 aspect ratio collimator. Aluminum was sputter deposited over the titanium layers. A determination was made of the aluminum fill and planarization. The deposition of aluminum was also varied and included a hot aluminum deposition (510-550°C), cold/hot aluminum deposition (initial temperature about 400°C with a subsequent increase in temperature to about 500-550°C), and power applied to the target during the deposition. All of the data of Figs. 3A to 3D were measured using 0.6 micron diameter openings.

Fig. 3A illustrates the percent of contact fill for the hot aluminum deposition. The percent fill varies from about 65-96%, with the optimum temperature being about 530°C.

Fig. 3B is a graph of percent contact fill versus temperature of the aluminum deposition which shows that optimum

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fill is achieved by depositing 2000Å of aluminum cold (400°C) and 6000Å of aluminum hot (530°C), although this can be varied to depositing 3000Å of cold aluminum and 5000Å of hot aluminum with little loss in percentage of contact fill.

Fig. 3C is a graph of percent contact fill versus power during the hot aluminum deposition which shows that the deposition of aluminum at low power is preferred.

The optimum thickness of titanium for wettability and percent contact fill is about 400Å, as shown in Fig. 3D. Since wall coverage is low, only about 14 percent at the bottom of a 2:1 aspect ratio opening, the minimum thickness for the titanium layer is about 50-60Å. At a higher titanium layer thickness of about 550Å, the overhang formed at the top of the opening prevents aluminum reflow into the opening.

Fig. 4A is a photomicrograph of a cross section of a contact filled with 400Å of titanium and then aluminum deposited by the cold/hot process.

Fig. 4B is a photomicrograph of a TEM analysis of the contact of Fig. 4A. A layer of $TiAl_3$ about 2000Å thick was measured.

Example 1 - Sputtered $TiAl_x$ as a Wetting Layer

After sputter depositing a layer of $TiAl_3$ into contact openings as in the Control, aluminum was sputter deposited using a 1:1 aspect ratio collimator into the contact openings.

Rutherford Backscattering analysis of the resultant films

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showed an Al:Ti ratio of about 3.5:1, or that an alloy containing 77.8% of aluminum and 22.2% of titanium was deposited. The resistivity of the $TiAl_3$ film was 158.96 μohms-cm, which confirms $TiAl_3$ formation. The sheet resistance uniformity of the sputtered $TiAl_3$ layer was about 2.266 percent, 1 sigma.

Aluminum was then deposited over the $TiAl_3$ layer using both the hot and the cold/hot processes.

Fig. 5 is a graph of percent fill of the overlying aluminum layer versus $TiAl_3$ layer thickness in angstroms for aluminum deposited by both the hot deposition and the cold/hot deposition methods. It is apparent that the hot process aluminum deposition gives excellent fill at any film thickness of $TiAl_3$. When depositing aluminum using the cold/hot process, the optimum percent fill is not obtained until a film of $TiAl_3$ at least about 1000Å thick is deposited.

Fig. 6 shows excellent fill of contact openings 0.6 micron in diameter with 400Å of $TiAl_3$ and 8000Å of aluminum deposited using the hot process.

Fig. 7 is a photomicrograph of a TEM analysis of the interface between a $TiAl_3$ layer and aluminum.

The above process requires only two sputter deposition chambers; one to sputter deposit the $TiAl_x$ alloy and a second to sputter deposit aluminum thereover. A suitable multi-chamber deposition system has been disclosed by Maydan et al in US

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Patent 4,951,601, incorporated hereby by reference, and is shown schematically in Fig. 8.

Fig. 8 illustrates a preferred deposition system in which all of the deposition and treatment steps of the present process can be carried out. This system comprises a plurality of processing vacuum chambers connected to a high vacuum substrate transfer chamber. Each of the processing chambers processes a single wafer at a time, but multiple wafers are accommodated in the system by parallel processing in the various chambers. The system 800 of Fig. 8 includes two independently operated load lock chambers 810A and 810B for loading and unloading substrates into the system. The substrates are transferred from load lock chamber 810A into a substrate transfer chamber 812 which includes a robot 813 for transfer of substrates to various of the connected processing chambers. For example, a preclean chamber 816 can be used to sputter clean or plasma clean the substrate to remove the native oxide layer from air exposed silicon substrates. The substrate can then be transferred to various processing chambers. For example, a titanium nitride layer can be deposited in chamber 820, the titanium aluminide layer can be deposited in chamber 822, and the aluminum layer can be deposited in chamber 826. The coated substrate is then transferred to the load lock chamber 810B for transfer out of the system 800.

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Additional processing chambers, as for heating or annealing and the like, can be added to the system 800.

Using a 1:1 aspect ratio collimator, a deposition rate of 2.91Å/kw is achieved.

In a preferred method of forming aluminum contacts, a first layer about 50~200Å thick of titanium nitride is sputter deposited in an opening and annealed in oxygen in conventional manner. The substrate is transferred to a chamber containing a titanium aluminide target and a $TiAl_x$ layer about 50-500Å thick is deposited using argon gas and a collimator in the chamber.

The substrate is then transferred to another sputtering chamber for the deposition of aluminum.

In a hot aluminum process, the substrate support is heated to a temperature of about 500°C or higher.

Using a cold/hot process, a first deposit of aluminum a few thousand angstroms thick is made at 350-400°C, and the substrate support then heated up to about 550°C and deposition continued to the desired aluminum thickness. The initial cold deposition of aluminum ensures good wetting between the titanium aluminide and aluminum layers. By increasing the temperature during deposition to a temperature above the flow point of the aluminum, e.g., about 550°C, the aluminum flows as it is deposited, eliminating the formation of voids in the aluminum layer. Heated argon can also be passed through the wafer support to raise the temperature of the substrate

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rapidly.

Only about 3500Å of aluminum is required to fill a contact to obtain the desired sheet resistance. Since little reaction takes place between aluminum and titanium during subsequent high temperature processing, the resistance of the contact remains low.

The stability of the contact resistance has another advantage in that it prevents electron migration effects of the aluminum line during operation of devices. If the aluminum sheet resistance increases over time, as when aluminum is consumed by reaction with titanium, the current density increases and electron migration in the aluminum line also increases, which can lead to breaks in the aluminum line.

Although the invention has been described in terms of specific embodiments, various changes in the materials, reaction conditions, and the like can be made by one skilled in the art and are meant to be included herein.

4. Brief Description of Drawings

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a cross sectional view of a contact of the invention.

Fig. 2 is a schematic view of a sputtering chamber in which the materials employed in the process of the invention can be deposited.

Fig. 3A is a graph of percent contact fill versus temperature for a hot aluminum deposition.

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Fig. 3B is a graph of percent contact fill versus hot/cold ratio of aluminum deposition.

Fig. 3C is a graph of percent contact fill versus power during aluminum deposition.

Fig. 3D is a graph of percent contact fill versus titanium thickness.

Fig. 4A is an SEM photograph of a cross section of a contact made using a titanium wetting layer.

Fig. 4B is a TEM photograph of a cross section of a contact made using a titanium wetting layer showing formation of a titanium aluminide layer.

Fig. 5 is a graph of percent aluminum fill versus titanium aluminide thickness for both hot aluminum deposition and cold/hot aluminum deposition.

Fig. 6 is an SEM photograph of a cross section of a contact made using titanium aluminide as a wetting layer.

Fig. 7 is a TEM photograph of a cross section of a contact made using titanium aluminide as a wetting layer.

Fig. 8 is a plan view of a multi-chamber vacuum deposition system useful for carrying out the present invention.

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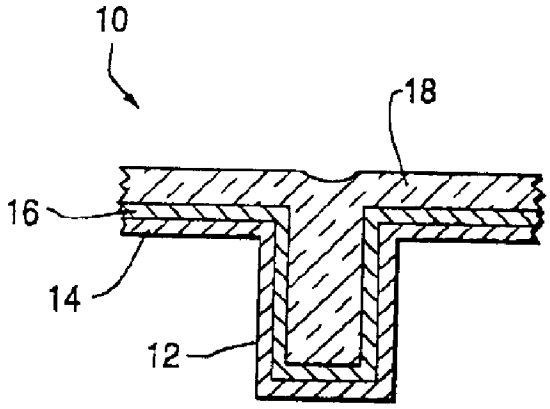


FIG. 1

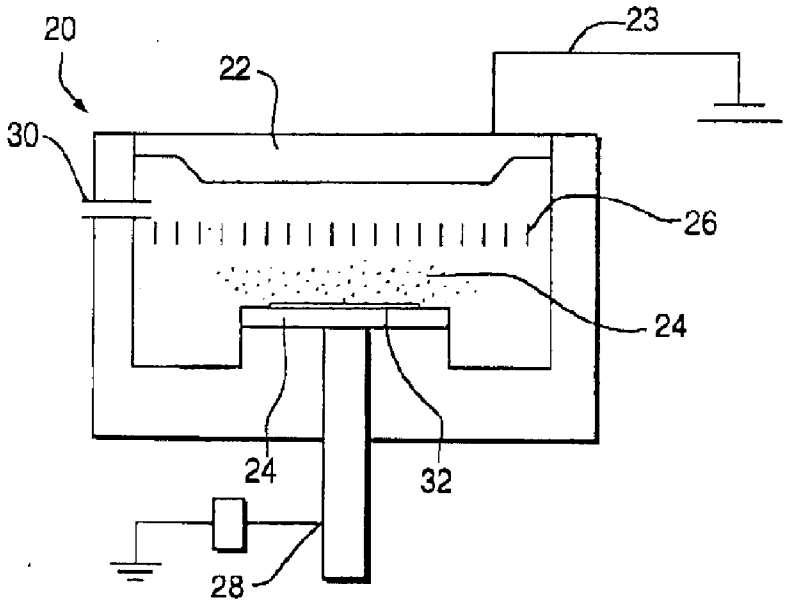


FIG. 2

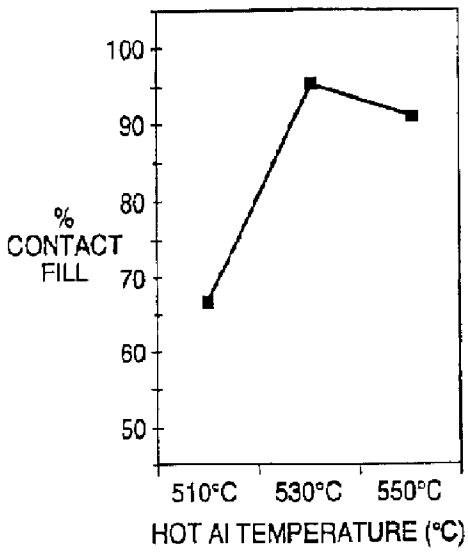


FIG. 3A

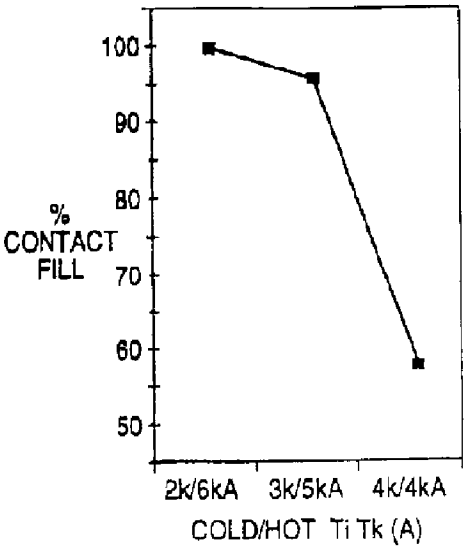


FIG. 3B

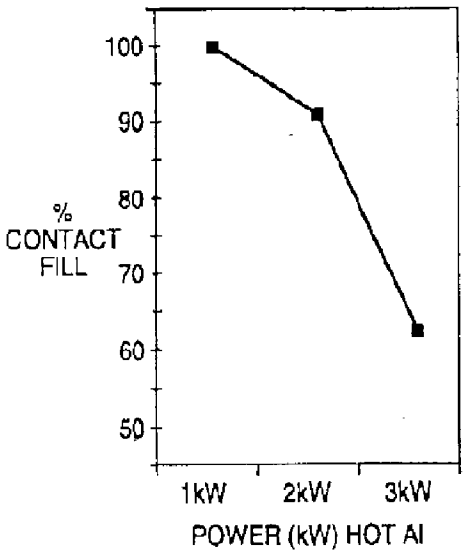


FIG. 3C

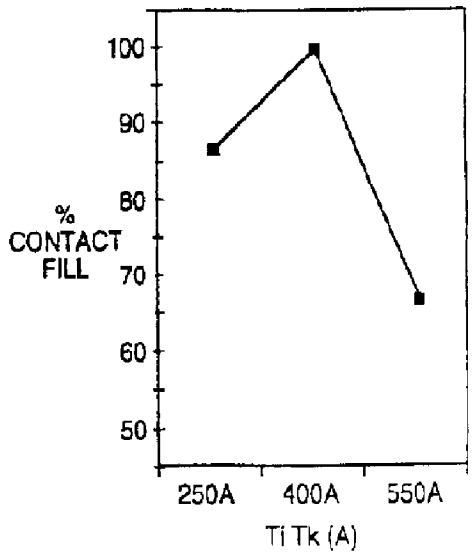


FIG. 3D

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P97AM－003

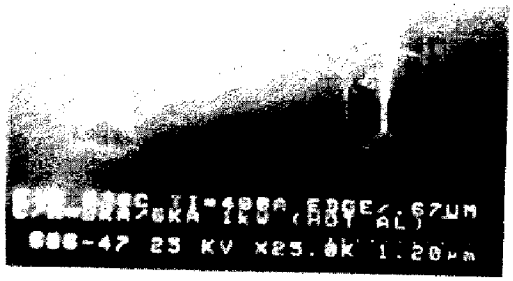


FIG. 4A

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FIG. 4B

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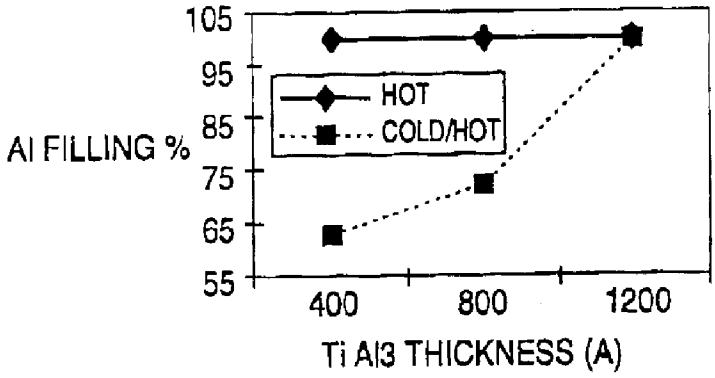

105
95
85
75
65
55
Al FILLING %
HOT
COLD/HOT
400
800
1200
Ti Al3 THICKNESS (A)

FIG. 5

(7)

P97AM－003

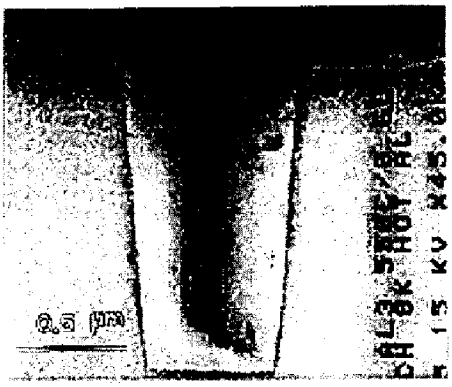


FIG. 6

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P97AM－003



FIG. 7

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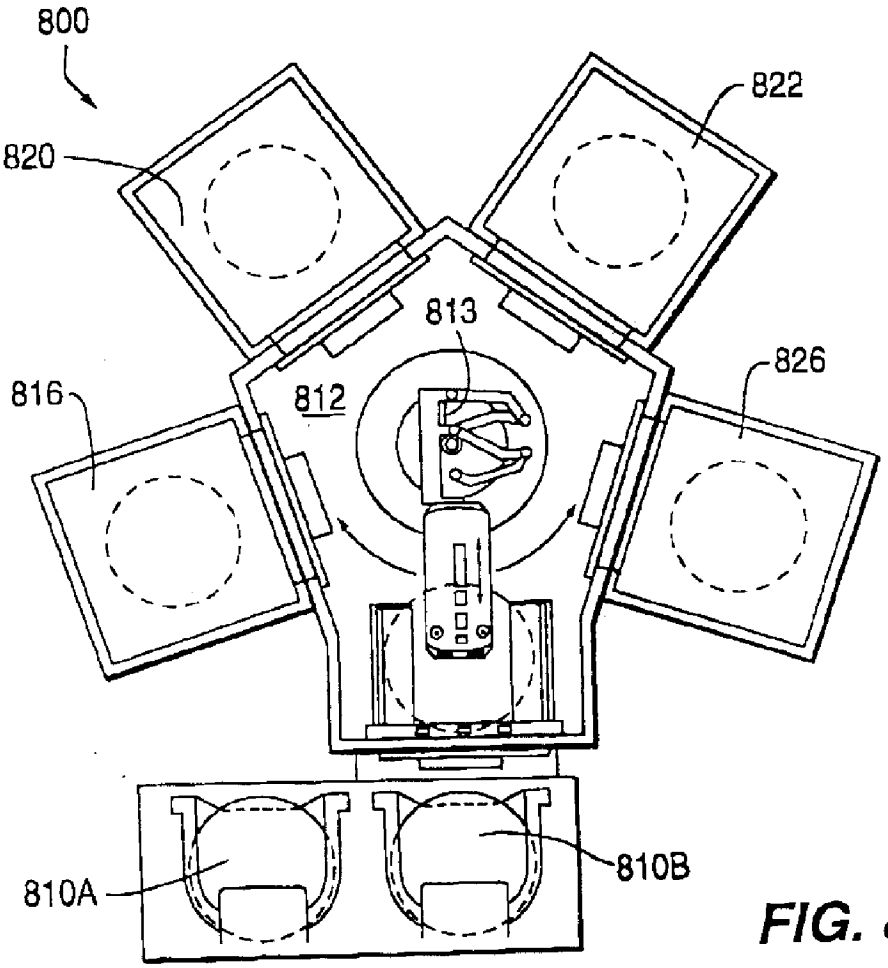


FIG. 8

1. Abstract

ABSTRACT OF THE DISCLOSURE

An improved aluminum contact and method of forming it in an opening in a substrate comprising sputter depositing a titanium aluminide wetting layer in the opening and depositing an aluminum layer thereover. The titanium aluminide wetting layer has a controlled thickness.

2. Representative Drawing

Fig. 1

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JPH1074707A TITANIUM ALUMINIDE WETTING LAYER FOR ALUMINUM CONTACT

Applicants: APPLIED MATERIALS INC

Inventors: KIEU HOA,XU ZHENG,YAO GONGDA

Classifications:

IPC ***C23C14/06; H01L21/203; H01L21/28; H01L21/285; H01L21/768;*** (IPC1-7): C23C14/06; H01L21/203; H01L21/28; H01L21/285; H01L21/768;

CPC **H01L21/76843 (EP);**

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TITANIUM ALUMINIDE WETTING LAYER FOR ALUMINUM CONTACT

Abstract

PROBLEM TO BE SOLVED: To form an aluminum contact on a titanium nitride with a good adhesive property in an opening, by sputter-depositing a layer of titanium aluminide into a contact opening as a wetting layer, and sputter-depositing a layer of aluminum after that. SOLUTION: A layer of silicon 10 having an opening 12 contains a barrier layer 14 of titanium nitride and a wetting layer 16 of TiAlx (in the formula x is 1-3) provided on it. After that, the opening 12 is filled up with aluminum 18. Namely, argon begins to flow in a chamber, after a board having an opening 12 is fitted to a board supporting part, and titanium aluminide is sputtered from a titanium aluminide target on the board. By sputtering through a collimator, a TiAlx layer is deposited on the bottom of the opening 12, and is deposited on the lateral wall also. After that, aluminum is sputter-deposited on a layer of titanium.

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DESCRIPTION JPH1074707

[0001]
The present invention relates to improved aluminum contacts. In particular, the present invention relates to planarized aluminum contacts and methods of making the same.

[0002]

BACKGROUND OF THE INVENTION In the manufacture of aluminum contacts for semiconductor devices, silicon wafers can be doped to provide source and drain regions for transistors and the like. In order to connect one integrated circuit layer with another, openings are deposited with a conductive metal such as aluminum or copper, or an aluminum alloy containing a small amount of copper. Built inside. There are several attempts in the manufacture of such contact openings. When a conductive metal such as aluminum is deposited adjacent to silicon (silicon), subsequent high temperature processing causes the aluminum and silicon to react to form a metal silicide. Aluminum silicides are also conductive and cause "spiking" between the aluminum and silicon junctions.

[0003]

It has been an acceptable practice to deposit a barrier layer, such as a titanium nitride layer, in the contact openings prior to aluminum deposition to avoid this spiking. However, titanium nitride has a higher sheet resistance than aluminum, so only a thin layer of titanium nitride can

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withstand the sheet resistivity of a contact without acting in the opposite direction. .. In addition, titanium nitride does not wet the overlying aluminum layer well, which causes adhesion problems between the titanium nitride and the overlying aluminum, ie the aluminum delamination from the titanium nitride. Various methods to improve the wettability between titanium nitride and aluminum, including depositing a titanium wetting layer on the titanium nitride barrier layer to eliminate the dewetting phenomenon. It has been tried.

[0004]

However, during subsequent processing, aluminum and titanium react at temperatures as low as about 400 ° C, forming titanium-trialuminide (TiAl3) regions at the titanium-aluminum interface, which are compared to aluminum. It has a relatively high sheet resistivity, which reduces the conductivity of the aluminum film and thus the device capability. Furthermore, titanium consumes some of the aluminum deposited on it during this reaction, further reducing the conductivity of the aluminum film. For example, for contact openings filled with 500 Å of titanium lined aluminum, the reaction between them to form TiAl3 consumes about 1500 Å of aluminum. Still further, as aluminum is deposited in the contact, the formation of a thick titanium trialuminide layer causes premature blockage of the contact opening and formation of voids in the contact, especially for contacts of small opening width.

[0005]
Thus, there has been a need for improved methods of forming aluminum contacts on titanium nitride in the openings.

[0006]

SUMMARY OF THE INVENTION We sputter deposit a layer of titanium aluminide (TiAlx, where x is 1-3) with a controlled thickness in the contact opening as a wetting layer. Have found that during subsequent aluminization, 30-60% less aluminum is consumed in the contact than when titanium is used as the wetting layer.

As a result, the contact sheet resistance of aluminum contacts is more predictable and lower. Less aluminum needs to be deposited to obtain a similar contact sheet resistivity and the planarization of the overlying aluminum layer is improved because the reaction between aluminum and titanium is greatly reduced.

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[0007]
The contacts of the present invention are compatible with dry etch techniques and are easily sputter deposited in a physical vapor deposition chamber to provide sheet resistivity compatible with the presence of interconnecting materials. Have.

[0008]

DETAILED DESCRIPTION OF THE INVENTION FIG. 1 is an example of a contact of the present invention.

Silicon layer 10 having openings 12 therein includes a first layer 14 of barrier material such as titanium nitride and a wetting layer 16 of TiAlx thereon. After that, the opening 12 is filled with aluminum 18.

[0009]

According to the method of the present invention, a layer of TiAlx where x is 1-3 contains 37.8% by weight of aluminum, or by sputtering from a TiAlx target having an aluminum: titanium ratio of about 3: 5. It is deposited in a substrate such as a silicon wafer or a dielectric film layer, preferably through a collimator, into an aperture such as a via or contact opening. In this way, a homogeneous layer of TiAlx is deposited on the bottom as well as on the sidewalls of the aperture, the aperture having an aspect ratio higher than 2: 1. This TiAlx layer wets the subsequently deposited and overlying aluminum layer as it is deposited thereon. In addition, some aluminum, eg, 30 percent, is already present in the TiAlx wetting layer, so that the wetting layer is titanium alone between the aluminum contact layer and the wetting layer deposited thereon during subsequent processing. Sometimes less reaction occurs. Subsequent high temperature treatment acts very little on the aluminum layer, as less of the aluminum layer is consumed by the wetting layer, preventing an increase in metal line sheet resistance and preventing the formation of voids in the aluminum layer. .

[0010]
Titanium, titanium nitride, titanium aluminide and aluminum can be sputter deposited in a PVD chamber as shown in FIG.

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[0011]

Referring to FIG. 2, the sputtering chamber 20 includes a DC power source 23 and a desired target 22 coupled to a substrate support 24.

The target 22 may consist of titanium, titanium aluminide or aluminum, depending on the material being deposited. The collimator 26 is attached between the target 22 and the substrate support 24. RF power source 28 is coupled to substrate support 24. The gas inlet manifold 30 allows the various gases such as argon or nitrogen to be controllably passed through the chamber. During processing, the substrate 32 is mounted on the substrate support 24.

[0012]

The preparation of a typical aluminum contact is described below. A thin titanium nitride layer, for example 50-200 Å thick, is first deposited in the aperture. This layer can be formed by sputtering a titanium target in the presence of nitrogen gas in the chamber. The titanium nitride layer may be annealed or oxygen filled in known manner if desired.

[0013]

To perform the titanium aluminide deposition, a substrate is provided having a plurality of exposed openings in which aluminum contacts are formed. After mounting the substrate 32 on the substrate support 24, a flow of argon is initiated in the chamber and titanium aluminide is sputtered from the titanium aluminide target 22 on the substrate 32. By sputtering through collimator 26, a layer of TiAl3 can be deposited on the sidewalls as well as on the bottom of the exposed openings, filling the openings with higher aspect ratios.

[0014]

In the following examples, contact openings in a silicon layer with a layer of thermal silicon oxide thereon were made using standard photolithographic techniques. The contact openings were

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manufactured in varying sizes or diameters of 0.6, 0.8, and 1.0 microns and were 1.2 microns deep.

[0015]

Controlled-Sputtered Titanium as Wetting Layer Layers of titanium of various thicknesses were deposited in 0.6 micron diameter contact openings having an aspect ratio of 2: 1 (1.2 micron depth). It was Titanium was sputter deposited using a 1: 1 aspect ratio collimator. Aluminum was sputter deposited on the titanium layer. Measurements were made on aluminum fill and planarization. Aluminum deposition can also be varied, hot aluminum deposition (510-550 ° C), cold / hot aluminum deposition (initial temperature about 400 ° C up to about 500-550 ° C with subsequent temperature rise), and The applied power of the target was included during deposition. All data in Figures 3 (a) to 3 (d) were measured using a 0.6 micron diameter opening.

[0016]

FIG. 3 (a) shows the percentage of contact fill for hot aluminum deposition. Percent fill varies about 65-96% with an optimum temperature of about 530 ° C.

[0017]

FIG. 3 (b) is a graph of percent contact fill versus temperature of aluminum deposition, which can be varied to deposit 3000 Å of cold aluminum and 5000 Å of hot aluminum with little loss of contact fill. , Shows that optimum fill is achieved by deposition of 2000 Å aluminum cold (400 ° C.) and 6000 Å aluminum hot (530 ° C.).

[0018]

FIG. 3 (c) is a graph of percent contact fill versus power during hot aluminum deposition, showing that aluminum deposition at low power is preferred.

[0019]

The optimum titanium thickness for wettability and percent contact fill is about 400 Å, as shown in FIG. 3 (d).

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Since the wall coverage is low and only about 14 percent at the bottom of the 2: 1 aspect ratio opening, the minimum thickness for the titanium layer is about 50-60 Å.

At higher titanium layer thicknesses of about 550 Å, the overhang formed at the top of the opening prevents reflow of aluminum into the opening.

[0020]
FIG. 4 (a) is a photomicrograph of a cross section of a contact filled with 400 Å of titanium and then aluminum deposited by a cold / hot process.

[0021]

FIG. 4 (b) is a TEM micrograph of the contact of FIG. 4 (a).

A layer of TiAl3 about 2000 Å thick was measured.

[0022]
Example 1-Sputtered TiAlx as Wetting Layer After sputter deposition of a layer of TiAl3 in the contact openings as in Control, the aluminum has a 1: 1 aspect ratio collimator in the contact openings. It was sputter deposited using.

[0023]

Rutherford Backscattering analysis of the resulting film showed that an Ai: Ti ratio of about 3.5: 1 or an alloy containing 77.8% aluminum and 22.2% titanium was deposited. It was

The resistivity of TiAl3 is 158. It was 96 μ ohms-cm confirming the formation of TiAl3. The sheet resistance uniformity of the sputtered TiAl3 layer was about 2.266 percent, 1 sigma.

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[0024]
Aluminum was then deposited on the TiAl3 layer using both hot and cold / hot processes.

[0025]

FIG. 5 is a graph of the percent fill of an overlying aluminum layer versus the thickness of the TiAl3 layer in Angstroms for aluminum deposited by both hot and hot / cold deposition methods.

It is clear that hot aluminum deposition gives excellent fill at any film thickness of TiAl3. When depositing aluminum using the cold / hot process, optimum percent fill is not obtained until a film of TiAl3 is deposited at a thickness of at least 1000 Å.

[0026]
FIG. 6 shows the excellent filling of 0.6 micron diameter contact openings with 400 Å TiAl 3 and 8000 Å aluminum deposited using a hot process.

[0027]
FIG. 7 is a TEM micrograph of the interface between the TiAl3 layer and aluminum.

[0028]

The above process requires only two sputter deposition chambers, the first is to sputter deposit a TiAlx alloy and the second is to sputter deposit aluminum on it.

A suitable multi-chamber deposition system is disclosed by Maydan et al. In US Pat. No. 4,951,601, which is hereby incorporated by reference, and is shown schematically in FIG.

[0029]

FIG. 8 shows a preferred deposition system in which all of the deposition and processing steps of

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this process can be performed.

The system includes a plurality of processing vacuum chambers connected to a high vacuum substrate transfer chamber. Each of the processing chambers processes a single wafer at the same time, but multiple wafers are accommodated in the system by parellel processing in various chambers. The system 800 of FIG. 8 includes two independently operated load lock chambers 810A and 810B for loading and unloading substrates into the system. The substrate is moved from the load lock chamber 810A into a substrate transfer chamber 812 that includes a robot 813 for transfer of the substrate to various connected processing chambers. For example, the preclean chamber 816 can be used to sputter or plasma clean a substrate to remove native oxide layers from a silicon substrate exposed to air. The substrate can then be moved to various processing chambers. For example, a titanium nitride layer can be deposited in chamber 820, a titanium aluminide layer can be deposited in chamber 822, and an aluminum layer can be deposited in chamber 826. The coated substrate is then moved from system 800 to load lock chamber 810B for transfer.

[0030]
Additional processing chambers can be added to the system 800 for heating or annealing and similar purposes.

[0031]
A deposition rate of 2.91 Å/ kw is achieved using a 1: 1 aspect ratio collimator.

[0032]

In the preferred method of forming aluminum contacts, a first layer of titanium nitride about 50-200 Å thick is sputter deposited in the openings and annealed in oxygen in the conventional manner.

The substrate is moved to a chamber containing a titanium aluminide target and a TiAlx layer approximately 50-500 .ANG. Thick is deposited using argon gas and a collimator in the chamber.

[0033]
The substrate is then moved to another sputtering chamber for aluminum deposition.

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[0034]
In the hot aluminum process, the substrate support is heated to a temperature of about 500 ° C or higher.

[0035]

Using a cold / hot process, a first deposition of aluminum with a thickness of several thousand angstroms was done at 350-400 ° C, after which the substrate support was heated to about 550 ° C and the deposition was performed to the desired aluminum It continues until now.

The first cold deposition of aluminum ensures good wetting between the titanium aluminide and the aluminum layer.

By increasing the temperature during deposition to a temperature above the aluminum flow point, for example up to about 550 ° C., the aluminum is removed while removing the formation of voids in the aluminum layer. To flow.

Heated argon can also be passed through the wafer support to rapidly raise the temperature of the substrate.

[0036]

Only about 3500 Å of aluminum is needed to fill the contacts to obtain the desired sheet resistance. The resistance of the contact remains low because little reaction takes place between aluminum and titanium during the subsequent high temperature treatment.

[0037]

The stability of contact resistance has other advantages in preventing electron migration effects of the aluminum line during operation of the device. If the aluminum sheet resistance increases

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over time, such as when aluminum is consumed by the reaction with titanium, the current density increases and the electron transfer in the aluminum line also increases, which means that in the aluminum line. Can lead to destruction in.

[0038]
Although the present invention has been described in terms of particular embodiments, various modifications in materials, reaction conditions, and the like can be made by those of ordinary skill in the art, which are herein described. Means to be included in.

[0039]
Brief description of the drawings

[0040]
1 is a cross-sectional view of the contact of the present invention.

[0041]
2 is a schematic diagram of a sputtering chamber in which the material used in the process of the present invention can be deposited.

[0042]

FIG. 3 (a) is a graph of percent contact fill versus temperature for hot aluminum deposition.

(B) is a graph of percent contact fill versus hot / cold aluminum deposition.

(C) is a graph of percent contact fill versus power during aluminum deposition.

(D) is a graph of percent contact fill versus titanium thickness.

[0043]

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FIG. 4A is a SEM photograph of a cross section of a contact manufactured using the titanium wetting layer.

(B) is a TEM photograph of a cross section of a contact manufactured using a titanium wetting layer showing the formation of a titanium aluminide layer.

[0044]
FIG. 5 is a graph of percent aluminum fill versus titanium aluminide thickness for both hot aluminum and cold / hot aluminum deposition.

[0045]
FIG. 6 is a SEM photograph of a cross section of a contact manufactured using titanium aluminide as a wetting layer.

[0046]
FIG. 7 is a TEM photograph of a cross section of a contact manufactured using titanium aluminide as a wetting layer.

[0047]
FIG. 8 is a plan view of a multi-chamber vacuum deposition system useful for practicing the present invention.

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CLAIMS JPH1074707

1.
a) sputter depositing a layer of titanium aluminide through a collimator to cover the bottom and sidewalls of the opening, and b) sputter depositing a layer of aluminum on top of the aluminum in the opening in the substrate. A method of depositing a contact layer.

2.
The method of claim 1, wherein x is 1-3 and TiAlx is sputtered from a TiAlx target.

3.
The method of claim 2 wherein TiAlx is sputtered to a depth of about 50-500 Angstroms.

4.
The method of claim 2, wherein x is about 3.

5.
The method of claim 2, wherein aluminum is sputter deposited on the TiAlx layer at a temperature of about 500-550 ° C.

6.
The method of claim 2 wherein aluminum is sputter deposited at a first temperature of about

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350-400 ° C on the TiAlx layer to fill the opening and then sputtered at a second temperature of about 500-550 ° C.

7.
The method of claim 1 wherein titanium nitride is sputter deposited to a thickness of about 50-200 Å as the first layer in the opening.

8.
While maintaining the substrate under vacuum, titanium nitride is sputtered in the first physical vapor deposition chamber, titanium aluminide is sputtered in the second physical vapor deposition chamber, and aluminum is sputtered in the third physical vapor deposition chamber. The method of claim 7, wherein the method is sputtered in a vapor deposition chamber.

9.
A first layer of titanium nitride about 50-200 angstroms thick, a second layer of titanium aluminide (TiAlx, x 1-3) with a controlled thickness of 50-500 angstroms, and a first layer of aluminum. Aluminum contact with 3 planarized layers.

10.
The aluminum contact of claim 9 wherein x is about 3.

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PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/847,878	06/17/2020 05:30:56 PM ET	3771-0003-DC13

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8164	FILED BY	Sarah Zizzo
PATENT CENTER #	60039909	FILING DATE	04/14/2020
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

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Appendix_E4.pdf	59352651B5E5D5CD603676625B51B07FB4C73B91878AFDCAF82A0A4F4D83EDCE986510B54B3581F96EBE444152A2FC8800EA3896B21F3FC20E70060CB8D6902B
Appendix_E7.pdf	6C9AB55E912246BEC81EF4C68956B13A8214F90506AE433C3A7B23D63C6EDDDAE7BBEA71A8F028B53C4D5F854803C2D927A8224F714C6FB4CC7AD0D5B8585807
Appendix_F2.pdf	EC22062ED504CA252F29932C7D19733D3EA75B2C07DDCCB001F2F5D4BD52CBEA01FD2D5F6AF9CAEFAF8B4C886BCF8D7A26C364156062680FCFF615A89EE1E20F
Appendix_F3.pdf	A73BB2A2FFC12E50A99D951050394E706AE5072DCD292B0030FB32C31FCF472070D0548B29EADBFACA4FE6D3423EF26A58DAD93ECC4C28B81C9A2028BADDA2FC
WALDROP_1993.pdf	49321F6ACF8D9B4574DE432772801B7589D0957FA9889040708EBE3413909C3237222B43CE8C2F10674396817094F35DB37382FC0D450AD2F5A99CBFD8760081
EP0458353A2.pdf	DC7748F2715F02D3C130FC901B20A7F611F3705BFB0A43B1396236AD7D2B16EFDD3C8AEF0B719AF8AA848434350CD47EDDBC2FB5F25CEB4440942A83F87FEE2F
FR2814856A1.pdf	CAC1222F6F2852B0809C6BD30EE9940075486F18C130B84524FAE6140FB8146154855308CA510DEE59196C21507F397FDC2E93589293DC983067643EC1D93B66
EP0789388A2.pdf	BF5A9D6988918E0D39D20D362B995A0BC2EF03DCD031D5C7943167340BAF7AA366B06B14DDB99E3AF06198B84F71591423C4E0C455C54D64709851D4F0D0724D
JP3208599B2_wTransl.pdf	7F84E4D67A725021E1927EAE73367AF3BC5FBD9A95BDCF9EFC5181E2675B41FC2CE8D41150CF616A8B4D4340F68416525B9791B9624834558A4C55E63A2997E7

JP2000236086A_wTransl.pdf	E703208BC36577BF5C313604A5C7B1DA1E0A211F06E6FA5F7 ADA72EEFE72D613B9368E2E1A1CD23F6F908F4987F6C52F48 28AC2125B65A300161039EC60F40C2
Appendix_F10.pdf	424103E783804DA38472D31BE2ED8BCD754D4EA63D2620BC3 ECF320058B7A444F44E399F7222E4428467F64828007E3CBAE 5A498E7FD7551E7BD4D99825A8839
Appendix_F7.pdf	8104BBB0790A9779ACF3C38D7E3C262005EC84983A74DCA0C 19085DEBB943BF84565104F19D3172733741B4CDBBE34C4D4 F7CDC6691869E42E1256644B3A073E
SCHMIDT.pdf	3FD9801407CE800094F98693B3260759768846003 90FA070EF8 C0B14569CBA12B61C3D73DFD1A4D19D02B7A6C9CE88E7077 8B782DC2AE015E4A41CCEBAD6C650
EP0111364A2.pdf	5BA4CA24465A5EDD29FA0CCE9C0261CFE13C909502868D17 882EC9A59DCF798202BFC7448799EFCCAD20C9E1D6484907 D101DCBCBBEEA6CDDC8AC27441DA9803
JP2002184978A_wTransl.pdf	D2C6EAC1843DEA3E62E4EE08E65C5F425C5821E6FDCA50FD 81EFE2EC6A1F0487ADB0322502AAD34F915FDD473012DE29C 5667028051362601830189 97BFA6F9D
JPH065737B2_wTransl.pdf	4E85EE3729250F924EB07D169CD0B5A3668CB9847E037E91F2 74440EF9F1CAFE31470F5A27DE46C5631610A47669E8353960 1FC5732425A1BD00C9B7541CFD6A
JP2001223180A_wTransl.pdf	A60045944270814A04D286B3020A756E60217BC55BAB0DDB01 27598C92D7FD2F84E5114B2E94913B53C55E7DF7213E094D72 50DD647FAFE16C2727C7AC60BAEA
JPH0329355A_wTransl.pdf	0975F4909CD677A66E6ADF12294A2EA7BA80AED8E56A08331 A5DA1B959FF6959526C36B27B7EB84DFE0A941F7D7570CCF1 F840031F85348F7E4D6F7B3C1390A3
Appendix_B4.pdf	75A7EF7609870081BFB1B07D4912C74F5B6E51D6544B3ABC5 445B928CF129639C995878B51297C58ACCF18BEEEFD9E25F5 B26D2AC425A3D435CA98519925E5DE

Appendix_B7.pdf	04FC67B29A188D229B24DA7ABBC97D91E44CCFD066243DA7238F81E9C84E6B5E4A494AF1DE848F0B2C22A3EDEE2B95662E66ABFE5BB78928DDE8D4CE19E8CC6E
Appendix_C1.pdf	4FB8CEFBA8DE622DBACB1AFF066EF88630CCF69E8731DFD17DC6B6035C99CA864B1A96BCDFC8E1FF28453EDCB43BA27E33DF244C7175192C674A4B651F45DFFB
JP3191728B2_wTransl.pdf	455E6F179790B378C0D516F8D8B37BB0703F2F83A8EB9964D3CC1DD4079C9884B1902178C2CF48C902104A7F35A47BC2057092762C098BD38A64A7EBE4F28180
JP2000174261A_wTransl.pdf	C533DAE2C93CB78244CE9036487AC9B7D676F23A576B121F1A98E3DF5ACCB113289FCD4A944786C360487582265E51BDDE5B8C511E637BDAEEBB713104756CBE
JP2000101100A_wTransl.pdf	49B2F35C0B573395C93D23D8FB864E340CA51CC4E4B70E15EFB6A596B4E5FA202B65EC1D53A080A162839C63E2E31C5D883D650EBC903CD089E8B7ED1D0AB382
JP2000299479A_wTransl.pdf	72381992969D18D59BE7FD29494755AE1FE9D047A57224A12C246719339F4DB184EEE976EC86003E57BA6B5FE10718372C76E14133889B83D83E7DC087D7B052
JP2002093742A_wTransl.pdf	060F914F495BFA1345DA4D6C4B65C4017212E6605F9076C819365DB82021C3C712EF360D1A9A6787D98851C4D311AB507C54320F02590CA910E37AC694247F6F
Appendix_C6.pdf	17318C81DD75A9F8B8947829D87F081347C44261AFA6B42F61EB9D1772A66C9C506323CBB61D84DD057170A305D6FAA208321FE17080980989AB40759E94DA20
Appendix_C10.pdf	8209A031F91B89A916D5BDDC7D91CBD6F086FD75FCD58D33EFDB2998D7C13C014E186481E816E6A6F3E29636D0C5F6E5EA7CA3C8B86503338FC2F951B8D79B78
Appendix_C8.pdf	FBCD4EABB2500739ACED3A8A57460480782 6EC34520E30B5D3CB32CC162EE1BCA63270248B6DF1C6130D1B78B9D0087A9245956311F353C09C5D0F478091320F

JPH0653165A_wTransl.pdf	B9916256A1AB4943CBFAA1DBDFD2C3D7899F01F4EEAADF2F05FF102D6EED871E08B9A3240CCDD2D793FAD9CC1911C20F66D9A2575862FF18A77EFC038B1F0041
JP2002075909A_wTransl.pdf	81747C5E1C33756FB2CF4C303BCBA0228FA768C8DE0BE39CA679543C77E3A53537099E40C4E2BAA2C318FAE22FD035F096E1402E856A9125B65B3E402C144171
JPH03191518A_wTransl.pdf	8E2B57B548C10DA1692D97BE590868B199737101FE844A6650EB35B4F78F6E7C28B585C7EACA92C68A5A239A0535C1E88010292BFC908903DAA5251224A3EB48
JPH04199628A_wTransl.pdf	F88F8609E3DF9B435AF2B9408E3DFA00B11121F2E5199A3F7DE08F186454D69242DA38A0EA8B6B2C2AB5C6D45F965D695CA2A526A34212B172B174F449E5B615
JPH03274735A_wTransl.pdf	347C249602D18795F2236E68AF1CB408425B017391A24F98BD95C7DAEBB32B48E52F20C96B88D05FF57743CF9B567BFFAE25421DD6A4E4046BC1F057A1E4F90D
Appendix_B10.pdf	02EF135E7FF4AD1023FBAD681901777B87CBABD67A35E6F88626B11E4CE458B6DB917EBC314A8B5DB3523AC80D374EA1DEBB043A0BD52E77D5D53A246901F8DB
JPH1126713A_wTransl.pdf	1624B665083CC76F840BC96B1A11FAED0FBB6AC2CCD074EFD36F49215139671B010EEB84B2CBB06EC2333623A8373F239E6413EB87605A92AA73D105D325498B
Appendix_B1.pdf	7E9F51B603F2ACDF3F6F06F35AF9291ABB9937F7E6C183441FFA8863E972C99307E710063D60C78422D7C085B4110C04029757D984BCE0CE05E8DC843DD3A7A2
Appendix_B2.pdf	3B2170CDFCE620CE221A62326AF86EA4FAFA850C037216E7A1854521F8D9CEF8144D37E0BD77121D8836FECDD731837B01FC5A1619EBB418A7F790A363FFB17C
Appendix_B5.pdf	74DF29B8439568F0A69C00F119286D22307BB2E6609DCF92DCE091BE95E3D1E70805645532F0C246E5E477B7E0052C47C23B7597692B9BDD6D09776240DDD572

Appendix_C2.pdf	20D5F72D01091D1D3CC86DA173CCC878E343ABB6F98647D16C922FAAFFC5E779EBF406E4EAFC018E5DD5F61E873A66F3423FC3792354606F5A9A452A073B0320
Appendix_D2.pdf	C7FD991805C29C0981D70AFFBE07E159A88832CE4870364A0FA73DBD3072DDA535BC95120E2998768DE94732B27A10AB7ABAD00DEEBDF6E60703688B874C0C9C
Appendix_D4.pdf	08631FCAEF87710EE61E622AC0A5A323FA0C5F488024CB8E562468554F1B3EF5A80218E73A08942DA2C2E3AF861CEA31DC80B4D778846D8E1564A80F19B081BF
DEFIVES.pdf	D3557CBDE243D1170E45CE798F05E63BAA3D89ADDD83E5FAE69708522BB73E3547BC173EC2105627D650FD3DC016072DE2D0FC5A5F2B41A038A62E72CE010BE5
DeBOSSCHER.pdf	5BB92C10C49B047A83149E5E48F4CA82574CBA65CA9BD83929E722C84D34A3AB6A3938FBE605527F8BEF81F96D5322F7390D3DE48F291D179EF858A162E11A7D
GOODNICK.pdf	95CFDA3978E867668D9DC752175EC3FE17D61E6CE4E48D3CD9B7B443FAEAD76BB05E0CE3F426DA26A7D958C4BB3D0EB086C81C1F540628238E0D2254D25DA277
EP0168125A1.pdf	35FDF54CB2C35BFEBC1EF679868F623A8B5D1EDE51195E846E651A35F605C88E31A6849A44469D5D9565F467306E07105C8963F70D50CD7E53F5246861DF50D0
EP0068897A2.pdf	4B75FBE9742A483E90C25E65861124AF41AD9247AE04464C3478B8C1E3A0DEB47B3CF6139A88D4C64C57BC3E9E40DA1BA93B04C72902A5811309A66C061BBA1C
GB1222594A.pdf	AD5DE71C335DD6FDAA94C2AA647274525BD85D0EF193EF290163B64665B0826D94022A7E678A24F9CF6D3CCD8AE17DFC7FD76F00E649A6DDE561CD584BF82F32
JP2002217425A_wTransl.pdf	468C57BB8F07649A098BC3A73A22AE2DAB2D6B8BAD84899C371B7B98453A85400AA32F27BFECFC9432DD02FC95382A63BB3963BA4B7D175F86313BAC664C9757

JP2002151428A_wTransl.pdf	7C9F0602C96B5369D77E138439BB9367A36B3B2B5A213532BC9112ABD23DF48906673BE06FA957C1C3BD6C89E17940002AFCB1194FE93842DFA92C81E831626B
JPH0661177A_wTransl.pdf	574DAA053950E0F3D40C7B92C82AD749CC7B0F96DBE432D154414340092 7FAE473CA29CD0F3AA549B7DA46B4FE415267459188C629E90B51C92328F046D00100
JPH04284668A_wTransl.pdf	A9DBDEEEFA81E711C05EFBFABD69892708DF700D6C86D209BBC7278092E7D06DB2703ED3F8D912A2AAD24A7E536BD7840079EA36EDE71625C3EA1FE95B6BB9C8
JPH1074707A_wTransl.pdf	050A8E24551A36D8683F6E724D6F5F149818601E85DD6700861F9DA9B5F11ECE419596ADA3263D27C59639D9D023E150CA3F97EABF57C908AB49804B596496D6
3771-0003-DC13_SB-08A_Other.pdf	D7D3AA7993AD5063A43E8AA41412399BCB4D34FB7924F3AADB9B751B561BF9BD2002C1339304498BED22E1F33A583458FC6E2046DFD39171922C51FE33DA8CCB
Appendix_A2.pdf	55389990521FB6A02C21453875FA2FD3F3C8256285B403DECBE264D3BF96240DEFA522C14D16A4F4BE5576979535F06A461AA0134B5B2A01E552603C974292EC
Appendix_A8.pdf	81D6BFC81C64F027F7AFECC3E4B25D50587F551FB705C64A5EE2C73E5AC5ABF4E13B173D4452543785159DC93CAAA4FF1053898AB33EAB6543C7A68227AC2663
Appendix_A7.pdf	4722C3D4637976B89DE0FCEC34F200931E5ECEB08E841A1A19E26FFEF1B32E2C5449906EE2D2A08BD9F6B7715A9ACB879C552BD812ACDB783EEFE21C8AFB4E32
Appendix_E2.pdf	F26A5C3678DE6F2BA4039FC635EEFDD7F2CE6D008429BB8B47DA742B06A38A170127CF3D6C9C80C9C2388E969DB40BE151C89C2564FF9DDE63F5D475E92B6A97
Appendix_E3.pdf	B643B8682DC6510B3FC75B3D450D3B3717F5DA89D4F0DF8986F6C1ED97DC8508BC20B0D3C0ED97FF21E6DD6925E241814A8AD42A80ECA3893D1888DB443D0B3C

Appendix_E10.pdf	D3C2811FDF4618999F72988F11831D0097D7D45FEC2848FDA DEA887ACFA2B6695E8F4B4104C2B2A0FC5223B705F043C962 03DB683D6EC2B82193C93026447D30
Appendix_E8.pdf	BCAC8ACCF39EEBDDED6BAF74F5858EFCE56941F888E57D2 DBDC98BCC236B4664F783E023368EB0992265DC99C16858C9 6503216B62B72E7EC50039592558B337
Appendix_F6.pdf	D0E17FEE1A2AB8F3A95139E77D49187E074BA3350D875F052 BAB4E5B2593339D6B7B4790C78CEA6C404641E44479A5AEC9 925D9846A90AD04A7A1F93782B3F8D
JP2000228523A_wTransl.pdf	36B4E11D8142BD3E76F07B6B50E580ADD63A36F457F2DE6CD 1136CB260E60E1D40F0816D7F1A7771B15D3A297BFF843DF71 016183275FB963EFB4C2D81A3F820
Appendix_A10.pdf	5406663172948375CB0CDE0BEF2FBEA4E27DCFCE9ABEB063 C1A92EF937511667D658A0794897B7DC86221EBC4887DF5D2 32708553E23C2B9CCB756E29D5A2FE7
Appendix_A4.pdf	B826949CA2BA8611442B2D88FA4F54DD063E86A0599A4FA43 8E2139B1250BC83F9FEED5FFAEFBA1015AACBB3CDFB3F6F2 11D1148E90C567483EA81C81000CD93
Appendix_A3.pdf	AB3731C328980865D66A5D457CE730D301D381E019F8D1BF7 3D146328D4CD4808077014260F5521488AE22F334E01BB93248 6A3BDD76EBF93C6693B38AEC9795
Appendix_B3.pdf	CF780A73E811AB8FF29D7C232F46593CA4CE1EBFE547FD1F DD32F9B6DB655C911EE3297722568D4FA095E6DDAF8CA60F C36A3C1B316A097D53EA77AB592134C7
Appendix_D6.pdf	51B9DFBD26591131DF6AAA12CBF5A893A0636E1908E873AFB 3DE8587D4EF71C77699F38CB666A5D61AF9C3EC22A58FC32E FFBE895DC45C74BAF1311E7D0E6C7C
Appendix_F1.pdf	51538768FB7D86764D13FC98D4911D89F3972929A2C168188F 58DEC1D519A49492B10D72EC741121B634C1D20FD98C8631B 2FFCD99098301601A2B5C6C74283F

JP2000101064A_wTransl.pdf	5814F1E13817D629755A0FC001E22BECB2754C339AC3B40EC227AA589DEF77406489B29D6A8860468E2442CB1CFFA4365CFF3110B08CB113DB808AED217E9A7D
JP2000195954A_wTransl.pdf	000AADEB0D08F940C976F60F5009E40E398A0E6CBD2A6A277E8DAADC3527E5D092E0245755455D0ED5C8CD81B1AE3BEF53FA533E62C423DC3846956DC8647906
JP2000216241A_wTransl.pdf	2C7A92FAEB665C58F0AF5BEB1146AA6385287262AC5CFEEDAEDB693B4E48AAE3564953DA1FC92E3BCD6B498DEC79FD3BD62D5BD1A666FD1519A40CD853FE0D09
Appendix_B6.pdf	FBC2CF7BD782EDDBCEF9375667E2C50075D6436E79116A58F237774C9C4D50EB1E03435CB48C9240D4B7053160F7276CC5AA6ADF90FF4842A35DFD4E7C876804
Samsung_Contentions.pdf	280D8865ED80244D8FAA4A3C40ABAB1DE90C8FF9E99279DFF6FDC1D27782308497B0C316189A0E42C43994DBD594EC9A3019E85B2C53B97EE9241298F27FEA17
Appendix_C5.pdf	8C70809BA9C3939CEF1596AE914733A805DD83EB61BCEDF7B38651EE1358342D32DF4CDF4C3AB4680E226FD9718F22F0F61E955EDABA9928FE5364626B0A8E69
Appendix_C3.pdf	B94C2921109B08C5BD0C5E2829C03C8B61ACDE10C2F44D8AB166658AAF7B72130F9882147EFE4CAF95A3901DEAA7693DAB4D95436A5C5156D489D43BB22A1D75
Appendix_C4.pdf	2B635B260F079DA7B48B4611759AA9D9BE5AADE07E6A643D403A51F9FBD62653FCB6DEDE9D192697A8B749462611FFC27DEAC250D6246B97794070E2C5B63DCA
Appendix_C7.pdf	CBD4AB341322800584E30856FE4203FCF750CDC248B25EE5E44E0A3682947FFAFD36EF3BEE96E2DC5FA4CEC56FF758B8E1F62E37370C39F3E63331D7048CE78E
Appendix_D1.pdf	735F18418DD6A880395E92833E38828C856845E1DF5760EEBB67D67E568010528D4A56925162A096BFFA1441036BB91C824EDAE559EA4CC9A7B683E9873DF828

Appendix_D5.pdf	3F108F09472218D94DD82B90D96C84B8004F47F15AEFCEEC70E5E59A7A72E358A6B6D795FE115498BBAFD483A711B57534D49953790BCA22C1D9A617C036A22E
Appendix_D10.pdf	415F00BD8F4322CD67887B801345EFED7EB742B27CBB4CF78A57B4F8923981A55FAD494440195AF05744EB4C5A8F4398DFD8A50C95CDA43CC2F1564B8F4E15DC
Appendix_D3.pdf	FDB77945D9AAE34EDA54FD9B9421744304F138064A284A3EE932A972EFE77CA83E333E3CF87B29EAA05F053E8E5C4D23DD14EAD7F32A231345572635F4FB5CC9
JPH0226073A_wTransl.pdf	C6CBD40BEF5F2AC6186240AF63F3D14B201F0D5289A8727F083D11255EF5C054972B3B8B9521A26249FA8B4F6C0DEAB5DFC9BEAD0DE90BF59B82D5CE0C32E6AB
JPH0864800A_wTransl.pdf	1558C1CE9EA07E3ABF959A486EDFDADF2F8856AB74862D693944425E90751B85799ED726C87D68D44B9DE5B1C038D78CEFC5BBAAC18BB20271395E6EEB25448A
JPH01186672A_wTransl.pdf	A6057F031E7F7690572AA6A692AC47735F21BC9EDAC2C484B38C3ED182AC91974B271CFF39D14394798047A5DA6939C6FD6DAEBDFCBC8D10AC715AC48829CF64
Appendix_D7.pdf	2140C16F246B3A963EDF76CD98E639A9F876FC6C2D96CBDD8A885D5AD72E68F913397CCC220C79D1E900F99E88062CC462C0C486E9359AE8440B6F08645C302C
3771-0003-DC13_SB-08A_Contentions.pdf	3D4EF901A653CC9E1080A3CA949EFD663415C0C64F6444562896DD87FCA96C72A6BECF5B80E78749D34E6A6FA56642D9873831C8DFC7C36386004213C27DD03E
Appendix_A1.pdf	84ECC18E44F3EA57B71E7878CFD3519BAE217BB7E268B52DDC167EC9478365C388595E5BB8172A21CF97C6B0CBABA9F292F7D373C6B219541DB18F497FDFBA47
Appendix_A6.pdf	772F6F091072B76B13494ABAD1FCBAF83527DE12F42CCA3BDACA4B9DFB2C0EF4D5B7624BA886919016EEF5B4D3CF35F15D685A1A227554BEFBE88D221B468C93

Appendix_F5.pdf	8E27790A382021AF99A7E4ED3DF6182894B1FA70F3B3D293D ACD800D7E87AAB0E1730C0C6BA7024217FA2551A3917BE87A 4D17D151FB7EEB57285BD1D5BA7432
Appendix_F4.pdf	02DC99013BC6E4D9A8E6965EE58E57C9ACC3A15DFC7328CD 42AE6E8BB2F1670B6D83F723E02EF5426EC8B1D0754DE2C3D 79EF274AA370B3B9BF7876F29BDCCDA
Appendix_F8.pdf	DCDD515515B0EB1BBF53A05546420669 5F086B68521AE143A9 5F4C71178BCD0209F2D808A822CA21CE16E3582BE4708D41A B7E37C2E3B0601C5CD900FA267CA9
EP0042066A2.pdf	7090AA71AED3A4B676747E335FE1F256529A5D574E186EFAF4 3BDB59143C0A6865A3D9E140FB8CF9DABD590A201D8D67886 7AA2A2CE37E8CC706E3663B854EA4
JP2630279B2_wTransl.pdf	9A8A216A9A6AA9B95538A6F1C235513A2DB7E39C6C26EC1B2 D724DF0BA83BACD42048C85FC0B391D5EDFF0258FB8016E1 0F74EB5B2E8FBE64A54AF8F6E7B3AAE
Appendix_B8.pdf	7AE008BADF2E8EC3397530401A159F8D07FA14FB0126E69D5 847DDEF288F1A8FC95EF73068F8CCB302D9FAD5D3CBA4DC1 397C4DFB9E23F35A7D10697CD5E8FDC
Appendix_D8.pdf	48389A56BBBF66D176E98C00C97A6C08E2CC4481A585D17E3 935D63428A0D4C7299516B607934D3A651B35258903EA022650 4A947723C5EAA07231E1ACD4C421
Appendix_E1.pdf	40D99048DBDA1D1D19012A13BC7AA5B58053038FD22A4D08D 6AFB2D0CDB24F738BD7014585F2D877CF18D91C953B5FA62E 28F2CD53A131BCBB5FECCB4BE78604
Appendix_E5.pdf	178390FC56F912CE087DA41BA55D79C372A6F112C77A2F84C B5C866DA84367B61446777B635CAFD86C1B6AA9B31D1CE8F4 28711658C04E35369EF1B1251B1959
JPH1027847A_wTransl.pdf	8FC7B16A482CF332BA98201D62A4B45AEB9ED0B70C2FDF6C 0260DAEF12DCAA76C2B2E6317059E41AFD65594C5C58CA941 E5B76DBF144C63B71CCBAA3A9CAB17F

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/847,878	06/17/2020 05:33:21 PM ET	3771-0003-DC13

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8164	FILED BY	Sarah Zizzo
PATENT CENTER #	60039949	FILING DATE	04/14/2020
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

TOTAL DOCUMENTS: 7

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
ZAIMA_Applied_Sci.pdf	5	Non Patent Literature	677 KB
ZAIMA_JPN.pdf	8	Non Patent Literature	1132 KB
1-250_Pages_from_WESTE_Part_1of3.pdf	250	Non Patent Literature	18975 KB
ZAFAR.pdf	4	Non Patent Literature	1118 KB
ZAIMA.pdf	18	Non Patent Literature	14243 KB
251-	250	Non Patent Literature	21875 KB

500_Pages_from_WESTE_Part_2of3.pdf			
551- 749 Pages from WESTE Part 3 of 3.pdf	249	Non Patent Literature	19047 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
ZAIMA_Applied_Sci.pdf	3425D27A297013B81E667E6486F1BA5869A7EFEF435D3068F86F0FC6F923A0EE1AFE0D97806CD40989D907BEC0D69B39140D18A7754BCC3986EA7D168B8A305E
ZAIMA_JPN.pdf	3ED8F48056B37874658E40EABA63D434CA37ADB55FD2EADC510692E92CDF8351D64B3EE78CB04CA2AC39F0F529678ABF444E589801B47113A27DF25FC4029F1D
1-250_Pages_from_WESTE_Part_1of3.pdf	5E12905062A2D5553EDFD9D3853A0DBBE28CC422406C9A450C9AD72E6FDB7B042E460A179023D34D0A2F36A992D00F301972F7D2173F90AC58AD97DE2DF9720E
ZAFAR.pdf	2563F45C9824A1971FABFA05771696D86670C8BC805846100EF39A2B5ADC3ACD6C9024A3CDD3C4BDFA365C0183AE444615AB31B08C99826577DE459B80281BF4
ZAIMA.pdf	2A576E4D217C05F33B917EABA3E5CE2FC722D5BBAF13B320015DEADF130F0FBFFC84740EB2C3AED138F8EB0F9A9E82D0C04CD3A3DBE72D3574E0E6530D18ADD2
251-500_Pages_from_WESTE_Part_2of3.pdf	F73480A97EA5B1267894F212070AD6B60186136E699EE905D3FD59CEB75408B876CD76CAED66D7C37AA2CDDDE398E7E9776D4076DB906BA7BA18C8BA4EFFE457
551- 749 Pages from WESTE Part 3 of 3.pdf	B0B9DA68576CEFD1675D91754794OB981325877C71506DDD30D4FBCDD6603CD9377119C8D70865290072FB88EC534FF13507C5AD26BFC439224F69139907B85B

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⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭63－175471

⑤1Int.Cl.⁴　識別記号　庁内整理番号　⑬公開　昭和63年(1988)7月19日
H 01 L 29/46　B－7638－5F

審査請求　未請求　発明の数 1　（全5頁）

⑤4発明の名称　半導体装置

⑳特　願　昭62－6078
㉒出　願　昭62(1987)1月16日

⑦2発明者　牧本　俊樹　東京都武蔵野市緑町3丁目9番11号　日本電信電話株式会社基礎研究所内
⑦2発明者　堀越　佳治　東京都武蔵野市緑町3丁目9番11号　日本電信電話株式会社基礎研究所内
⑦2発明者　小林　直樹　東京都武蔵野市緑町3丁目9番11号　日本電信電話株式会社基礎研究所内
⑦1出願人　日本電信電話株式会社　東京都千代田区内幸町1丁目1番6号
⑦4代理人　弁理士　谷　義一

明　細　書

1．発明の名称

半導体装置

2．特許請求の範囲

1)　半導体層の表面近傍に該表面と平行に第1の不純物ドープ単原子層が形成されており、該第1の不純物ドープ単原子層により内部に該第1の層と平行に第2の不純物ドープ単原子層が形成されていることを特徴とする半導体装置。

2)　前記第1の不純物ドープ単原子層の前記表面からの距離が100Å以内であり、かつ前記第2の不純物ドープ単原子層の前記表面からの距離が500 Å以内であることを特徴とする特許請求の範囲第1項記載の半導体装置。

3)　前記第1の不純物層のドーピング量は、金属と前記半導体を接触させた際に形成されるショットキバリアの高さに相当する電圧よりも小さな電圧降下を引き起こす量であることを特徴とする特許請求の範囲第1項または第2項に記載の半導体装置。

4)　前記第1および第2の不純物層によって引き起こされる電圧降下の量が前記ショットキバリアの高さに相当する電圧より大きいことを特徴とする特許請求の範囲第1項記載の半導体装置。

（以　下　余　白）

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3.発明の詳細な説明

[産業上の利用分野]

本発明は半導体装置に関し、特に合金化プロセスを経ずに、半導体上へオーミック電極の形成を可能とする不純物ドーピング層を有する半導体装置に関するものである。

[従来の技術]

原子層ドーピングを用いて、トンネル電流を流すことにより、低抵抗のオーミックコンタクトを形成する方法として、金属と半導体の界面近傍の半導体中に一層の原子層ドーピングを行う方法がある。この方法におけるエネルギバンド図を第3図に示す。この方法においては以下に示すような2つの欠点がある。

① まず、原子層ドープ層とショットキバリアにより形成される三角ポテンシャル（第3図参照）を通過するトンネル電流を増やさねばならない。このためには原子層ドープ層中の不純物が高濃度であり、かつ活性化していなければならない。しかし、高濃度に原子層ドーピングを行うと、不純物準位が深くなり、不純物が十分活性化されず。ショットキバリアの高さに相当する電圧よりも大きな電圧降下は得ることができず、ノンアロイオーミックコンタクトの実現は困難であった。

② 次に、一層の原子層ドーピングによって、ショットキバリアの高さに相当する電圧よりも大きな電圧降下を引き起こすためには、ドーピング層をある程度、金属と半導体の界面から離さねばならない。(Appl. Phys. Lett. ; 49 (5),1986, 292)。しかし、この時には三角ポテンシャルは厚くなり電子のトンネル確率は低いものとなるため、ノンアロイオーミックコンタクトの実現は困難なものとなる。

金属と半導体との界面から距離dの位置に、シートキャリア濃度がNcの原子層ドーピングを行った場合の電圧降下ΔVは

$$\Delta V = q \times d \times Nc / \epsilon \qquad (1)$$

（qは電子電荷、εは誘電率）

で与えられる。

ここでは、GaAs中にSiを原子層ドープした例について述べる。

原子層ドープ層にSi不純物を面密度で5×10^{13}個/cm²だけ入れた場合には、そのうちの20%だけがドナとなり活性化することが報告されている（Jpn. J. Appl. Phys. ; 25, (1986),L748)。これはSi不純物の準位が深くなっているため、不純物が十分に活性化されていないためである。

第4図に従来の方法で作成した一層のドープ層を有する半導体装置の例を示す。この従来例はn-type GaAs 基板1上にノンドープGaAs層2を200[Å] 形成した後、Si不純物を面密度で5×10^{13}個／cm² 入れた単原子層ドーピング層3を形成した後、再びノンドープGaAs層2をd [Å] 形成し、裏面にAuGeNiオーミックコンタクト4を蒸着し、表面には、Au電極5を蒸着した構造となっている。

接触抵抗ρ_cは第4図に示すように、膜厚方向に電圧をかけ、電流を測定することによって測定するができる。dによる接触抵抗ρ_cの変化を第5図に示す。dの小さいときには、一層の原子層ドープ層による電圧降下がショットキバリアに相当する電圧よりも小さなためρ_cは高い。また、dを大きくすると、三角ポテンシャルが厚いためρ_cは高い。接触抵抗ρ_cが最小となるのは式(1) においてΔVがショットキバリアの高さに相当するd＝60 [Å] である。しかし、この場合にも、三角ポテンシャルが厚いために十分なトンネル電流が流れないため、ρ_cは高い。

[発明が解決しようとする問題点]

本発明は、上述した従来の欠点、すなわちドーピング層の活性化率が低下し、トンネル電流が少なかった点を解決し、良好なノンアロイオーミック電極層を有する半導体装置を提供することを目的とする。

[問題点を解決するための手段]

このような目的を達成するために、本発明の半導体装置は、半導体層の表面近傍に表面と平行に

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第１の不純物ドープ単原子層が形成されており、第１の不純物ドープ単原子層により内部に第１の層と平行に第２の不純物ドープ単原子層が形成されていることを特徴とする。

［作　用］

本発明においては単原子層ドープ層によって形成されるポテンシャルを薄くすることによって、十分なトンネル電流を流すために、単原子層ドープ層を金属と半導体界面に十分に近くして不純物原子の活性化率を極めて高くし、さらに次の単原子層ドーピング層と供にショットキバリアの高さに相当する電圧よりも大きな電圧降下を引き起こさせる。金属と半導体との界面に近い高濃度のドーピング層の不純物準位は深いのにもかかわらず、フェルミレベルよりも上にあるために、すべて活性化されることになる。

このために十分なトンネル電流を流すことができるので、ノンアロイオーミックコンタクトの実現が可能である。

［実施例］

以下に図面を参照して本発明の実施例を説明する。

第１図に本発明の実施例を示す。

第１の不純物ドープ層としてｄ＝10［Å］の位置に５×10^{13}個／cm^2 だけSiを単原子層ドープした第１の層3Aを形成し、さらにｄ＝ 60[Å］の位置に、第２の不純物ドープ層3Bとして活性化率が100 %である５×10^{12}個／cm^2 のSi単原子層ドーピングを行った構造を作製した。他の構造は第４図に示した従来例と同じである。

第１および第２の不純物ドープ層はそれぞれ複数の原子層からなると、原子層間での不純物の相互作用によって電子の放出が抑制される。従って両不純物ドープ層はそれぞれ単原子層であることが必要である。高濃度の不純物をドープした単原子層を形成するには、MOCVD 法を改良した流量変調MOCVD 法が有効である。

このとき、第１の不純物ドープ層の活性化率を従来例と同様に20%とすると、第１層による電圧降下は$\Delta V_1 = 0.14$[V] となり、第２の不純物ドープ層による電圧降下は、$\Delta V_2 = 0.42$[V] であるから、$\Delta V_1 + \Delta V_2 < \phi_B$ (0.9V)となり、低い接触抵抗ρ_cは得られない。しかし、実際に測定を行なうと$\rho_c = 1 \times 10^{-6}$[Ω・$cm^2$]程度の極めて低い接触抵抗が得られた。

第２図に本発明における２層の単原子層ドープを行った構造のエネルギーバンドを示す。

本発明においてはフェルミレベルよりも上の不純物準位から電子が放出されることにより、第１層の活性化率が実質上高くなったために低い接触抵抗が得られる。このように第１層の位置における伝導帯とフェルミレベルとの差を比較的大きくとることにより、不純物の活性化率を上げることができる。第２図と第３図とを比較すれば明らかなように金属と半導体との界面付近の電子に対するポテンシャルは、従来の三角ポテンシャルに比べ薄くなり、十分なトンネル電流を流すことができるために、ノンアロイオーミックコンタクトの実現が可能である。

さらに、第１層および第２層のドーピング量をそれぞれ５×10^{13}個／cm^2 ，５×10^{12}個／cm^2 とし、第１層および第２層の半導体表面からの位置を変え、抵抗率の変化を調べた。その結果を第１表に示す。第１層の位置が界面から 100Åをこえて離れている場合および第２層の位置が 500Åをこえて離れている場合には10^{-6}Ω・cm^2 台の低い抵抗率を得ることはできなかった。従って10^{-6}Ω・cm^2 台の低い抵抗率を得るためには、第１層および第２層の位置は、半導体の表面から、それぞれ100 Å，500 Å以内が望ましい。

表　1

第１層の位置［Å］	第２層の位置［Å］	抵抗率［Ω・cm^2］
１０	１００	２×10^{-6}
１０	２００	４×10^{-6}
１０	５００	６×10^{-6}
５０	１５０	３×10^{-6}
１００	１５０	５×10^{-6}

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［効　果］

以上説明したように、本発明によれば金属と半導体との界面付近に存在する単原子層ドーピング層内の不純物原子のエネルギ準位が、フェルミレベルよりも上であり、高濃度にドーピングを行なっても不純物原子は十分活性化できる。このため、界面付近に存在するポテンシャルは、非常に薄くなり、十分なトンネル電流を流すことができるため、ノンアロイオーミックコンタクトの実現が可能となった。

4．図面の簡単な説明

第1図は本発明の実施例を示す断面図、

第2図は本発明におけるエネルギーバンド図、

第3図は従来の単一のドープ層を有する半導体装置におけるエネルギーバンド図、

第4図は従来の半導体装置の一例の断面図、

第5図は従来の装置における接触抵抗を示す図である。

1…n－GaAs基板、

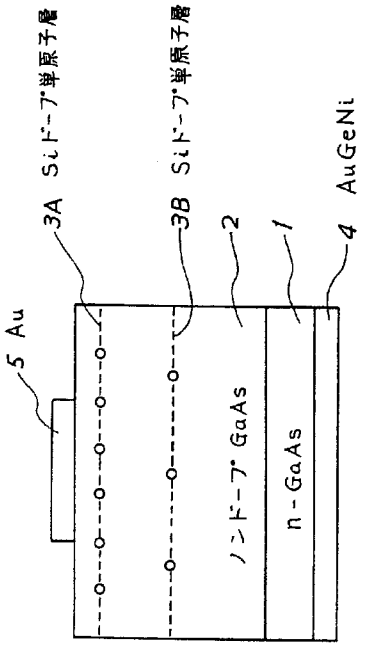
2…ノンドープGaAs層、

3A…第1の不純物ドープ単原子層、

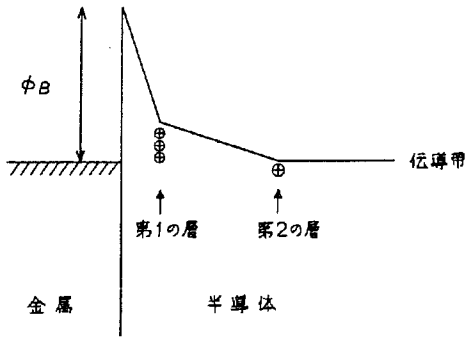
3B…第2の不純物ドープ単原子層。

特許出願人　　日本電信電話株式会社

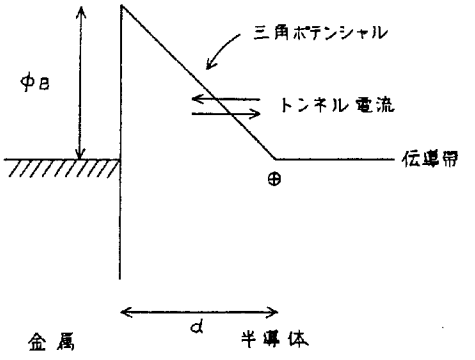
代　理　人　　弁理士　谷　　義　一



第1図

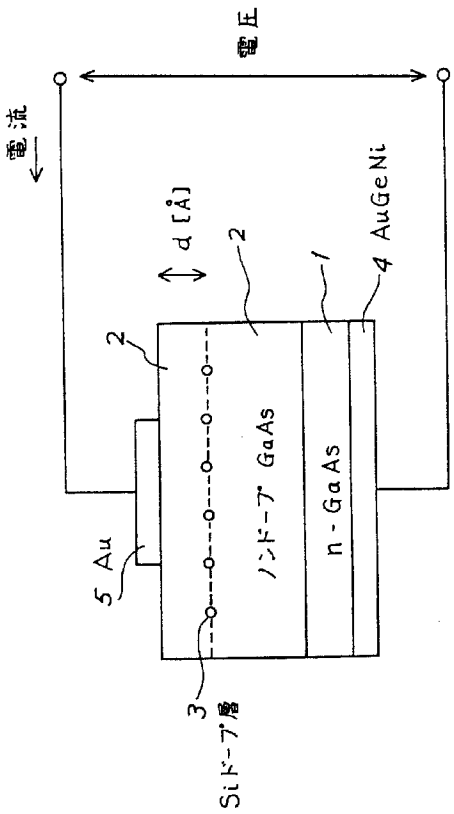


第2図

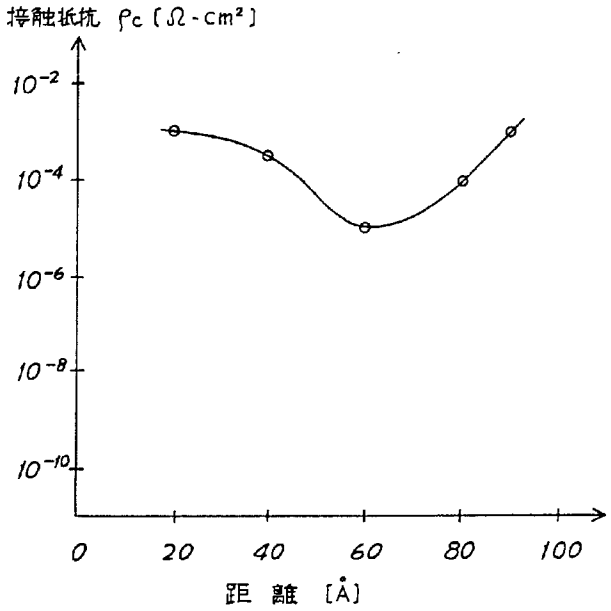


第3図

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第 4 図



第 5 図

GF Exhibit 1126 - 1315/2248

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JPS63175471A SEMICONDUCTOR DEVICE

Applicants: NIPPON TELEGRAPH & TELEPHONE

Inventors: HORIKOSHI YOSHIHARU,KOBAYASHI NAOKI,MAKIMOTO TOSHIKI

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SEMICONDUCTOR DEVICE

Abstract

PURPOSE:To make non-alloy ohmic contact by supplying sufficient tunnel current by a method wherein a single atomic doped layer is formed close to an interface between a metal and a semiconductor to augment the rate of activation of impurity atom. CONSTITUTION:The first impurity doped single atomic layer 3A is formed on the part near the surface of a semiconductor layer 2 while the second impurity doped single atomic layer 3B is formed in parallel with and inside the first impurity doped layer 3A. Resultantly, the energy level of impurity atom in a single atomic doped layer existing in the part near an interface between a metal and a semiconductor exceeds the Fermi level so that the impurity atom may be sufficiently activated even in high concentration doping process to lower the potential existing close to the interface for supplying a sufficient tunnel current. Through these procedures, non-alloy ohmic contact can be made.

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DESCRIPTION JPS63175471

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device, and more particularly to a semiconductor device having an impurity doping layer which enables formation of an ohmic electrode on a semiconductor without undergoing an alloying process. [Prior Art] As a method of forming a low-resistance ohmic contact by passing a tunnel current using atomic layer doping, there is a method of performing one atomic layer doping in a semiconductor in the vicinity of an interface between a metal and a semiconductor. . The energy band diagram in this method is shown in FIG. This method has the following two drawbacks. ■ First, the tunnel current that passes through the triangular potential (see Fig. 3) formed by the atomic layer dope layer and the Schottky barrier must be increased. For this purpose, the impurities in the atomic layer dope layer must be highly concentrated and activated. However, when the atomic layer doping is performed at a high concentration, the impurity level becomes deep and the impurities are not sufficiently activated. A voltage drop larger than the voltage corresponding to the height of the Schottky barrier could not be obtained, and it was difficult to realize a non-alloy ohmic contact. ■ Next, in order for one atomic layer doping to cause a voltage drop greater than the voltage corresponding to the height of the Schottky barrier, the doping layer must be separated from the metal-semiconductor interface to some extent. (Appl, Phys, Lett ,; 49 (5), 1986.292), L, streak. At this time, the triangular potential becomes thick and the electron tunneling probability becomes low, so it is difficult to realize a non-alloy ohmink contact. Will be things. The voltage drop ΔV is $\Delta V = qxdxNc / 6$ (1) (q is the electronic charge, ε is the read The electric rate) is given. Here, an example will be described in which GaAs is atomically layered with St. It has been reported that when 5 X 10 "pieces / cm" of Si impurity is added to the atomic layer dope layer in an area density, only 20% of it becomes a donor and is activated (Jpn, J, Appl, Phys ,; 25 ° (1986), L748), because the level of the Si impurity is deep and the impurity is not sufficiently activated. FIG. 4 shows an example of a

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semiconductor device having a single doped layer formed by a conventional method. In this conventional example, after forming the undoped GaAs layer 2 for 200 [persons] on the n-type GaAs substrate 1, after forming the monoatomic layer doping layer 3 containing 5 × 10″ Si / impurity / cm 2 in area density , The non-doped GaAs layer 2 is formed again [person], the AuGeNi ohmic contact 4 is vapor-deposited on the back surface, and the Au electrode 5 is vapor-deposited on the front surface.

Contact resistance ρ . Can be measured by applying a voltage in the film thickness direction and measuring the current as shown in FIG. The change in contact resistance ρ C due to d is shown in FIG. When d is small, pc is high because the voltage drop due to one atomic layer doped layer is smaller than the voltage corresponding to the Schottky barrier. Further, when d is increased, the triangular potential is thicker, so that pc is higher. The minimum contact resistance pc is d = 60 [ON], which corresponds to the height of the Schottky barrier in the formula (1). However, in this case as well, since the triangular potential is thick and a sufficient tunnel current does not flow, ρ 0 is high. [Problems to be Solved by the Invention] The present invention solves the above-mentioned conventional drawbacks, that is, the activation rate of the doping layer is lowered and the tunnel current is small, and has a good non-alloy ohmic electrode layer. An object is to provide a semiconductor device. [Means for Solving the Problems] In order to achieve such an object, in the semiconductor device of the present invention, a first impurity-doped monoatomic layer is formed in the vicinity of the surface of the semiconductor layer in parallel with the surface. A second impurity-doped monoatomic layer is formed inside the first impurity-doped monoatomic layer in parallel with the first layer. [Operation] In the present invention, by thinning the potential formed by the monoatomic layer-doped layer, the monoatomic layer-doped layer is sufficiently close to the metal-semiconductor interface in order to pass a sufficient tunnel current. The activation rate of atoms is made extremely high, and further, together with the subsequent monoatomic layer doping layer, a voltage drop larger than the voltage corresponding to the height of the Schottky barrier is caused. Although the impurity level of the high-concentration doping layer close to the interface between the metal and the semiconductor is deep, it is above the Fermi level, so that the impurity levels are all activated. For this reason, a sufficient tunnel current can be passed, so that non-alloy ohmic contact can be realized. [Embodiment] The present invention will be described below in detail with reference to the drawings. 1C shows an embodiment of the present invention. As the first impurity-doped layer, the first layer 3A was formed at the position of d = 10 [persons] by 5 × 10″ pieces / crn2 of mono atomic layer doped with St, and roughly at the position of d = 60 CAl. As the impurity-doped layer 3B of No. 2, a structure having 5 × 10″ pieces / cI 112 of Si monoatomic layer doping having an activation rate of 100% was prepared. The other structure is the same as the conventional example shown in FIG.

When each of the first and second impurity-doped layers is composed of a plurality of atomic

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layers, the interaction of impurities between the atomic layers suppresses electron emission. Therefore, it is necessary that both the impurity-doped layers are monoatomic layers. The flow rate modulation MOGVD method, which is an improved MOCVD method, is effective for forming a monoatomic layer doped with a high concentration of impurities. At this time, assuming that the activation rate of the first impurity-doped layer is 20% as in the conventional example, the voltage drop due to the first layer is $\Delta V, = O, 14$ [V], and the voltage due to the second impurity-doped layer is Since the drop is $\Delta V2 = 0{,}42$ [V], $\Delta v, -1 - AV2 < \phi B$ (0,9V), and a low contact resistance ρ. Can't get However, when actually measured, $\rho . = A$ very low contact resistance of about IX 10-'[$\Omega \cdot$ cm2] was obtained. FIG. 2 shows an energy band of a structure in which two layers of monoatomic layers are doped in the present invention. In the present invention, electrons are emitted from the impurity levels above the Fermi level, so that the activation rate of the first layer is substantially higher (a low contact resistance is obtained). Thus, by making the difference between the conduction band and the Fermi level at the position of the first layer relatively large, the activation rate of impurities can be increased. As is apparent from a comparison between FIG. 2 and FIG. 3, the potential for electrons near the interface between the metal and the semiconductor is thinner than the conventional triangular potential, and a sufficient tunnel current can flow. It is possible to realize non-alloy ohmic contact. Rokukyu Mu Flute 1 Maki) γ has a 7th layer doping layer of 5 x 1G "pieces / cod", 5 x 10'2 pieces / cm 2, and semiconductors of the first and second layers The position from the surface was changed and the change in resistivity was examined. The results are shown in Table 1. When the position of the first layer is more than 100 people away from the interface and the position of the second layer is more than 500 people, it is possible to obtain a low resistivity of $10^{-6}\ \Omega \cdot$ cm 2. There wasn't. Therefore, in order to obtain a resistivity as low as $10^{-8}\ \Omega \cdot$ cm 2, it is desirable that the positions of the first layer and the second layer are within 100 and 500 persons from the surface of the semiconductor, respectively. Table 1 [Effect] As described above, according to the present invention, the energy level of the impurity atom in the monoatomic layer doping layer existing near the interface between the metal and the semiconductor is higher than the Fermi level, Impurity atoms can be sufficiently activated even if doping is performed at a high concentration.

For this reason, the potential existing near the interface becomes extremely thin, and a sufficient tunnel current can flow, so that non-alloy ohmic contact can be realized.

[0002]
Brief description of the drawings

[0003]

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FIG. 1 is a sectional view showing an embodiment of the present invention, FIG. 2 is an energy band diagram in the present invention, FIG. 3 is an energy band diagram in a conventional semiconductor device having a single doped layer, and FIG. FIG. 5 is a sectional view of an example of the semiconductor device of FIG. 5, and FIG. 5 is a view showing the contact resistance in the conventional device.

1 --- n-GaAs substrate, 2 ... non-doped GaAs layer, 3A ... first impurity-doped monoatomic layer, 3B ... second impurity-doped monoatomic layer.

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CLAIMS JPS63175471

1.
A first impurity-doped monoatomic layer is formed in the vicinity of the surface in parallel with the surface, and a second impurity-doped monoatomic layer is provided inside the first impurity-doped monoatomic layer in parallel with the first layer by the first impurity-doped monoatomic layer. A semiconductor device in which a layer is formed. 2) The distance from the surface of the first impurity-doped monoatomic layer is within 100 Å, and the distance of the second impurity-doped monoatomic layer from the surface is within 500 Å The semiconductor device according to claim 1. 3) The doping amount of the first impurity layer is an amount that causes a voltage drop smaller than a voltage corresponding to the height of the Schottky barrier formed when the metal and the semiconductor are brought into contact with each other. The semiconductor device according to claim 1 or 2. 4) The semiconductor device according to claim 1, wherein the amount of voltage drop caused by the first and second impurity layers is larger than the voltage corresponding to the height of the Schottky barrier.

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(72) 발명자
황성보
서울특별시 영등포구 신길동 4656 우성아파트 303-701, 대한민국

(73) 특허권자
김영환
현대전자산업주식회사
경기도 이천시 부발읍 아미리 산 136-1, 대한민국

(74) 대리인
이정훈
이권희

(77) 심사관
권인회

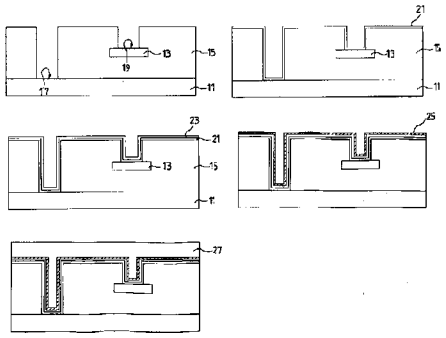
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(54) 반도체 소자의 콘택 형성방법

(57) 요 약

본 발명은 반도체소자의 콘택형성방법에 관한 것으로, 반도체기판 상부에 전도체가 형성된 절연층을 형성하고 상기 반도체기판과 전도체를 노출시키는 콘택홀을 형성한 다음, 전체표면상부에 티타늄막, 티타늄질화막, 티타늄산화막 적층구조나 티타늄막, 티타늄산화막, 티타늄질화막 적층구조 또는 이들 중 티타늄막이나 티타늄질화막이 제거된 적층구조를 갖는 콘택접합층을 형성하고 텅스텐으로 콘택플러그를 형성함으로써 티타늄막의 침식이나 절연체 형성을 억제하여 소자의 동작특성을 향상시켜 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 기술이다.

대 표 도 - 도 1



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청구의 범위

청구항 1

반도체기판 상부에 전도체가 구비된 절연층을 형성하는 공정과, 상기 반도체기판과 전도체를 노출시키는 제1, 2콘택홀을 각각 형성하는 공정과, 전체표면상부에 티타늄막과 티타늄질화막을 각각 일정두께 형성하는 공정과, 전체표면상부에 티타늄산화막을 일정두께 형성하여 티타늄막, 티타늄질화막, 티타늄산화막 적층구조의 콘택접합층을 형성하는 공정과, 전체표면상부에 텅스텐막을 형성하는 공정을 포함하는 반도체소자의 콘택 형성방법.

청구항 2

제1항에 있어서, 상기 티타늄막은 PVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 3

제1항에 있어서, 상기 티타늄막은 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 4

제1항 내지 제3항중 어느 한 항에 있어서, 상기 티타늄막은 100내지 500Å 두께로 형성되는 것을 특징으로 하는 반도체 소자의 콘택 형성방법.

청구항 5

제1항에 있어서, 상기 티타늄질화막은 PVD또는 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 6

제5항에 있어서, 상기 티타늄질화막은 300내지 1000Å두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 7

제1항에 있어서, 상기 티타늄산화막은 티타늄 아이소-프로포옥사이드와 산소(O_2)를 반응물로 하여 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 8

제1항에 있어서, 상기 티타늄산화막은 150내지 250℃의 온도, 0.5내지 2torr의 압력에서 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 9

제1항에 있어서, 상기 티타늄산화막은 10내지 30Å 두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 10

제1항에 있어서, 상기 콘택접합층은 티타늄막, 티타늄산화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 11

제1항에 있어서, 상기 콘택접합층은 티타늄질화막, 티타늄산화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 12

제1항에 있어서, 상기 콘택접합층은 티타늄막, 티타늄산화막, 티타늄질화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

청구항 13

제1항, 제10항 내지 제12항 중 어느 한 항에 있어서, 상기 콘택접합층은 하나의 챔버내에서 연속적으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

명세서

[발명의 명칭]

반도체 소자의 콘택 형성방법

[도면의 간단한 설명]

제1a도 내지 제1e도는 본 발명의 제1실시예에 따른 반도체소자의 콘택 형성 공정을 도시한 단면도.

제2a도 내지 제2c도는 본 발명의 제2실시예에 따른 반도체소자의 콘택 형성 공정을 도시한 단면도.

* 도면의 주요부분에 대한 부호의 설명

11, 31 : 반도체 기판　　13, 33 : 전도체

15, 35 : 절연층　　17, 37 : 제1콘택홀

19, 39 : 제2콘택홀　　21 : 티타늄막

23, 45 : 티타늄 질화막　　25, 43 : 티타늄 산화막

27, 47 : 텅스텐막

[발명의 상세한 설명]

본 발명은 반도체소자의 콘택 형성방법에 관한 것으로, 특히 화학기상 증착법에 의한 텅스텐 증착시 티타늄질화막(TiN)/티타늄의 접합층 위에 또는 티타늄질화막(TiN)과 티타늄(Ti)사이에 TiO_2(티타늄 산화물)박막을 형성 또는 증착하여 CVD(화학기상증착법) 텅스텐의 반응물인 텅스텐 헥사플루오라이드(WF_6)의 티타늄(Ti)침식에 의한 절연체 티타늄플루오라이트(TiF_3)형성을 억제시켜 신뢰성 있는 콘택을 형성하는 기술에 관한 것이다.

일반적으로, CVD텅스텐막의 접합층으로 티타늄(Ti)위에 티타늄질화막(TiN)를 적층한 구조를 사용하는데, 이 접합층 형성방법으로 스퍼터링을 사용하는 경우 박막의 밀도를 높이고 박막표면에 '산소(O)'가 거의 없는 상태로 만들어도 CVD텅스텐의 반응물인 WF_6가 티타늄질화막을 통과하여 티타늄과 반응하여 티타늄플루오라이트를 형성시키면서 콘택의 신뢰성을 떨어뜨린다.

그로 인하여, 반도체소자의 특성 및 신뢰성을 저하시키고 그에 따른 반도체소자의 고집적화를 어렵게 하는 문제점이 있다.

따라서, 본 발명은 티타늄질화막/티타늄의 접합층 위에 또는 티타늄 질화막과 티타늄 사이에 티타늄 산화물(TiO_2)을 얇게 증착하거나 형성시켜 CVD텅스텐 반응물인 WF_6과 티타늄의 반응을 억제시켜서 절연체인 TiF_3형성을 억제하고 신뢰성 있는 콘택을 형성함으로써 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 반도체소자의 콘택 형성방법을 제공하는데 그 목적이 있다.

이상의 목적을 달성하기 위하여 본 발명에 따른 반도체소자의 콘택 형성방법의 특징은, 반도체기판 상부에 전도체가 구비된 절연층을 형성하는 공정과, 상기 반도체기판과 전도체를 노출시키는 제1,2콘택홀을 각각 형성하는 공정과, 전체표면상부에 티타늄막과 티타늄질화막을 각각 일정두께 형성하는 공정

과, 전체표면상부에 티타늄산화막을 일정두께 형성하여 티타늄막, 티타늄질화막, 티타늄산화막 적층구조의 콘택접합층을 형성하는 공정과, 전체표면상부에 텅스텐막을 형성하는 공정을 포함하는데 있다.

여기서, 상기 티타늄막은 물리증착방법(PVD : Physical Vapor Deposition, 이하에서 PVD라 함)방법으로 형성되는 것과, 상기 티타늄막은 화학기상증착(CVD : Chemical Vapor Deposition, 이하에서 CVD라 함)방법으로 형성되는 것과, 상기 티타늄막은 100내지 500Å 두께로 형성되는 것과, 상기 티타늄질화막은 PVD 또는 CVD방법으로 형성되는 것과, 상기 티타늄질화막은 300내지 1000Å 두께로 형성되는 것과, 상기 티타늄산화막은 티타늄 아이소-프로포옥사이드와 산소(O_2)를 반응물로 하여 형성되는 것과, 상기 티타늄산화막은 150내지 250℃의 온도, 0.5 내지 2torr의 압력에서 CVD방법으로 형성되는 것과, 상기 티타늄산화막은 10내지 30Å 두께로 형성되는 것과, 상기 콘택접합층은 티타늄막, 티타늄산화막 적층구조로 형성되는 것과, 상기콘택접합층은 티타늄질화막, 티타늄산화막 적층구조로 형성되는 것과, 상기콘택접합층은 티타늄막, 티타늄산화막, 티타늄질화막 적층구조로 형성되는 것과, 상기 콘택접합층은 하나의 챔버내에서 연속적으로 형성되는 것이다.

본 발명의 원리는, 결합 에너지(binding energy)로 설명할 수 있는데 두 원자의 분자구조를 기본으로 실온에서의 결합에너지가 Ti-Ti 경우 141.4±21 $KJmol^{-1}$, F-Ti 경우 569.±33 $KJmol^{-1}$, O-Ti 경우 672.4±9.2 $KJmol^{-1}$이므로, 이를 비교하면 Ti-Ti F-Ti O-Ti과 같아 Ti-Ti는 플루오라이트(Ti-F_3)를 형성할 수 있지만 O-Ti 구조는 쉽게 플루오라이트를 형성할 수 없어 O-Ti 구조를 갖는 티타늄산화막으로 Ti-F_3 형성을 억제하는 것이다.

이하, 첨부된 도면을 참고로 하여 본 발명을 상세히 설명하기로 한다.

제1a도 내지 제1e도는 본 발명의 제1실시예에 따른 반도체소자의 콘택 형성공정을 도시한 단면도이다.

제1a도를 참조하면, 반도체기판(11)상부에 전도체(13)가 형성된 절연층(15)을 형성한다. 그리고, 콘택마스크(도시안됨)를 이용한 식각공정으로 상기 반도체기판(11)과 전도체(13)를 노출시키는 제1콘택홀(17)과 제2콘택홀(19)을 각각 형성한다.

제1b도를 참조하면, 전체표면상부에 PVD또는 CVD방법으로 티타늄막(21)을 100내지 500Å두께 형성한다.

제1c도를 참조하면, 전체표면상부에 PVD또는 CVD방법으로 티타늄질화막(23)을 300내지 1000Å 두께 형성한다.

제1d도를 참조하면, 전체표면상부에 티타늄(IV) 아이소-프로포옥사이드{Ti[OCH(CH_3)$_2$]$_4$}와 산소(O_2)를 반응물로 150내지 250℃온도, 0.5내지 2torr 압력의 증착조건에서 CVD방법에 의한 티바늄산화막(25)을 10내지 30Å두께 형성한다.

제1e도를 참조하면, 전체표면상부에 WF_6와 H_2를 반응물로 하여 300내지 500℃온도, 10내지 100torr압력의 증착조건에서 텅스텐막(27)을 형성함으로써 콘택을 형성한다.

제2a도 내지 제2c도는 본 발명의 제2실시예에 따른 반도체소자의 콘택형성공정을 도시한 단면도이다.

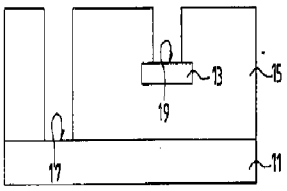
제2a도를 참조하면, 반도체기판(11)상부에 전도체(13)가 형성된 절연층(15)을 형성한다. 그리고, 콘택마스크(도시안됨)를 이용한 식각공정으로 상기 반도체기판(11)과 전도체(13)를 노출시키는 제1콘택홀(17)과 제2콘택홀(19)을 각각 형성한다. 그리고, 전체표면상부에 PVD또는 CVD방법으로 티타늄막(21)을 100내지 500Å두께 형성한다. 그리고, 전체표면상부에 티타늄(IV) 아이소-프로옥사이드

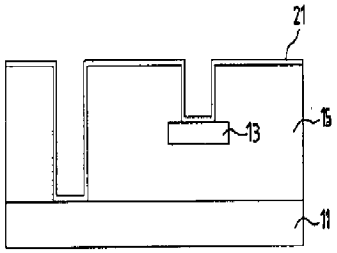
{Ti[OCH(CH3)2]4}와 산소를 반응물로 150내지 250℃온도, 0.5내지 2torr압력의 증착조건에서 CVD방법에 따라 티바늄산화막(43)을 10내지 30Å두께 형성한다.

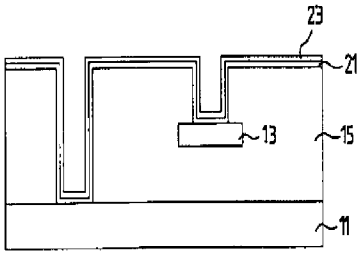
제2b도를 참조하면, 전체표면상부에 PVD 또는 CVD방법으로 티타늄질화막(45)을 300~1000Å 두께 형성한다.

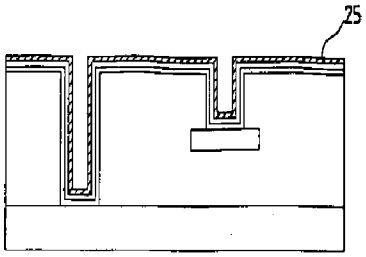
제2c도를 참조하면, 전체표면상부에 WF_6와 H_2를 반응물로 하여 300내지 500℃온도, 10내지 100torr압력의 증착조건에서 텅스텐막(47)을 형성함으로써 콘택을 형성한다.

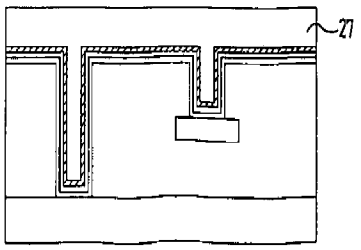
이상에서 설명한 바와 같이 본발명에 따른 반도체소자의 콘택 형성방법은, 콘택공정시 WF_6에 의한 티타늄막의 침식을 억제하고 절연체의 발생을 억제하여 콘택특성을 향상시킴으로써 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 잇점이 있다.

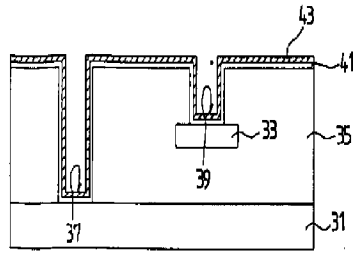

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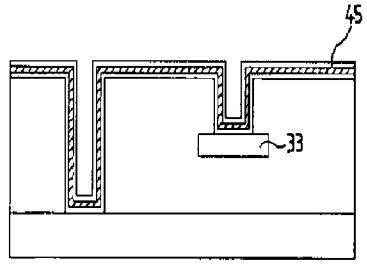

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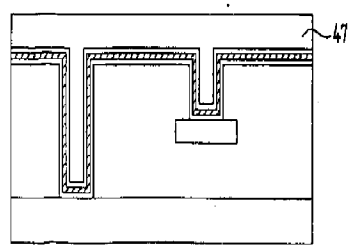

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Examined Patent Publication(B1)

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Agent.	LEE, Jung Hoon | HANYANG PATENT FIRM
Inventor	Hwang,Seong-Bo
Applicant	SK hynix Inc.
Rightholder	Hyundai Electronics industry CO., LTD

발명의 명칭

반도체 소자의 콘택 형성방법

Title of Invention

Manufacturing method of contact in semiconductor device

요약

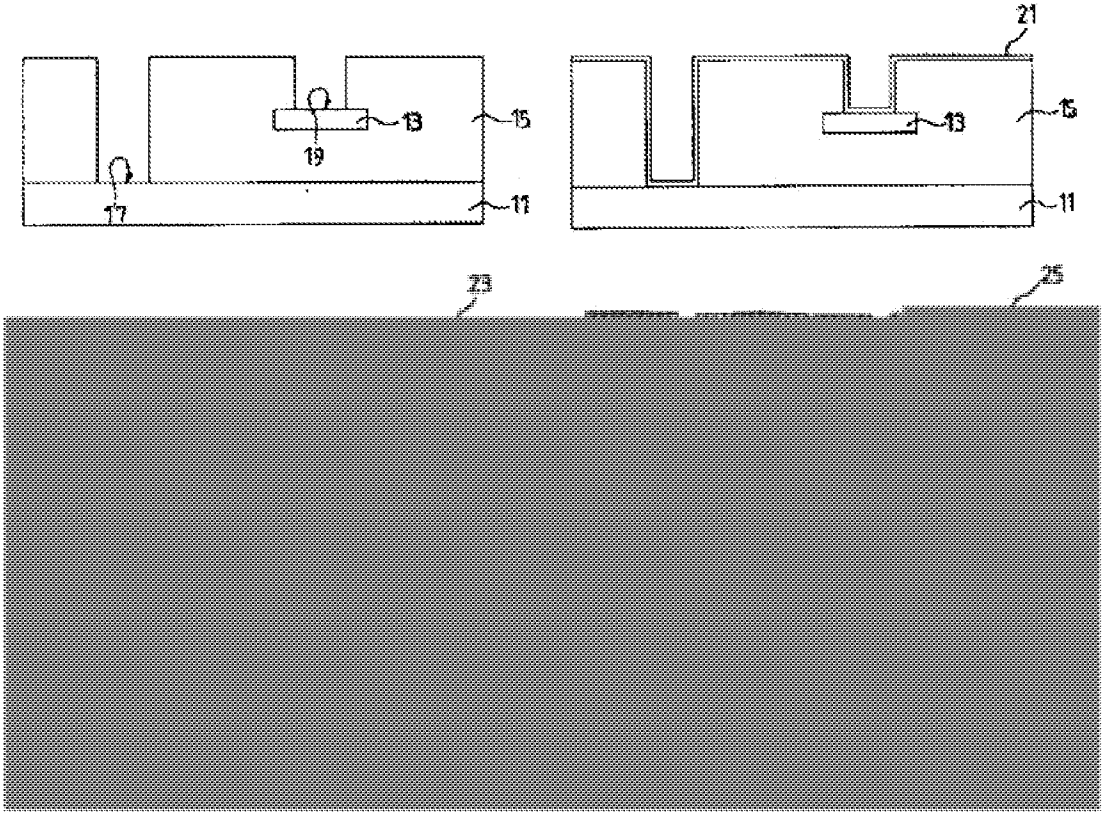
본 발명은 반도체소자의 콘택형성방법에 관한 것으로, 반도체 기판 상부에 전도체가 형성된 절연층을 형성하고 상기 반도체 기판과 전도체를 노출시키는 콘택홀을 형성한 다음, 전체표면 상부에 티타늄막, 티타늄질화막, 티타늄산화막 척층구조나 티타늄막, 티타늄산화막, 티타늄질화막 적층구조 또는 이들 중 티타늄막이나 티타늄질화막이 제거된 적층구조를 갖는 콘택접합층을 형성하고 텅스텐으로 콘택플러그를 형성함으로써 티타늄막의 침식이나 절연체 형성을 억제하여 소자의 동작특성을 향상시켜 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 기술이다.

Abstract

According to the invention, the insulating layer in which the conductive material is formed is formed in the semiconductor substrate upper as the contact forming method of a semiconductor device. And after the contact hole exposing the semiconductor substrate and conductive material is formed it is the technology suppressing the erosion or the insulator formation of the titanium film by forming the borderless junction layer having the titanium film, the TiN film, the titanium oxide film laminate structure or the titanium film, the titanium oxide film, and the structure of layer built titanium nitride or the laminating structure in which the titanium film or the TiN film is removed among these

at the upper part of the whole surface and formin g the contact plug into tungsten and improves the performance characteristic of the device and prop erty and reliability of the semiconductor device an d makes the high integration of the semiconducto r device according to the same possible.

대표도면(Representative drawing)



청구의 범위

청구 1항:

반도체기판 상부에 전도체가 구비된 절연층을 형성하는 공정과 , 상기 반도체기판과 전도체를 노출시키는 제1, 2콘택홀을 각 각 형성하는 공정과, 전체표면상부에 티타늄막과 티타늄질화막 을 각각 일정두께 형성하는 공정과, 전체표면상부에 티타늄산 화막을 일정두께 형성하여 티타늄막, 티타늄질화막, 티타늄산 화막 적층구조의 콘택접합층을 형성하는 공정과, 전체표면상부 에 텅스텐막을 형성하는 공정을 포함하는 반도체소자의 콘택 형성방법.

Scope of Claims

Claim 1:

The contact forming method of a semiconductor d evice which comprises the process of forming the insulating layer in which the conductive material i s equipped in the semiconductor substrate upper, the semiconductor substrate, and the process, of forming first and second contact hole exposing th e conductive material and the process, of respecti vely forming certain thickness the titanium film a nd TiN film at the upper part of the whole surface and the process, of forming the titanium film, the TiN film, and the borderless junction layer of the t itanium oxide film laminating structure the titaniu m oxide film is certain thickness formed at the up per part of the whole surface and the process of f orming the tungsten film at the upper part of the whole surface.

청구 2항:

제1항에 있어서, 상기 티타늄막은 PVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 2:

As for claim 1, the contact forming method of a semiconductor device in which the titanium film is formed with the PVD method.

청구 3항:

제1항에 있어서, 상기 티타늄막은 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 3:

As for claim 1, the contact forming method of a semiconductor device in which the titanium film is formed with the CVD method.

청구 4항:

제1항 내지 제3항중 어느 한 항에 있어서, 상기 티타늄막은 100내지 500Å 두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 4:

As for any one of claim 1 through 3, the contact forming method of a semiconductor device in which the titanium film is formed with 100 through 500Å thickness.

청구 5항:

제1항에 있어서, 상기 티타늄질화막은 PVD또는 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 5:

As for claim 1, the contact forming method of a semiconductor device in which the TiN film is formed with PVD or the CVD method.

청구 6항:

제5항에 있어서, 상기 티타늄질화막은 300내지 1000Å두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 6:

As for claim 5, the contact forming method of a semiconductor device in which the TiN film is formed with 300 through 1000Å thickness.

청구 7항:

제1항에 있어서, 상기 티타늄산화막은 티타늄 아이소-프로포옥사이드와 산소(O2)를 반응물로 하여 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 7:

As for claim 1, the contact forming method of a semiconductor device in which the titanium oxide film decides on the titanium iso - pro cannonade oxide and oxygen (O(SB)2(/SB)) to the reactant and which is formed.

청구 8항:

제1항에 있어서, 상기 티타늄산화막은 150내지 250℃의 온도, 0.5내지 2torr의 압력에서 CVD방법으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 8:

As for claim 1, the contact forming method of a semiconductor device in which the titanium oxide film is formed at the temperature of 150 through 250℃, and the pressure of 0.5 through 2torr into the CVD method.

청구 9항:

제1항에 있어서, 상기 티타늄산화막은 10내지 30Å 두께로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 9:

As for claim 1, the contact forming method of a semiconductor device in which the titanium oxide film is formed with 10 through 30Å thickness.

청구 10항:

제1항에 있어서, 상기 콘택접합층은 티타늄막, 티타늄산화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 10:

As for claim 1, the contact forming method of a semiconductor device in which the borderless junction layer is formed with the titanium film, and the titanium oxide film laminating structure.

청구 11항:

제1항에 있어서, 상기 콘택접합층은 티타늄질화막, 티타늄산화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 11:

As for claim 1, the contact forming method of a semiconductor device in which the borderless junction layer is formed with the TiN film, and the titanium oxide film laminating structure.

청구 12항:

제1항에 있어서, 상기 콘택접합층은 티타늄막, 티타늄산화막, 티타늄질화막 적층구조로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 12:

As for claim 1, the contact forming method of a semiconductor device in which the borderless junction layer is formed with the titanium film, the titanium oxide film, and the structure of layer built titanium nitride.

청구 13항:

제1항, 제10항 내지 제12항 중 어느 한 항에 있어서, 상기 콘택접합층은 하나의 챔버내에서 연속적으로 형성되는 것을 특징으로 하는 반도체소자의 콘택 형성방법.

Claim 13:

Claim 1, and the contact forming method of a semiconductor device in which as for any one of claim 10 through 12, the borderless junction layer is consecutively formed in one chamber.

상세설명

Detailed Description

[발명의 명칭]

반도체 소자의 콘택 형성방법

[Title of invention]

Contact forming method of a semiconductor device.

[도면의 간단한 설명]

제1a도 내지 제1e도는 본 발명의 제1실시예에 따른 반도체소자의 콘택 형성 공정을 도시한 단면도.

[Brief description of drawings]

To Figure 1a. And figure 1e is a cross-sectional view showing the contact forming process of the semiconductor device according to the first preferred embodiment of the invention.

제2a도 내지 제2c도는 본 발명의 제2실시예에 따른 반도체소자의 콘택 형성 공정을 도시한 단면도.

To Figure 2a. And figure 2c is a cross-sectional view showing the contact forming process of the semiconductor device according to the second preferred embodiment of the present invention.

* 도면의 주요부분에 대한 부호의 설명

* The description of reference numerals showing the main elements in drawings.

11, 31 : 반도체 기관 13, 33 : 전도체

11, 31: the semiconductor engine 13, 33: conductive material.

15, 35 : 절연층 17, 37 : 제1콘택홀

15, 35: insulating layer 17, 37: first contact hole.

19, 39 : 제2콘택홀 21 : 티타늄막

19, 39: second contact hole 21: titanium film.

23, 45 : 티타늄 질화막 25, 43 : 티타늄 산화막

23, 45: tiN film 25, 43: titanium oxide film.

27, 47 : 텅스텐막

27, 47: tungsten film.

[발명의 상세한 설명]

[Detailed description of the invention]

본 발명은 반도체소자의 콘택 형성방법에 관한 것으로, 특히 화학기상 증착법에 의한 텅스텐 증착시 티타늄질화막(TiN)/티타늄의 접합층 위에 또는 티타늄질화막(TiN)과 티타늄(Ti)사이

The invention relates to the contact forming method of a semiconductor device, and particularly, to the junction layer of the TiN film (TiN) / titanium i

에 TiO2(티타늄 산화물)박막을 형성 또는 증착하여 CVD(화학기상증착법) 텅스텐의 반응물인 텅스텐 헥사플루오라이드(WF6)의 티타늄(Ti)침식에 의한 절연체 티타늄플루오라이트(TiF3)형성을 억제시켜 신뢰성 있는 콘택을 형성하는 기술에 관한 것이다.

n the tungsten deposition by the chemistry gaseity deposition method, or, the TiN film (TiN) and the technology forming the TiO 2 (titanium oxide) thin film between the titanium (Ti) or deposits and suppresses the insulator titanium fluorite (TiF(SB)3(/SB)) formation by the titanium (Ti) erosion of the tungsten hexafluoride (WF(SB)6(/SB)) which is the reactant of the CVD (chemistry gaseity deposition method) tungsten and forms the contact having reliability.

일반적으로, CVD텅스텐막의 접합층으로 티타늄(Ti)위에 티타늄질화막(TiN)를 적층한 구조를 사용하는데, 이 접합층 형성 방법으로 스퍼터링을 사용하는 경우 박막의 밀도를 높이고 박막표면에 #39#산소(O)#39#가 거의 없는 상태로 만들어도 CVD텅스텐의 반응물인 WF6가 티타늄질화막을 통과하여 티타늄과 반응하여 티타늄플루오라이트를 형성시키면서 콘택의 신뢰성을 떨어뜨린다.

Generally, the structure of laminating the TiN film (TiN) in the junction layer of the CVD tungsten film on the titanium (Ti) is used. Even if while the density of the thin film is enhanced in case the use and the sputtering is made into the state where there is nearly no ' oxygen (O) ' with this manufacturing method of junction in the thin film surface the WF 6 which is the reactant of the CVD tungsten passes the TiN film and the thin film reacts to titanium and the titanium fluorite is formed the reliability of the contact is dropped down.

그로 인하여, 반도체소자의 특성 및 신뢰성을 저하시키고 그에 따른 반도체소자의 고집적화를 어렵게 하는 문제점이 있다.

There is a problem that property and reliability of the semiconductor device are lowered due to that and the high integration of the semiconductor device according to the same is made difficult.

따라서, 본 발명은 티타늄질화막/티타늄의 접합층 위에 또는 티타늄 질화막과 티타늄 사이에 티타늄 산화물(TiO2)을 얇게 증착하거나 형성시켜 CVD텅스텐 반응물인 WF6과 티타늄의 반응을 억제시켜서 절연체인 TiF3형성을 억제하고 신뢰성 있는 콘택을 형성함으로써 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 반도체소자의 콘택 형성방법을 제공하는데 그 목적이 있다.

Therefore, an object of the present invention are to provide the junction layer of the TiN film / titanium, or, the TiN film and the contact forming method of a semiconductor device which improves property and reliability of the semiconductor device by the thinly depositing the titanium oxide (TiO(SB)2(/SB)) between titanium or forming and suppressing the WF 6 which is the CVD tungsten reactant and the TiF 3 formation suppressing the reaction of titanium and is the insulator and forming the contact having reliability and makes the high integration of the semiconductor device according to the same possible.

이상의 목적을 달성하기 위하여 본 발명에 따른 반도체소자의 콘택 형성방법의 특징은, 반도체기판 상부에 전도체가 구비된 절연층을 형성하는 공정과, 상기 반도체기판과 전도체를 노출시키는 제1,2콘택홀을 각각 형성하는 공정과, 전체표면상부에 티타늄막과 티타늄질화막을 각각 일정두께 형성하는 공정과, 전체표면상부에 티타늄산화막을 일정두께 형성하여 티타늄막, 티타늄질화막, 티타늄산화막 적층구조의 콘택접합층을 형성하는 공정과, 전체표면상부에 텅스텐막을 형성하는 공정을 포함하는데 있다.

To achieve the above goals, the characteristic of the contact forming method of a semiconductor device according to the present invention comprises the process, of forming the insulating layer in which the conductive material is equipped in the semiconductor substrate upper and semiconductor substrate and the process, of forming first and second contact hole exposing the conductive material and the process, of respectively forming certain thickness the titanium film and TiN film at the upper part of the whole surface and the process, of forming the titanium film, the TiN film, and the borderless junction layer of the titanium oxide film laminating structure the titanium oxide film is certain thickness formed at the upper part of the whole surface and the process of forming the tungsten fi

lm at the upper part of the whole surface.

여기서, 상기 티타늄막은 물리증착방법(PVD : Physical Vapor Deposition, 이하에서 PVD라 함)방법으로 형성되는 것과, 상기 티타늄막은 화학기상증착(CVD : Chemical Vapor Deposition, 이하에서 CVD라 함)방법으로 형성되는 것과, 상기 티타늄막은 100내지 500Å 두께로 형성되는 것과, 상기 티타늄질화막은 PVD 또는 CVD방법으로 형성되는 것과, 상기 티타늄질화막은 300내지 1000Å 두께로 형성되는 것과, 상기 티타늄산화막은 티타늄 아이소-프로포옥사이드와 산소(O2)를 반응물로 하여 형성되는 것과, 상기 티타늄산화막은 150내지 250℃의 온도, 0.5 내지 2torr의 압력에서 CVD방법으로 형성되는 것과, 상기 티타늄산화막은 10내지 30Å 두께로 형성되는 것과, 상기 콘택접합층은 티타늄막, 티타늄산화막 적층구조로 형성되는 것과, 상기콘택접합층은 티타늄질화막, 티타늄산화막 적층구조로 형성되는 것과, 상기콘택접합층은 티타늄막, 티타늄산화막, 티타늄질화막 적층구조로 형성되는 것과, 상기 콘택접합층은 하나의 챔버내에서 연속적으로 형성되는 것이다.

Here, the borderless junction layer is consecutively formed in one chamber the titanium film is formed with the physical vapor deposition (hereinafter the PVD : Physical Vapor Deposition says to be PVD) method the reactant is formed.

본 발명의 원리는, 결합 에너지(binding energy)로 설명할 수 있는데 두 원자의 분자구조를 기본으로 실온에서의 결합에너지가 Ti-Ti 경우 141.4#177#21 KJmol-1, F-Ti 경우 569.#177#33 KJmol-1, O-Ti 경우 672.4#177#9.2 KJmol-1이므로, 이를 비교하면 Ti-Ti F-Ti O-Ti과 같아 Ti-Ti는 플루오라이트(Ti-F3)를 형성할 수 있지만 O-Ti 구조는 쉽게 플루오라이트를 형성할 수 없어 O-Ti 구조를 갖는 티타늄산화막으로 Ti-F3 형성을 억제하는 것이다.

The principles of the invention can illustrate as the binding energy but the binding energy at the room temperature is the molecular structure of two atoms the Ti-Ti case 141.4±21 KJmol - 1 , the F-Ti case 569.±33 KJmol - 1 , and the O-Ti case 672.4±9.2 KJmol - 1 to the basis. Therefore it suppresses the Ti- F 3 formation with the titanium oxide film is the same as that of the Ti-Ti F-Ti O-Ti and in which the Ti-Ti can form the fluorite (Ti-F(SB)3(/SB)) but if it compares this the O-Ti structure is easy it cannot form the fluorite and having the O-Ti structure.

이하, 첨부된 도면을 참고로 하여 본 발명을 상세히 설명하기로 한다.

The attached invention decides to be hereinafter particularly illustrated.

제1a도 내지 제1e도는 본 발명의 제1실시예에 따른 반도체소자의 콘택 형성공정을 도시한 단면도이다.

To Figure 1a. And figure 1e is a cross-sectional view showing the contact forming process of the semiconductor device according to the first preferred embodiment of the invention.

제1a도를 참조하면, 반도체기판(11)상부에 전도체(13)가 형성된 절연층(15)을 형성한다. 그리고, 콘택마스크(도시안됨)를 이용한 식각공정으로 상기 반도체기판(11)과 전도체(13)를 노출시키는 제1콘택홀(17)과 제2콘택홀(19)을 각각 형성한다.

Referring to figure 1a, the insulating layer (15) in which the conductive material (13) is formed at the upper part of the semiconductor substrate (11) is formed. And the first contact hole (17) and the second contact hole (19) exposing the semiconductor substrate (11) and conductive material (13) are formed into the etching process using the contact mask (is not shown).

제1b도를 참조하면, 전체표면상부에 PVD또는 CVD방법으로 티타늄막(21)을 100내지 500Å두께 형성한다.

Referring to figure 1b, the titanium film (21) is formed into PVD or the CVD method at the upper part of the whole surface with 100 through 500Å thickness.

제1c도를 참조하면, 전체표면상부에 PVD또는 CVD방법으로 티타늄질화막(23)을 300내지 1000Å두께 형성한다.

Referring to figure 1c, the TiN film (23) is formed into PVD or the CVD method at the upper part of the whole surface with 300 through 1000Å thickne

ss.

제1d도를 참조하면, 전체표면상부에 티타늄(IV) 아이소-프로포옥사이드{Ti[OCH(CH3)2]4}와 산소(O2)를 반응물로 150내지 250℃온도, 0.5내지 2torr 압력의 증착조건에서 CVD방법에 의한 티바늄산화막(25)을 10내지 30Å두께 형성한다.

Referring to figure 1d, in the reactant 150 through 250℃ temperature the titanium (IV) iso - pro cannonade oxide [Ti(OCH(CH(SB)3(/SB))(SB)2(/SB))(SB)4(/SB)] at the upper part of the whole surface and oxygen (O(SB)2(/SB)), and the deposition condition of 0.5 through 2torr pressure, *** oxide film (25) by the CVD method is formed with 10 through 30Å thickness.

제1e도를 참조하면, 전체표면상부에 WF6와 H2를 반응물로 하여 300내지 500℃온도, 10내지 100torr압력의 증착조건에서 텅스텐막(27)을 형성함으로써 콘택을 형성한다.

Referring to figure 1e, by having the WF 6 and H 2 as the reactant at the upper part of the whole surface and forming the tungsten film (27) at 300 through 500℃ temperature, and the deposition condition of 10 through 100torr pressure the contact is formed.

제2a도 내지 제2c도는 본 발명의 제2실시예에 따른 반도체소자의 콘택형성공정을 도시한 단면도이다.

To Figure 2a. And figure 2c is a cross-sectional view showing the contact of a semiconductor device formation process according to the second preferred embodiment of the present invention.

제2a도를 참조하면, 반도체기판(11)상부에 전도체(13)가 형성된 절연층(15)을 형성한다. 그리고, 콘택마스크(도시안됨)를 이용한 식각공정으로 상기 반도체기판(11)과 전도체(13)를 노출시키는 제1콘택홀(17)과 제2콘택홀(19)을 각각 형성한다. 그리고, 전체표면상부에 PVD또는 CVD방법으로 티타늄막(21)을 100내지 500Å두께 형성한다. 그리고, 전체표면상부에 티타늄(IV) 아이소-프로옥사이드{Ti[OCH(CH3)2]4}와 산소를 반응물로 150내지 250℃온도, 0.5내지 2torr압력의 증착조건에서 CVD방법에 따라 티바늄산화막(43)을 10내지 30Å두께 형성한다.

Referring to figure 2a, the insulating layer (15) in which the conductive material (13) is formed at the upper part of the semiconductor substrate (11) is formed. And the first contact hole (17) and the second contact hole (19) exposing the semiconductor substrate (11) and conductive material (13) are formed into the etching process using the contact mask (is not shown). And the titanium film (21) is formed into PVD or the CVD method at the upper part of the whole surface with 100 through 500Å thickness. And in the reactant 150 through 250℃ temperature the titanium (IV) iso - pro oxide [Ti(OCH(CH(SB)3(/SB))(SB)2(/SB))(SB)4(/SB)] at the upper part of the whole surface and oxygen, and the deposition condition of 0.5 through 2torr pressure, *** oxide film (43) is formed according to the CVD method with 10 through 30Å thickness.

제2b도를 참조하면, 전체표면상부에 PVD 또는 CVD방법으로 티타늄질화막(45)을 300~1000Å 두께 형성한다.

Referring to figure 2b, the TiN film (45) is formed into PVD or the CVD method at the upper part of the whole surface with 300~1000Å thickness.

제2c도를 참조하면, 전체표면상부에 WF6와 H2를 반응물로 하여 300내지 500℃온도, 10내지 100torr압력의 증착조건에서 텅스텐막(47)을 형성함으로써 콘택을 형성한다.

Referring to figure 2c, by having the WF 6 and H 2 as the reactant at the upper part of the whole surface and forming the tungsten film (47) at 300 through 500℃ temperature, and the deposition condition of 10 through 100torr pressure the contact is formed.

이상에서 설명한 바와 같이 본발명에 따른 반도체소자의 콘택형성방법은, 콘택공정시 WF6에 의한 티타늄막의 침식을 억제하고 절연체의 발생을 억제하여 콘택특성을 향상시킴으로써 반도체소자의 특성 및 신뢰성을 향상시키고 그에 따른 반도체소자의 고집적화를 가능하게 하는 잇점이 있다.

As illustrated in the above, the contact forming method of a semiconductor device according to the present invention has the advantage that property and reliability of the semiconductor device are improved by the erosion of the titanium film by the WF 6 being suppressed in the contact process a

nd the generation of the insulator being suppress ed and improving the contact quality and it makes the high integration of the semiconductor device according to the same possible.

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(73) 특허권자 현대전자산업주식회사
박종섭
경기 이천시 부발읍 아미리 산136-1

(72) 발명자 홍상기
경기도 성남시 분당구 구미동 엘지아파트 210동 1504호
김우현
서울특별시 용산구 용산동3가 1-70

(74) 대리인 신영무
최승민

심사관 : 김동원

(54) 반도체소자의확산방지막형성방법

요약

본 발명은 반도체 소자의 확산 방지막 형성 방법에 관한 것으로, 실리콘 기판 상부에 형성된 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하고, 상기 콘택홀을 포함한 전체 구조 상부에 스퍼터링 방법으로 제 1 티타늄 나이트라이드(TiN)층과 티타늄(Ti)층을 형성한 후 질소가 함유된 가스 분위기에서 급속 열질화 처리(RTN)를 실시함으로써 티타늄층은 미세 결정 구조의 제 2 티타늄 나이트라이드층으로 되고, 제 1 티타늄 나이트라이드층은 콘택홀 기저부에서 균일한 두께의 티타늄 실리사이드층으로 되며, 제 2 티타늄 나이트라이드층과 제 1 티타늄 나이트라이드층 및 티타늄 실리사이드층 사이에 티타늄 옥사이드(TiO)층이 형성되어 확산 방지 효과를 극대화시킨다.

대표도
도 3

색인어
층간 절연막, 콘택홀, 티타늄 옥사이드층, 티타늄 실리사이드층, 확산 방지막

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명세서

도면의 간단한 설명

도 1(a) 내지 1(c)는 종래의 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도.

도 2는 도 1(c)의 콘택홀 기저부를 확대한 도면.

도 3(a) 내지 3(c)는 본 발명에 따른 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도.

도 4는 도 3(c)의 콘택홀 기저부를 확대한 도면.

도 5(a) 및 도 5(b)는 종래의 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진.

도 6(a) 및 도 6(b)는 본 발명에 따른 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진.

< 도면의 주요 부분에 대한 부호 설명>

11 및 21 : 실리콘 기판12 및 22 : 층간 절연막

13 및 24 : 티타늄(Ti)층

14, 23 및 24A : 티타늄 나이트라이드(TiN)층

15 및 25 : 티타늄 실리사이드($TiSi_2$)층

26 : 티타늄 옥사이드(TiO)층17 및 27 : 텅스텐층

19 및 29 : 콘택홀

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 반도체 소자의 확산 방지막(metal barrier film) 형성 방법에 관한 것으로, 특히 콘택 저항을 감소시키며 확산 방지 효과를 증대시킬 수 있는 반도체 소자의 확산 방지막 형성 방법에 관한 것이다.

일반적으로, 반도체 소자가 고집적화 됨에 따라 콘택홀의 크기는 줄어들고 있다. 이에 따라 금속 콘택 공정시 콘택홀을 양호하게 매립하기 어렵고, 또한 콘택 저항이 증가되어 소자의 전기적 특성을 저하시키게 된다. 이를 해결하기 위하여, 티타늄(Ti)과 티타늄 나이트라이드(TiN)를 증착한 후 열처리하여 콘택홀 기저부에 티타늄 실리사이드($TiSi_2$)를 갖는 확산 방지막을 형성한다.

종래의 반도체 소자의 확산 방지막 형성 방법을 도 1(a) 내지 1(c)를 참조하여 설명하면 다음과 같다.

도 1(a)를 참조하면, 실리콘 기판(11) 상부에 형성된 층간 절연막(12)의 선택된 영역이 식각되어 실리콘 기판(11)의 소정 영역을 노출시키는 콘택홀(19)이 형성된다. 콘택홀(19)을 포함한 전체 구조 상부에 스퍼터링(sputtering) 방식으로 티타늄층(13) 및 티타늄 나이트라이드층(14)이 순차적으로 형성된다.

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도 1(b)를 참조하면, 질소(N_2) 또는 암모늄(NH_3) 가스 분위기에서 급속 열처리(Rapid Thermal Process; RTP) 공정을 실시하여 콘택홀(19) 기저부의 티타늄층(13)이 티타늄 실리사이드층(15)으로 변형되게 한다. 티타늄 실리사이드층(15)은 급속 열처리 공정 동안에 실리콘 기판(11)의 실리콘 원자(Si)와 티타늄층(13)의 티타늄 원자(Ti)가 상호 반응하여 형성된다.

이와 같이 티타늄층(13) 및 티타늄 나이트라이드층(14)을 순차적으로 형성한 후 급속 열처리 공정을 실시하여 확산 방지막이 형성되고, 이후 도 1(c)에 도시된 바와 같이, 텅스텐층(17)을 화학 기상 증착(Chemical Vapor Deposition ; CVD) 방식으로 형성한 후 패터닝하여 금속 배선이 형성된다.

도 1(c)의 콘택홀 기저부를 확대한 도 2에 도시된 바와 같이, 티타늄 나이트라이드층(14)은 원주형(columnar) 구조로 형성된다. 티타늄층(13)은 그 두께가 두꺼울 경우 급속 열처리에 의해 균일한 티타늄 실리사이드층을 형성할 수 있으나, 반도체 소자가 고집적화 되어감에 따라 콘택홀 크기가 줄어들어 종횡비(aspect ratio)가 크게되기 때문에 스퍼터링 방식으로 형성되는 티타늄층(13)의 층덮힘(step coverage)이 나쁘게 되므로 티타늄층(13)을 두껍게 형성하는데 한계가 있다. 티타늄층(13)을 두껍게 형성하기 위하여, 층덮힘이 우수한 CVD 방식을 적용하고 있으나, CVD 방식을 적용할 경우 박막에 불순물 함유량이 높아지는 등 많은 공정상의 문제점이 존재하므로 현재로서는 실질 공정에 적용하기 어려운 실정이다. 따라서, 텅스텐층(13)은 스퍼터링 방식으로 형성되며, 텅스텐층(13)의 두께가 임계 두께 이하일 경우 급속 열처리로 형성되는 티타늄 실리사이드층(15)은, 도 2에 도시된 바와 같이, 균일한 두께로 형성되지 못한다. 이와 같이 티타늄 나이트라이드층(14)이 원주형 구조를 갖고, 티타늄 실리사이드층(15)이 불균일하게 형성된 상태에서 WF_6가스를 이용하여 텅스텐층(17)을 형성할 경우, 형성 공정중에 원주형 구조의 티타늄 나이트라이드층(14)의 그레인 바운더리와 티타늄 실리사이드층(15)의 얇은 부분을 통해 텅스텐 원자(W)/플루오린 원자(F)와 실리콘 원자(Si)가 상호 확산되어 접합 파괴, 누설 전류 및 콘택 저항을 증가시켜 소자의 신뢰성을 저하시키는 문제점이 발생된다.

발명이 이루고자 하는 기술적 과제

따라서, 본 발명은 콘택 저항을 감소시키면서 확산 방지 효과를 증대시킬 수 있는 반도체 소자의 확산 방지막 및 그 형성 방법을 제공하는데 그 목적이 있다.

상술한 목적을 달성하기 위한 본 발명의 확산 방지막 형성 방법은 반도체 소자를 제조하기 위한 소정의 구조가 형성된 실리콘 기판 상부에 형성된 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하는 단계와, 상기 콘택홀을 포함한 전체 구조 상부에 제 1 티타늄 나이트라이드층 및 티타늄층을 순차적으로 형성하는 단계와, 질소가 함유된 가스 분위기에서 열처리 공정을 실시함으로써 상기 티타늄층은 제 2 티타늄 나이트라이드층이 되고, 상기 제 1 티타늄 나이트라이드층과 상기 제 2 티타늄 나이트라이드층 사이에는 티타늄 옥사이드층이 생성되며, 상기 콘택홀 기저부의 제 1 티타늄 나이트라이드층은 티타늄 실리사이드층으로 되는 단계를 포함하여 이루어진 것을 특징으로 한다.

발명의 구성 및 작용

첨부된 도면을 참조하여 본 발명을 상세히 설명하기로 한다.

도 3(a) 내지 3(c)는 본 발명에 따른 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도이고, 도 4는 도 3(c)의 콘택홀 기저부를 확대한 도면이다.

도 3(a)를 참조하면, 반도체 소자를 제조하기 위한 소정의 구조가 형성된 실리콘 기판(21) 상부에 형성된 층간 절연막(22)의 선택된 영역을 식각하여 실리콘 기판(21)의 소정 영역을 노출시키는 콘택홀(29)이 형성된다. 콘택홀(29)을 포함한 전체 구조 상부에 스퍼터링 방식으로 제 1 티타늄 나이트라이드층(23) 및 티타늄층(24)이 순차적으로 형성된다. 제 1 티타늄 나이트라이드층(23)은 약 50Å 의 두께로 형성되며, 티타늄층(24)은 약 400~600Å 의 두께로 형성된다.

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도 3(b)는 열처리 공정을 실시한 상태의 단면도로서, 열처리 공정은 저압용 반응로(low pressure furnace)에서 실시하거나 급속 열질화 처리(Rapid Thermal Nitridation; RTN)로 하며, 이때 분위기는 질소(N_2) 가스, 암모늄(NH_3) 가스 및 질소(N_2)와 암모늄(NH_3)의 혼합 가스 분위기중 어느 하나의 분위기로 한다. 열처리 결과, 티타늄층(24)은 제 2 티타늄 나이트라이드층(24A)으로 되고, 제 1 티타늄 나이트라이드층(23)과 제 2 티타늄 나이트라이드층(24A) 사이에는 티타늄 옥사이드층(TiO; 26)이 생성되며, 콘택홀(29) 기저부의 제 1 티타늄 나이트라이드층(23)은 티타늄 실리사이드층(25)으로 된다. 티타늄 실리사이드층(25)은 열처리 동안에 실리콘 기판(21)의 실리콘 원자(Si)와 제 1 티타늄 나이트라이드층(23)의 티타늄 원자(Ti)가 상호 반응함으로써 형성된다.

이와 같이 제 1 티타늄 나이트라이드층(23) 및 티타늄층(24)을 순차적으로 형성한 후 질소 분위기에서 열처리를 실시하여 확산 방지막이 완성되고, 이후 도 3(c)에 도시된 바와 같이, 텅스텐층(27)을 화학 기상 증착(Chemical Vapor Deposition; CVD) 방식으로 형성한 후 패터닝하여 금속 배선이 형성한다.

도 3(c)의 콘택홀 기저부를 확대한 도 4에 도시된 바와 같이, 제 2 티타늄 나이트라이드층(24A)은 미세 결정(microcrystalline) 구조로 형성된다. 티타늄 실리사이드층(25) 형성을 위한 열처리 공정 동안에 제 1 티타늄 나이트라이드층(23)에 함유된 질소 원자가 티타늄 원자와 실리콘 원자의 반응 속도 및 양을 일정하게 제어해 주기 때문에 제 1 티타늄 나이트라이드층(23)이 약 50Å 두께로 얇게 형성되더라도, 도 4에 도시된 바와 같이, 티타늄 실리사이드층(25)은 균일하게 형성된다. 따라서, 제 2 티타늄 나이트라이드층(24A)이 미세 결정 구조를 갖고, 티타늄 실리사이드층(25)이 균일하게 형성된 상태에서 WF_6가스를 이용하여 텅스텐층(27)을 형성할 경우, 형성 공정중에 텅스텐 원자(W)/플루오린 원자(F)와 실리콘 원자(Si)가 상호 확산되는 것이 방지된다. 한편, 열처리 동안에 극히 적은 산소(O_2) 가스에 의해 형성된 티타늄 옥사이드층(26)이 제 2 티타늄 나이트라이드층(24A)과 티타늄 실리사이드층(25) 사이에 존재하므로써, 확산 방지 효과는 더욱 극대화된다.

본 발명의 다른 실시 예로서 실리콘을 함유한 막 상부에 티타늄을 증착한 후 상술한 방법과 동일한 조건에서 급속 열질화 공정을 실시한 후 티타늄 나이트라이드층을 형성해도 동일한 효과를 얻을 수 있다.

도 5(a) 및 도 5(b)는 종래의 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진이고, 도 6(a) 및 도 6(b)는 본 발명에 따른 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진이다.

도 5(a)를 참조하면, 100Å 의 티타늄층을 형성하고 200Å 의 티타늄 나이트라이드층을 형성한 후 급속 열처리 공정을 실시하면 그레인 바운더리에서 티타늄 실리사이드의 덩어리가 형성된다. 이러한 상태에서 도 5(b)에서와 같이 890℃의 온도에서 1시간동안 열처리 공정을 실시하면 텅스텐 실리사이드층 하부에서 실리콘의 손실이 발생된다.

도 6(a)를 참조하면, 100Å 의 티타늄층을 형성하고 급속 열질화 공정을 실시한 후 200Å 의 티타늄 나이트라이드층을 형성하고 급속 열질화 공정을 실시한다. 이러한 공정에 의해 티타늄층과 티타늄 나이트라이드층 사이에 티타늄 실리사이드층과 티타늄 옥사이드층이 형성된다. 이러한 상태에서 도 6(b)에서와 같이 890℃의 온도에서 1시간동안 열공정을 실시하더라도 균일한 막질을 얻을 수 있다.

발명의 효과

상술한 바와 같이, 본 발명은 확산 방지막으로 스퍼터링 방식에 의해 제 1 티타늄 나이트라이드(TiN)층과 티타늄(Ti)층을 형성한 후 질소가 함유된 가스 분위기에서 급속 열질화 처리(RTN)를 실시하여 티타늄층을 미세 결정 구조의 제 2 티타늄 나이트라이드층으로 변형시키고, 콘택홀 기저부의 제 1 티타늄 나이트라이드층을 균일한 두께의 티타늄 실리사이드층으로 변형시키며, 제 1 티타늄 나이트라이드층과 티타늄 실리사이드층 사이에 티타늄 옥사이드(TiO)층이 형성되어 확산 방지 효과를 극대화시킬 수 있다.

(57) 청구의 범위

청구항 1.

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소정의 구조가 형성된 실리콘 기판 상부에 층간 절연막을 형성한 후 상기 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하는 단계와,

상기 콘택홀을 포함한 전체 구조 상부에 제 1 티타늄 나이트라이드층 및 티타늄층을 순차적으로 형성하는 단계와,

질소가 함유된 가스 분위기에서 열처리 공정을 실시하고, 이에 의해 상기 티타늄층은 제 2 티타늄 나이트라이드층으로 변화되고, 상기 제 1 티타늄 나이트라이드층과 상기 제 2 티타늄 나이트라이드층 사이에는 티타늄 옥사이드층이 생성되며, 상기 콘택홀 기저부의 제 1 티타늄 나이트라이드층은 티타늄 실리사이드층으로 변화되는 단계를 포함하여 이루어진 것을 특징으로 하는 반도체 소자의 확산 방지막 형성 방법.

청구항 2.

제 1 항에 있어서, 상기 열처리 공정은 질소(N_2) 가스, 암모늄(NH_3) 가스 및 질소(N_2)와 암모늄(NH_3)의 혼합 가스 분위기중 어느 하나의 분위기에서 실시하는 급속 열질화 공정인 것을 특징으로 하는 반도체 소자의 확산 방지막 형성 방법.

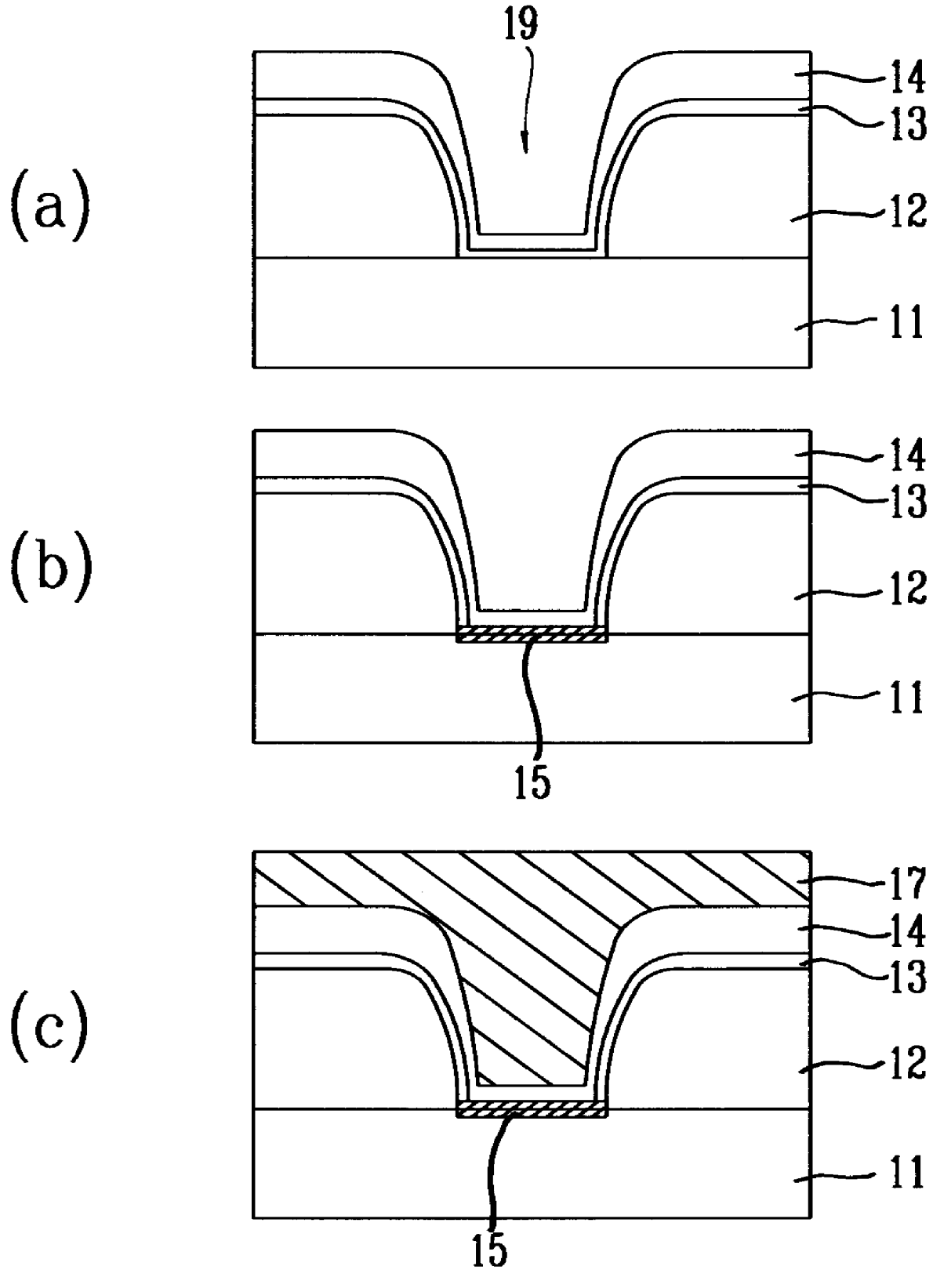
청구항 3.

제 1 항에 있어서, 상기 티타늄층은 400 내지 600Å 의 두께로 형성되는 것을 특징으로 하는 반도체 소자의 확산 방지막 형성 방법.

도면

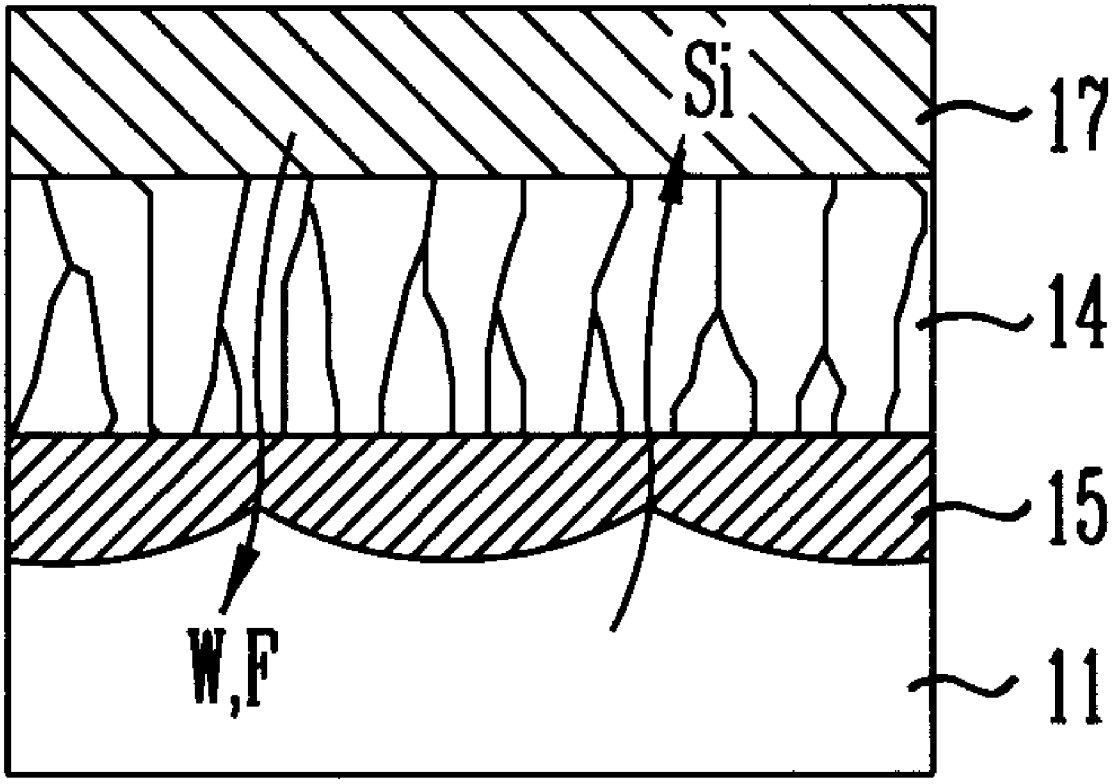
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도면 1



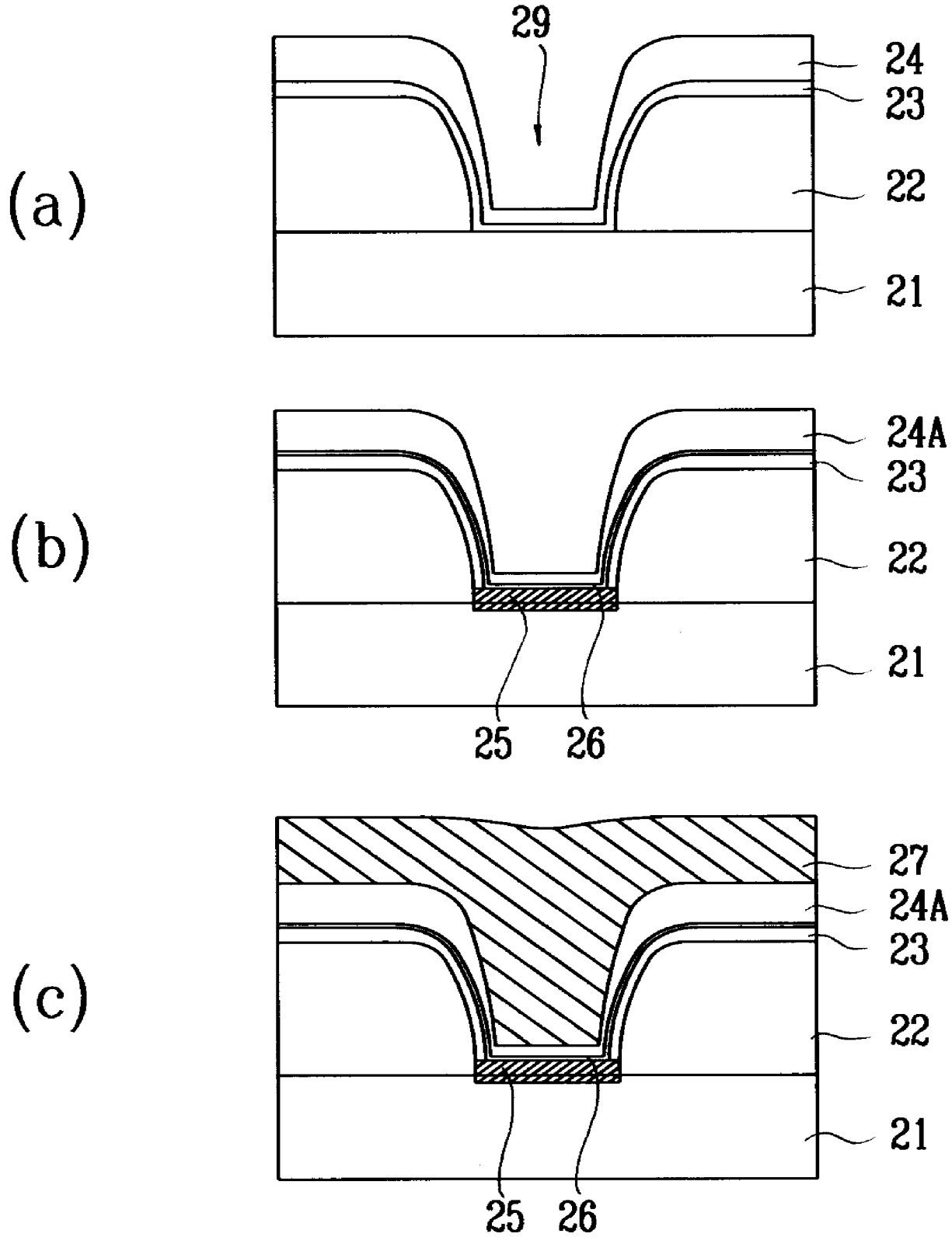
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도면 2



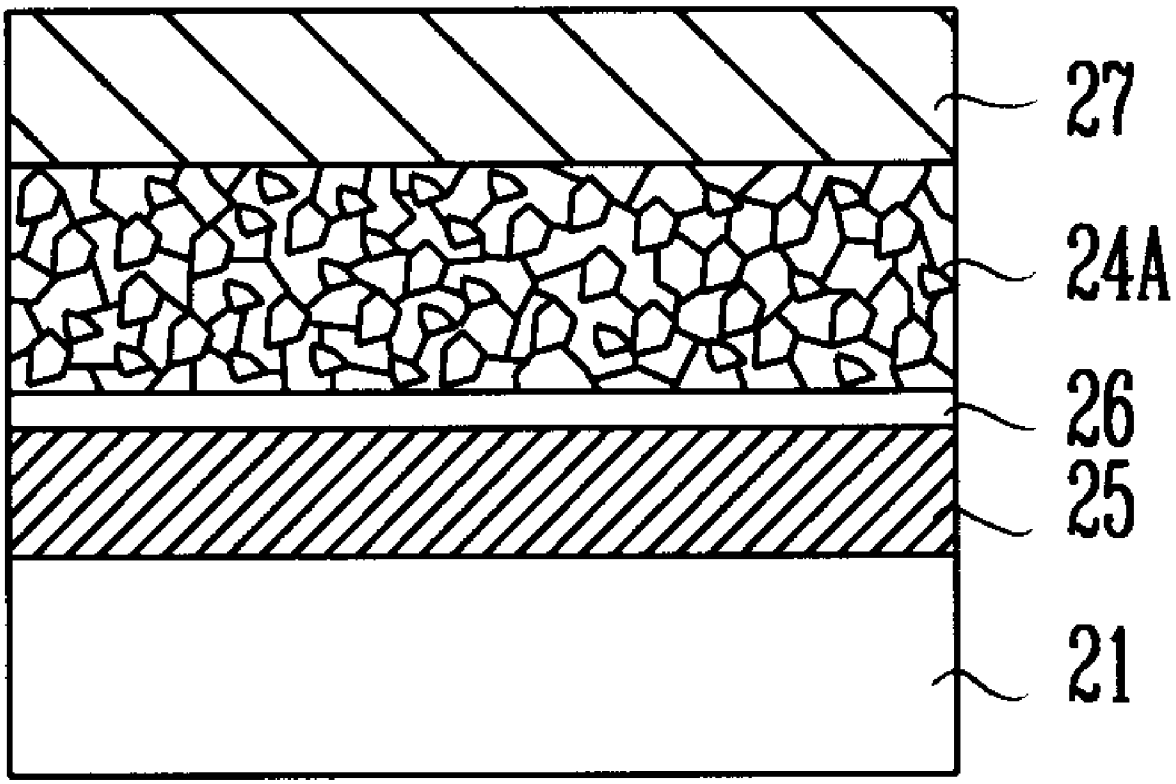
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도면 3

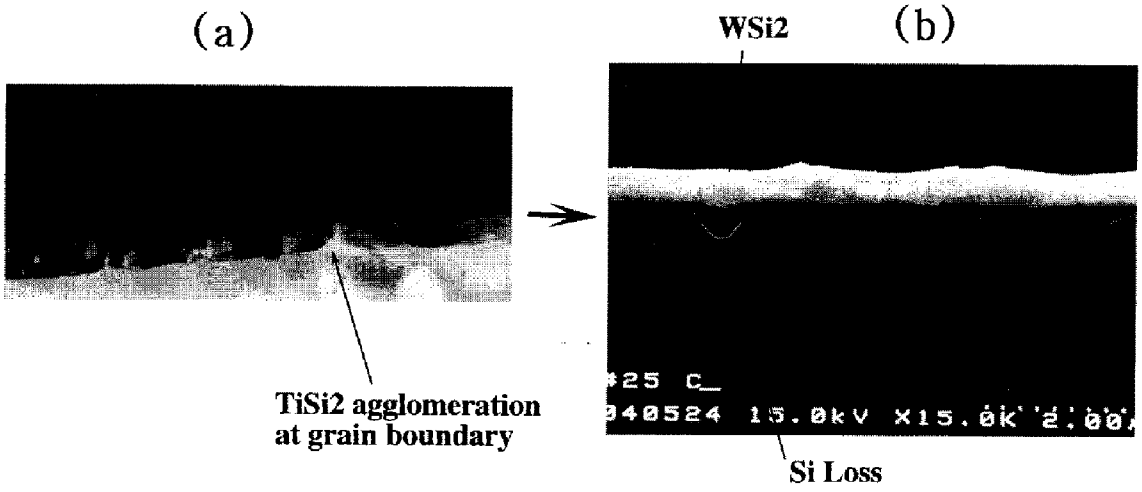


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도면 4

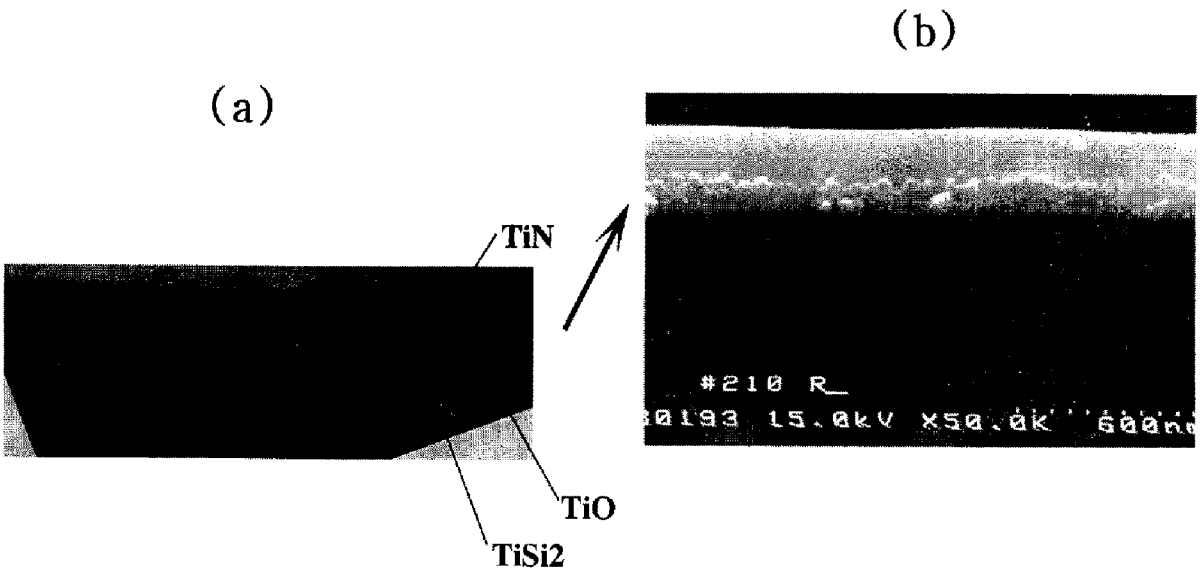


도면 5



GF Exhibit 1126 - 1346/2248

도면 6



GF Exhibit 1126 - 1347/2248

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Inventor	Sang-Gi Hong | U-Hyeon Kim
Applicant	SK hynix Inc.
Rightholder	Hyundai Electronics industry CO., LTD

발명의 명칭

반도체소자의확산방지막형성방법

Title of Invention

METHOD FOR FORMING DIFFUSION BARRIER LAYER OF SEMICONDUCTOR DEVICE

요약

본 발명은 반도체 소자의 확산 방지막 형성 방법에 관한 것으로, 실리콘 기판 상부에 형성된 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하고, 상기 콘택홀을 포함한 전체 구조 상부에 스퍼터링 방법으로 제 1 티타늄 나이트라이드(TiN)층과 티타늄(Ti)층을 형성한 후 질소가 함유된 가스 분위기에서 급속 열질화 처리(RTN)를 실시함으로써 티타늄층은 미세 결정 구조의 제 2 티타늄 나이트라이드층으로 되고, 제 1 티타늄 나이트라이드층은 콘택홀 기저부에서 균일한 두께의 티타늄 실리사이드층으로 되며, 제 2 티타늄 나이트라이드층과 제 1 티타늄 나이트라이드층 및 티타늄 실리사이드층 사이에 티타늄 옥사이드(TiO)층이 형성되어 확산 방지 효과를 극대화시킨다.

Abstract

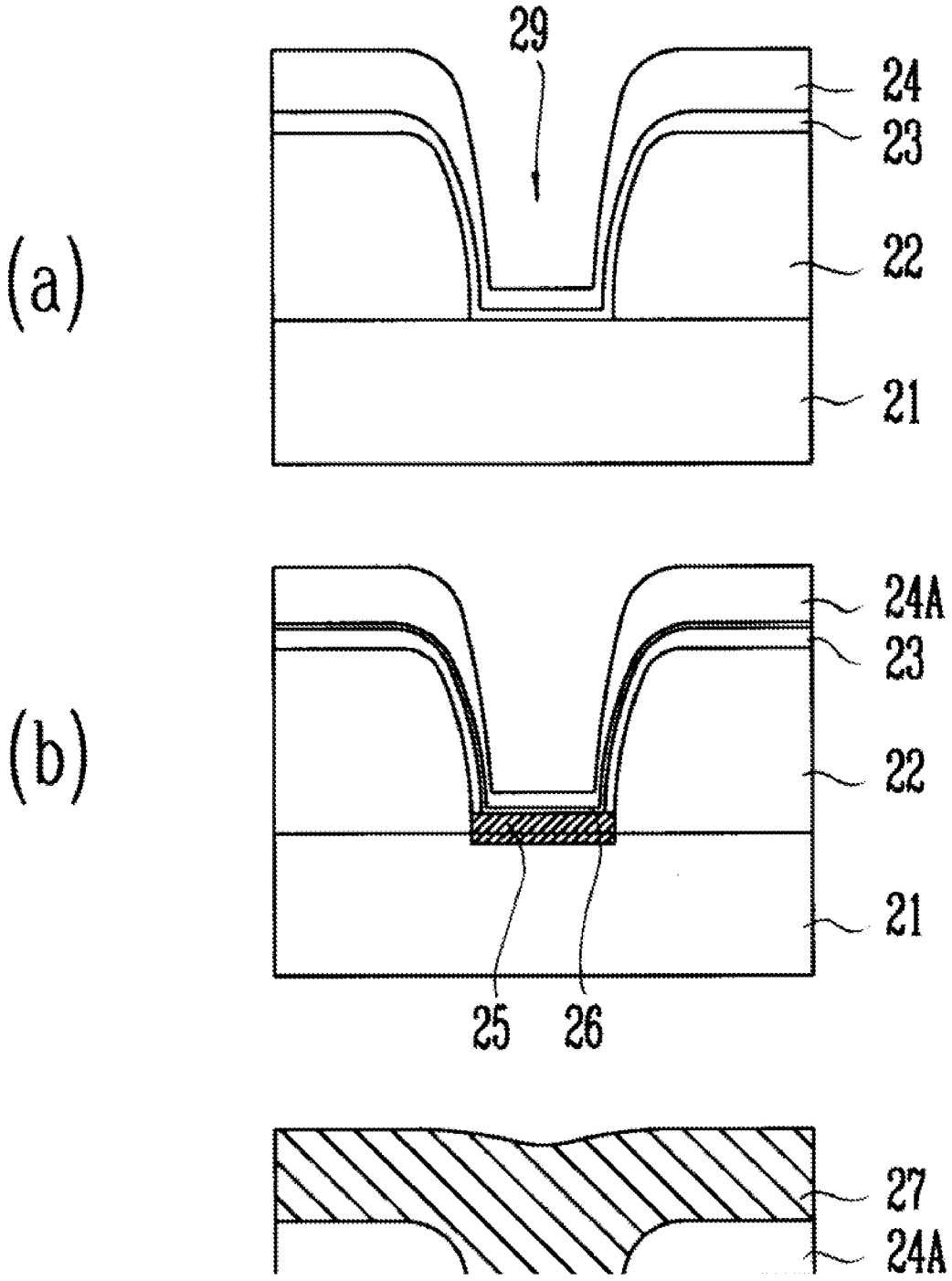
According to the invention, the contact hole etching the fixed region of the formed inter-layer insulating film and exposes the fixed region of the silicon substrate are formed in the upper silicon substrate as the method for forming diffusing barrier layer, of the semiconductor device. And by performing the rapid thermal nitridation (RTN) in the first titanium nitride (TiN) layer and the gas atmosphere in which nitrogen is the titanium (Ti) layer contained after doing the formation to the sputtering method including the contact hole the titanium layer is to the second titanium nitride layer of the nanocryatalline structure and the first titanium nitri

층간 절연막, 콘택홀, 티타늄 옥사이드층, 티타늄 실리사이드층, 확산 방지막

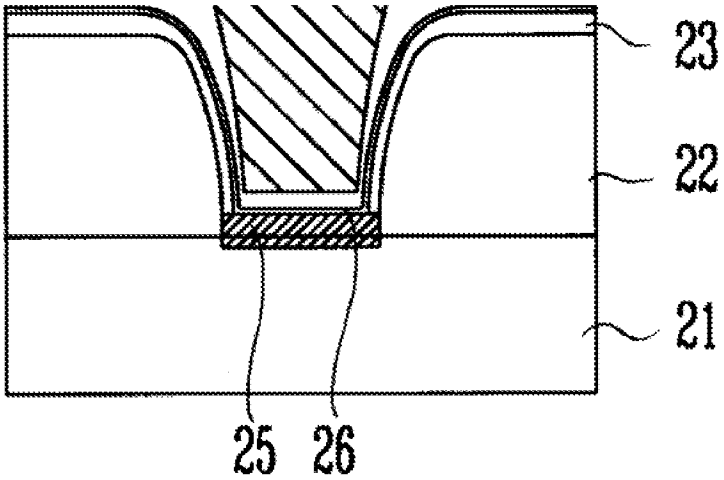
de layer is in the contact hole fundament to the titanium silicide layer of the uniform thickness and the titanium oxide (TiO) layer is formed between the second titanium nitride layer, the first titanium nitride layer and titanium silicide layer and the scattering prevention effect is maximized.

The inter-layer insulating film, the contact hole, the titanium oxide layer, the titanium silicide layer, the diffusion barrier .

대표도면(Representative drawing)



(c)



청구의 범위

청구 3항:

제 1 항에 있어서, 상기 티타늄층은 400 내지 600Å의 두께로 형성되는 것을 특징으로 하는 반도체 소자의 확산 방지막 형성 방법.

Scope of Claims

Claim 3:

As for claim 1, the method for forming diffusing barrier layer of the semiconductor device in which the titanium layer is formed into the thickness of 400 through 600Å.

배경기술

본 발명은 반도체 소자의 확산 방지막(metal barrier film) 형성 방법에 관한 것으로, 특히 콘택 저항을 감소시키며 확산 방지 효과를 증대시킬 수 있는 반도체 소자의 확산 방지막 형성 방법에 관한 것이다.

일반적으로, 반도체 소자가 고집적화 됨에 따라 콘택홀의 크기는 줄어들고 있다. 이에 따라 금속 콘택 공정시 콘택홀을 양호하게 매립하기 어렵고, 또한 콘택 저항이 증가되어 소자의 전기적 특성을 저하시키게 된다. 이를 해결하기 위하여, 티타늄(Ti)과 티타늄 나이트라이드(TiN)를 증착한 후 열처리하여 콘택홀 기저부에 티타늄 실리사이드(TiSi2)를 갖는 확산 방지막을 형성한다.

종래의 반도체 소자의 확산 방지막 형성 방법을 도 1(a) 내지 1(c)를 참조하여 설명하면 다음과 같다.

도 1(a)를 참조하면, 실리콘 기판(11) 상부에 형성된 층간 절연막(12)의 선택된 영역이 식각되어 실리콘 기판(11)의 소정 영역을 노출시키는 콘택홀(19)이 형성된다. 콘택홀(19)을 포함한 전체 구조 상부에 스퍼터링(sputtering) 방식으로 티타늄층(13) 및 티타늄 나이트라이드층(14)이 순차적으로 형성

Background Art

The invention relates to the diffusion barrier (metal barrier film) formation method of the semiconductor device, and particularly, to the method for forming diffusing barrier layer of the semiconductor device which can increase the scattering prevention effect while reducing the contact resistance.

Generally, the size of the contact hole is decreased as the semiconductor device is highly integrated. Accordingly, it is difficult in the metal contact process to be good reclaim the contact hole and moreover, the contact resistance is increased and the electrical characteristic of the device is lowered. To solve this, the titanium (Ti) and the diffusion barrier heat-treating the titanium nitride (TiN) after doing the deposition and has the titanium silicide (TiSi(SB)2(/SB)) on the contact hole fundament are formed.

The method for forming diffusing barrier layer of the conventional semiconductor device is made to be equal to the next it illustrates with reference to Figure 1(a) to 1 (c).

The contact hole (19) in which the selected domain of the inter-layer insulating film (12) formed in upper part the silicon substrate (11) is etched with reference to Figure 1(a) and exposing the fixed region of the silicon substrate (11) is formed. The

된다.

도 1(b)를 참조하면, 질소(N2) 또는 암모늄(NH3) 가스 분위기에서 급속 열처리(Rapid Thermal Process; RTP) 공정을 실시하여 콘택홀(19) 기저부의 티타늄층(13)이 티타늄 실리사이드층(15)으로 변형되게 한다. 티타늄 실리사이드층(15)은 급속 열처리 공정 동안에 실리콘 기판(11)의 실리콘 원자(Si)와 티타늄층(13)의 티타늄 원자(Ti)가 상호 반응하여 형성된다.

이와 같이 티타늄층(13) 및 티타늄 나이트라이드층(14)을 순차적으로 형성한 후 급속 열처리 공정을 실시하여 확산 방지막이 형성되고, 이후 도 1(c)에 도시된 바와 같이, 텅스텐층(17)을 화학 기상 증착(Chemical Vapor Deposition; CVD) 방식으로 형성한 후 패터닝하여 금속 배선이 형성된다.

도 1(c)의 콘택홀 기저부를 확대한 도 2에 도시된 바와 같이, 티타늄 나이트라이드층(14)은 원주형(columnar) 구조로 형성된다. 티타늄층(13)은 그 두께가 두꺼울 경우 급속 열처리에 의해 균일한 티타늄 실리사이드층을 형성할 수 있으나, 반도체 소자가 고집적화 되어감에 따라 콘택홀 크기가 줄어들어 종횡비(aspect ratio)가 크게되기 때문에 스퍼터링 방식으로 형성되는 티타늄층(13)의 층덮힘(step coverage)이 나쁘게 되므로 티타늄층(13)을 두껍게 형성하는데 한계가 있다. 티타늄층(13)을 두껍게 형성하기 위하여, 층덮힘이 우수한 CVD 방식을 적용하고 있으나, CVD 방식을 적용할 경우 박막에 불순물 함유량이 높아지는 등 많은 공정상의 문제점이 존재하므로 현재로서는 실질 공정에 적용하기 어려운 실정이다. 따라서, 텅스텐층(13)은 스퍼터링 방식으로 형성되며, 텅스텐층(13)의 두께가 임계 두께 이하일 경우 급속 열처리로 형성되는 티타늄 실리사이드층(15)은, 도 2에 도시된 바와 같이, 균일한 두께로 형성되지 못한다. 이와 같이 티타늄 나이트라이드층(14)이 원주형 구조를 갖고, 티타늄 실리사이드층(15)이 불균일하게 형성된 상태에서 WF6 가스를 이용하여 텅스텐층(17)을 형성할 경우, 형성 공정중에 원주형 구조의 티타늄 나이트라이드층(14)의 그레인 바운더리와 티타늄 실리사이드층(15)의 얇은 부분을 통해 텅스텐 원자(W)/플루오린 원자(F)와 실리콘 원자(Si)가 상호 확산되어 접합 파괴, 누설 전류 및 콘택 저항을 증가시켜 소자의 신뢰성을 저하시키는 문제점이 발생된다.

titanium layer (13) and titanium nitride layer (14) are successively formed with the sputtering mode including the contact hole (19).

In the nitrogen (N(SB)2(/SB)) with reference to Figure 1(b) or the ammonium (NH(SB)3(/SB)) gas atmosphere, the rapid thermal processing (Rapid Thermal Process: RTP) process is performed and the titanium layer (13) of the contact hole (19) base part is transformed into into the titanium silicide layer (15). The silicon atom (Si) of the silicon substrate (11) and titanium atom (Ti) of the titanium layer (13) cross-react and the titanium silicide layer (15) is formed for the rapid thermal processing.

In this way, the rapid thermal processing is successively performed after doing the formation and the diffusion barrier is formed with the titanium layer (13) and titanium nitride layer (14) as the and the tungsten layer (17) is patterned in the chemical vapor deposition (Chemical Vapor Deposition: CVD) mode after doing the formation and after the metal wiring is formed as shown in 1 (c).

The titanium nitride layer (14) enlarging the contact hole fundament of Figure 1(c) is formed with the columnar structure. In case the titanium layer (13) the thickness is thick the uniform titanium silicide layer can be formed with the rapid thermal processing. But as the semiconductor device is highly integrated the contact hole size is decreased and because the aspect ratio is large since the step coverage of the titanium layer (13) formed with the sputtering method is bad the titanium layer (13) is thickly formed but it has the limit. In order that the titanium layer (13) is thickly formed the CVD manner in which the step coverage is excellent is applied. But it is the difficult actual condition that it applies to the parenchyma process since the problem of many eutectic phase exists the impurity content is enhanced in the thin film in case of applying the CVD manner. Therefore, the titanium silicide layer (15) which the tungsten layer (13) is formed with the sputtering method and is formed into the rapid thermal processing in case the thickness of the tungsten layer (13) is the critical thickness or less as shown in FIG. 2 is unable to be formed with the uniform thickness. In this way, the titanium nitride layer (14) has the columnar structure and when the tungsten layer (17) is formed at the state is uneven where the titanium silicide layer (15) is formed using the WF 6 gas the problem of the tungsten atom (W) / fluorine atom (F) and silicon atom (Si) being mutually diffused among the formation process through the thin part of the grain boundary of the titanium nitride layer (14) of the columnar structure and titanium silicide l

ayer (15) and increasing the junction breakdown, and the leakage current and contact resistance an d decreasing the reliability of the device is genera ted.

발명의 내용

발명의 효과

상술한 바와 같이, 본 발명은 확산 방지막으로 스퍼터링 방식에 의해 제 1 티타늄 나이트라이드(TiN)층과 티타늄(Ti)층을 형성한 후 질소가 함유된 가스 분위기에서 급속 열질화 처리(RTN)를 실시하여 티타늄층을 미세 결정 구조의 제 2 티타늄 나이트라이드층으로 변형시키고, 콘택홀 기저부의 제 1 티타늄 나이트라이드층을 균일한 두께의 티타늄 실리사이드층으로 변형시키며, 제 1 티타늄 나이트라이드층과 티타늄 실리사이드층 사이에 티타늄 옥사이드(TiO)층이 형성되어 확산 방지 효과를 극대화시킬 수 있다.

Summary of Invention

Effects of the Invention

As described above, in the invention is the first titanium nitride (TiN) layer by the diffusion barrier the sputtering method and the gas atmosphere in which nitrogen is the titanium (Ti) layer contained after doing the formation, the rapid thermal nitridation (RTN) is performed and the titanium layer is transformed to the second titanium nitride layer of the nanocryatalline structure and the first titanium nitride layer of the contact hole fundament is transformed to the titanium silicide layer of the uniform thickness and the titanium oxide (TiO) layer is formed between the first titanium nitride layer and titanium silicide layer and the scattering prevention effect can be maximized.

기술적 과제

따라서, 본 발명은 콘택 저항을 감소시키면서 확산 방지 효과를 증대시킬 수 있는 반도체 소자의 확산 방지막 및 그 형성 방법을 제공하는데 그 목적이 있다.

상술한 목적을 달성하기 위한 본 발명의 확산 방지막 형성 방법은 반도체 소자를 제조하기 위한 소정의 구조가 형성된 실리콘 기판 상부에 형성된 층간 절연막의 소정 영역을 식각하여 상기 실리콘 기판의 소정 영역을 노출시키는 콘택홀을 형성하는 단계와, 상기 콘택홀을 포함한 전체 구조 상부에 제 1 티타늄 나이트라이드층 및 티타늄층을 순차적으로 형성하는 단계와, 질소가 함유된 가스 분위기에서 열처리 공정을 실시함으로써 상기 티타늄층은 제 2 티타늄 나이트라이드층이 되고, 상기 제 1 티타늄 나이트라이드층과 상기 제 2 티타늄 나이트라이드층 사이에는 티타늄 옥사이드층이 생성되며, 상기 콘택홀 기저부의 제 1 티타늄 나이트라이드층은 티타늄 실리사이드층으로 되는 단계를 포함하여 이루어진 것을 특징으로 한다.

Technical Task

Therefore, an object of the present invention is to provide the diffusion barrier of the semiconductor device which can increase the scattering preventi on effect while it reduces the contact resistance a nd method for forming the same.

The method for forming diffusing barrier layer of t he invention for achieving the above-described pu rpose comprises the step on the upper part of the entire structure, of successively forming the first t itanium nitride layer and titanium layer, and the s tep in the titanium layer, the second titanium nitri de layer is by performing the thermal process in t he gas atmosphere etching the fixed region of the inter-layer insulating film formed in the upper silic on substrate in which the predetermined structure for manufacturing the semiconductor device is for med and include the step of forming the contact h ole exposing the fixed region of the silicon substra te, and the contact hole. As to the step in the tita nium layer, the second titanium nitride layer is by, nitrogen occurs plentifully and the titanium oxide layer is generated between the first titanium nitri de layer and the second titanium nitride layer and that the first titanium nitride layer of the contact hole fundament consists of the titanium silicide la yer.

발명의 구성 및 작용

첨부된 도면을 참조하여 본 발명을 상세히 설명하기로 한다.

도 3(a) 내지 3(c)는 본 발명에 따른 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도이고, 도 4는 도 3(c)의 콘택홀 기저부를 확대한 도면이다.

도 3(a)를 참조하면, 반도체 소자를 제조하기 위한 소정의 구조가 형성된 실리콘 기판(21) 상부에 형성된 층간 절연막(22)의 선택된 영역을 식각하여 실리콘 기판(21)의 소정 영역을 노출시키는 콘택홀(29)이 형성된다. 콘택홀(29)을 포함한 전체 구조 상부에 스퍼터링 방식으로 제 1 티타늄 나이트라이드층(23) 및 티타늄층(24)이 순차적으로 형성된다. 제 1 티타늄 나이트라이드층(23)은 약 50Å의 두께로 형성되며, 티타늄층(24)은 약 400~600Å의 두께로 형성된다.

도 3(b)는 열처리 공정을 실시한 상태의 단면도로서, 열처리 공정은 저압용 반응로(low pressure furnace)에서 실시하거나 급속 열질화 처리(Rapid Thermal Nitridation; RTN)로 하며, 이때 분위기는 질소(N2) 가스, 암모늄(NH3) 가스 및 질소(N2)와 암모늄(NH3)의 혼합 가스 분위기중 어느 하나의 분위기로 한다. 열처리 결과, 티타늄층(24)은 제 2 티타늄 나이트라이드층(24A)으로 되고, 제 1 티타늄 나이트라이드층(23)과 제 2 티타늄 나이트라이드층(24A) 사이에는 티타늄 옥사이드층(TiO; 26)이 생성되며, 콘택홀(29) 기저부의 제 1 티타늄 나이트라이드층(23)은 티타늄 실리사이드층(25)으로 된다. 티타늄 실리사이드층(25)은 열처리 동안에 실리콘 기판(21)의 실리콘 원자(Si)와 제 1 티타늄 나이트라이드층(23)의 티타늄 원자(Ti)가 상호 반응함으로써 형성된다.

이와 같이 제 1 티타늄 나이트라이드층(23) 및 티타늄층(24)을 순차적으로 형성한 후 질소 분위기에서 열처리를 실시하여 확산 방지막이 완성되고, 이후 도 3(c)에 도시된 바와 같이, 텅스텐층(27)을 화학 기상 증착(Chemical Vapor Deposition; CVD) 방식으로 형성한 후 패터닝하여 금속 배선이 형성한다.

Structure & Operation of the Invention

The attached invention decides to be particularly illustrated.

It is the cross-sectional view in which Figure 3(a) to 3 (c) illustrates the method for forming diffusing barrier layer of the semiconductor device according to the present invention of the device. And figure 4 is a magnificated drawing the contact hole fundament of Figure 3(c).

The contact hole (29) etching the selected domain of the inter-layer insulating film (22) formed in upper part the silicon substrate (21) in which the predetermined structure for manufacturing the semiconductor device is formed with reference to Figure 3(a) and exposes the fixed region of the silicon substrate (21) is formed. The first titanium nitride layer (23) and titanium layer (24) are successively formed with the sputtering method including the contact hole (29). The first titanium nitride layer (23) is formed with the thickness of about 50 Å and the titanium layer (24) is formed into the thickness of about 400~600Å.

Figure 3(b) is the cross-sectional view of the state performing the thermal process. The thermal process performs in for low voltage furnace (low pressure furnace) or it does to the rapid thermal nitridation (Rapid Thermal Nitridation: RTN) and the environment does among the nitrogen (N(SB)2(/SB)) gas, and the ammonium (NH(SB)3(/SB)) gas, the nitrogen (N(SB)2(/SB)) and mixed gas atmosphere of the ammonium (NH(SB)3(/SB)) to one mood. The heat treatment result , and the titanium layer (24) consist of the second titanium nitride layer (24A) and the titanium oxide layer (TiO: 26) is generated between the first titanium nitride layer (23) and the second titanium nitride layer (24A) and the first titanium nitride layer (23) of the contact hole (29) base part consists of the titanium silicide layer (25). The titanium silicide layer (25) is formed for the thermal process since the silicon atom (Si) of the silicon substrate (21) and titanium atom (Ti) of the first titanium nitride layer (23) cross-react.

In this way, the first titanium nitride layer (23) and titanium layer (24) the thermal process are successively performed after doing the formation in the nitrogen atmosphere and the diffusion barrier is completed and the tungsten layer (27) is patterned in the chemical vapor deposition (Chemical Vapor Deposition: CVD) mode after doing the formation and after the metal wiring forms as shown in 3 (c).

도 3(c)의 콘택홀 기저부를 확대한 도 4에 도시된 바와 같이, 제 2 티타늄 나이트라이드층(24A)은 미세 결정(microcrystalline) 구조로 형성된다. 티타늄 실리사이드층(25) 형성을 위한 열처리 공정 동안에 제 1 티타늄 나이트라이드층(23)에 함유된 질소 원자가 티타늄 원자와 실리콘 원자의 반응 속도 및 양을 일정하게 제어해 주기 때문에 제 1 티타늄 나이트라이드층(23)이 약 50Å 두께로 얇게 형성되더라도, 도 4에 도시된 바와 같이, 티타늄 실리사이드층(25)은 균일하게 형성된다. 따라서, 제 2 티타늄 나이트라이드층(24A)이 미세 결정 구조를 갖고, 티타늄 실리사이드층(25)이 균일하게 형성된 상태에서 WF6 가스를 이용하여 텅스텐층(27)을 형성할 경우, 형성 공정중에 텅스텐 원자(W)/플루오린 원자(F)와 실리콘 원자(Si)가 상호 확산되는 것이 방지된다. 한편, 열처리 동안에 극히 적은 산소(O2) 가스에 의해 형성된 티타늄 옥사이드층(26)이 제 2 티타늄 나이트라이드층(24A)과 티타늄 실리사이드층(25) 사이에 존재하므로써, 확산 방지 효과는 더욱 극대화된다.

The second titanium nitride layer (24A) enlarging the contact hole fundament of Figure 3(c) is formed with the microcrystal (microcrystalline) structure. Because the nitrogen atom contained in the first titanium nitride layer (23) for the thermal process for the titanium silicide layer (25) formation regularly controls the reaction speed of the titanium atom and silicon atom and amount the first titanium nitride layer (23) is formed into about 50Å thickness. And yet the titanium silicide layer (25) is uniformly formed. Therefore, the second titanium nitride layer (24A) has the nanocryatalline structure and when the tungsten layer (27) is formed at the state where the titanium silicide layer (25) is uniformly formed using the WF 6 gas the state is prevented among the formation process that the tungsten atom (W) / fluorine atom (F) and silicon atom (Si) are mutually diffused. In the meantime, the titanium oxide layer (26) formed by the oxygen (O(SB)2(/SB)) gas which is exceedingly less for the thermal process exists between the second titanium nitride layer (24A) and titanium silicide layer (25). In that way the scattering prevention effect becomes more maximized.

본 발명의 다른 실시 예로서 실리콘을 함유한 막 상부에 티타늄을 증착한 후 상술한 방법과 동일한 조건에서 급속 열질화 공정을 실시한 후 티타늄 나이트라이드층을 형성해도 동일한 효과를 얻을 수 있다.

In the method and the same condition describing in detail at the upper part of the film containing the silicone as the dissimilar embodiment of the invention after depositing titanium, even if the titanium nitride layer is formed after the rapid thermal nitridation is performed the same effect can be obtained.

도 5(a) 및 도 5(b)는 종래의 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진이고, 도 6(a) 및 도 6(b)는 본 발명에 따른 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진이다.

Figure 5(a) and Figure 5(b) are the SEM picture of the diffusion barrier of the semiconductor device formed into the conventional method and Figure 6(a) and Figure 6(b) are the SEM picture of the diffusion barrier of the semiconductor device formed into the method according to the present invention.

도 5(a)를 참조하면, 100Å의 티타늄층을 형성하고 200Å의 티타늄 나이트라이드층을 형성한 후 급속 열처리 공정을 실시하면 그레인 바운더리에서 티타늄 실리사이드의 덩어리가 형성된다. 이러한 상태에서 도 5(b)에서와 같이 890℃의 온도에서 1시간동안 열처리 공정을 실시하면 텅스텐 실리사이드층 하부에서 실리콘의 손실이 발생된다.

The titanium layer of 100Å is formed and if the rapid thermal processing is performed after doing the formation, the lump of the titanium silicide is formed with the titanium nitride layer of 200Å as the with reference to Figure 5(a) at the grain boundary. In this state, the loss of the silicone comes in the tungsten silicide layer lower part if the thermal process is performed Figure 5(b) at a temperature of 890℃ for 1 hour.

도 6(a)를 참조하면, 100Å의 티타늄층을 형성하고 급속 열질화 공정을 실시한 후 200Å의 티타늄 나이트라이드층을 형성하고 급속 열질화 공정을 실시한다. 이러한 공정에 의해 티타늄층과 티타늄 나이트라이드층 사이에 티타늄 실리사이드층과 티타늄 옥사이드층이 형성된다. 이러한 상태에서 도 6(b)에서와 같이 890℃의 온도에서 1시간동안 열공정을 실시하더라도

After the titanium layer of 100Å is formed and the rapid thermal nitridation is performed with reference to Figure 6(a) the titanium nitride layer of 200Å is formed and the rapid thermal nitridation is performed. By this process, the titanium silicide layer and titanium oxide layer are formed between the titanium layer and titanium nitride layer. In thi

균일한 막질을 얻을 수 있다.

s state, although the thermal process is performe d Figure 6(b) at a temperature of 890℃ for 1 hou r the uniform thin film can be obtained.

도면에 대한 간단한 설명

도 1(a) 내지 1(c)는 종래의 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도.

도 2는 도 1(c)의 콘택홀 기저부를 확대한 도면.

도 3(a) 내지 3(c)는 본 발명에 따른 반도체 소자의 확산 방지막 형성 방법을 설명하기 위한 소자의 단면도.

도 4는 도 3(c)의 콘택홀 기저부를 확대한 도면.

도 5(a) 및 도 5(b)는 종래의 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진.

도 6(a) 및 도 6(b)는 본 발명에 따른 방법으로 형성된 반도체 소자의 확산 방지막의 SEM 사진.

#60#도면의 주요 부분에 대한 부호 설명>

11 및 21 : 실리콘 기판 12 및 22 : 층간 절연막

13 및 24 : 티타늄(Ti)층
14, 23 및 24A : 티타늄 나이트라이드(TiN)층
15 및 25 : 티타늄 실리사이드(TiSi2)층

26 : 티타늄 옥사이드(TiO)층 17 및 27 : 텅스텐층

19 및 29 : 콘택홀

Brief explanation of the drawing

The cross-sectional view in which Figure 1(a) to 1 (c) illustrates the method for forming diffusing ba rrier layer of the conventional semiconductor devi ce of the device.

Fig. 2 is the magnificated drawing the contact hol e fundament of Figure 1(c).

The cross-sectional view in which Figure 3(a) to 3 (c) illustrates the method for forming diffusing ba rrier layer of the semiconductor device according to the present invention of the device.

Fig. 4 is the magnificated drawing the contact hol e fundament of Figure 3(c).

The SEM picture of the diffusion barrier of the se miconductor device in which Figure 5(a) and Figur e 5(b) are formed into the conventional method.

The SEM picture of the diffusion barrier of the se miconductor device in which Figure 6(a) and Figur e 6(b) are formed into the method according to th e present invention.

The code description > toward the main part of th e < drawing.

With 11 21: with the silicon substrate 12 22: inter -layer insulating film.

With 13 24: titanium (Ti) layer.
With 14, 23 24A: titanium nitride (TiN) layer.
With 15 25: titanium silicide (TiSi(SB)2(/SB)) laye r.

26: with the titanium oxide (TiO) layer 17 27: tun gsten layer.

With 19 29: contact hole.

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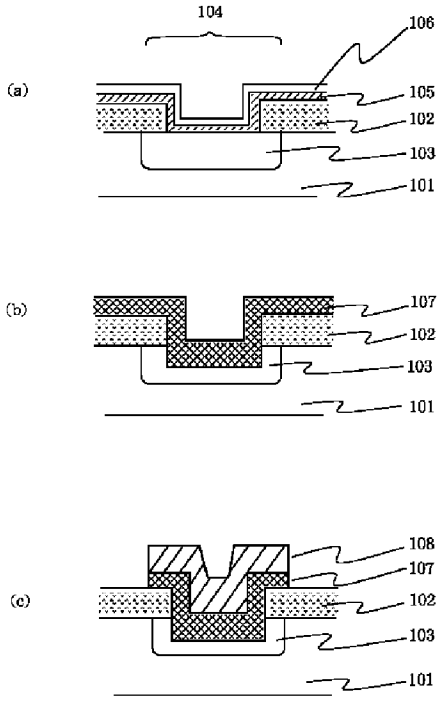
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(71)出願人　000205041
大見　忠弘
宮城県仙台市青葉区米ケ袋２－１－17－301
(72)発明者　大見　忠弘
宮城県仙台市青葉区米ケ袋２の１の17の301
(72)発明者　山田　圭一
宮城県仙台市青葉区荒巻字青葉（無番地）
東北大学工学部電子工学科内
(74)代理人　弁理士　福森　久夫

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】
【目的】　本発明は、電極と半導体とのコンタクト抵抗を低減し、また微細で、極浅・極薄層の半導体と電極との接触構造を形成することが可能な半導体装置及びその製造方法を提供することを目的とする。
【構成】　半導体表面に、少なくとも一層の金属層と半導体層とを大気に曝さずに連続して形成した後、熱処理して前記金属層と前記半導体とを反応させ金属と半導体との化合物を形成することを特徴とする。さらに、前記熱処理前に、イオン注入することを特徴とする。また、半導体と電極とのコンタクト部に、該半導体と金属との化合物が形成された半導体装置において、前記化合物と前記半導体との界面の深さを２２ｎｍより浅くした、または該化合物の厚さの半分以上が前記半導体表面より上方側に位置することを特徴とする。さらに、多層の金属配線構造を有する場合、上下の金属配線を接続するコンタクト部に薄いシリサイド層を有することを特徴とする。



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【特許請求の範囲】
【請求項１】　半導体表面の少なくとも一部に、少なくとも一層の金属層と半導体層とを大気に曝さずに連続して形成した後、熱処理して前記金属層と前記半導体とを反応させ金属と半導体との化合物を形成することを特徴とする半導体装置の製造方法。
【請求項２】　前記熱処理の前に、前記半導体に前記半導体層及び金属層を介して所定の不純物原子もしくは不純物分子をイオン注入することを特徴とする請求項１に記載の半導体装置の製造方法。
【請求項３】　前記イオンは、前記半導体を構成する元素または前記半導体中において電子あるいはホールを発生する原子あるいはその原子を含む分子であることを特徴とする請求項２に記載の半導体装置の製造方法。
【請求項４】　前記半導体と前記化合物との界面で前記半導体中の不純物濃度が最大となるように、前記半導体の不純物をイオン注入することを特徴とする請求項３に記載の半導体装置の製造方法。
【請求項５】　前記イオンの注入量は、1×10^{13}～$4\times10^{18}cm^{-2}$であることを特徴とする請求項２～４のいずれか１項に記載の半導体装置の製造方法。
【請求項６】　前記半導体は、シリコン（Ｓｉ）半導体であることを特徴とする請求項１～５のいずれか１項に記載の半導体装置の製造方法。
【請求項７】　前記金属層は、高融点金属、高融点金属を含む合金、または高融点金属の化合物であることを特徴とする請求項１～６のいずれか１項に記載の半導体装置の製造方法。
【請求項８】　前記金属層は、Ｔａ，Ｔｉ，Ｗ，Ｃｏ，Ｍｏ，Ｈｆ，Ｎｉ，Ｚｒ，Ｃｒ，Ｖ，Ｐｄ及びＰｔの内少なくとも１つ含むことを特徴とする請求項７に記載の半導体装置の製造方法。
【請求項９】　前記金属層の厚さは、１～５０ｎｍであることを特徴とする請求項１～８のいずれか１項に記載の半導体装置の製造方法。
【請求項１０】　前記半導体層は、不純物濃度が$1\times10^{18}cm^{-3}$以下であることを特徴とする請求項１～９のいずれか１項に記載の半導体装置の製造方法。
【請求項１１】　前記半導体層の厚さは、０．３ｎｍ以上であることを特徴とする請求項１～１０のいずれか１項に記載の半導体装置の製造方法。
【請求項１２】　前記半導体層の厚さを前記金属層の厚さ以上として、前記化合物と前記半導体との界面を浅くすることを特徴とする請求項１１に記載の半導体装置の製造方法。
【請求項１３】　前記熱処理後に形成された前記化合物の厚さの半分以上が、前記半導体層側に位置していることを特徴とする請求項１１または１２に記載の半導体装置の製造方法。
【請求項１４】　前記半導体層は、シリコン（Ｓｉ）半導体からなることを特徴とする請求項１～１３のいずれか１項に記載の半導体装置の製造方法。
【請求項１５】　前記熱処理後において、未反応の半導体層が残っていない場合には、続いて第２の金属層を形成することを特徴とする請求項１～１４のいずれか１項に記載の半導体装置の製造方法。
【請求項１６】　前記熱処理後において、未反応の半導体層を取り除いて、第２の金属層を形成することを特徴とする請求項１～１４のいずれか１項に記載の半導体装置の製造方法。
【請求項１７】　前記熱処理後において、未反応の半導体層上に第２の金属層を形成した後熱処理して、前記未反応の半導体層と第２の金属層の金属との化合物を形成することを特徴とする請求項１～１４のいずれか１項に記載の半導体装置の製造方法。
【請求項１８】　基板上に金属層、半導体層を大気に曝さずに連続して形成後、該半導体層を所定の形状にパターニングし、続いて熱処理して前記金属層と前記半導体層を反応させて金属と半導体との化合物を形成し、その後未反応の金属層をエッチングして取り除き、金属と半導体との化合物を所定の形状に形成することを特徴とする半導体装置の製造方法。
【請求項１９】　請求項１～１８のいずれか１項に記載の半導体装置の製造方法により作製された半導体装置。
【請求項２０】　半導体と電極とのコンタクト部に、該半導体と金属との化合物が形成された半導体装置において、前記化合物と前記半導体との界面の深さを２２ｎｍより浅くしたことを特徴とする半導体装置。
【請求項２１】　半導体と電極とのコンタクト部に、該半導体と金属との化合物が形成された半導体装置において、前記化合物と前記半導体との界面の深さを１２ｎｍ以下にしたことを特徴とする請求項２０に記載の半導体装置。
【請求項２２】　半導体と電極とのコンタクト部に、該半導体と金属との化合物が形成された半導体装置において、該化合物の厚さの半分以上が、前記半導体表面より上方側に位置していることを特徴とする半導体装置。
【請求項２３】　多層の金属配線構造を有する半導体装置において、上下の金属配線を接続するコンタクト部に薄いシリサイド層を有することを特徴とする半導体装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、半導体装置の製造方法に係わり、より詳細には、超高密度集積回路（ＵＬＳＩ）に適合した半導体装置及びその製造方法に関する。
【０００２】
【関連技術】現在、ＵＬＳＩの集積度は目ざましい勢いで増大し続けており、素子の寸法としては０．１μｍ、さらには、それをも凌駕する超微細寸法の素子の実現を

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も目指して盛んに研究開発が進められている。

【０００３】素子の高集積化により、配線構造の複雑化・多層化が一段と進展している。それに伴い、配線同士の接続や金属配線と半導体との接続のためのコンタクト部の数は爆発的に増大している上に、その寸法に関してはより一層の超微細化が推し進められてきている。ＵＬＳＩ中に存在する各種のコンタクトの高信頼化・高性能化は、ＵＬＳＩの高信頼化・高性能化を実現するための鍵となる重要な開発項目の一つである。

【０００４】金属と半導体とのコンタクト部の高信頼化・高性能化の達成のためには、低コンタクト抵抗化が必須であり、その実現のためには、超清浄なコンタクト界面の形成が必要不可欠である。その理由は、コンタクト界面における電気伝導の妨げとなるような絶縁物層（例えば酸化膜等）の存在は、コンタクト抵抗の増加及びコンタクト抵抗値のばらつきを招くからである。

【０００５】しかしながら、金属配線同士を接続するためのコンタクトの場合にせよ、半導体素子のオーミック性接触の電極を形成するための金属と半導体とのコンタクトの場合にせよ、超清浄なコンタクト界面を得ることは非常に難しい。その理由は、コンタクトを形成するためには、金属表面あるいは半導体に不純物が高濃度に添加された表面等、非常に酸化されやすい材質の表面に対して電極材料を形成しなければならず、形成された界面には酸化膜が残りやすいからである。例えば、金属表面であれば、大気に数秒曝すだけで２～５ｎｍの酸化膜が形成されるし，n^+－Ｓｉ表面であれば、通常の超純水で洗浄するだけで、０．５～１ｎｍのSiO_2が形成される。このことから、半導体素子のコンタクト構造形成において、酸化膜の存在しないコンタクト界面を安定して実現する事が、如何に困難な技術であるかが容易に理解できる。従って、ＵＬＳＩ製造技術において、超清浄な金属と半導体とのコンタクト界面の形成技術の確立が果たす役割は絶大なるものである。

【０００６】従来、コンタクト形成において、先に述べた様な界面に存在する汚染、特に酸化膜の成長に対する解決策として、コンタクト電極材料形成後の熱処理が行われている。金属とシリコンとの接合形成においては、高融点金属のシリサイドを形成しコンタクト抵抗の低減を図るという技術が開発されている。高融点金属薄膜をシリコン上に形成した後に熱処理を行い、シリサイド化合物を形成し、シリサイドとシリコンとの界面をコンタクト形成直後の界面の位置よりも深い地点にもってくることにより、清浄なシリサイドとＳｉとの界面を得ることが可能となる。さらには、安定したシリサイド形成を行うため、あるいはシリサイド化温度の低温化という目的から、イオンビームミキシングを用いたシリサイド形成技術も開発されている。シリコン上に高融点金属を成膜後、その上からイオン注入を行い、その後熱処理を施すことによりシリサイドを形成する技術である。

【０００７】しかしながら、これらのシリサイド形成による金属と半導体とのコンタクト形成方法には、解決すべきいくつかの問題点が存在する。

【０００８】ここで、n^+-Ｓｉ上へＴａシリサイド電極を形成する場合を例にとり、先行技術に係わる問題点を図１０～１２を用いて説明する。図１０は、n^+-Ｓｉ上へのＴａシリサイド電極の形成工程を示す断面図である。図１０（ａ）において、１００１はｐ型シリコンウェハであり、抵抗率は０．３～１．０Ω・ｃｍである。ウェハの表面には絶縁膜としてSiO_2 １００２が厚さ約５００ｎｍ程度形成されている。ウェハの表面には、一部にｎ型の不純物濃度が$2\times10^{20}cm^{-3}$であるn^+高濃度層１００３が形成されており、その高濃度層１００３内の領域の一部が外部と電気的に導通がとれるようにSiO_2 １００２に開口部１００４が少なくとも１ヶ所設けられている。その上には、Ｔａ層１００５が厚さ約１０ｎｍ程度形成されている。この構造を有するウェハに対して、熱処理を行いシリサイド層（$TaSi_2$）１００６を形成する（図１０（ｂ）参照）。熱処理の方法としては、電気炉を用い、Ａｒガス流量を２ｌ／ｍｉｎとし、９００℃、１時間のアニール処理を行った。その上に引き出し配線材料として、Ｔａ層１００７を厚さ５００ｎｍ程度形成した後に、パターニングを行った（図１０（ｃ）参照）。

【０００９】図１１に、この製作工程により形成された$TaSi_2$／n^+-Ｓｉコンタクトのコンタクト抵抗の測定結果を示す。抵抗値及びその値のばらつきの幅ともに、高性能ＵＬＳＩの実現のために充分な値とはなっていない。ＭＯＳトランジスタのソースやバイポーラトランジスタのエミッタの金属半導体の接触抵抗は徹底的に低いことが要求される。ソースやエミッタの抵抗Ｒｓが大きいと、トランジスタの流れる電流Ｉを大きくできず、ＬＳＩの高速動作が実現されなくなってしまうからである。ソースやエミッタに抵抗Ｒｓが存在すると、真性トランジスタに加わる電圧Ｖｇｉは、Ｖｇｉ＝Ｖｇ－ＲｓＩとなり、外部から印加された制御電圧ＶｇよりＲｓＩだけ小さくなってしまう。トランジスタの変換コンダクタンスをｇｍとすると、Ｉ＝ｇｍ（Ｖｇ－ＲｓＩ）より、Ｉ＝ｇｍＶｇ／（１＋ｇｍＲｓ）となり、Ｒｓが大きいと分母が大きくなって、電流Ｉは極端に小さくなってしまう。例えば、コンタクトホールの面積が０．１ｘ０．１μm^2（$=10^{-10}cm^2$）のとき、従来の接触抵抗Ｒｃ＝１ｘ$10^{-7}\Omega cm^2$では、１つのコンタクトだけで１ＫΩの接触抵抗となってしまう。通常、ＣＭＯＳ構造の場合、電源とアースの間には最低４個のコンタクトが入ることになるから、Ｒｃは$1\times10^{-9}\Omega cm^2$以下にすることが不可欠である。

【００１０】図１２に、以上の製作工程により形成された$TaSi_2$／n^+-Ｓｉ接合の深さ方向の不純物濃度分布を２次イオン質量分析（ＳＩＭＳ）により測定した結

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果を示す。以上の技術では、シリサイドとＳｉの界面の清浄化はある程度実現できるものの、初期の界面に存在していた酸素がシリサイド層中に取り込まれてしまい、抵抗の増加をもたらす一因となることが分かった。また、熱処理を施す前に、金属表面に酸化膜が形成されていれば、その酸素が熱処理中にシリサイド層に混入することとなり、形成されたシリサイド層の抵抗が増加することが確認された。

【００１１】さらに、先行技術によるシリサイド化を用いた電極形成工程における重大な問題として、シリコン基板へのシリサイド層の食い込みという問題がある。

【００１２】高融点金属とシリコンとのシリサイド化反応においては、シリサイド層がシリコン層へと深く進入していくため、シリサイドとシリコンとの接合の極浅化を達成することは非常に困難である。

【００１３】Ｔａとシリコンとの反応によるタンタルシリサイド（$TaSi_2$）の形成を例にとり、シリサイド層がどの程度シリコン基板に食い込むかを調べた結果を図１３に示す。厚さ１０ｎｍのＴａをシリコン基板上に成膜し熱処理を行いシリコン基板と反応させると、シリコン基板表面に厚さ約２４ｎｍのタンタルシリサイド層が形成される。初期のＴａとシリコン界面を基準にとると、深さ２２ｎｍの位置にまでシリサイド層が食い込んでいる。形成されたシリサイドは、膜厚の実に９割以上がシリコン基板中に沈み込んだ形となっていることが分かる。このため、Ｓｉとシリサイドの格子間隔の違いから大きな歪が局所的に発生し、欠陥、転移発生の原因となっている。従って、先行技術によるシリサイド化を用いた電極形成方法は、極薄・極浅接合を有する半導体素子の電極形成に用いるためには、素子構造上の制限を伴うことになる。

【００１４】ＵＬＳＩの超微細化・超高集積化の進展とともに、半導体中の接合、例えば、ＭＯＳＦＥＴのソース・ドレインやバイポーラトランジスタのエミッタ等、ますます極浅化が進み、１０～５０ｎｍ程度にまで達している。この様な極浅な接合深さを有する半導体層に対してオーミックコンタクト電極を形成する工程に金属薄膜とシリコンとのシリサイド化工程を用いる場合、先行技術による形成方法では、シリサイド層がソース・ドレインやエミッタ等の極薄層を突き抜けてしまう恐れがある。

【００１５】これらのことから判断すると、従来のシリサイド形成技術では、コンタクト抵抗の徹底的な低減のための完璧な解決策とはいえず、さらに接合の極浅化に対する問題も生じ、ＵＬＳＩの高性能化、高信頼化の達成は非常に困難であると言わざるを得ない。

【００１６】

【発明が解決しようとする課題】本発明は、高性能・高信頼性ＵＬＳＩのための半導体装置における電極・配線形成工程において必要不可欠である重要な２つの要求項目の実現を主目的とする。１つは、電極部と半導体層とのコンタクト抵抗の低減のために、酸化膜を主とした汚染層を無くし、金属層と半導体層界面近傍１ｎｍ程度の領域の半導体層中の不純物濃度即ち、電子、ホール密度を最大にした高品質の金属と半導体との接触構造を形成することであり、もう１つは、極浅・極薄層を有する半導体装置のための金属と半導体との接触構造を形成することである。

【００１７】

【課題を解決するための手段】本発明の半導体装置の製造方法は、半導体表面の少なくとも１部に、少なくとも一層の金属層と半導体層とを大気に曝さずに連続して形成した後、熱処理して前記金属層と前記半導体とを反応させ金属と半導体との化合物を形成することを特徴とする。

【００１８】さらに、前記熱処理の前に、前記半導体に前記半導体層及び金属層を介して所定の不純物原子もしくは不純物分子をイオン注入するのが好ましく、注入イオンとしては、前記半導体を構成する元素または前記半導体中において電子あるいはホールを発生する原子あるいはその原子を含む分子が好適であり、注入量は、1×10^{13}～$4\times10^{18}cm^{-2}$が好ましい。

【００１９】更に、前記金属層は、Ｔａ，Ｔｉ，Ｗ，Ｃｏ，Ｍｏ，Ｈｆ，Ｎｉ，Ｚｒ，Ｃｒ，Ｖ，Ｐｄ及びＰｔの内少なくとも１つ含む高融点金属、高融点金属を含む合金、または高融点金属の化合物であることが好ましく、その膜厚は、１～５０ｎｍが好ましい。

【００２０】また、前記半導体層は、不純物濃度が$1\times10^{18}cm^{-3}$以下であり、大気に曝したり超純水で洗浄しても、すぐには表面が酸化されない濃度であることが好ましい。また、膜厚は、０．３ｎｍ以上であることが好ましい。さらには、前記半導体層の厚さを前記金属層の厚さよりも大きくするのが好ましい。

【００２１】更にまた、前記半導体及び半導体層は、シリコン半導体であるのが好ましい。

【００２２】本発明において、前記熱処理後、更に第２の金属層を形成する際、未反応の半導体層が存在する場合、未反応の半導体層を取り除いて、第２の金属層を形成する、あるいは、未反応の半導体層上に第２の金属層を形成した後熱処理して、前記未反応の半導体層と第２の金属層の金属との化合物を形成する。

【００２３】また、本発明の半導体装置の製造方法は、基板上に金属層、半導体層を大気に曝さずに連続して形成後、続いて熱処理して前記金属層と前記半導体層を反応させて金属と半導体との化合物を形成し、その後未反応の金属層をエッチングして取り除き、金属と半導体との化合物を所定の形状に形成することを特徴とする。本発明の半導体装置は、上記製造方法により作製されたことを特徴とする。

【００２４】また、半導体と電極とのコンタクト部に、

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該半導体と金属との化合物が形成された半導体装置において、前記化合物と前記半導体との界面の深さを２２ｎｍより浅くしたことを特徴とする。さらに、本発明の半導体装置は、半導体と電極とのコンタクト部に、該半導体と金属との化合物が形成された半導体装置において、該化合物の厚さの半分以上が、前記半導体表面より上方側に位置していることを特徴とする。

【００２５】さらにまた、本発明の半導体装置は、多層の金属配線構造を有する半導体装置において、上下の金属配線を接続するコンタクト部に薄いシリサイド層を有することを特徴とする。

【００２６】

【作用】本発明では、金属配線同志あるいは電極材料と半導体の接合形成において、非常に酸化されやすい金属の超清浄な表面に対して、酸化膜の成長等の汚染を防ぐために半導体層を覆いかぶせ、熱処理を施し、金属と半導体との化合物を形成している。これにより、酸化膜の存在しない電極と半導体との接合、及び酸素等の不純物が非常に少なく低抵抗である電極層を形成することができる。また、それと同時に、金属層の上下を半導体で挟む形で金属と半導体とを反応させることにより、反応に必要な半導体を金属の上下両方から供給させることが可能となる。これにより、金属層全体を反応させた際の、金属と半導体との化合物層の半導体中への食い込み深さを浅くすることが可能となる。特に、半導体層の厚さを金属層の厚さ以上とすることで、この食い込みをより一層浅くすることができる。尚、本発明において、半導体層は半導体と同種の材料が好ましいが、異種材料であっても上記効果は得られる。

【００２７】さらに、熱処理前に、金属層及び半導体層を透過させて金属層と半導体との界面近傍にイオン注入を行うことも、接触抵抗低減等の特性改善のために効果的である。イオン注入により、金属と半導体とがミキシングされ化合物形成の為の熱処理温度や処理時間の低減が可能となる。注入イオン種としては、より一層のコンタクト抵抗の減少、半導体の再結晶化等の観点から、半導体のドーパント、半導体構成元素、金属層構成元素等が好適に用いられる。特に、半導体のドーパントとなるイオンを用いて、金属と半導体との化合物層と半導体との最終的な界面部で、ドーパント濃度が最大となるように製造工程条件を制御することにより、金属と半導体とのコンタクト抵抗の低減を図ることができる。イオン注入量及びイオンエネルギは、注入イオン種、熱処理条件、半導体層及び金属層の膜厚、構成元素等により適宜決定されるが、より一層のコンタクト抵抗の減少、半導体の再結晶化の観点から、それぞれ1×10^{13}～$4\times10^{18}cm^{-2}$、１６～２００ＫｅＶが好ましい。また、注入量は1×10^{15}～$1\times10^{17}cm^{-2}$がより好ましい。

【００２８】本発明の製造方法において、半導体及び半導体層としてはＳｉ，Ｇｅ等、金属層としてはＴａ，Ｔｉ，Ｗ，Ｃｏ，Ｍｏ，Ｈｆ，Ｎｉ，Ｚｒ，Ｃｒ，Ｖ，Ｐｄ，Ｐｔ等が好適に用いられる。特に、半導体の材料としてＳｉ、金属材料としてＴａ，Ｔｉ，Ｗ，Ｐｔ等の高融点金属を選択した場合に好適に適用され、ＬＳＩのより一層の高性能化を可能とする製造方法として非常に有望な製造方法となる。

【００２９】半導体層及び金属層の膜厚は、イオン注入条件、熱処理条件、及びその使用目的によって、相互に関連して決定される。半導体層の好適な膜厚は０．３ｎｍ以上である。また金属層は、１～５０ｎｍが好ましい。１ｎｍ以上とすることで、より一層均一な金属と半導体との化合物が形成され，５０ｎｍ以下とすることで化合物形成時の結晶欠陥の発生を抑えることができる。更に、本発明において、半導体層の不純物濃度は$1\times10^{18}cm^{-3}$以下とするのが好ましく、この範囲で生成する化合物の抵抗は、一層小さいものとすることができる。半導体層の不純物濃度がこれ以上高くなると、大気に曝したときに表面が酸化され易くなるからである。

【００３０】本発明の熱処理は、１００℃以上が好ましく、３００～５００℃がより好ましい。この範囲で、低抵抗でコンタクト抵抗の小さな金属と半導体との化合物が形成される。

【００３１】また、本発明においては、基体上に金属層、半導体層を大気に曝さずに連続して形成後、続いて熱処理して前記金属層と前記半導体層を反応させて金属と半導体との化合物を形成し、その後未反応の金属層をエッチングして取り除き、金属と半導体との化合物を所定の形状に形成することにより、従来微細パターンの形成が困難であった高融点金属またはその化合物（シリサイド等）等を精確に微細にパターニングすることが可能となる。

【００３２】

【実施例】以下に、実施例を挙げて本発明をより詳細に説明する。

【００３３】（実施例１）以下、本発明の第１の実施例を、第１図を用いて説明する。図１（ａ）～（ｃ）は、n^+-Ｓｉ上へのＴａシリサイドによるオーミックコンタクト電極を形成する工程を示す断面図である。１０１は例えばｐ型シリコンウェハであり、抵抗率は例えば０．３～１．０Ω・ｃｍである。ウェハは目的によってはｎ型を用いても構わない。ウェハの表面には絶縁膜として例えばSiO_2 １０２が厚さ約５００ｎｍ程度形成されている。ウェハの表面には、一部にｎ型の不純物濃度が例えば$1\sim2\times10^{20}cm^{-3}$である$n^+$ 高濃度層１０３が形成されており、その高濃度層１０３内の領域の一部が外部と電気的に導通がとれるようにSiO_2 １０２に開口部１０４が設けられている。その上には、電極材料層１０５（例えばＴａ層）が厚さ約5～５０ｎｍ程度形成されている。さらにＴａ層１０５の上には、抵抗率が例えば０．０１～１０ｋΩ・ｃｍ程度の不純物を極めて

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低濃度（1×10^{12}～$1\times10^{15}cm^{-3}$）に含むＳｉ層１０６が厚さ約２～３０ｎｍ程度形成されている。Ｔａ層とＳｉ層は高真空対応の薄膜形成装置を用いて、一切大気に曝すこと無く連続して形成されている。連続成膜が必要な理由は、金属は大気に曝されると瞬時に表面が２～５ｎｍ酸化されるからである。Ｔａ上に特にノンドープのＳｉを成膜すると、大気に曝しても１時間程度は酸化されない。勿論、目的や条件に応じて、Ｔａ以外の金属を用いても良いし、層の厚さも自由に選ぶことが可能であることは言うまでもない。Ｓｉ層に関しても、目的や条件に応じて層の厚さも自由に選ぶことが可能である（ここまで、図１（ａ）参照）。Ｔａは、ｎ－Ｓｉ、ｐ－Ｓｉに対しショットキ・バリア・ハイトが０．５６ｅＶ、０．５８ｅＶと殆ど等しいため、n^+－Ｓｉ、p^+－Ｓｉにそれぞれ極めて低い接触抵抗が実現される。Ｔｉも同様な特性をもつ金属である。

【００３４】この構造を有するウェハに対して、イオン注入を行った。注入するイオン種としてはウェハ上の高濃度層１０３と同型となる不純物、例えば、Ａｓイオンを注入する。これは、ＰでもよいしＳｂでも良いが、結晶構造の整合性を考慮すると高濃度層１０３中の不純物と同一元素であることが望ましい。注入ドーズ量としては、例えば$2\times10^{15}cm^{-2}$とし、イオンの加速エネルギーとしては例えば７５ｋｅＶとした。

【００３５】本実施例では、シリサイドとＳｉ半導体界面で不純物濃度を最大としコンタクト抵抗を一層低下させるためにＡｓイオンを用いたが、単にイオンミキシングする事が目的の場合においては、他のイオン（例えばＴａ、Ｓｉ等）を用いても良い。

【００３６】イオン注入後熱処理を行い、シリサイド層（$TaSi_2$）１０７の形成及びイオン注入層の再結晶化を行った。熱処理の方法としては、電気炉を用い、Ａｒガスを２ｌ／ｍｉｎ流しながら、９００℃、１時間のアニール処理を行った。熱処理方法は、ランプ加熱でも良いし、その他の方法でも良い。温度も９００℃に限らず、４００～５００℃で十分可能である。ガスに関しても、Ａｒに限らず、目的や条件に応じてH_2、N_2、Ｈｅ、等のガス、あるいはこれらの混合ガスを用いても構わないし、流量に関してもここに記した条件以外でも、ガスの清浄性が保証されるならば問題とはならない。あるいはプロセスの整合性を考慮して真空中にて熱処理を行うことがより効果的な場合もある。温度や処理時間に関しても、目的、条件に応じて最適な条件を用いれば良いことは言うまでもない。その後、高純度不活性ガス雰囲気内、例えば、N_2雰囲気において、最表面に残っている未反応のＳｉ層をエッチング液（例えばフッ酸と硝酸の混合水溶液）により除去し、シリサイド層を露出させた。Ｓｉ除去はCl_2ガス雰囲気下でＣｌラジカルを発生させても良い。これは、Ｓｉ層の残留の心配を完全に取り除くため為に行った処理であり、もし、Ｓｉ層がすべてシリサイド化されていれば、ここで述べた様なエッチング処理は行わなくともよい（ここまで図１（ｂ）参照）。

【００３７】更に、表面に露出しているシリサイド層を超高純度のN_2雰囲気において搬送し、超高真空スパッタリング成膜装置を用いて電極材料を形成した。本実施例においては、例えばＴａ層１０８を厚さ５００ｎｍ程度形成した。Ｔａ層１０８及びシリサイド層１０７にパターニングを施し、引き出し電極を形成した。言うまでもなく、引き出し電極としてはＴａ以外の電極材料を用いても構わないし、膜厚もここに記す以外の厚さでも一向に構わない（図１（ｃ）参照）。

【００３８】図２に、本発明の製作工程により形成された$TaSi_2$／n^+-Ｓｉコンタクトのコンタクト抵抗の測定結果を示す。従来例（図１１）に比べて、抵抗値及びそのばらつきの幅ともに低減されていることが分かる。図３には、本実施例の製作工程により形成された$TaSi_2$／n^+-Ｓｉ接合について、深さ方向の不純物濃度分布を２次イオン質量分析（ＳＩＭＳ）により測定した結果を示す。酸素に関しては、表面以外では測定限界値以下となっている。表面に酸素が確認されているのは、ＳＩＭＳ装置に搬入し測定を開始するまでの間に表面に形成された酸化膜によるものである。

【００３９】この結果から、本発明の方法により、電極と半導体の接合部形成において徹底的に酸素の混入を防ぐことが可能となり、この様な汚染物質の混入の低減が、半導体装置の電極形成工程において、抵抗値の低減に非常に効果的であることが容易に理解できる。

【００４０】また、この図からシリサイド界面近傍においてＡｓの濃度が高い値となっていることも分かる。

【００４１】本実施例では、ｎ型高濃度Ｓｉ層上への電極形成に関しての実施例を示したが、ｐ型高濃度Ｓｉ層上への電極形成に関しても同様である。但し、その場合には、高濃度層１０３は、ｐ型の高濃度不純物層が形成されている。また、注入するイオン種としてはウェハ上の高濃度層１０３と同型となる不純物（例えば、B^+イオンやBF_2^+イオン）が注入される。例えば、Ｂイオンを用いる場合には、イオンのエネルギは１６～２５ＫｅＶとなる。あるいは、その他のイオン（例えば、Ｓｉ、Ｔａ等）で良い場合もある。

【００４２】この様に本発明を用いれば、例えば、半導体装置における電極材料層と半導体とのコンタクト抵抗のさらなる低減が達成できる。その結果、ＵＬＳＩの高性能化を一段と押し進めることが可能となる。

【００４３】（実施例２）本発明の第２の実施例を図４を用いて説明する。本実施例では、金属層上に形成された半導体層を透過させてイオンを注入する事により、イオンミキシングのためのイオン注入と半導体高濃度層形成のためのイオン注入を同時に行った。図４（ａ）は、実施例１のウェハとは、高濃度層１０３が形成されてい

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ないことを除けば、同条件を満たしている。

【００４４】図４（ａ）の構造を有するウェハに対して、イオン注入を行った。注入するイオン種として、ｎ型のドーパントとなるＡｓイオンを注入した。これは、Ｐでもよいし Ｓｂでも良い。注入ドーズ量としては、例えば$2\times10^{15}cm^{-2}$とし、イオンの加速エネルギーとしては例えば７５ｋｅＶとした。

【００４５】イオン注入後、熱処理を行いシリサイド層（$TaSi_2$）４０７の形成及びイオン注入層の再結晶化を行った。熱処理の方法では、電気炉を用い、Ａｒガスを２１／ｍｉｎ流して、５００℃、１時間のアニール処理を行った（図４（ｂ）参照）。熱処理方法・条件に関しては実施例１と同じ条件である。

【００４６】その後、高純度不活性ガス雰囲気内、例えばＡｒ雰囲気において、最表面に残っている未反応のＳｉ層をフッ酸と硝酸の混合水溶液等のエッチング液により除去し、シリサイド層を露出させた。更に、大気に曝すこと無く、その上に電極材料として、例えばＴａ層４０８を厚さ５００ｎｍ程度形成した。Ｔａ層４０８及びシリサイド層４０７に対してパターニングを施し、引き出し電極を形成した（図４（ｃ）参照）。言うまでもなく、Ｔａ以外の電極材料を用いても構わないし、膜厚もここに記した以外の厚さでも良い。

【００４７】図５に、以上の製作工程により形成された$TaSi_2$を電極として有するn^+Si/pSi構造を有するｐｎダイオードの電流－電圧特性の測定結果を示す。図５が示すように、良好なダイオード特性が得られていることが分かる。この結果は、実施例１でも述べているとおり、接合形成時に酸素などの汚染物質の混入が徹底的に低減されていることに起因しており、本発明による接合形成方法の効果によるものである。

【００４８】本実施例では、ｎ型高濃度Ｓｉ層の形成と電極形成とに関する実施例を示したが、ｐ型高濃度Ｓｉ層の形成と電極形成に関しても同様である。但し、その場合には、注入するイオン種としては、ｐ型のドーパントとなるイオン（例えばＢイオン）を用いる。

【００４９】（実施例３）図６を用いて、非常に浅い接合を有するシリサイド・シリコン接合形成に関する本発明の第３の実施例を説明する。

【００５０】６０１はウェハ表面のｐ型のシリコンである。Ｓｉ層６０１はウェハ上に形成されたシリコン層でも良いし、シリコンウェハそのものでも良い。また、Ｓｉ層６０１の表面は何箇所かが絶縁層や金属層で覆われていても良いし、Ｓｉ層６０１の何箇所かに不純物が添加されている拡散層が形成されていても良い。Ｓｉ層の抵抗率は例えば０．３～１．０Ω・ｃｍである。Ｓｉ層６０１は、目的によりｎ型を用いても構わない。また、抵抗率は目的や条件によっては、ここに記す範囲に限らずとも良い。Ｓｉ層６０１上には、絶縁膜として例えばSiO_2 ６０２が厚さ約５００ｎｍ程度形成されている。SiO_2 ６０２に開口部６０３が少なくとも１ヶ所設けられている。その上には、シリコンと反応しシリサイドを生成する金属、例えばＴａ層６０４が厚さ約１０ｎｍ程度形成されている。厚さに関しては、この値より薄くても厚くても構わないが、シリサイド層を均一に形成すること、あるいはシリサイド形成時の体積変化に伴う欠陥発生を極力防ぐことを考慮すると、１０ｎｍ程度の膜厚にすることが最適である。さらにその上には、抵抗率が例えば０．０１～１０ｋΩ・ｃｍ程度の極めて低濃度な不純物を含むＳｉ層６０５が厚さ約３０ｎｍ程度形成されている。Ｓｉ層６０５の厚さは、３０ｎｍに限らずとも良いが、Ｔａ層６０４の表面を完全にＳｉ層６０５で覆うことや、Ｔａ層６０４全体を完全にシリサイド化させることを考慮すると、２５ｎｍ程度以上であれば問題ない（図６（ａ）参照）。

【００５１】熱処理を行い、シリサイド層（$TaSi_2$）６０６の形成を行った。熱処理の方法としては、電気炉を用い、Ａｒガスを２１／ｍｉｎ流し、７００℃、１時間のアニール処理を行った。熱処理方法は、ランプ加熱でも良いし、その他の方法でも良い。ガスに関しては、Ａｒに限らず、目的や条件に応じてH_2、N_2 、Ｈｅ、等といった他のガス、あるいは、これらの混合ガスを用いても構わないし、流量に関してもここに記す条件以外でも、ガスの清浄性が保証されるならば問題とはならない。また、あるいは真空中にて熱処理を行うことがより効果的な場合もある。温度や処理時間に関しても、目的、条件に応じて最適な条件を用いれば良いことは言うまでもない。

【００５２】シリサイド形成後、シリサイド層の反応前の初期のシリコンの最表面に対する接合の深さx_jを測定したところ１２ｎｍであった（図６（ｂ）参照）。なお、Ｓｉ層６０５を形成せずに行う従来の方法で形成されたシリサイド層に関して同様の測定を行ったところ、接合の深さは２２ｎｍであった。

【００５３】この結果から、本発明のシリサイド形成方法を用いることにより従来方法と比較して、接合深さを約５０％の値にまで浅くすることに成功していることが分かる。高性能・高集積化半導体素子の製造のためには、接合の徹底的な極浅化が必要不可欠である。この要求に対して、本発明によるシリサイド電極形成方法が非常に効果的であることは、本実施例から明らかである。

【００５４】（実施例４）図７は、本発明の第４の実施例である多層配線構造形成の為の製作工程を示す断面図である。

【００５５】７０１はウェハ表面の半導体である。ここでは、例としてｐ型シリコン層を用いた。Ｓｉ層７０１はウェハ上に形成されたシリコン層でも良いし、シリコンウェハそのものでも良い。また、Ｓｉ層７０１の表面は何箇所かが絶縁層や金属層で覆われていても良いし、Ｓｉ層７０１の何箇所かに不純物が添加されている拡散

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層が形成されていても良い。Ｓｉ層の抵抗率は例えば０．３～１．０Ω・ｃｍである。目的によってはｎ型を用いても構わない。また、抵抗率は目的や条件によっては、ここに記す範囲に限らずとも良い。Ｓｉ層７０１上には、絶縁膜層として例えばSiO_2層７０２が形成されており、SiO_2層７０２の一部はＳｉ層７０１を露出するための開口部７０３が少なくとも１箇所以上形成されている。開口部７０３を覆うように金属層（ここでは例えばＴｉ層）７０４が１０ｎｍ程度の厚さ形成されている。厚さに関しては、この値より薄くても厚くても構わないが、シリサイド層を均一に形成すること、あるいは、シリサイド形成時に極力結晶欠陥の発生を防ぐことを考慮すると、１０ｎｍ程度の膜厚にすることが最適である。さらにその上には、抵抗率が例えば０．０１～１０kΩ・ｃｍ程度の極めて低濃度な不純物を含むＳｉ層７０５が厚さ約１８ｎｍ程度形成されている。Ｓｉ層７０５の厚さは、１８ｎｍに限らずとも良いが、Ｔｉ層７０４の表面を完全にＳｉ層７０５で覆うことや、熱処理後において、金属と未反応のＳｉ層を最低１原子層以上を残し、かつ未反応のＳｉ層の厚さが余り厚すぎないようにすることを考慮して決めれば良い。ここでは、Ｔｉ層７０４よりも厚い値として例えば１８ｎｍ程度とした。その後、Ｔｉ層７０４とＳｉ層７０５に対して、適当な形状にパターニングを施した（ここまで図７（ａ）を参照）。

【００５６】その後、熱処理を施した。熱処理の方法としては、電気炉を用い、Ａｒガスを２１／ｍｉｎ流し、７００℃、１時間のアニール処理を行った。熱処理方法は、ランプ加熱でも良いし、その他の方法でも良い。ガスに関しては、Ａｒに限らず、目的や条件に応じてH_2、N_2、Ｈｅ、等といった他のガス、あるいは、これらの混合ガスを用いても構わないし、流量に関してもここに記す条件以外でも問題とはならない。また、あるいは真空中にて熱処理を行うことがより効果的な場合もある。温度や処理時間に関しても、目的、条件に応じて最適な条件を用いれば良いことは言うまでもない。この熱処理によりＴｉとＳｉが反応しチタンシリサイド（$TiSi_2$）７０６が２５ｎｍ程度の厚さで形成された。Ｓｉ層７０１に対するチタンシリサイド層の接合深さは約１２．５ｎｍ程度であり、接合の極浅化が図られている。また未反応のＳｉ層７０５の膜厚は約５．５ｎｍ程度であった（ここまで図７（ｂ）参照）。

【００５７】次に、配線間の電気的絶縁を行うために層間絶縁層として例えばSiO_2層７０７を化学的気相成長法（ＣＶＤ）法を用いて、厚さ５００ｎｍ～１μｍ程度形成した。層間絶縁層７０７の一部にはシリサイド層７０６上の未反応のＳｉ層７０５を露出するための開口部７０８がフォトリソ工程後の層間絶縁膜のリアクティブイオンエッチングにより少なくとも１箇所以上設けられている（ここまで図７（ｃ）参照）。

【００５８】次に、オゾンを数ｐｐｍ含む超純水で開口部７０８を十分洗浄した後、０．５～１％希フッ酸水溶液を用いてＳｉ層７０５表面上の酸化膜の除去を行った。続いて、開口部７０８を覆うように金属層７０９、例えばＴｉ層を厚さ５００ｎｍ程度形成した。金属層７０９は、シリコンと安定に反応しシリサイド化合物を形成する金属ならばＴａやＰｔ等の他の金属でも良い。また、その膜厚に関しても開口部７０８に露出しているＳｉ層７０５と完全に反応し、金属層７０９とシリサイド層７０６のコンタクト部が全体に亘りシリサイド化されるような膜厚とすれば良い。洗浄方法は、開口部７０８に対する洗浄効果が十分あり、且つ開口部７０８に露出しているＳｉ層が完全に消失してしまわないこと、及びＳｉ層表面に何らかの不動態膜を残すこと無しに開口部７０８に露出しているＳｉ表面を超清浄な状態に保てること、という条件を満たせば本実施例で用いた方法に限る必要はない。（図７（ｄ）参照）。

【００５９】その後に、熱処理を施し、新たにシリサイド層７１０を形成した。熱処理の方法は、本実施例中において既に記した条件と同様である。最後に、Ｔｉ層７１１に対して、少なくとも１ヶ所以上任意の形状にパターニングを行い配線構造を作製した（図７（ｅ）参照）。

【００６０】本実施例の多層配線構造形成方法により、金属配線同士のコンタクト部形成においても、金属表面をシリコンで覆い隠すことにより金属表面の酸化を防ぎ、金属層の界面における酸素の混入を徹底的に抑制する事に成功した。更に、コンタクト部への金属配線形成直前の開口部の洗浄において、金属表面をＳｉで覆うという方法を用いることで、金属表面が露出しているコンタクト開口部に対しては用いることができなかった酸性溶液を用いて洗浄することが可能となり、コンタクト界面の超清浄化の達成に成功し、金属配線同士のコンタクト部の信頼性の向上を可能とした。さらに、従来は金属表面上に直接接触する形で層間絶縁膜、主としてSiO_2を形成していたため、金属表面の酸化による電気抵抗やエレクトロマイグレーション耐性等の電気的特性が劣化する問題、あるいは金属と酸化膜との密着性の悪さの問題等があったが、本実施例の方法では、シリサイド層上にシリコン層を残した状態で絶縁膜を形成するため金属表面は酸化されず、また、シリサイド上にしっかりと残っているシリコン層上にSiO_2を形成しているため密着性も改善された。この例では、多層金属配線間のコンタクト抵抗を減少させることを目的としている。図７では、Ｓｉ層７０５上に形成する金属層７０９をＴｉで且つ全表面に形成する例を記述したが、表面平坦化を目的としてWF_6とSiH_4ガスを用いたタングステン（Ｗ）の選択成膜を開口部７０８のＳｉ層上にだけ行い、Ｓｉ層７０５との反応でWSi_2を形成すれば極めて有効である。

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【００６１】超高速のマイクロプロセッサ等においては、金属の多層配線が多用される。金属表面は大気に曝すと瞬時に表面が酸化され２～５ｎｍ程度の酸化膜が形成される。このため、金属・金属の接触抵抗は必然的に大きくならざるを得ずマイクロプロセッサの高速特性を劣化させたり、論理振幅を小さくしてしまう。金属表面の酸化を防ぐには、図１４のような工程が有効である。ここで、コンタクトホールの選択的穴埋めにWF_6，SiH_4を用いたWの選択成長を用いる例について説明する。

【００６２】層間絶縁膜１４０１上に第１層目のＡｌ金属配線（０．５～１μｍ程度）１４０２、ノンドープＳｉ層（５～１０ｎｍ程度）１４０３を連続成膜する。層間絶縁膜１４０４は、クラスタツールにより連続成膜した方が望ましいが、ノンドープＳｉ１４０３が酸化されにくいことから表面を水素終端した後、大気中を搬送して成膜しても良い。その後フォトリソ工程により所定のパターンに従って、層間絶縁膜１４０４に穴開けを行う。この時に、現状では大気に曝されるが、ノンドープＳｉの存在によりＡｌ合金表面は酸化されない。

【００６３】ノンドープＳｉにだけ、WF_6＋SiH_4系選択ＣＶＤ（１８０℃程度）により、Ｗ１４０５を選択的にコンタクトホール部に形成し、４００～４５０℃の熱処理によりノンドープＳｉ１４０３を全てWと反応させWSi_2に変える。このようにして、WとＡｌ合金の内にWSi_2が介在する形で、いっさい酸化膜を介在させないWとＡｌ合金の接触が実現される。

【００６４】更に、Ｗ１４０５上のＡｌ合金１４０６との接触にも酸化膜が存在しないようにすることで、多層配線構造における全ての接触部分で、酸化膜が介在しない接触を実現できる。クラスタツール等を用いて大気に曝すことなくＡｌ合金薄膜１４０６形成を行える場合には、図１４に示したように、形成したＷ１４０５の表面に直接Ａｌ合金薄膜１４０６を形成することで、酸素の混入の少ない界面を形成できる。ここで、Ｗ，Ａｌ合金の代わりに、Ｔａ，Ｔｉ，Ｃｕ，Ａｌ，Ａｇ等の金属またはこれらの合金であってもかまわない。また、この手法は多層配線構造のどの層に用いても良い。

【００６５】クラスタツールなどの装置を使わない場合でも、図１５のようにＷ１４０５上にノンドープＳｉ層１４０８を形成することで、界面に酸化膜の存在しない多層配線構造を実現できる。即ち、ノンドープＳｉ形成後大気中を搬送してＡｌ合金薄膜１４０６を形成することにより、ノンドープＳｉが酸化され難いことから、配線間に酸化膜のない界面を作製できる。また、更に耐酸化性を高めるため、ノンドープＳｉ形成後その表面を水素終端しても良い。

【００６６】ノンドープＳｉ１４０８の形成は、例えばＷ１４０５形成用ＣＶＤ装置を用い連続して行うことが可能である。即ち、WF_6とSiH_4ガスを用いてＷ１４０５を形成し、続いてWF_6ガスを止めSiH_4ガスだけを用いてノンドープＳｉ１４０８を形成すれば良い。Ａｌ合金薄膜１４０６を加工した後、絶縁膜１４０４上に残るノンドープＳｉは通常除去されるが、高抵抗なため除去する必要がない場合もある。一方、ノンドープＳｉ１４０８の形成をＷ１４０５上のみに選択的に行うことも可能であり、この場合は、Ａｌ合金薄膜１４０６を加工した後に図１６のような構造になり、絶縁膜１４０４上にはノンドープＳｉは形成されない。また、この場合も、上記したように、ノンドープＳｉ１４０８とＷ１４０５の形成を同じＣＶＤ装置内で連続して行うことができる。

【００６７】２層目のＡｌ合金薄膜１４０６には、ノンドープＳｉ薄膜１４０７が連続成膜されている。このようにＡｌ合金薄膜上にノンドープＳｉを成膜しておけば、特にノンドープＳｉ表面を水素終端しておけば、WF_6＋SiH_4によるW選択成長が完全に行え、表面平坦化に極めて有効である。ここで、Ａｌ合金が、純ＡｌやＣｕ，Ａｇでも良いことは言うまでもない。

【００６８】（実施例５）図8は、本発明の第５の実施例であるシリサイド形成による半導体と金属のオーミックコンタクト電極・配線構造の製作方法を示す断面図である。

【００６９】８０１は半導体層である。ここでは、例としてｎ型シリコン層を用いた。目的によってはｐ型を用いても構わない。Ｓｉ層８０１はウェハ上に形成されたシリコン層でも良いし、シリコンウェハそのものでも良い。また、Ｓｉ層８０１の表面は何箇所かが絶縁層や金属層で覆われていても良いし、Ｓｉ層８０１の何箇所かに不純物が添加されている拡散層が形成されていても良い。Ｓｉ層の抵抗率は例えば０．３～１．０Ω・ｃｍである。また、抵抗率は目的や条件によっては、ここに記す範囲に限らずとも良い。

【００７０】Ｓｉ層８０１上には、絶縁膜層として例えばSiO_2 層８０２が形成されており、SiO_2 層８０２の一部はＳｉ層８０１を露出するための開口部８０３が少なくとも１箇所以上形成されている。開口部８０３を覆うように金属層、ここでは例えばＴｉ層８０４が１０ｎｍ程度の厚さでほぼウェハ上全面に渡り形成されている。金属層８０４は、シリコンと安定に反応しシリサイド化合物を形成する金属ならばＴａ，ＣｏやW等の他の金属でも良い。

【００７１】但し、その金属をエッチングする溶液が、その金属のシリサイドに対してはエッチング反応が進みにくいこと、つまり、シリサイドのエッチング反応に対する金属のエッチング反応の比を大きくとれるようなエッチング溶液であることが必要とされる。ドライエッチングの場合も同様である。厚さに関しては、この値より薄くても厚くても構わないが、シリサイド層を均一に形成すること、あるいは、シリサイド形成時に極力結晶欠

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陥の発生を防ぐことを考慮すると、５～１０ｎｍ程度の膜厚にすることが最適である。

【００７２】さらにその上には、抵抗率が例えば０．０１～１０ｋΩ・ｃｍ程度の極めて低濃度な不純物を含むＳｉ層８０５が厚さ約８～１３ｎｍ程度形成されており、その一部は、少なくとも１ヶ所以上任意形状にパターニングが施されている。Ｓｉ層８０５の厚さは、８～１３ｎｍに限らずとも良いが、本実施例においては、Ｔｉ層８０４の表面を完全にＳｉ層８０５で覆うことや、Ｓｉ層８０５全体をシリサイド化させることを考慮して、例えば８～１３ｎｍ程度とした（ここまで図８（ａ）参照）。

【００７３】図８（ａ）の構造を有するウェハに対して、イオン注入を行った。注入するイオン種としては、例えば、ｎ型のドーパントとなるＡｓイオンを注入した。これは、Ｐでもよいし Ｓｂでも良い。本実施例においては、オーミックコンタクト電極・配線構造の製作のため、ｎ型のドーパントとなるイオンを注入したが、単にシリサイド化することが目的の場合には、他のイオン（例えばＳｉ、Ｔｉ）でも良い。注入ドーズ量としては、例えば2×10^{15}ｃｍ$^{-2}$とし、イオンの加速エネルギーとしては例えば７５ｋｅＶとした。本実施例においては、シリサイド化反応の促進のためにイオン注入によるミキシングを用いたが、必ずしもイオン注入を行わなくとも良い。

【００７４】イオン注入後、熱処理を行いシリサイド層（$TiSi_2$）の形成及びイオン注入層の再結晶化を行った。熱処理の方法としては、電気炉を用い、Ａｒガスを２１／ｍｉｎ流し、４５０℃、３時間のアニール処理を行った。熱処理方法は、ランプ加熱でも良いし、その他の方法でも良い。ガスに関しては、Ａｒに限らず、目的や条件に応じてH_2、N_2、Ｈｅ、等といった他のガス、あるいは、これらの混合ガスを用いても構わないし、流量に関してもここに記す条件以外でも問題とはならない。

【００７５】また、あるいは真空中にて熱処理を行うことがより効果的な場合もある。温度や処理時間に関しても、目的、条件に応じて最適な条件を用いれば良いことは言うまでもない。この熱処理によりＳｉ層８０５で覆われていた部分近傍のＴｉのみがシリコンと反応し、チタンシリサイド（$TiSi_2$）８０６が１２～２５ｎｍ程度の厚さで形成された。Ｓｉ層８０５で覆われていない他の部分のＴｉは未反応の状態で残った。注入されたＡｓが熱処理によりドーパントとして活性化され、シリサイド層８０６の周囲にはｎ型の高濃度層８０７が形成された（ここまで図８（ｂ）参照）。

【００７６】次に、このウェハをNH_4OHとH_2O_2とH_2Oを５：１：１の体積比で混合した水溶液（２５℃）に浸した。液の混合比は他の比率、例えば４：１：１：でも良い。液温に関しても、２５℃に限らずとも良いが、液温が高すぎるとH_2O_2の分解あるいは蒸発をもたらし、逆に、液温が低すぎると反応速度の低下をまねくため、２５℃程度とした。この水溶液に浸すことにより、未反応のＴｉ層はエッチングされて消失しSiO_2層８０２表面が露出された。一方、$TiSi_2$が形成されている部分はエッチングされずに残り、Ｓｉへのオーミックコンタクト用のチタンシリサイド（$TiSi_2$）電極及びその引き出し配線構造が形成された（図８（ｃ）参照）。本実施例においては、$TiSi_2$に関する方法を示したが、他の金属、例えばＣｏを用いる場合にはシリサイド形成後のエッチングには例えばＨＣｌとH_2O_2とH_2Oとを混合させた水溶液を用いれば良い。

【００７７】超微細構造の形成において、ドライエッチングプロセスによるパターニングが必須である。しかし、ＣｕＳｉのようにドライエッチングが行いにくい場合には、ウェットエッチング法も有効である。即ち、高融点金属上に所定の形状にパターニングされたシリコン層を形成する。ドライエッチングを用いて、シリコンに微細なパターニングを行うことは容易である。次に、熱処理を加え、あるいはイオンミキシングを先行させてもよいが、高融点金属層全体に渡りシリサイド層を形成する。シリコンと接触していた部分の高融点金属のみがシリサイドとなっているため、形成されたシリサイドの幅と予めパターニングされていたシリコン層の幅とはほぼ等しくなる。その後未反応の高融点金属のみを選択的にウェットエッチングすることによりシリサイドのみが残り、電極や配線などの微細構造を所定の形状に作製することが可能となる（図８（ｄ）参照）。

【００７８】（実施例６）図９は、本発明の第６の実施例を示す断面図である。本実施例は、極浅な接合深さを有する半導体層と、半導体と金属との化合物の電極構造とを有し、且つ電極・配線構造を任意の膜厚に形成できるものである。

【００７９】９０１は半導体層である。ここでは、例としてシリコンウェハを用いた。Ｓｉ層９０１の表面は何箇所かが絶縁層や金属層で覆われていても良いし、Ｓｉ層９０１の何箇所かに不純物が添加されている拡散層が形成されていても良い。Ｓｉ層９０１上には、絶縁膜層として例えばSiO_2層９０２が形成されている。ウェハの表面には、一部にｎ型の不純物濃度が例えば$1\sim2\times10^{20}$ｃｍ$^{-3}$であるn^+高濃度層９０３が形成されており、その高濃度層９０３内の領域の一部が外部と電気的に導通がとれるようにSiO_2 ９０２に開口部９０４が少なくとも１ヶ所設けられている。

【００８０】絶縁膜層９０２上には、開口部９０４を覆うようにして、金属層、ここでは例えばＴａ層９０５－１が１０ｎｍ程度の厚さでほぼウェハ上全面に渡り形成されている。金属層９０５－１は、シリコンと安定に反応しシリサイド化合物を形成する金属ならばＴｉ，Ｗ，Ｐｔ等の他の金属でも良い。厚さに関しては、この値よ

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り薄くても厚くても構わないが、シリサイド層を均一に形成すること、あるいは、シリサイド形成時に極力結晶欠陥の発生を防ぐことを考慮すると、５～１０ｎｍ程度の膜厚にすることが最適である。

【００８１】さらにその上には、抵抗率が例えば０．０１～１０ｋΩ・ｃｍ程度の極めて低濃度な不純物を含むＳｉ層９０６－１が厚さ約２２ｎｍ程度形成されている。Ｓｉ層９０６－１の厚さは、２２ｎｍに限らずとも良いが、本実施例においては、Ｔａ層９０５－１の表面を完全にＳｉ層９０６－１で覆うことや、Ｓｉ層９０６－１全体をシリサイド化させることを考慮して、例えば２２ｎｍ程度とした。

【００８２】続いてイオン注入を行った。注入するイオン種としては、例えば、ｎ型のドーパントとなるＡｓイオンを注入した。これは、Ｐでもよいし Ｓｂでも良い。注入ドーズ量としては、例えば2×10^{15}ｃｍ$^{-2}$程度とし、イオンの加速エネルギーとしては例えば７５ｋｅＶとした（ここまで図９（ａ）参照）。

【００８３】Ｓｉ層９０６－１上には、金属層、ここでは例えばＴａ層９０５－２が１０ｎｍ程度の厚さでほぼウェハ上全面にわたり形成されている。金属層９０５－２は、他の金属でもよい場合もあるが、金属層９０５－１と同一材料であることが最適である。厚さに関しては、この値より薄くても厚くても構わないが、シリサイド層を均一に形成すること、あるいはシリサイド形成時に極力結晶欠陥の発生を防ぐことを考慮すると、５～１０ｎｍ程度の膜厚にすることが最適である。さらにその上には、抵抗率が例えば０．０１～１０ｋΩ・ｃｍ程度の極めて低濃度な不純物を含むＳｉ層９０６－２が厚さ約２２ｎｍ程度形成されている。Ｓｉ層９０６－２の厚さは、２２ｎｍに限らずとも良いが、本実施例においては、Ｔａ層９０５－２の表面を完全にＳｉ層９０６－２で覆うことや、Ｓｉ層９０６－２全体をシリサイド化させることを考慮して、例えば２２ｎｍ程度とした（ここまで図９（ｂ）参照）。

【００８４】以降、形成したいシリサイド層の厚みを考慮して、金属層の形成とその金属層上へのシリコン層の形成を任意回数繰り返せばよいが、本実施例においてはさらに２回繰り返し、最終的に金属層とシリコン層との対を例えば４層形成した。Ｔａ層は９０５－３及び９０５－４、Ｓｉ層は９０６－３及び９０６－４である（ここまで図９（ｃ）を参照）。

【００８５】その後熱処理を施した。方法や条件に関しては、実施例１に記した熱処理に関するものと全く同様の条件である。熱処理により、タンタルシリサイド層９０７が厚さにして９６ｎｍ程度形成された。本例においては、金属層とシリコン層の対を４層形成し９６ｎｍとしたが、層の形成回数を制御することにより、比較的自由にシリサイド層の膜厚を制御することができる。また、本実施例においては熱処理を最終的な膜の形成後に１回行ったが、Ｓｉ層９０６－２形成後ならば、熱処理を任意の時点で少なくとも１回以上の任意の回数行ってもよい。また、Ｓｉ層９０６－２形成後ならば、イオン注入は、任意の時点で任意の回数行ってもよい。シリサイド層９０７形成後、任意形状にパターニングを行い電極・配線構造を作製した（ここまで第６図（ｄ）を参照）。

【００８６】この方法により、非常に浅い接合を有するシリサイドとシリコンとのコンタクト電極が形成できた。実施例１においても記したように、コンタクト形成工程の高性能化の結果、その界面におけるドーパント濃度が最大となり、なおかつ、酸素などの汚染が徹底的に低減された結果、非常に低いコンタクト抵抗値を実現できた。

【００８７】また、コンタクト部は、シリサイド形成時の熱ストレスに起因する応力歪み、あるいは格子定数の差により発生する結晶欠陥を抑えるために、金属の膜厚は極力薄いことが望ましい。しかしながら、配線抵抗あるいは断線の問題を考慮すると、シリサイド化によるコンタクト電極と引き出し配線を同時に形成するためには、金属の膜厚は極力厚い方が望ましい。本実施例に示した製造方法を用いれば、結晶欠陥の発生を徹底的に抑えつつ、ある程度の厚みを有するシリサイド層を用いて、コンタクト電極と引き出し配線構造を同時に作製でき、なおかつ、その電気特性も良好であり、その上、コンタクト部において、シリサイド形成により生じるシリコン層への侵入の深さも極浅化も実現できる。従って、本実施例による半導体装置製造方法が、高性能ＵＬＳＩの実現の為に非常に有益であるといえる。

【００８８】

【発明の効果】本発明により、非常に低いコンタクト抵抗を有する金属電極の形成、及び、その接合深さの極浅化の達成が可能となり、超高密度・超高性能・高信頼性ＵＬＳＩの実現が可能となる。

【図面の簡単な説明】

【図１】本発明の第１の実施例を示す概念図であり、シリサイド電極による高濃度シリコンへのオーミックコンタクト電極の製造方法を工程順に示した概念図である。

【図２】実施例１の電極と半導体間のコンタクト抵抗を示すグラフである。

【図３】実施例１の電極構造における深さ方向の不純物濃度分布を示すグラフである。

【図４】本発明の第２の実施例を示す概念図であり、ｐｎ接合ダイオード構造の製造方法を工程順に示した概念図である。

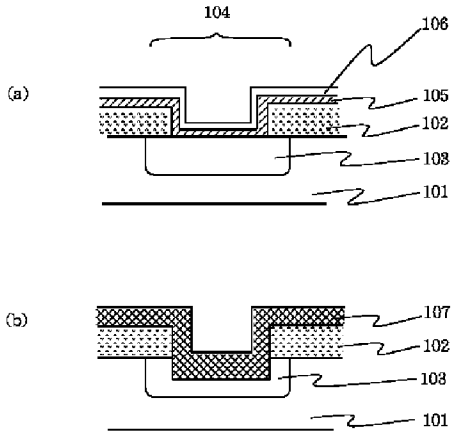
【図５】実施例２のダイオードの電流－電圧特性を示すグラフである。

【図６】本発明の第３の実施例を示す概念図であり、非常に浅い接合を有するシリサイドと半導体との接合構造の製造方法を工程順に示した概念図である。

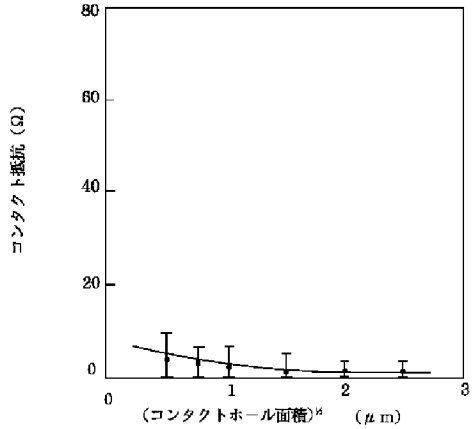
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【図７】本発明の第４の実施例であり、高信頼性を有する多層配線構造の製造方法を工程順に示した概念図である。
【図８】本発明の第５の実施例を示す概念図であり、シリサイド形成による電極・配線形状の製造方法を工程順に示した概念図である。
【図９】本発明の第６の実施例を示す概念図であり、シリサイドとシリコンとの接合深さが極浅で、且つ高信頼性シリサイド電極・配線構造の製造方法を工程順に示した概念図である。
【図１０】先行技術の電極と半導体間のコンタクトを示す概念図である。
【図１１】先行技術の電極と半導体間のコンタクト抵抗を示すグラフである。
【図１２】先行技術の電極構造における深さ方向の不純物濃度分布を示すグラフである。
【図１３】先行技術において、シリサイド・シリコン接合面の深さを示す概念図である。
【図１４】本発明の多層配線構造の他の例を示す概念図である。
【図１５】本発明の多層配線構造の他の例を示す概念図である。
【図１６】本発明の多層配線構造の他の例を示す概念図である。
【符号の説明】
１０１　半導体、
１０２　絶縁層、
１０３　高濃度半導体層、
１０４　開口部、
１０５　金属層、
１０６　半導体層、
１０７　半導体と金属との化合物層、
１０８　金属層、
４０３　高濃度半導体層、
４０７　半導体と金属との化合物層、
４０８　金属層、
６０１　半導体、
６０２　絶縁層、
６０３　開口部、
６０４　金属層、
６０５　半導体層、
６０６　半導体と金属との化合物層、
x_j　接合深さ、
７０１　半導体、
７０２　絶縁層、
７０３　開口部、
７０４　金属層、
７０５　半導体層、
７０６　半導体と金属との化合物層、
７０７　絶縁層、
７０８　開口部、
７０９　金属層、
７１０　半導体と金属との化合物層、
７１１　金属層、
８０１　半導体、
８０２　絶縁層、
８０３　開口部、
８０４　金属層、
８０５　半導体層、
８０６　半導体と金属との化合物層、
９０１　半導体、
９０２　絶縁層、
９０３　高濃度半導体層、
９０４　開口部、
９０５－１，－２，－３，－４　金属層、
９０６－１，－２，－３，－４　半導体層、
９０７　半導体と金属との化合物層、
１００１　半導体、
１００２　絶縁層、
１００３　高濃度半導体層、
１００４　開口部、
１００５　金属層、
１００６　半導体と金属との化合物層、
１００７　金属層、
１４０１，１４０４　層間絶縁膜、
１４０２　第１のＡｌ合金配線、
１４０３，１４０７，１４０８　ノンドープＳｉ層、
１４０５　選択成長タングステン（Ｗ）、
１４０６　第２のＡｌ合金配線。

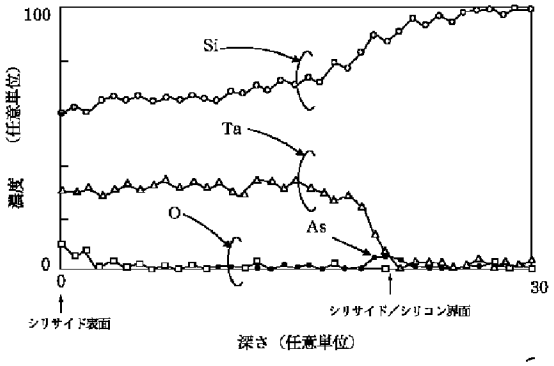
【図１】



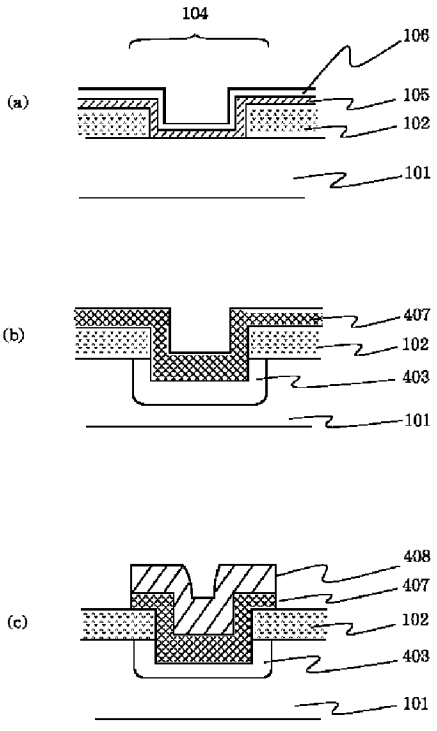
【図２】



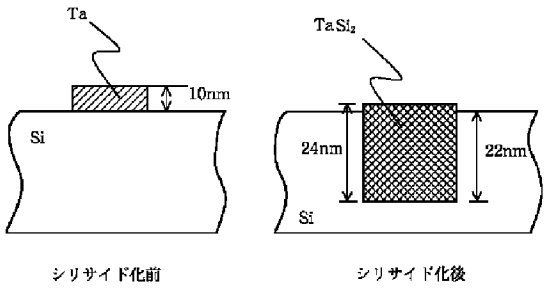
【図３】



【図４】

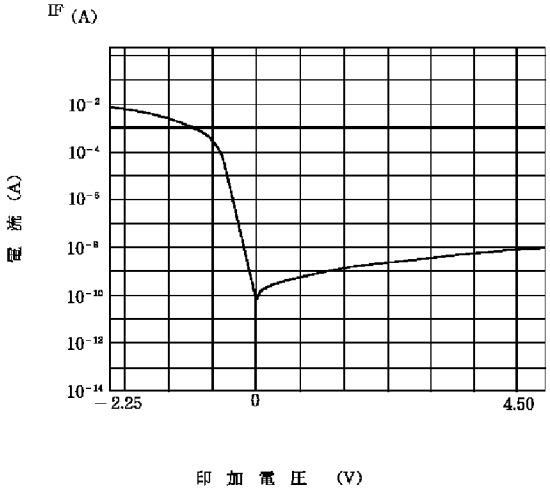


【図１３】

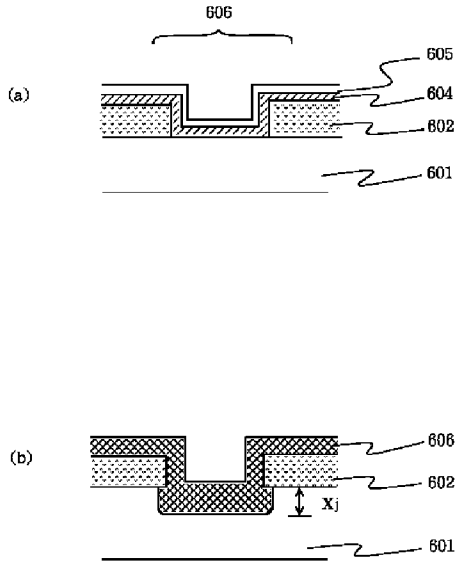


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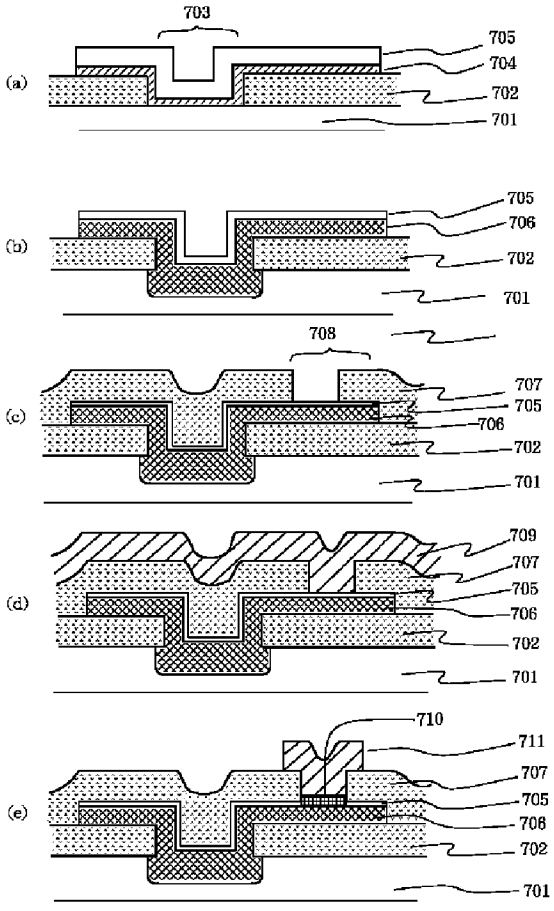
【図5】



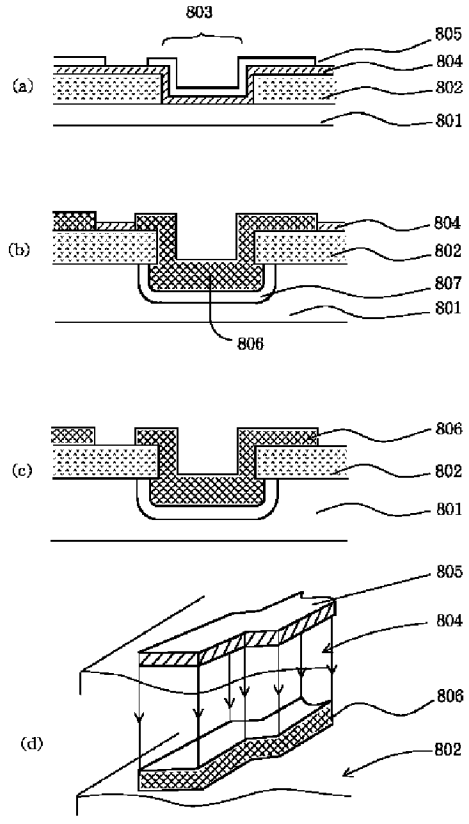
【図6】



【図7】

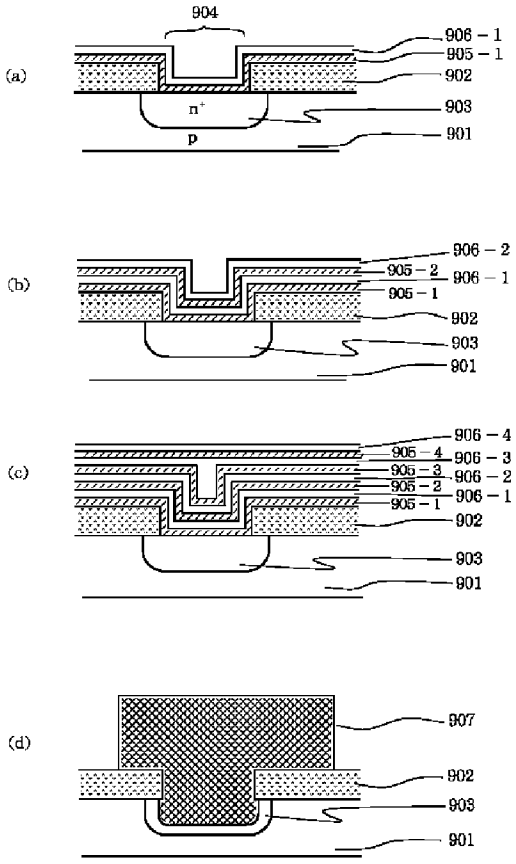


【図8】

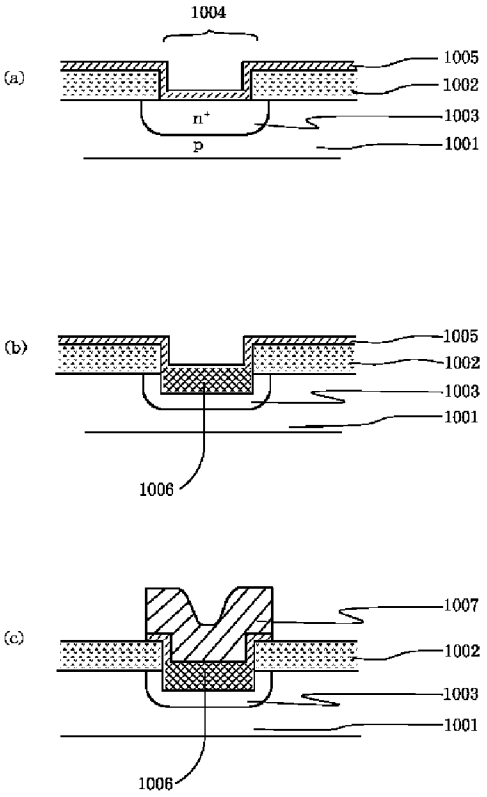


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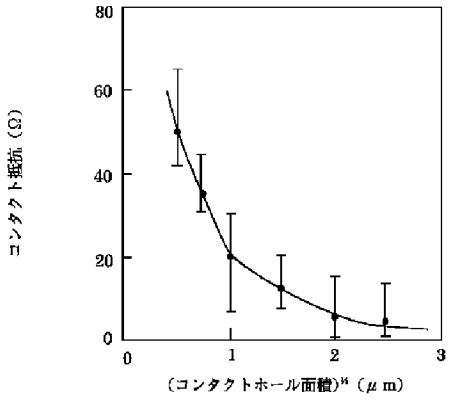
【図９】



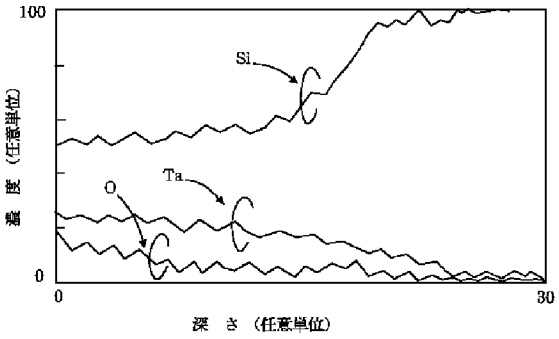
【図１０】



【図１１】

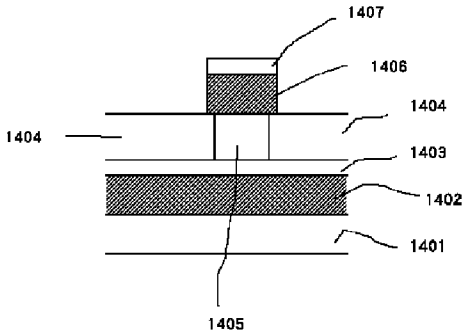


【図１２】

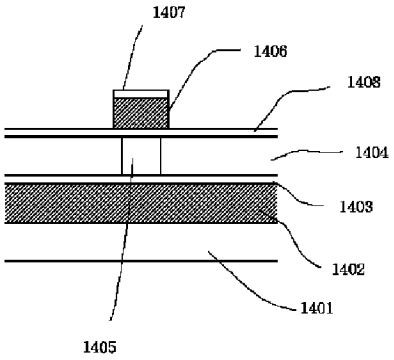


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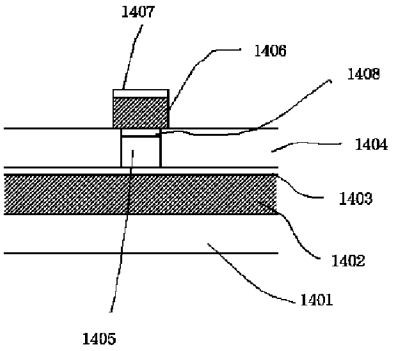
【図１４】



【図１５】



【図１６】



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JPH07122519A SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Applicants: OMI TADAHIRO

Inventors: OMI TADAHIRO,YAMADA KEIICHI

Classifications:

IPC ***H01L21/28; H01L21/285; H01L21/768; H01L23/522;*** (IPC1-7): H01L21/768; H01L21/28;

CPC **H01L21/28518 (EP); H01L21/76889 (EP);** H01L2924/0002 (EP);

C-sets **H01L2924/0002, H01L2924/00 (EP);**

Priorities: JP20674193A 1993-08-20; JP21888993A 1993-09-02; JP29078693A 1993-11-19

Application: JPH07122519A·1993-11-19

Publication: JPH07122519A·1995-05-12

Published as: **EP0715343A1; EP0715343A4;** JPH07122519A;**JP3688727B2; WO9506329A1**

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Abstract

PURPOSE:To reduce the contact resistance between an electrode part and a semiconductor layer by continuously forming one-layer metal layer and a semiconductor layer on one part of a semiconductor surface without exposing to atmosphere, causing the metal layer to react with the semiconductor, and forming the compound of the metal layer and the semiconductor. CONSTITUTION:An opening 104 is provided at SiO2 102 which is formed on the surface of a wafer 101 and Ta layer 105 and Si layer 106 are formed on it but the Ta layer 105 and Si layer 106 are formed continuously without exposing to atmosphere using a thin-film forming device for a high vacuum. Then, after an impurity ion which is of the same type as a high-density layer 103, heat treatment is performed and silicide layer 107 is formed and an ion implantation layer is recrystallized. Further, Ta layer 108 is formed on the silicide layer 107, the Ta layer 108 and the silicide layer 107 are subjected to patterning, and then an extraction electrode is formed, thus forming a metal electrode with an extremely low contact resistance.

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DESCRIPTION JPH07122519

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a method of manufacturing a semiconductor device, and more particularly to a semiconductor device suitable for an ultra high density integrated circuit (ULSI) and a method of manufacturing the same.

[0002]
[Related Art] Currently, the degree of integration of ULSI continues to increase at a remarkable rate, and the size of the device is 0.1 μm. Further, it is actively aimed at the realization of a device with an ultra-fine size that exceeds that. Research and development is in progress.

[0003]

With the high integration of devices, the wiring structure has become more complicated and multilayered.

Along with this, the number of contact portions for connecting wires to each other and for connecting metal wires to a semiconductor has explosively increased, and further miniaturization has been promoted with respect to the size thereof. High reliability and high performance of various contacts existing in ULSI are one of the important development items that are the key to realize high reliability and high performance of ULSI.

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[0004]

In order to achieve high reliability and high performance of the contact part between metal and semiconductor, low contact resistance is indispensable, and in order to realize it, formation of ultra-clean contact interface is indispensable. .. The reason is that the presence of an insulating layer (such as an oxide film) that hinders electrical conduction at the contact interface causes an increase in contact resistance and a variation in contact resistance value.

[0005]

However, it is extremely difficult to obtain a super-clean contact interface whether it is a contact for connecting metal wirings or a metal-semiconductor contact for forming an ohmic contact electrode of a semiconductor element. It's difficult. The reason is that in order to form a contact, the electrode material must be formed on a surface of a material that is very easily oxidized, such as a metal surface or a surface where impurities are added to a semiconductor at a high concentration. This is because an oxide film is likely to remain on the formed interface. For example, if it is a metal surface, an oxide film of 2 to 5 nm is formed only by exposing it to the atmosphere for a few seconds, and if it is an n + -Si surface, it is 0.5 to 5 1 nm of SiO2 is formed. From this, it can be easily understood how difficult it is to stably realize a contact interface without an oxide film in forming a contact structure of a semiconductor element. Therefore, in the ULSI manufacturing technology, the establishment of the technology for forming the contact interface between the ultra-clean metal and the semiconductor plays a great role.

[0006]

Conventionally, in forming a contact, a heat treatment after forming a contact electrode material has been performed as a solution to the above-mentioned contamination existing on the interface, in particular, growth of an oxide film. In forming a junction between metal and silicon, a technique has been developed in which silicide of a refractory metal is formed to reduce contact resistance. After forming the refractory metal thin film on silicon, heat treatment is performed to form a silicide compound, and the interface between the silicide and silicon is brought to a position deeper than the position of the interface immediately after the contact is formed. It becomes possible to obtain the interface with. Furthermore, a silicide formation technique using ion beam mixing has been developed for the purpose of forming a stable silicide

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or reducing the silicidation temperature. This is a technique in which a refractory metal is formed on silicon, ions are implanted from above, and then heat treatment is performed to form silicide.

[0007]
However, these methods of forming a contact between a metal and a semiconductor by forming silicide have some problems to be solved.

[0008]

Here, taking the case of forming a Ta silicide electrode on n + -Si as an example, the problems associated with the prior art will be described with reference to FIGS.

FIG. 10 is a sectional view showing a step of forming a Ta silicide electrode on n + -Si. In FIG. 10A, 1001 is a p-type silicon wafer, and the resistivity is 0.3 to 1.0 Ω · cm. SiO2 1002 is formed as an insulating film on the surface of the wafer to a thickness of about 500 nm. An n + high-concentration layer 1003 having an n-type impurity concentration of 2 × 10 20 cm −3 is partially formed on the surface of the wafer, and a part of the region in the high-concentration layer 1003 is electrically connected to the outside. At least one opening 1004 is provided in the SiO2 1002 so that electrical continuity can be obtained. A Ta layer 1005 is formed thereon with a thickness of about 10 nm. A wafer having this structure is heat-treated to form a silicide layer (TaSi2) 1006 (see FIG. 10B). As the heat treatment method, an electric furnace was used, and an annealing treatment was performed at 900 ° C. for 1 hour at an Ar gas flow rate of 2 l / min. A Ta layer 1007 having a thickness of about 500 nm was formed thereon as a lead wiring material, and then patterned (see FIG. 10C).

[0009]

FIG. 11 shows the measurement result of the contact resistance of the TaSi2 / n + -Si contact formed by this manufacturing process. Neither the resistance value nor the range of variation in the value is a sufficient value for realizing a high-performance ULSI. The contact resistance of the metal semiconductor of the source of the MOS transistor or the emitter of the bipolar transistor is required to be extremely low. This is because if the resistance Rs of the source or the emitter is large, the current I flowing through the transistor cannot be increased and the high speed operation of the LSI cannot be realized. If the resistance Rs exists in the source and the emitter, the voltage Vgi applied to the intrinsic transistor becomes Vgi = Vg-RsI, which is smaller than the

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control voltage Vg applied from the outside by RsI. If the transconductance of the transistor is gm, then I = gmVg / (1 + gmRs) rather than I = gm (Vg-RsI). If Rs is large, the denominator is large and the current I is extremely small. For example, when the area of the contact hole is 0.1.times.0.1 .mu.m @ 2 (= 10 @ -10 cm @ 2), the conventional contact resistance Rc=1.times.10@-7 .OMEGA.cm @ 2 results in a contact resistance of 1 K.OMEGA. With only one contact. Normally, in the case of the CMOS structure, at least four contacts are inserted between the power supply and the ground, so it is essential to set Rc to 1 × 10 −9 Ωcm 2 or less.

[0010]

FIG. 12 shows the result of measurement of the impurity concentration distribution in the depth direction of the TaSi2 / n + -Si junction formed by the above manufacturing process by secondary ion mass spectrometry (SIMS). With the above technique, although the interface between the silicide and Si can be cleaned to some extent, oxygen existing at the initial interface is taken into the silicide layer, which is one of the causes for increasing the resistance. It was It was also confirmed that if an oxide film was formed on the metal surface before the heat treatment, the oxygen was mixed into the silicide layer during the heat treatment, and the resistance of the formed silicide layer was increased.

[0011]
Further, as a serious problem in the electrode forming process using silicidation according to the prior art, there is a problem that the silicide layer bites into the silicon substrate.

[0012]
In the silicidation reaction between the refractory metal and silicon, the silicide layer penetrates deeply into the silicon layer, so that it is extremely difficult to achieve an extremely shallow junction between the silicide and silicon.

[0013]

The formation of tantalum silicide (TaSi2) by the reaction of Ta and silicon is taken as an example, and the result of examining how much the silicide layer digs into the silicon substrate is shown in FIG.

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When a Ta film having a thickness of 10 nm is formed on a silicon substrate and heat-treated to react with the silicon substrate, a tantalum silicide layer having a thickness of about 24 nm is formed on the surface of the silicon substrate.

Based on the interface between Ta and silicon in the initial stage, the silicide layer penetrates to the position of 22 nm in depth. It can be seen that the formed silicide has a shape in which 90% or more of the film thickness is submerged in the silicon substrate. Therefore, a large strain is locally generated due to the difference in the lattice spacing between Si and silicide, which causes defects and dislocations. Therefore, the electrode forming method using silicidation according to the prior art is accompanied by a limitation on the device structure in order to use it for forming an electrode of a semiconductor device having an ultrathin / shallow junction.

[0014]

With the progress of ultra-miniaturization and ultra-high integration of ULSI, junctions in semiconductors, such as source / drain of MOSFET and emitter of bipolar transistor, are becoming extremely shallow, reaching about 10 to 50 nm. .. When a silicidation process of a metal thin film and silicon is used in the process of forming an ohmic contact electrode for a semiconductor layer having such an ultra-shallow junction depth, according to the formation method of the prior art, the silicide layer is a source / drain layer. There is a risk of penetrating an ultra-thin layer such as an emitter.

[0015]
Judging from these facts, the conventional silicide formation technology cannot be said to be a perfect solution for drastically reducing the contact resistance, and also has a problem for extremely shallow junction, resulting in higher performance of ULSI, It must be said that achieving high reliability is extremely difficult.

[0016]

SUMMARY OF THE INVENTION The main object of the present invention is to realize two important requirements which are indispensable in the process of forming electrodes and wirings in a semiconductor device for high performance and high reliability ULSI.

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First, in order to reduce the contact resistance between the electrode portion and the semiconductor layer, the contamination layer mainly consisting of an oxide film is eliminated, and the impurity concentration in the semiconductor layer in the region of about 1 nm near the interface between the metal layer and the semiconductor layer, that is, Forming a high-quality metal-semiconductor contact structure that maximizes electron and hole densities, and another is a metal-semiconductor contact structure for a semiconductor device having an ultra-shallow and ultra-thin layer. Is to form.

[0017]
According to a method of manufacturing a semiconductor device of the present invention, at least a part of a semiconductor surface is continuously formed with at least one metal layer and a semiconductor layer without being exposed to the atmosphere, and then a heat treatment is performed. Then, the metal layer and the semiconductor are reacted to form a compound of the metal and the semiconductor.

[0018]
Further, before the heat treatment, it is preferable to ion-implant a predetermined impurity atom or impurity molecule into the semiconductor through the semiconductor layer and the metal layer. In (1), an atom generating an electron or a hole or a molecule containing the atom is suitable, and the injection amount is preferably $1 \times 10\ 13$ to $4 \times 10\ 18$ cm -2.

[0019]
Further, the metal layer is a refractory metal containing at least one of Ta, Ti, W, Co, Mo, Hf, Ni, Zr, Cr, V, Pd and Pt, an alloy containing a refractory metal, or a refractory metal. The compound is preferably a metal compound, and its film thickness is preferably 1 to 50 nm.

[0020]

Further, it is preferable that the semiconductor layer has an impurity concentration of $1 \times 10\ 18$ cm -3 or less so that the surface thereof is not immediately oxidized even when exposed to the atmosphere or washed with ultrapure water.

Further, the film thickness is preferably 0.3 nm or more.

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Furthermore, it is preferable that the thickness of the semiconductor layer is larger than the thickness of the metal layer.

[0021]
Furthermore, the semiconductor and the semiconductor layer are preferably silicon semiconductors.

[0022]
In the present invention, when an unreacted semiconductor layer is present when the second metal layer is further formed after the heat treatment, the unreacted semiconductor layer is removed to form the second metal layer, or A second metal layer is formed on the reacted semiconductor layer and then heat-treated to form a compound of the unreacted semiconductor layer and the metal of the second metal layer.

[0023]

In addition, the method for manufacturing a semiconductor device of the present invention is a method in which a metal layer and a semiconductor layer are continuously formed on a substrate without being exposed to the atmosphere, and subsequently, a heat treatment is performed to react the metal layer and the semiconductor layer with metal. It is characterized in that a compound with a semiconductor is formed and then the unreacted metal layer is removed by etching to form a compound with a metal and a semiconductor in a predetermined shape.

A semiconductor device of the present invention is manufactured by the above manufacturing method.

[0024]

Further, in the semiconductor device in which the compound of the semiconductor and the metal is formed in the contact portion between the semiconductor and the electrode, the depth of the interface between the compound and the semiconductor is shallower than 22 nm.

Furthermore, the semiconductor device of the present invention is a semiconductor device in

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which a compound of the semiconductor and a metal is formed at the contact portion between the semiconductor and the electrode, and at least half the thickness of the compound is above the semiconductor surface. It is characterized by being located.

[0025]
Furthermore, the semiconductor device of the present invention is characterized in that, in the semiconductor device having a multi-layered metal wiring structure, a thin silicide layer is provided in a contact portion connecting upper and lower metal wirings.

[0026]

According to the present invention, in forming a junction between metal wirings or electrode materials and a semiconductor, a semiconductor layer is covered on a super-clean surface of a metal which is very easily oxidized so as to prevent contamination such as growth of an oxide film. Then, heat treatment is performed to form a compound of a metal and a semiconductor.

This makes it possible to form a junction between an electrode having no oxide film and a semiconductor, and to form an electrode layer having very low impurities such as oxygen and low resistance.

At the same time, by reacting the metal and the semiconductor such that the upper and lower sides of the metal layer are sandwiched between the semiconductors, the semiconductor required for the reaction can be supplied from above and below the metal. This makes it possible to reduce the depth of penetration of the compound layer of the metal and the semiconductor into the semiconductor when the entire metal layer is reacted. In particular, by setting the thickness of the semiconductor layer to be equal to or greater than the thickness of the metal layer, this bite can be made even shallower. In the present invention, the semiconductor layer is preferably made of the same material as the semiconductor, but the same effect can be obtained even if the material is different.

[0027]

Further, before the heat treatment, it is effective to permeate the metal layer and the semiconductor layer and perform ion implantation in the vicinity of the interface between the

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metal layer and the semiconductor in order to improve characteristics such as reduction of contact resistance. By the ion implantation, the metal and the semiconductor are mixed and the heat treatment temperature and the treatment time for forming the compound can be reduced. As the implanted ion species, a semiconductor dopant, a semiconductor constituent element, a metal layer constituent element, or the like is preferably used from the viewpoint of further reducing the contact resistance, recrystallization of the semiconductor, and the like. In particular, by controlling the manufacturing process conditions such that the dopant concentration is maximized at the final interface between the compound layer of the metal and the semiconductor and the semiconductor by using the ion serving as the dopant of the semiconductor, the metal and the semiconductor are controlled. The contact resistance with can be reduced. The ion implantation amount and ion energy are appropriately determined depending on the implanted ion species, heat treatment conditions, the thickness of the semiconductor layer and the metal layer, the constituent elements, etc. , $1 \times 10\ 13$ to $4 \times 10\ 18$ cm -2 and 16 to 200 KeV, respectively. Further, the injection amount is more preferably $1 \times 10\ 15$ to $1 \times 10\ 17$ cm -2.

[0028]

In the manufacturing method of the present invention, Si, Ge or the like is preferably used as the semiconductor and the semiconductor layer, and Ta, Ti, W, Co, Mo, Hf, Ni, Zr, Cr, V, Pd, Pt or the like is preferably used as the metal layer. Be done. In particular, when Si is used as a semiconductor material and a refractory metal such as Ta, Ti, W, or Pt is selected as a metal material, it is preferably applied, and is extremely useful as a manufacturing method capable of further improving the performance of LSI. It is a promising manufacturing method.

[0029]

The film thicknesses of the semiconductor layer and the metal layer are mutually determined by the ion implantation conditions, the heat treatment conditions, and the purpose of use. The preferable film thickness of the semiconductor layer is 0.3 nm or more. The metal layer preferably has a thickness of 1 to 50 nm. When the thickness is 1 nm or more, a more uniform metal-semiconductor compound is formed, and when the thickness is 50 nm or less, generation of crystal defects during compound formation can be suppressed. Further, in the present invention, the impurity concentration of the semiconductor layer is preferably $1 \times 10\ 18$ cm -3 or less, and the resistance of the compound formed in this range can be further reduced. This is because if the impurity concentration of the semiconductor layer is higher than this, the surface is likely to be oxidized when exposed to the atmosphere.

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[0030]

100 degreeC or more is preferable and, as for the heat processing of this invention, 300-500 degreeC is more preferable. In this range, a compound of a metal and a semiconductor having low resistance and low contact resistance is formed.

[0031]

Further, in the present invention, after the metal layer and the semiconductor layer are continuously formed on the substrate without exposing them to the air, heat treatment is subsequently performed to react the metal layer and the semiconductor layer to form a compound of the metal and the semiconductor. By forming and then removing the unreacted metal layer by etching and forming the compound of the metal and the semiconductor in a predetermined shape, the refractory metal or its compound (silicide etc.) which has been difficult to form a fine pattern in the past was formed.) Etc. can be precisely and finely patterned.

[0032]

EXAMPLES The present invention will be described in more detail below with reference to examples.

[0033]

(Embodiment 1) A first embodiment of the present invention will be described below with reference to FIG.

1A to 1C are cross-sectional views showing a step of forming an ohmic contact electrode of Ta silicide on n + -Si.

101 is, for example, a p-type silicon wafer, and has a resistivity of, for example, 0.3 to 1.0 Ω · cm. An n-type wafer may be used depending on the purpose. For example, SiO2 102 is formed as an insulating film on the surface of the wafer to a thickness of about 500 nm. An n + high-concentration layer 103 having an n-type impurity concentration of, for example, 1 to 2 × 10 20 cm −3 is formed on the surface of the wafer, and a part of the region in the high-concentration layer 103 is exposed to the outside. An opening 104 is provided in the SiO2 102 so that it can be

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electrically conducted. An electrode material layer 105 (for example, Ta layer) having a thickness of about 5 to 50 nm is formed thereon. Further, on the Ta layer 105, a Si layer 106 containing an impurity having a resistivity of about 0.01 to 10 kΩ · cm in an extremely low concentration (1 × 10 12 to 1 × 10 15 cm −3) is formed to a thickness of about 2 to 30 nm. There is. The Ta layer and the Si layer are continuously formed by using a high vacuum thin film forming apparatus without exposing them to the atmosphere. The reason why continuous film formation is necessary is that the surface of metal is instantaneously oxidized by 2 to 5 nm when exposed to the atmosphere. Especially when non-doped Si is formed on Ta, it is not oxidized for about 1 hour even when exposed to the atmosphere. Needless to say, a metal other than Ta may be used and the layer thickness can be freely selected according to the purpose and conditions. Also for the Si layer, the thickness of the layer can be freely selected according to the purpose and conditions (up to this point, see FIG. 1A). Since Ta has Schottky barrier heights of 0.56 eV and 0.58 eV, which are almost equal to those of n-Si and p-Si, extremely low contact resistance is realized for n + -Si and p + -Si, respectively. Ti is also a metal having similar characteristics.

[0034]

Ion implantation was performed on the wafer having this structure. As the ion species to be implanted, impurities having the same type as the high concentration layer 103 on the wafer, for example, As ions are implanted. This may be P or Sb, but it is desirable that it is the same element as the impurity in the high concentration layer 103 in consideration of the matching of the crystal structures. The implantation dose is, for example, 2 × 10 15 cm −2, and the ion acceleration energy is, for example, 75 keV.

[0035]

In the present embodiment, As ions were used to maximize the impurity concentration at the interface between the silicide and the Si semiconductor and further reduce the contact resistance. However, when the purpose is simply ion mixing, other ions (for example, Ta, Si or the like) may be used.

[0036]

After the ion implantation, heat treatment was performed to form a silicide layer (TaSi2) 107 and recrystallize the ion implanted layer.

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As a heat treatment method, an electric furnace was used and an annealing treatment was performed at 900 ° C. for 1 hour while flowing Ar gas at a rate of 2 l / min. The heat treatment method may be lamp heating or other methods. The temperature is not limited to 900 ° C, but 400 to 500 ° C is sufficient. The gas is not limited to Ar, and gases such as H2, N2, He, and the like, or a mixed gas thereof may be used depending on the purpose and the conditions. Regarding the flow rate, other than the conditions described here, If cleanliness is assured, it is not a problem. Alternatively, it may be more effective to perform the heat treatment in a vacuum in consideration of process consistency. It goes without saying that optimum conditions may be used for the temperature and the processing time depending on the purpose and conditions. Then, the unreacted Si layer remaining on the outermost surface is removed by an etching solution (for example, a mixed aqueous solution of hydrofluoric acid and nitric acid) in a high-purity inert gas atmosphere, for example, in an N2 atmosphere to expose the silicide layer. .. For removing Si, Cl radicals may be generated in a Cl2 gas atmosphere. This is a process performed to completely eliminate the concern of residual Si layer. If the Si layer is entirely silicidized, the etching process described here may not be performed (here (See FIG. 1 (b)).

[0037]

Further, the silicide layer exposed on the surface was transported in an ultrahigh-purity N2 atmosphere, and an electrode material was formed using an ultrahigh vacuum sputtering film forming apparatus. In this embodiment, for example, the Ta layer 108 is formed to a thickness of about 500 nm. The Ta layer 108 and the silicide layer 107 were patterned to form a lead electrode. Needless to say, an electrode material other than Ta may be used as the extraction electrode, and the film thickness may be any thickness other than that described here (see FIG. 1C).

[0038]

FIG. 2 shows the measurement results of the contact resistance of the TaSi2 / n + -Si contact formed by the manufacturing process of the present invention. It can be seen that both the resistance value and the width of its variation are reduced as compared with the conventional example (FIG. 11). FIG. 3 shows the result of measuring the impurity concentration distribution in the depth direction of the TaSi2 / n + -Si junction formed by the manufacturing process of this embodiment by secondary ion mass spectrometry (SIMS). Regarding oxygen, it is below the measurement limit value except for the surface. The presence of oxygen on the surface is due to the oxide film formed on the surface between the time when the oxygen is carried into the SIMS device and the measurement is started.

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[0039]
From this result, the method of the present invention makes it possible to thoroughly prevent the mixing of oxygen in the formation of the junction between the electrode and the semiconductor, and to reduce the mixing of such contaminants in the electrode forming process of the semiconductor device, It can be easily understood that it is very effective in reducing the resistance value.

[0040]
It is also understood from this figure that the As concentration is high near the silicide interface.

[0041]

In this embodiment, an example of forming an electrode on an n-type high-concentration Si layer is shown, but the same applies to forming an electrode on a p-type high-concentration Si layer.

However, in that case, the high-concentration layer 103 is a p-type high-concentration impurity layer.

Further, as the ion species to be implanted, impurities having the same type as the high concentration layer 103 on the wafer (for example, B + ions or BF2 + ions) are implanted. For example, when B ions are used, the energy of ions is 16 to 25 KeV. Alternatively, other ions (eg, Si, Ta, etc.) may be acceptable.

[0042]

As described above, by using the present invention, for example, the contact resistance between the electrode material layer and the semiconductor in the semiconductor device can be further reduced. As a result, it is possible to further improve the performance of ULSI.

[0043]

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(Embodiment 2) A second embodiment of the present invention will be described with reference to FIG. In this example, ions are injected through the semiconductor layer formed on the metal layer to simultaneously perform ion implantation for ion mixing and ion implantation for forming the semiconductor high-concentration layer. FIG. 4A satisfies the same conditions as the wafer of Example 1 except that the high concentration layer 103 is not formed.

[0044]

Ion implantation was performed on the wafer having the structure of FIG. As ion species to be implanted, As ions serving as an n-type dopant were implanted. This may be P or Sb. The implantation dose is, for example, $2 \times 10\ 15\ \mathrm{cm}^{-2}$, and the ion acceleration energy is, for example, 75 keV.

[0045]

After the ion implantation, heat treatment was performed to form a silicide layer (TaSi2) 407 and recrystallize the ion implanted layer. In the heat treatment method, an electric furnace was used and Ar gas was caused to flow at a flow rate of 2 l / min for annealing at 500 ° C. for 1 hour (see FIG. 4B). The heat treatment method and conditions are the same as in Example 1.

[0046]

Then, in a high purity inert gas atmosphere, for example, an Ar atmosphere, the unreacted Si layer remaining on the outermost surface was removed by an etching solution such as a mixed aqueous solution of hydrofluoric acid and nitric acid to expose the silicide layer. Further, for example, a Ta layer 408 having a thickness of about 500 nm was formed thereon as an electrode material without being exposed to the atmosphere. The Ta layer 408 and the silicide layer 407 were patterned to form a lead electrode (see FIG. 4C). Needless to say, an electrode material other than Ta may be used, and the film thickness may be a thickness other than that described here.

[0047]

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FIG. 5 shows the measurement results of the current-voltage characteristics of the pn diode having the n + Si / pSi structure having TaSi2 as an electrode formed by the above manufacturing process. As shown in FIG. 5, it can be seen that good diode characteristics are obtained. As described in Example 1, this result is due to the thorough reduction of contamination such as oxygen during the formation of the bond, and is due to the effect of the bond forming method according to the present invention. ..

[0048]

In the present embodiment, an example relating to the formation of the n-type high-concentration Si layer and the electrode formation is shown, but the same applies to the formation of the p-type high-concentration Si layer and the electrode formation. However, in that case, as the ion species to be implanted, ions serving as p-type dopants (for example, B ions) are used.

[0049]
(Embodiment 3) A third embodiment of the present invention relating to formation of a silicide-silicon junction having a very shallow junction will be described with reference to FIG.

[0050]

Reference numeral 601 denotes p-type silicon on the wafer surface.

The Si layer 601 may be a silicon layer formed on the wafer or the silicon wafer itself. Further, the surface of the Si layer 601 may be covered with an insulating layer or a metal layer at some points, or a diffusion layer having impurities added thereto may be formed at some points of the Si layer 601. The resistivity of the Si layer is 0.3 to 1.0 Ω · cm, for example. The Si layer 601 may use an n-type depending on the purpose. Further, the resistivity is not limited to the range described here, depending on the purpose and conditions. On the Si layer 601, for example, SiO2 602 having a thickness of about 500 nm is formed as an insulating film. At least one opening 603 is provided in the SiO2 602. A metal that reacts with silicon to generate a silicide, for example, a Ta layer 604 is formed thereon with a thickness of about 10 nm. Regarding the thickness, it may be thinner or thicker than this value, but in consideration of forming the silicide layer uniformly or preventing the occurrence of defects due to the volume change during the formation of the silicide as much as possible, the film thickness is about 10 nm. Optimally, it

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should be thick. Furthermore, a Si layer 605 containing an extremely low-concentration impurity having a resistivity of, for example, about 0.01 to 10 kΩ · cm is formed thereon with a thickness of about 30 nm. The thickness of the Si layer 605 is not limited to 30 nm, but in consideration of completely covering the surface of the Ta layer 604 with the Si layer 605 and completely siliciding the entire Ta layer 604, it is about 25 nm or more. If so, there is no problem (see FIG. 6A).

[0051]

Heat treatment was performed to form a silicide layer (TaSi2) 606. As a heat treatment method, an electric furnace was used, and Ar gas was caused to flow at a rate of 2 l / min to perform annealing treatment at 700 ° C. for 1 hour. The heat treatment method may be lamp heating or other methods. The gas is not limited to Ar, and other gases such as H2, N2, He, etc., or a mixed gas thereof may be used depending on the purpose and the conditions, and the flow rate may be other than the conditions described here. It does not matter if the cleanliness of the gas is guaranteed. In some cases, it may be more effective to perform the heat treatment in vacuum. It goes without saying that optimum conditions may be used for the temperature and the processing time depending on the purpose and conditions.

[0052]

After the formation of the silicide, the junction depth xj of the initial surface of the silicon before the reaction of the silicide layer was measured and found to be 12 nm (see FIG. 6B). When the same measurement was performed on the silicide layer formed by the conventional method without forming the Si layer 605, the junction depth was 22 nm.

[0053]

From this result, it can be seen that the use of the silicide forming method of the present invention succeeds in making the junction depth shallow to a value of about 50% as compared with the conventional method. In order to manufacture high-performance and highly-integrated semiconductor elements, it is essential to make the junction extremely shallow. It is apparent from this example that the method of forming a silicide electrode according to the present invention is very effective in meeting this requirement.

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[0054]

(Embodiment 4) FIG. 7 is a sectional view showing a manufacturing process for forming a multilayer wiring structure according to a fourth embodiment of the present invention.

[0055]

701 is a semiconductor on the wafer surface.

Here, a p-type silicon layer is used as an example. The Si layer 701 may be a silicon layer formed on the wafer or the silicon wafer itself. Further, the surface of the Si layer 701 may be covered with an insulating layer or a metal layer at some places, or a diffusion layer having impurities added may be formed at some places of the Si layer 701. The resistivity of the Si layer is 0.3 to 1.0 Ω · cm, for example. Depending on the purpose, n-type may be used. Further, the resistivity is not limited to the range described here, depending on the purpose and conditions. For example, a SiO2 layer 702 is formed as an insulating film layer on the Si layer 701, and at least one opening 703 for exposing the Si layer 701 is formed in a part of the SiO2 layer 702. A metal layer (here, for example, a Ti layer) 704 is formed with a thickness of about 10 nm so as to cover the opening 703. Regarding the thickness, it may be thinner or thicker than this value, but in consideration of forming the silicide layer uniformly or preventing the occurrence of crystal defects as much as possible during the formation of the silicide, the film thickness is about 10 nm. Is best to do. Furthermore, a Si layer 705 containing an extremely low-concentration impurity having a resistivity of, for example, about 0.01 to 10 kΩ · cm is formed thereon with a thickness of about 18 nm. The thickness of the Si layer 705 is not limited to 18 nm, but the surface of the Ti layer 704 may be completely covered with the Si layer 705, or after the heat treatment, the metal layer and the unreacted Si layer should be at least one atomic layer or more. It may be determined in consideration of the thickness of the unreacted Si layer that is left unreacted. Here, the thickness is set to, for example, about 18 nm, which is thicker than the Ti layer 704. After that, the Ti layer 704 and the Si layer 705 were patterned into an appropriate shape (up to this point, see FIG. 7A).

[0056]

Then, it heat-processed. As a heat treatment method, an electric furnace was used, and Ar gas was caused to flow at a rate of 2 l / min to perform annealing treatment at 700 ° C. for 1 hour. The heat treatment method may be lamp heating or other methods. The gas is not limited to Ar,

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and other gases such as H2, N2, He, etc., or a mixed gas thereof may be used depending on the purpose and the conditions, and the flow rate may be other than the conditions described here. Does not mean In some cases, it may be more effective to perform the heat treatment in vacuum. It goes without saying that optimum conditions may be used for the temperature and the processing time depending on the purpose and conditions. By this heat treatment, Ti and Si react with each other to form titanium silicide (TiSi2) 706 with a thickness of about 25 nm. The junction depth of the titanium silicide layer to the Si layer 701 is about 12.5 nm, and the junction is extremely shallow. The film thickness of the unreacted Si layer 705 was about 5.5 nm (up to this point, see FIG. 7B).

[0057]

Next, a SiO2 layer 707, for example, is formed as an interlayer insulating layer for performing electrical insulation between the wirings by a chemical vapor deposition (CVD) method to a thickness of about 500 nm to 1 [mu] m. An opening 708 for exposing the unreacted Si layer 705 on the silicide layer 706 is provided in at least one portion of the interlayer insulating layer 707 by reactive ion etching of the interlayer insulating film after the photolithography process. (Up to here, refer to FIG. 7C).

[0058]

Next, the opening 708 was thoroughly washed with ultrapure water containing a few ppm of ozone, and then the oxide film on the surface of the Si layer 705 was removed using a 0.5 to 1% dilute hydrofluoric acid aqueous solution. Then, a metal layer 709, for example, a Ti layer was formed to a thickness of about 500 nm so as to cover the opening 708. The metal layer 709 may be another metal such as Ta or Pt as long as it is a metal that stably reacts with silicon to form a silicide compound. Further, the film thickness may be such that it completely reacts with the Si layer 705 exposed in the opening 708 and the contact portion between the metal layer 709 and the silicide layer 706 is entirely silicidized. .. The cleaning method has a sufficient cleaning effect on the opening 708, does not completely remove the Si layer exposed in the opening 708, and does not leave any passivation film on the surface of the Si layer. If the condition that the Si surface exposed in the portion 708 can be kept in an ultra-clean state is satisfied, the method used in this embodiment is not necessarily required. (See FIG. 7 (d)).

[0059]

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After that, heat treatment was performed to newly form a silicide layer 710. The heat treatment method is the same as the conditions already described in this example. Lastly, the Ti layer 711 was patterned into at least one or more arbitrary positions to form a wiring structure (see FIG. 7E).

[0060]

According to the method for forming a multilayer wiring structure of the present embodiment, even in the formation of a contact portion between metal wirings, the metal surface is covered with silicon to prevent the metal surface from being oxidized, and the mixing of oxygen at the interface of the metal layer is thoroughly suppressed. I succeeded in doing it. Further, in the cleaning of the opening immediately before the formation of the metal wiring on the contact portion, the method of covering the metal surface with Si was used, and therefore it could not be used for the contact opening portion where the metal surface is exposed. It became possible to clean using an acidic solution, succeeded in achieving super cleanliness of the contact interface, and improved the reliability of the contact part between metal wirings. Furthermore, conventionally, since the interlayer insulating film, mainly SiO2, is formed in direct contact with the metal surface, there is a problem that electrical characteristics such as electric resistance and electromigration resistance are deteriorated due to oxidation of the metal surface, or metal and oxide Although there was a problem of poor adhesion to the film, etc., in the method of the present embodiment, the metal film is not oxidized because the insulating film is formed with the silicon layer left on the silicide layer, and the metal surface on the silicide is not oxidized. The adhesion was also improved because SiO2 was formed on the remaining silicon layer. In this example, the purpose is to reduce the contact resistance between the multilayer metal wirings. In FIG. 7, an example in which the metal layer 709 formed on the Si layer 705 is made of Ti and on the entire surface is described. However, selective deposition of tungsten (W) using WF6 and SiH4 gas for the purpose of surface flattening. It is extremely effective if the above is performed only on the Si layer of the opening 708 and WSi2 is formed by the reaction with the Si layer 705.

[0061]

In an ultra-high speed microprocessor or the like, metal multilayer wiring is often used. When the metal surface is exposed to the air, the surface is instantly oxidized and an oxide film of about 2 to 5 nm is formed. For this reason, the metal-to-metal contact resistance inevitably increases, which deteriorates the high-speed characteristics of the microprocessor and reduces the logic

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amplitude. The process shown in FIG. 14 is effective for preventing the oxidation of the metal surface. Here, an example in which the selective growth of W using WF6 and SiH4 is used to selectively fill the contact hole will be described.

[0062]

A first-layer Al metal wiring (about 0.5 to 1 μm) 1402 and a non-doped Si layer (about 5 to 10 nm) 1403 are continuously formed on the interlayer insulating film 1401. It is desirable that the interlayer insulating film 1404 be continuously formed by a cluster tool, but since the non-doped Si 1403 is hard to be oxidized, the surface may be hydrogen-terminated and then transferred in the atmosphere to be formed. Then, a hole is formed in the interlayer insulating film 1404 according to a predetermined pattern by a photolithography process. At this time, although it is currently exposed to the atmosphere, the Al alloy surface is not oxidized due to the presence of non-doped Si.

[0063]

Only in the non-doped Si, W1405 is selectively formed in the contact hole portion by the WF6 + SiH4 system selective CVD (about 180 ° C.), and the non-doped Si1403 is entirely reacted with W by the heat treatment at 400 to 450 ° C. to be changed to WSi2. In this way, the contact between W and Al alloy is achieved without any oxide film, with WSi2 interposed between W and Al alloy.

[0064]

Further, by preventing the oxide film from existing even in contact with the Al alloy 1406 on W1405, it is possible to realize contact without the oxide film at all contact portions in the multilayer wiring structure. When the Al alloy thin film 1406 can be formed without exposing it to the atmosphere by using a cluster tool or the like, oxygen is mixed by forming the Al alloy thin film 1406 directly on the surface of the formed W1405 as shown in FIG. It is possible to form an interface with a small amount. Here, instead of the W and Al alloys, metals such as Ta, Ti, Cu, Al and Ag or alloys thereof may be used. Further, this method may be applied to any layer of the multilayer wiring structure.

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[0065]

Even when a device such as a cluster tool is not used, by forming the non-doped Si layer 1408 on the W 1405 as shown in FIG. 15, a multi-layer wiring structure having no oxide film at the interface can be realized. That is, by transporting in the air after forming non-doped Si to form the Al alloy thin film 1406, non-doped Si is less likely to be oxidized, and thus an interface having no oxide film can be formed between wirings. Further, in order to further improve the oxidation resistance, the surface may be hydrogen-terminated after the formation of non-doped Si.

[0066]

The non-doped Si 1408 can be continuously formed using, for example, a W1405 forming CVD apparatus. That is, W1405 may be formed by using WF6 and SiH4 gas, and then WF6 gas may be stopped and non-doped Si1408 may be formed by using only SiH4 gas. After processing the Al alloy thin film 1406, the non-doped Si remaining on the insulating film 1404 is usually removed, but it may not be necessary to remove it because of its high resistance. On the other hand, it is possible to selectively form the non-doped Si 1408 only on the W 1405. In this case, after the Al alloy thin film 1406 is processed, the structure as shown in FIG. 16 is obtained, and the non-doped Si 1404 is formed on the insulating film 1404. Is not formed. Also in this case, the non-doped Si 1408 and W 1405 can be continuously formed in the same CVD apparatus as described above.

[0067]

A non-doped Si thin film 1407 is continuously formed on the second-layer Al alloy thin film 1406. Thus, if non-doped Si is formed on the Al alloy thin film, especially if the non-doped Si surface is hydrogen-terminated, W selective growth by WF6 + SiH4 can be completed completely, and it is very effective for surface flattening. Here, it goes without saying that the Al alloy may be pure Al, Cu, or Ag.

[0068]

(Embodiment 5) FIG. 8 is a sectional view showing a method for manufacturing an ohmic contact electrode / wiring structure of a semiconductor and a metal by forming a silicide according to a fifth embodiment of the present invention.

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[0069]

801 is a semiconductor layer.

Here, an n-type silicon layer is used as an example. A p-type may be used depending on the purpose. The Si layer 801 may be a silicon layer formed on the wafer or the silicon wafer itself. Further, the surface of the Si layer 801 may be covered with an insulating layer or a metal layer at some points, or a diffusion layer having impurities added thereto may be formed at some points of the Si layer 801. The resistivity of the Si layer is 0.3 to 1.0 Ω · cm, for example. Further, the resistivity is not limited to the range described here, depending on the purpose and conditions.

[0070]

For example, a SiO2 layer 802 is formed as an insulating film layer on the Si layer 801, and at least one opening 803 for exposing the Si layer 801 is formed in a part of the SiO2 layer 802. A metal layer, here, for example, a Ti layer 804, having a thickness of about 10 nm, is formed over the entire surface of the wafer so as to cover the opening 803. The metal layer 804 may be another metal such as Ta, Co, or W as long as it is a metal that stably reacts with silicon to form a silicide compound.

[0071]

However, it is necessary that the solution for etching the metal is such that the etching reaction is difficult to proceed with the silicide of the metal, that is, the etching solution of the metal can have a large ratio of the etching reaction of the metal to the etching reaction of the silicide. It is said that. The same applies to dry etching. Regarding the thickness, it may be thinner or thicker than this value, but in consideration of forming the silicide layer uniformly or preventing the occurrence of crystal defects as much as possible during the formation of the silicide, a film of about 5 to 10 nm is formed. Optimally, it should be thick.

[0072]

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Further, a Si layer 805 containing an extremely low-concentration impurity having a resistivity of, for example, about 0.01 to 10 kΩ · cm is formed thereon to a thickness of about 8 to 13 nm, and at least one portion of the Si layer 805 is formed. As described above, patterning is performed in an arbitrary shape. The thickness of the Si layer 805 is not limited to 8 to 13 nm, but in the present embodiment, it is necessary to completely cover the surface of the Ti layer 804 with the Si layer 805 or to silicify the entire Si layer 805. Considering this, for example, the thickness is set to about 8 to 13 nm (up to this point, see FIG. 8A).

[0073]

Ion implantation was performed on the wafer having the structure of FIG. As the ion species to be implanted, for example, As ions serving as an n-type dopant were implanted. This may be P or Sb. In this embodiment, ions for n-type dopant are implanted for manufacturing the ohmic contact electrode / wiring structure. However, if the purpose is simply silicidation, other ions (eg, Si, Ti) are used. But good. The implantation dose is, for example, $2 \times 10\ 15\ \mathrm{cm}\ -2$, and the ion acceleration energy is, for example, 75 keV. In this embodiment, the mixing by ion implantation is used to promote the silicidation reaction, but the ion implantation need not necessarily be performed.

[0074]

After the ion implantation, heat treatment was performed to form a silicide layer (TiSi2) and recrystallize the ion implanted layer. As a heat treatment method, an electric furnace was used, and Ar gas was caused to flow at a rate of 2 l / min to carry out annealing treatment at 450 ° C. for 3 hours. The heat treatment method may be lamp heating or other methods. The gas is not limited to Ar, and other gases such as H2, N2, He, etc., or a mixed gas thereof may be used according to the purpose and the conditions, and the flow rate may be other than the conditions described here. Does not mean

[0075]

In some cases, it may be more effective to perform the heat treatment in vacuum. It goes without saying that optimum conditions may be used for the temperature and the processing time depending on the purpose and conditions. By this heat treatment, only Ti in the vicinity of the

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portion covered with the Si layer 805 reacted with silicon, and titanium silicide (TiSi2) 806 was formed with a thickness of about 12 to 25 nm. Other portions of Ti not covered with the Si layer 805 remained unreacted. The implanted As was activated as a dopant by heat treatment, and an n-type high concentration layer 807 was formed around the silicide layer 806 (up to this point, see FIG. 8B).

[0076]

Next, this wafer was immersed in an aqueous solution (25 ° C.) in which NH 4 OH, H 2 O 2 and H 2 O were mixed at a volume ratio of 5: 1: 1. The liquid mixing ratio may be another ratio, for example, 4: 1: 1 :. Regarding the liquid temperature, it is not limited to 25 ° C, but if the liquid temperature is too high, decomposition or evaporation of H2O2 will be caused, and conversely, if the liquid temperature is too low, the reaction rate will decrease, so it is around 25 ° C. And By immersing in this aqueous solution, the unreacted Ti layer was etched and disappeared, and the surface of the SiO2 layer 802 was exposed. On the other hand, the portion where TiSi2 was formed remained without being etched, and a titanium silicide (TiSi2) electrode for ohmic contact to Si and its lead wiring structure were formed (see FIG. 8C). In this embodiment, the method relating to TiSi2 has been described, but when another metal, for example, Co is used, an aqueous solution in which HCl, H2O2 and H2O are mixed may be used for etching after the silicide formation.

[0077]

Patterning by a dry etching process is essential in forming an ultrafine structure. However, when it is difficult to perform dry etching like CuSi, the wet etching method is also effective. That is, a silicon layer patterned into a predetermined shape is formed on the refractory metal. It is easy to perform fine patterning on silicon by using dry etching. Next, heat treatment may be applied or ion mixing may be preceded, but a silicide layer is formed over the entire refractory metal layer. Since only the refractory metal in the portion in contact with silicon is silicide, the width of the formed silicide and the width of the previously patterned silicon layer are almost equal. Then, only the unreacted refractory metal is selectively wet-etched, so that only the silicide remains, and it becomes possible to fabricate a fine structure such as an electrode and a wiring in a predetermined shape (see FIG. 8D).

[0078]

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(Embodiment 6) FIG. 9 is a sectional view showing a sixth embodiment of the present invention. The present embodiment has a semiconductor layer having an extremely shallow junction depth, an electrode structure of a compound of a semiconductor and a metal, and can form an electrode / wiring structure with an arbitrary film thickness.

[0079]

901 is a semiconductor layer. Here, a silicon wafer is used as an example. The surface of the Si layer 901 may be covered with an insulating layer or a metal layer at some points, or a diffusion layer having impurities added thereto may be formed at some points of the Si layer 901. An SiO2 layer 902, for example, is formed as an insulating film layer on the Si layer 901. An n + high-concentration layer 903 having an n-type impurity concentration of, for example, 1 to 2 × 10 20 cm −3 is formed on a part of the surface of the wafer. At least one opening 904 is provided in the SiO2 902 so that electrical connection can be established.

[0080]

On the insulating film layer 902, a metal layer, for example, a Ta layer 905-1 in this case is formed over the entire surface of the wafer so as to cover the opening 904 and has a thickness of about 10 nm. The metal layer 905-1 may be another metal such as Ti, W, or Pt as long as it is a metal that reacts with silicon stably to form a silicide compound. Regarding the thickness, it may be thinner or thicker than this value, but in consideration of forming the silicide layer uniformly or preventing the occurrence of crystal defects as much as possible during the formation of the silicide, a film of about 5 to 10 nm is formed. Optimally, it should be thick.

[0081]

Furthermore, a Si layer 906-1 containing an extremely low-concentration impurity having a resistivity of, for example, about 0.01 to 10 kΩ · cm is formed thereon with a thickness of about 22 nm. The thickness of the Si layer 906-1 is not limited to 22 nm, but in the present embodiment, the surface of the Ta layer 905-1 is completely covered with the Si layer 906-1, or the entire thickness of the Si layer 906-1 is large. In consideration of silicidation, the thickness is, for example, about 22 nm.

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[0082]

Then, ion implantation was performed. As the ion species to be implanted, for example, As ions serving as an n-type dopant were implanted. This may be P or Sb. The implantation dose amount is, for example, about 2×10 15 cm -2, and the ion acceleration energy is, for example, 75 keV (up to this point, see FIG. 9A).

[0083]

On the Si layer 906-1, a metal layer, here, for example, a Ta layer 905-2 is formed over the entire surface of the wafer with a thickness of about 10 nm. The metal layer 905-2 may be made of another metal, but is preferably made of the same material as the metal layer 905-1. Regarding the thickness, it may be thinner or thicker than this value, but in consideration of forming the silicide layer uniformly or preventing the occurrence of crystal defects as much as possible during the formation of the silicide, the film thickness is about 5 to 10 nm. It is best to Furthermore, a Si layer 906-2 containing an extremely low-concentration impurity having a resistivity of, for example, about 0.01 to 10 $k\Omega \cdot$ cm is formed thereon with a thickness of about 22 nm. The thickness of the Si layer 906-2 is not limited to 22 nm, but in the present embodiment, the surface of the Ta layer 905-2 is completely covered with the Si layer 906-2, or the Si layer 906-2 as a whole. Taking into consideration the silicidation of the above, the thickness was set to, for example, about 22 nm (up to this point, refer to FIG. 9B).

[0084]

After that, in consideration of the thickness of the silicide layer to be formed, the formation of the metal layer and the formation of the silicon layer on the metal layer may be repeated any number of times. For example, four pairs of layers and silicon layers were formed. The Ta layer is 905-3 and 905-4, and the Si layer is 906-3 and 906-4 (see FIG. 9C up to this point).

[0085]

Then, heat treatment was performed. The methods and conditions are exactly the same as those for the heat treatment described in Example 1. By heat treatment, the tantalum silicide layer 907

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was formed to a thickness of about 96 nm. In this example, four pairs of the metal layer and the silicon layer are formed to have a thickness of 96 nm, but the thickness of the silicide layer can be relatively freely controlled by controlling the number of times of forming the layers. Further, in the present embodiment, the heat treatment is performed once after the final film formation, but if the Si layer 906-2 is formed, the heat treatment may be performed at least once and any number of times. .. Further, if the Si layer 906-2 is formed, the ion implantation may be performed at any time and any number of times. After forming the silicide layer 907, patterning was performed in an arbitrary shape to fabricate an electrode / wiring structure (up to this point, refer to FIG. 6D).

[0086]

By this method, a contact electrode of silicide and silicon having a very shallow junction could be formed. As described in Example 1, as a result of the high performance of the contact formation process, the dopant concentration at the interface was maximized, and the contamination such as oxygen was thoroughly reduced, resulting in a very low contact resistance value. Was realized.

[0087]

Further, in the contact portion, it is desirable that the film thickness of the metal be as thin as possible in order to suppress the stress strain caused by the thermal stress at the time of forming the silicide or the crystal defect caused by the difference in the lattice constant. However, in consideration of the problem of wiring resistance or disconnection, it is desirable that the film thickness of the metal be as thick as possible in order to simultaneously form the contact electrode and the lead wiring by silicidation. By using the manufacturing method shown in this embodiment, the contact electrode and the lead-out wiring structure can be simultaneously formed by using the silicide layer having a certain thickness while thoroughly suppressing the occurrence of crystal defects, and the electrical characteristics In addition, the depth of penetration into the silicon layer caused by the formation of silicide and the extremely shallow depth can be realized at the contact portion. Therefore, it can be said that the semiconductor device manufacturing method according to the present embodiment is very useful for realizing a high performance ULSI.

[0088]

According to the present invention, it is possible to form a metal electrode having a very low contact resistance and achieve an extremely shallow junction depth. Realization is possible.

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CLAIMS JPH07122519

1.
After continuously forming at least one metal layer and a semiconductor layer on at least a part of the semiconductor surface without exposing to the atmosphere, heat treatment is performed to react the metal layer and the semiconductor to form a compound of the metal and the semiconductor. A method for manufacturing a semiconductor device, which comprises forming the semiconductor device.

2.
2. The method of manufacturing a semiconductor device according to claim 1, wherein a predetermined impurity atom or impurity molecule is ion-implanted into the semiconductor through the semiconductor layer and the metal layer before the heat treatment.

3.
3. The method of manufacturing a semiconductor device according to claim 2, wherein the ions are elements that form the semiconductor, atoms that generate electrons or holes in the semiconductor, or molecules that contain the atoms.

4.
4. The method of manufacturing a semiconductor device according to claim 3, wherein the impurities of the semiconductor are ion-implanted so that the impurity concentration in the semiconductor becomes maximum at the interface between the semiconductor and the compound.

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5.

5. The method of manufacturing a semiconductor device according to claim 2, wherein the implantation amount of the ions is 1 × 10 13 to 4 × 10 18 cm −2.

6.

The method for manufacturing a semiconductor device according to claim 1, wherein the semiconductor is a silicon (Si) semiconductor.

7.

7. The method for manufacturing a semiconductor device according to claim 1, wherein the metal layer is a refractory metal, an alloy containing a refractory metal, or a compound of a refractory metal.

8.

The method of manufacturing a semiconductor device according to claim 7, wherein the metal layer includes at least one of Ta, Ti, W, Co, Mo, Hf, Ni, Zr, Cr, V, Pd, and Pt. ..

9.

The method of manufacturing a semiconductor device according to claim 1, wherein the metal layer has a thickness of 1 to 50 nm.

10.

10. The method of manufacturing a semiconductor device according to claim 1, wherein the semiconductor layer has an impurity concentration of 1 × 10 18 cm −3 or less.

11.

11. The method of manufacturing a semiconductor device according to claim 1, wherein the semiconductor layer has a thickness of 0.3 nm or more.

12.

12. The method of manufacturing a semiconductor device according to claim 11, wherein the thickness of the semiconductor layer is equal to or larger than the thickness of the metal layer to

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make the interface between the compound and the semiconductor shallow.

13.

13. The method of manufacturing a semiconductor device according to claim 11, wherein at least half of the thickness of the compound formed after the heat treatment is located on the semiconductor layer side.

14.

14. The method of manufacturing a semiconductor device according to claim 1, wherein the semiconductor layer is made of a silicon (Si) semiconductor.

15.

15. The semiconductor device according to claim 1, further comprising forming a second metal layer when no unreacted semiconductor layer remains after the heat treatment. Production method.

16.

15. The method for manufacturing a semiconductor device according to claim 1, wherein after the heat treatment, the unreacted semiconductor layer is removed to form the second metal layer.

17.

After the heat treatment, a second metal layer is formed on the unreacted semiconductor layer and then heat treated to form a compound of the unreacted semiconductor layer and the metal of the second metal layer. The method of manufacturing a semiconductor device according to claim 1, wherein

18.

After continuously forming a metal layer and a semiconductor layer on a substrate without exposing them to the atmosphere, the semiconductor layer is patterned into a predetermined shape, and subsequently, heat treatment is performed to react the metal layer with the semiconductor layer to form a metal. A method for manufacturing a semiconductor device, which comprises forming a compound with a semiconductor, and then etching and removing an unreacted metal layer to form a compound with a metal and a semiconductor in a predetermined shape.

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19.

A semiconductor device manufactured by the method for manufacturing a semiconductor device according to claim 1.

20.

A semiconductor device in which a compound of a semiconductor and a metal is formed at a contact portion between a semiconductor and an electrode, wherein a depth of an interface between the compound and the semiconductor is shallower than 22 nm.

21.

21. In a semiconductor device in which a compound of a semiconductor and a metal is formed at a contact portion between a semiconductor and an electrode, a depth of an interface between the compound and the semiconductor is set to 12 nm or less. The semiconductor device described.

22.

In a semiconductor device in which a compound of a semiconductor and a metal is formed at a contact portion between a semiconductor and an electrode, at least half the thickness of the compound is located above the semiconductor surface. Semiconductor device.

23.

A semiconductor device having a multi-layered metal wiring structure, characterized in that a thin silicide layer is provided in a contact portion connecting upper and lower metal wirings.

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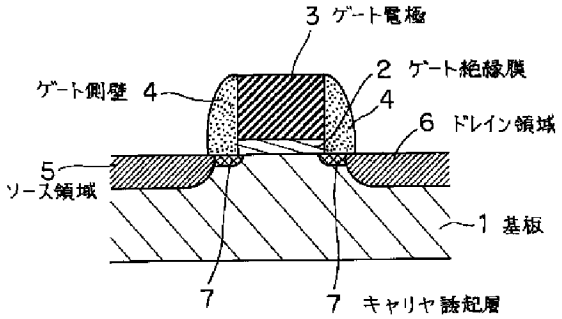
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(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号
(72)発明者　古川　昭雄
東京都港区芝五丁目７番１号　日本電気株式会社内
(74)代理人　弁理士　若林　忠

(54)【発明の名称】　ＭＯＳＦＥＴおよびその製造方法

(57)【要約】
【課題】　短チャネル効果を抑制するのに充分な拡散層の接合深さを、寄生容量増加によるスイッチング速度の低下、製造工程の複雑化などの問題を引き起こさず実現する。
【解決手段】　ゲート側壁４にシリコンよりバンドギャップの大きな半導体を用いているので、ゲート側壁４にドープされた不純物のエネルギーと基板１の伝導帯のエネルギー差のため、ゲート側壁４からその下の基板１上にキャリヤが移動するが、キャリヤにはゲート側壁４の方向に押し付けられるような力が働くため、キャリヤは基板１上でシート状に薄く蓄積され、厚さ５ｎｍ以下の極めて薄いソース領域５・ドレイン領域６端を形成することができ短チャネル効果を抑制することができる。



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【特許請求の範囲】
【請求項１】　シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、
前記ゲート電極の側壁部に設けられたゲート側壁と、
前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴにおいて、
前記ゲート側壁が、シリコンよりバンドギャップが大きく非導電性の半導体層により形成されるとともに不純物が導入されていることを特徴とするＭＯＳＦＥＴ。
【請求項２】　前記ゲート側壁が空乏化することにより非導電性となっている請求項１記載のＭＯＳＦＥＴ。
【請求項３】　前記ゲート側壁と前記ゲート電極の間、または前記ゲート側壁と前記シリコン基板の間、または前記ゲート側壁と前記ゲート電極および前記ゲート側壁と前記シリコン基板との間に絶縁膜が設けられている請求項１または２記載のＭＯＳＦＥＴ。
【請求項４】　シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、
前記ゲート電極の側壁部に設けられ、シリコンよりバンドギャップが大きく非導電性の半導体層により形成されるとともに不純物が導入されているゲート側壁と、
前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴの製造方法において、
前記ゲート側壁への不純物の導入を、前記ソース領域および前記ドレイン領域への不純物イオン注入または前記ゲート電極への不純物イオン注入と同時に行うことを特徴とするＭＯＳＦＥＴの製造方法。
【請求項５】　シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、
前記ゲート電極の側壁部に設けられたゲート側壁と、
前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴにおいて、
前記ゲート側壁が強誘電体材料により形成され、前記シリコン基板がｐ形の場合には前記ゲート電極から前記シリコン基板の方向に分極され、前記シリコン基板がｎ形の場合は前記シリコン基板からゲート電極の方向に分極されていることを特徴とするＭＯＳＦＥＴ。
【請求項６】　前記ゲート側壁と前記ゲート電極の間、または前記ゲート側壁と前記シリコン基板の間、または前記ゲート側壁と前記ゲート電極および前記ゲート側壁と前記シリコン基板との間に絶縁膜が設けられている請求項５記載のＭＯＳＦＥＴ。
【請求項７】　シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、
前記ゲート電極の側壁部に設けられ強誘電体材料により形成されたゲート側壁と、
前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴの製造方法において、
層間絶縁膜を前記シリコン基板の上に形成し、前記層間絶縁膜に前記シリコン基板へ通ずるコンタクト穴を形成し、前記コンタクト穴を金属で埋め込みコンタクト埋め込みとする工程と、
前記ゲート側壁上部に前記層間絶縁膜を介して第１の電極を形成し、前記コンタクト埋め込みの上部に第２の電極を形成する工程と、
前記第１の電極と前記第２の電極との間に電圧を印加し、前記ゲート側壁を分極する工程とを有することを特徴とするＭＯＳＦＥＴの製造成方法。
【請求項８】　シリコン基板の上に複数のウェルが設けられ、前記各ウェル上に複数のゲート絶縁膜を介して設けられた複数のゲート電極と、
前記各ゲート電極の側壁部に設けられ強誘電体材料により形成された複数のゲート側壁と、
前記各ウェル上に設けられた複数のソース領域と複数のドレイン領域とを有するＭＯＳＦＥＴの製造方法において、
層間絶縁膜を前記シリコン基板の上に形成し、前記層間絶縁膜に前記各ウェルへ通ずる複数のコンタクト穴を形成し、前記各コンタクト穴を金属で埋め込みコンタクト埋め込みとする工程と、
前記各ゲート側壁上部に前記層間絶縁膜を介して複数の第１の電極を形成し、前記各コンタクト埋め込みの上部に複数の第２の電極を形成する工程と、
前記各第１の電極どうしと前記各第２の電極どうしをそれぞれ配線により接続し、接続された前記各配線の間に電圧を印加し、前記各ゲート側壁を分極する工程とを有することを特徴とするＭＯＳＦＥＴの製造成方法。
【請求項９】前記第１と第２の電極を除去する工程をさらに有する請求項７または８記載のＭＯＳＦＥＴの製造方法。
【請求項１０】　前記ゲート側壁より外側のソース領域およびドレイン領域部が金属材料により形成されていることを特徴とする請求項１、２、３、５、６のいずれか１項記載のＭＯＳＦＥＴ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、ＭＯＳＦＥＴおよびその製造方法に関し、特にソース領域およびドレイン領域が浅く形成された構造のＭＯＳＦＥＴおよびその製造方法に関する。
【０００２】
【従来の技術】ＭＯＳＦＥＴのゲート長を０．１μｍ以下に微細化する上で問題となる現象として、しきい値がゲート長の微細化とともに減少する短チャネル効果がある。この短チャネル効果を抑制するためには、ソース領域およびドレイン領域構造において、その拡散層の接合深さ、特にゲート端付近の拡散層を浅くする方法が有効である。
【０００３】拡散層の接合深さを浅く形成する従来の方法として、図１０に示すような低エネルギーイオン注入

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法がある。この方法は、基板１０１表面のゲート電極１０３脇のソース領域１０５およびドレイン領域１０６に、例えば１０ｋｅＶ程度のできるだけ小さい値の注入エネルギーで不純物イオンを注入する方法であり、不純物イオン注入層１０４の深さを数十ｎｍ程度に浅くすることができる。

【０００４】拡散層の接合深さをさらに浅くする従来の方法として、図１１に示すような固層拡散法が例えば特開平７－３１２４２２号公報において提案されている。この方法は、ゲート電極１０３の横に例えばリンシリケイトガラス（ＰＳＧ）またはボロンシリケイトガラス（ＢＳＧ）からなる不純物を含んだ絶縁膜として側壁１０７をまず形成し、次いで熱処理により側壁１０７中の不純物を基板１０１中に拡散する。これにより、拡散層の深さを１０ｎｍから４０ｎｍ程度にでき、イオン注入法に比べてより浅い拡散層を得ることができる。

【０００５】また、ソース領域・ドレイン領域の接合深さをさらに浅くする方法として、図１２に示すような方法が例えば特開平１－１２５９７７号公報において提案されている。この方法は、ゲート電極１０３の横に絶縁膜１０８を介してポリシリコンからなる導電性のあるサブゲート１０９を設け、それに電圧を印加するものであり、この方法によれば、サブゲート１０９下の基板１０１上にキャリヤが誘起され反転層となったキャリヤ誘起層１１１が形成されきわめて浅い導伝層が形成される。

【０００６】また、反転層を形成した浅い接合をもったＭＯＳＦＥＴの他の構造として、例えば特開平１－２３２７６５号公報には、第１ゲート電極の横に第２ゲート電極として仕事関数の異なる材料、例えば第１ゲート電極がｐ型シリコンにより形成されている場合には第２ゲート電極にｎ型シリコンを用いたり、第１ゲート電極がｎ型シリコンにより形成されている場合には第２ゲート電極に白金を用いるなどして、第２ゲート電極の下に反転層を形成したものが提案されている。

【０００７】

【発明が解決しようとする課題】上述した従来のＭＯＳＦＥＴでは、下記のような問題点があった。

（１）低エネルギーイオン注入法や固相拡散法においては、拡散層の接合深さを１０ｎｍ以下とすることができず、ゲート長０．１μｍ以下のＭＯＳＦＥＴにおいて十分短チャネル効果を抑制することができない。

（２）サブゲートを設けて電圧を印加して反転層を形成した構造においては、接合深さは浅いものの、動作時にサブゲートに電圧を印加しつづけなければならないことと、サブゲートとゲート電極およびサブゲートとドレイン領域の間に寄生容量が形成されるために、スイッチング速度の低下を招く。

（３）仕事関数の異なる第２ゲート電極を設けた構造においては、第２ゲート電極がゲート電極と接続しており、しかも導電性を持つことから、ゲート電圧印加時に第２ゲート電極にも電圧がかかるため、第２ゲート電極とチャネル間の寄生容量が存在してスイッチング速度の低下をまねく。さらに、ゲート電極および第２ゲート電極の導電性の型が異なるときは、それぞれに異なる不純物を導入する必要があるためＭＯＳＦＥＴの形成工程が複雑となる。

【０００８】本発明の目的は、短チャネル効果を抑制するのに充分な拡散層の接合深さを、寄生容量増加によるスイッチング速度の低下、製造工程の複雑化などの問題を引き起こさず実現したＭＯＳＦＥＴを提供することである。

【０００９】

【課題を解決するための手段】上記目的を達成するために、本発明のＭＯＳＦＥＴは、シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、前記ゲート電極の側壁部に設けられたゲート側壁と、前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴにおいて、前記ゲート側壁が、シリコンよりバンドギャップが大きく非導電性の半導体層により形成されるとともに不純物が導入されていることを特徴とする。

【００１０】本発明は、ゲート側壁にシリコンよりバンドギャップの大きな半導体を用いているので、ゲート側壁にドープされた不純物がドナーの場合はその電子のエネルギーはシリコン基板の伝導帯のエネルギー準位より高くなり、アクセプタの場合はシリコン基板の価電子帯のエネルギー準位より低くなる。そのため、ゲート側壁にドナーがドープされていれば、そのエネルギーとシリコン基板の伝導帯のエネルギー差のため、ゲート側壁からその下のシリコン基板上に電子が移動・蓄積される。他方、アクセプタがドープされていれば、正孔が移動・蓄積される。この電子や正孔にはゲート側壁の方向に押し付けられるように力が働くため、これらの蓄積層はシート状に薄く形成され、その厚さは５ｎｍ以下となる。このため、この部分をソース領域やドレイン領域のゲート端として用いれば、５ｎｍ以下の極めて薄いソース領域・ドレイン領域端を形成することができ短チャネル効果を抑制することができる。

【００１１】本発明の実施態様によれば、前記ゲート側壁が空乏化することにより非導電性となっている。

【００１２】また、本発明の実施態様によれば、前記ゲート側壁と前記ゲート電極の間、または前記ゲート側壁と前記シリコン基板の間、または前記ゲート側壁と前記ゲート電極および前記ゲート側壁と前記シリコン基板との間に絶縁膜が設けられている。

【００１３】本発明は、絶縁膜をゲート側壁とゲート電極またはゲート側壁とシリコン基板の間に設けるようにしたものである。したがって、ゲート側壁とゲート電極またはゲート側壁とシリコン基板との間の絶縁性を向上することができる。

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【００１４】また、本発明のＭＯＳＦＥＴの製造方法は、シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、前記ゲート電極の側壁部に設けられ、シリコンよりバンドギャップが大きく非導電性の半導体層により形成されるとともに不純物が導入されているゲート側壁と、前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴの製造方法において、前記ゲート側壁への不純物の導入を、前記ソース領域および前記ドレイン領域への不純物イオン注入または前記ゲート電極への不純物イオン注入と同時に行うことを特徴とする。

【００１５】本発明は、ゲート側壁への不純物導入を、ソース領域およびドレイン領域への不純物イオン注入またはゲート電極への不純物イオン注入と同時に行うようにしたものである。

【００１６】したがって、ゲート側壁へイオン注入する独自の工程を必要としないので、製造工程数を減らすことができる。

【００１７】また、本発明のＭＯＳＦＥＴは、シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、前記ゲート電極の側壁部に設けられたゲート側壁と、前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴにおいて、前記ゲート側壁が強誘電体材料により形成され、前記シリコン基板がｐ形の場合には前記ゲート電極から前記シリコン基板の方向に分極され、前記シリコン基板がｎ形の場合は前記シリコン基板からゲート電極の方向に分極されていることを特徴とする。

【００１８】本発明は、ゲート側壁に分極された強誘電体を用いているので、その分極方向により電子または正孔がゲート側壁とシリコン基板の界面のシリコン基板側に誘起され、その単位面積当たりの濃度は$1\times10^{14}cm^{-2}$程度となる。そして、この電子や正孔にはゲート側壁の方向に押し付けられるように力が働くため、これらの層はシート状に薄く形成され、その厚さは５ｎｍ以下となる。このため、この部分をソース領域領域やドレイン領域のゲート端として用いれば、５ｎｍ以下の極めて薄いソース領域・ドレイン領域端を形成することができ短チャネル効果を抑制することができる。

【００１９】また、本発明の実施態様によれば、前記ゲート側壁と前記ゲート電極の間、または前記ゲート側壁と前記シリコン基板の間、または前記ゲート側壁と前記ゲート電極および前記ゲート側壁と前記シリコン基板との間に絶縁膜が設けられている。

【００２０】本発明は、絶縁膜をゲート側壁とゲート電極またはゲート側壁とシリコン基板の間に設けるようにしたものである。したがって、ゲート側壁とゲート電極またはゲート側壁とシリコン基板との間の絶縁性を向上することができる。

【００２１】また、本発明のＭＯＳＦＥＴは、シリコン基板の上にゲート絶縁膜を介して設けられたゲート電極と、前記ゲート電極の側壁部に設けられ強誘電体材料により形成されたゲート側壁と、前記シリコン基板上に設けられたソース領域とドレイン領域とを有するＭＯＳＦＥＴの製造方法において、層間絶縁膜を前記シリコン基板の上に形成し、前記層間絶縁膜に前記シリコン基板へ通ずるコンタクト穴を形成し、前記コンタクト穴を金属で埋め込みコンタクト埋め込みとする工程と、前記ゲート側壁上部に前記層間絶縁膜を介して第１の電極を形成し、前記コンタクト埋め込みの上部に第２の電極を形成する工程と、前記第１の電極と前記第２の電極との間に電圧を印加し、前記ゲート側壁を分極する工程とを有することを特徴とする。

【００２２】本発明は、シリコン基板上に層間絶縁膜を形成し、その層間絶縁膜にシリコン基板と電気的に接続するためのコンタクト埋め込みを設けるとともに層間絶縁膜を介したゲート電極上部とコンタクト埋め込み上にそれぞれ電極を設けるようにしたものである。

【００２３】したがって、その設けられた２つの電極間に電圧を印加することにより、ゲート側壁を分極することができる。

【００２４】また、本発明のＭＯＳＦＥＴは、シリコン基板の上に複数のウェルが設けられ、前記各ウェル上に複数のゲート絶縁膜を介して設けられた複数のゲート電極と、前記各ゲート電極の側壁部に設けられ強誘電体材料により形成された複数のゲート側壁と、前記各ウェル上に設けられた複数のソース領域と複数のドレイン領域とを有するＭＯＳＦＥＴの製造方法において、層間絶縁膜を前記シリコン基板の上に形成し、前記層間絶縁膜に前記各ウェルへ通ずる複数のコンタクト穴を形成し、前記各コンタクト穴を金属で埋め込みコンタクト埋め込みとする工程と、前記各ゲート側壁上部に前記層間絶縁膜を介して複数の第１の電極を形成し、前記各コンタクト埋め込みの上部に複数の第２の電極を形成する工程と、前記各第１の電極どうしと前記各第２の電極どうしをそれぞれ配線により接続し、接続された前記各配線の間に電圧を印加し、前記各ゲート側壁を分極する工程とを有することを特徴とする。

【００２５】本発明は、１つのシリコン基板の複数のウェル上に設けられた複数のＭＯＳＦＥＴに対して、シリコン基板上に層間絶縁膜を形成し、その層間絶縁膜に各ウェルと電気的に接続するためのコンタクト埋め込みを設けるとともに層間絶縁膜を介したゲート電極上部とコンタクト埋め込み上にそれぞれ第１と第２の電極を設け、第１の電極どうしと第２の電極どうしを配線により接続したものである。

【００２６】したがって、その接続された２つの電極間に電圧を印加することにより、複数のＭＯＳＦＥＴの強誘電体側壁を同時に分極することができる。

【００２７】また、本発明の実施態様によれば、第１と

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第２の電極を除去する工程をさらに有する。
【００２８】本発明は、ゲート側壁の分極を行った後に第１と第２の電極を除去するようにして、以後のプロセスを進める上で障害とならないようにしたものである。したがて、ＭＯＳＦＥＴの製作が容易になる。
【００２９】また、本発明の実施態様によれば、前記ゲート側壁より外側のソース領域およびドレイン領域部が金属材料により形成されていることを特徴とする。
【００３０】本発明は、ソース領域およびドレイン領域を金属材料により形成するようにしたものである。したがって、イオン注入の工程が不要となりＭＯＳＦＥＴを製造するための工程数を減らすことができる。
【００３１】
【発明の実施の形態】次に、本発明の実施形態について図面を参照して詳細に説明する。
（第１の実施形態）図１は本発明の第１の実施形態のＭＯＳＦＥＴの製造方法を示す断面摸式図、図２は図１のＭＯＳＦＥＴの構造を示す断面摸式図である。
【００３２】本実施形態のＭＯＳＦＥＴの製造方法を図１を用いて説明する。
【００３３】本実施形態は、不純物濃度が$1\times10^{14}cm^{-3}$程度のｐ型シリコンの基板１上に酸化シリコンでできた５ｎｍ厚のゲート絶縁膜２を形成し、絶縁膜２の上にｎ型ポリシリコン膜を２００ｎｍ形成した後、レジスト塗布、露光、現像工程をへてエッチングによりゲート電極３を形成する（図１（ａ））。
【００３４】次に、基板１上にノンドープのシリコンカーバイドを５０ｎｍ形成した後、異方性エッチングによりゲート側壁４を形成する（図１（ｂ））。
【００３５】この後、ＭＯＳＦＥＴ全面に砒素または燐をイオン注入することにより、ゲート電極３、ゲート側壁４への不純物導入と、基板１表面上にソース領域５およびドレイン領域６の形成を同時に行う（図１（ｃ））。この後、１０００℃、３０秒間の熱処理を行い不純物を活性化させる。
【００３６】上記の方法によれば、ゲート側壁４への不純物導入をソース領域５・ドレイン領域６へのイオン注入と同時に行うことができるので、工程数の増加を回避することができる。
【００３７】本実施形態のＭＯＳＦＥＴの構造を図２を用いて説明する。
【００３８】本実施形態のＭＯＳＦＥＴは、ゲート側壁４がシリコンよりバンドギャップの大きなシリコンカーバイドであるため、その中の電子はエネルギーの低いシリコンにより形成された基板１の表面に移動し、キャリヤ誘起層７が形成される。このキャリヤ誘起層７は電子の波動関数程度の広がりしか持たないために、その厚さは５ｎｍ以下と薄くなり短チャネル効果を抑制することができる。
【００３９】また、ゲート側壁４は半導体で形成されているため、伝導性をもつ可能性があり、その場合にはゲート側壁４はゲート電極３の一部となって実質上ゲート長が大きくなったり、ドレイン領域６との容量増加の原因となるため、ゲート側壁４は導電性をもたなくする必要がある。そのためには、ドナーやアクセプタが空乏化する程度にゲート側壁４の厚さを薄くする必要がある。
【００４０】しかし本実施形態では、ゲート側壁４の膜厚は５０ｎｍと薄いため、電子はすべて基板１に移動し、ゲート側壁４は空乏化し伝導性を持たなくなる。そのため、寄生容量の増加などによりＭＯＳＦＥＴの特性を劣化させることはない。
【００４１】本実施形態では、不純物をｎ型ＭＯＳＦＥＴの場合の導伝型として記述したが、ｐ型ＭＯＳＦＥＴの場合には、導伝型を逆にした不純物を用いればよい。
【００４２】また、ここではゲート側壁４の材料として、シリコンカーバイドを用いたが、ダイヤモンドやガリウムヒソ、インジウムリンなどシリコンよりバンドギャップの大きい材料を用いれば同様な効果が得られる。ただし、そのなかの元素がシリコン中に拡散しないようなプロセスや材料にする必要がある。
（第２の実施形態）図３は本発明の第２の実施形態のＭＯＳＦＥＴの構造を示す断面摸式図である。図２中と同番号は同じ構成要素を示す。
【００４３】本実施形態は、図２の第１の実施形態に対して、ゲート電極３の形成後にキャリヤが通過できない厚さ５ｎｍ程度の酸化シリコン膜を絶縁膜８として、ゲート側壁４とゲート電極３およびゲート側壁４と基板１との間に形成したものである。
【００４４】本実施形態は、絶縁膜８、ゲート側壁４を形成した後、ＭＯＳＦＥＴ全面に不純物をイオン注入することにより、第１の実施形態と同様にゲート側壁４に不純物を導入することができる。
【００４５】本実施形態のＭＯＳＦＥＴは、第１の実施形態と同様に短チャネル効果を抑制することができ、さらに絶縁膜８が存在するために、ゲート側壁４とゲート電極３およびゲート側壁４と基板１間の絶縁性を向上することができる。
【００４６】本実施形態ではゲート側壁４とゲート電極３およびゲート側壁４と基板１との間に絶縁膜８が設けられていたが、ゲート側壁４とゲート電極３の間またはゲート側壁４と基板１の間のみに絶縁膜８が設けられていてもよい。
（第３の実施形態）図４は本発明の第３の実施形態のＭＯＳＦＥＴの製造方法を示す断面摸式図、図５は図４のＭＯＳＦＥＴの強誘電体側壁４４の分極方法を示す断面模式図、図６は図４のＭＯＳＦＥＴの強誘電体側壁４４の分極方向を示す断面模式図、図７は図４のＭＯＳＦＥＴの構造を示す断面模式図である。
【００４７】本実施形態のＭＯＳＦＥＴの製造方法を図４を用いて説明する。

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【００４８】本実施形態は、不純物濃度が1×10^{14} cm^{-3}程度のｐ型シリコンの基板４１上に酸化シリコンでできた５ｎｍ厚のゲート絶縁膜４２、ｎ型ポリシリコン膜を２００ｎｍ形成した後、レジスト塗布、露光、現像工程をへてエッチングによりゲート電極４３を形成する（図4（ａ））。

【００４９】次に、ＰＺＴなどの強誘電体膜４０をゲート電極４３と基板４１の上に厚さ５０ｎｍで形成し（図４（ｂ））、異方性エッチングにより強誘電体側壁４４を形成する（図4（ｃ））。

【００５０】この後、基板４１の表面上に不純物をイオン注入することにより、ソース領域４５およびドレイン領域４６を形成することができる。このあと、１０００℃、３０秒間の熱処理を行い不純物を活性化させる。

【００５１】次に本実施形態のＭＯＳＦＥＴの強誘電体側壁４４の分極方法を図５を用いて説明する。図４中と同番号は同じ構成要素を示す。

【００５２】ＭＯＳＦＥＴを素子分離９３およびコンタクト層９４とともに基板４１に形成したあと、層間絶縁膜９９を形成し、基板４１へ通ずるコンタクト穴を形成し、それをタングステンなどで埋め込み、コンタクト埋め込み１００を形成する。

【００５３】素子分離９３は、SiO_2等により形成され、１つのチップ上に複数のＭＯＳＦＥＴを形成する場合等に、それぞれのＭＯＳＦＥＴどうしを電気的に分離するためのものである。

【００５４】コンタクト層９４は、コンタクト埋め込み１００と基板４１との間を電気的に低抵抗で接続するために、基板４１と同じ不純物を高濃度で導入した層である。

【００５５】その後、コンタクト埋め込み１００の上に電極１１３を形成し、層間絶縁膜９９を挟んだゲート電極９５上に電極１１２を形成する。

【００５６】そして、電極１１２と電極１１３の間に電圧を印加し、強誘電体側壁４４を分極する。電圧の印加の仕方は、ｎ型ＭＯＳＦＥＴでは基板４１に対して電極１１２を正にし、ｐ型ＭＯＳＦＥＴでは基板４１に対して電極１１２を負にすればよい。

【００５７】強誘電体側壁４４の分極は、図５の状態で行うか、または、さらにプロセスを進めた状態で行う。図５の状態で行う場合は、分極後に層間絶縁膜９９上に形成された電極１１２、１１３をエッチングにより除去しても、残しておいてもよい。しかし、電極１１２、１１３は除去したほうが以後のプロセスを進める上で障害とならずＭＯＳＦＥＴの製作が容易になる。

【００５８】本実施形態では、１つのＭＯＳＦＥＴに対する分極方法を示したが、１つの半導体の基板上に複数のＭＯＳＦＥＴが形成されている場合は、複数のＭＯＳＦＥＴの強誘電体側壁を同時に分極することが可能である。この場合、基板上に複数のウェルを形成し、そのそれぞれのウェル上に図５のようなＭＯＳＦＥＴを形成し、複数のＭＯＳＦＥＴのゲート電極の上に形成された電極どうしを配線で接続し、コンタクト埋め込みの上に形成された電極どうしを配線で接続し、それぞれの配線の間に電圧を印加すれば複数のＭＯＳＦＥＴの強誘電体側壁を同時に分極することができる。

【００５９】次に、本実施形態のＭＯＳＦＥＴにおける強誘電体側壁４４の分極の方向を図６を用いて説明する。図６において、強誘電体４４の中の矢印は分極方向を示している。図４中と同番号は同じ構成要素を示す。

【００６０】図６（ａ）はｎ型ＭＯＳＦＥＴにおける分極方向を示した図であり、強誘電体側壁４４の分極方向は下向きである。この場合、強誘電体側壁４４中の下側は正に帯電するため、それを打ち消すように基板に負の電荷（電子）が蓄積され、電子誘起層４９が形成される。

【００６１】図６（ｂ）はｐ型ＭＯＳＦＥＴにおける分極方向を示した図であり、強誘電体側壁４４の分極方向は上向きである。この場合、強誘電体側壁４４中の下側は負に帯電するため、それを打ち消すように基板に正の電荷（正孔）が蓄積され、正孔誘起層５０が形成される。

【００６２】また、上記の分極方向は基板４１に対し垂直な方向を向いているが、必ずしもその必要はなく、垂直から６０度程度傾いてもキャリヤは誘起することができるため問題はない。

【００６３】本実施形態のＭＯＳＦＥＴの構造を図７を用いて説明する。図４中と同番号は同じ構成要素を示す。

【００６４】本実施形態は、強誘電体側壁４４をゲート電極４３の側面に形成しているため、それをゲート電極４３から基板４１方向に平行に分極することにより基板４１の表面に電子が誘起され、キャリヤ誘起層４７が形成される。このキャリヤ誘起層４７は電子の波動関数程度の広がりしか持たないために、その厚さは５ｎｍ以下と薄く、短チャネル効果を抑制することができる。強誘電体側壁４４は伝導性をもたない絶縁体であるため、その形成による寄生容量の増加などのＭＯＳＦＥＴ特性を劣化することはない。

【００６５】ここでは、不純物はｎ型ＭＯＳＦＥＴを仮定して導伝型を記述したが、ｐ型ＭＯＳＦＥＴにおいては、導伝性が逆のものを用いればよい。

（第４の実施形態）図８は本発明の第４の実施形態のＭＯＳＦＥＴの構造を示す断面摸式図である。図７中と同番号は同じ構成要素を示す。

【００６６】本実施形態は、図７の第３の実施形態の構造に追加して、ゲート電極４３の形成後にキャリヤが通過できない５ｎｍ程度の厚さの酸化シリコン膜を絶縁膜４８として、強誘電体側壁４４とゲート電極４３および強誘電体側壁４４と基板４１の間に形成したものであ

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る。本実施形態のＭＯＳＦＥＴは、第４の実施形態のように短チャネル効果を抑制し、さらに絶縁膜４８が存在するために、強誘電体側壁４４とゲート電極４３や強誘電体側壁４４と基板４１間の絶縁性を向上することができる。

【００６７】本実施形態ではゲート側壁４４とゲート電極４３およびゲート側壁４４と基板４１との間に絶縁膜４８が設けられていたが、ゲート側壁４４とゲート電極４３の間またはゲート側壁４４と基板４１の間のみに絶縁膜４８が設けられていてもよい。

（第５の実施形態）図９は本発明の第５の実施形態のＭＯＳＦＥＴの構造を示す断面摸式図である。　本実施形態は、不純物濃度が$1\times10^{14}cm^{-3}$程度のｐ型シリコンの基板７１上に酸化シリコンでできた５ｎｍ厚のゲート絶縁膜７２、ｎ型ポリシリコン膜を２００ｎｍ形成した後、それをレジスト塗布、露光、現像工程をへてエッチングによりゲート電極７３を形成し、強誘電体のＰＺＴ膜１００ｎｍを形成したあと異方性エッチングにより強誘電体側壁７４を形成、その後チタンを全面に形成し、８００℃の熱処理により基板７１とチタンを反応させ、その後強誘電体側壁７４上のチタンの反応物およびチタンをフッ酸系のエッチング液により剥離し、チタンシリサイドでできた金属層のソース領域７５と金属層のドレイン領域７６を形成する。

【００６８】また、強誘電体側壁７４の下の基板７１の表面にはキャリヤ誘起層７７が形成され、その濃度は$1\times10^{14}cm^{-2}$程度である。

【００６９】本実施形態の構造では、キャリヤ誘起層７７の外側に金属層でできたソース領域７５とドレイン領域７６が形成されている。通常は金属とシリコンが接触している場合には、その間にショットキーバリヤというポテンシャル障壁が存在し、接触抵抗が生ずる。そして、この接触抵抗によりＭＯＳＦＥＴの特性が劣化する。但し、半導体側の不純物濃度が高い場合には、このポテンシャル障壁厚が薄くなるため、小さな接触抵抗になる。

【００７０】本実施形態の場合には、キャリヤ誘起層７７の濃度は非常に高く、単位体積当たりの濃度に換算すると$1\times10^{20}cm^{-3}$程度のため、接触抵抗はＭＯＳＦＥＴのチャネル抵抗に比べるとほとんどゼロに近く、ＭＯＳＦＥＴの特性には問題とならない。そして、短チャネル効果については、第４の実施形態と同じく抑制することができる。そのため、ソース領域７５、ドレイン領域７６を金属層により形成すると、短チャネル効果を抑制できるとともに、イオン注入の工程を不要とすることができＭＯＳＦＥＴを製造するための工程数を減らすことができる。

【００７１】本実施形態では、ゲート側壁として強誘電体を用いた場合について述べたが、第１の実施形態のようにシリコンよりバンドギャップが大きく、不純物をドープした半導体を用いた場合でも同様な効果がある。

【００７２】

【発明の効果】以上説明したように、本発明は、ゲート端の基板上部に浅いソース領域、ドレイン領域の一部を形成することができ、０．１μｍ以下のゲート長をもつＭＯＳＦＥＴにおいて、寄生抵抗を増加することなく短チャネル効果を抑制することができるという効果を有する。

【図面の簡単な説明】

【図１】本発明の第１の実施形態のＭＯＳＦＥＴの製造方法を示す断面模式図である。

【図２】図１のＭＯＳＦＥＴの構造を示す断面模式図である。

【図３】本発明の第２の実施形態のＭＯＳＦＥＴの構造を示す断面模式図である。

【図４】本発明の第３の実施形態のＭＯＳＦＥＴの製造方法を示す断面模式図である。

【図５】図４のＭＯＳＦＥＴの強誘電体側壁４４の分極方法を示す断面模式図である。

【図６】図４のＭＯＳＦＥＴの強誘電体側壁４４の分極方向を示す断面模式図である。

【図７】図４のＭＯＳＦＥＴの構造を示す断面模式図である。

【図８】本発明の第４の実施形態のＭＯＳＦＥＴの構造を示す断面模式図である。

【図９】本発明の第５の実施形態のＭＯＳＦＥＴの構造を示す断面模式図である。

【図１０】従来のＭＯＳＦＥＴの構造を示す断面模式図である。

【図１１】従来のＭＯＳＦＥＴの構造を示す断面模式図である。

【図１２】従来のＭＯＳＦＥＴの構造を示す断面模式図である。

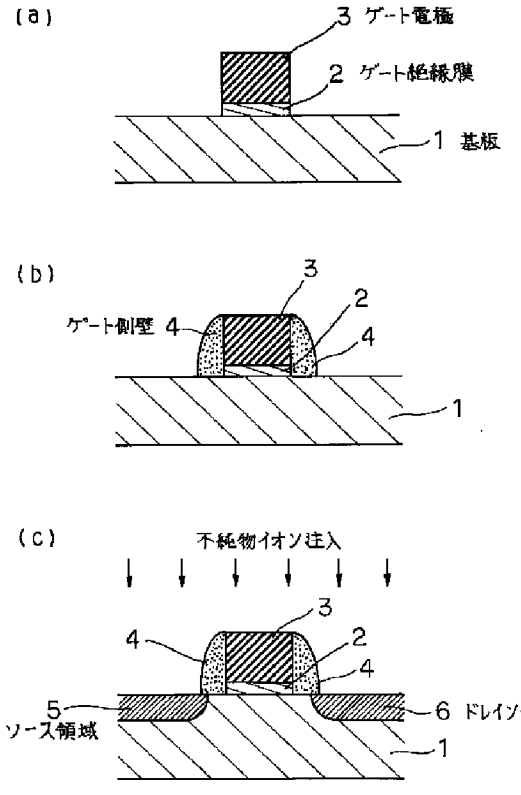
【符号の説明】

１　基板
２　ゲート絶縁膜
３　ゲート電極
４　ゲート側壁
５　ソース領域
６　ドレイン領域
７　キャリヤ誘起層
８　絶縁膜
４０　強誘電体膜
４１　基板
４２　ゲート絶縁膜
４３　ゲート電極
４４　強誘電体側壁
４５　ソース領域
４６　ドレイン領域
４７　キャリヤ誘起層

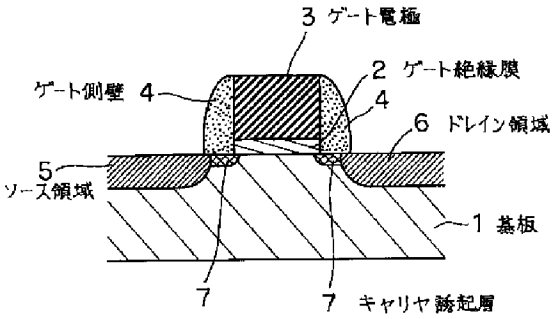
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４８　絶縁膜
４９　電子誘起層
５０　正孔誘起層
７１　基板
７２　ゲート絶縁膜
７３　ゲート電極
７４　強誘電体側壁
７５　ソース領域
７６　ドレイン領域
７７　キャリヤ誘起層
９３　素子分離
９４　コンタクト層
９９　層間絶縁膜
１００　コンタクト埋め込み
１０１　基板
１０２　ゲート絶縁膜
１０３　ゲート電極
１０４　不純物イオン注入層
１０５　ソース領域
１０６　ドレイン領域
１０７　側壁
１０８　絶縁膜
１０９　サブゲート
１１０　不純物拡散層
１１１　キャリア誘起層
１１２、１１３　電極

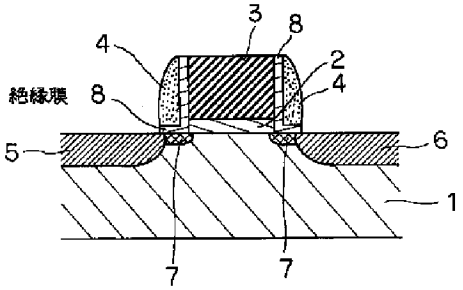
【図１】



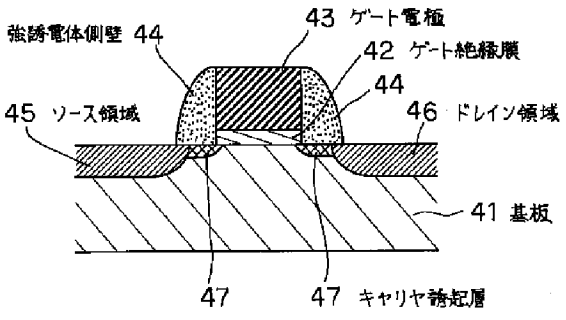
【図２】



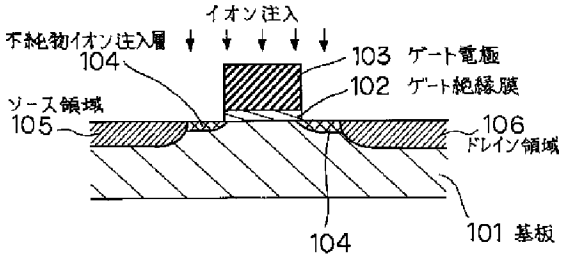
【図３】



【図７】

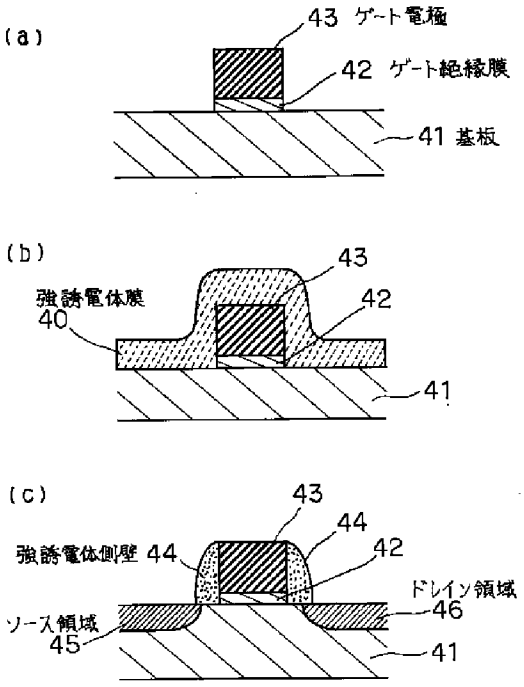


【図１０】

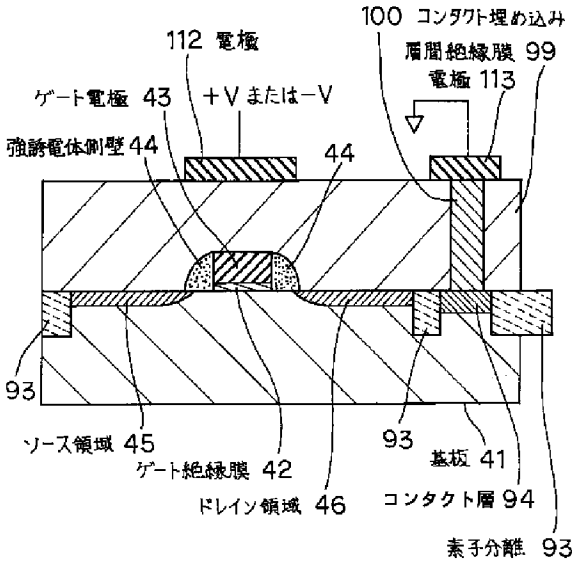


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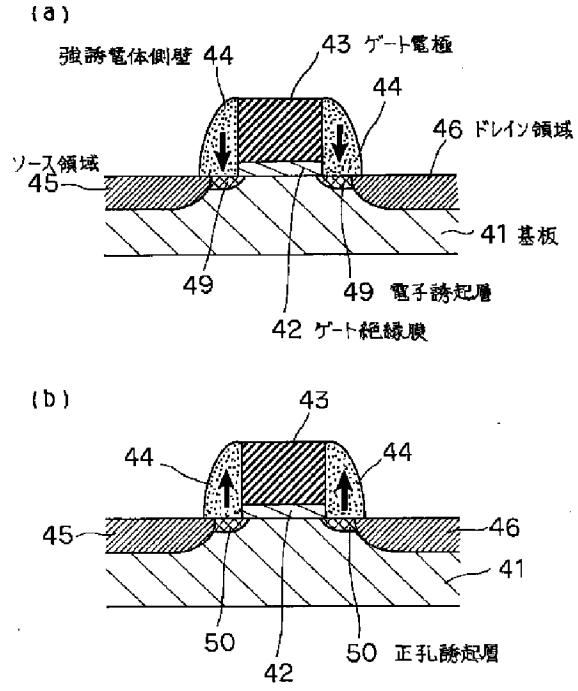
【図4】



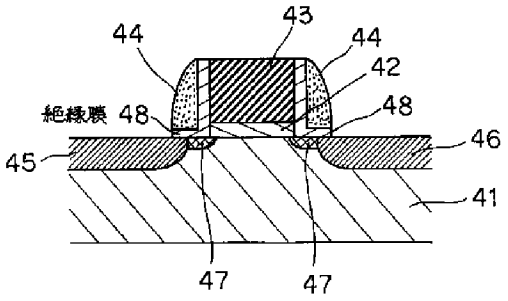
【図5】



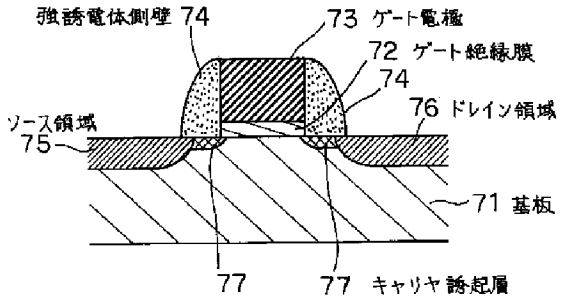
【図6】



【図8】

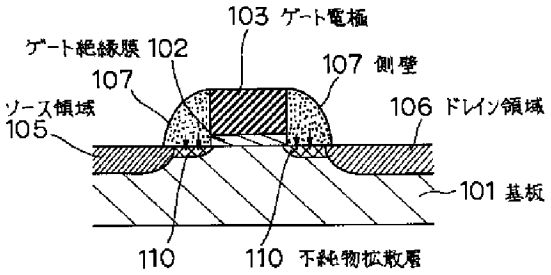


【図9】

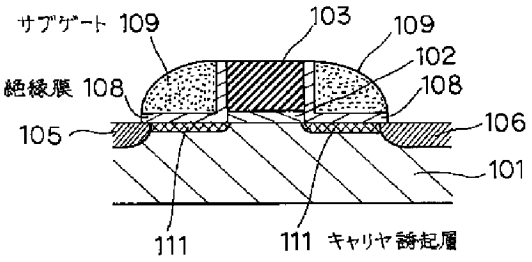


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【図１１】


103 ゲート電極
ゲート絶縁膜 102
107
107 側壁
ソース領域
105
106 ドレイン領域
101 基板
110
110 不純物拡散層

【図１２】


サブゲート 109
103
109
102
絶縁膜 108
108
105
106
101
111
111 キャリヤ誘起層

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JPH10209445A MOSFET AND MANUFACTURE THEREOF

Applicants: NEC CORP

Inventors: FURUKAWA AKIO

Classifications:
IPC ***H01L21/336; H01L29/78;*** (IPC1-7): H01L21/336; H01L29/78;

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Application: JPH10209445A·1997-01-21

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MOSFET AND MANUFACTURE THEREOF

Abstract

PROBLEM TO BE SOLVED: To reailize the junction depth of a diffused layer, which is enough for inhibiting the short tunnel effect of a MOSFET, without causing problems, such as a reduction in the switching rate of the MOSFET due to an increase in a parasitic capacitance and the complication of the manufacturing process of the MOSFET. SOLUTION: In a MOSFET, which has a gate electrode 3 on a silicon substrate 1 via a gate insulating film 3, gate sidewalls on the substrate 1 and source and drain regions 5 and 6 in the substrate 1, the sidewalls 4 are formed of a non-conductive semiconductor layer having a band gap larger than that of a silicon layer and at the same time, impurities are introduced in the substrate 1. As the semiconductor layer having a band gap larger than of the silicon layer is used for the gate sidewalls 4, carriers are moved from the sidewalls 4 to the interiors of the upper parts, which are located under the sidewalls 4, of the substrate 1 due to a difference between the energy of impurities doped to the sidewalls 4 and the energy of the conduction band of the substrate 1, but as such a force that the carriers are pressed in the directions of the sidewalls 4 works on the carriers, the carriers 4 are thinly stored in the substrate 1 in a sheet type, the ends, which have a very thin thickness of 5nm or thinner, of the regions 5 and 6 can be formed and the short channel effect of the MOSFET can be inhibited.

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DESCRIPTION JPH10209445

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a MOSFET and a manufacturing method thereof, and more particularly to a MOSFET having a structure in which a source region and a drain region are shallowly formed and a manufacturing method thereof.

[0002]

2. Description of the Related Art A phenomenon which becomes a problem in miniaturizing a gate length of a MOSFET to 0.1 .mu.m or less is a short channel effect in which a threshold value is reduced as the gate length is miniaturized. In order to suppress this short channel effect, it is effective to make the junction depth of the diffusion layer, especially the diffusion layer near the gate end, shallow in the source region and drain region structure.

[0003]

As a conventional method for forming the junction depth of the diffusion layer shallow, there is a low energy ion implantation method as shown in FIG. This method is a method of implanting impurity ions into the source region 105 and the drain region 106 beside the gate electrode 103 on the surface of the substrate 101 with implantation energy as small as possible, for example, about 10 keV, and the depth of the impurity ion implantation layer 104. Can be made as shallow

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as several tens of nm.

[0004]

As a conventional method for further reducing the junction depth of the diffusion layer, a solid layer diffusion method as shown in FIG. 11 is proposed in, for example, Japanese Unexamined Patent Publication No. 7-312422. According to this method, a side wall 107 is first formed as an insulating film containing impurities such as phosphorus silicate glass (PSG) or boron silicate glass (BSG) next to the gate electrode 103, and then the impurities in the side wall 107 are treated by heat treatment to the substrate. Diffuses into 101. Thereby, the depth of the diffusion layer can be set to about 10 nm to 40 nm, and a shallower diffusion layer can be obtained as compared with the ion implantation method.

[0005]

Further, as a method for further reducing the junction depth between the source region and the drain region, a method as shown in FIG. 12 is proposed in, for example, Japanese Patent Laid-Open No. 1-125977. In this method, a conductive sub-gate 109 made of polysilicon is provided beside the gate electrode 103 via an insulating film 108, and a voltage is applied to the conductive sub-gate 109. According to this method, the substrate 101 under the sub-gate 109 is provided. A carrier inducing layer 111, which is an inversion layer in which carriers are induced and which is an inversion layer, is formed to form an extremely shallow conductive layer.

[0006]

Further, as another structure of a MOSFET having a shallow junction in which an inversion layer is formed, for example, in JP-A-1-232765, a material having a different work function, for example, a second gate electrode beside the first gate electrode is used. When the first gate electrode is formed of p-type silicon, n-type silicon is used for the second gate electrode, and when the first gate electrode is formed of n-type silicon, platinum is used for the second gate electrode. It is proposed that an inversion layer is formed under the second gate electrode by using it.

[0007]

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The above-mentioned conventional MOSFET has the following problems.

(1) In the low energy ion implantation method or the solid phase diffusion method, the junction depth of the diffusion layer cannot be 10 nm or less, and the sufficiently short channel effect can be suppressed in the MOSFET having a gate length of 0.1 μm or less. Can not. (2) In the structure in which the subgate is provided and the voltage is applied to form the inversion layer, the junction depth is shallow, but the voltage must be continuously applied to the subgate during operation, and the subgate, the gate electrode, and the subgate Since the parasitic capacitance is formed between the drain regions, the switching speed is reduced. (3) In the structure in which the second gate electrode having a different work function is provided, since the second gate electrode is connected to the gate electrode and has conductivity, the voltage is applied to the second gate electrode when the gate voltage is applied. Therefore, there is a parasitic capacitance between the second gate electrode and the channel, which causes a decrease in switching speed. Further, when the conductivity types of the gate electrode and the second gate electrode are different, it is necessary to introduce different impurities into the respective gate electrodes, which complicates the MOSFET forming process.

[0008]
An object of the present invention is to provide a MOSFET in which a junction depth of a diffusion layer sufficient to suppress a short channel effect is realized without causing problems such as a decrease in switching speed due to an increase in parasitic capacitance and a complicated manufacturing process. That is.

[0009]
To achieve the above object, a MOSFET of the present invention is provided with a gate electrode provided on a silicon substrate via a gate insulating film and a sidewall portion of the gate electrode. In a MOSFET having a gate side wall and a source region and a drain region provided on the silicon substrate, the gate side wall is formed of a non-conductive semiconductor layer having a band gap larger than that of silicon and impurities are introduced. It is characterized by

[0010]

Since the present invention uses a semiconductor having a bandgap larger than that of silicon on the gate side wall, when the impurity doped on the gate side wall is a donor, the energy of the electron is higher than the energy level of the conduction band of the silicon substrate. In the case of an acceptor, it is lower than the energy level of the valence band of the silicon substrate.

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Therefore, if the side wall of the gate is doped with a donor, electrons move and accumulate from the side wall of the gate to the silicon substrate therebelow due to the energy difference between the energy and the conduction band of the silicon substrate.

On the other hand, if the acceptor is doped, holes move and accumulate. Since a force acts on these electrons and holes so that they are pressed toward the side wall of the gate, these accumulation layers are thinly formed in a sheet shape, and the thickness thereof is 5 nm or less. Therefore, if this portion is used as the gate end of the source region or the drain region, an extremely thin source / drain region end of 5 nm or less can be formed, and the short channel effect can be suppressed.

[0011]
According to an embodiment of the present invention, the gate sidewalls are depleted to render them non-conductive.

[0012]
According to an embodiment of the present invention, between the gate sidewall and the gate electrode, or between the gate sidewall and the silicon substrate, or between the gate sidewall and the gate electrode and the gate sidewall and the silicon substrate. An insulating film is provided between them.

[0013]

In the present invention, an insulating film is provided between the gate side wall and the gate electrode or between the gate side wall and the silicon substrate.

Therefore, the insulation between the gate sidewall and the gate electrode or between the gate sidewall and the silicon substrate can be improved.

[0014]
Further, a method for manufacturing a MOSFET according to the present invention includes a gate electrode provided on a silicon substrate via a gate insulating film, and a semiconductor

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provided on a sidewall portion of the gate electrode and having a band gap larger than that of silicon and being non-conductive. In a method of manufacturing a MOSFET having a gate side wall formed of a layer and having impurities introduced therein, and a source region and a drain region provided on the silicon substrate, the impurity is introduced into the gate side wall by the source. The impurity ion implantation into the region and the drain region or the impurity ion implantation into the gate electrode is performed simultaneously.

[0015]
According to the present invention, the impurity is introduced into the side wall of the gate simultaneously with the impurity ion implantation into the source region and the drain region or the impurity ion implantation into the gate electrode.

[0016]
Therefore, it is possible to reduce the number of manufacturing steps, because a unique step of implanting ions into the gate sidewall is not required.

[0017]
Further, the MOSFET of the present invention includes a gate electrode provided on a silicon substrate via a gate insulating film, a gate sidewall provided on a sidewall portion of the gate electrode, and a source region provided on the silicon substrate. And a drain region, the gate sidewall is formed of a ferroelectric material, and when the silicon substrate is p-type, it is polarized in the direction from the gate electrode to the silicon substrate, and the silicon substrate is n-type. In this case, the polarization is performed in the direction from the silicon substrate to the gate electrode.

[0018]

Since the present invention uses the polarized ferroelectric on the gate sidewall, electrons or holes are induced on the silicon substrate side of the interface between the gate sidewall and the silicon substrate depending on the polarization direction, and the concentration per unit area is It will be about 1 x 1014 cm-2.

Then, a force acts on the electrons and holes so that they are pressed toward the side wall of the gate, so that these layers are thinly formed in a sheet shape, and the thickness thereof is 5 nm or less.

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Therefore, if this portion is used as the gate end of the source region or drain region, an extremely thin source / drain region end of 5 nm or less can be formed, and the short channel effect can be suppressed.

[0019]
According to an embodiment of the present invention, between the gate sidewall and the gate electrode, or between the gate sidewall and the silicon substrate, or between the gate sidewall and the gate electrode and the gate sidewall and the silicon substrate. An insulating film is provided between them.

[0020]

In the present invention, an insulating film is provided between the gate side wall and the gate electrode or between the gate side wall and the silicon substrate.

Therefore, the insulation between the gate sidewall and the gate electrode or between the gate sidewall and the silicon substrate can be improved.

[0021]
Further, the MOSFET of the present invention includes a gate electrode provided on a silicon substrate via a gate insulating film, a gate sidewall formed on a sidewall portion of the gate electrode and made of a ferroelectric material, and the silicon substrate. In a method of manufacturing a MOSFET having a source region and a drain region provided above, an interlayer insulating film is formed on the silicon substrate, a contact hole communicating with the silicon substrate is formed in the interlayer insulating film, and the contact is formed. Filling the hole with a metal to fill the contact; forming a first electrode on the upper portion of the gate sidewall through the interlayer insulating film; forming a second electrode on the upper portion of the contact filling; A voltage is applied between the first electrode and the second electrode to polarize the side wall of the gate.

[0022]
According to the present invention, an interlayer insulating film is formed on a silicon substrate, a contact buried for electrically connecting to the silicon substrate is provided in the interlayer

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insulating film, and a gate electrode upper part and a contact buried via the interlayer insulating film are provided respectively. An electrode is provided.

[0023]
Therefore, the gate sidewall can be polarized by applying a voltage between the two electrodes provided.

[0024]
Further, in the MOSFET of the present invention, a plurality of wells are provided on a silicon substrate, a plurality of gate electrodes provided on each of the wells via a plurality of gate insulating films, and a sidewall portion of each of the gate electrodes. In a method of manufacturing a MOSFET having a plurality of gate sidewalls formed of a ferroelectric material and a plurality of source regions and a plurality of drain regions provided on each well, an interlayer insulating film is formed on the silicon substrate. Forming a plurality of contact holes in the interlayer insulating film leading to the respective wells, filling the contact holes with a metal to form a contact buried, and forming the contact insulating film on the upper side wall of each gate via the interlayer insulating film. Forming a plurality of first electrodes and forming a plurality of second electrodes on top of the respective contact embeddings, and connecting the first electrodes to the second electrodes by wiring. And applying a voltage between the connected wirings to polarize the sidewalls of the gates.

[0025]
The present invention forms an interlayer insulating film on a silicon substrate for a plurality of MOSFETs provided on a plurality of wells of one silicon substrate, and electrically connects each well to the interlayer insulating film. In this structure, contact embedding is provided, and first and second electrodes are respectively provided on the upper part of the gate electrode and the contact embedding via the interlayer insulating film, and the first electrode and the second electrode are connected by wiring.

[0026]
Therefore, by applying a voltage between the two connected electrodes, it is possible to polarize the ferroelectric sidewalls of the plurality of MOSFETs at the same time.

[0027]
In addition, according to the embodiment of the present invention, the method further includes the step of removing the first and second electrodes.

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[0028]

According to the present invention, the first and second electrodes are removed after the polarization of the gate sidewall so as not to hinder the subsequent process.

Therefore, the manufacture of the MOSFET becomes easy.

[0029]
According to an embodiment of the present invention, the source region and the drain region outside the gate sidewall are formed of a metal material.

[0030]

In the present invention, the source region and the drain region are made of a metal material.

Therefore, the step of ion implantation becomes unnecessary and the number of steps for manufacturing MOSFET can be reduced.

[0031]

DESCRIPTION OF THE PREFERRED EMBODIMENTS Next, embodiments of the present invention will be described in detail with reference to the drawings.

(First Embodiment) FIG. 1 is a schematic sectional view showing a method for manufacturing a MOSFET according to a first embodiment of the present invention, and FIG. 2 is a schematic sectional view showing the structure of the MOSFET shown in FIG.

[0032]
A method of manufacturing the MOSFET of this embodiment will be described with reference to

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FIG.

[0033]
In this embodiment, a 5 nm-thick gate insulating film 2 made of silicon oxide is formed on a p-type silicon substrate 1 having an impurity concentration of about $1 \times 10\ 14\ cm\ -3$, and an n-type polysilicon film is formed on the insulating film 2. After 200 nm is formed, the gate electrode 3 is formed by etching through resist coating, exposure, and development steps (FIG. 1A).

[0034]
Next, after forming 50 nm of non-doped silicon carbide on the substrate 1, the gate sidewall 4 is formed by anisotropic etching (FIG. 1B).

[0035]

After that, arsenic or phosphorus is ion-implanted into the entire surface of the MOSFET to simultaneously introduce impurities into the gate electrode 3 and the gate sidewall 4 and simultaneously form the source region 5 and the drain region 6 on the surface of the substrate 1 (see FIG. c)).

After that, heat treatment is performed at 1000 ° C. for 30 seconds to activate the impurities.

[0036]
According to the above method, the impurity can be introduced into the gate sidewall 4 at the same time as the ion implantation into the source region 5 and the drain region 6, so that an increase in the number of steps can be avoided.

[0037]
The structure of the MOSFET of this embodiment will be described with reference to FIG.

[0038]

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In the MOSFET of the present embodiment, since the gate sidewall 4 is silicon carbide having a bandgap larger than that of silicon, electrons therein move to the surface of the substrate 1 formed of silicon having low energy, and the carrier inducing layer 7 is formed. To be done.

Since the carrier inducing layer 7 has a spread of only about a wave function of electrons, its thickness is as thin as 5 nm or less, and the short channel effect can be suppressed.

[0039]

Further, since the gate side wall 4 is formed of a semiconductor, it may have conductivity, and in that case, the gate side wall 4 becomes a part of the gate electrode 3 to substantially increase the gate length and the drain length. The gate sidewall 4 needs to have no conductivity because it causes an increase in capacitance with the region 6.

For that purpose, it is necessary to reduce the thickness of the gate side wall 4 to the extent that the donor and the acceptor are depleted.

[0040]

However, in this embodiment, since the thickness of the gate side wall 4 is as thin as 50 nm, all the electrons move to the substrate 1 and the gate side wall 4 is depleted and has no conductivity.

Therefore, the characteristics of the MOSFET are not deteriorated due to an increase in parasitic capacitance.

[0041]
In this embodiment, the impurity is described as the conductivity type in the case of the n-type MOSFET, but in the case of the p-type MOSFET, the impurity having the opposite conductivity type may be used.

[0042]

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Further, although silicon carbide is used as the material of the gate side wall 4 here, the same effect can be obtained by using a material having a band gap larger than that of silicon such as diamond, gallium arsenide, and indium phosphide.

However, it is necessary to use a process or material that does not allow the elements in it to diffuse into silicon.

(Second Embodiment) FIG. 3 is a schematic sectional view showing the structure of a MOSFET according to a second embodiment of the present invention.

The same numbers as in FIG. 2 indicate the same components.

[0043]
This embodiment is different from the first embodiment in FIG. 2 in that the insulating film 8 is a silicon oxide film having a thickness of about 5 nm through which carriers cannot pass after the gate electrode 3 is formed, and the gate sidewall 4 and the gate electrode 3 and the gate are formed. It is formed between the side wall 4 and the substrate 1.

[0044]
In the present embodiment, after forming the insulating film 8 and the gate side wall 4, the impurities can be ion-implanted into the entire surface of the MOSFET to introduce the impurity into the gate side wall 4 as in the first embodiment.

[0045]
The MOSFET of the present embodiment can suppress the short channel effect as in the first embodiment, and since the insulating film 8 is present, the gate side wall 4 and the gate electrode 3 and the gate side wall 4 and the substrate 1 are separated from each other. The insulating property of can be improved.

[0046]

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In this embodiment, the insulating film 8 is provided between the gate sidewall 4 and the gate electrode 3 and between the gate sidewall 4 and the substrate 1. However, between the gate sidewall 4 and the gate electrode 3 or between the gate sidewall 4 and the substrate 1. The insulating film 8 may be provided only on the above.

(Third Embodiment) FIG. 4 is a schematic sectional view showing a method for manufacturing a MOSFET according to a third embodiment of the present invention, and FIG. 5 is a schematic sectional view showing a polarization method for a ferroelectric sidewall 44 of the MOSFET shown in FIG. 6 is a schematic sectional view showing the polarization direction of the ferroelectric sidewall 44 of the MOSFET of FIG. 4, and FIG. 7 is a schematic sectional view showing the structure of the MOSFET of FIG.

[0047]
A method of manufacturing the MOSFET of this embodiment will be described with reference to FIG.

[0048]
In this embodiment, a 5 nm-thick gate insulating film 42 made of silicon oxide and an n-type polysilicon film are formed to a thickness of 200 nm on a p-type silicon substrate 41 having an impurity concentration of about 1 × 10 14 cm −3, and then resist coating is performed. The gate electrode 43 is formed by etching through the exposure and development processes (FIG. 4A).

[0049]
Next, a ferroelectric film 40 such as PZT is formed on the gate electrode 43 and the substrate 41 with a thickness of 50 nm (FIG. 4B), and the ferroelectric sidewall 44 is formed by anisotropic etching (FIG. 4B). 4 (c)).

[0050]

After that, the source region 45 and the drain region 46 can be formed by ion-implanting impurities on the surface of the substrate 41.

Then, heat treatment is performed at 1000 ° C. for 30 seconds to activate the impurities.

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[0051]

Next, a polarization method of the ferroelectric sidewall 44 of the MOSFET of this embodiment will be described with reference to FIG.

The same numbers as in FIG. 4 indicate the same components.

[0052]

After the MOSFET is formed on the substrate 41 together with the element isolation 93 and the contact layer 94, an interlayer insulating film 99 is formed, a contact hole leading to the substrate 41 is formed, and it is filled with tungsten or the like to form a contact embedding 100.

[0053]

The element isolation 93 is formed of SiO2 or the like and is for electrically isolating each MOSFET when a plurality of MOSFETs are formed on one chip.

[0054]

The contact layer 94 is a layer in which the same impurity as that of the substrate 41 is introduced at a high concentration in order to electrically connect the contact embedding 100 and the substrate 41 with low resistance.

[0055]

After that, the electrode 113 is formed on the contact embedding 100, and the electrode 112 is formed on the gate electrode 95 with the interlayer insulating film 99 sandwiched therebetween.

[0056]

Then, a voltage is applied between the electrode 112 and the electrode 113 to polarize the ferroelectric side wall 44.

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The voltage may be applied by making the electrode 112 positive with respect to the substrate 41 in the n-type MOSFET and making the electrode 112 negative with respect to the substrate 41 in the p-type MOSFET.

[0057]

The polarization of the ferroelectric side wall 44 is performed in the state of FIG. 5 or in the state where the process is further advanced.

When performing in the state of FIG. 5, the electrodes 112 and 113 formed on the interlayer insulating film 99 after polarization may be removed by etching or may be left.

However, removal of the electrodes 112 and 113 does not hinder the subsequent process and facilitates the manufacture of the MOSFET.

[0058]

In the present embodiment, the polarization method for one MOSFET is shown, but when a plurality of MOSFETs are formed on one semiconductor substrate, it is possible to simultaneously polarize the ferroelectric sidewalls of the plurality of MOSFETs. is there.

In this case, a plurality of wells are formed on the substrate, MOSFETs as shown in FIG. 5 are formed on the respective wells, electrodes formed on the gate electrodes of the plurality of MOSFETs are connected by wiring, and contacts are formed. If the electrodes formed on the buried layers are connected by wirings and a voltage is applied between the wirings, the ferroelectric sidewalls of a plurality of MOSFETs can be polarized at the same time.

[0059]

Next, the polarization direction of the ferroelectric sidewall 44 in the MOSFET of this embodiment will be described with reference to FIG.

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In FIG. 6, the arrow in the ferroelectric substance 44 indicates the polarization direction.

The same numbers as in FIG. 4 indicate the same components.

[0060]

FIG. 6A is a diagram showing the polarization direction in the n-type MOSFET, and the polarization direction of the ferroelectric side wall 44 is downward.

In this case, since the lower side of the ferroelectric side wall 44 is positively charged, negative charges (electrons) are accumulated in the substrate so as to cancel it and the electron inducing layer 49 is formed.

[0061]

FIG. 6B is a diagram showing the polarization direction in the p-type MOSFET, and the polarization direction of the ferroelectric side wall 44 is upward.

In this case, since the lower side of the ferroelectric side wall 44 is negatively charged, positive charges (holes) are accumulated in the substrate so as to cancel it and the hole inducing layer 50 is formed.

[0062]

Further, although the above polarization direction is perpendicular to the substrate 41, this is not always necessary, and there is no problem because carriers can be induced even if they are inclined by about 60 degrees from the vertical.

[0063]

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The structure of the MOSFET of this embodiment will be described with reference to FIG.

The same numbers as in FIG. 4 indicate the same components.

[0064]

In this embodiment, since the ferroelectric side wall 44 is formed on the side surface of the gate electrode 43, electrons are induced on the surface of the substrate 41 by polarization of the ferroelectric side wall 44 parallel to the direction of the substrate 41 from the gate electrode 43, and carrier The induction layer 47 is formed.

Since the carrier inducing layer 47 has a spread of only about the wave function of electrons, its thickness is as thin as 5 nm or less, and the short channel effect can be suppressed.

Since the ferroelectric side wall 44 is an insulator having no conductivity, it does not deteriorate MOSFET characteristics such as an increase in parasitic capacitance due to its formation.

[0065]

Here, the conductivity is described assuming that the impurity is an n-type MOSFET, but in the p-type MOSFET, an impurity having an opposite conductivity may be used.

(Fourth Embodiment) FIG. 8 is a schematic sectional view showing the structure of a MOSFET according to a fourth embodiment of the present invention.

The same numbers as in FIG. 7 indicate the same components.

[0066]

In this embodiment, in addition to the structure of the third embodiment of FIG. 7, the

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ferroelectric side wall 44 is formed by using a silicon oxide film having a thickness of about 5 nm through which the carriers cannot pass after forming the gate electrode 43 as the insulating film 48. And the gate electrode 43 and the ferroelectric side wall 44 and the substrate 41.

The MOSFET according to the present embodiment suppresses the short channel effect as in the fourth embodiment, and further has the insulating film 48. Therefore, the ferroelectric side wall 44 and the gate electrode 43 or the ferroelectric side wall 44 and the substrate 41. The insulation between them can be improved.

[0067]

In this embodiment, the insulating film 48 is provided between the gate sidewall 44 and the gate electrode 43 and between the gate sidewall 44 and the substrate 41. However, between the gate sidewall 44 and the gate electrode 43 or between the gate sidewall 44 and the substrate 41. The insulating film 48 may be provided only on the above.

(Fifth Embodiment) FIG. 9 is a schematic sectional view showing the structure of a MOSFET according to a fifth embodiment of the present invention. In this embodiment, a 5 nm-thick gate insulating film 72 made of silicon oxide and an n-type polysilicon film are formed to a thickness of 200 nm on a p-type silicon substrate 71 having an impurity concentration of about 1 × 10 14 cm −3, and then the resist is used as a resist. The gate electrode 73 is formed by etching through the steps of coating, exposing, and developing, the ferroelectric PZT film 100 nm is formed, and then the ferroelectric side wall 74 is formed by anisotropic etching, and then titanium is formed on the entire surface. The substrate 71 and titanium are reacted by a heat treatment at 800 ° C., and then the titanium reactant and titanium on the ferroelectric side wall 74 are stripped off by a hydrofluoric acid-based etching solution to form a source region 75 of a metal layer made of titanium silicide. And a drain region 76 of the metal layer is formed.

[0068]
A carrier inducing layer 77 is formed on the surface of the substrate 71 below the ferroelectric side wall 74, and its concentration is about 1 × 10 14 cm −2.

[0069]

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In the structure of this embodiment, the source region 75 and the drain region 76 made of a metal layer are formed outside the carrier inducing layer 77.

Usually, when metal and silicon are in contact with each other, a potential barrier called a Schottky barrier exists between them, and contact resistance occurs. The contact resistance deteriorates the characteristics of the MOSFET. However, when the impurity concentration on the semiconductor side is high, this potential barrier thickness becomes thin, resulting in a small contact resistance.

[0070]

In the case of the present embodiment, the concentration of the carrier inducing layer 77 is very high, and when converted into the concentration per unit volume, it is about $1 \times 10\ 20\ \mathrm{cm}\ -3$, so the contact resistance is almost zero compared to the channel resistance of the MOSFET. , MOSFET characteristics do not matter. Then, the short channel effect can be suppressed similarly to the fourth embodiment. Therefore, when the source region 75 and the drain region 76 are formed of a metal layer, the short channel effect can be suppressed, the step of ion implantation can be omitted, and the number of steps for manufacturing the MOSFET can be reduced.

[0071]

In the present embodiment, the case where the ferroelectric is used as the gate sidewall has been described. However, similar to the first embodiment, the band gap is larger than that of silicon, and the same effect can be obtained when a semiconductor doped with impurities is used. ..

[0072]

As described above, according to the present invention, it is possible to form a part of the shallow source region and the drain region on the upper part of the substrate at the gate end, and in the MOSFET having the gate length of $0.1\ \mu\mathrm{m}$ or less, the parasitic It has an effect that the short channel effect can be suppressed without increasing the resistance.

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CLAIMS JPH10209445

1.
In a MOSFET having a gate electrode provided on a silicon substrate via a gate insulating film, a gate sidewall provided on a sidewall of the gate electrode, and a source region and a drain region provided on the silicon substrate. A MOSFET characterized in that the gate side wall is formed of a non-conductive semiconductor layer having a band gap larger than that of silicon and impurities are introduced.

2.
The MOSFET according to claim 1, wherein the gate sidewall is depleted to be non-conductive.

3.
An insulating film is provided between the gate sidewall and the gate electrode, between the gate sidewall and the silicon substrate, or between the gate sidewall and the gate electrode and between the gate sidewall and the silicon substrate. 1. The MOSFET according to 1 or 2.

4.
A gate electrode provided on a silicon substrate via a gate insulating film and a sidewall portion of the gate electrode, formed of a non-conductive semiconductor layer having a bandgap larger than that of silicon and impurities introduced thereinto. In a method of manufacturing a MOSFET having a gate side wall and a source region and a drain region provided on the silicon substrate, introducing an impurity into the gate side wall is performed by implanting impurity ions into the source region and the drain region. A method for manufacturing a MOSFET, which is performed

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simultaneously with the impurity ion implantation into the gate electrode.

5.

In a MOSFET having a gate electrode provided on a silicon substrate via a gate insulating film, a gate sidewall provided on a sidewall of the gate electrode, and a source region and a drain region provided on the silicon substrate. , The gate sidewall is formed of a ferroelectric material, and is polarized in the direction from the gate electrode to the silicon substrate when the silicon substrate is p-type, and is gated from the silicon substrate when the silicon substrate is n-type. A MOSFET characterized by being polarized in the direction of the electrodes.

6.

An insulating film is provided between the gate sidewall and the gate electrode, between the gate sidewall and the silicon substrate, or between the gate sidewall and the gate electrode and between the gate sidewall and the silicon substrate. 5. The MOSFET according to item 5.

7.

A gate electrode provided on a silicon substrate via a gate insulating film; a gate sidewall provided on a sidewall portion of the gate electrode and made of a ferroelectric material; and a source region provided on the silicon substrate. In a method of manufacturing a MOSFET having a drain region, an interlayer insulating film is formed on the silicon substrate, a contact hole communicating with the silicon substrate is formed in the interlayer insulating film, and the contact hole is filled with metal to fill the contact. And a step of forming a first electrode on the upper side wall of the gate via the interlayer insulating film, and forming a second electrode on the upper side of the contact embedding, the first electrode and the second electrode. A voltage is applied between the gate electrode and the electrode to polarize the side wall of the gate.

8.

A plurality of wells are provided on a silicon substrate, a plurality of gate electrodes are provided on each of the wells via a plurality of gate insulating films, and a ferroelectric material is provided on sidewalls of the gate electrodes. In a method of manufacturing a MOSFET having a plurality of gate sidewalls, a plurality of source regions and a plurality of drain regions provided on each well, an interlayer insulating film is formed on the silicon substrate, and the interlayer insulating film is formed. A step of forming a plurality of contact holes communicating with the respective wells in the film, burying the contact holes with a metal for contact filling, and forming a plurality of first electrodes on the upper portions of the respective gate sidewalls through the interlayer insulating film. Forming and forming a plurality of second electrodes on top of the respective contact embeddings; connecting the respective first electrodes to the respective

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second electrodes by wiring, and connecting the respective wirings And a voltage is applied between the gates to polarize the sidewalls of the gates.

9.

9. The method of manufacturing a MOSFET according to claim 7, further comprising a step of removing the first and second electrodes.

10.

10. The MOSFET according to claim 1, wherein the source region and the drain region outside the gate sidewall are formed of a metal material.

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(71)出願人　000002185
ソニー株式会社
東京都品川区北品川６丁目７番35号

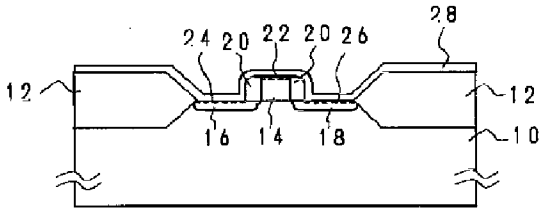
(72)発明者　千葉　安浩
東京都品川区北品川６丁目７番35号　ソニー株式会社内

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】

【課題】　本発明は、シリサイド膜を形成する際に、リーク電流の発生原因となるシリサイドのスパイクが形成されることを防止し、信頼性が高く、高速な半導体装置の製造方法を提供することを目的とする。

【解決手段】　ＲＴＡ法を用いたNH_3雰囲気ガス中における熱処理により、多結晶シリコン層からなるゲート電極１４並びにシリコン基板１０表層部のソース領域１６及びドレイン領域１８上にスパイク防止用のＳｉＮ薄膜２２、２４、２６を形成した後、基体全面にＣｏ膜２８を成膜し、第１回目のＲＴＡ法を用いたアニール処理によりＣｏ膜２８を下地のＳｉと反応させてＣｏＳｉ膜３０、３２、３４を形成する。このとき、ゲート電極１４並びにソース領域１６及びドレイン領域１８とＣｏ膜２８と間にＳｉＮ薄膜２２、２４、２６が介在し、局所的なＣｏ原子の異常拡散を抑制し、Ｃｏシリサイドのスパイクの形成を防止する。



10・・・Si基板　18・・・ドレイン領域
12・・・LOCOS膜　20・・・サイドウオール
14・・・ゲート電極　22、24、26・・・SiN薄膜
16・・・ソース領域　28・・・Co膜

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【特許請求の範囲】
【請求項１】　シリコン領域を含む基体全面に金属膜を形成した後、熱処理により前記金属膜と前記シリコン領域のＳｉとを反応させ、前記シリコン領域上にシリサイド膜を自己整合的に形成する半導体装置の製造方法であって、
前記シリコン領域を含む基体全面に前記金属膜を形成する前に、前記シリコン領域上にスパイク防止用の薄膜を形成する工程が含まれることを特徴とする半導体装置の製造方法。
【請求項２】　請求項１記載の半導体装置の製造方法において、
前記金属膜が、Ｃｏ膜であることを特徴とする半導体装置の製造方法。
【請求項３】　請求項１記載の半導体装置の製造方法において、
前記スパイク防止用の薄膜が、ＳｉＮ膜からなることを特徴とする半導体装置の製造方法。
【請求項４】　請求項３記載の半導体装置の製造方法において、
前記ＳｉＮ膜からなるスパイク防止用の薄膜を形成する工程が、短時間熱処理法を用いて、前記シリコン領域を含む基体全面に対してNH_3雰囲気中におけるアニール処理を行い、前記シリコン領域表面に前記ＳｉＮ膜を形成する工程であることを特徴とする半導体装置の製造方法。
【請求項５】　請求項２記載の半導体装置の製造方法において、
前記シリコン領域を含む基体全面に前記Ｃｏ膜を形成した後に、前記Ｃｏ膜上に酸化防止用の薄膜を形成する工程が含まれることを特徴とする半導体装置の製造方法。
【請求項６】　請求項５記載の半導体装置の製造方法において、
前記酸化防止用の薄膜が、ＴｉＮ膜からなることを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置の製造方法に係り、特にシリコン領域を含む基体全面に金属膜を形成し、熱処理により金属とＳｉ（シリコン）とを反応させてシリコン領域上にシリサイド膜を自己整合的に形成する、いわゆるサリサイド（ＳＡＬＩＣＩＤＥ；Self-Alinged Slicide）プロセスに関するものである。
【０００２】
【従来の技術】昨今の半導体デバイスの低抵抗化、高速化の要求から、ゲート（Gate）及びソース／ドレイン（Ｓ／Ｄ）領域上に低抵抗シリサイド膜を自己整合的に形成するサイサイド技術が注目されている。このような場合のシリサイド材料としては、Ｔｉ（チタン）シリサイドやＣｏ（コバルト）シリサイド等が活発に検討されている。
【０００３】しかし、Ｔｉシリサイドの場合、図１５のグラフに示されるように、n^+型拡散層上にＴｉシリサイド膜を形成すると、初期Ｔｉ膜の膜厚が厚くなるほどＴｉシリサイド膜のシート抵抗Ｒｓは減少するが、n^+型拡散層の幅Ｗが狭くなるほどＴｉシリサイド膜のシート抵抗Ｒｓは増大する傾向になる。そして、このＴｉシリサイド膜のシート抵抗Ｒｓの線幅依存性は、初期Ｔｉ膜の膜厚が厚くなるほど大きい。
【０００４】また、図１６のグラフに示されるように、p^+型拡散層上にＴｉシリサイド膜を形成する際にも、n^+型拡散層上に形成する場合と同様に、Ｔｉシリサイド膜のシート抵抗Ｒｓの線幅依存性が現れる。こうして、微細なライン上にＴｉシリサイド膜を形成する場合においては、そのシート抵抗Ｒｓが上昇する、いわゆる細線効果を生じることになる。
【０００５】これに対して、Ｃｏシリサイドの場合は、図１７のグラフに示されるように、n^+型拡散層上にＣｏシリサイド膜を形成すると、初期Ｃｏ膜の膜厚が厚くなるほどＣｏシリサイド膜のシート抵抗Ｒｓは減少するが、n^+型拡散層の幅Ｗが狭くなってもＣｏシリサイド膜のシート抵抗Ｒｓは殆ど変動しない。そして、このようにＣｏシリサイド膜のシート抵抗Ｒｓが線幅依存性を有していないことは、図１８のグラフに示されるように、p^+型拡散層上にＣｏシリサイド膜を形成する際も同様である。
【０００６】なお、上記図１７及び図１８のグラフにおいては、Ｃｏシリサイド膜を形成する際にＣｏ膜上にＴｉＮ膜を被せた、いわゆるＴｉＮキャップ（ｃａｐ）構造の場合のデータを示しているが、ＴｉＮ膜のないＣｏ膜だけを用いてＣｏシリサイド膜を形成する場合においても、基本的には同様の特性を示す。従って、微細なライン上にＣｏシリサイド膜を形成する場合にも、そのシート抵抗Ｒｓが上昇する細線効果を生じることはない。
【０００７】このように、微細なライン上に形成しても細線効果が生じないことから、最近においてはＣｏシリサイド膜についてより活発に検討されるようになっている。以下、従来のＣｏシリサイド・プロセスを図１９～図２２を用いて説明する。
【０００８】先ず、例えばＬＯＣＯＳ（Local Oxidation of Slicon ；選択酸化）法を用いて、シリコン基板５０上にＬＯＣＯＳ膜５２を選択的に形成して素子分離を行った後、素子領域のシリコン基板５０上に、ゲート酸化膜（図示せず）を介して、多結晶シリコン層からなるゲート電極５４を形成する。続いて、例えばイオン注入法を用いて、ＬＯＣＯＳ膜５２及びゲート電極５４をマスクに素子領域のシリコン基板５０表層部に不純物を選択的に添加して、ソース領域５６及びドレイン領域５８を形成する。続いて、基体全面にSiO_2膜（シリコン酸化膜）を堆積した後、ドライエッチング法により、こ

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のＳｉO_2膜をエッチング除去すると共に、ゲート電極５４側面にＳｉO_2膜を残存させ、ゲート電極５４側面にＳｉO_2膜からなるサイドウォール６０を形成する（図１９参照）。

【０００９】次いで、例えばスパッタ法を用いて、基体全面にＣｏ膜６２を一様に成膜する（図２０参照）。次いで、ＲＴＡ（Rapid Thermal Annealing ；短時間熱処理）法を用い、処理温度５５０℃程度の条件において、第１回目のアニール処理を行い、ゲート電極５４並びにソース領域５６及びドレイン領域５８上のＣｏ膜６２を下地のＳｉと反応させ、高抵抗のＣｏシリサイドであるＣｏＳｉ膜６４、６６、６８をそれぞれ形成する。このとき、ＬＯＣＯＳ膜５２及びサイドウォール６０上には、Ｃｏ膜６２が未反応なままの状態で残存する（図２１参照）。

【００１０】次いで、ウェット（ｗｅｔ）エッチング法を用いて、ＬＯＣＯＳ膜５２及びサイドウォール２０上に未反応のまま残っているＣｏ膜６２を選択的にエッチング除去する（図２２参照）。次いで、ＲＴＡ法を用い、処理温度７００℃程度の条件において、第２回目のアニール処理を行い、高抵抗のＣｏシリサイドであるＣｏＳｉ膜６４、６６、６８をＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$膜７０、７２、７４に相転移する（図２３参照）。

【００１１】即ち、この従来のＣｏシリサイド・プロセスは、ＬＯＣＯＳ法、イオン注入法、ドライエッチング法等を用いて、ＬＯＣＯＳ膜５２によって分離された素子領域のシリコン基板５０上にゲート酸化膜を介して多結晶シリコン層からなるゲート電極５４を形成し、シリコン基板５０表層部にソース領域５６及びドレイン領域５８を形成し、ゲート電極５４側面にサイドウォール６０を形成する工程と、スパッタ法を用いて、基体全面にＣｏ膜６２を成膜する工程と、ＲＴＡ法を用いた第１回目のアニール処理により、ゲート電極５４並びにソース領域５６及びドレイン領域５８上のＣｏ膜６２を下地のＳｉと反応させ、高抵抗のＣｏシリサイドであるＣｏＳｉ膜６４、６６、６８をそれぞれ形成する工程と、ウェットエッチング法を用いて、ＬＯＣＯＳ膜５２及びサイドウォール６０上の未反応Ｃｏ膜６２を除去した後、ＲＴＡ法を用いた第２回目のアニール処理により、ＣｏＳｉ膜６４、６６、６８をＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$膜７０、７２、７４にそれぞれ相転移する工程との４つの主要な工程からなる。

【００１２】このように、従来のＣｏシリサイド・プロセスにおいては、$CoSi_2$膜７０、７２、７４を形成するためのＲＴＡ法によるアニール処理を行う際に、Ｃｏ膜６２を下地のＳｉと反応させてＣｏＳｉ膜６４、６６、６８をそれぞれ形成する処理温度５５０℃程度の第１回目のアニール処理と、これらのＣｏＳｉ膜６４、６６、６８を$CoSi_2$膜７０、７２、７４に相転移する処理温度７００℃程度の第２回目のアニール処理との２段階に分けていることにより、ゲート電極５４並びにソース領域５６及びドレイン領域５８上にＣｏＳｉ膜６４、６６、６８が形成されるだけでなく、隣接するサイドウォール６０上にまでＣｏＳｉ膜が形成される、いわゆる這い上がり現象の発生が防止される。このため、サイドウォール２０上に形成されたＣｏＳｉ膜を介してゲート電極１４上のＣｏＳｉ膜３０とソース領域１６及びドレイン領域１８上のＣｏＳｉ膜３２、３４とが短絡する、即ちゲート電極１４とソース領域１６及びドレイン領域１８とが短絡する、いわゆるブリッジング現象が発生することもなく、ゲート電極５４並びにソース領域５６及びドレイン領域５８上に低抵抗の$CoSi_2$膜７０、７２、７４が自己整合的に形成される。

【００１３】

【発明が解決しようとする課題】しかしながら、上記従来のＣｏシリサイド・プロセスにおいては、図２４及び図２５のグラフに示されるように、n^+型拡散層及びp^+型拡散層上にそれぞれＣｏシリサイド膜を形成すると、これらのn^+型拡散層及びp^+型拡散層においてばらつきの大きなリーク電流が発生する。特に、n^+型拡散層上にＣｏシリサイド膜を形成する場合には、n^+型拡散層上に形成したＣｏ膜をシリサイド化する際のアニール処理温度によりリーク電流の発生に大きな差異が生じる。即ち、アニール処理温度が４００℃から４５０℃に上昇すると、リーク電流は急激に増大する。そして、アニール処理温度が４５０℃から更に７００℃に上昇するにつれて、リーク電流は僅かながら減少する傾向を示す。

【００１４】このようなことから、図２６に示されるように、例えばn^+型拡散層７６上にＣｏシリサイド膜７８を形成する際に発生するリーク電流は、４５０℃近傍の比較的低温のアニール処理温度においてn^+型拡散層７６中に形成されるＣｏシリサイドのスパイク８０に起因すると考えられている（K.Goto,et al., “LeakageMechanism and Optimized Conditions of Co Process for Deep-Submicron CMOSDevices” IEDM (1995) p.449 参照）。そして、このＣｏシリサイドのスパイク８０の形成は、Ｃｏ原子がn^+型拡散層７６中に異常拡散して、その部分だけにＣｏシリサイドが形成されるためであると考えられている。従って、Ｃｏシリサイドは、上述のように細線効果がないことから今後更に微細化する半導体デバイスへの適用を考えた場合に極めて有利である反面、シリサイド化反応の初期において発生するＣｏシリサイドのスパイクに起因するリーク電流の発生が実デバイスへの適用の大きな障害となっている。

【００１５】そこで本発明は、上記事情を鑑みてなされたものであり、シリサイド膜を形成する際に、リーク電流の発生原因となるシリサイドのスパイクが形成されることを防止し、信頼性が高く、高速な半導体装置の製造

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方法を提供することを目的とする。

【００１６】

【課題を解決するための手段】上記課題は、以下の本発明に係る半導体装置の製造方法により達成される。即ち、請求項１に係る半導体装置の製造方法は、シリコン領域を含む基体全面に金属膜を形成した後、熱処理により金属膜とシリコン領域のＳｉとを反応させ、シリコン領域上にシリサイド膜を自己整合的に形成する半導体装置の製造方法であって、シリコン領域を含む基体全面に金属膜を形成する前に、シリコン領域上にスパイク防止用の薄膜を形成する工程が含まれることを特徴とする。

【００１７】このように請求項１に係る半導体装置の製造方法においては、シリコン領域を含む基体全面に金属膜を形成する前に、このシリコン領域上にスパイク防止用の薄膜を形成することにより、熱処理によりシリコン領域のＳｉと金属とを反応させる際に、シリコン領域と金属膜との間にスパイク防止用の薄膜が介在することになるため、シリサイド化反応の初期において発生する局所的な金属原子の異常拡散が抑制され、金属原子が均一に拡散して、シリサイドのスパイクの形成が防止される。従って、このシリサイドのスパイクに起因するリーク電流の発生が防止される。

【００１８】なお、ここで、シリコン領域とは、多結晶シリコン領域及び単結晶シリコン領域の両方を含むものとする。また、シリコン領域と金属膜と間に介在するスパイク防止用の薄膜はその膜厚が極めて薄くなっているため、Ｓｉと金属とのシリサイド化反応を阻止するものではない。

【００１９】また、請求項２に係る半導体装置の製造方法は、上記請求項１に係る半導体装置の製造方法において、金属膜がＣｏ膜である構成とすることにより、Ｓｉとの反応によりシリサイド膜が形成される際、特にシリサイドのスパイクが形成され易いＣｏ膜の場合であっても、シリコン領域とＣｏ膜と間にスパイク防止用の薄膜が介在しているため、シリサイド化反応の初期において発生する局所的なＣｏ原子の異常拡散が抑制され、Ｃｏ原子が均一に拡散して、Ｃｏシリサイドのスパイクの形成が防止される。従って、このＣｏシリサイドのスパイクに起因するリーク電流の発生が防止される。

【００２０】また、請求項３に係る半導体装置の製造方法は、上記請求項１に係る半導体装置の製造方法において、スパイク防止用の薄膜がＳｉＮ膜（シリコン窒化膜）からなる構成とすることにより、例えばシリコン領域と金属膜と間に自然酸化膜が介在する場合のようにシリサイド化反応を妨害することがないため、シリコン領域と金属膜との間に介在するＳｉＮ膜は、局所的な金属原子の異常拡散を抑制するというシリサイド膜を形成する際のスパイク防止用薄膜としての機能を良好に発揮する。

【００２１】また、請求項４に係る半導体装置の製造方法は、上記請求項３に係る半導体装置の製造方法において、ＳｉＮ膜からなるスパイク防止用の薄膜を形成する工程が、ＲＴＡ法を用いて、シリコン領域を含む基体全面に対してNH_3（アンモニア）雰囲気中におけるアニール処理を行い、シリコン領域表面にＳｉＮ膜を形成する工程である構成とすることにより、Ｓｉと金属とのシリサイド化反応を阻止することなく、且つシリサイド膜を形成する際のスパイク防止用薄膜として機能するのに必要十分な膜厚をもつ緻密なＳｉＮ膜が容易に形成される。

【００２２】また、請求項５に係る半導体装置の製造方法は、上記請求項２に係る半導体装置の製造方法において、シリコン領域を含む基体全面にＣｏ膜を形成した後に、このＣｏ膜上に酸化防止用の薄膜を形成する工程が含まれる構成とすることにより、本来Ｃｏは非常に酸化され易い金属膜であるが酸化防止用の薄膜によって覆われるため、Ｃｏ膜が大気暴露によって表面酸化されることから保護される。なお、このＣｏ膜の酸化防止用の薄膜としては、ＴｉＮ膜が好適である。

【００２３】

【発明の実施の形態】以下、添付図面を参照しながら、本発明の実施の形態を説明する。

（第１の実施形態）図１～図６は、それぞれ本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図である。先ず、例えばＬＯＣＯＳ法を用いて、シリコン基板１０上にＬＯＣＯＳ膜１２を選択的に形成し、素子分離を行う。その後、ＬＯＣＯＳ膜１２によって分離された素子領域のシリコン基板１０上に、ゲート酸化膜（図示せず）を介して多結晶シリコン層からなるゲート電極１４を形成する。

【００２４】続いて、例えばイオン注入法を用いて、ＬＯＣＯＳ膜１２及びゲート電極１４をマスクに素子領域のシリコン基板１０表層部に不純物を選択的に添加して、ソース領域１６及びドレイン領域１８を形成する。続いて、基体全面にSiO_2膜を堆積した後、ドライエッチング法により、このSiO_2膜をエッチング除去すると共に、ゲート電極１４側面にこのSiO_2膜を残存させる。こうして、ゲート電極１４側面にSiO_2膜からなるサイドウォール２０を形成する（図１参照）。

【００２５】次いで、ＲＴＡ法を用いて、ゲート電極１４上面並びにソース領域１６及びドレイン領域１８表面が露出している基体全体をNH_3雰囲気中において熱処理する。こうして、ゲート電極１４上面並びにソース領域１６及びドレイン領域１８表面を窒化して、膜厚１．５ｎｍの緻密なＳｉＮ薄膜２２、２４、２６をそれぞれ形成する（図２参照）。なお、これらの膜厚１．５ｎｍのＳｉＮ薄膜２２、２４、２６を形成する際のＲＴＡ法を用いた熱処理条件は、

NH_3雰囲気ガス流量：５ｓｃｃｍ

処理温度：９００℃

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処理時間：３０秒
である。
【００２６】次いで、例えばスパッタ法を用いて、基体全面に膜厚１０ｎｍのＣｏ膜２８を一様に成膜する（図３参照）。なお、この膜厚１０ｎｍのＣｏ膜２８を形成する際の成膜条件は、
ＤＣパワー：０．８ｋＷ
圧力：０．４Ｐａ
ヒータ用のＡｒ（アルゴン）ガス流量：３０ｓｃｃｍ
プロセス用のＡｒガス流量：６０ｓｃｃｍ
基板加熱温度：１５０℃
である。
【００２７】次いで、ＲＴＡ法を用いて、全面にＣｏ膜２８が成膜された基体に対してN_2（窒素）雰囲気中における第１回目のアニール処理を行い、ゲート電極１４並びにソース領域１６及びドレイン領域１８上のＣｏ膜２８を下地のＳｉと反応させて、高抵抗のＣｏシリサイドであるＣｏＳｉ膜３０、３２、３４をそれぞれ形成する。このとき、ＬＯＣＯＳ膜１２及びサイドウォール２０上には、Ｃｏ膜２８が未反応なままの状態で残存している（図４参照）。なお、これらのＣｏＳｉ膜３０、３２、３４を形成する際の第１回目のＲＴＡ法を用いたアニール処理条件は、
N_2 雰囲気ガス流量：１０ｓｃｃｍ
処理温度：５５０℃
処理時間：３０秒
である。
【００２８】このとき、ゲート電極１４の多結晶シリコン面並びにソース領域１６及びドレイン領域１８の単結晶シリコン面（以下、多結晶シリコン面及び単結晶シリコン面の両方を併せて単に「シリコン面」という）とＣｏ膜２８との間にはそれぞれＳｉＮ薄膜２２、２４、２６が介在しているものの、これらのＳｉＮ薄膜２２、２４、２６はその膜厚が１．５ｎｍと極めて薄いため、Ｃｏ膜２８がゲート電極１４並びにソース領域１６及びドレイン領域１８のシリコン面と反応することを阻止することはない。
【００２９】また、上記の条件において第１回目のアニール処理を行うと、従来の場合は、上記図２６に示されるように、ＣｏＳｉのスパイクが形成されるのが通常であったが、本実施形態においては、Ｃｏ膜２８とその下地のシリコン面との間にそれぞれＳｉＮ薄膜２２、２４、２６が介在していることにより、局所的なＣｏ原子の異常拡散が抑制され、Ｃｏ原子が均一に拡散するため、ＣｏＳｉのスパイクが形成されることはなくなる。即ち、ＳｉＮ薄膜２２、２４、２６は、ＣｏＳｉ膜３０、３２、３４を形成する際のスパイク防止用薄膜として機能する。
【００３０】また、本実施形態においては、処理温度５５０℃、処理時間３０秒という条件においてアニール処理を行っているため、サイドウォール２０上にもＣｏＳｉ膜が形成されてゲート電極１４上のＣｏＳｉ膜３０とソース領域１６及びドレイン領域１８上のＣｏＳｉ膜３２、３４とが短絡する、即ちゲート電極１４とソース領域１６及びドレイン領域１８とが短絡する、いわゆるＣｏＳｉ膜の這い上がりによるブリッジング現象が起きることもない。
【００３１】次いで、ウェットエッチング法を用いて、ＬＯＣＯＳ膜１２及びサイドウォール２０上に未反応のままの状態で残存しているＣｏ膜２８を選択的にエッチング除去する（図５参照）。なお、この未反応Ｃｏ膜２８のウェットエッチング条件は、
薬液：硫酸過水（H_2SO_4：H_2O_2＝４：１）
薬液温度：７０℃
処理時間：３分
である。
【００３２】次いで、ＲＴＡ法を用いて、ゲート電極１４並びにソース領域１６及びドレイン領域１８上にそれぞれＣｏＳｉ膜３０、３２、３４が形成された基体に対してN_2 雰囲気中における第２回目のアニール処理を行い、これらのＣｏＳｉ膜３０、３２、３４をＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$ 膜３６、３８、４０に相転移する（図６参照）。
【００３３】なお、これらのＣｏＳｉ膜３０、３２、３４を$CoSi_2$ 膜３６、３８、４０に相転移する際の第２回目のアニール処理条件は、
N_2 雰囲気ガス流量：１０ｓｃｃｍ
処理温度：７００℃
処理時間：３０秒
である。
【００３４】以上のように本実施形態によれば、ＲＴＡ法を用いたNH_3 雰囲気中における熱処理により、多結晶シリコン層からなるゲート電極１４並びにシリコン基板１０表層部のソース領域１６及びドレイン領域１８上に膜厚１．５ｎｍのＳｉＮ薄膜２２、２４、２６を形成した後、基体全面に膜厚１０ｎｍのＣｏ膜２８を成膜し、第１回目のＲＴＡ法を用いたアニール処理によりＣｏ膜２８を下地のＳｉと反応させて、高抵抗のＣｏシリサイドであるＣｏＳｉ膜３０、３２、３４を形成し、第２回目のＲＴＡ法を用いたアニール処理によりＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$ 膜３６、３８、４０に相転移しているが、第１回目のＲＴＡ法を用いたアニール処理によりＣｏ膜２８と下地のＳｉとを反応させる際に、ゲート電極１４並びにソース領域１６及びドレイン領域１８とＣｏ膜２８と間にスパイク防止用のＳｉＮ薄膜２２、２４、２６が介在していることにより、局所的なＣｏ原子の異常拡散が抑制され、Ｃｏ原子が均一に拡散して、Ｃｏシリサイドのスパイクの形成を防止することができるため、このＣｏシリサイドのスパイクに起因するリーク電流の発生を防止することがで

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き、半導体デバイスの信頼性を向上させることが可能になる。

【００３５】また、このようにリーク電流の発生を防止することができることから、低抵抗の$CoSi_2$膜３６、３８、４０の膜厚を更に十分に厚くすることが可能になるため、これらの$CoSi_2$膜３６、３８、４０を形成したゲート電極１４並びにソース領域１６及びドレイン領域１８の抵抗を更に低減することができ、半導体デバイスの動作速度を更に高速化することが可能になる。

【００３６】（第２の実施形態）図７～図１４は、それぞれ本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図である。なお、上記図１～図６に示す構成要素と同一の要素には同一の符号を付して説明を省略する。先ず、ＬＯＣＯＳ法を用いて、シリコン基板１０上にＬＯＣＯＳ膜１２を選択的に形成し、素子分離を行った後、ＬＯＣＯＳ膜１２によって分離された素子領域のシリコン基板１０上に、ゲート酸化膜（図示せず）を介して多結晶シリコン膜からなるゲート電極１４を形成する。

【００３７】続いて、イオン注入法を用い、素子領域のシリコン基板１０表層部に不純物を選択的に添加し、ソース領域１６及びドレイン領域１８を形成した後、SiO_2膜の堆積及びそのドライエッチングにより、ゲート電極１４側面にSiO_2膜からなるサイドウォール２０を形成する（図７参照）。

【００３８】次いで、ＲＴＡ法を用いて、基体全体をNH_3雰囲気中において熱処理して、ゲート電極１４上面並びにソース領域１６及びドレイン領域１８表面を窒化し、膜厚１．５ｎｍの緻密なＳｉＮ薄膜２２、２４、２６をそれぞれ形成する（図８参照）。なお、これら膜厚１．５ｎｍのＳｉＮ薄膜２２、２４、２６を形成する際のＲＴＡ処理条件は、上記第１の実施形態の場合と同様である。

【００３９】次いで、スパッタ法を用いて、基体全面に膜厚１０ｎｍのＣｏ膜２８を一様に成膜する（図９参照）。なお、この膜厚１０ｎｍのＣｏ膜２８を形成する際の成膜条件は、上記第１の実施形態の場合と同様である。

【００４０】次いで、例えばスパッタ法を用いて、Ｃｏ膜２８を一様に成膜した基体を大気開放することなく、このＣｏ膜２８上に膜厚２０ｎｍのＴｉＮキャップ膜４２を成膜する（図１０参照）。なお、このＴｉＮキャップ膜４２を形成する際の成膜条件は、

ＤＣパワー：６．５ｋＷ
圧力：０．４Ｐａ
ヒータ用のＡｒガス流量：１５ｓｃｃｍ
プロセス用のN_2ガス流量：１３５ｓｃｃｍ
基板加熱温度：１５０℃
である。

【００４１】このとき、前の工程におけるスパッタチャンバ内において基体全面に成膜されたＣｏ膜２８は、大気開放されることなく、その全面がＴｉＮキャップ膜４２によって覆われるため、本来は非常に酸化され易い金属膜であるＣｏ膜２８が大気暴露されてその表面が酸化されることから保護される。即ち、ＴｉＮキャップ膜４２は、Ｃｏ膜２８の酸化防止用膜として機能する。

【００４２】次いで、ＲＴＡ法を用いて、全面にＣｏ膜２８及びＴｉＮキャップ膜４２が順に積層された基体に対してN_2雰囲気中における第１回目のアニール処理を行い、ゲート電極１４並びにソース領域１６及びドレイン領域１８上のＣｏ膜２８を下地のＳｉと反応させて、高抵抗のＣｏシリサイドであるＣｏＳｉ膜３０、３２、３４をそれぞれ形成すると共に、ＬＯＣＯＳ膜１２及びサイドウォール２０上には、未反応Ｃｏ膜２８を残存する（図１１参照）。なお、これらのＣｏＳｉ膜３０、３２、３４を形成する際の第１回目のアニール処理条件は、上記第１の実施形態の場合と同様である。

【００４３】このとき、上記第１の実施形態の場合と同様にして、ゲート電極１４並びにソース領域１６及びドレイン領域１８のシリコン面とＣｏ膜２８との間にはスパイク防止用薄膜として機能する膜厚１．５ｎｍのＳｉＮ薄膜２２、２４、２６がそれぞれ介在していることにより、ゲート電極１４並びにソース領域１６及びドレイン領域１８のシリコン面とＣｏ膜２８との反応を阻止することなく、局所的なＣｏ原子の異常拡散を抑制してＣｏ原子を均一に拡散させるため、ＣｏＳｉ膜３０、３２、３４が形成されると共に、ＣｏＳｉのスパイクの形成が防止される。また、本実施形態においても、上記第１の実施形態の場合と同様に、処理温度５５０℃、処理時間３０秒という条件においてアニール処理を行っているため、ＣｏＳｉ膜の這い上がりによるブリッジング現象が起きることもない。

【００４４】次いで、例えばウェットエッチング法を用いて、Ｃｏ膜２８の酸化防止用膜としてＣｏ膜２８上に成膜したＴｉＮキャップ膜４２をエッチング除去する（図１２参照）。なお、このＴｉＮキャップ膜４２のウェットエッチング条件は、

薬液：アンモニア過水（$NH_4OH:H_2O_2:H_2O$＝１：２：６）
薬液温度：６５℃
処理時間：３分
である。

【００４５】次いで、ウェットエッチング法を用いて、ＬＯＣＯＳ膜１２及びサイドウォール２０上の未反応Ｃｏ膜２８を選択的にエッチング除去する（図１３参照）。なお、この未反応Ｃｏ膜２８のウェットエッチング条件は、上記第１の実施形態の場合と同様である。

【００４６】次いで、ＲＴＡ法を用いて、ゲート電極１４並びにソース領域１６及びドレイン領域１８上にそれ

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ぞれＣｏＳｉ膜３０、３２、３４が形成された基体に対してN_2雰囲気中における第２回目のアニール処理を行い、これらのＣｏＳｉ膜３０、３２、３４をＣｏシリサイドの中で最も低抵抗な相である$CoSi_2$膜３６、３８、４０に相転移する（図１４参照）。なお、これらのＣｏＳｉ膜３０、３２、３４を$CoSi_2$膜３６、３８、４０に相転移する際の第２回目のアニール処理条件は、上記第１の実施形態の場合と同様である。

【００４７】以上のように本実施形態によれば、上記第１の実施形態にいわゆるＴｉＮキャップ・プロセスを組み合わせることにより、即ちＲＴＡ法を用いたNH_3雰囲気中における熱処理によりゲート電極１４並びにソース領域１６及びドレイン領域１８上にＳｉＮ薄膜２２、２４、２６をそれぞれ形成し、基体全面にＣｏ膜２８を成膜した後、このＣｏ膜２８上に酸化防止用膜としてＴｉＮキャップ膜４２を成膜し、続いて第１回目のＲＴＡ法を用いたアニール処理によりＣｏＳｉ膜３０、３２、３４をそれぞれ形成し、第２回目のＲＴＡ法を用いたアニール処理により$CoSi_2$膜３６、３８、４０に相転移することにより、成膜後のＣｏ膜２８全面がＴｉＮキャップ膜４２によって覆われ、大気暴露による表面酸化から保護されるため、その後の第１回目のアニール処理によるＣｏＳｉ膜３０、３２、３４の形成、更に第２回目のアニール処理による$CoSi_2$膜３６、３８、４０への相転移を安定して行うことができる。従って、上記第１の実施形態の場合と同様の効果を奏することに加え、低抵抗の$CoSi_2$膜３６、３８、４０をより安定に形成することができるため、更に信頼性の高い、より高速な半導体デバイスを作製することが可能になる。

【００４８】

【発明の効果】以上、詳細に説明した通り、本発明に係る半導体装置の製造方法によれば、次のような効果を奏することができる。即ち、請求項１に係る半導体装置の製造方法によれば、シリコン領域を含む基体全面に金属膜を形成する前に、このシリコン領域上にスパイク防止用の薄膜を形成することにより、シリコン領域と金属膜との間にスパイク防止用の薄膜が介在することになるため、熱処理によりシリコン領域のＳｉと金属とを反応させる際に、シリサイド化反応の初期において発生する局所的な金属原子の異常拡散が抑制され、金属原子が均一に拡散して、シリサイドのスパイクが形成されることを防止することが可能になり、このシリサイドのスパイクに起因するリーク電流の発生を防止することができる。また、こうしたリーク電流の発生を防止することができることから、低抵抗のシリサイド膜の膜厚を更に十分に厚くすることが可能になるため、このシリサイド膜を形成したシリコン領域の抵抗を更に低減することができる。従って、高信頼性、高性能の半導体デバイスを作製することが可能になる。

【００４９】また、請求項２に係る半導体装置の製造方法によれば、上記請求項１に係る半導体装置の製造方法において、金属膜がＣｏ膜であることにより、特にシリサイドのスパイクが形成され易いＣｏ膜の場合であっても、シリコン領域のＳｉとの反応によってシリサイド膜が形成される際に、シリコン領域とＣｏ膜と間にスパイク防止用の薄膜が介在しているため、局所的なＣｏ原子の異常拡散が抑制され、Ｃｏ原子が均一に拡散して、Ｃｏシリサイドのスパイクの形成を防止することが可能になる。このため、Ｃｏシリサイドのスパイクに起因するリーク電流の発生を防止することができると共に、こうしたリーク電流の発生を防止することができることから、最も低抵抗な相のＣｏシリサイド膜、即ち$CoSi_2$膜の膜厚を更に十分に厚くすることが可能になり、この$CoSi_2$膜を形成したシリコン領域、例えばゲート電極やソース領域及びドレイン領域の抵抗を更に低減することができるため、信頼性の高い、より高速な半導体デバイスを作製することが可能になる。

【００５０】また、請求項３に係る半導体装置の製造方法によれば、上記請求項１に係る半導体装置の製造方法において、スパイク防止用の薄膜がＳｉＮ膜からなることにより、シリコン領域と金属膜との間にＳｉＮ膜が介在するため、局所的な金属原子の異常拡散を抑制して均一に拡散させ、シリサイド膜を形成する際のスパイク防止用薄膜として機能することができる。

【００５１】また、請求項４に係る半導体装置の製造方法によれば、上記請求項３に係る半導体装置の製造方法において、ＳｉＮ膜からなるスパイク防止用の薄膜を形成する工程が、ＲＴＡ法を用いて、シリコン領域を含む基体全面に対してNH_3雰囲気中におけるアニール処理を行い、シリコン領域表面にＳｉＮ膜を形成する工程であることにより、Ｓｉと金属との反応を阻止することなく、且つシリサイド膜を形成する際のスパイク防止用薄膜として機能するのに必要十分な膜厚をもつ緻密なＳｉＮ膜を容易に形成することが可能になる。

【００５２】また、請求項５に係る半導体装置の製造方法によれば、上記請求項２に係る半導体装置の製造方法において、シリコン領域を含む基体全面にＣｏ膜を形成した後に、このＣｏ膜上に例えばＴｉＮ膜からなる酸化防止用の薄膜を形成する工程が含まれることにより、Ｃｏ膜が大気暴露によって表面酸化されることから保護されるため、上記請求項２に係る半導体装置の製造方法の場合よりも更に安定してＣｏシリサイド膜の形成を行うことができる。

【図面の簡単な説明】

【図１】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その１）である。

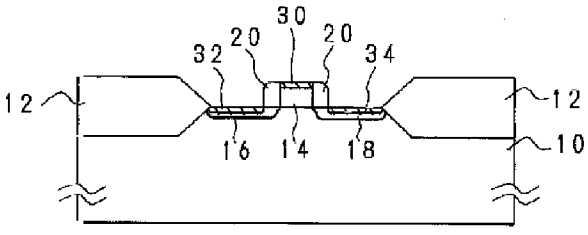
【図２】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その２）である。

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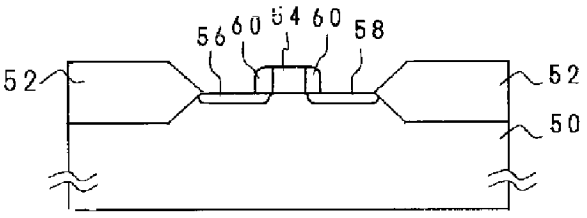
【図３】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その３）である。
【図４】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その４）である。
【図５】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その５）である。
【図６】本発明の第１の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その６）である。
【図７】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その１）である。
【図８】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その２）である。
【図９】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その３）である。
【図１０】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その４）である。
【図１１】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その５）である。
【図１２】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その６）である。
【図１３】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その７）である。
【図１４】本発明の第２の実施形態に係るＣｏシリサイド・プロセスを説明するための工程断面図（その８）である。
【図１５】n^+ 型拡散層上に形成されたＴｉシリサイド膜のシート抵抗Ｒｓの線幅依存性を示すのグラフである。
【図１６】p^+ 型拡散層上に形成されたＴｉシリサイド膜のシート抵抗Ｒｓの線幅依存性を示すのグラフである。
【図１７】n^+ 型拡散層上に形成されたＣｏシリサイド膜のシート抵抗Ｒｓの線幅依存性を示すのグラフである。
【図１８】p^+ 型拡散層上に形成されたＣｏシリサイド膜のシート抵抗Ｒｓの線幅依存性を示すのグラフである。
【図１９】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その１）である。
【図２０】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その２）である。
【図２１】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その３）である。
【図２２】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その４）である。
【図２３】従来のＣｏシリサイド・プロセスを説明するための工程断面図（その５）である。
【図２４】n^+ 型拡散層上にＣｏシリサイド膜を形成する際のシリサイド温度によるリーク電流の累積度数分布を示すのグラフである。
【図２５】p^+ 型拡散層上にＣｏシリサイド膜を形成する際のシリサイド温度によるリーク電流の累積度数分布を示すのグラフである。
【図２６】従来のＣｏシリサイド・プロセスにおいて形成されるＣｏシリサイドのスパイクを示す模式図である。

【符号の説明】
１０…シリコン基板、１２…ＬＯＣＯＳ膜、１４…ゲート電極、１６…ソース領域、１８…ドレイン領域、２０…サイドウォール、２２、２４、２６…ＳｉＮ薄膜、２８…Ｃｏ膜、３０、３２、３４…ＣｏＳｉ膜、３６、３８、４０…$CoSi_2$ 膜、４２…ＴｉＮキャップ膜、５０…シリコン基板、５２…ＬＯＣＯＳ膜、５４…ゲート電極、５６…ソース領域、５８…ドレイン領域、６０…サイドウォール、６２…Ｃｏ膜、６４、６６、６８…ＣｏＳｉ膜、７０、７２、７４…$CoSi_2$ 膜、７６…n^+ 型拡散層、７８…Ｃｏシリサイド膜、８０…Ｃｏシリサイドのスパイク。

【図5】

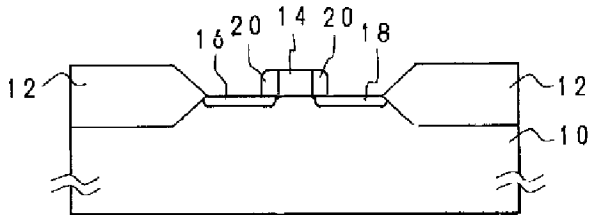


【図１９】



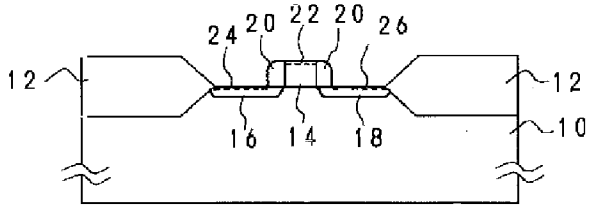
GF Exhibit 1126 - 1445/2248

【図1】



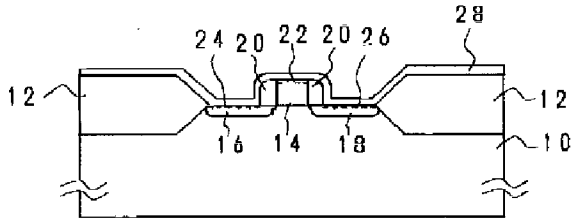
10・・・Si基板
12・・・LOCOS膜
14・・・ゲート電極
16・・・ソース領域
18・・・ドレイン領域
20・・・サイドウオール

【図2】



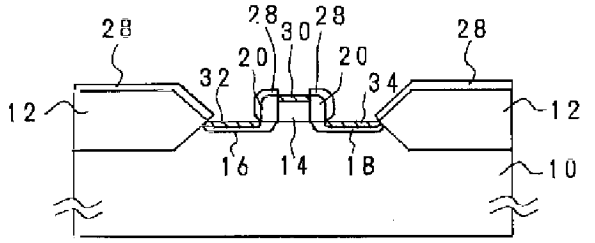
22、24、26・・・SiN薄膜

【図3】



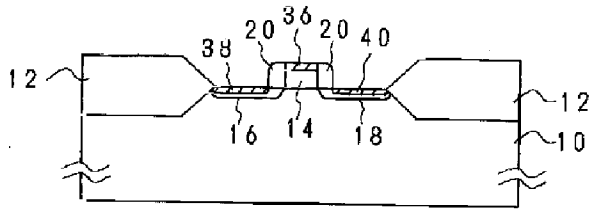
10・・・Si基板
12・・・LOCOS膜
14・・・ゲート電極
16・・・ソース領域
18・・・ドレイン領域
20・・・サイドウオール
22、24、26・・・SiN薄膜
28・・・Co膜

【図4】



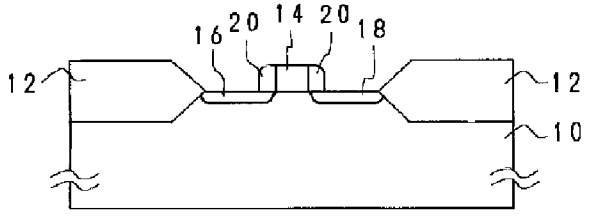
30、32、34・・・CoSi膜

【図6】



36、38、40・・・$CoSi_2$膜

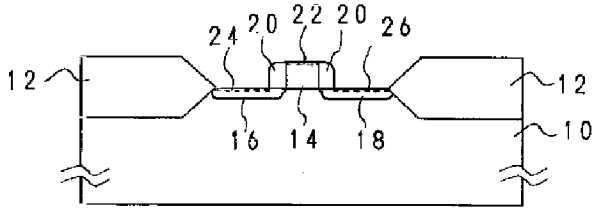
【図7】



10・・・Si基板
12・・・LOCOS膜
14・・・ゲート電極
16・・・ソース領域
18・・・ドレイン領域
20・・・サイドウオール

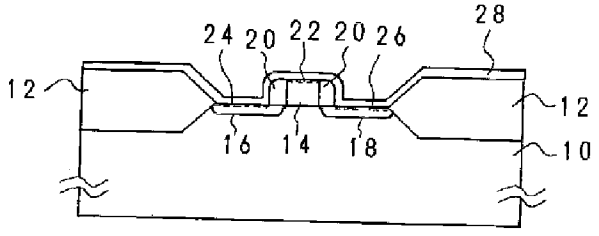
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【図8】



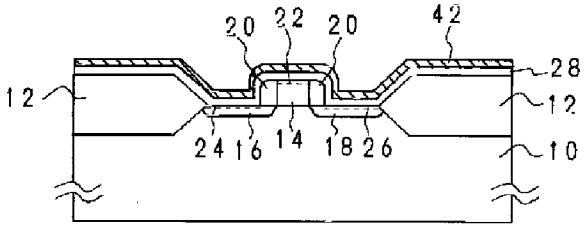
22、24、26・・・SiN膜

【図9】



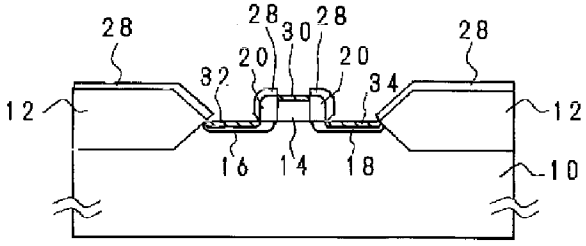
28・・・Co膜

【図10】

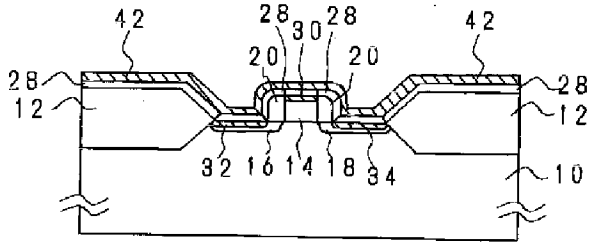


42・・・TiNキャップ膜

【図12】

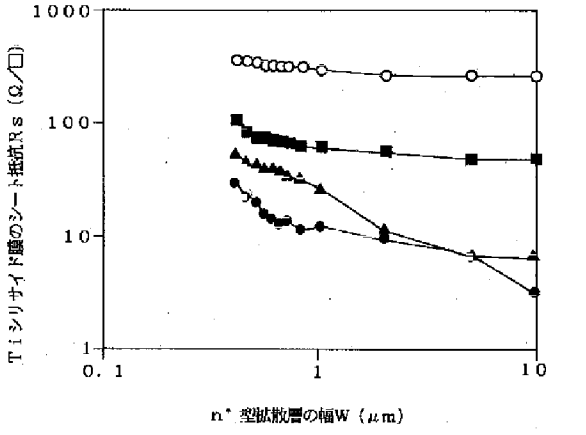


【図11】

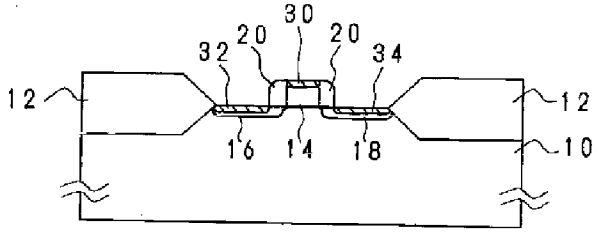


30、32、34・・・CoSi膜

【図15】

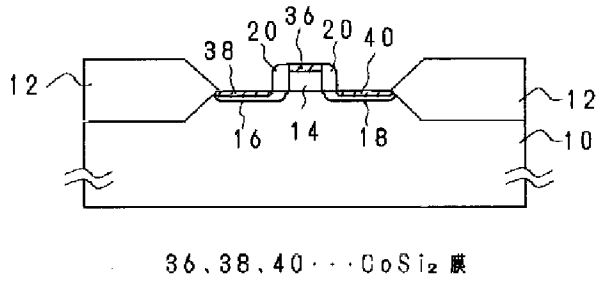


【図13】



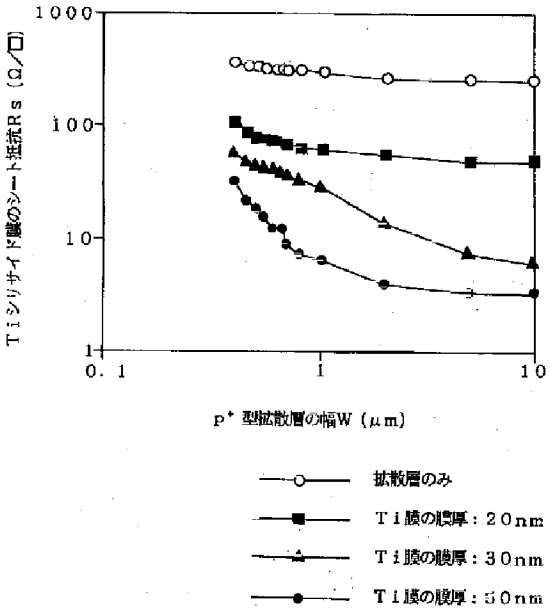
GF Exhibit 1126 - 1447/2248

【図14】

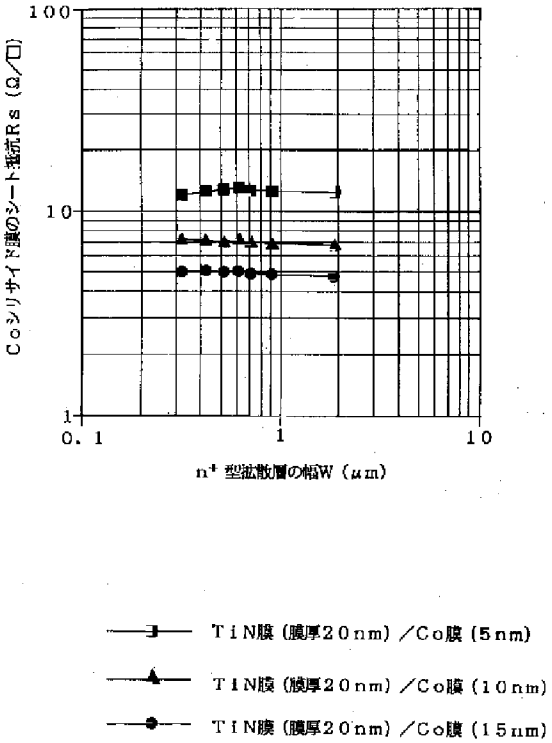


36、38、40・・・$CoSi_2$ 膜

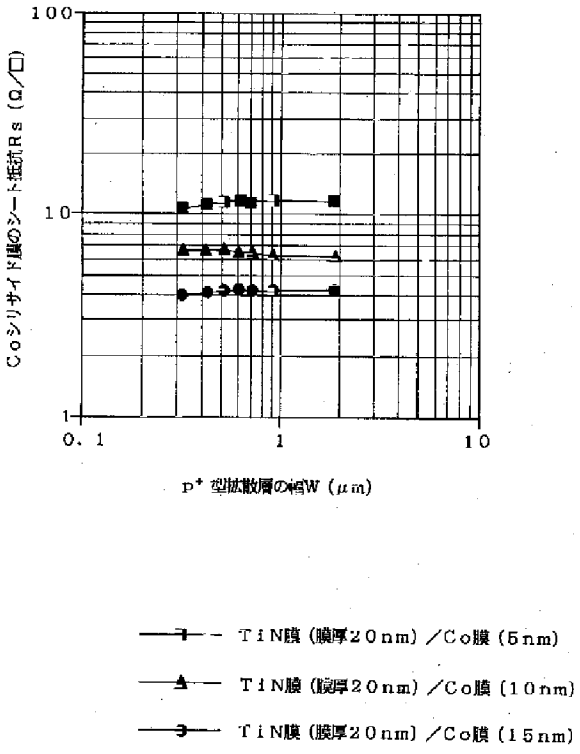
【図16】



【図17】

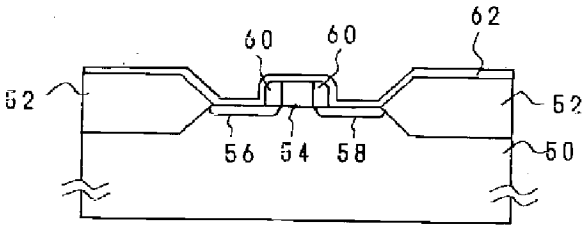


【図18】

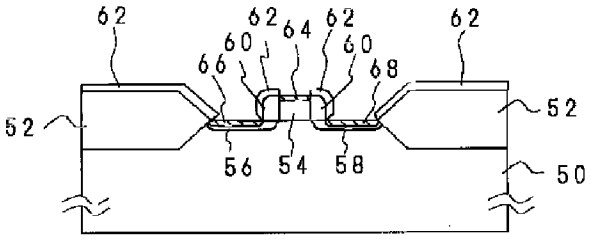


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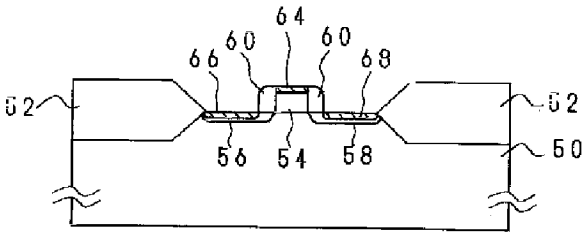
【図20】



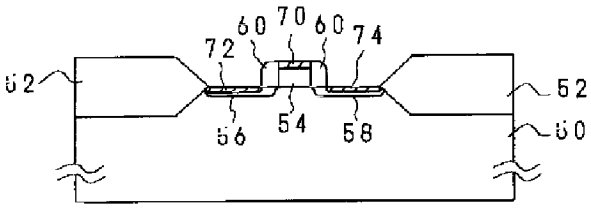
【図21】



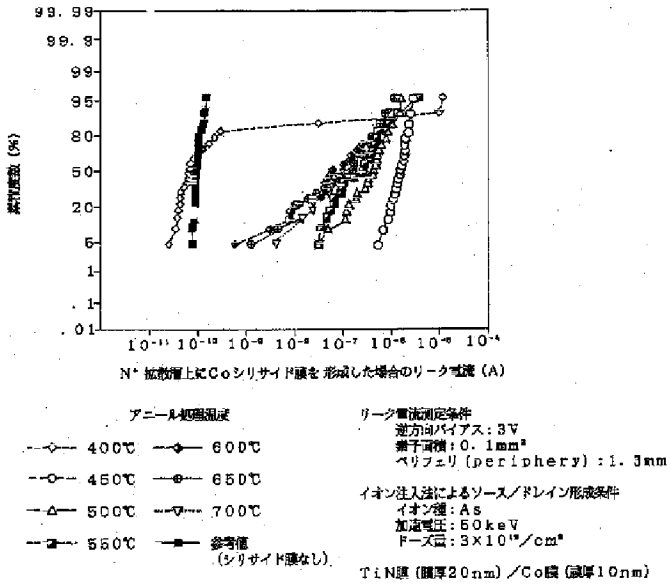
【図22】



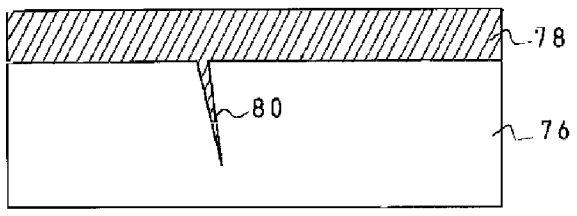
【図23】



【図24】

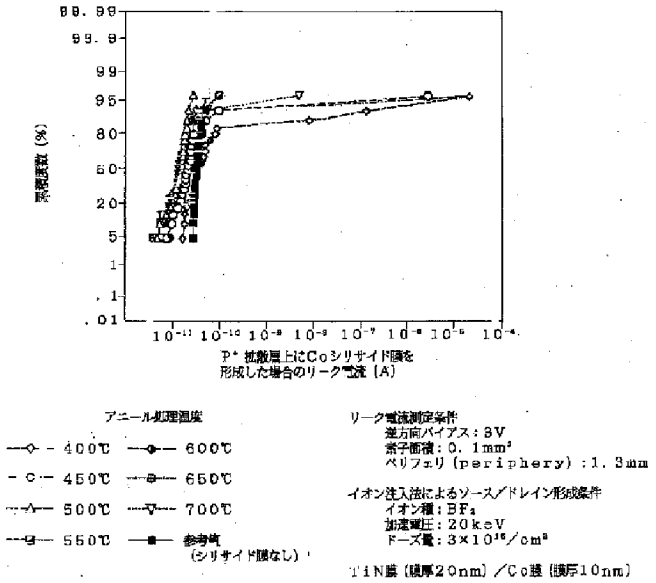


【図26】



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【図25】



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JPH10335265A MANUFACTURE OF SEMICONDUCTOR DEVICE

Applicants: SONY CORP

Inventors: CHIBA YASUHIRO

Classifications:

IPC ***H01L21/28; H01L21/285; H01L21/336; H01L29/78;*** (IPC1-7): H01L21/285; H01L21/336; H01L29/78;

Priorities: JP13706397A 1997-05-27

Application: JPH10335265A·1997-05-27

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Published as: JPH10335265A

MANUFACTURE OF SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To provide a manufacturing method for a highly reliable, high-speed semiconductor device by preventing the generation of spikes of Co silicide, which causes a leakage current when a silicide film is formed. SOLUTION: This SiN films 22, 24, 26 for preventing spikes are formed on a gate electrode 14 comprising a polycrystalline silicon layer and a source region 16 and a drain region 18 that are formed on the surface layer of a silicon substrate 10, by a heat treatment in NH3 atmospheric gas using a RTA(rapid thermal annealing) method, and then a Co film 28 is formed on the whole surface of the substrate and is reacted with Si in a base by first annealing treatment, using the RTA method to form CoSi films 30, 32, 34. At this time, the thin SiN films 22, 24, 26 are interposed between the Co film and the gate electrode 14 and the source region 16 and the drain region 18 and prevent the abnormal diffusion of local Co atoms, which prevents the formation of spikes of Co silicide.

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DESCRIPTION JPH10335265

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a method of manufacturing a semiconductor device, and more particularly, to forming a metal film on the entire surface of a substrate including a silicon region and heat treating the metal to react with Si (silicon) to form a silicon film on the silicon region. The present invention relates to a so-called salicide (SALIDE: Self-Alinged Slicide) process for forming a silicide film in a self-aligned manner.

[0002]

2. Description of the Related Art Due to recent demands for lower resistance and higher speed of semiconductor devices, there is a side technology for forming a low resistance silicide film on a gate and source / drain (S / D) regions in a self-aligned manner. Attention has been paid. As a silicide material in such a case, Ti (titanium) silicide, Co (cobalt) silicide, or the like has been actively studied.

[0003]

However, in the case of Ti silicide, as shown in the graph of FIG. 15, when a Ti silicide film is formed on the n + type diffusion layer, the sheet resistance Rs of the Ti silicide film decreases as the initial Ti film becomes thicker. However, the sheet resistance Rs of the Ti silicide film tends to

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increase as the width W of the n + type diffusion layer decreases. The line width dependence of the sheet resistance Rs of the Ti silicide film increases as the film thickness of the initial Ti film increases.

[0004]

In addition, as shown in the graph of FIG. 16, when the Ti silicide film is formed on the p + type diffusion layer, the sheet resistance Rs of the Ti silicide film is similar to the case where the Ti silicide film is formed on the n + type diffusion layer. The line width dependency of appears. Thus, when a Ti silicide film is formed on a fine line, the sheet resistance Rs of the film is increased, which is a so-called thin line effect.

[0005]

On the other hand, in the case of Co silicide, as shown in the graph of FIG. 17, when the Co silicide film is formed on the n + type diffusion layer, the sheet resistance of the Co silicide film increases as the initial Co film becomes thicker. Although Rs is reduced, the sheet resistance Rs of the Co silicide film hardly changes even if the width W of the n + type diffusion layer is narrowed. The fact that the sheet resistance Rs of the Co silicide film does not depend on the line width as described above also means that the Co silicide film is formed on the p + -type diffusion layer as shown in the graph of FIG. It is the same.

[0006]

The graphs of FIGS. 17 and 18 show data in the case of a so-called TiN cap structure in which a CoN film is covered with a TiN film when the Co silicide film is formed. In the case where the Co silicide film is formed using only the Co film that does not have the same characteristics, basically the same characteristics are exhibited. Therefore, even when a Co silicide film is formed on a fine line, the thin line effect of increasing the sheet resistance Rs does not occur.

[0007]

As described above, since the thin line effect does not occur even when formed on a fine line, the

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Co silicide film has recently been studied more actively. The conventional Co silicide process will be described below with reference to FIGS.

[0008]

First, for example, by using a LOCOS (Local Oxidation of Slicon; selective oxidation) method, a LOCOS film 52 is selectively formed on a silicon substrate 50 to perform element isolation, and then a gate is formed on the silicon substrate 50 in the element region. A gate electrode 54 made of a polycrystalline silicon layer is formed through an oxide film (not shown). Then, by using, for example, an ion implantation method, impurities are selectively added to the surface layer portion of the silicon substrate 50 in the element region using the LOCOS film 52 and the gate electrode 54 as a mask to form the source region 56 and the drain region 58. Subsequently, after depositing an SiO2 film (silicon oxide film) on the entire surface of the substrate, the SiO2 film is removed by etching by a dry etching method, the SiO2 film is left on the side surface of the gate electrode 54, and the SiO2 film is left on the side surface of the gate electrode 54. A sidewall 60 made of is formed (see FIG. 19).

[0009]

Then, the Co film 62 is uniformly formed on the entire surface of the substrate by using, for example, the sputtering method (see FIG. 20). Then, using RTA (Rapid Thermal Annealing) method, a first annealing process is performed at a processing temperature of about 550 ° C. to perform a Co film on the gate electrode 54 and the source region 56 and the drain region 58. 62 is reacted with the underlying Si to form CoSi films 64, 66 and 68 which are high resistance Co silicides, respectively. At this time, the Co film 62 remains unreacted on the LOCOS film 52 and the sidewall 60 (see FIG. 21).

[0010]

Then, the Co film 62 remaining unreacted on the LOCOS film 52 and the sidewall 20 is selectively removed by etching using a wet etching method (see FIG. 22). Then, using the RTA method, a second annealing process is performed under the condition of a processing temperature of about 700 ° C., and the CoSi films 64, 66 and 68 which are high resistance Co silicides have the lowest resistance among Co silicides. The phase changes to the CoSi2 films 70, 72 and 74 which are the phases (see FIG. 23).

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[0011]

That is, this conventional Co silicide process uses polycrystalline silicon through the gate oxide film on the silicon substrate 50 in the element region separated by the LOCOS film 52 by using the LOCOS method, the ion implantation method, the dry etching method, or the like. Forming a gate electrode 54 made of a layer, forming a source region 56 and a drain region 58 on the surface layer of the silicon substrate 50, and forming a sidewall 60 on the side surface of the gate electrode 54; By the step of forming the Co film 62 and the first annealing process using the RTA method, the Co film 62 on the gate electrode 54 and the source region 56 and the drain region 58 reacts with the underlying Si to obtain a high resistance. After removing the unreacted Co film 62 on the LOCOS film 52 and the sidewalls 60 by using the step of forming the CoSi films 64, 66, and 68 that are Co silicide and the wet etching method, respectively, the RTA method is used. By the second annealing, the CoSi films 64, 66 and 68 are transformed into the CoSi2 films 70, 72 and 74, which have the lowest resistance among Co silicides, respectively.

[0012]

As described above, in the conventional Co silicide process, when the annealing treatment by the RTA method for forming the CoSi2 films 70, 72 and 74 is performed, the Co film 62 reacts with the underlying Si to form the CoSi film 64, The first annealing treatment at a treatment temperature of about 550 ° C. to form 66 and 68, and the treatment temperature at a treatment temperature of about 700 ° C. at which these CoSi films 64, 66 and 68 undergo phase transition to the CoSi 2 films 70, 72 and 74. By being divided into two stages including the second annealing process, not only the CoSi films 64, 66 and 68 are formed on the gate electrode 54 and the source region 56 and the drain region 58, but also the adjacent sidewalls 60. It is possible to prevent a so-called creeping phenomenon that a CoSi film is formed up to the top.

Therefore, the CoSi film 30 on the gate electrode 14 and the CoSi films 32 and 34 on the source region 16 and the drain region 18 are short-circuited via the CoSi film formed on the sidewall 20, that is, the gate electrode 14 and the source. The low resistance CoSi2 films 70, 72 and 74 are self-aligned on the gate electrode 54 and the source region 56 and the drain region 58 without causing a so-called bridging phenomenon in which the region 16 and the drain region 18 are short-circuited. It is formed.

[0013]

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However, in the above conventional Co silicide process, as shown in the graphs of FIGS. 24 and 25, Co silicide is formed on the n + type diffusion layer and the p + type diffusion layer, respectively. When the film is formed, a leak current with large variations occurs in these n + type diffusion layer and p + type diffusion layer. In particular, when a Co silicide film is formed on the n + type diffusion layer, there is a large difference in the generation of leak current depending on the annealing treatment temperature for siliciding the Co film formed on the n + type diffusion layer. That is, when the annealing temperature rises from 400 ° C to 450 ° C, the leak current increases sharply. Then, as the annealing temperature rises from 450 ° C to 700 ° C, the leakage current tends to decrease slightly.

[0014]

For this reason, as shown in FIG. 26, for example, the leakage current generated when the Co silicide film 78 is formed on the n + type diffusion layer 76 is a relatively low annealing temperature near 450 ° C. (K. Goto, et al., "Leakage Mechanism and Optimized Conditions of Co Process for Deep-Submicron CMOSDevices" IEDM (1995). (See p.449). It is considered that the formation of the Co silicide spike 80 is because Co atoms are abnormally diffused into the n + type diffusion layer 76 and Co silicide is formed only in that portion. Therefore, since Co silicide has no thin line effect as described above, it is extremely advantageous when it is applied to a semiconductor device that will be further miniaturized in the future, while Co silicide has a spike in Co silicide that occurs in the initial stage of the silicidation reaction. The generation of leak current caused by this is a major obstacle to application to actual devices.

[0015]
Therefore, the present invention has been made in view of the above circumstances, and when forming a silicide film, it is possible to prevent formation of a spike of silicide that causes a leak current, and to achieve high reliability and high speed. It is an object to provide a method for manufacturing a semiconductor device.

[0016]

The above object can be achieved by the following method for manufacturing a semiconductor device according to the present invention.

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That is, in the method of manufacturing a semiconductor device according to the first aspect, after the metal film is formed on the entire surface of the base body including the silicon region, the metal film is reacted with Si in the silicon region by heat treatment to form the silicide film on the silicon region. A method of manufacturing a semiconductor device, which is formed in a consistent manner, characterized by including a step of forming a thin film for spike prevention on a silicon region before forming a metal film on the entire surface of a substrate including a silicon region. .

[0017]

As described above, in the method of manufacturing a semiconductor device according to the first aspect, before forming the metal film on the entire surface of the substrate including the silicon region, the spike preventing thin film is formed on the silicon region, so that the silicon is heat-treated. When reacting Si in the region with the metal, a thin film for preventing spikes is interposed between the silicon region and the metal film, so that local abnormal diffusion of metal atoms occurs at the initial stage of the silicidation reaction. Are suppressed and the metal atoms are uniformly diffused to prevent the formation of silicide spikes. Therefore, generation of a leak current due to the spike of the silicide is prevented.

[0018]

Note that here, the silicon region includes both a polycrystalline silicon region and a single crystal silicon region. Further, since the spike preventing thin film interposed between the silicon region and the metal film is extremely thin, it does not prevent the silicidation reaction between Si and the metal.

[0019]

A method of manufacturing a semiconductor device according to a second aspect is the method of manufacturing a semiconductor device according to the first aspect, wherein the metal film is a Co film, and a silicide film is formed by a reaction with Si. In particular, even in the case of a Co film in which a silicide spike is easily formed, since a thin film for preventing spikes is interposed between the silicon region and the Co film, the local occurrence of the silicide reaction occurs at the initial stage. Such abnormal diffusion of Co atoms is suppressed, Co atoms are uniformly diffused, and formation of spikes of Co silicide is prevented. Therefore, generation of a leak

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current due to the spike of Co silicide is prevented.

[0020]
Further, a method for manufacturing a semiconductor device according to a third aspect is the method for manufacturing a semiconductor device according to the first aspect, wherein the spike prevention thin film is made of a SiN film (silicon nitride film). Since the silicidation reaction is not disturbed as in the case where the natural oxide film is interposed between the region and the metal film, the SiN film interposed between the silicon region and the metal film has a local abnormality of metal atoms. The function as a spike prevention thin film at the time of forming a silicide film of suppressing diffusion is well exhibited.

[0021]
The method of manufacturing a semiconductor device according to claim 4 is the method of manufacturing a semiconductor device according to claim 3, wherein the step of forming the spike-preventing thin film made of a SiN film uses a RTA method to form a silicon region. Since the entire surface of the substrate including is subjected to an annealing treatment in an NH3 (ammonia) atmosphere to form a SiN film on the surface of the silicon region, the silicidation reaction between Si and metal can be prevented. In addition, a dense SiN film having a film thickness necessary and sufficient to function as a spike preventing thin film when forming a silicide film is easily formed.

[0022]

A method of manufacturing a semiconductor device according to a fifth aspect is the method of manufacturing a semiconductor device according to the second aspect, wherein a Co film is formed on the entire surface of the base body including a silicon region, and then a Co film for preventing oxidation is formed on the Co film. By adopting a configuration including a step of forming a thin film, Co is originally a metal film that is very easily oxidized, but it is covered with a thin film for oxidation protection, so the Co film is protected from surface oxidation by exposure to the atmosphere. To be done.

A TiN film is suitable as a thin film for preventing the oxidation of the Co film.

[0023]

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BEST MODE FOR CARRYING OUT THE INVENTION Embodiments of the present invention will be described below with reference to the accompanying drawings.

(First Embodiment) FIGS. 1 to 6 are process sectional views for explaining a Co silicide process according to a first embodiment of the present invention. First, the LOCOS film 12 is selectively formed on the silicon substrate 10 by using, for example, the LOCOS method, and element isolation is performed. After that, a gate electrode 14 made of a polycrystalline silicon layer is formed on the silicon substrate 10 in the element region separated by the LOCOS film 12 with a gate oxide film (not shown) interposed therebetween.

[0024]

Subsequently, by using, for example, an ion implantation method, impurities are selectively added to the surface layer portion of the silicon substrate 10 in the element region using the LOCOS film 12 and the gate electrode 14 as a mask to form the source region 16 and the drain region 18. Then, after depositing an SiO2 film on the entire surface of the substrate, the SiO2 film is removed by etching by a dry etching method, and the SiO2 film is left on the side surface of the gate electrode 14. Thus, the side wall 20 made of the SiO2 film is formed on the side surface of the gate electrode 14 (see FIG. 1).

[0025]

Then, by RTA method, the entire substrate with the upper surface of the gate electrode 14 and the surfaces of the source region 16 and the drain region 18 exposed is heat-treated in an NH3 atmosphere. In this way, the upper surface of the gate electrode 14 and the surfaces of the source region 16 and the drain region 18 are nitrided to form dense SiN thin films 22, 24 and 26 having a film thickness of 1.5 nm, respectively (see FIG. 2). The heat treatment conditions using the RTA method when forming these SiN thin films 22, 24, and 26 with a film thickness of 1.5 nm are as follows: NH3 atmosphere gas flow rate: 5 sccm Treatment temperature: 900 ° C. Treatment time: 30 seconds

[0026]

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Next, a 10 nm-thickness Co film 28 is uniformly formed on the entire surface of the substrate by using, for example, a sputtering method (see FIG. 3). The film forming conditions for forming the Co film 28 having a film thickness of 10 nm are as follows: DC power: 0.8 kW Pressure: 0.4 Pa Ar (argon) gas flow rate for heater: 30 sccm Ar gas flow rate for process: 60 sccm Substrate heating temperature: 150 ° C

[0027]

Next, the RTA method is used to perform the first annealing treatment in a N 2 (nitrogen) atmosphere on the substrate on which the Co film 28 is formed on the entire surface thereof, to thereby form the gate electrode 14, the source region 16 and the drain. The Co film 28 on the region 18 is reacted with the underlying Si to form CoSi films 30, 32, and 34 that are high-resistance Co silicide. At this time, the Co film 28 remains unreacted on the LOCOS film 12 and the sidewall 20 (see FIG. 4). The annealing treatment conditions using the first RTA method when forming these CoSi films 30, 32 and 34 are as follows: N2 atmosphere gas flow rate: 10 sccm Treatment temperature: 550 ° C. Treatment time: 30 seconds

[0028]
At this time, the polycrystalline silicon surface of the gate electrode 14 and the single crystal silicon surfaces of the source region 16 and the drain region 18 (hereinafter, both the polycrystalline silicon surface and the single crystal silicon surface are collectively referred to as "silicon surface").) And the Co film 28, the SiN thin films 22, 24, and 26 are interposed respectively, but since the SiN thin films 22, 24, and 26 have a very thin film thickness of 1.5 nm, the Co film 28 Does not block the reaction with the silicon surface of the gate electrode 14 and the source and drain regions 16 and 18.

[0029]

Further, when the first annealing treatment is performed under the above conditions, in the conventional case, CoSi spikes were usually formed as shown in FIG. 26, but in the present embodiment, Since the SiN thin films 22, 24, and 26 are interposed between the Co film 28 and the Co film 28 and the underlying silicon surface, the local abnormal diffusion of Co atoms is suppressed, and the Co atoms are uniformly diffused. , CoSi spikes are no longer formed.

That is, the SiN thin films 22, 24 and 26 function as spike preventing thin films when the CoSi

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films 30, 32 and 34 are formed.

[0030]
Further, in the present embodiment, since the annealing treatment is performed under the condition of the treatment temperature of 550 ° C. and the treatment time of 30 seconds, the CoSi film is formed also on the sidewall 20 and the CoSi film 30 on the gate electrode 14. A short circuit between the CoSi films 32 and 34 on the source region 16 and the drain region 18, that is, a short circuit between the gate electrode 14 and the source region 16 and the drain region 18, that is, a bridging phenomenon due to so-called CoSi film climbing may occur. Absent.

[0031]

Then, the Co film 28 remaining in the unreacted state on the LOCOS film 12 and the sidewalls 20 is selectively removed by etching using a wet etching method (see FIG. 5).

The wet etching conditions for the unreacted Co film 28 are as follows: chemical solution: sulfuric acid / hydrogen peroxide (H2 SO4: H2 O2 = 4: 1) chemical solution temperature: 70 ° C. Treatment time: 3 minutes

[0032]
Next, the RTA method is used to perform a second annealing treatment in a N 2 atmosphere on the substrate on which the CoSi films 30, 32, and 34 are formed on the gate electrode 14 and the source region 16 and the drain region 18, respectively. Then, the CoSi films 30, 32, and 34 undergo phase transition to the CoSi2 films 36, 38, and 40, which have the lowest resistance among the Co silicides (see FIG. 6).

[0033]
The second annealing treatment condition for the phase transition of the CoSi films 30, 32, 34 into the CoSi2 films 36, 38, 40 is as follows: N2 atmosphere gas flow rate: 10 sccm Processing temperature: 700 ° C Processing time: 30 Second

[0034]
As described above, according to this embodiment, the gate electrode 14 made of the polycrystalline silicon layer and the source region 16 and the drain region 18 at the surface layer

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of the silicon substrate 10 are heat-treated in the NH 3 atmosphere using the RTA method. After forming the SiN thin films 22, 24 and 26 having a film thickness of 1.5 nm on the substrate, a Co film 28 having a film thickness of 10 nm is formed on the entire surface of the substrate, and the Co film 28 is formed by the first annealing treatment using the RTA method. By reacting with the underlying Si, CoSi films 30, 32, and 34 that are high-resistance Co silicide are formed, and have the lowest resistance phase among the Co silicides by the second annealing treatment using the RTA method. Although the phase transition has occurred in the CoSi2 films 36, 38 and 40, when the Co film 28 and the underlying Si are reacted by the first annealing treatment using the RTA method, the gate electrode 14, the source region 16 and the drain are formed. Since the spike-preventing SiN thin films 22, 24, and 26 are interposed between the region 18 and the Co film 28, local abnormal diffusion of Co atoms is suppressed, and the Co atoms are uniformly diffused. Since the formation of the spike of silicide can be prevented, it is possible to prevent the generation of the leak current due to the spike of Co silicide, and it is possible to improve the reliability of the semiconductor device.

[0035]
Further, since the generation of the leak current can be prevented in this way, the film thickness of the low resistance CoSi2 films 36, 38 and 40 can be further increased sufficiently, and thus the CoSi2 films 36 and 38 can be made thicker. , 40, the resistance of the gate electrode 14 and the source region 16 and the drain region 18 can be further reduced, and the operation speed of the semiconductor device can be further increased.

[0036]

(Second Embodiment) FIGS. 7 to 14 are process cross-sectional views for explaining a Co silicide process according to a second embodiment of the present invention.

The same elements as those shown in FIGS. 1 to 6 are designated by the same reference numerals and the description thereof will be omitted.

First, by using the LOCOS method, the LOCOS film 12 is selectively formed on the silicon substrate 10 to perform element isolation, and then the gate oxide film (on the silicon substrate 10 in the element region isolated by the LOCOS film 12). A gate electrode 14 made of a polycrystalline silicon film is formed through (not shown).

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[0037]
Subsequently, by using the ion implantation method, impurities are selectively added to the surface layer portion of the silicon substrate 10 in the element region to form the source region 16 and the drain region 18, and then a gate electrode is formed by depositing a SiO2 film and dry etching the same. A sidewall 20 made of a SiO2 film is formed on the side surface 14 (see FIG. 7).

[0038]

Then, using RTA, the entire substrate is heat-treated in an NH3 atmosphere to nitride the upper surface of the gate electrode 14 and the surfaces of the source region 16 and the drain region 18, and the dense SiN thin films 22 and 24 having a thickness of 1.5 nm. 26 are formed respectively (see FIG. 8).

The RTA processing conditions for forming the SiN thin films 22, 24 and 26 having a film thickness of 1.5 nm are the same as in the case of the first embodiment.

[0039]

Then, a 10 nm-thickness Co film 28 is uniformly formed on the entire surface of the substrate by using the sputtering method (see FIG. 9).

The film forming conditions for forming the Co film 28 having the film thickness of 10 nm are the same as in the case of the first embodiment.

[0040]

Next, a TiN cap film 42 having a film thickness of 20 nm is formed on the Co film 28 by using, for example, a sputtering method without exposing the substrate on which the Co film 28 is uniformly formed to the atmosphere (see FIG. 10). ..

The film forming conditions for forming the TiN cap film 42 are: DC power: 6.5 kW Pressure: 0.4

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Pa Ar gas flow rate for heater: 15 sccm N2 gas flow rate for process: 135 sccm Substrate heating temperature: 150 ° C

[0041]

At this time, since the Co film 28 formed on the entire surface of the substrate in the sputtering chamber in the previous step is covered with the TiN cap film 42 without being exposed to the atmosphere, it is originally very oxidized. The Co film 28, which is a susceptible metal film, is protected from being exposed to the atmosphere and oxidizing its surface. That is, the TiN cap film 42 functions as an oxidation preventing film for the Co film 28.

[0042]

Next, the RTA method is used to perform a first annealing treatment in an N2 atmosphere on the base body on which the Co film 28 and the TiN cap film 42 are sequentially laminated on the entire surface, thereby performing the gate electrode 14, the source region 16 and the drain region. The Co film 28 on 18 is reacted with the underlying Si to form CoSi films 30, 32, and 34 that are high-resistance Co silicide, and the unreacted Co film is formed on the LOCOS film 12 and the sidewalls 20. 28 remains (see FIG. 11). The conditions of the first annealing treatment for forming these CoSi films 30, 32, 34 are the same as in the case of the first embodiment.

[0043]

At this time, similar to the case of the first embodiment, the film thickness 1. functioning as a spike preventing thin film is provided between the Co film 28 and the silicon surface of the gate electrode 14, the source region 16 and the drain region 18. Since the 5 nm SiN thin films 22, 24, and 26 are respectively interposed, the local Co atoms can be prevented without blocking the reaction between the silicon film of the gate electrode 14 and the source region 16 and the drain region 18 and the Co film 28. Since the abnormal diffusion of Co is suppressed and Co atoms are uniformly diffused, the CoSi films 30, 32, and 34 are formed, and the formation of CoSi spikes is prevented. Also in this embodiment, as in the case of the first embodiment, since the annealing treatment is performed under the conditions of the treatment temperature of 550 ° C. and the treatment time of 30 seconds, the bridging phenomenon due to the creeping-up of the CoSi film. Will never happen.

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[0044]

Next, by using, for example, a wet etching method, the TiN cap film 42 formed on the Co film 28 as an oxidation preventing film of the Co film 28 is removed by etching (see FIG. 12). The wet etching conditions for the TiN cap film 42 are as follows: chemical solution: ammonia hydrogen peroxide (NH4 OH: H2 O2: H2 O = 1: 2: 6) chemical solution temperature: 65 ° C. processing time: 3 minutes

[0045]

Next, the unreacted Co film 28 on the LOCOS film 12 and the sidewalls 20 is selectively removed by etching using a wet etching method (see FIG. 13). The wet etching conditions for the unreacted Co film 28 are the same as in the case of the first embodiment.

[0046]

Then, the RTA method is used to perform a second annealing treatment in an N 2 atmosphere on the substrate on which the CoSi films 30, 32, and 34 are formed on the gate electrode 14 and the source region 16 and the drain region 18, respectively. These CoSi films 30, 32 and 34 undergo phase transition to the CoSi2 films 36, 38 and 40 which have the lowest resistance among Co silicides (see FIG. 14). The conditions of the second annealing treatment when the CoSi films 30, 32 and 34 are phase-transitioned to the CoSi2 films 36, 38 and 40 are the same as those in the first embodiment.

[0047]

As described above, according to the present embodiment, the gate electrode 14, the source region 16 and the drain region are formed by combining the first embodiment with the so-called TiN cap process, that is, by the heat treatment in the NH 3 atmosphere using the RTA method. After forming SiN thin films 22, 24, and 26 on 18 respectively and forming a Co film 28 on the entire surface of the substrate, a TiN cap film 42 is formed on this Co film 28 as an oxidation preventing film, and then The CoSi films 30, 32, and 34 are formed by the first annealing process using the RTA method, and the phase transition to the CoSi2 films 36, 38, and 40 is performed

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by the second annealing process using the RTA method. Since the entire surface of the Co film 28 after the film is covered with the TiN cap film 42 and protected from surface oxidation due to exposure to the atmosphere, the CoSi films 30, 32, and 34 are formed by the subsequent first annealing treatment, and further the second time. It is possible to stably perform the phase transition to the CoSi2 films 36, 38 and 40 by the annealing treatment of. Therefore, in addition to achieving the same effect as in the case of the first embodiment, the CoSi2 films 36, 38, 40 having low resistance can be formed more stably, so that the reliability is higher and the speed is higher. It becomes possible to manufacture a semiconductor device.

[0048]

As described in detail above, according to the method of manufacturing a semiconductor device of the present invention, the following effects can be obtained. That is, according to the method of manufacturing a semiconductor device according to claim 1, before forming the metal film on the entire surface of the base body including the silicon region, a thin film for preventing spikes is formed on the silicon region to form the silicon region. Since a thin film for preventing spikes is interposed between the metal film and the metal film, when the Si in the silicon region is reacted with the metal by heat treatment, the local abnormal diffusion of metal atoms occurs at the initial stage of the silicidation reaction. It is possible to prevent the formation of a silicide spike by uniformly diffusing the metal atoms, and it is possible to prevent a leak current from being generated due to the silicide spike. Further, since it is possible to prevent the occurrence of such a leak current, it is possible to further increase the thickness of the low-resistance silicide film, thereby further reducing the resistance of the silicon region in which the silicide film is formed. be able to. Therefore, it becomes possible to manufacture a highly reliable and high performance semiconductor device.

[0049]

Further, according to the method of manufacturing a semiconductor device according to claim 2, in the method of manufacturing a semiconductor device according to claim 1, since the metal film is a Co film, a Co film that is particularly apt to form a spike of silicide is formed. Even in this case, when the silicide film is formed by the reaction with Si in the silicon region, a spike prevention thin film is interposed between the silicon region and the Co film, so that a local Co atom abnormality occurs. The diffusion is suppressed, Co atoms are uniformly diffused, and it becomes possible to prevent the formation of spikes of Co silicide. Therefore, it is possible to prevent the generation of a leak current due to the spike of Co silicide, and to prevent the generation of such a leak current. Therefore, the Co silicide film having the lowest resistance,

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that is, the film of the CoSi2 film. It is possible to further increase the thickness and further reduce the resistance of the silicon region in which the CoSi2 film is formed, for example, the gate electrode, the source region and the drain region, resulting in higher reliability and higher speed. It becomes possible to manufacture a semiconductor device.

[0050]
Further, according to the method of manufacturing a semiconductor device according to claim 3, in the method of manufacturing a semiconductor device according to claim 1, since the thin film for preventing spikes is made of a SiN film, a gap between the silicon region and the metal film is formed. Since the SiN film is interposed between the SiN film and the SiN film, it is possible to suppress the local abnormal diffusion of metal atoms and uniformly diffuse the metal atoms to function as a spike preventing thin film when forming a silicide film.

[0051]
According to the method of manufacturing a semiconductor device according to claim 4, in the method of manufacturing a semiconductor device according to claim 3, the step of forming the spike-preventing thin film made of a SiN film uses an RTA method. Since the entire surface of the substrate including the silicon region is annealed in an NH3 atmosphere to form a SiN film on the surface of the silicon region, a silicide film is formed without blocking the reaction between Si and a metal. It becomes possible to easily form a dense SiN film having a necessary and sufficient film thickness to function as a spike prevention thin film at the time of etching.

[0052]
Further, according to the method of manufacturing a semiconductor device according to claim 5, in the method of manufacturing a semiconductor device according to claim 2, after a Co film is formed on the entire surface of the substrate including a silicon region, for example, TiN is formed on the Co film. Since the Co film is protected from being surface-oxidized by exposure to the atmosphere by including the step of forming the oxidation-preventing thin film made of a film, the Co film is more protected than the semiconductor device manufacturing method according to claim 2. The Co silicide film can be formed more stably.

[0053]
Brief description of the drawings

[0054]
1 is a process sectional view (1) for explaining the Co silicide process according to the first

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embodiment of the present invention.

[0055]
2 is a process cross-sectional view (No. 2) for explaining the Co silicide process according to the first embodiment of the present invention.

[0056]
3 is a process sectional view (3) for explaining the Co silicide process according to the first embodiment of the present invention.

[0057]
4 is a process sectional view (4) for explaining the Co silicide process according to the first embodiment of the present invention.

[0058]
5 is a process sectional view (5) for explaining the Co silicide process according to the first embodiment of the present invention. FIG.

[0059]
6 is a process sectional view (6) for explaining the Co silicide process according to the first embodiment of the present invention.

[0060]
7 is a process sectional view (1) for explaining the Co silicide process according to the second embodiment of the present invention.

[0061]
8 is a process cross-sectional view (No. 2) for explaining the Co silicide process according to the second embodiment of the present invention.

[0062]
9 is a process sectional view (3) for explaining the Co silicide process according to the second embodiment of the present invention.

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[0063]
10 is a process sectional view (4) for explaining the Co silicide process according to the second embodiment of the present invention.

[0064]
FIG. 11 is a process sectional view (5) for explaining the Co silicide process according to the second embodiment of the present invention.

[0065]
FIG. 12 is a process sectional view (6) for explaining the Co silicide process according to the second embodiment of the present invention.

[0066]
13 is a process cross-sectional view (No. 7) for explaining the Co silicide process according to the second embodiment of the present invention.

[0067]
14 is a process sectional view (8) for explaining the Co silicide process according to the second embodiment of the present invention.

[0068]
15 is a graph showing the line width dependence of the sheet resistance Rs of the Ti silicide film formed on the n + type diffusion layer.

[0069]
16 is a graph showing the line width dependence of the sheet resistance Rs of the Ti silicide film formed on the p + type diffusion layer.

[0070]
17 is a graph showing the line width dependence of the sheet resistance Rs of the Co silicide film formed on the n + type diffusion layer.

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[0071]
18 is a graph showing the line width dependence of the sheet resistance Rs of the Co silicide film formed on the p + type diffusion layer.

[0072]
19 is a process sectional view (1) for explaining the conventional Co silicide process.

[0073]
20 is a process sectional view (2) for explaining the conventional Co silicide process.

[0074]
21 is a process sectional view (3) for explaining the conventional Co silicide process.

[0075]
22 is a process sectional view (4) for explaining the conventional Co silicide process.

[0076]
23 is a process sectional view (5) for explaining the conventional Co silicide process.

[0077]
FIG. 24 is a graph showing a cumulative frequency distribution of leak current depending on a silicide temperature when forming a Co silicide film on the n + type diffusion layer.

[0078]
FIG. 25 is a graph showing a cumulative frequency distribution of leak current depending on a silicide temperature when forming a Co silicide film on a p + type diffusion layer.

[0079]
26 is a schematic view showing a spike of Co silicide formed in the conventional Co silicide process.

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[0080]
Explanation of symbols

[0081]
10 ... Silicon substrate, 12 ... LOCOS film, 14 ... Gate electrode, 16 ... Source region, 18 ... Drain region, 20 ... Side wall, 22, 24, 26 ... SiN thin film, 28 ... Co film, 30, 32, 34 ... CoSi film, 36, 38, 40 ... CoSi2 film, 42 ... TiN cap film, 50 ... Silicon substrate, 52 ... LOCOS film, 54 ... Gate electrode, 56 ... Source region, 58 ... Drain region, 60 ... Sidewall, 62 ... Co film, 64, 66, 68 ... CoSi film, 70, 72, 74 ... CoSi2 film, 76 ... N + type diffusion layer, 78 ... Co silicide film, 80 ... Co silicide spike.

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CLAIMS JPH10335265

1.
A method of manufacturing a semiconductor device, comprising forming a metal film on the entire surface of a substrate including a silicon region, and then heat treating the metal film to react with Si in the silicon region to form a silicide film on the silicon region in a self-aligned manner. A method for manufacturing a semiconductor device, further comprising the step of forming a spike prevention thin film on the silicon region before forming the metal film on the entire surface of the substrate including the silicon region.

2.
The method of manufacturing a semiconductor device according to claim 1, wherein the metal film is a Co film.

3.
The method of manufacturing a semiconductor device according to claim 1, wherein the spike prevention thin film is a SiN film.

4.
4. The method of manufacturing a semiconductor device according to claim 3, wherein the step of forming the spike-preventing thin film made of the SiN film is performed in a NH3 atmosphere on the entire surface of the substrate including the silicon region by using a short time heat treatment method. A method of manufacturing a semiconductor device, comprising a step of performing an annealing treatment to form the SiN film on the surface of the silicon region.

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5.

The method of manufacturing a semiconductor device according to claim 2, further comprising the step of forming the oxidation preventive thin film on the Co film after forming the Co film on the entire surface of the substrate including the silicon region. Method of manufacturing semiconductor device.

6.

The method for manufacturing a semiconductor device according to claim 5, wherein the oxidation preventing thin film is a TiN film.

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(71)出願人　000002037
新電元工業株式会社
東京都千代田区大手町２丁目２番１号

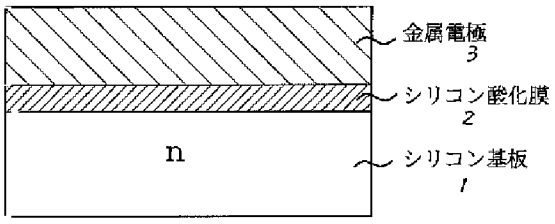
(72)発明者　岩黒　弘明
埼玉県飯能市南町10番13号新電元工業株式会社工場内

(54)【発明の名称】　オーム性接合電極およびこれを用いた半導体装置

(57)【要約】　（修正有）

【課題】　シリコン基板上に金属膜を形成してオーミック電極を形成するとき、そのシリコン基板の不純物の数は理論上１ｃｍ^{3}当たり１０^{20}個以上必要であるが、この不純物濃度よ売りも低いシリコン基板に対しても良好な低接触抵抗を示すオーム性接合電極を提供する。

【解決手段】　シリコン基板１とオーム接合用金属３との間にシリコンサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］２を介在せしめ且つ前記酸化膜の厚さを０．３ｎｍ～２．２５ｎｍとしたことを特徴とする。



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【特許請求の範囲】
【請求項１】　シリコン基板とオーム接合用金属との間にシリコンサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］を介在せしめ且つ前記酸化膜の厚さを０．３ｎｍ～２．２５ｎｍとしたことを特徴とするオーム性接合電極。
【請求項２】　ｎ型シリコン基板を用い且つ前記基板の不純物濃度を10^{16}ｃｍ$^{-3}$乃至10^{20}ｃｍ$^{-3}$としたことを特徴とする請求項１のオーム性接合電極。
【請求項３】　シリコン基板に能動領域を形成し、前記シリコン基板の表面もしくは裏面にシリコンサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］を介して電極金属を接合したことを特徴とする半導体装置。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明はオーム性接合電極及びこれを用いた半導体装置に関するものである。
【０００２】
【従来の技術】シリコン電子デバイスを作る上で金属半導体接合は重要な要素である。この接合には、整流性を示すショットキー接合、他は整流性のないオーム性接合の２つがある。ｎ型シリコン基板と金属を接触させて良好な低接触抵抗を示すオーム性接合電極を形成するには、理論上、シリコン基板の不純物濃度を10^{20}ｃｍ$^{-3}$以上にする必要がある。実用的には、シリコン基板の不純物濃度が10^{19}から10^{20}ｃｍ$^{-3}$でオーム性接合を作っている。シリコンに不純物を多量に導入するために、イオン注入・熱処理法や不純物デポジション・熱拡散法などの方法が使われてきた。
【０００３】最近のシリコンウェーハの大口径化に伴い、ウェーハの厚さは厚くなっている。縦型構造のパワーデバイスにおいては、ウェーハの厚さが厚くなることは、オ
（２）
ン抵抗の上昇を引き起こすことになるので、このオン抵抗の上昇を抑えるためにウェーハ表側のデバイスを作製した後、組み立て前にウェーハを裏側から削って薄くする。この裏側を薄くした後、裏側にオーム性接合電極を作製する。しかしながら、このときシリコン基板の不純物濃度は、10^{20}ｃｍ$^{-3}$よりも低いことが多い。表側にデバイスがすでにできており、Ａ１などの金属配線がなされているため、高温熱処理が困難であり、イオン注入・熱処理法や不純物デポジション・熱拡散法を使って意識的に不純物をシリコン基板に導入することはできない。又、特開平７－３０７３０６号に示すように半導体基板表面に電荷を内存する薄膜を設けてオーム性電極を形成することも提案されている。
【０００４】
【発明が解決しようとする課題】本発明はこのような問題に対して、たとえシリコン基板の不純物濃度が10^{20}ｃｍ$^{-3}$よりも低くても良好な低接触抵抗を示すオーム性接合を提供するものである。通常、シリコン基板の不純物濃度が低いとき、その上に金属膜を堆積させると、金属とシリコン基板の間でショットキー接触となる。このような場合でも、金属とシリコン基板の間にシリコン酸化膜を介することで、良好な低接触抵抗を示すオーム性接合を得る。
【０００５】
【課題を解決するための手段】本発明は、シリコン基板とオーム接合用金属との間にシリコンサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］を介在せしめ且つ前記酸化膜の厚さを０．３ｎｍ～２．２５ｎｍとしたことを特徴とする。
【０００６】シリコン基板を熱酸化法やプラズマ酸化法で酸化させると、２酸化シリコン（ＳｉO2）がシリコン基板上には生成される。この２酸化シリコンとシリコン基板の界面には、２酸化シリコン（ＳｉO2）ではなく、サブシリコン酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］が形成される。このサブシリコン酸化膜の厚さは界面から２ｎｍ程度である。本発明の電極構造のシリコン酸化膜とは
（３）
このサブ酸化膜［ＳｉＯｘ（ｘ＝０．５，１．０，１．５）］のことである。金属膜とサブシリコン酸化膜とを接触させることによって、良好で低接触抵抗を示すオーム性接合が得られる。サブシリコン酸化膜の化学的な活性さによって、本発明の効果が得られるものと思われるが、詳細な理由は明確ではない。２酸化シリコン層と金属膜を接触させると、効果はまったくなくなる。
【０００７】
【実施例】図１は本発明の一実施例を示す断面図で図中１はシリコン基板、２はシリコンサブ酸化膜、３は電極金属である。図２は本発明の酸化膜の厚さの有効性を調べるためのデバイス構造を示す。使用したシリコン基板は、抵抗率が２ｍΩｃｍ（不純物濃度：8×10^{19}ｃｍ$^{-3}$）のｎ+シリコン基板６に、抵抗率が０．５Ωｃｍ（不純物濃度：10^{16}ｃｍ$^{-3}$）のシリコンエピタクシャル層５を５μｍ成長させたものを使用した。このエピタクシャル面はミラーポリッシュ加工されており、表面のひずみは小さい。
【０００８】図２の構造を作製するための製造プロセスは、まず、シリコン基板を希沸酸で１分間洗浄した後、ドライ酸化法を用いて８００℃、３０分間酸化させた。酸化膜厚は約３ｎｍである。次に、その酸化膜の厚さを変えるために希沸酸（ＨＦ：H_2O＝１：１００）液中に一定の時間だけ浸漬させた。この希沸酸で上記３ｎｍの酸化膜を完全にエッチングするには、１００秒の時間がかかった。さらに、上部電極４を形成するために、シリコンエピタクシャル層５の上にチタン膜をスパッタ法で５００ｎｍの厚さに堆積した後、ホトリソグラフィ技

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術を使って図２に示すように０．９ｍｍ角にパターン化した。チタンの化学エッチングには希沸酸を使用した。エッチング時間は２．５分間である。ホトレジストは、沸騰硝酸を用いて除去した。最後に、シリコン基板の裏側にチタンを１００ｎｍ、ニッケルを５００ｎｍ、銀を１００ｎｍ真空蒸着し、下部電極７を形成した。下部電極７はオーム性接合電極である。

【０００９】（４）

図３は各ＨＦ浸漬時間に対する評価デバイス（図２）の電流－電圧特性を示すもので、図２において電極４をプラス（＋）、電極７をマイナス（－）にした時を第一象限に示し（順方向特性）、又極性を逆にした時を第３象限に示した（逆方向特性）ものである。ＨＦ浸漬しない時（酸化膜の厚さ３ｎｍ）図中特性Ａに示すように順方向、逆方向共、電流は全く流れない。ＨＦ浸漬時間を増加するのに伴って電流は両方向共流れ始め酸化膜が厚さ１．５ｎｍで（浸漬時間５０秒）で特性Ｂに示すオーミック特性が得られている。更に浸漬時間を増し約１００秒で酸化膜はなくなり特性Ｃに示す整流特性（ショットキー特性）になった。

【００１０】図４は図３の電流－電圧特性から抵触抵抗の変化を示す値（ΔＲ）のＨＦ浸漬時間依存性を示す特性図で横軸は浸漬時間Ｓ（秒）、縦軸に変化値ΔＲ（ｍΩｃｍ^2）を示す。なお、ΔＲは酸化膜を介さない従来デバイスの抵抗値（図３Ｃ）を基準に算出した。又、この時の抵抗値は第１象限の特性から求めた。この方法により接触抵抗以外の抵抗成分は相殺され、接触抵抗の変化分のみ得られる。ΔＲの値がマイナス（負）であることは従来デバイスより接触抵抗が減少していることを意味する。このマイナス領域は図４から明らかなように浸漬時間で２５秒～９０秒の範囲即ち残余の酸化膜の厚さ２．２５ｎｍ～０．３ｎｍに相当する。

【００１１】図５は酸化法をO_2プラズマ照射法および基板を２ｍΩｃｍにしたとき、接触抵抗が改善されるかどうかを調べるためのデバイス構造を示す。使用したシリコン基板は、抵抗率が２ｍΩｃｍ（不純物濃度：８×10^{19}ｃｍ$^{-3}$）のn^+シリコン基板６を使用した。この構造を作製するため、まず、シリコン基板を希沸酸で１分間洗浄した後、マイクロ波プラズマ照射装置で酸素プラズマをシリコンに照射させた。すなわち、シリコン基板の表側のみに酸素プラズマを照射させ、酸化させた。プラズマパワーを１０００Ｗ、酸素圧を０．５Ｔｏｒｒ、照射時間を２分とした。このときの酸化膜の厚さは２．５ｎｍであった。次に、その酸化膜の厚さを変えるために希沸酸（ＨＦ：H_2O＝１：１００）液中に一定時間だけ浸漬させ、さらに、上部電極４を形成するために、シリコンの上にチタン膜をスパ

（５）

ッタ法で５００ｎｍの厚さに堆積した後、ホトリソグラフィ技術を使って０．９ｍｍ角にパターン化した。チタンの化学エッチングには希沸酸を使用した。エッチング時間は２．５分間である。ホトレジストは、沸騰硝酸を用いて除去した。最後にシリコン基板の裏側にチタンを１００ｎｍ、ニッケルを５００ｎｍ、銀を１００ｎｍ真空蒸着し、下部電極７を形成した。下部電極７はオーム性接合電極である。

【００１２】図６は酸化膜厚に対するデバイスの（図５）電流－電圧特性を示したものである。この特性は、図５において上部電極４をプラス、下部電極７をマイナスにしたときと第１象限に描き、逆の場合を第３象限に描いている。ＨＦ浸漬をしないとき（酸化膜厚：２．５ｎｍ）、電流は順、逆の両方向とも流れていない（Ａ）。ＨＦ浸漬を３０秒行って、酸化膜の厚さを、１．６ｎｍとしたとき、電流－電圧特性Ｂが得られた。さらに、浸漬時間を９０秒行って酸化膜を完全にエッチングすると電流－電圧特性はＣになった。図６から明らかなように、酸化膜を１．６ｎｍ残したときに得られた特性Ｂは酸化膜のないときの特性Ｃよりも抵抗は低減している。特性Ｃにおいてもオーミック特性が得られているのは抵抗率が２ｍΩｃｍの基板を使用したためである。結果として、酸化膜を介した電極構造とすることでより低い接触抵抗を持ったオーミック特性が得られることがわかった。この実施例では、上部電極４の金属膜をチタンとしたが、チタン以外の金属膜たとえばクロムに対しても同様に本発明の効果を確認した。

【００１３】図７は本発明の電極構造にパワーＭＯＳＦＥＴ（６０Ｖ、４０Ａ級）のドレイン電極に適用したＭＯＳＦＥＴの出力特性図で図中特性Ｂは従来例（酸化膜なし）特性Ａは実施例を示す。従来例のドレイン電極構造の出力特性Ｂのオン抵抗は、１９．０４ｍΩであるのに対して、酸化膜を介したドレイン電極構造の出力特性Ａのオン抵抗は、１６．３１ｍΩとなり、酸化膜を介さない電極構造の出力特性のオン抵抗よりも約１４．３％低下した。なお、ＭＯＳＦＥＴはアンチモン添加した抵抗率が１７ｍΩｃｍ（不純物濃度約10^{18}ｃｍ$^{-3}$）シリコン基板にソー

（６）

ス領域、ドレイン領域、ゲート等の能動領域を形成した後、ウェーハの裏側を削って薄くし、その表面に厚さ１．２ｎｍのシリコン酸化膜をシリコン基板の裏側に形成した。その後、チタンを１００ｎｍの厚さだけ真空蒸着し、さらに引き続きニッケルを５００ｎｍ、銀を１００ｎｍの厚さだけ真空蒸着しドレイン電極とした。

【００１４】

【発明の効果】本発明によれば、０．３～２．２５ｎｍのシリコンサブ酸化膜を金属膜とシリコン基板の間にはさむことにより、良好なオーミック接触電極が得られ、高性能デバイスの開発に極めて有効である。

【図面の簡単な説明】

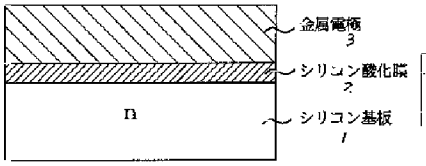
【図１】本発明の実施例を示す断面図

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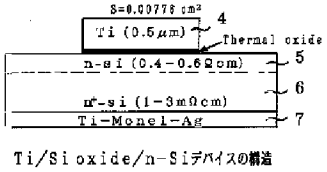
【図２】本発明の有効性を評価するデバイスの構造図
【図３】評価デバイスの電圧－電流特性図
【図４】ＨＦ浸漬時間依存性を示す特性図
【図５】他の評価デバイスの電流－電圧特性図
【図６】評価デバイスの電流－電圧特性図
【図７】本発明をＭＯＳＦＥＴに適用した出力特性図
【符号の説明】

１，６　シリコン基板
２　　シリコンサブ酸化膜
（７）
３　　電極金属
４，７　電極
５　　エピタキシアル層

【図１】

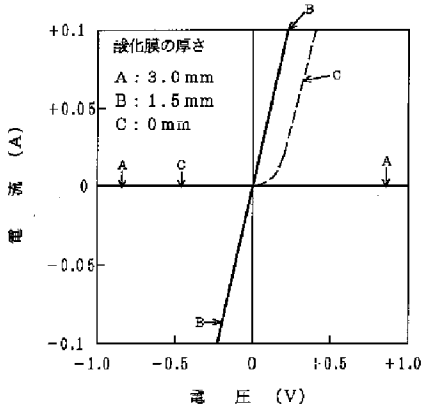


【図２】

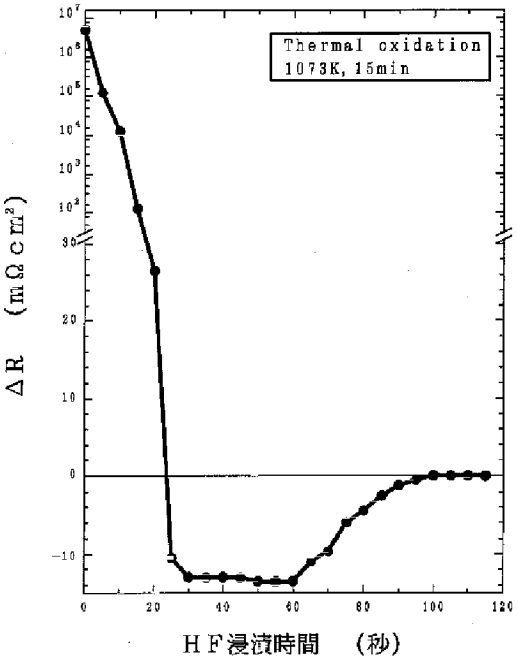


Ti/Si oxide/n-Siデバイスの構造

【図３】

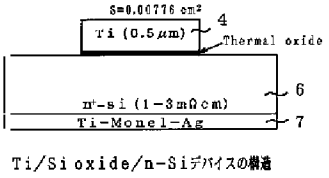


【図４】



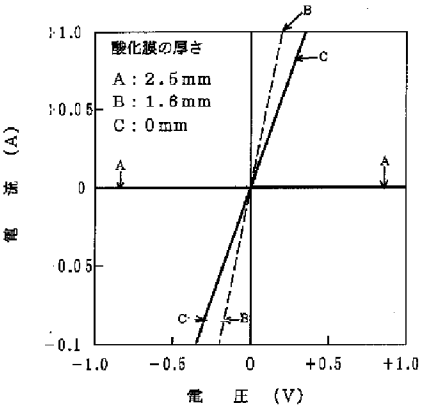
金属／熱酸化膜／ｎ－Ｓｉ構造における
ΔＲの浸漬時間依存性

【図５】



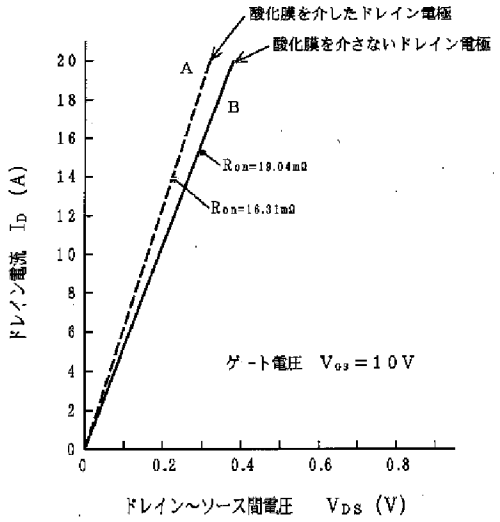
Ti/Si oxide/n-Siデバイスの構造

【図６】



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【図７】


酸化膜を介したドレイン電極
酸化膜を介さないドレイン電極
A
B
Ron=18.04mΩ
Ron=16.31mΩ
ゲート電圧　VGS＝１０Ｖ
ドレイン電流　ID（A）
ドレイン～ソース間電圧　VDS（V）
0
2
4
6
8
10
12
14
16
18
20
0.2
0.4
0.6
0.8

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JPH11162874A OHMIC JOINT ELECTRODE AND SEMICONDUCTOR DEVICE USING THE SAME

Applicants: SHINDENGEN ELECTRIC MFG

Inventors: IWAGURO HIROAKI

Classifications:
IPC ***H01L21/283;*** (IPC1-7): H01L21/283;

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OHMIC JOINT ELECTRODE AND SEMICONDUCTOR DEVICE USING THE SAME

Abstract

PROBLEM TO BE SOLVED: To allow ohmic joint which represents a good low contact resistance even when impurity concentration of a silicon substrate is low, by inserting a silicon sub-oxide film of specific film thickness between the silicon substrate and an ohmic joint metal. SOLUTION: A silicon substrate 1 is oxidized by thermal oxidation method or plasma oxidation method to generate a silicon dioxide (SiO2) 2 on the silicon substrate 1. At true interface between the silicon dioxide 1 and the silicon substrate, a sub-silicon oxide film [SiOx (x=0.5, 1.0, 1.5)] is formed instead of the silicon dioxide (SiO2). The thickness of the sub-silicon oxide film is 0.3-2.25 nm from the interface. In short, the silicon oxide film 2 of electrode structure is a sub oxide film [SiOx (x=0.5, 1.0, 1.5)]. So, a metal film and a sub-silicon oxide film are made to contact each other to obtain ohmic joint representing good and low contact resistance.

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DESCRIPTION JPH11162874

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to an ohmic junction electrode and a semiconductor device using the same.

[0002]

Metal-semiconductor junctions are an important factor in making silicon electronic devices. There are two types of this junction, a Schottky junction that exhibits a rectifying property and an ohmic junction that has no other rectifying property. In order to bring an n-type silicon substrate into contact with a metal to form an ohmic contact electrode exhibiting a good low contact resistance, theoretically, the impurity concentration of the silicon substrate must be 1020 cm-3 or more. Practically, the ohmic junction is made with the impurity concentration of the silicon substrate of 1019 to 1020 cm-3. In order to introduce a large amount of impurities into silicon, methods such as ion implantation, heat treatment, impurity deposition, and thermal diffusion have been used.

[0003]

With the recent increase in the diameter of silicon wafers, the thickness of wafers has increased. In a vertical structure power device, an increase in wafer thickness causes an increase in on-resistance, so in order to suppress this increase in on-resistance, the device on the front surface

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of the wafer is manufactured and then assembled. Then thin the wafer from the back side. After thinning this back side, an ohmic bonding electrode is produced on the back side. However, at this time, the impurity concentration of the silicon substrate is often lower than 10 20 cm −3. Since the device has already been made on the front side and metal wiring such as A1 has been made, high temperature heat treatment is difficult, and impurities are intentionally added to the silicon substrate by ion implantation / heat treatment method or impurity deposition / thermal diffusion method. Cannot be introduced to. It has also been proposed to form an ohmic electrode by providing a thin film containing electric charges on the surface of a semiconductor substrate as shown in JP-A-7-307306.

[0004]

SUMMARY OF THE INVENTION In order to solve the above problems, the present invention provides an ohmic junction exhibiting a good low contact resistance even if the impurity concentration of the silicon substrate is lower than 10 20 cm -3. is there. Usually, when the impurity concentration of the silicon substrate is low, depositing a metal film on the silicon substrate results in Schottky contact between the metal and the silicon substrate. Even in such a case, by interposing the silicon oxide film between the metal and the silicon substrate, an ohmic junction exhibiting a good low contact resistance can be obtained.

[0005]
According to the present invention, a silicon sub oxide film [SiOx (x = 0.5, 1.0, 1.5)] is interposed between a silicon substrate and an ohmic bonding metal. The oxide film has a thickness of 0.3 nm to 2.25 nm.

[0006]

When a silicon substrate is oxidized by a thermal oxidation method or a plasma oxidation method, silicon dioxide (SiO2) is generated on the silicon substrate.

At the interface between the silicon dioxide and the silicon substrate, not the silicon dioxide (SiO2) but the sub-silicon oxide film [SiOx (x = 0.5, 1.0, 1.5)] is formed. The thickness of this sub-silicon oxide film is about 2 nm from the interface. The silicon oxide film of the electrode structure of the present invention is this sub oxide film [SiOx (x = 0.5, 1.0, 1.5)]. By bringing the metal film and the sub-silicon oxide film into contact with each other, an ohmic bond exhibiting

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good and low contact resistance can be obtained. The effect of the present invention is considered to be obtained by the chemical activity of the sub-silicon oxide film, but the detailed reason is not clear. When the silicon dioxide layer and the metal film are brought into contact with each other, the effect is completely lost.

[0007]

FIG. 1 is a sectional view showing an embodiment of the present invention, in which 1 is a silicon substrate, 2 is a silicon sub-oxide film, and 3 is an electrode metal. FIG. 2 shows a device structure for investigating the effectiveness of the oxide film thickness of the present invention. The silicon substrate used is an n + silicon substrate 6 having a resistivity of 2 mΩcm (impurity concentration: 8 × 10 19 cm -3) and a silicon epitaxial layer 5 having a resistivity of 0.5 Ωcm (impurity concentration: 10 16 cm -3) of 5 μm. The grown one was used. This epitaxial surface is mirror-polished, and the surface strain is small.

[0008]

In the manufacturing process for manufacturing the structure of FIG. 2, first, the silicon substrate was washed with dilute hydrofluoric acid for 1 minute and then oxidized at 800 ° C. for 30 minutes using the dry oxidation method. The oxide film thickness is about 3 nm. Next, in order to change the thickness of the oxide film, it was immersed in a dilute hydrofluoric acid (HF: H2O = 1: 100) solution for a certain period of time. It took 100 seconds to completely etch the oxide film having a thickness of 3 nm with this dilute hydrofluoric acid. Further, in order to form the upper electrode 4, a titanium film having a thickness of 500 nm is deposited on the silicon epitaxial layer 5 by a sputtering method, and then a 0.9 mm square is formed by photolithography as shown in FIG. Patterned. Dilute hydrofluoric acid was used for the chemical etching of titanium. The etching time is 2.5 minutes. The photoresist was removed using boiling nitric acid. Finally, 100 nm of titanium, 500 nm of nickel, and 100 nm of silver were vacuum-deposited on the back side of the silicon substrate to form the lower electrode 7. The lower electrode 7 is an ohmic junction electrode.

[0009]

(4) FIG. 3 shows the current-voltage characteristics of the evaluation device (FIG. 2) with respect to each HF immersion time, and shows the results when the electrode 4 is positive (+) and the

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electrode 7 is negative (−) in FIG. It is shown in one quadrant (forward characteristic), and when the polarity is reversed is shown in the third quadrant (reverse characteristic). When not immersed in HF (thickness of oxide film: 3 nm), no current flows in both forward and reverse directions as indicated by characteristic A in the figure. As the HF immersion time is increased, the current starts to flow in both directions, and the ohmic characteristics shown in the characteristic B are obtained when the oxide film has a thickness of 1.5 nm (immersion time is 50 seconds). When the immersion time was further increased and the oxide film disappeared after about 100 seconds, the rectifying characteristic (Schottky characteristic) shown in characteristic C was obtained.

[0010]

FIG. 4 is a characteristic diagram showing the HF immersion time dependency of the value (ΔR) indicating the change in contact resistance from the current-voltage characteristics of FIG. 3, in which the horizontal axis represents the immersion time S (seconds) and the vertical axis represents the change value ΔR (mΩcm 2) Is shown. Note that ΔR was calculated based on the resistance value (FIG. 3C) of the conventional device without the oxide film. The resistance value at this time was obtained from the characteristics of the first quadrant. By this method, the resistance components other than the contact resistance are canceled out, and only the change in the contact resistance is obtained. The minus (negative) value of ΔR means that the contact resistance is smaller than that of the conventional device. As is apparent from FIG. 4, this minus region corresponds to a range of 25 seconds to 90 seconds in the immersion time, that is, a remaining oxide film thickness of 2.25 nm to 0.3 nm.

[0011]

FIG. 5 shows a device structure for investigating whether the contact resistance is improved when the oxidation method is O2 plasma irradiation method and the substrate is 2 mΩcm. As the silicon substrate used, an n + silicon substrate 6 having a resistivity of 2 mΩcm (impurity concentration: 8×10^{19} cm $^{-3}$) was used. In order to manufacture this structure, first, the silicon substrate was washed with dilute hydrofluoric acid for 1 minute, and then oxygen plasma was applied to the silicon with a microwave plasma irradiation device. That is, only the front side of the silicon substrate was irradiated with oxygen plasma for oxidation. The plasma power was 1000 W, the oxygen pressure was 0.5 Torr, and the irradiation time was 2 minutes. At this time, the thickness of the oxide film was 2.5 nm. Next, in order to change the thickness of the oxide film, it is dipped in a dilute hydrofluoric acid (HF: H2O = 1: 100) solution for a certain period of time, and titanium is deposited on silicon to form the upper electrode 4. The film was deposited

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by sputtering to a thickness of 500 nm and then patterned into 0.9 mm square using photolithography technology. Dilute hydrofluoric acid was used for the chemical etching of titanium. The etching time is 2.5 minutes. The photoresist was removed using boiling nitric acid. Finally, 100 nm of titanium, 500 nm of nickel and 100 nm of silver were vacuum-deposited on the back side of the silicon substrate to form the lower electrode 7. The lower electrode 7 is an ohmic junction electrode.

[0012]

FIG. 6 shows the current-voltage characteristics of the device (FIG. 5) with respect to the oxide film thickness. This characteristic is drawn in the first quadrant as compared with the case where the upper electrode 4 is made positive and the lower electrode 7 is made negative in FIG. 5, and the opposite case is drawn in the third quadrant. When not immersed in HF (oxide film thickness: 2.5 nm), current does not flow in both forward and reverse directions (A). When the HF immersion was performed for 30 seconds and the thickness of the oxide film was set to 1.6 nm, the current-voltage characteristic B was obtained. Further, when the immersion time was 90 seconds to completely etch the oxide film, the current-voltage characteristic became C. As is clear from FIG. 6, the characteristic B obtained when the oxide film is left to have a thickness of 1.6 nm is lower in resistance than the characteristic C when the oxide film is not present. In the characteristic C, the ohmic characteristic is obtained because the substrate having the resistivity of 2 mΩcm is used. As a result, it was found that the ohmic characteristics with lower contact resistance can be obtained by using the electrode structure with the oxide film interposed. In this example, the metal film of the upper electrode 4 was titanium, but the effect of the present invention was similarly confirmed for metal films other than titanium, such as chromium.

[0013]

FIG. 7 is an output characteristic diagram of a MOSFET applied to the drain electrode of a power MOSFET (60 V, 40 A class) in the electrode structure of the present invention. In the figure, characteristic B shows a conventional example (no oxide film) and characteristic A shows an example. The on-resistance of the output characteristic B of the drain electrode structure of the conventional example is 19.04 mΩ, while the on-resistance of the output characteristic A of the drain electrode structure through the oxide film is 16.31 mΩ, and the oxide film It was about 14.3% lower than the on resistance of the output characteristics of the electrode structure without the interposition. The MOSFET has an antimony-added resistivity of 17 mΩcm (impurity concentration of about 10 18 cm -3) After forming active regions such as a source region, a drain region, and a gate on a silicon substrate, the back side of the wafer is ground and thinned, A

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silicon oxide film having a thickness of 1.2 nm was formed on the back side of the silicon substrate. Then, titanium was vacuum-deposited to a thickness of 100 nm, and then nickel was vacuum-deposited to a thickness of 500 nm and silver to a thickness of 100 nm to form a drain electrode.

[0014]
According to the present invention, by sandwiching a silicon sub-oxide film of 0.3 to 2.25 nm between a metal film and a silicon substrate, a good ohmic contact electrode can be obtained and a high performance device can be developed. It is extremely effective for

[0015]
Brief description of the drawings

[0016]
1 is a sectional view showing an embodiment of the present invention

[0017]
Fig. 2 Structural diagram of device for evaluating effectiveness of the present invention

[0018]
Figure 3 Voltage-current characteristic diagram of the evaluation device

[0019]
Figure 4 Characteristic diagram showing HF immersion time dependence

[0020]
Figure 5 Current-voltage characteristics of other evaluation devices

[0021]
Figure 6 Current-voltage characteristic diagram of the evaluation device

[0022]

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Fig. 7 Output characteristic diagram in which the present invention is applied to a MOSFET

[0023]

Explanation of symbols

[0024]

1,6 Silicon substrate 2 Silicon sub oxide film (7) 3 Electrode metal 4,7 Electrode 5 Evitaxial layer

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1.
A silicon sub oxide film [SiOx (x = 0.5, 1.0, 1.5)] is interposed between the silicon substrate and the ohmic bonding metal, and the thickness of the oxide film is 0.3 nm to 2. An ohmic contact electrode having a thickness of 25 nm.

2.
The ohmic contact electrode according to claim 1, wherein an n-type silicon substrate is used and the impurity concentration of the substrate is set to 10 16 cm -3 to 10 20 cm -3.

3.
An active region is formed on a silicon substrate, and an electrode metal is bonded to the front surface or the back surface of the silicon substrate through a silicon sub oxide film [SiOx (x = 0.5, 1.0, 1.5)]. Semiconductor device.

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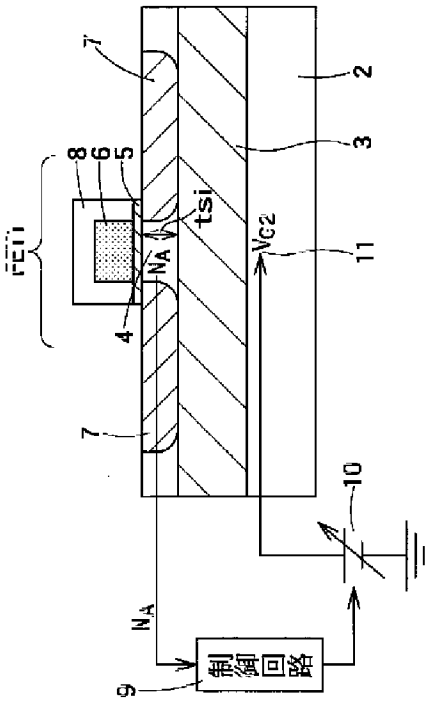
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(71)出願人　000003078
株式会社東芝
神奈川県川崎市幸区堀川町72番地
(72)発明者　沼　田　敏　典
神奈川県川崎市幸区小向東芝町１　株式会社東芝研究開発センター内
(72)発明者　野　口　充　宏
神奈川県横浜市磯子区新杉田町８番地　株式会社東芝横浜事業所内
(74)代理人　弁理士　佐藤　一雄　（外３名）

(54)【発明の名称】　半導体装置

(57)【要約】
【課題】　ＳＯＩ層を用いた完全空乏化ＭＩＳＦＥＴトランジスタを形成してなる半導体装置において、ＭＩＳＥＴのチャネル不純物濃度に依存して、バックゲート電圧を変化させることによって、不純物濃度が変動しても、ＳＯＩ膜厚バラツキに対するしきい値感度をほぼ極小に保ったままで、しきい値を規定する値にできるようにする半導体装置を提供することを目的とする。
【解決手段】　ＳＯＩ層の膜厚を、しきい値変動が小さくなる膜厚に設定する。さらに、ダミー素子を用いてチャネル領域の不純物濃度を測定し、その測定値に基づいてバックゲート電圧を調節することにより所望のしきい値を維持することができる。



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【特許請求の範囲】
【請求項１】バックゲートが形成されてなる支持基板と、
前記支持基板上に設けられた絶縁膜と、
前記絶縁膜上に設けられた第１の半導体層と、
前記支持基板の前記バックゲートに対向して前記第１の半導体層の一部をチャネル領域としたＭＩＳＦＥＴトランジスタと、
前記第１の半導体層の不純物濃度またはキャリア濃度に応じて変化する測定信号を出力するダミー素子と、
前記ダミー素子から出力される前記測定信号に応じて前記バックゲートに電圧を印加する電圧印加手段と、
を備えたことを特徴とする半導体装置。
【請求項２】第１及び第２のバックゲートが形成されてなる支持基板と、
前記支持基板上に設けられた絶縁膜と、
前記絶縁膜上に設けられ第１の膜厚を有する第１の半導体層と、
前記支持基板の前記第１のバックゲートに対向して前記第１の半導体層の一部をチャネル領域とした第１のＭＩＳＦＥＴトランジスタと、
前記絶縁膜上に設けられ前記第１の膜厚とは異なる第２の膜厚を有する第２の半導体層と、
前記支持基板の前記第２のバックゲートに対向して前記第２の半導体層の一部をチャネル領域とした第２のＭＩＳＦＥＴトランジスタと、
前記第１のバックゲートに、前記第２のバックゲートの電圧とは独立に電圧を印加する電圧印加手段と、
を備えたことを特徴とする半導体装置。
【請求項３】バックゲートが形成されてなる支持基板と、
前記支持基板上に設けられた絶縁膜と、
前記絶縁膜上に設けられた第１の半導体層と、
前記支持基板の前記バックゲートに対向して前記第１の半導体層の一部をチャネル領域としたＭＩＳＦＥＴトランジスタと、
前記バックゲートに印加する電圧に対応する情報を記憶する記憶素子と、
前記記憶素子に記憶された前記情報に基づいて前記バックゲートに電圧を印加する電圧印加手段と、
を備えたことを特徴とする半導体装置。
【請求項４】第１及び第２のバックゲートが形成されてなる支持基板と、
前記支持基板上に設けられた絶縁膜と、
前記絶縁膜上に設けられ第１の膜厚を有する第１の半導体層と、
前記支持基板の前記第１のバックゲートに対向して前記第１の半導体層の一部をチャネル領域とした第１のＭＩＳＦＥＴトランジスタと、
前記第１のバックゲートに印加する電圧に対応する情報を記憶する第１の記憶素子と、
前記絶縁膜上に設けられ前記第１の膜厚とは異なる第２の膜厚を有する第２の半導体層と、
前記支持基板の前記第２のバックゲートに対向して前記第２の半導体層の一部をチャネル領域とした第２のＭＩＳＦＥＴトランジスタと、
前記第２のバックゲートの電圧とは独立に、前記第１の記憶素子に記憶された前記情報に基づいて前記第１のバックゲートに電圧を印加する電圧印加手段と、
を備えたことを特徴とする半導体装置。
【請求項５】前記記憶素子は、前記第１の半導体層の不純物濃度またはキャリア濃度に応じた情報を記憶することを特徴とする請求項３または４に記載の半導体装置。
【請求項６】前記ＭＩＳＦＥＴトランジスタは、前記チャネル領域が完全に空乏化した完全空乏型トランジスタであることを特徴とする請求項１～５のいずれか１つに記載の半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置に関する。より具体的には、本発明は、支持基板上に絶縁膜を介して設けられた半導体層上に完全空乏化ＭＩＳＦＥＴ（Metal Insulator Semiconductor Field Effect Transistor）を形成してなる半導体装置に関する。
【０００２】
【従来の技術】ＳＯＩ（Silicon on Insulator）すなわち絶縁性の基板上に形成された半導体層を用いて形成されたＦＥＴ型トランジスタは、ソース・ドレイン間の寄生容量を、バルク（bulk）の半導体基板上に形成したＦＥＴより小さくすることができることから、低消費電力デバイスあるいは高速ＣＰＵなどの高速動作回路への応用が期待されている。特に、半導体層であるＳＯＩ膜の厚さをチャネル領域の空乏層の厚さ以下にすると、チャネル領域を完全に空乏化することができる。その結果として、空乏層より厚い半導体層を用いて形成されたＳＯＩトランジスタで問題となるキンク特性や電流オーバーシュート効果などの好ましくない現象を、解消または抑制することができる。
【０００３】このようにチャネル領域を全て空乏化することができるトランジスタ（以下、これを「完全空乏化トランジスタ」と呼ぶ）は、さらに、短チャネル効果の抑制、パンチスルー耐性の向上、サブスレッショルド係数の改善、チャネル移動度の増大などの多岐にわたる利点が得られる。
【０００４】
【発明が解決しようとする課題】しかし、完全空乏化トランジスタには、例えば、プロセス条件のバラツキによって、チャネル領域の半導体層の不純物濃度やＳＯＩ膜厚が変化すると、しきい値が変化してしまうという問題があった。

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【０００５】このようなプロセス条件のバラツキに起因する問題に対処する方法として、従来、例えば、特開平９－３１２４０１号公報において開示されているように、ＳＯＩ層の下の絶縁層の下の支持基板にバックゲートを設け、そのバックゲートに印加する電圧を動作時と待機時とで変化させて、しきい値を制御する例が知られている。

【０００６】しかし、この方法においては、バックゲートの電圧は、ＳＯＩ膜厚のバラツキや基板濃度のバラツキに無関係に決定される。そして、例えばＳＯＩ膜厚バラツキに対するしきい値感度を極小にするバックゲート電圧印加手段やその具体的な構成については何ら開示されていなかった。

【０００７】つまり、従来の完全空乏化トランジスタにおける、しきい値感度を低減する手法および構造では、ＳＯＩ膜厚バラツキに対するしきい値感度を低減するためのバックゲート電圧制御について検討されてきたが、ＳＯＩ膜厚の最適値や、不純物濃度との関係については考慮されていなかった。そのため、しきい値を規定の値に設定し、かつＳＯＩ層の膜厚や不純物濃度のバラツキに対するしきい値感度を小さくすることは困難であった。

【０００８】本発明は、かかる課題の認識に基づいてなされたものである。すなわち、その目的とするところは、ＳＯＩ層を用いた完全空乏化ＭＩＳＦＥＴトランジスタを形成してなる半導体装置において、ＭＩＦＳＥＴのチャネル不純物濃度に依存して、バックゲート電圧を変化させることによって、不純物濃度が変動しても、ＳＯＩ膜厚バラツキに対するしきい値感度をほぼ極小に保ったままで、しきい値を規定する値にできるようにする半導体装置を提供することにある。

【０００９】

【課題を解決するための手段】本発明の骨子は、絶縁膜を介してバックゲートと対向した半導体層に、完全空乏化トランジスタを形成してなる半導体装置において、前記トランジスタのチャネル不純物濃度に応じてバックゲート電圧を制御できる制御回路を設け、不純物濃度に応じたバックゲート電圧をバックゲートに印加することを特徴とする半導体装置を提供することにある。

【００１０】なお、完全空乏化ＳＯＩトランジスタを形成する半導体層は、規定のしきい値で、しきい値変動が小さくなるＳＯＩ膜厚に設定し、さらに、不純物濃度に関しては、半導体層の絶縁膜に接した表面がaccumulationとinversion とで決まる範囲内に、例えば中間に、設定する。ここで、規定のしきい値が異なると、それぞれしきい値変動が抑えられる膜厚が異なる。

【００１１】すなわち、本発明の半導体装置は、バックゲートが形成されてなる支持基板と、前記支持基板上に設けられた絶縁膜と、前記絶縁膜上に設けられた第１の半導体層と、前記支持基板の前記バックゲートに対向して前記第１の半導体層の一部をチャネル領域としたＭＩＳＦＥＴトランジスタと、前記第１の半導体層の不純物濃度またはキャリア濃度に応じて変化する測定信号を出力するダミー素子と、前記ダミー素子から出力される前記測定信号に応じて前記バックゲートに電圧を印加する電圧印加手段と、を備えたことを特徴とする。

【００１２】または、本発明の半導体装置は、第１及び第２のバックゲートが形成されてなる支持基板と、前記支持基板上に設けられた絶縁膜と、前記絶縁膜上に設けられ第１の膜厚を有する第１の半導体層と、前記支持基板の前記第１のバックゲートに対向して前記第１の半導体層の一部をチャネル領域とした第１のＭＩＳＦＥＴトランジスタと、前記絶縁膜上に設けられ前記第１の膜厚とは異なる第２の膜厚を有する第２の半導体層と、前記支持基板の前記第２のバックゲートに対向して前記第２の半導体層の一部をチャネル領域とした第２のＭＩＳＦＥＴトランジスタと、前記第１のバックゲートに、前記第２のバックゲートの電圧とは独立に電圧を印加する電圧印加手段と、を備えたことを特徴とする。

【００１３】または、本発明の半導体装置は、バックゲートが形成されてなる支持基板と、前記支持基板上に設けられた絶縁膜と、前記絶縁膜上に設けられた第１の半導体層と、前記支持基板の前記バックゲートに対向して前記第１の半導体層の一部をチャネル領域としたＭＩＳＦＥＴトランジスタと、前記バックゲートに印加する電圧に対応する情報を記憶する記憶素子と、前記記憶素子に記憶された前記情報に基づいて前記バックゲートに電圧を印加する電圧印加手段と、を備えたことを特徴とする。

【００１４】または、本発明の半導体装置は、第１及び第２のバックゲートが形成されてなる支持基板と、前記支持基板上に設けられた絶縁膜と、前記絶縁膜上に設けられ第１の膜厚を有する第１の半導体層と、前記支持基板の前記第１のバックゲートに対向して前記第１の半導体層の一部をチャネル領域とした第１のＭＩＳＦＥＴトランジスタと、前記第１のバックゲートに印加する電圧に対応する情報を記憶する第１の記憶素子と、前記絶縁膜上に設けられ前記第１の膜厚とは異なる第２の膜厚を有する第２の半導体層と、前記支持基板の前記第２のバックゲートに対向して前記第２の半導体層の一部をチャネル領域とした第２のＭＩＳＦＥＴトランジスタと、前記第２のバックゲートの電圧とは独立に、前記第１の記憶素子に記憶された前記情報に基づいて前記第１のバックゲートに電圧を印加する電圧印加手段と、を備えたことを特徴とする。

【００１５】ここで、前記記憶素子は、前記第１の半導体層の不純物濃度またはキャリア濃度に応じた情報を記憶することを特徴とする。

【００１６】また、前記ＭＩＳＦＥＴトランジスタは、前記チャネル領域が完全に空乏化した完全空乏型トラン

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ジスタであることを特徴とする。
【００１７】また、前記ダミー素子は、前記第１または第２の半導体層の不純物濃度またはキャリア濃度に応じてその抵抗値、容量値、またはインダクタンスの少なくともいずれかが変化するインピーダンス素子であることを特徴とする。
【００１８】また、前記ＭＩＳＦＥＴトランジスタのチャネル領域が形成された前記第１または第２の半導体層の厚さは、４０ｎｍ乃至１００ｎｍの範囲にあり、不純物濃度は3×10^{16}ｃｍ$^{-3}$乃至3×10^{17}ｃｍ$^{-3}$の範囲にあることを特徴とする。
【００１９】また、前記支持基板は、半導体基板で形成され、前記バックゲートの不純物濃度は1×10^{17}ｃｍ$^{-3}$乃至1×10^{20}ｃｍ$^{-3}$の範囲にあることを特徴とする。
【００２０】また、前記ダミー素子により前記不純物濃度または前記キャリア濃度を測定する回路がＭＩＳＦＥＴトランジスタと同一の半導体層上に設けられていることを特徴とする。
【００２１】また、前記第１の半導体層は前記第２の半導体層よりも膜厚が厚く、且つ、前記第１の半導体層は、前記第２の半導体層よりも不純物濃度が低いことを特徴とする。
【００２２】また、前記第１のＭＩＳＦＥＴトランジスタのしきい値は、前記第２のＭＩＳＦＥＴトランジスタのしきい値より小さいことを特徴とする。
【００２３】
【発明の実施の形態】本発明によれば、ＳＯＩ層の膜厚を、しきい値変動が小さくなる膜厚に設定する。さらに、ダミー素子を用いてチャネル領域の不純物濃度を測定し、その測定値に基づいてバックゲート電圧を調節することにより所望のしきい値を維持することができる。よって、完全空乏化トランジスタで問題となるＳＯＩ膜厚や不純物濃度のバラツキに対するしきい値感度をほぼ最小に保ったままで、かつしきい値を所望の値にすることが可能である。
【００２４】以下に図面を参照しつつ本発明の実施の形態について説明する。なお、以下の説明では、ｎ型ＭＯＳＦＥＴを例に挙げて説明する。また、ＳＯＩ層の素子分離のパターン形状については、本発明においては本質的ではないので特に触れない。
【００２５】図１は、本発明の第１の具体例に係わる半導体装置を表す要部断面図である。すなわち、同図において、６はゲート電極、７はソース・ドレイン領域、２は支持基板、３は絶縁膜、４はチャネル領域、５はゲート絶縁膜、８は絶縁膜、９は制御回路、１０は可変電源（例えば出力電流または電圧を制御入力の電圧または電流によって制御する電源）、そして１１はバックゲートを表す。
【００２６】その具体的な構成例について説明すれば、以下の如くである。すなわち、シリコンからなる支持基板２の主面上に、例えば厚さ１０ｎｍ～１μｍのシリコン酸化膜やシリコン窒化膜からなる絶縁膜３が形成され、この絶縁膜３上に膜厚t_{si}、ボロンまたはインジウムなどのｐ型不純物濃度N_Aを有するシリコンなどからなるチャネル領域４が形成されている。膜厚t_{si}は、例えば１ｎｍ～５００ｎｍとし、不純物濃度N_Aは、例えば10^{16}～10^{19}ｃｍ$^{-3}$とすることができる。
【００２７】このチャネル領域４の上に、ゲート絶縁膜５を介して、ゲート電極６が形成されている。ゲート絶縁膜５の材料としては、例えば、シリコン酸化膜、シリコン窒化膜、タンタル酸化膜、チタン酸化膜などを用いることができ、その厚さは１ｎｍ～２００ｎｍとすることができる。ゲート電極６の材料としては、例えば、多結晶シリコン、アルミニウム（Ａｌ）、タングステン（Ｗ）、チタンナイトライド（ＴｉＮ）などを用いることができ、その厚さは１０ｎｍ～１μｍとすることができる。
【００２８】そして、このゲート電極６は、その側壁を例えばシリコン酸化膜、シリコン窒化膜からなる絶縁膜８で覆われて絶縁されている。チャネル領域４の両側には、ｎ型不純物となる砒素（Ａｓ）、リン（Ｐ）、アンチモン（Ｓｂ）などを、例えば10^{18}～10^{21}ｃｍ$^{-3}$添加したソース・ドレイン領域７が形成されている。ここでチャネル領域４は、チャネル領域４と絶縁膜５との界面に反転層が形成された状態で完全に空乏化しており、完全空乏化トランジスタＦＥＴ１を形成している。
【００２９】一方、制御回路９は、後に詳述するように、半導体層、特にチャネル領域４における不純物濃度N_Aを測定する図示しないダミー素子からの電圧、電流、容量または抵抗値の情報を入力して最適なバックゲート電圧値を算出し、それに対応する制御信号を出力する。可変電源１０は、制御回路９から出力された制御信号に基づいて所定のバックゲート電圧をバックゲート１１に印加する。
【００３０】次に、図１に示した半導体装置の製造工程を説明する。ここでは、支持基板２としてシリコン基板、絶縁膜３としてシリコン酸化膜、そしてチャネル領域４やソース・ドレイン領域７としてシリコンからなるＳＯＩ層をそれぞれ用いることとする。このようなＳＯＩ基板の作成方法としては、片面を酸化した２枚のシリコン基板を酸化膜面を密着させ１０００～１２００℃で熱処理して張り合わせる方法を用いることができる。または、シリコン基板に酸素イオンを、加速電圧１６０ｋｅＶドーズ量$1.5\sim3.0\times10^{18}$ａｔｏｍ／ｃｍ^{2}程度の条件でイオン注入し、１３００～１３５０℃で熱処理することにより、埋め込み酸化膜３を形成する方法でもよい。
【００３１】絶縁膜３上の半導体層は、ポリッシングやイオンエッチング、あるいはウェットエッチングにより

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薄膜化し、４０ｎｍ～１μｍの厚さの均一なＳＯＩ膜を形成する。

【００３２】次に、バックゲート１１として、リソグラフィとイオン注入により支持基板２に不純物添加領域を形成する。すなわち、リソグラフィによりＭＩＳＦＥＴトランジスタを形成する領域の絶縁膜３を介して支持基板２へ例えば、燐（Ｐ）またはヒ素（Ａｓ）を、加速電圧５０～７００ｋｅＶ、ドーズ量1×10^{13}～1×10^{16}ａｔｏｍ／ｃｍ^2 程度の条件で注入することにより、バックゲート１１を形成することができる。但し、このようなバックゲート１１の形成工程は、絶縁膜３やＳＯＩ層４の形成よりも前に行うようにしても良い。

【００３３】次に、チャネル領域４の不純物濃度が1×10^{16}ｃｍ$^{-3}$～1×10^{19}ｃｍ$^{-3}$の範囲になるようにイオン注入する。

【００３４】この後、ゲート酸化膜５を形成し、さらにゲート電極６や絶縁膜８を形成することにより、ＭＩＳＦＥＴ１の要部が完成する。

【００３５】以上説明した製造工程においては、特に、完全空乏化ＳＯＩトランジスタでしきい値を－０．１～０．４Ｖの範囲に設定するために、チャネル層４のＳＯＩ膜厚、不純物濃度をそれぞれ４０ｎｍ～１μｍ、3×10^{16}ｃｍ$^{-3}$～3×10^{17}ｃｍ$^{-3}$の範囲とすることが望ましい。

【００３６】次に、本発明の半導体装置におけるチャネル領域４のＳＯＩ膜厚t_{si}、不純物濃度N_A、そしてバックゲート電圧V_{G2}の最適範囲について説明する。

【００３７】図２は、本発明者の計算により得られた完全空乏化ＦＥＴのＳＯＩ層としきい値との関係を表すグラフ図である。ここでは、絶縁体基板３として膜厚８０ｎｍのシリコン酸化膜、バックゲート１１に1×10^{20}ｃｍ$^{-3}$のｐ型Ｓｉ基板、ゲート電極６として1×10^{20}ｃｍ$^{-3}$のｎ型ポリシリコン（多結晶シリコン）、そしてゲート酸化膜５としてシリコン酸化膜３ｎｍからなるｎ型ＭＯＳＦＥＴをモデルとした。そして、バックゲート電圧を０Ｖ、チャネル領域４の不純物濃度1×10^{17}ｃｍ$^{-3}$とした時の、チャネル領域４の膜厚すなわちＳＯＩ膜厚t_{si}としきい値Ｖthの関係を図２において実線で示した。

【００３８】このグラフ図に示した関係の算出にあたっては、完全空乏化トランジスタのしきい値を表す式として文献（“Electrical characterization of Silicon-on-Insulator Materials and Devices ”Sorin Cristlovеanu and Sheng S.Li 著、Kluwer Academic Publishers,（1995））に記載されているものと同様の式を用い、さらに表面量子効果として文献（M.J.van Dort, P.H.Woerlee, A.J.Walker, C.A.H.Juffermans and H.Lifka: IEDM91 p495,（1991））、（J.W.Slotboom and H.C.de Graaff, IEEE trans. Electron Devices, vol.ED-24, No.8,pp.1123-1125,(1977)）、（「デバイス物理のための量子力学」David K.Ferry 著、長岡洋介他訳、丸善、（１９９６））に記載されているものを考慮した。

【００３９】図２からわかるように、トランジスタのしきい値は、チャネル領域４の膜厚t_{si}に対して、極小値（図２中の矢印）を有する。この極小値の付近においては、膜厚t_{si}の変化に対して、しきい値の変化量が最小となる。つまり、ＳＯＩ層の膜厚のバラツキに対する、しきい値感度は極めて小さくなる。

【００４０】また、バックゲート電圧を印加することにより、チャネル領域４のうちの絶縁膜３に接した表面の電子状態が蓄積（図２中の破線$V_{th1,ac2}$）、または反転（図２中の破線$V_{th1,inv2}$）となる範囲内で、しきい値を変えることができる。従って、所定のバックゲート電圧を印加することにより、しきい値を制御して、設定したいしきい値が図２での極小値と一致するようにチャネル領域４の膜厚を形成した完全空乏化トランジスタは、設定した値でＳＯＩ膜厚バラツキに対するしきい値感度をほぼ最小とすることができる。

【００４１】次に、図２に示したようなＳＯＩのしきい値の計算方法について詳細に説明する。以下の説明では、まず、古典論モデルに基づく計算方法について説明し、次にチャネル反転層の表面量子化の効果の補正を加えた計算方法について説明する。

【００４２】まず、バックゲート電圧を印加できる完全空乏化トランジスタにおいては、しきい値は、チャネル領域４の絶縁膜３に接した表面における電子状態に依存する。そして、絶縁膜３に接したチャネル領域４の表面の状態はバックゲート電圧により、蓄積状態から反転状態まで変化させることが可能である。

【００４３】この時のゲート電圧V_{G1}と表面ポテンシャルとの関係は次式で表される。

【００４４】

【数１】

$$V_{G1}=\Phi_{MS1}-\frac{Q_{OX1}}{C_{OX1}}+\left(1+\frac{C_{Si}}{C_{OX1}}\right)\Phi_{S1}-\frac{C_{Si}}{C_{OX1}}\Phi_{S2}-\frac{\frac{1}{2}Q_{depl}+Q_{invl}}{C_{OX1}} \qquad (1)$$

ここで、Φ_{s1}、Φ_{s2}はそれぞれチャネル領域４のゲート絶縁膜５に接した表面、絶縁膜３に接した表面でのフェルミポテンシャル、Φ_{Ms1} はゲート絶縁膜５側のゲート電極６との仕事関数の差、Q_{OX1} はゲート絶縁膜５中の固定電荷密度、C_{OX1} はゲート絶縁膜５のキャパシタンス、Q_{invl}はチャネル領域４におけるチャネルの反転層電荷を表す。また、Q_{depl}はチャネル領域４での空乏層電荷を表し、電子の電荷量ｑ、チャネル領域４の不純物

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濃度N_A、チャネル領域４の膜厚t_{si}を用いて$-qN_At_{si}$で表される。また、フェルミポテンシャルΦpは、シリコンの真性キャリア密度n_i、ボルツマン定数k、温度T、電子の電荷量qを用いて、$\Phi p = (kT/q)\ln(N_A/n_i)$と表され、また、$C_{si}=\varepsilon_{si}/t_{si}$である（$\varepsilon_{si}$はシリコンの誘電率）。

【００４５】完全空乏化トランジスタのしきい値V_{th}は、絶縁膜３に接した側のチャネル領域４の表面の電子状態によって以下のように場合分けして表すことができる。なお、$V_{G1}=V_{th}$となる時の表面ポテンシャルΦ_{si}とチャネルの反転層電荷Q_{inv1}は、ゲート電圧がしきい値である条件からそれぞれ$\Phi_{si}=2\Phi_F$、$Q_{inv1}=0$となる。

【００４６】①back surfaceが蓄積（accumulation）した時は、$\Phi_{s2}=0$より

【００４７】

【数２】

$$V_{th1,acc2}=\Phi_{MS1}-\frac{Q_{OX1}}{C_{OX1}}+\left(1+\frac{C_{Si}}{C_{OX1}}\right)2\Phi_F-\frac{Q_{depl}}{2C_{OX1}} \qquad (2)$$

ここで$V_{th1,acc2}$の添字である「１」と「２」は、チャネル領域４のゲート絶縁膜５と接する表面、絶縁膜３と接する表面での状態をそれぞれ表す。式（２）の場合は、絶縁膜３に接したチャネル領域４の表面が蓄積状態である場合を示している。

【００４８】②back surfaceが反転（inversion）した時は、$\Phi_{s2}=2\Phi_F$より

【００４９】

【数３】

$$V_{th1,inv2}=\Phi_{MS1}-\frac{Q_{OX1}}{C_{OX1}}+2\Phi_F-\frac{Q_{depl}}{2C_{OX1}} \qquad (3)$$

③back surfaceが空乏（depletion）した時は、そのポテンシャルは蓄積時と反転時の中間となり、Φ_{s2}はバックゲート電圧V_{G2}に依存する。この時、絶縁膜３と接したチャネル領域４の表面が蓄積、反転した時のバックゲート電圧V_{G2}をそれぞれ$V_{G2,acc}$、$V_{G2,inv}$とすると、$V_{G2,acc}<V_{G2}<V_{G2,inv}$の条件を満たす。さらに、チャネル領域４の容量$C_{si}$、および絶縁膜３の容量$C_{OX2}$が直列に接続されているから、Φs2は、

【００５０】

【数４】

$$\Phi_{S2}=\frac{C_{OX2}}{(C_{si}+C_{OX2})}(V_{G2}-V_{G2,acc})$$

と表される。よってしきい値は次式で表される。

【００５１】

【数５】

$$V_{th1,depl2}=V_{th1,acc2}-\frac{C_{Si}C_{OX2}}{C_{OX1}(C_{Si}+C_{OX2})}(V_{G2}-V_{G2,acc}) \qquad (4)$$

ここで$V_{G2,acc}$は絶縁膜３について表面と対称であると考えて、$\Phi_{s1}=2\Phi_F$、$\Phi_{s2}=0$の条件から以下のようになる。

【００５２】

【数６】

$$V_{G2,acc}=\Phi_{MS2}-\frac{Q_{OX2}}{C_{OX2}}-\frac{C_{Si}}{C_{OX2}}2\Phi_F-\frac{Q_{depl}}{2C_{OX2}} \qquad (5)$$

図３は、式（２）～（５）により、チャネル領域４の不純物濃度$N_A=1\times10^{17}cm^{-3}$、ＳＯＩ膜厚$t_{si}=60nm$、$\Phi_{Ms1}=-1V$、$Q_{OX1}=Q_{OX2}=0$の場合について計算したバックゲート電圧に対するしきい値の関係を表したグラフである。完全空乏化トランジスタにおいて、チャネル領域４の絶縁膜３に接する表面での電子状態が、反転または蓄積になると、その表面でのポテンシャルΦ_{s2}は一定となる。このため、それ以上のバックゲート電圧を印加してもしきい値はバックゲート電圧に依存せず一定値となる。つまり、完全空乏化トランジスタのしきい値は、チャネル領域４の絶縁膜３に接した表面の電子状態が、蓄積した時のしきい値と反転した時のしきい値の範囲内に限定される。

【００５３】図４は、チャネル領域４の不純物濃度を$1\times10^{17}cm^{-3}$としたときの、式（２）～（５）の古典論モデルを用いて計算したしきい値のチャネル領域４のＳＯＩ膜厚の依存性を示したグラフである。同図においては、$V_{th1,acc2}$を破線、$V_{th1,inv2}$を点線で、そして$V_{G2}=0V$におけるＳＯＩ膜厚に対するしきい値を実線で示している。$V_{th1,acc2}$、$V_{th1,inv2}$はV_{G2}に依存せずチャネル領域４の膜厚により決まる。一方$V_{th1,depl2}$はバックゲート電圧V_{G2}によりしきい値が変化する。図４からわかるように、古典論モデルでの$V_{th1,depl2}$はＳＯＩ膜厚が薄くなるとＳＯＩ空乏層に含まれる空乏層電荷（$-Q_{depl}$）が減少するため線形に減少する。

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【００５４】次に、以上説明した古典論モデルにチャネル反転層の表面量子化補正を加えた場合について説明する。このような表面量子化補正によるしきい値変化は解析的に求めることができる。ここで、表面量子化補正は、表面ポテンシャルの表面バンド曲がりの増加量ΔΨ

$$\Delta\Psi_S=(E_0-E_C-\Delta E_g)/q+E_S\Delta z \qquad (6)$$

で表される。この式に$2\Phi_F$を加えたものをゲート電圧がしきい値である時の表面ポテンシャルΦ_{s1}とした。

【００５７】図５は、表面量子化補正を説明するためのバンド図である。

【００５８】式（６）は、図５に示したように伝導帯Ｅｃから最低エネルギー準位Ｅｏへのシフト$Eo-Ec$、高濃度のチャネル不純物添加によるバンドギャップの縮小（bandgap narrowing）効果ΔEg、そして量子論に

$$E_0-E_C=\frac{h^2}{2m}\left(\frac{9\pi m q E_S}{4h^2}\right)^{2/3} \qquad (7)$$

ここでＥｓは表面電界を表し、

【００６１】

$$E_S=\left(\frac{\Phi_{S1}-\Phi_{S2}}{t_{Si}}+\frac{qN_A t_{Si}}{2\varepsilon_{Si}}\right) \qquad (8)$$

と表される。

【００６２】また、高濃度のチャネル不純物添加によるbandgap narrowing効果ΔEgは、

$$\Delta E_g/q=\Delta V_{g0}(N_A)=9\left\{\ln\left(\frac{N_A}{10^{17}}\right)+\sqrt{\left[\ln\left(\frac{N_A}{10^{17}}\right)\right]^2+0.5}\right\}\ [mV] \qquad (9)$$

$Es\Delta z$の近似式は、

【００６４】

$$E_S\Delta z\approx max\left((1-(1/3)^{2/3})(E_0-E_C)-\frac{kT}{q},0\right) \qquad (10)$$

と表される。

【００６５】また、有効界面量子効果により、反転層電荷の中心がＳｉ膜とＳｉＯ2膜との界面からΔzだけ離れているから、ゲート酸化膜容量C_{OX1}は、$C_{OX1}=\varepsilon_{OX}/(t_{OX1}+\varepsilon_{Si}/\varepsilon_{OX}\Delta z)$と表される。

【００６６】以上説明したように量子補正を考慮して得られた、チャネル領域４のＳＯＩ膜厚に対するしきい値の依存性が図２である。図２からわかるように、バックゲート電圧を一定とし、チャネル領域４の膜厚を変化させた場合には、しきい値が極小値（図２中の矢印）を取る。そしてさらにチャネル領域４の膜厚が薄くなるとしきい値は増加する。これは、バックゲート電圧が一定の条件でチャネル領域４の膜厚が薄くなるとSiとSiO_2との界面の電界Ｅｓが大きくなるために、量子準位のエネルギーが大きくなり、表面が反転するのにより大きなゲート電圧が必要となるからである。

【００６７】このように、量子補正を考慮した計算を用いることによって、チャネル領域４の膜厚バラツキに対し、しきい値感度が極小となるチャネル領域４の膜厚が存在することが説明される。

【００６８】図６は、図２と同一のＦＥＴのモデルにおいて、図２でしきい値が極小となるチャネル領域４のＳＯＩ膜厚t_{Si}と印加するバックゲート電圧V_{G2}とを、チャネル領域４の不純物濃度N_Aに対して示したグラフである。ここでは、しきい値の設定値がそれぞれ０．１Ｖ、０．２Ｖ、０．３Ｖの場合について示した。

【００６９】図６からわかるように、しきい値が設定した値となり、かつ膜厚バラツキに対するしきい値感度が最小となるＳＯＩ膜厚t_{Si}は、チャネル領域４の不純物濃度N_Aに対する依存性が低いことが、本発明者の詳細な検討により新たに明らかとなった。つまり、ＳＯＩ膜厚t_{Si}の最適値は、不純物濃度N_Aに対してあまり変化せず、ほぼ一定の値をとる。

【００７０】また、設定するしきい値が異なると、ＳＯ

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Ｉ膜厚のバラツキに対するしきい値感度がほぼ最小となるＳＯＩ膜厚t_{Si}は異なることがわかった。ここで、t_{Si}の最適値としきい値V_{th}との関係は、$t_{Si}=250V_{th}^2-275V_{th}+105$（ｎｍ）で、$V_{th}$が０ボルト以上０．５ボルト以下は近似できる。よって、V_{th}が任意の値でも、t_{Si}の最適値を求めることができる。また、しきい値が設定した値となるために必要なバックゲート電圧V_{G2}は、チャネル領域４の不純物濃度N_Aに対して、ほぼ線形に増加することが新たに明らかになった。

【００７１】従って、設定したいしきい値に応じて図６にもとづいて決定したＳＯＩ膜厚t_{Si}、不純物濃度N_Aで作成した場合には、不純物濃度N_Aが例えばプロセスのバラツキ等で所望の値からずれたとしても、チャネル領域４の不純物濃度を測定し、それに応じて、しきい値が設定した大きさとなるのに必要なバックゲート電圧を印加することにより、ＳＯＩ膜厚に対するしきい値感度が最小で、且つ設定したしきい値を有する半導体装置を実現することができる。

【００７２】ここで、膜厚バラツキに対するしきい値感度がほぼ最小となるＳＯＩ膜厚が、チャネル領域４の不純物濃度N_Aに対してほぼ一定となるのは、式（６）の量子力学補正項がt_{Si}に強く依存し、N_Aにはあまり依存しないこと、および、式（５）の空乏層電荷のQ_{depl}が、N_Aが変化してもV_{G2}を変化させることによりほぼ補償することができることによる。

【００７３】この特徴により、もちろん、チャネル領域４の濃度分布が均一でなく所定の不純物プロファイルを有するような場合でも、式（２）で$Q_{depl}/2C_{OX1}$が$2\Phi_F$よりも小さい場合には、上記の不純物濃度N_Aに対してしきい値感度がほぼ一定となる特徴は維持される。

【００７４】また、図７に示したような、ＬＯＣＯＳ犠牲酸化などの方法により形成されたリセス（Recess）ゲート構造を有するＭＩＳＦＥＴの場合には、ＬＯＣＯＳ端部のバーズビークにより、チャネル領域４の膜厚が一定でない場合が多い。すなわち、チャネル領域の膜厚は、ソース・ドレイン寄りで厚く、中央付近で薄くなる。図８は、ＬＯＣＯＳ犠牲酸化法によるリセス型ゲート構造の製造工程を表す概略工程断面図である。例えば、厚さ２０ｎｍ～１μｍのシリコンなどのＳＯＩ層４の上に、厚さが５～１００ｎｍ程度のシリコン酸化膜１４を形成し、その上に例えば膜厚が５０～２００ｎｍのシリコン窒化膜からなる酸化防止膜２０を堆積する。次に、図８（ａ）に示したように、熱酸化法により、ＬＯＣＯＳを形成する。さらに、図８（ｂ）に示したように、酸化防止膜２０をマスクとしてＬＯＣＯＳ酸化膜をイオンエッチングし、ゲート形成領域を形成する。この方法によると、ゲート電極をセルフアラインに形成できるが、ＬＯＣＯＳのバーズビークがゲート形成領域に残るために、チャネル領域のＳＯＩ膜厚が図示したように不均一になりやすい。このようにチャネル領域の膜厚が不均一になると、しきい値の安定性が劣化して問題となる。

【００７５】これに対して、本発明によれば、チャネルの膜厚が均一でない場合にも、例えばチャネルの中央部のＳＯＩ膜厚で、所定のしきい値に対して膜厚ばらつきに対するしきい値感度が最小となるようなＳＯＩ膜厚を設定すれば、所望のしきい値を安定して得ることができる。従って、チャネル領域のＳＯＩ膜厚が、図２または図６に示したような最適膜厚となるように、チャネル中央付近と端部でのＳＯＩ膜厚の不均一性が例えば２０％以内に収まるように、ＬＯＣＯＳ酸化を行うと、所望のしきい値を得ることができる。

【００７６】ここで、チャネル領域４の不純物濃度N_Aの測定箇所は、必ずしもＭＩＳＦＥＴのチャネル領域４そのものである必要はなく、ＭＩＳＦＥＴのチャネル領域と同一の不純物濃度を有する領域であればよい。例えば、複数のＭＩＳＦＥＴを集積した集積素子を製造する際には、その集積素子のいずれかの箇所で測定しても良い。また、ウェーハ上に複数の集積素子を作成する場合に、ウェーハ内での不純物濃度の均一性が良好であれば、ウェーハのいずれかの箇所で測定しても良い。さらに、このようなウェーハを複数枚同時にプロセスする、いわゆる「バッチ処理」の製造プロセスにおいて、バッチ内のウェーハ毎の不純物濃度の変動が小さい場合には、バッチ毎にいずれかのウェーハで測定を行えば良い。

【００７７】このようにして、チャネル領域４の不純物濃度を測定し、設定するしきい値にするためのバックゲート電圧を決定すれば、このしきい値でトランジスタを用いる限りバックゲート電圧を変更する必要はない。つまり、バックゲート電圧が決まった後は、制御回路は必ずしも必要としない。そのため、チャネル領域４の不純物濃度測定を行い、本発明に必要なバックゲート電圧を求めれば、バックゲートに印加する可変電源を必要な電圧を出力するよう設定するだけでよい。

【００７８】ここで、チャネル領域４の不純物濃度の測定には、例えば、文献（“Materials Processing Theory and Practice volume.2-impurity doping processes in silicon”：F.F.Y.Wang著, North Holland Publishing Company(1981)）に紹介されているような測定手法を用いればよい。以下に、不純物濃度測定を含めた構成例を示す。

【００７９】図９は、本発明の半導体装置の第２の具体例を表す概略断面図である。なお、同図においては、図１と同一の部分には、同一符号を付し、その詳しい説明は省略する。

【００８０】図９において、４ａはダミー領域、１２は素子分離領域、１３は高濃度半導体領域、１８は電極領域、そして１９はメタルプラグを示している。ダミー領

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域４ａは、チャネル領域と同一の条件で作成された半導体領域である。高濃度半導体領域１３は、例えば、ｐ型のドーパントが固溶限界までドーピングされた半導体領域である。

【００８１】また、バックゲート１１は、支持基板２内に形成された導電性領域であり、例えば支持基板２をｐ型Ｓｉとし、バックゲート１１をｎ型Ｓｉとすることによって、それぞれ別の電圧が加えられるようにすることが望ましい。また、バックゲート１１は、しきい値を制御するＦＥＴの直下に形成し、不純物濃度を測定するダミー領域４ａの下には形成しない。これは、バックゲート１１に印加する電圧によってダミー領域４ａの空乏層厚さが変化するのを防ぐためである。

【００８２】以下に、チャネル領域４の不純物濃度と膜厚を測定する方法について説明する。図９において、回路９、９ａは制御回路で、回路９ａでは固溶限界で形成された高濃度半導体領域１３の抵抗を測定して、ＳＯＩ膜厚を求め、回路９へ出力する。回路９ではダミー領域４ａの両端の抵抗１８－４ａ－１８を測定し、回路９ａより入力されたＳＯＩ膜厚データを用いてチャネル領域４の不純物濃度を求める。このようにして求めた不純物濃度より、所望のしきい値を得るために必要なバックゲート電圧の値を求め、電源１０へ出力する。

【００８３】図９の構成例では、トランジスタＦＥＴ１のチャネル部分と同じ不純物添加を行ったダミー領域４ａに接するように半導体層と同じ導電性をもつ例えばp^+型の電極領域１８を形成している。そして制御回路９では、電極領域１８と１８との間の抵抗を測定する。ここで、抵抗率ρは、抵抗をＲ、電極領域１８の間隔をＬ、幅をＷ、そしてＳＯＩ膜厚をt_{Si}とすると、$\rho = W t_{Si} R / L$と表される。このようにして、抵抗率ρが得られれば、チャネル領域４の不純物濃度N_Aは、例えば、アービン曲線より求めることができる。

【００８４】一方、ＳＯＩ膜厚t_{Si}については、高濃度半導体領域１３から求めることができる。すなわち、図９に示したように、シリコン中にホウ素（Ｂ）などが固溶限界の濃度までドープされたp^+型の高濃度半導体領域１３において、この半導体領域１３の抵抗を求める。この高濃度半導体領域１３の抵抗から、抵抗率ρを求めることができ、さらに、不純物濃度は固溶度で定まる値となっているので、t_{Si}とN_Aとを分解することができる。よって、高濃度半導体領域１３における抵抗を測定することで半導体層の膜厚を求めることができる。

【００８５】以上の手法により得られたＳＯＩ膜厚t_{Si}を前述の式に代入することでチャネル領域４における不純物濃度N_Aを求めることができる。本構成例では、ＭＩＳＦＥＴ１を形成するのと同じプロセスでN_A測定領域を形成できる。

【００８６】ここで、回路９、回路１０の具体例としては、例えば、ｈａｌｆ－V_{dd}回路や基板バイアス回路などを挙げることができる。図１０は、ｈａｌｆ－V_{dd}回路を用いた実施例を表す概略回路図である。V_{B2}は例えば、０Ｖとなる電圧であり、V_{B1}は例えばV_{DD}となる電圧であり、$V_{B1} > V_{B2}$となっている。図１０の１８－４－１８の抵抗器は図９のダミー領域４ａにおいて形成された抵抗測定装置１８－４－１８であり、Ｒ１はダミー領域４ａが設定した不純物濃度で形成されたときの抵抗値と同じ抵抗値を有する抵抗器である。またトランジスタＱ３、Ｑ４はＱ１、Ｑ２よりも幅広く形成され、電流バッファとなっている。さらにＲ１および１８－４－１８のコンダクタンスはＱ１またはＱ２のトランスコンダクタンスよりも十分小さいとする。不純物濃度が変動したとき、１８－４－１８の抵抗が変化するため、抵抗分割によって、それにより出力される電圧も変化し、１８－４－１８抵抗が大きくなると出力は小さく、また１８－４－１８抵抗が小さくなるとノードＶｏの電圧は大きくなる。この出力ノードＶｏ は電圧と等しくなるように、バックゲート１１に接続されるノードの電圧Ｖ1 が定まる。よって抵抗測定装置の抵抗の変化によりバックゲート電圧を変化することができる。ここで、ＳＯＩ膜厚t_{Si}の変化の影響は、V_{B1}を変化させることによって取り除くことができる。

【００８７】また、図１１（ａ）（ｂ）は、基板バイアス回路による実施例を表す概略回路図である。すなわち、リング・オシレータ中に１８－４－１８抵抗器を設け、ダミー領域４ａの不純物濃度が変化すると、抵抗が変わるためにリング・オシレータの周波数が変化する。この周波数変化によって、チャージポンプ回路の励起回数が変化し、バックゲートへ供給される電流が変化し、バックゲート電圧を変化させることができる。

【００８８】次に、図９の半導体装置の製造工程について説明する。図１２～図１４は、図９の半導体装置の要部製造工程を表す工程断面図である。まず、図１２に示したように、バックゲート１１を形成する。具体的には、ＳＯＩウェーハ上にレジストマスク１５を形成し、チャネル領域４と絶縁膜３を介してシリコンなどの支持基板２にホウ素などの不純物をイオン注入する。このようにして、例えば$1 \times 10^{17} cm^{-3}$から$1 \times 10^{20} cm^{-3}$の不純物濃度からなるｐ型のバックゲート１１を形成することができる。

【００８９】ここで、チャネル領域４、ダミー領域４ａは、図１に関して前述したような方法により形成することができる。なお、ダミー領域４ａチャネル領域４における不純物濃度を測定するための領域である。従って、製造工程においてはチャネル領域４と同時に同じ条件で作成することが望ましい。

【００９０】次に、図１３に示したように素子分離領域１２を形成し、リソグラフィによりゲート長Ｌからなるゲート電極を６、６ａを形成する。さらに、ゲート電極の上に絶縁膜８、８ａを形成する。

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【００９１】次に、図１４に示したように、電極領域を形成する。具体的には、ＭＩＳＦＥＴを形成する領域をレジストマスク１５でマスキングし、例えばホウ素をゲート電極６の両脇にドーズ量10^{13}～10^{16}ｃｍ$^{-2}$でイオン注入することにより、ｐ型の電極領域１８を形成する。

【００９２】この電極領域１８を形成する工程は、ｐ型ＭＩＳＦＥＴのソース・ドレインを形成する時に同時に行うこともできる。つまり、ゲート電極の形成工程の後、例えばホウ素をイオン注入することによりゲート電極がマスクとなりｐ型の電極領域１８とソース・ドレイン領域７とを同時に形成することができる。

【００９３】さらに、電極領域１８を形成した領域とは異なる領域に、例えばホウ素を半導体層の固溶限までイオン注入した高濃度半導体領域１３を形成する（図１４）。この高濃度半導体領域１３は、先の電極領域１８やソース・ドレイン領域７を形成するイオン注入により同時に形成することができる。つまり、ゲートを形成しない領域を設け、ｐ型ＭＩＳＦＥＴのソース・ドレイン領域の形成ためのイオン注入を実施する時、例えばホウ素をシリコンの固溶限の不純物濃度まで注入することにより高濃度半導体領域１３も形成することができる。

【００９４】次に、図９に示したようにバックゲート１１へのコンタクト１９を形成する。具体的には、素子分離領域１２の上から、例えばイオンエッチングによりコンタクトホールを形成し、さらに例えばタングステン（Ｗ）などの電極材料を堆積することにより、メタルコンタクト１９を形成することができる。このメタルコンタクト１９を形成する工程は、図９に示した抵抗測定領域のメタルコンタクトや、ゲート・ソース・ドレイン電極への図示しないコンタクト形成と同時に行うこともできる。これらのコンタクトホール形成する際に、シリコン酸化膜とシリコンのエッチングの選択比の大きいガスを用いてイオンエッチングすることにより、コンタクトホールの深さの異なる領域も同時にエッチングすることができる。次に、ＳＯＩ膜厚t_{Si}を求めるための別の構成例について説明する。

【００９５】図１５は、本発明の半導体装置の第３の具体例を表す概略断面図である。同図の構成においては、ＭＩＳＦＥＴトランジスタ１とは別に、ダミー領域４ｂが形成され、そのダミー領域４ｂの上下にゲート電極６ｂとバックゲート１１ａとが設けられている。そして、これらの電極間のキャパシタンスの容量を測定する。ここでバックゲート１１ａは、バックゲートの表面半導体層に表面空乏化が生じないように充分、例えば10^{18}ｃｍ$^{-3}$以上に不純物添加することが望ましい。また、電極６ｂおよび電極１１ａは、ダミー領域４ｂが完全に空乏化し、その表面に反転層が生じないようにすることが望ましい。

【００９６】このような条件で測定したキャパシタンスC_{total}は、ゲート絶縁膜５、ダミー領域４ｂ、および絶縁膜３のキャパシタンスを直列したものと等しい。従って、ゲート絶縁膜５およびダミー領域４ｂ（すなわちチャネル領域４）の誘電率をそれぞれε_{OX}、ε_{Si}、ゲート絶縁膜５、ダミー領域４ｂ、絶縁膜３の膜厚をそれぞれ、t_{OX}、t_{Si}、t_{box}とすると、キャパシタンスは

【００９７】

【数１２】

$$C_{total}=\frac{1}{\frac{1}{\frac{\varepsilon_{Si}}{t_{Si}}}+\frac{1}{\frac{\varepsilon_{OX}}{t_{OX}}}+\frac{1}{\frac{\varepsilon_{OX}}{t_{box}}}}$$

であらわされる。よって、ゲート絶縁膜５の膜厚t_{OX}と絶縁膜３の膜厚t_{box}が求められ、ゲート絶縁膜５、および絶縁膜３のキャパシタンスが既知であればダミー領域４ｂ（すなわちチャネル領域４）の膜厚$t_{Si}=\varepsilon_{Si}/C_{total}-\varepsilon_{Si}(t_{OX}+t_{box})/\varepsilon_{OX}$を算出することができる。

【００９８】また、後に詳述する図１８に表した半導体装置の図中の左側に形成したダミー素子を用いてt_{Si}を求めることもできる。すなわち、図１８において、ｎ＋層１６とバックゲート１１ｂとの間の容量C_{total}を測定する。ここで、１０ｂの電圧源は、ゲート絶縁膜５ｂとＳＯＩ層４ａとの界面とに反転層が形成されるだけ十分に電圧が印加されているとする。また、バックゲートに十分な電圧を印加することにより、ダミー領域４ａのバックゲート側が空乏化するようにした条件では、測定容量C_{total}は、

【００９９】

【数１３】

$$C_{total}=\frac{\frac{\varepsilon_{Si}}{t_{Si}}\frac{\varepsilon_{OX}}{t_{box}}}{\frac{\varepsilon_{Si}}{t_{Si}}+\frac{\varepsilon_{OX}}{t_{box}}}$$

で表される。よって、t_{box}が既知であればt_{Si}を算出できる。この方法によれば、t_{ox}がばらついても正確にt_{Si}を算出することができる。

【０１００】また、抵抗率を求める方法としては、電圧電流端子を分離した４端子法を用いても良い。この方法の場合には、電極のコンタクト抵抗による誤差を低減できるという利点がある。

【０１０１】次に、図１５に示した半導体装置の製造方法について説明する。図１６、図１７は、図１５の半導体装置の要部製造工程を表す概略工程断面図である。ＭＩＳＦＥＴ、およびキャパシタンス容量を測定する領域の絶縁膜３を介して対抗する例えばシリコンからなる支持基板２の領域に、リソグラフィーと例えばホウ素をイオン注入することにより、例えば1×10^{18}ｃｍ$^{-3}$から1×10^{20}ｃｍ$^{-3}$の不純物濃度からなるｐ型バックゲート１１、１１ａを形成する（図１６）。ここで、チャネ

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ル領域４、ダミー領域４ｂは、図１に関して前述したような製造工程により形成することができる。

【０１０２】次に、図１７に示したように、素子分離領域１２を形成し、さらにゲート絶縁膜５とゲート電極６を形成する。引き続き、図１５に示したように電極領域１８と、ソース・ドレイン領域７を形成する。これらの製造方法は、図９に関して前述したものと同様とすることができる。ここで、図１５の具体例の場合は、ダミー領域４ｂの容量を測定するためにはゲート電極６ｂ下の半導体層が十分空乏化すればよい。従って、電極領域１８およびソース・ドレイン領域７を形成するイオン注入においても、ゲート電極６ｂがマスクの役割を果たすので、この領域をレジストなどでマスキングしなくとも良い。

【０１０３】次に、本発明の半導体装置の第４の具体例について説明する。図１８は、本発明の半導体装置の第４の具体例を表す概略断面図である。すなわち、同図に表した半導体装置においては、ＭＩＳＦＥＴ１とは別に設けられたＭＩＳキャパシタのダミー素子を用いてＣ－Ｖ測定法により不純物濃度を求めることができる。ＦＥＴ１と素子分離領域１２を介して隣接するダミー領域４ａの上に絶縁膜を５ｂが積層され、さらにＭＩＳキャパシタ電極として例えばp^+型ポリシリコン（多結晶シリコン）６ｂが積層されている。

【０１０４】また、このＭＩＳキャパシタの下部に作成したバックゲート１１にＭＩＳＦＥＴトランジスタに使う電圧源とは別の電圧源V_{G2}ｂを設ける。この電圧源V_{G2}ｂはダミー領域４ａの絶縁膜３に接する表面の電子状態が蓄積するだけの電圧が印加される固定電源でよい。

【０１０５】このようなＭＩＳキャパシタを用いてＣ－Ｖ法により半導体の不純物濃度を求め、本発明を実現するのに必要なバックゲート電圧を決定することができる。キャパシタンス測定は、ダミー領域４ａが完全に空乏化しない程度で固定のゲート電圧を印加し、そして、ゲート近傍に設けたn^+型、p^+型の半導体領域の電極を用いてキャパシタンス測定を行う。

【０１０６】この時の容量は、不純物濃度をN_Aとすると$(N_A)^{1/2}$に比例するため、容量からN_Aを求めることができる。

【０１０７】図１９は、回路９ｃ、１０ｂの具体例を表す概略回路図である。同図に表した回路は、例えば、図１１の回路と似ており、リング・オシレータにダミー素子のＭＩＳキャパシタによるキャパシタンスＣが組み込まれている。ダミー領域４ａの不純物濃度が変動するとキャパシタンスＣが変化し、リング・オシレータの周波数が変化する。この周波数の変化によって、バックゲート電圧を変化することができる。

【０１０８】次に、図１８の半導体装置の製造方法について説明する。図２０、図２１は、図１８の半導体装置の要部製造工程を表す概略工程断面図である。まず、図２０に示したように、ＭＩＳＦＥＴトランジスタを形成する領域に、例えば隣接する領域に、ＭＩＳＦＥＴトランジスタとは別のバックゲート１１ｂを形成する。次に、ゲート工程と同じ工程で、例えば、シリコン酸化膜からなるゲート絶縁膜５ｂおよび、ｎ型ポリシリコンからなるゲート電極６ｂを作成し、これがＭＩＳキャパシタを形成する。これは、ＭＩＳＦＥＴ１のゲート形成工程と同時に形成しても良い（図２０）。

【０１０９】次に、ＭＩＳキャパシタのゲート電極近傍にn^+型とp^+型の半導体領域を形成する。具体的には、ｎ型ＭＩＳＦＥＴ、ｐ型ＭＩＳＦＥＴのソース・ドレイン領域７の形成のためのイオン注入に際して、ＭＩＳキャパシタ領域にはそれぞれ片側ずつイオン注入すればよい（図２１）。

【０１１０】Ｃ－Ｖ法を用いた不純物濃度測定としては、ｐｎ接合により求める手法もある。図２２は、ｐｎ接合により不純物濃度を測定するためのダミー素子を設けた半導体装置を例示する概略断面図である。すなわち、ＦＥＴ１と素子分離領域１２を介して隣接するダミー領域４ａの表面層に、n^+型シリコン領域１４を形成する。このようにして形成したｐｎ接合を用いて、Ｃ－Ｖ法により不純物濃度を測定し、本発明を実現するのに必要なバックゲート電圧を決定することができる。ここで、ダミー領域４ａに絶縁膜３を介して対向するバックゲート１１ｃには、十分大きな負の電圧V_{G2a}を印加して、絶縁膜３に接した表面の電子状態を蓄積状態にする。

【０１１１】図２３は、図２２のダミー素子を含めた回路９ｄ、１０ｂの具体例を表す概略回路図である。図２３の回路における容量Ｃは図２２の電極６ｂで測定される容量である。図２２に示したようなダミー領域のｐｎ接合ダイオードのダイオードキャパシタンスは不純物濃度の変動によって変化する。このように容量Ｃが変化するとリング・オシレータの周波数が変化し、バックゲート電圧V_{G2}にフィードバックすることができる。ここで、容量Ｃが小さい場合にはポンプ周波数が上昇してV_{G2}が上昇する。もちろん、ｐｎ接合ではなく、例えばショットキー接合を用いていもよい。

【０１１２】次に、本発明の第５の具体例について説明する。図２４は、本発明の第５の具体例に係わる半導体装置の概略断面図である。本実施形態においては、同一基板上に、２つ以上の異なるしきい値を有する完全空乏化トランジスタを設け、それぞれのトランジスタのしきい値が、膜厚バラツキに対してしきい値感度が最小で、かつ設定したしきい値となるようにする。

【０１１３】なお、図２４に示した具体例では、説明の便宜上、チャネル領域４の膜厚や不純物濃度が異なる２つの完全空乏化トランジスタが並列している場合を示したが、絶縁体基板３上に形成されていればよく、必ずしも、同図に示した方向に隣接する必要はない。また、図

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２４において、図１と同一部分には、同一符号を付して、その詳しい説明は省略する。

【０１１４】本実施例は、同一基板上に少なくとも２つの異なるしきい値を有する完全空乏化トランジスタ１Ａ、１Ｂを備えている。具体的に説明すると、例えばシリコンからなる支持基板２上のシリコン酸化膜などの絶縁膜３の上に、２０ｎｍ～０．１μｍ程度の膜厚のＳＯＩ層、例えば、膜厚が８０ｎｍのチャネル領域４Ａと、６０ｎｍのチャネル領域４Ｂとが形成されている。それぞれの不純物濃度は、$1\times10^{16}cm^{-3}$～$1\times10^{19}cm^{-3}$程度の範囲にあり、例えば、それぞれ$1\times10^{17}cm^{-3}$と、$1.6\times10^{17}cm^{-3}$という異なる不純物濃度N_{AA}、N_{AB}を有する。ＭＩＳＦＥＴ１Ａ、１Ｂを形成するＳＯＩ層と絶縁膜３を介して対向する支持基板２には、それぞれのＭＩＳＦＥＴに異なる電位を与えられるバックゲート１１Ａ、１１Ｂが形成されている。また、チャネル領域４Ａ、４Ｂのそれぞれの不純物濃度に応じたバックゲート電圧を設定する制御回路９Ａ、９Ｂが設けられ、電極１１Ａ、１１Ｂに印加する可変電源１０Ａ、１０Ｂが設けられている。

【０１１５】ここで、図２に関して前述したモデルを用いて説明すると、図６に例示したように、ＳＯＩ膜厚のバラツキに対するしきい値感度がほぼ最小で、かつしきい値が設定した値になるチャネル領域４の最適領域すなわち設計値は、しきい値により一義的に決まる。つまり、設定するしきい値が異なると、しきい値のＳＯＩ膜厚バラツキ感度を最小とするための半導体層の最適膜厚は異なる。

【０１１６】図６に示した計算結果を用いると、同一基板上にしきい値が０．１Ｖと０．２Ｖの２つのしきい値変動が極小となる完全空乏化トランジスタを形成する時、チャネル領域４は例えば、それぞれ膜厚８０ｎｍ、６０ｎｍ、不純物濃度$1.0\times10^{17}cm^{-3}$、$1.6\times10^{17}cm^{-3}$で形成する必要があり、膜厚および不純物濃度を２つトランジスタで同じ値にすることはできない。すなわち、それぞれのトランジスタのＳＯＩ膜厚や不純物濃度を別々の値に設定することによって、ＳＯＩ膜厚のばらつきなどに対してしきい値が変動しにくいトランジスタを実現することができる。従来のようにＳＯＩ膜厚が同一では、それぞれのトランジスタのしきい値感度を低減することは困難である。

【０１１７】ＦＥＴ１Ａの設定しきい値がＦＥＴ１Ｂの設定しきい値よりも小さい場合には、それぞれのしきい値感度を極小にするために、同一基板上において、ＦＥＴ１ＡのＳＯＩ膜厚（t_{siA}）が厚く不純物濃度（N_{AA}）が低くチャネル領域４Ａと、ＳＯＩ膜厚（t_{siB}）が薄く不純物濃度（N_{AB}）が大きいチャネル領域４Ｂとを形成することが望ましい。

【０１１８】また、このようにチャネル領域の厚さや不純物濃度が異なる複数の領域に対応して、それぞれの領域に独立に電位を設定することができるバックゲート電極および図示しないダミー素子を設けることが望ましい。すなわち、これらのダミー素子を用いてそれぞれのチャネル領域の不純物濃度や層厚を測定し、その測定結果をフィードバックして、それぞれのＦＥＴに所定のバックゲート電圧を印加することにより、それぞれのＦＥＴのしきい値を所望の値に調節することができる。このためのダミー素子は、例えば、図９、図１５、図１８、或いは図２２などに例示したものを用いることができる。さらに、測定のための回路やバックゲート電圧の印加回路も、本願明細書において例示した種々のものを用いることができる。

【０１１９】さらに、ｎ型ＭＩＳＦＥＴとｐ型ＭＩＳＦＥＴを同一基板上に形成する場合にも、本実施例を用いることができる。つまり、図２４に示したＦＥＴ１Ａとして、例えば、ｎ型ＭＩＳＦＥＴを用い、ＦＥＴ１Ｂとして、例えばｐ型ＭＩＳＦＥＴを用いればよい。通常、ゲート電極と基板との仕事関数の差やゲート絶縁膜界面の電荷は、ｎ型ＭＩＳＦＥＴとｐ型ＭＩＳＦＥＴで異なるため、そのフラットバンド電圧の絶対値$|V_{FB}|$も異なる。このため、たとえ同じしきい値を設定しても、ｎ型ＭＩＳＦＥＴとｐ型ＭＩＳＦＥＴのそれぞれに対し、ＳＯＩ膜厚変動に対するしきい値感度を最小にするためのＳＯＩ膜厚も異なる。すなわち、図２４に例示したように、それぞれのトランジスタＦＥＴ１ＡおよびＦＥＴ１Ｂで最適なＳＯＩ膜厚を用いることで、しきい値感度を小さく保つことができる。

【０１２０】次に、図２４の半導体装置の製造方法について説明する。図２５は、図２４の半導体装置の要部製造工程を表す概略工程断面図である。本構造の形成に際しては、図２５（ａ）に示したように、ＳＯＩ基板に対して、リソグラフィとイオン注入によって、バックゲート１１Ａ、１１Ｂを、それぞれのＭＩＳＦＥＴに対し別の電位を与えられるように形成する。絶縁膜３の上のＳＯＩ層をポリッシングやドライエッチング、あるいはウエットエッチングにより薄膜化し、例えば８０ｎｍの膜厚で、またホウ素（Ｂ）などをイオン注入することにより、例えば$1\times10^{17}cm^{-3}$の不純物濃度のＳＯＩ層４を形成する。次に、レジストマスク１５を形成して、エッチングすることにより、例えば、６０ｎｍの膜厚からなるチャネル領域４Ｂを形成する。引き続き、チャネル領域４Ｂに、例えばホウ素（Ｂ）をイオン注入して、この領域の不純物濃度N_{AB}を例えば、$1.6\times10^{17}cm^{-3}$とする。

【０１２１】そして、図示しないゲート工程以降の工程を行うことにより、同一の基板上に完全空乏化トランジスタＦＥＴ１Ａ、ＦＥＴ１Ｂを形成することができる。また、それぞれのチャネル領域に対応して、図示しないダミー素子を適宜形成する。さらに、ＭＩＳＦＥＴを形成するＳＯＩ層の不純物濃度に応じてバックゲート電圧

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を制御する回路９Ａ、９Ｂを設け、各々バックゲート１１Ａ、１１Ｂに印加する可変電源１０Ａ、１０Ｂなどを設置して半導体装置が完成する。

【０１２２】次に、本発明の第６の具体例について説明する。

【０１２３】図２６は、本発明の第６の具体例に係わる半導体装置の概略断面図である。本具体例においては、薄いＳＯＩ層にＦＥＴ１を形成し、厚いＳＯＩ層に不純物濃度を測定するためのダミー素子を形成することを特徴とする。

【０１２４】このダミー素子はｐｎ接合を有し、Ｃ－Ｖ法を用いて不純物濃度を測定できるものであり、その構造及び測定の方法の詳細は、図２２に関して前述したものと同様とすることができる。膜厚の薄いＳＯＩ層にｐｎ接合を形成する際には、その接合位置の制御は容易でなく、イオン注入するりん（Ｐ）や砒素（Ａｓ）の突き抜けなどによってｐ型層が失われるおそれがあり、また、ｐ型層の空乏層がバックゲート領域まで延びN_Aを測定できなくなるおそれがある。これに対して、本具体例によれば、ＳＯＩ層の膜厚を厚くした領域でｐｎ接合を形成することができるので、その形成がはるかに容易となり、ｐ型層の領域が確保できるなどの利点がある。

【０１２５】その製造工程について概説すると以下の如くである。まず、例えば膜厚が８０ｎｍで不純物濃度が$1\times10^{17}cm^{-3}$のｐ型シリコン層からなるＳＯＩ層を形成する。次に、パターニングとエッチングにより、トランジスタを形成する部分のＳＯＩ層の膜厚を例えば６０ｎｍとする。次に、これらのＳＯＩ層の不純物濃度が例えば、$1.6\times10^{17}cm^{-3}$となるようにホウ素（Ｂ）などをイオン注入する。さらに、ＭＩＳＦＥＴを形成する領域に、ゲート工程以降の工程を行う。

【０１２６】次に、図２７に示したように、ダミー素子を形成する領域に例えばリン（Ｐ）をイオン注入することによりｐｎ接合を形成する。このイオン注入工程は、ｎ型ＭＩＳＦＥＴのソース・ドレイン領域７の形成工程と兼ねることも可能である。ここで、図２４や図２６に例示したように膜厚が異なるＳＯＩ領域を方法としは、ＬＯＣＯＳ（Local Oxidation of Silicon）犠牲酸化によることもできる。図２８は、ＬＯＣＯＳ犠牲酸化によるリセス（Recess）構造を用いることにより膜厚の薄いＳＯＩ領域を形成する技術を説明する工程断面図である。この方法においては、まず、ＳＯＩ層４ａの上にシリコン酸化膜１４を形成し、その全面に例えば、シリコン窒化膜からなる膜２０を堆積する。そして、図２８（ａ）に示したように、薄膜化したいチャネル領域においてシリコン窒化膜２０を開口する。そして、開口した領域のＳＯＩ層にイオン注入し、熱処理を施すことにより所定の不純物濃度とする。

【０１２７】次に、図２８（ｂ）に示したように、開口した領域のＳＯＩ層の膜厚が所定の厚さに低下するまで、表面層を熱酸化する。そして、シリコン窒化膜２０、シリコン酸化膜１４を剥離することにより、膜厚が薄く、所定の不純物濃度を有するＳＯＩ領域を形成することができる。この後は、図示しないゲート形成工程以降の工程を実施することにより、半導体装置を完成することができる。

【０１２８】ここでは、ＳＯＩ層のチャネル部の薄膜化についてＬＯＣＯＳ犠牲酸化によるリセス構造について説明した。しかし、この他にも、図２９に示すように、チャネル領域のＳＯＩ層をリソグラフィとエッチングにより薄膜化するコーンケーブ（concave）構造により形成してもよい。

【０１２９】次に、本発明の第７の具体例について説明する。前述した各具体例では、所望のしきい値を有し且つプロセスのばらつきによるしきい値の変動を低減するために、完全空乏化トランジスタを形成する基板と同一基板上に、不純物濃度またはキャリア濃度を測定する測定用ダミー素子と、測定用ダミー素子により測定した不純物濃度またはキャリア濃度に応じてバックゲート電圧を設定する制御回路を設ける技術について説明した。これに対して、本具体例では、あらかじめ測定用ダミー素子で不純物濃度またはキャリア濃度を測定し、その値を記憶させた記憶素子を設けた半導体装置を実現する。

【０１３０】図３０は、本具体例に係わる半導体装置の要部断面図である。また、図３１は、本具体例における各構成要素の関連を説明する機能ブロック図である。同図においては、前述した各具体例と同一部分には同一記号を付して、その詳細な説明は省略する。本具体例においても、所望のしきい値に対し、しきい値感度が低減されるように設定されたＳＯＩ膜厚と、不純物濃度またはキャリア濃度（例えば、図６）を有するチャネル領域４とバックゲート１１からなる完全空乏化トランジスタＦＥＴ１が設けられている。さらに、本具体例においては、バックゲート１１に印加するバックゲート電圧を設定するための、不純物濃度またはキャリア濃度の情報を記憶する記憶素子を有する。この記憶素子は、例えば、ポリシリコンやアモルファスシリコンやアルミニウム（Ａｌ）や銅（Ｃｕ）、あるいは白金シリサイド（ＰｔＳｉ）やチタンシリサイド（ＴｉＳｉ）などからなる配線層で形成されたヒューズＦ１、Ｆ２、Ｆ３を有することを特徴とする。

【０１３１】図３２～３４は、図３０の半導体装置の製造工程を説明するための断面図である。すなわち、本具体例においても、図３２に示したように、製造工程の途中では測定用ダミー素子を設ける。このダミー素子は、図９に示したように、ＳＯＩ層の抵抗率ρから不純物濃度またはキャリア濃度を測定するものである。

【０１３２】次に、図３３に示したように、測定用ダミー素子を用いて、チャネル領域４の不純物濃度またはキャリア濃度を測定する。そして、この測定値に基づい

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て、所望のしきい値に要するバックゲート電圧を決定し、記憶素子に記憶する。すなわち、ヒューズを切断して、必要なバックゲート電圧を作成する。ここで、測定用ダミー素子はＦＥＴ１のそれぞれについて形成されている必要は必ずしもない。例えば、共通するしきい値を有する複数のＦＥＴについて１つの測定用ダミー素子を形成することにより、素子面積を減らすことができる。さらに具体的には、複数のＦＥＴが形成された集積回路を有する半導体装置について１つの測定用ダミー素子を設けても良く、または、このような半導体装置が複数個形成されるウェーハについて１つの測定用ダミー素子を設けても良い。さらに、これらのウェーハが複数枚バッチ処理される場合に、ウェーハ間のばらつきが小さければ、いずれかのウェーハのみに測定用ダミー素子を設けても良い。

【０１３３】一旦、チャネル領域４の不純物濃度またはキャリア濃度が測定され、図６に示したような関係に基づいて必要なバックゲート電圧が決定されると、測定用ダミー素子は不要となる。そこで、図３４に示すように、チップ化するための例えば、ダイシング工程において、ＦＥＴ１と測定用ダミー素子とを分離することができる。

【０１３４】本具体例によれば、不純物濃度またはキャリア濃度を測定するための回路を最終的に得られるチップ上に形成する必要がなく、はるかに小さなサイズの記憶素子に記憶させればよい。よって、高集積化およびチップ面積の縮小を図ることができる。また、不純物濃度またはキャリア濃度測定回路が不要となるために、より低消費電力化を図ることもできる。

【０１３５】ここで、チャネル領域の不純物濃度またはキャリア濃度の測定は、図３２に示した測定用ダミー素子に限らず、前述した各具体例にて説明したいずれの手法も同様に用いることができる。

【０１３６】また、本具体例は、図２４に例示したような複数の異なるＦＥＴが形成されてなる半導体装置についても適用することができる。すなわち、チャネル領域の層厚や不純物濃度などが異なる複数の種類のＭＩＳＦＥＴが形成されている場合に、それぞれの種類のＦＥＴ毎に記憶素子を設けることにより、ダミー素子の測定結果をフィードバックして最適なバックゲート電圧を印加することができる。

【０１３７】次に、本具体例で使用するバイアス回路の具体的な構成を例示する。

【０１３８】図３５～図４０は、本具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。

【０１３９】図３５は、チャネル領域４の不純物濃度またはキャリア濃度のばらつく範囲をあらかじめ予測し、それぞれの予測値に対応した最適なバックゲート電圧を、例えばV_{G1}、V_{G2}、V_{G3}、と設けておいて、必要に応じて記憶素子のヒューズを切断する例である。

【０１４０】図６のＳＯＩ膜厚と不純物濃度との関係のグラフを用いて具体的に説明する。まず、所望のしきい値を０．２Ｖとし、不純物濃度が例えば、１．２×10^{17}ｃｍ$^{-3}$～１．８×10^{17}ｃｍ$^{-3}$までの範囲内でばらつくとする。この時、バックゲート電圧の供給電源として例えば、V_{G1}、V_{G2}、V_{G3}として－１、０、１Ｖを設けておく。次に、ダミー素子を用いてチャネル領域４の不純物濃度の測定を行い、その測定値が１．２×10^{17}ｃｍ$^{-3}$～１．４×10^{17}ｃｍ$^{-3}$の時は、記憶素子のＦ１を非切断とし、Ｆ２とＦ３を切断することによりバックゲート電圧としてV_{G1}＝－１Ｖを印加する。また、測定値が１．４×10^{17}ｃｍ$^{-3}$～１．６×10^{17}ｃｍ$^{-3}$の時は、Ｆ２を非切断とし、Ｆ１とＦ３を切断することによりバックゲート電圧としてV_{G2}＝０Ｖを印加する。さらに、測定値が１．６×10^{17}ｃｍ$^{-3}$～１．８×10^{17}ｃｍ$^{-3}$の時は、Ｆ３を非切断とし、Ｆ１とＦ２を切断することによりバックゲート電圧としてV_{G3}＝１Ｖを印加するようにヒューズを各々切断する。このようにすれば、測定値に基づいて、所望の範囲内のバックゲート電圧を印加することが可能となり、所望のしきい値に近いしきい値を得ることができる。

【０１４１】図３６は、図３５の電源V_{G1}～V_{G3}を、昇降圧回路に置き換えた例である。このようにすれば、従来から用いられている電源電圧を基にして適宜、所定のバックゲート電圧に昇圧または降圧することができる点で便利である。

【０１４２】図３７は、例えば、電源電圧であるＶcc＝３ＶからＶss＝０Ｖまでの、Ｖcc～Ｖssの電圧範囲内で適宜分圧して、バックゲート電圧として用いる例である。例えば抵抗Ｒからなる抵抗器を直列に接続し、それぞれの端子にて電圧が抽出できるようにヒューズを配線する。そして、バックゲート電圧印加の際には、例えばヒューズＦ２を非切断、Ｆ１、Ｆ３を切断することで２／３Ｖcc、またＦ３を非切断、Ｆ１、Ｆ２を切断することで１／３Ｖcc、そして例えば全てのヒューズを非切断することでＶccの電圧をバックゲートに印加することができる。図３７では抵抗器を３つ設けたが、複数個であればよく、より多くの抵抗器を設ければ、より細かく分圧されることになり、所望のしきい値に近い値を得ることができる。また電圧の範囲は、Ｖcc～Ｖssの範囲に限らず、昇降圧回路を用いることで範囲を変えることも可能である。

【０１４３】図３８は、図３７の変形例であり、２つの抵抗器と１つのヒューズとからなるセルをｎ個用いることで、例えばＶcc～Ｖssまでの電圧の範囲を分割することができる回路例である。

【０１４４】また、図３７のように、抵抗器の出力を直接基板バイアスノードに加える他に、図３９に示したように、制御入力によって出力電圧が変化する可変電源に

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抵抗器出力を接続してもよい。このようにすることにより、抵抗器に流す電流を小さくしても大きな基板バイアス出力電流が得られるという利点がある。

【０１４５】さらに図４０のように、複数のチャージポンプ回路を縦続接続し、基板バイアス電圧を記憶素子のヒューズＦ１～Ｆ３の状態によって切り替えるようにしても良い。ここでトランジスタのしきい値をV_tとすると、Ｆ１、Ｆ２、Ｆ３が非切断の時、基板バイアス電源出力の開放電圧は$-3Vcc+4V_t$、Ｆ１、Ｆ２非切断、Ｆ３切断の時、$-2Vcc+4V_t$、Ｆ１非切断、Ｆ２、Ｆ３切断の時$-Vcc+4V_t$の出力を得ることができる。

【０１４６】本具体例において用いる記憶素子としては、上述したようなヒューズを切断する方法の他にも、例えば、浮遊ゲート電極に電荷を蓄積する方法や、強誘電体を分極させて記憶させる方法、さらには、金属またはシリサイドにはさまれた薄い半導体または絶縁体の絶縁破壊によって記憶させる方法、いわゆるアンチヒューズを用いてもよい。

【０１４７】以上、具体例を例示しつつ本発明の実施の形態について説明した。しかし、本発明は、上述した各具体例に限定されるものではない。

【０１４８】例えば、絶縁膜の形成法としては、熱酸化による酸化膜形成法や、３０ｋｅＶ程度の低加速エネルギーで酸素を注入した酸化膜を形成する方法としてもよいし、シリコン酸化膜を堆積する方法や、シリコン窒化膜を堆積する方法、またはこれらを組み合わせた方法でもよい。また、シリコンをシリコン酸化膜やシリコン窒化膜に変換するこれら以外の方法、例えば酸素イオンを堆積したシリコンに注入する方法や、堆積したシリコンを酸化する方法を用いてもかまわない。また、これらの絶縁膜に、シリコン窒化膜その他タンタル酸化膜、チタン酸化膜、チタン酸ストロンチウムやチタン酸バリウム、チタン酸ジルコニウム鉛などの強誘電体膜、常誘電体膜の単層膜またはそれらの複合膜を用いることもできる。

【０１４９】また、上述した具体例においては特に言及していないが、素子分離としては、トレンチ分離の素子分離や、ＬＯＣＯＳ素子分離膜や、リセス型（Recessed）ＬＯＣＯＳや改良ＬＯＣＯＳ法やフィールドシールド分離を用いても良いし、これらを組み合わせてもよい。

【０１５０】さらに、上述した各具体例では、ＳＯＩ層としてｐ型Ｓｉを用いたが、代わりにｎ型ＳｉやＧａＡｓ、ＩｎＰを用いても良い。また、ｎ型ＭＩＳＦＥＴではなくｐ型ＭＩＳＦＥＴに適用してもよく、その場合、上述の実施例のｎ型をｐ型、ｐ型をｎ型と読み替え、さらに、ドーピング不純物種のＡｓ、Ｐ、Ｓｂなどを Ｉｎ、Ｂなどのいずれかと読み替え、イオン注入の場合にもＡｓ、Ｐ、ＳｂをＩｎ、Ｂ、ＢＦ2 のいずれかと読み替えればよい。

【０１５１】さらに、ゲート電極は、多結晶シリコン以外の単結晶シリコン、ポーラス（多孔質）シリコン、アモルファスシリコン、ＳｉＧｅ混晶、ＳｉＣ混晶、ＧａＡｓ、Ｗ、Ｔａ、Ｔｉ、Ｈｆ、Ｃｏ、Ｐｔ、Ｐｄの金属あるいはシリサイドを用いることもできる。さらに、これらの積層構造としても良い。

【０１５２】その他、本発明の趣旨を逸脱しない範囲で種々に変形して実施することができる。

【０１５３】

【発明の効果】本発明は、以上説明した形態で実施され、以下に説明する効果を奏する。

【０１５４】まず、本発明によれば、完全空乏化トランジスタで問題となるＳＯＩ膜厚や不純物濃度のバラツキに対するしきい値感度をほぼ最小に保ったままで、かつしきい値を所望の値にすることが可能である。

【０１５５】また、本発明によれば、例えば集積回路を形成した場合に、不純物濃度のばらつきを補正し、従来例よりもＳＯＩ膜厚ばらつきに対するしきい値感度が小さいので、より、特性が均一な素子を集積できる。

【０１５６】一方、ＭＯＳ論理回路では、トランジスタのしきい値が高くなると、電流駆動能力が落ち遅延時間が長くなる一方、しきい値が低くなると、ｏｆｆ時のサブスレッショルドリーク電流が大きくなる。よって、本発明によれば、より遅延時間や消費電力のばらつきを小さく保つことができる。

【０１５７】また、遅延時間はしきい値V_{th}に対し、電源電圧をV_{DD}として（$V_{DD}-V_{th}$）$-\alpha$（αは１以上の正の数）に比例する。よって、遅延時間をV_{th}のばらつき分だけ低下させることができ、より遅延時間が同じでも低電圧動作させることができる。よって、低電圧動作させることによって、より例えばゲート絶縁膜の電源電圧に対する信頼性を向上させ、ゲート充放電の消費電力を小さくすることができる。

【０１５８】また、本発明によれば、ＬＯＣＯＳ犠牲酸化によるリセスゲート構造を形成した場合においても、所望のしきい値でＳＯＩ膜厚のばらつきに対してしきい値感度が最小となるようなＳＯＩ膜厚を設定することにより、このＳＯＩ膜厚付近でのしきい値の変動が最小化されるため、所望のしきい値を得ることができる。

【０１５９】また、ペアトランジスタ間のしきい値のばらつきをより抑えられるので、例えばカレントミラー回路や交差結合型センスアンプをより精度よく対称に実現することができ、より電流源の精度やセンスアンプの感度を増大することができる。さらに、本発明によれば、２つ以上のしきい値を持つＭＩＳＦＥＴを集積した半導体回路に対し、ＳＯＩ膜厚ばらつきに対するしきい値感度をそれぞれの素子に対して極小とすることができる。これはＣＭＯＳ回路においても、ｎ型ＭＩＳＦＥＴ、ｐ型ＭＩＳＦＥＴの所望のしきい値に応じたＳＯＩ膜厚で

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形成された完全空乏化ＭＩＳＦＥＴでは、それぞれのＭＩＳＦＥＴにおいて、ＳＯＩ膜厚バラツキに起因するしきい値感度は最小になる。これは従来の単一なＳＯＩ膜厚を有するＦＤ－ＳＯＩＭＩＳＦＥＴでは困難である。よって、複数のしきい値を有するトランジスタやＣＭＯＳ回路を用いた論理回路において、ＳＯＩ膜厚がばらついても、各々所望のしきい値で、しきい値感度をほぼ最小に保つことができる。また、本発明によれば、不純物濃度に応じたバックゲート電圧制御回路はｈａｌｆ－V_{dd}回路や、基板バイアス回路を応用することにより、同一基板上に形成することも可能である。

【０１６０】また、本発明においてＭＩＳＦＥＴを形成する半導体層の不純物濃度を抵抗を測定することから求める手法は、キャパシタンスの容量を測定する手法により低電圧で行うことができ、そしてゲート酸化膜耐圧による印加電圧の限界に問題はないという利点を有する。一方、キャパシタンスの容量測定より不純物濃度を求める手法では、抵抗測定による手法より感度が高く、消費電力を小さくすることが可能であるという利点を有する。

【０１６１】さらに、本発明のダミー素子の製造に際しては、ＭＩＳＦＥＴに用いるゲートをそのまま用いることもできるため、従来の半導体装置の工程数で同一基板上に不純物濃度測定のためのダミー素子を形成することができる。

【０１６２】また、本発明によれば、薄いＳＯＩ膜厚からなる半導体層の不純物濃度測定のためのダミー素子を、厚いＳＯＩ膜厚からなる半導体層領域に形成することにより、ダミー素子のｐｎ接合形成のための膜厚マージンを確保することができる。そして、例えば、ｐ型半導体層にイオン注入によりｎ型層を形成しｐｎ接合領域を形成するとき、ｎ型ＭＩＳＦＥＴにおけるソース・ドレイン電極領域形成のイオン注入と同時に行うことで、リソグラフィー工程を現状のままで、ｐｎ接合領域を形成することが可能である。

【０１６３】以上説明したように、本発明によれば、完全空乏化トランジスタを有する半導体装置において、ＳＯＩ膜厚や不純物濃度のばらつきに対するしきい値感度をほぼ最小に保ったままで、しきい値を所望する値にすることができ、産業上のメリットは多大である。

【図面の簡単な説明】

【図１】本発明の第１の具体例に係わる半導体装置を表す要部断面図である。

【図２】本発明者の計算により得られた完全空乏化ＦＥＴのＳＯＩ層としきい値との関係を表すグラフ図である。

【図３】式（２）～（５）により、チャネル領域４の不純物濃度N_A＝１×10^{17}ｃm^{-3}、ＳＯＩ膜厚t_{si}＝６０ｎｍ、Φ_{Ms1}＝－１Ｖ、Q_{0X1}＝Q_{0X2}＝０の場合について計算したバックゲート電圧に対するしきい値の関係を表したグラフである。

【図４】チャネル領域４の不純物濃度を１×10^{17}ｃm^{-3}としたときの、式（２）～（５）の古典論モデルを用いて計算したしきい値のチャネル領域４のＳＯＩ膜厚の依存性を示したグラフである。

【図５】表面量子化補正を説明するためのバンド図である。

【図６】図２と同一のＦＥＴのモデルにおいて、図２でしきい値が極小となるチャネル領域４のＳＯＩ膜厚t_{Si}と印加するバックゲート電圧V_{GZ}とを、チャネル領域４の不純物濃度N_Aに対して示したグラフである。

【図７】ＬＯＣＯＳ犠牲酸化などの方法により形成されたリセス（Recess）ゲート構造を有するＭＩＳＦＥＴを表す断面図である。

【図８】ＬＯＣＯＳ犠牲酸化法によるリセス型ゲート構造の製造工程を表す概略工程断面図である。

【図９】本発明の半導体装置の第２の具体例を表す概略断面図である。

【図１０】ｈａｌｆ－V_{dd}回路を用いた実施例を表す概略回路図である。

【図１１】基板バイアス回路による実施例を表す概略回路図である。

【図１２】図９の半導体装置の要部製造工程を表す工程断面図である。

【図１３】図９の半導体装置の要部製造工程を表す工程断面図である。

【図１４】図９の半導体装置の要部製造工程を表す工程断面図である。

【図１５】本発明の半導体装置の第３の具体例を表す概略断面図である。

【図１６】図１５の半導体装置の要部製造工程を表す概略工程断面図である。

【図１７】図１５の半導体装置の要部製造工程を表す概略工程断面図である。

【図１８】本発明の半導体装置の第４の具体例を表す概略断面図である。

【図１９】回路９ｃ、１０ｂの具体例を表す概略回路図である。

【図２０】図１８の半導体装置の要部製造工程を表す概略工程断面図である。

【図２１】図１８の半導体装置の要部製造工程を表す概略工程断面図である。

【図２２】ｐｎ接合により不純物濃度を測定するためのダミー素子を設けた半導体装置を例示する概略断面図である。

【図２３】図２２のダミー素子を含めた回路９ｄ、１０ｂの具体例を表す概略回路図である。

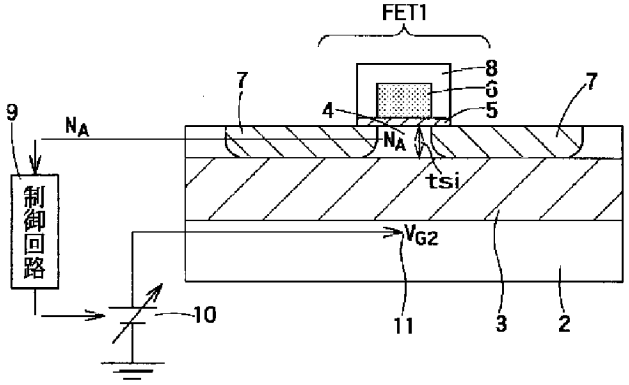
【図２４】本発明の第５の具体例に係わる半導体装置の概略断面図である。

【図２５】図２４の半導体装置の要部製造工程を表す概

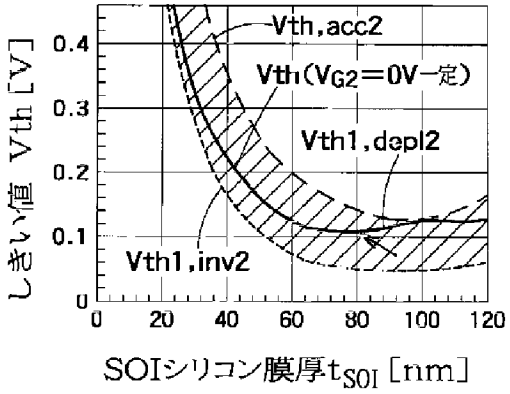
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略工程断面図である。
【図２６】本発明の第６の具体例に係わる半導体装置の概略断面図である。
【図２７】リン（Ｐ）をイオン注入する工程を表す概略断面図である。
【図２８】ＬＯＣＯＳ犠牲酸化によるリセス（Recess）構造を用いることにより膜厚の薄いＳＯＩ領域を形成する技術を説明する工程断面図である。
【図２９】コーンケーブ（concave）構造を表す概略断面図である。
【図３０】第７具体例に係わる半導体装置の要部断面図である。
【図３１】第７具体例における各構成要素の関連を説明する機能ブロック図である。
【図３２】図３０の半導体装置の製造工程を説明するための断面図である。
【図３３】図３０の半導体装置の製造工程を説明するための断面図である。
【図３４】図３０の半導体装置の製造工程を説明するための断面図である。
【図３５】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図３６】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図３７】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図３８】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図３９】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【図４０】第７具体例で用いることができる記憶素子を含んだバイアス回路の構成例を表す。
【符号の説明】
１　完全空乏化トランジスタ
２　導電性支持基板
３　絶縁膜
４　チャネル領域
５　ゲート絶縁膜
６　ゲート電極
７　ソース・ドレイン電極
８，１４　絶縁膜
９　制御回路
１０　可変電源（電圧制御電圧源）
１１　バックゲート
１２　素子分離領域
１３　半導体層領域
１５　レジスト
１８　電極
１９　メタルプラグ
Ｆ１～Ｆ３　ヒューズ

【図１】

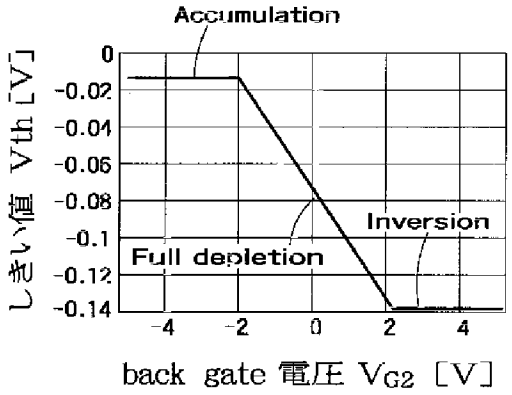


【図２】

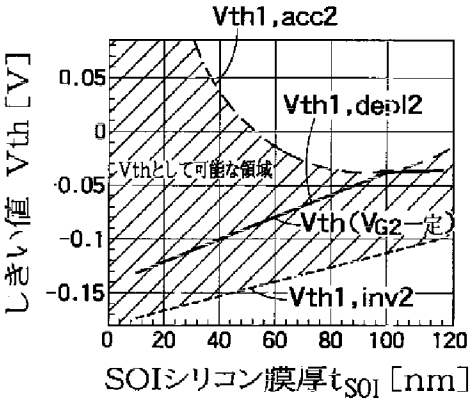


GF Exhibit 1126 - 1504/2248

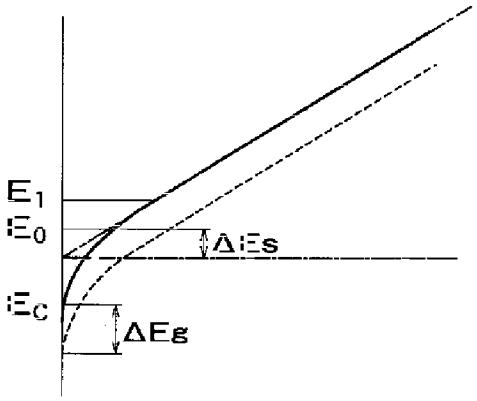
【図3】



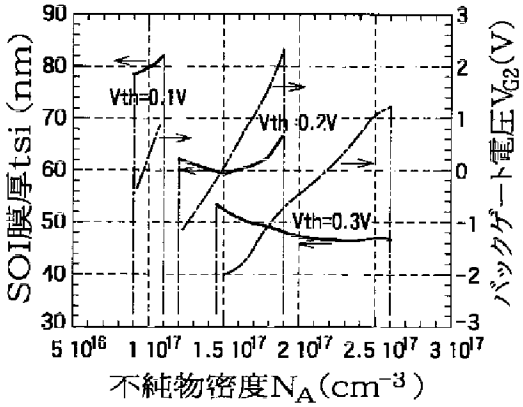
【図4】



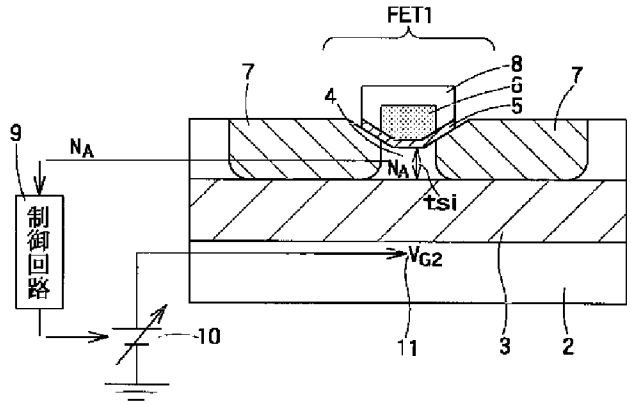
【図5】



【図6】

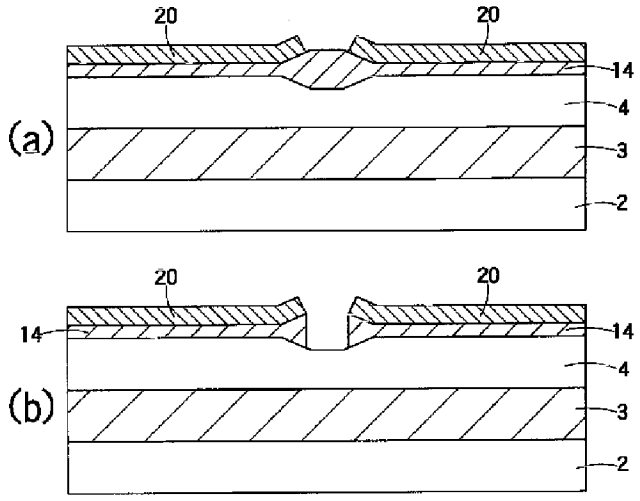


【図7】

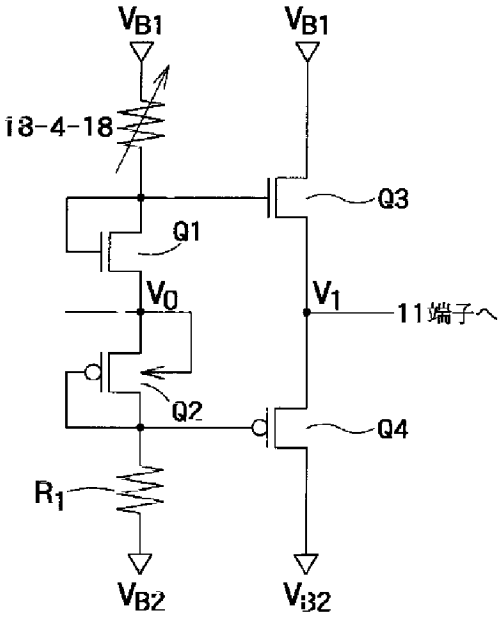


GF Exhibit 1126 - 1505/2248

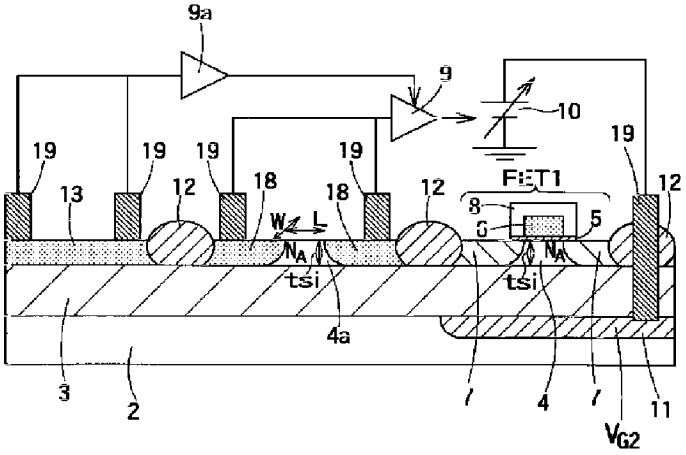
【図8】



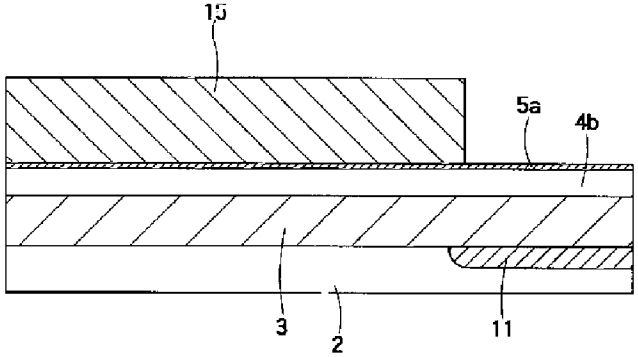
【図10】



【図9】

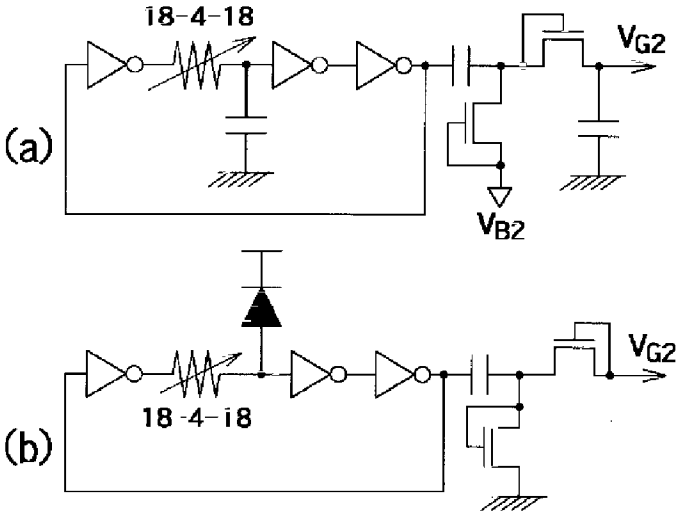


【図12】

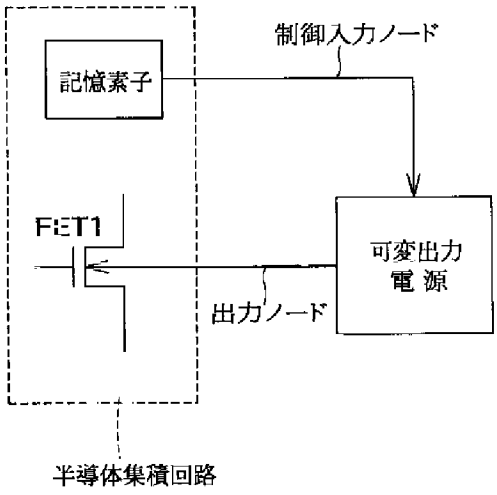


GF Exhibit 1126 - 1506/2248

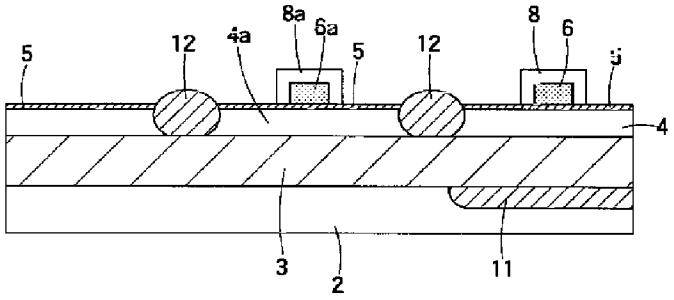
【図１１】



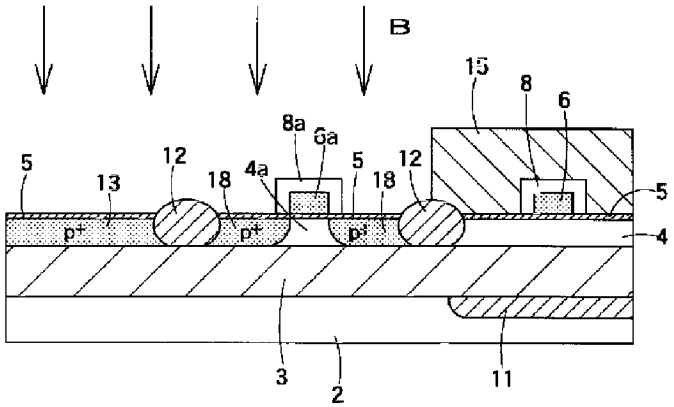
【図３１】



【図１３】

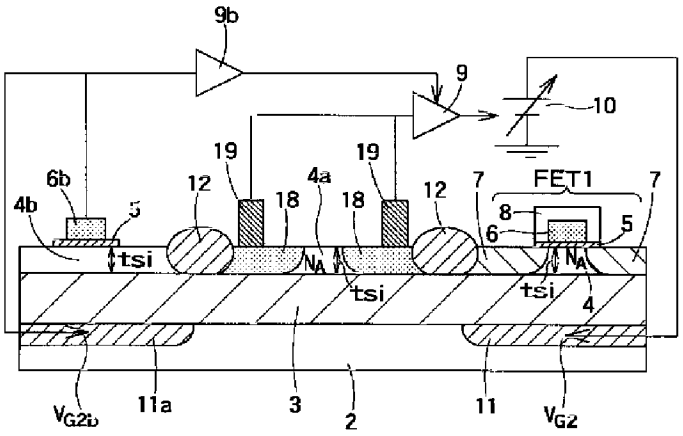


【図１４】

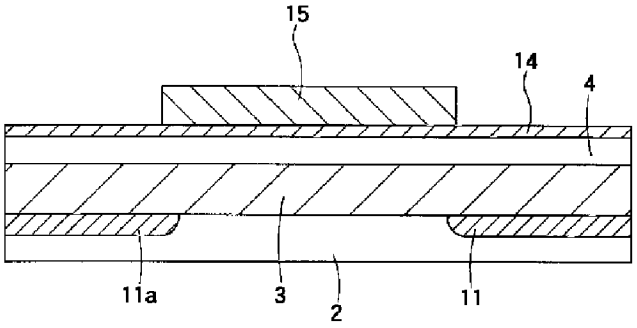


GF Exhibit 1126 - 1507/2248

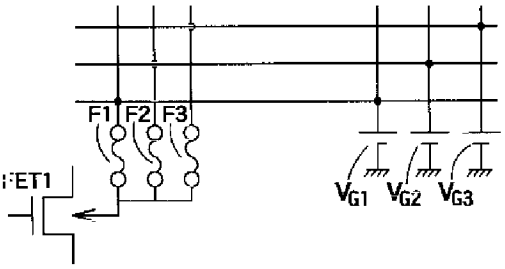
【図１５】



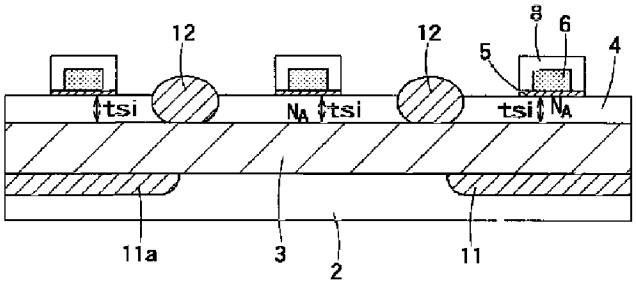
【図１６】



【図３５】

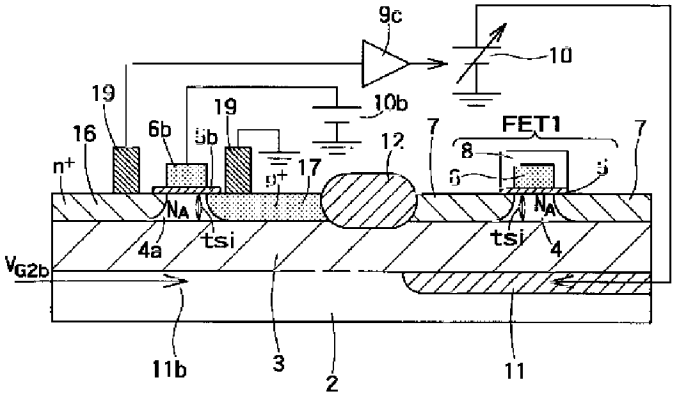


【図１７】

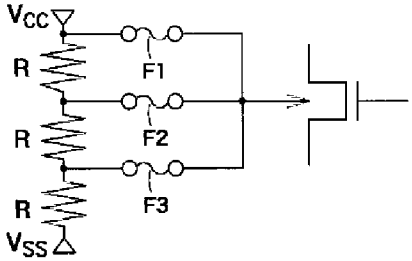


GF Exhibit 1126 - 1508/2248

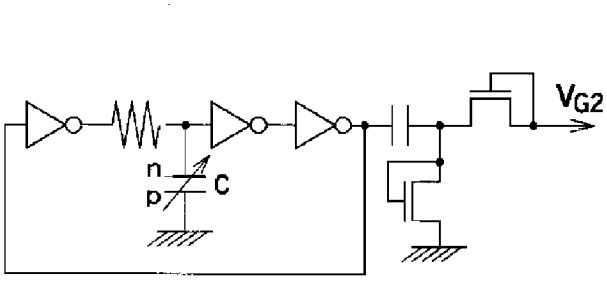
【図１８】



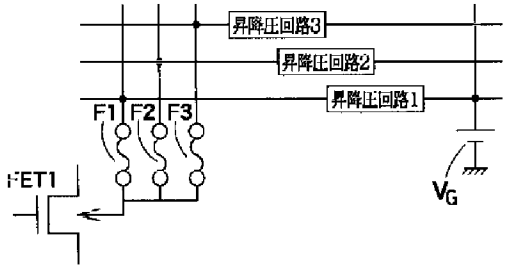
【図３７】



【図１９】

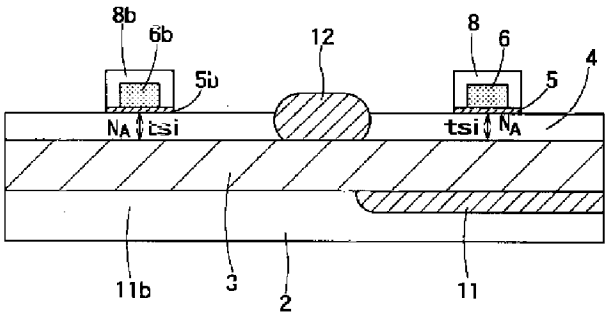


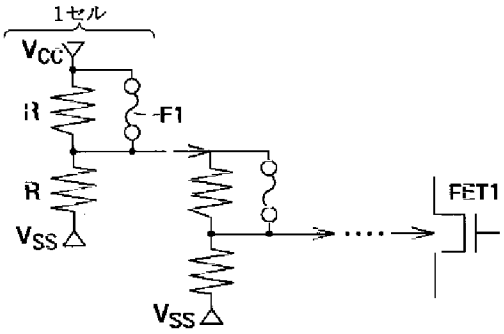
【図３６】



【図３８】

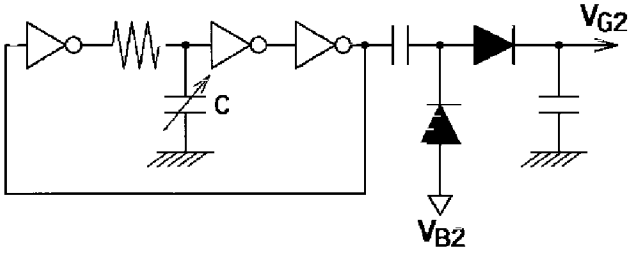
【図２０】

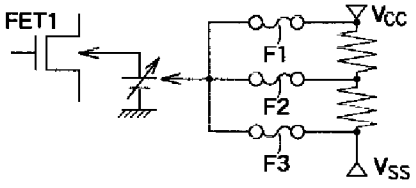




【図３９】

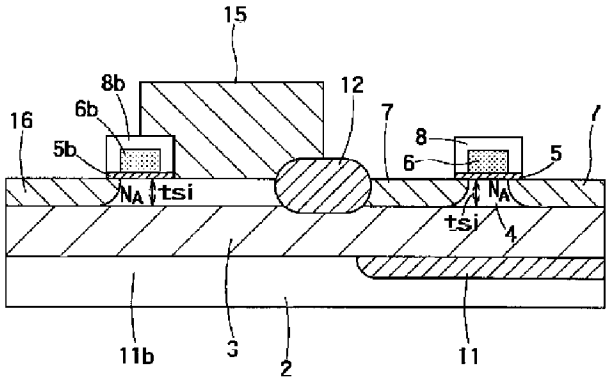
【図２３】



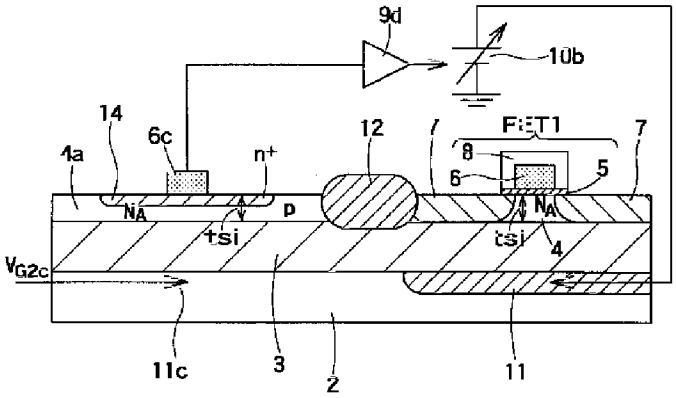


GF Exhibit 1126 - 1509/2248

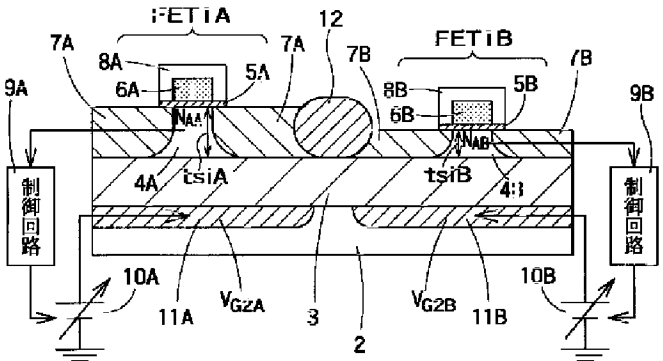
【図２１】



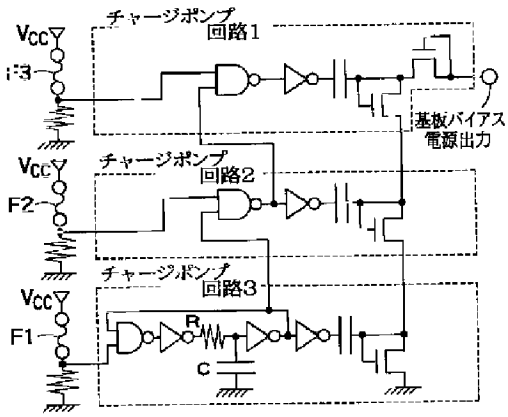
【図２２】



【図２４】

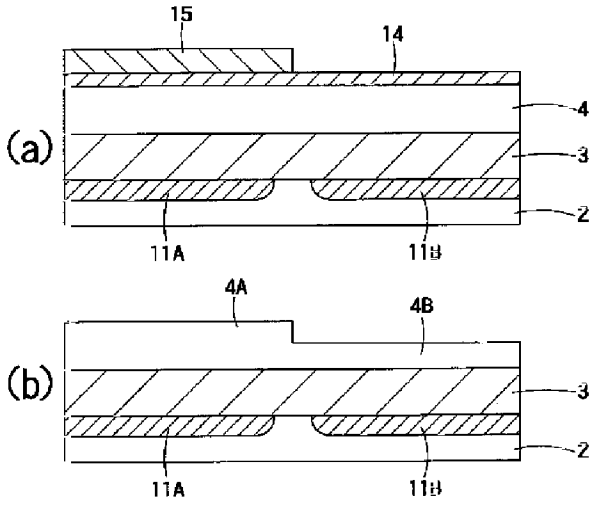


【図４０】

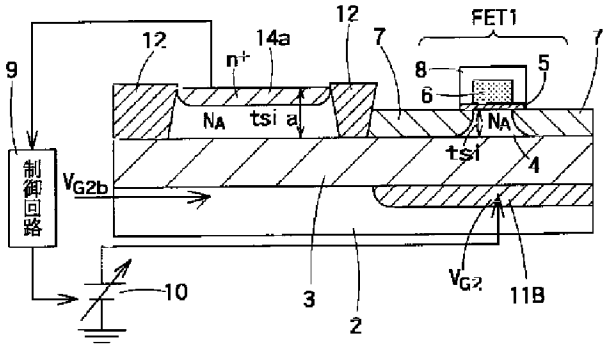


GF Exhibit 1126 - 1510/2248

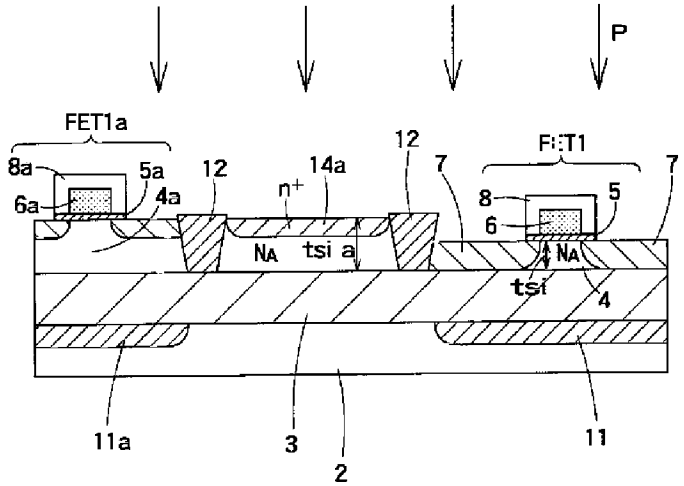
【図25】



【図26】

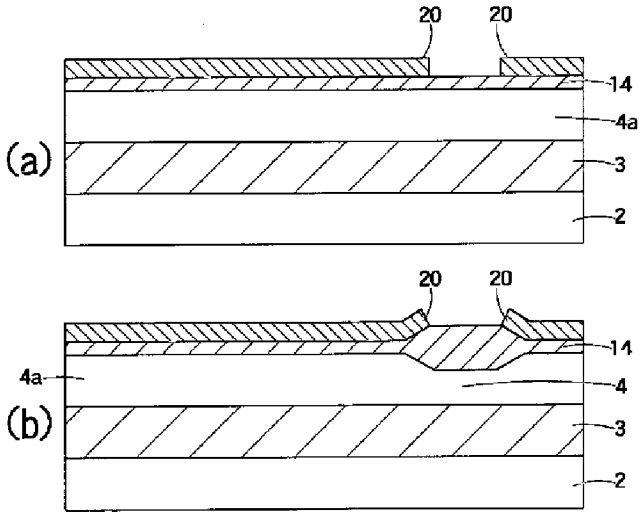


【図27】

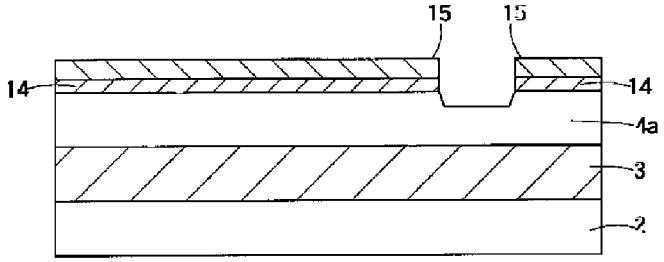


GF Exhibit 1126 - 1511/2248

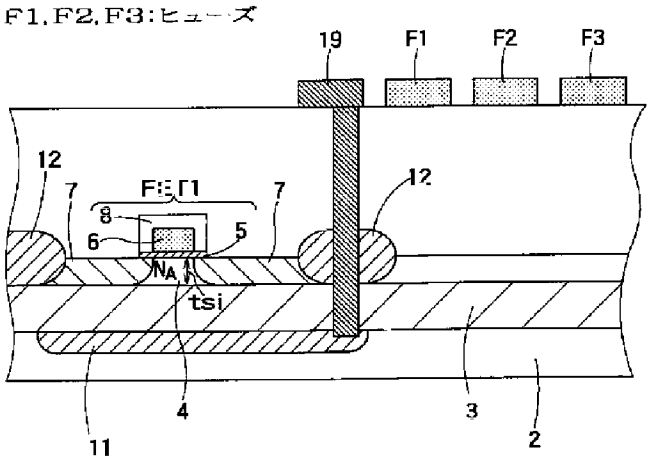
【図２８】



【図２９】

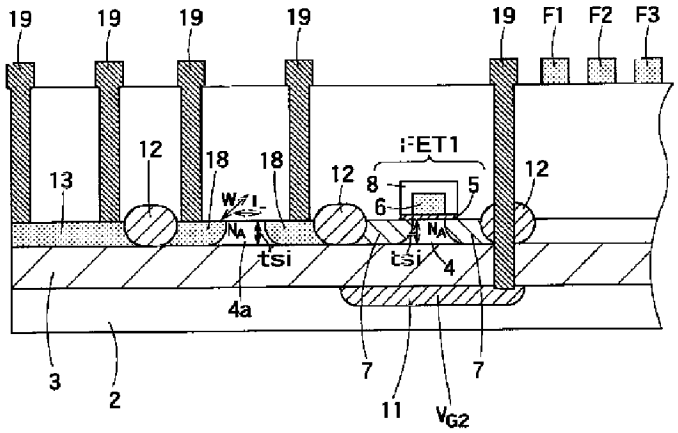


【図３０】

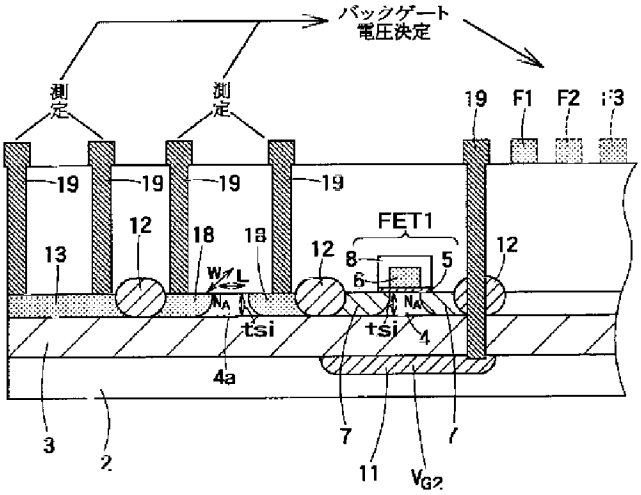


GF Exhibit 1126 - 1512/2248

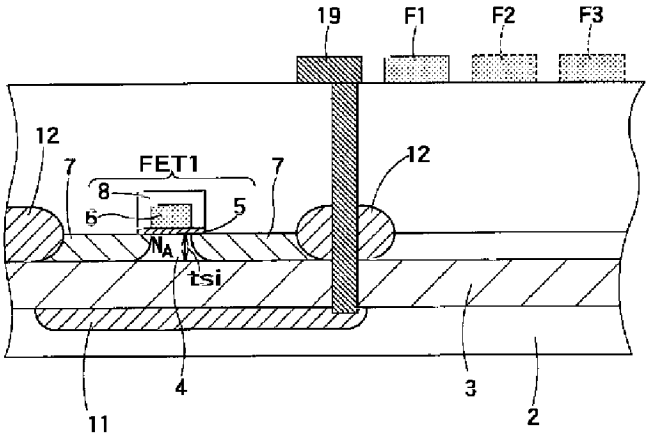
【図３２】



【図３３】



【図３４】



GF Exhibit 1126 - 1513/2248