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JPH11330482A SEMICONDUCTOR DEVICE

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SEMICONDUCTOR DEVICE

Abstract

PROBLEM TO BE SOLVED: To hold threshold sensitivity for variations of a SOI film thickness substantially at a minimum to set to a value prescribing a threshold by a method, wherein a back gate voltage is applied from a control circuit, in response to channel impurity concentration of transistors. SOLUTION: An insulating film 3, such as a silicon oxide film or the like, is formed on the main face of a silicon substrate 2, and a channel region 4 of silicon having a p-type impurity concentration NA, such as boron is formed on this insulating film. A gate electrode 6 is formed via the gate insulating film 5 on the channel region 4, and a source/drain region 7 is formed on both sides of the channel region 4, to form completely depleted transistors FET1. A control circuit 9 inputs the information measuring the impurity concentration NA and calculates an optimum back gate voltage value and outputs a corresponding control signal to a variable power source 10, so that a specified voltage is applied on a back gate 11. This application substantially minimizes the threshold sensitivity for variations of a SOI film thickness by controlling the threshold.

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DESCRIPTION JPH11330482

[0001]

TECHNICAL FIELD The present invention relates to a semiconductor device. More specifically, the present invention relates to a semiconductor device in which a fully depleted MISFET (Metal Insulator Semiconductor Field Effect Transistor) is formed on a semiconductor layer provided on a supporting substrate via an insulating film.

[0002]

2. Description of the Related Art A FET type transistor formed by using an SOI (Silicon on Insulator), that is, a semiconductor layer formed on an insulating substrate, has a parasitic capacitance between a source and a drain, which is a bulk semiconductor substrate. Since it can be made smaller than the FET formed above, it is expected to be applied to a low power consumption device or a high speed operation circuit such as a high speed CPU. In particular, when the thickness of the SOI film which is the semiconductor layer is set to be equal to or less than the thickness of the depletion layer in the channel region, the channel region can be completely depleted. As a result, it is possible to eliminate or suppress an unfavorable phenomenon such as a kink characteristic or a current overshoot effect, which is a problem in an SOI transistor formed using a semiconductor layer thicker than a depletion layer.

[0003]

In this way, a transistor capable of depleting the entire channel region (hereinafter, referred to as "completely depleted transistor") further suppresses the short channel effect, improves punch-

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through resistance, improves the subthreshold coefficient, It offers a number of benefits, including increased channel mobility.

[0004]
However, in the fully depleted transistor, if the impurity concentration of the semiconductor layer in the channel region or the SOI film thickness changes due to variations in process conditions, the threshold value changes. There was a problem.

[0005]
As a method of coping with the problem caused by such variation in process conditions, conventionally, as disclosed in, for example, Japanese Patent Laid-Open No. 9-321401, a back surface of a support substrate below an insulating layer below an SOI layer is backed up. An example is known in which a gate is provided and the threshold voltage is controlled by changing the voltage applied to the back gate during operation and during standby.

[0006]

However, in this method, the back gate voltage is determined regardless of variations in the SOI film thickness and variations in the substrate concentration.

Further, for example, there is no disclosure about a back gate voltage applying means for minimizing the threshold sensitivity to variations in the SOI film thickness and its specific configuration.

[0007]

That is, in the conventional method and structure for reducing the threshold sensitivity in the fully depleted transistor, the back gate voltage control for reducing the threshold sensitivity with respect to the variation in the SOI film thickness has been studied. The optimum value of, and the relationship with the impurity concentration were not considered.

Therefore, it is difficult to set the threshold value to a prescribed value and reduce the threshold sensitivity to variations in the film thickness of the SOI layer and the impurity concentration.

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[0008]

The present invention has been made based on the recognition of such problems.

That is, the purpose is to change the back gate voltage depending on the channel impurity concentration of MIFSET in a semiconductor device formed by forming a fully depleted MISFET transistor using an SOI layer so that the impurity concentration is It is an object of the present invention to provide a semiconductor device in which the threshold value can be set to a value that regulates the threshold value while keeping the threshold sensitivity to the SOI film thickness variation to a minimum even if it fluctuates.

[0009]
The gist of the present invention is to provide a semiconductor device in which a fully depleted transistor is formed in a semiconductor layer opposed to a back gate with an insulating film interposed therebetween, depending on the channel impurity concentration of the transistor. A semiconductor device characterized in that a control circuit capable of controlling a back gate voltage is provided to apply a back gate voltage according to an impurity concentration to the back gate.

[0010]

The semiconductor layer forming the fully-depleted SOI transistor is set to an SOI film thickness at which the threshold fluctuation is reduced at a specified threshold, and the impurity concentration is in contact with the insulating film of the semiconductor layer. The surface is set within a range determined by accumulation and inversion, for example, in the middle.

Here, if the specified threshold values are different, the film thickness for suppressing the threshold variation is different.

[0011]
That is, the semiconductor device of the present invention includes a support substrate having a back gate formed thereon, an insulating film provided on the support substrate, a first

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semiconductor layer provided on the insulating film, and the support substrate. Of a MISFET transistor facing the back gate and having a part of the first semiconductor layer as a channel region, and a dummy element for outputting a measurement signal that changes according to an impurity concentration or a carrier concentration of the first semiconductor layer. And voltage applying means for applying a voltage to the back gate according to the measurement signal output from the dummy element.

[0012]
Alternatively, in the semiconductor device of the present invention, a supporting substrate on which the first and second back gates are formed, an insulating film provided on the supporting substrate, and a first film thickness provided on the insulating film. Provided on the insulating film, a first semiconductor layer having a first semiconductor layer, a first MISFET transistor facing the first back gate of the support substrate and having a part of the first semiconductor layer as a channel region, A second semiconductor layer having a second film thickness different from the first film thickness, and a part of the second semiconductor layer facing the second back gate of the support substrate to form a channel region. And a voltage applying means for applying a voltage to the first back gate independently of the voltage of the second back gate.

[0013]
Alternatively, in the semiconductor device of the present invention, a supporting substrate having a back gate formed thereon, an insulating film provided on the supporting substrate, a first semiconductor layer provided on the insulating film, and the supporting substrate. Of a MISFET transistor having a channel region of a part of the first semiconductor layer facing the back gate, a storage element for storing information corresponding to a voltage applied to the back gate, and a storage element stored in the storage element. And a voltage applying unit that applies a voltage to the back gate based on the information.

[0014]
Alternatively, in the semiconductor device of the present invention, a supporting substrate on which the first and second back gates are formed, an insulating film provided on the supporting substrate, and a first film thickness provided on the insulating film. A first semiconductor layer having: a first MISFET transistor facing the first back gate of the supporting substrate and having a part of the first semiconductor layer as a channel region; and the first back gate. A first memory element that stores information corresponding to a voltage applied to the second semiconductor layer; a second semiconductor layer that is provided on the insulating film and has a second film thickness different from the first film thickness; A second MISFET transistor in which a part of the second semiconductor layer is used as a channel region facing the second back gate of the substrate, and the voltage of the second back gate is independent of the first

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MISFET transistor. Voltage applying means for applying a voltage to the first back gate based on the information stored in the storage element.

[0015]
Here, the storage element stores information according to an impurity concentration or a carrier concentration of the first semiconductor layer.

[0016]
Further, the MISFET transistor is a fully depleted transistor in which the channel region is completely depleted.

[0017]
In addition, the dummy element is an impedance element in which at least one of a resistance value, a capacitance value, and an inductance changes according to an impurity concentration or a carrier concentration of the first or second semiconductor layer. .

[0018]
The thickness of the first or second semiconductor layer in which the channel region of the MISFET transistor is formed is in the range of 40 nm to 100 nm, and the impurity concentration is in the range of 3×10 16 cm -3 to 3×10 17 cm -3. It is characterized by being in.

[0019]
Further, the support substrate is formed of a semiconductor substrate, and the impurity concentration of the back gate is in the range of 1×10 17 cm -3 to 1×10 20 cm -3.

[0020]
Further, a circuit for measuring the impurity concentration or the carrier concentration by the dummy element is provided on the same semiconductor layer as the MISFET transistor.

[0021]
Further, the first semiconductor layer is thicker than the second semiconductor layer, and the first semiconductor layer is lower in impurity concentration than the second semiconductor layer.

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[0022]
Further, the threshold value of the first MISFET transistor is smaller than the threshold value of the second MISFET transistor.

[0023]

According to the present invention, the film thickness of the SOI layer is set to a film thickness with which the threshold variation is reduced.

Furthermore, a desired threshold value can be maintained by measuring the impurity concentration of the channel region using the dummy element and adjusting the back gate voltage based on the measured value.

Therefore, the threshold value can be set to a desired value while keeping the threshold sensitivity to the variation of the SOI film thickness and the impurity concentration, which is a problem in the fully depleted transistor, at a minimum.

[0024]

Embodiments of the present invention will be described below with reference to the drawings.

In the following description, an n-type MOSFET will be described as an example.

Further, the pattern shape of the element isolation of the SOI layer is not essential in the present invention, and is not particularly mentioned.

[0025]

FIG. 1 is a cross-sectional view of essential parts showing a semiconductor device according to a first example of the present invention.

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That is, in the figure, 6 is a gate electrode, 7 is a source / drain region, 2 is a support substrate, 3 is an insulating film, 4 is a channel region, 5 is a gate insulating film, 8 is an insulating film, 9 is a control circuit, and 10 is a control circuit. Is a variable power supply (for example, a power supply whose output current or voltage is controlled by the voltage or current of the control input), and 11 represents a back gate.

[0026]

The specific configuration example is as follows.

That is, the insulating film 3 made of, for example, a silicon oxide film or a silicon nitride film having a thickness of 10 nm to 1 μm is formed on the main surface of the support substrate 2 made of silicon, and the film thickness tsi, boron or indium is formed on the insulating film 3. A channel region 4 made of silicon or the like having a p-type impurity concentration NA is formed.

The film thickness tsi may be, for example, 1 nm to 500 nm, and the impurity concentration NA may be, for example, 1016 to 1019 cm-3.

[0027]

A gate electrode 6 is formed on the channel region 4 with a gate insulating film 5 interposed therebetween.

As a material of the gate insulating film 5, for example, a silicon oxide film, a silicon nitride film, a tantalum oxide film, a titanium oxide film, or the like can be used, and the thickness thereof can be set to 1 nm to 200 nm.

As a material of the gate electrode 6, for example, polycrystalline silicon, aluminum (Al), tungsten (W), titanium nitride (TiN), or the like can be used, and the thickness thereof can be set to 10 nm to 1 μm.

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[0028]

The gate electrode 6 is insulated by covering its sidewall with an insulating film 8 made of, for example, a silicon oxide film or a silicon nitride film.

On both sides of the channel region 4, there are formed source / drain regions 7 to which arsenic (As), phosphorus (P), antimony (Sb), etc., which are n-type impurities, are added, for example, 10 18 to 10 21 cm −3.

Here, the channel region 4 is completely depleted in the state where the inversion layer is formed at the interface between the channel region 4 and the insulating film 5, and forms the fully depleted transistor FET1.

[0029]

On the other hand, as will be described later in detail, the control circuit 9 inputs the information on the voltage, current, capacitance or resistance value from a dummy element (not shown) for measuring the impurity concentration NA in the semiconductor layer, particularly in the channel region 4, to obtain the optimum value. The back gate voltage value is calculated and a control signal corresponding to it is output.

The variable power supply 10 applies a predetermined back gate voltage to the back gate 11 based on the control signal output from the control circuit 9.

[0030]

Next, a manufacturing process of the semiconductor device shown in FIG. 1 will be described. Here, a silicon substrate is used as the support substrate 2, a silicon oxide film is used as the insulating film 3, and an SOI layer made of silicon is used as the channel region 4 and the source / drain regions 7. As a method of producing such an SOI substrate, a method of bonding two silicon substrates whose one surface is oxidized with their oxide film surfaces in close contact

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with each other by heat treatment at 1000 to 1200 ° C. can be used. Alternatively, a buried oxide film 3 is formed by implanting oxygen ions into a silicon substrate under conditions of an acceleration voltage of 160 keV and a dose amount of about 1.5 to 3.0 × 10 18 atoms / cm 2 and heat treating at 1300 to 1350 ° C. You can also do

[0031]
The semiconductor layer on the insulating film 3 is thinned by polishing, ion etching, or wet etching to form a uniform SOI film having a thickness of 40 nm to 1 μm.

[0032]

Next, as the back gate 11, an impurity added region is formed in the supporting substrate 2 by lithography and ion implantation.

That is, for example, phosphorus (P) or arsenic (As) is applied to the supporting substrate 2 through the insulating film 3 in a region where a MISFET transistor is formed by lithography, an accelerating voltage of 50 to 700 keV, a dose amount of 1 × 10 13 to 1 × 10 16 atom / The back gate 11 can be formed by implanting under the condition of about cm 2. However, the step of forming the back gate 11 may be performed before the formation of the insulating film 3 and the SOI layer 4.

[0033]
Next, ion implantation is performed so that the impurity concentration of the channel region 4 is in the range of 1.times.10@16 cm @ -3 to 1.times.10@19 cm @ -3.

[0034]
After that, the gate oxide film 5 is formed, and further the gate electrode 6 and the insulating film 8 are formed, whereby the main part of the MISFET 1 is completed.

[0035]
In the manufacturing process described above, in particular, in order to set the threshold value in the range of −0.1 to 0.4 V in the fully depleted SOI transistor, the SOI film thickness and impurity concentration of the channel layer 4 are 40 nm to 40 nm, respectively. It is desirable that the thickness is in the range of 1 μm, 3 × 10 16 cm −3 to 3 × 10 17 cm −3.

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[0036]
Next, the optimum range of the SOI film thickness tsi of the channel region 4, the impurity concentration NA, and the back gate voltage VG2 in the semiconductor device of the present invention will be described.

[0037]

FIG. 2 is a graph showing the relationship between the SOI layer and the threshold value of the fully depleted FET obtained by the calculation of the present inventor.

Here, a silicon oxide film having a film thickness of 80 nm is used as the insulating substrate 3, a 1×10 20 cm -3 p-type Si substrate is used as the back gate 11, and 1×10 20 cm -3 n-type polysilicon (polycrystalline silicon) is used as the gate electrode 6. As the gate oxide film 5, an n-type MOSFET having a silicon oxide film of 3 nm was used as a model.

The solid line in FIG. 2 shows the relationship between the film thickness of the channel region 4, that is, the SOI film thickness tsi and the threshold value Vth, when the back gate voltage is 0 V and the impurity concentration of the channel region 4 is 1×10 17 cm -3.

[0038]

In the calculation of the relationship shown in this graph, an equation expressing the threshold value of the fully depleted transistor was used as a reference (“Electrical characterization of Silicon-on-Insulator Materials and Devices” Sorin Cristloveanu and Sheng S.Li, Kluwer Academic. Publishers, (1995)) and the surface quantum effect as a reference (MJvan Dort, PHWoerlee, AJWalker, CAHJuffermans and H.Lifka: IEDM91 p495, (1991)). , (JWSlotboom and HCde Graaff, IEEE trans.

Electron Devices, vol.

ED-24, No.8, pp.1123-1125, (1977)), ("Quantum Mechanics for Device Physics" by David K.

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Ferry, Yosuke Nagaoka et al., Maruzen, (1996)). Considering what is present.

[0039]

As can be seen from FIG. 2, the threshold value of the transistor has a minimum value (arrow in FIG. 2) with respect to the film thickness tsi of the channel region 4. In the vicinity of this minimum value, the amount of change in the threshold value becomes minimum with respect to the change in the film thickness tsi. That is, the threshold sensitivity to the variation in the film thickness of the SOI layer becomes extremely small.

[0040]

Further, by applying the back gate voltage, the electronic state of the surface of the channel region 4 in contact with the insulating film 3 is accumulated (broken line Vth1, ac2 in FIG. 2) or inverted (broken line Vth1, in FIG. 2). The threshold can be changed within the range of inv2). Therefore, the threshold voltage is controlled by applying a predetermined back gate voltage, and the film thickness of the channel region 4 is formed so that the desired threshold value matches the minimum value in FIG. The transistor can set the threshold value sensitivity to the SOI film thickness variation to a minimum at a set value.

[0041]

Next, a method of calculating the SOI threshold value as shown in FIG. 2 will be described in detail. In the following description, the calculation method based on the classical theory model will be described first, and then the calculation method in which the effect of the surface quantization of the channel inversion layer is corrected will be described.

[0042]

First, in a fully depleted transistor to which a back gate voltage can be applied, the threshold value depends on the electronic state on the surface of the channel region 4 in contact with the insulating film 3. The state of the surface of the channel region 4 in contact with the insulating film 3 can be changed from the accumulated state to the inverted state by the back gate voltage.

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[0043]
The relationship between the gate voltage VG1 and the surface potential at this time is expressed by the following equation.

[0044]

Here, Φs1 and Φs2 are the Fermi potentials on the surface in contact with the gate insulating film 5 and the surface in contact with the insulating film 3, respectively, of the channel region 4, and ΦMs1 is the difference in work function from the gate electrode 6 on the gate insulating film 5 side. , QOX1 represents the fixed charge density in the gate insulating film 5, COX1 represents the capacitance of the gate insulating film 5, and Qinv1 represents the inversion layer charge of the channel in the channel region 4.

Qdep1 represents the charge of the depletion layer in the channel region 4, and is represented by −qNAtsi using the electron charge amount q, the impurity concentration NA of the channel region 4, and the film thickness tsi of the channel region 4. The Fermi potential Φp is expressed as Φp = (kT / q) ln (NA / ni) using the intrinsic carrier density ni of silicon, the Boltzmann constant k, the temperature T, and the amount of charge q of electrons, and Csi = E si / tsi (ε si is the dielectric constant of silicon).

[0045]

The threshold value Vth of the fully depleted transistor can be expressed in the following cases depending on the electronic state of the surface of the channel region 4 in contact with the insulating film 3. The surface potential Φsi and the channel inversion layer charge Qinv1 when VG1 = Vth are Φsi = 2ΦF and Qinv1 = 0, respectively, because the gate voltage is the threshold value.

[0046]
When back surface is accumulated, Φs2 = 0

[0047]

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Here, the subscripts "1" and "2" of Vth1 and acc2 represent the states of the surface of the channel region 4 in contact with the gate insulating film 5 and the surface in contact with the insulating film 3, respectively.

In the case of the formula (2), the case where the surface of the channel region 4 in contact with the insulating film 3 is in an accumulated state is shown.

[0048]
When the back surface is inversion, $\Phi s2 = 2\Phi F$

[0049]

When the back surface is depleted, its potential is intermediate between accumulation and inversion, and $\Phi s2$ depends on the back gate voltage VG2.

At this time, if the back gate voltage VG2 when the surface of the channel region 4 in contact with the insulating film 3 is accumulated and inverted is VG2, acc and VG2, inv, respectively, the condition of VG2, acc <VG2 <VG2, inv is satisfied. .. Furthermore, since the capacitance Csi of the channel region 4 and the capacitance COX2 of the insulating film 3 are connected in series, $\Phi s2$ is

[0050]

Is expressed as Therefore, the threshold value is expressed by the following equation.

[0051]
Here, VG2, acc is considered to be symmetrical with respect to the surface of the insulating film 3, and the following is obtained from the condition of $\Phi s1 = 2\Phi F$ and $\Phi s2 = 0$.

[0052]

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FIG. 3 is calculated by the equations (2) to (5) for the case where the impurity concentration NA of the channel region 4 is NA = 1 × 10 17 cm −3, the SOI film thickness tsi = 60 nm, ΦMs1 = −1V, and QOX1 = QOX2 = 0. 6 is a graph showing a relationship between a back gate voltage and a threshold.

In the fully depleted transistor, when the electronic state on the surface of the channel region 4 in contact with the insulating film 3 is inverted or accumulated, the potential Φs2 on the surface becomes constant. Therefore, even if a back gate voltage higher than that is applied, the threshold value becomes a constant value without depending on the back gate voltage. That is, the threshold value of the fully depleted transistor is limited within the range of the threshold value when the electronic state of the surface of the channel region 4 in contact with the insulating film 3 and the threshold value when the electronic state is inverted. ..

[0053]

FIG. 4 shows the SOI film thickness of the channel region 4 of the threshold value calculated using the classical theory model of the equations (2) to (5) when the impurity concentration of the channel region 4 is 1 × 10 17 cm −3. It is the graph which showed the dependency. In the figure, Vth1 and acc2 are shown by broken lines, Vth1 and inv2 are shown by dotted lines, and the threshold for the SOI film thickness at VG2 = 0V is shown by solid lines. Vth1, acc2, Vth1, inv2 are determined by the film thickness of the channel region 4 without depending on VG2. On the other hand, the threshold values of Vth1 and dep12 change depending on the back gate voltage VG2. As can be seen from FIG. 4, Vth1, dep12 in the classical theory model linearly decreases as the SOI film thickness decreases, because the depletion layer charge (−Qdep1) contained in the SOI depletion layer decreases.

[0054]

Next, a case where the surface quantization correction of the channel inversion layer is added to the classical model described above will be described. The threshold change due to such surface quantization correction can be analytically obtained. Here, in the surface quantization correction, the increase amount ΔΨs of the surface band bending of the surface potential and the decrease of the gate capacitance due to the inversion layer capacitance were considered.

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[0055]
The amount of increase in surface band bending due to surface quantization correction of the surface potential is

[0056]

It is represented by.

The surface potential Φs1 when the gate voltage is the threshold value is obtained by adding 2ΦF to this equation.

[0057]
FIG. 5 is a band diagram for explaining the surface quantization correction.

[0058]
As shown in FIG. 5, the equation (6) is a shift Eo-Ec from the conduction band Ec to the lowest energy level Eo, a bandgap narrowing effect ΔEg due to the addition of a high concentration channel impurity, and quantum theory. Of Es Δz of the surface potential due to the shift Δz of the position where the surface charge density is maximum due to the above, and each term is expressed as follows.

[0059]
The shift Eo-Ec to the lowest energy level Eo is

[0060]
Where Es is the surface electric field,

[0062]
The bandgap narrowing effect ΔEg due to the addition of high-concentration channel impurities is

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[0063]
The approximate expression of Es Δz is

[0065]
Further, due to the effective interface quantum effect, the center of the inversion layer charge is separated from the interface between the Si film and the SiO2 film by Δz, so that the gate oxide film capacitance COX1 is COX1 = ε OX / (tOX1 + ε Si / ε OX Δz). expressed.

[0066]

FIG. 2 shows the dependence of the threshold value on the SOI film thickness of the channel region 4 obtained in consideration of the quantum correction as described above.

As can be seen from FIG. 2, when the back gate voltage is kept constant and the film thickness of the channel region 4 is changed, the threshold takes a minimum value (arrow in FIG. 2).

Then, as the thickness of the channel region 4 becomes thinner, the threshold value increases.

This is because the electric field Es at the interface between Si and SiO2 increases when the film thickness of the channel region 4 decreases under the condition that the back gate voltage is constant, so that the energy of the quantum level increases and the surface is inverted. This is because a large gate voltage is required.

[0067]
As described above, it is explained that there is a film thickness of the channel region 4 having the minimum threshold sensitivity with respect to the film thickness variation of the channel region 4 by using the calculation considering the quantum correction.

[0068]

FIG. 6 shows the same FET model as in FIG. 2, in which the SOI film thickness tSi of the channel region 4 and the back gate voltage VG2 to be applied, which has the minimum threshold value in

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FIG. It is the graph shown to the contrary.

Here, the case where the set values of the threshold values are 0.1 V, 0.2 V, and 0.3 V are shown.

[0069]

As can be seen from FIG. 6, the SOI film thickness tSi at which the threshold value is set and the threshold sensitivity to the film thickness variation is minimum has a low dependence on the impurity concentration NA of the channel region 4. It was newly clarified by the detailed study by the present inventor.

That is, the optimum value of the SOI film thickness tSi does not change much with respect to the impurity concentration NA, and takes an almost constant value.

[0070]

Further, it has been found that when the thresholds to be set are different, the SOI film thickness tSi at which the threshold sensitivity to the variation of the SOI film thickness is almost minimum is different.

Here, the relationship between the optimum value of tSi and the threshold value Vth is tSi = 250Vth2−275Vth + 105 (nm), and it can be approximated that Vth is 0 volt or more and 0.5 volt or less.

Therefore, even if Vth is an arbitrary value, the optimum value of tSi can be obtained.

Further, it is newly revealed that the back gate voltage VG2 required for the threshold value to reach the set value increases almost linearly with respect to the impurity concentration NA of the channel region 4.

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[0071]
Therefore, when the SOI film thickness tSi and the impurity concentration NA are determined based on FIG. 6 according to the desired threshold value, even if the impurity concentration NA deviates from a desired value due to, for example, process variations. By measuring the impurity concentration of the channel region 4 and applying the back gate voltage required for the threshold value to have a set value accordingly, the threshold sensitivity to the SOI film thickness is minimized, and A semiconductor device having a set threshold value can be realized.

[0072]
Here, the SOI film thickness at which the threshold sensitivity to film thickness variation is almost the same is almost constant with respect to the impurity concentration NA of the channel region 4 because the quantum mechanical correction term of the equation (6) is tSi. It is strongly dependent and not so dependent on NA, and that Qdep1 of the depletion layer charge in the equation (5) can be almost compensated by changing VG2 even when NA is changed.

[0073]
Due to this feature, of course, even when the concentration distribution of the channel region 4 is not uniform and has a predetermined impurity profile, when Qdep1 / 2COX1 is smaller than 2ΦF in the formula (2), the impurity concentration NA becomes On the other hand, the characteristic that the threshold sensitivity is almost constant is maintained.

[0074]

In the case of a MISFET having a recess gate structure formed by a method such as LOCOS sacrificial oxidation as shown in FIG. 7, the thickness of the channel region 4 is not constant due to the bird's beak at the LOCOS end. In many cases.

That is, the thickness of the channel region is thicker near the source / drain and thinner near the center.

FIG. 8 is a schematic process cross-sectional view showing a manufacturing process of a recess type gate structure by the LOCOS sacrificial oxidation method.

For example, a silicon oxide film 14 having a thickness of about 5 to 100 nm is formed on an SOI

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layer 4 such as silicon having a thickness of 20 nm to 1 μm, and a silicon nitride film having a thickness of, for example, 50 to 200 nm is formed thereon. The antioxidant film 20 is deposited. Next, as shown in FIG. 8A, LOCOS is formed by a thermal oxidation method. Further, as shown in FIG. 8B, the LOCOS oxide film is ion-etched using the antioxidant film 20 as a mask to form a gate formation region. According to this method, the gate electrode can be formed in a self-aligned manner, but since the bird's beak of LOCOS remains in the gate formation region, the SOI film thickness in the channel region tends to be nonuniform as shown in the figure. When the film thickness of the channel region becomes nonuniform in this way, the stability of the threshold value deteriorates, which becomes a problem.

[0075]

On the other hand, according to the present invention, even when the film thickness of the channel is not uniform, for example, in the SOI film thickness of the central portion of the channel, the threshold sensitivity with respect to the film thickness variation with respect to a predetermined threshold value is obtained. A desired threshold value can be stably obtained by setting the SOI film thickness so as to be the minimum. Therefore, the non-uniformity of the SOI film thickness in the vicinity of the center of the channel and the end part thereof falls within, for example, 20% so that the SOI film thickness of the channel region becomes the optimum film thickness as shown in FIG. 2 or 6. Thus, the desired threshold value can be obtained by performing the LOCOS oxidation.

[0076]

Here, the measurement location of the impurity concentration NA of the channel region 4 does not necessarily have to be the channel region 4 of the MISFET itself, and may be a region having the same impurity concentration as the channel region of the MISFET. For example, when manufacturing an integrated device in which a plurality of MISFETs are integrated, the measurement may be performed at any place of the integrated device. Further, when a plurality of integrated devices are formed on a wafer, if the uniformity of the impurity concentration within the wafer is good, the measurement may be performed at any place on the wafer. Furthermore, in a so-called “batch processing” manufacturing process in which multiple such wafers are processed at the same time, if the fluctuation of the impurity concentration for each wafer in the batch is small, measurement is performed on either wafer for each batch. I'm fine.

[0077]

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In this way, by measuring the impurity concentration of the channel region 4 and determining the back gate voltage for setting the threshold value, it is not necessary to change the back gate voltage as long as the transistor is used at this threshold value. .. That is, the control circuit is not necessarily required after the back gate voltage is determined. Therefore, if the impurity concentration of the channel region 4 is measured and the back gate voltage required for the present invention is obtained, it is only necessary to set the variable power supply applied to the back gate so as to output the required voltage.

[0078]

Here, the measurement of the impurity concentration of the channel region 4 is introduced, for example, in a document (“Materials Processing Theory and Practice volume.2-impurity doping processes in silicon” : FFYWang, North Holland Publishing Company (1981)). The measurement method described above may be used. An example of the configuration including the measurement of the impurity concentration is shown below.

[0079]

FIG. 9 is a schematic sectional view showing a second specific example of the semiconductor device of the present invention. In the figure, the same parts as those in FIG. 1 are designated by the same reference numerals, and detailed description thereof will be omitted.

[0080]

In FIG. 9, 4a is a dummy region, 12 is an element isolation region, 13 is a high-concentration semiconductor region, 18 is an electrode region, and 19 is a metal plug. The dummy region 4a is a semiconductor region created under the same conditions as the channel region. The high-concentration semiconductor region 13 is, for example, a semiconductor region doped with a p-type dopant to the solid solution limit.

[0081]

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The back gate 11 is a conductive region formed in the support substrate 2. For example, when the support substrate 2 is p-type Si and the back gate 11 is n-type Si, different voltages are applied to the back gate 11 and the back gate 11. It is desirable to do so. The back gate 11 is formed immediately below the FET for controlling the threshold value, and is not formed below the dummy region 4a for measuring the impurity concentration. This is to prevent the thickness of the depletion layer in the dummy region 4a from changing due to the voltage applied to the back gate 11.

[0082]

Hereinafter, a method for measuring the impurity concentration and the film thickness of the channel region 4 will be described. In FIG. 9, circuits 9 and 9a are control circuits, and the resistance of the high concentration semiconductor region 13 formed at the solid solution limit in the circuit 9a is measured to obtain the SOI film thickness and output to the circuit 9. In the circuit 9, the resistances 18-4a-18 at both ends of the dummy region 4a are measured, and the impurity concentration of the channel region 4 is obtained using the SOI film thickness data input from the circuit 9a. The value of the back gate voltage required to obtain a desired threshold value is obtained from the impurity concentration thus obtained, and is output to the power supply 10.

[0083]

In the configuration example of FIG. 9, a p + type electrode region 18 having the same conductivity as the semiconductor layer is formed so as to contact the dummy region 4a to which the same impurity is added as the channel portion of the transistor FET1. Then, the control circuit 9 measures the resistance between the electrode regions 18 and 18. Here, the resistivity ρ is expressed as $\rho = WtSiR / L$, where R is the resistance, L is the distance between the electrode regions 18, W is the width, and tSi is the SOI film thickness. If the resistivity ρ is obtained in this way, the impurity concentration NA of the channel region 4 can be obtained from, for example, an Irvin curve.

[0084]

On the other hand, the SOI film thickness tSi can be obtained from the high concentration

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semiconductor region 13. That is, as shown in FIG. 9, in the p + type high-concentration semiconductor region 13 in which silicon (B) or the like is doped to a concentration of the solid solution limit, the resistance of the semiconductor region 13 is obtained. The resistivity ρ can be obtained from the resistance of the high-concentration semiconductor region 13, and since the impurity concentration has a value determined by the solid solubility, tSi and NA can be decomposed. Therefore, the film thickness of the semiconductor layer can be obtained by measuring the resistance in the high-concentration semiconductor region 13.

[0085]

The impurity concentration NA in the channel region 4 can be obtained by substituting the SOI film thickness tSi obtained by the above method into the above equation. In this configuration example, the NA measurement area can be formed by the same process as that for forming the MISFET 1.

[0086]

Here, as specific examples of the circuit 9 and the circuit 10, for example, a half-Vdd circuit and a substrate bias circuit can be cited. FIG. 10 is a schematic circuit diagram showing an embodiment using the half-Vdd circuit. VB2 is, for example, a voltage of 0 V, VB1 is, for example, a voltage of VDD, and VB1> VB2. The resistor 18-4-18 in FIG. 10 is the resistance measuring device 18-4-18 formed in the dummy region 4a in FIG. 9, and R1 is the resistance when the dummy region 4a is formed at the set impurity concentration. A resistor having the same resistance value as the value. Further, the transistors Q3 and Q4 are formed wider than Q1 and Q2 to form a current buffer. Furthermore, it is assumed that the conductance of R1 and 18-4-18 is sufficiently smaller than the transconductance of Q1 or Q2. When the impurity concentration fluctuates, the resistance of 18-4-18 changes, so the voltage output by the resistance division also changes, and when the 18-4-18 resistance increases, the output decreases, and 18-4 As the −18 resistance decreases, the voltage at the node Vo increases. The voltage V1 of the node connected to the back gate 11 is determined so that the output node Vo becomes equal to the voltage. Therefore, the back gate voltage can be changed by changing the resistance of the resistance measuring device. Here, the influence of the change in the SOI film thickness tSi can be removed by changing VB1.

[0087]

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11 (a) and 11 (b) are schematic circuit diagrams showing an embodiment of the substrate bias circuit. That is, when the 18-4-18 resistor is provided in the ring oscillator and the impurity concentration of the dummy region 4a changes, the resistance changes, so that the frequency of the ring oscillator changes. Due to this frequency change, the number of excitations of the charge pump circuit changes, the current supplied to the back gate changes, and the back gate voltage can be changed.

[0088]

Next, a manufacturing process of the semiconductor device of FIG. 9 will be described. 12 to 14 are process cross-sectional views showing the main part manufacturing process of the semiconductor device of FIG. First, as shown in FIG. 12, the back gate 11 is formed. Specifically, a resist mask 15 is formed on the SOI wafer, and impurities such as boron are ion-implanted into the supporting substrate 2 such as silicon via the channel region 4 and the insulating film 3. In this way, the p-type back gate 11 having an impurity concentration of, for example, 1×10 17 cm -3 to 1×10 20 cm -3 can be formed.

[0089]

Here, the channel region 4 and the dummy region 4a can be formed by the method described above with reference to FIG. The dummy region 4a is a region for measuring the impurity concentration in the channel region 4. Therefore, it is desirable that the channel region 4 and the channel region 4 are formed under the same conditions in the manufacturing process.

[0090]

Next, the element isolation region 12 is formed as shown in FIG. 13, and gate electrodes 6 and 6a having a gate length L are formed by lithography. Further, insulating films 8 and 8a are formed on the gate electrode.

[0091]

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Next, as shown in FIG. 14, an electrode region is formed. Specifically, the region where the MISFET is formed is masked with a resist mask 15, and, for example, boron is ion-implanted on both sides of the gate electrode 6 at a dose amount of 1013 to 1016 cm-2 to form a p-type electrode region 18. To do.

[0092]

The step of forming the electrode region 18 can be performed simultaneously with the formation of the source / drain of the p-type MISFET. That is, after the step of forming the gate electrode, the p-type electrode region 18 and the source / drain region 7 can be simultaneously formed by using the gate electrode as a mask by ion-implanting boron, for example.

[0093]

Further, a high-concentration semiconductor region 13 in which, for example, boron is ion-implanted to the solid solution limit of the semiconductor layer is formed in a region different from the region where the electrode region 18 is formed (FIG. 14). The high-concentration semiconductor region 13 can be formed at the same time by ion implantation for forming the electrode region 18 and the source / drain region 7 described above. That is, when the region where the gate is not formed is provided and the ion implantation for forming the source / drain regions of the p-type MISFET is performed, for example, by implanting boron to the impurity concentration of the solid solution limit of silicon, the high concentration semiconductor region 13 is formed. Can also be formed.

[0094]

Next, as shown in FIG. 9, the contact 19 to the back gate 11 is formed. Specifically, the metal contact 19 can be formed by forming a contact hole from above the element isolation region 12 by, for example, ion etching, and further depositing an electrode material such as tungsten (W). The step of forming the metal contact 19 can be performed simultaneously with the formation of the metal contact in the resistance measuring region shown in FIG. 9 and the contact (not shown) to the gate / source / drain electrodes. When these contact holes are formed, ion etching is performed using a gas having a large etching selection ratio between the silicon oxide film and silicon, so that regions having different depths of the contact holes can be simultaneously etched. Next, another configuration example for obtaining the SOI film thickness tSi will be described.

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[0095]

FIG. 15 is a schematic cross-sectional view showing a third specific example of the semiconductor device of the present invention. In the configuration shown in the figure, a dummy region 4b is formed separately from the MISFET transistor 1, and a gate electrode 6b and a back gate 11a are provided above and below the dummy region 4b. Then, the capacitance of the capacitance between these electrodes is measured. Here, it is desirable that the back gate 11a be sufficiently doped with impurities, for example, 1018 cm-3 or more, so that surface depletion does not occur in the surface semiconductor layer of the back gate. Further, it is desirable that the dummy region 4b of the electrode 6b and the electrode 11a be completely depleted so that an inversion layer does not occur on the surface thereof.

[0096]

The capacitance Ctotal measured under such conditions is equal to the capacitance of the gate insulating film 5, the dummy region 4b, and the insulating film 3 in series. Therefore, assuming that the dielectric constants of the gate insulating film 5 and the dummy region 4b (that is, the channel region 4) are ε OX and ε Si, and the film thicknesses of the gate insulating film 5, the dummy region 4b, and the insulating film 3 are tOX, tSi, and tbox, respectively. , The capacitance is

[0097]

であらわされる。 Therefore, the film thickness tOX of the gate insulating film 5 and the film thickness tbox of the insulating film 3 are obtained, and if the capacitances of the gate insulating film 5 and the insulating film 3 are known, the film thickness of the dummy region 4b (that is, the channel region 4). It is possible to calculate tSi = ε Si / Ctotal− ε Si (tOX + tbox) / ε OX.

[0098]

Further, tSi can be obtained by using a dummy element formed on the left side of the semiconductor device shown in FIG. 18, which will be described later in detail. That is, in FIG. 18,

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the capacitance Ctotal between the n + layer 16 and the back gate 11b is measured. Here, it is assumed that the voltage source of 10b is applied with a voltage sufficient to form an inversion layer at the interface between the gate insulating film 5b and the SOI layer 4a. Further, under the condition that the back gate side of the dummy region 4a is depleted by applying a sufficient voltage to the back gate, the measured capacitance Ctotal is

[0099]

It is represented by. Therefore, if tbox is known, tSi can be calculated. According to this method, tSi can be accurately calculated even if tox varies.

[0100]

Further, as a method for obtaining the resistivity, a 4-terminal method in which the voltage / current terminals are separated may be used. This method has an advantage that errors due to the contact resistance of the electrodes can be reduced.

[0101]

Next, a method of manufacturing the semiconductor device shown in FIG. 15 will be described. 16 and 17 are schematic process cross-sectional views showing the main part manufacturing process of the semiconductor device of FIG. For example, 1 × 10 18 cm −3 to 1 × 10 20 cm is formed by lithography and ion implantation of boron, for example, into the MISFET and the region of the support substrate 2 made of, for example, silicon that opposes through the insulating film 3 in the region for measuring capacitance. The p-type back gates 11 and 11a having an impurity concentration of −3 are formed (FIG. 16). Here, the channel region 4 and the dummy region 4b can be formed by the manufacturing process as described above with reference to FIG.

[0102]

Next, as shown in FIG. 17, the element isolation region 12 is formed, and the gate insulating film 5 and the gate electrode 6 are further formed. Subsequently, as shown in FIG. 15, the electrode

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region 18 and the source / drain region 7 are formed. These manufacturing methods can be similar to those described above with reference to FIG. Here, in the case of the specific example of FIG. 15, in order to measure the capacitance of the dummy region 4b, the semiconductor layer under the gate electrode 6b may be sufficiently depleted. Therefore, even in the ion implantation for forming the electrode region 18 and the source / drain region 7, the gate electrode 6b plays a role of a mask, and it is not necessary to mask this region with a resist or the like.

[0103]

Next, a fourth specific example of the semiconductor device of the present invention will be described. FIG. 18 is a schematic cross-sectional view showing a fourth specific example of the semiconductor device of the present invention. That is, in the semiconductor device shown in the figure, the impurity concentration can be obtained by the CV measurement method using the dummy element of the MIS capacitor provided separately from the MISFET 1. An insulating film 5b is laminated on the dummy region 4a adjacent to the FET 1 via the element isolation region 12, and, for example, p + type polysilicon (polycrystalline silicon) 6b is further laminated as a MIS capacitor electrode.

[0104]

Further, a voltage source VG2b different from the voltage source used for the MISFET transistor is provided in the back gate 11 formed under the MIS capacitor. The voltage source VG2b may be a fixed power supply to which a voltage is applied so that the electronic state of the surface of the dummy region 4a in contact with the insulating film 3 is accumulated.

[0105]

By using such a MIS capacitor, the impurity concentration of the semiconductor can be obtained by the CV method, and the back gate voltage required to realize the present invention can be determined. The capacitance is measured by applying a fixed gate voltage to the extent that the dummy region 4a is not completely depleted, and using the electrodes of the n + type and p + type semiconductor regions provided near the gate.

[0106]

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Since the capacity at this time is proportional to (NA) 1/2 when the impurity concentration is NA, NA can be obtained from the capacity.

[0107]

FIG. 19 is a schematic circuit diagram showing a specific example of the circuits 9c and 10b.

The circuit shown in the figure is similar to the circuit shown in FIG. 11, for example, and the capacitance C by the MIS capacitor of the dummy element is incorporated in the ring oscillator. When the impurity concentration of the dummy region 4a changes, the capacitance C changes and the frequency of the ring oscillator changes. The back gate voltage can be changed by changing the frequency.

[0108]

Next, a method of manufacturing the semiconductor device of FIG. 18 will be described. 20 and 21 are schematic process cross-sectional views showing the main part manufacturing process of the semiconductor device of FIG. First, as shown in FIG. 20, a back gate 11b different from the MISFET transistor is formed in a region where the MISFET transistor is formed, for example, in an adjacent region. Next, in the same step as the gate step, for example, a gate insulating film 5b made of a silicon oxide film and a gate electrode 6b made of n-type polysilicon are formed, and this forms a MIS capacitor. This may be formed simultaneously with the step of forming the gate of the MISFET 1 (FIG. 20).

[0109]

Next, n + type and p + type semiconductor regions are formed near the gate electrode of the MIS capacitor. Specifically, in the ion implantation for forming the source / drain regions 7 of the n-type MISFET and the p-type MISFET, one side may be implanted into each MIS capacitor region (FIG. 21).

[0110]

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As the impurity concentration measurement using the CV method, there is also a method of obtaining it by a pn junction. FIG. 22 is a schematic cross-sectional view illustrating a semiconductor device provided with a dummy element for measuring an impurity concentration by a pn junction. That is, the n + type silicon region 14 is formed in the surface layer of the dummy region 4a which is adjacent to the FET 1 via the element isolation region 12. Using the pn junction formed in this way, the impurity concentration can be measured by the CV method to determine the back gate voltage required to realize the present invention. Here, a sufficiently large negative voltage VG2a is applied to the back gate 11c that faces the dummy region 4a via the insulating film 3 to bring the electronic state of the surface in contact with the insulating film 3 into an accumulated state.

[0111]

FIG. 23 is a schematic circuit diagram showing a specific example of the circuits 9d and 10b including the dummy element of FIG. The capacitance C in the circuit of FIG. 23 is the capacitance measured at the electrode 6b of FIG. The diode capacitance of the pn junction diode in the dummy region as shown in FIG. 22 changes depending on the fluctuation of the impurity concentration. When the capacitance C changes in this way, the frequency of the ring oscillator changes and can be fed back to the back gate voltage VG2. Here, when the capacity C is small, the pump frequency rises and VG2 rises. Of course, for example, a Schottky junction may be used instead of the pn junction.

[0112]

Next, a fifth specific example of the present invention will be described. FIG. 24 is a schematic sectional view of a semiconductor device according to the fifth example of the present invention. In the present embodiment, fully depleted transistors having two or more different threshold values are provided on the same substrate, and the threshold values of the respective transistors have the minimum threshold sensitivity to the film thickness variation. , And the threshold is set.

[0113]

Note that, in the specific example shown in FIG. 24, for convenience of description, a case where two fully depleted transistors having different film thicknesses and impurity concentrations of

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the channel region 4 are arranged in parallel is shown. However, they are formed on the insulator substrate 3. It does not necessarily have to be adjacent in the direction shown in FIG. 24, the same parts as those in FIG. 1 are designated by the same reference numerals, and detailed description thereof will be omitted.

[0114]

This embodiment includes fully depleted transistors 1A and 1B having at least two different threshold values on the same substrate. More specifically, for example, an SOI layer having a film thickness of about 20 nm to 0.1 μm, for example, a channel region 4A having a film thickness of 80 nm is formed on an insulating film 3 such as a silicon oxide film on a support substrate 2 made of silicon. And a channel region 4B of 60 nm are formed. The respective impurity concentrations are in the range of about $1 \times 10\ 16\ \mathrm{cm}^{-3}$ to $1 \times 10\ 19\ \mathrm{cm}^{-3}$, and for example, they have different impurity concentrations NAA and NAB of $1 \times 10\ 17\ \mathrm{cm}^{-3}$ and $1.6 \times 10\ 17\ \mathrm{cm}^{-3}$, respectively. Back gates 11A and 11B for applying different potentials to the respective MISFETs are formed on the support substrate 2 facing the SOI layer forming the MISFETs 1A and 1B with the insulating film 3 interposed therebetween. Further, control circuits 9A and 9B that set back gate voltages according to the impurity concentrations of the channel regions 4A and 4B are provided, and variable power sources 10A and 10B that are applied to the electrodes 11A and 11B are provided.

[0115]

Now, using the model described above with reference to FIG. 2, as illustrated in FIG. 6, the channel region in which the threshold sensitivity to variations in the SOI film thickness is almost the minimum and the threshold value is the set value. The optimum region of 4, that is, the design value is uniquely determined by the threshold value. That is, when the set threshold value is different, the optimum film thickness of the semiconductor layer for minimizing the sensitivity of the SOI film thickness variation of the threshold value is different.

[0116]

Using the calculation results shown in FIG. 6, when forming a fully depleted transistor in which two threshold voltage variations of 0.1 V and 0.2 V are minimal on the same substrate, the channel region 4 is The film thickness and the impurity concentration cannot be the same in two

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transistors, since it is necessary to form them with the film thicknesses of 80 nm and 60 nm and the impurity concentrations of 1.0 × 10 17 cm −3 and 1.6 × 10 17 cm −3, respectively. That is, by setting the SOI film thickness and the impurity concentration of each transistor to different values, it is possible to realize a transistor in which the threshold value is less likely to vary with variations in the SOI film thickness and the like. If the SOI film thickness is the same as in the conventional case, it is difficult to reduce the threshold sensitivity of each transistor.

[0117]

When the set threshold value of the FET 1A is smaller than the set threshold value of the FET 1B, the SOI film thickness (tsiA) of the FET 1A is large and the impurity concentration is high on the same substrate in order to minimize the threshold sensitivity of each. It is desirable to form the channel region 4A having a low (NAA) and the channel region 4B having a small SOI film thickness (tsiB) and a large impurity concentration (NAB).

[0118]

Further, it is desirable to provide a back gate electrode and a dummy element (not shown) capable of independently setting a potential in each of the plurality of regions having different thicknesses or impurity concentrations of the channel region as described above.

That is, the impurity concentration and the layer thickness of each channel region are measured using these dummy elements, the measurement result is fed back, and a predetermined back gate voltage is applied to each FET, thereby The threshold can be adjusted to the desired value. As the dummy element for this purpose, for example, the one illustrated in FIG. 9, FIG. 15, FIG. 18, or FIG. 22 can be used. Further, as the circuit for measurement and the circuit for applying the back gate voltage, various circuits exemplified in the present specification can be used.

[0119]

Further, this embodiment can be used also when the n-type MISFET and the p-type MISFET are formed on the same substrate. That is, for example, an n-type MISFET may be used as the FET 1A shown in FIG. 24, and a p-type MISFET may be used as the FET 1B. Normally, the work function difference between the gate electrode and the substrate and the charge at the interface of the gate insulating film are different between the n-type MISFET and the p-type MISFET, and therefore the absolute value ¦ VFB ¦ of the flat band voltage is also different. Therefore, even if

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the same threshold value is set, the n-type MISFET and the p-type MISFET also have different SOI film thicknesses for minimizing the threshold sensitivity with respect to variations in the SOI film thickness. That is, as illustrated in FIG. 24, the threshold sensitivity can be kept small by using the optimum SOI film thickness for each of the transistors FET1A and FET1B.

[0120]

Next, a method of manufacturing the semiconductor device of FIG. 24 will be described. FIG. 25 is a schematic process cross-sectional view showing a main part manufacturing process of the semiconductor device of FIG. In forming this structure, as shown in FIG. 25A, the back gates 11A and 11B can be applied to the SOI substrate by lithography and ion implantation, and different potentials can be applied to the respective MISFETs. Form. The SOI layer on the insulating film 3 is thinned by polishing, dry etching, or wet etching, and has a film thickness of, for example, 80 nm and boron (B) ions are implanted to obtain an impurity concentration of, for example, 1×10 17 cm -3. The SOI layer 4 is formed. Next, a resist mask 15 is formed and etching is performed to form a channel region 4B having a film thickness of 60 nm, for example. Subsequently, for example, boron (B) is ion-implanted into the channel region 4B so that the impurity concentration NAB in this region is set to, for example, 1.6×10 17 cm -3.

[0121]

Then, by performing steps after the gate step (not shown), the fully depleted transistors FET1A and FET1B can be formed on the same substrate. Further, a dummy element (not shown) is appropriately formed corresponding to each channel region. Further, circuits 9A and 9B that control the back gate voltage according to the impurity concentration of the SOI layer forming the MISFET are provided, and variable power supplies 10A and 10B that are applied to the back gates 11A and 11B, respectively, are installed to complete the semiconductor device. To do.

[0122]

Next, a sixth specific example of the present invention will be described.

[0123]

FIG. 26 is a schematic sectional view of a semiconductor device according to the sixth example of

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the present invention.

This specific example is characterized in that the FET 1 is formed in the thin SOI layer and the dummy element for measuring the impurity concentration is formed in the thick SOI layer.

[0124]

This dummy element has a pn junction and can measure the impurity concentration using the CV method. The structure and the details of the measuring method can be the same as those described above with reference to FIG. When forming a pn junction in a thin SOI layer, it is not easy to control the junction position, and the p-type layer may be lost due to penetration of phosphorus (P) or arsenic (As) that is ion-implanted. In addition, the depletion layer of the p-type layer may extend to the back gate region and NA may not be measured. On the other hand, according to this example, since the pn junction can be formed in the region where the film thickness of the SOI layer is thick, the formation is much easier and the region of the p-type layer can be secured. There are advantages.

[0125]

The outline of the manufacturing process is as follows. First, for example, an SOI layer made of a p-type silicon layer having a film thickness of 80 nm and an impurity concentration of 1 × 10 17 cm −3 is formed. Next, by patterning and etching, the film thickness of the SOI layer in the portion where the transistor is formed is set to 60 nm, for example. Next, boron (B) or the like is ion-implanted so that the impurity concentration of these SOI layers becomes, for example, 1.6 × 10 17 cm −3. Further, steps after the gate step are performed in the region where the MISFET is formed.

[0126]

Next, as shown in FIG. 27, a pn junction is formed by ion-implanting phosphorus (P), for example, into a region where a dummy element is to be formed. This ion implantation step can also serve as the step of forming the source / drain regions 7 of the n-type MISFET. Here, as a method using the SOI regions having different film thicknesses as illustrated in FIGS. 24 and 26, LOCOS (Local Oxidation of Silicon) sacrificial oxidation may be used. FIG. 28 is a process cross-sectional view

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illustrating a technique of forming an SOI region having a small film thickness by using a recess structure by LOCOS sacrificial oxidation. In this method, first, a silicon oxide film 14 is formed on the SOI layer 4a, and a film 20 made of, for example, a silicon nitride film is deposited on the entire surface thereof. Then, as shown in FIG. 28A, the silicon nitride film 20 is opened in the channel region to be thinned. Then, the SOI layer in the opened region is ion-implanted and heat-treated to obtain a predetermined impurity concentration.

[0127]

Next, as shown in FIG. 28B, the surface layer is thermally oxidized until the film thickness of the SOI layer in the opened region is reduced to a predetermined value. Then, by peeling off the silicon nitride film 20 and the silicon oxide film 14, an SOI region having a small film thickness and a predetermined impurity concentration can be formed. After that, the semiconductor device can be completed by carrying out steps after the gate forming step (not shown).

[0128]

Here, the recess structure by LOCOS sacrificial oxidation has been described for thinning the channel portion of the SOI layer. However, in addition to this, as shown in FIG. 29, the SOI layer in the channel region may be formed by a concave structure in which it is thinned by lithography and etching.

[0129]

Next, a seventh specific example of the present invention will be described. In each of the specific examples described above, in order to have a desired threshold value and reduce the fluctuation of the threshold value due to the process variation, the impurity concentration or the carrier concentration is formed on the same substrate on which the fully depleted transistor is formed. The technique has been described in which the measurement dummy element for measuring the voltage and the control circuit for setting the back gate voltage according to the impurity concentration or the carrier concentration measured by the measurement dummy element are provided. On the other hand, in this example, a semiconductor device provided with a storage element in which the impurity concentration or the carrier concentration is measured in advance by a measurement dummy element and the value is stored is realized.

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[0130]

FIG. 30 is a cross-sectional view of essential parts of a semiconductor device according to this example. In addition, FIG. 31 is a functional block diagram illustrating the relationship between the components in the present specific example. In the figure, the same parts as those in the above-described specific examples are designated by the same reference numerals, and detailed description thereof will be omitted. Also in this specific example, the SOI film thickness and the channel region 4 having the impurity concentration or the carrier concentration (for example, FIG. 6) set so that the threshold sensitivity is reduced with respect to a desired threshold value and the back surface. A fully depleted transistor FET1 consisting of a gate 11 is provided. Further, this specific example has a storage element for storing the information of the impurity concentration or the carrier concentration for setting the back gate voltage applied to the back gate 11. This memory element includes, for example, fuses F1, F2, and F3 formed of wiring layers made of polysilicon, amorphous silicon, aluminum (Al), copper (Cu), platinum silicide (PtSi), titanium silicide (TiSi), or the like. It is characterized by having.

[0131]

32 to 34 are cross-sectional views for explaining the manufacturing process of the semiconductor device of FIG. That is, also in the present specific example, as shown in FIG. 32, the measurement dummy element is provided during the manufacturing process. As shown in FIG. 9, this dummy element measures the impurity concentration or carrier concentration from the resistivity ρ of the SOI layer.

[0132]

Next, as shown in FIG. 33, the impurity concentration or the carrier concentration of the channel region 4 is measured using the measurement dummy element. Then, based on this measured value, the back gate voltage required for a desired threshold value is determined and stored in the storage element. That is, the fuse is blown to create the required back gate voltage. Here, the measurement dummy element does not necessarily have to be formed for each FET 1. For example, the element area can be reduced by forming one measurement dummy element for a plurality of FETs having a common threshold value. More specifically, one measurement dummy element may be provided for a semiconductor device having an integrated circuit in which a plurality of FETs are formed, or one measurement dummy element for a wafer on which a

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plurality of such semiconductor devices are formed. Dummy elements may be provided. Further, when a plurality of these wafers are batch processed, if the variation between the wafers is small, the measurement dummy element may be provided only on any one of the wafers.

[0133]

Once the impurity concentration or the carrier concentration of the channel region 4 is measured and the required back gate voltage is determined based on the relationship shown in FIG. 6, the measurement dummy element becomes unnecessary. Therefore, as shown in FIG. 34, the FET 1 and the measurement dummy element can be separated in a dicing process for chip formation, for example.

[0134]

According to this example, it is not necessary to form a circuit for measuring the impurity concentration or the carrier concentration on the finally obtained chip, and it suffices to store the circuit in a memory element having a much smaller size. Therefore, high integration and reduction in chip area can be achieved. Further, since the impurity concentration or carrier concentration measuring circuit is unnecessary, it is possible to further reduce power consumption.

[0135]

Here, the measurement of the impurity concentration or the carrier concentration in the channel region is not limited to the measurement dummy element shown in FIG. 32, and any method described in each of the above-described specific examples can be used as well.

[0136]

In addition, this specific example can be applied to a semiconductor device in which a plurality of different FETs as illustrated in FIG. 24 are formed.

That is, when a plurality of types of MISFETs having different layer thicknesses and impurity concentrations of the channel region are formed, a storage element is provided for each type of

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FET, and the measurement result of the dummy element is fed back and optimized. It is possible to apply various back gate voltages.

[0137]
Next, a specific configuration of the bias circuit used in this example is illustrated.

[0138]
35 to 40 show a configuration example of a bias circuit including a memory element that can be used in this example.

[0139]
In FIG. 35, the range in which the impurity concentration or the carrier concentration varies in the channel region 4 is predicted in advance, and the optimum back gate voltage corresponding to each predicted value is set as, for example, VG1, VG2, VG3, This is an example in which the fuse of the memory element is blown accordingly.

[0140]

This will be specifically described with reference to the graph of the relationship between the SOI film thickness and the impurity concentration in FIG.

First, the desired threshold value is set to 0.2 V, and the impurity concentration varies within the range of 1.2 × 10 17 cm −3 to 1.8 × 10 17 cm −3, for example.

At this time, for example, -1, 0, 1V are provided as VG1, VG2, and VG3 as the power supply for the back gate voltage.

Next, the impurity concentration of the channel region 4 is measured using a dummy element, and when the measured value is 1.2 × 10 17 cm −3 to 1.4 × 10 17 cm −3, the memory element F1 is not cut., F2 and F3 are cut off to apply VG1 = -1V as a back gate voltage. When the measured value is 1.4.times.10@17 cm @ -3 to 1.6.times.10@17 cm @ -3, F2 is not cut and F1 and F3 are cut to apply VG2 = 0V as the back gate voltage. Further, when the measured value is 1.6 × 10 17 cm −3 to 1.8 × 10 17 cm −3, F3 is not cut and F1 and F2 are cut so that VG3 =

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1V is applied as the back gate voltage. Cut each fuse. By doing so, it is possible to apply a back gate voltage within a desired range based on the measured value, and a threshold value close to the desired threshold value can be obtained.

[0141]

FIG. 36 shows an example in which the power supplies VG1 to VG3 in FIG. 35 are replaced with a step-up / down circuit. This is convenient in that it can appropriately step up or step down to a predetermined back gate voltage based on the conventionally used power supply voltage.

[0142]

FIG. 37 shows an example in which the voltage is appropriately divided within the voltage range of Vcc to Vss from Vcc = 3V which is the power supply voltage to Vss = 0V and used as the back gate voltage. For example, a resistor composed of a resistor R is connected in series, and a fuse is wired so that a voltage can be extracted at each terminal. When the back gate voltage is applied, for example, the fuse F2 is not cut, F1 and F3 are cut to 2/3 Vcc, and F3 is not cut and F1 and F2 are cut to 1/3 Vcc. By disconnecting all fuses, the voltage of Vcc can be applied to the back gate. Although three resistors are provided in FIG. 37, a plurality of resistors may be provided, and if more resistors are provided, the voltage is divided more finely and a value close to a desired threshold value is obtained. You can The range of voltage is not limited to the range of Vcc to Vss, and it is possible to change the range by using a step-up / down circuit.

[0143]
FIG. 38 is a modification of FIG. 37, and is a circuit example in which the voltage range from Vcc to Vss can be divided by using n cells each including two resistors and one fuse. ..

[0144]

Further, as shown in FIG. 37, in addition to directly applying the output of the resistor to the substrate bias node, as shown in FIG. 39, the resistor output may be connected to a variable power source whose output voltage changes according to the control input. ..

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By doing so, there is an advantage that a large substrate bias output current can be obtained even if the current flowing through the resistor is reduced.

[0145]

Further, as shown in FIG. 40, a plurality of charge pump circuits may be connected in series and the substrate bias voltage may be switched depending on the states of the fuses F1 to F3 of the memory element. Assuming that the threshold value of the transistor is Vt, the open circuit voltage of the substrate bias power supply output is -3Vcc + 4Vt when F1, F2 and F3 are not disconnected, and -2Vcc + 4Vt and F1 are not connected when F1 and F2 are disconnected. An output of -Vcc + 4Vt can be obtained at the time of disconnection, F2 and F3 disconnection.

[0146]

As the memory element used in this example, in addition to the method of cutting the fuse as described above, for example, a method of accumulating charges in the floating gate electrode, a method of polarizing and storing a ferroelectric substance, and Alternatively, a so-called antifuse may be used, which is a method of storing data by dielectric breakdown of a thin semiconductor or an insulator sandwiched between a metal or a silicide.

[0147]

The embodiments of the present invention have been described above by exemplifying specific examples.

However, the present invention is not limited to the above specific examples.

[0148]

For example, as an insulating film forming method, an oxide film forming method by thermal oxidation, a method of forming an oxide film into which oxygen is injected with low acceleration energy of about 30 keV, a method of depositing a silicon oxide film, A method of depositing a silicon nitride film or a method of combining these may be used. Further, a method other than these methods for converting silicon into a silicon oxide film or a silicon nitride film, for example,

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a method of implanting oxygen ions into deposited silicon or a method of oxidizing deposited silicon may be used. In addition, a silicon nitride film or other tantalum oxide film, a titanium oxide film, a ferroelectric film such as strontium titanate or barium titanate, or lead zirconium titanate, a single-layer film of a paraelectric film, or a film thereof Composite membranes can also be used.

[0149]
Further, although not particularly mentioned in the above-mentioned specific examples, as the element isolation, element isolation of trench isolation, LOCOS element isolation film, recessed type (Recessed) LOCOS, improved LOCOS method, or field shield isolation is used. Or a combination of these.

[0150]

Furthermore, although p-type Si is used for the SOI layer in each of the above-described specific examples, n-type Si, GaAs, or InP may be used instead.

Further, it may be applied to a p-type MISFET instead of the n-type MISFET. In that case, the n-type in the above-described embodiment is read as p-type and the p-type is read as n-type, and the doping impurity species As, P and Sb are used. Etc. may be read as either In, B or the like, and As, P, Sb may be read as any of In, B, BF2 in the case of ion implantation.

[0151]

Further, the gate electrode is made of single crystal silicon other than polycrystalline silicon, porous silicon, amorphous silicon, SiGe mixed crystal, SiC mixed crystal, GaAs, W, Ta, Ti, Hf, Co, Pt, Pd metal. Alternatively, silicide can be used. Further, a laminated structure of these may be used.

[0152]
In addition, various modifications can be made without departing from the spirit of the present invention.

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[0153]
The present invention is carried out in the form described above, and has the following effects.

[0154]
First, according to the present invention, the threshold value can be set to a desired value while keeping the threshold sensitivity to the variation of the SOI film thickness and the impurity concentration, which is a problem in the fully depleted transistor, at a minimum. Is.

[0155]
Further, according to the present invention, for example, when an integrated circuit is formed, the variation of the impurity concentration is corrected, and the threshold sensitivity to the variation of the SOI film thickness is smaller than that of the conventional example. Can be accumulated.

[0156]

On the other hand, in the MOS logic circuit, when the threshold value of the transistor is high, the current driving capability is low and the delay time is long, while when the threshold value is low, the subthreshold leak current when off is large.

Therefore, according to the present invention, variations in delay time and power consumption can be kept small.

[0157]

Further, the delay time is proportional to (VDD-Vth) - α (α is a positive number of 1 or more), where VDD is the power supply voltage, with respect to the threshold value Vth.

Therefore, the delay time can be reduced by the variation of Vth, and the low voltage operation can be performed even if the delay time is the same.

Therefore, by operating at a low voltage, the reliability of the gate insulating film with respect to

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the power supply voltage can be further improved, and the power consumption for gate charge / discharge can be reduced.

[0158]
Further, according to the present invention, even when the recess gate structure is formed by LOCOS sacrificial oxidation, the SOI film thickness is set so that the threshold sensitivity becomes minimum with respect to the variation of the SOI film thickness at a desired threshold value. By doing so, the fluctuation of the threshold value near the SOI film thickness is minimized, so that a desired threshold value can be obtained.

[0159]

Further, since the variation in the threshold value between the pair transistors can be further suppressed, for example, a current mirror circuit or a cross-coupled sense amplifier can be realized more accurately and symmetrically, and the accuracy of the current source and the sensitivity of the sense amplifier can be improved. Can be increased.

Further, according to the present invention, in a semiconductor circuit in which MISFETs having two or more threshold values are integrated, the threshold sensitivity to variations in SOI film thickness can be minimized for each element.

This is because even in the CMOS circuit, in the fully depleted MISFET formed with the SOI film thickness corresponding to the desired threshold value of the n-type MISFET and the p-type MISFET, the threshold caused by the SOI film thickness variation in each MISFET. Value sensitivity is minimal. This is difficult for the conventional FD-SOIMISFET having a single SOI film thickness. Therefore, in a logic circuit using a transistor having a plurality of threshold values or a CMOS circuit, even if the SOI film thickness varies, the threshold sensitivity can be kept to a minimum at each desired threshold value. Further, according to the present invention, the back gate voltage control circuit according to the impurity concentration can be formed on the same substrate by applying a half-Vdd circuit or a substrate bias circuit.

[0160]

Further, in the present invention, the method of obtaining the impurity concentration of the

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semiconductor layer forming the MISFET by measuring the resistance can be performed at a low voltage by the method of measuring the capacitance of the capacitance, and the applied voltage due to the breakdown voltage of the gate oxide film can be changed. It has the advantage that there are no limits. On the other hand, the method of obtaining the impurity concentration by measuring the capacitance of the capacitance has the advantages that the sensitivity is higher than the method of measuring the resistance and the power consumption can be reduced.

[0161]
Further, when manufacturing the dummy element of the present invention, the gate used for the MISFET can be used as it is, so that the dummy element for measuring the impurity concentration can be formed on the same substrate by the number of steps of the conventional semiconductor device. ..

[0162]

Further, according to the present invention, a dummy element for measuring the impurity concentration of a semiconductor layer having a thin SOI film thickness is formed in a semiconductor layer region having a large SOI film thickness to form a pn junction of the dummy element. The film thickness margin can be secured.

Then, for example, when the n-type layer is formed in the p-type semiconductor layer by ion implantation to form the pn junction region, the lithography process is performed at the same time as the ion implantation for forming the source / drain electrode region in the n-type MISFET. Up to this, it is possible to form a pn junction region.

[0163]
As described above, according to the present invention, in a semiconductor device having a fully depleted transistor, a desired threshold value is maintained while the threshold sensitivity to variations in SOI film thickness and impurity concentration is kept at a minimum. The industrial advantages are enormous.

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CLAIMS JPH11330482

1.
A support substrate having a back gate formed thereon, an insulating film provided on the support substrate, a first semiconductor layer provided on the insulating film, and the support substrate facing the back gate. A MISFET transistor using a part of the first semiconductor layer as a channel region, a dummy element that outputs a measurement signal that changes according to the impurity concentration or the carrier concentration of the first semiconductor layer, and the dummy element that outputs the measurement signal. A semiconductor device comprising: a voltage applying unit that applies a voltage to the back gate according to the measurement signal.

2.
A supporting substrate formed with first and second back gates, an insulating film provided on the supporting substrate, and a first semiconductor layer having a first film thickness provided on the insulating film, The first MISFET transistor having a part of the first semiconductor layer as a channel region facing the first back gate of the supporting substrate and the first film thickness provided on the insulating film are A second semiconductor layer having a different second film thickness; a second MISFET transistor facing the second back gate of the support substrate and having a part of the second semiconductor layer as a channel region; A semiconductor device comprising: a voltage applying unit that applies a voltage to the first back gate independently of a voltage of the second back gate.

3.
A support substrate having a back gate formed thereon, an insulating film provided on the

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support substrate, a first semiconductor layer provided on the insulating film, and the support substrate facing the back gate of the support substrate. A MISFET transistor using a part of the first semiconductor layer as a channel region, a storage element that stores information corresponding to a voltage applied to the back gate, and the back gate based on the information stored in the storage element A semiconductor device comprising: a voltage applying unit that applies a voltage to the.

4.

A supporting substrate having first and second back gates formed thereon, an insulating film provided on the supporting substrate, and a first semiconductor layer having a first film thickness provided on the insulating film, Information corresponding to a first MISFET transistor in which a part of the first semiconductor layer is a channel region facing the first back gate of the support substrate and information corresponding to a voltage applied to the first back gate is provided. A first memory element for storing, a second semiconductor layer provided on the insulating film and having a second film thickness different from the first film thickness, and a second back gate of the support substrate. A second MISFET transistor, which opposes and uses a part of the second semiconductor layer as a channel region, and a voltage of the second back gate are independent of the information stored in the first storage element. And a voltage applying unit that applies a voltage to the first back gate based on the semiconductor device.

5.

The semiconductor device according to claim 3, wherein the storage element stores information according to an impurity concentration or a carrier concentration of the first semiconductor layer.

6.

The semiconductor device according to claim 1, wherein the MISFET transistor is a fully depleted transistor in which the channel region is completely depleted.

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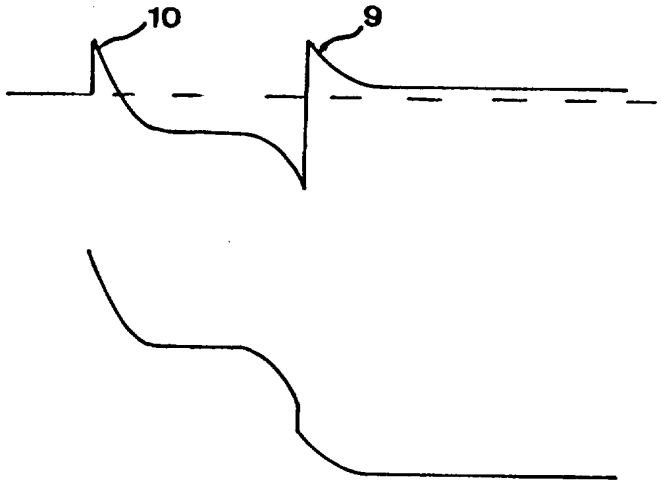
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(54) Title: A SEMICONDUCTOR DEVICE WITH A LOW RESISTANCE OHMIC CONTACT BETWEEN A METAL LAYER AND A SiC-LAYER

(57) Abstract

A semiconductor device comprises a semiconductor layer (1) of SiC, a metal layer (2) adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer (3) of a material having a smaller bandgap than the SiC of the SiC-layer placed between the SiC-layer and the metal layer. The SiC-layer is at least in the region next to said thin layer highly doped. The material of said thin layer is a Group 3B-nitride.



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A semiconductor device with a low resistance ohmic contact between a metal layer and a SiC-layer

Technical field of the invention and prior art

The present invention relates to a semiconductor device comprising a semiconductor layer of SiC, a metal layer adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer of a material having a smaller band gap than the SiC of the SiC-layer and placed between the SiC-layer and the metal layer, said SiC-layer being at least in the region next to said thin layer highly doped.

All types of semiconductor devices in which a contact between a metal layer and a SiC-layer is to be formed are comprised, such as for example different types of diodes, transistors and thyristors. Due to the characteristics of SiC such devices are often high power devices.

SiC is a semiconductor material having a large band gap, the magnitude of which is between 2,3 and 3,3 eV dependent on the polytype in question, i.e. the gap between the valence band and the conduction band. For this reason SiC has, in common with other wide band gap semiconductors, the problem that it is extremely difficult to form low resistance ohmic contacts on SiC. One reason for this difficulty is the large difference between the work function of the metal of such a metal layer and the electron affinity of the semiconductor, which results in a large Schottky-barrier height. It has been tried to solve this problem by making a heterojunction

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contact, whereby a material having a lower band gap is grown as an intermediate layer between the metal layer and the wide band gap semiconductor as defined above and as described in U.S. patent 3 984 261. Accordingly, the definition "a metal layer adapted to form a low resistance ohmic contact with the SiC-layer" is to be interpreted broadly and it expresses that there shall be formed a low resistance ohmic contact between a metal layer and a SiC-layer, but this may be done by interposing a thin layer of another material.

The European patent B1 0 249 777 describes how such a heterojunction is used for obtaining a low resistance ohmic contact between a semiconductor material and a metal layer, but the semiconductor is not SiC, but a III-V-material, for instance GaP, which has a considerably lower band gap than SiC.

A known semiconductor device according to the introduction has been suggested (V.A. Dimitriev, K. Irvine, M. Spencer and G. Kelner Appl. Phys. Lett. vol. 64(3) p. 318 (1994)) for 6H SiC, while using the polytype 3C SiC as an intermediate layer, but the disadvantage of this is that the polytype 3C is still a relatively wide band gap material and the contact problem is thus not solved.

Another problem of different materials used so far as intermediate layers in such heterojunctions and also as semiconductors making a direct contact with a metal layer is that the Fermi-level of these materials is pinned as a result of a high density of traps within the band gap of the semiconductor. Typically pinning is due to deep states (traps) and therefore the Fermi-level resides close to the centre of the band gap of the material. These states are for example formed by the deposition of the metal. The pinning is for a narrow region only, in this case the interface between the metal layer and the semiconductor, so that the Fermi-level

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is not "pinned" in the bulk of the semiconductor. Pinning is defined as the phenomena such that the Fermi-energy of the semiconductor is in this single location, i.e. at said interface, fixed at a single energy (the trap energy) independent of the doping condition in the semiconductor. This effect is typically seen between a metal and a semiconductor, for example the III-V compounds, such as GaAs, and results in a large barrier height. It is not observed at the heterojunction between semiconductors provided the interface is of good quality, i.e. of low trap density, and it would accordingly not be present between the SiC-layer and said thin layer in the device defined in the introduction. Normally, it is desired that the work function of the metal in question is matched with the electron affinity of the semiconductor for making a low resistance ohmic contact, but due to said pinning the midgap states in the semiconductor will determine the height of the Schottky-barrier independent of the work function of the metal. This "pinning" phenomena is also there in the semiconductor device according to the European patent B1 0 249 777, but this phenomena is of minor importance, since the band gap of the semiconductors used there is very narrow.

Summary of the invention

The object of the present invention is to provide a semiconductor device according to the introduction, which has an excellent low resistance ohmic contact between the SiC-layer and the metal layer.

This object is in accordance with the invention obtained by making said thin layer of a Group 3B-nitride.

Thus, it has been realised that Group 3B-nitrides do not have pinned (fixed) Fermi-levels at the interface with a metal, which means that the work function of the metal will

determine the Schottky-barrier height, so that it will be possible to choose a suitable metal for a low barrier. Thus, it is possible to form a low resistance ohmic contact between the SiC-layer and a metal layer by choosing a Group 3B-nitride having a smaller bandgap than the SiC of the SiC-layer as a thin layer between the metal layer and the SiC layer. Thanks to the fact that the SiC-layer is highly doped at least in the region next to said thin layer the thin layer may be undoped, since there will due to "modulation doping" be a transfer of charge from the SiC layer having a large band gap to the thin layer having a narrower band gap, so that the narrow band gap material has an excess of charge in the conduction band thereof and will in fact behave as a metal, so that a low resistance ohmic contact may be established without any doping in advance of said thin layer. This means that it will be easier to grow said thin layer of a high quality. Furthermore, it is important that the heterojunction of the device has a high quality so as to avoid traps, i.e. mid gap states, there, and this is obtained thanks to the comparatively good lattice match of the Group 3B-nitrides with SiC.

According to a preferred embodiment of the invention said Group 3B-nitride comprises a content of indium and at least another Group 3B-element. Indium is a suitable element for making the band gap of the Group 3B-nitride narrower than that of SiC of any polytype, so that it is very advantageous to have such content in said Group 3B-nitride. However, it is for the ease of the growth of a high quality thin layer of importance that it also contains at least another Group 3B-element besides indium.

According to another preferred embodiment of the invention said Group 3B-nitride has a content of at least indium and gallium. GaN has a larger band gap than SiC, but it may be easily grown on SiC and thanks to the addition of indium the

band gap is made narrower, so that said Group 3B-nitride may be suited for forming a low resistance ohmic contact aimed at.

According to another preferred embodiment of the invention said Group 3B-nitride is $Ga_{1-x}In_xN$. Such a material for said thin layer has been found to be easy to grow on SiC, have a smaller band gap than SiC and have a not pinned Fermi-level at the interface with a metal.

According to a very preferred embodiment of the invention the indium content of the Group 3B-nitride is adjusted to the metal chosen for matching the electron affinity of said material with the work function of the metal of said metal layer. Thus, the indium content is a parameter easy to handle to adjust the electron affinity of the Group 3B-nitride for matching the work function of the metal of said metal layer for reducing the barrier height of said ohmic contact between the metal layer and said thin layer.

According to a still further, also very preferred embodiment of the invention the indium content of said Group 3B-nitride is adjusted according to the type of doping, p or n, of said SiC-layer. In this way the indium content will be a parameter to adjust the band-alingement according to whether you want a p- or n-type contact. The other Group 3B-element of said Group 3B-nitride may namely have a gap between the conduction band and the valence band which is not centered with respect to the band gap of the SiC of said SiC-layer, so that different concentrations of indium in said Group 3B-nitride may be appropriate depending on the type of doping of the SiC-layer close to the interface to said thin layer. For instance, it is believed that GaN has a band gap centre being displaced with respect to the band gap centre of SiC, which means that different indium-contents may be needed for p- and n-doped SiC-layers.

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According to another preferred embodiment of the invention said thin layer is undoped. The advantages thereof has already been presented above, and the possibility to make this layer undoped is provided by the fact that a modulation doping process takes place thanks to the high doping of the SiC next to said thin layer, the smaller band gap of the thin layer and the fact that the layer really is thin.

Further advantages and preferred features of the invention will appear from the following description and the other dependent claims.

Brief description of the drawings

With reference to the appended drawings, below follows a specific description of a preferred embodiment of the invention cited as an example.

In the drawings:

Fig. 1 is a view illustrating how the extension of the conduction band and the valence band would be in a semiconductor device of the invention from a SiC-layer, a thin Group 3B-nitride layer and a metal layer at a contact of said device if the different layers would not have any influence on each other, and

Fig. 2 is a view corresponding to Fig. 1 but illustrating the real extension of said conduction and valence bands at said contact of the semiconductor device.

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Detailed description of a preferred embodiment of the invention

Fig. 1 illustrates a low resistance ohmic contact between a SiC-layer 1 and a metal layer 2 with an intermediate thin layer 3 of a Group 3B-nitride in a semiconductor device. The SiC-layer is a mono-crystalline layer of SiC of any polytype. The Group 3B-nitride is in the present case $Ga_{1-x}In_xN$, in which x is chosen to obtain a smaller bandgap of the Group 3B-nitride than the SiC of the SiC-layer 1 and for obtaining an electron affinity of the Group 3B-nitride matching the work function of the metal selected for said metal layer. The semiconductor device in question may be of any type, such as an IGBT, a GTO and a rectifying diode.

In this way two junctions are formed, a first heterojunction 4 between the SiC-layer 1 and said thin layer 3 and a second junction 5 between the thin layer and the metal layer. The SiC-layer 1 is highly doped with donors at least close to the heterojunction 4, but it would also be possible to highly dope it with acceptors. Highly doped does here mean that the concentration of dopants exceeds 10^{17}, preferably exceeding 10^{18} cm^{-3}. It is very schematically illustrated that the energy gap between the valence band 6 and the conduction band 7 is larger in the SiC layer 1 than in said thin layer 3. In this way a band-offset is obtained at said heterojunction 4. Since the SiC-layer is highly doped with donors these have their extra electrons 8 at a higher energy level than the conduction band level at the other side of the heterojunction, which will result in a fall of said electrons as indicated by the arrow to the lower energy level in said thin layer 3 while ionising said donors and leaving a positive charge 9 in the SiC-layer 1. This technique of providing only the layer with the largest band gap with impurities is called selective doping or modulation doping. In this way an electrical field is created at the

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heterojunction bending the conduction bands in the way shown in Fig. 2. The higher the concentration of donors in the first layer comparatively close to the heterojunction the sharper will the conduction band be bent. Thanks to the high concentration of dopants in the SiC-layer a very narrow barrier 9 will in this way be established between the SiC-layer and said thin layer 3, so that electrons may easily tunnel through this barrier and the resistance of this heterojunction will be neglectable.

The thin layer 3 may be undoped, since the conduction band thereof will in this way by the modulation doping process be filled with electrons, so that this thin layer will act as a metal and have a very low resistance. It would however also be possible to dope the thin layer 3 with the dopant type corresponding to that of the SiC-layer, thus in the case shown in the figures with donors. The layer 3 has to be thin for obtaining this metal behaviour thereof, and thin will in this embodiment mean a thickness below 300Å and in some applications below 100Å. The thin layer 3 is preferably monocrystalline, but it may also be poly-crystalline and still work depending on the influence of the grain boundary.

The Fermi-levels of the different layers have, as known, to be at the same level, which will result in an extension of the conduction band and the valence band in accordance with Fig. 2. It has been found that the Fermi-level of a Group 3B-nitride is not pinned, i.e. fixed, at the interface to a metal, which means that there are relatively few mid gap states (traps) at said interface, which would change the position of the Fermi-level of said thin layer there, so that the barrier 10 then would be much higher. Accordingly, a low resistance ohmic contact between a SiC-layer and a metal layer may be achieved by selecting a Group 3B-nitride as a material for a thin layer between the SiC-layer and the metal layer.

As already mentioned above the mole fraction of In incorporated in said thin layer 3 can be varied to tune the band offset with respect to both the SiC-layer 1 and the metal layer 2. The higher the content of In in the Group 3B-nitride the smaller will the band gap thereof be. GaN has a band gap being slightly larger than most polytypes of SiC and a content of indium therein will reduce this band gap. The band gap of GaN is not centered with respect to the band gap of SiC, so that it will be suitable to choose different concentrations of indium in said Group 3B-nitride according to the type of doping, p or n, of the SiC-layer. Thus, the indium content may vary according to certain considerations, and it will typically be between 5 and 20% of the N content.

A contact of this type may be easily produced by forming the highly doped SiC-layer 1 either by epitaxial growth (CVD, MBE etc.) or by ion implantation. The Group 3B-nitride layer 3 should be of high quality single crystal and should again be grown using an epitaxial technique (CVD, MBE, magnetron sputtering, etc.). Following the deposition of the Group 3B-nitride a metal layer 2 should be deposited by any of the available techniques, said metal being chosen to give a good contact to the Group 3B-nitride. Finally, the layers are patterned using lithography to cover only those areas where a contact is required. The annealing temperature should be low, which means below 1000°C, but in most cases it may be considerably lower. The possibility to not dope said thin layer but nevertheless obtain a low resistance ohmic contact simplifies the production of this contact.

The invention is of course not in any way restricted to the preferred embodiments described above, but many possibilities to modifications thereof will be apparent to a man with ordinary skill in the art.

All definitions concerning the materials of the different device layers do of course include inevitable impurities as well as intentional doping of the layers in question.

The definition layer is to be interpreted broadly and comprises all types of volume extensions and shapes.

Other Group 3B-nitrides than GaInN are also conceivable, such as AlInN, in which case the In-content has to be comparatively high, since AlN has a much higher bandgap than SiC.

The SiC-layer may be of any polytype of SiC, such as for example 6H, 4H, 3C and 15R.

Claims

1. A semiconductor device comprising a semiconductor layer (1) of SiC, a metal layer (2) adapted to form a low resistance ohmic contact with the SiC-layer and a thin layer (3) of a material having a smaller bandgap than the SiC of the SiC-layer and placed between the SiC-layer and the metal layer, said SiC-layer being at least in the region next to said thin layer highly doped, **characterized** in that the material of said thin layer is a Group 3B-nitride.

2. A device according to claim 1, **characterized** in that said Group 3B-nitride comprises a content of indium and at least another Group 3B-element.

3. A device according to claim 2, **characterized** in that said Group 3B-nitride has a content of at least indium and gallium.

4. A device according to claim 3, **characterized** in that said Group 3B-nitride is $Ga_{1-x}In_xN$.

5. A device according to any of claims 2-4, **characterized** in that the indium content of the Group 3B-nitride is adjusted to the metal chosen for matching the electron affinity of said material with the work function of the metal of said metal layer.

6. A device according to any of claims 2-4, **characterized** in that the indium content of said Group 3B-nitride is adjusted according to the type of doping, p or n, of said SiC-layer (1).

7. A device according to any of claims 1-6, **characterized** in that said thin layer (3) is undoped.

8. A device according to any of claims 1-7, **characterized** in that said thin layer (3) has a thickness below 300 Å.

9. A device according to any of claims 1-8, **characterized** in that said thin layer (3) is a mono-crystalline layer.

10. A device according to any of claims 1-9, **characterized** in that highly doped means a concentration of dopants exceeding 10^{18} cm^{-3}.

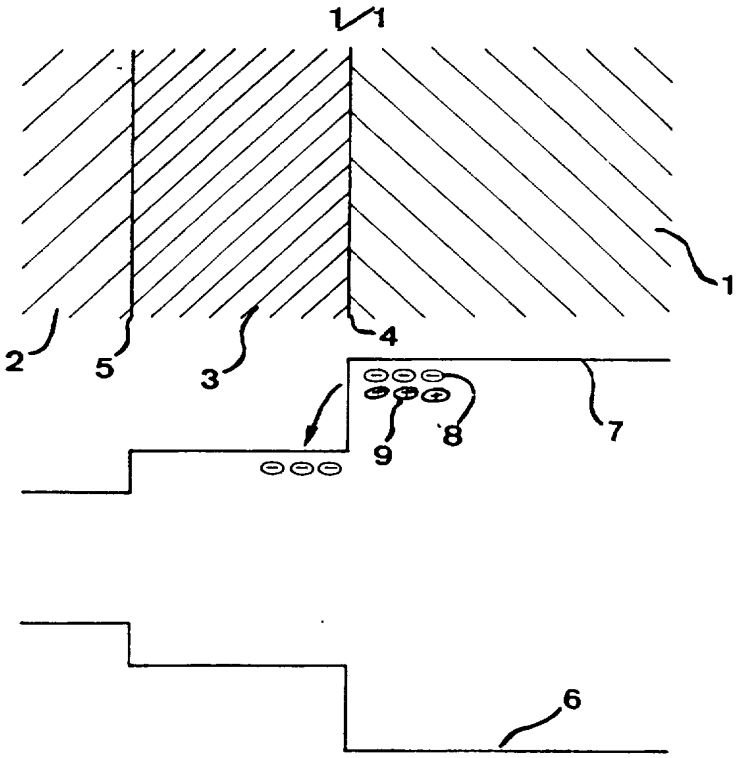


Fig 1

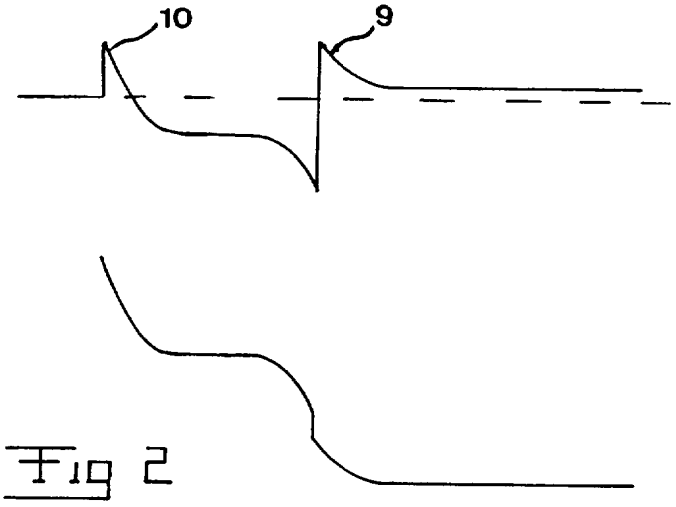


Fig 2

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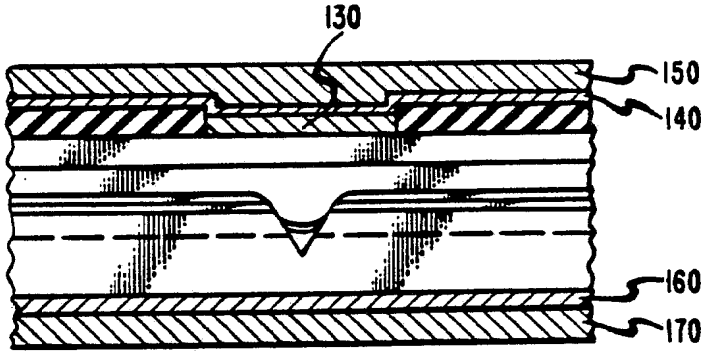
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(57) Abstract

New technique for forming non-rectifying electrical contacts to III-V semiconductor materials, without the use of dopants or of an alloying procedure. In accordance with this technique, an electrical contact is formed simply by depositing a region of material e.g., 130, (onto the semiconductor material) having a composition which includes at least one metal element and at least one of three specific Group V elements, i.e., P, As, or Sb, and having a bulk electrical resistivity equal to or less than about 250 μΩ-cm. Alternatively, a contact is formed by depositing nickel, or a nickel-containing material essentially free of gold and silver, and having a composition which does not include any of the three Group V elements. The nickel, or nickel-containing material, is then reacted with the substrate to form a region, e.g., 130, including a compound having a composition which includes nickel as well as one of the three Group V elements.

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METHOD FOR FABRICATING DEVICES IN III-V SEMICONDUCTOR SUBSTRATES AND DEVICES FORMED THEREBY

Background of the Invention

1. Field of the Invention

The invention pertains generally to a method for fabricating devices in III-V semiconductor substrates, as well as the resulting devices.

2. Art Background

A wide variety of devices, including discrete electronic devices, discrete opto-electronic devices (devices which produce an optical output in response to an electrical input, or vice versa), as well as integrated circuit and integrated optical devices, are now being fabricated, or have been proposed for fabrication, in substrates which include III-V semiconductor materials, because these materials exhibit a number of significant advantages. (A III-V semiconductor material, for purposes of this disclosure, is a semiconductor which includes Group III and Group V elements.) Included among these advantages is the fact that the mobility of electrons in the III-V semiconductor materials is much higher than in other semiconductor materials, such as silicon. As a consequence, electronic and opto-electronic devices, e.g., discrete transistors, lasers and integrated circuit devices, fabricated in the III-V semiconductor materials are capable of achieving much higher operating speeds than are the corresponding devices fabricated in, for example, silicon. In addition, the III-V semiconductor materials are direct bandgap materials, rather than indirect bandgap materials, as is the case with silicon. As is known, stimulated emission of light is only achievable in the former type of materials. Consequently, opto-electronic devices which depend, for their operation, on stimulated light emission, e.g., lasers, must be fabricated in direct bandgap materials. Moreover, direct bandgap materials exhibit much higher quantum efficiencies than indirect bandgap materials, and therefore the former materials are preferred for the fabrication of optical detector, opto-electronic devices, such as avalanche photodiode (APD) detectors.

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The various types of devices fabricated in III-V semiconductor substrates include a variety of device components, such as active regions (a region of semiconductor material in a light-emitting opto-electronic device from which most of the light is emitted), sources, drains, p-n junctions and heterojunctions. (The term heterojunction, as used in this disclosure, denotes the interface between two semiconductor materials having different compositions or different doping levels.) Each such device also includes one or more metallic wires or metallic runners, generally fabricated from gold (Au), terminating in one or more non-rectifying, low specific contact resistance (LSCR) electrical contacts to the substrate, through which electrical signals are communicated to the device. (As used herein, the term non-rectifying, LSCR electrical contact denotes an electrical contact which permits electrical current flow in two opposed directions across the contact, and exhibits a specific contact resistance less than or equal to about 10^{-4}ohm-cm^2 in both directions. Significantly, such contacts to III-V semiconductor substrates are essential because the gold (per se) in the gold wires and gold runners yields a rectifying, rather than non-rectifying, electrical contact to III-V semiconductor materials.)

A non-rectifying, LSCR electrical contact to a III-V semiconductor substrate is conventionally formed by depositing, e.g., e-beam evaporating, a region of material which includes gold and a p-type (e.g., zinc or beryllium) or n-type (e.g., tin or germanium) dopant (depending upon whether the underlying semiconductor material is of p-type or n-type conductivity) onto the substrate. Because ultra-high-vacuum conditions are typically not employed, a native oxide (or oxides) of the semiconductor material tends to form on the surface of the substrate during the deposition procedure. Such native oxides are generally undesirable because their presence serves to increase specific contact resistance. Although the surface of the substrate is typically cleaned to remove these oxides, it is generally acknowledged that complete removal of the oxides is impossible. However, the presence of these oxides does not, in this instance, preclude the formation of a LSCR electrical contact. That is, after deposition, the gold-and-dopant-containing region is alloyed at temperatures as high as about 450 degrees Centigrade (C) for periods of time equal to about 7 minutes. Significantly, it is believed that this alloying procedure serves to drive the dopant through the native oxide (or oxides) and into the substrate, and

electrically activate the dopant, to produce an electrical contact having a low specific contact resistance.

While the above alloying procedure does produce useful, non-rectifying, LSCR electrical contacts, this procedure does have a number of disadvantages, including undesirable interactions between the gold and the semiconductor substrate. For example, the relatively high temperatures involved in the alloying process result in the gold diffusing into the substrate, causing decomposition of the substrate material. As a consequence, and if, for example, the substrate material includes indium phosphide (InP), then the resulting free In and P (freed by the decomposition of the InP) tend to diffuse to the surface of the electrical contact, where they may undergo oxidation to form electrically insulating layers. In addition, the relatively high alloying temperatures also result in upward diffusion of the p- or n-type dopant to the surface of the electrical contact, where the dopant also tends to become oxidized to form an electrically insulating layer. Unless great care is taken to remove these insulating layers, the electrical contact will exhibit undesirably high series resistance.

The downward diffusion of gold into the substrate is also undesirable because the presence of gold in, for example, an active region constitutes a non-radiative recombination center, which serves to reduce the useful lifetime of light-emitting opto-electronic devices, such as lasers. In addition, the downward diffusion of gold into a substrate containing a relatively shallow p-n junction (a p-n junction having a depth equal to or less than about one-half micrometer) is undesirable because the gold penetrates through, and thus short circuits, these relatively shallow p-n junctions.

The relatively high alloying temperatures employed in forming the gold electrical contacts are further disadvantageous because they sometimes lead to significant, differential thermal expansions of the materials covering the substrate, which in turn leads to high stress in the substrate. Such high stress is undesirable because it leads to bending of the substrate, which makes conventional lithographic processing very difficult, if not impossible. This high stress often also leads to cracking and/or peeling of material layers overlying the substrate.

The above contact-fabrication procedure is further disadvantageous because it requires that the relative amounts of gold and dopant be precisely controlled to achieve the eutectic composition. Otherwise, the gold may not melt during the alloying process and/or the alloying process may not produce a sufficient or desired interaction between the dopant and the substrate, leading to an undesirably high specific contact resistance.

The above-described problems, resulting from the undesirable interactions between gold and III-V semiconductors, as well as scientific curiosity, have led to investigations of the interactions between various metals, including nickel, and III-V semiconductor substrates, such as InP. (Regarding these investigations see E. Hokelek et al., "A Study of Schottky Contacts on Indium Phosphide", Journal of Applied Physics, Vol. 54, No. 9, September 1983, pp. 5199-5205 and G. J. Hughes et al., "Nickel and Copper on Cleaved Indium Phosphide: Structure, Metallurgy and Electronic Properties," Journal of Physics C: Solid State Physics, Vol.16 (1983), pp. 2391-2405.) In these investigations, the various metals were deposited onto indium phosphide substrates cleaved under ultra-high-vacuum conditions to avoid adsorption of contaminants, such as carbon and oxygen (which might increase specific contact resistance, or preclude the formation of non-rectifying contacts). As a result of these investigations, it was concluded, among other things, that nickel produces a Schottky barrier contact (a rectifying, metal-semiconductor contact) to InP and, moreover, that a relatively thin nickel phosphide layer is formed at the interface between the nickel and the InP. While no connection was made (in these investigations) between the existence of the nickel phosphide layer and the existence of the Schottky barrier contact, it has long been believed that a non-rectifying, LSCR contact between a metal, such as nickel, and a substrate of InP can only be achieved if the metal-InP interface is rich in indium. But the interfacial nickel phosphide layer found in the investigations was, presumably, the result of nickel reacting, i.e. combining, with the phosphorus in the InP substrate. Such a reaction would necessarily produce free indium (In), which (under the resulting In concentration gradient) would diffuse to the surface of the nickel, resulting in a nickel-InP interface which is depleted of In. Significantly, a substantial amount of In was found (presumably the result of upward diffusion) on the surface of the nickel, in these investigations.

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Consequently, and on the basis of current beliefs, an In-depleted interface, produced by the formation of an interfacial, nickel phosphide layer, would preclude the formation of a non-rectifying, LSCR contact, and would be consistent with the Schottky barrier contacts found in the investigations.

Thus, those engaged in the development of III-V semiconductor devices have sought, and continue to seek, new materials and new methods for forming non-rectifying, LSCR electrical contacts to III-V semiconductor substrates.

Summary of the Invention

The invention embodies a method of fabricating a device in a body which includes Group III - Group V semiconductor material and involves the finding that simply depositing any one of a specific class of compounds onto a p- or n-type III-V semiconductor substrate, having a doping level equal to or greater than about 10^{17} per cubic centimeter (cm^{-3}), yields a non-rectifying, LSCR electrical contact to the substrate. The members of this class of compounds are those having compositions which include at least one metal element and at least one of three specific Group V elements, i.e., phosphorus (P), arsenic (As) or antimony (Sb), and having bulk electrical resistivities equal to or less than about 250 micro-ohm-centimeters ($\mu\Omega$-cm), and preferably equal to or less than about 100 $\mu\Omega$-cm. In addition, the invention involves the finding that depositing nickel, or a nickel-containing material which is essentially free of gold and silver and does not include any of the above three Group V elements, onto a III-V semiconductor material, and then reacting the nickel, or nickel-containing material with the semiconductor material to produce a compound having a composition which includes nickel as well as at least one of the three Group V elements, also yields a non-rectifying, LSCR electrical contact. Significantly, these contacts are formed without the use of dopants and without the need for an alloying procedure. Moreover, these contacts are formed (through deposition or deposition followed by chemical reaction) without the use of ultra-high-vacuum conditions, and despite the (presumed) adsorption of contaminants and formation of native oxides of the semiconductor material.

By way of example, a non-rectifying, LSCR electrical contact to a semiconductor substrate of, for example, InP is readily formed simply by depositing a region of nickel phosphide directly onto the substrate. Alternatively, a region of nickel is deposited onto the substrate and allowed to

spontaneously react with substrate material to form a relatively thin, interfacial layer of nickel phosphide. Contrary to the conventional wisdom, the (presumably) In-depleted interface between the deposited nickel and the semiconductor substrate does not preclude formation of a non-rectifying, LSCR electrical contact.

After being formed, the inventive LSCR electrical contacts are often subjected to relatively high temperatures during various device fabrication steps. Depending upon the particular compositions of the materials employed in the electrical contacts, these materials may (under the influence of the relatively high temperatures) undergo reactions with the substrate material. As a consequence, Group III and/or Group V elements in the substrate may be freed to diffuse to the surface of the electrical contacts, where they may undergo oxidation to form electrically insulating layers.

To avoid the possibility of reactions during high temperature processing, the compositions of the materials employed in the inventive LSCR electrical contacts are preferably chosen (in accordance with a two-step procedure, described below) to have heats of formation which preclude such reactions.

Significantly, it has been found that non-rectifying, LSCR electrical contacts having compositions which preclude reactions with the III-V semiconductor substrates, which are amorphous, and have thicknesses equal to or greater than about 20 nm, are effective barriers to the diffusion of gold (from overlying gold regions, used to facilitate bonding of gold wires or runners) into underlying substrates. As a consequence, light-emitting opto-electronic devices which include such contacts have significantly increased lifetimes. Moreover, LSCR electrical contacts to relatively shallow p-n junctions are now readily formed, without short-circuiting the p-n junctions.

Brief Description of the Drawings

The invention is described with reference to FIGS. 1-6, which depict the steps involved in fabricating a channel-substrate-buried-heterostructure indium phosphide laser, using the inventive device fabrication method.

Detailed Description

The invention involves a method for fabricating devices in III-V semiconductor substrates, which is distinguished from previous such methods in that it includes a new technique for forming non-rectifying, LSCR electrical

contacts to these substrates. The invention also involves the devices, e.g., transistors, lasers, light-emitting diodes, photodetectors, integrated circuits and integrated optical devices, resulting from the inventive method.

As discussed, the invention involves the finding that non-rectifying, LSCR electrical contacts to p- or n-type III-V semiconductor substrates, having doping levels equal to or greater than about $10^{17}cm^{-3}$, are readily formed, using either of two techniques. In the first technique, an electrical contact is formed by first cleaning the substrate (using conventional degreasers and oxide strippers), and then simply depositing, e.g., DC magnetron sputtering, any one of a specific class of compounds onto the substrate. The members of this class of compounds are those having compositions which include at least one metal element and at least one of three specific Group V elements, i.e., P, As or Sb, and having bulk resistivities equal to or less than about 250 $\mu\Omega$-cm, and preferably equal to or less than about 100 $\mu\Omega$-cm. The compounds which meet these requirements are typically (although not exclusively) binary, ternary, or quatenary metallic compounds which include, for example, Ni_3P, Ni_2P, NiP, $Ni_{11}In_4P_2$, Ni_3As, Ni_2As, NiAs, Ni_3Sb, Ni_2Sb, and NiSb.

Significantly, the compound deposition, referred to above, need not take place under ultra-high-vacuum conditions, and, if possible, even ordinary room atmospheric conditions are useful. Surprisingly, and even though contaminants are presumably adsorbed, and native oxides of the semiconductor material are presumed to form, during the time interval between cleaning and deposition, the resulting electrical contact is highly useful, i.e., exhibits a specific contact resistance equal to or less than about $10^{-4}ohm\text{-}cm^2$ to current flow in two opposed directions.

In the second technique, a non-rectifying, LSCR electrical contact to a III-V semiconductor substrate is formed by (cleaning the substrate and) depositing nickel, or a nickel-containing material which is essentially free of gold and silver and does not include any of the three Group V elements, onto the substrate. Then the deposited material is either induced to react (e.g., heat is supplied), or allowed to spontaneously react (i.e., no external stimulus, such as heat, is supplied), with the substrate to form a compound having a composition which includes both nickel as well as one (or more) of the three Group V elements. (Generally, it cannot be predicted whether any particular set of

deposition conditions will result in a spontaneous reaction between the deposited material and the substrate material to produce the desired compound. However, the presence or absence of the desired compound is readily detected using conventional techniques such as Auger electron spectroscopy. Thus, the utility of a particular deposition procedure for achieving the desired spontaneous reaction is readily determined empirically.)

By way of example, an electrical contact to a substrate of InP is formed by depositing, e.g., e-beam evaporating, a region of nickel directly onto the substrate, and then allowing the nickel to spontaneously react with the substrate (during and after the deposition procedure) to form a relatively thin, interfacial layer of nickel phosphide. (The thickness of this interfacial layer is typically several fractions of a nanometer.) If a thicker layer of nickel phosphide is desired, then the nickel-bearing InP-substrate should, for example, be heated, to react additional nickel with the substrate material. In this regard, it has been found that a relatively thick layer of essentially pure Ni_2P is readily formed by carrying out the heating process (at a temperature of, for example, 300 degrees C) in an atmosphere of forming gas, i.e., an atmosphere which includes about 15 percent (by volume) of H_2 and about 85 percent of N_2.

It is contemplated that the two techniques, described above, yield non-rectifying, LSCR contacts because Group III elements in the substrate form chemical bonds with the Group V elements in the contacts. Moreover, it is believed that electron-transport across the contact-substrate interface is largely due to thermionic emission.

Significantly, the nickel-containing electrical contacts formed by deposition and reaction are typically crystalline in nature. By contrast, the electrical contacts formed by deposition, alone, are either crystalline or amorphous in nature, depending upon deposition conditions. (For purposes of the invention, a material is amorphous if it either has no grains or, if grains are present, their dimensions are equal to or less than about 50 nm.) For example, if an electrical contact of Ni_2P is deposited using conventional DC magnetron sputtering techniques, then a relatively low substrate-support temperature (e.g., -100 degrees Centigrade) and/or a relatively low sputtering voltage (e.g., 280 volts) yields amorphous Ni_2P. On the other hand, a substrate-support maintained at room temperature (23 degrees Centigrade) and/or a relatively

high sputtering voltage (e.g., 300 volts) yields crystalline Ni_2P. This distinction between the natures of the electrical contacts results in different contact properties. That is, crystalline contacts typically exhibit lower bulk resistivities than amorphous contacts, which leads to reduced series resistance. On the other hand, as discussed more fully below, amorphous contacts are better diffusion barriers than crystalline contacts.

The inventive method for fabricating devices often involves relatively high temperature processing subsequent to the fabrication of a non-rectifying LSCR electrical contact (or contacts). Such high temperature processing may result in chemical reactions between the material of the electrical contact and the substrate material. As a consequence, some Group III and/or Group V elements in the substrate may be freed to diffuse to the surface of the electrical contact, where they may be oxidized to form electrically insulating layers. Such layers may lead to relatively high series resistance.

Preferably, to avoid the high temperature reactions, discussed above, the composition of the material employed in the inventive electrical contact is chosen in accordance with a two-step procedure. In the first step, those compositions are identified which include P, As, or Sb (and nickel, if the contact is formed by deposition and reaction), have bulk resistivities less than or equal to about 250 $\mu\Omega$-cm, and have heats of formation per metal atom (kilocalories per metal atom) which are more negative than that of the substrate composition, i.e., in magnitude (absolute value), the heats of formation per metal atom of the potentially useful compositions are larger than that of the substrate composition. (If a composition includes more than one metal element, then the average heat of formation per metal atom is employed.) Compositions which meet this requirement are (by definition) thermodynamically more stable than the substrate composition. However, one or more of these compositions might still react (under the influence of the relatively high temperatures) with substrate material to form an even more stable composition. To avoid this possibility, these particular compositions are identified and weeded out. That is, during the second step, the most stable composition, i.e., the composition having the most negative heat of formation per metal atom, is initially identified. Then, the magnitude (the absolute value) of the difference between the heat of formation per metal atom of each composition (identified in the first

step) and the most stable composition is calculated. If, for any particular composition, this magnitude is less than the magnitude (absolute value) of the heat of formation per metal atom of the semiconductor composition, then (thermodynamically) this particular composition is precluded from reacting with the substrate to form a more stable composition. Alternatively, and regardless of this requirement, if a particular composition has a larger relative amount of the Group V element than the most stable composition, then this composition too is precluded from reacting with the substrate.

By way of example, if the semiconductor substrate is of InP, then the first step (of the two-step procedure) implies that the potentially useful compositions include Ni_6P_5, Ni_3P_2, and Ni_2P. Significantly, Ni_6P_5 is the most stable of these compositions. Applying the criterion of the second step implies that all of these compositions are thermodynamically stable, i.e., will not react with InP. Moreover, NiP is also useful (will not react with InP) because it contains a larger relative amount of P than Ni_6P_5.

Typically, after an electrical contact is formed, a region of gold (and, perhaps, other materials) is deposited onto the contact to facilitate the bonding of gold wires and/or gold runners to the electrical contact. Significantly, it has been found that material regions which are thermodynamically stable, as defined by the above two-step procedure, are amorphous, and have thicknesses equal to or greater than about 20 nanometers are effective barriers to undesirable interdiffusion of gold (from the overlying gold region) and the underlying semiconductor material. (Such interdiffusion is undesirable for the reasons given above, in relation to conventional gold electrical contacts.) Thus, such materials are useful both as diffusion barriers and as non-rectifying, LSCR electrical contacts. In fact, such material regions are highly useful just as diffusion barriers interposed between any of a variety of electrical contacts and, for example, the corresponding, overlying gold regions.

Among other advantages, the inventive technique for forming electrical contacts makes it possible to form a relatively shallow electrical contact to a relatively shallow p-n junction or a relatively shallow heterojunction (a p-n junction or heterojunction having a depth less than or equal to about 1/2 micrometer), without short-circuiting the p-n junction or heterojunction. (For purposes of the invention, the depth of a p-n junction, or of a heterojunction, is

defined with reference to the device surface, or interface between different material regions of the device, on which the electrical contact is formed, or from, or through which, the electrical contact extends. That is, the depth of a p-n junction formed, for example, by producing a p-type region within an n-type substrate, is defined as the length of a perpendicular extending from a least-squares-fit planar approximation to the above reference surface or reference material interface to the lowest point where the dopant concentration in the p-type region is equal to the dopant concentration in the n-type substrate. On the other hand, the depth of a heterojunction formed by different semiconductor materials is defined as the length of a perpendicular extending from the above least-squares-fit planar approximation to the lowest point of the interface between the two materials, as determined using, for example, Auger electron spectroscopy. Further, the depth of a heterojunction formed by semiconductor materials having the same composition but different doping levels is as defined above, except that the perpendicular extends to the lowest point of the interface between the two materials where the doping level is the average of the doping levels in the two materials as determined, for example, by SIMS analysis.) That is, and as discussed above, the alloying procedure involved in forming a conventional gold contact typically results in gold being diffused downwardly into the semiconductor substrate. If the electrical contact is to a substrate region containing a p-n junction or heterojunction having a depth equal to or less than about 1/2 micrometer, then the gold invariably diffuses more than about 1/2 micrometer, i.e., the gold diffuses into, and through, the junction, short-circuiting the junction. By contrast, the inventive technique involves no alloying procedure. Thus, provided the contact material is thermodynamically stable, amorphous, and has a thickness equal to or greater than about 20 nanometers, both gold and contact material are largely precluded from diffusing downwardly into the semiconductor substrate into electrical contact with the p-n junction or heterojunction.

Yet another advantage of the invention is the fact that it permits the useful lifetimes of light-emitting, discrete opto-electronic and integrated optical devices to be significantly increased. That is, by forming the material compositions with thicknesses equal to or greater than about 20 nanometers, the downward diffusion of gold into the active regions of such devices is largely

precluded. As a consequence, the formation of non-radiative recombination centers is largely avoided.

As a pedagogic aid to an even more complete understanding of the invention, the application of the inventive device fabrication method to the formation of a channel-substrate-buried-heterostructure InP laser, is described below.

With reference to FIGS. 1-6, the laser is formed in a substrate which initially includes just a bulk region 10 of, for example, n-type InP, e.g., a wafer of n-type InP. The doping level within the bulk region 10 is, for example, about $8 \times 10^{17} cm^{-3}$.

The first step in the fabrication of the laser is to form a blocking layer 30, i.e., a layer which blocks the flow of currents external to the active region (described below) into the bulk region 10, adjacent to the upper surface 20. The blocking layer 30 is formed, for example, by diffusing a p-type dopant, such as cadmium, into the bulk region 10. The doping level within the blocking layer should be equal to or greater than about $4 \times 10^{18} cm^{-3}$ to avoid the flow of undesirable leakage currents across the blocking layer and into the bulk region 10. In addition, the thickness of the blocking layer 30 ranges from about 0.5 μm to about 1.5 μm. Thicknesses less than about 0.5 μm are undesirable because they too result in undesirable leakage currents across the blocking layer. Thicknesses greater than about 1.5 μm are undesirable because they result in lasers which require undesirably large amounts of electrical power to achieve stimulated light emission.

Alternatively, the blocking layer 30 is formed by depositing a layer of semi-insulating InP onto the surface 20, using conventional metal organic chemical vapor deposition techniques. Here, the term semi-insulating means that the deposited semiconductor material has a bulk resistivity equal to or greater than about 10^7 ohm-cm.

After the formation of the blocking layer 30, an etch mask 40 is formed on the upper surface of the blocking layer. This etch mask includes, for example, a layer of silicon dioxide which is deposited onto the blocking layer 30 using conventional plasma deposition techniques. The etch mask is formed by patterning the silicon dioxide layer using, for example, conventional lithographic techniques. The thickness of the silicon dioxide layer ranges from 110 nm to

about 130 nm. Thicknesses less than about 110 nm are undesirable because they result in an undesirably large number of pinholes in the silicon dioxide. On the other hand, thicknesses greater than about 130 nm are undesirable because they make it difficult to achieve the desired sidewall inclination of the V-groove, described below.

With the etch mask 40 in place, a crystallographic, chemical etchant, e.g., 3:1 $HCl:H_3PO_4$, is applied to the exposed region of the substrate surface to form a V-groove 50. This V-groove 50 serves to channel, and confine, the electrical current to the active region of the laser. The etchant is chosen to expose (111) facets of the crystalline substrate. Moreover, the width of the V-groove ranges from about 3.5 micrometers (μm) to about 4.5 μm. Widths less than about 3.5 μm, or greater than about 4.5 μm, are undesirable because they result in devices which require an undesirably large amount of electrical power to achieve stimulated emission of light.

After the etching of the V-groove 50, and after removing (using conventional chemical etchants) the etch mask 40, an n-type InP buffer region 60 is grown in the bottom of the V-groove 50 (as well as on the surface of the blocking layer 30) using conventional liquid phase epitaxy (LPE) techniques. The thickness of the buffer region, as measured from the bottom of the V-groove, typically ranges from about 0.5 μm to about 1 μm. Unlike the sidewalls of the V-groove, the buffer region 60 is largely free of contaminants and defects.

An undoped, active region 70 of III-V semiconductor material is now grown on the buffer region 60 in the V-groove 50 (as well as on the upper surface of the blocking layer 30) using conventional LPE techniques. To ensure that electrical conduction is largely confined to the active region 70, the bandgap of the semiconductor material employed in the active region should be less than that of the semiconductor material employed both in the blocking layer 30 and in the cladding layer (discussed below). One such useful (active region) material is, for example, (undoped) indium gallium arsenide phosphide (InGaAsP). The thickness of the active region ranges from about 0.2 μm to about 0.7 μm. Thicknesses less than about 0.2 μm are undesirable because such thin regions result in undesirably little stimulated light emission from the laser. Thicknesses greater than about 0.7 μm are undesirable because they result in lasers which require an undesirably large amount of electrical power to achieve

stimulated emission of light.

The growth of the active region 70 is followed by the LPE-growth of a cladding layer 80 and of a cap layer 90. The former is, for example, of p-type InP, while the latter is of p-type indium gallium arsenide (InGaAs). The thickness of the cladding layer, and of the cap layer, is typically about 1 μm.

A (patterned) deposition mask 120 is now formed on the upper surface of the cap layer 90. As discussed below, the deposition mask permits the electrical contact to the laser to be formed in vertical alignment with the active region 70. The deposition mask 120 includes a layer 100 of silicon dioxide which is deposited onto the cap layer 90 using, for example, conventional plasma deposition techniques. In addition, the deposition mask includes a layer 110 of, for example, photoresist. The thickness of the silicon dioxide layer is typically about 0.3 μm, while the thickness of the photoresist is typically about 1 μm. In forming the deposition mask, the photoresist is initially patterned, i.e., a region of the photoresist overlying the active region 70 is removed, using conventional exposure and development techniques. The width of this region (and thus the ultimate width of the electrical contact) is typically about 6 μm. The patterned photoresist layer is then used as an etch mask during the etching of the silicon dioxide layer 100, resulting in the removal of a region of the silicon dioxide layer which also overlies the active region 70. Useful silicon dioxide-etchants include, for example, buffered HF.

An electrical contact to the laser is now produced by depositing, e.g., sputtering, an amorphous region 130 of, for example, Ni_6P_5 onto the exposed upper surface of the cap layer 90. Preferably, the thickness of the region 130 is equal to a greater than about 20 nanometers, to avoid the downward diffusion of gold (from a gold region subsequently formed on the region 130).

Preferably, to enhance the adhesion of the region 130 to the cap layer 90, a layer 140 of titanium is deposited onto the upper surface of the region 130 as well as onto the upper surface of the silicon dioxide layer 100. The thickness of the titanium layer is typically about 5 nanometers.

With the completion of the electrical contact, a layer 150 of gold is deposited onto the upper surface of the titanium layer 140, to facilitate the subsequent bonding of a gold wire to the electrical contact. The thickness of the gold layer is typically about 1 μm.

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A second electrical contact is, of course, needed to apply voltages to the laser. This second contact is formed on the backside of the substrate by initially thinning the bulk region 10 (typically by about 75 μm) using conventional mechanical lapping, and then depositing successive layers 160 and 170 of, respectively, Ni_6P_5 and gold, onto the backside, as described above.

The bulk region 10, which is now an integral part of the laser, is typically a portion of a wafer which, at this point, is cleaved (using conventional techniques) to form the end mirror-facets of the laser device. The laser device is separated from the wafer using saw cuts transverse to the mirror-facets.

The final steps in the fabrication of the laser typically involve soldering (at temperatures ranging from about 200 degrees C to about 350 degrees C) the laser to a stud which serves both as a heat sink for the device, as well as a device carrier or package. Then, gold wires are bonded to the gold regions 150 and 170 covering the top and bottom of the laser.

Example 1

The lower surface of a 1.27 cm (one-half-inch) diameter indium phosphide wafer, of n-type conductivity, and having a doping level of $8 \times 10^{17} cm^{-3}$, was cleaned using conventional degreasers and oxide strippers. Using conventional e-beam evaporation techniques, successive layers of gold, germanium, and gold were deposited onto the cleaned lower surface. The thicknesses of these layers were, respectively, 5 nm, 15 nm, and 100 nm.

The upper surface of the wafer was degreased, and a layer of SiO_2, having a thickness of 500 nm, was plasma deposited onto the upper surface. A layer of photoresist was spin-deposited onto the SiO_2, and conventionally lithographically patterned to remove circular regions of photoresist having diameters ranging from about 20 μm to about 200 μm. Using the patterned photoresist as an etch mask, the silicon dioxide was chemically etched with buffered HF to expose corresponding circular surface areas of the indium phosphide.

A layer of Ni_2P, having a thickness of about 100 nm, was deposited onto the exposed, circular surface areas of the wafer, as well as onto the photoresist, using DC magnetron sputtering. The gas within the sputtering chamber was argon, the pressure of the gas was 1.6 Pa (12 millitorr), and the DC voltage was 300 volts. The Ni_2P-covered photoresist was then stripped from the wafer using

conventional chemical etchants.

The conventional Cox and Strack technique (see R. H. Cox and H. Strack, Solid State Electronics, Vol. 10, page 1213 (1967)) was employed to measure the specific contact resistance at each of the Ni_2P-covered regions of the wafer, using electrical currents of opposite polarity. In all cases, the specific contact resistance was equal to or less than about 3×10^{-6} ohm-cm^2.

Example 2

A 1.27 cm (one-half-inch) indium phosphide wafer was processed, as in Example 1, except that a different technique was used to form the circular regions of Ni_2P on the upper surface of the wafer. That is, after the photoresist and SiO_2 were patterned, a 100 nm-thick layer of Ni was e-beam evaporated onto the exposed, circular surface areas of the wafer, as well as onto the photoresist. After stripping the Ni-covered photoresist, the wafer was placed in an atmosphere of forming gas, and heated to a temperature of 300 degrees C for 30 minutes to produce circular regions of Ni_2P, having thicknesses of about 130 nm, on the wafer.

Using the technique employed in Example 1, the specific contact resistance, in all cases, was found to be equal to or less than about 3×10^{-6} ohm-cm^2.

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Claims

1. A method for fabricating a device in a body which includes III-V semiconductor material, comprising the steps of:

forming a non-rectifying, low-specific-contact-resistance electrical contact to a region of said body having a doping level equal to or greater than about $10^{17}cm^{-3}$; and

completing the fabrication of said device,

CHARACTERIZED IN THAT

said forming step includes the step of

(a) depositing a metal-containing first region of material onto said region of said body, or

(b) depositing a nickel-containing second region of material, essentially free of gold and silver, onto said region of said body and reacting said second region with said semiconductor material to form a nickel-containing third region of material,

each of said first and third regions having a composition which includes at least one element chosen from the group consisting of phosphorus, arsenic and antimony, and having a bulk resistivity equal to or less than about 250 $\mu\Omega$-cm.

2. The method according to claim 1

CHARACTERIZED IN THAT

said metal of said first region includes nickel.

3. The method according to claim 1,

CHARACTERIZED IN THAT

said composition is chosen to preclude chemical reactions between said first or said third of material and said semiconductor material.

4. The method according to claim 1,

CHARACTERIZED IN THAT

said first region of material, or said third region of material, is amorphous.

5. The method according to claim 1,

CHARACTERIZED IN THAT

said first region of material, or said third region of material, has a thickness equal to or greater than about 20 nanometers.

6. The method according to claim 1,

CHARACTERIZED IN THAT

said device includes a discrete electronic device or an integrated circuit device or an opto-electronic or an integrated optical device.

7. The method according to claim 6,

CHARACTERIZED IN THAT

said discrete electronic device includes a transistor.

8. The method according to claim 6,

CHARACTERIZED IN THAT

said opto-electronic device includes a laser or a light-emitting diode or a photodetector.

9. A method according to claim 1,

CHARACTERIZED IN THAT

said body includes a surface or material interface, and said body region includes a p-n junction or a heterojunction adjacent said surface or material interface;

said p-n junction or said heterojunction has a depth, as measured from said surface or material interface, equal to or less than about 1/2 micrometer,

a non-rectifying, low-specific-contact-resistance electrical contact is on and/or extends from or through said surface or material interface, and

said electrical contact includes material which, if it extends into said body, does not extend into electrical contact with said p-n junction or said heterojunction.

FIG. 1

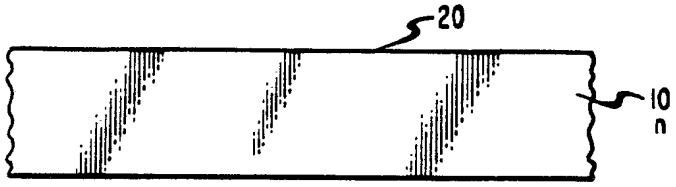


FIG. 2

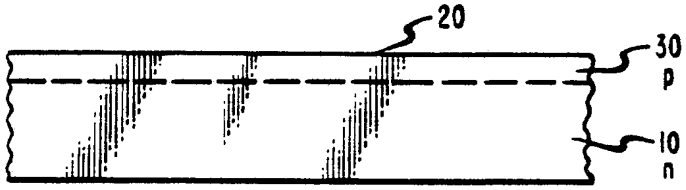


FIG. 3

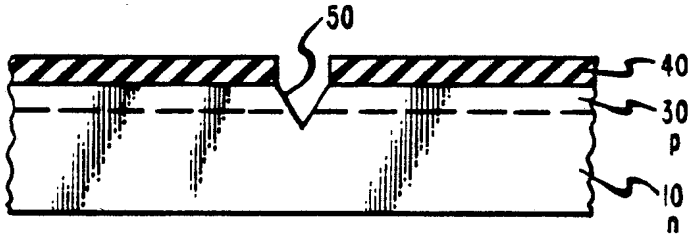
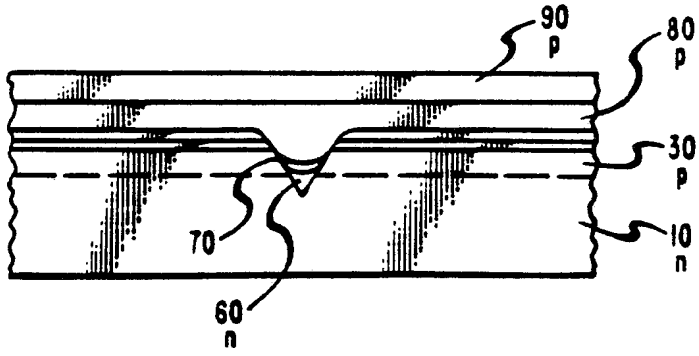


FIG. 4



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FIG. 5

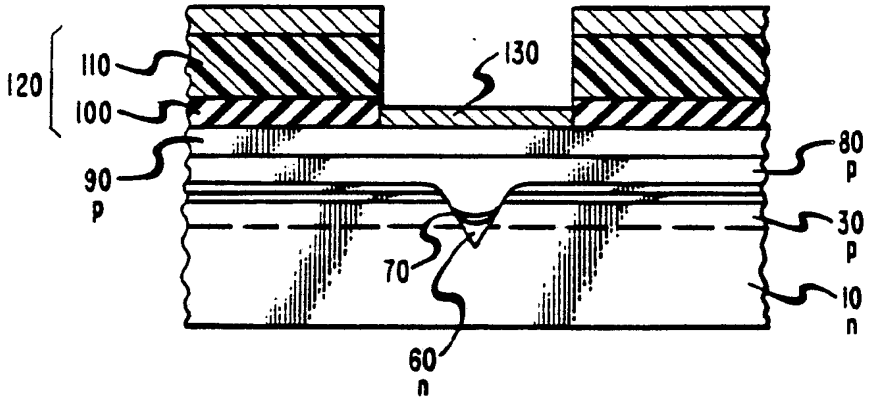
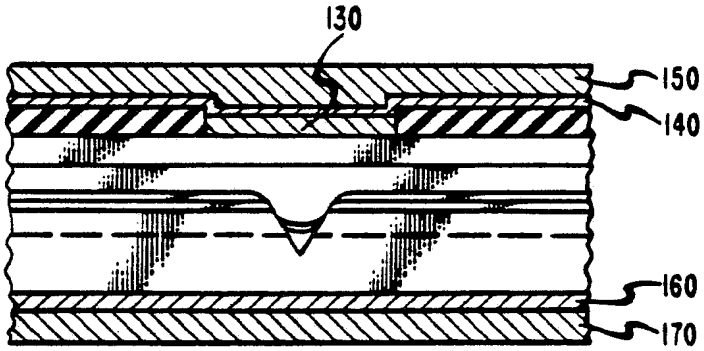


FIG. 6



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/01520

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [5]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 21/285; H 01 L 29/40; H 01 L 33/00

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	Materials Letters, volume 3, no. 7,8, May 1985, Elsevier Science Publishers B.V., (Amsterdam, NL), S.R. Smith et al.: "Stable ohmic contacts to n-GaAs using ion-beam mixing", pages 294-298 see the whole document	1,2,6,9
A	GB, A, 2024506 (WESTERN ELECTRIC CO.) 9 January 1980 see the whole document	1,6-9
A	Journal of Physics C: Solid State Physics, volume 16, 1983, The Institute of Physics, (London, GB), G.J. Hughes et al.: "Nickel and copper on cleaved indium phosphide: structure, metallurgy and electronic properties", pages 2391-2406 see paragraph 1: "Introduction"; paragraph 4: "Discussion" cited in the application	1-3

./.

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
21st September 1987	18 NOV 1987
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

Form PCT/ISA/210 (second sheet) (January 1985)

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III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	Thin Solid Films, volume 70, no. 1, July 1980, Elsevier Sequoia S.A., (Lausanne, CH), M. Ogawa: "Alloying reaction in thin nickel films deposited on GaAs", pages 181-189 see the whole document	1
A	Solid-State Electronics, volume 26, no. 3, March 1983, Pergamon Press Ltd, (Exeter, GB), A. Piotrowska et al.: "Ohmic contacts to III-V compound semiconductors: a review of fabrication techniques", pages 179-197	
A	Journal of Applied Physics, volume 54, no. 9, September 1983, American Insitute of Physics, (New York, US), E. Hökelek et al.: "A study of Schottky contacts on indium phosphide", pages 5199-5205 cited in the application	

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/01520 (SA 17750)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 29/09/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
GB-A- 2024506	09/01/80	BE-A-	877189	15/10/79
		NL-A-	7904979	02/01/80
		FR-A,B	2430090	25/01/80
		DE-A-	2925791	03/01/80
		US-A-	4186410	29/01/80
		JP-A-	55004999	14/01/80
		CA-A-	1125924	15/06/82

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特開平9－289178

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Ｈ０１Ｌ	21/28	３０１		Ｈ０１Ｌ	21/28	３０１Ｒ	
	21/265				21/265	Ｗ	
	21/3205				21/88	Ｎ	
	21/768				21/90	Ｃ	
	29/78				29/78	３０１Ｐ	

審査請求　未請求　請求項の数23　ＦＤ　（全 18 頁）　最終頁に続く

(21)出願番号　特願平9－47053

(22)出願日　平成９年(1997)２月14日

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(33)優先権主張国　日本（ＪＰ）

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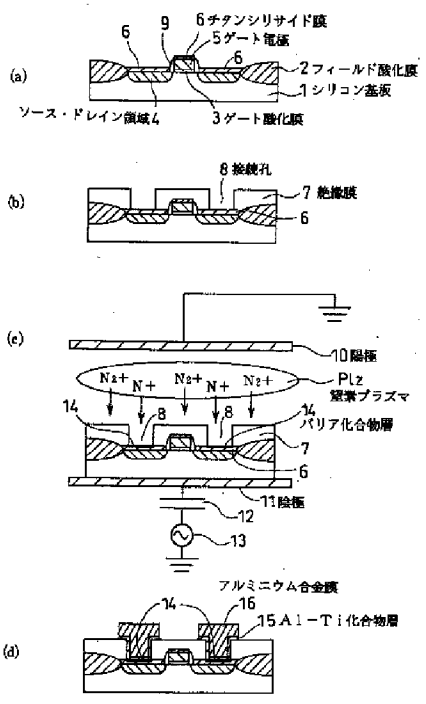
(74)代理人　弁理士　前田　弘　（外２名）

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】

【課題】　半導体装置において、熱処理時に金属シリサイドとその上の金属層との間の反応に起因する接合リーク等の発生を防止する。

【解決手段】　接続孔８の開口後ないしは絶縁膜７の堆積前に、半導体装置をプラズマ発生装置の陰極１１に固定し、例えばチタンシリサイド膜６等の金属シリサイド膜の表面を５５０℃以下で窒素を含むガスのプラズマにさらす。この処理により、チタンシリサイド膜６等の金属シリサイド膜の表面付近の領域に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層１４を形成する。その後、接続孔８に窒化チタン・窒化膜等のバリアメタルを堆積しなくても、Ａｌ－Ｔｉ化合物層１５，アルミニウム合金膜１６等の段差被覆性のよい材料で埋込層を形成しながら、後の熱処理時における金属シリサイドと埋込層との反応を阻止できる。したがって、コンタクト抵抗やシート抵抗及び接合リークを低減し、信頼性を向上させることができる。



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【特許請求の範囲】
【請求項１】　半導体基板と、
上記半導体基板の一部に形成され第１の金属がシリサイド化されてなる金属シリサイド膜と、
上記金属シリサイド膜の上に形成された第２の金属からなる金属膜と、
上記金属シリサイド膜の表面付近の領域に形成され、窒素－酸素－第１の金属－シリコン間化合物からなるバリア化合物層とを備えていることを特徴とする半導体装置。
【請求項２】　請求項１記載の半導体装置において、
上記金属シリサイド膜全体の表面付近の領域に上記バリア化合物層が形成されていることを特徴とする半導体装置。
【請求項３】　請求項１又は２記載の半導体装置において、
上記バリア化合物層の厚みは、上記第２の金属の上記バリア化合物層への拡散を阻止するのに十分な厚み以上で上記金属シリサイド膜の厚みの３０％以下であることを特徴とする半導体装置。
【請求項４】　請求項１又は２記載の半導体装置において、
上記バリア化合物層の厚みは、２～２０ｎｍの範囲であることを特徴とする半導体装置。
【請求項５】　請求項１，２又は３記載の半導体装置において、
上記バリア化合物層内における上記窒素の濃度が最大となる位置は、上記酸素の濃度が最大となる位置よりも奥方であることを特徴とする半導体装置。
【請求項６】　請求項１記載の半導体装置において、
上記金属シリサイド膜の上に形成された絶縁膜と、
上記絶縁膜の一部に形成され上記金属シリサイド膜に到達する接続孔とをさらに備え、
上記金属膜は、上記接続孔内に堆積された第２の金属からなる埋込層であることを特徴とする半導体装置。
【請求項７】　請求項１記載の半導体装置において、
上記金属シリサイド膜の上に形成された絶縁膜と、
上記絶縁膜の一部に形成され上記金属シリサイド膜に到達する接続孔と、
上記接続孔内に堆積された第３の金属からなる埋込層とをさらに備えていることを特徴とする半導体装置。
【請求項８】　請求項１，２，３，４，５，６又は７記載の半導体装置において、
上記第１の金属は、チタン，コバルト，ニッケル，タンタル，タングステン，ニオブ，パラジウム，白金及びモリブデンのうちいずれか１つであることを特徴とする半導体装置。
【請求項９】　請求項１，２，３，４，５，６又は７記載の半導体装置において、
上記第２の金属は、アルミニウムを含む金属，銅を含む金属及びタングステンを含む金属のうちいずれか１つであることを特徴とする半導体装置。
【請求項１０】　半導体基板上に、第１の金属とシリコンとの化合物からなる金属シリサイド膜を形成する第１の工程と、
中性ないし酸化雰囲気下で、上記金属シリサイド膜の表面に窒素を含むイオンを照射して、上記金属シリサイド膜の表面付近の領域に窒素－酸素－第１の金属－シリコン間化合物からなるバリア化合物層を形成する第２の工程と、
上記金属シリサイド膜の上記バリア化合物層の上に第２の金属を堆積して金属膜を形成する第３の工程とを備えていることを特徴とする半導体装置の製造方法。
【請求項１１】　請求項１０記載の半導体装置の製造方法において、
上記第１の工程の後かつ上記第２の工程の前に、上記金属シリサイド膜の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記金属シリサイド膜に到達する接続孔を形成する工程とをさらに備え、
上記第２の工程では、上記金属シリサイド膜の表面付近の領域のうち上記接続孔の底部に露出した領域に上記バリア化合物層を形成し、
上記第３の工程では、上記接続孔内を上記第２の金属で埋め込むことを特徴とする半導体装置の製造方法。
【請求項１２】　請求項１０記載の半導体装置の製造方法において、
上記第２の工程の後に、上記金属シリサイド膜の上記バリア化合物層の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記バリア化合物層に到達する接続孔を形成する工程とをさらに備え、
上記第３の工程では、上記接続孔内に上記第２の金属を堆積することを特徴とする半導体装置の製造方法。
【請求項１３】　請求項１２記載の半導体装置の製造方法において、
上記第３の工程の後に、
上記金属シリサイド膜の上記バリア化合物層の上に絶縁膜を形成する工程と、
上記絶縁膜の一部を選択的に除去して上記バリア化合物層に到達する接続孔を形成する工程と、
上記接続孔内に第３の金属を堆積して埋込層を形成する工程とをさらに備えていることを特徴とする半導体装置の製造方法。
【請求項１４】　請求項１０，１１，１２又は１３記載の半導体装置の製造方法において、
上記第２の工程では、チャンバ内に陰極である下部電極と陽極である上部電極とを配置したプラズマ発生装置を用い、上記チャンバ内において、上記半導体基板を上記下部電極上に載置した状態で上記金属シリサイド膜を窒素を含むガスのプラズマにさらすことにより上記バリア化合物層を形成することを特徴とする半導体装置の製造

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方法。
【請求項１５】　請求項１０，１１，１２又は１３記載の半導体装置の製造方法において、
上記第２の工程では、上記金属シリサイド膜の表面を窒素を含むガスにさらしながら紫外線及び電離放射線のうちいずれか一方を照射することにより、上記バリア化合物層を形成することを特徴とする半導体装置の製造方法。
【請求項１６】　請求項１０，１１，１２又は１３記載の半導体装置の製造方法において、
上記第２の工程では、上記金属シリサイド膜の表面を窒素を含むイオンビームにさらすことにより、上記バリア化合物層を形成することを特徴とする半導体装置の製造方法。
【請求項１７】　請求項１０，１１，１２，１３，１４，１５又は１６記載の半導体装置の製造方法において、
上記第２の工程を、５５０℃以下で行なうことを特徴とする半導体装置の製造方法。
【請求項１８】　請求項１０，１１，１２，１３，１４，１５又は１６記載の半導体装置の製造方法において、
上記第２の工程では、上記窒素を含むガスとしてN2 ガスを用いることを特徴とする半導体装置の製造方法。
【請求項１９】　請求項１０，１１，１２，１３，１４，１５，１６，１７又は１８記載の半導体装置の製造方法において、
上記第２の工程の前に、水素を含むガスを流すことにより、上記金属シリサイド膜上の自然酸化膜を除去する工程をさらに備え、
上記第２の工程では、酸素を含むガスを添加することを特徴とする半導体装置の製造方法。
【請求項２０】　請求項１０，１１，１２，１３，１４，１５又は１６記載の半導体装置の製造方法において、
上記第２の工程では、窒素を含むイオンを３ｋｅＶ以下のイオンエネルギーで上記金属シリサイド膜内に導入することを特徴とする半導体装置の製造方法。
【請求項２１】　請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０記載の半導体装置の製造方法において、
上記第１の工程では、金属シリサイド膜として、チタン，コバルト，ニッケル，タンタル，タングステン，パラジウム，白金及びモリブデンのうちいずれか１つのシリサイド膜を形成することを特徴とする半導体装置の製造方法。
【請求項２２】　請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０記載の半導体装置の製造方法において、
上記第３の工程では、ＣＶＤ法を用いてアルミニウムを含む金属，銅を含む金属及びタングステンを含む金属のうちいずれか１つを堆積することを特徴とする半導体装置の製造方法。
【請求項２３】　請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０記載の半導体装置の製造方法において、
上記第３の工程では、チタン及びアルミニウム合金を連続的にスパッタすることにより、上記金属膜をＡｌ－Ｔｉ化合物層及びアルミニウム合金膜により構成することを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、シリサイド層を有する半導体装置及びその製造方法に係り、特にシリサイド層の上層配線や上部低抵抗金属膜との間におけるコンタクト部の構造の改良に関するものである。
【０００２】
【従来の技術】近年、超ＬＳＩの高集積化、高密度化にともない、超ＬＳＩに搭載されるＭＯＳ型トランジスタのゲート電極、ソース・ドレイン領域の表面に自己整合的に金属シリサイド層を形成し、ゲート電極、ソース・ドレイン領域のシート抵抗を小さくすると共にコンタクト抵抗や拡散抵抗等の寄生抵抗を低減し、半導体素子の動作速度を向上させる技術（サリサイド技術）が用いられている。
【０００３】ところで、上記金属シリサイド層の上にアルミニウム，タングステン，銅からなる埋込層を形成する方法として、例えば高温におけるアルミニウム合金の流動性を利用した高温スパッタ法、あるいは、被覆性に優れる化学気相堆積（以下ＣＶＤと記す）法により選択的に接続孔内にアルミニウムやタングステン、銅等の金属を堆積して、信頼性の高い埋込層を形成する方法が知られている。その場合、埋込層を構成するこれらの金属と金属シリサイド層とが接する部分において、両者間で反応が生じ問題となることがある。すなわち、高温スパッタや選択ＣＶＤあるいは上層の配線を形成するＣＶＤにおいて４５０～６００℃程度の熱履歴が生じるので、金属シリサイドと埋込層を構成する金属とが反応し、この反応生成物によってシリコン基板が浸食されて、接合リークを発生する虞れがある。そのため、両者間における反応を抑制すべく、埋込層と金属シリサイド層との間に窒化チタン等のバリアメタルを形成することが一般的に行なわれている。
【０００４】以下、図１５（ａ）～（ｄ）を参照しながら、高温スパッタ法を用いて金属シリサイド層上の埋込層を形成する従来の方法について説明する。
【０００５】まず、図１５（ａ）に示すように、シリコン基板１上のフィールド酸化膜２により取り囲まれる活性領域の上に、シリコン酸化膜からなるゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、シリコン

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酸化膜からなるサイドウォール９と、シリコン基板１内に不純物を導入してなるソース・ドレイン領域４とを備えたＭＯＳトランジスタを形成する。そして、ＭＯＳトランジスタのソース・ドレイン領域４とゲート電極５との上に、スパッタ法により例えばチタン膜を堆積し、６００～９００℃で熱処理した後、H2 SO4 －H2 O2 混合液で未反応チタン膜を除去することにより、ソース・ドレイン領域４とゲート電極５との上にのみチタンシリサイド膜６を選択的に形成する。

【０００６】次に，図１５（ｂ）に示すように、基板の全面上に絶縁膜７を形成し、絶縁膜７にソース・ドレイン領域４のチタンシリサイド膜６に到達する接続孔８を開口する。

【０００７】次に、図１５（ｃ）に示すように、接続孔８内及び絶縁膜７の上にソース・ドレイン領域４上のチタンシリサイド膜６との接触特性を良好にするためのチタン膜、バリアメタルとしての窒化チタン膜をスパッタ法により堆積し、窒化チタン・チタン膜１９を形成する。

【０００８】次に、図１５（ｄ）に示すように、チタンをスパッタした後その上にアルミニウム合金を５００℃でスパッタすることにより、アルミニウム合金とチタンとが化合してなるＡｌ－Ｔｉ化合物層１５と、その上のアルミニウム合金膜１６とを形成する。その際、Ａｌ－Ｔｉ間の反応熱を利用することにより、接続孔８内をアルミニウム合金で埋め込む。そして、フォトリソグラフィ法により、窒化チタン・チタン膜１９、Ａｌ－Ｔｉ化合物層１５、アルミニウム合金１６をパターニングして、金属配線を形成する。

【０００９】

【発明が解決しようとする課題】しかしながら、半導体装置の微細化に応じて接続孔の径が微細化が進行すると、上記従来の方法において、図１５（ｃ）に示す工程で、窒化チタン・チタン膜１９をスパッタ法により堆積することは、以下の理由により好ましくない。

【００１０】　一般的に、スパッタ法で成膜した窒化チタン膜は段差被覆性がよくないので、接続孔上部の角でオーバーハング形状が形成されやすい。そのため、高温スパッタ時の接続孔内へのアルミニウム合金の流動を妨げ、接続孔が埋め込みにくくなる（例えばY.Takegawa他 Ext. Abst. SSDM,p.558, 1993）。

【００１１】　そこで、窒化チタン膜を形成する際に、N2 ガスを流しながらハニカム状のフィルタ（コリメータ）を通してチタンをスパッタすることによりオーバーハング形状の形成を抑制する方法もあるが、コリメータを使用するとパーティクルを発生しやすい。

【００１２】　また、図１５（ｂ）に示す工程で、接続孔８以外の部分（絶縁膜７上の部分　）も窒化チタン・チタン膜１９で覆われてしまうため、下地の違いを利用した選択ＣＶＤ法により接続孔８内にのみ選択的にアルミニウムやタングステン、銅等の金属を堆積するという方法を用いることができない。

【００１３】一方、上述のような問題を回避するために、絶縁膜に接続孔を形成した後、窒化チタン・チタン膜１９を堆積せずに、８５０℃程度のＮH3 雰囲気中で熱処理を行うことにより、チタンシリサイド膜の表面に窒化チタン膜を形成した後、選択ＣＶＤ法により接続孔内にのみ、選択的にアルミニウムを堆積する技術が提案されている（例えばH.Shinriki他 Ext. Abst. SSDM,p.968, 1994）。

【００１４】しかし、８００℃以上の熱処理をチタンシリサイド膜に加えると、ソース・ドレイン領域中のボロンがチタンシリサイド膜中に吸い上げられ、Ｐチャネルトランジスタの飽和電流値が低下するという虞れがある。また、金属シリサイドの種類によっては、高温で熱処理を行なうとシリサイドの凝集がおこり、ソース・ドレインのシート抵抗が増大する。そのため、上記従来の方法を適用し得るシリサイドの種類が限定される。

【００１５】また、以上のような不具合は、接続孔内の埋込層とシリサイド膜との間だけでなく、シリサイド膜の上に低抵抗の金属膜を形成しようとするときにも同じように生じるので、シリサイド膜と金属膜との積層構造における信頼性を悪化させる原因となっている。

【００１６】本発明は、金属シリサイド層とその上の金属膜との境界付近に窒素－酸素－金属－シリコン間化合物からなる化合物層が形成されると、半導体基板中に接合リークの原因となるような化合物の侵入が生じないという事実の発見に基づきなされたものであり、その目的は、このようなバリアとなる化合物層を形成することにより、バリアメタルを不要として埋込層やシリサイド膜と金属膜の積層構造における信頼性の向上を図りつつ、金属シリサイド膜全体のシート抵抗値を低く保ち、かつ接合リークの発生を防止し得る半導体装置およびその製造方法を提供することにある。

【００１７】

【課題を解決するための手段】上記目的を達成するために、本発明では、請求項１～９に記載されている半導体装置に関する手段と、請求項１２～２３に記載されている半導体装置の製造方法に関する手段とを講じている。

【００１８】本発明の半導体装置は、請求項１に記載されているように、半導体基板と、上記半導体基板の一部に形成され第１の金属がシリサイド化されてなる金属シリサイド膜と、上記金属シリサイド膜の上に形成された第２の金属からなる金属膜と、上記金属シリサイド膜の表面付近の領域に形成され、窒素－酸素－第１の金属－シリコン間化合物からなるバリア化合物層とを備えている。

【００１９】これにより、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層が形成されているので、金属膜を堆積する際などの

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製造工程中における高温履歴があっても、金属シリサイド膜を構成する第１の金属と金属膜を構成する第２の金属との反応が抑制されている。すなわち、窒化チタン・窒化膜等のバリアメタルを介在させなくても、接合リークの発生やゲート酸化膜の特性の劣化が抑制される。したがって、バリアメタルの段差被覆性や抵抗特性がよくないことに起因する不具合、例えば信頼性の低下やシート抵抗の増大を回避できる。

【００２０】請求項２に記載されているように、請求項１において、上記金属シリサイド膜全体の表面付近の領域に上記バリア化合物層が形成されていることが好ましい。

【００２１】これにより、半導体装置の製造工程が簡略化され、かつ金属シリサイド層の耐薬品性が向上するので、その結果製造コストも低減できることになる。

【００２２】請求項３，４に記載されているように、請求項１又は２において、上記バリア化合物層の厚みは、上記第２の金属の上記バリア化合物層への拡散を阻止するのに十分な厚み以上で上記金属シリサイド膜の厚みの３０％以下であることが好ましく、或いは別の観点からすると、２～２０ｎｍの範囲であることが好ましい。

【００２３】これにより、あまりに厚いバリア化合物層が形成されることによるコンタクト抵抗やシート抵抗の増大が可及的に抑制されることになる。

【００２４】請求項５に記載されているように、請求項１，２又は３において、上記バリア化合物層内における上記窒素の濃度が最大となる位置を上記酸素の濃度が最大となる位置よりも奥方に位置させることが好ましい。

【００２５】これにより、窒素濃度が高くなる位置では相対的に酸素濃度が低くなっていくので、特にコンタクト抵抗やシート抵抗の増大を招く酸化物層の濃度の高い領域をごく表面近傍に抑制することができる。したがって、金属膜とシリサイド膜との接触部におけるシート抵抗等の増大が可及的に抑制されることになる。

【００２６】請求項６に記載されているように、請求項１において、上記金属シリサイド膜の上に形成された絶縁膜と、上記絶縁膜の一部に形成され上記金属シリサイド膜に到達する接続孔とをさらに備え、上記金属膜を上記接続孔内に堆積された第２の金属からなる埋込層とすることができる。

【００２７】これにより、金属膜の表面付近の領域に第１の金属と第２の金属との反応を抑制するバリア化合物が存在しているので、接続孔にバリアメタルを形成する必要がなくなる。したがって、特に段差被覆性が要求される接続孔内の埋込層を構成する第２の金属としてカバレージの良好なものを選択することができ、半導体装置の信頼性が向上する。

【００２８】請求項７に記載されているように、請求項１において、上記金属シリサイド膜の上に形成された絶縁膜と、上記絶縁膜の一部に形成され上記金属シリサイド膜に到達する接続孔と、上記接続孔内に堆積された第３の金属からなる埋込層とをさらに備えることができる。

【００２９】これにより、第２の金属で構成される金属膜として電気抵抗の小さい材料を選択して埋込層と金属シリサイド膜との間に低抵抗層を介在させることができるので、コンタクト抵抗の小さい微細化に適した半導体装置が得られることになる。

【００３０】請求項８に記載されているように、請求項１，２，３，４，５，６又は７において、上記第１の金属を、チタン，コバルト，ニッケル，タンタル，タングステン，ニオブ，パラジウム，白金及びモリブデンのうち少なくともいずれか１つで構成することが好ましい。

【００３１】請求項９に記載されているように、請求項１，２，３，４，５，６又は７において、上記第２の金属を、アルミニウムを含む金属，銅を含む金属及びタングステンを含む金属のうち少なくともいずれか１つで構成することが好ましい。

【００３２】本発明の半導体装置の製造方法は、請求項１０に記載されているように、半導体基板上に、第１の金属とシリコンとの化合物からなる金属シリサイド膜を形成する第１の工程と、中性ないし酸化雰囲気下で、上記金属シリサイド膜の表面に窒素を含むイオンを照射して、上記金属シリサイド膜の表面付近の領域に窒素－酸素－第１の金属－シリコン間化合物からなるバリア化合物層を形成する第２の工程と、上記金属シリサイド膜の上記バリア化合物層の上に第２の金属を堆積して金属膜を形成する第３の工程とを備えている。

【００３３】この方法により、第２の工程において金属シリサイド膜の表面にバリア化合物層が形成されるので、第３の工程において、バリアメタルを形成することなく金属膜を形成することが可能となる。したがって、第２の金属として段差被覆性のよい材料を適宜選択して用いることにより、金属膜の下地に対する段差被覆性が向上し、信頼性の高い半導体装置を形成することができる。

【００３４】請求項１１に記載されているように、請求項１０において、上記第１の工程の後かつ上記第２の工程の前に、上記金属シリサイド膜の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記金属シリサイド膜に到達する接続孔を形成する工程とをさらに備え、上記第２の工程では、上記金属シリサイド膜の表面付近の領域のうち上記接続孔の底部に露出した領域に上記バリア化合物層を形成し、上記第３の工程では、上記接続孔内を上記第２の金属で埋め込むことができる。

【００３５】この方法により、バリア化合物層の形成領域が特に必要な領域に限定されるので、金属シリサイド膜のシート抵抗の増大が抑制される。

【００３６】請求項１２に記載されているように、請求

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項１０において、上記第２の工程の後に、上記金属シリサイド膜の上記バリア化合物層の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記バリア化合物層に到達する接続孔を形成する工程とをさらに備え、上記第３の工程では、上記接続孔内に上記第２の金属を堆積することができる。

【００３７】この方法により、金属シリサイド膜の任意の場所に各配線層からコンタクトを形成する際に、どの部位においてもバリア化合物層が形成されていることから、接続孔を形成するごとにバリア化合物層を形成する必要がないので、工程が簡略化される。また、金属シリサイド膜のＨＦ等の薬品に対する耐性も向上するので、後の工程上の制限が緩和されることになる。

【００３８】請求項１３に記載されているように、請求項１２において、上記第３の工程の後に、上記金属シリサイド膜の上記バリア化合物層の上に絶縁膜を形成する工程と、上記絶縁膜の一部を選択的に除去して上記バリア化合物層に到達する接続孔を形成する工程と、上記接続孔内に第３の金属を堆積して埋込層を形成する工程とをさらに備えることができる。

【００３９】この方法により、第２の金属として電気抵抗の小さい材料を選択すれば、金属シリサイド膜の上に低抵抗層が形成され、その上に埋込層が形成されるので、コンタクト抵抗の小さい特性の良好な半導体装置が得られることになる。

【００４０】請求項１４に記載されているように、請求項１０，１１，１２又は１３において、上記第２の工程では、チャンバ内に陰極である下部電極と陽極である上部電極とを配置したプラズマ発生装置を用い、上記チャンバ内において、上記半導体基板を上記下部電極上に載置した状態で上記金属シリサイド膜を窒素を含むガスのプラズマにさらすことにより上記バリア化合物層を形成することができる。

【００４１】この方法により、陰極上に半導体基板を設置することで窒素プラズマ中でプラスイオンとなっている窒素が効率的に金属シリサイド中に取り込まれる。

【００４２】請求項１５に記載されているように、請求項１０，１１，１２又は１３において、上記第２の工程では、上記金属シリサイド膜の表面を窒素を含むガスにさらしながら紫外線及び電離放射線のうちいずれか一方を照射することにより、上記バリア化合物層を形成することができる。

【００４３】請求項１６に記載されているように、請求項１０，１１，１２又は１３において、上記第２の工程では、上記金属シリサイド膜の表面を窒素を含むイオンビームにさらすことにより、上記バリア化合物層を形成することができる。

【００４４】請求項１７に記載されているように、請求項１０，１１，１２，１３，１４，１５又は１６において、上記第２の工程を５５０℃以下で行なうことが好ましい。

【００４５】この方法により、５５０℃以下の低温条件でプラズマ処理等が行なわれるので、チタンシリサイドなどを用いた場合でも金属シリサイドの凝集を招くことがなく、金属シリサイドの種類の選択幅が拡大される。

【００４６】請求項１８に記載されているように、請求項１０，１１，１２，１３，１４，１５又は１６において、上記第２の工程では、上記窒素を含むガスとしてＮ２ガスを用いることができる。

【００４７】この方法により、バリア化合物層を形成する際に、金属シリサイド膜の表面に存在する自然酸化膜を利用して、窒素－酸素－金属－シリコン間化合物からなるバリア化合物層が容易に形成される。

【００４８】請求項１９に記載されているように、請求項１０，１１，１２，１３，１４，１５，１６，１７又は１８において、上記第２の工程の前に、水素を含むガスを流すことにより、上記金属シリサイド膜上の自然酸化膜を除去する工程をさらに備え、上記第２の工程では、酸素を含むガスを添加することができる。

【００４９】この方法により、バリア化合物層内における酸素濃度が制御されるので、各元素の分布状態をより好ましい状態に調整することが可能となる。

【００５０】請求項２０に記載されているように、請求項１０，１１，１２，１３，１４，１５又は１６において、上記第２の工程では、窒素を含むイオンを３ｋｅＶ以下のイオンエネルギーで上記金属シリサイド膜内に導入することが好ましい。

【００５１】この方法により、バリア化合物層が形成される領域が金属シリサイド膜の表面から２０ｎｍ程度の深さまでに限定されるので、形成される半導体装置のコンタクト抵抗やシート抵抗の増大が抑制されることになる。

【００５２】請求項２１に記載されているように、請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０において、上記第１の工程では、金属シリサイド膜として、チタン，コバルト，ニッケル，タンタル，タングステン，パラジウム，白金及びモリブデンのうちいずれか１つのシリサイド膜を形成することが好ましい。

【００５３】請求項２２に記載されているように、請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０において、上記第３の工程では、ＣＶＤ法を用いてアルミニウムを含む金属，銅を含む金属及びタングステンを含む金属のうちいずれか１つを堆積することが好ましい。

【００５４】請求項２３に記載されているように、請求項１０，１１，１２，１３，１４，１５，１６，１７，１８，１９又は２０において、上記第３の工程では、チタン及びアルミニウム合金を連続的にスパッタすることにより、上記金属膜をＡｌ－Ｔｉ化合物層及びアルミニ

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ウム合金膜により構成することができる。
【００５５】これらの方法により、半導体装置の種類や金属シリサイド膜の上に形成される配線層の相違に応じた金属膜及び配線の形成方法の選択が可能となる。
【００５６】
【発明の実施の形態】
（第１の実施形態）図１（ａ）～（ｄ）は、第１の実施形態に係る半導体装置の製造工程を示す断面図である。
【００５７】まず、図１（ａ）に示すように、シリコン基板１上のフィールド酸化膜２により取り囲まれる活性領域の上に、シリコン酸化膜からなるゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、シリコン酸化膜からなるサイドウォール９と、シリコン基板１内に不純物を導入してなるソース・ドレイン領域４とを備えたＭＯＳトランジスタを形成する。そして、スパッタ法により、基板上に例えばチタン膜を堆積し、６５０℃で熱処理した後、H2 SO4 －H2 O2 混合液で未反応チタン膜を除去することにより、ソース・ドレイン領域４とゲート電極５との上にのみ、厚みが７０ｎｍ程度のチタンシリサイド膜６を選択的に形成する。その後、８５０℃で熱処理を行いチタンシリサイド膜を低抵抗化する。
【００５８】次に，図１（ｂ）に示すように、上記基板の全面上に厚みが８００ｎｍ程度の絶縁膜７を形成し、絶縁膜７にソース・ドレイン領域４のチタンシリサイド膜６に到達する接続孔８を開口する。
【００５９】次に、図１（ｃ）に示すように、平行平板電極を構成する陽極１０及び陰極１１と、ブロッキングコンデンサー１２と、高周波電源１３とを有するプラズマ発生装置を用い、プラズマ発生装置の反応室（図示せず）内に配置される陰極１１上に、図１（ｂ）までの工程を経た半導体装置を載置し、チタンシリサイド膜６の表面を窒素含有ガスのプラズマにさらす。例えば、温度５０℃にて、圧力８０ｍTorr の下で、１００％のN2 ガスを導入し、平行平板型電極１０，１１間に電力３００W程度の高周波電力を３００sec の間印加する。このとき、反応室内に窒素プラズマPlzが発生する。この窒素プラズマPlz中の窒素はN+ ，N2+等の陽イオンになっており、陰極１１方向にプラズマ電位約６０Ｖと自己バイアス電圧約２４０Ｖとを加算した合計３００Ｖの電位が発生する。そして、窒素イオンがこの電位で半導体装置の表面に引かれる。つまり、平行平板型電極１０，１１のうち陰極１１の上に半導体装置を設置することで、チタンシリサイド膜６表面への窒素の導入が促進されることとなる。この時、チタンシリサイド膜６の表面に形成されている自然酸化層中の酸素もチタンシリサイド層６内に取り込まれ、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４がチタンシリサイド膜６の表面付近に形成される。
【００６０】次に、図１（ｄ）に示すように、チタンを７５ｎｍ程度の厚み分だけスパッタした後、シリコン１％と銅０．５％を含むアルミニウム合金を５００℃で９００ｎｍ程度の厚み分だけスパッタすることにより、アルミニウム合金とチタンとが化合してなるＡｌ－Ｔｉ化合物層１５と、その上のアルミニウム合金膜１６とを形成する。その際、Ａｌ－Ｔｉ間の反応熱を利用することにより、接続孔８内をアルミニウム合金で埋め込んで埋込層を形成する。そして、フォトリソグラフィ法により、Ａｌ－Ｔｉ化合物層１５、アルミニウム合金膜１６をパターニングして、金属配線を形成する。
【００６１】なお、ゲート電極５上にも同時に接続孔を形成し（図１（ａ）～（ｄ）に示す断面とは別の断面で）、ゲート電極５上のチタンシリサイド膜６の表面付近にバリア化合物層１４を形成した後、Ａｌ－Ｔｉ化合物層１５、アルミニウム合金膜１６を堆積して埋込層及び金属配線を形成するようにしてもよい。
【００６２】図2は、上述の製造方法によって形成された半導体装置の断面構造を示すものである。すなわち、シリコン基板１上に、ゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、ソース・ドレイン領域４と、ソース・ドレイン領域４及びゲート電極５上に形成されたチタンシリサイド膜６と、サイドウォール９とを備えたＭＯＳトランジスタが形成されている。そして、基板上に形成された絶縁膜７にはソース・ドレイン領域４上のチタンシリサイド膜６に到達する接続孔８が形成されており、この接続孔８内及び絶縁膜７の上に埋込層及び金属配線を構成するＡｌ－Ｔｉ化合物層１５とアルミニウム合金膜１６とが形成されている。そして、本実施形態に係る半導体装置の特徴として、アルミニウム合金膜１６の下に窒化チタン・窒化膜等のバリアメタルは形成されておらず、代わりに、ソース・ドレイン領域４上のチタンシリサイド膜６のうち接続孔８の底面となる領域の表面のみに、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されている。
【００６３】次に、本実施形態で得られる半導体装置のバリア化合物層１４の構造の詳細と本実施形態の半導体装置におけるコンタクト抵抗等等の詳細とについて説明する。
【００６４】図９は、本実施形態における図１（ｃ）に示す工程を経た後のチタンシリサイド膜６の表面付近の領域をオージェ電子分光法によって分析した結果得られた各元素の濃度プロファイルを示す図である。ただし、オージェ電子分光法による分析の際各元素に対する感度が異なっているので、図９は各元素の組成比を正確に示すものではなく、各元素個々の濃度分布を示しているに過ぎない。図９に示されるように、表面から２～３ｎｍまではシリコンと酸素が特に多く存在しており、これは分析する過程でチタンシリサイド膜の表面に自然酸化膜としてＳｉO2膜が形成されたことによるものと考えられる。そして，ＳｉO2 膜の下方に８ｎｍ程度の範囲で

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窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層が形成されている。そして、表面付近のＳｉＯ２膜を除外してみると、表面のごく近傍に酸素濃度のピークが見られ、さらにＳｉO2 膜の下方４～５ｎｍ程度の深さ位置に窒素濃度のピークが見られる。

【００６５】このバリア化合物層１４内における各元素間の結合状態については、反応層が薄いため分析することはできなかったが、ＴｉＮ，ＴｉO２，Ｓi３Ｎ４，ＳｉO2 の標準生成熱は、順に、－７３．０ｋｃａｌ／ｍｏｌ、－２１８．０ｋｃａｌ／ｍｏｌ、－１７９．３、－２０２．５ｋｃａｌ／ｍｏｌであるところから、本実施形態のようにチタンシリサイド膜を用いた場合は、酸素はチタン、シリコンと結合しており、窒素は主としてシリコンと結合していると考えられる。

【００６６】このバリア化合物層１４を形成した結果、シート抵抗は２．６Ω／□から２．９Ω／□に増加したが、増加の割合は１０％程度であり、トランジスタ動作等には特に問題のない十分低い値である。本実施形態では、接続孔８内のチタンシリサイド膜表面のみに、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されているだけなので、チタンシリサイド６の上記窒素プラズマ処理によるシート抵抗の上昇率はさらに小さくなる。

【００６７】図１０は、図１（ｃ）に示す窒素プラズマ処理を行なわない試料、本実施形態の処理を行なった試料、及び図１５に示す従来の方法で製造されたリファレンスの試料（ＴｉＮ・Ｔｉ膜からなるバリアメタルを有し高温スパッタを行なっていない試料）についての接合リーク特性を比較する図である。ただし、面積が８０００μm2 のN+ Ｐ接合部に５．５Ｖの逆方向電圧を印加したときの接合リーク特性を示す。同図に示されるように、窒素プラズマ処理を行わなかった試料では接合リークが大きい。これは、図１（ｄ）に示す工程で、５００℃でアルミニウム合金をスパッタする際に、アルミニウム合金膜１６ないしはＡｌ－Ｔｉ化合物層１５がチタンシリサイド膜６と反応して，シリコン基板１中にアルミニウムが侵入し、接合リークが発生しているものと考えられる。これに対し、本実施形態による窒素プラズマ処理を行った試料の接合リークは、バリアメタルを有しないにも拘らず、バリアメタルを有し高温スパッタを行わなかったリファレンスの試料の接合リークと同等であることがわかる。これは、アルミニウム合金を５００℃でスパッタする際に、アルミニウム合金膜１６ないしはＡｌ－Ｔｉ化合物層１５がチタンシリサイド膜６と反応するのをバリア化合物層１４が阻止しているためと考えられる。

【００６８】また、本実施形態におけるN+ 拡散領域に対するコンタクト抵抗は、１．０μm角のコンタクト形状を有し窒素プラズマ処理を行なった試料で１５Ωであり、リファレンスの試料のコンタクト抵抗は５Ωである。本実施形態に係る試料のコンタクト抵抗はやや高いが、トランジスタの動作等には特に不具合は生ぜず、シリコン基板との電気的接続も十分とれていることがわかる。

【００６９】図１１は、窒素プラズマ処理を行なった後Ａｌ合金を堆積してアニール処理を行なった各種試料のシート抵抗のアニール温度依存性を示す図である。処理条件は、厚みが７０ｎｍのチタンシリサイド膜上に、図１（ｃ）に示す窒素プラズマ処理を行ない、さらにＡｌ－１％Ｓｉ－０．５％Ｃｕ合金を２００ｎｍの厚み分だけ堆積した後、３０分間アニールしている。試料には、窒素プラズマ処理を行なわなかったものと、２０sec の間窒素プラズマ処理を行なったものと、６０sec の間窒素プラズマ処理を行なったものと、３００sec の間窒素プラズマ処理を行なったものとがある。同図に示されるように、窒素プラズマ処理を６０sec 間行ったものと窒素プラズマ処理を３００sec 間行ったものでは、５３０℃でアニールした時のシート抵抗の上昇が抑制されていることがわかる。この図からも、チタンシリサイド膜表面に形成した窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層が、アルミニウム合金とチタンシリサイド膜との反応を抑制する効果があることがわかる。

【００７０】以上のように、本実施形態によれば、金属シリサイドの表面に窒素プラズマ処理を行なって、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成するようにしたので、その後の工程の熱処理により金属シリサイド膜とアルミニウム合金との反応により生じた金属のシリコン基板中への侵入を有効に阻止できる。つまり、従来の方法のごとくアルミニウム合金膜等からなる埋込層と金属シリサイドとの間に窒化チタン・窒化膜等のバリアメタルを介在させることなく、接合リークの発生を抑制できる。したがって、バリアメタルを設けた場合のような埋込層の信頼性の悪化を回避できる。しかも、コンタクト抵抗は実用的に十分低く抑制することができ、金属シリサイド膜自体のシート抵抗も十分低く保つことができる。

【００７１】また、ゲート電極５上の金属シリサイド膜の表面付近に領域にバリア化合物層を形成した場合にも、ゲート電極中に金属が侵入するのを阻止できるので、ゲート酸化膜の特性の劣化等を有効に阻止することができる。

【００７２】特に、本実施形態では、５５０℃以下の低い温度で窒素プラズマ処理を行なっているので、多種類の金属シリサイドについて金属シリサイド膜の凝集を生じることがない、つまり、金属シリサイドを構成する金属材料の選択の幅の拡大を図ることができる利点がある。

【００７３】（第２の実施形態）次に、第２の実施形態

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について説明する。本実施形態では、製造工程の図示は省略するが、上述の第１の実施形態における図１（ａ）～（ｃ）と同じ処理を行なった後、選択的ＣＶＤ法により、接続孔８内に埋込層となるタングステン膜１７を堆積する。そして、タングステン膜１７及び絶縁膜７の上にアルミニウム合金膜１６を堆積した後、これをパターニングして金属配線を形成する。

【００７４】図３は、本実施形態により形成された半導体装置の構造を示す断面図である。上記第１の実施形態では、Ａｌ－Ｔｉ化合物層１５とアルミニウム合金膜１６とによって埋込層及び金属配線が一体的に構成されていたが、本実施形態では、タングステン膜１７により埋込層が構成され、アルミニウム合金膜１６により金属配線が構成されている。そして、ソース・ドレイン領域４上のチタンシリサイド膜６のうち接続孔８の底面の部分のみに窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されていて、タングステン膜１７とチタンシリサイド膜６とがこのバリア化合物層１４を介して接触している。つまり、本実施形態の半導体装置は、埋込層と金属配線とが異なる材料で構成されている点のみが第１の実施形態の半導体装置と異なり、他の部分は第１の実施形態の半導体装置と同じ構造を有する。したがって、上記第１の実施形態と基本的には同様の効果を発揮することができる。

【００７５】加えて、本実施形態の半導体装置においては、埋込層がタングステン膜１７で構成されているので、半導体装置の接合リークをもたらす反応の生じる温度がアルミニウム合金膜等の場合よりも高くなる。本実施形態では、バリア化合物層１４により、その後の６００℃以上の熱処理でチタンシリサイドとタングステンとが反応してシリコン基板中に金属が侵入し、接合リークが発生するのを防止することができる。

【００７６】（第３の実施形態）次に、第３の実施形態について説明する。図４（ａ）～（ｄ）は、本実施形態の半導体装置の製造工程を示す断面図である。

【００７７】まず、図４（ａ）に示すように、シリコン基板１上のフィールド酸化膜２により取り囲まれる活性領域の上に、シリコン酸化膜からなるゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、シリコン酸化膜からなるサイドウォール９と、シリコン基板１内に不純物を導入してなるソース・ドレイン領域４とを備えたＭＯＳトランジスタを形成する。そして、スパッタ法により、基板上に例えばチタン膜を堆積し、６５０℃で熱処理した後、H2 SO4 －H2 O2 混合液で未反応チタン膜を除去することにより、ソース・ドレイン領域４とゲート電極５との上にのみ、厚みが７０ｎｍ程度のチタンシリサイド膜６を選択的に形成する。その後、８５０℃で熱処理を行いチタンシリサイド膜を低抵抗化する。

【００７８】次に、図４（ｂ）に示すように、平行平板電極を構成する陽極１０及び陰極１１と、直流電源１８とを有するプラズマ発生装置を用い、プラズマ発生装置の反応室（図示せず）内に配置される陰極１１上に半導体装置を載置し、チタンシリサイド膜６の表面を窒素ガス等の窒素含有ガスのプラズマにさらす。すると、上記第１の実施形態と同様に、チタンシリサイド膜６の表面に形成されている自然酸化膜中の酸素もチタンシリサイド膜６内に取り込まれ、N2 ガスのプラズマによってチタンシリサイド膜６全体の表面付近に窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成される。

【００７９】次に，図４（ｃ）に示すように、上記基板の全面上に厚みが８００ｎｍ程度の絶縁膜７を形成し、絶縁膜７にソース・ドレイン領域４のチタンシリサイド膜６に到達する接続孔８を開口する。

【００８０】次に、図４（ｄ）に示すように、スパッタ装置にて、チタンを７５ｎｍ程度の厚み分だけスパッタした後、シリコン１％と銅０．５％を含むアルミニウム合金を５００℃で９００ｎｍ程度の厚み分だけスパッタすることにより、アルミニウム合金とチタンとが化合してなるＡｌ－Ｔｉ化合物層１５と、その上のアルミニウム合金膜１６とを形成する。その際、Ａｌ－Ｔｉ間の反応熱を利用することにより、接続孔８内をアルミニウム合金で埋め込んで埋込層を形成する。そして、フォトリソグラフィ法により、Ａｌ－Ｔｉ化合物層１５、アルミニウム合金膜１６をパターニングして、金属配線を形成する。

【００８１】図５は、上述の製造方法によって形成された半導体装置の断面構造を示すものである。すなわち、シリコン基板１上に、ゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、ソース・ドレイン領域４と、ソース・ドレイン領域４とゲート電極５との上に形成されたチタンシリサイド膜６と、サイドウォール９とを備えたＭＯＳトランジスタが形成されている。そして、チタンシリサイド膜６の全面上に窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されている。そして、基板上に形成された絶縁膜７にはソース・ドレイン領域４上のチタンシリサイド膜６に到達する接続孔８が形成されており、この接続孔８内及び絶縁膜７の上に埋込層及び金属配線を構成するＡｌ－Ｔｉ化合物層１５とアルミニウム合金膜１６とが形成されている。つまり、上記第１の実施形態の半導体装置においては、ソース・ドレイン領域４上のチタンシリサイド膜６のうち接続孔８の底面となる領域の表面のみに、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されていたが、本実施形態の半導体装置においては、ソース・ドレイン領域４及びゲート電極５の上のチタンシリサイド膜６の全面上にバリア化合物層１４が形成されている点に特徴がある。

【００８２】本実施形態においても、チタンシリサイド

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膜６の表面付近の領域に窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４が形成されているので、上記第１の実施形態と同様の効果が得られる。特に、本実施形態の方法では、ソース・ドレイン領域４だけでなくゲート電極５上のチタンシリサイド膜６の表面付近の領域にもバリア化合物層１４が形成されているので、図４（ｄ）に示すＡｌ－Ｔｉ化合物層１５及びアルミニウム合金膜１６とは別の配線層からゲート電極５にコンタクト部を形成する際にも、再度窒素プラズマ処理を行なわなくても、バリア化合物層１４を介してコンタクトすることができる利点がある。

【００８３】また、図４（ｄ）に示す工程の前つまり半導体装置をスパッタ装置内に入れる前に、接続孔８内をＨＦ溶液でウエットエッチングし、金属シリサイドの表面酸化層を除去する必要があるが、チタンシリサイド膜６はＨＦ溶液でエッチングされやすい。その点、本実施形態では、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層１４はシリコンと窒素の結合を含んでいるためＳｉＮに近い組成を有しているものと思われ、ＨＦ溶液でエッチングされにくいと考えられる。そのため、本実施形態ではチタンシリサイド膜の対薬品性が向上し、プロセスの余裕度が増すという利点もある。

【００８４】ただし、本実施形態の半導体装置においては、チタンシリサイド膜６の表面全面にバリア化合物層１４が形成されるため、第１の実施形態の半導体装置よりは、チタンシリサイド膜６のシート抵抗上昇は大きくなる。しかし、第１の実施形態で述べたようにその場合でもシート抵抗の増加割合は１０％程度であり、トランジスタ動作等には特に問題のない十分低い値である。

【００８５】（第４の実施形態）次に、第４の実施形態について説明する。本実施形態では、製造工程の図示は省略するが、上述の第３の実施形態における図３（ａ）～（ｃ）と同じ処理を行なった後、選択的ＣＶＤ法により、接続孔８内に埋込層となるタングステン膜１７を堆積する。そして、タングステン膜１７及び絶縁膜７の上にアルミニウム合金膜１６を堆積した後、これをパターニングして金属配線を形成する。

【００８６】図６は、本実施形態により形成された半導体装置の構造を示す断面図である。上記第３の実施形態では、Ａｌ－Ｔｉ化合物層１５とアルミニウム合金膜１６とによって埋込層及び金属配線が一体的に構成されていたが、本実施形態では、タングステン膜１７により埋込層が構成され、アルミニウム合金膜１６により金属配線が構成されている。そして、ソース・ドレイン領域４及びゲート電極５の上のチタンシリサイド膜６の全面上に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層１４が形成されていて、タングステン膜１７とチタンシリサイド膜６とがこのバリア化合物層１４を介して接触している。つまり、本実施形態の半導体装置は、埋込層と金属配線とが異なる材料で構成されている点のみが第３の実施形態の半導体装置と異なり、他の部分は第３の実施形態の半導体装置と同じ構造を有する。したがって、上記第３の実施形態と基本的には同様の効果を発揮することができる。

【００８７】加えて、本実施形態の半導体装置においては、埋込層がタングステン膜１７で構成されているので、バリア化合物層１７により、タングステンとチタンシリサイドとの反応を防止すればよい。したがって、その後の６００℃以上の熱処理でチタンシリサイドとタングステンとが反応してシリコン基板中に金属が侵入し、接合リークが発生するのを防止することができる。

【００８８】（第５の実施形態）次に、第５の実施形態について説明する。図７（ａ）～（ｄ）は、本実施形態の半導体装置の製造工程を示す断面図である。

【００８９】まず、図７（ａ）に示すように、シリコン基板１上のフィールド酸化膜２により取り囲まれる活性領域の上に、シリコン酸化膜からなるゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、シリコン酸化膜からなるサイドウォール９と、シリコン基板１内に不純物を導入してなるソース・ドレイン領域４とを備えたＭＯＳトランジスタを形成する。そして、スパッタ法により、基板上に例えばコバルト膜を堆積し、窒素雰囲気中５００℃で熱処理した後、H2 SO4 －H2 O2 混合液で未反応コバルト膜を除去することにより、ソース・ドレイン領域４とゲート電極５との上にのみ、厚みが５０ｎｍ程度のコバルトシリサイド膜２４を選択的に形成する。その後、８５０℃で熱処理を行いコバルトシリサイド膜２４を低抵抗化する。

【００９０】次に、図７（ｂ）に示すように、平行平板電極を構成する上部電極２９及び下部電極２６と、ハイパスフィルター２７と、ローパスフィルター２８と、１３．５６ＭＨｚの高周波電源２９と、４００ＫＨｚの高周波電源３０とを有するプラズマ発生装置を用い、プラズマ発生装置の反応室（図示せず）内に配置される下部電極２６の上に半導体装置を載置し、コバルトシリサイド膜２４の表面を窒素ガス等の窒素含有ガスのプラズマにさらす。例えば温度４００℃，圧力２Torrの下で、１００％のN2 ガスを導入し、上部電極２５に高周波電源２９により８０Wの高周波電力を、下部電極２６に高周波電源３０により１００Wの高周波電力を９００secの間印加する。このとき、反応室内に窒素プラズマＰlzが発生する。この窒素プラズマＰlz中の窒素はN+ ，Ｎ2+等の陽イオンになっており、下部電極２６の方が周波数が低いため、下部電極２５の方向に窒素イオンが引かれる。つまり、２周波数電力加式のプラズマ発生装置を使用しても、低周波数側の電力が印加される電極の上に半導体装置を設置することで、コバルトシリサイド膜２４表面への窒素の導入が促進されることとなる。この時、コバルトシリサイド膜２４の表面に形成されている自然酸化層中の酸素ないしチャンバに残存していた酸素

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もコバルトシリサイド層２４内に取り込まれ、窒素－酸素－コバルト－シリコン間化合物からなるバリア化合物層１４がコバルトシリサイド膜２４の表面付近に形成される。

【００９１】次に、図7（ｃ）に示すように、ＤＭＡＨ（ジメチルアルミニウムハイドライド）を用いた選択ＣＶＤ法により、バリア化合物層１４の上のみに第１のアルミニウム膜２２を形成する。ＤＭＡＨを用いた選択ＣＶＤ法は導電層の上のみに選択的にアルミニウム膜を堆積できる方法である。

【００９２】次に，図7（ｄ）に示すように、第１のアルミニウム膜２２の上に厚みが８００ｎｍ程度の絶縁膜７を形成し、絶縁膜7にソース・ドレイン領域４上の第１のアルミニウム膜２２に到達する接続孔８を開口する。

【００９３】次に、図7（ｅ）に示すように、ＤＭＡＨを用いた選択ＣＶＤ法により、接続孔８内に第２のアルミニウム膜２３を形成する。さらに、スパッタ法により、第２のアルミニウム膜２３及び絶縁膜7の上にアルミニウム合金膜１６を堆積し、フォトリソグラフィ法により、アルミニウム合金膜１６をパターニングして、金属配線を形成する。

【００９４】図8は、上述の製造方法によって形成された半導体装置の断面構造を示すものである。すなわち、シリコン基板１上に、ゲート酸化膜３と、ポリシリコン膜からなるゲート電極５と、ソース・ドレイン領域４と、ソース・ドレイン領域４及びゲート電極５上に形成されたコバルトシリサイド膜２４と、サイドウォール９とを備えたＭＯＳトランジスタが形成されている。そして、コバルトシリサイド膜２４の全面上に窒素－酸素－コバルト－シリコン間化合物からなるバリア化合物層１４が形成され、さらにコバルトシリサイド膜２４のバリア化合物層１４の上に第１のアルミニウム膜２２が形成されている。そして、基板上に形成された絶縁膜７にはソース・ドレイン領域４上の第１のアルミニウム膜２２に到達する接続孔８が形成されており、この接続孔８内に埋込層としての第２のアルミニウム膜２３が形成されている。また、第２のアルミニウム膜２３及び絶縁膜７の上に金属配線を構成するアルミニウム合金膜１６が形成されている。つまり、本実施形態の半導体装置においては、ソース・ドレイン領域４及びゲート電極５の上のコバルトシリサイド膜２４の全面上にバリア化合物層１４が形成されているとともに、コバルトシリサイド膜２４の上に電気抵抗の低いアルミニウム膜（低抵抗層）が形成されている点に特徴がある。

【００９５】次に、本実施形態で得られる半導体装置のバリア化合物層１４の構造の詳細と、本実施形態の半導体装置における第１のアルミニウム膜２２の反応防止効果の詳細とについて説明する。

【００９６】図１２（ａ）～（ｃ）は、プラズマ処理されていないコバルトシリサイド膜，N2 ガス中でプラズマ処理されたコバルトシリサイド膜及びNH3 ガス中でプラズマ処理されたコバルトシリサイド膜について、それぞれの表面付近の領域をＸＰＳ法によって分析した結果得られた各元素の濃度プロファイルを示す図である。ただし、図１２（ａ）～（ｃ）において、横軸は表面からの深さを、縦軸は各元素の組成比を示している。プラズマ処理されていないコバルトシリサイド膜でも、シリサイド形成時に窒素雰囲気中で７５０℃の熱処理が行われるので、その表面付近に窒素が導入されているが、窒素濃度のピークは表面位置にあり、その後窒素濃度が減少して約２ｎｍの深さ位置において窒素がなくなっている。また、酸素濃度も約２ｎｍの深さ位置でほとんど無視できるぐらいまで小さくなっている。それに対し、Ｎ２ ガス中或いはNH3 ガス中でプラズマ処理されたコバルトシリサイド膜においては、その表面から２ｎｍ程度奥方に入った深さ位置に窒素濃度のピークがみられる。また、酸素濃度の濃い領域も、その表面から約６ｎｍの深さ位置にまで及んでいる。すなわち、窒素雰囲気中でプラズマ処理が行われたコバルトシリサイド膜においては、その表面から約６ｎｍの深さ位置に亘って窒素－酸素－コバルト－シリコン間化合物からなるバリア化合物層が形成されていることがわかる。

【００９７】本実施形態では、コバルトシリサイド膜２４の表面付近にバリア化合物層１４を形成した結果、コバルトシリサイド膜２４の電気抵抗が３．５Ω／□から３．６Ω／□に増大したが、その増加割合は１０％以下であり、トランジスタの動作等には特に問題のない十分低い値である。

【００９８】図１３は、コバルトシリサイド膜の上に第１のアルミニウム膜２２としてＡｌ－０．５％Ｃｕ膜を堆積してアニール処理を行った結果得られた各種試料のシート抵抗のアニール温度依存性を示す図であり、コバルトシリサイド膜には、９００sec の間N2 ガス中でプラズマ処理されたものと、９００sec の間NH3 ガス中でプラズマ処理されたものと、プラズマ処理されなかったものとがある。プラズマ処理は、厚みが５０ｎｍのコバルトシリサイド膜に、９００sec の間、N2ガス又はNH3 ガス中で窒素プラズマを照射することにより行われた。そして、いずれの試料についても、コバルトシリサイド膜の上にＡｌ－０．５％Ｃｕ合金膜が約２００ｎｍの厚みで堆積されており、その後、約３０分間アニールされている。

【００９９】同図を参照するとわかるように、プラズマ処理されていない試料では、４００℃でアニールされたときのシート抵抗値の増大はそれほどでないものの４３０℃でアニールされたときのシート抵抗値は著しく増大している。それに対し、プラズマ処理された試料は、いずれも４００℃，４３０℃でアニールされても抵抗値の増大が抑制されている。すなわち、コバルトシリサイド

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膜の表面に形成されたバリア化合物層により、アルミニウム膜とコバルトシリサイド膜との反応が抑制されていることがわかる。一般に、シンターは４００～４５０℃程度で行われるので、このようなシート抵抗値の抑制効果は、実用上重要な意義がある。

【０１００】また、４３０℃でアニールされた試料をＸＰＳ分析した結果、窒素プラズマ処理されていないものは、Ｃｏ2 Ａｌ19又はＣｏ4 Ａ13 合金が形成されていたのに対し、窒素プラズマ処理された試料では、ＡｌとＣｏＳｉ2 のピークしか見られなかった。つまり、Ｘ線分析からも窒素プラズマ処理によりＡｌとＣｏＳｉ2との反応が４３０℃まで抑制されていることがわかった。

【０１０１】以上のように、本実施形態によれば、金属シリサイドの表面に窒素プラズマ処理を行って、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成するようにしたので、その後の工程の熱処理により金属シリサイド膜とアルミニウム合金との反応により生じた金属のシリコン基板中への進入を有効に阻止できる。つまり、従来の方法のごとく８００℃以上の熱処理をシリサイド膜に加えてバリア化合物層を形成する必要がないので、ソース・ドレイン領域中のボロンが金属シリサイド膜中に吸い上げられ、Ｐチャネルトランジスタの飽和電流値が低下するという問題がない。また、５５０℃以下の低い温度で窒素プラズマ処理を行っているので、多種類の金属シリサイドについても金属シリサイド膜の凝集を生じることがないという効果をることができる。つまり、金属シリサイドを構成する金属材料の選択の幅の拡大を図ることができるのである。

【０１０２】（他の実施形態）上記第１又は第３の実施形態において、アルミニウム合金膜１６とＡｌ－Ｔｉ化合物層１５から接続孔８上の金属配線を形成しているが、Ａｌ－Ｔｉ化合物層１５は別の金属膜ないしはその化合物でもよく、あるいは設けなくてもよい。さらに、他の金属膜をアルミニウム合金膜１６上に積層してもよい。また、アルミニウム合金膜１６として、シリコンと銅を含むアルミニウム合金を用いたが、シリコンのみやスカンジウムなど他の金属を含む他のアルミニウム合金や純アルミニウムを用いてもよい。また、アルミニウム合金の代わりに銅または銅合金を用いてもよい。

【０１０３】上記各実施形態では、窒素を含むガスとしてN2 ガスを用いたが、まず、NH3 ガスやH2 ガスを流して金属シリサイド膜の表面の自然酸化膜を除去し、その後、N2 ガスに微量のO2 ガスを加えた雰囲気の中でプラズマを発生させて、窒素－酸素－チタン－シリコン間化合物からなるバリア化合物層を形成してもよい。その場合、酸素量をコントロールできるので、バリア化合物層内の各元素の分布をできるだけ最適状態に近付けることができ、自然酸化膜を利用するよりもさらにコンタクト抵抗の低いかつ接合リーク防止効果の高いバリア化合物層を有する半導体装置を形成することができる。

【０１０４】また、NH3 ガスを用いてプラズマ処理を行なう場合でも、５５０℃以下でプラズマ処理を行なうことにより、上記従来の８００℃程度の条件下でプラズマ処理を行なって窒化チタンを形成する場合のような不具合は生じない。さらに、NH3 ガスを用いてプラズマ処理を行なう場合でも、自然酸化膜を利用して窒素－酸素－チタン等の金属－シリコン間化合物からなるバリア化合物層を形成することができる条件下であれば、本発明の効果を発揮することは可能である。

【０１０５】図１４は、NH3 ガスを用いてコバルトシリサイド表面をプラズマ処理した場合にシリサイド表面に形成されるバリア化合物層を示すＴＥＭ写真図である。プラズマ発生条件は第５の実施形態で述べたN2 ガスのプラズマ発生条件と同じである。約４－６ｎｍ厚みの窒素－酸素－コバルト－シリコン間化合物層（アモルファス層）が形成されていることがわかる。また、すでに述べた図１３のデータに示されるように、熱処理の際のアルミニウムとコバルトシリサイドとの反応によるシート抵抗の上昇が４３０℃まで抑制されており、N2 ガスを用いた場合と同じ程度の反応抑制効果があることがわかる。その理由は、すでに説明した図１２に示されるように、NH3 ガスを用いると、窒素－酸素－コバルト－シリコン間化合物層中の酸素の組成比が低減され、窒素の組成比が高くなっており、両者の組成比が適度に調整されることによるものと推定される。

【０１０６】なお、プラズマ形成の条件としては、上記各実施形態における条件以外の他の条件を用いることができることはいうまでもない。

【０１０７】上記各実施形態において、チタンシリサイド膜又はコバルトシリサイド膜の表面を窒素プラズマ処理して窒素－酸素－シリコン間化合物層を形成する工程は、スパッタ装置ないしは選択ＣＶＤ装置内で、接続孔内に銅、アルミニウム、タングステンないしはその合金を堆積させる直前に同一装置内でおこなってもよいし、あるいは、バリア化合物層の上のみに銅，アルミニウム，タングステンないしはその合金を選択ＣＶＤ法で形成する直前に同一装置内で行ってもよい。

【０１０８】また、上記各実施形態において、金属シリサイド膜としてチタンシリサイドを用いたが、コバルトシリサイド，ニッケルシリサイド，タンタルシリサイド，タングステンシリサイド，ニオブシリサイド，パラジウムシリサイド，白金シリサイド及びモリブデンシリサイド等を用いてもよい。

【０１０９】また、上記各実施形態において、窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成する工程において、金属シリサイド膜の表面を窒素を含むガスのプラズマにさらす代わりに、金属シリサイド膜の表面を窒素を含むガスにさらすと同時に紫外線や電離放射線を照射することにより、紫外線等のエネルギ

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ーを利用して、温度５５０℃以下の低温で、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成してもよい。あるいは、プラズマを使用する代わりに、金属シリサイド膜の表面を窒素を含むイオンビームにさらすことにより、イオンのエネルギーを利用して、温度５５０℃以下の低温で、金属シリサイド膜の表面に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成してもよい。

【０１１０】なお、第１～第４の実施形態において、窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成する工程において、プラズマ処理、紫外線線等の照射、イオンビームの照射などのいずれを選択する場合にも、窒素イオンを金属シリサイド側に引き寄せるための電位は、３ｋｅＶ程度以下であることが好ましい。その理由について説明する。一般的に、シリコン中における窒素イオンの飛程から類推すると、電位が１ｋｅＶの場合には、シリコン中の窒素濃度は深さ３．８ｎｍの部位でピークとなり、深さ９．８ｎｍの部位で１０％まで減小する。そして、電位が３ｋｅＶの場合には、シリコン中の窒素濃度は深さ８．５ｎｍの部位でピークとなり、深さ２０．３ｎｍの部位で１０％まで減小する。したがって、通常７０ｎｍ程度の厚みのシリサイド膜のうち３０％に相当する２０ｎｍ程度の深さまでにバリア化合物層の形成を抑えておくことで、シート抵抗やコンタクト抵抗の増大を回避できる。

【０１１１】また、本発明のバリア化合物層が形成される金属シリサイド膜は上記各実施形態に示すゲート電極やソース・ドレイン領域上に限定されるものではない。例えば、ポリシリコン膜を抵抗やコンデンサの構成要素（特に電極）として利用する際にも、ポリシリコン膜上のシリサイド膜が形成されることがあり、その場合にも、上層配線とコンタクトする金属シリサイド膜の表面に本発明の窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成することにより、接続孔内にバリアメタルを堆積しなくても、埋込層と金属シリサイド層との反応で生じた金属等が電極中あるいは電極を介して他の部材中に侵入するのを有効に防止することができる利点がある。

【０１１２】また、第５の実施形態では、ソース・ドレイン領域４及びゲート電極５の上のコバルトシリサイド膜２４の全面上に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層１４が形成されていて、第１のアルミニウム膜２２とチタンシリサイド膜６とがこのバリア化合物層１４を介して接触しているが、第１のアルミニウム膜２２の代わりに、アルミニウムを含む金属，銅を含む金属及びタングステンを含む金属からなる膜が堆積された場合にも同じ効果が得られる。例えば第１のアルミニウム膜２２の代わりにタングステン膜が用いられた場合でも、バリア化合物層１４の存在によって、その後の６００℃以上の熱処理でコバルトシリサイドとタングステンとが反応してシリコン基板中に金属が進入し、接合リークが生じるのを有効に防止することができる。

【０１１３】

【発明の効果】以上説明したように、本発明によれば、金属シリサイド上の絶縁膜に形成される接続孔内の埋込層を介して金属シリサイド膜と上層の配線とが電気的に接続される半導体装置において、少なくとも接続孔の底面となる金属シリサイド膜の表面付近の領域に窒素－酸素－金属－シリコン間化合物からなるバリア化合物層を形成するようにしたので、接続孔内にバリアメタルを堆積することによる信頼性の低下を招くことなく、半導体基板等への化合物の侵入を阻止することができ、よって、金属シリサイド膜全体のシート抵抗値を低く保ち、かつ接合リークを抑制し得ると共に接続孔内への埋込層の信頼性の高い半導体装置およびその製造方法を提供することができる。

【図面の簡単な説明】

）

【図１】第１の実施形態における半導体装置の製造工程を示す断面図である。

【図２】第１の実施形態における半導体装置の断面図である。

【図３】第２の実施形態における半導体装置の断面図である。

【図４】第３の実施形態における半導体装置の製造工程を示す断面図である。

【図５】第３の実施形態における半導体装置の断面図である。

【図６】第４の実施形態における半導体装置の断面図である。

【図７】第５の実施形態における半導体装置の製造工程を示す断面図である。

【図８】第５の実施形態における半導体装置の断面図である。

【図９】第１の実施形態における半導体装置のチタンシリサイド膜表面の深さ方向の元素分析結果を示す図である。

【図１０】窒素プラズマ処理を行なわない試料、第１の実施形態の処理を行なった試料、及びリファレンスの試料についての接合リーク特性を比較する図である。

【図１１】窒素プラズマ処理を行なった後Ａｌ合金を堆積してアニール処理を行なった各種試料のシート抵抗のアニール温度依存性を示す図である。

【図１２】プラズマ窒化処理を行わない場合、N2 ガス雰囲気でプラズマ窒化処理を行った場合、ＮH3 ガス雰囲気でプラズマ窒化処理を行った場合におけるＣｏＳｉ2膜の表面付近をＸＰＳ分析した結果得られた各元素の組成比をそれぞれ示す図である。

【図１３】プラズマ窒化処理を行わない場合、N2 ガス

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雰囲気でプラズマ窒化処理を行った場合、ＮＨ3 ガス雰囲気でプラズマ窒化処理を行った場合におけるＡｌＣｕ／ＣｏＳｉ2 構造のシート抵抗の温度依存性を示す図である。

【図１４】ＮＨ3 ガス雰囲気でプラズマ窒化処理を行った場合におけるＡｌＣｕ／ＣｏＳｉ2 構造の境界付近におけるＴＥＭ写真図である。

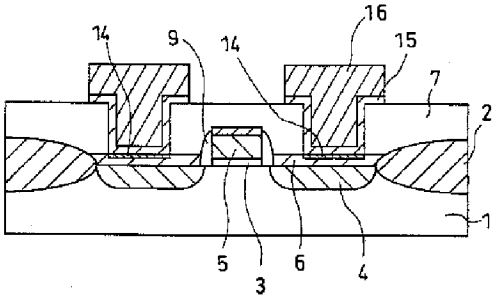
【図１５】従来の半導体装置の製造工程を示す断面図である。

【符号の説明】

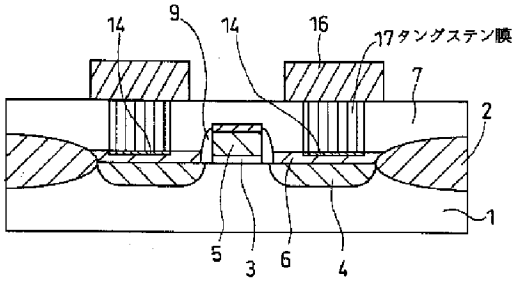
１	シリコン基板
２	フィールド酸化膜
３	ゲート酸化膜
４	ソース・ドレイン領域
５	ゲート電極
６	チタンシリサイド膜
７	絶縁膜
８	接続孔
９	サイドウォール
１０	陽極
１１	陰極
１２	ブロッキングコンデンサー
１３	高周波電源
１４	バリア化合物層
１５	Ａｌ－Ｔｉ化合物層
１６	アルミニウム合金膜
１７	タングステン膜
１８	直流電源
Ｐｌｚ	窒素プラズマ
２２	第１のアルミニウム膜
２３	第２のアルミニウム膜
２４	コバルトシリサイド膜
２５	上部電極
２６	下部電極
２７	ハイパスフィルター
２８	ローパスフィルター
２９	高周波電源
３０	高周波電源

【図１】

【図２】

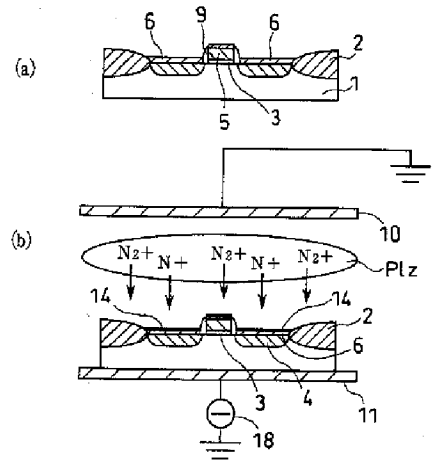


【図３】

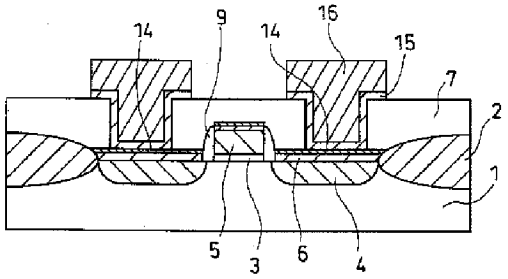


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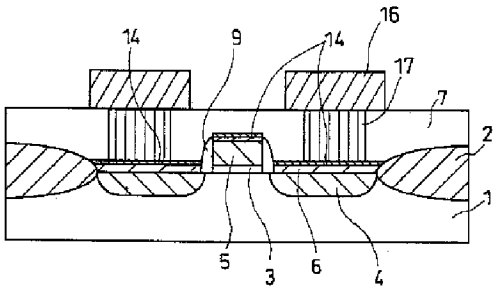
【図4】



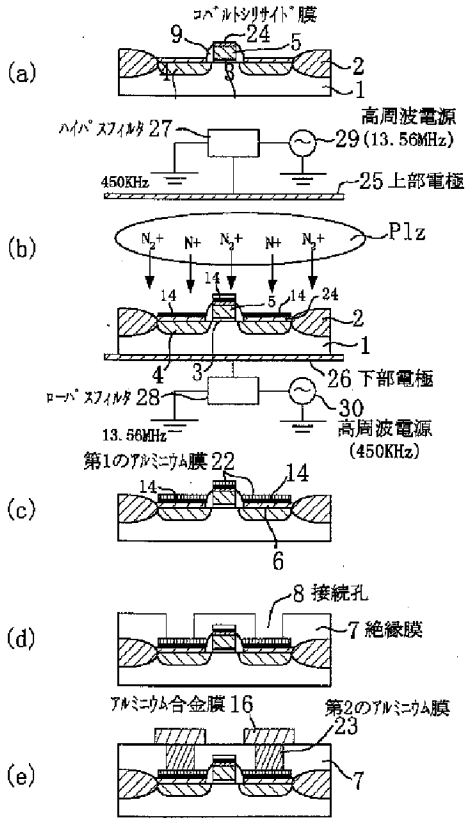
【図5】



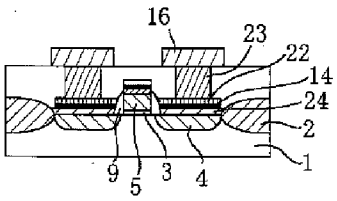
【図6】



【図7】

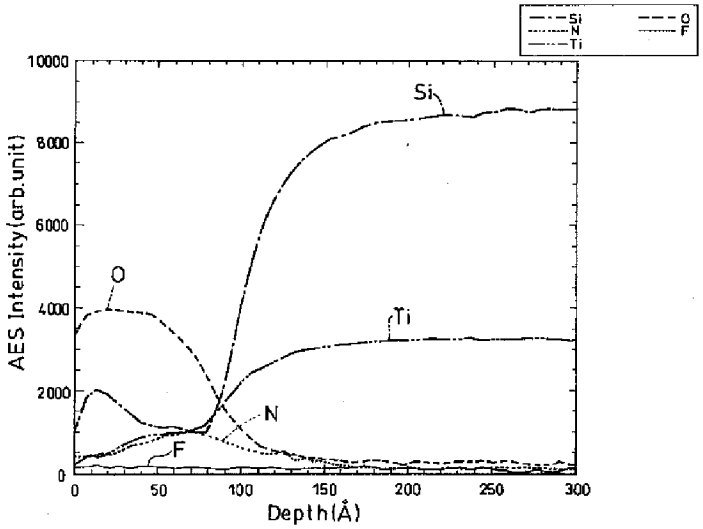


【図8】

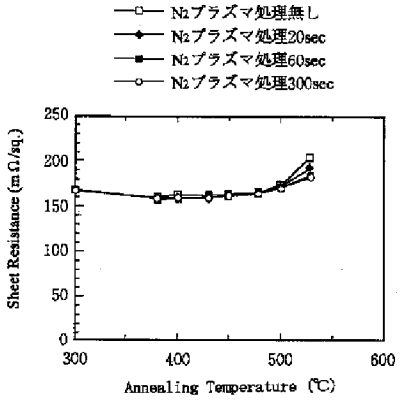


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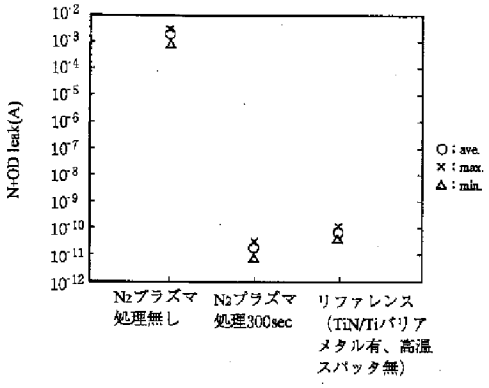
【図9】



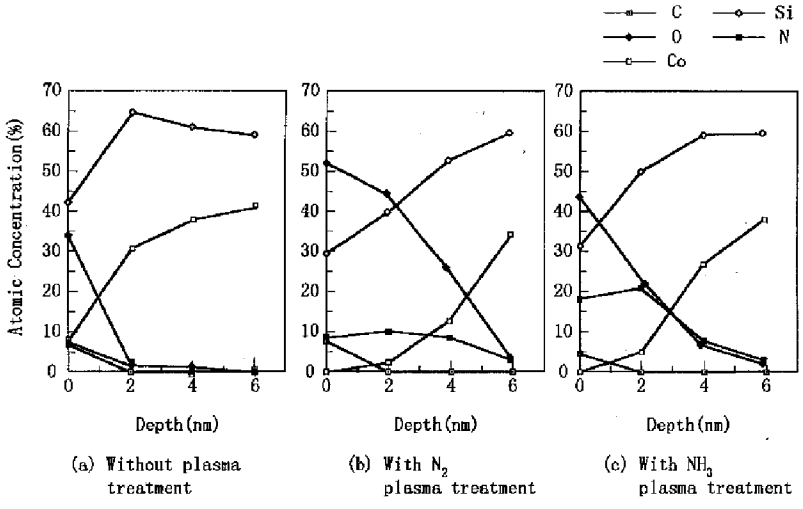
【図11】



【図10】

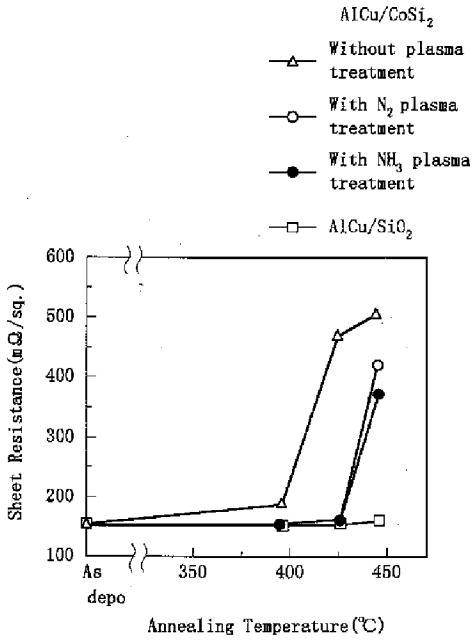


【図12】

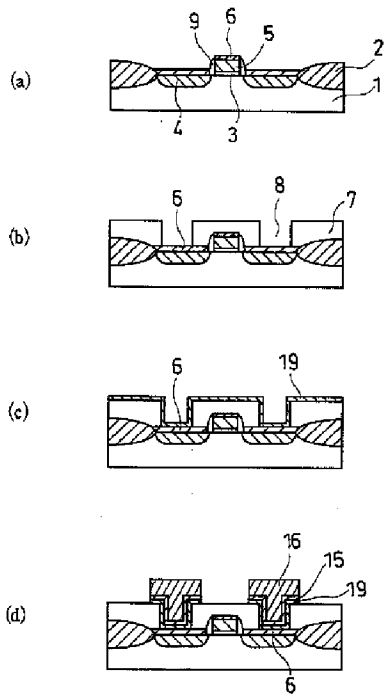


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【図13】



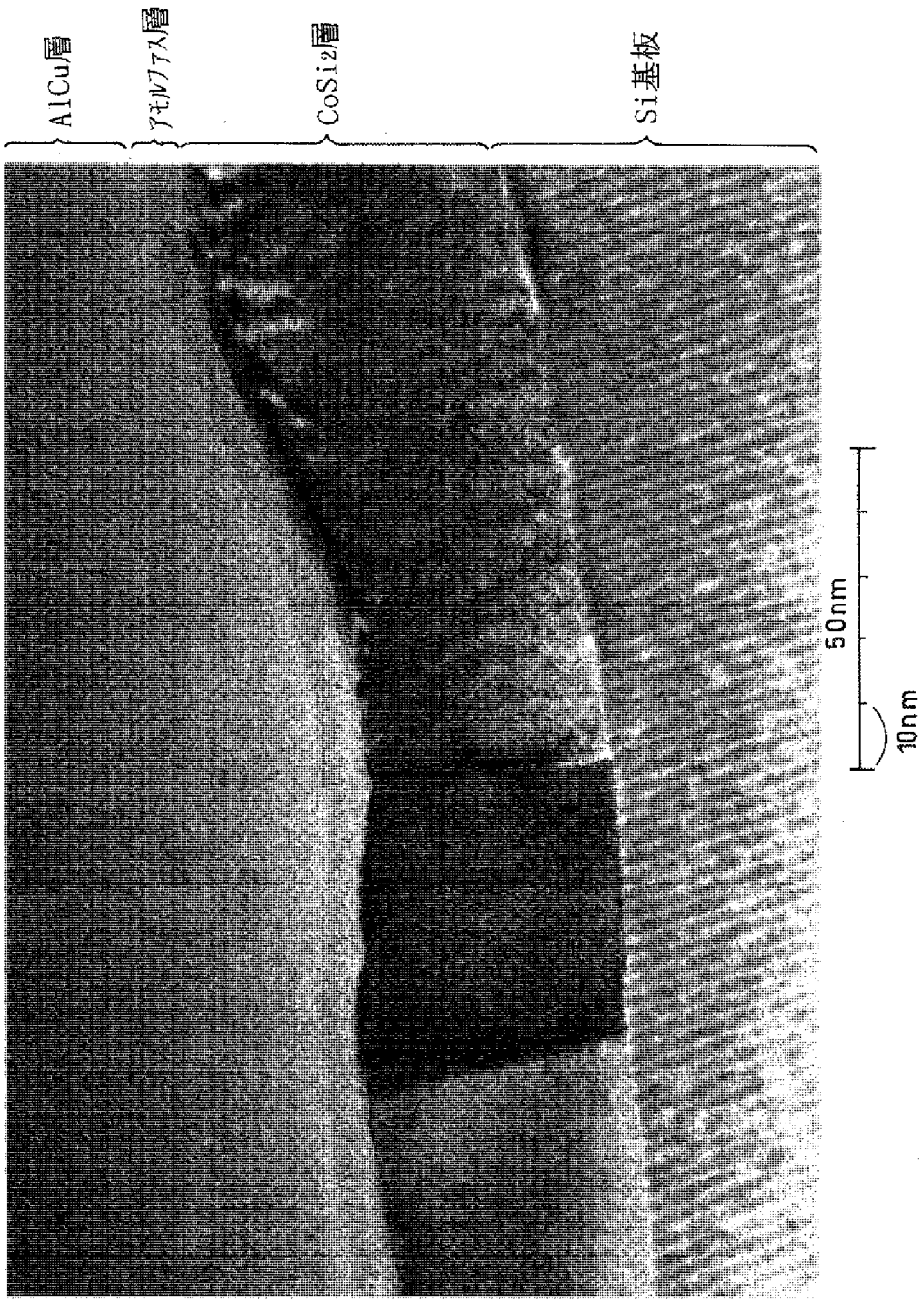
【図15】



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【図14】

図面代用写真



フロントページの続き

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Espacenet

JPH09289178A SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

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(IPC1-7): H01L21/265; H01L21/28; H01L21/3205; H01L21/336; H01L21/768; H01L29/78;

Priorities: JP3451296A 1996-02-22; JP4705397A 1997-02-14

Application: JPH09289178A·1997-02-14

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SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Abstract

PROBLEM TO BE SOLVED: To prevent generation of junction leak or the like which are to be caused by reaction between a metal silicide and a metal layer thereon at the time of thermal treatment, in a semiconductor device. SOLUTION: After connection holes 8 is formed or before an insulating film 7 is deposited, a semiconductor device is fixed on a cathode 11 of a plasma generating equipment. For example, the surface of a metal silicide layer such as a titanium silicide film 6 is exposed to plasma of gas containing nitrogen at a temperature lower than or equal to 550 deg.C. By this treatment, a barrier compound layer 14 composed of nitrogen-oxygen-metal-intersilicon compound is formed in a region in the vicinity of the surface of the metal silicide film such as the titanium silicide film 6. Reaction between the metal silicide layer and a buried layer in the later thermal treatment can be obstructed, while the buried layer is formed by using material having excellent step-difference coverage, e.g. an Al-Ti compound layer 15 and an aluminum alloy film 16, without depositing barrier metal such as titanium nitride . a nitride film on the connection holes 8. Thereby contact resistance, sheet resistance, and junction leak are reduced, and reliability can be improved.

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DESCRIPTION JPH09289178

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device having a silicide layer and a method of manufacturing the same, and more particularly to improvement of a structure of a contact portion between an upper wiring of the silicide layer and an upper low resistance metal film. ..

[0002]
2. Description of the Related Art In recent years, with higher integration and higher density of VLSI, metal silicide layers are formed on the surfaces of gate electrodes and source / drain regions of MOS transistors mounted on VLSI in a self-aligned manner. A technique (salicide technique) is used to reduce the sheet resistance of the gate electrode and the source / drain regions and reduce the parasitic resistance such as contact resistance and diffusion resistance to improve the operation speed of the semiconductor element.

[0003]

By the way, as a method of forming a buried layer made of aluminum, tungsten, and copper on the metal silicide layer, for example, a high temperature sputtering method utilizing the fluidity of an aluminum alloy at a high temperature, or a chemical vapor deposition excellent in coating property. There is known a method of forming a highly reliable buried layer by selectively depositing a metal such as aluminum, tungsten, or copper in the connection hole by a (hereinafter referred to as CVD) method.

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In that case, a reaction may occur between the metal composing the buried layer and the metal silicide layer, which may cause a problem. That is, since a thermal history of about 450 to 600 ° C. is generated in high temperature sputtering, selective CVD, or CVD for forming an upper layer wiring, the metal silicide reacts with the metal forming the buried layer, and the reaction product produces silicon. The substrate may be eroded and a junction leak may occur. Therefore, in order to suppress the reaction between the two, a barrier metal such as titanium nitride is generally formed between the buried layer and the metal silicide layer.

[0004]
Hereinafter, a conventional method of forming a buried layer on a metal silicide layer by using a high temperature sputtering method will be described with reference to FIGS.

[0005]

First, as shown in FIG. 15A, a gate oxide film 3 made of a silicon oxide film and a gate electrode 5 made of a polysilicon film are formed on an active region surrounded by a field oxide film 2 on a silicon substrate 1. Then, a MOS transistor having sidewalls 9 made of a silicon oxide film and source / drain regions 4 made by introducing impurities into the silicon substrate 1 is formed.

Then, for example, a titanium film is deposited on the source / drain region 4 and the gate electrode 5 of the MOS transistor by a sputtering method, heat-treated at 600 to 900 ° C., and then unreacted titanium is mixed with a H 2 SO 4 -H 2 O 2 mixed solution. By removing the film, the titanium silicide film 6 is selectively formed only on the source / drain regions 4 and the gate electrode 5.

[0006]
Next, as shown in FIG. 15B, an insulating film 7 is formed on the entire surface of the substrate, and a contact hole 8 reaching the titanium silicide film 6 in the source / drain region 4 is opened in the insulating film 7.

[0007]
Next, as shown in FIG. 15C, a titanium film and a barrier metal for improving the contact characteristics with the titanium silicide film 6 on the source / drain regions 4 in the connection

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hole 8 and on the insulating film 7. A titanium nitride film is deposited by the sputtering method to form a titanium nitride / titanium film 19.

[0008]

Next, as shown in FIG. 15 (d), titanium is sputtered and then an aluminum alloy is sputtered thereon at 500 ° C. to form an Al—Ti compound layer 15 formed by combining the aluminum alloy and titanium. , And the aluminum alloy film 16 thereon is formed.

At this time, the reaction heat between Al and Ti is used to fill the inside of the connection hole 8 with an aluminum alloy.

Then, the titanium nitride / titanium film 19, the Al—Ti compound layer 15, and the aluminum alloy 16 are patterned by photolithography to form metal wiring.

[0009]
However, when the diameter of the connection hole is further miniaturized in accordance with the miniaturization of the semiconductor device, in the above-mentioned conventional method, titanium nitride / titanium nitride is used in the step shown in FIG. 15 (c). It is not preferable to deposit the film 19 by the sputtering method for the following reasons.

[0010]

In general, since the titanium nitride film formed by the sputtering method does not have good step coverage, an overhang shape is likely to be formed at the corner of the connection hole.

Therefore, the flow of the aluminum alloy into the connection hole during high-temperature sputtering is hindered and the connection hole becomes difficult to fill (for example, Y. Takegawa et al. Abst. SSDM, p.558, 1993).

[0011]
Therefore, when forming a titanium nitride film, there is also a method of suppressing the

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formation of an overhang shape by sputtering titanium through a honeycomb filter (collimator) while flowing N2 gas, but when a collimator is used, particles are generated. It's easy to do.

[0012]

Further, in the step shown in FIG. 15B, the part other than the connection hole 8 (the part on the insulating film 7) is also covered with the titanium nitride / titanium film 19, so that the selective CVD method utilizing the difference in the underlying layer is used. It is not possible to use a method of selectively depositing a metal such as aluminum, tungsten, or copper only in the connection hole 8.

[0013]

On the other hand, in order to avoid the above-mentioned problems, after forming the contact hole in the insulating film, the titanium nitride / titanium film 19 is not deposited and heat treatment is performed in an NH3 atmosphere at about 850 ° C. A technique has been proposed in which a titanium nitride film is formed on the surface of a titanium silicide film, and then aluminum is selectively deposited only in the contact holes by a selective CVD method (for example, H. Shinriki et al. Ext.

Abst.

SSDM, p.968, 1994).

[0014]

However, if a heat treatment at 800 ° C. or higher is applied to the titanium silicide film, boron in the source / drain regions may be absorbed into the titanium silicide film, and the saturation current value of the P-channel transistor may decrease. Further, depending on the type of metal silicide, when heat treatment is performed at a high temperature, the silicide agglomerates to increase the sheet resistance of the source / drain. Therefore, the types of silicide to which the above conventional method can be applied are limited.

[0015]

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In addition, the above-mentioned problems occur not only between the buried layer in the connection hole and the silicide film, but also when a low resistance metal film is formed on the silicide film. This is a cause of deteriorating the reliability of the laminated structure of the silicide film and the metal film.

[0016]
The present invention relates to a compound that causes a junction leak in a semiconductor substrate when a compound layer made of a nitrogen-oxygen-metal-silicon compound is formed in the vicinity of a boundary between a metal silicide layer and a metal film thereon. It was made based on the discovery of the fact that the invasion of the barrier does not occur, and the purpose is to form a compound layer that serves as such a barrier, thereby eliminating the need for a barrier metal and forming a buried layer or a silicide film and a metal film. It is an object of the present invention to provide a semiconductor device capable of keeping the sheet resistance value of the entire metal silicide film low and preventing the occurrence of a junction leak while improving the reliability of the laminated structure, and a manufacturing method thereof.

[0017]
In order to achieve the above object, the present invention provides means for a semiconductor device according to claims 1 to 9 and a semiconductor device according to claims 12 to 23. Measures related to the manufacturing method are taken.

[0018]
As described in claim 1, a semiconductor device of the present invention includes a semiconductor substrate, a metal silicide film formed on a part of the semiconductor substrate and having a first metal silicided, and the metal silicide film. And a barrier compound layer formed of a nitrogen-oxygen-first metal-silicon compound and formed in a region near the surface of the metal silicide film. There is.

[0019]

As a result, since the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound is formed on the surface of the metal silicide film, even if there is a high temperature history during the manufacturing process such as when depositing the metal film, the metal The reaction between the first metal forming the silicide film and the second metal forming the metal film is suppressed.

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That is, the occurrence of junction leakage and the deterioration of the characteristics of the gate oxide film are suppressed without interposing a barrier metal such as titanium nitride / nitride film.

Therefore, it is possible to avoid problems due to poor step coverage and resistance characteristics of the barrier metal, such as a decrease in reliability and an increase in sheet resistance.

[0020]
As described in claim 2, in claim 1, it is preferable that the barrier compound layer is formed in a region near the surface of the entire metal silicide film.

[0021]
This simplifies the manufacturing process of the semiconductor device and improves the chemical resistance of the metal silicide layer, and as a result, the manufacturing cost can be reduced.

[0022]
As described in claims 3 and 4, in claim 1 or 2, the thickness of the barrier compound layer is not less than a thickness sufficient to prevent diffusion of the second metal into the barrier compound layer. Then, it is preferably 30% or less of the thickness of the metal silicide film, or from another viewpoint, it is preferably in the range of 2 to 20 nm.

[0023]
As a result, an increase in contact resistance and sheet resistance due to the formation of a too thick barrier compound layer is suppressed as much as possible.

[0024]
As described in claim 5, in claim 1, 2 or 3, the position where the concentration of the nitrogen in the barrier compound layer is maximum is located deeper than the position where the concentration of the oxygen is maximum. Preferably.

[0025]

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As a result, the oxygen concentration becomes relatively low at the position where the nitrogen concentration becomes high, so that the region where the concentration of the oxide layer is high, which causes the increase in contact resistance and sheet resistance, can be suppressed near the surface. ..

Therefore, an increase in sheet resistance or the like at the contact portion between the metal film and the silicide film can be suppressed as much as possible.

[0026]
According to a sixth aspect of the present invention, in the first aspect, the insulating film formed on the metal silicide film and the connection hole formed in a part of the insulating film and reaching the metal silicide film are provided. Further, the metal film may be a buried layer made of the second metal deposited in the connection hole.

[0027]

Accordingly, since the barrier compound that suppresses the reaction between the first metal and the second metal exists in the region near the surface of the metal film, it is not necessary to form the barrier metal in the connection hole.

Therefore, it is possible to select a second metal having a good coverage as the second metal forming the burying layer in the connection hole which is required to have the step coverage, and the reliability of the semiconductor device is improved.

[0028]
As described in claim 7, in claim 1, an insulating film formed on the metal silicide film, a connection hole formed in a part of the insulating film and reaching the metal silicide film, A buried layer made of a third metal deposited in the connection hole may further be provided.

[0029]
This makes it possible to select a material having a low electric resistance as the metal film composed of the second metal and to interpose the low resistance layer between the buried layer

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and the metal silicide film. It is possible to obtain a semiconductor device that is suitable for the realization.

[0030]
As described in claim 8, in claim 1, 2, 3, 4, 5, 6 or 7, the first metal is titanium, cobalt, nickel, tantalum, tungsten, niobium, palladium, platinum. And at least one of molybdenum.

[0031]
As described in claim 9, in claim 1, 2, 3, 4, 5, 6 or 7, the second metal is a metal containing aluminum, a metal containing copper or a metal containing tungsten. It is preferable to configure at least one of them.

[0032]
According to a tenth aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising: forming a metal silicide film made of a compound of a first metal and silicon on a semiconductor substrate; Of a nitrogen-oxygen-first metal-silicon compound in the region near the surface of the metal silicide film by irradiating the surface of the metal silicide film with ions containing nitrogen under a neutral or oxidizing atmosphere. And a third step of depositing a second metal on the barrier compound layer of the metal silicide film to form a metal film.

[0033]

By this method, since the barrier compound layer is formed on the surface of the metal silicide film in the second step, it is possible to form the metal film in the third step without forming the barrier metal.

Therefore, by appropriately selecting and using a material having a good step coverage as the second metal, the step coverage with respect to the base of the metal film is improved, and a highly reliable semiconductor device can be formed.

[0034]
As described in claim 11, in claim 10, after the first step and before the second step, a step of forming an insulating film on the metal silicide film; And a step of selectively removing a part of

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the film to form a contact hole reaching the metal silicide film. In the second step, the contact hole in the region near the surface of the metal silicide film is formed. The barrier compound layer may be formed in a region exposed at the bottom of the substrate, and in the third step, the inside of the connection hole may be filled with the second metal.

[0035]
By this method, the formation region of the barrier compound layer is limited to a particularly required region, so that the increase of the sheet resistance of the metal silicide film is suppressed.

[0036]
As described in claim 12, in claim 10, the step of forming an insulating film on the barrier compound layer of the metal silicide film after the second step, and a part of the insulating film. Is further removed to form a connection hole reaching the barrier compound layer. In the third step, the second metal can be deposited in the connection hole.

[0037]

By this method, when the contact is formed from each wiring layer at an arbitrary position of the metal silicide film, the barrier compound layer is formed at any position. Therefore, the barrier compound layer is formed every time the connection hole is formed. Therefore, the process is simplified.

Further, since the resistance of the metal silicide film to chemicals such as HF is also improved, restrictions on subsequent steps are alleviated.

[0038]
As described in claim 13, in claim 12, the step of forming an insulating film on the barrier compound layer of the metal silicide film after the third step, and a part of the insulating film. The method may further include a step of selectively removing the metal to form a connection hole reaching the barrier compound layer, and a step of depositing a third metal in the connection hole to form a buried layer.

[0039]

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By this method, when a material having a low electric resistance is selected as the second metal, a low resistance layer is formed on the metal silicide film and a buried layer is formed on the metal silicide film. A good semiconductor device can be obtained.

[0040]
As described in claim 14, in claim 10, 11, 12 or 13, in the second step, a plasma generating device in which a lower electrode which is a cathode and an upper electrode which is an anode are arranged in a chamber. The barrier compound layer can be formed by exposing the metal silicide film to plasma of a gas containing nitrogen in a state where the semiconductor substrate is placed on the lower electrode in the chamber.

[0041]
By this method, by placing a semiconductor substrate on the cathode, nitrogen, which is a positive ion in nitrogen plasma, is efficiently taken into the metal silicide.

[0042]
As described in claim 15, in claim 10, 11, 12 or 13, in the second step, one of ultraviolet rays and ionizing radiation is performed while exposing the surface of the metal silicide film to a gas containing nitrogen. The barrier compound layer can be formed by irradiating either one.

[0043]
As described in claim 16, in claim 10, 11, 12 or 13, in the second step, the barrier compound layer is formed by exposing the surface of the metal silicide film to an ion beam containing nitrogen. Can be formed.

[0044]
As described in claim 17, in claim 10, 11, 12, 13, 14, 15 or 16, the second step is preferably performed at 550 ° C or lower.

[0045]
By this method, plasma treatment or the like is performed under a low temperature condition of 550 ° C. or less, so that even when titanium silicide or the like is used, the metal silicide is not aggregated and the selection range of the type of metal silicide is expanded.

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[0046]
As described in claim 18, in claim 10, 11, 12, 13, 14, 15 or 16, N 2 gas can be used as the nitrogen-containing gas in the second step.

[0047]
According to this method, when forming the barrier compound layer, the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound is easily formed by utilizing the natural oxide film existing on the surface of the metal silicide film.

[0048]
As described in claim 19, in claim 10, 11, 12, 13, 14, 15, 16, 17 or 18, by flowing a gas containing hydrogen before the second step, The method further comprises a step of removing the natural oxide film on the metal silicide film, and a gas containing oxygen can be added in the second step.

[0049]
By this method, the oxygen concentration in the barrier compound layer is controlled, so that the distribution state of each element can be adjusted to a more preferable state.

[0050]
As described in claim 20, in claim 10, 11, 12, 13, 14, 15 or 16, in the second step, the nitrogen-containing ion is ion-energy of 3 keV or less, the metal silicide film. It is preferable to introduce it inside.

[0051]
By this method, the region where the barrier compound layer is formed is limited to a depth of about 20 nm from the surface of the metal silicide film, so that the increase in contact resistance and sheet resistance of the formed semiconductor device is suppressed. ..

[0052]
As described in claim 21, in claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, in the first step, titanium is used as the metal silicide film. It is preferable to form a silicide film of any one of cobalt, nickel, tantalum, tungsten, palladium, platinum and molybdenum.

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[0053]
As described in claim 22, in claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, in the third step, the CVD method is used to remove aluminum. It is preferable to deposit any one of a metal containing metal, a metal containing copper, and a metal containing tungsten.

[0054]
As described in claim 23, in claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, titanium and aluminum alloy are continuously added in the third step. The metal film can be composed of an Al—Ti compound layer and an aluminum alloy film by sputtering.

[0055]
By these methods, it is possible to select the method of forming the metal film and the wiring according to the type of the semiconductor device and the difference in the wiring layer formed on the metal silicide film.

[0056]
DESCRIPTION OF THE PREFERRED EMBODIMENTS (First Embodiment) FIGS. 1A to 1D are cross-sectional views showing a manufacturing process of a semiconductor device according to a first embodiment.

[0057]

First, as shown in FIG. 1A, a gate oxide film 3 made of a silicon oxide film and a gate electrode 5 made of a polysilicon film are formed on an active region surrounded by a field oxide film 2 on a silicon substrate 1. Then, a MOS transistor having sidewalls 9 made of a silicon oxide film and source / drain regions 4 made by introducing impurities into the silicon substrate 1 is formed.

Then, for example, a titanium film is deposited on the substrate by a sputtering method, heat-treated at 650 ° C., and then the unreacted titanium film is removed with a mixed solution of H 2 SO 4 -H 2 O 2 to form the source / drain region 4 and the gate electrode. A titanium silicide film 6 having a thickness of about 70 nm is selectively formed only on the film 5.

Then, heat treatment is performed at 850 ° C. to reduce the resistance of the titanium silicide film.

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[0058]
Next, as shown in FIG. 1B, an insulating film 7 having a thickness of about 800 nm is formed on the entire surface of the substrate, and a contact hole reaching the titanium silicide film 6 in the source / drain region 4 is formed in the insulating film 7. Open 8

[0059]

Next, as shown in FIG. 1C, a plasma generator having an anode 10 and a cathode 11 forming a parallel plate electrode, a blocking capacitor 12, and a high frequency power source 13 is used, and a reaction chamber of the plasma generator (A semiconductor device which has undergone the steps up to FIG. 1B is mounted on a cathode 11 arranged inside (not shown), and the surface of the titanium silicide film 6 is exposed to plasma of a nitrogen-containing gas.

For example, at a temperature of 50 ° C. and under a pressure of 80 mTorr, 100% N 2 gas is introduced, and high frequency power of about 300 W is applied between the parallel plate electrodes 10 and 11 for 300 seconds.

At this time, nitrogen plasma Plz is generated in the reaction chamber.

Nitrogen in the nitrogen plasma Plz is positive ions such as N + and N2 +, and a total potential of 300V is generated in the direction of the cathode 11 by adding the plasma potential of about 60V and the self-bias voltage of about 240V.

Then, nitrogen ions are attracted to the surface of the semiconductor device at this potential.

That is, by installing the semiconductor device on the cathode 11 of the parallel plate electrodes 10 and 11, the introduction of nitrogen to the surface of the titanium silicide film 6 is promoted.

At this time, oxygen in the natural oxide layer formed on the surface of the titanium silicide film 6 is also taken into the titanium silicide layer 6, and the barrier compound layer 14 made of the nitrogen-oxygen-titanium-silicon compound is formed into the titanium silicide film 6. Formed

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near the surface of the.

[0060]

Next, as shown in FIG. 1D, titanium is sputtered to a thickness of about 75 nm, and then an aluminum alloy containing 1% of silicon and 0.5% of copper is sputtered to a thickness of about 900 nm at 500 ° C. By doing so, the Al—Ti compound layer 15 formed by combining the aluminum alloy and titanium and the aluminum alloy film 16 thereon are formed.

At this time, the reaction heat between Al and Ti is used to fill the inside of the connection hole 8 with an aluminum alloy to form a buried layer.

Then, the Al—Ti compound layer 15 and the aluminum alloy film 16 are patterned by photolithography to form metal wiring.

[0061]

In addition, a connection hole is also formed on the gate electrode 5 at the same time (in a cross section different from the cross section shown in FIGS. 1A to 1D), and a barrier compound is formed near the surface of the titanium silicide film 6 on the gate electrode 5. After forming the layer 14, the Al—Ti compound layer 15 and the aluminum alloy film 16 may be deposited to form the buried layer and the metal wiring.

[0062]

FIG. 2 shows a cross-sectional structure of a semiconductor device formed by the above manufacturing method.

That is, a gate oxide film 3, a gate electrode 5 made of a polysilicon film, a source / drain region 4, and a titanium silicide film 6 formed on the source / drain region 4 and the gate electrode 5 are formed on a silicon substrate 1. , Sidewalls 9 are formed.

A connection hole 8 reaching the titanium silicide film 6 on the source / drain region 4 is formed

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in the insulation film 7 formed on the substrate. The connection hole 8 is buried in the connection hole 8 and on the insulation film 7. An Al—Ti compound layer 15 and an aluminum alloy film 16 that form a layer and a metal wiring are formed.

As a feature of the semiconductor device according to the present embodiment, a barrier metal such as titanium nitride / nitride film is not formed under the aluminum alloy film 16, and instead, the titanium silicide film 6 on the source / drain region 4 is used. A barrier compound layer 14 made of a nitrogen-oxygen-titanium-silicon compound is formed only on the surface of a region which will be the bottom surface of the connection hole 8.

[0063]
Next, details of the structure of the barrier compound layer 14 of the semiconductor device obtained in the present embodiment and details of the contact resistance and the like in the semiconductor device of the present embodiment will be described.

[0064]

FIG. 9 is a diagram showing the concentration profile of each element obtained as a result of analyzing the region near the surface of the titanium silicide film 6 after the step shown in FIG. 1C according to the present embodiment by Auger electron spectroscopy. is there.

However, since the sensitivities of the respective elements are different during the analysis by Auger electron spectroscopy, FIG. 9 does not accurately show the composition ratio of each element, but merely shows the concentration distribution of each element.

As shown in FIG. 9, silicon and oxygen are particularly abundant up to 2 to 3 nm from the surface. This is because the SiO2 film was formed as a natural oxide film on the surface of the titanium silicide film in the analysis process. Thought to be a thing.

A barrier compound layer made of a nitrogen-oxygen-titanium-silicon compound is formed below the SiO2 film in the range of about 8 nm.

When the SiO2 film near the surface is excluded, a peak of oxygen concentration is found in the

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vicinity of the surface, and a peak of nitrogen concentration is found at a depth of about 4-5 nm below the SiO2 film.

[0065]
The bonding state between the elements in the barrier compound layer 14 could not be analyzed because the reaction layer was thin, but the standard heats of formation of TiN, TiO2, Si3 N4 and SiO2 were -73.0 kcal in order. / Mol, -218.0 kcal / mol, -179.3, and -202.5 kcal / mol, oxygen is bonded to titanium and silicon when the titanium silicide film is used as in the present embodiment. It is considered that nitrogen is mainly bonded to silicon.

[0066]

As a result of forming the barrier compound layer 14, the sheet resistance increased from 2.6Ω / □ to 2.9Ω / □, but the increase rate was about 10%, which is sufficiently low that there is no particular problem in transistor operation or the like. It is a value.

In the present embodiment, since the barrier compound layer 14 made of the nitrogen-oxygen-titanium-silicon compound is formed only on the surface of the titanium silicide film in the connection hole 8, the sheet of titanium silicide 6 obtained by the above-mentioned nitrogen plasma treatment is used. The rate of resistance increase is even smaller.

[0067]

FIG. 10 shows a sample shown in FIG. 1C that is not subjected to the nitrogen plasma treatment, a sample that has been subjected to the treatment of the present embodiment, and a reference sample that is manufactured by the conventional method shown in FIG. 15 (from a TiN / Ti film). FIG. 3 is a diagram comparing the junction leak characteristics of samples having a barrier metal that does not perform high temperature sputtering.

However, the junction leakage characteristics are shown when a reverse voltage of 5.5 V is applied to the N + P junction having an area of 8000 μm 2.

As shown in the figure, the junction leak is large in the sample which is not subjected to the

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nitrogen plasma treatment.

In the process shown in FIG. 1D, the aluminum alloy film 16 or the Al—Ti compound layer 15 reacts with the titanium silicide film 6 when the aluminum alloy is sputtered at 500 ° C. It is probable that aluminum invaded into the structure and caused a junction leak.

On the other hand, the junction leak of the sample subjected to the nitrogen plasma treatment according to the present embodiment is equivalent to the junction leak of the reference sample which has the barrier metal and does not perform high-temperature sputtering despite having no barrier metal. I know there is.

It is considered that this is because the barrier compound layer 14 prevents the aluminum alloy film 16 or the Al—Ti compound layer 15 from reacting with the titanium silicide film 6 when the aluminum alloy is sputtered at 500 ° C.

[0068]

Further, the contact resistance to the N + diffusion region in this embodiment is 15Ω for the sample having a contact shape of 1.0 μm square and subjected to the nitrogen plasma treatment, and the contact resistance of the reference sample is 5Ω.

Although the contact resistance of the sample according to this embodiment is slightly high, it is understood that no particular trouble occurs in the operation of the transistor and the electrical connection with the silicon substrate is sufficient.

[0069]

FIG. 11 is a diagram showing the annealing temperature dependence of the sheet resistance of various samples that have been subjected to a nitrogen plasma treatment and then deposited with an Al alloy and annealed.

The processing conditions are as follows. After performing the nitrogen plasma treatment shown

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in FIG. 1C on the titanium silicide film having a thickness of 70 nm and further depositing an Al-1% Si-0.5% Cu alloy by a thickness of 200 nm, Annealed for 30 minutes.

The samples were those that were not subjected to nitrogen plasma treatment, those that were subjected to nitrogen plasma treatment for 20 seconds, those that were subjected to nitrogen plasma treatment for 60 seconds, and those that were subjected to nitrogen plasma treatment for 300 seconds. is there.

As shown in the figure, it can be seen that the increase in the sheet resistance when annealed at 530 ° C. is suppressed between the nitrogen plasma treatment for 60 seconds and the nitrogen plasma treatment for 300 seconds.

This figure also shows that the barrier compound layer formed of the nitrogen-oxygen-titanium-silicon compound formed on the surface of the titanium silicide film has an effect of suppressing the reaction between the aluminum alloy and the titanium silicide film.

[0070]

As described above, according to the present embodiment, the surface of the metal silicide is subjected to the nitrogen plasma treatment to form the barrier compound layer including the nitrogen-oxygen-metal-silicon compound on the surface of the metal silicide film. Therefore, it is possible to effectively prevent the metal generated by the reaction between the metal silicide film and the aluminum alloy from entering the silicon substrate by the heat treatment in the subsequent process.

That is, it is possible to suppress the occurrence of a junction leak without interposing a barrier metal such as a titanium nitride / nitride film between the buried layer made of an aluminum alloy film and the metal silicide as in the conventional method.

Therefore, it is possible to prevent the reliability of the buried layer from being deteriorated as in the case where the barrier metal is provided.

Moreover, the contact resistance can be suppressed to a sufficiently low level for practical use,

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and the sheet resistance of the metal silicide film itself can be kept to a sufficiently low level.

[0071]
Further, even when the barrier compound layer is formed in the region near the surface of the metal silicide film on the gate electrode 5, it is possible to prevent the metal from entering the gate electrode, which effectively prevents the deterioration of the characteristics of the gate oxide film. Can be blocked.

[0072]
In particular, in this embodiment, since the nitrogen plasma treatment is performed at a low temperature of 550 ° C. or less, aggregation of the metal silicide film does not occur for many kinds of metal silicide, that is, the metal material forming the metal silicide. There is an advantage that the range of selection can be expanded.

[0073]

(Second Embodiment) Next, the second embodiment will be described.

In the present embodiment, although illustration of the manufacturing process is omitted, after performing the same processing as in FIGS. 1A to 1C in the above-described first embodiment, the inside of the connection hole 8 is formed by the selective CVD method. A tungsten film 17 to be a buried layer is deposited.

Then, after depositing the aluminum alloy film 16 on the tungsten film 17 and the insulating film 7, the aluminum alloy film 16 is patterned to form a metal wiring.

[0074]

FIG. 3 is a cross-sectional view showing the structure of the semiconductor device formed according to this embodiment.

In the first embodiment, the embedded layer and the metal wiring are integrally formed by the

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Al—Ti compound layer 15 and the aluminum alloy film 16, but in the present embodiment, the embedded layer is formed by the tungsten film 17. The aluminum alloy film 16 constitutes a metal wiring.

The barrier compound layer 14 made of a nitrogen-oxygen-titanium-silicon compound is formed only on the bottom surface of the connection hole 8 in the titanium silicide film 6 on the source / drain region 4, and the tungsten film 17 and the titanium film are formed. The silicide film 6 is in contact with the barrier compound layer 14.

That is, the semiconductor device of this embodiment is different from the semiconductor device of the first embodiment only in that the buried layer and the metal wiring are made of different materials, and the other parts are the semiconductor of the first embodiment. It has the same structure as the device.

Therefore, basically the same effect as the first embodiment can be exhibited.

[0075]

In addition, in the semiconductor device of this embodiment, since the buried layer is formed of the tungsten film 17, the temperature at which the reaction causing the junction leak of the semiconductor device occurs is higher than that of the aluminum alloy film or the like. In the present embodiment, the barrier compound layer 14 can prevent a junction leak from occurring due to the reaction of titanium silicide and tungsten by the subsequent heat treatment at 600 ° C. or more to cause the metal to enter the silicon substrate. ..

[0076]

(Third Embodiment) Next, a third embodiment will be described. 4A to 4D are cross-sectional views showing the manufacturing process of the semiconductor device of this embodiment.

[0077]

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First, as shown in FIG. 4A, a gate oxide film 3 made of a silicon oxide film and a gate electrode 5 made of a polysilicon film are formed on an active region surrounded by a field oxide film 2 on a silicon substrate 1. Then, a MOS transistor having sidewalls 9 made of a silicon oxide film and source / drain regions 4 made by introducing impurities into the silicon substrate 1 is formed. Then, for example, a titanium film is deposited on the substrate by a sputtering method, heat-treated at 650 ° C., and then the unreacted titanium film is removed with a mixed solution of H 2 SO 4 -H 2 O 2 to remove the source / drain region 4 and the gate electrode. A titanium silicide film 6 having a thickness of about 70 nm is selectively formed only on the film 5. Then, heat treatment is performed at 850 ° C. to reduce the resistance of the titanium silicide film.

[0078]

Next, as shown in FIG. 4B, in a reaction chamber (not shown) of the plasma generator, a plasma generator having an anode 10 and a cathode 11 forming parallel plate electrodes and a DC power supply 18 is used. The semiconductor device is placed on the cathode 11 arranged in the above, and the surface of the titanium silicide film 6 is exposed to plasma of nitrogen-containing gas such as nitrogen gas. Then, as in the first embodiment, oxygen in the natural oxide film formed on the surface of the titanium silicide film 6 is also taken into the titanium silicide film 6, and the entire titanium silicide film 6 is exposed by the plasma of N2 gas. A barrier compound layer 14 made of a nitrogen-oxygen-titanium-silicon compound is formed near the surface.

[0079]

Next, as shown in FIG. 4C, an insulating film 7 having a thickness of about 800 nm is formed on the entire surface of the substrate, and a contact hole reaching the titanium silicide film 6 in the source / drain region 4 is formed in the insulating film 7. Open 8

[0080]

Next, as shown in FIG. 4 (d), after sputtering titanium by a thickness of about 75 nm with a sputtering apparatus, an aluminum alloy containing 1% of silicon and 0.5% of copper is about 900 nm at 500 ° C. The Al—Ti compound layer 15 formed by combining the aluminum alloy and titanium and the aluminum alloy film 16 thereon are formed by sputtering by the thickness of the above.

At this time, the reaction heat between Al and Ti is used to fill the inside of the connection hole 8

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with an aluminum alloy to form a buried layer. Then, the Al—Ti compound layer 15 and the aluminum alloy film 16 are patterned by photolithography to form metal wiring.

[0081]

FIG. 5 shows a sectional structure of a semiconductor device formed by the above-described manufacturing method. That is, a gate oxide film 3, a gate electrode 5 made of a polysilicon film, a source / drain region 4, and a titanium silicide film formed on the source / drain region 4 and the gate electrode 5 on the silicon substrate 1. A MOS transistor including 6 and the sidewall 9 is formed. Then, the barrier compound layer 14 made of a nitrogen-oxygen-titanium-silicon compound is formed on the entire surface of the titanium silicide film 6. A connection hole 8 reaching the titanium silicide film 6 on the source / drain region 4 is formed in the insulation film 7 formed on the substrate. The connection hole 8 is buried in the connection hole 8 and on the insulation film 7. An Al—Ti compound layer 15 and an aluminum alloy film 16 that form a layer and a metal wiring are formed. That is, in the semiconductor device of the first embodiment, the nitrogen-oxygen-titanium-silicon compound is formed only on the surface of the region of the titanium silicide film 6 on the source / drain region 4 which will be the bottom of the contact hole 8. However, in the semiconductor device of this embodiment, the barrier compound layer 14 is formed on the entire surface of the titanium silicide film 6 on the source / drain regions 4 and the gate electrode 5. The point is characteristic.

[0082]

Also in this embodiment, since the barrier compound layer 14 made of the nitrogen-oxygen-titanium-silicon compound is formed in the region near the surface of the titanium silicide film 6, the same effect as that of the first embodiment can be obtained. Be done. In particular, according to the method of the present embodiment, the barrier compound layer 14 is formed not only in the source / drain regions 4 but also in the region near the surface of the titanium silicide film 6 on the gate electrode 5, so that FIG. Even when a contact portion is formed on the gate electrode 5 from a wiring layer different from the Al—Ti compound layer 15 and the aluminum alloy film 16 shown, the contact is made via the barrier compound layer 14 without performing the nitrogen plasma treatment again. There is an advantage that can be done.

[0083]

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Further, before the step shown in FIG. 4D, that is, before the semiconductor device is put into the sputtering apparatus, it is necessary to wet etch the inside of the connection hole 8 with an HF solution to remove the surface oxide layer of the metal silicide. The titanium silicide film 6 is easily etched by the HF solution. In this respect, in the present embodiment, the barrier compound layer 14 made of the nitrogen-oxygen-titanium-silicon compound is considered to have a composition close to SiN because it contains a bond between silicon and nitrogen, and therefore the HF solution is used. It is thought that it is difficult to etch. Therefore, this embodiment also has an advantage that the chemical resistance of the titanium silicide film is improved and the process margin is increased.

[0084]

However, in the semiconductor device of this embodiment, since the barrier compound layer 14 is formed on the entire surface of the titanium silicide film 6, the increase in sheet resistance of the titanium silicide film 6 is larger than that of the semiconductor device of the first embodiment. Become. However, as described in the first embodiment, even in that case, the increase rate of the sheet resistance is about 10%, which is a sufficiently low value that causes no particular problem in the transistor operation and the like.

[0085]

(Fourth Embodiment) Next, a fourth embodiment will be described. In the present embodiment, although illustration of the manufacturing process is omitted, after performing the same processing as in FIGS. 3A to 3C in the above-described third embodiment, the inside of the connection hole 8 is formed by the selective CVD method. A tungsten film 17 to be a buried layer is deposited. Then, after depositing the aluminum alloy film 16 on the tungsten film 17 and the insulating film 7, the aluminum alloy film 16 is patterned to form a metal wiring.

[0086]

FIG. 6 is a cross-sectional view showing the structure of the semiconductor device formed according to this embodiment. In the third embodiment, the embedded layer and the metal wiring are integrally formed by the Al—Ti compound layer 15 and the aluminum alloy film 16, but in the present embodiment, the embedded layer is formed by the tungsten film 17. The aluminum alloy film 16 constitutes a metal wiring. A barrier compound layer 14 made of a

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nitrogen-oxygen-metal-silicon compound is formed on the entire surface of the titanium silicide film 6 on the source / drain regions 4 and the gate electrode 5, and the tungsten film 17 and the titanium silicide film are formed. 6 are in contact with each other via the barrier compound layer 14. That is, the semiconductor device of this embodiment is different from the semiconductor device of the third embodiment only in that the buried layer and the metal wiring are made of different materials, and the other parts are the semiconductor of the third embodiment. It has the same structure as the device. Therefore, basically the same effect as the third embodiment can be obtained.

[0087]

In addition, in the semiconductor device of this embodiment, since the buried layer is composed of the tungsten film 17, the barrier compound layer 17 may prevent the reaction between tungsten and titanium silicide. Therefore, it is possible to prevent a junction leak from occurring due to the reaction of titanium silicide and tungsten with the subsequent heat treatment at 600 ° C. or more to cause the metal to enter the silicon substrate.

[0088]

(Fifth Embodiment) Next, a fifth embodiment will be described. 7A to 7D are cross-sectional views showing the manufacturing process of the semiconductor device of this embodiment.

[0089]

First, as shown in FIG. 7A, a gate oxide film 3 made of a silicon oxide film and a gate electrode 5 made of a polysilicon film are formed on an active region surrounded by a field oxide film 2 on a silicon substrate 1. Then, a MOS transistor having sidewalls 9 made of a silicon oxide film and source / drain regions 4 made by introducing impurities into the silicon substrate 1 is formed. Then, for example, a cobalt film is deposited on the substrate by a sputtering method, heat-treated at 500 ° C. in a nitrogen atmosphere, and then the unreacted cobalt film is removed with a H 2 SO 4 -H 2 O 2 mixed solution to form the source / drain region 4. A cobalt silicide film 24 having a thickness of about 50 nm is selectively formed only on the gate electrode 5 and the gate electrode 5. Then, heat treatment is performed at 850 ° C. to reduce the resistance of the cobalt silicide film 24.

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[0090]

Next, as shown in FIG. 7B, an upper electrode 29 and a lower electrode 26 which form a parallel plate electrode, a high pass filter 27, a low pass filter 28, a 13.56 MHz high frequency power supply 29, and a 400 KHz high frequency. A semiconductor device is placed on a lower electrode 26 arranged in a reaction chamber (not shown) of the plasma generator using a plasma generator having a power supply 30, and the surface of the cobalt silicide film 24 is replaced with nitrogen gas or the like. Exposed to plasma of nitrogen-containing gas. For example, under a temperature of 400 ° C. and a pressure of 2 Torr, 100% N2 gas is introduced, and a high frequency power of 29 W is applied to the upper electrode 25 by a high frequency power supply 29, and a high frequency power of 100 W is applied to the lower electrode 26 of a high frequency power supply of 900 W for 900 sec. Apply for a period of time. At this time, nitrogen plasma Plz is generated in the reaction chamber. Nitrogen in the nitrogen plasma Plz is positive ions such as N + and N2 +, and the lower electrode 26 has a lower frequency. Therefore, nitrogen ions are attracted toward the lower electrode 25. That is, even if a plasma generator of dual frequency power addition type is used, the introduction of nitrogen to the surface of the cobalt silicide film 24 is promoted by installing the semiconductor device on the electrode to which the low frequency power is applied. Will be done. At this time, oxygen in the natural oxide layer formed on the surface of the cobalt silicide film 24 or oxygen remaining in the chamber is also taken into the cobalt silicide layer 24, and is a barrier composed of a nitrogen-oxygen-cobalt-silicon compound. The compound layer 14 is formed near the surface of the cobalt silicide film 24.

[0091]

Next, as shown in FIG. 7C, the first aluminum film 22 is formed only on the barrier compound layer 14 by the selective CVD method using DMAH (dimethyl aluminum hydride). The selective CVD method using DMAH is a method capable of selectively depositing an aluminum film only on a conductive layer.

[0092]

Next, as shown in FIG. 7D, an insulating film 7 having a thickness of about 800 nm is formed on the first aluminum film 22, and the first aluminum film on the source / drain region 4 is formed on the insulating film 7. The connection hole 8 reaching 22 is opened.

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[0093]

Next, as shown in FIG. 7E, the second aluminum film 23 is formed in the connection hole 8 by the selective CVD method using DMAH.

Further, the aluminum alloy film 16 is deposited on the second aluminum film 23 and the insulating film 7 by the sputtering method, and the aluminum alloy film 16 is patterned by the photolithography method to form the metal wiring.

[0094]

FIG. 8 shows a cross-sectional structure of a semiconductor device formed by the above manufacturing method. That is, a gate oxide film 3, a gate electrode 5 made of a polysilicon film, a source / drain region 4, and a cobalt silicide film 24 formed on the source / drain region 4 and the gate electrode 5 on the silicon substrate 1. , Sidewalls 9 are formed. Then, the barrier compound layer 14 made of a nitrogen-oxygen-cobalt-silicon compound is formed on the entire surface of the cobalt silicide film 24, and the first aluminum film 22 is further formed on the barrier compound layer 14 of the cobalt silicide film 24. Has been done. A connection hole 8 reaching the first aluminum film 22 on the source / drain region 4 is formed in the insulating film 7 formed on the substrate, and the connection hole 8 has a first hole as a buried layer. 2 aluminum film 23 is formed. Further, the aluminum alloy film 16 forming the metal wiring is formed on the second aluminum film 23 and the insulating film 7. That is, in the semiconductor device of this embodiment, the barrier compound layer 14 is formed on the entire surface of the cobalt silicide film 24 on the source / drain regions 4 and the gate electrode 5, and the cobalt silicide film 24 is electrically connected to the barrier compound layer 14. The feature is that an aluminum film (low resistance layer) having a low resistance is formed.

[0095]
Next, details of the structure of the barrier compound layer 14 of the semiconductor device obtained in the present embodiment and details of the reaction prevention effect of the first aluminum film 22 in the semiconductor device of the present embodiment will be described.

[0096]

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FIGS. 12A to 12C show a cobalt silicide film which is not plasma-treated, a cobalt silicide film which is plasma-treated in N2 gas, and a cobalt silicide film which is plasma-treated in NH3 gas. It is a figure which shows the concentration profile of each element obtained as a result of having analyzed the area ¦ region by the XPS method.

However, in FIGS. 12A to 12C, the horizontal axis represents the depth from the surface, and the vertical axis represents the composition ratio of each element. Even in the cobalt silicide film which is not plasma-treated, since the heat treatment is performed at 750 ° C. in the nitrogen atmosphere during the formation of the silicide, nitrogen is introduced near the surface, but the peak of the nitrogen concentration is at the surface position, The nitrogen concentration decreased and nitrogen was lost at a depth of about 2 nm. Also, the oxygen concentration is so small that it can be almost ignored at a depth of about 2 nm. On the other hand, in the cobalt silicide film plasma-processed in N2 gas or NH3 gas, a peak of nitrogen concentration is found at a depth of about 2 nm from the surface. In addition, the region where the oxygen concentration is high extends to a depth position of about 6 nm from the surface. That is, in the cobalt silicide film subjected to the plasma treatment in the nitrogen atmosphere, the barrier compound layer made of the nitrogen-oxygen-cobalt-silicon compound is formed from the surface to a depth position of about 6 nm. I understand.

[0097]
In the present embodiment, as a result of forming the barrier compound layer 14 near the surface of the cobalt silicide film 24, the electric resistance of the cobalt silicide film 24 increased from 3.5Ω / □ to 3.6Ω / □, but the increase rate is It is 10% or less, which is a sufficiently low value that does not cause any particular problem in the operation of the transistor.

[0098]

FIG. 13 shows the annealing temperature dependence of the sheet resistance of various samples obtained by depositing an Al-0.5% Cu film as the first aluminum film 22 on the cobalt silicide film and performing annealing treatment. It is a diagram, and there are two types of cobalt silicide films that have been plasma-treated in N2 gas for 900 seconds, those that have been plasma-treated in NH3 gas for 900 seconds, and those that have not been plasma-treated.

The plasma treatment was performed by irradiating a cobalt silicide film having a thickness of 50 nm with nitrogen plasma in N2 gas or NH3 gas for 900 seconds. Then, in each of the samples, an Al-0.5% Cu alloy film was deposited to a thickness of about 200 nm on the cobalt silicide film,

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and then annealed for about 30 minutes.

[0099]

As can be seen from the figure, in the sample not subjected to the plasma treatment, the sheet resistance value when annealed at 400 ° C does not increase so much, but the sheet resistance value when annealed at 430 ° C significantly increases. is doing. On the other hand, in each of the plasma-treated samples, the increase in resistance value is suppressed even if they are annealed at 400 ° C and 430 ° C. That is, it is understood that the barrier compound layer formed on the surface of the cobalt silicide film suppresses the reaction between the aluminum film and the cobalt silicide film. Generally, since sintering is performed at about 400 to 450 ° C., such an effect of suppressing the sheet resistance value is of significant significance in practical use.

[0100]

Further, as a result of XPS analysis of the sample annealed at 430 ° C., those not treated with nitrogen plasma showed that Co2 Al19 or Co4 Al3 alloy was formed, whereas the sample treated with nitrogen plasma showed Al. Only the CoSi2 peak was seen. That is, it was found from the X-ray analysis that the reaction between Al and CoSi2 was suppressed up to 430 ° C by the nitrogen plasma treatment.

[0101]

As described above, according to this embodiment, the surface of the metal silicide is subjected to the nitrogen plasma treatment to form the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound on the surface of the metal silicide film. Therefore, the heat treatment in the subsequent steps can effectively prevent the metal generated by the reaction between the metal silicide film and the aluminum alloy from entering the silicon substrate. In other words, unlike the conventional method, it is not necessary to apply a heat treatment at 800 ° C. or higher to the silicide film to form the barrier compound layer, so that boron in the source / drain regions is absorbed in the metal silicide film and the P-channel transistor There is no problem that the saturation current value decreases. Further, since the nitrogen plasma treatment is performed at a low temperature of 550 ° C. or lower, it is possible to obtain an effect that the metal silicide film does not aggregate even for many kinds of metal silicide. That is, it is possible

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to increase the range of selection of the metal material forming the metal silicide.

[0102]

(Other Embodiments) In the first or third embodiment, the metal wiring on the connection hole 8 is formed from the aluminum alloy film 16 and the Al—Ti compound layer 15, but the Al—Ti compound layer 15 is It may be another metal film or its compound, or may not be provided. Further, another metal film may be laminated on the aluminum alloy film 16. Further, although the aluminum alloy containing silicon and copper is used as the aluminum alloy film 16, other aluminum alloy containing only metal such as silicon or scandium, or pure aluminum may be used. Further, copper or a copper alloy may be used instead of the aluminum alloy.

[0103]

In each of the above embodiments, N2 gas was used as the gas containing nitrogen. First, NH3 gas or H2 gas was flowed to remove the natural oxide film on the surface of the metal silicide film, and then a small amount of O2 gas was added to the N2 gas. Plasma may be generated in an atmosphere to which is added to form a barrier compound layer composed of a nitrogen-oxygen-titanium-silicon compound. In that case, since the amount of oxygen can be controlled, the distribution of each element in the barrier compound layer can be made as close as possible to the optimum state, and the barrier having a lower contact resistance and a higher junction leak prevention effect than using a natural oxide film A semiconductor device having a compound layer can be formed.

[0104]

Even when the plasma treatment is performed using NH3 gas, by performing the plasma treatment at 550 ° C or lower, it is possible to perform the plasma treatment under the conventional conditions of about 800 ° C to form titanium nitride. No trouble will occur. Further, even when performing plasma treatment using NH3 gas, under the condition that a barrier compound layer made of a metal-silicon compound such as nitrogen-oxygen-titanium can be formed by utilizing a natural oxide film. It is possible to exert the effect of the present invention.

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[0105]

FIG. 14 is a TEM photograph showing the barrier compound layer formed on the surface of the silicide when the surface of the cobalt silicide is plasma-treated using NH3 gas. The plasma generation conditions are the same as the N2 gas plasma generation conditions described in the fifth embodiment. It can be seen that a nitrogen-oxygen-cobalt-silicon compound layer (amorphous layer) having a thickness of about 4-6 nm is formed. Further, as shown in the data of FIG. 13 already described, the increase of the sheet resistance due to the reaction between aluminum and cobalt silicide during the heat treatment is suppressed up to 430 ° C., which is about the same as when using N 2 gas. It can be seen that there is an effect of suppressing the reaction. The reason is that, as shown in FIG. 12 already described, when NH3 gas is used, the composition ratio of oxygen in the nitrogen-oxygen-cobalt-silicon compound layer is reduced and the composition ratio of nitrogen is increased. It is presumed that the composition ratio of the two is adjusted appropriately.

[0106]

Needless to say, as the conditions for plasma formation, conditions other than the conditions in the above embodiments can be used.

[0107]

In each of the above-described embodiments, the step of forming the nitrogen-oxygen-silicon compound layer by subjecting the surface of the titanium silicide film or the cobalt silicide film to nitrogen plasma treatment is performed in a sputtering device or a selective CVD device by using copper in the connection hole, It may be performed in the same apparatus immediately before depositing aluminum, tungsten or an alloy thereof, or in the same apparatus immediately before forming copper, aluminum, tungsten or an alloy thereof only on the barrier compound layer by the selective CVD method. You may go in.

[0108]

Although titanium silicide is used as the metal silicide film in each of the above embodiments, cobalt silicide, nickel silicide, tantalum silicide, tungsten silicide, niobium silicide, palladium silicide, platinum silicide, molybdenum silicide, or the like may be used.

[0109]

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Further, in each of the above-described embodiments, in the step of forming the barrier compound layer composed of the nitrogen-oxygen-metal-silicon compound, instead of exposing the surface of the metal silicide film to plasma of a gas containing nitrogen, the surface of the metal silicide film is Of the nitrogen-oxygen-metal-silicon on the surface of the metal silicide film at a low temperature of 550 ° C. or lower by exposing the material to a gas containing nitrogen and irradiating it with ultraviolet rays or ionizing radiation at the same time by using energy such as ultraviolet rays. You may form the barrier compound layer which consists of an intermetallic compound.

Alternatively, instead of using plasma, by exposing the surface of the metal silicide film to an ion beam containing nitrogen, the energy of the ions is used to remove nitrogen-on the surface of the metal silicide film at a low temperature of 550 ° C. or lower. A barrier compound layer made of an oxygen-metal-silicon compound may be formed.

[0110]

In the first to fourth embodiments, in the step of forming the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound, any one of plasma treatment, irradiation with ultraviolet rays, irradiation with ion beam, etc. is selected. Also in this case, the potential for attracting nitrogen ions to the metal silicide side is preferably about 3 keV or less.

The reason will be described.

By analogy with the range of nitrogen ions in silicon, when the potential is 1 keV, the nitrogen concentration in silicon peaks at a depth of 3.8 nm and reaches 10 at a depth of 9.8 nm. Reduce to%. When the potential is 3 keV, the nitrogen concentration in silicon reaches a peak at a depth of 8.5 nm and decreases to 10% at a depth of 20.3 nm. Therefore, by suppressing the formation of the barrier compound layer to a depth of about 20 nm, which corresponds to 30% of the silicide film having a thickness of about 70 nm, it is possible to avoid an increase in sheet resistance and contact resistance.

[0111]

Further, the metal silicide film on which the barrier compound layer of the present invention is

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formed is not limited to the gate electrode and the source / drain regions shown in the above embodiments. For example, when the polysilicon film is used as a component (particularly an electrode) of a resistor or a capacitor, a silicide film on the polysilicon film may be formed, and even in that case, a metal silicide that contacts the upper wiring By forming the barrier compound layer of the nitrogen-oxygen-metal-silicon compound of the present invention on the surface of the film, the reaction between the buried layer and the metal silicide layer is achieved without depositing the barrier metal in the connection hole. There is an advantage that it is possible to effectively prevent the metal or the like generated in step 2 from entering the electrode or other members through the electrode.

[0112]

In the fifth embodiment, the barrier compound layer 14 made of a nitrogen-oxygen-metal-silicon compound is formed on the entire surface of the cobalt silicide film 24 on the source / drain regions 4 and the gate electrode 5. The first aluminum film 22 and the titanium silicide film 6 are in contact with each other via the barrier compound layer 14, but instead of the first aluminum film 22, a metal containing aluminum, a metal containing copper and tungsten are contained. The same effect is obtained when a metal film is deposited. For example, even when a tungsten film is used instead of the first aluminum film 22, the presence of the barrier compound layer 14 causes the cobalt silicide and tungsten to react with each other in the subsequent heat treatment at 600 ° C. or higher, so that the metal in the silicon substrate is reacted. Can be effectively prevented from entering and causing a junction leak.

[0113]

As described above, according to the present invention, the metal silicide film and the upper wiring are electrically connected via the buried layer in the connection hole formed in the insulating film on the metal silicide. In the semiconductor device described above, since the barrier compound layer made of the nitrogen-oxygen-metal-silicon compound is formed at least in the region near the surface of the metal silicide film that becomes the bottom surface of the connection hole, the barrier metal layer is formed in the connection hole. The compound can be prevented from entering the semiconductor substrate or the like without lowering the reliability due to the deposition of the metal, and thus the sheet resistance value of the entire metal silicide film can be kept low and the junction leakage can be suppressed. At the same time, it is possible to provide a semiconductor device having a highly reliable buried layer in the connection hole and a method for manufacturing the same.

[0114]

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Brief description of the drawings

[0115]
1 is a cross-sectional view showing a manufacturing process of the semiconductor device in the first embodiment.

[0116]
2 is a cross-sectional view of the semiconductor device in the first embodiment.

[0117]
3 is a cross-sectional view of the semiconductor device in the second embodiment.

[0118]
4 is a cross-sectional view showing a manufacturing process of the semiconductor device in the third embodiment.

[0119]
5 is a cross-sectional view of a semiconductor device in the third embodiment.

[0120]
6 is a cross-sectional view of a semiconductor device according to the fourth embodiment.

[0121]
7 is a cross-sectional view showing the manufacturing process of the semiconductor device in the fifth embodiment.

[0122]
8 is a cross-sectional view of a semiconductor device according to the fifth embodiment.

[0123]
<Figure 9> It is the figure which shows the elemental analysis result of the depth direction of the titanium silicide film surface of the semiconductor device in 1st execution form.

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[0124]
10 is a diagram comparing the junction leakage characteristics of the sample not subjected to the nitrogen plasma treatment, the sample subjected to the treatment of the first embodiment, and the reference sample.

[0125]
11 is a diagram showing the annealing temperature dependence of the sheet resistance of various samples annealed by depositing an Al alloy after performing the nitrogen plasma treatment.

[0126]
Fig. 12 XPS analysis of the vicinity of the surface of the CoSi2 film when plasma nitriding was not performed, plasma nitriding was performed in an N2 gas atmosphere, and plasma nitriding was performed in an NH3 gas atmosphere. It is a figure which shows each composition ratio.

[0127]
FIG. 13 is a diagram showing the temperature dependence of the sheet resistance of the AlCu / CoSi2 structure when plasma nitriding is not performed, when plasma nitriding is performed in an N2 gas atmosphere, and when plasma nitriding is performed in an NH3 gas atmosphere. ..

[0128]
14 is a TEM photograph near the boundary of the AlCu / CoSi2 structure when plasma nitriding is performed in an NH3 gas atmosphere.

[0129]
15 is a cross-sectional view showing a manufacturing process of a conventional semiconductor device.

[0130]
Explanation of symbols

[0131]

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1 Silicon Substrate 2 Field Oxide Film 3 Gate Oxide Film 4 Source / Drain Region 5 Gate Electrode 6 Titanium Silicide Film 7 Insulating Film 8 Connection Hole 9 Sidewall 10 Anode 11 Cathode 12 Blocking Capacitor 13 High Frequency Power Supply 14 Barrier Compound Layer 15 Al-Ti Compound layer 16 Aluminum alloy film 17 Tungsten film 18 DC power supply Plz Nitrogen plasma 22 First aluminum film 23 Second aluminum film 24 Cobalt silicide film 25 Upper electrode 26 Lower electrode 27 High-pass filter 28 Low-pass filter 29 High-frequency power supply 30 High-frequency power supply 30

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CLAIMS JPH09289178

1.
A semiconductor substrate, a metal silicide film formed on a part of the semiconductor substrate by siliciding the first metal, a metal film formed of a second metal on the metal silicide film, and the metal A semiconductor device, comprising: a barrier compound layer formed in a region near the surface of a silicide film and made of a nitrogen-oxygen-first metal-silicon compound.

2.
The semiconductor device according to claim 1, wherein the barrier compound layer is formed in a region near the surface of the entire metal silicide film.

3.
3. The semiconductor device according to claim 1, wherein the thickness of the barrier compound layer is at least a thickness sufficient to prevent the diffusion of the second metal into the barrier compound layer, and is 30 times the thickness of the metal silicide film. % Or less, a semiconductor device.

4.
The semiconductor device according to claim 1, wherein the barrier compound layer has a thickness in the range of 2 to 20 nm.

5.

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The semiconductor device according to claim 1, 2, or 3, wherein the position where the concentration of nitrogen is maximum in the barrier compound layer is deeper than the position where the concentration of oxygen is maximum. apparatus.

6.

The semiconductor device according to claim 1, further comprising: an insulating film formed on the metal silicide film; and a connection hole formed in a part of the insulating film and reaching the metal silicide film, wherein the metal film is A buried layer made of the second metal deposited in the connection hole.

7.

2. The semiconductor device according to claim 1, wherein an insulating film formed on the metal silicide film, a connection hole formed in a part of the insulating film and reaching the metal silicide film, and deposited in the connection hole. And a buried layer made of a third metal.

8.

The semiconductor device according to claim 1, 2, 3, 4, 5, 6 or 7, wherein the first metal is any one of titanium, cobalt, nickel, tantalum, tungsten, niobium, palladium, platinum and molybdenum. A semiconductor device characterized in that

9.

The semiconductor device according to claim 1, 2, 3, 4, 5, 6 or 7, wherein the second metal is any one of a metal containing aluminum, a metal containing copper and a metal containing tungsten. A semiconductor device characterized by the above.

10.

A first step of forming a metal silicide film made of a compound of a first metal and silicon on a semiconductor substrate, and irradiating the surface of the metal silicide film with ions containing nitrogen in a neutral or oxidizing atmosphere. Then, a second step of forming a barrier compound layer made of a nitrogen-oxygen-first metal-silicon compound in a region near the surface of the metal silicide film, and a step of forming a barrier compound layer of the metal silicide film on the barrier compound layer. And a third step of depositing a second metal to form a metal film.

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11.

11. The method for manufacturing a semiconductor device according to claim 10, wherein an insulating film is formed on the metal silicide film after the first step and before the second step, A step of selectively removing a portion to form a connection hole reaching the metal silicide film, and in the second step, a bottom portion of the connection hole in a region near the surface of the metal silicide film is formed. A method of manufacturing a semiconductor device, comprising forming the barrier compound layer in an exposed region, and filling the inside of the connection hole with the second metal in the third step.

12.

11. The method of manufacturing a semiconductor device according to claim 10, wherein after the second step, a step of forming an insulating film on the barrier compound layer of the metal silicide film, and a part of the insulating film are selectively formed. And a step of forming a connection hole that reaches the barrier compound layer by removing the second metal in the connection hole in the third step. Production method.

13.

13. The method of manufacturing a semiconductor device according to claim 12, wherein after the third step, a step of forming an insulating film on the barrier compound layer of the metal silicide film, and a part of the insulating film are selectively formed. And a step of forming a contact hole that reaches the barrier compound layer by removing the second metal, and a step of depositing a third metal in the contact hole to form a buried layer. Method of manufacturing semiconductor device.

14.

14. The method of manufacturing a semiconductor device according to claim 10, 11, 12 or 13, wherein in the second step, a plasma generating device in which a lower electrode as a cathode and an upper electrode as an anode are arranged in a chamber, In the chamber, the barrier compound layer is formed by exposing the metal silicide film to plasma of a gas containing nitrogen while the semiconductor substrate is placed on the lower electrode. Method.

15.

14. The method of manufacturing a semiconductor device according to claim 10, 11, 12, or 13, wherein in the second step, one of ultraviolet rays and ionizing radiation is exposed while exposing the surface of the metal silicide film to a gas containing nitrogen. A method for manufacturing a semiconductor device, which comprises forming the barrier compound layer by irradiation.

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16.

14. The method of manufacturing a semiconductor device according to claim 10, 11, 12 or 13, wherein in the second step, the barrier compound layer is formed by exposing the surface of the metal silicide film to an ion beam containing nitrogen. A method of manufacturing a semiconductor device, comprising:

17.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15 or 16, wherein the second step is performed at 550 ° C or lower.

18.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15 or 16, wherein in the second step, N2 gas is used as the gas containing nitrogen. Production method.

19.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15, 16, 17 or 18, wherein the metal silicide is obtained by flowing a gas containing hydrogen before the second step. A method of manufacturing a semiconductor device, further comprising a step of removing a natural oxide film on the film, wherein a gas containing oxygen is added in the second step.

20.

17. The method for manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15 or 16, wherein in the second step, ions containing nitrogen are introduced into the metal silicide film at an ion energy of 3 keV or less. A method of manufacturing a semiconductor device, comprising:

21.

21. A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, wherein titanium, cobalt, nickel is used as the metal silicide film in the first step. And tantalum, tungsten, palladium, platinum, and molybdenum, a silicide film is formed.

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22.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 or 20, wherein in the third step, a metal containing aluminum using a CVD method, A method of manufacturing a semiconductor device, comprising depositing one of a metal containing copper and a metal containing tungsten.

23.

A method of manufacturing a semiconductor device according to claim 10, 11, 12, 13, 14, 15, 15, 16, 17, 18, 19 or 20, wherein in the third step, titanium and aluminum alloys are continuously sputtered. Thus, the method for manufacturing a semiconductor device is characterized in that the metal film is composed of an Al—Ti compound layer and an aluminum alloy film.

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(54) 반도체 소자 및 그 제조 방법

요약

내용 없음.

대표도

도1

명세서

[발명의 명칭]

반도체 소자 및 그 제조 방법

[도면의 간단한 설명]

제1도 내지 제8도는 본 발명의 반도체 소자 제조 방법의 실시예 1에 수반된 단계를 도시하는 도면.

제9도 내지 제17도는 본 발명의 반도체 소자 제조 방법의 실시예 2에 수반된 단계를 도시하는 도면.

* 도면의 주요부분에 대한 부호의 설명

10 : P형 실리콘 기판 20 : FOX

30 : GASAD영역 50 : 다결정 실리콘층

100 : 소스 110 : 드레인

230 : 실리콘 이산화물층

[발명의 상세한 설명]

본 발명은 일반적으로 반도체 소자, 즉 반도체 집적 회로 IC)소자 뿐만 아니라 그 결과로된 소자를 제조하는 방법에 관한 것이다.

반도체 집적 회로(IC)는 반도체 기판에 형성된 다수의 전기적으로 상호 접속된 별개의 소자를 포함하는 소자와, 이들 IC중에는 MOS(metal-oxide semiconductor) 및 MES(metal-semiconductor) IC등에 포함한다. MOS IC는 통상적으로 다수의 MOSFET(CMOS 전계효과 트랜지스터)를 포함하는데 이 MOSFET 각각은 반도체 물질, 즉 실리콘의 활성 표면층을 포함한다. 각각의 MOSFET는 또는 활성층의 표면에 형성된 비교적 얇은 게이트 산화물(GOX)과, 예를들어, GOX의 표면상에 형성된 다결정 실리콘(폴리실리콘)의 게이트 전극 및, 상기 게이트 전극의 반대측에 MOSFET의 소스 및 드레인을 구성하는 활성층의 2개의 비교적 두껍게 도핑된 부분을 포함한다. 비교적 두꺼운(GOX와 비교하여) 필드 산화물(FO

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X)이 서로로 부터 MOSFET를 분리하고 전기적으로 절연하도록 작용한다. 유사하게, MES IC도 통상적으로 다수의 MESFET(MES전계효과 트랜지스터)를 포함하는데 MESFET는 MESFET의 게이트 전극이 금속이나 금속함유 혼합물, 즉 금속 실리사이드로 이루어지고 반도체 물질과 직접 접촉하고 있다는 점에서만 MOSFET와 다르다.

현재 상업적으로 유용한 IC에 있어서, 게이트 전극의 길이, 즉 전류 채널의 길이는 통상적으로 약 2마이크로미터(㎛)이며, 소스 및 드레인의 두께는 약 0.5㎛이다. 그러나 증가된 패킹 밀도(별개 소자의)를 가진 IC를 실현하기 위해, 게이트 전극 길이(즉 전류 채널 길이)가 약 1㎛보다 작거나 같게 축소될 것으로 기대된다. 동시에, 통상 짧은 채널 영향으로 불리는 어떤 바람직하지 않은 영향을 피하기 위해, 소스 및 드레인의 두께가 약 0.2㎛보다 작거나 같은 값으로 축소될 것이다(여기서 언급된 바람직하지 않은 짧은 채널 영향은 바람직하지 않은 임계 전압 시프와 소스-드레인 부임계 결핍 전류인데, 이것은 소스/드레인 두께에 대한 채널 길이의 비율이 비교적 작을때 즉, 약 2.5이하일때 발생한다. 짧은-채널 영향에 대해서는 제이.알.브로우스 등의 "MOSFET 소형화에 대한 일반 안내"란 논문을 참조하라).

비교적 얇은 소스 및 드레인, 즉 0.2㎛이하인 두께를 가진 소스 및 드레인은 바람직하지 못하게 큰 저항을 가지는데, 이것은 소자의 성능에 역으로 영향을 미친다. 비교적 얇은 소스 및 드레인을 사용하여 비교적 낮은 소스/드레인 저항을 실현하기 위해, 몰리브데늄 실리사이드($MoSi_2$), 텅스텐 실리사이드(WSi_2)나 티타늄 실리사이드($TiSi_2$)와 같은 금속 실리사이드의 위에 놓인 영역을 포함하도록 각각의 비교적 얇은 소스 및 드레인이 형성되는 것이 제안되었는데 그 목적은 저-저항 전류 분류기로서 작용하도록 한 것이다. 이에 관해 금속 실리사이드 커버된 소스 및 드레인의 효과적인(전기적)두께, 즉 소스-드레인-게이트 상호 작용에 포함되는 두께는 활성층의 표면 아래로 뻗어있으며 그 표면에 비교하여 아래에 놓인(두껍게 도핑된) 소스 및 드레인과 금속 실리사이드 영역의 결합된 두께이다.

금속 실리사이드 커버된 소스 및 드레인을 포함하는 IC를 제조하기 위한 이전의 시도는 소스 및 드레인을 형성하기 위한 통상적인 절차의 이용을 포함하고 있는데, 즉 소스 및 드레인이 필요한 실리콘 기판의 영역으로 소스 및 드레인 도펀트를 주입 및 확산하는 단계와 다음에 밑에 있는 소스 및 드레인의 표면에 Mo, W, Ti와 같은 금속을 증착시키는 단계를 포함하고 있다. 이때 증착된 금속은 대응하는 금속 실리사이드를 형성하도록 소스 및 드레인의 아래에 놓인 실리콘과 반응한다. 이 기술은 소스 및 드레인이 초기에(금속 실리사이드의 형성에 앞서) 실리콘내로 비교적 깊게 연장된 경우, 즉 실리콘내로 약 0.25㎛ 이상 연장된 경우에 효과적인 것으로 입증되었다. 그러나 이 기술은 소스 및 드레인이 초기에 실리콘내로 비교적 작은 거리만을 연장되어 있는 경우, 즉 약 0.25㎛보다 작거나 같은 거리만큼 연장되어 있는 경우에는 바람직하지 못한 것으로 입증되었는데, 이것은 바람직하지 못하게 큰 양의 소스/드레인 실리콘이 금속 실리사이드를 형성하는데 소비되어 결과적으로 소스/드레인 p-n 접합을 통해 연장된 즉 단락 회로시키는 금속 실리사이드 스파이크를 초래하기 때문이다.

금속 실리사이드 커버된 소스 및 드레인을 형성하기 위한 다른 기술이 1983년 IEDM 기술 다이제스트 670 내지 673페이지에 "실리사이드를 통한 측면 확산을 이용한 새로운 저 저항의 얇은 접합 형성 방법"이란 제목으로 에이취.오가바야시 등에 의해 기술되어 있다. 이 기술에 따라, 이와 같은 소스 및 드레인은 초기에 실리콘 기판의 표면상에 예를들어 0.1㎛의 두께를 가진 몰리브데늄 실리사이드($MoSi_2$) 영역을 제조함으로써 형성되는데, 이것은 실리콘 기판상에 몰리브데늄을 증착시키고 아래에 놓인 실리콘과 몰리브에늄을 반응시킴으로써 실현된다. 이때 소스/드레인 도펀트를 몰리브데늄 실리사이드로 확산되어 그곳으로 부터 소스/드레인 p-n 접합을 형성하도록 아래에 놓인 실리콘으로 확산된다. 즉 몰리브데늄 실리사이드 커버된 실리콘 기판이 개스 또는 고체의 도펀트 소스에 접촉되어져 한 단계로 몰리브데늄 실리사이드와 아래에 놓인 실리콘내로 도펀트를 효과적으로 확산시키기 위해 충분히 높은 온도와 충분히 긴 시간 주기동안, 즉 1000℃에서 20분동안 가열된다. 이와 달리 도펀트는 2단계 공정으로 실리콘내로 확산되는데, 제1단계는 초기에 몰리브데늄 실리사이드 커버된 실리콘 기판을 비교적 낮은 온도, 즉 800℃로 가열하여 가스 또는 고체의 도펀트 소스로 부터 몰리브데늄 실리사이드내로(실리콘내로는 확산되지 않음)도펀트를 확산시키는 것이다. 계속해서 도펀트는 실질적으로 보아 높은 온도, 즉 950℃나 1000℃로 기판을 가열함으로써 몰리브데늄 실리사이드로 부터 실리콘내로 확산된다. 1단계 확산 공정을 비교적 깊은 소스 및 드레인을 만드는데, 즉 만일 몰리브데늄 실리사이드가 0.1㎛ 두께이면, 소스 및 드레인은 실리사이드의 상부 표면 아래로 약 1.5㎛ 연장된다. 2단계 확산 공정은 보다 얕은 소스 및 드레인을 만드는데, 이것은 비교적 깊은 것으로서, 만일 몰리브데늄 실리사이드가 0.1㎛ 두께라면, 소스 및 드레인은 실리사이드의 상부 표면아래로 약 0.36㎛ 연장된다.

금속 실리사이드 커버된 소스 및 드레인을 형성하기 위해 이전에 사용된 또다른 기술에 있어서, 텅스텐 실리사이드(WSi_2) 영역이 초기에 실리콘 기판상에 형성되고 텅스텐 실리사이드내로 도펀트가 주입된다(확산이 아님)(1985년 IEDM 기술 다이제스트 407 내지 410페이지에 있는 에프.씨.쇤 등의 "도핑된 실리사이드 기술에 의한 0.1㎛ N^+/P와 P^+/N 접합의 형성"을 참조) 이때 주입된 도펀트는 통상적인 용광로 어닐링 기술이나 금속 열 어닐링(RTA)기술을 이용하여 기판을 가열함으로써 텅스텐 실리사이드로 부터 실리콘 기판내로 확산된다(RTA에 대해서는 1983년 전자화학회의 저널 130권의 484페이지에 있는 티.오.세리웍크의 "단시간 어닐링"을 참조) 중요하게도(에프.씨.쇤 등에 의해 알려진 바와 같이), 텅스텐 실리사이드 영역의 두께는 0.2㎛이며, 대응하는 주입량과 가열 온도 및 가열 시간은 텅스텐 실리사이드의 특정 두께에 대해 모두(추정적으로)특수하게 맞추어진다. 결과적으로, 상기 특정 기술은 단지 0.3㎛보다 크거나 같은 깊이(텅스텐 실리사이드의 상부 표면으로 부터 측정될때)를 가진 소스 및 드레인만을 만들게된다.

1986년 산 디에고의 VLSI에 관한 1986 심포지엄에서 논문 다이제스트의 "서브-미크론 CMOS에 대한 $TiSi_2$ 및 WSi_2 실리사이드된 낮은 접합의 비교"란 제목으로 엔.고바야시 등에 의해 상기 기술의 변

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형이 기술되어 있다. 여기에서는 텅스텐 실리사이드 또는 티타늄 실리사이드의 0.1㎛ 두께 영역이 초기에 실리콘 기판상에 형성되고, 소스/드레인 도펀트가 실리사이드 내로 주입되어 실리사이드로부터 실리콘내로 확산된다. 그러나 텅스텐 실리사이드의 경우에 엔.고바야시 등의 저널 논문의 제1도에 도시된 바와같이, 이 논문의 저자는 0.2㎛보다 훨씬 큰 깊이(텅스텐 실리사이드의 상부 표면으로 부터 측정할때), 즉 0.26㎛ 및 0.28㎛의 깊이를 가진 소스 및 드레인을 만드는 주입량과 가열 온도 및 가열 시간을 가르쳐주고 있다. 이에 대비하여, 티타늄 실리사이드의 경우에는 제1도에 도시된 바와같이 저자가 0.2㎛보다 작은 깊이(티타늄 실리사이드의 표면으로 부터 측정할때), 즉 0.16㎛의 깊이를 가진 소스나 드레인을 만드는 비소 주입량과 가열 온도 및 가열 시간을 가르쳐 주고 있지 않다. 그러나 제1도로 부터 명백한 바와같이, 티타늄 실리사이드/실리콘 인터페이스에서의 비소의 농도는 비교적 낮다. 이것은(저널 논문의 저자의 주장과는 반대로) 상기 비교적 낮은 인터페이스 농도가 바람직하지 못하게 높은 특정 저항(Rc)을 유도하기 때문에 매우 중요한데, 여기서 Rc는 $10^{-6}\Omega$-Cm^2 보다도 크다. 사실 상기 저널 논문에서 저자는 인터페이스 비소 농도를 증가시키기 위해(추정상 Rc를 낮추기 위한 목적으로) 추가의 비소를 실리콘(티타늄 실리사이드가 아님)대로 주입하는 바람직성을 나타내고 있다. 그러나 불행하게도 알려진 바와같이, 이와 같은 절차는 실리콘 기판이 추가의 도펀트 확산, 결과적으로 비교적 깊은 소스 및 드레인을 만드는 실리콘내로의 생성 주입 손상을 어닐링하기 위해 비교적 높은 온도로 가열되어야만 하기 때문에 바람직하지 못하다.

그러므로 IC제조 방법의 개발에 종사하는 사람들은 약 $10^{-6}\Omega$-cm^2 이하의 Rc를 나타내는 금속 실리사이드를 포함하는 비교적 얕은 소스 및 드레인을 가진 IC를 제조하기 위한 방법을 추구해왔다.

본 발명은 금속 함유 물질 영역, 즉 기초 금속이나 금속 실리사이드와 같은 금속 함유 혼합물을 함유하는 영역으로 커버된 소스나 드레인을 형성하기 위한 새로운 기술을 포함한다. 중요하게도 이 새로운 기술은 약 0.2㎛이하의 깊이(물질 영역의 상부 표면과 비교하여)를 갖고 약 $10^{-6}\Omega$-cm^2 이하의 Rc를 나타내는 물질 영역 커버된 소스나 드레인을 만든다.

본 발명의 기술에 따라, 0.2㎛이하의 평균 두께 t를 가진 금속 함유 물질 영역이 초기에 반도체 기판의 표면상에 형성된다. 그 다음에, 하나 혹은 그 이상의 도펀트가 상기 영역에 주입되고, 반도체 기판이 가열되어 상기 도펀트가 상기 영역으로 부터 기판내로 확산되게 된다. 약 $10^{-6}\Omega$-cm^2 이하의 Rc를 발생하기 위해, 가열 절차는 상기 물질 영역/기판 인터페이스에 인접한 기판에서 최소한 하나의 도펀트를 집중시켜야 하는데, 이것은 기판 가열전의 인터페이스에서의 쇼트키 전위 장벽의 높이에 의해 결정되는 최소 값보다 크거나 같다. 상기 최소값을 실현하기 위해 다음 3조건이 만족되어야 한다고 알려져 있다. 제1조건은 가열 절차 동안에 사용된 온도에서 기판내의 최소한 하나의 도펀트의 고체 용해도가 상기 최소값보다 크거나 같아야 한다는 것이다. 제2조건은 상기 동일한 도펀트에 있어서, 상기 물질 영역의 평균 두께에 대한 대응하는 주입량의 비율이 상기 가열 온도에서 상기 물질 영역내의 상기 도펀트의 고체 용해도의 약 1/2보다 크거나 같아야 된다는 것이다.(이것에 대해서, 예를들어, 엔.고바야시 등에 의해 사용된 비소 주입량이 상기 제2임계 요구조건을 만족하지 못한다고 결정되었다). 원하는 인터페이스 농도를 실현하고 유용한 소스/드레인 접합을 실현하기 위해 만족되어야할 제3조건은, 상기 동일한 도펀트에 대해 상기 물질 영역내로 주입되는 도펀트 이온의 총수효가 아래에 놓인 확산된 소스 및 드레인을 형성하는데 필요한 수보다 실질적으로 커야된다는 것이다. 만일 상기 물질 영역/기판 인터페이스에 가까이 인접한 기판에서의 도펀트의 농도의 필요한 최소값이 Co로 표시되고 상기 물질 영역의 바닥과 비교하여 소스/드레인 접합의 원하는 깊이가 X로 표시되면 제3조건은 자동적으로 $1 \geq g5Co \cdot X/2$가 만족된다. 실예로 제2조건을 만족하는 주입량은 또한 제3조건도 만족한다. 그러나 주입량의 제2조건을 만족하지만 5Co·X/2 보다 작은 경우에 제3조건은 Co·X/2보다 크거나 같은 양만큼 상기 주입량을 증가시킴으로써 확실하게 만족되게 된다.

본 발명의 기술은 또한 원하는 깊이를 가진 소스 및 드레인을 만드는데 필요한 가열 온도-시간 프로필을 선택하기 위한 절차(후술됨)를 포함한다.

본 발명은 MOS나 MES 반도체 IC와 같은 반도체 소자뿐 아니라 그 합성 소자를 제조하기 위한 방법을 모두 포함하고 있다. 본 발명의 방법에 따라 제조된 소자는 금속 함유 물질 영역, 즉 텅스텐(W)과 같은 기초 금속을 함유하는 영역으로 커버된 최소한 하나의 소스나 드레인을 포함하고 있다. 이와 달리 금속 함유 물질 영역은 금속 실리사이드, 즉 코발트 실리사이드($CoSi_2$), 티타늄 실리사이드($TiSi_2$), 텅스텐 실리사이드(WSi_2), 몰리브데늄 실리사이드($MoSi_2$), 탄탈륨 실리사이드($TaSi_2$)나 플라티늄 실리사이드(ptSi)와 같은 금속 함유 혼합물을 포함한다. 또한 상기 물질 영역의 상부 표면에 비교하여 상기 물질 영역으로 커버된 소스나 드레인의 깊이는 약 0.2㎛ 보다 작거나 같다. (본 발명의 목적을 위해 상기 물질 영역 커버된 소스나 드레인의 깊이는 상기 물질 영역의 상부 표면에 대한 최소 면적 평면 근사부로 부터 소스나 드레인이 형성되는 반도체 기판과 소스나 드레인 사이의 인터페이스의 최저점까지 직각으로 연장된 길이다. 만일 예를들어 소스나 드레인이 n형 전도성이면 인터페이스는 소스나 드레인에서의 n형 도펀트의 농도가 기판에서의 p형 도펀트의 농도가 같은 (그 역도 마찬가지임) 점들이 궤적이다. 이와 같은 인터페이스는 2차 이온 질량 분광학(secondary ion mass spectroscopg : SIMS)과 같은 종래의 기술을 이용하여 쉽게 위치된다.) 또한 아래에 놓인(확산된) 소스나 드레인에 대한 상기 물질 영역의 특정 접촉 저항, Rc는 약 $10^{-6}\Omega \cdot cm^2$ 보다 작거나 같다.(Rc는 IEEE전자 소자란 책의 544페이지에 있는 케이.케이.에지, "MOSFET의 접촉 저항을 측정하기 위한 새로운 기술" 에 기술된 종래의 절차를 이용하여 쉽게 측정된다.)

본 발명의 방법에 따라, 상기 물질 영역 커버된 소스나 드레인이 초기에 실리콘이나 갈륨 비소와 같은 반도체 물질을 포함하는 기판상에 상기 물질 영역을 형성함으로써 형성된다. 이와 같은 물질 영역은 예를들어, 종래 기술, 즉 종래의 스퍼터링(sputtering)기술을 이용하여, 기판상에 상기 영역을 구성하는 물질을 침착시킴으로써 형성된다. 이와 달리, 만일 상기 물질 영역이 예를들어 금속 실리사이드를 포함하고 기판이 실리콘으로 되어 있으면, 상기 물질 영역은 대응하는 기초 금속을 실리콘 기판상에 침착시키고 금속 실리사이드를 형성하기 위해 침착된 금속을 아래에 있는 실리콘과 반응시

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킴으로써 최소한 부분적으로 쉽게 형성된다. 약 0.2㎛보다 작거나 같은 깊이를 가진 상기 물질 영역 커버된 소스나 드레인을 실형하기 위해서는 상기 물질 영역의 최대 두께, 즉 결과적으로 평균 두께 (일반적으로 균일하지 않은 두께임)가 0.2㎛보다 작아야 된다. 또한 (균일하지 않은 두께의) 상기 물질 영역의 최소 두께는 약 0.1㎛보다 크거나 같은 것이 양호하다. 약 0.1㎛보다 작은 최소 두께는 바람직하지 못한데 이것은 다른 이유중에서, 상기 물질 영역의 대응하는 부분이 종종, 주입 단계동안에 매우 많은 양의 도펀트를 상기 물질 영역이 아닌 기판내로 주입되도록 허용하는 매우 많은 수의 핀구멍을 포함하게 되기 때문이다.

상기 물질 영역을 형성한 후에, 하나 혹은 그 이상의 도펀트가 상기 물질 영역내로 주입되고, 계속해서 원하는 소스나 드레인을 형성하기 위해 상기 물질 영역으로 부터 상기 기판내로 주입된 도펀트가 확산되도록 기판이 가열된다. 만일 기판 반도체 물질이 p형 전도성이면, 주입된 도펀트는 기판에서 전자도우너를 형성해야 하며, 만일 기판 반도체 물질이 n형 전도성이면 상기 도펀트는 전자 액셉터를 형성해야 한다. 예를들어 실리콘의 경우에, 유용한 도오너 이온은 인(p)과 비소(As)이온을 포함하며, 동시에 유용한 액셉터 이온은 붕소(B)이온을 포함한다.

전술한 바와같이, 약 $10^{-6}\Omega \cdot cm^2$보다 작거나 같은 Rc를 실현하기 위해, 기판 가열 절차는 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 최소한 하나의 도펀트의 농도를 산출해야 되는데 이것은 기판 가열 이전의 상기 물질 영역/기판 인터페이스에서의 쇼트키 전위 장벽의 높이에 의해 결정되는 최소값보다 크거나 같다. 즉, 상기 전위 장벽 높이를 아는 것은 대응하는 최소값을 의미하고 있다. 이점에 있어서, 금속 함유 물질과 반도체 물질 사이의 인터페이스에서의 쇼트키 전위 장벽 높이는 원하는 Rc를 발생시키기 위해 인터페이스 도펀트 농도의 대응하는 최소값이 필요한 바와같이 문헌상 쉽게 이용할 수 있다. 예를들어, n형이나 p형 실리콘과 다양한 기초 금속 사이의 인터페이스에서의 쇼트키 전위 장벽 높이는 에스.엠.스제의 "반도체 소자의 물리학" 제2판(1981) 292페이지에서 찾아볼 수 있다. 비슷하게 예를들어 n형 또는 p형 실리콘과 다양한 기초 금속 사이의 인터페이스 사이의 쇼트키 전위 장벽 높이는 에스.피.유라카의 "VLSI 응용을 실라이드"(1983) 15페이지에서 찾아볼 수 있다.

또한 거의 모든 쇼트키 전위 장벽 높이에 대응하는 약 $10^{-6}\Omega \cdot cm^2$보다 작거나 같은 Rc를 발생시키는데 필요한 최소 인터페이스 도펀트 농도는 에스.엠.스제의 상기 참조 논문의 304 내지 305페이지에서 찾아볼 수 있다. 예를들어 만일 상기 물질 영역이 코발트 실리사이드($CoSi_2$)를 포함하고 기판이 p형 실리콘을 포함하며 주입된 n형 도펀트중 하나가 비소(As)라면, 에스.피.유라카의 상기 참조 온도에 따라, 대응하는 쇼트키 전위 장벽 높이는 0.64볼트이며, 에스.엠.스제의 상기 참조는 논문에 따라 비소의 대응하는 최소 인터페이스 농도는 약 $1\times10^{20}cm^{-3}$이다. 비슷하게, 만일 상기 물질 영역이 티타늄 실리사이드($TiSi_2$)를 포함하고 기판이 n형 실리콘을 포함하며 주입된 p형 도펀트중 하나가 붕소(B)라면, 에스.피.유라카의 상기 논문에 따라 대응하는 쇼트키 전위 장벽 높이는 0.5볼트이고 에스.엠.스제의 상기 논문에 따라 붕소의 대응하는 최소 인터페이스 농도는 약 $3\times10^{19}cm^{-3}$이다.

또한 전술한 바와같이, 약 $10^{-6}\Omega \cdot cm^2$보다 작거나 같은 Rc를 발생시키기 위해 필요한 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 도펀트 농도를 실현하기 위해서는 3가지 조건이 만족되어야 한다고 알려져 있다. 제1조건은 기판 가열 절차동안에 사용된 온도에서 최소한 하나의 도펀트의 기판에서의 고체 용해도가 전술한 최소 인터페이스 농도보다 크거나 같아야 된다는 것이다. 중요하게도, 반도체에서 도펀트의 고체 용해도는 일반적으로 매우 민감하며 온도에 따라 증가한다. 결과적으로 제1조건은 사실 기판 가열 절차동안에 사용될 수도 있는 온도에 대한 최소값 Tmin을 강요한다. 즉, 최소한 하나의 도펀트의 기판에서의 고체 용해도가 원하는 Rc를 실현하는데 필요한, 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 최소 도펀트 농도의 최소한 같게 되는 것을 보장하기 위해 가열 온도는 Tmin보다 크거나 같아야 된다. 이점에 있어서, 온도 함수로서의 다양한 반도체 물질에서의 다양한 도펀트의 고체 용해도는 문헌에서 이용 가능하다.(즉 에서 엠.스제에 의해 출판된 "VLSI 기술에서의 제이.씨.씨.츠아이" 198 내지 199페이지를 참조하라).

결과적으로 제1조건을 만족하는데 필요한 Tmin은 쉽게 결정된다. 예를들어, 740℃, 800℃ 및 900℃에서, 실리콘에서의 비소의 고체 용해도는 각각 $1\times10^{20}cm^{-3}$, $1.5\times10^{20}cm^{-3}$, $2\times10^{20}cm^{-2}$이다. (상기 논문 제이.씨.씨.츠아이를 참조). 만일 비소가 n형 실리콘에서 n형 도펀트로서 사용되고 상기 물질 영역이 $CoSi_2$로 이루어져 있으면, 전술한 바와같이 원하는 Rc를 실현하는데 필요한 최소 인터페이스 농도는 $1\times10^{20}cm^{-3}$이며, 결과적으로 Tmin은 740℃이다. 유사하게, 800℃ 및 900℃에서 실리콘에서의 붕소의 고체 용해도는 각각 $3\times10^{19}cm^{-3}$ 및 $6\times10^{19}cm^{-3}$이다. 만일 붕소가 n형 실리콘에서 p형 도펀트로서 사용되고 상기 물질 영역이 $TiSi_2$라면, 전술한 바와 같이 원하는 Rc를 실현하는데 필요한 최소 인터페이스 농도는 $3\times10^{19}cm^{-3}$이며, 결과적으로 Tmin은 800℃이다.

만족되어야 할 제2조건은 위에서 언급된 최소한 하나의 도펀트에 대해 상기 물질 영역의 두께 t에 대한 대응하는 주입량의 비율, 즉 I/t가 기판 가열동안에 사용된 온도(필수적으로 대응하는 보다 크거나 같은)에서 상기 물질 영역에서의 상기 도펀트의 고체 용해도의 1/2보다 크거나 같아야 되며, 바람직하게는 더 커야된다는 것이다. 여기서 논의되는 고체 용해도는 기판 가열 절차 동안에 사용된 온도에서, 상기 물질 영역과 기판 사이의 인터페이스를 포함하여 상기 물질 영역에서의 최소한 하나의 도펀트의 포화 레벨을 말한다. 중요하게도, 이 포화 레벨은 온도에 민감하며, 일반적으로 온도에 따라 증가한다. 또한 이 포화 레벨은 상기 물질 영역의 합성 성분과 상기 물질 영역의 결정성의 정도에 의존한다(즉, 예를들어 다결정 물질의 경우에, 도펀트는 종종 그레인(grain) 및 그레인 경계내에 분배된다). 또한 상기 포화 레벨은 상기 물질 영역/기판 인터페이스의 특성에 의존하는데, 즉 도펀트가 상기 인터페이스에서 비교적 높게 농축되는지의 여부에 의존한다.

일반적으로, 기판 가열 절차동안에 사용된 온도에서, (상기 물질 영역/기판 인터페이스를 포함하여)

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상기 물질 영역내의 도펀트의 고체 용해도는 실험적으로 결정된다. 즉, 본 발명에 따라, 소자에 사용된 상기 물질 영역과 동일한 평균 두께를 가진 상기 물질 영역의 제어 샘플이(소자에 사용된 기판과 동일한 합성 성분 및 구조를 가진)반도체 기판상에(소자의 제조에 사용된 바와 동일한 기술을 이용하여)형성된다. (중요하게도, 이하에서 더욱 자세히 설명되는 바와같이, 제어 샘플의 상부 표면의 영역 A는 상기 물질 영역의 그것과 동일하게 되는 것을 필요로 하지 않는다. 제어 샘플을 지탱하는 기판은 비워진 용광로, 즉 주위 압력이 예를들어 10^{-6} 토르(torr)의 값으로 낮아지는 용광로에 배치된다. 이때 관심있는 도펀트를 포함하는 가스가 용광로내로 흘러들어간다. 예를들어, 만일 인이라면 유용한 인 함유 가스는 PH_3이다. 유사하게, 만일 도펀트가 비소라면, 유용한 비소 함유 가스는 AsH_3이며, 만일 도펀트가 붕소라면 유용한 붕소 함유 가스는 B_2H_6이다(PH_3, AsH_3 및 B_2H_6는 매우 유독성 가스이므로 적당한 안전 예방책이 사용되어야 한다는 것을 주목하자). 이점에 있어서, 도펀트 함유 가스의 유동률은 상기 가스의 부분 압력이 주위 압력의 최소한 백배가 되도록 충분히 높아야 되는데, 만일 주의 가스 압력이 10^{-6} 토르이면 도펀트 함유 가스의 부분 압력은 최소한 10^{-4} 토르가 되어야 한다. 이 필요성은 제어 샘플이 필수적으로 주위의 오염물질이 아닌 도펀트에 의해서만 (다음 단계 동안에)포화되는 것을 보장하기 위한 것이다. 도펀트 함유 가스가 용광로내로 흐르는 동안, 용광로는 관련있는 온도, 즉 기판 가열동안에 사용될 온도로 가열되게 된다. 제어 샘플내에서 도펀트 포화를 실현하기 위해서는 이 온도가 최소한 1분동안 유지되어야 하는데, 최소한 30분동안 유지되는 것이 바람직하다.

도펀트 함유 가스에 영향을 받은 후에 제어 샘플은 용광로로 부터 이동되며 제어 샘플/기판 인터페이스를 포함하며 제어 샘플내의 도펀트 원자의 총 수 N이 예를들어 종래의 SIMS 기술을 이용하여 측정된다. 상기 물질 영역에서 도펀트의 고체 용해도는 바로 N/At이다. (원자의 총 수 N는 표면 영역 A에 선형적으로 비례한다는 것을 주목하자.) 결과적으로, 표면 영역은 다르지만, 동일한 평균 두께를 가진 제어 샘플은 동일한 값의 고체 용해도를 산출하게 된다). 결과적으로 제2조건을 만족하기 위해서는 $I/t \geq g0.5N/At$가 되도록 I가 선택되어야 한다.

전술한 실험적 절차를 이용하여, 예를들어 만일 상기 물질 영역이 코발트 실리사이드로 이루어지고, 0.07㎛의 평균 두께를 가지며, 실리콘 기판위에 놓여 있고, 도펀트가 비소라면, 5×10^{15} cm^{-2} 이상의 주입량이 800℃의 온도에서 제2조건을 만족한다. 비슷하게, 상기 물질 영역이 티타늄 실리사이드로 이루어져 있고 0.08㎛의 평균 두께를 가지며 실리콘 기판위에 놓여있고, 도펀트가 붕소라면, 1×10^{16} cm^{-2} 이상의 주입량의 800℃의 온도에서 제2조건을 만족한다.

원하는 Rc를 실현하고 유용한 소스/드레인 접합(즉 예를들어 0.5볼트의 전압과 25℃의 온도에서 반전 전류에 대한 진행 전류의 비율이 10^6 보다 크거나 같아지는 접합)을 실현하기 위해 만족되어져야 하는 제3조건은, 최소한 하나의 도펀트에 대해, 상기 물질 영역내로 주입된 도펀트 이온의 총수가 아래에 놓인, 확산된 소스나 드레인을 형성하는데 필요한 수보다 실질적으로 커야된다는 것이다. 만일 상기 물질 영역/기판 인터페이스에 인접한 상기 기판에의 도펀트 농도의 최소값이 Co로 표시되고 상기 물질 영역의 바닥과 비교하여 소스/드레인 P-N접합의 원하는 깊이가 X로 표시되면, 제3조건은 자동적으로 $1 \geq 5Co \cdot X/2$이 만족되도록 제공된다. 그러나 만일 주입량이 제2조건을 만족하지만 $5Co \cdot X/2$보다 작다면, 제3조건은 보다 크거나 같은 양만큼 상기 주입량을 증가시킴으로써 확실하게 만족되게 된다. 이점에 있어서, 위에서 주어진 두 주입량은 또한 제3조건도 만족한다.

상기 금속 함유 물질 영역내로 주입된 이온의 에너지는 근본적으로 모든 이온, 즉, 이온의 최소한 90퍼센트가 상기 영역내로 주입되는 기초적인 반도체 기판내로는 주입되지 않도록 선택된다는 것을 주목하자. 이점에 있어서, 또한 실리콘의 본 발명에 사용된 금속 함유 물질 영역보다 밀도가 높지 않고, 그러므로 동일한 에너지를 가진 동일한 이온이 상기 물질 영역보다 더 큰 깊이로 실리콘내로 관통된다는 것을 주목하자. 결과적으로, 거의 모든 이온이 상기 물질 영역내로 주입되는 것을 보장하기 위해, 이온 에너지는 상기 물질 영역의 두께이하의 실리콘내로의 대응하는 관통 깊이를 산출하도록 선택된다.(이온 에너지의 함수로서의 실리콘내로의 이온 관통 깊이는 알.에이.콜콜레이저의 "마이크로 전자공학처리 및 소자 설계" 150 내지 153페이지에서 찾아볼 수 있다.)

예를 들어, 60keV 이하의 주입 에너지(0.07㎛보다 작거나 같은 깊이로 실리콘을 관통하는 비스 이온의 90퍼센트가 되는 비소 이온 에너지)를 이용하여 0.07㎛의 평균 두께를 가진 코발트 실리사이드의 영역내로의 비소 이온의 주입은 거의 모든 비소 이온이 코발트 실리사이드내로 주입되는 것을 보장한다. 유사하게, 10keV 이하의 주입 에너지(0.08㎛ 이하의 깊이로 실리콘을 관통하는 붕소 이온의 90퍼센트가 되는 붕소 이온 에너지)를 이용하여, 0.08㎛의 평균 둑께를 가진 티타늄 실리사이드의 영역내로 붕소 이온을 주입하면 거의 모든 붕소 이온의 티타늄 실리사이드로 주입되는 것을 보장한다.

본 발명은 또한 원하는 소스/드레인 깊이를 실현하기 위해 기판 가열 동안에 이용될 온도-시간 프로필을 선택하기 위한 반복적(iterative) 기술을 포함하고 있다. 여기서, 상기 물질 영역이 두게는 기판의 도핑 레벨, NA 일대 공지되거나 지정된 것을 가정 한다. 또한 상기 세가지 조건이
만족되었고, 기판 가열의 결과로서 상기 물질 영역/기판 인터페이스에 인접한 기판내의 도펀트 농도가 원하는 Rc를 실현하는데 필요한 (공지된) 최소값인 Co보다 크거나 같은 것으로 가정한다.
처음에, 또한 간편성을 위해, 필수적으로 Tmin보다 크거나 같은 온도 T만이 가열 절차 동안에 사용된다고 가정한다. 만일 변수 X′가 상기 물질 영역의 바닥에 대한(확산된) 소스나 드레인내의 점의 수직 위치를 표시하고, T가 시간을 나타내고, D(=D(T))가 기판에서의 도펀트의 확산 계수를 표시하고, Co′가 약 10^{-6} Ω-cm^2 이하의 Rc를 산출하는 상기 물질 영역/기판 인터페이스에 인접한 원하는 도펀트 농도를 나타낸다면, C가 공식

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$$C(X', \gamma) = Co' \cdot erfc(X'/2\sqrt{D\Gamma}) \quad \cdots\cdots (1)$$

에 의해 잘 근사된다는 것이 결정되었다. 여기서 erfc는 상보 에러 함수이다. X′가 X(상기 물질 영역의 바닥에 비교한 소스나 드레인의 원하는 깊이)와 같아지는 소스나 드레인의 바닥에서, C(X, Γ)는 필수적으로 NA와 동일하며, 그러므로 공식(1)로 부터,

$$erfc(X/2\sqrt{D\Gamma}) = NA/Co' \quad \cdots\cdots (2)$$

이다.

공식(2)의 오른쪽이 공지된 양이기 때문에, 공식(2)에서 상보 에러 함수의 독립변수(argument)가 알려지며, 즉 예를 들어 erfc 함수의 테이블로 부터 쉽게 결정된다(엠.아브라모위쯔와 아이.에디.세건에 의해 출판된 "수학적 함수의 핸드북"에서 윌터 고쯔찌를 참조하라). 그러나 X는 알려져 있다. 또한 D는 필수적으로 온도의 함수이며, 단일 온도만이 가열 절차동안에 사용되기 때문에 D도 또한 낮게되며, 단일 온도T에 대응하는 D의 값은 예를 들어, 테이블(제이.씨.씨.쯔아이의 상기 참조 논문을 참조)로 부터 쉽게 결정된다. 그러므로, erfc 함수의 독립 변수의 값이 알려지고, X와 D의 값이 알려졌기 때문에 Γ(가열시간)의 값은 쉽게 추론할 수 있다. 만일(제어 샘플의 바닥과 비교하여) 소스나 드레인의 생성 깊이가(예를 들어 SIMS 기술을 통해 결정될때) 원하는 깊이가 아니면 가열시간 및 가열온도가 변경된다.

만일 대응하는 다수의 시간 간격 Γ_1, $\Gamma_2 \cdots \Gamma_n$에 대해 다수의 가열온도 T_1, $T_2 \cdots T_n$을 사용하는 것이 필요하다면, C는

$$C(X', T_1, T_2 \cdots T_n) = Co' erfc(X'/2\sqrt{D_1(T_1)T_1 + D_2(T_2)T_2 + \cdots D_n(T_n)T_n}) \quad \cdots\cdots (3)$$

의해 잘 근사된다. 여기서 D_1, D_2, $\cdots D_n$는 온도 T_1, T_2, $\cdots T_n$에서 기판내의 도펀트의 확산 계수를 표시한다. 그러므로, C가 NA와 동일한, 즉 X′=X인 소스나 드레인의 바닥에서,

$$erfc(X/2\sqrt{D_1T_1 + D_2T_2 + \cdots (D_nT_n)}) = NA/Co' \quad \cdots\cdots (4)$$

이된다. 전술한 바와 같이, 공식(4)의 오른쪽은 알려져 있고, 그러므로 공식(4)에서 erfc 함수의 독립변수는 쉽게 결정된다. 또한 X는 알려져 있고, T_1, T_2, $\cdots T_n$가 지정된 것으로 가정하면 D_1, D_2, $\cdots D_n$도 또한 쉽게 결정된다. 그러므로 공식(4)를 만족하는 Γ_1, Γ_2, $\cdots \Gamma_n$의 값이 쉽게 선택된다. 만일 Γ가 원하는 소스/드레인 깊이를 산출하지 못하면, 반복적 절차에 따라, Γ 및 T가 변경된다.

상기 반복적 기술을 이용하여, $1 \times 10^{16} cm^{-3}$의 도핑레벨을 가진 P형 실리콘 기판을 가열하는 단계와 800℃의 온도로 130분 동안 상기 비소가 주입된 코발트 실리사이드 영역을 지탱하는 단계는 0.15㎛와 동일한 깊이(코발트 실리사이드의 상부 표면에 대하여)를 가진 소스나 드레인을 산출한다는 것이 알려졌다. 유사하게, $1 \times 10^{17} cm^{-3}$의 도핑 레벨을 가진 n형 실리콘 기판을 가열하는 단계와 124분 동안 800℃의 온도로 상기 붕소가 주입된 티타늄 실리사이드 영역을 지탱하는 단계는 0.2㎛와 동일한 깊이(티타늄 실리사이드의 상부 표면에 대하여)를 가진 소스나 드레인을 산출한다는 것도 알려져 있다.

본 발명의 보다 완전한 이해를 위한 교육학적 도움으로서 n채널 MOS IC 및 CMOS(상보 금속 산화물 반도체) IC의 제조를 위한 본 발명의 소자 제조 방법의 용융이 이하에서 기술되게 된다(간략하게 하기 위해 완전히 통상적인 몇몇 단계는 생략된다).

제1도 내지 제8도를 참조하면, 예를 들어 종래의 산화 기술을 이용하여, P형 실리콘 기판(10)상에 FOX(20)(비교적 두꺼운 SiO_2층)을 형성함으로써 본 발명의 한 실시예에 따라 n채널 MOS IC가 제조된다. 기판(10)에서 P형 도펀트의 도핑 레벨은 예를 들어 $1 \times 10^{15} cm^{-3}$이다. 또한 FOX(20)의 두께는 예를 들어 0.35㎛이다.

이제 FOX(20)는 MOSFET가 형성될, 여기서는 GASAD(gate-and-source-and-drain)으로 불리는 기판 표면의 영역(30)을 노출시키기 위해 예를 들어, 석판 인쇄술 및 반응 이온 에칭(RIE)기술을 이용하여 선택적으로 에칭된다. 예를 들어, 0.15㎛의 두께를 가진 GOX(40)(비교적 얇은 SiO_2층)는 예를 들어 종래의 산화 기술을 이용하여 GASAD 영역(30)의 표면상에 형성된다.

MOSFET의 게이트 전극은 GASAD 영역(30) 뿐만 아니라 FOX(20)상에도 다결정 실리콘(이후 폴리실리콘)의 층(50)을 초기에 침착시킴으로써 형성된다. 침착은 예를 들어 종래의 저압 화학적 증기 침착(LPCVD) 기술을 이용하여 실행되며, 침착된 폴리실리콘의 두께는 예를 들어 0.3㎛가 된다.

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침착후에, 폴리실리콘은 예를 들어 $1\times10^{15}cm^{-2}$의 주입량(implant dose)과 80kev의 이온 에너지를 이용하여, 폴리실리콘에 비소와 같은 n형 도펀트를 주입함으로써 전기적 전도성으로 만들어진다.

침착된 전기적 전도성의 폴리실리콘(50)은 이제 제4도에 도시된 바와 같이, 간각이 GASAD 영역(30) 위에 있는 폴리실리콘 구조를 형성하기 위해 종래의 RIE 기술을 이용하여 패턴된다. 상기 구조의 측벽은 대응하는 GASAD 영역이 표면에 직각인 면에 비하여 각도 α(제4도 참조)를 형성하는데, 이것은 +15° 보다 작거나 같으며, 0도가 되는것이 바람직하다(제4도에 도시한 폴리실리콘 구조의 좌측벽에 대해, 각도 X는 수직으로 부터 시계 방향으로 측정될때 포지티브가 된다. 한편 우측벽에 대해서는 이 각도가 반시계 방향으로 측정될때 포지티브다 된다). 측벽 각도에 관한 관계는 이하에서 논의되는 바와 같이 실리콘 이산화물 측벽 스페이서(55)의 형성과 관련하여 매우 중요하다.

이하에서 논의되는 소자 제조 절차는 결과적으로 금속 실리사이드 영역을 각각의 MOSFET의 소스, 드레인 및 게이트 전극으로 병합시킨다. 게이트 전극에서의 금속실리사이드 영역과 소스 및 드레인에서의 금속 실리사이드 영역 사이의 전기적 접촉을 배제하기 위해, 각 게이트 전극의 폴리실리콘 부분은 각 폴리실리콘 측벽을 커버링하는 실리콘 이산화물 측벽 스페이서(55)(제4도 참조)를 포함하도록 형성된다. 이것은 예를 들어 FOX의 상부 및 측벽 표면과 GASAD 영역의 노출된 표면상에 뿐만 아니라 폴리실리콘 구조의 상부 및 측벽 표면상에 테트라에틸오소실리케이트(TEOS)와 같은 실리콘과 산소 함유 물질의 층을 침착 시킴으로써 실현된다. TEOS의 침착은 예를 들어 종래의 LPCVD 기술을 이용하여 쉽게 실행되며, TEOS의 두께는 예를 들어 0.1㎛이다. 침착이 이루어진 후에, TEOS는 TEOS를 농후하게 하고 효과적으로 실리콘 이산화물과 같은 물질로 변환시키기 위해 스팀 대기에서 20분 동안 900℃로 가열되는 것이 바람직하다. 이때 TEOS는 폴리실리콘 구조의 상부 표면 뿐만 아니라 FOX 및 GASAD 표면으로 부터 TEOS를 제거하기 위해 예를 들어 CHF_3 및 O_2의 에천트(etchant) 환경에서 예를 들어 RIE를 이용하여 이등방향으로 에칭된다. 이 에칭 절차 이후에, 예를 들어 0.06㎛의 두께를 가진 농후하게 된 TEOS의 층이 측벽 각도가 전술한 요구를 만족하도록 제공되어 폴리실리콘 구조의 측벽상에 남아 있게 된다.

측벽 스페이서(55)의 형성 이후에, 티타늄과 같은 금속 실리사이드를 형성하기 위해 실리콘과 반응할 수 있는 금속층이 각 폴리실리콘 구조의 상부 표면과, 측벽 스페이서(55)의 표면과, GASAD 영역의 노출된 표면(소스와 드레인 형성될 곳) 및 FOX(20)의 상부 및 측벽 표면상에 침착된다. 이 침착은 예를 들어, 종래의 스퍼터링 기술을 이용하여 실현되며, 침착된 티타늄의 두께는 예를 들어, 0.1㎛이다. 침착 이후에, 티타늄으로 커버된 실리콘 기판은 종래의 RTA 기술을 이용하여 약 1분동안 약 600℃의 온도로 질소(N_2) 환경에서 가열된다. 티타늄 층이 실리콘과 접촉하는 곳, 즉 GASAD 영역의 표면 뿐만 아니라 폴리실리콘 구조의 상부 표면상에서, 이 가열 절차는 TiN, Ti 및 Tisiy의 연속한 층의 형성을 초래하게 되는데, 여기서 y≤2이다. 대조적으로, 침착된 티타늄 층이 실리콘 이산화물과 접촉하는 곳, 즉 FOX 및 측벽 스페이서의 표면에서, 상기 가열절차는 TiN 및 Ti의 연속한 층의 형성을 야기하게 된다.

TiSiy(y≤2)가 아닌 TiN 및 Ti층은 90℃의 온도로 가열된 H_2SO_4 : H_2O_2(1 : 1)의 용액과 같은 선택적 습식 에천트를 사용하여 에칭된다. 폴리실리콘 구조의 상부 표면과 GASAD 영역의 노출된 표면을 커버링하는 남아있는 TiSiy(y≤2)는 이제 종래의 RTA 기술을 이용하여 예를 들어 20초동안 800℃의 온도로 질소 환경에서 TiSiy로 커버된 실리콘 기판을 가열함으로써(폴리실리콘 구조 및 실리콘 기판에서) 아래에 있는 실리콘과 반응하게 된다. 그 결과 $TiSi_2$ 함유 영역(60, 70)(제5도 참조)이 폴리실리콘 주조의 반대측에 형성되어 수직으로 정렬되고 $TiSi_2$ 함유 영역(80)은 폴리실리콘 구조의 정상부에 형성되는데, 이와 같은 영역은 약 0.08㎛의 동일한 $TiSi_2$의 두께를 갖는다(각각의 이와 같은 영역은 또한 통상적으로 약 0.01㎛의 두께를 갖고 $TiSi_2$ 위에 있는 TiN층(양호한 전기적 전도체)을 포함한다).

n^+형 소스 및 드레인을 형성하기 위해, 하나 혹은 그 이상의 도펀트, 즉 비소 이온이나 인 이온이 $TiSi_2$ 함유 영역(60, 70)내로 주입된다. 주입량은 물론 전술한 세가지 조건을 만족하도록 선택된다. 또한 이온 에너지도 거의 모든 이온이 영역(60, 70)내로 주입되고 아래에 놓인 실리콘내로는 주입되지 않도록 선택된다.

이온 주입 이후에, 인터레벨 유전체(90)(제6도 참조)가 기판상에 침착된다. 이와 같은 유용한 인터레벨 유전체는 예를 들어, 0.2㎛의 두께를 가진 도핑되지 않은 TEOS와 약 0.8㎛의 두께를 가진 인으로 도핑된 TEOS의 잇따른 층을 포함한다.

침착된 인터레벨 유전체(9)의 상부 표면은 통상적으로 비평면이다(일반적으로 후속 처리동안 바람직하지 못하다). 인터레벨 유전체(90)를 흐르도록 유도하고 그래서 표면 평면성을 실현하고 또한 티타늄 실리사이드로 커버된 소스 및 드레인(100, 110)(제7도 참조)을 형성하도록 $TiSi_2$ 함유 영역(60, 70)으로 부터 아래에 놓인 실리콘내로 주입 도펀트를 확산시키기 위해, 기판이 가열된다. 전술한 바와 같이, 가열 절차의 온도-시간 프로필은 약 0.2㎛ 이하의 깊이를 가진 소스 및 드레인을 산출하도록 선택된다.

소스 및 드레인 형성 이후에, 인터레벨 유전체는 소스와 드레인 및 게이트 전극으로 경유 구멍을 개방하도록(종래 기술을 이용하여) 패턴된다. 이제 물질층(120, 130, 140)(제8도 참조)이 기판상에 침착되는데 그래서, 알루미늄과 실리콘의(바람직하지 못한) 상호 확산에 대한 장벽으로서 작동하도록 소스와 드레인 및 게이트 전극으로 각각 뻗은 경유 구멍내로 침착되게 된다. 이들 층은 예를 들어, 10퍼센트(중량으로)의 티타늄과 90퍼센트의 텅스텐 합성물을 포함하며 예를 들어 0.1㎛의 두께를 갖는다.

이제, 예를 들어 1㎛의 두께를 가진 알루미늄 층이 경유 구멍내의 장벽층(120, 130, 140) 뿐만 아니라 인터레벨 유전체(90)상에도 침착된다. 침착후 계속해서, 금속 접촉 패드에서 중단되는 상호 접속

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알루미늄 런너(runner)(150, 160, 170)를 형성하기 위해 종래의 기술을 이용하여 알루미늄층이 패턴된다.

n채널 MOS IC는 통상적인 일련의 단계를 통해 완성되는데, 통상적으로 습기 및 기계적 손상에 대비한 장벽을 형성하기 위해 IC상에 실리콘 질화물 층을 침착하는 단계를 포함한다.

이제 제9도 내지 제17도를 참조하면, 종래기술을 이용하여 P+형 실리콘 기판(200)상에 P형 실리콘층(210)(제9도 참조)을 에피택셜 성장시킴으로써 본 발명의 제2실시예에 따라 CMOS IC가 제조된다. 기판(200)의 도핑 레벨은 예를 들어 $10^{18}cm^{-3}$ 이며, 에피택셜 성장된 층(210)의 도핑 레벨은 예를 들어 $10^{15}cm^{-2}$이다. 또한, 에피택셜 성장된 층(210)의 두께는 예를 들어 5㎛이다.

1984년 3월 13일 엘.씨.파릴로와 알.에스.페인에게 특허된 미합중국 제 4,435,896호에 기술된 바와 같은 소위 2중 튜브 공정을 이용하여 에피택셜 성장층(210)에 인접한 n튜브 및 P튜브(240, 250)가 형성된다. 즉 예를 들어 0.1㎛의 두께를 가진 실리콘 질화물층(220)(제10도 참조)이 통상적인 침착 기술을 이용하여 상기 층(210)의 상부 표면에 처음에 침착된다. 종래의 석판 인쇄술 및 RIE 기술이 실리콘 질화물층(220)의 일부분을 제거하고, 그러므로 n튜브(240)가 될 실리콘 표면을 노출시키는데 이용된다. 이제 도우너 이온, 즉 인 이온과 비소 이온이 상기 층(210)(층(210)의 노출되지 않는 실리콘을 주입으로 부터 차폐하도록 작용하는 잔여 실리콘 질화물층)의 노출된 실리콘 표면내로 주입되는데, 인과 비소 이온 모두에 대한 주입량 및 에너지는 예를 들어 각각 $2\times10^{12}cm^{-2}$와 100keV이다. 다음에, n튜브의 표면상에 약 0.4㎛의 두께를 가진 실리콘 이산화물의 층(230)(제10도 참조)을 형성하기 위해, 예를 들어 950℃의 온도로 140분의 대응하는 가열 시간동안 스팀 함유 환경에서 실리콘 기판이 가열된다.

이제 실리콘 질화물의 층(220)이 뜨거운 H_3Po_4와 같은 습식 에천트로 에칭되고, 액셉터 이온 즉 붕소 이온이 P튜브(250)가 될 노출된 실리콘 표면으로 주입된다(실리콘 이산화물층(230)은 n튜브(240)을 주입으로 부터 차폐한다). 만일 붕소 이온이 사용되면, 주입량 및 대응하는 주입 에너지는 예를 들어 각각 $2\times10^{12}cm^{-2}$ 및 50keV이다. 다음에, 실리콘 기판은 붕소 이온 및 인 이온을 약 2㎛의 깊이까지 상기 층(210)내로 확산시켜 n튜브(240) 및 p튜브(250)(제11도 참조) 모두를 형성시키기 위해, 예를 들어 1150℃의 온도로 120분의 대응하는 시간 주기동안 질소(N_2) 환경에서 가열된다.

n튜브(240)를 커버링하는 실리콘 이산화물층(230)은 H_2O : HF(7 : 1)와 같은 습식 에천트로 에칭된다. 이제 CMOS IC에서 FOX로서 작용하는 예를 들어 0.4㎛의 두께를 가진 실리콘 이산화물의 비교적 두꺼운 층(260)(제12도 참조)이 에피택셜 성장층(210)의 (이제 완전히 노출된) 상부 표면상에 형성된다. 이것을 예를 들어 850℃의 온도로 25분의 대응하는 가열 시간동은 고압스팀 함유 대기, 즉 25기압의 압력을 나타내는 스팀 함유 대기에서 실리콘 기판을 가열함으로써 실현된다.

실리콘 이산화물의 비교적 두꺼운 층(260)은, n채널 MOSFET가 형성된 P튜브(250)과 표면상의 GASAD 영역(270)을 노출시키고, P채널 MOSFET가 형성될 n튜브(240)의 표면상의 GASAD 영역(400)을 노출시키기 위해 종래의 기술을 이용하여 패턴된다. 다음에, 실리콘 기판은 GASAD 영역(270)의 표면상에 실리콘 이산화물의 층(280)을 형성하고 GASAD 영역(400)의 표면상에 실리콘 이산화물의 층(410)을 형성하기 위해 900℃의 온도로 27분의 대응하는 시간 주기동안 가열되게 되는데, 이들 층(280, 410)은 약 0.0125㎛의 두께를 가지며, n채널 및 P채널 MOSFET의 GOX로서 작용한다.

n채널 및 P채널 MOSFET의 게이트 전극은 처음에, FOX(260) 뿐만 아니라 GASAD 영역(270, 400)상에 예를 들어 0.3㎛의 두께를 가진 폴리실리콘 층을 침착시킴으로써 형성되며, 포토레지스트가 기판상에 침착되어 n튜브(240)에 대응하는 기판 표면을 노출시키기 위해 패턴된다. 이제 액셉터 이온, 즉 붕소 이온이 n튜브 위에 놓인 폴리실리콘내로 주입되는데 레지스트는 P튜브 위에 놓인 폴리실리콘을 주입으로 부터 차폐한다. 주입량 및 주입 에너지는 예를 들어, 각각 $1\times10^{15}cm^{-2}$와 30keV이다. 이 레지스트는 벗겨지고, 제2레지스트가 기판상에 침착되어 P튜브(250)에 대응하는 기판 표면을 노출시키기 위해 패턴된다. 이제 도우너 이온, 즉 비소 이온이 P튜브(250)위에 놓인 폴리실리콘내로 주입되는데, 제2레지스트는 n튜브(240) 위에 놓인 폴리실리콘을 제2주입으로 부터 차폐한다. 도우너 이온에 대응하는 주입량 및 주입 에너지는 예를 들어, 각각 $1\times10^{15}cm^{-2}$와 30keV이다. 이제 제2레지스트는 벗겨지고, 기판은, 예를 들어 900℃의 온도로 30분의 대응하는 시간 주기동안 질소(N_2) 디기에서 가열된다. 결과적으로, 주입된 도펀트가 폴리실리콘내로 확산되어, n튜브(240)위에 놓인 폴리실리콘은 P형 전도성이 되고, P튜브(250)위에 놓인 폴리실리콘은 n형 전도성이 된다.

이제, 침착되고 주입된 폴리실리콘(도한 아래에 놓인 비교적 얇은 실리콘 이산화물층(280, 410)로 마찬가지)이 각각 GASAD 영역(270, 400)위에 놓인 폴리실리콘 구조(290, 420)(제13도 참조)를 형성하기 위해 전술한 바와 같이 패턴된다. 이 폴리실리콘 구조의 측벽은 위에서 논의된 요구에 부합해야 한다. 또한 전술한 바와 같이 실리콘 이산화물 측벽 스페이서(295, 425)가 각각 폴리실리콘 구조(290, 420)상에 형성된다.

이제 코발트와 같이 금속 실리사이드를 형성 하기 위해 실리콘과 반응할 수 있는 금속층이 폴리실리콘구조(290, 410)의 상부 표면과, 측벽 스페이서(295, 425)의 표면과, GASAD 영역의 노출된 표면(소스와 드레인의 형성될 곳)과, FOX(260)의 상부 및 측벽 표면상에 침착된다. 침착된 코발트의 두께는 예를 들어 0.02㎛이다. 침착 이후에, 코발드로 커버된 기판은 450℃의 온도로 90분의 대응하는 시간 주기동안, 감소대기, 즉 대기에서 가열된다. 코발트가 실리콘과 접촉하는 곳, 즉 GASAD 영역과 노출된 표면뿐만 아니라 폴리실리콘 구조의 상부 표면상에서, 이 가열 절차는 코발트 모노실리사이드(CoSi)를 형성하게 된다. 모든 다른 영역에 있어서, 코발트는 반응하지 않은채로 남아 있다. 반응하지 않은 코발트(CoSi가 아님)는 이제 H_3Po_4 : CH_2COOH : HNO_3 : H_2O(16 : 2 : 1 : 1)과 같은 선택적 습식 에천트를 사용하여 벗겨진다. 다음에, 기판은 예를 들어 700℃의 온도로 30분의 대응하는 시간 주기동안 불활성 대기, 즉 아르곤(Ar) 대기에서 두번째 가열된다. 이 제2가열은 약 0.07㎛의 두께를

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가진 코발트 다이실리사이드($CoSi_2$)를 형성하기 위해 CoSi를 아래에 놓인 실리콘과 반응하도록 한다. 그러므로, $CoSi_2$ 함유 영역(300, 310)(제14도 참조)이 각각의 폴리실리콘구조(290)와 수직으로 정렬하여 반대측에 형성되고, 함유 영역(320)이 각각의 폴리실리콘구조(290)의 정상부에 형성된다. 유사하게, $CoSi_2$ 함유 영역(430, 440)이 각각의 폴리실리콘 구조(420)와 수직으로 정렬하여 반대측에 형성되고, $CoSi_2$ 함유 영역(450)이 각각의 폴리실리콘 구조(420)의 정상부에 형성된다.

n튜브(240)에서 P채널 MOSFET에 대한 P^+형 소스 및 드레인을 형성하기 위해, 예를 들어 1㎛의 두께를 가진 포토레지스트가 기판상에 침착되어, n튜브의 표면을 노출시키도록 패턴된다. 이제 액셉터 이온이 $CoSi_2$ 함유 영역(430, 440)내로 주입된다(이 레지스트는 P튜브(250)를 주입으로 부터 차폐한다). 전술한 바와 같이, 주입량은 3가지 조건을 만족하도록 선택되며, 이온 에너지는 거의 모든 이온이 상기 영역(430, 440)내로 주입되도록 선택된다. 이점에 있어서, 액셉터 이온은 예를 들어 붕소 이온이며, 유용한 주입량은 $8\times10^{15}cm^{-2}$이고 유용한 대응하는 주입 에너지는 10keV인 것으로 결정되었다.

침착되어 패턴된 포토레지스트는 벗겨지고, 약 1㎛의 두께를 가진 다른 포토레지스트가 기판상에 침착되고, 이번에는 P튜브(250)의 표면을 노출시키기 위해 패턴된다. 이제, 도우너 이온이 $CoSi_2$ 함유 영역(300, 310)내로 주입된다(세로 침착된 레지스트는 n튜브(240)를 제2주입으로 부터 차폐한다). 다시, 주입량 및 이온 에너지는 상기 조건과 요구를 만족하도록 선택된다. 이점에 있어서, 만일 도우너 이온이 예를 들어 비소 이온이면, 유용한 주이량은 $5\times10^{15}cm^{-2}$이고 유용한 대응하는 이온 에너지는 60keV 보다 작거나 같다. 한편, 만일 도우너 이온이 인 이온이면, 유용한 주입량은 $5\times10^{25}cm^{-2}$이고, 유용한, 대응하는 주입 에너지는 30keV 이하의 에너지이다.

이온 주입 이후에, 예를 들어, 0.2㎛ 두께의 도핑 되지 않은 TEOS층과 0.2㎛두께의 인 도핑된 TEOS층의 연속한 층을 포함하는 인터레벨 유전체(600)(제15도 참조)가 기판상에 침착된다. 인터레벨 유전체(600)는 흐르도록 유도되고, 주입된 도펀트는 $CoSi_2$로 커버된 n^+형 소스 및 드레인(330, 340)(제16도 참조)과, $CoSi_2$로 커버된 P^+형 소스 및 드레인(460, 470)을 기판 가열에 의해 형성하기 위해 $CoSi_2$ 함유 영역으로 부터 아래에 놓인 실리콘으로 확산된다. 이점에 있어서, 약 0.2㎛보다 작거나 같은 깊이를 가진 소스 및 드레인을 실현하기 위해, 유용한 가열 절차가 800℃의 온도로 120분동안 기판을 가열하는 것이라는 것이 결정되었다.

COMOS IC의 제조와 관련하여, 금속 실리사이드 영역으로 부터 기판내로 주입된 도펀트를 확산하는데 사용되는 가열 온도를 선택할때 만족되어야 할 추가의 요구 조건이 있다는 것을 주목하자. 즉 예를 들어 종래의 용광로 가열을 이용할때, 약 900℃를 초과하는 온도에서, n형 폴리실리콘 구조(420)내의 n형 도펀트가 P형 폴리실리콘구조(290)(통상적으로 n형 폴리실리콘 주조(420)와 접속 되어 있음)로 확산되어 그것을 카운터 도핑하려는 경향이 있는 것으로 알려져 있다. 이와 같은 카운터 도핑은 그것이 P채널 MOSFET에서 바람직하지 못한 임계 전압 시프트를 유도하기 때문에 바람직하지 못하다. 결과적으로, 본 발명의 실시예 2에 따라, CMOS IC를 제조하기 위해 용광로 가열을 이용할때 사용된 가열 온도는 900℃보다 낮으며, 850℃ 이하의 것이 바람직하다.

소스와 드레인을 형성한 후에, 인터레벨 유전체(600)가 소스와 드레인 및 게이트 전극으로 경유 구멍을 개방하기 위해 패턴된다. 알루미늄과 실리콘, 즉 층(350, 360과 370(제17도 참조), 480, 490과 500)의 상호 확산에 대한 장벽이 경유 구멍으로 침착된다. 소스와 드레인 및 게이트 전극으로 부터 금속 접촉 패드로 연장된 상호 접속 알루미늄 런너(375, 385, 395와 505, 515, 525)(제17도 참조)가 전술한 바와 같이 형성된다.

CMOS IC는 습기 및 기계적 손상에 대비한 장벽을 형성하기 위해 IC상에 실리콘 질화물층을 침착시키는 단계를 포함하는 통상적인 일련의 단계를 통해 완성된다.

(57) 청구의 범위

청구항 1

기초적인 반도체 물질을 포함하는 기판상(10)에 금속 함유 물질 영역(60)을 형성하는 단계와, 상기 금속 함유 물질 영역내에 도펀트를 주입시키는데, 상기 도펀트는 상기 기초적인 반도체 물질이 P-형 전도성으로 되어 있으면 상기 기초적인 반도체 물질내에서 도우너가 되나 상기 기초적인 반도체 물질이 n-형 전도성으로 되어 있으면 액셉터가 되는 최소한 하나의 도펀트를 상기 금속 함유 물질 영역내에 주입시키는 단계와, 상기 금속 함유 물질 영역에서 상기 기판내로 상기 도펀트를 확산시키도록 상기 기판을 가열하며, 그로써 상기 기판내에 도펀트 함유 영역(100)을 형성하는 단계와, 반도체 소자 제조를 완료시키는 단계를 포함하는 반도체 소자 제조 방법에 있어서, 상기 금속 함유 물질 영역은 0.2㎛ 이하의 평균 두께 t를 가지며, 상기 가열 온도 및 시간은 상기 도펀트 함유 영역의 깊이가 상기 금속 함유 물질 영역의 정상부로부터 측정할때 약 0.2㎛ 이하가 되도록 선정되며, 상기 금속 함유 물질 영역 I내로 주입된 단위면적당 도펀트의 양은 t에 대한 I의 비율이 상기 가열동안에 사용된 온도에서 상기 금속 함유 물질 영역내의 상기 도펀트의 고체 용해도의 약 1/2 이상이 되도록 선정되는 것을 특징으로 하는 반도체 소자 제조 방법.

청구항 2

제1항에 있어서, 상기 금속 함유 혼합물은 금속 실리사이드인 것을 특징으로 하는 반도체 소자 제조 방법.

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청구항 3

제2항에 있어서, 상기 금속 실리사이드는 코발트 실리사이드인 것을 특징으로 하는 반도체 소자 제조 방법.

청구항 4

제1항에 있어서, 상기 반도체 물질은 실리콘을 포함하는 것을 특징으로 하는 반도체 소자 제조 방법.

청구항 5

표면, 반도체 물질 및 상기 표면으로 부터 기판내로 연장되고 상기 표면보다 작은 측면 넓이를 가지며, 주위 반도체 물질의 전도성과 반대인 전도성을 가진 기판 영역을 포함하는 기판(10)과, 상기 표면과 접촉하고 상기 기판 영역 위에 놓인 금속 함유 물질 영역(60)을 구비하는 반도체 소자에 있어서, 상기 기판 영역의 깊이는 상기 금속 함유 물질 영역의 정상부로 부터 측정할때 약 0.2㎛ 이하이고, 상기 기판에 대한 상기 금속 함유 물질 영역의 특정 접촉 저항은 약 $10^{-6}\Omega \cdot cm^2$ 이하인 것을 특징으로 하는 반도체 소자.

청구항 6

제5항에 있어서, 상기 반도체 소자는 MOSFET를 포함하고, 상기 금속 함유 물질 영역과 상기 기판 영역은 상기 MOSFET의 소스나 드레인을 형성하는 것을 특징으로 하는 반도체 소자.

청구항 7

제5항에 있어서, 상기 반도체 소자는 MESFET를 포함하고, 상기 금속 함유 물질 영역과 상기 기판 영역은 상기 MESFET의 소스나 드레인을 형성하는 것을 특징으로 하는 반도체 소자.

청구항 8

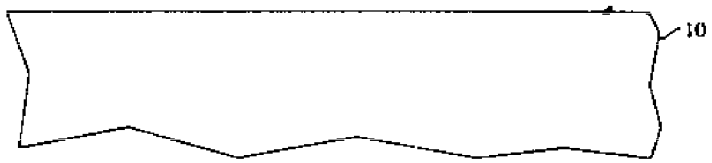
제5항에 있어서, 상기 금속 함유 혼합물은 금속 실리사이드인 것을 특징으로 하는 반도체 소자.

청구항 9

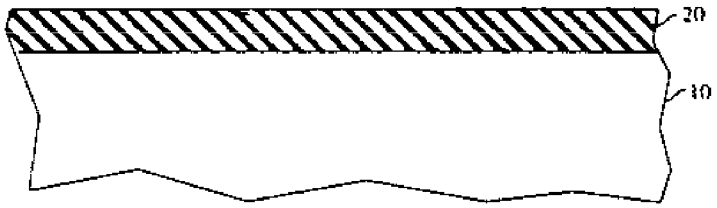
제8항에 있어서, 상기 금속 실리사이드는 코발트 실리사이드인 것을 특징으로 하는 반도체 소자.

도면

도면1

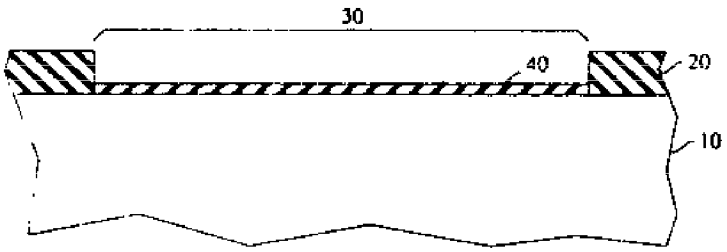


도면2

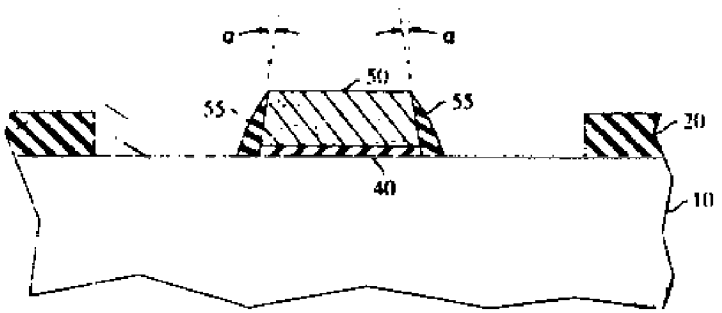


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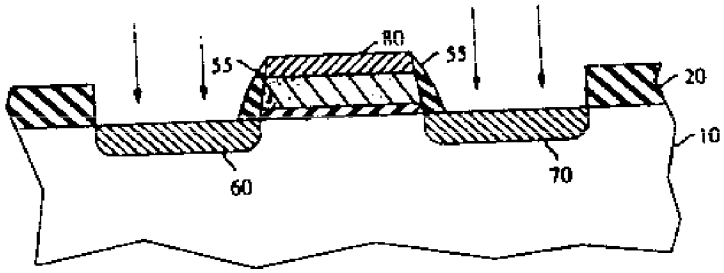
도면3



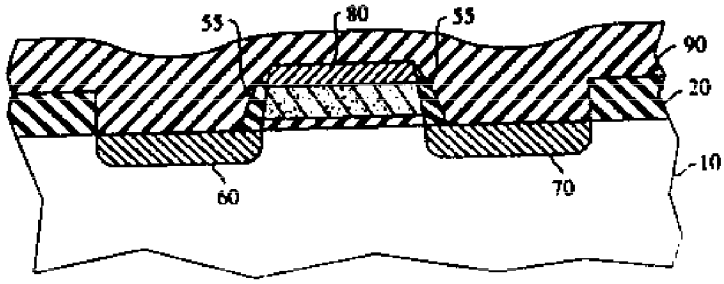
도면4



도면5

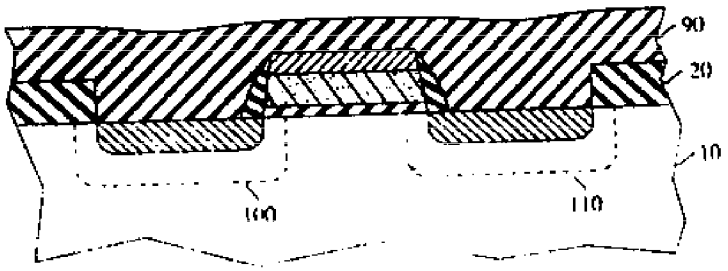


도면6

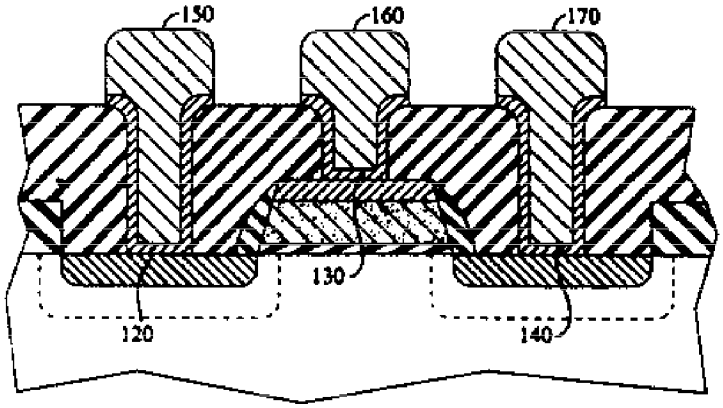


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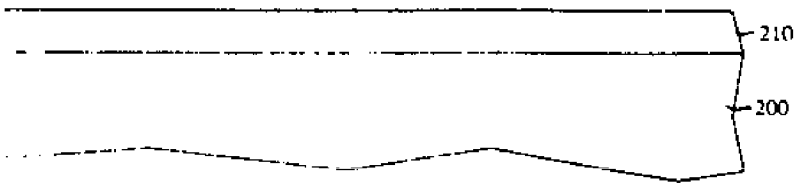
도면7



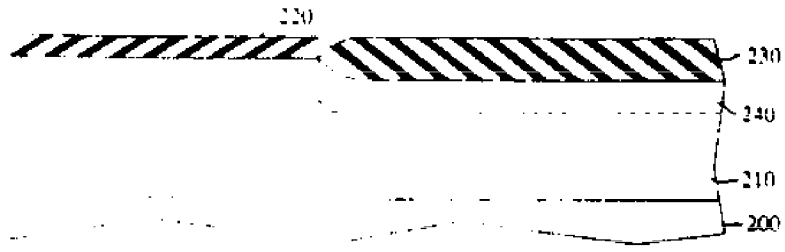
도면8



도면9

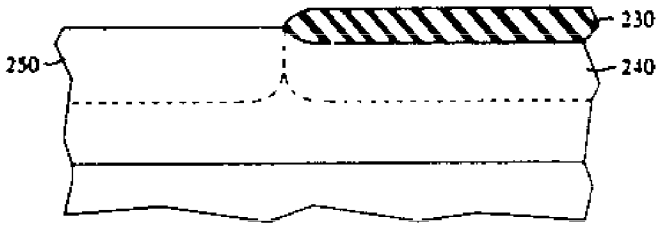


도면10

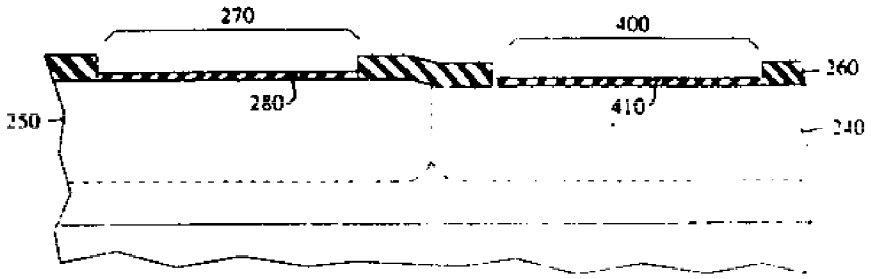


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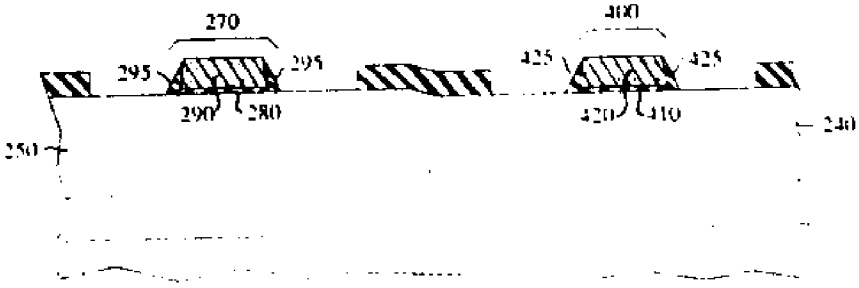
도면11



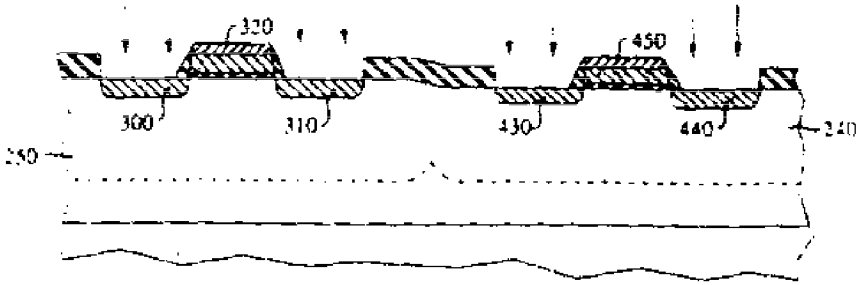
도면12



도면13

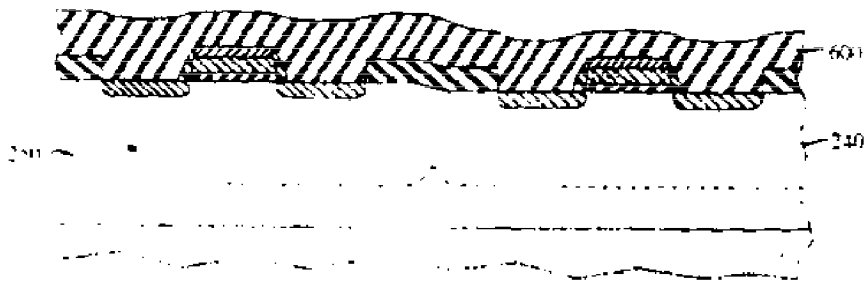


도면14

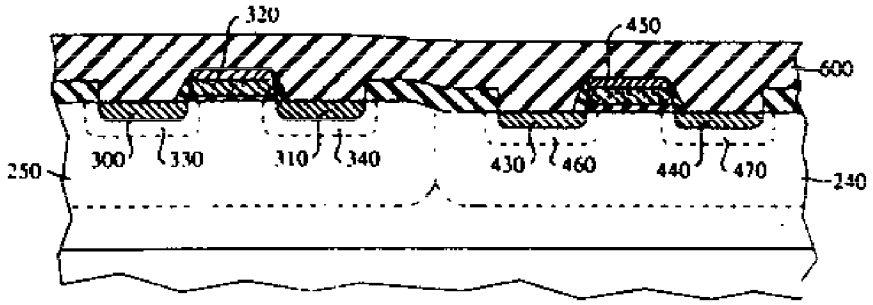


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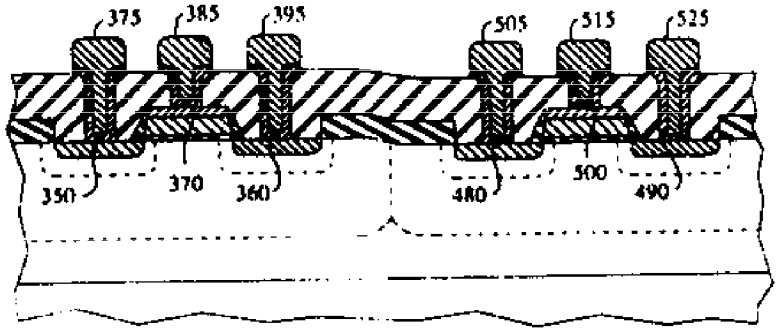
도면15



도면16



도면17



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Bibliographic Data

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Agent.	LEE, Byong Ho | CHOI, Dall Ryong
Inventor	RuUChenRiU | WilRiAmToMaSeuRinCheu | DeIBiDeuSeulReITeuWilRiAmSeu
Applicant	AT&T Corp.
Rightholder	AMeRiKanTelRiPonAenDeuTelReGeuRaPeuKamPaNi

발명의 명칭

반도체소자및그제조방법

Title of Invention

MANUFACTURING METHOD AND THERE DEVICES OF SEMICONDUCTOR ELEMENTS

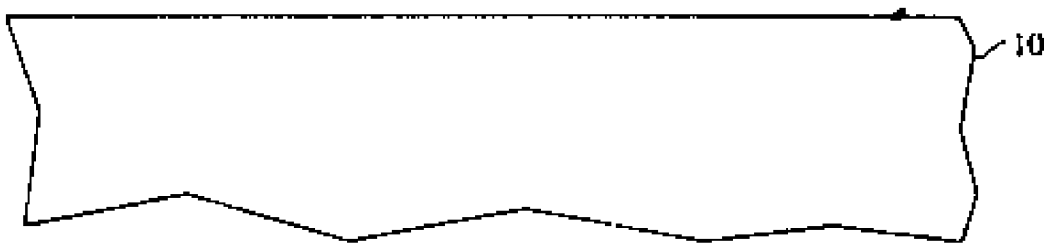
요약

내용 없음.

Abstract

Content none.

대표도면(Representative drawing)



청구의 범위

Scope of Claims

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청구 1항:

기초적인 반도체 물질을 포함하는 기판상(10)에 금속 함유 물질 영역(60)을 형성하는 단계와, 상기 금속 함유 물질 영역내에 도펀트를 주입시키는데, 상기 도펀트는 상기 기초적인 반도체 물질이 P-형 전도성으로 되어 있으면 상기 기초적인 반도체 물질내에서 도우너가 되나 상기 기초적인 반도체 물질이 n-형 전도성으로 되어 있으면 액셉터가 되는 최소한 하나의 도펀트를 상기 금속 함유 물질 영역내에 주입시키는 단계와, 상기 금속 함유 물질 영역에서 상기 기판내로 상기 도펀트를 확산시키도록 상기 기판을 가열하며, 그로써 상기 기판내에 도펀트 함유 영역(100)을 형성하는 단계와, 반도체 소자 제조를 완료시키는 단계를 포함하는 반도체 소자 제조 방법에 있어서, 상기 금속 함유 물질 영역은 0.2㎛ 이하의 평균 두께 t를 가지며, 상기 가열 온도 및 시간은 상기 도펀트 함유 영역의 깊이가 상기 금속 함유 물질 영역의 정상부로부터 측정할때 약 0.2㎛ 이하가 되도록 선정되며, 상기 금속 함유 물질 영역 I내로 주입된 단위 면적당 도펀트의 양은 t에 대한 I의 비율이 상기 가열동안에 사용된 온도에서 상기 금속 함유 물질 영역내의 상기 도펀트의 고체 용해도의 약 1/2 이상이 되도록 선정되는 것을 특징으로 하는 반도체 소자 제조 방법.

Claim 1:

The dopant is injected within the step of forming the metal containing material domain (60) on the substrate phase (10) including the fundamental semiconductor material, and the metal containing material domain ; the substrate is heated up in order to diffuse the dopant in the step of injecting the dopant of at least one in which the acceptor is within the metal containing material domain if the donor is in the above-mentioned fundamental semiconductor material if in the dopant, the above-mentioned fundamental semiconductor material is to the P- type conductivity but the above-mentioned fundamental semiconductor material is to the n-type conductivity, and the metal containing material domain within the substrate ; the metal containing material domain has the average thickness t less than 0.2㎛ as to the semiconductor device fabricating method including the step of forming the dopant containing domain (100) as that within the substrate, and the step of completing the semiconductor device fabrication ; and it is chosen so that in the heating temperature and time, about 0.2㎛ this are when the depth of the dopant containing domain measures from the top of the metal containing material domain. The semiconductor device fabricating method in which amount of the dopant per the unit area injected within the metal containing material domain I is chosen in the temperature in which the rate of I about the t is used for for heating in order to become over about 1/2 of the solid solubility of the dopant within the metal containing material domain.

청구 2항:

제1항에 있어서, 상기 금속 함유 혼합물은 금속 실리사이드인 것을 특징으로 하는 반도체 소자 제조 방법.

Claim 2:

As for claim 1, the semiconductor device fabricating method in which the metal containing mixture is the metal silicide.

청구 3항:

제2항에 있어서, 상기 금속 실리사이드는 코발트 실리사이드인 것을 특징으로 하는 반도체 소자 제조 방법.

Claim 3:

As for claim 2, the semiconductor device fabricating method in which the metal silicide is the cobalt silicide.

청구 4항:

제1항에 있어서, 상기 반도체 물질은 실리콘을 포함하는 것을 특징으로 하는 반도체 소자 제조 방법.

Claim 4:

The semiconductor device fabricating method of claim 1, wherein the above semiconductor material comprises the silicone.

청구 5항:

표면, 반도체 물질 및 상기 표면으로 부터 기판내로 연장되고 상기 표면보다 작은 측면 넓이를 가지며, 주위 반도체 물질의 전도성과 반대인 전도성을 가진 기판 영역을 포함하는 기판(10)과, 상기 표면과 접촉하고 상기 기판 영역 위에 놓인 금속 함유 물질 영역(60)을 구비하는 반도체 소자에 있어서, 상기 기판 영역의 깊이는 상기 금속 함유 물질 영역의 정상부로 부터 측정할때 약 0.2㎛ 이하이고, 상기 기판에 대한 상기 금속 함유 물질 영역의 특정 접촉 저항은 약 10-6Ω#183#cm2 이하인 것을 특징으로 하는 반도체 소자.

Claim 5:

The semiconductor device in which it is about 0.2㎛ or less as to the semiconductor device equipped with the metal containing material domain (60) contacting with the substrate (10) and contacts with the surface and is puts on the substrate region when the depth of the substrate region measures from the top of the metal containing material domain ; and the specific constant resistance of the metal containing material domain about the substrate is about 10 - 6 Ω· cm 2 or less which comprise the surface, the semiconductor material, and the substrate region which is extended from the surface within the substrate and it has the side width smaller than the surface ; and has the conductivity which is conduc

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tivity and opposite of the surrounding semiconductor material.

청구 6항:

제5항에 있어서, 상기 반도체 소자는 MOSFET를 포함하고, 상기 금속 함유 물질 영역과 상기 기판 영역은 상기 MOSFET의 소스나 드레인을 형성하는 것을 특징으로 하는 반도체 소자.

Claim 6:

The semiconductor device of claim 5, wherein the semiconductor device comprises MOSFET, and the metal containing material domain and substrate region forms the source or the drain of MOSFET.

청구 7항:

제5항에 있어서, 상기 반도체 소자는 MESFET를 포함하고, 상기 금속 함유 물질 영역과 상기 기판 영역은 상기 MESFET의 소스나 드레인을 형성하는 것을 특징으로 하는 반도체 소자.

Claim 7:

The semiconductor device of claim 5, wherein the semiconductor device comprises MESFET, and the metal containing material domain and substrate region forms the source or the drain of MESFET.

청구 8항:

제5항에 있어서, 상기 금속 함유 혼합물은 금속 실리사이드인 것을 특징으로 하는 반도체 소자.

Claim 8:

As for claim 5, the semiconductor device in which the metal containing mixture is the metal silicide.

청구 9항:

제8항에 있어서, 상기 금속 실리사이드는 코발트 실리사이드인 것을 특징으로 하는 반도체 소자.

Claim 9:

As for claim 8, the semiconductor device in which the metal silicide is the cobalt silicide.

상세설명

Detailed Description

[발명의 명칭]

반도체 소자 및 그 제조 방법

[Title of invention]

Semiconductor device and method for manufacturing the same.

[도면의 간단한 설명]

제1도 내지 제8도는 본 발명의 반도체 소자 제조 방법의 실시예 1에 수반된 단계를 도시하는 도면.

제9도 내지 제17도는 본 발명의 반도체 소자 제조 방법의 실시예 2에 수반된 단계를 도시하는 도면.

[Brief description of drawings]

Drawing in which the first the inland eighth drawing shows the step accompanied with the embodiment 1 of the semiconductor device fabricating method of the invention.

Drawing in which the ninth the inland seventeenth drawing shows the step accompanied with the embodiment 2 of the semiconductor device fabricating method of the invention.

* 도면의 주요부분에 대한 부호의 설명

10 : P형 실리콘 기판 20 : FOX

30 : GASAD영역 50 : 다결정 실리콘층

100 : 소스 110 : 드레인

230 : 실리콘 이산화물층

* The description of reference numerals showing the main elements in drawings.

10: p-sub 20: FOX.

30: GASAD domain 50: polycrystalline silicon layer.

100: source 110: drain.

230: silicon dioxide layer.

[발명의 상세한 설명]

본 발명은 일반적으로 반도체 소자, 즉 반도체 집적 회로 IC)소

[Detailed description of the invention]

The invention generally relates to the method for

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자 뿐만 아니라 그 결과로된 소자를 제조하는 방법에 관한 것이다.

manufacturing the device which becomes with the semi conductor device, in other words, not only the semicon ductor IC(integrated circuit) IC) device but also the re sult furnace.

반도체 집적 회로(IC)는 반도체 기판에 형성된 다수의 전기적으로 상호 접속된 별개의 소자를 포함하는 소자와, 이들 IC중에는 MOS(metal-oxide semiconductor) 및 MES(metal-semiconductor) IC등에 포함한다. MOS IC는 통상적으로 다수의 MOSFET(CMOS 전계효과 트랜지스터)를 포함하는데 이 MOSFET 각각은 반도체 물질, 즉 실리콘의 활성 표면층을 포함한다. 각각의 MOSFET는 또는 활성층의 표면에 형성된 비교적 얇은 게이트 산화물(GOX)과, 예를들어, GOX의 표면상에 형성된 다결정 실리콘(폴리실리콘)의 게이트 전극 및, 상기 게이트 전극의 반대측에 MOSFET의 소스 및 드레인을 구성하는 활성층의 2개의 비교적 두껍게 도핑된 부분을 포함한다. 비교적 두꺼운(GOX와 비교하여) 필드 산화물(FOX)이 서로로 부터 MOSFET를 분리하고 전기적으로 절연하도록 작용한다. 유사하게, MES IC도 통상적으로 다수의 MESFET(MES전계효과 트랜지스터)를 포함하는데 MESFET는 MESFET의 게이트 전극이 금속이나 금속함유 혼합물, 즉 금속 실리사이드로 이루어지고 반도체 물질과 직접 접촉하고 있다는 접에서만 MOSFET와 다르다.

It includes the MOS (metal-oxide semiconductor) and MES (metal-semiconductor) IC etc. among the device, in which the semiconductor IC(integrated circuit) (IC) i ncludes lots of the separate device which is formed in t he semiconductor substrate and the electrically is inter connected and these ICs. The generally the MOS IC in cludes multiple MOSFETs (CMOS field effect transistor) but this MOSFET includes semiconductor material, and i n other words, the active surface layer of the silicone. Each MOSFET comprises the gate oxide (GOX) which or is formed on the surface of the active layer and is relat ively thin, the source of MOSFET in the opposite side o f the gate electrode of the poly-crystal silicon (poly-sili con) formed on for example, the surface of GOX and ga te electrode, and the part thickly doped in the relativel y of 2 of the active layer comprising the drain. It acts i n order to the relative thick (it compares with GOX) fiel d oxide (FOX) separate MOSFET and electrically insulat e. Similarly, MESFET the generally the MES IC includes multiple MESFETs (the MES field effect transistor) is co mposed of the gate electrode of MESFET is the metal o r the metal-containing mixture, in other words, the met al silicide. And in the semiconductor material and direct contact that it contacts, it is different from MOSFET.

현재 상업적으로 유용한 IC에 있어서, 게이트 전극의 길이, 즉 전류 채널의 길이는 통상적으로 약 2마이크로미터(㎛)이며, 소스 및 드레인의 두께는 약 0.5㎛이다. 그러나 증가된 패킹 밀도(별개 소자의)를 가진 IC를 실현하기 위해, 게이트 전극 길이(즉 전류 채널 길이)가 약 1㎛보다 작거나 같게 축소될 것으로 기대된다. 동시에, 통상 짧은 채널 영향으로 불리는 어떤 바람직하지 않은 영향을 피하기 위해, 소스 및 드레인의 두께가 약 0.2㎛보다 작거나 같은 값으로 축소될 것이다(여기서 언급된 바람직하지 않은 짧은 채널 영향은 바람직하지 않은 임계 전압 시프와 소스-드레인 부임계 결핍 전류인데, 이것은 소스/드레인 두께에 대한 채널 길이의 비율이 비교적 작을때 즉, 약 2.5 이하일때 발생한다. 짧은-채널 영향에 대해서는 제이.알.브로우스 등의 #8220#MOSFET 소형화에 대한 일반 안내#8221#란 논문을 참조하라).

Presently, as to the commercially useful IC, the length of the gate electrode, in other words, the length of the current channel, generally, the thickness of about 2 mi crometer (㎛), the source and drain are about 0.5㎛. Bu t in order that IC having the increased packing density (of the discrete device) is realized it is smaller than ab out 1㎛ or it is the same the gate electrode length (in o ther words, the current channel length) be reduced. Si multaneously, generally, it in order to avoid the influen ce noting any kind of be desirable paper called the shor t channel effect is the critical voltage thief and the so urce-drain subthreshold lack current in which the short channel effect noting the be desirable paper which the thickness of the drain and source will be reduced to th e value which is smaller than about 0.2㎛ or thes same is mentioned nots the be desirable paper. Relatively wh en the rate of the channel length about the source/dra in thickness is little, when being in other words, about 2.5 or less, this is generated. J about short - channel e ffect. The general guideline " about the "MOSFET minia turization including the egg Brouse. etc. refers to pape r.

비교적 얇은 소스 및 드레인, 즉 0.2㎛이하인 두께를 가진 소스 및 드레인은 바람직하지 못하게 큰 저항을 가지는데, 이것은 소자의 성능에 역으로 영향을 미친다. 비교적 얇은 소스 및 드레인을 사용하여 비교적 낮은 소스/드레인 저항을 실현하기 위해, 몰리브데늄 실리사이드(MoSi2), 텅스텐 실리사이드(WSi2)나 티타늄 실리사이드(TiSi2)와 같은 금속 실리사이드의 위에 놓인 영역을 포함하도록 각각의 비교적 얇은 소스 및 드레인

Relatively, the source and the drain having the thickness which is the thin source and drain, in other w ords, 0.2㎛ or less have the big resistance to cannot wi th the be desirable paper. This reversely affects the el ement performance. Relatively, it was proposed that th e source and the drain which was thin with each relativ e were formed but the purpose acts as the low-ohmic

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이 형성되는 것이 제안되었는데 그 목적은 저-저항 전류 분류기로서 작용하도록 한 것이다. 이에 관해 금속 실리사이드 커버된 소스 및 드레인의 효과적인(전기적)두께, 즉 소스-드레인-게이트 상호 작용에 포함되는 두께는 활성층의 표면 아래로 뻗어있으며 그 표면에 비교하여 아래에 놓인(두껍게 도핑된) 소스 및 드레인과 금속 실리사이드 영역의 결합된 두께이다.

electric current division device in order to include the molybdenum silicide (MoSi(SB)2(/SB)) the relatively low source/drain resistance is realized using the source and the thin drain, and the domain put on the upper part of the metal silicide like the tungsten silicide (WSi(SB)2(/SB)) or the titanium silicide (TiSi(SB)2(/SB)). It is the source, which the effective thickness of the drain and the source , and the thickness included in other words, the source-drain - gate interaction compare in the surface the metal silicide is covered about this while spreading under the surface of the active layer and is put (it the thickly is doped)s the drain and the combined thickness of the metal silicide domain.

금속 실리사이드 커버된 소스 및 드레인을 포함하는 IC를 제조하기 위한 이전의 시도는 소스 및 드레인을 형성하기 위한 통상적인 절차의 이용을 포함하고 있는데, 즉 소스 및 드레인이 필요한 실리콘 기판의 영역으로 소스 및 드레인 도펀트를 주입 및 확산하는 단계와 다음에 밑에 있는 소스 및 드레인의 표면에 Mo, W, Ti와 같은 금속을 증착시키는 단계를 포함하고 있다. 이때 증착된 금속은 대응하는 금속 실리사이드를 형성하도록 소스 및 드레인의 아래에 놓인 실리콘과 반응한다. 이 기술은 소스 및 드레인이 초기에(금속 실리사이드의 형성에 앞서) 실리콘내로 비교적 깊게 연장된 경우, 즉 실리콘내로 약 0.25㎛ 이상 연장된 경우에 효과적인 것으로 입증되었다. 그러나 이 기술은 소스 및 드레인이 초기에 실리콘내로 비교적 작은 거리만을 연장되어 있는 경우, 즉 약 0.25㎛보다 작거나 같은 거리만큼 연장되어 있는 경우에는 바람직하지 못한 것으로 입증되었는데, 이것은 바람직하지 못하게 큰 양의 소스/드레인 실리콘이 금속 실리사이드를 형성하는데 소비되어 결과적으로 소스/드레인 p-n 접합을 통해 연장된 즉 단락 회로시키는 금속 실리사이드 스파이크를 초래하기 때문이다.

The previous attempt for manufacturing the source which the metal silicide is covered and IC including the drain comprise the step of evaporating the Mo on the surface of the step of being expanded over the domain of the silicon substrate in which in other words, the source and drain are necessary it injects the source and drain dopant it includes the usage of the normal procedure for forming the source and drain and the source which is in the beneath in the next and drain, W, and the metal like the Ti. It then reacts with the silicone which is beneath puts of the drain and source in order to form the metal silicide in which the deposited metal corresponds. Relatively in case this technology the source and drain were deeply extended due to the initial (before the formation of the metal silicide) within the silicone with it was effective in case of being extended within in other words, the silicone over about 0.25㎛ it was proved. But it was proved that it could not with the be desirable paper in case this technology the source and drain were extended due to the initial within the silicone only the distance which was relatively small as the distance which was smaller than the case, of being extended in other words, about 0.25㎛ or thed same. When the metal silicide is formed but the source/drain silicone of the large amount is consumed and so that this cannot with the be desirable paper this is extended through the source/drain p-n junction the key in the short circuit is due to cause the metal silicide spike.

금속 실리사이드 커버된 소스 및 드레인을 형성하기 위한 다른 기술이 1983년 IEDM 기술 다이제스트 670 내지 673페이지에 #8220#실리사이드를 통한 측면 확산을 이용한 새로운 저저항의 얇은 접합 형성 방법#8221#이란 제목으로 에이취.오가바야시 등에 의해 기술되어 있다. 이 기술에 따라, 이와 같은 소스 및 드레인은 초기에 실리콘 기판의 표면상에 예를들어 0.1㎛의 두께를 가진 몰리브데늄 실리사이드(MoSi2) 영역을 제조함으로써 형성되는데, 이것은 실리콘 기판상에 몰리브데늄을 증착시키고 아래에 놓인 실리콘과 몰리브에늄을 반응시킴으로써 실현된다. 이때 소스/드레인 도펀트를 몰리브데늄 실리사이드로 확산되어 그곳으로 부터 소스/드레인 p-n 접합을 형성하도록 아래에 놓인 실리콘으로 확산된다. 즉 몰리브데늄 실리사이드 커버된 실리콘 기판이 개스 또는 고체의 도펀트 소스에 접촉되어져 한 단계로 몰리브데늄 실리사이드와 아래에 놓인 실리콘내로 도펀트를 효과적으로 확산시키기 위해 충분히 높은 온도와 충분히 긴 시간 주기동안, 즉 1000℃에서 20분동안 가열된다. 이와 달리 도펀트는 2단계 공정으로 실리콘내로

The thin joining formation process " of the new low resistance in which the source which the metal silicide is covered and the dissimilar technology for forming the drain use the side spreading through the " silicide for 1983 year IEDM technology digest 670 through 673 page is the title H. It is described by the auger drill night market etc. According to this technology, by manufacturing the molybdenum silicide (MoSi(SB)2(/SB)) domain having for example, the thickness of 0.1㎛ on the surface of the silicon substrate at a rate per the initial this kind of source and drain are formed. By reacting the silicone and the mole rib enium in which this evaporates molybdenum on the silicon substrate and which is beneath puts it is realized. Then, it is diffused to the silicone which is beneath puts in order to be the source / drain dopant diffused including to the molybdenum silicide and form the source/drain p-n junction from that place. That is,

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확산되는데, 제1단계는 초기에 몰리브데늄 실리사이드 커버된 실리콘 기판을 비교적 낮은 온도, 즉 800℃로 가열하여 가스 또는 고체의 도펀트 소스로 부터 몰리브데늄 실리사이드내로(실리콘내로는 확산되지 않음)도펀트를 확산시키는 것이다. 계속해서 도펀트는 실질적으로 보아 높은 온도, 즉 950℃나 1000℃로 기판을 가열함으로써 몰리브데늄 실리사이드로 부터 실리콘내로 확산된다. 1단계 확산 공정을 비교적 깊은 소스 및 드레인을 만드는데, 즉 만일 몰리브데늄 실리사이드가 0.1㎛ 두께이면, 소스 및 드레인은 실리사이드의 상부 표면 아래로 약 1.5㎛ 연장된다. 2단계 확산 공정은 보다 얕은 소스 및 드레인을 만드는데, 이것은 비교적 깊은 것으로서, 만일 몰리브데늄 실리사이드가 0.1㎛ 두께라면, 소스 및 드레인은 실리사이드의 상부 표면아래로 약 0.36㎛ 연장된다.

enough enough heated with the high temperature for the long time period in other words, 1000℃ for 20 minutes the dopant is effectively diffused to the step that the silicon substrate which the molybdenum silicide is covered is contacted with the dopant source of the gas or solid within the silicone which is beneath puts with the molybdenum silicide. On the other hand, the dopant is diffused to 2 stage processing within the silicone. The first step heats the silicon substrate which the molybdenum silicide is covered with the relatively low temperature, in other words, 800℃ in the initial and the dopant is diffused from the dopant source of the gas or solid in the molybdenum silicide (it is not diffused within the silicone). And then, by the dopant substantially looking and heating the substrate with the high temperature, in other words, 950℃ or 1000℃ the dopant is diffused from the molybdenum silicide within the silicone. 1 step diffusion process the source and the drain which is relatively deep is made. If the molybdenum silicide is 0.1㎛ thickness , the source and drain are extended under the top surface of the silicide with about 1.5㎛. The source and the drain which is shallow than 2 step diffusion process are made. Relatively this is deep. The molybdenum silicide is 0.1㎛ thickness. If it is the case the source and drain are extended under the top surface of the silicide.

금속 실리사이드 커버된 소스 및 드레인을 형성하기 위해 이전에 사용된 또다른 기술에 있어서, 텅스텐 실리사이드(WSi2) 영역이 초기에 실리콘 기판상에 형성되고 텅스텐 실리사이드내로 도펀트가 주입된다(확산이 아님)(1985년 IEDM 기술 다이제스트 407 내지 410페이지에 있는 에프.씨.쇤 등의 #8220#도핑된 실리사이드 기술에 의한 0.1㎛ N+/P와 P+/N 접합의 형성#8221#을 참조) 이때 주입된 도펀트는 통상적인 용광로 어닐링 기술이나 금속 열 어닐링(RTA)기술을 이용하여 기판을 가열함으로써 텅스텐 실리사이드로 부터 실리콘 기판내로 확산된다(RTA에 대해서는 1983년 전자화학회의 저널 130권의 484페이지에 있는 티.오.세리윅크의 #8220#단시간 어닐링#8221#을 참조) 중요하게도(에프.씨.쇤 등에 의해 알려진 바와 같이), 텅스텐 실리사이드 영역의 두께는 0.2㎛이며, 대응하는 주입량과 가열 온도 및 가열 시간은 텅스텐 실리사이드의 특정 두께에 대해 모두(추정적으로)특수하게 맞추어진다. 결과적으로, 상기 특정 기술은 단지 0.3㎛보다 크거나 같은 깊이(텅스텐 실리사이드의 상부 표면으로 부터 측정될때)를 가진 소스 및 드레인만을 만들게된다.

F which the tungsten silicide (WSi(SB)2(/SB)) domain is formed in the initial on the silicon substrate and the dopant is injected as to the source which the metal silicide is covered and another technology which is used in order to form the drain, within the tungsten silicide (it is not diffusion) is in 1985(year IEDM technology digest 407 through 410 page. The furnace annealing technology, in which the dopant which is then the formation " of 0.1㎛ N + / P by the A -doped silicide technology the " including seed etc. and P + / N union injected with the reference) is normal importantly, the drawing F it is diff used from the tungsten silicide within the silicon substr ate (the reference the " short time annealing " of the t hio. ***. which is in 484 page of the journal 130 Keow n of 1983 year electronization learned society about RT A) the substrate is heated up using the metal thermal annealing (RTA) technology. As is well known, seed the thickness of the tungsten silicide area is 0.2㎛ with the etc. and the everyone (putatively) is unusual the injec tion amount, the heating temperature and heating time corresponding to are adjusted about the specific thickn ess of the tungsten silicide. Consequently, it produces only the source and the drain in which the specific tec hnique has the depth (it is measured from the top surfa ce of the tungsten silicide) which is only greater than 0.3㎛ or thes same.

1986년 산 디에고의 VLSI에 관한 1986 심포지엄에서 논문 다이제스트의 #8220#서브-미크론 CMOS에 대한 TiSi2 및 WSi2 실리사이드된 낮은 접합의 비교#8221#란 제목으로 엔.고바야시 등에 의해 상기 기술의 변형이 기술되어 있다. 여기에서는 텅스텐 실리사이드 또는 티타늄 실리사이드의 0.1㎛ 두께 영역이 초기에 실리콘 기판상에 형성되고, 소스/드레인 도펀트가 실리사이드 내로 주입되어 실리사이드로 부터 실리콘내로 확산

In 1986 symposium about VLSI of 1986 year San Diego, disclosed is the deformation of technology including the comparison " of the low junction which is silicidated the TiSi 2 about the " sub-micron CMOS of the paper digest and WSi 2 is the title N Kobayashi. etc. Here, 0.1㎛ thickness domain of the tungsten silicide or the titanium silicide is formed in the initial on the silicon substrate a

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된다. 그러나 텅스텐 실리사이드의 경우에 엔.고바야시 등의 저널 논문의 제1도에 도시된 바와같이, 이 논문의 저자는 0.2㎛보다 훨씬 큰 깊이(텅스텐 실리사이드의 상부 표면으로 부터 측정할때), 즉 0.26㎛ 및 0.28㎛의 깊이를 가진 소스 및 드레인을 만드는 주입량과 가열 온도 및 가열 시간을 가르쳐주고 있다. 이에 대비하여, 티타늄 실리사이드의 경우에는 제1도에 도시된 바와같이 저자가 0.2㎛보다 작은 깊이(티타늄 실리사이드의 표면으로 부터 측정할때), 즉 0.16㎛의 깊이를 가진 소스나 드레인을 만드는 비소 주입량과 가열 온도 및 가열 시간을 가르쳐 주고 있지 않다. 그러나 제1도로 부터 명백한 바와같이, 티타늄 실리사이드/실리콘 인터페이스에서의 비소의 농도는 비교적 낮다. 이것은(저널 논문의 저자의 주장과는 반대로) 상기 비교적 낮은 인터페이스 농도가 바람직하지 못하게 높은 특정 저항(Rc)을 유도하기 때문에 매우 중요한데, 여기서 Rc는 10-6Ω-Cm2보다도 크다. 사실 상기 저널 논문에서 저자는 인터페이스 비소 농도를 증가시키기 위해(추정상 Rc를 낮추기 위한 목적으로) 추가의 비소를 실리콘(티타늄 실리사이드가 아닝) 대로 주입하는 바람직성을 나타내고 있다. 그러나 불행하게도 알려진 바와같이, 이와 같은 절차는 실리콘 기판이 추가의 도펀트 확산, 결과적으로 비교적 깊은 소스 및 드레인을 만드는 실리콘내로의 생성 주입 손상을 어닐링하기 위해 비교적 높은 온도로 가열되어야만 하기 때문에 바람직하지 못하다.

nd the source / drain dopant is injected within the silici de and it is diffused from the silicide within the silicone. But in case of the tungsten silicide, the source, in whic h the author of this paper has the depth (it measures f rom the top surface of the tungsten silicide), which is more greater than 0.2㎛ in other words, the depth of 0.28㎛ and 0.26㎛ the injection amount, making the drai n the heating temperature and heating time are taught as shown in Figure 1 of the journal paper including N Ko bayashi. etc. Thus, it compares and the source in whic h the author has the depth (it measures from the surfa ce of the titanium silicide), smaller than 0.2㎛ in other words, the depth of 0.16㎛ in the titanium silicide as sh own in Figure 1 or the arsenic implant amount making t he drain and heating temperature and heating time are not taught. But as shown in it is clear from Figure 1 rel atively the concentration of the arsenic at the titanium silicide / silicon interface is low. Because the high speci fic resistance (Rc) is induced so that the interface con centration which is low with this (contrary to the insist ence of the author of the journal paper) relative canno t with the be desirable paper it is very important. Here the Rc is greater than 10 - 6 Ω- Cm 2 . Fact, in the jo urnal paper, so that the author increase the interface arsenic concentration (to the purpose of lowering the e stimation phase Rc), the additional arsenic the overall quality injected is shown according to silicone (it is not titanium silicide). But because the relatively high tempe rature has to be heated by this kind of the procedure s o that the silicon substrate anneal the additional dopan t diffusion, and the production injection damage into th e source which is consequentlyrelatively deep and the silicone making the drain as is well known, it unfortunat ely cannot with the be desirable paper.

그러므로 IC제조 방법의 개발에 종사하는 사람들은 약 10-6Ω-cm2 이하의 Rc를 나타내는 금속 실리사이드를 포함하는 비교적 얕은 소스 및 드레인을 가진 IC를 제조하기 위한 방법을 추구해왔다.

Therefore, the process for manufacturing the source which was relatively shallow including the metal silicide in which the people engaged in the development of the method of fabricating IC showed the Rc less than abou t 10 - 6 Ω- cm 2 and IC having the drain had been bein g investigated.

본 발명은 금속 함유 물질 영역, 즉 기초 금속이나 금속 실리사이드와 같은 금속 함유 혼합물을 함유하는 영역으로 커버된 소스나 드레인을 형성하기 위한 새로운 기술을 포함한다. 중요하게도 이 새로운 기술은 약 0.2㎛이하의 깊이(물질 영역의 상부 표면과 비교하여)를 갖고 약 10-6Ω-cm2이하의 Rc를 나타내는 물질 영역 커버된 소스나 드레인을 만든다.

The invention includes the source covered with the domain containing the metal containing mixture or the new technology for forming the drain, such as the met al containing material domain, in other words, the base metal or the metal silicide. Importantly, the source or t he drain which the territory of material in which this ne w technology has the depth (it compares with the top surface of the territory of material) less than about 0.2 ㎛ and showing the Rc less than about 10 - 6 Ω- cm 2 i s covered is made.

본 발명의 기술에 따라, 0.2㎛이하의 평균 두께 t를 가진 금속 함유 물질 영역이 초기에 반도체 기판의 표면상에 형성된다. 그 다음에, 하나 혹은 그 이상의 도펀트가 상기 영역에 주입되고, 반도체 기판이 가열되어 상기 도펀트가 상기 영역으로 부터 기판내로 확산되게 된다. 약 10-6Ω-cm2이하의 Rc를 발생하기 위해, 가열 절차는 상기 물질 영역/기판 인터페이스에 인접한 기판에서 최소한 하나의 도펀트를 집중시켜야 하는데, 이것은 기판 가열전의 인터페이스에서의 쇼트키 전위 장벽의 높이에 의해 결정되는 최소 값보다 크거나 같다. 상기 최소값을 실현하기 위해 다음 3조건이 만족되어야 한다고 알려져 있다. 제1조건은 가열 절차 동안에 사용된 온도에서 기판내의 최소한 하나의 도펀트의 고체 용해도가 상기 최소값보다 크거나 같아야 한

According to the technology of the invention, the metal containing material domain having the average th ickness t less than 0.2㎛ is formed in the initial on the s urface of the semiconductor substrate. And then, one or the dopant described in the above is injected in the domain and the semiconductor substrate is heated and the dopant is diffused from the domain within the subst rate. In order that it is generated the Rc less than abo ut 10 - 6 Ω- cm 2 the dopant of at least one has to be focused in the substrate in which the heating process i s adjacent to the territory of material / plate interface. It is greater than the minimum value in which this is de

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다는 것이다. 제2조건은 상기 동일한 도펀트에 있어서, 상기 물질 영역의 평균 두께에 대한 대응하는 주입량의 비율이 상기 가열 온도에서 상기 물질 영역내의 상기 도펀트의 고체 용해도의 약 1/2보다 크거나 같아야 된다는 것이다.(이것에 대해서, 예를들어, 엔.고바야시 등에 의해 사용된 비소 주입량이 상기 제2임계 요구조건을 만족하지 못한다고 결정되었다). 원하는 인터페이스 농도를 실현하고 유용한 소스/드레인 접합을 실현하기 위해 만족되어야할 제3조건은, 상기 동일한 도펀트에 대해 상기 물질 영역내로 주입되는 도펀트 이온의 총수효가 아래에 놓인 확산된 소스 및 드레인을 형성하는데 필요한 수보다 실질적으로 커야된다는 것이다. 만일 상기 물질 영역/기판 인터페이스에 가까이 인접한 기판에서의 도펀트의 농도의 필요한 최소값이 Co로 표시되고 상기 물질 영역의 바닥과 비교하여 소스/드레인 접합의 원하는 깊이가 X로 표시되면 제3조건은 자동적으로 1g5Co#183#X/2가 만족된다. 실예로 제2조건을 만족하는 주입량은 또한 제3조건도 만족한다. 그러나 주입량의 제2조건을 만족하지만 5Co#183#X/2 보다 작은 경우에 제3조건은 Co#183#X/2보다 크거나 같은 양만큼 상기 주입량을 증가시킴으로써 확실하게 만족되게 된다.

termined with the height of the schottky potential barrier at the interface of the substrate heating total or it is the same. It is known the minimum value is realized that the next 3 condition has to be satisfied. In the temperature in which the first condition is used for the heating process, it is greater than the minimum value or the solid solubility of the dopant of at least one within the substrate has to be the same. As to the article 2 gun is the above-mentioned same dopant, the rate is large than about 1/2 of the solid solubility of the dopant within the territory of material or the rate of the injection amount corresponding to about the average thickness of the territory of material be the same in the heating temperature. (This was determined that the arsenic implant amount used with the etc. was unable to be satisfied the second critical requirement specification about this) The article 3 gun to be satisfied it realizes the source/drain junction realizing the desired interface concentration and is useful forms the source and the diffused drain in which the total amount of the dopant ion injected within the territory of material is beneath puts about the above-mentioned same dopant but the substantially is *** than the necessary number. If the necessary minimum value of the concentration of the dopant at the substrate adjacent to the territory of material / plate interface is indicated as the Co and it compares with the bottom surface of the territory of material and the desired depth of the source/drain junction is indicated as X, the article 3 gun 1 g5Co·X / 2 is automatically satisfied. For example, the injection amount satisfied the article 2 gun moreover, the article 3 gun is satisfied. But it is satisfied the article 2 gun of the injection amount but in case of being smaller than 5Co·X / 2 since the article 3 gun increases the injection amount as the amount which is large than the Co·X / 2 or thes same it is authentically satisfied.

본 발명의 기술은 또한 원하는 깊이를 가진 소스 및 드레인을 만드는데 필요한 가열 온도-시간 프로필을 선택하기 위한 절차(후술됨)를 포함한다.

The technology of the invention includes the source having the desired depth and the procedure (it is mentioned later) which it is to make the drain but select the necessary heating temperature - time profile.

본 발명은 MOS나 MES 반도체 IC와 같은 반도체 소자뿐 아니라 그 합성 소자를 제조하기 위한 방법을 모두 포함하고 있다. 본 발명의 방법에 따라 제조된 소자는 금속 함유 물질 영역, 즉 텅스텐(W)과 같은 기초 금속을 함유하는 영역으로 커버된 최소한 하나의 소스나 드레인을 포함하고 있다. 이와 달리 금속 함유 물질 영역은 금속 실리사이드, 즉 코발트 실리사이드(CoSi2), 티타늄 실리사이드(TiSi2), 텅스텐 실리사이드(WSi2), 몰리브데늄 실리사이드(MoSi2), 탄탈륨 실리사이드(TaSi2)나 플라티늄 실리사이드(ptSi)와 같은 금속 함유 혼합물을 포함한다. 또한 상기 물질 영역의 상부 표면에 비교하여 상기 물질 영역으로 커버된 소스나 드레인의 깊이는 약 0.2㎛ 보다 작거나 같다. (본 발명의 목적을 위해 상기 물질 영역 커버된 소스나 드레인의 깊이는 상기 물질 영역의 상부 표면에 대한 최소 면적 평면 근사부로 부터 소스나 드레인이 형성되는 반도체 기판과 소스나 드레인 사이의 인터페이스의 최저점까지 직각으로 연장된 길이다. 만일 예를들어 소스나 드레인이 n형 전도성이면 인터페이스는 소스나 드레인에서의 n형 도펀트의 농도가 기판에서의 p형 도펀트의 농도가 같은 (그 역도 마찬가지임) 점들이 궤적이다. 이와 같은 인터페이스는 2차 이온 질량 분광학(secondary ion mass spectroscopg : SIMS)과 같은 종래의 기술을 이용하여 쉽게 위치된다.) 또한 아래에 놓인(확산된) 소스나 드레인에 대한 상기 물질 영역의 특정 접촉 저항, Rc는 약 10-6Ω#183#cm2보다 작거나 같다.(Rc는 IEEE전자

The method in which the invention manufactures not only the semiconductor device like MOS or the MES semiconductor IC but also the synthesis element the altogether is included. The device manufactured according to the method of the invention includes the source or the drain of at least one covered with the domain containing the base metal, such as the metal containing material domain, in other words, the tungsten (W). On the other hand, the metal containing material domain comprises the metal silicide, in other words, the cobalt silicide (CoSi(SB)2(/SB)), the titanium silicide (TiSi(SB)2(/SB)), the tungsten silicide (WSi(SB)2(/SB)), the molybdenum silicide (MoSi(SB)2(/SB)), the tantalum silicide (TaSi(SB)2(/SB)), or the metal containing mixture like the platinum silicide (ptSi). Moreover, it is smaller than about 0.2㎛ or the depth of the source or the drain which compares in the top surface of the territory of material and which is covered with the territory of material is the same. (It is the way in which the depth of the source or the drain which the territory of material is covered for the object of the present invention is abeam extended to the peak base of the interface between the semiconductor substrate in which the source or the drain is formed from the minimum area plane approximation part

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소자란 책의 544페이지에 있는 케이.케이.에지, #8220#MOSFET의 접촉 저항을 측정하기 위한 새로운 기술#8221#에 기술된 종래의 절차를 이용하여 쉽게 측정된다.)

toward the top surface of the territory of material and the source or the drain. For example, if the source or the drain is the n-type conductivity, it is the trajectory the concentration of the P-dopant at the substrate as to the interface, of the concentration of the n-type dopant at the source or the drain is the same (it applies equally to the reverse) that. It is smaller than about 10 - 6 Ω· cm 2 or the specific constant resistance of the territory of material about the source or the drain , and the Rc which this kind of the interface is easily located using the conventional technology like the secondary ion mass spectrometry (secondary ion mass spectroscopg : SIMS) is moreover beneath put (it is diffused)s are the same. K in which (Rc the IEEE electric component is in 544 page of book. K. It is easily measured using the conventional procedure described in the new technology " for measuring the edge, and the constant resistance of the "MOSFET.

본 발명의 방법에 따라, 상기 물질 영역 커버된 소스나 드레인이 초기에 실리콘이나 갈륨 비소와 같은 반도체 물질을 포함하는 기판상에 상기 물질 영역을 형성함으로써 형성된다. 이와 같은 물질 영역은 예를들어, 종래 기술, 즉 종래의 스퍼터링(sputtering)기술을 이용하여, 기판상에 상기 영역을 구성하는 물질을 침착시킴으로써 형성된다. 이와 달리, 만일 상기 물질 영역이 예를들어 금속 실리사이드를 포함하고 기판이 실리콘으로 되어 있으면, 상기 물질 영역은 대응하는 기초 금속을 실리콘 기판상에 침착시키고 금속 실리사이드를 형성하기 위해 침착된 금속을 아래에 있는 실리콘과 반응시킴으로써 최소한 부분적으로 쉽게 형성된다. 약 0.2㎛보다 작거나 같은 깊이를 가진 상기 물질 영역 커버된 소스나 드레인을 실형하기 위해서는 상기 물질 영역의 최대 두께, 즉 결과적으로 평균 두께(일반적으로 균일하지 않은 두께임)가 0.2㎛보다 작아야 된다. 또한 (균일하지 않은 두께의) 상기 물질 영역의 최소 두께는 약 0.1㎛보다 크거나 같은 것이 양호하다. 약 0.1㎛보다 작은 최소 두께는 바람직하지 못한데 이것은 다른 이유중에서, 상기 물질 영역의 대응하는 부분이 종종, 주입 단계동안에 매우 많은 양의 도펀트를 상기 물질 영역이 아닌 기판내로 주입되도록 허용하는 매우 많은 수의 핀구멍을 포함하게 되기 때문이다.

According to the method of the invention, since the source or the drain which the territory of material is covered forms the territory of material on the substrate including the semiconductor material such as the silicone and GaAs in the initial the drain is formed. By sinking the material comprising the domain on the substrate this kind of the territory of material is formed using for example, the prior art, in other words, the conventional sputtering technology. On the other hand, if the territory of material includes for example, the metal silicide and the substrate if to the silicone , by the base metal in which the territory of material corresponds being sunk on the silicon substrate and reacting the metal which is deposited in order to form the metal silicide, with the silicone which is beneath have the metal is partly easily formed. It is for the source or the drain which the territory of material having the depth which is smaller than about 0.2㎛ or thes same is covered with the prison sentence and consequently the average thickness (it the generally is the thickness which is not uniform) be smaller than 0.2㎛ with the maximum thickness of the territory of material. Moreover, is good what the minimum thickness of (of the thickness which is not uniform) territory of material is greater than about 0.1㎛ or thes same. The minimum thickness smaller than about 0.1㎛ cannot with the be desirable paper but the part corresponding to of the territory of material includes the pin hole which often allows very many dopant of the amount for the impregnation step in order to be injected within the substrate which is not territory of material, and is very many of the number among the reason why this is different.

상기 물질 영역을 형성한 후에, 하나 혹은 그 이상의 도펀트가 상기 물질 영역내로 주입되고, 계속해서 원하는 소스나 드레인을 형성하기 위해 상기 물질 영역으로 부터 상기 기판내로 주입된 도펀트가 확산되도록 기판이 가열된다. 만일 기판 반도체 물질이 p형 전도성이면, 주입된 도펀트는 기판에서 전자도우너를 형성해야 하며, 만일 기판 반도체 물질이 n형 전도성이면 상기 도펀트는 전자 액셉터를 형성해야 한다. 예를들어 실리콘의 경우에, 유용한 도오너 이온은 인(p)과 비소(As)이온을 포함하며, 동시에 유용한 액셉터 이온은 붕소(B)이온을 포함한다.

After the territory of material is formed one or the dopant described in the above is injected within the territory of material and the substrate is heated so that the dopant injected from the territory of material within the substrate is diffused in order to form the source or the desired drain. If the substrate semiconductor material is the p-type conductivity , the injected dopant has to form the electron donor at the substrate and the dopant has to form the electron acceptor if the substrate semiconductor material is the n-type conductivity. For example, the drawing owner ion which is useful in case of the silicone includes the phosphorus (p) and the acceptor ion which includes the arsenic (As) ion and is sim

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ultaneously useful. Is the boron (B) ion.

전술한 바와같이, 약 10-6Ω#183#cm2보다 작거나 같은 Rc를 실현하기 위해, 기판 가열 절차는 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 최소한 하나의 도펀트의 농도를 산출해야 되는데 이것은 기판 가열 이전의 상기 물질 영역/기판 인터페이스에서의 쇼트키 전위 장벽의 높이에 의해 결정되는 최소값보다 크거나 같다. 즉, 상기 전위 장벽 높이를 아는 것은 대응하는 최소값을 의미하고 있다. 이점에 있어서, 금속 함유 물질과 반도체 물질 사이의 인터페이스에서의 쇼트키 전위 장벽 높이는 원하는 Rc를 발생시키기 위해 인터페이스 도펀트 농도의 대응하는 최소값이 필요한 바와같이 문헌상 쉽게 이용할 수 있다. 예를들어, n형이나 p형 실리콘과 다양한 기초 금속 사이의 인터페이스에서의 쇼트키 전위 장벽 높이는 에스.엠.스제의 #8220#반도체 소자의 물리학#8221# 제2판(1981) 292 페이지에서 찾아볼 수 있다. 비슷하게 예를들어 n형 또는 p형 실리콘과 다양한 기초 금속 사이의 인터페이스 사이의 쇼트키 전위 장벽 높이는 에스.피.뮤라카의 #8220#VLSI 응용을 실라이드#8221#(1983) 15페이지에서 찾아볼 수 있다.

As described above, in order that the Rc which is smaller than about 10 - 6 Ω· cm 2 or thes same is reali zed it is greater than the minimum value which produce the concentration of the dopant of at least one at the substrate in which the substrate heating process is adj acent to the territory of material / plate interface but i n which this is determined with the height of the schot tky potential barrier at the territory of material / plate i nterface of the substrate heating previous or it is the s ame. That is, the minimum value in which it correspond s to know the potential barrier height is meant. As to t he advantage, in order to generate the Rc in which the schottky potential barrier height at the interface betwe en the metal containing material and the semiconducto r material desires, as the minimum value corresponding to of the interface dopant concentration been necessa ry it easily can use. For example, the schottky potentia l barrier height at the interface between the n-type or the p-type silicone and the various base metal is S. It can look out in the physics " second board (1981) 292 page of the " semiconductor device of M S. M. Sze. An alogously, for example, the schottky potential barrier h eight between the interface between the n-type or the p-type silicone and the various base metal is S. The "V LSI application of the blood Mura. car can be looked ou t in the ride #8221 U # (1983) 15 page.

또한 거의 모든 쇼트키 전위 장벽 높이에 대응하는 약 10-6Ω#183#cm2보다 작거나 같은 Rc를 발생시키는데 필요한 최소 인터페이스 도펀트 농도는 에스.엠.스제의 상기 참조 논문의 304 내지 305페이지에서 찾아볼 수 있다. 예를들어 만일 상기 물질 영역이 코발트 실리사이드(CoSi2)를 포함하고 기판이 p형 실리콘을 포함하며 주입된 n형 도펀트중 하나가 비소(As)라면, 에스.피.뮤라카의 상기 참조 온도에 따라, 대응하는 쇼트키 전위 장벽 높이는 0.64볼트이며, 에스.엠.스제의 상기 참조는 논문에 따라 비소의 대응하는 최소 인터페이스 농도는 약 1#215#1020cm-3이다. 비슷하게, 만일 상기 물질 영역이 티타늄 실리사이드(TiSi2)를 포함하고 기판이 n형 실리콘을 포함하며 주입된 p형 도펀트중 하나가 붕소(B)라면, 에스.피.뮤라카의 상기 논문에 따라 대응하는 쇼트키 전위 장벽 높이는 0.5 볼트이고 에스.엠.스제의 상기 논문에 따라 붕소의 대응하는 최소 인터페이스 농도는 약 3#215#1019cm-3이다.

Moreover, the minimum interface dopant concentration necessary to generate the Rc which is smaller than abo ut 10 - 6 Ω· cm 2 corresponding to all schottky potenti al barrier heights or thes same is S. It can look out in 3 04 of the reference paper of M S. M. Sze. through 305 page. For example, one among the n-type dopant whic h is injected while the territory of material includes the cobalt silicide (CoSi(SB)2(/SB)) and the substrate inclu des the p-type silicone is the arsenic (As), S. S the sc hottky potential barrier height corresponding according to the reference temperature of the blood Mura. car is 0.64 bolt. According to the see above of M S. M. Sze. i s paper, the minimum interface concentration of arseni c corresponding to is about 1× 10 20 cm - 3 . Analogo usly, one among the P-dopant which is injected while t he territory of material includes the titanium silicide (Ti Si(SB)2(/SB)) and the substrate includes N type silicon is the boron (B), S. S the schottky potential barrier hei ght corresponding according to the paper of the blood Mura. car is 0.5 bolt. According to the paper of M S. M. Sze, the minimum interface concentration of boron corresponding to is about 3× 10 19 cm - 3 .

또한 전술한 바와같이, 약 10-6Ω#183#cm2보다 작거나 같은 Rc를 발생시키기 위해 필요한 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 도펀트 농도를 실현하기 위해서는 3가지 조건이 만족되어야 한다고 알려져 있다. 제1조건은 기판 가열 절차동안에 사용된 온도에서 최소한 하나의 도펀트의 기판에서의 고체 용해도가 전술한 최소 인터페이스 농도보다 크거나 같아야 된다는 것이다. 중요하게도, 반도체에서 도펀트의 고체 용해도는 일반적으로 매우 민감하며 온도에 따라 증가한다. 결과적으로 제1조건은 사실 기판 가열 절차동안에 사용될 수도 있는 온도에 대한 최소값 Tmin을 강요한다. 즉, 최소한

Moreover, as described above, in order to realize the dopant concentration at the substrate adjacent to the necessary territory of material / plate interface in order to generate the Rc which is smaller than about 10 - 6 Ω· cm 2 or thes same, , the substrate is known that th ree condition has to be satisfied. In the temperature in which the first condition is used for the substrate heati ng process, it is greater than the minimum interface co ncentration in which the solid solubility at the substrat e of the dopant of at least one describes in the above

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하나의 도펀트의 기판에서의 고체 용해도가 원하는 Rc를 실현하는데 필요한, 상기 물질 영역/기판 인터페이스에 인접한 기판에서의 최소 도펀트 농도의 최소한 같게 되는 것을 보장하기 위해 가열 온도는 Tmin보다 크거나 같아야 된다. 이점에 있어서, 온도 함수로서의 다양한 반도체 물질에서의 다양한 도펀트의 고체 용해도는 문헌에서 이용 가능하다.(즉 에서 엠.스제에 의해 출판된 #8220#VLSI 기술에서의 제이.씨.씨.츠아이#8221#198 내지 199페이지를 참조하라).

or it be the same. Importantly, in the semiconductor, generally the solid solubility of the dopant is very sensitive and it increases according to the temperature. Consequently, the first condition extorts the minimum value Tmin which can be used about the temperature for the substrate heating process in fact. That is, in order to realize the Rc in which the solid solubility at the substrate of the dopant of at least one desires but guarantee being the same of the minimum dopant concentration at the necessary substrate adjacent to the territory of material / plate interface at least, it is greater than the Tmin or the heating temperature be the same. As to the advantage, the various various dopant at the semiconductor materials of solid solubilities as the temperature function plays in literature with available. (J in the "VLSI technology published by M S. M. Sze in other words. 198 through 199 page is referred to the CC. Tsai.

결과적으로 제1조건을 만족하는데 필요한 Tmin은 쉽게 결정된다. 예를들어, 740℃, 800℃ 및 900℃에서, 실리콘에서의 비소의 고체 용해도는 각각 1#215#1020cm-3, 1.5#215#1020cm-3, 2#215#1020cm-2이다. (상기 논문 제이.씨.씨.츠아이를 참조). 만일 비소가 n형 실리콘에서 n형 도펀트로서 사용되고 상기 물질 영역이 CoSi2로 이루어져 있으면, 전술한 바와 같이 원하는 Rc를 실현하는데 필요한 최소 인터페이스 농도는 1#215#1020cm-3이며, 결과적으로 Tmin은 740℃이다. 유사하게, 800℃ 및 900℃에서 실리콘에서의 붕소의 고체 용해도는 각각 3#215#1019cm-3 및 6#215#1019cm-3이다. 만일 붕소가 n형 실리콘에서 p형 도펀트로서 사용되고 상기 물질 영역이 TiSi2라면, 전술한 바와 같이 원하는 Rc를 실현하는데 필요한 최소 인터페이스 농도는 3#215#1019cm-3이며, 결과적으로 Tmin은 800℃이다.

Consequently, it is satisfied the first condition but the necessary Tmin is easily determined. For example, in 740℃, 800℃ and 900℃, the respectively the solid solubility of the arsenic at the silicone is 1× 10 20 cm - 3 , 1.5× 10 20 cm - 3 , 2× 10 20 cm - 2 . (The paper J. If arsenic is used in N type silicon as the n-type dopant and the territory of material is the CC. Tsai made of the CoSi 2 with the reference) , the consequently the Tmin is 740℃ the minimum interface concentration necessary is 1× 10 20 cm - 3 . Similarly, in 800℃ and 900℃, the respectively the solid solubility of the boron at the silicone is 3× 10 19 cm - 3 and 6× 10 19 cm - 3 . Boron is used in N type silicon as the P-dopant and consequently the if the Tmin is 800℃ the minimum interface concentration necessary to realize the territory of material is the TiSi 2 , the desired Rc as described above, is 3× 10 19 cm - 3 .

만족되어야 할 제2조건은 위에서 언급된 최소한 하나의 도펀트에 대해 상기 물질 영역의 두께 t에 대한 대응하는 주입량의 비율, 즉 I/t가 기판 가열동안에 사용된 온도(필수적으로 대응하는 보다 크거나 같은)에서 상기 물질 영역에서의 상기 도펀트의 고체 용해도의 1/2보다 크거나 같아야 되며, 바람직하게는 더 커야된다는 것이다. 여기서 논의되는 고체 용해도는 기판 가열 절차 동안에 사용된 온도에서, 상기 물질 영역과 기판 사이의 인터페이스를 포함하여 상기 물질 영역에서의 최소한 하나의 도펀트의 포화 레벨을 말한다. 중요하게도, 이 포화 레벨은 온도에 민감하며, 일반적으로 온도에 따라 증가한다. 또한 이 포화 레벨은 상기 물질 영역의 합성 성분과 상기 물질 영역의 결정성의 정도에 의존한다(즉, 예를들어 다결정 물질의 경우에, 도펀트는 종종 그레인(grain) 및 그레인 경계내에 분배된다). 또한 상기 포화 레벨은 상기 물질 영역/기판 인터페이스의 특성에 의존하는데, 즉 도펀트가 상기 인터페이스에서 비교적 높게 농축되는지의 여부에 의존한다.

The article 2 gun to be satisfied is the rate of the injection amount corresponding to about the thickness t of the territory of material about the dopant of at least one mentioned by the upper part, and *** it is large than 1/2 of the solid solubility of the dopant at the territory of material are. Here, the interface between the substrate and the territory of material are included and the saturation level of the dopant of at least one at the territory of material is referred to the temperature in which the discussed solid solubility is used for the substrate heating process. Importantly, this saturation level is sensitive to the temperature and the temperature increases according to the temperature. Moreover, this saturation level depends on the extent of the crystallization of the compound ingredient of the territory of material and territory of material moreover, the saturation level depends on the property of the territory of material / plate interface. The property depends on acceptance and rejection of the paper (in case of in other words, for example, the polycrystalline material, the dopant is often distributed within the grain and grain boundary) in which it is relatively high in other words, the dopant is concentrated in the interface.

일반적으로, 기판 가열 절차동안에 사용된 온도에서, (상기 물질 영역/기판 인터페이스를 포함하여) 상기 물질 영역내의 도펀트의 고체 용해도는 실험적으로 결정된다. 즉, 본 발명에 따라, 소자에 사용된 상기 물질 영역과 동일한 평균 두께를 가진

Generally, in the temperature used for the substrate heating process, the solid solubility of the dopant within (the territory of material / plate interface is included) territory of material is experimentally determined. That i

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상기 물질 영역의 제어 샘플이(소자에 사용된 기판과 동일한 합성 성분 및 구조를 가진)반도체 기판상에(소자의 제조에 사용된 바와 동일한 기술을 이용하여)형성된다. (중요하게도, 이하에서 더욱 자세히 설명되는 바와같이, 제어 샘플의 상부 표면의 영역 A는 상기 물질 영역의 그것과 동일하게 되는 것을 필요로 하지 않는다. 제어 샘플을 지탱하는 기판은 비워진 용광로, 즉 주위 압력이 예를들어 10-6 토르(torr)의 값으로 낮아지는 용광로에 배치된다. 이때 관심있는 도펀트를 포함하는 가스가 용광로내로 흘러들어간다. 예를들어, 만일 인이라면 유용한 인 함유 가스는 pH3이다. 유사하게, 만일 도펀트가 비소라면, 유용한 비소 함유 가스는 AsH3이며, 만일 도펀트가 붕소라면 유용한 붕소 함유 가스는 B2H6이다(pH3, AsH3 및 B2H6는 매우 유독성 가스이므로 적당한 안전 예방책이 사용되어야 한다는 것을 주목하자). 이점에 있어서, 도펀트 함유 가스의 유동률은 상기 가스의 부분 압력이 주위 압력의 최소한 백배가 되도록 충분히 높아야 되는데, 만일 주의 가스 압력이 10-6토르이면 도펀트 함유 가스의 부분 압력은 최소한 10-4토르가 되어야 한다. 이 필요성은 제어 샘플이 필수적으로 주위의 오염물질이 아닌 도펀트에 의해서만 (다음 단계동안에)포화되는 것을 보장하기 위한 것이다. 도펀트 함유 가스가 용광로내로 흐르는 동안, 용광로는 관련있는 온도, 즉 기판 가열동안에 사용될 온도로 가열되게 된다. 제어 샘플내에서 도펀트 포화를 실현하기 위해서는 이 온도가 최소한 1분동안 유지되어야 하는데, 최소한 30분 동안 유지되는 것이 바람직하다.

s, according to the invention, control sample (it has the compound ingredient which is identical with the used substrate in the device and the structure thereof) of the territory of material having the same average thickness as the territory of material used for the device are formed in the semiconductor substrate phase (using the used for the manufacture of the device same technology). (Importantly, hereinafter, as shown in it is more explained in detail the domain A of the top surface of the control sample does not require being identical with that of the territory of material. It is arranged in the blast furnace in which the substrate supporting the control sample is vacated, and the blast furnace in which in other words, the ambient pressure is decreased to for example, the value of 10 - 6 Torr. Then, the gas including the dopant having finds the gas way within the blast furnace. For example, the phosphorus containing gas which is useful if the if is the phosphorus is the pH 3 . Similarly, the arsenic containing gas is the AsH 3 , the boron contain gas which is useful if the dopant is boron is B 2 H 6 . The dopant is arsenic. If it is the case (it pays attention that the safety precaution in which the p H 3 , and the AsH 3 and B 2 H 6 are very appropriate since it is the toxic gas has to be used). As to the advantage, the flow rate of the dopant containing gas the partial pressure of the gas be enough high so that it becomes at least white times of the ambient pressure. In the partial pressure of the dopant containing gas, at least 10 - 4 Torr has to be if the attention gas pressure is 10 - 6 Torr. This necessity is to guarantee that the control sample is saturated with the dopant which the obligatorily is not neighbouring contaminant with (for the following step). While the dopant containing gas flows within the blast furnace the relevant temperature, and the temperature used for in other words, the substrate heating are heated by the blast furnace. The ionic degree has to be maintained for at least 1 minutes in order to realize the dopant saturation in the control sample. It is the be desirable to be maintained for at least 30 minutes.

도펀트 함유 가스에 영향을 받은 후에 제어 샘플은 용광로로 부터 이동되며 제어 샘플/기판 인터페이스를 포함하며 제어 샘플내의 도펀트 원자의 총 수 N이 예를들어 종래의 SIMS 기술을 이용하여 측정된다. 상기 물질 영역에서 도펀트의 고체 용해도는 바로 N/At이다. (원자의 총 수 N는 표면 영역 A에 선형적으로 비례한다는 것을 주목하자.) 결과적으로, 표면 영역은 다른지만, 동일한 평균 두께를 가진 제어 샘플은 동일한 값의 고체 용해도를 산출하게 된다). 결과적으로 제2조건을 만족하기 위해서는 I/tg0.5N/At가 되도록 I가 선택되어야 한다.

While including the control sample / plate interface after it is affected by the dopant containing gas while the control sample is moved from the blast furnace the total count N of the dopant atom within the control sample is measured using for example, the conventional SIMS technology. In the territory of material, the solid solubility of the dopant is immediately, N / At. (It pays attention that the total count N of the atom is linearly in proportion to the surface region A) Consequently, the surface region is different only whether I have to be selected so that I / t g0.5N / At is in order to the control sample having the same average thickness produce the solid solubility of the same value consequently be satisfied the article 2 gun.

전술한 실험적 절차를 이용하여, 예를들어 만일 상기 물질 영역이 코발트 실리사이드로 이루어지고, 0.07㎛의 평균 두께를 가지며, 실리콘 기판위에 놓여 있고, 도펀트가 비소라면, 5#215 #1015cm-2 이상의 주입량이 800℃의 온도에서 제2조건을 만족한다. 비슷하게, 상기 물질 영역이 티타늄 실리사이드로 이루어져 있고 0.08㎛의 평균 두께를 가지며 실리콘 기판위에 놓여있고, 도펀트가 붕소라면, 1#215#1016cm-2 이상의 주입량의 800℃의 온도에서 제2조건을 만족한다.

The territory of material is made of the cobalt silicide using the above-described empirical procedure for example and it has the average thickness of 0.07㎛ and it is puts on on silicon substrate and the dopant is arsenic. If it is the case the injection amount more than 5× 10 15 cm - 2 is satisfied the article 2 gun at a temperature of 800℃. Analogously, while the territory of material is made of the titanium silicide and it has the average thickness of 0.08㎛ it is puts on on silicon substrate a

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nd the dopant is boron. If it is the case it is satisfied t he article 2 gun at a temperature of 800℃ of the injecti on amount more than 1× 10 16 cm - 2 .

원하는 Rc를 실현하고 유용한 소스/드레인 접합(즉 예를들어 0.5볼트의 전압과 25℃의 온도에서 반전 전류에 대한 진행 전류의 비율이 106보다 크거나 같아지는 접합)을 실현하기 위해 만족되어져야 하는 제3조건은, 최소한 하나의 도펀트에 대해, 상기 물질 영역내로 주입된 도펀트 이온의 총수가 아래에 놓인, 확산된 소스나 드레인을 형성하는데 필요한 수보다 실질적으로 커야된다는 것이다. 만일 상기 물질 영역/기판 인터페이스에 인접한 상기 기판에의 도펀트 농도의 최소값이 Co로 표시되고 상기 물질 영역의 바닥과 비교하여 소스/드레인 P-N접합의 원하는 깊이가 X로 표시되면, 제3조건은 자동적으로 1#8805#5 Co#183#X/2이 만족되도록 제공된다. 그러나 만일 주입량이 제2조건을 만족하지만 5Co#183#X/2보다 작다면, 제3조건은 보다 크거나 같은 양만큼 상기 주입량을 증가시킴으로써 확실하게 만족되게 된다. 이점에 있어서, 위에서 주어진 두 주입량은 또한 제3조건도 만족한다.

The article 3 gun which is satisfied it realizes source/drain junction (the junction which is large than 10 6 or in which the rate of the progressing current ab out the reverse current becomes same at a temperatur e of in other words, for example, the voltage and 25℃ of 0.5 bolt) realizing the desired Rc and are useful form s the source or the diffused drain in which the total co unt of the dopant ion injected within the territory of m aterial is beneath puts about the dopant of at least on e but the substantially is *** than the necessary num ber. If the minimum value of the dopant concentration of the substrate adjacent to the territory of material / plate interface is indicated as the Co and it compares with the bottom surface of the territory of material and the desired depth of the source/drain P-N junction is in dicated as X , the article 3 gun is provided so that 1≥5 Co·X / 2 is automatically satisfied. But if the injection a mount is satisfied the article 2 gun but it is smaller tha n 5Co·X / 2 , by increasing the injection amount as the amount which is large than the article 3 gun or thes sa me it is authentically satisfied. As to the advantage, t wo injection amounts given in the upper part moreover, the article 3 gun is satisfied.

상기 금속 함유 물질 영역내로 주입된 이온의 에너지는 근본적으로 모든 이온, 즉, 이온의 최소한 90퍼센트가 상기 영역내로 주입되는 기초적인 반도체 기판내로는 주입되지 않도록 선택된다는 것을 주목하자. 이점에 있어서, 또한 실리콘의 본 발명에 사용된 금속 함유 물질 영역보다 밀도가 높지 않고, 그러므로 동일한 에너지를 가진 동일한 이온이 상기 물질 영역보다 더 큰 깊이로 실리콘내로 관통된다는 것을 주목하자. 결과적으로, 거의 모든 이온이 상기 물질 영역내로 주입되는 것을 보장하기 위해, 이온 에너지는 상기 물질 영역의 두께이하의 실리콘내로의 대응하는 관통 깊이를 산출하도록 선택된다.(이온 에너지의 함수로서의 실리콘내로의 이온 관통 깊이는 알.에이.콜롤레이저의 #8220#마이크로 전자공학처리 및 소자 설계#8221# 150 내지 153페이지에서 찾아볼 수 있다.)

The energy of the ion injected within the metal containing material domain fundamentally pays attentio n being selected in order not to be injected within the f undamental semiconductor substrate in which all ions in other words at least 90 percent of ion are injected wit hin the domain. As to the advantage, the density is no t moreover higher than the metal containing material d omain used for the invention of the silicone and it there fore pays attention that the same ion having the same energy is penetrated toward the depth which is greater than the territory of material within the silicone. Conse quently, in order that it guarantees that all ions are ne arly injected within the territory of material the thickne ss is selected so that the ion energy produces the nee dle depth corresponding to into the silicone less than t he thickness of the territory of material. (The ion need le depth into the silicone as the function of the ion ene rgy is the ra. It can look out in the " microelectronics p rocessing of the call call laser and device design " 150 through 153 page.

예를 들어, 60keV 이하의 주입 에너지(0.07㎛보다 작거나 같은 깊이로 실리콘을 관통하는 비스 이온의 90퍼센트가 되는 비소 이온 에너지)를 이용하여 0.07㎛의 평균 두께를 가진 코발트 실리사이드의 여역내로의 비소 이온의 주입은 거의 모든 비소 이온이 코발트 실리사이드내로 주입되는 것을 보장한다. 유사하게, 10keV 이하의 주입 에너지(0.08㎛ 이하의 깊이로 실리콘을 관통하는 붕소 이온의 90퍼센트가 되는 붕소 이온 에너지)를 이용하여, 0.08㎛의 평균 둑께를 가진 티타늄 실리사이드의 영역내로 붕소 이온을 주입하면 거의 모든 붕소 이온의 티타늄 실리사이드로 주입되는 것을 보장한다.

For example, the injection of the arsenic ion into the women reverse of the cobalt silicide having the averag e thickness of 0.07㎛ using the implant energy (the ars enic ion energy in which it becomes 90 percent of the bis ion passing through the silicone through the depth which is smaller than 0.07㎛ or thes same) less than 60 keV guarantees that all arsenic ions are injected within the cobalt silicide. Similarly, it guarantees that the dom ain is injected to the titanium silicide of all boron ions if the boron ion is injected using the implant energy (the boron ion energy in which it becomes 90 percent of the boron ion passing through the silicone through the dept h less than 0.08㎛) less than 10keV within the domain of the titanium silicide having the average bank of 0.08 ㎛.

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본 발명은 또한 원하는 소스/드레인 깊이를 실현하기 위해 기판 가열 동안에 이용될 온도-시간 프로필을 선택하기 위한 반복적(iterative) 기술을 포함하고 있다. 여기서, 상기 물질 영역이 두게는 기판의 도핑 레벨, NA 일대 공지되거나 지정된 것을 가정 한다. 또한 상기 세가지 조건이 만족되었고, 기판 가열의 결과로서 상기 물질 영역/기판 인터페이스에 인접한 기판내의 도펀트 농도가 원하는 Rc를 실현하는데 필요한 (공지된) 최소값인 Co보다 크거나 같은 것으로 가정한다. 처음에, 또한 간편성을 위해, 필수적으로 Tmin보다 크거나 같은 온도 T만이 가열 절차 동안에 사용된다고 가정한다. 만일 변수 X#180#가 상기 물질 영역의 바닥에 대한(확산된) 소스나 드레인내의 점의 수직 위치를 표시하고, T가 시간을 나타내고, D(=D(T))가 기판에서의 도펀트의 확산 계수를 표시하고, Co#180#가 약 10-6 Ω-cm2 이하의 Rc를 산출하는 상기 물질 영역/기판 인터페이스에 인접한 원하는 도펀트 농도를 나타낸다면, C가 공식

The repetitive (iterative) technology which it is to select the temperature-time profile used for the substrate heating in order to realize the source/drain depth in which the invention moreover desires, is contained. Here, it assumes that the thickness is known as the doping level of the substrate, and the NA area or the territory of material is designated. Moreover, three conditions was satisfied and with it is greater than the Co realizing the Rc in which the dopant concentration within the substrate adjacent to the territory of material / plate interface desires as the result of the substrate heating but is the necessary (it is known) minimum value or it is the same it assumes. First, moreover, it assumes that it is used for simplicity only the temperature T which is obligatorily greater than the Tmin or thes same for the heating process. C is the equation the desired dopant concentration in which the Co´ is adjacent to the territory of material / plate interface producing the Rc less than about 10 - 6 Ω- cm 2 is shown the variable X´ indicates the perpendicular position of the point within the source about the bottom surface (it is diffused) of the territory of material or the drain and T shows time and D (=D(T)) indicates the diffusion coefficient of the dopant at the substrate.

에 의해 잘 근사된다는 것이 결정되었다. 여기서 erfc는 상보에러 함수이다. X#180#가 X(상기 물질 영역의 바닥에 비교한 소스나 드레인의 원하는 깊이)와 같아지는 소스나 드레인의 바닥에서, C(X, Γ)는 필수적으로 NA와 동일하며, 그러므로 공식(1)로 부터,

It was determined that it was due to and the well was approximated. Here, the erfc is the complementary error function. From the equation (1) the obligatorily C (X, Γ) is identical with NA in the bottom surface of the source in which the X´ becomes same with X (the desired depth of the source compared in the bottom surface of the territory of material or the drain) or the drain.

이다.

It is.

공식(2)의 오른쪽이 공지된 양이기 때문에, 공식(2)에서 상보에러 함수의 독립변수(argument)가 알려지며, 즉 예를 들어 erfc 함수의 테이블로 부터 쉽게 결정된다(엠.아브라모위쯔와 아이.에디.세건에 의해 출판된 #8220#수학적 함수의 핸드북 #8221#에서 왈터 고쯔찌를 참조하라). 그러나 X는 알려져 있다. 또한 D는 필수적으로 온도의 함수이며, 단일 온도만이 가열 절차동안에 사용되기 때문에 D도 또한 낮게되며, 단일 온도 T에 대응하는 D의 값은 예를 들어, 테이블(제이.씨.씨.쯔아이의 상기 참조 논문을 참조)로 부터 쉽게 결정된다. 그러므로, erfc 함수의 독립 변수의 값이 알려지고, X와 D의 값이 알려졌기 때문에 Γ(가열시간)의 값은 쉽게 추론할 수 있다. 만일(제어 샘플의 바닥과 비교하여) 소스나 드레인의 생성 깊이가(예를 들어 SIMS 기술을 통해 결정될때) 원하는 깊이가 아니면 가열 시간 및 가열온도가 변경된다.

The M(***. Larmor and I the right of the equation (2) is known amount is determined from in other words, for example, the table of the erfc function it is the amount in which and therefore the independent variable (argument) of the complementary error function is known in the equation (2). Eddy. In the handbook " published by the force gun of the " mathematical function, but X is known because of referring to the Walter Gozdz fishing float. Moreover, the value of the D, which corresponds to the monothermal T the obligatorily D is the function of the temperature and D is low because it is used only the monothermal for the heating process. For example, the table (J. It is easily the reference paper of the CC. I determined from the reference). Therefore, the value of the independent variable of the erfc function becomes known and the value of Γ (the heating time) easily can reason because the value of D and X became known. If it is not depth in which the production depth (it is determined through the SIMS technology for example) of the if (it compares with the bottom surface of the control sample) source or the drain desires, the heating time and heating temperature are changed.

만일 대응하는 다수의 시간 간격 Γ1, Γ2…Γn에 대해 다수의 가열온도 T1, T2…Tn을 사용하는 것이 필요하다면, C는

C it is requisite about the multiple time interval Γ 1 s which the if corresponds, and Γ 2 … Γ n to use the multiple heating temperature T 1 s, and T 2 … T n .

의해 잘 근사된다. 여기서 D1, D2, …Dn는 온도 T1, T2, …Tn

It is according to and it is approximated to the well.

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에서 기판내의 도펀트의 확산 계수를 표시한다. 그러므로, C가 NA와 동일한, 즉 X#180#=X인 소스나 드레인의 바닥에서,

Here, in D 1 , D 2 , … D n is the temperature T 1 , T 2 , and … T n , the diffusion coefficient of the dopant with in the substrate is indicated. Therefore, in the bottom surface of the source in which C is identical with NA an d which is in other words, the X′=X or the drain

이된다. 전술한 바와 같이, 공식(4)의 오른쪽은 알려져 있고, 그러므로 공식(4)에서 erfc 함수의 독립변수는 쉽게 결정된다. 또한 X는 알려져 있고, T1, T2, …Tn가 지정된 것으로 가정하면 D1, D2, …Dn도 또한 쉽게 결정된다. 그러므로 공식(4)를 만족하는 Γ1, Γ2, …Γn의 값이 쉽게 선택된다. 만일 Γ가 원하는 소스/드레인 깊이를 산출하지 못하면, 반복적 절차에 따라, Γ 및 T가 변경된다.

It is ***. As described above, the right of the equation (4) is known and the independent variable of the erfc function is therefore easily determined on the equation (4). Moreover, X is known and if it assumes th at T 1 , T 2 , and … T n are designated, D 1 , D 2 , an d … D n are moreover easily determined. Therefore, Γ 1 , satisfied the equation (4) Γ 2 , and the value of … Γ n are easily selected. If the source/drain depth in whic h Γ desires is unable to be produced , Γ and T are acco rding to procedure changed.

상기 반복적 기술을 이용하여, 1#215#1016cm-3의 도핑레벨을 가진 P형 실리콘 기판을 가열하는 단계와 800℃의 온도로 130분 동안 상기 비소가 주입된 코발트 실리사이드 영역을 지탱하는 단계는 0.15㎛와 동일한 깊이(코발트 실리사이드의 상부 표면에 대하여)를 가진 소스나 드레인을 산출한다는 것이 알려졌다. 유사하게, 1#215#1017cm-3의 도핑 레벨을 가진 n형 실리콘 기판을 가열하는 단계와 124분 동안 800℃의 온도로 상기 붕소가 주입된 티타늄 실리사이드 영역을 지탱하는 단계는 0.2㎛와 동일한 깊이(티타늄 실리사이드의 상부 표면에 대하여)를 가진 소스나 드레인을 산출한다는 것도 알려져 있다.

The source having the depth (about the top surface of the cobalt silicide) in which the step and the step of su pporting the cobalt silicide domain in which arsenic was injected as the temperature of 800℃ for 130 minutes w ere identical with 0.15㎛ of heating up the P-sub havin g the doping level of 1× 10 16 cm - 3 or the to produc e the drain thing was known using the iterative techniq ue. Similarly, it is known that the step and the step of supporting the titanium silicide region in which boron is injected to the temperature of 800℃ for 124 minutes pr oduce the source or the drain having the same depth (about the top surface of the titanium silicide) as 0.2㎛ of heating up the n-type silicon substrate having the d oping level of 1× 10 17 cm - 3 .

본 발명의 보다 완전한 이해를 위한 교육학적 도움으로서 n채널 MOS IC 및 CMOS(상보 금속 산화물 반도체) IC의 제조를 위한 본 발명의 소자 제조 방법의 용융이 이하에서 기술되게 된다(간략하게 하기 위해 완전히 통상적인 몇몇 단계는 생략된다).

Hereinafter the melting of the element manufacture method of the invention for the manufacture of the N-channel Metal Oxide Semiconductor IC and CMOS (com plementary metal oxide semiconductor) IC are describe d as the pedagogy help for the complete understanding of the invention (brevis breviterLat, it is to do and the normal some step is completely omitted).

제1도 내지 제8도를 참조하면, 예를 들어 종래의 산화 기술을 이용하여, P형 실리콘 기판(10)상에 FOX(20)(비교적 두꺼운 SiO2층)을 형성함으로써 본 발명의 한 실시예에 따라 n채널 MOS IC가 제조된다. 기판(10)에서 P형 도펀트의 도핑 레벨은 예를 들어 1#215#1015cm-3이다. 또한 FOX(20)의 두께는 예를 들어 0.35㎛이다.

The first the N-channel Metal Oxide Semiconductor IC is manufactured with reference to the inland eighth dra wing using for example, the conventional oxidation tech nology according to one embodiment of the invention b y forming the FOX (20) (the SiO 2 layer which is relativ ely thick) on the P-sub (10). In the substrate (10), the doping level of the p-dopant is for example, 1× 10 15 c m - 3 . Moreover, the thickness of the FOX (20) is for example, 0.35㎛.

이제 FOX(20)는 MOSFET가 형성될, 여기서는 GASAD (gate-and-source-and-drain)으로 불리는 기판 표면의 영역(30)을 노출시키기 위해 예를 들어, 석판 인쇄술 및 반응 이온 에칭(RIE)기술을 이용하여 선택적으로 에칭된다. 예를 들어, 0.15㎛의 두께를 가진 GOX(40)(비교적 얇은 SiO2층)는 예를 들어 종래의 산화 기술을 이용하여 GASAD 영역(30)의 표면상에 형성된다.

Now, it is etched at the selectively using for example, lithography and reactive ion etching (RIE) technology t he domain (30) of the substrate surface called here, th e GASAD (gate-and-source-and-drain) in which the FO X (20) MOSFET is formed is exposed. For example, the GOX (40) (the SiO 2 layer which is relatively thin) havin g the thickness of 0.15㎛ is formed on the surface of th e GASAD domain (30) using for example, the conventio nal oxidation technology.

MOSFET의 게이트 전극은 GASAD 영역(30) 뿐만 아니라 FOX(20)상에도 다결정 실리콘(이후 폴리실리콘)의 층(50)을 초기에 침착시킴으로써 형성된다. 침착은 예를 들어 종래의 저

The gate electrode of MOSFET is formed by sinking the layer (50) of the poly-crystal silicon (then, the poly-sili con) into the initial on not only the GASAD domain (30)

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압 화학적 증기 침착(LPCVD) 기술을 이용하여 실행되며, 침착된 폴리실리콘의 두께는 예를 들어 0.3㎛가 된다. 침착후에, 폴리실리콘은 예를 들어 1#215#1015cm-2의 주입량(implant dose)과 80kev의 이온 에너지를 이용하여, 폴리실리콘에 비소와 같은 n형 도펀트를 주입함으로써 전기적 전도성으로 만들어진다.

but also the FOX (20). The deposition is performed using for example, the conventional low pressure chemical vapour deposition (LPCVD) technology and for example, 0.3㎛ becomes the deposited thickness of the poly-silicon. The poly-silicon is made as the electrical conductivity after the deposition using for example, the injection amount (implant dose) of 1× 10 15 cm - 2 and ion energy of 80kev by injecting the n-type dopant like arsenic into the poly-silicon.

침착된 전기적 전도성의 폴리실리콘(50)은 이제 제4도에 도시된 바와 같이, 간각이 GASAD 영역(30)위에 있는 폴리실리콘 구조를 형성하기 위해 종래의 RIE 기술을 이용하여 패턴된다. 상기 구조의 측벽은 대응하는 GASAD 영역이 표면에 직각인 면에 비하여 각도 #945#(제4도 참조)를 형성하는데, 이것은 +15#176# 보다 작거나 같으며, 0도가 되는것이 바람직하다(제4도에 도시한 폴리실리콘 구조의 좌측벽에 대해, 각도 X는 수직으로 부터 시계 방향으로 측정될때 포지티브가 된다. 한편 우측벽에 대해서는 이 각도가 반시계 방향으로 측정될때 포지티브다 된다). 측벽 각도에 관한 관계는 이하에서 논의되는 바와 같이 실리콘 이산화물 측벽 스페이서(55)의 형성과 관련하여 매우 중요하다.

So that the liver angle form the polysilicon structure of having on the GASAD domain (30), the deposited poly-silicon (50) of the electrical conductivity is patterned on the now as shown in Figure 4 using the conventional RIE technology. The GASAD domain in which the sidewall of the structure corresponds forms the angle α (the fourth is the reference) on the surface in comparison with the side which is the right angle. This is smaller than the +15° or it is the same and when the angle X is clockwise measured from the perpendicularity, it is positive about the left side wall of the polysilicon structure of showing in the be desirable or figure the fourth that figure 0 is. In the meantime, as when this angle is counterclockwise measured about the right side wall, it becomes as positive hereinafter the relation about the side wall angle been discussed it is important in connection with the formation of the silicon dioxide side wall spacer (55).

이하에서 논의되는 소자 제조 절차는 결과적으로 금속 실리사이드 영역을 각각의 MOSFET의 소스, 드레인 및 게이트 전극으로 병합시킨다. 게이트 전극에서의 금속실리사이드 영역과 소스 및 드레인에서의 금속 실리사이드 영역 사이의 전기적 접촉을 배제하기 위해, 각 게이트 전극의 폴리실리콘 부분은 각 폴리실리콘 측벽을 커버링하는 실리콘 이산화물 측벽 스페이서(55)(제4도 참조)를 포함하도록 형성된다. 이것은 예를 들어 FOX의 상부 및 측벽 표면과 GASAD 영역의 노출된 표면상에 뿐만 아니라 폴리실리콘 구조의 상부 및 측벽 표면상에 테트라에틸오소실리케이트(TEOS)와 같은 실리콘과 산소 함유 물질의 층을 침착 시킴으로써 실현된다. TEOS의 침착은 예를 들어 종래의 LPCVD 기술을 이용하여 쉽게 실행되며, TEOS의 두께는 예를 들어 0.1㎛이다. 침착이 이루어진 후에, TEOS는 TEOS를 농후하게 하고 효과적으로 실리콘 이산화물과 같은 물질로 변환시키기 위해 스팀 대기에서 20분동안 900℃로 가열되는 것이 바람직하다. 이때 TEOS는 폴리실리콘 구조의 상부 표면뿐만 아니라 FOX 및 GASAD 표면으로 부터 TEOS를 제거하기 위해 예를 들어 CHF3 및 O2의 에천트(etchant) 환경에서 예를 들어 RIE를 이용하여 이동방향으로 에칭된다. 이 에칭 절차 이후에, 예를 들어 0.06㎛의 두께를 가진 농후하게 된 TEOS의 층이 측벽 각도가 전술한 요구를 만족하도록 제공되어 폴리실리콘 구조의 측벽상에 남아 있게 된다.

Hereinafter, the consequently the device manufacture procedure of being discussed incorporates the metal silicide domain to the source of each MOSFET, and the drain and gate electrode. In order that the electrical contact of the metal silicide between area at the metal silicide domain at the gate electrode and source and drain are excluded drain are formed in order to include the silicon dioxide side wall spacer (55) (the fourth is the reference) in which the polysilicon part of each gate electrode covers each polysilicon side wall. By sinking the layer of the silicone like the taraethylothosilicate (TEOS) and oxygen containing material on the upper portion and side wall surface of the polysilicon structure besides this is realized on for example, the exposed surface of the upper portion of FOX and side wall surface and GASAD domain. The deposition of TEOS is easily performed using for example, the conventional LPCVD technology and the thickness of TEOS is for example, 0.1㎛. After the deposition is made it is the be desirable that the material is heated in the steam atmosphere for 20 minutes by 900℃ so that it make TEOS strong and TEOS effectively change to the material like the silicon dioxide. Then, it is etched at the moving direction in for example, the etchant environment of O 2 and CHF 3 using for example, RIE so that TEOS remove TEOS from not only the top surface of the polysilicon structure but also FOX and GASAD surface. The layer of thick TEOS having for example, the thickness of 0.06㎛ is provided in order to be satisfied the demand in which the side wall angle describes in the above and , the layer remains after this etching procedure on the sidewall of the polysilicon structure.

측벽 스페이서(55)의 형성 이후에, 티타늄과 같은 금속 실리사이드를 형성하기 위해 실리콘과 반응할 수 있는 금속층이 각 폴리실리콘 구조의 상부 표면과, 측벽 스페이서(55)의 표면과, G

In order to form the metal silicide like titanium, the metallic layer reacting to the silicone is deposited after the formation of the side wall spacer (55) on the upper

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ASAD 영역의 노출된 표면(소스와 드레인 형성될 곳) 및 FOX (20)의 상부 및 측벽 표면상에 침착된다. 이 침착은 예를 들어, 종래의 스퍼터링 기술을 이용하여 실현되며, 침착된 티타늄의 두께는 예를 들어, 0.1㎛이다. 침착 이후에, 티타늄으로 커버된 실리콘 기판은 종래의 RTA 기술을 이용하여 약 1분동안 약 600℃의 온도로 질소(N2) 환경에서 가열된다. 티타늄 층이 실리콘과 접촉하는 곳, 즉 GASAD 영역의 표면 뿐만 아니라 폴리실리콘 구조의 상부 표면상에서, 이 가열 절차는 TiN, Ti 및 Ti siy의 연속한 층의 형성을 초래하게 되는데, 여기서 y#8804# 2이다. 대조적으로, 침착된 티타늄 층이 실리콘 이산화물과 접촉하는 곳, 즉 FOX 및 측벽 스페이서의 표면에서, 상기 가열절차는 TiN 및 Ti의 연속한 층의 형성을 야기하게 된다.

portion of exposed surface (the place formed with sour ce and drain) of the surface of the top surface of each polysilicon structure and side wall spacer (55) and GAS AD domain and FOX (20) and side wall surface. This de position is realized using for example, the conventional sputtering technique and the deposited thickness of th e titanium is for example, 0.1㎛. The temperature of ab out 600℃ is heated by the silicon substrate covered wi th titanium after the deposition using the conventional RTA technology for about 1 minute in the nitrogen (N(S B)2(/SB)) environment. This heating process causes th e TiN, and the formation of the consecutive layer of th e Ti and Tisiy on the place, where the titanium layer co ntacts with the silicone in other words, the top surface of not only the surface of the GASAD domain but also t he polysilicon structure. It the here is the y≤2. Contras tively, the heating process causes the formation of the consecutive layer of the TiN and Ti on the surface of t he place, where the deposited titanium layer contacts the silicon dioxide in other words, FOX and side wall sp acer.

TiSiy(y#8804#2)가 아닌 TiN 및 Ti층은 90℃의 온도로 가열된 H2SO4 : H2O2(1 : 1)의 용액과 같은 선택적 습식 에천트를 사용하여 에칭된다. 폴리실리콘 구조의 상부 표면과 GASA D 영역의 노출된 표면을 커버링하는 남아있는 TiSiy(y#8804 #2)는 이제 종래의 RTA 기술을 이용하여 예를 들어 20초동안 800℃의 온도로 질소 환경에서 TiSiy로 커버된 실리콘 기판을 가열함으로써(폴리실리콘 구조 및 실리콘 기판에서) 아래에 있는 실리콘과 반응하게 된다. 그 결과 TiSi2 함유 영역(60, 70)(제5도 참조)이 폴리실리콘 주조의 반대측에 형성되어 수직으로 정렬되고 TiSi2 함유 영역(80)은 폴리실리콘 구조의 정상부에 형성되는데, 이와 같은 영역은 약 0.08㎛의 동일한 TiSi2의 두께를 갖는다(각각의 이와 같은 영역은 또한 통상적으로 약 0.01㎛의 두께를 갖고 TiSi2위에 있는 TiN층(양호한 전기적 전도체)을 포함한다).

The TiN and the Ti layer which is not TiSiy (y≤2) are etched using the optional wet etchant like the service of H 2 SO 4 : H 2 O 2 (1 : 1) which the temperature of 90℃ is heated. By the nitrogen ambient heating the sili con substrate covered with the TiSiy using the conven tional RTA technology for for example, 20 second with the temperature of 800℃ (in the polysilicon structure a nd silicon substrate) the TiSiy (y≤2) which covers the top surface of the polysilicon structure and the expose d surface of the GASAD domain remaining now reacts w ith the silicone which is beneath have. Consequently, t he TiSi 2 containing domain (60, 70) (the fifth is the re ference) is formed in the opposite side of the poly-silic on casting and it is arranged in the perpendicularly and the TiSi 2 containing domain (80) is formed in the top o f the polysilicon structure. This kind of domain has the thickness of the same TiSi 2 of about 0.08㎛ (generally the domain like each this moreover has the thickness o f about 0.01㎛ and the TiN layer (the good electrically conducting body) having on the TiSi 2 is included).

n+형 소스 및 드레인을 형성하기 위해, 하나 혹은 그 이상의 도펀트, 즉 비소 이온이나 인 이온이 TiSi2 함유 영역(60, 70)내로 주입된다. 주입량은 물론 전술한 세가지 조건을 만족하도록 선택된다. 또한 이온 에너지도 거의 모든 이온이 영역(60, 70)내로 주입되고 아래에 놓인 실리콘내로는 주입되지 않도록 선택된다.

In order that the n + type source and drain are formed one or the dopant described in the above, in other wor ds, the arsenic ion or the phosphor ion is injected withi n TiSi 2 containing domains (60, 70). It is selected in o rder to be satisfied above-described three conditions a s well as the injection amount. Moreover, the all ions ar e injected within domains (60, 70) and the ion energy i s beneath puts silicone is selected in order not to be in jected within the silicone in which.

이온 주입 이후에, 인터레벨 유전체(90)(제6도 참조)가 기판상에 침착된다. 이와 같은 유용한 인터레벨 유전체는 예를 들어, 0.2㎛의 두께를 가진 도핑되지 않은 TEOS와 약 0.8㎛의 두께를 가진 인으로 도핑된 TEOS의 잇따른 층을 포함한다.

The interlevel dielectric (90) (the sixth is the reference) is deposited after the ion implantation on th e substrate. This kind of the interlevel dielectric which i s useful includes undoped TEOS having for example, th e thickness of 0.2㎛ and the layer following of TEOS do ped to the phosphorus having the thickness of about 0.8㎛.

침착된 인터레벨 유전체(9)의 상부 표면은 통상적으로 비평면이다(일반적으로 후속 처리동안 바람직하지 못하다). 인터레벨 유전체(90)를 흐르도록 유도하고 그래서 표면 평면성을 실현하고 또한 티타늄 실리사이드로 커버된 소스 및 드레인(100, 1

The generally the deposited top surface of the interlevel dielectric (9) is the non-planar (generally, it c annot for the next treatment with the be desirable pap er). In order that it induces in order to flow the interlev

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10)(제7도 참조)을 형성하도록 TiSi2 함유 영역(60, 70)으로부터 아래에 놓인 실리콘내로 주입 도펀트를 확산시키기 위해, 기판이 가열된다. 전술한 바와 같이, 가열 절차의 온도-시간 프로필은 약 0.2㎛ 이하의 깊이를 가진 소스 및 드레인을 산출하도록 선택된다.

el dielectric (90) and , so the injection dopant is diffused within the silicone which is beneath puts from TiSi 2 containing domains (60, 70) in order to realize the surface planarity and form the source and the covered drain (100, 110) (the seventh is the reference) into moreover, the titanium silicide the substrate is heated. As described above, the source are selected in order to produce the source and the drain in which the temperature-time profile of the heating process has the depth less than about 0.2㎛.

소스 및 드레인 형성 이후에, 인터레벨 유전체는 소스와 드레인 및 게이트 전극으로 경유 구멍을 개방하도록(종래 기술을 이용하여) 패턴된다. 이제 물질층(120, 130, 140)(제8도 참조)이 기판상에 침착되는데 그래서, 알루미늄과 실리콘의(바람직하지 못한) 상호 확산에 대한 장벽으로서 작동하도록 소스와 드레인 및 게이트 전극으로 각각 뻗은 경유 구멍내로 침착되게 된다. 이들 층은 예를 들어, 10퍼센트(중량으로)의 티타늄과 90퍼센트의 텅스텐 합성물을 포함하며 예를 들어 0.1㎛의 두께를 갖는다.

It is patterned after the source and drain formation so that the interlevel dielectric opens the via hole to source and drain and gate electrode (using the prior art). Now, the material layer (120, 130, 140) (the eighth is the reference) is deposited on the substrate but it is deposited to the so within the via hole spreading toward source and drain and gate electrode in order to operate as the obstacle about the interdiffusion of aluminum and silicone (it cannot with the be desirable paper). These layers has for example, the titanium of 10 percent (to the weight) and for example, the thickness of 0.1㎛ the tungsten synthesized material of 90 percent is included.

이제, 예를 들어 1㎛의 두께를 가진 알루미늄 층이 경유 구멍내의 장벽층(120, 130, 140) 뿐만 아니라 인터레벨 유전체(90) 상에도 참착된다. 침착후 계속해서, 금속 접촉 패드에서 중단되는 상호 접속 알루미늄 런너(runner)(150, 160, 170)를 형성하기 위해 종래의 기술을 이용하여 알루미늄층이 패턴된다.

Now, for example, the aluminum layer having the thickness of 1㎛ is settled down on not only barriers (120, 130, 140) within the via hole but also the interlevel dielectric (90). In order to form interconnection aluminum runner (runner) (150, 160, 170) and then interrupted in the metal contact pad after the deposition, the aluminum layer is patterned using the conventional technology.

n채널 MOS IC는 통상적인 일련의 단계를 통해 완성되는데, 통상적으로 습기 및 기계적 손상에 대비한 장벽을 형성하기 위해 IC상에 실리콘 질화물 층을 침착하는 단계를 포함한다.

The N-channel Metal Oxide Semiconductor IC comprises the step of being compose the silicon nitride layer on IC the obstacle which generally compares for moisture and mechanical damage is formed it is completed through normal a series of step.

이제 제9도 내지 제17도를 참조하면, 종래기술을 이용하여 P+형 실리콘 기판(200)상에 P형 실리콘층(210)(제9도 참조)을 에피택셜 성장시킴으로써 본 발명의 제2실시예에 따라 CMOS IC가 제조된다. 기판(200)의 도핑 레벨은 예를 들어 1018cm-3이며, 에피택셜 성장된 층(210)의 도핑 레벨은 예를 들어 1015cm-2이다. 또한, 에피택셜 성장된 층(210)의 두께는 예를 들어 5㎛이다.

Referring now to the ninth is the inland seventeenth drawing, according to the second preferred embodiment of the present invention, the CMOS IC is manufactured by making the P-type silicon layer (210) (the ninth is the reference) using the prior art on the P+ type silicon substrate (200) with epitaxial growth. The doping level of the substrate (200), for example, the doping level of 10 18 cm - 3 , the layer (210) which epitaxially grows is for example, 10 15 cm - 2 . Moreover, the thickness of the layer (210) which epitaxially grows is for example, 5㎛.

1984년 3월 13일 엘.씨.파릴로와 알.에스.페인에게 특허된 미합중국 제 4,435,896호에 기술된 바와 같은 소위 2중 튜브 공정을 이용하여 에피택셜 성장층(210)에 인접한 n튜브 및 P튜브(240, 250)가 형성된다. 즉 예를 들어 0.1㎛의 두께를 가진

1984 year March 13 LC. Parrillo. and RS. The n tube and P tubes (240, 250) adjacent to the Epitaxial growth layer (210) among the patented so-called 2 like being described in US4,435,896 A using the tube processing

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실리콘 질화물층(220)(제10도 참조)이 통상적인 침착 기술을 이용하여 상기 층(210)의 상부 표면에 처음에 침착된다. 종래의 석판 인쇄술 및 RIE 기술이 실리콘 질화물층(220)의 일부분을 제거하고, 그러므로 n튜브(240)가 될 실리콘 표면을 노출시키는데 이용된다. 이제 도우너 이온, 즉 인 이온과 비소 이온이 상기 층(210)(층(210)의 노출되지 않는 실리콘을 주입으로부터 차폐하도록 작용하는 잔여 실리콘 질화물층)의 노출된 실리콘 표면내로 주입되는데, 인과 비소 이온 모두에 대한 주입량 및 에너지는 예를 들어 각각 2#215#1012cm-2와 100keV이다. 다음에, n튜브의 표면상에 약 0.4㎛의 두께를 가진 실리콘 이산화물의 층(230)(제10도 참조)을 형성하기 위해, 예를 들어 950℃의 온도로 140분의 대응하는 가열 시간동안 스팀 함유 환경에서 실리콘 기판이 가열된다.

are formed to the pain. That is, for example, it at first time is sunk in the top surface of the layer (210) using the deposition technology in which the silicon nitride layer (220) (the tenth is the reference) having the thickness of 0.1㎛ is normal. The conventional lithography and RIE technology remove one part of the silicon nitride layer (220) and it is therefore used to expose the surface of silicon in which the n tube (240) is. Now, the donor ion, in other words, the phosphor ion and arsenic ion are injected within the exposed surface of silicon of the layer (210) (the residual silicon nitride layer which acts in order to shield the silicone which is not exposed of the layer (210) from injection). For example the injection amount about the phosphorus and arsenic ion every one and energy is 2× 10 12 cm - 2 and 100keV. Next, in order that the layer (230) (the tenth is the reference) of the silicon dioxide having the thickness of about 0.4㎛ is formed on the surface of the n tube the silicon substrate is heated by for example, the temperature of 950℃ for the heating time to correspond to of 140 minutes in the steam containing environment.

이제 실리콘 질화물의 층(220)이 뜨거운 H3Po4와 같은 습식 에천트로 에칭되고, 액셉터 이온 즉 붕소 이온이 P튜브(250)가 될 노출된 실리콘 표면으로 주입된다(실리콘 이산화물층(230)은 n튜브(240)을 주입으로 부터 차폐한다). 만일 붕소 이온이 사용되면, 주입량 및 대응하는 주입 에너지는 예를 들어 각각 2#215#1012cm-2 및 50keV이다. 다음에, 실리콘 기판은 붕소 이온 및 인 이온을 약 2㎛의 깊이까지 상기 층(210) 내로 확산시켜 n튜브(240) 및 p튜브(250)(제11도 참조) 모두를 형성시키기 위해, 예를 들어 1150℃의 온도로 120분의 대응하는 시간 주기동안 질소(N2) 환경에서 가열된다.

Now, it is etched at the wet etchant like H 3 Po 4 in which the layer (220) of the silicon nitride is hot and if it is injected to the exposed surface of silicon (the silicon dioxide layer (230) shields the n tube (240) from injection) in which for the acceptor ion, in other words, the boron ion, P tube (250) is the boron ion is used , for example the implant energy corresponding with the injection amount is 2× 10 12 cm - 2 and 50keV. Next, in order that the boron ion and phosphor ion are diffused to the depth of about 2㎛ within the layer (210) and the silicon substrate forms both the n tube (240) and p tube (250) (the eleventh is the reference) for example, the temperature of 1150℃ is heated for the time period corresponding to of 120 minutes in the nitrogen (N(SB)2(/SB)) environment.

n튜브(240)를 커버링하는 실리콘 이산화물층(230)은 H2D : HF(7 : 1)와 같은 습식 에천트로 에칭된다. 이제 CMOS IC에서 FOX로서 작용하는 예를 들어 0.4㎛의 두께를 가진 실리콘 이산화물의 비교적 두꺼운 층(260)(제12도 참조)이 에피택셜 성장층(210)의 (이제 완전히 노출된) 상부 표면상에 형성된다. 이것을 예를 들어 850℃의 온도로 25분의 대응하는 가열 시간동은 고압스팀 함유 대기, 즉 25기압의 압력을 나타내는 스팀 함유 대기에서 실리콘 기판을 가열함으로써 실현된다.

The silicon dioxide layer (230) covering the n tube (240) is etched at the wet etchant like H 2 D : HF (7 : 1). Now, in the CMOS IC, the layer (260) (the twelfth is the reference) which is relatively thick of the silicon dioxide having the thickness of 0.4㎛ acting as FOX is formed on (it is now completely exposed) top surface of the Epitaxial growth layer (210). Since the steam containing atmosphere showing the high pressure steam containing atmosphere, in other words, the pressure of 25 atmospheric pressure the heating time copper of 25 minutes corresponding to heats the silicon substrate with for example, the temperature of 850℃ it is this realized.

실리콘 이산화물의 비교적 두꺼운 층(260)은, n채널 MOSFET가 형성된 P튜브(250)과 표면상의 GASAD 영역(270)을 노출시키고, P채널 MOSFET가 형성될 n튜브(240)의 표면상의 GASAD 영역(400)을 노출시키기 위해 종래의 기술을 이용하여 패턴된다. 다음에, 실리콘 기판은 GASAD 영역(270)의 표면상에 실리콘 이산화물의 층(280)을 형성하고 GASAD 영역(400)의 표면상에 실리콘 이산화물의 층(410)을 형성하기 위해 900℃의 온도로 27분의 대응하는 시간 주기동안 가열되게 되는데, 이들 층(280, 410)은 약 0.0125㎛의 두께를 가지며, n채널 및 P채널 MOSFET의 GOX로서 작용한다.

The layer (260) which is relatively thick of the silicon dioxide exposes the GASAD domain (270) on P tube (250) and the surface in which the n channel type MOSFET is formed and it is patterned using the conventional technology it exposes the GASAD domain (400) on the surface of the n tube (240) in which the P-ch MOSFET is formed. Next, in order to the silicon substrate form the layer (280) of the silicon dioxide on the surface of the GASAD domain (270) and form the layer (410) of the silicon dioxide on the surface of the GASAD domain (400), the surface is heated by the temperature of 900℃ for the time period corresponding to of 27 minutes. These layers (280, 410) have the thickness of about 0.012

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5㎛ and the temperature acts as GOX of the P-ch MOS FET and n channel.

n채널 및 P채널 MOSFET의 게이트 전극은 처음에, FOX(260) 뿐만 아니라 GASAD 영역(270, 400)상에 예를 들어 0.3㎛의 두께를 가진 폴리실리콘 층을 침착시킴으로써 형성되며, 포토레지스트가 기판상에 침착되어 n튜브(240)에 대응하는 기판 표면을 노출시키기 위해 패턴된다. 이제 액셉터 이온, 즉 붕소 이온이 n튜브 위에 놓인 폴리실리콘내로 주입되는데 레지스트는 P튜브 위에 놓인 폴리실리콘을 주입으로 부터 차폐한다. 주입량 및 주입 에너지는 예를 들어, 각각 1#215#1015cm-2와 30keV이다. 이 레지스트는 벗겨지고, 제2레지스트가 기판상에 침착되어 P튜브(250)에 대응하는 기판 표면을 노출시키기 위해 패턴된다. 이제 도우너 이온, 즉 비소 이온이 P튜브(250) 위에 놓인 폴리실리콘내로 주입되는데, 제2레지스트는 n튜브(240) 위에 놓인 폴리실리콘을 제2주입으로 부터 차폐한다. 도우너 이온에 대응하는 주입량 및 주입 에너지는 예를 들어, 각각 1#215#1015cm-2와 30keV이다. 이제 제2레지스트는 벗겨지고, 기판은, 예를 들어 900℃의 온도로 30분의 대응하는 시간 주기동안 질소(N2) 디기에서 가열된다. 결과적으로, 주입된 도펀트가 폴리실리콘내로 확산되어, n튜브(240)위에 놓인 폴리실리콘은 P형 전도성이 되고, P튜브(250)위에 놓인 폴리실리콘은 n형 전도성이 된다.

By sinking the polysilicon layer having for example, the thickness of 0.3㎛ on not only the FOX (260) but also G ASAD domains (270, 400) at first time the gate electro de of the P-ch MOSFET and n channel is formed and so that the photoresist is deposited on the substrate and the substrate surface corresponding to the n tube (24 0) be exposed, it is patterned. Now, it is injected withi n the poly-silicon in which the acceptor ion, in other w ords, the boron ion is puts on the n tube but the poly- silicon in which the resist is puts on P tube is shielded f rom injection. For example the injection amount and im plant energy are 1× 10 15 cm - 2 and 30keV. This resis t comes off and so that the second resist is deposited on the substrate and the substrate surface correspondi ng to P tube (250) be exposed, it is patterned. Now, th e donor ion, in other words, the arsenic ion is injected within the poly-silicon which is puts on P tube (250). T he poly-silicon in which the second resist is puts on th e n tube (240) is shielded from the second injection. Fo r example the injection amount and the implant energy corresponding to the donor ion are 1× 10 15 cm - 2 an d 30keV. Now, the second resist comes off and the sub strate is heated by for example, the temperature of 90 0℃ for the time period corresponding to of 30 minutes i n the nitrogen (N(SB)2(/SB)) di. Consequently, the inje cted dopant is diffused within the poly-silicon and in th e poly-silicon which is puts on the n tube (240), the p- type conductivity is and in the poly-silicon which is put s on P tube (250), the n-type conductivity is.

이제, 침착되고 주입된 폴리실리콘(도한 아래에 놓인 비교적 얇은 실리콘 이산화물층(280, 410)로 마찬가지)이 각각 GAS AD 영역(270, 400)위에 놓인 폴리실리콘 구조(290, 420)(제13도 참조)를 형성하기 위해 전술한 바와 같이 패턴된다. 이 폴리실리콘 구조의 측벽은 위에서 논의된 요구에 부합해야 한다. 또한 전술한 바와 같이 실리콘 이산화물 측벽 스페이서(295, 425)가 각각 폴리실리콘 구조(290, 420)상에 형성된다.

Now, it is patterned on as described above the polysilicon structure (290, 420) (the thirteenth is the r eference) in which poly-silicons (silicon dioxide layers (280, 410) which *** are beneath put and are relativel y thin the likeness) that deposited are injected are put on GASAD domains (270, 400) is formed. It has to coin cide with the demand in which the sidewall of this poly silicon structure is discussed before the upper part. Mo reover, as described above, silicon dioxide side wall spa cers (295, 425) are formed on polysilicon structures (2 90, 420).

이제 코발트와 같이 금속 실리사이드를 형성 하기 위해 실리콘과 반응할 수 있는 금속층이 폴리실리콘구조(290, 410)의 상부 표면과, 측벽 스페이서(295, 425)의 표면과, GASAD 영역의 노출된 표면(소스와 드레인의 형성될 곳)과, FOX(260)의 상부 및 측벽 표면상에 침착된다. 침착된 코발트의 두께는 예를 들어 0.02㎛이다. 침착 이후에, 코발트로 커버된 기판은 450℃의 온도로 90분의 대응하는 시간 주기동안, 감소대기, 즉 대기에서 가열된다. 코발트가 실리콘과 접촉하는 곳, 즉 GASAD 영역과 노출된 표면뿐만 아니라 폴리실리콘 구조의 상부 표면상에서, 이 가열 절차는 코발트 모노실리사이드(CoSi)를 형성하게 된다. 모든 다른 영역에 있어서, 코발트는 반응하지 않은채로 남아 있다. 반응하지 않은 코발트(CoSi가 아님)는 이제 H3Po4 : CH2COOH : HNO3 : H2O(16 : 2 : 1 : 1)과 같은 선택적 습식 에천트를 사용하여 벗겨진다. 다음에, 기판은 예를 들어 700℃의 온도로 30분의 대응하는 시간 주기동안 불활성 대기, 즉 아르곤(Ar) 대기에서 두번째 가열된다. 이 제2가열은 약 0.07㎛의 두께를 가진 코발트 다이실리사이드(CoSi2)를 형성하기 위해 CoSi를 아래에 놓인 실리콘과 반응하도록 한다. 그러므로, CoSi2 함유 영역(300, 310)(제14도 참조)이 각각

Now, the metal silicide is respected like cobalt to do with formation and the metallic layer reacting to the sili cone is deposited on the upper portion of exposed surf ace (the place to be formed of source and drain), of th e surface of the top surface of polysilicon structures (2 90, 410) and side wall spacers (295, 425) and GASAD d omain and FOX (260) and side wall surface. The deposi ted thickness of the cobalt is for example, 0.02㎛. The temperature of 450℃ is heated by the substrate covere d with cobalt after the deposition for the time period c orresponding to of 90 minutes in the reducing atmosph ere, in other words, the atmosphere. This heating proc ess forms the cobalt monosilicide (CoSi) on the place w here cobalt contacts with the silicone, and the top surf ace of not only the surface exposed with other words, the GASAD domain but also the polysilicon structure. A s to dissimilar domains, it remains while cobalt does not react. The cobalt (it is not CoSi) which does not react now comes off using the optional wet etchant like H 3 Po 4 : CH 2 COOH : HNO 3 : H 2 O (16 : 2 : 1 : 1). Nex

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의 폴리실리콘구조(290)와 수직으로 정렬하여 반대측에 형성되고, 함유 영역(320)이 각각의 폴리실리콘구조(290)의 정상부에 형성된다. 유사하게, CoSi2 함유 영역(430, 440)이 각각의 폴리실리콘 구조(420)와 수직으로 정렬하여 반대측에 형성되고, CoSi2 함유 영역(450)이 각각의 폴리실리콘 구조(420)의 정상부에 형성된다.

t, secondly for example, the temperature of 700℃ is he ated by the substrate for the time period correspondin g to of 30 minutes in the inert atmosphere, in other wo rds, the argon (Ar) atmosphere. It reacts with the silic one which is beneath the CoSi puts in order to form th e cobalt disilicide (CoSi(SB)2(/SB)) in which this secon d heating has the thickness of about 0.07㎛. Therefor e, the CoSi 2 containing domain (300, 310) (the fourte enth is the reference) perpendicularly arranges with ea ch polysilicon structure (290) and it is formed in the op posite side and the containing domain (320) is formed i n the top of each polysilicon structure (290). Similarly, it perpendicularly arranges with each polysilicon structu re (420) and CoSi 2 containing domains (430, 440) are formed in the opposite side and the CoSi 2 containing d omain (450) is formed in the top of each polysilicon str ucture (420).

n튜브(240)에서 P채널 MOSFET에 대한 P+형 소스 및 드레인을 형성하기 위해, 예를 들어 1㎛의 두께를 가진 포토레지스트가 기판상에 침착되어, n튜브의 표면을 노출시키도록 패턴된다. 이제 액셉터 이온이 CoSi2 함유 영역(430, 440)내로 주입된다(이 레지스트는 P튜브(250)를 주입으로 부터 차폐한다). 전술한 바와 같이, 주입량은 3가지 조건을 만족하도록 선택되며, 이온 에너지는 거의 모든 이온이 상기 영역(430, 440)내로 주입되도록 선택된다. 이점에 있어서, 액셉터 이온은 얘를 들어 붕소 이온이며, 유용한 주입량은 8#215#1015cm-2이고 유용한 대응하는 주입 에너지는 10keV인 것으로 결정되었다.

In the n tube (240), in order that P + type source and drain about the P-ch MOSFET are formed the photoresi st having for example, the thickness of 1㎛ is deposited on the substrate and it is patterned in order to expose the surface of the n tube. Now, the acceptor ion is inje cted within CoSi 2 containing domains (430, 440) as de scribed above, the injection amount is selected in order to be satisfied three condition and the ion energy is sel ected so that all ions are nearly injected within domain s (430, 440) (A resist shields P tube (250) from injectio n). As to the advantage, it lifted and the acceptor ion was the boron ion and the injection amount which was useful was 8× 10 15 cm - 2 and the implant energy whi ch was useful corresponding to was 10keV and the inje ction amount was determined.

침작되어 패턴된 포토레지스트는 벗겨지고, 약 1㎛의 두께를 가진 다른 포토레지스트가 기판상에 침착되고, 이번에는 P튜브(250)의 표면을 노출시키기 위해 패턴된다. 이제, 도우너 이온이 CoSi2 함유 영역(300, 310)내로 주입된다(세로 침착된 레지스트는 n튜브(240)를 제2주입으로 부터 차폐한다). 다시, 주입량 및 이온 에너지는 상기 조건과 요구를 만족하도록 선택된다. 이점에 있어서, 만일 도오너 이온이 예를 들어 비소 이온이면, 유용한 주이량은 5#215#1015cm-2이고 유용한 대응하는 이온 에너지는 60keV 보다 작거나 같다. 한편, 만일 도우너 이온이 인 이온이면, 유용한 주입량은 5#215#1025cm-2이고, 유용한, 대응하는 주입 에너지는 30keV 이하의 에너지이다.

The photoresist which deposited is patterned comes off and the dissimilar photoresist having the thickness of about 1㎛ is deposited on the substrate and it is pat terned this time, in order to expose the surface of P tu be (250). Now, demand are selected so that the donor ion is injected within CoSi 2 containing domains (300, 3 10) (the resist deposited to the force shields the n tub e (240) from the second injection) the injection amoun t and ion energy are again satisfied the condition and d emand. As to the advantage, if the drawing owner ion i s for example, the arsenic ion , the heed amount which is useful is 5× 10 15 cm - 2 and it is smaller than 60ke V or the ion energy which is useful corresponding to is the same. In the meantime, if the donor ion is the phos phor ion , the injection amount which is useful is 5× 10 25 cm - 2 and the implant energy which is useful corre sponding to is energy less than 30keV.

이온 주입 이후에, 예를 들어, 0.2㎛ 두께의 도핑 되지 않은 TEOS층과 0.2㎛두께의 인 도핑된 TEOS층의 연속한 층을 포함하는 인터레벨 유전체(600)(제15도 참조)가 기판상에 침착된다. 인터레벨 유전체(600)는 흐르도록 유도되고, 주입된 도펀트는 CoSi2로 커버된 n+형 소스 및 드레인(330, 340)(제16도 참조)과, CoSi2로 커버된 P+형 소스 및 드레인(460, 470)을 기판 가열에 의해 형성하기 위해 CoSi2 함유 영역으로 부터 아래에 놓인 실리콘으로 확산된다. 이점에 있어서, 약 0.2㎛보다 작거나 같은 깊이를 가진 소스 및 드레인을 실현하기 위해, 유용한 가열 절차가 800℃의 온도로 120분동안 기판을 가열하는 것이라는 것이 결정되었다.

It was induced so that the interlevel dielectric (600) (the 15 is the reference) including for example, the und oped TEOS layer of 0.2㎛ thickness and the consecutiv e layer of the A -doped TEOS layer the phosphorus of 0.2㎛ thickness after the ion implantation was deposite d on the substrate the interlevel dielectric (600) flowed and in order that form the n + type source and the drai n (330, 340) (the 16 is the reference), covered with th e CoSi 2 and P + type source and drains (460, 470) co vered with the CoSi 2 with the substrate heating, the i njected dopant was diffused to the silicone which was beneath puts from the CoSi 2 containing domain the so urce and the drain having the depth which was smaller

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than about 0.2㎛ or thed same were realized as to the advantage the source were determined that the heatin g process which was useful heated the substrate with the temperature of 800℃ for 120 minutes.

COMOS IC의 제조와 관련하여, 금속 실리사이드 영역으로 부터 기판내로 주입된 도펀트를 확산하는데 사용되는 가열 온도를 선택할때 만족되어야 할 추가의 요구 조건이 있다는 것을 주목하자. 즉 예를 들어 종래의 용광로 가열을 이용할때, 약 900℃를 초과하는 온도에서, n형 폴리실리콘 구조(420)내의 n형 도펀트가 P형 폴리실리콘구조(290)(통상적으로 n형 폴리실리콘 주조(420)와 접속 되어 있음)로 확산되어 그것을 카운터 도핑하려는 경향이 있는 것으로 알려져 있다. 이와 같은 카운터 도핑은 그것이 P채널 MOSFET에서 바람직하지 못한 임계 전압 시프트를 유도하기 때문에 바람직하지 못하다. 결과적으로, 본 발명의 실시예 2에 따라, CMOS IC를 제조하기 위해 용광로 가열을 이용할때 사용된 가열 온도는 900℃보다 낮으며, 850℃ 이하의 것이 바람직하다.

It pays attention that it has the additional requirement specification to be satisfied when choosing the heating temperature which is used to diffuse the dopant inject ed from the metal silicide domain within the substrate i n connection with the manufacture of the COMOS IC. That is, for example, when the conventional blast furna ce heating is used , it has the tendency to the n-type dopant within the n-type polysilicon structure (420) be diffused to the P-type polysilicon structure (290) (gene rally it is connected to the n-type poly-silicon casting (420)) and decide on that in the temperature exceedin g about 900℃ with counter doping and it is known. In t his kind of counter doping, that the P-ch MOSFET, bec ause the threshold voltage shift could not with the be desirable paper is induced it cannot with the be desirab le paper. Consequently, to produce the CMOS IC accor ding to the embodiment 2 of the invention, the heating temperature which is used when using the blast furnac e heating is lower than that of 900℃ and less than 85 0℃ is the be desirable.

소스와 드레인을 형성한 후에, 인터레벨 유전체(600)가 소스와 드레인 및 게이트 전극으로 경유 구멍을 개방하기 위해 패턴된다. 알루미늄과 실리콘, 즉 층(350, 360과 370(제17도 참조), 480, 490과 500)의 상호 확산에 대한 장벽이 경유 구멍으로 침착된다. 소스와 드레인 및 게이트 전극으로 부터 금속 접촉 패드로 연장된 상호 접속 알루미늄 런너(375, 385, 395와 505, 515, 525)(제17도 참조)가 전술한 바와 같이 형성된다.

After source and drain are formed it is patterned so that the interlevel dielectric (600) open the via hole to source and drain and gate electrode. Aluminum and silic one, in other words, the obstacle toward the interdiffu sion of layers (350, 360 and 370 (the seventeenth is th e reference), 480, 490 and 500) are deposited to the v ia hole. As described above, interconnection aluminum r unner (375, 385, 395 and 505, 515, 525) (the sevente enth is the reference) extended to the metal contact p ad from source and drain and gate electrode are forme d.

CMOS IC는 습기 및 기계적 손상에 대비한 장벽을 형성하기 위해 IC상에 실리콘 질화물층을 침착시키는 단계를 포함하는 통상적인 일련의 단계를 통해 완성된다.

It is completed through normal a series of step that the CMOS IC includes the step of sinking the silicon nitr ide layer on IC in order to form the obstacle comparing for moisture and mechanical damage.

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요약

내용 없음.

대표도

도1

명세서

[발명의 명칭]

반도체 장치

[도면의 간단한 설명]

제1도는 종래의 CMOS를 도시한 단면도.

제2도는 A는 종래의 이중 드레인 구조를 갖는 MISFET의 단면도.

제3도는 BSMS 제2도의 A의 MISFET의 반도체 표면의 불순물농도 분포와 그에 있어서의 전계를 해석한 것은 도시한 도면.

제3도~제6도는 본 발명의 제1의 실시에의 제조 공정을 순으로 도시한 단면도.

제7도는 본 발명의 제2의 실시에의 단면도.

제8도는 본 발명의 제3의 실시에의 단면도.

제9도는 본발명의 제1의 실시에의 특성을 도시한 도면.

제10도는 본 발명의 제4의 실시예의 단면도.

제11도는 본 발명의 제5의 실시예의 단면도.

제12도는 본 발명의 제6의 실시예의 단면도.

제13도, 제14도는 본 발명의 제7~제9의 실시에의 특성을 표시한 도면.

제15도~제17도는 본 발명의 제7의 실시에를 제조 공정 순서로 도시한 단면도.

제18도~제19도는 본 발명의 제8의 실시에를 제조 공정 순서로 도시한 단면도.

제20도는 본 발명의 제9의 실시예의 단면도.

제21도는 본 발명의 제9의 실시예의 드레인의 깊이 방향의 불순물 농도 분포를 도시한 도면.

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[발명의 상세한 설명]

본 발명은 MISFET에 관하여, 특히 초미세 MISFET의 고내압화에 가장 적합하고, 내 핫 캐리어 효과가 우수한 MISFET에 관한 것이다.

또한, 본 발명은 CMOSFET에 관하여, 특히 0.5μm 이하의 게이트 길이에 있어서도 5V 전원으로 동작가능한 고내압초미세 CMOSFET에 관한 것이다.

현재, MIS 전계 효과 트랜지스터(이하MISFET라 한다)는 미세화를 위해 게이트 절연막을 얇게 하여, 소오스와 드레인의 간격을 좁게하고, 또한 소오스와 드레인의 접합을 얇게 하려고 하고 있다.

상기의 경향의 결과, 현재의 MISFET에 있어서의 최대의 문제는 소오스와 드레인 사이의 내압의 저하이다. 드레인 측에서 신장해온 공핍층이 소오스 영역에 도달하기 때문에 생긴 소위, 펀치 스루 내압의 저하는 기판 농도를 증가하는 것에 의해 피할 수가 있으나, 그와 같이 하는 것에 의해서 역으로 전자사태 항복내압(avalanche effect break down)이 감소하게 된다. 특히, 게이트, 소오스 및 기판 전압을 영으로 하였을때의 전자사태 항복전압(이하, BV_{DS}라 한다)은 게이트 전압에 의해서 기판표면 전위의 증가가 억제되기 때문에 젖합 내압에비해서 극단으로 저하해 버린다. 그 결과, 찬넬 길이 1μm, 게이트 산화막의 두께20nm, 소오스 드레인 접합 깊이 0.35μm인 미세 MISFET의 소오스와 드레인 사이의 내압은 약6V로 통상의 전원 전압5V에 거의 일치할때까지 저하한다. 상기와 같이 미세 트랜지스터에 있어서는 전원 전압의 변동에 의해 간단히 파괴된다.

따라서, 종래의 미세 MISFET에 있어서는 상기의 결점을 극복하기 위해 드레인 구조에 관하여 0.2μm 정도의 얇은 접합 깊이를 갖는 고농도 불순물 확산층과 0.35μm 정도의 보다 깊은 접합깊이를 갖는 저농도 불순물확산층을 조합시키는 소위, 이중 드레인 구조를 채용하고 있다. 상기 구조에의 BV_{DS} 값을 약 1.5내지 2V 향상시킬 수가 있다. 그러나, 상기의 개량된 미세 MISFET에 있어서는 전원 전압의 변동에 의한 파괴로부터 통상 피할 수가 있다. 그러나, 상기의 개량된 미세MISFET에 있어서도 신뢰성의 관점에서는 아직까지 만족할 수가 없었다.

즉, 통상 조건의 장기간 동작에 있어서는 드레인 근방에 있어서의 강한 전계 효과에 의해 핫 케리어(hot carrier)가 게이트 절연막중에 주입되어 임계 전압 값의 변동, 또 표면준의 밀도의 증대 및 전달 콘덕턴스의 저항 등의 열화가 생긴다.

또, 이상은 MISFET의 단일체에 관한 것이지만, 2개 이상의 트랜지스터를 조합해서 구성한 CMOS(Complementary Metal Oxide Semiconductor) 구조에 있어서도 대략 마찬가지로 적용된다. 또, CMOS에서는 다음의 문제도 갖고 있다.

여기서, CMOS는 P 찬넬 MOS(이하 PMOS라 한다)와 N 찬넬 MOS(이하 NMOS라 한다)를 쌍으로 해서 동일칩위에 형성하고 있는 구조이다.

제1도는 2μm 이상의 게이트 길이를 갖는 종래의 CMOS의 단면 구조도이다.

제1도에 있어서 (21)은 N 도전형의 반도체 기판, (22)는 반도체 기판(21)내에 형성된 P 도전형의 확산층 영역으로 웰이라 한다. (23)은 필드 산화막, (24) 및 (25)는 웰(22)내에 형성된 NMOS의 소오스 및 드레인 확산층 영역으로 n 도전형을 가지며, 그 최대 불순물 농도는 $10^{20}cm^{-3}$이상으로 구성된다. (26) 및 (27)은 PMOS의 소오스 및 드레인 확산층 영역으로 P 도전형을 가지며, 그 최대 불순물 농도는 $10^{19}cm^{-3}$이상으로 구성된다. (28) 및 (29)는 각각 게이트 절연막 및 게이트 전극이다. (210) 및 (211)은 각각 보호절연막 및 소오스 또는 드레인 전극이다.

이와 같은 드레인 확산층의 불순물농도 구성을 갖는 종래 구조의 CMOS에 있어서는 소자의 미소화에 따라서 여러 가지의 결점이 발생한다.

(i) 소오스와 드레인 사이의 내압 저하, 즉 소자가 미소화 되는데 따라 찬넬 길이가 감소하기 때문에 펀치 스루 내압이 저하한다. 펀치 스루 내압의 향상은 기판 농도를 증가하는 것에 의해 달성할 수 있으나, 기판 농도의 증가는 역으로 전자사태 항복 내압이 저하하여 버린다. 찬넬 길이가 0.3μm 이하의 매우 미소한 NMOS에 있어서는 소오스와 드레인 사이의 내압이 2V이하로 현저하게 저하하기 때문에 통상의 전원 전압의 5V로서는 동작이 불가능하다.

그리고, 편치 수루 내압의 향상을 위해서 기판 농도를 증가하면, 찬넬 콘덕턴스 gm의 감소를 수반하기 때문에 MISFET이 미세화에 의해 얻어지는 고속 동작 특성은 저해된다.

(ii) 래치 업에 의한 MISFET의 파괴, 즉 종래 구조를 갖는 CMOSFET의 최대의 결점은 래치업이라고 부르는 사이리스터(thyristor) 동작에 기인하는 MISFET의 파괴이다. 이 래치 업 현상은 특히 CMOSFET의 미세화에 따라서 현저하게 된다. 즉, NMOS와 PMOS사이의 거리가 근접된 CMOSFET에 있어서는 NMOS의 드레인(25), 웰(22),반도체 기판(21) 및 PMOS의 소오스(26) 또는 드레인 (27)사이에 NPNP 구조를 갖는 기생 사이리스터가 형성된다. 상기의 사이리스터는 과전압의 인가, 통상 스위치 동작중의 내부과도적 과전압의 발생, 또는 광이나 방사선의 조사에 기인하는 소수 캐리어의 유기 등에 의해 유발되어 동작을 개시하고 전원을 정지할때까지 사이리스터 동작을 억제하는 것은 불가능하게 된다. 이 사이리스터 동작에 기인하여 과대 전류가 CMOSFET에 흐르기 때문에 CMOSFET는 파괴된다.

상기의 사이리스터 동작은 CMOSFET의 미세화에 따라서 웰(22)와 PMOS의 간격이 축소되어 기생 PNP 바이폴라 트랜지스터 및 기생 NPN 바이폴라 트랜지스터의 각각의 전류 이득률의 곱이 1보다 크게 되기 때문에 발생한다는 것이 알려져 있다.

상기의 각 기생 바이폴라 트랜지스터에 있어서의 전류 이득률의 곱을 갖게 하는 것에 의해 사이리스터 동작을 저지하는 방법이 제안되고 있다. 즉, P+N 접합으로 형성된 제1도에 도시한 종래 구조 PMSO의 소

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오스(26) 및 드레인(27)을 쇼트기 접합로 치환한 CMOSFET 구조가 1982년도 국제 전자 장치 학회(International Electron Devices Meeting) 예고집 462페이지에 기재되어 있다. 상기의 "쇼트키 장벽 PMOS에 의한 CMOS 래치 업 현상의 해결(CMOS latch-up elimination using schottky barrier PMOS)"라고 하는 보고서에서는 쇼트키 접합에 있어서의 소수 캐리어 주입 효율이 P+N접합의 것과 비교해서 대단히 작은 사실을 이용해서 기생 PNP 바이폴라 트랜지스터의 전류 이득률을 P+N 접합에 의한 종래 구조의 것과 비교해서 1/100 이하로 까지 저하시키는 것에 의해 래치 업 현상을 해결하고 있다.

P+N 접합대신에 쇼트키 접합으로 소오스 접합 및 드레인 접합을 형성하는 상기의 CMOSFET에 있어서 래치 업 현상은 방지되지만, 쇼트키 접합 특유의 결점이 존재한다. 즉, 쇼트키 접합을 사용한 CMOSFET에 있어서는 드레인 접합누설 전류가 큰 것, 비선형 출력으로 되어 옴접촉 특성을 얻을 수 없는 것 및 전달 콘덕턴스가 낮기 때문에 충분한 전류가 확보되지 않아 고속 동작을할 수 없는 것 등의여러 가지의 결점이 있다.

쇼트키 접합에 따른 상기의 결점은 그후 제한된 "저농도 불순물 확산을행한 쇼트키 트랜지스터(blightly doped schottky MOSFET)"에 의해 해결할 수가 있다. (1982년도 국제 전자 장치 학회 예고집, 466페이지 참조). 즉, 상기 쇼트키 트랜지스터에 있어서는 낮은 불순물 분포의 드레인 영역 위에 쇼트키 접합을 형성하면, 드레인 접합의 누설 전류가 작게할 수가 있고, 또한 전달 콘덕턴스도 통상 구조의 PMOS의 그것에 가깝게 할 수가 있다.

그러나, 낮은 불순물 농도 드레인 확산층과 쇼트키 접합을 조합시킨 구조에 의해 CMOSFET를 구성하는 방법에도 다음과 같은 결점이 존재한다. 즉, 상기의 문헌 "CMOS latch-up elimination using schottky barrier PMOS"에도 기재되어 있는 바와 같이 NMOS의 소오스 접합 및 드레인 접합을 쇼트키 접합으로 형성한 경우에 있어서의 기생 NPN 바이폴라 트랜지스터의 전류 이득률은 N+P 접합에 의해 드레인 접합을 형성한 종래 구조에 있어서의 기생 NPN 바이폴라 트랜지스터의 전류 이득률에 비해서 최대 10배나 크게 되는 것이다. 이에 따르면, 낮은 불순물 농도를 갖는 드레인 확산층의 유무에 관계없이 쇼트키 접합으로 PMOS 및 NMOS를 형성한 CMOS 트랜지스터는 PMOS의 소오스 접합 및 드레인 접합을 쇼트키접합으로 형성하고, NMOS의 각 접합은 통상의 N+P접합으로 형성한 CMOS트랜지스터보다 래치 업 현상이 생기기 쉽다는 결점이 있다.

쇼트키 접합에 의한 래치 방지에 관한 상기 2건의 문헌에 의하면, 낮은 불순물 농도 분포를 갖는 소오스 영역 및 드레인 영역의 각 표면에 쇼트키 장벽을 형성한 PMOS와 웅상의 높은 불순물 농도를 갖는 소오스 확산층 및 드레인 확산층이 형성된 NMSO의 조합에 의해 CMOS 트랜지스터를 구성하는 것이 래치업방지의 관점에서 가장 바람직한 것이된다.

그러나 , 상기 2건의 문헌 및 그들의 조합에 의해 얻어지는 결론은 CMOS 트랜지스터의 래치 업 방지의 관점에서만 성립하는 것으로서 CMOS 트랜지스터의 미세화에 따른 NMOS 및 PMOS의 내압 저하에 관한 상술한 결점에 대해서는 아무런 해결 방법도 제안되어 있지 않았다.

특히 , 찬넬길이가 0.5㎛이하의 초미세 CMOS 트랜지스터에 관해서는 상기 2건의 문헌에는 아무런 기재도 없고, 상술의 결점에 대해서는 전혀 해결 방법이 없다.

본 발명의 목적은 소오스와 드레인 사이의 내압이 통상의 전원 전압에 비해 충분히 높고, 핫 케리어 주입에 따라 특성 열화가 생기지 않는 초미세 MISFET를 제공하는데 있다.

본 발명의 다른 목적은 상기와 같은 종래의 결점을 해소하고, 극히 짧은 찬넬 길이로도 통상의 전원 전압으로 동작하고, 또한 래치 업 현상도 방지할 수 있는 CMOSFET를 제공하는데 있다.

본 발명은 종래의 이중드레인 구조의 가장 적합한 조건의 검토에 있어서, 특히 얕은 접합깊이를 갖는 고농도 불순물분포 영역이 완수하는 역할에 착안하여 해석한 결과에 기인한다. 제2도 A는 종래하여금 이중 드레인 구조를 갖는 MISFET의 단면도이다. 제2도 A에 있어서 (1)은 P형 반도체 기판, (2)는 필드 산화막, (2)은 게이트 산화막, (5)~(8)은 게이트 전극(4)를 확산 마스크로서 형성한 n형 불순물 영역으로 (5) 및 (7)은 드레인 확산층 (6) 및 (8)은 소오스 확산층이다. 여기서 (5) 및 (6)은 낮은 불순물 농도 확산층이며, 표면 불순물 농도를 Cs_2, 접합 깊이를 Xj_2로 정의한다. (7) 및 (8)은 높은 불순물 농도 확산층이며, 표면 불순물 농도를 Cs_1, 접합 깊이를 Xj_1로 정의한다. (9) 및 (10)은 각각 드레인 전극, 소오스 전극이다. 제2도 B는 제2도 A의 MISFET의 반도체 표면에 있어서 드레인 확산층 끝에서 소오스 확산층 측으로의 거리의 함수로서의 불순물 농도 분포가 거기에 있어서의 전계를 해석한 대표적인 결과다. 제2도 B는 실효 찬넬 길이가 1.1㎛, 게이트 산화막(3)의 막의 두께가 20nm, Xj_1이 0.25㎛, Xj_2가 0.3㎛, Cs_1이 $1\times10^{21}cm^{-3}$, $Cs_2\times10^{19}cm^{-3}$의 경우이고, 게이트 전극(4) 및 드레인 전극(9)에 인가한 전압은 각각 0V 및 10V이다.

제2도 B에서 명확한 바와 같이 드레인 전압의 인가에 의해 반도체 표면에 있어서, 최대 전계는 불순물농도가 $10^{18}cm^{-3}$부근에 있어서의 드레인 확산층 내부에서 형성되고, 불순물 농도가 보다 높은 드레인 확산층(7)내에서는 전계가 보다 작게 되어 가는 것을 알 수 있다. 본 발명은 이러한 해석 결과, 높은 불순물 농도 확산층(7) 내에 있어서하여금 전계가 보다 작게 되어 가는 것을 알 수 있다. 본 발명은 이러한 해석 결과, 높은 불순물농도 확산층(7)내에 있어서의 전계의 급격한 저하 경향에 착안한 것에 기안한다.

즉, 상기의 결과는 종래의 이중 드레인 구조의 MISFET에 있어서 상기 영역(7)이고, 내압화에 관해 거의 기여하고 있지 않다고 생각할 수 있다. 상기 개념에 따르면, 미세 MISFET의 고내압화의 관점에서 높은 불순물 농도 확산층의 존재는 도리어 장해로 되고 있으며, 드레인 확산층을 낮은 불순물 농도 확산층으로 구성하는 것이 바람직하다고 생각된다.

그러나 , 상기의 개념은 종래에 실시되어 있지 않는다. 이것은 종래의 드레인 확산층이 높은 불순물 농도 확산층으로 구성되는 것이라는 고정 개념에서 벗어나지 못했기 때문이고, 따라서 이중 드레인 구조에

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있어서도 높은 불순물 농도 확산층의 존재는 불가피하다라고 생각하였기 때문이다.

상기의 관점에 따라서 이중 드레인 구조에 있어서의 높은 불순물 농도 확산층(7) 및 (8)의 역할을 보면, 상기 영역(7) 및 (8)은 단지 전극(9) 및 (10)과의 옴접촉의 확보 및 소오스 및 드레인 영역의 확산층 저항의 저감화 이외는 아무런 역할에서도 하고 있지 않는 것은 명확하다. 한편, 소오스 및 드레인 영역의 확산층저항에 관해서는 백금 등의 실리사이드를 확산층 위에 형성하는 종래 기술에 의해 통상의 높은 불순물 농도확산층에 의한 시이트 저항값 50Ω/cm^3를 3!&/cm^2이하의 1/10 이하로 까지 저감화 할 수 있는 것이 알려져 있다. 그러나, 상기의 실리사이드 드레인 구조에 있어서는 시이트 저항의 저감 효과에만 착안하고, 소오스와 드레인 사이의 내압의 향상의 관점에서의 검토는 종래에 있어서 행하여지지 않아 드레인 확산층에는 고정 개념에 따라서 10^{20} cm^{-3}이상의 표면 농도를 갖는 높은 불순물 확산층이 사용되어 왔다.

본발명은 상기의 고정 개념이 무의미한 것이며, 드레인 확산층, 불순물 분포의 최적화에 의해 소오스 및 드레인 내압의 고내압화와 드레인 전극, 드레인 확산층사이의 양호한 옴접촉, 더 나아가서는 낮은 시이트저항화가 가능하게 된다고 생각하고, 검토한 결과에 따른 즉, 본 발명은 실리사이드 층을 형성하여야 할 드레인 확산층의 표면농도가 10^{18} cm^{-3}이상이면, 실리사이드 층 바로 아래에 표면농도가 10^{19} cm^{-3}정도의 석출층이 10nm 정도 형성되어 실리사이드와 드레인 확산층 사이에 MISFET의 통상동작에 충분한 옴접촉이 확보되는 사실을 발견한 것에 따른다. 또 본 발명은 상기 드레인 확산층의 표면 농도가 10^{20} cm^{-3}이하이면, 소오스와 드레인 사이의 내압을 실효 찬넬 길이 1μm 이하의 MISFET에 있어서도 최대 5V 이상 종래의 MISFET에 비해서 고내압화 할 수 있는 것을 발견한 사실에 따른다.

본 발명에 의한 CMOSFET는 불순물 확산 영역의 최대 불순물 농도가 10^{18} ~ 10^{20} cm^{-3}정도의 N형드레인 영역과 최대 불순물 농도가 10^{17} ~ 10^{19} cm^{-3}정도의 P형 드레인 영역을 가지며, 또한 상기 각 드레인 영역의 적어도 일부가 고용점 금속 또는 상기 금속의 실리사이드 층과 접합되어 구성되어 있는 것에 특징이 있다.

다음에 본 발명을 실시예에 따라서 더욱 상세하게 설명한다. 설명의 편의상, 도면을 가지고 설명하지만 주요부를 확대하여 도시하고 있으므로 주의를 한다.

[실시예 1]

제3도~제6도는 본 발명에 의한 MISFET하여금 1실시예의 제조 공정을 공정 순서로 도시한 도면으로서, (1)은 P도전형 비저항 1Ω/cm의 실리콘 기판이다. 반도체 기판(1)표면에 종래의 소자 분리 기술을 이용해서 0.8μm의 두꺼운 필드 산화막(2)를 선택적으로 형성한 후, 활성 영역의 반도체 표면을 노출하고, 20nm의 깨끗한 게이트 산화막(3)을 형성한다. 그후, 약 0.3μm하여금 실리콘 박막을 게이트 산화막(3) 위에 형성하고, $POCl_3$을 소오스로 하는 열 확산에 의해 실리콘박막에 인(p)의 고농도 확산을 행한다.

그 후에, 리도그래피에 의해 게이트 전극(4)를 형성한다. 리도그래피후의 찬넬 길이는 1μm이다. 다음에 테트라에록시실란 ($Si(OC_2H_5)_4$)을 사용한 화학 기상반응에 의해 0.5μm의 막의 두께를 갖는 실리콘 산화막(11)을 전면으로 퇴적시킨다. 상기의 퇴적막(11)을 반응성 스퍼터 에칭에 의해 최대기판 표면과 수직방향으로 에칭을 행하여 평탄부에 퇴적된 실리콘 산화막을 제거하면, 제4도에 도시한 바와 같이 게이트 전극(4)의 측벽에만 실리콘 산화막(11)이 남게된다. 이 상태에서 산화막(3)을거쳐서 비소를 가속에너지70 KeV의 조건에서 이온 주입에 의해 반도체 기판(1) 표면에 주입한다. 상기의 조건은 최대 기판 표면에서 최대 불순물 농도로 되는 조건이다. 본 실시예에 있어서는 주입량을 변수로 하고, 표면 불순물 농도가 1×10^{17} ~ 10^{19} cm^{-3}의 범위에서 여러 가지의 값을취할 수 있도록 다수개의 MISFET를 작성하였다. 상기의 이온주입 공정후 주입 이온의 활성화의 열처리를 행하였다.

상기의 열처리는 1000℃에서 행하였지만, 여러가지의 주입량을 갖는 각각의 MISFET에 대해 접합깊이 Xj가 0.25μm로 되도록 각각 열처리 시간을 설정하였다. 그후, 드레인 확산층(5) 및 소오스 확산층(6) 위의 게이트 산화막(3)을 제거하고, 50nm의 막의 두께의 백금(Pt)를 전면에 스퍼터링법에 의해 증착한다. 다음에 450℃의 열처리를 하고, 드레인(5), 소오스 확산층(6) 표면 및 게이트 전극(4)표면에 백금 실리사이드(PtSi)(12)를 형성한다.

상기의 열처리에 있어서 산화막(11) 및 (2) 위에서는 실리콘과의 반응은 일어나지 않아 실리사이드는 형성되지 않는다. 따라서 상기 열처리 공정후, 왕수로 에칭하면 PtSi는 왕수로 에칭되지 않기 때문에 산화막 및 반응하지 않는 Pt만이 제거되고, 게이트 전극(4), 드레인 확산층 (5) 침소오스 확산층(6)의 각 표면에 위에만 PtSi가 자기 정합적으로 남게 된다. 여기에 있어서 PtSi 층(12) 바로 아래에는 PtSi 층 형성전의 표면 불순물 농도 보다도 1자리수 높은 불순물 농도를 갖는 약 10nm두께의 석출층(13)이 PtSi 층(12)와 자기 정합적으로 형성되었다. 상기 석출층(13)내에 있어서의 깊이 방향의 불순물 분포는 깊이에 대해 아래로 볼록한 형상을 갖는다. PtSi 층 (12)의 형성 후, 공지의 기술을 사용해서 보호 절연막(15), 또 드레인 전극(9) 및 소오스 전극(10)을포함하는 배선전극을 바라는 회로 방식에 따라서 형성한다. 상기의 전극(9)(10)에는 알루미늄(Al)의 증착만을 사용하지만, Al이 PtSi 층 (12)와 반응하는 것을 방지하기 위하여 A1배선 공정전에 Ti와 Ta의 동시 스퍼터링에 의해 TiTa 막(14)를 PtSi 막(12)위의 접촉구멍 부분에 사전에 형성한다.

상기의 제조 과정을 거쳐서 제조된 각종의 표면 불순물 농도 Cs_2를 갖는 드레인 확산층(5)로 구성된 각각의 MISFET의 게이트 전압이 영에서 소오스와 드레인 사이의 내압 BV_{DS}를 측정하였을 때, 제9도의 결과가 얻어졌다. 제9도의 측정에 사용한 각 MISFET는 본 실시예의 제조 과정에서도 명확한 바와 같이 실효찬넬 길이가 1μm 게이트 산화막(3)의 막의 두께가 20nm, 드레인 접합 깊이 0.25μm의 동일 조건의 것이고, 드레인 확산층(5)의 표면 불순물 농도만이 달라지고 있다. 본 실시예의 각 MISFET에 있어서는 드레인 접합끝이 게이트 전극(4)의 끝과 일치하도록 게이트 측벽 산화막(11)의 막하여금 두께를 제어하고 있

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다. 제9도의 결과로 주목되는 것은 드레인 확산층(5)의 표면 불순물 농도가 $5\times10^{18}cm^{-3}$부근에서 BV_{DS}값이 최대로 되어 11.5V에 까지 도달하는 것이다.

상기의 값은 표면 불순물 농도가 $10^{20}cm^{-3}$이상의 드레인으로 구성되는 동일 접합 깊이를 갖는 종래 MISFET의 BV_{DS}값보다 4.5V 이상이나 높은 내압화가 실현되어 있는 것을 나타내고 있다. 또, 제9도에 있어서 점선으로 표시한 종래의 이중 드레인 구조 MISFET에 있어서 BV_{DS}값의 최대값보다도 본 발명에 의한 MISFET의 쪽이 3.5V 이상이나 높은 내압화가 실현되어 있는 것을 나타내고 있다.

그리고, 제9도에 도시한 이중 드레인 구조의 특성은 낮은 불순물 농도 분포(5)의 접합 깊이 Xj_2가 0.25 μm, 표면 불순물 농도 Cs_2는 도시한 각각의 값이고, 높은 불순물농도 분포 (7)의 접합 깊이 Xj_1이 0.15 μm, 표면 불순물 농도 Cs_1은 $1\times10^{21}cm^{-3}$의 구성으로 되는 드레인 확산층을 갖는 MISFET에 관한 것이다. 여기에서 게이트 산화막(3)의 막 두께는 20nm, 실효 찬넬 길이는 1μm이다.

본 실시예에 따라서 제조한 MISFET에 있어서의 전류 전압 특성을 상세하게 검토하였으나, 드레인(5) 및 소오스 확산층(6)의 표면 불순물 농도가 $1\times10^{18}cm^{-3}$ 이상으로 구성된 MISFET에 있어서는 전류의 상승 특성에 쇼트키 성분이나 큰 직렬 저항 등이 발견되지 않고, 양호한 옴접촉이 드레인(5) 및 소오스 확산층(6)과 백금 실리사이드(12) 사이가 얻어지고 있는 것이 명확하게 되었다. 본실시예에 따라서 제조된 MISFET에 관한 상기 측정결과에서 드레인 확산층(5)의 표면 불순물 농도로 $10^{18}cm^{-3}$이상$10^{20}cm^{-3}$ 미만인 것이 소오스 드레인 내압의 고내압화의 관점 및 양호한 음접촉의 관점에서 바람직하고, 특히 $5\times10^{18}cm^{-3}$ 정도인 것이 바람직하다. 상기의 조건에서 드레인 확산층이 구성된 본 발명에 의한 MISFET에 있어서는 종래의 동일치수의 미세 MISFET에 비해서 BV_{DS} 값에서 3.5V 이상의 고내압비가 실현되고, 또한 양호한 옴접촉도 확보할 수가 있었다. 상기의 양호한 옴접촉은 낮은 불순물 농도 표면으로서 실리사이드 형성시에 실리사이드층 (12) 바로 아래에 매우 얇은 높은 불순물 농도 석출층(13)이 동시에 형성되기 때문이라고 생각된다.

본발명에 따라서 구성된 MISFET에 있어서는 종래의 실리사이드 드레인 구조를 갖는 MISFET와 마찬가지로 $3\Omega/cm^2$ 의 낮은 시이트 저항을 확보할 수가 있었다.

[실시예 2]

제7도는 본발명의 다른 실시예를 도시한 도면이며, 상기 제1의 실시예에 있어서 게이트 측벽 산화막(11)의 막의 두께를 얇게 하고, 드레인 접합 끝이 게이트 전극(4)아래에 존재하도록 구성하여 MISFET를 작성하였다.

상기 구성에 있어서는 드레인 확산층(5)의 낮은 불순물 농도 영역의 대부분 이 게이트 인가 전압에 의해 제어되는 것이 가능하게 된다. 실효 찬넬 길이 1μm, 소오스와 드레인의 각 적합 깊이 0.25μm 및 게이트 산화막의 두께 20nm등 MISFET의 구조 파라미터를 동일하게 하고, 상기 제1의 실시예 및 본 실시예에 따라서 구성된 MISF ET, 또 종래의 높은 불순물농도 분포만으로 소오스 및 드레인이 구성된 MISFET에 대해서 각각 그 전달 콘덕턴스를 측정하였다. 그 결과, 상기 종래 구조 MISFET의 전달 콘덕턴스를 1로 하였을 때, 제1 및 본 실시예에 따라서 구성된 각 MISFET의 전달 콘덕턴스는 각각 0.95 및 0.98로 되었다.

본 실시예에 따른 상기 MISFET의 전달콘덕턴스의 값은 드레인 접합 깊이의 약절반이 게이트 전극(4)로 덮여지도록 구성된 MISFET에 관한 것이다. 상기 측정 결과에서 명확한 바와 같이, 드레인 접합이 게이트 전극(4)로 덮여지는 것과 같이 구성한 MISFET에 있어서는 종래 구조 MISFET와 거의 동일한 전달콘덕턴스를 확보하고, 또한 종래 구조 MISFET의 약2배의 소오스와 드레인 사이의 내압을 실현할 수가 있었다. 본 실시예에 있어서, 전달 콘덕턴스 향상의 관점에서는 게이트 전극(4)로 덮여지는 드레인 저농도 영역의 비율을 크게 하는 것이 바람직하지만, 게이트 용량의 저하의 관점에서는 상기 비율을 적게하는 쪽이 바람직하다. 따라서, 상기의 비율은 집적회로 설계에 관한 종합적 판단에 의해 결정하면 좋다.

[실시예 3]

제8도는 본 발명의 다른 실시예를 도시한 도면으로서, 상기 제1의 실시예에 있어서 낮은 불순물 농도 드레인 확산층의 형성을 위한 비소 이온 주입 공정을 2회로 나누어 각각 70KeV 및 300KeV의 에너지로 이온주입하고, 다음에 상기 제1의 실시예에 따라서 MISFET를 제조하였다.

상기 제1의 이온 주입에 의해 $5\times10^{18}cm^{-3}$ 인 최대 불순물 농도가 반도체 표면에 형성되고, 제2의 이온 주입에 의해서는 $5\times10^{17}cm^{-3}$ 인 최대 불순물 농도가 반도체 기판 표면에서 약 0.16μm 내부에 구성되는 드레인 확산층 구조로 하였다. 상기 MISFET에 있어서 소오스와 드레인 사이에 5V의 전압을 인가하고, 게이트 인가 전압의 함수로서 기판(1)에 흐르는 전류를 측정하였을 때, 그 최대 전류값은 $1.7\times10^{-7}A$이었다.

본 실시예에 의한 MISFET와 동일한 구조 파라미터를 갖는 상기 제1의 실시예에 따른 트렌지스터 및 공지의 이중 드레인 구조로 구성된 MISFET에 대해서 상기와 동일한 조건에 의해 기판 전류를 측정한 결과는 그 최대 전류가 각각 $9.6\times10^{-7}A$ 및 $1.2\times10^{-5}A$이었다.

본 실시예에 따른 MISFET의 기판전류가 종래의 구조의 MISFET에 있어서의 기판전류 보다도 약 2리 수만큼이나 작은 것은 MISFET의 신뢰성의 향상에 본 발명에 의한 MISFET가 매우 유효하다는 것을 나타내고 있다. 즉, 기판 전류의 저감은 게이트 산화막 속의로의 핫 캐리어 주입량의 저감화의 작용을 갖는 것으로 알려져 있고, 임계 전압값의 변동이나 표면 준위 밀도의 증가등의 트랜지스터 특성이 저하하지 않도

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록 한다.

본 실시예에 있어서는 이온 주입의 가속 에너지를 변경한 2회의 이온 주입 공정에 의해 다른 분포를 갖는 낮은 불순물 농도 분포의 합성에 의해 드레인 확산층 (5)를 구성한 일 예를 나타냈지만, 상기의 드레인 확산층은 3종류 이상의 낮은 불순물 농도 분포의 합성에 의해서도 좋고, 제조 공정도 이온 주입 법에 한정되는 것이 아니라 예를들면, 공지의 열 확산법에 의해서도 좋다. 또, 드레인 확산층을 형성하는 불순물은 동일의 것일 필요는 없고, 동일한 도전형의 원자이면 그 조합은 아무래도 좋다. 즉, 본 실시예의 기본 개념은 드레인 확산층(5)내의 최대 전계인가 영역이 한점에 집중하는 일 없이 인가 전계를 가능한 한 분산시킬 수 있는 드레인 불순물 분포를 실현하는데 있다. 상기 개념에 따르면, 최대 전계가 인가되는 불순물 농도가 약 $1\times10^{18}cm^{-3}$로 드레인 확산층(5) 전체가 구성되는 것이 이상적이고, 상기의 이상에 의해 합당한 불순물 농도 분포를 합성하여 드레인 확산층(5)를 구성하는 것이바람직하다.

[실시예 4]

제10도는 본 발명의 다른 실시예를 도시한 도면으로, 상기 제1의 실시예에 있어서의 실리콘 박막에 의해 구성된 게이트 전극(4) 대신에 Mo 박막에 의한 금속 게이트 전극(4)를 사용하고 있다. 상기의 Mo 전극의 표면 위에는 실리콘 질화막으로 되는 전국 보호막(18)을 게이트 전극(4)와 자기 정합적으로 구성하였다. 이것은 동일의 포토레지스트를 사용해서 에칭하는 것에 의해 행한 상기의 게이트 구조는 금속 게이트 구조로서 공지이며, 그 상세한 설명은 생략한다. 상기 제1의 실시예 및 상기 공지의 금속 게이트 구조 트랜지스터의 제조 방법에 따라서 낮은 불순물 농도 드레인 확산층(5) 및 소오스 확산층(6)위에 PtSi층 (12)를 형성한다.

그후, 상기 실리사이드 층(12) 바로 아래에 실리사이드층과 자기 정합의 관계로 As 이온을 주입하였다. 상기 As 이온 주입에 의한 최대 불순물 농도는$1\times10^{21}cm^{-3}$이고, 반도체 표면에서 최대값을 갖는 구성으로 되어 있다. 상기 As 이온 주입에 의한 접합 깊이는 50nm 이하로 되는 것과 같이 이온 주입기에 가속 에너지를 여러 가지로 변화시켜서 실시하였다. 그후 램프가열을 사용한 순간가열법에 의해 상기의 높은 불순물농도 영역(16)만을 활성화 하였다.

그후, 상기 제1의 실시예에 따라서 보호 절연막(15) 및 드레인 전극(9)와 소오스 전극(10)을 구성하였다. 상기 전극(9) 및 (10)과 실리사이드 층(12) 사이에는 A1과 실리사이드의 반응을 방지하기 위한 Ti,Ta혼합막(14)가 상기 실시예 1에 따라서 구성되어 있다. 상기 구성에 따라서 제조된 접합 깊이 10nm에서 50nm인 높은 불순물 농도 영역(16)을갖는 각종 MISFET에 있어서 그 BV_{DS} 값을 측정하였을 때 모든 MISFET에 있어서도 BV_{DS}값은 상기 제1의 실시예에 따른 MISFET의 BV_{DS} 값보다 약0.5V낮을 뿐 이었다.

상기의 결과는 실리사이드 층(12) 바로 아래의 높은 불순물 농도 영역(16)이 50nm 이하로 얇으면, 종래 구조 MISFET에 비해서 소오스 및 드레인 내압이 한층 개선되는 것을 나타내고 있다. 본 실시예의 기본적 개념은 드레인 확산층(5) 표면에 구성하는 높은 불순물 농도 영역(16)이 접합 깊기로 50nm 이하로 매우 얇으면 BV_{DS}값의 고내압화에 실효적으로 지장이 없고, 또한 양호한 옴접촉도 확보할 수 있는 것이다. 본 실시예에 있어서는 실리사이드 층(12)를 드레인 확산층(5) 위에 구성한 에에 대해서 나타내었지만, 상기 개념에 따르면 실리사이드 층은 백금 실리사이드에 한정되는 것이 아니고, Mo,W,Pt,Pd,Ni,Ti,Ta,Nb,Cr,Pr등의 고융점 금속 및 그들의 실리사이드 막으로 치환하여 구성하여도 지장이 없다.

[발명의 다른 실시예]

이상의 각 길기에에서는 모두 소오스, 드레인 영역으로 되는 확산층은 낮은 불순물 농도의 얇은 확산층이고, 화산층 저항을 저감하는 길리사이드 층은 게이트 전국에서 분리(오프 셋)되어 형성되어 있다. 따라서, 이와 같은 오프 셋 구조의 트랜지스터에서는 소오스와 드레인을 고농도, 확산층으로 형성한 것보다도 실효찬넬 콘덕턴스가 저하한다.

그래서, 게이트 측벽 절연막(제6도, 제7도, 제8도, 제19도의 부호(11)을 실리콘 산화막이 아니고, 비유전율이 보다 높은 재료로 형성하면 게이트에서의 프린지(fringe) 용량(면이 대향하는 용향보다 광의의 의미로서, 도전체의 언저리나 끝에 생기는 용량을 말한다.)에 의해 소오스 및 드레인의 낮은 불순물 농도 확산층의 표면으로의 게이트 전압의 영향을 높일 수가 있어 실효 전달 콘덕턴스가 높은 디바이스를 얻을 수가 있다. 이것은 제1도에 도시한 바와 같은 이중 확산 구조의 소오스와 드레인을 갖는 MIS FET에 대해서도 적용된다.

[실시예 5]

제11도는 본 발명에 의한 MISFET의 1실시예를 도시한 도면으로, (1)은 P 도전형 비저항 1Ω/cm의 실리콘 기판이고, (2)는 공지의 선택 산화법에 의해 형성된 필드 산화막으로 인접하는 MISFET사이를 분리하는 두꺼운 실리콘 산화막이다. (3)은 20 nm의 실리콘 열 산화막, (4)는 인을 첨가시켜 저 조항화된 실리콘 박막으로 구성된 게이트 전극이다. 공지의 실리콘 게이트 기술에 의해 게이트 전극(4)을 형성한 후, 실리콘 열 산화막(3)을 거쳐 게이트 전극을 마스크로 해서 비소(As) 이온을 이온 주입법에 의해 실리콘 기판 표면에 주입하고, 이어서 주입 이온의 활성화를 위한 열처리를 행하여 드레인 확산층(5) 및 소오스 확산층(6)을 형성하였다. 상기의 이온 주입에 있어서는 반도체 표면에서 불순물 농도가 최대로 되고, 그 최대값이$5\times10^{18}Cm^{-3}$으로 되는 조건에서 행하였다.

그후, 암모니아(NH_3)와 모노실란(SiH_4)의 화학 기상 반응에 의해 주표면 전면에 비유전율 6.0인 실리콘질화(Si_3N_4)막을 막두께 0.25㎛의 조건으로 퇴적한다.

그후, 평행 평판형 반응성 스피터 에칭 장치에 의해 상기의 Si_3N_4 막을 0.25㎛두께만큼 에칭하였다.

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상기의 에칭은 소위 이방성 에칭이라고 하는 것으로서 반도체 기판 표면과 수직 방향에만 에칭을 진행시킬 수가 있다. 따라서, 상기의 에칭후에는 게이트 전극(4)의 측벽부에만 Si_3N_4막(19)가 남게 된다. Si_3N_4막으로 구성되는 측벽 절연막(19)의 형성 후, 게이트 전극(4)와 측벽절연 막(19)를 마스크로 하여 소오스 및 드레인 확산층 표면에서 최대 불순물 농도로 되는 조건으로 재차 As 이온 주입을 행한 후, 그 활성화를 위한 열처리를 실시하였다.

살기 제2의 이온 주입에 의해서 고오스 및 드에인 확산층의 최대 불순물 농도는 1×10^{-3} 이상의 높은 불순물 농도로 되었다. 그후, 통상의 반도체 제조 공정 순서에 따라, 게이트 보호 산화막(20) 및 드네인 전극(21)과 소오스 전극(22)를 형성하고 MISFET로 되는 반도체 장치를 제조하였다.

본 실시에에 따라서 제조한 MISFET는 실효 찬넬 길이가 0,9㎛, 드레인 확산층에 있어서의 낮은 불순물 농도 영역(5)의 접합 깊이가 0.35㎛, 높은 불순물 농도 영역(7)의 접합 깊이가 0.15㎛이었다.

상기 MISFET에 있어서 측벽 절연막(19)는 소오스 및 드레인 확산층 위에서 10^{20} cm^{-3} 이하의 불순물 농도 영역 표면을 덮고 있는 구성으로 되어 있다. 본 실시에에 따른 상기 MISFET의 전달 콘덕턴스는 측벽 절연막이 증래의 실리콘 산화막으로 구성되는 동일 치수의 MISFET에 있어서 전달 콘덕턴스의 약1.1배 크다는 것을 알게 되었다.

상기의 전달 콘덕턴스의 차이는 게이트 전극(4)의 측벽에 있어서 절연막(19)의 비유전율의 차이에 차이에 따른 전속 밀도의 차이에 의한 것이라고 생각된다. 즉, 본 실시에와 같아 측벽 절연박(19)의 비유전율이 게이트 산화막의 비유전율 보다 1.6배 큰 경우에는 측벽 절연막의 비유전율이 게이트 산화막의 비유전율과 동등한 종래 구성의 MISFET의 경우보다 게이트 전계가 소오스 및 드레인 확산층의 낮은 불순물 농도 영역 표면으로 돌아 들어가는 전속 밀도가 크고, 낮은 불순물 농도 영역 표면을 보다 n형화하여 전도도를 높이기 위함이라고 생각된다.

[실시에 6]

제12도는 본 발명의 다른 실시에를 설명하기 위한 도면이다. 상기 제1의 실시에에 있어서 낮은 불순물농도의 드레인 확산층(5)및 소오스 확산층(6)을 형성한 후, 실리콘 게이트 전극(4)의 표면을 열산화하여 10㎚의 실리콘 산화막(23)으로 게이트 전극(4)을 덮는다. 그후, 비유전율로 되는 실리콘 박막을 SiH_4가스의 화학 기상 반응을 사용해서 전면에 퇴적하였다. 퇴적막의 두께는 약0,5㎛이었다.

그후, 평행 평판형 반응성 스피터 장치에 의해 반도체 표면과 수직 방향으로 상기 실리콘 박막을 0.5㎛ 에칭하였다.

상기 공정에 의해 게이트 전극(4)의 측벽에 얇은 실리콘 박막(23)을 거쳐서 실리콘 퇴적막(19)가 외부로부터 격리되어 0.5㎛의 으로 남게 되었다. 상기 에칭 후는 상기 제1의 실시에에 따라서 MISFET를 제조하였다. 본 실시에에 따라서 제조한 MISFET의 전달 콘덕턴스를 측정하였을 때 실리콘 산화막으로 게이트 전극의측벽 절연막을 구성한 동일 치수의 증래 MISFET의 전달 콘덕턴스의 약 1.2배에 달하였다. 더욱 주목 되는 것은 본 실시에에 따른 MISFET의 정특성 측정후에 재차 전달 콘덕턴스를 측정하였을 때 전달 콘덕턴스는 더욱 증가하여 통상 이중 드레인 구조 MISFET의 전달 콘덕턴스의 약 1.25배까지 달한다.

상기는 소오스 및 드레인 확산층이 높은 불순물 증도 분포만으로 구성되는 통상MISFET의 전달 콘덕턴스와 거의 같은 것이다. 본 실시에의 MISFET에 있어서 실효적인 전달 콘덕턴스가 향상한 제1의 이유는 측벽 퇴적막(19)의 비유전율이 실리사이드(12)와 실리콘 산화막의 값에 비해서 충분히 크기 때문이라고 생각된다. 또, 제2의 이유는 정특성의 측정으로 5V 이상의 게이트 전압을 인가하였을 때, 게이트 전극보다 정의 전하가 얇은 산화막(23)을 거쳐서 실리콘 퇴적막(19)에 천이되어 축적되고, 이 정의 축적 전하에 의해 소오스 및 드레인 확산층의 낮은 불순물 농도 영역표면이 더욱 n형화하여 전도도가 상승하였기 때문이라고 생각된다.

즉, 실리콘 퇴적막(19)는 전기적으로 프로그램 가능한 불휘발성 메모리에 있어서의 부유 게이트의 작용을 갖는 것이라고 생각된다. 실리콘 퇴적막(19)를 정의 전하를 축적하는 부유 게이트로서 작용시키는 것은 MISFET 제조후의 좋은 품질 선택 테스트시에 특성 점검을 행할 때에 실시할 수 있으므로 제품 출하전에 전하를 주입하여 축적, 유지시키는 본 실시례의 트랜지스터에 있었어는 드레인 전계에 의한 드레인의 낮은 불순물 농도 영역의 표면 전계를 약하게 하는 적용도 갖고 있으며, 드레인 강전계에 의한 핫 캐리어의 게이트 산화막으로 주입에 따른 MISFET의 열화현상도 방지하는 다른 작용도 갖고 있다.

이상과 같이 하면 ,게이트 측벽에 있어서 프린지 용량을 개재한 게이트 전계의 영향을 소오스 및 드레인의 낮은 불순물 농도 영역 표면에 강하게 영향을 줄 수가 있고, 실효적인 전달 콘턴스를 종래 구조에 비해서 1.1~1.2배 이상 크헤 할 수 있다.

본 발명의 기본적인 개념에 따르면, 측벽 퇴적막은 실리콘 질화막에 한정되는 것은 아니고, 알루미나(Al_2O_3)탄달 산화막(Ta_2O_5), 티타늄(TiO_2), 지르코늄 산화막(Zr_2O_3), 하프늄 산화막(Hf_2O3)등 실리콘 산화막의 비유전율 보다 충분히 큰 비유전율을 갖는 유전체이면 좋다.

또, 본 발명에 의한 전달 콘덕턴스의 향상 효과는 게이트 측벽에 반도체 등으로 구성되고, 외부에서 격리된 부유 게이트 또는 외부에서 격리되 전하 축적 기구를 갖는 절연막 또는 절연막 사이의 경계면에서 형성되어도 좋으며, 외부에서 격리된 측벽 퇴적막은 실리콘에 한정되는 것은 아니고, 다른 반도체 예를 들면, 실리콘 카바이드(SiC)나 게르마늄(Ge)등이라도 좋고, 또 실리콘 질화막이나 알루미나막 등의 절연막이라도 좋다.

[발명의 또 다른 실시에]

본 발명은 드레인 확산층에 있어서의 높은 불순물 농도 영역에 관해서 증래의 상식에 구애받지 않고 그

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물리적 근간에 까지 되돌아가 해석한 결과에 기인한다. 즉, 여러가지의 드레인 확산층 농도를 갖는 MISFET에 있어서 드레인 확산층 표면에 고융점 금속의 실리 사이드 층을 형성 하였을 때, 인(P) 및 비소(As)등의 도전형의 불순물로 상기 드레인 확산층이 형성되어 있는 경우에 한하여 드레인 확산층 표면에 불순물 농도가 약 10nm의 깊이로 고농도화 되는 현상이 있다. 즉, NMOS에 있어서는 드레인 확산층 표면 불순물 농도가 $1\times10^{18}cm^{-3}$이상이면 상기 실리사이드 층과 반도체 표면 사이에 양호한 옴특성이 얻어져 NMOS로서의 특성에 아무런 문제도 생기지 않는다는 사실이 발견되었다.

통상의 MISFET에 있어서의 드레인 확산층은 반도체 기판 표면 부근에서 $10^{20}cm^{-3}$이상의 높은 불순물농도 영역을 가지며, 기판 내부를 향해서 가우스 분포, 또는 오차함수 분포로 감쇠하는 불순물 농도 분포를 갖는다.

상기의 통상 드레인 확산층에 전압을 인가하고, 이 즉, 불순물 농도의 함수로서 인가 전계를 해석하면, $10^{20}cm^{-3}$이상의 높은 불순물 농도 영역에 있어서는 매우 약한 전계밖에 인가되지 않는다는 사실이 판명되었다. 이 사실은, 초미세MISFET의 고내압화의 관점에서 보면, 높은 불순물 농도의 존재는 도리어 유해하고, 드레인 확산층의 최대 불순물 농도는 $10^{19}cm^{-3}$이하로 구성되는 것이 바람직하다는 것이 판명되었다. 상기의 $10^{20}cm^{-3}$이상의 높은 불순물 농도 영역의 MISFET에 있어서의 역할은 확산층 정항의 저감화와 배선 금속의 양호한 옴접촉의 확보에 있지만, 상기 후자의 역활 즉, 배선 금속과의 양호한 옴 접촉은 $1\times10^{18}cm^{-3}$이상의 표면 불순물 농도를 갖는 드레인 확산층 위의 실리사이드 층의 구조에 의해서 치환이 가능하다. 상기 전자의 역할, 즉 소오스 확산저항 및 드레인 확산 저항의 저감화에 관해서는 소오스 및 드레인 확산층 표면의 실리사이드화에 의해 실현되는 것이 알려져 있고 , 특히 초미세 트랜지스터에 있어서의 매우 얕은 접합 형성에서는 실리사이드화에 의한 저항 저감의 효과는 현저한 것이 있다.

그리하여, 본 발명의 CMOSFET는 상기의 해석 결과에 따른 개념을 발전시켜 드레인 확산층의 높은 불순물 농도 영역을 드레인 확산층과 옴 접촉으로 결합된 얇은 실리사이드 층으로 치환하고 , 또한 드레인 확산층의 불순물 농도에 관한 최적 조건을 해석적으로 구한 결과를 이용하는 것이다.

상기 최적조건은 특히 0.5㎛이하의 게이트 길이를 갖는 초미세 MISFET의 고내압화 및 래치 업 방지에 관한 최적 조건이다.

제13도 및 제14도는 각각 본 발명에 의한 해석 결과를 도시한 도면으로서, 드레인 확산층 표면 불순물 농도의 함수로써 구한 소오스 및 드레인 내압 및 최대 기판 전류의 곡선을 표시하고 있다.

제13도에 있어서는 소오스와 드레인 사이의 내압으로서 전자사태 항복전압을 점선으로 표시하고, 펀치 스루 내압을 실선으로 표시하고 있다. 각 내압 모두 찬넬 길이의 함수로서 각각 구하고 있다.

제13도에 있어서 전자사태 항복전압은 PMOS에 관한 것이고 , NMOS의 값의 전체적으로 표시된 곡선보다 0.1~1(V) 저하하는 경향에 있다. 펀치 스루 내압에 대해서는 PMOS와 MNOS의 값 사이에 다른 것은 발견되지 않는다.

제13도에서 새로이 명확하게 된 사실은 찬넬 길이가 0.5㎛ 이상의 트랜지스터에 있어서는 드레인 확산층의 표면 불순물 농도를 $3\times10^{18}cm^{-3}$으로 설정하면, 통상 구조의 동일 치수의 트랜지스터에 있어서 소오스 및 드레인 내압에 비해서 약 2배에 해당하는 10V 이상의 내압을 실현할 있는 것이다. 또, 찬넬 길이가 0.4㎛ 이하의 트랜지스터에 있어서는 찬넬 길이에 의존해서 각각 최적의 드레인 확산층 표면 불순물 농도를 약 $1\times10^{18}cm^{-3}$으로 설정하면, 소오스 및 드레인 내압을 약 7V로 까지 향상할 수가 있다. 찬넬 길이가 0.2㎛의 PMOS 트랜지스터에 있어서는 5×10^{17}의 드레인 표면 불순물 농도로 설정하면, 약 5V의 내압이 얻어지게 된다.

다음에, 제14도에 있어서는 드레인 전류에 의해 유기되는 소수 캐리어가 기판측으로 흐르는 기판 전류를 게이트 전압의 함수로써 구하고, 그 최대로 되는 값, 즉 최대 기판 전류를 드레인 확산층 표면 불순물 농도의 함수로서 해석한 것이다.

제14도에서는 찬넬 길이 1.0㎛, 찬넬 폭 10㎛의 MISFET에 관해서 소오스 및 드레인 확산층의 접합 깊이를 파라미터로 하고 , 드레인 전압은 5V이다.

제14도에서 새로이 명확하게 된 사실은 드레인 접합 깊이에 다소 의존하지만 , 드레인 확산층 표면 농도를 10^{17}내지 $10^{18}cm^{-3}$으로 설정하면, 기판전류를 통상구조의 것에 비해서 현저하게 개선할 수가 있어 래치 업 현상을 방지할 수도 있다.

내 래치 업 현상에 대한 최적 표면 불순물 농도의 드레인 확산층 위에 실리사이드층을 형성하면, 음접촉은 얻을 수 없고, 쇼트키 장벽이 형성된다.

본 발명에 있어서는 제13도 및 제14도에서 얻어진 새로운 해석 결과와 상술한 2건의 참고문헌에 따라서 지금까지 없었던 고내압에서 내 래치 업의 초미세 CMOS FET를 실현하였다. 즉, 발명의 CMOSFET에 있어서는 PMOS를 간디 2건의 문헌에 따른 쇼트키 장벽의 드레인 접합으로 형성하고, 한편 NMOS에 대해서는 제13도에서 얻어진 새로운 해석 결과에 따라서 $10^{18}cm^{-3}$이상의 표면 불순물 농도를 갖는 확산층과 음접촉을 갖는 실리사이드등의 조합으로 드레인 접합을 형성하고 있다. 이것에 의하여 내 래치 업 특성 향상 이외의 PMOS 및 NMOS의 각 소오스 드레인 확산층의 표면 불순물 농도를 0.5㎛이하의 초미세 COMSFET의 고내압화의 관점에서 더욱 최적화 하는 것이 가능하게 된다.

[실시예 7]

제15도, 제16도 및 제17도는 각각 본 발병의 제7의 실시예를 도시한 CMOSF ET의 제조공정의 단면 구조도

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이다.

제15도~제17도에 있어서 (221)은 n도전형으로 비저항 0.4Ω.㎝의 실리콘 기판이며, 이 기판(221)의 소정의 위치에 붕소를 접합깊이 2㎛, 표면 불순물 농도 $1\times10^{16}㎝^{-3}$으로 확산하고, P오전형 웰(222)를 형성한다. 다음에 공지의 소자 분리 기술을 이용해서 0.5㎛의 두꺼운 필드 산화막(223)을 선택적으로 형성한 후 활성 영역의 반도체 표면을 노출하고 20㎚의 막의 두께를 갖는 깨끗한 게이트 산화막(28)을 형성한다. 그후, 약 0.4㎛두께의 실리콘 박막을 게이트 산화막(28)위에 형성하고, POC_3을 확산원으로 하는 열확산에 의해 상기 실리콘 각막에 인(P)의 고능도 확산을 행한다. 다음에 상기 실리콘 박막 표면을 열산화 하고 0.2㎛두께의 실리콘 산화막을 상기 실리콘 박막위에 형성한다. 그후, 리도그래피에 의해 상기 실리콘 산화막 및 실리콘 박막을 바라는 회로구성에 따라서 동시에 제거하고, 게이트 보호 절연막(212) 및 게이트 전극(29)를 각각 남겨 놓는다. 그리고, 상기 리도그래피 후의 게이트 전극(29)의 폭 즉, 찬넬폭으로서는 1.0, 0.5, 0.3, 0.2 및 0.1㎛의 5개 조건에 대해서 실시하였다.

상기 리도그래피 후, 테트라 에록시실란($Si(OC_2H_5)_4$)를 사용한 화학 기상 반응에 의해 0.3㎛의 막의 두께를 갖는 실리콘 산화막을 전면적으로 퇴적시킨다. 상기 퇴적막을 반응성 스피터 에칭에 의해 반도체 기판 표면과 수직방향으로 에칭하고, 평탄부에 퇴적된 실리콘 산화 퇴적막을 제거하면 게이트 전극(29) 및 필드 산화막(223)의 각 측벽부분에만 실리콘 산화 퇴적막(213)이 남게 된다. 다음에 0.8㎛두께의 포트 레지스트막을 웰(222)를 제외한 영역의 게이트 산화막(28)위에 남겨 놓고, 가속 에너지 70KeV의 조건에서 비소(As)의 이온주입을 행한다. 상기의 이온주입은 웰 영역(222)에 대해서는 게이트 산화막(28)을 거쳐서 행하여지고, 반도체 기판 표면에서 최대 불순물 농도로 되는 조건이다. 한편, 웰 영역(222)이외에 대해서는 상기 포트 레지스트막에 의해 주입 이온이 저지되어 반도체 기판(221)내에는 주입되지 않는다. 상기의 이온 주입후, 남겨진 포트 레지스트막을 제거하고 나서 주입 이온의 활성화, 열처리를 실시하고, N도 전형의 소오스(24) 및 드레인(25)를 형성한다(이상 제15도).

그리고, 상기의 소오스 및 드레인 확산층(24), (25)의 각각의 표면 불순물 농도는 찬넬 길이가 0.5㎛이상 일때에는 3×10^{18}, 0.3㎛이하 일때에는 $1\times10^{18}㎝^{-3}$으로 최종적으로 형성되도록 비소(As) 이온 양을 설정한다. 도, 상기의 소오스(24), 드레인(25)의 확산층의 접합 깊이가 최종적으로 0.25㎛가 되도록 상기의 열처리 조건을 제어한다. 상기 열처리후, 웰 영역(222)위에만 0.8㎛두께의 포트 레지스트막으로 덮고, 붕소를 가속 에너지 70KeV의 조건으로 이온 주입을 행한다. 상기의 이온 주입에 의해 웰 영역(222) 이외의 영역에 있어서 게이트 산화막(28)을 거쳐서 붕소가 반도체 기판(221)에 주입되고, 그 최대 불순물 농도는 반도체 기판(221)의 표면이었다. 웰 영역(222)에 있어서는 상기 포토 레지스트막에 의해 이온주입이 저지되어 반도체 기판(221)내에 주입되지 않는다. 상기의 이온주입 후, 남겨진 포트 레지스트막을 제거하고 나서 주입 붕소 이온의 활성화 열처리를 실시하고, P도전형의 소오스(26)및 드레인(27)을 형성한다(이상 제16도 참조).

상기 소오스(26) 및 드레인(27)의 확산층의 각각의 표면 불순물 농도는 최종적으로 3종류의 조건 $3\times10^{17}㎝^{-3}$, $1\times10^{18}㎝^{-3}$로 되도록 주입 붕소량을 설정한다. 또, 소오스(26)및 드레인(27)의 확산층의 접합 깊이가 최종적으로 0.25㎛로 되도록 상기의 열처리 조건을 제어한다. 상기 열처리 후, 반도체 기판(221)위에 노출되어 있는 게이트 산화막을 제거하고 나서 50㎚의 막의 두께를 갖는 백금(Pt)을 스피터링 법에 의해 전면에 증착하고, 계속하여 450℃의 열처리를 실시한다. 상기의 저온 열처리에 의해 반도체 기판(221)의 표면에 노출하고 있는 소오스 확산층 영역(24) 및 (26), 드레인 확산층 영역(25) 및 (27)의 각 표면 부분에 백금 실리사이드(PtSi)층(214)가 자기 정합적으로 형성된다. 상기의 열처리에 있어서 필드 산화막(223), 측벽 퇴적 산화막(213) 및 보호 산화막(212)위에서 백금(Pt)은 반응하지 않으므로 실리사이드층(214)는 형성되지 않는다. 상기의 저온 열처리 후, 왕수로 전면적에 백금(Pt)을 에칭한다. 백금 실리사이드(PtSi)는 왕수로 제거되지 않아 소오스 확산층(24) 및 (26)과 드레인 확산층(25) 및 (27)위에만 자기 정합적으로 남게 된다. 이 시점에서는 N도전형의 소오스(24) 및 드레인(25)영역에 있어서의 백금 실리사이드(PtSi)층(214)의 바로 아래에는 백금 실리사이드층 형성전의 표면 불순물 농도보다도 1자리수 높은 불순물 농도를 갖는 약 10㎚두께의 석출층의 백금 실리사이드(PtSi)층(214)에 대해 자기 정합적으로 형성된다.

백금 실리사이드층(214)형성후, 모노실란(SiH_4)과 산소(O_2)의 화학 기상 반응에 의해 약 500㎚두께의 실리콘 산화막(210)을 전면에 퇴적하고, 소오스(24) 및 (26), 드레인(25) 및 (27)위, 또 게이트 전극(29)위의 접촉구멍을 구성시키는 부분의 상기 실리콘 산화막(210)를 리도그래피에 의해 선택적으로 제거한다. 상기의 실리콘 산화막(210)의 선택적 제거를 한 후, 상기 공정에 사용한 포트 레지스트막을 남겨둔 채, 티타늄(Ti)와 텅스텐(W)의 동시 스퍼터에 의해 TiW 막(215)를 전면에 피착시킨다. 그후, 상기 포토 레지스트막을 제거하지만, 이 공정에 의해 포트 레지스트막 위의 TiW막도 동시에 제거되기 때문에 실리콘 산화막(210)이 제거된 영역에만 선택적으로 TiW막(215)가 남게 된다. 최후로 바라는 회로구성에 따라서 알루미늄(Al)에 의한 배선(211)을 형성한다(이상 제17도 참조).

그리고, TiW막(215)는 알루미늄 배선(211)과 실리사이드층(214)의 반응을 방지하기 위해서 필요하게 된다.

다음에, 상기 제조 공정에 의해서 제조된 CMOSFET에 관하여 우선, 소오스와 드레인 사이의 내압을 측정하였을때, 다음의 결과를 얻었다. 즉, P도전형의 소오스(26) 및 드레인(27)의 각 확산층에 있어서의 표면 불순물 농도를 $3\times10^{37}㎝^{-3}$으로 설정한 PMOS에 있어서는 쇼트키 특성을 나타내지만, 찬넬 길이가 0.2㎛이상의 MOSFET의 내압은 약 5V의 값을 얻을수가 있었다. 이 값은 P전형 드레인 표면 불순물 농도가 $10^{18}㎝^{-3}$이상에서 구성되는 종래 구조의 MOSFET에 있어서의 내압의 2배 이상의 값이다. P도전형 드레인 표면 불순물 농도를 $1\times10^{18}㎝^{-3}$으로 설정한 PMOS에 있어서는 P+N접점에 따른 트랜지스터 특성을 표시하지만, 그 소오스와 드레인 사이의 내압은 찬넬 길이가 0.3㎛이상의 MOSFET에 있어서 6.5 내지 7V로 되었다. 이

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값은 종래의 값에 비해서 1.6 내지 1.7배 이며, 고내압화가 실현된 것을 나타내고 있다. 또, P도전형 드레인 표면 불순물 농도를 $3\times10^{18}cm^{-3}$로 설정한 PMOS있어서도 P+N접합에 따르는 특성을 나타내지만, 그 소오스와 드레인 사이의 내압은 찬넬 길이가 0.5㎛이상의 MOSFET에 있어서는 약 12V로 되었다. 이 값을 종래의 값에 비해서 2V이상 높고, 고내압이 실현되게 된다.

N도전형의 소오스(4) 및 드레인(5)의 각 확산층에 있어서의 표면 불순물 농도를 $3\times10^{18}cm^{-3}$으로 설정한 NMOS에 있어서 찬넬 길이가 0.5㎛이상의 MOSFET에 있어서는 그 소오스와 드레인 사이의 내압은 약 10V이었다. 이 값 은 종래의 값에 비해서 약 2배의 값이며, 고내압화가 되게 된다. 드레인 표면 불순물 농도를 $1\times10^{18}cm^{-3}$으로 설정한 NMOS에 있어서도 소오스(24) 및 드레인(25)와 실리사이드층(214)의 사이에는 양호한 음특성이 확보되어 P+N 접합에 따흐는 트랜지스터 특성이 얻어졌다. 그 소오스와 드레인 사이의 내압은 찬넬 길이에 의존하고, 찬넬 길이가 0.3㎛MOSFET에서는 약 3V로 되었다. 이들의 값은 종래 구조의 NMOS에 있어서의 소오스와 드레인 사이의 내압에 비해서 2배 이상의 고내압화로 된다.

본 실시예에 따른 CMOSFET에 있어서의 NMOS 및 PMOS의 소오스와 드레인 사이의 내압은 제13도에 도시한 해석결과의 매우 잘 일치하고 있으며, 상기 해석의 타당성이 증명되게 된다. 즉, 본 실시예에 의하면 0.5㎛이하의 찬넬 길이를 갖는 초미세 CMOSFET의 소오스와 드레인 사이의 내압을 종래에 비해서 2배이상 향상시킬 수가 있다. 구체적으로는 찬넬 길이가 0.5㎛이상의 CMOSFET에 있어서는 NMOS 및 PMOS의 각 소오스 및 드레인 확산층 표면 불순물 농도를 $3\times10^{18}cm^{-3}$으로, 찬넬 길이가 0.3㎛일때에는 상기 불순물 농도를 $1\times10^{18}cm^{-3}$로 설정해서 본 실시예에 따라 MOSFET를 완성시키면, 각각 10V 및 6V의 고내압 초미세 COMSFET를 얻을 수가 있다. 또, 찬넬길이가 0.2㎛일때에는, PMOS의 소오스 및 드레인 확산층이 표면 불순물 농도를 $3\times10^{17}cm^{-3}$으로, NMON의 상기 표면 불순물 농도를 $1\times10^{18}cm^{-3}$에 각각 설움직여써하고, 본 실시에에 따라서 MOSFET를 완성시키면, 소오스와 드레인 사이의 내압 3V의 초미세 CMOSFET를 얻을 수가 있다. 상기의 MOSFET에 있어서 POMS의 소오스(26) 및 드레인 (27)과 실리사이드층(214)의 사이에는 쇼트키 장벽이 형성되지만, 특성상 문제로 되지 않는다. 이 쇼트키 장벽은 오히려 내 래치 업 특성을 향상시키는 기능을 갖추고 있다.

다음에, 본 실시에에 표시한 제조 공정에 의해 제조된 CMOSFET에 대해서 내 래치 업 특성을 평가한다. 내 래치 업 특성으로서는 다음의 것을 측정한다. 즉, NMOS의 드레인(25)를 에미터, 웰(22)를 베이스, 반도체 기판(21)를 콜렉터로 하는 기생 NPN트랜지스터의 전류 이득률 βN과 PMOS의 소오스(26)을 에미터, 반도체 기판(21)을 베이스, 웰(22)를 콜렉터로 하는 기생 PNP트랜지스터의 전류 이득률 βP와의 곱 βN · βP를 측정하였다. 이 측정에서는 베이스와 콜렉터 사이에 5V의 전압을 인가하고, 10^{-6}내지 10^{-2}A의 범위의 에미터 전류의 함수로서 βN · βP를 구하였다. 그 결과, PMOS 및 NMOS의 각 드레인 표면 불순물 농도가 $3\times10^{18}cm^{-3}$ 찬넬 길이가 0.5㎛의 CMOSFET상기 각 드레인 표면 불순물 농도가 $1\times10^{18}cm^{-3}$ 찬넬 길이가 0.3㎛의 CMOSFET 및 PMOS의 드레인 표면 불순물 농도가 $3\times10^{17}cm^{-3}$, NMOS의 상기 표면 불순물 농도가 $1\times10^{18}cm^{-3}$ 찬넬 길이가 0.2㎛의 CMOSFET에 있어서의 각 βN · βP의 곱의 최고 값은 모두 10^{-2} 내지 10^{-4}이었다. 상기의 값은 래치 업이 발생할 수 있는 조건 βN · βP> 1을 만족시킬수 있는 것은 아니며, 또 ,PMOS의 드레인을 쇼트키 접합으로, NMOS의 드레인을 통상의 높은 불순물 농도 N+P접합으로 구성한 CMOSFET에 있어서의 βN · βP 곰의 값 10^{-2}와 거의 같던가 그 이하의 값이다. 상기의 결과에서 PMOS의 드레인 확산층을 낮은 불순물 농도로 설정한 COMSFET에 있어서는 내 래치 업의 관점에서 오히려 소오스와 드레인 사이의 내압의 향상의 관정에 있어서 NMOS의 드레인 표면 불순물 농도의 최적조건을 바라는 찬넬 길이에 따라서 설정하면 좋은 것으로 된다.

다음에 본 실시에에 의한 CMOSFET에 있어서 NMOS 및 PMOS의 각 드레인 표면 불순물 농도를 5×10^{18}내지 $10^{20}cm^{-3}$으로 설정한 찬넬 길이 0.2 내지 1.0㎛의 COMSFET도 동시에 제조하고, 그 소오스와 드레인 사이의 내압 및 내 래치 업 특성을 측정하였다. 상기 COMSFET의 소오스 드레인 사이의 내압은 종래의 값보다 최대 수 V로 개선되고, 또 βN · βP곱도 1이하이었지만, 상술의 결과에 비하면 약간 뒤떨어지는 특성이었다.

[실시에 8]

제18도 및 제19도는 본 발명의 제8의 실시예를 도시한 CMOSFET의 제조 공정의 단면 구조도이다.

제15도에 도시한 상술한 제7의 실시에에 있어서 실리콘 산화 퇴적막(213)를 게이트 전극(29)및 필드 산화막(23)의 측벽부에만 자기 정합적으로 남겨둔 후, 노출되어 있는 게이트 산화막을 완전히 제거한다. 다음에, 지클로루실탄(SiH_2Cl)과 염산(HCL)의 화학기상반응을 775℃의 온도로 행하고, 0.3㎛의 두께의 다결정질 또는 비정질의 실리콘 박막(216)을 웰(222)표면위 및 N도전형을 유지하고 있는 반도체 기판(21) 표면 위에 선택적으로 퇴적시킨다(이상 제18도 참조). 상기 실리콘 퇴적막의 형성조건은, 지클로루실란200cc, 염산 60cc의 조건으로 퇴적속도는 10㎚/분이다. 이 조건에 있어서는 피퇴적 표면에 실리콘 질화막(Si_3N_4)이 존재하지 않는 한 실리콘 기판 위에만 선택적으로 퇴적하고, 또 측벽 절연막(213)과의 경계부에 있어서도 소위 파셋(facet)이라 하는 오목 볼록이 없는 평탄한 현상을 얻을 수가 있다.

실리콘 박막(216)의 퇴적후, 웰 영역(222)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 포토 레지스트막을 선택적으로 형성하고, 붕소 이온 주입을 실시한다. 붕소 주입량은 상기 실리콘 박막(216)내의 불순물 농도가 웰 (222)표면의 불순물 농도와 일치하도록 설정한다. 주입 에너지는 25KeV이다. 그후, 이온 주입의 마스크에 사용한 포토 레지스트막을 제거하고 나서 1150℃, 15초의 조건으로 고온 단시간 열처리를 실시하고, 주입 이온의 활성화와 실리콘 박막(216)의 단결정화를 행한다. 사전에 다결정질, 또는 비정질로 형성된 실리콘 박막(216)내에 있어서 불순물의 확산 계수는 단결정 실리콘 내에 있어서의 확장 계수에 비해서 10 내지 20배나 크다. 따라서, 상기의 단시간 열처리에 의해 웰(222)위의 실리콘 박

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막(216)에 주입된 붕소는 실리콘 박막(216)내에서 깊이 방향에 대해 대략 균일하게 분포한다. 상기 열처리를 한 후, 상술의 제7의 실시예에 따라서 N도전형의 소오스(24) 및 드레인(25)와 P도전형의 소오스(26) 및 드레인(27)을 형성한다. 상기의 단시간 고온 열처리에 의해 실리콘 박막(216)은 이미 단결정화 되어 있다. 따라서, 상기의 각 소오스 및 드레인의 형성 조건은 상기 제7의 실시예의 경우와 같은 조건으로 실시된다. 그후의 공정도 상술한 제7의 실시예에 따라서 CMOSFET를 제조한다(이상 제19도 참조).

제19도에 표시한 제8실시에 따른 CMOSFET는 상술한 제7의 실시예에 따른 CMOSFET와 동일 치수를 갖고 있으며, 양자의 소오스와 드레인 사이의 내압을 비교하였을때, 찬넬 길이 0.3㎛, 소오스 및 드레인 표면 불순물 농도 $1\times10^{18}cm^{-3}$의 조건에 있어서의 제8실시에의 CMOSFET의 쪽이 약 1V만큼 높고, 7V의 내압이 얻어졌다. 또, 찬넬 길이 0.2㎛, NMOS 및PMOS의 드레인 표면 불순물 농도가 각각 $1\times10^{18}cm^{-3}$ 및 $3\times10^{17}cm^{-3}$의 조건으로 구성된 제8실시에의 CMOSFET의 내압을 측정하고, 상술한 제7실시에의 CMOSFET의 내압과 비교하였을때, 전자의 쪽이 약 2V높은 5V의 값을 얻었다. 상기의 값은 종래 구조에 따른 CMOSFET의 소오스, 드레인 사이의 내압과 비교해서 3배 이상의 고내압화를 실현한 것으로 된다. 제8의 실시에에 따르는 CMOS FET에 있어서 기생 바이폴라 트랜지스터에 관한 전류 이득률의 곱 βN · βP를 여러가지의 찬넬 길이, 소오스 및 드레인 표면 불순물 농도를 갖는 경우에 대해서 측정하였으나, 모두 상술의 제7실시에에 따른 CMOSFET의 측정값에 비해서 2/3 내지 1/2로 저감화 되어 있었다. 이와 같이, 제8실시에에 따른 CMOSFET는 제7실시에에 따른 CMOSFET보다 소오스와 드레인 사이의 내압 및 내 래치 업 특성에 있어서 향상하고 있지만, 그 이유는 소오스 및 드레인의 각 접합이 반도체 박막(216)내에 설치된 것에 의해 접합 면적이 저하하고, 또한 실효 찬넬 길이가 증가하였기 때문이라고 생각된다.

[실시에 9]

제20도 및 제21도는 본 발명의 제9의 실시예를 표시한 CMOSFET의 단면구조도와 N도전형의 드레인 확산영역에서의 깊이 방향에 관한 불순물 농도 분포도이다.

제18도에 도시한 제8실시에에 있어서 다결정질, 또는 비정질의 실리콘 박막(216)을 반도체 기판(221)위에 자기 정합적으로 퇴적시킨 후, 웰 영역(222)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 다른 영역 표면위에 포토 레지스트막을 남겨 놓는다. 그후, 웰 영역9222)위의 실리콘 박막 부분에 비소의 이온 주입을 행하고 나서 상기의 남겨진 포트 레지스트막을 제거한다.

다음에, 웰 영역(222)를 포토 레지스트막으로 덮고, 웰 영역(222)이외의 N도전형을 갖는 반도체 기판(221)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 재차 포트 레지스트막을 남겨 놓는다. 그후, 붕소를 이온 주입하고, 재차 포토 레지스트막을 완전히 제거해서 실리콘 박막(216)의 표면을 노출시킨다. 이상태에서 1100℃, 30초의 조건의 단시간 고온 열처리를 실시한다. 상기 조건의 열처리을 행하여도 실리콘박막(216)은 단결정화 되지 않고, 다경정질 또는 비정질의 상태를 유지하고 있다. 다결정질, 또는 비정질의 실리콘 박막(216)내에 있어서의 불순물의 확산 계수는 상술과 같이 매우 큰 값이기 때문에 상기 조건에 의한 단시간 열처리에 의해서 실리콘 박막(216)내에서 비소 및 붕소는 고속으로 거의 균일한 농도 분포로 된다. 그러나, 반도체 기판(21)내에 있어서의 각 불순물의 확산 계수는 상대적으로 작고, 상기 단시간의 열처리에 의해서는 반도체 기판(21)내에 약 20㎚정도밖에 확산되지 않았다.

이와 같이 비소 및 붕소의 이온 주입과 그에 따르는 단시간 열처리에 의해 실리콘 박막(216)과 웰(222) 및 N도전형 반도체 기판(221)내에 각각 N도전형의 소오스(24)와 드레인(25) 및 P도전형의 소오스(26)과 드레인(27)을 형성한다. 그후, 상기 각 소오스(24) 및 (26)과 드레인(25) 및 (27)위에 백금 실리사이드(PiSi)층(214)를 상술의 제7의 실시에에 따라서 자기 정합적으로 형성하고, 그후의 공정도 제7의 실시에에 따라서 실시하는 것에 의해 제20도에 도시한 CMOSFET를 제조할 수가 있다.

제9실시에에 의한 CMOSFET의 N도전형 소오스(24) 및 드레인(25)의 불순물 농도 분포는 제21도에 도시한 바와 같이 3개의 영역 A, B, C로 분리된다. 즉, 실리사이드층(214)바로 아래에 있어서의 약 10㎚두께의 불순물 석출 영역A, 실리콘 박막(216) 내부의 균일 분포 영역 B 및 웰9222)내에 있어서의 접합 깊이 약 20㎚를 갖는 급격한 농도 분포 영역 C이다. P도전형 소오스(26) 및 드레인(27)내에 있어서는 상기 불순물 석출 영역 A의 존재는 인정되지 않았다.

제9실시에에 따른 CMOSFET에 있어서는 상기 실리콘 박막(216)내의 균일 분포 농도로서, NMOS에 관해서는 $1\times10^{18}cm^{-3}$, $3\times10^{18}cm^{-3}$, $10^{19}cm^{-3}$, $5\times10^{19}cm^{-3}$의 각 값이, 또 PMOS에 관해서는 $1\times10^{17}cm^{-3}$, $3\times10^{17}cm^{-3}$, $1\times10^{18}cm^{-3}$, $3\times10^{18}cm^{-3}$ 및 $5\times10^{18}cm^{-3}$의 값이 최종적으로 되도록 비소 또는 붕소 이온 주입량을 설정하는 것에 의해서 MOSFET를 제조하였다. 또, 찬넬 길이에 관해서도, 0.1, 0.2, 0.3, 0.5 및 1.0㎛의 값 일 때에 대해서 MOSFET를 제조하였다. 상기 각종의 CMOSFET에 대해서 소오스와 드레인 사이의 내압 및 기생 바이폴라 트랜지스터의 각 전류 이득률의 곱 βN · βP를 측정하였다. NMOS의 드레인(27)내의 균일 분포 불순물 농도가 $10^{18}cm^{-3}$이상 일 때, 상기 특성 향상은 그다지 확인되지 않았다. 그러나, 상기 균인 분포 불순물 농도가 10^{17} 내지 $10^{19}cm^{-3}$의 낮은 불순물 농도로 설정되어 있을 때에는 특히 소오스와 드레인 사이의 내압의 향상이 현저하였다. 드레인 내의 균일 분포 불순물 농도가 $1\times10^{18}cm^{-3}$일 때 찬넬 길이가 0.1 및 0.2㎛의 각 CMOSFET에 있어서의 소오스와 드레인 사이의 내압은 각각 4.5 및 8 V에 달하였다. 이들이 값은 제8의 실시에에 따른 CMOSFET일 때에 비해서도 많이 개선되어 있으나, 이 효과는 찬넬 길이가 짧은 경우의 쪽이 상대적으로 현저하였다. PMOS에 있어서의 드레인(25) 내의 균일 분포 불순물 농도가 10^{17} 내지 $10^{18}cm^{-3}$미만으로 설정되고, 또한 게이트 길이가 0.1㎛일때에도 소오스와 드레인 사이의 내압은 제8의 실시에 일 때와 비교해서 수 V 향상되고 있으며, 그 값은 5V 이상에 달하였다.

제9의 실시에와 제8의 실시에에 있어서의 이 효과의 차이는 드레인 최대 전계가 인가되는 낮은 불순물 농도 영역이 제9실시에일 때에는 실리콘 박막(216)내에서 제21에 도시한 바와 같이 대략 균일하게 형성

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되기 때문이고, 그에 의한 전계분산 효과가 된다고 생각된다.

또, 제9실시예에 따른 초미세 CMOSFET의 기생 바이폴라 트랜지스터의 곱 βN · βP에 관해서는 제8실시예의 경우와 거의 변함이 없고, 래치 업 현상은 무시할 수 있는 정도이었다.

본 발명의 제1내지 제6의 실시예에 의하면, 최대 전계인가 영역이 드레인 확산층내에서 넓게 분산할 수 있으므로, 동일 구조 파라미터를 갖는 종래 구조의 트랜지스터 보다 5V이상이나 소오스와 드레인 사이의 내압을 향상할 수 있다. 따라서, 본 발명에 의하면 전원 정압을 종래의 5V에서 3V이하로 내리는 것과 같은 변경도 없이 실효 찬넬 길이가 0.5㎛이하의 미세 트랜지스터를 동작시킬수가 있다.

본 발명의 제1 내지 제3의 실시예에 있어서는 PtSi층의 형성시에 있어서의 PtSi층 바로 밑의 불순물의 석출 효과를 이용해서 음 접촉에 필요한 불순물 농도 영역을 PtSi층과 자기 정합의 관계로 구성하였으나, 상기의 PtSi층은 Mo, W, Pb, Ni, Ti, Ta, Nb, Cr, Pr등의 다른 고융점 금속 또는 그들의 실리사이드막으로 치환해서 구성하여도 지장이 없다. 또, 본 발명의 각 실시예에 있어서는 소오스 및 드레인 확산층을 P이온에 의해 형성한 이를 도시하였으나, 상기 확산층은 P이온에 의해서 형성하여도 좋다. 또, 그 형성 방법도 이온 주입에 한정되는 일없이 열 확산법 등 다른 공지의 수단에 의해서도 본 발명의 요지를 이탈하지 않는다. 또, 본 발명은 상기와 같은 단일체 트랜지스터에 한정되는 일이 없이 반도체 집적회로 장치에 대해서도 적용된다.

또, 제7 내지 제9도의 실시예에 의한 효과는 종래 구조에 있어서의 소오스와 드레인에 대응하는 영역을 개선하는 것에 의해 얻어지는 것으로, 결코 반도체 기판(221)의 농도를 증대시켜서 고내압화를 도모하는 것은 아니다. 따라서, 반도체 기판 농도의 증대에 따르는 이동도의 저하를 조래하는 일도 없고 고속 동작을 손상하는 일도 없다.

본 발명의 제7 내기 제9의 실시예에 의하면, 소오스 및 드레인 위에 고융점 금속 또는 그 실리사이드층이 형성되어있기 때문에 초미세 CMOSFET에 있어서도 그 시이트 저항는 수Ω/㎠으로 낮은 저항성을 유지할 수 있어 고속 동작을 보장할 수가 있다.

제7~제9의 각 실시예에 있어서는 소오스 및 드레인 확산층의 최대 불순물 농도에 관하여 $1\times10^{17}cm^{-3}$이상일 때에 대해서 기술하였으나, 이것은 제13도의 해석 결과 즉, 0.1㎛의 게이트 길이에 대하여서의 해석 결과에 따르고 있다. 0.1㎛의 값은 실현할 수 있는 최소의 게이트 길이이다. 또, 상기의 불순물 농도($1\times10^{17}cm^{-3}$)이하에서 본 발명을 적용할 때에 제14도에서 추측할 수 있는 바와 같이 기판 전류의 증대 및 드레인 누설 전류의 증대를 초래하게 되는 것이다.

또, 제7~제9의 각 실시예에 있어서는 소오스 및 드레인 확산층 위에 백금 실리사이드(PtSi)층을 자기 정합적으로 형성하였으나, 이것은 일예로서 이 PtSi층 대신에 Mo, W, Pb, N, Ti, Ta, Nb, Cr, Pr등의 고융점 금속 또는 그 실리사이드 막을 사용할 수가 있다. 또, 각 실시예에 있어서는 단시간 열처리로서 고온 전기로를 사용하는 방법에 대해서 설명하였으나, 이 공정은 램프가열법, 레이저 또는 전자선 조사법 등의 다른 방법에 의해서도 가능하다. 또, 각 실시예에 있어서는 P도전형 웰을 사용한 경우에 대해서 설명하였으나, 역으로 P도전형 반도체 기판내에 N도전형의 웰을 형성한 구조의 CMOSFET에 대해서도 본 발명을 적용할 수가 있다.

이상 설명한 바와 같이 본 발명에 의하면, 0.2㎛의 극히 짧은 찬넬 길이라도 5V의 통상 전원으로 동작시킬수가 있고, 또 래치 업 현상을 방지할 수 있기 때문에 고속 동작을 손상시키는 일없이 초미세 CMOSFET를 실현하는 것이 가능하다.

(57) 청구의 범위

청구항 1

전계 효과 트랜지스터에 있어서, 반도체 기판(1)과 반대 도전형의 드레인(5) 또는 소오스(6) 영역에 있어서 최대 불순물 농도가 $10^{18}cm^{-3}$이상 $10^{20}cm^{-3}$미만으로 구성되고, 상기 드레인 또는 소오스 영역표면의 적어도 일부는 고융점 금속층 또는 그 실리사이드층(12)와 50㎚을 초과하지 않는 두께를 갖는 높은 불순물 농도 영역(16)으로 되는 높은 도전층과 접하고 있는 것을 특징으로 하는 반도체 장치.

청구항 2

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 높은 도전층이 고융점 금속층 또는 그 실리사이드층(12)만으로 구성되어 있는 것을 특징으로 하는 반도체 장치.

청구항 3

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 드레인(5) 또는 소오스(6)영역의 적어도 일부가 게이트 전극(4)아래에 존재하는 것을 특징으로 하는 반도체 장치.

청구항 4

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 드레인(5) 또는 소오스(6)영역의 적어도 한쪽이 적어도 2회의 이온 주입에 의해서 형성되는 것을 특징으로 하는 반도체 장치.

청구항 5

특허청구의 범위 제3항 기재의 전계 효과 트랜지스터에 있어서, 상기 게이트 전극(4)가 Mo 박막 또는 실리콘 박막으로 구성되는 것을 특징으로 하는 반도체 장치.

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청구항 6

특허청구의 범위 제3항 기재의 전계 효과 트랜지스터에 있어서, 상기 게이트 전극(4)의 측벽부에 비유전율이 실리콘 산화막 보다 높은 게이트 측벽 절연막(19)를 형성하여 되는 것을 특징으로 하는 반도체 장치.

청구항 7

특허청구의 범위 제6항 기재의 전계 효과 트랜지스터에 있어서, 상기 측벽 절연막(19)를 실리콘 질화막으로 구성한 것을 특징으로 하는 반도체 장치.

청구항 8

불순물 확산 영역의 최대 불순물 농도가 10^{18} 내지 $10^{20}cm^{-3}$정도의 N형 드레인(24) 또는 소오스 영역(25)와 최대 불순물 농도가 10_1^7 내지 $10^{19}cm^{-3}$정도의 P형 드레인(26) 또는 소오스 (27)영역을 가지며, 또 상기 각 드레인 또는 소오스 영역의 적어도 일부가 고융점 금속 또는 금속의 실리사이드층(214)와 접합되어 구성되고 있는 것을 특징으로 하는 반도체 장치.

청구항 9

특허청구의 범위 제8항에 있어서, 상기 각 드레인(24, 26) 또는 소오스 (25, 27)영역의 일부는 반도체 기판 표면 위에 절연막(28)을 거쳐서 구성된 게이트 전극(29)와 상기 게이트 전극의 측벽에 형성된 절연막(213)을 거쳐서 인접해서 형성되는 반도체 장치.

청구항 10

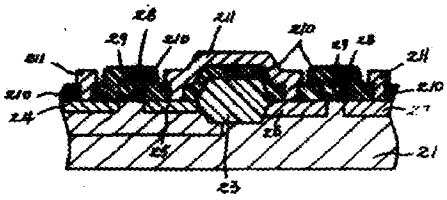
특허청구의 범위 제 8항에 있어서, 상기 N형 드레인(24) 또는 소오스(25)영역은 고융점 금속 또는 그 실리사이드층(214) 바로 아래의 불순물 석출영역(A), 실리콘박막(216)내부의 균일한 분포의 영역(B), 급격한 농도 분포 영역(C)의 3개의 불순물 농도 분포 영역을 수직 방향으로 갖고 있는 반도체 장치.

청구항 11

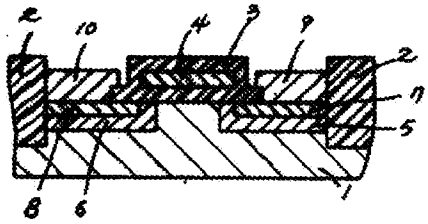
특허청구의 범위 제9항에 있어서, 상기 각 드레인(24, 26) 또는 소오스(25, 27)영역의 일보는 다결정 박막 또는 비정질 박막(216)으로 형성되는 반도체 장치.

도면

도면1

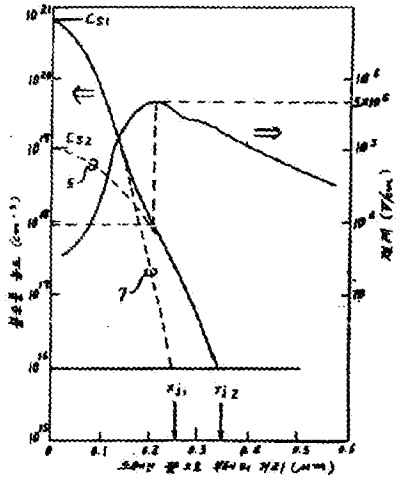


도면2a

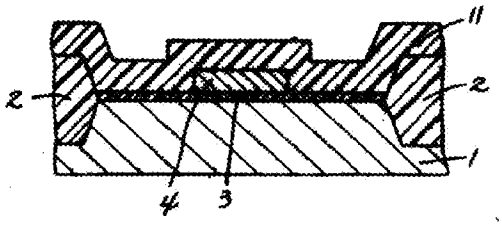


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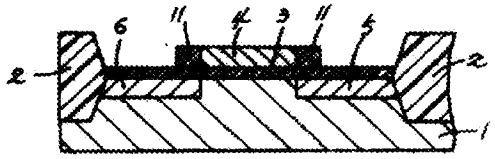
도면2b



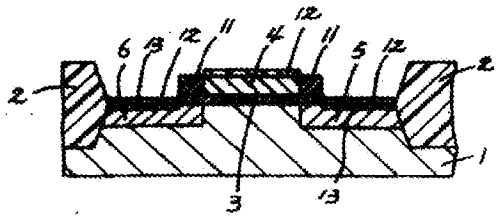
도면3



도면4

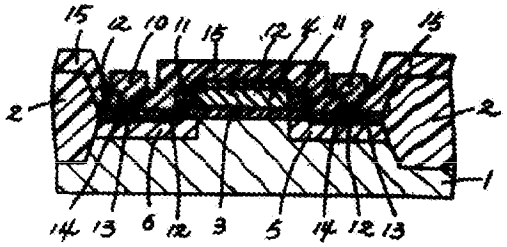


도면5

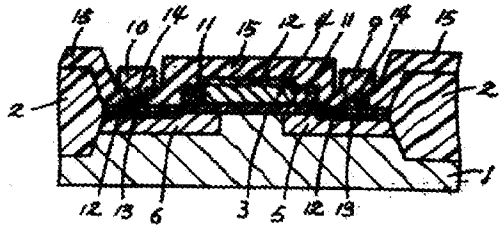


GF Exhibit 1126 - 1709/2248

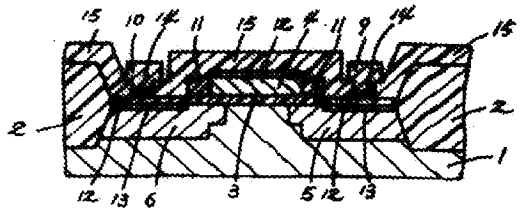
도면6



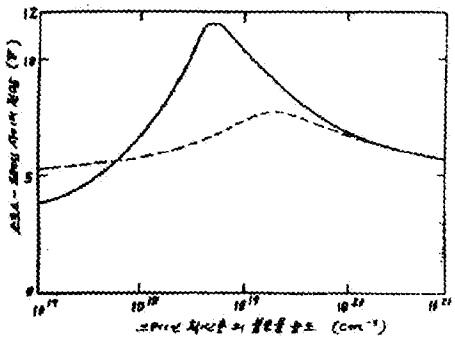
도면7



도면8

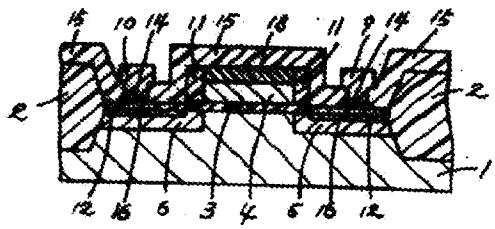


도면9

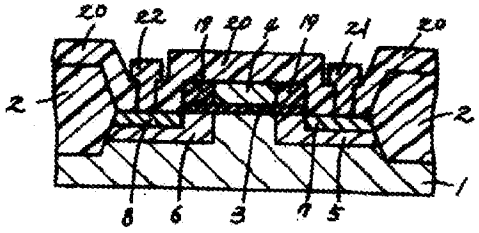


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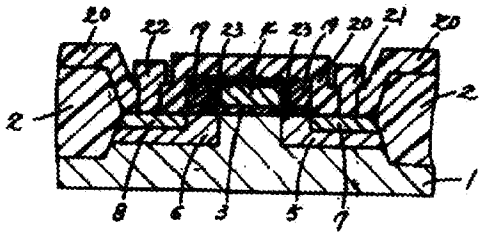
도면10



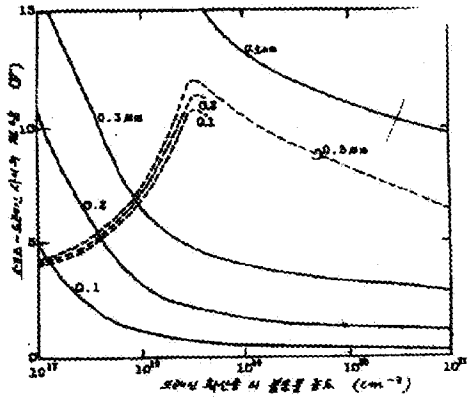
도면11



도면12

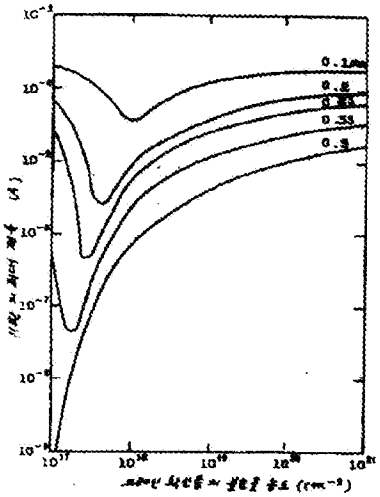


도면13

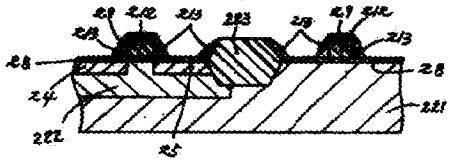


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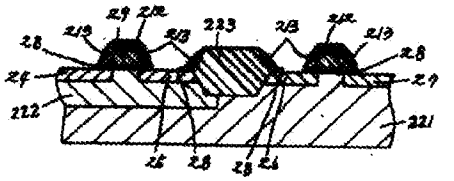
도면14



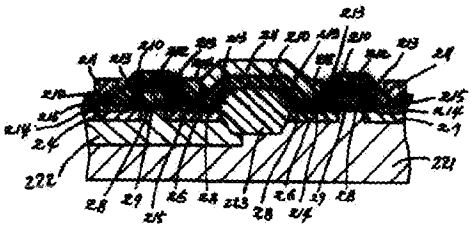
도면15



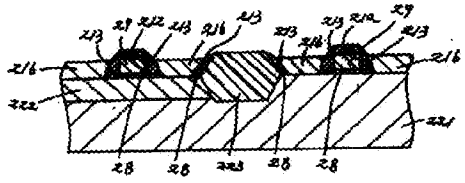
도면16



도면17

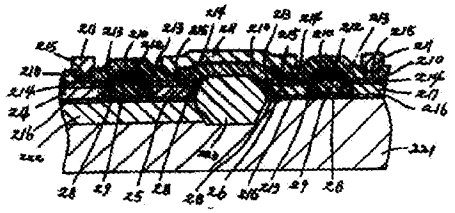


도면18

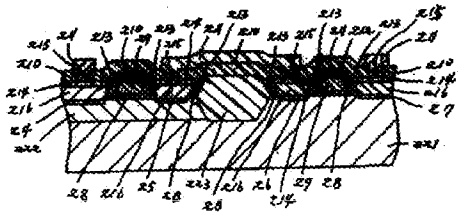


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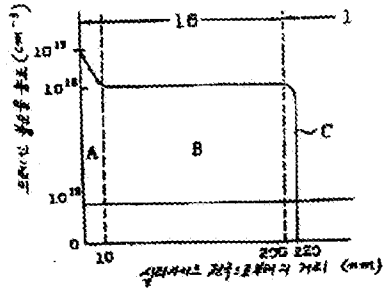
도면19



도면20



도면21



GF Exhibit 1126 - 1713/2248

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Agent.	PAIK, Nam Ki
Inventor	HoRiUJiMaSaDaTa | YaMaGuJiGen
Applicant	HITACHI, LTD.
Rightholder	HITACHILTD CO., LTD

발명의 명칭

반도체장치

Title of Invention

Semiconductor device.

요약

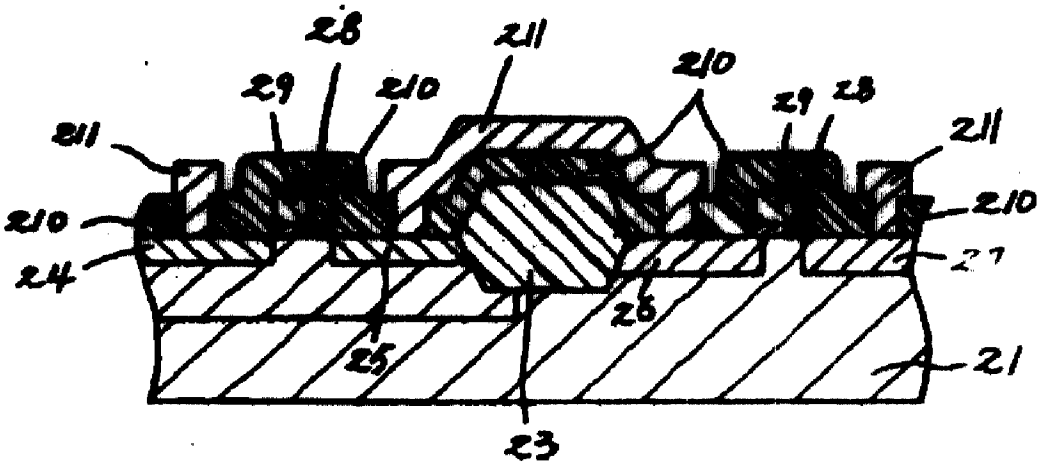
내용 없음.

Abstract

Content none.

대표도면(Representative drawing)

GF Exhibit 1126 - 1714/2248



청구의 범위

청구 1항:

전계 효과 트랜지스터에 있어서, 반도체 기판(1)과 반대 도전형의 드레인(5) 또는 소오스(6) 영역에 있어서 최대 불순물 농도가 1018㎝-3이상 1020㎝-3미만으로 구성되고, 상기 드레인 또는 소오스 영역표면의 적어도 일부는 고융점 금속층 또는 그 실리사이드층(12)와 50㎚을 초과하지 않는 두께를 갖는 높은 불순물 농도 영역(16)으로 되는 높은 도전층과 접하고 있는 것을 특징으로 하는 반도체 장치.

청구 2항:

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 높은 도전층이 고융점 금속층 또는 그 실리사이드층(12)만으로 구성되어 있는 것을 특징으로 하는 반도체 장치.

청구 3항:

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 드레인(5) 또는 소오스(6)영역의 적어도 일부가 게이트 전극(4)아래에 존재하는 것을 특징으로 하는 반도체 장치.

청구 4항:

특허청구의 범위 제1항은 기재의 전계 효과 트랜지스터에 있어서, 상기 드레인(5) 또는 소오스(6)영역의 적어도 한쪽이 적어도 2회의 이온 주입에 의해서 형성되는 것을 특징으로 하는 반도체 장치.

청구 5항:

특허청구의 범위 제3항 기재의 전계 효과 트랜지스터에 있어서, 상기 게이트 전극(4)가 Mo 박막 또는 실리콘 박막으로 구성되는 것을 특징으로 하는 반도체 장치.

청구 6항:

Scope of Claims

Claim 1:

The semiconductor device the maximum impurity concentration consists of 10 20 ㎝ - 3 under as to the field effect transistor as to the drain (5) of the semiconductor substrate (1) and opposite conductive or the source (6) domain over 10 18 ㎝ - 3 ; and for contacting with the high conductive layer consisting of the high concentration domain of impurities (16) having the thickness in which at least a part of the drain or the source area surface does not exceed the metal layer or the silicide layer (12) and 50㎚.

Claim 2:

The semiconductor device in which the above-mentioned high conductive layer the scope of claims claim 1 consists of the metal layer or the silicide layer (12) as to the field effect transistor of the material.

Claim 3:

The semiconductor device in which the scope of claims claim 1 at least a part of the drain (5) or the source (6) domain exists as to the field effect transistor of the material under the gate electrode (4).

Claim 4:

The semiconductor device in which the scope of claims claim 1 at least one side of the drain (5) or the source (6) domain is formed by the ion implantation of at least two times as to the field effect transistor of the material.

Claim 5:

The gate electrode (4) as to the field effect transistor of the scope of claims claim 3 material is the Mo thin film or the semiconductor device for consisting of the silicon thin film.

Claim 6:

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특허청구의 범위 제3항 기재의 전계 효과 트랜지스터에 있어서, 상기 게이트 전극(4)의 측벽부에 비유전율이 실리콘 산화막 보다 높은 게이트 측벽 절연막(19)를 형성하여 되는 것을 특징으로 하는 반도체 장치.

The semiconductor device for the relative permittivity forming the gate sidewall insulation film (19) higher tha n the silicon oxide film on the sidewall part of the gate electrode (4) as to the field effect transistor of the sc ope of claims claim 3 material and becoming.

청구 7항:

Claim 7:

특허청구의 범위 제6항 기재의 전계 효과 트랜지스터에 있어서, 상기 측벽 절연막(19)를 실리콘 질화막으로 구성한 것을 특징으로 하는 반도체 장치.

The semiconductor device for organizing the side wall insulating film (19) on the silicon nitride film as to the fi eld effect transistor of the scope of claims sixth claim materials.

청구 8항:

Claim 8:

불순물 확산 영역의 최대 불순물 농도가 1018 내지 1020㎝-3정도의 N형 드레인(24) 또는 소오스 영역(25)와 최대 불순물 농도가 1017 내지 1019㎝-3정도의 P형 드레인(26) 또는 소오스 (27)영역을 가지며, 또 상기 각 드레인 또는 소오스 영역의 적어도 일부가 고융점 금속 또는 금속의 실리사이드층(214)와 접합되어 구성되고 있는 것을 특징으로 하는 반도체 장치.

The semiconductor device N type drain (24) of 10 18 to about 10 20 ㎝ - 3 or the source area (25) and maxi mum impurity concentration of the maximum impurity c oncentration of the impurity diffusion region has the P- type drain (26) of 10 1 7 to about 10 19 ㎝ - 3 or the s ource (27) domain ; and for and, at least a part of eac h drain or the source area being welded to the silicide l ayer (214) of the high melting point metal or the metal and being formed.

청구 9항:

Claim 9:

특허청구의 범위 제8항에 있어서, 상기 각 드레인(24, 26) 또는 소오스 (25, 27)영역의 일부는 반도체 기판 표면 위에 절연막(28)을 거쳐서 구성된 게이트 전극(29)와 상기 게이트 전극의 측벽에 형성된 절연막(213)을 거쳐서 인접해서 형성되는 반도체 장치.

The semiconductor device for the part of each drain (24, 26) or the source (25, 27) domain being adjacent as to the scope of claims eighth claim after the insulati ng layer (213) formed on the surface of semiconductor substrate after the insulating layer (28) in the sidewall of the gate electrode and the formed gate electrode (2 9) and being formed.

청구 10항:

Claim 10:

특허청구의 범위 제 8항에 있어서, 상기 N형 드레인(24) 또는 소오스(25)영역은 고융점 금속 또는 그 실리사이드층(214) 바로 아래의 불순물 석출영역(A), 실리콘박막(216)내부의 균일한 분포의 영역(B), 급격한 농도 분포 영역(C)의 3개의 불순물 농도 분포 영역을 수직 방향으로 갖고 있는 반도체 장치.

The semiconductor device in which N type drain (24) or the source (25) domain has the high melting point meta l or the silicide layer (214), immediately, the following i mpurity precipitation domain (A), the domain (B) of the uniform distribution of the silicon thin film (216) inside, and the impurity concentration distribution domain of 3 of the sudden concentration distribution domain (C) to that as to the scope of claims eighth claim in the verti cal direction.

청구 11항:

Claim 11:

특허청구의 범위 제9항에 있어서, 상기 각 드레인(24, 26) 또는 소오스(25, 27)영역의 일보는 다결정 박막 또는 비정질 박막(216)으로 형성되는 반도체 장치.

The semiconductor device in which the step of each drain (24, 26) or the source (25, 27) domain is formed as to the scope of claims ninth claim into the polycryst alline thin film or the amorphous thin film (216).

상세설명

Detailed Description

[발명의 명칭]

[Title of invention]

반도체 장치

Semiconductor device.

[도면의 간단한 설명]

[Brief description of drawings]

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제1도는 종래의 CMOS를 도시한 단면도.

Figure 1 is a cross-sectional view showing the conventional CMOS.

제2도는 A는 종래의 이중 드레인 구조를 갖는 MISFET의 단면도.

The cross-sectional view of MISFET in which figure the second A has the drain structure among the conventio nal this.

제3도는 BSMS 제2도의 A의 MISFET의 반도체 표면의 불순물 농도 분포와 그에 있어서의 전계를 해석한 것은 도시한 도면.

Drawing illustrated figure the third interprets the electric field in the impurity concentration distribution o f the semiconductive surface of MISFET of A of the BS MS second drawing and that.

제3도~제6도는 본 발명의 제1의 실시예의 제조 공정을 순으로 도시한 단면도.

The cross-sectional view in which the third figure the sixth shows the manufacturing process of the first emb odiment of the invention to the net.

제7도는 본 발명의 제2의 실시예의 단면도.

Figure the seventh is the cross-sectional view of the embodiment of the second of the invention.

제8도는 본 발명의 제3의 실시예의 단면도.

Figure the eighth is the cross-sectional view of the embodiment of the third of the invention.

제9도는 본발명의 제1의 실시예의 특성을 도시한 도면.

Figure 9 is a drawing showing the property of the first embodiment of the invention.

제10도는 본 발명의 제4의 실시예의 단면도.

Figure the tenth is the cross-sectional view of the embodiment of the fourth of the invention.

제11도는 본 발명의 제5의 실시예의 단면도.

Figure the eleventh is the cross-sectional view of the embodiment of the fifth of the invention.

제12도는 본 발명의 제6의 실시예의 단면도.

Figure the twelfth is the cross-sectional view of the embodiment of the sixth of the invention.

제13도, 제14도는 본 발명의 제7~제9의 실시예의 특성을 표시한 도면.

Drawing in which the thirteenth figure the fourteenth indicates the property of the embodiment of 7~ ninth o f the invention.

제15도~제17도는 본 발명의 제7의 실시예를 제조 공정 순서로 도시한 단면도.

The cross-sectional view in which the 15 figure the seventeenth shows the embodiment of the seventh of the invention to the fabrication sequence.

제18도~제19도는 본 발명의 제8의 실시예를 제조 공정 순서로 도시한 단면도.

The cross-sectional view in which the eighteenth figure the nineteenth shows the embodiment of the eighth of the invention to the fabrication sequence.

제20도는 본 발명의 제9의 실시예의 단면도.

Figure the twentieth is the cross-sectional view of the embodiment of the ninth of the invention.

제21도는 본 발명의 제9의 실시예의 드레인의 깊이 방향의 불순물 농도 분포를 도시한 도면.

Figure 21 is a drawing showing the impurity concentration distribution of the longitudinal direction o f the drain of the embodiment of the ninth of the inven tion.

[발명의 상세한 설명]

[Detailed description of the invention]

본 발명은 MISFET에 관하여, 특히 초미세 MISFET의 고내압화에 가장 적합하고, 내 핫 캐리어 효과가 우수한 MISFET에 관한 것이다.

The present invention relates to MISFET in which it is most suitable for especially, the high voltage-resistant of the ultra-fine MISFET about MISFET and my hot carr ier effect is excellent.

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또한, 본 발명은 CMOSFET에 관하여, 특히 0.5#956#m 이하의 게이트 길이에 있어서도 5V 전원으로 동작가능한 고내압초미세 CMOSFET에 관한 것이다.

Moreover, the present invention relates to the high voltage-resistant ultra-fine CMOSFET which is operable in the drawing 5V power source about CMOSFET as to especially, the gate length less than 0.5μm.

현재, MIS 전계 효과 트랜지스터(이하MISFET라 한다)는 미세화를 위해 게이트 절연막을 얇게 하여, 소오스와 드레인의 간격을 좁게하고, 또한 소오스와 드레인의 접합을 얕게 하려고 하고 있다.

It makes the gate insulating layer the present , and the metal-insulation-semiconductor field effect transistor (it says to be less than MISFET) thin for the miniaturization and it makes the gap of the drain and source narrow and it makes moreover, the junction of the drain and source shallow.

상기의 경황의 결과, 현재의 MISFET에 있어서의 최대의 문제는 소오스와 드레인 사이의 내압의 저하이다. 드레인 측에서 신장해온 공핍층이 소오스 영역에 도달하기 때문에 생긴 소위, 편치 스루 내압의 저하는 기판 농도를 증가하는 것에 의해 피할 수가 있으나, 그와 같이 하는 것에 의해서 역으로 전자사태 항복내압(avalanche effect break down)이 감소하게 된다. 특히, 게이트, 소오스 및 기판 전압을 영으로 하였을때의 전자사태 항복전압(이하, BVDS라 한다)은 게이트 전압에 의해서 기판표면 전위의 증가가 억제되기 때문에 젖합 내압에비해서 극단으로 저하해 버린다. 그 결과, 찬넬 길이 1#956#m, 게이트 산화막의 두께20nm, 소오스 드레인 접합 깊이 0.35#956#m인 미세 MISFET의 소오스와 드레인 사이의 내압은 약6V로 통상의 전원 전압5V에 거의 일치할때까지 저하한다. 상기와 같이 미세 트랜지스터에 있어서는 전원 전압의 변동에 의해 간단히 파괴된다.

The result of the state of things described in the above , and the problem of the maximum in the current MISFET are the degradation of the internal pressure between the source and the drain. By the result of that the degradation of the so-called piece value slew internal pressure which is generated because the depletion layer has been extend in the drain section reaches the source area increases the substrate concentration it can avoid. But the electron avalanche breakdown internal pressure (avalanche effect break down) reduces by doing like that. Especially, because the increase of the substrate surface electric potential is suppressed by the gate voltage the electron avalanche breakdown voltage (it the hereinafter says to be the BV DS) when having gate, and the source and substrate voltage as zero is degraded in comparison with the breast sum total internal pressure to extreme. Consequently, the channel length 1μm, the thickness 20nm of the gate oxidation film , and the internal pressure between the source of the minute MISFET and the drain which is the source drain conjugation depth 0.35μm are degraded until it nearly coincides with the normal power supply voltage 5V to about 6V. As described above, it is in the minute transistor and it is simply destroyed by the change of the power supply voltage.

따라서, 종래의 미세 MISFET에 있어서는 상기의 결점을 극복하기 위해 드레인 구조에 관하여 0.2#956#m 정도의 얕은 접합 깊이를 갖는 고농도 불순물 확산층과 0.35#956#m 정도의 보다 깊은 접합깊이를 갖는 저농도 불순물확산층을 조합시키는 소위, 이중 드레인 구조를 채용하고 있다. 상기 구조에의 BVDS 값을 약 1.5내지 2V 향상시킬 수가 있다. 그러나, 상기의 개량된 미세 MISFET에 있어서는 전원 전압의 변동에 의한 파괴로부터 통상 피할 수가 있다. 그러나, 상기의 개량된 미세MISFET에 있어서도 신뢰성의 관점에서는 아직까지 만족할 수가 없었다.

Therefore, the drain structure is employed among the so-called this combining the highly doped impurity diffusion layer which has the shallow junction depth of about 0.2μm about the drain structure in order to be in the conventional minute MISFET and overcome the defect described in the above, and the lightly doped drain implant diffusion layer having the junction depth which is more deep of about 0.35μm. The BV DS value of the structure can be improved with about 1.5 through 2V. But it is in the improved minute MISFET described in the above and generally it can avoid from the break down by the change of the power supply voltage. But in the viewpoint of the reliability as to the improved minute MISFET described in the above, it could not be so far satisfied.

즉, 통상 조건의 장기간 동작에 있어서는 드레인 근방에 있어서의 강한 전계 효과에 의해 핫 케리어(hot carrier)가 게이트 절연막중에 주입되어 임계 전압 값의 변동, 또 표면준의 밀도의 증대 및 전달 콘덕턴스의 저항 등의 열화가 생긴다.

That is, generally, the deterioration including the resistance of the transfer conductance and increase in the change of the threshold voltage value, and, the density of the Pyo MyeonJun it is in the long period operation of the condition and the hot carrier is injected with the strong field effect in the drain neighborhood among the gate insulating layer etc. comes up.

또, 이상은 MISFET의 단일체에 관한 것이지만, 2개 이상의 트랜지스터를 조합해서 구성한 CMOS(Complementary Metal Oxide Semiconductor) 구조에 있어서도 대략 마찬가지로 적

And over relates to the monolith of MISFET, but it is applied as to the CMOS (Complementary Metal Oxide Semiconductor) structure of assembling at least 2 transi

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용된다. 또, CMOS에서는 다음의 문제도 갖고 있다.

stors and configuring to approximately, the likeness. And in CMOS, the following problem has.

여기서, CMOS는 P 찬넬 MOS(이하 PMOS라 한다)와 N 찬넬 MOS(이하 NMOS라 한다)를 쌍으로 해서 동일칩 위에 형성하고 있는 구조이다.

Here, CMOS is P channel MOS (it the hereinafter says to be PMOS) and the structure of N channel MOS (it the hereinafter says to be NMOS) being to pair and forming on the same chip.

제1도는 2#956#m 이상의 게이트 길이를 갖는 종래의 CMOS의 단면 구조도이다.

Figure 1 is a sectional configuration of the conventional CMOS having the gate length more than 2μm.

제1도에 있어서 (21)은 N 도전형의 반도체 기판, (22)는 반도체 기판(21)내에 형성된 P 도전형의 확산층 영역으로 웰이라 한다. (23)은 필드 산화막, (24) 및 (25)는 웰(22)내에 형성된 NMOS의 소오스 및 드레인 확산층 영역으로 n 도전형을 가지며, 그 최대 불순물 농도는 1020cm-3이상으로 구성된다. (26) 및 (27)은 PMOS의 소오스 및 드레인 확산층 영역으로 P 도전형을 가지며, 그 최대 불순물 농도는 1019cm-3이상으로 구성된다. (28) 및 (29)는 각각 게이트 절연막 및 게이트 전극이다. (210) 및 (211)은 각각 보호절연막 및 소오스 또는 드레인 전극이다.

(21) is done by the diffusion layer area of P conductivity type in which the semiconductor substrate of N conductivity type , and (22) is formed within the semiconductor substrate (21) as to Figure 1 because of being the well. (23) has the n conductivity type to the source and drain diffusion layer domain of NMOS in which the field oxide film , and (24) and (25) are formed within the well (22) and the maximum impurity concentration is formed over 10 20 cm - 3 . (26) (27) has P conductivity type to the source and drain diffusion layer domain of PMOS and the maximum impurity concentration is formed over 10 19 cm - 3 . (28) The respectively (29) is the gate insulating layer and gate electrode. (210) The respectively (211) is the protective insulator film and source or the drain electrode.

이와 같은 드레인 확산층의 불순물농도 구성을 갖는 종래 구조의 CMOS에 있어서는 소자의 미소화에 따라서 여러 가지의 결점이 발생한다.

It is in CMOS having the impurity concentration configuration of this kind of drain diffusion layer of the conventional structure and the defect of the various is generated according to the submicron of the device.

(i) 소오스와 드레인 사이의 내압 저하, 즉 소자가 미소화 되는데 따라 찬넬 길이가 감소하기 때문에 펀치 스루 내압이 저하한다. 펀치 스루 내압의 향상은 기판 농도를 증가하는 것에 의해 달성할 수 있으나, 기판 농도의 증가는 역으로 전자사태 항복 내압이 저하하여 버린다. 찬넬 길이가 0.3#956#m 이하의 매우 미소한 NMOS에 있어서는 소오스와 드레인 사이의 내압이 2V이하로 현저하게 저하하기 때문에 통상의 전원 전압의 5V로서는 동작이 불가능하다.

(i) Because the channel length decreases as the internal pressure degradation between the drain and the source, in other words, the device become microscopic the punch-through breakdown voltage is degraded. It can achieve by the result of that the improvement of the punch-through breakdown voltage increases the substrate concentration. But the increase of the substrate concentration the electron avalanche breakdown internal pressure is reversely degraded. Because it is in NMOS which is very minute less than 0.3μm and the internal pressure between the drain and the source of the channel length is remarkably degraded less than 2V the operation is impossible as 5V of the normal power supply voltage.

그리고, 편치 수루 내압의 향상을 위해서 기판 농도를 증가하면, 찬넬 콘덕턴스 gm의 감소를 수반하기 때문에 MISFET이 미세화에 의해 얻어지는 고속 동작 특성은 저해된다.

And if the substrate concentration is increased for the improvement of the piece value *** internal pressure , because the reduction of the channel conductance gm is accompanied the high speed operation characteristic that MISFET is obtained with the miniaturization is hindered.

(ii) 래치 업에 의한 MISFET의 파괴, 즉 종래 구조를 갖는 CMOSFET의 최대의 결점은 래치업이라고 부르는 사이리스터(thyristor) 동작에 기인하는 MISFET의 파괴이다. 이 래치 업 현상은 특히 CMOSFET의 미세화에 따라서 현저하게 된다. 즉,

(ii) It is the break down of MISFET by the latch up, and the break down of MISFET in which the defect of the maximum of CMOSFET having in other words, the conventional structure is caused by the thyristor operatio

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NMOS와 PMOS사이의 거리가 근접된 CMOSFET에 있어서는 NMOS의 드레인(25), 웰(22),반도체 기판(21) 및 PMOS의 소오스(26) 또는 드레인 (27)사이에 NPNP 구조를 갖는 기생 사이리스터가 형성된다. 상기의 사이리스터는 과전압의 인가, 통상 스위치 동작중의 내부과도적 과전압의 발생, 또는 광이나 방사선의 조사에 기인하는 소수 캐리어의 유기 등에 의해 유발되어 동작을 개시하고 전원을 정지할때까지 사이리스터 동작을 억제하는 것은 불가능하게 된다. 이 사이리스터 동작에 기인하여 과대 전류가 CMOSFET에 흐르기 때문에 CMOSFET는 파괴된다.

n of calling as the latch up. This latch-up is significant according to especially, the miniaturization of CMOSFE T. That is, in CMOSFET in which the distance between PMOS and NMOS are near and the parasitic Thyristor h aving the NPNP structure is formed between the drain (25) of NMOS, the well (22), and the source (26) of th e semiconductor substrate (21) and PMOS or the drain (27). Generally the thyristor described in the above is i mpossible with the approval of the overvoltage to supp ress the thyristor operation until it is caused by the org anic of the minority carrier caused by the investigation of the generation of the inside transient overvoltage a mong the switch operation or the light or radiation etc. and the operation is disclosed and the power source is readjusted. CMOSFET is destroyed because the overcu rrent flows due to this thyristor operation in CMOSFET.

상기의 사이리스터 동작은 CMOSFET의 미세화에 따라서 웰(22)와 PMOS의 간격이 축소되어 기생 PNP 바이폴라 트랜지스터 및 기생 NPN 바이폴라 트랜지스터의 각각의 전류 이득률의 곱이 1보다 크게 되기 때문에 발생한다는 것이 알려져 있다.

According to the thyristor operation described in the above is the miniaturization of CMOSFET, it is known th at the gap is generated because the gap of PMOS and well (22) is reduced and it becomes the double of each current gain modulus of the parasitism PNP bipolar tran sistor and parasitism NPN bipolar transistor than 1.

상기의 각 기생 바이폴라 트랜지스터에 있어서의 전류 이득률의 곱을 갖게 하는 것에 의해 사이리스터 동작을 저지하는 방법이 제안되고 있다. 즉, P+N 접합으로 형성된 제1도에 도시한 종래 구조 PMSO의 소오스(26) 및 드레인(27)을 쇼트기 접합로 치환한 CMOSFET 구조가 1982년도 국제 전자 장치 학회(International Electron Devices Meeting) 예고집 462페이지에 기재되어 있다. 상기의 #8220#쇼트키 장벽 PMOS에 의한 CMOS 래치 업 현상의 해결(CMOS latch-up elimination using schottky barrier PMOS)#8221#라고 하는 보고서에서는 쇼트키 접합에 있어서의 소수 캐리어 주입 효율이 P+N접합의 것과 비교해서 대단히 작은 사실을 이용해서 기생 PNP 바이폴라 트랜지스터의 전류 이득률을 P+N 접합에 의한 종래 구조의 것과 비교해서 1/100 이하로 까지 저하시키는 것에 의해 래치 업 현상을 해결하고 있다.

The method for interrupting the thyristor operation by making have the double of the current gain modulus in each parasitic bipolar transistor described in the above is proposed. That is, the CMOSFET structure of substit uting for the source (26) and drain (27) of the convent ional structure PMSO shown with the P+N junction in f ormed Figure 1 with the shot machine bonding furnace 1982 year is written in the international electronic devi ce learned society (International Electron Devices Meet ing) preview collection 462 page. In the report done as the resolution (CMOS latch-up elimination using schott ky barrier PMOS) " of the CMOS latch-up by the " Scho ttky barrier PMOS described in the above, by comparin g with of the P+N junction and the minority carrier inje ction efficiency in the Schottky barrier using the fact t hat is very small and the current gain modulus of the p arasitism PNP bipolar transistor being compared with of the conventional structure by the P+N junction and lo wering to 1/100 less than furnace the latch-up is solve d.

P+N 접합대신에 쇼트키 접합으로 소오스 접합 및 드레인 접합을 형성하는 상기의 CMOSFET에 있어서 래치 업 현상은 방지되지만, 쇼트키 접합 특유의 결점이 존재한다. 즉, 쇼트키 접합을 사용한 CMOSFET에 있어서는 드레인 접합누설 전류가 큰 것, 비선형 출력으로 되어 옴접촉 특성을 얻을 수 없는 것 및 전달 콘덕턴스가 낮기 때문에 충분한 전류가 확보되지 않아 고속 동작을할 수 없는 것 등의여러 가지의 결점이 있다.

The latch-up is prevented as to the CMOSFET described in the above forming the source junction and drain junction on the P+N splicer into the Schottky bar rier. However the defect of the Schottky barrier charac teristic exists. That is, in CMOSFET using the Schottky barrier and, and the current enough because it consist s of the non-linear output and it cannot obtain the oh mic contact property the transfer conductance is low a re not secured and the drain junction leakage current i s large it there is no with the high speed operation num ber it has the defect of the tergal various.

쇼트키 접합에 따른 상기의 결점은 그후 제한된 #8220#저농도 불순물 확산을행한 쇼트키 트랜지스터 (blightly doped sc hottky MOSFET)#8221#에 의해 해결할 수가 있다. (1982년도 국제 전자 장치 학회 예고집, 466페이지 참조). 즉, 상기 쇼트키 트랜지스터에 있어서는 낮은 불순물 분포의 드레인 영역 위에 쇼트키 접합을 형성하면, 드레인 접합의 누설 전류가

It can solve with the schottky transistor (blightly doped schottky MOSFET) " done with the " lightly dope d drain implant diffusion row thereafter the defect desc ribed in the above according to the Schottky barrier is l imited. (1982 year is the international electronic device learned society preview collection, 466 page reference)

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작게할 수가 있고, 또한 전달 콘덕턴스도 통상 구조의 PMOS의 그것에 가깝게 할 수가 있다.

If it is in other words, the schottky transistor and the Schottky barrier is formed on the drain region of the lo w impurity distribution , it makes small and it makes ne ar to that of PMOS of the trading structure.

그러나, 낮은 불순물 농도 드레인 확산층과 쇼트키 접합을 조합시킨 구조에 의해 CMOSFET를 구성하는 방법에도 다음과 같은 결점이 존재한다. 즉, 상기의 문헌#8220#CMOS latch-up elimination using schottky barrier PMOS#8221#에도 기재되어 있는 바와 같이 NMOS의 소오스 접합 및 드레인 접합을 쇼트키 접합으로 형성한 경우에 있어서의 기생 NPN 바이폴라 트랜지스터의 전류 이득률은 N+P 접합에 의해 드레인 접합을 형성한 종래 구조에 있어서의 기생 NPN 바이폴라 트랜지스터의 전류 이득률에 비해서 최대 10배나 크게 되는 것이다. 이에 따르면, 낮은 불순물 농도를 갖는 드레인 확산층의 유무에 관계없이 쇼트키 접합으로 PMOS 및 NMOS를 형성한 CMOS 트랜지스터는 PMOS의 소오스 접합 및 드레인 접합을 쇼트키 접합으로 형성하고, NMOS의 각 접합은 통상의 N+P접합으로 형성한 CMOS트랜지스터보다 래치 업 현상이 생기기 쉽다는 결점이 있다.

But the defect as follows exists in the method for configuring CMOSFET with the low impurity concentrati on drain diffusion layer and the structure of combining the Schottky barrier. That is, it as described in the liter ature "CMOS latch-up elimination using schottky barrie r PMOS" described in the above is large in comparison with the current gain modulus in which the current gain modulus of the parasitism NPN bipolar transistor forms t he drain junction with the N+P junction it has in case o f forming the source junction and drain junction of NMO S into the Schottky barrier of the parasitism NPN bipola r transistor in the conventional structure as the maxim um factor of ten. According to this, the CMOS transist or forming PMOS and NMOS into the Schottky barrier re gardless of the occurrence of the drain diffusion layer h aving the low impurity concentration forms the source j unction and drain junction of PMOS into the Schottky b arrier and it has the defect that it is easy than the CM OS transistor which each junction of NMOS forms into t he normal N+P junction that the latch-up is generated.

쇼트키 접합에 의한 래치 방지에 관한 상기 2건의 문헌에 의하면, 낮은 불순물 농도 분포를 갖는 소오스 영역 및 드레인 영역의 각 표면에 쇼트키 장벽을 형성한 PMOS와 옹상의 높은 불순물 농도를 갖는 소오스 확산층 및 드레인 확산층이 형성된 NMSO의 조합에 의해 CMOS 트랜지스터를 구성하는 것이 래치업 방지의 관점에서 가장 바람직한 것이된다.

According to the literature of 2 cases about the latch prevention by the Schottky barrier, it do in the viewpoi nt of the latch-up protection with desirable to arrange the CMOS transistor by the combination of NMSO in wh ich the drain diffusion layer is formed and the source di ffusion layer having the high impurity concentration on PMOS forming the Schottky barrier on each surface of the drain region and the source area having the low im purity concentration distribution and NULL.

그러나 , 상기 2건의 문헌 및 그들의 조합에 의해 얻어지는 결론은 CMOS 트랜지스터의 래치 업 방지의 관점에서만 성립하는 것으로서 CMOS 트랜지스터의 미세화에 따른 NMOS 및 PMOS의 내압 저하에 관한 상술한 결점에 대해서는 아무런 해결 방법도 제안되어 있지 않았다.

But the outcome obtained with literature and their combinations of the , 2 cases was established in the vi ewpoint of the latch-up protection of the CMOS transis tor and any solution was not proposed about the abov e-described defect about the internal pressure degrada tion of NMOS according to the miniaturization of the C MOS transistor and PMOS.

특히 , 찬넬길이가 0.5#956#m이하의 초미세 CMOS 트랜지스터에 관해서는 상기 2건의 문헌에는 아무런 기재도 없고, 상술의 결점에 대해서는 전혀 해결 방법이 없다.

Especially, in the , channel length is the literature of 2 cases about the ultra-fine CMOS transistor less than 0.5μm, any material does not have and there is no solu tion about the defect of the detailed description at all.

본 발명의 목적은 소오스와 드레인 사이의 내압이 통상의 전원 전압에 비해 충분히 높고, 핫 케리어 주입에 따라 특성 열화가 생기지 않는 초미세 MISFET를 제공하는데 있다.

As to the object of the present invention, the internal pressure between the drain and the source are enough high in comparison with the normal power supply voltag e and the ultra-fine MISFET in which the characteristic deterioration is not generated according to the hot car rier injection is to be provided.

본 발명의 다른 목적은 상기와 같은 종래의 결점을 해소하고, 극히 짧은 찬넬 길이로도 통상의 전원 전압으로 동작하고, 또한 래치 업 현상도 방지할 수 있는 CMOSFET를 제공하는데 있다.

Another object of the invention is to provide CMOSFET which it cancels the above-mentioned conventional def ect and it operates to the channel length which is exce edingly short to the normal power supply voltage and m oreover, the latch-up can prevent.

본 발명은 종래의 이중드레인 구조의 가장 적합한 조건의 검토에 있어서, 특히 얕은 접합깊이를 갖는 고농도 불순물분포 영역

As for the review of the condition that is most suitable of the conventional duplication drain structure of the in

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이 완수하는 역할에 착안하여 해석한 결과에 기인한다. 제2도 A는 종래하여금 이중드레인 구조를 갖는 MISFET의 단면도이다. 제2도 A에 있어서 (1)은 P형 반도체 기판, (2)는 필드 산화막, (2)은 게이트 산화막, (5)~(8)은 게이트 전극(4)를 확산 마스크로서 형성한 n형 불순물 영역으로 (5) 및 (7)은 드레인 확산층 (6) 및 (8)은 소오스 확산층이다. 여기서 (5) 및 (6)은 낮은 불순물 농도 확산층이며, 표면 불순물 농도를 Cs2, 접합 깊이를 Xj2로 정의한다. (7) 및 (8)은 높은 불순물 농도 확산층이며, 표면 불순물 농도를 Cs1, 접합 깊이를 Xj1로 정의한다. (9) 및 (10)은 각각 드레인 전극, 소오스 전극이다. 제2도 B는 제2도 A의 MISFET의 반도체 표면에 있어서 드레인 확산층 끝에서 소오스 확산층 측으로의 거리의 함수로서의 불순물 농도 분포가 거기에 있어서의 전계를 해석한 대표적인 결과다. 제2도 B는 실효 찬넬 길이가 1.1#956#m, 게이트 산화막(3)의 막의 두께가 20nm, Xj1이 0.25#956#m, Xj2가 0.3#956#m, Cs1이 1#215#1021cm-3, Cs2#215#1019cm-3의 경우이고, 게이트 전극(4) 및 드레인 전극(9)에 인가한 전압은 각각0V 및 10V이다.

vention, caused by the result which takes notice of the role that the highly doped impurity distribution area having especially, the shallow junction depth accomplishes and interpreted. The second is the cross-sectional view of MISFET in which A has the conventional women gold duplication drain structure. The second is (1) as to A is the P-type semiconductor substrate, and (2) are the n-impurity area in which the field oxide film , and (2) the gate oxidation film , and (5) ~ (8) form the gate electrode (4) as the diffusion mask (5) and (7) the drain diffusion layer (6) and (8) is the source diffusion layer. Here, it is the impurity concentration diffusion layer in which (5) and (6) are low and the surface impurity concentration the Cs 2 , and the junction depth is defined as the Xj 2 . (7) It is the impurity concentration diffusion layer in which (8) is high and the surface impurity concentration the Cs 1 , and the junction depth is defined as the Xj 1 . (9) The respectively (10) is the drain electrode, and the source electrode. In the second B the second is the drain diffusion layer end as to the semiconductive surface of MISFET of A, it is the typical result in which the impurity concentration distribution as the function of the distance to the source diffusion layer interprets the electric field in the there. The second is B is the effectiveness channel length is 1.1μm, and the voltage which 0.3μm, and the Cs 1 of 0.25μm, and the Xj 2 of 20nm, and the Xj 1 of the thickness of the film of the gate oxidation film (3) is in case of 1× 10 21 cm − 3 , and the Cs 2 × 10 19 cm − 3 and it applies in the gate electrode (4) and drain electrode (9) are 0V and 10V.

제2도 B에서 명확한 바와 같이 드레인 전압의 인가에 의해 반도체 표면에 있어서, 최대 전계는 불순물농도가 1018cm-3부근에 있어서의 드레인 확산층 내부에서 형성되고, 불순물 농도가 보다 높은 드레인 확산층(7)내에서는 전계가 보다 작게 되어 가는 것을 알 수 있다. 본 발명은 이러한 해석 결과, 높은 불순물농도 확산층(7) 내에 있어서하여금 전계가 보다 작게 되어 가는 것을 알 수 있다. 본 발명은 이러한 해석 결과, 높은 불순물농도 확산층(7)내에 있어서의 전계의 급격한 저하 경향에 착안한 것에 기안한다.

As to the maximum electric field, the impurity concentration is formed by the approval of the drain voltage as to the semiconductive surface within the drain diffusion layer in 10 18 cm − 3 vicinity as the second been clear and accurate in B than and the impurity concentration can know in the higher drain diffusion layer (7) that the electric field is smaller. The invention can know within such interpretation result , and the high impurity concentration diffusion layer (7) Ha YeoGeum, that at the electric field is smaller with ***. The invention takes notice of such interpretation result , and the degradation tendency to be rapid of the electric field in the high impurity concentration diffusion layer (7) in it drafts.

즉, 상기의 결과는 종래의 이중 드레인 구조의 MISFET에 있어서 상기 영역(7)이고, 내압화에 관해 거의 기여하고 있지 않다고 생각할 수 있다. 상기 개념에 따르면, 미세 MISFET의 고내압화의 관점에서 높은 불순물 농도 확산층의 존재는 도리어 장해로 되고 있으며, 드레인 확산층을 낮은 불순물 농도 확산층으로 구성하는 것이 바람직하다고 생각된다.

That is, the result described in the above is the domain (7) among the conventional this as to MISFET of the drain structure and it can think that it nearly does not contribute about the resisting voltage. According to the concept, the high presence of the impurity concentration diffusion layer rather consists of the failure in the viewpoint of the high voltage-resistant of the minute MISFET and it is sweet with be desirable and it is the drain diffusion layer regarded as the low impurity concentration diffusion layer to configure.

그러나 , 상기의 개념은 종래에 실시되어 있지 않는다. 이것은 종래의 드레인 확산층이 높은 불순물 농도 확산층으로 구성되는 것이라는 고정 개념에서 벗어나지 못했기 때문이고, 따라서 이중 드레인 구조에 있어서도 높은 불순물 농도 확산층의 존재는 불가피하다라고 생각하였기 때문이다.

But it was not contrary to the fixing concept the concept of the , the above was not performed on the convention that this consisted of the impurity concentration diffusion layer in which the conventional drain diffusion layer was high and it was due to think among this as to the drain structure that the high presence of the impurity concentration diffusion layer was inevitable.

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상기의 관점에 따라서 이중 드레인 구조에 있어서의 높은 불순물 농도 확산층(7) 및 (8)의 역할을 보면, 상기 영역(7) 및 (8)은 단지 전극(9) 및 (10)과의 옴접촉의 확보 및 소오스 및 드레인 영역의 확산층 저항의 저감화 이외는 아무런 역할에서도 하고 있지 않는 것은 명확하다. 한편, 소오스 및 드레인 영역의 확산층저항에 관해서는 백금 등의 실리사이드를 확산층 위에 형성하는 종래 기술에 의해 통상의 높은 불순물 농도확산층에 의한 시이트 저항값 50Ω/cm3를 3!&/cm2이하의 1/10 이하로 까지 저감화 할 수 있는 것이 알려져 있다. 그러나, 상기의 실리사이드 드레인 구조에 있어서는 시이트 저항의 저감 효과에만 착안하고, 소오스와 드레인 사이의 내압의 향상의 관점에서의 검토는 종래에 있어서 행하여지지 않아 드레인 확산층에는 고정 개념에 따라서 1020cm-3이상의 표면 농도를 갖는 높은 불순물 확산층이 사용되어 왔다.

According to the viewpoint described in the above, if the role of the impurity concentration diffusion layer (7) in the drain structure and high (8) are looked at among this , it is clear that the domain (7) and (8) the reduction except of the diffusion layer resistance of the security of the ohmic contact with the electrode (9) and (10) and source and drain region only does not play in any role. In the meantime, what can reduce is the sheet resistance value 50Ω / cm 3 by the high impurity concentration diffusion layer known with the prior art forming the silicide including platinum etc. about the diffusion layer resistance of the drain region and source on the diffusion layer until 1/10 less than furnace less than 3!& / cm 2 . But in the drain diffusion layer the review at the viewpoint of the improvement of the internal pressure between the source and the drain are not performed as to the convention it is in the silicide drain structure described in the above and it takes notice of the reduction effect of the sheet resistance, the high impurity spreading layer having the surface concentration more than 10 20 cm - 3 according to the fixing concept should be used.

본발명은 상기의 고정 개념이 무의미한 것이며, 드레인 확산층, 불순물 분포의 최적화에 의해 소오스 및 드레인 내압의 고내압화와 드레인 전극, 드레인 확산층사이의 양호한 옴접촉, 더 나아가서는 낮은 시이트저항화가 가능하게 된다고 생각하고, 검토한 결과에 따른 즉, 본 발명은 실리사이드 층을 형성하여야 할 드레인 확산층의 표면농도가 1018cm-3이상이면, 실리사이드 층 바로 아래에 표면농도가 1019cm-3정도의 석출층이 10nm 정도 형성되어 실리사이드와 드레인 확산층 사이에 MISFET의 통상동작에 충분한 옴접촉이 확보되는 사실을 발견한 것에 따른다. 또 본 발명은 상기 드레인 확산층의 표면 농도가 1020cm-3이하이면, 소오스와 드레인 사이의 내압을 실효 찬넬 길이 1#956#m 이하의 MISFET에 있어서도 최대 5V 이상 종래의 MISFET에 비해서 고내압화 할 수 있는 것을 발견한 사실에 따른다.

As to the invention, the fixing concept described in the above is meaningless and it thinks that the high voltage-resistant of the source and drain internal pressure and drain electrode, the good ohmic contact between the drain diffusion layer, and the sheet resistance are possible with the drain diffusion layer, and the optimization of the impurity distribution and is morefurther more low if the surface concentration of the drain diffusion layer in which the result, in other words, the invention examined has to form the silicide layer is 10 18 cm - 3 or greater , 10nm gad is formed and the precipitation layer of about 10 19 cm - 3 of the surface concentration discovers the fact that the ohmic contact sufficient in the typical operation of MISFET is secured between the silicide and drain diffusion layer the fact immediately beneath follows. And if the surface concentration of the drain diffusion layer as to the invention, is 10 20 cm - 3 or less , it follows the fact that discovers making the internal pressure between the drain and the source endure high voltage as to MISFET less than the effectiveness channel length 1μm over the maximum 5V in comparison with the conventional MISFET.

본 발명에 의한 CMOSFET는 불순물 확산 영역의 최대 불순물 농도가 1018~1020cm-3정도의 N형드레인 영역과 최대 불순물 농도가 1017~1019cm-3정도의 P형 드레인 영역을 가지며, 또한 상기 각 드레인 영역의 적어도 일부가 고융점 금속 또는 상기 금속의 실리사이드 층과 접합되어 구성되어 있는 것에 특징이 있다.

N type drain domain maximum impurity concentration of about 10 18 ~ 10 20 cm - 3 as to the CMOSFET according to the invention, of the maximum impurity concentration of the impurity diffusion region has the P-type drain region of about 10 17 ~ 10 19 cm - 3 and moreover, at least a part of each drain region is welded to the silicide layer of the refractory or the metal and it is formed it has the characteristic.

다음에 본 발명을 실시예에 따라서 더욱 상세하게 설명한다. 설명의 편의상, 도면을 가지고 설명하지만 주요부를 확대하여 도시하고 있으므로 주의를 한다.

Next, according to the embodiment the invention, more specifically, it illustrates. Since it illustrates having for convenience of the description, and drawing but the main part is augmented and it shows it notes.

[실시예 1]

[Embodiment 1]

제3도~제6도는 본 발명에 의한 MISFET하여금 1실시예의 제

The third is drawing in which Ha YeoGeum, figure the

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조 공정을 공정 순서로 도시한 도면으로서, (1)은 P도전형 비저항 1Ω/cm의 실리콘 기판이다. 반도체 기판(1)표면에 종래의 소자 분리 기술을 이용해서 0.8#956#m의 두꺼운 필드 산화막(2)를 선택적으로 형성한 후, 활성 영역의 반도체 표면을 노출하고, 20nm의 깨끗한 게이트 산화막(3)을 형성한다. 그 후, 약 0.3#956#m하여금 실리콘 박막을 게이트 산화막(3)위에 형성하고, PDC/3을 소오스로 하는 열 확산에 의해 실리콘박막에 인(p)의 고농도 확산을 행한다.

sixth shows the manufacturing process of 1 embodiment to the processing procedure with MISFET according to the invention. (1) It is the silicon substrate of the silver P conductivity type resistivity 1Ω / cm. The thick field oxide film (2) of 0.8μm the semiconductive surface of the active area is selectively exposed after doing the formation by using the conventional isolation technology for the semiconductor substrate (1) surface and the gate oxidation film (3) which is clean of 20nm is formed. Thereafter, ha YeoGeum, the silicon thin film is formed on the gate oxidation film (3) with about 0.3μm and the high concentration diffusion of the phosphorus (p) is performed with the thermal diffusion the PDC / 3 to the source in the silicon thin film.

그 후에, 리도그래피에 의해 게이트 전극(4)를 형성한다. 리도그래피후의 찬넬 길이는 1#956#m이다. 다음에 테트라에톡시실란(Si(OC2H5)4)을 사용한 화학 기상반응에 의해 0.5#956#m의 막의 두께를 갖는 실리콘 산화막(11)을 전면으로 퇴적시킨다. 상기의 퇴적막(11)을 반응성 스퍼터 에칭에 의해 최대기판 표면과 수직 방향으로 에칭을 행하여 평탄부에 퇴적된 실리콘 산화막을 제거하면, 제4도에 도시한 바와 같이 게이트 전극(4)의 측벽에만 실리콘 산화막(11)이 남게된다. 이 상태에서 산화막(3)을거쳐서 비소를 가속 에너지70KeV의 조건에서 이온 주입에 의해 반도체 기판(1) 표면에 주입한다. 상기의 조건은 최대 기판 표면에서 최대 불순물 농도로 되는 조건이다. 본 실시예에 있어서는 주입량을 변수로 하고, 표면 불순물농도가 1#215#1017~1019cm-3의 범위에서 여러 가지의 값을취할 수 있도록 다수개의 MISFET를 작성하였다. 상기의 이온주입 공정후 주입 이온의 활성화의 열처리를 행하였다.

Thereafter, the gate electrode (4) is formed with lithography. The channel length after lithography is 1μm. Next, the silicon oxide film (11) having the thickness of the film of 0.5μm with the chemical vapor deposition using the tetraethoxysilane (Si(OC(SB)2(/SB)H(SB)5(/SB))(SB)4(/SB)) is sedimented with the front side. As shown in Figure 4 the heap film (11) described in the above the etching is performed with the reactive sputter etching into the maximum substrate surface and vertical direction, the silicon oxide film (11) remains in the side wall of the gate electrode (4). In this state, in the condition of the acceleration energy 70 KeV the arsenic through the oxide film (3), it injects into the semiconductor substrate (1) surface with the ion implantation. In the condition described in the above is the maximum substrate surface, it is the condition consisting of the maximum impurity concentration. It was in this embodiment and the injection amount was to the variable and the surface impurity concentration prepared multiple MISFETs in order to have in the range of 1× 10 17 ~ 10 19 cm - 3 with the value number of the various. The thermal process of the activation of the implant ion was performed after the ion implantation process described in the above.

상기의 열처리는 1000℃에서 행하였지만, 여러가지의 주입량을 갖는 각각의 MISFET에 대해 접합깊이 Xj가 0.25#956#m로 되도록 각각 열처리 시간을 설정하였다. 그후, 드레인 확산층(5) 및 소오스 확산층(6) 위의 게이트 산화막(3)을 제거하고, 50nm의 막의 두께의 백금(Pt)를 전면에 스퍼터링법에 의해 증착한다. 다음에 450℃의 열처리를 하고, 드레인(5), 소오스 확산층(6) 표면 및 게이트 전극(4)표면에 백금 실리사이드(PtSi)(12)를 형성한다.

The thermal process described in the above is for the establishment of the junction depth Xj about each MISFET which has the injection amount of the various performed in 1000℃ is 0.25μm, as as possible, the thermal processing annealing time. Thereafter, the gate oxidation film (3) above the drain diffusion layer (5) and source diffusion layer (6) is removed and the platinum (Pt) of the thickness of the film of 50nm is deposited on front with the sputtering method. Next, it heat-treats of 450℃ and the platinum-silicide (PtSi) (12) is formed on the drain (5), and the source diffusion layer (6) surface and gate electrode (4) surface.

상기의 열처리에 있어서 산화막(11) 및 (2) 위에서는 실리콘과의 반응은 일어나지 않아 실리사이드는 형성되지 않는다. 따라서 상기 열처리 공정후, 왕수로 에칭하면 PtSi는 왕수로 에칭되지 않기 때문에 산화막 및 반응하지 않는 Pt만이 제거되고,

Reaction with the silicone on the oxide film (11) as to the thermal process described in the above and (2) have the oxide film it does not occur and the silicide is not formed if it etches to the aqua regia after the therma

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게이트 전극(4), 드레인 확산층 (5) 침소오스 확산층(6)의 각 표면에 위에만 PtSi가 자기 정합적으로 남게 된다. 여기에 있어서 PtSi 층(12) 바로 아래에는 PtSi 층 형성전의 표면 불순물 농도 보다도 1자리수 높은 불순물 농도를 갖는 약 10nm두께의 석출층(13)이 PtSi 층 (12)와 자기 정합적으로 형성되었다. 상기 석출층(13)내에 있어서의 깊이 방향의 불순물 분포는 깊이에 대해 아래로 볼록한 형상을 갖는다. PtSi 층 (12)의 형성 후, 공지의 기술을 사용해서 보호 절연막(15), 또 드레인 전극(9) 및 소오스 전극(10)을포함하는 배선전극을 바라는 회로 방식에 따라서 형성한다. 상기의 전극(9)(10)에는 알루미늄(Al)의 증착만을 사용하지만, Al이 PtSi 층 (12)와 반응하는 것을 방지하기 위하여 A1배선 공정전에 Ti와 Ta의 동시 스퍼터링에 의해 TiTa 막(14)를 PtSi 막(12)위의 접촉구멍 부분에 사전에 형성한다.

l process, the therefore the PtSi is not etched at the a qua regia and the PtSi layer (12) as to the excitation, i mmediately, the impurity distribution of the longitudinal direction in the precipitation layer (13) is the convex s hape down the depth the precipitation layer (13) of ab out 10nm thickness having the impurity concentration which the single digit was beneath higher than the surf ace impurity concentration of the PtSi layer formation t otal was formed with the PtSi layer (12) and self-align ment manner the PtSi remains in the upper part in the gate electrode (4), and each surface of the drain diffus ion layer (5) sleeping place OSS diffusion layer (6) as t he self-alignment manner it is removed only the Pt whic h does not react. And and it forms according to the cir cuit method wanting the interconnection electrode whi ch the drain electrode (9) and source electrode (10) in clusion is named by using the publicly known technolog y after the formation of the PtSi layer (12). In the elec trode (9) (10) described in the above, it uses only the deposition of the aluminum (Al). However in order to pr event the Al from reacting to the PtSi layer (12), the T iTa film (14) is formed on the contact hole part above t he PtSi film (12) before the A1 interconnection process with the co-sputtering of the Ta and Ti in advance.

상기의 제조 과정을 거쳐서 제조된 각종의 표면 불순물 농도 Cs2를 갖는 드레인 확산층(5)로 구성된 각각의 MISFET의 게이트 전압이 영에서 소오스와 드레인 사이의 내압 BVDS를 측정하였을 때, 제9도의 결과가 얻어졌다. 제9도의 측정에 사용한 각 MISFET는 본 실시예의 제조 과정에서도 명확한 바와 같이 실효찬넬 길이가 1#956#m 게이트 산화막(3)의 막의 두께가 20nm, 드레인 접합 깊이 0.25#956#m의 동일 조건의 것이고, 드레인 확산층(5)의 표면 불순물 농도만이 달라지고 있다. 본 실시예의 각 MISFET에 있어서는 드레인 접합끝이 게이트 전극(4)의 끝과 일치하도록 게이트 측벽 산화막(11)의 막하 여금 두께를 제어하고 있다. 제9도의 결과로 주목되는 것은 드레인 확산층(5)의 표면 불순물 농도가 5#215#1018cm-3부근에서 BVDS값이 최대로 되어 11.5V에 까지 도달하는 것이다.

When the gate voltage of each MISFET consisting of the drain diffusion layer (5) having the various surface i mpurity concentration Cs 2 manufactured after the ma nufacturing process described in the above measured t he internal pressure BV DS between the drain and the s ource in zero , the result of Figure 9 was obtained. As each MISFET used in the measurement of Figure 9 bee n clear and accurate in the manufacturing process of t his embodiment than the thickness of the film of 1μm g ate oxidation film (3) of the effectiveness channel leng th is 20nm, and of the same condition of the drain conj ugation depth 0.25μm and the thickness is changed onl y the surface impurity concentration of the drain diffusi on layer (5). It is in each MISFET of this embodiment a nd the staff-officer women gold thickness of the gate s idewall oxide (11) is controlled so that the drain junctio n end coincides with the end of the gate electrode (4). The BV DS value is maximized in 5× 10 18 cm − 3 vicini ty and the surface impurity concentration of the drain diffusion layer (5) reaches 11.5V to be watched to the result of Figure 9.

상기의 값은 표면 불순물 농도가 1020cm-3이상의 드레인으로 구성되는 동일 접합 깊이를 갖는 종래 MISFET의 BVDS값보다 4.5V 이상이나 높은 내압화가 실현되어 있는 것을 나타내고 있다. 또, 제9도에 있어서 점선으로 표시한 종래의 이중 드레인 구조 MISFET에 있어서 BVDS값의 최대값보다도 본 발명에 의한 MISFET의 쪽이 3.5V 이상이나 높은 내압화가 실현되어 있는 것을 나타내고 있다.

It shows that the resisting voltage which is higher than the BV DS value of the conventional MISFET in which t he value described in the above has the identical juncti on depth in which the surface impurity concentration c onsists of the drain more than 10 20 cm − 3 over 4.5V is realized. And it shows among the conventional this in dicated by the dotted line as to Figure 9 that the resis ting voltage in which the side of the MISFET according to the invention is higher than the maximum value of th e BV DS value over 3.5V is realized as to the drain stru cture MISFET.

그리고, 제9도에 도시한 이중 드레인 구조의 특성은 낮은 불순물 농도 분포(5)의 접합 깊이 Xj2가 0.25#956#m, 표면 불순물 농도 Cs2는 도시한 각각의 값이고, 높은 불순물농도 분포(7)의 접합 깊이 Xj1이 0.15#956#m, 표면 불순물 농도 Cs1

And the property of the drain structure among this shown in Figure 9 relates to MISFET which the junction depth Xj 2 of the low impurity concentration distributio n (5) is each value which 0.25μm , and the surface imp

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은 1#215#1021cm-3의 구성으로 되는 드레인 확산층을 갖는 MISFET에 관한 것이다. 여기에서 게이트 산화막(3)의 막두께는 20nm, 실효 찬넬 길이는 1#956#m이다.

urity concentration Cs 2 show and has the drain diffusion layer in which the junction depth Xj 1 of the high impurity concentration distribution (7) 0.15μm , and the surface impurity concentration Cs 1 consists of the configuration of 1× 10 21 cm − 3 . Here, the film thickness of the gate oxidation film (3) is 20nm, and the effectiveness channel length are 1μm.

본 실시예에 따라서 제조한 MISFET에 있어서의 전류 전압 특성을 상세하게 검토하였으나, 드레인(5) 및 소오스 확산층(6)의 표면 불순물 농도가 1#215#1018cm-3 이상으로 구성된 MISFET에 있어서는 전류의 상승 특성에 쇼트키 성분이나 큰 직렬 저항 등이 발견되지 않고, 양호한 옴접촉이 드레인(5) 및 소오스 확산층(6)과 백금 실리사이드(12) 사이가 얻어지고 있는 것이 명확하게 되었다. 본실시예에 따라서 제조된 MISFET에 관한 상기 측정결과에서 드레인 확산층(5)의 표면 불순물 농도로 1018cm-3이상1020cm-3 미만인 것이 소오스 드레인 내압의 고내압화의 관점 및 양호한 음접촉의 관점에서 바람직하고, 특히 5#215#1018cm-3 정도인 것이 바람직하다. 상기의 조건에서 드레인 확산층이 구성된 본 발명에 의한 MISFET에 있어서는 종래의 동일치수의 미세 MISFET에 비해서 BVDS 값에서 3.5V 이상의 고내압비가 실현되고, 또한 양호한 옴접촉도 확보할 수가 있었다. 상기의 양호한 옴접촉은 낮은 불순물 농도 표면으로서 실리사이드 형성시에 실리사이드층 (12) 바로 아래에 매우 얇은 높은 불순물 농도 석출층(13)이 동시에 형성되기 때문이라고 생각된다.

According to the present preferred embodiment, specifically the current voltage property in MISFET manufactured was examined. But it was in formed MISFET and the short key component or the serial resistance etc. of the surface impurity concentration of the source diffusion layer (6) and drain (5) was not discovered over 1× 10 18 cm −3 in the rising characterisitics of the current and big it was clear that the drain (5), the source diffusion layer (6) and platinum-silicide (12) interval of the good ohmic contact was obtained. According to the present preferred embodiment, in the measurement result about manufactured MISFET, it is the be desirable to the surface impurity concentration of the drain diffusion layer (5) 10 18 cm − 3 over 10 20 cm −3 under in the viewpoint of the viewpoint of the high voltage-resistant of source and drain internal pressure and the good negative principle in nature contact and what is about especially, 5× 10 18 cm −3 is the be desirable. In the condition described in the above, it was in the MISFET according to the invention in which the drain diffusion layer was formed and the high voltage-resistant ratio more than 3.5V in the BV DS value was realized in comparison with the minute MISFET of the conventional same size and the ohmic contact which was moreover good could secure. It is regarded that very thin high impurity concentration precipitation layer (13) is due to be immediately simultaneously beneath formed as the impurity concentration surface in which the good ohmic contact described in the above is low in the silicide formation with the silicide layer (12).

본발명에 따라서 구성된 MISFET에 있어서는 종래의 실리사이드 드레인 구조를 갖는 MISFET와 마찬가지로 3Ω/cm2 의 낮은 시이트 저항을 확보할 수가 있었다.

The low sheet resistance of 3Ω / cm 2 could be secured like MISFET which was in MISFET formed according to the invention and had the conventional silicide drain structure.

[실시예 2]

[Embodiment 2]

제7도는 본발명의 다른 실시예를 도시한 도면이며, 상기 제1의 실시예에 있어서 게이트 측벽 산화막(11)의 막의 두께를 얇게 하고, 드레인 접합 끝이 게이트 전극(4)아래에 존재하도록 구성하여 MISFET를 작성하였다.

It is drawing in which figure the seventh shows the other embodiment of the invention. It made the thickness of the film of the gate sidewall oxide (11) thin as to the first embodiment and it configured so that the drain junction end existed under the gate electrode (4) and MISFET was prepared.

상기 구성에 있어서는 드레인 확산층(5)의 낮은 불순물 농도 영역의 대부분 이 게이트 인가 전압에 의해 제어되는 것이 가능하게 된다. 실효 찬넬 길이 1#956#m, 소오스와 드레인의 각 적합 깊이 0.25#956#m 및 게이트 산화막의 두께 20nm등 MISFET의 구조 파라미터를 동일하게 하고, 상기 제1의 실시예 및 본 실시예에 따라서 구성된 MISF ET, 또 종래의 높은 불순물농도 분포만으로 소오스 및 드레인이 구성된 MISFET에 대해서 각각 그 전달 콘덕턴스를 측정하였다. 그 결과, 상기 종래 구조 MISFET의 전달 콘덕턴스를 1로 하였을 때, 제1 및 본 실시예에 따라서 구성된 각 MISFET의 전달 콘덕턴스는 각각 0.95 및 0.98로 되었다.

It is possible that it is in the configuration and the mostly is controlled of the low concentration domain of impurities of the drain diffusion layer (5) with this gate impressed voltage. It made the structure parameter of MISFET including the thickness 20nm of the gate oxidation film and 0.25μm etc. the deeply identical with the effectiveness channel length 1μm, and each conformity of the drain and source and the transfer conductance was measured about MISFET in which the source and drain consisted of the high impurity concentration distribution with the MISF ET. According to the present preferred embodiment. was formed with the first embodimen

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t. Consequently, when the transfer conductance of the conventional structure MISFET was done to 1 , it beca me the transfer conductance of each MISFET which ac cording to the present preferred embodiment, was form ed with the first with 0.95 to 0.98.

본 실시예에 따른 상기 MISFET의 전달콘덕턴스의 값은 드레인 접합 깊이의 약절반이 게이트 전극(4)로 덮여지도록 구성된 MISFET에 관한 것이다. 상기 측정 결과에서 명확한 바와 같이, 드레인 접합이 게이트 전극(4)로 덮여지는 것과 같이 구성한 MISFET에 있어서는 종래 구조 MISFET와 거의 동일한 전달콘덕턴스를 확보하고, 또한 종래 구조 MISFET의 약2배의 소오스와 드레인 사이의 내압을 실현할 수가 있었다. 본 실시예에 있어서, 전달 콘덕턴스 향상의 관점에서는 게이트 전극(4)로 덮여지는 드레인 저농도 영역의 비율을 크게 하는 것이 바람직하지만, 게이트 용량의 저하의 관점에서는 상기 비율을 적게 하는 쪽이 바람직하다. 따라서, 상기의 비율은 집적회로 설계에 관한 종합적 판단에 의해 결정하면 좋다.

The value of the transfer conductance of MISFET according to this embodiment relates to MISFET in whi ch about half of the drain conjugation depth is covered with the gate electrode (4). As shown in it was clear a nd accurate in the measurement result than it was in M ISFET which it configured as the drain junction been co vered with the gate electrode (4) and the same transf er conductance as the conventional structure MISFET was secured and moreover, the internal pressure betw een the source of about two times of the conventional structure MISFET and the drain could be realized. As to this embodiment, it is the be desirable to play the rate of the drain low density area covered with the gate ele ctrode (4) in the viewpoint of the transfer conductanc e improvement. However the side writing the rate is th e be desirable in the viewpoint of the degradation of th e gate capacitance. Therefore, it is better that the rat e described in the above determines with the synthetic determination about the integrated circuit design.

[실시예 3]

[Embodiment 3]

제8도는 본 발명의 다른 실시예를 도시한 도면으로서, 상기 제1의 실시예에 있어서 낮은 불순물 농도 드레인 확산층의 형성을 위한 비소 이온 주입 공정을 2회로 나누어 각각 70KeV 및 300KeV의 에너지로 이온 주입하고, 다음에 상기 제1의 실시예에 따라서 MISFET를 제조하였다.

Figure 8 is drawing showing the other embodiment of the invention. The arsenide ion injection process for th e formation of the low impurity concentration drain diff usion layer was divided into two times as to the first e mbodiment and it ion-implanted the respectively at the energy of 300KeV and 70KeV and next MISFET was ma nufactured according to the first embodiment.

상기 제1의 이온 주입에 의해 5#215#1018cm-3 인 최대 불순물 농도가 반도체 표면에 형성되고, 제2의 이온주입에 의해서는 5#215#1017cm-3 인 최대 불순물 농도가 반도체 기판 표면에서 약 0.16#956#m 내부에 구성되는 드레인 확산층 구조로 하였다. 상기 MISFET에 있어서 소오스와 드레인 사이에 5V의 전압을 인가하고, 게이트 인가 전압의 함수로서 기판(1)에 흐르는 전류를 측정하였을 때, 그 최대 전류값은 1.7#215#10-7A이었다.

The maximum impurity concentration which was 5× 10 18 cm - 3 was formed in the semiconductive surface w ith the first ion implantation and it was according to du e to the second ion implantation and the maximum impu rity concentration which was 5× 10 17 cm -3 was don e by the drain diffusion layer structure of being formed in the surface of semiconductor substrate inside about 0.16μm. The voltage of 5V was applied as to MISFET b etween the source and drain and when the current flo wing in the substrate (1) was measured as the functio n of the gate impressed voltage , the peak current valu e was 1.7× 10 - 7 A.

본 실시예에 의한 MISFET와 동일한 구조 파라미터를 갖는 상기 제1의 실시예에 따른 트렌지스터 및 공지의 이중 드레인 구조로 구성된 MISFET에 대해서 상기와 동일한 조건에 의해 기판 전류를 측정한 결과는 그 최대 전류가 각각 9.6#215#10-7A 및 1.2#215#10-5A이었다.

As to the measured result, the maximum current was the substrate current 9.6× 10 - 7 A and 1.2× 10 - 5 A about MISFET consisting of the drain structure amon g the transistor according to the first embodiment havi ng the same structure parameter as MISFET by this em bodiment and publicly known this with the above and s ame condition.

본 실시예에 따른 MISFET의 기판전류가 종래의 구조의 MISFET에 있어서의 기판전류 보다도 약 2리 수만큼이나 작은 것은 MISFET의 신뢰성의 향상에 본 발명에 의한 MISFET가 매우 유효하다는 것을 나타내고 있다. 즉, 기판 전류의 저감은 게이트 산화막 속의로의 핫 캐리어 주입량의 저감화의 작용을 갖는 것으로 알려져 있고, 임계 전압값의 변동이나 표면 준위

The that the MISFET according to the invention is very effective thing is shown in the improvement of the relia bility of MISFET that the substrate current of MISFET according to this embodiment is smaller than the substr ate current in MISFET of the conventional structure as about 2 Lee number. That is, the action is known that

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밀도의 증가등의 트랜지스터 특성이 저하하지 않도록 한다.

the reduction of the substrate current has the action o f the reduction of the hot carrier injection amount to t he gate oxidation film *** and the transistor characteri stic including the increase of the change of the thresh old voltage value or the surface level density etc. is no t degraded.

본 실시예에 있어서는 이온 주입의 가속 에너지를 변경한 2회의 이온 주입 공정에 의해 다른 분포를 갖는 낮은 불순물 농도 분포의 합성에 의해 드레인 확산층 (5)를 구성한 일 예를 나타냈지만, 상기의 드레인 확산층은 3종류 이상의 낮은 불순물 농도 분포의 합성에 의해서도 좋고, 제조 공정도 이온 주입 법에 한정되는 것이 아니라 예를들면, 공지의 열 확산법에 의해서도 좋다. 또, 드레인 확산층을 형성하는 불순물은 동일의 것일 필요는 없고, 동일한 도전형의 원자이면 그 조합은 아무래도 좋다. 즉, 본 실시예의 기본 개념은 드레인 확산층(5)내의 최대 전계인가 영역이 한점에 집중하는 일 없이 인가 전계를 가능한 한 분산시킬 수 있는 드레인 불순물 분포를 실현하는데 있다. 상기 개념에 따르면, 최대 전계가 인가되는 불순물 농도가 약 1 #215#1018cm-3로 드레인 확산층(5) 전체가 구성되는 것이 이상적이고, 상기의 이상에 의해 합당한 불순물 농도 분포를 합성하여 드레인 확산층(5)를 구성하는 것이바람직하다.

One example configuring the drain diffusion layer (5) with the composition of the low impurity concentration distribution having the dissimilar distribution with the io n implantation process of being in this embodiment and changing the acceleration energy of the ion implantatio n of two times was shown. However the drain diffusion layer described in the above is good with the compositi on of the low impurity concentration distribution more t han 3 kind and the manufacturing process is not restric ted to the ion implantation method but it is good with f or example, the publicly known thermal diffusion metho d. And the need that the impurity forming the drain diff usion layer is of the identity does not have and the co mbination is by no means good if it is the atom of the s ame conductivity type. That is, the basic concepts of this embodiment is to realize the drain impurity distribut ion which can disperse the applied field as long as the maximum electric field approved area within the drain di ffusion layer (5) converges on one point task is possibl e without the task in which. According to the concept, it is ideal that the drain diffusion layer (5) whole of the impurity concentration in which the maximum electric fi eld is applied is formed of about 1× 10 18 cm - 3 and t he impurity concentration distribution merging is synthe sized with over described in the above and the drain dif fusion layer (5) is configured it is the lice be desirable.

[실시예 4]

[Embodiment 4]

제10도는 본 발명의 다른 실시예를 도시한 도면으로, 상기 제1의 실시예에 있어서의 실리콘 박막에 의해 구성된 게이트 전극(4) 대신에 Mo 박막에 의한 금속 게이트 전극(4)를 사용하고 있다. 상기의 Mo 전극의 표면 위에는 실리콘 질화막으로 되는 전국 보호막(18)을 게이트 전극(4)와 자기 정합적으로 구성하였다. 이것은 동일의 포토레지스트를 사용해서 에칭하는 것에 의해 행한 상기의 게이트 구조는 금속 게이트 구조로서 공지이며, 그 상세한 설명은 생략한다. 상기 제1의 실시예 및 상기 공지의 금속 게이트 구조 트랜지스터의 제조 방법에 따라서 낮은 불순물 농도 드레인 확산층(5) 및 소오스 확산층(6)위에 PtSi층 (12)를 형성한다.

Figure 10 is a drawing of the other embodiment of the invention, the metal gate electrode (4) by the Mo thin film instead of the gate electrode (4) which the silicon thin film in the first embodiment is organized is used. T he whole country protective film (18) consisting of the silicon nitride film was organized on the gate electrode (4) and self-alignment manner on the surface of the M o electrode described in the above. The gate structure described in the above of performing by this using the photoresist of the identity and etching is the bulletin a s the metal gate structure and the detailed explanation omits. The PtSi layer (12) is formed according to the m anufacturing method of the publicly known metal gate structure transistor and the first embodiment on the im purity concentration drain diffusion layer (5) and the lo w source diffusion layer (6).

그후, 상기 실리사이드 층(12) 바로 아래에 실리사이드층과 자기 정합의 관계로 As 이온을 주입하였다. 상기 As 이온 주입에 의한 최대 불순물 농도는1#215#1021cm-3이고, 반도체 표면에서 최대값을 갖는 구성으로 되어 있다. 상기 As 이온 주입에 의한 접합 깊이는 50nm 이하로 되는 것과 같이 이온 주입기에 가속 에너지를 여러 가지로 변화시켜서 실시하였다. 그후 램프가열을 사용한 순간가열법에 의해 상기의 높은 불순물농도 영역(16)만을 활성화 하였다.

Thereafter, the As ion was immediately beneath injected to the relation of the self alignment and silicid e layer with the silicide layer (12). It is the maximum im purity *** × 10 21 cm - 3 by the As ion implantation and it consists of the configuration of having the maxi mum value in the semiconductive surface. As the juncti on depth by the As ion implantation become less than 50nm the acceleration energy was variously diversified and it performed to the ion-implanter. Thereafter, it ac tivated with the flash heating method using the Lamp h eating only the high concentration domain of impurities (16) described in the above.

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그후, 상기 제1의 실시예에 따라서 보호 절연막(15) 및 드레인 전극(9)와 소오스 전극(10)을 구성하였다. 상기 전극(9) 및 (10)과 실리사이드 층(12) 사이에는 A1과 실리사이드의 반응을 방지하기 위한 Ti,Ta혼합막(14)가 상기 실시예 1에 따라서 구성되어 있다. 상기 구성에 따라서 제조된 접합 깊이 10nm에서 50nm인 높은 불순물 농도 영역(16)을갖는 각종 MISFET에 있어서 그 BVDS 값을 측정하였을 때 모든 MISFET에 있어서도 BVDS값은 상기 제1의 실시예에 따른 MISFET의 BVDS 값보다 약0.5V낮을 뿐 이었다.

Thereafter, according to the first embodiment, the protective insulator film (15), the drain electrode (9) a nd source electrode (10) were configured. The Ti,Ta mi xing film (14) for preventing the reaction of the silicide and A1 is formed between the electrode (9), (10) and silicide layer (12) according to the embodiment 1. In th e junction depth 10nm manufactured according to the configuration, when measuring the BV DS value as to t he high concentration domain of impurities (16) *** all kinds of MISFET that was 50nm, the BV DS value conti nued about 0.5V day as to all MISFETs than the BV DS value of MISFET according to the first embodiment wit h only.

상기의 결과는 실리사이드 층(12) 바로 아래의 높은 불순물 농도 영역(16)이 50nm 이하로 얇으면, 종래구조 MISFET에 비해서 소오스 및 드레인 내압이 한층 개선되는 것을 나타내고 있다. 본 실시예의 기본적 개념은 드레인 확산층(5) 표면에 구성하는 높은 불순물 농도 영역(16)이 접합 깊기로 50nm 이하로 매우 얇으면 BVDS값의 고내압화에 실효적으로 지장이 없고, 또한 양호한 옴접촉도 확보할 수 있는 것이다. 본실시예에 있어서는 실리사이드 층(12)를 드레인 확산층(5) 위에 구성한 예에 대해서 나타내었지만, 상기 개념에 따르면 실리사이드 층은 백금 실리사이드에 한정되는 것이 아니고, Mo,W,Pt,Pd,Ni,Ti,Ta,Nb,Cr,Pr등의 고융점 금속 및 그들의 실리사이드 막으로 치환하여 구성하여도 지장이 없다.

If as to the result described in the above, the silicide layer (12), immediately, the following high concentratio n domain of impurities (16) is thin less than 50nm , it s hows that the source and drain internal pressure are m ore and more improved in comparison with the conventi onal structure MISFET. If it is very thin, the impedimen t is effectively not in the high voltage-resistant of the BV DS value less than 50nm that the basic concept of this embodiment the high concentration domain of impu rities (16) configured is deep in the drain diffusion layer (5) surface with junction and the ohmic contact which is moreover good can secure. It showed about the exa mple which was in this embodiment and configured the silicide layer (12) on the drain diffusion layer (5). Howe ver the silicide layer is not restricted according to the concept to the platinum-silicide but even if it substitut es with the high melting point metal and their silicide fil ms including Mo,W,Pt,Pd,Ni,Ti,Ta,Nb,Cr,Pr etc. and it c onfigures there is no impediment.

[발명의 다른 실시예]

[The other embodiment of the invention]

이상의 각 길기예에서는 모두 소오스, 드레인 영역으로 되는 확산층은 낮은 불순물 농도의 얇은 확산층이고, 화산층 저항을 저감하는 길리사이드 층은 게이트 전국에서 분리(오프 셋)되어 형성되어 있다. 따라서, 이와 같은 오프 셋 구조의 트랜지스터에서는 소오스와 드레인을 고농도, 확산층으로 형성한 것보다도 실효찬넬 콘덕턴스가 저하한다.

In each road arts described in the above, it is the thin diffusion layer of the impurity concentration in which th e diffusion layer which altogether consists of the sourc e, and the drain region is low and it becomes in the gat e whole country with the separation (offset) and the gi lly side layer reducing the volcano layer resistance is fo rmed. Therefore, in the transistor of this kind of the off set structure, the effectiveness channel conductance i s degraded than forms the source and drain into the hi gh concentration, and the diffusion layer.

그래서, 게이트 측벽 절연막(제6도, 제7도, 제8도, 제19도의 부호(11)을 실리콘 산화막이 아니고, 비유전율이 보다 높은 재료로 형성하면 게이트에서의 프린지(fringe) 용량(면이 대향하는 용향보다 광의의 의미로서, 도전체의 언저리나 끝에 생기는 용량을 말한다.)에 의해 소오스 및 드레인의 낮은 불순물 농도 확산층의 표면으로의 게이트 전압의 영향을 높일 수가 있어 실효 전달 콘덕턴스가 높은 디바이스를 얻을 수가 있다. 이것은 제1도에 도시한 바와 같은 이중 확산 구조의 소오스와 드레인을 갖는 MIS FET에 대해서도 적용된다.

So, the seventh the eighth is the denotation (11) of Figure 19 not gate sidewall insulation film (sixth the sili con oxide film and if the relative permittivity forms into the higher material, the influence of the gate voltage t o the surface of the low impurity concentration diffusio n layer of the source and drain can be enhanced with t he fringe (fringe) capacity (as the meaning of the broa d sense than the capacity in which side is faced, the g enerated capacity is referred to the brim or the end of the conductor.) at gate and the device in which the ef fectiveness transfer conductance is high can be obtain ed. This is applied to Figure 1 to the MIS FET having th e source and drain of the spread structure among this l ike showing.

[실시예 5]

[Embodiment 5]

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제11도는 본 발명에 의한 MISFET의 1실시예를 도시한 도면으로, (1)은 P 도전형 비저항 1Ω/㎝의 실리콘 기판이고, (2)는 공지의 선택 산화법에 의해 형성된 필드 산화막으로 인접하는 MISFET사이를 분리 하는 두꺼운 실리콘 산화막이다. (3)은 20 nm의 실리콘 열 산화막, (4)는 인을 첨가시켜 저 조항화된 실리콤 박막으로 구성된 게이트 전극이다. 공지의 실리콘 게이트 기술에 의해 게이트 전극(4)을 형성한 후, 실리콘 열 산화막(3)을 거쳐 게이트 전극을 마스크로 해서 비소(As) 이온을 이온 주입법에 의해 실리콘 기판 표면에 주입하고, 이어서 주입 이온의 활성화를 위한 열처리를 행하여 드레인 확산층(5) 및 소오스 확산층(6)을 형성하였다. 상기의 이온 주입에 있어서는 반도체 표면에서 불순물 농도가 최대로 되고, 그 최대값이5#215#1018Cm-3으로 되는 조건에서 행하였다.

Figure 11 is a drawing of 1 embodiment of the MISFET according to the invention, (1) is the silicon substrate of P conductivity type resistivity 1Ω / ㎝. (2) It is the thick silicon oxide film separating according to the field oxide film formed with the increased publicly known local oxidation of silicon between adjacent MISFET. (3) is the silicon thermal oxide film of 20 nm, and (4) are the gate electrode consisting of the silicon thin film adding the phosphorus and becomes with the base clause. The gate electrode was after the silicon thermal oxide film (3) to the mask and the gate electrode (4) the arsenic (As) ion was injected with the publicly known silicon gate technology after doing the formation with the ion implantation method into the silicon substrate surface and subsequently the thermal process for the activation of the implant ion was performed and the drain diffusion layer (5) and source diffusion layer (6) were formed. It was in the ion implantation described in the above and the impurity concentration was maximized in the semiconductive surface and it performed in the condition consisting of the maximum value lice 5× 10 18 Cm - 3 .

그후, 암모니아(NH3)와 모노실란(SiH4)의 화학 기상 반응에 의해 주표면 전면에 비유전율 6.0인 실리콘질화(Si3N4)막을 막두께 0.25㎛의 조건으로 퇴적한다.

Thereafter, the silicon nitride (Si(SB)3(/SB)N(SB)4 (/SB)) film which is the relative permittivity 6.0 is accumulated with the chemical vapor deposition of the monosilane (SiH(SB)4(/SB)) and ammonia (NH(SB)3(/SB)) in the major surface front side to the condition of the film thickness 0.25㎛.

그후, 평행 평판형 반응성 스피터 에칭 장치에 의해 상기의 Si3N4 막을 0.25㎛두께만큼 에칭하였다.

Thereafter, the si 3 N 4 film described in the above was etched with the parallel plate type reactive Peter etching device as 0.25㎛ thickness.

상기의 에칭은 소위 이방성 에칭이라고 하는 것으로서 반도체 기판 표면과 수직 방향에만 에칭을 진행시킬 수가 있다. 따라서, 상기의 에칭후에는 게이트 전극(4)의 측벽부에만 Si3N4막(19)가 남게 된다. Si3N4막으로 구성되는 측벽 절연막(19)의 형성 후, 게이트 전극(4)와 측벽절연 막(19)를 마스크로 하여 소오스 및 드레인 확산층 표면에서 최대 불순물 농도로 되는 조건으로 재차 As 이온 주입을 행한 후, 그 활성화를 위한 열처리를 실시하였다.

The etching described in the above is called the so-called anisotropic etching and the etching can be proceeded in the surface of semiconductor substrate and vertical direction. Therefore, in the post-etching described in the above, the Si 3 N 4 film (19) remains in the sidewall part of the gate electrode (4). It had the gate electrode (4) and side wall insulating film (19) as the mask and the As ion implantation the thermal process for the activation was again performed after the formation of the side wall insulating film (19) consisting of the Si 3 N 4 film in the source and drain diffusion layer surface to the condition consisting of the maximum impurity concentration after doing the row.

살기 제2의 이온 주입에 의해서 고오스 및 드에인 확산층의 최대 불순물 농도는 1#215#10㎝-3 이상의 높은 불순물 농도로 되었다. 그후, 통상의 반도체 제조 공정 순서에 따라, 게이트 보호 산화막(20) 및 드네인 전극(21)과 소오스 전극(22)를 형성하고 MISFET로 되는 반도체 장치를 제조하였다.

The maximum impurity concentration of the diffusion layer which was in the high OSS and consisted of the high impurity concentration more than 1×10 ㎝ - 3 with the ion implantation of the violent temper second. Thereafter, according to the normal process of manufacturing semiconductor order, the electrode (21) which was the protecting gate oxide film (20) and the semiconductor device for forming the source electrode (22) and consisting of MISFET were manufactured.

본 실시예에 따라서 제조한 MISFET는 실효 찬넬 길이가 0,9㎛, 드레인 확산층에 있어서의 낮은 불순물 농도 영역(5)의 접합 깊이가 0.35㎛, 높은 불순물 농도 영역(7)의 접합 깊이가 0.15㎛이었다.

According to the present preferred embodiment, 0.35㎛, and the junction depth of the high concentration domain of impurities (7) of 0,9㎛, and the junction depth of the low concentration domain of impurities (5) in the drain diffusion layer as to the MISFET, manufactured of the effectiveness channel length was 0.15㎛.

GF Exhibit 1126 - 1730/2248

상기 MISFET에 있어서 측벽 절연막(19)는 소오스 및 드레인 확산층 위에서 1020㎝-3 이하의 불순물 농도 영역 표면을 덮고 있는 구성으로 되어 있다. 본 실시예에 따른 상기 MISFET의 전달 콘덕턴스는 측벽 절연막이 종래의 실리콘 산화막으로 구성되는 동일 치수의 MISFET에 있어서 전달 콘덕턴스의 약 1.1배 크다는 것을 알게 되었다.

It consists of the configuration where the side wall insulating film (19) covers the concentration domain of impurities surface less than 10 20 ㎝ -3 as to MISFET in the source and drain diffusion layer. The transfer cond uctance of MISFET according to this embodiment knew as to MISFET of the same size in which the side wall in sulating film consisted of the conventional silicon oxide film being large with about 1.1 times of the transfer co nductance.

상기의 전달 콘덕턴스의 차이는 게이트 전극(4)의 측벽에 있어서 절연막(19)의 비유전율의 차이에 차이에 따른 전속 밀도의 차이에 의한 것이라고 생각된다. 즉, 본 실시예와 같아 측벽 절연박(19)의 비유전율이 게이트 산화막의 비유전율 보다 1.6배 큰 경우에는 측벽 절연막의 비유전율이 게이트 산화막의 비유전율과 동등한 종래 구성의 MISFET의 경우보다 게이트 전계가 소오스 및 드레인 확산층의 낮은 불순물 농도 영역 표면으로 돌아 들어가는 전속 밀도가 크고, 낮은 불순물 농도 영역 표면을 보다 n형화하여 전도도를 높이기 위함이라고 생각된다.

It is regarded in the difference of the difference is the relative permittivity of the insulating layer (19) as to th e sidewall of the gate electrode (4) of the transfer con ductance described in the above as by the difference o f the electric flux density according to the difference. That is, in case it is the same as that of this embodime nt and the relative permittivity of the sidewall insulatio n tape (19) is greater than the relative permittivity of t he gate oxidation film with 1.6 times the electric flux d ensity in which the gate electric field rotates into the l ow concentration domain of impurities surface of the dr ain diffusion layer and source than the relative permitti vity of the gate oxidation film and MISFET of the equiv alent conventional composition and the relative permitti vity of the side wall insulating film enters is large and it is for the low concentration domain of impurities surfac e to the n-type more look fine and raise conductivity it is regarded.

[실시예 6]

[Embodiment 6]

제12도는 본 발명의 다른 실시예를 설명하기 위한 도면이다. 상기 제1의 실시예에 있어서 낮은 불순물농도의 드레인 확산층(5)및 소오스 확산층(6)을 형성한 후, 실리콘 게이트 전극(4)의 표면을 열산화하여 10nm의 실리콘 산화막(23)으로 게이트 전극(4)을 덮는다. 그후, 비유전율로 되는 실리콘 박막을 SiH4 가스의 화학 기상 반응을 사용해서 전면에 퇴적하였다. 퇴적막의 두께는 약0,5㎛이었다.

Figure 12 is a drawing illustrating the other embodiment of the invention. The surface of the silicon gate electro de (4) thermally is oxidated and the drain diffusion laye r (5) and source diffusion layer (6) of the low impurity concentration the gate electrode (4) are covered as to the first embodiment after doing the formation with the silicon oxide film (23) of 10nm. Thereafter, the silicon t hin film consisting of the relative permittivity was accu mulated in the front side by using the chemical vapor d eposition of the SiH 4 gas. The thickness of the heap fi lm was about 0,5㎛.

그후, 평행 평판형 반응성 스피터 장치에 의해 반도체 표면과 수직 방향으로 상기 실리콘 박막을 0.5㎛ 에칭하였다.

Thereafter, the silicon thin film 0.5㎛ was etched to the semiconductive surface and vertical direction with the parallel plate type reactive Peter apparatus.

상기 공정에 의해 게이트 전극(4)의 측벽에 얇은 실리콘 박막(23)을 거쳐서 실리콘 퇴적막(19)가 외부로 부터 격리되어 0.5㎛의 으로 남게 되었다. 상기 에칭 후는 상기 제1의 실시에에 따라서 MISFET를 제조하였다. 본 실시예에 따라서 제조한 MISFET의 전달 콘덕턴스를 측정하였을 때 실리콘 산화막으로 게이트 전극의측벽 절연막을 구성한 동일 치수의 종래 MISFET의 전달 콘덕턴스의 약 1.2배에 달하였다. 더욱 주목 되는 것은 본 실시예에 따른 MISFET의 정특성 측정후에 재차 전달 콘덕턴스를 측정하였을 때 전달 콘덕턴스는 더욱 증가하여 통상 이중 드레인 구조 MISFET의 전달 콘덕턴스의 약 1.25배까지 달한다.

Silicone heap film (19) was isolated from the outside and it remained in the sidewall of the gate electrode (4) with the process after the thin silicon thin film (23) as 0.5㎛. According to the first operation after the etc hing, MISFET was manufactured. According to the pres ent preferred embodiment, number reached about 1.2 ti mes of the transfer conductance of the conventional M ISFET of the same size organizing the gate electrode si de wall insulating film on silicon oxide film when measuri ng the transfer conductance of MISFET manufactured. More, when again measuring the transfer conductance after the static characteristics measurement of MISFE T according to this embodiment, the transfer conducta nce more increases and generally the number reaches among this to about 1.25 times of the transfer conduct ance of the drain structure MISFET to be watched.

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상기는 소오스 및 드레인 확산층이 높은 불순물 종도 분포만으로 구성되는 통상MISFET의 전달 콘덕턴스와 거의 같은 것이다. 본 실시예의 MISFET에 있어서 실효적인 전달 콘덕턴스가 향상한 제1의 이유는 측벽 퇴적막(19)의 비유전율이 실리사이드(12)와 실리콘 산화막의 값에 비해서 충분히 크기 때문이라고 생각된다. 또, 제2의 이유는 정특성의 측정으로 5V 이상의 게이트 전압을 인가하였을 때, 게이트 전극보다 정의 전하가 얇은 산화막(23)을 거쳐서 실리콘 퇴적막(19)에 천이되어 축적되고, 이 정의 축적 전하에 의해 소오스 및 드레인 확산층의 낮은 불순물 농도 영역표면이 더욱 n형화하여 전도도가 상승하였기 때문이라고 생각된다.

The impurity type in which as to the above, the source and drain diffusion layer are high is is nearly the same a s that of the transfer conductance of the formed ordin arily MISFET to the distribution. Reason for the first th e relative permittivity of the sidewall heap film (19) is e nough regarded in comparison with the value of the sili con oxide film and silicide (12) as the because why the effective transfer conductance improves as to MISFET of this embodiment to be large. And when the second r eason applied the gate voltage more than 5V to the me asurement of the static characteristics , it is transmitt ed after the oxide film (23) in which the definition elect ric charge is thin than the gate electrode in silicone he ap film (19) and it is accumulated and it is regarded th at the n-type the low concentration domain of impuriti es surface of the drain diffusion layer and source more looked fine and conductivity was due to rise with the bi modal stored charge.

즉, 실리콘 퇴적막(19)는 전기적으로 프로그램 가능한 불휘발성 메모리에 있어서의 부유 게이트의 작용을 갖는 것이라고 생각된다. 실리콘 퇴적막(19)를 정의 전하를 축적하는 부유 게이트로서 작용시키는 것은 MISFET 제조후의 좋은 품질 선택 테스트시에 특성 점검을 행할 때에 실시할 수 있으므로 제품 출하전에 전하를 주입하여 축적, 유지시키는 본 실시례의 트랜지스터에 있었어는 드레인 전계에 의한 드레인의 낮은 불순물 농도 영역의 표면 전계를 약하게 하는 적용도 갖고 있으며, 드레인 강전계에 의한 핫 캐리어의 게이트 산화막으로 주입에 따른 MISFET의 열화현상도 방지하는 다른 작용도 갖고 있다.

That is, regarded that silicone heap film (19) electrically has the action of the floating gate in the pr ogrammable nonvolatile memory. The application which injects the electric charge before the product shipment and makes the reduced surface field of the low concen tration domain of impurities of the drain by the drain el ectric field which was in accumulation, and the transist or of this operation example which maintained weak sin ce it can perform to operate silicone heap film (19) as t he floating gate accumulating the definition electric ch arge when performing the characteristic test in the goo d quality selection test after the MISFET manufacture has and the dissimilar action of the degradation of MIS FET according to injection preventing to the gate oxida tion film of the hot carrier by the drain strong electric fi eld has.

이상과 같이 하면 ,게이트 측벽에 있어서 프린지 용량을 개재한 게이트 전계의 영향을 소오스 및 드레인의 낮은 불순물 농도 영역 표면에 강하게 영향을 줄 수가 있고, 실효적인 전달 콘턴스를 종래 구조에 비해서 1.1~1.2배 이상 크헤 할 수 있다.

As described above, the influence is strong against the low concentration domain of impurities surface of the d rain and source the influence the influence of the gate electric field which interposes the fringe capacitance a s to the , gate sidewall if it does can be given and the effective transmission cone turns can be done in comp arison with the conventional structure over 1.1~1.2 ti mes with ***.

본 발명의 기본적인 개념에 따르면, 측벽 퇴적막은 실리콘 질화막에 한정되는 것은 아니고, 알루미나(Al2O3)탄달 산화막(Ta2O5), 티타늄(TiO2), 지르코늄 산화막(Zr2O3), 하프늄 산화막(Hf2O3)등 실리콘 산화막의 비유전율 보다 충분히 큰 비유전율을 갖는 유전체이면 좋다.

According to the cardinal concept of the invention, it is better that the sidewall heap film is not restricted to th e silicon nitride film and it is the dielectric which enoug h has the big relative permittivity as compared with the relative permittivity of the oxide film (Ta(SB)2(/SB)O(S B)5(/SB)), the titanium (TiO(SB)2(/SB)), the zirconium oxide layer (Zr(SB)2(/SB)O(SB)3(/SB)), the silicon oxid e film including the hafnium dioxide layer (Hf(SB)2(/SB) O3) etc which is sweet with the alumina (Al(SB)2(/SB) O(SB)3(/SB)) coal.

또, 본 발명에 의한 전달 콘덕턴스의 향상 효과는 게이트 측벽에 반도체 등으로 구성되고, 외부에서 격리된 부유 게이트 또는 외부에서 격리되 전하 축적 기구를 갖는 절연막 또는 절연막 사이의 경계면에서 형성되어도 좋으며, 외부에서 격리된 측벽 퇴적막은 실리콘에 한정되는 것은 아니고, 다른 반도체 예를 들면, 실리콘 카바이드(SiC)나 게르마늄(Ge)등이라도 좋고, 또 실리콘 질화막이나 알루미나막 등의 절연막이라도 좋다.

And the enhancement effect of the transfer conductance according to the invention comprises the semiconductor in the gate sidewall etc. And in the float ing gate or the outside isolated in the outside, it is goo d even if it is formed at the boundary face between th e insulating layer having the isolation measure charge a ccumulation tool or the insulating layer and the sidewall heap film isolated in the outside is not restricted to the silicone and it is good although it is the dissimilar semic

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onductor, for example, the silicon carbide (SiC) or the germanium (Ge) etc. and it is good although it is and, t he insulating layer lice including the silicon nitride film o r the alumina film etc.

[발명의 또 다른 실시예]

[Another preferred embodiment of the invention]

본 발명은 드레인 확산층에 있어서의 높은 불순물 농도 영역에 관해서 종래의 상식에 구애받지 않고 그 물리적 근간에 까지 되돌아가 해석한 결과에 기인한다. 즉, 여러가지의 드레인 확산층 농도를 갖는 MISFET에 있어서 드레인 확산층 표면에 고융점 금속의 실리 사이드 층을 형성 하였을 때, 인(P) 및 비소(As)등의 도전형의 불순물로 상기 드레인 확산층이 형성되어 있는 경우에 한하여 드레인 확산층 표면에 불순물 농도가 약 10nm의 깊이로 고농도화 되는 현상이 있다. 즉, NMOS에 있어서는 드레인 확산층 표면 불순물 농도가 1#215#1018㎝-3이상이면 상기 실리사이드 층과 반도체 표면 사이에 양호한 옴특성이 얻어져 NMOS로서의 특성에 아무런 문제도 생기지 않는다는 사실이 발견되었다.

It is caused by the result in which the invention is not restricted by the conventional common sense about th e high concentration domain of impurities in the drain di ffusion layer and returning in the physical basis and int erpreted. That is, in case the drain diffusion layer is for med with the impurity of the conductivity type includin g the phosphorus (P) and arsenic (As) etc. it is limited and when the silicide layer of the high melting point me tal in the drain diffusion layer surface as to MISFET ha ving the drain diffusion layer concentration of the vario us is formed, the phenomenon that is highly enriched h as the impurity concentration in the drain diffusion laye r surface to the depth of about 10nm. That is, the fact that the good ohmic property was obtained between th e silicide layer and semiconductive surface if it was in NMOS and the drain diffusion layer surface impurity con centration was 1× 10 18 ㎝ - 3 or greater and any prob lem was not generated in property as NMOS was disco vered.

통상의 MISFET에 있어서의 드레인 확산층은 반도체 기판 표면 부근에서 1020㎝-3이상의 높은 불순물농도 영역을 가지며, 기판 내부를 향해서 가우스 분포, 또는 오차함수 분포로 감쇠하는 불순물 농도 분포를 갖는다.

The drain diffusion layer in the normal MISFET includes the high concentration domain of impurities more than 10 20 ㎝ - 3 in the surface of semiconductor substrate vicinity, and the Gaussian distribution towards the insid e substrate or the impurity concentration distribution d amping to the error-function distribution.

상기의 통상 드레인 확산층에 전압을 인가하고, 이 즉, 불순물 농도의 함수로서 인가 전계를 해석하면, 1020㎝-3이상의 높은 불순물 농도 영역에 있어서는 매우 약한 전계밖에 인가되지 않는다는 사실이 판명되었다. 이 사실은, 초미세MISFET의 고내압화의 관점에서 보면, 높은 불순물 농도의 존재는 도리어 유해하고, 드레인 확산층의 최대 불순물 농도는 1019㎝-3이하로 구성되는 것이 바람직하다는 것이 판명되었다. 상기의 1020㎝-3이상의 높은 불순물 농도 영역의 MISFET에 있어서의 역할은 확산층 정항의 저감화와 배선 금속의 양호한 옴접촉의 확보에 있지만, 상기 후자의 역활 즉, 배선 금속과의 양호한 옴접촉은 1#215#1018 ㎝-3이상의 표면 불순물 농도를 갖는 드레인 확산층 위의 실리사이드 층의 구조에 의해서 치환이 가능하다. 상기 전자의 역할, 즉 소오스 확산저항 및 드레인 확산저항의 저감화에 관해서는 소오스 및 드레인 확산층 표면의 실리사이드화에 의해 실현되는 것이 알려져 있고 , 특히 초미세 트랜지스터에 있어서의 매우 얕은 접합 형성에서는 실리사이드화에 의한 저항 저감의 효과는 현저한 것이 있다.

The voltage the generally was applied of the above in the drain diffusion layer and if the applied field was inte rpreted as the , in other words, the function of the imp urity concentration , the fact that was in the high con centration domain of impurities more than 10 20 ㎝ - 3 and was not applied to the outside electric field which was very weak was confirmed. If this fact looked aroun d the viewpoint of the high voltage-resistant of the ult ra-fine MISFET , the high presence of the impurity con centration was rather harmful and this fact was proven that this fact was sweet that the maximum impurity co ncentration of the drain diffusion layer was formed less than 10 19 ㎝ - 3 . The high role in MISFET of the conc entration domain of impurities more than 10 20 ㎝ - 3 d escribed in the above is in the security of the good oh mic contact of the reduction of the diffusion layer cons tant resistance and wiring metal. However the substitu tion is possible with the structure of the silicide layer a bove the drain diffusion layer in which good said later r ole the , in other words, the ohmic contact of the wirin g metal has the surface impurity concentration more th an 1× 10 18 ㎝ - 3 . It is known about the role of the e lectron, in other words, the reduction of the drain diffu sion resistance and source diffusion resistance to be re alized by the salicidation of the drain diffusion layer sur face and source and it has that the effect of the resist ance reduction by the salicidation is very significant es pecially, the ultra-fine transistor in the shallow junction formation.

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그리하여, 본 발명의 CMOSFET는 상기의 해석 결과에 따른 개념을 발전시켜 드레인 확산층의 높은 불순물 농도 영역을 드레인 확산층과 옴 접촉으로 결합된 얇은 실리사이드 층으로 치환하고 , 또한 드레인 확산층의 불순물 농도에 관한 최적 조건을 해석적으로 구한 결과를 이용하는 것이다.

And the result in which the CMOSFET of the invention develops the concept according to the interpretation r esult described in the above and which substitutes for the high concentration domain of impurities of the drain diffusion layer with the thin silicide layer which is combi ned to the drain diffusion layer and ohmic contact and which analytically saves moreover, the optimal conditio n about the impurity concentration of the drain diffusio n layer is used.

상기 최적조건은 특히 0.5㎛이하의 게이트 길이를 갖는 초미세 MISFET의 고내압화 및 래치 업 방지에 관한 최적 조건이다.

It is the optimal condition about the high voltage-resistant of the ultra-fine MISFET in which the optimal condition has especially, the gate length less than 0.5 ㎛ and latch-up protection.

제13도 및 제14도는 각각 본 발명에 의한 해석 결과를 도시한 도면으로서, 드레인 확산층 표면 불순물 농도의 함수로써 구한 소오스 및 드레인 내압 및 최대 기판 전류의 곡선을 표시하고 있다.

As Figure 13 and drawing in which figure the fourteenth shows the interpretation result according to the inventi on, the source, saved the drain internal pressure and c urve of the maximum substrate current are indicated as the function of the drain diffusion layer surface impurit y concentration.

제13도에 있어서는 소오스와 드레인 사이의 내압으로서 전자사태 항복전압을 점선으로 표시하고, 펀치 스루 내압을 실선으로 표시하고 있다. 각 내압 모두 찬넬 길이의 함수로서 각각 구하고 있다.

It is in Figure 13 and the electron avalanche breakdown voltage is indicated by the dotted line as th e internal pressure between the drain and the source a nd the punch-through breakdown voltage is indicated b y the solid line. It altogether saves as the function of t he channel length with each internal pressure.

제13도에 있어서 전자사태 항복전압은 PMOS에 관한 것이고 , NMOS의 값의 전체적으로 표시된 곡선보다 0.1~1(V) 저하하는 경향에 있다. 펀치 스루 내압에 대해서는 PMOS와 MNOS의 값 사이에 다른 것은 발견되지 않는다.

It is in the tendency to the electron avalanche breakdown voltage be as to Figure 13 about PMOS and be degraded than the curve which on the whole, is indi cated of the value of the , NMOS with 0.1~ 1 (V). The other is not discovered about the punch-through break down voltage between the value of MNOS and PMOS.

제13도에서 새로이 명확하게 된 사실은 찬넬 길이가 0.5㎛ 이상의 트랜지스터에 있어서는 드레인 확산층의 표면 불순물 농도를 3#215#1018㎝-3으로 설정하면, 통상 구조의 동일 치수의 트랜지스터에 있어서 소오스 및 드레인 내압에 비해서 약 2배에 해당하는 10V 이상의 내압을 실현할 있는 것이다. 또, 찬넬 길이가 0.4㎛ 이하의 트랜지스터에 있어서는 찬넬 길이에 의존해서 각각 최적의 드레인 확산층 표면 불순물 농도를 약 1#215#1018㎝-3으로 설정하면, 소오스 및 드레인 내압을 약 7V로 까지 향상할 수가 있다. 찬넬 길이가 0.2㎛의 PMOS 트랜지스터에 있어서는 5#215#1017의 드레인 표면 불순물 농도로 설정하면, 약 5V의 내압이 얻어지게 된다.

In Figure 13, if it is in the transistor more than 0.5㎛ and as to the fact, that is afresh clear the channel len gth sets up the surface impurity concentration of the d rain diffusion layer as 3× 10 18 ㎝ - 3 , the fact, has. I t realizes the internal pressure more than 10V correspo nding to about two times as to the transistor of the sa me size of the trading structure in comparison with the source and drain internal pressure. And if it is in the tra nsistor less than 0.4㎛ and the channel length depends on the channel length and the optimal drain diffusion la yer surface impurity concentration is set up as about 1 × 10 18 ㎝ - 3 , the source and drain internal pressure can be improved to about 7V. If it is in the PMOS transi stor of 0.2㎛ and the channel length sets up as the drai n surface impurity concentration of 5× 10 17 , the inte rnal pressure of about 5V is obtained.

다음에, 제14도에 있어서는 드레인 전류에 의해 유기되는 소수 캐리어가 기판측으로 흐르는 기판 전류를 게이트 전압의 함수로써 구하고, 그 최대로 되는 값, 즉 최대 기판 전류를 드레인 확산층 표면 불순물 농도의 함수로서 해석한 것이다.

Next, it is in Figure 14 and the substrate current in which the minority carrier induced with the drain curren t flows toward the substrate side is saved as the funct ion of the gate voltage and the maximized value, in oth er words, the maximum substrate current is interpreted as the function of the drain diffusion layer surface impu rity concentration.

제14도에서는 찬넬 길이 1.0㎛, 찬넬 폭 10㎛의 MISFET에 관해서 소오스 및 드레인 확산층의 접합 깊이를 파라미터로 하고 , 드레인 전압은 5V이다.

In Figure 14, it has the junction depth of the drain diffusion layer and source as the parameter about the channel length 1.0㎛, and MISFET of the channel width

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10㎛ and the , drain voltage is 5V.

제14도에서 새로이 명확하게 된 사실은 드레인 접합 깊이에 다소 의존하지만 , 드레인 확산층 표면 농도를 1017내지 1018㎝-3으로 설정하면, 기판전류를 통상구조의 것에 비해서 현저하게 개선할 수가 있어 래치 업 현상을 방지할 수도 있다.

In Figure 14, if the fact that is afresh clear a bit depends on the drain conjugation depth but the , drain diffusion layer surface concentration is set up as 10 17 to 10 18 ㎝ - 3 , the substrate current can be remarka bly improved in comparison with of the trading structur e and the latch-up can be prevented.

내 래치 업 현상에 대한 최적 표면 불순물 농도의 드레인 확산층 위에 실리사이드층을 형성하면, 음접촉은 얻을 수 없고, 쇼트키 장벽이 형성된다.

If the silicide layer is formed on the drain diffusion layer of the optimal surface impurity concentration about my latch-up , the negative principle in nature contact can not obtain and the Schottky barrier is formed.

본 발명에 있어서는 제13도 및 제14도에서 얻어진 새로운 해석결과와 상술한 2건의 참고문헌에 따라서 지금까지 없었던 고내압에서 내 래치 업의 초미세 CMOS FET를 실현하였다. 즉, 발명의 CMOSFET에 있어서는 PMOS를 간디 2건의 문헌에 따른 쇼트키 장벽의 드레인 접합으로 형성하고, 한편 NMOS에 대해서는 제13도에서 얻어진 새로운 해석 결과에 따라서 1018㎝-3이상의 표면 불순물 농도를 갖는 확산층과 음접촉을 갖는 실리사이드등의 조합으로 드레인 접합을 형성하고 있다. 이것에 의하여 내 래치 업 특성 향상 이외의 PMOS 및 NMOS의 각 소오스 드레인 확산층의 표면 불순물 농도를 0.5㎛이하의 초미세 COMSFET의 고내압화의 관점에서 더욱 최적화 하는 것이 가능하게 된다.

It was in the invention and the ultra-fine CMOS FET of my latch up was realized with the new interpretation re sult which was obtained in Figure 13 and Figure 14 in t he high voltage-resistant which there was so far no ac cording to the above-described reference of 2 cases. T hat is, in CMOSFET of the invention and PMOS is forme d into the drain junction of the Schottky barrier accordi ng to the literature of the Gandie 2 cases and the drain junction is formed into the combination including the dif fusion layer having the surface impurity concentration more than 10 18 ㎝ - 3 according to the new interpreta tion result which is obtained about NMOS in Figure 13 a nd silicide etc. in the meantime. Having the negative pr inciple in nature contact. According to this, in the view point of the high voltage-resistant of the ultra-fine CO MSFET less than 0.5㎛ the surface impurity concentrati on of each source drain diffusion layer of PMOS except my latch up property improvement and NMOS, it is poss ible to more optimize.

[실시예 7]

[Embodiment 7]

제15도, 제16도 및 제17도는 각각 본 발병의 제7의 실시예를 도시한 CMOSF ET의 제조공정의 단면 구조도이다.

With the 15, is Figure 16. And figure 17 is a sectional configuration of the manufacturing process of the CMO SF ET showing the seventh embodiment of the onset lo oked.

제15도~제17도에 있어서 (221)은 n도전형으로 비저항 0.4Ω.㎝의 실리콘 기판이며, 이 기판(221)의 소정의 위치에 붕소를 접합깊이 2㎛, 표면 불순물 농도 1#215#1016㎝-3으로 확산하고, P오전형 웰(222)를 형성한다. 다음에 공지의 소자 분리 기술을 이용해서 0.5㎛의 두꺼운 필드 산화막(223)을 선택적으로 형성한 후 활성 영역의 반도체 표면을 노출하고 20㎚의 막의 두께를 갖는 깨끗한 게이트 산화막(28)을 형성한다. 그후, 약 0.4㎛두께의 실리콘 박막을 게이트 산화막(28)위에 형성하고, POC3을 확산원으로 하는 열 확산에 의해 상기 실리콘 각막에 인(P)의 고농도 확산을 행한다. 다음에 상기 실리콘 박막 표면을 열산화 하고 0.2㎛두께의 실리콘 산화막을 상기 실리콘 박막위에 형성한다. 그후, 리도그래피에 의해 상기 실리콘 산화막 및 실리콘 박막을 바라는 회로구성에 따라서 동시에 제거하고, 게이트 보호 절연막(212) 및 게이트 전극(29)를 각각 남겨 놓는다. 그리고, 상기 리도그래피 후의 게이트 전극(29)의 폭 즉, 찬넬폭으로서는 1.0, 0.5, 0.3, 0.2 및 0.1㎛의 5개 조건에 대해서 실시하였다.

The 15 (221) is the silicon substrate of the resistivity 0.4Ω ㎝. as to figure the seventeenth to the n conduct ivity type and boron is diffused to the predetermined p osition of this substrate (221) to the junction depth 2 ㎛, and the surface impurity concentration 1× 10 16 ㎝ - 3 and the gate oxidation film (28) which selectively e xposes the semiconductive surface of the active area t he thick field oxide film (223) of 0.5㎛ after doing the fo rmation by it forms P forenoon type well (222) next usi ng the publicly known isolation technology and has the thickness of the film of 20㎚ and is clean is formed ther eafter the silicon thin film of about 0.4㎛ thickness is fo rmed on the gate oxidation film (28) and the high conc entration diffusion of the phosphorus (P) is performed with the thermal diffusion the POC 3 to the diffusion so urce in silicone cornea the silicon thin film surface ther mally is oxidated to the next and the silicon oxide film o f 0.2㎛ thickness is formed on the silicon thin film it sim ultaneously removes with lithography according to the circuit configuration wanting the silicon oxide film and s ilicon thin film and the gate protective insulator film (21 2) and gate electrode (29) are left respectively. And it performed about 5 the condition of 0.1㎛ and 1.0, 0.5,

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0.3, 0.2 as the width of the gate electrode (29) after t he lithography, in other words, the channel width.

상기 리도그래피 후, 테트라 에톡시실란(Si(OC2HS)4)를 사용한 화학 기상 반응에 의해 0.3㎛의 막의 두께를 갖는 실리콘 산화막을 전면적으로 퇴적시킨다. 상기 퇴적막을 반응성 스피터 에칭에 의해 반도체 기판 표면과 수직방향으로 에칭하고, 평탄부에 퇴적된 실리콘 산화 퇴적막을 제거하면 게이트 전극(29) 및 필드 산화막(223)의 각 측벽부분에만 실리콘 산화 퇴적막(213)이 남게 된다. 다음에 0.8㎛두께의 포트 레지스트막을 웰(222)를 제외한 영역의 게이트 산화막(28)위에 남겨 놓고, 가속 에너지 70KeV의 조건에서 비소(As)의 이온주입을 행한다. 상기의 이온주입은 웰 영역(222)에 대해서는 게이트 산화막(28)을 거쳐서 행하여지고, 반도체 기판 표면에서 최대 불순물 농도로 되는 조건이다. 한편, 웰 영역(222)이외에 대해서는 상기 포트 레지스트막에 의해 주입 이온이 저지되어 반도체 기판(221)내에는 주입되지 않는다. 상기의 이온 주입후, 남겨진 포트 레지스트막을 제거하고 나서 주입 이온의 활성화, 열처리를 실시하고, N도 전형의 소오스(24) 및 드레인(25)를 형성한다(이상 제15도).

The silicon oxide film having the thickness of the film of 0.3㎛ with the chemical vapor deposition using the tetr aethoxysilane (Si(OC(SB)2(/SB)H(SB)S(/SB))(SB)4(/S B)) the extensively is sedimented after lithography. Th e heap film is etched to the surface of semiconductor s ubstrate and vertical direction with the reactive Peter etching and if the silicon oxidation heap film accumulat ed in the plateau is removed, the silicon oxidation heap film (213) remains in each sidewall portion of the field o xide film (223) and gate electrode (29). Next, the phot oresist film of 0.8㎛ thickness is left on the gate oxidati on film (28) of the domain except for the well (222) an d the ion implantation of the arsenic (As) is performed i n the condition of the acceleration energy 70KeV. The i on implantation described in the above is performed ab out the well region (222) after the gate oxidation film (28) and it is the condition consisting of the maximum i mpurity concentration in the surface of semiconductor substrate. In the meantime, the photoresist film hinder s the implant ion and it is not injected about the well r egion (222) except within the semiconductor substrate (221). After the photoresist film remaining is removed t he activation of the implant ion, and the thermal proce ss is performed after the ion implantation described in t he above and N forms the source (24) and drain (25) o f the model (over the 15).

그리고, 상기의 소오스 및 드레인 확산층(24), (25)의 각각의 표면 불순물 농도는 찬넬 길이가 0.5㎛이상 일때에는 3#215#1018, 0.3㎛이하 일때에는 1#215#1018㎝-3으로 최종적으로 형성되도록 비소(As) 이온 양을 설정한다. 도, 상기의 소오스(24), 드레인(25)의 확산층의 접합 깊이가 최종적으로 0.25㎛가 되도록 상기의 열처리 조건을 제어한다. 상기 열처리후, 웰 영역(222)위에만 0.8㎛두께의 포트 레지스트막으로 덮고, 붕소를 가속 에너지 70KeV의 조건으로 이온 주입을 행한다. 상기의 이온 주입에 의해 웰 영역(222)이외의 영역에 있어서 게이트 산화막(28)을 거쳐서 붕소가 반도체 기판(221)에 주입되고, 그 최대 불순물 농도는 반도체 기판(221)의 표면이었다. 웰 영역(222)에 있어서는 상기 포토 레지스트막에 의해 이온 주입이 저지되어 반도체 기판(221)내에 주입되지 않는다. 상기의 이온주입 후, 남겨진 포트 레지스트막을 제거하고 나서 주입 붕소 이온의 활성화 열처리를 실시하고, P도전형의 소오스(26)및 드레인(27)을 형성한다(이상 제16도 참조).

And the source described in the above and drain diffusion layer (24), and each surface impurity concent ration of (25) are for the establishment of the arsenic (As) ion dose when it is less than 3× 10 18 , 0.3㎛ whe n the channel length is 0.5㎛, the finally is formed with 1× 10 18 ㎝ - 3 . Drawing, the source (24) described in the above, and the junction depth of the diffusion laye r of the drain (25) control the heat treatment condition described in the above so that 0.25㎛ finally. It covers up with the photoresist film of 0.8㎛ thickness on the p ost-baking, and the well region (222) and boron the ion implantation is performed into the condition of the acce leration energy 70KeV. Boron was injected with the ion implantation described in the above as to the domain e xcept the well region (222) after the gate oxidation film (28) in the semiconductor substrate (221) and the max imum impurity concentration was the surface of the se miconductor substrate (221). It is in the well region (2 22) and the photoresist film hinders the ion implantatio n and it is not injected within the semiconductor substr ate (221). After the photoresist film remaining is remov ed the activation annealing of the injection boron ion is performed after the ion implantation described in the a bove and the source (26) and drain (27) of P conductiv ity type are formed (over the 16 is the reference).

상기 소오스(26) 및 드레인(27)의 확산층의 각각의 표면 불순물 농도는 최종적으로 3종류의 조건 3#215#1017㎝-3, 1#215#1018㎝-3로 되도록 주입 붕소량을 설정한다. 또, 소오스(26)및 드레인(27)의 확산층의 접합 깊이가 최종적으로 0.25㎛로 되도록 상기의 열처리 조건을 제어한다. 상기 열처리 후, 반도체 기판(221)위에 노출되어 있는 게이트 산화막을 제거하

Each surface impurity concentration of the diffusion layer of the source (26) and drain (27) are for the esta blishment of finally, the condition 3× 10 17 ㎝ - 3 of 3 kind, and 1× 10 18 ㎝ - 3 , as as possible, the injection boron amount. And finally the junction depth of the diff usion layer of the source (26) and drain (27) control th

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고 나서 50㎚의 막의 두께를 갖는 백금(Pt)을 스피터링 법에 의해 전면에 증착하고, 계속하여 450℃의 열처리를 실시한다. 상기의 저온 열처리에 의해 반도체 기판(221)의 표면에 노출하고 있는 소오스 확산층 영역(24) 및 (26), 드레인 확산층 영역(25) 및 (27)의 각 표면 부분에 백금 실리사이드(PtSi)층(214)가 자기 정합적으로 형성된다. 상기의 열처리에 있어서 필드 산화막(223), 측벽 퇴적 산화막(213) 및 보호 산화막(212)위에서 백금(Pt)은 반응하지 않으므로 실리사이드층(214)는 형성되지 않는다. 상기의 저온 열처리 후, 왕수로 전면적에 백금(Pt)을 에칭한다. 백금 실리사이드(PtSi)는 왕수로 제거되지 않아 소오스 확산층(24) 및 (26)과 드레인 확산층(25) 및 (27)위에만 자기 정합적으로 남게 된다. 이 시점에서는 N도전형의 소오스(24) 및 드레인(25)영역에 있어서의 백금 실리사이드(PtSi)층(214)의 바로 아래에는 백금 실리사이드층 형성전의 표면 불순물 농도보다도 1자리수 높은 불순물 농도를 갖는 약 10㎚두께의 석출층의 백금 실리사이드(PtSi)층(214)에 대해 자기 정합적으로 형성된다.

e heat treatment condition described in the above to 0.25㎛ as as possible. The platinum (Pt) which has the thickness of the film of 50㎚ after it removes the gate oxidation film exposed on the post-baking, and the sem iconductor substrate (221) is deposited on front with t he spirofluorene method and then, the thermal process of 450℃ is performed. The platinum-silicide (PtSi) layer (214) is formed in the source diffusion layer domain (2 4) and (26) exposing on the surface of the semiconduc tor substrate (221), and each surface part of (27) and drain diffusion layer domain (25) with the anneal descri bed in the above into the self-alignment manner. The si licide layer (214) is not formed since the platinum (Pt) does not react as to the thermal process described in t he above in the field oxide film (223), and the sidewall deposition oxide layer (213) and passivation (212). The platinum (Pt) is etched to the aqua regia after the ann eal described in the above. The platinum-silicide (PtSi) is not removed to the aqua regia and it remains as the self-alignment manner on the source diffusion layer (2 4), (26), the drain diffusion layer (25) and (27). At this moment, it is formed with the self-alignment manner ab out the platinum-silicide (PtSi) layer (214) of the precip itation layer of about 10㎚ thickness having the impurit y concentration which the single digit is beneath higher than the surface impurity concentration of the platinum silicide layer formation total of the platinum-silicide (Pt Si) layer (214) in the source (24) of N conductivity typ e and drain (25) domain.

백금 실리사이드층(214)형성후, 모노실란(SiH4)과 산소(O2)의 화학 기상 반응에 의해 약 500㎚두께의 실리콘 산화막(210)을 전면에 퇴적하고, 소오스(24) 및 (26), 드레인(25) 및 (27)위, 또 게이트 전극(29)위의 접촉구멍을 구성시키는 부분의 상기 실리콘 산화막(210)를 리도그래피에 의해 선택적으로 제거한다. 상기의 실리콘 산화막(210)의 선택적 제거를 한 후, 상기 공정에 사용한 포트 레지스트막을 남겨둔 채, 티타늄(Ti)와 텅스텐(W)의 동시 스퍼터에 의해 TiW 막(215)를 전면에 피착시킨다. 그후, 상기 포토 레지스트막을 제거하지만, 이 공정에 의해 포트 레지스트막 위의 TiW막도 동시에 제거되기 때문에 실리콘 산화막(210)이 제거된 영역에만 선택적으로 TiW막(215)가 남게 된다. 최후로 바라는 회로구성에 따라서 알루미늄(Al)에 의한 배선(211)을 형성한다(이상 제17도 참조).

The silicon oxide film (210) of about 500㎚ thickness is accumulated after the platinum silicide layer (214) form ation with the chemical vapor deposition of the oxygen (O(SB)2(/SB)) and monosilane (SiH(SB)4(/SB)) in the fr ont side and after the silicon oxide film (210) of the par t organizing the contact hole above the gate electrode (29) is selectively removed with lithography and the sel ective removal of the silicon oxide film (210) described i n the above is done with the source (24) and (26), and the drain (25) and (27) the upper part the photoresist film used in the process is left. The TiW film (215) is at tached in the front side with the same time sputtering of the tungsten (W) and titanium (Ti) thereafter the ph otoresist film is removed. However because the simulta neously the TiW film above the photoresist film is remo ved using this process the TiW film (215) selectively re mains in the domain from which the silicon oxide film (2 10) is removed the wiring (211) by the aluminum (Al) is formed according to the circuit configuration which it la stly hopes in their heart (over seventeenth is the refer ence).

그리고, TiW막(215)는 알루미늄 배선(211)과 실리사이드층(214)의 반응을 방지하기 위해서 필요하게 된다.

And the reaction is necessary so that the TiW film (215) prevent the reaction of the silicide layer (214) an d aluminium wiring (211).

다음에, 상기 제조 공정에 의해서 제조된 CMOSFET에 관하여 우선, 소오스와 드레인 사이의 내압을 측정하였을때, 다음의 결과를 얻었다. 즉, P도전형의 소오스(26) 및 드레인(27)의 각 확산층에 있어서의 표면 불순물 농도를 3#215#1037㎝-3

Next, first when the internal pressure between the drain and the source were measured about CMOSFET m anufactured by the manufacturing process , the followi ng result was obtained. That is, it was in PMOS setting

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으로 설정한 PMOS에 있어서는 쇼트키 특성을 나타내지만, 찬넬 길이가 0.2㎛이상의 MOSFET의 내압은 약 5V의 값을 얻을 수가 있었다. 이 값은 P전형 드레인 표면 불순물 농도가 1018㎝-3이상에서 구성되는 종래 구조의 MOSFET에 있어서의 내압의 2배 이상의 값이다. P도전형 드레인 표면 불순물 농도를 1#215#1018㎝-3으로 설정한 PMOS에 있어서는 P+N접점에 따른 트랜지스터 특성을 표시하지만, 그 소오스와 드레인 사이의 내압은 찬넬 길이가 0.3㎛이상의 MOSFET에 있어서 6.5 내지 7V로 되었다. 이 값은 종래의 값에 비해서 1.6 내지 1.7 배 이며, 고내압화가 실현된 것을 나타내고 있다. 또, P도전형 드레인 표면 불순물 농도를 3#215#1018㎝-3로 설정한 PMOS있어서도 P+N접합에 따르는 특성을 나타내지만, 그 소오스와 드레인 사이의 내압은 찬넬 길이가 0.5㎛이상의 MOSFET에 있어서는 약 12V로 되었다. 이 값을 종래의 값에 비해서 2V 이상 높고, 고내압이 실현되게 된다.

up the surface impurity concentration in each diffusion layer of the source (26) of P conductivity type and drai n (27) as 3× 10 37 ㎝ - 3 and the schottky property w as shown. However the channel length the internal pre ssure of MOSFET more than 0.2㎛ could obtain the valu e of about 5V. This value is the value in which P model drain surface impurity concentration is formed in 10 18 ㎝ - 3 or greater more than two times of the internal pr essure in MOSFET of the conventional structure. It wa s in PMOS setting up P conductivity type drain surface impurity concentration as 1× 10 18 ㎝ - 3 and the tran sistor characteristic according to the P+N contact poin t was indicated. However in the internal pressure betw een the drain and the source, the channel length were as to MOSFET more than 0.3㎛ to 6.5 through 7V. This value is 1.6 through 1.7 times in comparison with the c onventional value and it shows that the high voltage-r esistant is realized. And even by being PMOS setting u p P conductivity type drain surface impurity concentrat ion as 3× 10 18 ㎝ - 3 the property of following the P+ N junction was shown. However it was in MOSFET more than 0.5㎛ and in the internal pressure between the dra in and the source, the channel length were to about 12 V. It is this value high in comparison with the conventi onal value over 2V and the high voltage-resistant is re alized.

N도전형의 소오스(4) 및 드레인(5)의 각 확산층에 있어서의 표면 불순물 농도를 3#215#1018㎝-3으로 설정한 NMOS에 있어서 찬넬 길이가 0.5㎛이상의 MOSFET에 있어서는 그 소오스와 드레인 사이의 내압은 약 10V이었다. 이 값은 종래의 값에 비해서 약 2배의 값이며, 고내압화가 되게 된다. 드레인 표면 불순물 농도를 1#215#1018㎝-3으로 설정한 NMOS에 있어서도 소오스(24) 및 드레인(25)와 실리사이드층(214)의 사이에는 양호한 음특성이 확보되어 P+N 접합에 따흐는 트랜지스터 특성이 얻어졌다. 그 소오스와 드레인 사이의 내압은 찬넬 길이에 의존하고, 찬넬 길이가 0.3㎛MOSFET에서는 약 3V로 되었다. 이들의 값은 종래 구조의 NMOS에 있어서의 소오스와 드레인 사이의 내압에 비해서 2배 이상의 고내압화로 된다.

It was in MOSFET more than 0.5㎛ and the channel length the internal pressure between the drain and the source was about 10V as to NMOS setting up the surfa ce impurity concentration in each diffusion layer of the source (4) of N conductivity type and drain (5) as 3× 10 18 ㎝ - 3 . This value is the value of about two time s in comparison with the conventional value and it bec omes the high voltage-resistant. In the interval of the source (24) as to NMOS setting up the drain surface im purity concentration as 1× 10 18 ㎝ - 3 and drain (25) and silicide layer (214), the good negative characteristi c was secured and as to ***, the transistor characteri stic was obtained in the P+N junction. The internal pre ssure between the drain and the source depended on t he channel length and the channel length was in 0.3㎛ MOSFET to about 3V. Their value is in comparison with the internal pressure between the source in NMOS of t he conventional structure and the drain to the high vol tage-resistant more than two times.

본 실시예에 따른 CMOSFET에 있어서의 NMOS 및 PMOS의 소오스와 드레인 사이의 내압은 제13도에 도시한 해석결과의 매우 잘 일치하고 있으며, 상기 해석의 타당성이 증명되게 된다. 즉, 본 실시예에 의하면 0.5㎛이하의 찬넬 길이를 갖는 초미세 CMOSFET의 소오스와 드레인 사이의 내압을 종래에 비해서 2배이상 향상시킬 수가 있다. 구체적으로는 찬넬 길이가 0.5㎛이상의 CMOSFET에 있어서는 NMOS 및 PMOS의 각 소오스 및 드레인 확산층 표면 불순물 농도를 3#215#1018㎝-3으로, 찬넬 길이가 0.3㎛일때에는 상기 불순물 농도를 1#215#1018㎝-3로 설정해서 본 실시예에 따라 MOSFET를 완성시키면, 각각 10V 및 6V의 고내압 초미세 COMSFET를 얻을 수가 있다. 또, 찬넬길이가 0.2㎛일때에는, PMOS의 소오스 및 드레인 확산층이 표면 불순물 농도를 3#215#1017㎝-3으로, NMON의 상기 표면 불순물 농도를 1#215#1018㎝-3에 각각 설움직여써하고, 본 실시예에 따라서 MOSFET를 완성시키면, 소오스와 드레인 사이의 내압 3V의 초미세 CMOSFET를 얻을 수가 있다. 상기의 MOSFET에 있어서 POMS의 소오스(26)

The internal pressure between the source of NMOS in CMOSFET according to this embodiment and PMOS and drain very well coincide with Figure 13 and it shows the feasibility of the interpretation is proved. That is, accor ding to this embodiment, in comparison with the conve ntional invention, the internal pressure between the so urce of the ultra-fine CMOSFET having the channel len gth less than 0.5㎛ and the drain can be improved over two times. Specifically, if it is in CMOSFET more than 0.5㎛ and when the channel length is 0.3㎛, the impurit y concentration is set up as 1× 10 18 ㎝ - 3 and accor ding to the present preferred embodiment, the channel length completes MOSFET each source of NMOS and P MOS and drain diffusion layer surface impurity concentr ation to 3× 10 18 ㎝ - 3 , the high voltage-resistant ult ra-fine COMSFET of 6V and 10V can be obtained. And when the channel length was 0.2㎛ , the source and dr ain diffusion layer of PMOS were the surface impurity c

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및 드레인 (27)과 실리사이드층(214)의 사이에는 쇼트키 장벽이 형성되지만, 특성상 문제로 되지 않는다. 이 쇼트키 장벽은 오히려 내 래치 업 특성을 향상시키는 기능을 갖추고 있다.

oncentration of NMON the surface impurity concentrati on the sorrow work to 3× 10 17 ㎝ - 3 in 1× 10 18 ㎝ - 3 and according to the present preferred embodiment, i f MOSFET is completed , the ultra-fine CMOSFET of the internal pressure 3V between the source and the drain can be obtained. In the interval of the source (26) of P OMS as to the MOSFET described in the above and drai n (27) and silicide layer (214), the Schottky barrier is f ormed. However it does not consist of the property pro blem. This Schottky barrier has the function rather of i mproving my latch up property.

다음에, 본 실시예에 표시한 제조 공정에 의해 제조된 CMOSFET에 대해서 내 래치 업 특성을 평가한다. 내 래치 업 특성으로서는 다음의 것을 측정한다. 즉, NMOS의 드레인(25)를 에미터, 웰(22)를 베이스, 반도체 기판(21)를 콜렉터로 하는 기생 NPN트랜지스터의 전류 이득률 #946#N과 PMOS의 소오스(26)을 에미터, 반도체 기판(21)을 베이스, 웰(22)를 콜렉터로 하는 기생 PNP트랜지스터의 전류 이득률 #946#P와의 곱 #946#N#183##946#P를 측정하였다. 이 측정에서는 베이스와 콜렉터 사이에 5V의 전압을 인가하고, 10-6내지 10-2A의 범위의 에미터 전류의 함수로서 #946#N#183##946#P를 구하였다. 그 결과, PMOS 및 NMOS의 각 드레인 표면 불순물 농도가 3#215#1018㎝-3 찬넬 길이가 0.5㎛의 CMOSFET상기 각 드레인 표면 불순물 농도가 1#215#1018㎝-3 찬넬 길이가 0.3㎛의 CMOSFET 및 PMOS의 드레인 표면 불순물 농도가 3#215#1017㎝-3, NMOS의 상기 표면 불순물 농도가 1#215#1018㎝-3 찬넬 길이가 0.2㎛의 CMOSFET에 있어서의 각 #946#N#183##946#P의 곱의 최고 값은 모두 10-2 내지 10-4이었다. 상기의 값은 래치 업이 발생할 수 있는 조건 #946#N#183##946#P〉 1을 만족시킬수 있는 것은 아니며, 또 ,PMOS의 드레인을 쇼트키 접합으로, NMOS의 드레인을 통상의 높은 불순물 농도 N+P접합으로 구성한 CMOSFET에 있어서의 #946#N#183##946#P 곰의 값 10-2와 거의 같던가 그 이하의 값이다. 상기의 결과에서 PMOS의 드레인 확산층을 낮은 불순물 농도로 설정한 COMSFET에 있어서는 내 래치 업의 관점에서 오히려 소오스와 드레인 사이의 내압의 향상의 관점에 있어서 NMOS의 드레인 표면 불순물 농도의 최적조건을 바라는 찬넬 길이에 따라서 설정하면 좋은 것으로 된다.

Next, my latch up property is evaluated about CMOSFET manufactured by the manufacturing process of indicating in this embodiment the following is measur ed as my latch up property in other words, the drain (2 5) of NMOS is emitted and the current gain modulus βN of the parasitism NPN transistor doing the base, and th e semiconductor substrate (21) about the well (22) to the collector and source (26) of PMOS are emitted and the double βN·βP with the current gain modulus βP of t he parasitism PNP transistor doing the base, and the w ell (22) about the semiconductor substrate (21) to the collector was measured the voltage of 5V is applied in t his measurement between the base and collector The β N·βP was saved as the function of the emitter current of the range of 10 - 6 to 10 - 2 A 1× 10 18 ㎝ - 3 chan nel length of 3× 10 17 ㎝ - 3 , and the surface impurity concentration of NMOS of CMOSFET of 0.3㎛ and drain surface impurity concentration of PMOS of 1× 10 18 ㎝ - 3 channel length of the CMOSFET each drain surface impurity concentration of 0.5㎛ of 3× 10 18 ㎝ -3 chan nel length of each drain surface impurity concentration of NMOS and PMOS the highest value of the double of each βN·βP in CMOSFET of 0.2㎛ was altogether 10 - 2 to 10 - 4 it is not consequently the value described in the above satisfies the condition βN·βP>1 in which the latch up can be generated. And it is better that the dr ain of the ,PMOS is set up according to the channel len gth which is in COMSFET which is nearly the same as t hat of the value 10 - 2 of the βN·βP bear in CMOSFET organizing the drain of NMOS on the high impurity conc entration N+P junction to the Schottky barrier it is the value of less sets up the drain diffusion layer of PMOS as the low impurity concentration in the result describe d in the above and rather hopes the optimal condition of the drain surface impurity concentration of NMOS in the viewpoint of my latch up as to the viewpoint of the improvement of the internal pressure between the sour ce and the drain.

다음에 본 실시예에 의한 CMOSFET에 있어서 NMOS 및 PMOS의 각 드레인 표면 불순물 농도를 5#215#1018내지 1020㎝-3으로 설정한 찬넬 길이 0.2 내지 1.0㎛의 COMSFET도 동시에 제조하고, 그 소오스와 드레인 사이의 내압 및 내 래치 업 특성을 측정하였다. 상기 COMSFET의 소오스 드레인 사이의 내압은 종래의 값보다 최대 수 V로 개선되고, 또 #946#N#183##946#P곱도 1이하이었지만, 상술의 결과에 비하면 약간 뒤떨어지는 특성이었다.

Next, COMSFET of the channel length 0.2 through 1.0 ㎛ setting up each drain surface impurity concentration of PMOS and NMOS as 5× 10 18 to 10 20 ㎝ - 3 as to CMOSFET by this embodiment simultaneously manufact ured and the internal pressure between the source and the drain and my latch up property were measured. Th e internal pressure between source and drain of COMSF ET were improved with the maximum number V than th e conventional value and and, the βN·βP double was 1 or less. However it was the property of being a little bit inferior if the property compared to the result of the de tailed description.

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[실시예 8]

제18도 및 제19도는 본 발명의 제8의 실시예를 도시한 CMOSFET의 제조 공정의 단면 구조도이다.

제15도에 도시한 상술한 제7의 실시예에 있어서 실리콘 산화 퇴적막(213)를 게이트 전극(29)및 필드 산화막(23)의 측벽부에만 자기 정합적으로 남겨둔 후, 노출되어 있는 게이트 산화막을 완전히 제거한다. 다음에, 지클로루실탄(SiH2Cl)과 염산(HCL)의 화학기상반응을 775℃의 온도로 행하고, 0.3㎛의 두께의 다결정질 또는 비정질의 실리콘 박막(216)을 웰(222)표면 위 및 N도전형을 유지하고 있는 반도체 기판(21)표면 위에 선택적으로 퇴적시킨다(이상 제18도 참조). 상기 실리콘 퇴적막의 형성조건은, 지클로루실란200cc, 염산 60cc의 조건으로 퇴적속도는 10㎚/분이다. 이 조건에 있어서는 피퇴적 표면에 실리콘 질화막(SiN4)이 존재하지 않는 한 실리콘 기판 위에만 선택적으로 퇴적하고, 또 측벽 절연막(213)과의 경계부에 있어서도 소위 파셋(facet)이라 하는 오목 볼록이 없는 평탄한 현상을 얻을 수가 있다.

실리콘 박막(216)의 퇴적후, 웰 영역(222)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 포토 레지스트막을 선택적으로 형성하고, 붕소 이온 주입을 실시한다. 붕소 주입량은 상기 실리콘 박막(216)내의 불순물 농도가 웰 (222)표면의 불순물 농도와 일치하도록 설정한다. 주입 에너지는 25KeV이다. 그후, 이온 주입의 마스크에 사용한 포토 레지스트막을 제거하고 나서 1150℃, 15초의 조건으로 고온 단시간 열처리를 실시하고, 주입 이온의 활성화와 실리콘 박막(216)의 단결정화를 행한다. 사전에 다결정질, 또는 비정질로 형성된 실리콘 박막(216)내에 있어서 불순물의 확산 계수는 단결정 실리콘 내에 있어서의 확장 계수에 비해서 10 내지 20배나 크다. 따라서, 상기의 단시간 열처리에 의해 웰(222)위의 실리콘 박막(216)에 주입된 붕소는 실리콘 박막(216)내에서 깊이 방향에 대해 대략 균일하게 분포한다. 상기 열처리를 한 후, 상술의 제7의 실시예에 따라서 N도전형의 소오스(24) 및 드레인(25)와 P도전형의 소오스(26) 및 드레인(27)을 형성한다. 상기의 단시간 고온 열처리에 의해 실리콘 박막(216)은 이미 단결정화 되어 있다. 따라서, 상기의 각 소오스 및 드레인의 형성 조건은 상기 제7의 실시예의 경우와 같은 조건으로 실시된다. 그후의 공정도 상술한 제7의 실시예에 따라서 CMOSFET를 제조한다(이상 제19도 참조).

제19도에 표시한 제8실시에 따른 CMOSFET는 상술한 제7의

[Embodiment 8]

With Figure 18. And figure 19 is a sectional configuration of the manufacturing process of CMOSFET showing the embodiment of the eighth of the invention.

In a preferred embodiment, after the silicon oxidation heap film (213) is left in the sidewall part of the field oxide film (23) and gate electrode (29) of the above-described seventh shown in Figure 15 through the self-alignment manner the exposed gate oxidation film is completely removed. Next, the chemical vapor deposition of the hydrochloric acid (HCL) and paper chloro bullet (SiH(SB)2(/SB)Cl) is performed into the temperature of 775℃ and the polycrystalline of the thickness of 0.3㎛ or the amorphous silicon thin film (216) the selectively is sedimented on the semiconductor substrate (21) surface maintaining the well (222) surface the upper part and N conductivity type (over eighteenth is the reference). The formation condition of silicone heap film is the paper chloro silane 200cc, and the condition of the hydrochloric acid 60cc the deposition rate are 10㎚/. It is in this condition and as long as the silicon nitride film (SiN(SB)4(/SB)) is nonexistent in the blood deposition surface it selectively accumulates in on silicon substrate and the even phenomenon without the concave-convex that it is the so-called facet as to and, the border of the side wall insulating film (213) can be obtained.

The photoresist film is selectively formed so that the ion implantation is performed after the deposition of the silicon thin film (216) in the silicon thin film part above the well region (222) and the boron ion implantation is performed. The boron injection level sets up so that the impurity concentration within the silicon thin film (216) coincides with the impurity concentration of the well (222) surface. The implant energy is 25KeV. Thereafter, after the photoresist film used in the mask of the ion implantation is removed the rapid thermal annealing is performed to 1150℃, and the condition of 15 second and the activation of the implant ion and monocrystallization of the silicon thin film (216) are performed. In advance, it is in the silicon thin film (216) formed with the polycrystalline or the amorphous and the diffusion coefficient of the impurity is large in comparison with the coefficient of expansion in inside of the single-crystal silicon as 10 through 20 times. Therefore, the boron injected with the RTA described in the above in the silicon thin film (216) above the well (222) is distributed to uniform approximately in the silicon thin film (216) about the longitudinal direction. After it heat-treats at the above the source (26) of the source (24) of N conductivity type and drain (25) and P conductivity type and drain (27) are formed according to the seventh embodiment of the detailed description. The already the silicon thin film (216) is single crystallized with the RCA described in the above. Therefore, the formation condition of the drain and each source described in the above is performed to the condition like the case of the seventh embodiment. According to the seventh embodiment in which the process of the after describes in detail, CMOSFET is manufactured (over nineteenth is the reference).

CMOSFET according to the eighth operation indicated

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실시예에 따른 CMOSFET와 동일 치수를 갖고 있으며, 양자의 소오스와 드레인 사이의 내압을 비교하였을때, 찬넬 길이 0.3㎛, 소오스 및 드레인 표면 불순물 농도 1#215#1018㎝-3의 조건에 있어서의 제8실시예의 CMOSFET의 쪽이 약 1V만큼 높고, 7V의 내압이 얻어졌다. 또, 찬넬 길이 0.2㎛, NMOS 및 PMOS의 드레인 표면 불순물 농도가 각각 1#215#1018㎝-3 및 3#215#1017㎝-3의 조건으로 구성된 제8실시예의 CMOSFET의 내압을 측정하고, 상술한 제7실시예의 CMOSFET의 내압과 비교하였을때, 전자의 쪽이 약 2V높은 5V의 값을 얻었다. 상기의 값은 종래 구조에 따른 CMOSFET의 소오스, 드레인 사이의 내압과 비교해서 3배 이상의 고내압화를 실현한 것으로 된다. 제8의 실시예에 따르는 CMOS FET에 있어서 기생 바이폴라 트랜지스터에 관한 전류 이득률의 금 #946#N#183##946#P를 여러가지의 찬넬 길이, 소오스 및 드레인 표면 불순물 농도를 갖는 경우에 대해서 측정하였으나, 모두 상술의 제7실시예에 따른 CMOSFET의 측정값에 비해서 2/3 내지 1/2로 저감화 되어 있었다. 이와 같이, 제8실시예에 따른 CMOSFET는 제7실시예에 따른 CMOSFET보다 소오스와 드레인 사이의 내압 및 내 래치 업 특성에 있어서 향상하고 있지만, 그 이유는 소오스 및 드레인의 각 접합이 반도체 박막(216)내에 설치된 것에 의해 접합 면적이 저하하고, 또한 실효 찬넬 길이가 증가하였기 때문이라고 생각된다.

in Figure 19 had the same dimension as CMOSFET according to the above-described the seventh embodiment and when the internal pressure between the source of both sides and the drain was compared , the channel length 0.3㎛, and the side of CMOSFET of the eighth preferred embodiment in the condition of the source and drain surface impurity concentration 1× 10 18 ㎝ - 3 were high as about 1V and the internal pressure of 7V was obtained. And the internal pressure of CMOSFET of the eighth preferred embodiment consisting of channel length 0.2㎛, and the drain surface impurity concentration of NMOS and PMOS is the condition of 1× 10 18 ㎝ - 3 and 3× 10 17 ㎝ - 3 was measured and when it compared with the internal pressure of CMOSFET of the above-described the seventh preferred embodiment , the side of the electron about 2V obtained the value of 5V. It compares with the source of CMOSFET according to the conventional structure, and the internal pressure between the drain and the value described in the above realizes the high voltage-resistant more than the treble. In case of having the channel length of the various, and the source and drain surface impurity concentration the gold βN·βP of the current gain modulus about the parasitic bipolar transistor was confronted as to the CMOS FET followed the eighth embodiment and it measured. But the altogether became decreasing in comparison with the measured value of CMOSFET according to the seventh preferred embodiment of the detailed description to 2/3 through 1/2. In this way, CMOSFET according to the eighth preferred embodiment improves than CMOSFET according to the seventh preferred embodiment as to the internal pressure between the source and the drain and my latch up property. However the junction area is degraded by the result of that reason for the each junction of the drain and source is installed within the semiconductor film (216) and it is regarded that moreover, the effectiveness channel length was due to increase.

[실시예 9]

[Embodiment 9]

제20도 및 제21도는 본 발명의 제9의 실시예를 표시한 CMOSFET의 단면구조도와 N도전형의 드레인 확산영역에서의 깊이 방향에 관한 불순물 농도 분포도이다.

With Figure 20. And figure 21 is an impurity concentration distribution drawing about the longitudinal direction at the drain diffusion region of the sectional configuration of CMOSFET indicating the ninth embodiment and N conductivity type of the invention.

제18도에 도시한 제8실시예에 있어서 다결정질, 또는 비정질의 실리콘 박막(216)을 반도체 기판(221)위에 자기 정합적으로 퇴적시킨 후, 웰 영역(222)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 다른 영역 표면위에 포토 레지스트막을 남겨 놓는다. 그후, 웰 영역9222)위의 실리콘 박막 부분에 비소의 이온 주입을 행하고 나서 상기의 남겨진 포트 레지스트막을 제거한다.

After the polycrystalline or the amorphous silicon thin film (216) is sedimented with the self-alignment manner in Figure 18 as to the eighth preferred embodiment shown on the semiconductor substrate (221) the photoresist film is left on the dissimilar domain surface so that the ion implantation is performed in the silicon thin film part above the well region (222). Thereafter, the photoresist film remaining described in the above is removed after the ion implantation of arsenic is performed in the silicon thin film part above the well region 9222).

다음에, 웰 영역(222)를 포토 레지스트막으로 덮고, 웰 영역(222)이외의 N도전형을 갖는 반도체 기판(221)위의 실리콘 박막 부분에만 이온 주입이 행하여지도록 재차 포트 레지스트막을 남겨 놓는다. 그후, 붕소를 이온 주입하고, 재차 포토 레지스트막을 완전히 제거해서 실리콘 박막(216)의 표면을 노출시킨다. 이상태에서 1100℃, 30초의 조건의 단시간 고온 열처

Next, the well region (222) is covered up with the photoresist film and the photoresist film is left again so that the ion implantation is performed in the silicon thin film part above the semiconductor substrate (221) having N conductivity type except the well region (222). Thereafter, boron is ion-implanted and the photoresist fil

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리를 실시한다. 상기 조건의 열처리을 행하여도 실리콘박막(216)은 단결정화 되지 않고, 다경정질 또는 비정질의 상태를 유지하고 있다. 다결정질, 또는 비정질의 실리콘 박막(216)내에 있어서의 불순물의 확산 계수는 상술과 같이 매우 큰 값이기 때문에 상기 조건에 의한 단시간 열처리에 의해서 실리콘 박막(216)내에서 비소 및 붕소는 고속으로 거의 균일한 농도 분포로 된다. 그러나, 반도체 기판(21)내에 있어서의 각 불순물의 확산 계수는 상대적으로 작고, 상기 단시간의 열처리에 의해서는 반도체 기판(21)내에 약 20㎚정도밖에 확산되지 않았다.

m is again completely removed and the surface of the silicon thin film (216) is exposed. In this state, 1100℃, and RCA of the condition of 30 second are performed. The silicon thin film (216) is not single crystallized even if the thermal process of the condition is performed and the multi-stem chiseling or the amorphous state is maintained. Because it is the big value the diffusion coefficient of the impurity in the polycrystalline or the amorphous silicon thin film (216) in very consists of the concentration distribution in which arsenic and boron are nearly uniform at high speed like the detailed description with RTA by the condition in the silicon thin film (216). But relatively the diffusion coefficient of each impurity in the semiconductor substrate (21) in was small and it was according to due to the thermal process of the short time and it was not diffused within the semiconductor substrate (21) about 20㎚.

이와 같이 비소 및 붕소의 이온 주입과 그에 따르는 단시간 열처리에 의해 실리콘 박막(216)과 웰(222) 및 N도전형 반도체 기판(221)내에 각각 N도전형의 소오스(24)와 드레인(25) 및 P도전형의 소오스(26)과 드레인(27)을 형성한다. 그후, 상기 각 소오스(24) 및 (26)과 드레인(25) 및 (27)위에 백금 실리사이드(PiSi)층(214)를 상술의 제7의 실시예에 따라서 자기 정합적으로 형성하고, 그후의 공정도 제7의 실시예에 따라서 실시하는 것에 의해 제20도에 도시한 CMOSFET를 제조할 수가 있다.

In this way, the source (26) of the source (24) of N conductivity type and drain (25) and P conductivity type and drain (27) are formed with the ion implantation of arsenic and boron and RTA followed that within the silicon thin film (216), the well (222) and N conductive semiconductor board (221). Thereafter, according to the seventh embodiment of the detailed description the platinum-silicide (PiSi) layer (214) on each source (24) and (26) and drain (25) and (27), it forms into the self-alignment manner and by the result of that the process of the after performs by the seventh embodiment CMOSFET shown can be manufactured at a rate per Figure 20.

제9실시예에 의한 CMOSFET의 N도전형 소오스(24) 및 드레인(25)의 불순물 농도 분포는 제21도에 도시한 바와 같이 3개의 영역 A, B, C로 분리된다. 즉, 실리사이드층(214)바로 아래에 있어서의 약 10㎚두께의 불순물 석출 영역A, 실리콘 박막(216) 내부의 균일 분포 영역 B 및 웰9222)내에 있어서의 접합 깊이 약 20㎚를 갖는 급격한 농도 분포 영역 C이다. P도전형 소오스(26) 및 드레인(27)내에 있어서는 상기 불순물 석출 영역 A의 존재는 인정되지 않았다.

It as shown in the impurity concentration distribution of N conductivity type source (24) of CMOSFET by the ninth preferred embodiment and drain (25) is Figure 21 is separated into the domain A of 3, B, and C. That is, the sudden concentration distribution domain C having the impurity precipitation domain A of about 10㎚ thickness in the lower part, and the junction depth about 20 ㎚ in the uniform distribution domain B of the silicon thin film (216) inside and well 9222) in the silicide layer (214). It was in P conductivity type source (26) and drain (27) and the presence of the impurity precipitation domain A was not recognized.

제9실시예에 따른 CMOSFET에 있어서는 상기 실리콘 박막(216)내의 균일 분포 농도로서, NMOS에 관해서는 1#215#1018㎝-3, 3#215#1018㎝-3, 1019㎝-3, 5#215#1019㎝-3의 각 값이, 또 PMOS에 관해서는 1#215#1017㎝-3, 3#215#1017㎝-3, 1#215#1018㎝-3, 3#215#1018㎝-3 및 5#215#1018㎝-3의 값이 최종적으로 되도록 비소 또는 붕소 이온 주입량을 설정하는 것에 의해서 MOSFET를 제조하였다. 또, 찬넬 길이에 관해서도, 0.1, 0.2, 0.3, 0.5 및 1.0㎛의 값일때에 대해서 MOSFET를 제조하였다. 상기 각종의 CMOSFET에 대해서 소오스와 드레인 사이의 내압 및 기생 바이폴라 트랜지스터의 각 전류 이득률의 곱 #946#N#183##946#P를 측정하였다. NMOS의 드레인(27)내의 균일 분포 불순물 농도가 1018㎝-3이상 일 때, 상기 특성 향상은 그다지 확인되지 않았다. 그러나, 상기 균인 분포 불순물 농도가 1017 내지 1019㎝-3의 낮은 불순물 농도로 설정되어 있을 때에는 특히 소오스와 드레인 사이의 내압의 향상이 현저하였다. 드레인 내의 균일 분포 불순물 농도가 1#215#1018㎝-3일 때 찬넬 길이가 0.1 및 0.2㎛의 각 CMOSFET에 있어서의 소오스와 드레인 사이의 내압은 각각 4.5 및 8 V에 달하였다. 이들이 값은 제8의 실시

It was in CMOSFET according to the ninth preferred embodiment and it was the uniform distribution concentration within the silicon thin film (216) and MOSFET was manufactured finally by the result of that the value of 5× 10 18 ㎝ - 3 and 1× 10 17 ㎝ - 3 , 3× 10 17 ㎝ - 3 , 1× 10 18 ㎝ - 3 , 3× 10 18 ㎝ - 3 of each value of 1 × 10 18 ㎝ - 3 , 3× 10 18 ㎝ - 3 , 10 19 ㎝ - 3 , 5× 10 19 ㎝ - 3 set up arsenic or the boron ion dosage about NMOS about and, PMOS as as possible. And MOSFET was manufactured about the value task time of 1.0㎛ and drawing about the channel length, 0.1, 0.2, 0.3, 0.5. The double βN·βP of each current gain modulus of the internal pressure between the source and the drain and parasitic bipolar transistor were measured about the various CMOSFET. The uniform distribution impurity concentration within the drain (27) of NMOS the characteristic improvement was not particularly confirmed over 10 18 ㎝ - 3 in the task. But when the distribution impurity concentration which was the bacteria was set up as the low impurity concentration of 10 17 to 10 19 ㎝ - 3 ,

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예에 따른 CMOSFET일 때에 비해서도 많이 개선되어 있으나, 이 효과는 찬넬 길이가 짧은 경우의 쪽이 상대적으로 현저하였다. PMOS에 있어서의 드레인(25) 내의 균일 분포 불순물 농도가 1017 내지 1018㎝-3미만으로 설정되고, 또한 게이트 길이가 0.1㎛일때에도 소오스와 드레인 사이의 내압은 제8의 실시예 일 때와 비교해서 수 V 향상되고 있으며, 그 값은 5V 이상에 달하였다.

especially, the improvement of the internal pressure between the source and the drain was remarkable. The channel length the internal pressure between the source in each CMOSFET of 0.1 and 0.2㎛ and drain reached 4.5 and 8 V when the uniform distribution impurity concentration within the drain was 1× 10 18 ㎝ - 3 . Even though the value compared when being CMOSFET according to the eighth embodiment these were improved. But relatively the side of the case where this effect the channel length was short was significant. The uniform distribution impurity concentration within the drain (25) in PMOS was set up as 10 17 to 10 18 ㎝ - 3 under and even when moreover, the gate length was 0.1㎛ it compared with the eighth embodiment task time and the internal pressure between the drain and the source were improved with the number V and the number of the value reached 5V or greater.

제9의 실시예와 제8의 실시예에 있어서의 이 효과의 차이는 드레인 최대 전계가 인가되는 낮은 불순물 농도 영역이 제9실시예일 때에는 실리콘 박막(216)내에서 제21에 도시한 바와 같이 대략 균일하게 형성되기 때문이고, 그에 의한 전계분산 효과가 된다고 생각된다.

As shown in the twenty first within the silicon thin film (216) the low concentration domain of impurities in which the drain maximum electric field the difference of this effect in the ninth embodiment and the eighth embodiment is applied is the ninth preferred embodiment, it is due to be formed to uniform approximately and it is regarded to become with electric field dispersion effect thereby.

또, 제9실시예에 따른 초미세 CMOSFET의 기생 바이폴라 트랜지스터의 곱 #946#N#183##946#P에 관해서는 제8실시예의 경우와 거의 변함이 없고, 래치 업 현상은 무시할 수 있는 정도이었다.

And the case there was no to nearly change about the double βN·βP of the parasitic bipolar transistor of the ultra-fine CMOSFET according to the ninth preferred embodiment with the case of the eighth preferred embodiment and it was the extent which the latch-up could ignore.

본 발명의 제1내지 제6의 실시예에 의하면, 최대 전계인가 영역이 드레인 확산층내에서 넓게 분산할 수 있으므로, 동일 구조 파라미터를 갖는 종래 구조의 트랜지스터 보다 5V이상이나 소오스와 드레인 사이의 내압을 향상할 수 있다. 따라서, 본 발명에 의하면 전원 정압을 종래의 5V에서 3V이하로 내리는 것과 같은 변경도 없이 실효 찬넬 길이가 0.5㎛이하의 미세 트랜지스터를 동작시킬수가 있다.

According to the first through the sixth embodiment of the present invention., it wides the maximum electric field approved area can be scattered in the drain diffusion layer. Therefore the internal pressure between the drain and the source can be improved than the transistor having the identical structure parameter of the conventional structure over 5V. Therefore, the effectiveness channel length can operate the minute transistor less than 0.5㎛ without the varying degree which according to the invention seems to drop the power source hydrostatic from the conventional 5V less than 3V.

본 발명의 제1 내지 제3의 실시예에 있어서는 PtSi층의 형성시에 있어서의 PtSi층 바로 밑의 불순물의 석출 효과를 이용해서 음 접촉에 필요한 불순물 농도 영역을 PtSi층과 자기 정합의 관계로 구성하였으나, 상기의 PtSi층은 Mo, W, Pb, Ni, Ti, Ta, Nb, Cr, Pr등의 다른 고융점 금속 또는 그들의 실리사이드 막으로 치환해서 구성하여도 지장이 없다. 또, 본 발명의 각 실시예에 있어서는 소오스 및 드레인 확산층을 P이온에 의해 형성한 이를 도시하였으나, 상기 확산층은 P이온에 의해서 형성하여도 좋다. 또, 그 형성 방법도 이온 주입에 한정되는 일없이 열 확산법 등 다른 공지의 수단에 의해서도 본 발명의 요지를 이탈하지 않는다. 또, 본 발명은 상기와 같은 단일체 트랜지스터에 한정되는 일이 없이 반도체 집적회로 장치에 대해서도 적용된다.

The concentration domain of impurities required for the negative principle in nature contact was gotten the relation of the self alignment and PtSi layer comprise by being in the first of the invention to the third embodiment and using the precipitation effect of the PtSi layer impurity immediately below in the formation time of the PtSi layer. But even if the ptSi layer described in the above substitutes with the high melting point metal or dissimilar their silicide films of the mo, W, pb, ni, ti, ta, nb, cr, the Pr etc and it configures there is no impediment. And it may be acceptable that this which was in each embodiment of the invention and formed the source and drain diffusion layer with P ion was shown. But the diffusion layer forms with P ion. And the gist of the invention is not broken away from without the task in which the formation method is restricted to the ion implantation with the different publicly known means. And it is applied to without the task in which the invention is restricted to the above-mentioned monolith transistor semico

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nductor integrated circuit device.

또, 제7 내지 제9도의 실시예에 의한 효과는 종래 구조에 있어서의 소오스와 드레인에 대응하는 영역을 개선하는 것에 의해 얻어지는 것으로, 결코 반도체 기판(221)의 농도를 증대시켜서 고냉압화를 도모하는 것은 아니다. 따라서, 반도체 기판 농도의 증대에 따르는 이동도의 저하를 조래하는 일도 없고 고속 동작을 손상하는 일도 없다.

And by improving the domain in which the effect by the embodiment of the seventh through Figure 9 correspon ds to the source in the conventional structure and drai n the domain is obtained. The concentration of the se miconductor substrate (221) is ever increased and the high cold press is not planned. Therefore, *** the task does the degradation of the mobility following the incre ase in semiconductor substrate concentration not have and there is no task injuring the high speed operation.

본 발명의 제7 내기 제9의 실시예에 의하면, 소오스 및 드레인 위에 고융점 금속 또는 그 실리사이드층이 형성되어있기 때문에 초미세 CMOSFET에 있어서도 그 시이트 저항는 수Ω/㎠으로 낮은 저항성을 유지할 수 있어 고속 동작을 보장할 수가 있다.

According to the embodiment of the seventh betting ninth of the present invention., because the high melti ng point metal or the silicide layer is formed on the sou rce and drain the low resistivity can be maintained with the number Ω / ㎠ which the sheet resistance is increa sed as to the ultra-fine CMOSFET and the high speed o peration can be guaranteed.

제7~제9의 각 실시예에 있어서는 소오스 및 드레인 확산층의 최대 불순물 농도에 관하여 1#215#1017㎝-3이상일 때에 대해서 기술하였으나, 이것은 제13도의 해석 결과 즉, 0.1㎛의 게이트 길이에 대하여서의 해석 결과에 따르고 있다. 0.1㎛의 값은 실현할 수 있는 최소의 게이트 길이이다. 또, 상기의 불순물 농도(1#215#1017㎝-3)이하에서 본 발명을 적용할 때에 제14도에서 추측할 수 있는 바와 같이 기판 전류의 증대 및 드레인 누설 전류의 증대를 초래하게 되는 것이다.

It was in each embodiment of the 7~ ninth and when being 1× 10 17 ㎝ - 3 or greater, it confronted and it d escribed about the maximum impurity concentration of the drain diffusion layer and source. But this follows th e interpretation result of Figure 13, in other words, the gate length of 0.1㎛ into the interpretation result at ** *. It is the minimum gate length which the value of 0.1 ㎛ can realize. And in the impurity concentration (1×10 (SP)17(/SP)㎝(SP)-3(/SP)) or less described in the abo ve, the increase in the substrate current it can guess and increase in drain leak electric current are caused in Figure 14 when applying the invention.

또, 제7~제9의 각 실시예에 있어서는 소오스 및 드레인 확산층 위에 백금 실리사이드(PtSi)층을 자기 정합적으로 형성하였으나, 이것은 일예로서 이 PtSi층 대신에 Mo, W, Pb, N, Ti, Ta, Nb, Cr, Pr등의 고융점 금속 또는 그 실리사이드 막을 사용할 수가 있다. 또, 각 실시예에 있어서는 단시간 열처리로서 고온 전기로를 사용하는 방법에 대해서 설명하였으나, 이 공정은 램프가열법, 레이저 또는 전자선 조사법등의 다른 방법에 의해서도 가능하다. 또, 각 실시예에 있어서는 P도전형 웰을 사용한 경우에 대해서 설명하였으나, 역으로 P도전형 반도체 기판내에 N도전형의 웰을 형성한 구조의 CMOSFET에 대해서도 본 발명을 적용할 수가 있다.

And it was in each embodiment of the 7~ ninth and the platinum-silicide (PtSi) layer was formed into the self-al ignment manner on the source and drain diffusion layer. But as an example, this instead of can use the high mel ting point metal or the silicide film of the mo, W, pb, N, ti, ta, nb, cr, the Pr etc with this PtSi layer. And it expl ained the method for being in each embodiment and usi ng the high temperature electric furnace as RTA. But t his process is possible with the dissimilar method includi ng the lamp heating method, the laser or the electronic beam irradiation method etc. And in case of being in ea ch embodiment and using P conductive well it confront ed and it illustrated. But the invention can be applied t o CMOSFET which reversely forms the well of N conduc tivity type within P conductive semiconductor board of the structure.

이상 설명한 바와 같이 본 발명에 의하면, 0.2㎛의 극히 짧은 찬넬 길이라도 5V의 통상 전원으로 동작 시킬수가 있고, 또 래치 업 현상을 방지할 수 있기 때문에 고속 동작을 손상시키는 일없이 초미세 CMOSFET를 실현하는 것이 가능하다.

As described above, although it is the channel length which is exceedingly short of 0.2㎛ the generally can a ctivate from the according to the invention to the pow er source of 5V and the injures the high speed operatio n because it can prevent and, the latch-up task is pos sible to realize the ultra-fine CMOSFET without the tas k which.

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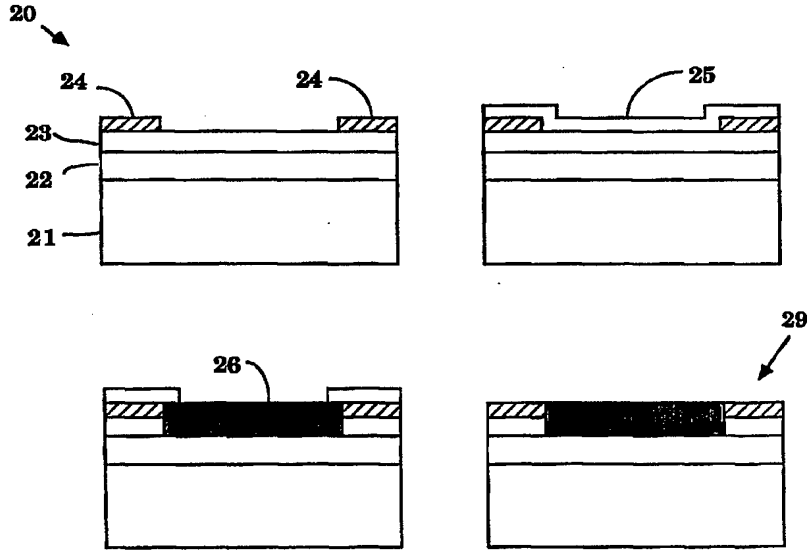
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(57) Abstract

Stable, high temperature electrical contacts (29) to silicon carbide formed using a unique silicide formation process that employs a sacrificial silicon layer (23) between the silicon carbide (21) and the contacting metal (25) which forms a metal silicide interlayer (26) providing the resulting contact with low specific contact resistance and high electrical and structural stability. The contact interface is formed by reaction below the semiconductor surface, and thus the in situ silicide formation process is insensitive to surface impurities and oxides and permits the controlled formation of silicides without the formation of excess carbon and carbides at the contact interface. The silicon layer (23) may optionally be doped in situ during growth or implanted with dopants after growth, to lower the contact resistance and enhance its operational stability.

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"LOW RESISTANCE, STABLE OHMIC CONTACTS TO SILCON CARBIDE, AND METHOD OF MAKING THE SAME"

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to electrical contact structures formed between silicon carbide and silicide-forming metals, having low specific resistances and ohmic behavior and long-term electrical and structural stability, and methods for making the same.

Description of the Related Art

An extensive technology of semiconductor devices has been developed based upon the properties of single crystal silicon and other similar materials which may be doped, heat treated, and otherwise processed to produce adjacent layers and regions of varying electronic characteristics. The use of devices produced by silicon technology is generally limited to operation at ambient or, at most, moderately elevated temperatures and in non-corrosive, inert atmospheres. The temperature limitation is a consequence of the small band gap of silicon (1.1. eV), which leads to large leakage currents and device failure at elevated temperatures. In addition, rapid diffusion of dopants and/or impurity species can occur in silicon, which in turn can substantially alter the character of the fabricated semiconductor device. The limitation to relatively inert environments results from the high chemical reactivity of silicon in many corrosive environments, which also can alter the character of the fabricated device. Silicon devices are also limited as to power level, frequency, and radiation tolerance by the materials used therein.

For some applications, the temperature, environmental, and other use limitations on silicon microelectronic devices may be overcome by the use of

proper cooling and packaging techniques. In other applications, these limitations have prevented the use of silicon for integrated circuit technology. For example, in many spacecraft and aircraft applications, elevated temperatures are encountered, and it is not always possible to insure that adequate cooling will be provided. In high power applications, device temperatures can rise to levels which degrade or destroy the device solely through internal heating. Silicon's inability to withstand high temperatures limits the amount of power which can be generated or controlled by silicon electronics. In addition, internal thermal transients in devices otherwise operating at ambient temperature can rapidly destroy the operability of the device unless extensive cooling is provided. Such cooling requires that the device be larger in size than might otherwise be necessary, in part defeating the purpose of the integrated circuit technology.

There has therefore been an ongoing, but as yet not fully successful, search over a period of twenty years to identify and develop a semiconductor technology based in other materials. Such a technology would desirably allow the fabrication of devices for use at higher temperatures such as, for example, the range of at least about 400°C to 600°C, and in applications not amenable to the use of silicon. Because corrosive effects can be greatly accelerated at elevated temperatures and pressures, any such materials and devices must also exhibit excellent corrosion resistance at the elevated use temperatures and over a range of pressures from vacuum to many atmospheres. Some generally desirable characteristics of such materials have been identified, including large band gap, good electrical conductivity, high electric field breakdown strength, low dielectric constant, ability to be doped to produce regions of varying electronic characteristics, a high melting temperature, good strength at operating temperatures, resistance to diffusion by undesired foreign atoms, good thermal conductivity, thermal stability, chemical inertness, and the ability to form stable ohmic and rectifying external contacts.

Silicon carbide has been identified as a candidate material meeting the indicated requirements. Silicon carbide has a high decomposition temperature, good strength, good resistance to radiation damage, and good corrosion resistance in many environments. Silicon carbide has a high breakdown field strength, ten times that of silicon, a relatively large band gap, low dielectric constant, and a thermal conductivity of more than three times that of silicon at ambient

temperature. The diffusion coefficients in silicon carbide are also much smaller than those in silicon or gallium arsenide, and so silicon carbide is resistant to the diffusion of impurity species. Silicon carbide may be processed by several techniques similar to those used in silicon device technology, and in many instances silicon carbide devices may be substituted at moderate and low temperatures for silicon devices. Silicon carbide semiconductor device technology therefore offers the opportunity for supplementing, and in some instances replacing, conventional silicon device technology.

Silicon carbide crystallizes in a cubic polytype as well as numerous hexagonal and rhombohedral polytypes. The 6H-SiC hexagonal polytype is currently the most developed for electronic device applications, but other polytypes, especially the hexagonal 4H-SiC and the cubic 3C-SiC, have also attracted attention for use in high power, high temperature devices. Properties of the 6H polytype are compared with those of silicon and gallium arsenide below. Combined, these advantages in physical and electrical properties predict high maximum acceptable junction temperatures and will allow extremely high power and high temperature operation.

Property	Si	GaAs	6H-SiC
E_g (eV) 300K	1.11	1.43	2.93
Electron mobility (R.T. $cm^2/V\text{-}s$)	1400	8500	400
Hole mobility (R.T. $cm^2/V\text{-}s$)	600	400	40
Breakdown V (E_b, 10^6 V/cm)	0.3	0.4	4.0
Thermal conductivity (W/cm-°C)	1.5	0.5	5.0
Saturated electron drift velocity (10^7 cm/s)	1.0	2.0	2.0
Dielectric constant	11.8	12.8	10.0
Maximum junction temp (°C)	≈200	≈300	≈1000

Silicon carbide in single crystalline form may be prepared by sublimation growth. Silicon carbide epitaxial layers may be formed or deposited by many techniques, including reactive evaporation and chemical vapor deposition (CVD). CVD is a particularly desirable fabrication approach, as it permits the controlled growth of undoped and doped layers and structures of a variety of forms. The layers may be doped in situ by inclusion of dopant species in the source gases of the CVD process, or after growth by implantation. Thus many of the processes for silicon carbide device fabrication are well-known.

Ohmic contacts, important elements of any device, are critical to the performance and stability of high power and high temperature devices. Wide band gap materials, including silicon carbide (SiC), diamond, and the III-V nitrides, currently suffer from a dearth of suitable contact strategies. Contact strategies to date have been fairly conventional, involving implantation, metallization, and deposition of simple silicides directly onto the silicon carbide surface. Although silicon carbide devices have been operated at temperatures as high as 650°C (J.W. Palmour, H.S. Kong and R.F. Davis, Appl. Phys. Lett. **51** (2028 (1987), the contacts have not demonstrated contact resistances comparably low to those achieved in gallium arsenide or silicon, or long term stability.

In addition to the semiconductor material, the entire microelectronic device and package (including metallization) must be suitable for high temperature operation. Stability of the contact is extremely important. Typical projected junction operating temperatures for these devices are as high as 1000°C. High temperature operation exacerbates diffusion; contacts must be designed to remain stable, both structurally and electrically, over the expected life of the device.

In addition to being stable, the contact resistance must be very low. While low contact resistances are desirable in all devices, they are a necessity in high power devices. A high contact resistance will increase the forward voltage drop and thus severely decrease device efficiency. Specific examples of high temperature devices that would desirably be fabricated in silicon carbide include power MOSFETs, thyristors, rectifiers and high frequency devices such as IMPATTs. Today, typical specific contact resistances to SiC are in the range of mid 10^{-5} to 10^{-4} Ω-cm^2. Tomorrow, specific contact resistances need to be in the 10^{-6} Ω-cm^2 range, similar to those attained in GaAs-based materials. Without low resistance contacts, the GaAs devices would not work; an analogous fate will befall SiC devices if low specific contact resistance strategies are not deployed.

A number of metals have been investigated for ohmic contacts to SiC. Typical ohmic contacts to SiC are nickel for n-type contacts and aluminum for p-type contacts. Waldrop and Grant (Appl. Phys. Lett. **56** (1990) 557) have examined additional metals in the as-deposited state; Pd, Au, Co, Ti, Ag and Tb. From the I-V characteristics, Pd, Au and Co are rectifying whereas Ti, Ag, Tb and Al are

"ohmic-like" (essentially linear I-V curve in forward and reverse bias). However, as-deposited metals are not suitable for high temperature contacts – they must be annealed at a temperature higher than their intended operating temperature. During annealing, these metals chemically react with the SiC to produce metal carbides and/or metal silicides, which are stable at the device operating temperatures.

Direct silicide formation on SiC is complicated by the fact that SiC, in addition to silicon, also contains carbon. After annealing, complicated metallurgy at the interface results. For example, annealing Ti on SiC at temperatures between 570-800°C resulted in diffusion of C and Si into the titanium and the formation of TiC and excess silicon (M.B. Chamberlain, Thin Solid Films **72** (1980) 305). No titanium silicides were observed. While TiC is a potential contact, the silicide would be preferred because of its lower sheet resistance. In addition, carbide formation continued for at least 20 hrs at 606°C; clearly not acceptable metallurgy for a stable high temperature contact. Other examples include Mo and Pt on SiC. In the case of Mo, a $Mo_2C/Mo_5Si_3/SiC$ multilayer was observed after annealing (S. Hara et al., Jap. J. Appl. Phys. **29** (1990) L394). Annealing Pt on SiC resulted in a periodic structure consisting of alternating layers of platinum silicides and carbon (T.C. Chou, J. Mater. Res., **5** (1990) 601).

We have demonstrated Ti-based contacts to SiC with specific contact resistances as low as 10^{-4} Ω-cm^2, as well as co-evaporated TiSi contacts which showed resistances as low as ~5 x 10^{-3} Ω-cm^2. These results indicate that co-evaporation is not ideal for deposition of TiSi to produce low resistance contacts. From Chamberlain's results discussed above, it is likely that the actual contact in the Ti case was TiC. More recent results indicate that Ti_5Si_3, as well as TiC, form at the interface between silicon carbide and titanium (L.B. Rowland et al., ONR Workshop on SiC Materials and Devices, September 10-11, 1992, Charlottesville, VA pp. 8). This work used epitaxially deposited Ti, followed by 700°C annealing in vacuum.

Tungsten and tungsten-gold alloys, after annealing at temperatures between 800-1600°C, had contact resistances between 7 x 10^{-4} and 7 x 10^{-5} Ω-cm^2, depending on the SiC carrier concentration (M. Anikin et al., Ioffe Physico-Technical Institute, Academy of Sciences of the USSR, Leningrad). Sputtered and alloyed $TaSi_2$ has been used in devices operating up to 650°C, although no contact

resistances or stability data have been reported (J.W. Palmour, H.S. Kong and R.F. Davis, J. Appl. Phys. 64 (1988) 2168). Nickel has also been used in high temperature devices, but again no data specific to the contacts has been reported (R.F. Davis et al., Proc. IEEE. **79** (1991) 677). It is likely that in this case Ni_2Si was formed, as was reported when nickel was annealed at 600°C on SiC (I. Ohdomari, et al., J. Appl. Phys. **62** (1987) 3747). No carbides were detected, but carbon was distributed uniformly throughout the reacted film. Investigations of platinum silicide indicate that it forms a Schottky contact to SiC (N.A. Papanicolaou et al., J. Appl. Phys. **65** (1989) 3526).

Therefore there is a need for a technology capable of forming stable, low specific resistance contacts to silicon carbide in all of its useful polytypes. Key to making such stable contacts is to understand and control the metallurgy and band structure at the contact interface. In an ohmic contact, the current flow is proportional to the applied voltage, both in sign and magnitude. For a low resistance contact, large currents should be supported without a significant voltage drop across the contact region. Tunneling processes exhibit linearity over a larger range than thermionic or thermionic field emission and thus it is desired that current conduction be dominated by tunneling in a low resistance contact. A large conductance (or small specific contact resistance) is achieved with a heavily doped semiconductor and a small potential energy barrier height. Heavy doping decreases the barrier width, resulting in increased current flow and a lower potential drop across the contact. The depletion region under the contact for heavily doped material is very small, on the order of 100Å for a carrier concentration of 10^{19} cm^{-3}. This means that the heavily doped contact region can be extremely thin. A small barrier height at the contact interfaces facilitates current flow with little resistive loss. The barrier height in the ideal case is determined by the work function of the metal and the electron affinity of the semiconductor. However, because of interface states, the actual barrier height often does not agree with this value.

J.M. Andrews and J.C. Phillips (Phys. Rev. Lett. **35** (1975) 56) correlated the barrier height of a number of silicide-silicon interfaces with the heats of formation of the silicides. Their work clearly showed that those metals which are more reactive with silicon, i.e. form silicides with higher heats of formation, made better ohmic contacts (lower barrier heights). From these results, silicides

of Ni, Co, W, Ta, Ti, Cr, Mo and Zr have been identified as good candidate metals for formation of ohmic contacts to SiC.

One problem observed with all of these contacts is that many phases of metal silicides and carbides are possible. This is because both silicon and carbon are present in SiC. The case is much simpler for contacts to an elemental semiconductor such as silicon or germanium since only one element is available for reaction with the metal.

Accordingly, it is an object of the present invention to provide stable, low resistance ohmic contacts to silicon carbide for use in high temperature, high power devices by controlling the metallurgy of the contact interface through the use of a sacrificial interlayer structure. This interlayer presents only one element to the metal, which greatly simplifies the contact metallurgy. A further object of the invention is to provide methods for fabricating these contact structures.

Other objects and advantages of the present invention will be more fully apparent from the ensuing disclosure and appended claims.

SUMMARY

In one aspect, the present invention relates to stable, high temperature electrical contacts to silicon carbide formed using a unique silicide formation process that employs a sacrificial silicon layer between the silicon carbide and an appropriate contacting metal. The silicon layer reacts with the contacting metal to form a metal silicide interlayer providing the resulting contact with low specific contact resistance and high electrical and structural stability. This "sacrificial" silicon layer permits the controlled formation of silicides without the formation of excess carbon and carbides at the contact interface. These "non-carbonaceous" metal silicide contacts contain less than 5% and preferably less than 1% of carbonaceous species, including free elemental carbon, carbides, or other carbon-containing compounds. Elimination of extraneous species which can diffuse and degrade the contact enhances the long term stability of the contact. The contact interface is formed by reaction below the semiconductor surface, and thus the in-situ silicide formation process is insensitive to surface impurities and oxides.

In another aspect, the invention pertains to stable, high temperature electrical contacts to silicon carbide formed using a silicide formation process that employs a heavily doped sacrificial silicon layer between the silicon carbide and the contacting metal. The doped silicide interlayer provides a diffusion source to heavily dope the semiconductor-silicide interface to further lower contact resistance.

In yet another aspect, the invention pertains to a method of forming stable, high temperature electrical contacts to silicon carbide, wherein a sacrificial layer of silicon is deposited on the silicon carbide surface followed by an overlayer of the contacting metal. Upon annealing at temperatures of 800-1100°C, stable low resistance ohmic contacts are formed. The silicon layer may optionally be doped in situ during growth or doped after growth by implantation, in-diffusion of a deposited layer of dopant species, or other suitable means.

In yet another aspect, the present invention pertains to a method for fabricating self-aligned stable, high temperature electrical contacts to silicon carbide, wherein a sacrificial layer of silicon is deposited on the silicon carbide surface, and a dielectric film (i.e. SiO_2) is deposited and patterned followed by

deposition of an appropriate contact metal. Upon annealing, a silicide forms only where the contact metal touches the silicon layer. The remaining metal on the SiO_2 pattern is then etched off, leaving intact the self-aligned silicide contact, which is much more resistant to the etchant. The silicon layer may optionally be doped in situ during growth or doped after growth.

Other aspects and features of the invention will be more fully apparent from the ensuing disclosure and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a schematic of the process for fabricating contacts to SiC, wherein a thin silicon layer in grown or deposited on top of the SiC (A), followed by metal deposition (B), and annealing to form the metal silicide (C). Optionally, if the silicon layer is heavily doped, a heavily doped interface region results (D).

Figure 2 shows a schematic wherein the process of the present invention can be used to make self-aligned contacts as well by first depositing and patterning a dielectric film (i.e. SiO_2) prior to metal deposition; upon annealing, a silicide forms only where the metal touches the silicon and the remaining metal on the SiO_2 pattern is then etched off, leaving intact the self-aligned silicide contact, which is much more resistant to the etchant. The remaining silicon layer may be removed if desired.

Figure 3 shows a number of I-V scans for 250 μm diameter nickel contacts to n-doped 6H-SiC annealed for 60 minutes at 900°C, of the same size contacts on different parts of the wafer, with Figure 3A showing scans of 15 contact structures fabricated with a 500Å sacrificial silicon interlayer structure and 3B showing scans of 12 contact structures for a sample fabricated with no silicon interlayer.

Figure 4 shows a number of I-V scans for palladium contacts to n-doped 6H-SiC, with 4A showing scans of five contact structures on different parts of the SiC wafer fabricated employing a 300Å Pd layer over a 600Å silicon interlayer, 40 μm diameter contact annealed at 1050°C for 30 minutes, and 4B showing scans of

eight contact structures fabricated employing a 500Å Pd layer over a 380Å silicon interlayer, 100 μm diameter contact annealed at 1100°C.

DETAILED DESCRIPTION OF THE INVENTION, AND PREFERRED EMBODIMENTS THEREOF

The present invention relates to stable, high temperature electrical contacts to silicon carbide formed using a unique silicide formation process that employs a sacrificial silicon layer between the silicon carbide semiconductor substrate and the contacting metal, wherein the silicon layer reacts with the contacting metal to form a metal silicide. The sacrificial silicon layer may optionally be heavily doped, in order to provide a diffusion source which will, during annealing, diffuse dopant into the immediate contact region and so provide a lower potential energy barrier between the semiconductor and the metal silicide contact. The silicide contact ensures operational stability at high temperatures. In the practice of the present invention, "heavily doped" refers to material that is doped to levels of $\geq 10^{18}$ carriers/cm^3, and preferably to levels $\geq 10^{19}$ carriers/cm^3.

The contact interface is formed by reaction below the semiconductor surface, and thus the process of reaction of the silicon layer with the contact metal to form metal silicide is relatively insensitive to surface impurities and oxides and permits the controlled formation of silicides without the formation of excess carbon and carbides at the contact interface. Elimination of extraneous species which can diffuse and degrade the contact enhances the long term structural and electrical stability of the contact. Because a metal or a metal silicide is not directly deposited upon the silicon carbide, carbides do not form upon annealing. The resulting "non-carbonaceous" metal silicide contacts contain less than 5% and preferably less than 1% of carbonaceous species, including free elemental carbon, carbides, or other carbon-containing compounds.

In addition to forming low resistance contacts, metal silicides useful in the practice of the invention should themselves have low resistivity to reduce parasitic resistances from the interconnects. The resistivities of thin films of various silicides and carbides are listed below:

Silicide	Resistivity ($\mu\Omega$-cm)	Thickness (nm)
PtSi	51	44
Pd_2Si	30	64
WSi_2	70	Thin film
$TaSi_2$	50-55	Thin film
TiC	50	Bulk
NiSi	14	36
$TiSi_2$	17	25
$CoSi_2$	16	29

In many ways, silicides are the ideal contact compounds. They are extremely stable at high temperatures and have low resistances, and, based on the results obtained with silicon semiconductors, have the potential to form contacts with low specific contact resistances. Silicides can be formed between silicon and almost half of the elements in the Periodic Table. Transition metal silicides are of the most interest because of their low resistivities. In addition to low resistivity, the metal silicide should preferably have a high melting point to provide the electrical contact with structural stability at high temperature. A low potential energy barrier between the metal silicide and the silicon carbide substrate is important, and so metal silicides that are known to make ohmic contact with silicon or silicon carbide are good candidate materials for the contacts of the present invention.

Suitable contacting metals for the present invention must form a stable, low resistivity silicide compound as described above. Such metals include the Group 4b, 5b, 6b, 7b, and 8 transition metals of the Periodic Table (CRC Handbook of Chemistry and Physics, 62nd Ed., 1981, CRC Press, Boca Raton, Florida) and their mixtures and alloys. In addition, the metal should form a silicide with a high melting point, greater than 1000°C and preferably greater than 1200°C. Of these metals, Ni, Cr, Pd, Ti, W, Ta, Mo, Co, Zr, and Ti-W alloy are preferred, and Mo, Ta, Ni, Pd, and Ti-W are most preferred.

The present invention provides a contact to SiC using a metal silicide formed in situ. The advantages of this technique include (1) the silicides provide stability at high temperatures, (2) the fabrication process permits self-alignment of the contact. Furthermore, the metal silicide layer may optionally be heavily doped, whereupon it may serve as a diffusion source for diffusing dopants into the contact region. Using the silicide as a diffusion source produces a heavily doped layer at the semiconductor-silicide interface, resulting in low contact resistance. A single dopant may be used to dope both the silicide and the SiC substrate, where such dopant is an effective doping species for both silicon and silicon carbide. Otherwise, two dopants may be used, one to dope the silicide and the other to dope the SiC. For p-type doping, boron can be used to dope both the silicide contact and the SiC substrate. Aluminum may also be used to dope the silicide. For n-type doping, P, As or Sb may be preferably employed to dope the silicide while N may be preferably employed to dope the SiC; As and Sb may be employed to dope both the silicide and the SiC.

The dopant may be implanted directly into the silicide. Co-doping during silicon growth, or during metal or silicide deposition may also be employed. To summarize, the doping may be accomplished using the following approaches:

1. After the metal is deposited, the structure may be implanted with the appropriate dopant. Ultra shallow silicide contacts have been formed to silicon by implanting arsenic or boron fluoride in this fashion (H. Jiang et al., J. Electrochem. Soc., **139** (1992), 196). However, implantation may cause damage and requires extra steps.

2. The silicon layer may be co-doped during growth by including the p- or n-type dopant source (e.g., AsH_3, PH_3, B_2H_6, etc.) in the source gas flowing into the CVD reactor. Better control of doping profile is possible via CVD compared to implantation, less damage results to the semiconductor lattice compared to the results from high energy species being implanted.

3. After the (undoped) silicon layer is grown, a thin layer of dopant may be deposited by, for example, sputtering, evaporation, CVD etc.) followed by deposition of the metal layer. The dopant is then diffused into the contact region by annealing. This technique is well-adapted for device fabrication schemes

employing sputtering or evaporation deposition processes. This process is also useful if it is desirable to avoid introducing silicon dopant species into the silicon carbide deposition reactor.

The advantages of doping the SiC-silicide interface from the silicide over conventional implantation into the interface are that (1) fewer process steps are required, (2) implantation damage in the SiC is eliminated, and (3) very shallow junctions can be formed.

The diffusion coefficients in SiC are very small, on the order of 10^{-13} to 10^{-16} cm^2/second at 1400°C (*Technology of Si, Ge and SiC*, subvolume C, Landolt-Bornstein, v. 17, ed. O. Madelung, M. Schulz and H. Weiss, Springer-Verlag, Berlin (1984)). However, as noted above, the thickness of the heavily doped region is very thin, less than 100Å. Thus annealing the silicon carbide / doped silicon / contact metal structure at temperatures near the epitaxial growth temperature of SiC (1400°C) for about 1 hour provides enough diffusion to form the required low resistance silicide contact structure.

The silicides are fabricated using a novel technique to prevent the formation of excess carbon or carbides at the SiC-contact interface, thus enhancing the thermal stability of the contact by eliminating extraneous species which could diffuse and degrade the contact. A thin silicon layer, optionally heavily doped, is grown on top of the SiC, followed by metal deposition on top of the silicon layer and annealing. A schematic of the process for fabricating contacts with this technique is shown in Figure 1. The structure 10 consists of a SiC substrate 11 on a surface of which is formed a heavily doped SiC contact layer 12 followed by a thin sacrificial silicon layer 13 (Figure 1A). In an actual device, these layers would be the last to be grown. Silicon is easily grown by simply turning off the carbon source in a SiC CVD growth reactor; or alternatively the silicon layer may be deposited by sputtering or evaporation. The silicon layer may be doped during or after growth to achieve even lower resistances in the metal silicide contact. After growth of the device and contact layers (heavily doped SiC followed by silicon), the metal layer 14 is deposited (Figure 1B), by sputtering, evaporation, CVD or any suitable technique. The silicide is then formed by annealing structure 17 in an inert ambient (Figure 1C), whereupon the metal and silicon layers react in situ to

form a metal silicide. These steps may optionally include introduction of a dopant, and annealing to diffuse the dopant to the SiC interface (Figure 1D).

It should be noted that this process can be used to make self-aligned contacts as well by first depositing and patterning a dielectric film (for example, SiO_2, silicon nitride, silicon oxynitride) prior to metal deposition. Upon annealing, a silicide forms only where the metal touches the silicon. The remaining metal on the dielectric pattern is then etched off, leaving intact the self-aligned silicide contact, which is much more resistant to the etchant. In addition, the deposited silicon (especially if it is undoped) and dielectric act as passivants for the SiC surface.

The steps for fabrication of such self-aligned contacts are shown schematically in Figure 2. Structure 20 in Figure 2A comprises a SiC substrate 21 on a surface of which is formed a heavily doped SiC contact layer 22 followed by a thin sacrificial silicon layer 23, upon which a dielectric masking material 24 such as silicon dioxide, silicon nitride, silicon oxynitride, etc. is deposited and patterned, leaving openings only where the contact is to be formed. The metal layer 25 for the silicide contact is then deposited over the entire sample as shown in Figure 2B. The sample is then annealed (Figure 2C), and the silicide 26 is only formed where the metal is in contact with the silicon interlayer. Finally the remaining metal is removed (Figure 2D) to leave the final self-aligned contact structure 29. The excess metal is typically removed using a wet chemical etch that preferentially etches the metal with respect to the silicide, but other removal techniques such as reactive ion etching, plasma etching, etc. are also possible. The remaining silicon (especially if it is undoped) and dielectric can be left on the sample to act as a passivation for the SiC surface or can optionally be removed, for example by using chemical etches such as HF/water etches for the silicon dioxide and HF/nitric acid etches for the silicon.

The thickness of the deposited silicon layer is selected so that the silicon is the stoichiometrically limiting material in reaction with the subsequently deposited metal to form metal silicide. In this way, excess carbon and carbide do not form, as they do when silicides are directly made on SiC. The amount of metal which should be deposited to consume a given layer of silicon during silicide formation may be calculated on the basis of stoichiometry of the silicide

compound formed and atomic weight and density of the pure metal. The deposited metal thicknesses required to consume a 30 nm layer of silicon during silicide formation are listed below for titanium, cobalt, nickel, and palladium, calculated on the basis of stoichiometry of the silicide compound formed and atomic weight and density of the pure metal:

Metal	Metal Thickness (nm)	Silicide Thickness (nm)
Ti	18	25
Co	8.3	29
Ni	16	36
Pd	45	64

After the deposition steps, the contact structure is typically annealed. It should be noted that annealing is required to form the ohmic silicide contact. If the silicon layer is heavily doped, the annealing step also promotes out-diffusion of the dopant into the immediate contact region to dope the interlayer structure and provide a narrower potential energy barrier. The contact structures may be annealed at 800-1100°C, with 900-1050°C preferred.

The contact structures of the present invention have been characterized based on two major parameters, specific contact resistances and reproducibility of electrical properties. The specific contact resistances to SiC were measured using the method of Cox and Strack (Solid State Electron., **10**, 1213 (1967)). This technique is easy to implement and does not require insulating substrates. Reproducibility was evaluated by recording current-voltage curves for contacts of the same size fabricated at different locations on the SiC wafers.

The features and advantages of the invention are more fully illustrated by the following non-limited examples.

EXAMPLE 1

Nine samples were prepared. First, 0.5 μm of heavily doped (~ 2×10^{18} cm^3 nitrogen-doped) n-type 6H-SiC was epitaxially grown by low pressure CVD. The substrates were single crystal 6H-SiC. On samples 2, 3, 5, 6, 8, and 9 a second

layer of silicon was grown on top of the n-type SiC epilayer in situ, without removal from the CVD reactor, by turning off the hydrocarbon source and lowering the reactor temperature to 850°C. All films had a specular appearance. The samples differed in the thicknesses of the silicon layers. Contact resistance patterns were fabricated on the samples by first forming the back contact to the SiC surface and then forming a silicide contact to the front silicon surface. The back contact consisted of a large area nickel ohmic contact that was annealed prior to deposition of the front metal. The front metal was deposited using lift-off lithography and evaporated metal. The diameters of the front contacts varied from 6 to 250 μm. Contact resistances were measured in the as-deposited state and after annealing. The annealing temperatures ranged from 900°C to 1100°C, the annealing time was 60 minutes, and the ambient gas was forming gas (N_2/H_2). The metal thicknesses were chosen to form most of the silicide from the silicon and not from the silicon carbide. Specific contact resistances R_C were measured by the Cox and Strack technique. The results are shown below:

Sample	Si Thickness (Å)	Ni Thickness (Å)	Anneal (°C)	R_C (x10^{-5} Ω-cm^2)
1	0	500	900	11±5
2	300	250	900	18±8
3	600	500	900	3±1.8
4	0	500	1000	5±4
5	300	250	1000	3±2.6
6	600	500	1000	1.3±0.5
7	0	500	1100	1.7±0.5
8	300	250	1100	n.o.*
9	600	500	1100	n.o.

* "n.o." means a non-ohmic contact was formed.

Clearly the samples with the silicon interlayer exhibited lower specific contact resistances. Nickel contacts required annealing to become ohmic. After a 900°C anneal in forming gas, most became ohmic and after annealing at 1000°C, all were ohmic. However, after a 1100°C forming gas anneal, only the large area contacts (>20 μm diameter) in most samples were ohmic. These results indicate that the optimum annealing temperature for nickel contacts is near 1000°C.

Because of the limitations of the Cox and Strack method, it is important to have an additional check on the calculated R_C values. The total resistance values have been measured for the same diameter contacts which have been processed together, with and without the silicon interlayer, as outlined below. Where all other parameters are the same, the contacts with the lowest total resistance will also have the lowest specific contact resistance. In virtually all cases, the samples with the lowest total resistance also have the lowest calculated R_C. Thus even though there may be some small errors in the determination of the absolute R_C values, the silicon interlayer does produce lower resistance contacts in this one-to-one comparison.

Total Resistance (Ω)	**Contact Diameter (μm)**						
Sample (Si thickness, Å)	**100**	**50**	**40**	**30**	**20**	**15**	**12**
1 (0)	16	18.9	21.9	28	41	-	-
2 (300)	22	23.8	26.2	31.2	-	-	-
3 (600)	8.8	12	13.4	15.4	33		
4 (0)	14	18.3	20.9	25.8	32.5	37.2	48
5 (300)	13.2	15.6	20	22	30	36	41
6 (600)	8.8	13	14.1	17.9	27.4	31.3	41.7

In addition to lower contact resistances, the silicon interlayer gave greatly improved reproducibility. Figure 3 shows many I-V scans for 250 μm diameter Ni contacts annealed at 900°C in forming gas for 60 minutes. Figure 3A shows scans of 15 contact structures on different parts of the wafer, fabricated with a 500Å sacrificial silicon interlayer structure, and 3B shows scans of 12 contact structures for a sample fabricated with no silicon interlayer. It is clear that the silicon interlayer greatly increases the reproducibility of the contact resistance.

EXAMPLE 2

Palladium contacts of sizes ranging from 10 μm up to 250 μm in diameter were fabricated to n-type 6H-SiC (nitrogen-doped) by the method described in Example 1, with silicon interlayer thicknesses varying from 300Å to 600Å and Pd

thicknesses of 300Å and 500Å. Annealing was performed in forming gas at temperatures varying from 800 to 1100°C, with the anneal at about 1000°C to 1100°C giving the ohmic contacts of the lowest contact resistances. Specific contact resistances of these were:

Sample	Si Thickness (Å)	Pd Thickness (Å)	Anneal (°C)	R_C (x10^{-5} Ω-cm^2)
10	600	300	1050	2±1
11	300	300	1100	3.5±1
12	380	500	1100	11±1

Figure 4 shows current-voltage scans of palladium contacts on n-doped 6H-SiC, with 4A showing scans of five contact structures on different parts of the SiC wafer fabricated employing a 300Å Pd layer over a 600Å silicon interlayer, 40 μm diameter contact annealed at 1050°C for 30 minutes in forming gas (5% H_2 in N_2, and 4B showing current-voltage scans of eight contact structures fabricated employing a 500Å Pd layer over a 380Å silicon interlayer, 100 μm diameter contact annealed at 1100°C for 30 minutes in forming gas.

While the invention has been described herein with reference to specific aspects, features, and embodiments, it will be apparent that other variations, modifications, and embodiments are possible, and all such variations, modifications, and embodiments therefore are to be regarded as being within the spirit and scope of the invention.

What is claimed is:

1. An ohmic contact SiC article, comprising:

a SiC base layer; and

a non-carbonaceous metal silicide ohmic contact structure on the SiC layer.

2. An article according to claim 1, further comprising a contact metal overlayer on the non-carbonaceous metal silicide ohmic contact structure.

3. An article according to claim 1, wherein the metal constituent of the metal silicide comprises a material selected from the group consisting of the Group 4b, 5b, 6b, 7b, and 8 transition metals and their mixtures and alloys.

4. An article according to claim 1, wherein the metal constituent of the metal silicide comprises a material selected from the group consisting of nickel, chromium, palladium, titanium, tungsten, tantalum, molybdenum, cobalt, zirconium, and their mixtures and alloys.

5. An article according to claim 1, wherein the metal constituent of the metal silicide comprises a material selected from the group consisting of molybdenum, tantalum, nickel, and titanium-tungsten alloys.

6. An article according to claim 1, wherein the metal silicide has a melting point of at least 1000°C.

7. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure comprises a metal silicide selected from the group consisting of platinum silicide, palladium silicide, tungsten silicide, tantalum silicide, nickel silicide, titanium silicide and cobalt silicide.

8. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure has been formed in situ by deposition of a silicon layer on the SiC base layer and deposition and deposition of a silicide-forming metal on the

silicon layer, with subsequent reaction of the silicide-forming metal with the silicon layer at sufficient temperature and for sufficient time to form said non-carbonaceous metal silicide ohmic contact structure.

9. An article according to claim 8, wherein the silicon layer comprises a dopant species, and the non-carbonaceous metal silicide ohmic contact structure is correspondingly doped in character.

10. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure comprises a material having a resistivity not exceeding 75 micro-ohms-cm.

11. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure comprises a material having a resistivity not exceeding 40 micro-ohms-cm.

12. An article according to claim 9, wherein the silicon layer is doped to a level of at least 10^{18} carriers/cm^3, with a dopant species selected from the group consisting of n-type dopant atoms and p-type dopant atoms.

13. An article according to claim 12, wherein the dopant species comprises an n-type dopant species.

14. An article according to claim 13, wherein the n-type dopant species is selected from the group consisting of phosphorus, arsenic, and antimony.

15. An article according to claim 12, wherein the dopant species comprises a p-type dopant species.

16. An article according to claim 15, wherein the p-type dopant species is selected from the group consisting of boron and aluminum.

17. An article according to claim 1, wherein the non-carbonaceous metal silicide ohmic contact structure has a specific contact resistance to SiC of less than about 5×10^{-5} ohm-cm^2.

18. A method of forming ohmic contacts on a SiC substrate, comprising the steps of:

forming a silicon layer on the SiC substrate;

providing a contact metal on the silicon layer; and

annealing the resulting article for sufficient time and at sufficient temperature to form a metal silicide contact by reaction of the silicon layer with the contact metal.

19. A method according to claim 18, wherein the reaction does not comprise the SiC substrate as a reactant.

20. A method according to claim 18, wherein said annealing is carried out at a temperature in the range of from about 800°C to about 1100°C.

21. A method according to claim 18, wherein the silicon layer is doped with a dopant species selected from the group consisting of p-type dopant atoms and n-type dopant atoms, at a doping concentration of at least 10^{18} carriers/cm^3.

22. A method according to claim 18, wherein the SiC substrate is grown by vapor deposition of silicon and carbon source reagents, immediately prior to growth of said silicon layer on the SiC substrate.

23. A method according to claim 22, wherein the SiC substrate is grown for a predetermined time by flowing of silicon-containing source reagent and carbon-containing source reagent to a deposition locus at which said growth is carried out, and wherein the supply of carbon-containing source reagent is discontinued to provide growth of silicon on the SiC substrate.

24. A method according to claim 18, comprising forming self-aligned contacts on the SiC substrate, by depositing and patterning a dielectric material on the SiC substrate prior to deposition of contact metal, so that upon annealing, a metal silicide forms only where the deposited metal contacts the silicon layer, and

etching to remove remaining metal on the patterned dielectric material to leave intact a self-aligned contact.

25. A method according to claim 18, wherein said step of forming the silicon layer on the SiC substrate comprises a forming method selected from the group consisting of chemical vapor deposition, sputtering, and evaporation from a silicon source.

26. A method according to claim 18, wherein the step of providing a contact metal on the silicon layer comprises a provision step selected from the group consisting of chemical vapor deposition, sputtering, and evaporation from a metal source.

27. A method according to claim 18 wherein the silicon layer is doped, by a doping method selected from the group consisting of ion implantation, co-deposition via chemical vapor deposition, sputtering and evaporation.

FIGURE 1

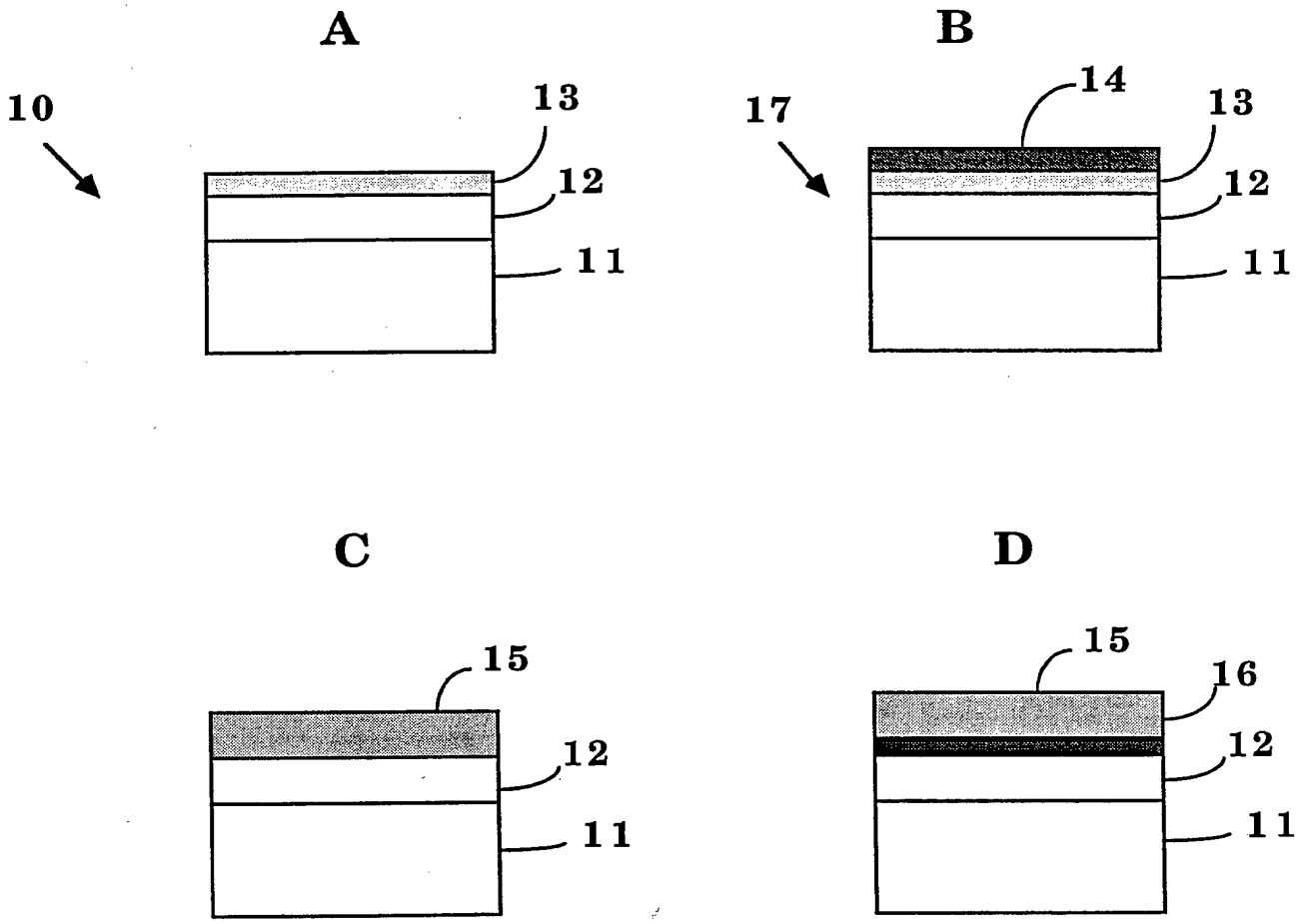


FIGURE 2

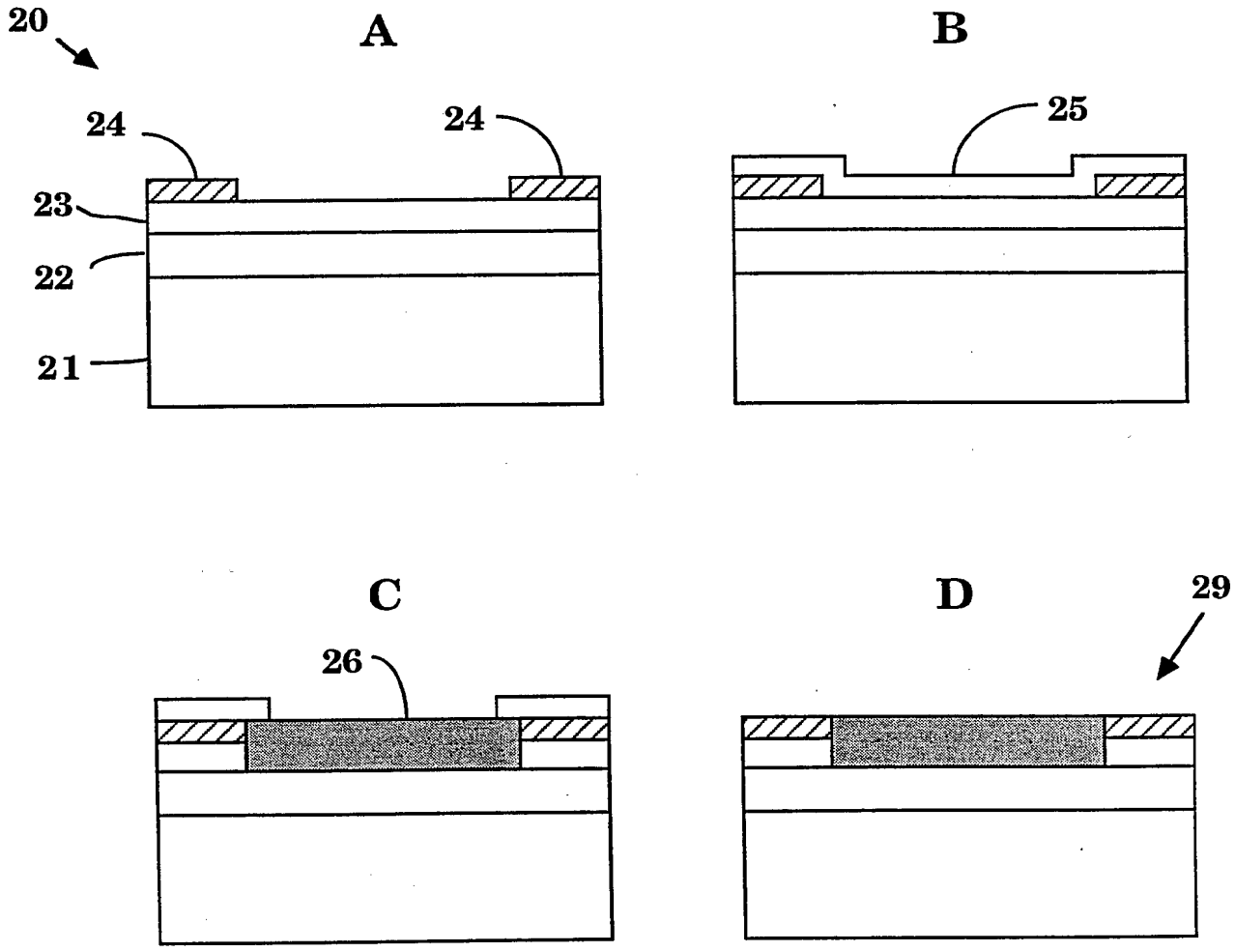
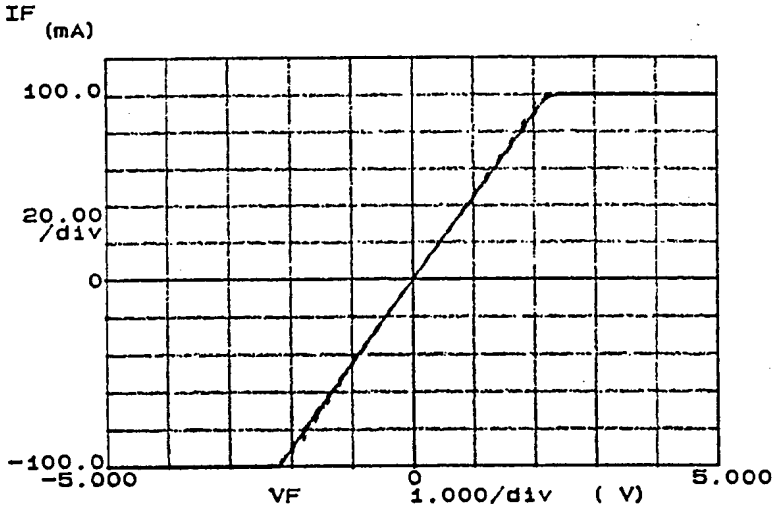


FIGURE 3

A


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5.000
VF
1.000/div (V)

B

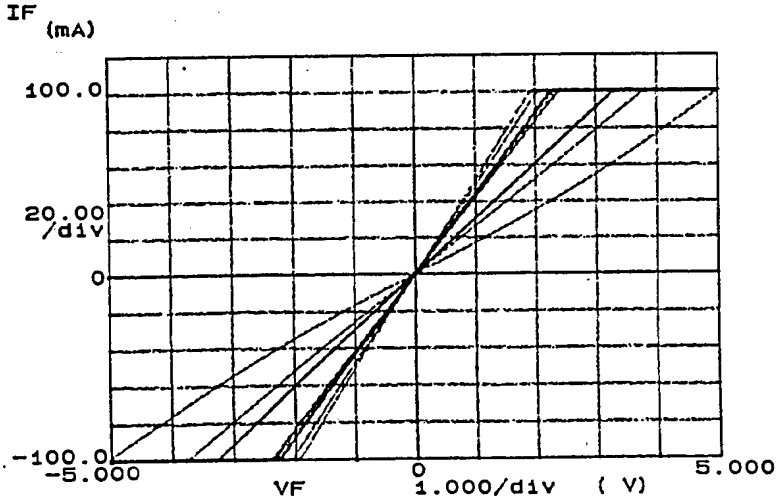
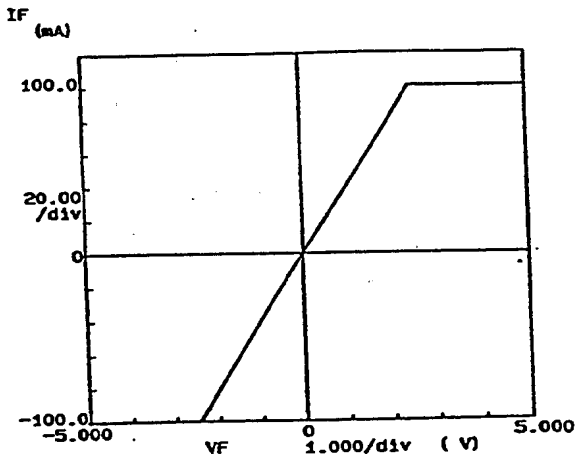
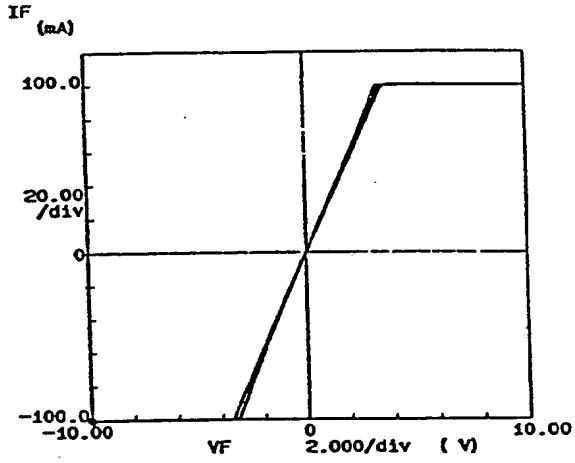

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VF
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FIGURE 4

A


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(V)
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/06983

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) : H01L 31/0312, 29/22, 31/0256, 31/0296, 21/20
US CL : 257/77, 78; 437/100
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/77, 78; 437/100

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Journal of Applied Physics, Volume 62, No. 9, issued 01 November 1987, I. Ohdomari et al, "Investigation of thin-film Ni/single-crystal SiC interface reaction", pages 3747-3750, particularly page 3748.	NONE
A	Semicounductor Devices - Physics and Technology, issued 1985, S.M. Sze, page 377.	NONE
A	US, A, 4,875,083 (PALMOUR) 17 October 1989, generally entire document.	NONE
A	Journal of Electrochemical Society, Volume 135, No 2, issued February 1988, J.A. Edmond et al, "Electrical Contacts to Beta Silicon Carbide Thin Films", pages 359-362.	NONE

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"O"	document referring to an oral disclosure, use, exhibition or other means		
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/06983

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Japanese Journal of Applied Physics, Volume 29, No. 3, issued March 1990, S. Hara et al, "Solid State Reaction of Mo on Cubic and Hexagonal SiC", pages 395-397.	NONE
A	Journal of Materials Research, Volume 5, No. 12, issued December 1990, V.M. Bermudez et al, "Investigation of the structure and stability of the Pt/SiC(001) interface", pages 2882-2893.	NONE

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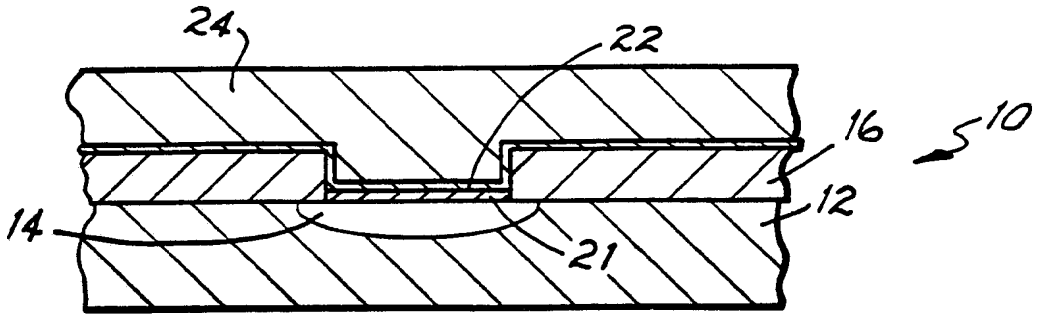
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(54) Title: METHOD OF MODIFYING CONTACT RESISTANCE IN SEMICONDUCTOR DEVICES AND ARTICLES PRODUCED THEREBY



(57) Abstract

A method is disclosed for modifying (reducing) the contact resistance in semiconductor devices having doped silicon junctions (14). The method includes selectively depositing a thin film of tungsten (21) on the exposed surface of a silicon wafer substrate (12) which has a native oxide layer thereon. The tungsten reduces or deteriorates the native oxide layer and makes clean contact to the silicon substrate. Subsequently a titanium nitride barrier layer (22) is deposited over the tungsten layer (21). Semiconductor devices produced according to the method of the invention have contact resistance values less than about $5x10^{-7}$ ohm cm^2.

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METHOD OF MODIFYING CONTACT RESISTANCE IN SEMICONDUCTOR DEVICES AND ARTICLES PRODUCED THEREBY

Field of the Invention

The present invention relates to semiconductor devices and more particularly to a process for improving the contact resistance of doped silicon junctions in semiconductor devices.

Background of the Invention

Semiconductor devices are typically fabricated starting with a substrate, e.g., a silicon wafer, having an insulating dielectric layer such as silicon dioxide on the surface thereof. In many applications, the silicon substrate has contact or junction regions in which the silicon is doped with boron, phosphorous, arsenic, or any other suitable doping compound. The doped contact regions in the substrate are exposed by etching a desired pattern in the oxide layer to form contact or via holes therein. Such etching is performed using etching techniques well known in the art. The contact holes are then filled with a conductor, such as aluminum, to provide electrical contact between the doped regions of the substrate and a conductive film which may be deposited

over the dielectric insulating layer to serve as a low resistance interconnection within the semiconductor device. Such films may be aluminum, doped polycrystalline silicon, tungsten, or another refractory metal.

The deposition of aluminum as the interconnect layer over an oxide insulating layer having contact holes therein has several drawbacks. One of these which is of particular concern is that aluminum diffuses rapidly or "spikes" into the silicon contact or junction regions exposed in the contact holes. As a means for inhibiting aluminum spiking in doped silicon contacts, it is known to deposit a barrier layer in the contact holes over the silicon contacts. One suitable barrier material is titanium nitride (TiN) and it may be deposited by known chemical vapor deposition or sputtering techniques.

The fabrication of semiconductor devices including, among other things, a barrier layer and an interconnect layer, as described above, typically includes as a first step etching the insulating layer to form contact holes therein. Subsequently, the barrier layer is deposited in the contact holes, and thereafter the desired interconnect layer may be deposited. In such fabrication processes, it is imperative that the surfaces upon which the various layers are deposited be free from impurities such as oxide films which form upon exposure to oxygen, i.e.,

native oxide films. The failure to provide clean contact between the layers of conductive material results in undesirably high contact resistance of the semiconductor device at the location of the contact regions. This high contact resistance greatly limits overall device speed and limits the development of higher density semiconductor devices.

Various techniques are known for removing native oxide films prior to performing chemical vapor deposition of subsequent layers over silicon contact regions. For example, U.S. Patent No. 4,902,645 discloses a dry etching treatment in which the native oxide layer is removed by a sputtering process or, alternatively, is etched away using an activated halide in combination with microwaves, high frequency waves, or ultraviolet light. In either case, the native oxide layer and the adjacent oxide insulator layer are both simultaneously etched, which is undesirable in certain circumstances. Furthermore, such processes may require more complicated apparatus to achieve the desired result. U.S. Patent No. 5,023,201 discloses the removal of a native oxide layer on an exposed titanium silicide ($TiSi_2$) surface by exposing that surface to a dilute hydrogen fluoride (HF) acid solution. This method is undesirable where the semiconductor devices being fabricated includes sensitive components and/or materials which are

deleteriously affected by exposure to an acid solution.

There is a need for semiconductor devices which have improved contact resistance and for a process of making such devices wherein native oxides present during fabrication are removed by steps which do not have the drawbacks associated with the prior art methods.

Summary of the Invention

The present invention overcomes the problems of the prior art processes mentioned above and improves the contact resistance of semiconductor devices by removing native oxide layers and providing a low contact resistance intermediary layer prior to depositing a titanium nitride barrier layer and a subsequent conductive interconnect layer thereon.

One aspect of the present invention is directed to a method wherein a thin film of tungsten (W) is selectively deposited by chemical vapor deposition in the contact holes on the exposed doped regions of the semiconductor substrate. These exposed regions will have a native oxide film thereon due to their exposure to oxygen. The thin tungsten film deteriorates the native oxide present on the substrate surface and makes a clean contact to the doped silicon regions. The tungsten is selectively deposited by silane (SiH_4) reduction of tungsten hexafluoride (WF_6) in the presence of a suitable diluent carrier gas such

as hydrogen, nitrogen or argon. This selective tungsten deposition step is preferably carried out at a pressure in the range of 2 to 150 m torr and at a temperature in the range of 240-400°C.

Subsequently, a titanium nitride (TiN) barrier layer is deposited on the exposed surface of the tungsten film in the contact hole. Preferably, the titanium nitride layer is deposited by low pressure chemical vapor deposition utilizing titanium tetrachloride ($TiCl_4$) and ammonia (NH_3) as reactant gases. The deposition of titanium nitride is effected at a temperature in the range of 400-750°C. At this elevated temperature, any tungsten oxides present on the exposed tungsten surface are evolved, resulting in clean contact of the titanium nitride to the tungsten film. Alternatively, the titanium nitride may be deposited utilizing suitable sputtering techniques.

When the method of the present invention is used in connection with substrates having contact regions doped with p-type dopants, the contact resistance of the resulting semiconductor device is less than about $5x10^{-7}$ ohm cm^2. When the method is used in connection with substrates having contact regions doped with n-type dopants, the contact resistance of the resulting semiconductor device is less than about $1x10^{-7}$ ohm cm^2. This represents a substantial reduction in the contact resistance of devices wherein the titanium nitride barrier layer is deposited directly

onto the exposed substrate surface. Such devices have a contact resistance on the order of about $5x10^{-5}$ ohm cm^2. This significant reduction in contact resistance improves the speed at which the ultimate device can be operated.

In another aspect, the present invention encompasses semiconductor devices produced according to the method of this invention. More particularly, the semiconductor devices of this invention include a thin tungsten film deposited on the exposed doped regions of a semiconductor substrate in the contact holes. The tungsten film deteriorates or reduces any native oxide present on the substrate and makes a clean contact thereto. The devices of the invention further include a titanium nitride barrier layer deposited over the thin tungsten film. The titanium nitride barrier layer is deposited on the tungsten film at a sufficiently high temperature such that any tungsten oxides present on the exposed tungsten surface are evolved and the titanium nitride makes a clean contact to the tungsten layer. The device of the invention has significantly reduced contact resistance vis-a-vis prior art devices.

Brief Description of the Drawings

Fig. 1 is a schematic sectional view of a silicon substrate, an etched insulating layer and a native oxide layer on the exposed substrate surface.

Fig. 2 is a schematic sectional view of the silicon substrate of Fig. 1 wherein a thin tungsten film has been deposited in the contact hole.

Fig. 3 is a schematic sectional view of the semiconductor device shown in Fig. 2 wherein a titanium nitride barrier layer has been deposited on the tungsten film and an additional blanket conductor layer has been deposited thereon.

Fig. 4 is a schematic sectional view of an alternative embodiment of the semiconductor device shown in Fig. 3 wherein the titanium nitride barrier layer is a thin blanket layer.

Detailed Description of the Invention

For purposes of illustration and description of the present invention, a basic semiconductor device structure useful in the practice of the present invention will be described. It should be appreciated, however, that various other configurations and/or arrangements can be utilized.

Figure 1 shows a semiconductor device 10 which comprises a substrate 12, which is typically a silicon substrate. Substrate 12 has a plurality (only one shown) of doped contact or junction regions 14, which are formed by techniques well known in the art and which do not form a part of the present invention. Typically, a semiconductor device initially has a continuous dielectric insulating layer 16 formed on the substrate. This dielectric insulating layer may

be a doped or undoped, deposited or grown silicon dioxide insulating layer. Insulating layer 16 is then selectively etched by known techniques to form contact holes 18 (only one shown) in which the doped regions 14 are exposed. Exposure of the device to oxygen oxidizes the silicon substrate and a thin layer of native oxide 20 is formed on the exposed surface of doped regions 14. This native oxide layer 20 must be removed since it increases the contact resistance of the semiconductor device.

In accordance with one aspect of the present invention, native oxide layer 20 is removed or deteriorated by selectively depositing a thin film of tungsten 21 in the contact hole 18 on the surface of the exposed silicon substrate at the location of the doped regions 14. The deposition of tungsten removes the native oxide 20 and forms a clean contact with the doped region 14 of the substrate, as shown in Fig. 2. Deposition of selective tungsten is accomplished by the silane reduction of tungsten hexafluoride in the presence of a diluent carrier gas such as hydrogen, nitrogen or argon at a pressure in the range of 2 to 150 m torr and a temperature in the range of 240-400°C. Preferably, silane is utilized at a flow rate of about 0.5 to 4.0 sccm (standard cubic centimeters), tungsten hexafluoride is utilized at a rate of about 1.0 to 10.0 sccm, and hydrogen is utilized at a flow rate of about 6 to 50 sccm.

Once the thin tungsten film 21 has been deposited, a barrier layer 22 of titanium nitride is deposited by low pressure chemical vapor deposition on the exposed thin tungsten film 21, as shown in Fig. 3. Titanium nitride layer 22 is deposited using known techniques. More particularly, the deposition is effected at a temperature in the range of 400-750°C and at a pressure in the range of about 50-50,000 m torr. By depositing the titanium nitride at this elevated temperature, any tungsten oxides which may have formed on the exposed tungsten surface will be evolved and thus the titanium nitride layer will form a clean contact with the tungsten layer. The titanium nitride deposition preferably utilizes titanium tetrachloride at about 10-30 sccm, ammonia at approximately 100 sccm and argon at approximately 20-30,000 sccm.

The titanium nitride acts as a barrier layer to inhibit aluminum spiking when aluminum is deposited as a blanket conductive interconnect layer 24 on the semiconductor device 10, as shown in Fig. 3. It will be appreciated that other materials may be used for interconnect layer 24, such as tungsten, or other suitable refractory metals. Additionally, the titanium nitride layer 22 may act as an adhesion layer for subsequent blanket tungsten deposition.

In accordance with a further aspect of the present invention, a semiconductor device 10 comprises

a silicon wafer substrate 12, a dielectric insulating layer 16 having at least one contact hole 18 etched therein to expose doped regions 14 of the silicon substrate. The device 10 further comprises a thin film 21 of tungsten selectively deposited by chemical vapor deposition on the exposed substrate surface and making clean contact thereto by the reduction or deterioration of any native oxide layer present. The tungsten layer acts as a low contact resistance intermediary layer. The device further comprises a titanium nitride barrier layer deposited in the contact hole 18 on the exposed surface of the tungsten layer 21. The deposition of the titanium nitride barrier layer is sufficiently high (on the order of 400-750°C) that any tungsten oxides present on the exposed surface of tungsten layer 21 thus are evolved and the titanium nitride makes clean contact to the tungsten layer. The device 10 may further comprise an additional blanket layer 24 of aluminum, tungsten, or any other suitable conductor.

The semiconductor device 10 of the present invention possesses superior contact resistance properties. More particularly, because of the clean contact between the thin tungsten film 21 and the doped region 14 of the silicon substrate 12, together with the clean contact between the titanium nitride layer 22 and the tungsten film 21, the contact resistance of the final product is less than about $5x10^{-7}$

ohm cm^2 in the case of p-type dopants in the silicon substrate, and less than about $1x10^{-7}$ ohm cm^2 in the case of n-type dopants, both of which are significantly lower than prior art devices that may have contact resistance values on the order of $5x10^{-5}$ ohm cm^2.

Fig. 4 shows an alternative embodiment of the semiconductor device of the present invention. In this embodiment, the titanium nitride barrier layer 22 is a thin blanket layer which covers both the dielectric layer 16 as well as the tungsten film 21. The subsequently applied conductor layer 24 covers the titanium nitride layer and fills in the remainder of contact hole 18.

It will be appreciated by persons skilled in the art that various modifications can be made to the method and device of the present invention without departing from the scope of the present invention as defined by the appended claims.

What is claimed is:

1. A method of modifying the contact resistance of wafers used for integrated circuits, comprising the steps of:

selectively depositing, by chemical vapor deposition, a thin film of tungsten on the exposed surface of a silicon wafer substrate having a native oxide layer thereon, whereby said native oxide present on said exposed surface is reduced so that said tungsten film makes clean contact to said substrate; and

depositing, by chemical vapor deposition, a titanium nitride barrier layer over the exposed surface of said tungsten film, wherein said titanium nitride deposition is effected at a sufficiently high temperature to evolve any tungsten oxide present on the exposed tungsten surface so that said titanium nitride layer makes clean contact to said tungsten film.

2. The method of claim 1 wherein said tungsten film is deposited by silane reduction of tungsten hexafluoride in the presence of a carrier gas selected from a group comprising hydrogen, nitrogen and argon.

3. The method of claim 2 wherein said deposition takes place at a temperature in the range of about 240-400°C.

4. The method of claim 3 wherein said deposition takes place at a pressure in the range of about 2-150 m torr.

5. The method of claim 1 wherein said titanium nitride layer is deposited by low pressure chemical vapor deposition utilizing titanium tetrachloride and ammonia as reactant gases.

6. The method of claim 5 wherein said titanium nitride deposition takes place at a temperature in the range of about 400-750°C.

7. The method of claim 6 wherein said titanium nitride deposition takes place at a pressure in the range of about 50 to 50,000 m torr.

8. A method of making wafers used for integrated circuits, said wafers having reduced contact resistance, comprising the steps of:

selectively depositing, by chemical vapor deposition, a thin film of tungsten on the exposed surface of a silicon wafer substrate having a native oxide layer thereon, whereby said native oxide present on said exposed surface is reduced so that said tungsten film makes clean contact to said substrate;

depositing, by chemical vapor deposition, a titanium nitride barrier layer over the exposed surface of said tungsten film, wherein said titanium nitride deposition is effected at a sufficiently high temperature to evolve any tungsten oxide present on the exposed tungsten surface so that said titanium nitride layer makes clean contact to said tungsten film;

whereby the clean contact between said tungsten film and said substrate, and the clean contact between said titanium nitride layer and said tungsten film serve to reduce the contact resistance of said wafer at the location of said tungsten and titanium nitride layers.

9. The method of claim 8 wherein said contact resistance of said wafer is less than about $5x10^{-7}$ ohm cm^2.

10. The method of claim 8 wherein said tungsten film is deposited by silane reduction of tungsten hexafluoride in the presence of a carrier gas selected from a group comprising hydrogen, nitrogen and argon.

11. The method of claim 10 wherein said deposition takes place at a temperature in the range of about 240-400°C.

12. The method of claim 11 wherein said deposition takes place at a pressure in the range of about 2-150 m torr.

13. The method of claim 8 wherein said titanium nitride layer is deposited by low pressure chemical vapor deposition utilizing titanium tetrachloride and ammonia as reactant gases.

14. The method of claim 13 wherein said titanium nitride deposition takes place at a temperature in the range of about 400-750°C.

15. The method of claim 14 wherein said titanium nitride deposition takes place at a pressure in the range of about 50 to 50,000 m torr.

16. A wafer for integrated circuits having reduced contact resistance, comprising:

a substrate;

an insulating layer on one surface of said substrate, said insulating layer having a contact hole formed therein such that a portion of said one surface of said substrate is exposed;

a thin film of tungsten selectively deposited, by chemical vapor deposition, in said contact hole and on said exposed surface of said substrate, whereby any native oxide present on said exposed surface is reduced so that said tungsten film makes clean contact to said substrate; and

a barrier layer of titanium nitride deposited, by chemical vapor deposition, over the exposed surface of said tungsten film, wherein said titanium nitride deposition is effected at a sufficiently high temperature to evolve any tungsten oxide present on said exposed tungsten surface so that said titanium nitride layer makes clean contact to said tungsten film.

17. The wafer of claim 16 wherein said wafer has a contact resistance less than about $5x10^{-7}$ ohm cm^2 at the location of said tungsten and titanium nitride layers.

18. The wafer of claim 17 wherein said substrate is silicon.

19. The wafer of claim 18 wherein said insulating layer is a dielectric insulating layer.

20. The wafer of claim 19 wherein said substrate is doped at the location of the contact hole in said insulating layer.

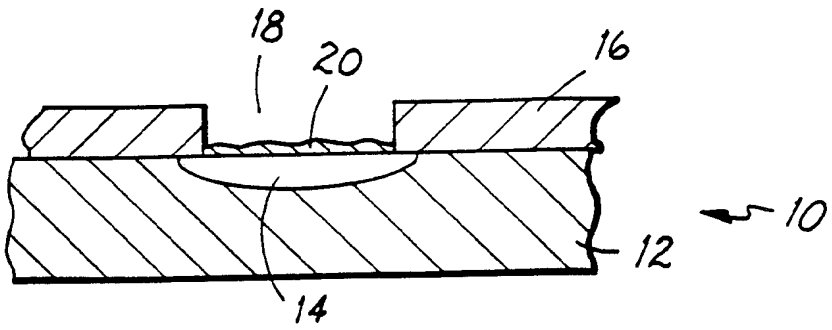


FIG. 1

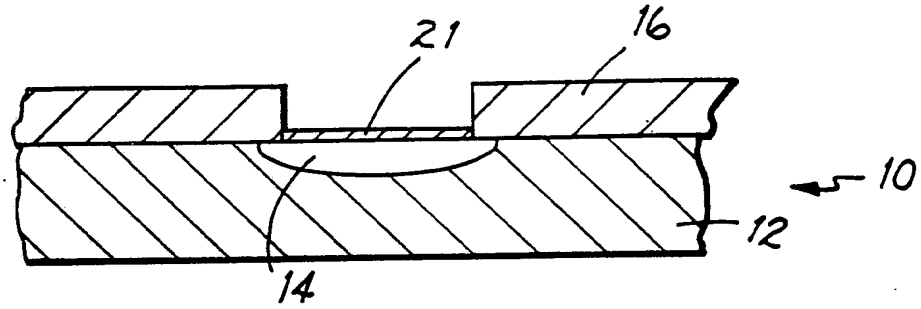


FIG. 2

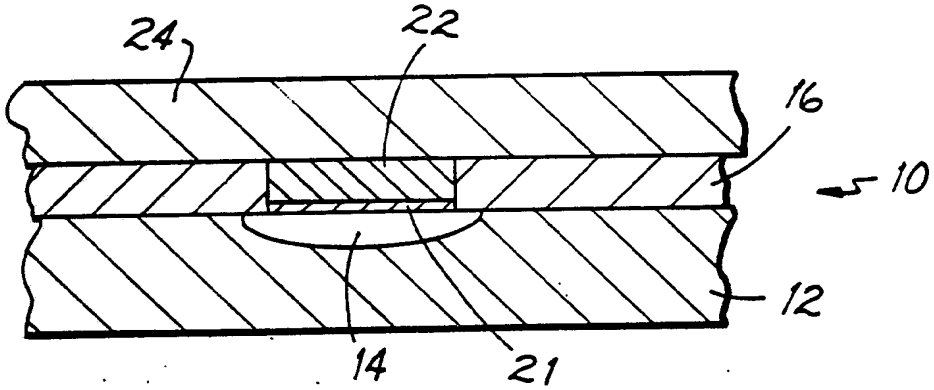


FIG. 3

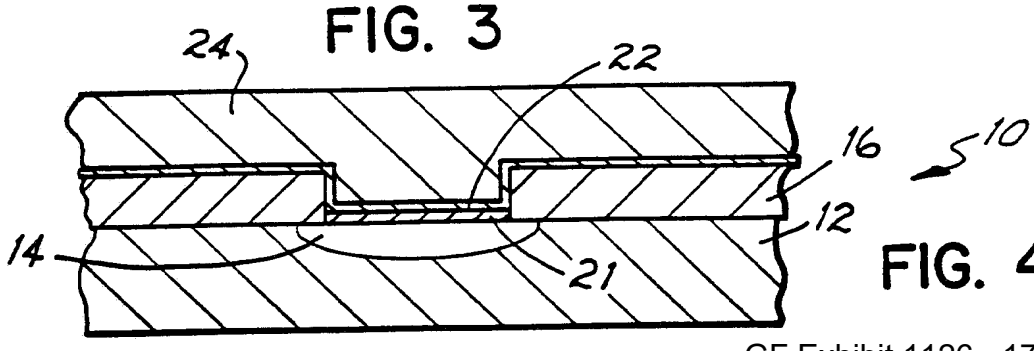


FIG. 4

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INTERNATIONAL SEARCH REPORT

PCT/US 92/10213

International Application No

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L21/285

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H01L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 067 (E-0885)7 February 1990 & JP,A,12 86 447 (MITSUBISHI ELECTRIC CORP.) 17 November 1989 see abstract	1,8,16, 18-20
A	US,A,3 535 176 (P.J.WHORISKEY) 20 October 1970 see column 2, line 9 - line 19	1
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 425 (E-681)10 November 1988 & JP,A,63 164 242 (FUJITSU LTD) 7 July 1988 see abstract	1
A	EP,A,0 414 267 (APPLIED MATERIALS INC.) 27 February 1991 see column 7, line 28 - line 41	2-3, 10-11

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
19 MARCH 1993	29. 03. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	SCHUERMANS N.F.

Form PCT/ISA/210 (second sheet) (January 1985)

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III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	US,A,4 897 709 (N.YOKOYAMA ET AL.) 30 January 1990 see column 14, line 10 - line 43	5-6, 13-14

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

US 9210213
SA 68041

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-3535176	20-10-70	None		
EP-A-0414267	27-02-91	US-A-	5028565	02-07-91
		JP-A-	3090572	16-04-91
US-A-4897709	30-01-90	JP-A-	1264258	20-10-89

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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(33)優先権主張国　ドイツ（ＤＥ）

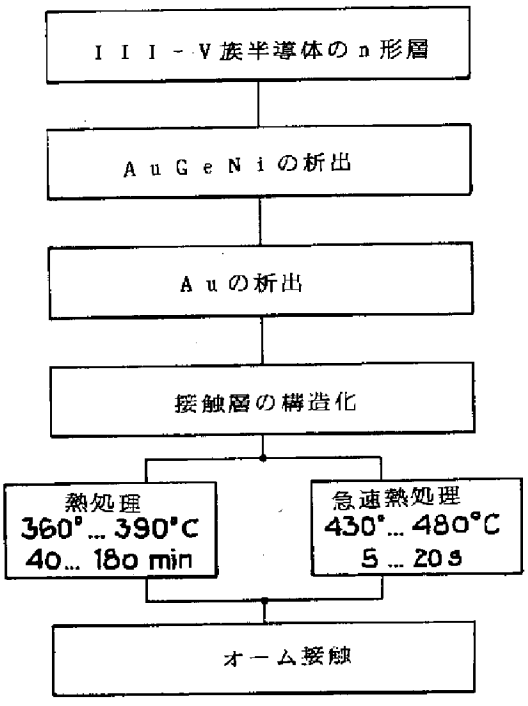
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(54)【発明の名称】　化合物半導体用オーム接触の製造方法

(57)【要約】
【構成】　ｎ形ＩＩＩ－Ｖ族化合物半導体上にＡｕＧｅＮｉ層が形成され、ＡｕＧｅＮｉ層の厚さが５０～２００ｎｍであり、ＡｕＧｅＮｉ層中のゲルマニウム濃度もニツケル濃度も１重量％未満である。ＡｕＧｅＮｉ層上には２５０～１０００ｎｍの厚さのＡｕ層が形成される。この層配列は合金化されるのではなく、４３０～４８０℃の温度で５～２０秒間、又は３６０～４００℃の温度で４０～１８０分間熱処理される。
【効果】　製造された金属半導体接触は接触抵抗が低く、合金化ＡｕＧｅＮｉ接触の不均一性が取り除かれている。



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【特許請求の範囲】
【請求項１】　ＩＩＩ－Ｖ族化合物半導体のｎ形半導体層上にオーム接触を製造する方法であつて、まずｎ形半導体層上に金属接触層を形成し、該金属接触層上に金層を形成し、次いで得られた配列を熱処理工程で熱処理するものにおいて、前記金属接触層がＡｕＧｅＮｉからなり、そのゲルマニウム分とニツケル分がそれぞれ１重量％を超えないことを特徴とする方法。
【請求項２】　前記層配列を３６０～３９０℃で４０～１８０分間熱処理することを特徴とする、請求項１に記載の方法。
【請求項３】　前記層配列を４３０～４８０℃で５～２０秒間熱処理することを特徴とする、請求項１に記載の方法。
【請求項４】　前記ＡｕＧｅＮｉ層中のニツケル分が０．５重量％であることを特徴とする、請求項１ないし３の１つに記載の方法。
【請求項５】　前記ＡｕＧｅＮｉ層中のゲルマニウム分が０．４重量％であることを特徴とする、請求項１ないし４の１つに記載の方法。
【請求項６】　前記ＡｕＧｅＮｉ層の厚さが５０～２００ｎｍの範囲であることを特徴とする、請求項１ないし５の１つに記載の方法。
【請求項７】　前記金層の厚さが２５０～１０００ｎｍの範囲であることを特徴とする、請求項１ないし６の１つに記載の方法。
【請求項８】　前記熱処理工程の前に、前記ＡｕＧｅＮｉ層を覆う前記金属上にまずＴｉＷＮ層、次いでアルミニウム層を析出させることを特徴とする、請求項１ないし７の１つに記載の方法。
【請求項９】　前記ＴｉＷＮ膜層の厚さが１００～５００ｎｍの範囲内であることを特徴とする、請求項８に記載の方法。
【請求項１０】　前記アルミニウム層の厚さが１～３μｍの範囲内であることを特徴とする、請求項８又は９に記載の方法。
【請求項１１】　前記熱処理工程の前に接触配列が構造化されることを特徴とする請求項１ないし９の１つに記載の方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、ＩＩＩ－Ｖ族化合物半導体のｎ形半導体層、特にＧａ１－ｘＡｌｘＡｓからなるｎ形半導体層上にオーム接触を製造する方法であつて、アルミニウムの混合比（ｘ）が０≦×≦１の範囲内であるものに関する。
【０００２】
【従来の技術】工業用半導体技術においては、ｎ形ＩＩＩ－Ｖ族化合物半導体結晶ＧａＡｓ及びＧａＡｌＡｓ用のオーム接触としてＡｕＧｅ及びＡｕＧｅＮｉ共融合金が主に使用される。接触層のゲルマニウム濃度が低く、かつオーム接触の形成が合金化工程ではなく、熱処理によつて行われるとき、金ゲルマニウム接触層を用いて２元ｎ形化合物半導体ガリウムヒ素上に再現可能に均一な接触を製造することができる。このような方法がドイツ連邦共和国特許第４１１３９６９号明細書に記載されている。熱処理された接触の比接触抵抗は、代表的には約１×１０$^{-5}$Ωｃｍ^{2}である。
【０００３】３元ｎ形化合物半導体Ｇａ１－ｘＡｌｘＡｓ用オーム接触としての金ゲルマニウム層に適した用途は限られている。アルミニウム分の増加に伴い、蒸着ＡｕＧｅ層の密着性が劣化し、かつその接触抵抗が上昇する。ＧａＡｌＡｓの表面に自然酸化皮膜が生成するので、アルミニウム混合比（ｘ）が０≦×≦０．４の範囲内にあるＧａ１－ｘＡｌｘＡｓについてのみ、金ゲルマニウム接触の使用が可能となる。任意のアルミニウム混合比を有するｎ形Ｇａ１－ｘＡｌｘＡｓ用の接触としては金、ゲルマニウム及びニッケルからなる多層接触が好適であることが知られている。ニツケルは合金化工程の間に固体反応によつてＧａＡｌＡｓ表面上の自然酸化皮膜を溶解して、ＮｉＡｓ、β－ＡｕＧａ等の化合物を生成する。文献に記録されたＡｕＧｅＮｉ接触では、金ゲルマニウムは共融合金ＡｕＧｅ（８８／１２）として形成されるか、又は金とゲルマニウムとからなる離散層として形成される。第１の方法は、例えばＡｐｐｌｉｅｄ　Ｐｈｙｓｉｃ　Ｌｅｔｔｅｒｓ５４（８）、１９８９年２月、７２１～７２３頁と欧州公開特許第３２３５５４号明細書に記載されており、第２の方法は欧州公開特許第４１９０６２号明細書に記載されている。引き続き金／ゲルマニウム層上にニッケル層が形成される。ニツケル層は、一般にＡｕＧｅ（８８／１２）１００ｎｍ当たり約２８ｎｍに相当する厚さを有する。
【０００４】ＡｕＧｅＮｉ接触の総厚は決定的要素ではなく、多くの場合１００～２５０ｎｍの範囲にある。しかし総厚が１００ｎｍ以下に減少すると接触抵抗が上昇する恐れがある。化合物半導体上に各層が形成される順序は、層配列が後続の熱処理工程において溶解され、合金化されるので、特別重要ではない。それ故に文献には、まずニツケル、次に金ゲルマニウムを化合物半導体結晶上に形成して製造されるＡｕＧｅＮｉ接触も記録されている。合金化ＡｕＧｅＮｉ接触の層抵抗が高く、代表的には約２Ω／スクエアであるので、通常は付加的な金補強材が形成される。オーム接触を形成するためにはＡｕＧｅＮｉ膜に熱処理を施す必要がある。その際の温度は好ましくは３６０～５００℃である。ＡｕＧｅ（８８／１２）共融混合物の溶融温度が約３６０℃と低いので、この工程は合金化工程である。接触金属は加熱されると液化し、冷却されると再結晶化する。
【０００５】公知のＡｕＧｅＮｉ接触は以下の欠点を有する。合金化の制御は技術的に困難であり、劣化した形

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態構造と不規則な周縁部とを有する接触を生じる。この接触は離散ニツケル層を有するので、エツチング法による構造化は不可能であるか、又は多大の経費をかけてはじめて可能となる。寸法安定性の維持の可能性はきわめて限られている。それ故公知のＡｕＧｅＮｉ接触に対する構造化法としては、接触金属の不要部分をその下部にあるフオトレジスト構造を利用して除去する技術（リフトオーフ法）が利用される。しかしこの方法は、一層簡単かつ一層確実な方法が適用できない場合にのみ、大量生産において利用される。

【０００６】

【発明が解決しようとする課題】それ故に本発明の課題は、任意の混合比（ｘ）を有する化合物半導体Ｇａ１－ｘＡｌｘＡｓのｎ形半導体層上にオーム接触を製造する方法を示すことであり、その際オーム接触は簡単なエツチング法によつて構造化可能でなければならない。上記接触は更に接触抵抗が低く、不均一性が除去されていなければならない。

【０００７】

【課題を解決するための手段】この課題を解決するため本発明によれば、金属接触層がＡｕＧｅＮｉからなり、そのゲルマニウム分とニツケル分がそれぞれ１重量％を超えないことによつて解決される。本方法の更なる展開は従属請求項の特徴にしたがつて行われる。

【０００８】半導体結晶のｎ形半導体層上にまずＡｕＧｅＮｉ皮膜を蒸着させるか、陰極スパツタリングによつてスパツタする。ＡｕＧｅＮｉ皮膜は１重量％未満のゲルマニウムと１重量％未満のニツケルを含有している。引き続きＡｕＧｅＮｉ皮膜上に金補強材を形成する。好ましくはこの工程は酸化膜の生成を防止するために、下層を形成したのと同じ工程によつて行われる。従来の合金化工程の代わりに、本方法は短時間熱処理による熱処理を含み、急速熱処理（ＲＴＰ）又は炉内の従来の熱処理工程による熱処理も含んでいる。熱処理の間に、ＡｕＧｅＮｉ皮膜は合金化工程におけるような液化とそれに続く再結晶とを生じない。オーム接触は固体反応によつてゲルマニウム原子がＡｕＧｅＮｉ層からＩＩＩ－Ｖ族化合物半導体のｎ形層の表面に拡散することによつて生じる。この接触は簡単に製造され、ゲルマニウム及びニツケルの濃度が低いので、半導体技術において一般的な金エツチング法によつて難なく残さいなしに構造化することができる。

【０００９】

【実施例】以下図を参考に、１実施例に基づいて本発明を詳しく説明する。

【００１０】図１はＩＩＩ－Ｖ族化合物半導体、例えばアルミニウム混合比ｘ（０≦ｘ≦１）のＧａＡｌＡｓのｎ形半導体層上にオーム接触を製造する方法の流れ図を示す。この方法は、半導体結晶の前面上に第１及び第２金属層を形成するための各１つの工程と、オーム接触を生成するための熱処理工程とを含んでいる。本方法の第１工程において、ＡｕＧｅＮｉ層２は電子線によつて加熱されるＡｕＧｅＮｉ源からの熱蒸発によるか、又はＡｕＧｅＮｉターゲツトの陰極スパツタリングによつて、ＩＩＩ－Ｖ族化合物半導体結晶１上に形成される。本方法の第２工程において、Ａｕ層３は同じ方法に基づいてＡｕＧｅＮｉ層２上に形成される。蒸着又は陰極スパツタリングは約2×10^{-7}ｍｂａｒのベース圧力において行われる。

【００１１】図２は熱処理前のオーム接触の層配列を示す。金属半導体接触は２つの層、即ちＡｕＧｅＮｉ層２とＡｕ層３とからなる。ＡｕＧｅＮｉ層２はｎ形ＩＩＩ－Ｖ族化合物半導体１の直上にあり、厚さが５０～２００ｎｍである。ＡｕＧｅＮｉ層中のゲルマニウム濃度は約０．４重量％であり、１重量％を超えてはならない。ニツケル濃度は約０．５重量％であり、やはり１重量％を超えてはならない。ＡｕＧｅＮｉ層上には厚さ２５０～１０００ｎｍのＡｕ層３がある。

【００１２】熱処理工程において多層接触配列は、オーム接触層を生成するために、４３０～４８０℃の温度で５～２０秒間、いわゆる急速熱処理によつて熱処理される。熱処理工程は、例えばN_2又はＡｒ等の不活性ガスの不活性雰囲気中で行われる。オーム接触はゲルマニウム原子がＡｕＧｅＮｉ層２からｎ形ＩＩＩ－Ｖ族化合物半導体１の表面に拡散することによつて生じる。この方法において特に重要なことは、接触層が溶融して合金化接触の方から公知の不均一性が生じることのないように、熱処理工程の時間及び温度を選択することである。

【００１３】急速熱処理の代わりに従来の熱処理工程も実施することができる。この場合、プロセス温度は３６０～３９０℃である。熱処理工程の持続時間は４０分～３時間である。この場合にも、温度と時間は接触層が溶融しないように選択されている。従来の工程による熱処理は、好ましくは例えばN_2ガス又はＡｒガスの不活性雰囲気中で実施される。しかし熱処理工程は還元性雰囲気中でも実施することができる。

【００１４】本発明による方法によつてその上にオーム接触が製造されるｎ形ＩＩＩ－Ｖ族化合物半導体の例には、ＧａＡｓ、Ｇａ１－ｘＡｌｘＡｓ、ＧａＰ、ＩｎＰ及び

類似の半導体結晶がある。特に適しているのは、Ｇａ１－ｘＡｌｘＡｓ（０≦ｘ≦１）のための方法であり、特にアルミニウム混合比（ｘ）が０．４より多い場

合である。

【００１５】金又はアルミニウムからなる１つ又はそれ以上のボンデイングワイヤによつて接触層をボンデイングする場合、ボンデイング中の接触又は半導体結晶の破

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損を防止するために、1つ又はそれ以上の金属層によつて接触を補強する必要がある。補強層（ボンデイングパツド）として、好ましくは金又はアルミニウムが使用される。厚い金層はＡｕＧｅＮｉ接触層上に直接形成することができるのに対して、アルミニウムからなるボンデイングパツドは拡散障壁として作用する中間層上に形成せねばならない。チタンタングステン窒化物（ＴｉＷＮ）からなる層はアルミニウムがボンデイングパツドから接触層中に拡散するのを防止する。副次的効果として、熱処理工程におけるオーム接触とアルミニウム補強材との合金化が阻止される。

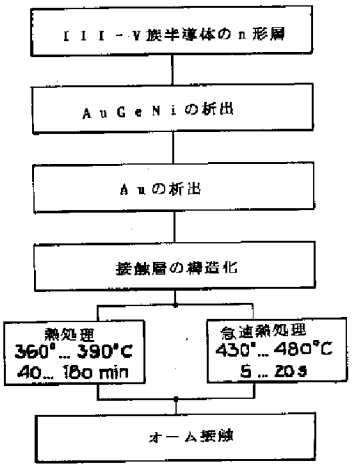
【００１６】好ましい1実施態様では、ｐ形$Ga_{0.65}Al_{0.35}As$及びn形$Ga_{0.32}Al_{0.68}As$からなる単一ヘテロ構造を有する半導体結晶が液相エピタキシヤル成長によつてｐ形ＧａＡｓ基板上に製造され、ｎ形エピタキシヤル層中の電荷キヤリヤ濃度が$1\times10^{18}cm^{-3}$であり、この結晶の表面上に厚さ１００ｎｍのＡｕＧｅＮｉ層と厚さ５００ｎｍのＡｕ層が形成される。ＡｕＧｅＮｉ層は０．４重量％のゲルマニウム分と０．５重量％のニツケル分とを含有する。別の方法工程においてＡｕ層上にまず、厚さ０．２５μのＴｉＷＮ拡散障壁と厚さ２μの別のＡｌ補強材を析出させる。ＴｉＷＮ層はスパツタされる。引き続き接触はフオトレジストマスクを利用して湿化学的に構造化される。例えばアルミニウム層の不要部分はリン酸で除去され、ＴｉＷＮ層の不要部分は過酸化水素で除去され、ＡｕＧｅＮｉ－Ａｕ層の不要部分は金エツチングで除去される。フオトレジストマスクの除去後に多層接触配列は４８０℃で１５秒間急速熱処理工程によつて熱処理される。こうして製造されたオーム接触は表面が平滑であり、問題なくワイヤボンデイングすることができる。接触抵抗は約$5\times10^{-5}\Omega cm^2$である。

【図面の簡単な説明】

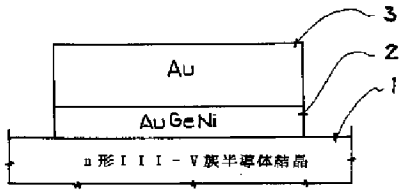
【図１】本発明による方法の流れ図である。

【図２】温度処理前の接触の層配列の横断面図である。

【図１】



【図２】



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Espacenet

JPH07263375A MANUFACTURE OF OHMIC CONTACT FOR COMPOUND SEMICONDUCTOR

Applicants: TELEFUNKEN MICROELECTRON

Inventors: YOTSUHEN GERUNERU

Classifications:

IPC ***H01L21/203; H01L21/28; H01L21/285; H01L29/45;*** (IPC1-7): H01L21/203; H01L21/28;

CPC **H01L21/28575 (EP); H01L29/452 (EP);**

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MANUFACTURE OF OHMIC CONTACT FOR COMPOUND SEMICONDUCTOR

Abstract

PURPOSE: To obtain an ohmic contact exhibiting a low contact resistance and without nonuniformity in a structure which is comprised of an n-type semiconductor layer on which a metallic contact layer and a gold layer are formed and are heat treated by forming the metallic contact layer with AuGeNi and by limiting the content of germanium and nickel to a specified weight %, respectively. CONSTITUTION: An AuGeNi layer 2 is formed on a III-V compound semiconductor crystal 1 by heat vaporization from an AuGeNi source which is heated by an electron beam or by cathode sputtering of an AuGeNi target. In this case, the content of germanium and nickel in the AuGeNi layer 2 must not exceed 1 weight % respectively. A gold layer 3 is similarly formed on the AuGeNi layer 2. An ohmic contact exhibiting a low contact resistance and without nonuniformity is produced by diffusing atoms of germanium from the AuGeNi layer 2 to the surface of the n-type III-V compound semiconductor 1 by a so-called high-speed heat treatment.

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DESCRIPTION JPH07263375

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a method for producing an ohmic contact on an n-type semiconductor layer of a III-V group compound semiconductor, particularly an n-type semiconductor layer made of Gal-xAlxAs, which has a mixing ratio of aluminum x) is within the range of $0 \leqq \times \leqq 1$.

[0002]

BACKGROUND OF THE INVENTION In industrial semiconductor technology, AuGe and AuGeNi eutectic alloys are mainly used as ohmic contacts for n-type III-V compound semiconductor crystals GaAs and GaAlAs. When the germanium concentration of the contact layer is low and the formation of the ohmic contact is performed not by the alloying process but by the heat treatment, the gold germanium contact layer is used to reproducibly and uniformly form the binary n-type compound semiconductor gallium arsenide. The contact can be manufactured. Such a method is described in German Patent DE 41 13 969. The specific contact resistance of the heat treated contact is typically about $1 \times 10 -5\ \Omega\mathrm{cm}\ 2$.

[0003]

Suitable applications for gold germanium layers as ohmic contacts for the ternary n-type compound semiconductor Gal-xAlxAs are limited. As the aluminum content increases, the

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adhesion of the vapor-deposited AuGe layer deteriorates and the contact resistance increases. Since a natural oxide film is formed on the surface of GaAlAs, it is possible to use gold-germanium contact only for Gal-xAlxAs whose aluminum mixing ratio (x) is in the range of $0 \leqq \times \leqq 0.4$. It is known that multilayer contacts consisting of gold, germanium and nickel are suitable as contacts for n-type Gal-xAlxAs having an arbitrary aluminum mixing ratio. Nickel dissolves the native oxide film on the surface of GaAlAs by a solid reaction during the alloying process to form compounds such as NiAs and β-AuGa. In the AuGeNi contacts documented in the literature, gold germanium is formed as the eutectic AuGe (88/12) or as a discrete layer of gold and germanium. The first method is described, for example, in Applied Physic Letters 54 (8), February 1989, pages 721 to 723 and European Patent No. 323554, and the second method is described in European Patent No. 419062. It is described in the book. Subsequently, a nickel layer is formed on the gold / germanium layer. The nickel layer typically has a thickness corresponding to about 28 nm per 100 nm of AuGe (88/12).

[0004]

The total thickness of the AuGeNi contacts is not critical and often lies in the range 100-250 nm. However, if the total thickness is reduced to 100 nm or less, the contact resistance may increase. The order in which the layers are formed on the compound semiconductor is not particularly important as the layer sequence is melted and alloyed in the subsequent heat treatment step. Therefore, the literature also records AuGeNi contacts made by first forming nickel and then gold germanium on the compound semiconductor crystal. Due to the high layer resistance of the alloyed AuGeNi contacts, typically around 2 Ω / square, additional gold reinforcement is usually formed. It is necessary to subject the AuGeNi film to a heat treatment in order to form an ohmic contact. The temperature at that time is preferably 360 to 500 ° C. This step is an alloying step because the melting temperature of the AuGe (88/12) eutectic mixture is as low as about 360 ° C. The contact metal liquefies when heated and recrystallizes when cooled.

[0005]

Known AuGeNi contacts have the following drawbacks. Controlling alloying is technically difficult and results in contacts with degraded morphology and irregular edges. Since this contact has discrete nickel layers, structuring by the etching method is not possible or only possible at great expense. The possibilities of maintaining dimensional stability are very limited. Therefore, as a known structuring method for the AuGeNi contact, there is used a technique (lift-off method) of removing an unnecessary portion of the contact metal by using the photoresist structure under the contact metal. However, this method is used in mass production only if simpler and more

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reliable methods cannot be applied.

[0006]

It is therefore the object of the present invention to show a method for producing ohmic contacts on an n-type semiconductor layer of a compound semiconductor Gal-xAlxAs having an arbitrary mixing ratio (x), The ohmic contact must then be structurable by simple etching methods. The contact should have a lower contact resistance and the non-uniformity should be eliminated.

[0007]

In order to solve this problem, according to the present invention, the metal contact layer is made of AuGeNi, and its germanium content and nickel content do not exceed 1 wt% each. . Further developments of the method are made according to the features of the dependent claims.

[0008]

An AuGeNi coating is first deposited on the n-type semiconductor layer of the semiconductor crystal or is sputtered by cathode sputtering. The AuGeNi coating contains less than 1% by weight germanium and less than 1% by weight nickel. Subsequently, a gold reinforcing material is formed on the AuGeNi coating. Preferably, this step is performed by the same step as that for forming the lower layer in order to prevent the formation of an oxide film. Instead of a conventional alloying process, the method includes a heat treatment by a short time heat treatment, including a rapid thermal treatment (RTP) or a conventional heat treatment process in a furnace. During the heat treatment, the AuGeNi coating does not undergo liquefaction and subsequent recrystallization as in the alloying process. The ohmic contact is caused by the diffusion of germanium atoms from the AuGeNi layer to the surface of the n-type layer of the III-V compound semiconductor by a solid state reaction. This contact is easy to manufacture and, due to the low concentration of germanium and nickel, can be structured without difficulty and without residue by the gold etching method common in semiconductor technology.

[0009]

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS The present invention will be

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described in detail based on one embodiment with reference to the drawings.

[0010]

FIG. 1 shows a flow chart of a method for making an ohmic contact on an n-type semiconductor layer of a III-V compound semiconductor, for example a GaAlAs with an aluminum mixing ratio x ($0 \leqq x \leqq 1$).

The method includes one step each for forming first and second metal layers on the front surface of the semiconductor crystal, and a heat treatment step for creating an ohmic contact. In the first step of the method, the AuGeNi layer 2 is formed on the III-V compound semiconductor crystal 1 by thermal evaporation from an AuGeNi source heated by an electron beam or by cathodic sputtering of the AuGeNi target. To be done. In the second step of the method, the Au layer 3 is formed on the AuGeNi layer 2 according to the same method. Deposition or cathodic sputtering is done at a base pressure of about 2×10^{-7} mbar.

[0011]

FIG. 2 shows the ohmic contact layer arrangement before heat treatment. The metal semiconductor contact consists of two layers, an AuGeNi layer 2 and an Au layer 3. The AuGeNi layer 2 is directly above the n-type III-V compound semiconductor 1 and has a thickness of 50 to 200 nm. The germanium concentration in the AuGeNi layer is about 0.4% by weight and should not exceed 1% by weight. The nickel concentration is about 0.5% by weight and again should not exceed 1% by weight. On the AuGeNi layer is the Au layer 3 having a thickness of 250 to 1000 nm.

[0012]

In the heat treatment step, the multi-layer contact array is heat treated by a so-called rapid heat treatment for 5 to 20 seconds at a temperature of 430 to 480 ° C to produce an ohmic contact layer. The heat treatment step is performed in an inert atmosphere of an inert gas such as N2 or Ar. The ohmic contact is caused by the diffusion of germanium atoms from the AuGeNi layer 2 to the surface of the n-type III-V compound semiconductor 1. Of particular importance in this method is the selection of the time and temperature of the heat treatment step so that the

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contact layer does not melt and cause the known non-uniformities from alloying contact.

[0013]

Conventional heat treatment steps can also be performed instead of rapid heat treatment. In this case, the process temperature is 360-390 ° C. The duration of the heat treatment process is 40 minutes to 3 hours. Again, the temperature and time are chosen so that the contact layer does not melt. The heat treatment according to conventional processes is preferably carried out in an inert atmosphere of eg N2 gas or Ar gas. However, the heat treatment step can also be performed in a reducing atmosphere.

[0014]
Examples of n-type III-V compound semiconductors on which ohmic contacts are produced by the method according to the invention are GaAs, Gal-xAlxAs, GaP, InP and

[0015]

When bonding the contact layer with one or more bonding wires made of gold or aluminum, one or more metal layers may be provided on one or more metal layers to prevent contact or damage to the semiconductor crystals during bonding. Therefore, it is necessary to reinforce the contact.

Gold or aluminum is preferably used as the reinforcing layer (bonding pad). The thick gold layer can be formed directly on the AuGeNi contact layer, whereas the bonding pad made of aluminum must be formed on the intermediate layer which acts as a diffusion barrier. The layer of titanium tungsten nitride (TiWN) prevents aluminum from diffusing from the bonding pad into the contact layer. As a side effect, the ohmic contact in the heat treatment step and the alloying with the aluminum reinforcement are prevented.

[0016]

In a preferred embodiment, a semiconductor crystal having a single heterostructure consisting of p-type Ga0.65Al0.35As and n-type Ga0.32Al0.68As is produced on a p-type GaAs substrate by liquid phase epitaxial growth, The charge carrier concentration in the epitaxial layer is 1 × 10

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18 cm −3, and a 100 nm thick AuGeNi layer and a 500 nm thick Au layer are formed on the surface of this crystal. The AuGeNi layer contains 0.4% by weight of germanium and 0.5% by weight of nickel. In another method step, a TiWN diffusion barrier with a thickness of 0.25 μ and another Al reinforcement with a thickness of 2 μ are first deposited on the Au layer. The TiWN layer is sputtered. The contacts are subsequently wet-chemically structured using a photoresist mask. For example, unnecessary portions of the aluminum layer are removed with phosphoric acid, unnecessary portions of the TiWN layer are removed with hydrogen peroxide, and unnecessary portions of the AuGeNi-Au layer are removed with gold etching. After removal of the photoresist mask, the multi-layer contact array is heat treated by a rapid heat treatment process at 480 ° C for 15 seconds. The ohmic contact thus produced has a smooth surface and can be wire bonded without problems. The contact resistance is about 5 × 10 −5 Ωcm 2.

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CLAIMS JPH07263375

1.
A method of making an ohmic contact on an n-type semiconductor layer of a III-V compound semiconductor, comprising first forming a metal contact layer on the n-type semiconductor layer, then forming a gold layer on the metal contact layer, and then forming a gold layer on the metal contact layer. A method of heat-treating the obtained array in a heat treatment step, wherein the metal contact layer is made of AuGeNi, and the germanium content and nickel content of each do not exceed 1% by weight.

2.
The method according to claim 1, characterized in that the layer arrangement is heat-treated at 360-390 ° C. for 40-180 minutes.

3.
Method according to claim 1, characterized in that the layer arrangement is heat-treated at 430-480 ° C for 5-20 seconds.

4.
4. The method according to claim 1, wherein the nickel content in the AuGeNi layer is 0.5% by weight.

5.

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Method according to one of the claims 1 to 4, characterized in that the germanium content in the AuGeNi layer is 0.4% by weight.

6.
Method according to one of the claims 1 to 5, characterized in that the thickness of the AuGeNi layer is in the range 50-200 nm.

7.
Method according to one of the claims 1 to 6, characterized in that the thickness of the gold layer is in the range 250 to 1000 nm.

8.
Method according to one of claims 1 to 7, characterized in that, prior to the heat treatment step, first a TiWN layer and then an aluminum layer is deposited on the metal covering the AuGeNi layer.

9.
The method according to claim 8, wherein the thickness of the TiWN film layer is in the range of 100 to 500 nm.

10.
A method according to claim 8 or 9, characterized in that the thickness of the aluminum layer is in the range of 1 to 3 µm.

11.
10. The method according to claim 1, wherein the contact arrangement is structured before the heat treatment step.

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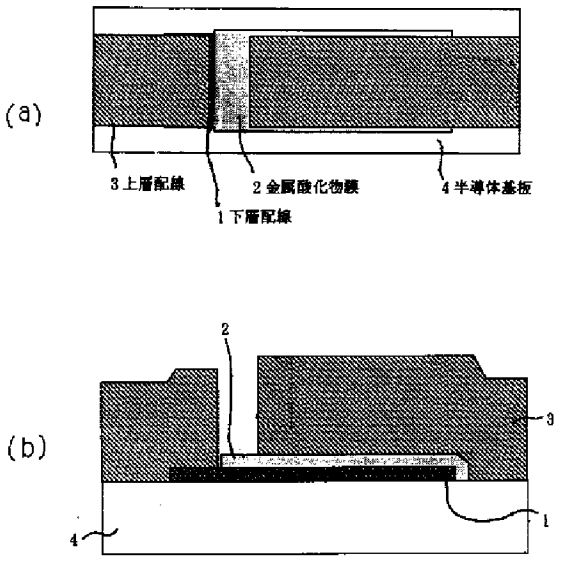
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(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】

【目的】　充分な酸素欠陥を形成して実用的な電流（～ｍＡ）が流せる金属酸化物を利用した、ダイオード並びにキャパシタとして動作する半導体装置を提供することを目的とする。

【構成】　この発明の半導体装置は、半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とする。



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【特許請求の範囲】
【請求項１】　半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とする半導体装置。
【請求項２】　下層配線が、金属酸化物膜と接する上部表面に白金層を有し、上層配線が、金属酸化物膜と接する下部表面にチタン層を有してなる請求項１記載の半導体装置。
【請求項３】　下層配線が、チタン／白金の積層体からなり、上層配線が、チタン／金又はチタン／白金／金の積層体からなる請求項１又は２記載の半導体装置。
【請求項４】　金属酸化物膜が、バリウムチタン酸ストロンチウム（$Ba_xSr_{1-x}TiO_3$ ；$0 \leqq x \leqq 0.7$）である請求項１～３いずれか１つに記載の半導体装置。
【請求項５】　半導体基板と下層配線の間に、窒化シリコン膜又は酸化シリコン膜が挟まれてなる請求項１～４いずれか１つに記載の半導体装置。
【請求項６】　半導体装置が、ダイオードとして使用される請求項１～５いずれか１つに記載の半導体装置。
【請求項７】　下層配線が、上層配線と相対的に一定のＤＣ負バイアスを絶縁を破壊しない範囲で印加してキャパシタとして使用される請求項１～５いずれか１つに記載の半導体装置。
【請求項８】　一定のＤＣ負バイアスが、－０．５Ｖ～－１０Ｖである請求項７記載の半導体装置。
【請求項９】　回路内に、同じ工程で作製した請求項６と請求項７又は８の半導体装置が構成素子として含まれてなることを特徴とする集積回路半導体装置。
【請求項１０】　請求項１～９の金属酸化物膜が、金属酸化物膜を構成する金属のアルコキシドからなる前駆体溶液を下層配線上へ塗布し、次いで焼成を空気中３００℃～５００℃の範囲で行なうことからなる加水分解を利用したゾルゲル法により形成されてなることを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】この発明は、半導体装置及びその製造方法に関する。更に詳しくは、この発明は、金属酸化物を用いた半導体装置及びその製造方法に関する。
【０００２】
【従来の技術】純粋な金属酸化物の場合、３から４ｅＶと大きいバンドギャップを有するので絶縁体としての性質を示す。しかし、酸素欠陥が存在すると、ドナー準位が生じ、ｎ型の半導体導電性を示す。金属酸化物は、上記のように大きいバンドギャップを有するので、電流を流すための適当なキャリアを酸素欠陥によって生じさせれば、高耐圧特性を示すダイオードとしての利用が期待される。
【０００３】金属酸化物をチャネルとして利用する半導体装置として、第１１回強誘電体応用会議講演予稿集ｐ２７－ｐ２８に示されているもの（文献１）が挙げられる。即ち、この文献１では酸化マグネシウム（ＭｇＯ）上にレーザーアブレーション法によって形成したチタン酸ストロンチウム（$SrTiO_3$）をチャネルに用いた薄膜トランジスタにおいて、ニオブ（Ｎｂ）をオーミックメタルとして用い、オーミック形成領域にアルゴン（Ａｒ）イオンの注入を行なって酸素欠陥を作りキャリアを形成している。得られた半導体装置の特性は、ゲート幅２０μｍに対し、１００ｎＡの電流が得られている程度である。
【０００４】また、金属酸化物を用いた半導体装置のうち、金属酸化物の絶縁特性と高誘電率特性を用いた半導体装置としての利用は、例えば、日経マイクロデバイス、ｐ１１１～ｐ１１６、１９９２年1月号（文献２）及び特開平５－２６７５６５号公報（文献３）にも示されている。即ち、文献２では、Ｓｉ基板上にマグネトロンスパッタで形成した$Ba_{0.5}Sr_{0.5}TiO_3$を用い、金属酸化物の高温の熱工程を受ける下側の電極に熱工程による劣化の少ないＰｔ／Ｔａを用い、上側の電極にＴｉＮを用いたＤＲＡＭ用のキャパシタが記載されている。一方、文献３では、誘電体にゾルゲル法で形成した$Ba_{0.7}Sr_{0.3}TiO_3$を用い、その下側の電極にＰｔ／Ｔｉ、上側の電極にＰｔを用いたキャパシタが記載されている。
【０００５】また文献２では、５００℃以上で熱処理を施すと、Ｐｔ／Ｔｉ電極に反応が生じ、信頼性の低下を生じることも報告されている。
【０００６】
【発明が解決しようとする課題】金属酸化物をチャネルとした薄膜トランジスタとして使用している文献１では、電極とコンタクトする部分にＡｒイオン注入を行なって酸素欠陥を形成することによりn^+層を形成しているが、チャネルの$SrTiO_3$には、充分な酸素欠陥、すなわちキャリアが形成されていないので、実用的な電流が流れないと考えられる。
【０００７】また、この文献１のデバイスは、金属電極が金属酸化物膜の両端にある横型構造であり、電流が流れる方向の金属酸化物の距離が長く、電流が流れ難い構造である。実際、この例での金属酸化物膜の通過電流は、ゲート幅２０μｍに対して、１００ｎＡ程度であり、デバイスとして実用的な電流（～ｍＡ）は、得られていない。
【０００８】金属酸化物を高誘電体として用いた半導体装置の従来例、即ち文献２及び３では、キャパシタとして用いる場合、金属酸化物の高誘電率特性を利用するので、リーク電流の存在によって、例えば、ＤＲＡＭのメ

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モリーに蓄積されている電荷が消失し、キャパシタとしての特性を劣化させる。このために、文献２のように、ペロブスカイト型の結晶化を促進するため６５０℃でのスパッタ成膜や、文献３のように７００℃以上の高温の酸素処理等によって結晶化を促進し、金属酸化物のリーク電流を現象させる工夫を行なっている。

【０００９】しかしながら、高温でのスパッタ成膜や、高温の酸素中焼成が必要なために、低温での処理が必要なＳｉやＧａＡｓ等の半導体素子とのプロセス温度の整合が取れない。このために、文献２のように、Ｐｔ／Ｔａを電極に採用したり、ＦＥＴを先に作り込む従来の工程では、ＩＣの多層配線がキャパシタの上下電極として使用できるのにもかかわらず、文献３では、ＦＥＴ作製工程より以前にキャパシタをつくりこむため、キャパシタ用の電極を別工程でつくる必要が生じている。このような電極や工程の大幅な変化は、電極材料への悪影響（信頼性の低下）や、製造コストの大幅な増加をもたらす。

【００１０】このように、従来の技術では、金属酸化物を半導体材料として利用する場合、金属酸化物に充分な酸素欠陥が簡単には形成されず、電流を制御通過できる半導体層としての特性を利用することが困難であり、そのオーミック接触電極の形成においても、あえてＡｒイオンの注入を行ないｎ$^{+}$ 層を形成するなど、工程が複雑になる問題があった。

【００１１】また、金属酸化物を高誘電率の絶縁体として利用する場合、高温処理が必要なため、ＳｉやＧａＡｓ等の半導体基板上に形成する場合、電極や、製造工程の変更が必要になり、信頼性の低下や、製造コストの増加をもたらす問題があった。従って、この発明は、充分な酸素欠陥を形成して実用的な電流（～ｍＡ）が流せる金属酸化物を利用した、ダイオード並びにキャパシタとして動作する半導体装置を提供することを目的とする。

【００１２】

【課題を解決するための手段】かくしてこの発明によれば、半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とする半導体装置が提供される。

【００１３】更に、この発明によれば、上記金属酸化物膜が、金属酸化物膜を構成する金属のアルコキシドからなる前駆体溶液を下層配線上へ塗布し、次いで焼成を空気中３００℃～５００℃の範囲で行なうことからなる加水分解を利用したゾルゲル法により形成されてなることを特徴とする半導体装置の製造方法も提供される。この発明に使用できる半導体基板としては、特に限定されず、シリコン、ＧａＡｓ等が挙げられる。この半導体基板上には下層配線が配設されるが、その前に窒化シリコン、酸化シリコン等の絶縁膜を形成しておいてもよい。絶縁膜を半導体基板上に形成することにより、基板上に形成された他の半導体装置との製造工程の整合性を良好にすることができる。絶縁膜の厚さは、３００～５０００Åである。

【００１４】次に、この発明に使用できる下層配線は、後に説明する金属酸化物膜を構成する金属とショットキィ接触を形成する金属からなる。下層配線に使用できる金属としては、例えば、白金、チタン、タングステン等が挙げられ、このうち、白金が好ましい。下層配線の厚さは５００～２００００Åであり、更に６０００～１００００Åであることが好ましい。ここで、５００Åより小さいと配線が高抵抗化して好ましくなく、２００００Åより大きいと電極エッジの段差が大きくなりすぎるので好ましくない。また、下層配線は必ずしも１層からなる必要はなく、２層以上であってもよい。例えば、２層からなる場合は、チタン／白金、アルミニウム／白金等の積層体が挙げられる。このうち、チタン／白金からなる積層体が半導体基板及び金属酸化物膜との密着力を考慮すると好ましく、厚さはチタン層が５００～１０００Åであり、白金層が５００～２０００Åである。なお、下層配線は金属酸化物膜と接する上部表面に白金層が形成されていることが好ましい。これは、白金層が酸化されにくく、金属酸化物膜とある程度の密着力があるためである。下層配線の形成方法は、特に限定されず、スパッタ法、真空蒸着法等が挙げられ、所望の形状にするためにフォトリソグラフ法により成形してもよい。

【００１５】次に、上記上層配線の上には、酸素欠陥を有する金属酸化物膜が形成される。この発明に使用できる金属酸化物としては、例えば、$Ba_x Sr_{1-x} TiO_3$（$0 \leqq x \leqq 0.7$）、$SrTiO_3$、$BaMgF_4$、$LiNbO_3$、$LiTaO_3$、$CaBi_4 Ti_4 O_{15}$、$KNbO_3$、$NaNbO_3$ 等の高誘電率材料が挙げられる。このうち、$Ba_x Sr_{1-x} TiO_3$（$0 < x \leqq 0.7$、特に$0.5 < x \leqq 0.7$）が好ましい。また、金属酸化物層の厚さは１０００～３０００Åであり、更に２０００～２５００Åであることが好ましい。ここで、１０００Åより小さいと破壊耐圧が著しく小さくなるので好ましくなく、３０００Åより大きいと形成時にストレスによりクラックが生じるので好ましくない。金属酸化物膜の形成方法は、ゾルゲル法が好ましい。この方法は、金属酸化物を構成する金属のアルコキシドからなる前駆体溶液を、例えばスピンコート等により塗布し、３００～５００℃の低温で焼成することにより金属酸化物膜を形成する方法である。焼成温度が３００℃より低い場合、金属酸化物膜の結晶化が十分ではなく、５００℃より高い場合、半導体装置の製造工程自体を変更する必要があり、また新たな配線材料の選択が必要となり、信頼性の低下及び製造コストを増加させるので好ましくない。このような形成条件では完全な結晶状態（ペロブス

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カイト構造）とならないが、比誘電率が２０～３０のものを得ることができる。この値は、ＳｉＮに比べて４～６倍の比誘電率であり、絶縁体を金属で挟んだ構造のＭＩＭ（メタル／絶縁体／メタル）キャパシタ材料として使用することができる。また、金属酸化物膜は、所望の形状にするためにフォトリソグラフ法により成形してもよい。

【００１６】次に、金属酸化物膜の上には上層配線が形成される。この発明に使用できる上層配線は、上記で説明した金属酸化物膜を構成する金属より酸素に対する親和力の大きい金属からなる。上層配線に使用できる金属としては、例えば、チタン、白金、金、アルミニウム等が挙げられ、このうち、チタンが好ましい。上層配線の厚さは５００Å～１０μｍであり、更に２～１０μｍであることが好ましい。ここで、５００Åより小さいと高抵抗化し好ましくなく、１０μｍより大きいと製作が困難なので好ましくない。また、上層配線は必ずしも１層からなる必要はなく、２層以上であってもよい。例えば、２層からなる場合は、チタン／金、白金／金等の積層体が挙げられ、３層からなる場合は、チタン／白金／金、タングステン／白金／金等の積層体が挙げられる。このうち、チタン／金、チタン／白金／金からなる積層体が半導体基板及び金属酸化物膜との密着力を考慮すると好ましく、厚さは２層の場合、チタン層が５００～１０００Åであり、金層が２～１０μｍであり、一方３層の場合、チタン層が５００～１０００Åであり、白金層が１０００～２０００Åであり、金層が２～１０μｍである。なお、上層配線は金属酸化物膜と接する下部表面にチタン層が形成されていることが好ましい。これは、チタン層が金属酸化物膜の表面から酸素を奪うことにより酸化チタンを形成し、金属酸化物膜表面に高濃度の酸素欠乏層を形成し、オーミック接触を形成することができるからである。上層配線の形成方法は、特に限定されず、スパッタ法、真空蒸着法等が挙げられ、所望の形状にするためにフォトリソグラフ法により成形してもよい。

【００１７】この発明の縦型構造を有する半導体装置は、キャパシタ、ダイオード、バイパスコンデンサ等に使用することができる。例えば、下層配線が、上層配線と相対的に一定のＤＣ負バイアスを絶縁を破壊しない範囲で印加することによりキャパシタとして使用することができる。一定のＤＣ負バイアスに固定して、金属酸化物膜を流れる電流を抑制すると、金属酸化物膜は絶縁体としての特性を示し、ロスの小さいキャパシタとして動作する。なお、一定のＤＣ負バイアスは、－０．５～－１０Ｖが好ましい。－１０Ｖより大きいと絶縁が破壊される恐れがあるので好ましくなく、－０．５Ｖより小さいと回路に制約が多いので好ましくない。

【００１８】また、上記では、簡単のため、１つの半導体装置のみを例として説明したが、２つ以上の半導体装置を同時に形成してもよく、他の半導体装置と組み合わせてもよい。

【００１９】

【作用】この発明の半導体装置は、半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とするので、半導体基板上に高耐圧の素子を形成することができ、基板上に形成されたその他の能動素子とともに動作させることができ集積回路の高性能化が図られる。

【００２０】また、下層配線が、金属酸化物膜と接する上部表面に白金層を有し、上層配線が、金属酸化物膜と接する下部表面にチタン層を有してなるので、下部配線と金属酸化物膜間ではショットキィ接触が、上部配線と金属酸化物膜間ではオーミック接触が形成される。また、金属酸化物膜の上下配線の金属を変えることで、縦方向に実用的な電流密度１～１０Ａ／ｃｍ^2 の電流を流すことができる半導体装置が提供される。

【００２１】更に、下層配線が、チタン／白金の積層体からなり、上層配線が、チタン／金又はチタン／白金／金の積層体からなるので、更に特性の良好な半導体装置が得られる。また、金属酸化物が、バリウムチタン酸ストロンチウム（$Ba_x\ Sr_{1-x}\ TiO_3$ ；０≦ｘ≦０．７）であるので、従来のＳｉＮ等の絶縁物を使用したものと比べて比誘電率が向上した半導体装置が得られる。

【００２２】更に、半導体基板と下層配線の間に、窒化シリコン又は酸化シリコンが挟まれてなることにより、半導体基板上の他の半導体装置とのプロセス整合が良好となる。また、半導体装置が、ダイオードとして使用されるので、高耐圧のダイオードが得られる。

【００２３】更に、下層配線が、上層配線と相対的に一定のＤＣ負バイアスを絶縁を破壊しない範囲で印加してキャパシタとして使用するので、金属酸化物膜の絶縁体としての特性が示され、ロスの少ないキャパシタが得られる。また、一定のＤＣ負バイアスが、－０．５Ｖ～－１０Ｖであるので、更にロスの少ないキャパシタが得られる。

【００２４】更に、回路内に、同じ工程で作製したダイオードとキャパシタが構成素子として含まれてなるので、キャパシタとダイオードが同一の工程で形成される。また、金属酸化物膜が、金属酸化物膜を構成する金属のアルコキシドからなる前駆体溶液を下層配線上へ塗布し、次いで焼成を空気中３００℃～５００℃の範囲で行なうことからなる加水分解を利用したゾルゲル法により形成されてなるので、十分な通過電流（１～１０Ａ／ｃｍ^2 ）を奏する酸素欠陥状態が維持される。

【００２５】

【実施例】以下、この発明を実施例をもとに説明する

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が、この発明は実施例に限定されるものではない。

実施例１

図１に示す半導体装置を形成した。なお、図１（ａ）は平面図、（ｂ）は断面図を表す。図１中１は白金からなる下層配線、２はバリウムチタン酸ストロンチウム（$Ba_x Sr_{1-x} TiO_3$，ｘ＝０．５又は０．７）からなる金属酸化物膜、３はチタンからなる上層配線、４はＧａＡｓからなる絶縁性半導体基板を示している。

【００２６】まず、絶縁性半導体基板４上にレジストをスピンコート法により塗布し、フォトリソグラフィ法によりレジストに１１０μｍ×１５０μｍの矩形のスペースパターンを形成した。この基板４上にチタンをスパッタ法により厚さ２５００Åで堆積し、リフトオフにより１１０μｍ×１５０μｍの矩形の下層配線１のパターンを形成した。

【００２７】次に、この基板４上に後にバリウムチタン酸ストロンチウム（$Ba_x Sr_{1-x} TiO_3$ ｘ＝０．５又は０．７）となる金属アルコキシドからなる前駆体溶液を、スピンコート法により厚さ２０００Åに塗布した。この後、空気中で１５０℃、１５分間乾燥させ、続いて空気中で５００℃、１時間の焼成を行い金属酸化物膜２を形成した。次いで、金属酸化物膜２上にレジストをスピンコート法により塗布し、エッチングにより下層配線１を一部露出させ、コンタクト用のホールを形成すると共に、不要な部分の金属酸化物膜を取り去った。なお、エッチャントは５％バッファーフッ酸：塩酸：純水（１：１：２）溶液とし、この溶液に１５秒浸すことによりエッチングを行った。

【００２８】次に、上記基板４上にレジストをスピンコート法により塗布し、フォトリソグラフィ法によりレジストにスペースパターンを形成した。この基板４上に白金をスパッタ法により厚さ２μｍで堆積し、リフトオフにより上層配線３のパターンを形成することにより図１に示す如き半導体装置を形成した。なお、下層配線１と上層配線３が金属酸化物膜２を介して接している面積は１００μｍ×１００μｍであった。

【００２９】実施例２

図５に示す半導体装置を図２～４に基づいて形成した。なお、図２～５において（ａ）は平面図、図２（ｂ）は断面図を示している。図２～５中１～４は図１と同じであり、５はチタン層、６は白金層、７は金層、８はＳｉＮからなる絶縁膜を示している。

【００３０】まず、絶縁性半導体基板４上にＳｉＮからなる絶縁膜８を厚さ２０００ÅでＰＣＶＤ法により形成した。次に、実施例１と同様にして、１１０μｍ×１５０μｍのレジストからなる矩形のスペースパターンを形成し、スパッタ法によりチタン層５を５００Å、白金層６を２０００Åこの順で堆積し、リフトオフにより１１０μｍ×１５０μｍの矩形の下層配線１のパターンを形成した（図２（ａ）及び（ｂ）参照）。

【００３１】次に、実施例１と同様にして、金属酸化物膜２を下層配線１上に形成した。なお、ｘは０．７とした（図３（ａ）及び（ｂ）参照）。次に、実施例１と同様にして、レジストからなるパターンを形成し、スパッタ法によりチタン層５を５００Å、金層７を２μｍこの順で堆積し、リフトオフにより上層配線３のパターンを形成した（図４（ａ）及び（ｂ）参照）。

【００３２】この後レジストを取り除くことにより、図５に示す如き半導体装置を得た。なお、下層配線１と上層配線３が金属酸化物膜２を介して接している面積は１００μｍ×１００μｍであった。図６は、図５の構成において、焼成を５００℃で１時間行なった厚み２０００Åの$Ba_{0.7} Sr_{0.3} TiO_3$を金属酸化物膜２に用いた半導体装置の下層配線１に与える電圧と、下層配線から上層配線３に半導体装置を流れる電流の関係を示すグラフである。

【００３３】図６から明らかなように、下層配線に－１０Ｖ印加しても、電流はほとんど流れず、良好なダイオード特性を示している。また、下層配線に、－１０Ｖ以下の範囲で長時間電圧を印加した場合、高誘電体に流れる電流が増加し、絶縁破壊に到った。

実施例３

図７に示す半導体装置を、上層配線３の形成において、チタン層５と金層７の間に厚さ１００Åの白金層６を形成すること、絶縁膜８をSiO_2にすること以外は、実施例２と同様の工程を繰り返すことにより形成した。

【００３４】図８は、図７の構成において、焼成を３００℃で１時間行なった厚み２０００Åの$Ba_{0.5} Sr_{0.5} TiO_3$を金属酸化物膜２に用いた半導体装置の、下層配線１に与える電圧と、下層配線１から上層配線３に半導体装置を流れる規格化電流の関係を示す。図８では、上層配線３の寸法を、２０μｍ×１０μｍ～２００μｍ×２００μｍまで、変化させている。

【００３５】図８から明らかなように、順方向電流は、上層配線３の面積に依存していることが判る。また、－８～－１０Ｖまで下層電極にＤＣバイアスを印加しても、ほとんど逆方向電流は流れず、＋２～３ＶのＤＣバイアスを印加すると、実用レベルの順方向電流（約１Ａ／cm^2）が流れる。このことは、この発明によって得られる半導体装置が、逆耐圧の高いダイオードとして動作することを示している。更に、下層電極に印加されるＤＣバイアスを－２Ｖに固定すると、電流が10^{-6}～10^{-4}Ａ／cm^2に抑制され、良好なリーク特性を示す。

【００３６】実施例４

図９は、この発明の半導体装置を、キャパシタとして用いる際の回路構成の一例を示す。なお、図９中Ａは、下層配線１、金属酸化物膜２及び上層配線３からなるこの発明の半導体装置である。下層配線１に、－５Ｖ印加した際の１～１５ＧＨｚの比誘電率は、$Ba_{0.7} Sr_{0.3} TiO_3$の場合が３０、$Ba_{0.5} Sr_{0.5} TiO_3$の場

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合が２５、$SrTiO_3$ の場合が２０であった。これら高誘電体金属酸化物で本来得られる比誘電率（１００～３００）は得られていないが、ＳｉＮが５．６，SiO_2 が4であることに比べると、これらの金属酸化物で作ったキャパシタは、４～7倍の容量を示すことが判った。従って、同じ厚みのＳｉＮやSiO_2 を使う場合、キャパシタ面積を１／４～１／７に縮小することが可能である。

【００３７】実施例５

図１０は、この発明の半導体装置を同一基板上でダイオード及びキャパシタとして使用する場合の回路構成の一例を示している。同じデバイス構造でも、キャパシタとダイオードを一度に作りこむことが可能で、プロセスの簡略化が可能になる。

【００３８】

【発明の効果】この発明の半導体装置は、半導体基板上に、金属酸化物とショットキィ接触を形成する金属により構成された任意の形状の下層配線と、酸素欠陥を有する金属酸化物膜を挟んで、酸素との親和力が該金属酸化物膜に含まれる金属より大きい金属より構成される任意の形状の上層配線をもつ縦型構造を特徴とするので、半導体基板上に高耐圧の素子を形成することができ、基板上に形成されたその他の能動素子とともに動作させることができ集積回路の高性能化を図ることができる。

【００３９】また、下層配線が、金属酸化物膜と接する上部表面に白金層を有し、上層配線が、金属酸化物膜と接する下部表面にチタン層を有してなるので、下部配線と金属酸化物膜間ではショットキィ接触を、上部配線と金属酸化物膜間ではオーミック接触を形成することができる。また、金属酸化物膜の上下配線の金属を変えることで、縦方向に実用的な電流密度１～１０Ａ／cm^2 の電流を流すことができる半導体装置を提供できる。

【００４０】更に、下層配線が、チタン／白金の積層体からなり、上層配線が、チタン／金又はチタン／白金／金の積層体からなるので、更に特性の良好な半導体装置を得ることができる。また、金属酸化物が、バリウムチタン酸ストロンチウム（$Ba_x\ Sr_{1-x}\ TiO_3$ ；０≦ｘ≦０．７）であるので、従来のＳｉＮ等の絶縁物を使用したものと比べて比誘電率が向上した半導体装置を得ることができる。

【００４１】更に、半導体基板と下層配線の間に、窒化シリコン又は酸化シリコンが挟まれてなることにより、半導体基板上の他の半導体装置とのプロセス整合が良好となる。また、半導体装置が、ダイオードとして使用されるので、高耐圧のダイオードが得られる。

【００４２】更に、下層配線が、上層配線と相対的に一定のＤＣ負バイアスを絶縁を破壊しない範囲で印加してキャパシタとして使用するので、金属酸化物膜の絶縁体としての特性が示され、ロスの少ないキャパシタを得ることができる。また、一定のＤＣ負バイアスが、－０．５Ｖ～－１０Ｖであるので、更にロスの少ないキャパシタを得ることができる。

【００４３】更に、回路内に、同じ工程で作製したダイオードとキャパシタが構成素子として含まれてなるので、キャパシタとダイオードが同一の工程で形成することができる。また、金属酸化物膜が、金属酸化物膜を構成する金属のアルコキシドからなる前駆体溶液を下層配線上へ塗布し、次いで焼成を空気中３００℃～５００℃の範囲で行なうことからなる加水分解を利用したゾルゲル法により形成されてなるので、十分な通過電流（１～１０Ａ／cm^2 ）を奏する酸素欠陥状態を維持することができる。また、焼成を低温で行うことができるので、半導体基板上に形成される他の半導体装置の製造工程を大幅に変更することはなく、信頼性の低下を生じさせる電極材料の選択も不要である。従って、信頼性の低下の問題や、製造コストは増加しない。

【図面の簡単な説明】

【図１】この発明の半導体装置の概略平面図及び断面図である。

【図２】この発明の半導体装置の製造工程の概略平面図及び断面図である。

【図３】この発明の半導体装置の製造工程の概略平面図及び断面図である。

【図４】この発明の半導体装置の製造工程の概略平面図及び断面図である。

【図５】この発明の半導体装置の概略平面図及び断面図である。

【図６】この発明の半導体装置の電流と下層配線への印加電圧との関係を示すグラフである。

【図７】この発明の半導体装置の概略平面図及び断面図である。

【図８】この発明の半導体装置の電流と下層配線への印加電圧との関係を示すグラフである。

【図９】この発明の半導体装置をキャパシタとして使用した場合の回路構成図である。

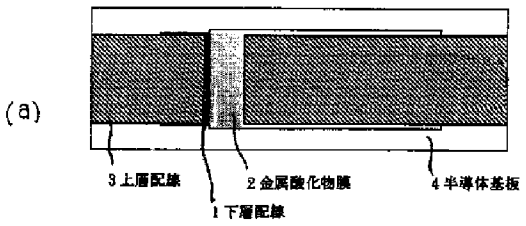
【図１０】この発明の半導体装置を同一基板上でダイオード及びキャパシタとして使用した場合の回路構成図である。

【符号の説明】

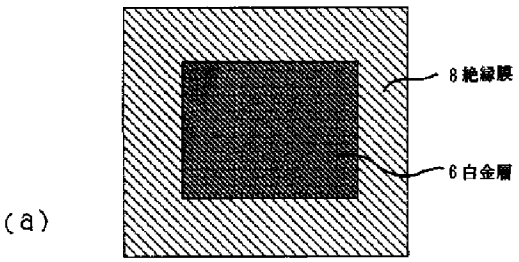
１　下層配線
２　金属酸化物膜
３　上層配線
４　半導体基板
５　チタン層
６　白金層
７　金層
８　絶縁膜
Ａ　半導体装置

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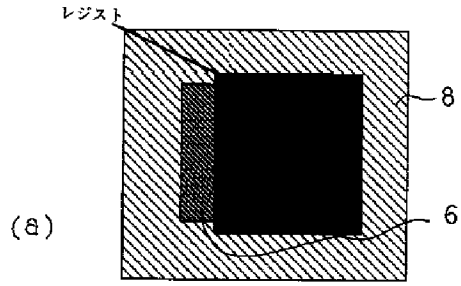
【図1】



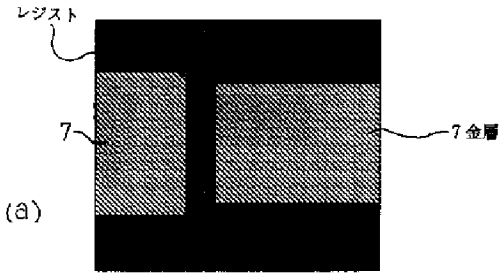
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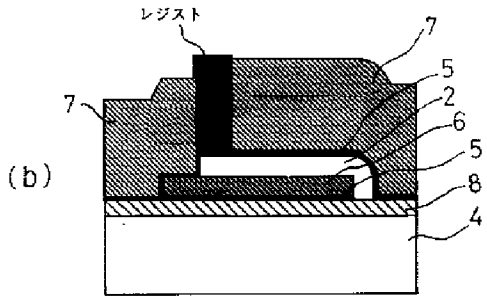


【図3】



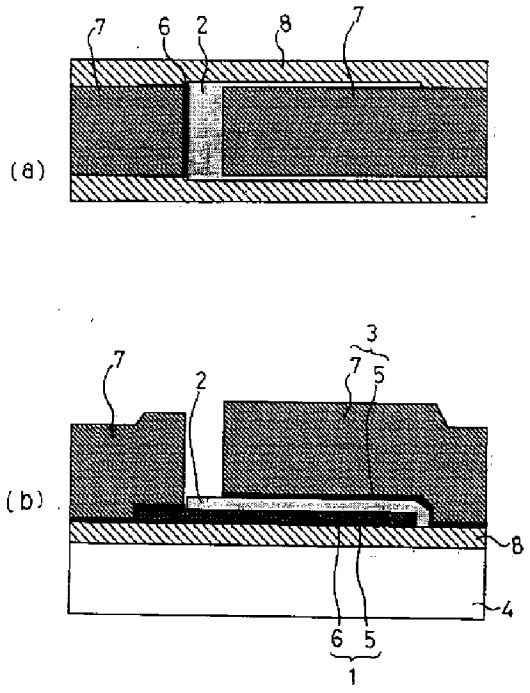
【図4】



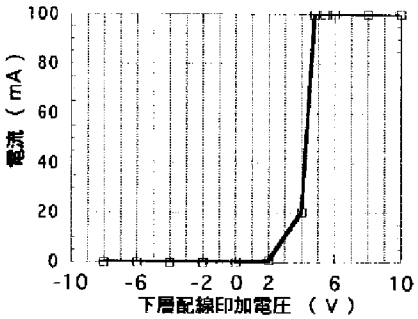


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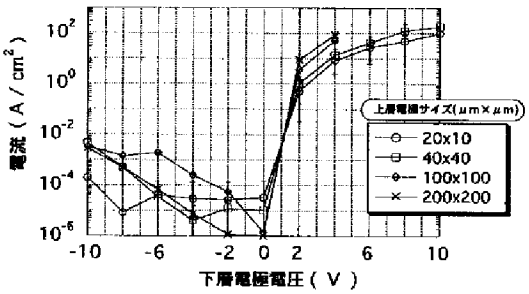
【図5】



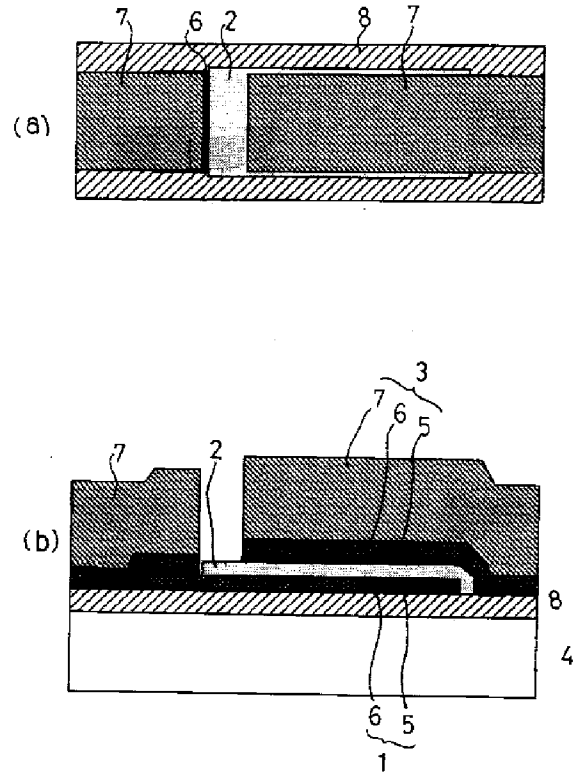
【図6】



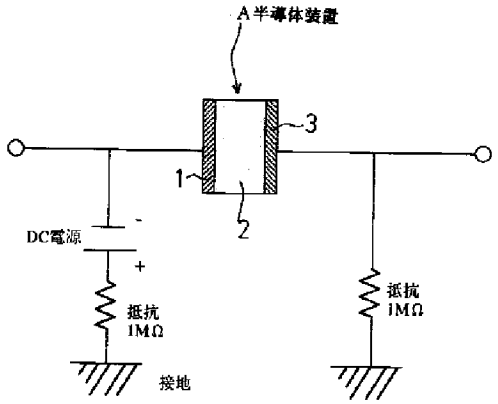
【図8】



【図7】

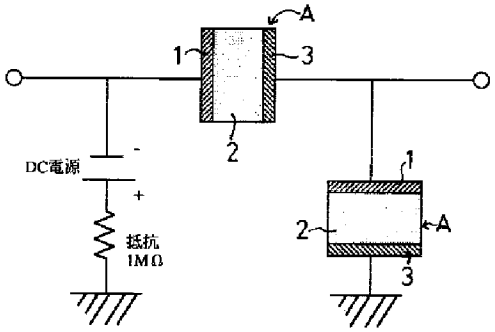


【図9】



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【図１０】



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JPH08167693A SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

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Classifications:
IPC ***H01L21/822; H01L27/04; H01L29/861;*** (IPC1-7): H01L21/822; H01L27/04; H01L29/861;

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SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Abstract

PURPOSE: To raise the performance of an integrated circuit by forming a vertical structure which has lower-layer wiring and upper-layer wiring in an optional shape consisting of each specified metal, on a semiconductor substrate. CONSTITUTION: A vertical structure, which has lower-layer wiring 1 in an optional shape consisting of metal to form Schottky contact with a metallic oxide and upper-layer wiring 3 in optional shape consisting of metal whose affinity with oxygen is larger than that of the metal contained in a metallic oxide film 2, with a metallic oxide film 2 having oxygen defect between, is made on a semiconductor substrate 4. The metallic oxide film 2 is made by sol gel method making use of the hydrolysis by applying precursor solution consisting of alkoxide of metal constituting the metallic oxide film 2 on the lower-layer wiring 1, and baking it in the range of 300 deg.C-500 deg.C in air. Hereby, a high breakdown strength element can be made on the semiconductor substrate 4, and it can be operated together with other active elements made on the substrate 4, so that an integrated circuit can enhance performance.

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DESCRIPTION JPH08167693

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device and its manufacturing method. More specifically, the present invention relates to a semiconductor device using a metal oxide and a method for manufacturing the same.

[0002]

2. Description of the Related Art In the case of a pure metal oxide, it has a large band gap of 3 to 4 eV and thus exhibits a property as an insulator. However, in the presence of oxygen defects, a donor level is generated, and n-type semiconductor conductivity is exhibited. Since the metal oxide has a large band gap as described above, it is expected to be used as a diode exhibiting a high withstand voltage characteristic if oxygen carriers generate suitable carriers for passing a current.

[0003]

As a semiconductor device using a metal oxide as a channel, the one shown in Proceedings of the 11th Ferroelectric Application Conference p27-p28 (Reference 1) can be mentioned. That is, in Document 1, in a thin film transistor using strontium titanate (SrTiO3) formed on a magnesium oxide (MgO) by a laser ablation method as a channel, niobium (Nb) is used as an ohmic metal and argon (Ar) is formed in an ohmic formation region.) Ions are implanted to create oxygen defects

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and form carriers. The characteristics of the obtained semiconductor device are such that a current of 100 nA is obtained for a gate width of 20 μm.

[0004]

Further, among semiconductor devices using metal oxides, the use as a semiconductor device using the insulating properties and high dielectric constant properties of metal oxides is described in, for example, Nikkei Microdevice, p111 to p116, January 1992 issue (Reference 2) and Japanese Patent Laid-Open No. 267565/1993 (Reference 3). That is, in Reference 2, Ba0.5 Sr0.5 TiO3 formed by magnetron sputtering on a Si substrate is used, and Pt / Ta, which is less deteriorated by the thermal process, is used for the lower electrode which is subjected to the high temperature thermal process of the metal oxide. A capacitor for DRAM using TiN for the upper electrode is described. On the other hand, Document 3 describes a capacitor in which Ba0.7Sr0.3TiO3 formed by a sol-gel method is used as a dielectric, Pt / Ti is used as the lower electrode and Pt is used as the upper electrode.

[0005]
Further, in Document 2, it is also reported that when heat treatment is performed at 500 ° C. or higher, a reaction occurs in the Pt / Ti electrode and reliability is lowered.

[0006]
In Reference 1, which is used as a thin film transistor using a metal oxide as a channel, Ar ion implantation is performed in a portion in contact with an electrode to form an oxygen defect, thereby forming an n + layer. However, since sufficient oxygen defects, that is, carriers are not formed in the SrTiO3 of the channel, it is considered that a practical current does not flow.

[0007]

Further, the device of Document 1 has a horizontal structure in which metal electrodes are provided at both ends of the metal oxide film, and the distance of the metal oxide in the direction in which the current flows is long, so that the current hardly flows.

In fact, the current passing through the metal oxide film in this example is about 100 nA for a gate width of 20 μm, and a practical current (mA) as a device has not been obtained.

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[0008]

In a conventional example of a semiconductor device using a metal oxide as a high dielectric, that is, in Documents 2 and 3, the high dielectric constant characteristic of the metal oxide is used when used as a capacitor. The electric charge accumulated in the memory disappears, and the characteristics as a capacitor are deteriorated.

For this reason, as in Reference 2, the crystallization is promoted by sputter film formation at 650 ° C. in order to promote crystallization of the perovskite type or by oxygen treatment at a temperature of 700 ° C. or higher as in Reference 3. , We are making efforts to make the leakage current of metal oxides a phenomenon.

[0009]

However, since the sputtering film formation at a high temperature and the baking in oxygen at a high temperature are required, the process temperature cannot be matched with that of a semiconductor element such as Si or GaAs that needs a low temperature treatment. Therefore, as in Reference 2, in the conventional process of adopting Pt / Ta for the electrode or forming the FET first, the multilayer wiring of the IC can be used as the upper and lower electrodes of the capacitor. In No. 3, since the capacitor is formed before the FET manufacturing process, it is necessary to form the capacitor electrode in another process. Such a drastic change in the electrode and the process causes an adverse effect on the electrode material (reduction in reliability) and a drastic increase in manufacturing cost.

[0010]

As described above, in the conventional technique, when a metal oxide is used as a semiconductor material, sufficient oxygen defects are not easily formed in the metal oxide, and the characteristics of the semiconductor layer that can control and pass an electric current are used. However, in forming the ohmic contact electrode, there is a problem that the process is complicated, such as intentionally implanting Ar ions to form an n + layer.

[0011]

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Further, when using a metal oxide as an insulator having a high dielectric constant, high temperature treatment is required. Therefore, when it is formed on a semiconductor substrate such as Si or GaAs, it is necessary to change an electrode or a manufacturing process. However, there is a problem that the productivity is lowered and the manufacturing cost is increased.

Therefore, an object of the present invention is to provide a semiconductor device that operates as a diode and a capacitor, which uses a metal oxide capable of forming a sufficient oxygen defect and allowing a practical current (-mA) to flow.

[0012]
Thus, according to the present invention, an underlayer wiring of any shape made of a metal forming a Schottky contact with a metal oxide and a metal oxide having an oxygen defect are formed on a semiconductor substrate. Provided is a semiconductor device characterized by a vertical structure having an upper layer wiring of any shape made of a metal having an affinity for oxygen higher than that of a metal contained in the metal oxide film with a physical film sandwiched therebetween.

[0013]

Further, according to the present invention, the metal oxide film is formed by applying a precursor solution composed of an alkoxide of a metal forming the metal oxide film onto the lower layer wiring, and then baking the same in air at 300 ° C to 500 ° C. Also provided is a method for manufacturing a semiconductor device, which is formed by a sol-gel method utilizing hydrolysis, which is performed in the range of

The semiconductor substrate that can be used in the present invention is not particularly limited, and examples thereof include silicon and GaAs. The lower layer wiring is provided on this semiconductor substrate, but an insulating film of silicon nitride, silicon oxide or the like may be formed before that. By forming the insulating film on the semiconductor substrate, it is possible to improve the compatibility of the manufacturing process with other semiconductor devices formed on the substrate. The thickness of the insulating film is 300 to 5000 Å.

[0014]

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Next, the lower layer wiring that can be used in the present invention is made of a metal forming a metal oxide film, which will be described later, and a metal forming a Schottky contact. Examples of the metal that can be used for the lower layer wiring include platinum, titanium, and tungsten. Of these, platinum is preferable. The thickness of the lower layer wiring is 500 to 20000 Å, preferably 6000 to 10000 Å. Here, if it is less than 500 Å, the wiring becomes high in resistance, which is not preferable, and if it is more than 20000 Å, the step difference of the electrode edge becomes too large, which is not preferable. Further, the lower layer wiring does not necessarily have to be composed of one layer and may be composed of two or more layers. For example, when it is composed of two layers, a laminate of titanium / platinum, aluminum / platinum, etc. may be mentioned. Of these, a laminate of titanium / platinum is preferable in consideration of the adhesion to the semiconductor substrate and the metal oxide film, and the titanium layer has a thickness of 500 to 1000 Å and the platinum layer has a thickness of 500 to 2000 Å. The lower wiring preferably has a platinum layer formed on the upper surface in contact with the metal oxide film. This is because the platinum layer is not easily oxidized and has a certain degree of adhesion to the metal oxide film. The method for forming the lower layer wiring is not particularly limited, and examples thereof include a sputtering method and a vacuum vapor deposition method, and the lower layer wiring may be formed by a photolithographic method in order to obtain a desired shape.

[0015]

Next, a metal oxide film having oxygen defects is formed on the upper wiring. Examples of the metal oxide usable in the present invention include high dielectric constant materials such as Bax Sr1-x TiO3 (0 x 0.7), SrTiO3, BaMgF4, LiNbO3, LiTaO3, CaBi4 Ti4 O15, KNbO3, and NaNbO3. Can be mentioned. Of these, Bax Sr1-x TiO3 (0 <x 0.7, particularly 0.5 <x 0.7) is preferable. Further, the thickness of the metal oxide layer is 1000 to 3000 Å, and preferably 2000 to 2500 Å. Here, if it is less than 1000 Å, the breakdown voltage is remarkably reduced, and if it is more than 3000 Å, cracks are generated due to stress during formation, which is not preferable. The method of forming the metal oxide film is preferably the sol-gel method. This method is a method of forming a metal oxide film by applying a precursor solution composed of a metal alkoxide constituting a metal oxide by, for example, spin coating and baking at a low temperature of 300 to 500 ° C. . If the firing temperature is lower than 300 ° C, the crystallization of the metal oxide film is not sufficient, and if it is higher than 500 ° C, the manufacturing process of the semiconductor device itself needs to be changed, and a new wiring material needs to be selected. It is not preferable because it becomes necessary and the reliability is lowered and the manufacturing cost is increased. Under such forming conditions, a perfect crystalline state (perovskite structure) is not obtained, but a dielectric constant of 20 to 30 can be obtained. This value is 4 to 6 times as high as that of SiN and can be used as an MIM (metal / insulator / metal)

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capacitor material having a structure in which an insulator is sandwiched between metals. Further, the metal oxide film may be formed by a photolithography method so as to have a desired shape.

[0016]

Next, an upper wiring is formed on the metal oxide film. The upper layer wiring that can be used in the present invention is made of a metal having a greater affinity for oxygen than the metal forming the metal oxide film described above. Examples of the metal that can be used for the upper layer wiring include titanium, platinum, gold, aluminum and the like, and among these, titanium is preferable. The upper wiring has a thickness of 500 Å to 10 μm, and preferably 2 to 10 μm. Here, if it is less than 500 Å, the resistance becomes high, which is not preferable, and if it is more than 10 μm, it is difficult to manufacture. Further, the upper layer wiring does not necessarily have to be composed of one layer and may be composed of two or more layers. For example, in the case of two layers, a laminate of titanium / gold, platinum / gold, etc. may be mentioned, and in the case of three layers, a laminate of titanium / platinum / gold, tungsten / platinum / gold, etc. may be mentioned. Of these, a laminate of titanium / gold and titanium / platinum / gold is preferable in consideration of the adhesiveness to the semiconductor substrate and the metal oxide film, and when the thickness is two layers, the titanium layer has a thickness of 500 to 1000 Å, The gold layer is 2-10 μm, while in the case of three layers the titanium layer is 500-1000 Å, the platinum layer is 1000-2000 Å and the gold layer is 2-10 μm. The upper wiring preferably has a titanium layer formed on the lower surface in contact with the metal oxide film. This is because the titanium layer can form titanium oxide by depriving the surface of the metal oxide film of oxygen, form a high-concentration oxygen-deficient layer on the surface of the metal oxide film, and form ohmic contact. is there. The method for forming the upper layer wiring is not particularly limited, and examples thereof include a sputtering method, a vacuum vapor deposition method, and the like, and the upper layer wiring may be formed by a photolithography method in order to obtain a desired shape.

[0017]

The semiconductor device having the vertical structure of the present invention can be used for capacitors, diodes, bypass capacitors, and the like. For example, the lower layer wiring can be used as a capacitor by applying a constant DC negative bias relative to the upper layer wiring within a range that does not destroy the insulation. When the current flowing through the metal oxide film is suppressed by fixing it to a constant DC negative bias, the metal oxide film exhibits characteristics as an insulator and operates as a capacitor with low loss. The constant DC

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negative bias is preferably -0.5 to -10V. If it is higher than -10V, the insulation may be broken, which is not preferable, and if it is lower than -0.5V, there are many restrictions on the circuit, which is not preferable.

[0018]

Further, in the above description, only one semiconductor device is described as an example for simplicity, but two or more semiconductor devices may be formed at the same time or may be combined with another semiconductor device.

[0019]

According to the semiconductor device of the present invention, a lower layer wiring of any shape made of a metal forming a Schottky contact with a metal oxide and a metal oxide film having an oxygen defect are sandwiched on a semiconductor substrate. Since a vertical structure having an upper wiring of arbitrary shape made of a metal having an affinity for oxygen higher than that of the metal contained in the metal oxide film is formed, a high breakdown voltage element can be formed on a semiconductor substrate. Therefore, it can be operated together with other active elements formed on the substrate, and high performance of the integrated circuit can be achieved.

[0020]

In addition, since the lower wiring has a platinum layer on the upper surface in contact with the metal oxide film and the upper wiring has a titanium layer on the lower surface in contact with the metal oxide film, the lower wiring and the metal oxide film are Schottky contact is formed between the upper wiring and the metal oxide film, and ohmic contact is formed between the upper wiring and the metal oxide film.

Further, by changing the metal of the upper and lower wirings of the metal oxide film, a semiconductor device capable of passing a current having a practical current density of 1 to 10 A / cm @ 2 in the vertical direction is provided.

[0021]

Furthermore, since the lower layer wiring is made of a titanium / platinum laminated body and

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the upper layer wiring is made of a titanium / gold or titanium / platinum / gold laminated body, a semiconductor device having further excellent characteristics can be obtained.

Further, since the metal oxide is barium strontium titanate (Bax Sr1-x TiO3; $0 \leqq x \leqq 0.7$), the relative dielectric constant is improved as compared with the conventional one using an insulator such as SiN. A semiconductor device can be obtained.

[0022]

Further, since silicon nitride or silicon oxide is sandwiched between the semiconductor substrate and the lower layer wiring, the process matching with other semiconductor devices on the semiconductor substrate becomes good. Further, since the semiconductor device is used as a diode, a high breakdown voltage diode can be obtained.

[0023]

Further, since the lower layer wiring applies a DC negative bias, which is relatively constant to the upper layer wiring, within a range where the insulation is not destroyed, and is used as a capacitor, the characteristics of the metal oxide film as an insulator are exhibited and the loss is small. A capacitor is obtained. Further, since the constant DC negative bias is -0.5V to -10V, a capacitor with less loss can be obtained.

[0024]

Furthermore, since the diode and the capacitor manufactured in the same process are included in the circuit as constituent elements, the capacitor and the diode are formed in the same process. In addition, the metal oxide film is formed by applying a precursor solution composed of a metal alkoxide constituting the metal oxide film onto the lower layer wiring, and then performing firing in air in the range of 300 ° C to 500 ° C. Since it is formed by a sol-gel method utilizing hydrolysis, an oxygen deficiency state that provides a sufficient passing current (1 to 10 A / cm2) is maintained.

[0025]

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EXAMPLES The present invention will be described below based on examples, but the present invention is not limited to the examples. The semiconductor device shown in FIG. 1 was formed. 1A is a plan view and FIG. 1B is a sectional view. In FIG. 1, 1 is a lower layer wiring made of platinum, 2 is a metal oxide film made of barium strontium titanate (Bax Sr1-x TiO3, x = 0.5 or 0.7), 3 is an upper layer wiring made of titanium, 4 Indicates an insulating semiconductor substrate made of GaAs.

[0026]

First, a resist was applied on the insulating semiconductor substrate 4 by spin coating, and a 110 μm × 150 μm rectangular space pattern was formed on the resist by photolithography. Titanium was deposited to a thickness of 2500 Å on the substrate 4 by a sputtering method, and a pattern of a rectangular lower layer wiring 1 of 110 μm × 150 μm was formed by lift-off.

[0027]

Next, a precursor solution of a metal alkoxide which later becomes barium strontium titanate (Bax Sr1-x TiO3 x = 0.5 or 0.7) was applied on the substrate 4 by a spin coating method to a thickness of 2000 Å. Then, it was dried in air at 150 ° C. for 15 minutes, and subsequently baked in air at 500 ° C. for 1 hour to form a metal oxide film 2. Next, a resist was applied onto the metal oxide film 2 by a spin coating method, a part of the lower wiring 1 was exposed by etching, a hole for contact was formed, and an unnecessary portion of the metal oxide film was removed. The etchant was a 5% buffer hydrofluoric acid: hydrochloric acid: pure water (1: 1: 2) solution, and etching was performed by immersing the solution in this solution for 15 seconds.

[0028]

Next, a resist was applied on the substrate 4 by spin coating, and a space pattern was formed on the resist by photolithography. Platinum was deposited on the substrate 4 to a thickness of 2 μm by a sputtering method, and a pattern of the upper wiring 3 was formed by lift-off to form a semiconductor device as shown in FIG. The area where the lower layer wiring 1 and the upper layer wiring 3 were in contact with each other through the metal oxide film 2 was 100 μm × 100 μm.

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[0029]

Example 2 The semiconductor device shown in FIG. 5 was formed based on FIGS. 2 to 5, (a) is a plan view and FIG. 2 (b) is a sectional view. 2 to 5, 1 to 4 are the same as those in FIG. 1, 5 is a titanium layer, 6 is a platinum layer, 7 is a gold layer, and 8 is an insulating film made of SiN.

[0030]

First, the insulating film 8 made of SiN was formed on the insulating semiconductor substrate 4 to a thickness of 2000 Å by the PCVD method. Next, in the same manner as in Example 1, a rectangular space pattern made of a resist having a size of 110 μm × 150 μm was formed, a titanium layer 5 was deposited in a thickness of 500 Å and a platinum layer 6 was deposited in a thickness of 2000 Å in this order, and 110 μm × was lifted off. A 150 μm rectangular lower layer wiring 1 pattern was formed (see FIGS. 2A and 2B).

[0031]

Next, in the same manner as in Example 1, the metal oxide film 2 was formed on the lower layer wiring 1. Note that x was 0.7 (see FIGS. 3A and 3B). Then, in the same manner as in Example 1, a resist pattern was formed, a titanium layer 5 of 500 Å and a gold layer 7 of 2 μm were deposited in this order by a sputtering method, and a pattern of the upper wiring 3 was formed by lift-off (See FIGS. 4 (a) and 4 (b)).

[0032]

After that, the resist was removed to obtain a semiconductor device as shown in FIG. The area where the lower layer wiring 1 and the upper layer wiring 3 were in contact with each other through the metal oxide film 2 was 100 μm × 100 μm. FIG. 6 shows a voltage applied to the lower wiring 1 of the semiconductor device using Ba0.7Sr0.3TiO3 having a thickness of 2000 Å which is obtained by firing at 500 ° C. for 1 hour in the structure of FIG. 6 is a graph showing the relationship between the current flowing through the semiconductor device from the lower layer wiring to the upper layer wiring 3.

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[0033]

As is clear from FIG. 6, even if −10 V is applied to the lower layer wiring, almost no current flows and good diode characteristics are shown. Further, when a voltage was applied to the lower layer wiring for a long time within the range of −10 V or less, the current flowing through the high dielectric material increased, resulting in dielectric breakdown. The semiconductor device shown in FIG. 7 is the same as the semiconductor device shown in FIG. 7 except that the platinum layer 6 having a thickness of 100 Å is formed between the titanium layer 5 and the gold layer 7 and the insulating film 8 is SiO 2 in the formation of the upper wiring 3. It was formed by repeating the same process as in 2.

[0034]

FIG. 8 shows the voltage applied to the lower layer wiring 1 of the semiconductor device in which Ba 0.5 Sr 0.5 TiO 3 having a thickness of 2000 Å, which was fired at 300 ° C. for 1 hour in the structure of FIG. 7, was used for the metal oxide film 2. , The relationship of the standardized current flowing through the semiconductor device from the lower layer wiring 1 to the upper layer wiring 3 is shown. In FIG. 8, the size of the upper layer wiring 3 is changed from 20 μm × 10 μm to 200 μm × 200 μm.

[0035]

As is clear from FIG. 8, the forward current depends on the area of the upper layer wiring 3. Further, even if a DC bias is applied to the lower layer electrode from -8 to -10V, almost no reverse current flows. When a DC bias of +2 to 3V is applied, a practical level forward current (about 1A / cm2) is obtained. Flowing. This indicates that the semiconductor device obtained by the present invention operates as a diode having a high reverse breakdown voltage. Further, when the DC bias applied to the lower layer electrode is fixed at -2 V, the current is suppressed to 10 -6 to 10 -4 A / cm 2 and good leak characteristics are exhibited.

[0036]

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Fourth Embodiment FIG. 9 shows an example of a circuit configuration when the semiconductor device of the present invention is used as a capacitor. In addition, A in FIG. 9 is a semiconductor device of the present invention including a lower layer wiring 1, a metal oxide film 2, and an upper layer wiring 3. The relative dielectric constant of 1 to 15 GHz when -5 V is applied to the lower layer wiring 1 is 30 in the case of Ba0.7 Sr0.3 TiO3, 25 in the case of Ba0.5 Sr0.5 TiO3, and 20 in the case of SrTiO3. there were. Although the relative permittivity (100 to 300) originally obtained by these high dielectric metal oxides has not been obtained, compared with the fact that SiN is 5.6 and SiO2 is 4, it is made of these metal oxides. It has been found that the capacitor exhibits a capacity of 4 to 7 times. Therefore, when SiN or SiO2 having the same thickness is used, the capacitor area can be reduced to 1/4 to 1/7.

[0037]

Fifth Embodiment FIG. 10 shows an example of a circuit configuration when the semiconductor device of the present invention is used as a diode and a capacitor on the same substrate. Even with the same device structure, it is possible to build capacitors and diodes at the same time, which simplifies the process.

[0038]

According to the semiconductor device of the present invention, a lower layer wiring of any shape made of a metal forming a Schottky contact with a metal oxide and a metal oxide film having an oxygen defect are sandwiched on a semiconductor substrate. In addition, since the vertical structure having an upper wiring of arbitrary shape made of a metal having an affinity with oxygen larger than that of the metal contained in the metal oxide film is formed, a high breakdown voltage element is formed on the semiconductor substrate. Therefore, the integrated circuit can be operated together with other active elements formed on the substrate, and high performance of the integrated circuit can be achieved.

[0039]

In addition, since the lower wiring has a platinum layer on the upper surface in contact with the metal oxide film and the upper wiring has a titanium layer on the lower surface in contact with the metal oxide film, the lower wiring and the metal oxide film are Can form a Schottky contact between the upper wiring and the ohmic contact between the upper wiring and the metal oxide film.

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Further, by changing the metal of the upper and lower wirings of the metal oxide film, it is possible to provide a semiconductor device capable of flowing a current having a practical current density of 1 to 10 A / cm @ 2 in the vertical direction.

[0040]

Further, since the lower layer wiring is made of a titanium / platinum laminated body and the upper layer wiring is made of a titanium / gold or titanium / platinum / gold laminated body, a semiconductor device having further excellent characteristics can be obtained. Further, since the metal oxide is barium strontium titanate (Bax Sr1-x TiO3; $0 \leqq x \leqq 0.7$), the relative dielectric constant is improved as compared with the conventional one using an insulator such as SiN. A semiconductor device can be obtained.

[0041]

Further, since silicon nitride or silicon oxide is sandwiched between the semiconductor substrate and the lower layer wiring, the process matching with other semiconductor devices on the semiconductor substrate becomes good. Further, since the semiconductor device is used as a diode, a high breakdown voltage diode can be obtained.

[0042]

Further, since the lower layer wiring applies a DC negative bias, which is relatively constant to the upper layer wiring, within a range where the insulation is not destroyed, and is used as a capacitor, the characteristics of the metal oxide film as an insulator are exhibited and the loss is small. A capacitor can be obtained. Further, since the constant DC negative bias is −0.5 V to −10 V, it is possible to obtain a capacitor with less loss.

[0043]

Furthermore, since the diode and the capacitor manufactured in the same process are included in the circuit as constituent elements, the capacitor and the diode can be formed in the same

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process. In addition, the metal oxide film is formed by applying a precursor solution composed of a metal alkoxide constituting the metal oxide film onto the lower layer wiring, and then performing firing in air in the range of 300 ° C to 500 ° C. Since it is formed by the sol-gel method utilizing hydrolysis, it is possible to maintain an oxygen deficiency state that provides a sufficient passing current (1 to 10 A / cm 2). Further, since the firing can be performed at a low temperature, the manufacturing process of other semiconductor devices formed on the semiconductor substrate is not significantly changed, and it is not necessary to select an electrode material that causes a decrease in reliability. .. Therefore, the problem of deterioration of reliability and the manufacturing cost do not increase.

[0044]
Brief description of the drawings

[0045]
1 is a schematic plan view and a sectional view of a semiconductor device of the present invention.

[0046]
2 is a schematic plan view and a sectional view of the manufacturing process of the semiconductor device of the present invention.

[0047]
3 is a schematic plan view and a sectional view of the manufacturing process of the semiconductor device of the present invention.

[0048]
4 is a schematic plan view and a sectional view of the manufacturing process of the semiconductor device of the present invention.

[0049]
5 is a schematic plan view and a sectional view of the semiconductor device of the present invention.

[0050]

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6 is a graph showing the relationship between the current and the voltage applied to the lower layer wiring of the semiconductor device of the present invention.

[0051]
7 is a schematic plan view and a sectional view of the semiconductor device of the present invention.

[0052]
8 is a graph showing the relationship between the current of the semiconductor device of the present invention and the voltage applied to the lower layer wiring.

[0053]
9 is a circuit configuration diagram when the semiconductor device of the present invention is used as a capacitor.

[0054]
10 is a circuit configuration diagram when the semiconductor device of the present invention is used as a diode and a capacitor on the same substrate.

[0055]
Explanation of symbols

[0056]
1 Lower Layer Wiring 2 Metal Oxide Film 3 Upper Layer Wiring 4 Semiconductor Substrate 5 Titanium Layer 6 Platinum Layer 7 Gold Layer 8 Insulating Film A Semiconductor Device

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CLAIMS JPH08167693

1.
A metal oxide film having an oxygen defect is sandwiched between a lower wiring of an arbitrary shape formed of a metal that forms a Schottky contact with a metal oxide on a semiconductor substrate, and the affinity with oxygen is high. A semiconductor device characterized by a vertical structure having an upper layer wiring of an arbitrary shape composed of a metal larger than the metal contained in.

2.
2. The semiconductor device according to claim 1, wherein the lower wiring has a platinum layer on the upper surface in contact with the metal oxide film, and the upper wiring has a titanium layer on the lower surface in contact with the metal oxide film.

3.
3. The semiconductor device according to claim 1, wherein the lower layer wiring is made of a titanium / platinum laminated body, and the upper layer wiring is made of a titanium / gold or titanium / platinum / gold laminated body.

4.
4. The semiconductor device according to claim 1, wherein the metal oxide film is barium strontium titanate (BaxSr1-x TiO3; 0 x 0.7).

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5.
The semiconductor device according to claim 1, wherein a silicon nitride film or a silicon oxide film is sandwiched between the semiconductor substrate and the lower layer wiring.

6.
The semiconductor device according to claim 1, wherein the semiconductor device is used as a diode.

7.
The semiconductor device according to claim 1, wherein the lower layer wiring is used as a capacitor by applying a constant DC negative bias relative to the upper layer wiring within a range that does not destroy the insulation.

8.
8. The semiconductor device according to claim 7, wherein the constant DC negative bias is −0.5V to −10V.

9.
An integrated circuit semiconductor device, comprising the semiconductor device according to claim 6 and claim 7 or 8 manufactured in the same step as a constituent element in a circuit.

10.
The metal oxide film according to any one of claims 1 to 9 is obtained by applying a precursor solution consisting of a metal alkoxide constituting the metal oxide film onto the lower layer wiring, and then firing in air in the range of 300 ° C to 500 ° C. The method for manufacturing a semiconductor device is characterized in that the semiconductor device is formed by a sol-gel method utilizing hydrolysis, which is performed in 1.

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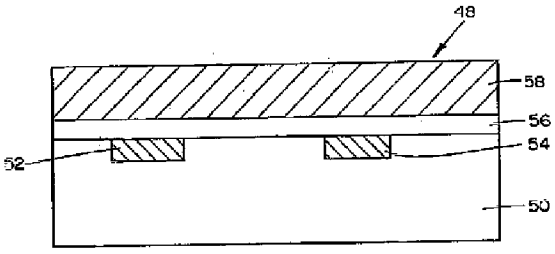
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(54)【発明の名称】　中間ギャップ作業関数タングステン・ゲートの製造方法

(57)【要約】

【課題】高速・高密度アドバンスト酸化金属半導体（ＭＯＳ）および相補形金属酸化膜半導体（ＣＭＯＳ）デバイスに使用される超薄ゲート誘電体等のゲート誘電体上に対して直接に中間ギャップ仕事関数タングステン（Ｗ）ゲートおよびW電極を製造する方法と、該方法によって製造された少なくとも一つのCVDによるWゲートまたはW電極を持つMOSおよびCMOSデバイスを提供する。本発明の方法を量子デバイスに使用可能なW電極の製造にも適用可能とする。

【解決手段】中間ギャップ作業関数タングステン・ゲートの製造方法は、（ａ）原料物質として$W(CO)_6$を使用した化学蒸着（ＣＶＤ）によって、半導体基板上に配置されているゲート誘電体上にタングステン（Ｗ）の層を蒸着する工程と、（ｂ）ゲート誘電体上に中央ギャップ作業関数Wゲートを含むMOSデバイスを形成するために、（ａ）の工程で形成された構造をリソグラフィ技術を用いてパターニングする工程とを有する。



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【特許請求の範囲】
【請求項１】金属酸化物半導体（MOS）の応用に使用される中間ギャップ作業関数タングステン・ゲートの製造方法であって、
（ａ）原料物質として$W(CO)_6$を使用した化学蒸着（CVD）によって、半導体基板上に配置されているゲート誘電体上にタングステン（Ｗ）の層を蒸着する工程と、
（ｂ）前記ゲート誘電体上に前記中間ギャップ作業関数Wゲートを含むMOSデバイスを形成するために、前記（ａ）の工程で形成された構造をリソグラフィ技術を用いてパターニングする工程とを有する中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項２】前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項３】前記超薄ゲート誘電体は、厚さが３nm未満であることを特徴とする請求項２に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項４】前記超薄ゲート誘電体は、SiO_2 窒化SiO_2 Si_3N_4、金属酸化物、およびこれらの混合物からなる群から選択されることを特徴とする請求項３に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項５】前記超薄ゲート誘電体は、SiO_2であることを特徴とする請求項４に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項６】前記半導体基板は、少なくとも一つのソース領域と少なくとも一つのドレイン領域とを備えることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項７】前記半導体基板は、ｐ型の半導体基板またはｎ型の半導体基板であることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項８】前記半導体基板は、シリコン、SiGe、またはGaAsからなることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項９】前記半導体基板は、シリコンからなることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１０】前記化学蒸着（CVD）を行う工程は、250℃から500℃までの温度範囲で実施されることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１１】前記化学蒸着（CVD）を行う工程は、275℃から500℃までの温度範囲で実施されることを特徴とする請求項１０に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１２】前記化学蒸着（CVD）を行う工程は、$1x10^{-6}$Torrから$3x10^{-4}$Torrまでの圧力範囲で実施されることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１３】前記化学蒸着（CVD）を行う工程は、$1x10^{-4}$Torrから$2x10^{-4}$Torrまでの圧力範囲で実施されることを特徴とする請求項１２に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１４】前記化学蒸着（CVD）を行う工程によって得られる前記タングステンの層は、厚さが3.5nmから200nmまでの範囲にあることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１５】前記タングステンの層は、厚さが50nmから100nmまでの範囲にあることを特徴とする請求項１４に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１６】前記パターニングを行う工程は、
前記タングステンの層の所定の領域上に少なくとも一つのフォトレジストを配置する工程と、
前記フォトレジストを現像する工程と、
前記フォトレジストが含まれない前記タングステンの層の領域をエッチングする工程とからなることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１７】前記エッチングの工程は、ウエット・エッチングまたはドライ・エッチングからなることを特徴とする請求項１６に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１８】前記ウエット・エッチングは、H_2O_2、リン酸、クロム酸、硝酸、およびこれらの混合物からなる群から選択される化学エッチング剤を用いて行われることを特徴とする請求項１７に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項１９】前記化学エッチング剤は、H_2O_2であることを特徴とする請求項１８に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項２０】前記ドライ・エッチングとして、反応性イオン・エッチング（RIE）、イオン・ビーム・エッチング（IBE）、およびレーザ切除によるエッチングが挙げられることを特徴とする請求項１７に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項２１】MOSウエハを設ける工程をさらに含み、また前記MOSウエハは、少なくとも一つのソース領域と少なくとも一つのドレイン領域とを有するｐ型半導体基板またはｎ型半導体基板であり、さらに該ｐ型半導体基板またはｎ型半導体基板上に誘電体が配置されていることを特徴とする請求項１に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
【請求項２２】タングステン電極を製造する方法であって、
（ａ）原料材料として$W(CO)_6$を用いる化学蒸着（CV

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D）によって、誘電体をタングステンの層に蒸着する工程と、
（ｂ）前記誘電体上にタングステン電極を形成するために、前記タングステンの層をパターニングする工程とを有することを特徴とするタングステン電極の製造方法。
【請求項２３】ゲート誘電体上に少なくとも一つの中間ギャップ作業関数タングステン・ゲートを有するMOSデバイスであって、
前記中間ギャップ作業関数タングステン・ゲートは、請求項１に記載の方法によって形成されることを特徴とするMOSデバイス。
【請求項２４】前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする請求項２３に記載のMOSデバイス。
【請求項２５】ゲート誘電体上に少なくとも一つの中間ギャップ作業関数タングステン・ゲートを有する電界効果トランジスタ（FET）であって、
前記中間ギャップ作業関数タングステン・ゲートは、請求項１に記載の方法によって形成されることを特徴とする電界効果トランジスタ。
【請求項２６】前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする請求項２５に記載の電界効果トランジスタ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、高速・高密度アドバンスト酸化金属半導体（MOS）および相補形金属酸化膜半導体（CMOS）デバイスに使用される超薄ゲート誘電体等のゲート誘電体上に直接に中間ギャップ仕事関数（mid-gap workfuncition）タングステン（W）ゲートを製造する方法に関する。特に、本発明の中間ギャップ仕事関数Wゲートは、六塩化タングステン（以下、$W(CO)_6$とする）を原料物質として用いる低温・低圧化学蒸着法によって直接にゲート誘電体上に製造する。本発明の方法を量子デバイスに使用可能なW電極の製造にも適用することができる。
【０００２】本発明は、電界効果トランジスタ（FET）やゲート誘電体上に、本発明の方法によって製造される少なくとも一つの中間ギャップ仕事関数Wゲートを含む単純なキャパシタ等の高速・高密度アドバンストMOSおよびCMOSデバイスに関する。
【０００３】
【従来の技術】アドバンスト半導体製造の分野では、高速・高密度MOSデバイスは一般に0.1μm未満のたいへん短いチャンネル長を必要とする。既存のMOSデバイス構造を直線的にそのような短いチャンネル長に合わせることは実用的ではなく、また実行可能なものでもない。
【０００４】したがって、従来のMOSデバイスの上記問題点を克服するために、ポリシリコン・ゲートを持つMOSデバイスのいくつかの新しい型、例えばシリコン・オン・インシュレータ（SOI）やダブル・ゲートMOSデバイスが開発されてきた。しかし、このような従来のデバイスのすべてに共通することは、一般に厚さが約4.0nm未満のたいへん薄い誘電体を必要とする。そのような薄いゲート誘電体を持つデバイスは、可能な限り低いバイアス電圧でもって作動させなければならない。
【０００５】現在のところ、閾値電圧VTの制御は２つのパラメータを調整することによって行われる。第１に、ポリシリコン・ゲートの仕事関数を、p-FETおよびn-FETそれぞれについて、ゲートにp^+またはn^+をドープすることで調整する。第２に、チャンネルの仕事関数を、該チャンネルとゲートとの間に許容可能な仕事関数差を設けるために、基板へ相応にドーピングすることで調節する。この仕事関数差によって内部拡散電位が与えられる。この内部拡散電位は、外部に印加されたバイアス電圧とともに作用して、デバイスのオンおよびオフを行う。
【０００６】ゲート長が0.1μmよりもかなり下回るMOSデバイスでは、一つのデバイスから他のデバイスまでの局所的ドーパント濃度の変動は、容認できないほどのVTの分散をもたらす。したがって、アドバンストCMOSの設計は、本質的に固有のチャンネルで作られなければならない。このことは、VTを設定するために今まで使用された上記パラメータの一つを取り除くので、ゲート仕事関数だけが残る。
【０００７】もっとも低い実現可能な外部から印加されたバイアス電圧を得るために、ゲートのフェルミ準位は、シリコンの価電子帯と伝導帯との間の中間、すなわち中間ギャップに位置すべきである。その結果、ポリシリコン・ゲートを使用する既存の技術ではこのような要求に応えることができない。したがって、精巧な超薄誘電体の加工ができるほど良好な導電率、中間ギャップ仕事関数を持つ新規ゲート材料の開発が求められている。このことには、限定されるものではないけれども、高エネルギー荷電粒子、イオン照射、超薄ゲート誘電体を腐食すると思われる腐食性薬品、および任意の好ましくないゲート材料と誘電体との間の熱力学的に固有の相互作用、例えば相互拡散、粗面化、または相互的な科学的不安定性が無いことが含まれる。ここで注目すべきことは、後に掲げられた固有の要件は、超薄誘電体にとってたいへん厳しいものである。なぜなら、許容できないほど大きな漏れ電流が誘電体の有効厚さにおけるたいへん小さな変化によって誘導されるかもしれないからである。
【０００８】これらの目的および他の目的は、タングステン・ヘキサカルボニル、$W(CO)_6$を原料物質とする低温・低圧CVDプロセスを用いて超薄誘電体等の誘電体層に直接蒸着される中間ギャップ仕事関数Wゲートまたは電極を提供する本発明の方法に合致する。
【０００９】ここで、強調しておくべきことは、CVD技

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術を用いたWの蒸着は当該技術分野において熟知されたものであり、一般に実装の際に配線手段として適用されるということである。そのような用途では、$W(CO)_6$ではなくタングステン・ヘキサフルオリド、WF6が原料物質として一般に用いられる。配線の応用にタングステン・カルボニルを使用することについてはほとんど注目されてこなかった。なぜなら、適度に純粋なW膜を作る上で相対的に高温が必要とされるからである。

【００１０】WF_6を用いたCVDの化学的性質を用いた中間ギャップ仕事関数Wゲートについては、従来技術にすでに開示されている。しかし、このプロセスは、基本的に本発明のものとは異なる。WF_6は超薄ゲート誘電体上に直接Wを蒸着させることに使用することはできない。その代わり、化学的活性段階においてゲート誘電体上にシリコンの薄層を最初に蒸着させ、つぎに（SiF_4を形成するために）シリコンを反応させて除去し、そのかわりにWを残す。さらに、均一にかなり厚い酸化物膜（250nm）の露光はいかなる例外もなしに、大規模なゲート誘電体漏れ電流が認められる完全なデバイス破損を引き起こす。CVDに加えて他の技術が用いられてきたが、従来のプロセスのいずれも超薄ゲート誘電体上に直接Wを蒸着することはできない。

【００１１】配線の用途にタングステン・カルボニルがかなり使用されているにもかかわらず、超薄ゲート誘電体等の誘電体上に中間ギャップ仕事関数Wゲートを設けるために$W(CO)_6$をCDV原料物質として使用することは開示されていない。

【００１２】

【発明が解決しようとする課題】本発明の第１の目的は、ほとんどの従来のプロセスによって一般に必要とされるような任意の化学的活性化準備段階の必要性なしにMOSおよびCMOS用途に使用するために超薄ゲート誘電体等のゲート誘電体に直接中間ギャップ作業関数Wゲートを製造するための方法を提供することである。

【００１３】本発明の第２の目的は、高純度（99.99%以上）で、かつ一般に約５ないし６μohm－cmである理想的なバルク値に近似する抵抗値を持つ超薄ゲート誘電体等のゲート誘電体と合致する中間ギャップ作業関数Wゲートの製造方法を提供することである。

【００１４】本発明の第３の目的は、原料物質として$W(CO)_6$を用いた低温度・低圧力CVDプロセスを含む誘電体上に直接W電極を製造する方法を影響することである。

【００１５】本発明の第４の目的は、原料物質として$W(CO)_6$を用いたCVDによってゲート誘電体上に直接蒸着された本発明の少なくとも一つのWゲートを含むFET等のMOSおよびCMOSデバイスに関する。

【００１６】

【課題を解決するための手段】これらの目的は他の目的と同様に、原料物質として$W(CO)_6$を使用した低温・低圧CVD技術を用いることで本発明によって達成される。特に、本発明の方法は、（ａ）薄膜ゲート誘電体のような誘電体上にWの均一層を直接蒸着する工程と、（ｂ）前記誘電体上に前記中間ギャップ作業関数Wゲートを含むMOSデバイスを形成するために、標準的なリソグラフィック技術を用いて、工程（ａ）で形成された構造をパターニングする工程とを有する。ここで強調すべきことは、本発明では誘電体上にW層を蒸着する上で化学的活性化段階を必要としない。

【００１７】本発明はまた、本発明の方法にもとづいて調製された少なくとも一つの中間ギャップ作業関数Wゲートを含むFET等のMOSデバイスを提供する。本発明にもとづくこのデバイスは、既存の技術にもとづいて調製された従来のデバイスに匹敵するゲート漏れ電流を示し、さらに金属ゲート作業関数に対する理論的値を示す。

【００１８】さらに、本発明は量子デバイスで使用するためのW電極を製造する方法を提供する。本発明のこの実施形態例によれば、W電極は（ａ）誘電体上にWからなる層を蒸着する工程と、前記誘電体上に前記W電極を形成するために前記W層をパターニングする工程とを有し、さらに前記蒸着は$W(CO)_6$を原料物質として用いる化学蒸着法によって行われる方法によって製造される。

【００１９】

【発明の実施の形態】上記したように、本発明は中間ギャップ作業関数WゲートまたはW電極を、いっさいの化学的活性化工程を必要とすることなし、MOSデバイス上に存在する誘電体上に直接設ける方法を提供する。本発明にもとづいて作られる中間ギャップ作業関数WゲートまたはW電極は、高純度であり、MOSデバイス上に見いだされる町薄ゲート誘電体との適合性を有し、さらに理想的なバルク値に近似した固有抵抗値をを持つ。

【００２０】本発明の方法によれば、誘電体上にW層を形成するのに十分な条件下で原料材料として$W(CO)_6$を用いたCDVを採用することによって、Wからなる層を半導体基板の表面にある誘電体の表面に直接蒸着する。当業者が熟知している従来の技術を用いて、W層を含むそのような構造をパターニングする。

【００２１】図１は、W層を蒸着するために本発明に適用される典型的なCVD装置10を示す。特に、装置10は、試験MOSウエハが置かれるグラファイト試料ホルダ・カートリッジ（不図示）を有するロード－ロック・ステンレス合金製反応室12が備わっている。この反応室12は、さらに蒸着中に試料を加熱するためのヒータ・アセンブリ18と蒸着中の圧力を制御する２つの超高真空管16および20とを備える。

【００２２】原料物質14、タングステン・ヘキサカルボニル、$W(CO)_6$は、ステンレス合金製バルブ22を介して反応室12に導入され、かつ管24によって反応室12内に入れられた試験MOSウエハに向けられる。

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【００２３】本発明では任意の等級の$W(CO)_6$を使用することができよう。もし低純度の等級の$W(CO)_6$を用いるとするならば、当業者に既知の精製技術を用いて反応室12への導入に先だって精製することができる。

【００２４】約250℃から約600℃の温度でもって$W(CO)_6$のCVDが起こる。より好ましくは、WのCVD蒸着は約275℃から約500℃の温度でもって起こる。CVD中の反応室の圧力は、$1x10^{-6}$Torrないし約$3x10^{-4}$Torrである。より好ましくは、$W(CO)_6$のCVDは、約$1x10^{-4}$Torrないし約$2x10^{-4}$Torrである。

【００２５】CVDプロセスの実行に要する時間は、一般に約３分から約４時間までの範囲である。この範囲よりも長い時間あるいは短い時間もここで考察する。

【００２６】上記条件下で、厚さが約3.5ないし約200、より好ましくは約50ないし100nmであるWからなる層を、誘電体上に直接蒸着させる。

【００２７】本発明に用いられる典型的なMOSウエハを図３に示す。特に、本発明に適用されうるMOSウエハ48は、少なくとも１つのドレイン領域52と少なくとも一つのソース領域54とを有し、かつこれらの領域が組み入れられた半導体基板50から構成される。また、ドレイン領域52およびソース領域54を半導体基板50の表面に配置してもよい。半導体基板50の表面には、誘電体56からなる層が配置されている。W58からなる層は、既に述べたCVD技術によってゲート誘電体層56の上面に形成される。

【００２８】本発明で使用してもよい半導体基板50は、限定されるものではないが、シリコン、SiGe、またはGaAsである。半導体基板としては、シリコンがもっとも好ましい。

【００２９】製造されている所望のMOSデバイスに応じて、本発明で用いる半導体基板をｐ－型またはｎ－型とすることができる。基板は、当業者に既知の技術を用い製造することができる。半導体基板の厚さは、本発明の方法にとっては重要なことではない。製造されている所望のデバイスに応じて厚さを変えてもよい。

【００３０】本発明で用いる超薄誘電体としては、SiO_2、窒化SiO_2、Si_3N_4、金属酸化物、およびこれらの混合物または化合物が挙げられる。本発明で用いる誘電体を、当業者に既知の方法でもって成長、蒸着、または反応させてもよい。ここで言及したゲート誘電体のため、SiO_2または軽く窒化SiO_2（全窒素含有量５％以下）が現時点ではかなり好ましいものとなっている。

【００３１】本発明の別のかなり好ましい実施形態例では、超薄ゲート誘電体を用いる。「超薄」という用語は、上記に定義したようなゲート誘電体を意味する。この材料の全体の厚さは、デバイスに組み込まれ、かつ通常の状態で作動させた場合に、ゲート漏れ電流の大部分が直接的なトンネル形成の結果によるものとなるような厚さである。特にSiO_2では、このことは約4.0nm未満の厚さに一致する。よりいっそう明確には、「超薄」という用語は、約3.0nm未満の厚さを持つゲート誘電体を意味する。

【００３２】W層58を蒸着させた後、図２に示すMOSウエハを当業者に既知の標準的なリソグラフィ技術を用いてパターニングする。この工程には、限定されるものではないが、化学蒸着（CVD）したW層の表面にフォトレジストを位置決めする段階と、フォトレジストを現像する段階と、フォトレジストがない領域をエッチング技術によって除去する段階とを含む。パターニング後の最終構造60を図３に示す。

【００３３】エッチングは、当業者に既知のウエット・エッチングあるいはドライ・エッチングの技術を用いて行うことができる。ウエット・エッチングを採用する場合、化学エッチング剤はH_2O_2、クロム酸、リン酸、酢酸硝酸等からなる群から選択される。本発明において好ましい化学エッチング剤は、H_2O_2である。化学エッチング剤からなる混合物単独で、あるいは該混合物に水を加えたものもここで検討される。

【００３４】本発明においてドライ・エッチングが採用される場合、反応性イオン・エッチング（RIE）、イオン・ビーム・エッチング（IBE）、またはレーザ切除によってエッチングを行ってもよい。これらのドライ・エッチング技術の各々は、当業者によく知られたものである。

【００３５】本発明はまた、発明の方法によって作製された超薄ゲート誘電体上に少なくとも一つの中間ギャップ作業関数Wゲートをデバイス構造内に含むMOSデバイスに関する。本発明にもとづいて調製された一つの中間ギャップ作業関数Wゲートを含む単純化されたMOSデバイスを図３に示す。デュアル・ゲートMOSデバイスのような２つ以上のMOSゲートを有するデバイスもここで検討される。

【００３６】他のMOSデバイス、例えば電解効果トランジスタ（FET）、単純キャパシタ構造、電解放出デバイス、および量子デバイスもまたここで検討される。これらの構造全体に共通なことは、本発明の方法にもとづいて製造される少なくとも一つの中間ギャップ作業関数Wゲートまたは W電極が誘電体上に直接設けられていることである。

【００３７】以下の実施例は、本発明の範囲を説明するためのものである。この実施例はただ単に説明を目的したものであることから、本発明の実施形態例はそれに限定されてはならない。

【００３８】実施例１

厚さが2.8～7.0nmの範囲内にある熱成長二酸化珪素薄膜を用いて試験構造を製造した。個々のキャパシタを100nm熱成長フィールド酸化物を用いて絶縁した。約0.1ないし0.2ohm－cmの抵抗率を持つｐ型ウエハおよびｎ型ウエハの両方に膜を成長させた。

【００３９】タングステン膜を一括して試験ウエハ上に

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蒸着した。特にW蒸着は約10^{-9}torrのベース圧力を持ち、荷重がロックされたステンレス合金製反応室内で行われた。タングステン・ヘキサカルボニル、$W(CO)_6$を原料気体として用いた。また、この$W(CO)_6$をステンレス合金バルブ経由で反応室に放出するとともに、銅管を介して試料上に向けた。試料をグラファイト製試料ホルダ・カートリッジに導入し、次に反応室チャンバ内に位置したヒータ・アセンブリに導入した。約500℃で蒸着を行った。この系における成長速度は、概して約１．５nm／分であり、大ざっぱにいって温度に依存したものではなく、輸送が限定された成長の仕方を示す。

【００４０】W膜の蒸着後、標準的なリソグラフィ技術を用いてデバイスをパターニングした。各デバイスのタングステン膜に対して、H_2O_2を用いたウエット・エッチングを施した。これによって約10^{-6}から約$10^{-2}cm^2$までの範囲の面積を持つキャパシタ構造が形成された。

【００４１】上記のようにして形成されたキャパシタを高周波数および準静的キャパシタンス－電圧（Ｃ－Ｖ）および電流－電圧技術を用いて試験した。図４および図５は、約3.0ないし7.0nmキャパシタの厚さを持つWゲート酸化膜により形成されたWゲート・キャパシタ構造に関する典型的なＣ－Ｖデータを示す。データは、ｐ型およびｎ型シリコン・ウエハの両方とも含まれるデバイスに関するものである。破線および実線は、約30分間にわたって450℃で10％H_2含有窒素中で実行される標準的な後金属ゲート蒸着成形ガス・アニーリング（FGA）段階の前および後のＣ－Ｖデータを示すものである。図６および図７は、それぞれ処理通りの構造およびFGA構造のＣ－Ｖ特性を示す。

【００４２】Ｃ－Ｖデータを分析すると、FGA処理された試料について低$10^{11}cm^{-2}ev^{-1}$の境界状態密度が示される。平坦なバンド電圧は、ｎ型シリコン・ウエハでは約0.3ボルトであり、ｐ型シリコン・ウエハでは約－0.3ボルトである。このことは、それ自身のなかで、金属ゲートの準位はシリコン中間ギャップにたいへん近いところに位置していることを示している。このことはまた、図４および図５のｙ軸でのＣ－Ｖ曲線の対称性を示している。基板はｎ型およびｐ型の基板の両方ともにドーピング濃度がほぼ同一であることから、電圧の軸について完全な対称性を中間ギャップ金属作業関数ゲートが示すであろうことが予想できよう。

【００４３】上記キャパシタ構造からの電流－電圧データは、図６および図７に示すように、タングステン・ゲートおよびシリコン基板の相対的フェルミ準位と一致している漏れ電流を示している。

【００４４】これらのデータによって、タングステン・ゲート・キャパシタが図６に示すような標準的なポリシリコンをベースとしたキャパシタによって示される漏れ電流と同等の低さの漏れ電流を持つことが示される（妥当な比較を行うために、漏れ電流は真のゲート誘電体電圧降下、$V_{ox} = V_{gate} - V_{FB}$の関数として比較した）。この結果は、厚さ、7.0nmゲート誘電体についてのみ得たものではなく、超薄3.0nm誘電体膜についても求めた。タングステン・ゲートを作る（他の技術によって）ために他の研究者による以前の試みは、厚さが7.0nmの膜であってもこの要求を達成することはできない。

【００４５】本発明を詳細に示し、かつ好ましい実施形態例によって記載してきた一方で、形態および記載において上述および他の変更は本発明の精神および範囲から離れることなく実施することは当業者によって容易に理解されよう。

【００４６】まとめとして、本発明の構成に関して以下の事項を開示する。

（１）金属酸化物半導体（MOS）の応用に使用される中間ギャップ作業関数タングステン・ゲートの製造方法であって、（ａ）原料物質として$W(CO)_6$を使用した化学蒸着（CVD）によって、半導体基板上に配置されているゲート誘電体上にタングステン（Ｗ）の層を蒸着する工程と、（ｂ）前記ゲート誘電体上に前記中間ギャップ作業関数Wゲートを含むMOSデバイスを形成するために、前記（ａ）の工程で形成された構造をリソグラフィ技術を用いてパターニングする工程とを有する中間ギャップ作業関数タングステン・ゲートの製造方法。

（２）前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（３）前記超薄ゲート誘電体は、厚さが３nm未満であることを特徴とする上記（２）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（４）前記超薄ゲート誘電体は、SiO_2 窒化SiO_2 Si_3N_4、金属酸化物、およびこれらの混合物からなる群から選択されることを特徴とする上記（３）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（５）前記超薄ゲート誘電体は、SiO_2であることを特徴とする上記（４）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（６）前記半導体基板は、少なくとも一つのソース領域と少なくとも一つのドレイン領域とを備えることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（７）前記半導体基板は、ｐ型の半導体基板またはｎ型の半導体基板であることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（８）前記半導体基板は、シリコン、SiGe、またはGaAsからなることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。

（９）前記半導体基板は、シリコンからなることを特徴とする上記（１）に記載の中間ギャップ作業関数タング

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ステン・ゲートの製造方法。
（１０）前記化学蒸着（CVD）を行う工程は、250℃から500℃までの温度範囲で実施されることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１１）前記化学蒸着（CVD）を行う工程は、275℃から500℃までの温度範囲で実施されることを特徴とする上記（１０）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１２）前記化学蒸着（CVD）を行う工程は、$1x10^{-6}$Torrから$3x10^{-4}$Torrまでの圧力範囲で実施されることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１３）前記化学蒸着（CVD）を行う工程は、$1x10^{-4}$Torrから$2x10^{-4}$Torrまでの圧力範囲で実施されることを特徴とする上記（１２）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１４）前記化学蒸着（CVD）を行う工程によって得られる前記タングステンの層は、厚さが3.5nmから200nmまでの範囲にあることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１５）前記タングステンの層は、厚さが50nmから100nmまでの範囲にあることを特徴とする上記（１４）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１６）前記パターニングを行う工程は、前記タングステンの層の所定の領域上に少なくとも一つのフォトレジストを配置する工程と、前記フォトレジストを現像する工程と、前記フォトレジストが含まれない前記タングステンの層の領域をエッチングする工程とからなることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１７）前記エッチングの工程は、ウエット・エッチングまたはドライ・エッチングからなることを特徴とする上記（１６）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１８）前記ウエット・エッチングは、H_2O_2、リン酸、クロム酸、硝酸、およびこれらの混合物からなる群から選択される化学エッチング剤を用いて行われることを特徴とする上記（１７）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（１９）前記化学エッチング剤は、H_2O_2であることを特徴とする上記（１８）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（２０）前記ドライ・エッチングとして、反応性イオン・エッチング（RIE）、イオン・ビーム・エッチング（IBE）、およびレーザ切除によるエッチングが挙げられることを特徴とする上記（１７）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（２１）MOSウエハを設ける工程をさらに含み、また前記MOSウエハは、少なくとも一つのソース領域と少なくとも一つのドレイン領域とを有するｐ型半導体基板またはｎ型半導体基板であり、さらに該ｐ型半導体基板またはｎ型半導体基板上に誘電体が配置されていることを特徴とする上記（１）に記載の中間ギャップ作業関数タングステン・ゲートの製造方法。
（２２）タングステン電極を製造する方法であって、（ａ）原料材料として$W(CO)_6$を用いる化学蒸着（CVD）によって、誘電体をタングステンの層に蒸着する工程と、（ｂ）前記誘電体上にタングステン電極を形成するために、前記タングステンの層をパターニングする工程とを有することを特徴とするタングステン電極の製造方法。
（２３）ゲート誘電体上に少なくとも一つの中間ギャップ作業関数タングステン・ゲートを有するMOSデバイスであって、前記中間ギャップ作業関数タングステン・ゲートは、上記（１）に記載の方法によって形成されることを特徴とするMOSデバイス。
（２４）前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする上記（２３）に記載のMOSデバイス。
（２５）ゲート誘電体上に少なくとも一つの中間ギャップ作業関数タングステン・ゲートを有する電界効果トランジスタ（FET）であって、前記中間ギャップ作業関数タングステン・ゲートは、上記（１）に記載の方法によって形成されることを特徴とする電界効果トランジスタ。
（２６）前記ゲート誘電体は、厚さが4.0nm未満である超薄ゲート誘電体であることを特徴とする上記（２５）に記載の電界効果トランジスタ。

【図面の簡単な説明】

【図１】超薄ゲート誘電体上にWを直接蒸着するために、本発明に適用される典型的なCVD装置の構成を説明するための模式的平面図である。
【図２】本発明にもとづく方法にもとづいて調製された典型的なMOSデバイスの構成を示すもので、Wを蒸着した後の断面図である。
【図３】本発明にもとづく方法にもとづいて調製された典型的なMOSデバイスの構成を示すもので、パターニングを施した後の断面図である。
【図４】本発明にもとづいて形成された厚さ3.0nmのWゲート・キャパシタ構造のキャパシタンスと電圧との関係を示すキャパシタンス－電圧曲線図であり、図中、破線は成長した際の関係を示し、実線は成形ガス・アニーリング（FGA）を行った後の関係を示す。
【図５】本発明にもとづいて形成された厚さ7.0nmのWゲート・キャパシタ構造のキャパシタンスと電圧との関係を示すキャパシタンス－電圧曲線図であり、図中、破線は成長した際の関係を示し、実線は成形ガス・アニーリング（FGA）を行った後の関係を示す。

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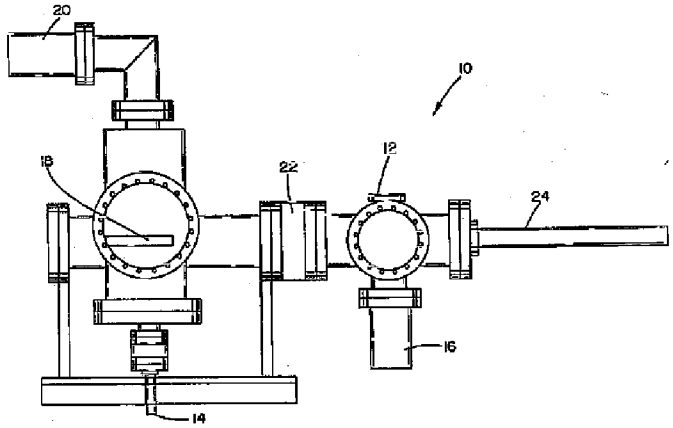
【図６】本発明にもとづいて形成された厚さ3.0nmのWゲート・キャパシタ構造の電流と電圧との関係を示す電流－電圧曲線図であり、図中、破線は成長した際の関係を示し、実線は成形ガス・アニーリング（FGA）を行った後の関係を示す。

【図７】本発明にもとづいて形成された厚さ7.0nmのWゲート・キャパシタ構造の電流と電圧との関係を示す電流－電圧曲線図であり、図中、破線は成長した際の関係を示し、実線は成形ガス・アニーリング（FGA）を行った後の関係を示す。

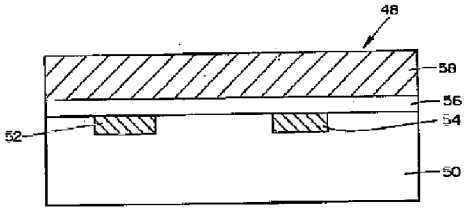
【符号の説明】

１０	CVD装置
１２	ロード－ロック・ステンレス合金製反応室
１４	原料物質
１６	超高真空管
１８	ヒータ・アセンブリ
２０	超高真空管
２２	ステンレス合金製バルブ
２４	管
４８	MOSウエハ
５０	半導体基板
５２	ドレイン領域
５４	ソース領域
５６	誘電体からなる層（ゲート誘電体層）
５８	タングステン（W）からなる層
６０	最終構造

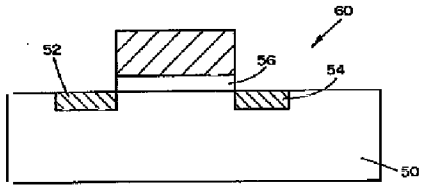
【図１】



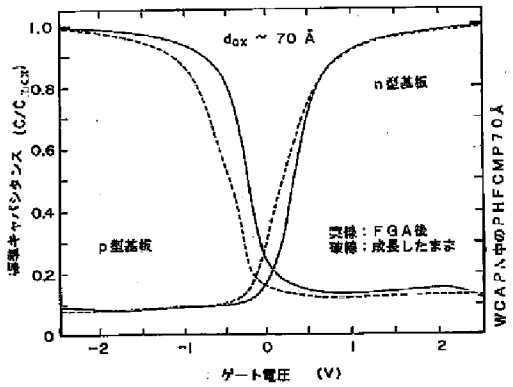
【図２】



【図３】

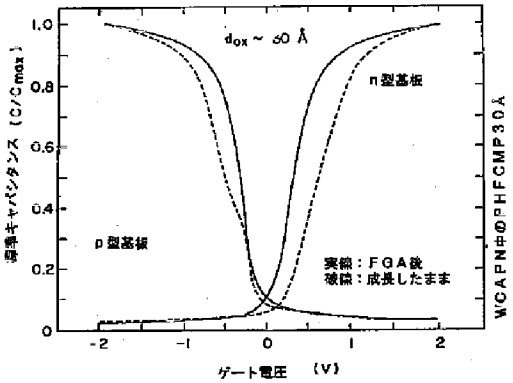


【図４】

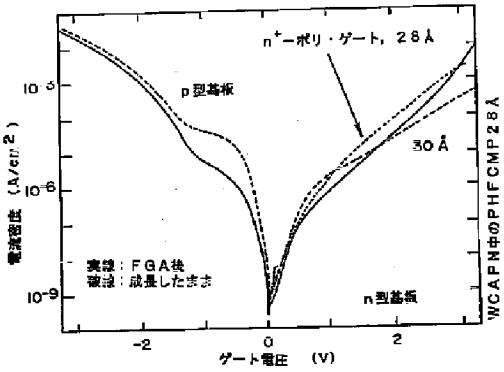


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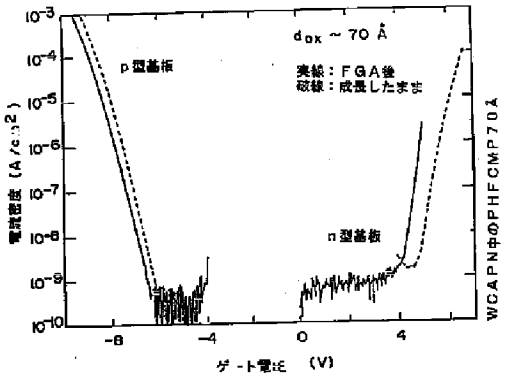
【図５】



【図６】



【図７】



フロントページの続き

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JPH10135452A MANUFACTURE OF INTERMEDIATE GAP WORK FUNCTION TUNGSTEN GATE

Applicants: IBM

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CPC **C23C16/16 (EP); H01L21/28079 (EP); H01L21/32051 (EP);**

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MANUFACTURE OF INTERMEDIATE GAP WORK FUNCTION TUNGSTEN GATE

Abstract

PROBLEM TO BE SOLVED: To provide a method of forming an intermediate gap work function tungsten (W) gate and a W electrode directly on a gate dielectric such as an ultra-thin gate dielectric for use in a high speed and high density advanced metal-oxide semiconductor(MOS) and a complementary metal oxide film semiconductor(CMOS) device, and an MOS device and a CMOS device each having at least one W gate or W electrode formed by the above method by chemical vapor deposition(CVD), and to enable the method to be applied to the manufacture of a W electrode which can be used in a quantum device. SOLUTION: This method comprises the steps of (a) vapor depositing a tungsten (W) layer 58 on a gate dielectric 56 arranged on a semiconductor substrate 50 by CVD using W(CO)6 as a material substance, and (b) patterning the structure formed by the step (a) by using a lithography technique in order to form a MOS device including an intermediate gap work function W gate on the gate dielectric 56.

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DESCRIPTION JPH10135452

[0001]
FIELD OF THE INVENTION This invention relates directly to gate dielectrics such as ultra-thin gate dielectrics used in high speed, high density advanced metal oxide semiconductor (MOS) and complementary metal oxide semiconductor (CMOS) devices. To a method for manufacturing a mid-gap workfunction tungsten (W) gate. In particular, the intermediate gap work function W gate of the present invention is fabricated directly on the gate dielectric by low temperature low pressure chemical vapor deposition using tungsten hexachloride (hereinafter W (CO) 6) as the source material. The method of the present invention can also be applied to the manufacture of W electrodes that can be used in quantum devices.

[0002]
The present invention is directed to high speed, high density advanced MOS and CMOS devices such as simple capacitors containing at least one intermediate gap work function W gate fabricated by the method of the present invention on field effect transistors (FETs) and gate dielectrics. Regarding

[0003]

BACKGROUND OF THE INVENTION In the field of advanced semiconductor manufacturing, high speed, high density MOS devices typically require very short channel lengths of less than 0.1 μm.

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Linearly matching existing MOS device structures to such short channel lengths is neither practical nor feasible.

[0004]

Therefore, in order to overcome the above problems of conventional MOS devices, several new types of MOS devices with polysilicon gates have been developed, such as silicon-on-insulator (SOI) and double-gate MOS devices. It was However, common to all such conventional devices requires a very thin dielectric, typically less than about 4.0 nm thick. Devices with such thin gate dielectrics must operate with the lowest possible bias voltage.

[0005]

At present, the control of the threshold voltage VT is done by adjusting two parameters. First, the work function of the polysilicon gate is tuned for p-FET and n-FET, respectively, by doping the gate with p + or n +. Second, the work function of the channel is adjusted by correspondingly doping the substrate to provide an acceptable work function difference between the channel and the gate. An internal diffusion potential is given by this work function difference. This internal diffusion potential acts with the externally applied bias voltage to turn the device on and off.

[0006]

For MOS devices with gate lengths well below 0.1 μm, variations in local dopant concentration from one device to another result in unacceptable VT dispersion. Therefore, advanced CMOS designs must be made with essentially unique channels. This removes one of the above parameters previously used to set VT, so that only the gate work function remains.

[0007]

In order to obtain the lowest feasible externally applied bias voltage, the Fermi level of the gate should be located at the middle, or middle gap, between the valence band and the conduction band of silicon. As a result, existing technology using polysilicon gates cannot meet such

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demands. Therefore, there is a demand for the development of a new gate material having a good conductivity and an intermediate gap work function, which are capable of processing delicate ultrathin dielectrics. This includes, but is not limited to, energetic charged particles, ion bombardment, corrosive chemicals that are believed to corrode ultra-thin gate dielectrics, and any unwanted heat between the gate material and the dielectric. It includes the absence of mechanically intrinsic interactions such as interdiffusion, roughening, or mutual scientific instability. It is worth noting here that the unique requirements listed below are very strict for ultra-thin dielectrics. This is because unacceptably high leakage currents may be induced by very small changes in the effective thickness of the dielectric.

[0008]
These and other objectives are the intermediate gap work function that is directly deposited on the dielectric layer such as ultra-thin dielectric by using low temperature / low pressure CVD process using tungsten / hexacarbonyl and W (CO) 6 as raw materials. Consistent with the method of the present invention to provide a W gate or electrode.

[0009]

Here, it should be emphasized that the vapor deposition of W using the CVD technique is well known in the technical field and is generally applied as a wiring means at the time of mounting.

For such applications, tungsten hexafluoride, WF6, rather than W (CO) 6, is commonly used as the source material. Little attention has been given to using tungsten carbonyl for wiring applications. This is because a relatively high temperature is required in order to make a moderately pure W film.

[0010]

Intermediate gap work function W gates using the CVD chemistry of WF6 have already been disclosed in the prior art. However, this process is fundamentally different from that of the present invention. WF6 cannot be used to deposit W directly on ultra-thin gate dielectrics. Instead, a thin layer of silicon is first deposited on the gate dielectric in a chemically active step, then the silicon is reacted away (to form SiF4) and removed, leaving W in its place. Furthermore, the exposure of a uniformly thick oxide film (250 nm), without any exception, causes complete device damage with large gate dielectric leakage currents observed. Although other techniques

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have been used in addition to CVD, none of the conventional processes are capable of depositing W directly on the ultrathin gate dielectric.

[0011]
Uses W (CO) 6 as a CDV source material to provide intermediate gap work function W gates on dielectrics such as ultra-thin gate dielectrics, despite the considerable use of tungsten carbonyl for wiring applications It is not disclosed.

[0012]
The first object of the present invention is to use it in MOS and CMOS applications without the need for any chemical activation preparatory steps as is generally required by most conventional processes. To provide a method for fabricating an intermediate gap work function W gate directly on a gate dielectric, such as an ultra thin gate dielectric.

[0013]
A second object of the invention is a gate dielectric, such as an ultra-thin gate dielectric, which is highly pure (99.99% or higher) and which has a resistance value that approximates the ideal bulk value, which is generally about 5 to 6 μ ohm-cm. Is to provide a method of manufacturing an intermediate gap work function W gate that conforms to

[0014]
A third object of the present invention is to influence the method of producing W electrodes directly on a dielectric including a low temperature, low pressure CVD process using W (CO) 6 as the source material.

[0015]
A fourth object of the invention relates to MOS and CMOS devices such as FETs comprising at least one W gate of the invention deposited directly on the gate dielectric by CVD using W (CO) 6 as the source material.

[0016]

These objects, as well as other objects, are achieved by the present invention by using a low temperature, low pressure CVD technique using W (CO) 6 as a starting material.

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In particular, the method of the present invention includes (a) depositing a uniform layer of W directly on a dielectric, such as a thin film gate dielectric, and (b) including the intermediate gap work function W gate on the dielectric. Patterning the structure formed in step (a) using standard lithographic techniques to form a MOS device.

It should be emphasized that the present invention does not require a chemical activation step to deposit the W layer on the dielectric.

[0017]

The invention also provides a MOS device, such as a FET, comprising at least one intermediate gap work function W gate prepared according to the method of the invention.

This device according to the invention exhibits a gate leakage current comparable to conventional devices prepared according to the existing technology, and also a theoretical value for the metal gate work function.

[0018]

Furthermore, the present invention provides a method of making a W electrode for use in a quantum device.

According to this exemplary embodiment of the present invention, the W electrode comprises (a) depositing a layer of W on the dielectric and patterning the W layer to form the W electrode on the dielectric. And the vapor deposition is performed by a chemical vapor deposition method using W (CO) 6 as a raw material.

[0019]

DETAILED DESCRIPTION OF THE INVENTION As indicated above, the present invention provides

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an intermediate gap work function W-gate or W-electrode on a dielectric present on a MOS device without the need for any chemical activation step. Provide a method of providing directly.

The mid-gap work function W-gates or W-electrodes made in accordance with the present invention are of high purity, compatible with the thin gate dielectrics found on MOS devices, and even closer to the ideal bulk value. It has a specific resistance value.

[0020]

According to the method of the present invention, by adopting CDV using W (CO) 6 as a raw material under conditions sufficient to form a W layer on a dielectric, a layer made of W is formed on a semiconductor substrate. Evaporate directly on the surface of the dielectric on the surface. Patterning such structures, including W layers, using conventional techniques familiar to those skilled in the art.

[0021]

FIG. 1 shows a typical CVD apparatus 10 applied to the present invention to deposit a W layer. In particular, the apparatus 10 includes a load-lock stainless steel alloy reaction chamber 12 having a graphite sample holder cartridge (not shown) on which a test MOS wafer is placed. The reaction chamber 12 further comprises a heater assembly 18 for heating the sample during deposition and two ultra high vacuum tubes 16 and 20 for controlling the pressure during deposition.

[0022]
The source material 14, tungsten hexacarbonyl, W (CO) 6 is introduced into the reaction chamber 12 via a stainless alloy valve 22 and directed by a tube 24 to a test MOS wafer contained in the reaction chamber 12.

[0023]

Any grade of W (CO) 6 could be used in the present invention.

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If a low purity grade W (CO) 6 is used, it can be purified prior to introduction into reaction chamber 12 using purification techniques known to those skilled in the art.

[0024]

CVD of W (CO) 6 occurs at temperatures of about 250 ° C to about 600 ° C. More preferably, the CVD deposition of W occurs at a temperature of about 275 ° C to about 500 ° C. The pressure of the reaction chamber during CVD is 1x10-6 Torr to about 3x10-4 Torr. More preferably, the W (CO) 6 CVD is from about 1×10^{-4} Torr to about 2×10^{-4} Torr.

[0025]

The time required to perform the CVD process generally ranges from about 3 minutes to about 4 hours. Times longer or shorter than this range are also considered here.

[0026]
Under the above conditions, a layer of W having a thickness of about 3.5 to about 200, more preferably about 50 to 100 nm is deposited directly on the dielectric.

[0027]

A typical MOS wafer used in the present invention is shown in FIG.

In particular, the MOS wafer 48 applicable to the present invention comprises a semiconductor substrate 50 having at least one drain region 52 and at least one source region 54 and incorporating these regions. Further, the drain region 52 and the source region 54 may be arranged on the surface of the semiconductor substrate 50. On the surface of the semiconductor substrate 50, a layer made of a dielectric material 56 is arranged. A layer of W58 is formed on top of the gate dielectric layer 56 by the CVD technique previously described.

[0028]

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The semiconductor substrate 50 that may be used in the present invention is, but not limited to, silicon, SiGe, or GaAs. Silicon is the most preferable semiconductor substrate.

[0029]

The semiconductor substrate used in the present invention can be p-type or n-type depending on the desired MOS device being manufactured. The substrate can be manufactured using techniques known to those skilled in the art. The thickness of the semiconductor substrate is not critical to the method of the present invention. The thickness may vary depending on the desired device being manufactured.

[0030]

Ultrathin dielectrics used in the present invention include SiO2, SiO2 nitride, Si3N4, metal oxides, and mixtures or compounds thereof. The dielectric used in the present invention may be grown, deposited, or reacted by methods known to those skilled in the art. Due to the gate dielectrics mentioned here, SiO2 or lightly nitrided SiO2 (total nitrogen content <5%) is currently quite preferred.

[0031]

Another fairly preferred embodiment of the present invention uses an ultra-thin gate dielectric. The term "ultra thin" means a gate dielectric as defined above. The total thickness of this material is such that when incorporated into a device and operated under normal conditions most of the gate leakage current is the result of direct tunneling. Especially for SiO2, this corresponds to a thickness of less than about 4.0 nm. Even more specifically, the term "ultra-thin" means a gate dielectric having a thickness of less than about 3.0 nm.

[0032]

After the W layer 58 is deposited, the MOS wafer shown in FIG. 2 is patterned using standard

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lithographic techniques known to those skilled in the art. The process is not limited to, but includes the steps of positioning the photoresist on the surface of the chemical vapor deposition (CVD) W layer, developing the photoresist, and removing the photoresist-free area by an etching technique. And the step of doing. The final structure 60 after patterning is shown in FIG.

[0033]

Etching can be performed using wet etching or dry etching techniques known to those skilled in the art. If wet etching is employed, the chemical etchant is selected from the group consisting of H2O2, chromic acid, phosphoric acid, acetic acid nitric acid and the like. The preferred chemical etchant in the present invention is H2O2. Mixtures of chemical etchants either alone or with water added are also contemplated herein.

[0034]

When dry etching is employed in the present invention, the etching may be done by reactive ion etching (RIE), ion beam etching (IBE), or laser ablation. Each of these dry etching techniques are well known to those skilled in the art.

[0035]

The present invention also relates to a MOS device including at least one intermediate gap work function W gate in a device structure on an ultrathin gate dielectric made by the method of the invention. A simplified MOS device containing one mid-gap work function W gate prepared according to the present invention is shown in FIG. Devices having more than one MOS gate, such as dual gate MOS devices, are also contemplated herein.

[0036]

Other MOS devices, such as field effect transistors (FETs), simple capacitor structures, field emission devices, and quantum devices are also discussed herein. Common to all of these structures is that at least one intermediate gap work function W gate or W electrode manufactured according to the method of the present invention is provided directly on the

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dielectric.

[0037]

The following examples serve to illustrate the scope of the invention. The example embodiments of the present invention should not be limited thereto, as this example is for illustrative purposes only.

[0038]

Example 1 A test structure was manufactured using a thermally grown silicon dioxide thin film having a thickness in the range of 2.8 to 7.0 nm. Individual capacitors were insulated with 100 nm thermally grown field oxide. Films were grown on both p-type and n-type wafers with a resistivity of about 0.1 to 0.2 ohm-cm.

[0039]

A tungsten film was collectively deposited on the test wafer. In particular, W deposition was performed in a stainless steel reaction chamber with a base pressure of about 10-9 torr and a load locked. Tungsten hexacarbonyl and W (CO) 6 were used as source gases. In addition, this W (CO) 6 was discharged into the reaction chamber via a stainless steel alloy valve and was directed onto the sample via a copper tube. The sample was introduced into a graphite sample holder cartridge and then into a heater assembly located in the reaction chamber chamber. Deposition was performed at about 500 ° C. The growth rate in this system is generally about 1.5 nm / min and is roughly temperature independent and shows a mode of transport limited growth.

[0040]

After deposition of the W film, the device was patterned using standard lithographic techniques. Wet etching using H2O2 was performed on the tungsten film of each device. This formed a capacitor structure with an area in the range of about 10-6 to about 10-2 cm2.

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[0041]

The capacitors formed as described above were tested using high frequency and quasi-static capacitance-voltage (CV) and current-voltage techniques. 4 and 5 show typical CV data for a W gate capacitor structure formed by a W gate oxide having a thickness of about 3.0 to 7.0 nm capacitor. The data is for devices that include both p-type and n-type silicon wafers. Dashed and solid lines show C-V data before and after a standard post metal gate deposition forming gas annealing (FGA) step performed in nitrogen containing 10% H2 at 450 ° C for about 30 minutes. Is. 6 and 7 show the CV characteristics of the as-processed structure and the FGA structure, respectively.

[0042]

Analysis of the CV data shows a low 1011 cm-2ev-1 boundary state density for the FGA treated sample. The flat band voltage is about 0.3 volts for n-type silicon wafers and about -0.3 volts for p-type silicon wafers. This indicates that in itself the metal gate level is located very close to the silicon intergap. This also shows the symmetry of the CV curve on the y-axis of FIGS. 4 and 5. Since the substrates are nearly identical in doping concentration for both n-type and p-type substrates, one would expect that the mid-gap metal work function gate would exhibit perfect symmetry about the voltage axis.

[0043]
The current-voltage data from the above capacitor structure shows leakage currents consistent with the relative Fermi levels of the tungsten gate and silicon substrate, as shown in FIGS.

[0044]

These data show that tungsten gate capacitors have leakage currents comparable to those exhibited by standard polysilicon-based capacitors as shown in Figure 6 (a reasonable comparison). The leakage current is compared as a function of the true gate dielectric voltage drop, Vox = Vgate-VFB).

The results were not only obtained for 7.0 nm thick gate dielectrics, but also for ultrathin 3.0 nm dielectric films. Earlier attempts by other researchers to make tungsten gates (by other

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techniques) cannot meet this requirement even with 7.0 nm thick films.

[0045]
While the present invention has been shown in detail and described by way of preferred example embodiments, it will be readily understood by those skilled in the art that the above and other changes in form and description may be made without departing from the spirit and scope of the invention. See.

[0046]

As a summary, the following matters are disclosed regarding the configuration of the present invention.

(1) A method of manufacturing an intermediate gap work function tungsten gate used in metal oxide semiconductor (MOS) applications, which is (a) by chemical vapor deposition (CVD) using W (CO) 6 as a source material. Depositing a layer of tungsten (W) on a gate dielectric disposed on a semiconductor substrate, and (b) forming a MOS device including the intermediate gap work function W gate on the gate dielectric. And a step of patterning the structure formed in the step (a) by using a lithographic technique. (2) The method of manufacturing an intermediate gap work function tungsten gate according to (1) above, wherein the gate dielectric is an ultra-thin gate dielectric having a thickness of less than 4.0 nm. (3) The method for manufacturing an intermediate gap work function tungsten gate according to (2) above, wherein the ultrathin gate dielectric has a thickness of less than 3 nm. (4) The intermediate gap work function tungsten of (3) above, wherein the ultra-thin gate dielectric is selected from the group consisting of SiO2, SiO2 nitride, Si3N4, metal oxides, and mixtures thereof. -Method of manufacturing gate. (5) The method of manufacturing the intermediate gap work function tungsten gate according to the above (4), wherein the ultra-thin gate dielectric is SiO2. (6) The method of manufacturing the intermediate gap work function tungsten gate according to the above (1), wherein the semiconductor substrate has at least one source region and at least one drain region. (7) The method for manufacturing an intermediate gap work function tungsten gate according to (1) above, wherein the semiconductor substrate is a p-type semiconductor substrate or an n-type semiconductor substrate. (8) The method for manufacturing an intermediate gap work function tungsten gate according to the above (1), wherein the semiconductor substrate is made of silicon, SiGe, or GaAs. (9) The method of manufacturing the intermediate gap work function tungsten gate according to the above (1), wherein the semiconductor substrate is made of silicon. (10) Manufacturing of the intermediate gap work function tungsten gate according to the above (1), wherein the step of performing the chemical vapor deposition (CVD) is performed in a

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temperature range of 250 ° C to 500 ° C. Method. (11) Manufacturing of the intermediate gap work function tungsten gate according to the above (10), wherein the step of performing the chemical vapor deposition (CVD) is performed in a temperature range of 275 ° C to 500 ° C. Method.

(12) Manufacturing of the intermediate gap work function tungsten gate according to the above (1), wherein the step of performing the chemical vapor deposition (CVD) is performed in a pressure range of 1x10-6 Torr to 3x10-4 Torr. Method. (13) Manufacturing of the intermediate gap work function tungsten gate according to the above (12), wherein the step of performing the chemical vapor deposition (CVD) is performed in a pressure range of 1x10-4 Torr to 2x10-4 Torr. Method. (14) The intermediate gap work function tungsten according to the above (1), wherein the tungsten layer obtained by the step of performing the chemical vapor deposition (CVD) has a thickness in a range of 3.5 nm to 200 nm. -Method of manufacturing gate. (15) The method of manufacturing the intermediate gap work function tungsten gate according to the above (14), wherein the tungsten layer has a thickness in a range of 50 nm to 100 nm. (16) The patterning step includes the steps of disposing at least one photoresist on a predetermined region of the tungsten layer, developing the photoresist, and removing the tungsten not containing the photoresist. The method of manufacturing an intermediate gap work function tungsten gate according to (1) above, comprising the step of etching a region of the layer. (17) The method for manufacturing an intermediate gap work function tungsten gate according to the above (16), wherein the etching step comprises wet etching or dry etching. (18) The wet etching according to (17) above, wherein the wet etching is performed using a chemical etching agent selected from the group consisting of H2O2, phosphoric acid, chromic acid, nitric acid, and a mixture thereof. Method of manufacturing intermediate gap work function tungsten gate. (19) The method for manufacturing an intermediate gap work function tungsten gate according to the above (18), wherein the chemical etching agent is H2O2. (20) The intermediate gap work according to (17) above, wherein the dry etching includes reactive ion etching (RIE), ion beam etching (IBE), and laser ablation etching. Method of manufacturing a function tungsten gate. (21) The method further includes the step of providing a MOS wafer, and the MOS wafer is a p-type semiconductor substrate or an n-type semiconductor substrate having at least one source region and at least one drain region, and the p-type semiconductor substrate is further included. Alternatively, the method for manufacturing the intermediate gap work function tungsten gate according to the above (1), wherein the dielectric is disposed on the n-type semiconductor substrate.

(22) A method of manufacturing a tungsten electrode, comprising: (a) depositing a dielectric material on a tungsten layer by chemical vapor deposition (CVD) using W (CO) 6 as a raw material; A step of patterning the tungsten layer in order to form a tungsten electrode on the body. (23) A MOS device having at least one intermediate gap work function tungsten gate on a

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gate dielectric, wherein the intermediate gap work function tungsten gate is formed by the method according to (1) above. Characteristic MOS device. (24) The MOS device according to (23) above, wherein the gate dielectric is an ultrathin gate dielectric having a thickness of less than 4.0 nm. (25) A field effect transistor (FET) having at least one intermediate gap work function tungsten gate on a gate dielectric, said intermediate gap work function tungsten gate formed by the method according to (1) above. A field effect transistor characterized by being formed. (26) The field effect transistor according to the above (25), wherein the gate dielectric is an ultrathin gate dielectric having a thickness of less than 4.0 nm.

[0047]
Brief description of the drawings

[0048]
1 is a schematic plan view for explaining the configuration of a typical CVD apparatus applied to the present invention to deposit W directly on the ultra-thin gate dielectric.

[0049]
2 is a cross-sectional view showing the structure of a typical MOS device prepared by the method according to the present invention, after W is deposited.

[0050]
3 is a cross-sectional view after patterning, showing the structure of a typical MOS device prepared according to the method according to the present invention.

[0051]
4 is a capacitance-voltage curve diagram showing the relationship between the capacitance and voltage of the W gate capacitor structure having a thickness of 3.0 nm formed according to the present invention, in which the broken line shows the relationship when grown, The solid line shows the relationship after performing forming gas annealing (FGA).

[0052]
5 is a capacitance-voltage curve diagram showing the relationship between the capacitance and the voltage of the W gate capacitor structure having a thickness of 7.0 nm formed according to the present invention, in which the broken line shows the relationship when grown, The solid line shows the relationship after performing forming gas annealing (FGA).

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[0053]
6 is a current-voltage curve diagram showing the relationship between the current and voltage of the W gate capacitor structure having a thickness of 3.0 nm formed according to the present invention, in which the broken line shows the relationship when grown, The solid line shows the relationship after performing forming gas annealing (FGA).

[0054]
7 is a current-voltage curve diagram showing the relationship between the current and voltage of the W gate capacitor structure having a thickness of 7.0 nm formed according to the present invention, in which the broken line shows the relationship when grown, The solid line shows the relationship after performing forming gas annealing (FGA).

[0055]
Explanation of symbols

[0056]
10 CVD Device 12 Load-Lock Stainless Steel Reaction Chamber 14 Raw Material 16 Ultra High Vacuum Tube 18 Heater Assembly 20 Ultra High Vacuum Tube 22 Stainless Alloy Valve 24 Tube 48 MOS Wafer 50 Semiconductor Substrate 52 Drain Region 54 Source Region 56 Dielectric Material Layer made of (gate dielectric layer) 58 Layer made of tungsten (W) 60 Final structure

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CLAIMS JPH10135452

1.
A method of manufacturing an intermediate gap work function tungsten gate used in metal oxide semiconductor (MOS) applications, comprising: (a) a chemical vapor deposition (CVD) using W (CO) 6 as a source material to form a semiconductor substrate. Depositing a layer of tungsten (W) on an overlying gate dielectric, and (b) forming a MOS device including the intermediate gap work function W gate on the gate dielectric. Patterning the structure formed in step (a) using a lithographic technique.

2.
The method of claim 1, wherein the gate dielectric is an ultra-thin gate dielectric having a thickness of less than 4.0 nm.

3.
The method of claim 2, wherein the ultra-thin gate dielectric has a thickness of less than 3 nm.

4.
The fabrication of intermediate gap work function tungsten gates according to claim 3, wherein the ultra-thin gate dielectric is selected from the group consisting of SiO2, SiO2 nitride, Si3N4, metal oxides, and mixtures thereof. Method.

5.

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The method of claim 4, wherein the ultra-thin gate dielectric is SiO2.

6.
The method of claim 1, wherein the semiconductor substrate comprises at least one source region and at least one drain region.

7.
The method of claim 1, wherein the semiconductor substrate is a p-type semiconductor substrate or an n-type semiconductor substrate.

8.
The method of claim 1, wherein the semiconductor substrate comprises silicon, SiGe, or GaAs.

9.
The method of claim 1, wherein the semiconductor substrate is made of silicon.

10.
The method of claim 1, wherein the step of performing chemical vapor deposition (CVD) is performed in a temperature range of 250 ° C to 500 ° C.

11.
The method of claim 10, wherein the step of performing chemical vapor deposition (CVD) is performed in a temperature range of 275 ° C to 500 ° C.

12.
The method of claim 1, wherein the step of performing chemical vapor deposition (CVD) is performed in a pressure range of 1x10-6 Torr to 3x10-4 Torr.

13.
13. The method of claim 12, wherein the step of performing chemical vapor deposition (CVD) is performed in a pressure range of 1x10-4 Torr to 2x10-4 Torr.

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14.

10. The intermediate gap work function tungsten gate of claim 1, wherein the layer of tungsten obtained by the step of performing chemical vapor deposition (CVD) has a thickness in the range of 3.5 nm to 200 nm. Production method.

15.

15. The method of manufacturing a mid-gap work function tungsten gate of claim 14, wherein the layer of tungsten has a thickness in the range of 50 nm to 100 nm.

16.

The step of patterning comprises the steps of disposing at least one photoresist over a predetermined region of the tungsten layer, developing the photoresist, and removing the tungsten layer not containing the photoresist. The method of claim 1, further comprising the step of etching the region.

17.

17. The method of claim 16, wherein the etching step comprises wet etching or dry etching.

18.

18. The intermediate gap work of claim 17, wherein the wet etching is performed with a chemical etchant selected from the group consisting of H2O2, phosphoric acid, chromic acid, nitric acid, and mixtures thereof. Method of manufacturing a function tungsten gate.

19.

19. The method of claim 18, wherein the chemical etchant is H2O2.

20.

18. The intermediate gap work function tungsten of claim 17, wherein the dry etching includes reactive ion etching (RIE), ion beam etching (IBE), and laser ablation etching. Gate manufacturing method.

21.

The method further includes the step of providing a MOS wafer, and the MOS wafer is a p-type semiconductor substrate or an n-type semiconductor substrate having at least one source region

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and at least one drain region, and the p-type semiconductor substrate or n-type semiconductor substrate. The method of claim 1, wherein the dielectric is disposed on the semiconductor substrate of the mold.

22.

A method of manufacturing a tungsten electrode, the method comprising: (a) depositing a dielectric material on a tungsten layer by chemical vapor deposition (CVD) using W (CO) 6 as a raw material; and (b) on the dielectric material. A step of patterning the tungsten layer to form a tungsten electrode on the substrate.

23.

A MOS device having at least one intermediate gap work function tungsten gate on a gate dielectric, said intermediate gap work function tungsten gate being formed by the method of claim 1. MOS device.

24.

The MOS device of claim 23, wherein the gate dielectric is an ultra-thin gate dielectric having a thickness of less than 4.0 nm.

25.

A field effect transistor (FET) having at least one intermediate gap work function tungsten gate on a gate dielectric, said intermediate gap work function tungsten gate being formed by the method of claim 1. Field-effect transistor characterized by.

26.

The field effect transistor of claim 25, wherein the gate dielectric is an ultra-thin gate dielectric having a thickness of less than 4.0 nm.

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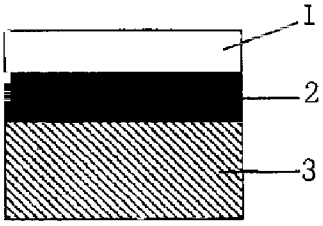
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(54)【発明の名称】　金属、酸化膜及び炭化珪素半導体からなる積層構造体

(57)【要約】
【課題】　炭化珪素単結晶表面を熱酸化して作製したＭＯＳ構造を持つ素子の熱酸化膜内部に発生する正及び負電荷を低減させてＭＯＳ構造のＣ－Ｖ特性及びＩ－Ｖ特性の横方向シフトを低減させることに関するものである。
【構成】　金属、熱酸化膜及び炭化珪素半導体から構成される積層構造体において、その熱酸化膜を５ｎｍ以下の熱酸化膜で形成したことからなる積層構造体であり、又、その熱酸化膜の上に、更に熱酸化以外の方法で酸化膜を作製することにより２層以上の酸化膜を堆積させた積層構造体であり、更に又、その熱酸化以外の方法で作製した酸化膜が窒化膜である積層構造体である。



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【特許請求の範囲】
【請求項１】　金属、酸化膜及び炭化珪素（ＳｉＣ）半導体からなるＭＯＳ構造を有する積層構造体において、この酸化膜が５ｎｍ以下の熱酸化膜で形成されたことを特徴とする積層構造体。
【請求項２】　熱酸化膜の上に熱酸化以外の方法で酸化膜を堆積させて作製した２層以上の酸化膜を持つ請求項１記載の積層構造体。
【請求項３】　熱酸化膜の上に窒化膜を堆積させて作製した請求項２記載の積層構造体。
【請求項４】　金属、酸化膜及び炭化珪素（ＳｉＣ）半導体からなるＭＯＳ構造を有する積層構造体において、金属が導電性の物質で置き換えられた請求項１に記載の積層構造体。
【請求項５】　導電性の物質が多結晶シリコンである請求項４に記載の積層構造体。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、炭化珪素（ＳｉＣ）単結晶表面を熱酸化して作製したＭＯＳ構造を持つ積層構造体の熱酸化膜内部に発生する正電荷及び負電荷を低減させてＭＯＳ構造におけるＣ－Ｖ（容量－電圧）特性及びＩ－Ｖ（電流－電圧）特性の横方向シフトを低減させることに関するものである。
【０００２】
【従来の技術】従来の炭化珪素におけるＭＯＳ構造は、単に炭化珪素単結晶表面に熱酸化膜を作製し、その表面にＭＯＳ構造を形成しただけのものであるので、これらＭＯＳ構造の酸化膜中には、炭化珪素単結晶と熱酸化膜との界面近傍に負の電荷が存在し、又その界面から４０ｎｍ程度離れた酸化膜中には正の多量の電荷が存在していた。
【０００３】このＭＯＳ構造とは、半導体トランジスタを作製する上で基本となる、金属（Ｍｅｔａｌ）ー酸化膜（Ｏｘｉｄｅ）－半導体（Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）の積層構造を意味している。この積層構造の酸化膜は、正確にはSiO_2から構成されるが、電気的には絶縁体である。即ち、半導体表面の酸化を行うだけで、半導体表面に酸化膜からなる絶縁体が形成されるが、これは工業的利用価値が極めて高いので、現在トランジスタ等を作製するための基本的な技術となっている。そこで、現在、シリコン（Ｓｉ）半導体が使用されるのは、この表面を酸化すると酸化膜の絶縁体が形成されるためである。
【０００４】炭化珪素（ＳｉＣ）半導体も、シリコン（Ｓｉ）半導体と同様に、その表面を酸化するとSiO_2酸化膜が形成される。この炭化珪素（ＳｉＣ）半導体は、シリコン（Ｓｉ）半導体の作製技術と同様な方法によりＭＯＳ構造が作製できるので、半導体素子の集積化等の可能性が他の半導体に比べて高く、現在注目されている。
【０００５】
【発明が解決しようとする課題】炭化珪素単結晶表面を熱酸化し、その表面に熱酸化膜を作製した炭化珪素ＭＯＳ構造を持つ積層構造体は、その作製条件により、ＭＯＳ構造のＣ－Ｖ特性及びＩ－Ｖ特性の横方向シフトの量が異なったり、放射線照射時のＣ－Ｖ特性及びＩ－Ｖ特性の横方向シフトが酸化膜の吸収線量により増減するなどの複雑で不安定な挙動を示した。
【０００６】即ち、ＳｉＣのＭＯＳ構造を作製するためにＳｉＣ表面を酸化すると、その時の酸化法によって、酸化膜の中に電子や正孔（電子の抜けた穴）が形成される。トランジスタを、炭化珪素単結晶のＭＯＳ構造を利用して作製する場合には、この電子や正孔がトランジスタ特性を劣化させるので、大きな問題となっていた。
【０００７】又、Ｃ－Ｖ特性とは、ＭＯＳ構造を形成する酸化膜に電圧（Ｖｏｌｔａｇｅ）を印加したときの、酸化膜内部、又は酸化膜と炭化珪素との界面近傍に蓄積する電子や正孔の量を反映する電気容量（Ｃａｐａｃｉｔａｎｃｅ）の変化を調べる測定のことで、ＭＯＳ構造のＣ－Ｖ特性を調べることにより、トランジスタ特性の劣化の主原因となる電子や正孔の量を評価することができる。したがって、種々の酸化方法で半導体表面を酸化してＭＯＳ構造を形成し、そのＣ－Ｖ特性を測定することにより酸化方法の最適化を行うことが可能になる。
【０００８】更に又、Ｉ－Ｖ特性とは、ＭＯＳ構造を有する半導体素子を図４のように作製したときに、ＭＯＳ構造電極に印加する電圧（Ｖ）に対し、ＭＯＳ構造を挟むようにして配置した電極間に流れる電流（Ｉ）の強さを表す特性のことであり、これは、ＭＯＳ構造の電極に電圧を印加すると、電極直下の酸化膜と炭化珪素半導体界面、あるいは炭化珪素半導体中の抵抗を大きく変化することを利用している。
【０００９】したがって、酸化膜中に図３に示されるような電荷が蓄積しているときには、酸化膜を介して電圧を炭化珪素半導体に印加すると、酸化膜内の電荷の影響により印加電圧（Ｖ）の強さが変化する。これにより、ＭＯＳ構造電極に電圧（Ｖ）を印加したときには、ＭＯＳ構造を挟むようにして配置した電極間に流れる電流（Ｉ）の流れ具合が変化してしまい、本来のＩ－Ｖ特性が得られなくなる。そこで、本発明による５ｎｍ以下の酸化膜を有するＭＯＳ構造を作製すると、酸化膜中の電荷が大きく低減されるので、Ｉ－Ｖ特性の大きな改善がなされることになる。
【００１０】
【課題を解決するための手段】本発明は、炭化珪素単結晶表面に形成された熱酸化膜の厚さを５ｎｍ以下に保つことにより、熱酸化によって酸化膜内部に発生する、炭化珪素と酸化膜との界面から５ｎｍ以上離れ且つ約２０ｎｍ以内までの範囲に分布する負電荷、及び界面から４

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０ｎｍの位置近傍に生ずる正電荷を除去できるので、酸化膜中の電荷量が減少してＭＯＳ構造のＣ－Ｖ特性の挙動を安定させることができるものである。

【００１１】即ち、本発明は、金属、酸化膜及び炭化珪素半導体からなるＭＯＳ構造を有する積層構造体において、この酸化膜が５ｎｍ以下の熱酸化膜で形成された積層構造体であり、又この熱酸化膜の上に熱酸化以外の方法で酸化膜を堆積させて２層以上の酸化膜を持つことができ、更に又熱酸化膜の上に窒化膜を堆積させることもできるものである。

【００１２】本発明において、炭化珪素単結晶半導体表面に酸化膜を形成してＭＯＳ構造を作製した場合には、図１に示されるように、炭化珪素半導体３の上に熱酸化膜２が作製され、その上に金属１が形成される。又図２に示されるように、炭化珪素半導体３の上に熱酸化膜２が作製され、更にその上に熱酸化以外の方法で作製された酸化膜４又は窒化膜４が形成され、更にその上に金属１が形成される。

【００１３】又、炭化珪素単結晶半導体表面に酸化膜を形成してＭＯＳ構造を有する半導体素子を作製した場合には、図４に示されるように、ＭＯＳ構造を挟むような形で半導体に直接触れる金属電極を配置した構造となり、そのＭＯＳ構造部分に電圧を印加すると、挟み込むように配置した電極間の抵抗が減少して電流が流れるようになるので、この素子構造の動作をつかさどる中心部はＭＯＳ構造である。

【００１４】

【発明の実施の形態】本発明のＭＯＳ構造の作製においては、熱酸化膜の厚さが５ｎｍ以下になるように熱酸化する。また、耐電圧が必要なＭＯＳ構造の半導体素子を作製するには、熱酸化により５ｎｍ以下の熱酸化膜を作製後、ＣＶＤ法等の熱酸化以外の方法により、その熱酸化膜の上に酸化膜又は窒化膜などの絶縁膜を堆積成長させて増加した膜厚を得る。

【００１５】本発明の金属、酸化膜及び炭化珪素半導体からなるＭＯＳ構造を有する積層構造体における金属としては、アルミニウム、金、白金、モロブデン等の導電性金属が使用されるが、この金属のに代えて導電性が金属に匹敵する燐を多量に含むポリシリコン（多結晶シリコン）等の導電性物質も使用され得る。

【００１６】熱酸化方法には、１０００－１２００℃の乾燥酸素中でＳｉＣを酸化する方法と同程度の温度の水蒸気中でＳｉＣを酸化する方法とが知られているが、水蒸気による酸化法が電気的に良い酸化膜を得ることができるので、本発明においてもこの方法を使用する。

【００１７】なお、熱酸化方法以外の酸化方法としては、ＳｉＣに対して室温でオゾンを用いてＳｉＣ表面を酸化して酸化膜を作製する方法、Ｓｉ原子を含むガスと酸素を含むガスとを１０００℃程度に加熱したＳｉＣに吹き付けて、その表面にSiO_2膜を化学的に堆積させる化学気相堆積法（Ｃｈｅｍｉｃａｌ　Ｖａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ法）等の方法が使用される。

【００１８】図３に、炭化珪素単結晶表面に１００ｎｍの熱酸化膜を作製してＭＯＳ構造を形成したときの熱酸化膜内部の電荷分布を示している。負電荷は、結晶界面から５ｎｍまでの範囲と、５ｎｍから２０ｎｍまでの範囲とに分布する２種類の負電荷からなり、前者が極めて応答時間の長いイオン化した界面準位を示し、後者が熱酸化膜中に捕らえられた負電荷である。また正電荷は４０ｎｍ近傍の位置に局在している。したがって、熱酸化膜を５ｎｍ以下にすることにより、上述の負電荷の一部と正電荷の全て（５ｎｍから２０ｎｍまでの負電荷、及び４０ｎｍ近傍の位置の正電荷）を除去する事ができる。

【００１９】ＳｉＣの酸化膜中には、図３に示すように、通常の酸化方法で酸化膜を作製すると深さ方向に向かって負電荷や正電荷が局在することが知られているが、界面準位とは、酸化膜と炭化珪素（ＳｉＣ）半導体の界面近傍に発生する酸化膜の欠陥のことであり、ＭＯＳ構造に印加される電圧の強さによって酸化膜中の電子や正孔を捕獲したり放出したりするので、この捕獲や放出のタイミングがトランジスタ特性に悪影響を与えるために、通常はこれを無くすことが技術的に重要である。しかし、ＳｉＣの界面準位（ＳｉＣ半導体の界面から５ｎｍの範囲の酸化膜）の場合は、この捕獲又は放出のタイミングが、室温では極めて遅い性質があり、電圧を加えても捕らえた電子をなかなか放出しないので、あたかも捕獲や放出を行わない酸化膜内部に蓄積した負電荷のように行動する。

【００２０】

【実施例】ＳｉＣ半導体の表面処理を行い、その清浄表面を露出させた。次に、酸化炉を立ち上げて酸化炉内を１０００－１２００℃の高温の水蒸気雰囲気（水素燃焼酸化が行われる雰囲気）に保持した。この炉内に表面浄化された半導体を挿入し、その浄化表面に酸化膜を作製した。酸化が終了した段階で得られた半導体を炉外に引き出して室温まで急速に冷却した。その結果、酸化時間を調整することにより５ｎｍの酸化膜を半導体表面に作製できた。

【００２１】次に、必要に応じて、この半導体をＣＶＤ装置の炉内に入れ、その表面に酸化膜又は窒化膜を堆積させた。

【００２２】なお、酸化時間は、ＳｉＣ半導体の面方位と呼ばれている結晶軸の方向や結晶の形態により異なり、比較的よく使用されている６Ｈ－ＳｉＣ（六方晶ＳｉＣ）と呼ばれる単結晶のシリコン面（０００１面）では、１１００℃の温度で、その表面を酸化すると一分間に０．４ｎｍ酸化されるので、５ｎｍの酸化膜を作製するためには、約１３分の酸化時間を要した。

【００２３】

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【発明の効果】本発明の方法によれば、ＳｉＣのＭＯＳ構造体の熱酸化膜中に発生する電荷量を低く押さえることができるため、炭化珪素ＭＯＳ構造のＣ－Ｖ特性及びＩ－Ｖ特性、あるいは炭化珪素ＭＯＳ構造を有する炭化珪素半導体素子などの電気特性を安定させる事ができる。

【図面の簡単な説明】

【図１】　ＭＯＳ構造の基本断面図である。

【図２】　酸化膜とＣＶＤ法で堆積させた２層の酸化膜又は窒化膜を持つＭＯＳ構造の基本断面図である。

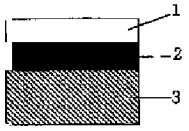
【図３】　炭化珪素単結晶表面に１００ｎｍの熱酸化膜を作製し、その表面にＭＯＳ構造を形成したときの、熱酸化膜内部の電荷分布を示す図である。

【図４】　ＭＯＳ構造及びＭＯＳ構造を有する炭化珪素半導体素子構造を示す図である。

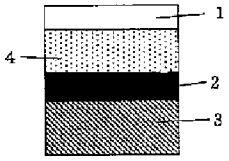
【符号の説明】

１：電極、２：熱酸化膜、３：炭化珪素半導体、４：ＣＶＤ法で堆積させた酸化膜又は窒化膜、５：電極。

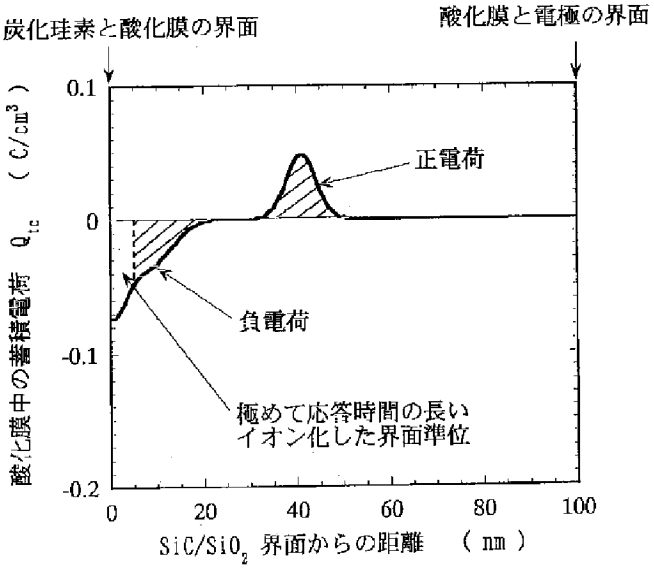
【図１】



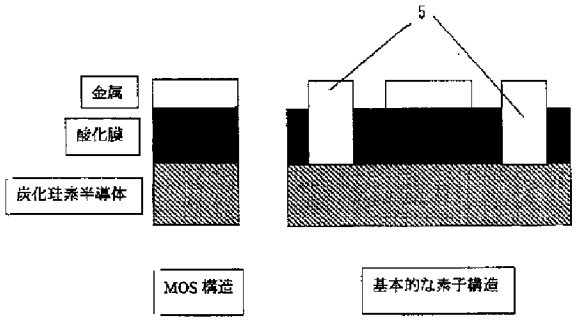
【図２】



【図３】



【図４】



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JPH11233760A LAMINATED STRUCTURE MEMBER COMPOSED OF METAL, OXIDE FILM AND SILICON CARBIDE SEMICONDUCTOR

Applicants: JAPAN ATOMIC ENERGY RES INST

Inventors: NASHIYAMA ISAMU,YOSHIKAWA MASATO

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LAMINATED STRUCTURE MEMBER COMPOSED OF METAL, OXIDE FILM AND SILICON CARBIDE SEMICONDUCTOR

Abstract

PROBLEM TO BE SOLVED: To reduce lateral direction shift of C-V characteristics and I-V characteristics of an MOS structure, by reducing positive and negative charges generated in a thermal oxidation film of an element having an MOS structure which is formed by thermally oxidizing silicon carbide single crystal surface. SOLUTION: This laminated structure member is constituted of metal 1, a thermal oxidation film 2 and silicon carbide semiconductor 3. The thermal oxidation film 2 is formed of a thermal oxidation film of at most 5 nm in thickness. By forming an oxide film on the thermal oxidation film by using a method except thermal oxidation, a laminated structure member in which at least two layers of oxide films are deposited is obtained. The oxide film formed by a method except the thermal oxidation is a nitride film.

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DESCRIPTION JPH11233760

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention reduces the positive and negative charges generated inside a thermal oxide film of a laminated structure having a MOS structure, which is produced by thermally oxidizing the surface of a silicon carbide (SiC) single crystal. The present invention relates to reducing a lateral shift of a CV (capacitance-voltage) characteristic and an IV (current-voltage) characteristic in a MOS structure.

[0002]
2. Description of the Related Art In the conventional MOS structure in silicon carbide, a thermal oxide film is simply formed on the surface of a silicon carbide single crystal, and the MOS structure is formed on the surface. , There was a negative charge near the interface between the silicon carbide single crystal and the thermal oxide film, and a large amount of positive charges were present in the oxide film about 40 nm away from the interface.

[0003]

The MOS structure means a laminated structure of metal (Metal) -oxide film (Oxide) -semiconductor (Semiconductor) which is a basis for manufacturing a semiconductor transistor.

To be precise, the oxide film of this laminated structure is composed of SiO2, but is electrically an insulator. That is, an insulator made of an oxide film is formed on the semiconductor surface only

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by oxidizing the semiconductor surface. However, since this has an extremely high industrial utility value, it is currently used as a basic technique for manufacturing a transistor or the like. Has become. Therefore, a silicon (Si) semiconductor is currently used because an oxide film insulator is formed when the surface is oxidized.

[0004]

Similar to a silicon (Si) semiconductor, a silicon carbide (SiC) semiconductor forms a SiO2 oxide film when its surface is oxidized. Since this silicon carbide (SiC) semiconductor has a MOS structure that can be manufactured by a method similar to that of a silicon (Si) semiconductor, the possibility of integration of semiconductor elements is higher than that of other semiconductors, and it is currently receiving attention. ing.

[0005]
A laminated structure having a silicon carbide MOS structure, in which a surface of a silicon carbide single crystal is thermally oxidized and a thermal oxide film is formed on the surface, has a C-V structure of a MOS structure depending on the manufacturing conditions. The amount of lateral shift of the characteristics and IV characteristics is different, and the lateral shift of the CV characteristics and IV characteristics during irradiation increases or decreases depending on the absorbed dose of the oxide film. showed that.

[0006]

That is, when the SiC surface is oxidized to form a SiC MOS structure, electrons and holes (holes from which electrons have been removed) are formed in the oxide film by the oxidation method at that time.

In the case of manufacturing a transistor using a silicon carbide single crystal MOS structure, the electrons and holes deteriorate the transistor characteristics, which is a serious problem.

[0007]

The C-V characteristic is the amount of electrons and holes accumulated inside the oxide film or

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near the interface between the oxide film and silicon carbide when a voltage (Voltage) is applied to the oxide film forming the MOS structure. It is possible to evaluate the amount of electrons and holes, which are the main causes of deterioration of transistor characteristics, by examining the CV characteristic of the MOS structure by measuring the change in the capacitance that reflects the change. .. Therefore, it becomes possible to optimize the oxidation method by oxidizing the semiconductor surface by various oxidation methods to form a MOS structure and measuring the CV characteristics thereof.

[0008]

Furthermore, the IV characteristic means that when a semiconductor device having a MOS structure is manufactured as shown in FIG. 4, a voltage (V) applied to the MOS structure electrodes is applied between electrodes arranged so as to sandwich the MOS structure. This is a characteristic that expresses the strength of a current (I) that flows, and when a voltage is applied to an electrode with a MOS structure, the resistance in the oxide film and silicon carbide semiconductor interface directly under the electrode or in the silicon carbide semiconductor changes greatly. You are taking advantage of what you do.

[0009]

Therefore, when the voltage as shown in FIG. 3 is accumulated in the oxide film and the voltage is applied to the silicon carbide semiconductor through the oxide film, the applied voltage (V) is increased due to the influence of the charges in the oxide film. Changes.

As a result, when a voltage (V) is applied to the MOS structure electrodes, the flow condition of the current (I) flowing between the electrodes arranged so as to sandwich the MOS structure changes, and the original IV characteristic cannot be obtained. .. Therefore, when a MOS structure having an oxide film of 5 nm or less according to the present invention is manufactured, the charge in the oxide film is greatly reduced, and thus the IV characteristic is greatly improved.

[0010]

According to the present invention, by keeping the thickness of a thermal oxide film formed on the surface of a silicon carbide single crystal to be 5 nm or less, silicon carbide and oxides generated inside the oxide film by thermal oxidation can be obtained. Since the negative charges distributed in the range of 5 nm or more from the interface with the film and within about 20 nm and the positive charges generated in the vicinity of the position of 40 nm from the interface can

GF Exhibit 1126 - 1875/2248

be removed, the amount of charges in the oxide film is reduced and The behavior of the C-V characteristic can be stabilized.

[0011]
That is, the present invention is a laminated structure having a MOS structure composed of a metal, an oxide film and a silicon carbide semiconductor, wherein the oxide film is a thermal oxide film of 5 nm or less, and the thermal oxide film is It is possible to deposit an oxide film by a method other than thermal oxidation to have two or more oxide films, and it is also possible to deposit a nitride film on the thermal oxide film.

[0012]

In the present invention, when an oxide film is formed on the surface of a silicon carbide single crystal semiconductor to produce a MOS structure, a thermal oxide film 2 is produced on a silicon carbide semiconductor 3 as shown in FIG. Metal 1 is formed on top.

Further, as shown in FIG. 2, thermal oxide film 2 is formed on silicon carbide semiconductor 3, and further, oxide film 4 or nitride film 4 formed by a method other than thermal oxidation is formed thereon. Metal 1 is formed on top.

[0013]
When an oxide film is formed on the surface of a silicon carbide single crystal semiconductor to manufacture a semiconductor device having a MOS structure, as shown in FIG. 4, a metal electrode that directly contacts the semiconductor with the MOS structure sandwiched therebetween. When a voltage is applied to the MOS structure part, the resistance between the electrodes arranged so as to sandwich it is reduced and a current flows. Therefore, the central part that controls the operation of this element structure is the MOS structure. is there.

[0014]

BEST MODE FOR CARRYING OUT THE INVENTION In manufacturing the MOS structure of the present invention, thermal oxidation is performed so that the thickness of the thermal oxide film is 5 nm or less.

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Further, in order to manufacture a semiconductor device having a MOS structure that requires a withstand voltage, a thermal oxide film having a thickness of 5 nm or less is formed by thermal oxidation, and then oxidation is performed on the thermal oxide film by a method other than thermal oxidation such as a CVD method. An insulating film such as a film or a nitride film is deposited and grown to obtain an increased film thickness.

[0015]

A conductive metal such as aluminum, gold, platinum, or molobden is used as the metal in the laminated structure having the MOS structure including the metal, the oxide film, and the silicon carbide semiconductor according to the present invention. Conductive materials such as polysilicon (polycrystalline silicon) containing a large amount of phosphorus whose properties are comparable to those of metals can also be used.

[0016]

As a thermal oxidation method, a method of oxidizing SiC in dry oxygen at 1000 to 1200 ° C. and a method of oxidizing SiC in steam at a temperature similar to that of steam are known. This method is also used in the present invention because an excellent oxide film can be obtained.

[0017]

As an oxidation method other than the thermal oxidation method, a method of oxidizing the SiC surface by using ozone at room temperature for SiC to form an oxide film, and a gas containing Si atoms and a gas containing oxygen at 1000 ° C. A method such as a chemical vapor deposition method (Chemical Vapor Deposition method) for spraying moderately heated SiC to chemically deposit an SiO2 film on the surface is used.

[0018]

FIG. 3 shows the charge distribution inside the thermal oxide film when a 100 nm thermal oxide film was formed on the surface of a silicon carbide single crystal to form a MOS structure.

Negative charges consist of two types of negative charges distributed in the range from the crystal interface to 5 nm and in the range from 5 nm to 20 nm. The former shows an ionized interface state with a very long response time, and the latter shows thermal oxidation. It is the negative charge trapped in the film.

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The positive charge is localized at a position near 40 nm.

Therefore, by setting the thermal oxide film to 5 nm or less, it is possible to remove a part of the above-mentioned negative charges and all of the positive charges (negative charges from 5 nm to 20 nm, and positive charges in the vicinity of 40 nm).

[0019]

As shown in FIG. 3, it is known that, when an oxide film is formed by an ordinary oxidation method, negative charges and positive charges are localized in the depth direction in the oxide film of SiC. The term "position" refers to a defect in the oxide film that occurs near the interface between the oxide film and the silicon carbide (SiC) semiconductor, and traps electrons and holes in the oxide film depending on the strength of the voltage applied to the MOS structure. It is technically important to eliminate this because the timing of this capture or release adversely affects the transistor characteristics.

However, in the case of the SiC interface state (oxide film in the range of 5 nm from the interface of the SiC semiconductor), the timing of this capture or release is extremely slow at room temperature, and it is difficult to capture the captured electrons even if a voltage is applied. Since it does not release, it behaves as if it were a negative charge accumulated inside the oxide film that does not capture or release.

[0020]

EXAMPLE A surface treatment of a SiC semiconductor was performed to expose its clean surface. Next, the oxidation furnace was started up and the inside of the oxidation furnace was maintained in a high temperature steam atmosphere of 1000 to 1200 ° C (an atmosphere in which hydrogen combustion oxidation is performed). A semiconductor whose surface was purified was inserted into this furnace, and an oxide film was formed on the purified surface. The semiconductor obtained at the stage when the oxidation was completed was taken out of the furnace and rapidly cooled to room temperature. As a result, a 5 nm oxide film could be formed on the semiconductor surface by adjusting the oxidation time.

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[0021]
Next, if necessary, this semiconductor was put in a furnace of a CVD apparatus, and an oxide film or a nitride film was deposited on the surface thereof.

[0022]
Note that the oxidation time varies depending on the direction of the crystal axis, which is called the plane orientation of the SiC semiconductor, and the form of the crystal, and is a relatively frequently used single-crystal silicon surface called 6H—SiC (hexagonal SiC) (0001 plane), when the surface is oxidized at a temperature of 1100 ° C., 0.4 nm is oxidized in 1 minute, so that it takes about 13 minutes to form a 5 nm oxide film.

[0023]
According to the method of the present invention, the amount of charges generated in the thermal oxide film of the SiC MOS structure can be kept low, so that the C-V characteristic and the I-V characteristic of the silicon carbide MOS structure can be suppressed. Alternatively, the electrical characteristics of a silicon carbide semiconductor device having a silicon carbide MOS structure or the like can be stabilized.

GF Exhibit 1126 - 1879/2248

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CLAIMS JPH11233760

1.
A laminated structure having a MOS structure composed of a metal, an oxide film, and a silicon carbide (SiC) semiconductor, wherein the oxide film is formed of a thermal oxide film of 5 nm or less.

2.
The laminated structure according to claim 1, which has two or more oxide films formed by depositing an oxide film on the thermal oxide film by a method other than thermal oxidation.

3.
The laminated structure according to claim 2, which is manufactured by depositing a nitride film on the thermal oxide film.

4.
The laminated structure according to claim 1, wherein the metal is replaced with a conductive substance in the laminated structure having a MOS structure composed of a metal, an oxide film, and a silicon carbide (SiC) semiconductor.

5.
The laminated structure according to claim 4, wherein the conductive substance is polycrystalline silicon.

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GF Exhibit 1126 - 1881/2248

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심사청구 : 없음

(54) 반도체장치의 제조방법

요약

본 발명은 프로그램가능한 접속소자(programmable interconnect devices;PID)용 안티퓨즈 제조방법에 관한 것이다.

본 발명에 의한 PID용 안티퓨즈 제조방법은 PID용 안티퓨즈콘택과 금속콘택을 동시에 형성하는 공정과 안티퓨즈 막질로서 금속산화막을 형성하는 공정으로 이루어지는 것을 특징으로 한다.

본 발명에 의하면, 최소한의 포토리소그래픽공정에 의해 ID용 안티퓨즈를 형성할 수 있으며, 금속산화막을 안티퓨즈막으로 사용함으로써 막질의 두께를 조절할 수 있고 누설전류를 감소시킬 수 있어 안정된 소자동작을 얻을 수 있다.

대표도

도7

명세서

[발명의 명칭]

반도체장치의 제조방법

[도면의 간단한 설명]

제7도 내지 제11도는 본 발명에 의한 PID용 안티퓨즈 제조방법을 도시한 공정순서도.

본 내용은 요부공개 건이므로 전문 내용을 수록하지 않았음.

(57) 청구의 범위

청구항 1

반도체기판상에 하부도전층을 형성하는 공정; 상기 하부도전층상에 절연층을 형성하는 공정; 상기 하부도전층의 소정부분을 노출시키기 위해 상기 절연층에 안티퓨즈 콘택개구부 및 금속 콘택개구부를 동시에 형성하는 공정; 상기 결과물 전면에 금속산화막을 형성하는 공정; 상기 안티퓨즈 콘택영역에만 상기 금속산화막을 남기는 공정; 상기 결과물 전면에 금속을 증착한 후 이를 소정패턴으로 패터닝하여 상기 안티퓨즈 콘택영역의 상기 남아있는 금속산화막의 상부 및 상기 금속 콘택영역상에 상부도전층을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 2

제1항에 있어서, 상기 금속산화막은 금속을 증착한 후 산화공정에 의해 상기 금속을 산화시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 3

제2항에 있어서, 상기 금속은 Ti, Al, Ba, Ge, Sn, Be, Nb 및 Ta 중에서 선택한 어느 하나임을 특징으로 하는 반도체장치의 제조방법.

청구항 4

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제2항에 있어서, 상기 산화공정은 400℃~800℃의 온도 범위에서 행하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 5

제1항에 있어서, 상기 금속산화막은 금속가스를 산소플라즈마에 통과시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

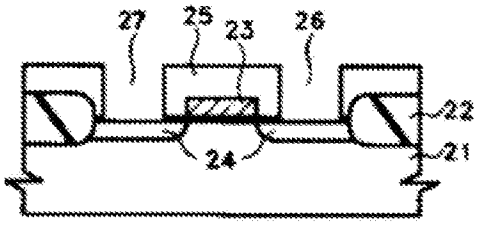
청구항 6

제1항에 있어서, 상기 상부도전층은 반도에기판에 형성된 불순물확산영역, 불순물이 도우프된 폴리실리콘층, 폴리사이드층 또는 반도체기판의 도전영역임을 특징으로 하는 프로그램가능한 접속소자의 제조방법.

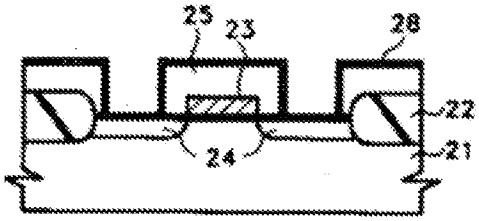
※ 참고사항 : 최초출원 내용에 의하여 공개하는 것임

도면

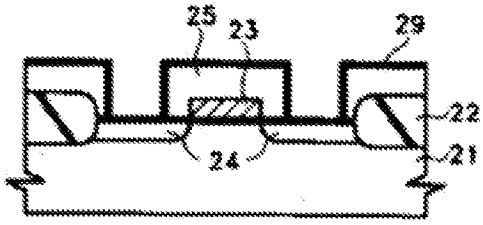
도면7



도면8

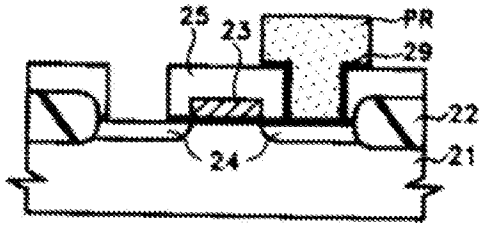


도면9

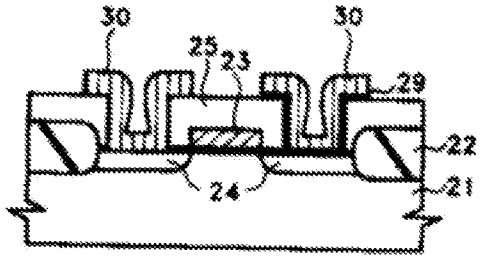


GF Exhibit 1126 - 1883/2248

도면10



도면11



GF Exhibit 1126 - 1884/2248

Unexamined Patent Publication(A)

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Requested Date of Examination	19930227
Agent.	PARK, Young Woo | Lee Young Pil | Lee Yoon Min
Inventor	Jin-U Kim
Applicant	SAMSUNG ELECTRONICS CO., LTD.
Rightholder	SAMSUNG ELECTRONICS CO., LTD.

발명의 명칭

반도체장치의제조방법

Title of Invention

SEMICONDUCTOR DEVICE

요약

본 발명은 프로그램가능한 접속소자(programmable interconnect devices;PID)용 안티퓨즈 제조방법에 관한 것이다.

본 발명에 의한 PID용 안티퓨즈 제조방법은 PID용 안티퓨즈콘택과 금속콘택을 동시에 형성하는 공정과 안티퓨즈 막질로서 금속산화막을 형성하는 공정으로 이루어지는 것을 특징으로 한다.

본 발명에 의하면, 최소한의 포토리소그래픽공정에 의해 ID용 안티퓨즈를 형성할 수 있으며, 금속산화막을 안티퓨즈막으로 사용함으로써 막질의 두께를 조절할 수 있고 누설전류를 감소시킬 수 있어 안정된 소자동작을 얻을 수 있다.

Abstract

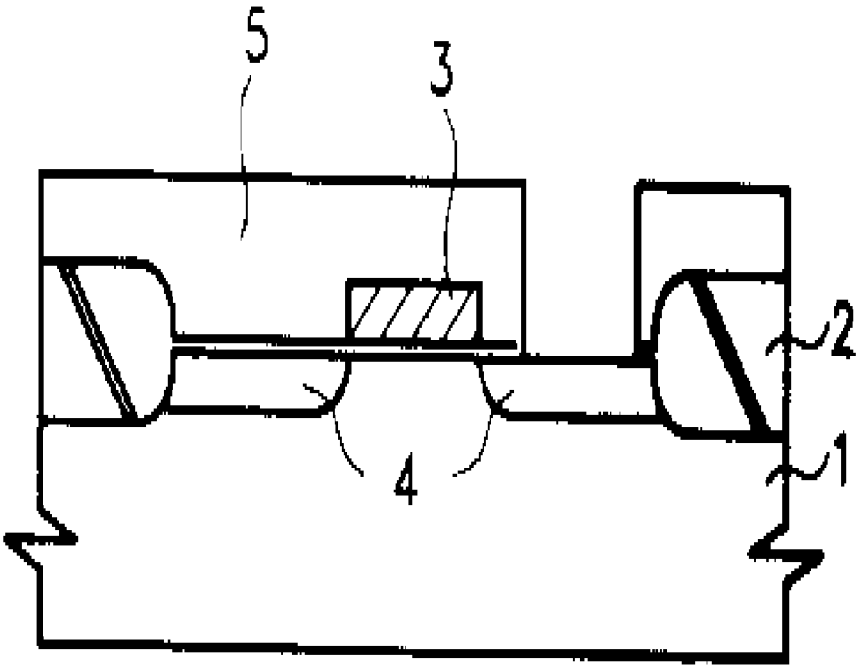
The present invention relates to the programmable method for manufacturing anti-fuse for the connection element (programmable interconnect devices:PID).

The method for manufacturing anti-fuse for PID according to the invention comprises the anti-fuse contact for PID and the process of simultaneously forming the metal contact and the process of forming the metal oxide layer as the anti-fuse thin film.

According to the invention, the anti-fuse for ID by the minimum photolithographic process is used as the anti-fuse film the metal oxide layer it can form. And the component performance controlling the thickness of the thin film and reduce the leakage current and is stabilized can be obtained.

대표도면(Representative drawing)

GF Exhibit 1126 - 1885/2248



청구의 범위

청구 1항:

반도체기판상에 하부도전층을 형성하는 공정; 상기 하부도전층상에 절연층을 형성하는 공정; 상기 하부도전층의 소정부분을 노출시키기 위해 상기 절연층에 안티퓨즈 콘택개구부 및 금속 콘택개구부를 동시에 형성하는 공정; 상기 결과물 전면에 금속산화막을 형성하는 공정; 상기 안티퓨즈 콘택영역에만 상기 금속산화막을 남기는 공정; 상기 결과물 전면에 금속을 증착한 후 이를 소정패턴으로 패터닝하여 상기 안티퓨즈 콘택영역의 상기 남아있는 금속산화막의 상부 및 상기 금속 콘택영역상에 상부도전층을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구 2항:

제1항에 있어서, 상기 금속산화막은 금속을 증착한 후 산화공정에 의해 상기 금속을 산화시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구 3항:

제2항에 있어서, 상기 금속은 Ti, Al, Ba, Ge, Sn, Be, Nb 및 Ta 중에서 선택한 어느 하나임을 특징으로 하는 반도체장치의 제조방법.

Scope of Claims

Claim 1:

The method for fabricating semiconductor device consisting of the process of forming the bottom conductive layer on the semiconductor substrate, the process of forming the insulating layer on the bottom conductive layer, the anti-fuse contact opening in the insulating layer and the process of simultaneously forming the metal contact opening part the prescribed part of the bottom conductive layer is exposed, the process of forming the metal oxide layer on the outcome front side, the process of leaving the metal oxide layer in the anti-fuse contact area, and the process of patterning this in the desired pattern after depositing the metal and forming the top conductive layer on the outcome front side on the upper portion of the above-mentioned metal oxide layer remaining of the anti-fuse contact area and metal contact area.

Claim 2:

As for claim 1, the method for fabricating semiconductor device which oxidizes the metal after depositing the metal with the oxidation process and which the metal oxide layer forms.

Claim 3:

As for claim 2, the method for fabricating semiconductor device which is characterized that the metal is any one that selects between the ti, al, ba, ge, sn, be, nb and Ta.

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청구 4항:

제2항에 있어서, 상기 산화공정은 400℃~800℃의 온도 범위에서 행하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 4:

As for claim 2, the method for fabricating semiconductor device which the oxidation process perf orms in the temperature range of 400℃~800℃.

청구 5항:

제1항에 있어서, 상기 금속산화막은 금속가스를 산소플라즈마에 통과시켜 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 5:

As for claim 1, the method for fabricating semiconductor device which passes the metal gas thro ugh in the oxygen plasma and which the metal oxide la yer forms.

청구 6항:

제1항에 있어서, 상기 상부도전층은 반도에기판에 형성된 불순물확산영역, 불순물이 도우프된 폴리실리콘층, 폴리사이드층 또는 반도체기판의 도전영역임을 특징으로 하는 프로그램가능한 접속소자의 제조방법.※ 참고사항 : 최초출원 내용에 의하여 공개하는 것임.

Claim 6:

As for claim 1, the manufacturing method of the programmable connection element which is characteriz ed being the impurity diffusion region, in which the top conductive layer is formed in the Ban DoE substrate th e polysilicon layer in which the impurity is doped, and t he conductive region of the polycide layer or the semic onductor substrate. ※ list of reference: it discloses wit h the initial application contents.

상세설명

[발명의 명칭]

반도체장치의 제조방법

[도면의 간단한 설명]

제7도 내지 제11도는 본 발명에 의한 PID용 안티퓨즈 제조방법을 도시한 공정순서도.

본 내용은 요부공개 건이므로 전문 내용을 수록하지 않았음.

Detailed Description

[Title of invention]

Method for fabricating semiconductor device.

[Brief description of drawings]

The process flowchart in which the seventh the inland eleventh drawing shows the method for manufacturing anti-fuse for PID according to the invention.

The technical content was not given mention of since this content was the main part disclosure gun.

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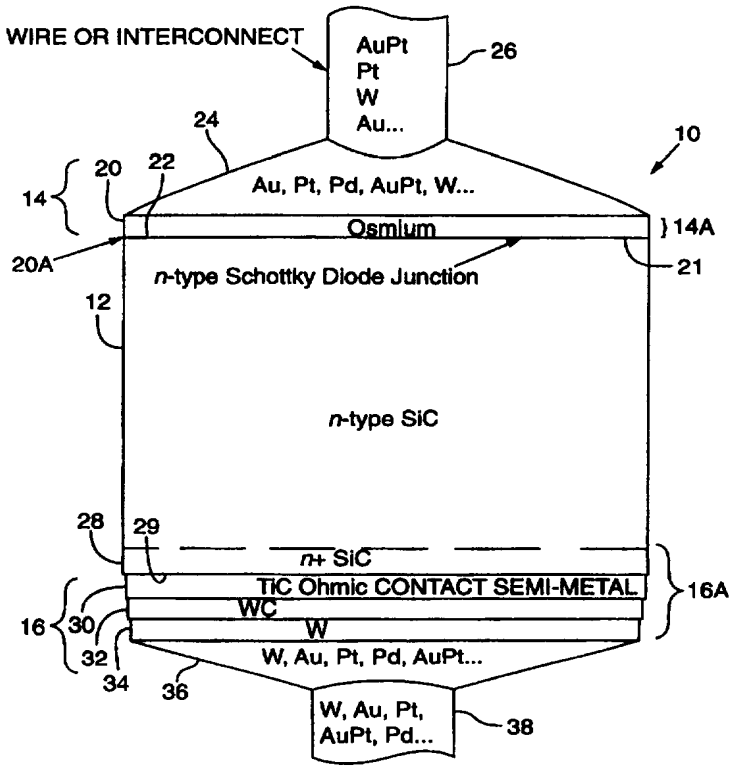
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(57) Abstract

Metallic osmium on SiC (either β or α) forms a contact that remains firmly attached to the SiC surface and forms an effective barrier against diffusion from the conductive metal. On n-type SiC (12), Os (20) forms an abrupt Schottky rectifying junction having essentially unchanged operating characteristics to at least 1050 °C and Schottky diodes that remain operable to 1175 °C and a barrier height over 1.5 eV. On p-type SiC, Os forms an ohmic contact with specific contact resistance of $<10^{-4}$ ohm-cm^2. Ohmic and rectifying contacts to a TiC layer (30) on a SiC substrate (12) are formed by depositing a WC layer (32) over the TiC layer (30), followed by a metallic W layer (34). Such contacts are stable to at least 1150 °C. Electrodes (38) connect to the contacts either directly or via a protective bonding layer (36) such as Pt or PtAu alloy.



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Os RECTIFYING SCHOTTKY AND OHMIC JUNCTION AND W/WC/TiC OHMIC CONTACTS ON SiC

BACKGROUND OF THE INVENTION

This invention relates generally to electrical contacts on SiC-based semiconductor devices. and more particularly to ohmic and rectifying contacts on silicon carbide semiconductors.

SiC possesses tremendous advantages for high temperature and high power solid state electronics. In addition, it offers potential advantages for high frequency and logic circuit applications: e.g., power conversion (mixer diodes, MESFETs), single chip computers (n-MOS, CMOS, bipolar transistors), non-volatile random access memory SiC CCDs can hold charge for more than a thousand years thus, for example, making hard disks a thing of the past.

The potential maximum average power, maximum operating temperature, thermal stability, and the reliability of SiC electronics far exceeds Si or GaAs based electronics. The degree to which these advantages of SiC can be utilized, however, is presently constrained by the thermal stability and electrical properties of the metal/SiC junctions. The primary reasons for this are: (1) the power density of SiC devices is limited by the thermal stability of the ohmic contact junctions, and (2) substantial cooling is required to insure the stability of electrical contact junctions.

For a long time, researchers have been striving without success to develop electrical contacts to silicon carbide trying overcome these constraints. Until these constraints are removed, SiC devices/circuits offer only marginal - if any - advantages over Si and GaAs. Utilization of the full performance potential of SiC itself (for all devices), requires four types of performance-limiting electrical contacts: (1) ohmic to p-type SiC, (2) ohmic to n-type SiC, (3) rectifying to p-type SiC, and (4) rectifying to n-type SiC.

The value of SiC electronics lies in its potential to extend the capabilities of solid state electronics beyond what is possible with Si or GaAs. Thus, suitable electrical contact characteristics obtained in the laboratory - under low stress conditions - must not drift or degrade, due to changes at the metal/SiC junctions, under actual device operating conditions. This requires two additional attributes of metal/SiC electrical contacts. First, the contact metal must form a junction with SiC that is chemically stable to approximately 1000°C (joule heating at high forward current densities in power SiC devices could easily cause metal/SiC junctions to reach such temperatures). Second, the contact metal (or metallization structure) must act as a diffusion barrier to circuit and bonding metals (electrode metals) at the same temperatures. Metal/SiC electrical contacts demonstrated previously do not come close to meeting all these stability requirements.

The best known p-type SiC ohmic contact metallizations demonstrated to date are Al, Al/Ti and Pt (Refs. 2,3).

Although specific contact resistances as low as $1x10^{-5}\Omega \cdot cm^2$ have been reported in laboratory studies, actual SiC devices exhibit p-type contact resistances of $1x10^{-2}\Omega \cdot cm^2$ to $1x10^{-3}\Omega \cdot cm^2$ (Refs 10, 11).

Aluminum and its silicides, and Al/Ti form thermally unstable interfaces with SiC and/or have melting problems (Ref. 12, pg. 2). Platinum reacts with SiC to form many different silicides at temperatures as low as 280°C. At temperatures as low as 400°C, Pt continues to react with SiC until it is entirely consumed by the formation of PtSi (Refs. 4, 5). Thus, Pt cannot protect its contact from circuit and bonding metal diffusion; this characteristic of Pt, in contact with SiC, requires that Pt itself not be used as a circuit or bonding metal. Further, PtSi reacts with virtually all suitable circuit and bonding metallizations at very low temperatures.

Virtually every electronic device -- unipolar or bipolar -- requires n-type ohmic contacts. The most successful n-type SiC ohmic contact metallizations demonstrated to date are Ni and TiC. Both exhibit specific contact resistances between $1x10^{-5}\Omega \cdot cm^2$ and $1x10^{-6}\Omega \cdot cm^2$ (Ni: Ref. 13; TiC: Refs. 7&9). Nickel forms silicides at very low temperatures. Its graded Ni-silicide junction is thermally unstable, and it cannot form a protective diffusion barrier to circuit and bonding metals. Other silicide, nitride, carbide-former, and multilayers of same ohmic contact approaches exhibit stability problems similar to Ni contacts. Transition metal such as Mo and W do not adhere well to SiC surfaces, and they spall at elevated

temperatures.

TiC forms an electrical ohmic contact junction with n-type SiC, that is stable to at least 1400°C (Ref. 14). However, it reacts with all candidate circuit and bonding metals at low temperatures; thus, it cannot form a protective diffusion barrier to circuit and bonding metals.

Low work function metals and semi-metals, that do not react with SiC to form tunnel junctions, can be used to form rectifying electrical contacts to p-type SiC. This type of electrical contact has not been required for SiC devices demonstrated to date; thus, there is little, if any, background literature. We have demonstrated that TiC forms an excellent rectifying contact to p-type SiC, that is stable to at least 1400° C (Ref 14.). However, it reacts with all candidate circuit and bonding metals at low temperatures; thus, it cannot form a protective diffusion barrier to circuit and bonding metals.

The n-type, rectifying Schottky diode is required to modulate the current and voltage in all majority carrier solid state devices. The most important devices of this type are Schottky diodes and MESFETs. Excellent adhesion and abrupt metal-SiC interfaces are cornerstone requirements for this type of contact. Metallizations previously developed for this purpose exhibit various deficiencies. For example, attempts to make thermally stable Schottky rectifying junctions on n-type SiC have been stymied. Many of the metals that are capable of forming such junctions (e.g., Ti, Au/Ti, Pt and PtSi) react with SiC to form silicides at relatively low temperatures,

or--in the case of Au--do not adhere to the SiC surface. The electrical contact junction is thermally unstable, leading to compositional grading of the junction interface at elevated temperatures. This grading effect is exacerbated by the creation of free carbon at the original metal/SiC interface, causing substantial performance degradation, and limiting SiC device operation to well below the capabilities of SiC itself. The (W/Ti, Ti, Au/Ti and Pt)/SiC n-type Schottky junctions demonstrated by Cree Research, N.C. State, NASA Lewis and the Japanese, are unstable at high temperatures or under sustained high current density conditions.

The best rectifying contact metal to n-type SiC, demonstrated to date appears to be W/Ti, extensively tested at the U.S. Army Res. Labs in Adelphi, MD. This contact, however, exhibited unstable leakage-current characteristics, probably due to thermally-driven reactions at the interface. The testing consisted of cycling the junctions between room temperature and 500°C (number of cycles unknown), and measuring the junction reverse leakage current I(L) at room temperature as a function of the number of cycles. During a first series of cycles, I(L) increased. During the next series of cycles, I(L) decreased, reaching a minimum value about 10 μA greater than it was before stress testing was begun. Thereafter, I(L) did not change.

U.S. Pat. No. 2,918,396 to Hall describes formation of rectifying and ohmic contacts on silicon carbide PN diodes and PNP and NPN transistors by alloying two silicon-

acceptor or silicon-donor alloy globules to an N-type or P-type silicon carbide crystal at high temperature, (1700°C). The alloying metals disclosed include aluminum, phosphorus, tungsten, molybdenum or tungsten-molybdenum, with nickel or tungsten conducting electrodes.

U.S. Pat. No. 3,308,356 to Rutz discloses a method of making rectifying contacts to PN junctions in a silicon carbide substrate bonded on one side to a tungsten block by alloying fragments of silicon doped with Ga (P-type) or As (N-type) onto the exposed face of the SiC substrate in a forming gas atmosphere (90% N, 10% H) at high temperature.

U.S. Pat. No. 3,510,733 to Addamiano discloses forming on SiC semiconductor devices electrical leads of an alloy consisting primarily of chromium and nickel, but which can include traces of Si, Fe, C and Fe.

U.S. Pat. No. 4,738,937 to Parsons describes a method of making nonrectifying (ohmic) Schottky contacts on a semiconductor substrate, such as Si or SiC, by epitaxially depositing a metal having suitable work function and lattice parameters, the identified metals including Yb on Si, $NiSi_2$ and ßW on N-type Si, and TiC on N-type ßSiC.

U.S. Pat. No. 5,442,200 to Tischler discloses forming an ohmic contact on a SiC surface by depositing a sacrificial silicon layer followed by a metal (Ni, Cr, Pd, Ti, W, Ta, Mb, Co, Zr or mixtures or alloys thereof to form a noncarbonaceous ohmic contact structure.

U.S. Pat. No. 5,448,081 to Malhi proposes a MOSFET device formed on a SiC substrate, with doped source and

drain regions but does not disclose any means for connecting electrodes to such regions.

U.S. Pat. No. 5,471,072 to Papanicolaou discloses a Pt rectifying contact and a Ti/Au ohmic contact on n-type SiC. Both forms of contacts degrade at high operating temperatures, e.g., subject to catastrophic degradation at over 800°C as disclosed and probably unstable at temperatures of 500°C or less.

Although the semiconductor materials α and ß-SiC have a demonstrated capability for stable, efficient performance at high temperatures, the same is not true of SiC devices/circuits, due to the instabilities of their electrical contact structures.

Also, applicant has learned that a TiC contact on ßSiC does not, by itself, form a diffusion barrier to circuit or bonding metals. Appropriate circuit/bonding metals such as W, Pt, Au and Pd, form intermetallics with TiC. These solid state reactions change the composition of the electrical contact junction, thus degrading it.

Accordingly, a need remains for thermally stable ohmic and rectifying electrical contacts to n-type and p-type SiC.

SUMMARY OF THE INVENTION

It is, therefore, one object of the invention to make an electrical contact to SiC; where, the contact metal exhibits the following properties:

1. Metal/SiC junction stable to over 1000°C,
2. Protects its junction with SiC from circuit and

bonding metal diffusion (forms an electrically transparent diffusion barrier) to >1000°C, and either

3. Forms an ohmic electrical contact to p-type SiC, or
4. Forms rectifying (Schottky) contact to n-type SiC.

Another object of the invention is to form an electrically transparent diffusion barrier (ETDB) for TiC electrical contacts to SiC; where, the ETDB exhibits the following properties:

1. ETDB/TiC junction is stable to over 1000°C,
2. Protects its junction with TiC from circuit and bonding metal diffusion to 1000°C; thereby, also protecting the TiC/SiC junction.

In one aspect of the invention, I have discovered that osmium (Os) forms a rectifying (Schottky) metal junction on n-type SiC semiconductor surfaces, which remains abrupt and firmly attached to at least 1050°C. A thermally stable contact structure is made by forming a metallic osmium layer on the surface of a semiconductive SiC substrate (either ß or α) and connecting a conductive metal electrode to the osmium layer through a suitable metal bonding and protective layer, such as Pt or PtAu alloy. The room temperature rectifying characteristics of this structure on n-type SiC are essentially unchanged by annealing at temperatures as high as 1050°C for 2 hours in an inert environment (Ar, hydrogen or vacuum). These junction degrade, but remain operable after annealing for 1 hour at temperatures as high as 1175°C. The resulting barrier height of Os / n-type SiC junctions is 1.78 ± 0.1 ev. Of equal importance, the Os layer forms a diffusion barrier,

which prevents diffusion of electrode metals to the Os/(n-type SiC) junction.

On P-type SiC, the Os layer will form a stable ohmic contact with the lowest specific contact resistance now possible with ohmic contacts to p-type SiC. Stable, low resistance, p-type ohmic contacts are the key to development of all SiC bipolar high temperature power electronics. Forming an Os contact on p-type SiC will provide a lower-energy tunneling barrier and thinner tunnel depth than Pt contacts on p-type SiC.

Os can also be deposited on SiO_2 to form MOS gate structures and field spreading structures. Os on SiO_2 forms a stable interface and has mechanical and thermal properties equal to those of Os on SiC.

Another aspect of the invention, is a method and structure for making an electrically transparent diffusion barrier (ETDB) which shields TiC/SiC junctions from electrode metals to 1150°C, and which forms a metallurgical junction with TiC that remains firmly attached and is stable to 1150°C. The ETDB structure consists of 2 layers: (1) a tungsten carbide (WC) layer in contact with the TiC surface, and (2) a layer of elemental tungsten (W) on the WC surface. This ETDB structure works because W is stable in contact with WC at a temperature greater than 1150°C. The TiC/SiC junction remains stable because W does not react with WC to form W_2C in this temperature range (unlike all other transition metals in contact with their mono-carbides). Thus, a concentration gradient to drive diffusion between the WC/TiC, and thus, TiC/SiC interfaces

does not exist. 1.78Elemental W is the actual diffusion barrier. It forms a bond with potential electrode metals because of solid solubility which increases with increasing temperature. Once "formed", the thin bonding layer is absolutely stable at or below the forming temperature. Electrodes can then be freely connected to this contact layer either directly or though a suitable intermediate bonding layer such as Pt or PtAu alloy. Such contacts are stable to at least 1050°C.

The invention enables fabrication of SiC devices and circuits that will not degrade, or become unstable, under all strain conditions (thermal, electric field, mechanical) for which SiC itself can perform as a semiconductor device. This invention removes all restrictions imposed by metal contacts on the operating envelope of SiC solid state device technology. In particular, it provides rectifying (Schottky) junctions and ohmic contacts that will withstand sustained exposure to temperature as high as 1150°C, and electron migration effects at high electric fields.

Os forms a rectifying Schottky junction to n-type SiC, as do several other metals. Os is set apart from all other metals by the following characteristics: (1) it forms an electrically transparent diffusion barrier to 1050° C {which protects the junction from diffusion of electrode metals}, (2) the Os/SiC junction itself remains stable to 1050°C, and (3) the electrical properties of the junction do not change after sustained exposure to temperatures as high as 1050°C. Os will form an ohmic contact junction to p-type SiC exhibiting the same unique stability characteristics

as the n-type SiC rectifying junction.

W/WC is an electrically transparent diffusion barrier, which forms a stable junction with TiC to 1150°C. Its purpose is to protect the chemical and electrical integrity of the TiC/SiC junction. TiC forms ohmic contact junctions to n-type SiC; and rectifying contact junctions to p-type SiC. The TiC/SiC junction, by itself, is stable to temperatures greater than 1400°C.

Based on the foregoing developments, applicant has developed a family of high temperature/power semiconductor devices which satisfy a number of unmet commercial needs. One immediate application is thermal sensors. The invention can be used to make junction or resistive thermistors, that measure temperatures to 1922°F (>1050°C), and 2100°F (1150°C). This development permits SiC thermistors to compete, for the first time, with thermocouples, oxide resistors and pyrometers in the temperature range of 300°F to 2100°F (150°C to 1150°C). It also enables the manufacture of hostile environment transducers, operable at temperatures above 460°F (238°C).

The invention enables making Schottky diodes, PN diodes and transistors as either discrete devices or as components of integrated circuits. Importantly, the invention opens up many potential applications in the power conditioning and conversion field, such as power rectifiers for converting AC power to clean DC power. N-SiC Schottky rectifiers could handle powers nearly as high as the best Si PN junction rectifiers, and PN junction SiC rectifiers could replace vacuum tubes. Other types of devices include

bipolar transistors, thyristors, MOSFETs, MESFETs, IGBTs, and mixer diodes for use in communications, as well as digital and analog to digital electronics.

In summary, all solid state semiconductor devices require one, or more, of the four electrical contacts discussed, which the present invention makes possible.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of a preferred embodiment of the invention which proceeds with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional diagram of a vertical n-type SiC Schottky diode structure made using prior electrical contacts, showing blurring (interdiffusion) of junctions that results from operation at temperatures greater than 300°C.

FIG. 2 is a cross-sectional diagram of a vertical n-type SiC Schottky diode structure made according to the present invention., as fabricated, and after sustained operation at temperatures up to 1050°C.

FIG. 3 is a cross-sectional diagram of a vertical SiC PN diode structure made according to the present invention.

FIGS. 4A, 4B, 4C, 4D and 4E are cross-sectional views showing the photolithography, Si deposition and osmium deposition and annealing to form a vertical n-type SiC Schottky diode (with electric field spreading SiO_2 ring) on the upper surface of the an n-type SiC substrate, in an Os/SiC n-Schottky diode fabrication process according to

the invention.

FIG. 5 is a top plan view of the diode structure formed by the fabrication process of FIGS. 4A, 4B, 4C, 4D and 4E; and an edge view of the diode structure.

FIG. 6 is a cross-sectional view of the diode of FIG. 5 after applying a platinum layer over the osmium layer.

FIG. 7 is a perspective view of a planar NPN bipolar transistor on a SiC substrate with an Os base contact and W/WC/TiC emitter and collector contacts in accordance with the invention.

FIGS. 8A and 8B are cross-sectional views of two MESFET structures formed on a semi-insulating SiC substrate with an Os/Si gate contact and W/WC/TiC ohmic source and drain contacts in accordance with the invention.

FIGS. 9A and 9B are cross-sectional views of N-channel and P-channel MOSFETs formed on a semiconducting SiC substrate with an Os/oxide gate structure and respective W/WC/TiC or Os ohmic source and drain contacts, in accordance with the invention.

FIGS. 10A and 10B are cross-sectional views of gate controlled thyristor/SCR/IGBT devices with W/WC/TiC, Os and Os-on-oxide contacts in accordance with the invention.

DETAILED DESCRIPTION

Referring to FIG. 1, applicant herein has experimented extensively trying to make devices are cross-sectional views of two versions of MESFET structures formed on a SiC substrate with an Os/Si gate contact and W/WC/TiC source and drain contacts in accordance with the invention.based

on the TiC/SiC metallic/semiconductor combination described in his prior U.S. Pat. No. 4,738,937. FIG.1 illustrates the problems encountered in trying to make contacts to both the upper SiC surface and the lower TiC surface of the structure. Even if the metal layers applied to such surfaces form clean, abrupt interfaces in their as-deposited state, the boundaries of these interfaces blur when the devices are annealed due to diffusion into and/or reactions with: (1) the silicon carbide (top rectifying junction, and (2) the TiC ohmic contact.

Schottky Diode with Os Schottky and TiC/WC/W Ohmic Contacts

Referring to FIG. 2, the present invention is described with reference to the fabrication of a vertical Schottky diode 10 formed on a silicon carbide (SiC) substrate 12, with a Schottky rectifying junction and contact structure 14 formed on an upper side thereof, and an ohmic contact structure 16 formed on an opposite or lower side thereof. The starting material is a single-crystal wafer of uniformly-doped, N-type SiC, designated as substrate 12. First, the n^+-SiC/TiC/WC/W structure 16A is formed (in which TiC = ohmic contact semi-metal; WC/W = ETDB); then, the Schottky rectifying junction and ETDB structure 14A is formed, by the processes described in further detail below together with examples of suitable dimensions of the various layers that form the contact structures. Subsequently, wires may be bonded to the structure to complete contact structures 14 and 16 as shown, or circuit metals may be deposited on and reacted with the ETDB surfaces to complete the structure. In

either case, the resulting contacts will be thermally stable to 1050°C (contact structure 14) and 1150°C (contact structure 16).

The Schottky rectifying junction and ETDB structure 14A preferably comprises a very thin layer 20A of Si (≥ 1 monolayer). The purpose of this layer is to permit Os to bond to the SiC surface 22 without creating a monolayer of free carbon. A layer 20 of osmium then deposited on and in contact with the upper surface 22 of substrate 12. The interface of the osmium layer with substrate 12 forms a Schottky rectifying junction 21, once the structure is annealed ("formed") at a temperature approximately equal to or greater than or 900°C. Preferably, layer 20 consists of elemental osmium (Os), but some impurities can be included, due to mixing of osmium and bonding/circuit metals at the exposed Os surface due to solid solubility, and a few monolayers of OsSi will form between the Os and the SiC when structure 14 is completed.

A metal protective cap and bonding layer 24 is formed on and in contact with the osmium layer 20. A first circuit metallization or wire 26 is electrically and mechanically connected to the upper side of the device 10 via the bonding layer 24. The bonding layer 24 preferably comprises a layer of gold (Au) or gold-platinum (AuPt) alloy, although other known electrical contact metals can be used, in particular tungsten or tungsten-platinum, but any metal selected from a group consisting of Pt, Pd, W, Ti, Hf, Zr, Au, PtAu, V, Cr, Fe, Ni, Cu, Nb, Mo, Tc, Ru, Rh, Ag, Ta, Re, Ir, can be used. The circuit metallization

or wire 26 is preferably tungsten (W), although an alloy of tungsten can also be used, as well as other metals compatible with the bonding metals and intended operating temperatures and environments. The use of Os removes all restrictions on the bonding/circuit metal type, method of application and the bond "forming" temperature.

The ohmic contact structure 16 on the underside of the substrate 12 includes a tungsten carbide (WC) layer 32 deposited on the TiC layer 30. Preferably, the structure of the Schottky diode 10 includes an n+ doped SiC layer 28 on the underside of the n-type substrate, with the TiC layer 30 contacting the lower surface 29 of layer 28 to form an ohmic contact. Tungsten carbide layer 32 covers the TiC layer 30 and a layer 34 elemental tungsten(W) is in turn deposited on the WC layer 32. A bonding layer 36 on the tungsten layer 34 connects a second circuit metallization or wire 38 to the device. The bonding layer 36 is preferably of PdAu or PtAu, but could alternatively be made of W, Pt, Pd, Au, or any other compatible electrical contact metals. The wire 38 is preferably tungsten but could alternatively be Pt, PtAu, Au, Pd or other compatible metals.

This structure forms a highly stable Schottky diode which remains stable under high temperature conditions, over 1050°C without discernible changes in I-V characteristics, and operative as a Schottky diode after annealing at temperatures up to about 1175°C.

Using elemental osmium to form the Schottky junction and ETDB structure 14A on N-type SiC ($n \leq 1x10^{18}cm^{-3}$)

produces the highest known barrier height: 1.78 ± 0.1 electron volts, as compared to a range of 1.1 to 1.2 ev. for prior Schottky junctions in SiC. The Os/n-SiC junctions will block substantially higher voltages than possible with any other known metal.

The physical properties of the Os/SiC interface are also advantageous, with good interface adhesion and expansion coefficient mismatch characteristics that will readily exceed device/circuit requirements, and so does not spall. The osmium film remains smooth after annealing, and does not scratch or peel. The osmium layer additionally provides a diffusion barrier to circuit metallizations that is effective to temperatures of at least 1050°C. Os will form an interface with SiC and a diffusion barrier that is stable over a broader range of thermal, electrical and mechanical stresses than any other known metals. Also, Os does not react with SiO_2, when annealed in H_2 in the absence of oxygen at up to 1050°C. Thus, the use of osmium is compatible with MOS fabrication processes and can readily be used as a gate metal over oxide, as shown in FIGS. 9A and 9B.

The ohmic contact structure 16 with WC layer 32 covering the TiC layer 30 and layer 34 of elemental tungsten (W) on the WC layer 32 forms a highly advantageous ohmic contact on the SiC substrate. It forms an electrically transparent interface to the substrate onto which it is practical to deposit all known electrical contact metals. It provides a very

hard surface as well as an effective diffusion barrier to circuit metallizations to at least 1150°C. It forms a stable interface that does not diffuse into the TiC layer or the SiC substrate, unlike other metals applicant has tried (e.g., Au, Ag, Ti). The W/WC layers form a diffusion barrier which is stable over a broader range of thermal, electrical and mechanical stresses than any other known metals. The WC layer 32 in contact with the TiC layer 30 stabilizes the TiC/SiC junction to about 1150°C. The W layer 34 on the WC layer stabilizes the WC/TiC junction to about 1150°C.

PN Diode with Osmium Ohmic Contact

Referring next to FIG. 3, the invention can also be used to form contacts on semiconductor devices comprising multiple layers of opposite dopant types, such as a vertical pn diode 40. Much of the structure shown in FIG. 3 is similar to that of FIG. 3, so similar reference numerals are used wherever applicable to identify like features already described above. The main difference is that the substrate is doped to form two dopant-type regions or layers, a p-type layer 12A and a n-type layer 12B, interfacing at a pn junction 42. The p-type layer is formed in the upper portion of the substrate to form a nonrectifying ohmic junction 41 at upper surface 22, instead of the Schottky junction described above, and can include a p+ region adjacent surface 22. Another difference between this ohmic contact and ETDB structure 14B and the Os/n-SiC

rectifying Schottky contact and ETDB structure 14A, is that the Si layer is not required in structure 14B. This is because a few monolayers of free carbon at the Os/SiC junction will not have any detrimental effects on the ohmic contact performance.

The ohmic junction 41 between the osmium layer 20 and the p-type SiC material 12A should exhibit a specific contact resistance of 10^{-4} ohm-cm^2 or less. Tests of a statistically significant sample of prototype devices consistently demonstrated low specific contact resistance (high 10^{-5} ohm-cm^2 range for both 4H- and 6H-SiC) of different crystallographic orientations, and thermally stable metal/SiC junction (>1050°C). The diffusion and mechanical properties of Os/SiC ohmic contacts are identical to those of the above-described Schottky contacts.

Description of Schottky Diode Fabrication Process

Following is a description of a process for making a vertical n-type SiC Schottky diode, as shown in FIGS. 5 and 6, with a field spreading ring, as shown in FIGS. 4A, 4B, 4C, 4D, 4E, 5 & 6, starting with a uniformly doped, n-type SiC, single crystal wafer (thickness ≈ 400 μms) as substrate 12. NOTE: the W/WC layers must be deposited and annealed before processing of the Os/n-SiC contact structure begins.

1. Deposit (or ion implant nitrogen and activate) approximately 100 Å to 1,000 Å of n+ SiC on one (bottom) side of substrate 12.

Cold wall chemical vapor deposition (CVD) @ 1400°C in diluent hydrogen.

Reactants: silane and ethylene for SiC growth, and ammonia as the nitrogen source for n-type doping ($n \approx\geq$ 1E18/cc).

No fundamental limit on layer thickness (>0 to ∞).

1A. On the top (opposite) n-type SiC surface, grow native oxide in wet oxygen at 1100-1250°C. Any other oxide formation procedure can be used.

2. Deposit approximately 700 Å of TiC on the n+ SiC (bottom) surface.

CVD @ 1290°C in diluent hydrogen; this temperature anneals the TiC as it is formed.

Reactants: titanium tetrachloride (Ti source) and ethylene (carbon source).

TiC thickness should be less than about 1,800 Å, or it will begin to introduce strain into the SiC layer (Ref. 14).

3. Perform photolithography and oxide etching procedures as shown in FIGS. 4A and 4B to mask the opposite (upper) SiC surface such that an array of circular areas are exposed on the SiC upper surface and each exposed SiC circle is surrounded by an annular oxide ring (the remainder of the

surface is covered with photoresist). The diameters of the exposed SiC circles in experimental devices were 20, 40, 80 and 200 μms.

3B. For the rectifying n-type contact only, we should have RF sputtered a few monolayers of Si on the structure shown in FIG. 4C.

4. Deposit approximately 1,000 Å of Os (>99% purity) on the masked SiC and oxide field ring surfaces. RF sputter deposit Os in a vacuum, as shown in FIG. 4D, after 20 sec. in-situ Ar sputter cleaning of the SiC surface. Note: Os can also be deposited by CVD, DC sputtering or electroplating.
No fundamental limit on layer thickness (>0 to ∞).

5. Remove photoresist mask (lift-off) and clean SiC surface containing circular Os diodes, as shown in FIG. 5.

6. Deposit ~400 Å of WC on TiC surface.
Reactive sputtering: DC sputter W and react with hydrocarbon gas to form WC at the TiC surface.
No fundamental limit on WC thickness (> 0 to ∞).

7. Deposit ~400 Å of W (>96% purity; >99.9% preferred) on WC surface, as shown in FIG. 2.
DC sputtering in vacuum.

8. Deposit ~150 Å Pt (or W, Pd, Au, Cu, Ni, etc.) cap over Os as shown in FIGS. 4E and 6. The cap serves several purposes: (1) protect Os from oxidation (Pt does not oxidize at any temperature, but Os forms a volatile oxide at about 160°C), (2) circuit metal, (3)

part of a bonding layer (electrode).

DC sputtering in vacuum.

9.1 Anneal structure at ≤1150°C, if Os/OsSi/SiC junction is desired.

9.2 Anneal structure at ~1000°C to obtain a thin OsSi layer and a fully formed Os/SiC junction. Annealing at 1000°C bonds Pt cap to Os surfaces to protect Os from oxidation; also bonds W layer to WC layer.

10. Continuation of the structure can be performed by standard techniques.

Description of PN Diode Fabrication Process

Following is a description of the process for fabrication of a vertical p+-n SiC diode as shown in Fig. 3, starting with a uniformly doped, n-type SiC, single crystal wafer (thickness ≈ 400 μms). Photolithography steps to define device shape and field spreading ring can be performed as shown in FIGS. 4A, 4B, 4C, 4D, 4E & 5.

1. Deposit approximately 1,000 Å of p+-SiC on one side.

Cold wall chemical vapor deposition (CVD) @ 1400°C in diluent hydrogen.

Reactants: silane and ethylene for SiC growth, and dimethylaluminum hydride as the A1 source for p-type doping [p ≥ 1E18/cc].

2. Deposit approximately 1,000 A of n+-SiC on opposite side.

Cold wall chemical vapor deposition (CVD) @ 1400°C

in diluent hydrogen. Reactants: silane and ethylene for SiC growth, and ammonia as the nitrogen source for n-type doping [n ≈ 1E18/cc].

No fundamental limit on layer thickness (> 0 to ∞).

3. Deposit approximately 700 Å of TiC on the n+-SiC surface.

CVD @ 1250°C in diluent hydrogen. Reactants: titanium tetrachloride (Ti source) and ethylene (carbon source).

TiC should be less than about 1,800 Å, or it will begin to introduce strain into the SiC layer(Ref. 14).

4. Deposit approximately 1,000 Å of Os on the p+-SiC surface.

DC sputter deposit Os in a vacuum, after 20 sec. in-situ Ar sputter cleaning of the SiC surface.

No fundamental limit on Os layer thickness (> 0 to ∞). Then deposit ~150 Å Pt cap over Os.

CVD or electroplating also can be used.

5. Deposit ~400 Å of WC on TiC surface.

Reactive sputtering: DC sputter W and react with hydrocarbon gas to form WC at the TiC surface.

No fundamental limit on WC thickness (>0 to ∞).

6. Deposit ~400 Å of W on WC surface.

DC sputtering in vacuum.

7. Anneal structure at ≤1150°C.

8. Continuation of the structure can be performed by standard techniques.

Other SiC Devices Using Os and Ti/WC/W Contacts

The basic solid state semiconductor devices used as building blocks for solid state electronic circuits are resistors, diodes, transistors and thyristors. All of these can be made in SiC using the contact structures of the present invention, using the foregoing processes.

RESISTORS:

Majority carrier devices requiring at least two spaced p-type or two spaced n-type ohmic contacts. Examples include varistors and resistance thermistors. A typical lateral form of such devices can be that of the MESFETs further described below with reference to FIGS. 8A and 8B but without a gate contact. Vertical varistors and resistance thermistors can be made in the manner shown in FIG. 2 but with ohmic contacts 16 at both ends.

Applications include temperature transducers operable over temperature ranges from 100°C. to at least 1050°C. for Os ohmic contacts on p-type devices and to 1150°C. for TiC/WC/W ohmic contacts on n-type devices.

DIODES:

Majority carrier diodes (p-type & n-type) require an ohmic and a rectifying metal contact, as described above with reference to FIGS. 2, 5 and 6. Examples include junction thermistors (thermal sensors) mixers (communications), ultrafast recovery (power conditioning), light emitting displays (LEDs).

Minority carrier diodes (p^+n & n^+p and pin) require

both n-type and p-type ohmic contacts, as described above with reference to FIG. 3. The range of applications and types of devices are enormous (see e.g. Sze). Such diodes are used for thermal sensing, power conditioning, power conversion, radiation detection and LED display electronics.

TRANSISTORS:

Bipolar transistors are minority carrier devices with two p-n junctions. They require two n-type and one p-type, or vise-versa, contacts. While the applications range is enormous, bipolar transistors are best known for use in TTL (transistor-transistor-logic). Referring to FIG. 7, an npn bipolar transistor 50 is shown. It includes an Os ohmic contact 52 to the p-type base region 54, preferably capped with Pt as shown in FIG. 6, a TiC/WC/W ohmic contact 56 to the emitter region 60 and a TiC/WC/W ohmic contact 58 to collector region 62 via n+ layer 62.

Unipolar transistors, commonly referred to as MESFETs (metal-semiconductor FETs) are majority carrier devices (usually n-type, but can be p-type). Two such devices are shown in FIGS. 8A and 8B. MESFET 70A in FIG. 8A is formed by diffusing n++ source and drain contact regions 72A, 74A into an n-channel layer 76 epitaxially-deposited on a semi-insulating SiC substrate 78. MESFET 70B in FIG. 8B is formed by epitaxially-depositing an n++ source and drain layer on channel layer 76 on a semi-insulating SiC substrate 78, and then dividing the n++ layer into separate source and drain contact regions 72B, 74B by etching a channel down to layer 76B prior to forming gate structure

82B. The source and drain each use an ohmic contact: in the illustrated example, this is the TiC/WC/W ohmic contact 80, made in the form of the contact structure 16 shown in FIGS. 2 and 3, on the n++ regions 72B, 74B. The gate requires a Schottky rectifying contact 82 which is provided by the Os contact 14 of the form shown in FIG. 6. The gate structure is formed in the same manner as the Schottky contact 14 shown in FIGS 4A-4E. In similar manner, a p-channel MESFET can be formed using p++ source and drain regions, a p-type channel, Os source and drain contact structures, and a TiC/WC/W rectifying gate contact over the p-channel. The MESFET Applications include power conversion (DC to high frequency), generally used for high frequency communications and radar.

MOSFET (depletion & inversion). Requires ohmic contacts to source and drain, parasitic p-n junction and back contact. FIGS. 9A and 9B respectively show n-channel and p-channel MOSFET devices, 88A, 88B. In FIG. 9A, the n-channel device 88A has n-type source and drain regions 90A, 92A formed in a p-type SiC substrate 94A. W/WC/TiC ohmic contacts 96 are formed over regions 90A, 92A, in the manner described above. In the p-channel device 88B, n-type source and drain regions 90B, 92B are formed in a p-type SiC substrate 94B. The source and drain regions 90B, 92B have Os ohmic contacts 98, as described above. In both devices 88A and 88B, the MOSFET gate is formed by a thin oxide layer 97 positioned over the channel between the source and drain regions and covered by a conductive Os layer 99. The use of Os as a gate metal on an oxide layer

could have significant advantages for creating n-channels in p-type SiC. Osmium has good adherence to SiO_2 and is highly conductive.

THYRISTORS (and GTO, IGT, IGBT, etc. devices):

Having three p-n junctions, these devices are typically used for power conditioning. Thyristor structures can requires as many as four ohmic contacts. MOS-gated and IGBT-type devices are essentially thyristors or silicon controlled rectifiers (SCRs) with capacitively coupled control electrodes, i.e. a MOSFET gate, as shown for example, in U.S. Pat. Nos. 3,831,187 to Neilson; 4,199,774 to Plummer; and 4,364,073 to Becke, and further described in Ref. 16. Such devices typically require ohmic contacts to the MOSFET source and drain, and ohmic contacts to the n and p sides of the two non-shorted junctions in order to control the voltage bias and polarity at each junction, as well as a MOS gate.

Examples of such devices are shown in FIGS. 10A and 10B. The illustrated vertical devices 100A, 100B are similar in overall arrangement, both being formed on an n-type SiC substrate 102 with an n+ buffer layer 104 and a p+ anode region 106 and an Os ohmic contact layer 108 capped by a Pt protective bonding layer 110. The MOS-gated structures on the opposite side of the device are also similar, having Ti/WC/W ohmic contacts 112 to the n+ source and drain regions 114 and also forming a tunneling junction short or field emission contact to p+ portions of the base or body regions 116 associated with each region 114. Alternatively, the Ti/WC/W ohmic contacts 112 can be

connected to the n+ source and drain regions 114 alone and an Os ohmic contact portion 112B can be connected to the adjoining P-type base in electrical contact to Ti/WC/W ohmic contacts 112. The MOS gate structure in device 100A is planar, similar to that of FIGS. 9A and 9B, with an oxide layer 118A and a platinum-capped Os electrode layer 120A forming the MOS gate contact. The MOS gate structure in device 100B is recessed in a trench formed between the source and drain regions, with an oxide layer 118B and a platinum-capped Os electrode layer 120B lining the sidewalls of the trench to form the MOS gate contact along the sidewalls adjacent the p-body.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. While the devices shown herein are vertical and lateral devices formed on planar substrates, with the contacts either on both sides or spaced apart on one side of the substrate, other surface arrangements may be used, for example, a V-shaped notch or U-shaped trench, for placement of the claimed contacts. I claim all modifications and variation coming within the spirit and scope of the following claims.

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CLAIMS

1. A SiC semiconductor device comprising:

a semiconductor substrate comprising silicon carbide having a first surface and a second surface, the substrate including a first doped region adjacent the first surface and a second doped region adjacent the second surface;

a first conductive layer comprising metallic osmium (Os) contacting the first surface to form a first contact having an electronic interface to the first region; and

a second layer comprising a metal contacting the second surface to form a second electronic contact to the second doped region.

2. A SiC semiconductor device according to claim 1 in which the first region is doped n-type, and the first contact forms a Schottky junction as said electronic interface.

3. A SiC semiconductor device according to claim 2 in which the first conductive layer includes a thin film of Si or OsSi interfacing the metallic osmium to the first surface of the silicon carbide substrate.

4. A SiC semiconductor device according to claim 1 in which the first and second regions are doped n-type, the first contact forms a Schottky junction and the second contact forms an ohmic junction.

5. A SiC semiconductor device according to claim 4 in which the first and second regions and intervening portions of the substrate are doped n-type, the first contact forms a Schottky junction and the second contact

forms an ohmic junction, so that the device acts as a Schottky diode.

6. A SiC semiconductor device according to claim 1 in which the first region is doped p-type, and the first contact forms an ohmic junction as said electronic interface.

7. A SiC semiconductor device according to claim 6 in which the second region is doped n-type, to form a pn junction at an interface between said regions.

8. A SiC semiconductor device according to claim 7 in which the second layer includes:

a titanium carbide (TiC) layer contacting the second surface;

a tungsten carbide (WC) layer covering the titanium carbide (TiC) layer; and

a layer consisting essentially of elemental tungsten contacting the tungsten carbide (WC) layer.

9. A SiC semiconductor device according to claim 1 in which the first and second regions are doped to a first dopant type and an intervening portion of the substrate is doped to an opposite dopant type to form a first pn junction at an interface adjoining the first region and a second pn junction at an interface adjoining the second region.

10. A SiC semiconductor device according to claim 1 in which the first region is doped to a first dopant type and the second region is doped to a second, opposite dopant type, and an intervening portion of the substrate is doped to form a first pn junction at an interface adjoining the

first region, a second pn junction at an interface adjoining the second region and a third pn junction within the intervening portion.

11. A SiC semiconductor device according to claim 1 including a layer of a protective metal covering the Os first conductive layer, selected from a group of conductive metals that is protective of the Os layer against oxidation and adapted to bond to an osmium surface.

12. A SiC semiconductor device according to claim 1 including a layer of a protective metal selected from a group consisting of Pt, Pd, W, Au, PtAu, Ti, Zr, Hf, V, Cr, Fe, Ni, Cu, Nb, Mo, Tc, Ru, Rh, Ag, Ta, Re, Ir.

13. A SiC semiconductor device according to claim 1 in which the second conductive layer comprises metallic osmium (Os).

14. A SiC semiconductor device according to claim 13 in which the first and second regions and intervening portions of the substrate are doped p-type so that the first contact and the second contact each form an ohmic junction and the device acts as a resistive device.

15. A SiC semiconductor device according to claim 13 in which the first and second regions and an intervening portion of the substrate are doped p-type so that the first contact and the second contact each form an ohmic junction and a gate structure contacts a third surface portion contacting the intervening portion of the substrate so that the device acts as field effect transistor.

16. A SiC semiconductor device according to claim 13 in which the first and second regions of the substrate are doped p-type so that the first contact and the second contact each form an ohmic junction, and an intervening portion of the substrate is doped n-type to form a pn junction with at least one of said first and second regions.

17. A SiC semiconductor device according to claim 13 including a contact coupled to the intervening portion of the substrate so that the device acts as a transistor.

18. A SiC semiconductor device according to claim 17 in which the first and second regions are doped p-type and the intervening region is doped n-type and contact coupled to the intervening portion comprises a material which forms an ohmic contact therewith so that the device is operable as a bipolar transistor.

19. A SiC semiconductor device according to claim 17 in which the first and second regions are doped p-type and the contact coupled to the intervening portion includes a third metallic layer overlying an insulative layer to form an insulated gate over the intervening portion so that the device is operable as a field effect transistor.

20. A SiC semiconductor device according to claim 19 in which the third conductive layer includes an Os layer.

21. A SiC semiconductor device according to claim 19 in which the third conductive layer includes:

a titanium carbide (TiC) layer the insulative layer;

a tungsten carbide (WC) layer covering the titanium carbide (TiC) layer; and

a layer consisting essentially of elemental tungsten contacting the tungsten carbide (WC) layer.

22. A SiC semiconductor device according to claim 17 in which the first and second regions are doped p-type and the contact coupled to the intervening portion includes a conductive layer contacting a surface of the intervening portion so that the device is operable as a transistor.

23. A SiC semiconductor device according to claim 22 in which the contact coupled to the intervening portion includes:

a titanium carbide (TiC) layer contacting the a surface portion of the intervening layer;

a tungsten carbide (WC) layer covering the titanium carbide (TiC) layer; and

a layer consisting essentially of elemental tungsten contacting the tungsten carbide (WC) layer;

the intervening layer being doped p-type so that the device is operable as a transistor.

24. A SiC semiconductor device according to claim 22 in which the contact coupled to the intervening portion includes an Os layer contacting the a surface portion of the intervening layer.

25. A SiC semiconductor device according to claim 1 in which the second layer includes:

a titanium carbide (TiC) layer on the second surface;

a tungsten carbide (WC) layer on the titanium carbide (TiC) layer; and

a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

26. A SiC semiconductor device comprising:

a semiconductor substrate comprising silicon carbide having a first surface and a second surface, the substrate including a first doped region adjacent the first surface and a second doped region adjacent the second surface;

a first conductive layer comprising a first contact metal layer on the first surface to form a first contact having an electronic interface to the first region; and

a second conductive layer contacting the second surface to form a second electronic contact to the substrate, the second layer including:

a titanium carbide (TiC) layer contacting the second surface;

a tungsten carbide (WC) layer covering the titanium carbide (TiC) layer; and

a layer consisting essentially of elemental tungsten contacting the tungsten carbide (WC) layer.

27. A SiC semiconductor device according to claim 26 in which the second region is doped n-type, and the second contact forms an ohmic junction.

28. A SiC semiconductor device according to claim 26 including a layer of a bonding metal contacting the tungsten layer, selected from a group of conductive metals that is adapted to bond to a tungsten surface.

29. A SiC semiconductor device according to claim 26 including a layer of a bonding metal contacting the tungsten layer, the bonding metal being selected from a group consisting of Pt, Pd, W, Au, PtAu, V, Ti, Zr, Hf,

Cr, Fe, Ni, Cu, Nb, Mo, Tc, Ru, Rh, Ag, Ta, Re, Ir.

30. A SiC semiconductor device according to claim 26 in which the second region is doped p-type, and the second contact forms a rectifying junction.

31. A SiC semiconductor device according to claim 26 in which the first layer includes:

a titanium carbide (TiC) layer on the first surface;

a tungsten carbide (WC) layer on the titanium carbide (TiC) layer; and

a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

32. A SiC semiconductor device according to claim 31 in which the first and second regions and intervening portions of the substrate are doped n-type so that the first contacts and the second contact each form an ohmic junction and the device acts as a resistive device.

33. A SiC semiconductor device according to claim 31 in which the first and second regions are doped n-type and a contact is coupled to an intervening portion of the substrate, the contact including a third conductive layer overlying an insulative layer to form an insulated gate over the intervening portion so that the device is operable as a field effect transistor.

34. A SiC semiconductor device according to claim 33 in which the conductive layer overlying the insulative layer includes:

a titanium carbide (TiC) layer on the insulative surface;

a tungsten carbide (WC) layer on the titanium carbide

(TiC) layer; and

a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

35. A SiC semiconductor device according to claim 33 in which the conductive layer overlying the insulative layer includes a layer of Os contacting the insulative layer.

36. A SiC semiconductor device according to claim 31 in which the first and second regions are doped n-type and a contact is coupled to an intervening portion of the substrate, the contact including a conductive layer contacting a surface of the intervening portion so that the device is operable as a transistor.

37. A SiC semiconductor device according to claim 36 in which the conductive layer includes:

a titanium carbide (TiC) layer on the surface of the intervening portion;

a tungsten carbide (WC) layer on the titanium carbide (TiC) layer; and

a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

38. A SiC semiconductor device according to claim 36 in which the conductive layer includes a layer of Os contacting the surface of the intervening region.

39. A SiC semiconductor device according to claim 36 in which the intervening portion of the substrate is doped p-type so that the device is operable as a bipolar transistor.

40. A SiC semiconductor device according to claim 36 in which intervening portion of the substrate is doped n-type so that the device is operable as a MESFET.

41. A SiC semiconductor device according to claim 40 the contact contacting a surface portion of the intervening portion comprises an Os layer.

42. A SiC semiconductor device according to claim 31 including a contact coupled to an intervening portion of the substrate so that the device acts as a transistor.

43. A SiC semiconductor device according to claim 42 in which the gate contact material includes a third conductive layer overlying an insulative layer to form an insulated gate over the intervening portion so that the device acts as a field effect transistor.

44. A SiC semiconductor device according to claim 26 in which the first region is doped p-type and the first conductive layer is formed of a material suitable to form an ohmic contact with the first region, the second region is doped n-type to form an ohmic contact to the second layer, and the substrate includes a first n-type intervening portion adjoining the region and a second p-type intervening portion adjoining the second region of the substrate so as to define a four-layer device having three pn junctions electrically coupled between said first and second conductive layers.

45. A SiC semiconductor device according to claim 44 in which the first conductive layer comprises an Os layer contacting the first region.

46. A SiC semiconductor device according to claim 44 including a third conductive layer contacting a surface of one of the intervening portions.

47. A SiC semiconductor device according to claim 46 in which the third conductive layer comprises one of an Os layer and a TiC/WC/W layer.

48. A SiC semiconductor device according to claim 44 in the third conductive layer is capacitively coupled to a surface of one of the intervening portions.

49. A SiC semiconductor device according to claim 48 in which the third conductive layer comprises one of an Os layer and a TiC/WC/W layer.

50. A method of forming an electrical contact to a surface of SiC semiconductor substrate comprising:

depositing a layer comprising metallic osmium (Os) on an area of the substrate surface to form a contact having an electronic interface to the substrate; and

forming a protective cap over the osmium layer.

51. A method according to claim 50 including annealing the substrate after depositing the Os layer to bond the Os layer to the SiC substrate at said surface.

52. A method according to claim 51 including doping a portion of the substrate in said area with an n-type impurity so that the Os layer and the n-type doped substrate portion form a rectifying Schottky junction.

53. A method according to claim 52 including depositing a thin silicon layer on the substrate surface in said area prior to depositing the Os layer.

54. A method according to claim 51 including doping a portion of the substrate in said area with an p-type impurity so that the Os layer and the p-type doped substrate portion form an ohmic junction.

55. A method according to claim 51 in which the step of forming a protective cap over the osmium layer includes depositing a layer comprising platinum (Pt) over the osmium layer.

56. A method of forming an electrical contact to a surface of SiC semiconductor substrate comprising:

depositing a layer comprising metallic osmium (Os) on an area of the substrate surface to form a contact to the substrate; and

annealing the substrate after depositing the Os layer to bond the Os layer to the SiC substrate at said surface.

57. A method according to claim 56 including depositing a thin silicon layer on the substrate surface in said area prior to depositing the Os layer.

58. A method according to claim 56 including doping a portion of the substrate in said area with an n-type impurity so that the Os layer and the n-type doped substrate portion form a rectifying junction.

59. A method according to claim 56 including doping a portion of the substrate in said area with an p-type impurity so that the Os layer and the p-type doped substrate portion form an ohmic junction.

60. A method of forming an electrical contact to a surface of SiC semiconductor substrate comprising:

depositing a titanium carbide (TiC) layer on an area

of the substrate surface to form a contact having an electronic interface to the substrate;

depositing a tungsten carbide (WC) layer on the titanium carbide (TiC) layer; and

depositing a metallic tungsten (W) layer on the tungsten carbide (WC) layer.

61. A method according to claim 60 including doping a portion of the substrate in said area with an n-type impurity so that the TiC/WC/W layer and the n-type doped substrate portion form an ohmic junction.

62. A method according to claim 60 including doping a portion of the substrate in said area with an p-type impurity so that the TiC/WC/W layer and the p-type doped substrate portion form a rectifying junction.

63. A method according to claim 60 including annealing the substrate during or after deposition of the W layer to bond the W layer to the WC layer.

64. A method according to claim 60 including annealing the substrate during or after deposition of TiC layer to densify the TiC layer before deposition of the WC layer.

FIG. 1

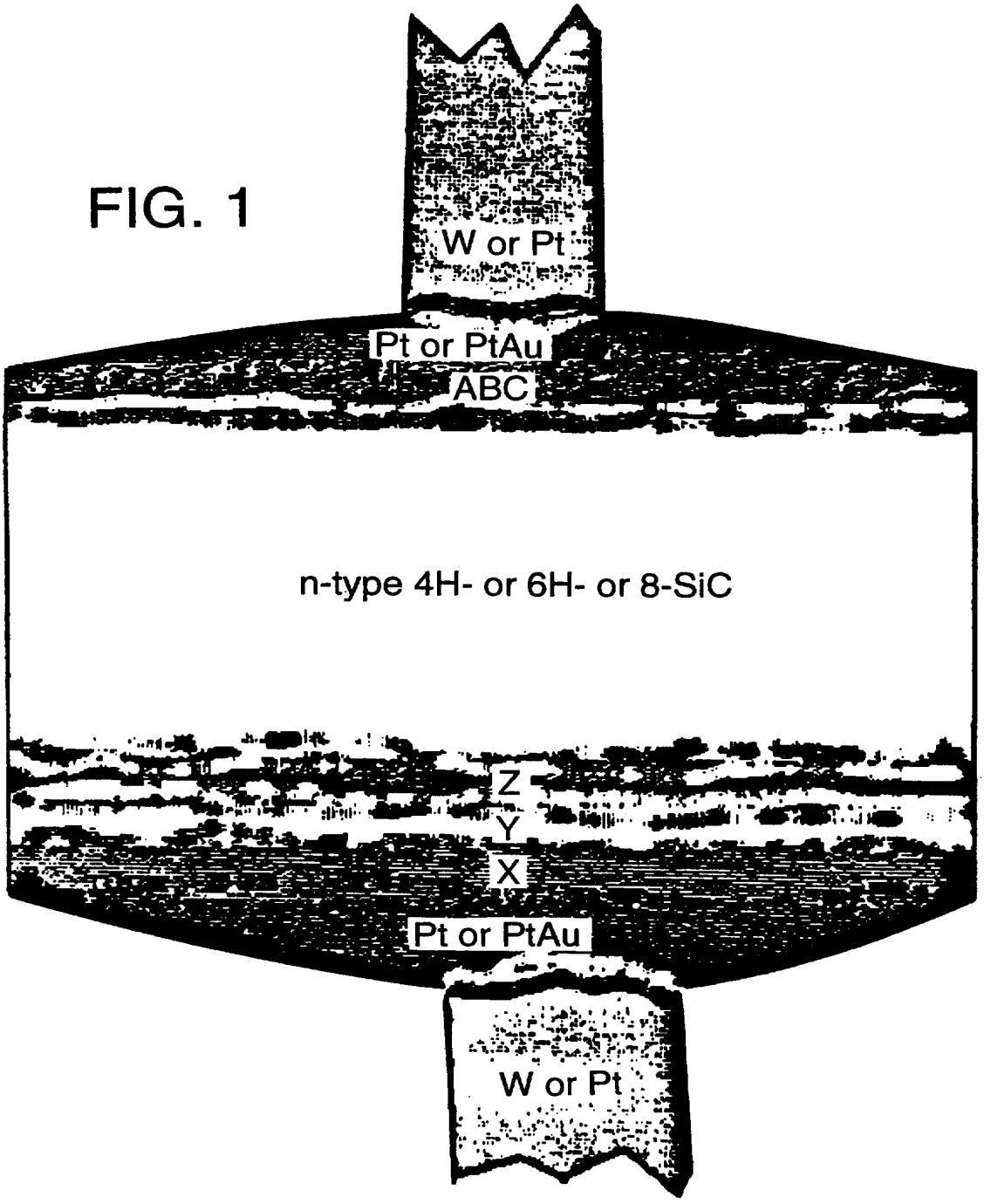


FIG. 2

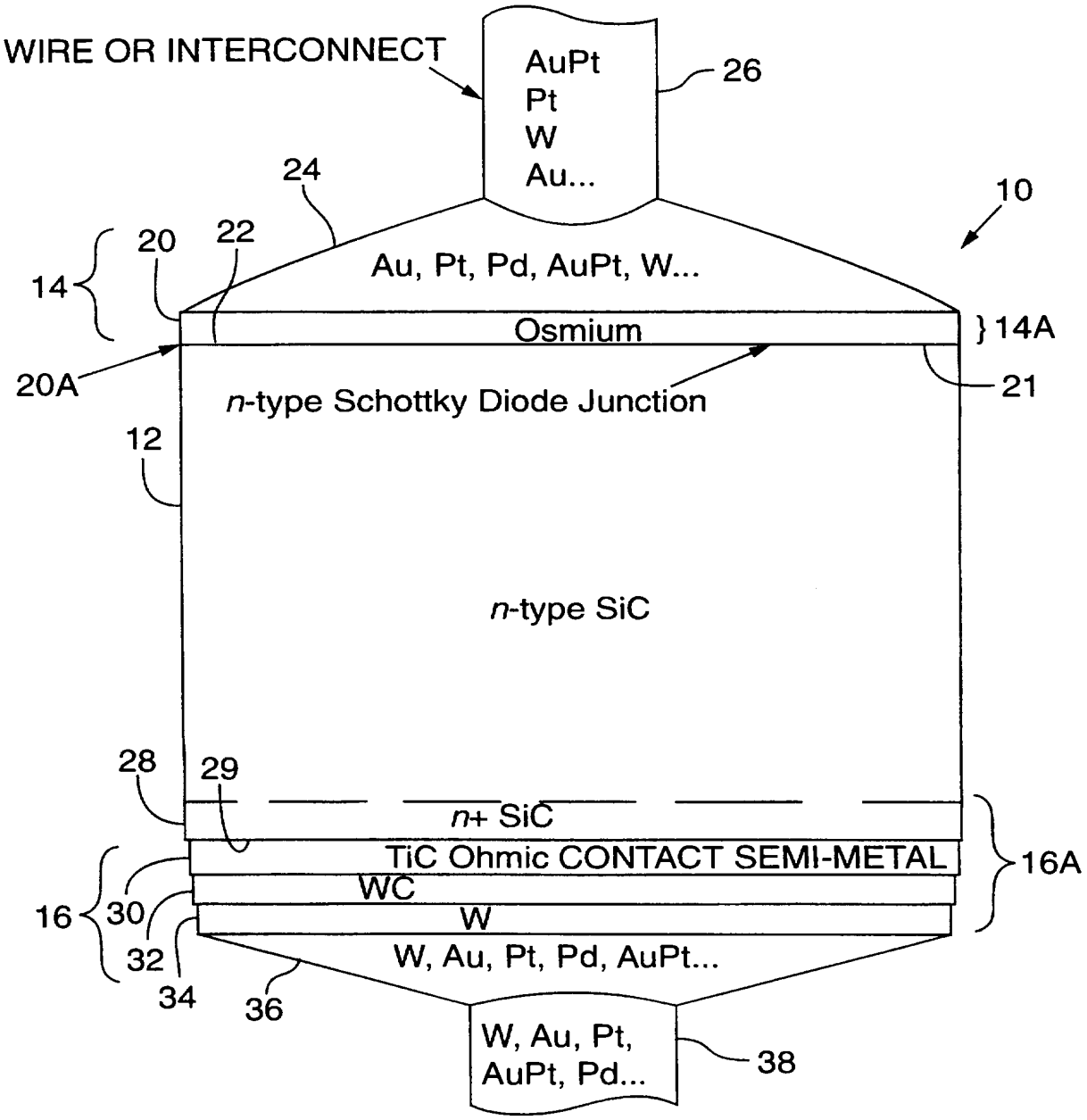

WIRE OR INTERCONNECT
AuPt
Pt
W
Au...
26
24
10
20
22
14
Au, Pt, Pd, AuPt, W...
Osmium
} 14A
20A
21
n-type Schottky Diode Junction
12
n-type SiC
28
29
n+ SiC
TiC Ohmic CONTACT SEMI-METAL
16A
WC
16
30
W
32
W, Au, Pt, Pd, AuPt...
34
36
W, Au, Pt,
AuPt, Pd...
38

FIG. 3

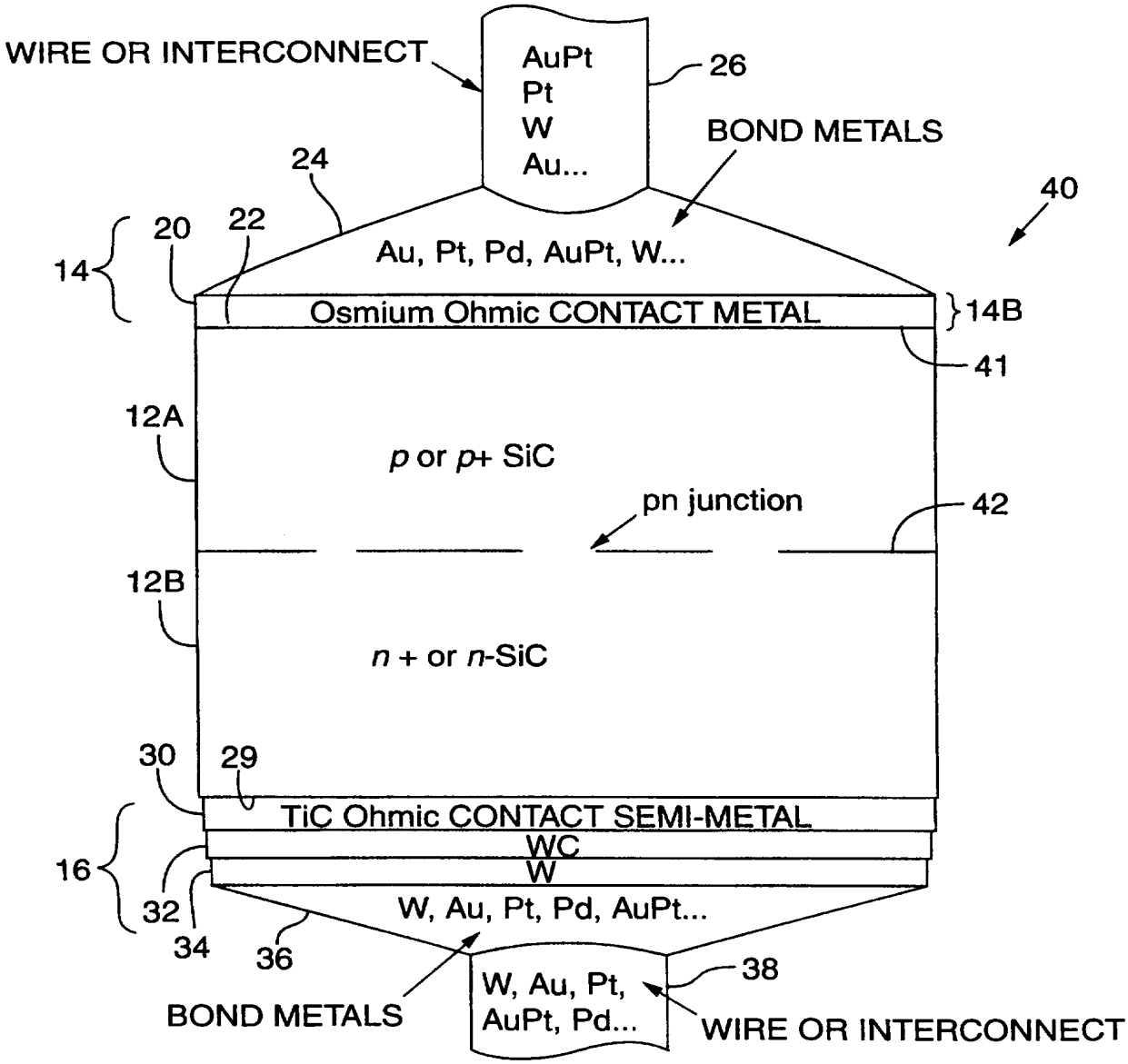

WIRE OR INTERCONNECT
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W
Au...
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24
40
20
22
14
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14B
41
12A
p or p+ SiC
pn junction
42
12B
n + or n-SiC
30
29
TiC Ohmic CONTACT SEMI-METAL
WC
W
16
32
34
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W, Au, Pt,
AuPt, Pd...
38
BOND METALS
WIRE OR INTERCONNECT

FIG. 4A

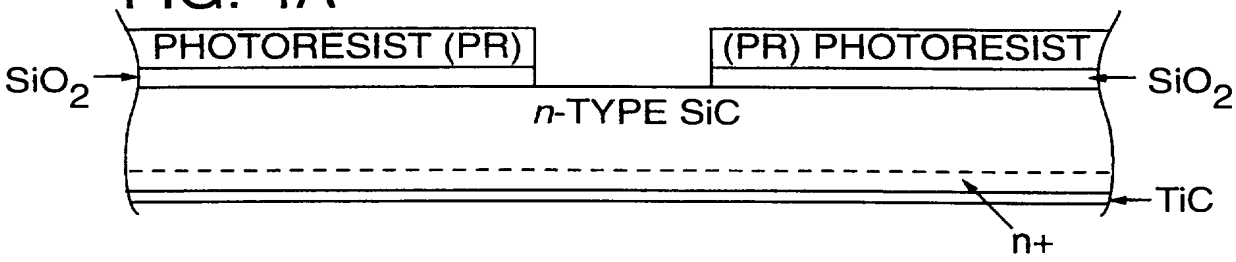


FIG. 4B

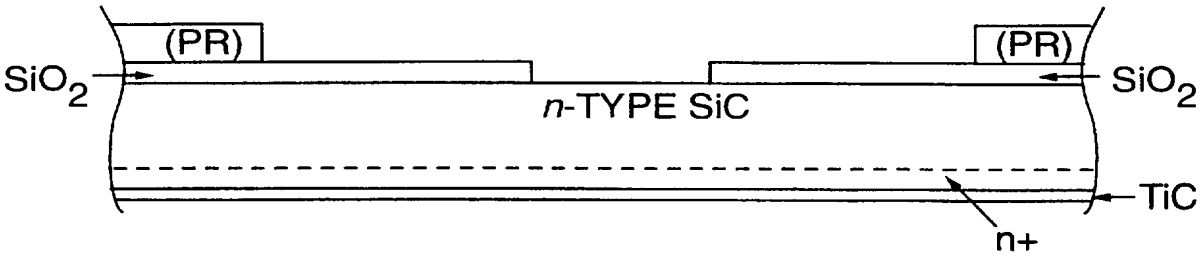


FIG. 4C

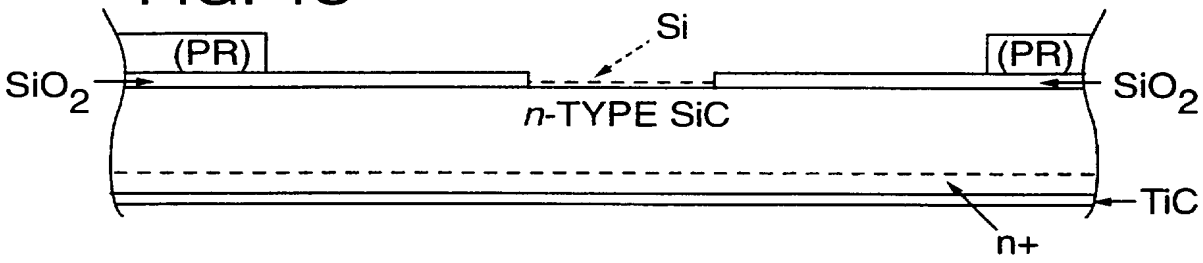


FIG. 4D

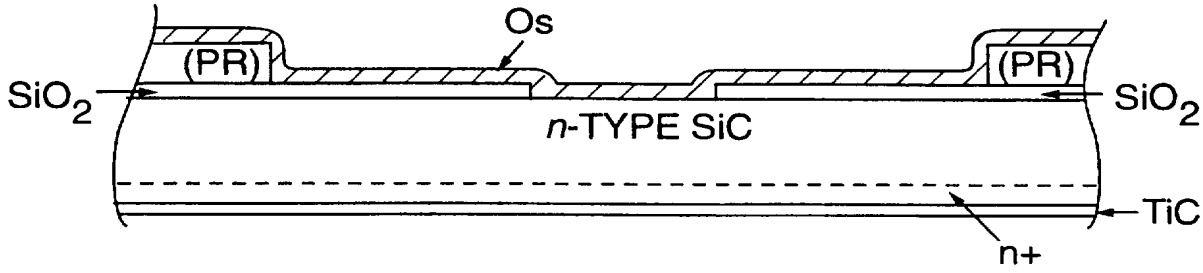


FIG. 4E

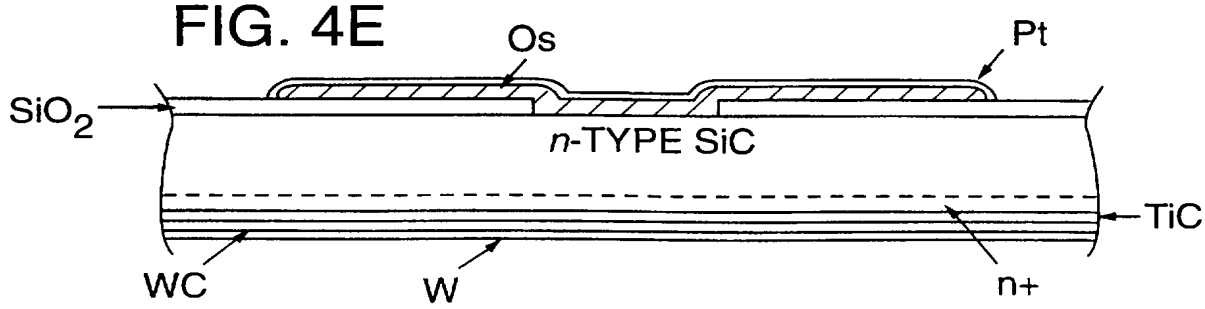


FIG. 5

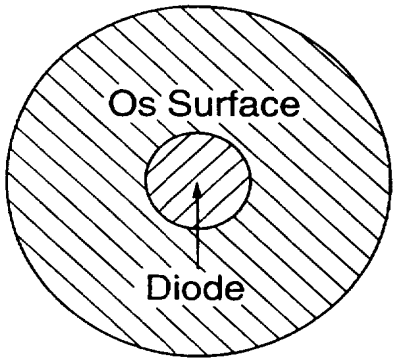


FIG. 6

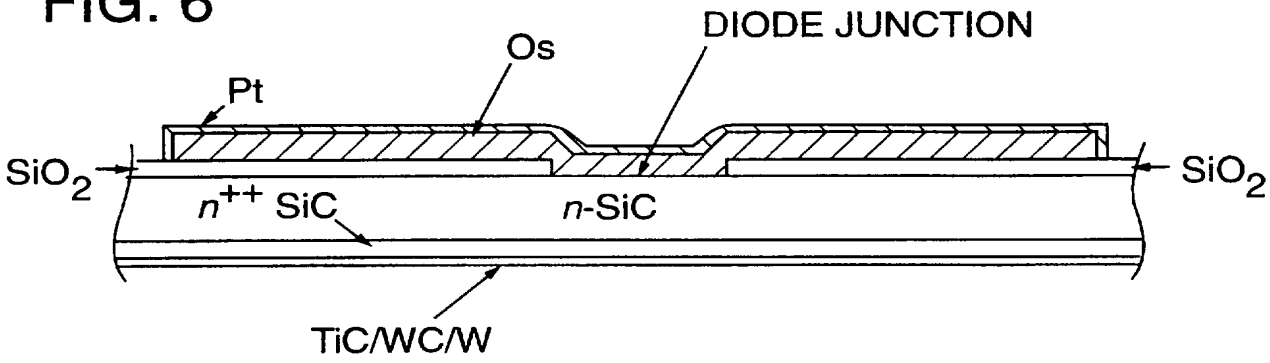
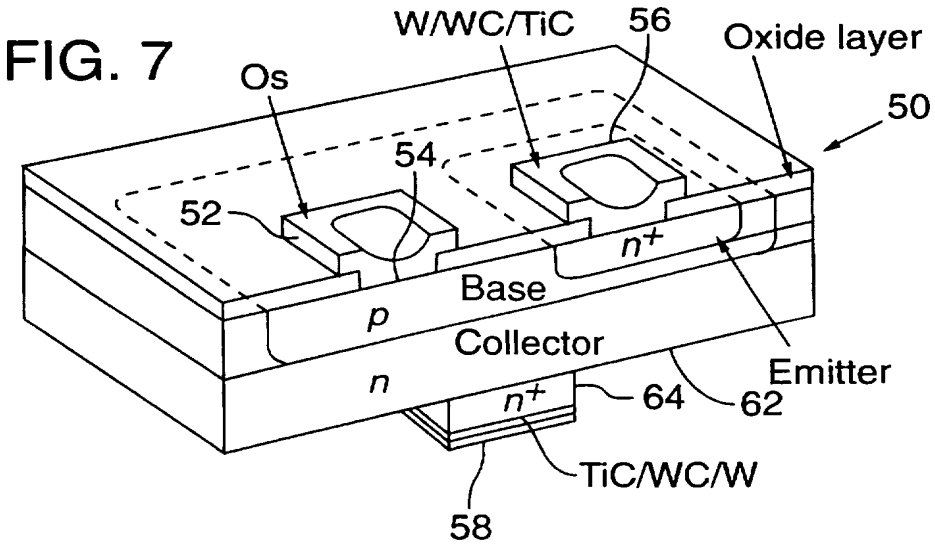


FIG. 7



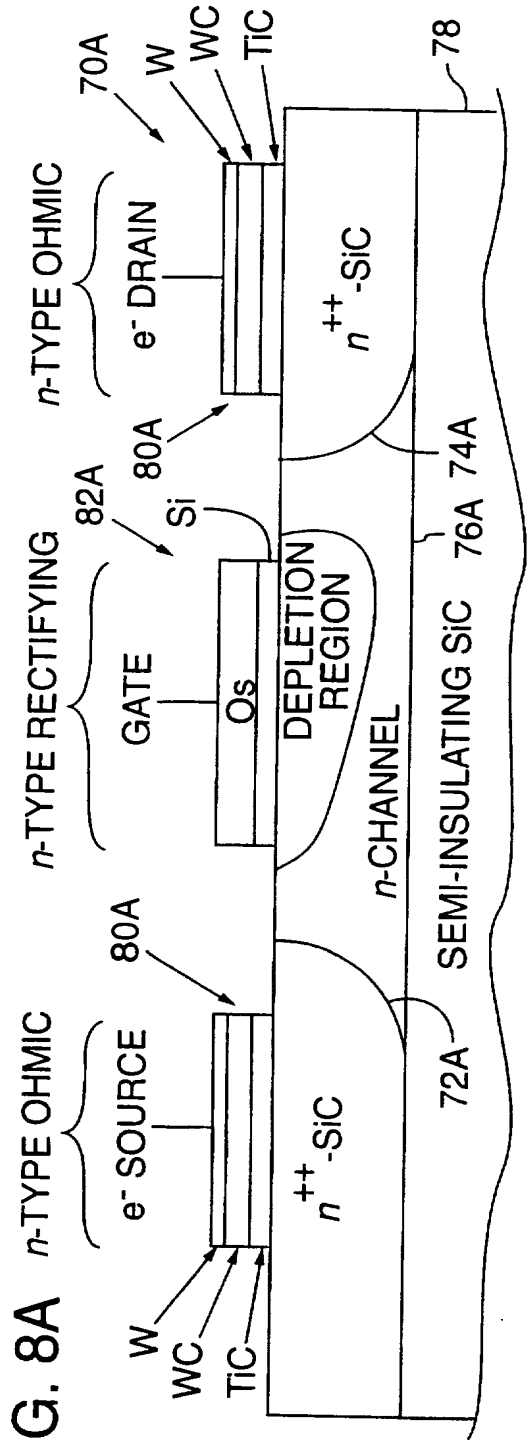

n-TYPE OHMIC
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n-TYPE RECTIFYING
GATE
n-TYPE OHMIC
e- DRAIN
W
WC
TiC
80A
82A
Os
Si
80A
70A
W
WC
TiC
n++-SiC
DEPLETION REGION
n-CHANNEL
SEMI-INSULATING SiC
n++-SiC
72A
76A
74A
78

FIG. 8A

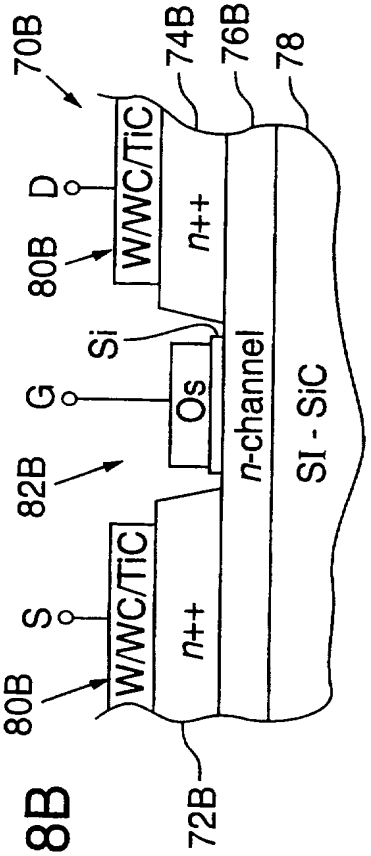

80B
S
82B
G
Si
80B
D
70B
W/WC/TiC
n++
Os
W/WC/TiC
n++
n-channel
SI - SiC
72B
74B
76B
78

FIG. 8B

FIG. 9A

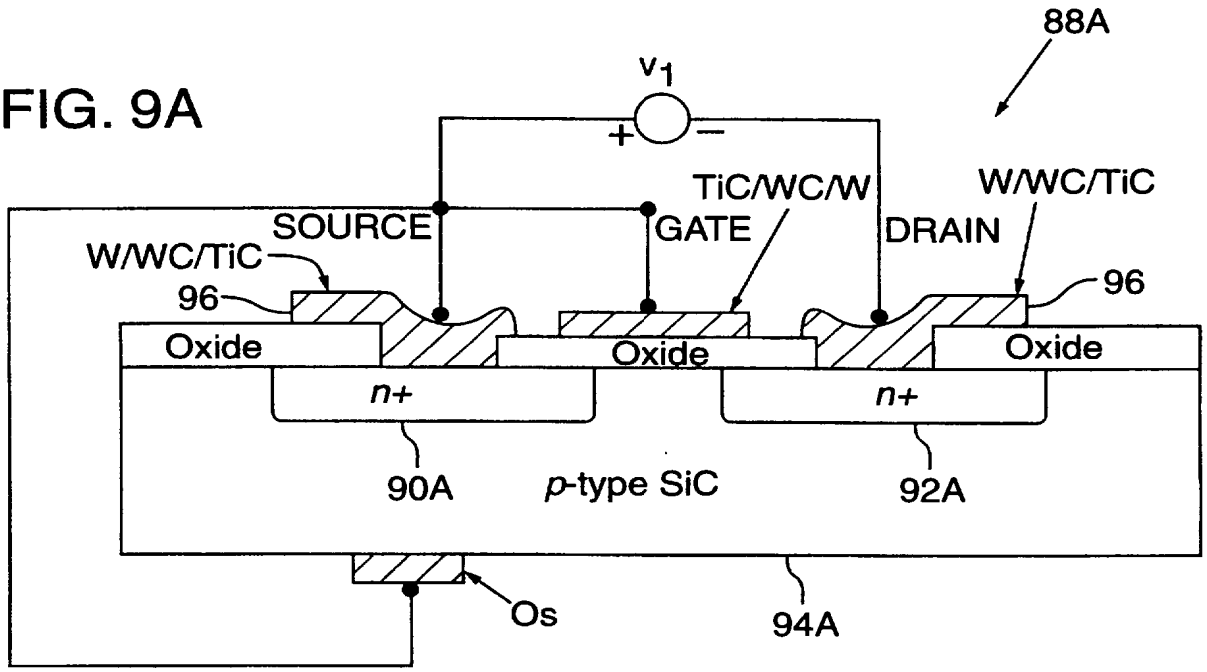

88A
v_1
+
−
TiC/WC/W
W/WC/TiC
SOURCE
GATE
DRAIN
W/WC/TiC
96
96
Oxide
Oxide
Oxide
n+
n+
90A
p-type SiC
92A
Os
94A

FIG. 9B

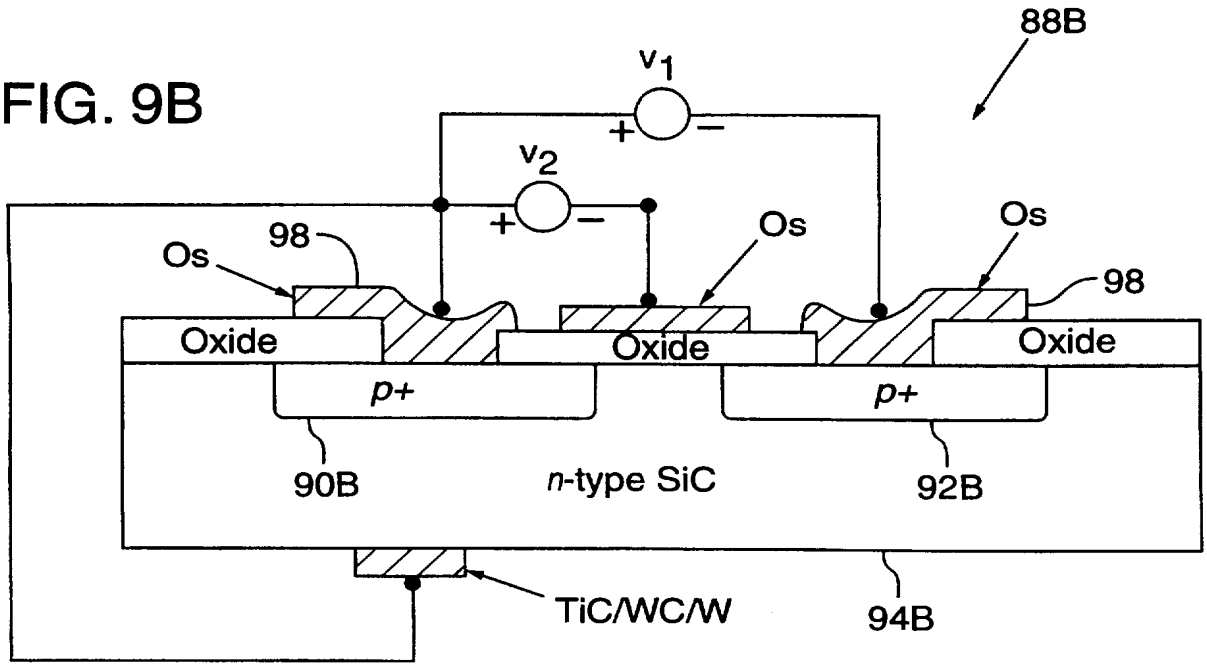

88B
v_1
+
−
v_2
+
−
Os
Os
98
Os
98
Oxide
Oxide
Oxide
p+
p+
90B
n-type SiC
92B
TiC/WC/W
94B

FIG. 10A

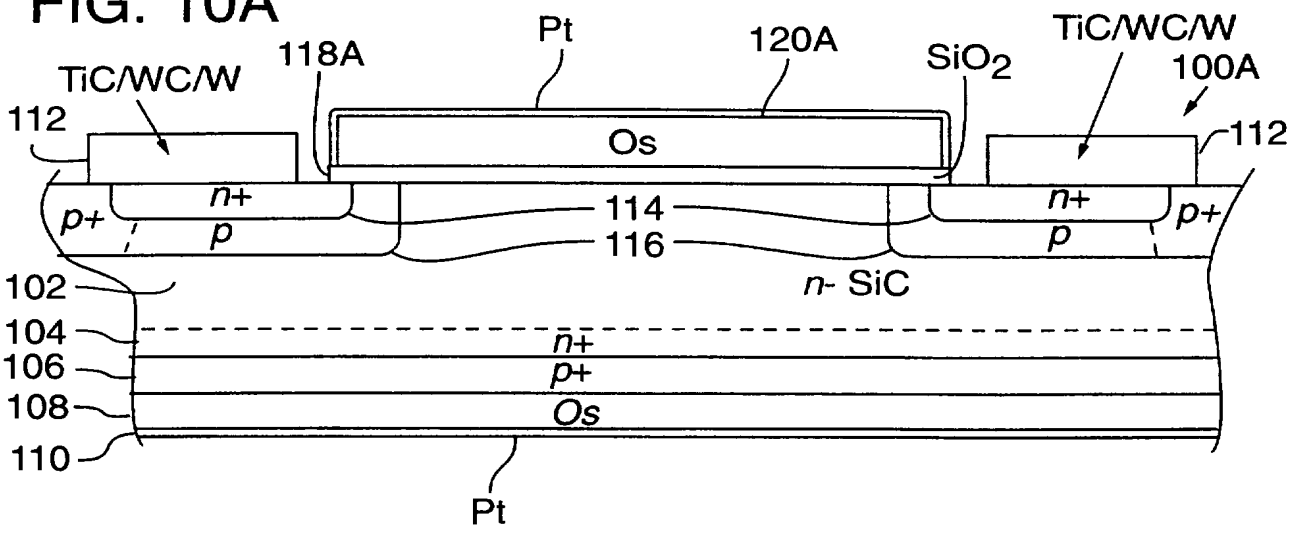
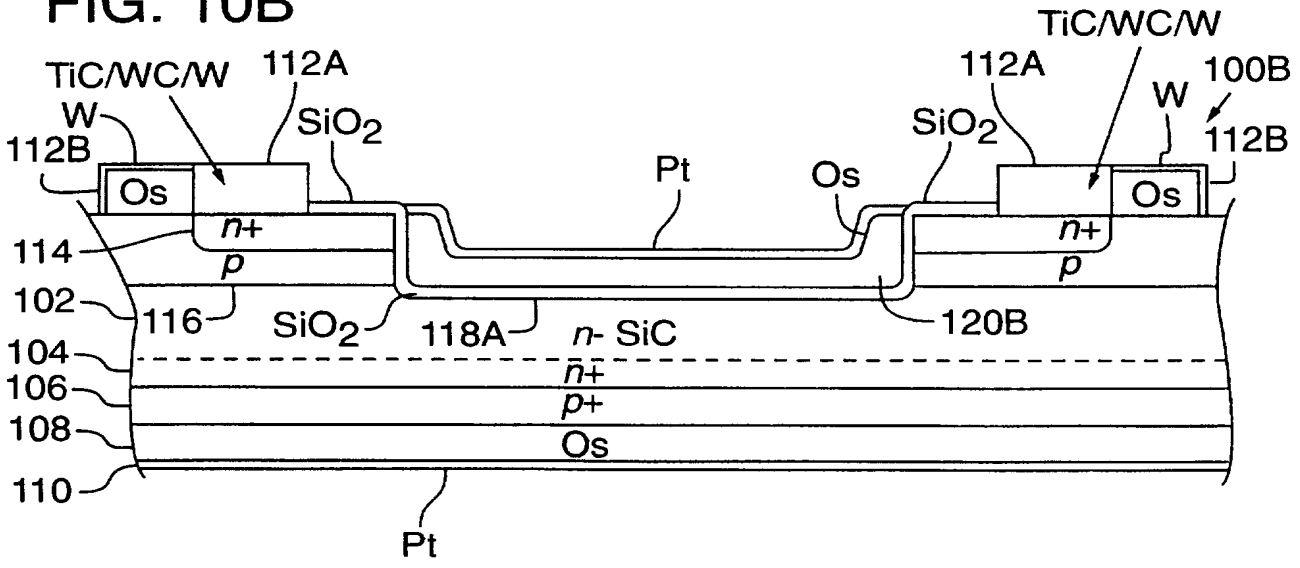


FIG. 10B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/03497

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/283, 21/338, 29/161, 29/45, 29/47, 29/73, 29/812
US CL :257/77, 472, 473; 437/31, 39, 40, 176, 179, 192

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/77, 472, 473; 437/176, 179, 192

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, STN (INSPEC, WPIDS)
search terms: silicon carbide, osmium, titanium carbide, tungsten carbide

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,270,252 A (PAPANICOLAOU) 14 December 1993 See column 2 line 40 to column 3 line 16.	1, 8, 12, 23-37, 50-60
A	US 5,278,431 A (DAS) 11 January 1994, col. 5, lines 40-65	8, 12, 21, 23, 25-37, 60-64
A	US 5,216,264 A (FUJII) 01 June 1993, col. 4 line 14 to col. 5 line 15.	15, 19, 33, 43
A	US 5,455,432 A (HARTSELL) 03 October 1995, col. 3 lines 37-65.	8, 12, 21, 26, 29, 31, 34, 37 47, 49, 60

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
08 MAY 1997	27 JUN 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer TUAN QUACH Telephone No. (703) 308-0661

Form PCT/ISA/210 (second sheet)(July 1992)*

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/847,878	06/17/2020 05:31:49 PM ET	3771-0003-DC13

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8164	FILED BY	Sarah Zizzo
PATENT CENTER #	60039917	FILING DATE	04/14/2020
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

TOTAL DOCUMENTS: 100

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
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DEBOIS.pdf	8	Non Patent Literature	974 KB
GETTO.pdf	5	Non Patent Literature	660 KB
GROVE.pdf	19	Non Patent Literature	1427 KB
GUO_Solid-State.pdf	5	Non Patent Literature	429 KB
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ABOELFOTOH_Materials_Res.pdf	13	Non Patent Literature	673 KB
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Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭61－133646

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審査請求　有　発明の数 1　（全4頁）

⑤4発明の名称　半導体装置の製造方法

⑳特　願　昭59－255500

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明　細　書

1. 発明の名称

半導体装置の製造方法

2. 特許請求の範囲

(1) 半導体層を有する基板上に形成された絶縁膜上に、障壁金属層を介して該半導体層に電気的に接続される電極配線層を形成する方法であって、

前記絶縁膜に対し、前記半導体層へのコンタクト用窓明けを行なう穿孔工程の後、前記障壁金属層および電極配線層の形成工程に先立ち、形成された前記コンタクト用窓内に気相成長法により高融点金属を選択的に被着する工程とを備えたことを特徴とする半導体装置の製造方法。

(2) 障壁金属層は、半導体層と電極配線層の界面反応を防ぐものであることを特徴とする特許請求の範囲第(1)項に記載した半導体装置の製造方法。

3. 発明の詳細な説明

〔発明の技術分野〕

本発明は、半導体装置の製造方法に係り、特に、半導体基板上に形成された拡散層領域と配線層との間に高い信頼性をもつ微細面積のコンタクト電極を形成する方法に関する。

〔発明の技術的背景とその問題点〕

半導体装置の分野では、１９７０年代以降、特に、高集積化への傾向は強まる一方となり、超大規模集積回路（超ＬＳＩ）へと進歩し、１つの半導体チップ上にコンピュータ等のシステムが構成されるまでになってきている。

ところで集積回路の高速化と高集積化は素子の微細化によって実現される。例えばＭＯＳ集積回路では、素子の微細化に伴い、多結晶シリコンゲート電極や、ソース拡散層、ドレイン拡散層等と金属配線層との間で電気的接続を行うためのコンタクト部の面積は縮小されると共にＰＮ接合の深さについても浅くなるように形成されることが必要となってくる。

しかしながら、コンタクト面積の縮小化あるい

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はＰＮ接合が浅く形成されるのに伴い、配線材料としてアルミニウムーシリコン合金を用いた場合においても、アルミニウム中に含まれる過剰シリコンの析出によるコンタクト抵抗の増加や浅いＰＮ接合の破壊等の問題が顕在化してくる。特に超ＬＳＩの場合、数ミリ角のシリコンチップ１個当たり、百万個以上のコンタクトが存在するため、このような接続特性の劣化は素子の信頼性の低下につながり、集積回路の高速化、高集積化への大きな障害となっている。

例えば、第５図に示す如くＰ型のシリコン（Ｓｉ）基板21内に砒素（Ａｓ）イオンをイオン注入して形成されたＰＮ接合の深さ $X=0.1\ \mu m$ となるような N^+ 型のシリコン拡散層22に対し、絶縁膜23内に穿孔されたコンタクト窓24を介してアルミニウム（Ａℓ）電極25を形成した場合、該 N^+ 型のシリコン拡散層22とアルミニウム電極25の間でシリコンとアルミニウムの相互作用に基づく界面反応によって前記ＰＮ接合部がショートすることがある。

（３）

なる。このように、バリヤーメタルを形成したにもかかわらずバリヤー効果がなくなり、アルミニウム層25と N^+ 型のシリコン拡散層22とが反応して第７図に示す如く、N^+ 型シリコンがアルミニウム層中へ溶け出し、シリコン原子の放出路にアルミニウムがくさび状に浸入することがあった。これは、拡散層の突き抜け27と呼ばれ、接合破壊の原因となっていた。

また、スパッタリング法によってバリヤーメタルを形成する場合、拡散層表面に、シリコンの自然酸化膜が生成され、接触抵抗が高くなるという問題があった。この問題を解決するため、バリヤーメタルの形成に先立ち、アルゴンイオン等を用いたスパッタエッチングによるシリコン自然酸化膜のクリーニング工程を付加するというような技術も提案されてはいるが、スパッタリングによるダメージあるいは装置内におけるデバイスの汚染等の問題を依然として残している。

このように、スパッタリング法によってバリヤーメタルを形成する方法では、接触抵抗が充分に

（５）

このような問題を解決する技術として、前記 N^+ 型のシリコン拡散層22とアルミニウム電極25との間に前述の如き界面反応が発生するのを防止するため、障壁金属（バリヤーメタル）を形成する方法が注目されている。

この方法は、例えば第６図に示す如く、Ｐ型のシリコン基板21内に形成された N^+ 型のシリコン拡散層22に対応する位置にコンタクト窓24を有するような絶縁層23を形成した後、コンタクト電極25としてのアルミニウム層の形成に先立ち、スパッタリング法により、全面にバリヤーメタルとして窒化チタン膜26を形成しようというものであるが、この方法は、また以下に述べるような欠点を有している。

すなわち、通常のスパッタリング法により、バリヤーメタルを形成した場合、コンタクト窓24の周囲におけるバリヤーメタルの膜厚は、平坦部では 500～1000 Åであるのに対し、その $\frac{1}{10}\sim\frac{1}{2}$ と薄くなる上、この部分でバリヤーメタルの膜応力による歪が集中して膜にクラックが発生し易く

（４）

低く、素子としての信頼性の高いコンタクト電極を実現するには、多くの問題があり、実用化は困難な状態であった。

〔発明の目的〕

本発明は、前記実情に鑑みてなされたもので、微細でかつ浅い半導体層（拡散層）をもつ基板に対しても、接合特性を劣化させることなく、配線層と半導体層（拡散層）との間に、低抵抗でかつ信頼性の高いオーミックコンタクトを形成することを目的とする。

〔発明の概要〕

そこで、本発明の方法では、拡散層等の半導体層を有する基板の表面に形成された絶縁膜上にコンタクト窓を形成した後、まず、気相成長法により該コンタクト窓内に露呈する基板の表面に選択的に高融点金属を形成し、この後、バリヤーメタル、配線層を順次形成するようにしている。

〔発明の効果〕

すなわち、拡散層（半導体層）に対するコンタクト窓を穿孔した後、スパッタリング法によりバ

（６）

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リヤーメタルを形成するに先立ち、金属化合物ガスを用いた高融点金属の気相成長工程を導入することにより、基板表面を覆う絶縁膜に形成されたコンタクト窓内にのみ選択的に高融点金属膜が析出せしめられ、コンタクト窓の存在による段差が緩和されるため、バリヤーメタルの膜厚が薄くなる部分がほとんどなくなり、ほぼ均一な膜厚のバリヤーメタルが形成され、拡散層（半導体層）の突き抜けによる接合破壊はほとんど皆無となる。

また、気相成長法によって高融点金属膜が形成される際に、半導体層（拡散層）と反応し、高融点金属が成長せしめられるという過程をとるため、基板表面上の自然酸化膜は完全に除去され、極めて低抵抗のオーミックコンタクトが実現可能となる。

このように、本発明の方法によれば、微細でかつ浅い拡散層をもつ基板に対し、低抵抗でかつ極めて信頼性の高い、拡散層へのオーミックコンタクトの形成が可能となる。

〔発明の実施例〕

（7）

ン（WF_6）とアルゴン（Ar）との混合ガスを用いた気相成長法により、高融点金属被膜としてタングステン（W）膜5を前記コンタクト窓3内に露呈するN^+型のシリコン拡散層2上にのみ選択的に形成する。形成条件としては、基板温度は250～450℃、反応炉内の圧力は1×10^{-2}～760Torr、六弗化タングステンガスの分圧は1×10^{-4}～5×10^{-2}の範囲にとるのが望ましい。また、膜厚は200～1000Åとするのが望ましい。

この後、スパッタリング法により、バリヤーメタルとして窒化チタン膜（TiN）6を通常の形成条件で、膜厚500～1000Åとなるように形成する。（第4図）

そして最後に、コンタクト用電極および電極配線層としてのアルミニウム膜7を形成し、第1図に示したような半導体装置が完成する。

このようにして形成されたコンタクト用電極は、N^+型シリコン拡散層上に自然酸化膜が残留していない状態で被着せしめられたタングステン膜上に、バリヤーメタルとしての窒化チタン膜を介し

（9）

以下、本発明の実施例を、図面を参照しつつ詳細に説明する。第1図に示すのは、本発明の一実施例の方法によって形成された半導体装置の構造を示すもので、P型のシリコン基板1内のN^+型のシリコン拡散層2に対応する部分にコンタクト窓3を有する絶縁膜4が形成されており、このコンタクト窓3内に高融点金属層としてタングステン膜5が形成され、この上膜にバリヤーメタルとしての窒化チタン膜6、そして電極配線層としてのアルミニウム膜7が順次形成されている。

次に、かかる構造の半導体装置の形成方法を説明する。まず、第2図に示す如く、P型のシリコン基板1上に砒素（As）をイオン注入することによって形成されたPN接合深さ$X=0.1\,\mu m$のN^+型のシリコン拡散層2の表面全体に絶縁膜として酸化シリコン膜4を堆積し、これにフォトリソエッチング法等により、コンタクト窓3を穿孔する。（このときのエッチングは、反応性イオンエッチングを用いて行なう。）

次いで、第3図に示す如く、六弗化タングステ

（8）

て形成されているため、コンタクト抵抗が低く抑えられる。すなわち、タングステン膜の成長は、N^+型のシリコン拡散層表面におけるシリコンとの反応によって進むため、前記自然酸化膜は完全に除去された状態でタングステン膜が被着せしめられており、コンタクト電極部が$1.0\,\mu m$口以下の微細なものについても、コンタクト抵抗を数十Ω程度におさえることができる。

また、バリヤーメタルとしての窒化チタン膜をスパッタリング法によって形成するに際しても、その下層のタングステン膜が均一な膜厚でコンタクト窓内に充填されているため、コンタクト窓による段差が緩和され、ほぼ均一な膜厚の窒化チタン膜が形成し得ることになり、充分なバリヤー効果を有するため、コンタクト電極としてのアルミニウム膜と拡散層との間に相互作用が生じることもなく、デバイスとしての信頼性は極めて高いものとなる。

なお、実施例においては、コンタクト窓内に形成する高融点被膜として、六弗化タングステンを

（10）

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反応ガスとして用いた気相成長法によって形成されるタングステン膜を用いたが、反応ガスとして、塩化タングステンWCl_6等の他のタングステン化合物を用いて形成されるタングステン膜を用いたり、更には、モリブデン（Mo）、ニオブ（Nb）、タンタル（Ta）、チタン（Ti）の弗化物、塩化物等による気相成長膜等から選択したものを使用してもよい。

また、実施例においては、バリヤーメタルとして窒化チタン膜を用いたが、その他窒化タンタル、窒化ハフニウムを用いてもよいことはいうまでもない。

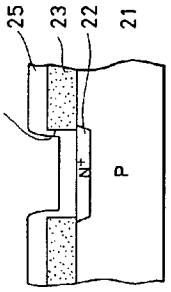
4. 図面の簡単な説明

第1図は、本発明実施例の方法によって形成された半導体装置のコンタクト部を示す図、第2図乃至第4図は、同装置の製造工程を示す図、第5図乃至第7図は、従来例を示す図である。

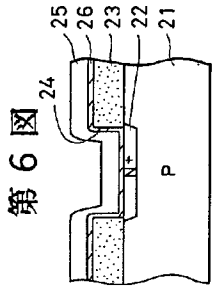
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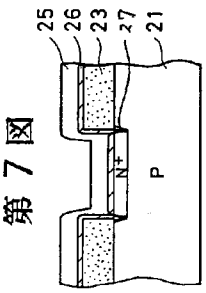
第5図



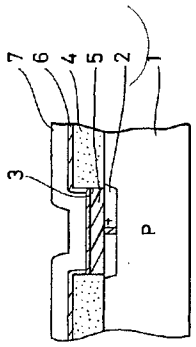
第6図



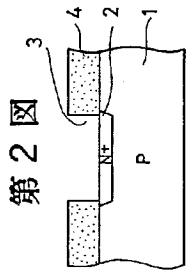
第7図



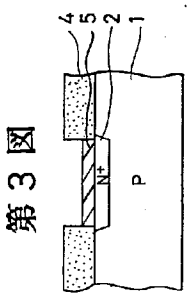
第1図



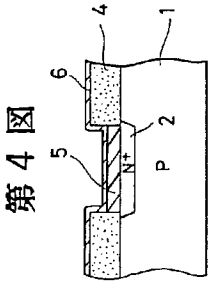
第2図



第3図



第4図



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JPS61133646A MANUFACTURE OF SEMICONDUCTOR DEVICE

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Classifications:
IPC ***H01L21/28; H01L21/768;*** (IPC1-7): H01L21/28;

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Published as: JPS61133646A

MANUFACTURE OF SEMICONDUCTOR DEVICE

Abstract

PURPOSE:To obtain highly reliable ohmic contact, by forming a high-melting- point metal on the surface of a substrate, which is exposed in a contact window, and forming a barrier metal and a wiring layer.
CONSTITUTION:As ions are implanted in a P type silicon substrate, and an N<+> type silicon diffused layer 2 is formed. Then, a silicon oxide film 4 is deposited on the surface. Thereafter, a contact window 3 is formed. Then, a tungsten film 5 as a high-melting-point metal film is formed on the layer 2. Thereafter a titanium nitride film 6 as a barrier metal is formed. Then, an aluminum film 7 as a contact electrode and a wiring layer is formed.

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DESCRIPTION JPS61133646

[0001]

TECHNICAL FIELD OF THE INVENTION The present invention relates to a method for manufacturing a semiconductor device, and more particularly, to forming a highly reliable contact electrode having a fine area between a diffusion layer region formed on a semiconductor substrate and a wiring layer. Regarding the method. [Technical Background of the Invention and Problems Thereof] In the field of semiconductor devices, the tendency toward high integration has been increasing especially since the 1970's, and the progress toward ultra-large-scale integrated circuits (ultra-LSI) has made it one semiconductor. A system such as a computer is being constructed on a chip. By the way, high speed and high integration of an integrated circuit are realized by miniaturization of elements. For example, in an MO8 integrated circuit, the area of a contact portion for making electrical connection between a polycrystalline silicon gate electrode, a source diffusion layer, a drain diffusion layer, and the like and a metal wiring layer is reduced with the miniaturization of elements. In addition, the PN junction needs to be formed so as to have a shallow depth. However, when the contact surface line is reduced or the PN junction is formed shallow, even when an aluminum-silicon alloy is used as the wiring material, the contact resistance increases or the depth is shallow due to the precipitation of excess silicon contained in aluminum. Problems such as destruction of the PN junction become apparent. In particular, in the case of an ultra-LSI, there are more than 1 million contacts per 211 mm square sili- lantich, so such deterioration of the connection characteristics leads to a decrease in the reliability of the element, which results in higher speed and It is a major obstacle to integration. For example, as shown in FIG. 5, a P + type silicon (8i) substrate 21 is formed of an N + type such that the depth X of a PN junction formed by implanting arsenic (As) ions is 0.1 μ. When the aluminum (A1) electrode 5 is formed on the silicon diffusion layer η through the contact window holes perforated in the insulating film n, silicon and aluminum are formed between the N + type silicon diffusion layer n and the aluminum electrode 5. The PN junction may be short-

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circuited due to an interfacial reaction based on the interaction of the above. As a technique for solving such a problem, a method of forming a barrier metal (barrier metal) in order to prevent the above-mentioned interfacial reaction between the N + type silicon diffusion layer n and the aluminum electrode 5 from occurring. Is getting attention. This method is, for example, as shown in FIG. 6, after forming an insulating layer portion having a contact window U at a position corresponding to the N + type silicon diffusion layer B formed in the P type silicon substrate 21, Prior to forming the aluminum layer as the contact electrode 5, a titanium nitride film is formed as a barrier metal on the entire surface by a sputtering method, but this method also has the following drawbacks. .

That is, when the barrier metal is formed by the normal sputtering method, the film thickness of the barrier metal around the contact window row becomes thinner at the flat portion, and the strain due to the film stress of the barrier metal concentrates at this portion. The film is likely to be cracked. In this way, despite the formation of the barrier metal, the barrier effect disappears and the aluminum layer reacts with the N + type silicon diffusion layer to dissolve the N + type silicon into the aluminum layer as shown in FIG. In some cases, aluminum was wedged out into the discharge path of silicon atoms. This was called the punch-out of the diffusion layer and was the cause of junction failure. Further, when the barrier metal is formed by the sputtering method, there is a problem that a natural oxide film of silicon is formed on the surface of the diffusion layer and the contact resistance increases. In order to solve this problem, a technique of adding a cleaning process of the silicon natural oxide film by sputter etching using argon ions or the like before forming the barrier metal has been proposed, but damage or damage caused by sputtering However, there still remain problems such as device contamination within the company. As described above, in the method of forming a barrier metal by the sputtering method, contact resistance is sufficiently low, and there are many problems in realizing a highly reliable contact electrode as an element. there were. [Object of the Invention] The present invention has been made in view of the above-mentioned circumstances, and even for a substrate having a fine and shallow semiconductor layer (diffusion layer), a wiring layer and a semiconductor layer can be formed without deteriorating the bonding characteristics. The purpose is to form a highly reliable ohmic contact with the (diffusion layer). SUMMARY OF THE INVENTION Therefore, in the method of the present invention, after forming a contact window on an insulating film formed on the surface of a substrate having a semiconductor layer such as a diffusion layer, first, the inside of the contact window is formed by vapor phase epitaxy. The refractory metal is selectively formed on the surface of the substrate exposed to the outside, and then the barrier metal and the wiring layer are sequentially formed. [Advantages of the Invention] That is, after the contact window for the diffusion layer (semiconductor layer) is punched, a vapor phase growth step of a refractory metal using a metal compound gas is introduced before forming a barrier metal by a sputtering method. By this, the refractory metal film is selectively deposited only in the contact window formed in the insulating film covering the substrate surface, and the step due to the existence of the contact window is mitigated, so that the barrier metal film thickness is reduced.

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Is almost eliminated, and a barrier metal having a substantially uniform film thickness is formed, and there is almost no junction breakdown due to penetration of the diffusion layer (semiconductor layer).

Also, when the refractory metal film is formed by the vapor phase growth method, the refractory metal reacts with the semiconductor layer (diffusion layer) to grow the refractory metal, so that the natural oxide film on the substrate surface is completely removed. It is possible to realize an ohmic contact with extremely low resistance. As described above, according to the method of the present invention, it is possible to form an ohmic contact with a diffusion layer having low resistance and extremely high reliability on a substrate having a fine and shallow diffusion layer. Embodiments of the Invention Embodiments of the present invention will be described in detail below with reference to the drawings. FIG. 1 shows the structure of a semiconductor device formed by the method of one embodiment of the present invention, in which a portion corresponding to an N + type silicon diffusion layer 2 in a P type silicon substrate 1 is contacted. An insulating film 4 having a window 3 is formed, a tungsten film 5 is formed in the contact window 3 as a refractory metal layer, and a titanium nitride film 6 as a barrier metal and an electrode wiring layer as a barrier metal are formed on the tungsten film 5. The aluminum film 7 is sequentially formed. Next, a method of forming a semiconductor device having such a structure will be described. First, as shown in FIG. 2, a surface metal body of an N + type silicon diffusion layer 20 having a PN junction depth X = 0.1 μm formed by ion-implanting arsenic (AS) on a P type silicon substrate 1. Then, a silicon oxide film 4 is deposited as an insulating film, and a contact window 3 is perforated by a photolithography method or the like. (At this time, etching is performed using reactive ion etching.) Then, as shown in FIG. 3, the tungsten (W) film 5 as a refractory metal film is formed on the contact window by a vapor phase growth method using a mixed gas of tungsten hexafluoride (WF6) and argon (Ar). It is selectively formed only on the N + type silicon diffusion layer 2 exposed in the inside 3. As the formation conditions, the substrate temperature is 250 to 450 ″ O, and the pressure in the reaction furnace is 1 × 10 −2 to 760 ° rr. The partial pressure of the tungsten hexafluoride gas is preferably in the range of IX 10- 'to 5 × 10-2. The film thickness is preferably 200 to 1000; Thereafter, a titanium nitride film (TiN) 6 is formed as a barrier metal by a sputtering method under normal forming conditions so as to have a film thickness of 500 to 1000 A. (FIG. 4) And finally, the aluminum film 7 as a contact electrode and an electrode wiring layer is formed, and the semiconductor device as shown in FIG. 1 is completed. The contact electrode thus formed has a tungsten film deposited on the N + type silicon diffusion layer in a state where no natural oxide film remains, and a titanium nitride film as a barrier metal is interposed therebetween.), The contact resistance can be kept low.

That is, since the growth of the tungsten film proceeds by the reaction with silicon on the surface of the N + type silicon diffusion layer, the tungsten film is deposited with the natural oxide film completely removed, and the contact electrode portion is The contact resistance can be

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suppressed to about several tens of Ω even for a fine one having a diameter of 1.0 μm or less. Further, even when the titanium nitride film as the barrier metal is formed by the sputtering method, the tungsten film as the lower layer is filled in the contact window with a uniform thickness, so that the step due to the contact window is relaxed, and the unevenness is almost uniform. Since a titanium nitride film having a large thickness can be formed and has a sufficient barrier effect, no interaction occurs between the aluminum film as the contact electrode and the diffusion layer, and the reliability as a device is high. It will be extremely expensive. In the examples, a tungsten film formed by a vapor phase growth method using tungsten hexafluoride as a reaction gas was used as the high melting point film formed in the contact window. A tungsten film formed by using another tungsten compound such as No. 6 is used. You may use what was selected from the phase growth film etc. Further, in the embodiment, the titanium nitride film is used as the barrier metal, but it is needless to say that tantalum carbide and hafnium nitride may be used.

[0002]
Brief description of the drawings

[0003]

FIG. 1 is a diagram showing a contact portion of a semiconductor device formed by the method of an embodiment of the present invention, FIGS. 2 to 4 are diagrams showing a manufacturing process of the device, and FIGS. FIG. 7 is a diagram showing a conventional example.

1 ... Silicon substrate, 2 ... Silicon diffusion layer, 3 ... Contact window, 4 ... Silicon oxide film, 5 ... Tungsten film, 6 ... Titanium nitride film, 7 ... Aluminum A film, 21 ... Silicon substrate, n ... Silicon diffusion layer, n ... Insulating film, U ... Contact window, 5 ... Aluminum electrode, 26 ... Titanium nitride film.

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CLAIMS JPS61133646

1.
A method of forming an electrode wiring layer electrically connected to the semiconductor layer via a barrier metal layer on an insulating film formed on a substrate having a layer, the method comprising: After the perforation step of opening a contact window to the above, prior to the step of forming the barrier metal layer and the electrode wiring layer, a refractory metal is selectively deposited in the formed contact window by vapor phase epitaxy. A method of manufacturing a semiconductor device, comprising: (2) The method for manufacturing a semiconductor device according to claim (1), wherein the barrier metal layer prevents an interface reaction between the semiconductor layer and the electrode wiring layer.

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⑲日本国特許庁（JP）　⑪特許出願公開

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審査請求　未請求　発明の数 1　（全5頁）

⑭発明の名称　ショットキーバリアダイオード

⑳特　願　昭61－304462
㉒出　願　昭61(1986)12月20日

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明細書

1.発明の名称

ショットキーバリアダイオード

2.特許請求の範囲

(1)半導体基板（2）上のエピタキシャル層（3）と金属層（5）との間の界面層（21a）を、窒化チタン（22）及び／又は酸化チタン（23）を所定量含有した組成としてなることを特徴とするショットキーバリアダイオード。

(2)上記界面層（21a）は、アルゴンガスに所望量の窒素及び／又は酸素を混合してなる混合ガスを使用してチタンをスパッタリングすることにより形成されてなることを特徴とする特許請求の範囲第1項記載のショットキーバリアダイオード。

3.発明の詳細な説明

（概要）

本発明はショットキーバリアダイオードおいて、アルミニウムとシリコンとの界面に窒化チタン及び／又は酸化チタンを一部介在させ、製造工程の種々の要因により影響されずに、所望の順方向電流－電圧特性を再現性良く得ることが出来るようにしたものである。

（産業上の利用分野）

本発明はショットキーバリアダイオードに係り、特に金属層とエピタキシャル層との界面に関する。

（従来の技術）

ショットキーバリアダイオードにおいて、順方向電流（I_F）－電圧（V_F）特性は重要であり、ばらつきの少ないことが要求される。

このダイオードをTTL回路に組み込んで使用する場合には動作速度が速いことが必要である。

動作速度はV_Fが低い程速いため、上記のダイオードでは、バリアハイトΦ_bが小さいTiをバリアメタルとして使用している。

第7図はこの種の従来のショットキーバリアダイオード1の一部を概略的に示す。同図中、2はシリコン基板、3はエピタキシャル成長層、4は絶縁層、5は導電メタルとしてのAℓ層、6はバ

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リアメタルである。バリアメタル６のうち符号６ａで示す部分がエピタキシャル成長層３とＡℓ層５との間の界面層を形成する。

界面層６ａ（バリアメタル６）は、×で示す$Ti_xAℓ_y$７と□で示すTi_xSi_y８とよりなる組成である。この界面層６ａのバイリアハイトは$Φ_{b1}$であり、ダイオード１は第８図中線Ⅰで示すI_F-V_F特性を有する。

〔発明が解決しようとする問題点〕

ところで、このダイオード１は、第９図に示すように、絶縁層４に窓をあけ、厚さが約 100Åの Ti 膜９をスパッタリングで形成し、この上にＡℓ層５を形成し、この後、図示はしないが、絶縁層とＡℓ層とを交互に形成することにより製造される。

絶縁層及びＡℓ層の形成過程で全体が加熱される。例えば絶縁層をＰＳＧで形成したときには、420～ 450℃の熱が３０分～１時間かゝる。

このＴｉ膜９形成後における製造工程における熱により、Ｔｉ膜７のＴｉは、Ａℓ及びＳｉと反応して前記の$Ti_xAℓ_y$７，Ti_xSi_y８となる。

各製造設備の間でのＴｉ膜７が受ける熱量のバラツキは避けられない。またＴｉ膜７自体の質についても、スパッタリング装置間である程度ばらついてしまう。

熱がかゝり過ぎたときには、第１０図に示すように$Ti_xAℓ_y$７の一部及びTi_xSi_y８の一部がＡℓ層５及びエピタキシャル成長層３内に拡散し、界面層６ａは薄くなる。これによりバリアハイトが増して$Φ_{b2}$となり、V_Fが高くなって、I_F-V_F特性は例えば線Ⅱで示すようになってしまい、所定のI_{F1}においてV_Fは所望の値より比較的大なる値$ΔV_F$違ってしまう。$ΔV_F$が大きいと、ダイオードは動作速度が遅くなりＴＴＬ回路に組み込むのに不適となり、不良品となってしまう。

上記のように従来のダイオードは、そのI_F-V_F特性が、製造過程で影響を受け易いという問題点があった。

〔問題点を解決するための手段〕

本発明は、半導体基板上のエピタキシャル層と金属層との間の界面層を、窒化チタン及び／又は酸化チタンを所望量含有した組成としてなるものである。

〔作用〕

上記の組成は、製造工程がばらついても、バリアハイトが影響されにくゝ、製造設備の違いによりI_F-V_F特性の違いを制限する。

〔実施例〕

第１図は本発明になるショットキーバリアダイオード２０を示す。同図中、第７図に示す構成部分と対応する部分には同一符号を付しその説明を省略する。

２１はバリアメタルであり、エピタキシャル成長層３とＡℓ層５との間に介在している。このうち符号２１ａで示す部分が、エピタキシャル成長層３とＡℓ層５との間の界面層を形成する。界面層２１ａ（バリアメタル２１）は、×で示す$Ti_xAℓ_y$７，□で示すTi_xSi_y８との他に○で示すTi_xN_y（窒化チタン）２２及び△で示すTi_xO_y（酸化チタン）２３を含んだ組成である。Ti_xN_y２２及びTi_xO_y２３の合計の含有量の全体に対する割合は２０％以下であり、以下に述べるように制御されている。

第２図はＴｉ膜２４をスパッタリングで形成した後の状態を示す。スパッタリングは、第３図に示すように、ＡｒにN_2及びO_2を所定の微少量混入させた混合ガスのボンベ２５を使用して行なう。例えばＡｒにN_2が200ppM及びO_2が20ppM混入された混合ガスのボンベを使用する。第３図中、２６は真空チャンバである。

この混合ガスを使用してスパッタリングを行なうことによりN_2，O_2がＴｉと反応し、

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Ti_xN_y，Ti_xO_yが生成し、Ti中にTi_xN_y22及びTi_xO_y23を含有する組成のTi膜24が形成される。

Ti膜形成後に、Al層5が形成され更に絶縁層とAl層とを交互に形成される。このときに全体が加熱され、Ti膜24中のTiはAl及びSiと反応して、Ti_xAl_y7，Ti_xSi_y8となる。Ti_xN_y22及びTi_xO_y23は安定でありAl，Siとは極めて反応しにくいため、そのまゝの形で、残る。

これにより、第1図に示すように、バリアメタル21は、Ti_xAl_y7，Ti_xSi_y8，Ti_xN_y22，Ti_xO_y23の組成となり、これらが協働してバリアハイトΦ_{B3}を形成し、ダイオード20は第4図中線IIIで示すI_F-V_F特性を有する。

上記のAl層，絶縁層の形成工程で予定より余分に加熱されたときには、従来の場合と同じく第5図に示すように、Ti_xAl_y7の一部及びTi_xSi_y8の一部がAl層5及びエピタキシャル成長層3内に拡散する。しかし、Ti_xN_y22及びTi_xO_y23は反応しにくいため、Al，Siとは反応せず、界面に残留し続ける。

このため、界面層21aのバリアハイトは前記の場合より多少上昇するも殆んど変わらず、I_F-V_F特性も例えば第4図中線IVで示す如くになり、所定のI_{F1}におけるV_Fの変化量ΔV_Fは僅かの値に留まり、ダイオードのI_F-V_F特性は許容誤差範囲に収まる。

従って、上記のダイオード20は、製造工程での種々のばらつきによりI_F-V_F特性が影響されにくいものとなる。

こゝで、バリアメタル21中のTi_xN_y22及びTi_xO_y23の量は、前記の混合ガス中のN_2，O_2の量により定まる。一方、混合ガス中のN_2，O_2の量を正確に定めることは容易である。従って、N_2，O_2の量を違えた混合ガスを使用することにより、バリアメタル21中のTi_xN_y22及びTi_xO_y23の量を制御することが可能となり、バリアメタル21中に所定量のTi_xN_y22及びTi_xO_y23量を形成させることが出来、終極的に所望のバリアハイトを有する界面層21aを形成することが出来る。

第6図はダイオードのI_F-V_F特性をスパッタリング工程で使用した混合ガスの成分と対応させて示す。同図中、線Vは$Ar+150ppM N_2+20ppM O_2$の混合ガスを使用した場合、線VIは$Ar+100ppM N_2+20ppM O_2$の混合ガスを使用した場合、線VIIは$Ar+50ppM N_2+20ppM O_2$の混合ガスを使用した場合、線VIIIは$Ar+150ppM N_2+40ppM O_2$の混合ガスを使用した場合のI_F-V_F特性を示す。同図よりN_2，O_2の混入量を増やす程V_Fが小さくなっていること及び所望の混合ガスを使用することにより希望するI_F-V_F特性を有するダイオードを製造できることが分かる。

なお、第6図は、100AのTi膜及び1μのAl層を形成し、アニール450℃，30分を3回繰り返した場合であって、界面層の面積が$256\mu^2$のときの特性である。

なお、バリアメタル21中に、Ti_xN_y22及びTi_xO_y23のうちいずれか一方のみが混入した構成であってもよく、上記と同様な効果を有する。

〔発明の効果〕

本発明によれば、界面層が所定量の窒化チタン及び／又は酸化チタンを含有した組成であるため、製造過程の違いによるバリアハイトへの影響が少なく、然して製造装置が相違しても、速い動作速度を有する所望の順方向電流－電圧特性を有するものを再現性良く得ることが出来、歩留りの向上を図ることが出来る。

4.図面の簡単な説明

第1図は本発明になるショットキーバリアダイオードの一実施例の要部の拡大断面図、

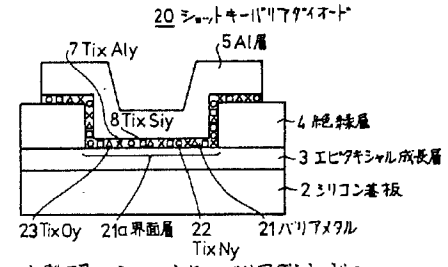
第2図はTi膜形成後の状態を示す図、

第3図はTi膜形成用のスパッタリング装置の

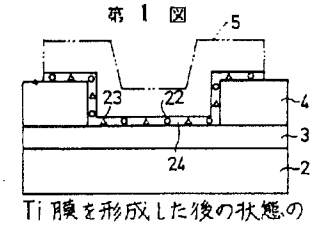
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概略図、
第４図は第１図のダイオードのI_F-V_F特性のばらつきを説明する図、
第５図は熱がかゝり過ぎた場合の界面層の状態を説明する図、
第６図は混合ガスの成分の違いに対応するダイオードのI_F-V_F特性の違いを説明する図、
第７図は従来のショットキーバリアダイオードの１例の要部の拡大断面図、
第８図は第７図のダイオードのI_F-V_F特性のばらつきを説明する図、
第９図はＴｉ膜形成後の状態を示す図、
第１０図は熱がかゝり過ぎた場合の界面層の状態を説明する図である。
図において、
２はシリコン基板、
３はエピタキシャル成長層、
４は絶縁層
５はＡｌ層、
７はTi_xAl_y、
８はTi_xSi_y、
２０はショットキーバリアダイオード、
２１はバリアメタル、
２１ａは界面層、
２２はTi_xN_y、
２３はTi_xO_y、
２４はＴｉ膜、
２５は混合ガスボンベである。

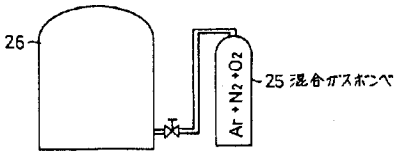
代理人　弁理士　井　桁　貞



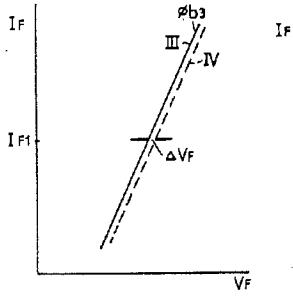
本発明のショットキーバリアダイオードの要部の断面図
第１図



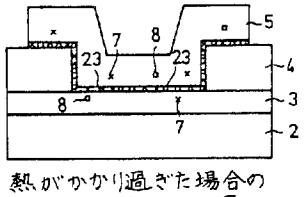
Ti膜を形成した後の状態の断面図
第２図



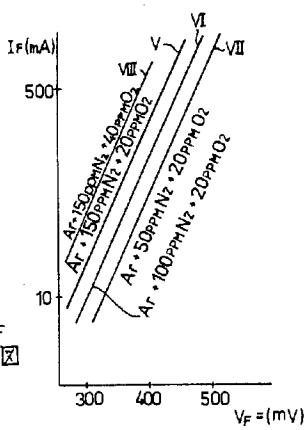
Ti膜形成用スパッタリング装置の概略図
第３図



第１図のダイオードのI_F-V_F特性のばらつきを説明する図
第４図

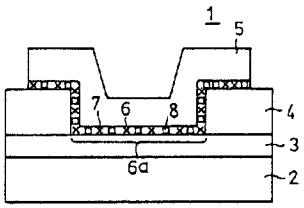


熱がかかり過ぎた場合の界面層の状態を示す図
第５図



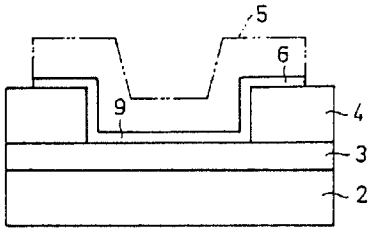
混合ガスの違いに対応するダイオードのI_F-V_F特性を示す図
第６図

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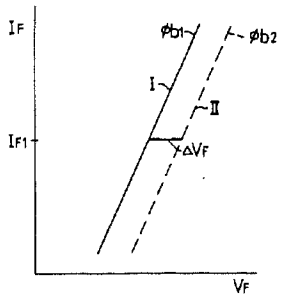
従来のショットキーバリア
ダイオードの要部の断面図

第 7 図



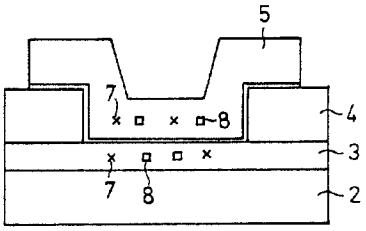
Ti膜形成後の状態を示す図

第 9 図



第7図のダイオードのIF-VF
特性のばらつきを説明する図

第 8 図



熱がかかり過ぎた場合の
界面層の状態を示す図

第 10 図

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JPS63157466A SCHOTTKY BARRIER DIODE

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SCHOTTKY BARRIER DIODE

Abstract

PURPOSE:To assure specified forward current-voltage characteristics with high reproducibility not to be affected by various factors of manufacturing processes by a method wherein TiN and/or TiO is partly laid on the interface between Al and Si. CONSTITUTION:An interface layer 21a by a barrier metal 21 is formed between an epitaxial layer 3 and an Al layer 5. The barrier metal 21 contains a TixAly 7, a Tix Siy 8, a TixNy 22 and a TixOy 23 while the total content TixNy 22 and TixOy 23 shall not exceed 20% out of the whole content. In order to form the barrier metal 21, firstly Ti films are formed by sputtering process using Al gas containing specified amount of N2 and O2 gas to form Ti films containing TixNy 22 and TixOy 23 and then TixNy 7 and TixSiy 8 are produced by repeatedly heating the Al layer 5. Through these procedures, the TixNy 22 and TixOy 23 are stabilized to be so hardly reactive to Al, Si that the barrier height is hardly changeable to assure IF-VF characteristics of diode with high reproducibility.

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DESCRIPTION JPS63157466

[0001]

(Outline) In the Schottky barrier diode of the present invention, titanium nitride and / or titanium oxide is partially interposed at the interface between aluminum and silicon, and a desired forward current is obtained without being affected by various factors in the manufacturing process. -The voltage characteristics can be obtained with good reproducibility. [Field of Industrial Application] The present invention relates to a Schottky barrier diode, and more particularly to an interface between a gold layer and an epitaxial layer. [Prior Art] In a Schottky barrier diode, the forward current (IF) -voltage (VF) characteristic is important, and it is required that the variation be small. When this diode is used by incorporating it in a TTL circuit, it is necessary to have a high operation speed. Since the operating speed is longer as vF is lower, in the above diode, Ti having a small barrier hide Φb is used as the barrier metal. FIG. 7 schematically shows a part of a conventional Schottky barrier diode 1 of this type. In the figure, 2 is a silicon substrate, 3 is an epitaxial growth layer, 4 is an insulating layer, 5 is an A2 layer as a conductive metal, and 6 is a barrier metal. A portion of the barrier metal 6 indicated by reference numeral 6a forms an interface layer between the epitaxial growth WJ3 and Ae115. The interface H6a (barrier metal 6) is composed of Ti A2 7 indicated by X and T indicated by the mouth; x s i y 8 and y. The vialiahide of this interface m6a is Φ, 1 and the diode 1 has the IF-V characteristic shown by degeneracy in FIG. [Problems to be Solved by the Invention] In the diode 1, as shown in FIG. 9, a window is formed in the insulating layer 4 and a Ti film 9 having a thickness of about 100 is formed by sputtering. It is manufactured by forming an A2 layer 5 on the upper surface and then forming insulating layers and A2 layers alternately, though not shown. Insulation layer and AJ! The whole is heated in the process of forming l. For example, when the insulating layer is formed of PSG, heat of 420 to 450 ° C. is 30 minutes to 1 hour). このＴｉ！！ The Ti in the T1 film 7 reacts with A2 and 3i due to the heat in the manufacturing process after the formation of J9, and the Ti XAly7. Ｔｉｘ Ｓ＋ｙ ８となる。 A variation in the heat m received by the T1 film 7

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between the manufacturing facilities is inevitable. The quality of the Ti film itself also varies to some extent between sputtering devices. When the heat is too much, a part of TiXA2,7 and a part of Tr xs t ys diffuse into the AIL layer 5 and the epitaxial growth layer 3 as shown in FIG. 10, and the interface 116a becomes thin.

As a result, the barrier hide is increased to Φb2, vF is increased, and rF-V, the characteristic is shown by, for example, a line {circle around (2)}, and vF is relatively larger than a desired value ΔVF at a predetermined IFl. Will end up. If ΔvF is large, the operating speed of the diode becomes slow, making it unsuitable for incorporation in a TTL circuit, resulting in a defective product. As described above, the conventional diode has a problem that its IF- ■ F characteristic is easily affected in the manufacturing process. [Means for Solving the Problems] In the present invention, the interface layer between the epitaxial layer and the metal layer on the semiconductor substrate has a composition containing titanium nitride and / or titanium oxide in a desired solid content. [Operation] The above composition limits the difference in IF-V and characteristics due to the difference in manufacturing equipment even if the manufacturing process varies. (Embodiment) FIG. 1 shows a Schottky barrier diode 20 according to the present invention. In the figure, those parts corresponding to the parts shown in FIG. 7 are designated by the same reference numerals, and a description thereof will be omitted. Reference numeral 21 is a barrier metal, which is interposed between the epitaxial growth layer 3 and the / 1 layer 5. Of these, the portion indicated by reference numeral 21a is the epitaxial growth layer 3 and / M! The interface layer between 1ii5 is formed. The interface 1121a (barrier metal 21) is Ti xAIly7. The composition includes TixNy (titanium nitride) 22 indicated by O and TixOy (titanium oxide) 23 indicated by Δ in addition to T i x S i y 8 indicated by mouth. The ratio of the total y content of Ti N 22 and T + xo, 23 to the total content is 20% or less, which is controlled as described below. FIG. 2 shows a state after the Ti film 24 is formed by sputtering. As shown in FIG. 3, the sputtering is performed using a gas cylinder 25 of a mixed gas in which A "is mixed with a predetermined minute amount of N2 and o2. For example, a cylinder of a mixed gas in which N2 is 2001) l) H and 02 is mixed with 20pp) l in Ar is used. In FIG. 3, 26 is a vacuum chamber. By performing sputtering using this mixed gas, N2.02 reacts with Ti to produce Ti N TiX0y, and a Ti film with a composition y containing X y'Ti N 22 and T i X0y23 in Ji. 24 is formed. (2) After forming the i film, the A2 layer 5 is formed, and the insulating layer and the A2 layer are alternately formed. At this time, the whole is heated, Ti in the T1 film 24 reacts with A2 and Si, and Ti Ae 7.

Ｔ ｌ Ｘ５ ｉ ｙ ｙ ８となる。 Since Ti N 22 and TixOy 23 are y stable and extremely difficult to react with Ae and st, they remain in that form. As a result, as shown in FIG. 1, the barrier metal 21 has T i A'l 7 and T i x S i y 8. The composition is yT i N 22 and T t x Oy 23, and these y cooperate to form the barrier hide Φb3, and the diode 20 has I, −V and characteristics shown by the solid line in FIG. Above An! f. When excessively heated in the insulating layer forming

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process, the T1xA-deficient y7 part and the TiX5iy8 part are in the A2 layer 5 and the epitaxial growth layer 3 as shown in FIG. Spread to. しかし、Ｔｉ Ｘ Ｎ。 Since 22 and Tr x o y 23 do not easily react, they do not react with Ae and Si and remain at the interface. Therefore, the barrier bite of the interface layer 21a is slightly higher than that in the above case, but is almost the same. -V, the characteristic also becomes as shown by the line IV in FIG. 4, for example, the change in V at a given IFI, ΔV [, remains at a slight value, and the diode 1. The -VF characteristic falls within the allowable error range. Therefore, the above-mentioned diode 20 is less susceptible to I-V and characteristics due to various variations in manufacturing: Here, the defects of T1xNy22 and TixOy23 in the barrier metal 21 are determined by the threshold of N2,02 in the mixed gas. On the other hand, it is easy to accurately determine the values of N and 02 in the mixed gas. Therefore, it is possible to control the mouths of Ti N 22 and T ixo, 23 in the barrier metal 21 by using a mixed gas having different N2, 02, and the predetermined amount in the barrier metal 21. ff1 (7) Ti N 22 and T + xo, 23 ffi can be formed and y, and finally the interface FIJ21a having a desired barrier hide can be formed. FIG. 6 shows the IF-V characteristics of the diode in correspondence with the components of the mixed gas used in the subbattering process. In the figure, line V shows the case where the mixed gas of Ar + 150p1) HN 2 +201) l) 802 is used, and line ■ shows the case where the mixed gas of Ar +1001) pHN 2 +20 DI) H02 is used. ■ indicates the IF-VF characteristics when using a mixed gas of Al + 50p11M N2 + 20p1) HO2, and line ■ indicates using a mixed gas of Δr + 150p1) HN2 + 40 DDHO2.

From the figure, it can be seen that as the mixing amount of N2 02 increases, F decreases and that a diode having a desired I-VF characteristic can be manufactured by using a desired mixed gas. Incidentally, FIG. 6 shows the characteristics when a Ti film of 100 persons and an A2 layer of 1 μm were formed and annealing at 450 ° C. for 230 minutes was repeated three times, and the area of the interface layer was 256 μ2. The barrier metal 21 may have a configuration in which only one of Ti XNy22 and T1xoy23 is mixed, and the same as above! Have a significant effect. [Effect of the Invention] According to the present invention, since the interface layer has a composition containing titanium nitride and / or titanium oxide a predetermined number of times, the influence on the barrier hide due to the difference in the manufacturing process is small, and the manufacturing apparatus is different. Even in this case, it is possible to obtain with high reproducibility a desired forward current-voltage characteristic having a high operation speed, and it is possible to improve the yield.

[0002]
Brief description of the drawings

[0003]

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FIG. 1 is an enlarged sectional view of an essential part of an embodiment of a Schottky barrier diode according to the present invention, FIG. 2 is a view showing a state after forming a 7i film, and FIG. 3 is a sputtering device for forming a Ti film. Fig. 4 is a schematic diagram, Fig. 4 is a diagram for explaining the variation in the IF-vF characteristics of the diode of Fig. 1, Fig. 5 is a diagram for explaining the state of the interface when too much heat is applied, and Fig. 6 is 1. The diode corresponding to the difference in the components of the mixed gas.

FIG. 7 is a diagram for explaining a difference in —VF characteristic, FIG. 7 is an enlarged cross-sectional view of a main part of an example of a conventional Schottky barrier diode, and FIG. 8 is a description of IF-V of the diode in FIG. 7 and characteristic variation. FIG. 9 is a diagram showing the state after the Ti film is formed, and FIG. 10 is a diagram explaining the state of the interface layer when the heat is excessive. In the figure, 2 is a silicon substrate, 3 is an epitaxial growth layer, 4 is an insulating layer 5 is an A2 layer, 7 is TixA, 8 is TjxSjys20 is a Schottky barrier diode, 21 is a barrier metal, and 21a is An interface layer, 22 is TjxNy123, TixOyl24 is a Ti film, and 25 is a mixed gas cylinder. Cross section of the zero portion of the 9th,-, Toki-It "IT lead wire. Fig. 1 Fig. 75 Fig. 3 Fig. 3 Fig. 3 Fig. 5 Fig. 5 Fig. 5 IF-VF 7 Confectionery 8 Fig. 1 T-pod type hair support 1 No, 1 small figure 9 Fig. 9 Fever and s"j 4 +-, interface counterfeiting, 1 Dimensions Figure 1O

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CLAIMS JPS63157466

1.
The interface layer (21a) between the epitaxial layer (3) and the metal layer (5) on the substrate (2) has a composition containing a predetermined amount of titanium nitride (22) and / or titanium oxide (23). Is a Schottky barrier diode. (2) The interface layer (21a) is formed by sputtering titanium using a mixed gas obtained by mixing a desired amount of nitrogen and / or oxygen with argon gas. A Schottky barrier diode according to item 1 above.

GF Exhibit 1126 - 1978/2248

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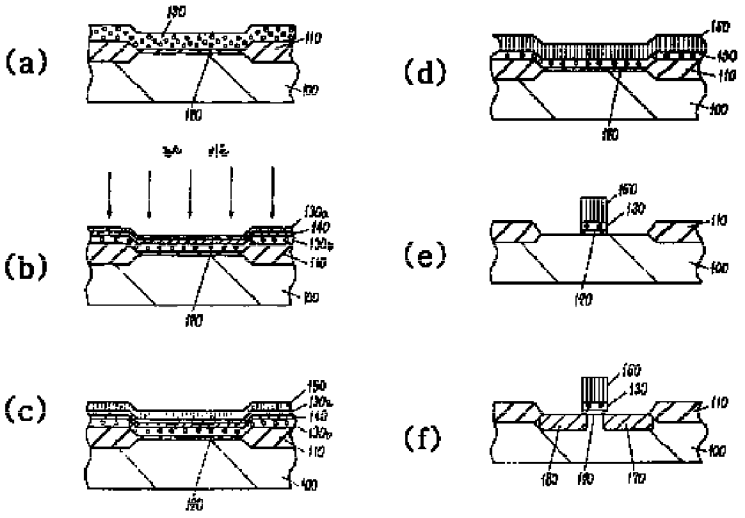
심사관 : 김경국 (책자공보 제2704호)

(54) 반도체장치의 제조방법

요약

내용 없음.

대표도



명세서

[발명의 명칭]

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반도체장치의 제조방법

[도면의 간단한 설명]

제1도는 본 발명의 제1실시예의 공정순서를 도시한 단면도.

제2도는 본 발명의 제2실시예의 공정순서를 도시한 단면도.

제3도는 본 발명의 제3실시예의 공정순서를 도시한 단면도.

제4도는 본 발명의 제4실시예의 공정순서를 도시한 단면도.

* 도면의 주요부분에 대한 부호의 설명

100,200,300,400 : 실리콘기판　　110,210,310,410 : 산화막

120,220,320,420 : 게이트 산화막　　130,230,330,430 : 다결정 실리콘막

140,440 : 원자도입층　　150 : 얇은 티탄막

160,260,360,460 : 합금화층　　170,270,370,470 : 소오스영역

180,280,380,480 : 드레인영역　　240,340 : 제1원자도입층

250,350,450 : 얇은 텅스텐막　　290,390 : 제2원자도입층

[발명의 상세한 설명]

본 발명은 반도체장치의 제조방법에 관한 것으로, 특히 MOS형 집적회로등의 비(非)단결정도전체막과 저(低)저항도전체막으로 구성된 저저항화된 게이트전극의 전기적 특성을 개량하고, 또 게이트절연막의 절약파괴를 방지할 수 있는 제조방법에 관한 것이다.

전계효과형 반도체집적회로에서 미세하고 고성능의 트랜지스터를 얻기 위하여, 비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성하고 열처리하여 게이전극의 저저항화를 일반적으로 실행한다.

예를 들면, 저저항전도체로서, 고융점 금속 또는 실리콘과의 합금, 즉, 실리사이드는 다결정체실리콘상에 퇴적되어 게이트전극으로 사용되고, 약 500℃로 열처리 하면 고융점금속 또는 실리사이드는 쉽게 다결정체실리콘과 반응하여 전부 실리사이드속으로 변형됨으로써 저저항화가 된다.

이렇게 형성된 도전체막의 시이트저항은 대략 1-10Ω/스퀘어로 낮아, 반도체집적회로의 고속작동이 예기된다.

반면, 금속종류에 의존하여, 다결정체실리콘과는 다른 물질과 반응하고, 특히 티탄은 게이트 전극물질로서 사용되는 실리콘산화막과 반응하므로, 비록 이것이 매우 저저항이지만 게이트전극물질로 사용되기는 어렵다.

따라서, 티탄보다는 약간 고저항이지만 실리콘산화막과는 거의 반응하지 않는, 텅스텐과 몰리브덴이 일반적으로 사용된다.

이런 고융점금속 또는 실리사이드와 실리콘질화막 또는 실리콘산화막과의 반응성 및 반응물의 생성에너지는 N.G.Einsprach 편(Academic Press 출판)의 VLSI 전자공학 : 미세구조, 제9권, 제2장에 기재되어 있다.

한편, 반응의 용이성은 활성화에너지의 크기에 의해 판단될 수 있으며, 활성화에너지가 작을수록 반응이 쉬워지는 것은 알려져 있다.

비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성한 후 열처리하면, 비단결정도전체막과 저저항도전체막사이의 계면에서 상호의 구성원자가 이동하여, 계면부근이 합금화되어, 저저항화된다.

그러나, 비단결정도전체의 결정입자사이의 계면, 즉, 입자 경계에서, 비단결정도전체의 구성원자의 결합력이 약하므로, 저저항도전체막의 구성원자와의 원자의 치환이 결정입자내에서 보다 빠르게 진행되어, 저저항도전체는 입자경계를 따라서 국부적으로 확산되는 경향이 있다.

저저항도전체가 국부적으로 확산되어 게이트전극 아래의 절연막을 찢게되면, 게이트전극이 다른 전극과 단락되어, 트랜지스터의 신뢰성 또는 제품의 수율을 저하시킨다.

이것을 방지하기 위해, 비단결정도전체와 저저항도전체 사이에 CVD(화학적 증착)에 의해 초박형의 실리콘질화막을 퇴적시켜 저저항도전체의 국부적인 확산을 억제하고 신뢰성을 증가시키는 방법이 IEEE Transactions of Electron Devices, Vol., ED-33, No.4, April 1986, pp. 464~467에 언급되어 있다.

그러나 이것은 막두께의 고재현성에서, CVD에 의한 초박편실리콘 질화막의 퇴적은 어렵고, 더욱이 비교적 낮은 온도에서의 퇴적과 불순물확산층내의 불순물의 재확산에 기인한 전기적 특성에의 변화를 방지하는 것이 필요하므로, 저저항도전체의 국부적 확산을 충분히 억제하는 조밀막성질을 얻기가 곤란하여, 신뢰성과 수율의 향상 또는 충분하지가 않았다.

상기 문제점을 해결하기 위해 본 발명의 일차적 목적은 저저항도전막의 구성원자와 비단결정도전체

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막의 구성원자사이의 양막의 계면부근에서의 치환을 제한하여, 입자경계를 따른 저저항도전체의 국부적인 확산을 억제하고 게이트전극의 전기저항을 균일하게 감소시켜 신뢰성을 향상시킨 반도체장치의 제조방법을 제공하는데 있다.

본 발명의 다른 목적은 절연막상에 비단결정도전체막을 형성하는 공정과, 상기 비단결정도전체막속에 최소한 한 종류의 원자를 도입하여 원자도입층을 형성하는 공정과, 상기 비단결정도전체막상에 저저항도전체막을 형성하는 공정과, 상기 비단결정도전체막상에 형성된 저저항도전체막을 열처리하는 공정을 포함하여, 비단결정도전체막표면으로부터 침입한 저저항도전체막의 원자가 원자도입층내에서 편재되거나 정지되는 특징을 지닌 반도체장치의 제조방법을 제공하는데 있다.

본 발명의 제조방법에 따라서, 비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성하고 열처리하여 게이트전극을 저저항화하므로써, 비단결정도전체의 구성원자와 저저항도전체막의 구성원자와의 상호원자치환은 두막의 계면의 제한된 영역에서만 균일하게 일어날 수 있다.

더욱이, 게이트전극의 전기저항이 일정하게 저감됨과 동시에, 입자경계를 따른 저저항도전체의 국부적인 확신이 억제될 수 있어, 결국, 신뢰성이 향상된 반도체장치를 제공하는 것이 가능하다.

본 발명의 신규한 특징은 특히, 첨부한 청구범위에 나타내었고, 본 발명의 구성과 내용에 대해서는 기타 다른 목적들과 특징에 따라, 도면과 함께 상세한 설명으로 충분히 이해될 수 있을 것이다.

[제1실시예]

본 발명의 제1실시예는 제1도(a)-제1도(f)를 참조하여, 게이트전극에 다결정실리콘과, 티탄을 조합시킨 전계효과형 금속-산화물-반도체(MOS)와 관련하여 상세히 설명한다.

(I) 실리콘기판(100)의 농동영역 형성 예정부를 제외한 표면에 대략 700nm의 산화막(110)을 피일드 산화막으로서 선택적으로 형성하고, 능동영역 형성 예정부의 표면에 대략 10nm의 게이트산화막(120)을 형성하고, 상기 산화막(110)과 (120)상에 대략 200nm의 다결정 실리콘막(130)을 퇴적시키고, $POCl_3$를 사용해 인을 확산시켜 다결정실리콘막(130)을 저저항화하였다(제1도(a)).

(II) 다음 단계로, 다결정실리콘막(130)에 질소이온을 가속에너지 150KeV로 $1\times10^{15}\sim1\times10^{18}cm^{-2}$ 주입하고, 다결정실리콘막(130)의 중간부분에 원자도입층(140)을 형성하였다(제1도(b)).

(III) 물리증착법에 의해서, 대략 100nm의 얇은 티탄막(150)을 퇴적하였다(제1도(c)).

(IV) 500-1000℃에서 10초간 신속하에 열어니일링하거나 500-1000℃에서 30분동안 용광로어니일링에 의한 열처리에 의해서, 질화티탄 및 티탄 실리사이드가 생성되어, 합금화층(160)이 형성되었다(제1도(d)).

(V) 다음 단계로, 포토마스크공정으로 저항패턴을 생성하고, 게이트전극 형성 예정부 및 그의 주변부부 이외의 다른 부분을 건식 에칭하여, 게이트전극을 형성하였다(제1도(e)).

(VI) 마지막으로, 가속에너지 80KeV로 As 이온을 $4\times10^{15}cm^{-2}$ 주입하여, 소오스영역(170) 및 드레인영역(180)을 형성하였다(제1도(f)).

이상의 일련의 공정에 의해서, 소망하는 전계효과형 트랜지스터가 형성되었다.

질소원자도입층(140)은 다결정실리콘 보다는 티탄과 반응하기 훨씬 쉽고, 원자도입층(140) 및 그의 윗부분에서 대부분의 합금화가 일어났다.

따라서, 합금화층의 두께가 균일하게 되므로, 게이트전극의 전기저항이 균일해지고 또한, 저저항도전체의 국부적인 확산도 거의 발생하지 않게 되어, 게이트산화막의 파괴를 방지할 수 있었다.

한편, 제1실시예의 공정(II)에서, 게이트산화막과 그 주변에 걸쳐서 상기 다결정층내에 원자도입층을 선택적으로 형성하고, 원자가 도입되지 않은 부분을 다음 공정의 저저항배선영역으로 사용하면, 이 부분에서는 저저항도전체막과 합금화층이 다결정실리콘막의 거의 전역에 퍼져서, 다결정실리콘과 저저항도전체막 사이의 접속저항을 낮출 수 있다.

그러므로, 게이트산화막에 대한 인가전계의 도전성은 개량된다.

배선영역아래의 산화막은 두꺼우므로, 저저항도전체가 산화막내에 국부적으로 확산되는 것은 문제가 되지 않는다.

이때에, 게이트산화막의 단부에서부터 저저항배선영역까지의 거리는 다음과 같이 규정되는 것이 바람직하다.

즉, 저저항도전체막의 구성원자가 저저항배선영역으로부터 원자도입영역의 하부를 통하여 확산되어 게이트 산화막의 단부까지 침입하고 있으므로, 이런 확산길이보다도 긴 길이로 설정하는 것이 바람직하다.

본 발명의 제1실시예에 있어서는, 저저항도전체로서 티탄을 사용하고, 원자도입층의 구성원자로서 질소를 사용하였으나, 저저항도전체로서 다른 고융점금속 또는 이것의 실리사이드를 사용해도 되며, 원자도입층의 구성원자로서 산소 또는 실리콘 또는 불활성 원자를 사용해도 게이트절연막의 파괴를 방지할 수 있다.

그러나, 저저항도전체막의 구성원자와 전자도입층의 구성원자의 조합에 의해, 게이트절연막의 파괴를 방지하는 메타니즘은 다양하다.

본 발명의 제1실시예인 티탄과 조합의 경우, 즉, 원자도입층의 구성원자가 비단결정도전체의 구성원자보다 저저항전체의 구성원자와 더욱 쉽게 반응할때, 원자도입층의 구성원자와 저저항도전체의 구

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성원자는 서로 반응하여 균일한 합금화층을 형성하고, 저저항도전체의 국부적인 확산이 억제됨으로써 게이트절연막의 파괴를 방지한다.

또, 비단결정도전체막과 저저항도전체막사이의 접속저항이 느려, 인가된 전계에 대한 게이트산화막의 내구력은 우수하다.

또한, 텅스텐과 산소를 조합하는 경우, 즉, 원자도입층의 구성원자가 저저항도전체막의 구성원자보다 비단결정도전체막의 구성원자와 더욱 쉽게 반응하면, 저저항도전체막의 구성원자의 확산은 원자도입층내에서 저지되고, 저저항도전체의 극부적인 확산은 억제되어 게이트절연막의 전기적 파괴를 방지한다.

그러므로 저저항화시 저저항도전체막의 막두께가 증가되면, 게이트절연막의 파괴는 효과적으로 방지될 수 있다.

또한, 원자도입층을 형성하기 위하여 도입되는 원자는, 1종류 또는 복수종류이어도 된다.

[제2실시예]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터에 관한 것으로 제2도(a)-제2도(g)를 참조하여 상세히 설명한다.

(I) 실리콘기판(200)의 능동영역 형성예정부를 제외한 표면상에, 대략 700nm의 산화막(210)을 피일드 산화막으로서 선택적으로 형성하고, 대략 10nm의 게이트산화막(220)을 능동영역 형성예정부의 표면상에 형성하고, 상기 산화막(210)과 (220)상에 대략 200nm의 다결정실리콘막(230)을 퇴적한 후, $POCl_3$를 사용해 인을 확산시켜서 다결정실리콘막(230)을 저저항화하였다(제2도(a)).

(II) 다음에, 다결정실리콘막(230)속으로 산소이온을 가소에너지 40keV로 $1\times10^{15}$$1\times10^{18}cm^{-2}$ 주입하고 열처리하여, 다결정실리콘막(230)의 중간 부분에 실리콘산화물의 제1원자도입층(240)을 형성하였다(제2도(b)).

(III) 다음단계로, 다결정실리콘막(230)의 표면상에 실리콘이온을 가속에너지 2keV로 1×10^{15}-$1\times10^{18}cm^{-2}$ 주입하고 열처리하여, 다결정실리콘막(230)의 표면상에 무정형실리콘으로 구성된 제2원자도입층(290)을 형성하였다(제2도(c)).

(IV) 물리증착법에 의해서 대략 100nm의 얇은 텅스텐막(250)을 퇴적하였다(제2도(d)).

(V) 500-1000℃에서 10초간 신속하게 열어니일링하거나 500-1000℃에서 30분간 전기오븐에서 열처리하면, 텅스텐 실리사이드에 의한 합금화층(260)이 다결정실리콘막(230)의 표면근처에 형성되었다(제2도(e)).

(VI) 포토마스크공정으로 저항패턴을 형성하여, 게이트전극 형성예정부 및 그의 주변부 이외의 부분을 건식 에칭하여 게이트전극을 형성하였다(제2도(f)).

(VII) As 이온을 가속에너지 80keV로 $4\times10^{15}cm^{-2}$ 주입하여, 소오스영역(270)과 드레인영역(280)을 최종적으로 형성하였다(제2도(g)).

상기 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

제2원자도입층(290)내의 무정형 실리콘은 다결정실리콘보다 텅스텐과 훨씬 쉽게 반응하여 원자도입층과 그 윗부분에서 대부분의 합금화가 일어났다.

그러므로, 두께가 균일한 우수한 합금화층이 얻어졌다.

텅스텐원자의 이동영역은 제2원자도입층(290)의 근처에서 정지되는 것이 가능하였으나, 약간의 텅스텐 원자가 제2원자도입층(290)을 통하여 침투하였다.

그러나, 제1원자도입층(240)내의 실리콘산화물은 효과적으로 텅스텐을 저지하여 대부분의 합금화는 원자도입층(240)의 윗부분으로 제한되었다.

합금화층(260)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 저저항도전체의 국부적인 확산도 덜 발생하여, 게이트산화막의 파괴를 방지할 수 있었다.

본 발명에서는, 제1원자도입층을 형성하는 방법으로서, 이온주입방법을 사용하였으나, 다음의 방법을 사용해도 된다.

즉, 게이트산화막상에 제1층으로서 대략 100nm의 다결정실리콘을 퇴적하고, 이 다결정실리콘막의 게이트전극 형성예정부 및 그의 주변부의 표면상에, 수 nm의 얇은 실리콘막을 선택적으로 형성하여, 대략 100nm의 제2의 다결정실리콘층을 퇴적하고, 이와 같이 선택적으로 형성된 수 nm의 실리콘산화막을 제1원자도입층으로 사용해도 된다.

반면, 제2원자도입층(290)은 선택적으로 형성해도 되나, 적어도 게이트전극 형성예정부와 그의 주변부상에 형성되어야 한다.

[제3실시예]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터에 관한 것으로 제3도(a)-제3도(g)를 참조하여 이하 상세히 설명한다.

(I) 실리콘기판(300)의 능동영역 형성예정부를 제외한 표면에 대략 700nm의 산화막(310)을 피일드산화막으로서 선택적으로 형성하고, 능동영역 형성예정부의 표면에 대략 10nm의 게이트산화막(320)을

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형성한 후, 상기 산화막(310)과 (320)상에 대략 100㎚의 다결정 실리콘막(330)을 퇴적시키고, $POCl_3$를 사용해 인을 확산시켜 다결정실리콘막(330)을 저저항화 하였다(제3도(a)).

(II) 다음 단계로 다결정실리콘막(330)에 산소이온을 가속에너지 10keV로 1×10^{15}-$1\times10^{18}cm^{-2}$ 주입하고 열처리하여, 다결정실리콘막(330)의 표면에 실리콘산화물의 제1원자도입층(340)을 형성하였다(제3도(b)).

(III) 물리증착법에 의해서, 대략 100㎚의 얇은 텅스텐막(350)을 퇴적하였다(제3도(c)).

(IV) 얇은 텅스텐막(350)의 표면상에, 실리콘이온을 가속에너지 20keV로 1×10^{15}-$1\times10^{18}cm^{-2}$ 주입하고, 얇은 텅스텐막(350)내부에 실리콘으로 구성된 제2원자도입층(390)을 형성하였다(제3도(d)).

(V) 500-1000℃에서 10초간 신속하게 열어니일링하거나 500-1000℃에서 30분동안 용광로 어니일링을 통한 열처리에 의해서 얇은 텅스텐막(350)의 내부에 텅스텐 실리사이드의 합금화층(360)을 형성하였다(제3도(e)).

(VI) 다음 단계로, 포토마스크공정으로 저항패턴을 형성하고, 게이트전극 형성 예정부와 그의 인접부분 이외의 다른 부분을 건식 에칭하여, 게이트전극을 형성하였다(제3도(f)).

(VII) 마지막으로, 가속에너지 80keV로 As이온을 $4\times10^{15}cm^{-2}$ 주입하여, 소오스영역(370)과 드레인영역(380)을 형성하였다(제3도(g)).

이상의 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

제2원자도입층(390)내의 실리콘은 결정형이 아니고, 다결정실리콘 보다는 텅스텐과 훨씬 쉽게 반응하여 제2원자도입층(390)의 근접부에서 대부분의 합금화가 일어났다.

그러므로, 두께가 균일한 우수한 합금화층이 얻어졌다.

텅스텐원자의 이동영역은 제2원자도입층(390)내에 거의 국한되고, 약간의 텅스텐원자는 제2원자도입층(390)에 의해 국한되지 않았으나, 제2원자도입층(390)내에 실리콘산화물은 효과적으로 텅스텐을 방해하여, 대부분의 합금화가 제1원자도입층(340)의 윗부분으로 제한되었다.

합금화층(360)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 또 저저항도전체의 국부적인 확산은 거의 발생되지 않아 게이트산화막의 파괴를 방지할 수 있었다.

[제4실시예]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터의 제4실시예에 관한 것으로 제4도(a)-제4도(f)를 참조하여 이하 설명한다.

(I) 실리콘기판(400)의 능동영역 형성예정부를 제외한 표면에 대략 700㎚의 산화막(410)을 피일드산화막으로 선택적으로 형성하고, 능동영역 형성예정부의 표면에 대략 10㎚의 게이트산화막(420)을 형성하여, 상기 산화막(410)과 (420)상에 대략 200㎚의 다결정실리콘막(430)을 퇴적시킨 후, $POCl_3$를 사용해 인을 확산시켜 다결정실리콘막(430)을 저저항화 하였다(제4도(a)).

(II) 물리증착법에 의해서, 대략 100㎚의 얇은 텅스텐막(450)을 퇴적하였다(제4도(b)).

(III) 이런 얇은 텅스텐막(450) 상에 산소이온을 가속에너지 60keV로 $1\times10^{15}\sim1\times10^{18}cm^{-2}$ 주입하여, 얇은 텅스텐막(450)과 다결정실리콘막(430) 사이의 계면부근에 실리콘산화물의 원자도입층(440)을 형성하였다(제4도(c)).

(IV) 다음에, 500-1000℃에서 10초간 신속하게 열어니일링하여, 다결정실리콘막(430)과 얇은 텅스텐막(450)사이의 계면부근에 텅스텐실리사이드의 합금화층(460)를 형성하였다(제4도(d)).

(V) 포토마스크공정에서 저항패턴을 형성하고 게이트전극 형성예정부와 그의 주변부이외의 부분을 건식 에칭하여 게이트전극을 형성하였다(제4도(e)).

(VI) 마지막으로, 가속에너지 80keV로 As 이온을 $4\times10^{15}cm^{-2}$ 주입하여, 소오스영역(470)과 드레인영역(480)을 형성하였다(제4도(f)).

이상의 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

원자도입층(440)의 실리콘산화물은 효과적으로 텅스텐을 방해하여, 대부분의 합금화는 원자도입층의 위부분으로 한정되었다.

합금화층(460)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 저저항도전체의 국부적인 확산도 덜 발생되어 게이트산화막의 파괴를 방지할 수 있었다.

본 발명의 제4실시예에서는, 이온주입에 의해 원자도입층을 형성한 후에도 저저항도전체막을 그대로 사용하였으나, 원자도입층형성후에 이 저저항도전체층의 일부 또는 전부를 제거해도 되며, 동일 또는 다른 저저항도전체막을 다시 퇴적해도 된다.

예를 들면, 이온주입을 위하여 사용된 제1저저항도전체층의 두께를 감축할 수 있으므로, 이온주입의 가속에너지를 저감할 수 있다.

또한, 저저항도전체막을 제거하지 않고, 동일 또는 다른 저저항도전체막을 퇴적하여 복수층의 막을 형성해도 된다.

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예를 들면, 텅스텐막상에 티틴막을 퇴적시키므로서, 보다 좋은 저저항화를 기대할 수 있다.

본 발명의 제4실시예에서는, 저저항도전체로서 텅스텐을 사용하고, 원자도입층의 구성원자로서 산소를 사용하였으나, 제1실시예에서와 같이, 저저항도전체로서 다른 고융점금속 또는 이것의 실리사이드를 사용해도 되며, 원자도입층의 구성원자로서 질소, 실리콘 또는 불활성원자를 사용하면, 게이트절연막의 파괴를 방지하는 동일효과를 얻을 수 있다.

마찬가지로, 원자도입층의 구성원자가 비단결정도전체의 구성원자보다 저저항도전체의 구성원자와 훨씬 쉽게 반응하는 조합의 경우, 저저항도전체의 구성원자와 원자도입층의 구성원자의 상호반응에 의해 균일한 합금화층이 형성되고, 저저항도전체의 국부적인 확산을 억제하여서 게이트절연막의 파괴를 방지하게 된다.

또한, 원자도입층의 구성원자가 저저항도전체의 구성원자보다 비단결정도전체의 구성원자와 훨씬 쉽게 반응하는 조합의 경우, 원자도입층내에서의 저저항도전체내의 구성원자의 확산을 억제하고, 저저항도전체의 국부적인 확산을 억제하여서 게이트절연막의 파괴를 또한 방지한다.

본 발명의 방법에 따라서, 전계효과형 트랜지스터가 게이트전극물질로서 열처리에 의한 다결정실리콘의 합금화를 이용하여 형성되면, 이때, 합금화층의 두께는 상기 설명한 바와 같이 균일해지고, 저저항도전체의 국부적인 확산에 기인한 게이트절연막의 파괴를 방지할 수 있다.

본 발명의 바람질한 실시예로서, 원자도입층을 고조사된 이온주입방법에 의해 형성하는 경우, 이온주입시 발생하는 표면상의 전기전하는 저저항도전체막을 통하여 효과적으로 제거될 수 있으므로, 게이트절연막의 전기적파괴도 방지할 수 있다.

이상, 본 발명의 특정실시예를 기술하였지만, 다른 변형과 변화도 당업자에 의해 실현될 수 있다.

그러므로 본 발명의 정신과 범위를 벗어나지 않는한 이런 모든 변형과 변화를 첨부한 청구범위내에 포함시키고자 한다.

(57) 청구의 범위

청구항 1

기판(100)위에 비단결정도전체막(130)을 형성하는 공정과, 상기 비단결정도전체막내부에 원자를 도입하므로써 원자도입층(140)을 형성하는 공정과, 상기 원자도입층이 형성된 비단결정도전체막상에 저저항도전체막(150)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 2

제1항에 있어서, 기판(100)의 표면위에 절연막(120)을 형성하고, 상기 절연막을 게이트절연막(120)으로서 사용하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 3

제2항에있어서, 반도체장치의 능동영역 형성예정부 상부와 그 근방의 비단결정도전체막내부에만 선택적으로 원자도입층(140)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 4

제3항에 있어서, 저저항도전체층(150)을 구성하고 있는 원자가, 원자도입층(140)아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부의 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

청구항 5

제4항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(130)내부에 원자도입층(140)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 6

기판(400)위에 비단결정도전체막(430)을 형성하는 공정과, 상기 비단결정 도전체막상에 저저항도전체막(450)을 형성하는 공정과, 상기 비단결정도전체막과 상기 저저항도전체막내부중 적어도 한쪽에 원자를 도입하므로서 원자도입층(440)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 7

제6항에 있어서, 비단결정도전체막(430)상에 형성된 저저항도전체막(450)을, 원자도입층(440)을 형성한 후 제거하고, 비단결정도전체막상에 다시 저저항도전체막(450)을 형성하는 것을 특징으로 하는 반도체 장치의 제조방법.

청구항 8

제7항에 있어서, 저저항도전체막(450)은 다층막을 형성하도록 비단결정도전체막(430)상에 복수회 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 9

제8항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(430) 내부에 원자도입층

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(440)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 10

기판(200)위에 비단결정도전체막(230)을 형성하는 공정과, 상기 비단결정도전체막내부에 제1원자를 도입하므로서 제1원자도입층(240)을 형성하는 공정과, 상기 비단결정도전체막내부에 제2원자를 도입하므로서 상기 제1원자도입층을 깊이보다도 얕게 제2원자도입층(290)을 형성하는 공정과, 상기 두개의 원자도입층(240),(290)이 형성된 비단결정도전체막상에 저저항도전체막(250)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 11

제10항에 있어서, 반도체장치의 능동영역 형성예정부상부와 그 근방의 비단결정도전체막내부에만 선택적으로 제1원자도입층(240)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 12

제11항에 있어서, 저저항도전체막(250)을 구성하고 있는 원자가, 제1원자도입층(240)아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부의 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

청구항 13

제12항에 있어서, 비단결정도전체막(230)을 적어도 두 번 퇴적하여 형성하고, 첫 번째 퇴적후 비단결정도전체의 표면근방에 제1원자로 구성된 제1원자도입층(240)을 형성한 후에만, 비단결정도전체막의 다음 퇴적을 시행하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 14

제13항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(230)내부에 원자도입층(240)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 15

기판(300)위에 비단결정도전체막(330)을 형성하는 공정과, 상기 비단결정도전체막내부에 제1원자를 도입하므로서 제1원자도입층(340)을 형성하는 공정과, 상기 제1원자도입층이 형성된 비단결정도전체막상에 저저항도전체막(350)을 형성하는 공정과, 상기 비단결정도전체막상에 형성된 저저항도전체막내부에 제2원자를 도입하므로서 제2원자도입층(390)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구항 16

제15항에 있어서, 반도체장치의 능동영역 형성예정부 상부와 그 근방의 비단결정도전체막내부에만 선택적으로 제1원자도입층(340)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 17

제16항에 있어서, 저저항도전체막(350)을 구성하고 있는 원자가, 제1원자도입층 아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

청구항 18

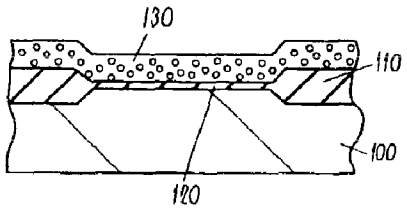
제17항에 있어서, 비단결정도전체막(330)을 적어도 두번 퇴적하여 형성하고, 첫번째 퇴적후 비단결정도전체의 표면근방에 제1원자로 구성된 제1원자도입층(340)을 형성한 후에만, 비단결정도전체막의 다음 퇴적을 시행하는 것을 특징으로 하는 반도체장치의 제조방법.

청구항 19

제18항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(330)내부에 원자도입층(340)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

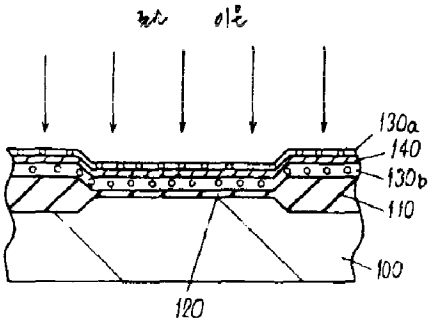
도면

도면1A

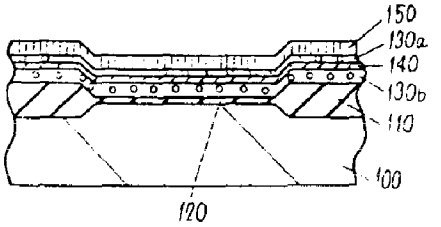


GF Exhibit 1126 - 1985/2248

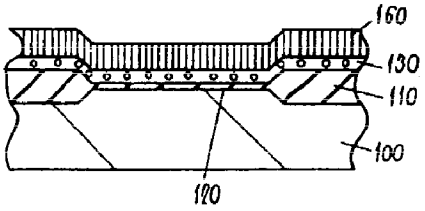
도면1-B



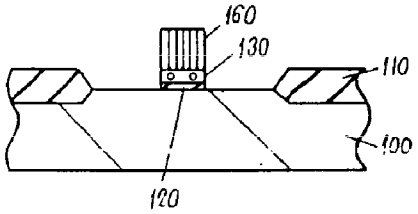
도면1-C



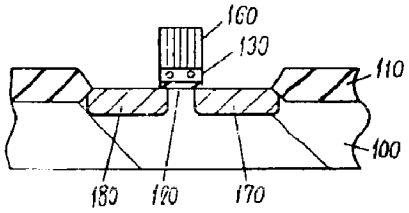
도면1-D



도면1-E

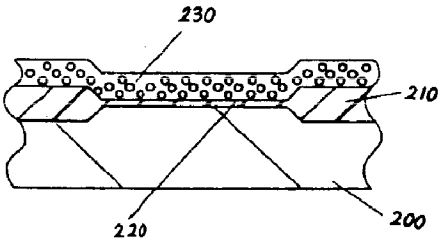


도면1-F

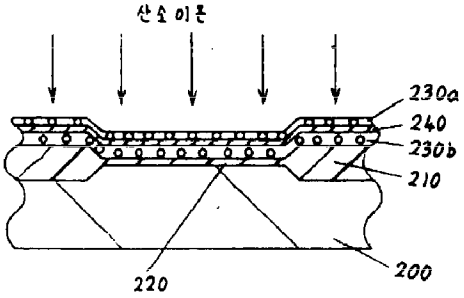


GF Exhibit 1126 - 1986/2248

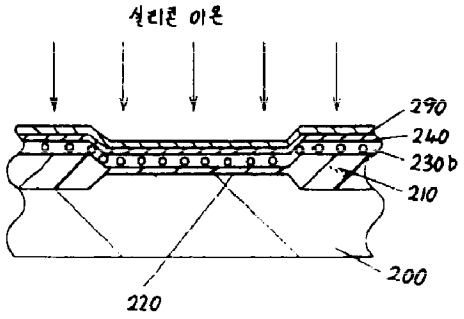
도면2-A



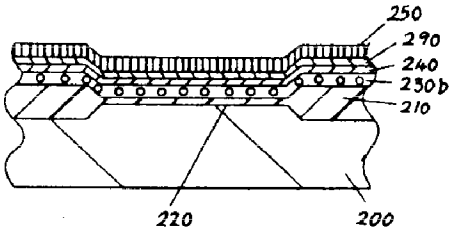
도면2-B



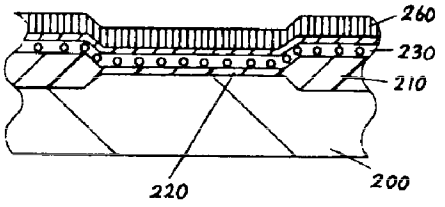
도면2-C



도면2-D

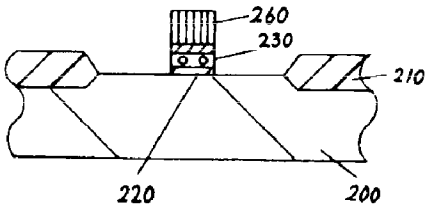


도면2-E

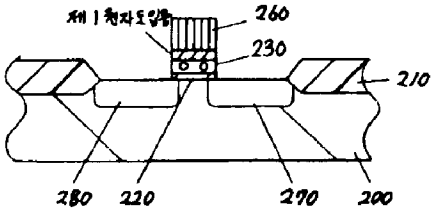


GF Exhibit 1126 - 1987/2248

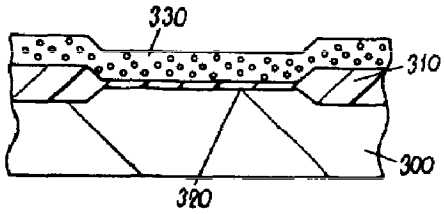
도면2-F



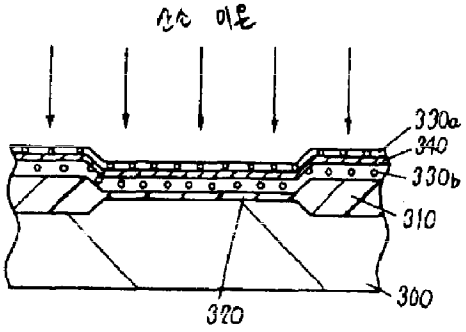
도면2-G



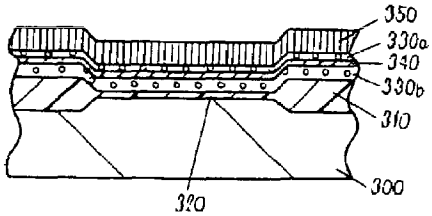
도면3-A



도면3-B

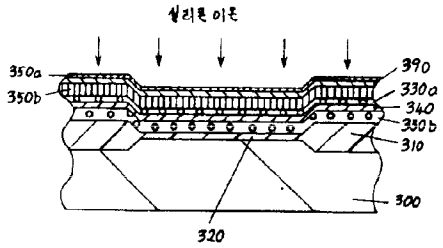


도면3-C

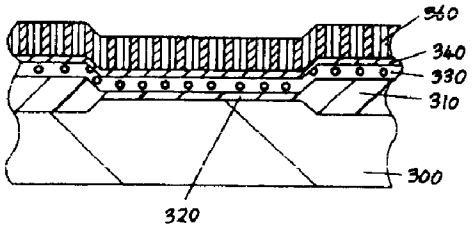


GF Exhibit 1126 - 1988/2248

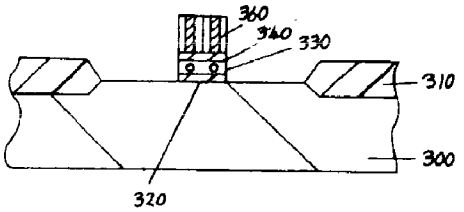
도면3-D



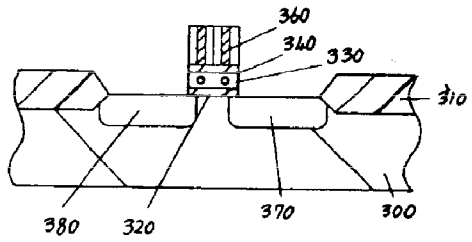
도면3-E



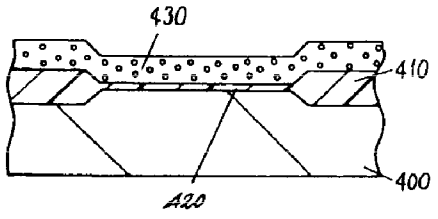
도면3-F



도면3-G

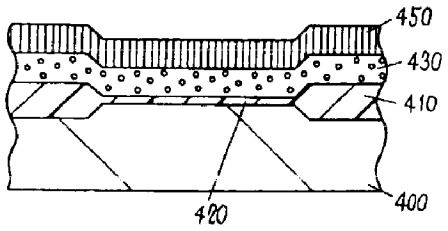


도면4-A

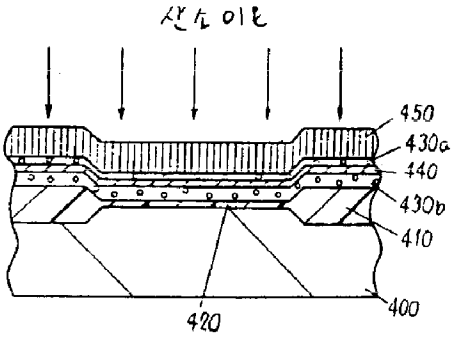


GF Exhibit 1126 - 1989/2248

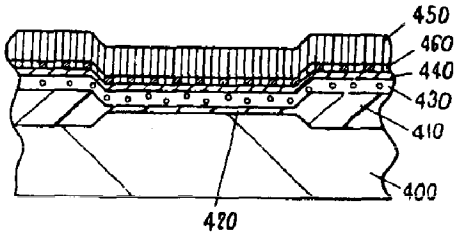
도면4-B



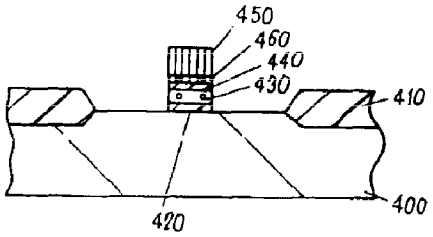
도면4-C



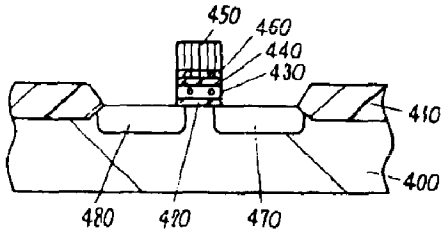
도면4-D



도면4-E



도면4-F



GF Exhibit 1126 - 1990/2248

Bibliographic Data

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Agent.	SHIN, Joong Hoon
Inventor	GoBuSiGaJeuHiRo | GaMeYaMaSyuUIJji | OGaDaSyoOJyoO | JjeuJiGaJeuHiGo
Applicant	PANASONIC CORPORATION
Rightholder	-Maysushita electric ind.

발명의 명칭

반도체장치의제조방법

Title of Invention

Method for fabricating semiconductor device.

요약

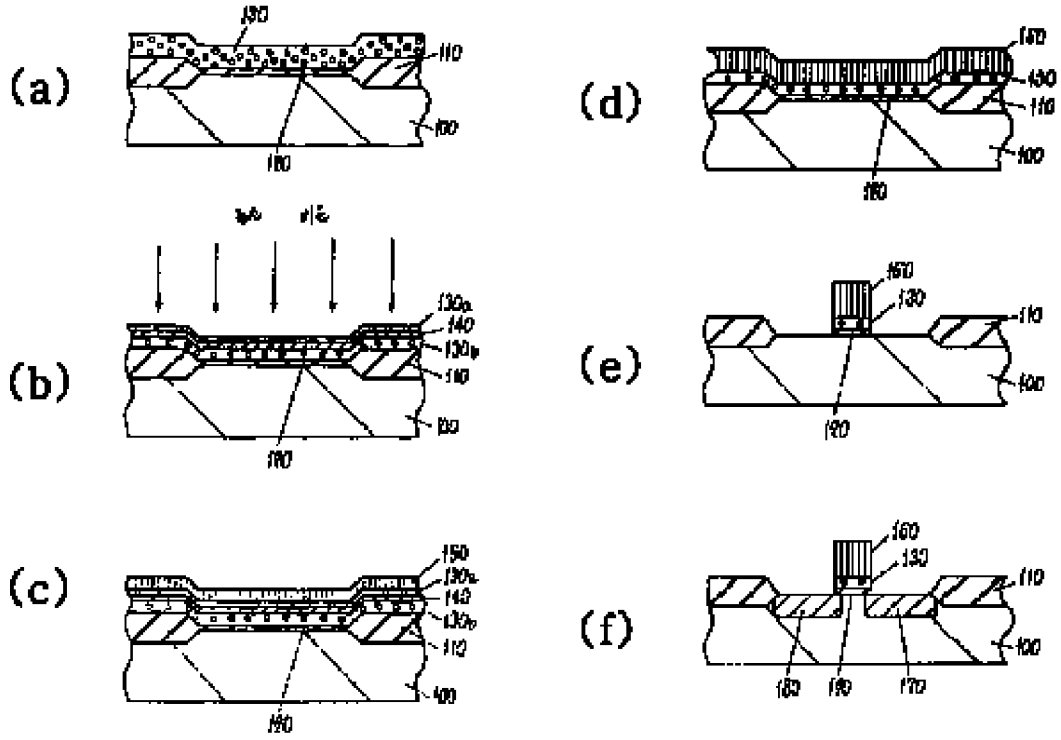
내용 없음.

Abstract

Content none.

대표도면(Representative drawing)

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청구의 범위

청구 1항:

기판(100)위에 비단결정도전체막(130)을 형성하는 공정과, 상기 비단결정도전체막내부에 원자를 도입하므로써 원자도입층(140)을 형성하는 공정과, 상기 원자도입층이 형성된 비단결정도전체막상에 저저항도전체막(150)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

청구 2항:

제1항에 있어서, 기판(100)의 표면위에 절연막(120)을 형성하고, 상기 절연막을 게이트절연막(120)으로서 사용하는 것을 특징으로 하는 반도체장치의 제조방법.

청구 3항:

제2항에있어서, 반도체장치의 능동영역 형성예정부 상부와 그 근방의 비단결정도전체막내부에만 선택적으로 원자도입층(140)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

청구 4항:

제3항에 있어서, 저저항도전체층(150)을 구성하고 있는 원자가, 원자도입층(140)아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부의 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

Scope of Claims

Claim 1:

The method for fabricating semiconductor device consisting of the process of forming the non-single crystal conductor film (130) on the substrate (100), the process of forming the atom introduction layer (140) by introducing the atom inside the non-single crystal conductor film, and the process of forming the low resistance conductor film (150) on the non-single crystal conductor film, and as to the process of, the atom introduction layer is formed.

Claim 2:

As for claim 1, the method for fabricating semiconductor device which forms the insulating layer (120) on the surface of the substrate (100) ; and uses the insulating layer as the gate insulating layer (120).

Claim 3:

As for claim 2, the method for fabricating semiconductor device which selectively forms the atom introduction layer (140) inside the active region formation presumptive region upper portion of the semiconductor device and non-single crystal conductor film of the neighborhood.

Claim 4:

As for claim 3, the method for fabricating semiconductor device which is designed to enough distance in order to prevent being diffused through the valence comprising the low resistance conductive filler layer (150), and the sub-layer under the atom introductio

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n layer (140) and entering into the end of the active re gion formation presumptive region of the semiconductor device forcibly.

청구 5항:

제4항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(130)내부에 원자도입층(140)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 5:

As for claim 4, the method for fabricating semiconductor device which forms the atom introductio n layer (140) inside the non-single crystal conductor fil m (130) since it introduces the atom with the ion impla ntation.

청구 6항:

기판(400)위에 비단결정도전체막(430)을 형성하는 공정과, 상기 비단결정 도전체막상에 저저항도전체막(450)을 형성하는 공정과, 상기 비단결정도전체막과 상기 저저항도전체막내부중 적어도 한쪽에 원자를 도입하므로서 원자도입층(440)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

Claim 6:

The method for fabricating semiconductor device consisting of the process of forming the non-single cry stal conductor film (430) on the substrate (400), the p rocess of forming the low resistance conductor film (45 0) on the non-single crystal conductor film, and the no n-single crystal conductor film and the process of formi ng the atom introduction layer (440) among the low res istance conductor film inside since it introduces the ato m to at least one side.

청구 7항:

제6항에 있어서, 비단결정도전체막(430)상에 형성된 저저항도전체막(450)을, 원자도입층(440)을 형성한 후 제거하고, 비단결정도전체막상에 다시 저저항도전체막(450)을 형성하는 것을 특징으로 하는 반도체 장치의 제조방법.

Claim 7:

As for claim 6, the method for fabricating semiconductor device which removes the atom introdu ction layer (440) the formed low resistance conductor f ilm (450) on the non-single crystal conductor film (430) after doing the formation ; and again forms the low resi stance conductor film (450) on the non-single crystal c onductor film.

청구 8항:

제7항에 있어서, 저저항도전체막(450)은 다층막을 형성하도록 비단결정도전체막(430)상에 복수회 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 8:

As for claim 7, the method for fabricating semiconductor device which it forms on the non-single crystal conductor film (430) so that the low resistance conductor film (450) forms the multilayer.

청구 9항:

제8항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(430) 내부에 원자도입층(440)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 9:

As for claim 8, the method for fabricating semiconductor device which forms the atom introductio n layer (440) inside the non-single crystal conductor fil m (430) since it introduces the atom with the ion impla ntation.

청구 10항:

기판(200)위에 비단결정도전체막(230)을 형성하는 공정과, 상기 비단결정도전체막내부에 제1원자를 도입하므로서 제1원자도입층(240)을 형성하는 공정과, 상기 비단결정도전체막내부에 제2원자를 도입하므로서 상기 제1원자도입층을 깊이보다도 얕게 제2원자도입층(290)을 형성하는 공정과, 상기 두 개의 원자도입층(240),(290)이 형성된 비단결정도전체막상에 저저항도전체막(250)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

Claim 10:

The method for fabricating semiconductor device consisting of the process of forming the non-single cry stal conductor film (230) on the substrate (200), the p rocess of forming the first circle toll dialing mouth layer (240) since it introduces the first circle person inside t he non-single crystal conductor film, the process it is s hallow than the depth of forming the second circle toll dialing mouth layer (290) said first circle toll dialing the mouth layer since it introduces the second circle perso n inside the non-single crystal conductor film, and the process of forming the low resistance conductor film (2 50) on the non-single crystal conductor film, and as to the process of, two atom introduction layers (240), an d (290) are formed.

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청구 11항:

제10항에 있어서, 반도체장치의 능동영역 형성예정부상부와 그 근방의 비단결정도전체막내부에만 선택적으로 제1원자도입층(240)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 11:

As for claim 10, the method for fabricating semiconductor device which selectively forms the first circle toll dialing mouth layer (240) inside the active re gion formation predetermine flotation part of the semic onductor device and non-single crystal conductor film of the neighborhood.

청구 12항:

제11항에 있어서, 저저항도전체막(250)을 구성하고 있는 원자가, 제1원자도입층(240)아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부의 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

Claim 12:

As for claim 11, the method for fabricating semiconductor device which is designed to enough dist ance in order to prevent being diffused through the val ence comprising the low resistance conductor film (25 0), and the sub-layer under the first circle toll dialing m outh layer (240) and entering into the end of the activ e region formation presumptive region of the semicondu ctor device forcibly.

청구 13항:

제12항에 있어서, 비단결정도전체막(230)을 적어도 두 번 퇴적하여 형성하고, 첫 번째 퇴적후 비단결정도전체의 표면근방에 제1원자로 구성된 제1원자도입층(240)을 형성한 후에만, 비단결정도전체막의 다음 퇴적을 시행하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 13:

As for claim 12, the method for fabricating semiconductor device which accumulates the non-singl e crystal conductor film (230) with at least twice and i t forms ; and implements the next deposition of the no n-single crystal conductor film the first circle toll dialing mouth layer (240) made up of the first circle person in the near surface of the non-single crystal conductor af ter the first deposition in the formation.

청구 14항:

제13항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(230)내부에 원자도입층(240)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 14:

As for claim 13, the method for fabricating semiconductor device which forms the atom introductio n layer (240) inside the non-single crystal conductor fil m (230) since it introduces the atom with the ion impla ntation.

청구 15항:

기판(300)위에 비단결정도전체막(330)을 형성하는 공정과, 상기 비단결정도전체막내부에 제1원자를 도입하므로서 제1원자도입층(340)을 형성하는 공정과, 상기 제1원자도입층이 형성된 비단결정도전체막상에 저저항도전체막(350)을 형성하는 공정과, 상기 비단결정도전체막상에 형성된 저저항도전체막내부에 제2원자를 도입하므로서 제2원자도입층(390)을 형성하는 공정으로 이루어진 것을 특징으로 하는 반도체장치의 제조방법.

Claim 15:

The method for fabricating semiconductor device consisting of the process of forming the non-single cry stal conductor film (330) on the substrate (300), the p rocess of forming the first circle toll dialing mouth layer (340) since it introduces the first circle person inside t he non-single crystal conductor film, the process of for ming the low resistance conductor film (350) on the no n-single crystal conductor film, and the process of form ing the second circle toll dialing mouth layer (390) sinc e it introduces the second circle person on the non-sin gle crystal conductor film inside the formed low resista nce conductor film, and as to the process of, said first circle toll dialing the mouth layer is formed.

청구 16항:

제15항에 있어서, 반도체장치의 능동영역 형성예정부 상부와 그 근방의 비단결정도전체막내부에만 선택적으로 제1원자도입층(340)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 16:

As for claim 15, the method for fabricating semiconductor device which selectively forms the first circle toll dialing mouth layer (340) inside the active re gion formation presumptive region upper portion of the semiconductor device and non-single crystal conductor film of the neighborhood.

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청구 17항:

제16항에 있어서, 저저항도전체막(350)을 구성하고 있는 원자가, 제1원자도입층 아래의 하부층을 통해서 확산되어 반도체장치의 능동영역 형성예정부 단부로 침입하는 것을 방지하도록 충분한 거리로 설계된 것을 특징으로 하는 반도체장치의 제조방법.

Claim 17:

As for claim 16, the method for fabricating semiconductor device which is designed to enough distance in order to prevent being diffused through the valence comprising the low resistance conductor film (350), and the sub-layer under the first circle toll dialing mouth layer and entering into the active region formation presumptive region end of the semiconductor device forcibly.

청구 18항:

제17항에 있어서, 비단결정도전체막(330)을 적어도 두번 퇴적하여 형성하고, 첫번째 퇴적후 비단결정도전체의 표면근방에 제1원자로 구성된 제1원자도입층(340)을 형성한 후에만, 비단결정도전체막의 다음 퇴적을 시행하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 18:

As for claim 17, the method for fabricating semiconductor device which accumulates the non-single crystal conductor film (330) with at least twice and it forms ; and implements the next deposition of the non-single crystal conductor film the first circle toll dialing mouth layer (340) made up of the first circle person in the near surface of the non-single crystal conductor after the first deposition in the formation.

청구 19항:

제18항에 있어서, 이온주입에 의해 원자를 도입하므로서 비단결정도전체막(330)내부에 원자도입층(340)을 형성하는 것을 특징으로 하는 반도체장치의 제조방법.

Claim 19:

As for claim 18, the method for fabricating semiconductor device which forms the atom introduction layer (340) inside the non-single crystal conductor film (330) since it introduces the atom with the ion implantation.

상세설명

Detailed Description

[발명의 명칭]

반도체장치의 제조방법

[Title of invention]

Method for fabricating semiconductor device.

[도면의 간단한 설명]

[Brief description of drawings]

제1도는 본 발명의 제1실시예의 공정순서를 도시한 단면도.

Figure 1 is a cross-sectional view showing the processing procedure of the first preferred embodiment of the invention.

제2도는 본 발명의 제2실시예의 공정순서를 도시한 단면도.

Figure 2 is a cross-sectional view showing the processing procedure according to the second preferred embodiment of the present invention.

제3도는 본 발명의 제3실시예의 공정순서를 도시한 단면도.

Figure 3 is a cross-sectional view showing the processing procedure according to the third preferred embodiment of the present invention.

제4도는 본 발명의 제4실시예의 공정순서를 도시한 단면도.

Figure 4 is a cross-sectional view showing the processing procedure according to the fourth preferred embodiment of the present invention.

* 도면의 주요부분에 대한 부호의 설명

* The description of reference numerals showing the main elements in drawings.

100,200,300,400 : 실리콘기판 110,210,310,410 : 산화막

100,200,300,400: silicon substrate 110,210,310,410: oxide film.

120,220,320,420 : 게이트 산화막 130,230,330,430 : 다

120,220,320,420: gate oxidation film 130,230,330,430:

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결정 실리콘막

polysilicon layer.

140,440 : 원자도입층 150 : 얇은 티탄막

140,440: atom introduction layer 150: the thin titan film.

160,260,360,460 : 함금화층 170,270,370,470 : 소오스영역

160,260,360,460: box gold 300coin layer 170,270,370,470: source area.

180,280,380,480 : 드레인영역 240,340 : 제1원자도입층

180,280,380,480: drain region 240,340: first circle toll dialing mouth layer.

250,350,450 : 얇은 텅스텐막 290,390 : 제2원자도입층

250,350,450: the thin tungsten film 290,390: second circle toll dialing mouth layer.

[발명의 상세한 설명]

[Detailed description of the invention]

본 발명은 반도체장치의 제조방법에 관한 것으로, 특히 MOS형 집적회로등의 비(非)단결정도전체막과 저(低)저항도전체막으로 구성된 저저항화된 게이트전극의 전기적 특성을 개량하고, 또 게이트절연막의 절약파괴를 방지할 수 있는 제조방법에 관한 것이다.

The invention relates to the method for fabricating semiconductor device, and particularly, to the manufacturing method which improves the electrical characteristic of the gate electrode which becomes to have low-resistance consisting of the low resistance conductor film and non-single crystal conductor film including the MOS type integrated circuit etc. and can prevent and, the saving break down of the gate insulating layer.

전계효과형 반도체집적회로에서 미세하고 고성능의 트랜지스터를 얻기 위하여, 비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성하고 열처리하여 게이전극의 저저항화를 일반적으로 실행한다.

In order that it is minute in the field effect type semiconductor IC(integrated circuit) and the transistor of the high effectiveness is obtained the low resistance conductor film is formed on the gate electrode consisting of the non-single crystal conductor film and it heat-treats and the low resistance of the gay electrode the generally is executed.

예를 들면, 저저항전도체로서, 고융점 금속 또는 실리콘과의 합금, 즉, 실리사이드는 다결정체실리콘상에 퇴적되어 게이트전극으로 사용되고, 약 500℃로 열처리 하면 고융점금속 또는 실리사이드는 쉽게 다결정체실리콘과 반응하여 전부 실리사이드속으로 변형됨으로써 저저항화가 된다.

For example, as the low resistance conductive material, it is accumulated in the polycrystal silicone phase and the alloy with the high melting point metal or the silicone, in other words, the silicide is used as the gate electrode and by if it heat-treats at about 500℃, the high melting point metal or the silicide reacting easily with the polycrystal silicone and being all transformed into inside the silicide it becomes to have low-resistance.

이렇게 형성된 도전체막의 시이트저항은 대략 1-10Ω/스퀘어로 낮아, 반도체집적회로의 고속작동이 예기된다.

The sheet resistance of the conductor film formed in this way is lower than approximately, 1-10Ω / specifying queries as relational expressions and the high-speed of the semiconductor IC(integrated circuit) is expected.

반면, 금속종류에 의존하여, 다결정체실리콘과는 다른 물질과 반응하고, 특히 티탄은 게이트 전극물질로서 사용되는 실리콘산화막과 반응하므로, 비록 이것이 매우 저저항이지만 게이트전극물질로 사용되기는 어렵다.

On the other hand, it depends on steel and it reacts with the material different from the polycrystal silicone and the material reacts to the silicon oxide film in which especially, titanium is used as the gate electrode material. Therefore this is difficult that it is the low resistance but this is very used as the gate electrode material.

따라서, 티탄보다는 약간 고저항이지만 실리콘산화막과는 거의 반응하지 않는, 텅스텐과 몰리브덴이 일반적으로 사용된다.

Therefore, a little bit is the high value resistor than titanium but tungsten and the molybdenum which nearly does not react are generally used with the silicon oxide film.

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이런 고융점금속 또는 실리사이드와 실리콘질화막 또는 실리콘산화막과의 반응성 및 반응물의 생성에너지는 N.G.Einsprach 편(Academic Press 출판)의 VLSI 전자공학 : 미세구조, 제9권, 제2장에 기재되어 있다.

The formation energy of the reactive reactant with such high melting point metal or the silicide and silicon nitride film or the silicon oxide film is the VLSI electronics of the No Good. Einsprach. piece (academic Press publication): it is written in the fine structure, the vol. 9, and the second field.

한편, 반응의 용이성은 활성화에너지의 크기에 의해 판단될 수 있으며, 활성화에너지가 작을수록 반응이 쉬워지는 것은 알려져 있다.

In the meantime, the simplicity of reaction can be determined by the size of the activation energy and the size is known that reaction becomes easy as the activation energy is small.

비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성한 후 열처리하면, 비단결정도전체막과 저저항도전체막사이의 계면에서 상호의 구성원자가 이동하여, 계면부근이 합금화되어, 저저항화된다.

If the low resistance conductor film is heat-treated on the gate electrode consisting of the non-single crystal conductor film after doing the formation , the constitutional atom of reciprocity moves in the interface between the low resistance conductor film and the non-single crystal conductor film and the interface department radical is alloyed and it becomes to have low-resistance.

그러나, 비단결정도전체의 결정입자사이의 계면, 즉, 입자 경계에서, 비단결정도전체의 구성원자의 결합력이 약하므로, 저저항도전체막의 구성원자와의 원자의 치환이 결정입자내에서보다 빠르게 진행되어, 저저항도전체는 입자경계를 따라서 국부적으로 확산되는 경향이 있다.

But in the interface between the crystal particle of the non-single crystal conductor, in other words, the grain boundary, the connectivity of the constitutional atom of the non-single crystal conductor is weak. Therefore the substitution of the atom with the constitutional atom of the low resistance conductor film is rapidly launched than inside of the crystal particle and the low resistance conductor tends to be diffused according to the grain boundary.

저저항도전체가 국부적으로 확산되어 게이트전극 아래의 절연막을 찢게되면, 게이트전극이 다른 전극과 단락되어, 트랜지스터의 신뢰성 또는 제품의 수율을 저하시킨다.

If the low resistance conductor is locally diffused and the insulating layer under the gate electrode is torn , it is circuit-shorted with the electrode in which the gate electrode is different and the yield of the reliability of the transistor or the product is lowered.

이것을 방지하기 위해, 비단결정도전체와 저저항도전체 사이에 CVD(화학적 증착)에 의해 초박형의 실리콘질화막을 퇴적시켜 저저항도전체의 국부적인 확산을 억제하고 신뢰성을 증가시키는 방법이 IEEE Transactions of Electron Devices, Vol., ED-33, No.4, April 1986, pp. 464~467에 언급되어 있다.

In order that this is prevented the non-single crystal conductor and the method for sedimenting the silicon nitride film of the ultra thin between the low resistance conductor with the CVD (chemical vapor deposition) and suppressing the local diffusion of the low resistance conductor and increasing the reliability are mentioned in the IEEE Transactions of Electron Devices, vol, ED-33, no.4, april 1986, pp. 464~467.

그러나 이것은 막두께의 고재현성에서, CVD에 의한 초박편실리콘 질화막의 퇴적은 어렵고, 더욱이 비교적 낮은 온도에서의 퇴적과 불순물확산층내의 불순물의 재확산에 기인한 전기적 특성에의 변화를 방지하는 것이 필요하므로, 저저항도전체의 국부적 확산을 충분히 억제하는 조밀막성질을 얻기가 곤란하여, 신뢰성과 수율의 향상 또는 충분하지가 않았다.

But in this is the high reproducibility of the film thickness, the deposition of the ultra-thin section silicon nitride film by CVD was difficult and the change was necessary to prevent the change of the electrical characteristic of being caused by the respread of the impurity within the deposition at the relatively low temperature and impurity spreading layer. Therefore it was difficult to get the density coating property which enough suppressed the local diffusion of the low resistance conductor and it improved of the reliability and yield or it was not sufficient.

상기 문제점을 해결하기 위해 본 발명의 일차적 목적은 저저항도전막의 구성원자와 비단결정도전체막의 구성원자사이의 양막의 계면부근에서의 치환을 제한하여, 입자경계를 따른 저저항도전체의 국부적인 확산을 억제하고 게이트전극의 전기저항을 균일하게 감소시켜 신뢰성을 향상시킨 반도체장치의 제조방법을 제공하는데 있다.

To solve the problem, the primary object of the invention limits the substitution at the interface department radical of the amnion between the constitutional atom of the constitutional atom of the low resistance conductive film and the non-single crystal conductor film and the local diffusion of the low resistance conductor following the grain boundary is to be suppressed and th

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e electric resistance of the gate electrode is uniformly reduced and the method for fabricating semiconductor device improving the reliability is to be provided.

본 발명의 다른 목적은 절연막상에 비단결정도전체막을 형성하는 공정과, 상기 비단결정도전체막속에 최소한 한 종류의 원자를 도입하여 원자도입층을 형성하는 공정과, 상기 비단결정도전체막상에 저저항도전체막을 형성하는 공정과, 상기 비단결정도전체막상에 형성된 저저항도전체막을 열처리하는 공정을 포함하여, 비단결정도전체막표면으로부터 침입한 저저항도전체막의 원자가 원자도입층내에서 편재되거나 정지되는 특징을 지닌 반도체장치의 제조방법을 제공하는데 있다.

Another object of the invention is to provide the method for fabricating semiconductor device carrying t he characteristic in which the atom of the low resistan ce conductor film breaking from the non-single crystal conductor film surface is maldistributed including the pr ocess, of forming the non-single crystal conductor film on the insulating layer and the process, of introducing the atom of at least one kind in the non-single crystal conductor film and forming the atom introduction layer and the process, of forming the low resistance conduct or film on the non-single crystal conductor film and the process of heat-treating the formed low resistance con ductor film on the non-single crystal conductor film in t he atom introduction layer or which is stopped.

본 발명의 제조방법에 따라서, 비단결정도전체막으로 구성된 게이트전극상에 저저항도전체막을 형성하고 열처리하여 게이트전극을 저저항화하므로써, 비단결정도전체의 구성원자와 저저항도전체막의 구성원자와의 상호원자치환은 두막의 계면의 제한된 영역에서만 균일하게 일어날 수 있다.

According to the manufacturing method of the invention, the low resistance conductor film is formed o n the gate electrode consisting of the non-single cryst al conductor film and it heat-treats and the gate electr ode is made lower resistance. In that way the reciproci ty atom substitution with the constitutional atom of th e constitutional atom of the non-single crystal conduct or and low resistance conductor film uniformly can occ ur in the limited domain of the interface of two films.

더욱이, 게이트전극의 전기저항이 일정하게 저감됨과 동시에, 입자경계를 따른 저저항도전체의 국부적인 확신이 억제될 수 있어, 결국, 신뢰성이 향상된 반도체장치를 제공하는 것이 가능하다.

Furthermore, the electric resistance of the gate electrode is regularly reduced. Simultaneously the local assurance of the low resistance conductor following th e grain boundary can be suppressed and it is possible t o provide the semiconductor device in which in conclusi on, the reliability is improved.

본 발명의 신규한 특징은 특히, 첨부한 청구범위에 나타내었고, 본 발명의 구성과 내용에 대해서는 기타 다른 목적들과 특징에 따라, 도면과 함께 상세한 설명으로 충분히 이해될 수 있을 것이다.

It showed in the claims which the characteristic which is novel of the invention especially attached and it will be able to be enough understood as the detailed expla nation about configuration and content of the present i nvention according to the purposes and the characteri stic which the other is different with drawing.

[제1실시예]

[First preferred embodiment]

본 발명의 제1실시예는 제1도(a)-제1도(f)를 참조하여, 게이트전극에 다결정실리콘과, 티탄을 조합시킨 전계효과형 금속-산화물-반도체(MOS)와 관련하여 상세히 설명한다.

The first preferred embodiment of the invention the first (a) particularly illustrates with reference to the firs t (f) in the gate electrode in connection with the poly-crystal silicon, and the field effect type metal-oxide-se miconductor (MOS) combining titanium.

(I) 실리콘기파(100)의 농동영역 형성 예정부를 제외한 표면에 대략 700nm의 산화막(110)을 피일드 산화막으로서 선택적으로 형성하고, 능동영역 형성 예정부의 표면에 대략 10nm의 게이트산화막(120)을 형성하고, 상기 산화막(110)과 (120)상에 대략 200nm의 다결정 실리콘막(130)을 퇴적시키고, POCl3를 사용해 인을 확산시켜 다결정실리콘막(130)을 저저항화하였다(제1도(a)).

(I)Approximately, the oxide film (110) of 700nm was selectively formed on the surface except for the same field formation presumptive region of the silicon group wave (100) as the field oxide film and approximately, th e gate oxidation film (120) of 10nm was formed on the surface of the active region formation presumptive regi on and approximately, the polysilicon layer (130) of 200 nm was sedimented on the oxide film (110) and (120) a nd the phosphorus was diffused by using the POCl 3 an d the polysilicon layer (130) was made lower resistance (first (a)).

(II) 다음 단계로, 다결정실리콘막(130)에 질소이온을 가속에

(II)The nitrogen ion was injected into the polysilicon

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너지 150KeV로 1#215#1015~1#215#1018cm-2 주입하고, 다결정실리콘막(130)의 중간부분에 원자도입층(140)을 형성하였다(제1도(b)).

layer (130) to the following step to the acceleration energy 150KeV with 1× 10 15 ~1× 10 18 cm - 2 and the atom introduction layer (140) was formed on the middle part of the polysilicon layer (130)(first (b)).

(III) 물리증착법에 의해서, 대략 100nm의 얇은 티탄막(150)을 퇴적하였다(제1도(c)).

(III)Using the physical vapour deposition, the thin titan film (150) of 100nm was approximately accumulated(first (c)).

(IV) 500-1000℃에서 10초간 신속하에 열어니일링하거나 500-1000℃에서 30분동안 용광로어니일링에 의한 열처리에 의해서, 질화티탄 및 티탄 실리사이드가 생성되어, 합금화층(160)이 형성되었다(제1도(d)).

(IV)In 500-1000℃, annealed thermally under for 10 seconds rapid or the titane nitride and titanium silicide were generated in 500-1000℃ for 30 minutes with the thermal process by the blast furnace annealing and the alloy layer (160) was formed(first (d)).

(V) 다음 단계로, 포토마스크공정으로 저항패턴을 생성하고, 게이트전극 형성 예정부 및 그의 주변부부 이외의 다른 부분을 건식 에칭하여, 게이트전극을 형성하였다(제1도(e)).

(V)The resistance pattern was produced to the following step to the photo mask process and the dissimilar part except the gate electrode forming presumptive region and its peripheral unit part dry were etched and the gate electrode was formed(first (e)).

(VI) 마지막으로, 가속에너지 80KeV로 As 이온을 4#215#1015cm-2 주입하여, 소오스영역(170) 및 드레인영역(180)을 형성하였다(제1도(f)).

(VI)Finally, the As ion was injected to the acceleration energy 80KeV with 4× 10 15 cm - 2 and the source area (170) and drain region (180) were formed(first (f)).

이상의 일련의 공정에 의해서, 소망하는 전계효과형 트랜지스터가 형성되었다.

Using the series of process described in the above, the desired field effect transistor was formed.

질소원자도입층(140)은 다결정실리콘 보다는 티탄과 반응하기 훨씬 쉽고, 원자도입층(140) 및 그의 윗부분에서 대부분의 합금화가 일어났다.

The nitrogen atom introduction layer (140) was more easy than the poly-crystal silicon to react with titanium and most of alloyings occurred in the atom introduction layer (140) and its top.

따라서, 합금화층의 두께가 균일하게 되므로, 게이트전극의 전기저항이 균일해지고 또한, 저저항도 전체의 국부적인 확산도 거의 발생하지 않게 되어, 게이트산화막의 파괴를 방지할 수 있었다.

Therefore, it became uniformly the thickness of the alloy layer. Therefore the electric resistance of the gate electrode was uniform and moreover, the low resistance the local diffusion of whole was not generated and the break down of the gate oxidation film could be prevented.

한편, 제1실시예의 공정(II)에서, 게이트산화막과 그 주변에 걸쳐서 상기 다결정층내에 원자도입층을 선택적으로 형성하고, 원자가 도입되지 않은 부분을 다음 공정의 저저항배선영역으로 사용하면, 이 부분에서는 저저항도전체막과 합금화층이 다결정실리콘막의 거의 전역에 퍼져서, 다결정실리콘과 저저항도전체막 사이의 접속저항을 낮출 수 있다.

In the meantime, in the process (II) of the first preferred embodiment, the atom introduction layer is selectively formed through the gate oxidation film and around within the polycrystalline layer and if the part in which the atom is not introduced is used as the low resistance wiring domain of the next process , the low resistance conductor film and alloy layer nearly spread to all the area from the teeth of the polysilicon layer and the contact resistance between the low resistance conductor film and the poly-crystal silicon can be lowered.

그러므로, 게이트산화막에 대한 인가전계의 도전성은 개량된다.

Therefore, the conductivity of the applied field about the gate oxidation film is improved.

배선영역아래의 산화막은 두꺼우므로, 저저항도전체가 산화막내에 국부적으로 확산되는 것은 문제가 되지 않는다.

The oxide film under the wiring area is thick. Therefore it does not become a problem that the low resistance conductor is locally diffused within the oxide film.

이때에, 게이트산화막의 단부에서부터 저저항배선영역까지의 거리는 다음과 같이 규정되는 것이 바람직하다.

Even in this case, in the end of the gate oxidation film, it is the be desirable that the distance to the low resistance wiring domain is prescribed like the next.

즉, 저저항도전체막의 구성원자가 저저항배선영역으로부터 원

That is, the constitutional atom of the low resistance

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자도입영역의 하부를 통하여 확산되어 게이트 산화막의 단부까지 침입하고 있으므로, 이런 확산길이보다도 긴 길이로 설정하는 것이 바람직하다.

conductor film is diffused through the lower part of the atom lead-in area from the low resistance wiring domain and it breaks to the end of the gate oxidation film. Therefore it is the be desirable to set up as the length longer than such diffusion length.

본 발명의 제1실시예에 있어서는, 저저항도전체로서 티탄을 사용하고, 원자도입층의 구성원자로서 질소를 사용하였으나, 저저항도전체로서 다른 고융점금속 또는 이것의 실리사이드를 사용해도 되며, 원자도입층의 구성원자로서 산소 또는 실리콘 또는 불활성 원자를 사용해도 게이트절연막의 파괴를 방지할 수 있다.

It was in the first preferred embodiment of the invention and titanium was used as the low resistance conductor and nitrogen was used as the constitutional atom of the atom introduction layer. But the silicide of the dissimilar high melting point metal or this is used as the low resistance conductor and the break down of the gate insulating layer can be prevented even if oxygen, the silicone, or the inactive atom is used as the constitutional atom of the atom introduction layer.

그러나, 저저항도전체막의 구성원자와 전자도입층의 구성원자의 조합에 의해, 게이트절연막의 파괴를 방지하는 메타니즘은 다양하다.

But using the combination of the constitutional atom of the constitutional atom of the low resistance conductor film and electron introduction layer, the mechanism preventing the break down of the gate insulating layer is various.

본 발명의 제1실시예인 티탄과 조합의 경우, 즉, 원자도입층의 구성원자가 비단결정도전체의 구성원자보다 저저항전체의 구성원자와 더욱 쉽게 반응할때, 원자도입층의 구성원자와 저저항도전체의 구성원자는 서로 반응하여 균일한 합금화층을 형성하고, 저저항도전체의 국부적인 확산이 억제됨으로써 게이트절연막의 파괴를 방지한다.

In case of titanium and the combination which is the first preferred embodiment of the invention, when it is more easy in other words, the constitutional atom of the atom introduction layer reacts with the constitutional atom of the low resistance whole than the constitutional atom of the non-single crystal conductor , the constitutional atom of the atom introduction layer and constitutional atom of the low resistance conductor react and the uniform alloy layer is formed and the break down of the gate insulating layer is prevented since the local diffusion of the low resistance conductor is suppressed.

또, 비단결정도전체막과 저저항도전체막사이의 접속저항이 느려, 인가된 전계에 대한 게이트산화막의 내구력은 우수하다.

And the contact resistance between the low resistance conductor film and the non-single crystal conductor film are slow and the applied endurance of the gate oxidation film about the electric field is excellent.

또한, 텅스텐과 산소를 조합하는 경우, 즉, 원자도입층의 구성원자가 저저항도전체막의 구성원자보다 비단결정도전체막의 구성원자와 더욱 쉽게 반응하면, 저저항도전체막의 구성원자의 확산은 원자도입층내에서 저지되고, 저저항도전체의 국부적인 확산은 억제되어 게이트절연막의 전기적 파괴를 방지한다.

Moreover, in other words, the constitutional atom of the atom introduction layer is more easy than the constitutional atom of the low resistance conductor film with the constitutional atom of the non-single crystal conductor film the reaction lower-side , and the diffusion of the constitutional atom of the low resistance conductor film are tungsten and oxygen interrupted in case the combination in the atom introduction layer and the local diffusion of the low resistance conductor is suppressed and the electrical breakdown of the gate insulating layer is prevented.

그러므로 저저항화시 저저항도전체막의 막두께가 증가되면, 게이트절연막의 파괴는 효과적으로 방지될 수 있다.

Therefore, if the film thickness of the low resistance conductor film is increased in the low resistance , the break down of the gate insulating layer can be effectively prevented.

또한, 원자도입층을 형성하기 위하여 도입되는 원자는, 1종류 또는 복수종류이어도 된다.

Moreover, the atom which is introduced in order to form the atom introduction layer is 1 kind or the plural species.

[제2실시예]

[The second preferred embodiment]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을

The second (a) particularly illustrates as the field

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조합시킨 전계효과형 트랜지스터에 관한 것으로 제2도(a)-제2도(g)를 참조하여 상세히 설명한다.

effect transistor in which the manufacturing method of the invention combines the poly-crystal silicon and tungsten in the gate electrode with reference to the second (g).

(I) 실리콘기판(200)의 능동영역 형성예정부를 제외한 표면상에, 대략 700nm의 산화막(210)을 피일드 산화막으로서 선택적으로 형성하고, 대략 10nm의 게이트산화막(220)을 능동영역 형성예정부의 표면상에 형성하고, 상기 산화막(210)과 (220)상에 대략 200nm의 다결정실리콘막(230)을 퇴적한 후, POCl3를 사용해 인을 확산시켜서 다결정실리콘막(230)을 저저항화하였다(제2도(a)).

(I)Approximately, the oxide film (210) of 700nm was selectively formed on the surface except for the active region formation presumptive region of the silicon substrate (200) as the field oxide film and approximately, the gate oxidation film (220) of 10nm was formed on the surface of the active region formation presumptive region and the phosphorus was diffused by using the POCl 3 approximately, the polysilicon layer (230) of 200nm on the oxide film (210) and (220) after doing the deposition and the polysilicon layer (230) was made lower resistance(second (a)).

(II) 다음에, 다결정실리콘막(230)속으로 산소이온을 가소에너지 40keV로 1#215#10151#215#1018cm-2 주입하고 열처리하여, 다결정실리콘막(230)의 중간 부분에 실리콘산화물의 제1원자도입층(240)을 형성하였다(제2도(b)).

(II)Next, the oxygen ion was injected inside the polysilicon layer (230) to the calcination energy 40keV with 1× 10 15 1× 10 18 cm -2 and it heat-treated and the first circle toll dialing mouth layer (240) of the silicon oxide was formed on the middle part of the polysilicon layer (230)(second (b)).

(III) 다음단계로, 다결정실리콘막(230)의 표면상에 실리콘이온을 가속에너지 2keV로 1#215#1015-1#215#1018cm-2 주입하고 열처리하여, 다결정실리콘막(230)의 표면상에 무정형실리콘으로 구성된 제2원자도입층(290)을 형성하였다(제2도(c)).

(III)The silicon ion was injected on the surface of the polysilicon layer (230) to the acceleration energy 2keV with 1× 10 15 -1× 10 18 cm - 2 and it heat-treated at the following step and the second circle toll dialing mouth layer (290) consisting of the amorphous silicon was formed on the surface of the polysilicon layer (230)(second (c)).

(IV) 물리증착법에 의해서 대략 100nm의 얇은 텅스텐막(250)을 퇴적하였다(제2도(d)).

(IV)Approximately, the thin tungsten film (250) of 100nm was accumulated with the physical vapour deposition(second (d)).

(V) 500-1000℃에서 10초간 신속하게 열어니일링하거나 500-1000℃에서 30분간 전기오븐에서 열처리하면, 텅스텐 실리사이드에 의한 합금화층(260)이 다결정실리콘막(230)의 표면근처에 형성되었다(제2도(e)).

(V)In 500-1000℃, if it rapidly annealed thermally for 10 seconds or it heat-treated in 30 min. electric oven in 500-1000℃ , the alloy layer (260) by the tungsten silicide was formed in the near surface of the polysilicon layer (230)(second (e)).

(VI) 포토마스크공정으로 저항패턴을 형성하여, 게이트전극 형성예정부 및 그의 주변부 이외의 부분을 건식 에칭하여 게이트전극을 형성하였다(제2도(f)).

(VI)The resistance pattern was formed into the photo mask process and the part except the gate electrode forming presumptive region and its peripheral unit dry were etched and the gate electrode was formed(second (f)).

(VII) As 이온을 가속에너지 80keV로 4#215#1015cm-2 주입하여, 소오스영역(270)과 드레인영역(280)을 최종적으로 형성하였다(제2도(g)).

(VII)The As ion was injected to the acceleration energy 80keV with 4× 10 15 cm - 2 and finally the source area (270) and drain region (280) were formed(second (g)).

상기 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

In said series of process, the desired field effect transistor was formed.

제2원자도입층(290)내의 무정형 실리콘은 다결정실리콘보다 텅스텐과 훨씬 쉽게 반응하여 원자도입층과 그 윗부분에서 대부분의 합금화가 일어났다.

The amorphous silicon within the second circle toll dialing mouth layer (290) more easily reacted with tungsten than the poly-crystal silicon and most of alloyings occurred in the atom introduction layer and top.

그러므로, 두께가 균일한 우수한 합금화층이 얻어졌다.

Therefore, the excellent alloy layer in which the thickness was uniform was obtained.

GF Exhibit 1126 - 2001/2248

텅스텐원자의 이동영역은 제2원자도입층(290)의 근처에서 정지되는 것이 가능하였으나, 약간의 텅스텐 원자가 제2원자도입층(290)을 통하여 침투하였다.

It was possible that the movement area of the tungsten atom was nearby stopped of the second circl e toll dialing mouth layer (290). But the some tungsten atom penetrated through the second circle toll dialing mouth layer (290).

그러나, 제1원자도입층(240)내의 실리콘산화물은 효과적으로 텅스텐을 저지하여 대부분의 합금화는 원자도입층(240)의 윗부분으로 제한되었다.

But the silicon oxide within the first circle toll dialing mouth layer (240) effectively interrupted tungsten and most of alloyings were limited within the top of the ato m introduction layer (240).

합금화층(260)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 저저항도전체의 국부적인 확산도 덜 발생하여, 게이트산화막의 파괴를 방지할 수 있었다.

The thickness of the alloy layer (260) was very uniform. Therefore the electric resistance of the gate e lectrode was uniform and the local diffusion of the low resistance conductor was generated and the break do wn of the gate oxidation film could be prevented.

본 발명에서는, 제1원자도입층을 형성하는 방법으로서, 이온주입방법을 사용하였으나, 다음의 방법을 사용해도 된다.

In the present invention, as the method for forming the first circle toll dialing mouth layer, the ion implantation method was used. But the following method is used.

즉, 게이트산화막상에 제1층으로서 대략 100nm의 다결정실리콘을 퇴적하고, 이 다결정실리콘막의 게이트전극 형성예정부 및 그의 주변부의 표만상에, 수 nm의 얇은 실리콘막을 선택적으로 형성하여, 대략 100nm의 제2의 다결정실리콘층을 퇴적하고, 이와 같이 선택적으로 형성된 수 nm의 실리콘산화막을 제1원자도입층으로 사용해도 된다.

That is, the first layer on the gate oxidation film, approximately, the poly-crystal silicon of 100nm can be used as the first circle toll dialing mouth layer the silico n oxide film of several nm which accumulates and it sel ectively forms the thin silicon film of several nm on the gate electrode forming presumptive region of this polysi licon layer and table all things in the universe of its peri pheral unit and it accumulates approximately, the seco nd polycrystalline silicon layer of 100nm and is selectiv ely formed in this way.

반면, 제2원자도입층(290)은 선택적으로 형성해도 되나, 적어도 게이트전극 형성예정부와 그의 주변부상에 형성되어야 한다.

On the other hand, the second circle toll dialing mouth layer (290) selectively forms. But it has to be formed o n at least gate electrode forming presumptive region an d its peripheral unit.

[제3실시예]

[The third preferred embodiment]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터에 관한 것으로 제3도(a)-제3도(g)를 참조하여 이하 상세히 설명한다.

The third (a) hereinafter particularly illustrates as the field effect transistor in which the manufacturing meth od of the invention combines the poly-crystal silicon an d tungsten in the gate electrode with reference to the third (g).

(I) 실리콘기판(300)의 능동영역 형성예정부를 제외한 표면에 대략 700nm의 산화막(310)을 피일드산화막으로서 선택적으로 형성하고, 능동영역 형성예정부의 표면에 대략 10nm의 게이트산화막(320)을 형성한 후, 상기 산화막(310)과 (320)상에 대략 100nm의 다결정 실리콘막(330)을 퇴적시키고, POCl 3를 사용해 인을 확산시켜 다결정실리콘막(330)을 저저항화하였다(제3도(a)).

(I)Approximately, the oxide film (310) of 700nm was selectively formed on the surface except for the active region formation presumptive region of the silicon subst rate (300) as the field oxide film and approximately, the polysilicon layer (330) of 100nm approximately, the gat e oxidation film (320) of 10nm was sedimented on the s urface of the active region formation presumptive regio n after doing the formation on the oxide film (310) and (320) and the phosphorus was diffused by using the PO Cl 3 and the polysilicon layer (330) was made lower resi stance(third (a)).

(II) 다음 단계로 다결정실리콘막(330)에 산소이온을 가속에너지 10keV로 1#215#1015-1#215#1018cm-2 주입하고 열처리하여, 다결정실리콘막(330)의 표면에 실리콘산화물의 제1원자도입층(340)을 형성하였다(제3도(b)).

(II)The oxygen ion was injected into the polysilicon layer (330) to the acceleration energy 10keV with 1× 1 0 15 -1× 10 18 cm - 2 and it heat-treated at the follo wing step and the first circle toll dialing mouth layer (3 40) of the silicon oxide was formed on the surface of t he polysilicon layer (330)(third (b)).

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(III) 물리증착법에 의해서, 대략 100nm의 얇은 텅스텐막(350)을 퇴적하였다(제3도(c)).

(III)Using the physical vapour deposition, the thin tungsten film (350) of 100nm was approximately accum ulated(third (c)).

(IV) 얇은 텅스텐막(350)의 표면상에, 실리콘이온을 가속에너지 20keV로 1#215#1015-1#215#1018cm-2 주입하고, 얇은 텅스텐막(350)내부에 실리콘으로 구성된 제2원자도입층(390)을 형성하였다(제3도(d)).

(IV)The silicon ion was injected on the surface of the thin tungsten film (350) to the acceleration energy 20k eV with 1× 10 15 -1× 10 18 cm - 2 and the second cir cle toll dialing mouth layer (390) consisting of the silico ne was formed inside the thin tungsten film (350)(third (d)).

(V) 500-1000℃에서 10초간 신속하게 열어니일링하거나 500-1000℃에서 30분동안 용광로 어니일링을 통한 열처리에 의해서 얇은 텅스텐막(350)의 내부에 텅스텐 실리사이드의 합금화층(360)을 형성하였다(제3도(e)).

(V)In 500-1000℃, rapidly annealed thermally for 10 seconds or the alloy layer (360) of the tungsten silicide was formed at 500-1000℃ for 30 minutes with the ther mal process through the blast furnace annealing inside the thin tungsten film (350)(third (e)).

(VI) 다음 단계로, 포토마스크공정으로 저항패턴을 형성하고, 게이트전극 형성 예정부와 그의 인접부분 이외의 다른 부분을 건식 에칭하여, 게이트전극을 형성하였다(제3도(f)).

(VI)The resistance pattern was formed into the following step into the photo mask process and the dis similar part except the gate electrode forming presumpt ive region and its adjacent part dry were etched and t he gate electrode was formed(third (f)).

(VII) 마지막으로, 가속에너지 80keV로 As이온을 4#215#1015cm-2 주입하여, 소오스영역(370)과 드레인영역(380)을 형성하였다(제3도(g)).

(VII)Finally, the As ion was injected to the acceleration energy 80keV with 4× 10 15 cm - 2 and the source are a (370) and drain region (380) were formed(third (g)).

이상의 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

In the series of process described in the above, the desired field effect transistor was formed.

제2원자도입층(390)내의 실리콘은 결정형이 아니고, 다결정실리콘 보다는 텅스텐과 훨씬 쉽게 반응하여 제2원자도입층(390)의 근접부에서 대부분의 합금화가 일어났다.

The silicone within the second circle toll dialing mouth layer (390) was not crystalline form and it more easily r eacted with tungsten than the poly-crystal silicon and most of alloyings occurred in the neighborhood portion of the second circle toll dialing mouth layer (390).

그러므로, 두께가 균일한 우수한 합금화층이 얻어졌다.

Therefore, the excellent alloy layer in which the thickness was uniform was obtained.

텅스텐원자의 이동영역은 제2원자도입층(390)내에 거의 국한되고, 약간의 텅스텐원자는 제2원자도입층(390)에 의해 국한되지 않았으나, 제2원자도입층(390)내에 실리콘산화물은 효과적으로 텅스텐을 방해하여, 대부분의 합금화가 제1원자도입층(340)의 윗부분으로 제한되었다.

The movement area of the tungsten atom was nearly limited within the second circle toll dialing mouth layer (390) and the some tungsten atom was not limited by t he second circle toll dialing mouth layer (390). But the silicon oxide effectively obstructed tungsten within the second circle toll dialing mouth layer (390) and most of alloyings were limited within the top of the first circle t oll dialing mouth layer (340).

합금화층(360)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 또 저저항도전체의 국부적인 확산은 거의 발생되지 않아 게이트산화막의 파괴를 방지할 수 있었다.

The thickness of the alloy layer (360) was very uniform. Therefore the electric resistance of the gate e lectrode was uniform and and, the local diffusion of the low resistance conductor was not nearly generated an d the break down of the gate oxidation film could be pr evented.

[제4실시예]

[The fourth preferred embodiment]

본 발명의 제조방법은 게이트전극에 다결정실리콘 및 텅스텐을 조합시킨 전계효과형 트랜지스터의 제4실시예에 관한 것으로 제4도(a)-제4도(f)를 참조하여 이하 설명한다.

The fourth (a) explains underneath as the fourth preferred embodiment of the field effect transistor in w hich the manufacturing method of the invention combin es the poly-crystal silicon and tungsten in the gate ele ctrode with reference to the fourth (f).

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(I) 실리콘기판(400)의 능동영역 형성예정부를 제외한 표면에 대략 700nm의 산화막(410)을 피일드산화막으로 선택적으로 형성하고, 능동영역 형성예정부의 표면에 대략 10nm의 게이트산화막(420)을 형성하여, 상기 산화막(410)과 (420)상에 대략 200nm의 다결정실리콘막(430)을 퇴적시킨 후, POCl3를 사용해 인을 확산시켜 다결정실리콘막(430)을 저저항화 하였다(제4도(a)).

(I)Approximately, the oxide film (410) of 700nm was selectively formed on the surface except for the active region formation presumptive region of the silicon subst rate (400) into the field oxide film and approximately, t he gate oxidation film (420) of 10nm was formed on the surface of the active region formation presumptive regi on and after approximately, the polysilicon layer (430) of 200nm was sedimented on the oxide film (410) and (420) the phosphorus was diffused by using the POCl 3 and the polysilicon layer (430) was made lower resistan ce(fourth (a)).

(II) 물리증착법에 의해서, 대략 100nm의 얇은 텅스텐막(450)을 퇴적하였다(제4도(b)).

(II)Using the physical vapour deposition, the thin tungsten film (450) of 100nm was approximately accum ulated(fourth (b)).

(III) 이런 얇은 텅스텐막(450) 상에 산소이온을 가속에너지 60keV로 1#215#1015~1#215#1018cm-2 주입하여, 얇은 텅스텐막(450)과 다결정실리콘막(430) 사이의 계면부근에 실리콘산화물의 원자도입층(440)을 형성하였다(제4도(c)).

(III)The oxygen ion was injected on the thin tungsten film (450) to the acceleration energy 60keV with 1× 10 15 ~1× 10 18 cm - 2 and the atom introduction layer (440) of the silicon oxide was formed on the interface department radical between the thin polysilicon layer (430) and the tungsten film (450)(fourth (c)).

(IV) 다음에, 500-1000℃에서 10초간 신속하게 열어니일링하여, 다결정실리콘막(430)과 얇은 텅스텐막(450)사이의 계면부근에 텅스텐실리사이드의 합금화층(460)를 형성하였다(제4도(d)).

(IV)Next, in 500-1000℃, rapidly annealed thermally for 10 seconds and the alloy layer (460) of the tungsten si licide was formed on the interface department radical b etween the thin tungsten film (450) and the polysilicon layer (430)(fourth (d)).

(V) 포토마스크공정에서 저항패턴을 형성하고 게이트전극 형성예정부와 그의 주변부이외의 부분을 건식 에칭하여 게이트전극을 형성하였다(제4도(e)).

(V)In the photo mask process, the resistance pattern was formed and the part except the gate electrode for ming presumptive region and its peripheral unit dry wer e etched and the gate electrode was formed(fourth (e)).

(VI) 마지막으로, 가속에너지 80keV로 As 이온을 4#215#1015cm-2 주입하여, 소오스영역(470)과 드레인영역(480)을 형성하였다(제4도(f)).

(VI)Finally, the As ion was injected to the acceleration energy 80keV with 4× 10 15 cm - 2 and the source are a (470) and drain region (480) were formed(fourth (f)).

이상의 일련의 공정에서, 소망하는 전계효과형 트랜지스터가 형성되었다.

In the series of process described in the above, the desired field effect transistor was formed.

원자도입층(440)의 실리콘산화물은 효과적으로 텅스텐을 방해하여, 대부분의 합금화는 원자도입층의 위부분으로 한정되었다.

The silicon oxide of the atom introduction layer (440) effectively obstructed tungsten and most of alloyings were restricted to the top area of the atom introductio n layer.

합금화층(460)의 두께가 매우 균일하였으므로, 게이트전극의 전기저항이 균일해지고, 저저항도전체의 국부적인 확산도 덜 발생되어 게이트산화막의 파괴를 방지할 수 있었다.

The thickness of the alloy layer (460) was very uniform. Therefore the electric resistance of the gate e lectrode was uniform and the local diffusion of the low resistance conductor was less generated and the break down of the gate oxidation film could be prevented.

본 발명의 제4실시예에서는, 이온주입에 의해 원자도입층을 형성한 후에도 저저항도전체막을 그대로 사용하였으나, 원자도입층형성후에 이 저저항도전체층의 일부 또는 전부를 제거해도 되며, 동일 또는 다른 저저항도전체막을 다시 퇴적해도 된다.

In the fourth preferred embodiment of the invention, the low resistance conductor film was like that used ev en after forming the atom introduction layer with the io n implantation. But a portion or the whole of this low re sistance conductive filler layer is removed after the ato m introduction layer formation and the identity or the d issimilar low resistance conductor film is again accumul ated.

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예를 들면, 이온주입을 위하여 사용된 제1저저항도전체층의 두께를 감축할 수 있으므로, 이온주입의 가속에너지를 저감할 수 있다.

For example, the thickness of the first low resistance conductive filler layer used for the ion implantation can be reduced. Therefore the acceleration energy of the i on implantation can be reduced.

또한, 저저항도전체막을 제거하지 않고, 동일 또는 다른 저저항도전체막을 퇴적하여 복수층의 막을 형성해도 된다.

Moreover, the low resistance conductor film is not removed and the identity or the dissimilar low resistanc e conductor film is accumulated and the film of the mul ti-layer is formed.

예를 들면, 텅스텐막상에 티틴막을 퇴적시키므로서, 보다 좋은 저저항화를 기대할 수 있다.

For example, the titin film is sedimented on the tungsten film. Therefore the low resistance which is be tter can be expected.

본 발명의 제4실시예에서는, 저저항도전체로서 텅스텐을 사용하고, 원자도입층의 구성원자로서 산소를 사용하였으나, 제1실시예에서와 같이, 저저항도전체로서 다른 고융점금속 또는 이것의 실리사이드를 사용해도 되며, 원자도입층의 구성원자로서 질소, 실리콘 또는 불활성원자를 사용하면, 게이트절연막의 파괴를 방지하는 동일효과를 얻을 수 있다.

In the fourth preferred embodiment of the invention, tungsten was used as the low resistance conductor an d oxygen was used as the constitutional atom of the a tom introduction layer. But the silicide of the dissimilar high melting point metal or this is used the first preferr ed embodiment as the low resistance conductor and if nitrogen, and the silicone or the inactive atom are used as the constitutional atom of the atom introduction lay er , the same effect preventing the break down of the gate insulating layer can be obtained.

마찬가지로, 원자도입층의 구성원자가 비단결정도전체의 구성원자보다 저저항도전체의 구성원자와 훨씬 쉽게 반응하는 조합의 경우, 저저항도전체의 구성원자와 원자도입층의 구성원자의 상호반응에 의해 균일한 합금화층이 형성되고, 저저항도전체의 국부적인 확산을 억제하여서 게이트절연막의 파괴를 방지하게 된다.

Similarly, in case of the combination in which it is more easy the constitutional atom of the atom introduction l ayer reacts with the constitutional atom of the low resi stance conductor than the constitutional atom of the n on-single crystal conductor, the uniform alloy layer is f ormed by the mutual reversal of the constitutional ato m of the constitutional atom of the low resistance con ductor and atom introduction layer and the local diffusi on of the low resistance conductor is suppressed and t he break down of the gate insulating layer is prevente d.

또한, 원자도입층의 구성원자가 저저항도전체의 구성원자보다 비단결정도전체의 구성원자와 훨씬 쉽게 반응하는 조합의 경우, 원자도입층내에서의 저저항도전체내의 구성원자의 확산을 억제하고, 저저항도전체의 국부적인 확산을 억제하여서 게이트절연막의 파괴를 또한 방지한다.

Moreover, in case of the combination in which it is more easy the constitutional atom of the atom introduc tion layer reacts with the constitutional atom of the no n-single crystal conductor than the constitutional atom of the low resistance conductor, the diffusion of the co nstitutional atom within the low resistance conductor within the atom introduction layer is held back and the local diffusion of the low resistance conductor is suppr essed and the break down of the gate insulating layer i s moreover prevented.

본 발명의 방법에 따라서, 전계효과형 트랜지스터가 게이트전극물질로서 열처리에 의한 다결정실리콘의 합금화를 이용하여 형성되면, 이때, 합금화층의 두께는 상기 설명한 바와 같이 균일해지고, 저저항도전체의 국부적인 확산에 기인한 게이트절연막의 파괴를 방지할 수 있다.

According to the method of the invention, if the total crab effect type transistor is formed as the gate electr ode material using the alloying of the poly-crystal silico n by the thermal process , as described above, the thi ckness of the alloy layer is then uniform and the break down of the gate insulating layer caused by the local di ffusion of the low resistance conductor can be prevent ed.

본 발명의 바람질한 실시예로서, 원자도입층을 고조사된 이온주입방법에 의해 형성하는 경우, 이온주입시 발생하는 표면상의 전기전하는 저저항도전체막을 통하여 효과적으로 제거될 수 있으므로, 게이트절연막의 전기적파괴도 방지할 수 있다.

As *** embodiment of the invention, the effectively the case , and the electric charge on the surface gene rated in the ion implantation can be removed using the ion implantation method which becomes the atom intro duction layer with the high irradiance through the low r esistance conductor film. Therefore of forming the elec trical breakdown of the gate insulating layer can preve

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nt.

이상, 본 발명의 특정실시예를 기술하였지만, 다른 변형과 변화도 당업자에 의해 실현될 수 있다.

Over, and the certain embodiment of the invention were described. However over can be materialized by deformation and the dissimilar gradient person skilled in the art.

그러므로 본 발명의 정신과 범위를 벗어나지 않는한 이런 모든 변형과 변화를 첨부한 청구범위내에 포함시키고자 한다.

Therefore, it tries to include within the claims which attaches such all deformations and change as long as it does not deviate from spirit and range of the present invention.

Disclaimer

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⑤4発明の名称　半導体装置

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最終頁に続く

明　細　書

発明の名称　半導体装置

特許請求の範囲

1．第1の導電性を有するIII－V族の第1の半導体領域上に界面準位層とこの界面準位層上に単結晶又は多結晶Siよりなる第2の半導体層とを少なくとも有する制御手段と、該制御手段をはさんで設けられたキヤリアの送受手段とを少なくとも有し、前記界面準位層は前記第2の半導体層が有するフエルミ・レベルを当該界面準位層のフエルミ・レベルにピンニングせしめて成ることを特徴とする半導体装置。

2．前記界面準位層は前記第1の半導体層のエネルギー・ギヤツプに当たる位置に10^{12}／cm／eV以上の界面準位を持つことを特徴とする特許請求の範囲第1項記載の半導体装置。

3．前記界面準位層の厚さは30Å以下になることを特徴とする特許請求の範囲第1項又は第2項記載の半導体装置。

4．前記第2の半導体層は縮退した半導体より成ることを特徴とする特許請求の範囲第1項～第3項のいずれかに記載の半導体装置。

5．エネルギー・バンド・ギヤツプの大きさが前記第1の半導体層の少数キヤリアの存在する界面におけるエネルギー・バンドの端と前記第2の半導体層の多数キヤリアの存在するエネルギー・バンドの端との差よりも大きく、且前記第1の半導体層と同一の導電性を有し、前記制御手段と前記キヤリアの送受手段との間の半導体層の導電性は前記第1の半導体層の導電性とは逆なることを特徴とする特許請求の範囲第1項～第4項のいずれかに記載の半導体装置。

6．エネルギー・バンド・ギヤツプの大きさが前記第1の半導体層の多数キヤリアの存在する界面におけるエネルギー・バンドの端と前記第2の半導体層の多数キヤリアの存在するエネルギー・バンドの端との差よりも大きく、且前記第1の半導体層と逆の導電性を有し、前記制御手段と前記キヤリアの送受手段との間の半導体層の導電性は前記第5項と同一であることを特徴

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とする特許請求の範囲第１項～第４項のいずれかに記載の半導体装置。

発明の詳細な説明

〔発明の利用分野〕

本発明は、高速の電界効果トランジスタに関するものである。

〔発明の背景〕

GaAsやＩｎＰ等の化合物半導体基板を用いたMISFET（Metal Insulator Field Effect Transistor）の断面図を第１図（ａ）に示す。ここで、１はｐ－GaAs基板、２はｎ－GaAs層、３は絶縁膜、４は界面準位層、５はゲート電極、６はソース電極、７はドレイン電極である。絶縁膜３の厚さは、1000～3000Åの間にとるのが通例である。このようなMISFETは、反転型の動作をさせることができるデバイスである。すなわち、ゲート電極５に正の電圧を印加すると、絶縁膜３とｐ－GaAs基板１の界面に電子の反転層８が形成される。反転転層をチヤンネルに用いるため、MISFETは大電流がとれ高速デバイスとしての可能性をもつている。しかし、実際には第１図（ｂ）のバンド構造図に示すように絶縁膜３とｐ－GaAs基板１の界面には、半導体のエネルギー・ギヤップ中央付近に10^{12}～10^{13}／㎠／ｅＶ台の極めて高密度の界面準位の存在する層４（以降、この層を界面準位層４と呼ぶ）が１０～３０Åの厚さで存在することが知られている。特に、化合物半導体では、これを10^{14}㎝$^{-2}$／ｅＶ以下に抑えることは、極めて困難である（例えば、GaAsにおいては、空気中にさらしたり、不純物汚染することにより、酸素原子や金属原子が表面に一層付着したのみで界面準位層が10^{12}㎝$^{-2}$／ｅＶ以上生ずることが知られている。）。このため、従来のMISFETは界面準位のフエルミレベルϕ_{ss}が半導体のフエルミレベルϕ_sに固定される傾向が強く、ゲート電極に正電圧を印加しても表面電位ϕ_sが変動せず反転層が形成され難いという欠点をもつていた。

このように、従来からあるMISFETでは反転層をチヤンネルとして用いることは困難であり、電流を多くとれない。これは高密度の界面準位層が存在し、その界面準位のフエルミレベルが半導体のフエルミレベルに固定される傾向が強いためである。以上説明した如きＭＩＳトランジスターの例はたとえばソリツドーステート　エレクトロニクス〔Solid－State Electronics〕vol．１７，pp７５１～７５９（1974）にみられる。

〔発明の目的〕

本発明の目的は大電流を流すことのできる高速の電界効果トランジスタを提供することにある。

〔発明の概要〕

前述のように、従来からあるMISFETでは界面準位のフエルミレベルが半導体のフエルミレベルに固定される傾向が強い。これは、物理的には、界面準位への半導体側からの電子の充放電時間が、他の領域（例えば、ゲート金属）からの充放電時間よりも短いために、準熱平衡状態が界面準位と半導体との間に成立するからである。

より定量的に記せば、界面準位への半導体側からの電子の充放電時間t_eは、例えば半導体がｎ－GaAsの場合に、１０nsec～１０msecの範囲にあり、より一般に、Ⅲ－Ⅴ族の化合物半導体においても、上記充放電時間は、１０nsec～１０msecの間におさまることが知られている。

一方、ゲート金属からの界面準位への電子の充放電時間t_eは、

$$t_e=\frac{D_{it}\cdot\Delta\phi_{ss}}{v_{th}\cdot N\cdot T_t} \quad \cdots(1)$$

$$T_t=\exp\left[-a\cdot\phi^{1/2}\cdot\left(\frac{m}{m_0}\right)^{1/2}\right] \quad \cdots(2)$$

となる。

但し、

D_{it}：界面準位層４の界面準位密度（㎝$^{-2}$／ｅＶ）

$\Delta\phi_{ss}$：電子の充放電に伴う界面準位のフエルミレベルϕ_{ss}の移動量（ｅＶ）

v_{th}：ゲート金属５中の自由電子の速度（㎝／sec）

Ｎ　：ゲート金属５中の自由電子濃度（㎝$^{-3}$）

T_t：絶縁膜３をトンネルする確率（但し、簡単のためここでは矩形のポテンシヤ

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ル障壁をトンネルすると仮定した。）

d　：絶縁膜3の厚さ（Å）

φ　：電子がトンネルする絶縁膜3による障壁の高さ（eV）

m　：絶縁膜3中の電子の有効質量（g）

m_0：真空中の電子の質量（g）

である。$D_s \cdot \Delta\phi_s \fallingdotseq 10^{12}cm^{-2}$，$v_{th} \fallingdotseq 10^7$ cm／sec，$N \fallingdotseq 10^{22}cm^{-3}$，$\phi \fallingdotseq 4eV$，$m/m_0 \fallingdotseq 0.2$，$d \fallingdotseq 1000Å$（上に列挙した値は、通常のMIS構造の典型値である。）とすれば、

$$\tau_s \fallingdotseq 10^{365}sec$$

となり、$\tau_s \ll \tau_n$となることがわかる。このため、準熱平衡状態は、界面準位と半導体の間に成立することとなり、界面準位のフエルミレベルは、半導体のフエルミレベルに固定されることになる。

したがつて、上述のことからわかるように、界面準位のフエルミレベルをゲート金属のフエルミレベルに固定させるには、$\tau_s \gg \tau_n$となるように、ゲート構造を構成すればよい。

本発明は、上記のゲート構造を実現するために、基本的に次の如き構成を有する。

第1の導電性を有するIII－V族半導体領域上に界面準位層とこの界面準位層上に単結晶あるいは多結晶Si層（以下、Si層と記す）とを少なくとも有する制御手段と、該制御手段をはさんで設けられたキヤリアの送受手段とを少なくとも有し、前記界面準位層は前記Si層が有するフエルミ・レベルを当該界面準位層のフエルミ・レベルにピンニングせしめて成る。

前記界面準位層は前記III－V族の半導体層のエネルギー・ギヤツプに当たる位置に10^{13}／cm／eV以上の界面準位を持つのが良い。又その厚さは30Å以下であることが好ましい。

このような界面準位層は、III－V族の半導体とSiの格子定数の不整合、Siの成長時、あるいは被着時の高温プロセスによるストイキオメトリのずれ、空気や水にさらすこと、あるいはSiの成長，被着時に成長，被着容器中残存する酸素により形成されるIII－V族の半導体とSiの界面に生ずるIII－V族の半導体あるいはSiの酸化物（自然酸化膜）等の絶縁物、界面に残存する微量な金属による汚染等により容易に導入することができる。また、このような界面準位層はより積極的には、プラズマ酸化法や陽極酸化法等の手段で形成することも出来る。

Si層としては縮退したものを用いるのが通例であるが、その条件はたとえばダブリユ・ショツクレー〔W. Shockley〕“エレクトロン・アンド・ホールズ・イン・セミコンダクター〔Electrons and Holes in Semiconductors〕” デイー・フアン・ノストランド・プリンストン・エヌ・ジエー〔D. Fan Nostrand. Princeton. N. J.〕，1950等に知られているものを用いれば良い。半導体の縮退条件は現実には不純物濃度によつて制御する。その条件を例示すれば第1表の如きである。

第　1　表

	Si
n導電型	4.2以上
p導電型	1.5以上

（単位×$10^{20}cm^{-3}$，室温）

（前記文献により、縮退条件をn導電型に対しては、$E_f - E_c \geqq kT$，p導電型に対しては$E_v - E_f \geqq kT$として計算した。但し、E_fは半導体のフエルミレベル、E_cは伝導帯端のエネルギー、E_vは価電子帯端のエネルギー、kはボルツマン定数、Tは絶対温度である。）

Si層の厚さは、少なくとも50Å以上であればよく、必要に応じて、50～5000Åの範囲を選択する。

更に具体的半導体装置の構成として次の2つの型が考えられる。

(1) Si層は、そのエネルギー・バンドギヤツプの大きさがIII－V族の半導体層の少数キヤリアの存在する界面におけるエネルギーバンドの端とSi層の多数キヤリアの存在するエネルギーバンドの端との差よりも大きく、III－V族の半導体層と同一の導電性を有し、ゲートとソースあるいはドレインの間の半導体層の導電性はIII－V族の半導体層の導電性とは逆となす。この構成によれば、反転層の形成が容易で、大電

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流を流すことを可能とする。

(2)Si層は、そのエネルギー・バンドギャップの大きさがIII－V族の半導体層の多数キャリアの存在する界面におけるエネルギーバンドの端とSi層の多数キャリアの存在するエネルギーバンドの端との差よりも大きく、III－V族の半導体層と逆の導電性を有し、ゲートとソースあるいはドレインとの間の半導体層の導電性はIII－V族の半導体層の導電性と同一となす。この構成によれば、薄積層の形成が容易で、大電流を流すことを可能とする。

以下、各々について説明する。

(1) 第1の型

本発明による縮退したSi層／界面準位層／III－V族半導体の三層構造を持つ電界効果トランジスタの第1の型のものの断面を第2図(a)に示す。この三層構造のバンド構造を第2図(b)に示す。9は、半絶縁性半導体基板、10はn型半導体層、11はIII－V族のp型半導体層、12は界面準位層、13は縮退したp型Si層（ゲート）、14はソース電極、15はドレイン電極である。9は、必ずしも半絶縁性半導体基板に限らず、11と同じp型導電性を有する半導体基板であってもよい。縮退したSi13がゲートをなしており、界面準位層12の厚さは30Å以下、界面準位の密度は10^{12}／cm／eV以上である。また、縮退したSi層13とIII－V族の半導体11との間には、$E_g \geqq V_{t1}$ の関係がある。ここで、E_g は縮退したSi層13のエネルギーバンドギャップであり、V_{t1}は、縮退したSi層13の価電子帯端E_{v0}とIII－V族の半導体11の伝導帯端E_nとのエネルギー差である。

Siのエネルギーギャップは、室温で1.1eVであることが知られており、また、III－V族半導体の場合、その半導体のエネルギーギャップE_g'のおよそ2／3だけ、伝導帯端から離れた位置に界面のフェルミレベルがあることは周知の事実である。すなわち、$V_{t1}=\frac{2}{3}E_g'$ である。したがって、

$$E_g \geqq \frac{2}{3}E_g'$$

なる関係を満たすIII－V族半導体は、上記III－V族半導体11に適用できる。例えば、GaAsのエネルギーギャップはE_g'＝1.4eVであり、上式を満足する。

縮退したSi層13は第2図(b)に示すように直接界面準位層12と接触しており、かつ、正孔濃度が$10^{20}cm^{-3}$以上と高いので、界面準位への正孔の充放電時間は縮退したSiからのものが最も短い。その理由は、以下に述べる通りである。

縮退したSi層からの界面準位への電子の充放電時間τ_nは、式(1)，(2)と類似の形式に表現できて、

$$\tau_n=\frac{D_t\cdot\Delta\phi_{n0}}{v_{t1}\cdot N\cdot T_t} \quad \cdots(3)$$

$$T_t=\exp\left[-d_1\cdot\phi_1^{1/2}\left(\frac{m_1}{m_0}\right)^{1/2}-d_2\cdot\phi_2^{1/2}\left(\frac{m_2}{m_0}\right)^{1/2}\right] \quad \cdots(4)$$

$$d_1=\sqrt{2\varepsilon_1\left(\phi_1+\frac{kT}{q}\ell_n(N/N_{v1})\right)/qN\times10^8} \quad \cdots(5)$$

となる。但し、

D_t ：界面準位層12の界面準位密度（cm^{-2}／eV）

$\Delta\phi_{n0}$：電子の充放電に伴う界面準位のフェルミレベルϕ_{n0}の移動量（eV）

V_{t1}：縮退したSi層13中の自由正孔の速度（cm／sec）

N ：縮退したSi層13中の自由正孔の濃度（cm^{-3}）

T_t ：縮退したSi層13中に生ずる空乏層17及び、界面準位層12をトンネルする確率。（但し、ここでも簡単のため矩形のポテンシャル障壁をトンネルすると仮定した。）

d_1 ：空乏層17の厚さ（Å）

ϕ_1 ：正孔がトンネルする空乏層17による障壁の高さ（eV）

m_1 ：縮退したSi層13中の正孔の有効質量（g）

m_0 ：真空中の電子の質量（g）

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d_2 ：界面準化層１２の厚さ（Å）

ϕ_2 ：正孔がトンネルする界面準位層１２による障壁の高さ（ｅＶ）

m_2 ：界面準位層１２中の正孔の有効質量（ｇ）

ε_1 ：縮退したＳｉ層１３の誘電率（Ｆ／ｃｍ）

ｋ　：ボルツマン定数（eng／Ｋ）

ｑ　：電子の電荷（ｃ）

Ｔ　：絶対温度（Ｋ）

N_{v1}：縮退したＳｉ層１３の価電子帯の有効状態密度（cm^{-3}）

である。

Ｄ．$\Delta\phi_{s1} \fallingdotseq 10^{12} cm^{-2}$，$v_{th} \fallingdotseq 10^{7}$ ｃｍ／ｓｅｃ，$\phi_1 \fallingdotseq 0.45$ ｅＶ，$m_1 \fallingdotseq 0.2 m_0$，$d_2 \fallingdotseq 10$ Å，$\phi_2 \fallingdotseq 1$ ｅＶ，$m_2 \fallingdotseq 0.2 m_0$，$\varepsilon_1 = 11.9 \varepsilon_0$（$\varepsilon_0$ は真空の誘電率：0.885×10^{-13} Ｆ／ｃｍ），Ｔ＝３００Ｋ，$N_{v1} \fallingdotseq 10^{19} cm^{-3}$と仮定すれば、縮退したＳｉ層１３の正孔濃度を$N = 10^{20} cm^{-3}$とおくと、

$d_1 = 26$ Å

$\tau_n = 200$ ｐｓ

となる。したがつて、半導体層１１からの充放電時間 τ_r（＝１０ｎｓｃｅ～１０ｍｓｃｅ）に比べ、τ_n は、十分短い。

したがつて、縮退したＳｉ層１３と界面準位とは準熱平衡状態を達成し、界面準位のフエルミレベル ϕ_{fs} は、縮退したＳｉ層のフエルミレベル ϕ_n に固定される。このため、ゲートに正電圧を印加すると、表面電位 ϕ_s がそれに伴い変動する。

一方、縮退したＳｉ層１３とⅢ－Ⅴ族の半導体１１との間には、$E_g \geqq V_{bi}$ の関係があるので、Ⅲ－Ⅴ族の半導体１１の伝導帯の電子にとつてゲート側にバリアが存在することになる。

以上述べたように、本発明によるＦＥＴのゲート構造は、表面電位 ϕ_s をゲート電圧とともに変動させることができ、しかも伝導帯の電子にとつてゲート側の界面にバリアが存在する。そのため、容易に電子の反転層１６を界面に形成することができ、このようなＦＥＴは大電流を流せて高速である。

以上の説明では、Ⅲ－Ⅴ族の半導体及び縮退したＳｉ層としてｐ型のものを一例として挙げたが、ｎ型の半導体のものでも全く同じように界面に正孔の反転層を形成することができる。

（２）第２の型

本発明による縮退したＳｉ層／界面準位層／Ⅲ－Ⅴ族半導体の三層構造をもつ電界効果トランジスタの第２の型のものの断面を第３図（ａ）に示す。この三層構造のバンド構造を第３図（ｂ）に示す。４０は、半絶縁性半導体基板、４１は高濃度ｎ型半導体層、４２はⅢ－Ⅴ族のｎ型半導体層、４３は界面準位層、４４は縮退したｐ型Ｓｉ層（ゲート）、４５はソース電極、４６はドレイン電極である。４０は、必ずしも半絶縁性半導体基板に限らず、４２と反対のｐ型導電性を有する半導体基板であつてもよい。縮退したＳｉ層４４がゲートをなしており、界面準位層４３の厚さは３０Å以下、界面準位の密度は10^{12}／ｃｍ／ｅＶ以上である。また、縮退したＳｉ層４４とⅢ－Ⅴ族半導体４２との間には、$E_g \geqq V_{bi}$ の関係がある。ここで、E_g は縮退したＳｉ層４４のエネルギー・バンドギヤツプであり、V_{bi} は縮退したＳｉ層４４の価電子帯端 E_{vs} とⅢ－Ⅴ族の半導体４２の伝導帯端 E_c とのエネルギー差である。

ここで、前述の第１の型の構成で説明したように、$E_g \geqq \frac{2}{3} E_g'$ なるエネルギーギヤツプ E_g' を有するⅢ－Ⅴ族半導体は、上記Ⅲ－Ⅴ族半導体４２に適用できることは言うまでもない。

縮退したＳｉ層４４は、第３図（ｂ）に示すように直接界面準位層４３と接触しており、かつ正孔濃度が$10^{20} cm^{-3}$以上と高いので界面準位への正孔の充放電時間は縮退したＳｉ層からのものが最も短い。その理由は、第１の型の構成で説明したのでここでは省略する。

したがつて、縮退したＳｉ層４４と界面準位とは準熱平衡状態を達成し、界面準位のフエルミレベル ϕ_{fs} は、縮退したＳｉ層のフエルミレベル ϕ_n に固定される。このため、ゲートに正電圧 V_g を印加すると、表面電位 ϕ_s がそれに伴い変

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動する。

一方、縮退したＳｉ層４４とⅢ－Ⅴ族半導体４２との間には、$E_{g} \geqq V_{bi}$の関係があるので、Ⅲ－Ⅴ族半導体４２の伝導帯の電子にとつてゲート側にバリアが存在することになる。

以上述べてきたように、本発明によるＦＥＴのゲート構造では、表面電位ϕ_{s}をゲート電圧V_{g}とともに変動させることができ、しかも伝導帯の電子にとつてゲート側の界面にバリアが存在する。そのため、容易に電子の蓄積層４７を界面に形成することができ、このようなＦＥＴは大電流を流せて高速である。

以上の説明では、Ⅲ－Ⅴ族半導体４２としてｎ型のものを、縮退したＳｉ層４４としてｐ型のものを一例として挙げたが、Ⅲ－Ⅴ族半導体４２としてｐ型，縮退したＳｉ層４４としてｎ型のものでも全く同じように界面に正孔の蓄積層を形成することができる。

以上、述べてきたゲート構成は、$\tau_{n} \gg \tau_{p}$となるように、Ⅲ－Ⅴ族半導体と単結晶あるいは多結晶Ｓｉの組み合わせで説明してきた。しかし、本発明のゲート構造は、より一般的に、構成の説明で述べてきた一定の条件を満足できるあらゆる半導体の組み合わせで構成できる一般的なゲート構造であることを付言しておく（但し、ゲート電極となる半導体は、多結晶であつても単結晶であつてもよい）。

〔発明の実施例〕

実施例１

第４図（ａ）～（ｄ）に主要工程を示す。

第４図（ａ）：半絶縁性GaAs基板５０上に、$^{28}Si^{+}$の選択イオン打込み法によつてｎ層５１とｎ$^{+}$層５２を形成し、その後SiO_{2}膜５３を表面に被着した状態で高温熱処理を行い活性化した。$^{28}Si^{+}$の打込み条件は、ｎ層５１については打込みエネルギ７５ｋｅＶ，ドーズ量３×$10^{12}cm^{-2}$であり、ｎ$^{+}$層５２については打込みエネルギ１５０ｋｅＶ，ドーズ量１×$10^{13}cm^{-2}$である。通常ｎ層５１の不純物濃度は、所望する素子特性に応じて10^{16}～$10^{18}cm^{-3}$の範囲で選ぶ。SiO_{2}膜５３の厚さは2000Åであり、CVD（Chemical Vapor Deposition）法で被着した。高温熱処理は、８００℃，２０分間、H_{2}雰囲気中で行つた。

第４図（ｂ）：SiO_{2}膜５３を除去後、プラズマＣＶＤ法により、ホウ素と不純物としてドーピングしたＳｉ膜５５を被着し、続いてスパツタ法によりＷ膜５６を被着した。その後、ホトレジストによるパターンニング後、Ｗ膜５６及びＳｉ膜５５をCF_{4}とO_{2}の混合ガスによるドライエツチングで加工し、ゲート電極を形成した。ここで、Ｓｉ膜５５の膜厚は3000Å、Ｗ膜５６の膜厚は1000Åである。Ｗ膜５６を被着し、Ｓｉ膜５５の膜厚を3000Åとしたのは、ゲート抵抗の低減を目的とするものであり、必ずしも必要でなく、Ｓｉ膜５５の膜厚はゲート電極としての役割を果たすために最低５０Åあればよい。

また、SiO_{2}膜５３除去からＳｉ膜５５被着までの間に通常の工程では、ｎ型５１の表面を空気中あるいは水中の酸素にさらすことが普通である。このためｎ層５１表面に自然酸化膜が１０Å程度形成される。このため、ｎ層５１とＳｉ膜５５との界面には、界面準位層５４が形成される。また、Ｓｉ膜５５とGaAsとの格子定数の不整合によつて、より一層界面準位は導入されやすくなる。

本実施例によるＳｉ膜５５は、基板温度200℃，$B_{2}H_{6}$とSiH_{4}の流量比４対１００，高周波電力１００Ｗ、圧力1Torrで形成した。この基板温度によれば、形成されたＳｉ膜５５はアモルファス状態である。また、この$B_{2}H_{6}$とSiH_{4}の流量比によれば、後の高温熱処理工程で、活性化するホウ素は$10^{20}cm^{-3}$以上となる。

第４図（ｃ）：SiO_{2}膜５７を2000Å被着した後、再び、８００℃，２０分間の熱処理をH_{2}雰囲気中で行つた。この高温熱処理により、Ｓｉ膜５５は多結晶へ転換し、膜中に含有されたホウ素は電気的に活性化する。この結果、Ｓｉ膜５５はｐ型の導電性を有する多結晶膜となり、電気的に活性なホウ素濃度は$10^{20}cm^{-3}$となつた。

ｐ型の導電性を実現するために、本実施例では

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ホウ素を添加したが、ガリウムやアルミニウムを添加してもp型導電性を実現できることは言うまでもない。ホウ素は、p－CVD法で、ガリウムやアルミニウムはMBE法で添加するのが容易である。

第4図（d）：ホトレジストにより電極パターンを形成した後、パターン部のSiO_2膜を除去し、AuGe／Ni／Auを全面に被着し、不要な金属をホトレジストとともに取り除き（リフトオフ法）、ソース・ドレイン電極58，59を形成した。金属の被着膜厚は、AuGe600Å，Ni100Å，Au800Åである。その後400℃，3分間，H_2雰囲気中で熱処理を行つた。この時、n⁺層52へのオーミツク接触が実現する。

本実施例によれば、多結晶p－Si層とn－GaAs層の界面に電子の蓄積層がゲート電圧0.8V以上で容易に形成され、従来のMISFETに比べ、同じゲート電圧で3倍以上の電流を流すことができ、相互コンダクタンスgm＝400mS／mmが得られた。また、界面準位の充放電時間が短く、相互コンダクタンスや容量の周波数依存性が小さくなるという改善効果も同時に確認された。

本実施例では、縮退したSi層がp型，Ⅲ－Ⅴ族半導体がn型，ゲートとソースあるいはドレインの間の半導体もn型であつたが、これらの導電性が逆の場合、すなわち縮退したSi層がn型であり、Ⅲ－Ⅴ族半導体及びゲートとソースあるいはドレインの間の半導体が共にp型である場合にも、同様に正孔の蓄積層が形成されて、大電流を流すことができた。

また、本実施例では、ゲート電極として縮退したSi層を用いたが、この他に以下に列挙する半導体を用いることもできる。すなわち、
BP，AlP，AlAs，AlSb，GaN，GaP，GaAs，GaSb，InN，InP，$Al_xIn_{1-x}P$（$0<x<1$），$Al_xGa_{1-x}As$（$0<x<1$），$Al_xIn_{1-x}As$（$0.2\leqq x<1$），$Al_xGa_{1-x}Sb$（$0<x<1$），$Al_xIn_{1-x}Sb$（$0.4\leqq x<1$），$Ga_xIn_{1-x}P$（$0<x<1$），$Ga_xIn_{1-x}As$（$0.4\leqq x<1$），GaP_xAs_{1-x}（$0<x<1$），$GaAs_xSb_{1-x}$（$0.8\leqq x<1$），InP_xAs_{1-x}（$0.4\leqq x<1$），$Al_xGa_{1-x}P_yAs_{1-y}$（$0<x<1$，$0<y<1$），$Al_xGa_{1-x}As_ySb_{1-y}$（$0<x<1$，$0<y<1$），$Ga_xIn_{1-x}P_yAs_{1-y}$（$0.4\leqq x<1$，$0.4\leqq y<1$），$Ga_xIn_{1-x}As_ySb_{1-y}$（$0.7\leqq x<1$，$0.7\leqq y<1$），$(Al_xGa_{1-x})_yIn_{1-y}P$（$0<x<1$，$0<y<1$），$(Al_xGa_{1-x})_yIn_{1-y}As$（$0<x<1$，$0.5<y<1$），$(Al_xGa_{1-x})_yIn_{1-y}Sb$

（$0.5\leqq x<1$かつ$0.5\leqq y<1$あるいは、
$0.4\leqq x<0.5$かつ$0.6\leqq y<1$あるいは、
$0.3\leqq x<0.4$かつ$0.7\leqq y<1$あるいは、
$0.2\leqq x<0.3$かつ$0.8\leqq y<1$）

$In(P_xAs_{1-x})_ySb_{1-y}$（$0.6\leqq x<1$）

からひとつを選ぶことができる。これらの半導体のエネルギーギヤツプE_gは、GaAs（エネルギーギヤツプ$E_g'=1.4eV$）に対して、前述の関係式$E_g\geqq\frac{2}{3}E_g'$を満足する。

また、本実施例ではⅢ－Ⅴ族半導体としてGaAsを用いたが、この他に、InP，AlGaAs，InGaAs，InGaAsP等のⅢ－Ⅴ族半導体を用いることもできる。特に、InPに対しては、このエネルギーギヤツプが1.3eVのため、前に列挙した半導体をゲート電極にすべて適用できる。また、Ⅲ－Ⅴ族半導体に限らず、Si，Geを用いても良いことは言うまでもない。

実施例2

第5図（a）～（d）に主要工程を示す。本実施例では、ゲート電極として用いるSi膜をマスクとして、自己整合的にn⁺層を形成する工程に特徴がある。

第5図（a）：半絶縁性GaAs基板50に、$^{28}Si^+$の選択イオン打込み法によつてn層51を形成し、その後SiO_2膜53を表面に被着した状態で、高温熱処理を行い活性化した。$^{28}Si^+$の打込み条件は、打込みエネルギー75keV，ドーズ量$3\times10^{13}cm^{-2}$である。SiO_2膜53の厚さは2000Åであり、CVD法で被着した。高温熱処理は、800℃，20分間，H_2雰囲気中で行つた。

第4図（b）：SiO_2膜53を除去後、プラ

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ズマCVD法により、ホウ素を不純物としてドーピングしたSi膜55を被着し、続いてスパッタ法によりW膜56を被着した。その後、ホトレジストによるパターンニング後、W膜56及びSi膜55をCF$_4$とO$_2$の混合ガスによるドライエッチングで加工し、ゲート電極を形成した。ここで、Si膜55の膜厚は3000Å，W膜56の膜厚は1000Åとしたが、この二層膜を合わせた膜厚は、後のn$^+$層形成に用いる$^{29}Si^+$のイオン打込みエネルギーに応じて決定される。また、Si膜55の膜厚はゲート電極としての役割を果たすために最低50Åあればよい。

実施例1で説明したように、n層51の表面には自然酸化膜が10Å程度形成される。このため、n層51とSi膜55との界面には、界面準位層54が形成される。また、Si膜55の製造条件は、実施例1と同様である。

第5図（c）：Si膜55とW膜56の二層膜をマスクとし、$^{29}Si^+$を選択的にイオン打込みし、ゲートに隣接する領域をn$^+$－GaAs層52とソース・ドレインのn$^+$層52へのオーミック接触がとれる。

本実施例のゲート構造は実施例1と同一であるが、特に本実施例によれば、ゲートとソース及びドレインの間のn$^+$層を$1\times10^{13}cm^{-2}$の高ドーズで形成したために、寄生抵抗が低下し、従来のMISFETに比べ4倍以上の電流を流すことができた。また、相互コンダクタンス540mS／mmが得られた。

本実施例においても、実施例1に列挙した如き、半導体をゲート電極として用いることは可能である。

ゲート電極にIII－V族半導体を用いる場合、実施例1の如く、n$^+$層52をゲートに自己整合して設けることをしない素子では、第4図（c）の高温熱処理工程は省略できる。なぜなら、たとえばAlGaAsをゲート電極として用いる場合には、通常MOCVD法やMBE法によつて成長することが可能であり、これらの方法によれば膜はすでに成長時に、多結晶あるいは単結晶となるからである。

しかし、本実施例の如く、n$^+$層52をゲートに自己整合して設ける素子においては、その高温熱処理工程を省略できない（第5図（c））。すなわち、ゲート電極にAlGaAs等のIII－V族半導体を用いた場合、ゲート電極をp型の導電性を持たせるためにドーピングする不純物は、GaAsに対してアクセプタとなりうる。そのため、第5図（c）の工程に含まれるn$^+$層を活性化する高温熱処理により、ゲート電極中の不純物がGaAs側に拡散し、n－GaAs層51のキャリア濃度を変動させる要因となる。このような、変動は、一般にキャリア濃度制御を精密に実現することが重要な高集積回路の製作には致命的である。

ところが、本実施例の如く、Si膜をゲート電極に用いた場合、Si膜にドーピングされる不純物はホウ素やガリウム等のIII族の元素であり、GaAs中においては、アクセプタあるいはドナーとならない。このため、高温熱処理を施してもキャリア濃度の変動要因とならない。したがつて、本実施例の如くIII－V族の半導体基板を用い、高温

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熱処理工程を終る素子においては、特にＳｉ膜が有用である。

実施例３

第６図（ａ）～（ｄ）に主要工程を示す。

第６図（ａ）：半絶縁性GaAs基板２０上に、$^{28}Si^{+}$の選択イオン打込み法によつてｎ層２１とｎ$^{+}$層２２を形成し、その後SiO_2膜２３を表面に被着した状態で高温熱処理（８００℃，２０分）を行い活性化した。$^{28}Si^{+}$の打込み条件は、ｎ層２１については打込みエネルギー７５ｋｅＶ，ドーズ量$3\times10^{12}cm^{-2}$であり、ｎ$^{+}$層２２については打込みエネルギー１５０ｋｅＶ，ドーズ量$1\times10^{13}cm^{-2}$である。SiO_2膜２３の厚さは2000Åであり、ＣＶＤ（Chemical Vapor Deposition）法で被着した。高温熱処理は、800℃，２０分間，H_2雰囲気中で行つた。

第６図（ｂ）：高温熱処理に用いたSiO_2膜２３のゲート部をエツチングにより除去した。その後空気中に長時間さらし、GaAsの自然酸化膜による界面準位層２４を１０Åの厚さでつくつた後、除去した領域だけにMOCVD（Metal Organic Chemical Vapor Deposition）法により縮退したｐ－$Ga_{0.7}Al_{0.3}As$層２５を選択エピタキシヤル成長した。ｐ－$Ga_{0.7}Al_{0.3}As$層２５の不純物濃度は縮退の条件を満足させるために10^{20}~$10^{21}cm^{-3}$台とした。この時用いた不純物はＺｎであり、MOCVD法による成長温度を、６８０℃としたのでｐ－$Ga_{0.7}Al_{0.3}As$層２５直下のｎ層はＺｎによる拡散で完全に補償されてｐ－GaAs層２６となる。また、ゲート部のSiO_2膜を除去したのち、空気中に長時間さらしてGaAs基板表面に、GaAs中のバンドギヤツプ中に準位を高密度に持つGaAsの自然酸化膜を１０Å程度つくり、その上にｐ－$Ga_{0.7}Al_{0.3}As$層を成長させたのでｐ－$Ga_{0.7}Al_{0.3}As$層２５とｐ－GaAs層２６の界面には高密度の界面準位層２４が形成されている。

第６図（ｃ）：AuGe／Ｎｉ／Ａｕをこの順に６００Å，１００Å，８００Åと被着し、イオンミリング法によりゲート部以外の領域の金属を除去し、ゲート電極２７を形成した。

第６図（ｄ）：ホトレジストにより電極パターンを形成した後、パターン部のSiO_2膜を除去しAuGe／Ｎｉ／Ａｕを全面に被着し、不要な金属をホトレジストとともに取り除き（リフトオフ法）ソース・ドレイン電極２８，２９を形成した。金属の被着膜厚は、AuGe６００Å，Ｎｉ１００Å，Ａｕ８００Åである。その後４００℃，３分間，H_2雰囲気中で熱処理を行つた。この時、ｎ$^{+}$層２２へのオーミツク接触とともに、ｐ－$Ga_{0.7}Al_{0.3}As$層２５へのオーミツク接触が実現する。

本実施例によれば、ｐ－$Ga_{0.7}Al_{0.3}As$層とｐ－GaAs層の界面に電子の反転層がゲート電圧が０．８Ｖ以上で容易に形成され、従来のMISFETに比べ、同じゲート電圧で３倍以上の電流を流すことができ相互コンダクタンスg_m＝４００ｍＳ／㎜が得られた。また、界面準位の充放電時間が短く、相互コンダクタンスや容量の周波数依存が小さくなるという改善効果も同時に確認された。

本実施例では、ゲート電極となる$Ga_{0.7}Al_{0.3}As$層もGaAs層も共にｐ型であり、ゲートとソースあるいはドレインの間の半導体はｎ型であつたが、これらの導電性が逆の場合、すなわちゲート電極となる$Ga_{0.7}Al_{0.3}As$層もGaAs層も共にｎ型であり、ゲートとソースあるいはドレインの間の半導体はｐ型である場合にも同様に正孔の反転層が形成されて、大電流を流すことができた。

また、本実施例では、ゲート電極として縮退した$Ga_{0.7}Al_{0.3}As$層を用いたが、この他にＳｉ層、あるいは、実施例１で列挙した半導体を用いることも可能である。また、基板に用いたGaAsの代りに、ＩｎＰ，ＡｌGaAs，InGaAs，InGaAsP等のⅢ－Ⅴ族半導体あるいはＳｉ，Ｇｅを用いることができることは言うまでもない。

〔発明の効果〕

以上述べたように、本発明によれば縮退した半導体と半導体の界面に反転層あるいは蓄積層が容易に形成され、従来のMISFETに比べ、同じゲート電圧で３倍以上の電流を流すことができ、ＦＥＴを高速化できる効果がある。

図面の簡単な説明

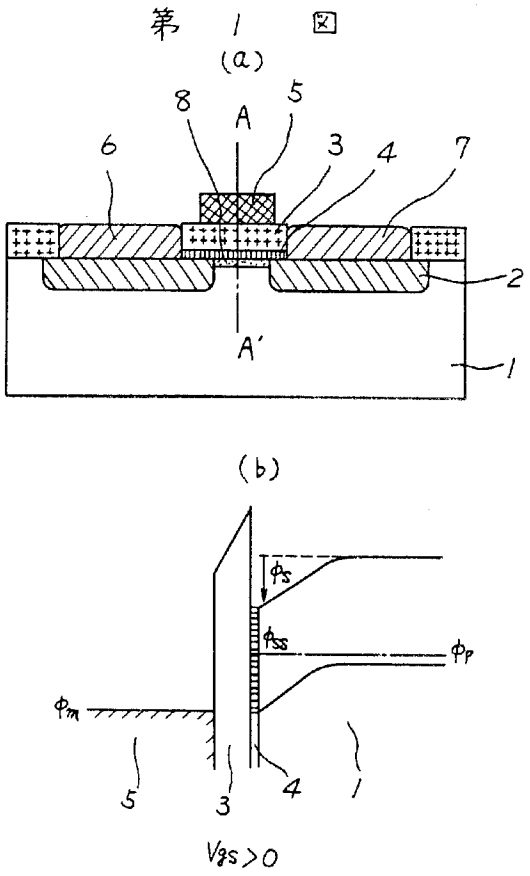
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第１図（ａ）はMISFETの構造断面図、同図（ｂ）はＡ－Ａ′線断面のバンド構造図である。第２図（ａ）は本発明によるＦＥＴの構造断面図、同図（ｂ）はＢ－Ｂ′線断面のバンド構造図である。第３図（ａ）は本発明によるＦＥＴの構造断面図、同図（ｂ）はＢ－Ｂ′線断面のバンド構造図である。第４図～第６図は、本発明によるＦＥＴの一実施例としての製造プロセスに従う装置断面図である。

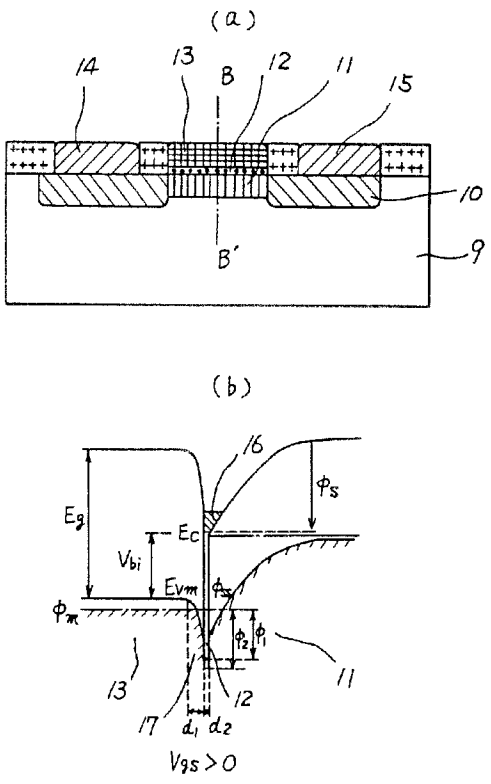
９…半絶縁性半導体基板、１０…ｎ型半導体層、１１…ｐ型Ⅲ－Ⅴ族半導体層、１２…界面準位層、１３…細退したｐ型Ｓｉ層（ゲート）、１４…ソース電極、１５…ドレイン電極、４０…半絶縁性半導体基板、４１…高濃度ｎ型半導体層、４２…ｎ型Ⅲ－Ⅴ族半導体層、４３…界面準位層、４４…細退したｐ型Ｓｉ層（ゲート）、４５…ソース電極、４６…ドレイン電極。

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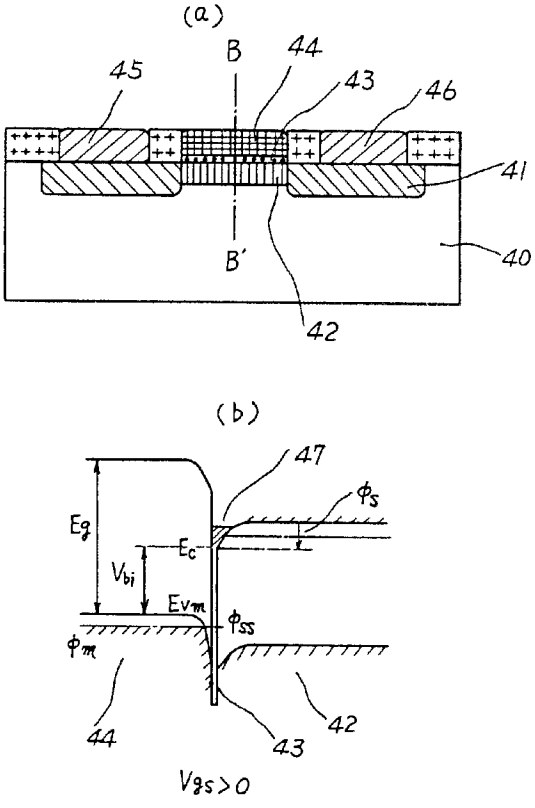
第１図



第２図

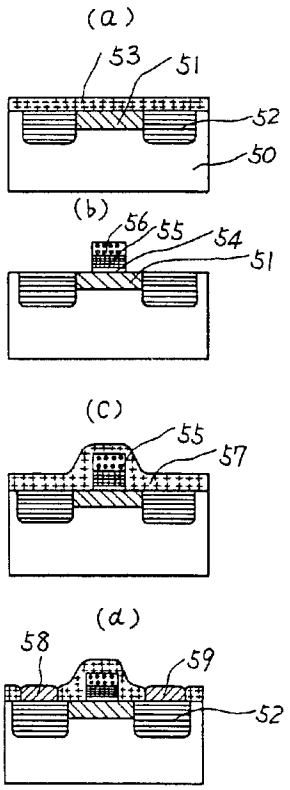


第３図

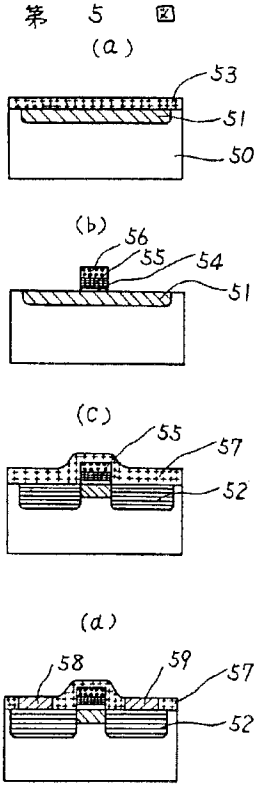


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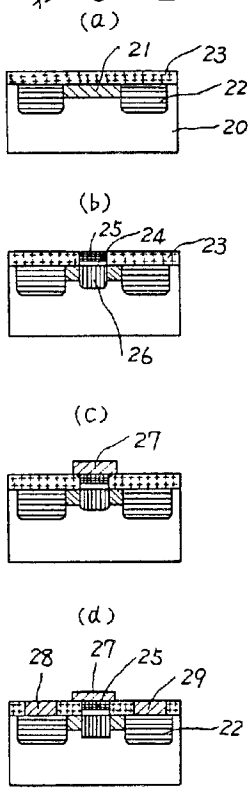
第 4 図



第 5 図



第 6 図



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第1頁の続き

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JPS6261363A SEMICONDUCTOR DEVICE

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SEMICONDUCTOR DEVICE

Abstract

PURPOSE:To obtain a high speed field effect transistor which can feed a large current by forming a 3-layer structure of a degenerate Si layer/boundary level layer/group III-V semiconductor, and pinning the Fermi level of the Si layer to that of the boundary level layer. CONSTITUTION:An N-type semiconductor layer 10, group III-V P-type semiconductor layer 11, a boundary level layer 12, a degenerate P-type Si layer (gate) 13, a source electrode 14, and a drain electrode 15 are formed on a semi- insulating semiconductor substrate 9. The thickness of the layer 12 is 30Angstrom or less, the density of the boundary level is 10<12>/cm<2>/eV or higher, and there is a relation of Eg>=Vbi between the layer 13 and the semiconductor 11. Eg is the energy band gap of the layer 13, and Vbi is the energy difference between the valence band end of the layer 13 and the conduction band end of the semiconductor 11. The layer 13 and the boundary level perform a quasi-thermal equilibrium state, and the Fermi level of the boundary level is secured to the Fermi level of the layer 13.

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DESCRIPTION JPS6261363

[0001]

[Field of Use of the Invention] The present invention relates to a high-speed electrodeposition effect transistor. [Background of the Invention] A cross-sectional view of a MISFET (Metal fi, nsu) ator Field E, ffcct Transistor) using a compound semiconductor substrate such as GaAs or InP is shown in Fig. 1 ('l). Here, 1 is a p-GaAs substrate, 2 is an n GaAs layer, 3 is an insulating film, 4 is an interface state layer, 5 is a gate electrode, 6 is a source electrode, and 7 is a drain electrode. The thickness of the insulating film 3 is usually between 1000 and 3000. Such an MJSFET is a device capable of performing an inversion type operation. That is, when the stopping voltage is applied to the gate electrode 5, the electron inversion layer 8 is formed at the interface between the insulating film 3 and the P-GaAs substrate 1. Since the inversion layer is used for the channel, the MISFET has a potential as a high speed device because it can draw a large current. However, in reality, as shown in the band structure diagram of FIG. 1 (b), at the interface between the insulating film 3 and the P GaAs substrate 1, the 10 ″ -1011 / cd / eV level is near the center of the semiconductor energy gap. It is known that there is a layer 4 with extremely high density of interface 1 (4) (hereinafter referred to as interface level layer 4) with a thickness of 10 to 30 people. Especially in compound semiconductors. It is extremely difficult to keep this value below LO "cx-'/ eV (for example, in GaA + s, oxygen atoms and metal atoms are exposed on the surface due to exposure to air or contamination with impurities. It is known that an interface state layer of 10 "aa-" / eV or more is generated only by attaching one layer.) Therefore, the conventional MIsFhi has the Fermi level ϕ 6. Has a strong tendency to be fixed to the Fermi level ϕ of the semiconductor, and even if a positive voltage is applied to the gate electrode, the surface potential ϕ 6 does not fluctuate and it is difficult to form the inversion layer. As described above, in the conventional MiSFET, it is difficult to use the inversion layer as a channel, and a large amount of current cannot be obtained. This is because there is a high-density interface state layer, and the Fermi level of the interface state tends to be fixed to the Fermi level of the

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semiconductor. Examples of MIS transistors as explained below can be found in, for example, solid-state electronics [5olid-8tate Electronics] vol, 17r pp751-759 (1974).

[Object of the Invention] An object of the present invention is to provide a high-speed field effect transistor capable of passing a large current. [Outline of the Invention] As described above, in the conventional MISFET, the Fermi level of the interface state tends to be fixed to the Fermi level of the semiconductor. This is physically the charge / discharge time of electrons from the semiconductor side to the interface state. This is because the quasi-thermal equilibrium state is established between the interface state and the semiconductor because it is shorter than the charging / discharging time from another region (for example, the gate metal). To describe more quantitatively, the charge / discharge time t of electrons from the semiconductor side to the interface state is, for example, in the range of 10n5ec-10m5ec when the semiconductor is n-GaAs, and more generally nl-V It is known that the charge / discharge time of the group compound semiconductors falls within the range of 10 n5ac to 10 m5ec. On the other hand, the charge / discharge time t of the charge P from the gate metal to the interface state is. となる。 However, D, the interface state density (cn-2 / eV) Aϕ1. = Is the Fermi level ϕ1. Movement of 1 t (eV) V @ k: velocity of free electrons in gate metal 5 (am / 5ee) N: concentration of free electrons in gate metal 5 (aII-J) T1: probability of tunneling through insulating film 3 (however, , For the sake of simplicity, it is assumed here that the rectangular potential barrier is 1-channel.) D: Insulation 1 (thickness of the island 3) ϕ: Height of the barrier due to the insulating film 3 through which electrons tunnel eV) m: Effective mass of electrons in the insulation 1 void 3 (g) mo: Electrons in vacuum Is the mass (g) of D, -Aϕs 6:10 ” ” ” (2m- “ gVtb in] 07cn / see, N * 10 ” ao-3, ϕ in 4eVrm / rr +. -: 0.2, d = I-1000A <up to 1 enumeration 1. 4 Ut, which is a typical value of a normal MIS structure.), T becomes 10 ″ 'sac, and τ becomes (τ). Therefore, the equilibrium state is established between the interface level and the conductor, and the Fermi level of the interface level is fixed to the Fermi level of the semiconductor. Therefore, as described above, in order to fix the Fermi level of the interface state to the Fermi level of the gate metal, the gate structure may be configured so that τ1 is controlled. The present invention realizes the above gate structure. Basically, it has the following configuration.

At least an interface level layer in the mv group semiconductor region having the first conductivity and a single crystal or polycrystalline Si layer (hereinafter referred to as Si layer) in the interface level layer-1. The interface level layer has at least a control unit and a carrier transmission / reception unit sandwiching the control unit, and the interface level layer pin the Fermi level of the Si layer to the Fermi level of the interface level layer. I will make it at least. It is preferable that the interface level layer has an interface level of 10 ″ / cd / eV or more at a position corresponding to the energy gap of the semiconductor layer of the group (1)-(4). The thickness is preferably 30 Å or less. Such an interface state layer has a mismatch in lattice constant between the semiconductor of the --- group and Si, deviation of stoichiometry due to a

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high temperature process during Si growth or deposition, exposure to air or water, Alternatively, the growth of Si, the growth during deposition, and the formation of oxygen in the deposition container by the oxygen remaining in the group ■-■ group ■-■ semiconductor or Si oxide (natural oxide film), etc. It can be easily introduced due to contamination by the insulating material and trace amount of metal remaining on the interface. Further, such an interface level layer can be more positively formed by means such as a plasma oxidation method or an anodic oxidation method. It is customary to use a degenerated Si layer, but the conditions are, for example, W Shockley [W, 5 hockley] "I Reftron and Holes in Semiconductor (Electron! 1 and Ho1es in Sem1conductors) ” , Dee 9 Juan Nostrand Princeton NJ (D, Fan No5trand, Pr1nceton, N, J,) +1950, etc. should be used. The degeneration condition of the semiconductor is actually controlled by the impurity concentration. An example of the condition is shown in Table 1. Table 1 Sinf! , Electric type 4.2 or higher P conductive type], 5 or higher (unit x t o) ■ -3. Room temperature) (According to the above-mentioned literature, the degeneracy condition was calculated as E, −EC ≧ kT for n conductivity type, and Ev−E, ≧ kT for p conductivity type. However, E is the Fermi level of the semiconductor, and Ec is the energy at the conduction band edge. Ev is the valence band edge energy, k is the Boltzmann constant, and T is the absolute temperature.) The thickness of the Si layer may be at least 50 Å or more, and the range of 50 to 5000 is selected as necessary.

The following two types are conceivable as more specific semiconductor device configurations. (1) The Si layer has an energy bandgap whose size is between the edge of the energy band at the interface where minority carriers are present in the semiconductor layer of the group and the edge of the energy band where majority carriers are present in the Si layer. It is larger than the difference, and has the same conductivity as that of the ■ -v semiconductor layer, and the conductivity of the semiconductor layer between the gate and the source or the drain is opposite to that of the ■-■ semiconductor layer. Eggplant According to this structure, the inversion layer can be easily formed and a large current can be passed. (2) In the Si layer, the size of the energy band gap is between the band of the energy band at the interface where majority carriers exist in the semiconductor layer of the group --- and the edge of the energy band where majority carriers exist in the Si layer. The conductivity is larger than the difference, and has the opposite conductivity to that of the group V semiconductor layer, and the conductivity of the semiconductor layer between the gate and the source or the drain is the same as that of the group S semiconductor layer. . According to the configuration of 1 :, the formation of the storage layer is easy and a large current can be passed. Each will be described below. (1) First type FIG. 2 (a) shows a cross section of a first type of field effect transistor having a three-layer structure of degenerated Si layer / metaphysical layer / m = v semiconductor according to the present invention. The band structure of this two-layer structure shown in FIG. 2 is shown in FIG. 9 is a semi-insulating semiconductor substrate, 10 is an n-type semiconductor layer, 11 is an m-v group p-type semiconductor layer, 12 is an interface state layer, 13 is a degenerate p-type Si layer (gate), and 14 is a source. Electrodes and 15 are drain bars. 9 is not necessarily a semi-

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insulating semiconductor substrate, but may be a semiconductor substrate having the same P-type thick electrical property as 1]. The degenerated Si 13 serves as a gate, and the thickness of the interface state layer 12 is 30 Å or less and the density of 5 interface states is], and O″ / ad / AV or less-hi. Further, there is a relationship of E, ≧ Vbl between the degenerated Si layer 13 and the semiconductor 11 of the group ■-■. Here, El is the energy bandgap of the degenerate S iMl 3, and ■, l are the valence band edge Ev of the degenerated Si layer 13 and the conduction band edge E of the mv semiconductor J1. It is the energy difference. The energy gap of Si is known to be 1.1 cV at room temperature, and in the case of In-V group semiconductors, about 2/3 of the energy gap E9 'of the semiconductor is separated from the conduction band edge. It is a well-known fact that there is a Fermi 1 novel on the interface at a different position, that is, Vbc = Eg '.

Therefore, the In-v group semiconductor satisfying the relationship of E and ≧ −E1 ′ can be applied to the above-mentioned 1-— group semiconductor 1.1. For example, the energy gap of GaAs is E, '= 1.4 eV, which satisfies the above equation. The degenerated Si layer] -3 is directly in contact with the interface level layer 12 as shown in FIG. 2 (b), and the hole concentration is as high as 10 "+ a ++-'or -L. At the time of charging / discharging holes to the level, IIn is the shortest from degenerate Si. The reason is that the charge / discharge time τ of electrons from the Si layer degenerate to 5 to the interface state can be expressed in a form similar to the equations (1) and (2), as described below. .. However, D ,: Interface state density of the interface state layer 12 (dll-"/ eV) A ϕ 8. Fermi level of interface level ϕ 8 due to charge / discharge of two electrons. + T (eV) V z k: Velocity of free holes in degenerated Si layer 13 (cs / 5ee) N: Concentration of free holes in degenerated Si layer 13 („ “3) Tt: Degeneracy Probability of tunneling the depletion layer 17 generated in the Si layer 13 and the interface state layer 12. (However, for the sake of simplicity, it is assumed here that a rectangular potential barrier is tunneled.) Dl: thickness of depletion layer 17) ϕ 1: height of barrier due to depletion layer 17 in which holes tunnel eV) ml: effective mass of holes in degenerated Si layer 13 (g) mo: in vacuum Mass of electron (g) d2 = thickness of interface enhancement layer 12) ϕ 2: height of barrier eV) m due to interface level layer 12 through which holes tunnel, m: of holes in interface coating layer 12 Effective mass (FC) ε : Dielectric constant (F / m) k of degenerated S i Ml 3 k: Boltzmann constant (eng / K) q: Electric charge (c) T: Absolute temperature (K) Nyl: Degenerated It is the effective state density (1-3) of the valence band of the Si layer 13. D, Δ ϕ as "F 10" (! 1-"+ Vtb" "10" 1 / 5ec) ϕ 1 * 0.45eV + m 0.2m in hand, 10 people in d2. ϕ 2-: 1 eV, m ,: 0.2 mo, E, = 11.9 f. (Fo is the dielectric constant of vacuum: 0,885X IQ- "F / m). Assuming T "300 K-Nvx f'10" low ", the hole concentration of the degenerated Si layer 13 is set as N = l 02oam- '. d, = 26 people τ , = 200 ps. Therefore, τ 1 is sufficiently shorter than the charge / discharge time v of the semiconductor layer 11 (= 10 n5ca to 10 m5ce).

Therefore, the degenerated S1 layers 1; 3 and the interface state achieve a montothermal

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equilibrium state, and the Fermi level ϕ9. Is fixed to the Fermi level ϕ of the degenerated Si layer. Therefore, when a positive voltage is applied to the gate, the surface potential ϕ changes accordingly. On the other hand, the degenerate Si layer 13 and the semiconductor 11 of the group 1 to 4 have a relation of E, ≧ 3. A barrier exists on the gate side for electrons in the conduction band of the semiconductor group 11-. As described above, in the gate structure of the FET according to the present invention, the surface potential ϕ can be varied with the goo voltage to the voltage, and further, a barrier exists at the interface on the gate side for electrons in the conduction band. Therefore, the electron inversion layer 16 can be easily formed at the interface, and such an FET can flow a large current at a high speed. In the above description, the group III-V semiconductor and the degenerate Si layer are used as P layers. I took the type as an example. A hole inversion layer can be formed at the interface in the same manner even with an n-type semiconductor. (2) Second type FIG. 3 (a) shows a cross section of a second type of field effect transistor having a three-layer structure of a degenerated Si layer / physical plane layer / group III-group semiconductor according to the present invention. The band structure of the three-layer structure shown in FIG. 3 is shown in FIG. 3B, 40 is a semi-insulating semiconductor substrate, 41 is a high-concentration n-type semiconductor layer, 42 is a ■ -V group n-type semiconductor layer, 43 is an interface state layer, 44 is a degenerated p-type Si layer (gate), 45 is a source electrode, and 4G is a drain electrode. 40 is not necessarily a semi-insulating semiconductor substrate, and may be a semiconductor substrate having a P-type trench property opposite to 42. The degenerated 31 layer 44 forms a gate, the thickness of the interface state layer 43 is 30 Å or less, and the density of the interface state is 10 ″ / ffl / eV or more. In addition, the degenerate 31 layer 44 and the {circle around (1)}-■ group semiconductor 42 have a relationship of E, ≧ 1. Here, E is the energy bandgap of the degenerate 31 layer 44, and ■ □ is the valence 1 of the degenerate 31 layer 44, and the conduction band edge E of the − and III-V semiconductor 42 4: F. This is the energy difference from the end E1. Here, as described in the configuration of the first type described above, the −V group semiconductor having the energy gaps E and J such that E and ≧ −E1 ′ is applicable to the III-V group semiconductor 42 described above. Needless to say. Since the degenerated 31 layer 44 is in direct contact with the interface level layer 43 as shown in FIG. 3 (b) and the hole concentration is as high as 10 ″ cs ° 1 or more, holes to the interface level are increased. The shortest charging / discharging time is from the degenerated Si layer. The reason for this is omitted here because it has been described in the first type configuration.

Therefore, the degenerated S1 layer 44 and the interface state achieve a heat-increasing equilibrium state, and the Fermi level ϕ1. Is fixed to the Fermi level ϕ of the degenerated Si layer. Therefore, a positive voltage is applied to the gate. Is applied, the surface potential ϕ fluctuates with the passing. On the other hand, since the degenerate Si layer 44 and the In-V group semiconductor 42 have a relationship of E and ≧ Vkl, a barrier exists on the gate side for electrons in the conduction band of the III-V group semiconductor 42. Will be done. As described above, in the gate structure of the FET according to the present invention, the surface potential

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ϕ can be changed along with the gate voltage v1 ° , and a barrier exists for the electrons in the conduction band at the interface on the gate side. Therefore, the FET can be easily formed on the interface of the electron storage layer 47, and such an FET can flow a large current and is high speed. In the following description, the n-type semiconductor is used as the 1 --- group semiconductor 42 and the n-type one is used as the degenerated Si layer 44 as an example. Even if an n-type layer 44 is used, a 9M layer for holes can be formed at the interface in the same manner. The gate structure described above has been described by combining {circle over ()} and [tau], and the combination of (1) -V group semiconductor and single crystal or polycrystalline Si. However, it should be added that the gate structure of the present invention is more generally a general gate structure that can be composed of any combination of semiconductors that can satisfy the certain conditions described in the description of the structure (however, Gate t !! The polar semiconductor may be polycrystalline or single crystal). [Embodiment of the Invention] Embodiment 1 Main steps are shown in FIGS. 4 (a) to 4 (d). Fig. 4 (a) A state in which the 1st layer 51 and the n0 layer 52 are formed on the semi-insulating GaAs substrate 5o by the selective ion implantation method of Z @ Si +, and then the S x Ox I grain 53 is deposited on the surface. Implantation conditions of e "S x" activated by high-temperature heat treatment are: implantation energy 75 θ V for 1 layer 51, dose 13X10 "as- ', implantation energy 150 keV, dose I for n0 layer 52. The impurity concentration of the 0 normal n-layer 51, which is X 1013aW- ', is selected in the range of 10 "to lO" cx- "according to the desired device characteristics, and the thickness of the 5iO7 film 53 is 2000 persons. (Chemical Vapor Deposition) method. The high temperature heat treatment was performed at 800 ° C. for 20 minutes in an H 2 atmosphere.

FIG. 4 (b): After removing the S x O 2 film 53, a Si film 55 doped with boron and impurities as a plasma CVD method is deposited, and then a W film 56 is deposited by a sputtering method 6 After that, After patterning with a photoresist, the W film 56 and the S1 film 55 were processed by dry etching with a mixed gas of CF4 and 0 □ to form a gate electrode. Here, the film thickness of the Si film 55 is 3000 and the film thickness of the W film 56 is 1000. The reason why the W film 56 is deposited and the film thickness of the Si film 55 is set to 3000 is for the purpose of reducing the gate resistance and is not always necessary. You need at least 50 people to play a role. In addition, in the usual process from the removal of the Sin / film 53 to the deposition of the Si film 55, the surface of the n-type 51 is usually exposed to oxygen in the air or water. Therefore, a natural oxide film is formed on the surface of the 9th layer 51 to the extent of [O]. Therefore, the interface level layer 54 is formed at the interface between the first layer 51 and the Si film 55. Further, due to the mismatch of lattice constants between the Si film 55 and GaAs, the interface state is more easily introduced. The Si film 55 according to the present embodiment has a substrate temperature of 200 ° C. B, H, and Sin flow rate ratio 4 to 100. The high frequency power was 100 W and the pressure was L Torr. According to this substrate temperature, the formed Si film 55 is in an amorphous state. Further, according to the flow rate ratio of B2H and Sin, the boron to be activated becomes lQ "an-" or more in the subsequent high temperature heat treatment step. FIG. 4 (c): After depositing 2000 people of SiO and film 57, heat

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treatment at 800 ° C. for 20 minutes is performed again for H. I went in the atmosphere. By this high temperature heat treatment, the Si film 55 is converted into polycrystal, and the boron contained in the film is electrically activated. As a result, the Si film 55 became a polycrystalline film having P-type conductivity, and the concentration of electrically active boron was 1020 -3. Although boron was added in this embodiment to achieve n-type conductivity, it goes without saying that p-type trench conductivity can also be achieved by adding gallium or aluminum. It is easy to add boron by the p-CVD method and gallium or aluminum by the MBE method. Fig. 4 (d): After forming a 7-pole pattern with photo-diss 1-, the SiO □ film of the pattern part is removed, AuGe / Ni / Au is deposited on the entire surface, and unnecessary metal is removed. It was removed together with the photoresist (lift-off method) to form source / drain electrodes 58.59.

The metal deposition thickness is 600 for AuGe, 100 for Ni, and 800 for Au. Then 400 ° C. Heat treatment was performed in (2) atmosphere for 3 minutes. At this time, ohmic contact with the n0 layer 52 appears. According to this embodiment, an electron accumulation layer is easily formed at the interface between the polycrystalline p-S i layer and the n-GaAs layer at a Goo 1-voltage of 0.8 V or more, and has the same gate voltage as that of the conventional MISFET. Then; a current of 3 times or more can be passed, and mutual conductance g m = 400 m S / m is nine, and interface 1 v! It was also confirmed at the same time that the charging / discharging time at 18:11) 1 was short and the frequency dependence of the mutual conductance and the capacity became small. In this example, the degenerated S1 layer was n-type, the mv group semiconductor was n-type, and the semiconductor between the gate and the source or the drain was also n-type. Even when the formed Si layer is of the rl type and the m-v group semiconductor and the semiconductor between the gate and the source or the drain are both of the n type, an alternate stack of holes is similarly formed to flow a large current. I was able to do it. Further, in this example, the degenerated Si layer is used as the gate electrode, but other semiconductors listed below may be used. すなわち。 ＢＰ、ＡＱＰ、ＡＲＡｓ、ＡＱＳｂ、ＧａＮ、ＧａＰ。
ＧａＡｓ、ＧａＳｂ、ＩｎＮｖＩｎＰ＋へＱ、Ｉｎ、－、Ｐ（０＜Ｘ＜１）、ＡＱ、Ｇａｌ－、
Ａｓ（０＜ｘ＜１）。ＡＱ、Ｉｎ、－、
Ａｓ（０，２≦ｘ＜１）＊ＡＱ－Ｇａｌ－．５ｂ（０＜ｘ＜１）、
ＡＱ－Ｉｎｔ－５ｂ（０，４≦ｘ＜１）。Ｇａ、Ｉｎ、－、Ｐ（０＜Ｘ＜１）ｒＧａＪｎ、－、
Ａｓ（０，４≦ｘ＜１）、ＧａＰ、Ａｓ、－、（０＜ｘ＜１）、ＧａＡｓ、Ｓｂ、－。
（０，８≦ｘ＜１）＝ＩｎＰ－Ａｓｌ－＋＋（０－４≦ｘ＜１）。ＡＱ、Ｇａ、－、
ＰｙＡｓｔ－ｙ（０＜ｘ＜１．Ｏ＜ｙ＜１）ＩＡＱ、Ｇａｔ－、
＋ＡｓｙＳｂｔ－ｙ（０＜ｘ＜１．Ｏ＜ｙ＜１）。Ｇａ、
Ｉｎｔ－ｗＰｙＡｓｔ－ｙ（０－４≦ｘ＜１、０、４≦ｙ＜１）。Ｇａ、Ｉｎ、－、Ａｓ、
Ｓｂ、－、（０、７≦ｘ＜１、０、７≦ｙ＜ｉ）ｖ（ＡＱ、Ｇａｌ－、
）ｙＩｎｘ－ｙＰ（０＜ｘ＜１、Ｏ＜ｙ＜１）。(A QmGal-, +) yIJ-yAS (0 <x <1, 0, 5 <y <IL (AQ, Ga,-)), In5-ysb (0,5 x <1 or-) 0 5 ≦ y <1 or 0.4 ≦ x <0, 5 and 0.6 ≦ y <1 or 0.3 ≦ x <0, 4 and 0.7 ≦ y <1 or 0.2 ≦ x <0, 3 and 0.8 ≦ y 1) In (P, As,), 5b1-, (0, 6 ≦ x 1), one can be selected.

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The energy gap EII of these semiconductors satisfies the above-mentioned relational expression E1 ≧ −E, l with respect to GaAs (energy gap E, '= 1.4 eV). Further, in the present embodiment, GaAs was used as the ■-■ group semiconductor, but in addition to this, it is also possible to use a ■ -V group semi-specialized body such as InP, AQ GaAs, InGaAsw ■ mouth GaAsP. In particular, for InP, this energy gap is 1.3 eV, so that all the semiconductors listed above are suitable for the gate electrode. Moreover, it is not limited to the ■-■ group semiconductors, and it is possible to use Sly (ro). Example 2 Main steps are shown in FIGS. 5 (a) to 5 (d). This embodiment is characterized by the step of forming the n3 layer in a self-aligned manner by using the Si film used as the gate 1'a electrode as a mask. 6 Fig. 5 (a) Two-hand insulating GaAst treatment 50, 21 SL The 0 layer 51 is formed by the selective ion implantation method of b. Then, with the SiO 2 film 5; 3 deposited on the surface, high temperature heat treatment was performed to activate it. The implantation conditions for 211 Sili are an implantation energy of 75 keV and a dose amount of 3 X 10 "am-". The thickness of S i O2 [53 was 2000 people and was deposited by the CVD method. The high temperature heat treatment was performed at 800 ° C. for 20 minutes in an H 2 atmosphere. FIG. 4 (b): After the SiO □ film 53 is removed, Sx pancreas 55 doped with boron as an impurity by plasma (, ▪ D method) is deposited, and then by a sputtering method, a W film 56 '! Lid deposited. Then, after patterning with Photolith 1-, the W film 56 and the Si film 55 were processed by dry etching with a mixed gas of CF4 and 02 to form a Goo 1-electrode. Here, the film thickness of the Sl film 55 was set to 3000 and the film thickness of the W film 56 was set to 1000, but the combined film thickness of these two layers is the ion of the Si film to be used later in n “layer formation”. It is determined according to the driving energy. Further, the film thickness of the Si film 55 may be at least 50 in order to function as a gate electrode. As described in the first embodiment, a natural oxide film is formed on the surface of the 0 layer 51- at a 1-0 boundary level. Therefore, the interface level layer 54 is formed at the interface between the 0 layer 51 and the Si film 55. The manufacturing conditions for 5il1955 are the same as in Example 1. FIG. 5 (c): Using the two-layer film of the Si film 55 and the W film 56 as a mask, "the Si film was selectively ion-implanted, and the region adjacent to the gate 1 was set to n" '-GiAsM52.

At this time, two layers! Under the itt of I9 is rrh, and for 24S 3. + Is not driven in. After that, the n ″ layer 52 was activated again by high-temperature treatment with 200 (one person's S10 film 57-coated spasticity). 2 ″ 'S ;, under the conditions of “implantation”, the implantation energy is 150 keV, the dose is tlX1013clQ-2, and the high temperature heat treatment is 800 ° C. It was carried out in an H1 atmosphere for 20 minutes. By this high temperature heat treatment, the Si film 55 is converted into polycrystal and the boron contained in the pancreas is electrically activated. As a result, the Si film 55 became a polycrystalline film having p-type conductivity, and the concentration of electrically active boron was 10 ″ l ″ ″. FIG. 5 (d): An electrical contact pattern by a photoresist. After forming the pattern, the S10 i film 57 of the pattern part is removed, and AuGe / N i / A 1. J was deposited on the entire surface and

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unnecessary metal was removed together with the photoresist (riff] -off method) to form source / drain electrodes 58.59. If the metal deposition v is thick, it is AuGc600A, Ni 100 people, Au 800 people. After that, 400 ° C. Heat treatment was performed in an H □ atmosphere for 3 minutes. このとき。 An ohmic contact is made to the n0 layer 52 of the source / drain. Although the gate structure of this embodiment is the same as that of the first embodiment, in particular, according to this embodiment, the n ″ ″ layer between the gate, the source and the train is formed with a high dose of IX 1013am− ″ , The parasitic resistance was reduced, and a current that was four times or more that of the conventional MISFET could flow. Also, mutual conductance of 540 ms / rm was obtained. Also in this embodiment, it is possible to use a semiconductor as the gate electrode as listed in the first embodiment. In the case where the group 1- to 6 group semiconductor is used for the gate electrode, the high temperature heat treatment step of FIG. 4 (e) can be omitted in the device in which the n "layer 52 is not provided in self alignment with the gate as in the first embodiment. Because, for example, when the person αGa ^ 3 is used as the gate fa pole. This is because it is usually possible to grow by the MOCVD method or the MBE method, and according to these methods, the film is already polycrystal or single crystal at the time of growth. However, in the device in which the n0 layer 52 is self-aligned with the gate as in the present embodiment, the high temperature heat treatment step cannot be omitted (FIG. 5 (c)), that is, AQ'GaAs or the like is used for the gate electrode. When using a group (1)-(6) group semiconductor, the impurities that are doped to make the gate electrode have P-type conductivity can serve as acceptors for GaAs.

Therefore, due to the high temperature heat treatment for activating the n0 layer included in the step of FIG. 5C, the impurities in the gate tI & the electrode diffuse to the GaAs side, which causes the carrier concentration of the n-GaAs layer 51 to change. .. Such a variation is fatal to the manufacture of a highly integrated circuit in which it is generally important to realize the gear rear concentration control at M '/ l. However, when the Si film is used for the gate (-electrode) as in this example, the impurities doped to 5 illi are group III elements such as boron and gallium, and do not serve as acceptors or donors in GaAs. Therefore, even if the high temperature heat treatment is performed, it does not cause a change in the key X7 rear concentration. Therefore, in the element using the <tO-V group semiconductor substrate as in the present embodiment and finishing the high temperature heat treatment step, the Si film is particularly It is useful. Example 3 Main steps are shown in FIGS. 6 (a) to 6 (d). FIG. 6 (a): A state in which n) fl 21 and n ” 122 are formed on the semi-absolute GaAs substrate 20 by the selective ion implantation method of “ Si ”, and then SiOz lli 23 is adhered to the surface. High temperature heat treatment (800 ° C. The activation conditions of 2 # Si + activated by performing 20 minutes) are as follows: n layer 21 has an implant energy of 75 ksV, dose amount 3 X i O "am-2, and n0 layer 22 has an implant energy of 150 keV. The dose filter 'XIQia,-, the thickness of the 5 in 2 film 23 is 2000 persons, and it was deposited by the CVD (Che + m1ca-i VaporDeposition) method. High temperature heat treatment is 800 ° C. It was carried out in a H2 atmosphere for 20 minutes. FIG. 6B: Sin used for the high temperature heat treatment, and the gate portion of the film 23 was removed by

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etching. After that, it was exposed to the air for a long time, and after forming the interface level layer 24 of a natural oxide film of GaAs with a thickness of 10 people, only the removed region was degenerated by MOCVD (Metal Organicqhs +++ 1cal cal Vapor Deposition) method. The impurity concentration of m-p-Ga5.tAQo and 3AF4 layer 25 obtained by selective epitaxial growth of the -1AQ6 and 3As layer 25 was set to three 1.0 "to 1021Qll" in order to satisfy the degeneracy condition. The impurity used at this time is Zn. Since the growth temperature by the MOCVD method was set to 680 ° C., P Gas, tA n 6 and the n layer directly under the As layer 25 were completely compensated by diffusion by Zn to become the p-GAAs layer 26. After removing the SiO film, it was exposed to the air for a long time and a natural oxide film of GaAs with a high density level in the band gap of GaAs was formed on the surface of the GaAs substrate for about 10 people. Since p-Ga, ..., AQll, and 3As layers were grown, PGa ++, iAQ, 0.

A high-density interface state layer 24 is formed at the interface between the As layer 25 and the p-GaAs7fl2F3. FIG. 6 (c): AuGa / Nj / Au was deposited in this order on 600 people, 100 people, and 800 people, and the metal in the region other than the gate portion was removed by the ion milling method to form the gate electrode 27. No. 614 (d): After forming the electrode pattern with the photoresist, the SiO □ film of the pattern part is removed, AuGe / Ni / Au is deposited on the entire surface, and unnecessary metal is removed together with the photoresist (Riff 1 to off Method) The deposited film thickness of the metal on which the source / drain electrodes 28.29 are formed is 600 AuGa and 100 Ni. There are 800 Au. After that, 400 ° C for 3 minutes. The heat treatment was performed with IL2 '+' lJ # width. At this time, along with ohmic contact to the fourth layer 22, P Ga11. .. AQ „ Ohmic contact to the As layer 25 is realized. According to this example, p Ga. , 7 A Q l, 3 An electron inversion layer is easily formed at the interface between the As layer and the P-GaAs layer with a gate voltage of 0.8 v or more, and is three times or more the same gate voltage as the conventional MISFET. An electric current could be passed, and a transconductance g- =400 m510n was obtained. At the same time, the improvement effect that the charge / discharge time of the interface state is short and the frequency dependence of the mutual conductance and the capacity is reduced was also confirmed. In this embodiment, both the Ga, tAQO,) As layer and the GaAs layer, which are gate electrodes, are D-type, and the semiconductor between the gate and the source or drain is D-type. In the opposite case, that is, when the Ga, 1, A, AQ, 3As layers and GaAs layers that are gate electrodes are both D-type and the semiconductor between the gate and the source or train is P-type, A hole inversion layer was formed and a large current could be passed. Also, in this example, the degenerate Gag, 7AQg, and 3 layers of 9 layers were used as the gate electrode, but in addition to this, it is also possible to use the Si layer or the semiconductors enumerated in Example J-. .. It goes without saying that, instead of GaAs used for the substrate, III-V group semiconductors such as InP, AQ GaAs, InGaAsP InGaAsP or Si, Ge can be used. As described above, according to the present invention, the inversion layer or the storage layer is easily formed at the interface between the degenerated semiconductor and the semiconductor i ´ : It is possible to flow a current more than twice as much, and there is an effect that the FE "I" can be

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speeded up.

[0002]
Brief description of the drawings

[0003]

FIG. 1 (a) is a structural cross-sectional view of a MISFET, and FIG. 1 (b) is a band cross-sectional structural view along the line A-A '.

FIG. 2 (a) is a structural sectional view of the FET according to the present invention, and FIG. 2 (b) is a band structure diagram of a B-B ″ sectional view. FIG. 3 (a) is a structural sectional view of the FET according to the present invention. FIG. 3B is a band structure diagram of a B-B ″ cross section. 4 to 6 are sectional views of the device according to the manufacturing process as one embodiment of the FET according to the present invention. 9 ... Semi-insulating semiconductor substrate, 1o ... n-type semiconductor layer, 11 ... p-type group ■-■ group semiconductor layer, 12 ... interface level layer. 13 ... Degenerate P-type Si layer (gate), 14 ... Source electrode, 15 ... Drain electrode, 40 ... Semi-insulating semiconductor substrate, 41 ... High-concentration n-type semiconductor layer, 42 ... n-type m-v group semiconductor layer, 43 ... interface level layer, 44 ... degenerate p-type Si layer (gate), 45 ... source number / ll (shi] vys>. Early 2 mouths (a-) (b) and 9s> O 3rd country (α) (b) V O> 0 4th mouth 4th! 5 mouth (d)

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1.
A control means having at least an interface level layer on the electrically conductive III-V group first semiconductor region and a second semiconductor layer made of single crystal or polycrystalline Si on the interface level layer; At least a carrier transmission / reception means sandwiching a control means is provided, and the interface level layer causes the Fermi level of the second semiconductor layer to be pinned to the Fermi level of the interface level layer. A semiconductor device characterized by being formed. 2. The interface level layer has an interface level of 10 ^ 1 ^ 2 / cm ^ 2 / eV or more at a position corresponding to an energy gap of the first semiconductor layer. The semiconductor device according to the paragraph. 3. The semiconductor device according to claim 1 or 2, wherein the interface level layer has a thickness of 30 Å or less. 4. The semiconductor device according to any one of claims 1 to 3, wherein the second semiconductor layer is made of a degenerate semiconductor. 5. The size of the energy band gap between the edge of the energy band at the interface where minority carriers exist in the first semiconductor layer and the edge of the energy band where majority carriers exist in the second semiconductor layer The conductivity of the semiconductor layer is larger than that of the first semiconductor layer, and has the same conductivity as that of the first semiconductor layer. The semiconductor device according to any one of claims 1 to 4, characterized in that: 6. The size of the energy band gap between the edge of the energy band at the interface where majority carriers exist in the first semiconductor layer and the edge of the energy band where majority carriers exist in the second semiconductor layer The conductivity of the semiconductor layer between the control means and the carrier transfer means is the same as that of the fifth term. The semiconductor device according to any one of claims 1 to 4, which is characterized.

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
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Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8164	FILED BY	Sarah Zizzo
PATENT CENTER #	60039933	FILING DATE	04/14/2020
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

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PARK_81.pdf	8608683B1C5EEB1ABCFEDAAF8347C763A37D9859056B9C0B1788EE1FBCE339054E11DBE8026C3E4C1DB98EEFAC076E574E8D2042088906E136CE9C38DB8949D6
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(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	
Attorney Docket Number	3771-0003-DC13

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	Examiner Name	
	Attorney Docket Number	3771-0003-DC13

	2	20140117465	A1	2014-05-01	Huang, et al.	

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	1	ARCHIBONG, et al., On the Structure of A12O3 and Photoelectron Spectra of A12O2 and A12O3; J. Phys. Chem.A 1999, 103, pp. 1109-1114.	
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	Attorney Docket Number	3771-0003-DC13

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	7	IPR2020-01182; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 23, 2020; 139 pp.	
	8	IPR2020-01182; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 7,084,423; June 24, 2020; 76 pp.	
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	16	IPR2020-01206; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,905,691; June 29, 2020; 76 pp.	

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	Examiner Name	
	Attorney Docket Number	3771-0003-DC13

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	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	
	Attorney Docket Number	3771-0003-DC13

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GF Exhibit 1126 - 2053/2248

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(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	
Attorney Docket Number	3771-0003-DC13

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That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-07-15
Name/Print	Tarek N. Fahmi	Registration Number	41402

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EFS ID:	40014304
Application Number:	16847878
International Application Number:	
Confirmation Number:	8164
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Jennifer Stewart
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC13
Receipt Date:	15-JUL-2020
Filing Date:	14-APR-2020
Time Stamp:	20:07:19
Application Type:	Utility under 35 USC 111(a)

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Warnings:					
Information:					

16	Non Patent Literature	IPR2020-01205_Petition.pdf	1273626 ac66c9655ad5f16b67b4bd699151e2edf7ab95ae	no	63
Warnings:					
Information:					
17	Non Patent Literature	IPR2020-01206_Dec.pdf	2994366 2e0b0c33c5cfd07db570de3c3975c37756d42f4a	no	164
Warnings:					
Information:					
18	Non Patent Literature	IPR2020-01206_Petition.pdf	1075189 bb3c13428dff58f80bf53c0ff4e1328162d86ce1	no	76
Warnings:					
Information:					
19	Non Patent Literature	IPR2020-01207_Dec.pdf	2822842 f33c074f0bf06a00e666ebeb7a0ae4a0edebc09e	no	146
Warnings:					
Information:					
20	Non Patent Literature	IPR2020-01207_Petition.pdf	1313963 96171196afd0ddd1db91190637101ad3a6c232fb	no	66
Warnings:					
Information:					
21	Non Patent Literature	IPR2020-01241_Dec.pdf	2626941 300287c7706cfb1e4a8e652471326695729 0df6f	no	165
Warnings:					
Information:					
22	Non Patent Literature	IPR2020-01241_Petition.pdf	1824376 74d367ef671ae938f07edd05b54ad8cbaf3a97fa	no	84
Warnings:					
Information:					

23	Non Patent Literature	IPR2020-01264_Dec.pdf	2493153 5a52055504ef7ba68f12adbc67cdc1ff9c554aa5	no	194
Warnings:					
Information:					
24	Non Patent Literature	IPR2020-01264_Petition.pdf	2121917 d8d412e76e2264a30e6f5512cf393b6db6dbba75	no	83
Warnings:					
Information:					
25	Non Patent Literature	IPR2020-01279_Dec.pdf	3085537 c9f95ef31474dc4918dba3adfe8742f79d77a472	no	182
Warnings:					
Information:					
26	Non Patent Literature	IPR2020-01279_Petition.pdf	2053661 123227cb45dc58c38997033290bf53342530f730	no	84
Warnings:					
Information:					
27	Non Patent Literature	IPR2020-01282_Dec.pdf	3720361 46b04411e7422e222b0ad6e643215383d39d200d	no	217
Warnings:					
Information:					
28	Non Patent Literature	IPR2020-01282_Petition.pdf	860880 84e289b4c42e76b3f51c16b08ed63c73425399f7	no	85
Warnings:					
Information:					
29	Non Patent Literature	Lang.pdf	1293754 3a408331a9a75c0d98ceff217647ed412bdd68f7	no	9
Warnings:					
Information:					

30	Non Patent Literature	Rohatgi.pdf	1047833 6af7099070e885b67e81572e402fc5f1f5b4894f	no	7
Warnings:					
Information:					
31	Non Patent Literature	Sakurai.pdf	2667974 b0d3a2342e2ef1be5bca929af0dba20d697bf37c	no	11
Warnings:					
Information:					
32	Non Patent Literature	Simmons.pdf	2094070 f3690af22c63aff9809162579c1a02a1f75a7c4c	no	11
Warnings:					
Information:					
33	Non Patent Literature	Stesmans.pdf	632891 fd6ad3e11bd5622c7e24b8a76f6bd8d0dba1f183	no	3
Warnings:					
Information:					
34	Non Patent Literature	Szydlo.pdf	774312 61f735cec595e161c8f61b98637680dd27f5252b	no	3
Warnings:					
Information:					
35	Non Patent Literature	Zheng.pdf	655606 bc806d41f8239788eb919eb1af70f8a9e218d74d	no	5
Warnings:					
Information:					
			Total Files Size (in bytes):	63418220	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Daniel E. Grupp

Application No.: 16/847,878
Filed: 04/14/2020

Examiner: Not Yet Assigned
Art Unit: 2815

Docket No.: 3771-0003-DC13

Customer No.: 27571

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g. copies of U.S. patents and U.S. published patent applications that need not be included). This IDS and IDS Citation Form are being submitted before the mailing of a First Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account No. 50-5798.

Respectfully submitted,

Date: July 15, 2020

/Tarek N. Fahmi/
Tarek N. Fahmi, Reg. No. 41,402

ASCENDA LAW GROUP, PC
2150 N First Street, Suite 420
San Jose, CA 95131
(866) 877-4883

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/847,878	04/14/2020	Daniel E. Grupp	3771-0003-DC13

CONFIRMATION NO. 8164

27571
Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

PUBLICATION NOTICE

OC00000018848014

Title:METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Publication No.US-2020-0243662-A1
Publication Date:07/30/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

GF Exhibit 1126 - 2065/2248

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC13

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040129087	A1	2004-07-08	ROWE; et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

GF Exhibit 1126 - 2066/2248

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16847878
	Filing Date	2020-04-14
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	HARRISON, MONICA D
	Attorney Docket Number	3771-0003-DC13

	1	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

GF Exhibit 1126 - 2067/2248

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC13

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-08-27
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

GF Exhibit 1126 - 2069/2248

Electronic Acknowledgement Receipt

EFS ID:	40404737
Application Number:	16847878
International Application Number:	
Confirmation Number:	8164
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC13
Receipt Date:	27-AUG-2020
Filing Date:	14-APR-2020
Time Stamp:	17:22:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3771-0003-DC13_IDS.pdf	1034322 f10fbb4c42d24fd817426c935486f040eeecd410	no	4

Warnings:

Information:	
Total Files Size (in bytes):	1034322

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/847,878	04/14/2020	Daniel E. Grupp	3771-0003-DC13	8164

27571 7590 09/23/2020

Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

EXAMINER
HARRISON, MONICA D

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
09/23/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@ascendalaw.com
tarek.fahmi@ascendalaw.com

GF Exhibit 1126 - 2072/2248

Office Action Summary	Application No. 16/847,878	Applicant(s) Grupp et al.	
	Examiner MONICA D HARRISON	Art Unit 2815	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 4/14/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-12 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-12 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 4/14/2020 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 4/14/2020,6/17/2020,7/15/2020,8/27/2020.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Priority

1. This application discloses and claims only subject matter disclosed in prior application no 16/506,022, filed 7/9/19, and names the inventor or at least one joint inventor named in the prior application. Accordingly, this application may constitute a continuation or division. Should applicant desire to claim the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120, 37 CFR 1.78, and MPEP § 211 *et seq.*

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for

applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention.

2. Regarding claims 1 and 7, lines 1-2 state "a metal electrical contact to said semiconductor substrate". This statement is unclear. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim(s) 1-12 is/are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Schroen et al (3,983,264).

3. Regarding claim 1, Schroen et al discloses an electrical junction (Figure 2), comprising: a semiconductor substrate (Figure 2, reference 11); a metal electrical contact (Figure 2, reference 16) to said semiconductor substrate (Figure 2, reference 11); and a passivating dielectric tunnel barrier layer (Figure 2, reference 15) between said semiconductor substrate (Figure 2, reference 11) and said metal electrical contact (Figure 2, reference 16), said semiconductor substrate (Figure 2, reference 11) being electrically connected to said

metal electrical contact (Figure 2, reference 16) through said passivating dielectric tunnel barrier layer (Figure 2, reference 15), wherein said passivating dielectric tunnel barrier layer (Figure 2, reference 15)is configured to increase a height of a Schottky barrier for electrons (column 1, lines 16-58) between the metal electrical contact (Figure 2, reference 16) and the semiconductor substrate (Figure 2, reference 11) from that which would exist at a contact junction between the metal electrical contact (Figure 2, reference 16) and the semiconductor substrate (Figure 2, reference 11) without the dielectric tunnel barrier layer (Figure 2, reference 15) disposed therebetween (column 1, lines 16-22).

4. Regarding claim 2, Schroen et al discloses wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si (Figure 2, reference 11; column 4, line 48; *silicon*).

5. Regarding claim 3, Schroen et al discloses wherein the metal electrical contact (Figure 2, reference 16) comprises a metal (column 5, lines 16-19; *aluminum*) having a work function near or substantially equal to a conduction band edge of the semiconductor (Figure 2, reference 11).

6. Regarding claim 4, Schroen et al discloses wherein the metal (Figure 2, reference 16) having a work function near or substantially equal to a conduction band edge of the

semiconductor (Figure 2, reference 11)comprises one of: aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn) (Figure 2, reference 16; lines 16-19; aluminum).

7. Regarding claim 5, Schroen et al discloses wherein the semiconductor substrate (Figure 2, reference 11) is doped p-type (column 4, lines 48-49) proximate to the electrical contact (Figure 2, reference 16).

8. Regarding claim 6, Schroen et al discloses wherein the semiconductor substrate (Figure 2, reference 11) is undoped (column 4, lines 48-49) proximate to the electrical contact (Figure 2, reference 16).

9. Regarding claim 7, Schroen et al discloses an electrical junction (Figure 2), comprising: a semiconductor substrate (Figure 2, reference 11); a metal electrical contact (Figure 2, reference 16) to said semiconductor substrate (Figure 2, reference 11); and a passivating dielectric tunnel barrier layer (Figure 2, reference 15) between said semiconductor substrate (Figure 2, reference 11) and said metal electrical contact (Figure 2, reference 16), said semiconductor substrate (Figure 2, reference 11) being electrically connected to said metal electrical contact (Figure 2, reference 16) through said passivating dielectric tunnel barrier layer (Figure 2, reference

15), wherein said passivating dielectric tunnel barrier layer (Figure 2, reference 15)is configured to increase a height of a Schottky barrier for holes (column 1, lines 16-58) between the metal electrical contact (Figure 2, reference 16) and the semiconductor substrate (Figure 2, reference 11) from that which would exist at a contact junction between the metal electrical contact (Figure 2, reference 16) and the semiconductor substrate (Figure 2, reference 11) without the dielectric tunnel barrier layer (Figure 2, reference 15) disposed therebetween (column 1, lines 16-22).

10. Regarding claim 8, Schroen et al discloses wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si (Figure 2, reference 11; column 4, line 48; silicon).

11. Regarding claim 9, Schroen et al discloses wherein the metal electrical contact (Figure 2, reference 16) comprises a metal (column 5, lines 16-19; aluminum) having a work function near or substantially equal to a valence band edge of the semiconductor (Figure 2, reference 11).

12. Regarding claim 10, Schroen et al discloses wherein the metal (Figure 2, reference 16) having a work function near or substantially equal to a valence band edge of the semiconductor (Figure 2, reference 11) comprises one of: platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu),

cobalt (Go), or palladium (Pd) (Figure 2, reference 16; column 3, lines 24-26; gold, molybdenum, tungsten and platinum).

13. Regarding claim 11, Schroen et al discloses wherein the semiconductor substrate (Figure 2, reference 11) is doped p-type (column 4, lines 48-49) proximate to the electrical contact (Figure 2, reference 16).

14. Regarding claim 12, Schroen et al discloses wherein the semiconductor substrate (Figure 2, reference 11) is undoped (column 4, lines 48-49) proximate to the electrical contact (Figure 2, reference 16).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759

F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved

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Claims 1-12 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-3 and 5-7 of U.S. Patent No. 10,388,748 B2 (Grupp et al). Although the claims at issue are not identical, they are not patentably distinct from each other because the claimed subject matter, of claims 1-12, of the instant application may be found in claims 1-3 and 5-7 of the patent.

15. Regarding claim 1, Grupp et al 748' discloses an electrical junction, comprising: a semiconductor substrate; a metal electrical contact to said semiconductor substrate; and a passivating dielectric tunnel barrier layer between said semiconductor substrate and said metal electrical contact, said semiconductor substrate being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer is configured to increase a height of a Schottky barrier for electrons between the metal electrical contact and the semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween (claim 1).

16. Regarding claim 2, Grupp et al 748’ discloses wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si (claim 3).

17. Regarding claim 3, Grupp et al 748’ discloses wherein the metal electrical contact comprises a metal having a work function near or substantially equal to a conduction band edge of the semiconductor (claim 2).

18. Regarding claim 4, Grupp et al 748’ discloses wherein the metal having a work function near or substantially equal to a conduction band edge of the semiconductor comprises one of: aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn) (claim 7).

19. Regarding claim 5, Grupp et al 748’ discloses wherein the semiconductor substrate is doped p-type proximate to the electrical contact (claim 6).

20. Regarding claim 6, Grupp et al 748’ discloses wherein the semiconductor substrate is undoped proximate to the electrical contact (claim 1).

21. Regarding claim 7, Grupp et al 748’ discloses An electrical junction, comprising: a semiconductor substrate; a metal electrical contact to said semiconductor substrate; and a

passivating dielectric tunnel barrier layer between said semiconductor substrate and said metal electrical contact, said semiconductor substrate being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer is configured to increase a height of a Schottky barrier for holes between the metal electrical contact and the semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween (claim 1).

22. Regarding claim 8, Grupp et al 748’ discloses wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si (claim 3).

23. Regarding claim 9, Grupp et al 748’ discloses wherein the metal electrical contact comprises a metal having a work function near or substantially equal to a valence band edge of the semiconductor (claim 2).

24. Regarding claim 10, Grupp et al 748’ discloses wherein the metal having a work function near or substantially equal to a valence band edge of the semiconductor comprises one of: platinum (Pt), gold (Au), tungsten (W), nickel (Ni),

molybdenum (Mo), copper (Cu), cobalt (Go), or palladium (Pd) (claim 2).

25. Regarding claim 11, Grupp et al 748' discloses wherein the semiconductor substrate is doped n-type proximate to the electrical contact (claim 5).

26. Regarding claim 12, Grupp et al 748' discloses wherein the semiconductor substrate is undoped proximate to the electrical contact (claim 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MONICA D HARRISON whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7-4:30pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MONICA D HARRISON/
Primary Examiner, Art Unit 2815

mdh
September 17, 2020

Notice of References Cited	Application/Control No. 16/847,878	Applicant(s)/Patent Under Reexamination Grupp et al.	
	Examiner MONICA D HARRISON	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-3983264-A	09-1976	Schroen; Walter H.	H01L21/28575	257/734
*	B	US-10388748-B2	08-2019	Grupp; Daniel E.	H01L29/7839	1/1
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GF Exhibit 1126 - 2086/2248

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L29/ 456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785	09/17/2020	MDH
H01L21/28,285,2853,28537	09/17/2020	MDH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
257	763	09/17/2020	MDH

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Search Notes		
Search Notes	**Date**	**Examiner**
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	09/17/2020	MDH
GRUPP ET AL .inv.	09/17/2020	MDH
ACORN TECHNOLOGIES .asn.	09/17/2020	MDH
IPR2020-01182 Reviewed Petition for Inter Partes Review of US. Patent No. 7,084,423 and Exhibits Ex.1001-Ex.1025	09/17/2020	MDH
IPR2020-01206 Reviewed Petition for Inter Partes Review of US. Patent No. 9,905,691 and Exhibits Ex.1001-Ex.1035	09/17/2020	MDH
PR2020-01279 Reviewed Petition for Inter Partes Review of US. Patent No. 9,905,691 and Exhibits Ex.1101-Ex.1150	09/17/2020	MDH

/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	

GF Exhibit 1126 - 2088/2248

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/17/2020								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								

GF Exhibit 1126 - 2089/2248

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC13

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	1	20040129087	A1	2004-07-08	ROWE; et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

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First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC13

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	HARRISON, MONICA D
Attorney Docket Number	3771-0003-DC13

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-08-27
Name/Print	Tarek N. Fahmi	Registration Number	41402

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"3983264".pn. and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 10:42
L2	1	"3983264".pn. and schottky and metal and oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 10:42
L3	60	("20040129087" | "20060178015" | "20140117465" | "4304042" | "4691219" | "5614745" | "6323508" | "6521502" | "0000001" | "0000002" | "10090395" | "20050093027" | "2981877" | "3614548" | "3623925" | "3719797" | "3877054" | "3983264" | "4110488" | "4278830" | "4356622" | "4485265" | "4538342" | "4696828" | "4698652" | "4752815" | "4763176" | "4772934" | "4794444" | "4796082" | "4800415" | "4801984" | "4835580" | "4960732" | "4961194" | "6724088" | "7176483" | "9461167" | "9905691" | "3590471" | "3708360" | "3983574" | "4019113" | "4056642" | "4300152" | "4338616" | "4422090" | "4485550" | "4566021" | "4583110" | "4689869" | "4723197" | "4811077" | "4843029" | "4999685" | "5021365" | "5027166" | "5098859" | "5191322" | "5216262").PN.	US-PGPUB; USPAT	OR	OFF	2020/09/17 11:28
L4	29	schottky and metal and oxide and L3	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2020/09/17 11:28

			EPO; JPO; DERWENT; IBM_TDB			
L5	15	(schottky with electron$4) and metal and oxide and L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:29
L6	14	(schottky with electron$4) and metal and oxide and L3 and (schottky near barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:30
L7	6	(schottky with electron$4) and metal and oxide and L3 and (schottky near barrier) and (schottky with holes)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:30
L8	5	(schottky with electron$4) and metal and oxide and L3 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:31

L9	0	(schottky with electron$4) and metal and oxide and L3 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and (undop$4 with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:31
L10	4	(schottky with electron$4) and metal and oxide and L3 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:32
L11	0	257/763.ccls. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:38
L12	79	257/'$'.ccls. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:39
L13	73	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/09/17 11:41

			DERWENT; IBM_TDB			
L14	37	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:42
L15	32	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:43
L16	36	H01L29/'$'.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:44
L17	14	H01L21/28,285,2853,28537.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:46
L18	20	H01L21/'$'.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate))	US-PGPUB; USPAT;	OR	ON	2020/09/17 11:47

		and undop$4 and (height with schottky) and (work near function)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L19	2	"10588748".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 12:43
L20	2	"10388748".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 12:44
L21	4	(schottky with electron$4) and metal and oxide and L3 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 13:34
L22	4	(schottky with electron$4) and metal and oxide and L3 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and acorn.asn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2020/09/17 13:37

			IBM_TDB			
S1	4	"16847878"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 14:54
S2	14	"15728002"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 14:54
S3	12	"15251210"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:20
S4	18	"15048877"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:24
S5	22	"13552556"	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2020/09/16 15:34

			EPO; JPO; DERWENT; IBM_TDB			
S6	25	"13022522"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:43
S7	25	"12197996"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:44
S8	36	"11181217"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:45
S9	76	"10217758"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:47

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First Named Inventor	Daniel E. Grupp
Art Unit	
Examiner Name	

Sheet	1	**of**	12	**Attorney Docket No:** 3771-0003-DC13

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](If known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		3513366	05/19/1970	CLARK	
		3590471	07/06/1971	LEPSELTER; et al.	
		3708360	01/02/1973	WAKEFIELD, JR.; et al.	
		3983264	09/28/1976	SCHROEN; et al.	
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		5243213	09/07/1993	MIYAZAWA; et al.	
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Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		EP 0295490 A1	12/21/1988	IBM		
		EP 0789388 A2	08/13/1997	AGENCY INDUSTRIAL SCIENCE AND TECHNOLOGY		
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		WO 2004/015782 A1	02/19/2004	ACORN TECHNOLOGIES, INC.		
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No.**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T2**
		Acorn Technologies, Inc., International Application No.: PCT/US2012/060893 filed 18 October 2012, ISA/US, International Search Report and Written Opinion, 11 December 2012, 23 pages.	
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		ADAM; et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", Applied Physics Letters (Jul. 2001), 79(5):623-625.	
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(Use as many sheets as necessary)

				Complete if Known
				Application Number	
				Filing Date	
				First Named Inventor	Daniel E. Grupp
				Art Unit	
				Examiner Name	
Sheet	12	**of**	12	**Attorney Docket No:** 3771-0003-DC13	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-04-14
Name/Print	Tarek N. Fahmi	Registration Number	41402

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	
Attorney Docket Number	3771-0003-DC13

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	2	4691219	A	1987-09-01	Goth	
	3	5614745	A	1997-03-25	Motonami	
	4	6323508	B1	2001-11-27	Takahashi, et al.	
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	2	20140117465	A1	2014-05-01	Huang, et al.	

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	1	ARCHIBONG, et al., On the Structure of A12O3 and Photoelectron Spectra of A12O2 and A12O3; J. Phys. Chem.A 1999, 103, pp. 1109-1114.	
	2	BORTZ, et al., Temperature Dependence of the Electronic Structure of Oxides: MgO, MgAl2O4 and Al2O3; Physica Scripta., Col. 41, pp. 537-541, 1990.	
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	7	IPR2020-01182; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 23, 2020; 139 pp.	
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	Examiner Name	
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	17	IPR2020-01207; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; June 29, 2020; 146 pp.	
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	19	IPR2020-01241; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 6, 2020; 165 pp.	
	20	IPR2020-01241; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,461,167; July 6, 2020; 84 pp.	
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	24	IPR2020-01279; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 9,905,691; July 10, 2020; 84 pp.	
	25	IPR2020-01282; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Declaration of Dr. E. Fred Schubert; July 12, 2020; 217 pp.	
	26	IPR2020-01282; Samsung Electronics Co., Ltd. v. Acorn Semi, LLC; Petition for Inter Partes Review of U.S. Patent No. 10,090,395; July 13, 2020; 85 pp.	
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	Art Unit	2815
	Examiner Name	
	Attorney Docket Number	3771-0003-DC13

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First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	
Attorney Docket Number	3771-0003-DC13

CERTIFICATION STATEMENT

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☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-07-15
Name/Print	Tarek N. Fahmi	Registration Number	41402

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SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/847,878	04/14/2020 RULE	257	2815	3771-0003-DC13

APPLICANTS
Acorn Semi, LLC, Palo Alto, CA;

INVENTORS /M.D.H/ 09/17/2020
Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

**** CONTINUING DATA ***************************
This application is a CON of 16/506,022 07/09/2019
which is a CON of 15/728,002 10/09/2017 PAT 10388748
which is a CON of 15/251,210 08/30/2016 PAT 9812542
which is a CON of 15/048,877 02/19/2016 PAT 9905691
which is a CON of 13/552,556 07/18/2012 PAT 9425277
which is a CON of 13/022,522 02/07/2011 PAT 8431469
which is a DIV of 12/197,996 08/25/2008 PAT 7884003
which is a DIV of 11/181,217 07/13/2005 PAT 7462860
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**** FOREIGN APPLICATIONS *************************** /M.D.H/ 09/17/2020

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TITLE

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Application Number	16/847,878
Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
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Sheet	1	of	9	**Attorney Docket No:** 3771-0003-DC13

U.S. PATENT DOCUMENTS

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		4845050	1989-07-04	Kim, et al.	
		6724088	2004-04-20	Jammy, et al.	
		7176483	2007-02-13	Grupp, et al.	
		9461167	2016-10-04	Grupp, et al.	
		9905691	2018-02-27	Grupp, et al.	
		10090395	2018-10-02	Grupp, et al.	
		20050093027	2005-05-05	Grupp; et al.	

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		APPENDIX A1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	
		APPENDIX A2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 7 pgs.	

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Application Number	16/847,878
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First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	

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		APPENDIX A3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 19 pgs.	
		APPENDIX A4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 21 pgs.	
		APPENDIX A6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	
		APPENDIX A7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 26 pgs.	
		APPENDIX A8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 28 pgs.	
		APPENDIX A10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 18 pgs.	
		APPENDIX B1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 41 pgs.	
		APPENDIX B2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 43 pgs.	

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		APPENDIX B4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 48 pgs.	
		APPENDIX B5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 47 pgs.	
		APPENDIX B6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 32 pgs.	
		APPENDIX B7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 42 pgs.	
		APPENDIX B8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 41 pgs.	
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		APPENDIX C1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	

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		APPENDIX C2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 5 pgs.	
		APPENDIX C3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 7 pgs.	
		APPENDIX C4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX C6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX C7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
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Sheet	5	of	9	**Attorney Docket No:** 3771-0003-DC13

		APPENDIX D1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 16 pgs.	
		APPENDIX D2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 20 pgs.	
		APPENDIX D3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 14 pgs.	
		APPENDIX D4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 11 pgs.	
		APPENDIX D5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 16 pgs.	
		APPENDIX D6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 12 pgs.	
		APPENDIX D7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 22 pgs.	
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		APPENDIX E1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
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		APPENDIX E8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX E10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 8 pgs.	
		APPENDIX F1., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 13 pgs.	
		APPENDIX F2., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	
		APPENDIX F3., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 11 pgs.	
		APPENDIX F4., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 15 pgs.	
		APPENDIX F5., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	
		APPENDIX F6., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 9 pgs.	

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Application Number	16/847,878
Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
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		APPENDIX F7., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 17 pgs.	
		APPENDIX F8., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 17 pgs.	
		APPENDIX F10., Claim Chart, from DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS AND ADDITIONAL DISCLOSURES PURSUANT TO PATENT LOCAL RULES dated May 19, 2020, ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD; et al., Civil Action No. 2:19-cv-347-JRG, 11 pgs.	
		De Bosscher, et al., The influence of silicide formation on the barrier height of Ti/Si MIS Schottky barriers, Semiconductor Sci., Tech., Vol. 1, 1986, pp. 376-382.	
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First Named Inventor	Daniel E. Grupp
Art Unit	2815
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Attorney Docket No: 3771-0003-DC13

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-06-17
Name/Print	Tarek N. Fahmi	Registration Number	41,402

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known	
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Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
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Sheet	5	of	24	**Attorney Docket No:** 3771-0003-DC13

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Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
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Sheet	11	of	24	**Attorney Docket No:** 3771-0003-DC13

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	16/847,878
Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	

Sheet	**23**	**of**	**24**	**Attorney Docket No:** 3771-0003-DC13

		Wilson, et al., Differential Capacitance-Voltage Profiling of Schottky Barrier Diodes for Measuring Implanted Depth Distributions in Silicon, U.S. Dept. of Commerce, Nat'l Bureau of Standards, Feb. 1982, 68 pgs.	
		Wittmer, et al., Ideal Schottky Diodes on Passivated Silicon, Physical Review Letters, Vol. 69, No. 18, Nov. 2, 1993, pp. 2701-2704.	
		Wu, Barrier height reduction of the Schottky barrier diode using a thin highly doped surface layer, Journal of Applied Physics, Vol. 51, No. 9, Sep. 1980, pp. 4919-4922.	
		Wu, et al., Interface capacitance in metal- semiconductor junctions, Journal of Applied Physics, Vol. 65, No. 9, May 1, 1989, pp. 3560-3567.	
		Yang, et al, Tunneling in a Metal- Semiconductor- Semiconductor Thin- Film Diode, Solid-State Elec., Vol. 29, No. 3, 1986, pp. 355-357.	
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		Zafar, A method for measuring barrier heights, metal work functions and fixed charge densities in metal/SiO2/Si capacitors, Applied Physics Letters, Vol. 80, No. 25, Jun. 24, 2002, pp. 4858-4860.	
		Zaima, et al., Electrical Properties and Crystallographic Structures of Transition Metal/Silicon Interface, Materia Japan, Vol. 33, No. 6, 1994, pp. 691-696.	
		Zaima, et al., Formation of silichide at metal/silicon interface and low-resistivity contacts, Applied Physics, Vol. 63, No. 11, 1994, pp. 1093-1105.	
		Zaima, et al., Study on determining factors of low contact resistivity in transition metal-silicon systems, Applied Surface Science, Vols. 70/71, 1993, pp. 624-628.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 09/17/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	**24**	**of**	**24**

Complete if Known

Application Number	16/847,878
Filing Date	04-14-2020
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	

Attorney Docket No: 3771-0003-DC13

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-06-17
Name/Print	Tarek N. Fahmi	Registration Number	41,402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENDFEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

[X] Practitioners associated with Customer Number: 27571

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

[X] The address associated with Customer Number: 27571

OR

[ ]

Firm or individual name		
Address		
City	State	Zip
Country		
Telephone	Email	

Assignee name and address: ACORN SEMI, LLC

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature	Date 07/10/2019
Name Tom Horgan	Telephone 858-775-1693
Title C.E.O.	

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 18 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Acorn Semi, LLC

Application No./Patent No.: 16/847,878 Filed/Issue Date: 04-14-2020

Titled: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECT

Acorn Semi, LLC, a company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: GRUPP, DANIEL E.; et al. To: ACORN TECHNOLOGIES, INC.

   The document was recorded in the United States Patent and Trademark Office at Reel 053773, Frame 0225, or for which a copy thereof is attached.

2. From: ACORN TECHNOLOGIES, INC. To: ACORN SEMI, LLC

   The document was recorded in the United States Patent and Trademark Office at Reel 053773, Frame 0306, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/	2020-09-23
Signature	Date
Tarek N. Fahmi	41402
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	40646341
Application Number:	16847878
International Application Number:	
Confirmation Number:	8164
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC13
Receipt Date:	23-SEP-2020
Filing Date:	14-APR-2020
Time Stamp:	16:19:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	Acorn_Semi_3771_Exe_POA.pdf	250008 5c4d6b3513a95bd0bc6e27d1ce83414ce09fcd58	no	2

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	3771-0003-DC13_Statement_3-73c.pdf	97896 15b2b11fa6883bc7e68e600e613fb1e63201cea9	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	347904		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/847,878	04/14/2020	Daniel E. Grupp	3771-0003-DC13

CONFIRMATION NO. 8164

POA ACCEPTANCE LETTER

27571
Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

OC000000120167363

Date Mailed: 09/28/2020

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/23/2020.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mbeyene/

GF Exhibit 1126 - 2162/2248

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/847,878	Filing Date 04/14/2020	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	12/22/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/MARCUS M WASHINGTON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	16847878
Filing Date	14-Apr-2020
First Named Inventor	Daniel Grupp
Attorney Docket Number	3771-0003-DC13
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Acorn Semi, LLC	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

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as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○	I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- (◉) Small Entity
- (○) Micro Entity
- (○) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- (◉) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

  Registration Number 41402

- (○) A sole inventor
- (○) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- (○) A joint inventor; all of whom are signing this request

Signature	/Tarek N. Fahmi/
Name	Tarek N. Fahmi

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16847878
Filing Date:	14-Apr-2020
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC13

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	170	170
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**170**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 16847878

Filing Date: 14-Apr-2020

Applicant/Patent under Reexamination: Grupp

Electronic Terminal Disclaimer filed on December 22, 2020

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	41461679
Application Number:	16847878
International Application Number:	
Confirmation Number:	8164
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC13
Receipt Date:	22-DEC-2020
Filing Date:	14-APR-2020
Time Stamp:	12:28:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$170
RAM confirmation Number	E2020BLC28396646
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33387 1fc89a3ab1d4b1c9f9e976cd42d5cf21bbf82b2c	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30329 2d83330d50e70b2d3ef4f18a467e556cf63b1219	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	63716		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 16/847,878

First Named Inventor: Daniel E. Grupp

Filed: 04/14/2020

Art unit: 2815

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC13

Confirmation No.: 8164

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

AMENDMENT

Dear Commissioner:

Responsive to the office action dated September 23, 2020, reconsideration of this application in view of the following amendments and remarks is respectfully requested.

Amendments to the claims are set forth in the listing of the claims that begins on page 2.

A Terminal Disclaimer with respect to US Pat. 10,388,748 accompanies this response.

Remarks begin on page 5.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/847,878	**12/22/2020 12:38:29 PM ET**	**3771-0003-DC13**

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8164	FILED BY	Sarah Zizzo
PATENT CENTER #	60122813	FILING DATE	04/14/2020
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel E. Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

TOTAL DOCUMENTS: 28

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
2020-12-22_3771-0003-DC13_R-OA.pdf		7	-	115 KB
2020-12-22_3771-0003-DC13_R-OA-A....pdf	(1-1)	1	Amendment/Req. Reconsideration-After Non-Final Reject	63 KB
2020-12-22_3771-0003-DC13_R-OA-CLM.pdf	(2-4)	3	Claims	71 KB
2020-12-22_3771-0003-DC13_R-OA-REM.pdf	(5-7)	3	Applicant Arguments/Remarks Made in an Amendment	102 KB
2020-12-21_3771-0003-		6	Information Disclosure	1011 KB

DC13_IDS.pdf		Statement (IDS) Form (SB08)	
2020-07-23 Joint Claim Construction and Prehearing Statement.pdf	10	Non Patent Literature	154 KB
2020-07-23 Joint Claim Construction Exhibit A - Plaintiffs Proposed Construction for Disputed Terms.pdf	9	Non Patent Literature	147 KB
2020-07-23 Joint Claim Construction Exhibit B - Defendants Proposed Construction for Disputed Terms.pdf	8	Non Patent Literature	140 KB
2020-08-20 Revised Joint Claim Construction Ex A - Pltfs Proposed Constructions for Disputed Terms.pdf	7	Non Patent Literature	130 KB
2020-08-20 Revised Joint Claim Construction and Prehearing Statement.pdf	9	Non Patent Literature	157 KB
2020-08-20 Revised Joint Claim Construction Ex B - Defs Revised Proposed Constructions for Disputed Terms.pdf	7	Non Patent Literature	134 KB
2020-08-21 Pltfs Opening Claim Construction Brief.pdf	39	Non Patent Literature	516 KB
2020-09-04 Defendants Responsive Claim Construction Brief.pdf	33	Non Patent Literature	367 KB
2020-09-11 Acorns Reply	17	Non Patent Literature	219 KB

Claim Construction Brief.pdf			
2020-09-18 Joint Claim Construction Chart Appendices.pdf	12	Non Patent Literature	137 KB
2020-09-18 Joint Claim Construction Chart.pdf	20	Non Patent Literature	241 KB
2020-12-14 Piner Rebuttal Report.pdf	114	Non Patent Literature	867 KB
EDTX-2-19-cv-00347-85.pdf	40	Non Patent Literature	443 KB
EDTX-2-19-cv-00347-103.pdf	2	Non Patent Literature	234 KB
Exhibit A.pdf	36	Non Patent Literature	429 KB
Exhibit B.pdf	4	Non Patent Literature	86 KB
Exhibit C.pdf	38	Non Patent Literature	350 KB
Exhibit D.pdf	7	Non Patent Literature	106 KB
Exhibit E.pdf	16	Non Patent Literature	198 KB
Exhibit F.pdf	8	Non Patent Literature	145 KB
Exhibit G.pdf	8	Non Patent Literature	144 KB
Exhibit H.pdf	4	Non Patent Literature	61 KB
Expert Report of Dr Jeffry Bokor re Invalidity.pdf	254	Non Patent Literature	10353 KB
Order Adopting Claim Construction Recommendation.pdf	2	Non Patent Literature	230 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2020-12-22_3771-0003-DC13_R-OA.pdf	5E5B4CB1315AF09D2C7D94CA3A5DFA26519D0C1539998FA3AFB91CE7B806BD1062492DF86D1047117835430F0EA82CC4FFB8405B5C07E77C1B7F20C6117FC0C7
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2020-12-22_3771-0003-DC13_R-OA-REM.pdf	66F0E7A26AF324478A210F14287D0565CDF3470D3C7ED930422DF5A372569A551D7772A9DFC152E7804CE4881341F7249D293D920D402796B97633C88E041E9C
2020-12-21_3771-0003-DC13_IDS.pdf	22BDB88DCE9DA3DBA5163EC3B4FCC45318347B40DAEA7654A343A3E195C8C9398AA2A4AB9CAF700FD316EABE09C13CBDF83E5837A64585E629B3D7E45AD87732
2020-07-23 Joint Claim Construction and Prehearing Statement.pdf	6F4E946CA8A46BBA360C9F441ED2733A80FC4C3B1D35A9CA85E6A61EDEA5AE09ED0E8305990EB672B9EB8CC11488071BF66C081B0DA77CA337B3C7EC33836C26
2020-07-23 Joint Claim Construction Exhibit A - Plaintiffs Proposed Construction for Disputed Terms.pdf	8EBDAFF7C3E965C26BF8CCB5CF1C99CA7E789242CAEC05C4E9E3C061346CA6BB318934A8AE985DD441456EA70D039CDA1EE4D2039A8259C17AE7313970F8CA58
2020-07-23 Joint Claim Construction Exhibit B - Defendants Proposed Construction for Disputed Terms.pdf	1EE1874DDE7F82B85800B546CE91F9E7C04E35197D03A27118971842E7CF6404BEA7325FEB3349C7821DDFBF7CB3341376A7471F1ADE117581F0B1688DB6CF71

2020-08-20 Revised Joint Claim Construction Ex A - Pltfs Proposed Constructions for Disputed Terms.pdf	97FF44A7A8007A50779C33CD17EFE7BBD2206AC19D59B56B5E065A1E0A2FCCED06E091F517DD35CD030AC1DC9E4FC2DCB730DA1DB5B957F8C923DD68DA2979EA
2020-08-20 Revised Joint Claim Construction and Prehearing Statement.pdf	69A2FA2EB90E7B6051FDF546CB9BC9246F2EB36F487F27DCA33EE09E5A24FF751E0DEE3F667E2F4538EAACA09377FDD605CC4B8D99B0A79C5FBE42E280ABA8D3
2020-08-20 Revised Joint Claim Construction Ex B - Defs Revised Proposed Constructions for Disputed Terms.pdf	53AF43FDAFCD62A323F08E6BF10581F6C558895D75BD3EE98C7E5600AB4950294FC3963052B740F3A499B6335AB37D2E6033A95AB039978FDCAB044A8DF8FE78
2020-08-21 Pltfs Opening Claim Construction Brief.pdf	A412AF74CB5A0D0D3A4E89DDFC25AC4719E661378B75EF211BDD260465A7EF319CBD68F26ACAAF775681B3C8BA4B4481D349FDAFB569B2B4983721E8354D0A88
2020-09-04 Defendants Responsive Claim Construction Brief.pdf	868F1F1B53EFFC18069CEFE15B66DC6E6878147936FC946F8978317A992F5E6B8A67DD1EDB6BE91F3C9338A7816280DB414A373C2687C3417A2495FE1CCB8964
2020-09-11 Acorns Reply Claim Construction Brief.pdf	49B35929D7891A7DE5D39480634 7D9B3516F17637805E7643394C26C5A22052AFDC82802E4F0C58A7D28E29588B838F44E458DA734206469E88DDA24851CDB99
2020-09-18 Joint Claim Construction Chart Appendices.pdf	9FDEC7CCC3CFC59D97F3DDC9F54A1E8D44B239E0D030BF617A2DC00A1AD202F56DEB4FDF32E5801EDD6A0E2ADC37EC8E92936A1C191550F320D88D305593DB27
2020-09-18 Joint Claim Construction Chart.pdf	01F92CAB7BB52A9A2196370AC418F0B28390BAE3A336B5159C5A0DA1214250833E86CBF6B643DF984335A21A08B973864E38FC253B2EAECB0107CA6ADB7999A9
2020-12-14 Piner Rebuttal Report.pdf	924C9B77686757E00FA7AC61FF5FCF4738FD2015813127BA115BBE9F744F4E8A99BBA6F816DF32388E8001ED605EF3E135484C2C5344F1521386143A0FB4EC82
EDTX-2-19-cv-00347-85.pdf	45117B81F914EF82AA6BE2AD943A9E6F73464176D20AC57DC1EDFE15BE5079BB931988049501ACB4BBA0614BFB2E75439F

	4B42244EF29A418256D3EB1E96DE65
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Exhibit A.pdf	35C8E44BE90149656E7B608F265A195F6956F40CB6E761F733278E328BBA590B46FA5BB0B157A7E8C62AEA32527A28178472BEF79D2197675C1E848C9C0FF015
Exhibit B.pdf	B7F5EE80971C53A303C0C643E425A2AF8E75A7B1CC51E3F379CF7F1EFF25288BAA6D741C558A31DE0DF69250D7FABBED97808A87C7DD12EB51626BF34898BB59
Exhibit C.pdf	5765EFF86E29CBB24B6CB6359EC5888399EB587400C1D24AA4340DE38120B683E8DC0024DB9B14A23F838DB111188A0061C84609747901051CE7F113439B0972
Exhibit D.pdf	EEFC2F3F8D8953381640535439B2A87ABF4242D47AB1C17CA94255DA4C10C69BAF88BDD2A0391B92E20BFEB87697163A6D81E0ED145A6973D8720EB3C5023124
Exhibit E.pdf	22BA94AEF5A1104CC7D474716AF1659D592865A18781A3C6D19C77FD7D262715EE80B4808772719576642000504749020DBFEE82F724F618BF473FD16AC5E2F0
Exhibit F.pdf	E14D29374ADA9F03771BBA14BC5A6A7392ADC61E9528D6D836222DC86CD29584FBD17E29C8DC5D0ECD14E1BAAFC464866BA46181E6AE21C69128499C883E0E68
Exhibit G.pdf	483BD5B5A258F85AB8034D2A0F023FA5A4F3D4920FE5A6A07FDEB7B8F8CC0D20BBB68B66DA36A4688AF1CB213DC62F06DF9934317BB19A972E21ED25B9DAF5D8
Exhibit H.pdf	EB6905903E8243AA12AFF10193B326847231CD8CA1450D51FCB6F6456881AF375A886627EFABA9CFF246C0F040E56CE10EAFE29201CFB0A74B8240D94E67C874
Expert Report of Dr Jeffry Bokor re Invalidity.pdf	1B75884B0931A0D0C383FE61620FB373D297AC78797CB7DD896C7B5977B9D998C14795E8C3EC7D4961DB44CC2EBC6FFCD

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Order Adopting Claim Construction Recommendation.pdf	DC060FEE38ED6FFF6A5F575109F324CBD90995C7D8B56AF62CD6D974F5CB65C102062FDB9AF114DC14F82A5936BB07D082966E3F214FAE4E128562D6AB964841

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/847,878	12/22/2020 12:38:29 PM ET	3771-0003-DC13

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	8164	FILED BY	Sarah Zizzo
PATENT CENTER #	60122813	AUTHORIZED BY	Tarek Fahmi
CUSTOMER #	27571	FILING DATE	04/14/2020
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Daniel E. Grupp

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 4028	E2020BLC39186871	Sarah Zizzo

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	130.00	1	130.00
			TOTAL AMOUNT:	$130.00

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If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

AMENDMENTS TO THE CLAIMS

The following listing of the claims shall replace all previous versions thereof in this application.

Listing of the Claims:

1. (Currently Amended) An electrical junction, comprising:

a semiconductor substrate;

a metal electrical contact proximate to said semiconductor substrate; and

a passivating dielectric tunnel barrier layer disposed between said semiconductor substrate and said metal electrical contact,

said semiconductor substrate being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer is configured to increase a height of a Schottky barrier for electrons between the metal electrical contact and the semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween.

2. (Original) The electrical junction of claim 1, wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si.

3. (Original) The electrical junction of claim 2, wherein the metal electrical contact comprises a metal having a work function near or substantially equal to a conduction band edge of the semiconductor.

4. (Original) The electrical junction of claim 3, wherein the metal having a work function near or substantially equal to a conduction band edge of the semiconductor comprises one of: aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum

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(Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn).

5. (Original) The electrical junction of claim 3, wherein the semiconductor substrate is doped p-type proximate to the electrical contact.

6. (Original) The electrical junction of claim 3, wherein the semiconductor substrate is undoped proximate to the electrical contact.

7. (Currently Amended) An electrical junction, comprising:

a semiconductor substrate;

a metal electrical contact proximate to said semiconductor substrate;

and a passivating dielectric tunnel barrier layer disposed between said semiconductor substrate and said metal electrical contact,

said semiconductor substrate being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer is configured to increase a height of a Schottky barrier for holes between the metal electrical contact and the semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween.

8. (Original) The electrical junction of claim 7, wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si.

9. (Original) The electrical junction of claim 8, wherein the metal electrical contact comprises a metal having a work function near or substantially equal to a valence band edge of the semiconductor.

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10. (Original) The electrical junction of claim 9, wherein the metal having a work function near or substantially equal to a valence band edge of the semiconductor comprises one of: platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Go), or palladium (Pd).

11. (Original) The electrical junction of claim 9, wherein the semiconductor substrate is doped n-type proximate to the electrical contact.

12. (Original) The electrical junction of claim 9, wherein the semiconductor substrate is undoped proximate to the electrical contact.

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REMARKS

Reconsideration of this application in view of the forgoing amendments and the concurrently filed terminal disclaimer with respect to US Pat. 10,388,748 is respectfully requested.

As noted in the specification and the Application Data Sheet filed April 14, 2020, the present application is a CONTINUATION of U.S. Patent Application 16/506,022, filed July 9, 2019, which is a CONTINUATION of U.S. Patent Application 15/728,002, filed 10/9/2017, now U.S. Patent 10,388,748, which is a CONTINUATION of U.S. Patent Application No. 15/251,210, filed 8/30/2016, now U.S. Patent 9,812,542, which is a CONTINUATION of U.S. Patent Application No. 15/048,877, filed 2/19/2016, now U.S. Patent 9,905,691, which is a CONTINUATION of U.S. Patent Application No. 13/552,556, filed 7/18/2012, now U.S. Patent 9,425,277, which is a CONTINUATION of U.S. Patent Application No. 13/022,522, filed 2/7/2011, now U.S. Patent 8,431,469, which is a DIVISIONAL of U.S. Patent Application 12/197,996, filed 8/25/2008, now U.S. Patent 7,884,003, which is a DIVISIONAL of U.S. Patent Application 11/181,217, filed 7/13/2005, now U.S. Patent 7,462,860, which is a CONTINUATION of U.S. Patent Application 10/217,758, filed 8/12/2002, now U.S. Patent 7,084,423. All of the requirements of 35 USC 120 and 37 CFR 1.78 having thus been satisfied, the application is entitled to its full priority claim.

Claims 1 and 7 have been amended to recite the metal electrical contact proximate to the semiconductor substrate; and the passivating dielectric tunnel barrier layer disposed between the semiconductor substrate and the metal electrical contact. Support for this amendment is found in the specification as filed, for example at [0013], [0026], [0047]-[0053], and [0069]-[0073] and Fig. 6. Accordingly, the rejection of claims 1 and 7 under 35 USC 112(b) should be withdrawn inasmuch as claims 1 and 7, as amended, recite the metal electrical contact proximate to the semiconductor substrate. The claims

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further make clear that the passivating dielectric tunnel barrier layer is disposed between the semiconductor substrate and the metal electrical contact, and the semiconductor substrate is electrically connected to the metal electrical contact through the passivating dielectric tunnel barrier layer.

The obviousness-type double patenting rejection of the claims is overcome by the terminal disclaimer with respect to US Pat. 10,388,748.

The rejection of claims 1-12 as being anticipated by Schroen, US 3,983,264, should be withdrawn. Contrary to the conclusions set forth in the office action, Schroen does not teach or suggest a passivating dielectric tunnel barrier layer configured to increase a height of a Schottky barrier for electrons between a metal electrical contact and a semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween, as recited in claim 1. Nor does Schroen teach or suggest a passivating dielectric tunnel barrier layer configured to increase a height of a Schottky barrier for holes between a metal electrical contact and a semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween, as recited in claim 7. If anything, Schroen teaches the opposite. For example, at 5:30 et seq, Schroen explains that by providing the oxide layer 15 between the metal 16 and the silicon substrate 11, "[e]xtremely low specific contact resistance is obtained, as contrasted with the Schottky barrier behavior obtained by direct metalization." This is an indication that the presence of the oxide layer 15 results in a *reduced* Schottky barrier height (for electrons or holes as appropriate for p-type or n-type substrates) from that which would exist in its absence. This is the opposite of what is being claimed in claims 1 and 7; hence, claims 1 and 7, and their respective dependent claims are not anticipated by Schroen.

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Respectfully submitted,
Ascenda Law Group, PC

Dated: December 22, 2020

/Tarek N. Fahmi/
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC13

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC13

	1	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction and Prehearing Statement, 10 pgs. (Jul. 23, 2020).	
	2	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Joint Claim Construction and Prehearing Statement, 9 pgs. (Jul. 23, 2020).	
	3	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Joint Claim Construction and Prehearing Statement, 8 pgs. (Jul. 23, 2020).	
	4	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Revised Joint Claim Construction and Prehearing Statement, 9 pgs. (Aug. 20, 2020).	
	5	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).	
	6	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).	
	7	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Opening Claim Construction Brief, 39 pgs. (Aug. 21, 2020).	
	8	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Defendant's Responsive Claim Construction Brief, 33 pgs. (Sep. 4, 2020).	
	9	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Reply Claim Construction Brief, 17 pgs. (Sep. 11, 2020).	
	10	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart, 20 pgs. (Sep. 18, 2020).	
	11	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart Appendices, 12 pgs. (Aug. 21, 2020).	

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	12	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Construction Memorandum Opinion and Order, 40 pgs. (Oct. 16, 2020).	
	13	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Order Correcting Typographical Error in Claim Construction Memorandum Opinion and Order, 2 pgs. (Nov. 18, 2020).	
	14	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Order of Judge R. Gilstrap Adopting Claim Construction Memorandum Opinion and Order, 2 pgs. (Dec. 10, 2020).	
	15	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Expert Report of Dr. Jeffrey Bokor Regarding Invalidity of U.S. Patent No. 7,084,423, U.S. Patent No. 8,766,336, U.S. Patent No. 9,209,261, U.S. Patent No. 9,461,167, U.S. Patent No. 9,905,691, and U.S. Patent No. 10,090,395 (Redacted) (Nov. 16, 2020).	
	16	Exhibit A to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), CV of Dr. Jeffrey Boker, 36 pgs. (Nov. 16, 2020).	
	17	Exhibit B to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Materials Considered in Connection with Report, 4 pgs. (Nov. 16, 2020).	
	18	Exhibit C to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '336 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 38 pgs. (Nov. 16, 2020).	
	19	Exhibit D to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '261 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 7 pgs. (Nov. 16, 2020).	
	20	Exhibit E to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '167 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 16 pgs. (Nov. 16, 2020).	
	21	Exhibit F to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '691 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 8 pgs. (Nov. 16, 2020).	
	22	Exhibit G to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipated of '395 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 8 pgs. (Nov. 16, 2020).	

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	Application Number	16847878
	Filing Date	2020-04-14
	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC13

	23	Exhibit H to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), List of Claims by Grouping, 4 pgs. (Nov. 16, 2020).
	24	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Rebuttal Expert Report of Edwin Piner, Ph.D. (Redacted) (Dec. 14, 2020).

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC13

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-12-22
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

EXAMINER
HARRISON, MONICA D

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/26/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/847,878	04/14/2020	Daniel E. Grupp	3771-0003-DC13	8164

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	04/26/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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Suite 420
San Jose, CA 95131

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/847,878	04/14/2020	Daniel E. Grupp	3771-0003-DC13	8164

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	04/26/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
HARRISON, MONICA D	2815	257-763000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

GF Exhibit 1126 - 2194/2248

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/847,878	04/14/2020	Daniel E. Grupp	3771-0003-DC13	8164

27571 7590 01/26/2021

Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/26/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

GF Exhibit 1126 - 2195/2248

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/847,878	Applicant(s) Grupp et al.	
	Examiner MONICA D HARRISON	Art Unit 2815	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 12/22/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-12 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/22/2020.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MONICA D HARRISON/
Primary Examiner, Art Unit 2815

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

1. Applicant's arguments, amendments and terminal disclaimer filed 12/22/2020 have been entered and considered.

Terminal Disclaimer

2. The terminal disclaimer filed on 12/22/2020 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of **10,388,748 B2 (Grupp et al)** has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

3. Claims 1-12 are allowed over the prior art of record.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance: After consideration and persuasion of applicant's arguments, amendments, approval of the terminal disclaimer and a further search of the prior art of record, examiner has concluded that the prior art does not disclose nor fairly suggest an electrical junction as described in independent claims 1 and 7.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to

avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MONICA D HARRISON whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7-4:30pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system,

see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MONICA D HARRISON/
Primary Examiner, Art Unit 2815

mdh
January 13, 2021

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	**Art Unit**
	MONICA D HARRISON	2815

CPC						
Symbol					**Type**	**Version**
H01L	/	29	/	456	F	2013-01-01
H01L	/	21	/	28537	I	2013-01-01
H01L	/	29	/	0895	I	2013-01-01
H01L	/	29	/	47	I	2013-01-01
H01L	/	29	/	66143	I	2013-01-01
H01L	/	29	/	812	I	2013-01-01
H01L	/	29	/	66643	I	2013-01-01
H01L	/	29	/	78	I	2013-01-01
H01L	/	29	/	7839	I	2013-01-01
H01L	/	29	/	16	I	2013-01-01
H01L	/	29	/	161	I	2013-01-01
H01L	/	29	/	45	I	2013-01-01
H01L	/	29	/	1608	I	2013-01-01
H01L	/	29	/	872	I	2013-01-01
H01L	/	29	/	806	I	2013-01-01
H01L	/	29	/	785	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	12	
/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	13 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig. 6

U.S. Patent and Trademark Office — Part of Paper No.: 20210113

GF Exhibit 1126 - 2201/2248

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	**Art Unit**
	MONICA D HARRISON	2815

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L	/	29	/	456	
H01L	/	21	/	28537	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	763

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	12	
/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	13 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig. 6

U.S. Patent and Trademark Office — Part of Paper No.: 20210113

GF Exhibit 1126 - 2202/2248

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	**Art Unit**
	MONICA D HARRISON	2815

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	13 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig. 6

U.S. Patent and Trademark Office Part of Paper No.: 20210113

GF Exhibit 1126 - 2203/2248

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L29/ 456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785	09/17/2020	MDH
H01L21/28,285,2853,28537	09/17/2020	MDH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
257	763	09/17/2020	MDH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

Search Notes		
Search Notes	**Date**	**Examiner**
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	09/17/2020	MDH
GRUPP ET AL .inv.	09/17/2020	MDH
ACORN TECHNOLOGIES .asn.	09/17/2020	MDH
IPR2020-01182 Reviewed Petition for Inter Partes Review of US. Patent No. 7,084,423 and Exhibits Ex.1001-Ex.1025	09/17/2020	MDH
IPR2020-01206 Reviewed Petition for Inter Partes Review of US. Patent No. 9,905,691 and Exhibits Ex.1001-Ex.1035	09/17/2020	MDH
PR2020-01279 Reviewed Petition for Inter Partes Review of US. Patent No. 9,905,691 and Exhibits Ex.1101-Ex.1150	09/17/2020	MDH
East updated	01/13/2021	MDH
USPAT, US-PGPUB txt .clm.	01/13/2021	MDH

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	USPAT, US-PGPUB txt .clm.	01/13/2021	MDH

/MONICA D HARRISON/ Primary Examiner, Art Unit 2815	

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/847,878	Grupp et al.
	Examiner	Art Unit
	MONICA D HARRISON	2815

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/17/2020	01/13/2021							
	1	✓	=							
	2	✓	=							
	3	✓	=							
	4	✓	=							
	5	✓	=							
	6	✓	=							
	7	✓	=							
	8	✓	=							
	9	✓	=							
	10	✓	=							
	11	✓	=							
	12	✓	=							

GF Exhibit 1126 - 2206/2248

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	"16847878"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 17:40
L2	60	("20040129087" | "20060178015" | "20140117465" | "4304042" | "4691219" | "5614745" | "6323508" | "6521502" | "0000001" | "0000002" | "10090395" | "20050093027" | "2981877" | "3614548" | "3623925" | "3719797" | "3877054" | "3983264" | "4110488" | "4278830" | "4356622" | "4485265" | "4538342" | "4696828" | "4698652" | "4752815" | "4763176" | "4772934" | "4794444" | "4796082" | "4800415" | "4801984" | "4835580" | "4960732" | "4961194" | "6724088" | "7176483" | "9461167" | "9905691" | "3590471" | "3708360" | "3983574" | "4019113" | "4056642" | "4300152" | "4338616" | "4422090" | "4485550" | "4566021" | "4583110" | "4689869" | "4723197" | "4811077" | "4843029" | "4999685" | "5021365" | "5027166" | "5098859" | "5191322" | "5216262").PN.	US-PGPUB; USPAT	OR	OFF	2021/01/13 17:41
L3	1	L2 and (substrate wafer carrier base plate) with (tunnel near barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 17:45
L4	1	L2 and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2021/01/13 17:45

			EPO; JPO; DERWENT; IBM_TDB			
L5	1	L2 and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 17:52
L6	4	"3983264".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 17:56
L7	61	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:00
L8	2	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:01

L9	2	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:02
L10	7	H01L29/'$'.cpc. and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:03
L11	0	H01L21/28,285,2853,28537.cpc. and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:04
L12	0	H01L21/'$'.cpc. and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:08
L13	8	(substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/01/13 18:08

			DERWENT; IBM_TDB			
L14	0	257/763.ccls. and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:11
L15	7	257/'$'.ccls. and (substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:11
L16	0	(substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height and (connelly grupp).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:13
L17	0	(substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height and acorn.asn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/13 18:14
S1	4	"16847878"	US-PGPUB; USPAT;	OR	ON	2020/09/16 14:54

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S2	14	"15728002"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 14:54
S3	12	"15251210"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:20
S4	18	"15048877"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:24
S5	22	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2020/09/16 15:34

			IBM_TDB			
S6	25	"13022522"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:43
S7	25	"12197996"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:44
S8	36	"11181217"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:45
S9	76	"10217758"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/16 15:47
S10	2	"3983264".pn. and schottky	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2020/09/17 10:42

			EPO; JPO; DERWENT; IBM_TDB			
S11	1	"3983264".pn. and schottky and metal and oxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 10:42
S12	60	("20040129087" | "20060178015" | "20140117465" | "4304042" | "4691219" | "5614745" | "6323508" | "6521502" | "0000001" | "0000002" | "10090395" | "20050093027" | "2981877" | "3614548" | "3623925" | "3719797" | "3877054" | "3983264" | "4110488" | "4278830" | "4356622" | "4485265" | "4538342" | "4696828" | "4698652" | "4752815" | "4763176" | "4772934" | "4794444" | "4796082" | "4800415" | "4801984" | "4835580" | "4960732" | "4961194" | "6724088" | "7176483" | "9461167" | "9905691" | "3590471" | "3708360" | "3983574" | "4019113" | "4056642" | "4300152" | "4338616" | "4422090" | "4485550" | "4566021" | "4583110" | "4689869" | "4723197" | "4811077" | "4843029" | "4999685" | "5021365" | "5027166" | "5098859" | "5191322" | "5216262").PN.	US-PGPUB; USPAT	OR	OFF	2020/09/17 11:28
S13	29	schottky and metal and oxide and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:28
S14	15	(schottky with electron$4) and metal and oxide and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/09/17 11:29

			DERWENT; IBM_TDB			
S15	14	(schottky with electron$4) and metal and oxide and S12 and (schottky near barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:30
S16	6	(schottky with electron$4) and metal and oxide and S12 and (schottky near barrier) and (schottky with holes)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:30
S17	5	(schottky with electron$4) and metal and oxide and S12 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:31
S18	0	(schottky with electron$4) and metal and oxide and S12 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and (undop$4 with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:31
S19	4	(schottky with electron$4) and metal and oxide and S12 and (schottky near barrier) and (schottky with holes) and	US-PGPUB; USPAT;	OR	ON	2020/09/17 11:32

		(dop$4 with (substrate wafer carrier base plate)) and undop$4	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S20	0	257/763.ccls. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:38
S21	79	257/'$'.ccls. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:39
S22	73	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:41
S23	37	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2020/09/17 11:42

			IBM_TDB			
S24	32	H01L29/456,0895,16,1608,161,45,47,66143,66643,78,7839,806,812,872,785.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:43
S25	36	H01L29/'$'.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:44
S26	14	H01L21/28,285,2853,28537.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:46
S27	20	H01L21/'$'.cpc. and (schottky with electron$4) and metal and oxide and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (height with schottky) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 11:47
S28	2	"10588748".pn.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2020/09/17 12:43

			EPO; JPO; DERWENT; IBM_TDB			
S29	2	"10388748".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 12:44
S30	4	(schottky with electron$4) and metal and oxide and S12 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 13:34
S31	4	(schottky with electron$4) and metal and oxide and S12 and (schottky near barrier) and (schottky with holes) and (dop$4 with (substrate wafer carrier base plate)) and undop$4 and acorn.asn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/17 13:37

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L18	1	(substrate wafer carrier base plate) with (tunnel near barrier) and (tunnel near barrier) with (metal conduct$4) and schottky and (fermi near level) with tunnel and height .clm.	US-PGPUB; USPAT	OR	ON	2021/01/13 18:14

1/13/2021 6:52:42 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\16847878.wsp

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16847878
Filing Date	2020-04-14
First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC13

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

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	Attorney Docket Number	3771-0003-DC13

	1	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction and Prehearing Statement, 10 pgs. (Jul. 23, 2020).	
	2	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Joint Claim Construction and Prehearing Statement, 9 pgs. (Jul. 23, 2020).	
	3	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Joint Claim Construction and Prehearing Statement, 8 pgs. (Jul. 23, 2020).	
	4	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Revised Joint Claim Construction and Prehearing Statement, 9 pgs. (Aug. 20, 2020).	
	5	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).	
	6	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).	
	7	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Opening Claim Construction Brief, 39 pgs. (Aug. 21, 2020).	
	8	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Defendant's Responsive Claim Construction Brief, 33 pgs. (Sep. 4, 2020).	
	9	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Reply Claim Construction Brief, 17 pgs. (Sep. 11, 2020).	
	10	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart, 20 pgs. (Sep. 18, 2020).	
	11	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart Appendices, 12 pgs. (Aug. 21, 2020).	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
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	12	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Construction Memorandum Opinion and Order, 40 pgs. (Oct. 16, 2020).	
	13	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Order Correcting Typographical Error in Claim Construction Memorandum Opinion and Order, 2 pgs. (Nov. 18, 2020).	
	14	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Order of Judge R. Gilstrap Adopting Claim Construction Memorandum Opinion and Order, 2 pgs. (Dec. 10, 2020).	
	15	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Expert Report of Dr. Jeffrey Bokor Regarding Invalidity of U.S. Patent No. 7,084,423, U.S. Patent No. 8,766,336, U.S. Patent No. 9,209,261, U.S. Patent No. 9,461,167, U.S. Patent No. 9,905,691, and U.S. Patent No. 10,090,395 (Redacted) (Nov. 16, 2020).	
	16	Exhibit A to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), CV of Dr. Jeffrey Boker, 36 pgs. (Nov. 16, 2020).	
	17	Exhibit B to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Materials Considered in Connection with Report, 4 pgs. (Nov. 16, 2020).	
	18	Exhibit C to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '336 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 38 pgs. (Nov. 16, 2020).	
	19	Exhibit D to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '261 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 7 pgs. (Nov. 16, 2020).	
	20	Exhibit E to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '167 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 16 pgs. (Nov. 16, 2020).	
	21	Exhibit F to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '691 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 8 pgs. (Nov. 16, 2020).	
	22	Exhibit G to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipated of '395 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Patent 7,176,483, 8 pgs. (Nov. 16, 2020).	

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	First Named Inventor	Daniel E. Grupp
	Art Unit	2815
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC13

	23	Exhibit H to Expert Report of Dr. Jeffrey Bokor in ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), List of Claims by Grouping, 4 pgs. (Nov. 16, 2020).
	24	ACORN SEMI, LLC v. SAMSUNG ELECTRONICS CO., LTD., ET AL., Case No. 2:19-cv-347-JRG (EDTX), Rebuttal Expert Report of Edwin Piner, Ph.D. (Redacted) (Dec. 14, 2020).

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EXAMINER SIGNATURE

Examiner Signature	/MONICA D HARRISON/	Date Considered	01/13/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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First Named Inventor	Daniel E. Grupp
Art Unit	2815
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC13

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2020-12-22
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
16847878	14-Apr-2020	Daniel Grupp	3771-0003-DC13	8164

TITLE OF INVENTION :

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Small	Utility under 35 USC 111(a)	2815	763000	MONICA HARRISON

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$600	$0	$600	26-Apr-2021	$0

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
27571 Ascenda Law Group, PC 2150 N First Street Suite 420 San Jose CA 95131 UNITED STATES 408-799-0612 patents@ascendalaw.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☐ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

◉ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

○ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

GF Exhibit 1126 - 2225/2248

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☒ Issue Fee

☐ I authorize USPTO to apply my previously paid issue fee to the current fees due

☐ Publication Fee

☐ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number _____

☐ Advance Order - # of copies _____

☒ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency or credit any overpayment, to Deposit Account Number 505798 . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. Ascenda Law Group, PC
2.
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Acorn Semi, LLC	Palo Alto	CALIFORNIA	united states	other

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Tarek N. Fahmi/	**Date**	04-26-2021
Name	Tarek N. Fahmi	**Registration Number**	41402

Electronic Patent Application Fee Transmittal

Application Number:	16847878
Filing Date:	14-Apr-2020
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC13

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPL ISSUE FEE	2501	1	600	600
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**600**

Electronic Acknowledgement Receipt

EFS ID:	42548333
Application Number:	16847878
International Application Number:	
Confirmation Number:	8164
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC13
Receipt Date:	26-APR-2021
Filing Date:	14-APR-2020
Time Stamp:	11:49:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$600
RAM confirmation Number	E20214PB49312886
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46029 1ad44702b98a3de94c4640f093640b3e3d1878d4	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32131 6b6c73edd8ebe53e80016cdba79a046165772104	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	78160		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/847,878	05/25/2021	11018237	3771-0003-DC13	8164

27571 7590 05/05/2021

Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Daniel E. Grupp, Palo Alto, CA;
Acorn Semi, LLC, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PTO/AIA/14 (01-22)
Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	16/847,878
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	~~Acorn Semi, LLC~~ Oak iP, LLC		
Mailing Address Information For Applicant:			
Address 1	~~455 Cambridge Ave.~~ 812 West McDermott Dr. #1026		
Address 2			
City	~~Palo Alto~~ Allen	**State/Province**	~~CA~~ TX
Country US		Postal Code	~~94306~~ 75013
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (01-22)
Approved for use through 05/31/2024. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC13
	Application Number	16/847,878
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Tarek N. Fahmi/			Date (YYYY-MM-DD)	2025-01-10
First Name	Tarek	Last Name	Fahmi	Registration Number	41402

Additional Signature may be generated within this form by selecting the Add button.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: OAK IP, LLC

Application No./Patent No.: 10,937,880 Filed/Issue Date: 03/02/2021

Titled: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

OAK IP, LLC, a company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: GRUPP, DANIEL E.; et al. To: ACORN TECHNOLOGIES, INC.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 053773, Frame 0225, or for which a copy thereof is attached.

2. From: ACORN TECHNOLOGIES, INC. To: ACORN SEMI, LLC

   The document was recorded in the United States Patent and Trademark Office at
   Reel 053773, Frame 0306, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: ACORN SEMI, LLC To: OAK IP, LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 069681, Frame 0837, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/	2025-01-10
Signature	Date
Tarek N. Fahmi	41402
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/847,878	**01/10/2025 04:59:18 PM Z ET**	**3771-0003-DC13**

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	11018237
CONFIRMATION #	8164	FILED BY	SARAH ZIZZO
PATENT CENTER #	68691798	FILING DATE	04/14/2020
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel E. Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Oak_IP_LLC_Exe_POA.pdf	4	Power of Attorney	258 KB
16847878_Statement_3-73c.pdf	3	Assignee showing of ownership per 37 CFR 3.73	118 KB
16847878_ADS_Acorn-Semi.pdf	2	Application Data Sheet	137 KB

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Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)

Oak_IP_LLC_Exe_POA.pdf	EB6526859CF929C3D04F15E92BD8DC1D4154F6AAFCF6F4BD08692FDA0C79D61A0524084B92C1C8911741CAD66222687A929690F36A553B7ED3CD75DF8D353B3E
16847878_Statement_3-73c.pdf	883DE4A07931AFE245F31F64519FD627F73D1B71AFB7488ADFBB526D53486984A175B3E20FB16896A5E6BD674D19AC6E162ACCA5039C74D542C25B81DFF9B3C3
16847878_ADS_Acorn-Semi.pdf	924AAD5B9EA7015F62D4D87985FC72C807B3F9C43C198DED31C2E57F3CF43E67CCD14234AC841FB9166C3BAA091F4B32DE9D59539668848D28969C3C8A58CF00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REVOCATION OF PREVIOUS POWERS OF ATTORNEY WITH NEW GENERAL POWER OF ATTORNEY TO PROSECUTE APPLICATIONS AND REEXAMINATION PROCEEDINGS BEFORE THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby revoke all previous powers of attorney given in the application(s), reexamination proceeding(s) and/or patent(s) listed below and appoint:

	Practitioners associated with the Customer Number	27571	

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications and reexamination proceedings assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73.

Please change the correspondence address for the application(s), reexamination proceeding(s) and/or patent(s) listed below to the address associated with Customer Number 27571.

Assignee Name and Address:

Oak IP, LLC
812 West McDermott Dr. #1026
Allen, TX 75013

A statement under 37 CFR 3.73 is attached.

List of application(s), reexamination proceeding(s) and/or patent(s):

See Attached List

SIGNATURE OF ASSIGNEE OF RECORD
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date: 12/27/24
Name	David Pridham	Telephone: 214-414-1164
Title	CEO	

Patent Number	Title	Issue Date
US-7084423-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	08/01/2006
US-7462860-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	12/09/2008
US-7884003-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	02/08/2011
US-8431469-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	04/30/2013
US-9209261-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	12/08/2015
US-9425277-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	08/23/2016
US-9812542-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	11/07/2017
US-10186592-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	01/22/2019
US-10388748-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	08/20/2019
US-11355613-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	06/07/2022
US-10937880-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	03/02/2021
US-10950707-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	03/16/2021
US-11018237-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	05/25/2021
US-11056569-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	07/06/2021
US-8766336-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	07/01/2014
US-9461167-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	10/04/2016

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Patent Number	Title	Issue Date
US-9905691-B2	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	02/27/2018
US-10090395-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	10/02/2018
US-6833556-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	12/21/2004
US-7112478-B2	Insulated gate field effect transistor having passivated Schottky barriers to the channel	09/26/2006
US-7883980-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	02/08/2011
US-8377767-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	02/19/2013
US-8916437-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	12/23/2014
US-9583614-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	02/28/2017
US-11043571-B2	Insulated gate field effect transistor having passivated schottky barriers to the channel	06/22/2021
US-6891234-B1	Transistor with workfunction-induced charge layer	05/10/2005
US-7382021-B2	Insulated gate field-effect transistor having III-VI source/drain layer(s)	06/03/2008
US-7176483-B2	Method for depinning the Fermi level of a semiconductor at an electrical junction and devices incorporating such junctions	02/13/2007
US-7902029-B2	Process for fabricating a self-aligned deposited source/drain insulated gate field-effect transistor	03/08/2011
US-8263467-B2	Process for fabricating a self-aligned deposited source/drain insulated gate field-effect transistor	09/11/2012
US-8212336-B2	Field effect transistor source or drain with a multi- facet surface	07/03/2012
US-9620611-B1	MIS contact structure with metal oxide conductor	04/11/2017
US-10147798-B2	MIS contact structure with metal oxide conductor	12/04/2018

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Patent Number	Title	Issue Date
US-10553695-B2	MIS contact structure with metal oxide conductor	02/04/2020
US-10872964-B2	MIS contact structure with metal oxide conductor	12/22/2020
US-11843040-B2	MIS contact structure with metal oxide conductor	12/12/2023

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UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/847,878	**01/10/2025 05:05:05 PM Z ET**	**3771-0003-DC13**

Title of Invention

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	11018237
CONFIRMATION #	8164	FILED BY	SARAH ZIZZO
PATENT CENTER #	68691933	FILING DATE	04/14/2020
CUSTOMER #	27571	FIRST NAMED INVENTOR	Daniel E. Grupp
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Tarek Fahmi

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
16847878_Statement_3-73c.pdf	3	Assignee showing of ownership per 37 CFR 3.73	118 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
16847878_Statement_3-73c.pdf	515A6368B71ADD0D6A6E9CB128DC1FE671A2DA688700E0F9213B538ECF6C8E4FD3B25AE214DAB2BF1DC25E7907E152FAE8899B3C280E45F502DF167FA5F0EFC2

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New International Application Filed with the USPTO as a Receiving Office

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PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: OAK IP, LLC

Application No./Patent No.: 11,018,237 Filed/Issue Date: 05/25/2021

Titled: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

OAK IP, LLC, a company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: GRUPP, DANIEL E.; et al. To: ACORN TECHNOLOGIES, INC.

   The document was recorded in the United States Patent and Trademark Office at Reel 053773, Frame 0225, or for which a copy thereof is attached.

2. From: ACORN TECHNOLOGIES, INC. To: ACORN SEMI, LLC

   The document was recorded in the United States Patent and Trademark Office at Reel 053773, Frame 0306, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: ACORN SEMI, LLC To: OAK IP, LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 069681, Frame 0837, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/	2025-01-10
Signature	Date
Tarek N. Fahmi	41402
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/847,878	04/14/2020	Daniel E. Grupp	3771-0003-DC13

CONFIRMATION NO. 8164

27571
Ascenda Law Group, PC
2150 N First Street
Suite 420
San Jose, CA 95131

POA ACCEPTANCE LETTER

DC00000008343247

Date Mailed: 01/27/2025

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/10/2025.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/atesfai/

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