US011018237B2

(12) **United States Patent**
Grupp et al.

(10) **Patent No.: US 11,018,237 B2**
(45) **Date of Patent: *May 25, 2021**

(54) **METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS**

(71) Applicant: **Acorn Semi, LLC**, Palo Alto, CA (US)

(72) Inventors: **Daniel E. Grupp**, Palo Alto, CA (US); **Daniel J. Connelly**, Redwood City, CA (US)

(73) Assignee: **Acorn Semi, LLC**, Palo Alto, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **16/847,878**

(22) Filed: **Apr. 14, 2020**

(65) **Prior Publication Data**

US 2020/0243662 A1 Jul. 30, 2020

Related U.S. Application Data

(60) Continuation of application No. 16/506,022, filed on Jul. 9, 2019, which is a continuation of application

(Continued)

(51) **Int. Cl.**
H01L 29/45 (2006.01)
H01L 21/285 (2006.01)

(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/456*** (2013.01); ***H01L 21/28537*** (2013.01); ***H01L 29/0895*** (2013.01); ***H01L 29/16*** (2013.01); ***H01L 29/161*** (2013.01); ***H01L 29/1608*** (2013.01); ***H01L 29/45*** (2013.01); ***H01L 29/47*** (2013.01);

(Continued)

(58) **Field of Classification Search**
CPC ... H01L 29/456; H01L 29/0895; H01L 29/16; H01L 29/1608; H01L 29/161; H01L 29/45; H01L 29/47; H01L 29/66143; H01L 29/66643; H01L 29/78; H01L 29/7839; H01L 29/809; H01L 29/812;

(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

2,981,877 A 4/1961 Noyce
3,513,366 A 5/1970 Clark

(Continued)

FOREIGN PATENT DOCUMENTS

EP 0 042 066 A2 12/1981
EP 0 068 897 A2 1/1983

(Continued)

OTHER PUBLICATIONS

Acorn Technologies, Inc., International Application No. PCT/U52012/060893 filed Oct. 18, 2012, ISA/US, International Search Report and Written Opinion, dated Dec. 11, 2012, 23 pages.

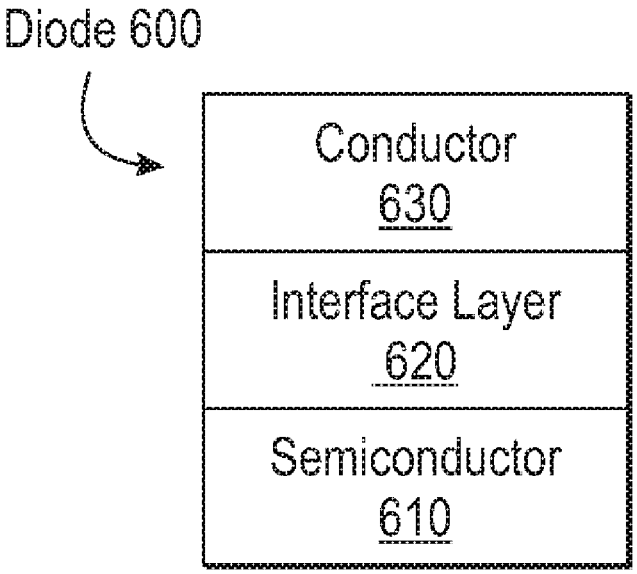
(Continued)

Primary Examiner — Monica D Harrison
(74) *Attorney, Agent, or Firm* — Ascenda Law Group, PC

(57) **ABSTRACT**

An electrical device in which an interface layer is disposed in between and in contact with a conductor and a semiconductor.

12 Claims, 6 Drawing Sheets



Related U.S. Application Data

No. 15/728,002, filed on Oct. 9, 2017, now Pat. No. 10,388,748, which is a continuation of application No. 15/251,210, filed on Aug. 30, 2016, now Pat. No. 9,812,542, which is a continuation of application No. 15/048,877, filed on Feb. 19, 2016, now Pat. No. 9,905,691, which is a continuation of application No. 13/552,556, filed on Jul. 18, 2012, now Pat. No. 9,425,277, which is a continuation of application No. 13/022,522, filed on Feb. 7, 2011, now Pat. No. 8,431,469, which is a division of application No. 12/197,996, filed on Aug. 25, 2008, now Pat. No. 7,884,003, which is a division of application No. 11/181,217, filed on Jul. 13, 2005, now Pat. No. 7,462,860, which is a continuation of application No. 10/217,758, filed on Aug. 12, 2002, now Pat. No. 7,084,423.

(51) **Int. Cl.**

H01L 29/08	(2006.01)
H01L 29/47	(2006.01)
H01L 29/66	(2006.01)
H01L 29/812	(2006.01)
H01L 29/78	(2006.01)
H01L 29/16	(2006.01)
H01L 29/161	(2006.01)
H01L 29/872	(2006.01)
H01L 29/80	(2006.01)

(52) **U.S. Cl.**

CPC .. ***H01L 29/66143*** (2013.01); ***H01L 29/66643*** (2013.01); ***H01L 29/78*** (2013.01); ***H01L 29/7839*** (2013.01); ***H01L 29/806*** (2013.01); ***H01L 29/812*** (2013.01); ***H01L 29/872*** (2013.01); *H01L 29/785* (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/872; H01L 29/785; H01L 21/28; H01L 21/285; H01L 21/2853; H01L 21/28537

USPC 257/763

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,590,471 A 7/1971 Lepselter et al.
3,614,548 A 10/1971 Inoue
3,623,925 A 11/1971 Jenkins et al.
3,708,360 A 1/1973 Wakefield, Jr. et al.
3,719,797 A 3/1973 Andrews, Jr. et al.
3,877,054 A 4/1975 Boulin et al.
3,983,264 A * 9/1976 Schroen H01L 21/28575 257/734
3,983,574 A 9/1976 Statz et al.
4,019,113 A 4/1977 Hartman
4,056,642 A 11/1977 Saxena et al.
4,110,488 A 8/1978 Risko
4,278,830 A 7/1981 Stirn et al.
4,300,152 A 11/1981 Lepselter
4,304,042 A 12/1981 Yeh
4,338,616 A 7/1982 Bol
4,356,622 A 11/1982 Widmann
4,422,090 A 12/1983 Shepherd et al.
4,485,265 A 11/1984 Gordon et al.
4,485,550 A 12/1984 Koeneke et al.
4,538,342 A 9/1985 Camlibel et al.
4,566,021 A 1/1986 Yokoyama
4,583,110 A 4/1986 Jackson et al.
4,689,869 A 9/1987 Jambotkar et al.
4,691,219 A 9/1987 Goth
4,696,828 A 9/1987 Schachter et al.
4,698,652 A 10/1987 Umemoto et al.
4,723,197 A 2/1988 Takiar et al.
4,752,815 A 6/1988 Tsao
4,763,176 A 8/1988 Ito
4,772,934 A 9/1988 Cunningham et al.
4,794,444 A 12/1988 Liu et al.
4,796,082 A 1/1989 Murakami et al.
4,800,415 A 1/1989 Simmons et al.
4,801,984 A 1/1989 Woodall
4,811,077 A 3/1989 Fowler et al.
4,835,580 A 5/1989 Havemann et al.
4,843,029 A 6/1989 Joyce et al.
4,845,050 A 7/1989 Kim et al.
4,960,732 A 10/1990 Dixit et al.
4,961,194 A 10/1990 Kuroda et al.
4,999,685 A 3/1991 Waldrop et al.
5,013,685 A 5/1991 Chiu et al.
5,019,530 A 5/1991 Kleinsasser et al.
5,021,365 A 6/1991 Kirchner et al.
5,021,840 A 6/1991 Morris
5,027,166 A 6/1991 Ohtsuka et al.
5,045,502 A 9/1991 Lau et al.
5,086,321 A 2/1992 Batey et al.
5,093,280 A 3/1992 Tully
5,098,859 A 3/1992 Jackson et al.
5,191,322 A 3/1993 Katayama et al.
5,216,262 A 6/1993 Tsu
5,216,271 A 6/1993 Takagi et al.
5,216,282 A 6/1993 Cote et al.
5,231,306 A 7/1993 Meikle et al.
5,238,872 A 8/1993 Thalapaneni
5,243,213 A 9/1993 Miyazawa et al.
5,292,677 A 3/1994 Dennison
5,294,834 A 3/1994 Fatemi et al.
5,308,998 A 5/1994 Yamazaki et al.
5,355,021 A 10/1994 Crouch et al.
5,358,574 A 10/1994 Sapori
5,399,206 A 3/1995 De Lyon
5,438,210 A 8/1995 Worley
5,442,200 A 8/1995 Tischler
5,480,829 A 1/1996 Abrokwah et al.
5,488,231 A 1/1996 Kwon et al.
5,534,449 A 7/1996 Dennison et al.
5,563,448 A 10/1996 Lee et al.
5,578,848 A 11/1996 Kwong et al.
5,592,736 A 1/1997 Akram et al.
5,596,218 A 1/1997 Soleimani et al.
5,608,266 A 3/1997 Agnello et al.
5,612,567 A 3/1997 Baliga
5,614,745 A 3/1997 Motonami
5,619,057 A 4/1997 Komatsu
5,654,234 A 8/1997 Shih et al.
5,663,584 A 9/1997 Welch
5,677,553 A 10/1997 Yamamoto et al.
5,689,125 A 11/1997 Vaccaro et al.
5,689,130 A 11/1997 Okabe et al.
5,744,817 A 4/1998 Shannon
5,789,312 A 8/1998 Buchanan et al.
5,793,109 A 8/1998 Nakamura
5,793,788 A 8/1998 Inaba et al.
5,801,398 A 9/1998 Hebiguchi
5,801,444 A 9/1998 Aboelfotoh et al.
5,851,912 A 12/1998 Liaw et al.
5,869,364 A 2/1999 Nakano et al.
5,876,796 A 3/1999 Regolini et al.
5,888,891 A 3/1999 Gould
5,897,331 A 4/1999 Sopori
5,903,053 A 5/1999 Iijima et al.
5,908,313 A 6/1999 Chau et al.
5,939,763 A 8/1999 Hao et al.
5,943,575 A 8/1999 Chung et al.
5,962,883 A 10/1999 Hong et al.
5,985,759 A 11/1999 Kim et al.
6,004,879 A 12/1999 Hu et al.
6,011,271 A 1/2000 Sakuma et al.
6,015,997 A 1/2000 Hu et al.
6,017,790 A 1/2000 Liou et al.
6,037,605 A 3/2000 Yoshimura

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,057,564	A	5/2000	Rennie
6,064,082	A	5/2000	Kawai et al.
6,071,783	A	6/2000	Liang et al.
6,091,076	A	7/2000	Deleonibus et al.
6,096,590	A	8/2000	Chan et al.
6,117,781	A	9/2000	Lukanc et al.
6,130,503	A	10/2000	Negishi et al.
6,144,097	A	11/2000	Asahina et al.
6,144,098	A	11/2000	Iyer
6,150,246	A	11/2000	Parsons
6,150,286	A	11/2000	Sun et al.
6,150,672	A	11/2000	Kaneko
6,166,487	A	12/2000	Negishi et al.
6,190,975	B1	2/2001	Kubo et al.
6,198,113	B1	3/2001	Grupp
6,207,976	B1	3/2001	Takahashi et al.
6,222,267	B1	4/2001	Omura et al.
6,225,168	B1	5/2001	Gardner et al.
6,228,732	B1	5/2001	Richardson et al.
6,261,932	B1	7/2001	Hulfachor
6,268,233	B1	7/2001	Sano
6,274,905	B1	8/2001	Mo
6,284,557	B1	9/2001	Yiu et al.
6,287,946	B1	9/2001	Micovic et al.
6,291,282	B1	9/2001	Wilk et al.
6,291,866	B1	9/2001	Wallace et al.
6,291,867	B1	9/2001	Wallace et al.
6,293,137	B1	9/2001	Liu et al.
6,303,479	B1	10/2001	Snyder
6,303,942	B1	10/2001	Farmer, II
6,320,238	B1	11/2001	Kizilyalli et al.
6,323,508	B1	11/2001	Takahashi et al.
6,326,294	B1	12/2001	Jang et al.
6,339,232	B1	1/2002	Takagi
6,344,673	B1	2/2002	Aussilhou
6,346,465	B1	2/2002	Miura et al.
6,350,685	B1	2/2002	Asahina et al.
6,372,536	B1	4/2002	Fischer et al.
6,373,076	B1	4/2002	Alok et al.
6,380,021	B1	4/2002	Wang et al.
6,388,272	B1	5/2002	Odekirk
6,396,191	B1	5/2002	Hagelstein et al.
6,426,542	B1	7/2002	Tan
6,444,516	B1	9/2002	Clevenger et al.
6,451,690	B1	9/2002	Matsumoto et al.
6,452,244	B1	9/2002	Miura et al.
6,462,931	B1	10/2002	Tang et al.
6,468,890	B2	10/2002	Bartsch et al.
6,492,735	B1	10/2002	Matsubara
6,509,254	B1	1/2003	Matsumoto et al.
6,511,905	B1	1/2003	Lee et al.
6,511,910	B2	1/2003	Asahina et al.
6,555,455	B1	1/2003	Wang et al.
6,521,502	B1	2/2003	Yu
6,548,875	B2	4/2003	Nishiyama
6,559,069	B2	5/2003	Goldbach et al.
6,593,219	B2	7/2003	Matsumoto et al.
6,593,229	B1	7/2003	Yamamoto et al.
6,599,644	B1	7/2003	Zekentes et al.
6,605,832	B2	8/2003	Van De Walle
6,608,352	B1	8/2003	Long et al.
6,639,288	B1	10/2003	Kunikiyo
6,680,224	B2	1/2004	Shin et al.
6,724,068	B2	4/2004	Matsuyama
6,724,088	B1	4/2004	Jammy et al.
6,914,272	B2	7/2005	Goetz et al.
6,972,436	B2	12/2005	Das et al.
6,979,846	B2	12/2005	Yagishita et al.
6,995,430	B2	2/2006	Langdo et al.
7,057,333	B1	6/2006	Vu Thien et al.
7,084,423	B2	8/2006	Grupp et al.
7,176,483	B2	2/2007	Grupp et al.
7,579,231	B2	8/2009	Matsuo et al.
7,863,606	B2	1/2011	Sung
8,110,877	B2	2/2012	Mukherjee et al.
8,952,541	B2	2/2015	Mukherjee et al.
9,209,261	B2	12/2015	Grupp et al.
9,425,277	B2	8/2016	Grupp et al.
9,461,167	B2	10/2016	Grupp et al.
9,905,691	B2	2/2018	Grupp et al.
10,090,395	B2	10/2018	Grupp et al.
10,388,748	B2 *	8/2019	Grupp H01L 29/7839
2001/0028067	A1	10/2001	Awano
2001/0030342	A1	10/2001	Ohnishi et al.
2001/0030352	A1	10/2001	Ruf et al.
2002/0017658	A1	2/2002	Tsubouchi et al.
2002/0061646	A1	5/2002	Kan et al.
2002/0098692	A1	7/2002	Miura
2002/0106536	A1	8/2002	Lee et al.
2002/0158250	A1	10/2002	Fujisaki et al.
2002/0163012	A1	11/2002	Nihei et al.
2002/0175386	A1	11/2002	Kim et al.
2002/0179980	A1	12/2002	Yagishita et al.
2002/0179993	A1	12/2002	Hshieh et al.
2003/0009463	A1	1/2003	Gallant
2003/0012146	A1	1/2003	Novaes
2003/0015707	A1	1/2003	Bosco et al.
2003/0020069	A1	1/2003	Holmes et al.
2003/0020165	A1	1/2003	Matsumoto
2003/0022474	A1	1/2003	Grover et al.
2003/0098489	A1	5/2003	Amos et al.
2003/0109114	A1	6/2003	Niwa
2003/0121468	A1	7/2003	Boone et al.
2003/0127700	A1	7/2003	Moddel et al.
2003/0132452	A1	7/2003	Boriuchi
2003/0132466	A1	7/2003	Shin et al.
2003/0193074	A1	10/2003	Hshieh et al.
2003/0219965	A1	11/2003	Cabral et al.
2003/0235936	A1	12/2003	Snyder et al.
2004/0026687	A1	2/2004	Grupp et al.
2004/0038467	A1	2/2004	Darwish et al.
2004/0093575	A1	5/2004	Heath et al.
2004/0129087	A1	7/2004	Rowe et al.
2004/0142524	A1	7/2004	Grupp et al.
2004/1029087		7/2004	Rowe et al.
2004/0159865	A1	8/2004	Allen et al.
2005/0009302	A1	1/2005	Wakui et al.
2005/0037557	A1	2/2005	Doczy et al.
2005/0093027	A1	5/2005	Grupp et al.
2006/0178015	A1	8/2006	Verhaverbeke
2011/0092047	A1	4/2011	Gaines et al.
2012/0181632	A1	7/2012	Watanabe et al.
2014/0117465	A1	5/2014	Huang et al.

FOREIGN PATENT DOCUMENTS

EP	0 111 364	A2	6/1984
EP	0 168 125	A1	1/1986
EP	0295490	A1	12/1988
EP	0 458 353	B1	11/1991
EP	0 789 388	A2	8/1997
EP	0789388	A2	8/1997
FR	2 814 856	A1	4/2002
GB	1 22 594	A	1/1919
JP	S61-133646	A	6/1986
JP	S62-61363	A	3/1987
JP	S63-157466	A	6/1988
JP	S63-175471	A	7/1988
JP	H01-186672	A	7/1989
JP	H02-26073	A	1/1990
JP	H03-29355	A	2/1991
JP	H03-191518	A	8/1991
JP	H03-274735	A	12/1991
JP	H04-199628	A	7/1992
JP	H04-284668	A	10/1992
JP	H06-5737	B2	1/1994
JP	H06-53165	A	2/1994
JP	H06-61177	A	3/1994
JP	H07-122519	A	5/1995
JP	H07-263375	A	10/1995
JP	H08-64800	A	3/1996
JP	H08-167693	A	6/1996
JP	2630279	B2	7/1997
JP	H09-289178	A	11/1997

(56) **References Cited**

FOREIGN PATENT DOCUMENTS

JP	H10-27847	A	1/1998
JP	H10-74707	A	3/1998
JP	H10-135452	A	5/1998
JP	H10-209445	A	8/1998
JP	H10-335265	A	12/1998
JP	H11-26713	A	1/1999
JP	H11-162874	A	6/1999
JP	H11-233760	A	8/1999
JP	H11-330482	A	11/1999
JP	2000-101064	A	4/2000
JP	2000-101100	A	4/2000
JP	2000-174261	A	6/2000
JP	2000-195954	A	7/2000
JP	2000-216241	A	8/2000
JP	2000-228523	A	8/2000
JP	2000-236086	A	8/2000
JP	2000-299479	A	10/2000
JP	3191728	B2	7/2001
JP	2001-223180	A	8/2001
JP	3208599	B2	9/2001
JP	2002-075909	A	3/2002
JP	2002-093742	A	3/2002
JP	2002-151428	A	5/2002
JP	2002-184978	A	6/2002
JP	2002-217425	A	8/2002
KR	1991-0006249	B1	8/1991
KR	92-002350	B1	3/1992
KR	1992-0010131	B1	11/1992
KR	1994-0020550	A	9/1994
KR	1995-0010873	B1	9/1995
KR	1997-0030333	A	6/1997
KR	1998-0024649	A	7/1998
KR	1999-0025041	A	4/1999
KR	10-0197653	B1	6/1999
KR	1999-0045323	A	6/1999
KR	2000-0025576	A	5/2000
KR	2000-0027908	A	5/2000
KR	10-0290467	B1	3/2001
SE	0875077	T3	1/2004
WO	WO 88/00392	A1	1/1988
WO	WO 93/11558	A1	6/1993
WO	WO 95/34095	A1	12/1995
WO	WO 97/26678	A2	7/1997
WO	WO 97/33308	A1	9/1997
WO	WO 01/28677	A1	4/2001
WO	WO 01/63677	A1	8/2001
WO	WO 2002/043109	A2	5/2002
WO	WO 2004/015782	A1	2/2004
WO	WO 2004/030104	A1	4/2004

OTHER PUBLICATIONS

"Patents Act 1977: Examination Report under Section 18(3)", UK Intellectual Property Office dated Apr. 29, 2015, Application No. GB1409999.8 (filed Oct. 18, 2012), 5 pgs.

"Research Achievements", Research Achievements at RCIQE, downloaded Apr. 12, 2002, from: http://www.rciqe.hokudai.ac.jp/RCIQEold/ResearchAchievements.html, 8 pgs.

Aberle, Armin G., et al., "Injection-Level Dependent Surface Recombination Velocities at the Silicon-Plasma Silicon Nitrite Interface", Institute fur Solarenergieforschung, ISFH, D-3 1860 Emmerthal, Germany, (Mar. 9, 1995), pp. 2828-2830.

"International Search Report and Written Opinion of the International Searching Authority", Patent Cooperation Treaty (dated Mar. 2, 2006), PCT/US2005/030209, 6 pgs.

"International Search Report", Patent Cooperation Treaty (dated Dec. 18, 2003), PCT/US03/25057, 4 pgs.

Adam; et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", Applied Physics Letters (Jul. 2001), 79(5):623-625.

Alers; et al., "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates", MRS Proceedings (1999), 567:391-395.

Almeida; et al., "Reaction-Diffusion Model for Thermal Growth of Silicon Nitrite Films on Si", Physical Review B (Dec. 2000), 62(24):R16255-R16258.

Aboelfotoh, "Influence of thin interfacial silicon oxide layers on the Schottky-barrier behavior of Ti on Si(100)", Phys Rev B Condens Matter (Mar. 1989), 39(8):5070-5078.

Bauernschmitt, et al., "Transition from MOS to Schottky-contract behaviour in Yb—SiO2—Si Tunneling Junctions with extremely thin SiO2 layer", Microelectronic Engineering (1993), 22:105-108.

Baumvol, "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon", Surface Science Reports (Dec. 1999), 36(1-8):1-166.

Berger, "Contact Resistance and Contact Resistivity" J. Electrochem. Soc.: Solid-State Science and Technology (1972), 119(4):507-514.

Bannikov; et al., "Field-Effect Transistor With Metal-(Tunneling-Insulator)-Semiconductor Contacts and a Gate Insulator Made of a Mangmuir-Blodgett Film", Soviet Technical Physics Letters (Mar. 1989), 15(3):211-212.

Bringans, "Arsenic Passivation of Si and Ge Surfaces", Critical Reviews in Solid State and Materials Sciences I(1992), 17(4):353-395.

Cai; et al., "Investigation of the Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitrite and its Effect on Silicon Surface Passivation", Journal of Applied Physics (May 1998), 83(11):5885-5889.

Blosse; et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", IEEE, Transactions of 2004 International Electron Device Meeting (Jan. 2005), pp. 669-672.

Chadi; et al., "Fermi-Level-Pinning Defects in Highly n-Doped Silicon", Physical Review Letters (Dec. 1997), 79(24):4834-4837.

Card; et al., "Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes", Journal of Physics D: Applied Physics (1971), 4(10):1589-1601.

Chen; et al., "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment", Electronic Letters, (May 2000), 36(11):981-983.

Chaneliere; et al., "Tantalum Pentoxide (Ta2O5) Thin Films for Advanced Dielectric Applications"; Materials Science and Engineering, R: Reports (May 1998), 22(6):269-322.

Connelly; et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate CMOS Performance", Electron Device Letters, IEEE (Jun. 2003), 24(6)411-413.

Gilmer; et al., "Process and Manufacturing Challenges for High-K Gate Stack Systems", MRS Proceedings, MRS Spring Meeting (1999), 567:323-341.

Edelstein; et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", Proceedings of the IEEE International Electron Device Meeting (1997), pp. 773-776.

Hara, et al., "Control of Schottky and Ohmic Interfaces by Unpinning Fermi Level", Applied Surface Science (1997), 117-118:394-399.

Hara; et al., "Pinning-Controlled Metal/Semiconductor Interfaces", Proc. SPIE 2779, 3rd International Conference on Intelligent Materials and 3rd European Conference on Smart Structures and Materials (Apr. 1996), 2779:802-807.

Hara; et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001)", Applied Surface Science (Nov. 1996), 107:218-221.

Hasegawa; et al., "Unpinning of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP", Applied Surface Science (2000): 166:92-96.

Gopalakrishnan; et al., "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit Simulations", IEEE Transactions Electron Devices (Jan. 2005), 52(1):69-76.

Heine, "Theory of Surface States", Physical Review (Jun. 1965), 138(6A):83-4.

Hilsenbeck; et al., "Aging Behavior of Algan HFETs With Advanced Ohmic and Schottky Contacts", Electronic letters (May 2000), 38(11):980-981.

Huang, "Metal-Oxide Semiconductor Field-Effect Transistors Using Schottky Barrier Drains", Electronics Letters (1797), 33(15):1341-1342.

(56) **References Cited**

OTHER PUBLICATIONS

Huang; et al., "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nn", IEEE (Apr. 1998), pp. 842-848.
Hayafuji; et al., "Nitridation of Silicon and Oxidized-Silicon", J. Electrochem. Soc. (1982), 129(9):2102-2108.
International Search Report, PCT/US2004/042084, dated Sep. 1, 2005, 4 pgs.
Izumi, "43 Hydrogen Termination: The Ideally Finished Silicon Surface", Ultraclean Surface Processing of Silicon Wafers (1998), pp. 559-565.
Kamins; et al., "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements", Electrochemical and Solid-State Letters (1998), 1(2):100-101.
Kamiyama; et al., "Ultrathin Tantalum Odise Capacitor DIELECTRIC Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition", J. Electrochem Soc. (1993), 140(6)1617.
Kaxiras, "Efthimios. Semiconductor-surface restoration by valence-mending adsorbates: Application to Si (100): S and Si (100): Se", Phys Rev B Condens Matter (Mar. 1991), 43(18):6824-6827.
Kedzierski; et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", IEEE Trans. Electron Devices (Apr. 2003), 50(4):952-958.
Keller; et al., "Calculations of the barrier height and charge distribution of a metal-dielectric interface", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (Jul. 1992), 10(4):775-780.
Kim; et al., "Metal-Dependent Fermi-Level Movement in the Metal/Sulfer-Passivated InGaP Contact", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (1997), 15(3):1124-1128.
Kimura; et al., "A New Type of Schottky Tunnel Transistor", IEEE Electron Device Letters (Oct. 1994), 15(10): 412-414.
Lee; et al., "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications for Nanoelectronic Device Applications", Journal of Nanoparticle Research (Dec. 2000), 2(4):345-362.
Louie; et al., "Ionicity and the Theory of Schottky Barriers", Physical Review B (Feb. 1977), 15(4):2154-2162.
Mandelis; et al., "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999), 8:13-17.
Martel; et al., "Ambipolar Single-Wall Carbon Nanotube Transistors and Inverters", AIP Conference Proceedings (Mar. 2001). 591:543-547.
McKee; et al., "Physical Structure and Inversion Charge at a Semiconductor Interface With a Crystalline Oxide", Science (Jul. 2001), 293(5529):468-471.
McKinley; et al., "Control of Ge homojunction band offsets via ultrathin Ga—As dipole layers", Applied Surface Science (1992), 56-58(Part 2):762-765.
McKinley; et al., "Controlled modification of heterojunction band lineups by diffusive intralayers", Journal of Vacuum Science & Technology A Vacuum Surfaces and Films (May/Jun 1990), 8(3):1917-21.
Miyawaki; et al., "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing", IEEE Electron Device Letters (Oct. 1990), 11(10):448-450.
Nauka; et al., "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces", Journal of Electrochemical Society (1999), 146(1):292-295.
Nishioka; et al., "Dielectric Characteristics of Fluorinated Ultradry SiO2", Appl. Phy. Letters (Mar. 1989), 54(12):1127-1129.
Okamoto; et al., "Near-Ohmic Contact of n—GaAs with GaS/GaAs Quaisi-Metal-Insulator-Semiconductor Structure", Jpn. J. Appl. Phys. (1998), 37:3248-3251.
Padovani, "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers", Journal of Applied Physics (1967), 38(2):891-892.
Park; et al., "Thermal stability of molybdenum-silicon nitride-silicon Schottky diodes", Journal of Applied Physics (Mar. 1991), 69(5):3149-3153.
Patel; et al., "Arsenic Atom Location on Passive Silicon (111) Surfaces", Physical Review B (Nov. 1987), 36(14):7715-17.
Porter; et al., "A Critical Review of Ohmic and Rectifying Contacts for Silicon Carbide", Material Science and Engineering: B (Nov. 1995), 34(2-3):83-105.
Ren; et al. "Metal I Silicon Schottky Barrier Lowering by RTCVD Interface Passivation" Electrochemical Society Proceedings (2000), 2000-9:161-166.
Ruzyllo; et al., "Semiconductor Glossary An Introduction to Semiconductor Terminology", Prosto Multimedia Publishing (2004), pp. 26.
Schmidt; et al., "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition", Journal of Applied Physics (Apr. 1999), 85(7):3626-3633.
Shalish; et al., "Yellow Luminescence and Fermi Level Pinning in GaN Layers", Appl Phys Lett (Aug. 2000), 77(7):987-989.
Snyder; et al., "Experimental Investigation of a PtSi Source and Drain Field Emission Transister", Appl Phys Lett (1995), 67:1420-1422.
Sobolewski; et al., "Properties of Ultrathin Thermal Nitrides in Silicon Schottky Barrier Structures", Applied Physics Letters, American Institute of Physics (1989), 54(7):638-640.
Sobolewski; et al., "Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes", Journal of Vacuum Science & Technology B (1989), 7:971-979.
Spicer; et al., "Unified Mechanism for Schottky-Barrier Formation and III-V Oxide Interface States", Physical Review Letters (Feb. 1980), 44(6):420-423.
Sze, "Metal-Semiconductor Contacts", Physics of Semiconductor Devices, John Wiley & Sons, (1981), pp. 245-311.
Takahagi; et al., "The formation of hydrogen passivated silicon singlecrystal surfaces using ultraviolet cleaning and HF etching", J Appl Phys (1988), 64(7):3516-21.
Tao; et al., "Removal of dangling bonds and surface states on silicon (001) with a monolayer of selenium", Applied Physics Letters (Mar. 2003), 82(10)1559-1561.
Tao; et al., "Suppression of silicon (001) surface reactivity using a valence-mending technique", Solid State Communications (Oct. 2004), 132(2):89-92.
Taubenblatt; et al., "Interface effects in titanium and hafnium Schottky barriers on silicon", Appl Phys Lett (May 1984), 44:895-897.
Teraji; et al., "Ohmic Contacts to n-Type 6H—SiC Without Post-Annealing", Material Research Society, MRS Spring Meeting (1996), 423:149-154.
Tersoff, "Schottky Barrier Heightsand the Continuum of Gap States", Physical Review Letters (Feb. 1984), 52(6):465-468.
Thanailakis; et al., "Transition-metal contacts to atomically clean silicon, Department of Electrical Engineering and Electronics", Journal of Physics C: Solid State Physics (1976), 9:337-343.
Thompson; et al., "A Logic Nanotechnology Featuring Strained-Silicon", IEEE Electron Device Letters (Apr. 2004),25(4):191-193.
Tung, "Electron Transport of Inhomogeneous Schottky Barriers", Appl Phys Letter (1991), 58(24):2821-2823.
Udeshi; et al., "Thermal stability of ohmic contacts between Ti and Sepassivated n-type Si(001)", J Appl Phys (2004), 95(8):4219-4222.
Uemoto, "Reduction of Ohmic Contact Resistance on N-Type 6H—SIC by Heavy Doping", Japanese Journal of Applied Physics (Jan. 1995), 34(Parts 2, No. 1A).
Verhaverbeke; et al., "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides", MRS Proceedings (1992), 259:391-399.
Wang; et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", Appl. Phys. Letters (Feb. 1996), 68(9):1267-1270.

(56) **References Cited**

OTHER PUBLICATIONS

Wei; et al., "The Use of Selective Electroless Metal Deposition for Micron Size Contact Fill", IEEE International Electron Device Meeting Technical Digest (1988), pp. 446-449.
Weinberger; et al., "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron and Ion Scattering Spectroscopy Results", J. Appl. Phys (Nov. 1986), 60(9):3232-34.
Widjaja; et al., "Ab Initlo Study and Decomposition of NH3 on Si(100)–(2×1)", J. Phy. Chem B, (2000), 104:2527-2533.
Wittmer; et al., "Ideal Schottky diodes on passivated silicon", Phys Rev Lett (Nov. 1992), 69(18):2701-2704.
Wolf; et al., "Spintronics: A Spin-Based Vision for the Future", Science (Nov. 2001), 294(5546):1488-95.
Wright; et al., "Hot-Electron Immunity of SiO2 Dielectrics with Fluorine Incorporation", IEEE Electron Device Letters (1989), 10(8):347-348.
Yablonovitch; et al., "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces", Physical Review Letters (Jul. 1986), 57(2):249-252.
Yagishita; et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 mm Regime", IEEE Trans. Electron Devices (2000), 47(5):1028-1034.
Yang; et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", IEEE Electron Device Letters (2000), 21(2):76-78.
Zhang; et al., "Schottky diodes of NiÕAu on n-GaN grown on sapphire and SiC substrates", Applied Physics Letters (Oct. 2001), 79(16):2567-69.
Zhu; et al., "Low-Resistance Ti/n-Type Si(100) Contacts by Monolayer Se Passivation", ECS Trans (2006), 2(2):401-409.
Zhu; et al., "Stability of Se passivation layers on Si(001) surfaces characterized by time-of-flight positron annihilation induced Auger electron spectroscopy", Journal of Applied Physics (2005), 97(10):103510-1103510-4.
Archibong, et al., On the Structure of A12O3 and Photoelectron Spectra of A12O2 and A12O3; J. Phys. Chem.A 1999, 103, pp. 1109-1114.
Bortz, et al., Temperature Dependence of the Electronic Structure of Oxides: MgO, MgAl2O4 and Al2O3; Physica Scripta., col. 41, pp. 537-541, 1990.
Carver, et al., Specific Contact Resistivity of Metal-Semiconductor Contacts—A New, Accurate Method Linked to Spreading Resistance; IEEE Transactions on Electron Devices, vol. 35, No. 4, Apr. 1988, pp. 489-497.
Lide, David R., CRC Handbook of Chemistry and Physics, Internet Version 2005; <http://www.hbcpnetbase.com>, CRC Press, Boca Raton, FL, 2005; 11 pp.
Distefano, et al., The Band Edge of Amorphous SiO2 by Photoinjection and Photoconductivity Measurements; Solid State Communications, vol. 9, pp. 2259-2261, 1971, Pergamon Press; Printed in Great Britain.
Fitting, et al., Monte-Carlo Approach of Electron Emission from SiO2; Phys. Stat. Sol. (a) 81, 323 (1984) pp. 323-332.
IPR2020-01182; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jun. 23, 2020; 139 pp.
IPR2020-01182; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 7,084,423; Jun. 24, 2020; 76 pp.
IPR2020-01183; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jun. 24, 2020; 178 pp.
IPR2020-01183; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 9,209,261; Jun. 24, 2020; 81 pp.
IPR2020-01204; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jun. 29, 2020; 178 pp.
IPR2020-01204; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 8,766,336; Jun. 29, 2020; 78 pp.
IPR2020-01205; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*;; Declaration of Dr. E. Fred Schubert; Jun. 29, 2020; 142 pp.
IPR2020-01205; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 9,461,167; Jun. 29, 2020; 63 pp.
IPR2020-01206; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jun. 29, 2020; 164 pp.
IPR2020-01206; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 9,905,691; Jun. 29, 2020; 76 pp.
IPR2020-01207; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jun. 29, 2020; 146 pp.
IPR2020-01207; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 10,090,395; Jun. 29, 2020; 66 pp.
IPR2020-01241; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jul. 6, 2020; 165 pp.
IPR2020-01241; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 9,461,167; Jul. 6, 2020; 84 pp.
IPR2020-01264; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jul. 8, 2020; 194 pp.
IPR2020-01264; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 8,766,336; Jul. 8, 2020; 83 pp.
IPR2020-01279; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jul. 9, 2020; 182 pp.
IPR2020-01279; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 9,905,691; Jul. 10, 2020; 84 pp.
IPR2020-01282; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Declaration of Dr. E. Fred Schubert; Jul. 12, 2020; 217 pp.
IPR2020-01282; *Samsung Electronics Co., Ltd.* v. *Acorn Semi, LLC*; Petition for Inter Partes Review of U.S. Pat. No. 10,090,395; Jul. 13, 2020; 85 pp.
Lang et al., Theory of Metal Surfaces: Work Functon *; Physical Review B, vol. 3, No. 4; Feb. 15, 1971; pp. 1215-1223.
Rohatgi et al., Comprehensive Study of Rapid, Low-Cost Silicon Surface Passivation Technologies; IEEE Transactions on Electron Devices, vol. 47, No. 5, May 2000; pp. 987-993.
Sakurai, et al., Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas; IEEE Journal of Solid-State Circuits, Vo. 25, No. 2, Apr. 1990, pp. 584-594.
Simmons, John G., Generalized Formula for the Electric Tunnel Effect Between Similar Electrodes Separated by a Thin Insulating Film; Journal of Applied Physics, vol. 34, No. 6, Jun. 1963; pp. 1793-1803.
Stesmans et al., Si Dangling-Bond-Type Defects at the Interface of (100)Si with Ultrathin Layers of SiOx, Al2O3, and ZrO2; Applied Physics Letters, vol. 80, No. 11, Mar. 18, 2002; pp. 1957-1959.
Szydlo, et al., I—V and C—V Characteristics of Au/TiO2 Schottky Diodes; J. Appl. Phys. 51(6), Jun. 1980; pp. 3310-3312.
Zheng et al., Electronic Structure Differences in ZeO2 vs 1-HfO2; J. Phys. Chem. A 2005, 109, pp. 11521-11525.
Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 79 pgs.
Appendix A1., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 5 pgs.
Appendix A2., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 7 pgs.
Appendix A3., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 19 pgs.

(56) **References Cited**

OTHER PUBLICATIONS

Appendix A4., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 21 pgs.
Appendix A6., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 15 pgs.
Appendix A7., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 26 pgs.
Appendix A8., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 28 pgs.
Appendix A10., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 18 pgs.
Appendix B1., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 41 pgs.
Appendix B2., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 43 pgs.
Appendix B3., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 48 pgs.
Appendix B4., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 48 pgs.
Appendix B5., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 47 pgs.
Appendix B6., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 32 pgs.
Appendix B7., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 42 pgs.
Appendix B8., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 41 pgs.
Appendix B10., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 30 pgs.
Appendix C1., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 5 pgs.
Appendix C2., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 5 pgs.
Appendix C3., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 7 pgs.
Appendix C4., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 9 pgs.
Appendix C5., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 9 pgs.
Appendix C6., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix C7., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 9 pgs.
Appendix C8., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 9 pgs.
Appendix C10., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 4 pgs.
Appendix D1., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 16 pgs.
Appendix D2., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 20 pgs.
Appendix D3., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 14 pgs.
Appendix D4., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 11 pgs.
Appendix D5., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 16 pgs.

(56) **References Cited**

OTHER PUBLICATIONS

Appendix D6., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 12 pgs.
Appendix D7., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 22 pgs.
Appendix D8., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 15 pgs.
Appendix D10., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 21 pgs.
Appendix E1., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix E2., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix E3., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix E4., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix E5., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix E6., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix E7., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix E8., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix E10., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 8 pgs.
Appendix F1., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 13 pgs.
Appendix F2., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 15 pgs.
Appendix F3., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 11 pgs.
Appendix F4., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 15 pgs.
Appendix F5., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 9 pgs.
Appendix F6., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 9 pgs.
Appendix F7., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 17 pgs.
Appendix F8., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 17 pgs.
Appendix F10., Claim Chart, from Defendants' Preliminary Invalidity Contentions and Additional Disclosures Pursuant to Patent Local Rules dated May 19, 2020, *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd; et al.*, Civil Action No. 2:19-cv-347-JRG, 11 pgs.
De Bosscher, et al., The influence of silicide formation on the barrier height of Ti/Si MIS Schottky barriers, Semiconductor Sci., Tech., vol. 1, 1986, pp. 376-382.
Defives, et al., Electrical behaviour and microstructural analysis of metal Schottky contacts on 4H—SiC, Microelec. Eng'g, vol. 55, 2001, pp. 369-374.
Goodnick, et al., Effects of a thin SiO2 layer on the formation of metal-silicon contacts, Journal of Vacuum Sci. & Tech., vol. 18, No. 3, Apr. 1981, pp. 949-954.
Schmidt, et al., Increased dependence of Schottky barrier height on metal work functions due to a thin-oxide layer, Journal of Vacuum Sci. & Tech., vol. 6, No. 4, Jul./Aug. 1988, pp. 1436-1439.
Waldrop, et al., Schottky barrier height and interface chemistry of annealed metal contacts to alpha 6H—SiC: Crystal face dependence, Applied Physics Letters, vol. 62, No. 21, May 24, 1993, pp. 2685-2687.
Aboelfotoh, Schottky Barrier Heights of Refractory Metals on Silicon, Materials Research Soc., vol. 71, 1986, pp. 273-285.
Aboelfotoh, et al., Schottky-barrier heights of Ti and TiSi2 on n-type and p-type Si(100), Physical Review B, vol. 34, No. 4, Aug. 15, 1986, pp. 2311-2317.
Aboelfotoh, et al., Schottky-barrier height of a Ti—W alloy on n-type and p-type Si, Physical Review B, vol. 33, No. 10, May 15, 1986, pp. 6572-6578.
Aboelfotoh, Temperature Dependence of the Schottky-Barrier Height of Tungsten on n-Type and p-Type Silicon, Solid-State Elecs, vol. 34, No. 1, 1991, pp. 51-55.
Asamizu, et al., Formation Mechanism of Low Contact Resistance PdZn-Based Ohmic Contacts for p-type InP, Materials Transactions, vol. 43, No. 6, 2002, pp. 1352-1359.
Bard, et al., The Concept of Fermi Level Pinning at Semiconductor/Liquid Junctions, Consequences for Energy Conversion Efficiency and Selection of Useful Solution Redox Couples in Solar Devices, Journal of the Am. Chem. Soc., vol. 12, No. 11, May 21, 1980, pp. 3671-3677.
Beatty, Metallization Systems for Integrated Circuits, NASA Technical Note D-5866, Jul. 1970., 26 pgs.
Boswell, Low Resistance Gold Contacts for Gallium Nitride, Gold Bulletin, vol. 31, No. 4, 1998, pp. 132-133.

(56) **References Cited**

OTHER PUBLICATIONS

Calvet, Electrical Transport in Schottky Barrier MOSFETS, Dissertation, Yale Univ., May 2001, 183 pgs.
Campbell, et al., Titanium dioxide (TiO2)-based gate insulators, IBM Journal of Research Development, vol. 43, No. 3, May 1999, pp. 383-392.
Card, et al., Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes, Journal of Applied. Physics, vol. 4, Jun. 1971, pp. 1589-1601.
Chang, et al., Specific Contact Resistance of Metal-Semiconductor Barriers, Solid-State Elecs., vol. 14, 1971, pp. 541-550.
Cheek, et al., MIS and SIS Silicon Solar Cells: A Review, Photovoltaic Solar Energy Conf., 1981, pp. 353-357.
Chen, et al., Band structure of Al/Si/n-type GaAs with a strained Si interfacial layer, Physical Review B, vol. 52, No. 7, Feb. 15, 1996, pp. 3879-3884.
Chen, et al., Properties of TiO2—GaAs Interface, Final Report on NASA Grant No. NSG 1202-S1, Jun. 1977, 100 pgs.
Chen, et al., The Use of Refractory Metal and Electron-Beam Sintering to Reduce Contact Resistance for VLSI, IEEE Trans. on Electron Devices, vol. ED-30, No. 11, Nov. 1983, pp. 1542-1550.
Chourasia, et al., X-ray photoelectron study of TiN/Si02 and TiN/Si interfaces, Thin Solid Films, vol. 266, 1995, pp. 298-301.
Claflin, et al., Interface formation and thermal stability of advanced metal gate and ultrathin gate dielectric layers, Journal of Vacuum Sci., & Tech., vol. 16, No. 4, Jul./Aug. 1998, pp. 2154-2158.
Claflin, et al., Interface studies of tungsten nitride and titanium nitride composite metal gate electrodes with within dielectric layers, Journal of Vacuum Sci., & Tech., vol. 16, No. 3, May/Jun. 1998, pp. 1757-1761.
Clarke, et al., Non-Equilibrium Effects on Metal-Oxide-Semiconductor Tunnel Currents, Solid-State Elecs., vol. 14, 1971, pp. 957-973.
Cohen, et al., Chapter 6: Practical Ohmic Contacts to Silicon, VLSI Electronics Microstructure Sci., vol. 13, 1986, pp. 213-310.
Connelly, et al., Speed Advantage of Optimized Metal S/D in 25 nm Dual-Gate Fully-Depleted CMOS, 60th DRC Conf. Digest Device Research Conf., 2002, pp. 1-2.
Costa, et al., Unpinned GaAs Schottky barriers with an epitaxial silicon layer, Journal of Applied Physics, vol. 70, No. 4, Aug. 15, 1991. pp. 2173-2184.
Cowley, Titanium-Silicon Schottky Barrier Diodes, Solid-State Elecs., vol. 12, 1970, pp. 403-414.
Davis, et al., Low Temperature Deposition and Characterization of N- and P-Type Silicon Carbide Thin Films and Associated Ohmic and Schottky Contacts, Semiannual Technical Report, Jun. 1995, 32 pgs.
Depas, et al., Electrical Characteristics of Al/SiO2/n—Si Tunnel Diodes with an Oxide Layer Grown by Rapid Thermal Oxidation, Solid-State Elecs., vol. 37, No. 3, 1994, pp. 433-441.
D'Heurle, Interfaces in Silicides, Journal de Physique IV Colloque, vol. 6, Mar. 1996, pp. C2-29-C2-46.
D'Heurle, Silicide interfaces in silicon technology, Journal of Elec. Materials, vol. 27, No. 11, Nov. 1998, 16 pgs.
Dubois, et al., Low Schottky barrier source/drain for advanced MOS architecture: device design and material considerations, Solid-State Elecs., vol. 46, 2002, pp. 997-1004.
EMC Corp., 2002 EMC At-a-Glance: EMC Plenary Lecture/Student Awards, 2002 Elec. Materials Conf., Jun. 26, 2002, 107 pgs.
Eun, et al., High Temperature Ohmic Contact Technology to N-Type GaAs, ECE Technical Reports, Purdue Univ., Jan. 1993, 113 pgs.
Fan, et al., Very low resistance multilayer Ohmic contact to n—GaN, Applied Physics Letters, vol. 68, No. 12, Mar. 18, 1996, pp. 1672-1674.
Franciosi, et al., Heterojunction band offset engineering, Surface Sci. Reports, vol. 25, 1996, pp. 1-140.
Frangoul, et al., The Fabrication of Metal-Oxide Semiconductor Transistors Using Cerium Dioxide as a Gate Oxide Material, Journal of Vacuum Sci. & Tech, vol. 9, No. 1, Jan./Feb. 1991, pp. 181-183.
Fulton, et al., Electronic states at the interface of Ti—Si oxide on Si(100), Journal of Vacuum Sci. & Tech., vol. 20, No. 4, Jul./Aug. 2002, pp. 1726-1731.
Gessmann, et al., Ohmic contact technology in III nitrides using polarization effects of cap layers, Journal of Applied Physics, vol. 92, No. 7, Oct. 1, 2002, pp. 3740-3744.
Getto, et al., Characterization of sputtered titanium silicide ohmic contacts on n-type 6H-silicon carbide, Materials Sci. and Eng'g B61-62, 1999, pp. 270-274.
Giboney, Travelling-Wave Photodetectors, Thesis, Univ. of Calif. at Santa Barbara, Aug. 1995, 170 pgs.
Glass, et al., Low energy ion-assisted deposition of titanium nitride ohmic contacts on alpha (6H)-silicon carbide, Applied Physics Letters, vol. 59, No. 22, Nov. 25, 1991, pp. 2868-2870.
Gordon, 5—Depositions and Reactions of Metals and Metal Compounds, Harvard Univ., pp. 171-196.
Green, et al., Current Multiplication in Metal-Insulator-Semiconductor (MIS) Tunnel Diodes, Solid-State Elecs., vol. 17, 1974, pp. 349-365.
Green, et al., Minority Carrier MIS Tunnel Diodes and Their Application to Electron- and Photo-Voltaic Energy Conversion-I. Theory, Solid-State Elecs., vol. 17, 1974, pp. 551-561.
Grove, et al., Investigation of Thermally Oxidised Silicon Surfaces Using Metal-Oxide-Semiconductor Structures, Solid-State Elecs., vol. 8, 1965, pp. 145-163.
Guo, et al., High Quality Ultra-thin (1.5 nm) TiO2/Si3N4 Gate Dielectric for Deep Sub-micron CMOS Technology, IEEE, 1999, pp. 137-140.
Guo, et al., High Temperature Lifetesting of Silicon Metal-Thin Insulator-Semiconductor Heterojunction Emitter Bipolar Transistors, Solid-State Elecs., vol. 31, No. 6, 1998, pp. 1071-1075.
Hara, Characterization of the 6H—SiC(0001) surface and the interface with Ti layer with the Schottky limit, Applied Surface Sci., vol. 162-163, 2000, pp. 19-24.
Hara, et al., New Technique for Ohmic Formation, Materials Research Soc., vol. 427, 1996, pp. 159-164.
Hartstein, et al., Determination of the inversion-layer thickness from capacitance measurements of metal-oxide-semiconductor field-effect transistors with ultrathin oxide layers, Physical Review B, vol. 38, No. 2, Jul. 15, 1988, pp. 1235-1240.
Hasegawa, et al., Control of compound semiconductor-insulator interfaces by an ultrathin molecular-beam epitaxy Si layer, Journal of Vacuum Sci. & Tech., Vo. 7, No. 4, 1989, pp. 870-878.
Hasegawa, et al., Control of Structure and Properties of Compound Semiconductor Interfaces by Si Interface Control Layer, 1993 (5th) Int'l Conf. on Indium Phosphide & Related Materials, 1993, pp. 289-292.
Hasegawa, et al., Correlation Between Atomic-Scale Structures and Macroscopic Electrical Properties of Metal-Covered Si(111) Surfaces, Int'l Journal of Modern Physics B, vol. 7, No. 22, 1993, pp. 3817-3876.
Hasegawa, Fermi Level Pinning and Schottky Barrier Height Control at Metal-Semiconductor Interfaces of InP and Related Materials, Japanese Journal of Applied Physics, vol. 38, 1999, p. 1098-1102.
Ho, et al., Low-resistance ohmic contacts of p-type GaN achieved by the oxidation of Ni/Au films, Journal of Applied Physics, vol. 86, No. 8, Oct. 1999, pp. 4491-4497.
Hofmann, et al., In situ fabrication of vertical tunnel junctions for SET devices, Microelec Eng'g, vols. 57-58, 2001, pp. 851-856.
Horiguchi, et al., Evaluation of interface potential barrier heights between ultrathin silicon oxides and silicon, Journal of Applied Physics, vol. 58, No. 4, 1985, pp. 1597.
Horváth, et al., The effect of the metal-semiconductor interface on the barrier height in GaAs Schottky junctions, Vacuum, vol. 41, No. 4, 1990, pp. 804-806.
Hudait, et al., Interface states density distribution in Au/n—GaAs Schottky diodes on n—Ge and n—GaAs substrates, Materials Sci. & Eng'g, vol. B87, 2001, pp. 141-147.
Hui, et al., Specific Contact Resistivity of TiSi2 to p+ and n+ Junctions, IEEE Electron Device Letters, vol. EDL-6, No. 9, Sep. 1985, pp. 479-481.

(56) **References Cited**

OTHER PUBLICATIONS

Ilderem, et al., Investigation of the Effects of Very Low Pressure Chemical Vapor Deposited TiSi2 on Device Electrical Characteristics, Journal Electrochem. Soc., vol. 136, No. 10, Oct. 1989, pp. 2989-2993.
Ingerly, et al., Low resistance ohmic contacts to n—GaN and n—AlGaN, Applied Physics Letters, vol. 77, No. 3, Jul. 17, 2000, pp. 382-384.
Itoh, et al., Analysis of Schottky Barrier Heights of Metal/SiC Contacts and Its Possible Application to High-Voltage Rectifying Devices, Physica Status Solidi, vol. 162, 1997, pp. 389-408.
ITRS, Process Integration, Devices, and Structures and Emerging Research Devices, 2001 Ed., 51 pgs.
Ivančo, et al., Electrical Characterization of Au/SiOx/n—GaAs Junctions, Solid-State Elecs., vol. 42, No. 2, 119, pp. 229-233.
Ivančo, et al., Schottky barrier height dependence on the silicon interlayer thickness of Au/Si/n—GaAs contacts: chemistry of interface formation study, Vacuum, No. 50, Issues 3-4, Jul. 1998, pp. 407-411.
Ivančo, et al., Unpinning of the Au/GaAs interfacial Fermi level by means of ultrathin undoped silicon interlayer inclusion, Journal of Applied Physics, vol. 87, No. 2, Jan. 15, 2000, pp. 795-800.
Ivey, Platinum Metals in Ohmic Contacts to III-V Semiconductors, Platinum Metals Research, vol. 43, No. 1, 1999, pp. 2-12.
Jacobs, et al., Optimisation of the Ti/Al/Ni/Au ohmic contact on AlGaN/GaN FET structures, Journal of Crystal Growth, vol. 241, 2002, pp. 15-18.
Kar, et al., Interface States in MOS Structures with 20-40 Å Thick SiO2 Films on Nondegenerate Si*, Solid-State Elecs., vol. 15, 1972, pp. 221-237.
Kasai, Control of Metal/III-V Compound Semiconductor Interfaces and Its Application to Quantum Effect Devices, Thesis, Hokkaido Univ., Dec. 1996, 309 pgs.
Kedzierski, Complementary silicide thin-body silicon-on-insulator CMOS devices, Thesis, U.C. Berkeley, 2001, 134 pgs.
Kim, et al., Low-Resistance Ti/Ai Ohmic Contact on Undoped ZnO, Journal of Elec Materials, vol. 31, No. 8, 2002, pp. 868-871.
Kipperman, et al., Improved efficiency of MIS-silicon solar cells by HF treatment of the oxide layer, Applied Physics Letters, vol. 28, No. 620, 1976, pp. 620-621.
Kobayashi, et al., Studies of interface states at ultrathin SiO2/Si(100) interfaces by means of x-ray photoelectron spectroscopy under biases and their passivation by cyanide treatment, Journal of Applied Physics, vol. 83, No. 4, Feb. 15, 1998, pp. 2098-2103.
Kolodzey, et al., Electrical Conduction and Dielectric Breakdown in Aluminum Oxide Insulators on Silicon, IEEE Trans. on Electron Devices, vol. 47, No. 1, Jan. 2000, pp. 121-128.
LaBrasca, et al., Scanning tunneling microscopy and spectroscopy on pn junctions formed by ion implantation, Journal of Vacuum Sci. & Tech., vol. 9, Mar./Apr. 1991, pp. 752-757.
Lee, et al., Effects of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon, Journal of Applied Physics, vol. 74, No. 21, May 24, 1999, pp. 3143-3145.
Lee, et al., Ohmic contact formation mechanism of nonalloyed contacts to p-type GaN observed by positron annihilation spectroscopy, Applied Physics Letters, vol. 74, No. 16, Apr. 19, 1999, pp. 2289-2291.
Lee, Processing and Characterization of Silicon Carbide (6H- and 4H—SiC) Contacts for High Power and High Temperature Device Applications, Ph.D. Dissertation, KTH, Royal Institute of Technology, 2002, 106 pgs.
Leprince-Wang, et al., Study of the growth morphology of TiO2 thin films by AFM and TEM, Surface and Coatings Tech., vol. 140, 2001, pp. 155-160.
Levy, et al., Selective LPCVD Tungsten for Contact Barrier Applications, Journal Electrochem. Soc., vol. 133, No. 9, Sep. 1986, pp. 1905-1912.
Liauh, et al., Electrical and microstructural characteristics of Ti contacts on (001)Si, Journal of Applied Physics, vol. 74, No. 4, Aug. 15, 1993, pp. 2590-2597.
Lillington, et al., Effects of interfacial oxide layers on the performance of silicon Schottky-barrier solar cells, Applied Physics Letters, vol. 28, No. 2, Jan. 15, 1976, pp. 97-98.
Lin, et al., A novel Pd/oxide/GaAs metal-insulator-semiconductor field-effect transistor (MISFET) hydrogen sensor, Semiconductor Sci. Tech., vol. 16, 2002, pp. 997-1001.
Lin, et al., Low resistance ohmic contacts on wide band-gap GaN, Applied Physics Letters, vol. 64, No. 8, Feb. 1994, pp. 1003-1005.
Look, et al., Unpinning of GaAs Surface Fermi Level by 200 Degrees C Molecular Beam Epitaxial Layer, Applied Physics Letters, vol. 57, No. 24, Dec. 10, 1990, pp. 2570-2572.
Lucovsky, Reaction/annealing pathways for forming ultrathin silicon nitride films for composite oxide-nitride gate dielectrics with nitrided crystalline silicon-dielectric interfaces for application in advanced complementary metal-oxide-semiconductor devices, Journal of Vacuum Sci. & Tech A, vol. 17, No. 4, Jul./Aug. 1999, pp. 1340-1351.
Lue, et al., A method to characterize the dielectric and interfacial properties of metal-insulator-semiconductor structures by microwave measurement, Journal of Applied Physics, vol. 91, No. 8, Apr. 15, 2002, pp. 5275-5282.
Luther, et al., Analysis of a thin AIN interfacial layer in Ti/Al and Pd/Al ohmic contacts to n-type GaN, Applied Physics Letters, vol. 71, No. 26, Dec. 29, 1997, pp. 3859-3861.
Maeda, et al., A Highly Reliable Interconnection for a BF2-Implanted Junction Utilizing TiN/Ti Barrier Metal System, IEEE Trans. of Electron Devices, vol. ED-34, No. 3, Mar. 1987, pp. 599-606.
Mahalingam, Trench MOS Based Power Devices with Graded Doped Profile, Thesis, No. Carolina Univ., 1999, 295 pgs.
Mamor, et al., Schottky Barrier Heights on IV-IV Compound Semiconductors, Journal of Elec Materials, vol. 25, No. 11, Nov. 1996, pp. 1748-1753.
Marinova, et al., Nickel based ohmic contacts on SiC, Materials Sci. & Eng'g, vol. B46, 1997, pp. 223-226.
Matsuzawa, et al., A Unified Simulation of Schottky and Ohmic Contacts, IEEE Trans. on Electron Devices, vol. 47, No. 1, Jan. 2000, pp. 103-108.
Miller, et al., Ohmic Contacts to n-Type GaN, Journal of Elec Materials, vol. 25, No. 11, 1996, pp. 1709-1714.
Mönch, Electron properties of ideal and interface-modified metal-semiconductor interfaces, Journal of Vacuum Sci. & Tech. B, vol. 14, No. 4, Jul./Aug. 1998, pp. 2985-2993.
Morita, et al., Growth of native oxide on a silicon surface, Journal of Applied Physics, vol. 68, No. 3, Aug. 1990, pp. 1272-1281.
Muret, et al., Unpinning of the Fermi level at erbium silicide/silicon interfaces, Physical Review B, vol. 56, No. 15, Oct. 15, 1997, pp. 9286-9289.
Nakasaki, et al., Tungsten/titanium nitride low-resistance interconnections durable for high-temperature processing, Journal of Applied Physics, vol. 64, No. 8, Sep. 15, 1988, pp. 3263-3268.
Nielsen, Current mechanism of tunnel m.i.s. solar cells, IEE Proceedings, vol. 127, Part 1, No. 6, Dec. 1980, pp. 301-307.
Nielsen, Current Mechanism of Tunnel MIS Solar Cells, IEE Proceedings, vol. 129, Part 1, No. 4, Aug. 1982, pp. 153-156.
O'Donnell, et al., Temperature dependence of semiconductor band gaps, Applied Physics Letters, vol. 58, No. 25, Jun. 24, 1991, pp. 2924-2926.
Okada, et al., Electrical Characteristics and Reliability of Pt/Ti/Pt/Au Ohmic Contacts to p-Type GaAs, Japanese Journal of Applied Physics, vol. 30, No. 4A, Apr. 1991, pp. L558-L560.
O'Meara, et al., Experimental Design Study of Coincident Titanium Nitride/Titanium Silicide Formation from Rapid Thermal Processing, Materials Research Soc. Symposium Proceedings, Vo. 260, 1992, pp. 805-811.
Oskam, et al., Electrochemical deposition of metals onto silicon, Journal of Applied Physics, vol. 31, 1998, pp. 1927-1949.
Park, et al., Impact of atomic-layer-deposited TiN on the gate oxide quality of W/TiN/SiO2/Si metal-oxide-semiconductor structures, Applied Physics Letters, vol. 80, No. 14, Apr. 8, 2002, pp. 2514-2516.

(56) **References Cited**

OTHER PUBLICATIONS

Park, et al., Improved Low Resistance Contacts of Ni/Au and Pd/Au to p-Type GaN Using a Cryogenic Treatment,Cambridge Univ. Press, Jun. 13, 2014, 6 pgs.
Park, et al., Metal-insulator-semiconductor structure on GaAs using a pseudomorphic Si/GaP interlayer, Journal of Vacuum & Sci. Tech., vol. 15, Mar./Apr. 1997, pp. 252-258.
Park, et al., Si3N4/Si/In0.05Ga0.95As/n-GaAs metal-insulator-semiconductor devices, Journal of Applied Physics, vol. 81, No. 1, Jan. 1, 1997, pp. 516-523.
Park, et al., Thermal stability of molybdenum-silicon nitride-silicon Schottky diodes, Journal of Applied Physics, vol. 69, No. 5, Mar. 1, 1991, pp. 3149-3153.
Patkar, et al., Very low resistance nonalloyed ohmic contacts using low-temperature molecular beam epitaxy of GaAs, Am. Institute of Physics, vol. 66, No. 11, Mar. 13, 1996, pp. 1412-1414.
Plummer, et al., Material and Process Limits in Silicon VLSI Technology, IEEE, vol. 89, No. 3, Mar. 2000, pp. 240-258.
Polishchuk, et al., Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion, IEEE Electron Device Letters, vol. 22, No. 9, Sep. 2001, pp. 444-446.
Porter, et al., Effect of Interfacial Oxide Layers on the Current-Voltage Characteristics of Al—Si Contacts, NASA Contracte #NAS8-26379, Nov. 1976, 67 pgs.
Proctor, et al., Direct Measurements of Interfacial Contact Resistance, End Contact Resistance, and Interfacial Contact Layer Uniformity, IEEE Trans. of Electron Devices, vol. ED-30, No. 11, Nov. 1983, pp. 1535-1542.
Ren, Nanoscale MOSFETS: Physics, Simulation and Design, Thesis, Purdue Univ., Oct. 2001, 211 pgs.
Rhoderick, Metal-semiconductor contacts, IEEE Proceedings, vol. 129, Part 1, No. 1, Feb. 1982, pp. 1-14.
Rhoderick, The physics of Schottky barriers, Review of Physics in Tech., 1970, pp. 81-95.
Richards, Novel Uses of Titanium Dioxide of Solar Cells, Thesis, Univ. of New South Wales, Apr. 2002, 259 pgs.
Rohdin, et al., Interfacial Gate Resistance in Schottky-Barrier-Gate Field-Effect Transistors, Hewlett-Packard Company, 1998, pp. 1-25.
Sambell, et al., Unpinning the GaAs Fermi Level with Thin Heavily Doped Silicon Overlayers, IEEE Trans. of Electron Devices, vol. 37, No. 1, Jan. 1990, pp. 88-95.
Schenk, Halbleiterbauelemente—Physikalische Grundlagen and Simulation, Integrated Sys Lab, Dec. 18, 2001, 177 pgs.
Schenk, Semiconductor components Physical basics and simulation, Integrated Sys Lab, Dec. 18, 2001, 5 pgs.
Semi. Indus. Assocation, The International Technology Roadmap for Semiconductors 2001 Edition—Interconnect, 2001, pp. 1-25.
Sharma, Influence of thin inversion layers on Schottky diodes, Revue de Physique Applicquee, vol. 21, Jan. 1986, pp. 25-33.
Shewchun, Metal-Insulator-Semiconductor (MIS) and Semiconductor-Insulator-Semiconductor (SIS) Solar Cells: 1. Basic Principles, 1979, pp. 843-867.
Shewchun, et al., MIS and SIS Solar Cells, IEEE Trans. on Electron Devices, vol. ED-27, vol. 4, Apr. 1980, pp. 705-716.
Shewchun, et al., Theory of metal-insulator-semiconductor solar cells, Journal of Applied Physics, vol. 48, Nov. 2, Feb. 1977, pp. 765-770.
Shih, et al., Effects of interfacial microstructure on uniformity and thermal stability of AuNiGe ohmic contact to n-type GaAs, Journal of Applied Physics, vol. 62, No. 2, Jul. 15, 1987, pp. 582-590.
Singh, Theory of Metal-Insulator-Semiconductor (MIS) and Semiconductor-Insulator-Semiconductor (SIS) Solar Cells, Thesis, McMaster University, Apr. 1979, 365 pgs.
Smith, et al., Chemical Vapour Deposition of the Oxides of Titanium, Zironium and Hafnium for Use as High-k Materials in Microelectronic Devices. A Carbon-free Precursor for the Synthesis of Hafnium Dioxide, Adv. Materials for Optics and Elecs, vol. 10, 2000, pp. 105-114.
Sobolewski, et al., Analysis of Thin Thermal Silicon Nitride Films on Silicon, Applied Surface Sci., vol. 30, 1987, pp. 210-215.
Sobolewski, et al., Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes, Journal of Sci. Tech., vol. 7, No. 4, Jul./Aug. 1989, pp. 971-979.
Song, et al., Effects of sulfur passivation on Ti/A1 ohmic contacts to n-type GaN using CH3CSNH2 solution, Applied Physics Letters, vol. 80, No. 17, Apr. 29, 2002, pp. 3129-3131.
Spicer, et al., Study of the Electronic Surface States of III-V Compounds and Silicon, DARPA Order No. 3564, Program Code No. HX 1241, Oct. 1, 1981, 158 pgs.
Spicer, et al., Unified Mechanism for Schottky-Barrier Formation and III-V Oxide Interface States, Physical Review Letters, vol. 44, No. 6, Feb. 11, 1980, pp. 420-423.
Srivastava, et al., Theory of Metal-Oxide-Semiconductor Solar Cells, Solid-State Elecs., vol. 22, 1987, pp. 581-587.
Streetman, Solid State Electronic Devices, Fourth Ed., Prentice-Hall, Inc., 1995, 91 pgs.
Suguro, et al., Reaction Kinetics in Tungsten/Barrier Metal Silicon Systems, Thin Solid Films, vol. 166, 1988, pp. 1-14.
Taboryski, et al., Superconductor-Semiconductor-Superconductor Planar Junctions of Aluminum on δ-doped Gallium-Arsenide, IEEE Trans. on Applied Superconductivity, vol. 7, No. 2, Jun. 2, 1997, pp. 2809-2813.
Taubeblatt, et al., Interface effects in titanium and hafnium Schottky barriers on silicon, Applied Physics Letters, vol. 44, No. 9, May 1, 1984, pp. 895-897.
Taubenlatt, et al., Silicide and Schottky barrier formation in the Ti—Si and the Ti—SiOx—Si systems, Journal of Applied Physics, vol. 53, No. 9, Sep. 1982, pp. 6308-6315.
Teraji, et al., Ideal Ohmic contact to n-type 6H—SiC by reduction of Schottky barrier height, Applied Physics Letters, vol. 71, No. 5, Aug. 1997, pp. 689-691.
Thanailakis, Contacts between simple metals and atomically clean silicon, Journal of Physics C: Solid State Physics, vol. 8, 1975, pp. 655-668.
Thanailakis, et al., Transition-metal contacts to atomically clean silicon, Journal of Physics C: Solid State Physics, vol. 9, 1976, pp. 337-343.
Tiwari, et al., Unpinned GaAs MOS Capacitors and Transistors, IEEE Electron Device Letters, vol. 9, No. 9, Sep. 1988, pp. 488-490.
Topham, Ohmic Contacts to N-Type Indium Phosphide, Thesis, Univ. of Surrey, Sep. 1983, 176 pgs.
Tsutsumi, et al., A Selective LPCVD Tungsten Process Using Silane Reduction for VLSI Applications, IEEE Trans. on Electron Devices, vol. 37, No. 3, Mar. 1990, pp. 569-576.
Tucker, Dynamic Capacitance of Metal-Oxide-Semiconductor Field-Effect Transistors, Thesis, Univ. of Missouri, 1968, 82 pgs.
Tung, Schottky-Barrier Formation of Single-Crystal Metal-Semiconductor Interfaces, Physical Review Letters, vol. 52, No. 6, Feb. 6, 1984, pp. 461-464.
Turner, et al., Metal-Silicon Schottky Barriers, Solid-State Elecs., vol. 11, 1968, pp. 291-300.
Van Otterloo, Schottky Barriers on Clean-Cleaved Silicon, Surface Science, vol. 104, 1981, pp. L205-L209.
Vilinaus Univ., The Metal-Semiconductor Junction. Schottky Diode Ohmic Contacts, Vilinaus Univ., Semiconductor Physics Dept., Lithuania, downloaded Jan. 25, 2020, 18 pgs.
Waldrop, et al., Formation and Schottky barrier height of metal contacts to β-SiC, Applied Physics Letters, vol. 56, No. 6, Feb. 5, 1990, pp. 557-559.
Waldrop, et al., Metal Schottky barrier contacts to alpha 6H-SiC, Journal of Applied Physics, vol. 72, No. 10, Nov. 15, 1992, pp. 4757-4760.
Waldrop, et al., Wide range of Schottky barrier height for metal contacts to GaAs controlled by Si interface layers, Journal of Vacuum Sci. & Tech. B, vol. 4, No. 4, Jul./Aug. 1988, pp. 1432-1435.
Walukiewicz, Mechanism of Schottky Barrier Formation: The Role of Amphoteric Native Defects, Lawrence Berkeley Nat'l Lab., Feb. 1, 1987, 23 pgs.
Werner, et al., Barrier inhomogeneities at Schottky contacts, Journal of Applied Physics, vol. 69, No. 3, Feb. 1, 1991, pp. 1522-1533.
Weste, et al., Principles of CMOS Technology: A Systems Perspective, Second Ed., Addison Wesley Longman, 1993, 749 pgs.

(56) **References Cited**

OTHER PUBLICATIONS

Williams, Interfaces in Semiconductor Structures and Devices, Physik Bl., vol. 45, Nr. 7, 1989, pp. 219-222.
Williams, Metal-Semiconductor Interfaces, The Physics of Submicron Semiconductor Devices, 1988, pp. 683-701.
Wilson, et al., Differential Capacitance-Voltage Profiling of Schottky Barrier Diodes for Measuring Implanted Depth Distributions in Silicon, U.S. Dept. of Commerce, Nat'l Bureau of Standards, Feb. 1982, 68 pgs.
Wittmer, et al., Ideal Schottky Diodes on Passivated Silicon, Physical Review Letters, vol. 69, No. 18, Nov. 2, 1993, pp. 2701-2704.
Wu, Barrier height reduction of the Schottky barrier diode using a thin highly doped surface layer, Journal of Applied Physics, vol. 51, No. 9, Sep. 1980, pp. 4919-4922.
Wu, et al., Interface capacitance in metal-semiconductor junctions, Journal of Applied Physics, vol. 65, No. 9, May 1, 1989, pp. 3560-3567.
Yang, et al, Tunneling in a Metal-Semiconductor—Semiconductor Thin-Film Diode, Solid-State Elec., vol. 29, No. 3, 1986, pp. 355-357.
Yen, et al., Thermally Assisted Multiphoton Photoelectric Emission from Tungsten, Optics Communications, vol. 35, No. 2, Nov. 1980, pp. 277-282.
Zafar, A method for measuring barrier heights, metal work functions and fixed charge densities in metal/SiO2/Si capacitors, Applied Physics Letters, vol. 80, No. 25, Jun. 24, 2002, pp. 4858-4860.
Zaima, et al., Electrical Properties and Crystallographic Structures of Transition Metal/Silicon Interface, Materia Japan, vol. 33, No. 6, 1994, pp. 691-696.
Zaima, et al., Formation of silichide at metal/silicon interface and low-resistivity contacts, Applied Physics, vol. 63, No. 11, 1994, pp. 1093-1105.
Zaima, et al., Study on determining factors of low contact resistivity in transition metal-silicon systems, Applied Surface Science, vols. 70/71, 1993, pp. 624-628.
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction and Prehearing Statement, 10 pgs. (Jul. 23, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Joint Claim Construction and Prehearing Statement, 9 pgs. (Jul. 23, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Joint Claim Construction and Prehearing Statement, 8 pgs. (Jul. 23, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Revised Joint Claim Construction and Prehearing Statement, 9 pgs. (Aug. 20, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Ex. A to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Ex. B to Revised Joint Claim Construction and Prehearing Statement, 7 pgs. (Aug. 20, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Opening Claim Construction Brief, 39 pgs. (Aug. 21, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Defendant's Responsive Claim Construction Brief, 33 pgs. (Sep. 4, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Plaintiff's Reply Claim Construction Brief, 17 pgs. (Sep. 11, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart, 20 pgs. (Sep. 18, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Joint Claim Construction Chart Appendices, 12 pgs. (Aug. 21, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Claim Construction Memorandum Opinion and Order, 40 pgs. (Oct. 16, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Order Correcting Typographical Error in Claim Construction Memorandum Opinion and Order, 2 pgs. (Nov. 18, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Order of Judge R. Gilstrap Adopting Claim Construction Memorandum Opinion and Order, 2 pgs. (Dec. 10, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Expert Report of Dr. Jeffrey Bokor Regarding Invalidity of U.S. Pat. No. 7,084,423, U.S. Pat. No. 8,766,336, U.S. Pat. No. 9,209,261, U.S. Pat. No. 9,461,167, U.S. Pat. No. 9,905,691, and U.S. Pat. No. 10,090,395 (Redacted) (Nov. 16, 2020).
Exhibit A to Expert Report of Dr. Jeffrey Bokor in *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), CV of Dr. Jeffrey Boker, 36 pgs. (Nov. 16, 2020).
Exhibit B to Expert Report of Dr. Jeffrey Bokor in *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Materials Considered in Connection with Report, 4 pgs. (Nov. 16, 2020).
Exhibit C to Expert Report of Dr. Jeffrey Bokor in *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '336 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Pat. No. 7,176,483, 38 pgs. (Nov. 16, 2020).
Exhibit D to Expert Report of Dr. Jeffrey Bokor in *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '261 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Pat. No. 7,176,483, 7 pgs. (Nov. 16, 2020).
Exhibit E to Expert Report of Dr. Jeffrey Bokor in *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '167 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Pat. No. 7,176,483, 16 pgs. (Nov. 16, 2020).
Exhibit F to Expert Report of Dr. Jeffrey Bokor in *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipation of '691 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Pat. No. 7,176,483, 8 pgs. (Nov. 16, 2020).
Exhibit G to Expert Report of Dr. Jeffrey Bokor in *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Claim Chart re Anticipated of '395 Patent Based on U.S. Patent Publication 2005/0093027 ("Grupp") and U.S. Pat. No. 7,176,483, 8 pgs. (Nov. 16, 2020).
Exhibit H to Expert Report of Dr. Jeffrey Bokor in *Acorn Semi, LLC* v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), List of Claims by Grouping, 4 pgs. (Nov. 16, 2020).
Acorn Semi, LLC v. *Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-cv-347-JRG (EDTX), Rebuttal Expert Report of Edwin Piner, Ph.D. (Redacted) (Dec. 14, 2020).

* cited by examiner

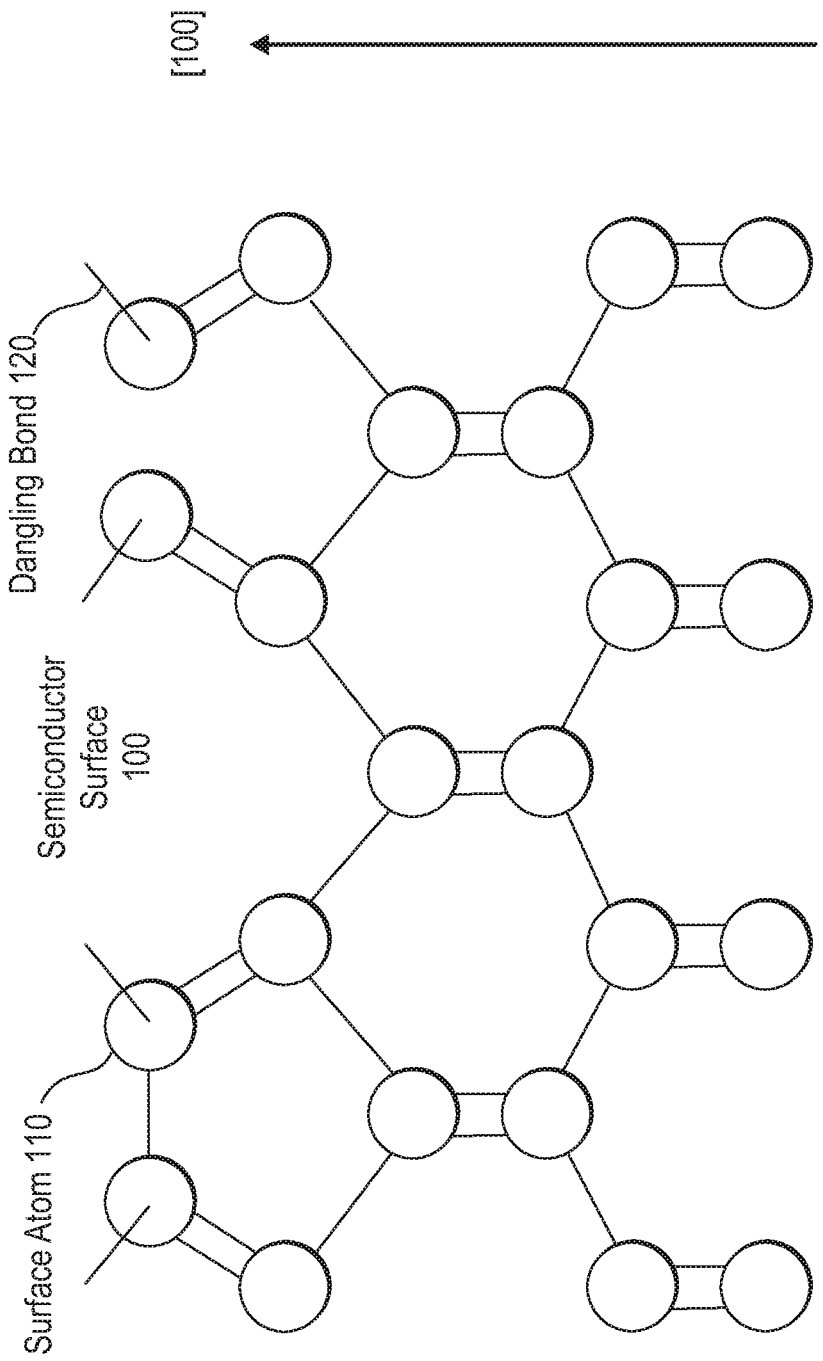

Surface Atom 110
Semiconductor Surface 100
Dangling Bond 120
[100]

Fig. 1

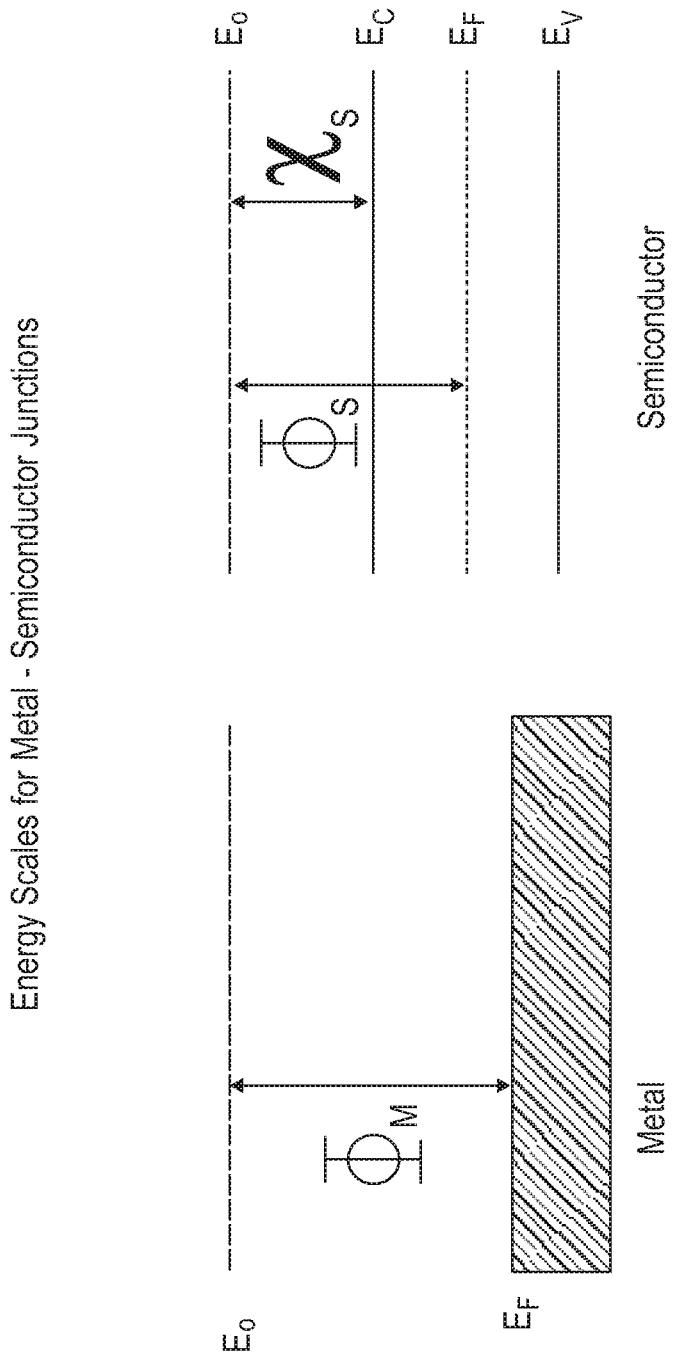

Energy Scales for Metal - Semiconductor Junctions
E_0
Θ_M
E_F
Metal
E_0
Θ_S
χ_S
E_C
E_F
E_V
Semiconductor

Fig. 2

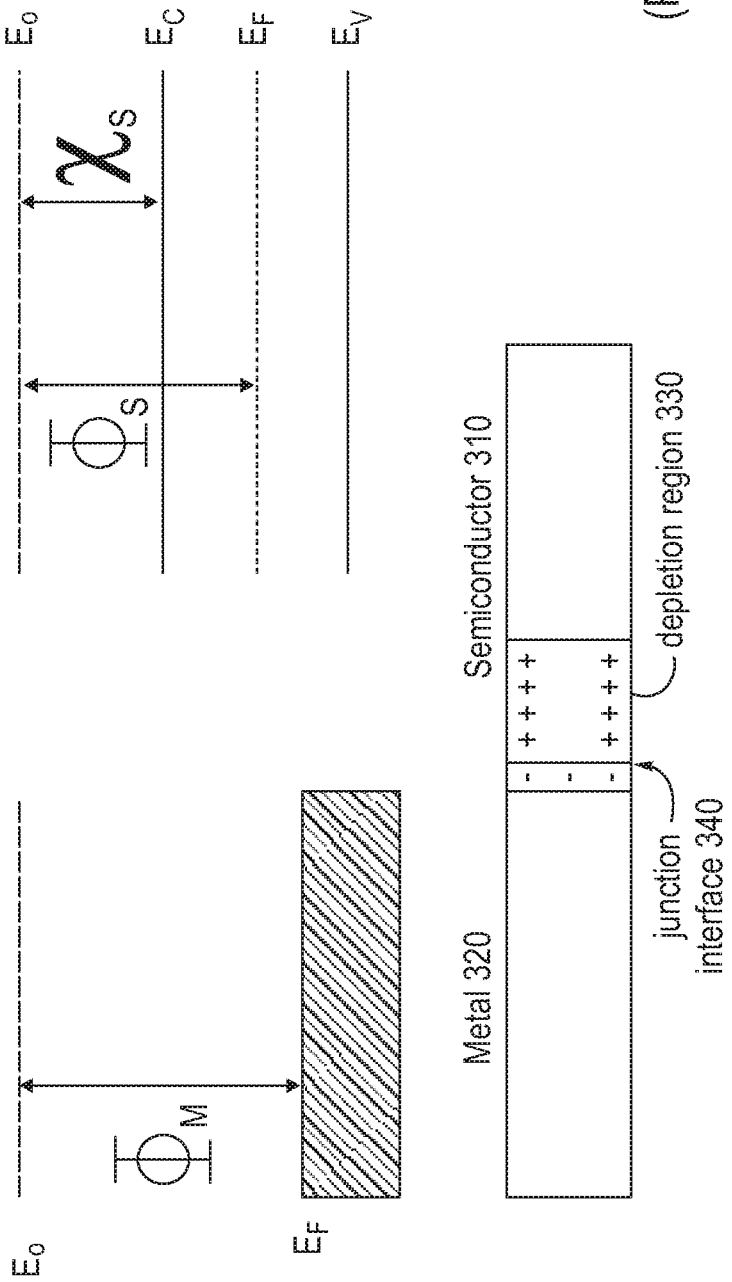


Fig. 3 (Prior Art)

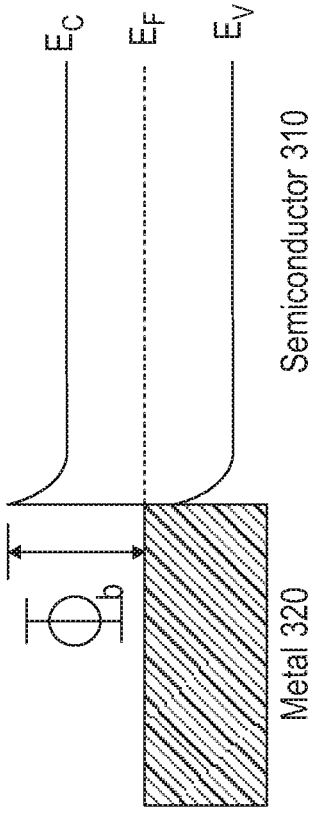


Fig. 4 (Prior Art)

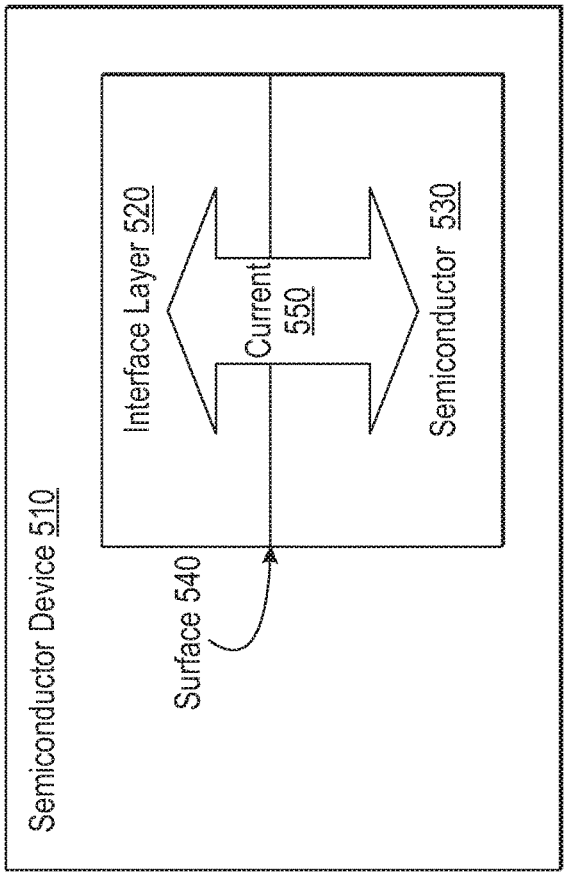

Semiconductor Device 510
Interface Layer 520
Current 550
Semiconductor 530
Surface 540

Fig. 5

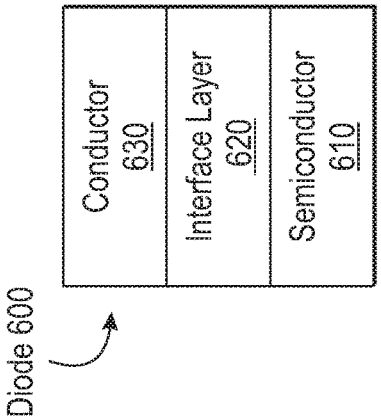

Diode 600
Conductor 630
Interface Layer 620
Semiconductor 610

Fig.6

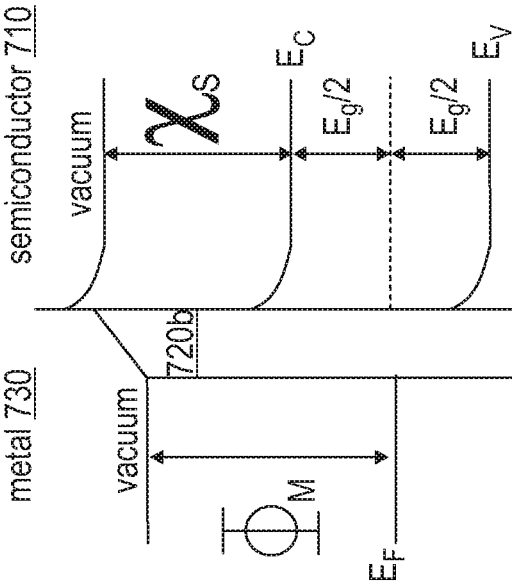


Fig. 7b

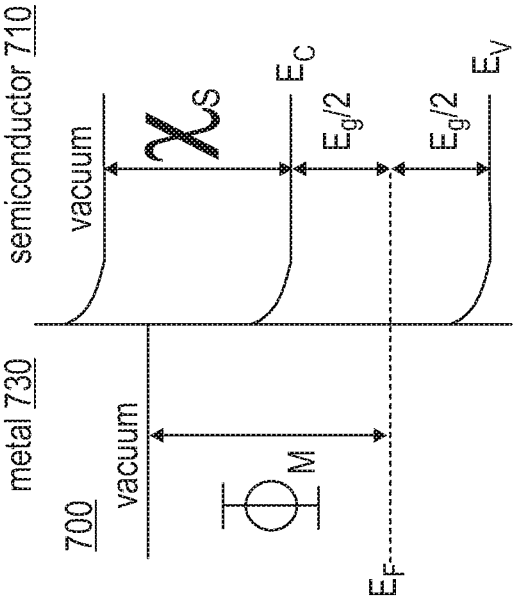


Fig. 7a

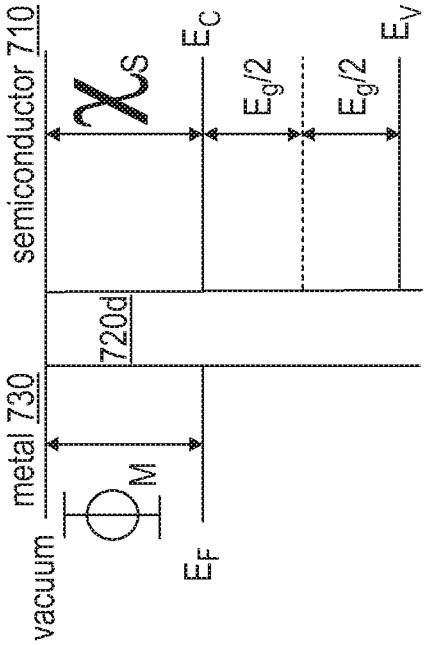


Fig. 7d

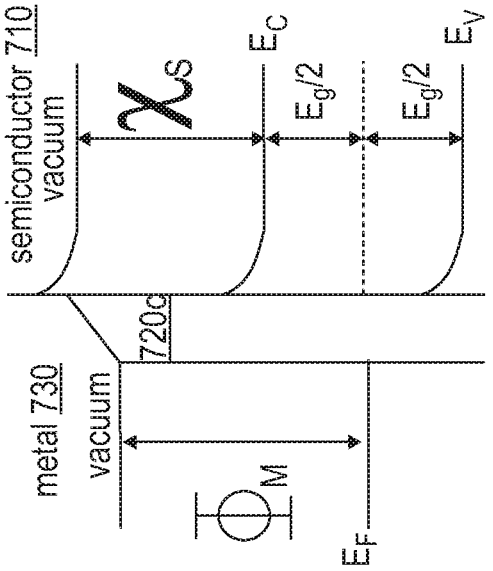


Fig. 7c

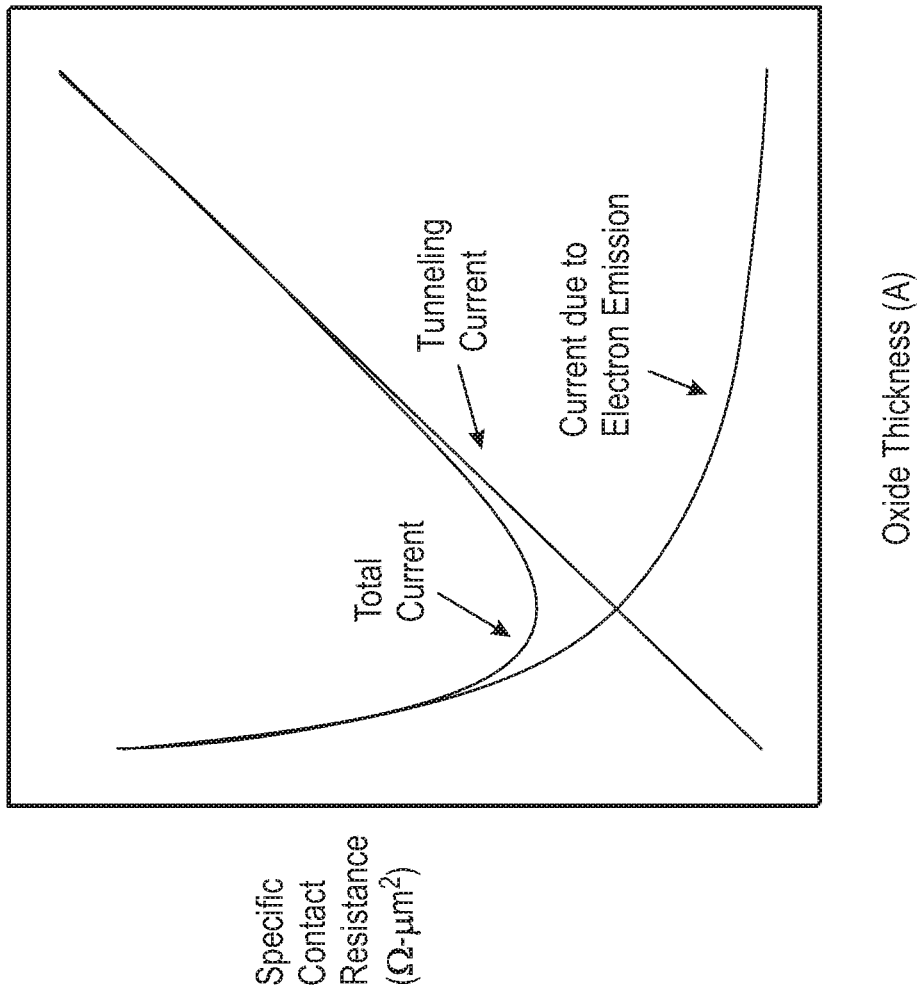

Specific Contact Resistance (Ω-μm^2)
Total Current
Tunneling Current
Current due to Electron Emission
Oxide Thickness (A)

Fig. 8

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

The present application is a CONTINUATION of U.S. patent application Ser. No. 16/506,022, filed Jul. 9, 2019, which is a CONTINUATION of U.S. patent application Ser. No. 15/728,002, filed Oct. 9, 2017, now U.S. Pat. No. 10,388,748, which is a CONTINUATION of U.S. patent application Ser. No. 15/251,210, filed Aug. 30, 2016, now U.S. Pat. No. 9,812,542, which is a CONTINUATION of U.S. patent application Ser. No. 15/048,877, filed Feb. 19, 2016, now U.S. Pat. No. 9,905,691, which is a CONTINUATION of U.S. patent application Ser. No. 13/552,556, filed Jul. 18, 2012, now U.S. Pat. No. 9,425,277, which is a CONTINUATION of U.S. patent application Ser. No. 13/022,522, filed Feb. 7, 2011, now U.S. Pat. No. 8,431,469, which is a DIVISIONAL of U.S. patent application Ser. No. 12/197,996, filed Aug. 25, 2008, now U.S. Pat. No. 7,884,003, which is a DIVISIONAL of U.S. patent application Ser. No. 11/181,217, filed Jul. 13, 2005, now U.S. Pat. No. 7,462,860, which is a CONTINUATION of U.S. patent application Ser. No. 10/217,758, filed Aug. 12, 2002, now U.S. Pat. No. 7,084,423, all of which are hereby incorporated by reference.

FIELD OF THE INVENTION

The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e. the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at T=0) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\varphi_B=\varphi_M-\chi_S \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the election affinity of the semiconductor.

Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination. FIG. **1** shows a cross-section of an un-passivated silicon surface labeled **100**. The particular silicon surface shown is an Si(100) 2×1 surface. As shown, the silicon atoms at the surface, such as atom **110**, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond **120**. These dangling bonds may be responsible for surface states that trap electrical charges.

Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depth the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention.

Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately 10 Ω-μm^2. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia (NH3), nitrogen (N2) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

FIG. **1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

FIG. **2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

FIG. **3** shows an energy band diagram for a conventional metal-n-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

FIG. **4** illustrates band bending at a conventional metal-n-type semiconductor junction.

FIG. **5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

FIG. **6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

FIGS. **7***a*, **7***b*, **7***c* and **7***d* show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

FIG. **8** shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately 10 Ω-$\|m^2$ or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal-interface layer-semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for n- and p-type semiconductors, respectively), the IV characteristic will be nearly symmetric, especially at low voltage. In this case, the term "forward bias" is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around midgap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a p-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an n-type semiconductor. These junctions are diodes, in that little current will flow if the n-type (p-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

I. Introduction and Definitions

The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in FIG. **2**. The so-called vacuum level (E0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents

the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (ΦM) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

Now consider a conventional junction between a metal and an n-type, semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S<\Phi_M$). An n-type semiconductor is one in which electrons are the majority charge carriers (in p-type semiconductors, holes are the majority charge carrier). As shown in FIG. **3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor **310** to the metal **320** when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) **330** forms near the junction interface **340**.

The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see FIG. **4**). The band bending creates an energy barrier (discussed above) that blocks further transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a p-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-n-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-p-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor-interface layer-metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrified semiconductor surface to provide chemical passivation. That is, a nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-

insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing n- and p-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

FIG. **5** shows a semiconductor device **510** that contains a semiconductor **530** and an interface layer **520** formed on a surface **540** of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

The semiconductor **530** contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

The semiconductor **530** has a surface **540** that is passivated by the interface layer **520**. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface **540**. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor **530** is operable to be electrically coupled with a first voltage associated with the semiconductor device **510** and to conduct electrical current **550** across the passivated surface **540**.

The interface layer **520** is formed on the semiconductor **530** and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer **520**, while in other cases the interface layer **520** may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface **540**, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

Different passivation materials are contemplated. According to one embodiment, the interface layer **520** is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer **520** may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer **520** includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface **540**.

In some cases, passivation of the semiconductor surface **540** will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen and Fluorine

An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300° C. and about 750° C., which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH_3) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10-9 Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900° C. and about 1000° C., or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700° C. and 1000° C., or higher.

Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

IV. Diodes Containing Passivated Semiconductor Surfaces

Diodes made from Schottky barriers (i.e. asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, con-

ductor-semiconductor junction, and multi-material junction are all related and appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

FIG. **6** shows an example of a diode **600** containing, according to one embodiment of the present invention, an interface layer **620** disposed between and attached to both a semiconductor **610** and a conductor **630**. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode **600** and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor **610** and the interface layer **620**.

The conductor **630** contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys), and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

A metal having a predetermined work function truly be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

The semiconductor-interface layer-conductor configuration illustrated in FIG. **6** defines what the present inventors have chosen to call a "passivated Schottky barrier". The passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

To understand why thickness of the interface layer is important, refer briefly to FIG. **8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used

(e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer **620** is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

Another advantage achieved through the use of the interface layer **620** is greater flexibility afforded in selecting a conductor **630**. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

For example, to make large-barrier diodes, for an n-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a p-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

The use of interface layer **620** thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer **620**, the barrier height would be substantially untunable, un-adjustable, and fixed (as discussed above).

The role played by interface layer **620** in tuning, adjusting, or controlling the height of the barrier between the conductor **630** and the semiconductor **610** may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

According to one embodiment of the present invention then, the interface layer **620** is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

FIG. **7***a*-**7***d* show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_S of the semiconductor. In FIG. **7***a*, an unpassivated Schottky barrier **700** is shown. In this example, the Fermi level (E_F) of the metal **730** is pinned in

the bandgap of the semiconductor **710**. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

In FIG. **7***b*, the interface layer **720***b* is thick enough to passivate dangling bonds at the surface of the semiconductor **710**, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in FIG. **7***c*, when the interface layer **720***c* is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in FIG. **7***d*, when the interface layer **720***d* is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately Φ_M=4.1 eV and the electron affinity for Si of approximately χ_S=4.05 eV.

V. Transistors Containing Passivated Semiconductor Surfaces

The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Pat. No. 6,833,556, issued Dec. 21, 2004, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed Jan. 14, 2003 by the present inventors, and assigned to the assignee of the present invention.

The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n+-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in FIG. **7***d*). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide-semiconductor junction a Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

What is claimed is:

1. An electrical junction, comprising:

a semiconductor substrate;

a metal electrical contact proximate to said semiconductor substrate; and

a passivating dielectric tunnel barrier layer disposed between said semiconductor substrate and said metal electrical contact,

said semiconductor substrate being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer is configured to increase a height of a Schottky barrier for electrons between the metal electrical contact and the semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween.

2. The electrical junction of claim **1**, wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si.

3. The electrical junction of claim 2, wherein the metal electrical contact comprises a metal having a work function near or substantially equal to a conduction band edge of the semiconductor.

4. The electrical junction of claim 3, wherein the metal having a work function near or substantially equal to a conduction band edge of the semiconductor comprises one of: aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn).

5. The electrical junction of claim 3, wherein the semiconductor substrate is doped p-type proximate to the electrical contact.

6. The electrical junction of claim 3, wherein the semiconductor substrate is undoped proximate to the electrical contact.

7. An electrical junction, comprising:

a semiconductor substrate;

a metal electrical contact proximate to said semiconductor substrate;

and a passivating dielectric tunnel barrier layer disposed between said semiconductor substrate and said metal electrical contact,

said semiconductor substrate being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer is configured to increase a height of a Schottky barrier for holes between the metal electrical contact and the semiconductor substrate from that which would exist at a contact junction between the metal electrical contact and the semiconductor substrate without the dielectric tunnel barrier layer disposed therebetween.

8. The electrical junction of claim 7, wherein the semiconductor substrate comprises one of: silicon (Si), an alloy of germanium (Ge) and Si, and an alloy of carbon (C) and Si.

9. The electrical junction of claim 8, wherein the metal electrical contact comprises a metal having a work function near or substantially equal to a valence band edge of the semiconductor.

10. The electrical junction of claim 9, wherein the metal having a work function near or substantially equal to a valence band edge of the semiconductor comprises one of: platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Go), or palladium (Pd).

11. The electrical junction of claim 9, wherein the semiconductor substrate is doped n-type proximate to the electrical contact.

12. The electrical junction of claim 9, wherein the semiconductor substrate is undoped proximate to the electrical contact.

* * * * *