Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Daniel E. Grupp	Nonprovisional Application Number (if known):	
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Tarek N. Fahmi/	Date 2018-01-23
Name (Print/Typed) Tarek N. Fahmi	Practitioner Registration Number 41402

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☐ *Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC10
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or **all** of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Daniel	E.	Grupp	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Palo Alto	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	1200 Prospect Street, Suite 475		
Address 2			
City	La Jolla	**State/Province**	CA
Postal Code	92037	**Country** i	US

Inventor 2 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Daniel	J.	Connelly	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Redwood City	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	1200 Prospect Street, Suite 475		
Address 2			
City	La Jolla	**State/Province**	CA
Postal Code	92037	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC10
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Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	27571		
Email Address	patents@ascendalaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS		
Attorney Docket Number	3771-0003-DC10	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	27571		

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC10
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15728002	2017-10-09
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15728002	Continuation of	15251210	2016-08-30	9812542	2017-11-07

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15251210	Continuation of	15048877	2016-02-19
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15048877	Continuation of	13552556	2012-07-18	9425277	2016-08-23

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13552556	Continuation of	13022522	2011-02-07	8431469	2013-04-30

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13022522	Division of	12197996	2008-08-25	7884003	2011-02-08

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12197996	Division of	11181217	2005-07-13	7462860	2008-12-09

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11181217	Continuation of	10217758	2002-08-12	7084423	2006-08-01

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC10
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC10
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Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC10
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Acorn Technologies, Inc.		
Mailing Address Information For Applicant:			
Address 1	1200 Prospect Street, Suite 475		
Address 2			
City	La Jolla	**State/Province**	CA
Country	US	Postal Code	92037
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC10
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Tarek N. Fahmi/			Date (YYYY-MM-DD)	2018-01-23
First Name	Tarek	Last Name	Fahmi	Registration Number	41402

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3771-0003-DC10
	Application Number	
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

[0001] The present application is a CONTINUATION of U.S. Patent Application No. 15/728,002, filed October 9, 2017, presently pending, which is a CONTINUATION of U.S. Patent Application No. 15/251,210, filed 8/30/2016, now U.S. Patent 9,812,542, which is a CONTINUATION of U.S. Patent Application No. 15/048,877, filed 2/19/2016, which is a CONTINUATION of U.S. Patent Application No. 13/552,556, filed 7/18/2012, now U.S. Patent 9,425,277, which is a CONTINUATION of U.S. Patent Application No. 13/022,522, filed 2/7/2011, now U.S. Patent 8,431,469, which is a DIVISIONAL of U.S. Patent Application 12/197,996, filed 8/25/2008, now U.S. Patent 7,884,003, which is a DIVISIONAL of U.S. Patent Application 11/181,217, filed 7/13/2005, now U.S. Patent 7,462,860, which is a CONTINUATION of U.S. Patent Application 10/217,758, filed 8/12/2002, now U.S. Patent 7,084,423, which is related to U.S. Patent Application 10/342,576, filed 1/14/2003, now U.S. Patent 6,833,556, all of which are hereby incorporated by reference.

FIELD OF THE INVENTION

[0002] The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with

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a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

[0004] Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at T=0) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\varphi_B = \varphi_M - \chi_S \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the electron affinity of the semiconductor.

[0005] Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

[0006] Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination. FIG. 1 shows a

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cross-section of an un-passivated silicon surface labeled 100. The particular silicon surface shown is an Si(100) 2×1 surface. As shown, the silicon atoms at the surface, such as atom 110, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond 120. These dangling bonds may be responsible for surface states that trap electrical charges.

[0007] Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

[0008] For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0009] Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band

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structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

[0010] One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

[0011] The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

[0012] The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the

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effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention.

[0013] Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately 10 Ω-μm^2. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

[0014] In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia (NH3), nitrogen (N2) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

[0015] A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

[0016] Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer

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configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0018] FIG. 1 shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

[0019] FIG. 2 illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

[0020] FIG. 3 shows an energy band diagram for a conventional metal-n-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

[0021] FIG. 4 illustrates band bending at a conventional metal-n-type semiconductor junction.

[0022] FIG. 5 shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

[0023] FIG. 6 shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

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[0024] FIGS. *7a*, *7b*, *7c* and *7d* show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

[0025] FIG. 8 shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0027] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0028] The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally

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near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

[0029] The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal-interface layer-semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

[0030] It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for n- and p-type semiconductors, respectively), the IV characteristic will be nearly symmetric, especially at low voltage. In this case, the term "forward bias" is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

[0031] It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a p-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an n-type semiconductor. These junctions are diodes, in that little current will flow if the n-type (p-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The

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low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

[0032] Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

[0033] In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

[0034] The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

[0035] I. Introduction and Definitions

[0036] The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some

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important energy scales, which are shown graphically in FIG. 2. The so-called vacuum level (E0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (ΦM) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

[0037] As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

[0038] Now consider a conventional junction between a metal and an n-type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S<\Phi_M$). An n-type semiconductor is one in which electrons are the majority charge carriers (in p-type semiconductors, holes are the majority charge carrier). As shown in FIG. 3, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor 310 to the metal 320 when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) 330 forms near the junction interface 340.

[0039] The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see FIG. 4). The band bending creates an energy barrier (discussed above) that blocks further transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a

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p-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-n-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-p-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

[0040] As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor—interface layer—metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

[0041] This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

[0042] II. Passivation of Semiconductor Surfaces

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[0043] A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

[0044] However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

[0045] Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

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[0046] These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing n- and p-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

[0047] FIG. 5 shows a semiconductor device 510 that contains a semiconductor 530 and an interface layer 520 formed on a surface 540 of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

[0048] The semiconductor 530 contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

[0049] The semiconductor 530 has a surface 540 that is passivated by the interface layer 520. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface 540. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to

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provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor 530 is operable to be electrically coupled with a first voltage associated with the semiconductor device 510 and to conduct electrical current 550 across the passivated surface 540.

[0050] The interface layer 520 is formed on the semiconductor 530 and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

[0051] Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer 520 may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

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[0052] Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface 540.

[0053] In some cases, passivation of the semiconductor surface 540 will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

[0054] III. Forming Interface Layers

[0055] Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

[0056] A. Hydrogen and Fluorine

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[0057] An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

[0058] It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

[0059] An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

[0060] B. Nitrogen

[0061] In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300° C. and about 750° C., which is lower than temperatures conventionally used for Rapid

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Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH_3) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

[0062] According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10−9 Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900° C. and about 1000° C., or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

[0063] Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in

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the vacuum chamber before removal, at a substantially elevated temperature between about 700° C. and 1000° C., or higher.

[0064] Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

[0065] Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

[0066] IV. Diodes Containing Passivated Semiconductor Surfaces

[0067] Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, conductor-semiconductor junction, and multi-material junction are all related and appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

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[0068] As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

[0069] FIG. 6 shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.

[0070] The conductor 630 contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys), and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

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[0071] Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

[0072] Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

[0073] A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

[0074] The semiconductor-interface layer-conductor configuration illustrated in FIG. 6 defines what the present inventors have chosen to call a "passivated Schottky barrier". The passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

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[0075] Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

[0076] To understand why thickness of the interface layer is important, refer briefly to FIG. 8 where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

[0077] Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

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[0078] One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer 620 is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

[0079] Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

[0080] According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

[0081] For example, to make large-barrier diodes, for an n-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a p-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an

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interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

[0082] The use of interface layer 620 thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer 620, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

[0083] The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

[0084] According to one embodiment of the present invention then, the interface layer 620 is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current

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to be transferred across the interface layer.

[0085] There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

[0086] FIG. 7*a*-7*d* show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_S of the semiconductor. In FIG. 7*a*, an unpassivated Schottky barrier 700 is shown. In this example, the Fermi level (E_F) of the metal 730 is pinned in the bandgap of the semiconductor 710. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

[0087] In FIG. 7*b*, the interface layer 720*b* is thick enough to passivate dangling bonds at the surface of the semiconductor 710, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in FIG. 7*c*, when the interface layer 720*c* is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in FIG. 7*d*, when the interface layer 720*d*

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is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately Φ_M=4.1 eV and the electron affinity for Si of approximately χ_S=4.05 eV.

[0088] V. Transistors Containing Passivated Semiconductor Surfaces

[0089] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Pat. No. 6,833,556, issued Dec. 21, 2004, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed Jan. 14, 2003 by the present inventors, and assigned to the assignee of the present invention.

[0090] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n+-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in FIG. 7*d*). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0091] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide—semiconductor junction a Schottky barrier is formed

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which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

[0092] Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

[0093] The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

[0094] In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

[0095] Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described

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herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

CLAIMS

What is claimed is:

1. An electrical junction, comprising a region in a semiconductor substrate, a metal electrical contact to said region, and an interface layer between said region and said metal electrical contact, said region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising a metal oxide in contact with said metal electrical contact and a semiconductor oxide in contact with said region in the semiconductor substrate.

2. The electrical junction of claim 1, wherein the semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

3. The electrical junction of claim 2, wherein the semiconductor oxide has a thickness of approximately 0.1 nm to 5 nm.

4. The electrical junction of claim 1, wherein said region in the semiconductor substrate comprises a source or drain of a transistor.

5. The electrical junction of claim 1, wherein said interface layer has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region.

6. The electrical junction of claim 1, wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than 10 Ω-μm^2.

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7. The electrical junction of claim 1, wherein said metal electrical contact comprises an alloy of a metal.

8. The electrical junction of claim 1, wherein said metal oxide comprises an oxide of said metal electrical contact.

9. The electrical junction of claim 8, wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

10. The electrical junction of claim 1, wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

11. The electrical junction of claim 1, wherein said metal oxide comprises an oxide of titanium.

12. The electrical junction of claim 11, wherein said semiconductor oxide comprises an oxide of silicon.

13. The electrical junction of claim 12, wherein said semiconductor oxide comprises silicon dioxide.

14. The electrical junction of claim 12, wherein said region in the semiconductor substrate comprises an n-type doped source or drain of a transistor.

15. The electrical junction of claim 1, wherein said metal electrical contact comprises titanium.

16. The electrical junction of claim 1, wherein said metal electrical contact comprises tungsten.

17. An electrical junction, comprising:

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a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor.

18. The electrical junction of claim 17, wherein said metal electrical contact includes titanium.

19. The electrical junction of claim 17, wherein said metal electrical contact includes tungsten.

20. The electrical junction of claim 17, wherein said semiconductor comprises silicon.

21. The electrical junction of claim 18, wherein said semiconductor comprises silicon.

22. The electrical junction of claim 19, wherein said semiconductor comprises silicon.

23. A semiconductor device, comprising:

a semiconductor region,

a metal electrical contact to said semiconductor region, and

an interface layer disposed between and in contact with said semiconductor region and said metal electrical contact, said semiconductor region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor region.

24. The semiconductor device of claim 23, wherein said metal electrical contact includes titanium.

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25. The semiconductor device of claim 23, wherein said metal electrical contact includes tungsten.

26. The semiconductor device of claim 23, wherein said semiconductor region comprises silicon.

27. The semiconductor device of claim 24, wherein said semiconductor region comprises silicon.

28. The semiconductor device of claim 25, wherein said semiconductor region comprises silicon.

29. An electrical junction, comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer being less than 1 nm thick and comprising an oxide of the semiconductor.

30. The electrical junction of claim 29, wherein the metal electrical contact comprises titanium.

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ABSTRACT

An electrical device in which an interface layer is disposed in between and in contact with a conductor and a semiconductor.

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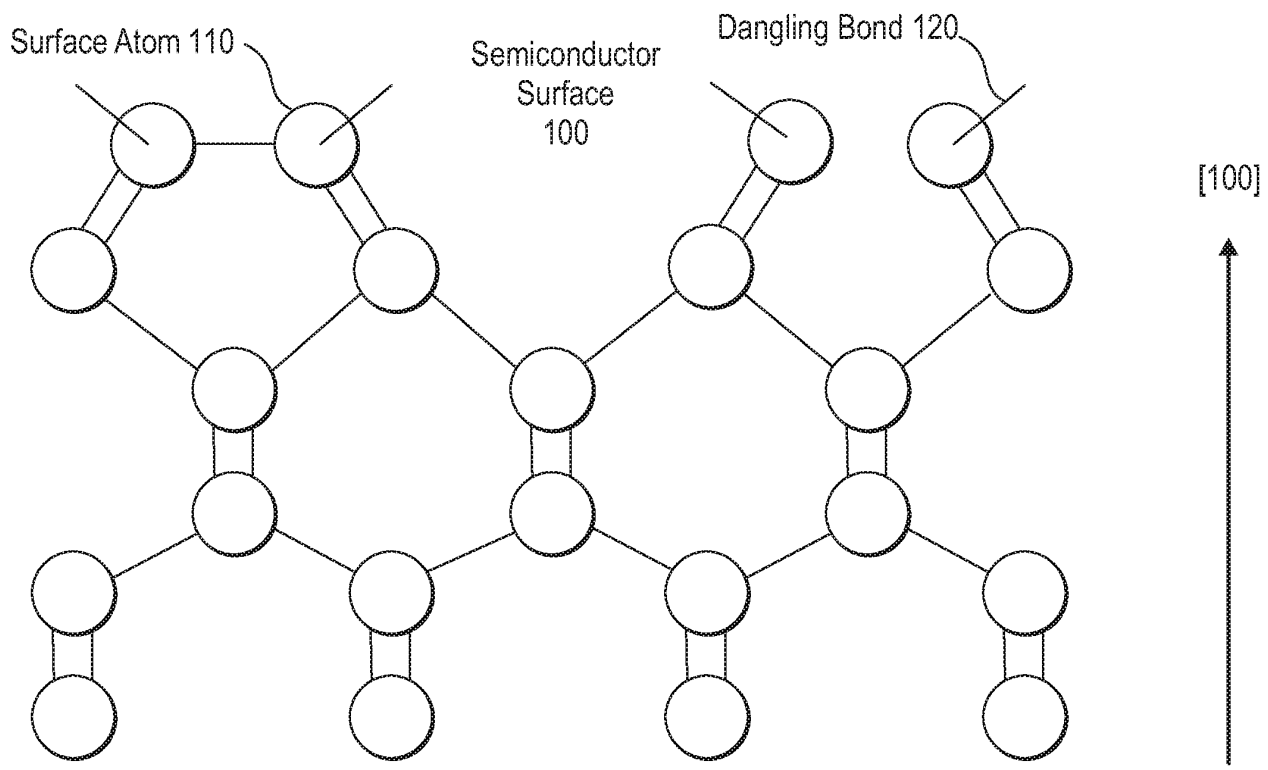
Surface Atom 110
Semiconductor Surface 100
Dangling Bond 120
[100]

Fig. 1

Energy Scales for Metal - Semiconductor Junctions

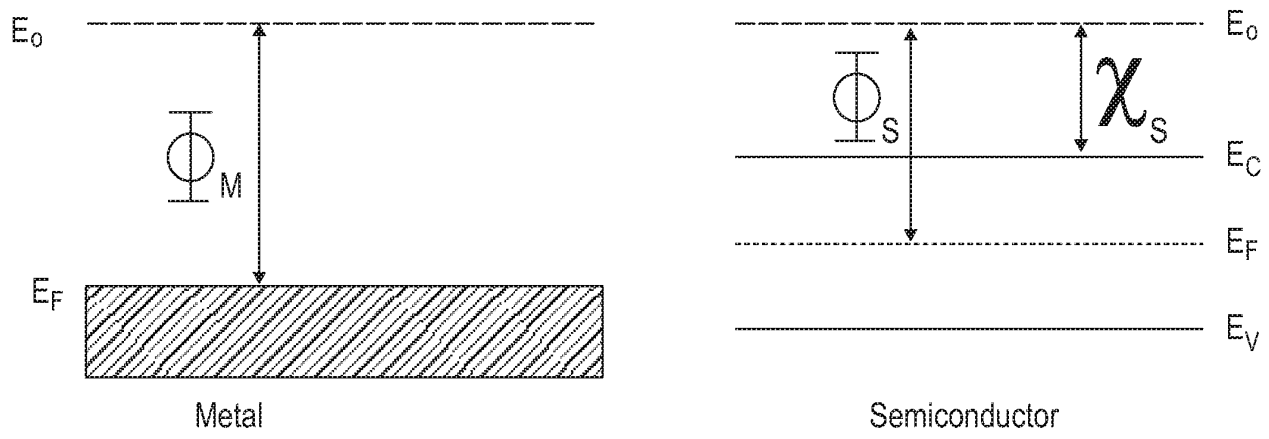

Fig. 2

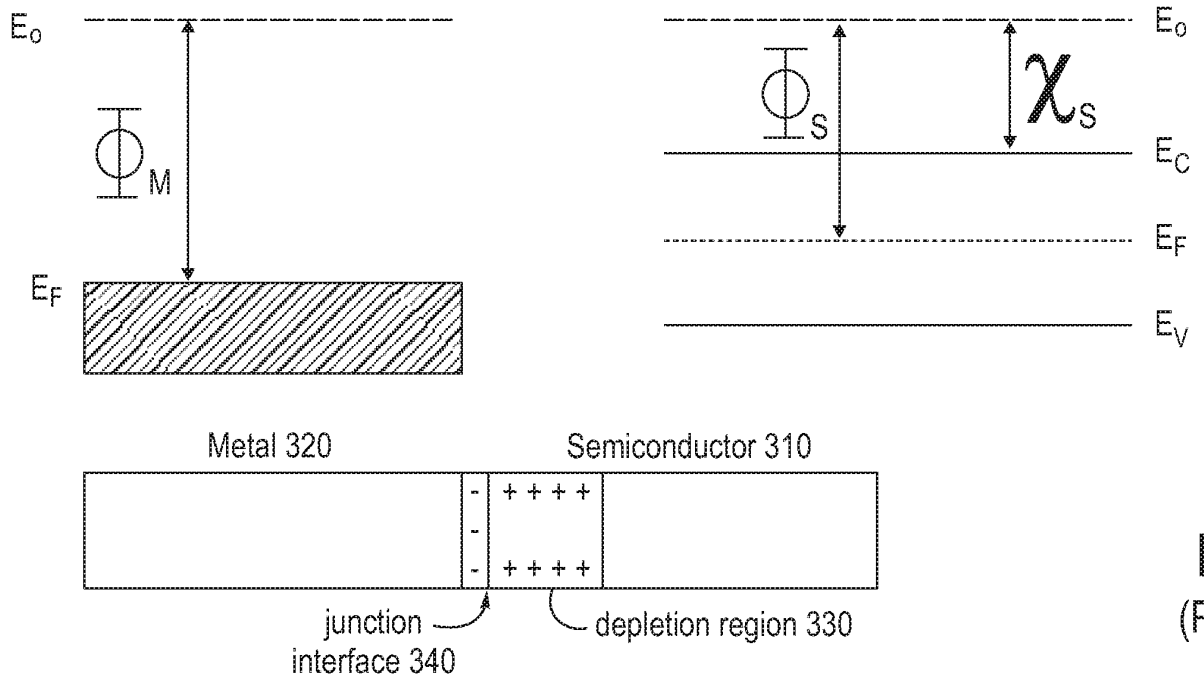

Fig. 3
(Prior Art)

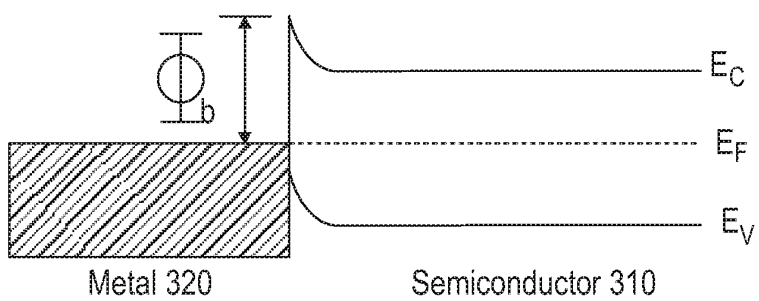

Fig. 4
(Prior Art)

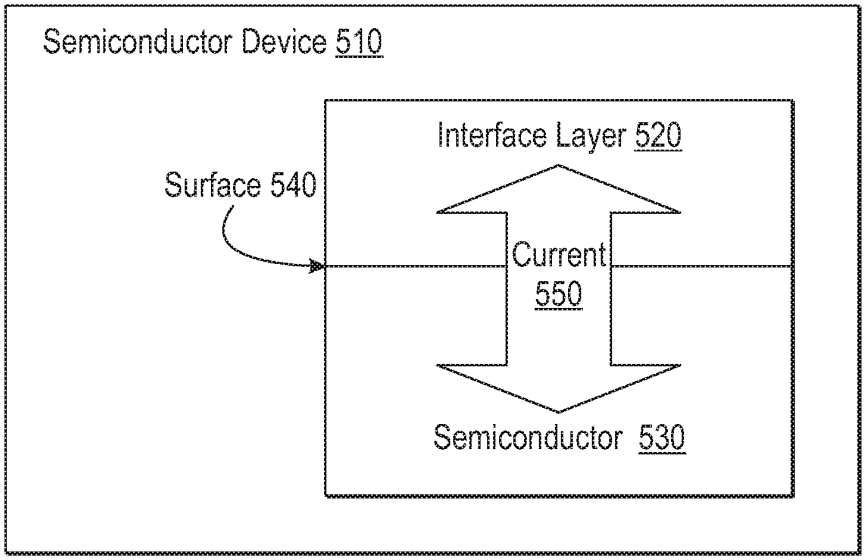
Semiconductor Device 510
Interface Layer 520
Surface 540
Current
550
Semiconductor 530

Fig. 5

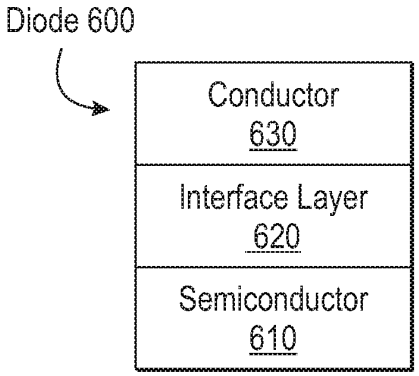
Diode 600
Conductor
630
Interface Layer
620
Semiconductor
610

Fig.6

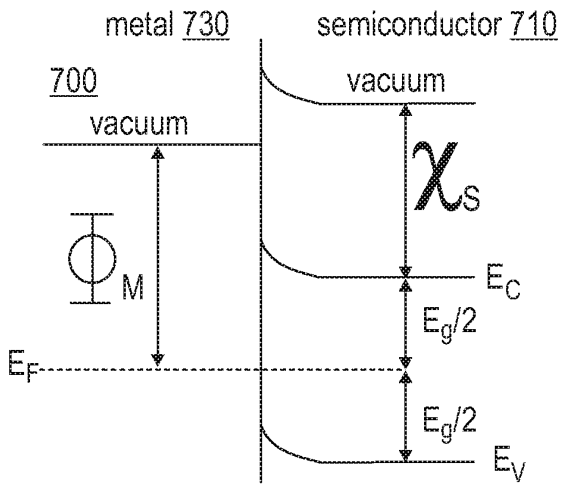

Fig. 7a

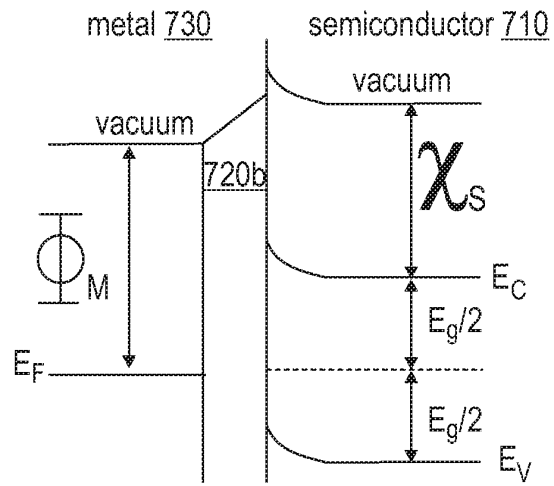

Fig. 7b

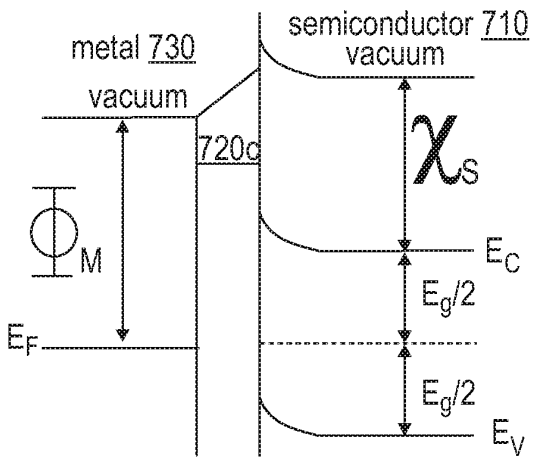

Fig. 7c

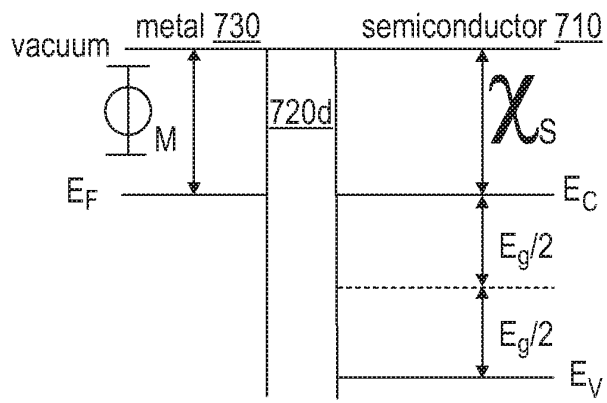

Fig. 7d

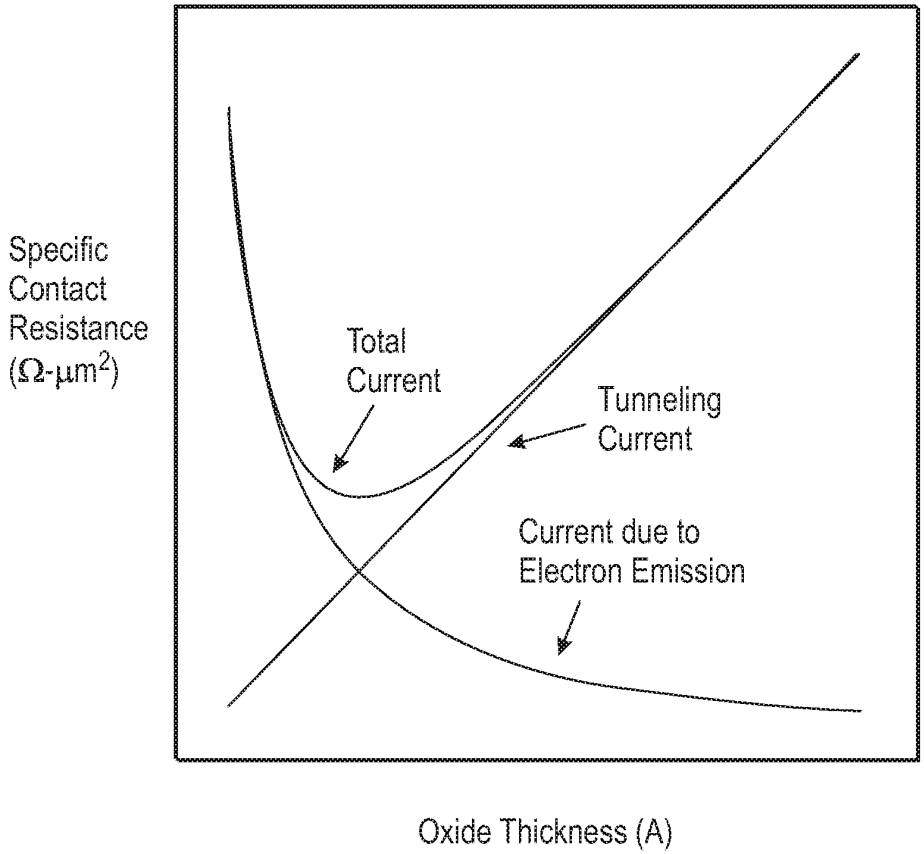
Specific
Contact
Resistance
(Ω-μm²)
Total
Current
Tunneling
Current
Current due to
Electron Emission
Oxide Thickness (A)

Fig. 8

Docket No.: 40003771-0003-473

Combined Declaration and Assignment for Utility and Design Patent Applications

DECLARATION

As a below named inventor, I hereby declare that:

I believe I am the original inventor or an original joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

Insert Title:	**Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions**

the application of which is attached hereto unless the following is checked

☐ was filed on _____ as United States Application Number _____ and was filed on _____ as PCT International Application Number _____ and was amended on _____ (if applicable).

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under section 1001 of title 18 by fine or imprisonment of not more than 5 years, or both.

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the adequacy and receipt of which is hereby acknowledged by the undersigned inventor(s) (hereinafter ASSIGNOR) by

Insert Assignee(s) Name/Address:	Acorn Technologies, Inc. 330 Wilshire Boulevard, 2nd Floor Santa Monica, CA 90401

(hereinafter ASSIGNEE), the undersigned ASSIGNOR hereby sells, assigns and transfers to ASSIGNEE the entire and exclusive right, title and interest to the above-identified application (e.g., provisional or non-provisional) and all Letters Patent of the United States to be obtained therefore on said application or any continuation, divisional, substitute, reissue , reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof for the full term or terms for which the same may be granted.

The ASSIGNOR agrees to execute all papers necessary in connection with the application and any continuation, divisional, reissue, reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof and also to execute separate assignments in connection with such applications as the ASSIGNEE may deem necessary or expedient.

The ASSIGNOR agrees to execute all papers necessary in connection with any interference, litigation, or other legal proceeding which may be declared concerning this application or any continuation, divisional, reissue or reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof or Letters Patent or reissue patent issued thereon and to cooperate with the ASSIGNEE in every way possible in obtaining and producing evidence and proceeding with such interference, litigation, or other legal proceeding.

The ASSIGNOR sells, assigns and transfers to said ASSIGNEE the entire and exclusive right, title and interest to the application(s) and the invention(s) disclosed therein for the United States of America and all countries foreign to the United States and do hereby authorize said ASSIGNEE to apply for patents therefore in its own name in countries where such procedure is proper and to claim the priority right under the International Convention and agrees to execute all papers

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necessary in connection with applications for such patents and any continuation, divisional, substitute, reissue or reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof and also execute separate assignments in connection with such applications as the ASSIGNEE may deem necessary or expedient.

Hereby executed by the undersigned on the date opposite the undersigned name:

Legal Name of inventor ⇨ Daniel E. Grupp Date: 17 NOV 2012

Inventor's Signature ⇨

Legal Name of inventor ⇨ Daniel J. Connelly Date:

Inventor's Signature ⇨

Docket No.: 40003771-0003 -473

Combined Declaration and Assignment for Utility and Design Patent Applications

DECLARATION

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I believe I am the original inventor or an original joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

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the application of which is attached hereto unless the following is checked

☐ was filed on _____ as United States Application Number _____ and was filed on _____ as PCT International Application Number _____ and was amended on _____ (if applicable).

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The ASSIGNOR agrees to execute all papers necessary in connection with any interference, litigation, or other legal proceeding which may be declared concerning this application or any continuation, divisional, reissue or reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof or Letters Patent or reissue patent issued thereon and to cooperate with the ASSIGNEE in every way possible in obtaining and producing evidence and proceeding with such interference, litigation, or other legal proceeding.

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necessary in connection with applications for such patents and any continuation, divisional, substitute, reissue or reexamination, supplemental examination, inter partes review, post grant review, or other procedures thereof and also execute separate assignments in connection with such applications as the ASSIGNEE may deem necessary or expedient.

Hereby executed by the undersigned on the date opposite the undersigned name:

Legal Name of inventor ⇨ Daniel E. Grupp Date: _____

Inventor's Signature ⇨ _____

Legal Name of inventor ⇨ Daniel J. Connelly Date: 11 Oct 2012

Inventor's Signature ⇨ _____

Legal Name of inventor ⇨ _____ Date: _____

Inventor's Signature ⇨ _____

Legal Name of inventor ⇨ _____ Date: _____

Inventor's Signature ⇨ _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Daniel E. Grupp

Application No.: Not Yet Assigned
Filed: Herewith

Examiner: Not Yet Assigned
Art Unit: Not Yet Assigned

Docket No.: 3771-0003-DC10

Customer No.: 27571

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g. copies of U.S. patents and U.S. published patent applications that need not be included and copies of Non Patent Literature documents that were previously provided in parent application nos. 13/552,556 filed 7/18/2012 and 13/022,522 filed 2/7/2011). This IDS and IDS Citation Form are being submitted before the mailing of a First Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account No. 50-5798.

Respectfully submitted,

Date: January 23, 2018

/Tarek N. Fahmi/
Tarek N. Fahmi, Reg. No. 41,402

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Complete if Known

Application Number	
Filing Date	
First Named Inventor	Daniel E. Grupp
Art Unit	
Examiner Name	

Attorney Docket No: 3771-0003-DC10

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		3513366	05/19/1970	CLARK	
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Application Number	
Filing Date	
First Named Inventor	Daniel E. Grupp
Art Unit	
Examiner Name	

Sheet	2	**of**	12	**Attorney Docket No:** 3771-0003-DC10

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First Named Inventor	Daniel E. Grupp
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Sheet	3	**of**	12	**Attorney Docket No:** 3771-0003-DC10

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				Application Number	
				Filing Date	
				First Named Inventor	Daniel E. Grupp
				Art Unit	
				Examiner Name	
Sheet	4	**of**	12	**Attorney Docket No:** 3771-0003-DC10	

		20050093027	05/05/2005	GRUPP; et al.	
		20110092047	04/21/2011	GAINES; et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		EP 0295490 A1	12/21/1988	IBM		
		EP 0789388 A2	08/13/1997	AGENCY INDUSTRIAL SCIENCE AND TECHNOLOGY		
		WO 2004/015782 A1	02/19/2004	ACORN TECHNOLOGIES, INC.		
		WO 2004/030104 A1	04/08/2004	ACORN TECHNOLOGIES, INC.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
		Acorn Technologies, Inc., International Application No.: PCT/US2012/060893 filed 18 October 2012, ISA/US, International Search Report and Written Opinion, 11 December 2012, 23 pages.	
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				First Named Inventor	Daniel E. Grupp
				Art Unit	
				Examiner Name	
Sheet	5	**of**	12	**Attorney Docket No:** 3771-0003-DC10	

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Sheet	6	**of**	12	**Attorney Docket No:** 3771-0003-DC10	

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2018-01-23
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENDFEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: TAREK FAHMI
TAREK N. FAHMI, APC
84 W. SANTA CLARA ST., SUITE 550
SAN JOSE, CA 95113

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day month year)* 11 DEC 2012
Applicant's or agent's file reference 400037710017PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2012/060893	International filing date *(day month year)* 18 October 2012
Applicant ACORN TECHNOLOGIES, INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 Telephone No. PCT OSP: 571-272-7774

Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: TAREK FAHMI
TAREK N. FAHMI, APC
84 W. SANTA CLARA ST., SUITE 550
SAN JOSE, CA 95113

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day month year)*
Applicant's or agent's file reference 400037710017PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2012/060893	International filing date *(day month year)* 18 October 2012
Applicant ACORN TECHNOLOGIES, INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

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   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 Telephone No. PCT OSP: 571-272-7774

Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 400037710017PCT	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2012/060893	International filing date *(day/month/year)* 18 October 2012	(Earliest) Priority Date *(day/month/year)* 23 November 2011
Applicant ACORN TECHNOLOGIES, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 4
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/060893

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/20 (2012.01)
USPC - 438/606
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/20, 21/28, 21/205, 21/285, 21/318, 21/762, 21/765, 33/28, 33/30 (2012.01)
USPC - 148/33.5; 257/14, E21.097, E21.54, E21.108, E21.546, 344, 407, 408, 412, 592, 929; 438/3, 424, 603-607

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent, Google Patents and Public AppFT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2005/0104137 A1 (FAULKNER et al) 19 May 2005 (19.05.2005) entire document	1, 3-12, 23-25, 27 --- 2, 13-22, 26, 28-30
Y	US 2011/0092047 A1 (GAINES et al) 21 April 2011 (21.04.2011) entire document	2, 22, 28-30
Y	US 4,843,029 A (JOYCE et al) 27 June 1989 (27.06.1989) entire document	13-21, 26

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 November 2012	11 DEC 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: 866-877-4883 5
TAREK N. FAHMI, APC
84 W. SANTA CLARA ST., SUITE 550
30 S. 17TH STREET
SAN JOSE, CA 95113

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)* 11 DEC 2012

Applicant's or agent's file reference	FOR FURTHER ACTION
400037710017PCT	See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2012/060893	18 October 2012	23 November 2011

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - H01L 21/20 (2012.01)
USPC - 438/606

Applicant ACORN TECHNOLOGIES, INC.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	29 November 2012	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/060893

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

   ☐ on paper

   ☐ in electronic form

   b. (time)

   ☐ in the international application as filed

   ☐ together with the international application in electronic form

   ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY	International application No. PCT/US2012/060893

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	2, 4-6, 12-23, 26-30	YES
	Claims	1, 3, 7-11, 24, 25	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-30	NO
Industrial applicability (IA)	Claims	1-30	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1, 3, 7-11, 24, and 25 lack novelty under PCT Article 33(2) as being anticipated by Faulkner et al.

Regarding claim 1, Faulkner et al. teach an electrical contact (semiconductor device or transistor, Claim 1; Paras. [0022]-[0027]), comprising a metal (metal layer 42, Para. [0077]; Figs. 2a-2d; Claims 1 and 6) and a group IV semiconductor (layer 26 may contain silicon, Figs. 2a-2d; Claim 1; Paras. [0073]-[0075]) separated by one of a monolayer of group V atoms, (ii) a monolayer of group III atoms, or (iii) one or more bi-layers, each bi-layer consisting of one monolayer of group V atoms and one monolayer of group III atom at an interface between the metal and the group IV semiconductor (layer 26 is separated from metal 42 by interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d), the atoms of the monolayer of group V or group III atoms or of each bi-layer of group V and group III atoms being in epitaxial alignment with a lattice structure of the semiconductor (the interfacial III-VI layered compound may be approximately epitaxially aligned with the underlying {111} semiconductor, Paras. [0024];[0027];[0031];[0062];[0067];[0076]).

Regarding claim 3, Faulkner et al. teach the contact of claim 1, wherein the metal comprises atoms of a different metallic element than the monolayer of group III metal atoms (the metal may comprise Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, Paras. [0063];[0077]).

Regarding claim 7, Faulkner et al. teach the contact of claim 1, wherein the group III atoms comprise any one or more of aluminum, gallium, indium, or alloys of aluminum, gallium and/or indium (elements from Groups IIIA-B include B, Al, Sc, Ga, Y, In, La, Tl and Ac, Para. [0023]).

Regarding claim 8, Faulkner et al. teach the contact of claim 1, wherein one monolayer of group III atoms is immediately adjacent the surface of the group IV semiconductor (layer 26 may contain silicon that is immediately adjacent interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0073]-[0076]; Figs. 2a-2d).

Regarding claim 9, Faulkner et al. teach the contact of claim 1, wherein one monolayer of group V atoms is immediately adjacent the surface of the group IV semiconductor (layer 26 may contain silicon that is immediately adjacent interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0073]-[0076]; Figs. 2a-2d).

Regarding claim 10, Faulkner et al. teach the contact of claim 1, wherein a surface of the group IV semiconductor at the interface is a {111} oriented surface or a {100} oriented surface (layer 26 may be a silicon containing {111} orientated surface, Figs. 2a-2d; Claim 1; Paras. [0073]-[0075]).

Regarding claim 11, Faulkner et al. teach the contact of claim 1, and a method of forming the contact (a method of forming a channel contact, Claim 13) by introducing at least the monolayer of group V atoms or the monolayer of group III atoms or the bi-layer of group V atoms and group III atoms at the interface between the metal (layer 26 is separated from metal 42 by interfacial layer 40, which may be a deposited monolayer or a bilayer of group III-VI compound, Claim 13; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d) and the group IV semiconductor (layer 26 may contain silicon, Figs. 2a-2d; Claim 13; Paras. [0073]-[0075]).

Regarding claim 24, Faulkner et al. teach the contact of claim 1, wherein one or more bi-layers of one monolayer of group V atoms and one monolayer of group III atoms are at the interface (layer 26 is separated from metal 42 by interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d) and each atomic layer of each bi-layer is in epitaxial alignment with one another and with the semiconductor lattice (the interfacial III-VI layered compound may be approximately epitaxially aligned with each other and the underlying {111} semiconductor, Paras. [0024];[0027];[0031];[0062];[0067];[0076]).

Regarding claim 25, Faulkner et al. teach an electrical contact (semiconductor device or transistor, Claim 1; Paras. [0022]-[0027]), comprising a metal (metal layer 42, Para. [0077]; Figs. 2a-2d; Claims 1 and 6) and a group IV semiconductor (layer 26 may contain silicon, Figs. 2a-2d; Claim 1; Paras. [0073]-[0075]) separated by ONE or both of a monolayer of epitaxially aligned group VI atoms (layer 26 is separated from metal 42 at the interface by epitaxially aligned interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d) and a monolayer of epitaxially aligned group II atoms at an interface between the metal and the semiconductor.

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Claims 4-6, 12, 23, and 27 lack an inventive step under PCT Article 33(3) as being obvious over Faulkner et al.

Regarding claim 4, Faulkner et al. teach the contact of claim 3, Faulkner et al. do not explicitly disclose wherein the metal comprises ruthenium, tantalum nitride or titanium nitride. However, Faulkner et al. teach the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]) and the use of metals, such as Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, (Paras. [0063];[0077]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a titanium compound as desired, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a metal of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Faulkner et al., Para. [0023]).

Regarding claim 5, Faulkner et al. teach the contact of claim 1, Faulkner et al. do not explicitly disclose wherein the group IV semiconductor comprises any of germanium, silicon, an alloy of silicon and germanium, an alloy of germanium and tin, an alloy of silicon with carbon, a compound of silicon and carbon, an alloy of germanium with carbon, a compound of germanium and carbon. However Faulkner et al. teaches the use of Group IV semiconductors in the interfacial layer as pure compounds or alloys of pure compounds (Para. [0023]) and that the semiconductor channel may contain Si, Ge, C; an alloy of Ge and Si; an alloy of Si and C; an alloy of Ge and C; or an alloy of Ge, Si, and C (Claim 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a group IV metal or an alloy thereof, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a Group IV semiconductor in the interfacial layer as pure compounds or alloys of pure compounds (Faulkner et al., Para. [0023]).

Regarding claim 6, Faulkner et al. teach the contact of claim 1, Faulkner et al. do not explicitly disclose wherein the group V atoms comprise any one of nitrogen, phosphorus, arsenic and antimony; or a mixture of any two or more of nitrogen, phosphorus, arsenic and antimony atoms. However Faulkner et al. teaches the use of Group V semiconductors in the interfacial layer as pure compounds or alloys of pure compounds (Para. [0023]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a group V metal or an alloy thereof, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a Group III-VI semiconductor in the interfacial layer as pure compounds or alloys of pure compounds (Faulkner et al., Para. [0023]).

Regarding claim 12, Faulkner et al. teach the method of claim 11, wherein a oriented surface of the group IV semiconductor (Si surface of layer 26, Paras. [0075]-[0076]) is etched with a crystallographically selective etch (etched with an etch for selective crystallographic orientation, Paras. [0069]-[0076]) to reveal and expose multiple {111} oriented semiconductor crystal facets (exposing {111} surfaces, Paras. [0069]-[0076]); the at least monolayer of group V atoms is formed on the {111} facets (the interfacial III-VI monolayer compound may be formed on the {111} semiconductor with approximate epitaxial alignment with the underlying, Paras. [0024];[0027];[0031];[0062]; [0069]-[0076]). Faulkner et al. do not explicitly disclose a {110} oriented surface and that the monolayer of group III atoms is subsequently deposited on the monolayer of group V atoms. However, Faulkner et al. teach that other surface orientations are possible (Para. [0071]), depositing bilayers of atoms with an atom of one group, such as Group III, is deposited and then capped with an atom of another group, such as Group VI (Paras. [0058]-[0062]) and depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surfaces so as to be epitaxially aligned therewith(Claim 13; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to modify a {110} surface and the deposition steps by depositing a group III atom monolayer on a monolayer of group V atoms, since selection of a known material on the basis of its suitability for an intended use and any order of process steps which did not result in a new or unexpected result would involve only routine skill in the art. The motivation for doing so would be to deposit an ultra-thin layer of a III-VI monolayered layers on the {110} surface transformed to a {111} surface so as to be epitaxially aligned therewith (Claim 13; Paras. [0031]-[0032]; [0058]-[0062];[0076]; Figs. 2a-2d).

Regarding claim 23, Faulkner et al. teach the contact of claim 1, Faulkner et al. do not explicitly disclose wherein the metal is one of: a metal silicide, a nickel silicide, a composition NiSi, a platinum silicide, a barrier metal consisting of tantalum nitride or titanium nitride or ruthenium, or a ferromagnetic metal comprising one or more of nickel, cobalt, iron and/or gadolinium. However, Faulkner et al. teach the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]) and the use of metals, such as Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, (Paras. [0063];[0077]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a metal or metal nitride as desired, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a metal of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Faulkner et al., Para. [0023]).

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:

Regarding claim 27, Faulkner et al. teach an electrical contact (semiconductor device or transistor, Claim 1; Paras. [0022]-[0027]), comprising a metal (metal layer 42, Para. [0077]; Figs. 2a-2d; Claims 1 and 6) and a group IV semiconductor (layer 26 may contain silicon, Figs. 2a-2d; Claim 1; Paras. [0073]-[0075]) separated by either a monolayer of epitaxially aligned group V atoms or a bi-layer consisting of the monolayer of epitaxially aligned group V atoms and a monolayer of group III atoms at an interface between the metal and the semiconductor (layer 26 is separated from metal 42 at the interface by epitaxially aligned interfacial layer 40, which may be a monolayer or a bilayer of group III-VI compound, Claim 1; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d). Faulkner et al. do not explicitly disclose that the metal is ferromagnetic. However, Faulkner et al. teach the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]) and the use of metals, such as Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, (Paras. [0063];[0077]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a metal as desired, such as a ferromagnetic metal, since selection of a known material on the basis of its suitability for an intended use involves only routine skill in the art. The motivation for doing so would be to select a metal of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Faulkner et al., Para. [0023]).

Claims 2, 22, and 28-30 lack an inventive step under PCT Article 33(3) as being obvious over Faulkner et al. in view of Gaines et al.

Regarding claim 2, Faulkner et al. teach the contact of claim 1, Faulkner et al. do not explicitly disclose wherein the metal comprises atoms of the same metallic element as the monolayer of group III metal atoms. However, Faulkner et al. teach the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]); and, Gaines et al. teach a semiconductor device with substrates of germanium, group III-V and group II-VI metals and deposition layers of buried stressor layers, active layers and sacrificial stressor layers on the substrate (Claim 1; Paras. [0004];[0019];[0031]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a metal with group III atoms. The motivation for doing so would be to select a metal of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Faulkner et al., Para. [0023]).

Regarding claim 22, Faulkner et al. teach the contact of claim 11, Faulkner et al. do not explicitly disclose wherein after forming the monolayer of group V atoms and the monolayer of group III atoms, further metal atoms are deposited on the group III atoms, the further atoms being of a same metallic element as the monolayer of group III atoms or atoms of a metal element different from the monolayer layer of group III atoms. However, Faulkner et al. teach depositing bilayers of atoms with an atom of one group, such as Group III, is deposited and then capped with an atom of another group, such as Group VI (Paras. [0058]-[0062]) and depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surfaces so as to be epitaxially aligned therewith (Claim 13; Paras. [0031]-[0032]; [0060]-[0062];[0076]; Figs. 2a-2d); and, Gaines et al. teach a multiple layer device (Paras. [0027]-[0030]; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit additional layers of any of the group III-VI elements as monolayers one on top another in the desired configuration, as taught by Gaines et al. The motivation for doing so would be to deposit the group III-VI elements in monolayers to desired thickness (Faulkner et al., Paras. [0020]-[0021]; [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d).

Regarding claim 28, Faulkner et al. teach a method of forming an electrical contact (a method of forming a channel contact, Claim 13), comprising depositing, on a surface of a group IV semiconductor, which has been prepared so as to include atoms of a first group V material near the surface (the interfacial III-VI monolayer compound may be formed on the prepared {111} semiconductor silicon surface with approximate epitaxial alignment with the underlying surface, Paras. [0024];[0027];[0031];[0062];[0069]-[0076]), the atoms of the group V material being epitaxially aligned with a lattice structure of the semiconductor (the interfacial III-VI layered compound may be approximately epitaxially aligned with the underlying {111} semiconductor, Paras. [0024];[0027];[0031];[0062];[0067];[0076]), and depositing a metal on the monolayer of the group V material (the metal is deposited on the monolayer or bi-layered interfacial layer, Paras. [0024];[0027];[0031];[0062];[0077]), there being formed between the atoms of the group V material dipoles (the metal is deposited on the interfacial interfacial III-VI layer, Paras. [0024];[0027];[0031];[0062];[0077]). Faulkner et al. do not explicitly disclose a monolayer of a second group V material and that the metal has image charges. However, Faulkner et al. teach depositing bilayers of atoms with an atom of one group, such as Group III, is deposited and then capped with an atom of another group, such as Group VI (Paras. [0058]-[0062]), depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surfaces so as to be epitaxially aligned therewith (Claim 13; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d) and that the selection of the metal is based on one or more metals of a work function appropriate for the type of the transistor, such as a relatively low work function for an n-channel transistor, or a relatively high work function for a p-channel transistor, (Para. [0023]) and the use of metals, such as Au, Cu, Ag, Sn, Pt, Fr, Pd, W and/or Ti, (Paras. [0063];[0077]); and, Gaines et al. teach a multiple layer device (Paras. [0027]-[0030]; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to select a metal that would exhibit the appropriate charge and to deposit additional layers of any of the group III-VI elements as monolayers one on top another in the desired configuration, as taught by Gaines et al. The motivation for doing so would be to deposit the group III-VI elements in monolayers to desired thickness with the appropriately selected metal (Faulkner et al., Paras. [0020]-[0023]; [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d).

Supplemental Box

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Regarding claim 29, Faulkner et al. in view of Gaines et al. teach the contact of claim 28, Faulkner et al. do not explicitly disclose wherein the first group V material and the second group V material are the same group V material. However, Faulkner et al. teach depositing bilayers of atoms with an atom of one group, such as Group III, is deposited and then capped with an atom of another group, such as Group VI (Paras. [0058]-[0062]) and depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surfaces so as to be epitaxially aligned therewith (Claim 13; Paras. [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d); and, Gaines et al. teach a multiple layer device (Paras. [0027]-[0030]; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit additional layers of any of the group III-VI elements as monolayers one on top another in the desired configuration, as taught by Gaines et al. The motivation for doing so would be to deposit the group III-VI elements in monolayers to desired thickness (Faulkner et al., Paras. [0020]-[0021]; [0031]-[0032];[0060]-[0062];[0076]; Figs. 2a-2d).

Regarding claim 30, Faulkner et al. in view of Gaines et al. teach the contact of claim 28, Faulkner et al. teach wherein the group IV semiconductor is prepared by depositing the first group V material on the semiconductor (the interfacial III-VI monolayer compound may be deposited on the prepared {111} semiconductor silicon surface with approximate epitaxial alignment with the underlying surface, Paras. [0024];[0027];[0031];[0062];[0069]-[0076]; Claim 13) at a sufficiently high temperature that atoms of the first group V material enter the semiconductor (the interfacial III-VI monolayer is deposited at a sufficiently high temperature so as to be epitaxially aligned with the semiconductor, Claim 13; Paras. [0024];[0027];[0031];[0062];[0069]-[0076]).

Claims 13-21 and 26 lack an inventive step under PCT Article 33(3) as being obvious over Faulkner et al. in view of Joyce et al.

Regarding claim 13, Faulkner et al. teach the method of claim 11, Faulkner et al. do not explicitly disclose wherein the monolayer of group V atoms is produced by way of a vapor deposition process that includes exposing the group IV semiconductor to a vapor flux of the group V atoms or a flux of homonuclear molecules of the group V element generated by thermally evaporating a source of the group V element, or by a chemical reaction. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach a method of manufacturing a semiconductor device with epitaxial growth of a group II-V material (Claim 1; Col. 9, Lines 51-65) with the deposition of a group V material by vapor flux (Col. 5, Line 3-Col. 7, Line 53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom by the processes taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as vapor flux (Joyce et al., Col. 5, Line 3-Col. 7, Line 53).

Regarding claim 14, Faulkner et al. in view of Joyce et al. teach the method of claim 13, Faulkner et al. do not explicitly disclose wherein the flux of group V atoms/molecules is either a flux of arsenic molecules of composition As4 or As2 and the molecular flux is created by thermal evaporation of an elemental arsenic source in a Knudsen cell. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the flux of group V atoms/molecules is either a flux of arsenic molecules of composition As4 or As2 (flux of As2 or As4 atoms, Col. 6, Line 30-Col. 7, Line 15) and the molecular flux is created by thermal evaporation of an elemental arsenic source in a Knudsen cell (the arsenic source is evaporated in a Knudsen cell, Col. 5, Line 3-Col. 7, Line 53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom by the processes taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as vapor flux in a Knudsen cell (Joyce et al., Col. 5, Line 3-Col. 7, Line 53).

Regarding claim 15, Faulkner et al. teach the method of claim 11, Faulkner et al. do not explicitly disclose wherein the group V element atoms are deposited on the semiconductor surface by decomposition of a vapor phase compound of the group V element. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the group V element atoms are deposited on the semiconductor surface by decomposition of a vapor phase compound of the group V element (elements, such as group V, are deposited on the surface by decomposition of the vapor phase, Col. 3, Lines 35-57; Col. 6, Line 30-Col. 7, Line 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom by the processes taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as decomposition vapor flux in a Knudsen cell (Joyce et al., Col. 3, Lines 35-57; Col. 5, Line 3-Col. 7, Line 53).

Regarding claim 16, Faulkner et al. in view of Joyce et al. teach the method of claim 15, Faulkner et al. do not explicitly disclose wherein the compound of the group V element is a hydride of the group V element, and the group V hydride gas comprises one of ammonia, phosphine, arsine, or stibine. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the compound of the group V element is a hydride of the group V element (group V compounds as hydrides, Col. 9, Line 66-Col. 10, Line 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom hydrides, as taught by Joyce et al., such as ammonia, phosphine, arsine, or stibine. The motivation for doing so would be to deposit the layers by known deposition processes, such as as group V metal hydrides (Joyce et al., Col. 9, Line 66-Col. 10, Line 7).

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Regarding claim 17, Faulkner et al. in view of Joyce et al. teach the method of claim 16, Faulkner et al. do not explicitly disclose wherein the group V hydride gas comprises arsine (AsH4) and the surface of the semiconductor is heated to a temperature in the range 675 °C to 725 °C. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach heating the substrate to a temperature for desired growth, such as 650 °C (Col. 6, Line 55-Col. 7, Line 15) and that group V material hydrides, such as As2 and As4, may be used (Col. 6, Line 55-Col. 7, Line 15; Col. 9, Line 66-Col. 10, Line 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom hydride at temperatures sufficient to heat the substrate for the desired growth, as taught by Joyce et al., such as a substrate at a temperature of 675 °C to 725 °C subjected to a group V hydride, such as AsH4. The motivation for doing so would be to deposit the layers by known deposition processes, such as through use of a group V metal hydride at sufficient substrate growth temperatures (Joyce et al., Col. 6, Line 55-Col. 7, Line 15; Col. 9, Line 66-Col. 10, Line 7).

Regarding claim 18, Faulkner et al. in view of Joyce et al. teach the method of claim 17, Faulkner et al. do not explicitly disclose wherein the semiconductor is silicon and prior to depositing the arsenic atoms, the silicon surface is heated to a sufficiently high temperature in hydrogen gas to remove any silicon oxide or other contamination. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the semiconductor is silicon (the semiconductor is silicon, Col. 9, Lines 51-65) and prior to depositing the arsenic atoms, the silicon surface is heated to a sufficiently high temperature (the substrate is heated to a sufficiently high temperature prior to depositing arsenic atoms, (Col. 6, Line 55-Col. 7, Line 53) in hydrogen gas to remove any silicon oxide or other contamination (in an atmosphere to remove volatile oxides and undesired impurities, Col. 6, Line 10-Col. 7, Line 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to heat the substrate in an atmosphere, such as hydrogen, to remove undesired impurities and volatile oxides, such as silicon oxide, as generally taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as through use of heating of the substrate to remove volatile oxides and impurities (Joyce et al., Col. 6, Line 10-Col. 7, Line 53).

Regarding claim 19, Faulkner et al. in view of Joyce et al. teach the method of claim 15, Faulkner et al. do not explicitly disclose wherein the compound of the group V element is a metalorganic compound of the group V element. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach wherein the compound of the group V element (group V metal, Col. 2, Lines 45-68) is a metalorganic compound of the group V element (metal organic compound of a group V metal, Col. 2, Lines 45-68; Claims 7 and 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to use a metal organic compound of a group V element, as taught by Joyce et al. The motivation for doing so would be to use a group V compound metal organic (Joyce et al., Col. 2, Lines 45-68).

Regarding claim 20, Faulkner et al. in view of Joyce et al. teach the method of claim 19, Faulkner et al. do not explicitly disclose wherein the metalorganic compound of the group V element comprises tertiary butyl arsine (TBA) and the surface of the semiconductor is heated to a temperature in the range 500 °C to 610 °C. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach the use of a group V metal organic (Col. 2, Lines 45-68; Claims 7 and 14) and heating the substrate to a temperature of 650 °C (Col. 6, Line 55-Col. 7, Line 15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to use a metal organic compound of a group V element, as taught by Joyce et al., such as tertiary butyl arsine, and to heat the substrate to a sufficient temperature, such as 650 °C, as taught by Joyce et al. The motivation for doing so would be to use a specific group V compound metal organic and to heat the substrate to sufficient temperatures (Joyce et al., Col. 2, Lines 45-68; Col. 6, Line 55-Col. 7, Line 15).

Regarding claim 21, Faulkner et al. teach the method of claim 12, wherein the semiconductor is silicon (silicon semiconductor, Paras. [0042];[0073]) and prior to depositing the group V atoms (the interfacial III-VI monolayer compound may be formed on the {111} semiconductor with approximate epitaxial aligned with the underlying, Paras. [0024];[0027];[0031];[0062];[0069]-[0076]), the {111} oriented surface is cleaned in situ (Si surface of layer 26 is etched with an etch for selective crystallographic orientation to expose clean {111} surfaces, Paras. [0027];[0069]-[0076]) and the silicon is heated to a sufficiently high temperature to obtain a 7 X 7 reconstruction of the {111} silicon surface (annealed at a temperature sufficient to generate a 7X7 reconstruction of the {111} surfaces, Para. [0027]) after which the silicon is held at a temperature in the range of approximately 20 °C to 750 °C (the deposition is carried out a temperatures from 500 to 875 °C, Paras. [0062];[0076]). Faulkner et al. do not explicitly disclose that during exposure to a vapor flux of the group V atoms or a compound molecular vapor of the group V element. However, Faulkner et al. teach depositing an ultra-thin layer of a III-VI monolayered or bi-layered compound on the {111} surface at elevated temperatures (Claim 13; Para. [0062]); and, Joyce et al. teach that during exposure to a vapor flux of the group V atoms or a compound molecular vapor of the group V element. (depositing by a vapor flux of group V atoms, Col. 5, Line 3-Col. 7, Line 53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faulkner et al. to deposit on the silicon layer a group V atom by the processes taught by Joyce et al. The motivation for doing so would be to deposit the layers by known deposition processes, such as vapor flux (Joyce et al., Col. 5, Line 3-Col. 7, Line 53).

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Regarding claim 26, Faulkner et al. in view of Joyce et al. teach the method of claim 19. Faulkner et al. further teach wherein the group VI atoms comprise any one or more of sulfur, selenium or tellurium (Group VIA elements include O, S, Se, Te and Po, Para. [0023]) and/or the group II atoms comprise zinc or cadmium, or an alloy of zinc and cadmium.

Claims 1-30 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.

Search History:

Limited Classification Search

The Patent Analyst performed a limited classification search within the following US, IPC, ECLA, or F-Term classification areas:

U.S. Class/Subclass(es): 148/33.5; 257/14, E21.097, E21.54, E21.108, E21.546, 344, 407, 408, 412, 592, 929; 438/3, 424, 603-607

IPC (8) Class/Subclass(es): H01L 21/20, 21/28, 21/205, 21/285, 21/318, 21/762, 21/765, 33/28, 33/30 (2012.01)

See Global Search Results.

Global Patent Literature Text Search

The Patent Analyst performed the following global text search, which was not limited by classification but may or may not have been limited by other criteria:

MICROPATENT

47	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current US Class	257014
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
46	9 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
45	2397 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

44	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
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		Years	1836-2012
43	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
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		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
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		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

39	30 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
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		Years	1836-2012
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		Years	1836-2012

34	2 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
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		Years	1836-2012

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		Years	1836-2012

24	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
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		Years	1836-2012

19	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
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		Years	1836-2012
15	197 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L002120
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

14	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L0021765
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
13	24 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L0021318
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
12	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021318
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
11	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021765
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
10	2 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L002120
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

9	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021285
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
8	1 hit	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021205
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
7	132 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L0021205
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
6	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L0021762
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
5	no hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux As4 As2
		Current IPC-R	H01L002128
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

4	56 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L002128
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
3	28 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride flux
		Current IPC-R	H01L0021762
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
2	538 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal nitride
		Current IPC-R	H01L0021762
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012
1	702 hits	Full patent spec.	semiconductor group V epitaxial layer*3 metal
		Current IPC-R	H01L0021762
		Databases	USG USA EPA EPB WO JP DEG DEA DET DEU GBA FRA
		Years	1836-2012

The Patent Analyst searched the following computer accessed text databases:

GOOGLE Search Engine http://www.google.com/intl/en/about/products/index.html

No. of Hits	Text String	Date	Other Limiting Criteria
1	2011/0092047	**11/28/2012**	Google Patents
485	semiconductor group V epitaxial layer metal nitride flux arsenic	**11/28/2012**	Google Patents
21	4843029	**11/28/2012**	Google Patents

Computer Accessed Text Databases Searched

Database: Public AppFT

No. of Hits	Text String	Date	Other Limiting Criteria
1	IN/"harrison walter"	**11/28/2012**	Patent Apps
17	IN/"clifton paul"	**11/28/2012**	Patent Apps
9	IN/"goebel andreas"	**11/28/2012**	Patent Apps
4	IN/"gaines r stockton"	**11/28/2012**	Patent Apps

Date search was completed: 29 November 2012

YLK/BT

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC10

Filed as Small Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	75	75
UTILITY SEARCH FEE	2111	1	330	330
UTILITY EXAMINATION FEE	2311	1	380	380
REQUEST FOR PRIORITIZED EXAMINATION	2817	1	2000	2000
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	10	50	500
INDEPENDENT CLAIMS IN EXCESS OF 3	2201	1	230	230

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous-Filing:				
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	2830	1	70	70
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**3585**

Electronic Acknowledgement Receipt

EFS ID:	31581358
Application Number:	15877837
International Application Number:	
Confirmation Number:	8140
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC10
Receipt Date:	23-JAN-2018
Filing Date:	
Time Stamp:	15:12:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$3585
RAM confirmation Number	012418INTEFSW15135500
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	TrackOne Request	3771-0003-DC10_TrackOne_Request.pdf	114224 ece879be8ee9df64893d74df0c82848144b1eebf	no	2
Warnings:					
Information:					
2	Application Data Sheet	3771-0003-DC10_ADS.pdf	1823889 13e79039911921860ef098cb3a47eede15ef7fbd	no	9
Warnings:					
Information:					
3		3771-0003-DC10_Specification.pdf	198847 68e6480648dbadfab800c1f7f093e2663742ef4f	yes	32

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	27
Claims	28	31
Abstract	32	32

Warnings:					
Information:					
4	Drawings-only black and white line drawings	3771-0003-DC10_Figures.pdf	144859 2b898120e44a0f06e1fbb344198b0666cb77e4d4	no	6
Warnings:					
Information:					
5	Oath or Declaration filed	Exe_Dec-Assign.pdf	173599 7f22e7895f87c1ad1996ccac8c8a3c8e022f0af7	no	4

Warnings:					
Information:					
6	Transmittal Letter	3771-0003-DC10_IDS_Statement.pdf	68179 16897403f3da8836024426a8cee1daddc01321ad	no	2
Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Form (SB08)	3771-0003-DC10_IDS.pdf	234893 3490af67b9dc48e5e8bba3200b5740b207fa94ec	no	12
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
8	Non Patent Literature	3771-0017-PCT_ISR_and_Written_Opinion_mailed_12-24-12.pdf	3198873 22114e67c86087fe4908dd6b6f93cf85a990ecbe	no	23
Warnings:					
Information:					
9	Non Patent Literature	MCKINLEY_1992.pdf	244430 1bf69ce766e60cdb6f9893a5e997cd92197ee3dc	no	4
Warnings:					
Information:					
10	Non Patent Literature	GB1409999-8_Exam_Rpt.pdf	224888 1895f36534674e20858d1b7bef94e14fd9cc12e3	no	5
Warnings:					
Information:					
11	Non Patent Literature	MCKINLEY_1990.pdf	644049 9ea15b3a80022e5a6c5d77afcd615cc45ead9057	no	5
Warnings:					
Information:					
12	Fee Worksheet (SB06)	fee-info.pdf	43032 f85beb311d8e1b237df40d2b2c1a6eba6925a314	no	2
Warnings:					

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Total Files Size (in bytes):	7113762

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82A (07-12)

Approved for use through 11/30/2014. OMB 0651-0035

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NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	15/877,837
Filing Date	01-23-2018
First Named Inventor	Daniel E. Grupp
Title	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
Art Unit	
Examiner Name	
Attorney Docket Number	3771-0003-DC10

SIGNATURE of Applicant or Patent Practitioner

Signature	/Tarek N. Fahmi/	Date	01-23-2018
Name	Tarek N. Fahmi	Telephone	866-877-4883
Registration Number	41402		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

■ *Total of 2 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/AIA/82B (07-12)
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I hereby revoke all previous powers of attorney given in the above-identified patent application.

[X] I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent): 27571

OR

[ ] I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name Registration	Number	Name Registration	Number

Please recognize or change the correspondence address for the above-identified patent to:

[X] The address associated with the above-mentioned Customer Number:

OR

[ ] The address associated with Customer Number:

OR

[ ] Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

SIGNATURE of Applicant for Patent

Signature	Joseph J. Daniele	Date	11/28/2012
Name	Joseph J. Daniele	Telephone	(858) 551-[redacted]/552
Title and Company	Chief Operating Officer, Acorn Technologies, Inc.		

JP

NOTE: This form must be signed by the applicant or applicant's representative in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

[ ] *Total of _____ forms are submitted.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Acorn Technologies, Inc.

Application No./Patent No.: 15/877,837 Filed/Issue Date: 01-23-2018

Titled: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELEC

Acorn Technologies, Inc., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 022077, Frame 0447, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/	01-23-2018
Signature	Date
Tarek N. Fahmi	41402
Printed or Typed Name	Title or Registration Number

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	31582136
Application Number:	15877837
International Application Number:	
Confirmation Number:	8140
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC10
Receipt Date:	23-JAN-2018
Filing Date:	
Time Stamp:	15:43:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	3771-0003-DC10_Executed_POA.pdf	199672 4bddc6df12dcf825a176663fd1137d8209c17c80	no	2

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	3771-0003-DC10_Statement_3-73c.pdf	96141 1c5764728875096db320b37e61576e02dd8980a5	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	295813		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15877837
Filing Date	2018-01-23
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	3771-0003-DC10

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4338616		1982-07-06	BOL	
	2	4566021		1986-01-21	YOKOYAMA	
	3	4999685		1991-03-12	WALDROP; et al.	
	4	5243213		1993-09-07	MIYAZAWA; et al.	
	5	7057333		2006-06-06	VU THIEN; et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20030022474		2003-01-30	GROVER; et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15877837
	Filing Date	2018-01-23
	First Named Inventor	Daniel E. Grupp
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	3771-0003-DC10

	2	20030219965		2003-11-27	CABRAL; et al.			

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15877837
	Filing Date	2018-01-23
	First Named Inventor	Daniel E. Grupp
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	3771-0003-DC10

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2018-01-31
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	31661223
Application Number:	15877837
International Application Number:	
Confirmation Number:	8140
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC10
Receipt Date:	31-JAN-2018
Filing Date:	
Time Stamp:	15:04:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2018-01-31_3771-0003-DC10_IDS.pdf	1035328 81437c6dd625fa4246f17aee49d644976f874b46	no	4

Warnings:

Information:	
Total Files Size (in bytes):	1035328

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/877,837	01/23/2018	2811	1515	3771-0003-DC10	30	4

CONFIRMATION NO. 8140

FILING RECEIPT

27571
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

Date Mailed: 03/06/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

Applicant(s)

Acorn Technologies, Inc., La Jolla, CA;

Power of Attorney: The patent practitioners associated with Customer Number 27571

Domestic Priority data as claimed by applicant

This application is a CON of 15/728,002 10/09/2017
which is a CON of 15/251,210 08/30/2016 PAT 9812542
which is a CON of 15/048,877 02/19/2016 PAT 9905691
which is a CON of 13/552,556 07/18/2012 PAT 9425277
which is a CON of 13/022,522 02/07/2011 PAT 8431469
which is a DIV of 12/197,996 08/25/2008 PAT 7884003
which is a DIV of 11/181,217 07/13/2005 PAT 7462860
which is a CON of 10/217,758 08/12/2002 PAT 7084423

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

GF Exhibit 1130 - 110/196

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 03/01/2018
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/877,837**
Projected Publication Date: 06/14/2018
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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GF Exhibit 1130 - 112/196

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
15/877,837

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	330		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	30 minus 20 =	* 10	x 50 =	500	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1	x 230 =	230			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1515		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/877,837	01/23/2018	Daniel E. Grupp	3771-0003-DC10	8140

27571 7590 03/15/2018
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

EXAMINER

ART UNIT	PAPER NUMBER
2896	

NOTIFICATION DATE	DELIVERY MODE
03/15/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@ascendalaw.com
tarek.fahmi@ascendalaw.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
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Doc Code:
TRACK1.GRANT

Decision Granting Request for Prioritized Examination (Track I or After RCE)	Application No.: 15/877,837

1. THE REQUEST FILED January 23, 2018 IS **GRANTED.**

   The above-identified application has met the requirements for prioritized examination
   A. ☒ for an original nonprovisional application (Track I).
   B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination.** The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

   A. filing a **petition for extension of time** to extend the time period for filing a reply;
   B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims**, or a multiple dependent claim;
   C. filing a **request for continued examination**;
   D. filing a notice of appeal;
   E. filing a request for suspension of action;
   F. mailing of a notice of allowance;
   G. mailing of a final Office action;
   H. completion of examination as defined in 37 CFR 41.102; or
   I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to Cheryl Gibson-Baylor at (571)272-3213, Office of Petitions. In his/her absence, calls may be directed to Brian W. Brown, (571)272-5338.

Cheryl Gibson-Baylor
/Cheryl Gibson-Baylor/
[*Signature*]

Petitions Paralegal Specialist
(Title)

U.S. Patent and Trademark Office
PTO-2298 (Rev. 02-2012)

Office of Petitions: Decision Count Sheet

Mailing Month 3

Application No. 15877837

15877837

For US serial numbers: enter number only, no slashes or commas. Ex: 10123456
For PCT: enter "51+single digit of year of filing+last 5 numbers", Ex. for PCT/US05/12345, enter 51512345

Deciding Official: GIBSON-BAYLOR, CHERYL

Count (1) - Palm Credit 15877837

Decision: GRANT

FINANCE WORK NEEDED
☐ Select Check Box for YES

GRANT

Decision Type: 643 - Track One request

643

Notes:

Count (2)

Decision: n/a

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: NONE

Notes:

Count (3)

Decision: n/a

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: NONE

Notes:

Initials of Approving Official (if required)

If more than 3 decisions, attach 2nd count sheet & mark this box ☐

Printed on: 3/12/2018

Office of Petitions Internal Document - Ver. 5.0

Office of Petitions: Routing Sheet

4700

Application No. 15877837

This application is being forwarded to your office for further processing. A decision has been rendered on a petition filed in this application, as indicated below. For details of this decision, please see the document PET.OP.DEC filed on the same date as this document.

- [x] **GRANTED**
- [ ] **DISMISSED**
- [ ] **DENIED**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/877,837	01/23/2018	Daniel E. Grupp	3771-0003-DC10	8140

27571 7590 04/03/2018
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

EXAMINER
HARRISON, MONICA D

ART UNIT	PAPER NUMBER
2896	

NOTIFICATION DATE	DELIVERY MODE
04/03/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@ascendalaw.com
tarek.fahmi@ascendalaw.com

Office Action Summary	Application No. 15/877,837	Applicant(s) GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/23/18*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-30* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-30* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *1/23/18* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *1/23/18,1/31/18*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Priority

1. This application discloses and claims only subject matter disclosed in prior application no 15/728,002, filed 10/9/17, and names the inventor or at least one joint inventor named in the prior application. Accordingly, this application may constitute a continuation or division. Should applicant desire to claim the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120, 37 CFR 1.78, and MPEP § 211 *et seq.*

2. The present application is a continuation of the previous applications (such as 13/552556). All of the independent claims recite either a semiconductor oxide or oxide of the semiconductor and a metal oxide or oxide of titanium in the interface layer, the pairing of which is not found or contemplated in the parent applications. As such, the claims of 15/877,837 should not be accorded the priority dates. Therefore, the date accorded to the present claims is February 19, 2016. Specifically, the subject matter of independent claim 1 of " said interface layer comprising a metal oxide in contact with said electrical contact and a semiconductor oxide in contact with said region in the semiconductor substrate" is not supported by any of the parent applications from which the present application claims prior to. Therefore, the claims of the present application should not be accorded the priority of the parent applications and is actually a Continuation-In-Part. The claimed subject matter of claim 1 should not be accorded the benefit of the priority filing dates. Additionally, the subject matter of independent claims 17, 23 and 29 also have the same issues of "the interface layer" not being supported by any of the parent applications from which the present application claims prior to. Therefore, the claims of the

present application should not be accorded the priority of the parent applications and is actually a Continuation-In-Part. The claimed subject matter of claims 1, 17, 23 and 29 should not be accorded the benefit of the priority filing dates.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim(s) 1-10 and 15 is/are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Huang et al (US 2014/0117465 A1).

3. Regarding claim 1, Huang et al discloses an electrical junction (Figure 1J), comprising a region (Figure 1J, reference 2) in a semiconductor substrate (Figure 1J, reference 1), a metal electrical contact (Figure 1J, reference 9) to said region (Figure 1J, reference 2), and an interface layer (Figure 1J, references 7 and 8) between said region (Figure 1J, reference 2) and said metal electrical contact (Figure 1J, reference 9), said region (Figure 1J, reference 2) being electrically connected to said metal electrical contact (Figure 1J, reference 9) through said interface layer (Figure 1J, references 7 and 8) and said interface layer (Figure 1J, references 7 and 8) comprising a metal oxide (Figure 1J, reference 8) in contact with said metal electrical

contact (Figure 1J, reference 9) and a semiconductor oxide (Figure 1J, reference 7) in contact with said region (Figure 1J, reference 2) in the semiconductor substrate (Figure 1J, reference 1).

4. Regarding claim 2, Huang et al discloses wherein the semiconductor oxide (Figure 1J, reference 7; paragraph 0033) comprises an oxide of the region (Figure 1J, reference 2) in the semiconductor substrate (Figure 1J, reference 1; paragraph 0027).

5. Regarding claim 3, Huang et al discloses wherein the semiconductor oxide (Figure 1J, reference 7) has a thickness of approximately 0.1 nm to 5 nm (paragraph 0033).

6. Regarding claim 4, Huang et al discloses wherein said region (Figure 1J, reference 2) in the semiconductor substrate (Figure 1J, reference 1) comprises a source or drain (Figure 1J, reference 9) of a transistor (Figure 1J).

7. Regarding claim 5, Huang et al discloses wherein said interface layer (Figure 1J, references 7and 8) has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region.

8. Regarding claim 6, Huang et al discloses wherein said interface layer (Figure 1J, references 7 and 8) is configured to provide a specific contact resistivity between the metal electrical contact (Figure 1J, reference 9) and the region (Figure 1J, reference 2) in the semiconductor (Figure 1J, reference 1) of less than 10 Ω-μm^2.

9. Regarding claim 7, Huang et al discloses wherein said metal electrical contact (Figure 1J, reference 9) comprises an alloy of a metal.

10. Regarding claim 8, Huang et al discloses wherein said metal oxide (Figure 1J, reference 8) comprises an oxide of said metal electrical contact (Figure 1J, reference 9).

11. Regarding claim 9, Huang et al discloses wherein said semiconductor oxide (Figure 1J, reference 7) comprises an oxide of the region (Figure 1J, reference 2) in the semiconductor substrate (Figure 1J, reference 1).

12. Regarding claim 10, Huang et al discloses wherein said semiconductor oxide (Figure 1J, reference 7) comprises an oxide of the region (Figure 1J, reference 2) in the semiconductor substrate (Figure 1J, reference 1).

13. Regarding claim 15, Huang et al discloses wherein said metal electrical contact (Figure 1J, reference 9) comprises titanium (paragraph 0035).

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-13 and 16 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 2014/0117465 A1) in view of Kim et al (US 2015/0001643 A1).

14. Huang et al discloses all of the above claimed subject matter.

However, Huang et al does not disclose wherein said metal oxide comprises an oxide of titanium (claim 11), wherein said semiconductor oxide comprises an oxide of silicon (claim 12),

wherein said semiconductor oxide comprises silicon dioxide (claim 13) nor wherein said metal electrical contact comprises tungsten (claim 16).

Kim et al discloses wherein said metal oxide comprises an oxide of titanium (Figure 8, reference 144; paragraphs 0018-0019), wherein said semiconductor oxide comprises an oxide of silicon (Figure 8, reference 150; paragraphs 0017 and 0021), wherein said semiconductor oxide comprises silicon dioxide (Figure 8, reference 150; paragraph 0021) and wherein said metal electrical contact comprises tungsten (Figure 8, reference 160; paragraph 0024).

It would have been obvious, for one with ordinary skill in the art, to modify Huang et al with the teachings of Kim et al for the purpose of forming metal oxide layers made of titanium, semiconductor oxide layers made of silicon oxides and contact layers made of tungsten which are all known in the art, to be used in MOS devices in order to form improved integrated circuits.

Claims 14 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 2014/0117465 A1) in view of Kim et al (US 2015/0001643 A1), further in view of Bohr (US 2007/0141798 A1).

15. Regarding claim 14, Huang et al discloses a region (Figure 1J, reference 2) in the semiconductor substrate (Figure 1J, reference 1).

However, Huang et al in view of Kim et al do not disclose wherein said region in the semiconductor substrate comprises an n-type doped source or drain of a transistor (claim 14).

Bohr discloses wherein said region in the semiconductor substrate (Figure 1, reference 112) comprises an n-type doped source or drain (Figure 1, references 108 and 110; paragraph 0011) of a transistor (Figure 1, reference 100).

It would have been obvious, for one with ordinary skill in the art, to modify Huang et al and Kim et al, with the teachings of Bohr for the purpose of forming an n-type doped source or drain of a transistor in order to form an NMOS transistor.

Claims 17-22 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 2014/0117465 A1) in view of Kim et al (US 2015/0001643 A1)

16. Regarding claim 17, Huang et al discloses an electrical junction, comprising: a source or drain of a transistor (Figure 1J, reference 9), said source or drain comprising a semiconductor (paragraph 0008), a metal electrical contact (Figure 1J, reference 10) to said source or drain (Figure 1, reference 9), and an interface layer (Figure 1J, oxide layer; paragraph 0036) disposed between and in contact with said source or drain (Figure 1J, reference 9) and said metal electrical contact (Figure 1J, reference 10), said source or drain (Figure 1J, reference 9) being electrically connected to said metal electrical contact (Figure 1J, reference 10) through said interface layer (Figure 1J, oxide layer; paragraph 0036).

However, Huang et al does not disclose said interface layer comprising an oxide of titanium and an oxide of the semiconductor.

Kim et al discloses said interface layer comprising an oxide of titanium (Figure 8, reference 144; paragraphs 0018-0019) and an oxide of the semiconductor (Figure 8, reference 150; paragraphs 0017 and 0021).

It would have been obvious, for one with ordinary skill in the art, to modify Huang et al with the teachings of Kim et al for the purpose of forming an interface layer made of titanium and an oxide layer made of a semiconductor in order to form improved integrated circuits in MOS devices.

17. Regarding claim 18, Huang et al discloses wherein said metal electrical contact (Figure 1J, reference 10) includes titanium (paragraph 0036).

18. Regarding claim 19, Huang et al in view of Kim et al discloses wherein said metal electrical contact includes tungsten (Figure 8, reference 160; paragraph 0024; Kim et al).

19. Regarding claims 20-22, Huang et al in view of Kim et al discloses wherein said semiconductor comprises silicon (Figure 8, reference 150; paragraphs 0017 and 0021; Kim et al).

Claims 23-28 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 2014/0117465 A1) in view of Kim et al (US 2015/0001643 A1)

20. Regarding claim 23, Huang et al discloses a semiconductor device (Figure 1J), comprising: a semiconductor region (Figure 1J, references 1 and 2) a metal electrical contact (Figure 1J, reference 9) to said semiconductor region (Figure 1J, references 1 and 2), and an interface layer (Figure 1J, references 7 and 8) disposed between and in contact (Figure 1J, reference 9) with said semiconductor region (Figure 1J, references 1 and 2) and said metal electrical contact (Figure 1J, reference 9), said semiconductor region (Figure 1J, references 1 and 2) being electrically connected to said metal electrical contact (Figure 1J, reference 9) through said interface layer (Figure 1J, references 7 and 8) and said interface layer (Figure 1J, references 7 and 8) comprising an oxide (paragraph 0033) of the semiconductor region (Figure 1J, reference 1 and 2; paragraphs 0027-0028).

However, Huang et al does not disclose said interface layer comprising an oxide of titanium.

Kim et al discloses interface layer comprising an oxide of titanium (Figure 8, reference 144; paragraphs 0018-0019).

It would have been obvious, for one with ordinary skill in the art, to modify Huang et al with the teachings of Kim et al for the purpose of forming an interface layer made of an oxide of titanium in order to form improved integrated circuits in MOS devices.

21. Regarding claim 24, Huang et al discloses wherein said metal electrical contact (Figure 1J, reference 10) includes titanium (paragraph 0036).

22. Regarding claim 25, Huang et al in view of Kim et al discloses wherein said metal electrical contact includes tungsten (Figure 8, reference 160; paragraph 0024; Kim et al).

23. Regarding claims 26-28, Huang et al in view of Kim et al discloses wherein said semiconductor comprises silicon (Figure 8, reference 150; paragraphs 0017 and 0021; Kim et al).

Claims 29 and 30 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 2014/0117465 A1) in view of Kim et al (US 2015/0001643 A1)

24. Regarding claims 29, Huang et al an electrical junction (Figure 1J), comprising: a source or drain (Figure 1J, reference 9) of a transistor, said source or drain (Figure 1J, reference 9) comprising a semiconductor (paragraph 0033), a metal electrical contact (Figure 1J, reference 10) to said source or drain (Figure 1J, reference 9), and an interface layer (Figure 1J, oxide layer; paragraph 0036) disposed between and in contact (Figure 1J, reference 10) with said source or drain (Figure 1J, reference 9) and said metal electrical contact (Figure 1J, reference 10), said source or drain (Figure 1J, reference 9) being electrically connected to said metal electrical contact (Figure 1J, reference 10) through said interface layer (Figure 1J, oxide layer; paragraph 0036).

However, Huang et al does not disclose said interface layer being less than 1 nm thick and comprising an oxide of the semiconductor.

Kim et al discloses said interface layer being less than 1 nm thick and comprising an oxide of the semiconductor (paragraph 0022).

It would have been obvious, for one with ordinary skill in the art, to modify Huang et al with the teachings of Kim et al for the purpose of forming an interface layer being less than 1 nm thick and comprising an oxide of the semiconductor in order to form improved integrated circuits in MOS devices.

25. Regarding claim 30, Huang et al discloses wherein said metal electrical contact (Figure 1J, reference 10) includes titanium (paragraph 0036).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Primary Examiner, Art Unit 2896

mdh
March 28, 2018

Notice of References Cited	Application/Control No. 15/877,837	Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2014/0117465 A1	05-2014	Huang; Ru	H01L29/78	257/411
*	B	US-2015/0001643 A1	01-2015	Kim; Hoon	H01L21/28229	257/410
*	C	US-2007/0141798 A1	06-2007	Bohr; Mark T.	H01L21/28079	438/301
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
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	K	US-				
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15877837
	Filing Date	2018-01-23
	First Named Inventor	Daniel E. Grupp
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	3771-0003-DC10

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4338616		1982-07-06	BOL	
	2	4566021		1986-01-21	YOKOYAMA	
	3	4999685		1991-03-12	WALDROP; et al.	
	4	5243213		1993-09-07	MIYAZAWA; et al.	
	5	7057333		2006-06-06	VU THIEN; et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20030022474		2003-01-30	GROVER; et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15877837
	Filing Date	2018-01-23
	First Named Inventor	Daniel E. Grupp
	Art Unit	2811
	Examiner Name	
	Attorney Docket Number	3771-0003-DC10

	2	20030219965		2003-11-27	CABRAL; et al.			

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EXAMINER SIGNATURE

Examiner Signature	/MONICA D HARRISON/	Date Considered	03/28/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15877837
Filing Date	2018-01-23
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	3771-0003-DC10

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

X A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2018-01-31
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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CONFIRMATION NO. 8140

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/877,837	01/23/2018 RULE	257	2896	3771-0003-DC10

APPLICANTS
Acorn Technologies, Inc., La Jolla, CA;

INVENTORS
Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

MDH 3/28/18

** **CONTINUING DATA** **********
This application is a CON of 15/728,002 10/09/2017
which is a CON of 15/251,210 08/30/2016 PAT 9812542
which is a CON of 15/048,877 02/19/2016 PAT 9905691
which is a CON of 13/552,556 07/18/2012 PAT 9425277
which is a CON of 13/022,522 02/07/2011 PAT 8431469
which is a DIV of 12/197,996 08/25/2008 PAT 7884003
which is a DIV of 11/181,217 07/13/2005 PAT 7462860
which is a CON of 10/217,758 08/12/2002 PAT 7084423

MDH 3/28/18

** **FOREIGN APPLICATIONS** ********** none MDH 3/28/18

** **IF REQUIRED, FOREIGN FILING LICENSE GRANTED** ** ** SMALL ENTITY **
03/01/2018

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged /MONICA D HARRISON/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	6	30	4

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Ascenda Law Group, PC
333 W San Carlos St.
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San Jose, CA 95110
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TITLE

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

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BIB (Rev. 05/07).

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15877837	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

CPC- SEARCHED

Symbol	Date	Examiner
H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872	3/28/18	MDH

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner
257	763	3/28/18	MDH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES

Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	3/28/18	MDH

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/MONICA D HARRISON/ Primary Examiner.Art Unit 2896

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15877837	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/28/2018								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
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	28	✓								
	29	✓								
	30	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17812	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:09
L2	7221	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:33
L3	6420	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:34
L4	68	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:34
L5	1	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:35
L6	8	H01L29/$'.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:35
L7	8	H01L29/$'.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:36

L8	0	H01L29/$'.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide and transistor and (metal near oxide) near5 tungsten	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:36
L9	2	H01L29/$'.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide and transistor and (metal near oxide) with tungsten	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:37
L10	7	"9812542".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 12:17
L11	1	(metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide and transistor and (metal near oxide) with tungsten AND ("20070141798" | "20030219965" | "4338616" | "4566021" | "7057333" | "20140117465" | "20030022474" | "20150001643" | "4999685" | "5243213").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 12:37
S1	1	"15877837"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/22 12:14
S2	985	257/763.ccls. and (substrate wafer carrier base plate) near9 metal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/22 12:21
S3	84	257/763.ccls. and (substrate wafer carrier base plate) with (metal near oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/22 12:22
S4	6	"20140117465"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/22 12:57
S5	4	257/763.ccls. and (silicon near cmos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2018/03/27 10:54

			IBM_TDB			
S6	233	257/763.ccls. and (source drain) near5 transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 10:55
S7	233	257/763.ccls. and (source drain) near5 transistor and (source drain) near5 transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 10:56
S8	60	257/763.ccls. and (source drain) near5 transistor and (source drain) near5 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 10:56
S9	42	257/763.ccls. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 10:57
S10	0	257/763.ccls. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal)) and (rais$4 near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:10
S11	802	257/'$'.ccls. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal)) and (rais$4 near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:11
S12	75	257/'$'.ccls. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal)) and (rais$4 near9 (source drain)) and (silicon near cmos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:12
S13	47	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal)) and (rais$4 near9 (source drain)) and (silicon near cmos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:22
S14	229	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and (metal near oxide) near9 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/03/27 11:25

			DERWENT; IBM_TDB			
S15	24	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and (metal near oxide) near9 interface and (interface near6 titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:26
S16	18	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and (metal near oxide) near9 interface and (interface near6 titanium) and (titanium with (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:27
S17	384	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:05
S18	110	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium) and ((semiconductor near oxide) with silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:06
S19	23	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium) and ((semiconductor near oxide) with silicon) and (silicon near dioxide) with semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:06
S20	5	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium) and ((semiconductor near oxide) with silicon) and (silicon near dioxide) with semiconductor and (tungsten with contact)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:07
S21	5	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium) and ((semiconductor near oxide) with silicon) and (silicon near dioxide) with semiconductor and (tungsten with contact) and ((implant$4 impur$4 dop$4) near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:07
S22	0	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (semicondcutor near oxide) near95 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:14
S23	0	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (semicondcutor near oxide) near5 silicon	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/03/27 13:14

			EPO; JPO; DERWENT; IBM_TDB			
S24	2392	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (semiconductor near oxide) near5 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:14
S25	42	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (semiconductor near oxide) near5 silicon and (metal near oxide) near5 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:15
S26	15	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) near5 titanium and (semiconductor near oxide) with (silicon near dioxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:16

EAST Search History (Interference)

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3/28/2018 12:38:32 PM
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PTO/SB/08a (07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Daniel E. Grupp
Art Unit	
Examiner Name	

Sheet	1	of	12	Attorney Docket No: 3771-0003-DC10

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		3513366	05/19/1970	CLARK	
		3590471	07/06/1971	LEPSELTER; et al.	
		3708360	01/02/1973	WAKEFIELD, JR.; et al.	
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		5608266	03/04/1997	AGNELLO; et al.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 03/28/2018

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Daniel E. Grupp
Art Unit	
Examiner Name	

Sheet	2	**of**	12	**Attorney Docket No:** 3771-0003-DC10

		5612567	03/18/1997	BALIGA	
		5663584	09/02/1997	WELCH	
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		6339232	01/15/2002	TAKAGI	
		6344673	02/05/2002	AUSSILHOU	

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Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Daniel E. Grupp
Art Unit	
Examiner Name	

Sheet	9	**of**	12	**Attorney Docket No:** 3771-0003-DC10

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Art Unit	
Examiner Name	

Sheet	10	**of**	12	**Attorney Docket No:** 3771-0003-DC10

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Sheet	11	**of**	12	**Attorney Docket No:** 3771-0003-DC10

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Art Unit	
Examiner Name	

Sheet	12	**of**	**12**	**Attorney Docket No:** 3771-0003-DC10

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2018-01-23
Name/Print	Tarek N. Fahmi	Registration Number	41402

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 15/877,837

First Named Inventor: Daniel E. Grupp

Filed: 01/23/2018

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC10

Confirmation No.: 8140

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

AMENDMENT

Dear Commissioner:

Responsive to the office action dated April 3, 2018, reconsideration of this application in view of the following amendments and remarks is respectfully requested.

Amendments to the claims are set forth in the listing of claims beginning on page 2.

Remarks begin on page 7.

AMENDMENTS TO THE CLAIMS

The following listing of the claims shall replace all previous versions thereof in this application.

Listing of claims:

1. (Currently Amended) An electrical junction, comprising a region in a semiconductor substrate, a metal electrical contact to said region, and an interface layer between said region and said metal electrical contact, said region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising a metal oxide ~~in contact with said metal electrical contact~~ and a semiconductor oxide, and being in contact with said region in the semiconductor substrate and said metal electrical contact.

2. (Original) The electrical junction of claim 1, wherein the semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

3. (Original) The electrical junction of claim 2, wherein the semiconductor oxide has a thickness of approximately 0.1 nm to 5 nm.

4. (Original) The electrical junction of claim 1, wherein said region in the semiconductor substrate comprises a source or drain of a transistor.

5. (Original) The electrical junction of claim 1, wherein said interface layer has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region.

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6. (Original) The electrical junction of claim 1, wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than 10 Ω-μm^2.

7. (Original) The electrical junction of claim 1, wherein said metal electrical contact comprises an alloy of a metal.

8. (Original) The electrical junction of claim 1, wherein said metal oxide comprises an oxide of said metal electrical contact.

9. (Original) The electrical junction of claim 8, wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

10. (Currently Amended) The electrical junction of claim [[1]] 8, wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

11. (Original) The electrical junction of claim 1, wherein said metal oxide comprises an oxide of titanium.

12. (Original) The electrical junction of claim 11, wherein said semiconductor oxide comprises an oxide of silicon.

13. (Original) The electrical junction of claim 12, wherein said semiconductor oxide comprises silicon dioxide.

14. (Original) The electrical junction of claim 12, wherein said region in the semiconductor substrate comprises an n-type doped source or drain of a transistor.

15. (Original) The electrical junction of claim 1, wherein said metal electrical contact comprises titanium.

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16. (Original) The electrical junction of claim 1, wherein said metal electrical contact comprises tungsten.

17. (Original) An electrical junction, comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor.

18. (Original) The electrical junction of claim 17, wherein said metal electrical contact includes titanium.

19. (Original) The electrical junction of claim 17, wherein said metal electrical contact includes tungsten.

20. (Original) The electrical junction of claim 17, wherein said semiconductor comprises silicon.

21. (Original) The electrical junction of claim 18, wherein said semiconductor comprises silicon.

22. (Original) The electrical junction of claim 19, wherein said semiconductor comprises silicon.

23. (Original) A semiconductor device, comprising:

a semiconductor region,

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a metal electrical contact to said semiconductor region, and

an interface layer disposed between and in contact with said semiconductor region and said metal electrical contact, said semiconductor region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor region.

24. (Original) The semiconductor device of claim 23, wherein said metal electrical contact includes titanium.

25. (Original) The semiconductor device of claim 23, wherein said metal electrical contact includes tungsten.

26. (Original) The semiconductor device of claim 23, wherein said semiconductor region comprises silicon.

27. (Original) The semiconductor device of claim 24, wherein said semiconductor region comprises silicon.

28. (Original) The semiconductor device of claim 25, wherein said semiconductor region comprises silicon.

29. (Original) An electrical junction, comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer being less than 1 nm thick and comprising an oxide of the semiconductor.

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30. (Original) The electrical junction of claim 29, wherein the metal electrical contact comprises titanium.

REMARKS

Reconsideration of this application in view of the foregoing amendments is respectfully requested.

As noted in the specification and the Application Data Sheet filed Oct. 9, 2017, the present application is a CONTINUATION of U.S. Patent Application No. 15/728,002, filed October 9, 2017, presently pending, which is a CONTINUATION of U.S. Patent Application No. 15/251,210, filed 8/30/2016, now U.S. Patent 9,812,542, which is a CONTINUATION of U.S. Patent Application No. 15/048,877, filed 2/19/2016, which is a CONTINUATION of U.S. Patent Application No. 13/552,556, filed 7/18/2012, now U.S. Patent 9,425,277, which is a CONTINUATION of U.S. Patent Application No. 13/022,522, filed 2/7/2011, now U.S. Patent 8,431,469, which is a DIVISIONAL of U.S. Patent Application 12/197,996, filed 8/25/2008, now U.S. Patent 7,884,003, which is a DIVISIONAL of U.S. Patent Application 11/181,217, filed 7/13/2005, now U.S. Patent 7,462,860, which is a CONTINUATION of U.S. Patent Application 10/217,758, filed 8/12/2002, now U.S. Patent 7,084,423. All of the requirements of 35 USC 120 and 37 CFR 1.78 having thus been satisfied, the application is entitled to its full priority claim.

As explained at [0050], "In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer . . . ." Further, at [0055] it is noted that, "passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer." And, at [0092] the use of TiO_2 as a separation layer is noted. Figure 6 shows an interface layer (620) in contact with both the metal

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contact (conductor 630) and the region in the semiconductor substrate (610), and [0069] explains, "according to one embodiment of the present invention, an interface layer 620 [is] disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620" Thus, the specification provides written description support for semiconductor-interface layer-metal contact junctions in which the interface layer includes both a semiconductor oxide and a metal oxide and the interface layer is in contact with both the semiconductor and the metal contact, as recited in the present claims. Further, the specification provides written description support for the claimed junctions with an interface layer disposed between and in contact with a semiconductor source or drain and a metal electrical contact, where the semiconductor source or drain is electrically connected to the metal electrical contact through the interface layer.

For at least the foregoing reasons, the objections relating to the claimed priority benefit should be withdrawn.

The rejections of the claims in view of Huang, US PGPUB 2014/0117465, should be withdrawn. The present application has an effective filing date of Aug. 12, 2002, which predates the earliest effective filing date of Huang. Therefore, Huang is not prior art to the present application.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 50-5798.

Respectfully submitted,
Ascenda Law Group, PC

Dated: May 11, 2018

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

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EFS ID:	32598269
Application Number:	15877837
International Application Number:	
Confirmation Number:	8140
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC10
Receipt Date:	11-MAY-2018
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Application Type:	Utility under 35 USC 111(a)

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	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	9

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/877,837	Filing Date 01/23/2018	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT

05/11/2018	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 30	Minus	** 30	= 0	X $50 =	0
Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $230 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**0**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/CHRISTINE MOLLISH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/877,837	01/23/2018	Daniel E. Grupp	3771-0003-DC10

CONFIRMATION NO. 8140

PUBLICATION NOTICE

OC000000100288578

27571
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

Title:METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Publication No.US-2018-0166552-A1
Publication Date:06/14/2018

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27571 7590 08/24/2018
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

EXAMINER
HARRISON, MONICA D

ART UNIT	PAPER NUMBER
2896	

DATE MAILED: 08/24/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/877,837	01/23/2018	Daniel E. Grupp	3771-0003-DC10	8140

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$500	$0	$0	$500	11/26/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

GF Exhibit 1130 - 169/196

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27571 7590 08/24/2018
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/877,837	01/23/2018	Daniel E. Grupp	3771-0003-DC10	8140

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$500	$0	$0	$500	11/26/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
HARRISON, MONICA D	2896	257-763000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

GF Exhibit 1130 - 170/196

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/877,837	01/23/2018	Daniel E. Grupp	3771-0003-DC10	8140

27571 7590 08/24/2018
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

EXAMINER
HARRISON, MONICA D

ART UNIT	PAPER NUMBER
2896	

DATE MAILED: 08/24/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/877,837	Applicant(s) GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/11/18*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-30*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Monica D. Harrison/
Primary Examiner, Art Unit 2896

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Priority

1. This application discloses and claims only subject matter disclosed in prior application no 15/728,002, filed 10/9/17, and names the inventor or at least one joint inventor named in the prior application. Accordingly, this application may constitute a continuation or division. Should applicant desire to claim the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120, 37 CFR 1.78, and MPEP § 211 *et seq.*

Allowable Subject Matter

2. Claims 1-30 are allowed over the prior art of record.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

After consideration and persuasion of applicant's arguments, amendments and a further search of the prior art of record, examiner has concluded that the prior art does not disclose nor fairly suggest the electrical junctions as described in the independent claims 1, 17 and 29.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Primary Examiner, Art Unit 2896

mdh
August 1, 2018

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1292	257/763.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:32
L2	115	257/763.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:32
L3	75	257/763.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:33
L4	8	257/763.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:33
L5	0	257/763.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:34
L6	386	257/'$'.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:36
L7	141	257/'$'.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:39

L8	78	257/'$'.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:40
L9	78	257/'$'.ccls. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi and source and drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:41
L10	35	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi and source and drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:43
L11	144	H01L29/'$'.cpc. and (substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi and source and drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:45
L12	157	(substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi and source and drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:49
L13	110	(substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi and source and drain.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:51
L15	2	(substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi and source and drain and acorn.asn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 16:53
L16	5	(substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi and source and drain and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/01 17:04
L17	2	"15877837"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2018/08/01 17:23

			IBM_TDB			
S1	1	"15877837"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/22 12:14
S2	985	257/763.ccls. and (substrate wafer carrier base plate) near9 metal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/22 12:21
S3	84	257/763.ccls. and (substrate wafer carrier base plate) with (metal near oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/22 12:22
S4	6	"20140117465"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/22 12:57
S5	4	257/763.ccls. and (silicon near cmos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 10:54
S6	233	257/763.ccls. and (source drain) near5 transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 10:55
S7	233	257/763.ccls. and (source drain) near5 transistor and (source drain) near5 transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 10:56
S8	60	257/763.ccls. and (source drain) near5 transistor and (source drain) near5 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 10:56
S9	42	257/763.ccls. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/03/27 10:57

			DERWENT; IBM_TDB			
S10	0	257/763.ccls. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal)) and (rais$4 near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:10
S11	802	257/'$'.ccls. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal)) and (rais$4 near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:11
S12	75	257/'$'.ccls. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal)) and (rais$4 near9 (source drain)) and (silicon near cmos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:12
S13	47	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (source drain) near5 transistor and (source drain) near5 silicon and (tungsten with (contact metal)) and (rais$4 near9 (source drain)) and (silicon near cmos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:22
S14	229	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and (metal near oxide) near9 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:25
S15	24	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and (metal near oxide) near9 interface and (interface near6 titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:26
S16	18	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and (metal near oxide) near9 interface and (interface near6 titanium) and (titanium with (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 11:27
S17	384	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:05
S18	110	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium) and ((semiconductor near oxide) with silicon)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/03/27 13:06

			EPO; JPO; DERWENT; IBM_TDB			
S19	23	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium) and ((semiconductor near oxide) with silicon) and (silicon near dioxide) with semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:06
S20	5	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium) and ((semiconductor near oxide) with silicon) and (silicon near dioxide) with semiconductor and (tungsten with contact)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:07
S21	5	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (substrate wafer carrier base plate) with (metal near oxide) and ((metal near oxide) with titanium) and ((semiconductor near oxide) with silicon) and (silicon near dioxide) with semiconductor and (tungsten with contact) and ((implant$4 impur$4 dop$4) near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:07
S22	0	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (semicondcutor near oxide) near95 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:14
S23	0	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (semicondcutor near oxide) near5 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:14
S24	2392	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (semiconductor near oxide) near5 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:14
S25	42	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (semiconductor near oxide) near5 silicon and (metal near oxide) near5 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:15
S26	15	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) near5 titanium and (semiconductor near oxide) with (silicon near dioxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/27 13:16
S27	17812	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide)	US-PGPUB; USPAT; USOCR;	OR	ON	2018/03/28 10:09

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S28	7221	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:33
S29	6420	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:34
S30	68	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:34
S31	1	H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:35
S32	8	H01L29/'$'.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:35
S33	8	H01L29/'$'.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:36
S34	0	H01L29/'$'.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide and transistor and (metal near oxide) near5 tungsten	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:36
S35	2	H01L29/'$'.cpc. and (metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide and transistor and (metal near oxide) with tungsten	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 10:37
S36	7	"9812542".pn.	US-PGPUB; USPAT;	OR	ON	2018/03/28 12:17

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S37	1	(metal near oxide) with (semiconductor near oxide) and (metal near oxide) with gate and (semiconductor near oxide) with gate and (metal near oxide) near5 titanium and (semiconductor near oxide) near9 dioxide and transistor and (metal near oxide) with tungsten AND ("20070141798" | "20030219965" | "4338616" | "4566021" | "7057333" | "20140117465" | "20030022474" | "20150001643" | "4999685" | "5243213").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/03/28 12:37

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L14	110	(substrate wafer carrier base plate) near9 (metal conduct$4) and (interface near9 (substrate wafer carrier base plate)) and (interface near9 (metal conduct$4)) and (metal near oxide) with interface and ((semiconductor near oxide) with interface) and ((semiconductor near oxide) with thickness) and fermi and source and drain.clm.	US-PGPUB; USPAT	OR	ON	2018/08/01 16:52

8/1/2018 5:26:12 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\15877837.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15877837	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

CPC- SEARCHED

Symbol	Date	Examiner
H01L29/45,456,08,089,0895,16,160,1608,161,47,66,661,6614,66143,666,6664,66643,78,783,7839,785,80,806,81,812,87,872	3/28/18	MDH

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner
257	763	3/28/18	MDH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES

Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	3/28/18	MDH
East updated	8/1/18	MDH
GRUPP ET AL .inv.	8/1/18	MDH
ACORN ET AL .asn.	8/1/18	MDH
USPAT, US-PGPUB txt .clm.	8/1/18	MDH

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	USPAT, US-PGPUB txt .clm.	8/1/18	MDH

	/MONICA D HARRISON/ Primary Examiner.Art Unit 2896

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15877837	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/28/2018	08/01/2018							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
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25	27	✓	=							
27	28	✓	=							
29	29	✓	=							
30	30	✓	=							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15877837	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

CPC						
Symbol					**Type**	**Version**
H01L		29	/	456	F	2013-01-01
H01L		21	/	28537	I	2013-01-01
H01L		29	/	0895	I	2013-01-01
H01L		29	/	47	I	2013-01-01
H01L		29	/	66143	I	2013-01-01
H01L		29	/	78	I	2013-01-01
H01L		29	/	7839	I	2013-01-01
H01L		29	/	785	A	2013-01-01
H01L		29	/	812	I	2013-01-01
H01L		29	/	16	I	2013-01-01
H01L		29	/	161	I	2013-01-01
H01L		29	/	45	I	2013-01-01
H01L		29	/	66643	I	2013-01-01
H01L		29	/	1608	I	2013-01-01
H01L		29	/	872	I	2013-01-01
H01L		29	/	806	I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 30	
/MONICA D HARRISON/ Primary Examiner.Art Unit 2896	08/01/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15877837	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
257	763	H	0	1	L	29 / 78 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

(Assistant Examiner) (Date)	Total Claims Allowed: 30	
/MONICA D HARRISON/ Primary Examiner.Art Unit 2896 08/01/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner) (Date)	1	6

U.S. Patent and Trademark Office

Part of Paper No. 20180801

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15877837	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	20	19												
4	4	22	20												
5	5	19	21												
6	6	21	22												
7	7	23	23												
8	8	24	24												
9	9	26	25												
10	10	28	26												
11	11	25	27												
12	12	27	28												
13	13	29	29												
14	14	30	30												
15	15														
16	16														

(Assistant Examiner)	(Date)	**Total Claims Allowed:** 30	
/MONICA D HARRISON/ Primary Examiner.Art Unit 2896	08/01/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
15877837	23-Jan-2018	Daniel Grupp	3771-0003-DC10	8140

TITLE OF INVENTION :

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Small	Utility under 35 USC 111(a)	2896	763000	MONICA HARRISON

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$500	$0	$500	26-Nov-2018	$0

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
27571 Ascenda Law Group, PC 333 W San Carlos St. Suite 200 San Jose CA 95110 UNITED STATES 408-799-0612 patents@ascendalaw.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☐ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

◉ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

○ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☒ Issue Fee

☐ I authorize USPTO to apply my previously paid issue fee to the current fees due

☐ Publication Fee

☐ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number _____

☐ Advance Order - # of copies _____

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4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. Ascenda Law Group, PC
2.
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Acorn Technologies, Inc.	La Jolla	CALIFORNIA	united states	corporation

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Tarek N. Fahmi/	**Date**	08-27-2018
Name	Tarek N. Fahmi	**Registration Number**	41402

Electronic Patent Application Fee Transmittal

Application Number:	15877837
Filing Date:	23-Jan-2018
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC10

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPL ISSUE FEE	2501	1	500	500
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**500**

Electronic Acknowledgement Receipt

EFS ID:	33548099
Application Number:	15877837
International Application Number:	
Confirmation Number:	8140
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC10
Receipt Date:	27-AUG-2018
Filing Date:	23-JAN-2018
Time Stamp:	15:04:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$500
RAM confirmation Number	082818INTEFSW15043500
Deposit Account	
Authorized User	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46039 cb943f2a2f88f573f05855caa99c9e3b7023f90d	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31913 5416071704093fa6d0be20b6801babfea5359154	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	77952		

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PTO/SB/08a (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Daniel E. Grupp
Art Unit	
Examiner Name	

Sheet	3	**of**	12	**Attorney Docket No:** 3771-0003-DC10

Change(s) applied to document, /Q.N./ 8/29/2018

		6380021	04/30/2002	WANG; et al.	
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		20050009302	01/13/2005	WAKUI; et al.	
		20050037557	02/17/2005	DOCZY; et al.	

EXAMINER SIGNATURE /MONICA D HARRISON/ **DATE CONSIDERED** 03/28/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/877,837	10/02/2018	10090395	3771-0003-DC10	8140

27571 7590 09/12/2018
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Daniel E. Grupp, Palo Alto, CA;
Acorn Technologies, Inc., La Jolla, CA;
Daniel J. Connelly, Redwood City, CA;

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