UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

ACORN SEMI, LLC,
Patent Owner

Case IPR2020-_____

U.S. Patent No. 9,905,691
Title: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
Issue Date: February 27, 2018

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,905,691

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All citations to 35 U.S.C. §§ 102, 103 and 112 in this paper refer to the pre-AIA statute unless otherwise noted.

All emphases are added unless otherwise noted.

This paper includes color illustrations and should be viewed in color.

PETITIONER'S EXHIBIT LIST

Petitioner Exhibit No.	DESCRIPTION
1101	U.S. Patent No. 9,905,691.
1102	File History of U.S. Patent No. 7,084,423.
1103	U.S. Patent No. 7,084,423.
1104	File History of U.S. Patent No. 6,833,556.
1105	U.S. Patent No. 6,833,556.
1106	File History of U.S. Patent No. 7,462,860.
1107	U.S. Patent No. 7,462,860.
1108	File History of U.S. Patent No. 7,884,003.
1109	U.S. Patent No. 7,884,003.
1110	File History of U.S. Patent No. 8,431,469.
1111	U.S. Patent No. 8,431,469.
1112	File History of U.S. Patent No. 9,425,277.
1113	U.S. Patent No. 9,425,277.
1114	File History of U.S. Patent No. 9,905,691.
1115	U.S. Patent No. 6,724,088 (cited as "Jammy").
1116	S.M. Goodnick et al., *Effects of a thin SiO_2 layer on the formation of metal-silicon contacts*, 18 J. VAC. SCI. & TECH. 949 (Apr. 1981) (cited as "Goodnick").
1117	M.A. Taubenblatt and C.R. Helms, *Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiO_x-Si systems*, 58 J. APPLIED PHYS. 6308 (1982) (cited as "Taubenblatt 1982").
1118	C.Y. Chang et al., *Specific contact resistance of metal-semiconductor barriers*, 15 SOLID STATE ELECS. 541 (1971) (cited as "Chang").
1119	Declaration of Dr. E. Fred Schubert (cited as "Schubert Decl.").
1120	E.H. Rhoderick, *Metal-semiconductor contacts*, 129 IEE REV. 1 (Feb. 1982) (cited as "Rhoderick").
1121	M.A. Sobolewski and C.R. Helms, *Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes*, J. VAC. SCI. & TECH. B 971 (Jul./Aug. 1989) (cited as "Sobolewski").
1122	U.S. Patent No. 4,110,488 (cited as "Risko").
1123	M.A. Taubenblatt et al., *Interface effects in titanium and hafnium Schottky barriers on silicon*, 44 APPLIED PHYS. LETTERS 895 (cited as "Taubenblatt 1984").

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1124	U.S. Patent No. 3,983,264 (cited as "Schroen").
1125	U.S. Patent No. 4,845,050 (cited as "Kim").
1126	Japanese Laid-Open App. No. JPH11162874A (June 18, 1999).
1127	Certified Translation of Japanese Laid-Open App. No. JPH11162874A (June 18, 1999) (cited as "Iwaguro").
1128	Gary P. Carver et al., *Specific Contact Resistivity of Metal-Semiconductor Contacts—A New, Accurate Method Linked to Spreading Resistance*, 35 IEEE TRANS. ELECTRON DEVICES 489 (Apr. 1988) (cited as "Carver").
1129	U.S. Patent No. 5,216,282 (cited as "Cote").
1130	A. Rohatgi et al., *Comprehensive Study of Rapid, Low-Cost Silicon Surface Passivation Technologies*, 47 IEEE Trans. Electron Devices 987 (May 2000) (cited as "Rohatgi").
1131	European Patent App. Pub. No. EP0789388A2 to Hara et al. (cited as "Hara").
1132	U.S. Patent No. 6,521,502 (cited as "Yu").
1133	T. Sakurai et al., *Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas*, 25 IEEE SOLID STATE CIRCUITS 584 (April 1990) (cited as "Sakurai").
1134	U.S. Patent No. 4,304,042 (cited as "Yeh").
1135	U.S. Patent No. 6,323,508 (cited as "Takahashi").
1136	U.S. Patent App. Pub. No. 2006/0178015 (cited as "Verhaverbeke").
1137	Declaration of Dr. Sylvia D. Hall-Ellis (cited as "Hall-Ellis Decl.").
1138	U.S. Patent No. 4,583,110.
1139	U.S. Patent No. 4,801,984.
1140	U.S. Patent No. 5,614,745.
1141	N. Szydlo and R. Poirier, *I-V and C-V Characteristics of Au/TiO_2 Schottky diodes*, 51 J. APPLIED PHYS. 6308 (June 1980) (cited as "Szydlo").
1142	M.L. Bortz et al., *Temperature dependence of the electronic structure of oxides: MgO, $MgAl_2O_4$ and Al_2O_3*, 41 PHYSICA SCRIPTA 537 (1990) (cited as "Bortz").
1143	Edet F. Archibong and Alain St-Amant, *On the Structure of Al2O3 and Photoelectron Spectra of $Al_2O_2^-$ and $Al_2O_3^-$*, 103 J. PHYS. CHEM. A 1109 (1998) (cited as "Archibong").
1144	N.D. Lang and W. Kohn, *Theory of Metal Surfaces: Work Function*, 3 PHYS. REV. B 1215 (1971) (cited as "Lang").

Petitioner Exhibit No.	DESCRIPTION
1145	I. Polishchuk et al., *Dual work function metal gate CMOS technology using metal interdiffusion*, 22 IEEE ELECTRON DEVICE LETTERS 444 (September 2001) (cited as "Polishchuk").
1146	Complaint in *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, Case No. 2:19-cv-00347, ECF No. 1 (E.D. Tex. Oct. 23, 2019).
1147	Summons and Return of Service in *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00347, ECF No. 8 (E.D. Tex. Oct. 29, 2019).
1148	Second Amended Docket Control Order, *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00347, ECF No. 39 (E.D. Tex. Apr. 21, 2020).
1149	Cover Pleading to Acorn's Preliminary Infringement Contentions in *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00347 (March 9, 2020).
1150	Exhibit E to Acorn's Preliminary Infringement Contentions in *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00347 (March 9, 2020).

All citations to specific pages of exhibits follow the pagination added to those exhibits per 37 C.F.R. § 42.63(d)(2)(i).

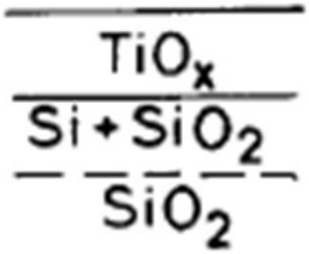
I. Introduction

Petitioner Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review and cancellation of Claims 1-4, 6, 8, 10-13, 15-20, 22, and 25-30 ("the challenged claims") of U.S. Patent No. 9,905,691 ("the '691 Patent"), assigned to Acorn Semi, LLC ("Acorn"). The '691 Patent purports to claim a priority date of August 12, 2002 through its parent applications. ('691 Patent at Cover, 1:8-21.)

The '691 Patent and the challenged claims generally relate to metal-semiconductor junctions and other structures that include a metal, a semiconductor, and an interface layer that includes a metal oxide and a semiconductor oxide therebetween. ('691 Patent at 1:25-29, Claims 1 and 25.) But those structures were well-known in the prior art. For example, the Goodnick reference, a 1981 journal article, describes a structure that includes aluminum, a silicon substrate, and an interface layer of aluminum oxide and silicon dioxide in between. (Goodnick at 1-2, 5.) Likewise, the Taubenblatt 1982 reference describes a structure that includes titanium, a silicon substrate, and an interface layer including titanium oxide and silicon dioxide in between. (Taubenblatt 1982 at 7-8.)

Certain challenged claims also require a specific contact resistivity (also called specific contact resistance) of less than 1 Ω-μm^2. ('691 Patent at Claims 18, 25-30.) But well before August 2002, ordinarily skilled artisans knew how to use interfacial oxide layers to reduce the specific contact resistivity of

metal-semiconductor junctions. One known technique for reducing the specific contact resistivity of a titanium to n-type silicon junction, such as that in Jammy, employed an interfacial layer of silicon dioxide to passivate the surface of the n-type silicon. (Jammy at Fig. 1, 4:5-17 (incorporating Cote by reference), 4:36-38; Cote at 8:24-28 (titanium conductive studs); Taubenblatt 1984 at 3.) That passivation reduced the junction's barrier height, which in turn reduced its specific contact resistivity. (Taubenblatt 1984 at 3; Chang at 4-5.) An ordinarily skilled artisan also would have known that converting some of that silicon dioxide to a titanium oxide—while leaving silicon dioxide to passivate the n-type silicon—would have further reduced specific contact resistance. (Kim at 4:63-5:1; Taubenblatt 1984 at 3.) An ordinarily skilled artisan therefore would have been motivated to form the following interface layer by combining Goodnick and Taubenblatt 1982:



(Taubenblatt 1982 at 7; *see also id.* at 8, Goodnick at 1-2.)

Finally, ordinarily skilled artisans would have reasonably expected to achieve a specific contact resistivity just under 1 Ω-μm^2 by using both that interface layer and standard semiconductor doping techniques. By both providing that interface layer and doping the Jammy reference's n-type silicon source or drain of a transistor

to a concentration of 10^{21} dopant atoms / cm^3 as taught by the Chang reference, an ordinarily skilled artisan would have reasonably expected to achieve a specific contact resistivity just under 1 Ω-μm^2.

In sum, an ordinarily skilled artisan would have found the challenged claims obvious over the Goodnick, Jammy, Taubenblatt 1982, and Chang references. As shown herein and as further explained in the declaration of Dr. E. Fred Schubert, an expert in metal-semiconductor junctions with more than thirty years of experience (Schubert Decl. ¶¶ 8-21), the challenged claims are unpatentable. Petitioner therefore respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

II. Mandatory Notices

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner identifies itself; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC as real parties-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

1. Judicial Matters

The following judicial matters may affect or be affected by this proceeding: *Acorn Semi, LLC v. Samsung Electronics Co. Ltd.*, Civil Action No. 2:19-cv-347 (E.D. Tex.) ("the Acorn Litigation"), in which Patent Owner Acorn Semi, LLC

("Acorn") filed a complaint alleging that Petitioner and its real parties-in-interest infringe the '691 Patent. (Ex. 1146 ¶¶ 98-107.) Acorn first served that complaint on October 24, 2019. (Ex. 1147.)

2. Administrative Matters

Public PAIR lists the following patents and applications that purport to claim the benefit of the priority of the filing date of the '691 Patent:

Patent or Application No.	Filing Date
U.S. Patent No. 9,812,542	August 30, 2016
U.S. Patent No. 10,388,748	October 9, 2018
U.S. Patent No. 10,090,395	January 23, 2018
U.S. Patent No. 10,186,592	May 16, 2018
U.S. Patent App. No. 16/506,022	July 9, 2019
U.S. Patent App. No. 16/847,878	April 14, 2020
U.S. Patent App. No. 15/929,592	May 12, 2020
U.S. Patent App. No. 15/929,593	May 12, 2020

Petitioner recently filed another petition for *inter partes* review against Claims 1-4, 6, 8, 10-13, 15-20, 22, and 25-30 of the '691 Patent in Case IPR2020-01206. Per the Board's guidance, Petitioner is also submitting a five-page paper explaining the differences between its two petitions, explaining why both petitions are necessary, and ranking the two petitions should the Board decide to institute only one of them. Patent Trial and Appeal Board Consolidated Trial Practice Guide, November 2019, at 59-60.

Petitioner is concurrently filing one or more petitions for *inter partes* review against the following patents related to the '691 Patent: U.S. Patent No. 7,084,423;

U.S. Patent No. 8,766,336; U.S. Patent No. 9,209,261; U.S. Patent No. 9,461,167; and U.S. Patent No. 10,090,395. Those proceedings may affect or be affected by this proceeding. Further, Acorn has asserted those five other patents against Petitioner and its real parties-in-interest in the Acorn Litigation. (Ex. 1146 ¶¶ 58-97, 108-117.)

C. Designation of Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

With this petition, Petitioner is filing a power of attorney appointing the practitioners associated with Customer Number 132,593. Petitioner designates the following lead and back-up counsel:

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Please direct all correspondence to lead and back-up counsel at the addresses listed above. Petitioner consents to electronic service at the following email addresses: jdesmarais@desmaraisllp.com; kkm-ptab@desmaraisllp.com; cmaier@desmaraisllp.com; and tkonstantakopoulos@desmaraisllp.com.

III. Fees

Petitioner is concurrently electronically submitting the required fees for this Petition. The Board is authorized to charge Desmarais LLP's deposit account, No. 50-6822, for any fee deficiency.

IV. Grounds for Standing

Petitioner certifies that the '691 Patent is available for *inter partes* review. Petitioner further certifies that neither Petitioner nor any real party-in-interest or privy is estopped or barred from requesting *inter partes* review of the challenged claims on the grounds identified in this petition.

V. Identification of Challenge and Relief Requested

Petitioner requests *inter partes* review and cancellation of Claims 1-4, 6, 8, 10-13, 15-20, 22, and 25-30 of the '691 Patent.

A. Identification of Prior Art

Although Petitioner is challenging the priority date of the challenged claims in its concurrent petition against the '691 Patent, all of the prior art cited herein qualifies as prior art even as of the earliest alleged priority date of the challenged claims in August 12, 2002. Petitioner reserves the right to challenge the priority date of the challenged claims in its reply in this proceeding, or in any other proceeding.

1. Goodnick (Ex. 1116)

S.M. Goodnick et al., *Effects of a thin SiO_2 layer on the formation of metal-silicon contacts*, 18 J. VAC. SCI. & TECH. 949 (Apr. 1981) (Ex. 1116, "Goodnick"), published in print in 1981 and again online in 1998. Because Goodnick became a prior art printed publication more than a year before August 12, 2002, Goodnick is prior art under at least 35 U.S.C. § 102(b).

On its face, Goodnick states that it is a publication of the Journal of Vacuum Science and Technology. (Goodnick at Cover, 1.) The Journal of Vacuum Science and Technology, the official publication of the AVS Science and Technology Society, was a well-known journal that split into two journals in 1983. (Schubert Decl. ¶¶ 74-76; Hall-Ellis Decl. ¶ 72.) That Goodnick published in the Journal of Vacuum Science and Technology—instead of either of its post-1983 successor journals—demonstrates that Goodnick first published before 1983, more than a year before August 12, 2002. Further, Goodnick bears a copyright date of 1981 and a

printing date of April 1981. (Goodnick at Cover, 1.) Goodnick also indicates that it published again online in June 1998. (*Id.* at Cover; Hall-Ellis Decl. ¶ 68.)

Further, the declaration testimony of Dr. Sylvia Hall-Ellis, an expert librarian, confirms that Goodnick was publicly accessible more than a year before August 12, 2002. As Dr. Hall-Ellis explains, MARC and OCLC records, as well as other records of the King Library at San José State University and the University of Minnesota Library, indicate that Goodnick was cataloged, indexed, and publicly available through at least the King Library on or shortly after April 30, 1981. (Hall-Ellis Decl. ¶¶ 69-76, Attachments 3a-3d.) Finally, the American Vacuum Society's records indicate that at least fourteen publications cited Goodnick more than a year before August 12, 2002. (Hall-Ellis Decl. ¶ 77, Attachment 3e (Citations 12-25).)

2. Jammy (Ex. 1115)

U.S. Patent No. 6,724,088 to Jammy et al., (Ex. 1115, "Jammy"), filed on April 20, 1999, qualifies as prior art under at least 35 U.S.C. § 102(e).

3. Taubenblatt 1982 (Ex. 1117)

M.A. Taubenblatt and C.R. Helms, *Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiO$_x$-Si systems*, 58 J. APPLIED PHYS. 6308 (1982) (Ex. 1117, "Taubenblatt 1982"), published in 1982. Because Taubenblatt 1982 became a prior art printed publication more than a year before August 12, 2002, Taubenblatt 1982 is prior art under at least 35 U.S.C. § 102(b).

Taubenblatt 1982 states that it is a publication of the Journal of Applied Physics. (Taubenblatt 1982 at 1.) Further, Taubenblatt 1982 states that it was "accepted for publication 27 May 1982" and published in September 1982. (*Id.*; *see also* Hall-Ellis Decl. ¶¶ 45-46 (confirming that Taubenblatt 1982 published in the September 1982 issue of the Journal of Applied Physics).) Taubenblatt 1982 also bears a copyright date of 1982 to the American Institute of Physics. (Taubenblatt 1982 at 1.) And, records of the American Institute of Physics indicate that Taubenblatt 1982 published again online in August 1998. (Hall-Ellis Decl. ¶ 46.)

Further, as Dr. Hall-Ellis explains, MARC and OCLC records, as well as other records of the King Library at San José State University and the University of Minnesota Library, indicate that Taubenblatt 1982 was cataloged, indexed, and publicly available through at least the King Library on or shortly after September 30, 1982. (Hall-Ellis Decl. ¶¶ 47-54, Attachments 1a-1c.) Finally, subsequent citations to Taubenblatt 1982, as indicated by Google Scholar, further confirm its public accessibility. (Hall-Ellis Decl. ¶ 55, Attachment 1d.)

4. Chang (Ex. 1118)

C.Y. Chang et al., *Specific contact resistance of metal-semiconductor barriers*, 15 SOLID STATE ELECS. 541 (1971) (Ex. 1118, "Chang") published in 1971. Because Chang became a prior art printed publication more than a year before August 12, 2002, Chang is prior art under at least 35 U.S.C. § 102(b).

Chang states that it is a publication of the journal *Solid-State Electronics* by Pergamon Press that was "Printed in Great Britain" in 1971. (Chang at 1; *see also* Hall-Ellis Decl. ¶¶ 56-57 (confirming that Chang published in the July 1971 issue of the journal *Solid-State Electronics*).) Further, as Dr. Hall-Ellis explains, MARC and OCLC records, as well as other records of the King Library at San José State University and the Library of Congress, indicate that Chang was cataloged, indexed, and publicly available through at least the King Library on or shortly after July 31, 1971. (Hall-Ellis Decl. ¶¶ 56-65, Attachments 2a-2c.) And, subsequent citations to Chang, as indicated by Google Scholar, further confirm Chang's public accessibility. (Hall-Ellis Decl. ¶ 66, Attachment 2d.)

Finally, Chang is cited on the faces of three semiconductor patents that issued more than a year before August 12, 2002: U.S. Patent No. 4,583,110 (Ex. 1138), issued in 1986; U.S. Patent No. 4,801,984 (Ex. 1139), issued in 1989; and U.S. Patent No. 5,614,745 (Ex. 1140), issued in 1997. Each citation both (1) confirms Chang's public accessibility during the prosecution of those patents; and (2) makes those patents "research aids" directing ordinarily skilled artisans to Chang. *Bruckelmyer v. Ground Heaters, Inc.*, 445 F.3d 1374, 1379 (Fed. Cir. 2006); *see also Cornell Univ. v. Hewlett-Packard Co.*, No. 01-cv-1974, 2008 WL 11274580, at *5-7 (N.D.N.Y. May 14, 2008).

B. Statutory Grounds of Unpatentability

Ground 1: Goodnick anticipates Claims 1-3 and 13 under 35 U.S.C. § 102(b).

Ground 2: Goodnick in view of Jammy renders Claim 4 obvious under 35 U.S.C. § 103(a).

Ground 3: Goodnick in view of Taubenblatt 1982 renders Claims 1, 3, 6, 10-13, 15, 16, 19, 20, and 22 obvious under 35 U.S.C. § 103(a).

Ground 4: Goodnick in view of Jammy and Taubenblatt 1982 renders Claims 8 and 17 obvious under 35 U.S.C. § 103(a).

Ground 5: Goodnick in view of Jammy, Taubenblatt 1982, and Chang renders Claims 18 and 25-30 obvious under 35 U.S.C. § 103(a).

VI. Overview of the '691 Patent

Metal-semiconductor junctions are a basic electronic component. (Schubert Decl. ¶¶ 30-31; '691 Patent at 1:33-34.) Those junctions are generally characterized by a barrier to the movement of charge carriers at the interface between the metal and the semiconductor, called a Schottky barrier. (Rhoderick at 1; '691 Patent at 1:46-48; Schubert Decl. ¶ 36.) The barrier's width and its height each affect the junction's specific contact resistance. (Chang at 5-6; Schubert Decl. ¶¶ 33-39.)

The Schottky barrier height of a metal-semiconductor junction can become fixed at a particular height in a phenomenon known as Fermi-level pinning. ('691 Patent at 2:4-61, 5:24-27, 7:44-48; Schubert Decl. ¶¶ 40-44.) Electron states,

including Bardeen states (such as dangling bonds at the semiconductor surface) and metal-induced gap states (energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal), can cause the Fermi level to become pinned between the semiconductor's conduction and valence bands, typically at or near the midgap. ('691 Patent at 2:35-3:3, 16:52-55; Schubert Decl. ¶¶ 44-45.) Fig. 7a shows a metal-semiconductor junction with a pinned Fermi level:

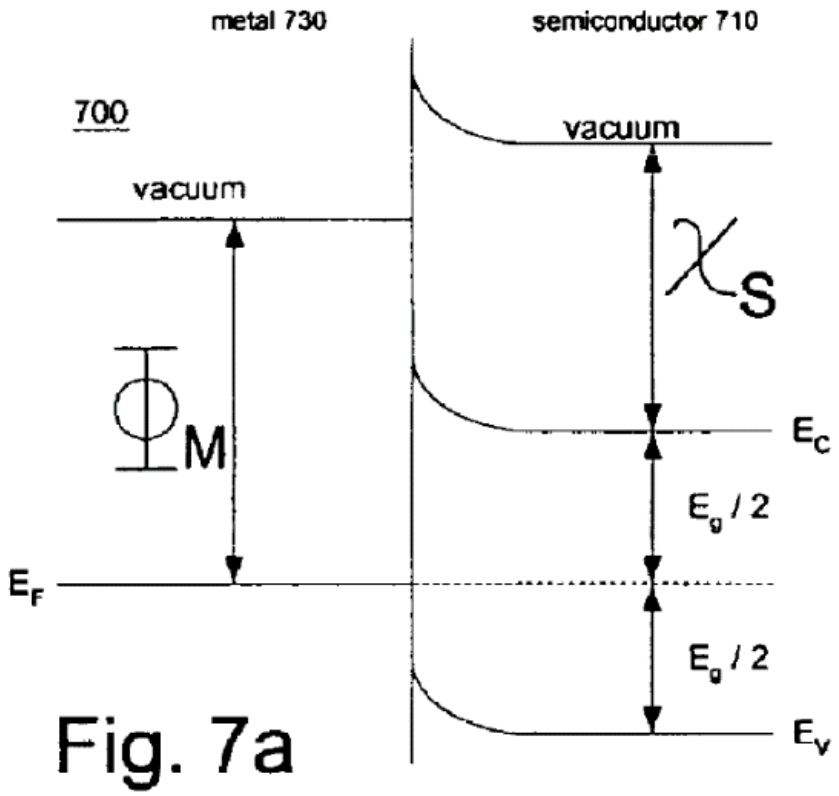


Fig. 7a

('691 Patent at Fig. 7a, 16:52-55.)

As Fig. 7a depicts, the pinned Fermi level E_F is not aligned with the conduction band edge E_C of the semiconductor at the interface. For an n-type semiconductor, the difference between the Fermi level E_F and the conduction band

edge of the semiconductor E_C at the interface produces a barrier to the flow of electrons of height Φ_b, as shown in Fig. 4 of the '691 Patent:

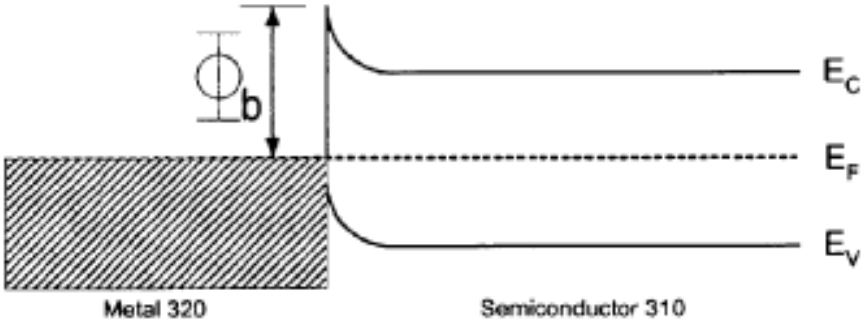


Fig. 4 (Prior Art)

('691 Patent at Fig. 4, 4:40-41, 7:24-48; Schubert Decl. ¶ 45.)

The junction's barrier height determines its electrical properties. ('691 Patent at 3:4-8.) According to the '691 Patent, depinning a Fermi level provides a way to control or adjust barrier height. (*Id.* at 16:23-44, Schubert Decl. ¶ 46.) But even before August 2002, techniques for depinning a Fermi level and controlling barrier height were well-known, as were techniques for reducing specific contact resistance. (Schubert Decl. ¶¶ 47-59.)

Indeed, the prior art was replete with examples of interface layers that depin a Fermi level by passivating the semiconductor surface (thereby satisfying dangling bonds and reducing Bardeen states) and reducing the effects of metal-induced gap states, including the examples described in the Goodnick, Rhoderick, and Sobolewski references. (Schubert Decl. ¶¶ 48-51; Goodnick at 1; Rhoderick at 3; Sobolewski at 1.) It was similarly known that an interfacial oxide could reduce the

barrier height of a metal-semiconductor junction. (Schubert Decl. ¶¶ 52-54; Risko at 1:43-50; Taubenblatt 1984 at 3.) Likewise, prior art from three decades taught that an interface layer could reduce the specific contact resistance of a metal-semiconductor junction: for example, the 1976 Schroen patent, the 1989 Kim patent, and the 1999 Iwaguro patent application publication. (Schubert Decl. ¶¶ 55-59; Schroen at Abstract; Kim at 4:63-5:1, 5:27-30; Iwaguro at [0005]-[0006], [0012]-[0014].)

A. The Purported Invention of the '691 Patent

The purported invention of the '691 Patent, like the prior art, involves providing an interface layer between the metal and the semiconductor in a metal-semiconductor junction. ('691 Patent at 1:25-29.) Claim 25 illustrates that uninventive approach:

> An electrical junction comprising an interface layer disposed between a contact metal and a semiconductor, the semiconductor comprising a source or drain of a transistor, the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer and configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω-μm^2.

B. Prosecution History

The ’691 Patent began as U.S. Patent App. No. 15/048,877 (“the ’877 Application”), filed on February 19, 2016. (Ex. 1114, at 9, 73.) The ’691 Patent purports to claim a priority date of August 12, 2002 through a series of parent applications. (Ex. 1105, at Cover, 1:8-21; Ex. 1114, at 9.)

Notably, the Examiner did not cite any prior art against any claim during prosecution. After signing the applicants’ information disclosure statements, the Examiner allowed the originally filed claims on the first office action, then later entered a corrected notice of allowance with an Examiner’s amendment to Claims 1, 6, 15, and 19. (Ex. 1114, at 61-64, 118-130, 142-152, 163-168.) The Examiner’s amendment did not make it into the issued claims, so the patentee requested and obtained a certificate of correction to effect the Examiner’s amendment. (*Id.* at 183-187, 191.) This petition addresses the claims as corrected.

VII. Level of Ordinary Skill in the Art

Any of the following combinations of education and experience would have qualified someone as an ordinarily skilled artisan in that field of the ’691 Patent as of its earliest alleged priority date in 2002:

- a Ph.D. in electrical engineering, physics, materials science, or chemical engineering, with two years of practical experience with semiconductor research and design;

- a Master's degree in electrical engineering, physics, materials science, or chemical engineering, with four years of practical experience with semiconductor research and design; or
- a Bachelor's degree in electrical engineering, physics, materials science, or chemical engineering, with six to eight years of practical experience with semiconductor research and design. (Schubert Decl. ¶ 66.)

Additional education could have made up for less practical experience, and vice versa. (*Id.*)

VIII. Claim Construction

Below, Petitioner construes the term "specific contact resistivity." As for all remaining claim terms, the challenged claims are unpatentable under those terms' ordinary and customary meanings, as explained in detail below. 37 C.F.R. § 42.100(b). The Board need not expressly construe any other term at this stage.[1]

[1] Petitioner reserves all rights to raise claim construction arguments and other arguments in the Acorn Litigation or other proceedings involving the '691 Patent. For example, Petitioner has not raised all of its challenges to the '691 Patent here, including invalidity under 35 U.S.C. § 112. Further, comparing the claims to the accused products in the Acorn Litigation may raise controversies that require claim construction in that litigation, but not here.

A. Claims 18 and 25-30: "specific contact resistivity"

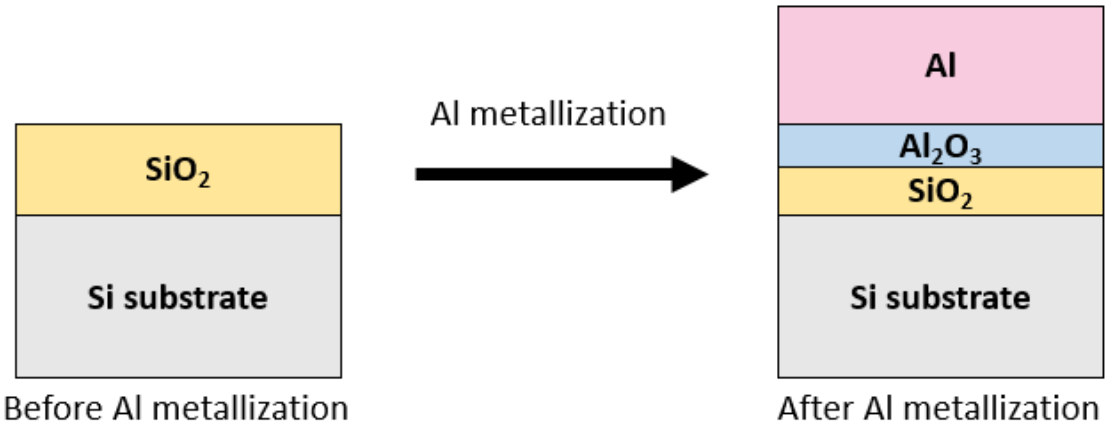
The term "specific contact resistivity" appears in Claims 18 and 25-30. Ordinarily skilled artisans commonly (if not universally) used the terms "specific contact resistivity" and "specific contact resistance" interchangeably. (Carver at 2; *see also* Schubert Decl. ¶ 69.) The '691 Patent's use of "specific contact resistivity" in Claims 18 and 25-30 tracks that common interchangeable use: the specification of the '691 Patent never uses the phrase "specific contact resistivity," but it does discuss specific contact resistance as part of the invention. (*E.g.*, '691 Patent at 3:19-23, 3:36-39, 3:46-47, 4:14-22; Schubert Decl. ¶ 70.) Thus, an ordinarily skilled artisan would have understood the term "specific contact resistivity" to refer to specific contact resistance in Claims 18 and 25-30. (Schubert Decl. ¶ 71.)

IX. Overview of the Prior Art

A. Goodnick (Ex. 1116)

Goodnick describes a series of experiments "to observe the influence of thin SiO_2 layers on the chemical formation of metal-silicon contacts." (Goodnick at 1.) Goodnick discloses that a thin interfacial oxide can satisfy dangling silicon bonds, thereby depinning a Fermi level. (*Id.*) Goodnick also teaches that "the presence of a thin oxide at the interface acts as a passivating influence, both from an electronic and a chemical standpoint." (*Id.*)

Goodnick discloses growing a thin, 30 Å SiO_2 layer on cleaned, phosphorous-doped silicon substrates, etching half of each substrate with hydrofluoric acid to remove the SiO_2 layers from those halves, then metallizing both the etched and unetched halves (which still had their SiO_2 layers) with aluminum, platinum, or gold. (Goodnick at 1-2.)[2] For the aluminum metallization, Goodnick explains that the aluminum partially reduced the 30 Å SiO_2 layer: "[a]s is seen in other studies, Al partially reduces the thin SiO_2 layer to form Al_2O_3 and free Si." (*Id.* at 5.) Thus, "[t]he results indicated that both SiO_2 and Al_2O_3 existed simultaneously at the interface, implying that the reaction is self-limiting, even at elevated temperatures. This is probably a result of the diffusion barrier formed by the Al_2O_3 layer to the transport of Al to the SiO_2 layer." (*Id.*) A schematic depiction of that metallization process and the resulting Al – Al_2O_3 – SiO_2 – Si contact appears below:



(Goodnick at 1-2, 5; Schubert Decl. ¶¶ 79-85.)

[2] One angstrom (Å) is equal to 0.1 nanometers (nm). Thus, 30 Å converts to 3 nm.

B. Jammy (Ex. 1115)

Jammy generally describes a MOSFET (metal oxide semiconductor field effect transistor) that incorporates an interface layer, which Jammy calls a quantum conductive barrier, between a conductive stud and a semiconductor substrate, such as that shown below in Fig. 1:

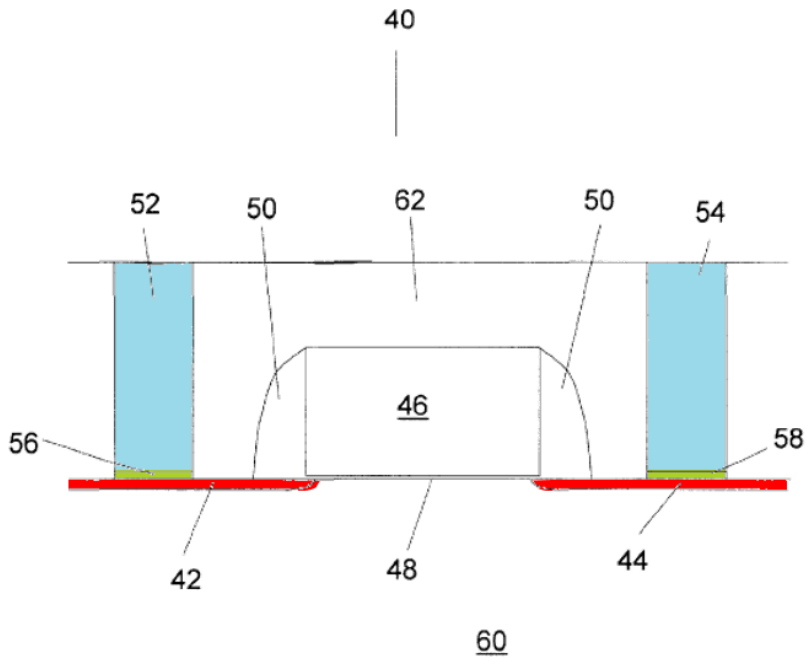


Figure 1

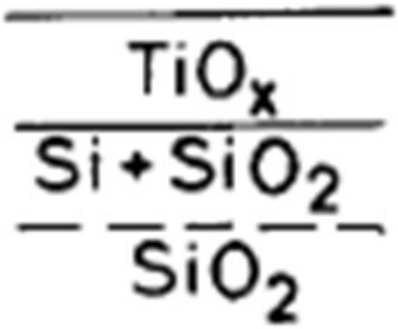
(Jammy at Fig. 1 (annotations added) Jammy at 2:42-53; 3:16-22.)

"FIG. 1 shows a schematic side view of a MOSFET 40 in a substrate 60. Shallow **source/drain diffusions (doped regions) 42 and 44** are formed in substrate 60. . . . **Conductive studs 52 and 54** contact **diffusions 42 and 44** through **quantum conductive barrier layers 56 and 58** respectively." (Jammy at 4:9-17.)

Jammy discloses forming those **source/drain diffusions** by implanting n-type dopants into a silicon substrate. (Jammy at 4:33-38.)

C. Taubenblatt 1982 (Ex. 1117)

Taubenblatt 1982 describes the interface layers that form when titanium is deposited on layer of SiO_2 (silicon dioxide) on an n-type silicon substrate and annealed. (Taubenblatt 1982 at 2, 7-8.) Taubenblatt 1982 discloses that when titanium is deposited on top of a layer of SiO_2 thicker than 20 Å, and the resulting structure is annealed at 700ºC – 900ºC, the TiO_x (titanium oxide) – SiO_2 interface layer depicted below forms between the titanium and the silicon:



(Taubenblatt 1982 at 7; *see also id.* at 8.)

As Taubenblatt 1982 describes, "in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide." (Taubenblatt 1982 at 8.) Thus, once the TiO_x layer forms, it prevents subsequent reactions between the titanium and the SiO_2, leaving a layer of unreacted Ti metal atop the TiO_x layer. (*Id.*; Schubert Decl. ¶ 95.)

D. Chang (Ex. 1118)

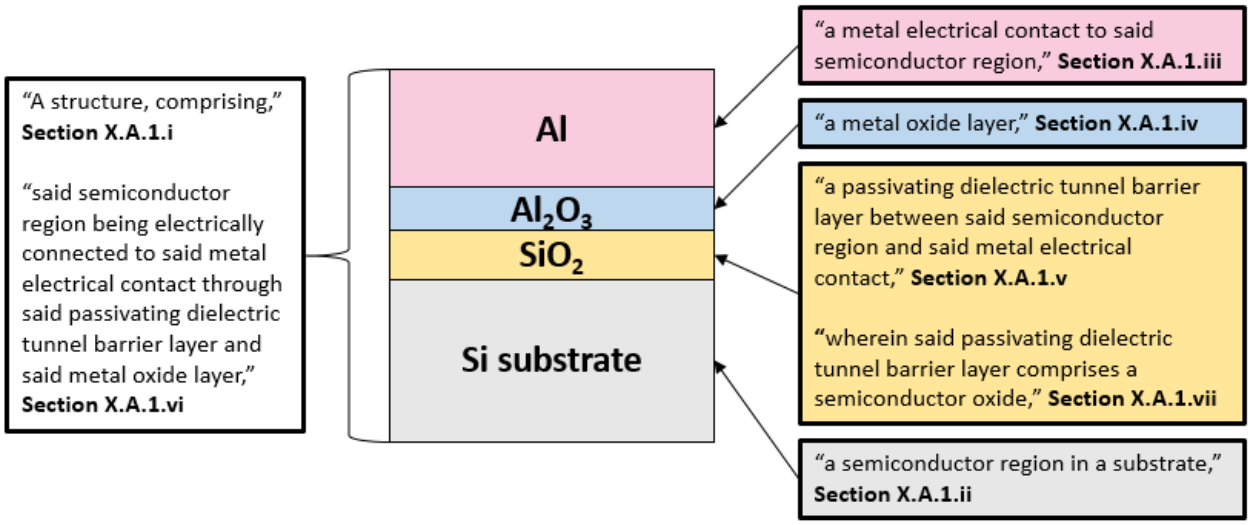
Chang generally addresses specific contact resistance for "various metals on silicon samples . . . . " (Chang at 1.) Chang describes that at doping levels above 10^{18} dopant atoms / cm^3, specific contact resistance "becomes a strong function of doping," decreasing as doping increases. (*Id.* at 4-5.) Chang also explains that the specific contact resistance of an electrical junction decreases as its barrier height decreases. (*Id.* at 6.) Finally, Chang describes a doping concentration as high as 10^{21} dopant atoms / cm^3 for n-type doped silicon. (*Id.* at 7 (Fig. 5).)

X. The challenged claims are unpatentable.

A. Ground 1: Goodnick anticipates Claims 1-3 and 13.

1. Claim 1

As discussed above in **Section IX.A**, Goodnick discloses an Al – Al_2O_3 – SiO_2 – Si contact. That contact meets every limitation of Claim 1, as summarized below:



(Goodnick at 1-2, 5; Schubert Decl. ¶¶ 79-85, 104.)

i. A structure, comprising

The preamble is not limiting. Nonetheless, Goodnick discloses an Al – Al_2O_3 – SiO_2 – Si contact as discussed above in **Section IX.A**, which contact is a structure. (Goodnick at 1-2, 5; Schubert Decl. ¶ 105.)

ii. a semiconductor region in a substrate,

Goodnick discloses this limitation. (Schubert Decl. ¶ 106.) Goodnick discloses a silicon substrate, and silicon is an example of a semiconductor. (Goodnick at 1; '691 Patent at 3:19-23.) "The silicon substrates used in this study were commercial single crystal (100) wafers, phosphorous doped to 10^{15} cm^{-3}." (Goodnick at 1.) Phosphorous is an n-type dopant, so Goodnick's silicon substrate is n-type doped. (*Id.*; Yu at 1:53-55, 4:19-21.)

iii. a metal electrical contact to said semiconductor region,

Goodnick discloses this limitation. (Schubert Decl. ¶ 107.) In particular, Goodnick discloses an aluminum metal electrical contact. (Goodnick at 1.) Goodnick describes forming a metal-silicon contact by evaporating aluminum (Al) onto a 30 Å layer of SiO_2 grown on a cleaned silicon substrate. (*Id.* at 1-2.)

iv. a metal oxide layer, and

Goodnick discloses this limitation. (Schubert Decl. ¶ 108.) In particular, Goodnick discloses an aluminum oxide (Al_2O_3) layer, which is a metal oxide layer. (Goodnick at 5.)

v. a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact,

Goodnick discloses this limitation. (Schubert Decl. ¶¶ 109-111.) In particular, Goodnick discloses a silicon dioxide (SiO_2) layer, which is a passivating dielectric tunnel barrier between said semiconductor region and said metal electrical contact. (*Id.* ¶ 109.) Goodnick describes thermally evaporating aluminum (a metal electrical contact) onto an SiO_2 layer grown on a silicon substrate (semiconductor region). (Goodnick at 1-2, 5; Schubert Decl. ¶¶ 108-110.) Although the aluminum partially reduced the SiO_2 to produce Al_2O_3, some of the SiO_2 layer grown on the silicon surface remained. (Goodnick at 5; Schubert Decl. ¶ 109.)

That remaining layer of SiO_2 grown on the silicon substrate, which lies between the silicon substrate (semiconductor region) and the aluminum (metal electrical contact), is a passivating layer. (Schubert Decl. ¶ 110.) Goodnick discloses that "the presence of a thin oxide at the interface acts as a passivating influence, both from an electronic and a chemical standpoint." (Goodnick at 1.) "A thin interfacial oxide also may significantly reduce the density of interface states by satisfying silicon dangling bonds." (*Id.*) And, the '691 Patent admits that silicon dioxide (SiO_2) grown on a silicon surface passivates the surface. ('691 Patent at 8:14-21.)

Goodnick's remaining layer of SiO_2 grown on the silicon substrate is also a dielectric tunnel barrier layer. (Schubert Decl. ¶ 111.) Silicon dioxide is an example

of a semiconductor oxide, and U.S. Patent No. 6,833,556, which the '691 Patent incorporates by reference, identifies "an oxide of a semiconductor" as an example of a dielectric material. (Ex. 1105, at 7:60-61; '691 Patent at 1:8-21; Schubert Decl. ¶ 111.) Goodnick also characterizes the SiO_2 layers in its experiments as "thin," and states that "an oxide layer that is sufficiently thin may sustain considerable current via tunneling." (Goodnick at 1.) Thus, the thin remaining layer of SiO_2 in Goodnick is a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact.

vi. said semiconductor region being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer and said metal oxide layer,

Goodnick discloses this limitation. (Schubert Decl. ¶ 112.) Goodnick's experiments, including its aluminum metallization, investigated "the influence of thin SiO_2 layers on the chemical formation of metal-silicon contacts." (Goodnick at 1.) For the aluminum metallization, Goodnick discloses that "both SiO_2 and Al_2O_3 existed simultaneously at the interface . . . ." (*Id.* at 5.) That Goodnick characterizes its Al – Al_2O_3 – SiO_2 – Si structure as a "metal-silicon contact" indicates that the silicon substrate (semiconductor region) is electrically connected to the aluminum (metal electrical contact) through the Al_2O_3 – SiO_2 interface layer. (Schubert Decl. ¶ 112.) Confirming that electrical connection, Goodnick describes its interfacial

oxide layers as "thin," and states that "an oxide layer that is sufficiently thin may sustain considerable current via tunneling." (Goodnick at 1; Schubert Decl. ¶ 112.)

vii. wherein said passivating dielectric tunnel barrier layer comprises a semiconductor oxide.

Goodnick discloses this limitation. (Schubert Decl. ¶ 113.) As discussed above in **Section X.A.1.v**, Goodnick describes an SiO_2 (silicon dioxide) passivating dielectric tunnel barrier layer. (*Id.*; Goodnick at 1-2, 5.) Silicon dioxide is an oxide of silicon, and silicon is a semiconductor. ('691 Patent at 3:19-23.)

2. Claim 2

i. The structure of claim 1,

Goodnick discloses the structure of Claim 1, as discussed above in **Section X.A.1**. (Schubert Decl. ¶ 115.)

ii. wherein the semiconductor oxide comprises an oxide of the semiconductor region.

Goodnick discloses this limitation. (Schubert Decl. ¶ 116.) As discussed above in **Sections X.A.1.v and X.A.1.vii**, Goodnick discloses thermally growing a layer of SiO_2 on a silicon substrate. (Goodnick at 1-2.) Some of that SiO_2 layer is partially reduced by aluminum to produce Al_2O_3, but an SiO_2 layer nonetheless remains on the silicon substrate, and it is an oxide of that silicon substrate. (*Id*. at 5; Schubert Decl. ¶ 116.)

3. Claim 3

i. The structure of claim 1,

Goodnick discloses the structure of Claim 1, as discussed above in **Section X.A.1**. (Schubert Decl. ¶ 118.)

ii. wherein the semiconductor oxide of the dielectric tunnel barrier layer has a thickness of approximately 0.1 nm to 5 nm.

Goodnick discloses this limitation. (Schubert Decl. ¶ 119.) Goodnick describes thermally growing a 30 Å (3 nm) thick layer of SiO_2 on a silicon substrate. (Goodnick at 1-2.) As discussed above with respect to Claim 2 in **Section X.A.2.ii**, some of that SiO_2 layer is partially reduced by aluminum to produce Al_2O_3, but an SiO_2 layer nonetheless remains on the silicon substrate. (*Id.* at 5.) The minimum possible thickness of the remaining SiO_2 layer is 2 angstroms (0.2 nm), the thickness of a monolayer of SiO_2, *i.e.*, a layer one SiO_2 molecule thick. (Verhaverbeke at [0004]; Schubert Decl. ¶ 119.) Thus, the thickness of Goodnick's post-metallization SiO_2 layer is between 0.2 nm and 3 nm, satisfying this limitation. (Schubert Decl. ¶ 119.)

4. Claim 13

i. The structure of claim 3,

Goodnick discloses the structure of Claim 3, as discussed above in **Section X.A.3**. (Schubert Decl. ¶ 121.)

ii. wherein the semiconductor oxide comprises an oxide of silicon.

Goodnick discloses this limitation. (Schubert Decl. ¶ 122.) As discussed above in **Section X.A.2**, Goodnick discloses a semiconductor oxide that comprises SiO_2 (silicon dioxide), which is an oxide of silicon. (Goodnick at 5.)

B. Ground 2: Goodnick in view of Jammy renders Claim 4 obvious.

1. Combination of Goodnick and Jammy

As discussed above in **Section X.A.1.ii**, Goodnick discloses a semiconductor region in a substrate. Further, Goodnick discloses growing a thin SiO_2 layer on a cleaned, phosphorus-doped silicon substrate, which is an n-type doped silicon semiconductor region. (Goodnick at 1; Yu at 1:53-55, 4:19-21; Schubert Decl. ¶ 123.) Goodnick does not expressly disclose that its n-type doped silicon semiconductor region "comprises an n-type doped source or drain of a transistor" as recited in Claim 4. Jammy, however, discloses a silicon substrate that includes an n-type doped source or drain of a MOSFET (metal oxide semiconductor field effect transistor), which Jammy calls a source/drain diffusion region. (Jammy at 4:1-4, 4:9-12, 4:33-38; Schubert Decl. ¶ 124.)

An ordinarily skilled artisan would have found it obvious to form Goodnick's Al – Al_2O_3 – SiO_2 – Si contact as described for Claim 1 in **Section X.A.1** using Jammy's n-type doped silicon source or drain of a transistor as the semiconductor region. (Schubert Decl. ¶ 125.) That combination would have involved growing

Goodnick's 30 Å thick layer of SiO_2 on Jammy's cleaned n-type doped source/drain diffusion regions, then depositing aluminum on the SiO_2 layer as described in Goodnick. (Goodnick at 1-2, 5; Jammy at 4:9-12, 4:33-38, 5:32-37.) An ordinarily skilled artisan would have expected that combination to produce the same Al – Al_2O_3 – SiO_2 – Si structure described in Goodnick; swapping out Goodnick's n-type doped silicon substrate for Jammy's n-type doped silicon source or drain of a transistor in a silicon substrate would not have changed the structure or function of the resulting Al_2O_3 – SiO_2 interface layer. (Schubert Decl. ¶ 125.) And, that simple substitution would have yielded a predictable result, which is a recognized obviousness rationale. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416-17 (2007).

Further, an ordinarily skilled artisan would have combined Goodnick and Jammy because their teachings fit "together like pieces of a puzzle." *KSR*, 550 U.S. at 420-421. (Schubert Decl. ¶ 126.) Goodnick describes contact metallization processes for semiconductor devices, and Jammy describes a semiconductor device. (Goodnick at 1; Jammy at 4:1-4, 4:9-11.) Jammy identifies alumina (aluminum oxide) as a suitable interface layer, and Goodnick discloses how to form an aluminum oxide interface layer, as discussed above in **Section X.A.1.iv**. (Jammy at 3:55-58; Goodnick at 1-2, 5.) Jammy also suggests using an interface layer that "prevent[s] or slow[s] diffusion of chemical species from one side of the layer to the

other," and Goodnick's Al_2O_3 layer forms a diffusion barrier against aluminum migrating to the SiO_2 layer. (Jammy at 3:27-29; Goodnick at 5.)

2. Claim 4

i. The structure of claim 3,

Goodnick discloses the structure of Claim 3, as discussed above in **Section X.A.3**. (Schubert Decl. ¶ 129.)

ii. wherein the semiconductor region comprises an n-type doped source or drain of a transistor.

Jammy discloses this limitation. (Schubert Decl. ¶ 130.) In particular, Jammy discloses a silicon substrate that includes an n-type doped source or drain of a MOSFET (metal oxide semiconductor field effect transistor), which Jammy calls a source/drain diffusion region. (Jammy at 4:1-4, 4:9-12, 4:33-38.)

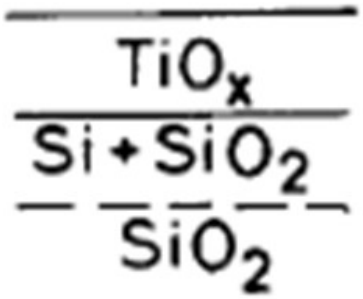
C. Ground 3: Goodnick in view of Taubenblatt 1982 renders Claims 1, 3, 6, 10-12, 13, 15, 16, 19, 20, and 22 obvious.

1. Combination of Goodnick and Taubenblatt 1982

As discussed above in **Section X.A.1**, Goodnick describes growing a 30 Å layer of SiO_2 on an n-type silicon substrate, then depositing aluminum on that layer of SiO_2 to form an Al – Al_2O_3 – SiO_2 – Si contact. (Goodnick at 1-2, 5; Schubert Decl. ¶ 131.) Although Goodnick discloses an interface layer that includes a metal oxide layer (aluminum oxide, Al_2O_3), Goodnick does not expressly describe a "metal oxide layer [that] comprises an oxide of titanium" as in Claims 6, 10-12, and 15-16.

But, an ordinarily skilled artisan could have provided and would have been motivated to provide Goodnick with an interface layer that includes both titanium oxide and silicon dioxide using the combined teachings of Goodnick and Taubenblatt 1982. (Schubert Decl. ¶¶ 132-133.) Below, Petitioner first explains ***how*** to form that interface layer using Goodnick and Taubenblatt 1982, and then ***why*** an ordinarily skilled artisan would have been motivated to do so.

Starting with the "how," Taubenblatt 1982 discloses a technique for forming an interface layer between titanium and silicon, which interface layer includes both a titanium oxide (TiO_x), which is a metal oxide, and silicon dioxide (SiO_2), which is a semiconductor oxide:



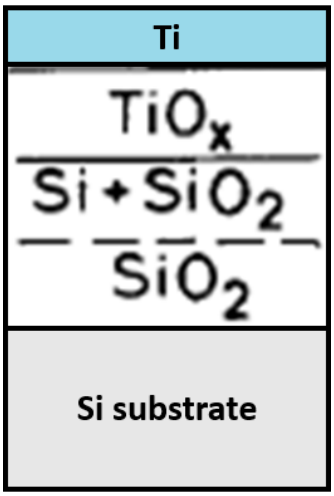
(Taubenblatt 1982 at 7; *see also id.* at 8.)

In particular, Taubenblatt 1982 discloses that when titanium is deposited on a layer of SiO_2 thicker than 20 Å (2 nm) and annealed at temperatures between 700ºC – 900ºC, the TiO_X – SiO_2 interface layer depicted above forms. (Taubenblatt 1982 at 7-8; Schubert Decl. ¶¶ 134-135.) Taubenblatt 1982 describes that "in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier

to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide." (Taubenblatt 1982 at 8.) Thus, once the TiO_x layer forms, it prevents subsequent reactions between the titanium and the SiO_2, leaving a layer of unreacted Ti metal atop the TiO_x layer. (*Id.*; Schubert Decl. ¶ 136.)

To provide the initial layer of SiO_2 thicker than 20 Å required by the Taubenblatt 1982 technique, Goodnick teaches thermally growing a 30 Å-thick layer of SiO_2 on a silicon substrate. (Goodnick at 1-2.) And to provide the titanium, Taubenblatt 1982 describes depositing titanium on a silicon dioxide layer. (Taubenblatt 1982 at 7-8.) With Taubenblatt 1982's titanium deposited on Goodnick's 30 Å-thick layer of thermally grown SiO_2, all that it would have taken to form a TiO_x – SiO_2 interface layer is annealing at 700ºC – 900ºC as described in Taubenblatt 1982. (Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 137.) And annealing was a common and necessary processing step for semiconductor devices; indeed, the prior art describes "[p]ost-deposition processing, such as annealing" as "critical for typical device fabrication . . . ." (Taubenblatt 1984 at 1; Schubert Decl. ¶ 137.)

In sum, an ordinarily skilled artisan could have readily applied the teachings of Goodnick and Taubenblatt 1982 to form a TiO_x – SiO_2 interface layer as taught in Taubenblatt 1982 between Goodnick's silicon substrate and Taubenblatt 1982's titanium. The result of that combination is depicted schematically below:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 138.)

Turning to the "why," an ordinarily skilled artisan would have been motivated to form the TiO_x – SiO_2 interface layer according to the combined teachings of Goodnick and Taubenblatt 1982 as an interface layer between Taubenblatt 1982's titanium and Goodnick's n-type silicon substrate because that interface layer would have been expected to reduce the specific contact resistivity of that junction. (Schubert Decl. ¶ 139.) Indeed, the prior art was replete with examples of interface layers that reduce the specific contact resistivity of a metal-semiconductor junction. (*Id.* ¶ 140; Schroen at Abstract; Kim at 4:63-5:1, 5:27-30; Iwaguro at [0005]-[0006], [0012]-[0014].)

The TiO_x – SiO_2 interface layer formed according to the combined teachings of Goodnick and Taubenblatt 1982 would have been yet another entry in the canon of interface layers that reduce specific contact resistance. In particular, it was known that an SiO_2 interface layer grown on silicon will passivate the surface of the silicon.

(Goodnick at 1; Taubenblatt 1984 at 3; Schubert Decl. ¶ 141.) That passivation would have reduced the barrier height of a titanium to n-type silicon junction, such as the junction between Taubenblatt's titanium and Goodnick's n-type source/drain silicon substrate. (Taubenblatt 1984 at 3; Goodnick at 1-2; Schubert Decl. ¶ 141.) For a junction between titanium and n-type silicon with an SiO_2 interface layer, the SiO_2 interface layer produces a net reduction of barrier height of more than 0.1 eV owing to the passivation that the SiO_2 interface layer provides. (Taubenblatt 1984 at 3.) And, reducing the barrier height of a junction reduces its specific contact resistivity. (Chang at 5-6; Schubert Decl. ¶ 141.)

By depositing titanium on the SiO_2 layer and annealing to convert part of that SiO_2 interface layer to a titanium oxide—while still leaving enough SiO_2 to passivate the silicon surface—specific contact resistivity will decrease further. (Schubert Decl. ¶ 142.) While titanium oxides modestly passivate silicon surfaces—and therefore modestly reduce the junction's barrier height—they present less resistance to current than SiO_2 does. (Rohatgi at 2-3; Kim at 4:63-5:1; Schubert Decl. ¶ 142.) Thus, converting some of the interface layer's SiO_2 to a titanium oxide would have decreased specific contact resistivity further. (Kim at 4:63-5:1; Schubert Decl. ¶ 142.) But, an ordinarily skilled artisan would have found it beneficial to leave ***some*** SiO_2 remaining in the interface layer to obtain the barrier-height reducing benefits of a passivating layer of SiO_2. (Taubenblatt 1984 at 3; Schubert Decl. ¶ 143.)

The desire to provide a low-resistance interface layer that also passivates the surface of the silicon would have led an ordinarily skilled artisan to the TiO_x – SiO_2 layer in Taubenblatt 1982. (Schubert Decl. ¶ 144.) In particular, Taubenblatt 1982 discloses an interface layer with an SiO_2 passivating layer that remains in contact with the silicon after titanium deposition and annealing at 700ºC-900ºC: "in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide." (Taubenblatt 1982 at 8.) And, the combination of a thicker (> 20 Å) silicon dioxide layer (such as the 30 Å layer taught in Goodnick) and annealing at 700ºC-900ºC was proven to produce a TiO_x – SiO_2 interface layer:

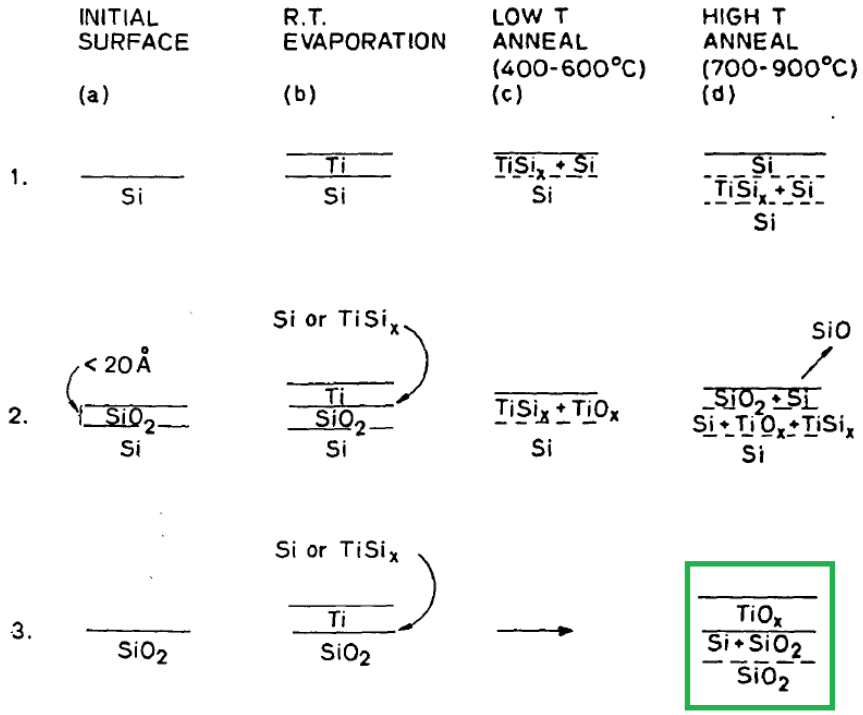


FIG. 11. Schematic diagram of Ti-Si and Ti-SiO_x reactions.

(Taubenblatt 1982 at 7 (annotations added); *see also* Goodnick at 1-2; Schubert Decl. ¶ 144.)

That TiO_x – SiO_2 interface layer combines the barrier-height-lowering of a passivating layer of SiO_2 with the lower resistance of a layer of titanium oxide. (Taubenblatt 1982 at 7-8; Kim at 4:63-5:1; Schubert Decl. ¶ 145.) Thus, Taubenblatt 1982's TiO_x – SiO_2 interface layer would have delivered the "best of both worlds" for reducing the specific contact resistivity of a junction between Taubenblatt 1982's titanium and Goodnick's n-type silicon substrate: the passivating benefits of silicon dioxide for reducing barrier height; and the lower resistance to electrical current of a titanium oxide. Schubert Decl. ¶ 146.)

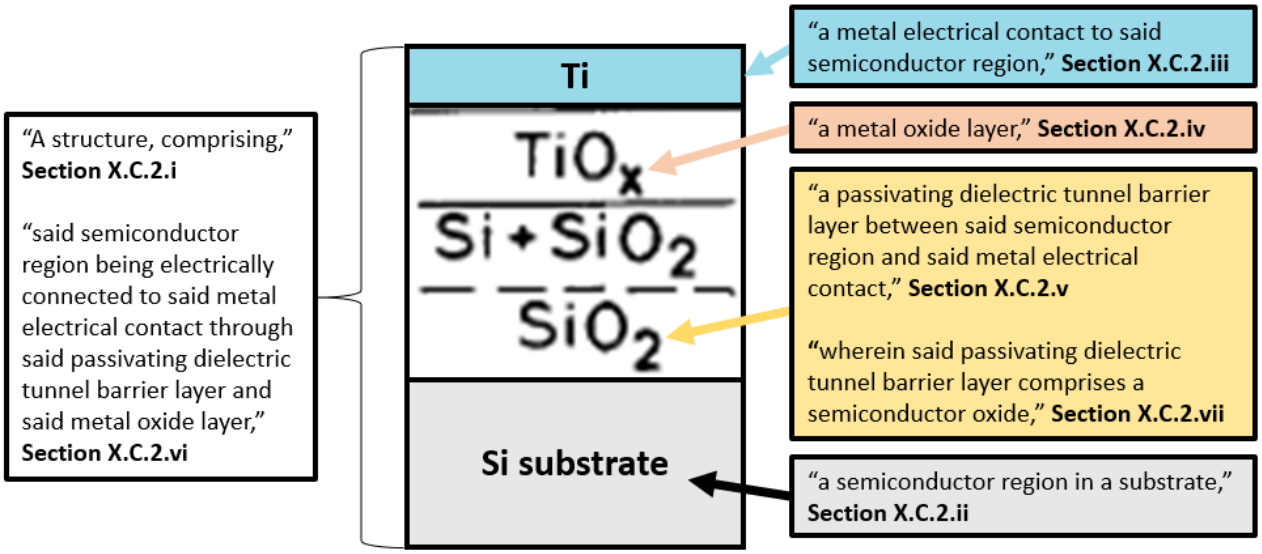
Further, an ordinarily skilled artisan would have expected that TiO_x – SiO_2 interface layer to present less electrical resistance than that presented by Goodnick's Al_2O_3 – SiO_2 interface layer. (Schubert Decl. ¶¶ 147-148.) In particular, titanium dioxide—the oxide of titanium most likely to form when titanium reacts with silicon dioxide—presents less resistance than aluminum oxide. (*Id.*; Taubenblatt 1982 at 2; Szydlo at 1, 3; Bortz at 1, 3; Lang at 4; Polishchuk at 3; Archibong at 1.) And, an ordinarily skilled artisan would have sought to provide an interface layer that reduces specific contact resistivity to reduce the power consumption of a device incorporating a contact with that interface layer. (Takahashi at 4:57-59; Schubert Decl. ¶ 149.)

Finally, turning to reasonable expectation of success, forming a TiO_x – SiO_2 interface layer described in Taubenblatt 1982 by depositing titanium on the

thermally grown 30 Å SiO_2 layer in Goodnick and annealing as described in Taubenblatt 1982 would have required nothing more than well-known, conventional semiconductor processing steps. (Schubert Decl. ¶ 150.) Growing a thermal oxide on a silicon surface, depositing titanium, and annealing were all conventional techniques well within the grasp of an ordinarily skilled artisan. (*Id.*; Goodnick at 1; Taubenblatt 1982 at 7-8; Taubenblatt 1984 at 1.)

2. Claim 1

As discussed above in **Section X.C.1**, combining Goodnick and Taubenblatt 1982 would have yielded a Ti – TiO_x – SiO_2 – Si contact. (Goodnick at 1-2; Taubenblatt 1982 at 7-8.) As the below graphic summarizes, that contact meets every limitation of Claim 1:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 151.)

i. A structure, comprising

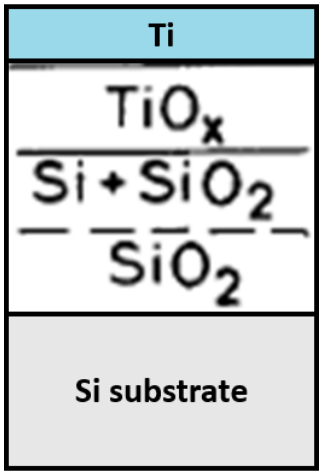
The preamble is not limiting. Nevertheless, as discussed above in **Section X.C.1**, Goodnick in view of Taubenblatt 1982 renders obvious a Ti – TiO_x – SiO_2 – Si contact, which is a structure. (Goodnick at 1-2, 5; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 152.)

ii. a semiconductor region in a substrate,

Goodnick discloses this limitation, as discussed above in **Section X.A.1.ii**. (Schubert Decl. ¶ 153.)

iii. a metal electrical contact to said semiconductor region,

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶¶ 154-155.) The combination discussed above in **Section X.C.1** would have yielded a **titanium** metal electrical contact as part of a Ti – TiO_x – SiO_2 – Si contact:

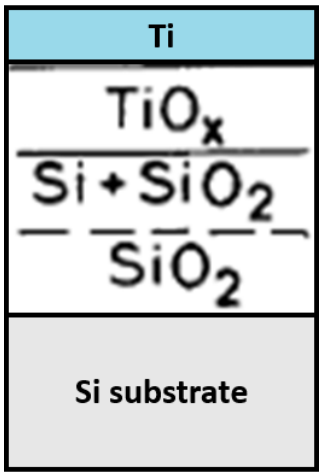


(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 154.)

Taubenblatt 1982 further explains that "in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by ***unreacted Ti metal*** or in the formation of silicide." (Taubenblatt 1982 at 8.) Because Taubenblatt 1982 discloses that the TiO_x layer forms a barrier between unreacted Ti and the SiO_2 layer, an ordinarily skilled artisan would have understood that unreacted titanium remained on top of the TiO_x layer that forms during annealing. (*Id.*; Schubert Decl. ¶ 155.) Thus, the combination of Goodnick and Taubenblatt 1982 teaches a titanium metal electrical contact.

iv. a metal oxide layer, and

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶¶ 156-157.) The combination discussed above in **Section X.C.1** would have yielded a titanium oxide (TiO_x) layer, which is a metal oxide layer:

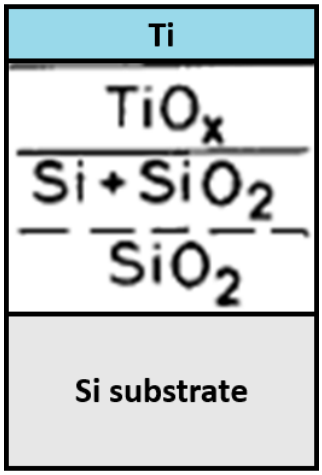


(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 156.)

Taubenblatt 1982 discloses that "in the reaction of Ti with a thicker SiO_2 layer, ***Ti oxide forms***, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide." (Taubenblatt 1982 at 8; Schubert Decl. ¶ 157.)

v. a passivating dielectric tunnel barrier between said semiconductor region and said metal electrical contact,

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶¶ 158-159.) The combination discussed above in **Section X.C.1** would have left some of the silicon dioxide (SiO_2) layer on Goodnick's silicon substrate, which puts that remaining SiO_2 layer between the silicon substrate (semiconductor region) and the deposited titanium (metal electrical contact):



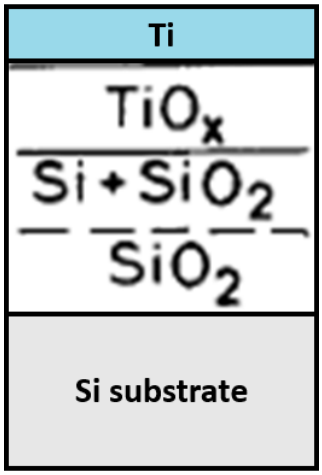
(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 158.)

Taubenblatt 1982 explains that the titanium reduces the SiO_2 grown on the silicon substrate to form titanium oxide and free silicon, but leaves some SiO_2 on the

surface of the silicon: "in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide." (Taubenblatt 1982 at 8.) That remaining layer of SiO_2 grown on the silicon substrate is a passivating dielectric tunnel barrier between said semiconductor region and said metal electrical contact for the reasons discussed above in **Section X.A.1.v**. (Schubert Decl. ¶ 159.)

vi. said semiconductor region being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer and said metal oxide layer,

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶¶ 160-165.) The combination discussed above in **Section X.C.1** would have yielded the following structure:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 160.)

In that structure, the silicon substrate (semiconductor region) is electrically connected to the titanium (metal electrical contact) through an SiO_2 layer (said

passivating dielectric tunnel barrier layer) and a TiO_x layer (said metal oxide layer). Three features demonstrate that the silicon substrate and the titanium are electrically connected. *First*, Goodnick describes its interfacial oxide layers as "thin," and states that "an oxide layer that is sufficiently thin may sustain considerable current via tunneling." (Goodnick at 1; Schubert Decl. ¶ 162.) *Second*, an ordinarily skilled artisan would have known that converting some of the interfacial SiO_2 to a titanium oxide (as occurs during the annealing process) would have decreased the specific contact resistivity of the structure. (Kim at 4:63-5:1; Schubert Decl. ¶ 163.) *Third*, an ordinarily skilled artisan would have recognized that because Goodnick's silicon substrate is n-type doped, the interfacial SiO_2 layer would have decreased the barrier height between that n-type doped silicon substrate and the titanium, also reducing the structure's specific contact resistivity. (Goodnick at 1; Taubenblatt 1984 at 3; Schubert Decl. ¶ 164.)

vii. wherein said passivating dielectric tunnel barrier layer comprises a semiconductor oxide.

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶ 166.) As discussed above in **Section X.C.2.v**, the combination of Goodnick and Taubenblatt 1982 yields a silicon dioxide (SiO_2) passivating dielectric tunnel barrier layer. (*Id.*; Goodnick at 1-2, 5; Taubenblatt 1982 at 7-8.)

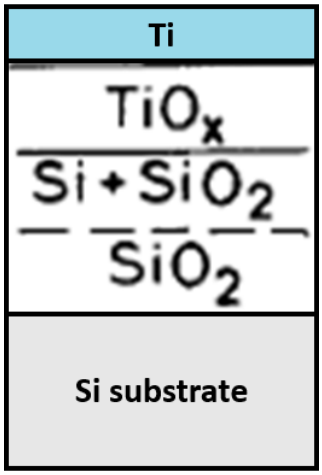
3. Claim 3

i. The structure of claim 1,

Goodnick and Taubenblatt 1982 render obvious the structure of Claim 1, as discussed above in **Section X.C.2**. (Schubert Decl. ¶ 168.)

ii. wherein the semiconductor oxide of the dielectric tunnel barrier layer has a thickness of approximately 0.1 nm to 5 nm.

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶¶ 169-173.) The combination discussed above in **Section X.C.1** would have yielded the following structure:



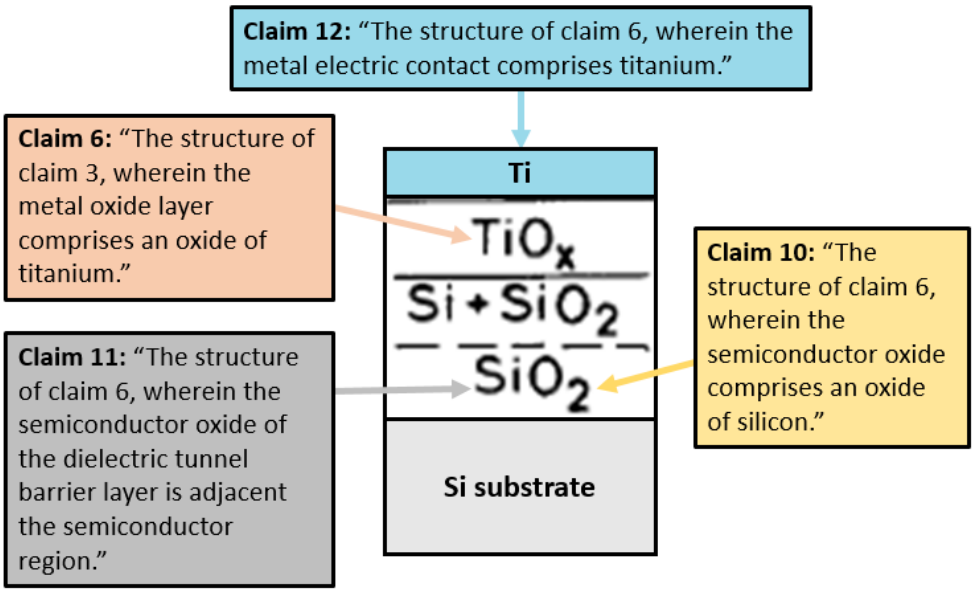
(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶¶ 138, 170.)

Taubenblatt 1982 further explains that the titanium reduces that SiO_2 to form titanium oxide and free silicon, but leaves some SiO_2 remaining. (Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 171.) The SiO_2 layer remaining after titanium deposition and annealing therefore must be less than the thickness of the original SiO_2 layer,

which was 30 Å, or 3 nm. (Goodnick at 1-2; Schubert Decl. ¶ 172.) The minimum possible thickness of that SiO_2 layer is 2 angstroms (0.2 nm), which is the monolayer thickness of SiO_2, *i.e.*, a layer one SiO_2 molecule thick. (Verhaverbeke at [0004]; Schubert Decl. ¶ 172.) Thus, the thickness of the SiO_2 in the Goodnick-Taubenblatt 1982 combination is between 0.2 nm and 3 nm, satisfying this limitation. (Schubert Decl. ¶ 173.)

4. Claims 6 and 10-12

Claim 6 depends on Claim 3; Claims 10, 11 and 12 depend on Claim 6. Goodnick in view of Taubenblatt 1982 renders Claim 3 obvious, as discussed above in **Section X.C.3.** (Schubert Decl. ¶ 174.) The structure produced by combining Goodnick and Taubenblatt 1982 as discussed above in **Section X.C.1** also satisfies every limitation of Claims 6, 10, 11, and 12, as summarized below:

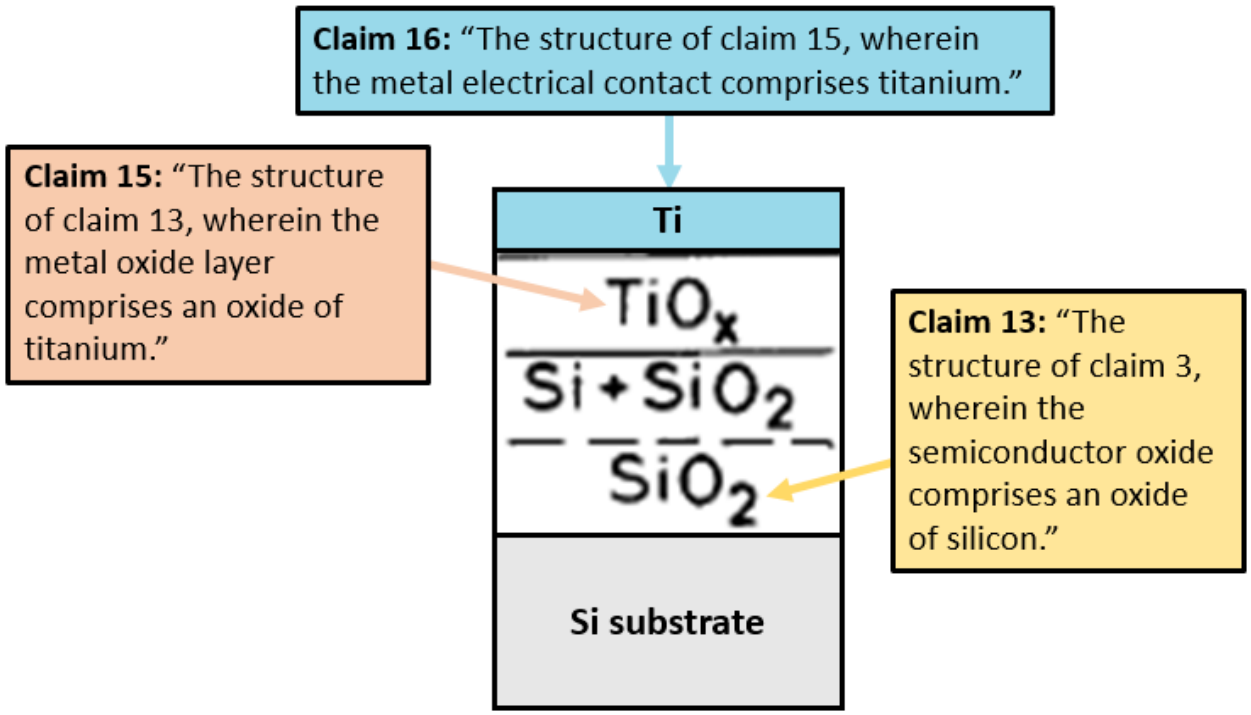


(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 174.)

Turning to each claim in detail, Claim 6 specifies that the metal oxide layer comprises an oxide of titanium; the combination of Goodnick and Taubenblatt 1982 teaches a TiO_x (titanium oxide) layer, as discussed above in **Section X.C.2.iv**. (Schubert Decl. ¶ 175.) Claim 10 specifies that the semiconductor oxide comprises an oxide of silicon; the combination of Goodnick and Taubenblatt 1982 teaches an SiO_2 (silicon dioxide) layer, as discussed above in **Section X.C.2.v**. (Schubert Decl. ¶ 176.) Claim 11 specifies that the semiconductor oxide of the dielectric tunnel barrier layer is adjacent to the semiconductor region; the combination of Goodnick and Taubenblatt 1982 teaches an SiO_2 (silicon dioxide) layer grown on a silicon substrate and that remains on (and therefore adjacent to) a silicon substrate, as discussed above in **Section X.C.2.v**. (Schubert Decl. ¶ 177.) Finally, Claim 12 specifies that the metal electrical contact comprises titanium; Taubenblatt 1982 describes a titanium electrical contact, as discussed above in **Section X.C.2.iii**. (Schubert Decl. ¶ 178.)

5. Claims 13, 15, and 16

Claim 13 depends on Claim 3; Claims 15 and 16 depend directly or indirectly from Claim 13. Goodnick in view of Taubenblatt 1982 renders Claim 3 obvious, as discussed above in **Section X.C.3**. (Schubert Decl. ¶ 180.) The structure produced by combining Goodnick and Taubenblatt 1982 as discussed above in **Section X.C.1** also meets every limitation of Claims 13, 15, and 16, as summarized below:

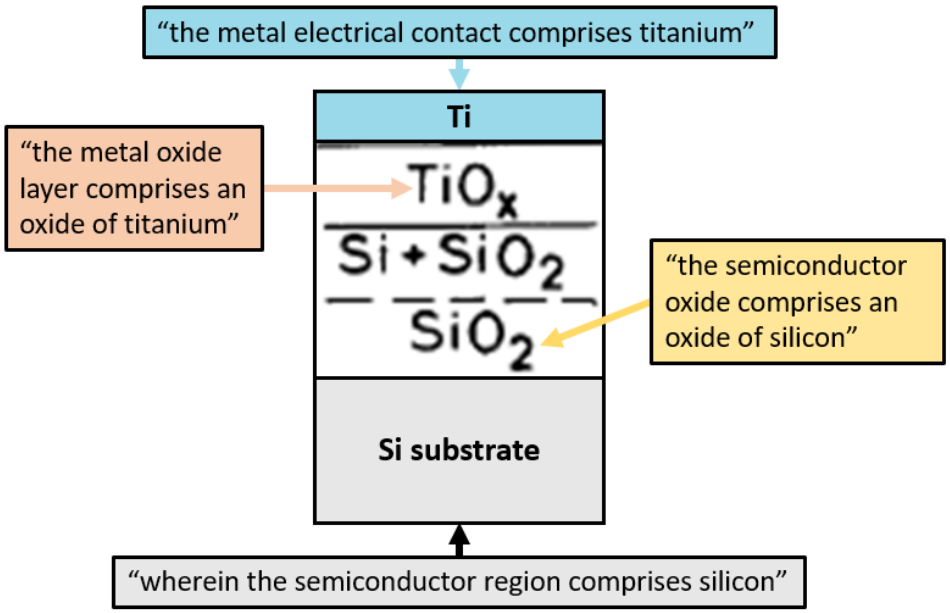


(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 180.)

Turning to each claim in detail, Claim 13 specifies that the semiconductor oxide comprises an oxide of silicon; the combination of Goodnick and Taubenblatt 1982 teaches an SiO_2 (silicon dioxide) layer that satisfies that limitation for the reasons discussed above in **Section X.C.2.v**. (Schubert Decl. ¶ 181.) Claim 15 specifies that the metal oxide layer comprises an oxide of titanium; the combination of Goodnick and Taubenblatt 1982 teaches a TiO_x layer that satisfies that limitation as discussed above in **Section X.C.2.iv**. (*Id.* ¶ 182.) Finally, Claim 16 specifies that the metal electrical contact comprises titanium; Taubenblatt 1982 describes a titanium electrical contact as discussed above in **Section X.C.2.iii**. (*Id.* ¶ 183.)

6. Claim 19

Claim 19 depends on Claim 1. Goodnick in view of Taubenblatt 1982 renders Claim 1 obvious, as discussed above in **Section X.C.2**. (Schubert Decl. ¶ 185.) The structure produced by combining Goodnick and Taubenblatt 1982 as discussed above in **Section X.C.1** also meets every limitation of Claim 19:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 185.)

Turning to each limitation, the combination of Goodnick and Taubenblatt 1982 teaches a semiconductor region comprising silicon as discussed above in **Section X.C.2.ii**. (Schubert Decl. ¶ 186.) That combination also teaches a semiconductor oxide comprising an oxide of silicon—namely, an SiO_2 (silicon dioxide) layer—as discussed above in **Section X.C.2.v**. (*Id.* ¶ 187.) That combination further teaches a metal oxide layer that comprises an oxide of titanium—a TiO_x (titanium oxide) layer—as discussed above in **Section X.C.2.iv**.

(*Id.* ¶ 188.) Finally, that combination teaches a metal electrical contact that comprises titanium, as discussed above in **Section X.C.2.iii**. (*Id.* ¶ 189.)

7. Claim 20

i. The structure of claim 1,

Goodnick in view of Taubenblatt 1982 renders Claim 1 obvious, as discussed above in **Section X.C.2**. (Schubert Decl. ¶ 191.)

ii. wherein the dielectric tunnel barrier layer is configured to reduce a height of a Schottky barrier between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶¶ 192-194.) As discussed above in **Section X.C.2.vii**, the combination of Goodnick and Taubenblatt 1982 yields an interface layer with an SiO_2 layer that passivates the surface of an n-type silicon substrate. (*Id.* ¶ 193; Goodnick at 1-2; Taubenblatt 1982 at 7-8.) That SiO_2 layer also reduces the Schottky barrier height between the titanium (the metal electrical contact) and the n-type silicon substrate (the semiconductor region) from the barrier height that would have existed without the SiO_2 layer disposed between them. Referring to titanium and hafnium, Taubenblatt 1984 discloses that "interfacial SiO_2 does increase (decrease) the barrier of these metals p-type (n-type) silicon by more than

0.1 eV." (Taubenblatt 1984 at 3.) The "decrease" that Taubenblatt 1984 describes is against a contact between titanium and a fully cleaned n-type silicon substrate where the oxide has been removed. (Taubenblatt 1984 at 2-3; Schubert Decl. ¶ 194.) Thus, the remaining SiO_2 layer is configured to reduce a height of a Schottky barrier between the metal electrical contact (titanium) and the semiconductor region (n-type silicon) from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.

8. Claim 22

i. The structure of claim 1,

Goodnick in view of Taubenblatt 1982 renders Claim 1 obvious, as discussed above in **Section X.C.2**. (Schubert Decl. ¶ 196.)

ii. wherein the dielectric tunnel barrier layer is configured to reduce contact resistivity between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶¶ 197-199.) As discussed above for Claim 20 in **Section X.C.7.ii**, the SiO_2 layer produces a net reduction in barrier height between the metal electrical contact (titanium) and the semiconductor region (n-type silicon)

from the barrier height that would have existed without the SiO_2 layer. (Schubert Decl. ¶¶ 192-194; Taubenblatt 1984 at 3.) Specific contact resistivity depends on barrier height, so decreasing the barrier height between the metal electrical contact (titanium) and the semiconductor region (n-type silicon) would have decreased specific contact resistivity. (Schubert Decl. ¶ 199, Chang at 5-6.)

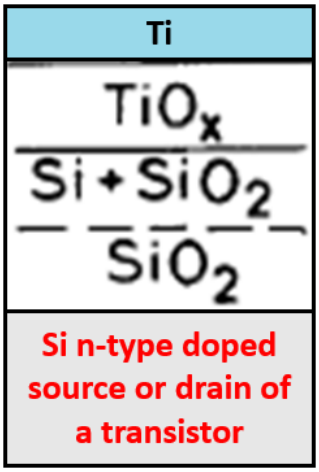
Finally, "contact resistivity" is interchangeable with "specific contact resistivity," so decreasing specific contact resistivity decreases "contact resistivity." (Carver at 2; Schubert Decl. ¶ 199.) And if "contact resistivity" is construed to refer to specific contact resistivity divided by the area of the contact—another quantity to which "contact resistivity" refers—the result would be the same: reducing specific contact resistivity would also reduce specific contact resistivity divided by the area of the contact. (Schubert Decl. ¶ 199.)

D. Ground 4: Goodnick in view of Jammy and Taubenblatt 1982 renders Claims 8 and 17 obvious.

1. Combination of Goodnick, Jammy, and Taubenblatt 1982

As discussed above in **Section X.B.1**, an ordinarily skilled artisan would have found it obvious to grow Goodnick's 30 Å SiO_2 layer on Jammy's n-type doped source or drain of a transistor in a silicon substrate, then to deposit aluminum on that 30 Å SiO_2 layer. (Schubert Decl. ¶ 200.) Further, as discussed above in **Section X.C.1,** an ordinarily skilled artisan would have both (1) deposited Taubenblatt 1982's titanium on that 30 Å SiO_2 layer instead of Goodnick's aluminum; and (2)

annealed the resulting structure at 700ºC - 900ºC as taught by Taubenblatt 1982. (Schubert Decl. ¶ 201.) Depositing titanium as taught by Taubenblatt 1982[3] on Goodnick's 30 Å SiO_2 layer grown on Jammy's n-type doped source or drain of a transistor in a silicon substrate and annealing at 700ºC - 900ºC as taught by Taubenblatt 1982 would have yielded the following structure for use in a transistor:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:9-12, 4:33-38; Schubert Decl. ¶ 202.)

[3] As an obvious alternative, Jammy describes depositing conductive studs on its "quantum conductive barrier," and incorporates titanium conductive studs. (Jammy at Fig. 1, 4:5-8 (incorporating the Cote patent by reference); Cote at 8:24-28 (titanium conductive studs).) Depositing Jammy's titanium conductive studs would have been equally suitable, and would have yielded the same TiO_x – SiO_2 interface layer owing to the formation of the TiO_x diffusion barrier layer during Taubenblatt 1982's annealing process. (Schubert Decl. ¶ 202 n.13; Taubenblatt 1982 at 8.)

In addition to the reasons for combining Goodnick and Jammy as discussed above in **Section X.B.1** and the reasons for combining Goodnick and Taubenblatt 1982 as discussed above in **Section X.C.1**, there is an additional reason to use the TiO_x – SiO_2 interface layer provided by combining Goodnick and Taubenblatt 1982 with Jammy's source or drain of a transistor. As discussed above in **Section X.C.1**, that TiO_x – SiO_2 interface layer would have reduced the specific contact resistivity of a device incorporating that interface layer (such as Jammy's transistor), reducing the device's power consumption. (Takahashi at 4:57-59; Schubert Decl. ¶ 203.) Further, reducing specific contact resistivity would have been especially desirable for a transistor because it would have avoided deteriorating the transistor's switching frequency. (Sakurai at 6; Yeh at 2:54-64; Schubert Decl. ¶ 203.)

Finally, as the combination of Goodnick, Jammy, and Taubenblatt 1982 involves only (1) swapping Goodnick's silicon substrate for Jammy's source or drain of a transistor; and (2) performing conventional semiconductor processing steps, an ordinarily skilled artisan would have had a reasonable expectation of successfully combining those references. (Schubert Decl. ¶ 204.)

2. Claim 8

i. The structure of claim 6,

Goodnick in view of Taubenblatt 1982 renders Claim 6 obvious, as discussed above in **Section X.C.4**. (Schubert Decl. ¶ 206.)

ii. wherein the semiconductor region comprises an n-type doped source or drain of a transistor.

This limitation also appears in Claim 4. Jammy discloses this limitation, as discussed above in **Section X.B.2.ii**. (Schubert Decl. ¶ 207.)

3. Claim 17

i. The structure of claim 15,

Goodnick in view of Taubenblatt 1982 renders Claim 15 obvious, as discussed above in **Section X.C.5**. (Schubert Decl. ¶ 209.)

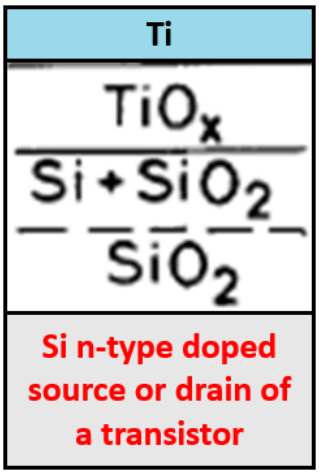
ii. wherein the semiconductor comprises an n-type doped source or drain of a transistor.

The meaning of this limitation is unclear, as there is no antecedent basis for the term "the semiconductor" in either Claim 17 or the claims from which Claim 17 depends. But, Jammy discloses a semiconductor that comprises an n-type doped source or drain of a transistor, as discussed above in **Section X.B.2.ii**. (Schubert Decl. ¶ 210.).

E. Ground 5: Goodnick in view of Jammy, Taubenblatt 1982, and Chang renders Claims 18 and 25-30 obvious.

1. Combination of Goodnick, Jammy, Taubenblatt 1982, and Chang

As discussed above in **Section X.D.1**, an ordinarily skilled artisan would have combined Goodnick, Jammy, and Taubenblatt 1982 to achieve the structure below:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:9-12, 4:33-38; Schubert Decl. ¶ 211.)

That combination of Goodnick, Jammy, and Taubenblatt 1982 does not expressly describe any specific contact resistivity. Nonetheless, an ordinarily skilled artisan would have been motivated to provide an interface layer configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω-μm^2, and would have had a reasonable expectation of achieving a specific contact resistivity in the claimed range based on the combined teachings of Goodnick, Jammy, Taubenblatt 1982, and Chang. (Schubert Decl. ¶ 212.)

In particular, Jammy does not expressly disclose any doping level for its n-type silicon **source/drain diffusion regions**. (Jammy at 4:33-38.) But, an ordinarily skilled artisan would have known that using high levels of doping for those n-type silicon **source/drain diffusion regions** would have reduced specific contact resistivity even further. (Schubert Decl. ¶ 213.) As Chang describes, at doping

levels above 10^{18} dopant atoms / cm^3, specific contact resistivity "becomes a strong function of doping," with specific contact resistivity decreasing as doping increases (Chang at 4-5.) Chang also describes doping levels for n-type silicon as high as 10^{21} dopant atoms / cm^3. (*Id.* at 7 (Fig. 5), Abstract.) An ordinarily skilled artisan would have been motivated to use Chang's high doping levels for Jammy's n-type silicon source/drain diffusion regions to further reduce specific contact resistivity. (Schubert Decl. ¶ 214.) In turn, reducing specific contact resistivity would have been desirable in Jammy's transistor for the reasons discussed above in **Section X.D.1**: improved switching speed and reduced power consumption. (*Id.* ¶ 215.)

By both (1) increasing the doping levels of Jammy's n-type doped source/drain to reduce specific contact resistivity and (2) disposing a specific-contact-resistivity-lowering TiO_x – SiO_2 interface layer between the titanium metal electrical contact and Jammy's n-type doped silicon source/drain diffusions, an ordinarily skilled artisan would have reasonably expected to achieve a specific contact resistivity of less than 1 Ω-μm^2. (Schubert Decl. ¶ 216.)

Indeed, ordinarily skilled artisans had already succeeded in reducing specific contact resistivity below 10 Ω-μm^2 using an interface layer. The Kim patent, issued in 1989, describes obtaining a specific contact resistance (resistivity) as low as 8 Ω-μm^2 for a junction between a Ti-W (titanium-tungsten) alloy and n-type silicon with an interfacial oxide layer that includes titanium dioxide therebetween. (Kim at 4:63-

5:1, 5:27-30.) Although it does not describe an interface layer, the Hara publication describes that a specific contact resistance (resistivity) of about 10^{-8} Ω-cm^2, which converts to about 1 Ω-μm^2, could have been achieved within the technical limits that existed as of Hara's 1996 filing date. (Hara at 2:55-56; Schubert Decl. ¶ 217.)

But an ordinarily skilled artisan would have reasonably expected to ***improve*** on Kim's and Hara's specific contact resistivities by combining Goodnick, Jammy, Taubenblatt 1982, and Chang. (Schubert Decl. ¶¶ 218-221.) At doping levels above 10^{18} dopant atoms / cm^3, specific contact resistivity "becomes a strong function of doping," decreasing as doping increases. (Chang at 4-5.) Hara describes using a doping level of about 10^{20} atoms / cm^3, achieving a 1 Ω-μm^2 specific contact resistivity. (Hara at 2:50-56.) While Hara describes that concentration as an "upper limit," Kim describes using doping levels as high as 3 x 10^{20} arsenic atoms / cm^3 for n-type doped silicon, achieving an 8 Ω-μm^2 specific contact resistivity. (Kim at 5:27-30.)

But Chang describes achieving an even higher doping concentration for n-type silicon. In particular, Chang describes a doping concentration for n-type doped silicon as high as 10^{21} dopant atoms / cm^3—more than triple the concentration described in Kim, and ten times the concentration described in Hara. (Chang at 7 (Fig. 5), Abstract; Kim at 5:27-30; Hara at 2:50-56; Schubert Decl. ¶ 219.) And, an ordinarily skilled artisan would have reasonably expected to successfully n-type

dope Jammy's silicon source or drain of a MOSFET to a concentration of 10^{21} dopant atoms / cm^3. For example, U.S. Patent No. 6,521,502 to Yu, filed in August 2000, describes implanting n-type dopants into silicon source or drain regions of a MOSFET to a concentration of up to 10^{21} dopant atoms / cm^3. (Yu at 4:4-12, 4:43-48; Schubert Decl. ¶ 220.)

Using the higher doping concentration described in Chang in Jammy's n-type source or drain of a transistor gives the combination of Goodnick, Jammy, Taubenblatt 1982, and Chang a feature for reducing specific contact resistance that Kim and Hara lack: n-type silicon doped to a concentration as high as 10^{21} dopant atoms / cm^3. (Schubert Decl. ¶ 221.) And, when used with that higher doping concentration, the specific-contact-resistivity-minimizing TiO_x – SiO_2 interface layer described above would have given an ordinarily skilled artisan a reasonable expectation of successfully achieving a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω-μm^2. (*Id* .)

2. Claim 18

i. The structure of claim 17,

Goodnick in view of Jammy and Taubenblatt 1982 renders Claim 17 obvious, as discussed above in **Section X.D.3**. (Schubert Decl. ¶ 223.)

ii. wherein a specific contact resistivity between the n-type doped source or drain and the metal electric contact is less than 1 Ω-μm^2.

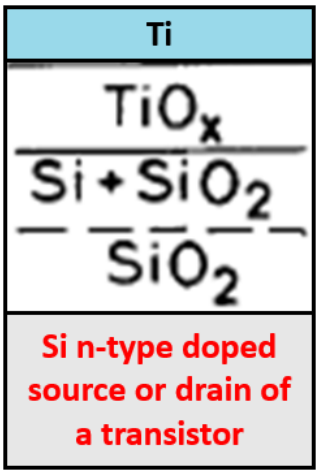
Goodnick in view of Jammy, Taubenblatt 1982, and Chang renders this limitation obvious. (Schubert Decl. ¶ 224.) As discussed above in **Section X.E.1**, an ordinarily skilled artisan would have been motivated to combine Jammy, Goodnick, Taubenblatt 1982, and Chang to provide a specific contact resistivity of less than 1 Ω-μm^2 between Jammy's n-type doped silicon source or drain and the titanium electrical contact of Taubenblatt 1982 (or Jammy). (*Id.*)

3. Claim 25

i. An electrical junction comprising

The preamble is not limiting. Nonetheless, it would have been obvious over Goodnick in view of Jammy and Taubenblatt 1982. (Schubert Decl. ¶¶ 226-229.) As discussed above in **Section X.D.1**, the combination of Goodnick, Jammy, and Taubenblatt 1982 would have yielded a Ti – TiO_x – SiO_2 – Si contact. (*Id.* ¶ 226.) That contact is an "electrical junction" as described and claimed in the '691 Patent, which uses the terms "junction" and "contact" interchangeably. (*Id.* ¶¶ 227-228; '691 Patent at 1:39-41, 7:61-8:8, 13:7-10, 17:28-31.) Further, as discussed above in **Section X.C.1.vi**, the TiO_x – SiO_2 interface provided by the combination of Goodnick and Taubenblatt 1982 would have permitted current to flow between the metal and the semiconductor on either side of the interface layer. (*Id.* ¶ 229.) That

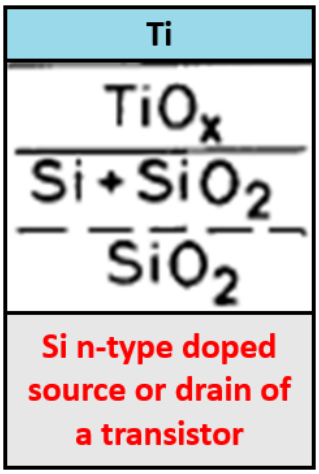
interface layer lies between titanium and Jammy's n-type doped source or drain of a transistor, which constitutes a metal—interface layer—semiconductor junction:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:9-12, 4:33-38; Schubert Decl. ¶ 229.)

ii. an interface layer disposed between a contact metal and a semiconductor,

This limitation would have been obvious over Goodnick in view of Jammy and Taubenblatt 1982. (Schubert Decl. ¶ 230.) As discussed above in **Section X.D.1**, that combination would have yielded a TiO_x – SiO_2 interface layer between a contact metal (titanium) and a semiconductor (Jammy's n-type doped source or drain of a transistor in a silicon substrate):



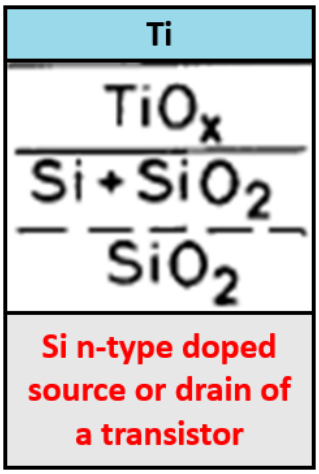
(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:9-12, 4:33-38; Schubert Decl. ¶ 230.)

iii. the semiconductor comprising a source or drain of a transistor,

Jammy discloses this limitation. (Schubert Decl. ¶ 231.) In particular, Jammy discloses a silicon substrate that includes an n-type doped source or drain of a MOSFET (metal oxide semiconductor field effect transistor), which Jammy calls a source/drain diffusion region. (Jammy at 4:1-4, 4:9-12, 4:33-38.)

iv. the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer and

This limitation would have been obvious over Goodnick in view of Jammy and Taubenblatt 1982. (Schubert Decl. ¶¶ 232-234.) As discussed above in **Sections X.C.1 and X.D.1**, the combination of Goodnick, Jammy, and Taubenblatt 1982 would have yielded the following structure:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:9-12, 4:33-38; Schubert Decl. ¶ 232.)

The titanium oxide (TiO_x) is an example of a metal oxide separation layer; indeed, the specification of the '691 Patent expressly identifies titanium dioxide, an oxide of titanium, as an example of a "spacer" layer. ('691 Patent at 17:60-62; Schubert Decl. ¶ 233.) And the remaining silicon dioxide (SiO_2) layer grown on the surface of Jammy's n-type silicon source/drain diffusion according to Goodnick's teachings is a semiconductor oxide passivation layer for at least the reasons discussed above in **Sections X.A.1.v and X.C.2.v**. (Schubert Decl. ¶ 234; Goodnick at 1-2.)

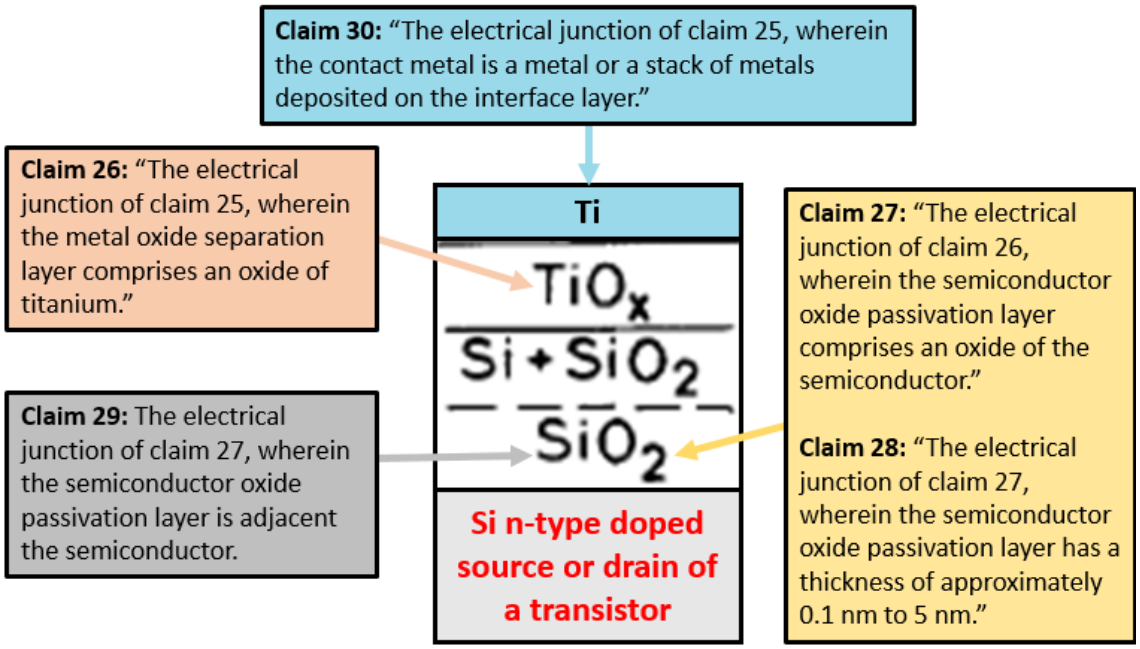
v. configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω-μm^2.

Jammy in view of Goodnick, Taubenblatt 1982, and Kim render this limitation obvious. (Schubert Decl. ¶ 235.) As discussed above in **Section X.E.1**, an ordinarily skilled artisan would have been motivated to combine Jammy, Goodnick,

Taubenblatt 1982, and Chang to provide a specific contact resistivity of less than 1 Ω-μm^2 between Jammy's n-type doped silicon source or drain and a titanium contact metal as described in Taubenblatt 1982, and would have had a reasonable expectation of successfully doing so. (*Id.*)

4. Claims 26-30

Claim 25, from which Claims 26-30 directly or indirectly depend, would have been obvious over Goodnick in view of Jammy, Taubenblatt 1982, and Chang, as discussed above in **Section X.E.3**. Further, the structure produced by combining Goodnick, Taubenblatt 1982, and Jammy as discussed above in **Section X.D.1**, which structure is part of the combination of references asserted against Claim 25, also satisfies every limitation of Claims 26-30, as summarized below:

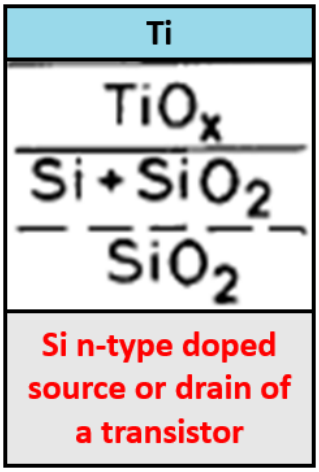


(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:9-12, 4:33-38; Schubert Decl. ¶ 236.)

Claim 26 specifies that the metal oxide separation layer comprises an oxide of titanium. The interface layer provided by combining Goodnick and Taubenblatt 1982 includes a titanium oxide (TiO_x) separation layer, as discussed above in **Sections X.C.1 and X.E.3.iv**. (Schubert Decl. ¶ 237.) Claim 27 specifies that the semiconductor oxide passivation layer comprises an oxide of the semiconductor; Claim 28 specifies that the semiconductor oxide passivation layer has a thickness of approximately 0.1 nm to 5 nm; and Claim 29 specifies that the semiconductor oxide passivation layer is adjacent the semiconductor. The interface layer provided by combining Goodnick and Taubenblatt 1982 includes an SiO_2 (semiconductor oxide) passivation layer between 0.2 nm and 3 nm thick and that was grown on (and therefore adjacent to) Jammy's n-type doped source or drain of a transistor, as discussed above in **Sections X.C.1**; **X.C.3.ii** (remaining SiO_2 layer has a thickness between 0.2 nm and 3 nm); **X.C.2.v and X.E.3.iv** (remaining SiO_2 passivates silicon surface); **and X.C.4** (remaining SiO_2 is adjacent the semiconductor on which it is grown). (Schubert Decl. ¶¶ 238-240.)

Finally, Claim 30 specifies that the contact metal is a metal or stack of metals deposited on the interface layer. As discussed above in **Sections X.C.1 and X.D.1**, it would have been obvious to deposit titanium on Goodnick's 30 Å layer of SiO_2 per either Taubenblatt 1982 or Jammy and to anneal as taught by Taubenblatt 1982. (Schubert Decl. ¶ 241.) Taubenblatt 1982 discloses that "in the reaction of Ti with

a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide." (Taubenblatt 1982 at 8.) Because of that diffusion barrier, unreacted deposited titanium would have remained on top of the TiO_x portion of the interface layer:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:9-12, 4:33-38; Schubert Decl. ¶ 241.)

F. Alleged Secondary Considerations for Grounds 2-5

Below, Petitioner addresses any alleged secondary considerations of non-obviousness currently of record. Petitioner reserves the right to address in its reply any alleged secondary considerations that Acorn presents. Here, any alleged secondary considerations currently of record have no nexus to the claims. They relate to either unclaimed features or features in the prior art, neither of which can provide nexus.

To start, while the specification purports to describe unexpected results related to silicon nitride layers ('691 Patent at 12:17-24), no challenged claim has a silicon

nitride layer. (Schubert Decl. ¶ 243.) Likewise, while Acorn's complaint in the Acorn Litigation alleges unexpected results and industry recognition related to the inventors' purported achievement of low specific contact resistances using an interface layer, only Claims 18 and 25-30 specify any particular specific contact resistivity. (Ex. 1146 ¶¶ 6, 48, 50, 51.) And, Acorn's complaint does not relate those alleged low specific contact resistances to any particular value for specific contact resistivity. (*Id.*)

Moreover, prior art such as Schroen and Iwaguro taught that using an interface layer in a metal-semiconductor junction can reduce specific contact resistance. (Schubert Decl. ¶¶ 245-246; Schroen at Abstract; Iwaguro at [0005]-[0006], [0012]-[0014].) Indeed, Iwaguro taught that an interface layer could reduce specific contact resistance by a factor of at least 100. (Schubert Decl. ¶ 246; Iwaguro at Fig. 3.) Further, the Hara patent application disclosed that a specific contact resistance (resistivity) of 1 Ω-μm^2 was achievable without an interface layer but within the technical limits that existed as of Hara's 1996 filing date. (Hara at 2:55-56; Schubert Decl. ¶ 247.) And, as discussed above in **Section X.E.1**, an ordinarily skilled artisan would have expected to improve on that specific contact resistivity by combining Goodnick, Jammy, Taubenblatt 1982, and Chang. (*Id.*) Thus, the specific contact resistivities in Claims 18 and 25-30 could not have provided a nexus to the alleged unexpected results and industry recognition in Acorn's complaint. (*Id.* ¶ 248.)

XI. The discretionary factors favor instituting trial.

A. 35 U.S.C. § 325(d)

The Office did not consider any of Goodnick, Taubenblatt 1982, or Chang during the prosecution of either the '691 Patent or its parent applications. And while Examiners signed off on Jammy in information disclosure statements in the '691 Patent and a parent application, no further consideration of Jammy with respect to the '691 Patent is of record. (Ex. 1112, at 391-392; Ex. 1114, at 128.) Crucially, no Examiner cited Jammy against any claim of the '691 Patent or of any parent application. And those signatures by themselves do not warrant denying institution, especially as Petitioner has combined Jammy with three new references here. *See*, *e.g.*, *Zip Top, LLC v. Stasher, Inc.*, Case IPR2018-01216, Paper 14, at 35-36 (PTAB Jan. 17, 2019); *Navistar, Inc. v. Fatigue Fracture Tech., LLC*, Case IPR2018-00853, Paper 13, at 16-17 (PTAB Sept. 12, 2018).

B. 35 U.S.C. § 314(a)

1. *General Plastic*

Petitioner filed this petition shortly after its earlier-filed petition in Case IPR2020-01206. But as this petition's filing date, nothing has happened in Case IPR2020-01206. Thus, *General Plastic* factors do not weigh against institution, especially if the Board elects to institute only one petition. *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, Case IPR2016-01357, Paper 19, at 9-10

(PTAB Sept. 6, 2017) (designated precedential). But, the Board should institute both petitions for the reasons in Petitioner's concurrent five-page submission.

2. *NHK Spring / Apple*

Despite concurrent litigation involving the '691 Patent, discretionary denial of institution under *NHK Spring Co., Ltd. v. Intri-Plex Techs., Inc.*, Case IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (designated precedential) is unwarranted. Congress gave *inter partes* review petitioners a full year to file a petition after service of an infringement complaint. 35 U.S.C. § 315(b). And with good reason: Congress recognized that petitioners deserved a "reasonable opportunity to identify and understand the patent claims that are relevant to the litigation" when a patent owner asserts "multiple patents with large numbers of vague claims." Joe Matal, *A Guide to the Legislative History of the America Invents Act: Part II of II*, 21 FED. CIR. B.J. 539, 611-612 (2012) (quoting 157 Cong. Rec. S5429 (daily ed. Sept. 8, 2011) (statement of Sen. Kyl)).

Here, Acorn has asserted ***108 claims across six patents*** in the Acorn Litigation, including ***23 claims of the '691 Patent***—precisely the scenario that Congress envisioned. (Ex. 1149; Ex. 1150.) Thus, denying institution because of the Acorn Litigation would contradict Congress's intent in enacting the AIA. Further, the six factors in *Apple, Inc. v. Fintiv, Inc.*, Case IPR2020-00019, Paper 11, at 6 (PTAB Mar. 20, 2020) (designated precedential) collectively favor institution.

i. *Apple* factor 1: whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted

This factor favors instituting trial. Petitioner will be promptly moving to stay the Acorn Litigation after filing this petition. Although the Court presiding over the Acorn Litigation infrequently grants pre-institution motions to stay, it nonetheless invites defendants to renew their motions to stay once the Board institutes trial. And it has granted those renewed motions to stay even when the stage of the case has significantly advanced in the interim—even after claim construction. *Image Processing Techs. LLC v. Samsung Elecs. Co., Ltd.*, Case No. 2:16-cv-505-JRG, 2017 WL 10185855, at *1 (E.D. Tex. Feb. 17, 2017) (denying pre-institution motion to stay); 2017 WL 2672616 (E.D. Tex. June 21, 2017) (claim construction order); 2017 WL 7051628, at *1 (E.D. Tex. Oct. 25, 2017) (granting Samsung's renewed motion to stay after the Board instituted *inter partes* review, four months after the claim construction order).

ii. *Apple* factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision

Although the district court's trial date is currently ahead of the Board's projected statutory deadline for the final written decision, that trial date does not favor denying institution here. While the Acorn Litigation trial is currently scheduled for April 2021 (Ex. 1148), jury trial dates—to say nothing of dates for

post-trial briefing—are inherently subject to change. *Precision Planting, LLC v. Deere & Co.*, Case IPR2019-01044, Paper 17, at 15 (PTAB Dec. 2, 2019). The inherent uncertainty in any district court schedule weighs against denying institution, and especially here given the Acorn Litigation Court's willingness to enter a stay when the Board institutes trial. *Image Processing Techs.*, 2017 WL 7051628, at *1.

iii. *Apple* factor 3: investment in the parallel proceeding by the court and the parties

This factor largely overlaps with factor 2; for similar reasons, it does not favor denying institution. Whatever investment in the Acorn Litigation that the parties and Court might make between now and the Board's institution decision, the Acorn Litigation Court is willing to stay even advanced cases for instituted *inter partes* reviews. *Image Processing Techs.*, 2017 WL 7051628, at *1.

Further, "it is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding." *Apple*, Case IPR2020-00019, Paper 11, at 11. Here, Acorn identified only one representative claim for each of six patents in its October 2019 complaint, including only one claim of the '691 Patent. (Ex. 1146 ¶¶ 63, 73, 83, 93, 103, 113.) Later, in March 2020, Acorn served its infringement contentions—which collectively span ***108 claims*** across those six patents, including ***22*** previously unidentified claims of the '691 Patent. (Ex. 1149; Ex. 1150.) Petitioner promptly filed its petitions against those 108 asserted claims after receiving those infringement contentions.

iv. *Apple* factor 4: overlap between issues raised in the petition and in the parallel proceeding

Although Petitioner is also challenging the validity of Claims 1-4, 6, 8, 10-13, 15-20, 22, 25-30 in the Acorn Litigation, that does not favor denying institution here. Instituting would make a stay possible in the Acorn Litigation, reducing the overlap of issues. Further, it is unlikely that the Acorn Litigation will resolve the validity of all 23 challenged claims of the '691 Patent. While Acorn may commit to bringing all 23 challenged claims to trial, the far more likely outcome is that some claims will drop out, leaving the Board as the only tribunal to assess those claims. Finally, to reduce overlap, if the Board institutes, Petitioner will promptly cease asserting Jammy, Goodnick, Taubenblatt 1982, and Chang as prior art references to the challenged claims in the Acorn Litigation. Thus, this factor favors institution.

v. *Apple* factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party

Petitioner and its real parties-in-interest are the defendants in the Acorn Litigation. But, that does not automatically favor denying institution. Rather, the Board principally considers this factor to avoid duplicating another tribunal's work. *Apple*, Case IPR2020-00019, Paper 11, at 13-14. And, as discussed above for factors 1-4, there is minimal risk of that happening here given (1) the Acorn Litigation Court's willingness to grant stays where the Board has instituted trial on the asserted claims; and (2) Petitioner's willingness to cease asserting Jammy, Goodnick,

Taubenblatt 1982, and Chang against the challenged claims in the Acorn Litigation if the Board institutes.

vi. *Apple* factor 6: other circumstances that impact the Board's exercise of discretion, including the merits

This factor favors institution: Petitioner has presented well-supported anticipation and obviousness grounds based on Goodnick, Taubenblatt 1982, Jammy, and Chang. Further, considerations similar to those under 35 U.S.C. § 325(d) are relevant. *Apple*, Case IPR2020-00019, Paper 11, at 16. As discussed above in **Section X.A**, the Office has not cited any of Jammy, Goodnick, Taubenblatt 1982, or Chang against the challenged claims. That favors institution.

* * *

In conclusion, the *Apple* factors favor institution, despite the Acorn Litigation trial date. And regardless, "*NHK Spring* does not suggest, much less hold, that *inter partes* review should be denied under § 314(a) solely because a district court is scheduled to consider the same validity issues before the *inter partes* review would be complete." *Intuitive Surgical, Inc. v. Ethicon LLC*, Case IPR2018-01703, Paper 7, at 13 (PTAB Feb. 19, 2019).

XII. Conclusion

Petitioner respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

Dated: July 10, 2020

Respectfully submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

I hereby certify that this paper, excluding the portions exempted under 37 C.F.R. § 42.24(a), has:

- 13,060 words as counted by Microsoft Word 2016, the word-processing system used to prepare this paper; and

- 770 words in the illustrations, counted manually.

This paper's total word count, excluding the portions exempted under 37 C.F.R. § 42.24(a), is **13,830** words.

Dated: July 10, 2020

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CERTIFICATE OF SERVICE

Under 37 C.F.R. § 42.6(e), the undersigned certifies that on July 10, 2020, a complete copy of the foregoing and all accompanying papers and exhibits were served via Federal Express Priority Overnight shipping, which is at least as fast and reliable as U.S. Priority Mail Express, on counsel of record for Acorn at the correspondence address indicated in PAIR:

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