

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GLOBALFOUNDRIES U.S., INC. and GLOBALFOUNDRIES, INC.,
Petitioners,

v.

OAK IP, LLC,
Patent Owner.

Case No. IPR2025-01129
Patent No. 10,937,880

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,937,880**

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LIST OF EXHIBITS

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1002	File History of U.S. Patent No. 7,084,423
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1004	File History of U.S. Patent No. 6,833,556
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1010	File History of U.S. Patent No. 8,431,469
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1019	U.S. Patent No. 10,388,748
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1042	Exhibit E to Acorn’s Preliminary Infringement Contentions, <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347 (Mar. 9, 2020)
1043	Redacted Acorn’s Opposition to Samsung’s Motion for Judgment, <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347, ECF No. 401 (E.D. Tex. Sept. 2, 2021)
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1092	Trial Transcript, <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347 (E.D. Tex. May 14, 2021)
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1096	Petition, <i>Samsung Electronics Co., Ltd. v. Acorn Semi, LLC</i> , IPR2020-01282, Paper 2 (P.T.A.B. July 13, 2020) (“Goodnick IPR”)
1097	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Acorn Semi, LLC</i> , IPR2020-01282, Paper 56 (P.T.A.B. Feb. 9, 2022) (“Goodnick IPR”)

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1123	Acorn’s Corrected Response Brief, <i>Samsung-Electronics Co. v. Acorn Semi, LLC</i> , No. 2022-1539, Doc. 19 (Fed. Cir. Oct. 11, 2022)
1124	File History of U.S. Patent No. 11,056,569
1125	U.S. Patent No. 11,056,569
1126	File History of U.S. Patent No. 11,018,237
1127	U.S. Patent No. 11,018,237
1128	U.S. Patent No. 5,792,703 (“Bronner”)
1129	U.S. Patent No. 10,090,395 (“the ’395 Patent”)
1130	File History of U.S. Patent No. 10,090,395
1131	Petition, <i>Samsung Electronics Co., Ltd. v. Acorn Semi, LLC</i> , IPR2020-01206, Paper 2 (P.T.A.B. June 29, 2020) (“Grupp’483 IPR”) (“Grupp’483 IPR”)

Exhibit	Description
1132	Decision Granting Institution, <i>Samsung Electronics Co., Ltd. v. Acorn Semi, LLC</i> , IPR2020-01206, Paper 22 (P.T.A.B. Jan. 13, 2021) (“Grupp’483 IPR”)
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1135	Decision Granting Institution, <i>Samsung Electronics Co., Ltd. v. Acorn Semi, LLC</i> , IPR2020-01279, Paper 20 (P.T.A.B. Jan. 13, 2021) (“Goodnick IPR”)
1136	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Acorn Semi, LLC</i> , IPR2020-01279, Paper 55 (P.T.A.B. Jan. 12, 2022) (“Goodnick IPR”)

All citations to specific pages of exhibits follow the pagination added to those exhibits per 37 C.F.R. § 42.63(d)(2)(i).

I. INTRODUCTION

GlobalFoundries U.S., Inc. and GlobalFoundries, Inc. (collectively, “Petitioners” or “GF”) request *inter partes* review of Claims 1-28 (“the Challenged Claims”) of U.S. Patent No. 10,937,880 (Ex.1001, “the ’880 Patent”) assigned to Oak IP, LLC (“PO” or “Oak”) (Ex.1095, ¶20). The ’880 Patent relates to metal-semiconductor junctions with an interface layer between a metal and a semiconductor. (Ex.1001, 1:31-36.) The ’880 Patent claims a priority date of August 12, 2002 through a series of parent applications, the earliest of which issued as U.S. Patent No. 7,084,423. (Ex.1001, Cover, 1:8-28; Ex.1003.) Oak filed a Complaint against Petitioners on February 4, 2025, and this is the first petition challenging the claims of the ’880 Patent.

Claims 1-22 and 28, which require an *oxide of titanium*, are not entitled to the August 2002 priority date because the specification does not provide adequate written description support to the “oxide of titanium” genus. Though the “oxide of titanium” genus purportedly covers any binary or ternary compound containing oxygen and titanium, the specification discloses *only one* example of such a compound: *titanium dioxide (TiO₂)*. The single disclosed species—TiO₂—is not representative of the entire “oxide of titanium” genus and does not describe features common to all members of the claimed genus. Thus, the “oxide of titanium” limitation lacks adequate written description support in the ’880 Patent.

Not all of the ancestor applications of the '880 Patent describe the “oxide of titanium” genus. Indeed, the first time the patentee even arguably described an “oxide of titanium” in an interface layer was in the originally filed claims of U.S. Patent App. No. 15/048,877—which was not filed until February 19, 2016. (Ex.1014, 61.) Thus, claims requiring an “oxide of titanium” cannot possibly obtain a priority date earlier than February 19, 2016, and, U.S. Patent No. 7,176,483 (Ex.1021, “Grupp’483”) qualifies as prior art to Claims 1-22 and 28.

Claims 26-28 of the '880 Patent require a specific contact resistivity of “less than $10\ \Omega\text{-}\mu\text{m}^2$ ” or “less than $1\ \Omega\text{-}\mu\text{m}^2$.” The Board addressed this limitation in an *inter partes* review (IPR2020-01206) challenging claims of U.S. Patent No. 9,905,691 (the '691 Patent). (Ex.1133, 27-39.) The Board ruled that the claims containing this limitation are not entitled to a priority date earlier than the filing date of the '691 Patent because the ancestor applications of the '691 Patent do not enable the breadth of the recited range of “a specific contact resistivity . . . less than $1\ \Omega\text{-}\mu\text{m}^2$.” (*Id.*) The Board concluded that Grupp '483 is prior art for the challenged claims.¹ The '880 Patent is part of the same family as the '691 Patent and the two

¹ In the Acorn Litigation mentioned in **Section VII**, Samsung appealed the decisions to the Federal Circuit noting that Board’s finding of no anticipation for Claims 18 and 26-29 of the '691 Patent was an oversight, (Ex.1122, 48-50), and Acorn

patents have nearly identical specifications. Thus, Claims 26-28 of the '880 Patent are not entitled to a priority date earlier than the filing date of the '880 Patent, and Grupp'483 is prior art for these claims.

Finally, for **Claims 23-25**, U.S. Patent No. 6,724,088 (Ex.1101, "Jammy")—filed on April 20, 1999—qualifies as prior art.

As shown herein and in the declaration of Dr. E. Fred Schubert, Grupp'483 anticipates every Challenged Claim except Claims 23-25, but Jammy alone renders these three claims obvious.

II. MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioners identify the following as the real parties-in-interest: GLOBALFOUNDRIES Inc. and GLOBALFOUNDRIES U.S., Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

1. Judicial Matters

The following judicial matters may affect or be affected by this proceeding:
Oak IP, LLC v. GlobalFoundries U.S., Inc. and GlobalFoundries, Inc., Civil Action No. 25-142 (MN) (D. Del.) ("the Oak Litigation"), in which PO filed a Complaint

concurrent. (Ex.1123, 82.) Like Claims 26-28 of the '880 Patent, Claim 18 and 26-29 of the '691 Patent also recited specific contact resistivity without a lower bound. (Ex.1015.)

alleging that Petitioners and their real parties-in-interest infringe the '880 Patent (Ex.1095, ¶¶1-2). Oak first served the complaint on GlobalFoundries U.S., Inc. on February 18, 2025, (Ex.1095), and GlobalFoundries, Inc., waived service on March 4, 2025. (Ex.1109.)

2. Administrative Matters

Petitioners have filed petitions for *inter partes* review against the following patents related to the '880 Patent: U.S. Patent Nos. 9,905,691 and 10,090,395. Those proceedings may affect or be affected by this proceeding. Further, Oak has asserted those two patents against Petitioners along with the '880 Patent. (Ex.1095 ¶¶1-2.)

C. Lead and Back-Up Counsel:

Lead Counsel	Back-Up Counsel
Scott C. Weidenfeller (Reg. No. 54,531) sweidenfeller@cov.com <u>Postal and Hand-Delivery Address:</u> Covington & Burling LLP One CityCenter, 850 Tenth Street NW Washington, DC 20001 T: (202) 662-5923; F: (202) 778-5923	Anupam Sharma (Reg. No. 55,609) asharma@cov.com <u>Postal and Hand-Delivery Address:</u> Covington & Burling LLP 3000 El Camino Real 5 Palo Alto Square Palo Alto, California 94306 T: (650) 632-4709; F: (650) 632-4809
	Peter P. Chen (Reg. No. 39,631) pchen@cov.com <u>Postal and Hand-Delivery Address:</u> Covington & Burling LLP 3000 El Camino Real 5 Palo Alto Square Palo Alto, California 94306 T: (650) 632-4720; F: (650) 632-4820
	Dr. W. Kiersten Choi (Reg. No. 73,012)

	wchoi@cov.com <u>Postal and Hand-Delivery Address:</u> Covington & Burling LLP One CityCenter, 850 Tenth Street NW Washington, DC 20001 T: (202) 662-5240; F: (202) 778-5240
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Pursuant to 37 C.F.R. § 42.10(b), Petitioners have filed a power of attorney with the above designation of counsel.

D. Service Information:

Please address correspondence to counsel at the address above. Petitioners consent to electronic service to: GF-Oak-IPR@cov.com and the email addresses listed above. Service information is provided in the designation of counsel above.

III. PAYMENT OF FEES

This Petition is accompanied by the fees set forth in 37 C.F.R. § 42.15(a). Please charge or credit Deposit Account No. 60-3160 with any shortage or overpayment of fees associated with this Petition and any other fees incurred by Petitioners.

IV. GROUNDS FOR STANDING

Petitioners certify that the '880 Patent is available for *inter partes* review. Petitioners further certify that neither Petitioners nor any real party-in-interest or privy is estopped or barred from requesting *inter partes* review of the challenged claims on the grounds identified in this Petition.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Petitioners request *inter partes* review and cancellation of Claims 1-28 of the '880 Patent.

A. Identification of Prior Art

1. Grupp'483 (Ex.1021)

As discussed in **Section X**, Claims 1-22 and 26-28 are not entitled to a priority date earlier than February 19, 2016, the filing date of U.S. Patent App. No. 15/048,877 (the "'877 Application"). Thus, U.S. Patent No. 7,176,483 (Ex.1021, "Grupp'483"), issued on February 13, 2007, qualifies as prior art to Claims 1-22 and 26-28 under at least pre-AIA 35 U.S.C. § 102(b).²

2. Jammy (Ex.1101)

U.S. Patent No. 6,724,088 (Ex.1101, "Jammy"), filed on April 20, 1999— qualifies as prior art to Claims 23-25 under at least pre-AIA 35 U.S.C. § 102(e).

B. Statutory Grounds of Unpatentability

Ground 1: Grupp'483 anticipates Claims 1-22 and 26-28 under at least pre-AIA 35 U.S.C. § 102(b) or under AIA 35 U.S.C. § 102(a)(1).

Ground 2: Jammy renders obvious Claims 23-25 under at least pre-AIA 35 U.S.C. § 103(a).

² If Oak argues that the '880 Patent is governed by the AIA, Grupp '483 qualifies as prior art under AIA 35 U.S.C. § 102(a)(1).

VI. OVERVIEW OF PRIOR ART

A. Grupp'483

Grupp'483 is a continuation-in-part of an August 2002 application that issued as U.S. Patent No. 7,084,423. (Ex.1021, Cover, 1:8-19.) The '880 Patent purports to claim priority to that same August 2002 application through a chain of ancestor applications. (Ex.1001, Cover, 1:8-29.) Thus, Grupp'483 and the '880 Patent and its ancestor applications have significantly overlapping disclosures.

Unsurprisingly, Grupp'483 anticipates Claims 1-22 and 26-28. (Ex.1022, ¶¶182-188, 197-200.)

B. Jammy

Jammy discloses incorporating quantum conductive barrier layers between conductive studs and diffusion regions in a transistor to improve reliability. (Ex.1101, Fig. 1, 2:42-53, 3:16-22.) Jammy teaches that its invention can be incorporated in transistors disclosed in other references, such as U.S. Patent No. 5,792,703 ("Bronner") (Ex.1128), and incorporates Bronner by reference. (Ex.1101, 4:1-8.)

Jammy renders obvious Claims 23-25 of the '880 Patent. (Ex.1022, ¶¶189-196, 201-216.)

VII. OVERVIEW OF THE '880 PATENT

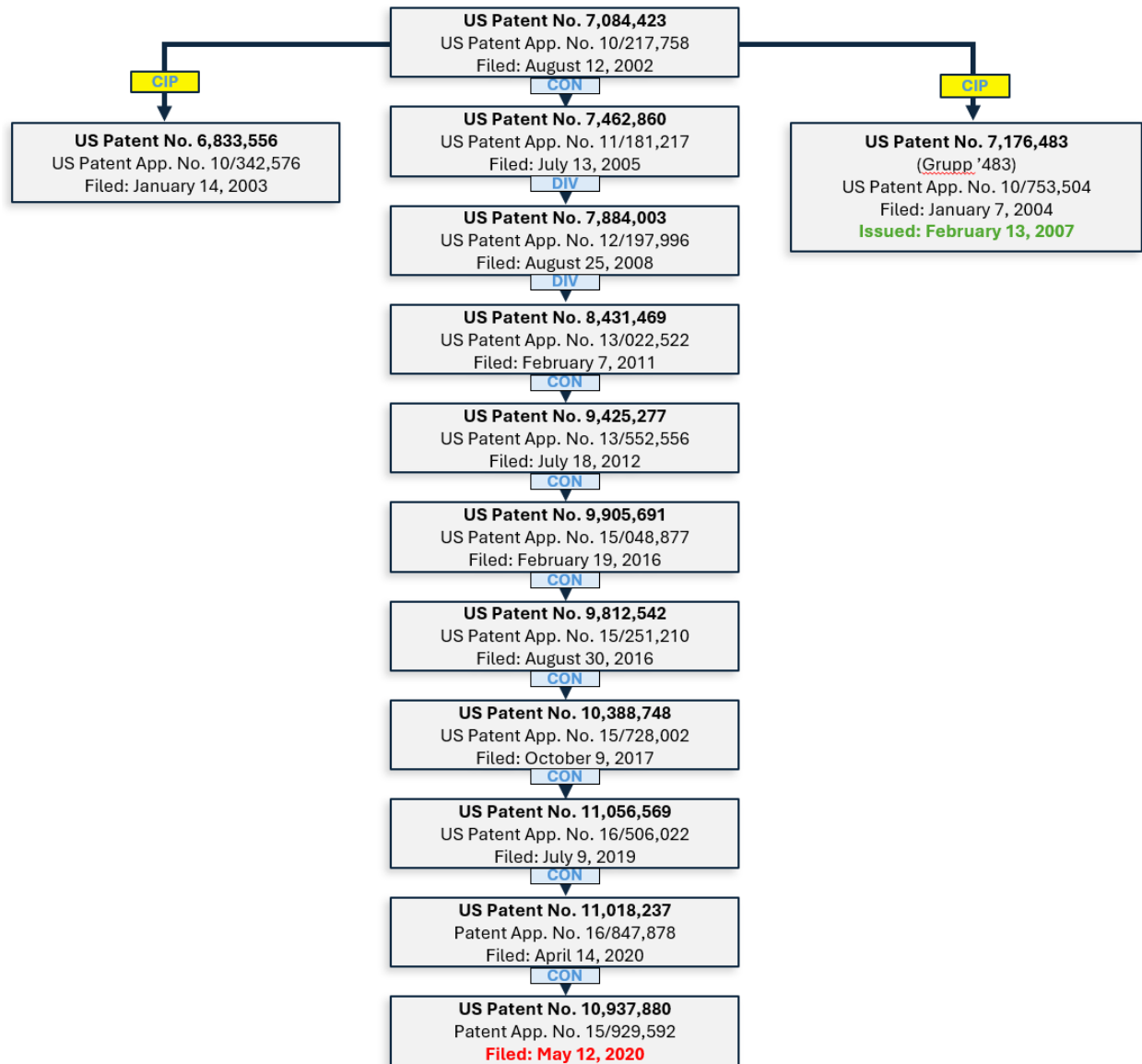
A. Technical Background

Metal-semiconductor junctions are characterized by a barrier to the movement of charge carriers at the interface between the metal and the semiconductor, called a

Schottky barrier. (Ex.1023, 1; Ex.1001, 1:39-40, 1:52-54; Ex.1022, ¶¶38-40.) The height of the Schottky barrier can become fixed at a particular height (i.e., Fermi-level pinning), which impedes the control of electrical properties of the junction. (Ex.1001, 2:10-67, 5:35-38, 7:55-59; Ex.1024, 545-546; Ex.1022, ¶¶41-52.) The '880 Patent provides an interface layer that depins the Fermi level to help control the barrier height and the electrical properties of the junction. (Ex.1001, Figs. 7a and 7d, 16:65-17:1, 17:13-25; Ex.1022, ¶¶53-55.) Even before the earliest alleged priority date the Challenged Claims, techniques for depinning a Fermi level were well-known. (Ex.1022, ¶¶56-68.)

B. Prosecution History

The '880 Patent began as U.S. Patent App. No. 15/292,592 (“the '592 Application,” filed on May 12, 2020. (Ex.1020, 1.) The partial family tree of the '880 Patent is below:



(Ex.1005, Cover; Ex.1020, 59-60; Ex.1021, Cover, 1:8-19.)

The Examiner rejected the pending claims of the '592 Application on the ground of nonstatutory double patenting as being unpatentable over claims of either U.S. Patent No. 9,461,167 (Grupp '167) or Grupp '167 in view of U.S. Patent No. 5,992,960 (Zhang). (Ex.1020, 2459-2471.) In response, the applicant filed a terminal

disclaimer based on U.S. Patent Nos. 9,872,542 and 9,461,167. (Ex.1020, 2540-2548.)

The Examiner allowed the claims on the next action. (*Id.*, 2582-2585, 2650-2653.) But the Examiner’s reasons for allowance did not actually ascribe any specific priority date to the Challenged Claims. (*Id.*) The ’592 Application then issued as the ’880 Patent. (*Id.*, 2695.)

C. Prior Litigation

On October 23, 2019, Acorn filed a Complaint against Samsung Electronics Co., Ltd. et al. (“Samsung”), alleging infringement of six patents that belong to the same family as the ’880 Patent. (Ex.1038) (“the Acorn Litigation”). The parties eventually settled the dispute in January 2023. (Ex.1104.)

VIII. CLAIM CONSTRUCTION

For petitions filed after November 13, 2018, the Board “constru[es] the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b); *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). The Board need only construe claim terms to the extent necessary to resolve a controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

In the Acorn Litigation, the district court issued a *Markman* order on October 16, 2020, construing several terms and the pertinent constructions are listed below:

Term	Claims	Construction
“interface layer”	1-28	Plain and ordinary meaning
“said interface layer comprising an oxide of titanium and an oxide of the semiconductor”	17-28	“said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor region”
“passivating material”	1-28	“material capable of terminating dangling bonds at the surface of the semiconductor”

(Ex.1100, 14, 21, 27-29.)

In the prior *inter partes* reviews for the '691 Patent filed by Samsung, the Board construed the terms “specific contact resistivity” and “specific contact resistance” to be interchangeable. (Ex.1133, 8-9; Ex.1136, 8.)

The '880 patent shares a specification with the patents-at-issue in the Acorn Litigation and, as a result, the constructions are relevant to the claims of the '880 Patent. *In re Rambus Inc.*, 694 F.3d 42, 48 (Fed. Cir. 2012) (“unless otherwise compelled . . . the same claim term in the same patent or related patents carries the same construed meaning” (quoting *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d

1314, 1334 (Fed. Cir. 2003))). The Petitioners have applied the constructions enumerated above. The Board need not expressly construe any term at this stage.³

IX. LEVEL OF ORDINARY SKILL

Any of the following combinations of education and experience would have qualified someone as an ordinarily skilled artisan in the field of the '880 Patent:

- a Ph.D. in electrical engineering, physics, materials science, or chemical engineering, with two years of practical experience with semiconductor research and design;
- a Master's degree in electrical engineering, physics, materials science, or chemical engineering, with four years of practical experience with semiconductor research and design; or
- a Bachelor's degree in electrical engineering, physics, materials science, or chemical engineering, with six to eight years of practical experience with semiconductor research and design.

³ Petitioners reserve all rights to raise claim construction arguments and other arguments in the Oak Litigation or other proceedings. Oak's infringement allegations may raise controversies that require claim construction in that litigation, but not here.

(Ex.1022, ¶¶76-81.) Additional education could make up for less practical experience, and vice versa. (*Id.*) The same level of skill would have been applicable in August 2002, February 2016, or May 2020. (*Id.*, ¶82.) The Board applied the above description in its final written decisions pertaining to patents belonging to the same family as the '880 Patent. (Ex.1091, 9; Ex.1097, 10.)

X. PRIORITY DATE OF THE CHALLENGED CLAIMS

The '880 Patent purports to claim priority to August 12, 2002. (Ex.1001, Cover, 1:8-27; Ex.1003, Cover.) For the Challenged Claims to receive the benefit of the priority of that August 12, 2002 filing date, Oak must show that every application in the priority chain leading to the application that issued as the '880 Patent must support (i.e., both enable and describe) every limitation of the challenged claims under 35 U.S.C. § 112 ¶1. *In re NTP, Inc.*, 654 F.3d 1268, 1277 (Fed. Cir. 2011); *Fiers v. Revel*, 984 F.2d 1164, 1169-70 (Fed. Cir. 1993).

A. Claims 1-22 and 28

Claims 1-22 and 28 have at least one limitation that the parent applications fail to support: *an oxide of titanium*. The specifications and figures in the parent applications are substantively identical to the '880 Patent, including in their incorporation by reference of U.S. Patent No. 6,833,556. (Ex.1005.) Thus, if the limitation lacks support in the specification of the '880 Patent, it also lacks support in the disclosures of the parent applications, and vice versa. (Ex.1002, 5-52;

Ex.1003; Ex.1006, 3-42; Ex.1007; Ex.1008, 8-48; Ex.1009; Ex.1010, 14-51; Ex.1011; Ex.1012, 6-46; Ex.1013; Ex.1014, 12-17, 35-65; Ex.1015; Ex.1016, 12-48; Ex.1017; Ex.1018, 51-87; Ex.1019; Ex.1130, 12-32; Ex.1129; Ex.1124, 62-90; Ex.1125; Ex.1126, 62-91; Ex.1127.)

The only differences among the parent applications and the '880 Patent are their respective abstracts and claims. But, even those abstracts and claims cannot provide the above claims with any priority date earlier than February 19, 2016. In particular, the patentee did not even arguably disclose a generic “oxide of titanium” limitation as part of an “interface layer” until February 19, 2016, in the originally filed claims in the '877 Application. (Ex.1014, 61; Ex.1022, ¶¶86-96.) Thus, the priority date of Challenged Claims requiring an “oxide of titanium” (i.e., Claims 1-22 and 28) is no earlier than February 19, 2016.

B. Claims 26-28

Claims 26 and 28 require a specific contact resistivity “of less than $10\ \Omega\text{-}\mu\text{m}^2$ ” whereas Claim 27 requires a resistivity “of less than $1\ \Omega\text{-}\mu\text{m}^2$.” As to the recited range of “less than $1\ \Omega\text{-}\mu\text{m}^2$ ” that appears in Claims 18 and 25 of the '691 Patent, the Board has found that those claims are not entitled to a priority date earlier than the filing date because the ancestor applications of the '691 Patent do not enable the breadth of the recited range of “a specific contact resistivity between the contact metal and the semiconductor of less than $1\ \Omega\text{-}\mu\text{m}^2$.” (Ex.1133, 27-39.) Likewise, a

specific contact resistivity “of less than $1\ \Omega\text{-}\mu\text{m}^2$ ” required by Claim 27 or a resistivity “of less than $10\ \Omega\text{-}\mu\text{m}^2$ ” required by Claims 26 and 28 are also not enabled by the ancestor applications of the ’880 Patent. Thus, the priority date of Claims 26-28 is not earlier than May 12, 2020.

However, as the Board found in the same IPR (Ex.1133), Grupp’483 enables the upper part of the range for purposes of anticipation, and thus Grupp’483 is prior art for Claims 26-28. (Ex.1133, 38-39.)

C. Claims 23-25

The priority date for the Claims 23-25 can be no earlier than August 12, 2002, which is the filing date of U.S. Patent App. No. 10/217,758. (Ex.1002.)

XI. ’880 PATENT AND ITS PARENT APPLICATIONS DO NOT ADEQUATELY DESCRIBE THE GENUS OF “OXIDE OF TITANIUM”

A. Genus of “oxide of titanium” is extremely broad

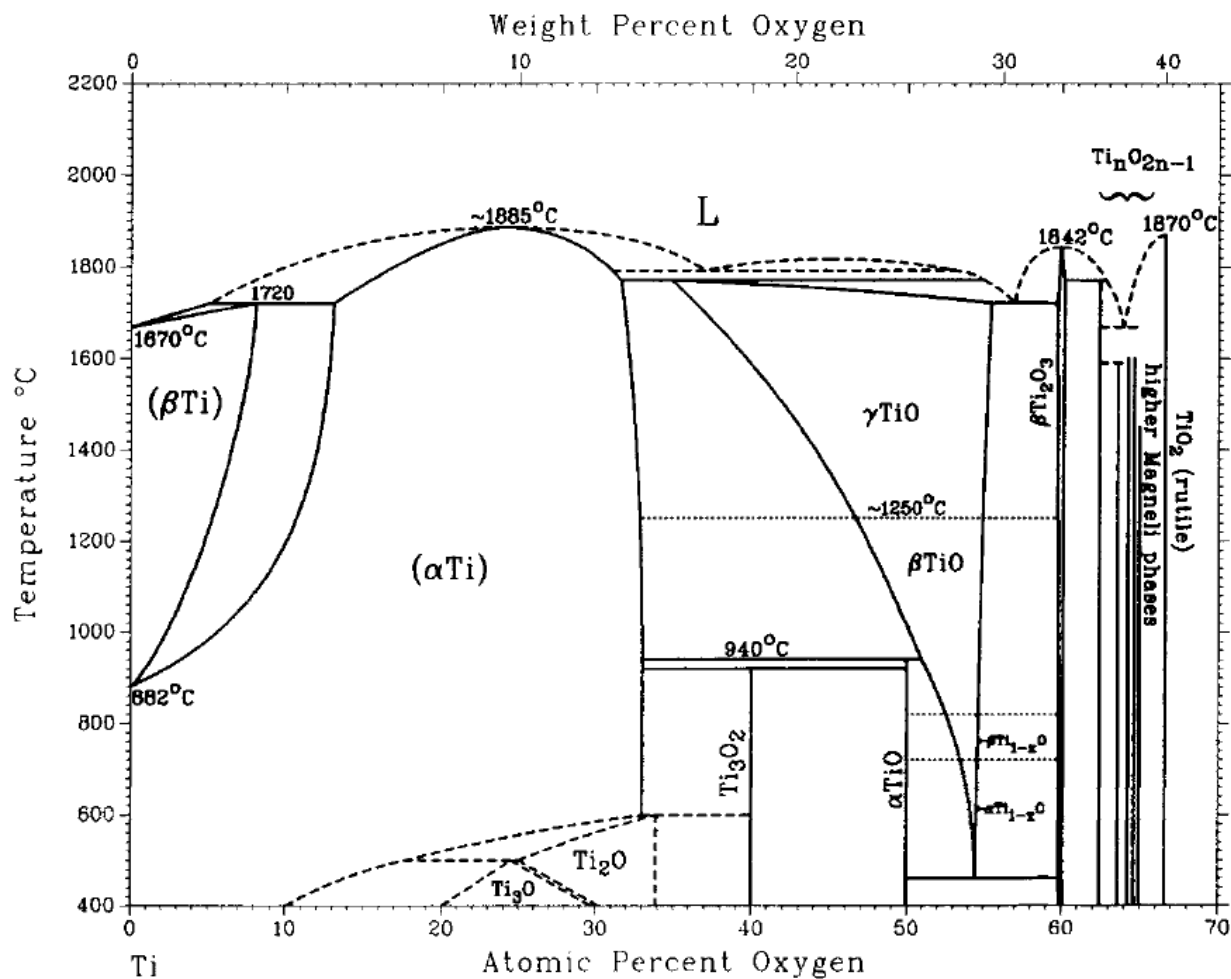
The genus of “oxide of titanium” is broad and is not adequately described by disclosure of a single species, TiO_2 . The genus encompasses (i) numerous binary compounds composed of varying ratios of titanium and oxygen and (ii) numerous ternary compounds composed of titanium, oxygen, and one other element. (Ex.1022, ¶¶97-105.) These binary and ternary compounds have drastically diverse physical, structural, and electrical properties that are vastly different from the properties of TiO_2 . (Ex.1022, ¶¶106-165.) Thus, claims requiring an “oxide of titanium” *cannot* obtain a priority date earlier than February 19, 2016 because the specification fails

to provide adequate written description support to the entire genus. *See In re NTP*, 654 F.3d at 1276-77. (Ex.1022, ¶¶182-184.)

1. Genus of “oxide of titanium” includes numerous binary compounds composed of oxygen and titanium

Like generic metal oxides, there are numerous oxides of titanium, yet the Priority Applications disclose only *one*.⁴ TiO₂. (Ex.1001, 18:6-8; Ex.1022, ¶¶86-96.) As shown below, some (but not all) titanium oxide species include TiO, Ti₂O, Ti₃O, TiO₂, Ti₂O₃, Ti₃O₅, and Ti₄O₇, among others. (Ex.1022, ¶¶97-98.)

⁴ Indeed, when deposed during the earlier IPR proceedings, Acorn’s expert could not even identify all of the titanium oxide species. (Ex.1048, 114:10-18.)



(Ex.1056, Figure 1; Ex.1022, ¶98.)

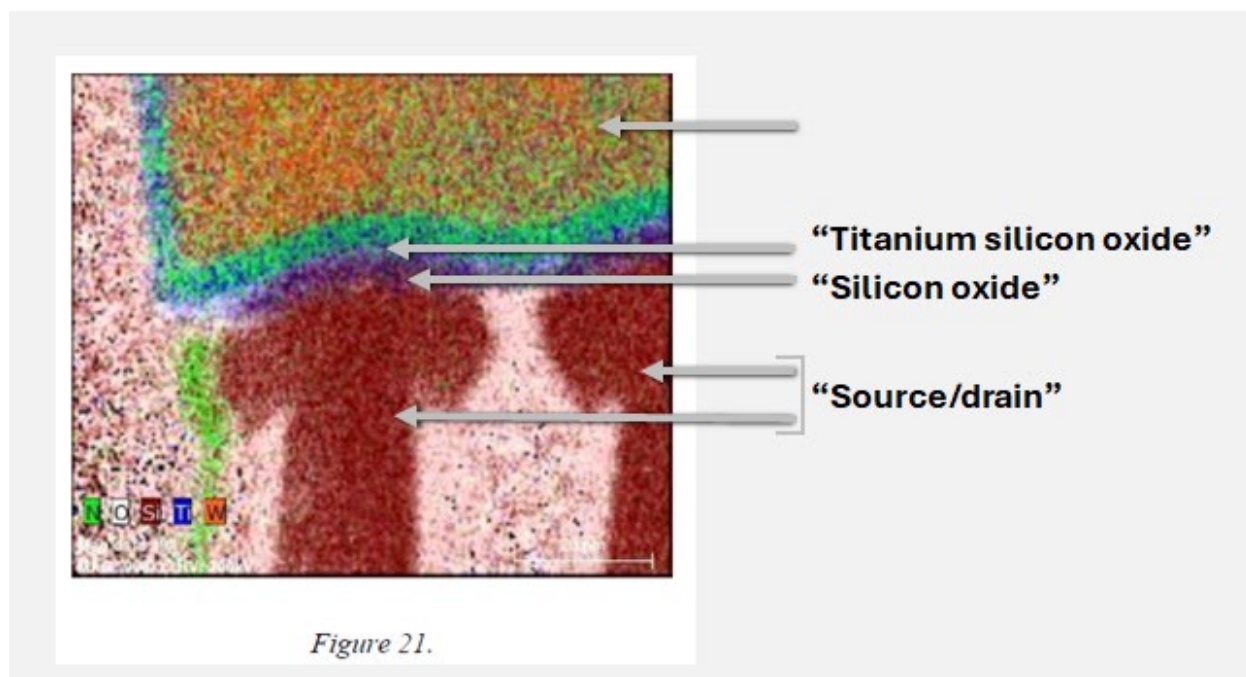
Moreover, in the semiconductor industry, titanium oxides are not limited to the equilibrium compounds discussed above; they can also include non-equilibrium compounds. (Ex.1048, 50:25-51:13; Ex.1022, ¶99.) In other words, a large number of different types of oxide of titanium species can be used in semiconductor devices. (Ex.1022, ¶99.)

2. Genus of “oxide of titanium” includes numerous ternary compounds composed of oxygen, titanium, and another element

Ternary compounds include titanium, oxygen, and another element. (Ex.1022, ¶¶100-101.) There may be at least ten to twenty such compounds with different characteristics making them suitable for multiple applications. (*Id.*) (listing ternary compounds comprising titanium, oxygen and one of the following: nitrogen, carbon, germanium, chromium, strontium, aluminum, barium, magnesium, calcium, and lithium.)

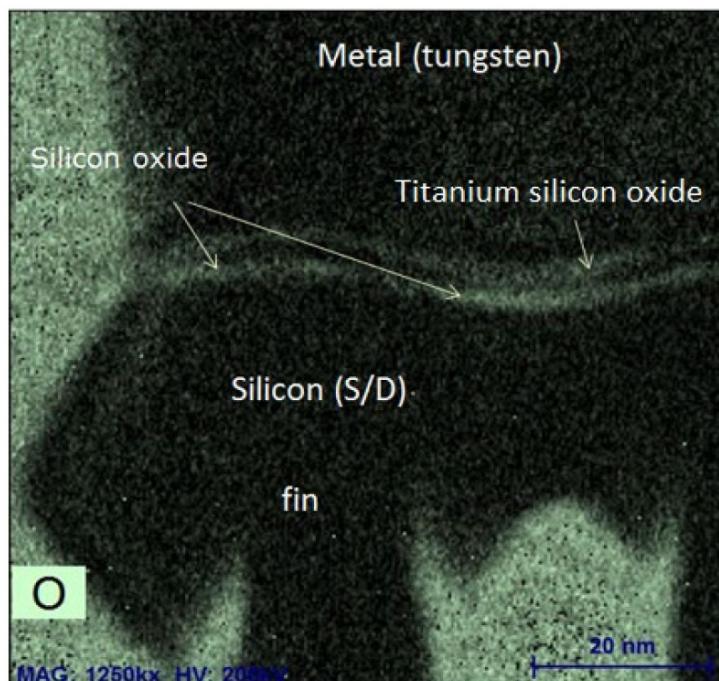
a) Oak argues that “oxide of titanium” includes ternary compounds composed of oxygen, titanium, and silicon

In the Oak Litigation, Oak contends that the genus of “oxide of titanium” includes “titanium silicon oxide.” (Ex.1095, ¶¶52-54, 68, 78) In the Complaint, with respect to the “interface layer” limitation of Claim 1 of the ’880 Patent that requires an *oxide of titanium*, Oak alleges that each product of the Petitioners “comprise[s] an *interface layer* of *titanium silicon oxide* and silicon oxide.” (*Id.* ¶76.) Specifically, Oak alleges that in “the microscopic image . . . of a chip” fabricated by the Petitioners, “the *titanium silicon oxide* and silicon oxide interface layer can be seen in purple and pink (or maroon-white) between the tungsten and titanium nitride metal contact and the silicon semiconductor source/drain.” (*Id.*)



(Ex.1095, 31, Fig. 21 (annotated).) Thus, Oak asserts that “oxide of titanium” genus is not limited to binary compounds but also includes ternary compounds that include titanium, silicon, and oxygen.

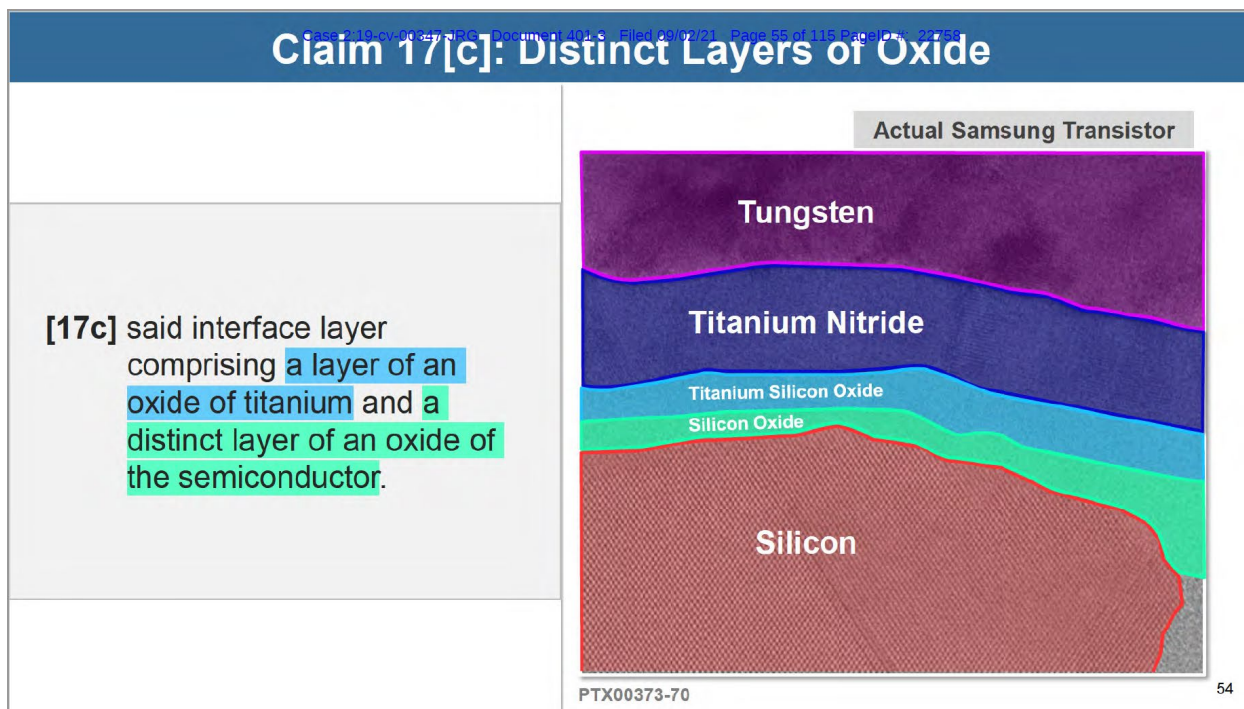
Likewise, in the Acorn Litigation, Acorn expressly interpreted the genus of “oxide of titanium” to encompass ternary compounds. Referring to the image below, Acorn argued that the accused products infringe Claim 17 of the U.S. Patent No. 10,090,395 (“the ’395 Patent”) (Ex.1129), because “the accused interface layer includes sublayers of *titanium silicon oxide, which comprises an oxide of titanium,* and silicon oxide, which is an oxide of silicon.” (Ex.1042, 25.)



Samsung 14nm LPE - Exynos 7420 (Galaxy S6)

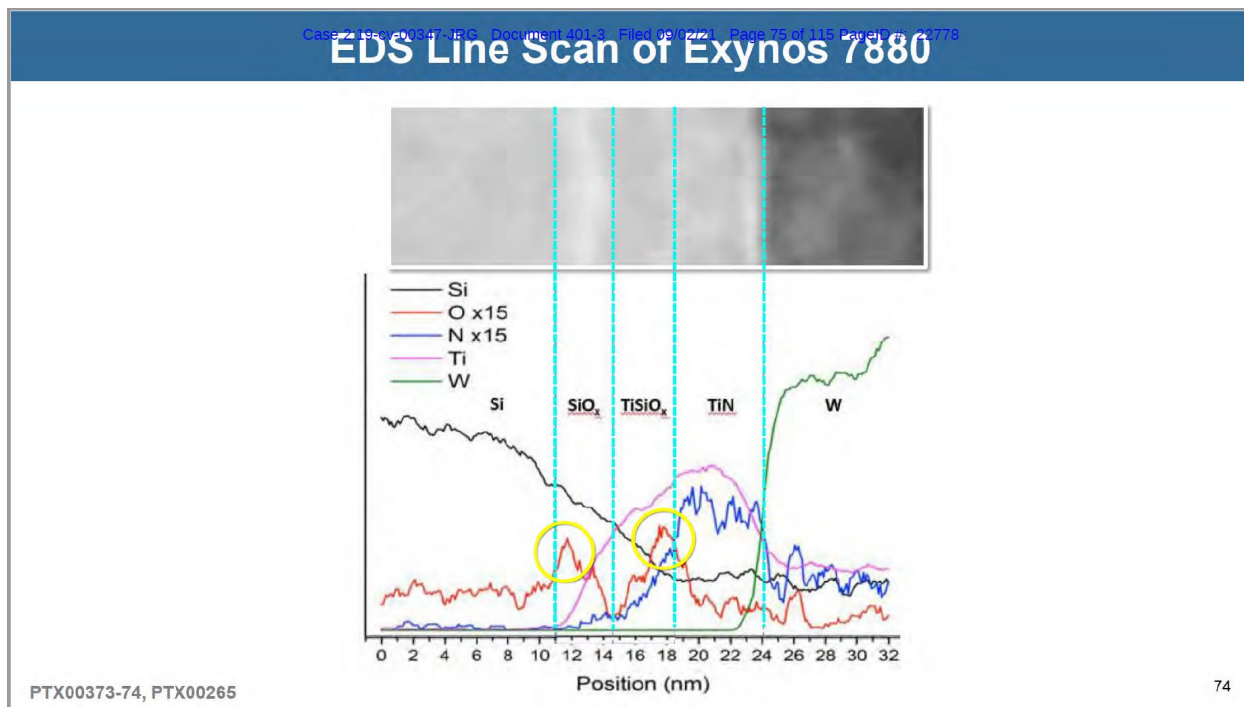
(Ex.1042, 23-24.) Like Claim 1 of the '880 Patent, Claim 17 of the '395 Patent requires an “oxide of titanium.” (Ex.1001, 18:44-51, Ex.1129, 19:31-40.).

At trial in the Acorn Litigation, Acorn argued that the “oxide of titanium” genus includes ternary compounds that contain silicon, oxygen and titanium. Using the demonstrative below, Acorn’s expert, Dr. Piner testified that the “layer of an oxide of titanium” present in Limitation [c] of Claim 17 corresponds to the “Titanium Silicon Oxide” layer in the accused products:



(Ex.1044, 55.) Dr. Piner testified the term “a layer of an oxide of titanium” corresponds to the layer of “Titanium Silicon Oxide” in blue in the demonstrative above. (Ex.1092, 476-77.)

Acorn’s expert, Dr. Piner, did not limit the scope to a particular composition of titanium silicon oxide. Through the slide below, Dr. Piner equated “oxide of titanium” to *TiSiO_x*, a compound in which the amount of oxygen can be arbitrary:



(Ex.1044, 75.) Acorn argued to the jury that the “oxide of titanium” includes all compounds of titanium, silicon, and oxygen irrespective of the amount of oxygen content. (Ex.1043, 23.) Acorn also argued that a compound containing “more than mere trace amounts” of oxygen, and as little as 5% or 15%, meets the “oxide of titanium” limitation. (*Id.*) During post-trial phase, while relying upon the above demonstrative, (Ex.1044, 75), Acorn did not limit ***TiSiO_x*** to a particular level of oxygen; instead it asserted that “Dr. Piner had identified the layer of silicon oxide and a ***layer of titanium silicon oxide.***” (Ex.1043, 5).

The jury found that Samsung infringes Claim 17 of the '395 Patent. (Ex.1045, 4; Ex.1129, 19:31-40.) The District Court entered a final judgment shortly thereafter noting, *inter alia*, that Samsung infringed Claim 17 of the '395 Patent. (Ex.1093, 2.)

b) Oak is estopped from arguing that ternary compounds containing titanium, silicon, and oxygen do not fall within the ambit of “oxide of titanium”

Acorn’s statements during the Acorn Litigation regarding the “oxide of titanium” genus, the doctrine of judicial estoppel now estops Oak from arguing a narrower scope of that genus. As the present assignee of the ’880 Patent, Oak is bound by the acts of Acorn, the previous assignee of that patent. *See Worely v Tobacco Co.*, 104 U.S. 340, 344 (1881) (“[T]he assignee of a patent right takes it subject to the legal consequences of the previous acts of the patentee.”); *In re Galaz*, 841 F.3d 316, 326 (5th Cir. 2016); *Adelphia Recovery Tr. v. Goldman, Sachs & Co.*, 748 F.3d 110, 120 (2d Cir. 2014); *see also Int’l Nutrition Co. v. Horphag Rsch., Ltd.*, 220 F.3d 1325, 1329 (Fed. Cir. 2000).

The doctrine of judicial estoppel prevents a party who relied on one argument to prevail in a legal proceeding from advancing a contradictory argument in another proceeding. *See New Hampshire v. Maine*, 532 U.S. 742, 749 (2001). The doctrine’s purpose is “to protect the integrity of the judicial process by prohibiting parties from deliberately changing positions according to the exigencies of the moment[.]” *Id.* at 749–50 (quotations and citations omitted). To determine whether judicial estoppel should apply, the Federal Circuit considers three non-exclusive factors. *Trs. in Bankr. of N. Am. Rubber Thread Co. v. United States*, 593 F.3d 1346, 1354 (Fed. Cir. 2010) (citing *New Hampshire*, 532 U.S. at 749 and enumerating three factors).

Because all three judicial estoppel factors are present, Oak should be estopped from arguing for a different scope of the “oxide of titanium” genus than Acorn obtained in the litigation against Samsung. *First*, any argument from Oak that the “oxide of titanium” genus does not include TiSiO_x would contradict Acorn’s earlier position that the “oxide of titanium” genus does include TiSiO_x . *Second*, Acorn prevailed in the infringement trial based on the interpretation that the “oxide of titanium” genus includes TiSiO_x . *Third*, Oak would derive an unfair advantage if it were permitted to advocate for inconsistent constructions of its patent claims. Thus, Oak should be precluded from asserting that the “oxide of titanium” genus does not include ternary compounds, such as TiSiO_x . *See Trs. in Bankr.*, 593 F.3d at 1356; *see also Trs. of Columbia Univ. v. NortonLifeLock, Inc.*, 2019 WL 7040931, at *3-6 (E.D. Va. Dec. 20, 2019).

B. Ancestor applications of the ’880 Patent fail to adequately describe an interface layer that comprises an “oxide of titanium”

Claims 1-22 and 28 cannot obtain their alleged August 12, 2002 priority date unless all of the ’880 Patent’s ancestor applications provide written description support for every limitation of these claims. *In re NTP*, 654 F.3d at 1277. “[T]he test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc); *see also Juno Therapeutics, Inc. v. Kite*

Pharma, Inc., 10 F.4th 1330, 1336 (Fed. Cir. 2021). Thus, “[a] disclosure in a parent application that merely renders the later-claimed invention obvious is not sufficient to meet the written description requirement; the disclosure must describe the claimed invention with all its limitations.” *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998).

To support a claim to a genus, the specification must disclose “either a representative number of species falling within the scope of the genus or structural features common to the members of the genus so that one of skill in the art can ‘visualize or recognize’ the members of the genus.” *Ariad*, 598 F.3d at 1350 (citation omitted); *see also Juno*, 10 F.4th at 1336. Here, Claims 1-22 and 28 require a “spacer layer that is *an oxide of titanium*.” (Ex.1001, Claims 1-22 and 28.) The only possible example of an “oxide of titanium” for a spacer layer described in any earlier parent application is a ***TiO₂ spacer layer***. (Ex.1001, 18:6-8; Ex.1022, ¶91.)⁵ Thus, the

⁵ The Board has found that although incorporated-by-reference U.S. Patent No. 6,833,556 describes a generic metal oxide and four example metal oxides, those metal oxides are only used to electrically isolate a transistor’s gate from its channel “such that essentially no current flows between the gate 270 and the channel 220”—not for an interface layer through which current does flow, as is claimed. Moreover, none of the examples disclosed (zinc oxide, aluminum oxide, zirconium oxide, and

relevant question is whether the statement in earlier parent applications that “[s]pacer layers may be used with lower barriers (e.g., TiO₂ has a barrier of less than 1 eV)” provides written description of the entire “oxide of titanium” genus. (Ex.1001, 18:6-8.) And the answer is no, as further explained below:

First, although Claims 1-22 and 28 purport to cover any “oxide of titanium,” the Priority Applications provide a **single** example: titanium dioxide (TiO₂). “[A] patentee will not be deemed to have invented species sufficient to constitute the genus by virtue of having disclosed a single species.” *In re Curtis*, 354 F.3d 1347, 1358 (Fed. Cir. 2004); *see also Juno*, 10 F.4th at 1336.

Second, the single disclosed species—TiO₂—is not representative of the entire genus of “oxide of titanium,” and the specification does not describe features common to all members of the claimed genus. (Ex.1022, ¶¶95-96.) There are numerous materials that fall within the “oxide of titanium” genus, including several binary and ternary compounds as discussed above, and these materials exhibit a very broad range of properties, including dielectric (i.e., insulators), metallic and semiconductive compounds. (Ex.1022, ¶¶97-101, 106-160.)

hafnium oxide) is an oxide of titanium. (Ex.1091, 18; Ex.1005, 7:60-8:22; *see also id.*, 13:44-14:20; Ex.1001, 14:58-65; Ex.1022, ¶94.)

There are many different properties that affect the characteristics of the compounds within the “oxide of titanium” genus and the applications for which those compounds may be employed. (*Id.*) Some of the non-limiting exemplary properties of the species of the genus include: (a) electrical (tunneling and bulk) conductivity (*or* resistivity); (b) barrier height; (c) electron affinity; (d) bandgap energy; (e) dielectric constants; (f) structural characteristics; (g) melting point; and (h) optical transparency. (Ex.1022, ¶107.) As discussed below, none of these properties exhibit a characteristic that is common to all the species in the “oxide of titanium” genus.

1. Electrical conductivity (or resistivity)

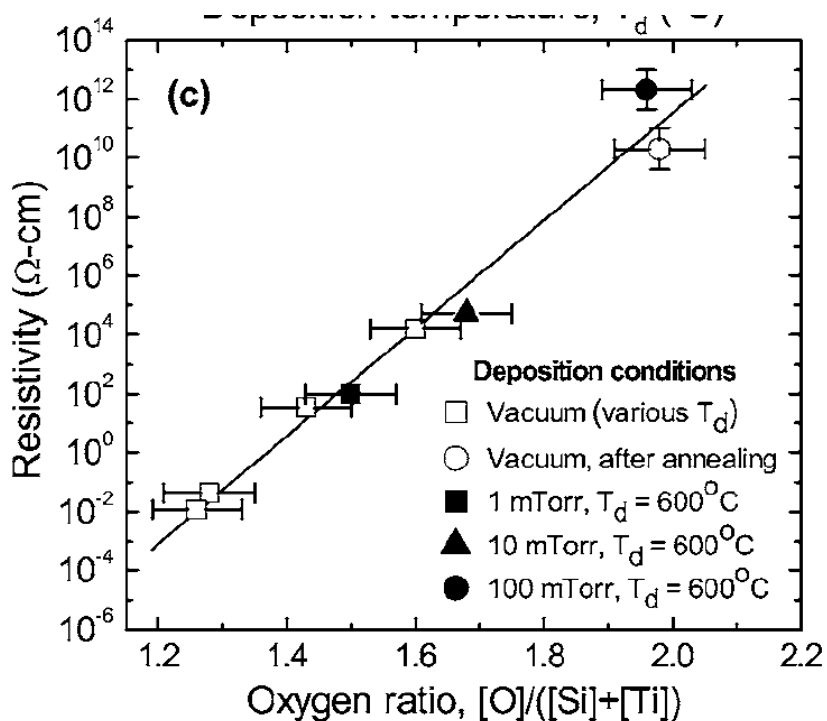
The electrical conductivity (or resistivity)⁶ of an “oxide of titanium” as used in an interface layer in a metal-semiconductor junction directly affects the specific contact resistivity of the junction. (Ex.1022, ¶¶109-110.) The Board also recognized for the ’395 Patent that “[t]he electrical conductivity of a metal oxide is an important property for the recited genus because electrical conductivity directly affects the specific contact resistance of a junction.” (Ex.1133, 20 n.3.) Because the ’395 and ’880 Patents share the specification, the electrical conductivity of an oxide of

⁶ Electrical conductivity is the reciprocal of electrical resistivity. (Ex.1022, ¶111.)

titanium is an important property for the purported invention of the '880 Patent as well.

That TiO_2 is insufficient to represent the full scope of the claimed genus is evident when only a ***single*** property—electrical conductivity—is compared between different species of oxides of titanium. TiO_2 (titanium dioxide) is an oxide of titanium with ***semi-conductive*** properties (which may vary depending on the impurity content). (Ex.1022, ¶113.) Mirroring the semi-conductive property, the electrical resistivity (ρ) of TiO_2 ranges from 1×10^4 to $1 \times 10^7 \Omega \text{ m}$. (Ex.1078, 88; Ex.1022, ¶113.)

Based upon their ***composition***, the conductivity of compounds within the “oxide of titanium” genus varies considerably and ranges from ***conductors*** at one end to ***insulators/dielectrics*** at the other end. (Ex.1022, ¶113.) For example, the conductivity of oxides of titanium composed of titanium, silicon, and oxygen (i.e., TiSi_xO_y) varies widely depending on the level of oxygen of the compound. (*Id.*, ¶114.) Fig. 6(c) of 2005-Brassard shows that titanium silicates (TiSi_xO_y) with high levels of oxygen content are insulators whereas titanium silicates with low levels of oxygen are conductors:



(Ex.1035, 054912-6, Fig. 6(c).) When oxygen and titanium are present in equal proportion (e.g., TiO), the compound acts like a **conductor** or has metallic properties. However, when oxygen content is high (e.g., 60% or more as in TiSiO_4) the compound acts like an **insulator**. (Ex.1022, ¶¶115-118.)

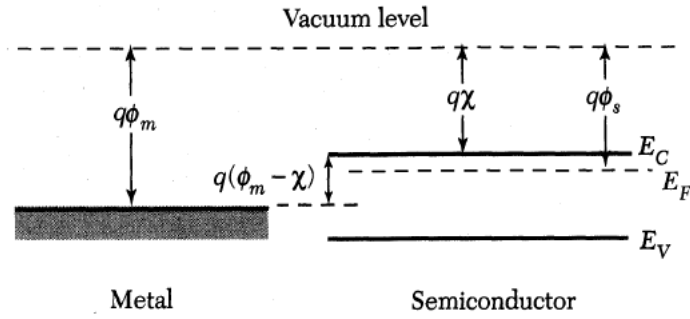
In addition to **composition**, the electrical conductivity of compounds in the “oxide of titanium” genus varies significantly based on **environmental conditions**, such as temperature (*Id.*, ¶119.) For example, Ti_3O_5 behaves like a semiconductor at room temperature, but becomes conductive at higher temperatures. (*Id.*) The conductivity of oxides of titanium also varies based on their **growth or film deposition conditions**, such as oxygen pressure and deposition temperature. (*Id.*, ¶¶120-122.) For example, the conductivity is low when the films are deposited at

low oxygen pressure, but when oxygen pressure is increased, the resistivity increases rapidly and highly insulating films are obtained. (*Id.*, ¶121.) The resistivity of titanium silicate films deposited under vacuum decreases when the deposition temperature is increased. (*Id.*, ¶122.)

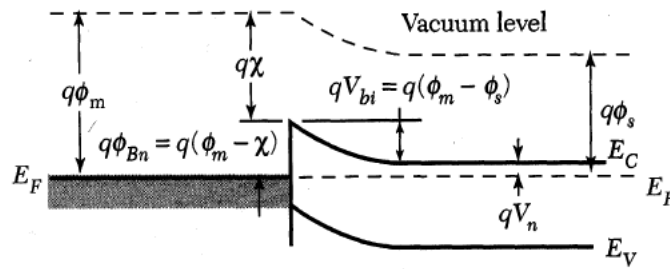
In light of the broad range of variation in the conductivity within the “oxide of titanium” genus, the disclosure of “TiO₂” with “a barrier less than 1 eV” alone does not convey to a POSITA the entire “oxide of titanium” genus. (*Id.*, ¶123.)

2. Barrier height

In a metal-semiconductor junction, the barrier height represents the energy an electron needs to overcome to move from the semiconductor to the metal or vice versa. Thus, barrier height influences the electrical characteristics of the junction, and impacts the specific contact resistivity. (Ex.1107, 72-74; Ex.1022, ¶124.) Fig. 2(a) from the Sze Textbook (excerpted below) is the energy band diagram of an isolated metal adjacent to an isolated n-type semiconductor and Fig. 2(b) is a diagram for a metal-semiconductor junction:



(a)



(b)

(Ex.1107, Figs. 2(a), 2(b), and 226.) The concept of barrier height is related to work function and electron affinity, and as shown in Fig. 2(b), barrier height ($q\phi_{Bn}$) of a metal-semiconductor junction is the difference between the metal's work function and the semiconductor's electron affinity:

$$q\phi_{Bn} = q\phi_m - q\chi$$

(Ex.1107, 226). The electron affinity $q\chi$ is the energy difference between the conduction band edge E_c and the vacuum level in the semiconductor (i.e., level at which an electron has no potential energy). (*Id.*) The work function $q\phi_s$ is the energy difference between the Fermi level E_F and the vacuum level in the semiconductor. (*Id.*) The work function of a metal $q\phi_m$ is an inherent property of the metal and does not vary. Thus, the barrier height varies along with the electron affinity $q\chi$. (Ex.1022,

¶124.) The choice of metal and the semiconductor to form the junction influences barrier height, which in turn influences the specific contact resistance. (*Id.*)

Species within the “oxide of titanium” genus can have a broad range of barrier heights. Some species can exhibit a barrier height that is equal to or higher than 1 eV. (*Id.*, ¶¶126-128.) For example, the barrier heights of some species of titanium aluminates relative to silicon conduction band (or the aluminum Fermi level) are higher than or equal to 1 eV and not less than 1 eV in some instances. (*Id.*) Further, metallic compounds, such as TiO (and likely Ti₃O and Ti₂O), do not have a barrier height because they behave like metals.⁷ (*Id.*, ¶129.) Accordingly, the species of the oxide of titanium genus cannot be characterized as fitting the description of having “a barrier of less than 1 eV.” (*Id.*, ¶¶125, 130.) The limited disclosure in the specification of the ’880 Patent does not convey the entire genus to a POSITA. (*Id.*)

⁷ When a dielectric is deposited on a semiconductor, a barrier forms at the semiconductor-dielectric interface. For Si and TiO₂, the ’880 Patent discloses a barrier of less than 1 eV. Such a barrier is absent when TiO₂ (a semiconductor / dielectric) is replaced by TiO (a metallic compound). Instead, metal-semiconductor junctions have a Schottky barrier. (Ex.1022, ¶129, n. 6.)

3. Electron affinity

In a metal-semiconductor junction, electron affinity $q\chi$ is the energy required to move an electron from the semiconductor's conduction band to the vacuum level. (Ex.1022, ¶131.) Electron affinity, along with the work function of a metal $q\phi_m$, determines the barrier height of the junction and the resistance of the junction. (*Id.*; *see also id.*, ¶¶132-133.)

The electron affinity of TiO_2 (a semiconductor) is 4.0 eV. (Ex.1087, 3; Ex.1022, ¶135.) Different compounds in the “oxide of titanium” genus have different electron affinities. (*Id.*, ¶134.) If, in terms of electrical conductivity, a compound in the “oxide of titanium” genus behaves like a metal (e.g., TiO), then its properties are more appropriately described by a metal work function. (*Id.*, ¶135) Further, electron affinities of some of the oxides of titanium (e.g., Ti_2O_3 and TiSiO_4) are not even known. (*Id.*) Thus, the electron affinity of TiO_2 does not convey the entire genus to a POSITA. (Ex.1022, ¶136.)

4. Bandgap energy

The bandgap energy E_g is the gap between the bottom of the conduction band and top of the valence band ($E_c - E_v$), as shown below in Fig. 15. (Ex.1107, 29; Ex.1022, ¶137.)

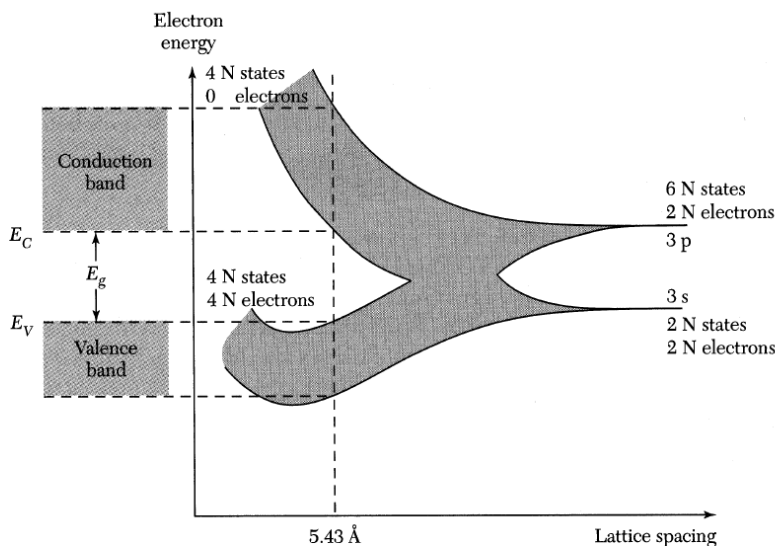


Fig. 15 Formation of energy bands as a diamond lattice crystal is formed by bringing isolated silicon atoms together.

(Ex.1107, 30.) E_g is the energy required to break a bond in the semiconductor to free an electron to the conduction band and leave a hole in the valence band. (*Id.*; Ex.1022, ¶137.) Higher bandgap energy E_g implies higher resistivity and smaller bandgap implies lower resistivity. Thus, the bandgap energy is a key factor in determining a material's electrical conductivity—a material's conductivity is inversely related to its bandgap energy. (*Id.*; see also *id.*, ¶¶138-140.)

The bandgap energy of TiO_2 is about 3.0 to 3.4 eV. (Ex.1074; Ex.1058; Ex.1022, ¶141.) Compounds in the “oxide of titanium” genus have different bandgap energies. (*Id.*) For example, TiO does not have a bandgap energy because it behaves like a metal, and the bandgap energies of Ti_2O_3 and TiSiO_4 are 0.1 eV and 1.75-2.68 eV, respectively. (*Id.*) Thus, the bandgap energy of TiO_2 does not convey the entire genus to a POSITA. (*Id.*, ¶142.)

5. Dielectric constant

The dielectric constant of a material is the ratio of the electrical permittivity of the material to the permittivity of vacuum. Permittivity of a material is its ability to store electrical energy in an electrical field. The dielectric constants are used to describe characteristics of insulators and thus determine the applications for which the insulators can be employed. (*Id.*, ¶143; *see also id.*, ¶144.)

TiO₂ is known to have a high dielectric constant with *k* values in excess of 80. (*Id.*, ¶145.) The dielectric constant also varies widely between different species in the “oxide of titanium” genus when compared to the dielectric constant of TiO₂. (*Id.*) For example, the dielectric constant of TiSiO₄, Ti_{0.5}Si_{0.5}O₂, and Ti_{0.51}Si_{0.49}O₂ is around “16.5,” “higher than 20,” and “as high as 26,” respectively. (*Id.*) Thus, the dielectric constant of TiO₂ fails to convey the entire genus to a POSITA. (*Id.*, ¶146.) Metallic compounds are commonly not characterized in terms of a “dielectric constant” because they are not dielectrics.

6. Structural properties

Structural properties of a compound affect the movement of charge carriers within the material. (Ex.1022, ¶¶147-149.) The compounds in the “oxide of titanium” genus have different structural properties and no one structural property is common to all compounds in that genus. (*Id.*, ¶¶150-152.)

7. Melting point

The melting point of TiO_2 is $1,855^\circ\text{C}$. (*Id.*, ¶153) The melting point of different species of the genus varies widely and the melting point of TiO_2 does not convey the entire genus to a POSITA. (Ex.1022, ¶¶153-155.)

8. Optical transparency

The species of the genus can have a wide variety of optical transparencies and, the optical transparency of TiO_2 does not describe the entire genus to a POSITA. (Ex.1022, ¶¶156-159.)

* * *

The table below compares a handful of binary and ternary compounds of oxides of titanium that could be used in semiconductor devices to illustrate their disparate nature:⁸

Properties	TiO	TiO ₂	Ti ₂ O ₃	Ti ₃ O ₅	TiSiO ₄
Electrical conductivity	Conductor	SemiC	SemiC at RoomT exhibiting SemiC-to-M at higher temp.	SemiC at RoomT exhibiting SemiC-to-M at higher temp.	Insulator

⁸ SemiC refers to semiconductor; RoomT refers to room temperature; SC-to-M refers to transition from semiconductor properties to metal properties. The blank entries in the table indicate that data is not available.

Properties	TiO	TiO ₂	Ti ₂ O ₃	Ti ₃ O ₅	TiSiO ₄
Electron affinity	None	4 eV	Probably unknown	Probably unknown, but relatively small	Probably unknown
Bandgap energy	None (metallic)	3.0-3.4 eV	0.1 eV	Small bandgap with semiconductor-to-metal transition at 440 K	1.75-2.68 eV
Dielectric constant		80			16.5
Structural properties	Monoclinic and cubic	Rutile, anatase and brookite	Corundum	Anosovite and monoclinic	Glass-like (no structure)
Melting point	1,700 °C	1,855 °C	2,130 °C	1,700 °C	
Optical transparency	Reflective (similar to a metal)	Transparent (high)	Optically absorbing and opaque (“dark violet”)	Optically absorbing and opaque (black colored)	Partially transparent

(Ex.1022, ¶160.)

The table above does not even consider all the equilibrium and non-equilibrium species⁹ of the binary and the ternary species of genus that collectively exhibit even broader disparities in the characteristics. (Ex.1022, ¶¶97-101.) Further, properties of some of the species of “oxide of titanium”—such as TiO₂ and non-stoichiometric compounds—were not entirely well understood. (*Id.*, ¶¶161-165.)

The variations show that neither TiO₂ nor “lower barriers” represents the full genus of oxides of titanium. (Ex.1022, ¶¶86-165.) Those disclosures, whether taken alone or together, do not reflect the full variation across the genus of oxide of titanium. (*Id.*) Thus, no application prior to the ’877 Application provides written description of a generic “oxide of titanium” interface layer. (*Id.*)

Indeed, “[a] patentee will not be deemed to have invented species sufficient to constitute the genus by virtue of having disclosed a single species when, as is the case here, the evidence indicates ordinary artisans could not predict the operability in the invention of any species other than the one disclosed.” *In re Curtis*, 354 F.3d

⁹ In the semiconductor fabrication process, nonequilibrium compounds can form because the products are fabricated in nonequilibrium conditions. (Ex.1022, ¶99; Ex.1048, 50:25-51:13.) Acorn argued in the Acorn Litigation that the oxide of titanium includes nonequilibrium compounds. (Ex.1043, 5 (identifying “TiSiO_x” in the interface layer).)

1347, 1358 (Fed. Cir. 2004). The Federal Circuit held *In re Curtis* that a lone disclosed example of a dental floss could not support a claim to a genus of friction-enhancing coatings. (*See id.* at 1358; *see also Juno*, 10 F.4th at 1336.)

Like the lone example in *In re Curtis*, TiO₂ is the only “oxide of titanium” layer disclosed in the parent applications predating the ’877 Application. Acorn alleged that the operability of the claimed interface layers was unpredictable; indeed, it alleged that using *any* interface layer was “counter[-]intuitive.” (Ex.1038 ¶¶6, 48; Ex.1022, ¶95.) Oak also alleges that the inventors found this result “remarkable.” (Ex.1095, ¶¶37-39.) Thus, just as the lone example of MCW in *In re Curtis* could not support a claim to the genus of friction-enhancing coatings, the previous parent applications’ lone example of TiO₂ as a spacer layer cannot support claims to a generic “oxide of titanium” for a spacer layer. Accordingly, no Challenged Claims requiring an “oxide of titanium” can possibly obtain a priority date earlier than February 19, 2016, the filing date of the ’877 Application. (Ex.1022, ¶¶84, 86-96.)

In light of the arguments made by Acorn during the earlier filed petitions, Oak may argue that the disclosure of TiO₂ is sufficient to support the “oxide of titanium” genus. (Ex.1091, 17.) Oak may argue that because the oxide of titanium is in the spacer layer, a common structural feature of oxides of titanium used for such purpose is that they are dielectrics. (*Id.*) The Board should reject Oak’s arguments for the same reason it rejected Acorn’s arguments. The Board noted that “[t]he ’423 patent

[parent of '880 Patent with same specification] does not discuss any properties of metal oxides (other than the lower barrier of the metal oxide TiO_2) or design considerations concerning the selection of particular oxides to use in the claimed structure, particularly in the context of MIGS separation.” (*Id.*, 24.) Thus, the Board did not credit Acorn’s analysis that a skilled artisan would have found that the inventors possessed the recited genus. (*Id.*, 25.)

XII. ANCESTOR APPLICATIONS OF THE '880 PATENT FAIL TO ENABLE A SPECIFIC CONTACT RESISTIVITY LESS THAN $1\ \Omega\text{-}\mu\text{m}^2$

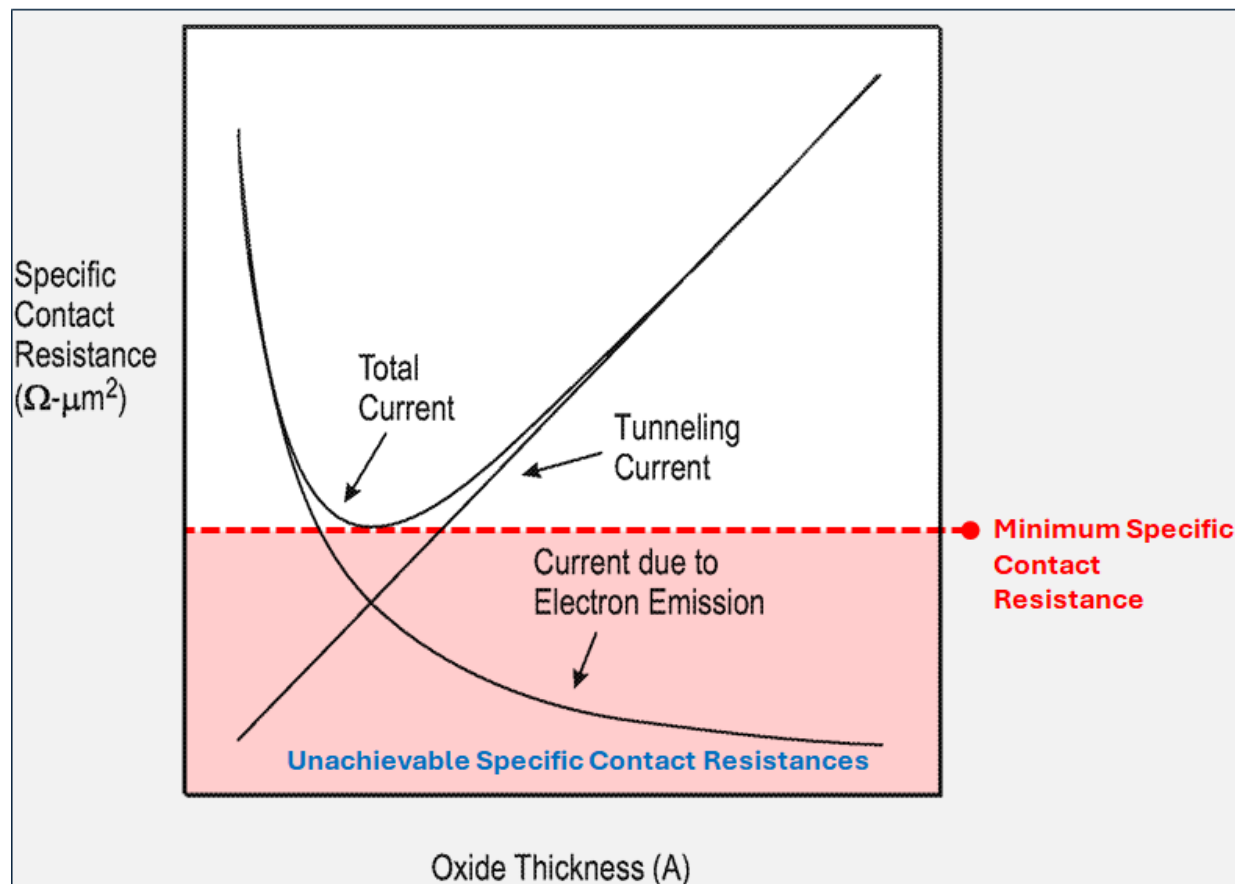
Claims 26 and 28 require a specific contact resistivity “of less than $10\ \Omega\text{-}\mu\text{m}^2$ ” whereas Claim 27 requires a specific contact resistivity “of less than $1\ \Omega\text{-}\mu\text{m}^2$.” However, none of the ancestor applications enable a specific contact resistivity of the full breadth of the ranges of less than $10\ \Omega\text{-}\mu\text{m}^2$ or less than $1\ \Omega\text{-}\mu\text{m}^2$. In the *inter partes* review challenging Claims 18 and 25-29 of the '691 Patent filed by Samsung containing the same claim element of “less than $1\ \Omega\text{-}\mu\text{m}^2$,” the Board found that these claims were not entitled to the benefit of any of the priority applications for the '691 patent because the ancestor applications of the '691 Patent do not enable the full breadth of the recited range of “less than $1\ \Omega\text{-}\mu\text{m}^2$.” (Ex.1133, 37-39.) The Board should reach the same conclusion as to Claims 26-28 of the '880 Patent.

“The enablement requirement asks whether ‘the specification teach[es] those in the art to make and use the invention without undue experimentation.’” *Enzo Life*

Scis., Inc. v. Roche Molecular Sys., Inc., 928 F.3d 1340, 1345 (Fed. Cir. 2019), *cert. denied*, 206 L.Ed.2d 513 (Mar. 30, 2020) (quoting *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988)); *Magsil Corp. v. Hitachi Global Storage Techs., Inc.*, 687 F.3d 1377, 1380-81 (Fed. Cir. 2012); *In re Goodman*, 11 F.3d 1046, 1050 (Fed. Cir. 1993). The '880 Patent and its ancestor applications fall well short of that mark. As written, the resistivity limitation in Claims 26-28 has no lower bound on specific contact resistivity. The specification imposes no lower bound on specific contact resistivity, either, as it does not quantify or describe any lower bound for the “minimum specific contact resistance” that it purports to describe. (Ex.1001, Fig. 8, 4:56-5:3, 15:34-54.) Thus, the “less than 1 $\Omega\text{-}\mu\text{m}^2$ ” part of that limitation encompasses specific contact resistivities down to and including approximately zero.

But specific contact resistances down to and including approximately zero cannot be achieved according to the teachings of the '880 Patent and its ancestor applications. Their shared disclosure purports to describe an interface layer that minimizes the total specific contact resistance (specific contact resistivity) of a metal-semiconductor junction, represented below by the “total current” curve that sums (1) resistance to tunneling current and (2) resistance to current by electron

emission:



(Ex.1001, Fig. 8 (annotations added), 14:29-49; Ex.1022, ¶¶ 166-171.)

As can be seen from the annotated figure above, the nadir of Fig. 8’s “total current” curve indicates a range of specific contact resistivities down to and including approximately zero that an ordinarily skilled artisan could not have attained by following the teachings of the ’880 Patent and its ancestor applications. Thus, those parent applications fail to enable the *full* scope of the specific contact resistivity “of less than $10\ \Omega\text{-}\mu\text{m}^2$ ” or “of less than $1\ \Omega\text{-}\mu\text{m}^2$ ” limitations in Claims 26-28. (Ex.1022, ¶¶ 172-181.)

Nor should the Board constrain “less than 10 $\Omega\text{-}\mu\text{m}^2$ ” or “less than 1 $\Omega\text{-}\mu\text{m}^2$ ” to some lower bound in order to enable Claims 26-28. *Chef America, Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004) (warning against redrafting claims); *see also Magsil Corp. v. Hitachi Global Storage Techs., Inc.*, 687 F.3d 1377, 1381 (Fed. Cir. 2012).

Claims 26-28 are no better off than the non-enabled claims in *Magsil*. The ’880 Patent and the parent applications do not describe any working examples of an electrical junction with a specific contact resistivity under 10 $\Omega\text{-}\mu\text{m}^2$ or 1 $\Omega\text{-}\mu\text{m}^2$, down to and including approximately zero—a range encompassed by each of Claims 26-28. Worse still, despite the ’880 Patent and its ancestor applications expressly teaching that the disclosed techniques cannot reduce specific contact resistivity below some unspecified minimum, the patentee nonetheless drafted open-ended claims with no lower bound on specific contact resistivity. (Ex.1001, Fig. 8, 15:34-54; Ex.1022, ¶¶ 172-181.)

Because Claims 26-28 encompass a range of specific contact resistivities down to and including approximately zero that cannot be achieved according to the ’880 Patent’s ancestors applications, those parent applications cannot enable the full scope of the challenged claims. *Magsil*, 687 F.3d at 1382. And when the breadth of a claim alone indicates that the claim is not enabled—as is the case here—that disposes of the enablement issue in its entirety, as it did in *Magsil*. *CommVault Sys.*,

Inc. v. Realtime Data, LLC, IPR2017-01710, Paper 11 at 20 (P.T.A.B. Jan. 18, 2018) (citing *Magsil*, 687 F.3d at 1382). Because no ancestor application enables the full scope of the challenged claims, their priority date is no earlier than the filing date of the '880 Patent: May 12, 2020.

In light of Acorn's arguments in earlier petitions, Oak may argue that the specification provides adequate disclosure. (Ex.1133, 29-32.) However, the Board has already found these arguments to be "off the mark" because the issue is "whether the disclosure enables the specific numerical ranges recited in the claims." (Ex.1133, 32.) The Board concluded that the ancestor applications of the '691 Patent do not enable the breadth of the recited range of "less than 1 $\Omega\text{-}\mu\text{m}^2$." (Ex. 1133, 37-39.) Given that the '880 Patent shares the specification with the '691 Patent, it also does not enable the breadth of the recited range of "less than 1 $\Omega\text{-}\mu\text{m}^2$. As the Board found in the claims of the '691 Patent (Ex. 1133, 38-39.), Grupp'483 enables the upper part of the range for purposes of anticipation and thus is prior art for Claims 26-28 of the '880 Patent.

XIII. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Grupp'483 anticipates Claims 1-22

1. Claim 1

a) An electrical junction, comprising:

To the extent the preamble is limiting, Grupp'483 discloses it. "[T]he present invention provides an electrical junction that includes a semiconductor (e.g., C, Ge,

or an Si-based semiconductor), a conductor, and an interface layer disposed therebetween.” (Ex.1021, 3:44-47; *see also id.*, 3:18-22, 5:49-58, 19:26-27.)

b) an interface layer disposed between a contact metal and a source or drain of a transistor,

Grupp’483 discloses this limitation. Grupp’483 describes that its invention is generally applicable to a broad category of metal-semiconductor contacts, which can include contacts to the source or drain of a transistor that is formed in a semiconductor region. (Ex.1021, 18:32-35.) Further, Grupp’483 discloses an interface layer disposed between and in contact with the source or drain of a transistor and a metal (i.e., metal electrical contact). For example, “the present invention provides an electrical device in which *an interface layer is disposed between and in contact with a metal and a semiconductor . . .*” (Ex.1021, 4:21-23; *see also id.*, Fig. 7d, 3:18-22, 3:44-47, 5:49-58, 18:4-17.) Grupp’483 discloses that the junction can be used in making contacts to source or drain implanted wells. (Ex.1021, 18:19-20, 19:11-15.)

c) the source or drain of the transistor comprising a silicon-based semiconductor, and

Grupp’483 discloses this limitation. Grupp’483 states “that for thin interface layers disposed between a metal and a semiconductor (e.g., C, Ge, Si, SiC and SiGe), so as to form a metal—interface layer—semiconductor junction, there exist corresponding minimum specific contact resistances.” (Ex.1021, 3:18-22.) “[T]he

present invention provides an electrical junction that includes a semiconductor (e.g., C, Ge, or an Si-based semiconductor), a conductor, and an interface layer disposed therebetween.” (*Id.*, 3:44-47.)

Grupp’483 describes that its invention is generally applicable to a broad category of metal-semiconductor contacts, which can include contacts to the source or drain of a transistor: “[t]he source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention.” (*Id.*, 18:32-35.)

One example of a region in a semiconductor substrate that Grupp’483 discloses is a source or drain of a transistor. Grupp’483 discloses that “the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility).” (Ex.1021, 18:19-20, 19:11-15.) In a transistor, a ‘well’ is a doped region of a semiconductor in which source and drain regions are formed by implanting dopants; the source and drain regions have a doping opposite that of the well. (Ex.1022, ¶197.)

d) the interface layer comprising a spacer layer that is an oxide of titanium and a semiconductor oxide passivation layer,

Grupp'483 discloses this limitation. Grupp'483 discloses an interface layer that includes (1) a spacer layer, which can be titanium dioxide; and (2) a passivation layer, which can be a semiconductor oxide.

First, for a spacer layer, Grupp'483 discloses that an interface layer can include a separation layer which is made of an oxide. (Ex.1021, 11:27-38.) The separation layer can be a “spacer layer” of TiO₂, which is titanium dioxide: “[s]pacer layers may be used with lower barriers (e.g., TiO₂ has a barrier of less than 1 eV).” (*Id.*, 18:65-67; *see also id.*, 18:45-65.)

Second, for the semiconductor oxide for a passivation layer, Grupp'483 discloses, for example, “[t]he interface layer includes a passivating material, for example, a nitride, a fluoride, an **oxide**, an oxynitride, a hydride and/or an arsenide **of the semiconductor**, and in some cases may also include a separation layer.” (Ex.1021, 3:53-56; *see also id.*, 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-44, 10:48-54, 10:60-63, 11:35-38, 13:41-46.)

Thus, Grupp'483 discloses an interface layer comprising a spacer layer that is an oxide of titanium and a semiconductor oxide passivation layer.

- e) **wherein the semiconductor oxide passivation layer has a thickness of less than about 1 nm.**

Grupp'483 discloses this limitation. Grupp'483 discloses that “[o]ften, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm.” (Ex.1021, 10:66-11:4.)

2. Claim 2

- a) **The electrical junction of claim 1,**

Grupp'483 discloses the electrical junction of Claim 1, as discussed in **Section XIII.A.1.**

- b) **wherein the contact metal comprises one of: platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), or palladium (Pd).**

Grupp'483 discloses this element. Grupp'483 discloses that “[t]he conductor 630 contains a conductive material such as a metal or an alloy of a metal” (Ex.1021, 14:5-6). Grupp'483 further discloses that “[e]xemplary metals that have a work function greater than silicon include *platinum (Pt)*, iridium (Ir), *gold (Au)*, *tungsten (W)*, *nickel (Ni)*, *molybdenum (Mo)*, *copper (Cu)*, *cobalt (Co)*, and *palladium (Pd)*.” (Ex.1021, 14:58-15:5)¹⁰.

¹⁰ Emphasis added unless noted.

3. Claim 3

a) The electrical junction of claim 2,

Grupp'483 discloses the electrical junction of Claim 2, as discussed in **Section XIII.A.2.**

b) wherein the silicon-based semiconductor comprises one of: Si, SiGe, and SiC.

Grupp'483 discloses this limitation. For example, “[t]he present inventors have determined that for thin interface layers disposed between a metal and a semiconductor (e.g., C, Ge, Si, SiC and SiGe), so as to form a metal—interface layer—semiconductor junction, there exist corresponding minimum specific contact resistances.” (Ex.1021, 3:18-22.) “[T]he present invention provides an electrical junction that includes a semiconductor (e.g., C, Ge, or an Si-based semiconductor), a conductor, and an interface layer disposed therebetween.” (*Id.*, 3:44-47.)

4. Claim 4

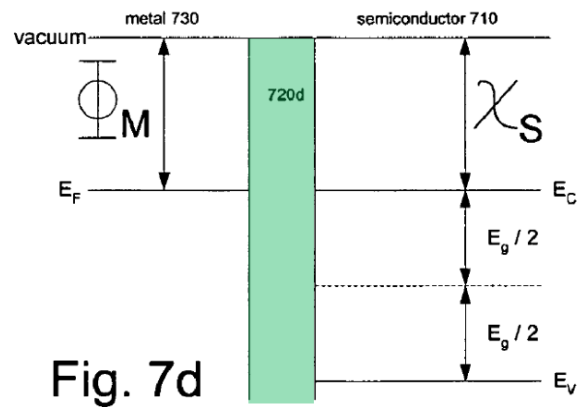
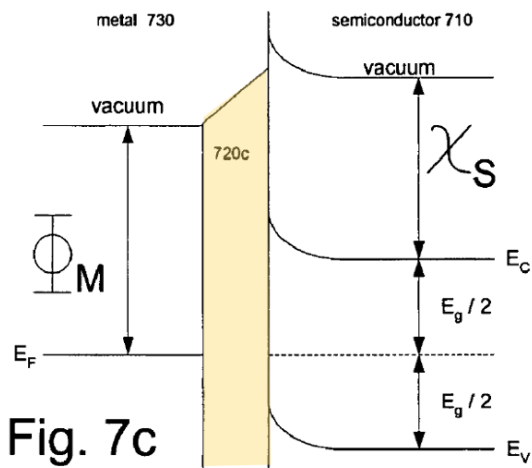
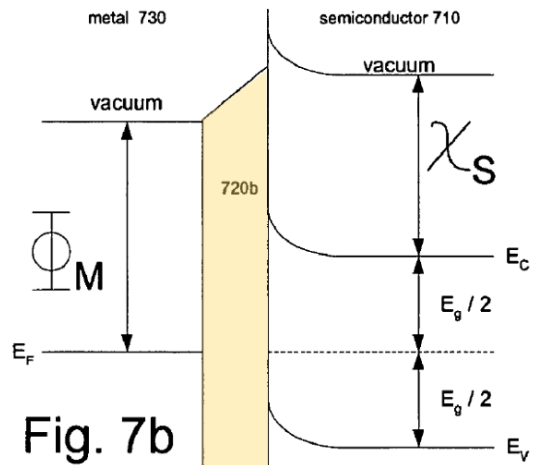
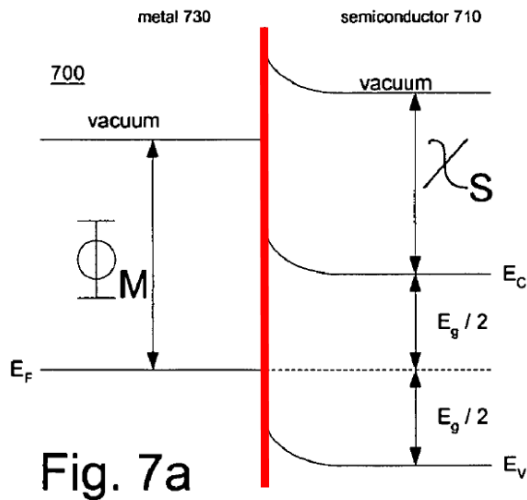
a) The electrical junction of claim 1,

Grupp'483 discloses the electrical junction of Claim 1, as discussed in **Section XIII.A.1.**

b) wherein the silicon-based semiconductor comprises an n-type semiconductor and

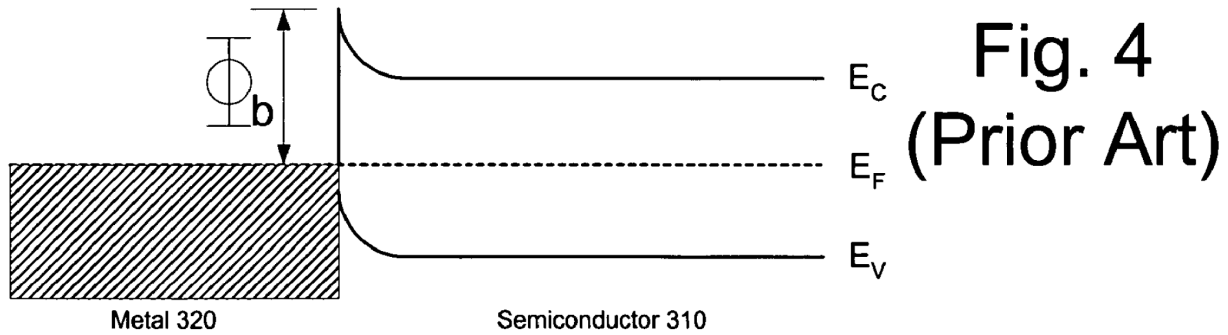
Grupp'483 discloses this limitation. Grupp'483 discloses that the semiconductor can be an n-type doped semiconductor. (Ex.1021, 6:5-9.)

Further, Fig. 7d of Grupp'483 shows a metal-interface layer-semiconductor junction, in which the semiconductor is an n-type semiconductor. (Ex.1021, Fig. 4, Fig. 7a, Fig. 7d, 5:22-23, 5:37-40, 18:4-10.) Grupp'483 depicts a series of band diagrams for metal-semiconductor junctions in Figs. 7a-7d, where the metal can be aluminum, and where the semiconductor can be n-type silicon. (Ex.1021, 5:33-40, 17:50-18:17.) In contrast to Figs. 7b-7d, which depict interface layers 720b, 720c, and 720d between the metal 730 and the semiconductor 710, Fig. 7a does not depict any interface layer, indicating that the metal 730 and the semiconductor 710 are in **direct contact with no interface layer** in Fig. 7a.



(Ex.1021, Figs. 7a-7d (annotations added), 5:33-40, 17:50-18:17.)

As Dr. Schubert explains, Grupp'483's Fig. 7a depicts the same band bending as Grupp'483's Fig. 4, which is described as a junction between a metal and an n-type semiconductor:



(Ex.1021, Fig. 4, 5:22-23, 8:10-15; Ex.1022, ¶¶198-199.)

Grupp'483 explains that Fig. 4 depicts a junction between an n-type semiconductor and a metal with barrier height ϕ_b , which is the difference between the Fermi level of the metal E_F and the conduction band edge of the semiconductor E_C at the interface. (Ex.1021, 5:22-23, 8:10-15.) A POSITA would have recognized that Fig. 4 and Figs. 7a-7d also depict band bending present in a junction of an n-type semiconductor and a metal. (Ex.1021, Fig. 4, Fig. 7a, 5:22-23, 8:10-15, 18:4-17.)

- c) the contact metal comprises one of: platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), or palladium (Pd).**

Grupp'483 discloses this element, as discussed in **Section XIII.A.2.b).**

5. Claim 5

- a) The electrical junction of claim 1,**

Grupp'483 discloses the electrical junction of Claim 1, as discussed in **Section XIII.A.1.**

- b) wherein the semiconductor oxide passivation layer is an oxide of the silicon-based semiconductor.**

Grupp'483 discloses this element. Grupp'483 discloses using a semiconductor oxide as a passivating material, as discussed in **Section XIII.A.1.d)**. Further, Grupp'483 discloses using either an oxide of silicon (Ex.1021, 10:27-34, 10:48-54, 10:60-63) or silicon dioxide (*id.*, 8:64-9:10) as the passivating semiconductor oxide.

6. Claim 6

- a) The electrical junction of claim 5,**

Grupp'483 discloses the electrical junction of Claim 5, as discussed in **Section XIII.A.5.**

- b) wherein the silicon-based semiconductor is an n-type doped semiconductor.**

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b)**.

7. Claim 7

- a) The electrical junction of claim 1,**

Grupp'483 discloses the electrical junction of Claim 1, as discussed in **Section XIII.A.1.**

- b) wherein the semiconductor oxide passivation layer is an oxide of silicon.**

Grupp'483 discloses this element, as discussed in **Section XIII.A.5.b)**.

8. Claim 8

a) The electrical junction of claim 7,

Grupp'483 discloses the electrical junction of Claim 7, as discussed in **Section XIII.A.7.**

b) wherein the silicon-based semiconductor is an n-type doped semiconductor.

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b).**

9. Claim 9

a) The electrical junction of claim 1,

Grupp'483 discloses the electrical junction of Claim 1, as discussed in **Section XIII.A.1.**

b) wherein the silicon-based semiconductor comprises an n-type silicon,

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b).**

c) the semiconductor oxide passivation layer of the interface layer is adjacent the silicon-based semiconductor and is an oxide of silicon, and

Grupp'483 discloses this element. Grupp'483 discloses two semiconductor oxides as passivating dielectric tunnel barrier layers: silicon oxide and silicon dioxide. (Ex.1021, 10:27-34, 10:48-54, 10:60-63 (silicon oxide); Ex.1021, 8:64-9:10 (silicon dioxide).) Grupp'483 further discloses forming a passivation material such as *silicon oxide* or *silicon dioxide* on a silicon surface such that it is adjacent to the

semiconductor region made of silicon and bonds to the silicon. (Ex.1021, 8:64-9:10, 10:27-34.)

d) the contact metal comprises titanium.

Grupp'483 discloses this limitation. Grupp'483 discloses that “[t]he conductor 630 contains a conductive material such as a metal or an alloy of a metal” (Ex.1021, 14:5-6). Grupp'483 further discloses that “[e]xemplary metals that have a work function smaller than silicon include Group 3A elements, . . . titanium (Ti).” (Ex.1021, 14:58-66.)

10. Claim 10

a) The electrical junction of claim 1,

Grupp'483 discloses the electrical junction of Claim 1, as discussed in **Section XIII.A.1.**

b) wherein the silicon-based semiconductor comprises an n-type silicon,

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b).**

c) the semiconductor oxide passivation layer of the interface layer is adjacent the silicon-based semiconductor and is an oxide of silicon.

Grupp'483 discloses this element, as discussed in **Section XIII.A.9.c).**

11. Claim 11

a) The electrical junction of claim 10,

Grupp'483 discloses the electrical junction of Claim 10, as discussed in **Section XIII.A.10.**

- b) wherein the spacer layer presents a potential barrier lower than 1 eV.**

Grupp'483 discloses this element. Grupp'483 discloses that an interface layer can include a separation layer which is made of an oxide. (Ex.1021, 11:27-38.) More specifically, the separation layer can be a “[s]pacer layer” of TiO₂, which “has a barrier of less than 1 eV.” (*Id.*, 18:65-67; *see also id.*, 18:45-65.)

12. Claim 12

- a) The electrical junction of claim 1,**

Grupp'483 discloses the electrical junction of Claim 1, as discussed in **Section XIII.A.1.**

- b) wherein the contact metal is titanium.**

Grupp'483 discloses this element, as discussed in **Section XIII.A.9.d).**

13. Claim 13

- a) The electrical junction of claim 1,**

Grupp'483 discloses the electrical junction of Claim 1, as discussed in **Section XIII.A.1.**

- b) wherein the passivation layer is adjacent to the source or drain of the transistor.**

Grupp'483 discloses this limitation, as discussed in **Sections XIII.A.9.c), XIII.A.1.b) and XIII.A.1.c).**

14. Claim 14

a) The electrical junction of claim 13,

Grupp'483 discloses the electrical junction of Claim 13, as discussed in **Section XIII.A.13.**

b) wherein the contact metal comprises tungsten.

Grupp'483 discloses this limitation, as discussed in **Section XIII.A.2.b).**

15. Claim 15

a) The electrical junction of claim 14,

Grupp'483 discloses the electrical junction of Claim 14, as discussed in **Section XIII.A.14.**

b) wherein the semiconductor comprises an n-type doped semiconductor.

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b).**

16. Claim 16

a) The electrical junction of claim 14,

Grupp'483 discloses the electrical junction of Claim 14, as discussed in **Section XIII.A.14.**

b) wherein the semiconductor comprises n-type silicon.

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b).**

17. Claim 17

a) The electrical junction of claim 16,

Grupp'483 discloses the electrical junction of Claim 16, as discussed in **Section XIII.A.16.**

b) wherein the semiconductor oxide passivation layer is an oxide of silicon.

Grupp'483 discloses this element, as discussed in **Section XIII.A.5.b).**

18. Claim 18

a) The electrical junction of claim 13,

Grupp'483 discloses the electrical junction of Claim 13, as discussed in **Section XIII.A.13.**

b) wherein the contact metal comprises titanium.

Grupp'483 discloses this element, as discussed in **Section XIII.A.9.d).**

19. Claim 19

a) The electrical junction of claim 18,

Grupp'483 discloses the electrical junction of Claim 18, as discussed in **Section XIII.A.18.**

b) wherein the semiconductor comprises an n-type doped semiconductor.

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b).**

20. Claim 20

a) The electrical junction of claim 18,

Grupp'483 discloses the electrical junction of Claim 18, as discussed in **Section XIII.A.18.**

b) wherein the semiconductor comprises n-type silicon.

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b).**

21. Claim 21

a) The electrical junction of claim 20,

Grupp'483 discloses the electrical junction of Claim 20, as discussed in **Section XIII.A.20.**

b) wherein the semiconductor oxide passivation layer is an oxide of silicon.

Grupp'483 discloses the electrical junction of Claim 20, as discussed in **Section XIII.A.5.b).**

22. Claim 22

a) An electrical junction, comprising

Grupp'483 discloses the electrical junction, as discussed in **Section XIII.A.1.a).**

b) an interface layer disposed between and in contact with a contact metal and a source or drain of a transistor,

Grupp'483 discloses this element, as discussed in **Section XIII.A.1.b).** For example, “[i]n further embodiments the present invention provides an electrical

device in which *an interface layer is disposed between and in contact with a metal and a semiconductor . . .*” (Ex.1021, 4:21-23; *see also id.*, Fig. 7d, 3:18-22, 3:44-47, 5:49-58, 18:4-17.)

- c) **the source or drain of the transistor comprising an n-type silicon-based semiconductor,**

Grupp’483 discloses this element, as discussed in **Section XIII.A.4.b).**

- d) **the contact metal comprising titanium, and**

Grupp’483 discloses this element, as discussed in **Section XIII.A.9.d).**

- e) **the interface layer comprising a spacer layer that is an oxide of titanium that presents a potential barrier lower than 1 eV and**

Grupp’483 discloses this element. Grupp’483 discloses that an interface layer can include a separation layer which is made of an oxide. (Ex.1021, 11:27-38.) More specifically, the separation layer can be a “spacer layer” of TiO₂, an oxide of titanium, which “has a barrier of less than 1 eV.” (*Id.*, 18:65-67; *see also id.*, 18:45-65.)

- f) **a passivation layer adjacent the silicon-based semiconductor that is an oxide of silicon and**

Grupp’483 discloses this element, as discussed in **Section XIII.A.9.c).**

- g) **has a thickness of less than about 1 nm.**

Grupp’483 discloses this element, as discussed in **Section XIII.A.1.e).**

B. Ground 1: Grupp’483 anticipates Claims 26-28

In the Acorn Litigation, Samsung appealed to the Federal Circuit noting that Board’s finding of no anticipation for Claims 18 and 26-29 of the ’691 Patent (i.e., specific contact resistivity claims) was an oversight of its own finding that the claims were not enabled. (Ex.1122, 48-50.) Acorn conceded that the Board “should have listed those claims as unpatentable because the Board found them unenabled. That was a simple typographical error.” (Ex.1123, 82.) The same conclusion is warranted here.

Petitioners address Claims 23-25 to show that Grupp’483 anticipates Claims 26-28 because Claims 26-28 depend upon Claims 23-25.

1. Claim 23

a) An electrical junction, comprising

Grupp’483 discloses the electrical junction, as discussed in **Section XIII.A.1.a).**

b) an interface layer disposed between and in contact with a conductor and a source or drain of a transistor,

Grupp’483 discloses this element, as discussed in **Section XIII.A.22.b).**

c) the conductor comprising a metal silicide,

Grupp’483 discloses this element. Grupp’483 discloses that “[t]he conductor may be one of: a metal, an alloy of a metal, *a metal silicide*.” (Ex.1021, 3:63-66.)

- d) **the source or drain of the transistor comprising an n-type silicon-based semiconductor, and**

Grupp'483 discloses this element, as discussed in **Section XIII.A.4.b)**.

- e) **the interface layer comprising a passivation layer adjacent the silicon-based semiconductor that is an oxide of silicon,**

Grupp'483 discloses this element, as discussed in **Section XIII.A.9.c)**.

- f) **the passivation layer having a thickness of less than about 1 nm.**

Grupp'483 discloses this element, as discussed in **Section XIII.A.1.e)**.

2. Claim 24

- a) **The electrical junction of claim 23,**

Grupp'483 discloses the electrical junction, as discussed in **Section XIII.B.1.a)**.

- b) **wherein the interface layer further includes a separation layer between the contact metal and the passivation layer.**

Grupp'483 discloses this limitation, as discussed in **Sections XIII.A.1.b)** (disclosing the interface layer between a contact metal and source or drain of a transistor) and **XIII.A.1.d)** (disclosing the interface layer comprising a spacer layer and a passivation layer). Though Claim 1 recites a “spacer layer” instead of a “separation layer,” the '880 Patent uses the terms interchangeably. (Ex.1001, 9:36-10:24, 18:7-8.) Because Grupp'483 discloses that the passivation layer is adjacent the silicon-based semiconductor that is an oxide of silicon as discussed in **Section**

XIII.A.9.c) above, the separation layer will be between the contact metal and the passivation layer.

3. Claim 25

a) The electrical junction of claim 24,

Grupp’483 discloses the electrical junction of Claim 24, as discussed in **Section XIII.B.2.**

b) wherein the interface layer has a thickness of less than 5 nm.

Grupp’483 discloses this limitation. Grupp’483 discloses that “[o]ften, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm.” (Ex.1021,10:66-11:4.)

4. Claim 26

a) The electrical junction of claim 25,

Grupp’483 discloses the electrical junction of claim 25, as discussed in **Section XIII.B.3.**

b) wherein the interface layer configured to provide a specific contact resistivity of the electrical junction of less than 10 $\Omega\text{-}\mu\text{m}^2$.

Grupp’483 discloses this limitation. “Specific contact resistivity” is interchangeable with “specific contact resistance.” *See Section VIII.*

Grupp’483 discloses “that for thin interface layers disposed between a metal and a semiconductor, so as to form a metal-interface layer-semiconductor junction,

there exist corresponding minimum specific contact resistances.” (Ex.1021, 5:64-6:1.) “Indeed, minimum specific contact resistances of even less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ or even less than equal to approximately $1\ \Omega\text{-}\mu\text{m}^2$ may be achieved for such junctions in accordance with the present invention.” (Ex.1021, 6:1-5; *see also id.*, 3:40-43, 5:64-6:1, 8:58-61, 10:44-47; 15:52-57.) Grupp’483 therefore discloses some non-zero specific contact resistivity of less than $10\ \Omega\text{-}\mu\text{m}^2$, such as a specific contact resistivity just under $10\ \Omega\text{-}\mu\text{m}^2$, between the n-type doped source or drain and the metal electric contact. (Ex.1022, ¶200.)

5. Claim 27

a) The electrical junction of claim 26,

Grupp’483 discloses the electrical junction of Claim 26, as discussed in **Section XIII.B.2.**

b) wherein the interface layer configured to provide a specific contact resistivity of the electrical junction of less than $10\ \Omega\text{-}\mu\text{m}^2$.

Grupp’483 discloses this element, as discussed in **Section XIII.B.4.b).**

6. Claim 28

a) A field effect transistor, comprising

Grupp’483 discloses a field effect transistor. Grupp’483 describes that its invention is generally applicable to a broad category of metal-semiconductor contacts, which can include contacts to the source or drain of a transistor: “[t]he source and drain contacts at the channel of a *field effect transistor* are examples of

a broader category of metal-interface layer-semiconductor contacts that make up the present invention.” (Ex.1021, 18:32-35.)

- b) an electrical junction that includes an interface layer disposed between and in contact with a contact metal and a source or drain of the field effect transistor,**

Grupp’483 discloses this element, as discussed in **Sections XIII.A.22.a) and XIII.A.22.b).**

- c) the source or drain comprising n-type silicon,**

Grupp’483 discloses this element, as discussed in **Section XIII.A.4.b).**

- d) the contact metal comprising titanium,**

Grupp’483 discloses this element, as discussed in **Section XIII.A.9.d).**

- e) the interface layer including a spacer layer that is an oxide of titanium and**

Grupp’483 discloses this element, as discussed in **Section XIII.A.1.d).**

- f) a passivation layer adjacent the source or drain that is an oxide of silicon,**

Grupp’483 discloses this element, as discussed in **Section XIII.A.9.c).**

- g) wherein the passivation layer has a thickness of less than about 1 nm and**

Grupp’483 discloses this element, as discussed in **Section XIII.A.1.e).**

- h) the electrical junction is operable to pass a current between the contact metal and the source or drain**

Grupp’483 discloses this element. “FIG. 6 shows an example of a diode 600 containing, . . . an interface layer 620 disposed between and attached to both a

semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.” (Ex.1021, 13:63-14:4; 6:50-60 (“Such junctions are formed in the present invention between a metal with a workfunction These junctions are diodes.”); *see also id.*, 5:64-6:5.)

i) while presenting a specific contact resistivity of less than $10\ \Omega\text{-}\mu\text{m}^2$.

Grupp’483 discloses this element, as discussed in **Section XIII.B.4.b).**

C. Ground 2: Jammy renders obvious claims 23, 24, and 25

Jammy generally describes a MOSFET (metal oxide semiconductor field effect transistor) that incorporates quantum conductive barrier layers 56 and 58 between conductive studs 52 and 54 and shallow source/drain diffusions (doped regions) 42 and 44 in a silicon substrate, as depicted below:

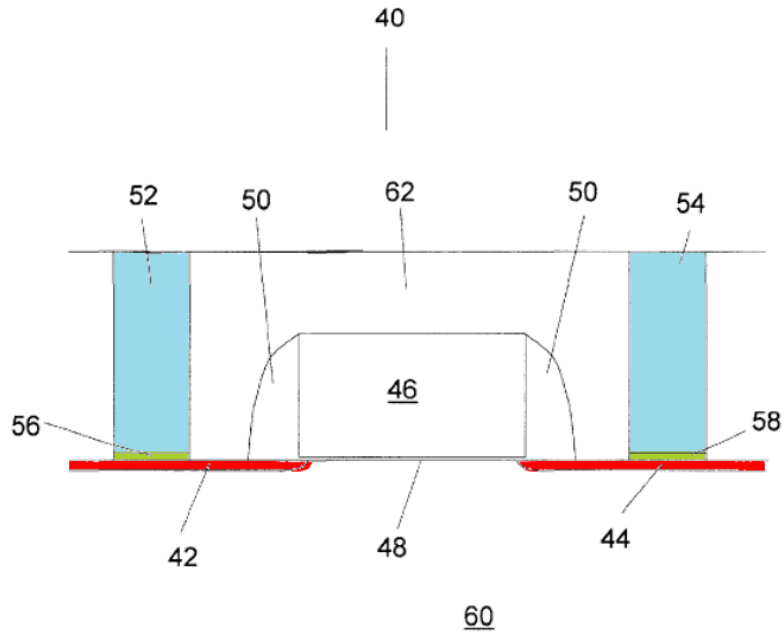


Figure 1

(Ex.1101, Fig. 1 (annotated), 2:42-53, 3:16-22.)

Jammy states that “[t]he invention is not limited to any specific device configuration incorporating the structures of the invention, however, the structures of the invention are preferably incorporated into a MOSFET or other transistor devices.” (Ex.1101, 4:1-5.) Jammy provides “[e]xamples of various transistor structures,” including U.S. Patent No. 5,792,703 (Ex.1128, “Bronner”), and states that “disclosures of which are incorporated herein by reference.” (Ex.1101, 4:5-8.) Thus, Jammy incorporates Bronner by reference. (See MPEP §2163.07(b); *Arbutus Biopharma Corp. v. ModernaTX, Inc.*, 65 F.4th 656, 662-63 (Fed. Cir. 2023) (“When a reference or material from various documents is incorporated, they are ‘effectively part of the host document as if [they] were explicitly contained therein.’”).)

Like Jammy, Bronner also pertains to Field Effect Transistors (FETs). (Ex.1128, 5:7-8.) Bronner discloses a method of making self-aligned electrical contacts to the device region (or diffusion regions) in a substrate. Fig. 4 of Bronner is a cross-sectional view of “a silicon substrate 50” having several FETs. (Ex.1128, 3:1-3, 7-8).

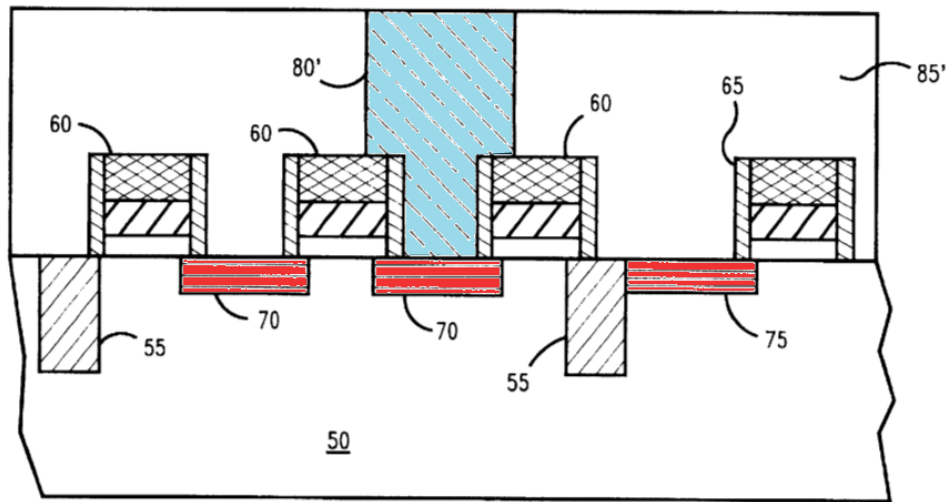


FIG. 4

(Ex.1128, Fig. 4 (annotated).) Like Jammy, Bronner discloses the components of an FET, i.e., a gate 60, **diffusion regions 70 and 75** in the substrate, and a **contact opening 80'** that is filled with conductor. (Ex.1128, 3:6-12, 4:6-7.) In view of Jammy's suggestion that its invention can be incorporated in the transistor disclosed in Bronner, a POSITA would place Jammy's **quantum conductive barrier layer 90** between the **filled contact opening 80'** and the **diffusion region 70** of the modified transistor in Bronner, as shown in the annotated Figure 4 below:

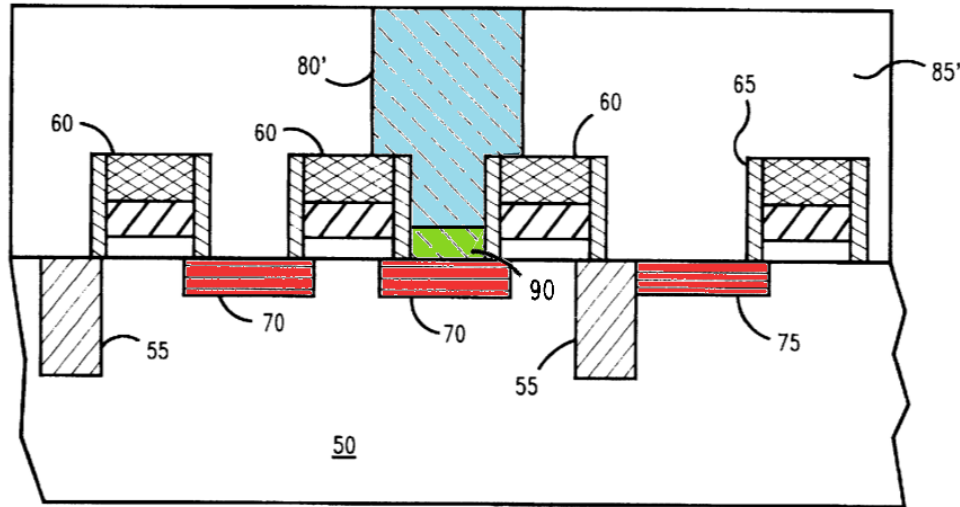


FIG. 4

(Ex.1128, Fig. 4 (annotated and modified).) In view of the benefits of the quantum conductive barrier layer disclosed in Jammy, a POSITA would be motivated to incorporate such a layer in the FET disclosed in Bronner because such a modification would improve Bronner's FET. (Ex.1022, ¶¶194-196.) As Dr. Schubert explains, incorporation of Jammy's layer in Bronner's FET would require combination of known elements in a known manner. (*Id.*) A POSITA would be familiar with the techniques involved in the fabrication of such devices, and, thus, would have a reasonable expectation of success. (*Id.*)

1. Claim 23

a) An electrical junction, comprising:

To the extent the preamble is limiting, Jammy discloses the preamble. As shown in modified Fig. 4, Bronner discloses an "electrical junction." (Ex.1128, 3:61-4:1.) Because Figure 4 depicts a modified Field Effect Transistor (FET), the "contact

opening 80' [that] is filled with a conductor" is in electrical contact with the "diffusion region 70" through the quantum conductive barrier layer 90. (Ex.1128, 3:65-4:11.) Jammy discloses that the quantum conductive barrier layer is conductive. (Ex.1101, 3:23-27.) The filled contact opening 80' and drain diffusion regions 70, 75, along with quantum conductive barrier layer 90, form an electrical junction. As the Board has previously found, the '395 Patent, which shares the specification with the '880 Patent, uses the terms "contact" and "junction" interchangeably. (Ex.1097, 18.)

b) an interface layer disposed between and in contact with a conductor and a source or drain of a transistor,

Jammy discloses an interface layer. The modified FET in Bronner incorporates Jammy's quantum conductive barrier layer 90 between the contact openings 80' that are filled with a conductor and diffusion regions 70 in the substrate, as shown below:

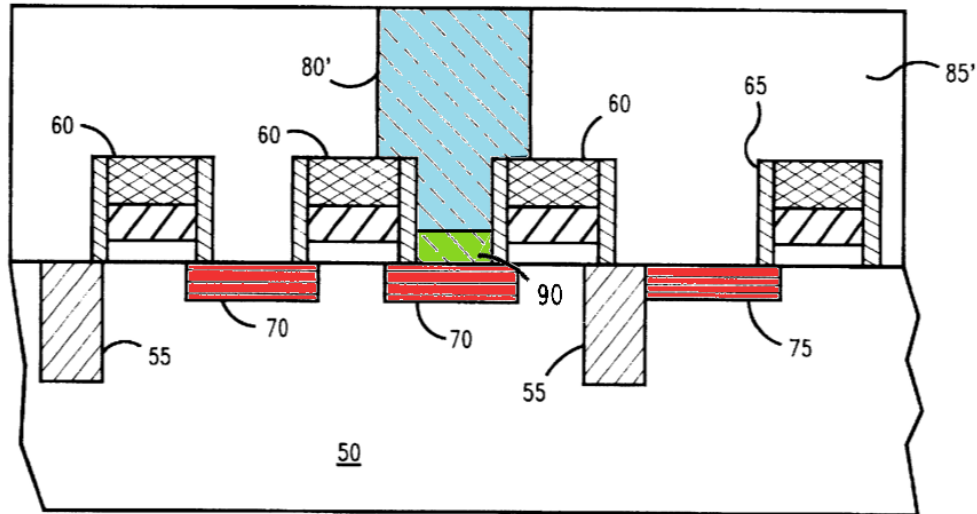


FIG. 4

(Ex.1128, Fig. 4 (annotated and modified).)

The filled contact opening 80' in Fig. 4 of Bronner forms a conductor. Because Bronner depicts a FET, a POSITA would understand that diffusion regions 70 in the silicon substrate 50 are a source or drain of a transistor.¹¹ Jammy discloses that “[t]he quantum conductive layers of the invention are very thin films of materials which in their bulk properties would be considered dielectrics (i.e., electrical insulators). In very thin layers, however, these materials become

¹¹ Mirroring the structure of Bronner, Jammy refers to diffusion regions 42 and 44 as source and drain diffusion regions. (Ex.1101, 4:9-17) (“FIG. 1 shows a schematic side view of a MOSFET 40 in a substrate 60. Shallow source/drain diffusions (doped regions) 42 and 44 are formed in substrate 60.”)

electrically conductive.” (Ex.1101, 3:23-27; *see also id.*, 3:61-4:1.) The **quantum conductive barrier layer 90** in annotated Fig. 4 above in Bronner is an interface layer that is between and in contact with a conductor and a source or drain of a transistor.

c) the conductor comprising a metal silicide,

Jammy discloses this element. Bronner discloses that “[t]he contact opening 80’ is filled with a conductor, such as . . . *metal silicide[,]* or *silicides of titanium, cobalt, platinum or palladium.*” (Ex.1128, 4:6-11.) Thus, the **filled contact opening 80’** comprises a metal silicide and is a conductor.

d) the source or drain of the transistor comprising an n-type silicon based semiconductor, and

Jammy discloses this limitation. Fig. 4 of Bronner depicts a Field Effect Transistor (FET) and diffusion regions 70, 75 formed on a silicon substrate 50. (Ex.1128, 3:7-9, 47-51.) A POSITA would understand that source or drain regions in a FET are formed on N-type or P-type substrate. For example, Jammy discloses forming **source/drain diffusions 42 and 44** by implanting n-type dopants into a silicon substrate, i.e., a semiconductor. (Ex.1101, 4:33-38 (“The shallow diffusions would typically be formed by diffusing an appropriate N-type or P-type dopant into the substrate.”).)

- e) **the interface layer comprising a passivation layer adjacent to the silicon-based semiconductor that is an oxide of silicon, the passivation layer having a thickness of less than about 1 nm.**

Jammy renders this element obvious. The quantum conductive barrier layer 90 in the modified transistor in Bronner is next to the diffusion regions 70 formed in the silicon substrate 50. (Ex.1128, 3:7). Thus, the quantum conductive barrier layer 90 is an interface layer comprising a passivation layer that is adjacent to the silicon-based semiconductor.

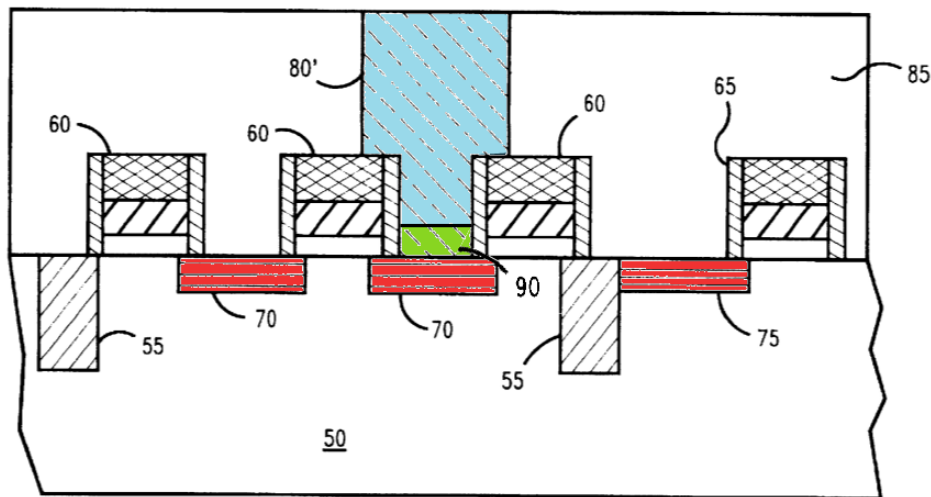


FIG. 4

(Ex.1128, Fig. 4 (annotated and modified).)

The **quantum conductive barrier layer 90** incorporated in Bronner's transistor is an oxide of silicon that has a thickness of less than about 1nm. Jammy discloses numerous compounds that can be used for forming the quantum conductive barrier layer, including *silicon oxynitride* or *alumina*. (Ex.1101, 3:1-4, 51-57.) Either

silicon oxynitride or *alumina* forms an interface layer comprising a passivation layer that is an oxide of silicon. (Ex.1022, ¶¶203-215.)

(1) “*oxide of the silicon*”: *silicon oxynitride*

Jammy discloses that “[p]referred quantum conductive barrier materials are . . . *silicon oxynitride*.” (Ex.1101, 3:1-2, 3:51-53.) A POSITA would understand that silicon oxynitride (SiON) is an “oxide of silicon.” (Ex.1022, ¶204.) Jammy discloses another layer that is also an “oxide of silicon.” (*Id.*) Jammy mentions that when “an oxynitride quantum conductive layer is desired, the . . . nitrogen reaction process may be conducted with a substrate having a *pre-existing very thin oxide layer*.” (Ex.1101, 5:41-43.) Because Jammy discloses using a silicon substrate, (*id.*, 4:33-36), the oxide layer will be an oxide of silicon. The pre-existing oxide layer together with the SiON layer will also be an interface layer comprising a passivation layer that is an “oxide of silicon.” (Ex.1022, ¶204.)

(2) “*oxide of silicon*”: *oxide of silicon layer formed during alumina (Al₂O₃) deposition*

Jammy discloses that “other ceramic materials, such as, for example, *alumina [Al₂O₃] . . . may be used*” as quantum conductive materials. (Ex.1101, 3:55-57). In a Final Written Decision for a petition involving U.S. Patent No. 9,209,261, a patent that shares the same specification with the ’880 Patent, the Board noted that “we agree with the Petitioner [i.e., Samsung] that Jammy discloses an embodiment in

which a *silicon oxide layer exists on the semiconductor surface between the alumina oxide and the source/drain regions of the semiconductor.*” (Ex.1116, 31.)

Jammy teaches “forming a quantum conductive layer on the exposed surface,” (Ex.1101, 4:64-65), of a semiconductor substrate, which can be a silicon substrate. (*Id.*, 4:33-36.) The fabrication method includes the step of cleaning the exposed silicon surface of the source/drain diffusions using an HF (hydrofluoric acid) solution (Ex.1101, 4:61-67, Ex.1022, ¶205.) Jammy also mentions that “the quantum conductive layer can be formed by chemical vapor deposition [CVD].” (*Id.*, 6:1-3.)

A POSITA would have been aware, before the alleged priority date of the claims of the '880 Patent, of the processes employed to form a layer of alumina on the exposed surface of silicon substrate using CVD. (Ex.1022, ¶206.) As Dr. Schubert explains, multiple contemporary technical articles in analogous art disclose forming an alumina layer on a silicon surface using CVD. (*Id.*) A POSITA would know that the deposition of alumina using CVD on a silicon substrate results in formation of a thin layer of silicon oxide directly on the substrate below the alumina layer. (*Id.*)

One such reference is 2002-Stesmans, published in early 2002, that analyzes ultrathin layers of alumina on silicon substrate. (Ex.1103, 1957; Ex.1022, ¶207.) 2002-Stesmans discloses that “ultrathin layers of Al_2O_3 (~0.5-3 nm) . . . as well as ultrathin SiO_x layer, were deposited at 300° C in an atomic-layer chemical-vapor-

deposition (ALCVD) reactor using $\text{Al}(\text{CH}_3)_3$ and H_2O . . . as precursors . . . at a pressure of ~ 1 Torr.” (*Id.*, 1957.) 2002-Stesmans notes that a thin interfacial layer of SiO_x is formed between the silicon and Al_2O_3 (alumina) interface. (Ex.1103, 1959.) In the ALCVD process, such as the one employed by Stesmans, the oxygen precursor H_2O is introduced at the initial stages of the growth process without simultaneous introduction of the aluminum precursor $\text{Al}(\text{CH}_3)_3$. (Ex.1022, ¶207.) As a result, oxygen reacts with the exposed surface of silicon substrate and forms a thin interfacial layer of SiO_x . (*Id.*) According to Dr. Schubert, a silicon atom does not bond well with an aluminum atom, but silicon and aluminum atoms bond easily with oxygen atoms. (*Id.*) Thus, the oxygen atoms facilitate formation of Al_2O_3 (alumina) layer on a silicon interface by forming a thin interfacial layer of SiO_x . (*Id.*) 2002-Stesmans recommends using a layer of SiO_x with a thickness of about 0.5 nm (5 Å) or more, (Ex.1103, 1959), and discloses forming alumina layers in in range of ~ 0.5 to 3 nm (5 Å to 30 Å). (*Id.*, 1957; Ex.1022, ¶207.) Thus, 2002-Stesmans teaches a POSITA how to form an interface layer comprising an “oxide of silicon” where the oxide layer is about 5 Å thick and the alumina layer that is also about 5 Å. The thickness of the resulting stack will be around 10 Å, which is within the most preferred range of 5-15 Å disclosed by Jammy. (Ex.1022, ¶207.)

In light of the disclosure of 2002-Stesmans, a POSITA would also have appreciated the benefits of having a silicon-oxide layer below the alumina layer.

(Ex.1022, ¶208.) Citing 1999-Lucovsky (Ex.1108), 2002-Stesmans underscores “the necessity for interposing an ultrathin SiO₂ layer between the Si substrate and high-κ oxides (Al₂O₃, Ta₂O₅, TiO₂) to attain device grade interfaces.” (Ex.1103, 1959; *see also* Ex.1108, 1806.) As Dr. Schubert explains, several additional technical articles published in 2001 and 2002 also disclose that deposition of thin alumina (Al₂O₃) films on a silicon substrate using CVD or similar processes results in an ultrathin silicon oxide layer on the silicon substrate below the alumina layer. (Ex.1022, ¶¶209-211; *see also* Ex.1110 (2002-Groner), Ex.1111 (2002-Tsai), Ex.1112 (1975-Raider); Ex.1113 (1997-Cerofolini), Ex.1114 (1983-Mende).)

(3) “thickness of less than about 1 nm”

Jammy renders obvious the interface layer comprising a passivation layer “having a thickness of less than about 1 nm.” (Ex.1022, ¶212.) Jammy discloses that “[t]he quantum conductive layer preferably has a thickness of about 50 Å [5 nm] or less, more preferably about 5-30 Å [0.5-3 nm], **most preferably about 5-15 Å** [0.5-1.5 nm].” (Ex.1101, 3:35-37.) Thus, the claimed range overlaps with the range disclosed in Jammy—especially, there is a significant overlap between the claimed range (i.e., less than about 1 nm) and the **most preferred** range in Jammy (i.e., 0.5-1.5 nm). (*Id.*)

The Federal Circuit has consistently held that “even a slight overlap in range established a *prima facie* case of obviousness.” *Genentech, Inc. v. Hospira, Inc.*, 946

F.3d 1333, 1341 (Fed. Cir. 2020). In *Genentech*, claims to a chemical process operating in a range of temperature below room temperature, “from about 10 °C to about 18 °C” were found to be obvious over a prior art process operating at room temperature, in a range from 18-25 °C.” (*Id.* at 1337-38, 1341 (Newman, J., dissenting) (citation omitted).) In other words, the overlap at a single number, 18 °C, rendered the patent invalid. *See also* MPEP 2144.05. Moreover, the claim requires that the thickness is ***less than about 1 nm***. The Federal Circuit noted that the term “about” “is a descriptive term commonly used in patent claims to avoid a strict numerical boundary to the specified parameter.” *Ecolab, Inc. v. Envirochem, Inc.*, 264 F.3d 1358, 1367 (Fed. Cir. 2001) (quotations and citation omitted). To the extent the thickness of the passivation layer is more than 1 nm, the overlap between the claimed range and the quantum conductive layer in Jammy would be even greater. (Ex.1022, ¶212.)

Though Claim 23 requires an interface layer comprising a passivation layer that is an oxide of silicon having thickness of less than about 1 nm, the '880 Patent discloses that such an interface layer can have a broad range of thickness. (Ex.1022, ¶213.) According to the '880 Patent, the thickness of an interface layer that includes a passivation layer can be “between approximately 0.1 nm [1 Å] to about 5 nm [50 Å].” (Ex.1001, 10:28-29.) The '880 Patent further mentions that depending upon the implementation, the thickness can be less than 1nm [10 Å], less than 0.5 nm [5 Å]

or less than 0.2 nm [2 Å]. (Ex.1001, 10:30-32.) The '880 Patent does not mention that the inventors discovered any unexpected properties of the passivation layer when the thickness is less than about 1 nm or any reason why the claimed range is “special or critical” to the invention. (Ex.1022, ¶214; *Genentech*, 946 F.3d at 1341.) Passivation layers of thickness less than 1 nm are merely embodiments of the broader range that varies from approximately 0.1 nm to about 5 nm. (Ex.1022, ¶214.) A POSITA would have been motivated to retain the thickness of the **quantum conductive layer** disclosed in Jammy (i.e., the interface layer) to 5-15 Å [0.5-1.5 nm] because Jammy explicitly identifies this range as the ***most preferred*** range. (Ex.1101, 3:36-38; Ex.1022, ¶215.) A POSITA would recognize that the thickness of the quantum conductive layer is a process parameter that affects the result, and is “result-effective.” (*Genentech*, 946 F.3d at 1341; Ex.1022, ¶215). Jammy mentions that the materials employed as quantum conductive layers would “in their bulk properties would be considered dielectrics (i.e., electrical insulators)” but “[i]n very thin layers, . . . these materials become electrically conductive.” (Ex.1101, 1:23-27). A POSITA would be motivated to keep the thickness of the layer in the ***most preferred range*** where the layer is “electrically conductive.” (Ex.1022, ¶215.) As Jammy warns, thicker layers may act like “dielectrics (i.e., electrical insulators)” and increase the overall resistance of the MOSFET 40 disclosed in Jammy. (*Id.*) A

POSITA would know that higher resistance in a transistor is an undesirable outcome.

(*Id.*)

2. Claim 24

a) The electrical junction of claim 23,

Jammy discloses the electrical junction of claim 23, as discussed in **Section XIII.C.1** above.

b) wherein the interface layer further includes a separation layer between the contact metal and the passivation layer.

Jammy discloses this element. Jammy discloses that *alumina* [Al_2O_3] may be used as quantum *conductive* materials. (Ex.1101, 3:55-57). As discussed in **Section XIII.C.1.e).(2)** above, when deposited on a silicon-based semiconductor substrate, the *alumina* layer includes an upper layer of alumina and a lower layer of oxide of silicon. (*See also* Ex.1116, 31.) The lower layer of oxide of silicon forms the passivation layer and the upper layer of alumina forms the separation layer, and the upper layer of alumina is between the contact metal and the passivation layer.

3. Claim 25

a) The electrical junction of claim 24,

Jammy discloses the electrical junction of claim 24, as discussed in **Section XIII.C.2.**

- b) wherein the interface layer has a thickness of less than 5 nm.

Jammy discloses this element. Jammy discloses that “[t]he quantum conductive layer preferably has a thickness of *about 50 Å [5 nm] or less, . . . most preferably about 5-15 Å [0.5-1.5 nm]*.” (Ex.1101, 3:35-37.) Thus, the quantum conductive layer is the interface layer with a thickness of less than 5 nm. *See also* Section XIII.C.1.e).(3).

XIV. THE DISCRETIONARY FACTORS

Petitioners will address discretionary factors per the guidelines provided by the Board. *See* Acting USPTO Director Coke Morgan Stewart, Memorandum, “Interim Processes for PTAB Workload Management” at 2 (Mar. 26, 2025).

XV. CONCLUSION

Petitioners request that the Board institute *inter partes* review, hold the Challenged Claims unpatentable, and cancel them.

Date: June 11, 2025

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,937,880 contains, as measured by the word-processing system used to prepare this paper, 13,905 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Date: June 11, 2025

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CERTIFICATE OF SERVICE

I hereby certify that on June 11, 2025, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,937,880, together with its supporting exhibits, and Power of Attorney was served by Federal Express, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record as listed on PAIR:

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