

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

JinkoSolar Co., Ltd.,
Petitioner,

v.

First Solar, Inc.,
Patent Owner.

Case No. IPR2025-01130
Patent No. 9,130,074

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,130,074**

LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 9,130,074
1002	File History for U.S. Patent No. 9,130,074
1003	Declaration of Dr. Miltiadis Hatalis
1004	Certified Translation of Japanese Patent Application Publication No. JP1992245683 (“Tamura”)
1005	Japanese Patent Application Publication No. JP1992245683
1006	Polysilicon Tunnel Junctions as Alternates to Diffused Junctions (“Borden”)
1007	U.S. Patent Application US 2010/0240172 (“Rana”)
1008	U.S. Patent No. 5,057,439 (“Swanson”)
1009	J.Y. Gan and R.M. Swanson, <i>Polysilicon Emitters for Silicon Concentrator Solar Cells</i> , Stanford Univ. (“Gan”)
1010	Young J. Kwark et al., <i>SIPOS Heterojunction Contacts to Silicon</i> , Stanford Elec. Lab., IEDM 742 (1984) (“Kwark”)
1011	Blank
1012	An Investigation of The Thermal Stability of The Interfacial Oxide in Polycrystalline Silicon Emitter Bipolar Transistors by Comparing Device Results with High-Resolution Electron Microscopy Observations (“Wolstenholme”)
1013	Structure and Morphology of Polycrystalline Silicon-Single Crystal Silicon Interfaces (“Bravman”)
1014	The Optical Properties of Metallic Aluminum, in <i>Handbook of Optical Constants of Solids</i> (Palik, ed., 1985) (“Smith”)
1015	Amorphous/Crystalline Silicon Heterojunction Solar Cells with Intrinsic Buffer Layer (“Froitzheim”)
1016	Antireflective coating for ITO films deposited on glass substrate (“Chiou”)
1017	An Approach for the Higher Efficiency in the HIT Cells (“Taguchi”)
1018	A high efficiency thin film silicon solar cell and module (“Yamamoto”)
1019	Photovoltaic Technology: The Case for Thin-Film Solar Cells (“Shah”)
1020	Semiconductor Material and Device Characterization, Third Edition (“Schroder”)
1021	Amorphous Hydrogenated Silicon, a-Si:H (“Fuhs”)

Exhibit	Description
1022	Large Grain Polycrystalline Silicon by Low-Temperature Annealing of Low-Pressure Chemical Vapor Deposited Amorphous Silicon Films (“Hatalis”)
1023	Crystalline Silicon Solar Cell, in Clean Electricity From Photovoltaics (Archer, ed., 2001) (“Green”)
1024	Solar Energy Conversion, 2d ed. (Neville, ed., 2001) (“Neville”)
1025	Semiconductor Materials and Modelling, in <i>Practical Handbook of Photovoltaics: Fundamentals and Applications</i> (Markvart, ed., 2003) (“Markvart”)
1026	High Efficient Concentrator Silicon Solar Cells, in <i>Practical Handbook of Photovoltaics: Fundamentals and Applications</i> (Markvart, ed., 2003) (“Verlinden”)
1027	Silicon for Photovoltaics, in Silicon (Siffert, ed., 2003) (“Muller”)
1028	Surface passivation Layers for Multicrystalline Silicon Solar Cells (“Ponce”)

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I. INTRODUCTION

JinkoSolar Co., Ltd. (“Petitioner”) petitions for *inter partes* review seeking cancellation of claims 1-8 of U.S. Patent No. 9,130,074 (Ex-1001, “’074 patent”), assigned to First Solar, Inc. (“Patent Owner”).

The ’074 patent describes allegedly “improved manufacturing methods” for creating “solar cells which attain high operational efficiency, and which can be manufactured in a cost effective manner.” Ex-1001, 1:40-42. The ’074 patent’s manufacturing methods include “single-side CVD [chemical vapor deposition] deposition processes and thermal treatment for layer formation and/or conversion.” Ex-1001, 1:54-57. As demonstrated below, every element of the eight process claims in the ’074 patent was well known in the prior art. The prior art discloses use of CVD in the fabrication of solar cells, as well as thermal treatment of layers in the production of solar cells (and other semiconductor devices). The solar cells manufactured by the ’074 patent’s claimed method have a quite conventional “structure composed of a central substrate, conductive layer(s), antireflection layer(s), passivation layer(s), and/or electrode(s).” Ex-1001, 1:49-51. Moreover, the solar cells include an amorphous interface passivation layer and a separate conductive and passivating layer, both of which the ’074 patent describes may be made from a material such as amorphous silicon or silicon oxide.

In prosecution, the only element of Claim 1 the Examiner found to be missing from the prior art was the limitation “providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof.” Ex-1002, 485. In reality, this metallization element was wholly conventional. For example, Tamura discloses “the formation of electrodes...can be performed as in the same manner as in a typical solar cell.” Tamura [0012]. Borden also discloses “Grids” or “Front Contact,” depicted in Figures 2 and 3 as electrodes formed by metallization. Borden, FIGs. 2-3. Similarly, Rana discloses that metallization “may be included to provide the front and rear contacts for a solar cell.” Rana, [0045].

The methods claimed in the '074 patent were not novel, or at minimum would have been obvious to a POSITA at the time of the invention. The challenged claims should be cancelled.

II. STANDING, MANDATORY NOTICES AND FEE AUTHORIZATION

A. Grounds for Standing:

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '704 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the '704 patent on the grounds set forth in this Petition.

B. Real Party-in-Interest:

Petitioner certifies that the real parties-in-interest of this Petition are JinkoSolar

Holding Co., Ltd., JinkoSolar (Vietnam) Industries Co. Ltd., Jinko Solar Technology Sdn. Bhd., Zhejiang Jinko Solar Co., Ltd., JinkoSolar (U.S.) Holding Inc., JinkoSolar (U.S.) Inc., Jinko Solar (U.S.) Manufacturing Inc., and Jinko Solar (U.S.) Industries Inc.

C. Related Matters:

Patent Owner has asserted the '704 patent in litigation against Petitioner and the real parties-in-interest in *First Solar, Inc. v. JinkoSolar Holding Co., Ltd. et al.*, Case No. 1-25-cv-00223 (D. Del.) (filed in February, 25, 2025).

D. Lead and Back-Up Counsel:

Petitioner designates the following counsel:

Lead Counsel	Back-Up Counsel
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Pursuant to 37 C.F.R. § 42.10 (b), Petitioners have filed a power of attorney with the above designation of counsel.

E. Service Information:

Service information is provided in the designation of counsel above. Petitioner consents to electronic service at the email addresses listed above and at Jinko-FirstSolar-IPR@cov.com.

F. Fee Authorization:

The Patent Trial and Appeal Board is authorized to charge fees associated with this Petition, including any fees for filing, institution, and post-institution proceedings under 37 C.F.R. § 42.15, as well as any additional fees that might be due, to Deposit Account No. 60-3160.

III. SUMMARY OF CHALLENGE

Petitioner requests *inter partes* review of claims 1–8 of the '704 patent under 35 U.S.C. §§ 102 and 103 based on the following grounds:

Ground I: Claims 1-8 are anticipated or rendered obvious over Tamura.

Ground II: Claims 1-2 and 4-8 are anticipated or rendered obvious over Borden.

Ground III: Claims 3-4 are rendered obvious over the combination of Borden and Gan, Kwark, or Swanson.

Ground IV: Claims 1-8 are anticipated or rendered obvious over Rana.

The earliest claimed priority date of the '704 patent is April 21, 2009. Each of the asserted references is available as prior art under 35 U.S.C. § 102 (pre-AIA)¹, as shown in the following table.

Exhibit	Reference	Date(s)	Availability as Prior Art
1004	Certified Translation of Japanese Patent Application Publication No. JP1992245683 (“Tamura”)	September 2, 1992 (published)	§§ 102(a) and (b)
1006	Polysilicon Tunnel Junctions as Alternates to Diffused Junctions (“Borden”)	September, 2009 (published)	§ 102 (a)
1007	U.S. Patent Application US 2010/0240172 (“Rana”)	September 19, 2008 (claimed priority to a provisional application filed on)	§ 102 (e)
1008	U.S. Patent No. 5,057,439 (“Swanson”)	October 15, 1991 (issued)	§§ 102 (a) and (b)
1009	Polysilicon Emitters for Silicon Concentrator Solar Cells (“Gan”)	1990 (published)	§§ 102 (a) and (b)
1010	SIPOS Heterojunction Contacts to Silicon (“Kwark”)	1984 (published)	§§ 102 (a) and (b)

IV. OVERVIEW OF U.S. PATENT NO. 9,130,074

A. Summary

The '074 patent, entitled “High-efficiency Solar Cell Structure and Methods of

¹ Because the application for the '704 patent was filed prior to March 16, 2013, the pre-AIA conditions for patentability apply.

Manufacture”, discloses “improved solar cell structures and methods of their manufacture for increased cell efficiency.” Ex-1001, 1:20-23; Ex-1003, ¶39. A stated object of the ’074 patent is disclosing “improved manufacturing methods including single-side CVD deposition processes and thermal treatment for layer formation and/or conversion.” Ex-1001, 1:54-57; Ex-1003, ¶40.

The ’074 patent describes a method of manufacturing a solar cell with the structure shown in Figure 6. Ex-1001, 2:56-57; Ex-1003, ¶41. Figure 6 depicts a solar cell structure containing a “p-type wafer 65,” “[e]lectrically passivating interface layer” 64 and 66, “transparent and conductive film” layers 63 and 67, “transparent and conductive film” layers 62 and 68, “front metal electrode” 61, and “back metal electrode” 69. Ex-1001, 5:14-6:25, FIG. 6; Ex-1003, ¶41.

The patent identifies several materials for “electrically passivating interface layer[s],” including “silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, [and] titanium nitride.” Ex-1001, 5:58-61, 6:1-4; Ex-1003, ¶42. The ’074 patent similarly identifies several materials for an “electrically passivating and conductive film,” including “amorphous or polycrystalline silicon carbides,” “amorphous or polycrystalline silicon,” and “amorphous or poly-crystalline diamond-like-carbon.” Ex-1001, 5:45-53, 6:8-15; Ex-1003, ¶43.

For use in the “transparent and conductive film 62” on the front side and the

“transparent and conductive film 68” on the back side, the ’074 patent discloses a variety of materials, including different types of “transparent conductive oxides.” Ex-1001, FIG. 6; 5:37-41, 6:2-24; Ex-1003, ¶44.

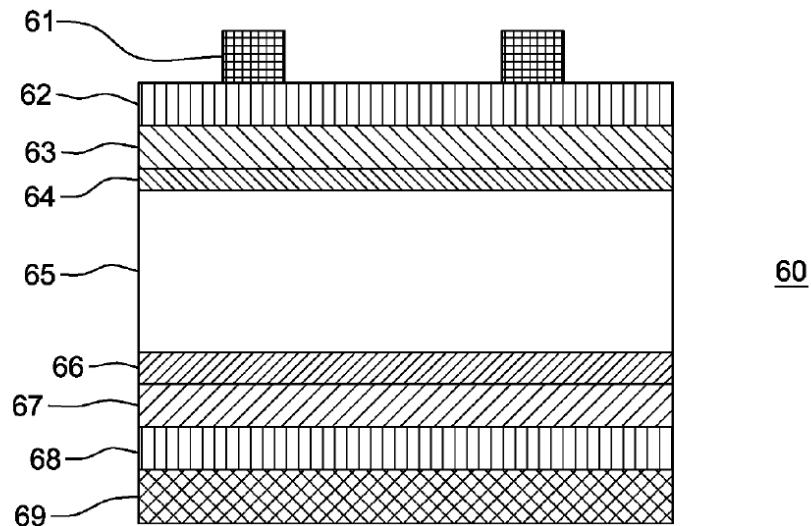


FIG. 6

Ex-1001, FIG. 6.

The ’074 patent includes eight claims: independent claim 1 and seven dependent claims (claims 2–8), as shown in Appendix A.

B. Level of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the alleged invention of the ’704 patent would have had a bachelor’s degree in material science, material engineering, physics, electrical engineering, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating

solar cells or solar module systems. Ex-1003, ¶¶47-49. A person with less formal education but additional relevant practical experience, or vice versa, would also qualify as a person of ordinary skill in the art. Ex-1003, ¶¶47-49.

C. Claim Construction

In IPR proceedings, claims are construed “in accordance with their ordinary and customary meaning.” 37 C.F.R. § 42.100(b); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). Petitioner does not believe that any specialized constructions are necessary at this stage of the proceeding. Ex-1003, ¶50.

V. OVERVIEW OF THE PRIOR ART

The prior art references discussed below—Tamura, Borden, Rana, Swanson, Gan, and Kwark—disclose various features of solar cell modules and techniques for improving key attributes of solar cells such as current collection and mechanical integrity.

A. JP1992245683 (“Tamura”)

Tamura is prior art under pre-AIA 35 U.S.C. §§ 102(a) and (b) because it was published on September 2, 1992, before the priority date of the ’074 patent. Tamura was not cited or discussed during the prosecution of the ’074 patent.

Tamura discloses “a method for manufacturing a solar cell in which a pn junction of the solar cell is formed by solid phase epitaxy,” as depicted in Figures 2 and 3 (below). Ex-1004, [0001]; Ex-1003, ¶52.

FIG. 2¶

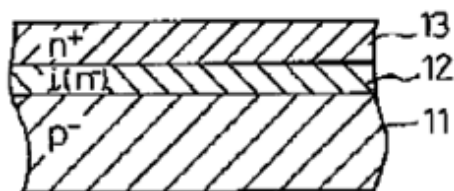
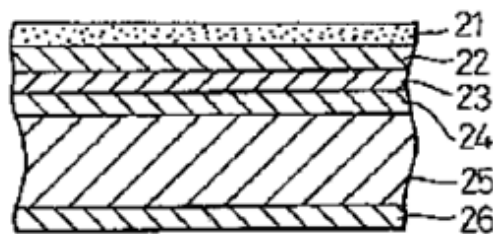


FIG. 3¶



Ex-1004, FIGs. 2 and 3.

Figure 2 of Tamura discloses a solar cell structure with a “p- type silicon substrate 11” that was placed in a deposition device where an “undoped amorphous silicon layer 12” was deposited on top of the substrate 11, and “a high-concentration n+ type amorphous silicon layer 13” was deposited on the layer 12. *See* Ex-1004, [0015]; Ex-1003, ¶52.

Tamura also discloses a heating treatment “maintained at 600°C for 5 minutes.” Ex-1004, [0016]; Ex-1003, ¶¶53-54. The solar cell structure after the heating process is depicted in Figure. 3. *See* Ex-1004, [0018]; Ex-1003, ¶55.

B. “Polysilicon Tunnel Junctions as Alternates to Diffused Junctions” (“Borden”)

Borden is prior art under pre-AIA 35 U.S.C. § 102(a) because it was published in September 2008, more than one year before the priority date of the '074 patent. Borden was not cited or discussed during the prosecution of the '074 patent.

Borden discloses the “use of heavily doped polysilicon combined with a tunnel

dielectric to provide an alternate to diffused junctions for silicon solar cells.” Ex-1006, Abstract, Ex-1003, ¶58. Figure 2 of Borden depicts a resulting solar cell structure with an n-type CZ wafer as a central substrate, a tunnel insulator, a poly (P doped) layer, and an AR (nitride or ITO) layer, a n-type substrate, a diffused BSF layer and a Poly (Phos doped) layer, and an Aluminum, as shown in Figure 2. *See* Ex-1006, §§ 2, 3; Ex-1003, ¶60.

Figure 3 of Borden depicts the corresponding process flow to make the solar cell structure as shown in Figure 2. Ex-1006 § 3, FIG. 3; Ex-1003, ¶61.

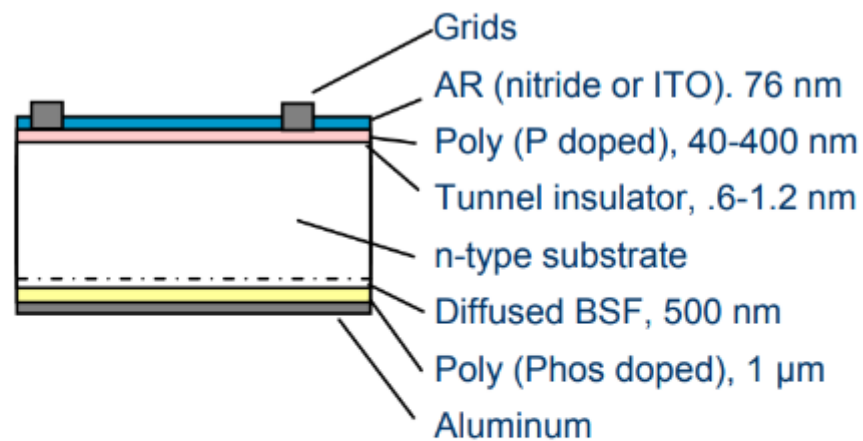
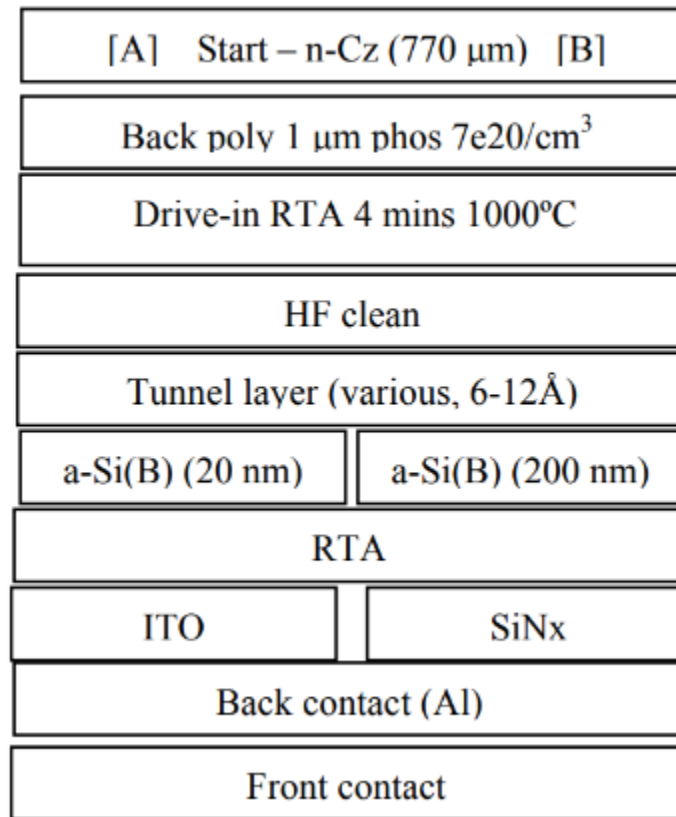


Figure 2: Device structure and process flow. A) with diffused BSF (formed by diffusion during Rapid Thermal Anneal (RTA) of phosphorous doped poly) on n-type Si.

Ex-1006, FIG. 2.

Figure 3: Process flow.



Ex-1006, FIG. 3.

C. U.S. Patent Application US 2010/0240172 (“Rana”)

Rana is prior art under pre-AIA 35 U.S.C. § 102(e) because it claims priority to Provisional Application No. 61/098,713, filed on September 19, 2008, before the earliest claimed priority date of the '074 patent. Rana was not cited or discussed during the prosecution of the '074 patent.

Rana relates to “silicon solar cells and, more particularly, to a method for obtaining a desired dopant profile in the emitter of a solar cell device.” Ex-1007, [0002]; Ex-1003, ¶64.

Rana discloses a method for forming an emitter in a crystalline silicon substrate by depositing a first lightly doped layer of amorphous silicon on the surface of the substrate. *See* Ex-1007, [0009]; Ex-1003, ¶65. Then, “subsequent to the deposition of the lightly doped amorphous silicon layer, a heavily doped phosphorous amorphous silicon layer is applied over the lightly doped region, as illustrated at step 14” of Figure 1 (below). Ex-1007, [0027].

This heavily doped amorphous silicon layer then undergoes “a thermal treatment that generates a selectively heavily doped surface region.” Ex-1007, [0009]; Ex-1003, ¶67.

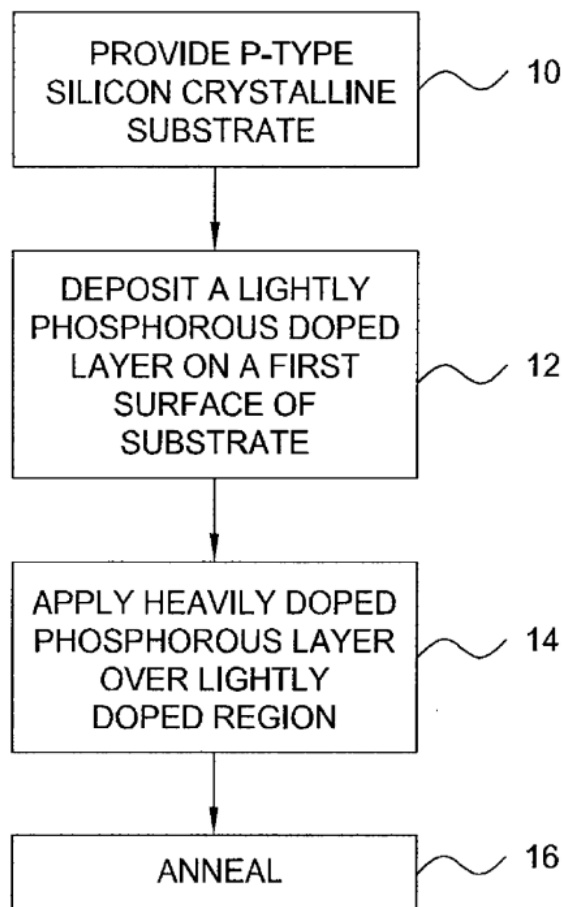


FIG. 1

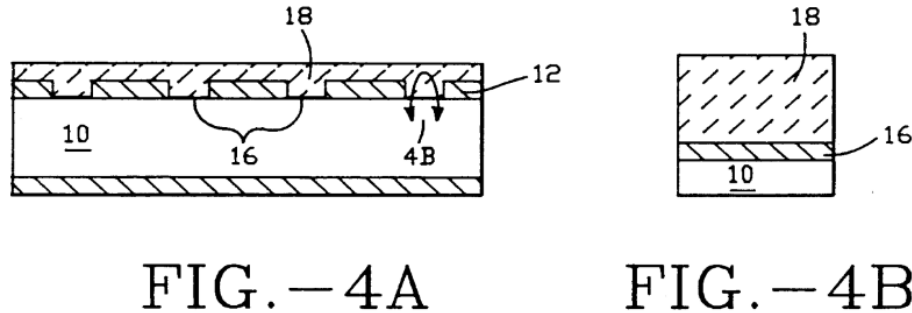
Ex-1007, FIG. 1.

D. U.S. Patent No. 5,057,439 (“Swanson”)

Swanson is prior art under pre-AIA 35 U.S.C. §§ 102(a) and (b) because it issued as a patent on October 15, 1991, before the earliest claimed priority date of the '074 patent. Swanson was not cited or discussed during the prosecution of the '074 patent. Ex-1003, ¶68.

Swanson discloses “an improved method of fabricating polysilicon emitters in

semiconductor devices such as silicon solar cells.” Ex-1008, 1:6-9; Ex-1003, ¶69. In particular, Swanson Figures 4A-4B disclose a solar cell structure with an “interfacial oxide 16” layer on top of a silicon substrate 10. *See* Ex-1008, FIGs 4A-4B, 2:43-60; Ex-1003, ¶70.



Ex-1008, FIGs. 4A and 4B.

Swanson Figures. 5A-5B further disclose a thermal treatment over 500°C results in perforation of the “interfacial oxide 16” to allow carrier transport therethrough. Ex-1008, FIGs. 5A-5B, 2:61- 3:3; Ex-1003, ¶71.

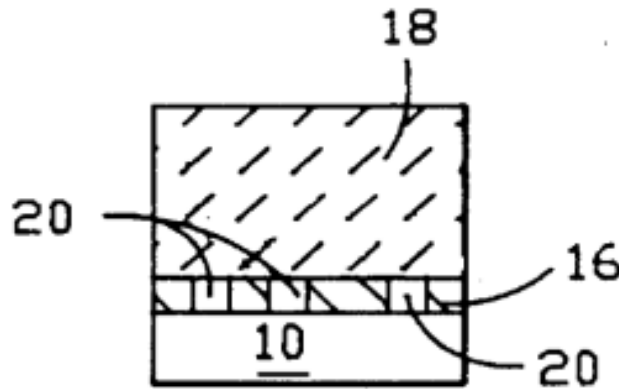


FIG.—5B

Ex-1008, FIG. 5B.

E. Polysilicon Emitters for Silicon Concentrator Solar Cells (“Gan”)

Gan is prior art under pre-AIA 35 U.S.C. §§ 102(a) and (b) because it was published in 1990, before the priority date of the '074 patent. Gan was not cited or discussed during the prosecution of the '074 patent.

Gan discloses a “polysilicon emitter with a thermally grown interfacial oxide” between a substrate and a polysilicon layer. Ex-1009, Abstract. Ex-1003, ¶¶73-74.

Gan also discloses that “the oxide is not thermally stable, i.e., it tends to break up during high temperature anneals.” *See* Ex-1009, 245. Gan further discloses that “[a]s the oxide starts to break up, additional conductive channels are created due to the intimate contacts formed between the polysilicon and the substrate in the broken

regions.” Ex-1009, 249, Ex-1003, ¶75.

F. SIPOS Heterojunction Contacts to Silicon (“Kwark”)

Kwark is prior art under pre-AIA 35 U.S.C. §§ 102(a) and (b) because it was published in 1984, before the priority date of the '074 patent. Gan was not cited or discussed during the prosecution of the '074 patent.

Kwark discloses the use of lower oxygen content Semi-Insulating Polycrystalline Silicon (SIPOS²) films whose lower bulk resistivities would allow utilization of these films in structures such as scaled VLSI bipolar devices and high concentration point contact solar cells where series resistance is detrimental to device performance. Ex-1010, Abstract; Ex-1003, ¶77. Kwark discloses “an interfacial layer between the SIPOS and underlying silicon may play an important, if not dominant, role with the implication that the high oxygen concentrations previously used may not be essential for J_{0e} reduction.” Ex-1010, 742; Ex-1003, ¶78. Kwark Figure 3 further discloses the SIPOS crystallizes during subsequent annealing instead of being crystallized as-deposited. Ex-1010, FIG. 3.

² SIPOS is a material used in the fabrication of high-voltage semiconductor devices.

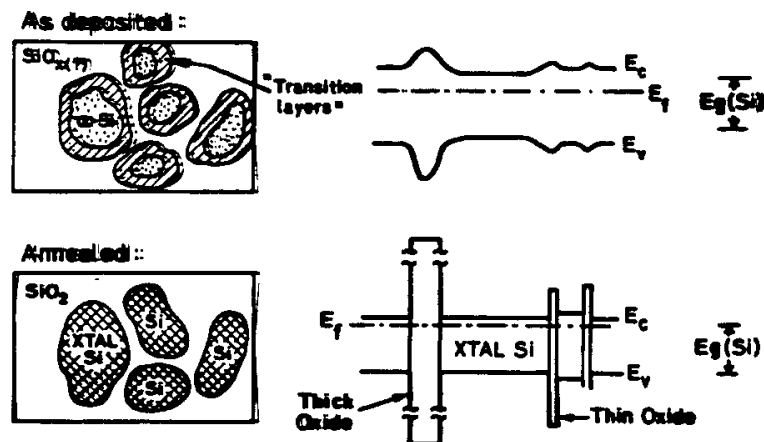


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the “oxide-like” regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Ex-1010, FIG. 3

VI. APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS

A. Ground 1: Claims 1-8 are Anticipated or Rendered Obvious by Tamura

1. Claim 1

a) 1[pre]

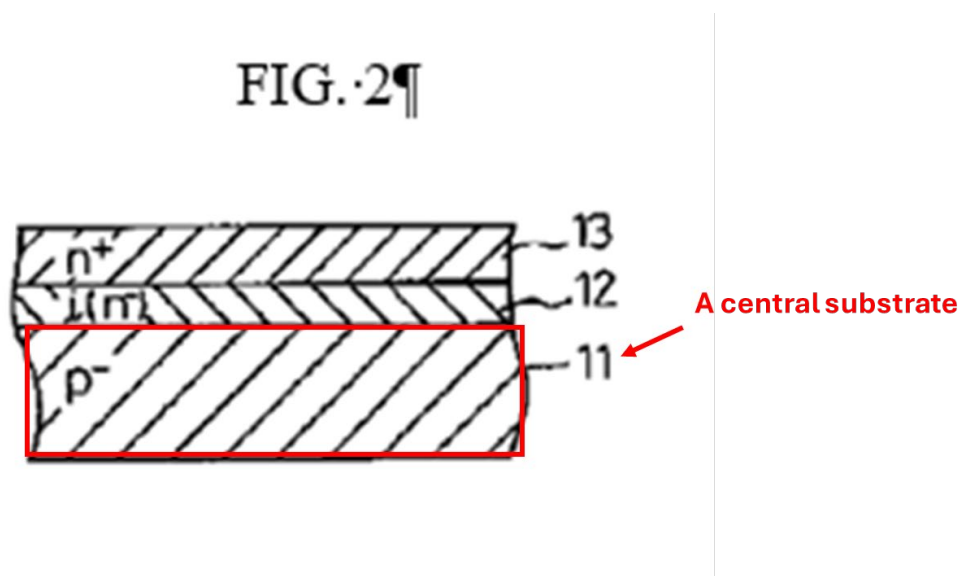
Tamura discloses that “[t]he present invention relates to **a method for manufacturing a solar cell**, and more particularly to **a method for manufacturing a solar cell** in which a pn junction of the solar cell is formed by solid phase epitaxy”.

Ex-1004, [0001]³; Ex-1003, ¶98.

³ All emphases are added, unless otherwise stated.

b) 1[a]

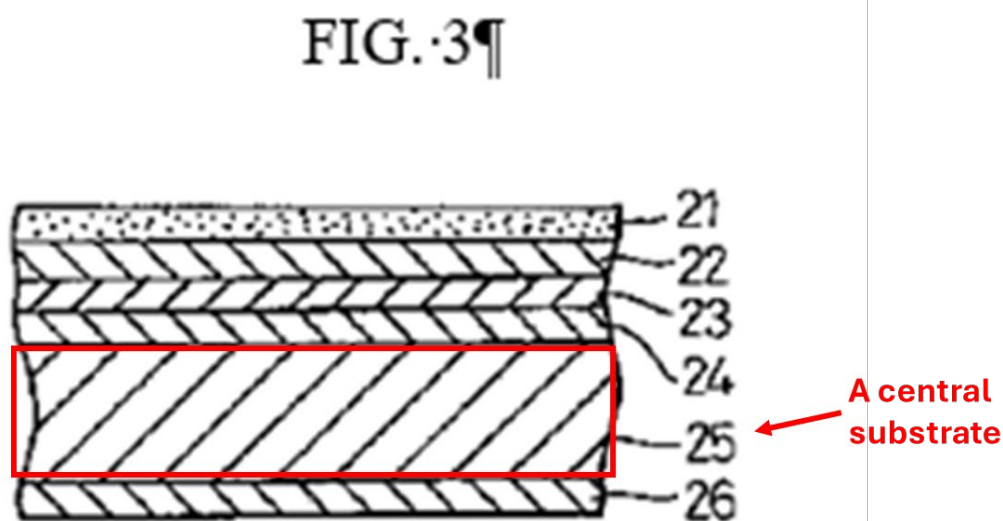
Tamura discloses a “method comprising steps for depositing an undoped amorphous silicon layer **on a substrate** having at least a surface including a first conductivity-type silicon crystal layer” Ex-1004, [0005]. Tamura further discloses that the substrate is a “p-type silicon substrate.” Ex-1004, [0015] (Referring to Figure 2, “This p-type silicon substrate 11 was placed in a deposition device, and an undoped amorphous silicon layer 12 was deposited under the following conditions.”); Ex-1003, ¶100.



Ex-1004, FIG. 2 (annotated).

A POSITA would understand that substrate 11 in FIG. 2 of Tamura is a silicon wafer because Tamura discloses that the silicon substrate is made through either the “Cz” (Czochralski) method, or through the “casting” method. Both were used extensively to manufacture solar cells. Ex-1004, [0014]; Ex-1003, ¶101.

Tamura further discloses that substrate 11, made of a silicon wafer, becomes a *central substrate* in the finished solar cell structure. Ex-1003, ¶102. Figure 3 depicts the p⁻ type crystalline silicon layer 25, which was the starting p-type silicon substrate 11 before the deposition of the various layers, is a *central substrate* with layers above and below it after the completion of the manufacturing process. Ex-1004, [0018] (“In FIG. 3, ... **25 denotes a p⁻ type crystalline silicon layer.**”); Ex-1003, ¶103.



Tamura, FIG. 2 (annotated).

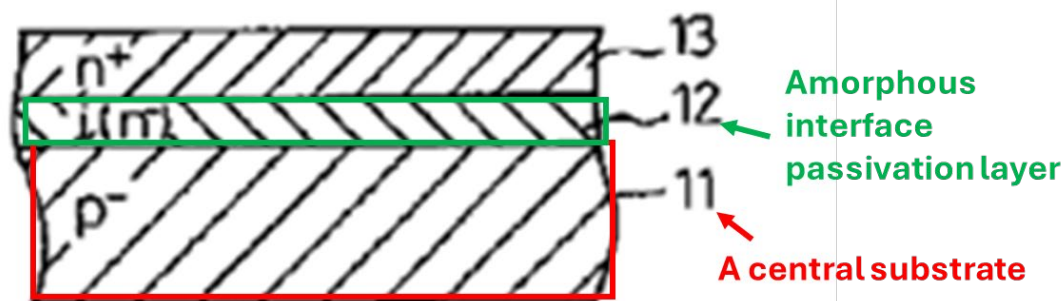
c) 1[b]

The '074 patent does not expressly define “*passivation/passivating.*” Ex-1003, ¶105. It discloses that “**Surface passivation** provides suppression of recombination of electrons and **holes at or in the vicinity of certain physical surfaces** within the solar cell.” Ex-1001, 3:50-52; Ex-1003, ¶105. The '074 patent states that undoped

amorphous silicon is an "example of a surface passivating layer." Ex-1001, 3:57-58; Ex-1003, ¶105.

Tamura discloses depositing "an undoped amorphous silicon layer 12," which comprises *an amorphous interface passivation layer*, over "the silicon substrate 11" (*the substrate*). Ex-1004, [0015] (explaining for Figure 2 that "**p- type silicon substrate 11 was placed in a deposition device, and an undoped amorphous silicon layer 12 was deposited** under the following conditions..."). Tamura further discloses "**heat-treating the undoped and second conductivity-type amorphous layers to convert the layers into crystalline silicon layers...**by solid phase epitaxy." Ex-1004, [0005]; Ex-1003, ¶106. Moreover, Tamura discloses that the "crystal structure of the resulting crystallized film was observed by ultraviolet surface reflection and RHEED (reflection high energy electron diffraction) ..." and that "[t]he results confirmed a crystal film was obtained." Ex-1004, [0017], Ex-1003, ¶106.

FIG. 2¶



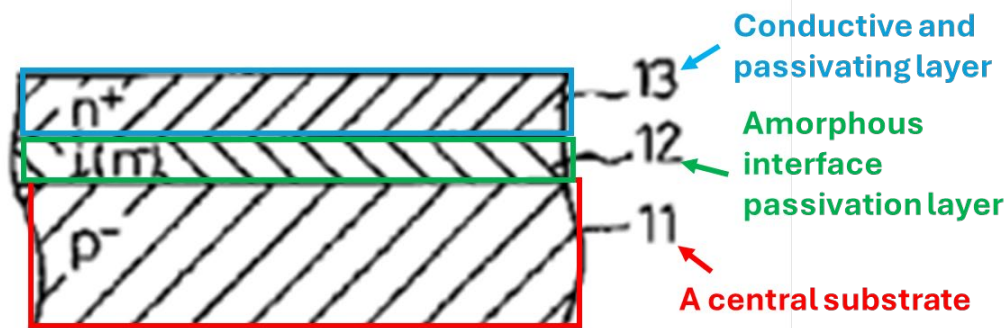
Ex-1004, FIG. 2 (annotated).

Dr. Hatalis opines that a POSITA would understand that the “undoped amorphous silicon layer 12” is a passivation layer because of its known passivation effect on the surface of substrate 11. Ex-1003, ¶¶107-108.

d) 1[c]

Tamura discloses depositing “a high-concentration n^+ type amorphous silicon layer 13,” which comprises *a conductive and passivating layer* on the undoped amorphous silicon layer 12 (*interface passivation layer*) as shown below in Figure 2. See Ex-1004, [0015], [0009]; Ex-1003, ¶110.

FIG. 2



Ex-1004, FIG. 2 (annotated).

A POSITA would understand that the “high-concentration n^+ type amorphous silicon layer 13” is *conductive*. Ex-1003, ¶111. Tamura discloses that “the high-concentration n^+ type amorphous silicon layer 13” comprises a “[d]opant (n-type) PH_3 .” Ex-1004, [0009], [0016] (“a high-concentration n^+ type amorphous silicon layer 13 was deposited...under the following conditions Source gas: SiH_4 gas containing **1%** **PH_3** ”). Dr. Hatalis explains that a POSITA would understand that, during the deposition process, SiH_4 and PH_3 will decompose such that the phosphorus atoms act as an n-type dopant. Ex-1003, ¶111-112.

A POSITA would understand that the “high-concentration n^+ type amorphous silicon layer 13” is *passivating*. Ex-1003, ¶113. See Froitzheim, 183 (“the a-Si:H(n) layer further reduces recombination at the interface due to enhanced band bending

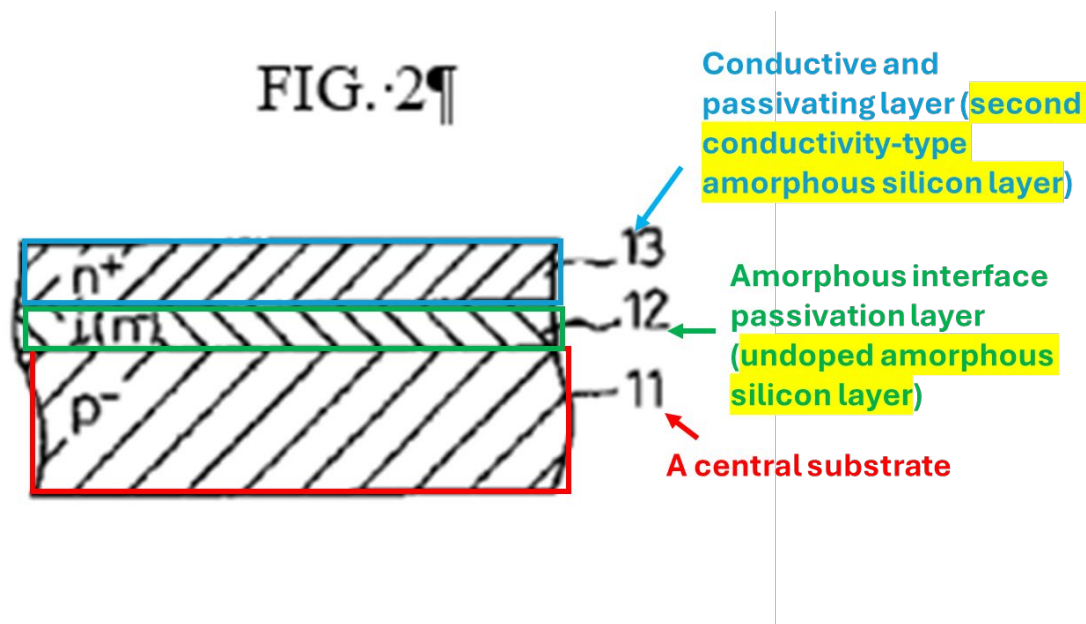
which leads to an additional field passivation”).

e) 1[d]

Tamura discloses that “the deposited undoped [the *interface passivation layer*] and second conductivity-type amorphous silicon [the *conductive and passivating layer*] are crystallized by heat treatment...typically, 600°C to 700°C.” Ex-1004, [0010]; Ex-1003, ¶115. Tamura also discloses *providing a thermal treatment* by heating the substrate 11, and silicon layers 12 and 13 “at **600°C** for 5 minutes.” Ex-1004, [0016]; Ex-1003, ¶115. Thus, Tamura discloses *providing thermal treatment at a temperature of about 500°C or higher*. Ex-1003, ¶115.

Tamura further discloses that *the thermal treatment crystallizes* “high-concentration n⁺ type amorphous silicon layer 13” (also referred to as “the second conductivity-type amorphous silicon layer(s)”), which is *the conductive and passivating layer*. Ex-1004, [0011] (“This heat treatment **crystallizes** the undoped and **second conductivity-type amorphous silicon layers**, forming a pn junction having a graded structure.”) Tamura also discloses that the “crystal structure of the resulting crystallized film was observed by ultraviolet surface reflection and RHEED (reflection high energy electron diffraction” and that the “results confirmed that a **crystal film** was obtained.” Ex-1004, [0017]; Ex-1003, ¶116. A POSITA would understand that the Tamura’s thermal treatment is *crystallizing, at least in part, the at least one conductive and passivating layer* as the deposited amorphous silicon layer 13 (the top

layer in Fig. 2) is confirmed by Tamura's ultraviolet surface reflection and RHEED observations to have become "a crystal film." Ex-1003, ¶116.



Ex-1004, FIG. 2 (annotated).

A POSITA would understand Tamura's disclosure that the thermal treatment *facilitat[es] diffusion of the phosphorus dopant*, introduced by the PH_3 gas during the deposition process, *from the "amorphous silicon layer 13" (at least one conductive and passivating layer) through the "amorphous silicon layer 12" (at least one interface passivation layer)*. Ex-1004, [0012]; Ex-1003, ¶117. Specifically, a POSITA would understand that heating silicon layers 12 and 13 at 600°C for 5 minutes causes the phosphorus dopant atoms to diffuse from layer 13 into layer 12. Ex-1003, ¶117. Dr. Hatalis further explains that Tamura discloses a pn junction having a graded structure formed after the heat treatment, in which a POSITA would understand that the doping

concentration changes gradually from the p region to the n region. Ex-1004, [0011], [0017]-[0018], FIG. 3; Ex-1003, ¶117.

Dr. Hatalis further explains that a POSITA would understand that phosphorus diffuses from the “amorphous silicon layer 13” through the “amorphous silicon layer 12” and the resulting phosphorus concentration gradually changes from 10^{20} cm^{-3} at the surface of the “n⁺ type crystalline silicon layer 23” across the “n⁻ type crystalline silicon layer 24” to 10^{17} to $10^{15} / \text{cm}^3$ of the “p⁻ type substrate 25”. Ex-1003, ¶118; Ex-1004, [0011].

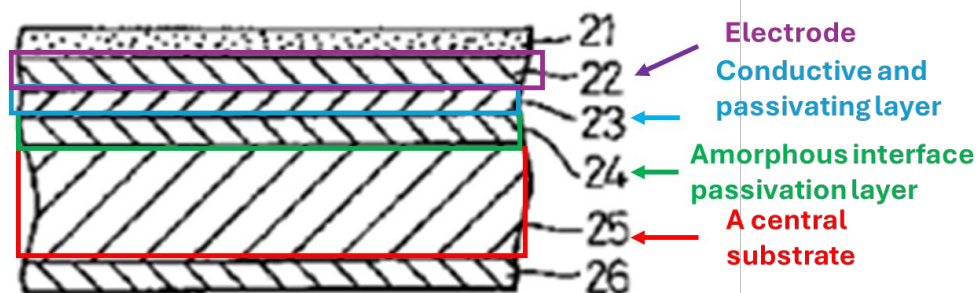
f) 1[e]

Tamura discloses *providing metallization as electrodes* in the solar cell *following the thermal treatment*. Tamura, [0012] (“After the heat treatment for solid phase growth...[t]he formation of electrodes and the like other than the formation of the pn junction can be performed in the same manner as in a typical solar cell.”); Ex-1003, ¶120.

Tamura also discloses a “comb-shaped front surface electrode 22,” which comprises an *electrode in direct contact with* “the n⁺ type crystalline silicon layer 23,” i.e., *at least one conductive and passivating layer*. As shown in FIG. 3, a comb-shaped front surface electrode 22 is directly in contact with the n⁺ type crystalline silicon layer 23 (*at least one conductive and passivating layer*). Ex-1004, [0018], (explaining for Figure 3 that “22 denotes a comb-shaped front surface electrode, 23 denotes an n⁺ type

crystalline silicon layer”); Ex-1003, ¶121.

FIG. 3



Tamura, FIG. 3 (annotated).

g) 1[f]

The '074 patent does not explicitly define “shortened charge carrier flow paths.” Ex-1003, ¶123. Rather, the '074 patent describes the “shortest geometrical” charge carrier flow path as the one that occurs when the “[charge carriers]” transport within the emitter is **vertical instead of mainly lateral.**” Ex-1001, 4:47-50. Such a vertical transport path is formed when using an electrode that has a “full area contact coverage” with the emitter, and the emitter is on the back side of the substrate, as shown in Figure 3. Ex-1001, 4: 47-51; Ex-1003, ¶124.

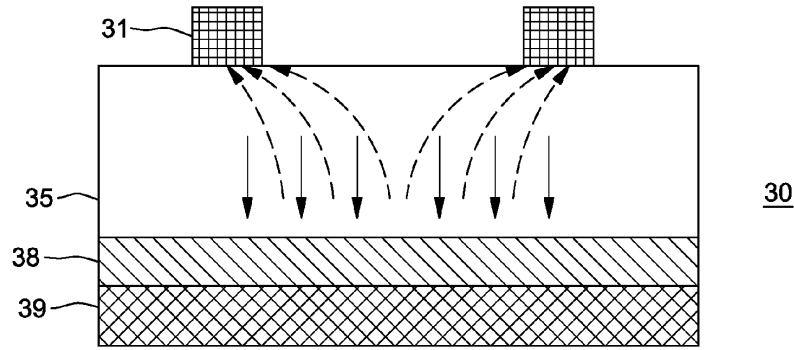


FIG. 3

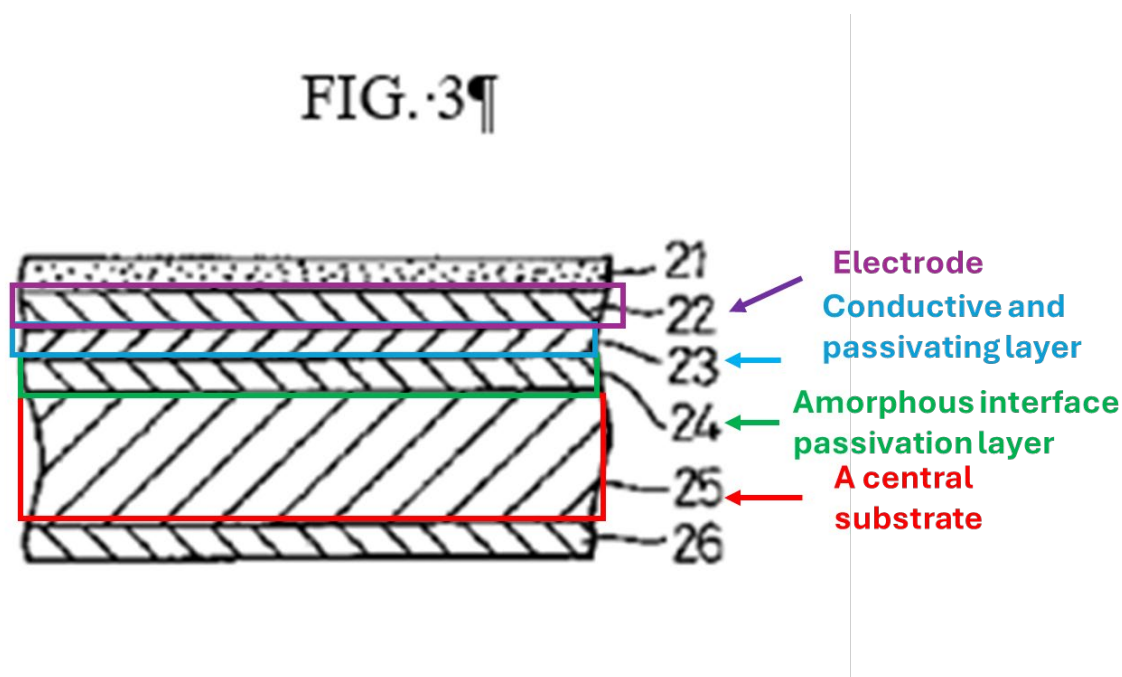
'074 patent, FIG. 3.

Dr. Hatalis explains that a POSITA would understand that the “shortened charge carrier flow paths” can be achieved by reducing the resistance of *the conductive and passivating layer*, which is disclosed by the '074 patent. Ex-1003, ¶¶125-127.

Tamura discloses that a heat treatment forms a pn junction between the p-type crystalline silicon substrate, which is uniformly doped and an n-region that has a graded doping structure and consisting of the crystallized “undoped amorphous silicon layer 12” (*the at least one interface passivation layer*) and “the second conductivity-type amorphous silicon layer 13” (*the at least one conductive and passivating layer*). Ex-1004, [0011] (“This heat treatment crystallizes the undoped and second conductivity-type amorphous silicon layers, forming a pn junction having a graded structure.”); Ex-1003, ¶128.

Tamura further discloses that, after the thermal treatment, *the dopant diffused through interface passivation layer* (“an n⁺ type crystalline silicon layer 24”) in the pn

junction provides shortened charge carrier flow path between the substrate (“a p⁻ type crystalline silicon layer 25”) and the electrodes (“a comb-shaped front surface electrode 22”). Ex-1003, ¶129. Dr. Hatalis explains that a POSITA would understand that the carriers in Tamura that flow between the silicon substrate and the electrodes are the minority carriers, and for these minority carriers to contribute to the current flow, they must reach the metal electrode layer 22. Ex-1003, ¶129.

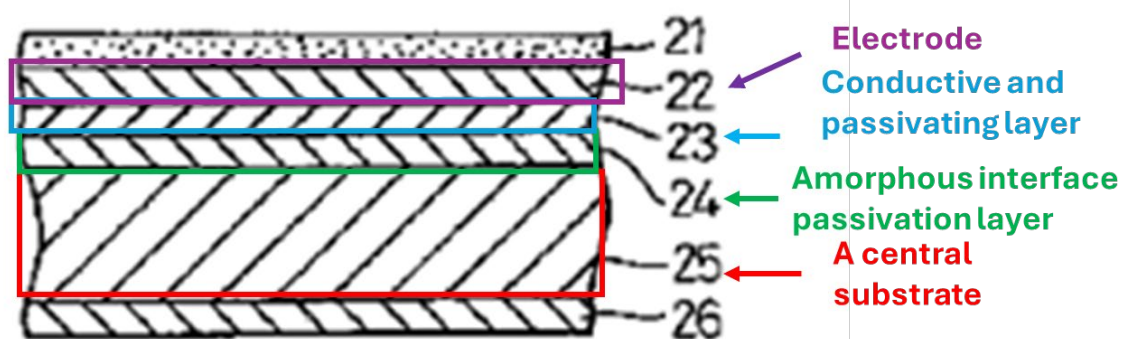


Ex-1004, FIG. 3 (annotated).

A POSITA would understand that, as shown in Tamura Figure 3 and related disclaoure, in a portion of the front or top surface, electrode 22 has a full area contact coverage with the “the n⁺ type crystalline silicon layer 23” (*the conductive and passivating layer*) and layer 23 provides a *shortened charge carrier flow path* (a vertical path) for carriers to pass through it. Ex-1003, ¶130. A POSITA would further

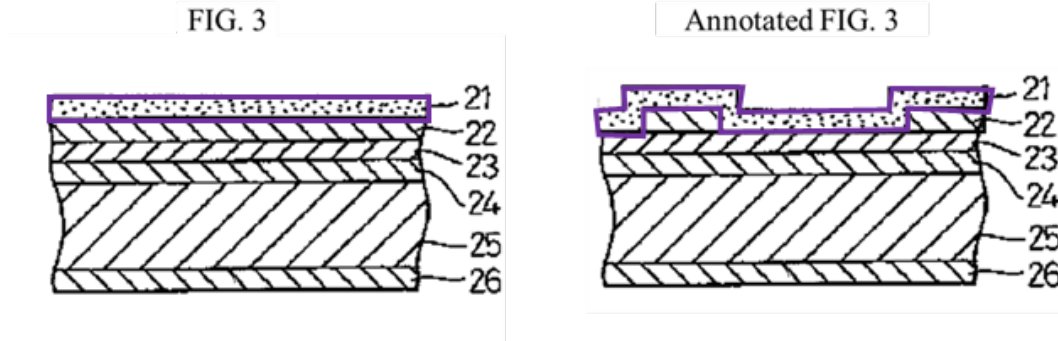
understand that the dopant diffusion from *the conductive and passivating layer* (silicon layer 23) to *the interface passivator layer* (n⁻ type crystalline silicon 24) and finally into *the substrate* (silicon layer 25) establishes continuous shortened vertical current pathways extending from the *electrodes* to the *substrate*. Ex-1003, ¶130.

FIG. 3¶



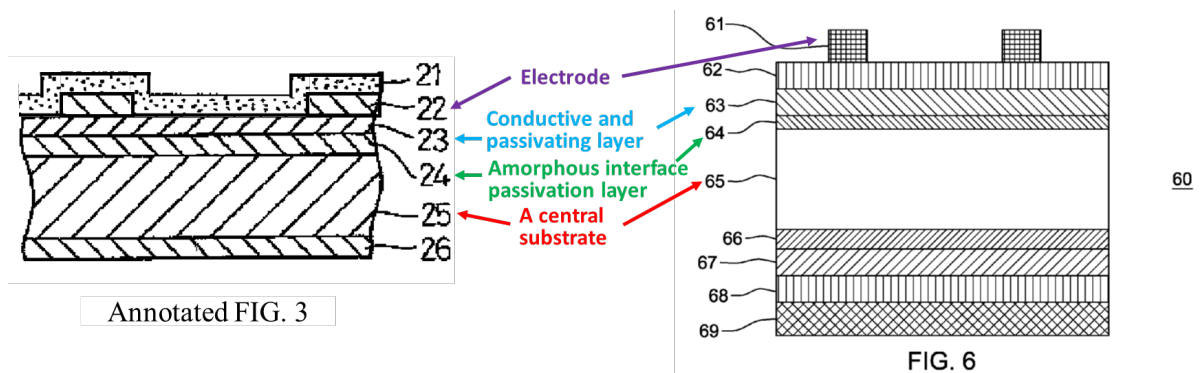
Ex-1004, FIG. 3 (annotated).

Dr. Hatalis further explains that a POSITA would understand that Tamura discloses the top n-region consisting of layers 23 and 24; the *conductive and passivating layer* and the *interface passivation layer*, respectively, provides a low resistance path for the minority carriers to flow from the substrate (element 25) to the electrode (element 22). Ex-1003, ¶131.



Ex-1004, FIG. 3 (left), Ex-1004, FIG. 3 (annotated, right).

Tamura discloses a *shortened charge carrier flow path* between the substrate and the electrodes, even in the regions not covered by the metal electrodes, as this flow path is a low resistance path. Ex-1003, ¶132. The comparison between annotated FIG. 3 of Tamura with Figure 6 of the '074 patent shows that Tamura discloses the same structure as the one in the '074 patent. Ex-1003, ¶132. Dr. Hatalis further shows that Tamura discloses the same materials as the examples in the '074 patent. Ex-1003, ¶132. Finally, Tamura discloses a sheet resistance for the n-region, which is within the range stated in the '074 patent. Ex-1003, ¶132.



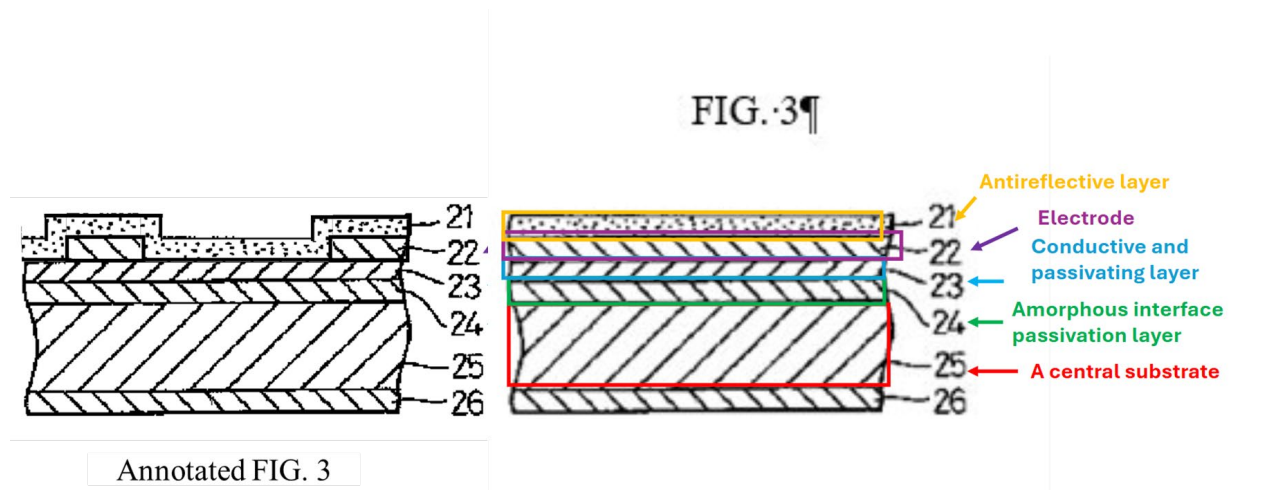
Ex-1004, FIG. 3 (annotated, left), Ex-1001, FIG. 6 (right).

2. Claim 2

The '074 patent allows the antireflective layer to be a transparent conductive oxide. '074 patent, 8:61-64 (“102: Antireflection film, ... Examples include ... **transparent conductive oxides.**”).

Tamura discloses depositing the *at least one antireflective layer*. Ex-1003, ¶136.

First, Tamura discloses a “transparent electrode” 21 that can be a transparent conductive oxide, *an antireflective layer*, (on the top or front side or light entering side). Ex-1004, [0018] (“In FIG. 3, **21 denotes a transparent electrode**”). Although FIG. 3 of Tamura depicts the antireflective layer on top of the metal electrode 22, a POSITA would understand that the cross section depicted in Figure 3 is along a direction that is parallel to one of the fingers of the comb. Ex-1003, ¶137. A POSITA would also understand that if the cross-section is drawn along a direction perpendicular to the fingers of the comb, it will appear as shown in the annotated FIG. 3 shown below. Ex-1003, ¶137. A POSITA would understand that in the portion of the top surface not covered with the metal electrode 22, i.e., in between two successive fingers, as shown in the annotated FIG. 3 below, the transparent electrode acts as an antireflective layer by minimizing the amount of light that is reflected by the top surface and thus more light is entering the solar cell. Ex-1003, ¶137.

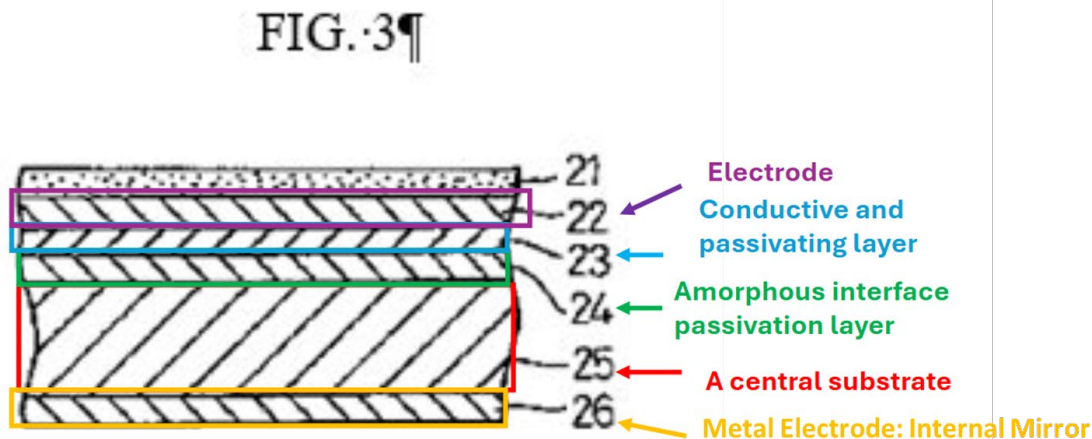


Ex-1004, FIG. 3 (annotated).

Dr. Hatalis further explains that a PHOSITA would understand a “transparent electrode” 21, e.g., a transparent conductive oxide such as Indium Tin Oxide (ITO) serves as an *antireflective layer* because a transparent electrode has optical transparency and can be deposited with a low index of refraction ($n < 2$) in order to minimize the difference between its index of refraction and the index of refraction of air $n=1$, thus minimizing reflection. Ex-1003, ¶138.

Second, Tamura also discloses a “back surface electrode” 26 that can *form a good internal mirror on a back of the solar cell*. Ex-1004, [0018] (“26 denotes a back surface electrode.”) A POSITA would understand that the “back surface electrode” 26 is a metal that serves as an internal mirror that reflects photons that reach the back side towards the front thus increasing the optical path of the photons. Ex-1003, ¶139. Dr. Hatalis further refers to Smith and the ’074 patent disclosure to explain that a

common back electrode used in solar cells is aluminum, and it was well known that aluminum has a high reflectance. Ex-1003, ¶139; Smith, FIG. 12; Ex-1001, 7:51-53, 12:8-9.



Ex-1004, FIG. 3 (annotated).

Furthermore, applying a metal electrode on the back side that can serve as a mirror to reflect photons toward the front side was standard practice in fabricating solar cells as of 2009. Ex-1003, ¶140. Tamura discloses that such standard practice can be performed on solar cells. Ex-1004, [0012] (“The formation of electrodes and the like other than the formation of the pn junction can be performed in the same manner as in a typical solar cell”); Ex-1003, ¶140. Dr. Hatalis refers to Yamamoto and explains that POSITA would understand that an internal mirror, e.g., a back surface electrode 26, as a typical industrial standard practice, is disclosed by Tamura. Ex-1003, ¶140.

3. Claim 3

a) 3[pre]

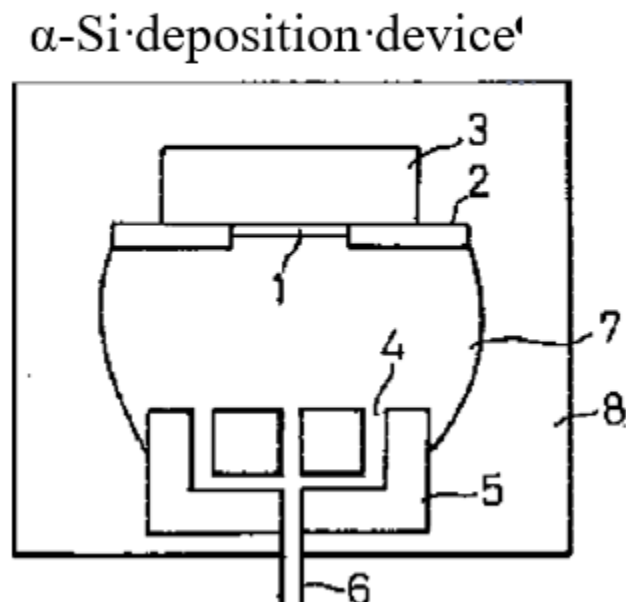
See discussion of claim 1.

b) 3[a]

Tamura discloses that both amorphous layer 12 (*interface passivation layer*) and amorphous layer 13 (*conductive and passivating layer*), depicted in FIG. 2, are layers of amorphous silicon. Tamura, [0015] (“Next, a high-concentration n^+ type amorphous silicon layer 13 was deposited on the undoped amorphous silicon layer 12...”); Ex-1003, ¶144.

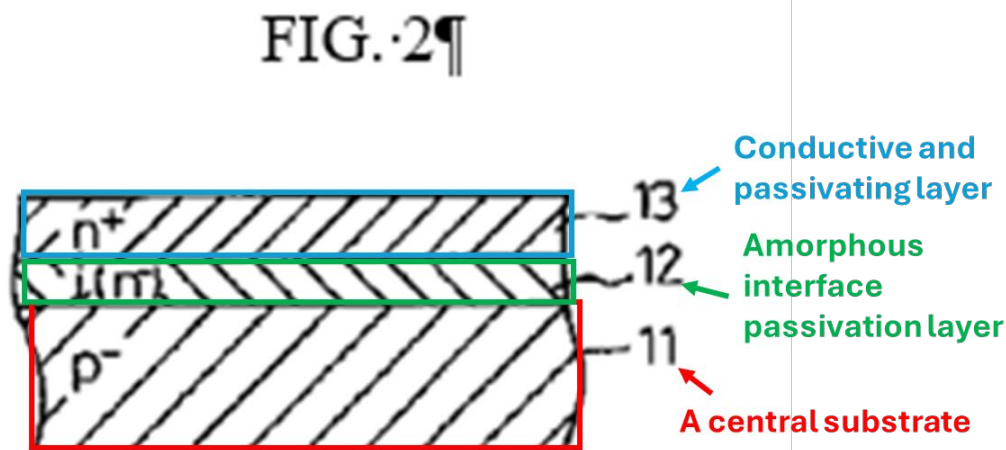
Tamura FIG. 1 further depicts a deposition device. Ex-1004, [0014]; Ex-1003, ¶145. Tamura also discloses that the deposition temperature is 170°C, the plasma power is 10W and the source gas is SiH_4 . Tamura [0015]-[0016]. Dr. Hatalis refers to Fuhs and explains that a POSITA would understand that Tamura’s deposition device uses Plasma Enhanced Chemical Vapor Deposition (PECVD). Ex-1003, ¶145.

FIG. 1¶



Tamura, FIG. 1.

Dr. Hatalis explains that a POSITA would understand that the plasma deposition conditions disclosed by Tamura for *depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer* (the two amorphous silicon layers 12 and 13) yield a material known as hydrogenated amorphous silicon, which is *an amorphous silicon-containing compound over the substrate* (“the p-type silicon substrate 11”); Ex-1003, ¶146.



Ex-1004, FIG. 2 (annotated).

Based on the disclosure of the '074 patent, a POSITA would understand that all intrinsic amorphous silicon or phosphorus-doped amorphous silicon films deposited by PECVD are amorphous silicon containing compounds known as hydrogenated amorphous silicon. Ex-1003, ¶147; Ex-1001, 5:56-60, 5:42-51, 15:54-55, 15:66-16:3.

c) 3[b]

As shown for limitation 3[a] above, the deposition conditions in Tamura to deposit the two amorphous silicon layers 12 and 13 yield an amorphous silicon-containing compound: hydrogenated amorphous silicon. Ex-1003, ¶148.

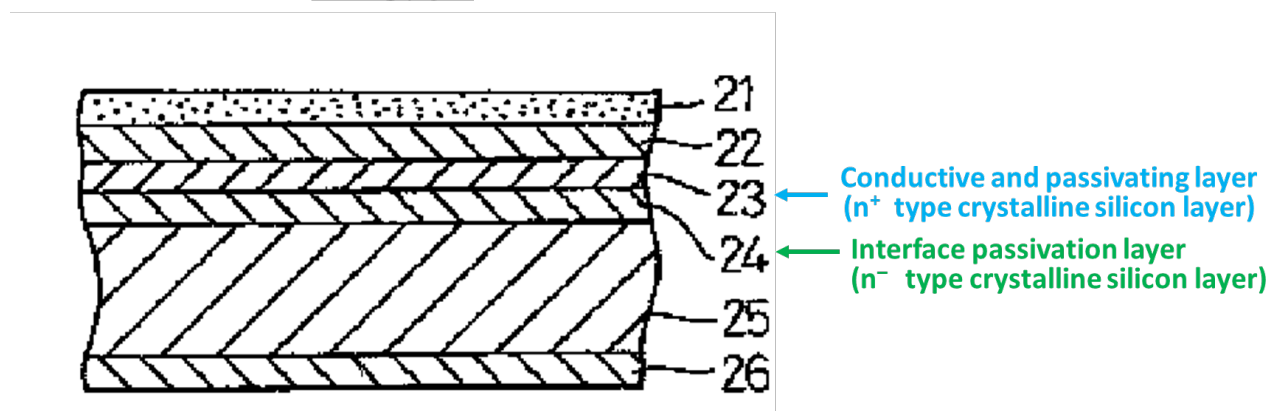
A POSITA would also understand that the thermal treatment will *separate the amorphous silicon-containing compound* into *at least one interface passivation layer* (the crystallized amorphous silicon layer 12 relabeled by Tamura as element 24 in

Figure 3) and at least one conductive and passivating layer (the crystallized amorphous silicon layer 13 relabeled by Tamura as element 23 in Figure 3). Ex-1003, ¶149.

As Dr. Hatalis explains, a POSITA would understand that *the thermal treatment* would separate *the amorphous silicon-containing compound* into the *conductive and passivating layer* (the n⁺ type crystalline silicon layer 24) and into the *interface passivation layer* (the n⁻ type crystalline silicon layer 23), because the following two phenomena occur during the thermal treatment. Ex-1003, ¶150.

First, the initially undoped amorphous silicon layer 12 (*interface passivation layer*) crystallizes by solid phase crystallization, which causes part of the amorphous silicon at the interface between amorphous silicon layer 12 and substrate 11 to crystallize epitaxially on the single-crystal substrate (“the p-type silicon substrate 11”). Ex-1004, [0005] (“heat-treating the undoped and second conductivity-type amorphous silicon layers to covert the layers into crystalline silicon layers, thereby forming a pn junction having a graded structure...by **solid phase epitaxy**.”). Moreover, Tamura discloses that after the thermal treatment, the initially undoped “amorphous silicon layer 12” becomes an “n⁻ type crystalline silicon,” the *interface passivation layer*, denoted as layer 24 in FIG. 3, which is distinct from the layer 23 “an n⁺ type crystalline layer,” the *conductive and passivating layer*, formed by the crystallized “n⁺ type amorphous silicon layer.” Ex-1003, ¶151.

FIG. 3



Tamura, FIG. 3 (annotated).

Tamura's disclosure on removing oxide film with hydrofluoric acid further confirms that the epitaxial growth phenomenon happens during thermal treatment. Ex-1004, [0007] ("The surface of the substrate is highly preferably subject to a cleaning treatment prior to deposition of an amorphous silicon layer in order to form a pn junction of favorable quality by **solid phase epitaxy**."), *see also* Ex-1004, [0014]; Ex-1003, ¶152.

Second, the initial n⁺ type amorphous silicon layer 13 (*one conductive and passivating layer*) crystallizes and becomes the "n⁺ type crystalline layer" denoted as layer 24 in Tamura's FIG 3. Ex-1003, ¶153.

4. Claim 4

As shown in claim 3, Tamura discloses the crystallization of amorphous silicon layer 12 (*interface passivation layer*) by "solid phase epitaxy," which a POSITA would understand to form single crystal regions that extend above the substrate ("the p-type

silicon substrate 11”) and into the crystallized amorphous silicon layer. Ex-1003, ¶156.

A POSITA would know that such epitaxially crystallized regions may not be continuous laterally, as residual native oxide of silicon may prevent epitaxial crystallization in certain regions. Ex-1003, ¶157. Accordingly, the epitaxially crystallized regions, which result from the *thermal treatment* in the *interface passivation layer* (amorphous silicon layer 12), form the “*perforation*” as *carriers would transport through* these regions since the carrier mobility is higher in such single crystal regions compared to the mobility in other regions in which the solid phase epitaxy was prevented by the presence of silicon’s native oxide which grows easily upon exposure of silicon to air. Ex-1003, ¶157.

5. Claim 5

a) 5[pre]

See discussion of claim 1.

b) 5[a]

See discussion of limitation 3[a].

c) 5[b]

Tamura teaches that the *thermal treatment initiates crystallization of* the amorphous silicon layer 13 (*at least one conductive and passivating layer*) into a crystalline silicon layer. Ex-1004, [0005] (“heat-treating the undoped and second conductivity-type amorphous silicon layers to convert the layers into crystalline silicon layers”), [0010] -[0011]; Ex-1003, ¶163.

Dr. Hatalis explained that, based on Tamura's disclosure, a POSITA would understand that the amorphous silicon layer 13 (the *conductive and passivating layer*) is in direct contact with the amorphous silicon later 12 and thus during the thermal anneal at least a portion of this layer will be crystallized by random nucleation, resulting in a polycrystalline film. Ex-1003, ¶164. A POSITA would also understand that the resulting structure of the crystallized layer 13 will resemble that of the "polycrystal substrate" and thus the amorphous silicon layer 13 (*at least one conductive and passivating layer*) is crystallized *into a polycrystalline film*. Ex-1003, ¶164.

6. Claim 6:

a) 6[pre]

See discussion of claim 1.

b) 6[a]

See discussion of limitation 3[a].

c) Limitation 6[b]

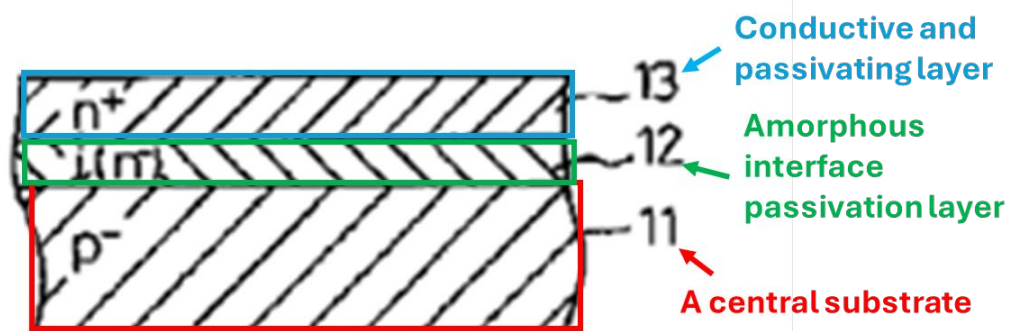
Tamura teaches or suggests this limitation.

Tamura teaches that *the thermal treatment initiates crystallization* of the amorphous silicon layer 13 (*one conductive and passivating layer* also referred to by Tamura as the second conductivity-type amorphous silicon layer). Ex-1004, [0011] ("This heat treatment **crystallizes** the undoped and **second conductivity-type amorphous silicon layers.**"); Ex-1003, ¶170.

Tamura further teaches that *the thermal treatment increases the optical transmissivity* through crystallizing the amorphous silicon layer 13. Ex-1004, [0017] (“A crystal structure of the resulting crystallized film was observed by ultraviolet surface reflection and R-HEED (reflection high energy electron diffraction). The results confirmed that a crystal structure was obtained.” Dr. Hatalis explains that a POSITA would understand that when the amorphous silicon layer 13 crystallizes and transforms into polycrystalline silicon, its optical transmissivity increases as the light absorption coefficient of crystalline silicon is lower than that of amorphous silicon. Ex-1003, ¶171.

Dr. Hatalis further refers to Shah and explains that the optical transmissivity of the crystallized silicon layer 13 is higher after the thermal treatment since it observes less light. Ex-1003, ¶172.

FIG. 2¶



Ex-1004, FIG. 2 (annotated).

7. Claim 7:

a) 7[pre]

See discussion of claim 1.

b) 7[a]

See discussion of limitation 3[a].

c) 7[b]:

Tamura teaches or suggests this limitation.

A POSITA would understand that the deposition conditions disclosed by Tamura to deposit the two amorphous silicon layers (layers 12 and 13 in FIG. 2) yield hydrogenated amorphous silicon, which is an amorphous silicon-containing *compound*. Ex-1003, ¶178.

Tamura discloses a thermal treatment at 600°C or higher. Ex-1004, [0016] (“the substrate 11, on which the amorphous silicon layers 12, 13 were deposited, maintained at 600°C for 5 minutes”) and Ex-1004, [0012]. A POSITA would understand that the thermal treatment disclosed by Tamura (600°C or higher) *activates doping atoms in the compound* which results in an n⁺ type crystalline silicon layer (depicted by element 23), and an n⁻ type crystalline silicon layer (depicted by element 23) in Figure 3. See Ex-1004, [0018]; Ex-1003, ¶178.

Tamura also discloses that the thermal treatment that *activates doping atoms in the compound* through creating a pn junction with a graded structure. Tamura, [0011]

(“[T]he **heat treatment** crystallizes the undoped and **second conductivity-type amorphous silicon layers**, forming a pn junction having a graded structure...The **dopant concentration** of the crystallized second conductivity-type silicon layer can easily **be increased to approximately 10^{21}cm^{-3}** .”). Moreover, Tamura discloses that after the thermal treatment, “the electrical properties were observed by Hall effect measurement and spreading resistance measurement” and that the “results confirmed that a crystal film was obtained, having a graded structure **with a carrier concentration of 10^{20}cm^{-3} near the surface, and a resistivity of approximately $10^{-3}\ \Omega\cdot\text{cm}$ (carrier concentration)**.” Ex-1004, [0017]. Dr. Hatalis explains that a POSITA would understand that the carrier characteristics disclosed by Tamura, i.e., “a carrier concentration of 10^{20}cm^{-3} near the surface” and “a pn junction with a graded structure,” refer to the carriers that result from the dopants as a direct result of their activation by the thermal treatment. Ex-1003, ¶179.

8. Claim 8:

a) 8[pre]

See discussion of claim 1.

b) 8[a]

See discussion of limitation 3[a].

c) 8[b]

Tamura discloses, “the heat treatment crystallizes the undoped and second conductivity-type amorphous silicon layers, **forming a pn junction having a graded**

structure.” *See* Ex-1004, [0011]; Ex-1003, ¶185.

Specifically, this “graded structure” is formed by the diffusion of the dopant atoms into the substrate to create a structure in which the concentration of the dopant atoms changes “gradually” from high concentration at the surface ($\geq 10^{20} \text{ cm}^{-3}$) to the same level as that of the substrate (“approximately 10^{17} to $10^{15}/\text{cm}^3$.”) Ex-1004, [0011] (“The dopant concentration of the crystallized second conductivity-type silicon layer can easily be increased to approximately 10^{21} cm^{-3} ”), *see also* Ex-1004, [0017], [0006]; Ex-1003, ¶186.

B. Ground 2: Claims 1-2 and 4-8 are Anticipated or Rendered Obvious by Borden

1. Claim 1

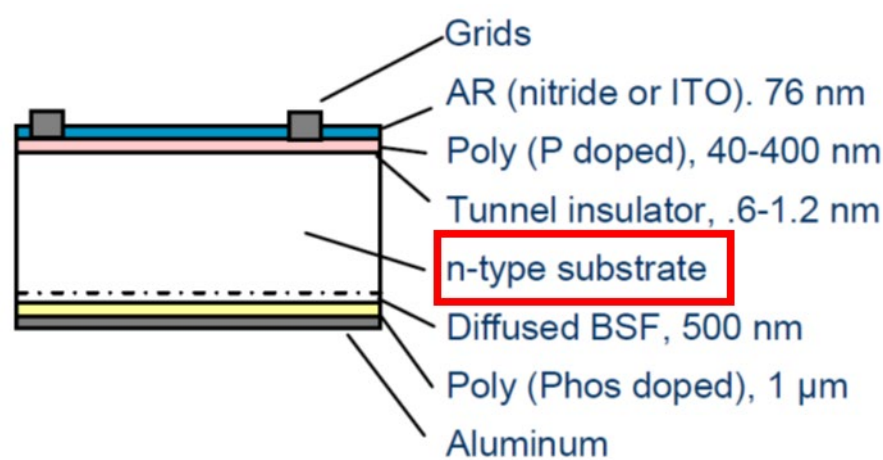
a) 1[pre]

Borden discloses that “use of heavily doped polysilicon combined with a tunnel dielectric to provide an alternate to diffused junctions for silicon solar cells.” Ex-1006, 1149; Ex-1003, ¶¶187-188.

b) 1[a]

Borden discloses an n-type CZ wafer as a central substrate. Ex-1006, 1149 (“Because the IC equipment runs **300 mm wafers**, we have been restricted to $780 \mu\text{m}$ thick **CZ substrates** without texture”), *see also* Ex-1006, 1150; Ex-1003, ¶190. Figure 2 of Borden depicts the structure of a single-sided device, and Figure 3 the corresponding process flow, while Figure 6 depicts the experimental lifetimes

measured on symmetric front/back polysilicon emitter (PE) structures; all these figures depict the use of n-type CZ silicon substrates.



Ex-1006, FIG. 2 (annotated).

[A] Start – n-Cz (770 μm) [B]	
Back poly 1 μm phos 7e20/cm ³	
Drive-in RTA 4 mins 1000°C	
HF clean	
Tunnel layer (various, 6-12Å)	
a-Si(B) (20 nm)	a-Si(B) (200 nm)
RTA	
ITO	SiNx
Back contact (Al)	
Front contact	

Ex-1006, FIG. 3 (annotated).

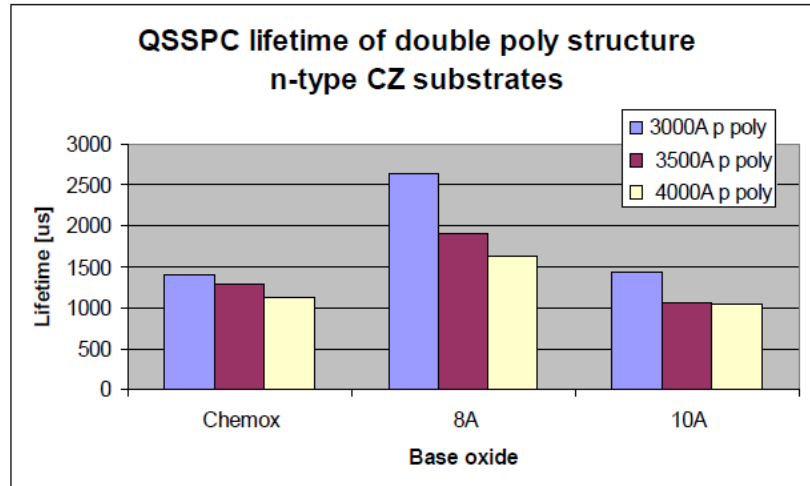
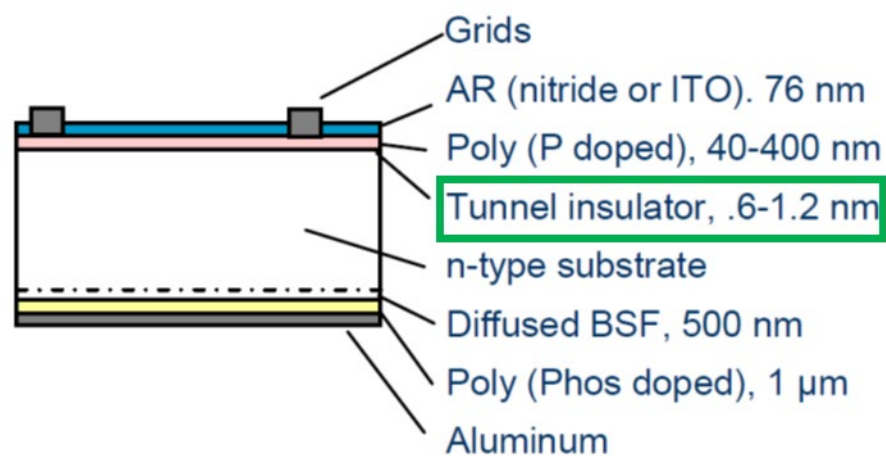


Figure 6: QSSPC lifetimes for symmetric front/back PE structures on n-type CZ.

Ex-1006, FIG. 6.

c) 1[b]

Borden discloses growing thin **tunnel dielectrics** (also referred to as **tunnel layers** or **tunnel insulators**) over the front and/or back of the n-type substrate. Ex-1006, 1149 (“Thin tunnel dielectrics (6-12Å) are fabricated using methods adapted from IC processing.”), *see also* Ex-1006, 1150-51, FIGs. 1-3, 5-7, 9, 10; Ex-1003, ¶192. Borden’s tunnel dielectric/layer/insulator is the *amorphous interface passivation layer over the substrate*. Ex-1003, ¶192



Ex-1006, FIG. 2 (annotated).

[A] Start – n-Cz (770 μm) [B]	
Back poly 1 μm phos 7e20/cm ³	
Drive-in RTA 4 mins 1000°C	
HF clean	
Tunnel layer (various, 6-12Å)	
a-Si(B) (20 nm)	a-Si(B) (200 nm)
RTA	
ITO	SiNx
Back contact (Al)	
Front contact	

Ex-1006, FIG. 3 (annotated).

A POSITA would understand that the tunnel dielectrics are grown directly on the substrate and thus are “over the substrate.” Ex-1003, ¶193. Borden discloses two methods for forming tunnel dielectrics: chemical oxidation (“chem-ox”) and rapid thermal oxidation (“RTO”) of the silicon substrate. Ex-1006, 1150; Ex-1003, ¶193. Dr.

Hatalis explains that a POSITA would understand that the material of these tunnel dielectrics is a silicon oxide, and silicon oxides grown on a silicon substrate either with chemical or thermal oxidation are amorphous materials. Ex-1003, ¶193. A POSITA would understand that the tunnel dielectrics are passivating because Borden states that the tunnel dielectrics can serve as “passivation layers.” Borden, 1149; Ex-1003, ¶194. Borden refers to the band diagram of the solar cell with thin “tunnel insulator” layers in Figure 1 as a “cell with a tunnel insulator **passivated interface**.” Ex-1003, ¶194.

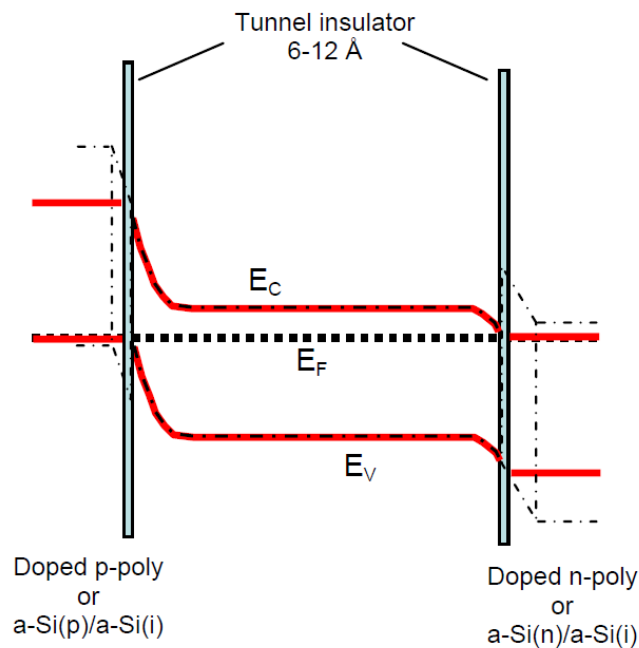
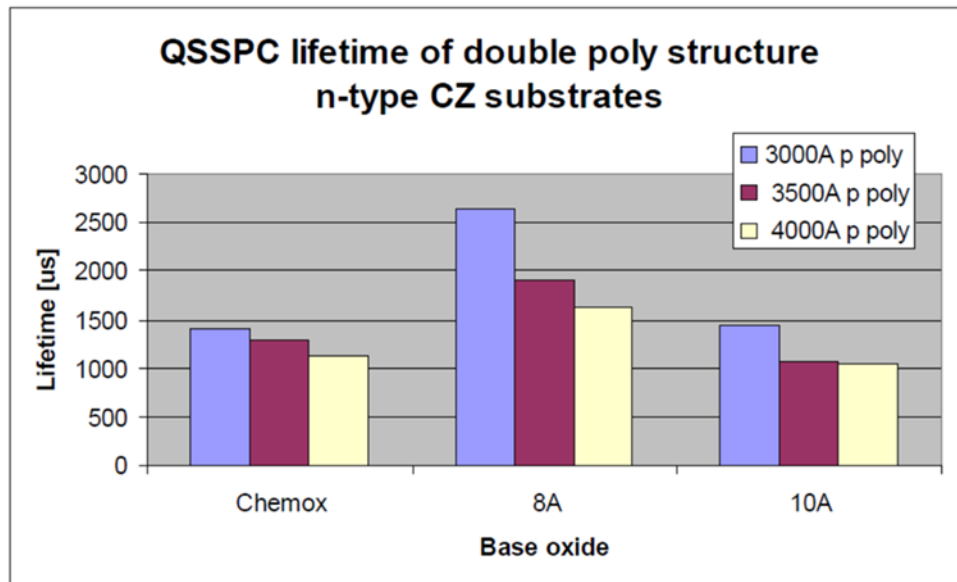


Figure 1: Comparison of band structures for doped polysilicon--c-Si(n) cell with a tunnel insulator passivated interface (red and blue) and a-Si(p)--c-Si(n) heterojunction (black) cells.

Ex-1006, FIG. 1.

Borden also teaches the impact of different tunnel dielectric materials, such as RTO, which yields a higher lifetime, thereby “provid[ing] improved interface

passivation.” Ex-1006, 1150-51; FIG. 6; Ex-1003, ¶195.



Ex-1006, FIG. 6.

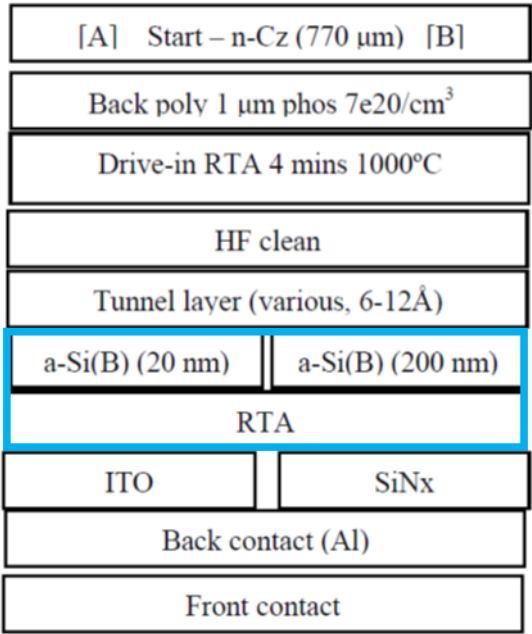
The '074 patent also acknowledges that dielectrics can provide interface passivation by listing “silicon oxide” as an example of an electrically passivating interface layer. *see e.g.*, Ex-1001, 3:50-53, 5:58-59; Ex-1003, ¶196.

d) 1[c]

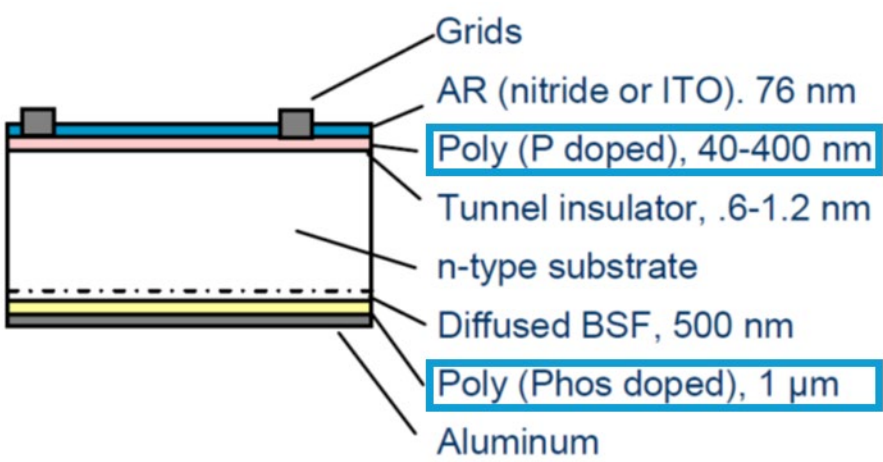
Borden discloses depositing an amorphous silicon layer, which is p-type doped, directly on top of the tunnel insulator layer, i.e., the *interface passivation layer*. Ex-1003, ¶198. Borden’s p-type doped amorphous silicon layer is the *conductive and passivating layer*. Ex-1006, 1150 (“n-type CZ wafers were coated front and back with a thin tunnel layer...Amorphous silicon was then deposited.”); Ex-1003, ¶198.

Borden further discloses that the deposited amorphous silicon is doped p-type

with a boron *dopant*. Ex-1006, FIG. 6; Ex-1003, ¶199. Borden discloses that after the deposition of the amorphous silicon, a rapid thermal annealing (RTA) step is performed, which crystallizes the doped amorphous silicon to generate a crystallized layer as “Poly (P doped).” Ex-1006, 1150, FIGs. 2, 3; Ex-1003, ¶199.

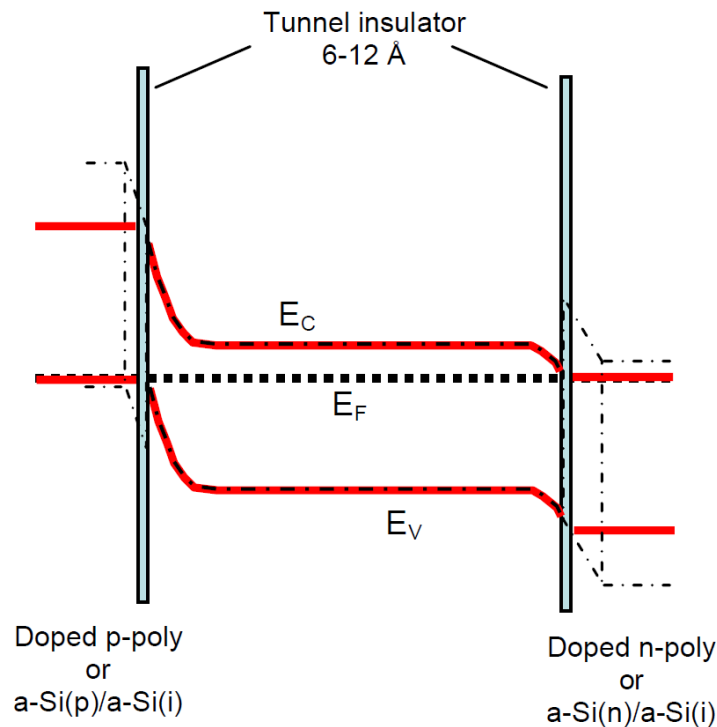


Ex-1006, FIG. 3.



Ex-1006, FIG. 2 (annotated).

Dr. Hatalis explains that a POSITA would understand that a doped polysilicon layer is conductive because Borden demonstrates that the “doped p-poly” has a high concentration of carriers that help to increase the electrical conductivity of this layer. Ex-1003, ¶201.



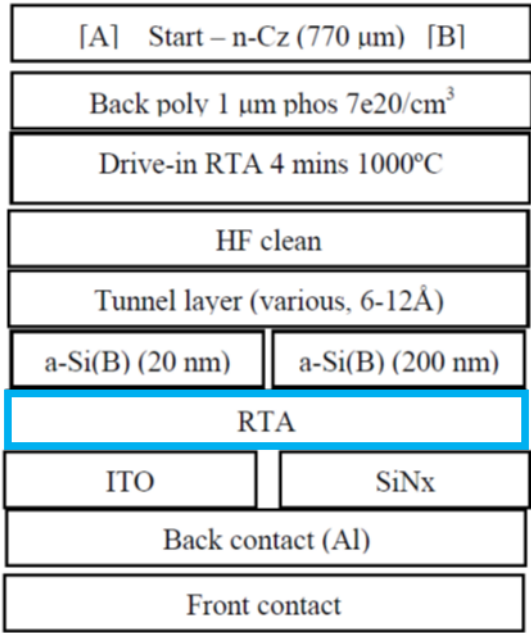
Ex-1006, FIG. 1.

Dr. Hatalis further explains that a POSITA would understand that a doped polysilicon layer is passivating based on the disclosure from Borden and the '074 specification. Ex-1003, ¶202.

e) 1[d]

Borden discloses that the doped polysilicon layer is initially amorphous silicon (a-Si) and is crystallized through thermal treatment, specifically through RTA “at

1000°C.” Ex-1006, 1150, FIGs. 3, 4.



Ex-1006, FIG. 3 (annotated).

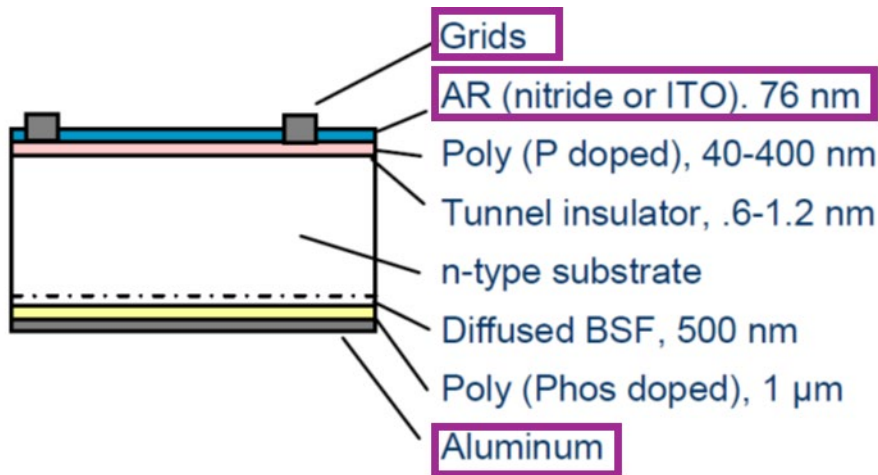
A POSITA would understand that the thermal treatment facilitates diffusion of the dopant from the crystallized poly layer (*the at least one conductive and passivating layer*) through the tunnel dielectric (*the at least one interface passivation layer*), because heating the poly layer at **1000°C** increases the atomic motion of the dopant atoms in the depoed poly layer and allow them to diffuse through the tunnel dielectric into the n-type silicon substrate. Ex-1003, ¶205.

Dr. Hatalis further explains that Borden discloses that the thermal treatment causes boron (i.e., the dopant) to diffuse into the substrate. Ex-1003, ¶206.

f) 1[e]

Borden discloses the formation of front-side metallization as grids that directly

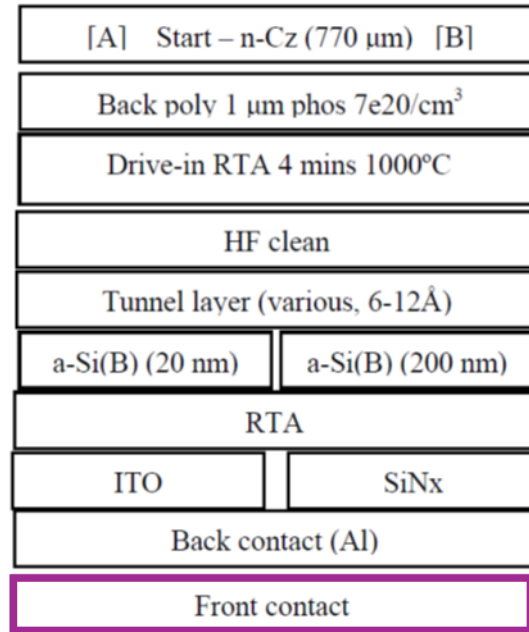
contact the front-side doped polysilicon layer, the *conductive and passivating layer*, and back-side aluminum electrodes that directly contact the back-side doped polysilicon layer. Ex-1006, FIGs 2, 3; Ex-1003, ¶208. Borden’s “Grids” or “Front Contact,” as depicted in Figures 2-3, provides *metallization as electrodes*.



Ex-1006, FIG. 2 (annotated).

A POSITA would understand that front-side grids in solar cells are typically formed through metallization while the aluminum back electrode discloses the metallization limitation as it is itself a metallic conductor. Ex-1003, ¶209.

Borden further discloses that the processing, i.e., “Front contact,” that results in the metallization, i.e., the grid electrodes depicted in Figure 2, takes place after the RTA, which is the *thermal treatment* step, as evident by Borden’s “process flow given in figure 3.” Ex-1006, 1149-50, FIG. 3; Ex-1003, ¶210.

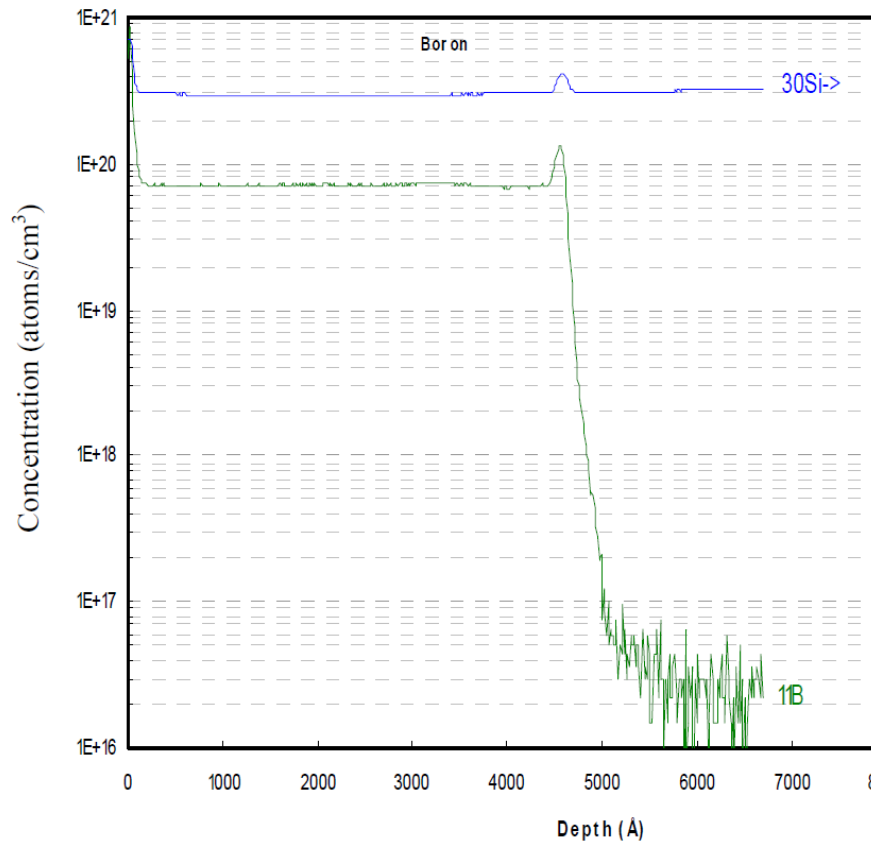


Ex-1006, FIG. 3 (annotated).

g) 1[f]

The '074 patent does not define the term *shortened charge carrier flow paths*. To the extent First Solar claims the dopant diffused from the conductive and passivating layer through the interface passivation layer provides shortened charge flow paths, Borden discloses such paths. Ex-1003, ¶212.

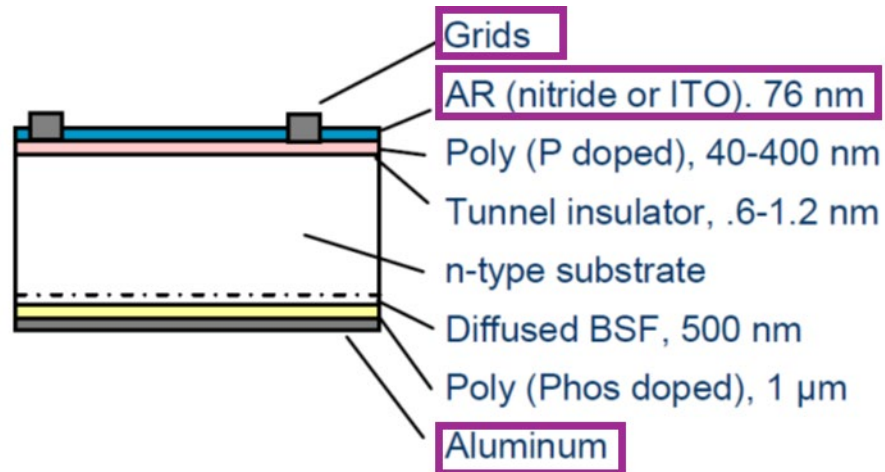
As explained in 1[d], Figure 4 of Borden discloses that the thermal treatment causes dopants to diffuse through the tunnel dielectric layer and ultimately into the substrate. A POSITA would understand that under the above interpretation, this process provides shortened charge flow paths between the substrate and the electrode on the doped polysilicon layer. Ex-1003, ¶213.



Ex-1006, FIG. 4.

To the extent First Solar claims the shortened paths occur when “[charge carriers’] transport within the emitter is vertical instead of mainly lateral,” which is achieved when using a “full area contact coverage” electrode that covers the emitter, *see e.g.*, Ex-1001, 4:49-50, Borden discloses such paths. Ex-1003, ¶214.

Borden discloses that the ITO front contact layer, serving as an electrode, covers nearly the entire area of the front-side doped polysilicon, while the aluminum back contact layer, also functioning as an electrode, fully covers the back-side doped polysilicon area. Ex-1006, FIG. 2; Ex-1003, ¶215.

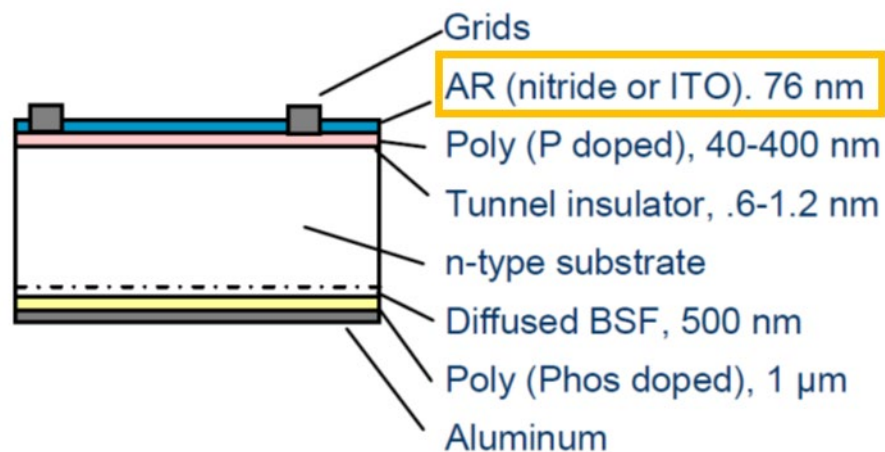


Ex-1006, FIG. 2 (annotated).

Dr. Hatalis explains that a POSITA would understand that this extensive electrode coverage over the doped polysilicon regions reduces unnecessary lateral current paths, thereby effectively shortening the charge carrier flow paths between the substrate and the electrodes. Ex-1003, ¶216.

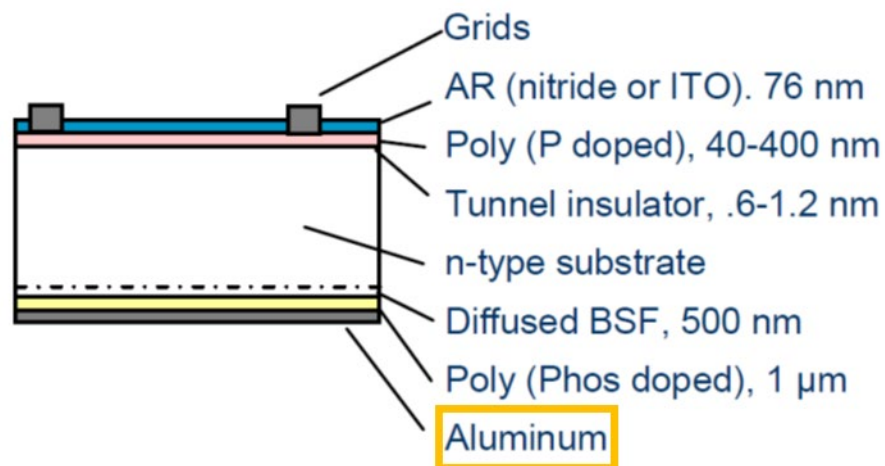
2. Claim 2

Borden discloses depositing at least two types of antireflective layer: an overlaid “ITO” and a “Si₃N₄ AR coating.” Ex-1006, 1149, FIGs. 2-3; Ex-1003, ¶218.



Ex-1006, FIG. 2 (annotated).

Borden also discloses an aluminum layer which is known to reflect light, thus forming a good internal mirror on the back of the solar cell. Ex-1006, FIGs. 2-3.



Ex-1006, FIG. 2 (annotated).

The '074 patent defines “a low reflective index layer for a good internal mirror on the back” as a layer with a “refractive index basically smaller than 3.0, smaller than 2.6, smaller than 2.0, smaller than 1.5.” Ex-1001, 15:31-35.

Dr. Hatalis refers to Smith and explains that a POSITA would understand that the aluminum layer on the back side, as disclosed in Borden, has a refractive index less than 2.0, which functions as a good internal mirror. Ex-1003, ¶221.

3. Claim 4

Borden discloses forming a tunnel dielectric layer on a substrate either by chemical oxidation or by RTO followed by deposition of amorphous silicon and subsequent crystallization at elevated temperatures (e.g., 1000°C). Ex-1006, 1150; Ex-

1003, ¶223.

Dr. Hatalis explains that a POSITA would understand that the high-temperature annealing and significantly different thermal expansion coefficients between the tunnel dielectric layer and the adjacent silicon layers above and below, develop perforations in the tunnel dielectric layer. Ex-1003, ¶¶224-225.

Dr. Hatalis refers to Wostenholme and Bravman to show that the thermal stability of a thin silicon oxide at the interface between a silicon substrate and a polycrystalline silicon emitter had been well-studied. Ex-1003, ¶226. Dr. Hatalis further explains that a POSITA would understand that, due to the thermal instability of thin oxides, perforations are formed in Borden's thin tunnel oxide, since it was well known that such perforations are formed when the anneal temperature exceeds 900°C. Ex-1003, ¶227.

4. Claim 5:

a) 5[pre]

See discussion of claim 1.

b) 5[a]

Borden discloses depositing amorphous silicon on the tunnel dielectric. Ex-1006, 1149-50; Ex-1003, ¶231. Borden also discloses that the amorphous silicon was deposited using standard "IC equipment" that "runs 300 mm wafers." Ex-1006, 1149. A POSITA would understand that the IC equipment that can deposit amorphous silicon on 300 mm wafers includes CVD equipment (either PECVD or Low Pressure CVD

(LPCVD)), both of which utilize decomposition of the silane (SiH_4) compound. Ex-1003, ¶231.

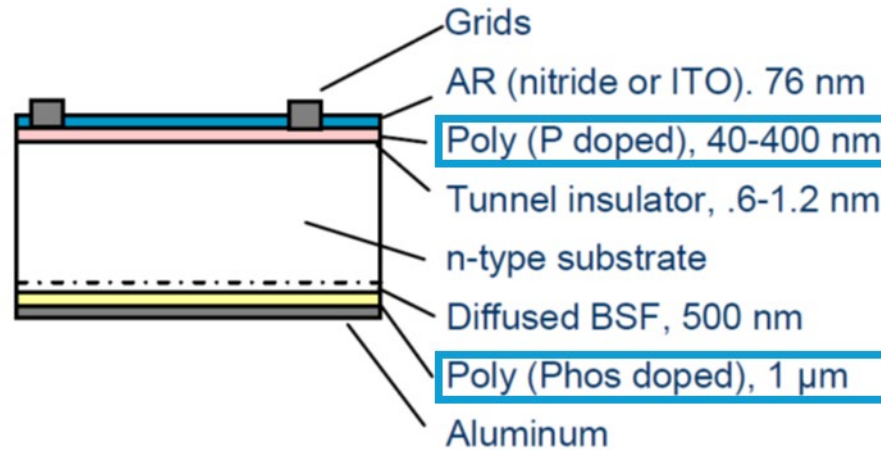
Moreover, Borden specifically discloses that the amorphous silicon layer, which is later crystallized, is “in-situ doped p-type”—i.e., doped with boron, a conductive dopant. Ex-1006, 1150; Ex-1003, ¶232.

A POSITA would understand that Borden discloses the deposition of an amorphous silicon containing compound as the conductive and passivating layer. Ex-1003, ¶233.

c) 5[b]

Borden discloses that on top of the thin silicon oxide layer (the *interface passivation layer*), “[a]morphous silicon was then deposited and crystallized with a 30 second RTA at 1000°C.” Ex-1006, 1150. Dr. Hatalis refers to Hatalis and explains that a POSITA would understand that, when an amorphous layer is not in direct contact with a crystalline substrate, its crystallization occurs by random nucleation and growth, which results in a polycrystalline silicon layer. Ex-1022, 2261, 2263; Ex-1003, ¶235.

Borden also refers to the crystallized form of amorphous silicon deposited on the tunnel dielectric layer as polycrystalline silicon (also referred to as “polysilicon” or “poly”). Ex-1006, 1149-50, FIGs. 1-3; Ex-1003, ¶236.



Ex-1006, FIG. 2 (annotated)

5. Claim 6

a) 6[pre]

See discussion of claim 1.

b) 6[a]

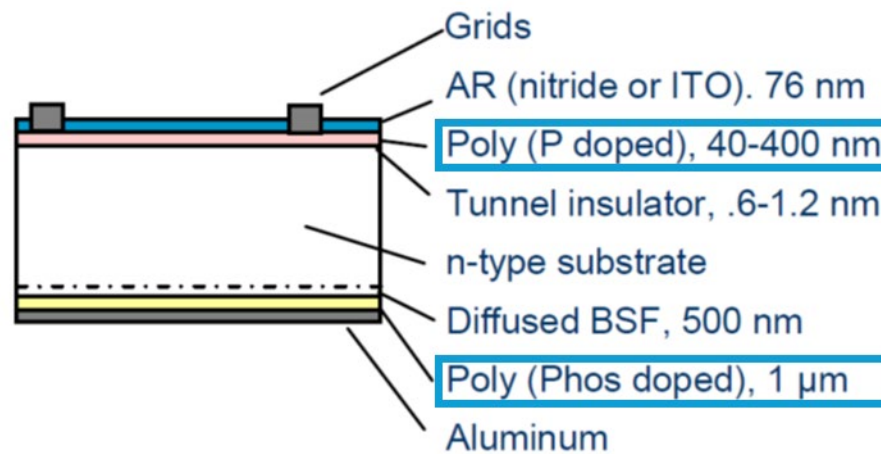
See discussion of limitation 5[a].

c) 6[b]

As discussed in 1[d], Figure 2 of Borden discloses that the doped polysilicon layer, which serves as the polysilicon emitter, i.e., the Poly (P doped) layer, is first deposited as amorphous silicon and then crystallized through a thermal treatment. Ex-1006, 1150 (“Amorphous silicon was then deposited and crystallized with a 30 second RTA at 1000°C”). Dr. Hatalis refers to Yamamoto and explains that based on Borden’s disclosure, a POSITA would understand that, when the amorphous silicon layer 13 crystallizes and transforms into polycrystalline silicon, its optical transmissivity increases because the light absorption coefficient of crystalline silicon is lower than

that of amorphous silicon. Ex-1003, ¶242.

Dr. Hatalis refers to Shah and explains that a POSITA would also understand that the optical transmissivity of the crystallized polysilicon layer, i.e., Poly (P doped), is higher after thermal treatment than the initially deposited amorphous silicon. Ex-1019, 696; Ex-1003, ¶243.



Ex-1006, FIG. 2 (annotated).

6. Claim 7

a) 7[pre]

See discussion of claim 1.

b) 7[a]

See discussion of limitation 5[a].

c) 7[b]

As shown in 1[c], Borden discloses that the conductive and passivating layer is deposited as an amorphous silicon, which is doped p-type with a boron dopant. Borden describes this doped amorphous silicon layer as “a-Si(B)” in Figure 3.

Borden discloses that after depositing the boron doped amorphous silicon, an RTA step is performed at 1000°C, which crystallizes the doped amorphous silicon. Ex-1006, 1150; Ex-1003, ¶249. Borden refers to the crystallized layer as “Poly (P doped)” in Figure 2. Borden also refers to the device structures formed after the thermal anneal as having “hyper-abrupt junctions.” Ex-1006, 1149; Ex-1003, ¶249. Borden, referring to a **boron-doped polysilicon** test structure, discloses that “Figure 4 shows the boron SIMS profile for a junction test sample...Note that a sharp junction profile is obtained.” Ex-1006, 1150; Ex-1003, ¶249.

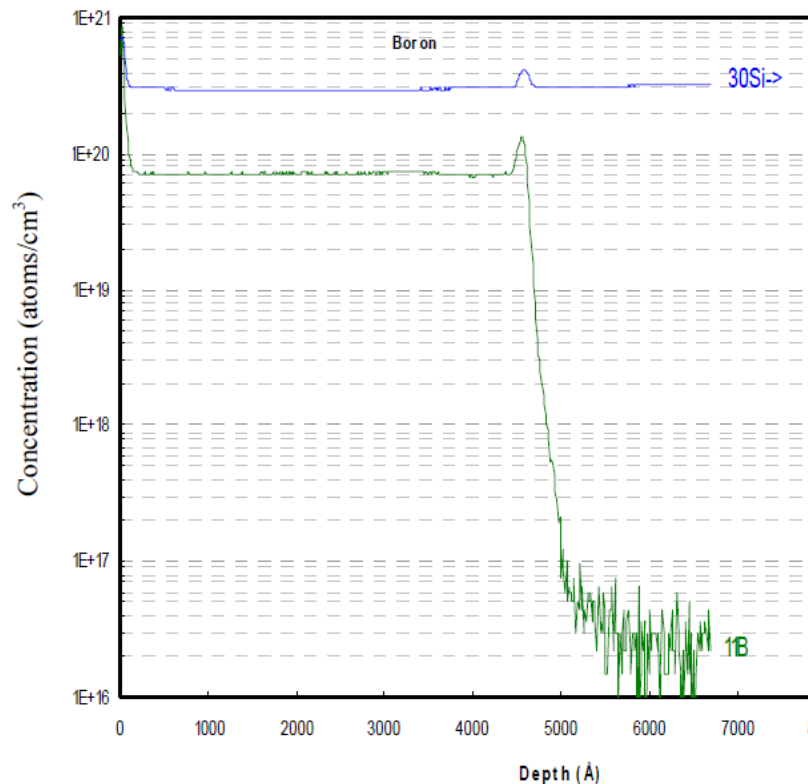


Figure 4: SIMS boron and reference silicon profile for a boron-doped polysilicon test structure.

Ex-1006, FIG. 4.

Moreover, Borden discloses in Figure 8 the current-voltage I(V) characteristics of seven completed solar cells having the structure depicted in Figure 2.

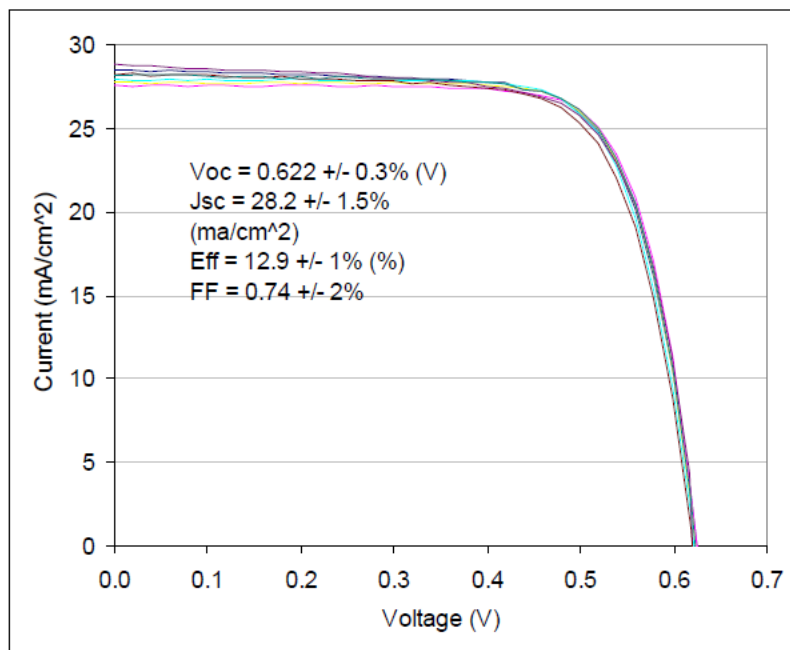


Figure 8: IV curves for seven 2x2 cm isolated PE cells in a 12.5x12.5 cm² area with 400 nm p-type poly on n-Si.

Ex-1006, FIG. 8.

Dr. Hatalis explains that a POSITA would understand that Borden's thermal treatment activates the dopant atoms, i.e., boron. Ex-1003, ¶250.

7. Claim 8

a) 8[pre]

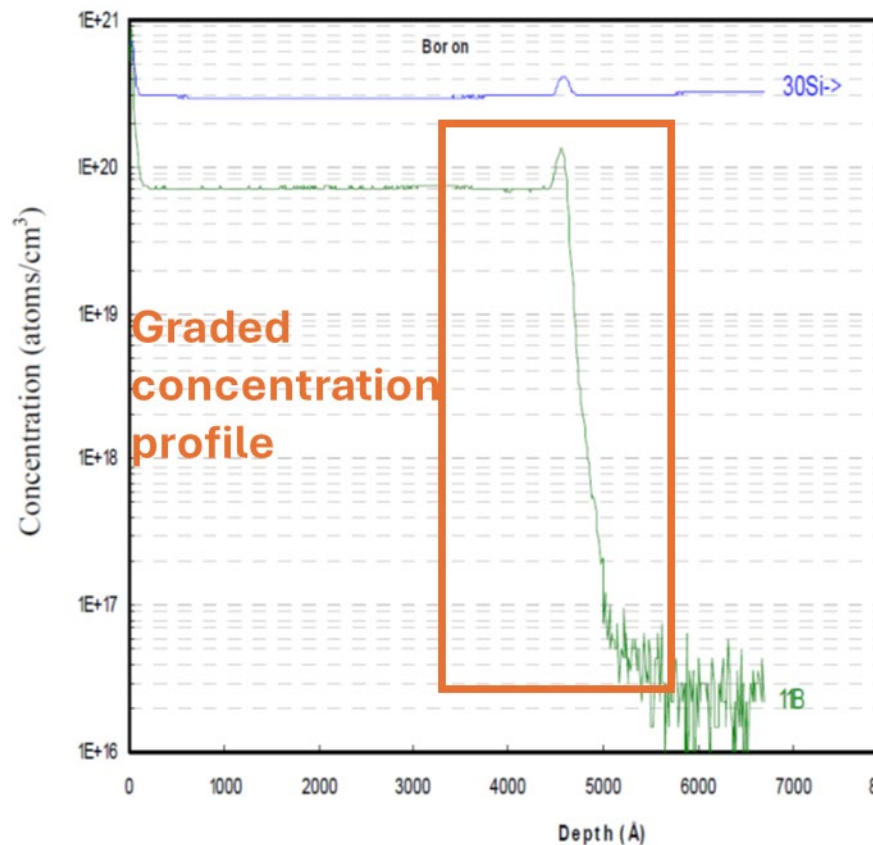
See discussion of claim 1.

b) 8[a]

See discussion of limitation 5[a].

c) 8[b]

Borden teaches or suggests that the thermal treatment facilitates the diffusion of dopants from the amorphous silicon layer (which becomes the doped polysilicon layer after crystallization) into the substrate. Borden discloses that the diffusion of dopants into the substrate creates a graded concentration profile. Ex-1006, FIG. 4; Ex-1003, ¶256. A POSITA would understand that this graded dopant concentration profile establishes a built-in electric field due to the carrier concentration gradient—forming a high-low junction.



Ex-1006, FIG. 4 (annotated).

C. Ground 3: Claims 3-4 are Rendered Obvious by Borden and Gan, Kwark, or Swanson

1. Motivation to Combine Borden and Kwark

A POSITA would be motivated to combine Kwark with Borden. Ex-1003, ¶257.

Borden teaches a two-step process for making a solar cell. The first step is to grow a thin oxide (or tunnel dielectric) layer on a crystalline silicon wafer and then an amorphous silicon containing compound is deposited on the tunnel dielectric layer. The second step is thermal treatment. Ex-1003, ¶258.

Kwark discloses a single step whereby an amorphous silicon containing compound is deposited. That compound consists of amorphous silicon oxide (SiO_x , where $x \leq 2$), and clusters of silicon surrounded by amorphous transition layers of silicon and oxygen. Ex-1010, 742. Ex-1003, ¶259. Like Borden, Kwark discloses a thermal treatment step in the temperature range of 800°C to 1000°C. Ex-1010, FIGs. 4-6. Kwark's thermal treatment induces a phase separation within the bulk of the SIPOS layer and growth of a silicon oxide layer at the interface between SIPOS and the silicon wafer. Ex-1010, 742. Ex-1003, ¶259.

Kwark discloses that a structure formed through this process features an interfacial oxide layer whose thickness is tunable by introducing a chemox layer. This structure serves as a more robust diffusion barrier and thereby suppresses bulk recombination. Ex-1010, 743; Ex-1003, ¶260.

Combining Kwark and Borden would achieve several known design goals for

solar cell manufacturing processes. Specifically, a POSITA would understand that the reduction in bulk recombination achieved through Kwark's process improves passivation in solar cells. Ex-1003, ¶261. By replacing the polysilicon deposition step in the Borden process with Kwark's process, a superior balance is achieved between passivation efficacy and suppression of dopant overdiffusion. Ex-1003, ¶261. This modification would also reduce process complexity and fabrication cost. Ex-1003, ¶262. A POSITA would also understand that Kwark's process eliminates the need for Borden's separate tunnel dielectric layer growth step. Ex-1003, ¶262.

A POSITA would be motivated to modify Borden's two-step process to achieve the advantages of reduced process complexity, reduced processing steps, higher yield, and reduced cost, while achieving the performance advantages disclosed by Kwark. Ex-1003, ¶263. A POSITA would understand that eliminating Borden's rapid thermal oxidation step would constitute a simple change in Borden's process. The CVD process was commonly used to deposit both Borden's amorphous silicon layer and Kwark's SIPOS layer. Ex-1003, ¶263. Thus, a POSITA would have combined the teachings of Borden and Kwark with a reasonable expectation of success, in order to achieve the aforementioned benefits. Ex-1003, ¶263.

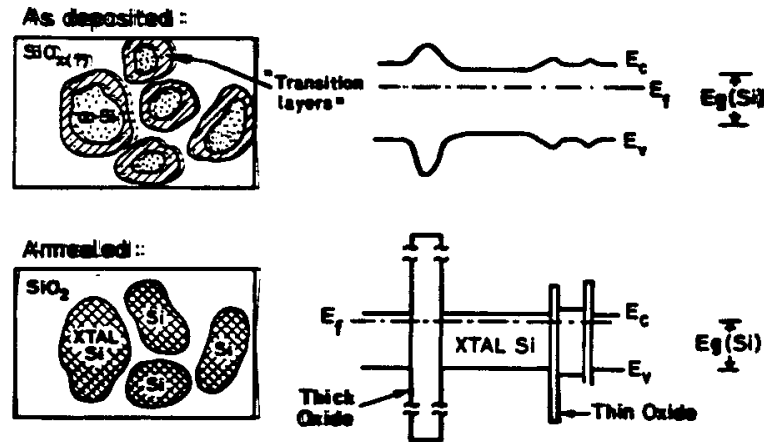


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the "oxide-like" regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Ex-1010, FIG. 3.

2. Motivation to Combine Borden and Gan

A POSITA would be motivated to combine Gan with Borden. Ex-1003, ¶264.

Both Gan and Borden disclose applying improved p-n junctions to solar cells, and both disclose that for high-efficiency solar cells, the junctions must have a low saturation current J_0 . Ex-1006, 1151-52; Ex-1009, 245; Ex-1003, ¶264. A POSITA would understand that a low J_0 is a function of the interfacial silicon oxide layer. Ex-1003, ¶264.

Borden discloses that a thermally grown oxide also yields higher open circuit voltage. Ex-1006, 1150 ("Higher values are found for the RTO dielectrics than the chem-ox, consistent with the results of figure 6, which suggests that the RTO provides

improved interface passivation.”). Borden also discloses that a “high tunnel layer thickness causes a strong series resistance problem.” Ex-1006, 1151; Ex-1003, ¶265.

Gan discloses that adjusting the processing conditions permits achieving both a low J_0 and a low ρ_c . Ex-1003, ¶266. A POSITA would understand that for optimum device performance, both a low J_0 and a low contact resistance ρ_c are required. Ex-1003, ¶266.

Therefore, as Dr. Hatalis explains, a POSITA would be motivated to combine Gan with Borden to reduce both J_0 and ρ_c . Ex-1003, ¶267. This way, a POSITA would achieve Borden’s requirement to “minimize J_0 ,” while at the same time solving one of Borden’s stated problems of high series resistance. Ex-1003, ¶267.

A POSITA would understand that applying Gan’s teachings of forming “a very small fraction of interfacial oxide breakup” in Borden’s thermal interfacial oxide would result in a robust and reproducible process that would also improve Borden’s solar cell performance as direct result of a low J_0 and ρ_c . Ex-1003, ¶268. Because Borden and Gan both disclose similar processing steps, a POSITA would understand that modifying Borden’s processing steps for forming Gan’s “very small fraction of interfacial oxide breakup” would entail simple experimentation on the growth of thermal oxide and the thermal anneal process (both steps disclosed by Borden). Ex-1003, ¶268. Thus, a POSITA would have combined the teachings of Borden and Gan with a reasonable expectation of success in order to achieve the aforementioned

benefits of a robust and reproducible process for achieving high-performance solar cells. Ex-1003, ¶268.

3. Motivation to Combine Borden and Swanson

A POSITA would be motivated to combine Swanson with Borden. Ex-1003, ¶269.

Both Swanson and Borden disclose that for high efficiency solar cells the junctions must have a low saturation current J_0 . Ex-1006, 1151; Ex-1008, 1:18-20; Ex-1003, ¶269. A POSITA would understand that a low J_0 is a function of the interfacial silicon oxide layer. Ex-1003, ¶269.

Borden discloses that a thermally grown oxide also yields higher open circuit voltage. Ex-1006, 1150 (“Higher values are found for the RTO dielectrics than the chem-ox, consistent with the results of figure 6, which suggests that the RTO provides improved interface passivation.”). Borden also discloses that a “high tunnel layer thickness causes a strong series resistance problem.” Ex-1006, 1151. Ex-1003, ¶270.

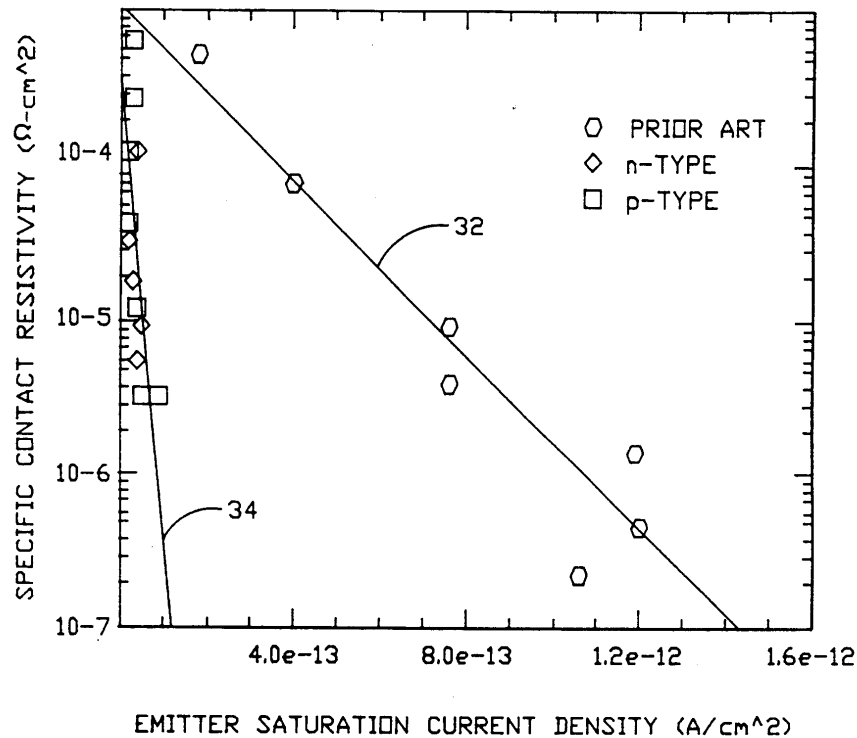


FIG.—8

Swanson, FIG. 8.

Swanson discloses that by adjusting the processing conditions, it will be possible to achieve both a low J_0 and a low ρ_c . Ex-1003, ¶271; Ex-1008, 1:32-35. Moreover, Swanson discloses that “[e]ither the anneal temperature or the annealing time can be used to control the extent of the interfacial oxide which is broken.” Ex-1008, 2:64-67, FIG. 5B; *see also* Ex-1008, 3:1-4, Ex-1003, ¶271. A POSITA would understand that the “broken areas” are depicted as element 20, since element 16 depicts Swanson’s thin “thermally grown oxide 16.” Ex-1008, 2:47-51; Ex-1003, ¶271. Swanson discloses that “the contact resistance is reduced by the presence of the broken regions

in the thin silicon oxide layer.” Ex-1008, 3:29-31, FIG. 8 (depicting in curve 34 both a low J_0 and a low ρ_c); Ex-1003, ¶271. A POSITA would understand that for optimum device performance both a low J_0 and a low ρ_c are preferred. Ex-1003, ¶271.

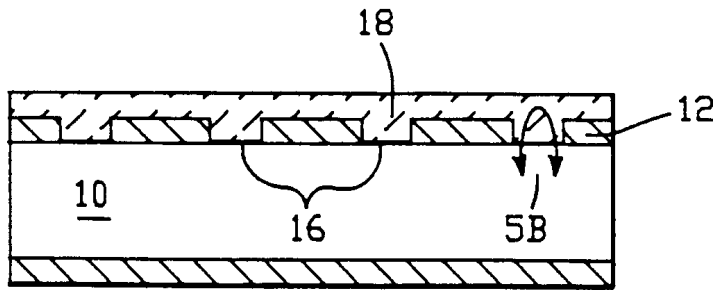


FIG.—5A

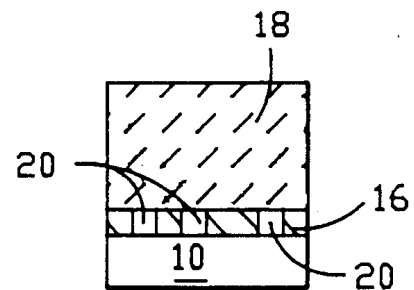


FIG.—5B

Swanson, FIGs. 5A, 5B.

A POSITA would be motivated to combine Swanson with Borden to achieve low values for both J_0 and ρ_c . This way, a POSITA would achieve Borden’s requirement to “minimize J_0 ,” while at the same time solving one of Borden’s stated problems of “high series resistance.” Ex-1003, ¶272.

A POSITA would understand that by applying Swanson’s teachings of forming “broken regions” in Borden’s thermal interfacial oxide would result in a robust and reproducible process, which would also improve Borden’s solar cell performance as direct result of a low J_0 and a low ρ_c . Ex-1003, ¶273. Because Borden and Swanson both disclose similar processing steps, a POSITA would understand that modifying

Borden's process per Swanson so that "the interfacial oxide is broken partially" would entail simple experimentation. Ex-1003, ¶273. A POSITA would have combined the teachings of Borden and Swanson with a reasonable expectation of success to achieve the aforementioned benefits of a robust and reproducible process for achieving high-performance solar cells. Ex-1003, ¶273.

4. Claim 3

a) 3[pre]

See discussion of claim 1 in Ground 2.

b) 3[a]

Borden in view of Kwark renders this claim element obvious. Ex-1003, ¶276.

Borden discloses the deposition of amorphous silicon layer on top of a tunnel oxide formed by chemical means or rapid thermal oxidation. Ex-1006 ,1149 ("use IC processing to understand the process requirements for a polysilicon emitter."); Ex-1003, ¶276. A POSITA would understand that the deposition of an amorphous silicon layer in a typical IC process is formed by the thermal decomposition of a silane (SiH_4) gas in Low-Pressure-Chemical-Vapor-Deposition(LPCVD)-type or Atmospheric-Pressure-Chemical-Vapor-Deposition (APCVD)-type reactor. Ex-1003, ¶276. As Dr. Hatalis explained, a POSITA would be motivated to modify Borden's deposition process in view of Kwark such that the substrates, after being cleaned, are loaded into the CVD reactor. And during the actual deposition process, Kwark discloses two reactant gases—silane (SiH_4) and nitrous oxide (N_2O)—will flow. Ex-1003, ¶276. Dr.

Hatalis further explained that a POSITA would understand that the thermal decomposition of SiH_4 and N_2O will result in the deposition of an amorphous silicon-containing compound called SIPOS, and the as-deposited SIPOS layer is the *amorphous silicon-containing compound* over the substrate. Ex-1003, ¶276.

Kwark discloses forming an interfacial oxide layer on a silicon substrate and forming a SIPOS film composed of a class of silicon oxides (which are silicon-containing compounds) thereon. Ex-1010, 742; Ex-1003, ¶277. Kwark also discloses that the SIPOS is not crystallized as-deposited but crystallizes during subsequent annealing. Ex-1010, FIG. 3; Ex-1003, ¶278.

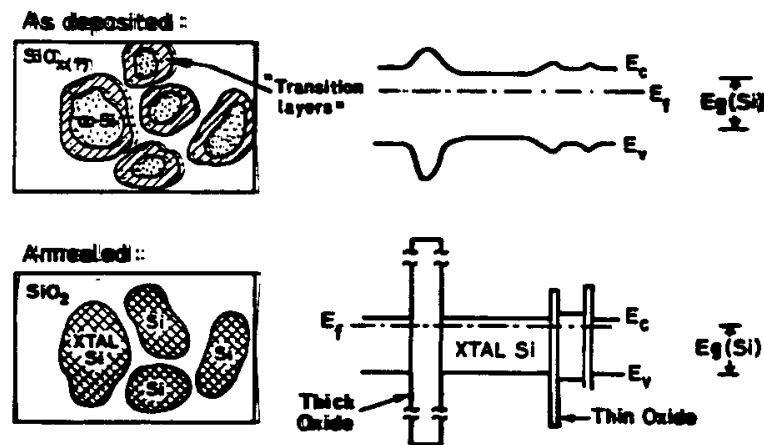


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the "oxide-like" regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Kwark, FIG. 3.

Dr. Hatalis explains that a POSITA would understand from Kwark that the

SIPOS would block hole transport and is passivating because the hole suppression means fewer holes are available for recombination. Ex-1010, 743; Ex-1003, ¶279. Kwark also discloses that the SIPOS is conductive. Ex-1010, 743 (“The addition of a dopant species converts [the SIPOS] films from semi-insulating to a form that can be made sufficiently conductive”). Ex-1003, ¶279.

Dr. Hatalis also explains that a POSITA would understand from Kwark that the interfacial oxide layer may suppress hole currents and function as an interfacial passivation layer. Ex-1010, 743; Ex-1003, ¶280.

c) 3[b]

Kwark FIG. 5 discloses that after the deposition of the SIPOS layer, a thermal treatment is conducted at a temperature in the range 800°C to 1000°C. Ex-1010, FIG. 5; Ex-1003, ¶282.

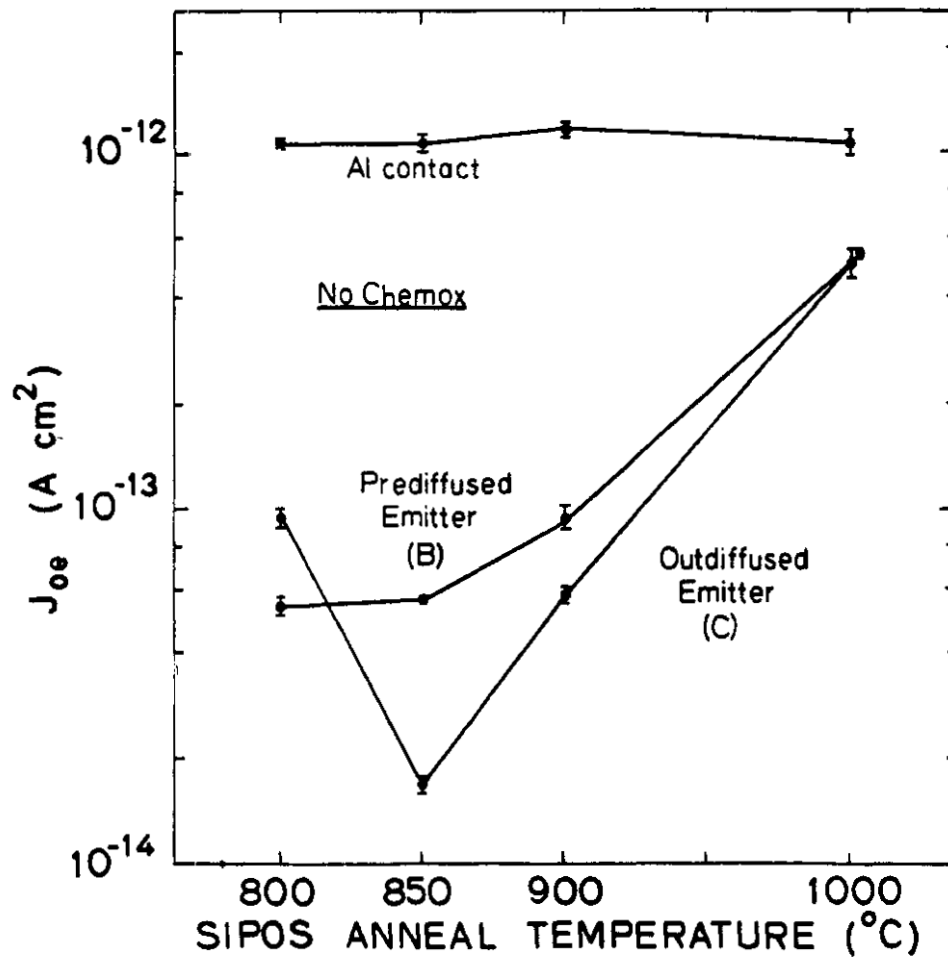


Fig. 5: emitter saturation current vs. anneal temperature for SIPOS contacts without a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

Ex-1010, FIG. 5.

Kwark further discloses that this thermal treatment induces phase separation in SIPOS to separate into a micro-crystallites layer and an interfacial oxide layer. Ex-1010, 742-743; Ex-1003, ¶283. Dr. Hatalis explained that a POSITA would understand that Kwark's thermal treatment *separates the amorphous silicon-containing compound*,

i.e., the SIPOS, into the “tunnelable interfacial oxide,” i.e., the *one interface passivation layer* and the layer that contains the “silicon microcrystallites,” i.e., the *conductive and passivation layer*. Ex-1003, ¶284; Ex-1010, 742. A POSITA would be motivated to combine Kwark’s method of simultaneously forming a conductive SIPOS layer and an interfacial oxide via annealing with Borden’s solar cell fabrication process due to the benefits of (1) enabling an optimal balance between passivation efficacy and suppression of dopant outdiffusion, and (2) simplifying the manufacturing process. *See* Section VI.C.1.

5. Claim 4

The ’074 patent does not explicitly define the morphology and formation principle of perforations. Ex-1003, ¶286. To the extent that First Solar claims that the perforations occur during carrier transport, causing the adjacent layers 1831 and 1871, as shown in the ’074 patent’s Figure 18, to make contact with the wafer 185 directly, Borden discloses that such perforations occur. Ex-1003, ¶286.

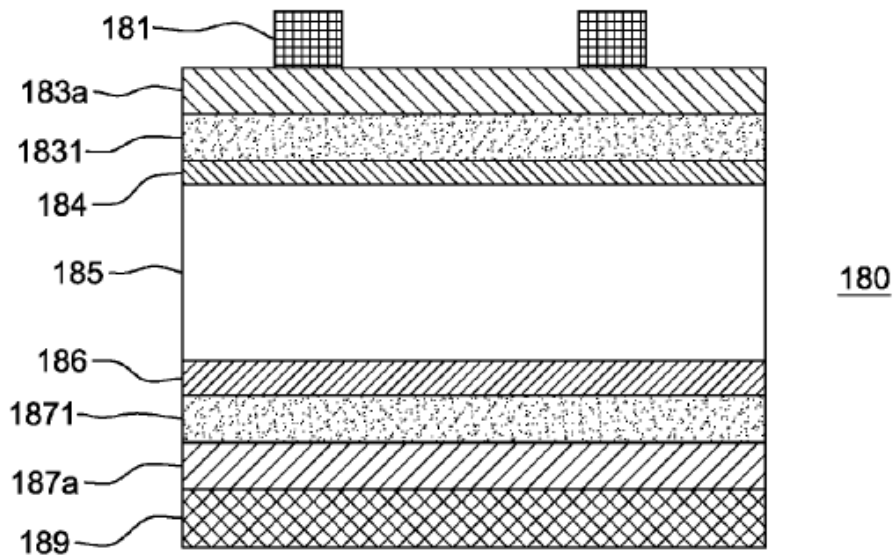


FIG. 18

Ex-1001, FIG. 18.

Borden discloses forming a tunnel dielectric layer on a substrate via the RTO method, followed by deposition of amorphous silicon and subsequent crystallization at elevated temperatures (e.g., 1000°C). Ex-1006, 1150. Ex-1003, ¶287.

Dr. Hatalis explains that a POSITA would understand that the resulting tunnel dielectrics layer becomes dense but highly brittle and the tunnel dielectrics layer develops perforations under the stress induced by thermal expansion mismatch. Ex-1003, ¶288.

This phenomenon can be corroborated by the observed phosphorus diffusion into the substrate under thermal treatment conditions, as analyzed for limitation 1(d). Borden teaches that the function of the tunnel dielectric layer is to block dopant (e.g.,

phosphorus) diffusion. Ex-1006, 1149 (“[The polysilicon emitter] requires a thin tunneling dielectric to block dopant diffusion and passivate the interface.”); Ex-1003, ¶288. Consequently, a POSITA would understand that without perforations in the tunnel dielectric layer, phosphorus dopants would be unable to penetrate through the dielectric layer and enter the substrate. Ex-1003, ¶288.

Alternatively, Borden in view of Gan renders this claim element obvious.

Gan discloses a solar cell structure with an interfacial oxide between the substrate and the polysilicon layer. Ex-1009, 245 (“It was found that, between the polysilicon and the substrate, there always exists a very thin oxide (interfacial oxide).”), Ex-1003, ¶290. As discussed for claim 1, the solar cell structure disclosed by Borden also has a similar structure, namely, a tunnel dielectric layer between the substrate and the poly layer, which is also an oxide of silicon. Ex-1003, ¶290.

Gan also discloses that “the oxide is not thermally stable; i.e., it tends to break up during high temperature anneals.” Ex-1009, 245. Gan further discloses that as the oxide breaks down under thermal treatment, “channels” are formed, allowing the substrate and the polysilicon layer to establish “intimate contacts” in these broken regions. Ex-1009, 249; Ex-1003, ¶291.

Dr. Hatalis explained that a POSITA would understand from Gan that perforations would form during the thermal treatment process. Ex-1003, ¶292. A POSITA would understand how to adjust the annealing to obtain a structure with low

ρ_c and J_0 , to get a high performance solar cell. Ex-1003, ¶292. As Dr. Hatalis explains, Borden discloses “a strong series resistance problem” and that a POSITA would “minimize j_0 and maximize lifetime” to achieve an efficient p-PE/c-Si(n) structure. Ex-1006, 1151-52; Ex-1003, ¶292. Therefore, as Dr. Hatalis explains, a POSITA seeking to create a solar cell with an efficiency that exceeds 20% would be motivated to modify the annealing conditions as Gan teaches. Ex-1003, ¶292. By modifying the thermal treatment of Borden in view of Gan, a POSITA would optimize the perforation of the oxide layer, i.e., the interface passivation layer, which will lead to easier carrier transport therethrough. Ex-1003, ¶292.

Alternatively, Borden in view of Swanson renders this claim element obvious. Ex-1003, ¶293.

Swanson first discloses *an interface passivation layer* (an “interfacial oxide 16”) layer on top of *the substrate* (silicon substrate 10). Ex-1008, 2:43-60 (In FIG. 4A...over the contact areas in contact with **the thermally grown oxide 16**. FIG. 4B is an enlarged view of the one region of a contact area showing...on the **interfacial oxide 16 formed on the surface of silicon substrate 10.**”) *See also* Ex-1008, FIGs. 4A-4B.

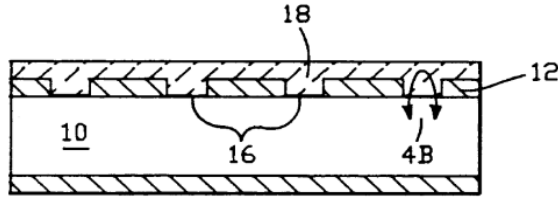


FIG.—4A

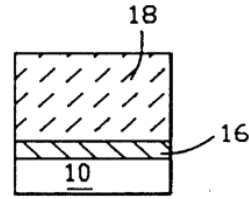


FIG.—4B

Ex-1008, FIGs. 4A and 4B.

Swanson further discloses a *thermal treatment* (over 500°C) *results in perforation of the at least one interface passivation layer* (“interfacial oxide 16”) *to allow carrier transport therethrough*. Ex-1008, 2:61-3:4 (“Thereafter as shown in FIGS. 5A and 5B the structure **is annealed at a high temperature to break the interfacial oxide and permit electrical contact between the polysilicon emitters and the underlying substrate**...For solar cell applications, **the typical anneal temperature is 1050°C**...As shown in the enlarged view of FIG. 5B, the **interfacial oxide is broken partially and polysilicon contacts the substrate intimately in the broken areas.**”) *See also* Ex-1008, FIGs. 5A-5B; Ex-1003, ¶295.

Swanson also discloses “the contact resistance is reduced by the presence of the broken regions in the thin silicon oxide layer which are created during the first anneal, as described above.” Ex-1008, 3:28-31.

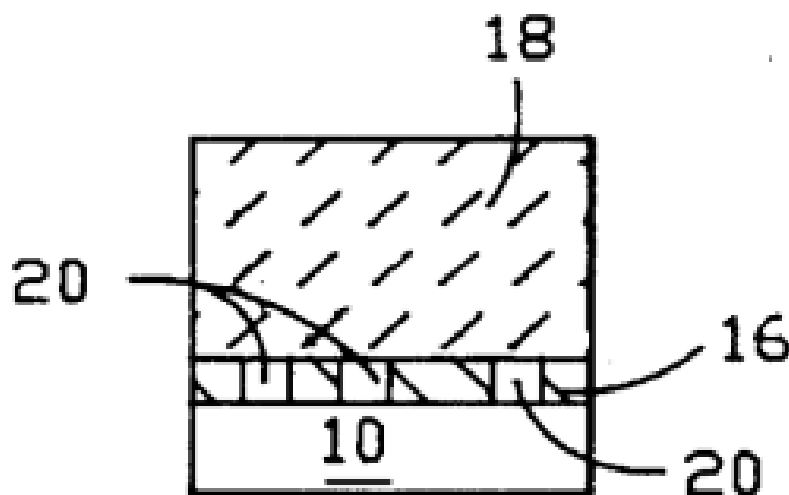


FIG.—5B

Ex-1008, FIG. 5 (annotated).

As discussed above, the interfacial oxide layer serving as a passivation layer is formed on the silicon substrate via thermal oxidation, while Borden's tunneling dielectric layer can also be generated through thermal oxidation (specifically, RTO). See discussion of claim 1[c] in Ground 2. Both Borden's and Swanson's layers consist of silicon oxide, but Swanson's longer reaction time makes its layer thicker (23 Å) than Borden's layers (8 Å and 10 Å). Ex-1008, 2:46-48; Ex-1006, 1150; Ex-1003, ¶297.

D. Ground 4: Claims 1-8 are Obvious over Rana

1. Claim 1

a) 1[pre]

Rana discloses that “[t]his invention relates generally to silicon solar cells and, more particularly, to a method for obtaining a desired dopant profile in the emitter of a solar cell device.” Ex-1007, [0002]; Ex-1003, ¶299.

b) 1[a]

Rana discloses a **crystalline silicon substrate** as a *central substrate*. Ex-1007, [0009] (“The present invention provides a method for forming an emitter in a **crystalline silicon substrate by depositing** a first lightly doped layer of amorphous silicon on a surface of the substrate.”), [0023], [0024], [0025], FIGs. 1, 2, 3, 4a-4c; Ex-1003, ¶301. In addition to the first lightly doped layer on a surface of the substrate Rana discloses also “[s]ubsequent to the deposition of the lightly doped amorphous silicon layer, a heavily doped phosphorous amorphous silicon layer is applied over the lightly doped region, as illustrated at step 14.” Ex-1007, [0027]. Rana also discloses that “additional processes such as metallization or patterning processes may be included to provide the front and rear contacts for a solar cell.” Ex-1007, [0045].

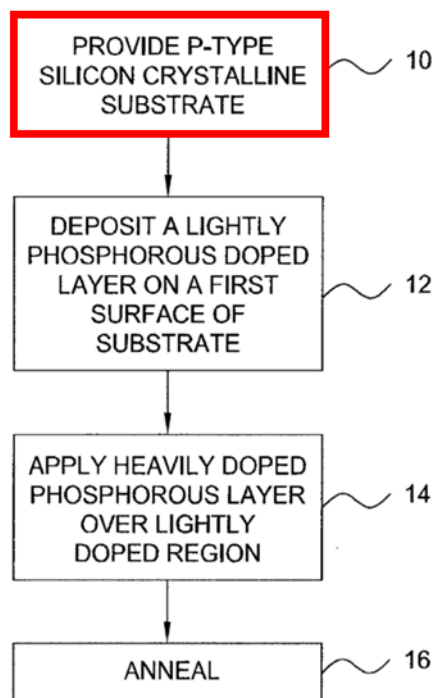


FIG. 1

Rana, FIG. 1 (annotated).

Rana discloses “[t]he substrate may be formed of single crystalline silicon or multi-crystalline silicon depending on the particular application of the product to be produced. In one embodiment, the substrate is a monocrystalline substrate (e.g., Si<100> or Si<111>).” Ex-1007, [0024]. A POSITA would understand that crystalline silicon, when utilized as a substrate material for solar cell manufacturing either as a single crystalline or as multicrystalline silicon, is conventionally provided in wafer form. Both types of silicon wafers were used extensively to manufacture solar cells. A POSITA would further understand that the crystalline silicon substrate can serve as the

central substrate, consistent with Rana's teaching of applying functional layers and metallization on both its sides.

Dr. Hatalis explains that a POSITA would understand that crystalline silicon is conventionally provided in wafer form, and the crystalline silicon substrate can serve as the central substrate. Ex-1003, ¶302.

c) 1[b]

Rana discloses depositing a **lightly doped layer of amorphous silicon** on the surface of the substrate. Ex-1007, [0009]. [0038], [0041], [0042], FIGs. 1, 3, 4a; Ex-1003, ¶304.

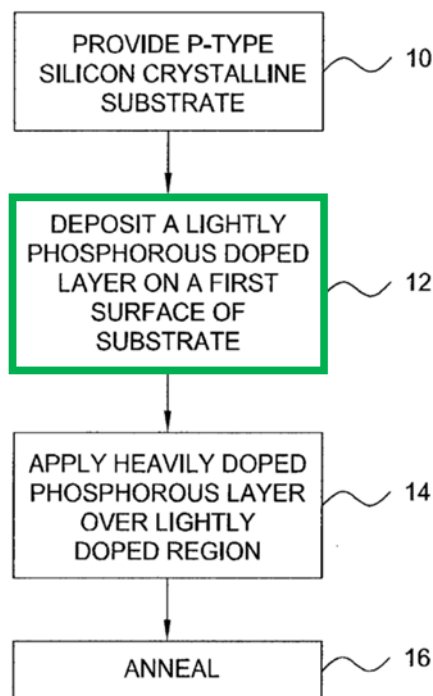
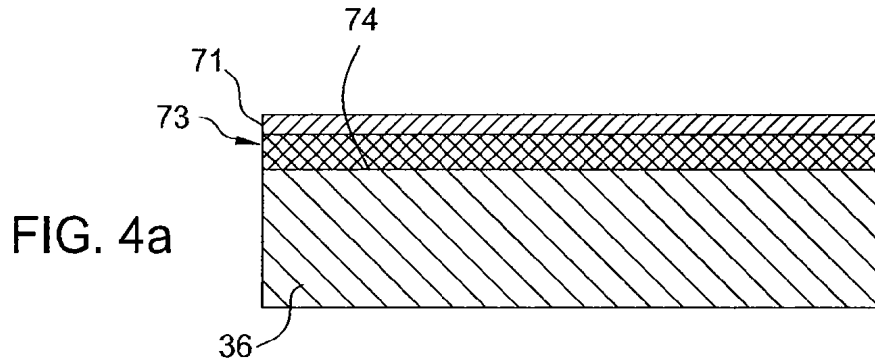


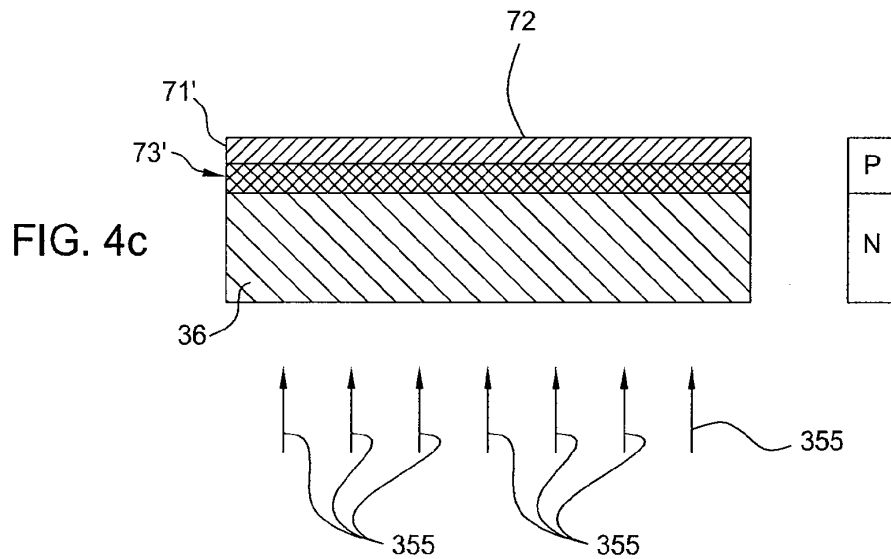
FIG. 1

Ex-1007, FIG. 1 (annotated)

A POSITA would understand that the lightly doped layer of amorphous silicon (element 73 in FIG. 4a of Ex-1007) is passivating, as Rana teaches that this layer can inhibit or reduce recombination at the interface. Ex-1007, [0023] (“The doping in the lightly doped layer is low enough so that the recombination of the minority carriers is inhibited or reduced”); Ex-1003, ¶305. Dr. Hatalis further explains that a POSITA would understand that the lightly doped layer of amorphous silicon in Rana serves a passivation function. Ex-1003, ¶305. Moreover, Rana discloses that after a subsequent thermal treatment the amorphous silicon layer 73 will crystallize and after completion of the crystallization process “the converted silicon layers 73’, 71’”, which were in amorphous state, will assume the same grain structure as the underlying crystalline silicon substrate 36 due to solid phase epitaxial growth from the first surface 74 of the substrate 36 having that grain structure.” Ex-1007, [0042], FIGs. 4a, 4c. A POSITA would understand that after the solid phase epitaxial crystallization, the crystallized silicon layer 73’ will reduce or eliminate any dangling bonds at the surface of the substrate 36 as the silicon atoms of this layer near the interface with the substrate 36 form bonds with the atoms at the surface of the silicon substrate 36, hence passivate the surface of the substrate.



Ex-1007, FIG. 4a.



Ex-1007, FIG. 4c.

Dr. Hatalis also explains that a POSITA would understand that depositing an undoped layer on the substrate is another viable design choice to provide interface passivation. Ex-1003, ¶306.

d) 1[c]

Rana discloses depositing a heavily doped amorphous silicon layer on the surface of the layer of lightly doped amorphous silicon layer. Ex-1007, [0027], [0009],

[0028], [0042], FIGs. 1, 4a; Ex-1003, ¶308.

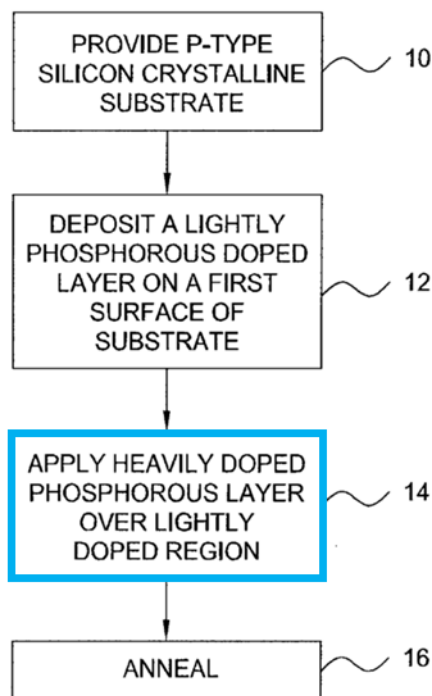


FIG. 1

Ex-1007, FIG. 1 (annotated).

A POSITA would understand that the heavily doped amorphous silicon layer is conductive. Ex-1003, ¶310. Specifically, Rana expressly teaches that this layer is doped to have the opposite “conductivity” type from the substrate. Ex-1007, Claim 2, [0023]; Ex-1003, ¶310. Rana teaches that the heavily doped amorphous silicon layer incorporates phosphorus dopants. Ex-1007, [0027]; Ex-1003, ¶310. Rana also discloses that “the concentration of the phosphorous atoms in the heavily doped layer is approximately higher than about 1×10^{19} atoms/cm³.” Ex-1007, [0034]; Ex-1003,

¶310. A POSITA would understand that the phosphorus dopants in silicon act as an n-type dopant, thereby enhancing the conductivity of the silicon. Ex-1007, [0030]; Ex-1003, ¶310.

A POSITA would understand that the heavily doped amorphous silicon layer is passivating. Ex-1003, ¶311. As discussed in Section VI.A.1.d, depositing a doped amorphous silicon layer on top of an undoped amorphous silicon above a silicon substrate can provide interface passivation. Ex-1003, ¶311. Rana teaches that its heavily doped amorphous silicon layer—when deposited on lightly doped amorphous silicon—can reduce the “dead” zone where significant recombination occurs. Ex-1007, [0023]; Ex-1003, ¶311. A POSITA would understand that such a reduction in the “dead” zone would provide passivation. Ex-1003, ¶311.

e) 1[d]

Rana discloses that after the deposition of the two amorphous layers, depicted as steps 12 and 14 in the process flow diagram depicted in FIG. 1, a thermal anneal step is performed. Specifically with respect to this thermal anneal “step 16,” Rana discloses “[a]s shown at step 16...the substrate with the lightly and heavily doped amorphous silicon layers is annealed by delivering heat energy to the substrate”. Ex-1007, [0029], FIG. 1; Ex-1003, ¶313.

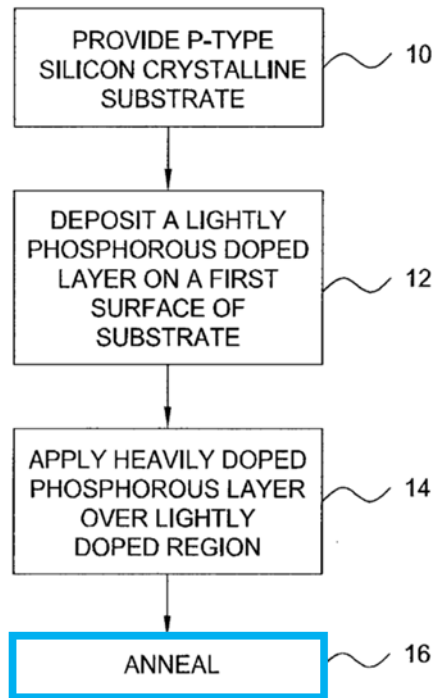


FIG. 1

Ex-1007, FIG. 1 (annotated)

Rana further that the thermal treatment is performed through “a rapid thermal processing” in which the temperature is “about 750°C. to about 1200°C” for a period that varies “from approximately 5 seconds” to a period of “over 30 minutes.” Ex-1007, [003], [0039]-[0040]; Ex-1003, ¶314.

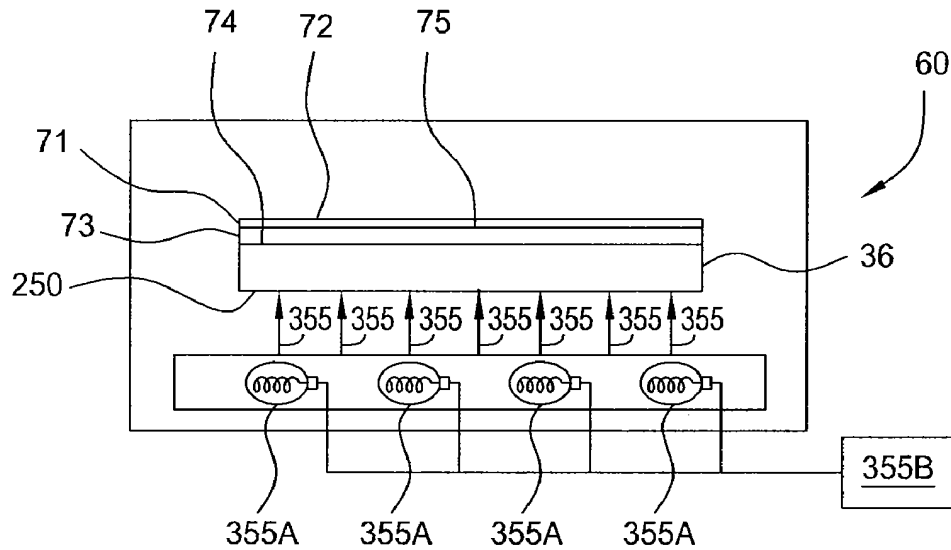
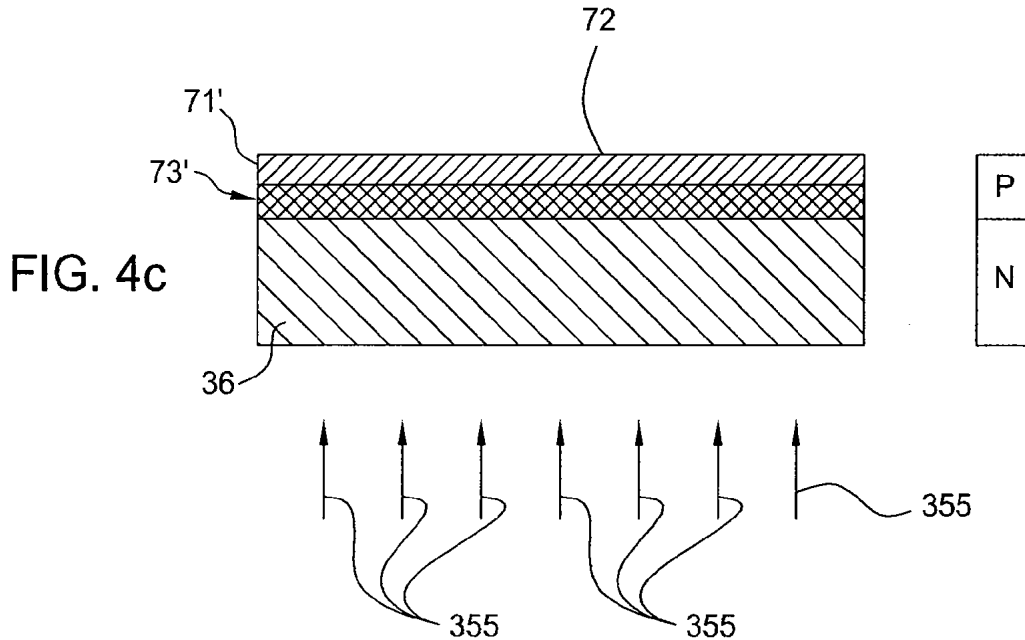


FIG. 3

Ex-1007, FIG. 3.

Rana further discloses that during the thermal treatment, the heavily doped amorphous silicon is crystallized. Ex-1007, [0010]; Ex-1003, ¶315. Rana also discloses that “[u]pon the completion of this directional crystallization process, the converted silicon layers 73’, 71’’, which were in amorphous state, will assume the same grain structure as the underlying crystalline silicon substrate 36” and that “[t]he resulting crystalline structure after heat treatment...has a consistent grain structure, as shown in FIG. 4c.” See Ex-1007, [0042]-[0043], [0013], [0029]; Ex-1003, ¶315.



Ex-1007, FIG. 4c.

Rana further discloses that during the annealing process, the heat energy facilitates diffusion of the dopants into the substrate. Ex-1007, [0042] (“the substrate 36 with the deposited amorphous silicon layers 73, 71 is annealed...at a temperature sufficient to activate and cause the dopant atoms (e.g., phosphorous) in the lightly and heavily doped amorphous silicon layers 73,71 to diffuse into the substrate 36”); Ex-1003, ¶316.

f) 1[e]

Rana teaches that the metallization provides the contacts to both the front and rear sides of the solar cell and that the metallization is performed after the thermal treatment. Ex-1007, [0045] (teaching provision of “front and rear contacts” for a solar cell); Ex-1003, ¶318. It is commonly known that contacts on solar cells typically

function as electrodes.

Dr. Hatalis explains that Rana discloses the metallization processes form the electrodes that serve as the electrical contacts on the front (or top side), and this metal electrode has an interconnected finger structure to reduce the light losses caused by reflection from the metal electrodes, while the rear metal electrode typically covers the entire back side. Ex-1003, ¶319.

In his declaration, Dr. Hatalis summarizes different embodiments in Rana as “Emitter with Desired Dopant Profile” and “Selective Emitter.” Ex-1003, ¶320. Dr. Hatalis further explains that a POSITA would understand to place the *interface passivation layer* and the *conductive and passivation layer* with respect the front (or top, i.e. light entering) side or the rear side of a solar cell. Dr. Hatalis further explains that a POSITA would also understand that Rana teaches when these layers are formed on the front side of a solar cell under the “selective emitter” embodiment; and when these layers are formed on the rear side under the “Emitter with Desired Dopant Profile” embodiment. Ex-1003, ¶¶320-323.

A POSITA would understand that such metallization occurs after thermal treatment, as Rana expressly states that metallization “follow[s] the deposition processes described above.” Ex-1007, [0045]; Ex-1003, ¶324. These “deposition processes” include “crystallizing the doped amorphous silicon layers” through thermal processing, where the heavily doped amorphous silicon layer is one of the doped

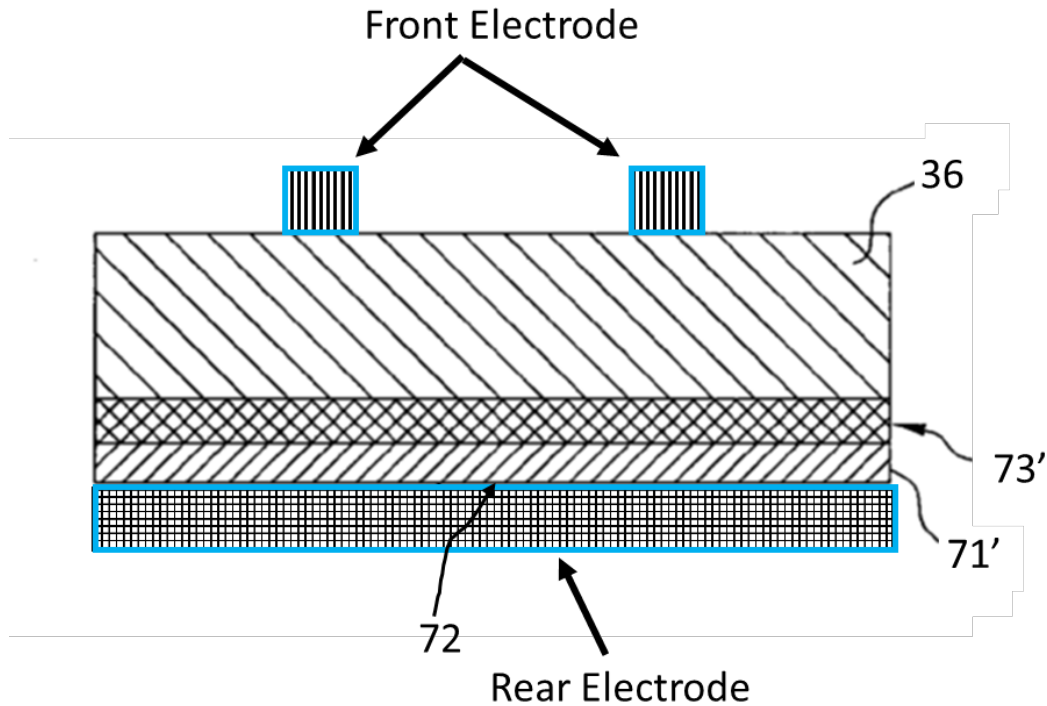
amorphous silicon layers. Ex-1007, [0009]; Ex-1003, ¶324. According to Rana's explicit disclosures, a POSITA would understand that the metallization is applied after the thermal treatment.

Rana specifically also discloses that the metallization contacts the thermal-crystallized heavily doped silicon layer, *i.e.*, the *conductive and passivation layer*. Ex-1007, [0009] (“The layer stack is then subjected to a thermal treatment that generates a selectively heavily doped surface region where the metallization is to be applied.”), *See also* [0047], [0049]. A POSITA would understand that Rana discloses the direct contact between a metal electrode and the crystallized heavily doped silicon layer (element 71' the *conductive and passivation layer*) to achieve low contact resistance. Ex-1003, ¶325.

g) 1[f]

As shown in 1[d], Rana discloses that the thermal treatment causes the dopant to diffuse into the substrate. Ex-1003, ¶327. Conductive paths for charge carriers are therefore formed via the dopant diffused from heavily doped amorphous layer (*i.e.*, the *conductive and passivating layer*) throughout the lightly doped amorphous layer (*i.e.*, the *interface passivation layer*) into the substrate. Ex-1003, ¶327-8. A POSITA would understand that this process provides shortened charge flow paths between the substrate and the electrode that contacts the thermal-crystallized heavily doped silicon layer.

As shown in 1[e], a POSITA would understand that Rana discloses a solar cell structure similar to the FIG. 3 of the '074 patent. Ex-1003, ¶329.



Ex-1007, FIG. 4c (annotated).

Dr. Hatalis further explains that Rana discloses a full contact coverage structure that inherently reduces unnecessary lateral current paths, thereby effectively shortening the charge carrier flow paths between the substrate and the electrodes. Ex-1003, ¶¶330-331.

2. Claim 2

The '074 patent describes that the antireflective layer may be silicon nitride. Ex-1001, 8:61-64, (“102: Antireflection film, refractive index in the range of $1.4 < n < 3$; thickness < 150 nm. Examples include silicon nitride”). Rana discloses the application

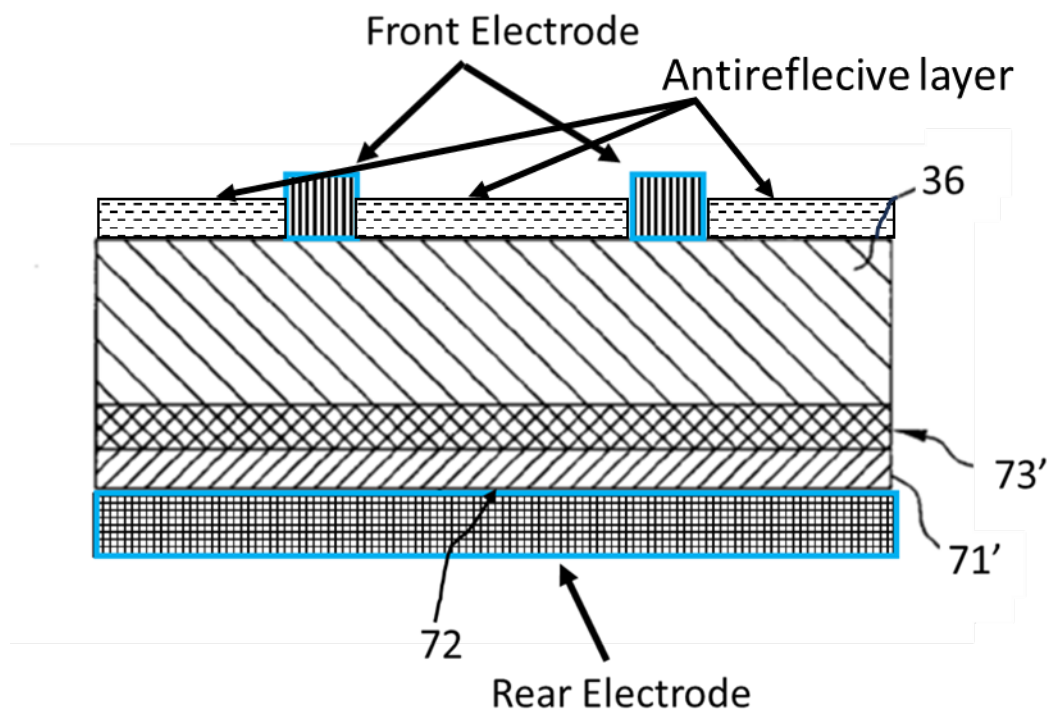
of silicon nitride on a heavily doped amorphous silicon layer. Ex-1007, [0031] (“it may be advantageous to deposit a passivation layer, for example SiN, over the heavily doped phosphorous layer”), see also *id.*, [0032], [0048], [0051]. A POSITA would understand that while Rana describes the silicon nitride layer as a passivation layer, it not only provides passivation but also offers excellent anti-reflection properties, as exemplified by the ’074 patent. Ex-1003, ¶333.

Additionally, the ’074 patent defines “a low reflective index layer for a good internal mirror on the back” as a layer with a “refractive index basically smaller than 3.0, smaller than 2.6, smaller than 2.0, smaller than 1.5.” Ex-1001, 15:31-35; Ex-1003, ¶334. As shown in 1[e], Rana discloses applying metallization as contact at the back (also referred to as “rear”) side of the solar cell. A POSITA would understand that the metallization layer on the back side as disclosed in Rana has a refractive index less than 3.0, which can redirect light back into the solar cell, thereby functioning as a good internal mirror. Ex-1003, ¶335.

Dr. Hatalis refers to Neville and Markvart to explain that it was well known that forming an antireflective layer on the light entering side of a solar cell reduces the light losses due to reduction of light lost due to reflection. Ex-1003, ¶336. It was also well known that silicon nitride is a very good antireflective layer. Ex-1003, ¶336.

Dr. Hatalis explains that a POSITA would understand that a silicon nitride layer disclosed by Rana as a surface passivation layer and an antireflective layer. Ex-1003,

¶337. Moreover, Rana discloses “additional processes such as metallization or patterning processes may be included to provide the front and rear contacts for a solar cell.” Ex-1007, [0045]; Ex-1003, ¶337. Dr. Hatalis refers to Green to explain that Rana’s solar cell structure as shown in the annotated Fig. 4c with a patterned antireflective layer formed on the front or light entering side of the solar cell was well known in the art. Ex-1003, ¶337.



Rana, FIG. 4c (annotated).

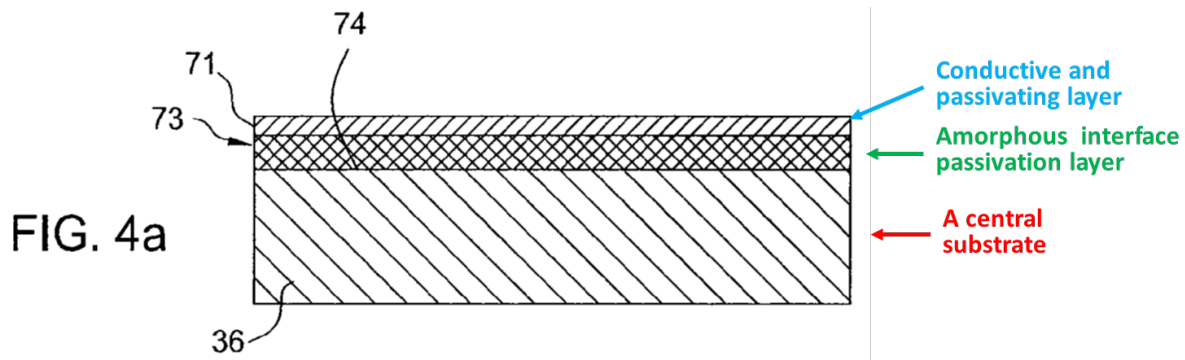
Additionally, the '074 patent defines “a low reflective index layer for a good internal mirror on the back” as a layer with a “refractive index basically smaller than 3.0, smaller than 2.6, smaller than 2.0, smaller than 1.5.” See Ex-1001, 15:31-35.

As discussed in 1[e], Rana discloses applying metallization as contact at the back (also referred to as “rear”) side of the solar cell. Dr. Hatalis explains that a POSITA would understand that the metallization layer, i.e., aluminum electrode, on the back side as disclosed in Rana Figure 2 has a refractive index less than 3.0, which can redirect light back into the solar cell, thereby functioning as a good internal mirror. Ex-1003, ¶338.

3. Claim 3

Rana discloses that both the amorphous silicon layer 73 (*interface passivation layer*) and the amorphous silicon layer 71 (*conductive and passivating layer*), depicted in FIG. 4a, are deposited in by PECVD. Rana, [0024]-[0027]; Ex-1003, ¶342.

Rana further discloses that “a plasma enhanced chemical vapor deposition (PECVD) chamber” may be “used in carrying out processes of the present invention.” Rana, [0037]-[0038]; Ex-1003, ¶343. Dr. Hatalis refers to Fuhs to explain that a POSITA would understand that the plasma deposition conditions as disclosed yield a material known as hydrogenated amorphous silicon, which is an amorphous silicon-containing compound over the substrate (element 36). Fuhs, 124; Ex-1003, ¶¶344-5.



Rana, FIG. 4a (annotated).

Dr. Hatalis also refers to Fuhs to explain that a POSITA would understand that the thermal treatment will separate the amorphous silicon-containing compound into *at least one interface passivation layer* (the crystallized layer 73) and *at least one conductive and passivating layer* (the crystallized layer 71) because it was well known that thermal treatment “usually induces a transition into the thermodynamically more stable crystalline phase.” Fuhs, 125; Ex-1003, ¶¶346-8.

Therefore, a POSITA would understand that during the thermal treatment, Rana’s initially undoped amorphous silicon layer 73 crystallizes by solid phase crystallization, which causes part of the amorphous silicon at the interface between amorphous silicon layer 73 and substrate 36 to crystallize epitaxially on the single-crystal substrate. Rana, [0030]; Ex-1003, ¶349. Moreover, Rana discloses that after the thermal treatment the initially undoped or lightly doped “amorphous silicon layer 73” has the same grain structure as that of the underlying substrate, which is distinct from the crystallized highly doped amorphous silicon layer. Ex-1003, ¶349.

Dr. Hatalis further explains that the initial highly doped amorphous silicon layer 71 crystallizes. A POSITA would understand that layer 71 is not in direct contact with the substrate thus portions of it crystallize by random nucleation and growth resulting in a different, i.e. polycrystalline, structure than the structure. Thus, the thermal treatment would separate the amorphous silicon-containing compound into the conductive and passivating layer (the crystallized layer 71') and into the interface passivation layer (the crystallized layer 73'). Ex-1003, ¶350.

4. Claim 4

Rana discloses that the thermal treatment step induces “solid phase epitaxial crystallization” of amorphous silicon layers, including the lightly doped amorphous silicon layer. Ex-1007, [0010]; Ex-1003, ¶353.

A POSITA would know that such epitaxially crystallized regions may not be continuous laterally, as residual native oxide of silicon may prevent epitaxial crystallization in certain regions. Accordingly, the epitaxially crystallized regions, which result from the *thermal treatment* in the *interface passivation layer* (Rana's element 73 or 73'), form the *perforation* as carriers would transport through these regions since the carrier mobility is higher in such single crystal regions compared to the mobility in other regions in which the solid phase epitaxy was prevented by the presence of silicon's native oxide which grows easily upon exposure of silicon to air. Ex-1003, ¶354.

5. Claim 5:

a) 5[pre]

See discussion of claim 1.

b) 5[a]

Rana discloses use of PECVD to deposit amorphous silicon layers, including the heavily doped amorphous silicon layer, on the substrate. Ex-1007, [0024], [0036], [0037]; Ex-1003, ¶358. A POSITA would understand that PECVD was a well-established process to form such amorphous silicon at the time of Borden. The PECVD process inherently forms hydrogenated amorphous silicon, an amorphous silicon-containing compound that also contains hydrogen. Ex-1003, ¶358.

c) Limitation 5[b]: “wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.”

Borden discloses the use of polycrystalline (also referred to as “multi-crystalline”) silicon as substrate. Ex-1007, [0024]; Ex-1003, ¶360. Rana further discloses that through solid phase epitaxial growth, the amorphous silicon layers—including the heavily doped amorphous silicon layer—will crystallize into the same crystal structure as the substrate. Ex-1007, [0010]; Ex-1003, ¶360.

A POSITA would understand that when the substrate is polycrystalline silicon, the heavily doped amorphous silicon will crystallize into a heavily doped polycrystalline silicon film—i.e., the crystal structure of the substrate—after solid-phase epitaxial growth occurs. Ex-1003, ¶361. A POSITA would also understand that

random nucleation within the heavily doped amorphous silicon layer will also result in regions that are polycrystalline after the crystallization is complete.

6. Claim 6:

a) 6[pre]

See discussion of claim 1.

b) 6[a]

See discussion of limitation 5[a].

c) 6[b]

Rana discloses that the doped polysilicon layer is initially amorphous silicon and is crystallized through thermal treatment. See discussion of limitation 1[d]. A POSITA would understand that thermal treatment enhances optical transmission in polycrystalline silicon. *See* Section VI.A.5.b; Ex-1003, ¶367.

7. Claim 7:

a) 7[pre]

See discussion of claim 1.

b) 7[a]

See discussion of limitation 5[a].

c) 7[b]

Rana discloses that thermal treatment (e.g., annealing) can simultaneously induce crystallization and activate phosphorus dopants. Ex-1007, [0029] (“the annealing is accomplished in a manner which will cause the amorphous layer to

directionally crystallize...while at the same time achieving the desired activation of the phosphorous atoms”), *see also id.*, [0042], [0047]-[0049]; Ex-1003, ¶373.

8. Claim 8

a) 8[pre]

See discussion of claim 1.

b) 8[a]

See discussion of limitation 5[a].

c) 8[b]

Rana discloses that during the crystallization of the amorphous silicon layers (including the heavily doped amorphous layer), phosphorus dopants diffuse into the substrate, thereby forming a “p-n junction.” Ex-1007, [0023], [0030]; Ex-1003, ¶¶379-80.

VII. CONCLUSION

Petitioner respectfully requests institution of *inter partes* review and cancellation of the challenged claims of the '074 Patent.

Date: July 18, 2025

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Counsel for Petitioner

CERTIFICATION UNDER 37 C.F.R. § 42.24(D)

I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 13,874 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: July 18, 2025

/Scott C. Weidenfeller/
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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6 and 42.105, I hereby certify that on July 18, 2025, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,130,074, together with its supporting exhibits, and Power of Attorney was served by Federal Express with Saturday delivery, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record as listed on USPTO Patent Center:

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A courtesy copy was also served via electronic mail on Patent Owner's counsel of record in the related District Court matter:

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APPENDIX A: THE CHALLENGED CLAIMS OF THE '074 PATENT

Claim Limitation #	Limitation
1[pre]	A method of fabricating a solar cell, comprising;
1[a]	providing a wafer as a central substrate;
1[b]	depositing or growing at least one amorphous interface passivation layer over the substrate;
1[c]	depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant,
1[d]	providing thermal treatment at a temperature of above 500°C. or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer; and,
1[e]	providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof
1[f]	wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.
2	The method of claim 1, further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.
3[pre]	The method of claim 1,
3[a]	wherein the depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer comprises depositing an amorphous silicon-containing compound over the substrate
3[b]	and the providing thermal treatment of about 500°C. or higher separates the amorphous silicon-containing

	compound into the at least one interface passivation layer and the at least one conductive and passivating layer.
4	The method of claim 1, wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.
5[pre]	The method of claim 1,
5[a]	wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and
5[b]	wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.
6[pre]	The method of claim 1,
6[a]	wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and
6[b]	wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer and increases the optical transmissivity.
7[pre]	The method of claim 1,
7[a]	wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and
7[b]	wherein the thermal treatment activates doping atoms in the compound.
8[pre]	The method of claim 1,
8[a]	wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound and
8[b]	wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.