

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

JinkoSolar Co., Ltd.,
Petitioner,

v.

First Solar, Inc.,
Patent Owner.

Case No. IPR2025-01130
Patent No. 9,130,074

**DECLARATION OF DR. MILTIADIS HATALIS IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,130,074**

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I. INTRODUCTION

1. I, Miltiadis Hatalis declare as follows.

2. I have been retained as a technical consultant on behalf of JinkoSolar Co., Ltd. (“Jinko” or “Petitioner”), which I understand to be the petitioner in the present proceeding. I have been asked to consider whether the references listed as Exhibits 1004-1028 below disclose or render obvious the limitations recited in claims 1-8 of U.S. Patent No. 9,130,074 (Ex. 1001, “’074 patent”). I have also been asked to consider the state of the art and the “prior art,” i.e., references available before the time of the alleged invention of the ’074 patent. My opinions are provided in this declaration.

3. I am being compensated at my standard consulting rate for my time. My compensation is in no way contingent on the results of these or any other proceedings relating to the ’074 patent.

II. BACKGROUND AND QUALIFICATIONS

4. My complete qualifications and professional experience are described in my academic *curriculum vitae*, a copy of which is provided as Appendix A of my declaration. The following is a summary of my most relevant qualifications and professional experience.

5. I am currently a Professor in the Department of Electrical and Computer Engineering at Lehigh University. I hold a B.S. degree in physics from Aristotle

University, Greece, an M.S. degree in electrical engineering from SUNY Buffalo, and a Ph.D. (1987) in electrical engineering from Carnegie Mellon University. In 1987, I joined Lehigh University as an assistant professor in the Department of Electrical & Computer Engineering. I served as an associate professor at Lehigh University from 1991 to 1995, and have been a full professor at Lehigh University since 1995. From 1988 to 1993, I served as associate director of the Microelectronics Research Laboratory at Lehigh University. From 1992 to 2018, I served as director of the Display Research Laboratory at Lehigh University. From 2010 to 2013, I also served as interim director of the Sherman Fairchild Center for Solid State Studies at Lehigh University. From 2003 to 2008, I concurrently served as a professor in the Department of Computer Science at Aristotle University, Greece.

6. From 1987 to 2015, I also worked as an independent consultant for a number of major technology companies in the flat panel display and semiconductor field, including IBM, Kodak, Sharp, Air Products and Motorola Solutions. In 1992, I was a visiting scientist at XEROX Palo Alto Research Laboratory. This industry work was related to electronic materials, semiconductor devices and their application to microelectronic systems.

7. I am the author or co-author of 180 technical publications including three issued patents, and two book chapters, including one on AMOLED pixel electronic

circuits and one on polysilicon TFT technology. As of this writing, I have a total of 4,822 citations and my h-index is 30 according to Google Scholar.

8. In 1992, I established and became director of a clean room facility dedicated to research and development of electronic thin film materials and devices, for flat panel displays, flexible electronics, photovoltaic energy systems and novel large area microelectronic system applications. I have raised over \$13 million through research contracts and grants to support my research activities in these areas. These contracts and grants were funded by the Defense Advanced Research Program Agency (DARPA), the Army Research Laboratory (ARL), the National Science Foundation (NSF), the National Aeronautics and Space Administration (NASA), the State of Pennsylvania, and a variety of industrial companies including Corning, IBM, Kodak, Sharp, Northrop Grumman, and others.

9. From 1984 to present I have conducted research in microelectronics, including semiconductors, electronic materials, devices and circuits for integrated circuits and integrated microsystems. My research mainly focuses on electronic thin film materials and devices, microelectronic fabrication processes, novel electronic circuits, and integrated microsystems. My research group pioneered the development of electronic materials, devices, and circuits on flexible substrates, active matrix organic light emitting diode displays, and addressable arrays for integrated sensor applications such as fingerprint sensors for biometrics and multichannel gas sensors.

10. As a faculty member, I supervised the research of twenty Ph.D. dissertations in the technical field of semiconductors/microelectronics from 1989 to 2016. Upon graduating, all twenty of my Ph.D. graduate students moved either to industrial positions in the electronic or flat panel display industry, including positions at Apple, IBM, Intel, Sharp, TSMC, and Motorola, or into academic positions in the United States or abroad. I have also supervised the research of several post-doctoral researchers and research associates at Lehigh. Moreover, I have supervised many graduate student Master's theses and numerous undergraduate research projects. I have been an invited lecturer at numerous universities, industrial laboratories, and conferences in the United States and overseas.

11. The list of peer-reviewed journals in which my papers were published include Thin Solid Films, Journal of the Electrochemical Society, Solid State Electronics, Journal of Applied Physics, Journal of the Society for Information Display, Journal of Materials Science, and multiple IEEE journals including the IEEE Journal of Display Technology, IEEE Transactions on Electronic Devices, IEEE Solid State Circuits, and IEEE Electron Device Letters. The technical conferences where my papers were presented have been organized by scientific societies including: Society of Information Display (SID), Materials Research Society (MRS), Electrochemical Society (ECS), and Institute of Electrical and Electronics Engineers (IEEE).

12. I am also a named inventor on U.S. Patent No. 8,390,536, directed to controlling current to pixels in an active matrix display by adjusting voltage on the data lines and two international patents, as foreign counterpart patents, associated with the above invention, one issued in Korea and one in Japan.

13. I have taught a number of different undergraduate and graduate level courses in the Electrical and Computer Engineering department at Lehigh University. These courses have generally centered on physics, technology, and the design and fabrication of solid-state devices and integrated circuits. I have also introduced several new courses which include “Introduction to VLSI Design,” “Semiconductor Material and Device Characterization,” and “Introduction to Photovoltaic Energy Systems.” I also regularly teach the “Principles of Electrical Engineering,” “Introduction to Computer Engineering,” “Electronic Circuits,” and “Introduction to VLSI Circuits” courses.

14. As part of my research, I utilize much of the same equipment and many of the same microfabrication processes that are in use by the semiconductor, solar cell and flat panel display industry including: Plasma-Enhanced Chemical Vapor Deposition (PECVD) for the deposition of hydrogenated amorphous silicon, silicon nitride and silicon dioxide films; Low Pressure Chemical Vapor Deposition (LPCVD) for the deposition of amorphous and polycrystalline silicon, sputter and e-beam deposition tools for aluminum, copper, nickel tungsten, titanium, gold, tantalum, and

other metallic thin films; photolithographic tools for defining photoresist patterns on the substrates; as well as reactive ion etching or wet etching tools for removing various thin film materials from the substrates. I also utilize several tools for the characterization of the materials and structures used in microelectronic devices including: optical microscopes, Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), and Atomic Force Microscopy (AFM). I further utilize a variety of electrical characterization techniques and instruments for testing the electrical performance of completed electronic circuits and systems.

15. During my Ph.D. dissertation research (1984-1987) and continuing that research as a faculty at Lehigh (1987-1995), I pioneered the solid phase crystallization of amorphous silicon at low temperatures. Similar techniques have been used in the manufacturing of integrated circuits, solar cells and flat panel displays during the last 30 years. In addition, my research group at Lehigh pioneered the fabrication of electronic devices and circuits on novel flexible substrates and the development of integrated microsystems on flexible substrates, including active matrix organic light emitting diode displays, solar cells and addressable arrays for integrated sensor applications such as fingerprint sensors for biometrics and multichannel gas sensors. Many industrial and academic laboratories currently pursue similar research activities; such research flows from the accomplishments of my research group in this technical field.

16. I am a member of several professional organizations including the Electron Device Society of the IEEE and the SID. I have also been the chair or co-chair at numerous national and international conferences and symposiums, including several SID-sponsored Workshops on Active Matrix Liquid Crystal Displays and a Materials Research Society Symposium on Flat Panel Displays. I have co-authored two book chapters, one dealing with the “Polysilicon TFT Technology” and another on the application of “Polysilicon TFTs in AMOLED Displays.” I have served as a reviewer for technical papers submitted to several scientific journals and have also served as a reviewer for several years for the National Science Foundation Small Business Innovative Research (SBIR) program.

17. A full list of my publications, education and professional experience, research grants, Ph.D. dissertations for which I served as advisor, and litigation cases in which I served as a technical expert, can be found in my *curriculum vitae* attached as appendix A.

III. MATERIALS REVIEWED

18. I am not an attorney. However, I have substantial experience analyzing patents from the perspective of a person skilled in the art. *See* Section VI.C below for the level of ordinary skill in the art applied in this declaration.

19. In forming the opinions set forth in this declaration, I reviewed the '074 patent, including the claims of the patent in view of the specification; the prosecution

history of the '074 patent; and various publications and technical references from and preceding the time of the alleged invention. More specifically, I have reviewed each of the reference as listed in Appendix B:

IV. RELEVANT LEGAL STANDARDS

20. I have been informed about certain aspects of the law relevant to my opinions. I have applied the following understanding of the law.

21. I have been informed that a patent claim may be “anticipated” if each element of that claim is present either explicitly or inherently in a single prior art reference, and that the elements of the claim are arranged in the reference in the same way as the claim. I have further been informed that for a claimed limitation to be inherently present, the prior art need not expressly disclose the limitation as long as the claimed limitation necessarily flows from a disclosure in the prior art.

22. I have been informed that, even if all of its elements are not disclosed in a single prior art reference, a claim can be unpatentable as “obvious” if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a person of ordinary skill in the art at the time the application was filed.

23. I have been informed that the question of whether a claim would have been obvious is answered through application of several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

24. I have been informed that a single reference can render a patent claim obvious if any differences between that reference and the claims would have been obvious to a person of ordinary skill in the art. Alternatively, the teachings of multiple references may be combined in the same way as disclosed in the claims, if the combination would have been obvious to one having ordinary skill in the art.

25. To determine whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, and when combined, would yield predictable results;
- whether a person of ordinary skill in the art could implement a predictable variation, and would see the benefit of doing so;
- whether a person of ordinary skill in the art could choose from a finite number of identified, predictable solutions with reasonable expectation of success;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by those skilled in the art;
- whether a person of ordinary skill would have recognized a reason to combine known elements in the manner described in the claim;

- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

26. I have been informed that one of ordinary skill in the art possesses ordinary creativity and is not an automaton. I have been informed that in considering obviousness, one should not to determine obviousness using the benefit of hindsight derived from the patent being considered.

27. I understand that certain so-called “real world” factors may also, in some cases, be indicative of non-obviousness. These factors are sometimes referred to as “objective indicia” or “secondary considerations.” I understand that such factors include:¹

- the commercial success of the claimed invention;
- the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;
- failed attempts to solve the problem solved by the claimed invention;
- copying of the claimed invention;
- unexpected results of the claimed invention;

¹ I am not aware of any objective evidence of non-obviousness having been identified in connection with the '074 patent.

- praise for the claimed invention by others in the relevant field; and
- willingness of others to accept a license under the patent because of the merits of the claimed invention.

V. TECHNOLOGY BACKGROUND

28. A solar cell is an electronic device that converts sunlight directly into direct current (DC) electricity. As far back as 1954, front-page headlines in the *New York Times* and the *Wall Street Journal* “heralded to the world the demonstration of the first reasonably efficient solar cells, an event made possible by the rapid development of crystalline silicon technology for miniaturized electronics. Since that time, the majority of solar cells fabricated to date have been based on silicon in monocrystalline or large-grained polycrystalline form.” Green, 149.

29. A typical solar cell is a semiconductor device that comprises two different regions within a semiconductor material, where one side is denoted as the “p-type region” and the other as the “n-type region,” as explained below. Such a device is called a “p-n junction diode.”

30. In the n-type semiconductor region, the majority of electrical carriers are electrons, which are negatively charged; at equilibrium (i.e., in the dark), the concentration of electrons is equal to the concentration of n-type dopants, such as phosphorus (P), when the semiconductor is silicon. In the p-type semiconductor region, the majority of the electrical carriers are “holes,” which are positively charged and

correspond to the absence of electrons where an atom can accept them; at equilibrium (i.e., in the dark), the concentration of holes is equal to the concentration of p-type dopants, such as boron (B), when the semiconductor is silicon (Si). A p-n diode device has a built-in electric field within a region known as depletion region and which extends within both the p-region and the n-region up to a certain distance away from the metallurgical junction, i.e. the location where the p-region and n-region meet. When sunlight strikes a solar cell, photons with sufficient energy create extra electrical carriers, which are formed as electron-hole pairs; in other words, for each absorbed photon, an extra electron and an extra hole are created.

31. If a photon is absorbed in the p-type region, the hole that will be created is a majority carrier, thus it is safe because it will be surrounded predominantly by other holes. However, the electron is a minority carrier and is at risk of recombining with a hole, as it is surrounded by many other holes, which in a p-type region are the majority carriers. If recombination occurs, the electron and a hole are annihilated, and no electricity is generated, even though a photon was absorbed. However, if the electron moves through the material and enters the depletion region, then due to the built-in electric field within the depletion region, it is pushed into the n-side. It remains safe there, as it becomes part of the majority carrier population surrounded predominantly by other electrons. When an electron that is created or generated in the p-region is collected by the n-region, it gives rise to an extra negative charge in the n-

region, and the corresponding hole that was created, and remained in the p- region, gives rise to an extra positive charge in the p-region. The reverse occurs when a photon is absorbed in the n-region, i.e., the electron remains in the n-region while the hole either recombines with an electron or crosses into the p-side; when the latter occurs, an extra negative charge builds in the n-side and an extra positive charge in the p-side. As more photons are absorbed and the electrons that are generated remain or are collected by the n-region while the holes remain or are collected by the p-side, then negative charge builds on the n-side and positive charge builds on the p-side.

32. The above describes the photovoltaic phenomenon where the absorption of photons and the subsequent separation of carriers by the built-in electric field present within the p-n diode device give rise to a voltage difference between the n- and the p- regions, thus making the solar cell act as a battery. If a circuit is formed by connecting the n-side to the p-side through an electrical load, then electrons flow from the n-side to the p-side, resulting in a flow of current through the load and thus generating electric power. Solar cells, like batteries, can be connected in series or parallel in order to increase the voltage or the current that would flow to the load. Typically, a number of solar cells are connected to form a photovoltaic panel, either in series or in parallel. The module thus formed has a specific electric power rating, and the modules may be tiled to form arrays.

33. In summary, a solar cell is a p-n junction device, in which the built-in electric field serves to separate the charge carrier pairs that are generated by the absorption of photons, driving electrons to the n-region and holes to the p-region. *See* Markvart, 83 (“In an ideal p-n junction solar cell, the junction (or depletion) region serves as a lossless mechanism for extracting and separating the minority carriers from the quasi-neutral regions - the base and the emitter.”) This separation of charge creates a voltage, and if the cell is connected to an external load, a current will flow, generating power.

34. The performance of a solar cell is characterized by three key parameters: the short-circuit current (I_{sc}), the open-circuit voltage (V_{oc}), and the fill factor (FF). The maximum power that a solar cell can provide (P_{max}) is the product of these three parameters. In an ideal solar cell, i.e., when the series resistance (R_s) of the solar cell is zero and the shunt resistance is infinite, the open circuit voltage is given by the following equation, where I_{ph} is the photogenerated current and I_0 is the diode’s saturation current:

$$V_{oc} = \frac{k_B T}{q} \ln \left(1 + \frac{I_{ph}}{I_0} \right)$$

The short circuit current is equal to the photogenerated current, $I_{sc} = I_{ph}$, and the fill factor, FF, increases as the open circuit voltage increases. *see*, e.g., Markvart, 72-75.

For these reasons, a POSITA at the time of the invention would, generally speaking, aim to make design choices that would reduce the diode's saturation current I_0 (or saturation current density J_0 which is equal to $J_0 = I_0/A$ where A is the area of the p-n junction, typically equal to the area of the solar cell) and the diode's series resistance R_s . "The saturation current density of an emitter, J_0 , represents the sum of all the recombination mechanisms inside the emitter. It includes the SRH, surface, contact, and Auger recombination mechanisms, as well as heavy doping effects such as band gap narrowing." Verlinden, 450. Many factors contribute to a solar cell's series resistance, one of which is the series resistance of the emitter region (R_e). In a wafer based solar cell the substrate is the "base region" and "the emitter region" is the region formed during processing by doping opposite to the doping type of the substrate, e.g. for a p-type substrate the emitter region is n-type. Markvart, 91. Increasing the series resistance is detrimental to a solar cell's performance, as it would degrade the fill factor (FF) and thus reduce the power produced by the solar cell. Markvart, 75-80, FIGs. 15, 6a.

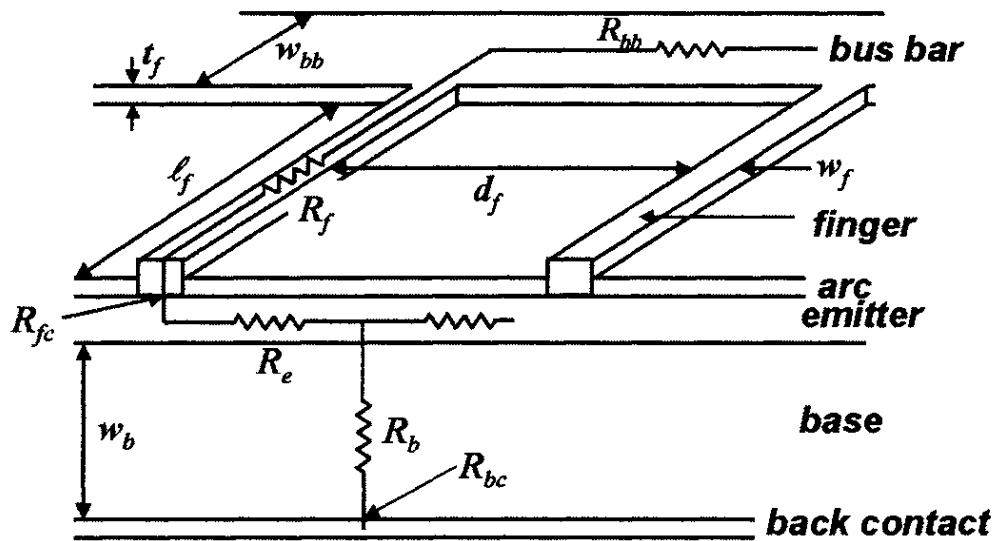
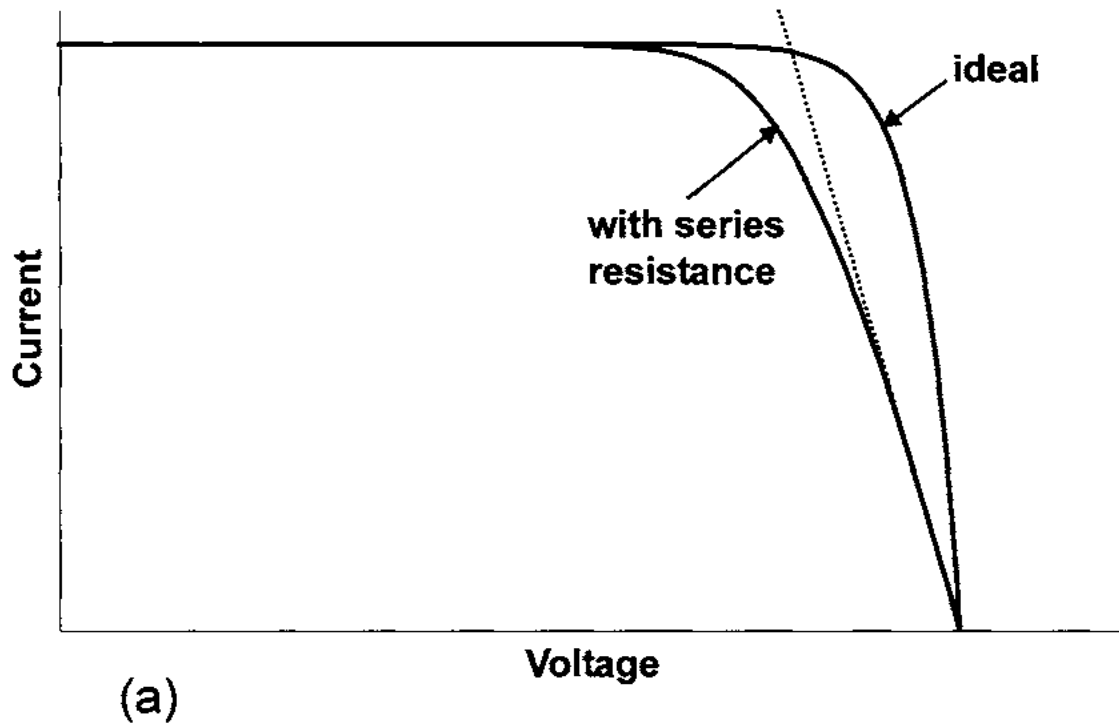


Figure 15 Components of the series resistance in a p-n junction solar cell (after [32] and [33]).

Markvart, FIG. 15.



Markvart, FIG. 6a.

35. “Many types of solar cell structures have been developed, based on various semiconductor materials, including II-VI or III-V compounds. Silicon was the first material used and is likely to remain the most suitable candidate for the next 20 years of large-scale applications. The reasons for this success are the great availability, technical advances, and environmental safety of silicon. Solar cells produced from cast multicrystalline silicon (large-grain polycrystalline silicon, referred to as mc-Si) can be considered as the only present-day technology capable of achieving low-cost high-rate production without excessive loss of efficiency compared with single-crystal silicon (sc-Si).” Muller, 73. As Muller’s FIG. 5.2 depicts, mc-Si comprised over 56% of the material used in solar cell production worldwide. “Multicrystalline silicon wafers are used exclusively to produce solar cells. Such wafers have the advantage of being cost-effective compared with single crystal wafers.” Muller, 84.

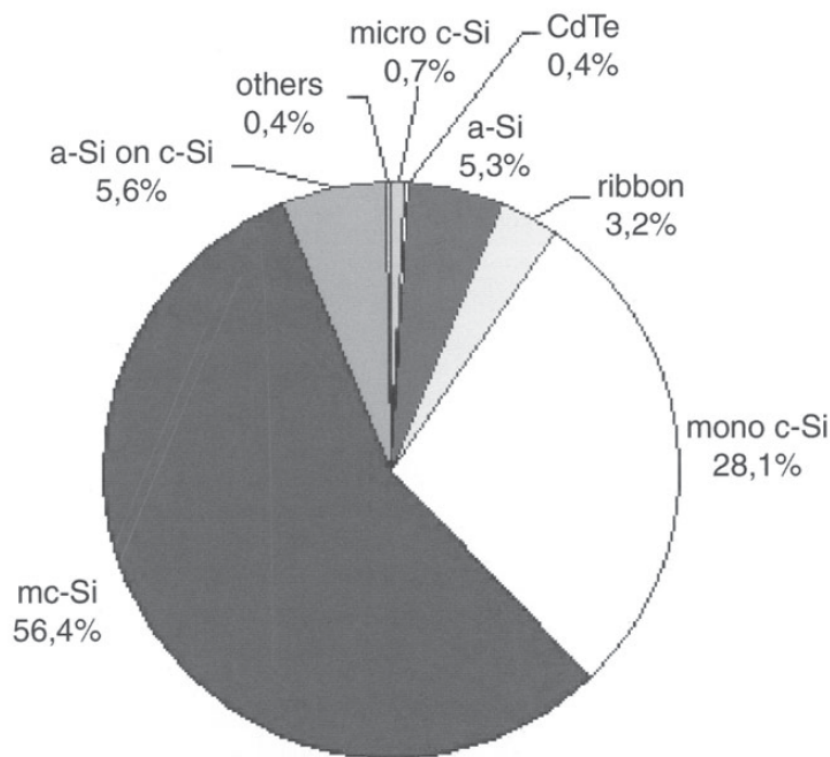


Fig. 5.2. Illustration of the percentage of the different type of materials in the total world production: The share of silicon in the total world product is still 99%, with more than 55% of it being cast mc-Si ingots [2]

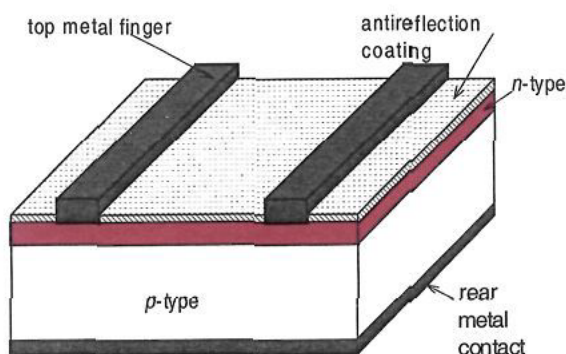
Muller, FIG. 5.2.

36. As stated above, the p-n junction in a conventional solar cell provides the mechanism for separating the light-generated charge carriers. A p-n junction is formed at the interface between a p-type and an n-type semiconductor. In silicon solar cells, this is typically achieved by diffusing phosphorus (an n-type dopant) into a boron-doped (p-type) silicon wafer. However, this diffusion process was known to have two drawbacks. First, it is expensive because it requires a long process at high temperatures. Second, the diode that results when the emitter region is contacted directly with a metal as shown in the figures below has a relatively high saturation current density (J_0) and

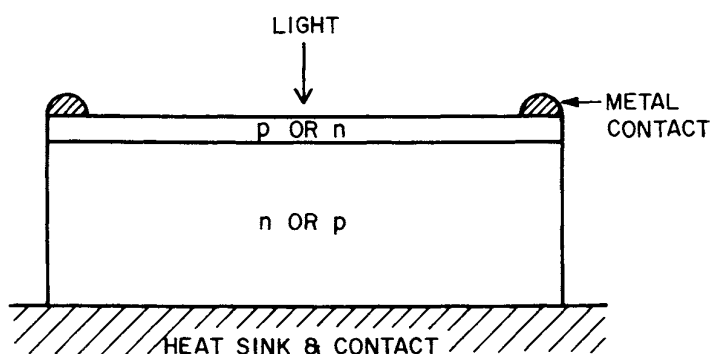
thus low open circuit voltage (V_{oc}). *See e.g.*, Verlinden, 450. “The best diffused emitter J_0 that can be achieved is around 2×10^{-14} A/cm². However, such an emitter is very transparent, which means that, if a metal contacts it, its saturation current density dramatically increases about 100-fold.” *Id.* [?] Thus, alternate approaches were reported, in which a doped silicon compound layer is deposited on a substrate at low temperatures; such processes will be discussed in more detail in the various grounds. *See id.*, 451 (“There are only two materials that were reported to have low J_0 : polysilicon emitters and semi-insulating polysilicon emitters (SIPOS), both used with an interfacial thin oxide layer.”). In such structures, it was known to form break-up regions in the oxide in order to reduce the series resistance. *See id.*, 451 (“The growth of a thin (10 to 20 Å) interfacial layer of silicon dioxide is critical to obtain low emitter saturation current density with polysilicon. However, in order to achieve a low contact resistance, it is necessary to anneal the polysilicon emitter to break up the oxide layer on about 1% of the contact area [23]. The trade-off between J_0 and a high contact resistance is highly dependent on the oxide thickness and the anneal (or breakup) step.”)

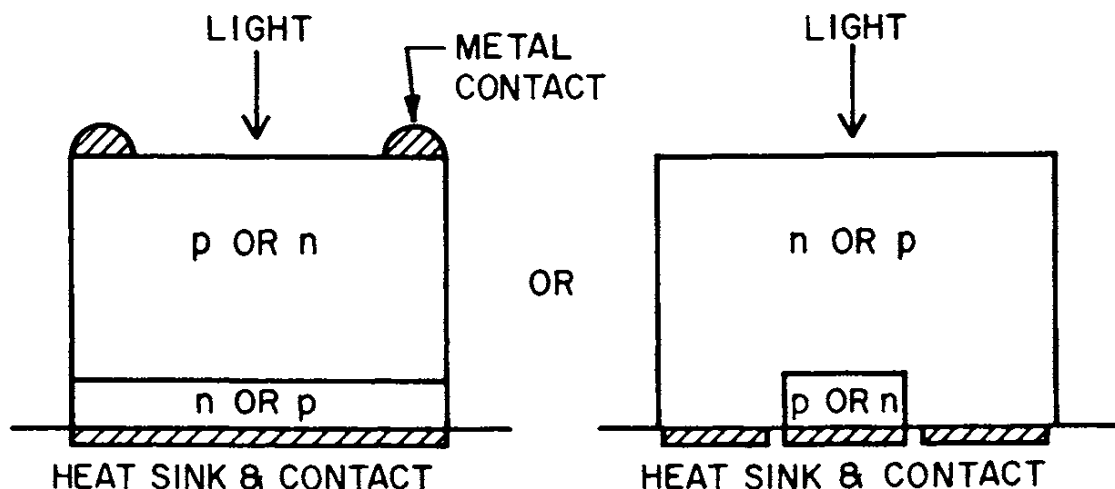
37. In addition to forming the p-n junction, manufacturing a solar cell includes the steps of forming metal electrodes, in order to extract the extra charge that builds as a result of light absorption. The metal electrodes are formed on the front (or top or light entering side) and the back (or rear) of the solar cell. Since metal electrodes reflect light, the metal electrode on the top side has a comb-shape structure consisting

of interconnected metal fingers that cover only a very small portion of the top surface, while the rear metal electrode typically covers the entire back side as shown. It was well known that the doping type of the substrate (n or p) and the placement of the junction (top side or rear side), as well as the placement of the electrode contacts (both sides or a single side) were design choices, as some of the designs shown in the figures below depict.



Green, FIG. 4.3a.





Neville, Figure VI.1 (PN and heterojunction solar cell-light).

38. Another significant aspect of a solar cell design is ensuring that as much of the incident sunlight as possible enters the semiconductor silicon to generate charge carriers. As Figures IV.1 and IV.2 of Neville depict, when “the photons strike the surface of the semiconductor a fraction of the photons is reflected from the surface, and the remaining photons enter the semiconductor. Some of these photons are absorbed within the semiconductor, and some pass entirely through the semiconductor and are lost.” Neville, 119. Thus, “[i]t is common practice to apply antireflection coatings to the optically absorbing surface of solar cells as a means of reducing energy losses due to reflection of photons.” *Id.*, 121. Bare, polished silicon is highly reflective, reflecting over 35% of the incoming light, but drastic reduction of the reflection coefficient occurs when an antireflective layer is used. Markvart, FIG. 8. One of the

materials that was well known to serve as an antireflective layer was silicon nitride.

“PECVD SiN, has two important additional advantages for Si solar cells. First, its refractive index can be strongly varied and adjusted to give excellent performance as a single or double layer antireflection (AR) coating on both encapsulated and non encapsulated Si cells.” Ponce, 295, *see also* e.g., Verlinden, 448. “The front surface of the solar cell should be coated with a thin layer of silicon nitride (as part of the ARC)...”

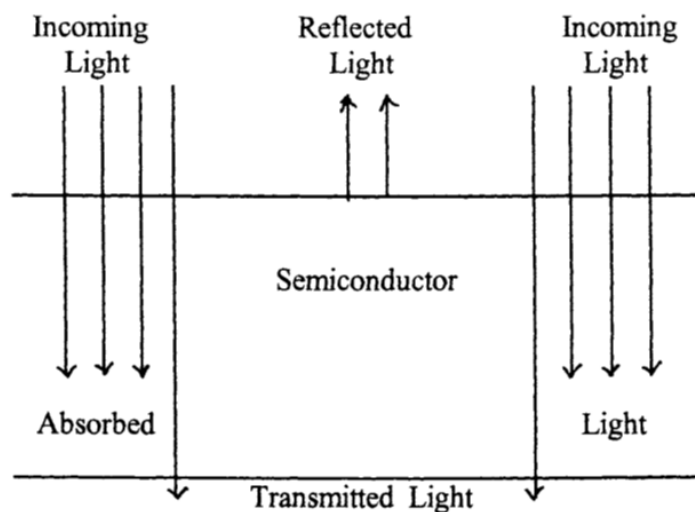


Figure IV.1. A vertically illuminated semiconductor illustrating the incoming light, the reflected light, the light absorbed in the semiconductor and the light passing through the semiconductor.

Neville, FIG. IV.1.

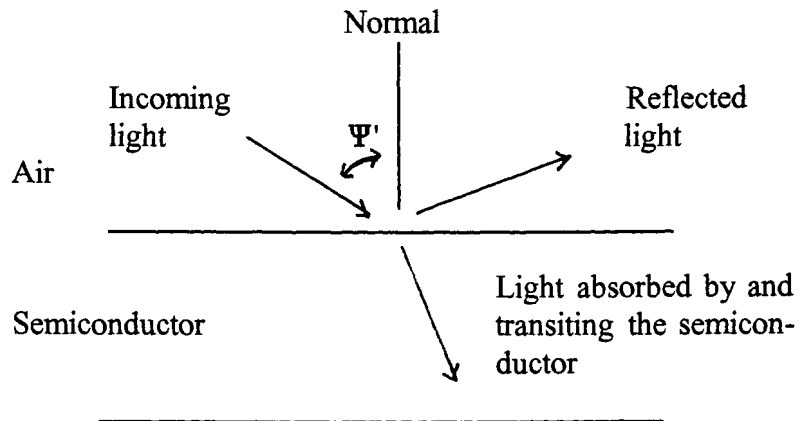


Figure IV.2. Light incident on a semiconductor at other than normal incidence.

Neville, FIG. IV.2.

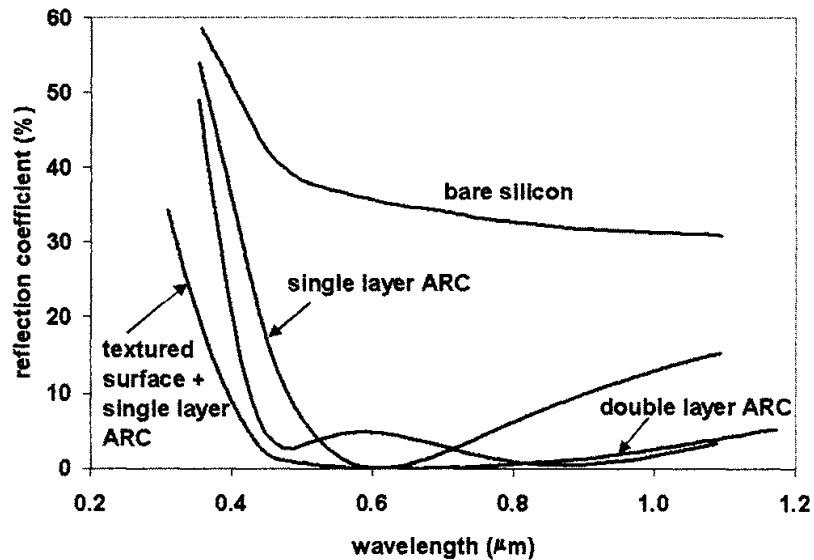
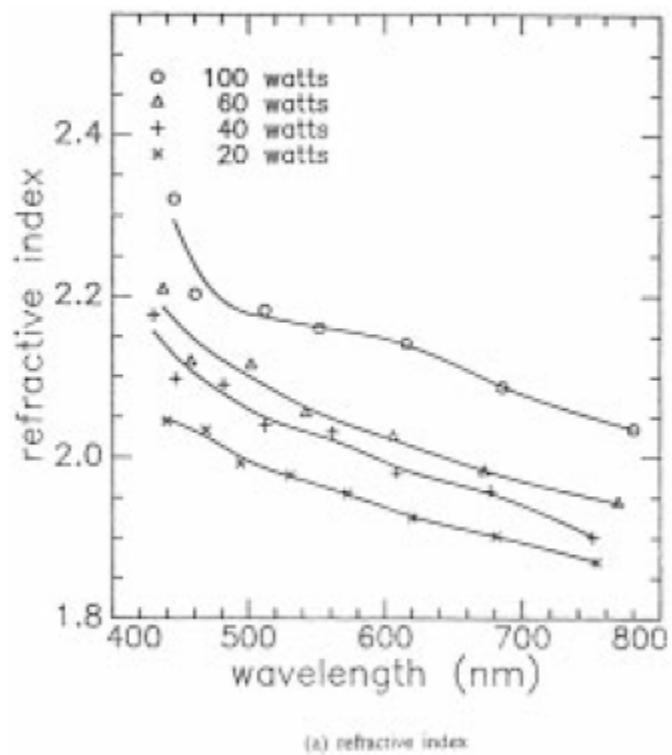


Figure 8 The reflection coefficient from polished bare silicon, and from a polished silicon surface covered with a single and double layer antireflection coating (after [31, 33]). The reflection coefficient for a textured surface is also shown.

Markvart, FIG. 8.

39. It was also well known that a “transparent electrode” 21, e.g., a transparent conductive oxide such as Indium Tin Oxide (ITO) serves as an antireflective layer because a transparent electrode has optical transparency and can be deposited with a low index of refraction ($n < 2$) in order to minimize the difference between its index of refraction and the index of refraction of air ($n = 1$), thus minimizing reflection. For example, Figure 1a of Chiou demonstrates an ITO layer having an index of refraction $n < 2$. It was well known that the reflection of light incident on a material increases as the difference between the index of refraction of the material and that of air increases. Froitzheim, 180 (“The transparent conducting oxide (TCO) is used to enhance the lateral conductivity and **to minimize reflection losses**,” referring to FIG. 1), *see also* Taguchi, 866 (“The TCO layer on the top also works as an anti-reflection (AR) layer,” referring to FIG. 1); Borden, 1149 (“an overlaid ITO as an antireflection (AR) coating and contacting layer,” referring to FIG. 2).



Chiou, FIG. 1(a).

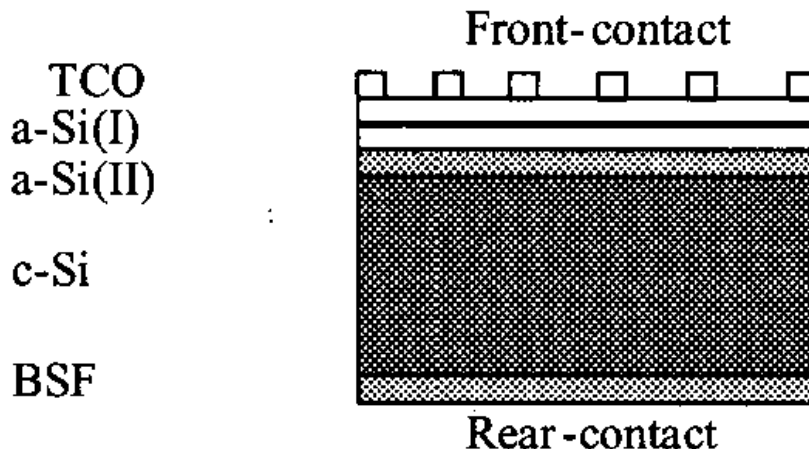


Fig. 1: Schematic structure of the prepared heterojunction solar cell. TCO is an 80 nm thick ITO, a-Si(I) is highly phosphorus doped a-Si:H(n), a-Si(II) is intrinsic a-Si:H(i), BSF is a boron diffused back surface field. The a-Si:H emitters have been prepared with and without the intrinsic buffer layer.

Froitzheim, FIG. 1.

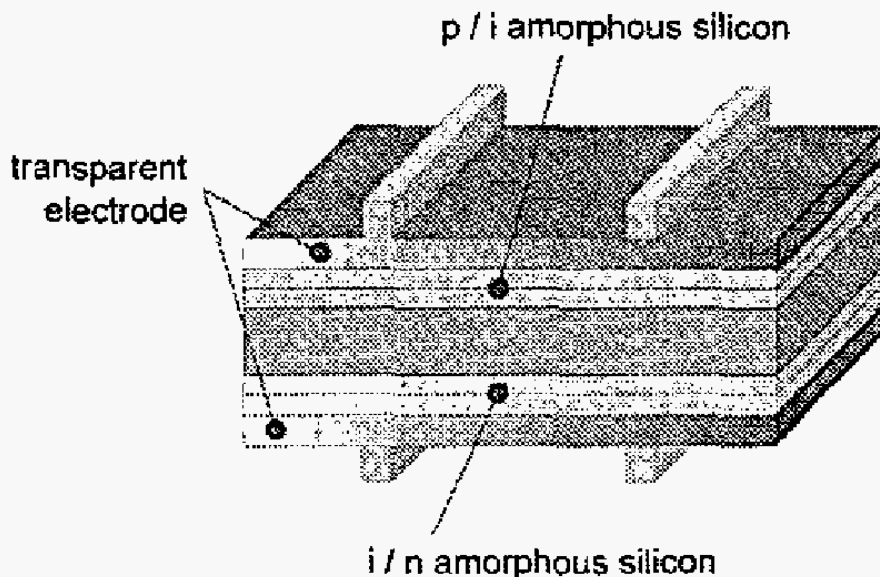


Fig. 1. Schematic diagram of the HIT cell.

Taguchi, FIG. 1.

40. In addition to minimizing the optical losses by applying an antireflective coating on the front or light entering side of a solar cell, applying a metal electrode on the back that can serve as a mirror to reflect photons toward the front side was also a standard practice in fabricating solar cells. For example, Figures 3 and 6 of Yamamoto depict an internal mirror forming a back reflector on the side of the solar cell opposite to the side where light enters the solar cell, in order to increase the optical path of the light. It was known that “[l]ight-trapping technology provides a means of extending the optical path of the incident light inside the solar cell by causing multiple reflections, thereby improving the light absorption in the active layer.” Yamamoto, 941, *see also id.* (“Light trapping can be achieved in two ways: (1) by introducing a highly reflective layer at the back surface to reflect the incident light without absorption loss, and (2) by introducing a textured structure at the back surface of the thin-film Si solar cell...As a[n] effective example of light trapping, Fig. 3(a) shows a cell that uses a flat highly reflective layer at the back surface, and Fig. 3(b) shows a cell that uses a textured type of highly reflective layer. This highly reflective back layer also acts as the solar cell’s back electrode.”)

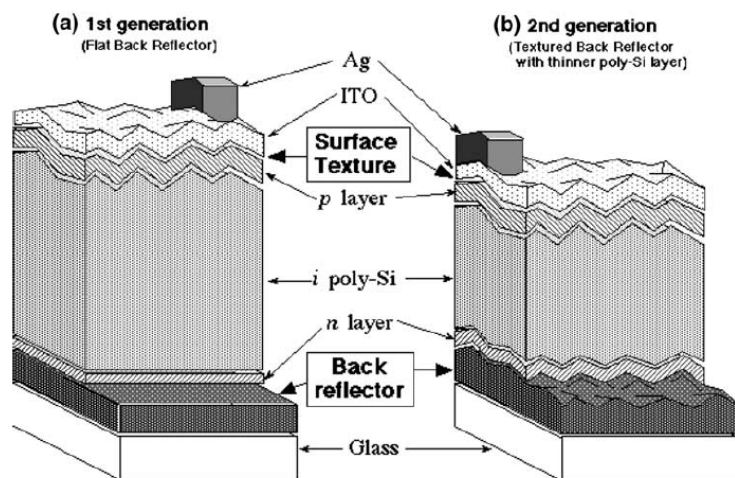


Fig. 3. Cross-sections through light-trapping microcrystalline silicon solar cell devices: (a) first generation (flat back reflector); (b) second generation (textured back reflector, thinner polycrystalline silicon layer).

Yamamoto, FIG. 3.

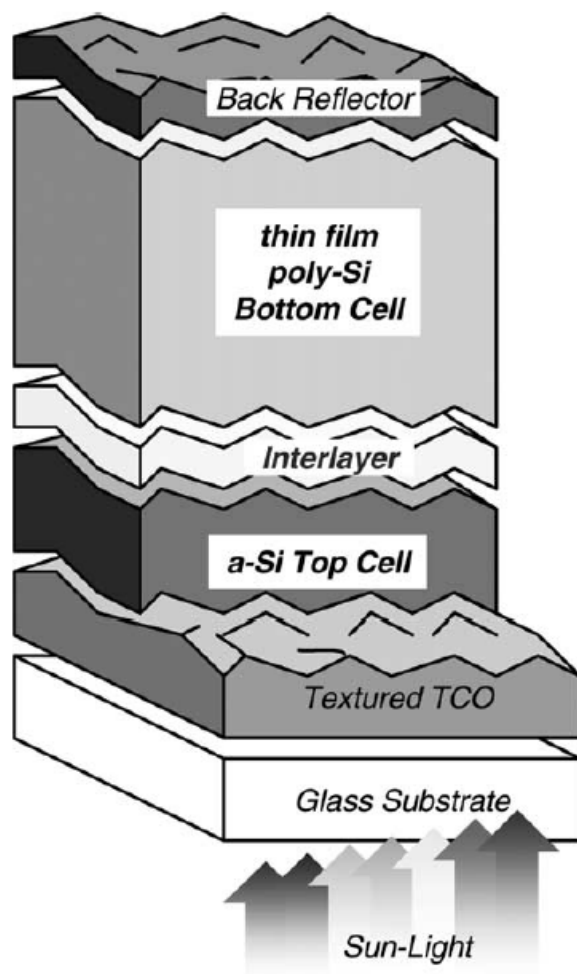


Fig. 6. Schematic view of a-Si/poly-Si (μ c-Si) stacked cells with an interlayer.

Yamamoto, FIG. 6.

41. A common back electrode used in solar cells is aluminum, which has a high reflectance. For example, Figure 12 of Smith depicts that the reflectance of aluminum is greater than 90% for wavelengths greater than 900 nm or 0.9 μ m. The '074 patent defines “a good internal mirror in the back” (18:25-26) as a material that

has a “high reflectivity for photons of more than 900 nm wavelength.” ’074 patent, 7:51-53, 12:8-9.

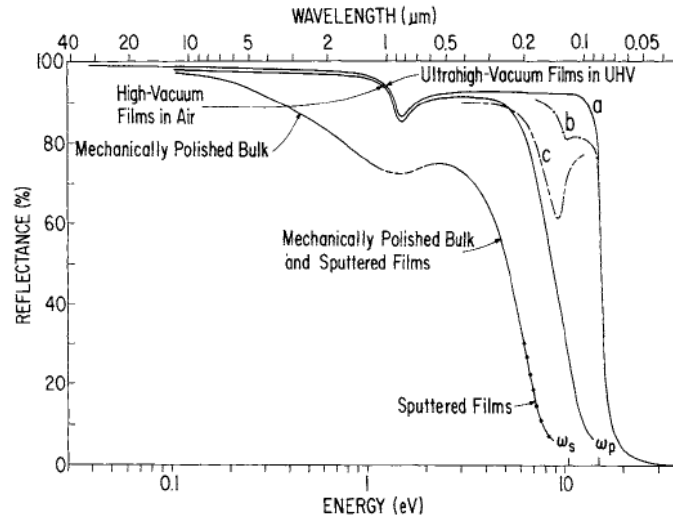


Fig. 12. The reflectance of metallic aluminum at room temperature. The uppermost curve gives the reflectance of opaque evaporated aluminum films prepared in ultrahigh vacuum. These films are presumed to be free of bulk and surface oxide contamination. The effect of light scattering and coupling to surface plasmons (at $\omega_s \approx 10.6$ eV) is illustrated by curves b and c. Curve b was obtained by Vehse *et al.* [90] for a film on a microscope slide cleaned by vapor decreasing and evaporated in a vacuum of $\sim 3 \times 10^{-8}$ torr; the “oxide-free” reflectance was obtained by extrapolation of the reflectance back to the time that the evaporation was completed. Curve c is for a uhv film with rms surface roughness σ of 18 Å, as reported by Endriz and Spicer [53]. The curve labeled high vacuum is an average for films evaporated in vacuum of the order of 10^{-5} torr. At this pressure surface and bulk oxidation occurs. The values reported for such films vary widely, especially in the ultraviolet, presumably because of surface roughness. The third curve is representative of mechanically polished samples, but the reported range of measurements is extremely large. Data for sputtered films are available from 380 nm well into the UV [44, 45]; curiously enough, they track the data for polished samples very closely.

Smith, FIG. 12.

VI. U.S. PATENT NO. 9,130,074

A. Overview

42. The '074 patent is entitled “High-efficiency Solar Cell Structure and Methods of Manufacture” and names Oliver Schultz-Wittmann and Denis DeCeuster as inventors. The '074 patent is generally directed to processes for manufacturing a solar cell composed of a central substrate, conductive layer(s), antireflection layers, passivation layers and/or electrodes. '074 patent, Abstract, 1:20-23.

43. A stated object of the '074 patent is disclosing “improved manufacturing methods including single-side CVD deposition processes and thermal treatment for layer formation and/or conversion.” '074 patent, 1:54-57. A further object of the '074 patent is to disclose “solar cells which attain high operational efficiency, and which can be manufactured in a cost effective manner.” '074 patent, 1:40-42.

44. The '074 patent discloses several examples of solar cells made with the claimed processes. '704 patent, 2:56-57. As shown in Figure 6, a solar cell structure according to the invention contains a “n- or p-type wafer 65”, “Electrically passivating interface layer” 64 and 66, “Electrically passivating and conductive film” layers 63 and 67, “transparent and conductive film” layers 62 and 68, “front metal electrode” 61 and “back metal electrode” 69. '074 patent, 5:14-6:25, FIG. 6.

45. The '074 patent does not explicitly define an “electrically passivating interface layer” but discloses several options for such a layer, including “silicon oxide,

silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, titanium nitride.” ’074 patent, 5:58-61, 6:1-4.

46. Similarly, the ’074 patent does not explicitly define an “electrically passivating and conductive film” but provides a broad range of options, including “n-type amorphous or polycrystalline silicon carbides,” “n-type amorphous or polycrystalline silicon,” and “n-type amorphous or poly-crystalline diamond-like-carbon.” ’074 patent, 5:45-53, 6:8-15.

47. For the “transparent and conductive film 62” (on the front side) and the “transparent and conductive film 68” on the back side, the ’074 patent discloses a variety of options, including different types of “transparent conductive oxides.” ’074 patent, FIG. 6; 5:37-41, 6:2-24.

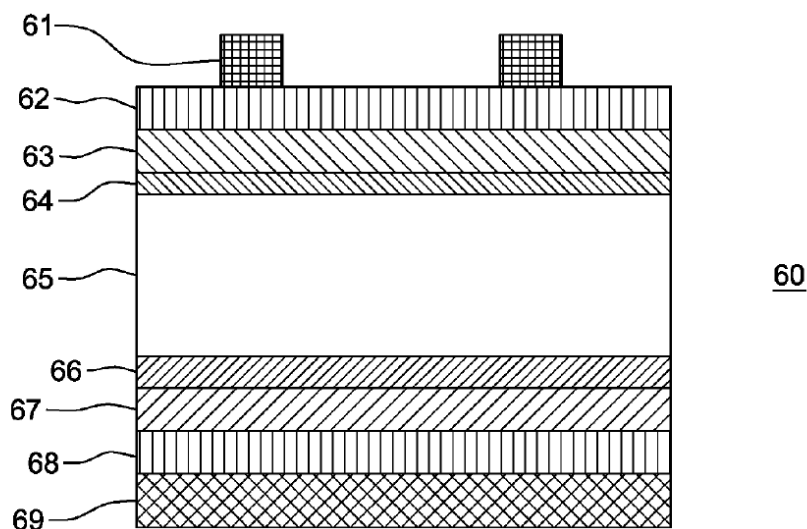


FIG. 6

'074 patent, FIG. 6.

48. The '074 patent includes eight claims: independent claim 1 and seven dependent claims (claims 2–8).

B. Priority Date of the '074 Patent

49. I have been asked to assume that the earliest possible priority date for the '074 patent is April 21, 2009, the filing date of the provisional application No. 61/171,194, as listed on the face of the '074 patent. I have therefore analyzed the prior art as of that date.

C. Level of Ordinary Skill in the Art

50. I have been instructed that factors defining the level of ordinary skill in the art are: (1) the types of problems encountered in the art; (2) the prior art solutions

to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of technology; and (5) the educational level of active workers in the field.

51. After considering the above factors, it is my opinion that a person of ordinary skill in the art (“POSITA”) as of April 2009 would have had a bachelor’s degree in material science, material engineering, physics, electrical engineering, or a related or equivalent field, and two years of experience researching, developing, designing, and/or evaluating solar cells or solar module systems. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard.

52. I met this definition of a POSITA as of April 2009. I applied this definition of a POSITA in forming my opinion in this declaration.

D. Claim Construction

53. I understand that in this proceeding, the claims should be construed in accordance with their ordinary and customary meaning in light of the specification, as understood by one of ordinary skill in the art. After reviewing the specification and the prosecution history, I do not believe that any constructions other than the plain and ordinary meaning of the claim terms of the ’074 patent are necessary for purposes of my analysis. I have therefore applied those plain and ordinary meanings in forming my opinions.

VII. OVERVIEW OF THE PRIOR ART

A. JP1992245683 (“Tamura”)

54. Tamura is prior art to the '074 patent. .

55. Tamura discloses “a method for manufacturing a solar cell, and more particularly to a method for manufacturing a solar cell in which a pn junction of the solar cell is formed by solid phase epitaxy...” Tamura, [0001].

56. One embodiment of Tamura is depicted in Figures 2 and 3 (below).



Tamura, FIGs. 2 and 3.

57. As depicted in Figure 2, Tamura discloses a solar cell structure with a “p-type silicon substrate 11” that was placed in a deposition device, and an “undoped amorphous silicon layer 12” was deposited on top of the substrate 11, and “a high-concentration n+ type amorphous silicon layer 13” was deposited on the layer 12. Tamura, [0015].

58. Tamura discloses that “the substrate 11, on which the amorphous silicon layers 12, 13 were deposited, was heated in an image furnace at a rate of 120°C/min, maintained at 600°C for 5 minutes.” Tamura, [0016].

59. The solar cell structure after the heating process is depicted in Figure. 3. *See* Tamura, [0018]. Tamura discloses that “In FIG. 3, 21 denotes a transparent electrode, 22 denotes a comb-shaped front surface electrode, 23 denotes an n^+ type crystalline silicon layer, 24 denotes an n^- type crystalline silicon layer, 25 denotes a p^- type crystalline silicon layer, and 26 denotes a back surface electrode.” Tamura, [0018]

B. “Polysilicon Tunnel Junctions as Alternates to Diffused Junctions” (“Borden”)

60. Borden is prior art to the '074 patent.

61. Borden discloses the “use of heavily doped polysilicon combined with a tunnel dielectric to provide an alternate to diffused junctions for silicon solar cells.” Borden, Abstract.

62. Borden discloses providing a solar cell structure as shown in Figure 2 and with process flow given in Figure 3. Borden, 1149-50.

63. Borden discloses providing a solar cell structure with an n-type CZ wafer as a central substrate. *See* Borden, 1149 (“Because the IC equipment runs 300 mm wafers, we have been restricted to 780 μm thick CZ substrates without texture, and are constrained to available 300 mm substrates...most processing has been on n-type.”)

64. Borden further discloses that “Amorphous silicon was then deposited and crystallized with a 30-second RTA at 1000°C”. Borden, 1150, FIGs. 3-4.

65. Borden also discloses its solar cell structure “uses a thin p-type poly with an overlaid ITO as an anti-reflection (AR) coating and contacting layer” as well as “a thicker poly with a Si₃N₄ AR coating”. Borden, 1149, FIGs. 2-3.

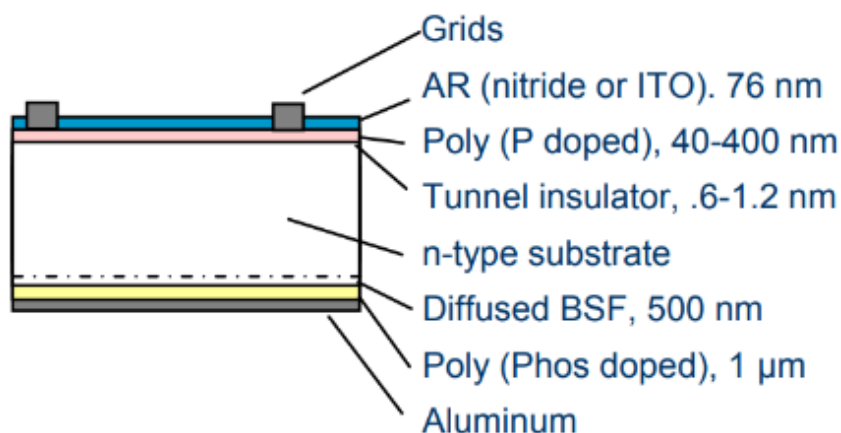
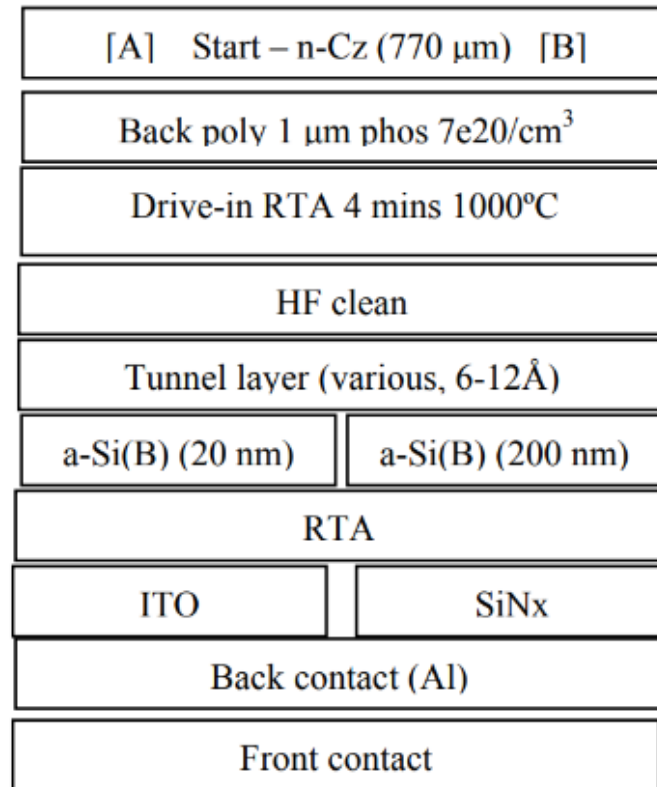


Figure 2: Device structure and process flow. A) with diffused BSF (formed by diffusion during Rapid Thermal Anneal (RTA) of phosphorous doped poly) on n-type Si.

Borden, FIG. 2.

Figure 3: Process flow.



Borden, FIG. 3.

C. U.S. Patent Application US 2010/0240172 (“Rana”)

66. Rana is prior art to the '074 patent.

67. Rana relates to “silicon solar cells and, more particularly, to a method for obtaining a desired dopant profile in the emitter of a solar cell device.” Rana, [0002].

68. Rana discloses a method for forming an emitter in a crystalline silicon substrate by depositing a first lightly doped layer of amorphous silicon on the surface of the substrate. Rana, [0009].

69. Rana further discloses that “subsequent to the deposition of the lightly doped amorphous silicon layer, a heavily doped phosphorous amorphous silicon layer is applied over the lightly doped region, as illustrated at step 14.” Rana, [0027].

70. Rana discloses that the heavily doped amorphous silicon layer undergoes thermal treatment. Rana, [0009] (“Thereafter, a second amorphous silicon layer which is heavily doped is deposited over the full or selected portions of the first deposited amorphous silicon layer. The layer stack is then subjected to a thermal treatment that generates a selectively heavily doped surface region.”)

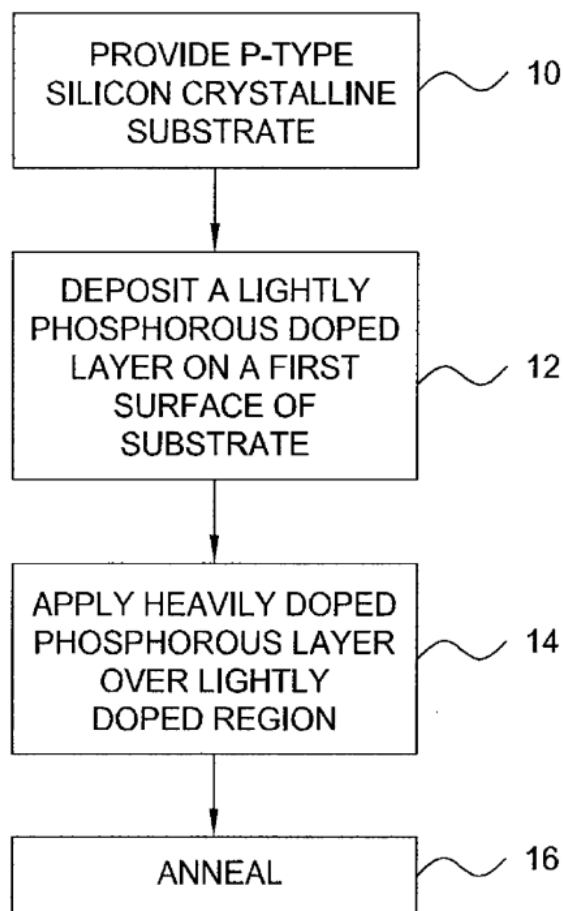


FIG. 1

Rana, FIG. 1.

D. U.S. Patent No. 5,057,439 (“Swanson”)

71. Swanson is prior art to the ’074 patent.

72. Swanson discloses “an improved method of fabricating polysilicon emitters in semiconductor devices such as silicon solar cells.” Swanson, 1:6-9.

73. Swanson Figures 4A-4B disclose a solar cell structure with an “interfacial oxide 16” layer on top of a silicon substrate 10. Swanson, FIGs. 4A-4B; 2:43-60 (“In

FIG. 4A...over the contact areas in contact with the thermally grown oxide 16. FIG. 4B is an enlarged view of the one region of a contact area showing...on the interfacial oxide 16 formed on the surface of silicon substrate 10.”)

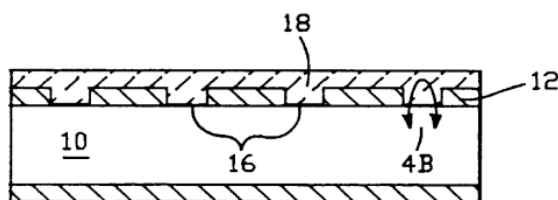


FIG.—4A

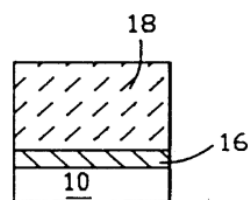


FIG.—4B

Swanson, FIGs. 4A and 4B.

74. Swanson Figures. 5A-5B further disclose that a thermal treatment over 500°C results in perforation of the “interfacial oxide 16” to allow carrier transport therethrough. Swanson, FIGs. 5A-5B; 2:61 3:3 (“Thereafter, as shown in FIGS. 5A and 5B the structure is annealed at a high temperature to break the interfacial oxide and permit electrical contact between the polysilicon emitters and the underlying substrate...For solar cell applications, the typical anneal temperature is 1050°C...As shown in the enlarged view of FIG. 5B, the interfacial oxide is broken partially and polysilicon contacts the substrate intimately in the broken areas.”)

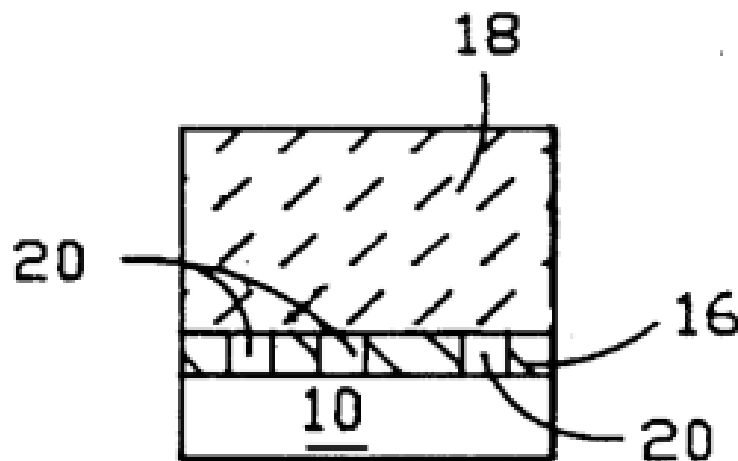


FIG.—5B

Swanson, FIG. 5B.

E. Polysilicon Emitters for Silicon Concentrator Solar Cells (“Gan”)

75. Gan is prior art to the '074 patent.

76. Gan studied “polysilicon emitter with a thermally grown interfacial oxide.” Gan, Abstract.

77. Gan discloses a solar cell structure with an interfacial oxide between the substrate and the polysilicon layer. Gan, 245 (“It was found that, between the polysilicon and the substrate, there always exists a very thin oxide (interfacial oxide).”)

78. Gan also discloses that “the oxide is not thermally stable, i.e., it tends to break up during high temperature anneals.” Gan, 245. Gan further discloses that “As the oxide starts to break up, additional conductive channels are created due to the intimate contacts formed between the polysilicon and the substrate in the broken regions.” Gan, 249.

F. SIPOS Heterojunction Contacts to Silicon (“Kwark”)

79. Kwark is prior art to the '074 patent.

80. Kwark discloses the use of lower oxygen content SIPOS films, whose lower bulk resistivities would allow utilization of these films in structures such as scaled VLSI bipolar devices and high concentration point contact solar cells, where series resistance is detrimental to device performance. Kwark, 742.

81. Kwark discloses “an interfacial layer between the SIPOS and underlying silicon may play an important, if not dominant, role with the implication that the high oxygen concentrations previously used may not be essential for J_{0e} reduction.” Kwark, 742 (“Deliberate introduction of controlled amounts of an oxygen bearing species...into the deposition ambient normally used for chemical vapor deposition of polysilicon produces SIPOS, a class of silicon oxides which exhibits a wide range of physical properties.”)

82. Kwark Figure 3 further discloses the SIPOS crystallizes during subsequent annealing instead of being crystallized. Kwark. FIG. 3.

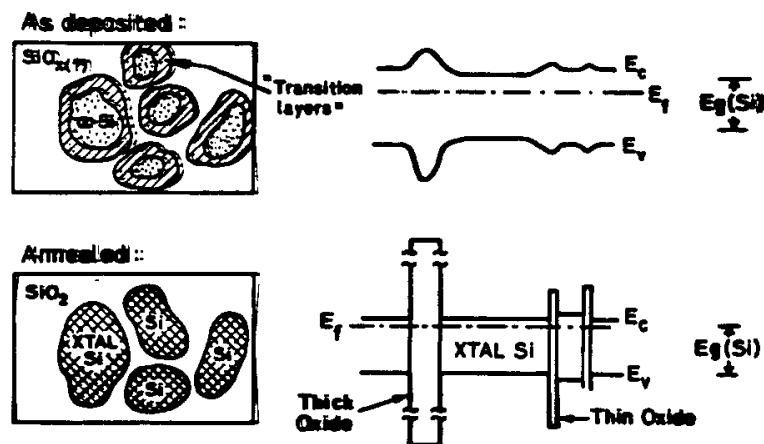


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the "oxide-like" regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Kwark, FIG. 3.

83. Kwark further discloses that the SIPOS would block hole transport. Kwark, 743 ("In N-type SIPOS emitter contacts the lining up of the equilibrium Fermi levels results in a barrier in the valence band which blocks hole transport and accounts for the reduction, in J_{0e} .") Kwark also discloses that the SIPOS is conductive. Kwark, 743 ("The addition of a dopant species converts [the SIPOS] films from semi-insulating to a form that can be made sufficiently conductive after annealing to make them interesting for electronic applications.")

84. Kwark also discloses that “the formation of an interfacial oxide layer as a result of the annealing process (Fig. 3), may be primarily responsible for the reduced hole currents.”.

G. An Investigation of The Thermal Stability of The Interfacial Oxide in Polycrystalline Silicon Emitter Bipolar Transistors by Comparing Device Results with High-Resolution Electron Microscopy Observations (“Wolstenholme”)

85. Wolstenholme is prior art to the '074 patent. Wolstenholme discloses that a chemical oxide (grown by the known RCA chemical clean) becomes discontinuous and holes are formed upon annealing at 950°C. Wolstenholme, Table 1. Wolstenholme also discloses that “[s]mall areas (C) of the polysilicon had been regrown through such holes to become single-crystal material with the same crystallographic orientation as the underlying silicon.” Wolstenholme, 226.

H. Structure and Morphology of Polycrystalline Silicon-Single Crystal Silicon Interfaces (“Bravman”)

86. Bravman is prior art to the '074 patent. Bravman reports that after annealing at 1000°C anneal, the chemical oxide layer itself, which became discontinuous over - 5% of the silicon surface area. Bravman, 2780. (“The second change attending the 1000°C anneal was an alteration of the chemical oxide layer itself, which became discontinuous over - 5% of the silicon surface area. In these regions, the polysilicon made direct contact with, and became epitaxially oriented to, the single crystal substrate. As seen in Fig. 3, however, these regions of epitaxial regrowth were

quite small. Typically, they were 30 to 100 Å in width, and protruded 20 to 30 Å above the interface.”)

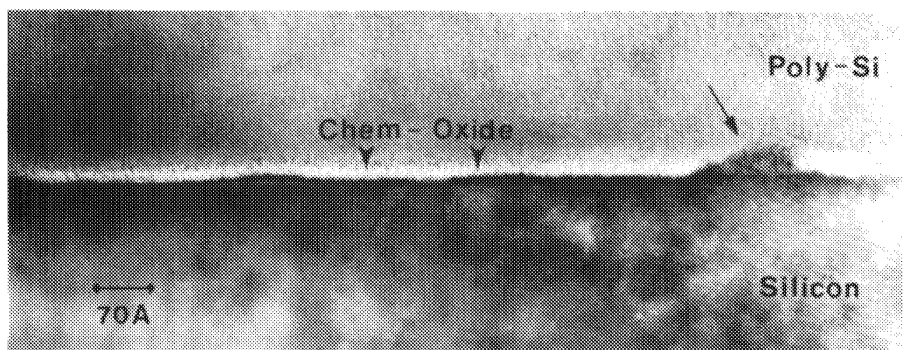


FIG. 3. Chemical-oxide interface following high-temperature annealing, showing a small region of polysilicon epitaxial realignment (arrowed) that formed at an oxide discontinuity.

Bravman, FIG. 3.

I. The Optical Properties of Metallic Aluminum, in *Handbook of Optical Constants of Solids* (Palik, ed., 1985) (“Smith”)

87. Smith is prior art to the '074 patent. Figure 12 of Smith depicts that the reflectance of aluminum is greater than 90% for wavelengths greater than 900 nm or 0.9 μm.

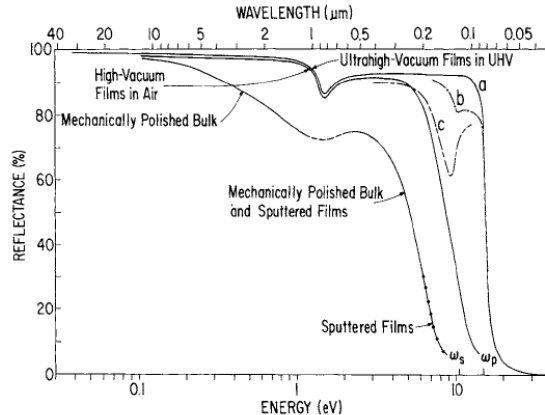


Fig. 12. The reflectance of metallic aluminum at room temperature. The uppermost curve gives the reflectance of opaque evaporated aluminum films prepared in ultrahigh vacuum. These films are presumed to be free of bulk and surface oxide contamination. The effect of light scattering and coupling to surface plasmons (at $\omega_s \approx 10.6$ eV) is illustrated by curves b and c. Curve b was obtained by Vehse *et al.* [90] for a film on a microscope slide cleaned by vapor decreasing and evaporated in a vacuum of $\sim 3 \times 10^{-8}$ torr; the “oxide-free” reflectance was obtained by extrapolation of the reflectance back to the time that the evaporation was completed. Curve c is for a uhv film with rms surface roughness σ of 18 Å, as reported by Endriz and Spicer [53]. The curve labeled high vacuum is an average for films evaporated in vacuum of the order of 10^{-5} torr. At this pressure surface and bulk oxidation occurs. The values reported for such films vary widely, especially in the ultraviolet, presumably because of surface roughness. The third curve is representative of mechanically polished samples, but the reported range of measurements is extremely large. Data for sputtered films are available from 380 nm well into the UV [44, 45]; curiously enough, they track the data for polished samples very closely.

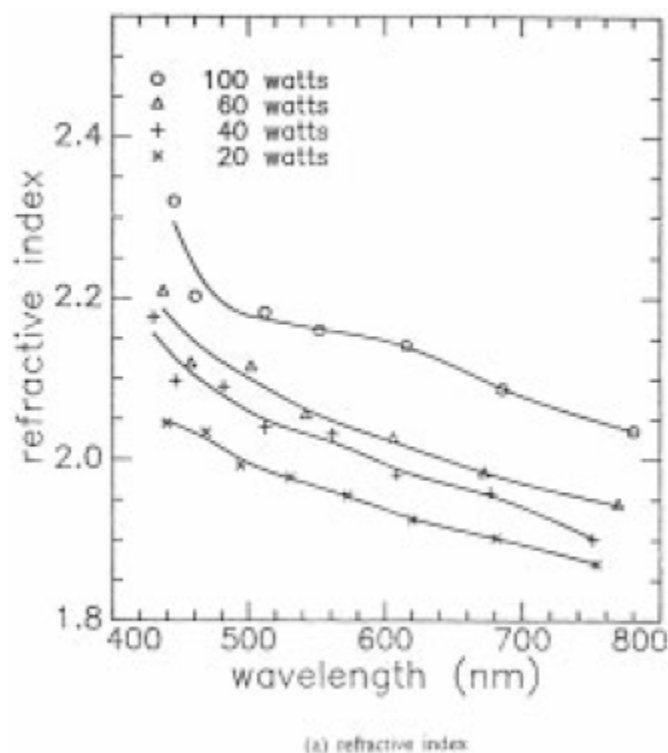
Smith, FIG. 12.

J. Amorphous/Crystalline Silicon Heterojunction Solar Cells with Intrinsic Buffer Layer (“Froitzheim”)

88. Froitzheim is prior art to the '074 patent. Froitzheim discloses that “best results are obtained by combining a-Si:H(n) layers with a-Si:H(i) layers. The a-Si:H(i) layer reduces interface recombination at the interface due to a low defect density in the gap, and the a-Si:H(n) layer further reduces recombination at the interface due to enhanced band bending which leads to an additional field passivation.” Friutzgeunm, 183.

K. Antireflective Coating for ITO Films Deposited on Glass Substrate (“Chiou”)

89. Chiou is prior art to the '074 patent. Figure 1a of Chiou demonstrates an ITO layers having an index of refraction $n < 2$. It was well known that the reflection of light incident on a material increases as the difference between the index of refraction of the material and that of air increases.

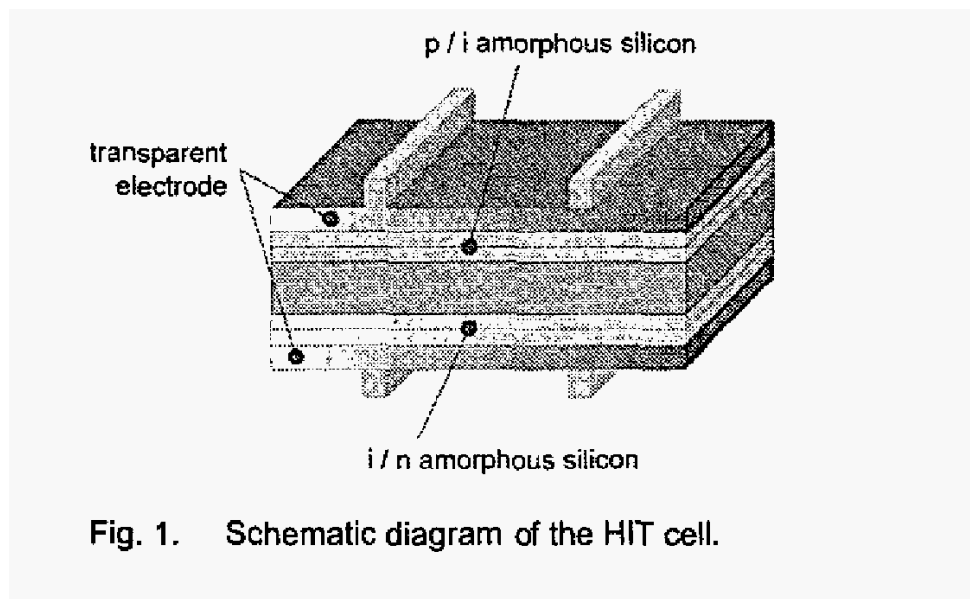


Chiou, FIG. 1(a).

L. An Approach for the Higher Efficiency in the HIT Cells (“Taguchi”)

90. Taguchi is prior art to the '074 patent. Taguchi discloses that “the HIT (Heterojunction with Intrinsic Thin-layer) structure, which features a very thin intrinsic

a-Si layer inserted between p-type a-Si and n-type c-Si...enables an excellent surface passivation and p-n junction, resulting in high efficiency.” Taguchi, 866. Figure 1 of Taguchi depicts that “the TCO layer on the top also works as an anti-reflection (AR) layer.”)



Taguchi, FIG. 1.

M. A High Efficiency Thin Film Silicon Solar Cell and Module (“Yamamoto”)

91. Yamamoto is prior art to the '074 patent. Figure 3 of Yamamoto depicts an internal mirror forming a back reflector on the side of the solar cell opposite to the side that light enters the solar cell, to increase the optical path of the light. As it was discussed in Section V, it was known that “[l]ight-trapping technology provides a means of extending the optical path of the incident light inside the solar cell by causing multiple reflections,” and that one way of achieving light trapping is “by introducing a

highly reflective layer at the back surface to reflect the incident light without absorption loss” and that “[t]his highly reflective back layer also acts as the solar cell’s back electrode.” Yamamoto, 941.

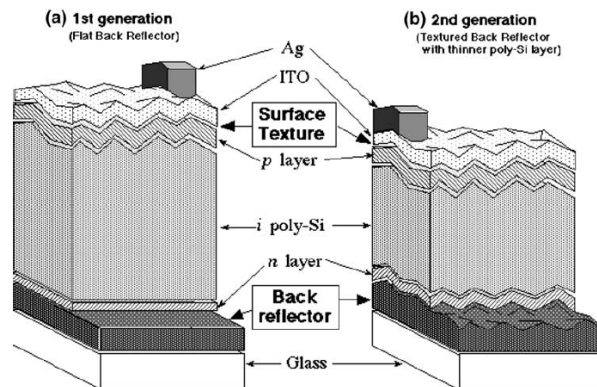


Fig. 3. Cross-sections through light-trapping microcrystalline silicon solar cell devices: (a) first generation (flat back reflector); (b) second generation (textured back reflector, thinner polycrystalline silicon layer).

Yamamoto, FIG. 3.

N. Photovoltaic Technology: The Case for Thin-Film Solar Cells (“Shah”)

92. Shah is prior art to the ’074 patent. Shah discloses that “amorphous silicon has, in the visible range of the spectrum, a higher optical absorption coefficient than crystalline silicon and thus, can have thicknesses much less than 1 μm .” Shah, 696.

O. Semiconductor Material and Device Characterization, Third Edition (“Schroder”)

93. Schroder is prior art to the ’074 patent. Schroder discloses that “the spreading resistance probe technique has been in use since the 1960s...it is mainly used today to generate resistivity and dopant density depth profiles. It has very high

dynamic range (10^{12} - 10^{21} cm⁻³) and is capable of profiling very shallow junctions into the nm regime.” Schroder, 29

P. Amorphous Hydrogenated Silicon, a-Si:H, in *Silicon* (Siffert, ed., 2004) (“Fuhs”)

94. Fuhs is prior art to the '074 patent. Fuhs discloses that “PECVD, silane (SiH₄) or mixtures of silane with rare gases or hydrogen are decomposed in a glow discharge. In most cases, parallel-plate systems in a stainless steel reactor have been used. The most important deposition parameters are substrate temperature, base pressure, flow rate of the process gas, power density and frequency. High-quality a-Si:H films are grown at deposition rates of typically 0.1 nm/s at substrate temperatures in the range 150-250°C.” Fuhs, 125-126. Fuhs further discloses that hydrogenated amorphous silicon, a-Si:H, offers a mature material and device technology, used for solar cells, thin-film transistors, sensors, imaging, radiation detectors and displays.” Fuhs, 124, and that “the hydrogen content can vary widely with the deposition conditions (5-40%)...In optimized films, the hydrogen concentration amounts to 5-15%.”) Fuhs, 126

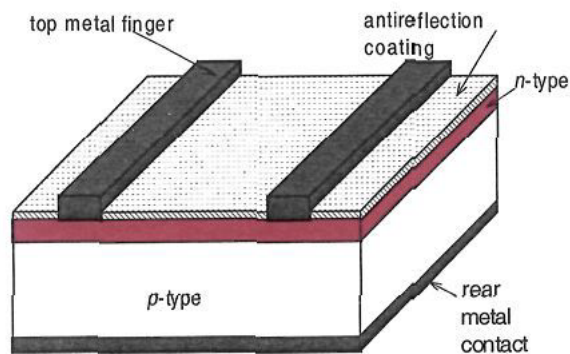
Q. Large Grain Polycrystalline Silicon by Low-Temperature Annealing of Low-Pressure Chemical Vapor Deposited Amorphous Silicon Films (“Hatalis”)

95. Hatalis is prior art to the '074 patent. Hatalis discloses that “the crystallization of amorphous silicon does not result in grains with a columnar structure.

After annealing, amorphous silicon deposited by CVD or by evaporation becomes polycrystalline with a needlelike or dendritic structure”); Hatalis, 2261. Hatalis further discloses that “most of the grains crystallize individually and are surrounded by amorphous silicon. Occasionally, nucleation of new grains occurs at the grain boundaries of existing ones.” Hatalis, 2263

R. Crystalline Silicon Solar Cells, in *Clean Electricity From Photovoltaics* (Archer, ed., 2001) (“Green”)

96. Green is prior art to the '074 patent. Figure 4.3 a of Green discloses a metal electrode on the front or top side has an interconnected finger structure, as shown in below, in order to reduce the light losses caused by reflection from the metal electrodes, while the rear metal electrode typically covers the entire back side as shown.



Green, FIG. 4.3a.

**S. Solar Energy Conversion, Second Edition (Neville, ed., 1995)
("Neville")**

97. Neville is prior art to the '074 patent. Neville discloses that "it is common practice to apply antireflection coatings to the optically absorbing surface of solar cells as a means of reducing energy losses due to reflection of photons." Neville, 121.

T. Silicon for Photovoltaics, in *Silicon* (Siffert, ed., 2003) ("Muller")

98. Muller is prior art to the '074 patent. Muller's FIG. 5.2 depicts a mc-Si comprised over 56% of the material is used in solar cell production worldwide. "Multicrystalline silicon wafers are used exclusively to produce solar cells. Such wafers have the advantage of being cost-effective compared with single crystal wafers." Muller, 84.

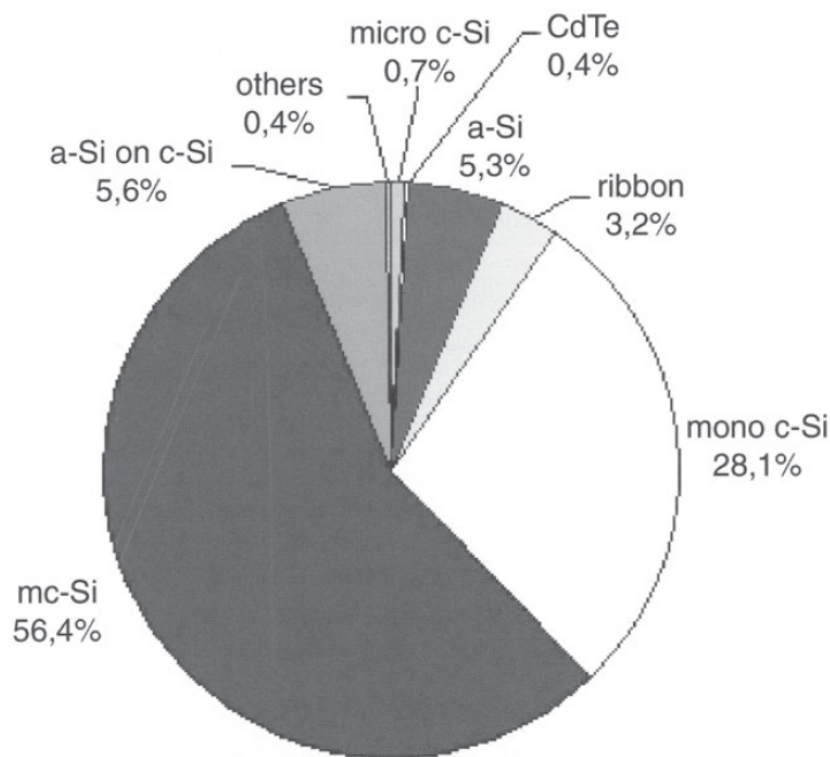


Fig. 5.2. Illustration of the percentage of the different type of materials in the total world production: The share of silicon in the total world product is still 99%, with more than 55% of it being cast mc-Si ingots [2]

Muller, FIG. 5.2.

U. Surface Passivation Layers for Multicrystalline Silicon Solar Cells (“Ponce”)

99. Ponce is prior art to the ’074 patent. Ponce discloses that “PECVD SiN, has two important additional advantages for Si solar cells. First, its refractive index can be strongly varied and adjusted to give excellent performance as a single or double layer antireflection (AR) coating on both encapsulated and non encapsulated Si cells.” Ponce, 295.

VIII. ANALYSIS

A. Ground 1: Claims 1-8 are Anticipated or Rendered Obvious by Tamura

1. Claim 1

a) Limitation 1[pre]: “A method of fabricating a solar cell, comprising;”

100. Tamura discloses that “[t]he present invention relates to **a method for manufacturing a solar cell**, and more particularly to **a method for manufacturing a solar cell** in which a pn junction of the solar cell is formed by solid phase epitaxy”. Tamura, [0001]².

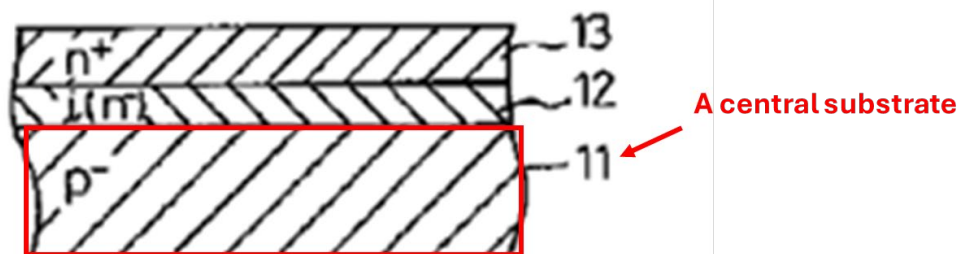
b) Limitation 1[a]: “providing a wafer as a central substrate;”

101. Tamura teaches or suggests this limitation.

102. Tamura discloses a “method comprising steps for depositing an undoped amorphous silicon layer **on a substrate** having at least a surface including a first conductivity-type silicon crystal layer” Tamura, [0005]. Tamura further discloses that the substrate is a “p- type silicon substrate.” Tamura, [0015] (Referring to Figure 2, “This p- type silicon substrate 11 was placed in a deposition device, and an undoped amorphous silicon layer 12 was deposited under the following conditions.”)

² All emphases in quotes have been added, unless otherwise stated.

FIG. 2



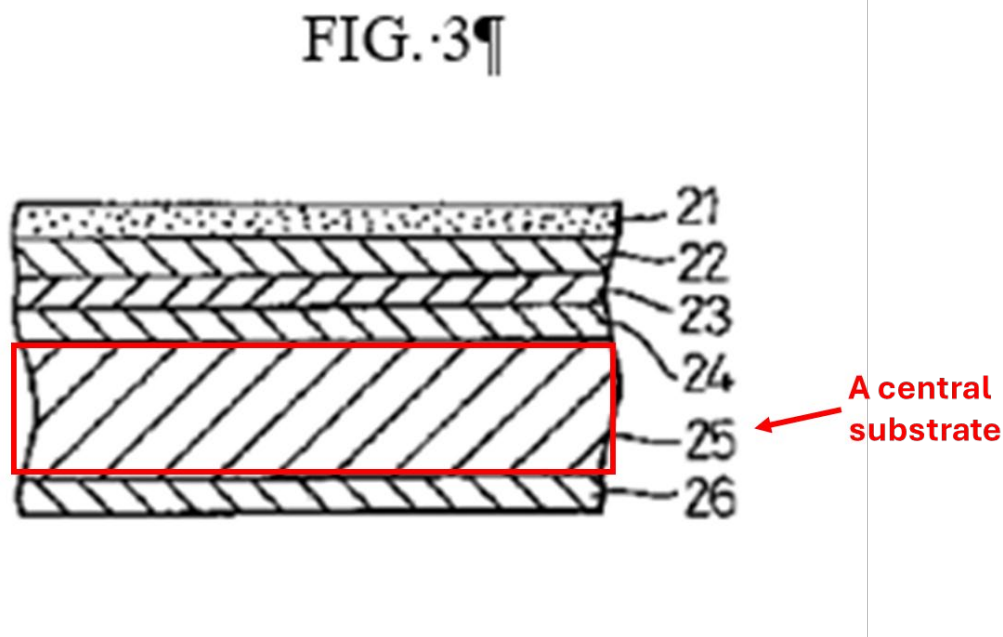
Tamura, FIG. 2 (annotated).

103. A POSITA would understand that substrate 11 in FIG. 2 of Tamura is a silicon wafer. Tamura discloses that the silicon substrate is made through either a single-crystal silicon wafer grown by the “Cz” method, i.e., the Czochralski method, or a polycrystalline silicon wafer grown by the “casting” method. Tamura, [0014] (“Referring to FIG. 2, (100) or (111) Cz monocrystal silicon (resistivity: 2 to 6 Ω cm) or cast polycrystalline silicon was used...”) Both types of silicon wafers were used extensively to manufacture solar cells as discussed in Section V.

104. Tamura further discloses that substrate 11, made of a silicon wafer, becomes a *central substrate* in the finished solar cell structure.

105. Figure 3 depicts the post-thermal treatment solar cell structure corresponding to Figure 2 of Tamura’s embodiment. As shown in Figure 3, the p-type crystalline silicon layer 25, which was the starting p-type silicon substrate 11 before

the deposition of the various layers, is a *central substrate* with layers above and below it after the completion of the manufacturing process. Tamura [0018] (“In FIG. 3, 21 denotes a transparent electrode, 22 denotes a comb-shaped front surface electrode, 23 denotes an n^+ type crystalline silicon layer, 24 denotes an n^- type crystalline silicon layer, **25 denotes a p^- type crystalline silicon layer**, and 26 denotes a back surface electrode.”).



Tamura, FIG. 2 (annotated).

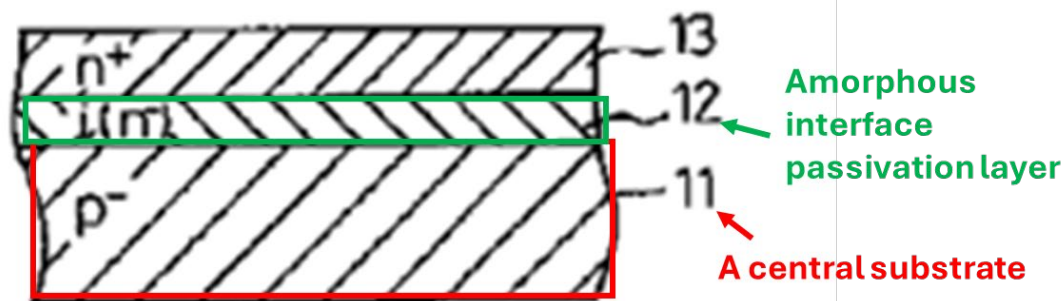
- c) **Limitation 1[b]: “depositing or growing at least one amorphous interface passivation layer over the substrate;”**

106. Tamura teaches or suggests this limitation.

107. The '074 patent does not expressly define “*passivation/passivating*.” However, it discloses that “**Surface passivation** provides suppression of recombination of electrons and **holes at or in the vicinity of certain physical surfaces** within the solar cell.” '074 patent, 3:50-52. The '074 patent also discloses that undoped amorphous silicon is an example of an amorphous interface passivation layer. '074 patent, 3:57-58 (“Another example of a surface passivating layer is intrinsic amorphous silicon.”)

108. Tamura discloses depositing “an undoped amorphous silicon layer 12”, which comprises *an amorphous interface passivation layer*, over “the silicon substrate 11” (*the substrate*). Tamura, [0015] (explaining for Figure 2 that “**p- type silicon substrate 11 was placed in a deposition device, and an undoped amorphous silicon layer 12 was deposited** under the following conditions...”¹). Tamura further discloses that “**heat-treating the undoped and second conductivity-type amorphous layers to convert the layers into crystalline silicon layers...by solid phase epitaxy**.” Tamura, [0005]. Moreover, Tamura discloses that the “crystal structure of the resulting crystallized film was observed by ultraviolet surface reflection and RHEED (reflection high energy electron diffraction) ...” and that “[t]he results confirmed a crystal film was obtained.” Tamura, [0017].

FIG. 2



Tamura, FIG. 2 (annotated).

109. A POSITA would understand that the “undoped amorphous silicon layer 12” is a passivation layer because of its known passivation effect on the surface of substrate 11. *See e.g.*, Froitzheimat, 183 (“ultra thin a-Si:H(i) layers on c-Si(p) reduce interface recombination more effectively than a-Si:H(n).”); *see also* Taguchi, 866 (“The HIT (Heterojunction with Intrinsic Thin-layer) structure, which features a very thin intrinsic a-Si layer inserted between p-type a-Si and n-type c-Si...enables an excellent surface passivation and p-n junction, resulting in high efficiency.”) The solid phase crystallization of the “undoped amorphous silicon layer 12” during the subsequent thermal treatment will also suppress the recombination of electrons and holes at the surface of the central substrate 11 due to the reduction of surface states.

It is well known that at the surface of a crystalline substrate, there are many dangling bonds due to the abrupt termination of the crystal structure, leading to the formation of surface states that increase the recombination of electrons and holes at the surface. After the solid phase crystallization, the “undoped amorphous silicon layer 12” will reduce or eliminate these dangling bonds as the silicon atoms of this layer near the interface with the substrate 11 form bonds with the atoms at the surface of the silicon substrate 11. Tamura discloses explicitly that “[t]he surface of the substrate is highly preferably subject to a cleaning treatment prior to the deposition of an amorphous silicon layer in order to form a pn junction of favorable quality by solid phase epitaxy.” Tamura, [0007]. Tamura also discloses that “[t]he present invention can provide, using a low-temperature process, a solar cell that has excellent film quality.” Tamura, [0019].

110. Tamura also discloses that the resulting solar cells have an increased short-circuit current, as explained in paragraph 34 the short-circuit current (I_{sc}) is one of the key parameters that characterise the performance of a solar cell. Tamura, [0011] (“Moreover, **due to the presence of an undoped layer**, a surface electric field is generated between the outermost surface of the second conductivity-type silicon layer and the pn junction, **resulting in an increase in the short-circuit photoelectric current of the solar cell.**”) It is commonly known in the art that the passivation effect can lead to a higher I_{sc} in devices like solar cells. This passivation effect results in

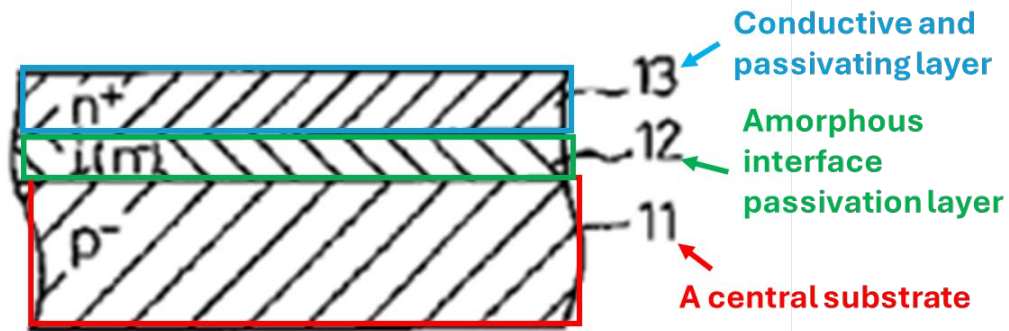
an increase in the number of photogenerated carriers, specifically through increasing the lifetime of minority carriers (electrons in p-type or holes in n-type material), giving them more time to reach the junction and contribute to the current. Here, under Tamura's disclosure, a POSITA would understand that the passivation resulting from the "undoped amorphous silicon layer 12" would increase the number of electrons photogenerated at the p-type substrate and collected by the top n-type region, as the recombination at the original substrate surface would be suppressed as explained above.

d) Limitation 1[c]: "depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant,"

111. Tamura teaches or suggests this limitation.

112. Tamura discloses depositing "a high-concentration n^+ type amorphous silicon layer 13," which comprises *a conductive and passivating layer* on the undoped amorphous silicon layer 12 (*interface passivation layer*) as shown below in Figure 2. *See also* Tamura, [0015] (explaining for Figure 2 that "a high-concentration n^+ type amorphous silicon layer 13 was deposited on the undoped amorphous silicon layer 12 ...") and Tamura, [0009] ("[o]n the undoped amorphous silicon layer obtained thereby, a second conductivity-type amorphous silicon layer, the conductivity type being opposite to the first conductivity type, is then deposited.")

FIG. 2



Tamura, FIG. 2 (annotated).

113. A POSITA would understand that the “high-concentration n^+ type amorphous silicon layer 13” is *conductive*. Tamura discloses that the deposition conditions of “the high-concentration n^+ type amorphous silicon layer 13” comprises a “[d]opant (n-type) PH_3 .” Tamura, [0009], *see also* Tamura, [0016] (“a high-concentration n^+ type amorphous silicon layer 13 was deposited ... under the following conditions Source gas: SiH_4 gas containing **1% PH_3** ”). A POSITA would understand that when the “source gas” is “ SiH_4 gas containing **1% PH_3** ” during the deposition process the two gases will decompose with the silane gas (SiH_4) providing the silicon and the phosphine gas (PH_3), providing the phosphorus so the resulting amorphous silicon film will be doped with phosphorus atoms which act as n-type dopant. It was

well known that phosphorus, which belongs in column V of the periodic table acts as a donor (i.e., n- type) dopant and thus increases the concentration of free electrons.

114. Tamura further discloses “the high-concentration n^+ type amorphous silicon layer 13” as “the second **conductivity-type** silicon layer”, indicating it is *conductive*. Tamura, [0009], [0011]. A POSITA would understand that silicon layer 13 is conductive since it is doped with phosphorus (introduced by the decomposition of the PH_3 , as discussed in the preceding paragraph. Tamura also discloses that “[w]ith this deposition method, an amorphous silicon layer doped at a high concentration can be formed to a desired thickness at a low temperature.” Tamura, [0009]. A POSITA would understand that “an amorphous silicon layer doped at a high concentration” is conductive. Moreover, Tamura teaches that “[t]he dopant concentration of the crystallized second conductivity-type silicon layer can easily be increased to approximately 10^{21} cm^{-3} .” Tamura, [0011]. A POSITA would understand that a dopant concentration of 10^{21} cm^{-3} is considered high and thus the “crystallized silicon layer” is conductive.

115. A POSITA would understand that the “high-concentration n^+ type amorphous silicon layer 13” is *passivating*. See Froitzheim, 183 (“Best results are obtained by combining a-Si:H(n) layers with a-Si:H(i) layers. The a-Si:H(i) layer reduces interface recombination at the interface due to a low defect density in the gap, and the a-Si:H(n) layer further reduces recombination at the interface due to enhanced

band bending which leads to an additional field passivation.”) Tamura discloses that both “the deposited undoped and second conductivity-type amorphous silicon layers are crystallized by heat treatment” resulting in “epitaxial growth” by “solid phase epitaxy.” Tamura, [0005], [0010]. As I explained above, the epitaxial crystallization of the amorphous silicon layers suppresses the recombination of electrons and holes at the original substrate surface. As I also explained above, this passivation effect can lead to a higher short circuit current I_{sc} in devices like solar cells by increasing the number of photogenerated carriers collected. Passivation increases the lifetime of minority carriers (electrons in p-type or holes in n-type material), giving them more time to reach the junction and contribute to the current.

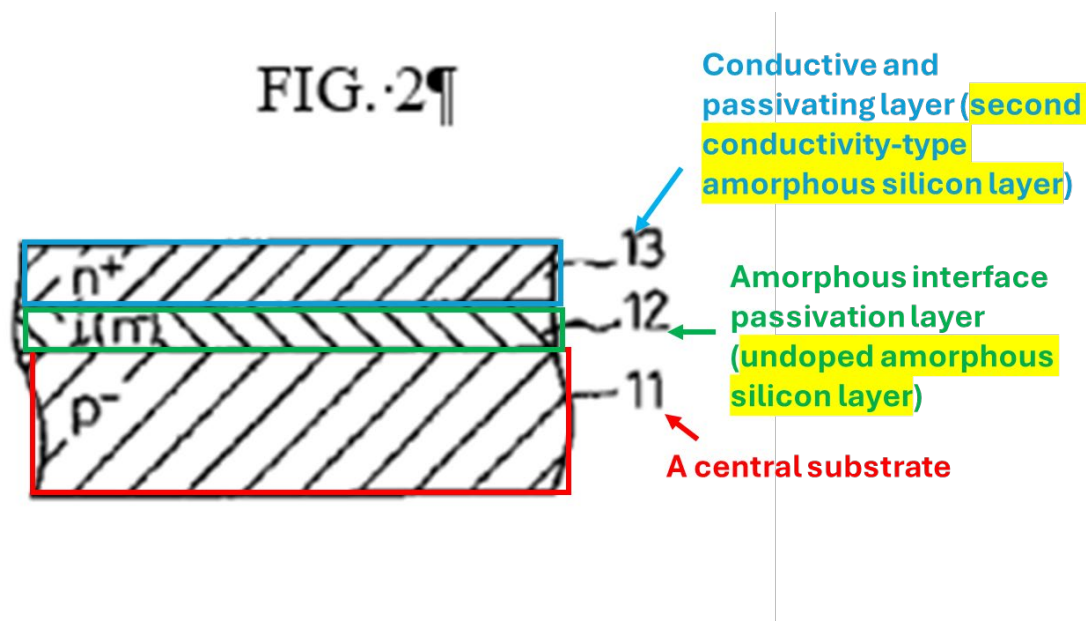
- e) **Limitation 1[d]: “providing thermal treatment at a temperature of above 500°C. or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer; and,”**

116. Tamura teaches or suggests this limitation.

117. Tamura discloses that “the deposited undoped [the *interface passivation layer*] and second conductivity-type amorphous silicon [the *conductive and passivating layer*] are crystallized by heat treatment... typically, 600°C to 700°C.” Tamura, [0010]. Tamura also discloses providing a thermal treatment by heating the substrate 11, and silicon layers 12 and 13 at **600°C** for 5 minutes. Tamura, [0016]

(“Next, the substrate 11, on which the amorphous silicon layers 12, 13 were deposited, was **heated** in an image furnace at a rate of 120°C/min, **maintained at 600°C for 5 minutes...**”). Thus, Tamura discloses *providing thermal treatment at a temperature of about 500°C or higher*.

118. Tamura further discloses that *the thermal treatment crystallizes* “high-concentration n⁺ type amorphous silicon layer 13” (also referred to as “the second conductivity-type amorphous silicon layer(s)”), which is *the conductive and passivating layer*. Tamura, [0011] (“This heat treatment **crystallizes** the undoped and **second conductivity-type amorphous silicon layers**, forming a pn junction having a graded structure”), Tamura also discloses that the “crystal structure of the resulting crystallized film was observed by ultraviolet surface reflection and RHEED (reflection high energy electron diffraction)” and that the “results confirmed that a **crystal film** was obtained.” Tamura, [0017]. According to Tamura’s explicit disclosures a POSITA would understand that the Tamura’s thermal treatment is *crystallizing, at least in part, the at least one conductive and passivating layer* as the deposited amorphous silicon layer 13 (the top layer in Fig. 2) is confirmed by Tamura’s ultraviolet surface reflection and RHEED observations to have become “a crystal film.”



Tamura, FIG. 2 (annotated).

119. Tamura also discloses that “[a]fter the heat treatment for solid phase growth, the temperature can be increased to a temperature equal to or higher than the solid phase growth temperature to diffuse a doped impurity and improve a junction interface.” Tamura, [0012]. A POSITA would understand from this that the thermal treatment *facilitat[es] diffusion of the phosphorus dopant*, introduced by the PH_3 gas during the deposition process, *from the “amorphous silicon layer 13” (at least one conductive and passivating layer) through the “amorphous silicon layer 12” (at least one interface passivation layer)*. Specifically, a POSITA would understand that heating silicon layers 12 and 13 at **600°C** for 5 minutes causes the phosphorus dopant atoms to diffuse from the silicon layer 13 into the silicon layer 12. Tamura discloses that “the electrical properties (of the resulting crystallized film) were observed by Hall

effect measurement and spreading resistance measurement” and that “[t]he results confirmed that a crystal film was obtained having a graded structure with a carrier concentration of 10^{20} cm^{-3} near the surface” and that “a pn junction having a graded structure” is formed. Tamura, [0011], [0017]. A POSITA would understand that the layered structure formed after the heat treatment and depicted in FIG. 3 of Tamura will be a graded pn junction in which the doping concentration changes gradually from the p- region (i.e., the “p⁻ type substrate 25”) to the n- region (i.e., the “n⁻ type crystalline silicon layer 24” and “n⁺ type crystalline silicon layer 23”). Tamura, [0018], FIG. 3.

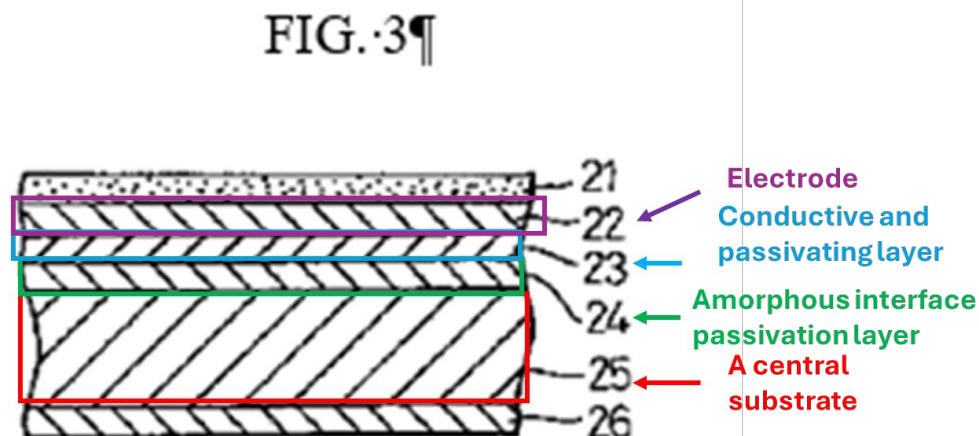
120. Since the substrate in Tamura is uniformly doped “having a dopant concentration of approximately 10^{17} to $10^{15}/\text{cm}^3$ ”, *see* Tamura, [0006], a POSITA would understand that phosphorus diffuses from the “amorphous silicon layer 13” through the “amorphous silicon layer 12” and the resulting phosphorus concentration gradually changes from 10^{20} cm^{-3} at the surface of the “n⁺ type crystalline silicon layer 23” across the “n⁻ type crystalline silicon layer 24” to 10^{17} to $10^{15} / \text{cm}^3$ of the “p⁻ type substrate 25”. Tamura explains that the low temperature used during the thermal treatment prevents the diffusion of the dopant “deeply” into the substrate 11, which indicates that the thermal treatment facilitates the diffusion of the dopant from silicon layer 13 to layer 12 sitting right above the substrate 11. Tamura, [0011] (“the low temperature prevents a dopant from diffusing deeply into the substrate.”)

f) Limitation 1[e]: “providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof”

121. Tamura teaches or suggests this limitation.

122. Tamura discloses *providing metallization as electrodes* in the solar cell *following the thermal treatment*. Tamura, [0012] (“After the heat treatment for solid phase growth...The formation of electrodes and the like other than the formation of the pn junction can be performed in the same manner as in a typical solar cell.”)

123. Tamura also discloses a “comb-shaped front surface electrode 22”, which comprises an *electrode in direct contact with* “the n⁺ type crystalline silicon layer 23” *at least one conductive and passivating layer*. As shown in Figure 3 below, a comb-shaped front surface electrode 22 is directly in contact with the n⁺ type crystalline silicon layer 23 (*at least one conductive and passivating layer*). Tamura, [0018], (explaining for Figure 3 that “22 denotes a comb-shaped front surface electrode, 23 denotes an n⁺ type crystalline silicon layer”).



Tamura, FIG. 3 (annotated).

- g) **Limitation 1[f]: “wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.”**

124. Tamura teaches or suggests this limitation.

125. The '074 patent fails to define or disclose “shortened charge carrier flow paths” as required in this claim element.

126. The '074 patent describes the “shortest geometrical” charge carrier flow path as the one that occurs when the “[charge carriers’] transport within the emitter is **vertical instead of mainly lateral.**” '074 patent, 4:47-50. According to the '074 patent, such a vertical transport path is formed when using an electrode that has a “full area contact coverage” with the emitter, and the emitter is on the back side of the substrate,

as shown in Figure 3. '074 patent, 4: 47-51 (explaining Figure 3 “The minority carriers (solid lines) can use the **shortest geometrical path** to reach the rear n-type emitter 38, and their transport within the emitter **is vertical instead of mainly lateral**”).

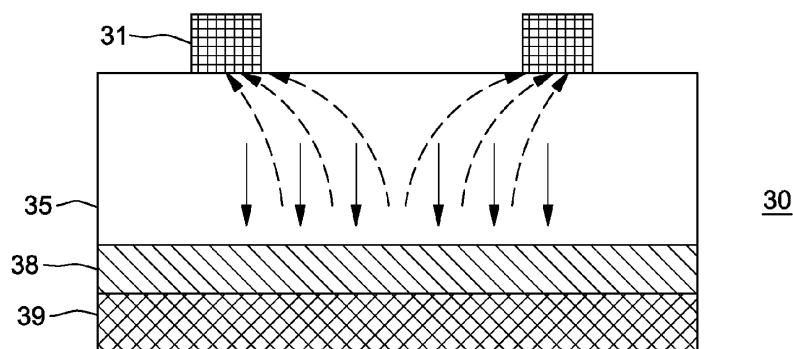


FIG. 3

'074 patent, FIG. 3.

127. A POSITA would understand that when the carrier flow is vertical, for example, in layer 38 in Figure 3 of the '074 patent, or in general, through the “conductive and passivating layer” of the '074 patent, the resistance of this layer to the current flow will have the lowest value, since in general the resistance (R) of a material is proportional to the length (L) of the material along which the current flows. It was well known that the resistance of a material is given by: $R = \rho L / (W t)$, where ρ is the resistivity of the material typically in units of ($\Omega \text{ cm}$), L is the length, W is the width and t is the thickness of the material. *see e.g.*, Schroder, 11. The resistance of a material can also be written as: $R = R_{sh} L / W$, where R_{sh} is the sheet resistance of the material

defined as: $R_{sh} = \rho / t$, and having units of (Ohm/square) where the number of squares is determined by the ratio (L / W). Therefore, a POSITA would understand that the “shortened charge carrier flow paths” can be achieved by reducing the resistance of the layer through which the carriers flow, i.e., the resistance of *the conductive and passivating layer*. Indeed, the '074 patent discloses that in the case of a front junction (formed as depicted in FIG. 2 between a p-type wafer 25 and a thin n-type emitter 22) “the minority carriers (solid lines) flow to front electrodes 21 from a p-type wafer 25” and in this case “[t]he electrons need to use lateral flow within the thin n-type emitter 22 to reach the electrodes 21, and the lateral sheet resistance of the emitter 22 increases **resistive losses**. The majority carriers (dashed lines) can use the shortest geometrical path to the full area back electrode 29.” '074 patent, 4:36-44.

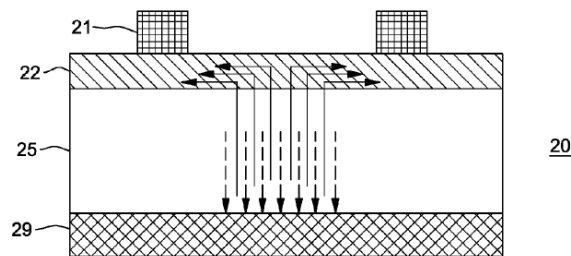


FIG. 2

'074 patent, FIG. 2.

128. In sum, the '074 patent states that in the case of a “back junction structure,” such as the one shown in Figure 3, “[t]his back junction structure reduces the requirements for lateral conductivity of the emitter layer.” '074 patent, 4:50-51.

However, in the case of a “front junction,” such as the one depicted in Figure 2, “the lateral sheet resistance of the emitter 22 increases resistive losses” and to reduce these resistive losses the '074 places an upper limit on the maximum lateral sheet resistance of the “thin n-type emitter region” of 500 Ohm/sq. '074 patent, 5:14-25 (explaining Figure 6 “This structure has an n-type front surface, which for a p-type wafer 65 collects the minority carriers (electrons) on the front. Therefore **a maximum lateral sheet resistance** of, for example **500 Ohm/sq** of the combined layers 62, 63 and 64 is required.”)

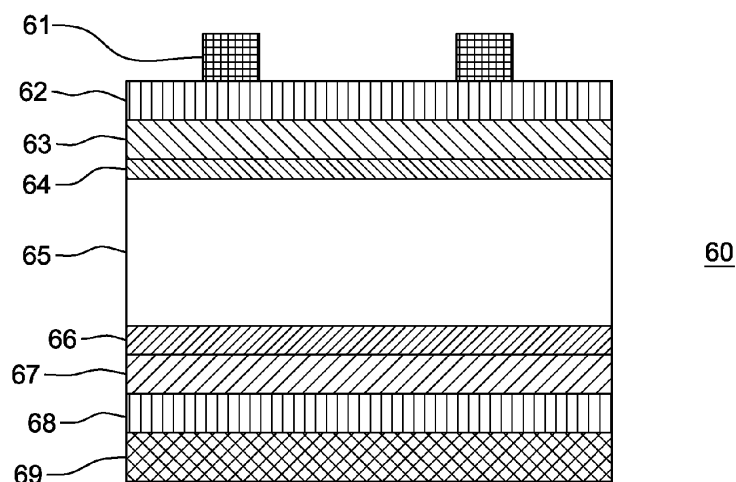


FIG. 6

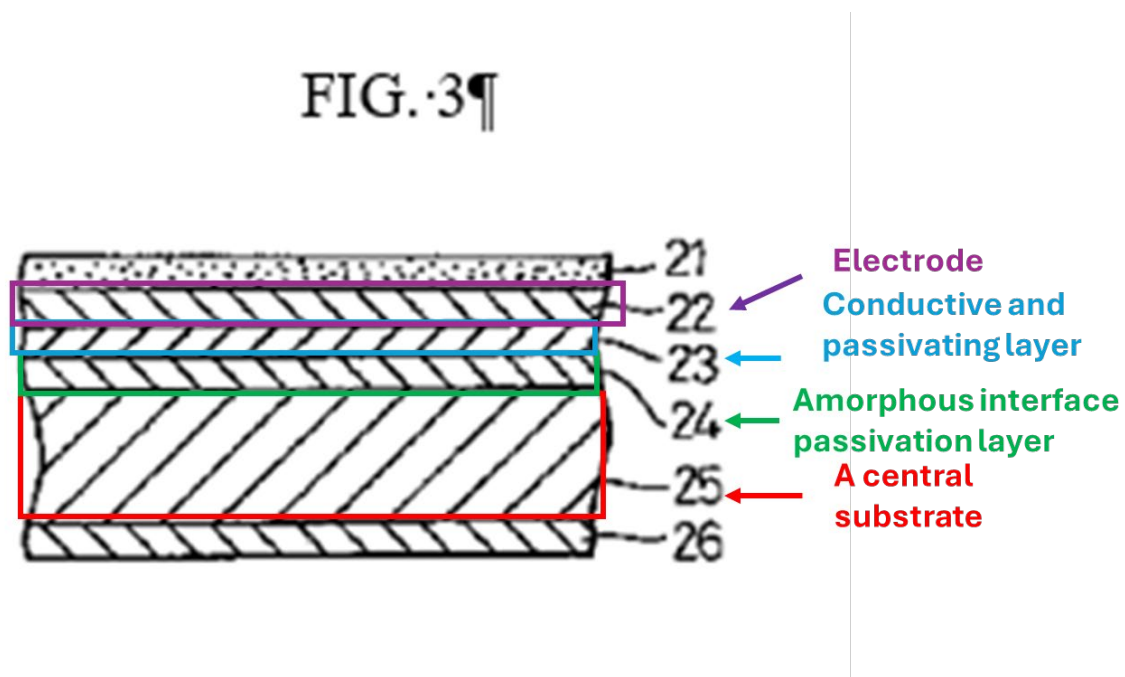
'074 patent, FIG. 6.

129. Therefore, according to the specifications of the '074 patent, a POSITA would understand that the “shortened charge carrier flow paths” are provided by layers that offer low electrical resistance, and according to the '074 patent, these layers are required to have a “maximum lateral sheet resistance” of 500 Ohm/sq.

130. Tamura discloses that a heat treatment forms a pn junction between the p-type crystalline silicon substrate, which is uniformly doped and an n-region that has a graded doping structure and consisting of the crystallized “undoped amorphous silicon layer 12” (*the at least one interface passivation layer*) and “the second conductivity-type amorphous silicon layer 13” (*the at least one conductive and passivating layer*). Tamura, [0011] (“This heat treatment crystallizes the undoped and second conductivity-type amorphous silicon layers, forming a pn junction having a graded structure.”)

131. Tamura further discloses that, after the thermal treatment, *the dopant diffused through interface passivation layer* (“an n⁻ type crystalline silicon layer 24”) in the pn junction *provides shortened charge carrier flow path between the substrate* (“a p⁻ type crystalline silicon layer 25”) *and the electrodes* (“a comb-shaped front surface electrode 22”). As explained below, a POSITA would understand that the carriers in Tamura that flow between the silicon substrate and the electrodes are the minority carriers, i.e., electrons, which are generated when photons are absorbed by the crystalline silicon substrate 25. A POSITA would further understand that for these minority carriers to contribute to the current flow, they must reach the metal

electrode, layer 22.

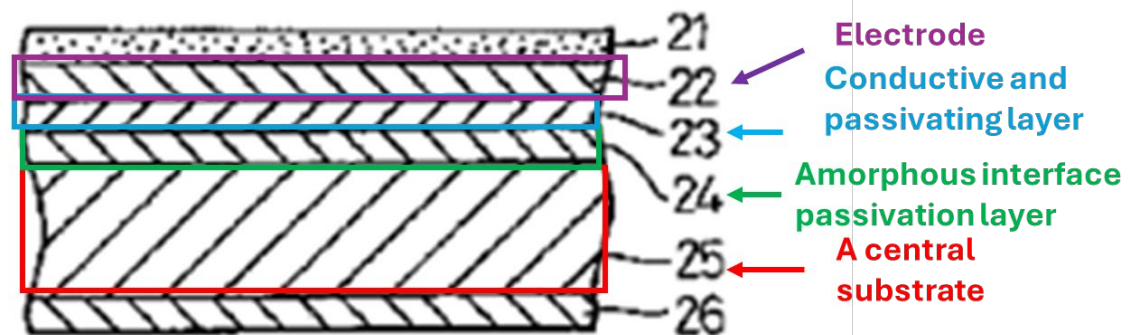


Tamura, FIG. 3 (annotated).

132. Tamura discloses that the “front surface electrode 22” is “comb-shaped.” Tamura, [0018]. A POSITA would understand that Figure. 3 of Tamura depicts the cross-section of “a comb-shaped front surface electrode 22” (the electrode) when the cross-section is taken in parallel with one of the fingers of the comb. *See* Tamura, FIG.3, [0018]. Thus, a POSITA would understand that in a portion of the front or top surface, electrode 22 has a full area contact coverage with the “the n+ type crystalline silicon layer 23” (*the conductive and passivating layer*), layer 23 provides a *shortened charge carrier flow path* (a vertical path) for carriers to pass through it. A POSITA would further understand that the dopant diffusion from *the conductive and passivating layer*

(silicon layer 23) to the *interface passivator layer* (n^- type crystalline silicon 24) and finally into the *substrate* (silicon layer 25) establishes continuous shortened vertical current pathways extending from the *electrodes* to the *substrate*. In other words, in the portion of the surface covered with metal, the carrier flow path is geometrically the shortest as the carrier travels vertically, thereby effectively shortening the charge carrier flow paths between the *substrate* (silicon layer 25) and the *electrode* (front surface electrode 22).

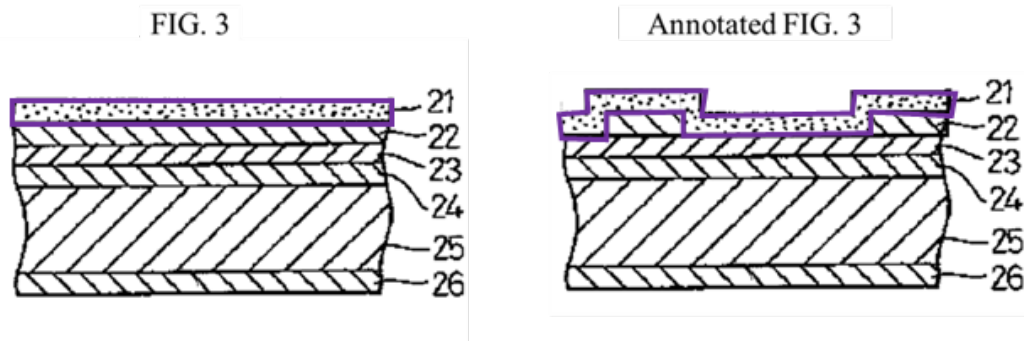
FIG. 3



Tamura, FIG. 3 (annotated).

133. As stated above, a POSITA would understand that in Tamura, the cross-section as depicted in FIG. 3 is drawn along a direction that is parallel to one of the fingers of the comb. A POSITA would also understand that if the cross-section is

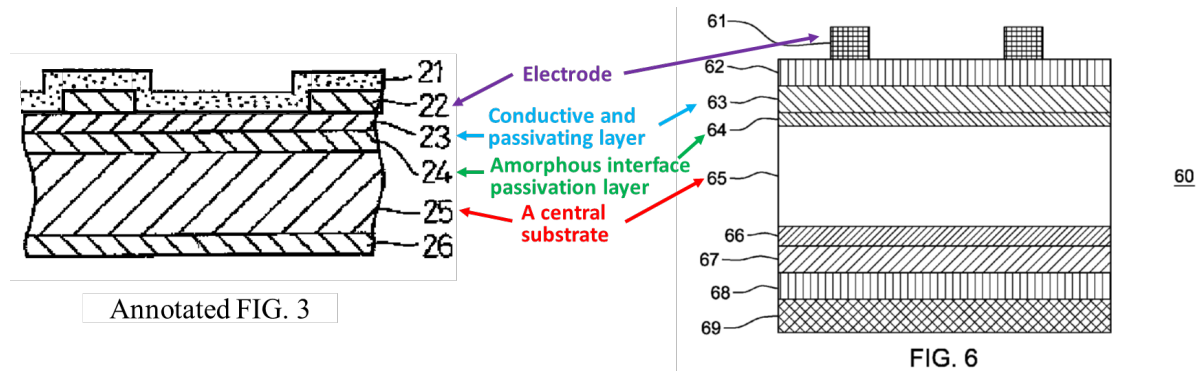
drawn along a direction perpendicular to the fingers of the comb, it will appear as shown in the annotated Figure 3, as shown below. A POSITA would understand that in the portion of the top surface not covered with the metal electrode 22, i.e., in between two successive fingers, as shown in the annotated FIG. 3 below, the minority carriers, i.e., electrons, that are generated at the substrate, will first flow through layer 24 due to the surface electrical field that Tamura discloses, and will flow laterally through layer 23 to the metal contacts 22. Tamura discloses that after the heat treatment, “a crystal film was obtained, having a graded structure with a carrier concentration of 10^{20} cm^{-3} near the surface, and a resistivity of approximately $10^{-3} \Omega\text{-cm}$.” Tamura, [0017]. Based on Tamura’s disclosure, a POSITA would understand that the sheet resistance (R_{sh}) of the n-region (consisting of layers 23 and 24) is equal to 100 Ohm/sq (as stated above $R_{sh} = \rho/t = 10^{-3}(\Omega\text{-cm})/(700\text{\AA} + 300\text{\AA}) = 10^{-3}(\Omega\text{-cm})/10^{-5}\text{cm} = 100 \Omega/\text{sq}$), which is lower than the maximum sheet resistance of 500 Ohm/sq stated by the ’074 patent. Thus, Tamura discloses the top n-region consisting of layers 23 and 24; the *conductive and passivating layer* and the *interface passivation layer*, respectively, provide a low resistance path for the minority carriers to flow from the substrate (element 25) to the electrode (element 22).



Tamura, FIG. 3 (annotated, left), Tamura, FIG. 3 (annotated, right).

134. As shown below, I compare the annotated Figure 3 of Tamura with Figure 6 of the '074 patent. The comparison shows that Tamura discloses the same structure as the one in claim 1 of the '074 patent. Moreover, as per my analysis of the above limitations, Tamura discloses the same materials (shown below in bold) as the ones stated as examples in the '074 patent. In regard to the structure depicted in Figure 6 of the '074 patent, “[e]xemplary layers of cell 60 include...61: Front **metal electrode** [layer 22 in Tamura]. 62: Transparent and conductive film...like **indium tin oxide** [layer 21 in Tamura]...63: Electrically passivating and conductive film...**n-type amorphous or polycrystalline silicon** [layer 23 in Tamura]...64: Electrically passivating interface layer ...**intrinsic amorphous silicon** [layer 24 in Tamura], intrinsic polycrystalline silicon.” ’074 patent, 5:29-61. Finally, Tamura discloses a sheet resistance for the n-region, which is within the range stated in the '074 patent. Thus, Tamura discloses a *shortened charge carrier flow path* between the substrate

and the electrodes, even in the regions not covered by the metal electrodes, as this flow path is a low-resistance path.



Tamura, FIG. 3 (annotated, left), '074 patent, FIG. 6 (annotated, right).

135. As per my analysis above, Tamura discloses that the dopant diffused through *the interface passivation layer* (“an n-type crystalline silicon layer 24” in the pn junction) provides a shortened charge carrier flow path between the substrate and the electrodes through *the conductive and passivating layer* (“the n+ type crystalline silicon layer 23”) and *the interface passivation layer*.

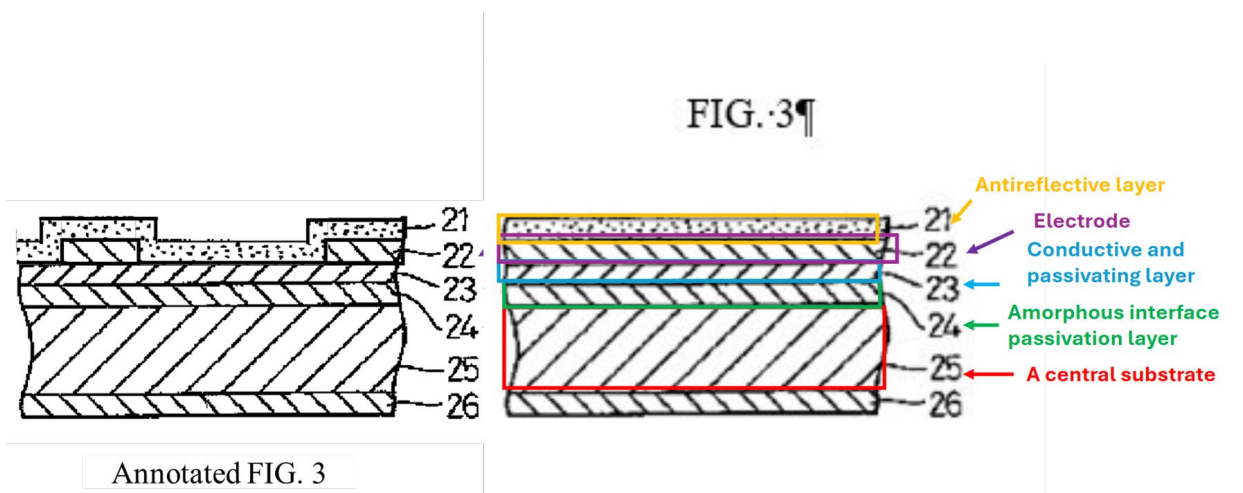
2. **Claim 2: “The method of claim 1, further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.”**

136. Tamura teaches or suggests this limitation.

137. The '074 patent allows the antireflective layer to be transparent conductive oxide. '074 patent, 8:61-64, (“102: Antireflection film, refractive index in the range of $1.4 < n < 3$; thickness < 150 nm. Examples include silicon nitride, silicon

carbide, silicon oxide, titanium oxide, **and transparent conductive oxides**. Tamura discloses depositing the *at least one antireflective layer*.

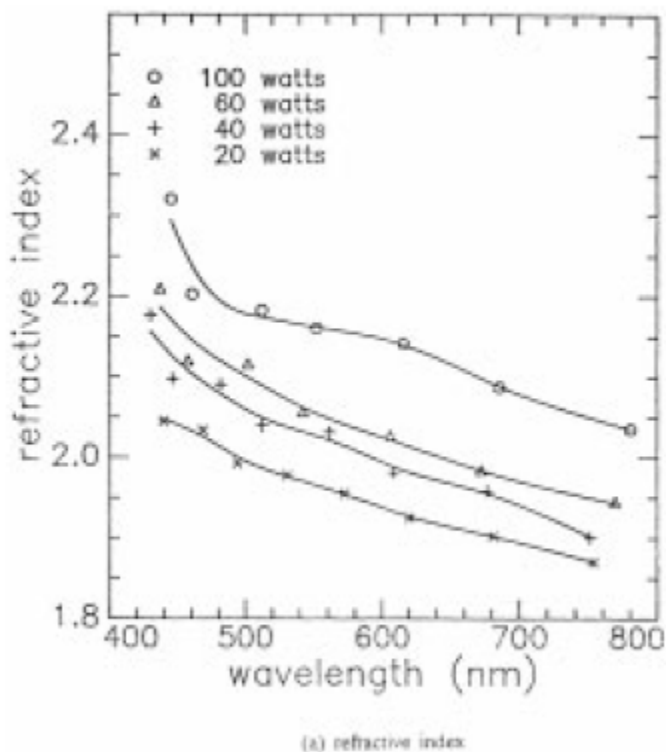
138. Tamura discloses a “transparent electrode” 21 that can be a transparent conductive oxide, *an antireflective layer*, (on the top or front side or light entering side). Tamura, [0018] (“In FIG. 3, **21 denotes a transparent electrode**”). Although Figure. 3 of Tamura depicts the antireflective layer on top of the metal electrode, element 22, as discussed above, a POSITA would understand that the cross section depicted in Figure 3 is along a direction that is parallel to one of the fingers of the comb. A POSITA would also understand that if the cross-section is drawn along a direction perpendicular to the fingers of the comb, it will appear as shown in the annotated Figure 3 shown below. A POSITA would understand that in the portion of the top surface not covered with the metal electrode 22, i.e., in between two successive fingers, as shown in the annotated FIG. 3 below, the transparent electrode acts as an antireflective layer by minimizing the amount of light that is reflected by the top surface, and thus more light is entering the solar cell.



Tamura, FIG. 3 (annotated).

139. It was well known in the art that a “transparent electrode” 21, e.g., a transparent conductive oxide such as Indium Tin Oxide (ITO) serves as an *antireflective layer* because a transparent electrode has optical transparency and can be deposited with a low index of refraction ($n < 2$) in order to minimize the difference between its index of refraction and the index of refraction of air $n = 1$ thus minimize reflection. For example, Figure 1a of Chiou demonstrates an ITO layer having an index of refraction $n < 2$. It was well known that the reflection of light incident on a material increases as the difference between the index of refraction of the material and that of air increases. See Froitzheim, 180 (referring to Figure 1 “The transparent conducting oxide (TCO) is used to enhance the lateral conductivity and **to minimize reflection losses.**”); See also Taguchi, 866, (referring to Figure 1 “The TCO layer on the top also

works as an anti-reflection (AR) layer.”); Borden, 1149 (referring to Figure 2 and disclosing “an overlaid ITO as an antireflection (AR) coating and contacting layer.”)



Chiou, FIG. 1(a).

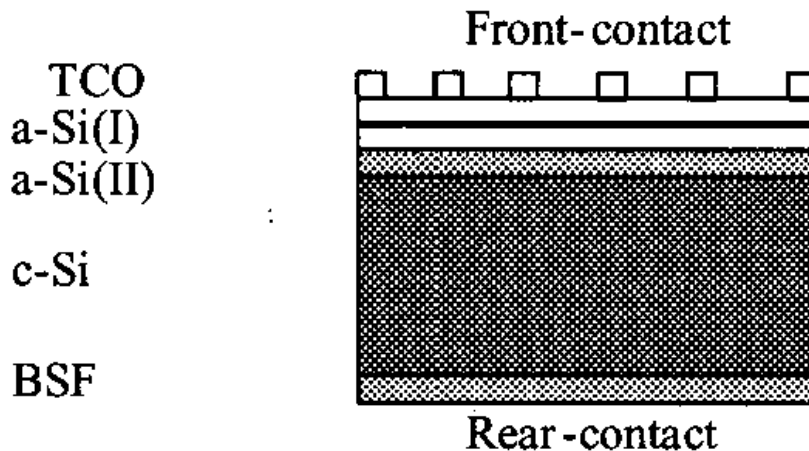


Fig. 1: Schematic structure of the prepared heterojunction solar cell. TCO is an 80 nm thick ITO, a-Si(I) is highly phosphorus doped a-Si:H(n), a-Si(II) is intrinsic a-Si:H(i), BSF is a boron diffused back surface field. The a-Si:H emitters have been prepared with and without the intrinsic buffer layer.

Froitzheim, FIG. 1.

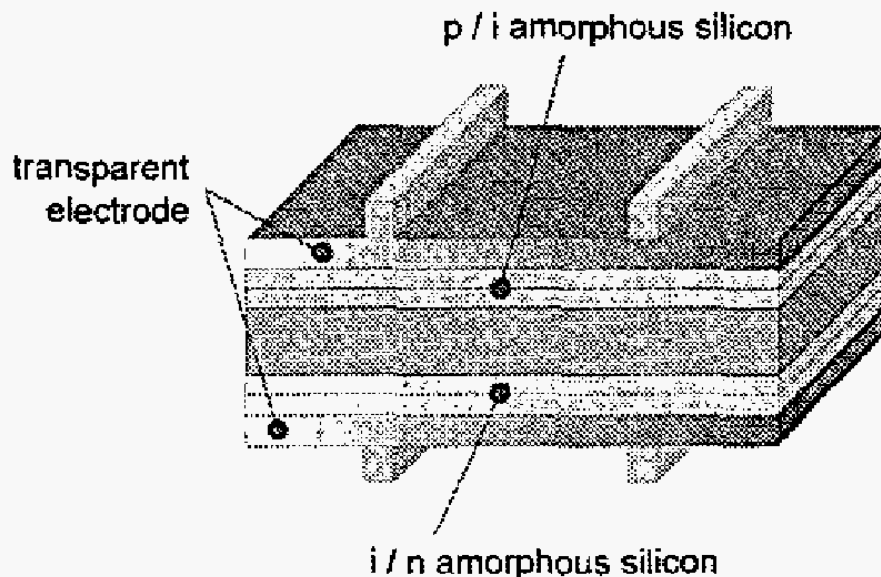
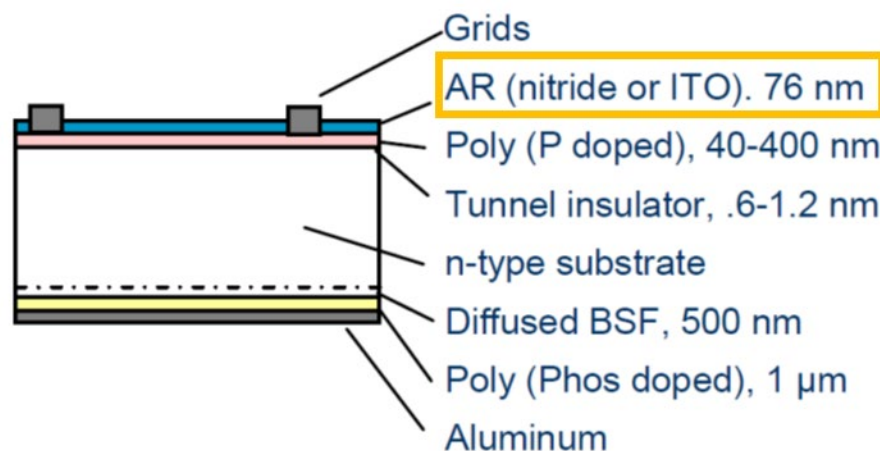


Fig. 1. Schematic diagram of the HIT cell.

Taguchi, FIG. 1.



Borden, FIG. 2 (annotated).

140. Tamura also discloses forming a good internal mirror on a back of the solar cell. Tamura also discloses a “back surface electrode” 26 that can *form a good internal mirror on a back of the solar cell*. Tamura, [0018] (“26 denotes a back surface electrode.”) A POSITA would understand that the “back surface electrode” 26 is a metal that serves as an internal mirror that reflects photons that reach the back side towards the front, thus increasing the optical path of the photons. A common back electrode used in solar cells is aluminum. It was well known that aluminum has a high reflectance. For example, Figure 12 of Smith depicts that the reflectance of aluminum is greater than 90% for wavelengths greater than 900 nm or 0.9 μm. The ’074 patent discloses “a good internal mirror in the back” (18:25-26) as a material that has a “high reflectivity for photons of more than 900 nm wavelength.” ’074 patent, 7:51-53, 12:8-9.

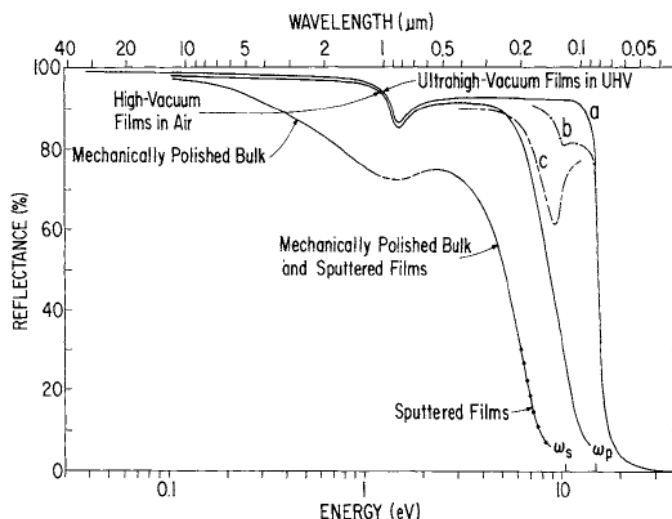
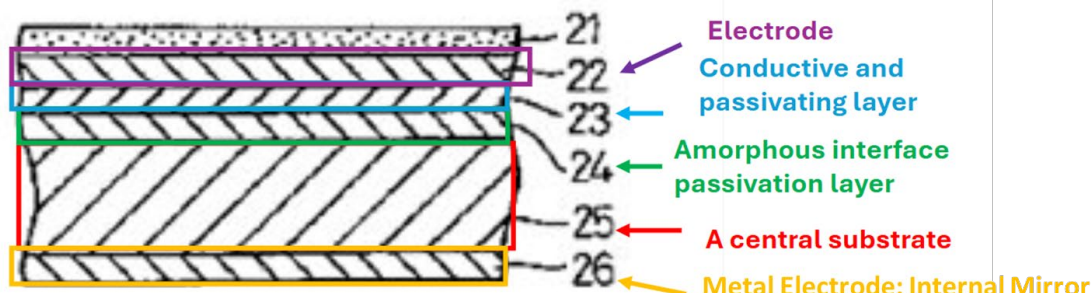


Fig. 12. The reflectance of metallic aluminum at room temperature. The uppermost curve gives the reflectance of opaque evaporated aluminum films prepared in ultrahigh vacuum. These films are presumed to be free of bulk and surface oxide contamination. The effect of light scattering and coupling to surface plasmons (at $\omega_s \approx 10.6$ eV) is illustrated by curves b and c. Curve b was obtained by Vehse *et al.* [90] for a film on a microscope slide cleaned by vapor decreasing and evaporated in a vacuum of $\sim 3 \times 10^{-8}$ torr; the "oxide-free" reflectance was obtained by extrapolation of the reflectance back to the time that the evaporation was completed. Curve c is for a uhv film with rms surface roughness σ of 18 Å, as reported by Endriz and Spicer [53]. The curve labeled high vacuum is an average for films evaporated in vacuum of the order of 10^{-5} torr. At this pressure surface and bulk oxidation occurs. The values reported for such films vary widely, especially in the ultraviolet, presumably because of surface roughness. The third curve is representative of mechanically polished samples, but the reported range of measurements is extremely large. Data for sputtered films are available from 380 nm well into the UV [44, 45]; curiously enough, they track the data for polished samples very closely.

Smith, FIG. 12.

FIG. 3



Tamura, FIG. 3 (annotated).

141. Furthermore, applying a metal electrode on the back that also serves as a mirror to reflect photons toward the front side was standard practice in fabricating solar cells. Tamura discloses that such standard practice can be performed on solar cells. Tamura, [0012] (“The formation of electrodes and the like other than the formation of the pn junction can be performed in the same manner as in a typical solar cell”). Therefore, a POSITA would understand that an internal mirror, e.g., a back surface electrode 26, as a typical industrial standard practice, is disclosed by Tamura. For example, Figure 3 of Yamamoto depicts an internal mirror forming a back reflector on the side of the solar cell opposite to the side that light enters the solar cell, in order to increase the optical path of the light. As discussed in Section V, it was known that “[l]ight-trapping technology provides a means of extending the optical path of the

incident light inside the solar cell by causing multiple reflections,” and that one way of achieving light trapping is “by introducing a highly reflective layer at the back surface to reflect the incident light without absorption loss” and that “[t]his highly reflective back layer also acts as the solar cell’s back electrode.” Yamamoto, 941.

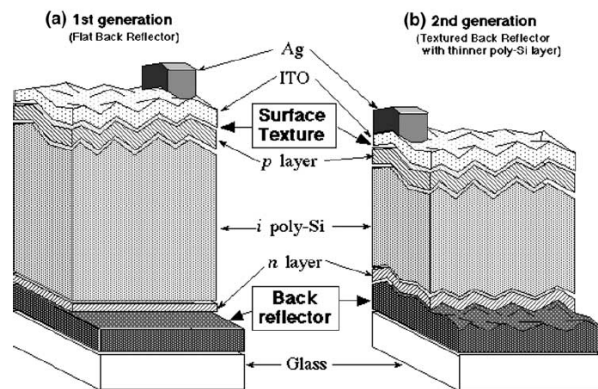


Fig. 3. Cross-sections through light-trapping microcrystalline silicon solar cell devices: (a) first generation (flat back reflector); (b) second generation (textured back reflector, thinner polycrystalline silicon layer).

Yamamoto, FIG. 3.

3. Claim 3: “The method of claim 1,”

142. Tamura teaches or suggests this limitation.

143. See discussion of claim 1.

- a) Limitation 3[a]: “wherein the depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer comprises depositing an amorphous silicon-containing compound over the substrate”**

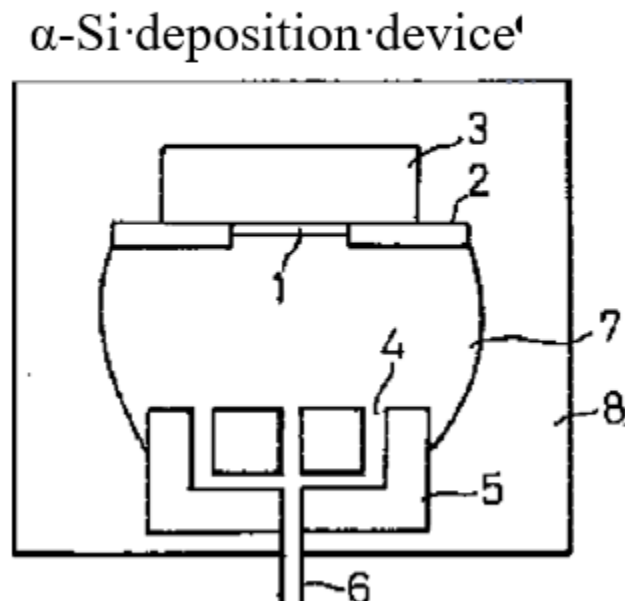
144. Tamura teaches or suggests this limitation.

145. Tamura discloses that both amorphous layer 12 (*interface passivation layer*) and amorphous layer 13 (*conductive and passivating layer*), depicted in FIG. 2,

are layers of amorphous silicon. Tamura, [0015] (“Next, a high-concentration n^+ type amorphous silicon layer 13 was deposited on the undoped amorphous silicon layer 12 under the following conditions.”)

146. Tamura further discloses a deposition device, depicted in Figure 1, to manufacture the solar cell. Tamura, [0014] (“A deposition device as depicted in FIG. 1 was used. In the drawing, reference numeral 1 denotes a silicon substrate, 2 denotes a substrate holder and RF electrode, 3 denotes a heater, 4 denotes a gas nozzle, 5 denotes an RF electrode, 6 denotes a gas introducing pipe, 7 denotes a plasma generation region, and 8 denotes a vacuum chamber...”). Tamura also discloses that the deposition temperature is 170°C, the plasma power is 10W, and the source gas is SiH_4 . Tamura [0015]-[0016]. A POSITA would understand that Tamura’s deposition device is a Plasma Enhanced Chemical Vapor Deposition (PECVD). *See* Fuhs, 125-126 (describing the PECVD process “PECVD, silane (SiH_4) or mixtures of silane with rare gases or hydrogen are decomposed in a glow discharge. In most cases, parallel-plate systems have been used in stainless steel reactors. The most important deposition parameters are substrate temperature, base pressure, flow rate of the process gas, power density, and frequency. High-quality a-Si:H films are grown at deposition rates of typically 0.1 nm/s at substrate temperatures in the range 150-250°C.”)

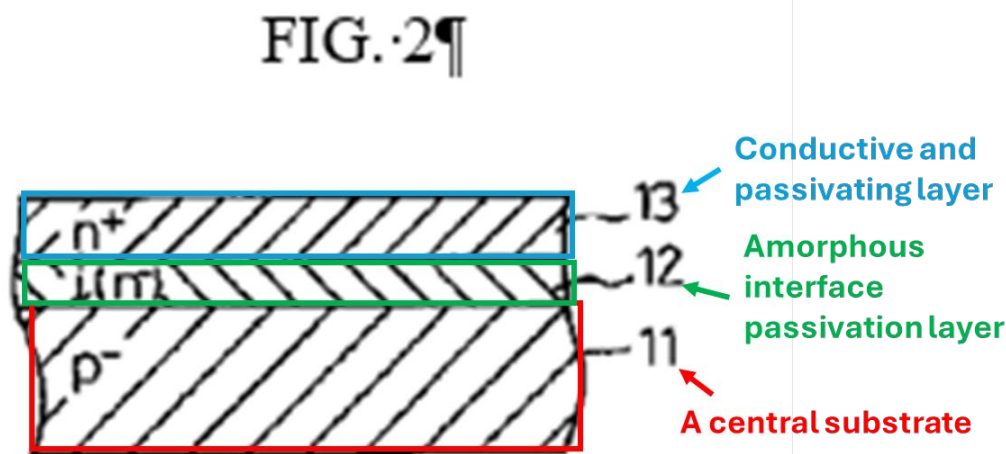
FIG. 1



Tamura, FIG. 1.

147. A POSITA would understand that the plasma deposition conditions disclosed by Tamura for *depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer* (the two amorphous silicon layers 12 and 13), as depicted in Figure 2 below, in the growth apparatus shown in Figure 1 yield a material known as hydrogenated amorphous silicon, which is *an amorphous silicon-containing compound over the substrate* (“the p-type silicon substrate 11”). See e.g., Fuhs, 124, (“Today hydrogenated amorphous silicon, a-Si:H, offers a mature material and device technology, used for solar cells, thin-film transistors, sensors, imaging, radiation detectors and displays.”) See also Fuhs, 126

(“The hydrogen content can vary widely with the deposition conditions (5-40%)...In optimized films, the hydrogen concentration amounts to 5-15%.”)



Tamura, FIG. 2 (annotated).

148. The '074 patent lists PECVD deposited amorphous silicon materials as examples for the passivating interface layer and the electrically passivating interface layer. '074 patent, 5:56-60 (“64:Electrically passivating interface layer;... Examples include ...intrinsic amorphous silicon...”); 5:42-51 (“63: Electrically passivating and conductive film;...Examples include...n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon.”) Moreover, the '074 patent lists as an example the PECVD method disclosed by Tamura. '074 patent, 15:54-55 (“Most layers within the solar cell structure described above can be deposited or grown with methods such as PECVD, ...), *see also* '074 patent, 15:66-16:3 (“a PECVD deposition can be done

on one side of a wafer without the deposition on the other side. PECVD tools are available on an industrial scale but may only operate at temperature regimes where amorphous or microcrystalline silicon layers can be deposited.”) A POSITA would understand that all intrinsic amorphous silicon or phosphorus-doped amorphous silicon films deposited by PECVD are amorphous silicon containing compounds known as hydrogenated amorphous silicon.

b) Limitation 3[b]: “and the providing thermal treatment of about 500°C. or higher separates the amorphous silicon-containing compound into the at least one interface passivation layer and the at least one conductive and passivating layer.”

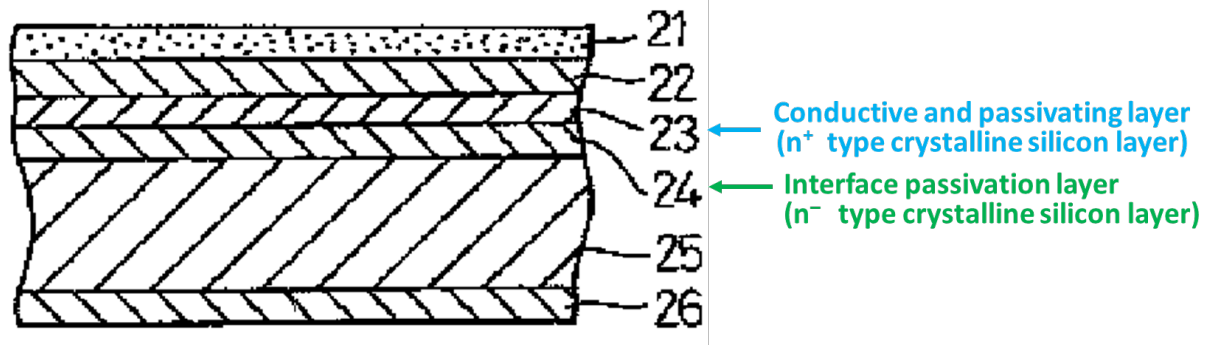
149. As I explained for limitation 3[a] above, a POSITA would understand that the deposition conditions disclosed by Tamura to deposit the two amorphous silicon layers 12 and 13, as depicted in Figure 2, yield an amorphous silicon-containing compound: hydrogenated amorphous silicon.

150. A POSITA would also understand that the thermal treatment will *separate the amorphous silicon-containing compound into at least one interface passivation layer* (the crystallized amorphous silicon layer 12 relabeled by Tamura as element 24 in Figure 3) *and at least one conductive and passivating layer* (the crystallized amorphous silicon layer 13 relabeled by Tamura as element 23 in Figure 3) for the following reasons.

151. It was well known that “[t]hemodynamically, amorphous silicon (a-Si) is in a metastable state... Heating above a temperature of about 500°C usually induces a transition into the thermodynamically more stable crystalline phase. The kinetics of solid phase crystallization (SPC) are characterized by nucleation and growth of crystal clusters at the expense of the surrounding amorphous material.” Fuhs, 125. Therefore, a POSITA would understand that during the thermal treatment disclosed by Tamura, the following two phenomena occur.

152. First, the initially undoped amorphous silicon layer 12 (*interface passivation layer*) crystallizes by solid phase crystallization, which causes part of the amorphous silicon at the interface between amorphous silicon layer 12 and substrate 11 to crystallize epitaxially on the single-crystal substrate (“the p-type silicon substrate 11”). Tamura, [0005] (“heat-treating the undoped and second conductivity-type amorphous silicon layers to convert the layers into crystalline silicon layers, thereby forming a pn junction having a graded structure... by **solid phase epitaxy**.”) Moreover, Tamura discloses that after the thermal treatment the initially undoped “amorphous silicon layer 12” becomes an “n⁻ type crystalline silicon,” the *interface passivation layer*, denoted as layer 24 in FIG. 3, which is distinct from the layer 23 “an n⁺ type crystalline layer,” the *conductive and passivating layer*, formed by the crystallized “n⁺ type amorphous silicon layer.”

FIG. 3



Tamura, FIG. 3 (annotated).

153. Tamura's disclosure on removing oxide film with hydrofluoric acid further confirms that the epitaxial growth phenomenon happens during thermal treatment in regions of the substrate not covered by an oxide film which was well known to occur naturally on silicon and referred as native-oxide. Tamura, [0007] ("The surface of the substrate is highly preferably subject to a cleaning treatment prior to deposition of an amorphous silicon layer in order to form a pn junction of favorable quality by **solid phase epitaxy**. Specifically, after organic cleaning, a clean substrate surface is achieved by etching with an alkaline solution or mixed acid"), *see also* Tamura, [0014] ("after performing alkali etching...**removal of an oxide film using hydrofluoric acid**").

154. Second, the initial n^+ type amorphous silicon layer 13 (*one conductive and passivating layer*) crystallizes and becomes the " n^+ type crystalline layer" denoted as layer 24 in Tamura's Figure 3. A POSITA would also understand that layer 13 is

not in direct contact with the substrate thus portions of it crystallize by random nucleation and growth resulting in a different, i.e. polycrystalline, structure than the structure, i.e. epitaxial, of the crystallized layer 12. Thus, a POSITA would understand that *the thermal treatment* would separate *the amorphous silicon-containing compound* into the *conductive and passivating layer* (the n⁺ type crystalline silicon layer 24) and the *interface passivation layer* (the n- type crystalline silicon layer 23).

155. Therefore, a POSITA would understand that Tamura teaches a thermal treatment above 500°C (“low-temperature process (600°C to 700°C)”) that *separates the amorphous silicon-containing compound into the at least one interface passivation layer and the at least one conductive and passivating layer*.

4. Claim 4: “The method of claim 1, wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.”

156. Tamura teaches or suggests this limitation.

157. As I discussed above in claim 3, Tamura discloses the crystallization of amorphous silicon layer 12 (*interface passivation layer*) by “solid phase epitaxy”, which a POSITA would understand to form crystalline regions that have the same crystal structure as the underlying substrate; in other words wherever the amorphous silicon layer 12 is in direct contact with the substrate, the crystal structure of the substrate extends above the substrate (“the p-type silicon substrate 11”) and into the crystallized amorphous silicon layer.

158. A POSITA would know that such epitaxially crystallized regions may not be continuous laterally, as residual native oxide of silicon may prevent epitaxial crystallization in certain regions. Accordingly, the epitaxially crystallized regions, which result from the *thermal treatment* in the *interface passivation layer* (amorphous silicon layer 12), form the “*perforation*” as *carriers would transport through* these regions since the carrier mobility is higher in such single crystal regions compared to the mobility in other regions in which the solid phase epitaxy was prevented by the presence of silicon’s native oxide. It was well known that silicon’s native oxide grows easily upon exposure of silicon to air. Thus a portion of the silicon substrate surface, even after a removal step with hydrofluoric acid, may still be covered with it as the silicon substrate after the removal step, may get oxidized again upon exposure to air prior to loading to the PECVD deposition. It was well known that complete removal of the native oxide and thus continuous epitaxial growth occurs only when an in-situ removal of the oxide film occurs prior to the epitaxial deposition of a silicon layer, but this occurs at high temperatures in special epitaxial deposition reactors. A POSITA would understand that such complete removal of the native oxide is not possible in Tamura’s “deposition device” which is a typical PECVD reactor; moreover Tamura did not disclose any in-situ oxide removal steps prior to the deposition of the amorphous silicon layer 12.

5. Claim 5: “The method of claim 1,”

159. Tamura teaches or suggests this limitation.

160. See discussion of claim 1.

a) Limitation 5[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and”

161. Tamura teaches or suggests this limitation.

162. See discussion of limitation 3[a].

b) Limitation 5[b]: “wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.”

163. Tamura teaches or suggests this limitation.

164. Tamura teaches that the *thermal treatment initiates crystallization of the amorphous silicon layer 13 (at least one conductive and passivating layer)* into a crystalline silicon layer. Tamura, [0005] (“heat-treating the undoped and second conductivity-type amorphous silicon layers to convert the layers into crystalline silicon layers”. See also Tamura, [0010] (“the deposited undoped and **second conductivity-type amorphous silicon layers are crystallized by heat treatment.**”) See also Tamura, [0011] (“This heat-treatment crystallizes the undoped and second conductivity-type amorphous silicon layers.”)

165. Tamura further discloses that the “crystal structure of the resulting film was observed by ultraviolet surface reflection and RHEED (reflection high energy

electron diffraction), and...[t]he results confirmed that a crystal film was obtained.” Tamura, [0017]. Tamura teaches that the “crystal structure” that results by the heat treatment depends upon the temperature. Tamura, [0010] (“At temperatures below 500°C, it is difficult to obtain favorable crystals, whereas at higher temperatures, random crystal nucleation occurs, preventing epitaxial growth and resulting in polycrystals with small grain sizes.” Tamura also discloses the use of “silicon polycrystals” as the semiconductor substrate for solar cells because “[s]ilicon polycrystals have the advantage of being easier to produce in large areas as compared to silicon monocrystals and are also inexpensive, making silicon polycrystals very promising as a semiconductor substrate for solar cells.” Tamura, [0002]. Tamura also demonstrates that solar cells on a polycrystal substrate having the following properties: “an open voltage of 0.56 V, a short circuit current of 29 mA/cm² on a polycrystal substrate and a conversion efficiency of 13%.” Tamura, [0018]. Based on Tamura’s disclosure, a POSITA would understand that the amorphous silicon layer 13 (the *conductive and passivating layer*) is in direct contact with the amorphous silicon layer 12 and thus during the thermal anneal, at least a portion of this layer will be crystallized by random nucleation, resulting in a polycrystalline film. A POSITA would also understand that even when the fabrication conditions are ideal (proper temperature and no native oxide) and the heat treatment results in “solid phase epitaxy,” the resulting structure of the crystallized layer 13 will resemble that of the “polycrystal substrate”

and thus the amorphous silicon layer 13 (*at least one conductive and passivating layer*) is crystallized *into a polycrystalline film*.

6. Claim 6: “The method of claim 1,”

166. Tamura teaches or suggests this limitation.

167. See discussion of claim 1.

a) Limitation 6[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and”

168. Tamura teaches or suggests this limitation.

169. See discussion of limitation 3[a].

b) Limitation 6[b]: “wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer and increases the optical transmissivity.”

170. Tamura teaches or suggests this limitation.

171. Tamura teaches that *the thermal treatment initiates crystallization* of the amorphous silicon layer 13 (*one conductive and passivating layer* also referred to by Tamura as the second conductivity-type amorphous silicon layer). Tamura, [0011] (“This heat treatment **crystallizes** the undoped and **second conductivity-type amorphous silicon layers.**”)

172. Tamura further teaches that *the thermal treatment increases the optical transmissivity* through crystallizing the amorphous silicon layer 13. Tamura, [0017] (“A crystal structure of the resulting crystallized film was observed by ultraviolet

surface reflection and R-HEED (reflection high energy electron diffraction). The results confirmed that a crystal structure was obtained.”). A POSITA would also know that when the amorphous silicon layer 13 crystallizes and transforms into polycrystalline silicon, its optical transmissivity increases as the light absorption coefficient of crystalline silicon is lower than that of amorphous silicon. For example, Figure 7.2 of Fuhs depicts that for the photons with energy of about 1.8 eV or higher, i.e. for photons corresponding to the entire visible spectrum of the light (i.e., from ultraviolet to red), the absorption coefficient of amorphous silicon is higher than that of crystalline silicon. Fuhs, 128, FIG. 7.2; *See also* Markvart, 107, FIG. 7.

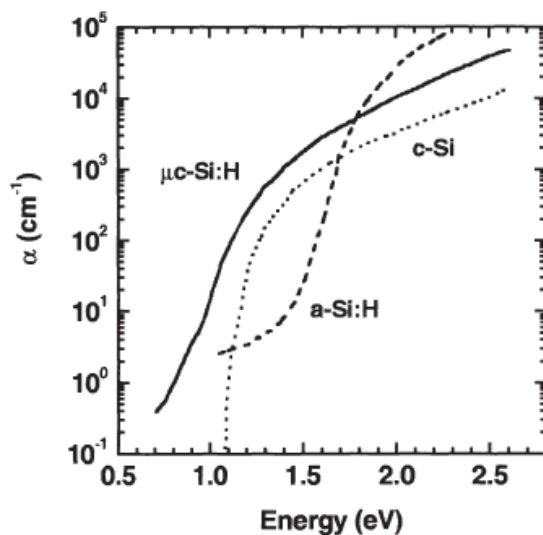
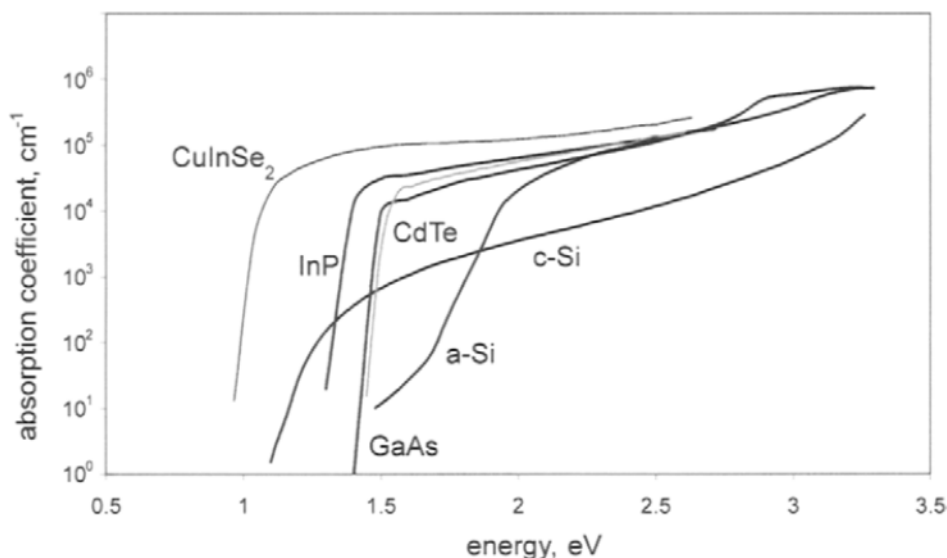


Fig. 7.2. Absorption edges of a-Si:H, monocrystalline Si and μ c-Si:H

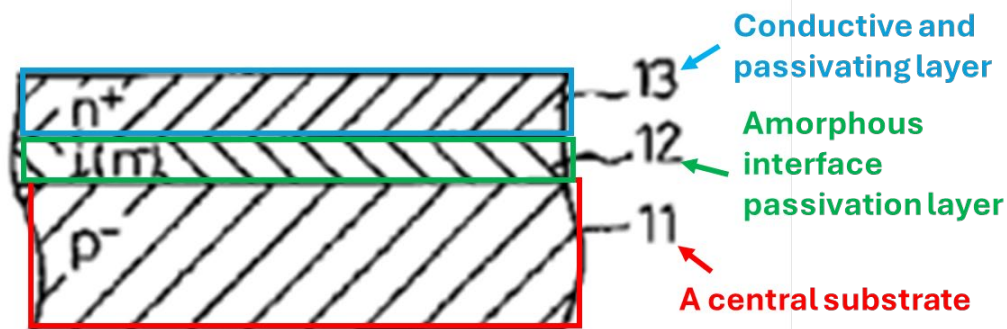
Fuhs, FIG. 7.2.



Markvart, FIG. 7.

173. Since less light is absorbed by the crystallized silicon layer 13, its optical transmissivity is higher after the thermal treatment. *See e.g.*, Shah, 696 (“Amorphous silicon has, in the visible range of the spectrum, a higher optical absorption coefficient than crystalline silicon and thus, can have thicknesses much less than 1 μm .”)

FIG. 2



Tamura, FIG. 2 (annotated).

7. Claim 7: “The method of claim 1,”

174. Tamura teaches or suggests this limitation.

175. See discussion of claim 1.

a) Limitation 7[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and”

176. Tamura teaches or suggests this limitation.

177. See discussion of limitation 3[a].

b) Limitation 7[b]: “wherein the thermal treatment activates doping atoms in the compound.”

178. Tamura teaches or suggests this limitation.

179. As I explained for limitation 3[a] above, A POSITA would understand that the deposition conditions disclosed by Tamura to deposit the two amorphous silicon layers (layers 12 and 13 in FIG. 2) yield hydrogenated amorphous silicon, which is an amorphous silicon-containing *compound*. Tamura discloses a thermal treatment at 600°C or higher. Tamura, [0016] (“Next, the substrate 11, on which the amorphous silicon layers 12, 13 were deposited, was heated in an image furnace at a rate of 120°C/min, maintained at 600°C for 5 minutes, and then slowly cooled.”) and Tamura, [0012] (“After the heat treatment for solid phase growth, the temperature can be increased to a temperature equal to or higher than the solid phase growth temperature to diffuse a doped impurity and improve a junction interface.”) A POSITA

would understand that the thermal treatment disclosed by Tamura (600°C or higher) *activates doping atoms in the compound*, which results in an n^+ type crystalline silicon layer (depicted by element 23), and an n^- type crystalline silicon layer (depicted by element 23) in Figure 3. *See* Tamura, [0018].

180. Tamura also discloses that the thermal treatment *activates doping atoms in the compound* as it creates a pn junction with a graded structure. Tamura, [0011] (“**the heat treatment** crystallizes the undoped and **second conductivity-type amorphous silicon layers**, forming a pn junction having a graded structure...The **dopant concentration** of the crystallized second conductivity-type silicon layer can easily **be increased to approximately 10^{21}cm^{-3}** ”). Moreover, Tamura discloses that after the thermal treatment “the electrical properties were observed by Hall effect measurement and spreading resistance measurement” and that the “results confirmed that a crystal film was obtained, having a graded structure **with a carrier concentration of 10^{20}cm^{-3} near the surface, and a resistivity of approximately $10^{-3}\Omega\cdot\text{cm}$ (carrier concentration).**”) *See* Tamura, [0017]. A POSITA would understand that the carrier characteristics disclosed by Tamura, i.e. “a carrier concentration of 10^{20}cm^{-3} near the surface” and “a pn junction with a graded structure,” refer to the carriers that result from the dopants as a direct result of their activation by the thermal treatment. It was well known that the measurement techniques disclosed by Tamura (i.e., Hall effect and spreading resistance) determine the characteristics of the carriers (e.g.,

mobility, concentration, position) in the material because *the thermal treatment activates the doping atoms* in the crystallized film. See e.g., Schroder, 29 (“The spreading resistance probe technique has been in use since the 1960s...it is mainly used today to generate resistivity and dopant density depth profiles. It has a very high dynamic range (10^{12} - 10^{21} cm⁻³) and is capable of profiling very shallow junctions into the nm regime.”)

8. Claim 8: “The method of claim 1,”

181. Tamura teaches or suggests this limitation.

182. See discussion of claim 1.

a) Limitation 8[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound and”

183. Tamura teaches or suggests this limitation.

184. See discussion of limitation 3[a].

b) Limitation 8[b]: “wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.”

185. Tamura teaches or suggests this limitation.

186. Tamura discloses, “the heat treatment crystallizes the undoped and second conductivity-type amorphous silicon layers, **forming a pn junction having a graded structure.**” See Tamura, [0011].

187. Specifically, this “graded structure” is formed by the diffusion of the dopant atoms into the substrate to create a structure in which the concentration of the dopant atoms changes “gradually” from high concentration at the surface ($\geq 10^{20} \text{ cm}^{-3}$) to the same level as that of the substrate (“approximately 10^{17} to $10^{15}/\text{cm}^3$.”) Tamura, [0011] (“The dopant concentration of the crystallized second conductivity-type silicon layer can easily be increased to approximately 10^{21} cm^{-3} ”), *see also* Tamura, [0017] (“The results confirmed that a crystal film was obtained, having a graded structure with a carrier concentration of 10^{20} cm^{-3} near the surface, and a resistivity of approximately $10^{-3} \Omega \cdot \text{cm}$ (carrier concentration).”); Tamura, [0006] (“The first conductivity-type silicon crystal layer on the substrate surface... having a dopant concentration of approximately 10^{17} to $10^{15}/\text{cm}^3$.”) Tamura also discloses that “[a]fter the heat treatment for solid phase growth, the temperature can be increased to a temperature equal to or higher than the solid phase growth temperature to diffuse a doped impurity and improve a junction interface” Tamura, [0012]. Moreover, Tamura discloses that “the low temperature prevents a dopant from diffusing deeply into the substrate” and “a pn junction having a shallow and steep concentration gradient is basically obtained.” Tamura, [0010]-[0011].

B. Ground 2: Claims 1-2 and 4-8 are Anticipated or Rendered Obvious by Borden,

1. Claim 1

a) Limitation 1[pre]: “A method of fabricating a solar cell, comprising;”

188. To the extent the preamble is limiting, Borden teaches or suggests this preamble.

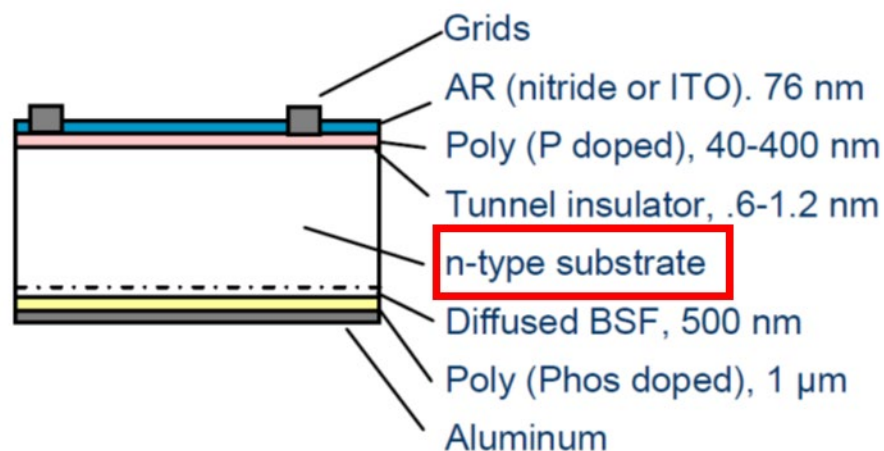
189. For example, Borden discloses that “[w]e report use of heavily doped polysilicon combined with a tunnel dielectric to provide an alternate to diffused junctions for silicon solar cells.” Borden, 1149.

b) Limitation 1[a]: “providing a wafer as a central substrate;”

190. Borden teaches or suggests this limitation.

191. Borden discloses an n-type CZ wafer as a central substrate. Borden, 1149 (“Because the IC equipment runs **300 mm wafers**, we have been restricted to 780 μm thick **CZ substrates** without texture, and are constrained to available 300 mm substrates...most processing has been on **n-type**”), *see also* Borden, 1150. Figure 2 of Borden depicts the structure of a single-sided device, and Figure 3 depicts the corresponding process flow, while Figure 6 depicts the experimental lifetimes measured on symmetric front/back polysilicon emitter (PE) structures; all three of these figures depict the use of n-type CZ silicon substrates, i.e., 300 mm n-type silicon wafers. Moreover, as shown in Figure. 2, the n-type substrate, which is the starting n-

type single crystal wafer, before the deposition of the various layers, is a *central substrate* with layers above and below it after the completion of the manufacturing process specifically having as shown a tunnel insulator, a p-type doped polycrystalline silicon layer, an antireflective (AR) layer and metal grid electrodes on the top or light entering side and phosphorus doped polycrystalline silicon layer and an aluminum metal electrode on the back side. Thus, the n-type CZ wafer/n-type substrate in Borden's solar cell is a central substrate.



Borden, FIG. 2 (annotated).

[A] Start – n-Cz (770 μm) [B]	
Back poly 1 μm phos 7e20/cm ³	
Drive-in RTA 4 mins 1000°C	
HF clean	
Tunnel layer (various, 6-12Å)	
a-Si(B) (20 nm)	a-Si(B) (200 nm)
RTA	
ITO	SiNx
Back contact (Al)	
Front contact	

Borden, FIG. 3 (annotated).

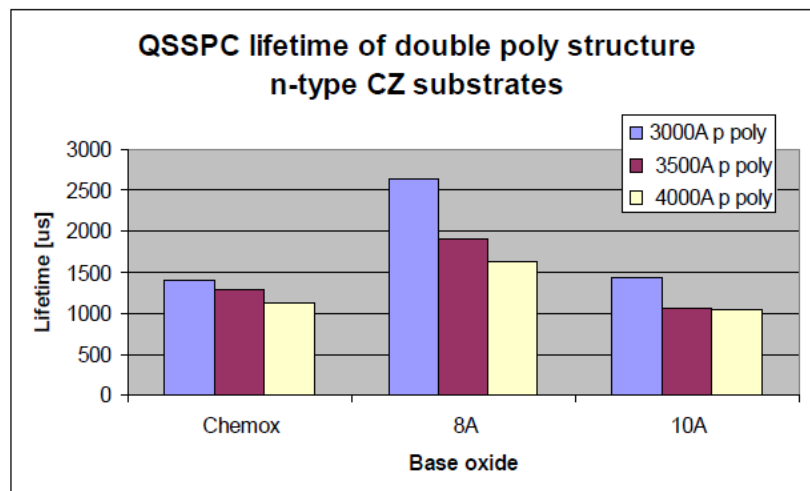


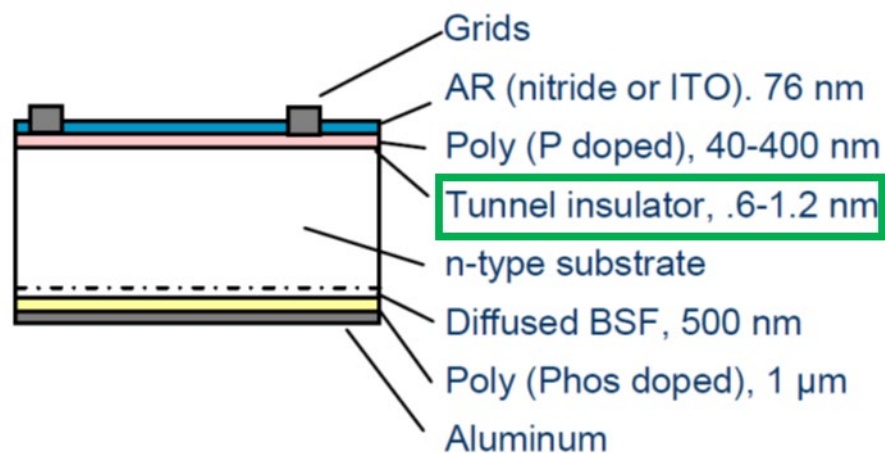
Figure 6: QSSPC lifetimes for symmetric front/back PE structures on n-type CZ.

Borden, FIG. 6.

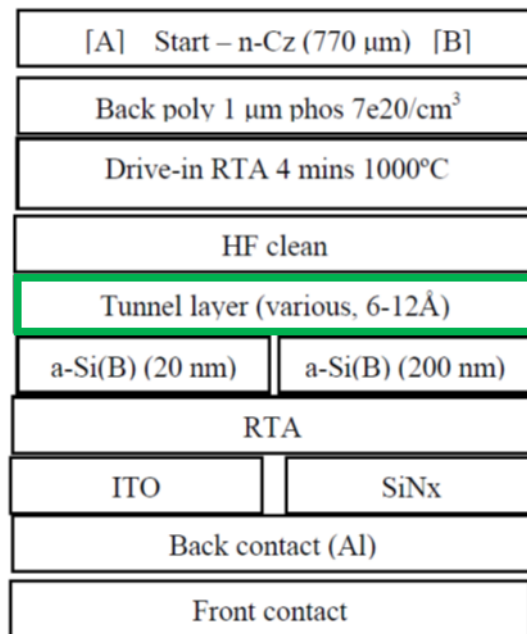
c) **Limitation 1[b]: “depositing or growing at least one amorphous interface passivation layer over the substrate;”**

192. Borden teaches or suggests this limitation.

193. Borden discloses growing thin **tunnel dielectrics** (also referred to as **tunnel layer** or **tunnel insulator**) over the front and/or back of the n-type substrate. Borden, 1149 (“Thin tunnel dielectrics (6-12Å) are fabricated using methods adapted from IC processing...When combined with heavily doped polysilicon, they can form an ideal step junction with interface passivation, enabling low dark currents not possible with diffused emitters”), *see also* Borden, 1150-51, FIGs 1-3, 5-7, 9, 10. Borden’s tunnel dielectric, tunnel layer or tunnel insulator, is the *amorphous interface passivation layer over the substrate*.



Borden, FIG. 2 (annotated).



Borden, FIG. 3 (annotated).

194. First, a POSITA would understand that the tunnel dielectrics are grown directly on the substrate and thus are “over the substrate.” Borden discloses two methods for forming tunnel dielectrics: chemical oxidation (“chem-ox”) and rapid thermal oxidation (“RTO”) of the silicon substrate. Borden, 1150 (“Three base oxide layers were used: chem-ox, which is a chemical oxide formed after the standard MOS clean, and 8 and 10 $\text{\AA}$ thick rapid thermal oxides (RTO).”) Also, a POSITA would understand that the material of these tunnel dielectrics is a silicon oxide. It was well known that silicon oxidizes and thus a thin silicon oxide grows via a chemical reaction of the silicon substrate with chemicals that are part of the “MOS clean.” It was also well known that silicon oxide grows via the reaction of silicon with a gas source of oxygen (e.g., O_2) at an elevated temperature. It is commonly known that the structure

of a material (i.e., single crystal, polycrystalline or amorphous) depends upon the material itself (i.e., its chemical composition) and the way this material is processed or formed. It was well known that silicon oxides grown on a silicon substrate, either with chemical oxidation or thermal oxidation, are amorphous materials. Therefore, Borden discloses that the tunnel dielectrics are amorphous in nature and over the substrate.

195. Second, a POSITA would understand the tunnel dielectrics is passivating, because Borden explicitly teaches that the tunnel dielectrics can serve a passivation function. Borden, 1149 (“Thin tunnel dielectrics (6-12Å) are fabricated using methods adapted from IC processing. These serve as diffusion barriers and **passivation layers**. When combined with heavily doped polysilicon, they can form an ideal step junction with **interface passivation**, enabling low dark currents not possible with diffused emitters. We show that it is possible to obtain hyper-abrupt junctions with the tunnel layer providing **interface passivation**, and that these junctions obtain a V_{oc} of 676 mV on 780 μm thick substrates.”) Borden refers to the band diagram of the solar cell with thin “tunnel insulator” layers in Figure 1 as a “cell with a tunnel insulator **passivated interface**.”

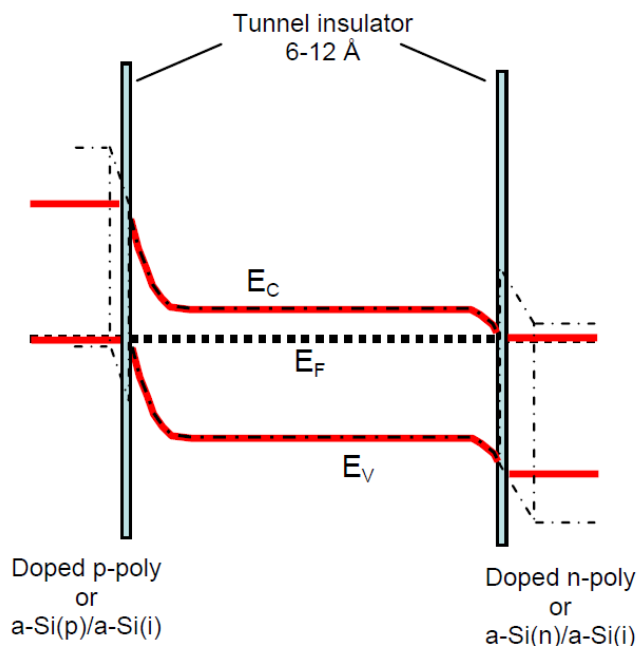
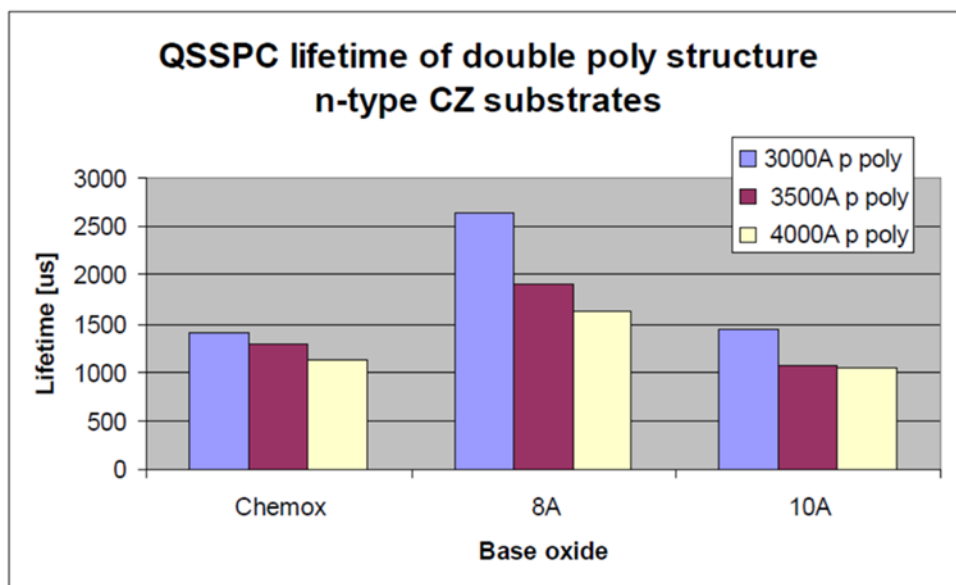


Figure 1: Comparison of band structures for doped polysilicon--c-Si(n) cell with a tunnel insulator passivated interface (red and blue) and a-Si(p)--c-Si(n) heterojunction (black) cells.

Borden, FIG. 1.

196. Borden also illustrates the impact of different tunnel dielectric materials—RTO dielectrics and chem-ox—on the lifetime of minority carriers. Borden, 1150 (“To characterize the passivation performance of the PE structure, n-type CZ wafers were coated front and back with a thin tunnel layer. Three base oxide layers were used: chem-ox, which is a chemical oxide formed after the standard MOS clean, and 8 and 10Å thick rapid thermal oxides (RTO).” *See also* Borden, FIG. 6. Borden also teaches that RTO yields a higher lifetime, thereby “provid[ing] improved interface passivation.” Borden, 1150-1151.



Borden, FIG. 6.

197. The '074 patent also acknowledges that dielectrics can provide interface passivation. '074 patent, 3:50-53 (“Surface passivation provides suppression of recombination of electrons and holes at or in the vicinity of certain physical surfaces within the solar cell. Surface recombination can be reduced by the application of dielectric layers. These layers reduce the interface density of states and therefore reduce the number of recombination centers. Two examples are thermally grown silicon oxide and PECVD deposited silicon nitride”). In several embodiments, the '074 patent lists “silicon oxide” as an example of electrically passivating interface layer, *see* e.g., '074 patent, 5:58-59; 7:1:1; 8:7-8; 10:10-11; 11:32-33; 12:40-41. Moreover, the '074 patent also acknowledges that “thermal oxidation or plasma deposition or plasma assisted oxidation can be used to form the interface passivating layer(s).” '074

patent, 15:58-60. It is important to note that according to the prior art cited by Borden, it was well known in the art that “a thin interfacial oxide can greatly enhance performance” of a solar cell due to its interface passivation property. Borden, 1149 (citing Martin Green, *Silicon Solar Cells: Advanced Principles & Practice* ch. 9 (1995)).

d) Limitation 1[c]: “depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant,”

198. Borden teaches or suggests this limitation.

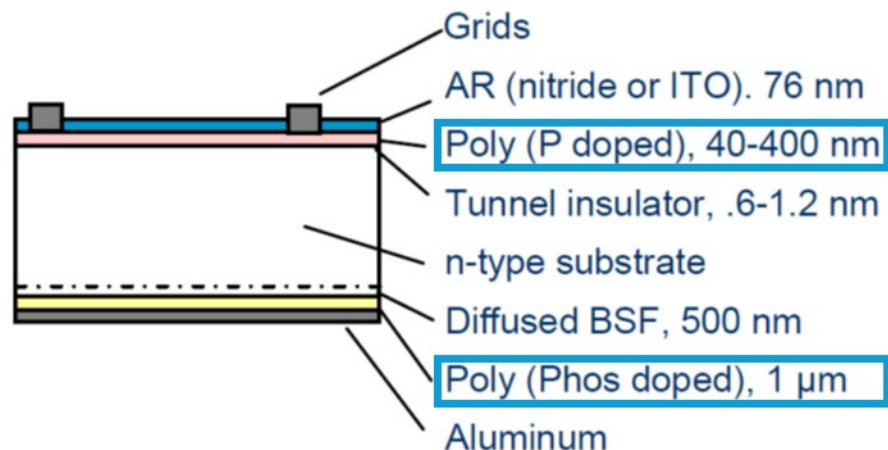
199. Borden discloses depositing an amorphous silicon layer which is p-type doped directly on top of the tunnel insulator layer, the *interface passivation layer*, Borden’s p-type doped amorphous silicon layer is the *conductive and passivating layer*. Borden, 1150 (“n-type CZ wafers were coated front and back with a thin tunnel layer...Amorphous silicon was then deposited and crystallized with a 30 second RTA at 1000°C.”)

200. Borden further discloses that the deposited amorphous silicon is doped p-type with a boron dopant. Borden describes this doped amorphous silicon layer as “a-Si(B)” in Figure 3. Borden discloses that after the deposition of the amorphous silicon, a rapid thermal annealing (RTA) step is performed, which crystallizes the doped amorphous silicon. Borden refers to the crystallized layer as “poly (P doped).”

Borden, 1150, FIGs. 2, 3. A POSITA would understand that the “poly (P doped)” designation refers to a layer that is p-type doped as this layer is doped with boron which belongs in column III of the periodic table and thus acts as a p-type dopant in silicon.

[A] Start – n-Cz (770 μm) [B]	
Back poly 1 μm phos $7\text{e}20/\text{cm}^3$	
Drive-in RTA 4 mins 1000°C	
HF clean	
Tunnel layer (various, 6-12 $\text{\AA}$)	
a-Si(B) (20 nm)	a-Si(B) (200 nm)
RTA	
ITO	SiNx
Back contact (Al)	
Front contact	

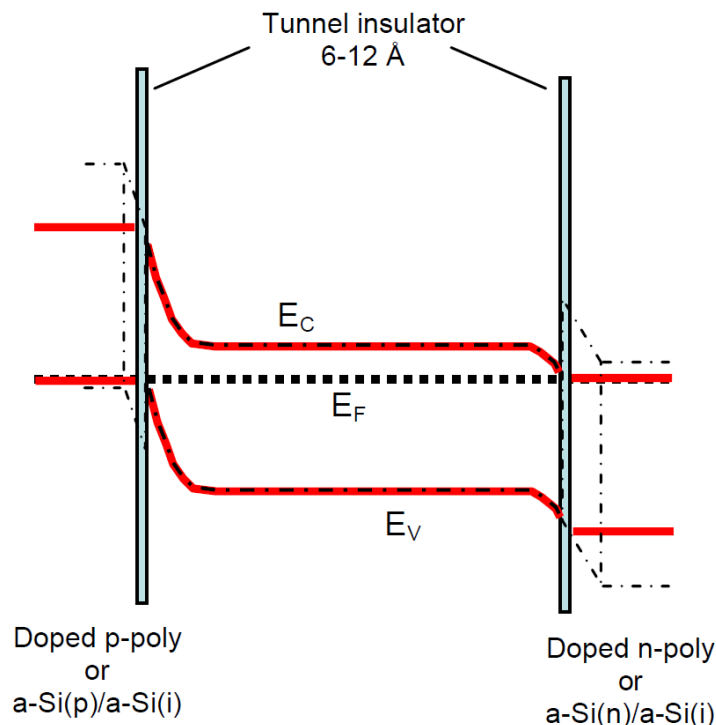
Borden, FIG. 3 (annotated).



Borden, FIG. 2 (annotated).

201. A POSITA would understand that a doped polysilicon layer is conductive and passivating.

202. First, a POSITA would understand that a doped polysilicon layer is conductive. Specifically, Borden Figure 1 demonstrates that in the “doped p-poly” (i.e., boron-doped polysilicon), the Fermi level (E_F) is located near the valence band edge (E_p), indicating that the material has a high concentration of carriers in the valence band (known as holes) which can move freely and thus increase the electrical conductivity of this layer. It was well known that when boron is introduced in silicon the concentration of electrical carriers, specifically the positively charged carriers, increases as each boron atom introduces a positively charged carrier, i.e. a “hole”, as explained in Section V.



Borden, FIG. 1.

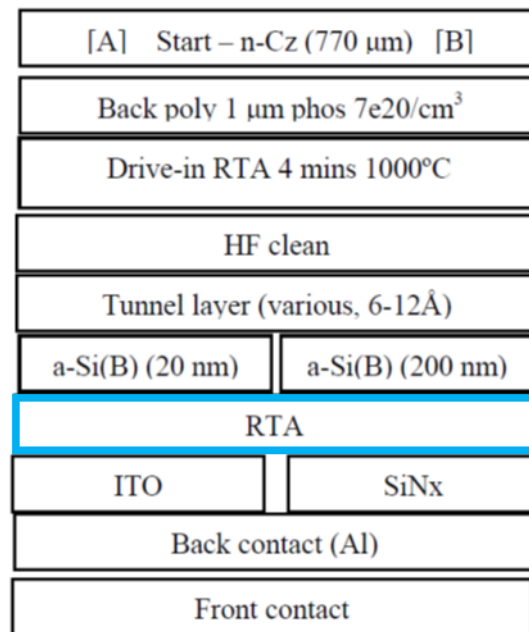
203. Second, a POSITA would understand that a doped polysilicon layer is passivating. Borden discloses that “[t]hin tunnel dielectrics...[w]hen combined with heavily doped polysilicon they can form an ideal step junction with interface passivation, enabling low dark currents.” Borden, 1149. Borden discloses that structures using polysilicon emitters (referred as “PEs” or “p-PE” in Borden) in solar cells were known since the ‘80s. Borden discloses a study “[t]o characterize the passivation performance of the PE structure” and reports that “[t]he passivation is a function of the poly thickness” and as depicted in Figure 6 of Borden the use of a thin doped polysilicon as PE can maximize minority carrier lifetime. *See* Borden, 1152 (“A

p-PE/c-Si(n) structure to minimize J_0 and maximize lifetime”). As discussed in 1[b], under the ’074 patent’s definition, passivation refers to suppressing the recombination of majority and minority carriers. *See* ’074 patent, 3:50-52. The reduction in such recombination can be directly reflected in an increase in V_{oc} (open-circuit voltage), as fewer recombined carriers mean more carriers are available to build up the potential difference at the junction as explained in Section V. Borden discloses that the poly layer can lead to improvement in V_{oc} . Borden, 1151 (“use of thinner poly provides a significant improvement in V_{oc} .”) Therefore, a POSITA would understand that the poly layer can provide passivation.

- e) **Limitation 1[d]: “providing thermal treatment at a temperature of above 500°C. or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer; and,”**

204. Borden teaches or suggests this limitation.

205. Borden discloses that the doped polysilicon layer is initially amorphous silicon (a-Si) and is crystallized through thermal treatment, specifically through rapid thermal annealing (RTA) at 1000°C. Borden, 1150 (“Amorphous silicon was then deposited and **crystallized** with a 30 second **RTA at 1000°C**”). *See also* Borden, FIGs. 3-4.

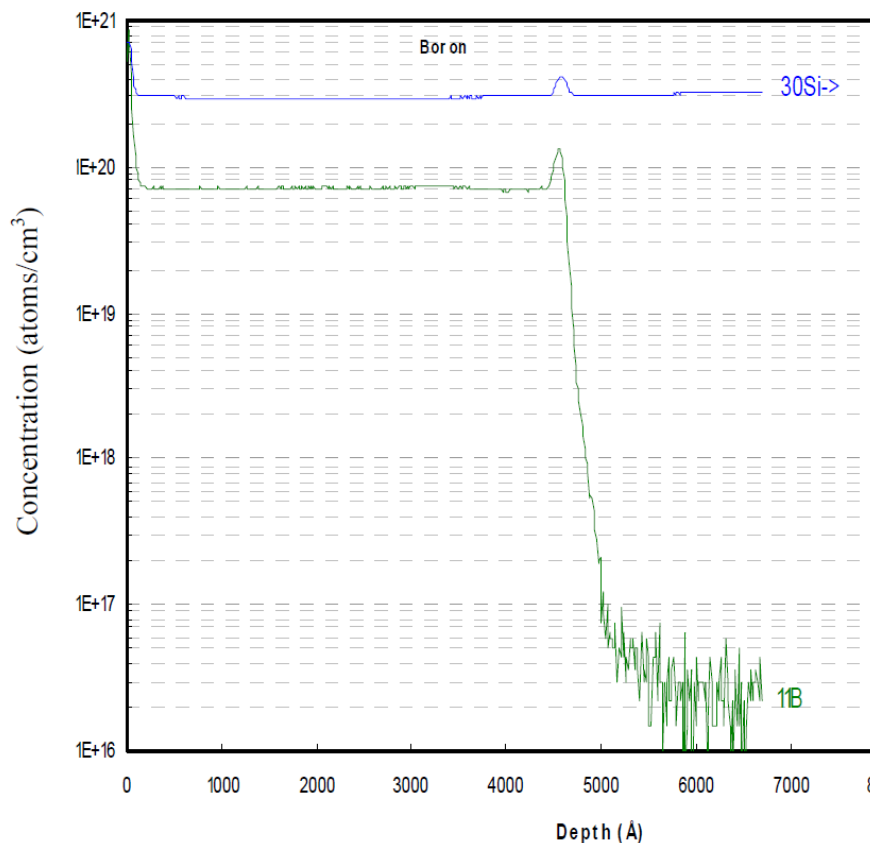


Borden, FIG. 3 (annotated).

206. A POSITA would understand that the thermal treatment facilitates diffusion of the dopant from the crystallized poly layer (*the at least one conductive and passivating layer*) through the tunnel dielectric (*the at least one interface passivation layer*). Specifically, a POSITA would understand that heating the poly layer at **1000°C** increases the atomic motion of the dopant atoms (i.e., boron), allowing the dopant atoms from the doped poly layer to diffuse through the tunnel dielectric into the n-type silicon substrate.

207. In fact, as stated above, Borden discloses using boron-doped amorphous silicon, which, after deposition, is crystallized with a Rapid Thermal Anneal at 1000°C . Borden also discloses that the thermal treatment causes boron (i.e., the dopant) to diffuse into the substrate. This is evident in the SIMS profile of a test structure depicted

in Figure 4; according to this figure the boron doped polysilicon layer is about 450 nm thick as at the thin silicon oxide. The SIMS reveals some boron segregation (resulting in an increased concentration at the interface with the substrate). This SIMS profile also reveals that the boron diffusion continues as evident by the notable concentrations of boron in the substrate (e.g., $>1 \times 10^{16}$ atoms/cm⁻³), thus demonstrating that the boron dopant atoms diffuse through the tunnel dielectric into the substrate (e.g., >4500 Å). Even though this SIMS profile is depicted for a test structure, a POSITA would understand that the dopant atoms would diffuse from the doped polysilicon layer (the *conductive and passivating layer*) through the grown silicon oxide layer (the *interface passivating layer*) in the solar cell structure depicted in Figure 2.



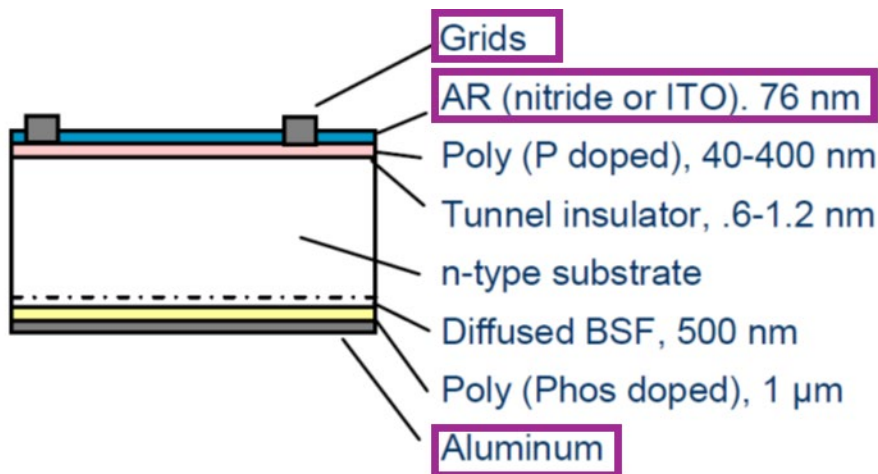
Borden, FIG. 4.

- f) **Limitation 1[e]: “providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof”**

208. Borden teaches or suggests this limitation.

209. Borden discloses the formation of front-side metallization as grids that directly contact the front-side boron doped polysilicon layer, the *conductive and passivating layer*, and back-side aluminum electrodes that directly contact the back-side doped phosphorus polysilicon layer. Borden, FIGs. 2-3. Borden’s “Grids” or

“Front Contact” as depicted in these two figures is the *providing metallization as electrodes*.



Borden, FIG. 2 (annotated).

210. It was commonly known in photovoltaic technology that front-side grids in solar cells are typically formed through metallization (e.g., using silver pastes), while the aluminum back electrode discloses the metallization limitation as it is itself a metallic conductor.

211. Borden further discloses that the processing, i.e., “Front contact,” that results in the metallization, i.e., the grid electrodes depicted in Figure 2, is taking place after the RTA (“rapid thermal annealing”), which is the *thermal treatment* step as evident by the Borden’s “process flow given in figure 3.” Borden, 1149-50, FIG. 3.

[A] Start – n-Cz (770 μm) [B]	
Back poly 1 μm phos 7e20/cm ³	
Drive-in RTA 4 mins 1000°C	
HF clean	
Tunnel layer (various, 6-12Å)	
a-Si(B) (20 nm)	a-Si(B) (200 nm)
RTA	
ITO	SiNx
Back contact (Al)	
Front contact	

Borden, FIG. 3 (annotated).

- g) **Limitation 1[f]: “wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.”**

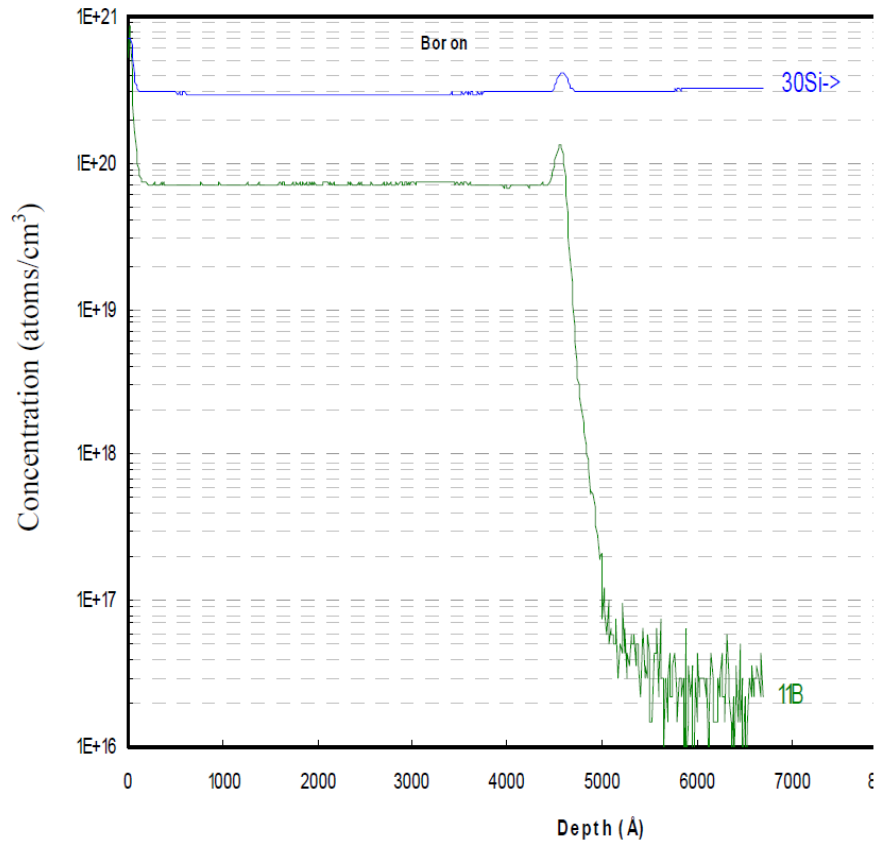
212. Borden teaches or suggests this limitation.

213. The '074 patent does not define the term *shortened charge carrier flow paths*. To the extent that First Solar claims that the dopant diffused from the conductive and passivating layer through the interface passivation layer provides shortened charge flow paths, Borden has provided teachings under this interpretation.

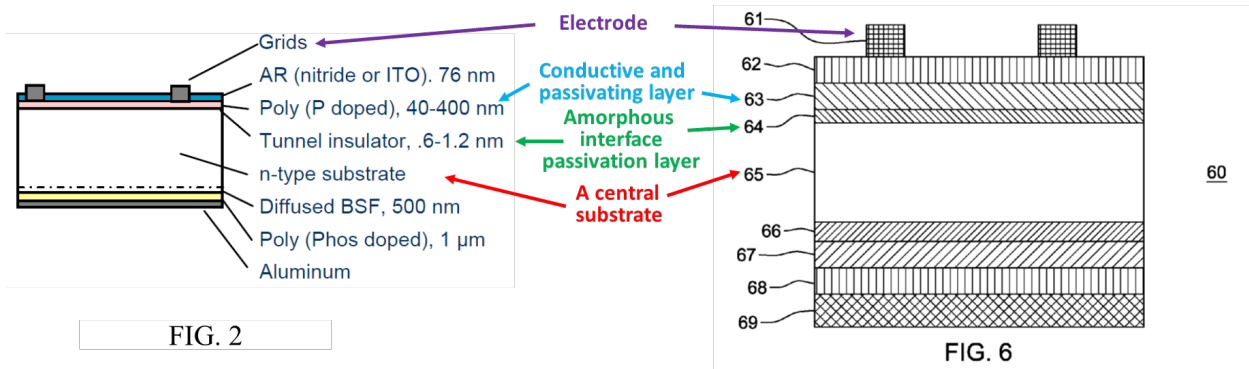
214. Specifically, Borden discloses that the thermal treatment causes dopants to diffuse through the tunnel dielectric layer and ultimately into the substrate, which is

evident in Figure 4, as the SIMS profile reveals that the dopant boron's diffusion persists and maintains notable concentrations (e.g., $>1 \times 10^{16}$ atoms/cm³) penetrating through the tunnel dielectrics into the substrate (e.g., >4500 Å). A POSITA would understand that under the above interpretation, this process provides shortened charge flow paths between the substrate and the electrode on the doped polysilicon layer.

215. As shown below, I compare the annotated FIG. 2 of Borden with Figure 6 of the '074 patent. The comparison shows that Borden discloses the same structure as the one in claim 1 of the '074 patent. Moreover, as per my analysis of the above limitations, Borden discloses the same materials (shown below in bold) as the ones stated as examples in the '074 patent. In regard to the structure depicted in Figure 6 of the '074 patent, “[e]xemplary layers of cell 60 include...61: Front **metal electrode** [Grids in Borden]. 62: Transparent and conductive film...like **indium tin oxide** [ITO in Borden]...63: Electrically passivating and conductive film...**n-type amorphous or polycrystalline silicon** [Poly (P doped) in Borden]...64: Electrically passivating interface layer...**silicon oxide** [Tunnel insulator in Borden].” ’074 patent, 5:29-61. As per my analysis above, Borden discloses that the dopant diffused through *the interface passivation layer* (“tunnel insulator”) provides a shortened charge carrier flow path between the substrate and the electrodes through *the conductive and passivating layer* (“Poly (P doped)”) and *the interface passivation layer*.



Borden, FIG. 4.

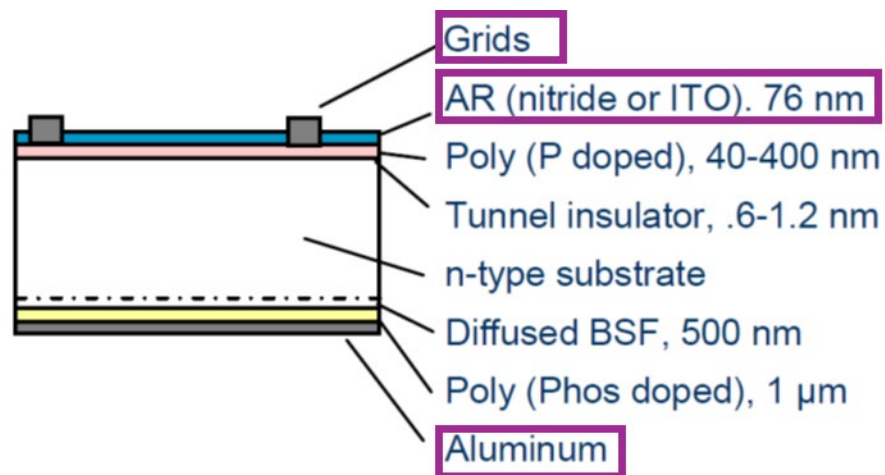


Borden, FIG. 2 (annotated, left), '074 patent, FIG. 6 (annotated, right).

216. To the extent that First Solar claims that the shortened paths occur when “[charge carriers’] transport within the emitter is vertical instead of mainly lateral,”

which is achieved when using a “full area contact coverage” electrode that covers the emitter, *see e.g.*, '074 patent, 4:49-50, Borden has provided teachings under this interpretation.

217. Specifically, Borden discloses that the ITO front contact layer, serving as an electrode, covers nearly the entire area of the front-side doped polysilicon, while the aluminum back contact layer, also functioning as an electrode, fully covers the back-side doped polysilicon area. Borden, FIG. 2.



Borden, FIG. 2 (annotated).

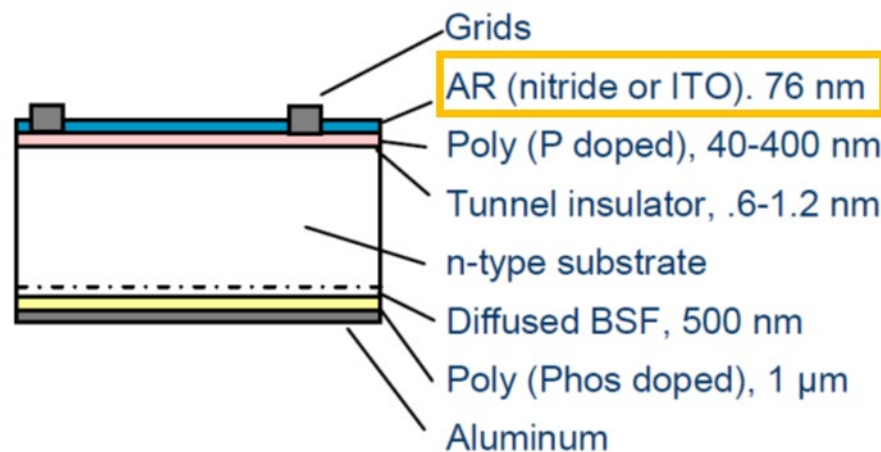
218. A POSITA would understand that this extensive electrode coverage over the doped polysilicon regions enables charge carriers to primarily follow vertical transport paths with minimal lateral movement, while dopant diffusion from the doped polysilicon layer into the substrate establishes continuous vertical current pathways extending from the electrodes through to the substrate. In other words, this

configuration inherently reduces unnecessary lateral current paths, thereby effectively shortening the charge carrier flow paths between the substrate and the electrodes.

2. Claim 2: “The method of claim 1, further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.”

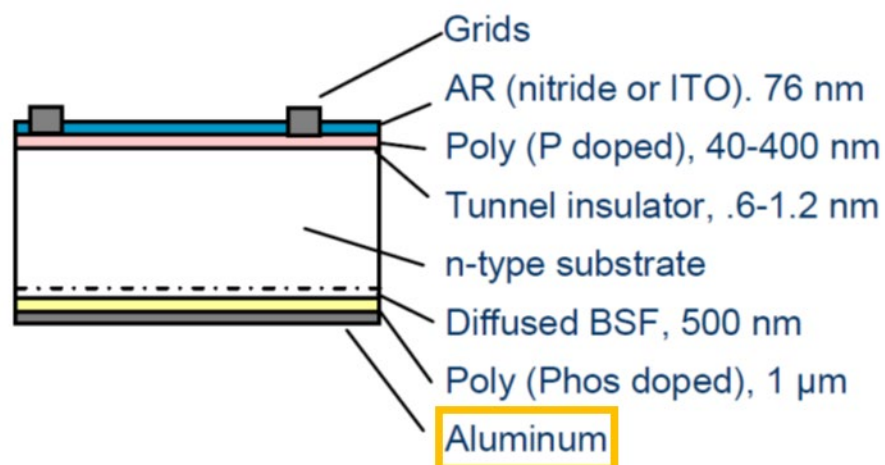
219. Borden teaches or suggests this limitation.

220. Borden discloses *forming a good internal mirror on a back of the solar cell*. Specifically, Borden discloses depositing at least two types of antireflective layer: an overlaid ITO and a Si_3N_4 AR coating. Borden, 1149 (“The first uses a thin p-type poly with an overlaid ITO as an anti-reflection (AR) coating and contacting layer. The second uses a thicker poly with a Si_3N_4 AR coating.”), *see also* Borden, FIGs. 2-3.



Borden, FIG. 2 (annotated).

221. Borden also discloses an aluminum layer, which is known to reflect light, thus forming a good internal mirror on the back of the solar cell. Borden, FIGs. 2-3.



Borden, FIG. 2 (annotated).

222. The '074 patent defines “a low reflective index layer for a good internal mirror on the back” as a layer with a “refractive index basically smaller than 3.0, smaller than 2.6, smaller than 2.0, smaller than 1.5.” '074 patent, 15:31-35.

223. A POSITA would understand that the aluminum layer on the back side as disclosed in Borden has a refractive index less than 2.0, which can redirect visible light back into the solar cell, thereby functioning as a good internal mirror. Smith, 398-99. As discussed in Section V, it was well known that aluminum has a high reflectance, greater than 90% for wavelengths greater than 900 nm or 0.9 μm. The '074 patent defines “a good internal mirror in the back” as a material that has a “high reflectivity for photons of more than 900 nm wavelength.” '074 patent, 7:51-53, 12:8-9, 18:25-26.

3. Claim 4: “The method of claim 1, wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.”

224. Borden teaches or suggests this limitation.

225. Borden discloses forming a tunnel dielectric layer on a substrate either by chemical oxidation or by Rapid Thermal Oxidation followed by deposition of amorphous silicon and subsequent crystallization at elevated temperatures (e.g., 1000°C). Borden, 1150 (“Three base oxide layers were used: chem-ox, which is a chemical oxide formed after the standard MOS clean, and 8 and 10Å thick rapid thermal oxides (RTO). Amorphous silicon was then deposited and crystallized with a 30 second RTA at 1000°C.”)

226. Borden also discloses that the area of the solar cells is 2x2 cm². Borden, 1150. A POSITA would understand that during the high-temperature annealing, due to the significantly different thermal expansion coefficients between the tunnel dielectric layer (i.e., silicon dioxide) and the adjacent silicon layers above and below, mechanical stresses are developing over the large solar cell area, causing the tunnel dielectric layer to develop perforations.

227. The thermal stability of a thin silicon oxide at the interface between a silicon substrate and a polycrystalline silicon emitter was a subject that had been well studied. Wolstenholme discloses that a chemical oxide (grown by the known RCA chemical clean) becomes discontinuous and holes are formed upon annealing at 950°C. Wolstenholme, Table 1. Wolstenholme also discloses that “[s]mall areas (C) of the polysilicon had been regrown through such holes to become single-crystal material with the same crystallographic orientation as the underlying silicon.” Wolstenholme,

226. Table 1 of Wolstenholme reports the “fraction of the interface regrown,” which a POSITA would understand as the fraction of the *perforations* formed at the interface by the thermal anneal.

TABLE 1. Summary of results.

Silicon slice surface treatment	Preanneal temperature (°C)	Interfacial oxide layer		Polysilicon			Transistor gain
		Geometry	Maximum thickness (Å)	Fraction of interface regrown	Grain size (Å)		
					Surface	Bulk	
RCA	900	continuous	~ 14	0	1200	400	1400
RCA	950	broken up	~ 19	0.3	1200	600	350
RCA	1000	broken up	~ 22	0.7	1200	1000	90
RCA	1100	balled up	~ 55	0.97	2000	1000	40
HF	None	broken up	~ 8	0.2	1200	400	240
HF	1000	balled up	~ 50	0.95	1200	1000	50

Wolstenholme, Table 1.

228. Similarly to Wolstenholme, Bravman reports that after annealing at 1000°C, the chemical oxide layer itself became discontinuous over ~5% of the silicon surface area. Bravman, 2780. (“The second change attending the 1000°C anneal was an alteration of the chemical oxide layer itself, which became discontinuous over ~5% of the silicon surface area. In these regions, the polysilicon made direct contact with and became epitaxially oriented to the single-crystal substrate. As seen in Figure 3, however, these regions of epitaxial regrowth were quite small. Typically, they were 30 to 100 Å in width, and protruded 20 to 30 Å above the interface.”)

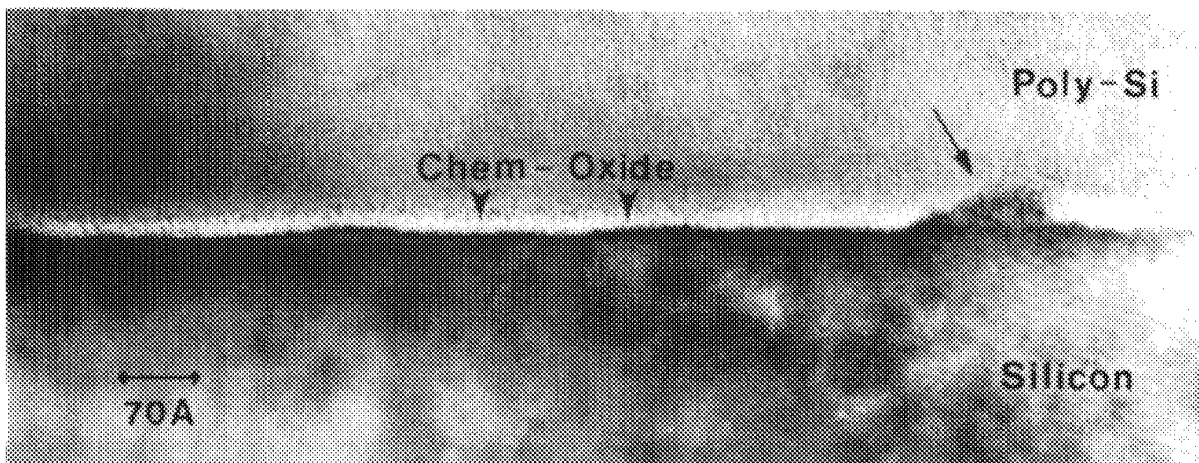


FIG. 3. Chemical-oxide interface following high-temperature annealing, showing a small region of polysilicon epitaxial realignment (arrowed) that formed at an oxide discontinuity.

Bravman, FIG. 3.

229. Borden teaches that thin oxides offer an “advantage” as thin oxides offer higher carrier lifetimes while in contrast thick oxides “causes a strong series resistance problem.” Borden, 1150 (“The advantage of the thinner base oxide is less clear... This shows that high tunnel layer thickness causes a strong series resistance problem.”), *see also* Borden, FIG. 6. Borden is also teaching a high temperature thermal treatment, i.e., 1000°C, for the crystallization of the deposited amorphous silicon. Consequently, a POSITA would understand that due to the thermal instability of thin oxides, perforations are formed in Borden’s thin tunnel oxide, since it was well known that such perforations are formed when the anneal temperature exceeds 900°C.

4. Claim 5: “The method of claim 1,”

230. Borden teaches or suggests this limitation.

231. See discussion of claim 1.

a) Limitation 5[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and”

232. Borden teaches or suggests this limitation, or renders this limitation obvious.

233. Borden discloses depositing amorphous silicon on the tunnel dielectrics layer. Borden, 1149-50. As discussed in Section VIII.A.3.a, Borden also discloses that the amorphous silicon was deposited using standard “IC equipment” that “runs 300 mm wafers.” Borden, 1149. A POSITA would understand that the IC equipment that can deposit an amorphous silicon containing compound on 300 mm wafers are chemical vapor deposition (CVD) equipment (either of the Plasma Enhanced CVD (PECVD) or the Low Pressure CVD type) and both CVD equipment utilize decomposition of the silane (SiH_4) compound. A POSITA would understand that depending on the type of CVD equipment used and the type of other gases used the amorphous silicon containing compound would include other elements in addition to silicon, e.g. oxygen (O_2), hydrogen (H_2).

234. Moreover, Borden specifically discloses that the amorphous silicon layer, which is later crystallized, is “in-situ doped p-type”—i.e., doped with boron, a conductive dopant. Borden, 1150.

235. According to Borden's disclosures, a POSITA would understand that Borden is disclosing the deposition of an amorphous silicon-containing compound as the conductive and passivating layer.

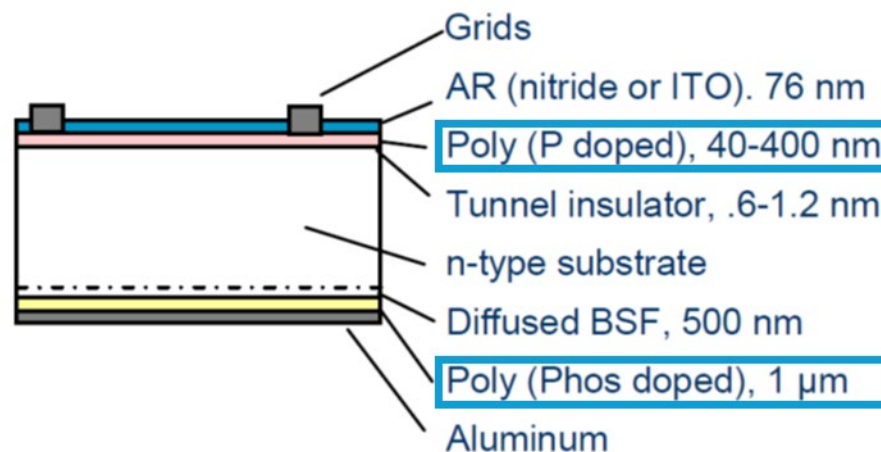
b) Limitation 5[b]: “wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.”

236. Borden teaches or suggests this limitation.

237. Borden discloses that on top of the thin silicon oxide layer (the *interface passivation layer*) “[a]morphous silicon was then deposited and crystallized with a 30 second RTA at 1000°C.” Borden, 1150. It was well known that when an amorphous layer is not in direct contact with a crystalline substrate, its crystallization occurs by random nucleation and growth, which results in a polycrystalline silicon layer. *See e.g.*, Hatalis, 2261 (“the crystallization of amorphous silicon does not result in grains with a columnar structure. After annealing, amorphous silicon deposited by CVD or by evaporation becomes polycrystalline with a needlelike or dendritic structure”); *see also* Hatalis, 2263 (“most of the grains crystallize individually and are surrounded by amorphous silicon. Occasionally, nucleation of new grains occurs at the grain boundaries of existing ones.”)

238. Borden also refers to the crystallized form of amorphous silicon deposited on the tunnel dielectric layer as polycrystalline silicon (also referred to as “polysilicon” or “poly”). *See* Borden, 1149 (“The standard back side enables understanding of the

physics of the polysilicon emitter on the front. Two variations are being examined. The first uses a thin p-type poly with an overlaid ITO as both an anti-reflective (AR) coating and a contacting layer. The second uses a thicker poly with a Si_3N_4 AR coating. Lithography is used to define contacts”), *see also* Borden, 1150, FIGs. 1-3.



Borden, FIG. 2 (annotated)

5. Claim 6: “The method of claim 1,”

239. Borden teaches or suggests this limitation.

240. See discussion of claim 1.

a) Limitation 6[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and”

241. Borden teaches or suggests this limitation or renders this limitation obvious.

242. See discussion of limitation 5[a].

b) Limitation 6[b]: “wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer and increases the optical transmissivity.”

243. Borden teaches or suggests this limitation, rendering it obvious.

244. As discussed in Section VIII.B.1.e, Borden discloses that the doped polysilicon layer, which serves as the polysilicon emitter, i.e., the Poly (P doped) layer in Figure 2 of Borden, is initially deposited as amorphous silicon and then is crystallized through a thermal treatment. *See* Borden, 1150 (“Amorphous silicon was then deposited and crystallized with a 30 second RTA at 1000°C”). Borden discloses that “[t]he polysilicon emitter has benefits over amorphous silicon in **reduced absorption**”. *See* Borden, 1149. A POSITA would understand that Borden refers to “reduced absorption” of light. Borden is also teaching “the need for thinner poly layers to achieve high efficiency, or, alternately, improvements in the optical properties of the poly” because as it is shown in Figure 9 of Borden “[t]he thick poly affects blue response” as “the absorption in it becomes quite severe.” Borden, 1151, FIG. 9. It was well known that when the amorphous silicon layer 13 crystallizes and transforms into polycrystalline silicon, its optical transmissivity increases as the light absorption coefficient of crystalline silicon is lower than that of amorphous silicon. For example, Figure 7.2 of Fuhs depicts that for the photons with energy of about 1.8 eV or higher, i.e., for photons corresponding to entire visible spectrum of the light (i.e. from violet

to red), the absorption coefficient of amorphous silicon is higher than that of crystalline silicon. Fuhs, 128, FIG. 7.2. *See also* Markvart, 107, FIG. 7.

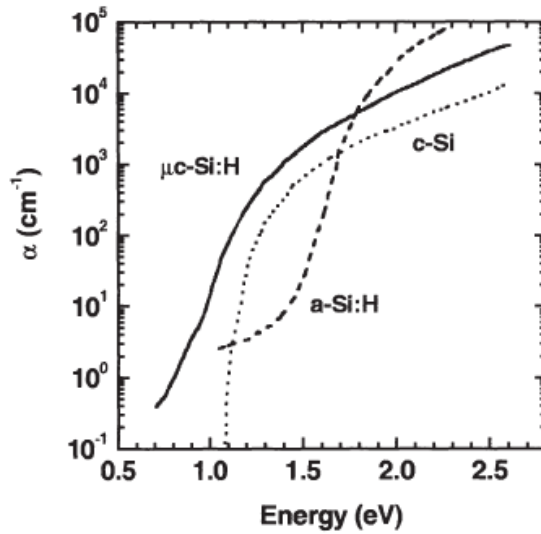
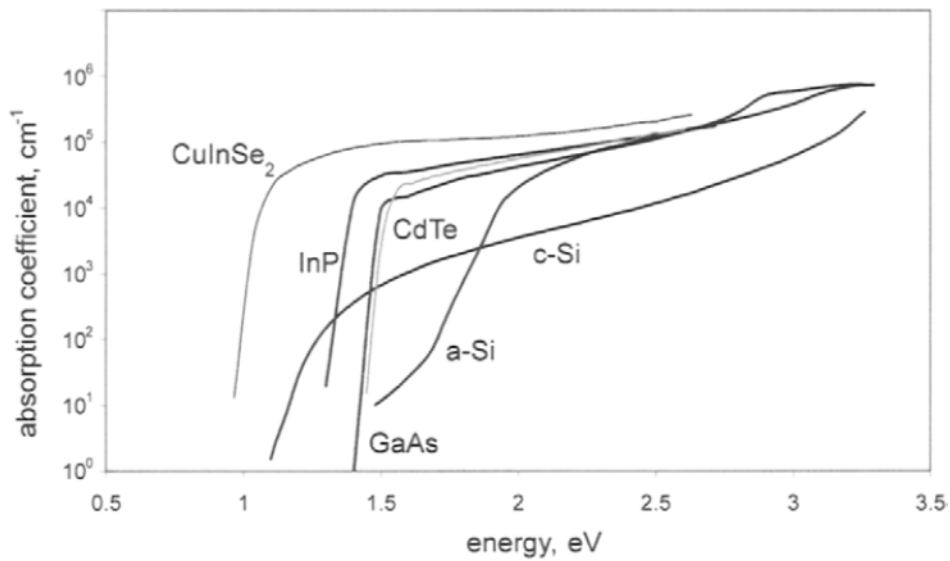


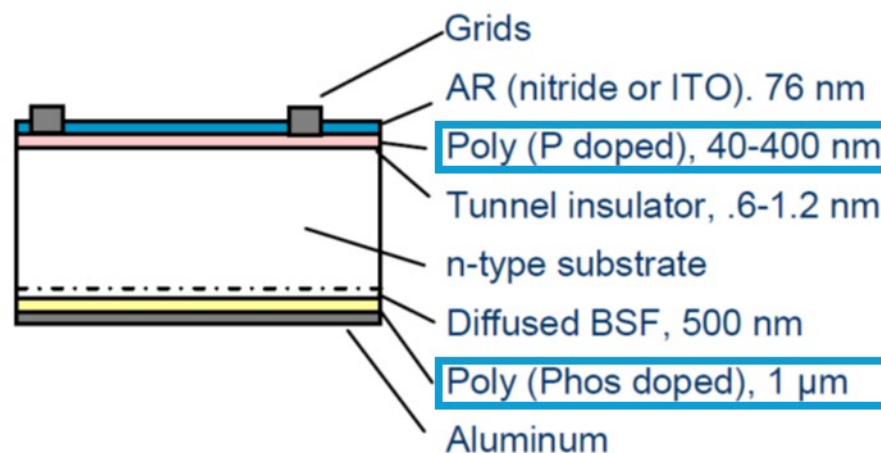
Fig. 7.2. Absorption edges of a-Si:H, monocrystalline Si and $\mu\text{c-Si:H}$

Fuhs, FIG. 7.2.



Markvart, FIG. 7

245. Since less light is absorbed by the crystallized polysilicon layer, i.e., Poly (P doped), its optical transmissivity is higher after the thermal treatment compared to the optical transmissivity of the initially deposited amorphous silicon. *See e.g., Shah, 696* (“Amorphous silicon has, in the visible range of the spectrum, a higher optical absorption coefficient than crystalline silicon and thus, can have thicknesses much less than 1 μm .”)



Borden, FIG. 2 (annotated).

6. Claim 7: “The method of claim 1,”

246. Borden teaches or suggests this limitation.

247. See discussion of claim 1.

a) Limitation 7[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and”

248. Borden teaches or suggests this limitation.

249. See discussion of limitation 5[a].

b) Limitation 7[b]: “wherein the thermal treatment activates doping atoms in the compound.”

250. Borden teaches or suggests this limitation.

251. As I explained in 1[c], Borden discloses that the conductive and passivating layer is deposited as amorphous silicon, which is doped p-type with a boron dopant. Borden describes this doped amorphous silicon layer as “a-Si(B)” in Figure 3. Borden discloses that after depositing the boron-doped amorphous silicon, a rapid thermal annealing (RTA) step is performed at 1000°C, which crystallizes the doped amorphous silicon. Borden, 1150. Borden refers to the crystallized layer as “Poly (P doped)” in Figure 2. Borden also refers to the device structures formed after the thermal anneal as having “hyper-abrupt junctions.” Borden, 1149. Borden, referring to a **boron-doped polysilicon** test structure, discloses that “Figure 4 shows the boron SIMS profile for a junction test sample...Note that a sharp junction profile is obtained.” Borden, 1150. Moreover, Borden discloses in Figure 8 the current-voltage I(V) characteristics of seven completed solar cells having the structure depicted in Figure 2.

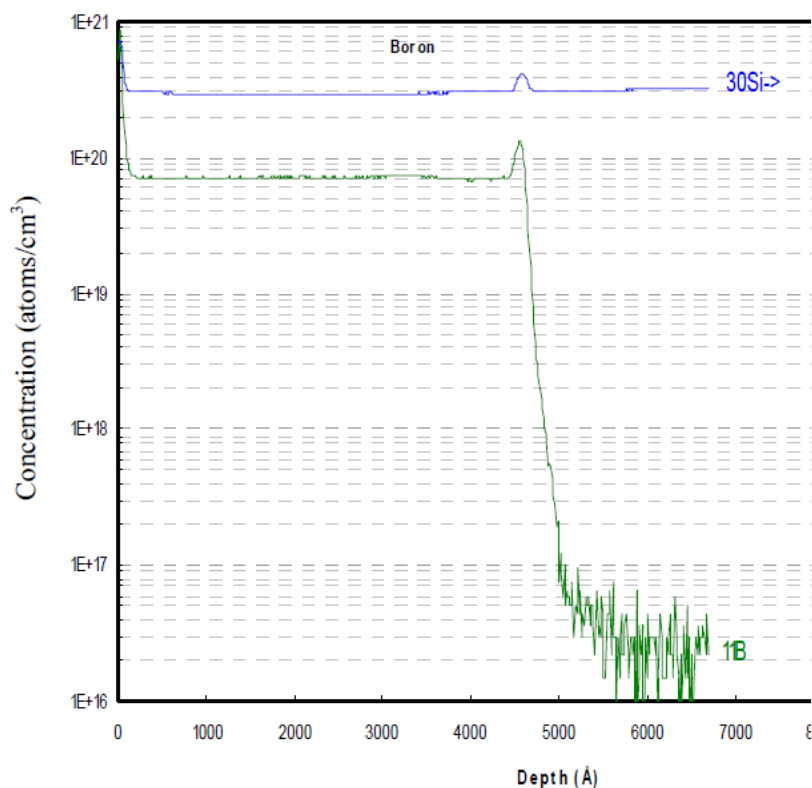


Figure 4: SIMS boron and reference silicon profile for a boron-doped polysilicon test structure.

Borden, FIG. 4.

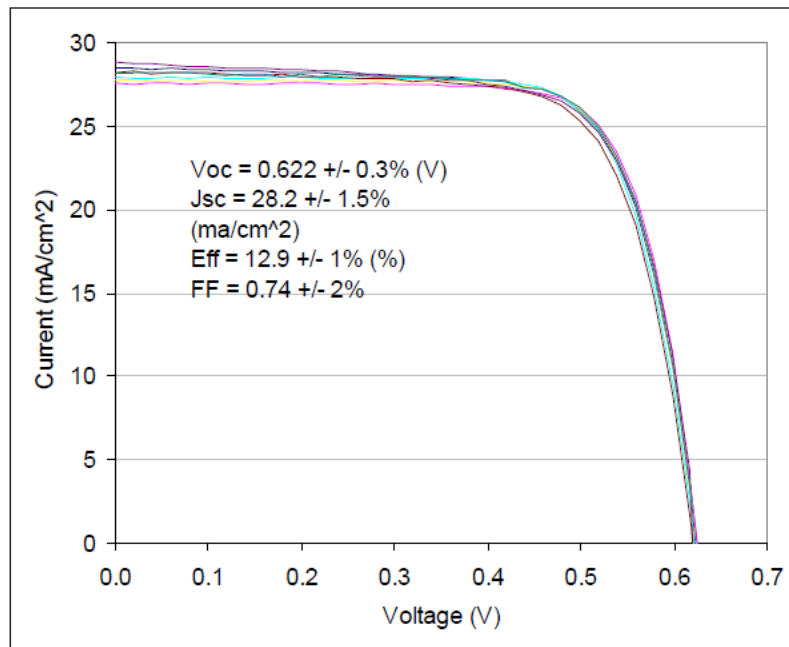


Figure 8: IV curves for seven 2x2 cm isolated PE cells in a 12.5x12.5 cm² area with 400 nm p-type poly on n-Si.

Borden, FIG. 8.

252. According to Borden's disclosures and teachings, a POSITA would understand that Borden's thermal treatment activates the dopant atoms, i.e., boron, for at least the following reasons. First, Borden's disclosed rapid thermal treatment at 1000°C, is a typical process used in IC processing for dopant activation. Borden discloses that "[t]he objective of this work is to use IC processing to understand the process requirements for a polysilicon emitter. This enables the use of well-characterized and controlled processes to determine which processes are best and to establish the process window." Borden, 1149. Second, Borden's disclosed boron profile in Figure 4 confirms, as discussed in more detail in 1[d], that the thermal

treatment causes boron to diffuse from the boron-doped polysilicon layer through the silicon oxide layer and thus forms a pn junction with “a sharp junction profile.” Borden, 1150. It was well known in the art that thermal treatments that result in dopant diffusion also activate the dopants. *See, e.g.,* Rana, 6 (“The end result after application of the heat...will activate and cause the dopant atoms in the...heavily doped discrete regions 71 to diffuse into the substrate 36 and the underlying layer a desired distance.”) Finally, Borden discloses experimental IV characteristics that demonstrate the typical IV characteristics of illuminated (“measured 1-sun IV curves for seven cells”) pn junctions. A POSITA would understand that since the substrate is n-type, the p-sides of these pn junctions were formed by the activation of the p-type dopant atoms, i.e., boron, caused by the thermal treatment.

7. Claim 8: “The method of claim 1,”

253. Borden teaches or suggests this limitation.

254. See discussion of claim 1.

a) Limitation 8[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound and”

255. Borden teaches or suggests this limitation.

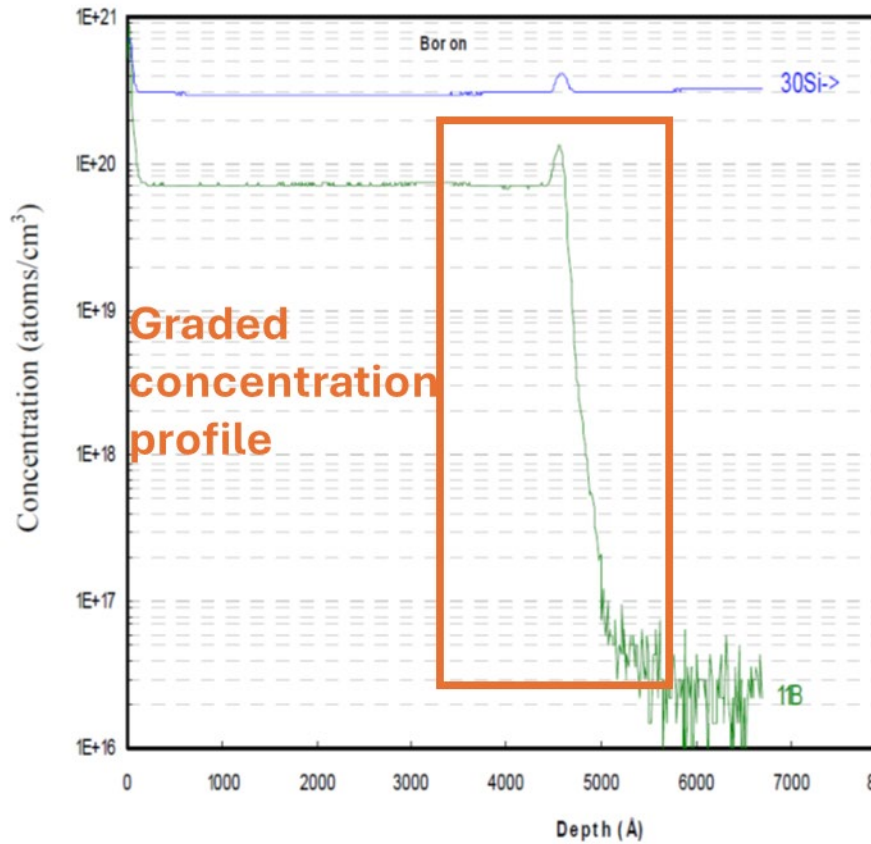
256. See discussion of limitation 5[a].

b) Limitation 8[b]: “wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.”

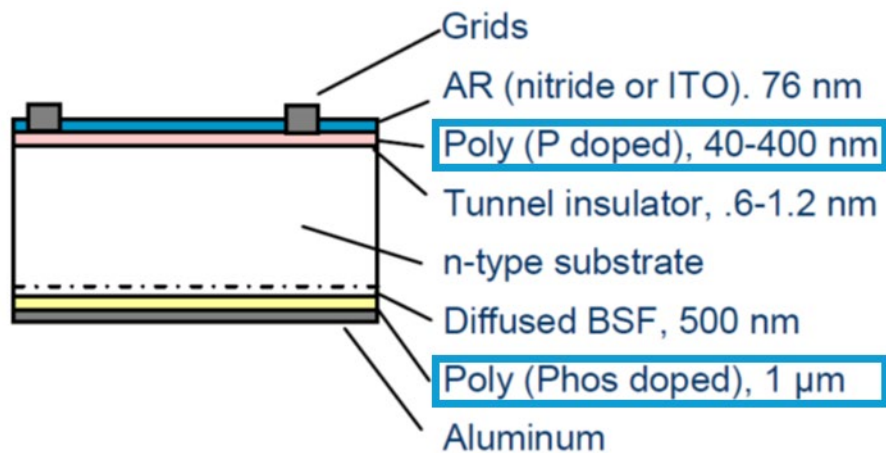
257. Borden teaches or suggests this limitation.

258. Borden teaches or suggests that the thermal treatment facilitates the diffusion of dopants (i.e., boron) from the amorphous silicon layer (which becomes the p-type doped polysilicon layer after crystallization) into the substrate. *See* Section VIII.B.1.e. Borden discloses that the diffusion of dopants into the substrate creates a graded concentration profile. *See* Borden, FIG. 4. A POSITA would understand that this graded boron dopant concentration profile establishes the p-side of a junction while the n-type doped substrate becomes the n-side of a p-n junction hence formed. Borden discloses schematically the device structure of the p-n junction in Figure 2, where the p-side (“Poly P doped,” i.e., p-type doped with boron) and the n-side (n-type substrate) of the p-n junction are clearly labelled. Borden also discloses in Figure 3 the physical structure of the p-n junction as observed with TEM (Transmission Electron Microscopy) that is formed with the “p-Si(poly),” i.e., the p-type doped polysilicon, and the “n-Si(c),” i.e., n-type doped crystalline silicon substrate, clearly doped. As discussed above and depicted in Figure 2, the boron dopant diffuses from the “p-Si(poly)” into the “n-Si(c)” substrate, thus forming the p-n junction. Moreover, Borden discloses actual electrical IV, i.e., current vs voltage, curves of seven completed cells,

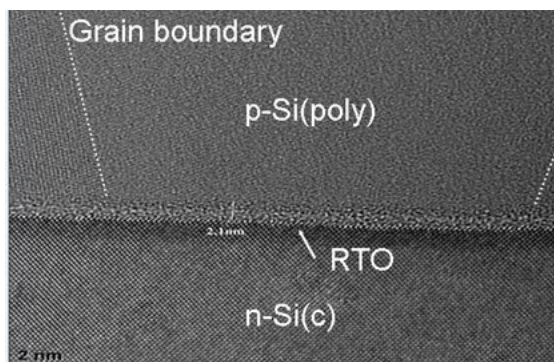
i.e., solar cells, that each comprises “400 nm p-type poly on n-Si.” A POSITA would understand that the depicted IV curves are typical curves of illuminated p-n junctions.



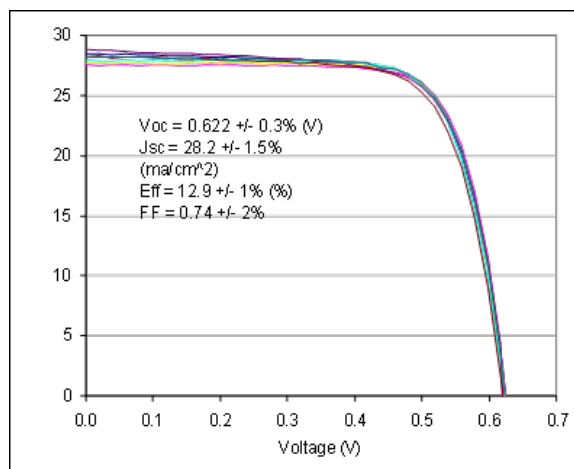
Borden, FIG. 4 (annotated).



Borden, FIG. 2 (annotated).



Borden, FIG. 3 (TEM of the interface, with poly on top and crystal silicon underneath).



Borden, FIG. 8 (IV curves for seven 2x2 cm isolated PE cells in a 12.5x12.5 cm² area with 400 nm p-type poly on n-Si).

C. Ground 3: Claims 3-4 are Rendered Obvious by Borden and Kwark, Gan or Swanson

1. Motivation to Combine Borden and Kwark

259. A POSITA would be motivated to combine Kwark with Borden. Kwark, like Borden, relates to forming an improved p-n junction where one side of it consists

of a crystalline silicon wafer, the other side consists of a deposited amorphous silicon containing compound, and at the interface between these two materials, a silicon oxide layer serves as an interface passivation layer.

260. Borden teaches a two-step process, whereby first a thin oxide (or tunnel dielectric) layer is grown on the crystalline silicon wafer and then an amorphous silicon containing compound is deposited on the tunnel dielectric layer. Afterwards, Borden teaches a thermal treatment step. Kwark discloses a single step whereby an amorphous silicon containing compound is deposited that consists of amorphous silicon oxide (SiO_x , where $x < 2$), and clusters of silicon surrounded by amorphous transition layers of silicon and oxygen. Kwark, 742. In particular, Kwark discloses that this material is deposited by Chemical Vapor Deposition (CVD) specifically by Atmospheric Pressure CVD (APCVD) using a mixture of silane (SiH_4) and nitrous oxide (N_2O) and is known as SIPOS. Kwark, 742 (“Deliberate introduction of controlled amounts of an oxygen bearing species...into the deposition ambient normally used for chemical vapor deposition of polysilicon produces SIPOS, a class of silicon oxides which exhibits a wide range of physical properties”). Like Borden, Kwark also discloses a thermal treatment step in the temperature range of 800°C to 1000°C . Kwark, FIGs. 4-6.

261. Kwark discloses that the thermal treatment induces a phase separation within the bulk of the SIPOS layer and a growth of silicon oxide layer at the interface between SIPOS and the silicon wafer. Kwark, 742. In particular, Kwark discloses that

the thermal treatment activates the in-situ dopant while simultaneously forming an interfacial oxide layer. Kwark, 742 (“the CVD deposited SIPOS films used in these devices require a high temperature anneal in order to activate the dopant.”) *See also* Kwark, 743 (“This insensitivity to bulk film properties implies that...the formation of an interfacial oxide layer as a result of the annealing process.”) Kwark teaches that “the distinguishing feature of SIPOS may be its built-in source of oxygen which aids in the formation and/or maintenance of this interfacial [oxide] layer.” Kwark, 743.

262. Kwark teaches that a structure formed through this process, featuring an interfacial oxide layer whose thickness is tunable by introducing a chemox layer, serves as a more robust diffusion barrier compared to structures without such an interfacial oxide layer formation and thereby suppresses bulk recombination. Kwark, 743 (“the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step. This would act as a more robust diffusion barrier and would limit the extent of outdiffusion of dopants from the SIPOS thus reducing bulk recombination in the monocrystalline emitter region.”)

263. A POSITA would understand that the reduction in bulk recombination achieved through Kwark’s process improves passivation in solar cells. By replacing the polysilicon deposition step in the Borden process with Kwark’s process, a superior balance is achieved between passivation efficacy and suppression of dopant over diffusion.

264. Borden discloses that the highest lifetimes are achieved by a thermally grown oxide layer. Borden, FIG. 6. A POSITA would also understand that the two-step process disclosed by Borden (growth of the tunnel oxide followed by polysilicon deposition) could be reduced to a single step as disclosed by Kwark, thus reducing process complexity and fabrication cost. Specifically, a POSITA would understand that Kwark's process eliminates the need for the separate tunnel dielectric layer (i.e., the *interfacial passivation layer*) growth step as required in the Borden process. This is because the SIPOS layer (i.e., the *conductive and passivating layer*) and the interfacial passivation oxide (i.e., the *interface passivation layer*) are formed simultaneously during a single high-temperature annealing step. This integration delivers process simplification advantages.

265. In summary, Kwark discloses the formation of both an interfacial oxide layer and a SIPOS layer on a substrate. Kwark, 742. This layered structure bears similarity to Borden's solar cell design, but Kwark's annealing process simultaneously induces phase separation within the SIPOS layer—transforming it into distinct microcrystalline silicon regions embedded within an oxygen-enriched amorphous matrix—while concurrently growing the critical interfacial oxide layer in a single processing step, as clearly illustrated in the structural evolution shown in Kwark's FIG. 3. As discussed above, a POSITA would be motivated to modify Borden's two-step process to achieve the advantages of reduced process complexity, reduced processing

steps, higher yield and reduced cost while achieving the performance advantages disclosed by Kwark. A POSITA would understand that such a modification would entail eliminating Borden's rapid thermal oxidation step and performing a simple change in Borden's process for depositing the amorphous silicon containing compound. The CVD process was very common process to deposit both the amorphous silicon layer of Borden and the SIPOS layer disclosed by Kwark. As discussed in Section V, it was known that the use of a SIPOS layer would result in p-n junctions that have very low saturation current (J_0) which results in a solar cell's improved performance. Verlinden, 451. Thus, a POSITA would have combined the teachings of Borden and Kwark with a reasonable expectation of success, in order to achieve the aforementioned benefits.

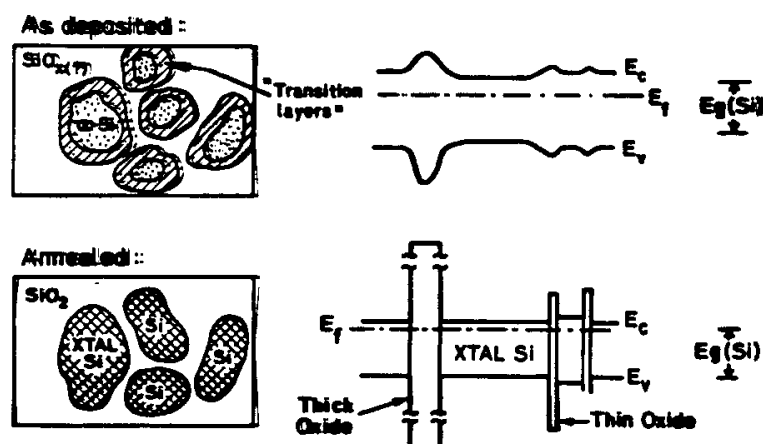


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the "oxide-like" regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Kwark, FIG. 3.

2. Motivation to Combine Borden and Gan

266. A POSITA would be motivated to combine Gan with Borden. Gan, like Borden, relates to forming an improved p-n junction where one side of it consists of a crystalline silicon wafer, the other side consists of a polysilicon emitter, and at the interface between these two materials, a silicon oxide layer serves as an interface passivation layer. Both Gan and Borden disclose the application of such improved p-n junctions to solar cells, and both disclose that for high-efficiency solar cells, the junctions must have a low saturation current J_0 . Borden, 1151-52 ("the path to a high efficiency PE cell structure is clear. The requirements include: A p-PE/c-Si(n)

structure to minimize J_0 "); Gan, 245 ("the cell performance can be improved if the diffused-emitter is replaced with the polysilicon emitter, of which the J_0 is less than 4.5×10^{-13} A/cm² and the ρ_c is low enough.") A POSITA would understand that a low J_0 is a function of the interfacial silicon oxide layer.

267. Borden discloses that a thermally grown oxide also yields higher open circuit voltage, "[h]igher values are found for the RTO dielectrics than the chem-ox, consistent with the results of figure 6, which suggests that the RTO provides improved interface passivation". Borden, 1150. Borden also discloses that a "high tunnel layer thickness causes a strong series resistance problem." Borden, 1151. Gan teaches that the "polysilicon-substrate contact resistance," i.e. ρ_c , is one of the components that contributes to the series resistance and that "[w]hen the interfacial oxide is intact, tunnelling is the only process available for the majority carriers to pass through interfacial oxide. This usually results in a high contact resistance because of low tunneling probability." Gan, 249. It was well known that a thin interfacial oxide between a crystalline silicon substrate and a deposited silicon layer is not thermally stable and breaks down during a high-temperature anneal. *See* Gan, 245 ("It was found that, between the polysilicon and the substrate, there always exists a very thin oxide (interfacial oxide), which can be as a by-product of the cleaning process or is grown intentionally. In either case, the oxide is not thermally stable, i.e., it tends to break up during high temperature anneals.") As Gan discloses, it was also well known that

“when the interfacial oxide loses its integrity in high temperature anneals, the ρ_c is low ($\sim 2 \times 10^{-7} \Omega\text{-cm}^2$) and the J_0 is high ($\sim 1 \times 10^{-12}$).” Gan, 245. Gan also discloses that it was known that for an intact interfacial oxide, “the ρ_c is high and the J_0 is low” and that “[t]ypically, $\rho_c > 1 \times 10^{-4} \Omega\text{-cm}^2$, and the corresponding $J_0 \sim 1 \times 10^{-14} \text{ A/cm}^2$ have been observed on the n-type polysilicon emitter.” Gan, 245.

268. Gan is teaching that by adjusting the processing conditions it will be possible to achieve both a low J_0 and a low ρ_c . Specifically, Gan is teaching “ ρ_c drops drastically when the oxide starts to breakup,” and that, “polysilicon emitters with low J_0 and ρ_c can be obtained with a very small fraction of interfacial oxide breakup. Typically, $\rho_c \sim 1 \times 10^{-5} \text{ A-cm}^2$ and $J_0 \leq 5 \times 10^{-14} \text{ A/cm}^2$ are obtained for both n- and p-type polysilicon emitters.” Gan, 249. A POSITA would understand that for optimum device performance, both a low J_0 and a low ρ_c are required.

269. Therefore, a POSITA would be motivated to combine Gan with Borden to achieve low values for both the saturation current J_0 and the contact resistance ρ_c . This way a POSITA will achieve Borden’s requirement to “minimize J_0 ”, *see* Borden, 1151-52 (“the path to a high efficiency PE cell structure is clear. The requirements include: A p-PE/c-Si(n) structure to minimize J_0 ”), while at the same time solving one of the Borden’s stated problems of high series resistance. A POSITA would understand that the integrity of Borden’s thin tunneling layer may not be high during a high-

temperature anneal, leading to excessive breakup and resulting in a high J_0 , thus creating a process that will not be very robust and reproducible. On the other hand, a POSITA would understand that while more robust as per Borden's teaching, a "high tunnel layer thickness causes a strong series resistance problem."

270. In summary, a POSITA would understand that by applying Gan's teachings of forming "a very small fraction of interfacial oxide breakup" into Borden's thermal interfacial oxide would result in a robust and reproducible process, which would also improve Borden's solar cell performance as a direct result of a low J_0 and a low ρ_c . Since Borden and Gan both disclose similar processing steps, a POSITA would understand that modifying Borden's processing steps for forming Gan's "very small fraction of interfacial oxide breakup" would entail simple experimentation on the growth of thermal oxide (a step disclosed by Borden) and the thermal anneal process (a step also disclosed by Borden). Moreover, as discussed in Section V, it was well known in the art to form break-up regions in the oxide in order to reduce the series resistance. Verlinden, 451 ("The growth of a thin (10 to 20 Å) interfacial layer of silicon dioxide is critical to obtain low emitter saturation current density with polysilicon. However, in order to achieve a low contact resistance, it is necessary to anneal the polysilicon emitter to break up the oxide layer on about 1% of the contact area. The trade-off between J_0 and a high contact resistance is highly dependent on the oxide thickness and the anneal (or breakup) step.") Thus, a POSITA would have

combined the teachings of Borden and Gan with a reasonable expectation of success in order to achieve the aforementioned benefits of a robust and reproducible process for achieving high-performance solar cells.

3. Motivation to Combine Borden and Swanson

271. A POSITA would be motivated to combine Swanson with Borden. Swanson, like Borden, relates to forming improved solar cells consisting of polysilicon emitters on crystalline silicon substrates and a thin silicon oxide layer in between, serving as an interface passivation layer. Both Swanson and Borden disclose that for high-efficiency solar cells, the junctions must have a low saturation current J_0 . Borden, 1151 (“the path to a high efficiency PE cell structure is clear. The requirements include: A p-PE/c-Si(n) structure to minimize J_0 ”; Swanson, 1:18-20 (“Two desirable characteristics in a polysilicon emitter or contact are low emitter saturation current (J_0) and low contact resistance.”) A POSITA would understand that a low J_0 is a function of the interfacial silicon oxide layer.

272. Borden discloses that a thermally grown oxide also yields higher open circuit voltage, “[h]igher values are found for the RTO dielectrics than the chem-ox, consistent with the results of figure 6, which suggests that the RTO provides improved interface passivation”. Borden also discloses that a “high tunnel layer thickness causes a strong series resistance problem.” As discussed in Section VIII.C.2, it was well known that a thin interfacial oxide between a crystalline silicon substrate and a

deposited silicon layer is not thermally stable and it breaks up during a high temperature anneal. Swanson also discloses that it was known in the art that when the interfacial oxide is intact, the ρ_c is high due to the series resistance, while J_0 is low due to improved interface passivation. Swanson, FIG. 8 (as shown in curve 32). However, as the oxide breaks up by a high temperature anneal, the contact resistance decreases, but the saturation current increases. Swanson, 1:18-21 (“Achieving a low contact resistance requires a high temperature annealing; however, high temperature annealing out diffuses dopant from the contact into the substrate, thereby reducing the integrity of the interfacial oxide and [increasing]³ J_0 .”

³ The original text is “reducing,” but a POSITA, based on the context and normal logic, would understand that “reducing” is a typo and the correct word should be “increasing.”

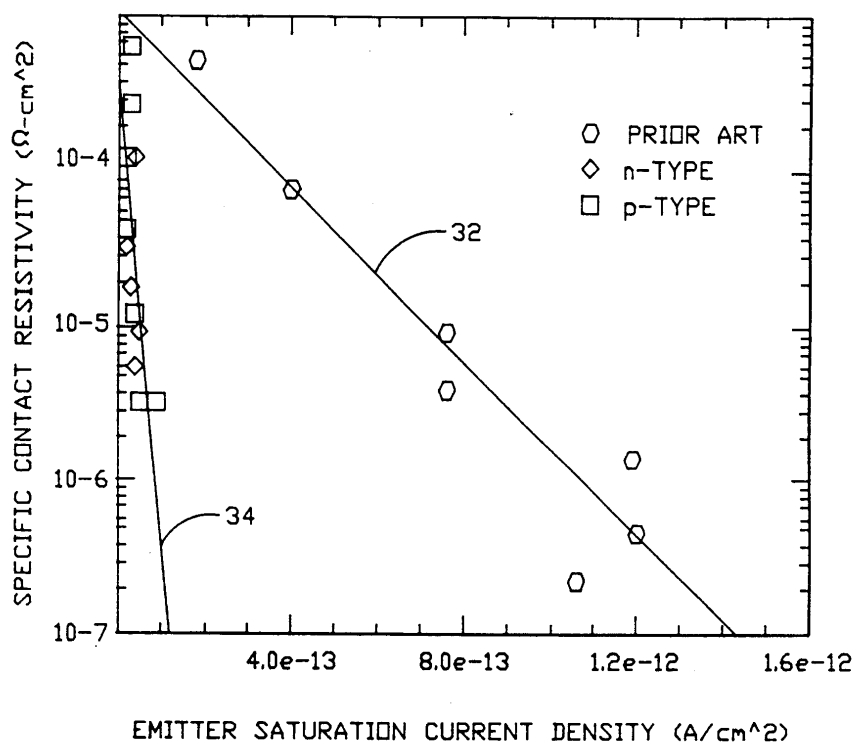


FIG.—8

Swanson, FIG. 8.

273. Swanson is teaching that by adjusting the processing conditions, it will be possible to achieve both a low J_0 and a low ρ_c . Specifically, Swanson teaches that “[a] misconception about the interfacial oxide of polysilicon emitters is that the contact resistance of polysilicon emitters is too high for device applications if the interfacial oxide is not broken completely.” Swanson, 1:32-35. Moreover, Swanson discloses that “[e]ither the anneal temperature or the annealing time can be used to control the extent of the interfacial oxide which is broken.” Swanson, 2:64-67, FIG. 5B; *see also* Swanson, 3:1-4 (“As shown in the enlarged view of FIG. 5B, the interfacial oxide is

broken partially and polysilicon contacts the substrate intimately in the broken areas”; here a POSITA would understand that the “broken areas” are depicted as element 20, since element 16 depicts the thin “thermally grown oxide 16” as per Swanson, 2:47-51.) Swanson teaches that “the contact resistance is reduced by the presence of the broken regions in the thin silicon oxide layer” Swanson, 3:29-31. *See also* Swanson, FIG. 8, where both a low J_0 and a low ρ_c are depicted as shown in curve 34. A POSITA would understand that for optimum device performance, both a low J_0 and a low ρ_c are required.

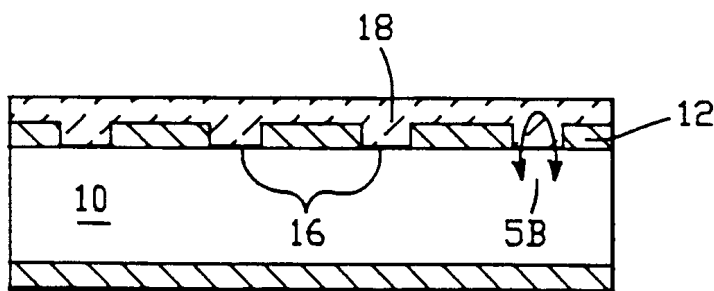


FIG.—5A

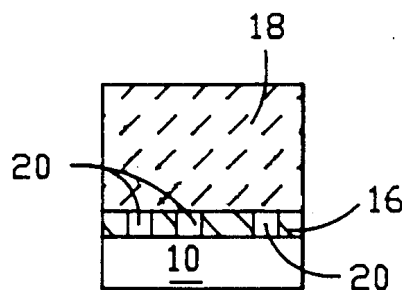


FIG.—5B

Swanson, FIGs. 5A, 5B.

274. Therefore, a POSITA would be motivated to combine Swanson with Borden to achieve low values for both the saturation current J_0 and the contact resistance ρ_c . This way a POSITA will achieve Borden’s requirement to “minimize J_0 ”, *see* Borden, 1151-52 (“the path to a high efficiency PE cell structure is clear. The

requirements include: A p-PE/c-Si(n) structure to minimize J_0 ”), while at the same time solving one of the Borden’s stated problems of “high series resistance.” A POSITA would understand that the integrity of Borden’s thin tunneling layer may not be high during a high temperature anneal, leading to excessive breakup and resulting in a high J_0 and thus to a process which will not be very robust and reproducible. On the other hand, a POSITA would also understand that while more robust, as per Borden’s teaching a “high tunnel layer thickness causes a strong series resistance problem.”

275. In summary, a POSITA would understand that applying Swanson’s teachings of forming “broken regions” into Borden’s thermal interfacial oxide would result in a robust and reproducible process, which would also improve Borden’s solar cell performance as a direct result of a low J_0 and a low ρ_c . Since Borden and Swanson both disclose similar processing steps, a POSITA would understand that modifying Borden’s processing steps, as per Swanson’s teaching, so that “the interfacial oxide is broken partially,” would entail simple experimentation. Specifically, this modification would entail adjusting the thickness of Borden’s thermal oxide and adjusting the thermal anneal process (a step also disclosed by Borden). As per Swanson’s teaching, “[either] the annealing temperature or the annealing time can be used to control the extent of the interfacial oxide which is broken.” Swanson, 3:29-31. Moreover, as discussed in Section V, it was well known in the art to form break-up regions in the oxide in order to reduce the series resistance. Verlinden, 451 (“The growth of a thin

(10 to 20 Å) interfacial layer of silicon dioxide is critical to obtain low emitter saturation current density with polysilicon. However, in order to achieve a low contact resistance, it is necessary to anneal the polysilicon emitter to break up the oxide layer on about 1% of the contact area. The trade-off between J_0 and a high contact resistance is highly dependent on the oxide thickness and the anneal (or breakup) step.”) Thus, a POSITA would have combined the teachings of Borden and Swanson with a reasonable expectation of success in order to achieve the aforementioned benefits of a robust and reproducible process for achieving high-performance solar cells.

4. Claim 3: “The method of claim 1,”

276. Borden teaches or suggests this limitation.

277. See discussion in Section VIII.C.1.

a) Limitation 3[a]: “wherein the depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer comprises depositing an amorphous silicon-containing compound over the substrate”

278. Borden in view of Kwark renders this claim element obvious. Borden discloses the deposition of an amorphous silicon layer on top of a tunnel oxide formed by chemical means or rapid thermal oxidation. Borden, 1149 (“The objective of this work is to use IC processing to understand the process requirements for a polysilicon emitter.”) A POSITA would understand that the deposition of an amorphous silicon layer in a typical IC process is typically formed by the thermal decomposition of a

silane (SiH_4) gas in a chemical vapor deposition reactor of either the Low-Pressure CVD (LPCVD) or the APCVD type. A POSITA in view of Kwark, as disclosed above, will be motivated to modify the deposition process disclosed by Borden as follows. After cleaning the silicon wafers, claimed substrates, will be loaded into the CVD reactor. Then during the actual deposition process two reactant gases will flow as disclosed by Kwark, silane (SiH_4) and nitrous oxide (N_2O). A POSITA would understand that the thermal decomposition of these two gasses, i.e. silane and nitrous oxide, as Kwark discloses, will result in the deposition of an amorphous silicon containing compound called SIPOS, and which is a material comprising of amorphous silicon oxide compound (SiO_x , $x < 2$) and clusters of amorphous silicon surrounded by a transition region. The as-deposited SIPOS layer is the *amorphous silicon-containing compound* over the substrate.

279. Kwark discloses forming an interfacial oxide layer on a silicon substrate and forming a SIPOS film composed of a class of silicon oxides (which are silicon-containing compounds) thereon. Kwark, 742 (“an interfacial layer between the SIPOS and underlying silicon may play an important, if not dominant, role with the implication that the high oxygen concentrations previously used may not be essential for J_{0e} reduction.”), *see also* Kwark, 742 (“Deliberate introduction of controlled amounts of an oxygen bearing species...into the deposition ambient normally used for

chemical vapor deposition of polysilicon produces SIPOS, a class of silicon oxides which exhibits a wide range of physical properties.”)

280. Kwark also discloses the SIPOS is not crystallized as-deposited but crystallizes during subsequent annealing. Kwark, FIG. 3.

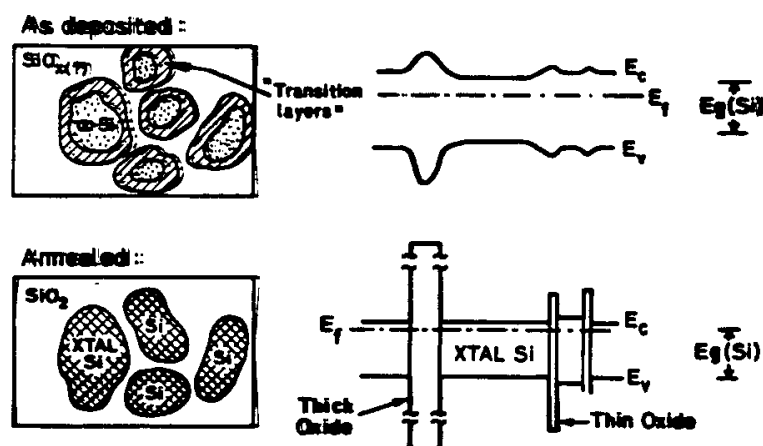


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the “oxide-like” regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Kwark, FIG. 3.

281. Kwark further discloses that the SIPOS would block hole transport. Kwark, 743 (“In N-type SIPOS emitter contacts the lining up of the equilibrium Fermi levels results in a barrier in the valence band which blocks hole transport and accounts for the reduction, in J_{0e} .”) A POSITA would understand that the SIPOS is passivating, because the hole suppression means fewer holes available for recombination, thereby

reducing recombination - that is, it provides a passivation effect. Kwark also discloses that the SIPOS is conductive. Kwark, 743 (“The addition of a dopant species converts [the SIPOS] films from semi-insulating to a form that can be made sufficiently conductive after annealing to make them interesting for electronic applications.”)

282. Kwark also discloses that the interfacial oxide layer may suppress hole currents. Kwark, 743 (“the formation of an interfacial oxide layer as a result of the annealing process (FIG. 3), may be primarily responsible for the reduced hole currents.”) A POSITA would understand that the interfacial oxide layer may function as an interfacial passivation layer because the hole suppression means fewer holes available for recombination, thereby reducing recombination—that is, it provides a passivation effect.

b) Limitation 3[b]: “and the providing thermal treatment of about 500°C. or higher separates the amorphous silicon-containing compound into the at least one interface passivation layer and the at least one conductive and passivating layer.”

283. Borden in view of Kwark renders this claim element obvious.

284. Kwark discloses that after the deposition of the SIPOS layer, i.e. the claimed amorphous-silicon containing compound, a high-temperature thermal treatment (e.g., by annealing) is conducted at a temperature in the range 800°C to 1000°C. For example, FIG. 5 of Kwark depicts that the SIPOS annealing temperature is in the range 800°C to 1000°C.

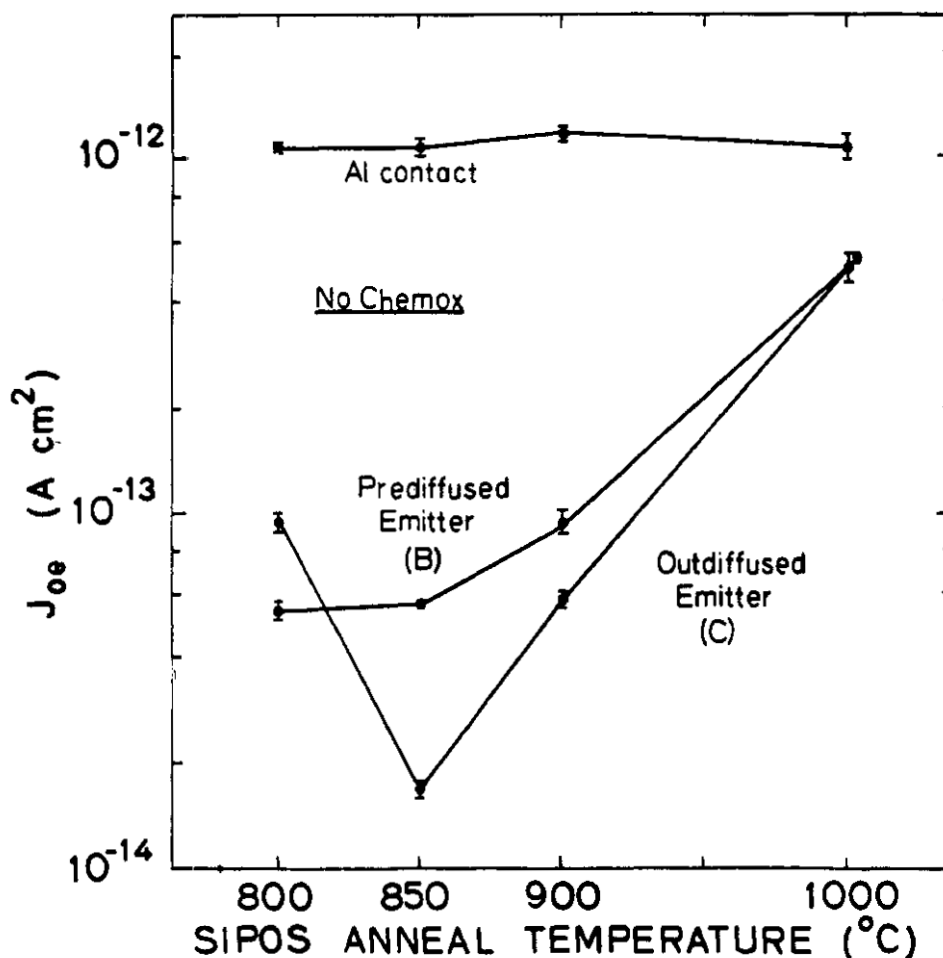


Fig. 5: emitter saturation current vs. anneal temperature for SIPOS contacts without a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

Kwark, FIG. 5.

285. Kwark further discloses that this high-temperature thermal treatment induces phase separation in SIPOS to separate into a micro-crystallite layer and an interfacial oxide layer. Kwark, 743 (“Postulating the formation of a thin tunnelable interfacial oxide as a consequence of the high temperature annealing step is consistent

with the observed similarities in J_{0e} .”) *See also* Kwark, 743 (“This conclusion suggests...that the distinguishing feature of SIPOS may be its built-in source of oxygen which aids in the formation and/or maintenance of this interfacial layer.”) *See also* Kwark, 742 (“the CVD deposited SIPOS films used in these devices require a high temperature anneal in order to activate the dopant. A phase precipitation which results in a fine dispersion of silicon microcrystallites embedded in an oxygen rich matrix appears to be the result of such anneals.”)

286. According to Kwark’s disclosures, a POSITA would understand that Kwark’s thermal treatment *separates the amorphous silicon-containing compound*, i.e. the as-deposited SIPOS layer, into the “tunnelable interfacial oxide” which is the *one interface passivation layer* and the layer that contains the “silicon microcrystallites”, the *conductive and passivation layer*. The latter as per Kwark is a mixture of crystallized doped silicon regions and silicon dioxide regions which are formed as a consequence of the annealing process. Kwark, 742. A POSITA would be motivated to combine Kwark’s method of simultaneously forming a conductive SIPOS layer and an interfacial oxide via annealing with Borden’s solar cell fabrication process to replace Borden’s separate deposition steps for the tunnel dielectric layer and polysilicon layer. As discussed in Section VIII.C.1, this integration achieves two critical advantages: (1) it enables an optimal balance between passivation efficacy and suppression of dopant

outdiffusion; and (2) it significantly simplifies the manufacturing process. Both outcomes constitute long-standing industry-desired benefits.

5. Claim 4: “The method of claim 1, wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.”

287. Borden teaches or suggests this limitation.

288. The '074 patent does not explicitly define the morphology and formation principle of perforations. To the extent that First Solar claims that the perforations occur when carrier transport such that the adjacent layers 1831 and 1871, as shown in '074 patent Figure 18, can make contact with the wafer 185 directly. Borden has provided teachings under this interpretation.

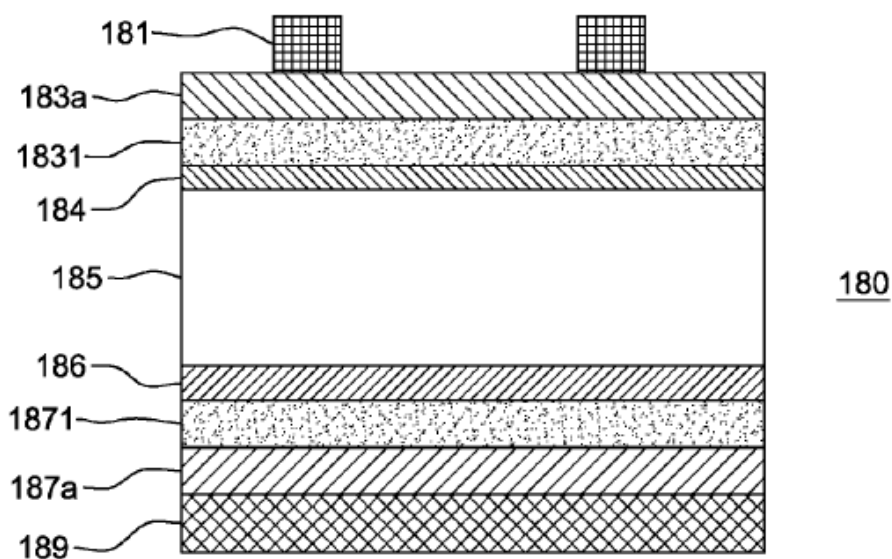


FIG. 18

'074 patent, FIG. 18.

289. Borden discloses forming a tunnel dielectric layer on a substrate, followed by deposition of amorphous silicon and subsequent crystallization at elevated temperatures (e.g., 1000°C). With respect the thin tunnel dielectric layer, Borden discloses that “[t]hree base oxide layers were used: chem-ox, which is a chemical oxide formed after the standard MOS clean, and 8 and 10Å thick rapid thermal oxides (RTO).” Borden, 1150.

290. A POSITA would understand that all three of Borden’s tunnel dielectric layers comprise a silicon oxide layer. As discussed in Section VIII.B.3, it was well known that the thin silicon oxides are not thermally stable when heated at high temperatures. Consequently, during Borden’s thermal treatment (which according to Borden is at 1000°C), due to the significantly different thermal expansion coefficients between the tunnel dielectrics layer (primarily composed on silicon oxides) and the adjacent silicon layers above and below, the tunnel dielectrics layer becomes discontinuous and holes are formed; these discontinuities and holes in the tunnel dielectric are the claimed *perforations*.

291. Alternatively, Borden in view of Gan renders this claim element obvious.

292. Gan discloses a solar cell structure with an interfacial oxide between the substrate and the polysilicon layer. Gan, 245 (“It was found that, between the polysilicon and the substrate, there always exists a very thin oxide (interfacial oxide)”).

As discussed for claim 1, the solar cell structure disclosed by Borden also has a similar structure, namely, a tunnel dielectric layer between the substrate and the poly layer, the composition of which is also an oxide of silicon.

293. Gan also discloses that the oxide is not thermally stable and therefore breaks up at high temperatures. Gan, 245 (“the oxide is not thermally stable; i.e., it tends to break up during high temperature anneals.”) Specifically, Gan further discloses that as the oxide breaks down under thermal treatment, “channels” are formed, allowing the substrate and the polysilicon layer to establish “intimate contact” in these broken regions. Gan, 249 (“As the oxide starts to break up, additional conductive channels are created due to the intimate contacts formed between the polysilicon and the substrate in the broken regions.”)

294. A POSITA, guided by Gan’s teachings, would understand that such channels connect the upper and lower surfaces of the oxide layer—in other words, perforations would form during the thermal treatment process. According to Gan’s teachings a POSITA would understand that by adjusting the annealing conditions (temperature and time) it is possible to obtain a structure that has low contact resistance (ρ_c) and low saturation current (J_0), two parameters that are important for a high performance solar cell. Borden discloses that “high tunnel layer thickness causes a strong series resistance problem.” Borden, 1151. Borden also discloses that “the path to a high efficiency PE cell structure is clear. The requirements include: A p-PE/c-Si(n)

structure to minimize j_0 and maximize lifetime...Following these guidelines, it should be possible to exceed 20% efficiency with a planar PE cell structure.” Borden, 1151-52. A POSITA in order to achieve Borden’s requirements for a solar cell having an efficiency that exceeds 20%, would modify the annealing conditions as per Gan’s teaching. Gan teaches that “[w]hen the interfacial oxide is intact, tunneling is the only process available for the majority carriers to pass through the interfacial oxide. This usually results in a high contact resistance because of low tunnelling probability. As the oxide starts to break up, additional highly conductive channels are created due to the intimate contacts formed between the polysilicon and the substrate in the broken regions.” Gan, 249. Therefore, a POSITA would understand that by applying Gan’s teachings of forming “a very small fraction of interfacial oxide breakup” into Borden’s interfacial oxide (as discussed in Section VIII.C.2) would result in a robust and reproducible process which would also improve Borden’s solar cell performance as direct result of a low J_0 and a low ρ_c . Since Borden and Gan both disclose similar processing steps a POSITA would understand that modifying Borden’s processing steps for forming Gan’s “very small fraction of interfacial oxide breakup” would entail simple experimentation on the growth of thermal oxide (a step disclosed by Borden) and the thermal anneal process (a step also disclosed by Borden). A POSITA would understand that by modifying Borden in view of Gan, then as per Gan’s teaching “additional conductive channels are created due to the intimate contacts formed

between the polysilicon and the substrate in the broken regions.” A POSITA would understand that the Gan’s disclosed “additional conductive channels” *allow carrier transport therethrough*.

295. Alternatively, Borden in view of Swanson renders this claim element obvious.

296. Swanson first discloses *an interface passivation layer* (an “interfacial oxide 16”) layer on top of *the substrate* (silicon substrate 10). Swanson, 2:43-60 (In FIG. 4A...over the contact areas in contact with **the thermally grown oxide 16**. FIG. 4B is an enlarged view of the one region of a contact area showing...on the **interfacial oxide 16 formed on the surface of silicon substrate 10**.”) *See also* Swanson, FIGs. 4A-4B.

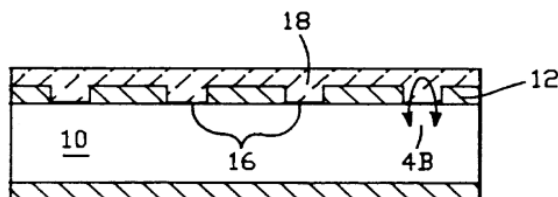


FIG.—4A

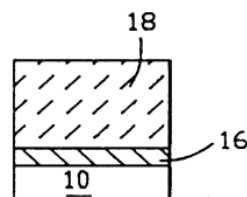


FIG.—4B

Swanson, FIGs. 4A and 4B.

297. Swanson further discloses a *thermal treatment* (over 500°C) *results in perforation of the at least one interface passivation layer* (“interfacial oxide 16”) *to allow carrier transport therethrough*. Swanson, 2:61-3:4 (“Thereafter as shown in

FIGS. 5A and 5B the structure **is annealed at a high temperature to break the interfacial oxide and permit electrical contact between the polysilicon emitters and the underlying substrate...**For solar cell applications, **the typical anneal temperature is 1050°C...**As shown in the enlarged view of FIG. 5B, the **interfacial oxide is broken partially and polysilicon contacts the substrate intimately in the broken areas.**") *See also* Swanson, FIGs. 5A-5B.

298. Swanson also teaches "the contact resistance is reduced by the presence of the broken regions in the thin silicon oxide layer which are created during the first anneal, as described above." Swanson, 3:28-31.

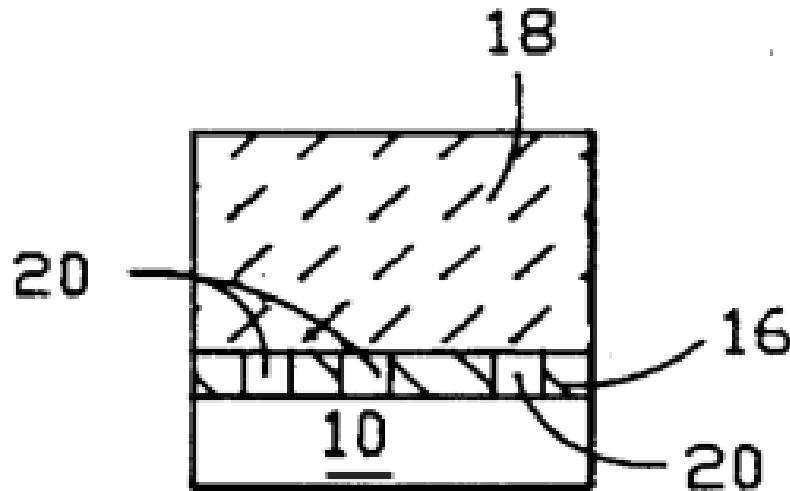


FIG.—5B

Swanson, FIG. 5 (annotated).

299. A POSITA, guided by Swanson’s teachings, would understand that when the **“interfacial oxide is broken partially”** the **“polysilicon contacts the substrate intimately in the broken areas”** —in other words, perforations form during the thermal treatment process. According to Swanson’s teachings, a POSITA would understand that by adjusting Borden’s processing conditions, it is possible to obtain a structure with low contact resistance (ρ_c) and low saturation current (J_0), two parameters crucial for a high-performance solar cell. Borden discloses that “high

tunnel layer thickness causes a strong series resistance problem.”. Borden, 1151. Borden also discloses that “the path to a high efficiency PE cell structure is clear. The requirements include: A p-PE/c-Si(n) structure to minimize J_0 and maximize lifetime...Following these guidelines, it should be possible to exceed 20% efficiency with a planar PE cell structure.” Borden, 1151-52. To achieve Borden’s requirements for a solar cell with an efficiency exceeding 20%, a POSITA would modify the processing conditions according to Swanson’s teachings. Therefore, a POSITA would understand that by applying Swanson’s teachings of forming an “**interfacial oxide [that] is broken partially**” into Borden’s interfacial oxide (as discussed above in the section motivation to combine Swanson and Borden) would result in a robust and reproducible process which would also improve Borden’s solar cell performance as direct result of a low J_0 and a low ρ_c . Since Borden and Swanson both disclose similar processing steps, a POSITA would understand that modifying Borden’s processing steps for forming Swanson’s “interfacial oxide [that] is broken partially” would entail simple experimentation on the growth of thermal oxide (a step disclosed by Borden) and the thermal anneal process (a step also disclosed by Borden). A POSITA would understand that by modifying Borden in view of Swanson then as per Swanson’s teaching “**polysilicon contacts the substrate intimately in the broken areas.**” A POSITA would understand that the Swanson’s disclosed areas, where the polysilicon contacts the substrate intimately, *allow carrier transport therethrough*.

D. Ground 4: Claims 1-2 and 4-8 are Obvious over Rana

1. Claim 1

a) Limitation 1[pre]: “A method of fabricating a solar cell, comprising;”

300. To the extent the preamble is limiting, Rana teaches or suggests this preamble.

301. For example, Rana discloses that “[t]his invention relates generally to silicon solar cells and, more particularly, to a method for obtaining a desired dopant profile in the emitter of a solar cell device.” *See* Rana, [0002].

b) Limitation 1[a]: “providing a wafer as a central substrate;”

302. Rana teaches or suggests this limitation.

303. Rana discloses a **crystalline silicon substrate** as a central substrate. *See* Rana, [0009] (“The present invention provides a method for forming an emitter in a crystalline silicon substrate by depositing a first lightly doped layer of amorphous silicon on a surface of the substrate.”), *see also* Rana, [0023]-[0025], FIGs. 1-3, 4a-4c. In addition to the first lightly doped layer on a surface of the substrate, Rana also discloses “[s]ubsequent to the deposition of the lightly doped amorphous silicon layer, a heavily doped phosphorus amorphous silicon layer is applied over the lightly doped region, as illustrated at step 14.” Rana, [0027]. Rana also discloses that “additional

processes such as metallization or patterning processes may be included to provide the front and rear contacts for a solar cell.” Rana, [0045].

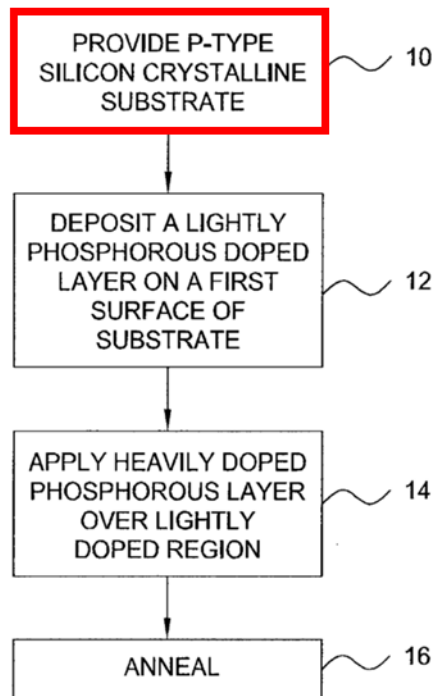


FIG. 1

Rana, FIG. 1 (annotated).

304. Rana discloses “[t]he substrate may be formed of single crystalline silicon or multi-crystalline silicon, depending on the particular application of the product to be produced. In one embodiment, the substrate is a monocrystalline substrate (e.g., Si<100> or Si<111>).” Rana, [0024]. A POSITA would understand that crystalline silicon, when utilized as a substrate material for solar cell manufacturing, either as a single crystalline or as multicrystalline silicon, is conventionally provided in wafer

form. Both types of silicon wafers were used extensively to manufacture solar cells. A POSITA would further understand that the crystalline silicon substrate can serve as the central substrate, consistent with Rana's teaching of applying functional layers and metallization on both its sides.

c) **Limitation 1[b]: “depositing or growing at least one amorphous interface passivation layer over the substrate;”**

305. Rana teaches or suggests this limitation.

306. Rana discloses depositing a **lightly doped layer of amorphous silicon** on the surface of the substrate, which is the *interface passivation layer*. Rana, [0009] (“The present invention provides a method for forming an emitter in a crystalline silicon substrate by depositing a first lightly doped layer of amorphous silicon on a surface of the substrate.”), *see also* Rana, [0038], [0041], [0042], FIGs. 1, 3, 4a.

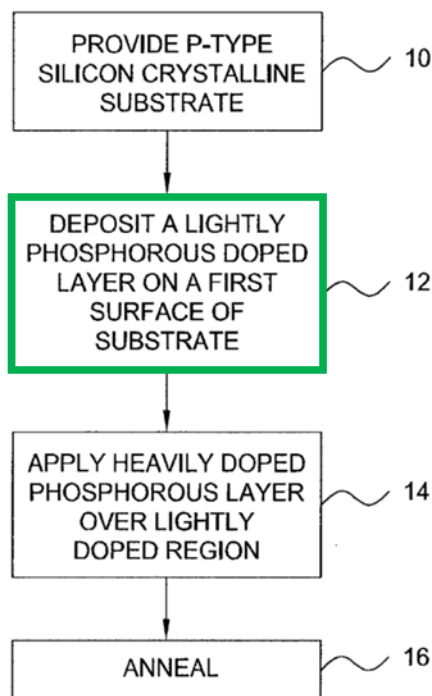
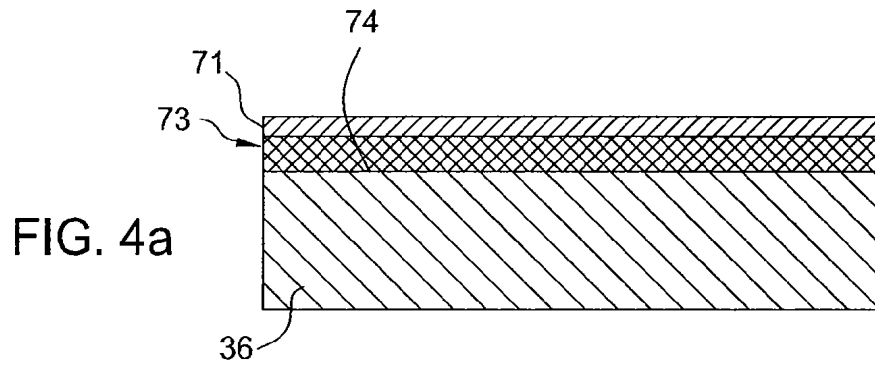


FIG. 1

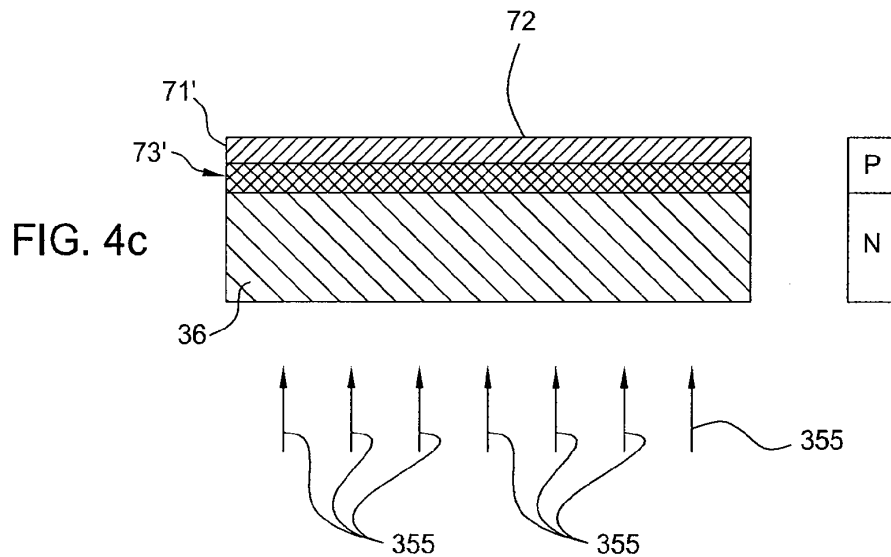
Rana, FIG. 1 (annotated)

307. Rana discloses “[t]he substrate may be formed of single crystalline silicon or multi-crystalline silicon, depending on the particular application of the product to be produced. In one embodiment, the substrate is a monocrystalline substrate (e.g., <Si-100> or <Si-111>).” Rana, [0024]. A POSITA would understand that the lightly doped layer of amorphous silicon (element 73 in FIG. 4a of Rana) is passivating, as Rana teaches that this layer can inhibit or reduce recombination at the interface. *See* Rana, [0023] (“The doping in the lightly doped layer is low enough so that the recombination of the minority carriers is inhibited or reduced, resulting in high carrier

collection.”) The ’074 patent does not define “passivation/passivating.” However, it discloses that “Surface passivation provides suppression of recombination of electrons and holes at or in the vicinity of certain physical surfaces within the solar cell.” ’074 patent, 3:50-52. Therefore, a POSITA would understand that the lightly doped layer of amorphous silicon in Rana, which inhibits or reduces carrier recombination, serves a passivation function. Moreover, Rana discloses that after a subsequent thermal treatment the amorphous silicon layer 73 will crystallize and after completion of the crystallization process “the converted silicon layers 73’, 71’, which were in amorphous state, will assume the same grain structure as the underlying crystalline silicon substrate 36 due to solid phase epitaxial growth from the first surface 74 of the substrate 36 having that grain structure.” Rana, [0042] *see also* FIGs. 4a, 4c. A POSITA would understand that after the solid phase epitaxial crystallization, the crystallized silicon layer 73’ will reduce or eliminate any dangling bonds at the surface of the substrate 36 as the silicon atoms of this layer near the interface with the substrate 36 form bonds with the atoms at the surface of the silicon substrate 36, hence passivate the surface of the substrate.



Rana, FIG. 4a.



Rana, FIG. 4c.

308. In addition to lightly doped amorphous silicon, a POSITA would also understand that depositing an undoped layer is another viable design choice, as Rana teaches that doping the amorphous silicon layer is optional rather than mandatory. *See* Rana, [0038] (“As described above, **if desired**, this layer of amorphous silicon layer **may** be doped with phosphorous to provide an emitter with a dopant concentration at about 1×10^{18} atoms/cm or **less** after anneal.”) As discussed in Section VIII.A.1.d, it

was known that the deposition of an undoped amorphous silicon layer on a crystalline silicon substrate serves to passivate the silicon surface and thus provides interface passivation. Froitzheimat, 183 (“ultra thin a-Si:H(i) layers on c-Si(p) reduce interface recombination more effectively than a-Si:H(n)”), *see also* Taguchi, 866 (“The HIT (Heterojunction with Intrinsic Thin-layer) structure, which features a very thin intrinsic a-Si layer inserted between p-type a-Si and n-type c-Si...enables an excellent surface passivation and p-n junction, resulting in high efficiency.”) Therefore, under Rana’s teachings, a POSITA would have the discretion to choose between an undoped or lightly doped configuration, since both layers meet the requirement of reducing carrier recombination and thereby providing interface passivation. The ’074 patent also discloses that undoped amorphous silicon is an example of an amorphous interface passivation layer. ’074 patent, 3:57-58 (“Another example of a surface passivating layer is intrinsic amorphous silicon.”)

d) Limitation 1[c]: “depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant,”

309. Rana teaches or suggests this limitation.

310. Rana discloses depositing a heavily doped amorphous silicon layer on the surface of the layer of lightly doped amorphous silicon layer, which is the *conductive and passivating layer*. *See* Rana, [0027] (“Subsequent to the deposition of the lightly

doped amorphous silicon layer, a heavily doped phosphorous amorphous silicon layer is applied over the lightly doped region, as illustrated at step 14.”), *see also* Rana, [0009], [0028], [0042], FIGs. 1, 4a.

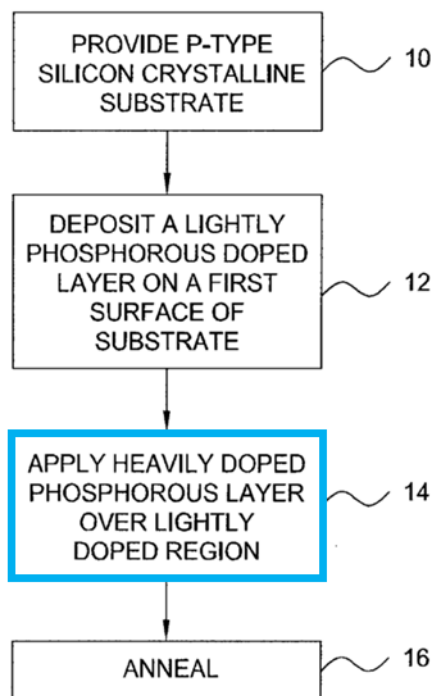


FIG. 1

Rana, FIG. 1 (annotated).

311. A POSITA would understand that the heavily doped amorphous silicon layer is conductive and passivating.

312. First, a POSITA would understand that the heavily doped amorphous silicon layer is conductive. Specifically, Rana expressly teaches that this layer is doped to have the opposite “conductivity” type from the substrate. *See* Rana, Claim 2 (“The

method of claim 1, wherein a dopant disposed in the first and the second amorphous silicon layers has opposite conductivity type from the crystalline silicon substrate.”), *see also* Rana, [0023]. In one embodiment, Rana teaches that the heavily doped amorphous silicon layer incorporates phosphorus dopants. *See* Rana, [0027]. Rana also discloses that “the concentration of the phosphorous atoms in the heavily doped layer is approximately higher than about 1×10^{19} atoms/cm³.” Rana, [0034]. A POSITA would understand that the phosphorus dopants in silicon act as an n-type dopant, since they provide additional free electrons, thereby enhancing conductivity of the silicon. Rana also discloses that when “amorphous silicon material is phosphorous doped” it is “(n-type).” Rana, [0030].

313. Second, a POSITA would understand that the heavily doped amorphous silicon layer is passivating. As discussed in Section VIII.A.1.e, depositing a doped amorphous silicon layer on top of an undoped amorphous silicon above a silicon substrate can also provide interface passivation. *See* Froitzheim, 183 (“Best results are obtained by combining a-Si:H(n) layers with a-Si:H(i) layers. The a-Si:H(i) layer reduces interface recombination at the interface due to a low defect density in the gap, and the a-Si:H(n) layer further reduces recombination at the interface due to enhanced band bending which leads to an additional field passivation.”) Rana teaches that, compared to conventional processes, its heavily doped amorphous silicon layer—when deposited on lightly doped amorphous silicon—can reduce the “dead” zone where

significant recombination occurs. *See* Rana, [0023] (“[T]he second layer, which is a thin heavily doped layer, is deposited onto the first lightly doped amorphous silicon layer to limit the thickness of the [‘]dead[’] region as discuss previously.”) A POSITA would understand that such a reduction in the “dead” zone would provide passivation.

- e) **Limitation 1[d]: “providing thermal treatment at a temperature of above 500°C. or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer; and,”**

314. Rana teaches or suggests this limitation.

315. Rana discloses that after the deposition of the two amorphous layers, depicted as steps 12 and 14 in the process flow diagram depicted in FIG. 1, a thermal anneal step is performed. Specifically with respect to this thermal anneal “step 16,” Rana discloses “[a]s shown at step 16, after the two layers of amorphous silicon layer have been deposited on the surface of the substrate, the substrate with the lightly and heavily doped amorphous silicon layers is annealed by delivering heat energy to the substrate at a desired temperature for a desired period of time sufficient to form the emitter.” Rana, [0029].

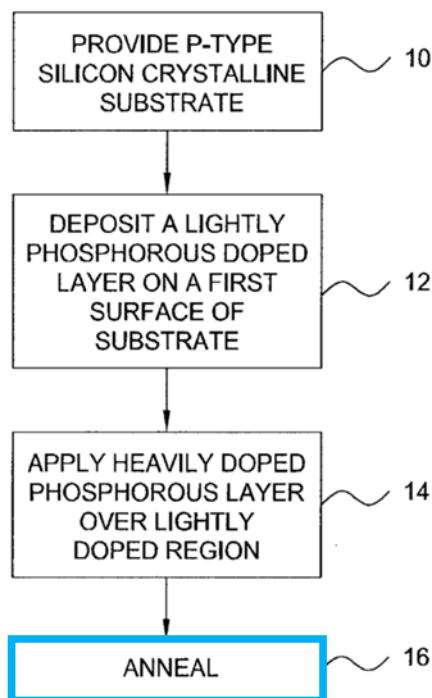


FIG. 1

Rana, FIG. 1 (annotated)

316. Rana further discloses that the thermal treatment is performed through rapid thermal processing. *See* Rana, [0039] (“FIG. 3 is a schematic, cross-sectional view of a chamber 60 for heating...the chamber 60 is a rapid thermal processing (RTP) chamber within which the application of the heat is controlled. For clarity, a single substrate 36 is shown in FIG. 3.” Rana discloses that the temperature during the thermal treatment is in the range 750°C to 1,200°C. *See* Rana, [0040] (“The heat energy 355 may be applied to the second surface 250 of the silicon substrate 36 at a temperature of about 750°C to about 1200°C”). Rana also discloses that the heat is

applied for a period that varies “from approximately 5 seconds” to a period of “over 30 minutes.” Rana, [0030].

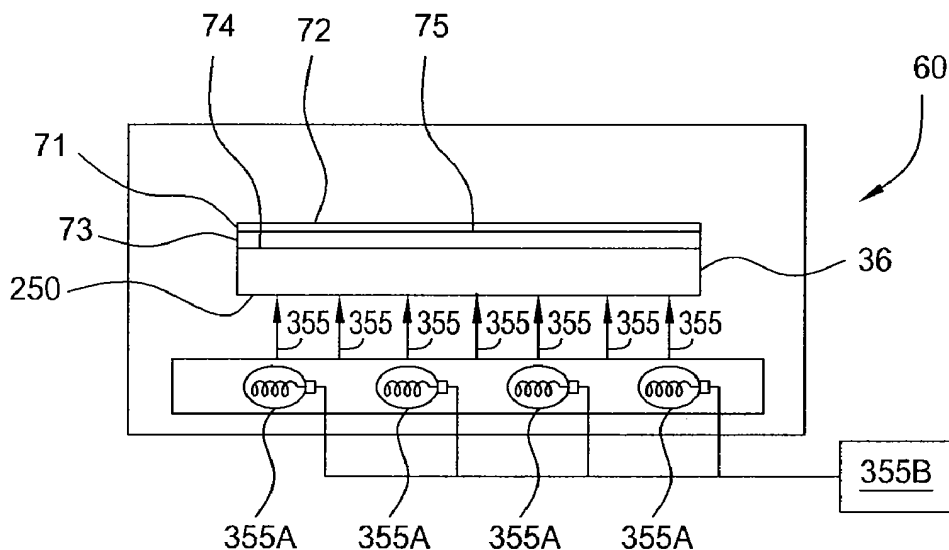
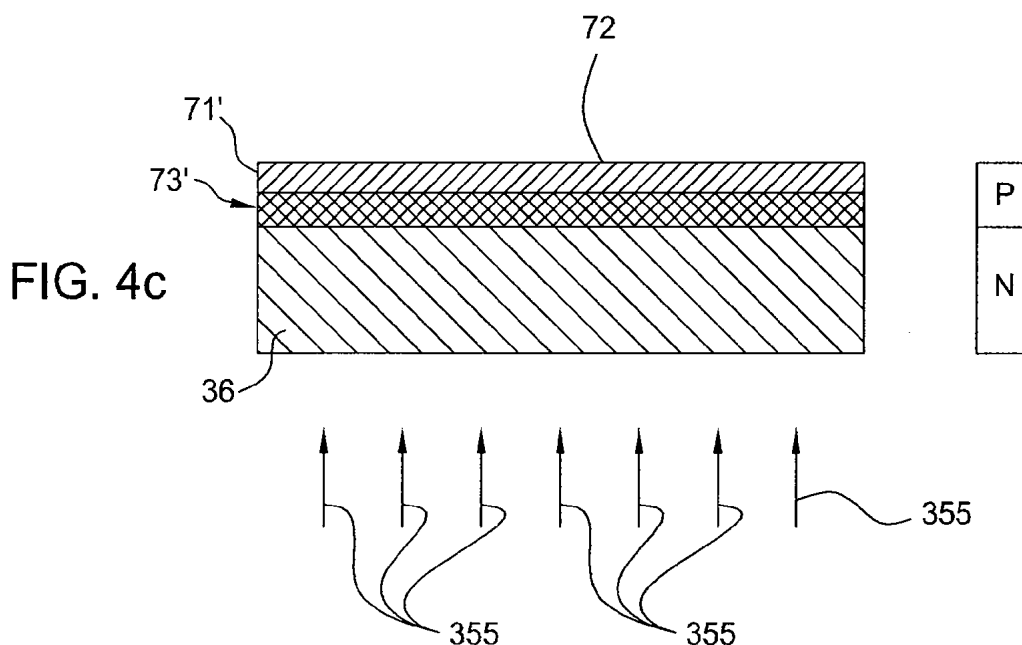


FIG. 3

Rana, FIG. 3.

317. Rana further discloses that during the thermal treatment, the heavily doped amorphous silicon is crystallized. *See* Rana, [0010] (“heating the crystalline silicon substrate and the first and second amorphous silicon layers to a temperature sufficient to cause solid phase epitaxial crystallization of the first and second amorphous silicon layers.”) Rana also discloses that “[u]pon the completion of this directional crystallization process, the converted silicon layers 73’, 71’”, which were in amorphous state, will assume the same grain structure as the underlying crystalline

silicon substrate 36” and that “[t]he resulting crystalline structure after heat treatment in the RTP chamber has a consistent grain structure, as shown in FIG. 4c.” *See* Rana, [0042]-[0043]; *See also* Rana, [0013], [0029].



Rana, FIG. 4c.

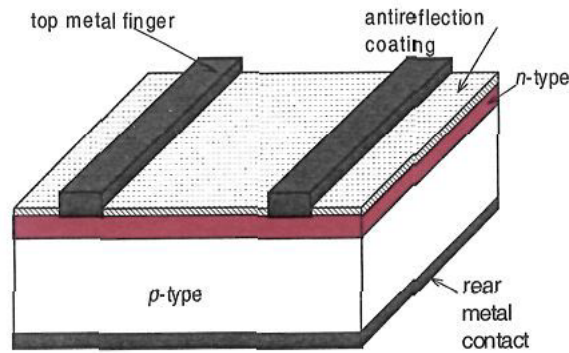
318. Rana further discloses that during the annealing process, the heat energy not only induces crystallization of the heavily doped amorphous silicon layer but also facilitates diffusion of the dopants into the substrate. *See* Rana, [0042] (“Thereafter, the substrate 36 with the deposited amorphous silicon layers 73, 71 is annealed...at a temperature sufficient to activate and cause the dopant atoms (e.g., phosphorous) in the lightly and heavily doped amorphous silicon layers 73, 71 to diffuse into the substrate 36 a desired distance, depending upon the given heating energy”).

f) Limitation 1[e]: “providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof”

319. Rana teaches or suggests this limitation.

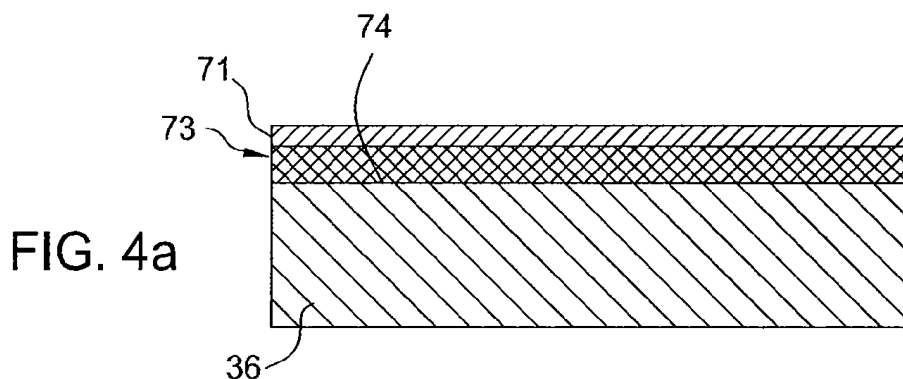
320. Rana teaches that the metallization provides the contacts to both the front and rear sides of the solar cell and that the metallization is performed after the thermal treatment. *See* Rana, [0045] (“following the deposition processes described above, additional processes such as metallization or patterning processes may be included to provide the front and rear contacts for a solar cell.”) It is commonly known that contacts on solar cells typically function as electrodes.

321. As discussed in Section V, and as Rana discloses, the metallization processes form the electrodes that serve as the electrical contacts on the front (or top side), which is the light entering side, and the rear (or back side). It was well known that the metal electrode on the front or top side has an interconnected finger structure, as shown in the figure below, in order to reduce the light losses caused by reflection from the metal electrodes, while the rear metal electrode typically covers the entire back side as shown.



Green, FIG. 4.3a.

322. In my analysis, I use Rana's "Emitter with Desired Dopant Profile" embodiment. The general structure of this embodiment, as shown in FIG. 4a, comprises of amorphous silicon layers element 73 (*interface passivation layer*) and element 71 (*conductive and passivation layer*) that coat one surface, element 74 of the silicon substrate element 36 (*central substrate*). See Rana, [0042] ("The embodiment illustrated in FIG. 4a shows a substrate 36 having a first lightly doped amorphous silicon layer 73 and a second heavily doped amorphous silicon layer 71 sequentially deposited **on a first surface 74** of the substrate 36.") Note that after the thermal anneal as explained in 1[d] above, the crystallized amorphous silicon layers, 71 and 73, are depicted as elements 71' and 73' which coat the one surface of the substrate as shown in FIG. 4c.



Rana, FIG. 4a.

323. Rana also discloses several other embodiments which collectively are called as “Selective Emitter.” In a “selective emitter” embodiment, the highly doped amorphous silicon layer (element 71) is selectively formed and thus covers only portions of one surface (element 74) of the substrate. *See* Rana, [0047] with respect to the FIG. 5 (“the deposition of heavily doped amorphous silicon layer is selectively deposited on the lightly doped amorphous silicon layer 73 in **pre-defined discrete areas** (e.g., reference numeral 71) where the low resistance contact material is to be provided for utilization in attaching the **metal contacts on the front surface 37** of the solar cell.”) Rana further explains with respect to the FIG. 6 that “[t]he end result after application of the heat in the RTP chamber is illustrated in FIG. 6, where the heat energy 355...will also crystallize the lightly doped amorphous silicon layer 73 and heavily doped **discrete regions** 71...thereby forming crystalline lightly doped n-type layer 73’ and heavily doped low contact resistance regions 71’ to which the

metallization will be applied to form the front contacts for the solar cell” Rana, [0047].

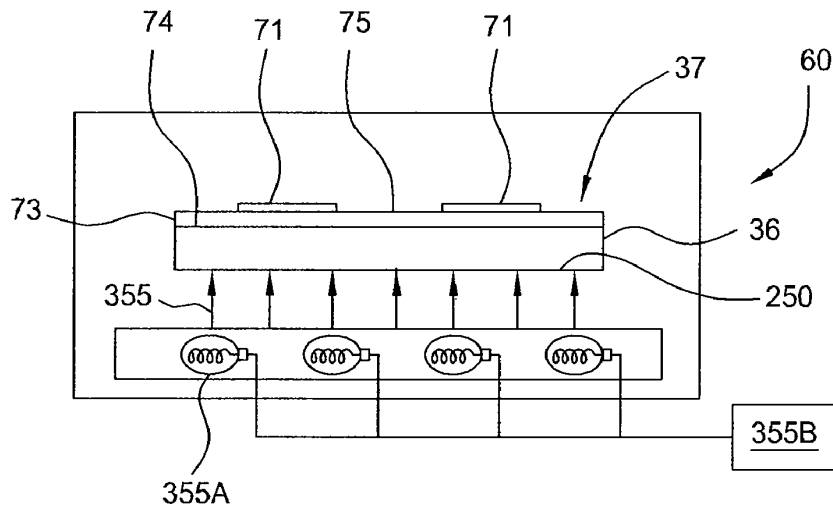


FIG. 5

Rana, FIG. 5.

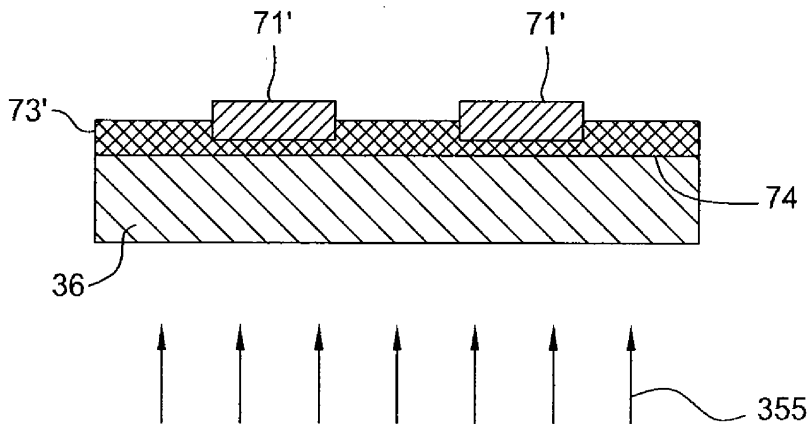
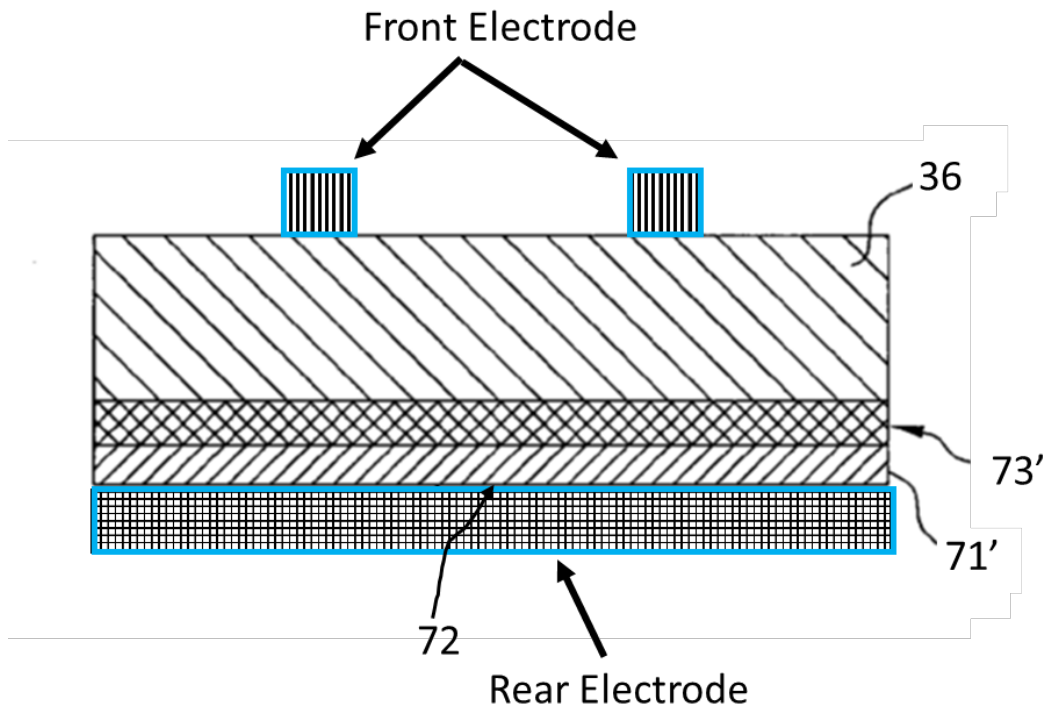


FIG. 6

Rana, FIG. 6.

324. A POSITA would understand that in general, the placement of the two amorphous silicon layers (elements 73 and 71 as the interface passivation layer and the conductive and passivation layer, respectively) with respect to the front (or top, i.e., light entering) side or the rear side of a solar cell is a design choice. A POSITA would also understand that Rana is teaching the “selective emitter” structure when these layers are formed on the front side of a solar cell. According to Rana, as discussed above, the highly doped amorphous silicon will be formed selectively only in the areas where the front contacts, i.e., the fingers of metal electrodes, will be placed by the metallization process to achieve “the low resistance contact material.” It was well known that the contact resistance between a metal electrode and a semiconductor layer is low when the doping of the semiconductor layer is high. *See* Rana, [0049] (referring to another embodiment having the selective emitter structure depicted in FIG. 7g and teaching “forming a plurality of heavily doped regions 126, 128, 130, and 132 in the body of the substrate 100. The resulting structure is then passed on to a metallization process **where the metal front contacts** are to be applied to the regions 126,128, 130, and 132 to provide the selective emitters for a silicon solar cell.”)

325. A POSITA would also understand that when the two amorphous layers are formed on the rear side of the solar cell (i.e. the side opposite to the light entering side) according to Rana's "Emitter with Desired Dopant Profile" embodiment the highly doped amorphous silicon covers the entire rear surface of the solar cell substrate area in order to provide a "low contact resistance material" across the entire rear side because the rear metal electrode covers the entire rear surface of the solar cell and thus is in direct contact with the surface 72 of the crystallized heavily doped amorphous silicon layer 71'. Thus, a POSITA would understand that the structure of the front and rear contacts would be as shown below, after the completion of the additional "metallization or patterning processes" in Rana's "Emitter with Desired Dopant Profile" embodiment. Rana, [0045].



Rana, FIG. 4c (annotated)

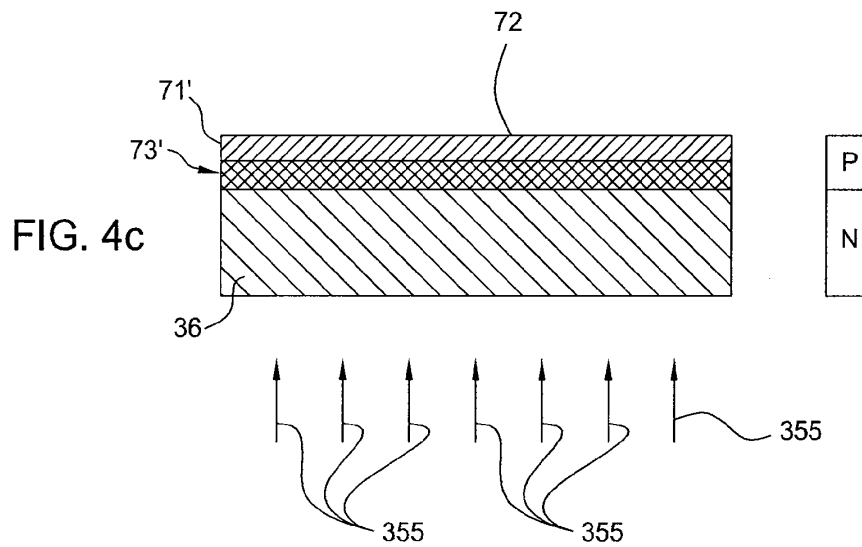


FIG. 4c

Rana, FIG. 4c.

326. A POSITA would understand that such metallization occurs after thermal treatment, as Rana, [0045] expressly states that metallization “follow[s] the deposition processes described above.” *See* Rana, [0045] (“following the deposition processes described above, additional processes such as metallization or patterning processes may be included to provide the front and rear contacts for a solar cell.”) These “deposition processes” include “crystallizing the doped amorphous silicon layers” through thermal processing, where the heavily doped amorphous silicon layer is one of the doped amorphous silicon layers. *See* Rana, [0009] (“[t]he present invention provides a method for forming an emitter in a crystalline silicon substrate by depositing a first lightly doped layer of amorphous silicon on a surface of the substrate. Thereafter, a second amorphous silicon layer, which is heavily doped, is deposited over the full or selected portions of the first deposited amorphous silicon layer. The layer stack is then subjected to a thermal treatment that generates a selectively heavily doped surface region where the metallization is to be applied.”) According to Rana’s explicit disclosures, a POSITA would understand that the metallization is applied after the thermal treatment.

327. Rana specifically also discloses that the metallization contacts the crystallized heavily doped silicon layer, i.e., the *conductive and passivation layer*. *See* Rana, [0009] (“The layer stack is then subjected to a thermal treatment that generates a selectively heavily doped surface region where the metallization is to be applied.”),

See also Rana, [0047], [0049]. As I explained above, a POSITA would understand that Rana is teaching the direct contact between a metal electrode and the heavily doped, crystallized silicon layer (element 71), the conductive and passivation layer, to achieve low contact resistance. Though Rana's explicit teaching regarding "low contact resistance material" is within the context of a different embodiment, a POSITA would understand that it applies to all embodiments.

- g) Limitation 1[f]: "wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer."**

328. Rana teaches or suggests this limitation.

329. Specifically, as discussed in Section VIII.D.1.e, Rana discloses that the thermal treatment causes the dopant to diffuse into the substrate. Conductive paths for charge carriers are therefore formed via the dopant diffused from the heavily doped amorphous layer (i.e., the *conductive and passivating layer*) throughout the lightly doped amorphous layer (i.e., the *interface passivation layer*) into the substrate. A POSITA would understand that this process provides shortened charge flow paths between the substrate and the electrode that contacts the crystallized heavily doped silicon layer.

330. The '074 fails to define or disclose “shortened charge carrier flow paths” as required in this claim element. The '074 patent describes the “shortest geometrical” charge carrier flow path as the one that occurs when the “[charge carriers]” transport within the emitter is **vertical instead of mainly lateral.**” According to the '074 patent, such vertical transport path is formed when using an electrode that has a “full area contact coverage” with the emitter, and the emitter is on the back side of the substrate, as shown in Figure 3. '074 patent. 4: 47-51 (explaining Figure 3 “The minority carriers (solid lines) can use the **shortest geometrical path** to reach the rear n-type emitter 38, and their transport within the emitter is **vertical instead of mainly lateral.**”)

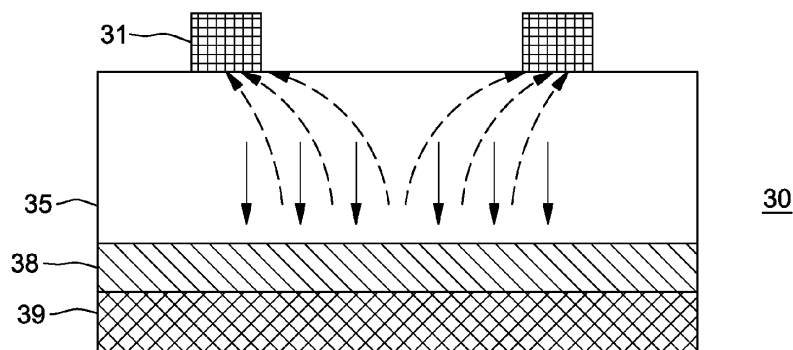
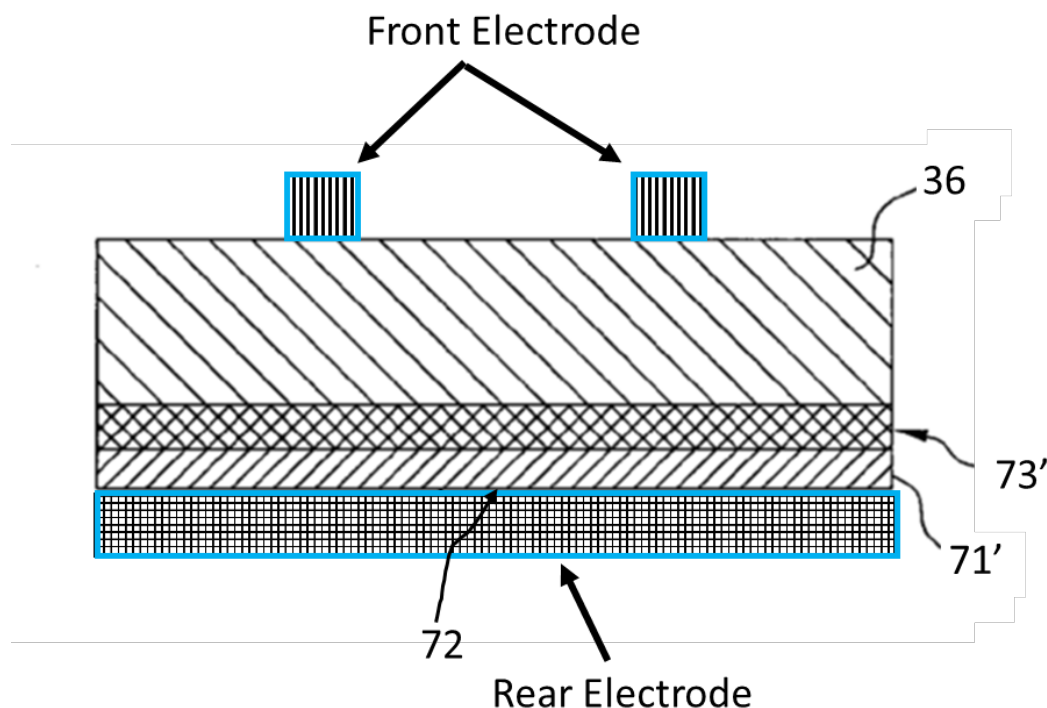


FIG. 3

'074 patent, FIG. 3.

331. As I explain in the discussion of 1[e], a POSITA, according to Rana's teachings, would understand that Rana is disclosing a solar cell structure, repeated below, which is the same as the Figure 3 of the '074 patent.



Rana, FIG. 4c (annotated).

332. Rana also explicitly discloses that the metallization contact covers the heavily doped surface region, i.e., the region formed after crystallization of the heavily doped amorphous silicon layer, as shown in element 71 of the annotated figure below. *See* Rana, [0009] (“Thereafter, a second amorphous silicon layer which is heavily doped is deposited over the **full** or selected portions of the first deposited amorphous silicon layer. The layer stack is then subjected to a thermal treatment that generates a selectively heavily doped surface region where the metallization is to be applied.”)

333. A POSITA would understand that this full contact coverage over the heavily doped surface region enables charge carriers to primarily follow vertical

transport paths with reduced lateral movement, while dopant diffusion from the heavily doped layer into the substrate establishes continuous vertical current pathways extending from the electrodes through to the substrate. In other words, this configuration inherently reduces unnecessary lateral current paths, thereby effectively shortening the charge carrier flow paths between the substrate and the electrodes.

2. Claim 2: “The method of claim 1, further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.”

334. Rana teaches or suggests this limitation.

335. The '074 patent describes that the antireflective layer may be silicon nitride. *See* '074 patent, 8:61-64, (“102: Antireflection film, refractive index in the range of $1.4 < n < 3$; thickness < 150 nm. Examples include silicon nitride, silicon carbide, silicon oxide, titanium oxide, transparent conductive oxides.”) Rana discloses the application of silicon nitride on a heavily doped amorphous silicon layer. *See* Rana, [0031] (“it may be advantageous to deposit a passivation layer, for example SiN, over the heavily doped phosphorous layer...”), *see also* Rana, [0032], [0048], and [0051]. A POSITA would understand that while Rana describes the silicon nitride layer as a passivation layer, it does not only provide passivation but also offers excellent anti-reflection properties, as exemplified in the '074 patent.

336. Moreover, it was well known that forming an antireflective layer on the light entering side of a solar cell reduces the light losses due to reduction of light lost due to reflection. *See* Neville, 121 (“It is common practice to apply antireflection coatings to the optically absorbing surface of solar cells as a means of reducing energy losses due to reflection of photons.”) *See also* Neville, Figure IV.1, IV.2. *See also* Markvart, FIG. 8 (depicting the drastic reduction of the reflection coefficient when an antireflective layer is used). It was also well known that silicon nitride is a very good antireflective layer.

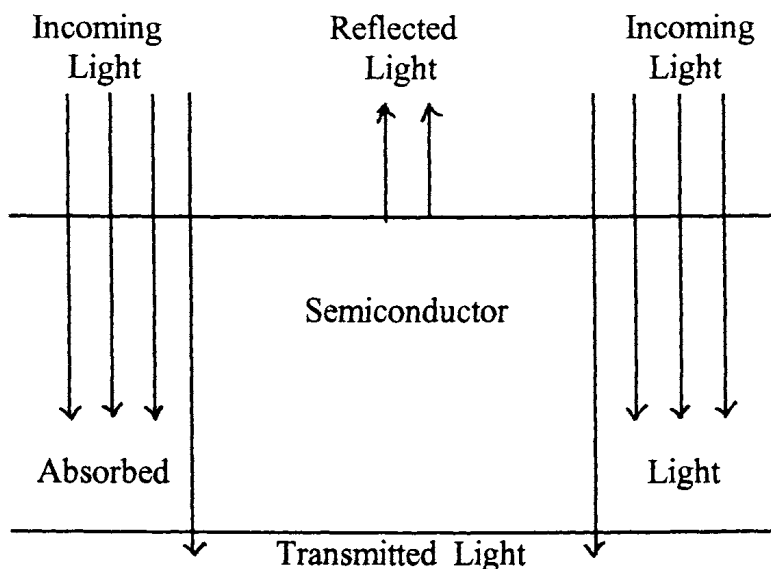


Figure IV.1. A vertically illuminated semiconductor illustrating the incoming light, the reflected light, the light absorbed in the semiconductor and the light passing through the semiconductor.

Neville, FIG. IV.1.

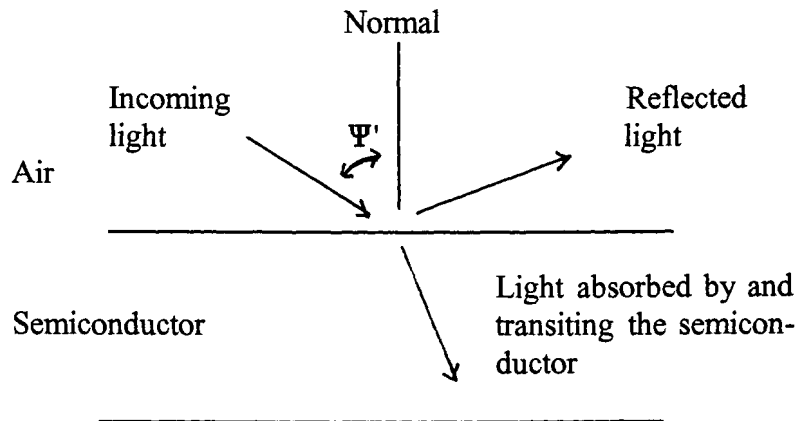


Figure IV.2. Light incident on a semiconductor at other than normal incidence.

Neville, FIG. IV.2.

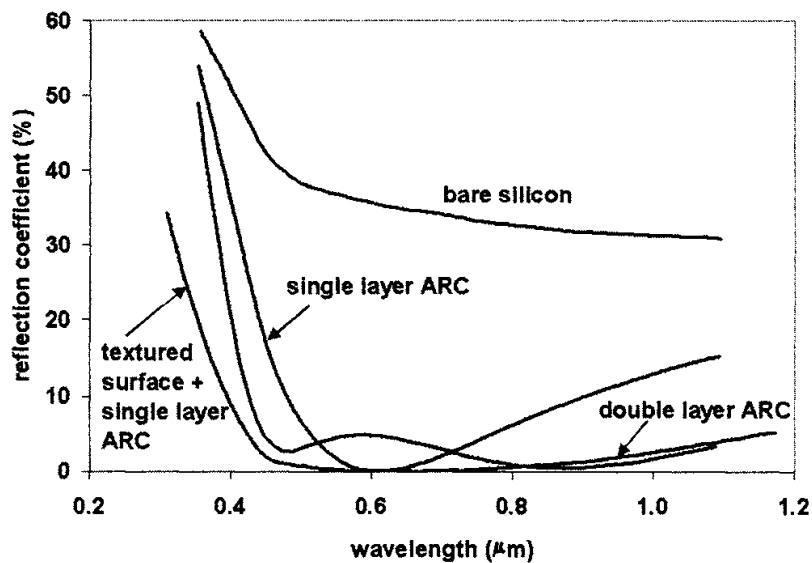
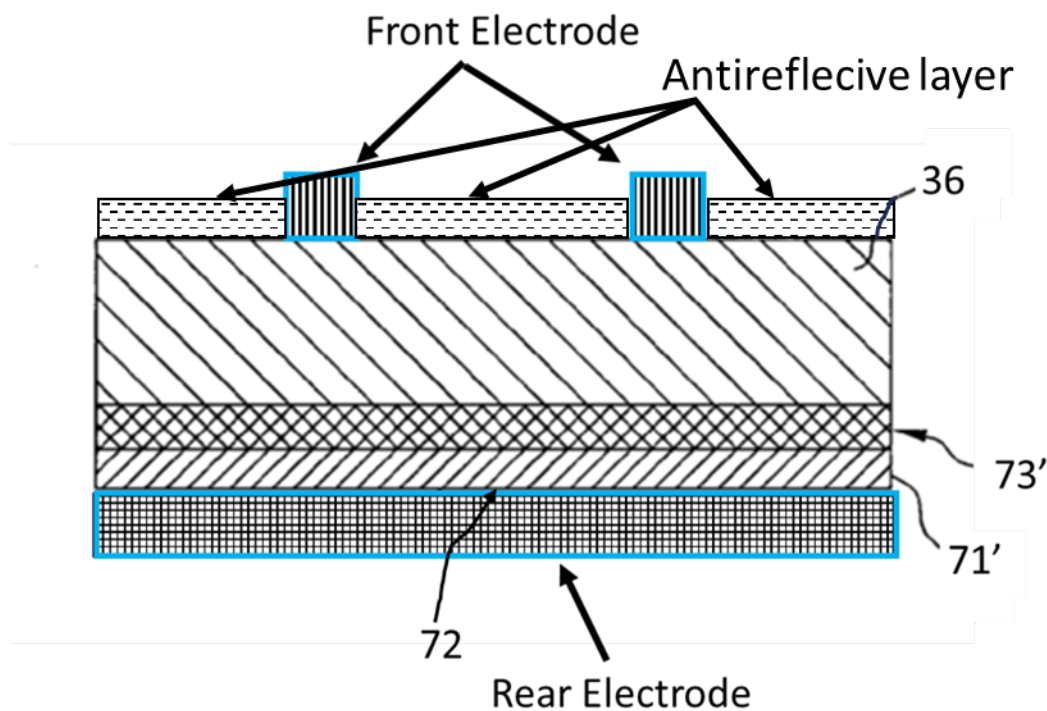


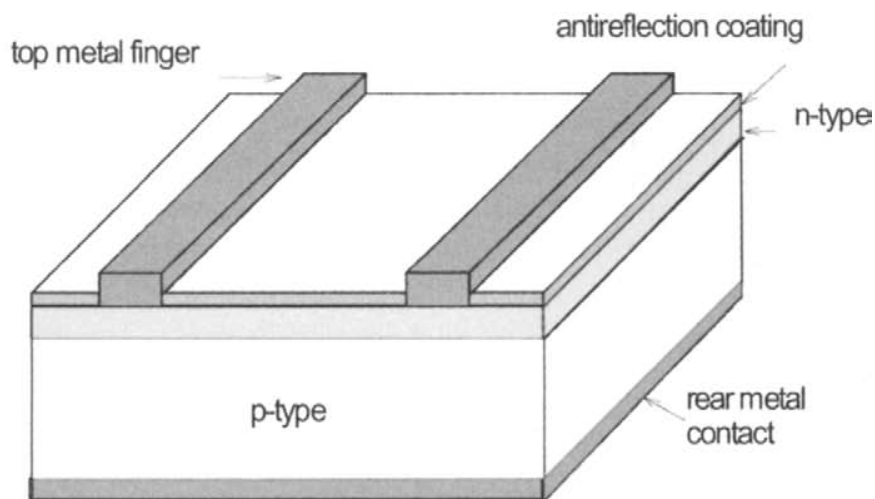
Figure 8 The reflection coefficient from polished bare silicon, and from a polished silicon surface covered with a single and double layer antireflection coating (after [31, 33]). The reflection coefficient for a textured surface is also shown.

Markvart, FIG. 8.

337. A POSITA would understand that a silicon nitride layer disclosed by Rana as passivation, serves a dual purpose when applied on Rana's solar cell structure discussed above for claim 1, i.e. as a surface passivation layer and an antireflective layer. Moreover, a POSITA would also understand that the "patterning processes" disclosed by Rana for forming the front contacts include a patterning step for removing the antireflective coating from the areas where a front electrode makes contact with the semiconductor silicon, as shown in the annotated Fig. 4c of Rana below. *See* Rana, [0045] ("additional processes such as metallization or patterning processes may be included to provide the front and rear contacts for a solar cell.") Rana's solar cell structure depicted below in the annotated Fig. 4c, i.e. a solar cell that has a patterned antireflective layer formed on the front or light entering side of the solar cell was well known. *See* e.g., Green, FIG. 2a.



Rana, FIG. 4c (annotated).



Green, FIG. 2a.

338. Rana also discloses forming a good internal mirror on a back of the solar cell. Rana discloses that “additional processes such as metallization or patterning

processes may be included to provide the front and rear contacts for a solar cell.” Rana, [0045]. Rana’s disclosed “rear contact for a solar cell” forms *a good internal mirror on a back of the solar cell* as explained below. As discussed in Section VIII.D.1.f, Rana discloses a rear electrode that covers the entire rear side of the solar cell.. A POSITA would understand that the metallization layer on the back side, as disclosed in Rana, is an aluminum electrode used in Borden. *See e.g., Borden, FIG. 2.* As discussed in Section V, it was well known that aluminum has a high reflectance, greater than 90% for wavelengths greater than 900 nm or 0.9 μm . The ’074 patent defines “a good internal mirror in the back” as a material that has a “high reflectivity for photons of more than 900 nm wavelength.” ’074 patent, 7:51-53, 12:8-9, 18:25-26. Additionally, the ’074 patent defines “a low reflective index layer for a good internal mirror on the back” as a layer with a “refractive index basically smaller than 3.0, smaller than 2.6, smaller than 2.0, smaller than 1.5.” ’074 patent, 15:31-35. It was well known that aluminum has a refractive index less than 3.0.

3. Claim 3: “The method of claim 1,”

339. Rana teaches or suggests this limitation.

340. See discussion of claim 1.

- a) **Limitation 3[a]: “wherein the depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer comprises depositing an amorphous silicon-containing compound over the substrate”**

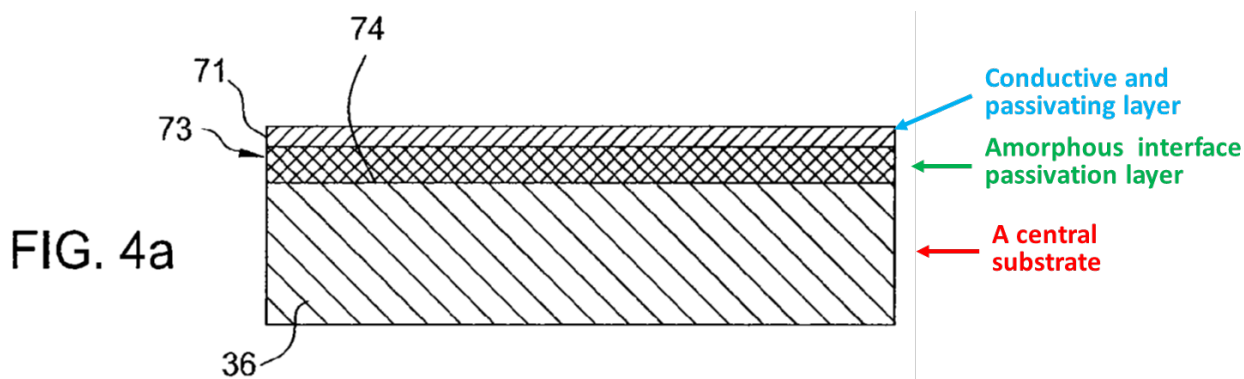
341. Rana teaches or suggests this limitation.

342. Rana discloses that both the amorphous silicon layer 73 (*interface passivation layer*) and the amorphous silicon layer 71 (*conductive and passivating layer*), depicted in FIG. 4a, are deposited by PECVD. Rana, [0024] (“The vacuum deposition chamber may be a PECVD chamber, either a stand-alone chamber or part of a multi-chamber processing system.”) *See also* Rana, [0025]-[0027].

343. Rana further discloses that “FIG. 2 is a schematic, cross-sectional representation of a plasma enhanced chemical vapor deposition (PECVD) chamber 3 that may be used in carrying out processes of the present invention...The chamber 30 as described herein is an AKTTM series PECVD chamber available from Applied Materials, Inc.” Rana, [0037]. *See also* Rana, [0038] (“To obtain the desired emitter dopant profile as illustrate in FIG. 1, steps 12 and 14, the plasma deposition within the chamber 30 generally continue for a period of time sufficient to deposit a first layer of amorphous silicon...Thereafter...to deposit a second layer of heavily doped amorphous silicon layer.”) Rana also discloses that the “silicon-containing compound may include silane gas (SiH_4)...for depositing a layer of amorphous silicon directly on the first surface of the crystalline silicon substrate.” Rana [0025]. Moreover, Rana

discloses that “[t]he mixture of precursors delivered to the deposition chamber may also include ...hydrogen gas (H₂).” Rana, [0026].

344. A POSITA would understand that the plasma deposition conditions disclosed by Rana for *depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer* (the two amorphous silicon layers 73 and 71), as depicted in FIG. 4a below, in the deposition chamber 30 shown in FIG.2 yield a material known as hydrogenated amorphous silicon, which is *an amorphous silicon-containing compound over the substrate* (element 36). See e.g., Fuhs, 124 (“Today hydrogenated amorphous silicon, a-Si:H, offers a mature material and device technology, used for solar cells, thin-film transistors, sensors, imaging, radiation detectors and displays.”) See also Fuhs, 126 (“The hydrogen content can vary widely with the deposition conditions (5-40%)...In optimized films, the hydrogen concentration amounts to 5-15%.”)



Rana, FIG. 4a (annotated).

345. The '074 patent lists PECVD deposited amorphous silicon materials as examples for the passivating interface layer and the electrically passivating interface layer. '074 patent, 5:56-60 (“64:Electrically passivating interface layer;... Examples include ...intrinsic amorphous silicon”); 5:42-51 (“63: Electrically passivating and conductive film...Examples include...n-type amorphous or polycrystalline silicon: phosphorus doped amorphous silicon”). Moreover the '074 patent lists as an example the PECVD method disclosed by Rana. '074 patent, 15:54-55 (“Most layers within the solar cell structure described above can be deposited or grown with methods such as PECVD), *see also* '074 patent, 15:66-16:3 (“a PECVD deposition can be done on one side of a wafer without the deposition on the other side. PECVD tools are available on an industrial scale but may only operate at temperature regimes where amorphous or microcrystalline silicon layers can be deposited.”) A POSITA would understand that all intrinsic amorphous silicon or phosphorus-doped amorphous silicon films deposited by PECVD are amorphous silicon containing compounds known as hydrogenated amorphous silicon.

- b) Limitation 3[b]: “and the providing thermal treatment of about 500°C. or higher separates the amorphous silicon-containing compound into the at least one interface passivation layer and the at least one conductive and passivating layer.”**

346. As I explained for limitation 3[a] above, a POSITA would understand that the deposition conditions disclosed by Rana to deposit the two amorphous silicon

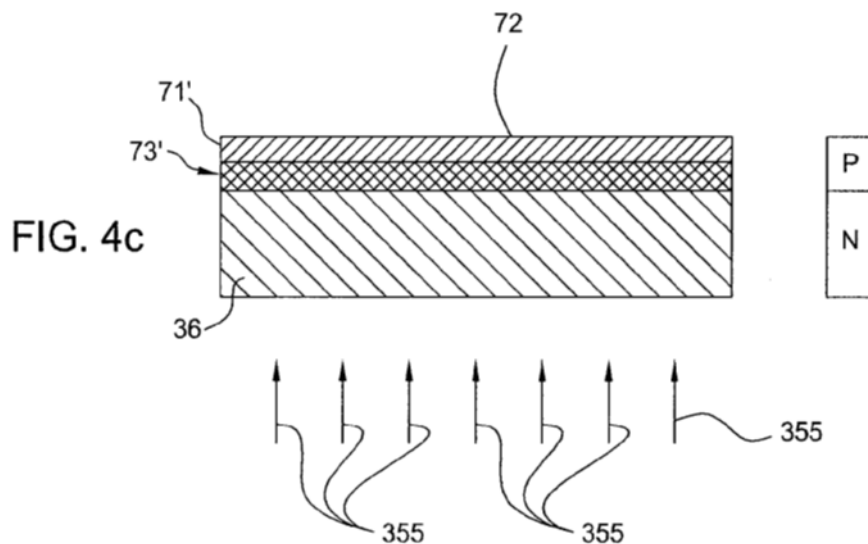
layers 73 and 71 as depicted in FIG. 4a, yield an amorphous silicon-containing compound known as hydrogenated amorphous silicon.

347. A POSITA would also understand that the thermal treatment will *separate the amorphous silicon-containing compound into at least one interface passivation layer* (the crystallized amorphous silicon layer 73 relabeled by Rana as element 73' in FIG. 4c) *and at least one conductive and passivating layer* (the crystallized amorphous silicon layer 71 relabeled by Rana as element 71' in FIG. 4c) for the following reasons.

348. It was well known that “[t]hemodynamically, amorphous silicon (a-Si) is in a metastable state... Heating above a temperature of about 500°C usually induces a transition into the thermodynamically more stable crystalline phase. The kinetics of solid phase crystallization (SPC) are characterized by nucleation and growth of crystal clusters at the expense of the surrounding amorphous material.” Fuhs, 125. Therefore, a POSITA would understand that during the thermal treatment disclosed by Rana, the following two phenomena occur.

349. First, the initially undoped amorphous silicon layer 73 (*interface passivation layer*) crystallizes by solid phase crystallization, which causes part of the amorphous silicon at the interface between amorphous silicon layer 73 and substrate 36 to crystallize epitaxially on the single-crystal substrate (“the p-type crystalline silicon substrate,” element 36). Rana, [0030] (“The application of the temperature

gradient causes the amorphous silicon layers to recrystallize, resulting in solid phase epitaxial growth that starts at the interface with the crystalline silicon substrate, and continuing outwardly to an outer surface of the amorphous silicon layers.”) Moreover, Rana discloses that after the thermal treatment the initially undoped or lightly doped “amorphous silicon layer 73” has the same grain structure as that of the underlying substrate and is denoted as layer 73’ (the *interface passivation layer*) in FIG. 4c, which is distinct from the layer 71’ the crystallized highly doped amorphous silicon layer (the *conductive and passivating layer*).



Rana, FIG. 4c.

350. Second, the initial highly doped amorphous silicon layer 71 (*one conductive and passivating layer*) crystallizes and is denoted as layer 71’ in Rana’s FIG 4c. A POSITA would also understand that layer 71 is not in direct contact with the substrate thus portions of it crystallize by random nucleation and growth resulting

in a different, i.e. polycrystalline, structure than the structure, i.e. epitaxial, of the crystallized layer 73'. Thus, a POSITA would understand that *the thermal treatment* would separate *the amorphous silicon-containing compound* into the *conductive and passivating layer* (the crystallized layer 71') and into the *interface passivation layer* (the crystallized layer 73').

351. Therefore, a POSITA would understand that Rana teaches a thermal treatment above 500°C (“by applying heat at about 750°C to about 1200°C”) that *separates the amorphous silicon-containing compound into the at least one interface passivation layer and the at least one conductive and passivating layer.*

4. Claim 4: “The method of claim 1, wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.”

352. Rana teaches or suggests this limitation or renders this limitation obvious.

353. Rana discloses that the thermal treatment step induces “solid phase epitaxial crystallization” of amorphous silicon layers, including the lightly doped amorphous silicon layer. *See, e.g., Rana, [0010]* (“heating the crystalline silicon substrate and the first and second amorphous silicon layers to a temperature sufficient to cause solid phase epitaxial crystallization of the first and second amorphous silicon layers, such that the first and second amorphous silicon layers, after heating, have the same grain structure and crystal orientation as the underlying crystalline silicon substrate.”)

354. A POSITA would know that such epitaxially crystallized regions may not be continuous laterally, as residual native oxide of silicon may prevent epitaxial crystallization in certain regions. Accordingly, the epitaxially crystallized regions, which result from the *thermal treatment* in the *interface passivation layer* (Rana's element 73 or 73'), form the *perforation* as carriers would transport through these regions since the carrier mobility is higher in such single crystal regions compared to the mobility in other regions in which the solid phase epitaxy was prevented by the presence of silicon's native oxide which grows easily upon exposure of silicon to air.

5. Claim 5: "The method of claim 1,"

355. Rana teaches or suggests this limitation.

356. See discussion of claim 1.

a) Limitation 5[a]: "wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and"

357. Rana teaches or suggests this limitation or renders this limitation obvious.

358. Rana discloses use of PECVD to deposit amorphous silicon layers, including the heavily doped amorphous silicon layer, on the substrate. *See* Rana, [0024] ("As is shown therein, there is provided at step 10 a p-type crystalline silicon substrate into a vacuum deposition chamber. The vacuum deposition chamber may be a PECVD chamber, either a stand-alone chamber or part of a multi-chamber processing system."), *see also* Rana, [0036], [0037]. A POSITA would understand that PECVD was a well-

established process to form such amorphous silicon at the time of Rana. As discussed in Section VIII.A.3.a, the PECVD process inherently forms hydrogenated amorphous silicon - an amorphous silicon-containing compound that also contains hydrogen.

b) Limitation 5[b]: “wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.”

359. Rana teaches or suggests this limitation.

360. Rana discloses the use of polycrystalline (also referred to as “multi-crystalline”) silicon as substrate. *See* Rana, [0024] (“The substrate may be formed of single crystalline silicon or multi-crystalline silicon depending on the particular application of the product to be produced.”) Rana further discloses that through solid phase epitaxial growth, the amorphous silicon layers—including the heavily doped amorphous silicon layer—will crystallize into the same crystal structure as the substrate. *See* Rana, [0010] (“heating the crystalline silicon substrate and the first and second amorphous silicon layers to a temperature sufficient to cause solid phase epitaxial crystallization of the first and second amorphous silicon layers, such that the first and second amorphous silicon layers, after heating, have the same grain structure and crystal orientation as the underlying crystalline silicon substrate.”)

361. A POSITA would understand that when the substrate is polycrystalline silicon and the solid phase epitaxial crystallization proceeds from the interface of Rana’s lightly doped amorphous silicon with the crystalline silicon substrate all the

way through the heavily doped amorphous silicon, then the later will crystallize into a heavily doped polycrystalline silicon film—i.e., having the same polycrystalline as the substrate—after completion of the solid-phase epitaxial growth. However, as discussed in Section VIII.A.1.c, it is difficult to eliminate silicon native oxide from the entire surface of a crystalline silicon substrate, thus in regions of the substrate surface covered with the native oxide solid phase epitaxial crystallization cannot occur and in these regions random nucleation and growth yields a polycrystalline structure. Moreover, the heavily doped amorphous silicon layer (the *conductive and passivation layer*) is not in direct contact with the crystalline substrate, thus a POSITA would understand that random nucleation within the heavily doped amorphous silicon layer will also result in regions that are polycrystalline after the crystallization is complete.

6. Claim 6: “The method of claim 1,”

362. Rana teaches or suggests this limitation.

363. See discussion of claim 1.

a) Limitation 6[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and”

364. Rana teaches or suggests this limitation, or renders this limitation obvious.

365. See discussion of limitation 5[a].

b) Limitation 6[b]: “wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer and increases the optical transmissivity.”

366. Rana teaches or suggests this limitation, or renders this limitation obvious.

367. Rana discloses that the doped polysilicon layer is initially amorphous silicon and is crystallized through thermal treatment. *See* Section VIII.D.1.e. A POSITA would understand that thermal treatment enhances optical transmission in polycrystalline silicon. *See* Sections VIII.A.5.b and VIII.B.5.b.

7. Claim 7: “The method of claim 1,”

368. Rana teaches or suggests this limitation.

369. *See* discussion of claim 1.

a) Limitation 7[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and”

370. Rana teaches or suggests this limitation.

371. *See* discussion of limitation 5[a].

b) Limitation 7[b]: “wherein the thermal treatment activates doping atoms in the compound.”

372. Rana teaches or suggests this limitation.

373. Rana discloses that thermal treatment (e.g., annealing) can simultaneously induce crystallization and activate phosphorus dopants. *See* Rana,

[0029] (“the annealing is accomplished in a manner which will cause the amorphous layer to directionally crystallize via a solid phase epitaxy process on the crystalline silicon substrate while at the same time achieving the desired activation of the phosphorous atoms and diffusing the phosphorous atoms into the silicon substrate to a desired distance.”), *see also* Rana, [0042], [0047]-[0049].

8. Claim 8: “The method of claim 1,”

374. Rana teaches or suggests this limitation.

375. See discussion of claim 1.

a) Limitation 8[a]: “wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound and”

376. Rana teaches or suggests this limitation.

377. See discussion of limitation 5[a].

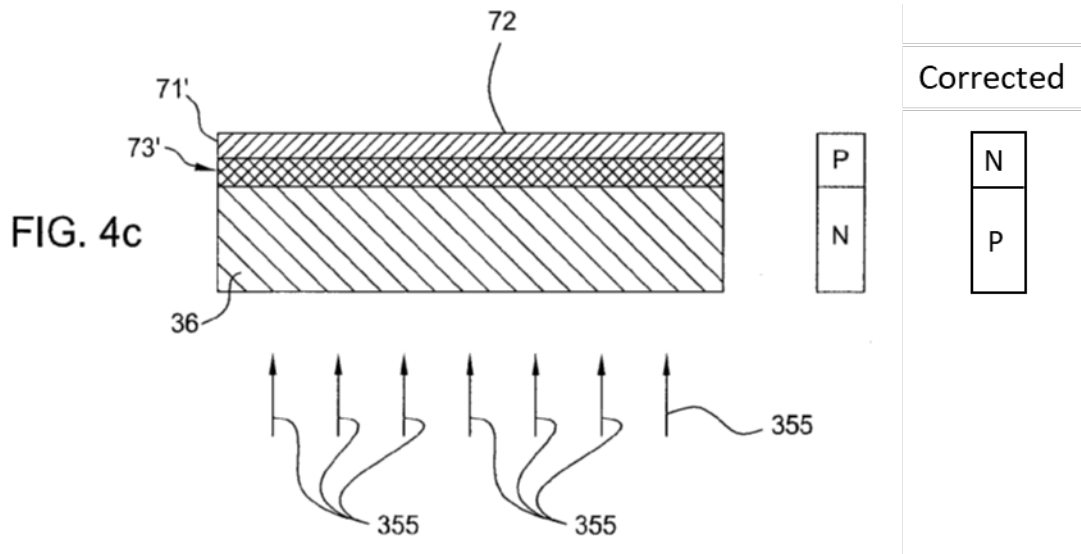
b) Limitation 8[b]: “wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.”

378. Rana teaches or suggests this limitation.

379. Rana discloses that during the crystallization of the amorphous silicon layers (including the heavily doped amorphous layer), phosphorus dopants diffuse into the substrate, thereby forming a p-n junction. *See* Rana, [0023] (“The amorphous silicon, when it is deposited on the crystalline silicon substrate, may, in accordance with one embodiment of the present invention, be doped with doping material of the

opposite conductivity type of the silicon substrate so as to provide a p-n junction when a doping material in the amorphous silicon has been diffused into the crystalline silicon substrate.”), *see also* Rana, [0030].

380. Rana also discloses that a p-n junction is formed when the n-type dopant, i.e., phosphorus, diffuses and forms a doped n-type region within the p-type doped crystalline silicon substrate, thus forming a p-n junction. *See* Rana, [0043] (“The resulting crystalline structure after heat treatment in the RTP chamber has a consistent grain structure, as shown in FIG. 4c...Upon the conversion of the amorphous silicon material, the lightly doped and heavily doped amorphous silicon layers 73, 71 as well as a region to which the phosphorous atoms from the lightly doped amorphous silicon layer is diffused will become a doped n-type region within the p-type single crystal silicon substrate 36 (i.e., **a p-n junction**), providing an emitter useful in a silicon solar cell.”) (Emphasis added). *See also* Rana, FIG. 4c, in which Rana provides a schematic of the p-n junction that is formed after the thermal anneal by the two differently doped materials the p-type doped substrate and the n-type doped polysilicon emitter layer. A POSITA would clearly understand that the schematic designation of the N and P regions were meant to be as shown in the corrected schematic in the annotated FIG. 4c below.



Rana, FIG. 4c (annotated).

IX. CONCLUSION

381. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on July 18, 2025


Miltiadis Hatalis

APPENDIX A: CV

Miltiadis K. Hatalis, Ph.D.

Professional Summary

Miltiadis (Miltos) Hatalis is a Professor in the Department of Electrical and Computer Engineering at Lehigh University. He received his B.S. degree in Physics from Aristotle University, Greece in 1982, the M.S. degree in Electrical Engineering from SUNY Buffalo in 1984, and the Ph.D. degree in Electrical Engineering from Carnegie Mellon University in 1987. He is teaching courses on semiconductor devices, electronic circuits, VLSI, computer engineering and photovoltaic energy systems. His research interests are on electronic materials, devices and circuits for VLSI, flat panel displays, photovoltaics, sensors, and integrated microsystems on a variety of rigid or flexible substrates including silicon, glass, metal foils, plastic, and paper. At Lehigh University, Prof Hatalis established a clean room facility for 150 mm substrates dedicated to the fabrication of ICs, sensors and flat panel displays and served as its Director for 25 years. Prof. Hatalis has received \$13.6 million of research funding and has been the Principal or Co-Principal Investigator of 41 research programs. Some of his group notable system demonstrations include flexible integrated circuits, flexible AMOLED displays, and large area sensor arrays for biometric and gas sensing applications. Prof. Hatalis has served as a consultant to several companies in the semiconductor and flat panel display fields and as an expert on patent litigation cases (on behalf of Samsung, LG, AMD, Applied Materials, etc.) including a testifying witness in an ITC case. As technical expert prepared 50 expert reports (30 related to IPRs) and was deposed 27 times. He is the author or co-author of over 180 technical publications including three issued patents related to driving of AMOLED displays, and two book chapters one on AMOLED pixel electronic circuits and one on polysilicon TFT technology. Prof. Hatalis has served as the PhD advisor of 20 completed PhD dissertations.

Expertise

- Electronic Materials & Micro/Nano Electronic Fabrication Processes
- Flat Panel Displays (TFTLCDs, AMOLEDs)
- Flexible Electronics and Photovoltaics
- Micro/Nano Electronic & Photonic Devices
- Sensor and Transducer Arrays
- Thin Film Transistor Technologies
- Integrated Circuits & VLSI

Education

Doctor of Philosophy (Ph.D.)	Electrical and Computer Engineering,	1987
	Carnegie Mellon University, Pittsburgh, PA USA	
Ph.D. Dissertation Title:	<i>“Crystallization of Amorphous Silicon Films and Application to Bipolar and Thin Film Transistors.”</i>	
Master of Science (M.S.)	Electrical and Computer Engineering,	1984
	State University of New York at Buffalo, NY, USA	
Bachelor of Science (B.S.)	Physics	1982
	Aristotle University of Thessaloniki, Greece	

Professional Experience

Academia

1995-today	Professor	Lehigh University, Bethlehem, PA Department Electrical & Computer Engineering
2003-2008	Professor	Aristotle University, Greece Department of Computer Science
1991-1995	Associate Professor	Lehigh University, Bethlehem, PA Department Electrical & Computer Engineering
1987-1991	Assistant Professor	Lehigh University, Bethlehem, PA Department Electrical & Computer Engineering

1993-today	Director	Display Research Laboratory Lehigh University
2010-2013	Interim Director	Sherman Fairchild Center for Solid State Studies Lehigh University
1988-1993	Associate Director	Microelectronics Research Laboratory Lehigh University

Industry

1987-2015 Independent Consultant

▪ Air Products	▪ IBM	▪ Next Biometrics
▪ Alcoa	▪ Intevac	▪ Sharp Labs of America
▪ Corning	▪ Kodak	▪ Spire
▪ Diamonex	▪ Litton Systems Canada	▪ Sterling Diagnostics
▪ Dow Corning	▪ Motorola Solutions	▪ Versatilis
▪ eMagin		

1992 Visiting Scientist XEROX Palo Alto Research Laboratory

Courses Taught

▪ Principles of Electrical Engineering	▪ Electronic Circuits
▪ Introduction to Computer Engineering	▪ Electronic Circuits Laboratory
▪ Physics of Semiconductor Devices	▪ Introduction to VLSI Circuits
▪ Microelectronics Technology	▪ VLSI Design
▪ Photovoltaic Energy Systems	▪ Solar Cells

Expert Engagements for Patent Litigation Cases

Total Court Appearances: 1 (Testified at an International Trade Commission (ITC) trial)
Total Expert Reports: 50 (IPR related Reports: 30)
Total Depositions: 27
Favorable Case Rulings: 5 (ITC: 1 / District Courts: 2 / PTAB: 2)

30) O'Melveny & Meyers, LLP
Case Name: BeSang Inc. v. Micron Technology Inc.
Services Provided: Engaged as Expert for Micron. I had a limited involvement.
Date: 2023.

29) Covington & Burling, LLP
Case Name: Samsung Displays v. BOE, ITC Inv. No. 337-TA-1351
Services Provided: Engaged as Expert for Samsung. I had a limited involvement.
Date: 2023

28) O'Melveny & Meyers, LLP
Case Name: Samsung Electronics v. Polaris
Services Provided: Engaged as Expert for Samsung. Prepare 1 expert report in support of a request to USPTO for Inter Parties Review of one patent and 1 expert report in support of *Ex Parte* Reexamination of one patent.
Date: 2022-2023

27) Nelson Bumgardner Albritton, PC
Case Name: Vista Peak Ventures v. Hisense, 21-cv-260, 21-cv-262, 21-cv-263, Federal District Court, Eastern District of Texas.
Services Provided: Engaged as Expert for Vista Peak Ventures. Prepared 1 expert report for claim construction.
Disposition: Case settled
Date: 2023

26) O'Melveny & Meyers, LLP
Case Name: Lynk Labs, Inc. v. Samsung Electronics Co., 1:21-cv-05126 (N.D.Ill.)
Services Provided: Engaged as Expert for Samsung. Prepared 1 expert report related to a motion for a summary judgment. I was deposed for this report.
Disposition: Case on stay pending outcomes of IPRs
Date: 2022

25) Axinn, Veltrop & Harkrider, LLP
Case Name: Ocean Semiconductors LLC v. Applied Materials, Inc.
Services Provided: Engaged as Expert for Applied. Prepared 2 expert reports in support of requests to USPTO for Inter Parties Review of two patents and deposed for one of these reports. One IPR was instituted.
Disposition: PTAB invalidated all claims asserted in the IPR.
Date: 2021-2022

M. K. Hatalis, Ph.D.

24) Covington & Burling, LLP
Case Name: Bishop Display LLC v. Samsung, Case No. 2:21-cv-00136-JRG (E.D. Tex.)
Services Provided: Engaged as Expert for Samsung. Prepared 2 expert reports in support of requests to USPTO for Inter Parties Review of two patents.
Disposition: Case settled
Date: 2021

23) O'Melveny & Meyers, LLP
Case Name: Solas OLED Ltd. v. Samsung (Civil Action No. 3:14-CV-00757)
Services Provided: Engaged as Expert for Samsung. Prepared 2 expert reports in support of requests to USPTO for Inter Parties Review of two patents. One IPR was instituted.
Disposition: Case settled
Date: 2021

22) Nelson Bumgardner Albritton, PC
Case Name: Vista Peak Ventures v. HannStar Display, Case Nos. 2:20-CV-00250-JRG; -00251-JRG; 00252-JRG.
Services Provided: Engaged as Expert for Vista Peak Ventures. Prepared 1 expert report for claim construction and was deposed for this report.
Disposition: Case settled
Date: 2021

21) Latham & Watkins, LLP
Case Name: Seoul Semiconductor v. Satco Products, IPR2021-00230
Services Provided: Limited engagement as Expert for Seoul. Prepared 1 expert report to USPTO on behalf of Seoul.
Date: 2021

20) O'Melveny & Meyers, LLP
Case Name: Monterey Research v. AMD, Case No. 1:19-cv-02149 (D. Del.)
Services Provided: Engaged as Expert for AMD. Prepared 1 expert report in support of a request to USPTO for Inter Parties Review of a patent and 1 Reply report. I was deposed 2 times.
Disposition: PTAB invalidated all claims asserted in the IPR.
Date: 2020-2021

19) Covington & Burling, LLP
Case Name: JOLED Inc. v. Samsung, Case No. 6:20-CV-00559 (WDTX)
Services Provided: Engaged as Expert for Samsung. Prepared 1 expert report for a request to USPTO for Inter Parties Review and 1 expert report for claim construction.
Disposition: Case settled
Date: 2020-2021

M. K. Hatalis, Ph.D.

- 18)** Latham & Watkins, LLP
Case Name: Solas OLED Ltd. v. LG Display,
Services Provided: Engaged as Expert for LG. Prepared 4 expert reports in support of requests to USPTO for Inter Parties Review of three patents. Deposed 2 times.
Disposition: Case settled
Date: 2019-2020
- 17)** K&L Gates, LLP
Case Name: Sharp. v. Visio et. al, CASE NO. 8:20-cv-00490
Services Provided: Engaged as Expert for Sharp. Prepared 1 expert report for claim construction.
Disposition: Case settled.
Date: 2020
- 16)** Bragalone Conroy, PC
Case Name: Vista Peak Ventures v. JDI, Case Nos. 2:19-cv-00323,-324,-325 (E.D. Tex.)
Services Provided: Engaged as Expert for Vista Peak Ventures. Prepared 1 expert report for claim construction.
Disposition: Case settled
Date: 2020
- 15)** Bragalone Conroy, PC
Case Name: Vista Peak Ventures v. AU Optronics, C.A. No. 2:18-cv-00276 (E.D. Tex.)
Services Provided: Engaged as Expert for Vista Peak. Prepared 1 expert report for claim construction.
Disposition: Case settled
Date: 2019
- 14)** O'Melveny & Meyers, LLP
Case Name: MediaTek v. Advanced Micro Devices, Inc., CA No.19-368-CFC (D. Del.)
Services Provided: Engaged as Expert for AMD. Search and analysis of relevant prior-art.
Disposition: Case settled
Date: 2019
- 13)** O'Melveny & Meyers, LLP
Case Name: Tessera v. Samsung Electronics, et al. ITC No. 337-3262
Invensas v. Samsung Electronics, et al. Civil Action No. 2:17-cv-670
Services Provided: Engaged as Expert for Samsung. Prepared 6 expert reports and deposed for 1 report, in support of requests to USPTO for Inter Parties Review of 5 patents.
Disposition: Case settled prior to USPTO making a decision
Date: 2017 – 2018

M. K. Hatalis, Ph.D.

12) Covington & Burling, LLP
Case Name: MiiCs & Partners America, et al. v. Toshiba, et al. Samsung Electronics Co., (Civil Action No. 1:14-cv-00803-RGA),
MiiCs & Partners America, et al. v. Funai, et al. Samsung Electronics Co., (Civil Action No. 1:14-cv-00804-RGA)
Services Provided: Engaged as Expert for Samsung on three patents. Prepared 3 Invalidity, 3 Rebuttal (Non-infringement) and 3 Reply Expert Reports. Also developed non-infringing alternatives for low damages. Deposed for all 9 reports.
Disposition: Judge ruled in favor of defendant's MSJ on non-infringement for two of the patents. Plaintiffs agreed to dismiss the case for the third patent.
Date: 2016-2017

11) Hogan Lovells, LLP
Case Name: Round Rock Research v. Ricoh Corporation, Case No. 1:15-CV-00157-SLR
Services Provided: Engaged as Expert for Ricoh. Prepared 2 expert reports in support of requests to USPTO for Inter Parties Review of two patents.
Disposition: Case settled prior to USPTO making a decision.
Date: 2016

10) O'Melveny & Meyers, LLP
Case Name: Samsung Electronics Co., v. NVIDIA, Case No. 3:14-CV-00757
Services Provided: Engaged as Expert for Samsung. I had a limited involvement.
Disposition: Undisclosed
Date: 2014 – 2015

9) Covington & Burling, LLP
Case Name: The Penn State Research Foundation v. Samsung, (Civil Action No. 4:14-CV-00124-MWB (M.D.Pa))
Services Provided: Engaged as Expert for Samsung on one patent. Performed invalidity analysis and provided non-infringement contentions.
Disposition: Complainant withdrew the complaint.
Date: 2014

8) Jeffer Mangels Butler & Mitchell, LLP
Case Name: SEL v. Innolux
Services Provided: Engaged as Expert for Innolux on five patents. Prepared 7 expert reports in support of requests to USPTO for Inter Partes Review of five different patents; all IPRs were instituted. I was deposed 7 times.
Disposition: Case settled prior to USPTO making a final decision.
Date: 2012-2013

7) Cozen O' Connor, LLP
Case Name: EIDOS Display v. AUO, et. al., Civil Action No. 6:11-CV-201-LED-JDL
Services Provided: Engaged as Expert for Innolux. I had a limited involvement.
Disposition: Undisclosed
Date: 2013

M. K. Hatalis, Ph.D.

- 6) O'Melveny & Meyers, LLP
Case Name: AUO v. Samsung, (Civil Action No. 3:09-CV-00001-BBC)
Services Provided: Engaged as Expert for Samsung. I had a limited involvement.
Disposition: Undisclosed
Date: 2011
- 5) White & Case, LLP
Case Name: Thomson v. CMI, (ITC Investigat. No. 337-TA-741 & No. 337-TA-749)
Services Provided: Engaged as Expert for CMI. Prepared 1 non-infringement and 1 invalidity expert reports. I was deposed 3 times. I testified in the ITC trial.
Disposition: Judge ruled in favor of CMI. Ruling explicitly cited my invalidity report.
Date: 2011
- 4) O'Melveny & Meyers, LLP
Case Name: SEL v. Samsung, (Civil Action No. 3:09-CV-00001-BBC)
Services Provided: Engaged as Expert for Samsung
Date: 2009
- 3) Irell & Manella, LLP
Case Name: LG v. CMO, (Civil Actions No.06-726 (JJF) & 07-357 (JJF))
Services Provided: Engaged as Expert for CMO. I had a limited involvement.
Disposition: Undisclosed
Date: 2008
- 2) Howrey, LLP
Case Name: SEL v. CMO, (Case No. C 04-04675 MH)
Services Provided: Engaged as Expert for CMO. I prepared 1 non-infringement expert report. I was deposed for that report.
Disposition: Judge ruled in favor of defendant's MSJ on non-infringement.
Date: 2007
- 1) Morrison & Foerster
Case Name: SEL v. Sanyo
Services Provided: Engaged as Expert for Sanyo. I had a limited involvement.
Disposition: Undisclosed
Date: 2001

Professional Affiliations and Involvement in Professional Societies

Affiliations: IEEE Electron Device Society, Society for Information Display (SID)

Editorships:

- “Flat Panel Display Materials II,” Materials Research Society Symposium Proceedings vol. 424, Published by the Materials Research Society, 1997.
- “Proceedings of the Second International Workshop on Active Matrix Liquid Crystal Displays,” Published by the IEEE Society, 1996

Chairman of the organization committee for the following workshops/conferences:

- International Workshop on Active Matrix Displays
 - It was sponsored by the Society of Information Display in co-operation with IEEE Electron Devices Society. It was held during the International Display Research Conference in Toronto, Canada, on September 20-23, 1997. There were 9 invited papers and 120 attendees.
- Flat Panel Display Materials II
 - Meeting held during Spring 1996 Meeting of the Materials Research Society. During the three day Symposium a total of 118 papers were presented. Prof. Hatalis was responsible for selecting the co-organizers, raising financial support, prepare the technical program and edit Symposium Proceedings.
- Second International Workshop on Active Matrix Liquid Crystal Displays
 - It was organized in co-operation with Society for Information Displays and the IEEE Electron Devices Society. It was held at Lehigh University on September 25-26, 1995. There were 11 invited and 25 contributed papers and 130 attendees.
- First International Workshop on Active Matrix Liquid Crystal Displays
 - Workshop sponsored by the Society of Information Display in co-operation with IEEE Electron Devices Society. It was held during the International Display Research Conference in Monterey CA, on October 10-13, 1994. There were 10 invited and 22 contributed papers and 170 attendees.
- Active Matrix Liquid Crystal Displays Symposium
 - It was organized in co-operation with Society for Information Display and IEEE Electron Devices Society. It was held at Lehigh University, on October 21-22, 1993. Seven invited and 35 contributed papers were presented. Attendance was 160.

Member of the organization committee for the following workshops/conferences:

- Active Matrix Liquid Crystal Displays Technology and Applications
 - Sponsored by the International Society for Optical Engineering (SPIE). USA, 1997
- Sixth International Conference on Polycrystalline Semiconductors
 - Conference was held in FRANCE, 2000
- Flat Panel Display Technology II
 - Sponsored by the International Society for Optical Engineering (SPIE). USA, 2001
- EURO-CVD Conference
 - Sponsored by the European Materials Research Society GREECE, 2001
- International Workshop on Active Matrix Liquid Crystal Displays
 - Sponsored by the Japan Society of Applied Physics, JAPAN: 1999, 2000, 2001, 2002, 2003, 2004, 2005, 2006
- IEEE Photonics Conference 2013
 - Member of the committee for Displays and Lighting Sessions

Patents & Publications

Total Citations 4,829 as of 6/20/2025 according to Google Scholar. H-index of 30

Patent	<u>Date</u>	<u>Description</u>
US Patent 8,390,536	March 5, 2013	Active Matrix Display and Method
Korean Patent No. 10-2009-7014517	November 2014	Active Matrix Display and Method
Japanese Patent 6043044	November 18, 2016	Active Matrix Display and Method

Book Chapters

1. "Technology of Polysilicon Thin Film Transistors." A. T. Voutsas and M. K. Hatalis. Chapter 4 in the book "Thin Film Transistors" edited by C. Kagan and P. Andy. Published by Marcel Dekker, Inc. 2003.
2. "AMOLED Display Pixel Electronics." M. Troccoli, M. K. Hatalis, A. T. Voutsas, Chapter 10, in the book "Organic Electroluminescence" edited by Z. Kafafi and H. Murata. Published by CRC Press & SPIE Press, 2005, p. 355.

Journal Papers

1. "High Performance Thin Film Transistors in Low Temperature Crystallized Amorphous Silicon Films" IEEE Electron Device Letters, vol. EDL-8, pp. 361-364, 1987. M. K. Hatalis and D. W. Greve.
2. "Solid Phase Epitaxy of LPCVD Amorphous Silicon Films." Journal of the Electrochemical Society, vol. 134, pp. 2536-2540, 1987. M.K. Hatalis and D.W. Greve.
3. "Large Grain Polycrystalline Silicon by Low Temperature Annealing of LPCVD Amorphous Silicon Films." Journal of Applied Physics, vol. 63, pp. 2260-2266, 1988. M.K. Hatalis and D.W. Greve.
4. "Interfacial Oxide, Grain Size and Hydrogen Passivation Effects on Polysilicon Emitter Transistors," IEEE Transactions on Electron Devices, vol. ED-35, pp. 1334-1343, 1988. P.A. Potyraj, D.L. Chen, M.K. Hatalis, and D.W. Greve.
5. "Minimum Detectable Solute Concentration by Atomic - Resolution TEM." Acta Crystallographica A, vol. A44, pp. 449-461, 1988. J.M. Howe, D.P. Basile, N. Prabhu, and M.K. Hatalis.
6. "Low Temperature Polycrystalline Silicon Thin Film Transistors for Displays" IEEE Transactions on Electron Devices, vol. ED-35, pp. 1842-1845, 1988. B.C. Hseih, M.K. Hatalis and D.W. Greve.
7. "Alternate Surface Cleaning Approaches for UHV/CVD Epitaxy of Si and Ge_xSi_{1-x}." Journal of the Electrochemical Society, vol. 138, pp. 3783-3789, 1991. M. Racanelli, D.W. Greve, M. K. Hatalis and L. J. van IJzendoorn.
8. "Investigations on Quality of Polysilicon Film-Gate Dielectric Interface in Polysilicon Thin Film Transistors." Thin Solid Films, vol. 216, pp. 137-141, 1992. J.-H. Kung, M. K. Hatalis and J. Kanicki.
9. "Flourine-Enhanced Oxidation of Polycrystalline Silicon and Application to Thin Film Transistor Fabrication" Applied Physics Letters, vol. 61, pp. 937-939, 1992. D. N. Kouvatsos, M. K. Hatalis and R. J. Jaccodine.

10. "Structure of as-Deposited LPCVD Silicon Films at Low Deposition Temperatures and Pressures." *Journal of the Electrochemical Society*, vol. 139, pp. 2659-2665, 1992. A. T. Voutsas and M. K. Hatalis.
11. "Surface Treatment Effect on the Grain Size and Surface Roughness of as Deposited LPCVD Silicon Films." *Journal of the Electrochemical Society*, vol. 140, pp. 282-288, 1993. A. T. Voutsas and M. K. Hatalis.
12. "Deposition and Crystallization of a-Si Low Pressure Chemically Vapor Deposited Films Obtained by Low-Temperature Pyrolysis of Disilane." *Journal of the Electrochemical Society*, vol. 140, pp. 871-877, 1993. A. T. Voutsas and M. K. Hatalis.
13. "Crystallized Mixed-Phase Silicon Films for Thin Film Transistors on Glass Substrates." *Applied Physics Letters*, vol. 63, pp. 1546-1548, 1993. A.T. Voutsas and M.K. Hatalis.
14. "Properties of the Cadmium Selenide Thin Films as a Function of Lateral Distance from Chromium Contacts," *Journal of the Electrochemical Society*, vol. 140, pp. 2994-2998, 1993. D. Waechter, M. R. Westcott, F. Lin, and M. K. Hatalis.
15. "Structural Characteristics of as-Deposited and Crystallized Mixed-Phase Silicon Films." *Journal of Electronic Materials*, vol. 23, pp. 319-330, 1994. A. T. Voutsas and M. K. Hatalis.
16. "Experimental and Theoretical Study on the Crystallization of Chemically Vapor Deposited Mixed-Phase Silicon Films," *Journal of Applied Physics*, vol. 76, pp. 777-790, 1994. A. T. Voutsas and M. K. Hatalis.
17. "Characterization of Cobalt Annealed on Silicon-Germanium Epilayers." *Thin Solid Films*, vol. 250, pp. 20-25, 1994. F. Lin, G. Sarcona, M. K. Hatalis, A. Cherhati, E. Austin and D. W. Greve.
18. "Raman Spectroscopy of Amorphous and Microcrystalline Silicon Films Deposited by Low Pressure Chemical Vapor Deposition" *Journal of Applied Physics*, vol. 78, pp. 6999 - 7005, 1995. A. T. Voutsas, M. K. Hatalis, J. Boyce and A. Chiang.
19. "High performance thin film transistors in large grain size polysilicon deposited by thermal decomposition of disilane," *IEEE Transactions on Electron Devices*, vol. 43, pp. 1399 - 1406, 1996. D. N. Kouvatsos, A. T. Voutsas, and M. K. Hatalis.
20. "Leakage current mechanism in submicron polysilicon thin film transistors" *IEEE Transactions on Electron Devices*, vol. 43, pp. 1218 - 1223, 1996. K. Olasupo and M. K. Hatalis.
21. "The effect of drain offset on current-voltage characteristics in sub-micron polysilicon thin film transistors," *IEEE Transactions Electron Devices*, vol. 43, pp. 1306-1308, 1996. K. Olasupo, W. Yarbrough and M. K. Hatalis.
22. "Single crystal silicon thin film transistors fabricated at low process temperatures on glass substrates" *Electronics Letters*, vol. 32, pp. 775 - 777, 1996. N. Kouvatsos, D. Tsoukalas, G. T. Sarcona, M. K. Hatalis and J. Stoemenos.
23. "Polycrystalline silicon thin film transistors fabricated at reduced thermal budgets by utilizing fluorinated gate oxidation." *IEEE Transactions on Electron Devices*, vol. 43, pp. 1448 - 1453, 1996. D. N. Kouvatsos and M. K. Hatalis.
24. "Nickel Silicides Grown on Amorphous Silicon and Silicon-Germanium Thin Films." *Electrochemical and Solid State Letters*, vol. 1, p. 233-234, 1998. G. Sarcona, S. K. Saha, and M. K. Hatalis.
25. "Non-Erratic Behavior of Overerased Bits in Flash EEPROM" *Journal of Vacuum Science and Technology B*, vol. 16, p 3065-3068, 1998. F. Nkansah, E. Prinz, and M. K. Hatalis.
26. "Thin Film Transistors in Low Temperature As-deposited and Reduced Crystallization-Time Polysilicon on 665 C Strain Point Glass Substrates." *Thin Solid Films*, vol. 338, pp. 281-285, 1999. M. K. Hatalis, D. N. Kouvatsos, J. H. Kung, A. T. Voutsas, and J. Kanicki.

27. "Silicidation Reactions with Co – Ni Bilayers for Low Thermal Budget Microelectronic Applications." *Thin Solid Films*, vol. 347, pp. 278-283, 1999. S. K. Saha, R. S. Howell, and M. K. Hatalis.
28. "Effect of Flash EEPROM Floating Gate Morphology on Electrical Behavior of Fast Programming Bits." *IEEE Transaction on Electron Devices*, vol. 46, pp. 1355- 1362, 1999. F. Nkansah and M. K. Hatalis.
29. "Polysilicon Thin Film Transistors using Self-Aligned Cobalt and Nickel Silicide Source and Drain contacts" *IEEE Electron Device Letters*, vol. 20, pp. 332-334, 1999. G. Sarcona, M. Stewart, and M. K. Hatalis.
30. "Elimination of Hillock Formation in Al Interconnects Using Ni or Co" *Journal of Applied Physics*, vol. 86, pp. 625-633, 1999. S. K. Saha, R. S. Howell, and M. K. Hatalis.
31. "Reaction Mechanisms in Al-ITO Ohmic Contact Metallization with Co and Ni Barrier Layers for Active Matrix Display Applications." *Journal of Electrochemical Society*, vol. 146, pp. 3134-3138, 1999. S. K. Saha, R. S. Howell, and M. K. Hatalis.
32. "Polycrystalline Silicon Thin Film Transistors in Various Solid Phase Crystallized Films Deposited on Glass Substrates" *Journal of Electronic Materials*, vol. 28, pp. 19-25, 1999. D. N. Kouvatsos, A. T. Voutsas, and M. K. Hatalis.
33. "Preparation and Stability of Low Temperature Cobalt and Nickel Silicides on Thin Polysilicon Films." *Journal of Vacuum Science and Technology A*, vol. 18, pp. 97- 93, 2000. R. S. Howell, G. Sarcona, and M. K. Hatalis.
34. "Poly-Si Thin Film Transistors on Steel Substrates" *IEEE Electron Device Letters*, vol. 21, pp. 70-72, 2000. R. S. Howell, M. Stewart, S. V. Karnik, S. K. Saha, and M. K. Hatalis.
35. "High Performance Gated Lateral Polysilicon PIN Diodes," *Solid State Electronics*, vol. 44, pp.1613-1619, 2000. M. Stewart and M. K. Hatalis.
36. "Characterization and Modeling of Fast Programming Bits in Flash EEPROM" *Solid State Electronics*, vol. 44, pp. 1887-1897, 2000. F. Nkansah, M. K. Hatalis and K. Olasupo.
37. "Polysilicon TFT Technology for Active Matrix OLED Display," *IEEE Transaction on Electron Devices*, vol. 48, pp. 845-851, 2001. M. Stewart, R. S. Howell, L. Pires, and M. K. Hatalis.
38. "Novel Cleaning Methodology for Steel Substrates in Microelectronic Fabrication." *Journal of Electrochemical Society*, vol. 149, pp. G143-G146, 2002. R. S. Howell and M. K. Hatalis.
39. "Trade Off Between Polysilicon Film Quality and Thin Film Transistor Operational Amplifier DC Gain." *Solid State Electronics*, vol. 46/9, pp. 1421-1425, 2002. T. Afentakis and M. K. Hatalis.
40. "A Simple Analytical Model for the Dependence of the Propagation Delay of the Polycrystalline Silicon CMOS Inverter on Temperature" *Solid State Electronics*, vol. 46/12, pp. 2301-2306, 2002 T. Afentakis and M. K. Hatalis.
41. "Palladium based Micro-Membrane for Water Gas Shift Reaction and Hydrogen Gas Separation." *J. of Microelectromechanical Systems*, vol. 12, pp.: 93- 100, 2003. S. V. Karnik, M. K. Hatalis, M. V. Kothare.
42. "Implementations of Rapid Thermal Processes in Polysilicon TFT Fabrication." Accepted for Publication by Elsevier for a Special Volume on Rapid Thermal Processing for Future Semiconductor Devices M. K. Hatalis and A. T. Voutsas.
43. "Lateral Polysilicon p⁺-p-n⁺ and p⁺-n-n⁺ Diodes." *Solid State Electronics*, Vol. 47, pp. 653-659, 2003 S. V. Karnik and M. K. Hatalis.
44. "Multiple Lateral Polysilicon Diodes as Temperature Sensors for Chemical Microreaction Systems," *Japanese Journal of Applied Physics (JJAP)*, vol. 42, pp.1200-1205, 2003. S.V. Karnik and M. K. Hatalis.

45. "Macroelectronics: Perspectives on Technology and Applications," Proceedings of IEEE, vol. 93, pp.1239-1256, 2005. R. H. Reuss, et.al. (M. Hatalis).
46. "Polysilicon TFT Circuits on Flexible Stainless Steel Foils," Solid State Electronics, vol. 50, pp 1080-1087, 2006. M. Troccoli, A. J. Roudbari, T. Chuang, M. Hatalis.
47. "Exciton dissociation by a static electric field followed by nanoscale charge transport in PPV polymer films," Phys. Rev. B (Condensed Matter and Materials Physics), vol. 73, p. 125202, 2006. H. Najafov, I. Biaggio, Ta-Ko. Chuang, M. K. Hatalis.
48. "Design and fabrication of high-performance polycrystalline silicon thin-film transistor circuits on flexible steel foils" IEEE Transactions on Electron Devices, v 53, p 815-22, 2006. T. Afentakis, M. Hatalis, A. Voutsas and J. Hartzell.
49. "Water Gas Shift Reaction in a Glass Microreactor," Catalysis Today, vol. 120, p.107–120, 2007. S. Mukherjee, M. K. Hatalis, and M. V. Kothare.
50. "Top-emitting 230 dots/in. Active-Matrix Polymer Light-Emitting Diode Displays on Flexible Metal Foil Substrates," Applied Physics Letters 90, 151114 (2007). T.-K. Chuang, M. Troccoli, P.-C Kuo, A. Jamshidi, M. K. Hatalis; I. Biaggio; A. T. Voutsas.
51. "Polysilicon TFT technology on Flexible Metal Foils for AM-PLED displays," Invited paper: Journal of Society for Information Displays, 15, 455 (2007). T.-K. Chuang, M. Troccoli, M. K. Hatalis, and A. T. Voutsas.
52. "Process Technology for High-Resolution AM-PLED Displays on Flexible Metal Foil Substrates," Electrochemical and Solid-State Letters, 10, J92 (2007). T.-K. Chuang, M. Troccoli, P.-C Kuo, A. Jamshidi, M. K. Hatalis, A. T. Voutsas, and T. Afentakis.
53. "Effect of mechanical strain on mobility of polycrystalline silicon thin-film transistors fabricated on stainless steel foil." Applied Physics Letters, 91, 243507 (2007). Po-Chin Kuo, Abbas Jamshidi-Roudbari and Miltiadis Hatalis.
54. "High Voltage, Moderate Current Thin Film Transistor for Actuator Applications," ECS Trans., vol. 11, pp: 31-39, 2008. A. Jamshidi-Roudbari, P.C. Kuo, and M. Hatalis.
55. "Luminescence of Intraporous Cerium(III) Complexes in Alkyl Sulfonic Mesoporous." Chemistry of Materials, vol. 20, pp. 1359-1366, 2008. Klier, K., Miller, A., Zhang, L., Hatalis, M.
56. "Tactile displays: Overview and recent advances." Displays, Vol. 29, pg. 185-194, 2008. V. G. Chouvardas, A. N. Miliou, M. K. Hatalis.
57. "Crystallization of amorphous silicon thin films: comparison between experimental and computer simulation results." Journal of Materials Science, Vol. 43, pg. 3976- 3981, 2008 J. Kioseoglou, P. Komninou, G. P. Dimitrakopoulos, I. P. Antoniadis, M. K. Hatalis and T. Karakostas.
58. "Effect of mechanical strain on laser crystallized polysilicon thin film transistors and ring oscillators fabricated on stainless steel foil." Solid-State Electronics vol. 52, pg.1594-1601, 2008. Abbas Jamshidi-Roudbari, Po-Chin Kuo, Miltiadis Hatalis.
59. "Electronic Structure of CeF₃ and TbF₃ by valence-band XPS and theory." Journal of Physics and Chemistry of Solids, vol. 70, pg. 1302-1311, 2009. K. Klier, P. Novak, A.C. Miller, J.A. Spirko and M.K. Hatalis.
60. "Effects of Mechanical Strain on Characteristics of Polycrystalline Silicon Thin Film Transistors Fabricated on Stainless Steel Foil." IEEE Journal of Display. Technology, vol. 5, pg. 202-205, 2009. Po-Chin Kuo, Abbas Jamshidi-Roudbari, and Miltiadis Hatalis.
61. "Electrical characteristics and mechanical limitation of polycrystalline silicon thin film transistor on steel foil under strain" Journal of Applied Physics, vol. 106, 114502 (2009). Po-Chin Kuo, Abbas Jamshidi-Roudbari and Miltiadis Hatalis.
62. "A Flash Analog to Digital Converter on Stainless Steel Foil" Solid-State Electronics, vol. 54, pg. 410-416, 2010. A. Jamshidi-Roudbari, P.C. Kuo, and M. Hatalis.

63. "High Frequency Half-Bit Shift Register with Amorphous Oxide TFT." *IEEE Electron Device Letters*, vol. 31, pg. 320-322, 2010. A. Jamshidi-Roudbari, S. A. Khan, and M. K. Hatalis.
64. "Integrated Full-Bit Shift Register by Low-Temperature Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors." *Electrochemical and Solid State Letters*, vol. 14, pg. J19-J21, 2011. Abbas Jamshidi-Roudbari, Shahrukh Akbar Khan, and Miltiadis K. Hatalis.
65. "Voltage Noise Characteristics of Polysilicon P-I-N Diodes." *IEEE Transactions on Electron Devices*, vol. 58, pg. 1054-1062, 2011. A. Jamshidi-Roudbari and M. K. Hatalis.
66. "Amorphous oxide Thin Film Transistors with Methyl Siloxane Based Gate Dielectric on Paper Substrate." *Electrochemical and Solid State Letters*, vol. 14, pg. H247-H249, 2011. Nackbong Choi, Shahrukh Khan, and Miltiadis K. Hatalis.
67. "Origin of low-frequency noise in the low drain current range of bottom-gate amorphous IGZO thin-film transistors." *IEEE Electron Device Letters*, vol. 32, pg. 898-900, 2011. C. G. Theodorou, A. Tsormpatzoglou, C. Dimitriadis, S. Khan, M. K. Hatalis, J. Jomaah, G. Ghibaudo.
68. "A modified offset roll printing for thin film transistor applications." *Microelectronics Engineering*, vol. 91, pp. 93-97, 2012. N. Choi, H. Wee, S. Nam, J. Lavelle, and M. K. Hatalis.
69. "Interface diffusion characteristics of Al-2 at.%Nd/n + a-Si:H and Al-2 at.%Nd/n + poly-Si bilayers." *Thin Solid Films*, vol. 520, pp. 1982-1987, 2012. Nackbong Choi, Soo-Young Yoon, Chang-Dong Kim, and Miltiadis Hatalis.
70. "Comparative Study of Active-Over-Metal and Metal-Over-Active Amorphous IGZO Thin-Film Transistors with Low Frequency Noise Measurements." *IEEE Electron Device Letters*, vol. 33, pp. 555-557, 2012. Andreas Tsormpatzoglou, Nikolaos A. Hastas, Shahrukh Khan, Charalabos A. Dimitriadis, Miltiadis Hatalis.
71. "Design and simulation of a tactile display based on a CMUT array." *International Journal of Electronics*, vol. 99, pp. 1351-1363, 2012. V. Chouvardas, M. Hatalis and A. N. Miliou.
72. "Optimizing the design of a tactile display based on a capacitive micromachined ultrasonic transducer array." *International Journal of Numerical Modelling: Electronic Networks, Devices and Field*, vol. 26, pp. 448-456, 2013. V. G. Chouvardas, M. K. Hatalis and A. N. Miliou.
73. "Characterization of High Current Stress Induced Instability in Amorphous InGaZnO Thin Film Transistors by Low Frequency Noise Measurements" *IEEE Electron Device Letters*, vol. 34, pp. 1403-1405, 2013. A. Tsormpatzoglou, N. Hastas, F. Mahmoudabadi, N. Choi, M. K. Hatalis and C. A. Dimitriadis.
74. "Analytical surface-potential-based drain current model for amorphous InGaZnO thin film transistors." *Journal of Applied Physics*, vol. 114, 184502, 2013. A. Tsormpatzoglou, N. Hastas, N. Choi, F. Mahmoudabadi, M. K. Hatalis and C. A. Dimitriadis.
75. "Amorphous IGZO TFTs and circuits on conformable aluminum substrates." *Solid State Electronics*, vol. 101, p 57-62, 2014. F. Mahmoudabadi, X. Ma, M. K. Hatalis, K. Shah and T. L. Leventusky.
76. "Novel analog feedback current programming architecture compatible with 2- transistor 1-capacitor pixel for active matrix organic light-emitting diode displays." *Journal of the Society for Information Display*, vol. 22, p 204-215, 2014. Thomas Charisoulis, Matias N. Troccoli, Douglas R. Frey, Miltiadis K. Hatalis.
77. "Current feedback compensation circuit for 2T1C LED displays: Method." *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, p 2423-2433, 2015. Thomas Charisoulis, Douglas R. Frey, Miltiadis K. Hatalis.
78. "Current Feedback Compensation circuit for 2T1C LED displays: Analysis and Evaluation." *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, p. 175-188, 2019. Thomas Charisoulis, Collin Reiman, Douglas R. Frey, Miltiadis K. Hatalis.

Refereed Conference Papers

1. "Solid Phase Epitaxy of LPCVD Silicon Films and Their Use as Diffusion Sources." The Electrochemical Society Extended Abstracts, Vol. 86-1, Spring 1986. M. K. Hatalis and D. W. Greve.
2. "TEM Studies of the Amorphous / Crystalline Transition in Silicon and Applications to Electronic Devices." Institute Physics Conference Series, vol. 87, pp. 479-484, 1987 D.W. Greve and M. K. Hatalis.
3. "Crystallization of Amorphous LPCVD Silicon Films and Application to Bipolar and Thin Film Transistors." Materials Research Society Symposium Proceedings, vol. 106, pp. 335-340, 1987 M. K. Hatalis and D. W. Greve.
4. "Thin Film Transistors in Low Temperature Crystallized Amorphous Silicon Films." The Electrochemical Society Extended Abstracts, Vol. 87-1, Spring 1987. M. K. Hatalis and D. W. Greve.
5. "Minimum Detectable Solute Concentration and Accuracy of Compositional Analysis in Atomic-Resolution Microscopy." Proceedings Microbeam Analysis Society, 22nd Annual Mtg., Hawaii, Summer 1987 J. M. Howe, D. P. Basile, N. Prabhu and M. K. Hatalis.
6. "Electrical Characteristics of Polysilicon Thin Film Transistors at Low Temperatures." Proceedings International Topical Conference on Hydrogenated Amorphous Silicon Devices and Technology 1988 M. K. Hatalis and N. Stylianou.
7. "Effect of Annealing on Grain Size of Undoped and Indium Doped CdSe Thin Films." The Electrochemical Society Extended Abstracts, Vol. 89-1, Spring 1989 M. K. Hatalis and M. R. Westcott.
8. "Structural and Electrical Characterization of CdSe Thin Films." Materials Research Society Symposium Proceedings, vol. 164, pp. 87-92, 1990 M. K. Hatalis, F. Lin and M. Westcott.
9. "Effect of Gate Dielectric on Performance of Polysilicon Thin Film Transistors." Materials Research Society Symposium Proceedings, vol. 182, pp. 357-362, 1990 M. K. Hatalis, J. H. Kung, J. Kanicki and A. Bright.
10. "Hydrogenation of Polycrystalline Silicon Thin Film Transistors." The Electrochemical Society Extended Abstracts, Vol. 91-1, Abstract 410, pp. 629-630, spring 1991 M. K. Hatalis, J. H. Kung and J. Kanicki.
11. "Effect of Temperature and Pressure on the Structure of LPCVD Polysilicon Films." The Electrochemical Society Extended Abstracts, Vol. 91-1, Abstract 416, pp. 639-640, Spring 1991 A. Voutsas and M. K. Hatalis.
12. "Nucleation and Crystallization of Amorphous Silicon-Aluminum Thin Films" Materials Research Society Symposium Proceedings, vol. 230, pp. 195-200, 1992 F. Lin, M. K. Hatalis, S. Girginoudi, D. Girginoudi, N. Georgoulas and A. Thanailakis.
13. "A Simple Polysilicon TFT Structure for Achieving High On/Off Current Ratio Independent upon Gate Bias," International Conference on Solid State Devices and Materials, Japan, Fall 1992. J. Kanicki and M. K. Hatalis.
14. "Thin Silicon Dioxide Films Grown at Very Low Oxygen Partial Pressure in Oxygen Diluted by Helium," The Electrochemical Society Extended Abstracts, Vol. 92-2, Fall 1992 D. N. Kouvatsos and M. K. Hatalis.
15. "Polysilicon TFTs with various 800°C Thermally Grown Gate Oxides" The Electrochemical Society Extended Abstracts, Vol. 92-2, Fall 1992 J.-H. Kung, D. N. Kouvatsos and M. K. Hatalis.
16. "Properties of cadmium selenide thin films as a function of lateral distance from chromium contacts (TFT)," The Electrochemical Society Proceedings of the 1st Symposium on Thin Film Transistor Technologies," p. 235, 1992 D. Waechter, F. Lin, M. K. Hatalis.

17. "Hydrogenation effects on polysilicon thin-film transistor structures" 50th Annual Device Research Conference, IEEE Transactions on Electron Devices, vol. 39, p. 2665, 1992. M. K. Hatalis, J. H. Kung, and J. Kanicki.
18. "Deposition and Characterization of Crystallized LPCVD Si-films Obtained by Low Temperature Pyrolysis of Disilane," The Electrochemical Society Extended Abstracts, Vol. 92-1, Spring 1992. A. T. Voutsas and M. K. Hatalis.
19. "Crystallization of Tin-Implanted Amorphous Silicon Thin Films," Materials Research Society Symposium Proceedings, vol. 279, pp. 553-558, 1993 F. Lin and M. K. Hatalis.
20. "A New Quantitative Roughness Measurement and its Application in the Polysilicon/Silicon Dioxide Interface." Materials Research Society Symposium Proceedings, vol. 280, pp. 285-288, 1993 S. Lin and M. K. Hatalis.
21. "Electrical and Structural Properties of Cobalt Annealed on Silicon-Germanium Epilayers," Materials Research Society Symposium Proceedings, vol. 281, pp. 647- 652, 1993 G. Sarcona, F. Lin, M. K. Hatalis, A. F. Cherhati, E. Austin, and D. W. Greve.
22. "Performance of Polycrystalline Silicon Thin Film Transistors with Double Layer Gate Dielectric," Materials Research Society Symposium Proceedings, vol. 284, pp. 431-436, 1993 J. H. Kung, M. K. Hatalis and J. Kanicki.
23. "Fluorinated Silicon Dioxide Films as Gate Dielectrics of Polysilicon Thin Film Transistors," Materials Research Society Symposium Proceedings," vol. 284, pp. 437-442, 1993 D. N. Kouvatsos, J. H. Kung, M. K. Hatalis and J. Kanicki.
24. "A Novel Low-Temperature LPCVD Process for Deposition of Polysilicon Films on Glass Substrates," The Electrochemical Society Proceedings, 12th International Conference on CVD, Honolulu, Hawaii, May 1993 A. T. Voutsas and M. K. Hatalis.
25. "Low Temperature Polysilicon Thin Film Transistors on Corning Code 1734 and 1735 Glass Substrates." Society for Information Displays International Symposium Digest, vol. 24, 1993 M. K. Hatalis, D. N. Kouvatsos, J.-H. Kung, A. T. Voutsas, F. P. Fehlner, and J. Kanicki.
26. "Amorphous Silicon and Silicon-Germanium Thin-Film Transistors Formed by Ion Implantation," Materials Research Society Symposium Proceedings," vol. 297, pp. 907-912, 1993 G. T. Sarcona, M. K. Hatalis, and A. Catalano.
27. "Nucleation and Grain Growth in Silicon Films Deposited by Thermal Decomposition of Disilane" Materials Science Forum," vol. 126-128, pp. 431-434, 1993 Presented at the 6th International Conference on Intergranular and Interface Boundaries in Materials A. T. Voutsas and M. K. Hatalis.
28. "Rapid Thermal Crystallization of LPCVD Amorphous Silicon Films," Materials Research Society Symposium Proceedings, vol. 345, pp. 93-98, 1994 A. T. Voutsas, M. K. Hatalis, K. R. Olasupo, A. K. Nanda and D. Alugbin.
29. "Characteristics of Sub-Micron Polysilicon Thin film Transistors" Materials Research Society Symposium Proceedings, vol. 345, pp. 129-134, 1994. K. Olasupo, M. K. Hatalis.
30. "Polysilicon TFT Technology for High Functionality Active Matrix Liquid Crystal Displays," Proceedings of the 1994 IEEE Princeton/Central Jersey Sarnoff Symposium, INVITED PAPER M. K. Hatalis.
31. "Effect of Grain Size and Process Temperature on Distribution of Polysilicon TFT's Electrical Characteristics," M. K. Hatalis, D. Kouvatsos, S.-H. Lin, and A. T. Voutsas Conference Record of 14th Annual International Display Research Conference, pp. 150-153, 1994 published by Society for Information Displays.
32. "Analysis of Scanners for TFT-LCDs." D. L. Fleischer and M. K. Hatalis. Proceedings of Second International Workshop on Active Matrix Liquid Crystal Displays (AMLCDs '95), pp.76-79, 1995 published by IEEE.

33. "Materials and Device Aspects of Polysilicon TFT-LCD Technology." Proceedings of the Second International Display Workshops, vol. 2, pp. 3-6, 1995, (Japan) INVITED PAPER M. K. Hatalis.
34. "Improvement of ON/OFF Current Ratio of n-Channel Offset-Gate Polysilicon Thin Film Transistors by Cesium Ion Implantation into Passivation Layer." Su-Heng Lin and M. K. Hatalis. Proceedings of Second International Workshop on Active Matrix Liquid Crystal Displays (AMLCDs '95), pp.111-114, 1995 published by IEEE.
35. "Polysilicon TFT Active Layer Fabrication Processes." M. K. Hatalis. INVITED PAPER Presented at the "International Active Matrix Workshop" held with the Euro Display '96: "The 16th International Display Research Conference." (October 1996). Paper published in the Proceedings of 1996 International Active Matrix Workshop, pp. 21-24, 1996.
36. "Low Temperature Silicides for Polysilicon Thin Film Transistor Applications" Materials Research Society Symposium Proceedings, vol. 402, pp.191-196, 1996. G. Sarcona and M. K. Hatalis.
37. "Polysilicon Thin Film Transistors with Cobalt and Nickel Silicide Source and Drain Contacts" Materials Research Society Symposium Proceedings, vol. 424. pp. 159-164, 1997 G. Sarcona and M. K. Hatalis.
38. "Helical Resonator Plasma Oxidation of Amorphous Silicon for Flat Panel Display," Materials Research Society Symposium Proceedings, vol. 424. pp. 165- 170, 1997 S. Kaluri, R. Howell, M. K. Hatalis and D. W. Hess.
39. "Polysilicon TFT Active Matrix Organic EL Displays" SPIE Proceedings Series, vol. 3057, pp.277-286, 1997 M. K. Hatalis, M. Stewart, C. Tang, and J. Burtis.
40. "Silicides for Polysilicon TFT-LCD applications," SPIE Proceedings Series, vol. 3014, pp.141-146, 1997 R. S. Howell, M. J. Stewart, G. Sarcona, and M. K. Hatalis.
41. "Polysilicon TFTs for AMLCD Applications with Gate Oxides Grown in a low Temperature N₂O Plasma," SPIE Proceedings Series, vol. 3014, pp.170-175, 1997 R. S. Howell, S. R. Kaluri, M. K. Hatalis, and D. W. Hess.
42. "Low Thermal Budget Polysilicon Crystallization by Rapid Thermal Processing." Proceedings of 1997 International Display Research Conference, pp. L70 - L73, 1997 H. Hovagimian, J. Mehlhaff, M. Stewart, M. Hatalis, and S. Saha.
43. "Polysilicon VGA Active Matrix OLED Displays: Technology and Performance," IEEE Technical Digest of 1998 International Electron Device Meeting, p. 871- 874, 1998. M. Stewart, R. Howell, L. Pires, M. K. Hatalis, W. Howard, and O. Prache.
44. "Advanced Polysilicon TFT Technology for Active Matrix Flat Panel Displays," SPIE Conference Proceedings, vol. 3363, p. 278-287, 1998 M. K. Hatalis, M. Stewart, and R. Howell.
45. "Low Temperature PECVD Polysilicon Crystallization by Rapid Thermal Processing ," Materials Research Society Symposium Proceedings, vol. 508, p. 109- 114, 1998 M. Stewart, H. Hovagimian, J. Arakkal, S. Saha, and M. K. Hatalis.
46. "Cobalt and Nickel for Improved Aluminum-Indium Tin Oxide Contact Metallurgy in Polysilicon TFT Display Applications," Materials Research Society Symposium Proceedings, vol. 508, p.321-326, 1998 R. S. Howell, S. K. Saha, and M. K. Hatalis.
47. "Hillock Formation and Reduction Using metal Interlayers for Active Matrix Display Applications," Materials Research Society Symposium Proceedings, vol. 508, p. 333-338, 1998 S. K. Saha, R. S. Howell, and M. K. Hatalis.
48. "Thin film transistors fabricated at low thermal budgets in various types of polycrystalline silicon films on glass substrates," Electrochemical Society Meeting Abstracts, vol. 98-2, abstract No. 683, 1998 D. N. Kouvatsos, A. T. Voutsas and M. K. Hatalis.
49. "Solid phase crystallization of amorphous silicon by rapid thermal processing for flat panel display applications," The Electrochemical Society Proceedings of the 4th Symposium on Thin Film

M. K. Hatalis, Ph.D.

- Transistor Technologies, vol. 98-22, pp. 92-99, 1999 Miltiadis K. Hatalis, Mark Stewart and Howard Hovagimian.
50. "VGA Active Matrix OLED Displays Having the Single Polysilicon TFT Pixel Structure." SPIE Conference Proceedings, vol. 3636, pp. 22-31, 1999 M. K. Hatalis, M. Stewart, R. Howell, L. Pires, W. Howard, and O. Prache.
 51. "Low Temperature Flat Panel Display Driver Circuits in RTP Crystallized Polysilicon," Society for Information Display, SID 99 Digest, pp. 460-463, 1999 M. Stewart, T. Afentakis, G. Sarcona, and M. K. Hatalis.
 52. "AMOLEDs with Rapid Thermal Processed (RTP) Polysilicon TFTs," Proceedings of 1999 Vehicle Displays and Microsensors, pp. 87-93, 1999 M. K. Hatalis, R. S. Howell, and M. Stewart.
 53. "Polysilicon TFT Display Driver Circuits on Stainless Steel Foil Substrates," Society for Information Display, SID 2000 Digest, pp. 538-541, 2000. T. Afentakis, M. Stewart, R. Howell, and M. K. Hatalis.
 54. "Reliability of Polysilicon Thin Film Transistors on Stainless Steel Foil Substrates," SPIE Proceedings, vol. 4295A, pp. 108-112, 2001 T. Afentakis, R. Howell, and M. K. Hatalis.
 55. "Modeling and Performance of Polysilicon Thin Film Transistor Circuits on Stainless Steel Foil Substrates," SPIE Proceedings, vol. 4295A, pp. 95-101, 2001 T. Afentakis and M. K. Hatalis.
 56. "Novel multiple lateral Polysilicon p+-n-n+ and p+-p-n+ Diodes," SPIE Proceedings, vol. 4295A, 2001 S. V. Karnik, S. Alexander, W. Bruce Jr., and M. K. Hatalis.
 57. "The Temperature Dependence of Threshold Voltage and Mobility of Polysilicon TFTs on Flexible Stainless Steel Foil and Quartz Substrates." Proceedings of the International Semiconductor Device Research Symposium (ISDRS) 2001, pp. 89-92, 2001 T. Afentakis and M. K. Hatalis.
 58. "Polysilicon Diodes as Temperature Sensors for Chemical Microreaction Systems." Proceedings of the International Semiconductor Device Research Symposium (ISDRS) 2001, pp. 174-177, 2001 S. V. Karnik, H. X. Vo, M. K. Hatalis, M. V. Kothare.
 59. "Implementations of Rapid Thermal Processes in Polysilicon TFT Fabrication." Rapid Thermal Processing for Future Semiconductor Devices, published by Elsevier, pp. 37-47, 2003. M. K. Hatalis and A. T. Voutsas.
 60. "High Performance Polysilicon Circuits on Thin Metal Foils." Proceedings of the SPIE, Vol. 5004, pp. 122-126, 2003. T. Afentakis, M. Hatalis, T. Voutsas, J. Hartzell.
 61. "Polysilicon TFT AM-OLED on Thin Flexible Metal substrates," Proceedings of the SPIE, Vol. 5004, pp. 187-191, 2003. T. Afentakis, M. Hatalis, T. Voutsas, J. Hartzell.
 62. "High Performance Polysilicon Thin Film Transistor Circuits on Flexible Stainless Steel Foils." MRS Symposium Proceedings, Vol. 769, pp. 47-52, 2003. T. Afentakis, M. Hatalis.
 63. "AMOLED TFT Pixel Circuitry for Flexible Displays on Metal Foils." MRS Symposium Proceedings, Vol. 769, pp. 93-99, 2003. M. Troccoli, T. Afentakis, M. Hatalis, A. Voutsas, M. Adachi, J. Hartzell.
 64. T. Afentakis, M. Hatalis, T. Voutsas, J. Hartzell, "Display Driver Circuits Fabricated on Flexible Stainless Steel Foils," SID Digest, Vol. 37, pp. 15-18, 2004.
 65. "Active-Matrix Organic Light-Emitting Displays on Flexible Metal Foils," Proc. SPIE 5801 (2005), 234. Ta-Ko Chuang, et. al. (M. Hatalis).
 66. "Poly-Silicon TFT's on Metal Foil Substrates for Flexible Displays," IMID Digest 2005. M. Hatalis, M. Troccoli, T. Chuang, A. Jamshidi, G. Reed.
 67. Polysilicon TFT technology on metal foils for large area flexible electronics. International Semiconductor Device research symposium (ISDRS), 2005. M.K. Hatalis, M. Troccoli, TK Chuang, A Jamshidi, G. Reed.

68. "230 dpi AMPLD TFT VGA Display on Flexible Metal Foils with Integrated Row Drivers," Thin Film Transistor Technologies VIII, Electrochemical Society Meeting, Fall 2006. M. Troccoli, T.K. Chuang, A. Jamshidi, P.C. Kuo, J. Spirko, M. Hatalis, A. Voutsas, J. Hartzell.
69. "230 DPI High Resolution AMPLD Display on Flexible Metal Foils with Integrated Row Drivers," 26th IDRC, Session 9.5; 2006. Troccoli, M.N., Chuang, T.K., Roudbari, A.J., Chang, Y.L., Reed, G., Spirko, J., Hatalis, M.
70. "Process Technology for High-Resolution AM-PLD Displays on Flexible Metal Foil Substrates," ECS Transactions, Thin Film Transistor Technologies, v 3, pp 349 (2006). T.-K. Chuang, M. Troccoli, P.-C Kuo, A. Jamshidi, J. A. Spirko, M. K. Hatalis, K. Klier, I. Biaggio, A. T. Voutsas, T. Afentakis, and J. W. Hartzell.
71. "Effect of mechanical strain on mobility of poly-silicon thin film transistors fabricated on stainless steel foil." 2007 International Symposium on Flexible Electronics and Display, Taiwan. P.C. Kuo, A.J. Roudbari and M. K. Hatalis.
72. "High Voltage, Moderate Current Thin Film Transistor for Actuator Applications." Electro Chemical Society (ECS) Fall 2007 Meeting, USA. Abbas Jamshidi- Roudbari, Po-Chin Kuo, Miltiadis Hatalis.
73. "Strained Laser Crystallized Poly-Silicon Thin Film Transistors and Ring Oscillators Fabricated on Stainless Steel Foils." International Semiconductor Device Research Symposium (ISDRS) 200. A. J. Roudbari, P.C. Kuo, M. K. Hatalis.
74. "Mechanical Limitations of Materials for Steel Foil Based Flexible Electronics." Materials Research Society Proceedings, 2007 Fall Meeting. P.C. Kuo, V. Chouvardas, K.M. Hatalis, J. Spirko, M. Hatalis.
75. "Low Temperature ZnO TFTs and Circuits." Materials Research Society Proceedings, 2007 Fall Meeting. S. Khan, A. J. Roudbari, M. Hatalis.
76. "Modeling tactile information flow using ontologies." 3rd Balkan Conference in Informatics (BCI 07) 2, 219-228 (2007). E. Myrgioti, V.Chouvardas, A. Miliou and M. Hatalis.
77. "Electrical Response of Polycrystalline Silicon Thin Film Transistor on Steel Foil under Mechanical Strain." Materials Research Society, Fall 2008 Meeting, Boston. Po-Chin Kuo, Abbas Jamshidi- Roudbari and Miltiadis Hatalis.
78. "Metal Oxide-based (IZO and ZnO) TFTs for Flexible Electronics." Materials Research Society, Fall 2008 Meeting, Boston. Shahrukh A. Khan, Abbas Jamshidi- Roudbari, Miltiadis Hatalis.
79. "Top-Gate ZnO-based TFTs by RF Sputtering." Mater. Res. Soc. Symp. Proc. Vol. 1035, 1035-L11-32, 2008. Shahrukh A. Khan and Miltiadis Hatalis.
80. "Laser-Crystallized Polysilicon TFT Adder Cells on Flexible Metal Foil." Appeared in proceedings of International Semiconductor Device Research Symposium (ISDRS), Dec. 2009. A. Jamshidi- Roudbari, P.C. Kuo, and M. Hatalis.
81. "Electrical Characteristics and Mechanical limitation of polycrystalline silicon thin film transistor on steel foil under strain," Appeared in proceedings of International Semiconductor Device Research Symposium (ISDRS), Dec. 2009. P. C. Kuo, A. Jamshidi-Roudbari, and M. Hatalis.
82. "High performance IGZO TFTs on Steel: Device Stability and Circuit Integration." ISDRS 2009, 5378154, pp1-2. Shahrukh A. Khan and Miltiadis K. Hatalis.
83. "Metal Oxide-based (IZO and ZnO) TFTs for Flexible Electronics." Mater. Res. Soc. Symp. Proc. vol. 1109, 1109-B03-38, 2009. S. A. Khan and M. K. Hatalis.
84. "Effect of Uniaxial Tensile Strain on Electrical Performance of Amorphous IGZO TFTs and Circuits on Flexible Metal Foils." DRC 2010, 5551869, pp119-120. Shahrukh A. Khan, Po-Chin Kuo, Abbas Jamshidi-Roudbari and Miltiadis Hatalis.

85. "Reverse offset roll printing using high resolution flat printing plate for electronic application," Presentation in Electronic Materials Conference 2010, Notre Dame, IN, USA, Jun 2010. N. Choi, S. Khan, X. Ma, J. Lavelle, J. Gallagher and M. Hatalis.
86. "Amorphous IGZO TFTs and Circuits on Highly Flexible and Dimensionally Stable Kovar (Ni-Fe alloy) Metal Foils." Materials Research Society Symposium Proceedings, vol. 1287, p. 63-68, 2011. Shahrukh A. Khan, Xiaoxiao Ma and Miltiadis Hatalis.
87. "Fe-42%Ni austenitic alloy as a novel substrate for flexible electronics." Mater. Res. Soc. Symp. Proc., vol. 1285, p 6-12, 2011. X. Ma, S. Khan, M. Hatalis and M. Robinson.
88. "Electret field enhanced organic photovoltaics cells." Conference Record of the IEEE Photovoltaics Specialists Conference, p. 000719-000722, 2011. S. Khan, N. Choi, X. Ma, M.K. Hatalis, A. Jain and G. Powch.
89. "Design of a tactile display based on a high power CMUT array." 2012 16th Panhellenic Conference on Informatic, pp. 228-233. Vasilios G. Chouvardas, Amalia N. Miliou, and Miltiadis K. Hatalis.
90. "A new feedback current programming architecture for 2T1C AMOLED displays." Digest of Technical Papers - SID International Symposium, v 44, p 465-468, June 2013. Thomas Charisoulis, Matias N. Troccoli, Douglas R. Frey, and Miltiadis K. Hatalis.
91. "Feedback Architecture for Uniform Brightness in TFT AMOLED Displays." 2013. IEEE Photonics Conference, IPC 2013, p 182-183, 2013. Thomas Charisoulis, Matias N. Troccoli, Douglas R. Frey, and Miltiadis K. Hatalis.
92. "CNT Sensor arrays with P-i-N diode." IEEE SENSORS 2013 - Proceedings. Thomas Charisoulis, Abbas Jamshidi-Roudbari, Miltiadis Hatalis, Nack Bong Choi, Yijiang Lu, and Jing Li.
93. "IGZO TFTs on Aluminum Substrates." Presented to ISDRC 2013 Conference. Forough Mahmoudabadi, Xiaoxiao Ma, Miltiadis K. Hatalis, Kirit N. Shah and Thomas L. Levendusky.
94. "High Performance IGZO TFTs with Modified Etch Stop Structure on Glass Substrates." MRS Symposium Proceedings, v 1633, 2014, Oxide Semiconductors. Forough Mahmoudabadi, Ta-Ko Chuang, Jerry Kung and Miltiadis Hatalis.
95. "Parameter extraction methodology for amorphous IGZO thin film transistors." Proceedings of the International Conference on Microelectronics, ICM, p 235-238, 2014, 2014 29th International Conference on Microelectronics, MIEL 2014 – Proceedings. Tsormpatzoglou, A., Hastas, N.A., Hatalis, M.K., Dimitriadis, C.A.
96. "Analytical unified drain current model of amorphous IGZO thin film transistors considering a Gaussian distribution of tail states." Proceedings of the International Conference on Microelectronics, ICM, p 269-272, 2014, 2014 29th International Conference on Microelectronics, MIEL 2014 – Proceedings. Tsormpatzoglou, A.; Hastas, N.A.; Hatalis, M.K.; Dimitriadis, C.A.
97. "RF-sputtered oxide TFTs and circuits on engineered aluminum substrates." Digest of Technical Papers - SID International Symposium, v 45, n 1, p 1043-1046, 2014. Mahmoudabadi, Forough; Charisoulis, Thomas; Hsiang, Kuei-Cheng; Hatalis, Miltiadis; Shah, Kirit N.; Levendusky, Thomas L.
98. "Effect of strain on Characteristics of amorphous In-Ga-Zn-O TFTs fabricated on engineered aluminum substrates ." Digest of Technical Papers - SID International Symposium, v 46, n 1, p 1188-1191, 2015. Forough Mahmoudabadi, Miltiadis Hatalis, Kirit N. Shah, Thomas L. Levendusky

Research Funding

- Total number of research programs: 41
- Total budget: \$13,609,775

Principal Investigator:

1. Title: "Silicon Alloy Thin Films for Solar Cells and Displays"
Agent: State of Pennsylvania / Solarex Corp.
Amount: **\$45,000** Period: 9/88 – 8/89
2. Title: "Thin Film Transistor Studies"
Agent: IBM
Amount: **\$150,750** Period: 9/89 – 8/91
3. Title: "Low temperature Polycrystalline Films for Display Applications"
Agent: Litton Systems Canada Inc.
Amount: **\$58,000** Period: 1989, unrestricted duration
4. Title: "Polysilicon TFTs for Advanced Flat Panel Displays"
Agent: Defense Advanced Research Program Agency
Amount: **\$126,500** Period: 10/90 – 9/91
5. Title: "Development of Electronic Grade CVD Diamond"
Agent: State of Pennsylvania / Diamonex Inc.
Amount: **\$125,000** Period: 9/91 – 8/93
6. Title: "High Performance Polysilicon TFTs for Advanced Flat Panel Displays"
Agent: Defense Advanced Research Program Agency
Amount: **\$260,000** Period: 9/91 – 8/92
7. Title: "Advanced Materials and Devices for High Definition TFT-LCD Displays"
Agent: Defense Advanced Research Program Agency
Amount: **\$1,170,000** Period: 9/92 – 5/96
8. Title: AASERT Award I "Advanced Materials and Devices for High Definition TFT-LCD Displays"
Agent: Defense Advanced Research Program Agency
Amount: **\$216,600** Period: 9/94 – 8/97
9. Title: AASERT Award II "Advanced Materials and Devices for High Definition TFT-LCD Displays"
Agent: Defense Advanced Research Program Agency
Amount: **\$200,000** Period: 9/95 – 8/98

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10. Title: "Low Temperature Polysilicon TFTs in Advanced Display Technologies"
Agent: Defense Advanced Research Program Agency
Amount: **\$1,498,000** Period: 6/96 – 8/99
11. Title: "Acquisition of Advanced Equipment for Rapid Thermal and High Density Plasma Processing for Integrated Circuits and Flat Panel Displays"
Agent: National Science Foundation
Amount: **\$130,000** Period: 9/96 – 8/99
12. Title: "Polysilicon pin Diode Based Direct x-Ray Sensor Array for Application in Fluoroscopy and Radiography"
Agent: Sterling Diagnostic Inc.
Amount: **\$150,000** Period: 9/97 – 12/98
13. Title: "Flexible AMOLED Displays on Metal Foils."
Agent: Army Research Laboratory / Lehigh cooperative program
Amount: **\$1,190,000** Period: 9/03 – 4/05
14. Title: "Novel Active Matrix Organic LED Flexible Displays"
Agent: State of PA; Dept. of Community & Economic Development
Amount: **\$150,000** Period: 3/03 – 2/04
15. Title: "Coordinated Micro-Fabrication Support for COT Projects"
Agent: State of PA; Dept. of Community & Economic Development
Amount: **\$182,006** Period: 1/03 – 12/05
16. Title: "High Performance Microelectronics Systems for Antenna Applications"
Agent: DARPA, subcontract to Lehigh from Northrop Grumman
Amount: **\$1,078,024** Period: 6/04 – 12/07
17. Title: "Polysilicon Thin Film Devices for Sensor Applications"
Agent: Ben Franklin Technology Partners of State of PA
Amount: **\$300,000** Period: 7/05 – 6/07
18. Title: "Flexible VGA AMOLED & AMPLD Displays on Metal Foils"
Agent: Army Research Laboratory / Lehigh cooperative program
Amount: **\$1,747,168** Period: 4/05 – 5/08
19. Title: "Array Electronics for Multichannel Carbon Nanotube Gas Sensors"
Agent: NASA / Lehigh cooperative program
Amount: **\$114,076** Period: 6/06 – 6/08
20. Title: "Comparison of Different Metal Foils for Flexible Displays"
Agent: United States Display Consortium
Amount: **\$205,000** Period: 12/07 – 5/10

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21. Title: "Development of Active Matrix Arrays for Nanosensors"
Agent: NASA AMES / Homeland Security Department
Amount: **\$269,000** Period: 9/08 – 3/12
22. Title: "Crystalline Silicon Thin Films for Solar Cells"
Agent: State of PA
Amount: **\$55,000** Period: 6/09 – 5/10
23. Title: "SBIR Phase II - Electret Enhanced Organic Solar Cell"
Agent: Versatilis, LLC
Amount: **\$60,000** Period: 1/11 – 6/12
24. Title: "AMOLED Display Drivers"
Agent: The Technology Collaborative
Amount: **\$72,081** Period: 4/11 – 3/12
25. Title: "Research Gift Grant"
Agent: Sharp Laboratories of America Inc.
Amount: **\$100,000** Period: 3/12 – no end date
26. Title: "Effect of Glass Substrates on IGZO TFTs"
Agent: Corning Inc.
Amount: **\$379,000** Period: 4/12 – 6/14
27. Title: "Research Gift Grant"
Agent: Robert Bosch LLC, Research and Technology Center.
Amount: **\$40,000** Received: May 2012
28. Title: "Research Gift Grant"
Agent: Air Products and Chemicals, Inc.
Amount: **\$90,000** Received: September 2012
29. Title: "Research Gift Grant"
Agent: Qualcomm, Inc.
Amount: **\$120,000** Received: January 2013
30. Title: "Research Gift Grant"
Agent: Alcoa, Inc.
Amount: **\$70,750** Received: March 2013
31. Title: "SBIR Phase I - Hybrid Projectile Components Miniaturization"
Agent: Custom Electronics, Inc.
Amount: **\$32,000** Period: 6/15 – 12/15
32. Title: "Research Gift Grant"
Agent: Corning, Inc.
Amount: **\$65,000** Received: June 2015

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33. Title: "EAGER: Plasmonic Transparent Electrodes for Organic Photovoltaics"
Agent: National Science Foundation
Amount: **\$80,000** Period: 7/15 – 6/16
34. Title: "SBIR Phase II - Hybrid Projectile Components Miniaturization"
Agent: Custom Electronics, Inc.
Amount: **\$200,820** Period: 8/16 – 7/18

Co-Principal Investigator:

1. Title: "Physical Electronics of Multi-Dielectric Microstructures."
Agent: National Science Foundation
Amount: **\$55,000** Period: 9/89-5/90 P.I.: M. White
2. Title: "Plasma Oxidation/Anodization of Si films for Photovoltaic and Flat Panel Display Applications"
Agent: National Science Foundation
Amount: **\$237,000** Period: 9/92-8/95 P.I.: D. W. Hess,
3. Title: "Acquisition of an Automated Digital Transmission Electron Microscope"
Agent: National Science Foundation
Amount: **\$709,300** Period: 6/96-8/99 P.I.: D. Smith
4. Title: "An Integrated Chemical Reforming Microplant for Fuel Cell Applications"
Agent: National Science Foundation
Amount: **\$533,000** Period: 11/99 – 10/02 P.I.: M. Kothare
5. Title: "Large Area Biosensing electronics"
Agent: National Science Foundation
Amount: **\$835,300** Period: 8/00 – 7/03 P.I.: D. W. Greve
6. Title: "Smart Microchemical Plant-on-Chip for High Performance Microscale Portable Power"
Agent: Pittsburgh Digital Greenhouse
Amount: **\$150,400** Period: 9/01 – 8/02 P.I.: M. Kothare
7. Title: "Acquisition of an Advanced Electron Lithography System"
Agent: National Science Foundation
Amount: **\$360,000** Period: 9/01 – 8/04 P.I.: M. White

SUPERVISION OF Ph.D. DISSERTATIONS

1. Fuyu Lin (1994) “Structural and Electrical Characteristics of Polycrystalline Semiconductors for Thin Film Transistor Applications”
Retired as: Vice President, Great Wall Semiconductor
Previous: Motorola Semiconductors
2. Apostolos Voutsas (1994) “Low Temperature Deposition of Polycrystalline Silicon for Active Matrix Liquid Crystal Applications”
Present Employment: Peratech Holdco Ltd. (CTO)
Previous: Director, Sharp Laboratories of America
3. Kola Olasupo (1994) “Physics and Technology of Submicron Polysilicon Thin Film Transistors.”
Previous: AMD, Prairie View A&M University
4. Ji-Ho Kung (1994) “Effect of Gate Dielectric on Performance of Polysilicon Thin Film Transistors”
Present Employment: Associate Professor, National United University, Taiwan
Previous: ITRI
5. Greg Sarcona (1995) “Effects of Silicides and Device Structure on the Characteristics and Circuit Performance of Polysilicon Thin Film Transistors for Active Matrix Liquid Crystal Display”
Present Employment: Roche (Project Manager)
Previous: Western Digital
6. Sue Heng Lin (1995) “Physics, Technology and Characterization of Polysilicon Thin Film Transistors with Low Leakage Current Performance.”
Present Employment: NXP Semiconductors (Principle Engineer)
Previous: Freescale Semiconductors
7. Mark Stewart (1999) “Polysilicon Devices for Large Area Electronics Applications: Organic Light Emitting Diode Displays and X-Ray Sensors.”
Present Employment: Chair STEM Department, SUNY Ulster
8. Robert Howell (2000) “Advanced Metallization and Applications to Large Area Active Matrix Arrays and Polysilicon Thin Film Transistors”
Present Employment: Northrop Grumman (Sector Architect)
9. Franklin Nkansah (2001) “Technology and Reliability of Sub-Micron 1T-Flash Electrically Erasable Programmable Read Only Memory (EEPROM)”
Previous: AMD
10. Suraj Karnik (2002) “Materials, Devices and Processes for Integrated Chemical Microsystems.”
Present Employment: AMD (Sr. Manager Product Development Engineering)
Previous: Intel

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11. Themis Afentakis (2004)
“Active Matrix Technology for Flexible Displays and Biosensors”
Present Employment: Apple (Senior Engineer)
Previous: Sharp Labs. of America
12. Sabrat Mukherjee (2006)
“Integrated Microchemical Systems for Processing Methanol Reformer Effluents for Portable Fuel Cell Applications.” Co-Advised with Prof. M. Kothare
13. Matias Troccoli (2006)
“TFT Circuits for Display and Large Electronics on Metal Foils.”
Present Employment: CEO and Co-Founder of Gybe
Previous: Vice President of Technology, Next Biometrics
14. Ta-Ko Chuang (2007)
“Active Matrix Organic Light Emitting Diode Displays on Flexible Metal Foil Substrates.”
Present Employment: Apple (Engineering Program Manager)
Previous: Corning Inc.
15. Po-Chin Kuo (2009)
“Flexible electronics based on polysilicon TFTs on steel foil: Fabrication and characterization under strain.”
Present Employment: Samsung
Previous: TSMC
16. Abbas Jamshidi-Roudbari (2010)
“Polysilicon TFT Devices, Circuits, & Systems for Large Area Flexible Electronic Applications.”
Present Employment: Apple (Senior Manager)
17. Shahrukh Akbar Khan (2011)
“Amorphous Metal-Oxide based Thin Film Transistors on Metal Foils: Materials, Devices and Circuits Integration.”
Present Employment: Global Foundries
Previous: IBM
18. Nackbong Choi (2011)
“Metal Oxide Thin Film Transistors on Paper Substrate: Fabrication, Characterization and Printing Process.”
Present Employment: LG (VP of Engineering)
19. Thomas Charisoulis (2014)
“Wide Bandwidth - High Accuracy Control Loops in the presence of Slow Varying Signals and Applications in AMOLED Displays and Sensor Arrays.”
Present Employment: Meta
Previous: Apple
20. Forough Mahmoudabadi (2016)
“Indium-Gallium-Zinc Oxide TFTs for Active-Matrix Flat-Panel Displays”
Present Employment: Intel

APPENDIX B: LIST OF MATERIALS CONSIDERED

Exhibit	Description
1001	U.S. Patent No. 9,130,074
1002	File History for U.S. Patent No. 9,130,074
1004	Certified Translation of Japanese Patent Application Publication No. JP1992245683 (“Tamura”)
1006	Polysilicon Tunnel Junctions as Alternates to Diffused Junctions (“Borden”)
1007	U.S. Patent Application US 2010/0240172 (“Rana”)
1008	U.S. Patent No. 5,057,439 (“Swanson”)
1009	Polysilicon Emitters for Silicon Concentrator Solar Cells (“Gan”)
1010	SIPOS Heterojunction Contacts to Silicon (“Kwark”)
1011	[omitted]
1012	An Investigation of The Thermal Stability of The Interfacial Oxide in Polycrystalline Silicon Emitter Bipolar Transistors by Comparing Device Results with High-Resolution Electron Microscopy Observations (“Wolstenholme”)
1013	Structure and Morphology of Polycrystalline Silicon-Single Crystal Silicon Interfaces (“Bravman”)
1014	The Optical Properties of Metallic Aluminum, in <i>Handbook of Optical Constants of Solids</i> (Palik, ed., 1985) (“Smith”)
1015	Amorphous/Crystalline Silicon Heterojunction Solar Cells with Intrinsic Buffer Layer (“Froitzheim”)
1016	Antireflective coating for ITO films deposited on glass substrate (“Chiou”)
1017	An Approach for the Higher Efficiency in the HIT Cells (“Taguchi”)
1018	A high efficiency thin film silicon solar cell and module (“Yamamoto”)
1019	Photovoltaic Technology: The Case for Thin-Film Solar Cells (“Shah”)
1020	Semiconductor Material and Device Characterization, Third Edition (“Schroder”)
1021	Amorphous Hydrogenated Silicon, a-Si:H, in <i>Silicon</i> (Siffert, ed., 2004) (“Fuhs”)
1022	Large Grain Polycrystalline Silicon by Low-Temperature Annealing of Low-Pressure Chemical Vapor Deposited Amorphous Silicon Films (“Hatalis”)
1023	Crystalline Silicon Solar Cell, in <i>Clean Electricity From Photovoltaics</i> (Archer, ed., 2001) (“Green”)

APPENDIX C: THE CHALLENGED CLAIMS OF THE '074 PATENT

THE CHALLENGED CLAIMS OF THE '074 PATENT

Claim Limitation #	Limitation
1[pre]	A method of fabricating a solar cell, comprising;
1[a]	providing a wafer as a central substrate;
1[b]	depositing or growing at least one amorphous interface passivation layer over the substrate;
1[c]	depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant,
1[d]	providing thermal treatment at a temperature of above 500°C. or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer; and,
1[e]	providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof
1[f]	wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.
2	The method of claim 1, further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.
3[pre]	The method of claim 1,
3[a]	wherein the depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer comprises depositing an amorphous silicon-containing compound over the substrate
3[b]	and the providing thermal treatment of about 500°C. or higher separates the amorphous silicon-containing

	compound into the at least one interface passivation layer and the at least one conductive and passivating layer.
4	The method of claim 1, wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.
5[pre]	The method of claim 1,
5[a]	wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and
5[b]	wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.
6[pre]	The method of claim 1,
6[a]	wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and
6[b]	wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer and increases the optical transmissivity.
7[pre]	The method of claim 1,
7[a]	wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and
7[b]	wherein the thermal treatment activates doping atoms in the compound.
8[pre]	The method of claim 1,
8[a]	wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound and
8[b]	wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.