CERTIFICATE OF TRANSLATION ACCURACY

I, Alex Jo, declare:

1. I am a professional reviewer and coordinator specializing in translating Chinese, Japanese and Korean to English.

2. I served as Chief Examiner of the certified court interpreter test for the State of California and as a contract translator and interpreter for various federal agencies through the U.S. Department of State of for more than a decade. I served as an instructor at the University of California at Berkeley and the Middlebury Institute of International Studies at Monterey (MIIS).

3. I have more than 30 years of experience in reviewing numerous technical, legal, and business documents from Japanese to English submitted to, among others, U.S. federal courts, the U.S. International Trade Commission (ITC), and the USPTO Patent Trial and Appeal Board (PTAB)

4. I certify that the following translation of the corresponding Japanese source text document is a true, correct, and complete translation to the best of my knowledge and ability.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and accurate.

Statements made herein are to the best of my knowledge true and are based on information that I believe to be true and further these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application in the United States of America or any patent issuing thereon.

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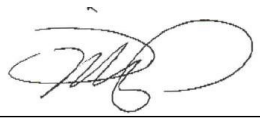
By: 

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(54)【Title of the invention】METHOD FOR MANUFACTURING SOLAR CELL

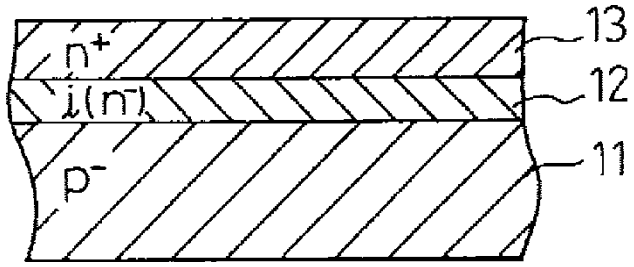
(57)【ABSTRACT】

【PURPOSE】

To form a pn junction at low temperature in order to suppress deterioration of film quality, and to form a pn junction with a high carrier concentration and a shallow graded structure.

【CONFIGURATION】

On a substrate having at least a first type conductive crystalline silicon layer (for example, a p^- type polycrystalline silicon layer) on the surface, a non-doped (for example, n^- type a-Si) layer and a second type conductive amorphous silicon layer (for example, n^+ type a-Si) are deposited at about 150 to 300°C by, for example, a CVD method, and then heat treated at 600 to 700°C (about 900 to 1100°C by conventional thermal diffusion method) to crystallize, forming a pn junction with a graded structure. The carrier concentration of the crystallized silicon layer can be on the order of 10^{21} cm^{-3}, and the film thickness can be 200 to 2000Å (thus the pn junction is also at this depth). Furthermore, the graded structure allows the surface field effect to improve the short-circuit photocurrent, and this pn junction has sufficient quality for practical use as a solar cell.



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What is claimed is:

[Claim 1] A method for manufacturing a solar cell, the method comprising steps of: depositing an undoped amorphous silicon layer on a substrate having at least a surface including a first conductivity-type silicon crystal layer; depositing a second conductivity-type amorphous silicon layer, the conductivity type being opposite to the first conductivity type, on the undoped amorphous silicon layer; and heat-treating the undoped and second conductivity-type amorphous silicon layers to convert the layers into crystalline silicon layers, thereby forming a pn junction having a graded structure.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

FIELD OF INDUSTRIAL USE

The present invention relates to a method for manufacturing a solar cell, and more particularly to a method for manufacturing a solar cell in which a pn junction of the solar cell is formed by solid phase epitaxy.

[0002]

CONVENTIONAL TECHNOLOGY

Solar cells using silicon polycrystals are known. Silicon polycrystals have the advantage of being easier to produce in large areas as compared to silicon monocrystals and are also inexpensive, making silicon polycrystals very promising as a semiconductor substrate for solar cells. In general, a pn junction is formed in a silicon polycrystal substrate by epitaxially growing an n type silicon layer on a p type silicon substrate by a CVD method, or by forming an n type diffusion layer in a p type silicon substrate by a diffusion method.

[0003]

PROBLEMS TO BE SOLVED BY THE INVENTION

However, a method of epitaxially growing a silicon layer by a CVD method requires a high temperature and there are limitations to a substrate that can be used. Moreover, while a plasma CVD method allows growth at a low temperature, there is the disadvantage that film quality deteriorates when a film is subsequently subjected to high-temperature heat treatment, such as electrode paste baking or the like (resulting in a deterioration of device properties). Furthermore, a diffusion method requires a high temperature, and it is difficult to form a diffusion layer with a high concentration of 10^{20} cm^{-3} or more. Moreover, there is the disadvantage that a diffusion depth increases when a concentration is increased, and the controllability of the diffusion layer formation is low.

[0004] Therefore, an object of the present invention is to provide a method for forming a pn junction having a shallow, high-concentration and graded structure at a low temperature, and to provide a high-quality solar cell thereby.

[0005]

MEANS FOR SOLVING THE PROBLEM

In order to achieve the aforementioned object, the present invention provides a method for manufacturing a solar cell, the method comprising steps for depositing an undoped amorphous silicon layer on a substrate having at least a surface including a first conductivity-type silicon crystal layer, depositing a second conductivity-type amorphous silicon layer, the conductivity type being opposite to the first conductivity type, on the undoped amorphous silicon layer, and heat-treating the undoped and second conductivity-type amorphous silicon layers to convert the layers into crystalline silicon layers, thereby forming a pn junction having a graded structure. In short, the present invention is a method for manufacturing a solar cell, the method comprising a step for forming a pn junction with a graded structure by solid phase epitaxy.

[0006] At least a surface of a substrate includes a first conductivity-type silicon crystal layer. The first conductivity-type silicon crystal layer may be the substrate itself, or may be a layer grown on the surface of the substrate. The first conductivity-type silicon crystal layer on the substrate surface is an n^- or p^- type crystal layer having a dopant concentration of approximately 10^{17} to $10^{15}/cm^3$ and a resistivity of approximately 0.1 to 10 Ω·cm.

[0007] The surface of the substrate is highly preferably subject to a cleaning treatment prior to deposition of an amorphous silicon layer in order to form a pn junction of favorable quality by solid phase epitaxy. Specifically, after organic cleaning, a clean substrate surface is achieved by etching with an alkaline solution or mixed acid. Alternatively, this can be achieved by insight plasma etching. First, an undoped amorphous silicon layer is deposited on the substrate, the surface of which includes the first conductivity-type silicon crystal layer.

Herein, “undoped” refers to a film formed using a sample gas that does not contain a dopant gas, such as PH_3 or the like, or a sample gas that contains a dopant gas of approximately several tens to several hundred ppm, including a dopant concentration of $10^{16}/cm^3$ or less.

General conditions for this deposition are as follows:

[0008]

Silicon source:	SiH_4
Gas flow rate:	10 to 50 sccm
Substrate temperature:	150 to 350°C
Pressure:	200 mTorr
Power:	10 to 20 W
Film thickness:	100 to 1000 Å

With this deposition method, an undoped amorphous silicon layer can be formed to a desired thickness at a low temperature.

[0009] On the undoped amorphous silicon layer obtained thereby, a second conductivity-type amorphous silicon layer, the conductivity type being opposite to the first conductivity type, is then deposited. General conditions for this deposition are as follows:

Silicon source:	SiH_4
Dopant (p type):	B_2H_6
Dopant (n type):	PH_3
Dopant concentration:	0.1 to 3%
Gas flow rate:	10 to 50 sccm
Substrate temperature:	150 to 350°C
Pressure:	200 mTorr
Plasma power:	10 to 20 W
Film thickness:	100 to 2000 Å or more

With this deposition method, an amorphous silicon layer doped at a high concentration can be formed to a desired thickness at a low temperature.

[0010] Next, the deposited undoped and second conductivity-type amorphous silicon layers are crystallized by heat treatment.

This heat treatment may be performed at a lower temperature than that required for deposition of a crystalline silicon layer (generally 900 to 1100° C.), and typically, 600 to 700°C may be sufficient, depending on the film quality of the amorphous silicon layer or the like.

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At temperatures below 500°C, it is difficult to obtain favorable crystals, whereas at higher temperatures, random crystal nucleation occurs, preventing epitaxial growth and resulting in polycrystals with small grain sizes.

The heat-treatment atmosphere may be an inert atmosphere, such as argon.

[0011] This heat treatment crystallizes the undoped and second conductivity-type amorphous silicon layers, forming a pn junction having a graded structure. This method first allows the pn junction to be formed at a low temperature, and therefore does not reduce the quality of a semiconductor film or layer. Furthermore, the low temperature prevents a dopant from diffusing deeply into the substrate.

The thickness of the silicon layer to be crystallized can be as thin as approximately 100 Å. In a conventional thermal diffusion method, diffusion to a high concentration reaches a thickness of at least approximately 5000 Å, but in the present invention, the thickness can be reduced regardless of the dopant concentration. However, if the thickness is less than 100 Å, both the open voltage and short-circuit current decrease, reducing the conversion efficiency of the solar cell. The dopant concentration of the crystallized second conductivity-type silicon layer can easily be increased to approximately $10^{21}cm^{-3}$.

Therefore, a pn junction having a shallow and steep concentration gradient is basically obtained. Moreover, due to the presence of an undoped layer, a surface electric field is generated between the outermost surface of the second conductivity-type silicon layer and the pn junction, resulting in an increase in the short-circuit photoelectric current of the solar cell.

[0012] After the heat treatment for solid phase growth, the temperature can be increased to a temperature equal to or higher than the solid phase growth temperature to diffuse a doped impurity and improve a junction interface. The formation of electrodes and the like other than the formation of the pn junction can be performed in the same manner as in a typical solar cell.

[0013]

FUNCTION

A conductive layer is formed on a substrate by solid phase epitaxy, and thus a high-concentration and shallow pn junction can be formed. By interposing an undoped layer, a graded structure can be formed, and the short-circuit photoelectric current can be improved by a surface field effect. Furthermore, this is a low-temperature treatment, and thus the crystal quality of the substrate and the like is not reduced.

[0014]

EMBODIMENT OF THE INVENTION

A deposition device as depicted in FIG. 1 was used. In the drawing, reference numeral 1 denotes a silicon substrate, 2 denotes a substrate holder and RF electrode, 3 denotes a heater, 4 denotes a gas nozzle, 5 denotes an RF electrode, 6 denotes a gas introducing pipe, 7 denotes a plasma generation region, and 8 denotes a vacuum chamber.

Referring to FIG. 2, (100) or (111) Cz monocrystal silicon (resistivity: 2 to 6 Ω•cm) or cast polycrystalline silicon was used, and after performing alkali etching, ultrasonic organic cleaning with acetone, cleaning with pure water, removal of an oxide film using hydrofluoric acid, rinsing with pure water, and dry nitrogen blowing were performed as a pre-treatment for film formation.

[0015] This p- type silicon substrate 11 was placed in a deposition device, and an undoped amorphous silicon layer 12 was deposited under the following conditions.

Source gas:	SiH_4 gas
Gas flow rate:	25 sccm
Substrate temperature:	170°C
Pressure:	200 mTorr
Power:	10 W
Film thickness:	300 Å

Next, a high-concentration n^+ type amorphous silicon layer 13 was deposited on the undoped amorphous silicon layer 12 under the following conditions.

[0016] Source gas: SiH_4 gas containing 1% PH_3

Gas flow rate:	25 sccm
Substrate temperature:	170°C
Pressure:	200 mTorr
Power:	10 W
Film thickness:	700 Å

Next, the substrate 11, on which the amorphous silicon layers 12, 13 were deposited, was heated in an image furnace at a rate of 120°C/min, maintained at 600°C for 5 minutes, and then slowly cooled.

[0017] A crystal structure of the resulting crystallized film was observed by ultraviolet surface reflection and R-HEED (reflection high energy electron diffraction), and the electrical properties were observed by Hall effect measurement and spreading resistance measurement. The results confirmed that a crystal film was obtained, having a graded structure with a carrier concentration of 10^{20} cm^{-1} near the surface, and a resistivity of approximately 10^{-3} Ω·cm (carrier concentration).

[0018] Next, a solar cell will be described with reference to FIG. 3, the solar cell being fabricated as follows. In FIG. 3, 21 denotes a transparent electrode, 22 denotes a comb-shaped front surface electrode, 23 denotes an n^+ type crystalline silicon layer, 24 denotes an n^- type crystalline silicon layer, 25 denotes a p^- type crystalline silicon layer, and 26 denotes a back surface electrode. The properties of the solar cell were measured at AM1.5 and showed an open voltage of 0.56 V, a short-circuit photoelectric current of 32.5 mA/cm^2 on a monocrystal substrate and 29 mA/cm^2 on a polycrystal substrate, and a conversion efficiency of 14.5% and 13%, respectively.

[0019]

EFFECTS OF THE INVENTION

The present invention can provide, using a low-temperature process, a solar cell that has excellent film quality and has a pn junction having a shallow graded structure with a high carrier concentration.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a CVD device of an amorphous silicon layer;

FIG. 2 is a schematic cross-sectional diagram depicting the formation of a pn junction in an embodiment; and

FIG. 3 is a schematic diagram of a solar cell of the embodiment.

DESCRIPTION OF REFERENTIAL NUMERICALS

1. Substrate
2. Substrate holder and RF electrode
3. Heater
4. Gas nozzle
5. RF electrode
6. Gas introducing pipe
7. Plasma generation region
8. Vacuum chamber

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11. p^- type silicon substrate
12. Non-doped amorphous silicon layer
13. n^+ type amorphous silicon layer

FIG. 1

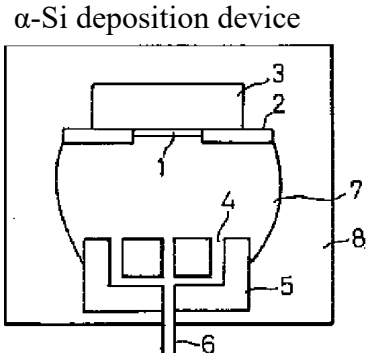


FIG. 2

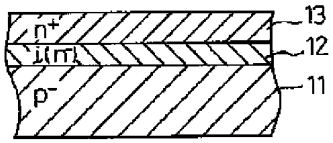
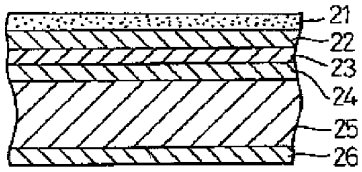


FIG. 3



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