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John C. Bravman; Gary L. Patton; James D. Plummer



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Structure and morphology of polycrystalline silicon-single crystal silicon interfaces

John C. Bravman

Department of Materials Science and Engineering, Stanford University, Stanford, California 94305

Gary L. Patton and James D. Plummer

Integrated Circuits Laboratory, Stanford University, Stanford, California 94305

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Using high resolution transmission electron microscopy, morphological aspects of the polycrystalline silicon (polysilicon)-single crystal silicon interface have been correlated to the surface treatment used prior to polysilicon deposition, and to high-temperature annealing. Specimens which were chemically oxidized prior to the deposition exhibited a continuous layer of amorphous oxide ~ 15 Å thick; high-temperature annealing results in the formation of small discontinuities in this oxide, and thus small regions of epitaxial realignment within the polysilicon layer. Specimens which were etched in HF prior to deposition were characterized by nearly oxide-free interfaces, and, following high-temperature annealing, exhibited regions of epitaxial realignment an order of magnitude larger than those found in the chemically oxidized samples.

INTRODUCTION

The polycrystalline silicon (polysilicon)-silicon interface plays an important role in the electrical behavior of both metal-oxide-semiconductor (MOS) transistors fabricated with polysilicon buried contacts and bipolar junction transistors fabricated with polysilicon emitter contacts. In MOS technology, the buried contact is simply a convenient ohmic connection to the source or drain of the transistor; in bipolar technology, the polysilicon emitter contact can actually enhance the performance of the device. The use of conventional metallization schemes with shallow emitter bipolar devices significantly degrades the emitter injection efficiency, and hence the current gain, due to recombination at the metal contact. Several workers¹⁻⁴ have demonstrated that this problem is greatly reduced by using doped polysilicon in place of metal as the emitter contact material. Suggested explanations for these observations have included reduced emitter band-gap narrowing,¹ tunneling transport of electrons and holes across a thin interfacial oxide layer between the polysilicon and single crystal silicon regions,² and minority-carrier transport effects within the heavily doped polysilicon layer.³ To attempt to distinguish between these models and to establish the relationship between the physical structure and the electrical characteristics of these devices, we have undertaken a high resolution transmission electron microscopy (TEM) study of typical interfacial structures using lattice imaging techniques. Earlier work on these structures by conventional microscopy suggested the presence of a thin amorphous region at the polysilicon-silicon interface,⁵ but was somewhat constrained by the comparatively low resolution of the micrographs presented. Fine details concerning the nature and extent of the epitaxial realignment of the polysilicon were thus obscured.

EXPERIMENTAL PROCEDURES

Three types of emitter contacts were formed on the same wafer: type A, standard metal; type B, polysilicon acting as contact and emitter diffusion source; type C, polysilicon acting as contact only. These three structures are illustrated in Fig. 1. Phosphorus-doped (100) 75-mm, 0.1–

0.9- Ω cm silicon wafers were used. After formation of the base regions, contact holes were opened and oxidized to 400 Å. Types A and C contact holes were then implanted with $10^{15}/\text{cm}^2$ arsenic at 120 keV. Types B and C contact holes were reopened. Following one of two surface treatments that are described in the next paragraph, 4000 Å of low pressure chemical vapor deposition (LPCVD) polysilicon was deposited at 620 °C. A capping oxidation was performed and followed by a blanket implant of $4 \times 10^{15}/\text{cm}^2$ arsenic at 150 keV. An additional implant of $3 \times 10^{15}/\text{cm}^2$ arsenic at 150 keV was done over the type B contacts. A two-step anneal was then performed in an inert ambient, consisting of 60 min at 900 °C followed by 45 min at 1000 °C.

RESULTS AND DISCUSSION

Detailed electrical measurements and parameter extractions of the devices fabricated above have been performed over a range of temperatures and have been reported elsewhere.⁶ The work reported here concerns the morphology of the polysilicon-silicon interface in the emitter contact regions of both type B and type C structures. The observed morphologies provide direct evidence and explanations for the measured electrical characteristics. Most importantly, this work illustrates the effects of two different surface treatments used prior to polysilicon deposition. These treatments correspond to standard wafer cleaning procedures used in many processing laboratories. One treatment, which all wafers received, consisted of an RCA clean followed by an HF dip etch. For the second treatment, some of these wafers

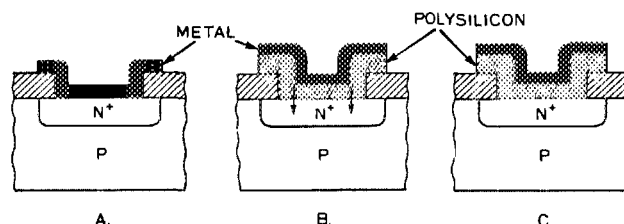


FIG. 1. Cross section of the three types of emitter contacts used: type A, standard metal (Al with a TiW or CVD W barrier layer); type B, polysilicon as the diffusion source for the emitter; type C, polysilicon acting as a contact only (the emitter is implanted prior to polysilicon deposition).

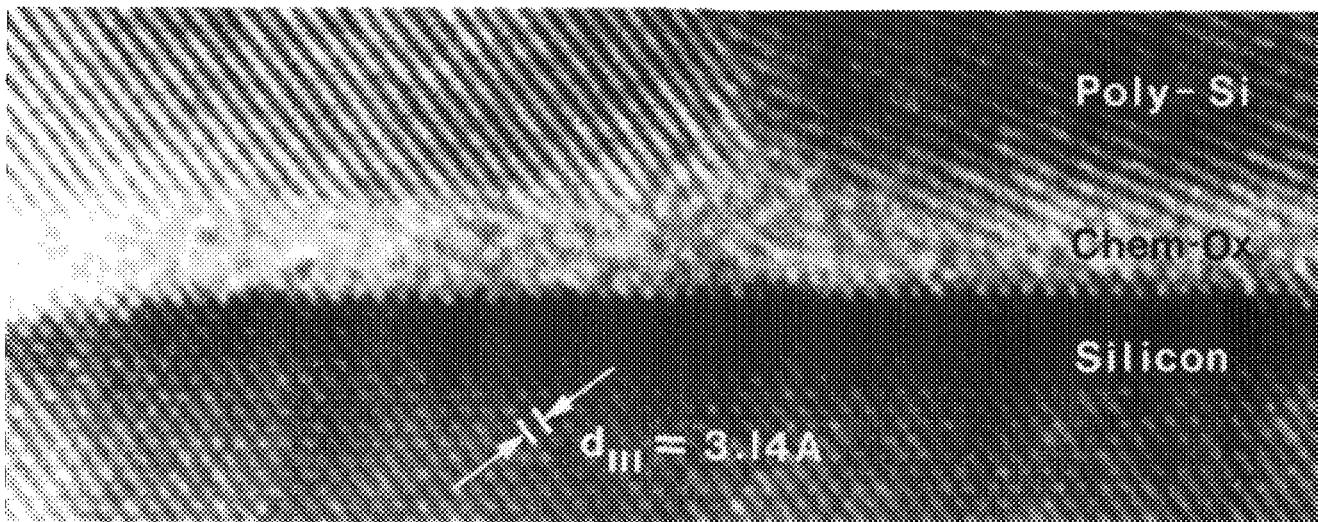


FIG. 2. Chemical-oxide interface imaged at high resolution; the $\langle 111 \rangle$ planes in both the single crystal substrate and in two polysilicon grains are resolved.

were then chemically oxidized via a 10-min immersion in a 70 °C solution of 1:1:5 $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$. Ellipsometry measurements indicated that the oxide thickness varied between 16 and 18 Å. Varying the immersion time (5–30 min), solution temperature (30–90 °C), substrate dopant concentration (5×10^{14} – 10^{20} cm^{-3}), and substrate crystallography ($\langle 100 \rangle$ and $\langle 111 \rangle$) had no discernible effect on the oxide thickness, suggesting that this particular chemical oxidation is a self-limiting process. Cross-section TEM specimens suitable for high resolution imaging were prepared as described elsewhere.⁷ All examinations were performed in a Philips EM400-ST operated at 120 keV and capable of achieving a point resolution of 3.2 Å.

Our TEM results indicate that the interface morphology (1) is strongly related both to the surface treatments described above (HF dip or chemical oxidation) and to any subsequent high-temperature annealing, and (2) is independent of the type of emitter contact (types B or C) being examined. Chemically oxidized wafers which had been exposed to temperatures no greater than 620 °C (the temperature of the polysilicon deposition) exhibited a continuous layer of interfacial oxide and a polysilicon layer characterized by the expected columnar grain structure. After these wafers were

implanted and annealed at 1000 °C, two differences were noted. First, the polysilicon grains had assumed an equiaxed structure, reaching diameters on the order of 2000 Å. As seen in Fig. 2, these grains extend to the interfacial oxide layer. By using the directly resolved Si $\langle 111 \rangle$ lattice planes as a measurement standard ($d_{111} = 3.141 \text{ Å}$), the thickness of the oxide was determined to be $\sim 15 \text{ Å}$, in close agreement with the ellipsometry data. The second change attending the 1000 °C anneal was an alteration of the chemical oxide layer itself, which became discontinuous over $\sim 5\%$ of the silicon surface area. In these regions, the polysilicon made direct contact with, and became epitaxially oriented to, the single crystal substrate. As seen in Fig. 3, however, these regions of epitaxial regrowth were quite small. Typically, they were 30 to 100 Å in width, and protruded 20 to 30 Å above the interface.

Wafers which received a HF dip etch prior to polysilicon deposition showed no evidence of epitaxial regrowth at the interface when examined immediately after the polysilicon deposition. However, implanted wafers annealed at 1000 °C exhibited regrowth structures similar to those cited above, differing primarily in their areal coverage (20–30%) and their size (up to 500 Å laterally along the interface and

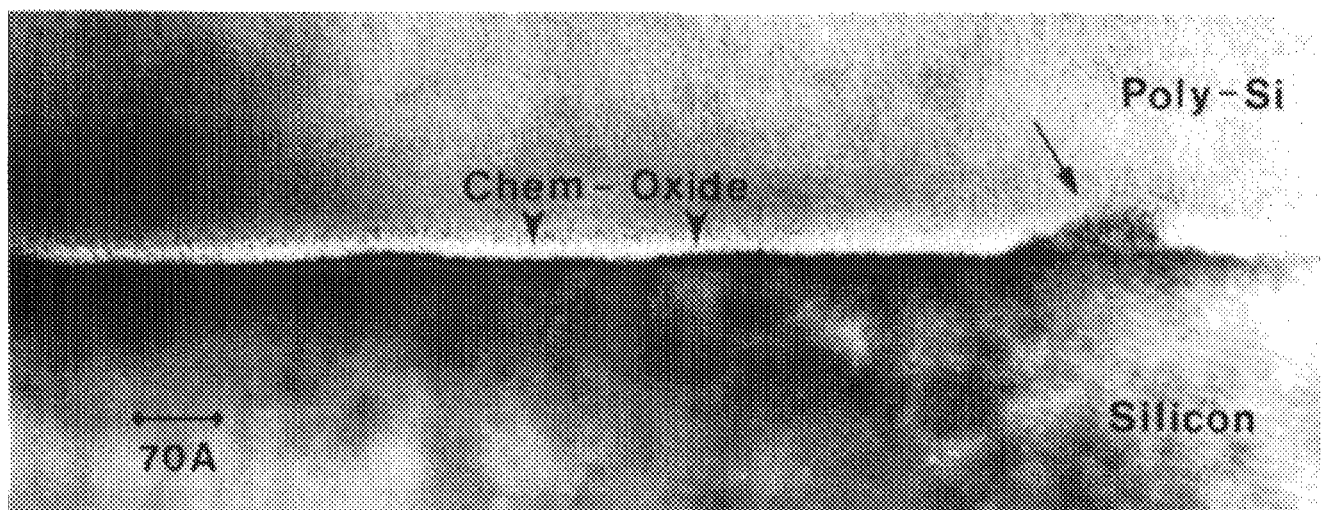


FIG. 3. Chemical-oxide interface following high-temperature annealing, showing a small region of polysilicon epitaxial realignment (arrowed) that formed at an oxide discontinuity.

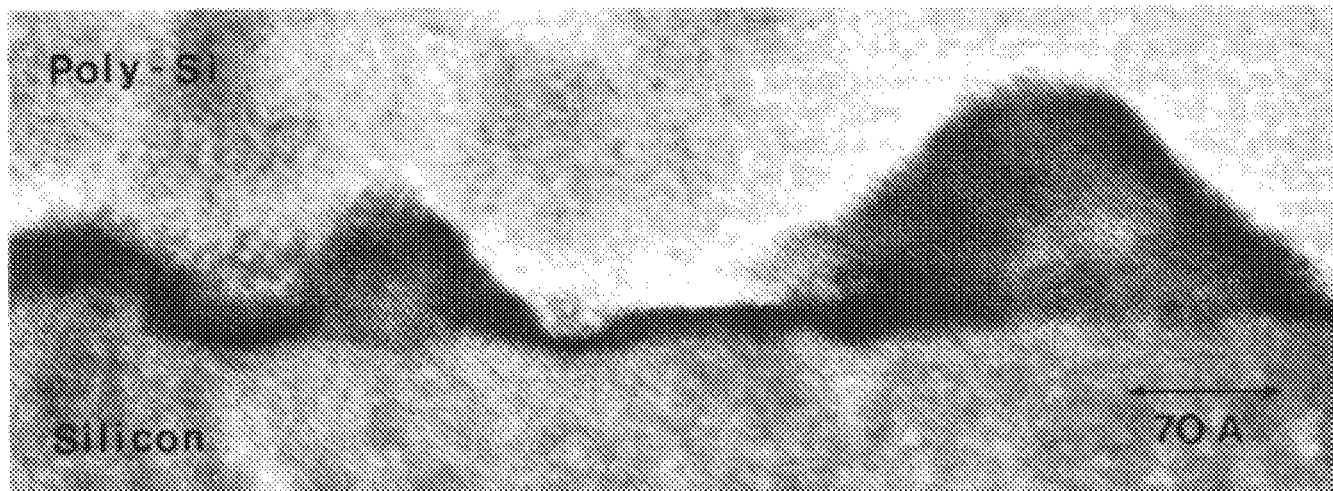


FIG. 4. HF dip etched and annealed interface illustrating size and distribution of typical realignment structures.

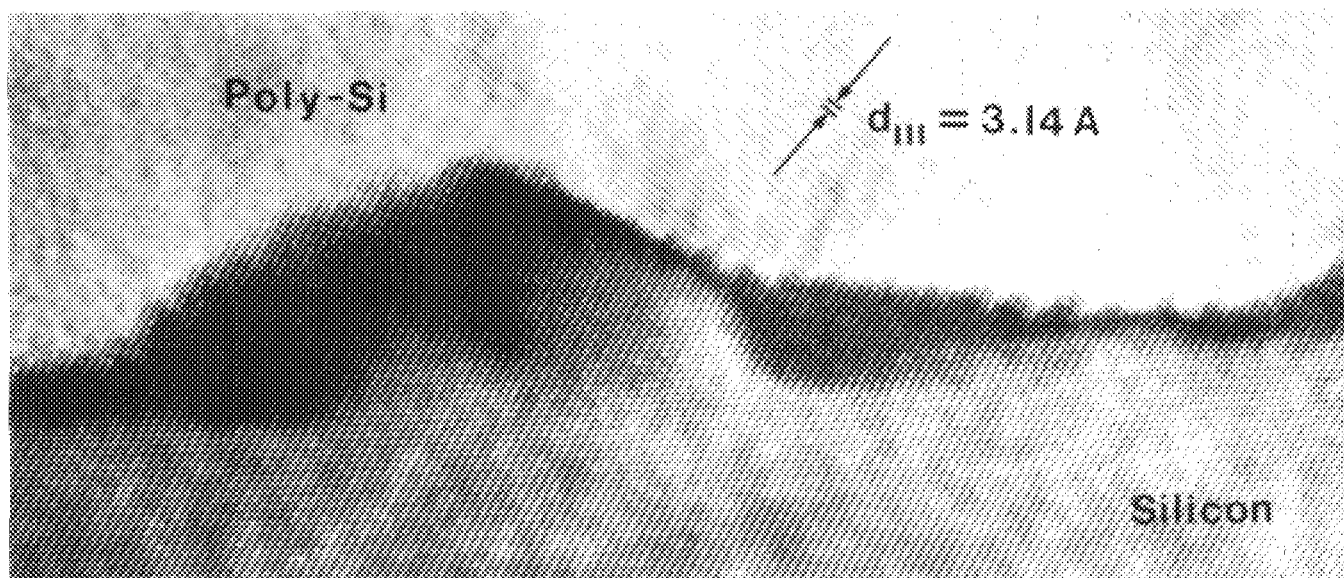


FIG. 5. Large realignment structure with clear epitaxial relationship to the single crystal substrate; misalignment of polysilicon (111) planes indicates that the reorientation did not occur throughout the film.

200 Å vertically into the polysilicon layer). Several of these structures are shown in Fig. 4. A complete epitaxial realignment of the polysilicon film did not occur, although it may be possible to achieve such a regrowth by annealing the samples at a higher temperature (e.g., 1100 °C), or for a longer period of time, or both. Such anneals are not normally encountered during device fabrication, owing to the problems of dopant redistribution and hence junction displacement. Observation of several samples indicated that virtually no oxide remained at these interfaces, suggesting that the interface tunneling transport theory² is inappropriate for modeling polysilicon emitter devices. It should be stressed, however, that the amount of residual interfacial oxide may be strongly related to certain processing techniques. To ensure that the cleanest possible interfaces were obtained, fresh HF solutions were mixed just prior to oxide etching; once etched, the wafers were immediately loaded into the polysilicon deposition system. The remaining small amounts of oxide that were observed were incorporated as small inclusions (20–30 Å in diameter) within the realigned polysilicon and near the original interface. A clear illustration of the epitaxial nature of the regrown polysilicon regions is seen in Fig. 5. In this mi-

crograph, the misalignment between the lattice fringe lines in the bulk of the polysilicon and in the substrate indicates that the epitaxial regrowth did not occur throughout the polysilicon film.

Although the issue is not directly addressed in this paper, it should be noted that interfacial structures of the type described above may act as a barrier to dopant diffusion between the polysilicon and the single crystal emitter. As indicated, however, the morphology of the polysilicon-silicon interface is independent of the type of emitter contact being examined (type B, polysilicon acting as contact and emitter diffusion source; type C, polysilicon acting as contact only), and hence appears to be unaffected by whatever changes, if any, occur in the diffusion process.

To characterize these structures, one of several spectroscopy techniques [such as secondary ion mass spectroscopy (SIMS) or Auger electron spectroscopy (AES)] might be used to measure the amount of oxygen at the polysilicon-silicon interface or the arsenic profile in the single crystal region of the emitter. Sputtering through the polysilicon layer to reach these regions limits the depth resolution of these techniques. Sputter induced surface roughness and ion

knock-on mixing, in the case of SIMS, provide an experimental limit for depth resolution. Figures 4 and 5, however, suggest an additional limitation of these measurements with regard to the HF dip samples. Since the small amounts of oxide remaining at these interfaces do not form a continuous layer, the use of a surface averaging technique will lead to erroneous conclusions concerning the oxygen concentration. Similar problems occur in the determination of the arsenic concentrations in the single crystal portion of the emitter. Arsenic will diffuse very rapidly along the polysilicon grain boundaries until it reaches the interface between the non-aligned and epitaxially aligned portions of the polysilicon layer. The structural roughness of this interface, as seen in the figures and as previously described, results in a nonuniform diffusion of arsenic from the polysilicon layer into the single crystal substrate. As a consequence, the resulting arsenic profile, and hence the base region width, will vary laterally across the structure. A surface averaging technique will not detect this nonuniformity.

ACKNOWLEDGMENT

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