

AN APPROACH FOR THE HIGHER EFFICIENCY IN THE HIT CELLS

Mikio Taguchi, Hitoshi Sakata, Yukihiro Yoshimine, Eiji Maruyama, Akira Terakawa and Makoto Tanaka
Technology R&D Headquarters, Sanyo Electric Co., Ltd.

Seiichi Kiyama
Clean Energy Company, Sanyo Electric Co., Ltd

ABSTRACT

The highest conversion efficiency to date of 21.5% (confirmed by AIST) with a size of 100.3 cm² has been achieved in an HIT cell. Because of this high efficiency and the cell's superior temperature characteristics, HIT cells are highly regarded by consumers. Sanyo will increase the production volume of cells and modules to meet the demand both inside and outside of Japan.

We have been investigating suitable materials based on Sanyo's technology for fabricating high-quality a-Si solar cells to obtain higher build-in potential and control the junction properties, and have been studying how to treat the surface to create a good interface without introducing any damage. We will continue our efforts to obtain even higher levels of conversion efficiency by using the high potential that this structure has.

INTRODUCTION

The HIT (Hetero-junction with Intrinsic Thin-layer) structure, which features a very thin intrinsic a-Si layer inserted between p-type a-Si and n-type c-Si, was originally investigated for a low-temperature junction fabrication technique for a thin-film poly-Si or nc-Si solar cell [1]. This technology is based on Sanyo's successful technologies for fabricating high-quality a-Si films and solar cells with low plasma damage processes. This simple but novel structure has been attracting a growing amount of attention. This is because (1) it simultaneously enables an excellent surface passivation and p-n junction, resulting in high efficiency, (2) its low-temperature processes (<200°C) can prevent any degradation of bulk quality that happen with high-temperature cycling processes in low-quality silicon materials such as solar grade Czochralski (CZ) Si, and (3) compared with conventional diffused cells, a much better temperature coefficient can be obtained with high Voc cells.

We have recently achieved an even higher conversion efficiency of 21.5% with a size of 100.3 cm² in our laboratory. This value was confirmed by AIST Japan.

In this paper, the features of the HIT cell and some ideas to further improve its efficiency are reviewed.

HIT CELL

Device structure

Figure 1 shows the structure of the HIT cell, which is now being mass-produced. The thickness of the randomly textured solar grade CZ Si substrate is ~200 μ m. The p-n junction is realized by the deposition of non-doped a-Si and p-type a-Si layers on an n-type c-Si substrate with the PECVD method. On the bottom side, the Back Surface Field (BSF) structure is used with non-doped a-Si and n-type a-Si layers. On both doped layers, transparent conductive oxide (TCO) layers and metal electrodes are formed with sputtering and a screen-printing method, respectively. All processes are done at temperatures below 200 °C. The TCO layer on the top also works as an anti-reflection (AR) layer. The finger electrode on the AR layer is fabricated with 2-mm spacing, which is narrower than that of conventional p-n diffused solar cells, to compensate for the poor sheet resistance of the TCO layer, whose thickness is optimized for AR coating. We also use a finger electrode for the electrode on the back, to make the HIT cell symmetrical so we can reduce the thermal and mechanical stresses in the device. This makes the cell suitable for various applications, such as bifacial modules [2]. This symmetrical structure and the low-temperature processes offer the advantage of decreasing the cell thickness.

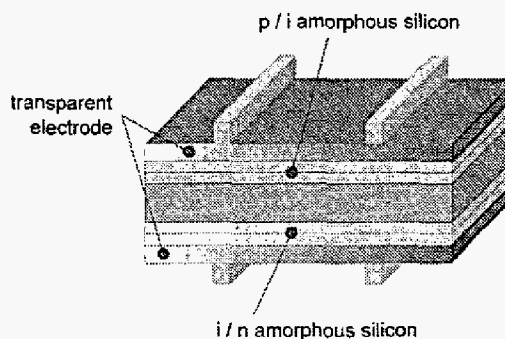


Fig. 1. Schematic diagram of the HIT cell.

Efficiency

Figure 2 shows the progress in conversion efficiency of HIT cells with a practical size of $\sim 100 \text{ cm}^2$. In 1990, we launched basic research into this structure with a size of 1 cm^2 or smaller. Many fundamental results have been obtained and reported. After we achieved efficiency exceeding 20% with this size in 1994, we shifted our target to develop the technology for the mass production of HIT cells. The first mass production lot of HIT modules with a high conversion efficiency of 17.3% was shipped in 1997. Since then, we have made every effort to achieve higher efficiency both in the laboratory and in the factory. Many new technologies for mass production have been developed and adopted. We succeeded in increasing the module efficiency and commercialized 200-W HIT modules in April 2003. In this module, the average cell efficiency is 19.5%. This is quite a high value for a solar cell in mass production.

Further, in our laboratory, we have been continuously developed technologies to improve efficiency and recently achieved a very high conversion efficiency of 21.5% (V_{oc} : 0.712 V, I_{sc} : 3.837 A, FF: 78.7%) with a size of 100.3 cm^2 as shown in figure 3. This value was confirmed by AIST. This is the world's highest value for a solar cell with a practical cell size ($\sim 100 \text{ cm}^2$ and up), matching the value of the SunPower cell [3].

To obtain this efficiency, we have developed new conductive paste materials to achieve high conductivity with a very fine pattern (finger electrode width: $\sim 85 \mu\text{m}$) and a new printing technology for a high aspect ratio (height/width > 0.5). With these technologies, we have been able to realize both a high FF value and a high I_{sc} .

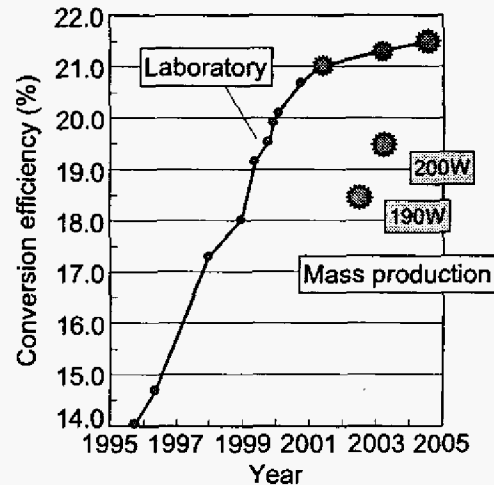


Fig. 2. Progress in HIT cell efficiency.

Temperature coefficient

The temperature dependence of the solar cell performance has been recognized as one of the most important characteristics for determining output power in practical use. Figure 4 shows the cell efficiency normalized at 25°C versus temperature. As reported before [2], the HIT cell shows a much better temperature coefficient of $-0.33 \text{ }^\circ\text{C}^{-1}$ than the conventional p/n diffused solar cell, whose temperature coefficient is

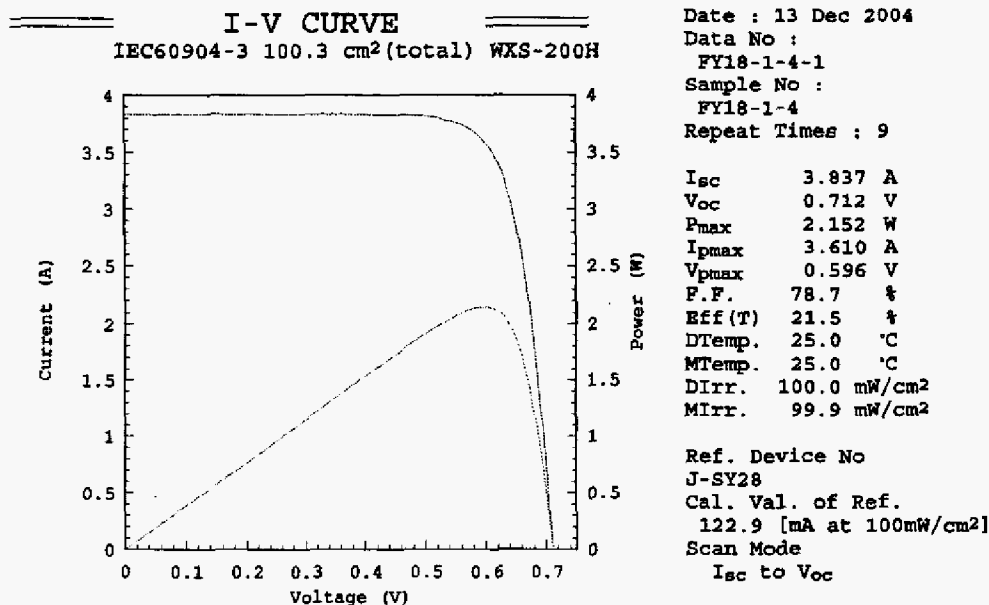


Fig. 3. Output characteristics of HIT cell confirmed by AIST.

AIST

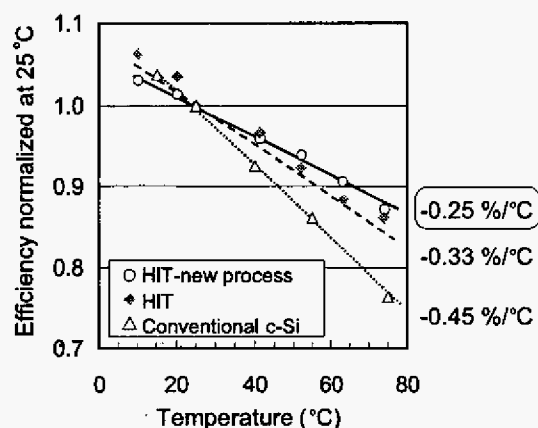


Fig. 4. Temperature dependence of conversion efficiency for crystalline silicon solar cells.

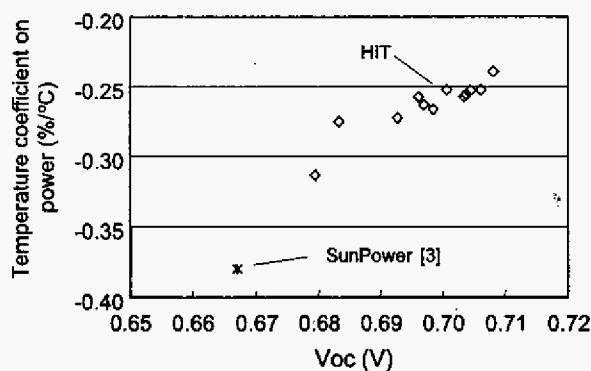


Fig. 5. The relationship between V_{oc} and temperature coefficient on power.

$-0.45\ \%/^{\circ}\text{C}$. With our progress in technologies to exceed 710 mV V_{oc} , the temperature coefficient has been reduced to $-0.25\ \%/^{\circ}\text{C}$. Empirically, we know that solar cells with good surface passivation, in other words, high V_{oc} solar cells, tend to exhibit better temperature dependence. The temperature coefficients for the power of various HIT cells are plotted in figure 5. Here we also plotted the value of the SunPower cell [3]. It is clear that there is a good correlation between the temperature coefficients and V_{oc} of the cells. It is therefore possible to take advantage to obtain more power in practical use by using a higher V_{oc} solar cell. We need more fundamental studies to understand the temperature dependence of solar cells. It would be very interesting to add the data of various kinds of solar cells to figure 5 to investigate the contribution of the a-Si/c-Si hetero-junction to the low temperature coefficients. Though the samples used for this evaluation were fabricated in our laboratory, the temperature coefficient in our production cells has also been improved to $-0.28\ \%/^{\circ}\text{C}$.

Efficiency improvement

Our approach for high efficiency has always been focused on the every interface in the junction. Any defects around the interface caused by poor materials or plasma damage deteriorate the solar cell performance. Based on Sanyo's technology for fabricating high-quality a-Si solar cells, we have investigated the most suitable materials for raising the conversion efficiency.

High-quality doped a-Si:H.

In studying the temperature dependence of the dark I-V characteristics of a-SiC/c-Si hetero-junctions, a change in the slope shape of the I-V curve was observed at lower temperatures [4]. The "S-shape," which can be fitted with the two diode model, could be seen only in the low-temperature region. Since the aim of that report was to investigate the transport mechanism in the device, the authors managed the data to cancel the effect of this change in shape by taking the derivative and did not comment on the reason for it. We thought that this change in shape was mainly caused by thermally activated defects in the doped layer. In order to check the influence of the defect density in the doped layer on the I-V curve, we tried to simulate it with "Aforshet" [5]. The recent progress in the numerical simulators has made it much easier to see the tendency of changes in device characteristics with different parameters. The structure of the cell was p/i-a-Si/n-c-Si/i/n-a-Si and no interface defects were assumed. The parameters used for the simulation were as follows: for c-Si, a band gap of 1.12 eV, a doping level of $N_{\text{donor}} = 5 \times 10^{16} \text{ cm}^{-3}$, and a constant defect state distribution of $1 \times 10^{11} \text{ cm}^{-3}$ were assumed. For a-Si, a band gap of 1.6 eV for the p-type, 1.7 eV for the i- and n-type, a doping level of $N_{\text{donor/acceptor}} = 5 \times 10^{18} \text{ cm}^{-3}$, and an effective density of the conduction band/valence band states of $N_{\text{cb/vb}} = 5 \times 10^{19} \text{ cm}^{-3}$ were assumed. For the defect-state distribution within the band gap, exponential band tail states and a Gaussian distribution σ of midgap states were assumed. The parameters are given in table 1.

Table 1. Parameters for a-Si layers.

	p-type a-Si	i-type a-Si	n-type a-Si
N_{tail} for donor/acceptor	$5 \times 10^{19} \text{ cm}^{-3}$	$5 \times 10^{19} \text{ cm}^{-3}$	$5 \times 10^{19} \text{ cm}^{-3}$
N_{db} for donor/acceptor	$5 \times 10^{16} \text{ cm}^{-3} / 5 \times 10^{16} \text{ cm}^{-3}$	$5 \times 10^{15} \text{ cm}^{-3} / 5 \times 10^{15} \text{ cm}^{-3}$	$5 \times 10^{15} \text{ cm}^{-3} / 5 \times 10^{16} \text{ cm}^{-3}$
σ_{db} for donor/acceptor	0.16 / 0.15 meV	0.1 / 0.1 meV	0.15 / 0.15 meV

For the band offset between a-Si and c-Si, $\Delta E_c = 50 \text{ meV}$ was assumed.

In figure 6, no change was found in the I-V curve with a defect density in the p-layer less than $5 \times 10^{18} \text{ cm}^{-3}$. When the defect density was increased from $5 \times 10^{18} \text{ cm}^{-3}$, the curve suddenly started to shift toward lower voltage and, at the same time, the saturation current density also

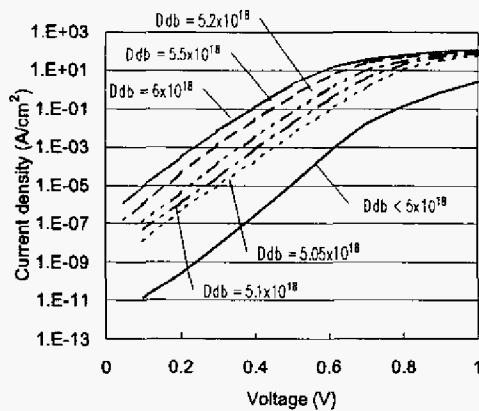


Fig. 6. Simulated data for the dark I-V characteristics of HIT cells by changing the dangling bond density in the p-layer.

started to increase. It was confirmed that a certain level of quality is necessary for the doped layer even if no interface state density is assumed. From a comparison between simulated and experimental data (not shown), we have confirmed that the defect density in our p-layer must be less than $5 \times 10^{18} \text{ cm}^{-3}$ and must not affect the I-V curve.

Controlling interface properties.

As we have reported [1], inserting a non-doped layer into the p-type a-Si/n-type c-Si hetero-junction improves the junction properties drastically. If we try a p/n hetero-junction structure now, we still obtain a value for Voc (~ 0.6 V) that is similar to the data of 15 years ago; meanwhile we can obtain a much-improved Voc in the HIT structure. This shows that the essence of the HIT structure is in creating a good interface to avoid recombination there.

Surface cleaning of c-Si is one of the most important technologies for achieving good interface properties. Since the HIT cell is fabricated under a low-temperature process, it is necessary to load c-Si into the CVD reactor as cleanly as possible. However, it is not suitable to use the expensive RCA cleaning process for the mass production of solar cells. We set up our original, necessary minimum cleaning process in the factory, and have been modifying it to reduce process costs. The wet process has been improved with a lifetime measurement with an iodine-ethanol passivation technique [6] by changing the cleaning conditions.

Controlling the interface properties during a-Si deposition is also important. Even if we used the same quality a-Si layers, we would have obtained different cell properties due to plasma damage during the deposition. We have reported that the lifetime measurement with the a-Si/c-Si structure has been useful for optimizing the a-Si deposition conditions, including reducing the plasma damage to the c-Si surface [7]. In this experiment, as shown in figure 7, we used silicon wafers from the same portion of the ingot to avoid changes in the bulk lifetime

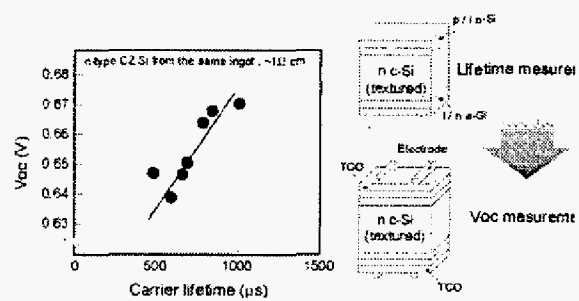


Fig. 7. Relationship between carrier lifetime and the Voc of HIT cells fabricated under various conditions.

for obtaining information about the surface recombination properties of the samples. The a-Si layers were deposited onto both sides of these controlled silicon wafers by changing the deposition conditions. The lifetime data were then measured, followed by the fabrication of TCO and collection electrodes to complete the process. Afterwards, the output characteristics, including Voc, were measured to investigate the influence of the deposition conditions on the solar cell. There is good dependence between carrier lifetime and open circuit voltage. This measurement is also very useful for forecasting the solar cell performance before the metallization process.

With regard to the passivation ability of a-Si film, we have reported that the surface recombination velocity at the interface between a-Si and c-Si on the backside was estimated to be less than 100 cm/s [8]. Further, the excellent surface passivation ability of non-doped a-Si film on c-Si has been intensively investigated by other research institutes and confirmed by various methods [9].

Design of the a-Si/c-Si hetero-junction.

From a numerical analysis of a-Si/c-Si hetero-junction solar cells under a certain level of density of interface states ($D_{it} = 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$), it has been demonstrated that the barrier height to block the minority carriers at the a-Si/c-Si hetero-interface may have been a key for achieving high performance. In the case of a D_{it} of $10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$, however, the effect of the barrier height is suppressed [10]. On the other hand, D_{it} has been experimentally estimated to be smaller than $2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ by the same group [9]. Since we have a very high Voc, we think that the HIT cell has a sufficiently low D_{it} so as not to have to consider the effect of the small change in barrier height.

In our experimental data of the dark I-V curve, the diffusion current region shifts to a higher voltage and, at the same time, the reverse leakage current decreases with increases in the Voc, as shown in figure 8. Here, we plotted the curve of the cell whose Voc was 718 mV, but we have obtained even higher Voc exceeding 720 mV in our laboratory. We think there must be a hint for high Voc cells in this shift of the I-V curve. By combining with our

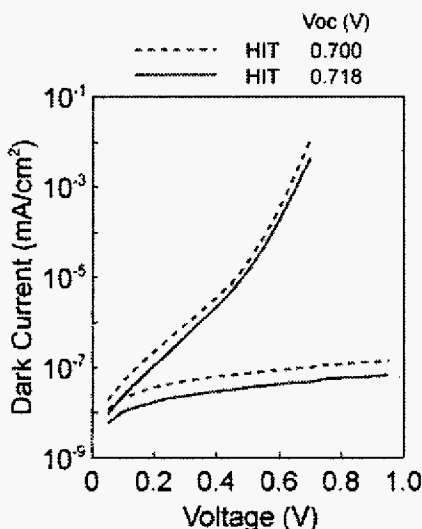


Fig. 8. Dark IV characteristics of the HIT cell

technologies for creating good hetero-junction and further progress in simulation technologies discussed above, we hope we can obtain deeper understandings in the HIT cell and accelerate our attempts to raise efficiency. We will continue to investigate new a-Si films to achieve further improvements in the HIT cell.

Increasing production

Because of the high efficiency and superior temperature characteristics discussed above, HIT cells are highly regarded by consumers both inside and outside Japan. In 2003, Sanyo established an HIT panel production facility for the North American market in Monterrey, Mexico. For the European market, which is expected to surpass the Japanese market in the near future, Sanyo will establish a solar panel production factory in Hungary at Sanyo Hungary Kft. Solar panel production at this new factory is planned to start in June 2005 with a first-year production target of 50 MW, which

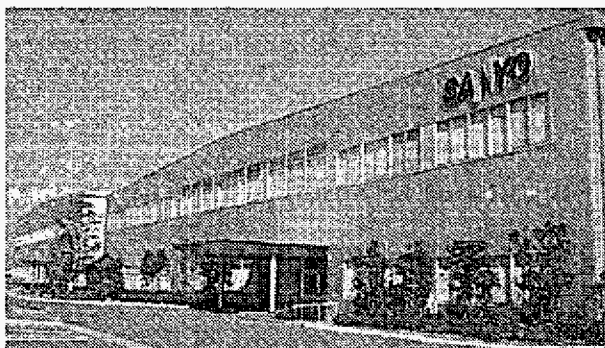


Fig. 9. The Nisiki-no-hama facility in Osaka produces HIT cells and modules. (The building in back has been newly built and started production in January 2005)

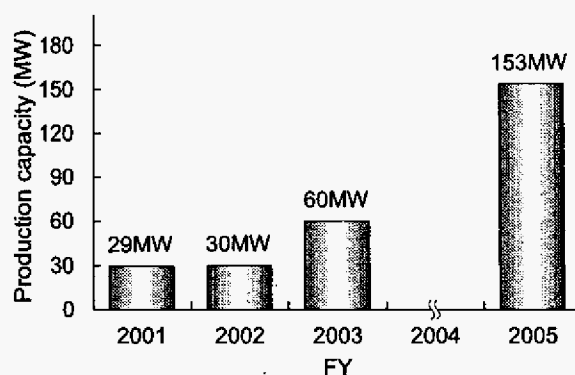


Fig. 10. Production capacity of HIT cell in Sanyo.

is set to grow to 100 MW by 2006.

The annual production output of HIT cells will be increased to 153 MW per year from FY2005. Sanyo intends to further increase its solar cell production capacity to respond to the growing world market (see figures 9, 10).

Conclusion

This paper has introduced Sanyo's recent activities in HIT cells. The highest conversion efficiency to date of 21.5% (confirmed by AIST) with a size of 100.3 cm² has been achieved. Increases in the production of HIT cells and modules have been announced and will begin soon to meet the world's demand for renewable energy.

We also discussed progress in the efficiency of HIT cells and our approach for higher efficiency. We think there are still more possibilities in this structure, and will continue to investigate the structure to produce more efficient and more cost-effective HIT modules.

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