

Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous silicon films

Miltiadis K. Hatalis and David W. Greve

Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, Pennsylvania 15213

(Received 9 June 1987; accepted for publication 2 December 1987)

The crystallization of undoped amorphous silicon films deposited by low-pressure chemical vapor deposition in the temperature range 580–530 °C and annealed from 550 to 950 °C has been studied by transmission electron microscopy. The average grain size of the crystallized films depends on the annealing temperature and the deposition conditions. The nucleation rate of new grains during annealing decreases as the deposition temperature decreases from 580 to 545 °C and/or when the deposition rate increases. The final grain size is also influenced by the annealing temperature with the largest grain size obtained at low annealing temperatures. A simple model is described which explains the dependence of grain size on the annealing temperature. An average grain size of 500 nm has been obtained in a 200-nm film deposited at 545 °C and annealed at 550 °C.

I. INTRODUCTION

Polycrystalline silicon is a material of great importance in microelectronic technology. It is been used as a gate material for field effect transistors, as the emitter in bipolar transistors, and as an interconnecting medium between devices. Active devices have also been made in polycrystalline silicon. Thin-film transistors fabricated in polycrystalline silicon are being actively studied since these devices are potentially useful in future 3D integrated circuits¹ and in the fabrication of flat panel displays.^{2,3}

Thin films of polycrystalline silicon can be obtained by a variety of chemical vapor deposition processes which include low-pressure chemical vapor deposition (LPCVD),⁴ atmospheric pressure chemical vapor deposition (APCVD),⁵ and plasma enhanced chemical vapor deposition (PECVD).⁶ In all of these processes there is a transition temperature below which the deposited film is amorphous. In an LPCVD process this transition temperature is approximately 600 °C. As-deposited amorphous silicon crystallizes and becomes polycrystalline after annealing at temperatures greater than about 500 °C.

Many of the electrical properties of the polycrystalline silicon depend upon its grain size and in general a large grain size is desirable. However, as-deposited polysilicon has a grain size less than 100 nm and after doping and annealing the grain size becomes only 100–200 nm. There have been a number of reported methods for enlarging the grain size of the as-deposited polysilicon. Laser⁷ and strip-heater⁸ recrystallization have been studied intensively. Secondary grain growth in very thin polysilicon films⁹ and grain growth of heavily phosphorus-doped polysilicon¹⁰ have also been reported. However, all these methods are high-temperature processes. Low-temperature processes have also been attempted.^{11–13} These methods involve amorphization of the polysilicon film by means of ion implantation followed by recrystallization of the film during low-temperature annealing. A grain size of 0.5–1.0 μm has been reported following

high implantation doses.^{11–13} However, ion implantation is an extra process step and it may also be impractical for some applications, such as large area flat panel displays.

It has been reported that polysilicon obtained after crystallization of amorphous silicon has a larger grain size than as-deposited polysilicon.^{14,15} In addition to larger grain size these films have other improved properties compared to as-deposited polycrystalline silicon. These include a smoother surface,¹⁴ higher conductivity,¹⁵ and larger breakdown voltages of metal-oxide-semiconductor capacitors.¹⁶ Because of these improved properties there is increasing interest in the use of polysilicon obtained by crystallization of amorphous silicon. However, there is a lack of information on the effect of the deposition conditions and annealing temperature, particularly low annealing temperatures (~ 600 °C), on the grain size of the resulting polysilicon.

In this work we studied the crystallization of amorphous silicon films equal or less than 200 nm in thickness. The films were deposited by LPCVD on oxidized silicon wafers and annealed in the temperature range 550–950 °C. We used transmission electron microscopy (TEM) to examine the grain size of the crystallized amorphous silicon. The effect of deposition conditions as well as the annealing temperature on the grain size is reported. In Sec. II we present data on the deposition rate of amorphous silicon deposited by LPCVD. In Sec. III we describe the method used for calculating the average grain size. The experimental results are presented in Sec. IV, followed by analysis and discussion of the experimental results in Sec. V. In Sec. VI the results are summarized and optimum deposition and annealing conditions are reported.

II. DEPOSITION OF AMORPHOUS SILICON BY LPCVD

All the depositions were performed in a standard LPCVD system. The temperatures reported in the following discussion were measured with a thermocouple while the tube was at atmospheric pressure; consequently the actual

temperatures during deposition may have been slightly different. The pressure of the system was varied by injecting nitrogen to control the effective pumping rate. For pressures up to 0.6 Torr nitrogen was injected at the inlet of the roots pump while for higher pressures nitrogen was also injected at the outlet of the tube. The reactant gas was undiluted silane (SiH_4).

Thermally oxidized silicon wafers 50 mm in diameter were used as substrates. The thickness of the deposited film was determined by first etching a step in a 1:50:20 $\text{HF}:\text{HNO}_3:\text{H}_2\text{O}$ solution and then measuring the height of the step using an Alpha Step 200. The number of wafers in each run was between 10 and 20 and they were located at the center of a three-zone furnace. Even though the load of wafers is much smaller than the load used in industrial runs, nonuniformities were present within a batch of wafers as well as across the wafers at temperatures less than 580 °C. The nonuniformities were significantly reduced when the first zone of the furnace was set 10–20 °C higher than the center zone. In our experiments the wafer load was small enough that the first zone was far from the wafers. However, if a large number of wafers are to be loaded in the furnace, these higher temperatures have to be taken into account; because, as it will be shown in the next sections, the grain size of the crystallized amorphous silicon depends upon the deposition temperature.

In Fig. 1 the deposition rate of amorphous silicon as a function of the deposition temperature is shown. The silane flow was 20 cm^3/min and the pressure was 0.6 Torr. The wafer spacing was 9.5 mm; approximately 8% reduction in the deposition rate was observed when the spacing was reduced to 6.3 mm. We see that the deposition rate down to 530 °C is thermally activated with an activation energy of 1.33 eV. Under the same conditions the deposition rate at 500 °C was only 0.8 nm/min and did not fall on the Arrhenius plot of the Fig. 1. For depositions performed at 2 Torr and 15 cm^3/min of silane the activation energy is 1.51 eV. These results agree well with the reported values of 1.39–1.73 eV.¹⁴

In order to examine the influence of deposition pressure and silane flow on the deposition rate a systematic study was

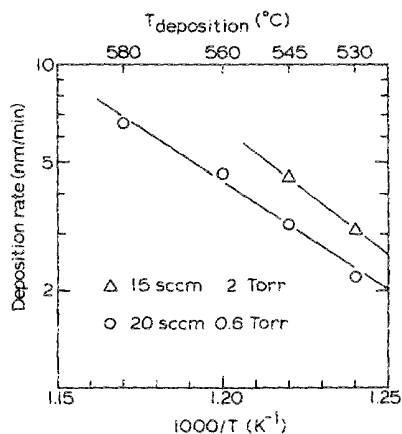


FIG. 1. Deposition rate of amorphous silicon as a function of deposition temperature.

carried out at 545 °C. In Fig. 2 the deposition rates are plotted as a function of deposition pressure for two different silane flows. As can be seen, the deposition rate can be increased by increasing the deposition pressure and/or the silane flow. However, we found that there is an upper limit of deposition rate beyond which the deposited wafers have rough surfaces and brown deposits are produced on the walls of the reactor tube. These results may be a consequence of polymerization of silane in the gas phase.¹⁷ We determined the upper limit of deposition rates in our reactor by increasing the silane flowrate at constant pressure until rough deposits were obtained. In Fig. 3 we plot the maximum silane flow as a function of pressure for depositions that resulted in smooth surfaces.

III. METHOD FOR CALCULATING GRAIN SIZE

There are a variety of methods for calculating the average grain size which have been developed for metallurgical applications.¹⁸ One of these, the intercept counting method,^{10,18} has also been used for determining the average grain size of polycrystalline silicon.¹⁰ However this method, as all the others intended for metallurgical applications, requires that the grain boundary between two grains be clearly visible. This usually presents no problem in as-deposited polycrystalline silicon, because this material has a columnar structure and the grain boundaries can clearly be distinguished.

It has been shown, however, that the crystallization of amorphous silicon does not result in grains with a columnar structure.¹⁹ After annealing, amorphous silicon deposited by CVD or by evaporation becomes polycrystalline with a needlelike or dendritic structure.^{19,20} We observed a similar structure in polycrystalline silicon obtained after annealing of LPCVD amorphous silicon. Because of fine structure at the grain boundaries and because grains overlap, the grain boundaries in these films are very difficult to resolve. The grains, however, are clearly visible in dark-field images, where only a few grains are visible in each image as a white area on a black background. Figure 4 shows a dark-field image of a film deposited at 545 °C and annealed at 550 °C for 72 h. As is shown, the grains have a needle or featherlike shape and a very fine structure exists inside the grains. This

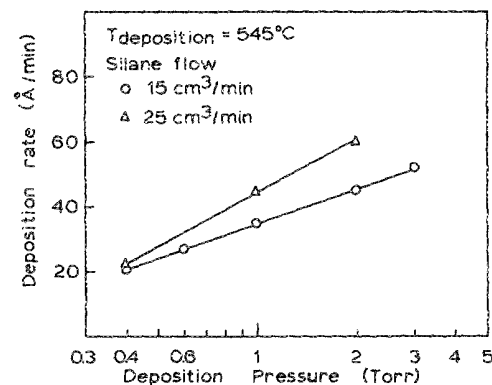


FIG. 2. Deposition rate as a function of deposition pressure for films deposited at 545 °C.

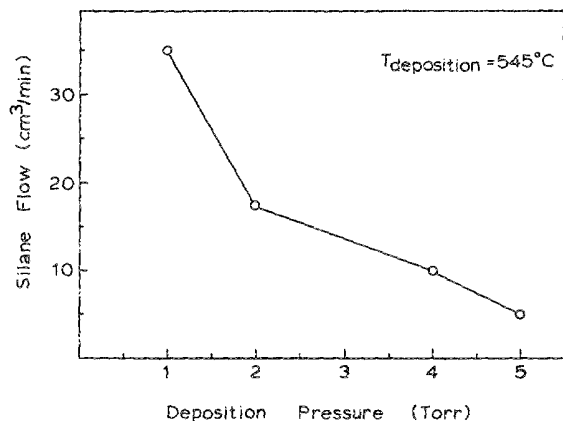


FIG. 3. Maximum silane flow as a function of deposition pressure for films deposited at 545 °C with smooth surface.

structure is visible as a fine black and white contrast in the TEM image, and is an indication that the grains have defects.

From Fig. 4 we can also see that the grains are approximately ellipsoidal in shape. By measuring the length of the two main axes (a, b) of these ellipsoids and by setting the area of each ellipsoid equal to the area of a square of side g , we find that the grain size of each grain is given by

$$g = (\pi ab)^{1/2}/2. \quad (1)$$

By actually measuring the area of different grains we found that this approach underestimates the grain size by less than 5%. In order to calculate the average grain size of each crystallized film a number of dark-field TEM images were recorded and the two main axes of the resolvable grains were measured. The grain size was first calculated for each grain and from these values the average grain size was computed. Generally 130 grains were measured from each sample and the results were reproducible within 10%.

As will be shown in the next section, the crystallized films consist mainly of grains with grain size greater than

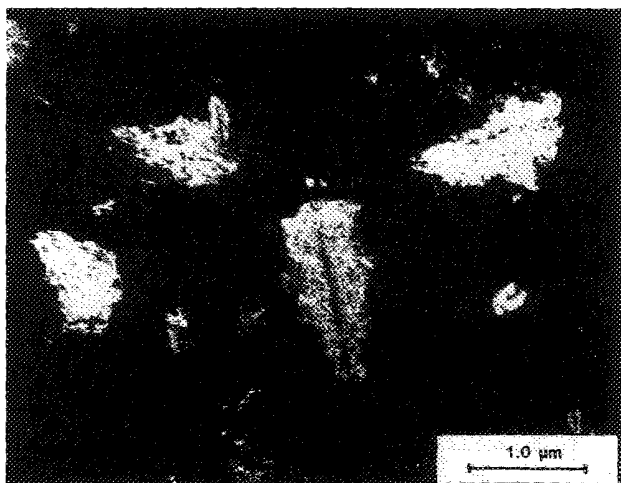


FIG. 4. Dark-field TEM micrograph of a film deposited at 545 °C and annealed at 550 °C for 72 h.

100 nm. Smaller grains are present but the area which they occupy is much less than the area of the larger grains. Thus grains with grain size smaller than 100 nm have not been taken into account. The standard deviations of the grain size distributions were approximately one half of the mean grain size.

IV. EXPERIMENTAL RESULTS

Having established a method for accurate and repeatable determination of the grain size, we will present, in this section, data on how the deposition and the annealing conditions affect the grain size of the annealed films. We will first examine the effect of the deposition and annealing temperatures. The effect of the deposition rate on the grain size will be presented next, followed by the influence of the film thickness on the grain size. Finally, we will discuss the crystallization of the amorphous films as revealed by TEM micrographs taken after annealing for various times.

Amorphous silicon films 190 ± 10 nm thick were deposited on oxidized silicon wafers by LPCVD at a silane flow of 20 cm³/min and deposition pressure of 0.6 Torr. The thickness of the silicon dioxide layer was 100 nm. After deposition the wafers were broken into several pieces, each of which was annealed at a different temperature between 550 and 950 °C until the crystallization was complete. In Fig. 5 the grain size is plotted as a function of the deposition temperature for two annealing temperatures (550 °C for 72 h and 950 °C for 30 min). For a given deposition temperature larger grain size was obtained after annealing at the lower temperature while for both annealing temperatures the grain size is greatest at a deposition temperature of 545 °C.

Our high-temperature annealing results agree very well with the results reported by Becker *et al.*¹⁵ who obtained 200 nm grain size for a 560 °C deposited film after annealing at 950 °C for 30 min. However, our results disagree with those of Harbeck *et al.*¹⁴ who obtained grain size of less than 100 nm after annealing at 1000 °C a film deposited at 560 °C. Low-temperature anneals of APCVD amorphous silicon were reported by Bisaro *et al.*²¹ who estimated an average grain size of 60 nm from x-ray data. However, the results for APCVD films cannot be directly compared with ours, be-

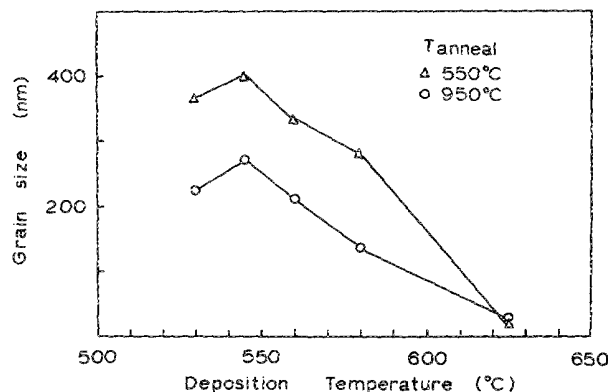


FIG. 5. Grain size as a function of deposition temperature for 200-nm-thick films annealed at 550 °C for 72 h and for films annealed at 950 °C for 30 min.

cause the transition from polycrystalline to amorphous deposition in an APCVD system occurs at a different temperature.

To examine the effect of deposition rate on the grain size, films were deposited at 545 °C with different deposition rates and annealed at 550 °C. The grain size as a function of the deposition rate is plotted in Fig. 6. It is apparent from Fig. 6 that high deposition rates result in larger grain size. However, this occurs at the expense of increased annealing time. Films deposited at high deposition rate required a longer annealing time than films deposited at low deposition rate. As will be discussed in the next section, higher deposition rates resulted in decreased nucleation rates; thus the films took longer to crystallize.

The effect of the film thickness on the grain size was also examined for two of the deposition temperatures. Films with thicknesses of 50, 100, and 200 nm were deposited at 530 and 560 °C with deposition rates of 2.2 and 4.6 nm/min, respectively (SiH_4 flow = 20 cm^3/min and pressure = 0.6 Torr). The grain size after annealing at 600 °C for 12 h is plotted as a function of the film thickness in Fig. 7. For the case of 560 °C the grain size increases monotonically as the thickness increases while for 530 °C the grain sizes for 100 and 200 nm are approximately the same. These results show that large grain size can be obtained even in a very thin film by using a low deposition temperature.

It is interesting to note that completion of crystallization can be detected by a change in the color of the film. This is a consequence of the different index of refraction of amorphous and polycrystalline films. The change in color correlated well with TEM results and was used to investigate the dependence of crystallization time on deposition and annealing temperatures. The crystallization time varied from a few minutes for annealing at 850 °C to several days at 550 °C. Shorter crystallization times were observed for higher deposition temperatures.

To gain more information about the crystallization of the amorphous silicon, samples were annealed at 600 °C for various times (1, 2, 4, and 12 h) and were studied by using TEM. The grain size was found to increase with time and when the crystallization had been completed after approximately 3–4 h the grain size remained constant and did not increase after further annealing. As expected, the grains are

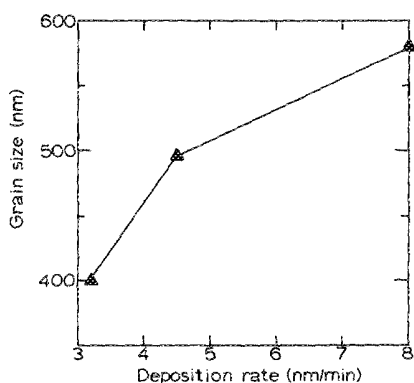


FIG. 6. Grain size as a function of deposition rate for 200-nm-thick films deposited at 545 °C and annealed at 550 °C.

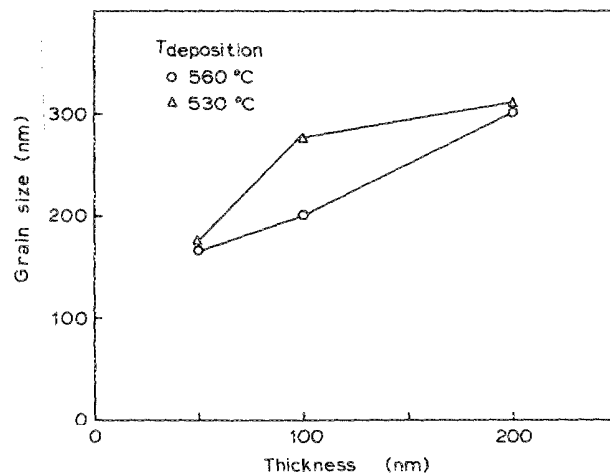


FIG. 7. Grain size as a function of film thickness for films deposited at 530 and 560 °C and annealed at 600 °C for 12 h.

stable after complete crystallization, because much higher annealing temperatures are required to increase the grain size of a polycrystalline film.²² TEM pictures of samples deposited at 545 and 560 °C and annealed at 600 °C for 2 h are shown in Figs. 8(a) and 8(b), respectively. The density of grains in the 560 °C deposited film is higher than the 545 °C deposited film suggesting that the nucleation rate of new grains increases as the deposition temperature increases. From Figs. 8(a) and 8(b) we can also see that most of the grains crystallize individually and are surrounded by amorphous silicon. Occasionally, nucleation of new grains occurs at the grain boundaries of existing ones.

V. DISCUSSION

Our results have shown that the crystallization and the final grain size of the annealed film depend on four main parameters: the annealing temperature, the deposition temperature, the deposition rate, and the thickness. For a given thickness the grain size increased with decreasing annealing temperature, decreasing deposition temperature down to 545 °C, and increasing deposition rate.

In this section, we will discuss how the four main parameters mentioned above affect the grain size. We will first discuss the crystallization of films by nucleation and growth and develop a simple analytical model in order to explain the dependence of grain size on annealing temperature. Then we will discuss how the deposition parameters affect the grain size.

The driving force for the crystallization of the amorphous silicon films is the lower Gibbs free energy of the crystalline phase compared to the amorphous phase. The phase transformation from amorphous to crystalline occurs in the solid state and can be characterized as an irreversible polymorphic change.²³ The crystallization of the amorphous silicon, like most of the transformations occurring in the solid state, takes place by nucleation and growth where both processes are thermally activated.²³

Calculation of the relation between the grain size and the growth and nucleation rates is a relatively complex prob-

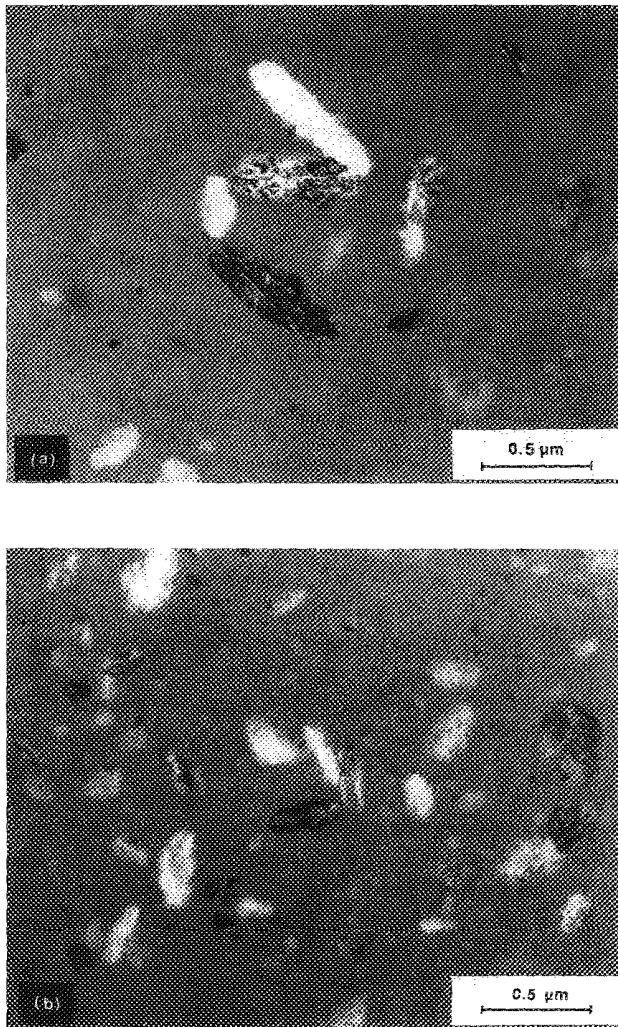


FIG. 8. Bright-field TEM micrographs of 200-nm-thick films annealed at 600 °C for 2 h; (a) film deposited at 545 °C and (b) film deposited at 560 °C.

lem and several approaches to its solution have been reported.²⁴⁻²⁷ Here, we make several simplifying assumptions in order to relate the grain size to the annealing temperature and the activation energies of the nucleation and growth rates. The purpose of this model is to explain our experimental results and to extract from them quantitative information about the growth and nucleation processes in LPCVD amorphous silicon films. Following the Johnson-Mehl equation,^{24,25} the amorphous fraction of the film as a function of time and annealing temperature is given by

$$1 - X_t = \exp \left(\int_0^t s u_x u_y u_z (t - t')^3 I dt' \right), \quad (2)$$

where X_t is the crystallized fraction of the film at a given time t ; u_x , u_y , u_z are the linear growth rates for the three coordinates; I is the nucleation rate; and s is a shape factor. Our results show that the average grain size is in all cases greater than the film thickness; thus we can reduce the three-dimensional problem of Eq. (2) to a two-dimensional one. If we also assume isotropic growth and that both the nucleation and growth rates are independent of time we can write

$$1 - X_t = \exp(-fdIu^2t^3/3), \quad (3)$$

where d is the film thickness and f is factor which is determined experimentally. The factor f is approximately the reciprocal of the number of grains across the film thickness. Cross-sectional TEM photographs such as the one shown in Fig. 9 indicate that f is between 0.5 and 1. The total number of nuclei formed in a film of volume V_0 is given by

$$N_{\text{tot}} = \int_0^\infty IV_0(1 - X_t)dt. \quad (4)$$

If we assume that each final grain with an average grain size g represents one nucleus then the total number of grains is also given by

$$N_{\text{tot}} = V_0/fdg^2, \quad (5)$$

since the product (fdg^2) is the average volume of each grain. Assuming that the nucleation and growth rates are thermally activated with activation energies E_n and E_g , respectively, we have

$$I = I_0 \exp(-E_n/kT) \quad \text{and} \quad u = u_0 \exp(-E_g/kT), \quad (6)$$

and then from Eqs. (4), (5), and (6) the average grain size becomes

$$g = g_0 \exp[(E_n - E_g)/3kT], \quad (7)$$

where g_0 is independent of the annealing temperature T . For thick films in which growth is three dimensional it can be shown that the exponent in Eq. (7) becomes $(E_n - E_g)/4kT$.

From Eq. (7) we can see that the grain size will increase with decreasing annealing temperature provided that E_n is greater than E_g . In Fig. 10 we plot the logarithm of the grain size as a function of the reciprocal of the annealing temperature for different deposition temperatures. These data show good agreement with the behavior predicted by Eq. 7. Our results indicate that the nucleation activation energy is higher than the growth activation energy and that the difference of the activation energies is 0.25 eV. Although this difference

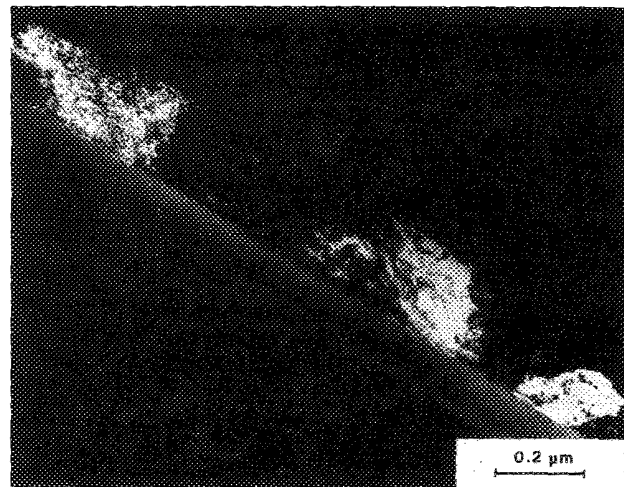


FIG. 9. Cross-sectional dark-field TEM micrograph of a film deposited at 560 °C and annealed at 600 °C for 12 h.

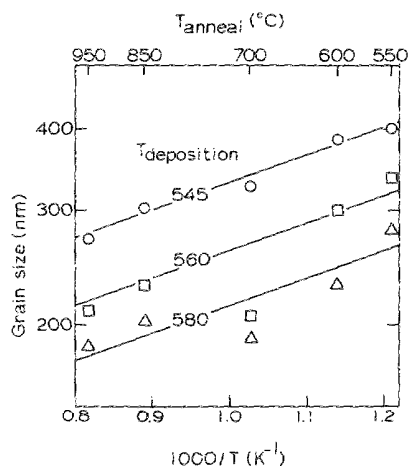


FIG. 10. Grain size as a function of annealing temperature for 200-nm-thick films deposited at three different deposition temperatures.

is positive, it is about one order of magnitude lower than the difference of the two activation energies reported for electron-beam-evaporated amorphous silicon.^{19,26} Evaporated amorphous silicon, however, is deposited under very different conditions and consequently the activation energies are not expected to be the same.

The dependence of the grain size upon the deposition conditions will now be considered. Our TEM studies of films that have been annealed for different time intervals show that there is a definite dependence of the nucleation rate upon the deposition temperature. In Fig. 8, TEM pictures of incompletely crystallized films deposited at 545 and 560 °C are shown. More crystallites are present for the higher deposition temperature indicating that at low deposition temperatures stable nuclei occur with more difficulty, i.e., the nucleation rate has been decreased. Consequently, for low deposition temperatures the grains grow larger before they impinge on each other. A reduction in the nucleation rate was also revealed by TEM micrographs, taken at different time intervals, when the deposition rate was increased at a constant deposition temperature (545 °C).

So far we have not discussed why the nucleation rate depends upon the deposition conditions. It has been shown that as the deposition temperature increases a larger number of stable crystallites are formed and buried in the deposited film.²⁸ These crystallites can form stable nuclei even at the beginning of the annealing step. In addition to these initial nuclei new nuclei are continually formed in the film with a rate which, for a given annealing temperature, depends upon the conditions under which the film has been deposited.

In amorphous silicon the short-range tetrahedral ordering of the diamond structure is retained but long-range disorder exists due to the different ways in which these tetrahedra are connected.²⁹ We suggest that the disorder which exists in the amorphous state is influenced by the deposition conditions. As the deposition temperature increases the local arrangement of the tetrahedra may more closely resemble that of single-crystal silicon and these ordered regions may be favorable sites for nucleation during annealing, thus

resulting in higher nucleation rates. This more ordered arrangement of the silicon tetrahedra is possible because at higher deposition temperatures silicon species have higher surface diffusivity.³⁰ We have also seen that the nucleation rate decreases as the deposition rate increases. This may occur because at higher deposition rates the silicon species have less time to rearrange themselves thus a higher degree of disorder exists resulting in decreased nucleation rate.

It was assumed so far that nucleation is homogeneous and uniform throughout the film. However, planar and cross-sectional TEM pictures have shown that this is not always true. For silicon deposited at 545 °C, at a deposition rate of 4.8 nm/min, heterogeneous nucleation on the SiO₂ at the bottom of the film occurs, while for the case of 530 °C deposited film, at a 2.2 nm/min deposition rate, we found that nucleation at the grain boundaries of existing grains is very common. Surface nucleation should be most important for very thin films. Figure 7 shows that the 50-nm-thick film had the lowest grain size, for both 530 and 560 °C deposition temperatures, indicating a higher nucleation rate than thicker films.

Although this paper discusses only the structural characteristics of the crystallized LPCVD amorphous films, we would like to note that we have fabricated thin-film transistors in these films.³¹ It was found that the performance of these devices depends upon the grain size and the performances of devices in crystallized films is far superior to devices fabricated in as-deposited polysilicon.

VI. SUMMARY

The crystallization of amorphous silicon films deposited by LPCVD in the temperature range 580–530 °C and annealed in the temperature range of 550–950 °C has been studied by TEM. It was found that the average grain size of the crystallized film is influenced by the annealing temperature, the deposition temperature, the deposition rate, and the film thickness. For a given thickness the grain size increases when the deposition temperature decreases, the deposition rate increases, and the annealing temperature decreases.

We explained the dependence of the average grain size on annealing temperature with a simple model. This model predicts a larger grain size at lower annealing temperature provided the activation energy for nucleation of new crystallites is larger than the activation energy for grain growth. From the experimental data we calculated a difference of 0.25 eV between the two activation energies. We also found that the nucleation rate decreased as the deposition temperature was lowered from 580–545 °C and when the deposition rate increased. The reduction of the nucleation rate explains the increase of grain size with decreasing deposition temperature and increasing deposition rate.

In this work average grain size as large as 500 nm was obtained for a 200-nm film deposited at 545 °C at a deposition rate of 4.8 nm/min after annealing at 550 °C. Large grain size has also been observed for thinner films after annealing at low temperatures.

Note added during revision: Since submission of this paper, R. B. Iverson and R. Reif [J. Appl. Phys. **62**, 1675

(1987)] have reported a similar study of grain growth in silicon films amorphized by ion implantation. A similar dependence of grain size on annealing temperature is observed but a different activation energy.

ACKNOWLEDGMENT

The authors would like to thank Philips Research Laboratories, Sunnyvale and the Semiconductor Research Corporation for supporting this work.

- ¹S. D. Malhi, H. Shichijo, S. K. Banerjee, R. Sundaresan, M. Elahy, G. Pollack, W. Richardson, A. H. Shah, L. R. Hite, R. H. Womack, P. K. Chatterjee, and H. W. Lam, *IEEE Trans. Electron Devices* **ED-32**, 258 (1985).
- ²J. R. Troxell, M. I. Harrington, J. C. Erskine, W. H. Dumbaugh, F. P. Fehner, and R. A. Miller, *IEEE Electron Device Lett.* **EDL-7**, 597 (1986).
- ³W. G. Hawkins, *IEEE Trans. Electron Devices* **ED-33**, 477 (1986).
- ⁴T. I. Kamins, M. M. Mandurah, and K. C. Saraswat, *J. Electrochem. Soc.* **125**, 927 (1978).
- ⁵N. Nagasima and N. Kubota, *Jpn. J. Appl. Phys.* **14**, 1105 (1975).
- ⁶T. I. Kamins and K. L. Chiang, *J. Electrochem. Soc.* **129**, 2326 (1982).
- ⁷D. K. Biegelsen, N. M. Johnson, D. J. Bartelink, and M. D. Moyer, *Appl. Phys. Lett.* **38**, 150 (1981).
- ⁸B. Y. Tsaur, J. C. C. Fan, G. W. Turner, M. W. Geis, D. J. Silversmith, and R. W. Mountain, *J. Appl. Phys.* **54**, 1151 (1983).
- ⁹C. V. Thomson and H. I. Smith, *Appl. Phys. Lett.* **44**, 603 (1984).
- ¹⁰Y. Wada and S. Nishimatsu, *J. Electrochem. Soc.* **125**, 1499 (1978).
- ¹¹P. Kwisera and R. Reif, *Appl. Phys. Lett.* **41**, 379 (1982).
- ¹²K. Egami, A. Ogura, and M. Kimura, *J. Appl. Phys.* **59**, 289 (1986).
- ¹³A. Bhattacharya and K. N. Ritz, *J. Electrochem. Soc.* **131**, 2143 (1984).
- ¹⁴G. Harbeke, L. Krausbauer, E. F. Steigmeier, A. E. Widmer, H. F. Kappert, and G. Neugebauer, *J. Electrochem. Soc.* **131**, 675 (1984).
- ¹⁵F. S. Becker, H. Oppolzer, I. Weitzel, H. Eichermüller, and H. Schaber, *J. Appl. Phys.* **56**, 1233 (1984).
- ¹⁶L. Faraone, *IEEE Trans. Electron Devices* **ED-33**, 1785 (1986).
- ¹⁷C. H. J. Van Den Brekel and L. J. M. Bollen, *J. Cryst. Growth* **54**, 310 (1981).
- ¹⁸ASTM Standard E112-84, "Standard Methods for Determining Average Grain Size," (American Society for Testing and Materials, Philadelphia, 1984).
- ¹⁹U. Koster, *Phys. Status Solidi A* **48**, 313 (1978).
- ²⁰R. M. Anderson, *J. Electrochem. Soc.* **120**, 1540 (1973).
- ²¹R. Bisaro, N. Proust, J. Magarino, and K. Zellama, *Thin Solid Films* **124**, 171 (1985).
- ²²L. Mei, M. Rivier, Y. Kwark, and R. W. Dutton, *J. Electrochem. Soc.* **129**, 1791 (1982).
- ²³D. A. Porter and K. E. Easterling, *Phase Transformations in Metals and Alloys* (Van Nostrand Reinhold, New York, 1981), p. 263.
- ²⁴W. A. Johnson and R. F. Mehl, *Trans. American Institute of Mining and Metallurgical Engineers*, **135**, 416 (1939).
- ²⁵M. E. Fine, *Introduction to Phase Transformations in Condensed Systems* (Macmillan, New York, 1964), p. 77.
- ²⁶K. Zellama, P. Germain, S. Squelard, and J. C. Bourgoin, *J. Appl. Phys.* **50**, 6995 (1979).
- ²⁷E. N. Gilbert, *Ann. Math. Stat.* **33**, 958 (1962).
- ²⁸J. T. McGinn, H. F. Kappert, L. Krausbauer, J. M. Shaw, and A. E. Widmer, *ECS Extended Abstracts* (The Electrochemical Society, Pennington, NJ, 1983), Vol. 83-1, p. 647.
- ²⁹M. H. Brodsky, *J. Vac. Sci. Technol.* **8**, 125 (1971).
- ³⁰J. Bloem, *J. Cryst. Growth* **50**, 581 (1980).
- ³¹M. K. Hatalis and D. W. Greve, *IEEE Electron Device Lett.* **EDL-8**, 361 (1987).