Solar Energy Conversion

THE SOLAR CELL

(SECOND EDITION)

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CHAPTER VI: SOLAR CELL CONFIGURATION AND PERFORMANCE

Introduction

The nature of the solar spectrum was described in Chapter II. In Chapter IV we discussed the maximum energy that was potentially available for conversion to useful electrical energy within a solar cell--as a function of the energy gap of the semiconductor employed. In Chapter V we discussed the effects, on solar cell performance, of solar cell internal series resistance and internal junction biasing. This was done in a general way by assigning values of saturation current, J_S, and diode loss factor, K', to solar cells as a function of the semiconductor energy gap. The later portions of Chapters IV and V also considered the effects of bulk and surface recombination on the potentially available photocurrent and output power from solar cells.

The characteristics of pn and heterojunction solar cells depend primarily on the properties of the semiconductor(s) employed. The most important semiconductor property in these cases is, clearly, the width of the energy gap. When Schottky junction or mos solar cells are employed, the barrier height, which is a function of the semiconductor and metal employed, is of prime importance. For all types of solar cells the charge carrier mobility and lifetime play major roles in overall performance. Both the collection/separation of electron-hole pairs (and, hence, the photocurrent) and the internal series resistance depend on the design philosophy of the solar cell and upon the techniques used in its construction.

In this chapter we will consider various solar cell optical orientations and construction techniques. With specific semiconductors as examples, we will determine solar cell series resistance, saturation current, optimum junction voltage, maximum power density delivered to the external load, and the value of the optimized external load. This will be

done assuming room temperature (300°C) operation. The net result will be a set of design relationships, indicating the potential output for solar cells of various types, as well as providing the reader with an appreciation of the various design trade-offs.

In keeping with the discussions of Chapters IV and V, let us select semiconductors with energy gaps lying between 1.0 and 1.8 electron volts. From these earlier discussions, we shall consider only single crystal semiconductors*. As earlier, let us select a number of semiconductors as specific examples, indicated in Table VI.1.

Table VI.1

Example semiconductors

Semiconductor	Symbol	Energy Gap at 300°C (eV)
Silicon	Si	1.106
Indium Phosphide	InP	1.35
Gallium Arsenide	GaAs	1.42
Cadmium Telluride	CdTe	1.50
Aluminum Antimonide	AlSb	1.58
Cadmium Selenide	CdSe	1.70

The preceding table of semiconductors does not exhaust the list of possibilities. It does, however, span the range of energy band gap widths which is considered to be most promising and provides a distribution of single element and compound semiconductors with a broad distribution of available technology and potential performance and problems. Clearly any one of these materials is also a potential semiconductor in a heterojunction or Schottky barrier solar cell. For example, GaAs has been

* Besides the additional complexity involved in the analysis of polycrystalline based solar cells, single crystal based solar cells exhibit a higher operating efficiency. We will, in a later chapter, consider amorphous and polycrystalline semiconductor based solar cells.

used for some time as the substrate semiconductor in a GaAs-AlGaAs heterojunction solar cell [1-3] and the other materials have been used as well [4-8].

Let us now proceed to a discussion of design philosophy and construction technology as applied to solar cells made from these example materials.

Optical Orientation

Light can enter a solar cell from a number of directions. Consider a pn junction or heterojunction solar cell. In Figure VI.1 we display three general configurations of solar cell-light interaction. In the top illustration of Figure VI.1 the solar cell is securely mounted on a heat sink. This heat sink also acts as an electrical contact to the larger of the two regions of the solar cell, the substrate. The light enters the solar cell via the other region, the "front layer". Metallic contacts to the upper region mask portions of the solar cell and thereby reduce the effective optically absorbing area. The middle illustration of Figure VI.1 presents a second configuration, known as the vertical configuration. Here, the light enters the solar cell unhampered by the presence of metallic contacts. The electrical contacts are at the non-illuminated ends of the solar cell and the junction is both parallel to the incoming light and vertical, in orientation, to the heat sink. Note that care must be taken to insure that the heat sink does not short out the pn junction. This limits the effectiveness of this configuration of solar cell.

There are two types of inverted configuration solar cell, displayed in the bottom illustration of Figure VI.1. In one case, there are electrical contacts on the illuminated surface, a situation which restricts the photon input. In the other inverted configuration the electrical contacts are on the down side and do not interfere with the passage of photons. In both instances the inverted configuration solar cell has a heat sink which is on the non-illuminated side and is positioned very close to the junction of the solar cell. This positioning assists in maintaining junctions at a low temperature and, as we will see, enhances the operating efficiency. Note that, if the electrical contacts to both solar cell regions (substrate and "front layer") are on the lower or heat sink side, it is necessary to configure the electrical contacts and heat sink in order to avoid shorting the junction.

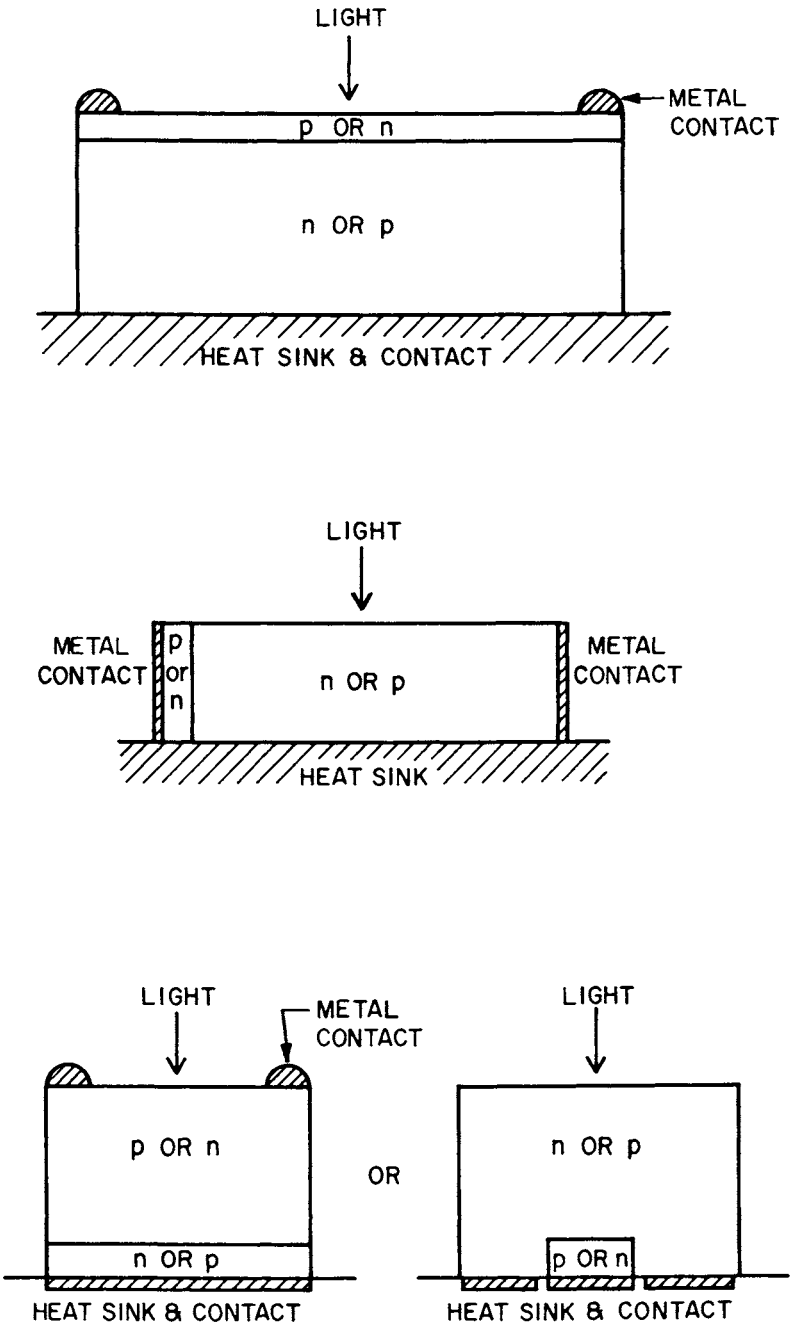


Figure VI.1. PN and heterojunction solar cell-light configurations.

Figure VI.1 is drawn for a pn or heterojunction cell with two semiconductor regions per solar cell. If we replace the thinner of the two regions by either a thin metal or thin metal-oxide layer, the same optical configuration classifications can be seen to apply to Schottky and mos cells. For standard configurations, it is clear that care is required to form metal layers thin enough to pass light and thick enough to carry current.

Before any numerical computations are made, consider some of the advantages and disadvantages of each configuration of solar cell. The standard configuration (top illustration of Figure VI.1) solar cell is simple to construct and has good contact from solar cell to heat sink. This last item is important for all semiconductor solar cells and, most particularly so, in terms of those systems where optical concentration is employed to increase the intensity of the photon flux. Recall, from Chapter V, that the saturation current density for the four types of junctions (pn junction, heterojunction, Schottky junction and mos junction--Equations V.2, V.17, V.19 and V.21). In every case, for every junction type, the saturation current density rises sharply with increasing temperature. From Equations V.31 through V.33 an increase in saturation current density results in a decrease in the solar cell delivered power density. Since practical solar cell efficiencies are rarely in excess of 25% this means that some 75%, or more, of the solar energy (~80 mW/cm^2 under AM1 conditions) is converted into heat within the semiconductor. This heat must be removed from the solar cell to avoid further increase in the operating temperature.

The standard configuration solar cell has a number of drawbacks as well. Once the electron-hole pairs are generated, they must be split into their component electrons and holes and the individual charge carriers must be collected by the junction. In the upper, or "front layer", the charge carriers must flow laterally to the electrical contacts. This upper region is a very thin (optically transparent) conductor (or semiconductor). Because this upper region is of low lifetime*, it acts, in part, as a "dead layer" (see Chapter IV). To minimize the loss of photon generated charge carriers in this "dead layer" we must make it thin. This thinness creates high internal resistance with attendant decreased power performance. This drawback is particularly severe in Schottky barrier and mos solar cells.

* This low lifetime is the result of the construction techniques employed. We will consider these techniques later in this work.

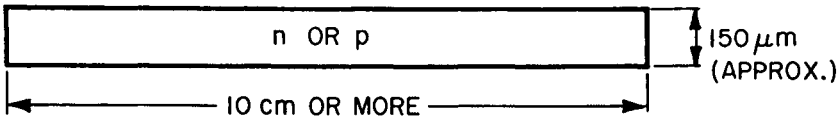
PN junction solar cells also show ill effects from this phenomenon, but heterojunction solar cells avoid the problem by constructing the "front layer" of the solar cell of a semiconductor which is optically transparent. This advantage is, in turn, counterbalanced by excess recombination at the heterojunction proper and by a more complicated fabrication technology. Another major drawback in standard configuration solar cells is the presence, on the illuminated surface, of the thick metal electrical contacts (the thickness is required to minimize the series resistance). This results in a reduction of the produced photocurrent.

The vertical configuration solar cell can be very well heat sunk, has no metal on the optical surface to reflect light and reduce optical input and photocurrent, and possesses a major circuit advantage. In Chapter V the low voltage output of solar cells was discussed in connection with the need for "stacking" or series connecting solar cells in order to obtain practical operating voltages (12 to 24 volts). The vertical configuration solar cell is particularly suited to stacking. The principal disadvantages of vertical solar cells are: (1) the need to passivate (protect) the large illuminated surface (which, in this configuration contains one "end" of the junction) from ambient conditions* and (2) the large number of electron-hole pairs generated at some considerable distance from the junction. When remote carrier generation occurs, the likelihood of charge carrier separation by the junction is reduced, decreasing the photocurrent. Both of these problems arise from the methods required for construction of a vertical solar cell.

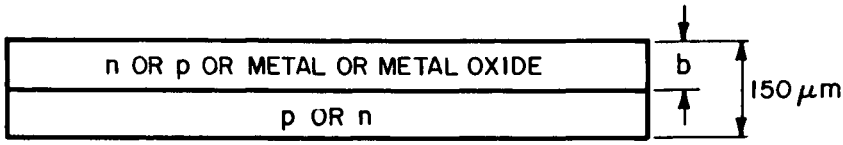
Referring to Figure VI.2, note that a vertical solar cell is often fabricated as one would construct a standard configuration solar cell--by taking a large slice of semiconductor# and placing a junction parallel to one side. A standard configuration solar cell would next be mounted on a heat sink and the "front layer" electrical contacts applied. In a vertical solar cell, the large slice is now diced into a large number of small cells (see Figure VI.2c). The small solar cells are rotated through 90° and

* The incoming photons are absorbed close to the illuminated surface and the passivation is required to minimize surface recombination and saturation current, and so to maximize the photocurrent.

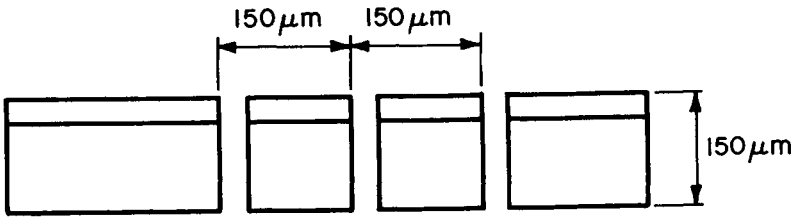
Presently, the slices of semiconductor are circular with diameters of some 15 to 20 centimeters. Other shapes and sizes will be discussed in a later chapter.



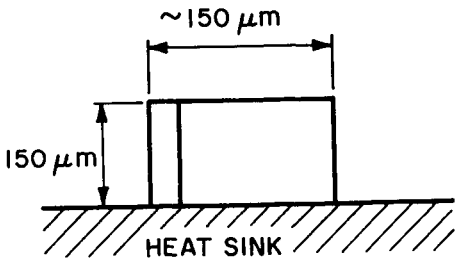
(a) A large slice, rectangular or round, of semiconductor



(b) Slice of semiconductor after junction fabrication



(c) Separation of slice into individual cells, two of which are detailed



(d) Attachment of vertical solar cell to heat sink

Figure VI.2. A brief outline of the fabrication process for a vertical configuration solar cell. In Figure VI.2b dimension b is between one and 10 μm for a heterojunction solar cell, less than one for a pn junction and on the order of 500 Å for Schottky or mos solar cells.

mounted upon a heat sink--very carefully, to avoid shorting the junction. The passivation and antireflection coating must now be applied to the illuminated surface. The size of a completed vertical configuration solar cell is dictated, in part, by the discussion in Chapter IV. There it was noted that a solar cell need only be some 150 μm thick, in the direction parallel to the incoming photons, to absorb in excess of 95% of the incoming optical energy. Any increase in thickness beyond this value increases construction cost with little or no corresponding increase in electrical power produced. Any decrease in thickness makes for substantially increased handling difficulty during fabrication, as a result of the fragile nature of semiconductors. This increases the cost of fabrication while diminishing the output power. The length of a vertical solar cell, in a direction at right angles to the photon flux, is limited by the mobility and lifetime of the minority charge carriers. Direct energy gap semiconductors have low minority carrier lifetimes and, as a result, hole-electron pairs generated far from the junction have a low probability of separation and collection.

The inverted solar cell configurations in the lower illustrations of Figure VI.1 have the advantage that no "dead layer" exists near the illuminated surface. The two types of inverted configurations presented represent two approaches to solving circuit, optical and thermal difficulties. In one, the contacts to the bulk (or substrate) region are on the illuminated surfaces. This reduces the optically absorbing area and increases the difficulty encountered in electrically "stacking" the solar cells to achieve higher system voltage, but does improve the heat sinking of the solar cell. The other approach places both sets of contacts on the down side, reducing "stacking" and photon collection problems, but making assembly more expensive and increasing the difficulty of adequately heat-sinking the solar cell.

In this chapter we will examine both standard and inverted configurations in detail, making use of our six example semiconductors. The results may be extended quite simply to vertical solar cells, provided that the semiconductor has sufficient lifetime and the charge carriers possess adequate mobility to enable them to reach the electrical contacts. Study of the lifetime and mobility data in Appendix B indicates that silicon is, by far, the most promising material for inverted and vertical solar cells. For an second examination of inverted solar cells, the reader is referred to Lammert and Schwartz [9].

Device Design - Minority Carrier Collection

When fabricating pn junction or heterojunction solar cells of any configuration, the bulk or substrate region of the semiconductor device is lightly or moderately doped with impurities while the second region (the top or "front layer" or illuminated region in a standard configuration cell, the bottom or non-illuminated region in an inverted solar cell and a thin, side-illuminated region in a vertical solar cell) is heavily doped. This heavy concentration of impurities is required to reduce the series resistance of the solar cell and to permit ohmic contact to be made to this region. Note that the large impurity concentration reduces the carrier lifetime and creates a "dead layer". This "dead layer" is not a problem in inverted or vertical configuration solar cells, but is of major concern for standard configuration solar cells. Therefore, for reasons of cost (the thicker a region of a solar cell, the greater the expense of fabrication) and, in standard solar cells, to minimize the "dead layer" width, it is desirable to keep this second region to minimum thickness.

From Chapter III we have the following expressions for the extent of the junction electric field into the p- and n-regions of a pn step junction solar cell.

$$x_n = \sqrt{\{2\epsilon V_D/qN_D\}}\ \sqrt{\{1/(1 + N_D/N_A)\}}\ ,$$

and (VI.1)

$$x_p = (N_D/N_A)x_n\ ,$$

where x_n is the space charge region expansion distance into the n-region from the junction (taken as $x = 0$), x_p is the expansion into the p-region, ϵ is the permittivity of the semiconductor, N_D is the impurity concentration in the n-region, and N_A is the impurity concentration in the p-region. The quantity, V_D, is the net voltage across the junction and is given by:

$$V_D = V_B - V_p\ , \qquad \text{(VI.2)}$$

where V_p is the photovoltage and V_B is the built-in voltage across the step junction and is determined from:

$$V_B = (kT/q)\ln\{N_A N_D/n_i^2\} \ , \qquad \text{(VI.3)}$$

where k is Boltzmann's constant, T is the absolute temperature of the junction and n_i is the intrinsic carrier concentration*.

Consider a pn step junction with $N_L >> N_S$#. In this situation, the value of X_L', the space charge (or electric field) width in the "front layer" will be zero (see Equation VI.1). In a heterojunction solar cell this is also effectively the case since the difference in energy gap widths for the two materials forces the electric field to expand only into the semiconductor with the lower energy gap. In metal/semiconductor or metal-oxide/semiconductor junctions the electric field also expands principally into the semiconductor substrate layer. The value of X_S, the space charge width in the substrate, is, at most, X_S', where:

$$X_S' = \sqrt{\{2\epsilon E_g/qn_i\}} \ . \qquad \text{(VI.4)}$$

Here, X_S' has been calculated assuming a built-in voltage equal to the band gap width of the semiconductor and a carrier concentration equal to the intrinsic value, n_i.

Table VI.2 presents a value of X_S' for the six sample semiconductors.

Table VI.2

Maximum extent of the junction electric field (the depletion or space charge layer), X_S'

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
X_S' (cm)	0.031	0.891	2.08	3.45	19.66	53.1

* From Chapter V we expect a positive value for the photovoltage when a solar cell is converting solar to electrical energy.

Here N_L refers to the "front layer" (which is the illuminated layer in standard configuration solar cells) and N_S refers to the substrate region (the illuminated region in an inverted solar cell). One of these two regions will be n-type and the other will be p-type.

Note that, under the assumptions made, this electric field (the depletion region) extends into the semiconductor in mos and Schottky junctions, into the smaller energy gap semiconductor in heterojunctions, and into the lightly doped substrate region in pn step junctions. Recall, also, that we are considering solar cells having a practical total thickness of 150 μm*. The electric field width as given in Table VI.2 is sufficient to completely fill the substrate region for all standard, vertical and inverted configuration solar cells. However, Table VI.2 is based on three assumptions; none of which can be fully realized in a realistic solar cell. The first assumption is that the substrate is intrinsic. In practice, the technology of the early 1990s cannot meet this requirement. A reasonable technology limited minimum value for N_S is on the order of $10^{14}/cm^3$. Moreover, in order to lower the saturation leakage current of the solar cell diode, N_S generally needs to be on the order of $10^{15}/cm^3$. The second assumption is that the junction voltage is only the built-in voltage of the step junction and is equal to the energy gap of the pn junction (or the energy gap of the substrate semiconductor in a heterojunction, mos or Schottky barrier solar cell. In practice, the junction voltage is always less than the energy gap width (see Equation VI.3). A third factor that must be included in any discussion of the substrate depletion layer width is that the solar cell becomes forward biased, owing to the separation/collection of the hole-electron pairs. As a result, the voltage, V_D, in Equation VI.2 is reduced, rapidly, towards some fraction of a volt#.

To estimate the junction voltage that actually exists in a Schottky barrier solar cell, consider the maximum built-in potential, ϕ_{Bo}, for a Schottky barrier solar cell. Given this value, we can substitute for V_B in Equation VI.2, and so determine the depletion layer thickness, for built-in voltage alone (i.e., for short circuit conditions), X_{SS}:

$$X_{SS} = \sqrt{\{2\epsilon\phi_{Bo}/qN_S\}} \ . \qquad \text{(VI.5)}$$

* This thickness is almost entirely due to the semiconductor in mos and Schottky junctions, the smaller energy gap semiconductor in heterojunctions and the lightly doped semiconductor substrate in pn step junctions.

Examples, using the six sample semiconductors, to be worked later in this chapter and in subsequent chapters, will demonstrate the exact values to be expected.

Table VI.3 presents values of Schottky barrier voltages for the six example semiconductors under consideration and selected metals.

Table VI.3

Metal-semiconductor barrier energies, ϕ_{Bo}, in eV for the six example semiconductors (10-15)

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
Metal		n-type semiconductor				
Pt	0.90	0.60	0.84	0.76	0.60	0.37
Au	0.80	0.52	0.90	0.71	0.51	0.49
Ag	0.78	0.54	0.88	0.81	0.52	0.43
Al	0.72	0.51	0.80	0.76	------	0.36
Pd	0.81	0.55	0.85	0.74	0.55	0.42
		p-type semiconductor				
Pt	-----	0.74	0.48	0.75	0.58	-----
Au	0.34	0.76	0.42	0.73	0.55	-----
Al	0.58	-----	0.67	0.54	-----	-----
Ti	0.61	0.74	0.53	-----	0.53	-----
Cu	0.46	-----	-----	-----	0.44	-----

Observe that the barrier values listed in Table VI.3 depend upon the metal, the semiconductor, and upon the semiconductor type. The values provided are all less than one volt and are less than the energy gap.

The mos junction is less well understood than the Schottky junction. As of 1993, this solar cell type has been constructed primarily on silicon because of the ease in fabricating the required thin oxide layer (see Chapter V) with this semiconductor. For this type of barrier, values of barrier energy of 0.85 (aluminum-silicon dioxide-on p-type silicon) and 0.67 (chromium-silica-on p-type silicon) have been reported [16]. Data from other sources [17-20] for mos barriers on both silicon and gallium arsenide substrates indicate similar values. Note that reduced leakage currents, resulting from the oxide layer, make these devices promising; even if, as yet, insufficiently understood.

The purpose of this chapter is to estimate the efficiencies of solar cells of "practical" construction. To this end, let us consider Schottky

and mos junctions under a single heading (Schottky) and select the "best" barrier energies from Table VI.3 and the literature. Then, the maximum barrier energies to be encountered, in practice, for Schottky junctions may be taken as those in Table VI.4.

Table VI.4

Practical maximum Schottky junction barrier energies (eV) and the specific metal employed for the six example semiconductors

Semiconductors	Si	InP	GaAs	CdTe	AlSb	CdSe
			n-type semiconductor			
Energy	0.90	0.60	0.90	0.81	0.60	0.49
Metal	Pt	Pt	Au	Ag	Pt	Au
			p-type semiconductor			
Energy	0.95	0.76	0.67	0.75	0.58	*
Metal	Hf	Au	Al	Pt	Pt	*

To compute pn junction built-in potentials we utilize Equation VI.3. As stated earlier, the minimum potential value for substrate impurity concentration, N_S, is an impurity concentration of $10^{14}/cm^3$. The value for the "front layer" concentration, N_L, depends, in part, on whether this region is introduced by diffusion or ion implantation. An effective value for N_L of $5 \times 10^{19}/cm^3$ is commonly encountered. Combining these values, with those for n_i^2 at 300°K from Chapter III, we have for the built-in voltage, the values of Table VI.5.

It is difficult to predict the effective barrier potential of a heterojunction. A rough estimate may be effected by observing the open circuit voltage of a heterojunction solar cell. From Sreedhar [21] and Sahi

* In Chapter III we discussed the fact that p-type CdSe has not been practically fabricated to date. Thus, neither metal-semiconductor (Schottky) junctions on p-type CdSe nor CdSe pn junctions are feasible. It is possible to construct heterojunction devices using n-type CdSe as one side of the junction. The values given in Table VI.6 are estimates for this case.

Table VI.5

Estimated practical maximum built-in voltages for pn junctions constructed from the example semiconductors (in volts)

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
V_B	0.76	1.08	1.18	1.23	1.41	*

and Milnes [22] some values of open circuit heterojunction solar cell voltages are: (1) n-type GaP on p-type Si, 0.67 V; (2) n-type GaP on p-type GaAs, 0.82 V; (3) p-type GaP on n-type GaAs, 1.05 V; and (4) n-type ZnSe on p-type GaAs, 0.925 V. Note that these values are on the order of those of Table VI.5 for pn junctions. Calculations of substrate depletion layer width using these barrier voltages lead to results similar in magnitude to those using of the results of Table VI.4 in Equation VI.5 for Schottky and Table VI.5 in Equation VI.3 for pn junctions.

For a substrate impurity concentration of $10^{14}/cm^3$ we can obtain an estimate of the substrate depletion layer width in a solar cell under short circuit conditions (the photovoltage equal to zero). These depletion widths, for the example semiconductors are given in Table VI.6.

Table VI.6

The "practical" maximum depletion layer width (in μm) in the semiconductor substrates for the six example semiconductors, as a function of the various junction types and at a temperature of 300°K

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
Metal-semiconductor barrier on n-type semiconductor substrate						
	3.457	3.049	3.547	3.126	2.703	2.398
Metal-semiconductor barrier on p-typ semiconductor substrate						
	3.552	3.432	2.983	2.999	2.657	*
Step pn junction or heterojunction						
	3.192	4.093	4.036	3.860	4.129	4.21

* P-type CdSe is not available so there is no Schottky barrier on p-type CdSe, but there can be a heterojunction in an n-type semiconductor.

Observe that the depletion layer widths of Table VI.6 are not only very much smaller than the electric field widths of Table VI.2, but they are also much less than the optical absorbing thickness of the semiconductor (~150μm). If electron-hole pair separation/collection depended solely on the depletion layer width, the performance of standard and inverted configuration solar cells would be largely negated. Fortunately, there are other phenomena which can assist in the production of photocurrent. These phenomena are used to bring the optically generated carriers within range of the electric field in the depletion layer of a solar cell junction. First, consider the diffusion length in a semiconductor and to what extent it effectively extends the collecting range of the depletion layer.

Once generated by photon absorption in the bulk regions (areas of no electric field) of the solar cell, hole-electron pairs move randomly through the semiconductor. Should there be a junction in the semiconductor crystal, there will be, of course, an electric field in the vicinity of the junction. This field serves to collect electron-hole pairs and to separate them, thus producing a concentration gradient in electron-hole pairs. Now consider the p-type region of a solar cell. Electrons in this region, close to the depletion region often, randomly, move into the electric field. When this occurs, the electrons are accelerated across the junction to the n-type side. A similar process occurs, of course, to the holes randomly moving on the n-type side as they are accelerated towards the p-type side. The effect of this minority carrier removal is to create an electron concentration gradient between the bulk region on the p-type side and the edge of the depletion region. Thus, an electron within a diffusion length of the junction on the p-type side will be collected (the same goes for holes within a diffusion length of the junction on the n-type side). The diffusion length, L, is given by:

$$L = \sqrt{\{D\tau\}} \ , \qquad \text{(VI.6)}$$

where, from Chapter III:

$$D = \{kT/q\}\mu \ . \qquad \text{(VI.7)}$$

The lifetimes, τ, and mobilities, μ, for the semiconductors being used as examples in this work were discussed in Chapter III. Recall that these material properties are functions of temperature and impurity

concentration. In this chapter we are considering solar cell operation at room temperature (27°C). The preceding discussion of depletion layer width used a substrate impurity concentration of $10^{14}/cm^3$ and a high impurity concentration "front layer" of 5 x $10^{19}/cm^3$. A few additional words concerning the "practicality" of these concentrations are in order. The "front layer" concentration varies with distance into the semiconductor. If the "front layer" is the result of a diffusion process, the impurity concentration at the surface is much higher than that at the junction. Typically, $N_L(x)$ will follow an error function curve [23, 24] with a surface concentration well in excess of either the conduction band or the valence band density of states (see Appendix B and [25]). If the "front layer" is the result of ion implantation, the impurity density reaches a peak at some distance into the semiconductor; the distance determined by the semiconductor, its crystal orientation, the impurity species and the energy of the implant [26]. Utilizing modern technologies, such as molecular beam epitaxy [27, 28], it is possible to keep the "front layer" concentration at approximately the density of states level, which is roughly 5 x $10^{19}/cm^3$. This impurity concentration is high enough to adversely affect the lifetime of the "front layer", but it also is high enough to support a thin "front layer" without excessive resistance.

The substrate impurity concentration must be small in order to enhance the diffusion length and the depletion layer width, but needs to be sufficiently high to reduce the bulk series resistance of the solar cell. This bulk series resistance, r_D, is given by:

$$r_D = \{l/A_D\}\{1/q\mu_{Sm}N_S\} \ , \qquad \text{(VI.8)}$$

where l is the length of the substrate (generally taken to be 150 μm in this work); A_D is the junction area of the solar cell, which we assume is equal to the cross-sectional area of the substrate; μ_{Sm} is the substrate majority carrier mobility; and N_S is the impurity concentration in the substrate. In Chapter V, in connection with saturation current, we used a substrate impurity concentration of $10^{16}/cm^3$. This produced a low value of saturation current density. Earlier in this chapter we utilized a substrate impurity concentration of $10^{14}/cm^3$ because this value yields a wider depletion layer width, at the cost of increased saturation current density. In practice, a carrier concentration of approximately $10^{15}/cm^3$ provides a satisfactory balance between series resistance, diffusion length, saturation current and processing technology.

Using a value of N_S equal to $10^{15}/cm^3$ and a value of N_L equal to $5 \times 10^{19}/cm^3$, in conjunction with the mobilities and lifetime values of Appendix B, the literature and Chapter III, we have the data provided in Table VI.7. This will be used as input for the computation of the minority carrier diffusion lengths in the substrates of solar cells made from our example semiconductors.

Table VI.7

Estimated values of impurity concentration, minority carrier mobility and lifetime, as functions of semiconductor for a temperature of 300°K and the six example semiconductors [22, 29, 30]

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
"Front Layer"						
Concentration (cm^{-3})	- - - - - - - - - - - - - - 5×10^{19} - - - - - - - - - - - - - -					
	"front layer" mobility (cm^2/volt-second)					
p-type layer	135	450	1000	700	140	-----
n-type layer	80	150	100	50	180	450
	"front" layer lifetime (seconds)					
p-type layer	10^{-7}	10^{-10}	10^{-10}	10^{-9}	10^{-10}	-----
n-type layer	10^{-7}	10^{-10}	10^{-10}	10^{-9}	10^{-10}	10^{-10}
Substrate						
Concentration (cm^{-3})	- - - - - - - - - - - - - - 1×10^{15} - - - - - - - - - - - - - -					
	substrate mobility (cm^2/volt-second)					
p-type layer	1500	3500	6500	950	200	-----
n-type layer	500	600	350	90	400	600
	substrate lifetime (seconds)					
p-type layer	8×10^{-5}	6×10^{-8}	6×10^{-8}	2×10^{-6}	1×10^{-7}	------
n-type layer	8×10^{-5}	3×10^{-8}	3×10^{-8}	1×10^{-7}	9×10^{-8}	1.5×10^{-9}

In a "realistic" solar cell, both the minority carrier mobilities and lifetimes may well be less than the values provided in Table VI.7, particularly if the processing involved in fabrication of the solar cell is substandard. However, the mobilities and lifetimes furnished in Table VI.7 are achievable and lead to the diffusion lengths of Table VI.8.

Table VI.8

Estimated minority carrier diffusion lengths for n- and p-type regions of solar cells employing the example semiconductors, at 300°K

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
		"front layer" diffusion length (μm)				
p-type layer	5.91	0.341	0.509	1.35	0.191	-----
n-type layer	4.55	0.197	0.161	0.36	0.216	0.341
		substrate diffusion length (μm)				
p-type layer	577	145	198	436	44.7	-----
n-type layer	322	42.4	32.4	30	60	9.49

From the discussion relating to "dead layer" thickness in Chapter V, the heavily doped "front layer" region in standard or vertical configuration step junction and heterojunction solar cells should be small, with a maximum thickness under a micron. Since this region has a low lifetime (see Table VI.7), and the surface recombination velocity of such heavily doped regions is high, it is unlikely that a large percentage of carriers will be collected and separated in this region. The diffusion lengths for the "front layer" provided in Table VI.8 are, therefore, adequate. The substrate, however, is another matter. For any configuration of solar cell, the electron-hole pairs will be generated by photon absorption within some distance of the illuminated surface. From Figures IV.7 and IV.8, this distance is given in Table VI.9.

Table VI.9

The approximate depth beneath the illuminated surface at which electron-hole pair optical generation ceases (μm)

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
Depth	1000	0.3	2	20	8	1

From practical considerations we have set the maximum solar cell thickness to a value of 150 μm. This results in a loss in the potentially

convertible solar energy of approximately 5% for silicon based solar cells. Note that, for the other example semiconductors, the absorption occurs so rapidly that this limited thickness of solar cell has no effect. Comparing the values of optical absorption depth in Table VI.9 with the diffusion lengths presented in Table VI.8, we see that, for 150 μm thick solar cells the diffusion lengths for all six example semiconducting materials are adequate to collect all of the optically generated charge carriers for standard configuration solar cells*.

Consider inverted and vertical configuration solar cells. From our discussions in connection with Figures VI.1 and VI.2 and Tables VI.9 it is possible, in these configurations, for optical hole-electron pair generation to take place at a distance approximating 150 μm from the junction. Considering the minority carrier diffusion lengths of Table VI.8 we note that, if the substrate is p-type, then silicon, indium phosphide, gallium arsenide and cadmium telluride have the potential of collecting almost all of the hole-electron pairs. Not all, because, even in the case of silicon with its 557 μm minority carrier diffusion length, the diffusion length in any of these example semiconductors is never more than four times the 150 μm limit. For indium phosphide and gallium arsenide, the diffusion length is approximately equal to the maximum generation distance of 150 μm. In the case of n-type substrates only silicon has a sufficiently large minority carrier diffusion length, long enough to assure the collection of most of the hole-electron pairs.

There is an additional source of charge carrier loss. The illuminated surface of vertical junction configuration solar cells is formed by sectioning the original wafer (see the discussion in association with Figure VI.2). This procedure enhances the surface recombination velocity and reduces the photocurrent for these devices. Note that this problem is not so severe with inverted configuration solar cells. For this configuration of device, the fabrication process is tailored to minimize surface recombination velocity. In standard configuration solar cells the surface recombination contributes to the "dead layer" and, hence, has already been taken into consideration. Finally, note that, at the substrate contact, the surface recombination is assumed to be essentially infinity (see the discus-

* This, clearly, does not include those carriers generated by optical absorption within the "dead layer".

sion in Chapter III). This produces a minority concentration gradient in the vicinity of the substrate contact which funnels charge carriers in the wrong direction. Study of Figure VI.1 will demonstrate to the reader that this problem is unimportant for standard configuration solar cells and those inverted configuration solar cells with their substrate contacts on the non-illuminated surface. It is, however, of importance to vertical junction solar cells, resulting in a "dead layer" near the substrate contact and reducing overall performance for the solar cell.

There is a solution to all of these problems; a solution which has the additional advantage of reducing the substrate series resistance. Consider the energy-versus-distance diagram for the solar cell displayed in Figure VI.3.

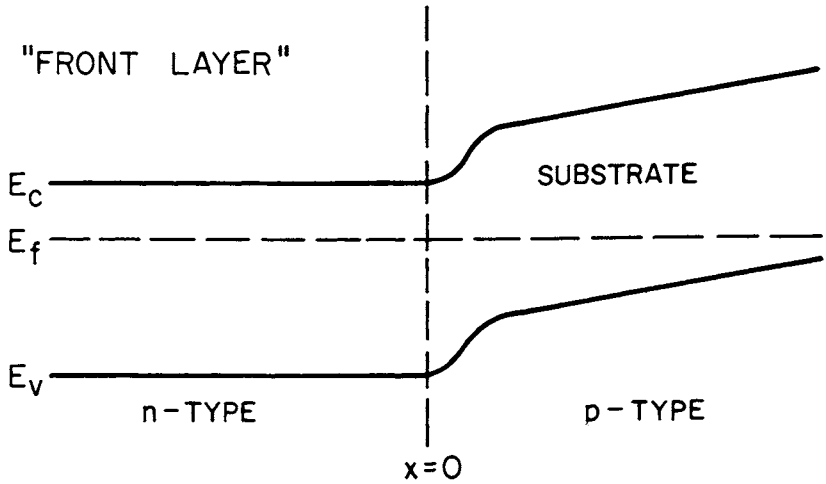


Figure VI.3. A solar cell with a variable impurity concentration in the substrate. E_c is the lower edge of the conduction band, E_F is the Fermi level and E_v is the upper edge of the valence band.

In Figure VI.3 the heavily doped "front layer" is assumed to have a constant impurity concentration of approximately $5x10^{19}/cm^3$. At x = 0 (the junction) the substrate is relatively lightly doped (an impurity concentration of approximately $10^{19}/cm^3$), but the impurity concentration (acceptor in the example of Figure VI.3) of the substrate is increased as the distance from the junction is increased. The result is a built-in electric field which impels minority carriers towards the junction. This electric

field is given by:

$$\mathscr{E}(x) = \frac{kT}{qN_S(x)} \frac{\partial N_S(x)}{\partial x} , \qquad \text{(VI.9)}$$

where $N_S(x)$ is the substrate impurity concentration. This varies from approximately $10^{14}/cm^3$ to a value on the order of 10^{17} to $10^{18}/cm^3$ (a value less than one-tenth of the effective density of states value for the substrate*). Note that if we desire a constant value of electric field, $\mathscr{E}$, then the substrate impurity concentration will be:

$$N_S(x) = N_S(o)\exp\{q\mathscr{E}x/kT\} , \qquad \text{(VI.10)}$$

where $N_S(o)$ is the substrate impurity concentration at the junction and x is positive into the substrate#.

Assume a substrate of 150 μm width. Then, for an electric field in the substrate of 16 volts/cm, the ratio $N_S(150)/N_S(o)$ is ten thousand. Given such a field, extending the width of the substrate, we can collect essentially all of the hole-electron pairs generated in the substrate and transport them to the edge of the depletion layer. In turn, the depletion layer separates the hole-electron pairs. As an added advantage, the graded substrate discussed here also serves to decouple the surface recombination velocity at the substrate contact [31-33].

Consider the photocurrent that may be expected in a solar cell of standard, inverted or vertical configuration. Suppose we have an inverted configuration solar cell, with a graded substrate, 95% efficient antireflection coating and 100% collection efficiency for all generated hole-electron pairs. The expected photocurrent density is that of Table VI.10.

In the case of a vertical configuration solar cell we must include additional losses from surface recombination owing to the fact that the

* Increasing the substrate impurity concentration above this value will decrease the minority carrier lifetime and mobility to such an extent as to decrease the collected photocurrent.

Clearly, the same procedure can be followed when the substrate is n-type.

Table VI.10

Estimated photocurrent density (mA/cm^2) in an inverted configuration solar cell at 300° K

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
AM0-conditions	44.65	41.7	37.2	35.8	28.6	26.0
AM1-conditions	36.1	31.8	28.7	27.2	21.9	20.5

surface which is illuminated has been cut from a wafer (see the discussion accompanying Figure VI.2). Assuming a reasonable surface recombination velocity of 10,000 cm/second, and using the data of Table VI.7 and Figure III.8, we can estimate that the maximum realizable photocurrent density will be some 5% or so below the photocurrents of the inverted solar cell, yielding the numbers of Table VI.11.

Table VI.11

The estimated photocurrent density (mA/cm^2) in a vertical configuration solar cell at 300°K

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
AM0-conditions	42.7	39.5	35.3	33.9	27.1	24.7
AM1-conditions	34.2	30.1	27.2	25.7	20.8	19.5

The expected photocurrent from a standard configuration solar cell is still less. There are additional recombination losses due to the "dead layer" (which is a result of the heavily doped "front layer") in pn step junctions, from the interface effects in a heterojunction solar cell and from reflection effects in the case of mos and Schottky junction solar cells. In the following table the estimated photocurrent density for a standard configuration solar cell is provided. In the case of a pn step junction, the "front layer" is thin to minimize the "dead layer" thickness (keeping this layer from 0.3 to 0.6 μm thick). The "dead" layer does not completely fill the "front layer", but comprises the top third or so. Assuming that this

"dead layer" is, indeed, totally dead, and utilizing Figures IV.10 and IV.11 the estimated maximum photocurrent density for standard configuration pn step junction solar cells is provided in Table VI.12. The estimated possible photocurrents for standard configuration heterojunctions are higher because the "dead layer" is not present--the semiconductor forming the "front layer" being transparent to the photons of interest. The photocurrent is also estimated for Schottky barrier standard configuration solar cells. The existence of a metal layer on the illuminated side of the solar cell drastically reduces the potential photocurrent and values indicated in Table VI.12 are, at best, estimates.

Table VI.12

The estimated photocurrent density (mA/cm^2) in a standard configuration solar cell, for pn step junction, heterojunction and Schottky junction devices at 300°K

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
		heterojunction solar cells				
AM0-conditions	37.95	35.44	31.62	30.43	24.31	22.10
AM1-conditions	30.68	27.03	24.40	23.12	18.62	17.42
		pn step junction solar cells				
AM0-conditions	31.77	07.02	20.88	22.54	18.45	11.25
AM1-conditions	25.02	05.67	15.75	17.10	14.04	09.18
		Schottky junction solar cells				
AM1-conditions	10.59	02.34	06.96	07.53	06.15	03.75
AM1-conditions	8.34	01.89	05.25	05.70	04.68	03.06

In studying Table VI.12 it is clear that the high absorption coefficient of InP results in unusually high recombination losses in step pn junction standard configuration solar cells. Also note that, for every one of the example semiconductors, there is a decline in the expected photocurrent density from inverted configuration through vertical configuration and to standard configuration. This decline is minor when vertical and inverted configuration solar cells are compared, but of major proportions when standard configuration solar cells are considered. It cannot be overemphasized that the values of expected photocurrent

density in Tables VI.10 through VI.12 are estimates and strongly dependent on the fabrication techniques employed in constructing the solar cells, upon surface crystal orientation, and on the semiconductor itself. The values listed above should be realizable, if sufficient care is exercised, but "mistakes" in fabrication technology and surface preparation can result in substantial reductions.

The overall purpose of this chapter is to provide an estimate of performance for several "realistic" situations. The heterojunction and pn step junction photocurrent density estimates of Table VI.12 are reasonable. The Schottky photocurrent density estimates are more problematic. To allow for photon penetration of the metal layer on top of a Schottky diode the layer must be very thin (<500 Å) [34]. Even so there is considerable loss due to photon reflection and the photocurrent density in such devices is small.

Device Design - Saturation Current

The saturation current densities for solar cells depend on the type of junction. From Chapter V and the discussions in Appendices B and C we have for the saturation current, J_S, in pn step junction solar cells:

$$J_S = \frac{qD_{pn}n_i^2}{L_{pn}N_D} + \frac{qD_{np}n_i^2}{L_{np}N_A}, \qquad \text{(VI.11)}$$

where D_{pn} and D_{np} are the diffusion constants for holes on the n-side of the junction and electrons on the p-side of the junction, L_{pn} and L_{np} are the diffusion lengths for holes on the n-side of the junction and electrons on the p-side of the junction. N_D and N_A are the net donor impurity concentration on the n-side and acceptor concentration on the p-side of the junction.

The saturation current for a heterojunction is given by:

$$J_S = J_{SH} = \frac{qD_S n_i^2}{L_S N_S} X_T, \qquad \text{(VI.12)}$$

where D_S, L_S and N_S are the minority carrier diffusion constants and

diffusion length in the substrate semiconductor (the semiconductor with the smaller energy gap) and the impurity concentration in the substrate. The quantity, X_T, is used to account for internal effects at the interface between the two semiconductors (see Chapter V).

The saturation current density for a Schottky junction is:

$$J_S = J_{SS} = A^*T^2\exp\{-\lambda\phi_{Bn}\} , \qquad \text{(VI.13)}$$

where λ is q/kT and the Richardson constant, A*, is given by:

$$A^* = 120m^* , \qquad \text{(VI.14)}$$

where m* is the effective mass of the majority charge carrier in the semiconductor (see Appendix B). The quantity, ϕ_{Bn}, is the barrier voltage adjusted for image force lowering (see Table VI.4).

As discussed earlier, mos junctions are imperfectly understood at present. This being the case, further discussions of mos cells will not be conducted in this work. The reader who wishes to estimate the performance of the mos solar cell is referred to, as an introduction, [16-20, 35 and 36].

Using Equations VI.11 through VI.14 in conjunction with a substrate impurity concentration level of $3 \times 10^{15}/cm^3$, the barrier energies for Schottky barriers of Table VI.4, the carrier mobility and lifetime values of Table VI.7, the diffusion lengths of Table VI.8, the intrinsic carrier concentrations from Table III.2 and the effective mass values from Appendix B, it is possible to estimate the saturation currents for pn step junctions, Schottky junctions and heterojunctions. In the case of heterojunctions, we will assume that X_T, the interface factor, is unity. In practice, it is probable that X_T is less than unity [37] so that the estimate used here is conservative. Because the impurity concentration of the illuminated or "front" layer in a pn step junction is much larger than the impurity concentration of the substrate (by approximately four orders of magnitude), Equation VI.11 is reduced to a single term, dependent on the substrate. The estimated values of saturation current are presented in Table VI.13.

Examination of Table VI.13 in conjunction with the minimum values of saturation current density used in the preceding chapter indicates that the values of saturation current density that we may reasonably expect to encounter in practice are one to two orders of magnitude

Table VI.13

Typical values of saturation current density for heterojunctions, pn step junctions and Schottky junctions on the example semiconductors (A/cm^2). The junction temperature is 300°K. (Note that the junction value for CdSe is valid for heterojunctions only, as p-type CdSe is not available)

Semi-cond-uctor	For pn step junctions and heterojunctions p+n	n+p	For Schottky Barriers on n	on p
Si	4.50×10^{-12}	7.80×10^{-12}	9.15×10^{-9}	6.89×10^{-9}
InP	1.27×10^{-16}	2.16×10^{-16}	6.43×10^{-5}	7.58×10^{-7}
GaAs	7.20×10^{-19}	2.19×10^{-18}	6.10×10^{-5}	3.13×10^{-5}
CdTe	1.31×10^{-20}	9.53×10^{-21}	3.02×10^{-8}	9.76×10^{-7}
AlSb	1.22×10^{-21}	8.20×10^{-22}	1.01×10^{-4}	7.56×10^{-4}
CdSe	1.89×10^{-22}	----------	8.38×10^{-3}	----------

higher than the ideal minimum values for pn and heterojunctions. The saturation current densities for Schottky barrier junctions are much higher. It is possible that breakthroughs in Schottky (or mos) technology will permit lower saturation current densities and that improvements in material preparation and junction fabrication technology will, by increasing minority carrier lifetime, lower the saturation current densities for both types of pn junctions. For the present, however, Table VI.13 is a reasonable approximation.

Device Design - Series Resistance

We have arrived at estimates for photocurrent density (Tables VI.10 through VI.12) and junction saturation current density (Table VI.13). These values can now be used in Equations VI.16 - VI.19 to determine the operating junction voltage for maximum power output density, V_p', the maximum power density which is transferable to the load, P_{max}/A, the efficiency for maximum power transference, η_S, and the internal loss factor, K':

$$(\lambda V_D' + 1 + K')\exp\{\lambda V_D'\} = (J_{ph} + J_S)(1 + K')/J_S \ , \tag{VI.16}$$

$$K' = 2(r_D A_D) J_S \lambda \exp\{\lambda V_D'\} \ , \tag{VI.17}$$

$$P_{max}/A_D = \frac{(J_{ph} + J_S)(\lambda V_D')V_D'}{(\lambda V_D' + 1 + K')}(1 - (K'/2)/(1 + K')) \ , \tag{VI.18}$$

and

$$\eta_S = (P_{max}/A_D)(I_{ns}) \ , \tag{VI.19}$$

where $\lambda = q/kT$, A_D is the junction area of the solar cell (assumed to be equal to the light collecting area of the cell), J_{pn} is the photocurrent, J_S is the saturation current density, r_D is the solar cell series resistance, and I_{ns} is 135.3 mW/cm^2 under AMO conditions and 107 mW/cm^2 under AM1 conditions.

In Chapter V we assumed values of the loss factor, K' and then computed efficiencies and power output densities for solar cells. We are now in a position to make estimates of the series resistance of a solar cell, and to calculate K' directly. To do this, let us assume the geometries for solar cells of the three configurations. Probable geometries for standard and vertical configuration cells are shown in Figure VI.4.

The standard cell is assumed to be round with a light sensitive area of πa^2; a "front layer" thickness, d, of 0.4 μm for pn step junctions, 0.5 μm for heterojunctions and 0.05 μm for Schottky junctions; and a substrate thickness, T_S, of 150 μm. Vertical configuration solar cells are rectangular parallelepipeds with light collecting areas of $T_S W$, where T_S is 150 μm and W is arbitrary*; a substrate width (distance in the direction of photon travel, Y, of 150 μm; and a total thickness of barrier plus substrate contact ($d + T_S + \Delta$) of 150.4 μm. The inverted solar cell we will take to be equivalent to the standard cell turned upside down (see Figure VI.1). Following Figure VI.1, the light sensitive area for inverted

* If the procedure for making vertical cells discussed in Figure VI.2 is followed, reasonable values of W might be as large as 10 cm. Since this dimension drops out of our calculations, the precise value is unimportant.

solar cells is taken to be twice the area of the junction (assuming that both contacts for the inverted solar cell are on the down or non-illuminated side. The actual junction, then, occupies only about half of the down side).

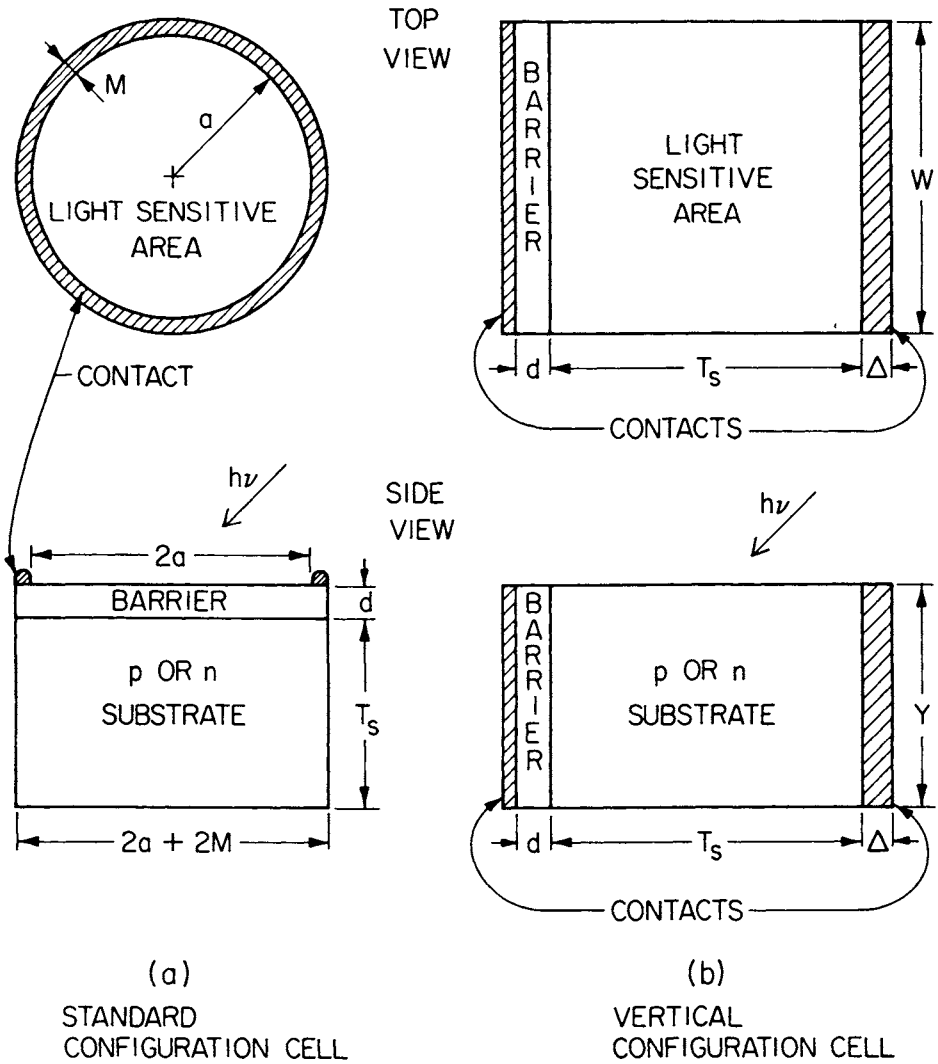


Figure VI.4. Probable standard and vertical solar cell configurations.

Note that in both the standard and vertical configurations some of the illuminated surface is obscured by the contacts on the illuminated surface. For the standard configuration solar cells the ratio of optically absorbing surface to total surface area, Φ, is given by:

$$\Phi_{standard} = a^2/(a + M)^2 , \qquad \text{(VI20a)}$$

where M is the width of the metal contact ring (see Figure VI.4). Even with a heavily doped barrier region, the metal contact ring is much better at carrying current. A practical ratio of contact area to light absorbing area is 1:10.

For vertical configuration solar cells, Φ is:

$$\Phi_{vertical} = T_S/(T_S + d + \Delta) , \qquad \text{(VI20b)}$$

where, from the preceding discussion, $\Phi_{vertical} = .997$.

For inverted configuration solar cells, the entire illuminated surface can be light absorbing; there being no contacts on the illuminated surface.

Note that, for standard configuration Schottky junction solar cells, the illuminated surface must be coated with a thin metal contact layer. This layer must be thick enough to conduct current to the metal contacts without excessive electrical resistance and thin enough to permit light to pass through it and reach the semiconductor substrate. The estimated photocurrent for this case is provided in Table VI.12.

The junction area, the area through which the current flows, is YW for vertical configuration solar cells, πa^2 for standard configuration solar cells and $\pi a^2/2$ for inverted configuration devices*. Now the series resistance of a solar cell consists of contact and lead resistance (small

* Note that the majority of the absorbed photons in a vertical configuration solar cell are absorbed close to the illuminated surface. Thus the photocurrent is generated close to the upper surface. The fact that the hole-electron pairs do spread via diffusion and the effect of electric fields does spread the hole-electron population, but the fact remains that the photocurrent does flow through a somewhat smaller area than that indicated. Lacking sufficient experimental data to predict this value exactly, we make the conservative assumption provided here.

since these are metal parts); resistance due to the substrate and resistance due to the "front layer". We will ignore the contact and lead resistance.

The substrate impurity concentration is often graded in order to improve the collection efficiency of the generated electron-hole pairs. From the discussion on this topic earlier in this chapter and using Equation VI.10, we can write for the series resistance times area product of the substrate:

$$(r_D A_D)_S = z\int_o^{T_S}[\exp\{-\lambda \mathscr{E}_S x\}/q\mu_{SM}N_{Sj}]dx \quad . \qquad \text{(VI21)}$$

In Equation VI.21, A_D is the area of the junction*, z is unity for vertical and standard configuration devices and is 0.96 for inverted configuration solar cells#. $\mathscr{E}_S$ is the electric field in the substrate region of the solar cell, μ_{SM} is the majority carrier mobility in the substrate and N_{Sj} is the impurity concentration in the substrate at the junction. Equation VI.21 is further complicated by the fact that the mobility of the carrier is a function of the impurity concentration (see data in Appendix B). Assume that the substrate thickness is 150 μm, N_{Sj} is $10^{15}/cm^3$ and $\mathscr{E}_S$ is 16 volts/cm**. From the data of Chapter III, Appendix B and using Equation VI.21, we can obtain for the approximate substrate series resistance times area product the results in Table VI.14.

The series resistance times junction area product of the heavily doped "front layer" for a vertical configuration solar cell is determined by using Equation VI.22:

---

* Recall that the junction and optically absorbing surfaces are approximately the same in vertical and standard configuration devices, while the optically absorbing surface is some twice the area of the junction for inverted configuration devices.

This factor reflects the efficiency of collection of hole electron pairs as a result of recombination on the lateral surfaces.

** For this value of substrate electric field we have seen that the substrate impurity concentration varies from $10^{15}/cm^3$ at the junction to $10^{19}/cm^3$ at the far side of the substrate. Recall that this range results from balancing the need for low saturation current (and hence high impurity concentration in the substrate) and a large extent for the electric fields produced by the junction in the substrate (and hence a low impurity concentration in the substrate).

Table VI.14

The approximate substrate series resistance times junction area $(r_D A_D)_S$ product for solar cells with a 150 μm thick substrate with an exponentially graded substrate impurity concentration ranging from $10^{15}/cm^3$ at the junction to $10^{19}/cm^3$ at the far substrate surface, at a temperature of 300°K (in ohm-cm^2)

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
		vertical and standard configurations				
n-type substrate	.0069	.0032	.0016	.0110	.0746	.0176
p-type substrate	.0192	.1033	.0294	.1127	.0258	*
		inverted configuration				
n-type substrate	.0066	.0030	.0015	.0106	.0695	.0169
p-type substrate	.0183	.0953	.0282	.1078	.0250	*

* p-type single crystal CdSe is not available.

$$(r_D A_D)_L = (\Delta + d)/(q\mu_{LM} N_L) \ . \qquad \text{(VI22)}$$

The resistance area product of the "front layer" can be easily computed using the approximation of a constant impurity concentration and the mobility values from Table VI.7. For Schottky barriers we can use the resistivity of a typical metal (approximately 5 μ ohm-cm) and find that $(r_D A_D)_L \simeq 2 \times 10^{-10}$ ohm-cm^2. For devices utilizing heterojunctions the resistance time junction area product for the "front" layer is on the order of 10^{-7} ohm-cm^2. The product for devices with pn junctions can similarly be determined, again using Table VI.7 and Equation VI.22, along with a "front layer" thickness of 0.4×10^{-4} centimeters.

Upon investigation of the "front layer" series resistance times junction area product for inverted configuration solar cells, we discover that the values are essentially of the same order of magnitude as those for the vertical configuration. These values are present in Table VI.15. Note that they are far smaller than the resistance times junction area product of the substrate region--so small as to enable us to ignore them in future calculations of solar cell performance.

In a standard configuration solar cell the "front layer" resistance times junction area product is not necessarily less than the substrate

Table VI.15

The series resistance times junction area product for the heavily doped "front layer" of vertical and inverted configuration solar cells as a function of the type of junction and at 300°K (ohm-cm^2)

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
		pn junctions				
n-type "front layer"	3.12×10^{-7}	1.67×10^{-7}	2.50×10^{-8}	3.57×10^{-8}	1.79×10^{-7}	8.33×10^{-7}
p-type "front layer"	1.85×10^{-7}	5.56×10^{-8}	2.48×10^{-7}	4.99×10^{-7}	1.37×10^{-7}	*
		heterojunctions*				
	10^{-7}	----------				10^{-7}
		Schottky junctions*				
	2×10^{-10}	----------				2×10^{-10}

* p-type single crystal CdSe is not available

area times junction product. Here, the current flows through the substrate and "front layer" to the metal contacts (See Figure VI.4). If we assume that the current flowing at the junction proper is uniformly distributed, then, from Ohm's law:

$$(R_D A_D)_L = (\rho_L a^2)/4d \ . \qquad \text{(VI.23)}$$

Equation VI.23 has been used to compute the "front layer" series resistance times junction area product for standard configuration solar cells. The data of Table VI.7 and Appendix B have been used, together with a value of d of 0.4 μm for pn junctions, ρ_L equal to 5×10^{-6} ohm-cm for Schottky metals and d equal to 0.05 μm for Schottky barriers. For a heterojunction we assume ρ_L equal to 5 μm and a resistivity of 0.01 ohm-cm [38]. Under these conditions, we have the results outlined in Table VI.16 for the "front layer" series resistance of standard configuration solar cells.

We are now in a position to determine the potential performance of the three configurations. Note that the results which we are about to determine are not intended to be the maximum potential. Rather, these

Table VI.16

The series resistance times junction area product for the "front layer" of a standard configuration solar cell as a function of the junction type and at 300°K (ohm-cm^2)

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
			Schottky junctions*			
	$0.25a^2$	----------	----------	----------	----------	$0.25a^2$
			heterojunctions*			
	$5a^2$	----------	----------	----------	----------	$5a^2$
substrate			pn junctions			
n-type	$28.94a^2$	$08.68a^2$	$03.91a^2$	$05.58a^2$	$27.9a^2$	*
p-type	$48.82a^2$	$26.04a^2$	$39.06a^2$	$78.12a^2$	$21.7a^2$	*

* p-type CdSe is not available

results are meant to indicate the "practical" output values achievable with more or less "normal" fabrication technologies. We will discuss potential, all-out, maximum output potentials later. The expected solar cell delivered power density is given by Equation V.33 where the junction voltage (the photovoltage) and loss factor for maximum power delivered (under the assumed conditions) must mutually satisfy Equations V.31 and V.32. The series resistance times junction area products for the "front layer" and substrate are provided in Tables VI.14 and VI.16. Note that for inverted and vertical configuration solar cells only the substrate series resistance is of importance. For the standard configuration solar cell, the "front layer" resistance times area product is of importance. The larger the area of the solar cell the larger the "front layer" resistance and the less expensive (within reason) it is to construct the device. For our purposes we will assume that the standard configuration solar cells are sufficiently large to exhibit a "front layer" series resistance times area product equal to one-tenth of the substrate resistance times area product. Thus, the effective resistance times junction area product for our example standard configuration solar cells is given by the substrate value from Table VI.14 times one point one. The saturation current densities for the various junction types are provided in Table VI.13. The photocurrent density for inverted configuration solar cells is taken to be 1.95 times the values in

Table VI.10 (the physical structure assumed in the discussion of this chapter leads to a degree of optical concentration equal to this value). The photocurrent density for vertical configuration solar cells is provided in Table VI.11 and the photocurrent for standard configuration solar cells lies between 0.3 and 0.9 times that of the values furnished in Table VI.12*. The solar spectra employed are AMO and AM1.

The loss factor, which depends directly on the series resistance times junction area product, for these devices is considerably less than unity. Selected values for K' are presented in Table VI.17 for standard configuration solar cells. Table VI.18 provides the loss factors for vertical configuration solar cells as a function of junction and substrate type. Table VI.19 presents the same data for inverted configuration solar cells. Note that p-type CdSe is not available. Comparison of these values of loss factor with those used in computing Tables V.2 and V.3 indicates that the assumptions used in those tables were conservative. Also note that the loss factor is higher for inverted configuration solar cells than for vertical configuration devices, which are, in turn, higher than K' values for standard configuration solar cells.

Figures VI.5 through VI.10 present values of the photovoltage, V_D', under conditions of maximum delivered power density, the maximum solar cell delivered power density, P_{max}/A_D, and η_S, the solar cell efficiency under these conditions, for standard configuration solar cells under AMO and AM1 illumination. Note that the realtively low barrier energies of the Schottky barrier solar cells, lead to high saturation current denisty and poor overall performance of Schottky barrier solar cells.

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* The physical configuration of an inverted solar cell, as described here, leads to a light collected area which is twice that of the junction. The collection of holes and electrons from the furthest distances within the solar cell is not perfect--hence the photocurrent density is 1.95 times Table VI.13. In the case of standard configuration solar cells, the necessity to make electrical contact to the illuminated surface results in a loss of at least 10% of the incoming light, owing to refection from the metal contacts. In the case of a Schottky barrier standard configuration solar cell, the requirement for a metal surface (to complete the Schottky junction) results in further decreases in the photocurrent density. Thus to determine the photocurrent density for pn and heterojunction standard configuration solar cells we multiply the values of Table VI.12 by 0.9, while for Schottky barrier diodes, we multiply by 0.3.

Table VI.17

The loss factor, K', as a function of the illumination conditions, barrier type, and substrate for six semiconductors used in standard configuration solar cells (at 300°K)

	AMO light input					
	n-type substrate			p-type substrate		
Junction	pn	hetero	Schottky	pn	hetero	Schottky
Si	.000904	.001072	.000500	.002581	.003058	.001361
InP	.000065	.000311	.000191	.002148	.010363	.002910
GaAs	.000082	.000123	.000228	.001524	.002281	.003620
CdTe	.000536	.000719	.000639	.005480	.007357	.009218
AlSb	.002833	.003712	.010524	.000969	.001269	.006453
CdSe	*	.000763	.015264	*	*	*
	AM1 light input					
Si	.000720	.000875	.000401	.002055	.002496	.001091
InP	.000053	.000239	.000163	.001747	.007955	.002413
GaAs	.000062	.000096	.000182	.001158	.001773	.002871
CdTe	.000410	.000550	.000495	.004181	.005618	.007190
AlSb	.002168	.002859	.008512	.000742	.000978	.005461
CdSe	*	.000605	.014785	* p-type CdSe is not available		

Table VI.18

The loss factor, K', as a function of the illumination conditions, barrier type, and substrate for six semiconductors used in vertical configuration solar cells (at 300°K)

	AMO light input					
	n-type substrate			p-type substrate		
Junction	pn	hetero	Schottky	pn	hetero	Schottky
Si	.001089	.001089	.001660	.003114	.003114	.004544
InP	.000316	.000316	.001724	.010468	.010468	.033751
GaAs	.000122	.000122	.000777	.002312	.002312	.013064
CdTe	.000726	.000726	.002327	.007430	.007430	.032825
AlSb	.003750	.003750	.032108	.001282	.001282	.016549
CdSe	*	.000772	.025312	*	*	*

Table VI.18, continued

	AM1 light input					
	n-type substrate			p-type substrate		
Junction	pn	hetero	Schottky	pn	hetero	Schottky
Si	.000881	.000881	.001350	.002519	.002519	.003691
InP	.000243	.000243	.001369	.008025	.008025	.026237
GaAs	.000095	.000095	.000623	.001794	.001794	.010425
CdTe	.000554	.000554	.001800	.005662	.005662	.025427
AlSb	.002894	.002894	.025687	.000990	.000990	.013570
CdSe	*	.000613	.022677	* p-type CdSe is not available		

Table VI.19

The loss factor, K', as a function of the illumination conditions, barrier type, and substrate for six semiconductors used in inverted configuration solar cells (at 300°K)

	AMO light input					
	n-type substrate			p-type substrate		
Junction	pn	hetero	Schottky	pn	hetero	Schottky
Si	.002059	.002059	.003092	.005871	.005871	.008459
InP	.000596	.000596	.003001	.019598	.019598	.061330
GaAs	.000230	.000230	.001348	.004477	.004477	.023573
CdTe	.001417	.001417	.004389	.014478	.014478	.061249
AlSb	.006915	.006915	.054453	.002454	.002454	.002759
CdSe	*	.001499	.035937	*	*	*
	AM1 light input					
Si	.001680	.001680	.002534	.004789	.004789	.006924
InP	.000458	.000458	.002376	.015009	.015009	.047348
GaAs	.000179	.000179	.001079	.003475	.003475	.018742
CdTe	.001083	.001083	.003398	.011037	.011037	.047620
AlSb	.005457	.005457	.044116	.001939	.001939	.002226
CdSe	*	.001188	.031298	* p-type CdSe is not available		

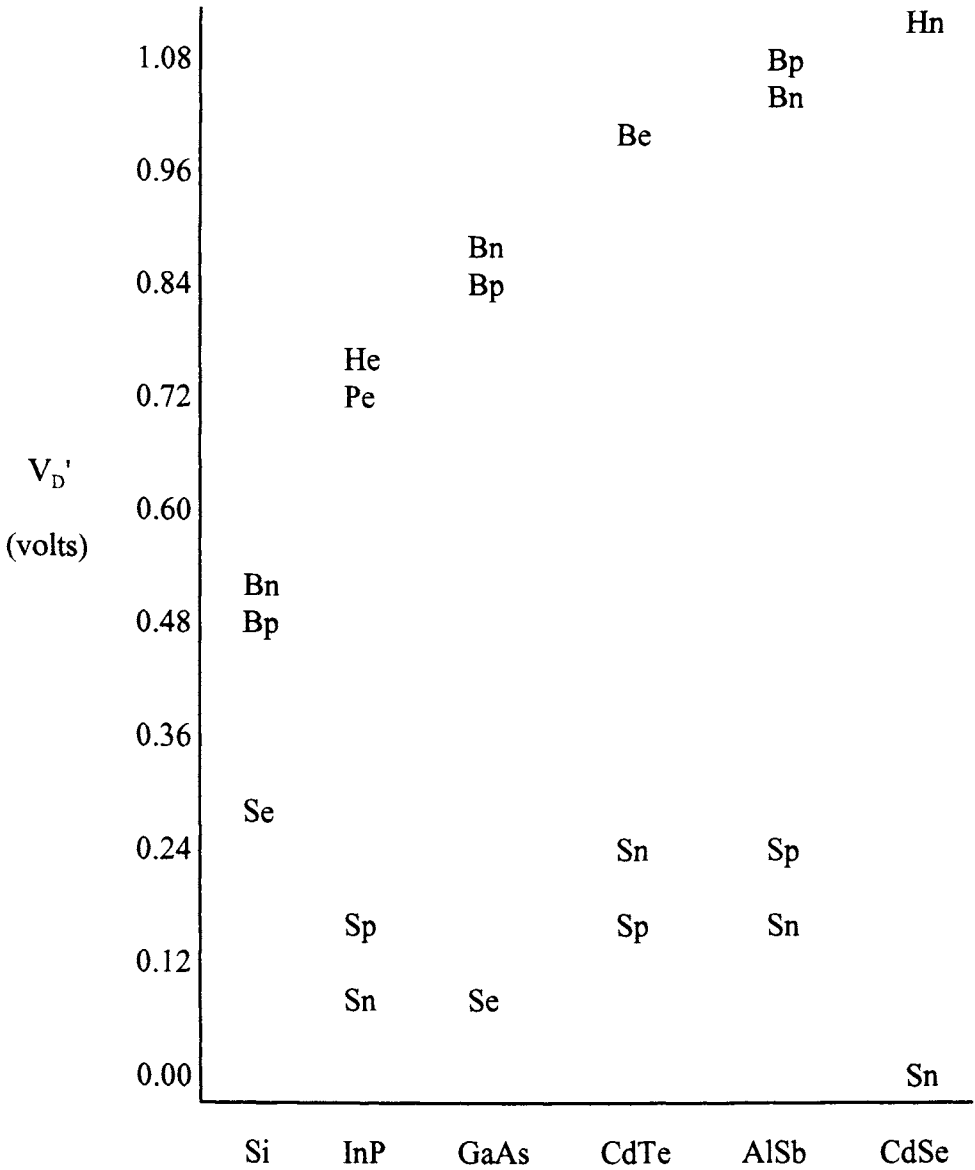

Figure VI.5. Photovoltage when the delivered solar cell power is a maximum, V_D', for standard configuration solar cells, as a function of barrier and substrate, under AMO light, at 300°K and for six example semiconductors.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

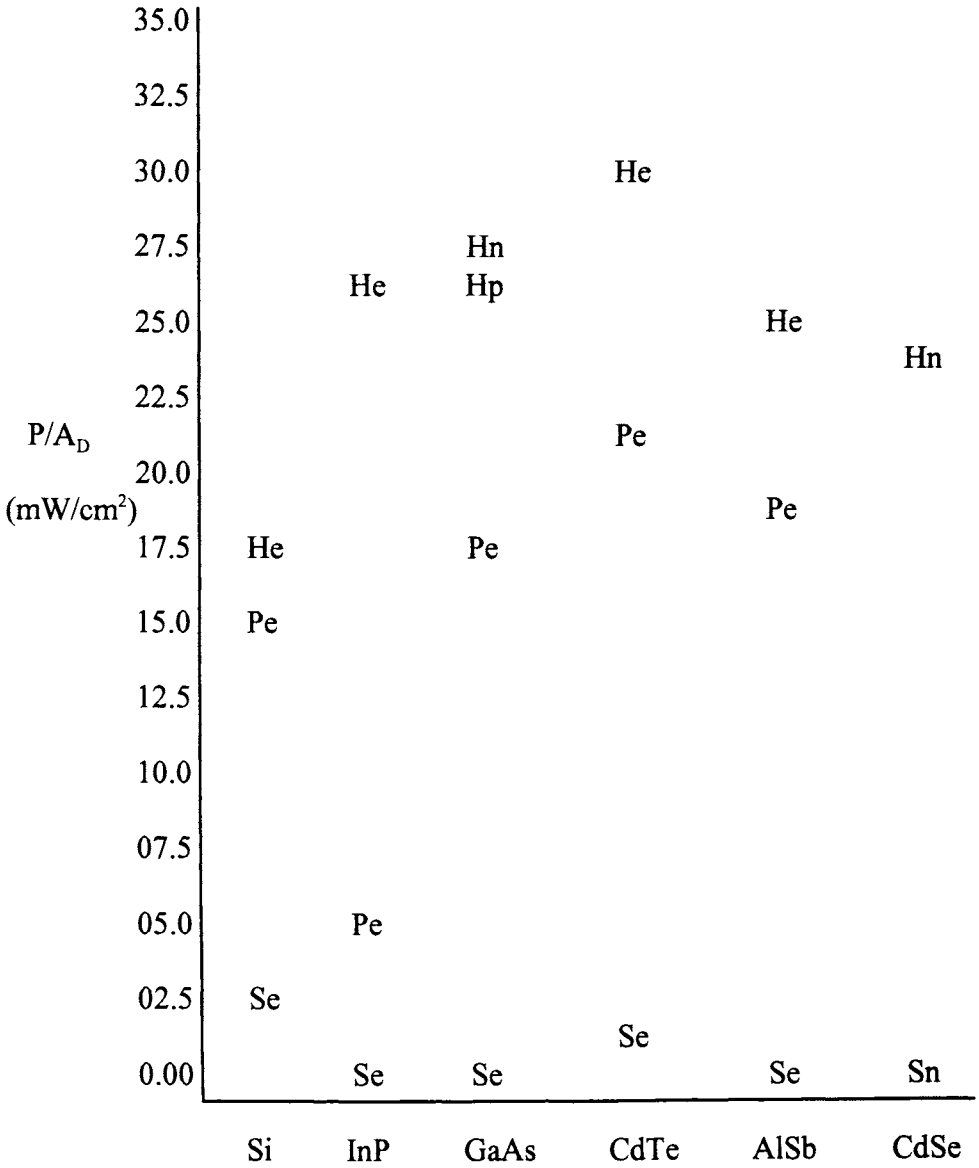

Figure VI.6. The maximum delivered power density, P/A_D, for standard configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AMO illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

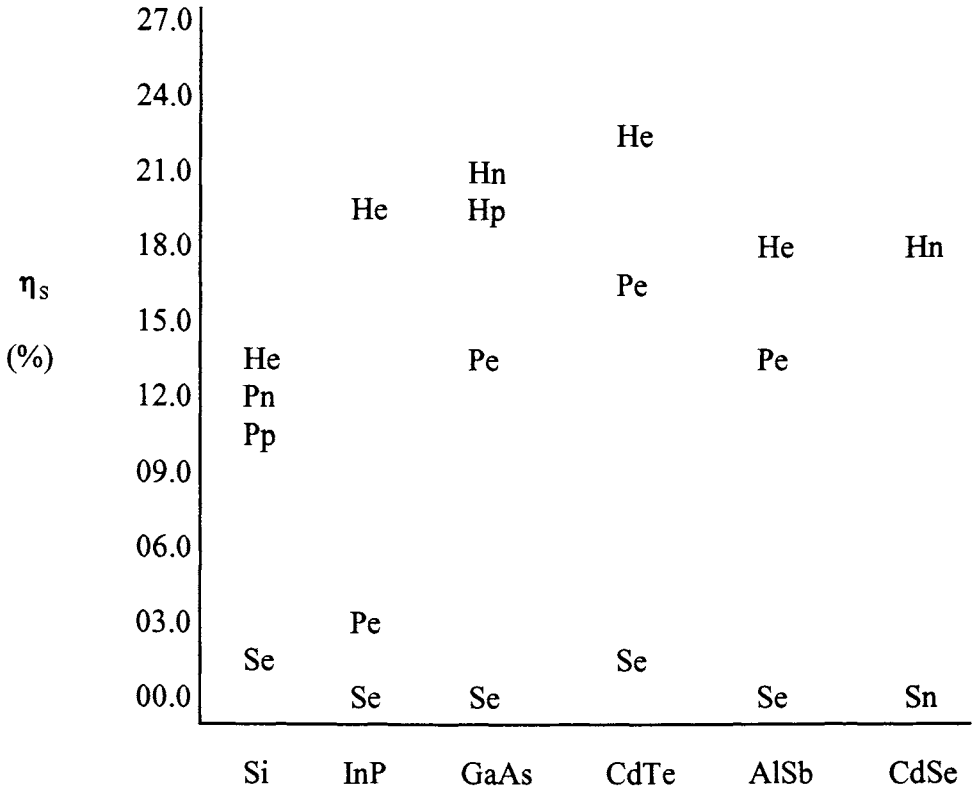

Figure VI.7. Solar cell efficiency, η_S, under the conditions of maximum delivered power density, for standard configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AMO illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

Figures VI.11 through VI.16 present values of photovoltage, maximum delivered power density and solar cell efficiency at 300°K for vertical configuration solar cells of various junction and substrate types. Note that the performance of these vertical configuration solar cells is higher than for standard configuration solar cells, partly as a result of higher effective (potentially higher!) photocurrents and partly as a result of the lower series resistance times junction area product of these solar cells. Further note that the low Schottky barrier heights result in higher saturation current density and poorer solar cell performance.

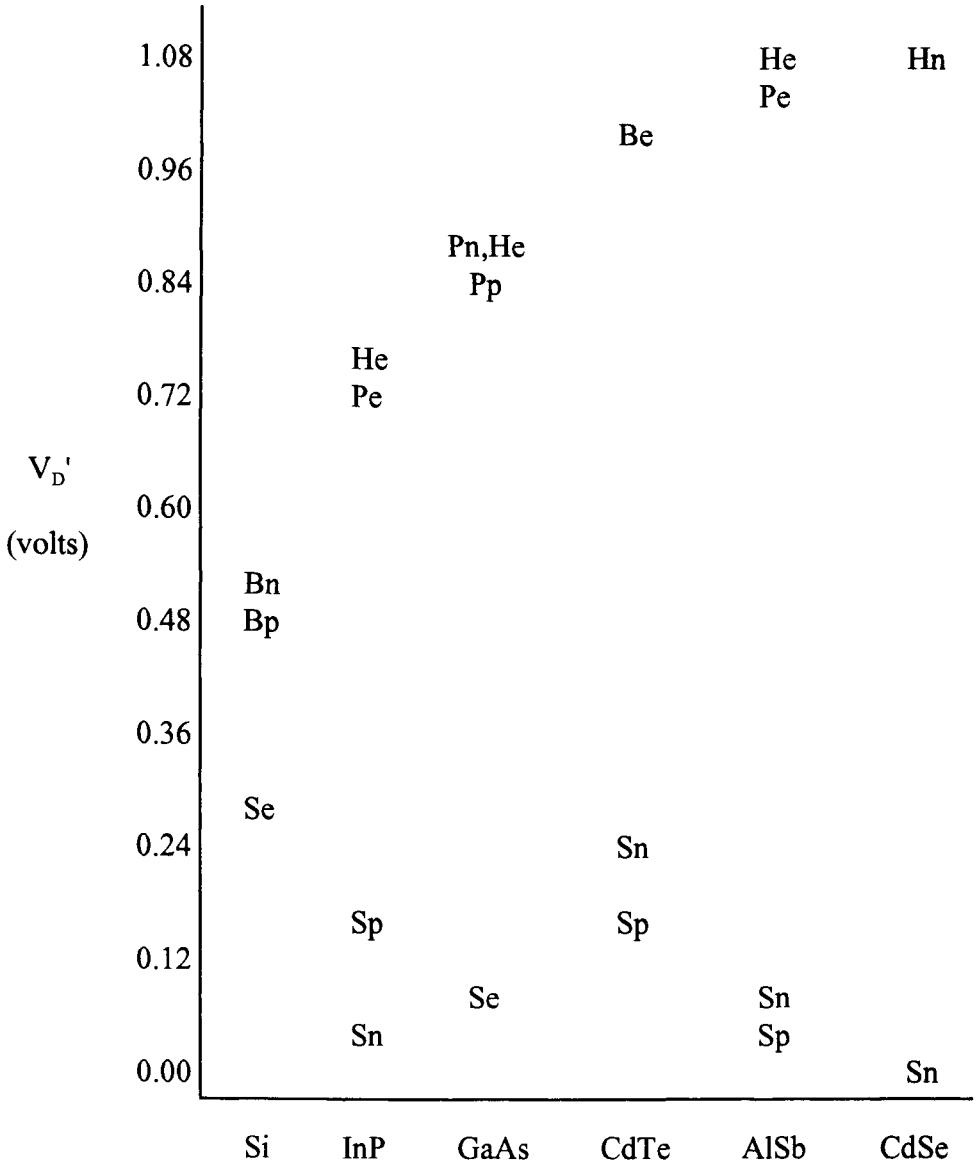

Figure VI.8. Photovoltage when the delivered solar cell power is a maximum, V_D', for standard configuration solar cells, as a function of barrier and substrate, under AM1 light, at 300°K and for six example semiconductors.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

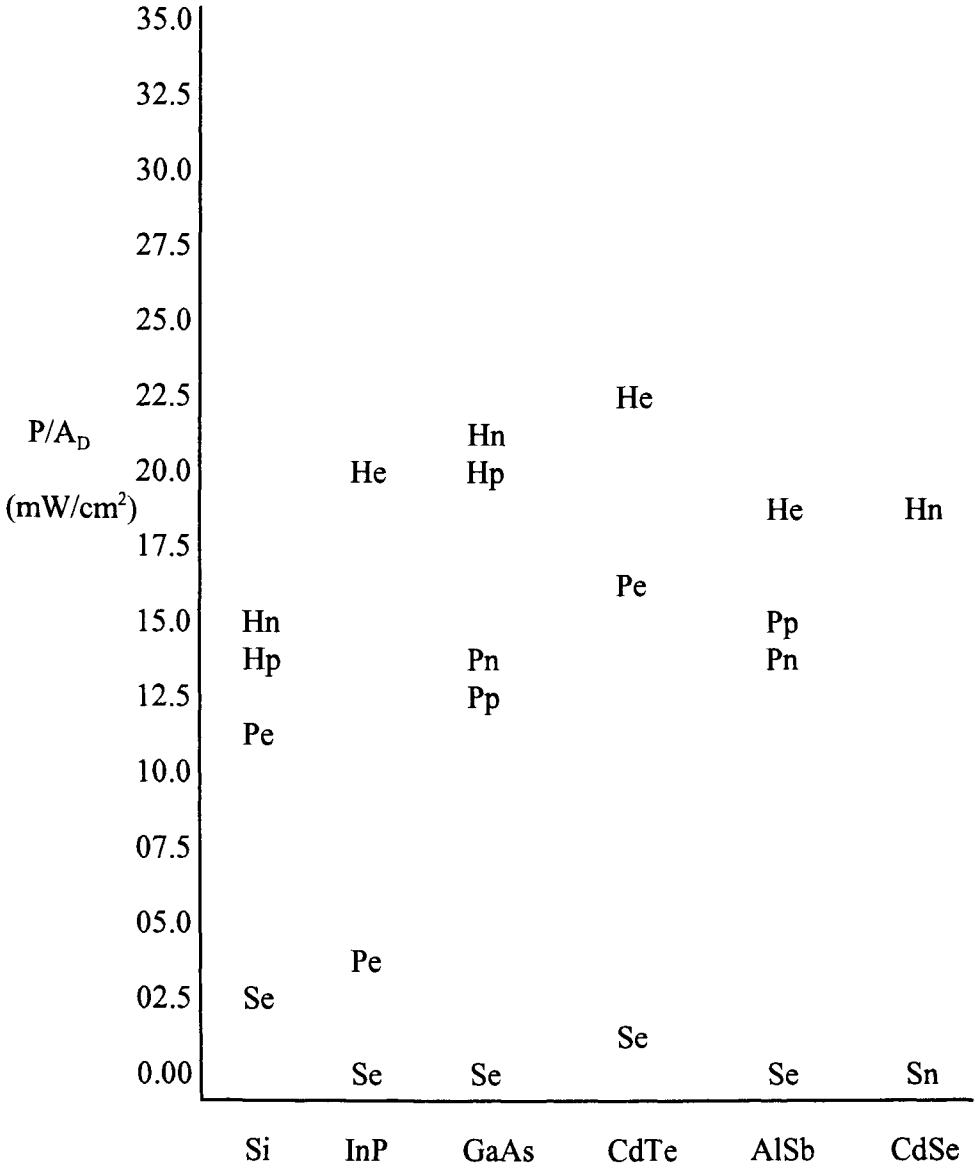

Figure VI.9. The maximum delivered power density, P/A_D, for standard configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AM1 illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

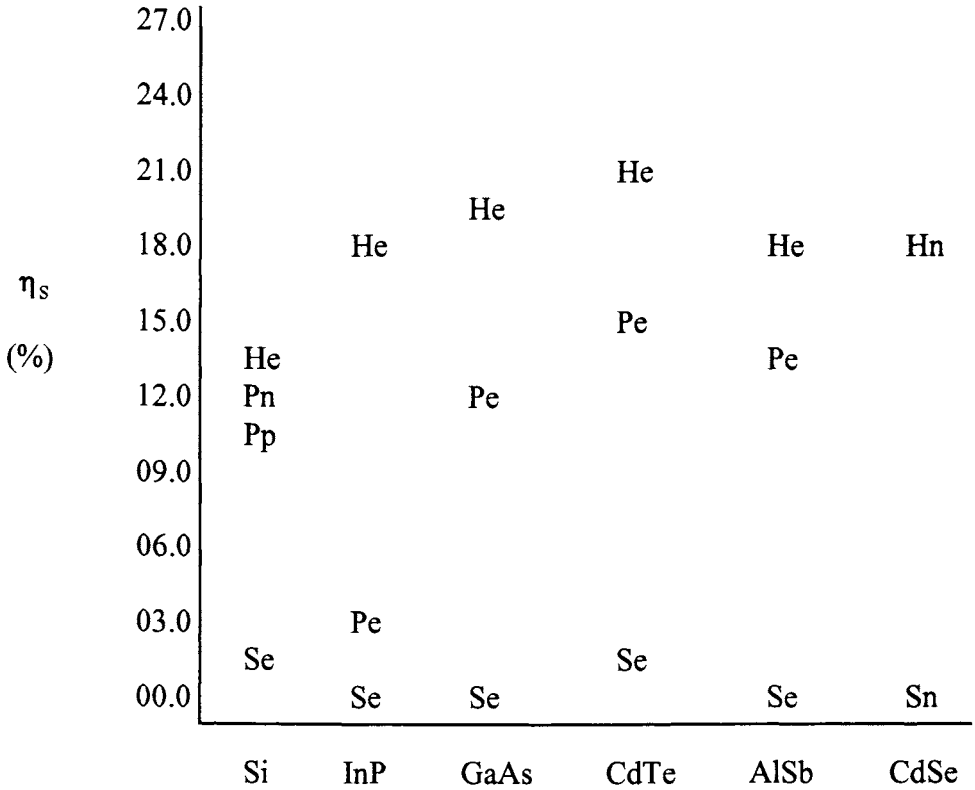

Figure VI.10. Solar cell efficiency, η_S, under the conditions of maximum delivered power density, for standard configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AM1 illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

Figures VI.17 through VI.22 present values of photovoltage, maximum delivered power density and solar cell efficiency at 300°K for inverted configuration solar cells of various junction and substrate types. Note that the performance of these inverted configuration solar cells is higher than for standard configuration solar cells, partly as a result of higher effective (potentially higher!) photocurrents and partly as a result of the lower series resistance times junction area product of these solar cells. Further note that the low Schottky barrier heights result in higher saturation current density and poorer solar cell performance.

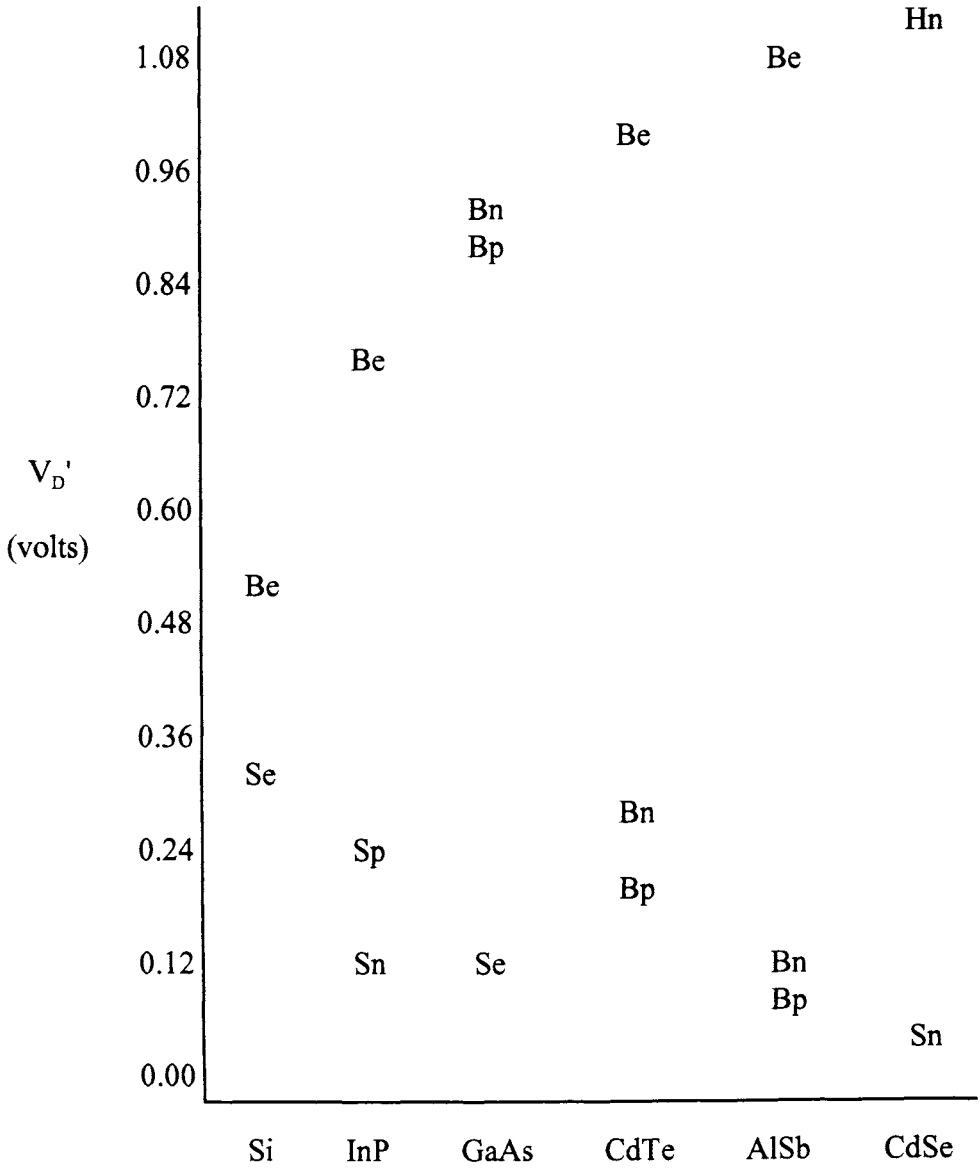

Figure VI.11. Photovoltage when the delivered solar cell power is a maximum, V_D', for vertical configuration solar cells, as a function of barrier and substrate, under AMO light, at 300°K and for six example semiconductors.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

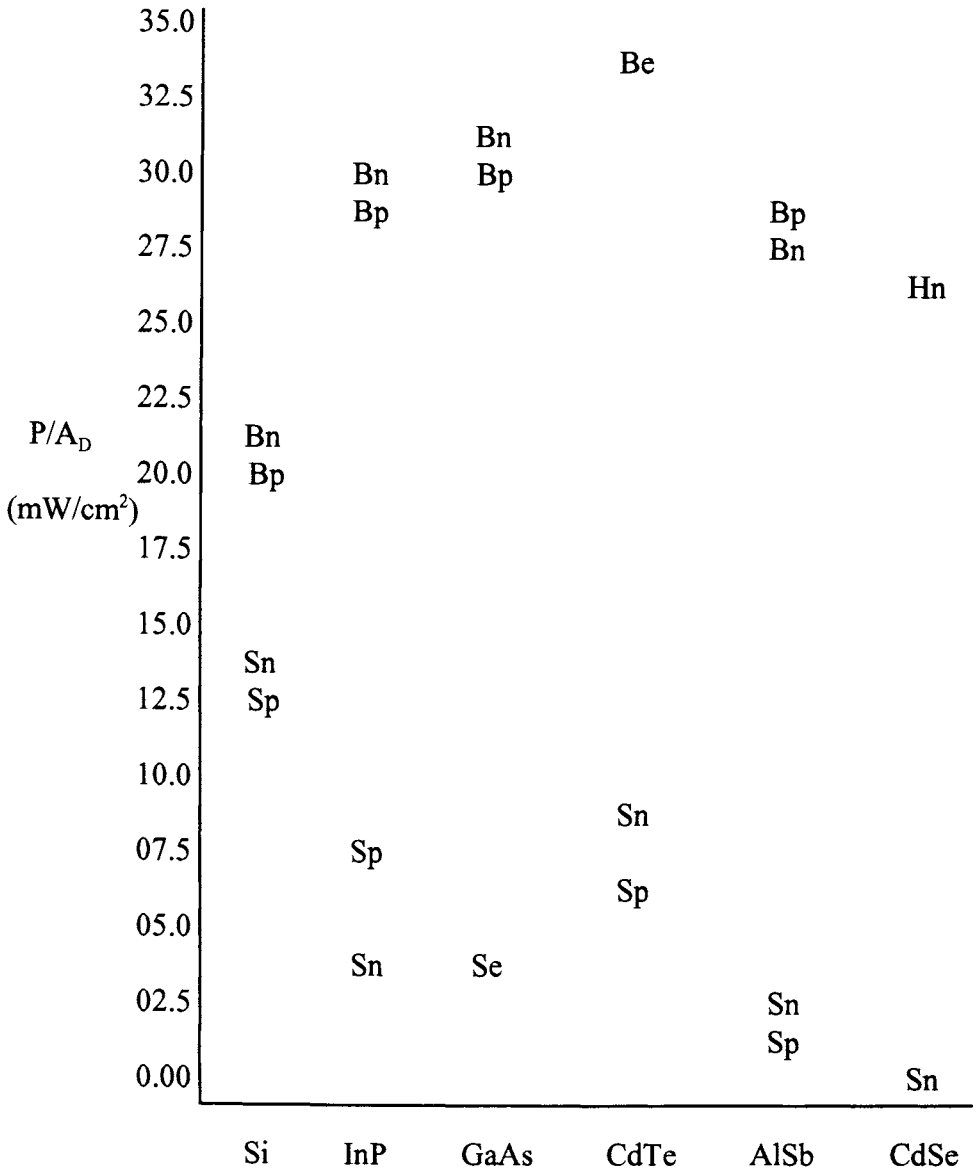

Figure VI.12. The maximum delivered power density, P/A_D, for vertical configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AMO illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

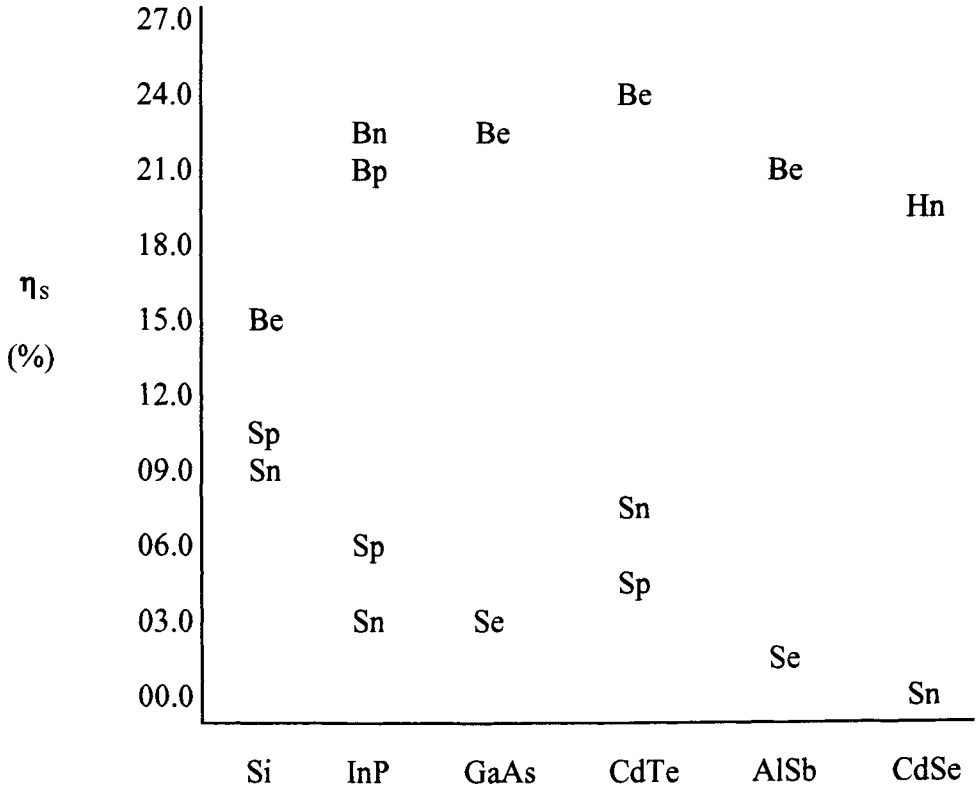

Figure VI.13. Solar cell efficiency, η_S, under the conditions of maximum delivered power density, for vertical configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AMO illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

Comparing the inverted solar cell types of Figures VI.17 through VI.22 with the vertical solar cell performance estimated in Figures VI. 11 through VI.16 note that the performance of the inverted solar cells is estimated to be significantly higher than that of the vetical solar cells. The principal reason for this is the higher photocurrent of the inverted type of solar cell. For inverted cells the effective junction area is approximately one half of the illuminated area. Thus there is significantly higher photocurrent in the inverted solar cells as these devices exhibit a moderate amount of built-in optical concentration.

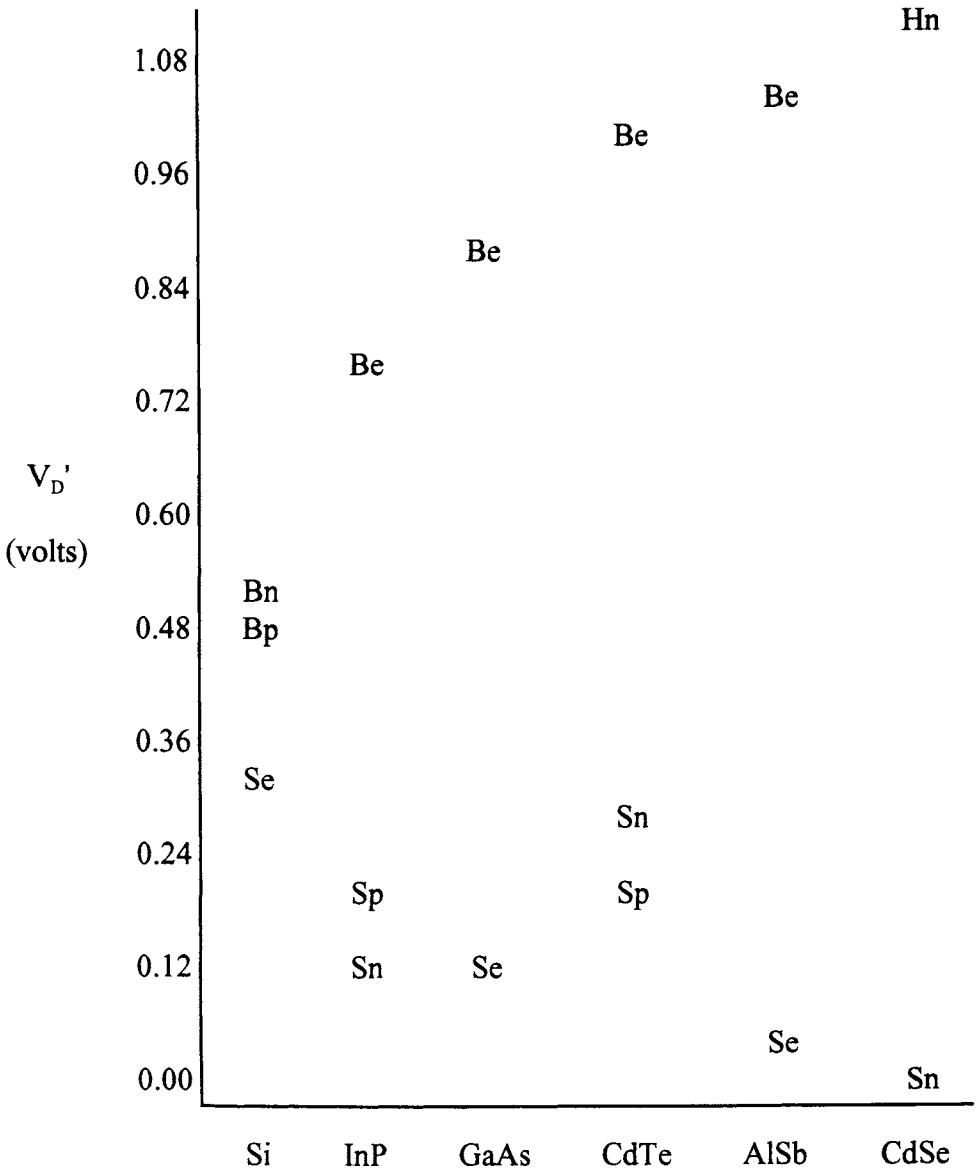

Figure VI.14. Photovoltage when the delivered solar cell power is a maximum, V_D', for vertical configuration solar cells, as a function of barrier and substrate, under AM1 light, at 300°K and for six example semiconductors.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

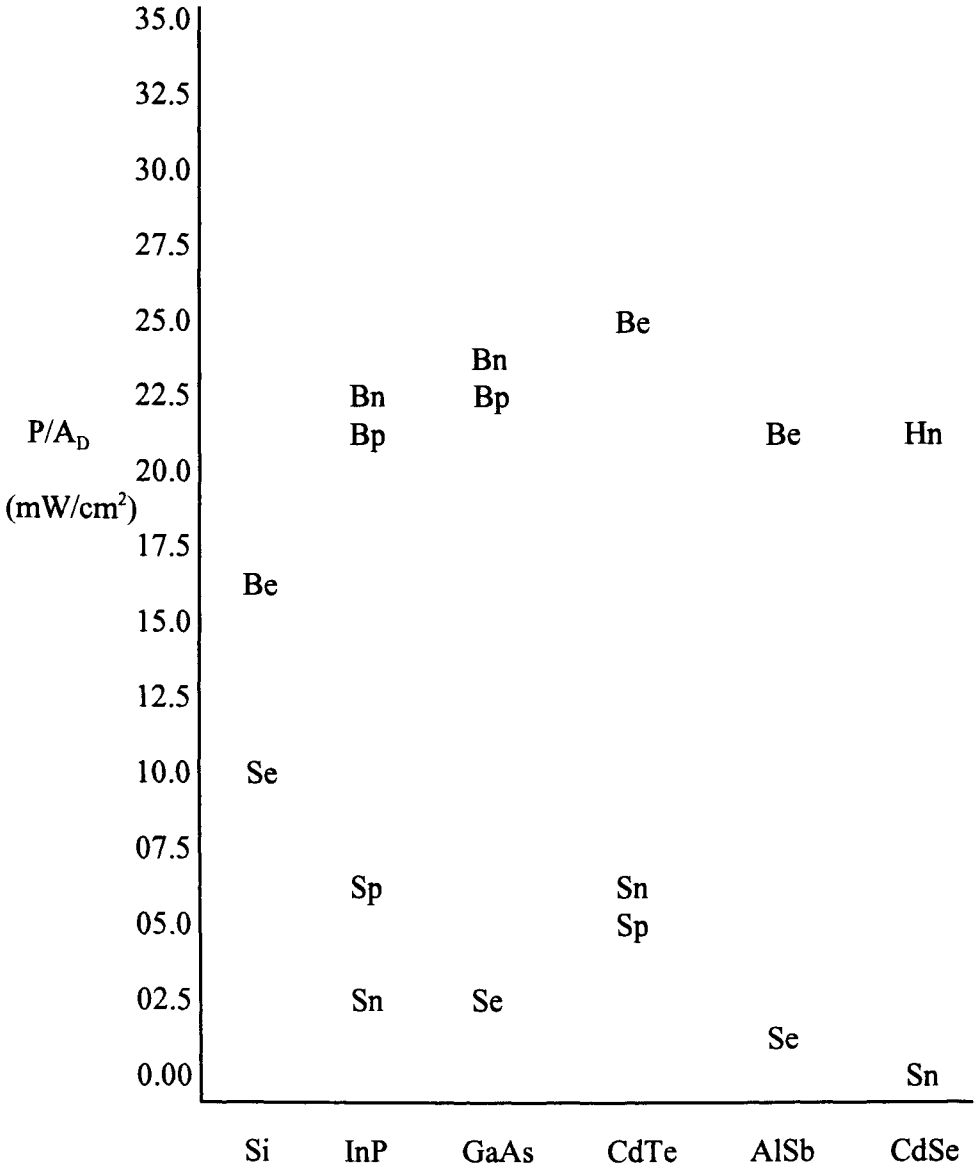

Figure VI.15. The maximum delivered power density, P/A_D, for vertical configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AM1 illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

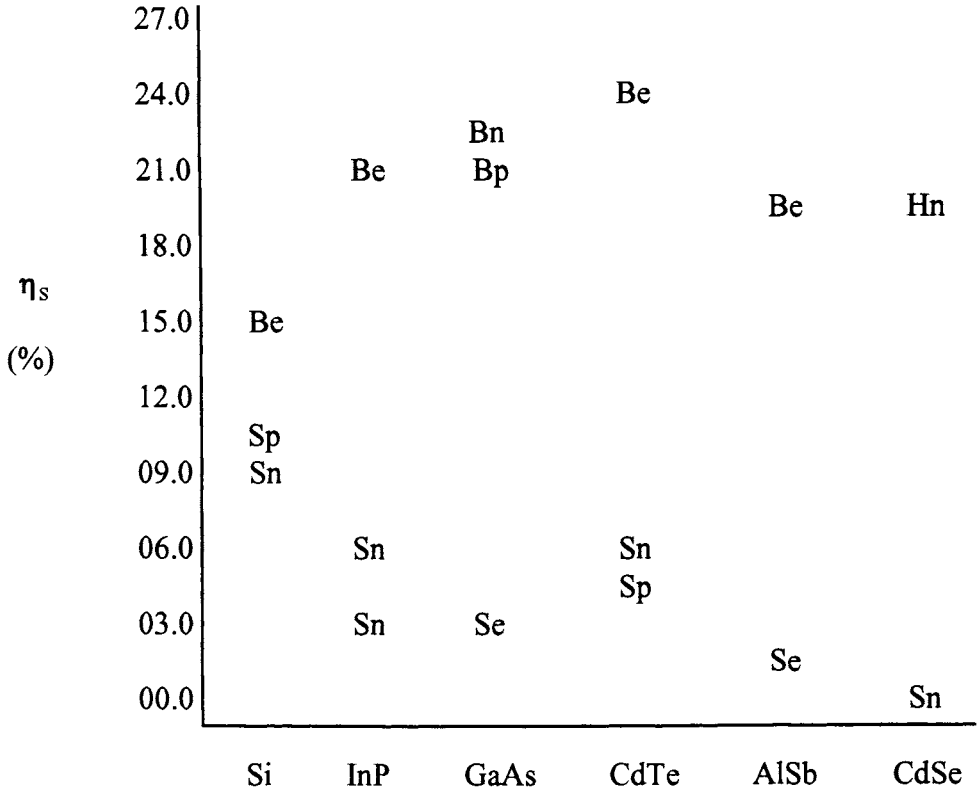

Figure VI.16. Solar cell efficiency, η_S, under the conditions of maximum delivered power density, for vertical configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AM1 illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

Solar Cell Performance - Discussion

Let us conclude this chapter with some discussion regarding Figures VI.5 through VI.22. Let it be emphasized that the devices whose photovoltage, maximum delivered power density and efficiency are shown in these figures are not considered to be the "best there can be" at performing as solar cells. Instead, these solar cells are constructed to represent practical devices. In other words, they are taken to be

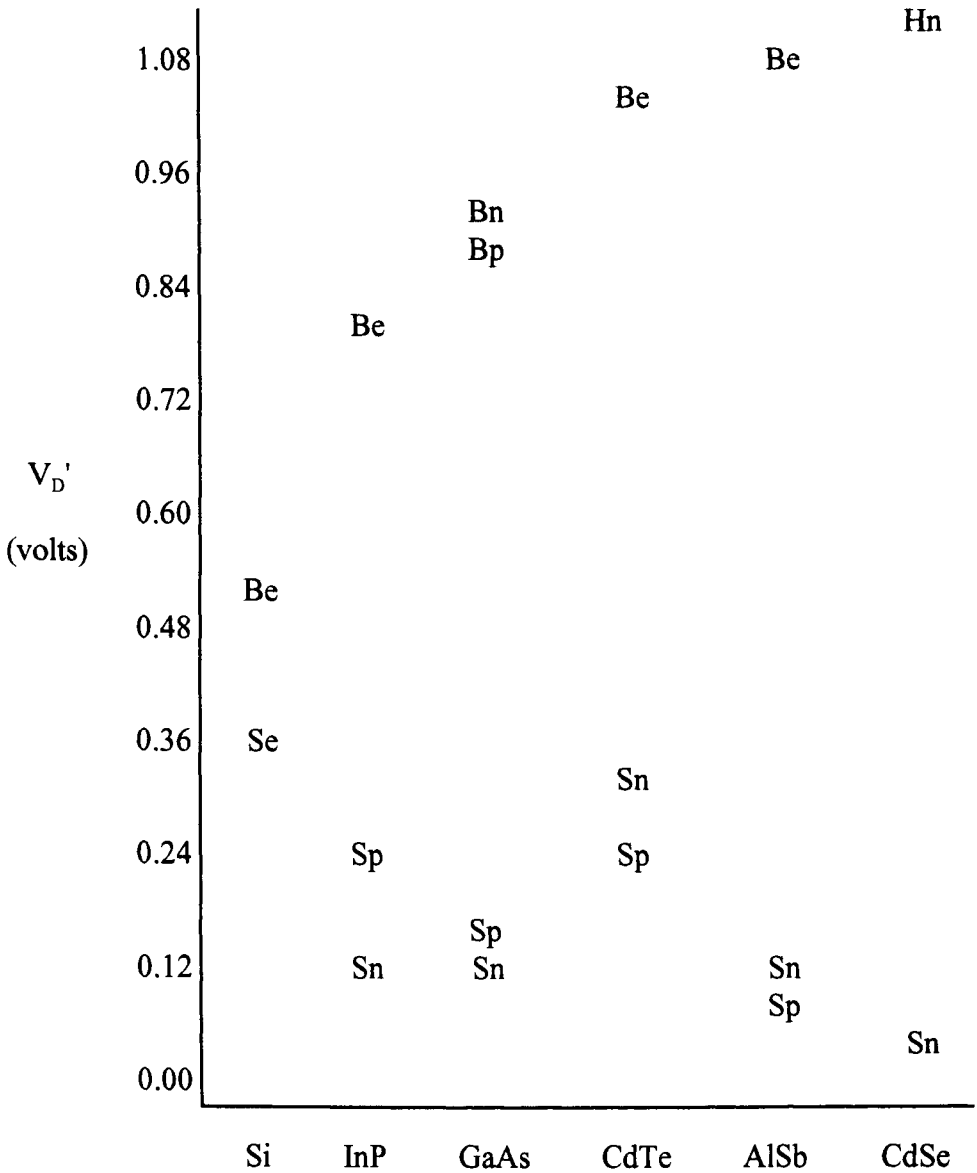

Figure VI.17. Photovoltage when the delivered solar cell power is a maximum, V_D', for inverted configuration solar cells, as a function of barrier and substrate, under AMO light, at 300°K and for six example semiconductors.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

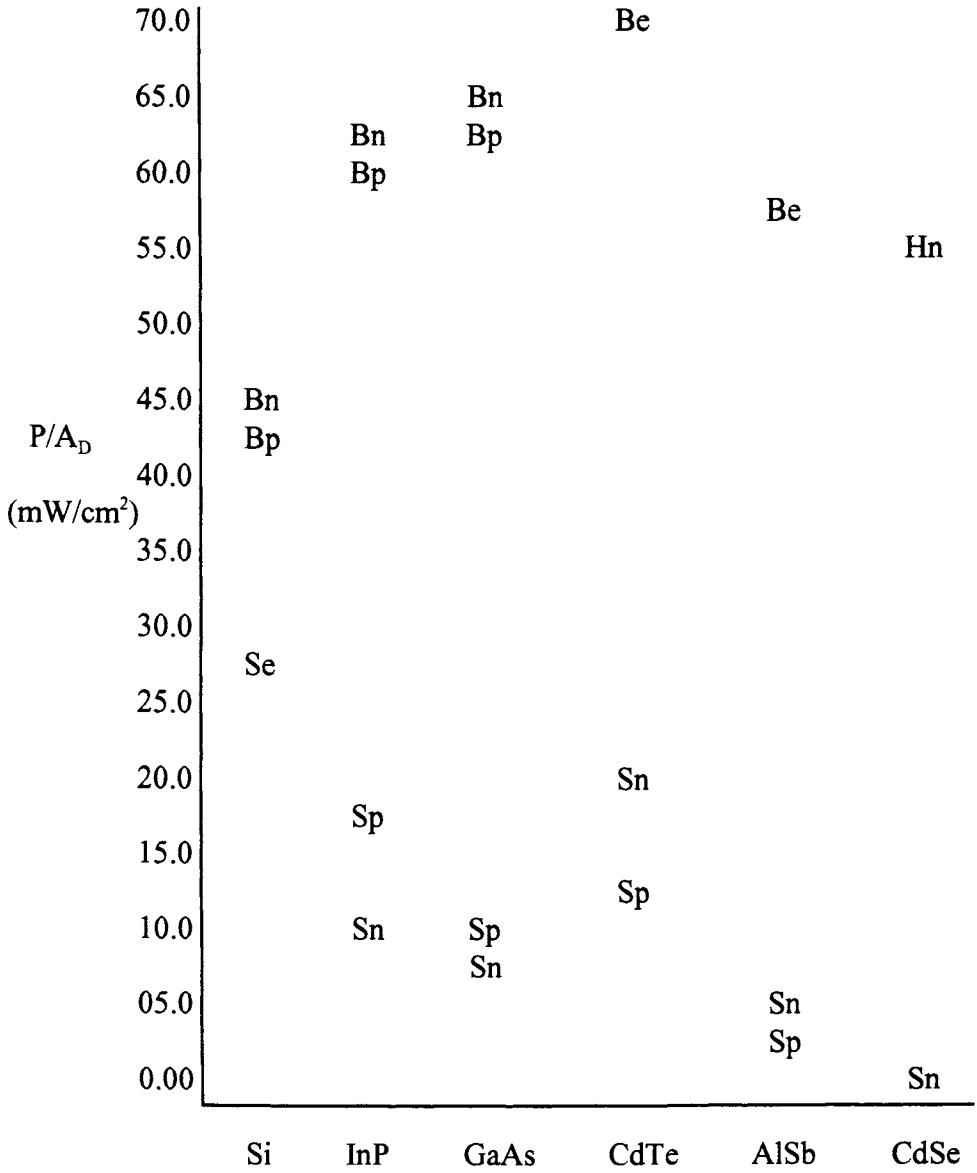

Figure VI.18. The maximum delivered power density, P/A_D, for inverted configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AMO illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

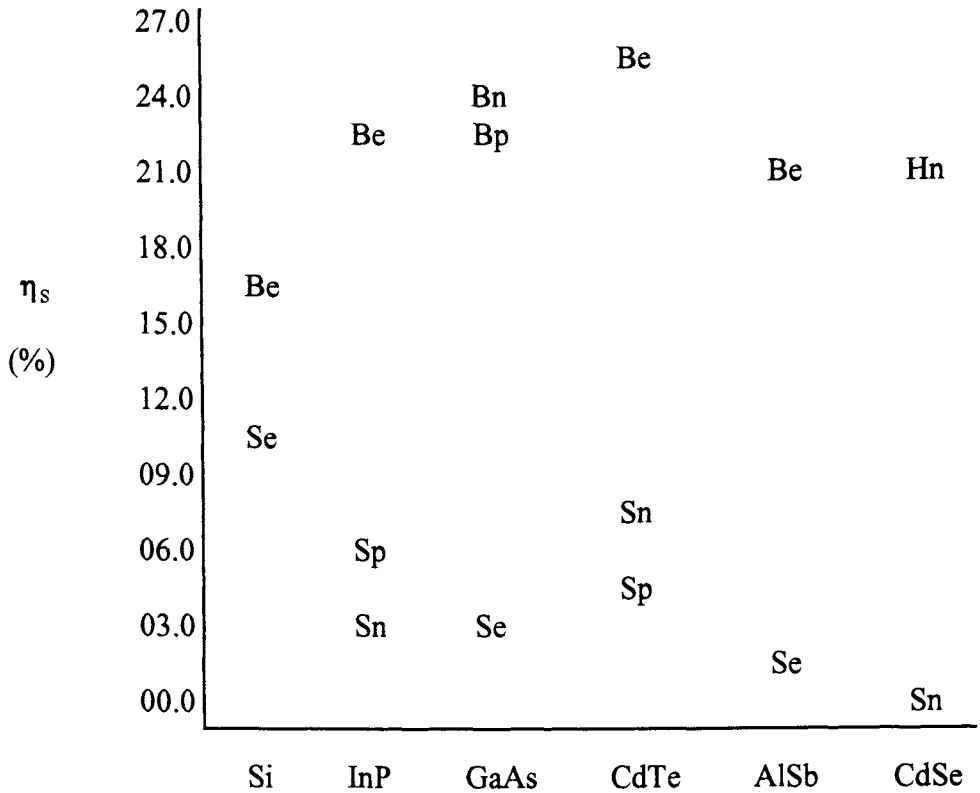

Figure VI.19. Solar cell efficiency, η_S, under the conditions of maximum delivered power density, for inverted configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AMO illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

representative of devices which can be reliably and repeatedly constructed to operate at the performance level indicated. It is possible to better the performance levels indicated in Figures VI.5 through VI.22 by spending a considerable amount of effort at maximizing the photocurrent, while minimizing the saturation current density and series resistance. For example, silicon devices with efficiencies in excess of 20% have been reported [39]. It is also, unfortunately, possible to "snatch defeat from the jaws of victory" and do much worse. The solar cells considered in this chapter are achievable, and allow us to draw some design conclusions.

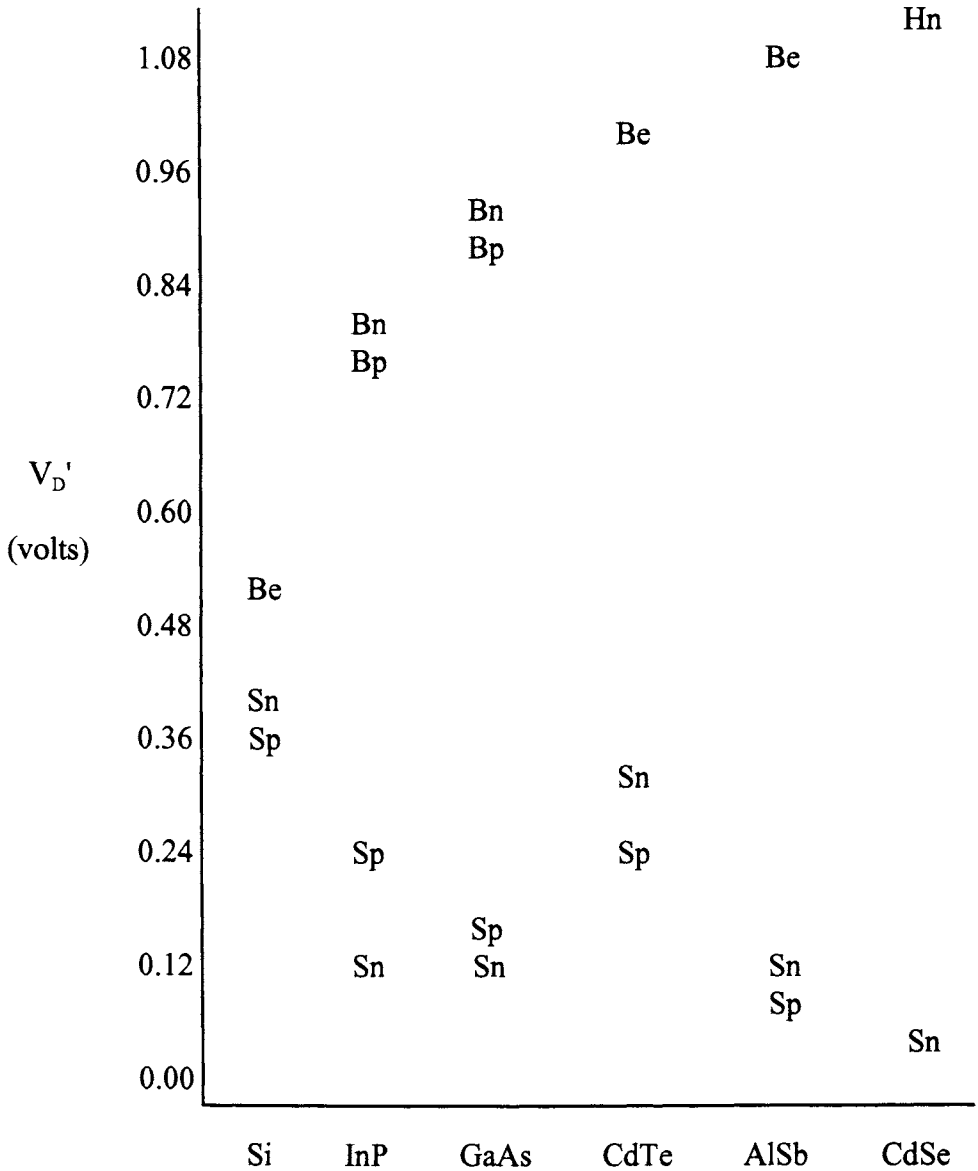

Figure VI.20. Photovoltage when the delivered solar cell power is a maximum, V_D', for inverted configuration solar cells, as a function of barrier and substrate, under AM1 light, at 300°K and for six example semiconductors.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

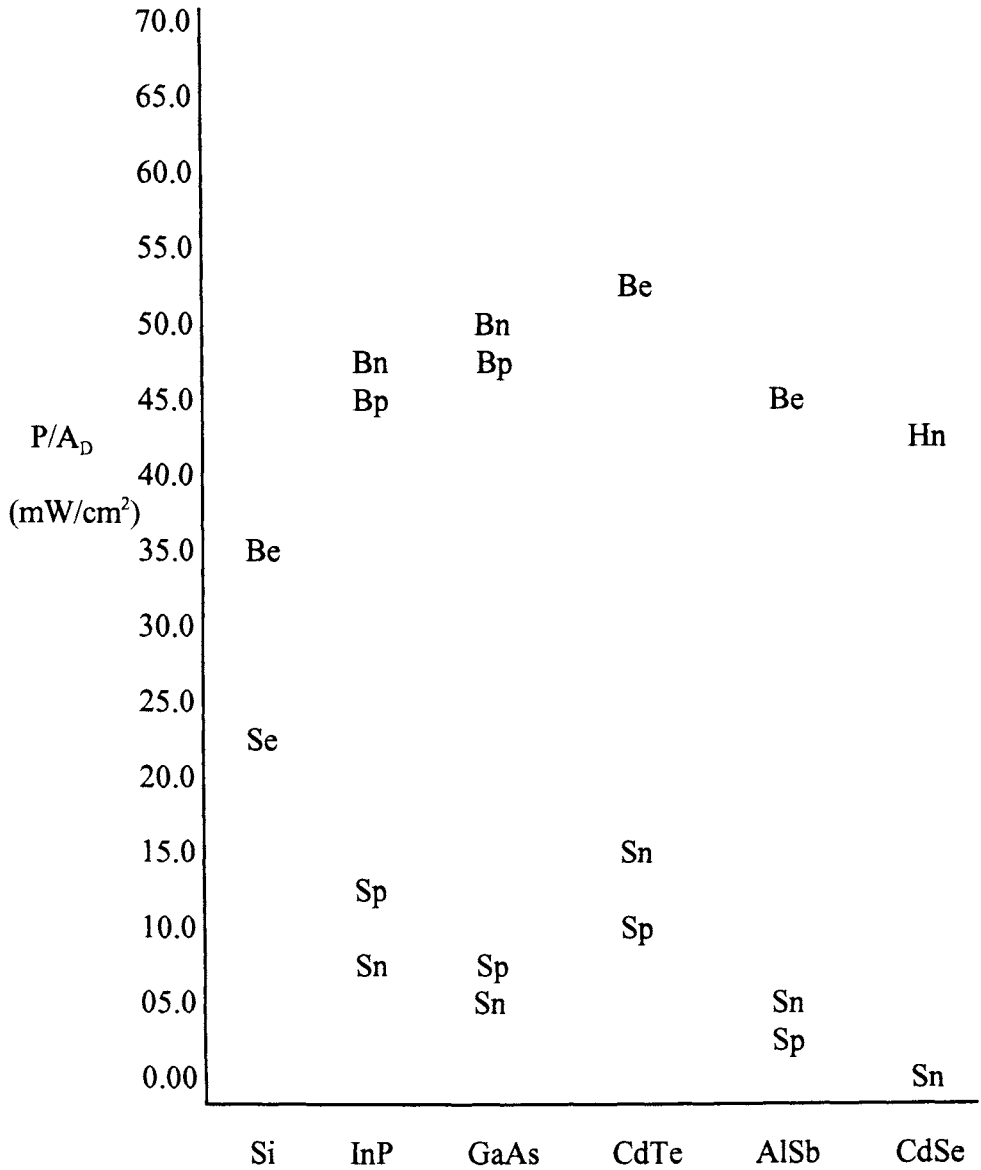

Figure VI.21. The maximum delivered power density, P/A_D, for inverted configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AM1 illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

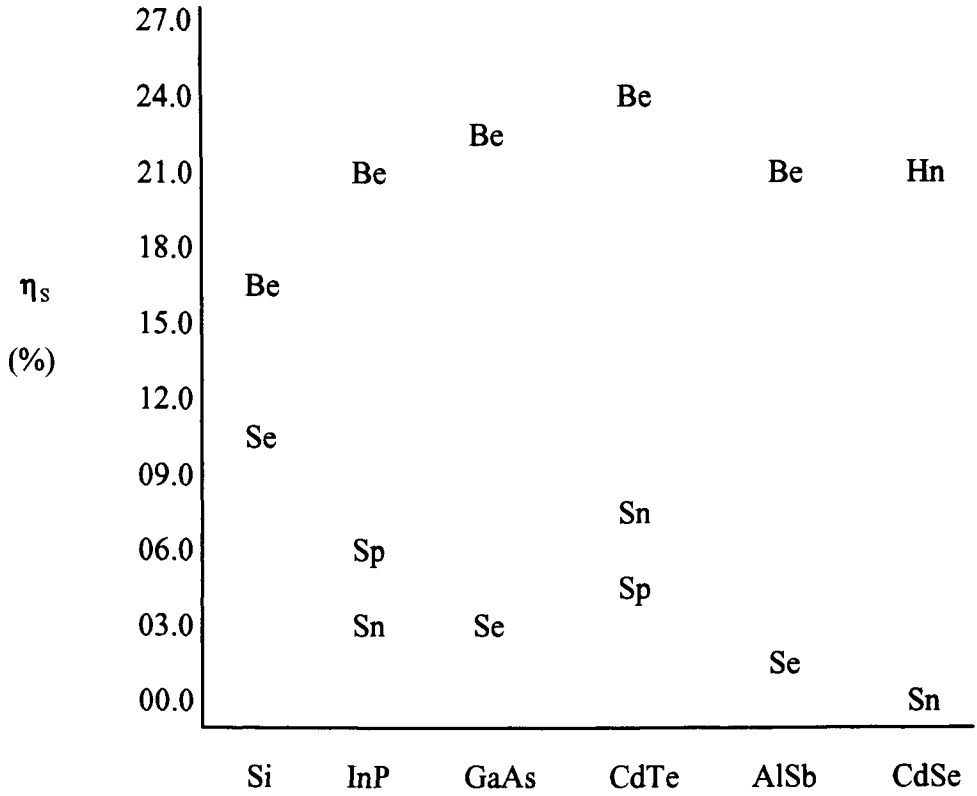

Figure VI.22. Solar cell efficiency, η_S, under the conditions of maximum delivered power density, for inverted configuration solar cells, as a function of barrier and substrate, for six example semiconductors under AM1 illumination and at 300°K.
Junction symbols: H for heterojunction, P for pn junction, S for Schottky barrier and B for both pn and heterojunctions.
Substrate symbols: n for n-type, p for p-type and e for either type.

Overall, pn junction and heterojunction solar cells are potentially capable of generating larger amounts of photopower than are Schottky barrier solar cells. This is the result of lower saturation current densities, particularly for non-silicon semiconductors. In all three optical configurations; standard, vertical and inverted; the predicted performance for solar cells appears to be at a maximum for CdTe. Also note that, in general, the substrate type is relatively unimportant.

From our discussion in Chapter V, the values for photovoltage, given in Figures VI.5, VI.8, VI.11, VI.14, VI.17 and VI.20, should be

in excess of V', the voltage at which the diode current is contributed equally by diffusion and by generation-recombination components. We can solve Equation V.11 to determine V' for the devices considered in this chapter. The results of this operation, along with the effective built-in voltage for pn junctions are provided in Table VI.20.

Table VI.20

Values of V_B and V' (in volts) for pn junctions made from the example semiconductors with the material parameters indicated in this chapter

Semiconductor	Si	InP	GaAs	CdTe	AlSb
		for p-type substrates			
V_B	0.815	1.14	1.23	1.29	1.46
V'	0.063	0.56	0.66	0.71	0.86
		for n-type substrates			
V_B	0.815	1.14	1.23	1.29	1.46
V'	0.036	0.52	0.59	0.65	0.87

Examination of Figures VI.5, VI.8, VI.11, VI.14, VI.17 and VI.20 shows that the experienced photovoltages for heterojunction and pn junction solar cells, for standard, inverted and vertical configurations, are in excess of V'. The photovoltages for Schottky diode solar cells are less than V' in Table VI.20 but the above mentioned limitation does not apply, because the overall performance is so low as to make Schottky barrier devices of little, or no, interest. Note that the optimum output solar cell voltage is less than V_B for all pn and heterojunction devices and is less than ϕ_{Bo} (see Table VI.4) for Schottky junction solar cells.

The performance of standard configuration solar cells as displayed in Figures VI.5 through VI.10 involves an approximation. The power density obtainable depends on the actual physical dimensions of the solar cell. The series resistance times area product contains a term due to the substrate which is independent of the illuminated area radius, a, and which is provided in Table VI.14. However, it also includes a term due to the series resistance of the "front layer". This term was presented in Table VI.16, assuming a circular area for the solar cells, and it was indicated in Table VI.16 that the series resistance times area product for standard

configuration solar cells varies as a^2. The performance displayed in Figures VI.5 through VI.10 is based on the assumption that the series resistance times area product for standard configuration solar cells is that of the substrate plus a contribution from the "front layer"--a contribution that amounts to 10% of the substrate value. Note that the greater the radius of the standard configuration solar cell the greater the light collecting area and the greater the experienced photocurrent. However, the resistance times area product will also increase, leading to a larger loss factor and a lower output power density and operating efficiency. The exact size which is most efficient is a function of the type of junction, the intensity of the light illuminating the solar cell and the economics of the fabrication process employed in constructing the solar cells. Clearly, if output power density is the sole important item, then the ideal solar cell has no internal resistance what-so-ever--a topic which will be addressed in the following chapter.

We will not pursue this topic further at present. For now, the reader will be interested in Table VI.21 which presents the effective radius of standard configuration solar cells for the case in which the "front layer" contributes an amount equal to 10% of the substrate series

Table VI.21

The illuminated region radius, a, (in μm) for standard configuration solar cells for a "front layer" series resistance times area product which is 10% of that of the substrate product

Semiconductor	Si	InP	GaAs	CdTe	AlSb	CdSe
Junction Type						
			n-type substrates			
Schottky	525	358	253	663	1727	839
heterojunction	152	103	073	191	0499	242
pn	038	035	020	038	0185	*
			p-type substrates			
Schottky	876	2032	1084	2123	1015	*
heterojunction	253	0567	0313	0613	0294	*
pn	081	0345	0027	1412	0096	*

* p-type CdSe is not available

resistance times area product--the situation leading to Figures VI.5 through VI.10. Note that the dimensions, a, are small, leading the reader to conclude that a larger device would exhibit a significantly higher series resistance area product, and hence would have a substantially lower performance.

Careful study of the theoretical predictions contained in Figures VI.5 through VI.22 and of the rest of this chapter indicates that inverted configuration solar cells are potentially capable of the highest level of performance, followed by vertical configuration solar cells and, followed, at the lowest level, by standard configuration solar cells. Considering the type of junction, pn or heterojunction (given the availability of suitable matching semiconductors) solar cells appear to be preferable, as compared to the poorly performing Schottky barriers. Substrate type, while it does exhibit some effect on solar cell performance, does not play a major role in device output. Finally, it would seem that the performance of solar cells (in terms of output power density and efficiency) is highest for those situations in which the semiconductor employed has an energy gap in the vicinity of 1.5 eV.

What we have not done, as yet, is consider the economics of the fabrication processes employed and the effects of increased illumination levels and solar cell junction temperatures. These topics will be covered in the succeeding chapters. In addition, we will consider additional techniques for improving solar cell performance. Even without these improvements, the potential performance for solar cells, as indicated in this chapter, is encouraging when we consider solar cells as a major energy source for our civilization.

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