IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND-ODESSA DIVISION

POLARIS INNOVATIONS LIMITED, a Delaware Corporation, Plaintiff v. QUALCOMM INCORPORATED and QUALCOMM TECHNOLOGIES, INC., both Delaware Corporations, Defendants	CIVIL ACTION NO. 7:24-cv-00296 **JURY TRIAL DEMANDED**

PLAINTIFF'S COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Polaris Innovations Limited ("Polaris") files this Complaint against Defendants Qualcomm Incorporated and Qualcomm Technologies, Inc. (together, "Qualcomm" or "Defendants") for infringement of U.S. Patent No. 7,184,339 (the "'339 Patent"); U.S. Patent No. 7,499,371 (the "'371 Patent"); U.S. Patent No. 7,872,936 ("the '936 Patent"); and U.S. Patent No. 8,161,344 (the "'344 Patent"), collectively, the "Asserted Patents."

THE PARTIES

1. Polaris Innovations Limited is a corporation organized and existing under the laws of Ireland, with its principal place of business at 77 Lower Camden Street, Dublin D02 XE80, Ireland.

2. Defendant Qualcomm Incorporated ("QCI") is a corporation organized and existing under the laws of Delaware and maintains established places of business at 9600 N. Mopac, Suite 900, Stonebridge Plaza II, Austin, Texas 78759 and 13929 Center Lake Drive, Parmer Building 1 Austin, Texas 78753. QCI may be served in Texas via its registered agent Prentice Hall Corp. System, 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

3. Defendant Qualcomm Technologies, Inc. ("QTI") is a corporation organized and existing under the laws of Delaware and maintains established places of business at 9600 N. Mopac, Suite 900, Stonebridge Plaza II, Austin, Texas 78759 and 13929 Center Lake Drive, Parmer Building 1, Austin, Texas 78753. QTI may be served in Texas via its registered agent Corporation Service Company d/b/a CSC-Lawyers Incorporating Service Company, 211 E. 7th Street, Suite 620, Austin, TX 78701.

4. QTI is a wholly-owned subsidiary of QCI and, together with its affiliates, serves and performs substantially all of Qualcomm's research and development efforts, its engineering operations, and its products and services businesses. *See* https://www.qualcomm.com/company. Relevant QTI-affiliated companies include, at least, Qualcomm CDMA Technologies and Qualcomm CDMA Technologies Asia Pacific Pte. Ltd.

5. Qualcomm is one of the world's premier manufacturers of integrated circuits for the wireless device industry. Its website states that "[r]eferences to 'Qualcomm' may mean Qualcomm Incorporated, or subsidiaries or business units within the Qualcomm corporate structure, as applicable." *Id*. Qualcomm's website further states that "Qualcomm Technologies, Inc., a subsidiary of Qualcomm Incorporated, operates, along with its subsidiaries, substantially all of our engineering, research and development functions, and substantially all of our products and services businesses, including our QCT semiconductor business." *Id*.

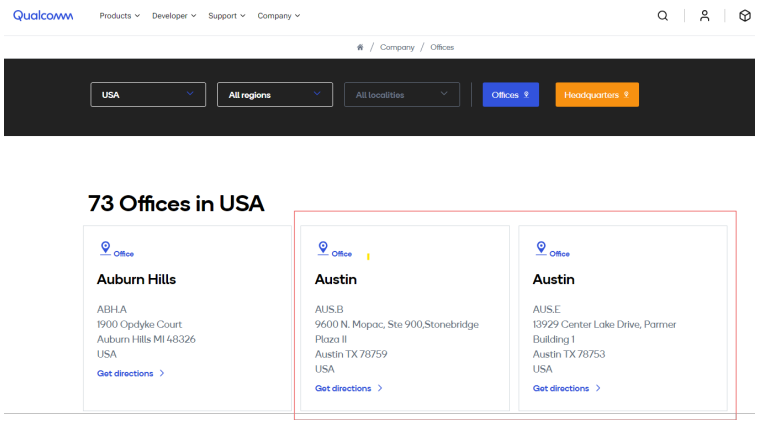
6. QCI, QTI, and their subsidiaries and related companies share the same management, common ownership, advertising platforms, facilities, distribution and sales channels, and accused products and product lines. In this way, QCI, QTI, and their subsidiaries and related companies operate as a singular, unitary business enterprise and are, thus, jointly, severally and communally liable for the acts of patent infringement detailed below.

7. QCI, QTI, and their subsidiaries and related companies are doing business collectively, directly and through agents, on a persistent and ongoing basis in this District and elsewhere in the United States, and they each have regular and established places of business here.

JURISDICTION AND VENUE

8. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, et seq. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

9. This Court has personal jurisdiction over Qualcomm because it has engaged, and continues to engage, in continuous, systematic, and substantial activities within this State, including the substantial marketing and sale of products and services within this State and this District. Indeed, this Court has personal jurisdiction over Qualcomm because it has committed acts giving rise to Polaris' claims for patent infringement within and directed to this District, has derived substantial revenue from its goods and services provided to individuals and entities in this State and this District, and maintains regular and established places of business in this District, including at least its two brick-and-mortar locations in Austin, Texas:[1]



[1] *See* https://www.qualcomm.com/company/facilities/offices?country=USA&page=2.

10. Relative to patent infringement, Qualcomm has committed and continues to commit acts in violation of 35 U.S.C. § 271, and has made, used, offered for sale, sold, and imported infringing products, systems, and services in this State, including this District, and has otherwise engaged in infringing conduct within and directed at, or from, this District. Infringing products, systems, and services (collectively, the "Accused Instrumentalities") include Qualcomm processors such as the Qualcomm Snapdragon 4, 6, 7, 8, and X Series products and other processors and platforms offered and sold by Qualcomm as described further below.

11. Qualcomm's infringing activities have caused harm to Polaris in this District. Qualcomm and/or its partners and agents offer to sell and sell the Accused Instrumentalities within this District, and on information and belief, Qualcomm, its partners and agents, and/or their customers use the Accused Instrumentalities in this District in infringing ways. These are purposeful acts and transactions in this State and this District such that Qualcomm reasonably should know and expect that it can be haled into this Court to answer for its actions.

12. Moreover, this Court maintains personal jurisdiction over Qualcomm because Qualcomm conducts business in this State by, among other things, "recruit[ing] Texas residents, directly or through an intermediary located in this State, for employment inside or outside this State." Tex. Civ. Prac. & Rem. Code § 17.042(3). For instance, Qualcomm lists dozens of job openings in Texas (as of Oct. 29, 2024):[2]

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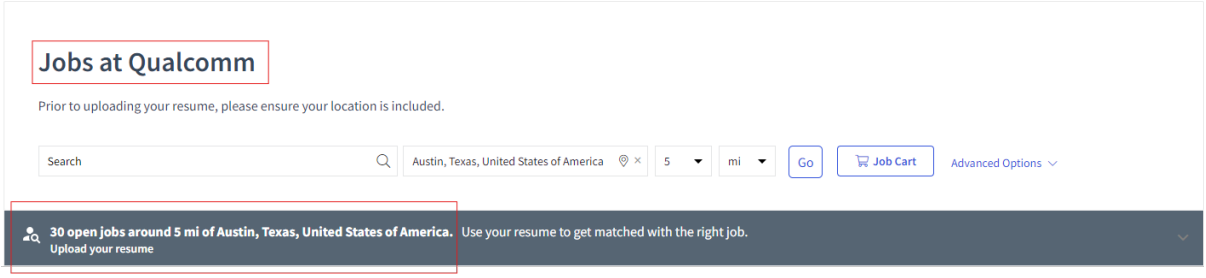
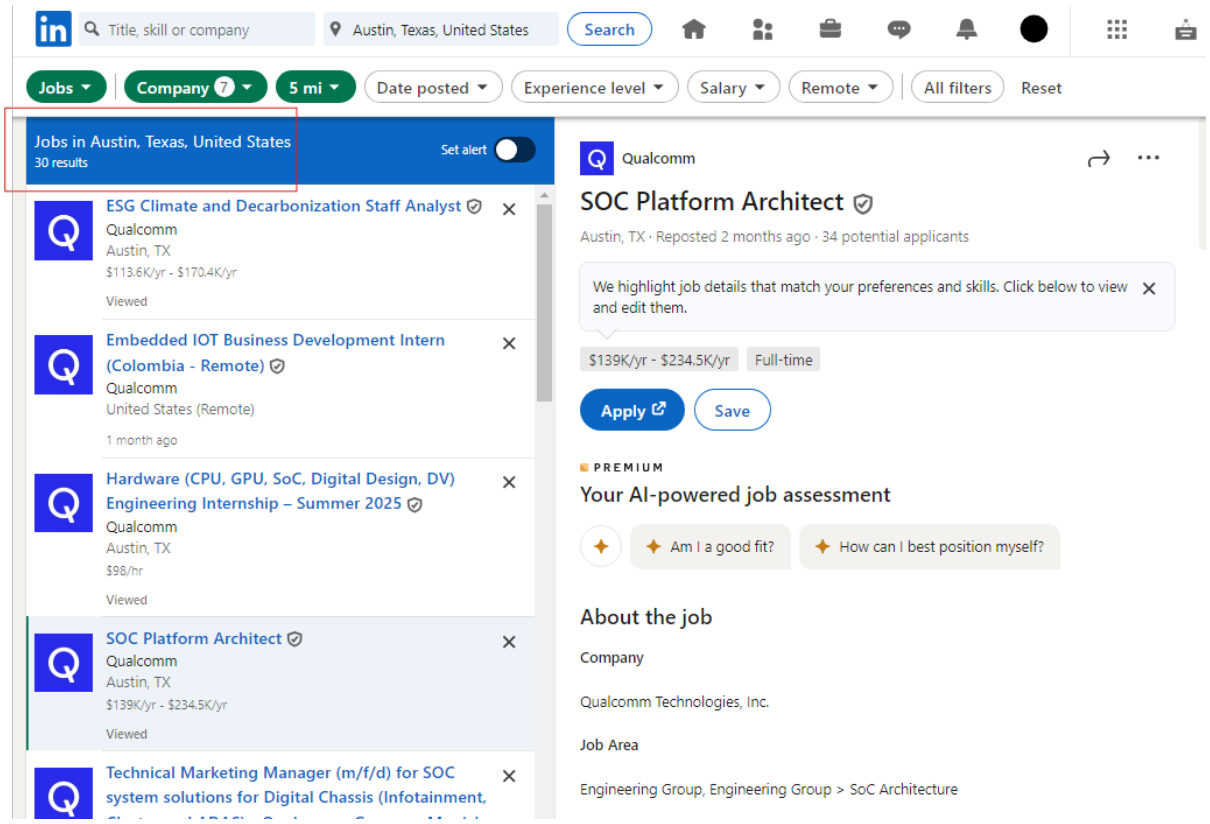
[2] https://careers.qualcomm.com/careers?location=Austin%2C%20Texas%2C%20United%20States%20of%20America&pid=446697682796&domain=qualcomm.com&sort_by=relevance&location_distance_km=8&triggerGoButton=true

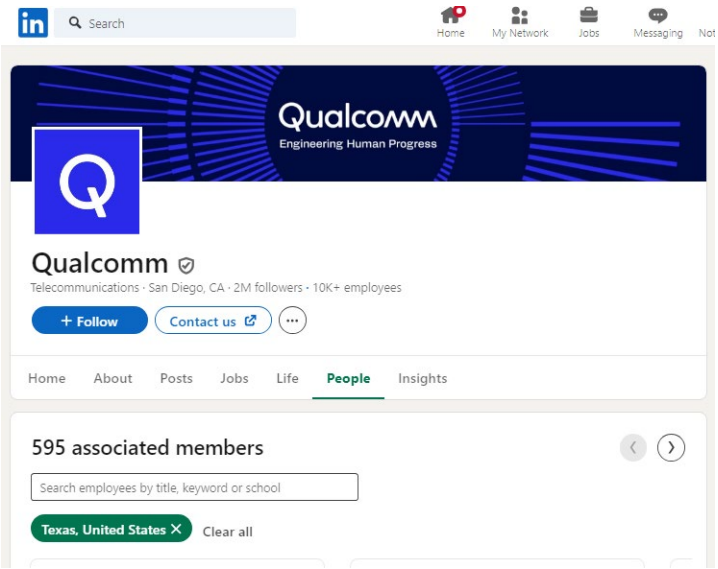


13. Qualcomm also lists its job openings in Texas on LinkedIn (as of Oct. 24, 2024):[3]



[3]https://www.linkedin.com/jobs/search/?currentJobId=3991694727&distance=5&f_C=2017%2C154985%2C162572%2C2923434%2C38387%2C595224%2C75115234&f_CR=103644278&geoId=104472865&origin=JOB_SEARCH_PAGE_JOB_FILTER&refresh=true&sortBy=R

14. Further, on Qualcomm's LinkedIn page, it boasts 603 "associated members" in its Texas offices (as of Oct. 24, 2024):[4]



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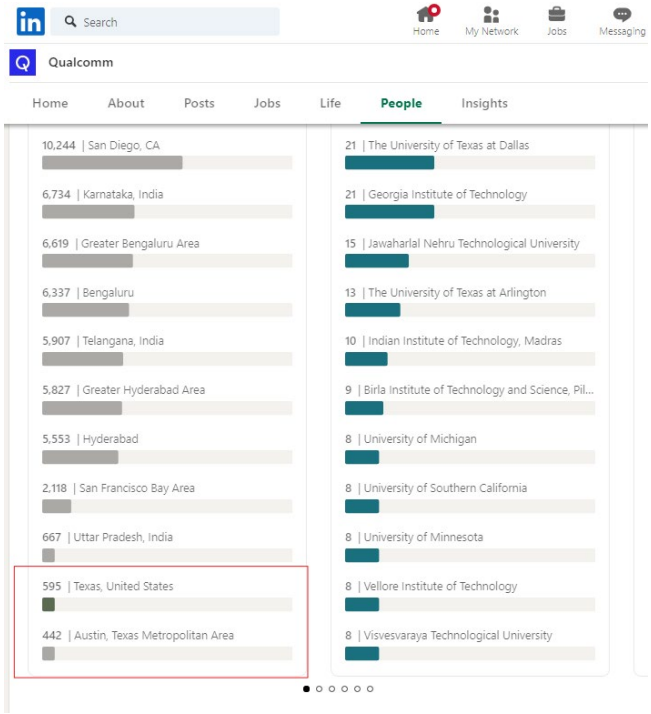

[4] https://www.linkedin.com/company/qualcomm/people/?facetGeoRegion=102748797

15. Venue is proper in this District under 28 U.S.C. §§ 1391 and 1400(b) because Qualcomm has at least two regular and established places of business in Austin, which is in this District. Venue is further proper in this District because Qualcomm has directly infringed and/or induced the infringements of others, including its customers, in this District by offering for sale and selling Accused Instrumentalities in this District, using Accused Instrumentalities in infringing ways in this District, and inducing infringing customer use of Accused Instrumentalities in this District.

THE ASSERTED PATENTS

16. Polaris is the sole and exclusive owner of all right, title, and interest in the'339 Patent, the '371 Patent, the '936 Patent, and the '344 Patent and holds the exclusive right to take all actions necessary to enforce its rights in, and to, the Asserted Patents, including the filing of this patent infringement lawsuit. Polaris also has the right to recover all damages for past, present, and future infringements of the Asserted Patents and to seek injunctive relief as appropriate under the law.

17. The '339 Patent is titled, "Semi-conductor component, as well as a process for the in-or output of test data." The '339 Patent issued on February 27, 2007 and stems from U.S. Patent Application No. 11/253,807, which was filed on October 20, 2005.

18. The '371 Patent is titled "Semiconductor memory system with a variable and settable preamble f." The '371 Patent issued on March 3, 2009 and stems from U.S. Patent Application 11/288,941, which was filed on November 28, 2005.

19. The '936 Patent is titled "System and method for packaged memory." The '936 Patent issued January 18, 2011 and stems from U.S. Patent Application No. 12/212,400 which was filed on September 17, 2008.

20. The ’344 Patent is titled “Circuits and methods for error coding data blocks.” The ’344 Patent issued April 17, 2012 and stems from U.S. Patent Application No. 12/046,099 which was filed on March 11, 2008.

21. Polaris and its predecessors complied with the requirements of 35 U.S.C. § 287, to the extent necessary, such that Polaris may recover pre-suit damages.

22. The claims of the Asserted Patents are directed to patent-eligible subject matter under 35 U.S.C. § 101. They are not directed to abstract ideas, and the technologies covered by the claims comprise systems and/or consist of ordered combinations of features and functions that, at the time of invention, were not, alone or in combination, well-understood, routine, or conventional.

DEFENDANTS’ PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENTS

23. Prior to the filing of this Complaint, Polaris sent letters to Qualcomm notifying Qualcomm that various exemplary products infringe at least one or more claims of the’339 Patent, the ’371 Patent, the ’936 Patent, and the ’344 Patent and that Qualcomm needs to take a license. *See* Aug. 9, 2024 Letter (and accompanying claim charts); *see also* October 13, 2015 Letter. Qualcomm has not agreed to license the Asserted Patents, and Polaris brought this action to protect its rights.

24. The Accused Products include, but are not limited to, the exemplary products identified in Polaris’ letters to Qualcomm. Qualcomm’s past and continuing sales of the Accused Products: (i) willfully infringe the Asserted Patents; and (ii) impermissibly usurp the significant benefits of Polaris’ patented technologies without fair compensation.

COUNT I

(INFRINGEMENT OF U.S. PATENT NO. USP 7,184,339)

25. Plaintiff incorporates the preceding paragraphs herein by reference.

26. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

27. Polaris is the owner of all substantial rights, title, and interest in and to the '339 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

28. The '339 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on February 27, 2007, after full and fair examination.

29. Qualcomm has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '339 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Qualcomm products, their components and processes, and/or products containing the same, that incorporate the fundamental technologies covered by the '339 Patent, including, but not limited to, its Snapdragon 4, 6, 7, 8, and X Series products incorporating LPDDR4/X or LPDDR5/5X memory (collectively, "the '339 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

30. Qualcomm has directly infringed and continues to directly infringe one or more claims of the '339 Patent in this District and elsewhere in Texas and the United States.

31. Qualcomm has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '339 Patent[5] as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '339 Accused Products. Furthermore, Qualcomm makes and sells the '339 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States or, in the case that it delivers the '339 Accused Products outside of the United States, does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '339 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

32. Furthermore, Qualcomm directly infringes the '339 Patent through its direct involvements in, and control of, the activities of subsidiaries and agents. Subject to Qualcomm's direction and control, the subsidiaries and agents conduct activities that constitute direct infringement of the '339 Patent under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing Accused Instrumentalities. Qualcomm receives direct financial benefit from such infringements by its U.S.-based subsidiaries and agents.

33. By way of illustration only, the '339 Accused Products perform each and every element of Claim 1 of the '339 Patent. The '339 Accused Products perform "[a] process for inputting and/or outputting test data and/or semi-conductor component operating control data into

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[5] Throughout this Complaint, wherever Polaris identifies specific claims of the Asserted Patents infringed by Qualcomm, Polaris expressly reserves the right to identify additional claims and products in its infringement contentions in accordance with applicable local rules and the Court's case management order. Specifically identified claims throughout this Complaint are provided for notice pleading only.

or from a semi-conductor component, whereby the semi-conductor component comprises one or more useful data memory cells for storing useful data, and one or more test data and/or semi-conductor component operating control data registers for storing test data and/or semi-conductor component operating control data, comprising" the steps of Claim 1. For instance, the '339 Accused Products, such as the SM8250, incorporate LPDDR4/4X or LPDDR5/5X memory that comply with JEDEC standards and perform the steps described below:

Qualcomm

SM8250
Device Specification
80-PL546-1 Rev. R

Qualcomm Technologies, Inc.

Device description

SM8250 is the new generation Qualcomm® Snapdragon™ premium-tier processor with external 4G/5G modem (SDX55M). It is designed with the 7 nm process, for superior performance and power efficiency. SM8250 includes the following key components:

- Qualcomm® Kryo™ 585 CPU built on Arm Cortex technology
- Qualcomm® Adreno™ 650 GPU for the highest in graphics performance and power efficiency
- Qualcomm® Hexagon™ DSP with quad Hexagon Vector eXtensions (HVX) processor for vision processing and machine learning
- Qualcomm Spectra™ 480 image processing engine for the ultimate photography and videography experiences
- Adreno 665 VPU for high-quality, ultra HD video encode and decode
- Adreno 995 DPU for on-device and external ultra HD display support
- Low-power audio subsystem combined with the Qualcomm Aqstic™ Audio Technologies WCD9380/WCD9385 audio codec for low power voice processing and audiophile quality audio playback
- Qualcomm® Sensing Hub for contextual awareness and always-on sensor support
- Qualcomm® Secure Processing Unit (SPU240) for advanced secure use cases
- Qualcomm® Neural Processing Unit (NPU230) for high-performance machine learning use cases
- External 802.11ax, 2 × 2 MIMO, and Bluetooth 5.1
- Quad-channel package-on-package (PoP) high-speed LPDDR5/LPDDR4X SDRAM

(80_PL546_1_R_SM8250_DEVICE_SPECIFICATION.PDF)

34. The '339 Accused Products perform a process that includes "applying a control signal to the semi-conductor component for switching over the semi-conductor component from a first to a second operating mode." For instance, the '339 Accused Products that incorporate LPDDR5/5X memory apply a control signal to the semi-conductor component for switching over the semi-conductor component from a first to a second operating mode when a Mode Register Write-1 command issued by the memory controller to the LPDDR5/5X memory causes the

following command to write to the addressed mode register (a second operating mode) instead of the memory array (a first operating mode):

Table 201 — Command Truth Table (cont'd)

SDRAM COMMAND	BK ORG (BG, 16B, 8B)	SDR CMD PIN	DDR COMMAND PINS							CK_t edge	Notes
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6		
MASK WRITE (MWR)	Any	H	L	H	L	C0	C3	C4	C5	R1	1, 2, 3, 6, 7
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1	
	16B		BA0	BA1	BA2	BA3					
	8B		BA0	BA1	BA2	V					
WRITE (WR16 or WR)	Any	H	L	H	H	C0	C3	C4	C5	R1	1, 2, 3, 6, 7, 8
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1	
	16B		BA0	BA1	BA2	BA3					
	8B		BA0	BA1	BA2	V					
MODE REGISTER WRITE-1 (MRW-1)	Any	H	L	L	L	H	H	L	H	R1	1, 2
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	F1	
MODE REGISTER WRITE-2 (MRW-2)	Any	H	L	L	L	H	L	L	OP7	R1	1, 2
		X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	F1	
MODE REGISTER READ (MRR)	Any	H	L	L	L	H	H	L	L	R1	1, 2
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	F1	

(JEDEC Standard No. 209-5C, Page 190)

35. As another example, the '339 Accused Products that incorporate LPDDR4/4X memory apply a control signal to the semi-conductor component for switching over the semi-conductor component from a first to a second operating mode when a Mode Register Write-1 command issued by the memory controller to the LPDDR4/4X memory causes the following command to write to the addressed mode register (a second operating mode) instead of the memory array (a first operating mode):

Table 169 — Command Truth Table

	SDR Command Pins	SDR CA Pins (6)							
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Mode Register Write -1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	

(JEDEC Standard No. 209-4C, Pages 270 and 271)

36. The ’339 Accused Products perform a process that includes “applying an address signal to the semi-conductor component.” For instance, the ’339 Accused Products that incorporate LPDDR5/5X memory apply an address signal to the semi-conductor component on lines CA0 to CA6:

Table 201 — Command Truth Table (cont'd)

SDRAM COMMAND	BK ORG (BG, 16B, 8B)	SDR CMD PIN	DDR COMMAND PINS							CK_t edge	Notes
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6		
MASK WRITE (MWR)	Any	H	L	H	L	C0	C3	C4	C5	R1	1, 2, 3, 6, 7
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1	
	16B		BA0	BA1	BA2	BA3					
	8B		BA0	BA1	BA2	V					
WRITE (WR16 or WR)	Any	H	L	H	H	C0	C3	C4	C5	R1	1, 2, 3, 6, 7, 8
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1	
	16B		BA0	BA1	BA2	BA3					
	8B		BA0	BA1	BA2	V					
MODE REGISTER WRITE-1 (MRW-1)	Any	H	L	L	L	H	H	L	H	R1	1, 2
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	F1	
MODE REGISTER WRITE-2 (MRW-2)	Any	H	L	L	L	H	L	L	OP7	R1	1, 2
		X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	F1	
MODE REGISTER READ (MRR)	Any	H	L	L	L	H	H	L	L	R1	1, 2
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	F1	

(JEDEC Standard No. 209-5C, Page 190)

37. As another example, the '339 Accused Products that incorporate LPDDR4/4X memory apply an address signal to the semi-conductor component on lines CA0 to CA5:

Table 169 — Command Truth Table

	SDR Command Pins	SDR CA Pins (6)							
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Mode Register Write -1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	

(JEDEC Standard No. 209-4C, Pages 270 and 271)

38. In the ’339 Accused Products, “in the second operating mode one or more of the test data and/or semi-conductor component operating control data registers of the semi-conductor component is addressed by the address signal, and in the first operating mode one or more of the useful data memory cells.” For instance, in the ’339 Accused Products that incorporate LPDDR5/5X memory, once the Mode Register Write-1 command is issued by the memory controller to the LPDDR5/5X memory, the following command Mode Register Write-2 writes the data to the register addressed by the address signal MA0 to MA6:

SDRAM COMMAND	BK ORG (BG, 16B, 8B)	SDR CMD PIN	DDR COMMAND PINS							CK_t edge	Notes
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6		
MASK WRITE (MWR)	Any	H	L	H	L	C0	C3	C4	C5	R1	1, 2, 3, 6, 7
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1	
	16B		BA0	BA1	BA2	BA3					
	8B		BA0	BA1	BA2	V					
WRITE (WR16 or WR)	Any	H	L	H	H	C0	C3	C4	C5	R1	1, 2, 3, 6, 7, 8
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1	
	16B		BA0	BA1	BA2	BA3					
	8B		BA0	BA1	BA2	V					
MODE REGISTER WRITE-1 (MRW-1)	Any	H	L	L	L	H	H	L	H	R1	1, 2
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	F1	
MODE REGISTER WRITE-2 (MRW-2)	Any	H	L	L	L	H	L	L	OP7	R1	1, 2
		X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	F1	
MODE REGISTER READ (MRR)	Any	H	L	L	L	H	H	L	L	R1	1, 2
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	F1	

(JEDEC Standard No. 209-5C, Page 190)

39. The LPDDR5/5X Mode Registers 31 to 34 are test data registers used for DQ Calibration operation, and other registers, for example Mode Registers 35 to 40 are operating control data registers. And the LPDDR5/5X memory is addressed by the address signals, for example during the write commands MWR, WR16, WR:

Table 58 — Mode Register Assignment in LPDDR5 SDRAM (MR8 OP[1:0]=00_B)[1,2,3,4,5] (cont'd)

MR#	MA[6:0]	Access	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
31	$1F_H$	W	Lower-Byte per-bit control Register for DQ Calibration							
32	20_H	W	Upper-Byte per-bit control Register for DQ Calibration							
33	21_H	W	DQ Calibration Pattern "A"							
34	22_H	W	DQ Calibration Pattern "B"							
35	23_H	R	WCK2DQI Oscillator Count - LSB							
36	24_H	R	WCK2DQI Oscillator Count - MSB							
37	25_H	R/W	WCK2DQI interval timer run time setting							
38	26_H	R	WCK2DQO Oscillator Count - LSB							
39	27_H	R	WCK2DQO Oscillator Count - MSB							
40	28_H	R/W	WCK2DQO interval timer run time setting							

(JEDEC Standard No. 209-5C, Page 127)

SDRAM COMMAND	BK ORG (BG, 16B, 8B)	SDR CMD PIN	DDR COMMAND PINS							CK_t edge	Notes
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6		
MASK WRITE (MWR)	Any	H	L	H	L	C0	C3	C4	C5	R1	1, 2, 3, 6, 7
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1	
	16B		BA0	BA1	BA2	BA3					
	8B		BA0	BA1	BA2	V					
WRITE (WR16 or WR)	Any	H	L	H	H	C0	C3	C4	C5	R1	1, 2, 3, 6, 7, 8
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1	
	16B		BA0	BA1	BA2	BA3					
	8B		BA0	BA1	BA2	V					
MODE REGISTER WRITE-1 (MRW-1)	Any	H	L	L	L	H	H	L	H	R1	1, 2
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	F1	
MODE REGISTER WRITE-2 (MRW-2)	Any	H	L	L	L	H	L	L	OP7	R1	1, 2
		X	OP0	OP1	OP2	OP3	OP4	OP5	OP6	F1	
MODE REGISTER READ (MRR)	Any	H	L	L	L	H	H	L	L	R1	1, 2
		X	MA0	MA1	MA2	MA3	MA4	MA5	MA6	F1	

(JEDEC Standard No. 209-5C, Page 190)

40. As another example, in the '339 Accused Products that incorporate LPDDR4/4X memory, once the Mode Register Write-1 command is issued by the memory controller to the LPDDR4/4X memory, the following command Mode Register Write-2 writes the data to the register addressed by the address signal MA0 to MA5:

	SDR Command Pins	SDR CA Pins (6)							
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Mode Register Write -1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	

(JEDEC Standard No. 209-4C, Pages 270 and 271)

41. The LPDDR4/4X Mode Registers 32 and 40 are test data registers used for DQ Calibration operation, and other registers, for example Mode Registers 0 to 4 are operating control data registers. And the LPDDR4/4X memory is addressed by the address signals, for example during the write commands WR-1, MWR-1, and the read command RD-1:

Table 13 — Mode Register Assignment in LPDDR4 SDRAM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	CATR	RFU	RFU	RZQI		RFU	Latency Mode	Refresh mode
1	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	WR Lev	WLS	WL			RL		
3	DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL
4	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		
32	DQ Calibration Pattern "A" (default = 5AH)							
33	RFU							
34	RFU							
35	RFU							
36	RFU							
37	RFU							
38	RFU							
39	Reserved for testing - SDRAM will ignore							
40	DQ Calibration Pattern "B" (default = 3CH)							

	SDR Command Pins	SDR CA Pins (6)							
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Mode Register Write -1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	

(JEDEC Standard No. 209-4C, Pages 270 and 271)

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

42. In addition and/or in the alternative to its direct infringements, Qualcomm has indirectly infringed and continues to indirectly infringe one or more claims of the ’339 Patent by knowingly and intentionally inducing others, including its subsidiaries, agents, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’339 Accused Products.

43. At a minimum, Qualcomm has knowledge of the ’339 Patent since being served with this Complaint. Qualcomm also had knowledge of the ’339 Patent since receiving letters from Polaris providing details of its infringements prior to the filing of this Complaint. Since receiving notice of its infringements, Qualcomm has actively induced the direct infringements of its subsidiaries, agents, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with

the knowledge, or with willful blindness to the fact, that the acts induced constitute infringements of the ’339 Patent. Indeed, Qualcomm has intended to cause, continues to intend to cause, and has taken and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’339 Accused Products; creating and/or maintaining established distribution channels for the ’339 Accused Products into and within the United States; manufacturing the ’339 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’339 Accused Products that promote their features, specifications, and applications; promoting the incorporation of the ’339 Accused Products into end-user products; and providing technical support and/or related services for these products to purchasers in the United States.

Damages

44. On information and belief, despite having knowledge of the ’339 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’339 Patent, Qualcomm has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Qualcomm infringing activities relative to the ’339 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

45. Polaris has been damaged as a result of Qualcomm’s infringing conduct described in this Count. Qualcomm is, thus, liable to Polaris in an amount that adequately compensates Polaris for Qualcomm’s infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II

(INFRINGEMENT OF U.S. PATENT NO. 7,499,371)

46. Plaintiff incorporates the preceding paragraphs herein by reference.

47. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

48. Polaris is the owner of all substantial rights, title, and interest in and to the '371 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

49. The '371 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on March 3, 2009, after full and fair examination.

50. Qualcomm has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '371 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Qualcomm products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '371Patent, including, but not limited to, its Snapdragon 8 and X series products that incorporate LPDDR5/5X memory (collectively, "the '371 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

51. Qualcomm has directly infringed and continues to directly infringe one or more claims of the '371 Patent in this District and elsewhere in Texas and the United States.

52. Qualcomm has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 6 of the '371 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '371 Accused Products. Furthermore, Qualcomm makes and sells the '371 Accused Products outside of the United States and either

delivers those products to its customers, distributors, and/or subsidiaries in the United States or, in the case that it delivers the ’371 Accused Products outside of the United States, does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’371 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

53. Furthermore, Qualcomm directly infringes the ’371 Patent through its direct involvements in, and control of, the activities of subsidiaries and agents. Subject to Qualcomm’s direction and control, the subsidiaries and agents conduct activities that constitute direct infringement of the ’371 Patent under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing Accused Instrumentalities. Qualcomm receives direct financial benefit from such infringements by its U.S.-based subsidiaries and agents.

54. By way of illustration only, the ’371 Accused Products include each and every element of Claim 6 of the ’371 Patent. The ’371 Accused Products are a “system” that comprise the limitations of Claim 6. For instance, the ’371 Accused Products comprise “a semiconductor memory apparatus” as shown below from the data sheet for the SM8450:

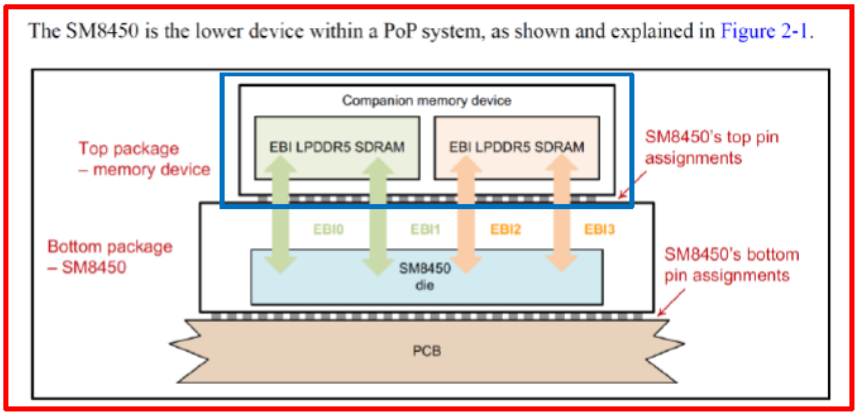
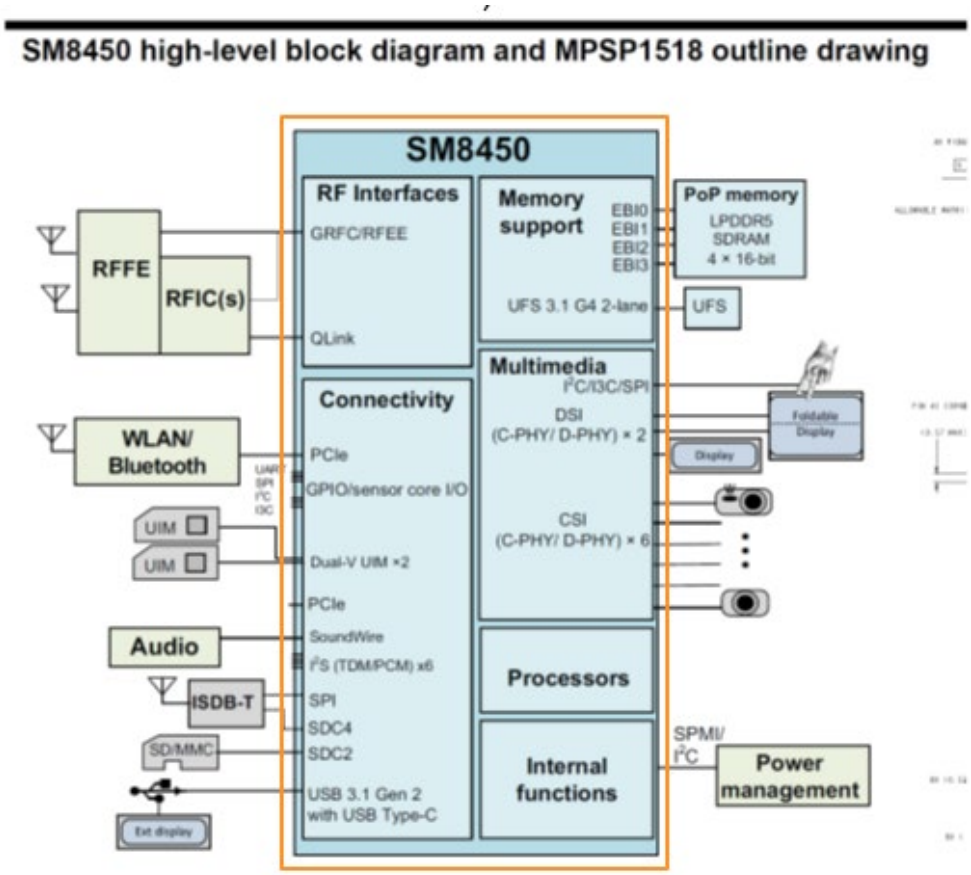


Figure 2-1 PoP system pin assignments

(80-11140-1 SM8450 SM8450P Data Sheet.pdf, Page 13)

55. The ’371 Accused Products further comprise “a processor unit which is configured to: transmit a command instruction to the semiconductor memory apparatus, wherein the command instruction is at least one of a write instruction and a read instruction.” For instance, the ’371 Accused Products such as the SM8450 incorporate a processor unit which is configured to transmit a command instruction to the semiconductor memory apparatus:



(80-11140-1 SM8450 SM8450P Data Sheet.pdf, Page 1)

2.3.2 Pin descriptions: MSM top

Descriptions of top pins are presented in Table 2-5 and Table 2-6.

Table 2-5 MSM top pin descriptions – general pins

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_F15	DDR_RESET_N	PX1	DO	LPDDR5 reset (shared by EBIs)
M_C6	EBI0_CA_0	EBI	DO	EBI0 LPDDR5 command/address bit 0
M_E6	EBI0_CA_1	EBI	DO	EBI0 LPDDR5 command/address bit 1
M_D7	EBI0_CA_2	EBI	DO	EBI0 LPDDR5 command/address bit 2
M_D8	EBI0_CA_3	EBI	DO	EBI0 LPDDR5 command/address bit 3
M_C8	EBI0_CA_4	EBI	DO	EBI0 LPDDR5 command/address bit 4
M_E9	EBI0_CA_5	EBI	DO	EBI0 LPDDR5 command/address bit 5
M_C9	EBI0_CA_6	EBI	DO	EBI0 LPDDR5 command/address bit 6
M_F8	EBI0_CK_C	EBI	DO	EBI0 LPDDR5 differential clock - negative
M_F7	EBI0_CK_T	EBI	DO	EBI0 LPDDR5 differential clock - positive
M_C7	EBI0_CS_0	EBI	DO	EBI0 LPDDR5 chip select 0
M_B7	EBI0_CS_1	EBI	DO	EBI0 LPDDR5 chip select 1
M_C4	EBI0_DMI_0	EBI	DO	EBI0 LPDDR5 data mask for byte 0
M_C11	EBI0_DMI_1	EBI	DO	EBI0 LPDDR5 data mask for byte 1
M_E1	EBI0_DQ_0	EBI	B	EBI0 LPDDR5 data bit 0
M_C1	EBI0_DQ_1	EBI	B	EBI0 LPDDR5 data bit 1

(80-11140-1 SM8450 SM8450P Data Sheet.pdf, Page 52)

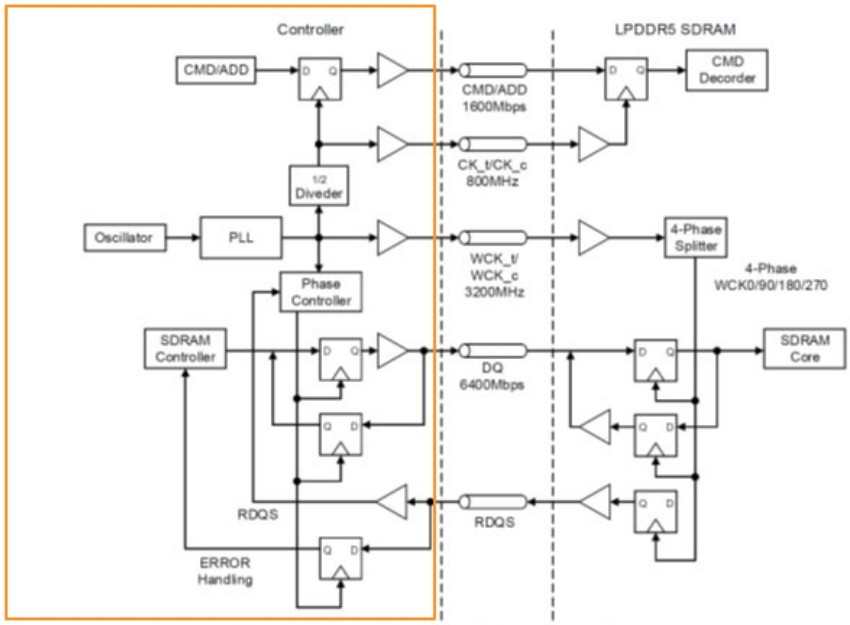


Figure 11 — Block Diagram of an Example System: CKR=4:1

(JEDEC Standard No. 209-5C, Page 25)

56. The ’371 Accused Products processor unit is further configured to “communicate a data signal with the semiconductor memory apparatus” and “transmit a data clock signal to latch the data signal.” For instance, the ’371 Accused Products such as the SM8450 incorporate a processor unit that is configured to communicate a data signal with the semiconductor memory apparatus and transmit a data clock signal to latch the data signal:

M_E1	EBI0_DQ_0	EBI	B	EBI0 LPDDR5 data bit 0
M_C1	EBI0_DQ_1	EBI	B	EBI0 LPDDR5 data bit 1
M_E13	EBI0_DQ_10	EBI	B	EBI0 LPDDR5 data bit 10
M_C13	EBI0_DQ_11	EBI	B	EBI0 LPDDR5 data bit 11
M_E11	EBI0_DQ_12	EBI	B	EBI0 LPDDR5 data bit 12
M_B10	EBI0_DQ_13	EBI	B	EBI0 LPDDR5 data bit 13
M_D10	EBI0_DQ_14	EBI	B	EBI0 LPDDR5 data bit 14
M_F10	EBI0_DQ_15	EBI	B	EBI0 LPDDR5 data bit 15
M_D2	EBI0_DQ_2	EBI	B	EBI0 LPDDR5 data bit 2
M_B2	EBI0_DQ_3	EBI	B	EBI0 LPDDR5 data bit 3
M_E4	EBI0_DQ_4	EBI	B	EBI0 LPDDR5 data bit 4
M_B5	EBI0_DQ_5	EBI	B	EBI0 LPDDR5 data bit 5
M_D5	EBI0_DQ_6	EBI	B	EBI0 LPDDR5 data bit 6
M_F5	EBI0_DQ_7	EBI	B	EBI0 LPDDR5 data bit 7
M_D14	EBI0_DQ_8	EBI	B	EBI0 LPDDR5 data bit 8
M_B14	EBI0_DQ_9	EBI	B	EBI0 LPDDR5 data bit 9

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
M_B12	EBI0_RDQS_T_1	EBI	B	EBI0 LPDDR5 differential read data strobe for byte 1 - negative
M_E3	EBI0_WCK_C_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 - positive
M_E12	EBI0_WCK_C_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 - positive
M_F3	EBI0_WCK_T_0	EBI	DO	EBI0 LPDDR5 differential data clock for byte 0 - negative
M_F12	EBI0_WCK_T_1	EBI	DO	EBI0 LPDDR5 differential data clock for byte 1 - negative
M_AE9	EBI1_CA_0	EBI	DO	EBI1 LPDDR5 command/address bit 0

(80-11140-1 SM8450 SM8450P Data Sheet.pdf, Page 52 and 53)

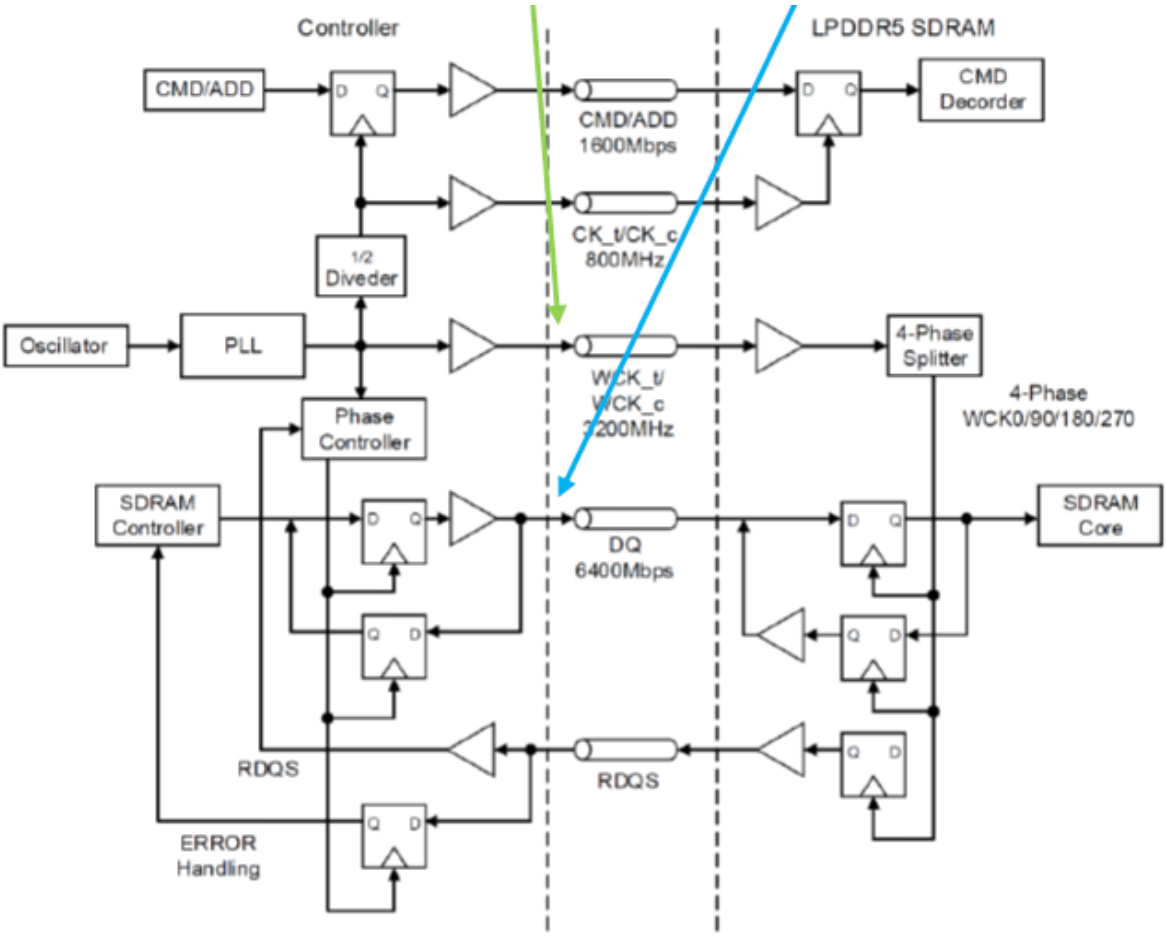


Figure 11 — Block Diagram of an Example System: CKR=4:1

(JEDEC Standard No. 209-5C, Page 25)

57. The ’371 Accused Products processor unit is further configured to “set a preamble, wherein the preamble is a period of time between a first edge of the data clock signal and a first bit of the data signal.” For instance, the ’371 Accused Products such as the SM8450 incorporate a processor unit that sets a preamble, wherein the preamble is a period of time between a first edge of the data clock signal and a first bit of the data signal, and wherein the data clock signal is present only during a read or write operation initiated by the command instruction and during which data is read or written from or to the semiconductor memory apparatus, wherein the preamble is set by

setting a number of clock cycles of the data clock signal in the period of time defined by the preamble:

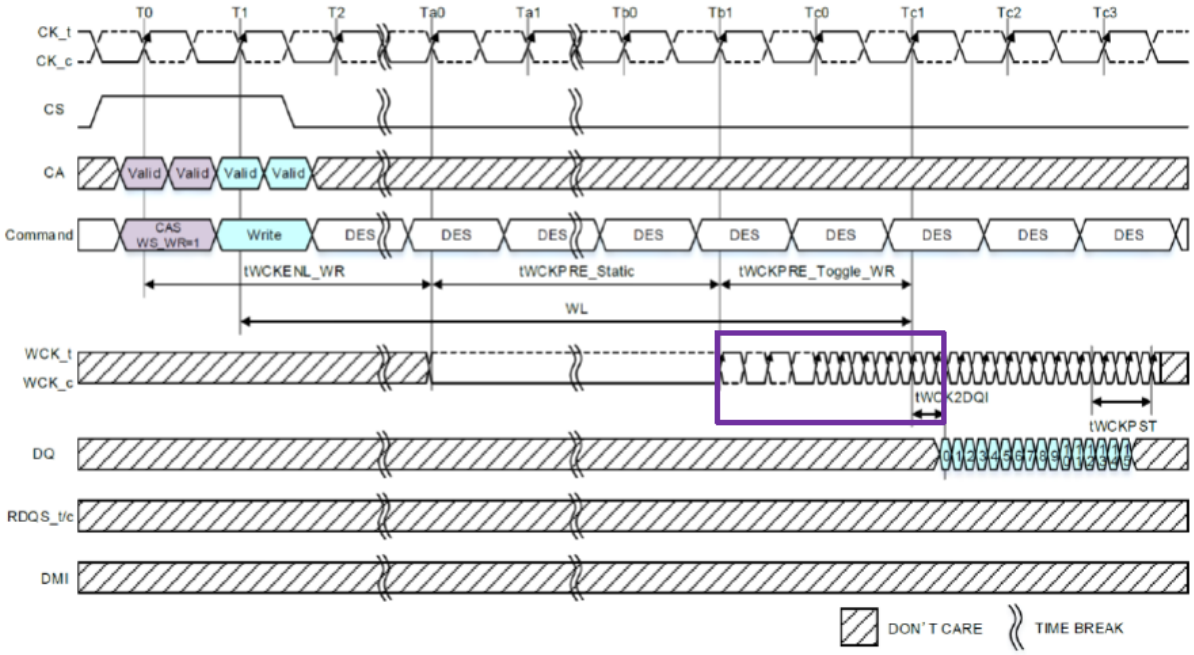


Figure 71 — WCK2CK Sync Operation Followed by a WRITE Command

(JEDEC Standard No. 209-5C, Page 197)

58. The '371 Accused Products processor unit is further configured "wherein the data clock signal is present only during a read or write operation initiated by the command instruction and during which data is read or written from or to the semiconductor memory apparatus." For instance, the '371 Accused Products such as the SM8450 incorporate a processor unit wherein the data clock signal is present only during a read or write operation initiated by the command instruction and during which data is read or written from or to the semiconductor memory apparatus:

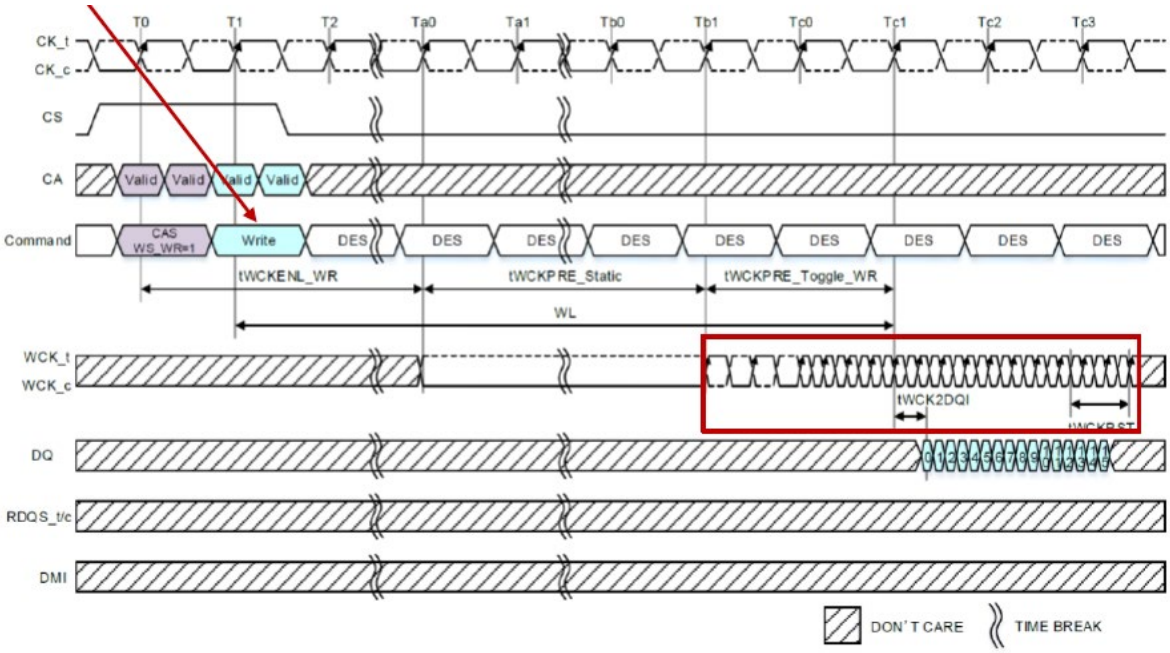


Figure 71 — WCK2CK Sync Operation Followed by a WRITE Command

(JEDEC Standard No. 209-5C, Page 197)

59. The '371 Accused Products processor unit is further configured "wherein the preamble is set by setting a number of clock cycles of the data clock signal in the period of time defined by the preamble." For instance, the '371 Accused Products such as the SM8450 incorporate a processor unit wherein the preamble is set by setting a number of clock cycles of the data clock signal in the period of time defined by the preamble:

Table 204 — WCK2CK Sync AC Parameters for WRITE Operation[1,2]

WCK:CK Ratio	Data Rate [Mbps]		CK Frequency [Mbps]		WL(SetA) [nCK]	WL(SetB) [nCK]	tWCKENL_WR(SetA) [nCK]	tWCKENL_WR(SetB) [nCK]	tWCKPRE_Static [nCK]	tWCKPRE toggle_WR [nCK]	tWCKPRE total_WR [nCK]
	Lower Limit(>)	Upper Limit(≤)	Lower Limit(>)	Upper Limit(≤)							
2:1	40	533	10	133	4	4	1	1	1	3	4
	533	1067	133	267	4	6	0	2	2	3	5
	1067	1600	267	400	6	8	1	3	2	4	6
	1600	2133	400	533	8	10	2	4	3	4	7
	2133	2750	533	688	8	14	1	7	4	4	8
	2750	3200	688	800	10	16	3	9	4	4	8
4:1	40	533	5	67	2	2	0	0	1	2	3
	533	1067	67	133	2	3	0	1	1	2	3
	1067	1600	133	200	3	4	1	2	1	2	3
	1600	2133	200	267	4	5	1	2	2	2	4
	2133	2750	267	344	4	7	1	4	2	2	4
	2750	3200	344	400	5	8	2	5	2	2	4
	3200	3733	400	467	6	9	2	5	3	2	5
	3733	4267	467	533	6	11	2	7	3	2	5
	4267	4800	533	600	7	12	3	8	3	2	5
	4800	5500	600	688	8	14	3	9	4	2	6
	5500	6000	688	750	9	15	4	10	4	2	6
	6000	6400	750	800	9	16	4	11	4	2	6
	6400	7500	800	937.5	11	19	5	13	5	2	7
	7500	8533	937.5	1066.5	12	22	5	15	6	2	8

NOTE 1 tWCKENL_WR = WL + 1 - tWCKPRE_total_WR

NOTE 2 tWCKPRE_total_WR = tWCKPRE_toggle_WR + tWCKPRE_Static

(JEDEC Standard No. 209-5C, Page 198)

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

60. In addition and/or in the alternative to its direct infringements, Qualcomm has indirectly infringed and continues to indirectly infringe one or more claims of the ’371 Patent by knowingly and intentionally inducing others, including its subsidiaries, agents, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’371 Accused Products.

61. At a minimum, Qualcomm has knowledge of the ’371 Patent since being served with this Complaint. Qualcomm also had knowledge of the ’371 Patent since receiving letters from Polaris providing details of its infringements prior to the filing of this Complaint. Since receiving notice of its infringements, Qualcomm has actively induced the direct infringements of its

subsidiaries, agents, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’371 Patent. Indeed, Qualcomm has intended to cause, continues to intend to cause, and has taken and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’371 Accused Products; creating and/or maintaining established distribution channels for the ’371 Accused Products into and within the United States; manufacturing the ’371 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’371 Accused Products that promote their features, specifications, and applications; promoting the incorporation of the ’371 Accused Products into end-user products; and providing technical support and/or related services for these products to purchasers in the United States.

Damages

62. On information and belief, despite having knowledge of the ’371 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’371 Patent, Qualcomm has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Qualcomm’s infringing activities relative to the ’371 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

63. Polaris has been damaged as a result of Qualcomm’s infringing conduct described in this Count. Qualcomm is, thus, liable to Polaris in an amount that adequately compensates

Polaris for Qualcomm's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT III

(INFRINGEMENT OF U.S. PATENT NO. USP 7,872,936)

64. Plaintiff incorporates the preceding paragraphs herein by reference.

65. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

66. Polaris is the owner of all substantial rights, title, and interest in and to the '936 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

67. The '936 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on January 18, 2011, after full and fair examination.

68. Qualcomm has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '936 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Qualcomm products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '936 Patent, including, but not limited to, its Snapdragon products that incorporate MCeP-based stack of AP and LPDDR4X/5/5X memory (collectively, "the '936 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

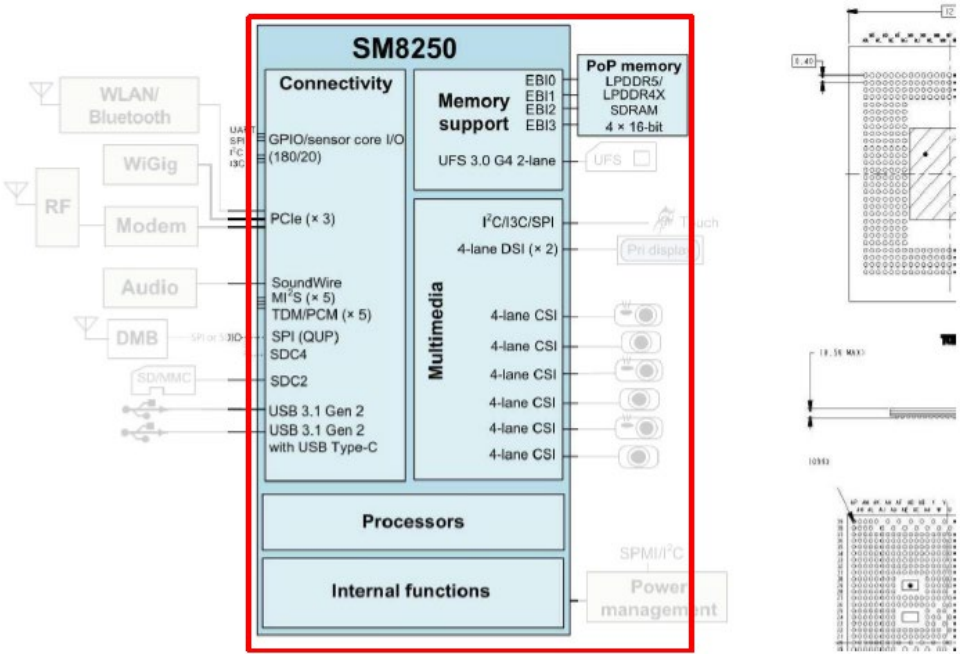
69. Qualcomm has directly infringed and continues to directly infringe one or more claims of the '936 Patent in this District and elsewhere in Texas and the United States.

70. Qualcomm has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’936 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the ’936 Accused Products. Furthermore, Qualcomm makes and sells the ’936 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States or, in the case that it delivers the ’936 Accused Products outside of the United States, does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’936 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

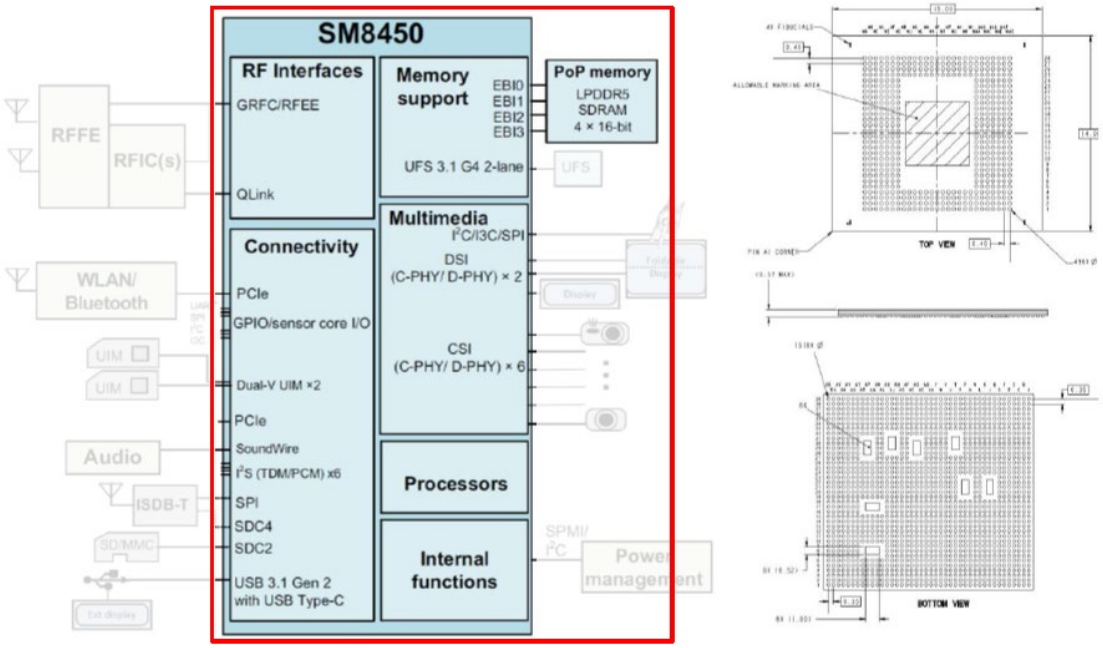
71. Furthermore, Qualcomm directly infringes the ’936 Patent through its direct involvements in, and control of, the activities of subsidiaries and agents. Subject to Qualcomm’s direction and control, the subsidiaries and agents conduct activities that constitute direct infringement of the ’936 Patent under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing Accused Instrumentalities. Qualcomm receives direct financial benefit from such infringements by its U.S.-based subsidiaries and agents.

72. By way of illustration only, the ’936 Accused Products include each and every element of Claim 1 of the ’936 Patent. The ’936 Accused Products are “[a] multi-chip memory device” that comprise all of the limitations of Claim 1 of the ’936 Patent including “a plurality of stacked semiconductor die.” For instance, the SM8250 is a multi-chip memory device comprising a plurality of stacked semiconductor die:

SM8250 high-level block diagram and 1099 (SM8250–LPDDR5) drawing



SM8450 high-level block diagram and MPSP1518 outline drawing



(80_PL546_1_R_SM8250_DEVICE_SPECIFICATION.pdf, page 1)

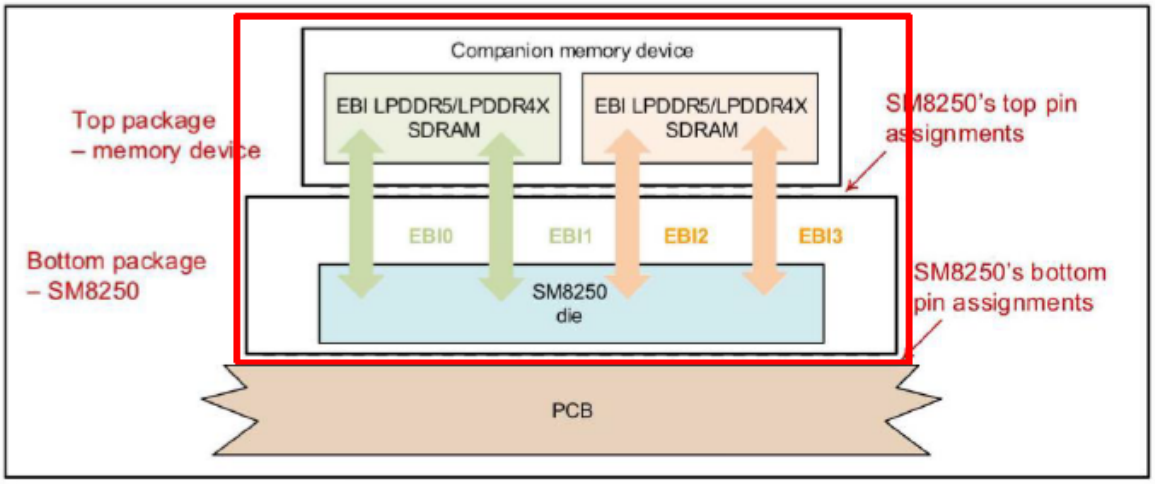


Figure 2-1 PoP system pin assignments

(80_PL546_1_R_SM8250_DEVICE_SPECIFICATION.pdf, page 10)

The application processor uses MCeP style PoP structure for the Qualcomm Snapdragon 855 application processor. The twin wirebond memory packages are mounted over the lower application processor, which was flip-chip mounted over 3 layer Embedded Trace Substrate (ETS) 10 um L/S. The application processor die with Cu pillar 25 um height and 100 um pitch is thermal compression bonded over NCF underfill.

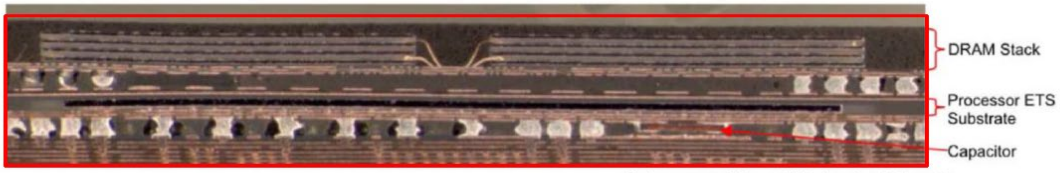


Photo source: Prismark/Binghamton University

12.3 x 12.4mm MCeP® style PoP
- 1.3mm height, with 4 die DRAM stack
- Reduced substrate thicknesses

Samsung LPDDR4X with 8 (1GB) Die
- Gold wire bonds
- Die: 50µm thick; FOW: 50µm
- 120µm EMC thickness over die

Processor Package
- 100µm thick die; 25µm Cu bump height
- TCB with NCP at <100µm pitch
- 4 capacitors (0402) between bottom solder balls
- 2L "Upper substrate": 100µm thick
- 3L Embedded Trace Substrate (ETS): 130µm thick, 10µm L/S, 55µm via diameter

(https://eps.ieee.org/images/files/HIR_2019/HIR1_ch07_mobile.pdf)

73. The '936 Accused Products further comprise a plurality of stacked semiconductor die comprising "a plurality of memory die." For instance, the SM8250 further comprises a plurality of stacked semiconductor die comprising a plurality of memory die:

The application processor uses MCeP style PoP structure for the Qualcomm Snapdragon 855 application processor. The twin wirebond memory packages are mounted over the lower application processor, which was flip-chip mounted over 3 layer Embedded Trace Substrate (ETS) 10 um L/S. The application processor die with Cu pillar 25 um height and 100 um pitch is thermal compression bonded over NCF underfill.

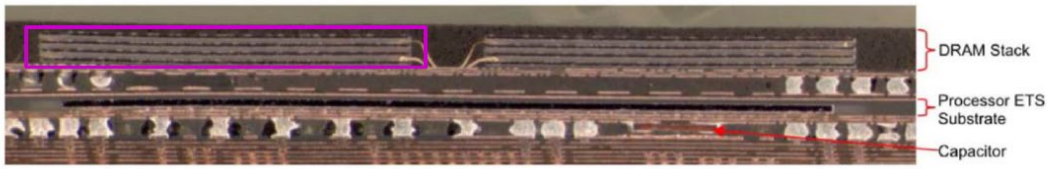


Photo source: Prismark/Binghamton University

12.3 x 12.4mm MCeP® style PoP
- 1.3mm height, with 4 die DRAM stack
- Reduced substrate thicknesses

Samsung LPDDR4X with 8 (1GB) Die
- Gold wire bonds
- Die: 50µm thick; FOW: 50µm
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Processor Package
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- 4 capacitors (0402) between bottom solder balls
- 2L "Upper substrate": 100µm thick
- 3L Embedded Trace Substrate (ETS): 130µm thick, 10µm L/S, 55µm via diameter

(https://eps.ieee.org/images/files/HIR_2019/HIR1_ch07_mobile.pdf)

74. The '936 Accused Products further comprise a plurality of stacked semiconductor die comprising "a memory controller and interface die, wherein the plurality of memory die and the memory controller comprise a single stack of die." For instance, the SM8250 further comprises a plurality of stacked semiconductor die comprising a memory controller and interface die, wherein the plurality of memory die and the memory controller comprise a single stack of die:

The application processor uses MCeP style PoP structure for the Qualcomm Snapdragon 855 application processor. The twin wirebond memory packages are mounted over the lower application processor, which was flip-chip mounted over 3 layer Embedded Trace Substrate (ETS) 10 um L/S. The application processor die with Cu pillar 25 um height and 100 um pitch is thermal compression bonded over NCF underfill.

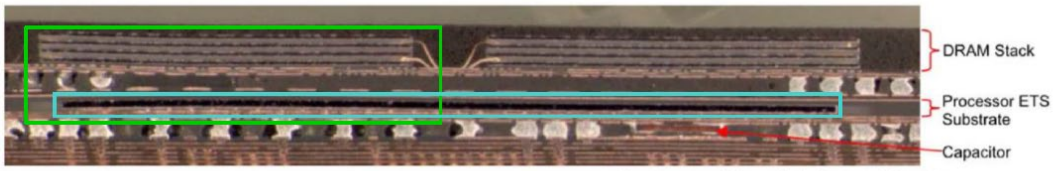

Photo source: Prismark/Binghamton University

12.3 x 12.4mm MCeP® style PoP
- 1.3mm height, with 4 die DRAM stack
- Reduced substrate thicknesses

Samsung LPDDR4X with 8 (1GB) Die
- Gold wire bonds
- Die: 50µm thick; FOW: 50µm
- 120µm EMC thickness over die

Processor Package
- 100µm thick die; 25µm Cu bump height
- TCB with NCP at <100µm pitch
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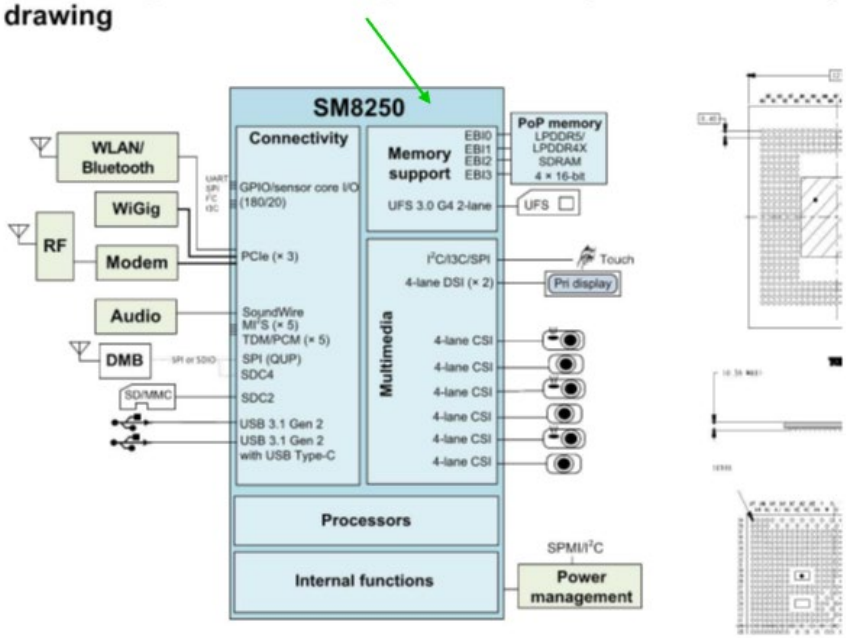
- 3L Embedded Trace Substrate (ETS): 130µm thick, 10µm L/S, 55µm via diameter

(https://eps.ieee.org/images/files/HIR_2019/HIR1_ch07_mobile.pdf)

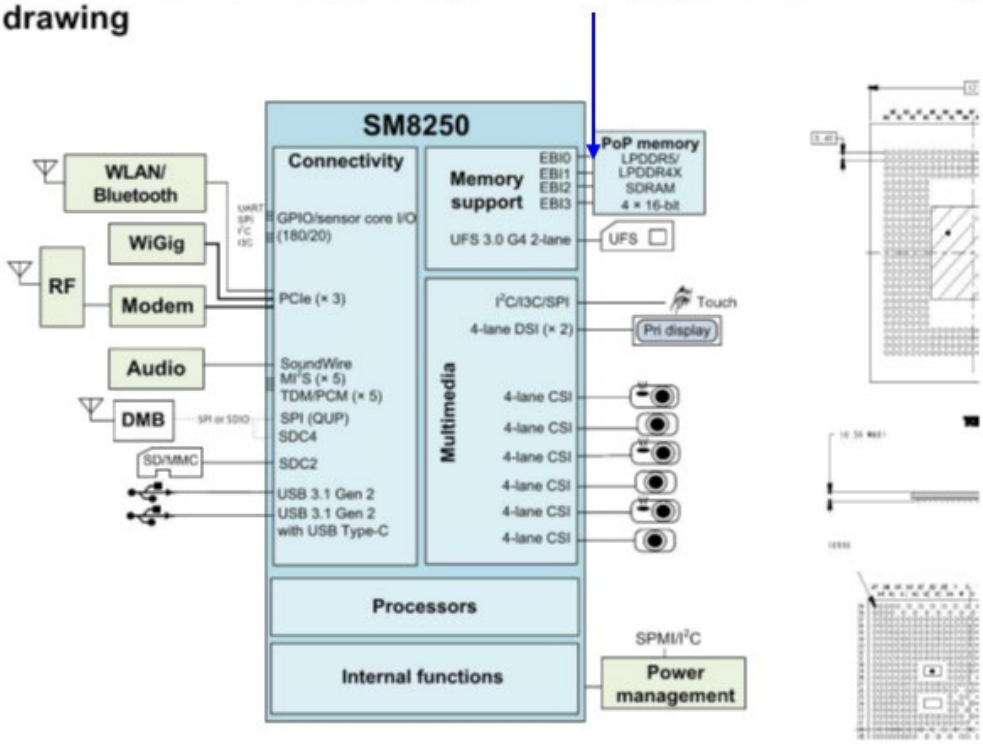
SM8250 high-level block diagram and 1099 (SM8250–LPDDR5) drawing



(80_PL546_1_R_SM8250_DEVICE_SPECIFICATION.pdf, page 1)

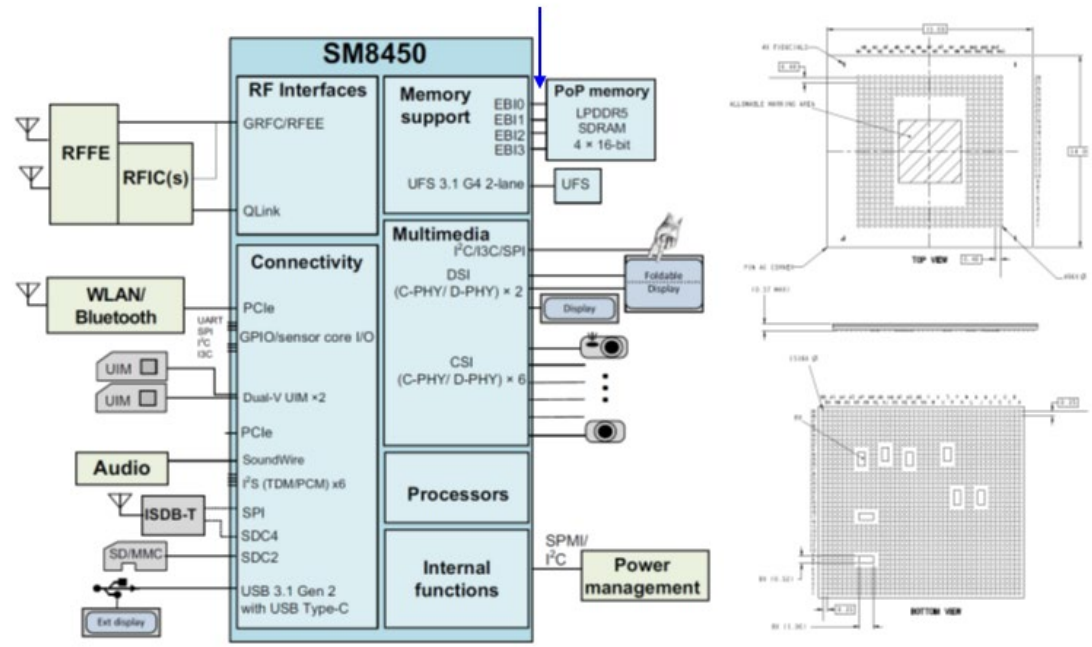
75. The ’936 Accused Products further comprise a plurality of stacked semiconductor die comprising “a plurality of bonded connections, the bonded connections coupling an internal interface of the memory controller with an internal interface of each of the plurality of memory die.” For instance, the SM8250 further comprises a plurality of stacked semiconductor die comprising a plurality of bonded connections, the bonded connections coupling an internal interface of the memory controller with an internal interface of each of the plurality of memory die:

SM8250 high-level block diagram and 1099 (SM8250–LPDDR5) drawing



(80_PL546_1_R_SM8250_DEVICE_SPECIFICATION.pdf, page 1)

SM8450 high-level block diagram and MPSP1518 outline drawing



(80-11140-1 SM8450 SM8450P Data Sheet.pdf, page 1)

The application processor uses MCeP style PoP structure for the Qualcomm Snapdragon 855 application processor. The twin wirebond memory packages are mounted over the lower application processor, which was flip-chip mounted over 3 layer Embedded Trace Substrate (ETS) 10 um L/S. The application processor die with Cu pillar 25 um height and 100 um pitch is thermal compression bonded over NCF underfill.

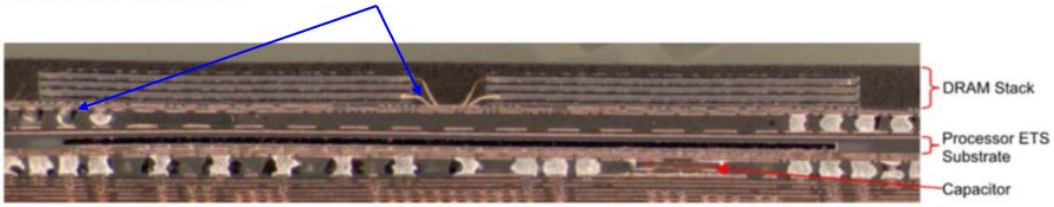


Photo source: Prismark/Binghamton University

12.3 x 12.4mm MCeP® style PoP
- 1.3mm height, with 4 die DRAM stack
- Reduced substrate thicknesses

Samsung LPDDR4X with 8 (1GB) Die
- Gold wire bonds
- Die: 50µm thick; FOW: 50µm
- 120µm EMC thickness over die

Processor Package
- 100µm thick die; 25µm Cu bump height
- TCB with NCP at <100µm pitch
- 4 capacitors (0402) between bottom solder balls
- 2L "Upper substrate": 100µm thick
- 3L Embedded Trace Substrate (ETS); 130µm thick, 10µm L/S, 55µm via diameter

(https://eps.ieee.org/images/files/HIR_2019/HIR1_ch07_mobile.pdf)

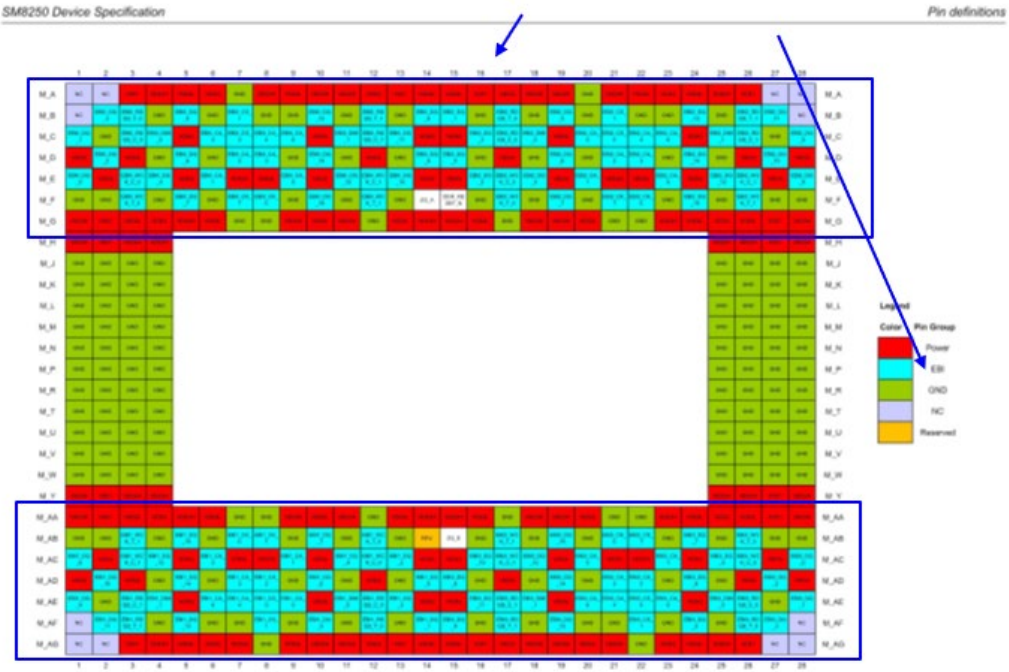


Figure 2-3 LPDDR5 top pin assignments

(80_PL546_1_R_SM8250_DEVICE_SPECIFICATION.pdf, page 39)

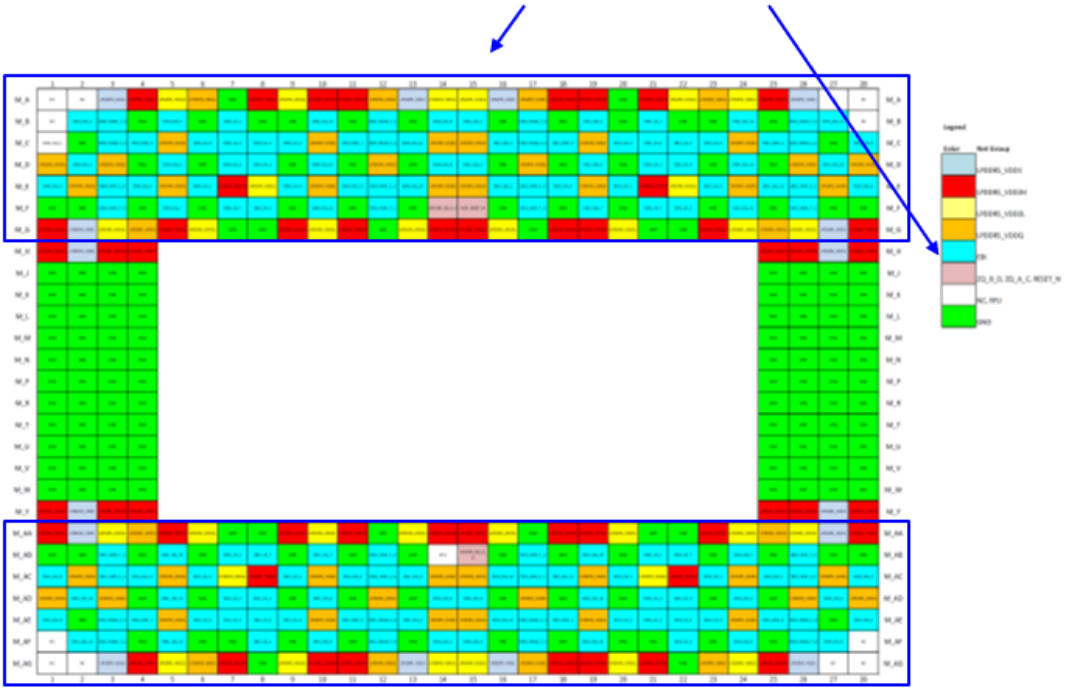
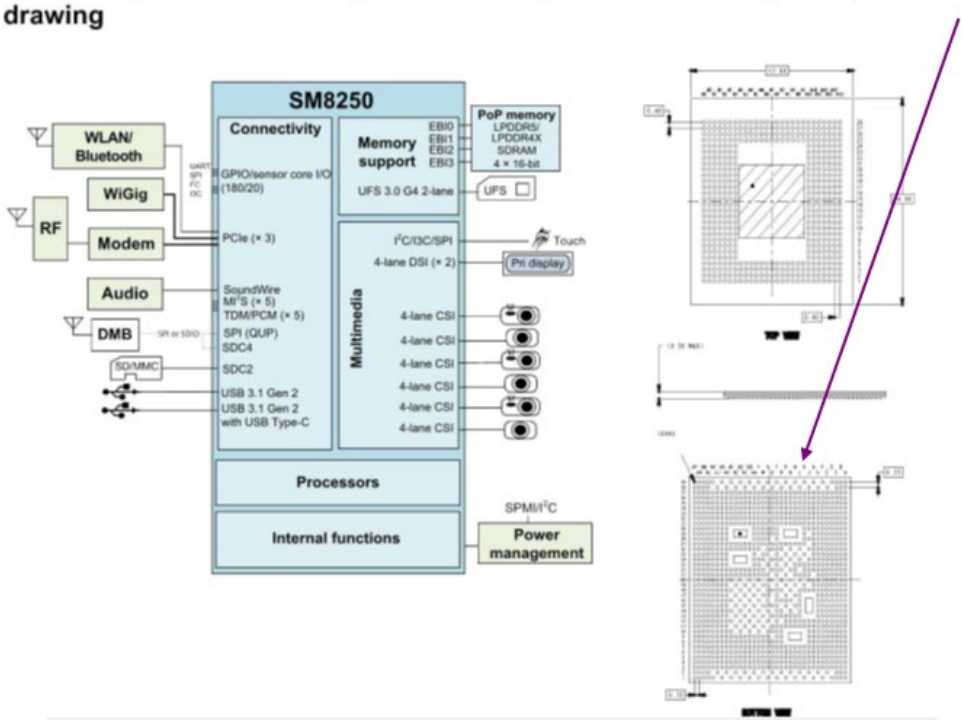


Figure 2-3 SM8450 top pin LPDDR5 assignments (top view)

(80-11140-1 SM8450 SM8450P Data Sheet.pdf, page 51)

76. The ’936 Accused Products further comprise a plurality of stacked semiconductor die comprising “a plurality of pins coupled to an external interface of the memory controller and interface die.” For instance, the SM8250 further comprises a plurality of stacked semiconductor die comprising a plurality of pins coupled to an external interface of the memory controller and interface die, including at least the ZQ calibration pins/IOs that are an external interface of the memory controller and interface die:

SM8250 high-level block diagram and 1099 (SM8250–LPDDR5)/1017 (SM8250-drawing



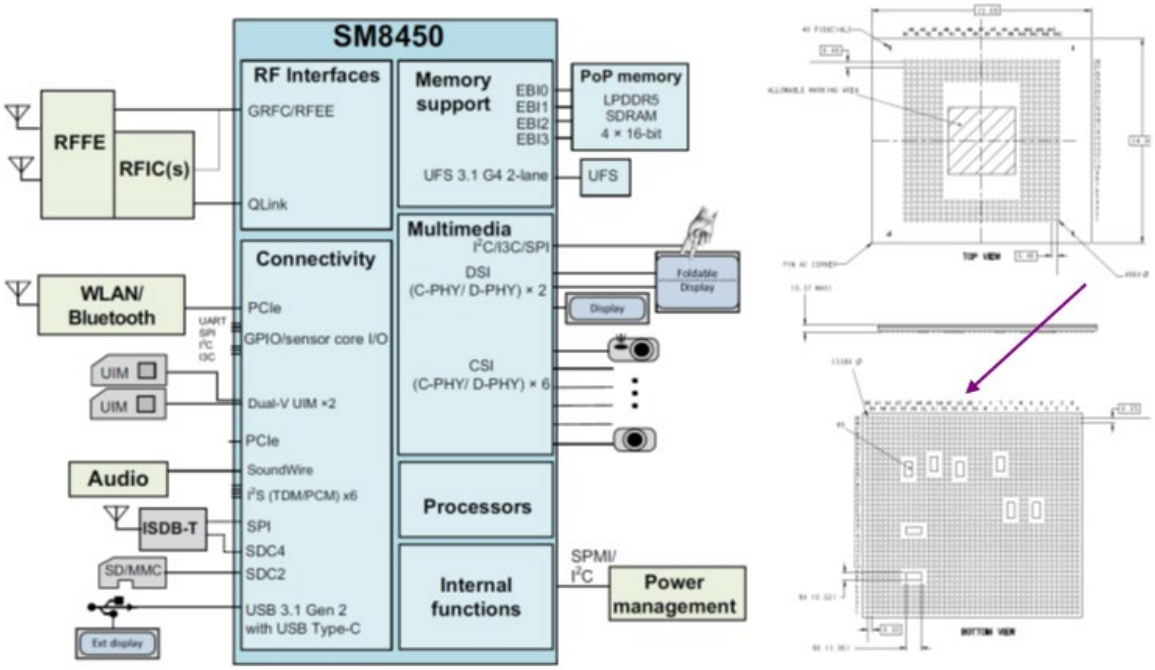
(80_PL546_1_R_SM8250_DEVICE_SPECIFICATION.pdf, page 1)

Table 2-2 Bottom pin descriptions – general pins (cont.)

Pad #		Pad name	Pad characteristics [1]		Functional description
LPDDR4X	LPDDR5		Pad voltage	Pad type	
AM21	AM23	DSI1_B0_LN0_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 0 – minus MIPI DSI 1 (CPHY), trio lane 0 – B
AL20	AL22	DSI1_B1_CLK_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential clock – plus MIPI DSI 1 (CPHY), trio lane 1 – B
AK21	AK23	DSI1_B2_LN2_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 2 – minus MIPI DSI 1 (CPHY), trio lane 2 – B
AM22	AM24	DSI1_C0_LN1_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 1 – plus MIPI DSI 1 (CPHY), trio lane 0 – C
AL21	AL23	DSI1_C1_CLK_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential clock – minus MIPI DSI 1 (CPHY), trio lane 1 – C
AK22	AK24	DSI1_C2_LN3_P	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – plus MIPI DSI 1 (CPHY), trio lane 2 – C
AK23	AK25	DSI1_NC_LN3_M	DSI	AI, AO	MIPI DSI 1 (DPHY), differential lane 3 – minus MIPI DSI 1 (CPHY), no connect
A7	A9	EBI02_CAL	PX_3	AI	EBI0/1 LPDDR5/LPDDR4X calibration resistor
AP30	AP32	EBI13_CAL	PX_3	AI	EBI2/3 LPDDR5/LPDDR4X calibration resistor
U31	U33	DP_AUX_M	–	AI, AO	DisplayPort auxiliary channel – minus
U32	U34	DP_AUX_P	–	AI, AO	DisplayPort auxiliary channel – plus

(80_PL546_1_R_SM8250_DEVICE_SPECIFICATION.pdf, page 18)

SM8450 high-level block diagram and MPSP1518 outline drawing



(80-11140-1 SM8450 SM8450P Data Sheet.pdf, page 1)

SM8450/SM8450P Data Sheet *Pin definitions*

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
L2	CSI4_B0_LN0_P	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 - positive MIPI CSI 4 (C-PHY), trio lane 0 – B
L1	CSI4_C0_LN0_M	CSI	AI, AO	MIPI CSI 4 (D-PHY), differential lane 0 - minus MIPI CSI 4 (C-PHY), trio lane 0 – C
				MIPI CSI 5 (C-PHY), trio lane 2 – A
U5	CSI5_B2_LN3_P	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 3 - positive MIPI CSI 5 (C-PHY), trio lane 2 – B
U4	CSI5_C2_LN3_M	CSI	AI, AO	MIPI CSI 5 (D-PHY), differential lane 3 - minus MIPI CSI 5 (C-PHY), trio lane 2 – C
E7	EBI02_CAL	LPDDR5_VDDQ	AI	EBI calibration resistor. The EBI02_CAL pin should be connected to S3H/PM8450 through a 240 Ω ±1% resistor.
AY32	EBI13_CAL	LPDDR5_VDDQ	AI	EBI calibration resistor. The EBI13_CAL pin should be connected to S3H/PM8450 through a 240 Ω ±1% resistor.
A24	LPDDR5_ZQ_A_C	LPDDR5_VDDQ	AI	ZQ calibration reference: The ZQ_A_C pin should be connected to VDDQ (S3H/PM8450) through a 240 Ω ±1% resistor. See LPDDR5 specification.

(80-11140-1 SM8450 SM8450P Data Sheet.pdf, page 19)

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

77. In addition and/or in the alternative to its direct infringements, Qualcomm has indirectly infringed and continues to indirectly infringe one or more claims of the ’936 Patent by knowingly and intentionally inducing others, including its subsidiaries, agents, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’936 Accused Products.

78. At a minimum, Qualcomm has knowledge of the ’936 Patent since being served with this Complaint. Qualcomm also had knowledge of the ’936 Patent since receiving letters from Polaris providing details of its infringements prior to the filing of this Complaint. Since receiving notice of its infringements, Qualcomm has actively induced the direct infringements of its subsidiaries, agents distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’936 Patent. Indeed, Qualcomm has intended to cause, continues to intend to cause, and has taken and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’936 Accused Products; creating and/or maintaining established distribution channels for the ’936 Accused Products into and within the United States; manufacturing the ’936 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’936 Accused Products that promote their features, specifications, and applications; promoting the incorporation of the ’936 Accused Products into end-user products; and providing technical support and/or related services for these products to purchasers in the United States.

Damages

79. On information and belief, despite having knowledge of the ’936 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’936 Patent, Qualcomm has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Qualcomm’s infringing activities relative to the ’936 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

80. Polaris has been damaged as a result of Qualcomm’s infringing conduct described in this Count. Qualcomm is, thus, liable to Polaris in an amount that adequately compensates Polaris for Qualcomm’s infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT IV

(INFRINGEMENT OF U.S. PATENT NO. USP 8,161,344)

81. Plaintiff incorporates the preceding paragraphs herein by reference.

82. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

83. Polaris is the owner of all substantial rights, title, and interest in and to the ’344 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

84. The ’344 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on April 17, 2012, after full and fair examination.

85. Qualcomm has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the ’344 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Qualcomm products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the ’344 Patent, including, but not limited to, its Snapdragon 8 and X Series products incorporating LPDDR5X memory (collectively, “the ’344 Accused Products”).

Direct Infringement (35 U.S.C. § 271(a))

86. Qualcomm has directly infringed and continues to directly infringe one or more claims of the ’344 Patent in this District and elsewhere in Texas and the United States.

87. Qualcomm has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 7 (which depends from Claim 1) of the ’344 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the ’344 Accused Products. Furthermore, Qualcomm makes and sells the ’344 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States or, in the case that it delivers the ’344 Accused Products outside of the United States, does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’344 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

88. Furthermore, Qualcomm directly infringes the ’344 Patent through its direct involvements in, and control of, the activities of subsidiaries and agents. Subject to Qualcomm’s direction and control, the subsidiaries and agents conduct activities that constitute direct infringement of the ’344 Patent under 35 U.S.C. § 271(a) by making, using, offering for sale,

selling, and/or importing Accused Instrumentalities. Qualcomm receives direct financial benefit from such infringements by its U.S.-based subsidiaries and agents.

89. By way of illustration only, the ’344 Accused Products include each and every element of Claim 7 of the ’344 Patent. The ’344 Accused Products include “[a] circuit for creating an error coding data block for a first data block” that incorporates all of the limitations of independent Claim 1 and dependent Claim 7. The ’344 Accused Products comprise “a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding,” for example as indicated by the JEDEC standard for LPDDR5/5X memory:

JEDEC Standard No. 209-5C
Page 472

7.7.8.6 ECC and DBI – Order of Operations

When transmitting Write data, the Controller can first perform DBI/DMI encoding of the data (if DBI is enabled). DBI encoding will follow the same rules as on LPDDR4. It can then perform ECC generation on the resulting Data and DMI bits (if ECC is enabled). It is important to perform ECC generation after the DBI encoding, because Masked writes can alter the data during DBI encoding. The modified data is used for calculating the data ECC in all cases. The 6-bit DMI ECC and 9-bit data ECC are both transmitted on the RDQS_t pin and sent at the bit-times previously defined. Figure 282 illustrates the data flow.

When receiving Write data, the DRAM will first perform checking & correction on the DMI ECC. In parallel, it will perform ECC checking and correction on the data itself. Once the DMI is verified, it will proceed to perform DBI decoding of the data. DBI decoding follows the same rules as on LPDDR4. The Data ECC can be checked prior to DBI decoding due to the unique characteristics of the ECC code (the nature of the code is such that inverting an entire beat of the data would not change the ECC). The Write operation diagram illustrates this data flow.

(JEDEC Standard No. 209-5C, Page 472)

90. The ’344 Accused Products further comprise “a second error coding path adapted to selectively create a second error coding data block in accordance with a second error coding”:

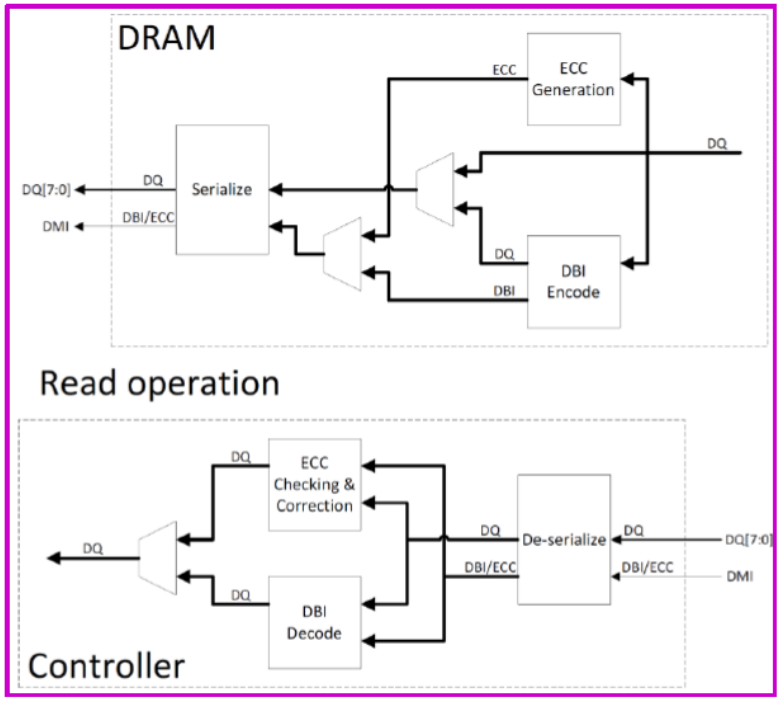


Figure 283 — Data Flow on a Memory Read Operation

(JEDEC Standard No. 209-5C, Page 473)

JEDEC Standard No. 209-5C
Page 473

7.7.8.6 ECC and DBI – Order of Operations (cont'd)

When transmitting Read data, the DRAM will either perform DBI encoding (if DBI is enabled), or ECC generation on the data (if ECC is enabled). Which operation is performed will depend on the features enabled. Since Read DBI and Link ECC are mutually exclusive, it never needs to perform both functions, and it never needs to compute or transmit ECC on the DBI bits. The DBI encoding follows the same rules as on LPDDR4. Figure 283 illustrates the data flow.

When receiving Read data, the Controller would want to perform either DBI decoding (if DBI is enabled), or ECC checking & correction (if ECC is enabled), depending on the features enabled. DBI decoding follows the same rules as on LPDDR4. The Read operation diagram illustrates this data flow.

(JEDEC Standard No. 209-5C, Page 473)

91. The '344 Accused Products further meet the limitation that "the first error coding path and the second error coding path being selected as a function of a control indicator, and at least the first error coding path comprising a data arrangement alteration device":

JEDEC Standard No. 209-5C
Page 472

7.7.8.6 ECC and DBI – Order of Operations

When transmitting Write data, the Controller can first perform DBI/DMI encoding of the data (if DBI is enabled). DBI encoding will follow the same rules as on LPDDR4. It can then perform ECC generation on the resulting Data and DMI bits (if ECC is enabled). It is important to perform ECC generation after the DBI encoding, because Masked writes can alter the data during DBI encoding. The modified data is used for calculating the data ECC in all cases. The 6-bit DMI ECC and 9-bit data ECC are both transmitted on the RDQS_t pin and sent at the bit-times previously defined. Figure 282 illustrates the data flow.

JEDEC Standard No. 209-5C
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7.7.8.6 ECC and DBI – Order of Operations (cont'd)

When transmitting Read data, the DRAM will either perform DBI encoding (if DBI is enabled), or ECC generation on the data (if ECC is enabled). Which operation is performed will depend on the features enabled. Since Read DBI and Link ECC are mutually exclusive, it never needs to perform both functions, and it never needs to compute or transmit ECC on the DBI bits. The DBI encoding follows the same rules as on LPDDR4. Figure 283 illustrates the data flow.

(JEDEC Standard No. 209-5C, Page 472 and 473)

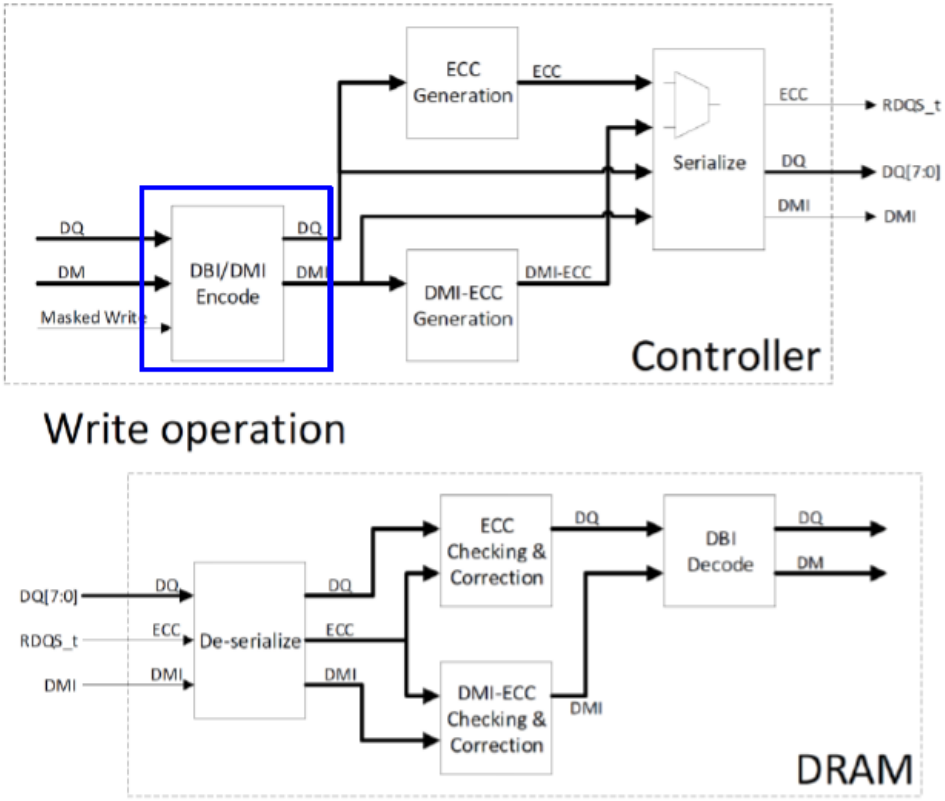

Figure 282 — Data Flow on a Memory Write Operation

JEDEC Standard No. 209-5C
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7.7.8.6 ECC and DBI – Order of Operations

When transmitting Write data, the Controller can first perform DBI/DMI encoding of the data (if DBI is enabled). DBI encoding will follow the same rules as on LPDDR4. It can then perform ECC generation on the resulting Data and DMI bits (if ECC is enabled). It is important to perform ECC generation after the DBI encoding, because Masked writes can alter the data during DBI encoding. The modified data is used for calculating the data ECC in all cases. The 6-bit DMI ECC and 9-bit data ECC are both transmitted on the RDQS_t pin and sent at the bit-times previously defined. Figure 282 illustrates the data flow.

When receiving Write data, the DRAM will first perform checking & correction on the DMI ECC. In parallel, it will perform ECC checking and correction on the data itself. Once the DMI is verified, it will proceed to perform DBI decoding of the data. DBI decoding follows the same rules as on LPDDR4. The Data ECC can be checked prior to DBI decoding due to the unique characteristics of the ECC code (the nature of the code is such that inverting an entire beat of the data would not change the ECC). The Write operation diagram illustrates this data flow.

(JEDEC Standard No. 209-5C, Page 472)

92. In the ’344 Accused Products, “the error coding data block for the first data block is selectively created by the first or second error coding paths as a function of the control indicator and a second control indicator”:

JEDEC Standard No. 209-5C
Page 472

7.7.8.6 ECC and DBI – Order of Operations

When transmitting Write data, the Controller can first perform DBI/DMI encoding of the data (if DBI is enabled). DBI encoding will follow the same rules as on LPDDR4. It can then perform ECC generation on the resulting Data and DMI bits (if ECC is enabled). It is important to perform ECC generation after the DBI encoding, because Masked writes can alter the data during DBI encoding. The modified data is used for calculating the data ECC in all cases. The 6-bit DMI ECC and 9-bit data ECC are both transmitted on the RDQS_t pin and sent at the bit-times previously defined. Figure 282 illustrates the data flow.

When receiving Write data, the DRAM will first perform checking & correction on the DMI ECC. In parallel, it will perform ECC checking and correction on the data itself. Once the DMI is verified, it will proceed to perform DBI decoding of the data. DBI decoding follows the same rules as on LPDDR4. The Data ECC can be checked prior to DBI decoding due to the unique characteristics of the ECC code (the nature of the code is such that inverting an entire beat of the data would not change the ECC). The Write operation diagram illustrates this data flow.

(JEDEC Standard No. 209-5C, Page 472)

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

93. In addition and/or in the alternative to its direct infringements, Qualcomm has indirectly infringed and continues to indirectly infringe one or more claims of the ’344 Patent by knowingly and intentionally inducing others, including its subsidiaries, agents, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’344 Accused Products.

94. At a minimum, Qualcomm has knowledge of the ’344 Patent since being served with this Complaint. Qualcomm also had knowledge of the ’344 Patent since receiving letters from Polaris providing details of its infringements prior to the filing of this Complaint. Since receiving notice of its infringements, Qualcomm has actively induced the direct infringements of its

subsidiaries, agents, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’344 Patent. Indeed, Qualcomm has intended to cause, continues to intend to cause, and has taken and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’344 Accused Products; creating and/or maintaining established distribution channels for the ’344 Accused Products into and within the United States; manufacturing the ’344 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’344 Accused Products that promote their features, specifications, and applications; promoting the incorporation of the ’344 Accused Products into end-user products; and providing technical support and/or related services for these products to purchasers in the United States.

Damages

95. On information and belief, despite having knowledge of the ’344 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’344 Patent, Qualcomm has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Qualcomm’s infringing activities relative to the ’344 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

96. Polaris has been damaged as a result of Qualcomm’s infringing conduct described in this Count. Qualcomm is, thus, liable to Polaris in an amount that adequately compensates

Polaris for Qualcomm's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

CONCLUSION

97. Polaris is entitled to recover from Qualcomm the damages sustained by Polaris as a result of Qualcomm's wrongful acts and willful infringements in an amount subject to proof at trial, which by law cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

98. Polaris has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and Polaris is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

JURY DEMAND

Polaris hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

Polaris respectfully requests that the Court find in its favor and against Qualcomm, and that the Court grant Polaris the following relief:

(i) Judgment that one or more claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by Defendants;

(ii) Judgment that one or more claims of the Asserted Patents have been willfully infringed, either literally and/or under the doctrine of equivalents, by Defendants;

(iii) Judgment that Defendants account for and pay to Plaintiff all damages and costs incurred by Plaintiff because of Defendants' infringing activities and other conduct

complained of herein, including an accounting for any sales or damages not presented at trial;

(iv) Judgment that Defendants account for and pay to Plaintiff a reasonable, ongoing, post-judgment royalty because of Defendants' infringing activities, including continuing infringing activities and other conduct complained of herein;

(v) Judgment that Plaintiff be granted pre-judgment and post-judgment interest on the damages caused by Defendants' infringing activities and other conduct complained of herein;

(vi) Judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and an award of enhanced damages; and

(vii) Such other and further relief as the Court deems just and equitable.

Dated: November 19, 2024

Respectfully submitted,

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