

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ASUSTEK COMPUTER, INC and
ASUS COMPUTER INTERNATIONAL,
Petitioners

v.

NOKIA TECHNOLOGIES OY,
Patent Owner

Case: IPR2025-01154
U.S. Patent No. 11,805,267

DECLARATION OF DR. IAIN RICHARDSON

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I. Introduction

1. I have been retained on behalf of Nokia Technologies Oy and asked to provide opinions in respect of Inter Partes Review (IPR) proceeding IPR2025-01154 which relates to U.S. Patent No. 11,805,267 (the “267 Patent”).

2. This Declaration summarises the independent opinions I have formed to date based on the material currently available to me. I reserve the right to modify my opinions, if necessary, based on further review and analysis of information I receive after the filing of this Declaration, including in response to any positions taken by Petitioners or their experts that I have not yet been provided with.

3. My findings, as explained below, are based on my study, experience, knowledge, and background in the fields discussed below. I am informed by my education and my extensive experience in the fields of video compression and multimedia coding and communications. I have also relied on my review and analysis of the prior art, information provided to me and information I have independently reviewed.

4. I note that Petitioner’s expert, Dr Havlicek, has adopted the analysis, claim constructions and technical opinions of Dr Immanuel Freedman in the Amazon 2024-00626 and 2024-00627 IPRs, Exhibits 1003 (ASUS-1003 at para 24). I note that the entirety of new or additional technical opinions provided by Dr

Havlicek are contained within paras 34-39 (ASUS-1003), a total of approximately three double-spaced pages.

5. In this Declaration I provide responses to the opinions of both Dr Havlicek (ASUS-1003) and Dr Freedman (Amazon 2024-00626 and 2024-00627 IPR Exhibits Ex-1003).

6. I provided technical opinions and analysis in the Amazon IPRs and I incorporate my declarations in those IPRs in their entirety (Amazon IPR 2024-00626 Ex-2030, Ex-2031 and Amazon IPR 2024-00627 Ex-2030, Ex-2031).

7. I am submitting this declaration in support of the Patent Owner's Preliminary Response in IPR2025-01154. The associated Petition and its supporting expert declaration (ASUS-1003) copy and/or reproduce arguments and expert declarations from two prior proceedings, IPR2024-00626 and IPR2024-00627, where the current expert declaration (ASUS-1003) incorporates the prior proceeding expert declarations (Freedman declarations) as appendices (Appendix B and Appendix C). These appendices may use different exhibit numbers. While I have attempted to cite to the exhibit numbers used in the current proceeding, I may find it necessary to refer to exhibit numbers in the ASUS-1003 expert declaration appendices in my arguments herein.

II. Educational Background and Qualifications

8. Details of my professional qualifications and background are summarized below and are set out in detail in my *Curriculum Vitae*, attached to this declaration.

9. I am Director and co-founder of Vcodex BV.

10. I have over 30 years of experience related to video and image compression and coding. I am qualified by education and experience to testify as an expert with respect to subject matter in the fields of video, image, multimedia and general-purpose data encoding, decoding, compression, decompression, and transmission.

11. I received a Master of Engineering (M.Eng.) degree in Electronic and Electrical Engineering from Heriot-Watt University in Edinburgh, Scotland in 1990. I received a Doctor of Philosophy (Ph.D.) degree in Video Compression from Robert Gordon University in Aberdeen, Scotland in 1999. I worked as a Digital Signal Processing (“DSP”) Hardware Designer with GEC Avionics Ltd. from 1990 to 1993.

12. In 1993, I assumed a post as a Lecturer, then Reader and eventually a Full Professor in the field of image and video compression in the School of Engineering at Robert Gordon University. In 2009, I was awarded the position of Honorary Professor with Robert Gordon University.

13. At Robert Gordon University, I founded and ran an image communication technology research laboratory. I carried out original research in the field of data, image, and video compression, initiated and managed research projects, and supervised research students.

14. I am the author of five books and over 70 journal and conference papers on video and image coding and communication, including two widely cited books on the H.264 / MPEG-4 industry standards for video compression. In my 2002 book, *Video Codec Design*, I discussed in detail the efficient implementation of image and video compression on software and hardware platforms.

15. In 1995, during my employment at Robert Gordon University, I cofounded and became Technical Director, equivalent of Chief Technology Officer, at 4i2i Communications Limited. I held this position until 2000. In my role at 4i2i, I was responsible for and engaged in the design of software and hardware modules for compression and communication systems. The designs included video processing algorithms in software and hardware for implementation on processing devices and the design of compression algorithms such as block-based transforms, run-length coding, and variable-length coding in software and hardware. A modified version of one of my video compression hardware designs was successfully used by NASA to stream video from the International Space Station.

16. In 2007, I founded Vcodex Limited and currently serve as the CEO, through which I provide technical and strategic advice to technology companies particularly relating to video, image, and data compression for streaming.

17. In 2009, I founded Onecodec Limited and served as CEO, leading the company's development of innovative video, image, and multimedia data compression and storage software and systems. Onecodec's technology and business activities were merged with Vcodex Limited in 2015.

18. I have previously prepared expert reports and testified in a number of cases concerning video and image compression, graphics compression, general-purpose data compression, and multimedia streaming.

19. I am a named inventor on 11 patents or patent applications, including U.S. and non-US patents and applications.

20. Because of my background, training, and experience, I am qualified as an expert in the technical areas relevant to the '267 patent.

21. My company, Vcodex BV, is being compensated for my independent analysis as an expert with respect to this inter partes review (IPR) proceeding, but neither my compensation nor Vcodex BV's compensation is contingent in any way on the content of my analysis or the outcome of this proceeding. I have no financial interest in Petitioners (ASUSTek Computer, Inc. and ASUS Computer International)

or Patent Owner (Nokia Technologies Oy) and I have no financial interest in the challenged patent.

III. Materials Reviewed

22. The opinions set forth in this Declaration are based on my professional judgment, education, experience, and knowledge regarding the video coding technologies that are discussed in the '267 Patent. In addition, I have based my opinions on my review of documents, including those listed below:

Exhibit	Description
2012	File History of App. Ser. No. 15/250,124 (“’124 Application”)
2013	File History of App. Ser. No. 15/490,469 (“’469 Application”)
2014	File History of App. Ser. No. 15/876,495 (“’495 Application”)
2015	File History of App. Ser. No. 16/729,974 (“’974 Application”)
2016	Pat. App. Pub. No. US 2009/0257503 to Yan Ye, Peisong Chen, and Marta Karczewicz (“Ye ’503”)
2017	Pat. App. Pub. No. US 2010/0086027 to Rahul Panchal and Marta Karczewicz (“Panchal”)
2018	Pat. App. Pub. No. US 2013/0142262 to Yan Ye and Alexandros Tourapis (“Ye ’262”)
2019	VCEG-AI33 by Yan Ye, Peisong Chen, and Marta Karczewicz
2020	U.S. Pat. No. 9,161,057 to Marta Karczewicz, Peisong Chen, and Yan Ye (“Karczewicz ’057”)
2021	Excerpts from “The H.264 Advanced Video Compression Standard”, Richardson, 2010 (Cover pages, book pages 28-38, 69,

Exhibit	Description
	106, 108, 223-229)
2022	Reserved
2023	Reserved
2024	Reserved
2025	Deposition Transcript of Immanuel Freedman, dated November 26, 2024
2026	Marta Karczewicz 50 Leading Tech Voices, available at https://www.epo.org/en/about-us/50-epc-anniversary/50-leading-tech-voices/marta-karczewicz (last accessed 10/2/2025)
2027	Richardson, The H.264 Advanced Video Compression Standard (page 283)
2028	Marta Karczewicz available at https://www.epo.org/en/news-events/european-inventor-award/meet-the-finalists/marta-karczewicz (last accessed 10/2/2025)
2029	The USPTO's Webpage Describing the European Patent Office (EPO), https://www.uspto.gov/learning-and-resources/pursuing-international-ip-protection/european-patent-office (Last accessed 10/6/2025).
2030	Declaration of Dr. Iain Richardson from IPR 2024-00626
2031	Declaration of Dr. Iain Richardson from IPR 2024-00626

IV. Legal Standards

23. I am not an attorney or a legal expert, and I do not opine on matters of law. All the legal standards, which are listed in this section and which I applied in reaching the conclusions expressed throughout this Declaration, were provided to

me and explained to me by counsel. In preparing this Declaration, I have endeavored to faithfully apply these legal standards. I do not intend to offer opinions on the law. Below, I describe the legal standards that I applied in my analysis of the claims of the '267 Patent.

24. I have been informed by counsel that an issued patent is presumed valid and that the challenger of a patent's validity bears the burden of proving invalidity of the patent.

A. Patent Claims

25. I have been informed by counsel that a patent's claims describe the invention made by the inventors and describe what the patent owner owns and what the owner may prevent others from doing.

26. I have been informed by counsel that claims may describe products, such as machines or chemical compounds, or processes for making or using a product. Claims are usually divided into parts or steps called limitations.

27. I have been informed by counsel that there are two types of claims: independent claims and dependent claims. An independent claim sets forth all the requirements that must be met in order to be covered by that claim. Thus, it is not necessary to look at any other claim to determine what an independent claim covers. A dependent claim does not itself recite all of the requirements of the claim but refers to another claim for some of its requirements. In this way, a dependent claim depends

on another claim. The law considers a dependent claim to incorporate all of the requirements of the claims to which it refers.

28. I have been informed by counsel that that a dependent claim then adds its own additional requirements. To determine what a dependent claim covers, it is necessary to look at both the dependent claim and any other claims to which it refers.

29. I have been informed by counsel that in a case where a dependent claim incorporates the limitations of an independent claim upon which it depends, if a reference fails to disclose any of the limitations of the independent claim, the claims which depend on that independent claim cannot be made invalid by such a reference. As a result, any of the references at issue in this proceeding that fail to disclose all of the limitations of an independent claim necessarily also fail to disclose all of the limitations of claims which depend on that independent claim.

B. Burden of Proof for Invalidity

30. I have been informed by counsel and I understand that the party challenging the validity of an issued U.S. patent in an IPR bears the burden of proving invalidity through facts supported by a preponderance of the evidence.

31. I have been informed that a “preponderance of the evidence” means evidence sufficient to prove that a fact is more likely true than it is not.

C. Claim Construction

32. I have been informed by counsel and I understand that the first step in determining validity is to properly construe the claims. I have further been informed by counsel that, in this proceeding, the Board must determine the scope of the claims by using the same claim construction standard that United States District Courts use. Under this standard, the words of a claim are given their “ordinary” and “customary” meaning as would have been understood by a person of ordinary skill in the art at the time of the invention. I have been informed that such a person looks to the claims, specification, and file history in understanding the meaning of the claim terms. I have applied this understanding in this declaration.

D. Person of Ordinary Skill in the Art

33. I have been informed by counsel and I understand that a person having ordinary skill in the art may be defined by factors such as, when considered at the time of the alleged invention: (a) the levels of education and experience of the inventor and other persons actively involved in the field; (b) the types of problems encountered in the field; (c) prior art solutions to those problems; (d) rapidity with which innovations are made; and (e) the sophistication of the technology.

E. Anticipation

34. I have been informed by counsel and I understand that a patent claim can be found invalid as anticipated if each and every element of the claim, as

properly construed, is found either explicitly or inherently in a single prior art reference. If the single prior art reference does not disclose explicitly or inherently any one claim limitation, then that claim is not anticipated. I have further been informed that the single prior art reference cannot merely disclose each element; rather, it must disclose all of the elements as arranged in the claim. I have been informed that for a prior art reference to “inherently” disclose something, the reference must necessarily function in accordance with, or include the claimed limitations, to anticipate. The missing descriptive matter cannot merely probably or possibly include the claimed limitations. I have further been informed by counsel that, with respect to an anticipation analysis, it is improper to combine separate, distinct embodiments of a single prior art reference.

35. I have been informed that for a reference to be anticipatory, the reference must contain an enabling disclosure. I have been informed that merely naming or describing the subject matter is insufficient if it cannot be produced without undue experimentation.

F. Obviousness

36. I have been informed by counsel that a patent claim can be found invalid as obvious if the differences between the claim and the prior art references would have been obvious to a person of ordinary skill in the art at the time of the invention, taking into account (1) the scope and content of the prior art, (2) the

differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any objective indicia of non-obviousness. I have further been informed by counsel that a claim can be found to be obvious in light of either a single prior art reference or multiple prior art references. I have been informed that references qualify as prior art for an obviousness determination only when they are analogous to the claimed invention. Two separate tests define the scope of analogous prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed; and (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved.

37. I have been informed that to be obvious in light of a single prior art reference or multiple prior art references, there must be a reason either to modify the single prior art reference or to combine the two or more prior art references to achieve the claimed invention. I have been informed by counsel that this reason may come from a teaching, suggestion, or motivation to combine which may come from the reference or references themselves, the knowledge or "common sense" of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole.

38. I have been informed by counsel that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.

39. I have further been informed by counsel that there is no suggestion to combine, however, if a reference teaches away from its combination with another source. A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant, or if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. If, when combined, the references would produce a seemingly inoperative device, then they teach away from their combination. I have been informed that it is improper to combine references where the references teach away from their combination.

40. I have been informed by counsel that the degree of teaching away will depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. I have been informed that a reference teaches away, for example, if (1) the combination would produce a

seemingly inoperative device, or (2) the references leave the impression that the product would not have the property sought by the applicant.

41. I have been informed by counsel that if the teachings of a prior art reference would lead one skilled in the art to make a modification that would render another prior art device inoperable, then such a modification would generally not be obvious. I have been informed that if a proposed modification would render the prior art device unsatisfactory for its intended purpose, then the proposed modification would generally not be obvious.

42. I have been informed by counsel that it is improper to use hindsight in making the obviousness determination.

43. I have been informed by counsel that some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness must be made. I have been informed that, for example, there may be no rational underpinning to support the legal conclusion of obviousness where systems are already complete and the party challenging validity seeks to mix and match components, which each exist in the separate systems, from these complete systems.

V. Person of Ordinary Skill in the Art

44. Based on my review of the '267 Patent, the types of problems encountered in the art at and prior to the time of the alleged invention, prior solutions to those problems, the pace with which innovations were made during the relevant

time period, the sophistication of the technology, and the educational level of active professionals in the field, I believe that a person of ordinary skill in the art, at the time of the invention, would have had at least a Bachelor's degree in electrical engineering, computer science, or computer engineering; familiarity with the relevant video coding standards as of this time; and at least two years of work experience in research, design, development, and/or testing of video coding hardware and/or software. More education could have substituted for less work experience and vice versa.

45. All my opinions in this Declaration are from the perspective of a person of ordinary skill in the art, as I have defined it above and during the relevant time frame (e.g., 2011). During that time frame, I possessed at least the qualifications of a POSITA, as defined above. I also note that Dr. Freedman is familiar with my work in video coding and described my 2010 book¹ as being heavily cited. ASUS-1030 at 108:19-110:1.

VI. Background of the Relevant Technology

A. Overview of Video Coding

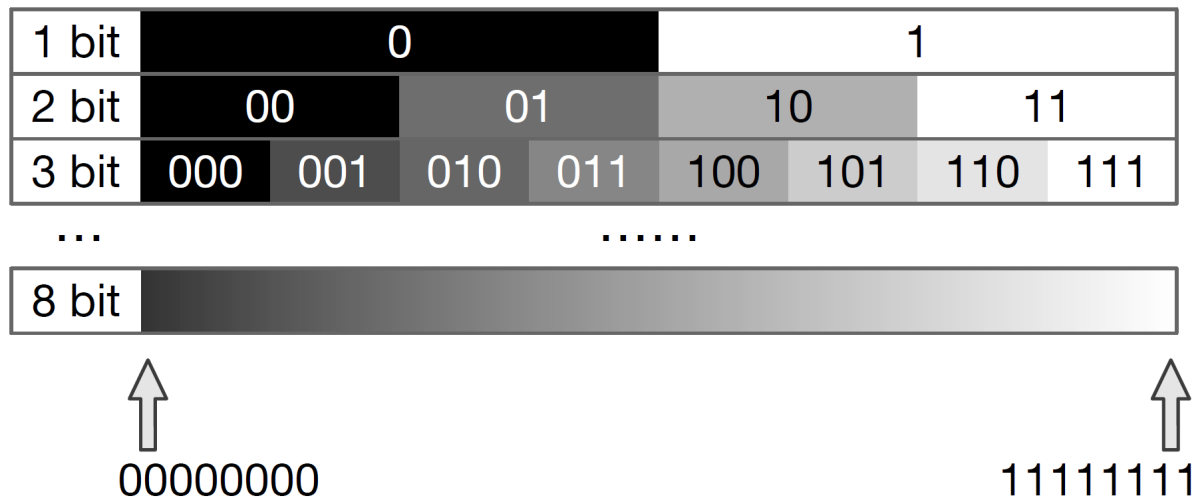
46. Digital video represents video content by sequentially displaying a series of images ("frames") each composed of individual picture elements ("pixels")

¹ I refer here to Ex-2021, which contains excerpts from my 2010 book, "The H.264 Advanced Video Compression Standard."

to produce the illusion of motion.² Various metrics are used to describe the quality of video, one of which is its resolution, which refers to the number of pixels making up each frame. Modern digital video commonly has a resolution of 1280x720 (“720p”), 1920x1080 (“1080p” or “Full HD”) or “4K” which is a term used for the resolutions 4096x2160 and 3840x2160.

47. Each pixel in a frame has a color, which can be represented in terms of its red, green, and blue values (“RGB”) or, equivalently, by its luminance, blue chrominance, and red chrominance (“YCbCr”). Each of these components can be expressed as a collection of bits. For example, 8-bit color uses 8 bits for each of the Y, Cb, and Cr components. In this context, a variable such as a single luminance (Y) sample represented using n bits can have 2^n possible values. 8-bit color allows for 256 possible values for each component, while 10-bit color allows for 1024 possible values for each component. I created the following diagram to illustrate how different bit depths correspond to more possible values. In these examples, a brightness (luma) value represented with one bit can have two possible values, represented as 0 or 1. A value represented with three bits can have 8 possible values, in this example from 000 (black) to 111 (white). A value represented with 8 bits can have 256 possible values and so on.

² For example, modern digital video commonly uses 30 frames per second.



48. Storing and transmitting three colour component values for each pixel in each frame of a digital video would require significant storage capacity and would require extremely fast internet connections in order to be streamed to consumers. As a result, various techniques have been developed for compressing digital video by encoding it to minimize the size of the video for storage and transmission and then decoding it when the video is viewed.

49. Certain common architectures for video coding systems have been established over the years. For example, my 2010 book, “The H.264 Advanced Video Compression Standard,” depicts a block diagram of a video encoder and decoder.

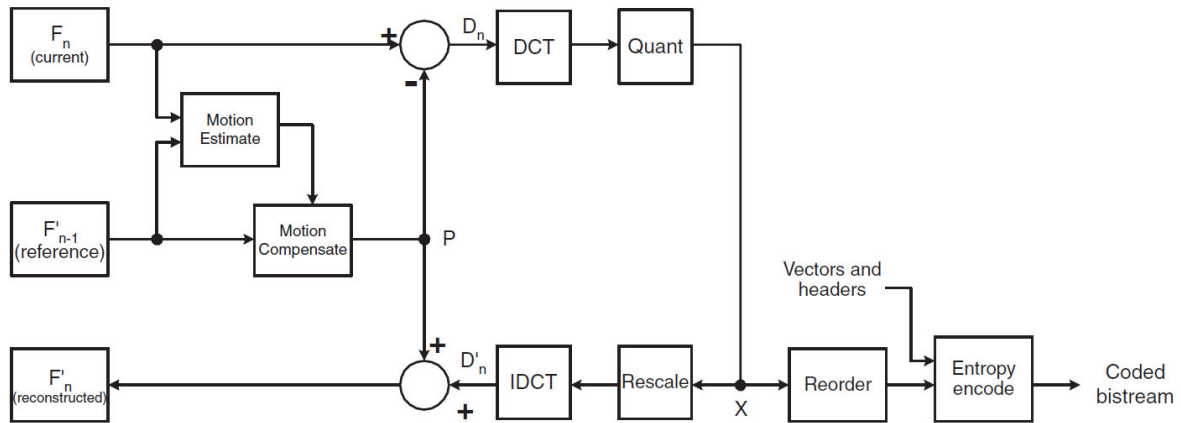


Figure 3.51 DPCM/DCT video encoder

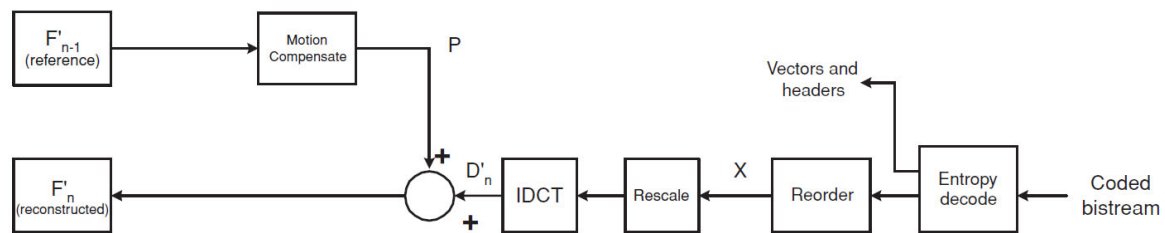


Figure 3.52 DPCM/DCT video decoder

Ex-2021 at page 69.

50. Encoders and decoders work largely symmetrically, with video encoders taking input video frames, F_n , and processing these frames in units of a block of pixels. For each block, the encoder chooses a prediction, P , which preferably closely matches the block being processed. The prediction, P , is subtracted from the block being processed to obtain a residual or difference macroblock D . The residual data is then transformed using a transform such as a Discrete Cosine Transform (the “DCT” block in the figures above) and quantized to eliminate DCT coefficients which contribute negligibly to the residual. Once

quantized, the coefficients are reordered and entropy coded to minimize the amount of data written to the output bitstream. Decoders follow a similar process, but in reverse. A coded bitstream is decoded and used to produce a residual block by application of an inverse transform such as an inverse DCT. A prediction, P, is determined using the same method followed by the encoder and combined with the residual to produce a reconstructed block of the current frame.

51. Although various modes of prediction exist in video coding systems, motion compensated prediction is of particular relevance to the '267 Patent. Motion compensated prediction exploits temporal redundancy in video. For example, in a scene in which the camera pans across a cityscape, each frame will be largely similar to the last but shifted in the direction that the camera is moving. Motion compensated prediction allows portions of a current frame to be predicted from reference frames (e.g., a previous frame) so that the encoded residual only accounts for the difference between the current frame and reference frame.

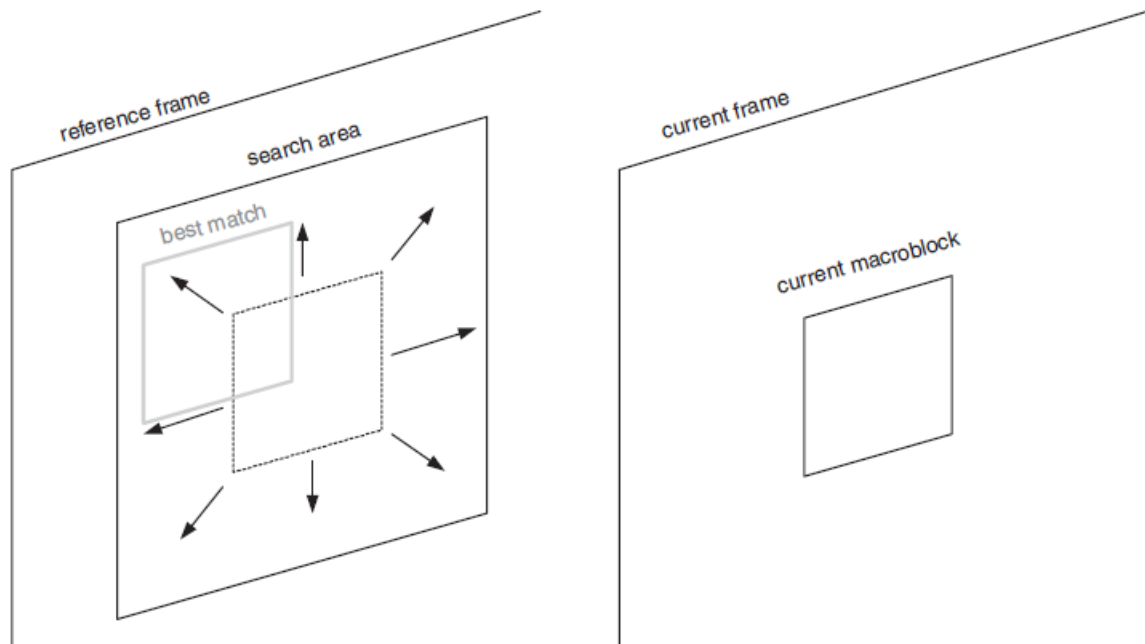
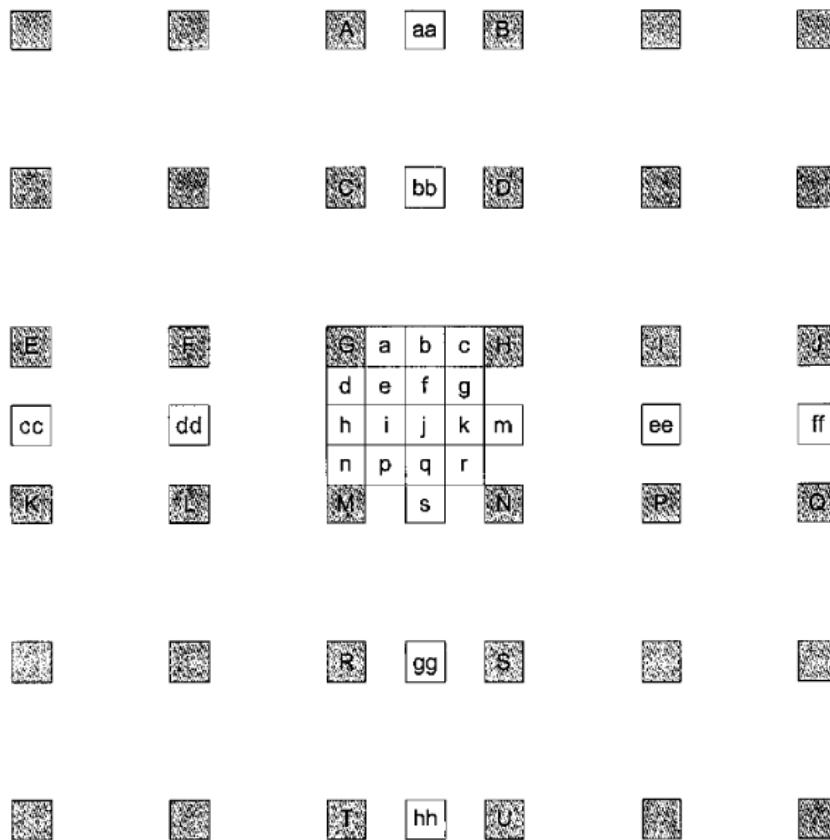


Figure 3.9 Motion estimation

Ex-2021 at page 32.

52. During encoding, motion estimation is used to determine, for a block in the current frame, the best matching block or region of a reference frame. A motion vector represents the displacement between the current block and the matching block or reference block determined during estimation. This motion vector may be encoded in the bitstream or may itself be determined by a motion vector prediction process. During decoding, the process is reversed as described above.



53. In some video codecs, a motion vector may point to a fractional-pixel position in the reference picture, where the fractional-pixel locations refer to locations in between original image pixels. This can enable the encoder and decoder to construct a prediction that is a better match than a prediction that is entirely formed using the actual pixels of the reference picture. The motion-compensated prediction process may involve applying interpolation filter(s)³ to the image pixels in a

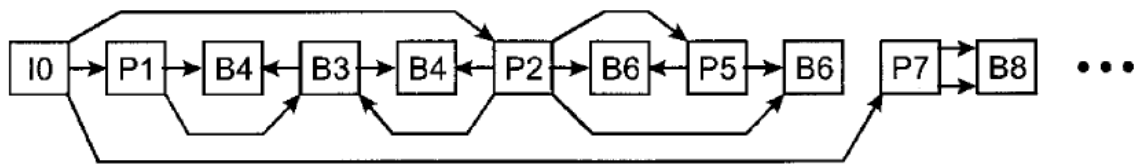
³ For example, a Finite Impulse Response (FIR) filter such as such as a 6-tap Wiener filter with coefficients corresponding to the weighted contribution of each input integer pixel might be used. Other widths of P-tap filter are also common.

reference picture or frame, to generate interpolated fractional-pixel values. *See* ASUS-1001 at 2:60-3:11. Figure 12 of the ‘267 Patent, reproduced above, illustrates examples of image pixel positions (also known as “integer” pixel positions), such as G, H, M and N, and examples of fractional pixel positions such as a, b and c. In the example of Figure 12, fractional pixel positions at $\frac{1}{2}$ and $\frac{1}{4}$ -pixel resolution may be generated. For example, position b is a $\frac{1}{2}$ -pixel position between G and H. Positions a and c are $\frac{1}{4}$ -pixel and $\frac{3}{4}$ -pixel positions respectively between G and H. *See* ASUS-1001 at 2:60-3:11, Fig. 12.

54. When a sub-pixel motion vector is chosen, generating the prediction block requires interpolation of pixel values in the reference picture to create interpolated values. Interpolation may require a computationally complex series of operations such as multiplications, additions and divisions to arrive at a final interpolated value that can be used as a prediction. ASUS-1001 at 3:7-11. Generating potential prediction values for sub-pixel positions is therefore typically computationally expensive.

55. For each current block, an encoder typically selects one matching region in a reference picture, with a corresponding motion vector. However, certain integer-pixel or subpixel values determined using the reference picture may require to be searched for multiple current blocks. For example, potential matching regions that are offset to the right of a first current block may overlap with potential matching

regions that are offset to the left of a second current block, and so on. Thus, an encoder may choose to store interpolated pixel values (i.e., calculated sub-pixel values) for use in motion estimation for multiple current blocks. One strategy that may be computationally efficient and which is used in practical implementations, is for the encoder to calculate all the possible interpolated pixel positions for a reference picture, prior to carrying out motion estimation for blocks of a current picture.



56. The '267 Patent is directed to an improvement in bi-directional motion compensated prediction or bi-prediction, which is a special case of motion compensated prediction that makes use of two reference blocks and two motion vectors to predict a current block. In bi-prediction, predictions are obtained from each reference block and then combined—for example, by simple averaging or weighted averaging of the two predictions. Figure 8 of the '267 Patent, reproduced above, illustrates this process. *See* ASUS-1001 at 2:35-51, Fig. 8. Each block in Figure 8 represents a picture/frame, and those labeled with a “B” are bi-predicted pictures. The arrows indicate the interdependencies between frames. For example, blocks in B4 may be predicted from P1 and B3. A bi-predicted frame can use

references that are in the past, in the future, or both, relative to the current frame. Bi-prediction often allows a lower residual error to be obtained relative to motion compensated prediction from a single reference, which in turn can lead to improved compression performance. *See* ASUS-1001 at 3:25-30.

57. Practical video coding involves a trade-off between decoded image quality, compressed bitrate and computational complexity, as I illustrated in Figure 9.28 of my 2010 book, which I reproduce here:

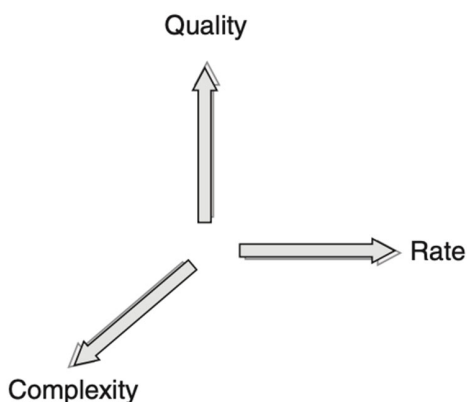


Figure 9.28 Rate, quality and complexity

Ex-2027 at 283.

58. As the ‘267 Patent explains, a typical video encoder seeks to optimize the trade-off between image quality (or conversely distortion, D) and compressed bitrate (or rate, R) during compression. ASUS-1001 at 3:31-48. In other words, a goal of video coding is to provide high compression (i.e., a low bitrate) whilst maintaining good or acceptable image quality (i.e., minimizing distortion). At the

same time, it is important to minimize the computational complexity at both encoder and decoder. For example, many video coding applications such as videoconferencing or video calling, require both encoding and decoding to be carried out in real time on practical devices such as PCs, tablets or cellphones, with limited computational resources. Thus, when designing a practical video codec, an important consideration is to achieve good compression performance (i.e., achieving a low bitrate and a good or acceptable decoded image quality) whilst minimizing computational complexity.

B. Video Coding Standards and Specifications

59. By 2011, a POSITA would have been familiar with video coding standards such as the ITU-T H.263 and H.264 standards discussed in the '267 patent. ASUS-1001, 1:34-37. From the late 1980s, the ITU-T and ISO/IEC international standards organizations have developed and published a series of industry standards relating to video coding. These include the well-known ISO/IEC MPEG and ITU-T H.26x standards. Each standard is/was developed in a similar way. A working group of industry experts is instructed by the standards organization (ITU-T and/or ISO/IEC) to seek to develop a new standard. Over a period of typically a few years, members of the working group contribute technology proposals and develop a draft standard which, if approved, is published by the standards organization.

60. In common with other video coding standards, these standards each specify a format for a compressed bitstream and a method of decoding such a bitstream to produce a decoded video sequence. These standards do not fully specify an encoding process. A video decoder conforming to a video coding standard such as H.263 or H.264 decodes a bitstream that conforms to the specified bitstream format, in order to produce the same output as the specified decoding process. A video encoder encodes a bitstream that conforms to the specified bitstream format and that can be successfully decoded by the specified decoding process.

61. Certain video coding standards have specified methods of bi-directional motion compensated prediction or bi-prediction. These include:

- ISO/IEC MPEG-1 Video and MPEG-2 Video, which each specify methods of bi-prediction of blocks in coded B-pictures, in which a bi-predicted block may be predicted from one past coded I- or P-picture and one future coded I- or P-picture.
- ISO/IEC MPEG-4 Part 2 and ITU-T H.263, which each specify methods of bi-prediction of blocks in coded B-pictures.
- ITU-T H.264 (also published as ISO/IEC MPEG-4 Part 10 and known as Advanced Video Coding or AVC), which specifies more flexible bi-prediction of blocks in coded B-pictures, for example including the ability to predict each block from two coded reference pictures, where

the two coded reference pictures may both be in the past, both in the future or one in the past and one in the future.

62. Certain video coding methods have been developed by technology companies or consortia, including for example Real Video (RV), developed by Real Networks, and Windows Media Video (WMV), initially developed by Microsoft and later published as the VC-1 industry standard.

63. All of the above-mentioned industry standards and proprietary video coding methods share certain common features, including: 1) prediction of image blocks, including the use of motion compensated prediction; 2) transform of residual blocks, e.g., using a Discrete Cosine Transform (DCT) or similar block transform; 3) quantization of transform coefficients; 4) entropy coding of quantized transform coefficients, prediction information (e.g., motion vectors) and other parameters; and 5) complementary encoding and decoding processes.

64. These and other features are illustrated in the following excerpt from my 2010 book (Ex-2021):

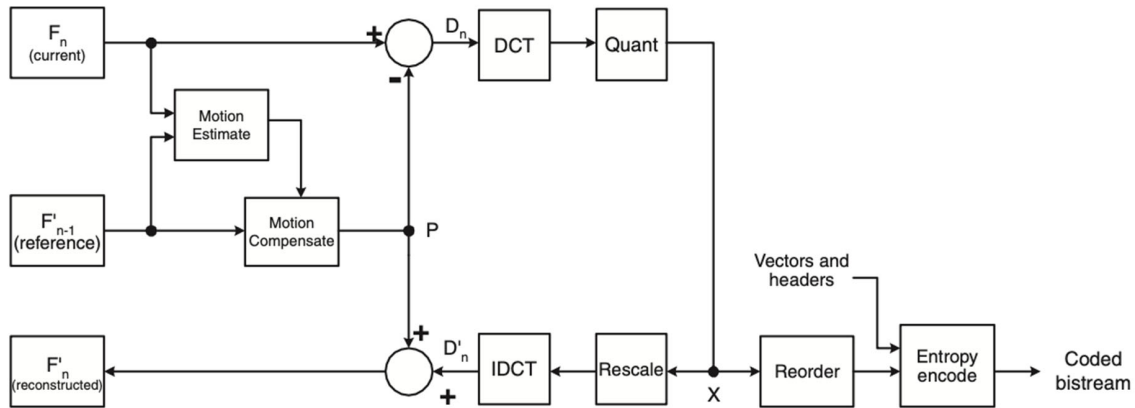


Figure 3.51 DPCM/DCT video encoder

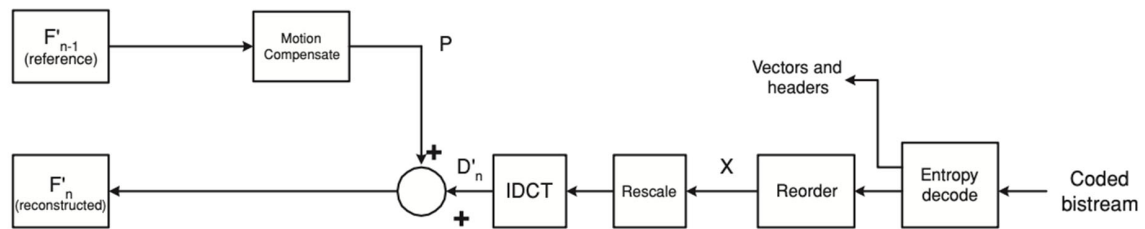


Figure 3.52 DPCM/DCT video decoder

Ex-2021 at 69.

65. As Dr. Freedman recognizes, the block diagrams above illustrate a general architecture for an encoder and decoder using motion compensated prediction which has been around since the 1990s. *See* ASUS-1003 Appendix B at ¶ 3. This general architecture is shared by H.26x-compliant systems, as well as other systems such as Windows Media Video and Real Video. A person of ordinary skill in the art would be accustomed to seeing this general architecture in such video coding systems.

C. The '267 Patent

66. The '267 Patent describes improvements to bi-prediction in video coding which increase the accuracy with which bi-predictions are made, and consequently improve the coding efficiency of a video coding system implementing its inventions. *See* ASUS-1001 at 3:56-65, 4:29-35. In prior art bi-prediction, after the initial predictions contributing to the final prediction were computed, their values were shifted to the precision of the input reference blocks. *See id.* at 13:43-55, Fig. 10. Figure 10 illustrates the prior art process. To form prediction P1, an integer-pixel or sub-pixel prediction value may be calculated at a higher precision (a higher-precision prediction) using a P-tap filter (ASUS-1001 at 12:56-13:8) then a rounding offset is added and the result is bit shifted to the original (input) bit depth to form prediction sample P1. *See* ASUS-1001 at 13:8-18. A similar process is applied to form prediction sample P2.

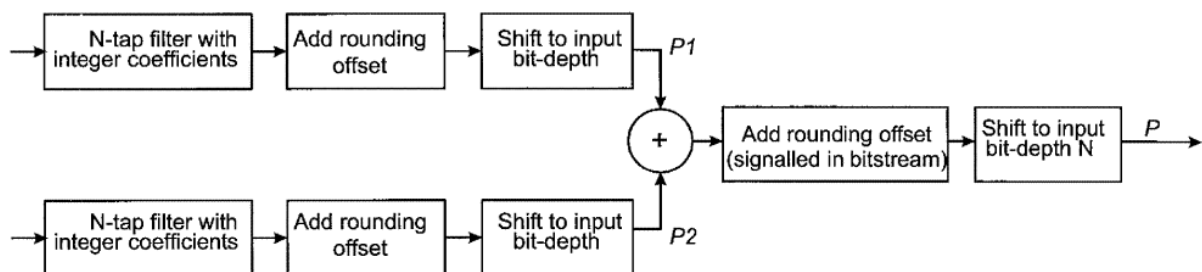


Fig. 10

67. The inventors of the '267 Patent recognized that in such a prior art implementation, the bi-prediction process was susceptible to the accumulation of

rounding errors which could cause degradation in coding efficiency. *Id.* at 3:56-65. Although other competing solutions to this degradation in bi-prediction efficiency existed, such as adjusting the rounding process itself by alternating upward and downward rounding to reduce rounding error on average, or by adjusting the rounding offset(s), as disclosed in Karczewicz-I (ASUS-1005 at ¶¶ 66-69), the inventors of the '267 Patent adopted a technique illustrated in Figure 11. *See id.* at 7:22-24, 13:56-62, Fig. 11. This approach improved the prior art by retaining additional precision resulting from the prediction process until the combination step, lessening the impact of rounding error. *Id.* at 13:43-55.

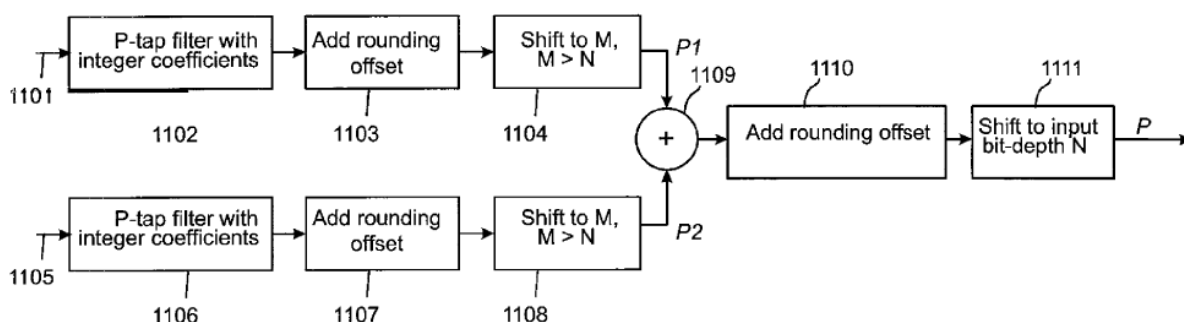


Fig. 11

68. As the '267 Patent explains, when combining two prediction values such as P1 and P2 to form a bidirectional prediction P, in order to predict a current pixel with a certain precision and bit depth, it can be advantageous to calculate P1 and P2 at a higher bit depth and precision than the current pixel. *Id.* at 13:43-55. P1 and P2 are summed at this higher precision and the results are then right-shifted to

create a prediction P that matches the precision of the current pixel. *Id.* at 13:46-48.

The advantage of this approach is that rounding errors are reduced. *Id.* at 4:29-31.

1. Predictions in the '267 Patent

69. In the context of the '267 Patent, a “prediction” for a block of pixels is a value or set of values generated through some coding process that is itself intended to approximately represent the pixel values for that block and that can then be used to form a residual that represents the error between the prediction and its original value. *See* ASUS-1001 at 2:1-51 (“in [motion compensated prediction], a prediction for a current frame is formed using a previously coded frame(s), where only the difference between original and prediction signals . . . is encoded.”). Because the residual value must be quantized and entropy coded, the efficiency of a prediction method is correlated with the extent to which it minimizes the residual value. *See id.* at 3:56-65.

70. For example, an 8-bit pixel value can have any value in the range 0-255. Given a current pixel value of 120 and a prediction of 116, a residual can be obtained by subtracting the prediction from the current pixel value: $120 - 116 = 4$. A 10-bit pixel value can range from 0-1023. Given a current pixel value of 480 and a prediction of 483, the residual is $480 - 483 = -3$. In both instances, the aim of the motion compensated prediction process is to minimize the residual value in order to maximize compression.

D. Alleged Prior Art

1. Karczewicz-I and Karczewicz-II

a) Karczewicz-I

71. U.S. Application No. 2011/0007799 (ASUS-1005) (“Karczewicz-I”) was published on January 13, 2011. It describes conventional bi-prediction as implemented in H.264/AVC in default weighted, implicitly weighted and explicitly weighted forms. ASUS-1005 at ¶ 44. Default weighted prediction performs simple averaging of two predictions by applying equal weights, as described by Walker in the trivial H.264 weighting scenario. *See id.* at ¶¶ 44, 60. Implicit weighted prediction and explicit weighted prediction both make use of non-equal weights but differ in how they compute the weights. In implicit weighted prediction, weights are determined based on the temporal distance between reference frames and the current frame. *See id.* at ¶¶ 45, 61. In explicit weighted prediction, the weights that should be applied to each prediction are explicitly coded in the bitstream. *See id.* at ¶¶ 46, 62. Karczewicz-I sets forth equations for each of these three scenarios.

Default	Bidirectional prediction: $\text{pred}(i,j) = (\text{pred0}(i,j) + \text{pred1}(i,j) + 1) \gg 1$
Implicit	Bidirectional prediction: $\text{pred}(i,j) = (\text{pred0}(i,j) * w0 + \text{pred1}(i,j) * w1 + 32) \gg 6$
Explicit	Bidirectional prediction: $\text{pred}(i,j) = (\text{pred0}(i,j) * w0 + \text{pred1}(i,j) * w1 + 2^r) \gg (r+1) + ((o1 + o2 + 1) \gg 1)$

Id. at ¶¶ 60-62, (annotated).

72. Karczewicz-I explains that these bidirectional prediction calculations employ rounding adjustments, generally adding a rounding adjustment of 2^{r-1} prior to a right shift by r binary places and that these frequent rounding operations can reduce the performance of prediction. *Id.* at ¶¶ 63-64. For example, rounding offsets (highlighted) of +1, +32, 2^r and +1 are expressed in the three equations above. Karczewicz-I proposes to mitigate the effect of such a loss of precision due to rounding and to improve the performance of prediction by adjusting the use of rounding offsets.

73. Karczewicz-I's proposed adjustments include: combining multiple offsets, using different offsets for uni- and bi-directional prediction, and adaptively selecting upward, downward or no rounding offsets. *Id.* at ¶¶ 64-68.

74. Thus, Karczewicz-I proposes to improve the performance of bidirectional prediction processes by manipulating the offsets used in the rounding

process. Importantly, Karczewicz-I does not propose any change in the precision of either of the two prediction values used in bidirectional prediction. Karczewicz-I incorporates the disclosure of Karczewicz-II as I explain later.

b) Karczewicz-II

75. U.S. Application No. 2009/0257499 (ASUS-1006) (“Karczewicz-II”) was published on October 15, 2009. Unlike Karczewicz-I, Karczewicz-II is not directed to bi-prediction. Instead, this reference concerns subpixel interpolation. *See, e.g.*, ASUS-1006 at ¶ 7. Because motion vectors used for motion-compensated prediction can point to fractional-pixel values, the effective value of pixels at those fractional locations (i.e. subpixels) are obtained by interpolation, as I explain in the “Overview of Video Coding” background section above. To interpolate subpixel values, video codecs typically use linear filters such as a 6-tap Wiener filter with coefficients corresponding to the weighted contribution of each input integer pixel. *See id.* at ¶ 68. For example, half-pixel values can be interpolated from integer pixels as shown in Figure 4B. *Id.* at ¶ 70.

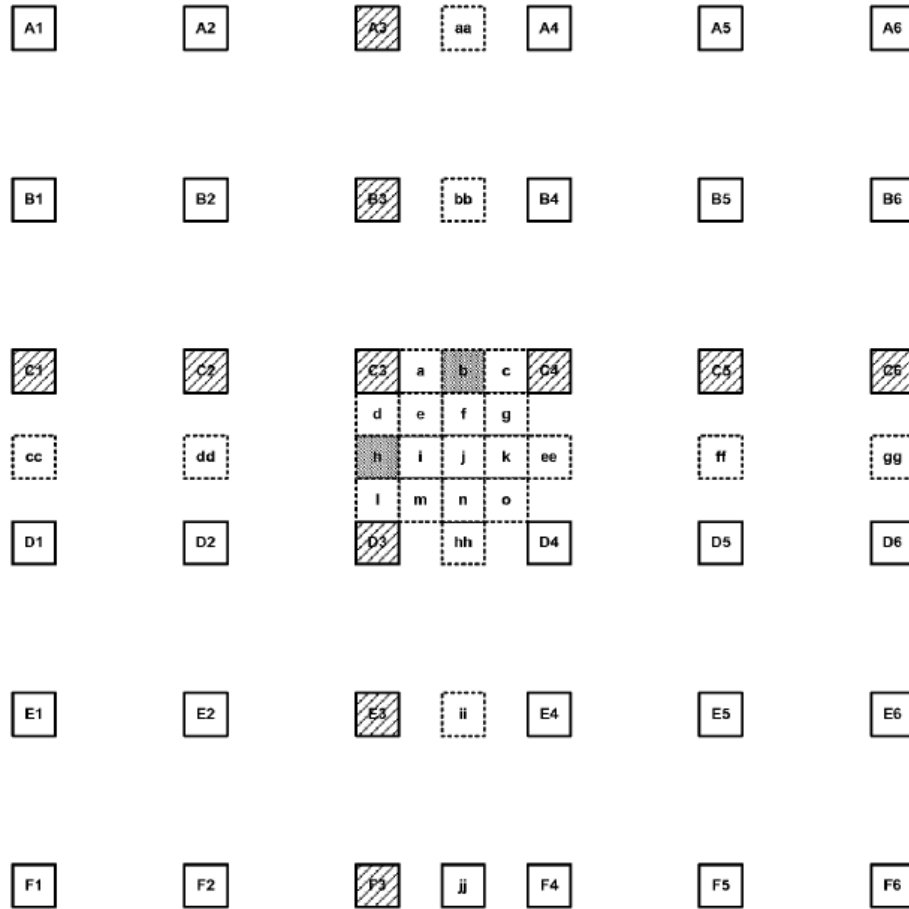


FIG. 4B

76. Using the 6-tap filter weights of [1, -5, 20, 20, -5, 1] described in Karczewicz-II, half-pixels “b” and “h” can be computed from the shaded integer pixels as discussed in paragraph 70:

$$b = C1 - 5 \cdot C2 + 20 \cdot C3 + 20 \cdot C4 - 5 \cdot C5 + C6$$

$$h = A3 - 5 \cdot B3 + 20 \cdot C3 + 20 \cdot D3 - 5 \cdot E3 + F3$$

77. Similarly, quarter-pixel values can be computed from both half-pixel and integer pixel values, as illustrated in Figure 4D. *See id.* at ¶ 72-74. Because of this dependency on half-pixel values as well as integer-pixel values, quarter-pixels cannot be computed until half-pixel values are known.

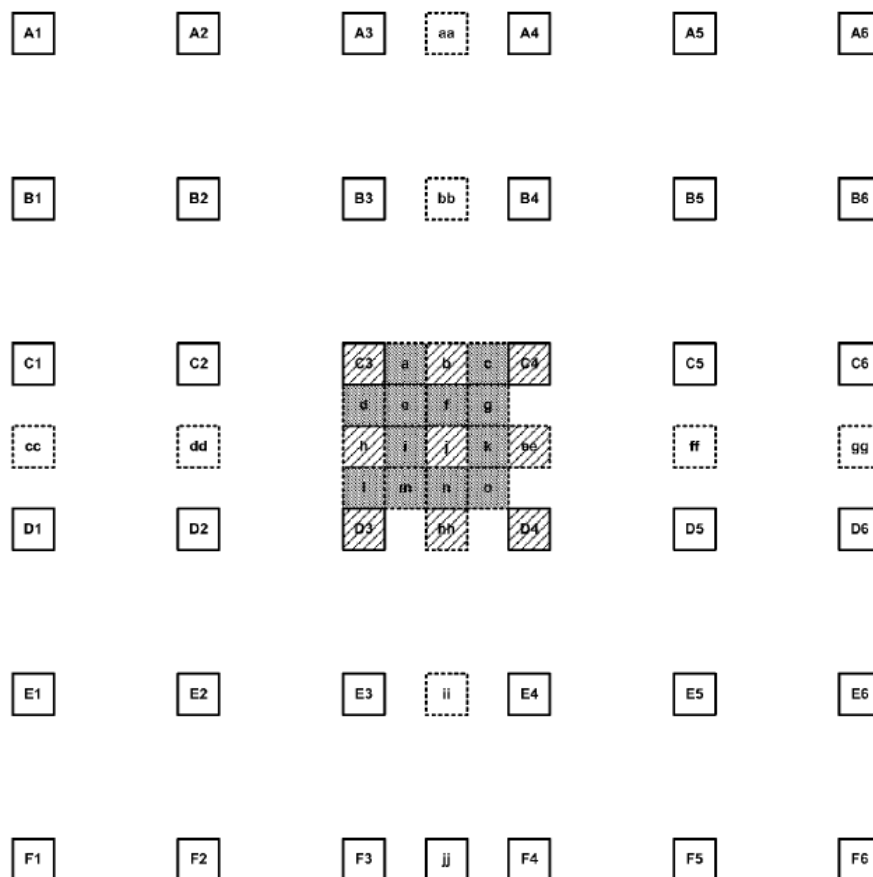


FIG. 4D

78. Karczewicz-II notes that H.264/AVC interpolation is performed with intermediate rounding operations, which round half-pixel values down to the input

precision before they are used to compute quarter-pixel values. *Id.* at ¶ 86. The reference suggests that, instead of rounding half-pixel values prior to quarter-pixel interpolation, the interpolated half-pixel values should be maintained at a high precision (e.g., 16 bits) until quarter-pixel interpolation has concluded, at which point they are rounded to the input precision (e.g., 8 bits). *See id.* at ¶¶ 100-102, 104, Tables 5-7.

VII. A POSITA would not be motivated to combine and modify Karczewicz-I and Karczewicz-II as Petitioner alleges.

79. I understand that Petitioners have asserted, and Dr. Havlicek has opined, that the combination of Karczewicz-I and Karczewicz-II would render obvious the challenged claims of the '267 Patent. I disagree because a POSITA would not be motivated to modify and combine the two references as Dr. Havlicek describes. Further, Petitioner and Dr. Havlicek fail to show that a POSITA would have had a reasonable expectation of success in making such modifications.

A. Petitioner's arguments based on Dr. Havlicek's opinions

80. In addition to agreeing with and adopting Dr. Freedman's analysis (ASUS-1003, Appendices B and C) as his own, Dr. Havlicek advances additional arguments only concerning motivation to combine, which I address below.

B. Petitioner's arguments based on Dr. Havlicek's adoption of Dr. Freedman's opinions

81. The petition seeks not only to combine Karczewicz-I and Karczewicz-II, but to modify them both in the process. The petition fails to show that a POSITA would be motivated to make this modified combination and fails to show that a POSITA would have had a reasonable expectation of success in making it.

82. First, the Petition asserts that Karczewicz-II “teaches improved calculations for averaging interpolated pixel values, where rounding is delayed until later in the process, thereby maintaining higher precision for intermediate calculations” and that those “complimentary teachings” would “improve Karczewicz-I by reducing rounding inaccuracies.” Petition at 10. However, Karczewicz-I already includes the higher-precision interpolation equations the petition relies upon due to its incorporation by reference of VCEG-AI33. ASUS-1005 at ¶ 37, explaining that VCEG-AI33 is “hereby incorporated by reference in its entirety”. As noted above, VCEG-AI33 includes the same teachings Petitioner relies upon in Karczewicz-II, including the same equations for interpolation of quarter-pixel values using intermediate values for half-pixel positions. A POSITA would therefore understand Karczewicz-I to already include the improved interpolation techniques of Karczewicz-II, and would not look to Karczewicz-II for any further combination or modification.

83. Second, Karczewicz-I teaches that its input must be at the same precision as the current block of pixels and Karczewicz-II teaches that its output must be at the same precision as the current block of pixels. As a result, even if a POSITA were motivated to combine Karczewicz-I and Karczewicz-II, they would not combine Karczewicz-I and Karczewicz-II in the manner asserted by the petition, namely storing and using selected higher bit-depth intermediate values of Karczewicz-II as predictions, and using such selected higher bit-depth intermediate values as inputs for bi-prediction in Karczewicz-I.

84. Karczewicz-I refers to the result of its bi-predictions as “prediction data.” ASUS-1005 at ¶¶ 64, 69. Karczewicz-I further teaches that, once suitable prediction data is found, it is subtracted from the original block being coded (the current block) to create a residual block. ASUS-1005 at ¶ 73. In a corresponding step at the decoder, the received residual block is added to the prediction data to reproduce the original data. ASUS-1005 at ¶ 84. At ¶ 73 and ¶ 84, Karczewicz-I discloses what a POSITA would understand to be well-known arithmetic operations of subtraction and addition respectively. Absent any special logic, which Karczewicz-I does not disclose, the current block pixels and the prediction data must have the same precision at the point at which they are added or subtracted. The unweighted bi-prediction equation relied upon by the Petition from Karczewicz-I has inputs of predictions $\text{pred0}(i,j)$ and $\text{pred1}(i,j)$, adds them and right-shifts by 1,

then outputs prediction data $\text{pred}(i,j)$. ASUS-1005 ¶ 60. A POSITA would understand that according to this equation, the predictions $\text{pred0}(i,j)$ and $\text{pred1}(i,j)$ and the combined prediction $\text{pred}(i,j)$ each have the same precision. As combined prediction $\text{pred}(i,j)$ necessarily has the same precision as the current block pixel data (as I explain above) and as $\text{pred0}(i,j)$, $\text{pred1}(i,j)$ and the combined prediction $\text{pred}(i,j)$ necessarily have the same precision as each other, predictions $\text{pred0}(i,j)$ and $\text{pred1}(i,j)$ in Karczewicz-I therefore have the same precision as the pixels of the current block.

85. Similarly, each of the interpolated values for sub-pixel positions in Karczewicz-II have the same precision as the original input pixels. The 6-tap filter used in Karczewicz-II has weights $[1, -5, 20, 20, -5, 1]$ which add to 32. ASUS-1006 ¶ 93. Thus intermediate values such as $b1$ and $h1$ that result from a single application of the 6-tap filter (without a right-shift) gain five bits of bit depth (since $2^5 = 32$), and intermediate values such as $j1$ that result from two applications of the 6-tap filter (without a right-shift) gain 10 bits of bit depth. Thus for input pixels with 8-bit precision, $b1$ or $h1$ have 13 bits of precision and $j1$ has 18 bits of precision. The equations for sub-pixels $a, c, d, l, f, i, k, n, e, g, m$, and o in Tables 3 and 4 of Karczewicz-II each specify the addition of two input values with bit depths which are 5 bits greater than the original pixel bit depth (such as for example $b1 + h1$, corresponding to sub-pixel e), followed by a right-shift of 6 binary places, which

would return a result with the original pixel precision. ASUS-1006 ¶¶ 99-100. The specific examples provided by Karczewicz-II, demonstrating how to implement these interpolation equations using 16-bit arithmetic, all specify 8-bit precision for input pixels such as x and for prediction outputs such as a, c, d, l and so on. ASUS-1006 ¶¶ 103-105. Thus Karczewicz-II teaches using 8-bit input pixel values to generate 8-bit predictions whilst using higher precision for certain intermediate calculation values.

86. In summary, Karczewicz-II teaches generating as its output 8-bit prediction values corresponding to fractional motion vector positions by interpolation of 8-bit pixel values, and Karczewicz-I teaches combining such 8-bit prediction values (as inputs) to generate an 8-bit combined prediction value. Were a POSITA to combine Karczewicz-II and Karczewicz-I (without modifying both references) the result would therefore be a combined process that at no point required or generated a prediction value with a precision higher than that of the input pixel values (8 bit precision in the specific examples of the two references).

87. Further, Petitioner suggests modifying both references in a manner not disclosed in either reference, namely storing and using selected higher bit-depth intermediate values of Karczewicz-II as predictions, and using such selected higher bit-depth intermediate values as inputs for bi-prediction in Karczewicz-I.

88. As I explain above, Karczewicz-I discloses an equation for calculating a bi-prediction $\text{pred}(i,j)$ from two input predictions $\text{pred0}(i,j)$ and $\text{pred1}(i,j)$, with all three predictions having a precision of 8 bits (Petition at p42, ASUS Ex 1005 at 60). Petitioner proposes replacing $\text{pred0}(i,j)$ in this process with ‘non-rounded ($\text{pred0}(i,j)$)’, a version of $\text{pred0}(i,j)$ that was calculated and stored at a higher precision such as 15 bits (Petition at 20). Petitioner suggests that the resulting combined equation for $\text{pred}(i,j)$ (Petition at 20) results from a combination of Karczewicz-II and Karczewicz-I. However, neither Petitioner’s newly-created prediction (‘nonrounded ($\text{pred0}(i,j)$)’) nor the combined equation (Petition at 20) are actually disclosed in Karczewicz-II. What is disclosed in Karczewicz-II is an intermediate value such as $b1$, calculated during averaging of a half-pixel and an integer-pixel value, which Petitioner arbitrarily chooses as an output of Karczewicz-II and an input of the bi-prediction equation of Karczewicz-I (Petition at 20-23).

89. To provide a basis for this modification, Petitioner points to paragraph 99 of Karczewicz-II in support of Petitioner’s proposition that Karczewicz-II “teaches improved calculations for averaging interpolated pixel values, where rounding is delayed until later in the process, thereby maintaining higher precision for intermediate calculations.” Petition at 10. However, the process addressed by Paragraph 99 of Karczewicz-II is the process of interpolating final 8-bit values to be used as predictions in motion compensated prediction. Thus the process addressed

by Karczewicz-II at Paragraph 99 does not disclose or suggest calculating or storing actual prediction values at a higher precision or bit-depth. Instead, such prediction values (the “very last step of the interpolation process” referred to in Karczewicz-II at Paragraph 99) are indeed subject to “shifting, rounding and clipping” in order to revert to the 8-bit precision Karczewicz-II requires for prediction values.

90. Petitioner never addresses, much less provides a motivation to incur, the significant computational, memory and memory bandwidth cost of calculating and storing predictions at a higher precision, necessarily required by its Karczewicz-I/Karczewicz-II combination. The advance of Karczewicz-II was the use of a limited number of 16-bit registers during the calculation of the 8-bit final prediction values for each sub-pixel position within a prediction block, using higher-precision intermediate values. ASUS-1006 ¶¶ 53, 59. In my opinion, a POSITA would not be motivated to change the whole focus of Karczewicz-II in order to reduce rounding errors in bi-prediction, especially considering that Karczewicz-I already provides a solution to rounding errors in the form of rounding offsets. ASUS-1005 ¶¶ 64-69. In other words, there is no need to modify Karczewicz-I to address the issue of rounding in bi-prediction, whereas such a modification would have significant potential technical disadvantages in terms of increased computation, memory and memory bandwidth, and so a POSITA would not be motivated to make the change contemplated by the Petitioner. Neither Petitioner or Dr Havlicek provide any

evidence that the proposed combination of Karczewicz-I and Karczewicz-II would provide a better solution to rounding errors than the solution already disclosed in Karczewicz-I, namely the use of rounding offsets.

91. Further to my discussion above, a POSITA would understand that the modifications proposed by Petitioner would have considerable technical costs and disadvantages in terms of computation, memory and memory bandwidth, and so would not be motivated to make them, without some external justification. For example, as I explained earlier, a video encoder typically generates and stores calculated prediction values for each of the 15 sub-pixel positions that surround each integer-pixel value (K-II, Fig. 4D), in order to search for a best matching region and thus an optimal motion vector, during the process of motion estimation. In the methods of Karczewicz-I and Karczewicz-II, such prediction values are generated and stored at the same precision as the integer pixel inputs, i.e. 8 bits per prediction value.

92. Video coding is performed on a block basis, where values for each position in a 4x4 or 8x8 block are calculated at the same time, in parallel, for a total of 16 or 64 8-bit values. Memory operates using “words” of a fixed, standardized size, so that each memory address refers to a fixed number of bits that written to or read from in a memory access to that address. At the time of the invention, consumer-level devices typically used 32-bit or 64-bit words, and a POSITA would be familiar

with the use of 32-bit words in designing a video codec for maximum compatibility and minimum implementation cost.

93. A 32-bit word allows for the storage of four of the 8-bit prediction values used by both Karczewicz-I and Karczewicz-II. Using such 8-bit values allows values stored and retrieved using 32-bit words to be byte-aligned within the memory word without waste. This would allow all of the values of a 4x4 block to be stored or retrieved using four 32-bit words of memory, and all of the values of an 8x8 block to be stored or retrieved using sixteen 32-bit words of memory, for example.

94. The approach suggested by Petitioner and Dr. Freedman would break this feature of Karczewicz-I and Karczewicz-II, as different predictions would require different numbers of bits. Assuming an 8-bit input value, the three scenarios identified in the petition and Dr. Freedman's declarations would require some prediction values to be stored at 8 bits, some to be stored at 13 bits, and some to be stored at 18 bits. I have illustrated this below, with color coding to indicate the number of bits required to store each prediction value (green is 8 bits, yellow is 13 bits, and blue is 18 bits):

Scenario	Equation
1	$\text{pred}(i,j) = (\text{non-rounded}(\text{pred0}(i,j)) + \text{pred1}(i,j) \ll 5 + 32) \gg 6$
2	$\text{pred}(i,j) = (\text{non-rounded}(\text{pred0}(i,j)) \gg 5 + \text{non-rounded}(\text{pred1}(i,j)) + 32) \gg 6$
3	$\text{pred}(i,j) = (\text{non-rounded}(\text{pred0}(i,j)) + \text{non-rounded}(\text{pred1}(i,j)) + 32) \gg 6$

95. Implementing the modifications contemplated by the petition and Dr. Freedman would therefore require the encoder to store and retrieve predictions of at least three different bit widths. Doing so using conventional memory architectures would be complex and wasteful. For example, only two 13-bit predictions could be stored using a single 32 bit word, resulting in a waste of 6 bits per 32-bit word. In this example, twice as many memory accesses would be required to store or retrieve the same number of prediction values, compared to 8-bit predictions. Only a single 18-bit prediction could be stored using a single 32-bit word, resulting in a waste of 14 bits per word. Four times as many memory accesses would be required to store or retrieve the same number of 18-bit prediction values, compared to 8-bit prediction values. This would make each search location checked significantly more expensive, which would either lead to a significant increase in computation or a decision to perform fewer motion estimation searches per block. Performing fewer motion estimation searches would result in a reduction in inter prediction performance. Thus Petitioner's proposed combination would result in either a significant increase in computational complexity or a significant reduction in compression performance.

96. Using non-standard memory sizes would not ameliorate the problem. If, for example, Petitioner's modification of Karczewicz-I and Karczewicz-II were performed using custom 18 bit words, for example, 13-bit prediction values would waste 5 bits and 8-bit prediction values would waste either 10 bits or 2 bits per word,

depending on whether one or two 8-bit prediction values were stored in each 18-bit word. The number of memory accesses per block would also be doubled for both 8-bit and 13-bit prediction values.

97. Beyond the increase in memory storage and access requirements, extensive changes in the hardware design of the video codec would be required. For example, if predictions were stored at different precisions as proposed by Petitioner, then the logic used to carry out motion compensated prediction with a single reference would also need to be changed to accommodate the variability in potential prediction values from interpolation. Additionally, the execution pipeline for the codec would need to be modified for the different number of memory accesses required for the different prediction sizes, and the codec would either lose capacity or need to perform other tasks as its execution unit waited for prediction values to be fetched in order to be evaluated as part of the search process. A POSITA would understand that the proposed modifications would require calculations such as subtracting the prediction from the residual or combining predictions to use higher-precision arithmetic, thus incurring a computational cost. A POSITA would not be motivated to incur such processing and memory penalties outlined above in order to avoid rounding errors, absent a strong external motivation which the Petition does not provide. Further, as I explained earlier, Karczewicz-I already presents a solution for rounding errors in bi-prediction using various offsets, so that a POSITA would

use Karczewicz-I's actual solution to address the problem of rounding errors, rather than any modification of the Karczewicz-I reference.

98. Further, a POSITA would not be motivated to make the above contemplated changes to a decoder unless he or she was first motivated to make the corresponding changes at the encoder. As I explained above, an encoder's predictions are used to generate the residual data at the encoder that the decoder receives, together with information such as motion vectors indicating how the decoder should make its own corresponding prediction. The decoder then generates the prediction block and adds it to the residual information to reconstruct the block. If the encoder and decoder were to use different processes to generate their predictions, such as a higher-precision "non-rounded prediction" at the decoder but a lower-precision prediction at the encoder, then the values added to the residual data by the decoder would not match the values subtracted at the encoder. This will introduce a distortion not only in the current picture, but also in subsequent pictures that refer back to the current picture or to pictures predicted from the current picture, resulting in both an unacceptable reduction in decoded image quality and an unacceptable loss of compression performance due to the mismatched predictions. A POSITA would therefore not be motivated to increase or change the precision of predictions only at the decoder, due to the necessity for both encoder and decoder to create identical predictions.

99. Further, as I explained earlier, Karczewicz-I already includes the higher-precision interpolation equations of Karczewicz-II. Further, Karczewicz-I has lower bit depth values as inputs and a POSITA would have no motivation to replace with high bit depth from Karczewicz-II. Petitioner arbitrarily chooses an intermediate value from Karczewicz-II, as an input to Karczewicz-I bi-prediction, without justification except for using roadmap of the '267 Patent. As Karczewicz-I already discloses a solution to the problem of rounding errors, namely the use of rounding offsets, a POSITA would see no need for the extra technical costs of attempting a combination with Karczewicz-II, with no guarantee that the Karczewicz-II method would improve upon the existing solution of Karczewicz-I.

100. Dr. Havlicek suggests that the additional complexity required by the proposed combination are generic costs already needed in H.264 or Karczewicz-I (Ex 1003 at para. 37) and appears to imply that adding complexity even without evidence of technical improvements, is a normal decision in video codec design. This is incorrect. A fundamental goal in video coding is to minimize computation and computational complexity whilst maintaining acceptable compression performance. Complexity, whether in the form of additional computation, additional storage requirements or both, makes it more difficult to encode or decode video in real time. An increase in complexity in a video codec can only be justified by significant improvements in compression efficiency. As I explained above, the

increase in complexity required by Petitioner's proposed modification of the Karczewicz-I and Karczewicz-II references would require extensive changes and increases in memory and computation requirements, without any evidence of an improvement in compression performance. Since Karczewicz-I already offers a solution for correcting for rounding error in bi-prediction, which a POSITA would expect to deliver an improvement in compression performance, a POSITA would not be motivated to depart from Karczewicz-I's teachings in the manner suggested by the Petition.

101. Dr. Freedman's proposed motivation to combine and modify these references is fundamentally flawed. Nothing in Karczewicz-I or Karczewicz-II (or any other cited art) supports the idea of combining the two. Dr. Freedman's first argument for motivation to combine is that the Karczewicz references are both directed to video coding and recite "similar architectures." *See* ASUS-1003, Appendix B at ¶ 136. Dr. Freedman presents side-by-side figures from the two references, which I reproduce below:

Karczewicz-I

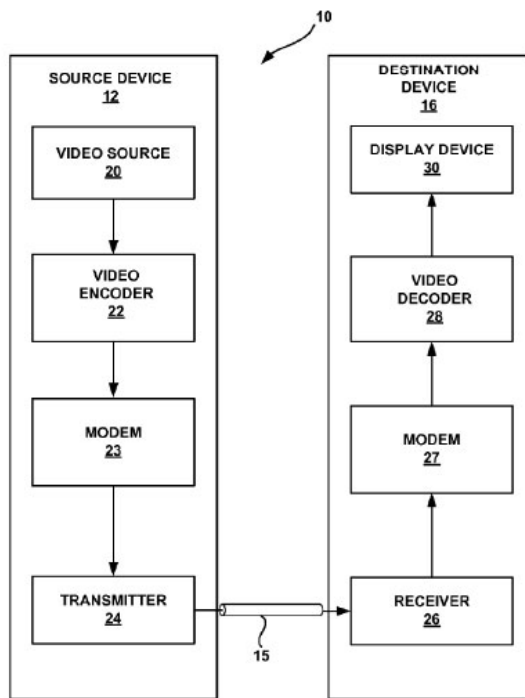


FIG. 1

Ex-1005, Fig. 1, ¶¶29-50.

Karczewicz-II

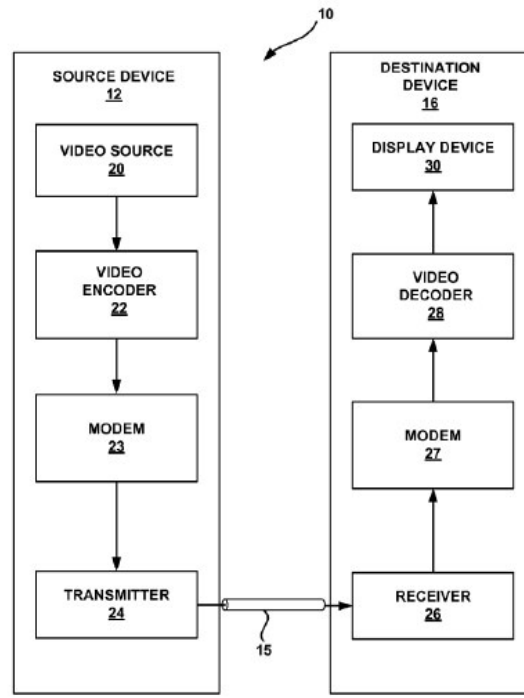


FIG. 1

Ex-1006, Fig. 1, ¶¶40-53.

102. The above figures represent the most abstracted view of a video transmission system that seems possible to me—one that applies to any video coding system which makes use of some means of telecommunication to transmit video between a “source” and “destination” device. Similarly, Dr. Freedman presents figures from both references depicting the same block diagram of a video coding system.

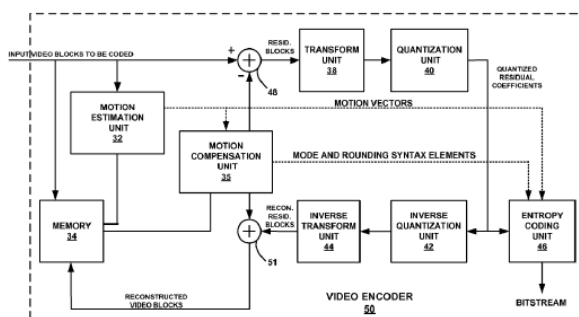


FIG. 2

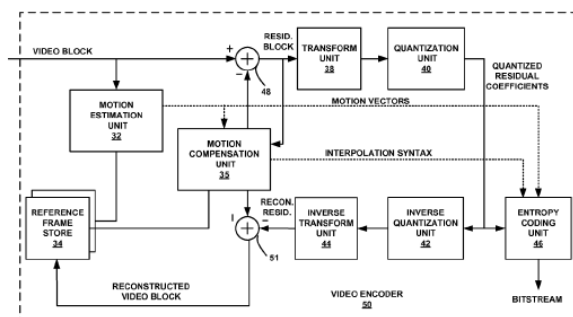


FIG. 2

Ex-1005, Fig. 2, ¶53 (“During the encoding process, video encoder 50 receives a video block to be coded, and motion estimation unit 32 and motion compensation unit 35 perform inter-predictive coding.”).

Ex-1006, Fig. 2, ¶56 (“During the encoding process, video encoder 50 receives a video block to be coded, and motion estimation unit 32 and motion compensation unit 35 perform inter-predictive coding.”).

103. These figures are, again, entirely generic, and depict basic components such as a “memory,” “motion estimation unit,” “motion compensation unit,” and “entropy coding unit” which can be found in virtually any video coding system since the 1990s. Dr. Freedman agreed with me on this point, and describes Karczewicz-I’s Figure 2 as “[t]he model of a typical general video encoder” that “has been used by major video encoding standards since the 1990s.” ASUS-1003 Appendix B at ¶ 3. I note that both of the above figures disclose essentially the same set of basic components in the same configuration as those illustrated in my book (Ex-2021) at page 69, which I discuss above. Accordingly, that the same two figures are presented

in both Karczewicz-I and Karczewicz-II does not reflect their inherent suitability for combination so much as it reflects their sharing the same three inventors (Marta Karczewicz, Peisong Chen, and Yan Ye), and I would speculate, a desire to avoid unnecessary effort in producing introductory diagrams by those drafting the references. These figures would not provide any inspiration to a POSITA to combine and modify the two references. Rather, a POSITA would recognize the figures as depicting generic video coding systems that have existed since the 1990s. This consistent use of the same generic architecture over the course of decades would not lead a POSITA to search for a way to modify such a system.

104. Whilst Dr Freedman states that the Karczewicz references both disclose “similar architectures”, Dr Havlicek appears to disagree with Dr Freedman. In referring to the Karczewicz-I and Karczewicz-II combination, Dr. Havlicek states that the “references share the same architecture, and the combination does not change the architecture; it simply uses more bits for intermediate calculations (Ex 1003 at para 35). I disagree that the Karczewicz references share the same architecture, for the reasons I explain above. I further fail to understand how Dr Havlicek can “agree with and adopt [Dr Freedman’s] analysis as [his] own” (Ex 1003 at para 34) whilst disagreeing on this important point, namely whether the two Karczewicz references have similar architectures or the same architecture.

105. The shared inventorship of the two Karczewicz references is also in my view highly relevant. During his deposition, Dr. Freedman denied any familiarity with the inventors, even saying that he could not be sure that they were persons of ordinary skill in the art. *See* ASUS-1030 at 76:19-78:22. As a professional with years of experience in the video coding industry, however, I am familiar with all three inventors and indeed very familiar with Dr. Marta Karczewicz. Dr. Karczewicz is a well-known, world-leading expert in video compression, currently occupying the role of Vice President of Technology at Qualcomm, where she continues to make significant contributions to the field of video coding. Dr. Karczewicz has made many technical contributions to international standards, taking a very active role in working groups such as the Joint Video Team and Joint Coding Team – Video Coding, as part of the MPEG and VCEG standardization committees. Dr. Karczewicz has been recognized by the European Patent Office as one of the “50 Leading Tech Voices” as part of the European Patent Office’s celebration of 50 years of the European Patent Convention. Ex-2026. Though Dr. Freedman may not be sure if Dr. Karczewicz is a POSITA, in my opinion her skills, education, and experience would establish her as a person of *extraordinary* skill in the art. Accordingly, the idea that Dr. Karczewicz would have overlooked an “obvious” combination and modification of her own inventions, despite the supposed “architectural similarity” between them, lacks credibility.

106. Further, the disclosures of Karczewicz-II (which relate to subpixel interpolation—not bi-prediction) are coextensive with VCEG-AI33, a standards contribution co-authored by Dr. Karczewicz and corresponding to the same inventions. *See* ASUS-1006 at ¶ 104, Table 7, 8 (showing the disclosed interpolation process and 16-bit registers); Ex-2019 at pp. 1-4 (showing the same interpolation process and registers). VCEG-AI33 was “incorporated by reference in its entirety” into Karczewicz-I. *See* ASUS-1005 at ¶ 37. Based on this, it is clear that Dr. Karczewicz had all the ingredients necessary to make the combination and modifications that Dr. Freedman proposes are obvious, and yet she and her co-authors did not do so. Therefore, I conclude that a POSITA with nothing more than a bachelor’s degree and a few years of industry experience would not find the inventions of the ’267 Patent obvious based on the disclosures of Karczewicz-I and Karczewicz-II. *See* ASUS-1003 Appendix B at ¶ 36 (stating that a POSITA would have “a (1) Bachelor’s degree in electrical engineering, computer engineering, computer science, or a comparable field of study such as physics, and (2) approximately two to three years of practical experience with video encoding/decoding”).

107. During deposition, Dr. Freedman speculated that the inventors of Karczewicz-I and Karczewicz-II may not have been aware that the applications had been filed in the first place. *See* ASUS-1030 at 79:18-80:12 (“I am sorry to say that

there are organizations that will file patent applications that may never have been reviewed or notified to their inventors . . . So, I cannot tell you whether those people actually even knew the patent application was being filed”). To the extent that Dr. Freedman intended to suggest that the reason that this supposedly “obvious” modification did not come about sooner was simply that the three co-authors did not realize the nature of their own work, I disagree. In my opinion, a more reasonable explanation is that Karczewicz-I and Karczewicz-II are not obvious to combine and modify in the way alleged by Dr. Freedman at all, and that it is only through the benefit of hindsight and reference to the inventions of the ’267 Patent that Dr. Freedman draws the opposite conclusion.

108. As I discuss above, Karczewicz-I discloses improving conventional bi-prediction by adaptively selecting the offsets used during rounding performed when calculating the final prediction and minimizing the number of offsets used. *See* ASUS-1005 at ¶¶ 63-65. The reference explains that careful choice of rounding offset can improve bi-directional prediction. Thus Karczewicz-I proposes a potential solution to the problem of bidirectional prediction performance that does **not** involve increasing the precision of the two component predictions. Instead, Karczewicz-I adjusts the rounding offset to improve prediction performance but maintains all predictions at the original pixel precision and bit depth. Each of the predictions $\text{pred}(i,j)$, $\text{pred0}(i,j)$ and $\text{pred1}(i,j)$ are retained at the original bit depth, as

demonstrated by Karczewicz-I's calculation of $\text{pred}(i,j)$. *See id.* at ¶¶ 64-66. This alone would teach away from the proposed combination and modifications because Karczewicz-I already discloses a solution to the problem of prediction performance and so a POSITA would not look to replace this or add to this solution in the way Dr. Freedman suggests.

109. Further, Karczewicz-II does not propose an improvement to the bi-prediction process itself. Instead, that reference discloses improving a different process, subpixel interpolation, by maintaining a higher precision for intermediate calculation of subpixel values. *See, e.g.*, ASUS-1006 at ¶ 88.

110. Karczewicz-II does not disclose improving bi-prediction accuracy, at most it teaches how to improve the performance of interpolation. Karczewicz-II's process does not output higher-precision predictions, it outputs subpixel values at the same 8-bit precision as the pixels used to obtain them. *See id.* at ¶ 102. Nothing in Karczewicz-I or Karczewicz-II states or hints that techniques of Karczewicz-I could be substituted for those of Karczewicz-II to yield predictable results for bi-prediction.

111. Further still, Dr. Freedman's description of how a POSITA would be motivated to modify Karczewicz-I by applying Karczewicz-II's "optimizations for averaging integer, half, and center pixels" are structured into three distinct scenarios, each of which operates differently and varies in the bit-depth of output prediction

values. *See* ASUS-1003 Appendix B at ¶ 150. Rather than motivating a POSITA to modify Karczewicz-I as Dr. Freedman describes, these so-called scenarios (which are a subset of possible outcomes) present additional computational complexity in an encoder implementing Dr. Freedman's proposed system, including additional computing, logic and/or memory storage costs, and that would suggest to a POSITA that such a combination was undesirable.

112. During video coding, an encoder determines a motion vector describing the position of a block in a frame which closely matches the macroblock being coded. Ex-2021 at 31. This process involves searching previously coded frames for a block of pixels which, if used as the basis for a prediction, minimizes the chosen matching criteria—typically the residual formed when subtracting the prediction from the block being coded. *See id.* at 31-32. During bi-prediction, two such motion vectors must be determined such that their combined predictions minimize the residual error, requiring further comparisons between potential best matches.

113. Dr. Freedman proposes that one of scenarios should apply based on the characteristics of both motion vectors used for bi-prediction. ASUS-1003 Appendix B at ¶ 150.

114. In his first scenario, corresponding to a half-pixel first motion vector and integer pixel second motion vector, he says that Karczewicz-II's Table 3 calculations should be applied, resulting in 13-bit prediction values. *Id.* at ¶¶ 151-

153. In his second scenario, where the first motion vector points to a “center-pixel position” and the second motion vector points to a half-pixel position, he proposes using the same interpolation methodology to yield 15-bit values. *Id.* at ¶¶ 157-159. Finally, his third scenario applies to two half-pixel motion vectors and uses Karczewicz-II’s Table 2 equations to produce a 15-bit prediction for each interpolated pixel. *Id.* at ¶¶ 163-165. Each of these scenarios results in a different value which may potentially have a different bit-depth. Dr Havlicek therefore is incorrect to state that across these three scenarios, ‘Karczewicz-II treats each type of motion vector the same’ (ASUS-1003 at ¶36).

115. As a result of these different potential interpolation equations, an encoder implementing Dr. Freedman’s three scenarios would be forced to allocate additional space in which to store each possible intermediate prediction value computed for a first motion vector while the second prediction is calculated. Further, because an encoder must repeatedly test potential predictions to determine which minimizes residual, this storage cost would be magnified. In a software environment, these costs would lead to additional memory and processing overhead which would be detrimental to the computational performance of an encoder. In a hardware environment, additional memory and logic to account for disparate scenarios translates to increased chip complexity and cost. Dr. Freedman does not consider or comment on these additional technical costs, noting that he was “not qualified to

“speak about the internals of any piece of hardware.” ASUS-1030 at 104:3-16. However, as I explained above, a POSITA would not choose to add computational complexity and additional storage requirements without a strong motivation to do so.

116. Because Dr. Freedman is unfamiliar with hardware, he instead discusses how such a system would be implemented at a software level, suggesting that it would be a “tiny change” that can be “decided with a switch statement” or an “if” statement.” *Id.* at 102:21-103:10. Dr. Freedman is suggesting adding “separate code branches” which would need to be written for bi-directional averaging, which the ’267 Patent discusses as an undesirable feature of prior attempts at solving the rounding error problem. ASUS-1001 at 4:21-25. Worse still, the ’267 Patent here criticizes the use of two branches, but Dr. Freedman’s proposed modifications implicate three or more extra code branches. A POSITA would be aware of the likely significant computational cost of adding further “code branches” to an operation (calculating bi-prediction values) that may be carried out millions of times per second in a typical video coding application⁴. *See id.* Dr Havlicek suggests that the

⁴ Consider a 30 frames per second High Definition video sequence. Each frame comprises $1920 \times 1080 = 2073600$ pixels. Assume (conservatively) that 20 frames per second use bi-prediction and that 10% of pixel values within these frames are predicted using bi-prediction. Over 4 million pixel values per second are predicted using bi-prediction at the decoder.

computing costs of code branches or logic are ‘generic costs that were already needed’ (ASUS-1003 at ¶ 37). This is incorrect, as Dr Freedman’s proposed changes results in **additional** computing, logic and/or memory storage costs that were not present in Karczewicz 1, as I explain above. The question is not whether or not code branches are known or used in the art, it is whether a POSITA would be motivated to add significantly **more** computing and/or logic as Drs Havlicek and Freedman propose. Far from being a ‘minor implementation detail’ as Dr Havlicek suggests (ASUS-1003 at ¶ 39), the considerable additional costs of computing, logic and/or memory storage of the proposed combination (K1 with K2) significantly change the principle of operation of K1 with no evidence or guarantee of an accompanying performance benefit.

117. As I have discussed above, it is my opinion that a POSITA would not be motivated to make the modifications which Dr. Freedman proposes. In addition, I believe a POSITA would recognize that Dr. Freedman’s proposal would incur considerable technical costs and disadvantages. Accordingly, it is my opinion that the challenged claims are not rendered obvious by the combination of Karczewicz-I and Karczewicz-II.

C. The '267 Patent Claims are Valid

1. Independent Claims 1, 7, and 13

118. Based on the above discussion, it is my opinion that a POSITA would not be motivated to combine and modify Karczewicz-I and Karczewicz-II to make the inventions of claims 1, 7, and 13.

2. Dependent Claims 2, 8, and 14

119. Dependent claims 2, 8, and 14 depend on independent claims 1, 7, and 13 respectively. These claims include the additional limitation “wherein in an instance in which said first motion vector points to a subpixel, said first prediction is obtained by interpolation using pixel values of said first reference block.” It is my opinion that a POSITA would not be motivated to modify Karczewicz-I and Karczewicz-II to make the inventions of claims 2, 8, and 14 for the same reasons as for the claims on which they depend.

3. Dependent Claims 3, 9, and 15

120. Dependent claims 3, 9, and 15 depend on claims 2, 8, and 14 respectively. These claims include the additional limitation “wherein said first prediction is obtained by interpolation using values of said first reference block by: right shifting a sum of a P-tap filter using values of said first reference block.” It is my opinion that a POSITA would not be motivated to combine and modify

Karczewicz-I and Karczewicz-II to make the inventions of claims 3, 9, and 15 for the same reasons as for the claims on which they depend.

4. Dependent Claims 4, 10, and 16

121. Dependent claims 4, 10, and 16 depend on claims 2, 8, and 14 respectively. These claims include the additional limitation “wherein in an instance in which said second motion vector points to an integer sample, said second prediction is obtained by shifting values of said second reference block to the left.” It is my opinion that a POSITA would not be motivated to combine and modify Karczewicz-I and Karczewicz-II to make the inventions of claims 4, 10, and 16 for the same reasons as for the claims on which they depend.

5. Dependent Claims 5, 11, and 17

122. Dependent claims 5, 11, and 17 depend on claims 1, 7, and 13 respectively. These claims include the additional limitation of decreasing the precision of the combined prediction by shifting bits of the combined prediction to the right by inserting a rounding offset to the combined prediction before said decreasing. It is my opinion that a POSITA would not be motivated to combine and modify Karczewicz-I and Karczewicz-II to make the inventions of claims 5, 11, and 17 for the same reasons as for the claims on which they depend.

6. Dependent Claims 6, 12, and 18

123. Dependent claims 6, 12, and 18 depend on claims 1, 7, and 13 respectively. These claims include the additional limitation “wherein the first precision indicates a number of bits needed to represent the values of the pixels, and the second precision indicates the number of bits needed to represent values of said first prediction and values of said second prediction.” It is my opinion that a POSITA would not be motivated to combine and modify Karczewicz-I and Karczewicz-II to make the inventions of claims 6, 12, and 18 for the same reasons as for the claims on which they depend.

7. Independent Claims 19, 25, and 31

124. Independent claims 19, 25, and 31 are decoding claims corresponding to encoding claims 1, 7, and 13. I understand that Dr. Freedman’s opinions with respect to these claims are largely the same as the ones he offers for their encoding counterparts, and so I disagree with him for the same reasons.

125. Additionally, I note that the same technical costs associated with Dr. Freedman’s three proposed scenarios for modifying Karczewicz-I using Karczewicz-II are also applicable to a decoder. A decoder which generates predictions using Dr. Freedman’s three scenarios would necessitate that bitstreams be conducted by an encoder using the same logic to generate its predictions and determine motion vectors to be encoded. A POSITA would understand that creating

a decoder implementing Dr. Freedman's proposed modifications would mean incurring the same encoding costs that I described with respect to claims 1, 7, and 13. Accordingly, it is my opinion that a POSITA would not be motivated combine and modify Karczewicz-I and Karczewicz-II as Dr. Freedman states.

8. Dependent Claims 20, 26, and 32

126. I note that Dr. Freedman's opinions with respect to decoding claims 20, 26, and 32 are substantially the same as his arguments with respect to encoding claims 2, 8, and 14. Accordingly, it is my opinion that these claims are valid for the same reasons.

9. Dependent Claims 21, 27, and 33

127. I note that Dr. Freedman's opinions with respect to decoding claims 21, 27, and 33 are substantially the same as his arguments with respect to encoding claims 3, 9, and 15. Accordingly, it is my opinion that these claims are valid for the same reasons.

10. Dependent Claims 22, 28, and 34

128. I note that Dr. Freedman's opinions with respect to decoding claims 22, 28, and 34 are substantially the same as his arguments with respect to encoding claims 4, 10, and 16. Accordingly, it is my opinion that these claims are valid for the same reasons.

11. Dependent Claims 23, 29, and 35

129. I note that Dr. Freedman's opinions with respect to decoding claims 23, 29, and 35 are substantially the same as his arguments with respect to encoding claims 5, 11, and 17. Accordingly, it is my opinion that these claims are valid for the same reasons.

12. Dependent Claims 24, 30, and 36

130. I note that Dr. Freedman's opinions with respect to decoding claims 24, 30, and 36 are substantially the same as his arguments with respect to encoding claims 6, 12, and 18. Accordingly, it is my opinion that these claims are valid for the same reasons.

VIII. Dr. Marta Karczewicz

131. I am the named inventor on 11 patents or patent applications. I have received patent grants from the United States Patent and Trademark Office ("USPTO"), the European Patent Organization ("EPO"), and the World Patent Organization.

132. From experience, I am familiar with the EPO's website, <https://www.epo.org>. The EPO's website provides official information regarding patents as well as news and information related to the EPO and to prominent figures related to European intellectual property. Based on my experience, I understand information on the EPO's website to be reliable. I am also aware that the USPTO

includes a description of the EPO and a link to the same www.epo.org website on its own webpage. Ex-2029.

133. I have reviewed Ex-2026, a webpage from the EPO's website titled "Marta Karczewicz." Ex-2026 is a short discussion of the achievements of Marta Karczewicz which the EPO published as part of a series on the "50 Leading Tech Voices." This series was published during the EPO's celebration of the 50th anniversary of the European Patent Convention which formed the EPO.

134. I have reviewed Ex-2028, a webpage from the EPO's website titled "Marta Karczewicz." Ex-2028 is a short discussion of the achievements of Marta Karczewicz which the EPO published in connection with her selection as a finalist for the European Inventor Award 2019, Lifetime Achievement Category. This was published in connection with annual awards by the EPO for the most impactful inventors in the world.

135. I am familiar with Dr. Karczewicz and her work in video coding. Based on my experience of Dr. Karczewicz's work and achievements, Ex-2026 and Ex-2028's characterizations of Dr. Karczewicz's achievements is accurate. I was familiar with the achievements of Dr Karczewicz listed in Ex-2026 and Ex-2028 prior to my involvement in this IPR proceeding. For example, these achievements are consistent with biographies of Dr Karczewicz that I have read in peer-reviewed

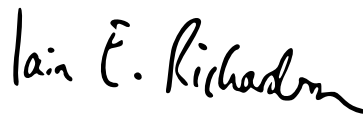
journal articles such as articles published in the IEEE Transactions on Circuits and Systems for Video Technology.

IX. Conclusion

136. This Declaration represents the opinions that I have formed to date based on the material currently available to me. I reserve the right to revise, supplement, and/or amend my opinions stated in this Declaration based on new information that becomes available to me and on my continuing analysis of the materials available.

137. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine, imprisonment, or both, under 18 U.S.C. § 1001.

Dated: October 7, 2025



Dr. Iain Richardson