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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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***EX PARTE* REEXAMINATION COMMUNICATION TRANSMITTAL FORM**

REEXAMINATION CONTROL NO. 90/019,426 .

PATENT UNDER REEXAMINATION 6816809 .

ART UNIT 3992 .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Final Office Action

This is a Final Office Action of claims 1-17 of United States Patent Number: 6,816,809 issued to Circenis (hereinafter the '809 Patent), responsive to the Patent Owner's Response to Non-Final Office Acton dated 7/3/2025. Reexamination was ordered on 5/20/2024 responsive to the Request for *ex parte* reexamination filed 2/21/2024.

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

References

- M.M. Theimer and K.A. Lantz, "Finding Idle Machines in a Workstation-based Distributed System," *EEE Transactions on Software Engineering*, vol. 15, no. 11, pp. 1444-1458 (November 1989) (EX1101, "Theimer")
- Japanese Patent Application No. 60-24655 (EX1005, "Ogawa")

- E. Hoekstra et al., "Design and Implementation of a DSP Based MPEG-1 Audio Encoder," JEEE Transactions on Consumer Electronics, vol. 45, no. 1, pp. 31-35 (Oct. 1998) (EX1102, "Hoekstra")
- U.S. Patent No. 7,032,119 (EX1103, "Fung-119")
- U.S. Patent No. 6,166,984 (EX1007, "Bohac")
- U.S. Patent No. 4,458,307 (EX1010, "McAnlis")
- U.S. Patent Pub. No. 2002/0133728 (EX1104, "Agarwal")

Prosecution History

Original Examination:

The '809 Patent was originally filed as U.S. Patent Application Serial No. 10/200,175 on July 23, 2002.

On 10/6/2003, the Office mailed a Non-Final rejection in which the claims were rejected under 35 USC § 103 over U.S. Patent No: 6,049,798 (to "Bishop") and U.S. Patent No.: 4,503,495 (to "Boudreau").

On 1/6/2004, Patent Owner (then Applicant) filed an amendment to the claims further specify a "idle indicator" rather than the previously claimed "state indicator":

1. (Currently Amended) A hardware based utilization metering device, comprising:

[a state] an idle indicator coupled to a processor, wherein the [state] idle indicator receives an indication when the processor is in a first state;

a counter coupled to the [state] idle indicator and coupled to a system clock, wherein the counter receives a measure of system time from the system clock and receives data related to the indication when the processor is in the first state, and generates a counter value indicative of time the processor is in the first state; and

a data usage provider coupled to the counter, wherein the data usage provider is capable of providing the counter value.

On 1/8/2004, the Office conducted an interview between Hien X. Vo (the Examiner of record) and John Harrop (the Attorney of record) where the Examiner noted in his Interview Summary that "Upon a receipt of amendment, the prior arts do not disclose a plurality of processors and the idle indicator of processors in a busy state."

On 4/6/2004, the Office mailed a Notice of Allowance without any further reasons for allowance.

Continuation Application (10/892,231):

The applicant filed U.S. Application No. 10/892,231 ("the '231 application") on July 16, 2004, as a continuation of the '175 application that issued as the '809 patent.

The Examiner for the '231 application was the same Examiner who reviewed the '175 application. The Examiner rejected '231 application claim 1 as anticipated by Vea (EX1006), finding that "Vea discloses... an idle indicator coupled to a processor" and a

“counter... coupled to said idle indicator[.]” EX1014, 300. The Examiner also rejected ’231 application claim 1 for non- statutory obviousness-type double patenting, finding it “not patentably distinct” from ’809 Patent claim 1. EX1014, 296-297. Thus, the Examiner found that Vea anticipated a claim that was patentably indistinct from ’809 Patent claim 1.

Following claim amendment, the Examiner rejected amended application claim 1 to “a device for metering processor utilization” as obvious over Vea and another reference, finding that Vea taught a system clock “to provide a count corresponding to the amount of time spent in at least one of said busy[] and idle states” as well as an “idle indicator” and “a counter” coupled to the idle indicator. EX1014, 366-367.

IPR2022-01197:

On 7/5/2022, Google (the same 3PR as in the present reexam) filed a petition for inter partes review challenging claims 1-17 of the ’809 patent in IPR2022-01197 on the following grounds:

Grounds 1-5 relied on Ogawa. EX1107, 10-41.

Grounds 6-8 relied on Vea. EX1107, 41-68.

On 1/3/2023, the Board denied institution. Paper 9, 12-20 (Mar. 29, 2023), attached as EX1108 for the following reasons:

For Grounds 1-5, reviewing the prosecution history, the Board described the Examiner as allowing the claims over Bishop because Bishop disclosed “calculating CPU utilization by, infer alia, running a program on a CPU.” EX1108, Paper 9, 17-18. The Board found that “similar to Bishop’s device, Ogawa runs a ‘program’ in order to

obtain the CPU's usage rate." EX1108, Paper 9, 18. The Board found that the Petition "has not explained how Ogawa's reliance on a software program to obtain CPU usage is distinguishable over Bishop's use of a software program to calculate CPU activity, or demonstrated sufficiently how such reliance on software corresponds to the limitations in claim 1." EX1108, Paper 9, 19.

For Grounds 6-8, the Board denied institution in its discretion under 35 U.S.C. §325(d), as a European counterpart to Vea was shown to be evaluated after allowance, by the Examiner initialing next to it on a 1449.

Litigation History

The '809 Patent has been involved in the following litigation (currently STAYED pending resolution of IPR petitions on five of six asserted patents including the '809 patent):

- *Valtrus Innovations, Ltd. v. Google LLC, No. 3:22-cv-00066 (N.D. Tex.)*
- *Valtrus Innovations, Ltd. v. Google LLC, No. 4:22-cv-00020 (N.D. Tex.)*

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 8-10, and 12 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Fung (U.S. Patent No. 7,032,119), hereinafter Fung-119.

Reading of the Fung-119 reference on the claims is further provided on pages 74-125 of the Request. Fung-119 incorporates by reference U.S. Patent No: 5,710,929, herein referred to as Fung-929.

[1PRE] - "A hardware based utilization metering device comprising:"

To the extent the preamble is considered to be limiting, Fung-119 meets it because Fung-929 discloses a hardware-based metering device that monitors central processing unit ("CPU") activity as explained below.

a) Terms

One of ordinary skill in the art would understand "metering" to mean "measuring". Madisetti-EPR, ¶94 (citing EX1013, EX1016).

b) Fung-929's hardware-based metering device.

Fung-929 discloses power management unit 15 (annotated Figs. 1-2 below) that incorporates a hardware monitor 79 comprising "circuitry" (e.g., hardware) that measures CPU utilization "independently from... software" and a "software monitor[.]" Fung-929, 5:44-47.

Figure 2 distinguishes hardware monitor 79 and its components (activity monitor 16 and timer unit 24) from software monitor 80. Fung-929, Figs. 1-2. Figure 3 provides further detail on hardware monitor 79. "[T]he hardware monitor 79 and power management unit 15 are provided in FIG. 3 as a hardware embodiment" Fung-929, 7:1-2. "[T]he power management unit 15 includes the hardware monitor 79 (activity monitor 16 and timer unit 24) which is designed to operate with minimal system requirements and without software support." Fung-929, 6:55-58.

POSITAs would have understood that the monitor "circuitry," including the activity monitor as explained below, were hardware. Madisetti-EPR, ¶298. This provides a "hardware based utilization metering device" as explained for limitations [1A]-[1C], thus meeting [1PRE]. Madisetti-EPR, ¶298.

The diagram illustrates a system architecture with the following components and connections:

- Hardware Monitor 79:** Connected to the **POWER MANAG. UNIT** (15) via a dashed line.
- CPU (4):** Connected to a system bus (5) and the **POWER MANAG. UNIT** (15) via NMI and other signals.
- POWER MANAG. UNIT (15):** Receives signals from the CPU, hardware monitor, and various power sources. It outputs signals like LB, LLB, ACPRV, and RAS/CAS to the **DRAM** (8).
- PC CTRL (13):** Connected to the system bus (5) and the **POWER MANAG. UNIT** (15).
- System Bus (5):** Connects the CPU, PC CTRL, I/O units, and Peripheral units.
- I/O Units (6-0 to 6-n):** Connected to the system bus (5) and output CLKOUT signals.
- Peripheral Units (7-0 to 7-n):** Connected to the I/O units and output R1 signals.
- DRAM (8):** Receives control signals from the **POWER MANAG. UNIT** (15) and is connected to the system bus (5).
- Power Supply (9):** Receives input from **AC** (14) and **BAT** (14). It outputs VCC and VSS.
- Switches (SW):** A series of switches (SW(CPU), SW(PC), SW(0) to SW(n)) are connected to the power supply and the system bus (5).
- Control Signals:** Various control signals (e.g., 27, 28, 29, 30, 31, 32, 33) are shown connecting different components.

Fung-929, Fig. 1 (annotated).

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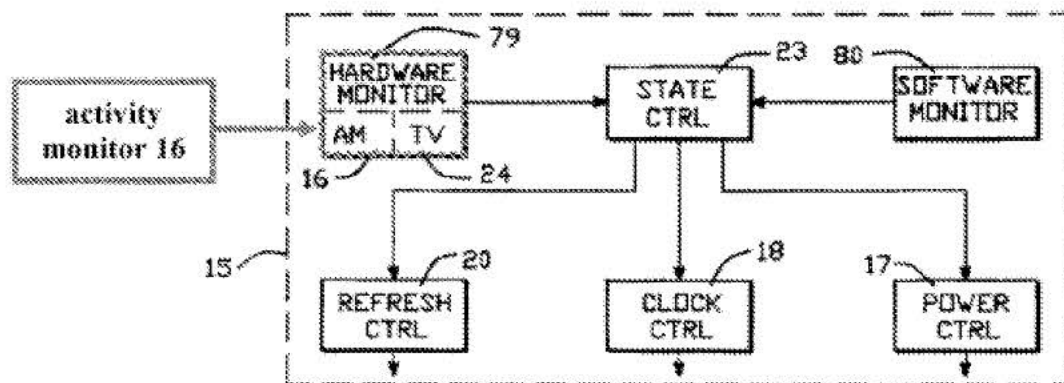


FIG. -2

Fung-929, Fig. 2 (annotated) showing PMU 15 components.

The activity monitor 16, timing unit 24, and other PMU 15 components are discussed further below.

[1A] – an idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state;

Fung-119 discloses “[t]he activity level of the CPU is monitored and a control signal... is generated based on that sensed activity or lack of activity.” Fung-119, 21:16-19. As detailed below, Fung-929 has an activity monitor 16 that is coupled to a processor [CPU 4] and receives indications of the CPU being in a first state and meets the “idle indicator” in limitation [1A].

a) “first state” may be busy or idle

The '809 specification says "[t]he idle indicator 120 is capable of providing either an 'idle' indication or a 'not-idle'/'busy' indication." EX1001, 3:57-60. The '809 patent describes two processor "states": (1) a "busy" state where "the CPU is running processes that perform useful work for the user," and (2) an "idle" state where "the CPU is not performing useful work." EX1001, 3:18-27; ([1PRE]). Thus, "first state" is a generic term encompassing a "busy" or an "idle" state. E.g., EX1001, claim 2 ("first state is a busy state"), claim 4 ([4B]: "processor is in the idle state"), Abstract ("first state... may be a busy state), 3:23 (similar), 3:26 ("first state may be an idle state where the CPU is not performing useful work"), 4:1-5 ("CPU 110 is not in an idle state" when it "is performing a service for the user of system 100").

b) Fung-119

Fung-119's CPU 404-1 and Fung-929's CPU 4 each is a processor just like the '809 patent's CPU 110. EX1001, Abstract, Fig. 1A. Fung-119 meets limitation [1A] because it incorporates Fung-929, and Fung-929's activity monitor 16 is the "idle indicator" meeting [1A].

(1) Fung-119 uses Fung-929's system to monitor CPU activity (e.g., CPU state).

Fung-119 describes monitoring CPU activity level in individual server modules for a multi-processor system. **Fung-119, 21:13-17** ("Attention is now focused on the

internal structure and operation of the server module 302. During operation CPU 320 executes commands or instructions [in a “busy” state], or **when no instructions are present to be executed, executes idle threads [in an “idle” state]. The activity level of the CPU is monitored[.]**). As noted above, Fung-119 “extends earlier power management systems, architectures, and methods” — including those in Fung-929 — “to multi-server or multi-node architectures.” Fung-119, 48:30-37. Thus, POSITAs understood that Fung-119 describes Fung-929’s techniques to monitor the activity level of a CPU in individual server modules.

(2) Fung-929’s hardware monitor 79 determines the CPU’s busy or idle state using activity monitor 16.

Fung-929’s **“hardware monitor 79 monitors the CPU to detect activity and inactivity. The hardware monitor 79 typically is circuitry for detecting inactivity independently from the software and the software monitor 80.”** Fung-929, 5:44-47. That is consistent with Fung-929’s explanation that “hardware monitor 79 and power management unit 15 are provided in FIG. 3 as a hardware embodiment[.]” Fung-929, 7:1-2. POSITAs understood that monitor “circuitry” for detecting inactivity “independently from software” means that Fung-929 uses hardware for “metering” and meets claim 1’s preamble.

Fung-929 further teaches, in 5:47-54, that “[H]ardware monitor 79 senses predetermined address ranges, such as an I/O address range and a video memory address range, and monitors the activity of addresses by the CPU to addresses within these ranges. If no data transfers occur within the specified address ranges for

predetermined periods of time, then a power control mode is entered to conserve power in the computer system.”

Hardware monitor 79 senses these “predetermined address ranges” using activity monitor 16 to evaluate activity on CPU bus 5. Fung-929, Fig. 2, 6:21-24 (“The hardware monitor 79 (using activity monitor 16) analyzes the address activity on the system bus 5 [e.g., CPU bus 5 (Fung-929, 4:38)] to provide activity information used to control power management.”), 6:55-58 ([T]he power management unit 15 includes the hardware monitor 79 (activity monitor 16 and timer unit 24) which is designed to operate with minimal system requirements and without software support.”).

POSITAs understood that the CPU bus connects and provides communication between the CPU and computer system components like memory and input/output (“I/O”) devices so that the activity on the CPU bus monitored by activity monitor 16 includes CPU communication with memory and I/O devices. Fung-929, 5:47-54, 6:21-24, Fig. 3 (showing CPU bus 5 signal inputs to activity monitor 16). POSITAs also understood that an idle CPU—such as a CPU whose clock was stopped—would not communicate with memory or I/O devices on the CPU bus. Madisetti-EPR, ¶309.

Annotated Fung-929 Fig. 2 shows hardware monitor 79 comprising activity monitor 16 (AM 16) and timer unit 24 (TV 24) (Fung-929, 6:16-19):

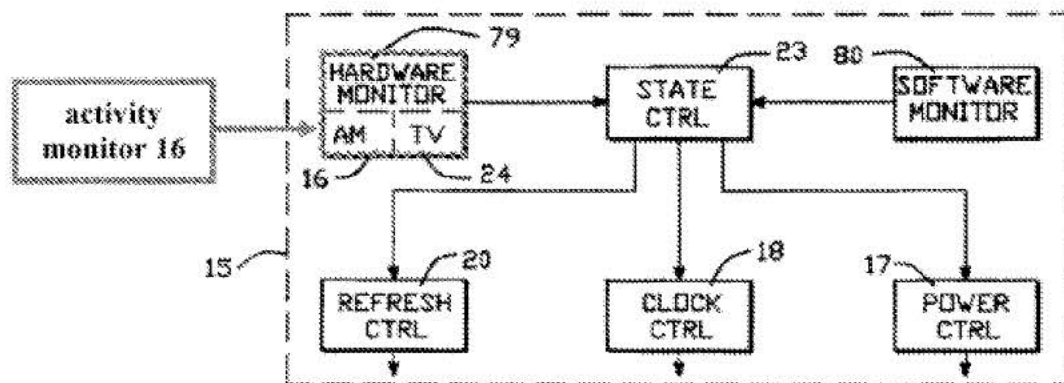


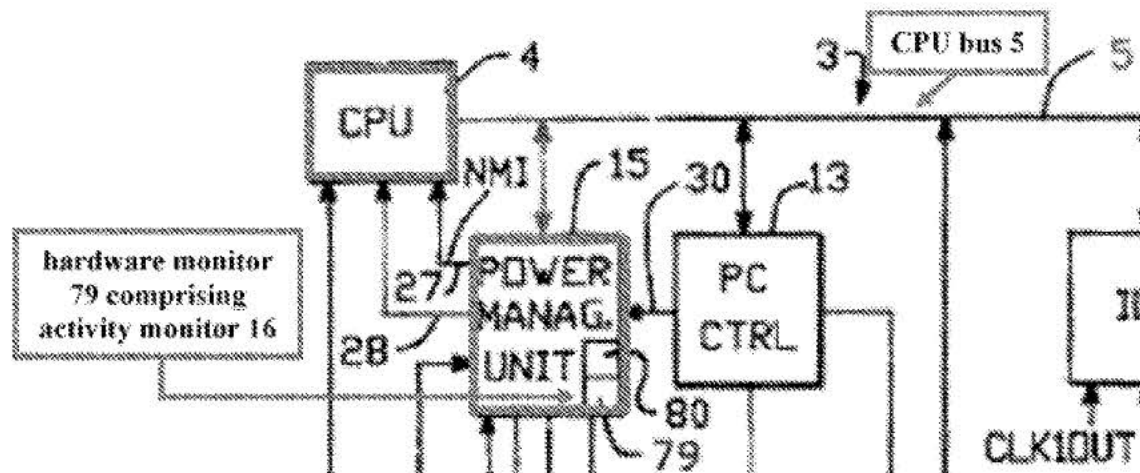
FIG.-2

Fung-929, Fig. 2 (annotated) showing PMU 15 components.

Like hardware monitor 79, activity monitor 16 is hardware. Fung-929, 7:1-2. It “monitors the activity level of the computer system and generates a first inactivity indicator after a first predetermined period of inactivity and a second inactivity indicator a second predetermined period of inactivity after generating the first inactivity indicator.” Fung-929, 38:47-54.

(a) the activity monitor 16 is “coupled to a processor”

Activity monitor 16 is coupled to the processor (CPU 4) via CPU bus 5 (Fung-929, 4:35-40). Figure 1 shows power management unit (“PMU”) 15 coupled to CPU bus 5. PMU 15 contains hardware monitor 79 which in turn contains activity monitor 16. Fung-929, Fig. 1 (power management unit 15 comprising hardware monitor 79 coupled to CPU 4 and CPU bus 5), Fig. 2 (hardware monitor 79 contains activity monitor 16).



Fung-929, Fig. 1 (annotated, exploded).

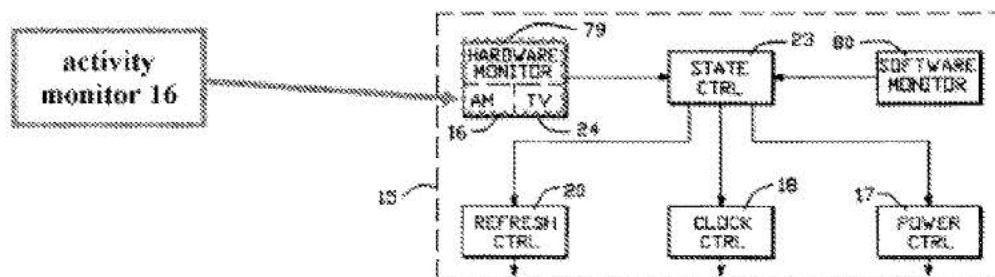
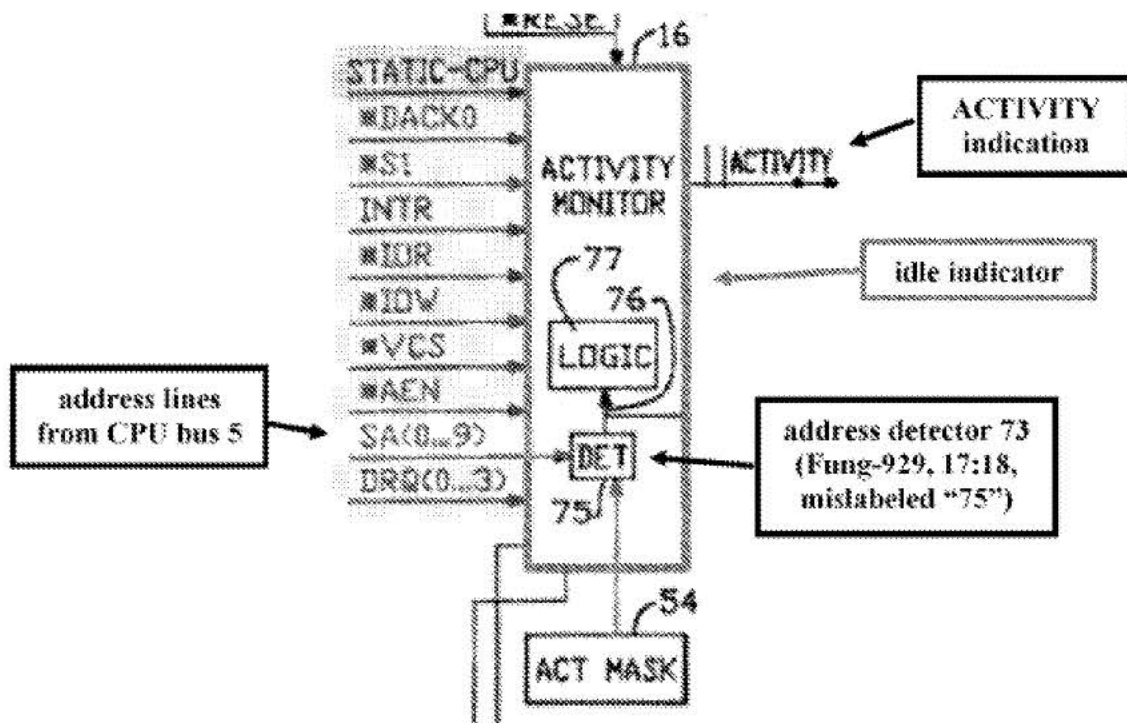


FIG. -2

Fung-929, Fig. 2 (annotated) showing PMU 15 components.

Fung-929 describes activity monitor 16 as coupled to the processor because activity monitor 16 receives signals that originate in the processor including "control lines and address lines SA(0 . . . 9) from [CPU] bus 5[]" where the addresses represent "the address activity of the CPU 4." Fung-929, 17:18-30; id., 5:47-51 ("[H]ardware monitor 79 senses predetermined address ranges... and monitors the activity of addresses by the CPU to addresses within these ranges."), 7:18-19 ("hardware monitor 79 senses the activity of addresses on the [CPU] bus 5."), 6:21-24 ("The hardware monitor 79 (using activity monitor 16) analyzes the address activity on the system bus 5 to provide activity information used to control power management."). Figure 3 shows activity monitor 16 signal inputs.



Fung-929, Fig. 3 (annotated, exploded).

Fung-929 explains:

The activity monitor 16 includes an address detector 73 [mislabeled "75" in Fig. 3] which receives addresses from [CPU] bus 5 representing the address activity of the CPU 4. The address detector 73 receives, for example, control lines and address lines SA(0 . . . 9) from bus 5 for sensing when those addresses are within the predetermined address set.

Fung-929, 17:18-23. Fung-929's reference to "addresses," "address activity," and "address lines" show addresses the CPU sent and received on CPU bus 5. Thus, it shows that "the address activity of CPU 4" meant addresses for lines carrying signals from CPU 4.

(b) "idle indicator receives an indication when the processor is in a first state"

Fung-929's activity monitor 16 "receives an indication" of the CPU being in an idle state and in a busy state, either of which meets the claimed first state.

(i) Idle State

Activity monitor 16 receives an indication that CPU 4 is "idle," e.g., not performing useful work for a user.

First, activity monitor 16 receives a "STATIC-CPU" input. Fung-929, Fig. 3. **The "STATIC-CPU" line is connected to the power supply, e.g., Vcc, "if CPU is static."** **Fung-929, 11:53-55, 12:27.** Put differently, when the CPU is "static" the power supply voltage Vcc is asserted on the STATIC-CPU line, e.g., the STATIC-CPU signal is the power supply voltage Vcc.

The CPU being "static" means it is idle because the CPU's clock is stopped. Fung-929 explains, "CLKOUT, as controlled by PMU 15 and control block 49, drives CPU 4. The CLKOUT clock can be stopped for static CPU's, or reduced automatically by a divisor specified in the CLOCK field of control register 53 during DOZE and SLEEP states." Fung-929, 8:1-5, 16:10-13 Thus, "STATIC-CPU" signal is "an indication" of a CPU idle state, e.g., a "first state," because the CPU performs no useful work for a user (e.g., is "idle") when the clock is stopped in the "static" CPU state. Fung-929, 3:26-27, 8:1-3, 16:10-13.

Thus, when the activity monitor 16 receives Vcc asserted on the STATIC-CPU input, that is receiving an indication that the CPU is in an idle state meeting [1A].

Second, Fung-929 explains that a **"DOZE state is entered from the ON state when the activity monitor 16 has not detected activity and therefore has not**

provided the ACTIVITY signal within the time, T1, specified by the DOZE timer

63.” Fung-929, 16:2-5. In other words, “if no data transfers occur within the specified address ranges for predetermined periods of time, then a power conservation mode is entered to conserve power in the computer system.” Fung- 929, 2:60-63. One of ordinary skill would understand that this means that the CPU is in idle “when activity monitor 16 has not detected activity.” One of ordinary skill would understand that this means that the inputs to logic 77 in activity monitor 16 are indications of CPU state, because logic 77 determines CPU state (and the ACTIVITY signal) based on those inputs.

Thus, activity monitor 16 “receives an indication when the processor is in a first state” comprising an “idle” state as used in the ’809 patent. Madisetti-EPR, ¶328

(ii) Busy State

Fung-929’s activity monitor 16 also “receives an indication when the processor is in a first state” comprising a “busy” state (e.g., not “idle” state). This provides an alternative basis to meet limitation [1A].

Activity monitor 16 receives a busy indication in two ways:

First, address detector 73 in activity monitor 16 **“provides an address detect signal on line 76” when it senses signals on address lines SA(0...9) “representing the address activity of the CPU 4.” Fung-929, 17:18-28.** Here, the fact that the address detector 73 provides an address detect signal means that the address line SA(0...9) inputs evaluated by address detector 73 provide an indication that the CPU is in a busy state.

Second, **logic 77 in activity monitor 16 generates an “ACTIVITY” signal that places PMU 15 in an “ON” state based on inputs including the “address detect signal on line 76.” “The ACTIVITY output is an OR function of a programmable selection of different activities specified in the ACTMASK register 54. When active, this output returns the PMU 15 (and the computer system) to the ON state and retriggers the DOZE timeout timer 63.” Fung-929, 17:36- 40; id., 14:21-22 (“The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources.”), 15:40-46** (power management unit 15 is placed in an “ON” state “when the activity monitor 16 detects activity with addresses in the predetermined address set.”). Here the PMU state “controls the consumption of power by different parts of the computer 3.” Fung-929, 7:19-23.

‘The ON state can... be entered if the hardware monitor 79 detects a predetermined set of address ranges on [CPU] bus 5. For example, the predetermined set of address ranges monitored for power management typically includes all of the I/O address range, that is, the addresses of the I/O controllers 6-0 through 6-n, and the video memory address range for the video memory locations 8 with the memory 11. Of course, other address ranges can be added to or used as the predetermined set for power management. The set of address ranges including the video memory and the I/O address range has been found to provide excellent information for controlling power management.’

Fung-929, 10:17-28.

This passage referring to activity monitor input signals, notes that I/O, video memory, and memory address signals were indications that CPU 4 was “busy” (not idle)

because these were conventionally signals provided by a CPU when it was operating, and an idle CPU or a CPU with a stopped clock would not provide signals on these addresses. A POSITA would have understood that a signal indicating a CPU reading or writing to memory was an indication of a busy (non-idle) CPU because a CPU that is reading or writing to memory is not “idle.” Madisetti-EPR, ¶333

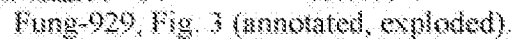
[1B] – “a counter coupled to the idle indicator and coupled to a system clock,”

As shown below, Fung-119 meets limitation [1B] because Fung-929 discloses a counter coupled to activity monitor 16 (the “idle indicator”). Fung-929 also discloses that the counter is coupled to a system clock.

Moreover, to the extent “system clock” is interpreted as limited to the same clock that the systems CPU runs on (it should not be), POSITAs had reasons to modify Fung-929’s clock distribution scheme to meet even that narrow interpretation of limitation [1B]. Madisetti-EPR, ¶335.

a) Fung-929’s timer unit 24 is coupled to the idle indicator (activity monitor 16) and is the counter in [1B].

Fung-929’s timer unit 24 is outlined in blue dashed lines in the annotated and exploded Figure 3 below. As illustrated therein, **timer unit 24 is “coupled” to the idle indicator (activity monitor 16) because it receives from activity monitor 16 the ACTIVITY, EL TRIG and LCD TRIG signals. Fung-929, Fig. 3.**



Counters are implemented using registers.

Fung-929 has an ON state the system enters anytime activity is detected. Fung-929, 7:24-35, 15:40-53. When the system enters the ON state, a DOZE timer begins running and if it expires without any activity being detected before the expiration, the system enters the DOZE state. Fung-929, 15:48-49, 16:1-5. When the system enters the DOZE state it starts a SLEEP timer running. Fung-929, 16:31-33. If the SLEEP timer expires without any activity being detected, the system enters a SLEEP state. Fung-929, 16:31-35. On entering the SLEEP state, the system starts a SUSPEND timer. Fung-929, 16:41-44. If the SUSPEND timer expires without any activity being detected, the system can enter a SUSPEND state. Fung-929, 16:41-44. If CPU activity is detected, the system returns to the ON state. Fung-929, 15:44-46 (ON state "is entered from DOZE or SLEEP when the activity monitor 16 detects activity with addresses in the predetermined address set."), 15:41-44 ("ON state is entered from the SUSPEND... when the *RESET is low, and also when one of EXT, RTC, or RI goes high...."), 16:52-54 ("[A]ctivity on the EXT, RI or RTC inputs can cause an exit from SUSPEND and the new state after exit will be ON.").

Thus, under control of the PMU, an idle CPU will cause the system to enter the DOZE state, and if the idle state persists the system will enter SLEEP, then SUSPEND state, while a busy CPU will cause the system to enter the ON state. Madisetti-EPR, ¶339.

As should be appreciated from the above, the DOZE 63, SLEEP 64, and SUSPEND 65 timers all monitor time when the CPU is in different CPU activity states

and expire after a plurality of predetermined time periods. Fung-929, 3:50-58 (“A first state, called a DOZE state, is entered after sensing inactivity by the hardware monitor for a first period of time. A second state, called a SLEEP state, is entered after sensing inactivity by the hardware monitor for a second predetermined time where the second predetermined time is greater than the first predetermined time. A third state, called a SUSPEND state, is entered after sensing inactivity by the hardware monitor for a third period of time greater than the first and second time periods”). The expiration of each of these time periods is determined by its corresponding timer. Each timer comprises registers that return a value that “was last written to it.” Fung-929, 15:15-30. The value in each of the DOZE, SLEEP, and SUSPEND timer registers corresponds to a counter value.

Fung-929’s user wait 24 (and each timer within it) is coupled to activity monitor 16 (the “idle indicator”) because the DOZE 63, SLEEP 64, LB 68, SUSPEND 65, and LCD 66 timer/registers each receive the ACTIVITY signal from activity monitor 16. Fung-929, Fig. 3. Since the timer unit 24 comprises these timers, and each timer is coupled to activity monitor 16, POSITAs understood that timer unit 24 is coupled to activity monitor 16. Madisetti-EPR, ¶341.

b) Fung-929’s timer unit 24 is “coupled to a system clock.”

(1) “system clock”

The '809 specification says a system clock “may measure ticks or cycles, or any other measure of system time, and then provide this data, or a modified form of the system time data, to the counter 140.” EX1001, 3:64-68. The '809 patent does not illustrate system clock 130 as coupled to CPU 110 (FIGs. 1A, 1C), does not say the counter’s clock must be the same clock that drives the CPU, and only says the counter value may (“e.g.”), not must, count “CPU cycles.” EX1001, 4:5-7.

POSITAs would have understood from the specification’s usage that “system clock” in limitation [1B] required only a clock that provided “a measure of system time” and was not limited to a clock that drove the CPU. Madisetti-EPR, ¶343.

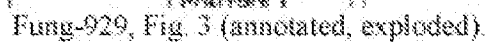
Claim 1 does not refer to “the system clock” and thus does not suggest that it is the singular clock in the system. Instead, it simply recites “a system clock.” Given that the '809 specification does not redefine the term “a system clock,” it should be given its plain meaning consistent with the specification. Phillips v. AWH Corp., 415 F.3d 1303, 1313-1314 (Fed. Cir. 2005) (en banc). The plain meaning of “a system clock” is a clock used in the system. Madisetti-EPR, ¶344.

(2) Fung-929’s oscillator 43 is a system clock.

Fung-929 discloses oscillator 43 “refresh control unit 20” that “provides the timebase for the timers” in timing unit 24 as well “the refresh for DRAM memory 11.” Fung-929, 17:44-46, Fig. 3. By providing the “timebase” for timing unit 24, its timers,

and the memory (DRAM) refresh, oscillator 43's clock signal provides a "measure of system time" and "system time data," which meets the "system clock" in limitation [1B]. This is consistent with the '809 patent specification's description of "system clock." Madisetti-EPR, ¶345.

Fung-929's oscillator 43 ("system clock") is coupled to Saver wait 28 ("counter") and the timers within it, meeting limitation [1B]. In an annotated and exploded view of Fung-929 Figure 3 (below), the highlight shows clock distribution providing a "measure of system time" from oscillator 43 to timer unit 24 and its timers/registers, including DOZE 63, SLEEP 64, and SUSPEND 65.

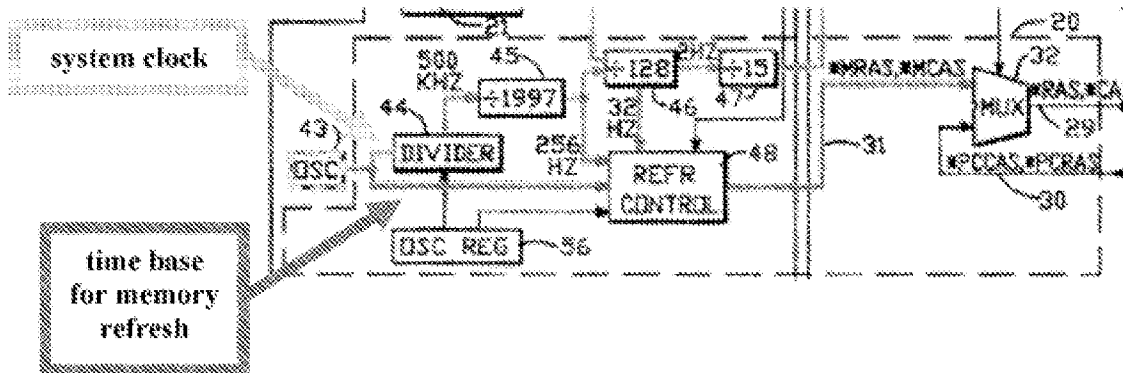


DOZE timer 63 “is triggered by the activity monitor ACTIVITY output in the ON state,” and “triggers the transition to the DOZE state when it times out.” Fung-929, 18:19-21. POSITAs understood that the ACTIVITY output triggering (or “retriggering”) the DOZE timer 63 when the system transitions “to the ON state” means that the

ACTIVITY signal resets the DOZE timer whenever CPU activity is detected. Fung-929, 16:2-5, 17:56-18:9. As a result, POSITAs understood that when the DOZE timer expires it provides a count indicative of the time the CPU was in an idle state because the activity monitor 16 resets the DOZE timer each time it detects CPU activity by asserting the ACTIVITY signal.

SLEEP timer 64 "is triggered when the DOZE state is entered and is cleared when the DOZE state is exited." Fung-929, 18:22-23. SUSPEND timer 65 "is triggered when the SLEEP state is entered and is cleared when the DOZE state is exited." Fung-929, 18:26-27. POSITAs would thus have understood that the SLEEP and SUSPEND timers in timer unit 24 count time during which a CPU was idle which kept the system in the DOZE or SLEEP state. Madisetti-EPR, ¶349.

Confirming that oscillator 43 is a system clock it is also used for providing timing to other aspects of Fung-929's system, including to generate refresh signals for the DRAM. This is shown, for example in the exploded view of Fung-929 Figure 3 below. Fung-929, 17:44-54, 19:7-9, Fig. 3.



Fung-929, Fig. 3, refresh control 20 and oscillator 43 clock distribution (annotated, exploded).

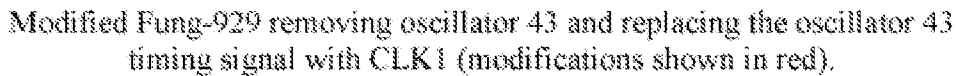
POSITAs would have understood that each use of the clock signal from oscillator 43 measure of system time for timing unit 24 and its timers/registers, and as a measure of system time for DRAM refresh—alone or in combination confirms that oscillator 43 clock signal meets the “system clock” in limitation [1B]. Madisetti-EPR, ¶351.

Fung-929 refers to a CLK1 as a “system clock oscillator signal.” Fung-929, 7:66. Fung- 929 does not explain what, if any, relationship CLK1 has to oscillator 43. Regardless, oscillator 43 clock output meets the “system clock” in limitation [1B], consistent with the way “system clock” is used in the '809 patent specification (Supra) because the claims in no way require that there be only one system clock and oscillator 43 clock output is undeniably “a system clock” — the claims require nothing more.

(3) In an alternate interpretation, if system clock is limited to a clock that drives the CPU that is met by an obvious implementation of Fung-119

As mentioned above, Fung-929 does not explain what, if any, relationship there is between the CLK1 signal the drives the CPU and oscillator 43. As explained below, a POSITA had reasons to use a single oscillator for Fung-119's computer system to drive all of its components that require a clock, including the CPU and power management unit (PMU), because this would save space and cost. Madisetti-EPR, ¶353. This could be achieved by either generating the CLK1 signal from oscillator 43 or by eliminating oscillator 43 and simply using CLK1 to be the timing reference for the PMU. Madisetti-EPR, ¶353.

For example, POSITAs had reasons to modify Fung-929 by removing crystal oscillator 43 and providing CLK1 as a frequency reference to programmable divider 44 and as a timing reference input to refresh control logic 48, with reasonable expectation of success. Madisetti-EPR, ¶354. In this straightforward variation of Fung-929, CLK1 supplies the "system clock" "coupled to" the counter in limitation [1B]. Madisetti-EPR, ¶354.



POSITAs understood that the CLK1 input to CPU Control block 49 was available as a timing reference and could provide a reference timing signal to programmable divider 44 and refresh control logic 48 instead of the clock signal from oscillator 43. Madisetti-EPR, ¶356. Fung-929 describes CLK1 as a “system clock oscillator signal” that provides a clock signal to CPU Clock Control block 49, which provides CLKOUT that “drives CPU 4.” Fung-929, 7:66- 8:2; Madisetti-EPR, ¶356.

POSITAs understood that using CLK1 instead of oscillator 43 would avoid the drawbacks associated with including a separate crystal oscillator 43, save space on the board layout, and reduce the bill of materials. Madisetti-EPR, ¶357. Thus, POSITAs would have understood that eliminating oscillator 43 and using CLK1 in place of the clock signal from oscillator 43 would have improved Fung-929. Madisetti-EPR, ¶357.

POSITAs would have reasonably expected this modification to succeed because Fung-929 describes divider 44 as programmable and was therefore not limited to a particular clock frequency from the oscillator 43 clock signal. Fung-929, 17:43-54 (“PMU 15 may be programmed to accept a range of OSC frequencies. ... The programmable counter output of divider 44 is divided....”); Madisetti-EPR, ¶358. POSITAs would have known that contemporaneous dividers could provide a 500 kHz signal (e.g., Fung-929, Fig. 3, divider 44 output) from clock signals that were provided as input to CPUs at the time of invention for the 809 patent. Madisetti-EPR, ¶358. For example, the AMD Athlon processor model 4 accepted a system clock in the range of 100 to 133 MHz and set the processor clock as a multiple of the system clock input. EX1113 (AMD Athlon Processor Model 4 Data Sheet), 28 Table 9 (specifying system clock input to CPU between 100 and 133 MHz), 37-38 (describing range of multipliers to set processor clock from input system clock), 64 (same); EX1114 (Athlon processor data sheet), 26 (“The AMD Athlon processor provides four frequency ID signals (FID[3:0]) to the system controller to indicate the SYSCLK multiplier at which the processor core operates.”), 58 (“The FID[3:0] signals are outputs to the system that report the multiplier used on the system clock (SYSCLK) producing the AMD Athlon processor core clock.”), 69 (similar);

Madisetti-EPR, ¶358. POSITAs knew that dividing 100 MHz by 200 would provide a 500 kHz signal, and achieving this time division was well-within the range of frequency dividers already disclosed in Fung-929 and otherwise known in the art. Fung-929, Fig. 3; Madisetti-EPR, ¶359.

POSITAs would have known that they could distribute CLK1 to divider 44 and refresh control logic 48 in the same manner that CLK1 was already distributed in the system. Madisetti- EPR, ¶360. Making this modification was well-within the POSITA's ordinary skill. Madisetti- EPR, ¶360.

Thus, while the '809 patent does not require the "system clock" be a clock that drives a CPU, this obvious modification to Fung-929 provides CLK1 (the clock that provides the time base for CPU Clock Control 49 and the CPU clock) as a clock signal to timing unit 24 and its timers/registers. This meets the "system clock" in limitation [1B] under any reasonable interpretation. CLK1 would then be "coupled" to the same "counter" as described above for the case that the counter is timer unit 24 (described above) or the case that the counter is the DOZE, SLEEP, and SUSPEND timers (described below).

[1B1] – "wherein the counter receives a measure of system time from the system clock and"

Each of Fung-119's timers in timing unit 24 (e.g., the DOZE, SLEEP and SUSPEND timers discussed supra)) meets limitation [1B1] and receives a measure of system time from the system clock in either of two alternative cases (case 1 or 2) as show below based on the system clock being met by oscillator 43 or CLK1.

Case	counter (limitation [1B])	system clock (limitation [1B])
1	timer unit 24 (<i>supra</i> §§XIII B 3.a)	oscillator 43 (<i>supra</i> §XIII B.3 b)(2))
2	timer unit 24 (<i>supra</i> §§XIII B 3.a)	CLK1 (<i>supra</i> §XIII B.3 b)(3))

Case 1

Fung-929's oscillator 43 provides each timer in timing unit 24 (including DOZE, SLEEP, and SUSPEND timers) with "a measure of system time" and is the "system clock" in limitation [1B])(2). DOZE 63 receives timing from oscillator 43 via dividers 44-46. Fung-929, Fig. 3. SLEEP 64 and SUSPEND 65 receive timing from oscillator 43 via dividers 44-47. Fung-929, Fig. 3. The timers receiving the oscillator 42 via a divider meets [1B1] because the '809 specification is clear that the counter need not receive the system clock directly, as it can alternatively receive "a modified form of the system time data [provided] to the counter 140." EX1001, 3:64-68.

Thus, each timer in Fung-929's timing unit 24 (including DOZE, SLEEP, and SUSPEND timers) is a counter that receives a measure of time from the system clock as required by [1B1].

Case 2

In the obvious alternative case **where CLK1 replaces oscillator 43 as the “system clock” (supra), then each of the DOZE 63, SLEEP 64, and SUSPEND 65 timers/registers within timer unit 24, would “receive[] a measure of system time” from CLK1 rather than oscillator 43. This obvious alternative implementation of Fung-929 meets limitation [1B1] for reasons similar to how it meets [1B1] with oscillator 43 2 as the “system clock.”**

[1B2] – (the counter) receives data related to the indication when the processor is in the first state, and

Claim 1 does not limit any way what the “first” state of the processor is, as is the case with later claims (see e.g., claim 2 where “the first state is a busy state”). For claim 1, the patent owner chose to broadly claim a “first state” that is not limited in any respect, so the “first state” can be any state of the processor. The first state in [1B2] is met by Fung-119 in numerous ways based on the first state being a “busy state,” an “idle state” and an inactive state where the processor does not perform any of the actions that Fung-929 monitors to determine that the processor is active.

a) Busy

Fung-119 meets limitation [1B2] because Fung-929 discloses that **activity monitor 16 provides an ACTIVITY signal to timing unit 24 and each of its DOZE,**

SLEEP, and SUSPEND timers, where the ACTIVITY signal places PMU 15 in the “ON” state and is data related to the indications that the CPU is in a busy state.

Supra / Fung-929, 10:17-28 (busy state);

b) Inactive

Fung-929’s counters treat the absence of the ACTIVITY signal at any point in time to be an indication that the CPU is not active at that point in time. Fung-929, 17:31-42. Specifically, whenever the ACTIVITY signal is received by the timing unit 24 each of the DOZE, SLEEP and SUSPEND timers is reset. Fung-929, 17:39-40 (DOZE timer) 18:19-21 (same), 18:42-43 (SLEEP timer “cleared when the DOZE state is exited”) 18:26-27 (SUSPEND timer “cleared when SLEEP is exited”). When the ACTIVITY signal is absent the DOZE timer immediately begins counting the period of inactivity, and the same is true for the SLEEP time after the DOZE timer has expired, and for the SUSPEND timer after the SLEEP timer has expired. (Supra). Thus, all of these timers count periods of time in which there is no CPU activity and thus each counts a time period when the CPU is in an inactive state. This meets [1B2] when the first state is considered to be an inactive state where the CPU is not performing any of the activities that Fung-929 monitors to generate the ACTIVITY signal.

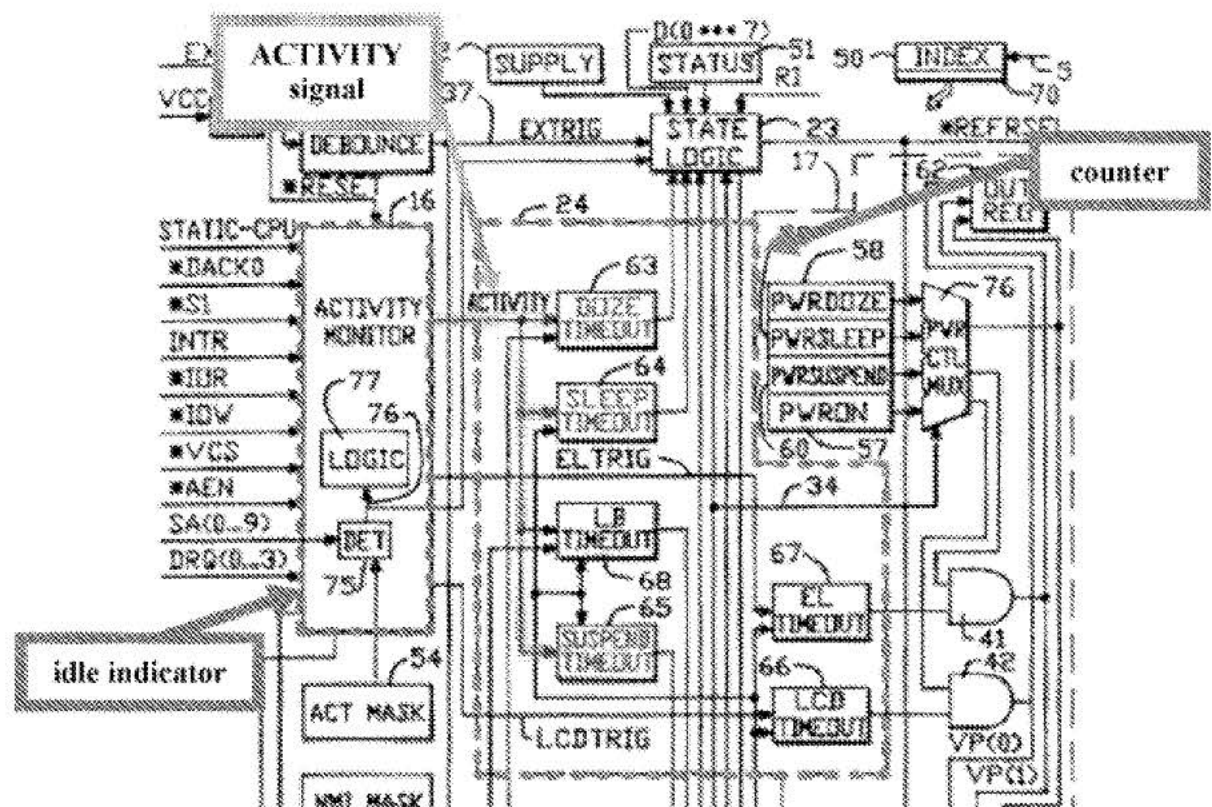
c) Idle

A POSITA would have understood that Fung-929's PMU treats the lack of CPU activity that triggers the ACTIVITY signal to be an indication that the CPU is idle. Madisetti-EPR, ¶309. Thus, the DOZE, SLEEP and SUSPEND timers each has a counter that determines a period of time that the CPU is in the idle state for the same reasons they determine how long the CPU is in an inactive state. Madisetti-EPR, ¶369.

d) Timing Unit Counters Receive the ACTIVITY Signal

Fung-929 Fig. 3 is annotated below with green highlighting showing the ACTIVITY signal path to the timers (counters) in the timing unit 24.

Logic 77 in activity monitor 16 generates an "ACTIVITY" signal that places PMU 15 in an "ON" state based on inputs including the "address detect signal on line 76." "The ACTIVITY output is an OR function of a programmable selection of different activities specified in the ACTMASK register 54. When active, this output returns the PMU 15 (and the computer system) to the ON state and retriggers the DOZE timeout timer 63." Fung-929, 17:36-40; id., 14:21-22 ("The activity monitor ACTIVITY output is the logical OR of all unmasked activity sources."), 15:40-46 (power management unit 15 is placed in an "ON" state "when the activity monitor 16 detects activity with addresses in the predetermined address set."). The PMU 15 "ON" state is associated with CPU 4 not being idle—e.g., in the '809 patent usage, with the CPU 4 being "busy."



Fung-929, Fig. 3 (annotated, exploded).

[1B3] – (the counter) “generates a counter value indicative of time the processor is in the first state, and”

Fung-119 meets limitation [1B3] based on the first state being an inactive state where the CPU performs none of the activities Fung-929 monitors to generate the ACTIVITY signal.

Fung-929 discloses that timer unit 24 and its DOZE, SLEEP and SUSPEND timers “generate[] a counter value indicative of time the processor is in the first state” wherein the first state is an inactive state where the CPU performs none of the activities Fung-919 monitors to generate the ACTIVITY signal.

In Fung-929, the DOZE, SLEEP, and SUSPEND timers count time when activity monitor 16 does not assert the ACTIVITY signal indicative of an active state. Thus, POSITAs would have understood that these timers count time when the CPU is in an inactive state.

Fung-929 explains that “[t]he DOZE timer 63 is retriggerable and is triggered by the activity monitor ACTIVITY output in the ON state[.]” Fung-929, 18:19-20; id., 15:48-49 (“Upon entering the ON state, the DOZE timeout timer 63 will be retriggered.”). POSITAs would have understood that “triggering” and “retriggering” meant resetting the timer and starting or restarting the timer count. Thus, POSITAs would have understood that the DOZE 63 timer counts an interval since last detecting CPU activity (which would have prompted a retriggering), and that this was indicative of the CPU being in an inactive state. Madisetti- EPR, ¶375.

Fung-929 explains that when the DOZE timer reaches a specified time T1, without being rest by an ACTIVITY signal indicating an active CPU, the system initiates a DOZE state. Fung-929, 16:2-5. Entering the DOZE state triggers SLEEP timer 64, which POSITAs would have understood counts time that the system remains inactive in a DOZE state. Fung-929, 16:31-33, 18:22-23. Thus, POSITAs would have understood that the SLEEP timer 64 count was an interval above specified time T1 since last detecting CPU activity (which would have prompted a retriggering), and that this was indicative of the CPU being in an inactive state. Madisetti-EPR, ¶376.

When the SLEEP timer reaches a specified time T2, without an ACTIVITY signal indicating an active CPU, the system enters a SLEEP state. Fung-929, 16:31-33. Entering the SLEEP state triggers SUSPEND timer 65. Fung-929, 18:26-27. Thus, POSITAs would have understood that the SUSPEND timer 65 count was an interval above specified times T1 and T2 since last detecting CPU activity (which would have prompted a retriggering), and that this was indicative of the CPU being in an inactive state. Madisetti-EPR, ¶377.

When SUSPEND timer 65 reaches a specified time T3, without an ACTIVITY signal indicating an active CPU, the system enters a SUSPEND state. Fung-929, 16:41-44.

Thus, POSITAs understood that the DOZE, SLEEP, and SUSPEND timers, individually and in combination, provided counts indicative of time the CPU was in an inactive state. This meets [1B3] when the “first” state is an inactive state. Madisetti-EPR, ¶379.

[1C] – “a data usage provider coupled to the counter, wherein the data usage provider is capable of providing the counter value.”

Fung-119 meets limitation [1C] as shown below.

a) “data usage provider”

As explained supra, the “data usage provider” is “capable of providing the counter value” (limitation [1C]). The only structural limitation in [1C] is that the “data usage provider” is “coupled to the counter” (limitation [1C]), whereas claim 9 further requires “an interface coupling the data usage provider to an external network” (claim 9). The specification describes a “usage data provider” as “capable of providing the counter value” (EX1001, 1:59-61). In some embodiments, “[t]he usage data provider 150 tracks the counter value and maintains a non-volatile master copy of the counter value,” EX1001, 4:12-14, while in another embodiment “[t]he usage data provider 150 maintains a connection, or network interface 160 to a system or network (not shown) that is external to the computer system 100” (EX1001, 4:24-26, dependent claim 9) and “can provide the current value of the counter value to the network by way of the network interface 160” (EX1001, 4:31-33). Nothing in the ’809 patent or its prosecution history limits the plain meaning of the “data usage provider,” which need only be coupled to the counter and “capable of providing the counter value.”

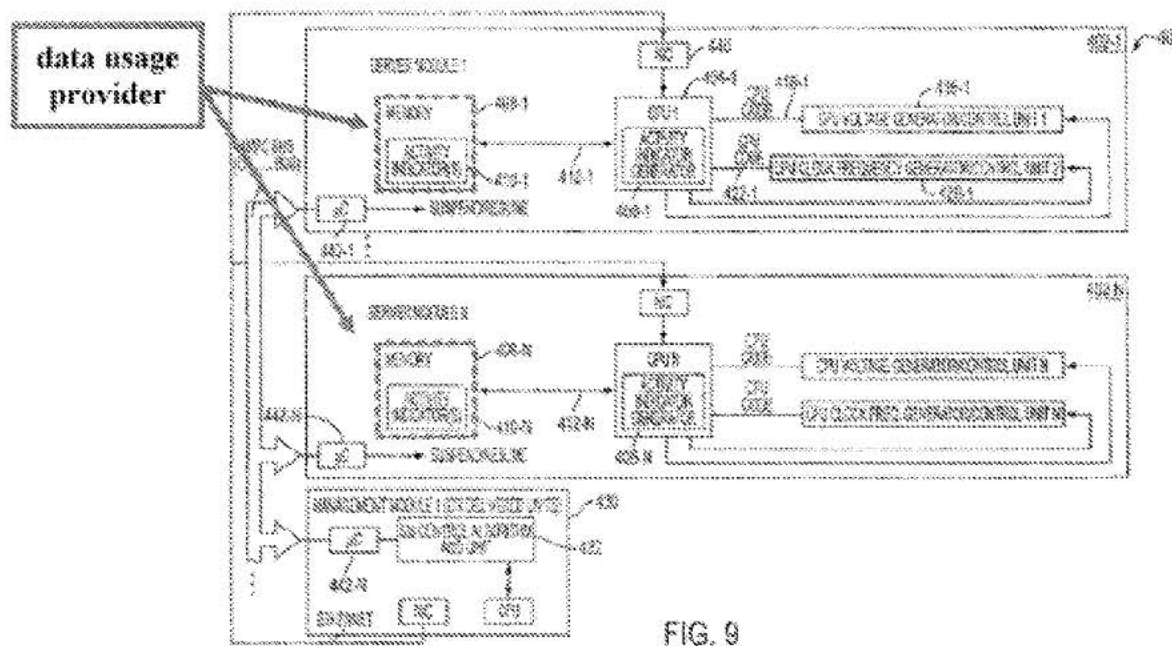
b) Fung-119’s memory 408 is a “data usage provider.”

(1) data usage provider coupled to the counter

[1C1] – **a data usage provider coupled to the counter, wherein the data usage provider is capable of providing the counter value**

Fung-119 meets limitation [1C] because it describes workload and power management in a multi-processor server environment comprising “at least two”

server modules 402-1 to 402-N (Fung-119, 19:40-42) and a management module 430 (Fung-119, 19:43-49). Fung-119, Fig. 9. Server modules include CPU 404 and memory 408. Fung-119, 19:40-43, Fig. 9. Fung-119 memory 408 is a “data usage provider” meeting limitation [1C] because as explained below it is: (1) coupled to the counter (e.g., Fung-929 timer unit 24 and the BUSY, DOZE, SLEEP, or SUSPEND timers within it, supra (limitation [1B]), and (2) “capable of providing the counter value” to the management module for power and workload management.



Fung-119, Fig. 9 (annotated).

(2) capable of providing the counter value

[1C2] – a data usage provider coupled to the counter, wherein the data usage provider is capable of providing the counter value

Fung-119's server module 408 includes an "activity indicator generator" 406 that "generates activity indicators." The activity indicator generator stores the indicators in memory 408. Fung-119, 19:43-46. Fung-119 explains that "[t]he activity level of the CPU is monitored." Fung-119, 21:16-17. Fung-929 is incorporated in Fung-119 (Fung-119, 48 :30-37) and discloses a system for monitoring CPU activity.

Thus, POSITAs understood that Fung-119 discloses using the system in Fung-929 (described as meeting limitations [1PRE]-[1B3], supra) to perform CPU monitoring information and to provide monitoring information to the activity indicator generator 406 in each server module. Indeed, a purpose of Fung-119 is to "extend[] earlier power management systems, architectures, and methods" — including Fung-929's — "to multi-server or multi-node architectures." Fung-119, 48:30-37. Madisetti-EPR, 9384. POSITAs would have understood that **Fung-929's timer unit 24 (and its DOZE, SLEEP, and SUSPEND timers) provides "activity indicators" to the activity indicator generator 406 because Fung-119 is concerned with CPU utilization (Fung-119, 29:63-30:32) and those counter values provide data on CPU utilization by indicating timer periods when the CPU is inactive. Supra; see also EX1001, 3:37-38 ("CPU utilization may be a counter value"), 4:30-31 (counter values can "indicate CPU utilization"), 8:58-59 claim 18 ("a counter value indicative of CPU utilization"); Madisetti-EPR, ¶385.**

Therefore, POSITAs understood that Fung-119 discloses storing the Fung-929 timer unit 24 timer values (e.g., the counter in limitation [1B]) as “activity indicators” in each respective server module memory 408. Madisetti-EPR, ¶386.

Furthermore, Fung-119 explains that the “activity indicator(s) are used by the management module to determine the loading [e.g., CPU utilization] on each of the server modules individually and as a group,” and “activity information or indicators created on any one computer or device (such as a server module) is accessible to a manager or supervisor via standard networking protocol.” Fung-119, 19:51-58; id., 20:29-31 (“[T]he activity indicators may be retrieved from... memory 408 via NIC 440 as is known in the art.”), 20:40-41 (“the server modules may be monitored for activity and controlled globally to reduce power consumption”), 34:47-50 (server module designated as manager given software “for receiving activity information from the server modules”), 35:4-5 (“the server modules each detect and report their activity to the manager”). POSITAs would have understood that this means memory 408 is “capable of providing the counter value” to the management module, which meets limitation [1C]. Madisetti-EPR, ¶387.

Fung-119 discloses storing the timer values from Fung-929’s in Fung-119’s activity indicator generator because it discloses using and extending Fung-929’s circuit for Fung-119’s power load management and workload management. To the extent Fung-119 does not expressly disclose storing the timer values from Fung-929’s in Fung-

119's activity indicator generator, that would have been an obvious way to implement Fung-119's multi-processor system.

Fung-119 says it is extending Fung-929 to "multi-server or multi-node architectures" and Fung-929 provides CPU activity monitoring as explained above for limitations [1PRE] to [1B3]. The timers in Fung-929's timer unit 24 provide data on CPU utilization (i.e., when the CPU is active and when it is not) as explained above, and a POSITA would have understood that this is the type of data Fung-119 uses for workload and power management in its multi-server architecture. Madisetti-EPR, ¶389. POSITAs would have reasonably expected success in storing the data from Fung-929's timer unit 24 in Fung-119's data structure 410 (in memory 408) that stores activity indicator information (Fung-119, 19:43-46) because doing so merely stores data in memory and uses known methods and components for their intended use with predictable results. Madisetti-EPR, ¶389.

[8] - The device of claim 1, wherein the usage data provider polls the counter to obtain the counter value,

Fung-119 does not expressly describe how activity indicator information is stored in memory 408 (e.g., the usage data provider), whether that data comes from Fung-929's timer unit 24 or elsewhere.

It was well-known in the computer art that a data transfer from a data producer to a data consumer can be initiated by the producer ("pushed") or consumer ("pulled"), and

that “polling” may involve the consumer pulling the data periodically. Madisetti-EPR, ¶391 (citing EX1044, 2:1 (describing “polling” in which a “client sends a request” to pull data). Polling had been used for monitoring CPUs and utilization data thereof. Madisetti-EPR, ¶391, citing EX1045, 5:33-51 (a gateway “periodically poll[s] the network resources ... to retrieve status information” including detecting when “CPU utilization” reaches a threshold), 15:28-47, 16:61-17:5; EX1046, 1:12-20 (monitoring “computer resources in a network” by sending “requests for information ... to these resources at regular intervals” which is known “as a cyclic polling, or “poll”).

It would have been an obvious design choice to implement Fung-119’s system to have server module memory 408 (the data usage provider) use well-known polling techniques to poll the timer unit 24 (and its counters DOZE, SLEEP, and SUSPEND) to pull the CPU activity data for storage. Madisetti-EPR, ¶392. This was among “a finite number of identified, predictable solutions” for meeting the design need of transferring data from timer unit 24 to the data usage provider (memory 408) with a reasonable expectation of success. KSR, 550 U.S. at 421; Madisetti-EPR, ¶392. Thus, Fung-119 renders obvious claim 8. Madisetti-EPR, ¶393.

[9] - The device of claim 1, further comprising an interface coupling the data usage provider to an external network, the interface used for providing processor utilization data to the external network.

Fung-119 meets the additional limitations in claim 9 because Fung-119 discloses a network interface card (NIC) 440 in each server module coupling the management module to the memory 408 which is the “data usage provider” as explained for limitation [1C]. Supra; Fung-119, 18:64-19:3 (servers have “a network communication card or circuit for communicating the data to the outside world”), 20:27-31 (“Activity monitoring of individual Server Modules 402 is desirably based on the standard network protocol, such as for example SNMP. Therefore the activity indicators may be retrieved from the CPU 406 or memory 408 via NIC 440 as is known in the art.”); Madisetti-EPR, ¶394. NIC 440 is an interface coupling the memory 408 (data usage provider) to an external network and provides the processor utilization data in the memory 408 to the external network. Fung-119, 20:27-31; Madisetti-EPR, ¶394. Thus, Fung-119 anticipates and/or renders obvious claim 9. Madisetti-EPR, ¶395.

[10] - The device of claim 1, further comprising a plurality of processors, each of the plurality of processors having an associated idle indicator and an associated counter, whereby the associated idle indicator and the associated counter combine to provide a counter value for their respective processor.

Fung-119 meets the additional limitations in claim 10 because Fung-119 discloses a plurality of server modules, each having at least one processor, so Fung-119 discloses a plurality of processors. Fung-119, Fig. 1 (server modules [“SM”] 54), Fig. 2 (same), Fig. 9 (server module 402-1 to 402-N with CPU 404-1 to 404-N), 19:37-43. Each server module processor has an associated idle indicator (Fung-929 activity

119, Fig. 9.



Fung-119, Fig. 9 (annotated).

¶398. Thus, Fung-119 anticipates and/or renders obvious claim 10. Madisetti-EPR,

[12] - The device of claim 10, wherein the plurality of processors are arranged in one or more cells.

Fung-119 meets claim 10 as shown supra. Fung-119 meets the additional limitations in claim 12 because POSITAs would have understood that Fung-119's server modules are each a "cell" as used in claim 12. Compare EX1001, Fig. 3 (cells 200, 300, 400) with Fung-119, Fig. 9 (server modules 402-1 to 402-N) and Fig. 1 (server module ("SM") 54); Fung-119, 5:36-49, 5:64-66 (discussing figure 1), 19:36-49 (discussing figure 9). Thus, the plurality of processors Fung-119 discloses are arranged in one or more server modules which are one or more cells as claimed. Fung-119, Figs. 1, 9., Fung-119 anticipates and/or renders obvious claim 12. Madisetti-EPR, ¶404.

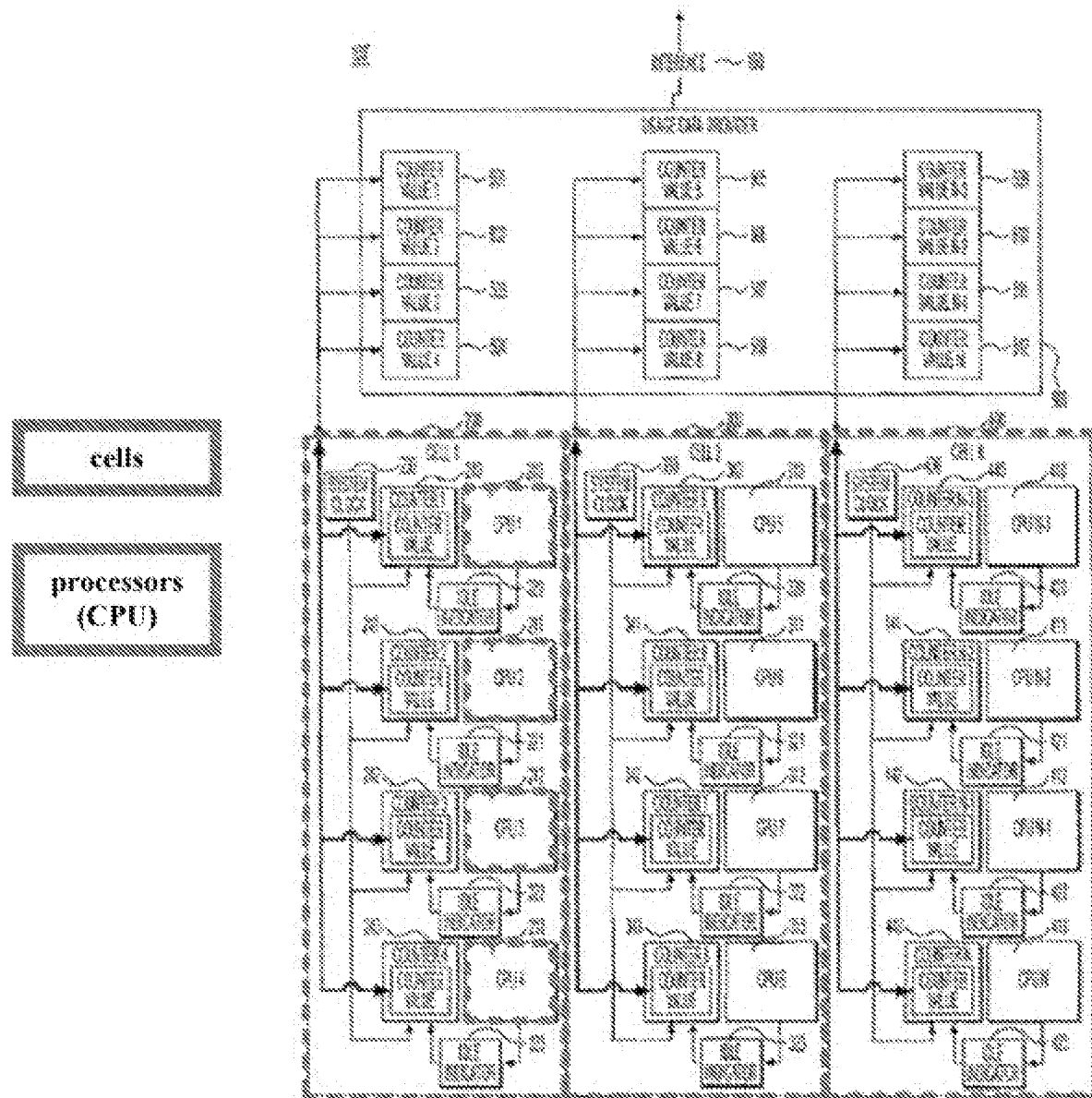
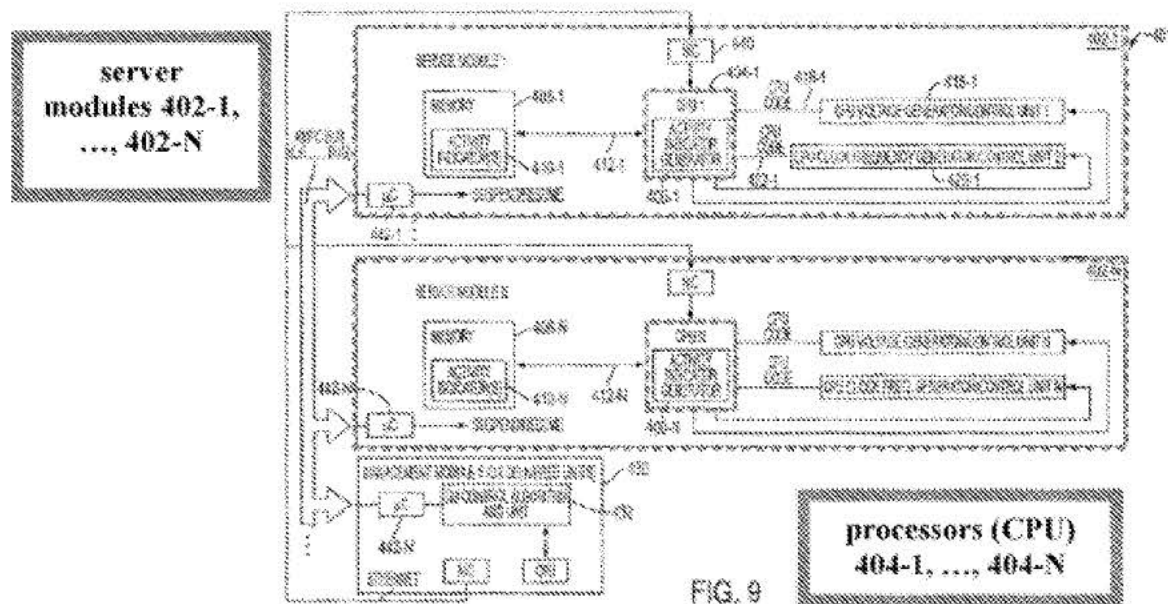
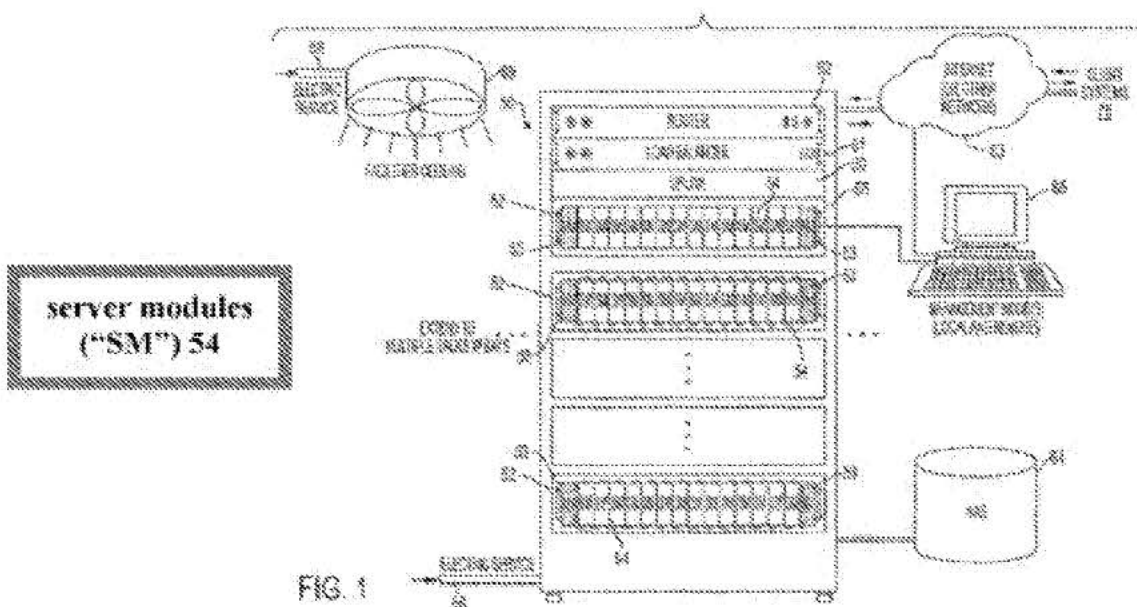


FIG. 3

'809 patent, Fig. 3 (annotated)



Fung-119, Fig. 9 (annotated).



Fung-119, Fig. 1 (annotated).

Claim 6 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Fung (U.S. Patent No. 7,032,119) in further view of Bohac (U.S. Patent No. 6,166,984).

[6] - The device of claim 1, wherein when the processor is powered on, the counter receives a current value of the counter value.

As was well-known, “volatile” storage (e.g., main memory, registers) loses stored data if power is lost, whereas “non-volatile” storage (e.g., hard drive, flash drive) does not. Madisetti-EPR, ¶152 (citing EX1031, [0022]), 451. Counters are well-known to have registers, and it was well-known to provide non-volatile storage to ensure the values in counters and other registers survive “a loss of power situation.” Madisetti-EPR, ¶451.

POSITA had reasons to use Bohac’s non-volatile counters to implement Fung-929’s timers including the BUSY, DOZE, SLEEP, and SUSPEND timers (“Fung-119+Bohac”) because this would have allowed Fung-119 to obtain CPU utilization data that spanned a power interruption to Fung-929’s timer unit 24 and its timers. Madisetti-EPR, ¶452. This would ensure the counter values are retained during power interruption (supra) and thereby allow Fung-119’s system to measure CPU utilization spanning a

power interruption. Madisetti-EPR, ¶452. Using a non-volatile counter to implement Fung-929's timers/registers would have been nothing but applying a known technique (non-volatile counters) to a known device (Fung-929's timers) ready for improvement to yield predictable results (preserve counter values spanning power interruption). KSR, 550 U.S. at 415-21; Madisetti-EPR, ¶452.

Fung-119+Bohac meets claim 1 for the reasons Fung-119 meets claim 1 as shown supra.

Fung-119+Bohac meets the additional limitations in claim 6 as follows.

The '809 patent says the usage data provider "maintains a non-volatile copy of the counter value" that is "an up-to-date, or nearly-up-to-date value of the counter value," and when the CPU is powered on, "the saved non-volatile counter value is provided ... to the counter 140 to initialize the counter value." EX1001, 4:14-23. This is the only counter value described as existing before the system is "powered on," so the "current value of the counter value" (claim 6).

Claim 6 claims the operation of a non-volatile counter precisely as Bohac describes—"[n]on-volatile counters ... consist of a volatile counter that transfer[s] its contents to a non-volatile register prior to power being removed. When power is restored, the contents of the non-volatile register ... are transferred back into the volatile counter." Bohac, 1:11-21. Thus, Fung-119+Bohac meets claim 6 ("when the processor is powered on, the counter receives a current value of the counter value") Madisetti-EPR, ¶457.

Claims 7 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Fung (U.S. Patent No. 7,032,119) in further view of Agarwal (U.S. Publication No. 2002/0133728).

[7] - The device of claim 1, wherein the counter provides the counter value to the data usage provider on a periodic basis.

Claim 7 relates generally to providing the counter value to the data usage provider periodically. Claim 7 depends on claim 1 and the counter is Fung-929 timing unit 24. Supra (limitation [1B]).

Like Fung-119, Agarwal relates to power management in a computer system. Agarwal, [0036]-[0037]. Agarwal monitors data flow through a network and adaptively controls cooling and ventilation requirements based on the amount of network traffic. Agarwal, [0018]. Agarwal discloses a “power management processor [that] can check the data traffic intensity at periodic intervals.” Agarwal, [0036]. A “traffic intensity value is stored in [a] register” and “is communicated to power management processor as the control data... . This 8-bit value can be transferred to power management processor on a periodic basis[.]” Agarwal, [0037]. Agarwal confirms that POSITAs knew it was conventional to monitor system utilization and communicate that information on a

periodic basis to a processor responsible for implementing power management functionality (e.g., the power management processor). Madisetti-EPR, ¶460.

Fung-119 does not describe details about how often timer unit 24 and its timers (the claimed “counter,” supra (limitation [1B])) provide counter value data to memory 408 (the claimed “data usage provider,” supra (limitation [1C])) and thus does not expressly disclose that this occurs “on a periodic basis.” Madisetti-EPR, ¶461. The same is true of the BUSY counter.

However, POSITAs would have understood that it would have been conventional to provide such values on a periodic basis because Agarwal discloses a register sending network traffic intensity to a management processor on a periodic basis. Madisetti-EPR, ¶462. POSITAs would have had reasons to do this because Fung-119 employs some technique for updating each server module 408 with the counter values, and Agarwal’s method was one of a limited number of ways to update memory 408 with counter values. Madisetti-EPR, ¶462. It would have been an obvious design choice to update the memory 408 on a periodic basis. Madisetti-EPR, ¶462. Furthermore, POSITAs would have known that periodically sending counter values to memory 408 would reduce bandwidth requirements as compared to continuously updating memory 408, and that the periodicity of sending counter values could have been adjusted commensurate with the desired responsiveness of the Fung-119 power management system to changes in CPU utilization. Supra; Madisetti-EPR, ¶462.

For claim 7, POSITAs would have had a reasonable expectation of success in having timing unit 24 and its DOZE, SLEEP, and SUSPEND timers send values

periodically to memory 408 in each server module because this was a simple and straightforward implementation like the one taught in Agarwal which periodically updated a management processor with register values reflecting network traffic intensity. Madisetti-EPR, ¶463.

This combination of Fung-119 using Agarwal's teaching of sending data from a register on a periodic basis is Fung-119+Agarwal. Madisetti-EPR, 7465.

Fung-119 meets claim 1 as shown supra. Fung-119 memory 408 on each server module is the data usage provider as explained supra (limitation [1C]).

Fung-119+Agarwal meets the additional requirements in claim 7 because the counter value (from timer unit 24 and its counters) is provided to the data usage provider (memory 408) on a periodic basis. Supra. Thus, Fung-119+Agarwal renders obvious claim 7.

Reasons for Confirmation

The following is an Examiner's statement of reasons for patentability and/or confirmation of claims found patentable in this reexamination proceeding.

Typically, the primary source of prior art in an ex parte reexamination will be the patents and printed publications cited in the request for ex parte reexamination. MPEP § 2256. The Examiner had previously applied Fung (U.S. Patent No. 7,032,119) / Fung-119 which incorporates by reference Fung (U.S. Patent No: 5,710,929) / Fung-929

when rejecting claims 2-5, 11, and 13-17 of the Reexamination. Below the Examiner shows where the applied references are deficient in covering the limitations of the noted claims.

Claims 2-5 and 13-17:

Specifically, while the Request and associated references do show using a BUSY indication to reset timers, neither the Request nor the references adequately show an embodiment where the Fung reference uses a BUSY state indication to “generate a counter value indicative of time the processor is in the first (busy) state” / “incrementing a counter value in the counter based on the provided busy indication”. It’s for these reasons that the Examiner doesn’t believe the rejection can be sustained.

Claim 11:

Specifically, neither the Request nor the references show a common storage element for storing a “non-volatile counter value for each of the plurality of processors”.

It’s for these reasons that the Examiner doesn’t believe the rejection can be sustained.

Accordingly, Fung-119 / Fung-929 have been shown to not sufficiently cover the claim limitations of claims 2-5, 11, and 13-17. With regard to the remaining art, no sustainable rejection has been proposed for the subject matter of claims 2-5, 11, and 13-17.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Claims 2-5, 11, and 13-17 are confirmed.

Response to Arguments

Patent Owner's arguments filed 7/3/2025 have been fully considered. Some of the arguments are persuasive, accordingly those claims are confirmed, while others remain rejected with their corresponding arguments answered below.

I.

Patent Owner argues **"to the extend the Office action relies on FUNG-929's oscillator 43 (either as-is or replaced by CLK1) as the claimed system clock, Fung-929 does not suggest any alleged counter that receives the output of the oscillator 43"**.

In response, the Examiner respectfully submits that as mentioned in the Non-Final office action Fung-929 is explicit about the oscillator (OSC) providing "the timebase for the timers" (17:44-46), where an oscillator to one of ordinary skill in the art is a known clock signal generation circuit element. Therefore the timers (claimed counter) receives the output of the OSC (claimed system clock).

The specific claim language surrounding argued element is “a system clock”, in other words, a clock within the system, which the OSC clearly meets. The '809 specification says a system clock “may measure ticks or cycles, or any other measure of system time, and then provide this data, or a modified form of the system time data, to the counter 140.” EX1001, 3:64-68. The '809 patent does not illustrate system clock 130 as coupled to CPU 110 (FIGs. 1A, 1C), does not say the counter's clock must be the same clock that drives the CPU, and only says the counter value may (“e.g.”), not must, count “CPU cycles.” EX1001, 4:5-7.

Therefore a person of ordinary skill in the art would have understood from the specification's usage that “system clock” in limitation [1B] required only a clock that provided “a measure of system time” and was not limited to a clock that drove the CPU. Madisetti-EPR, ¶343.

With regard to **arguments directed a use of the CPU clock being utilized**, the Examiner believes the claims are not so narrowly worded so as to require this specific system clock. But nevertheless, the reference discloses a CPU clock could easily be substituted in place of the OSC with little to no change in the Fung system, while providing predictable results.

Patent Owner argues **“Fung-929 does not teach that its DOZE, SLEEP, and SUSPEND timers are counters — Fung-929 uses the word “timer” to describe DOZE, SLEEP, and SUSPEND because they provide a preset trigger, not that they count or track time.”**

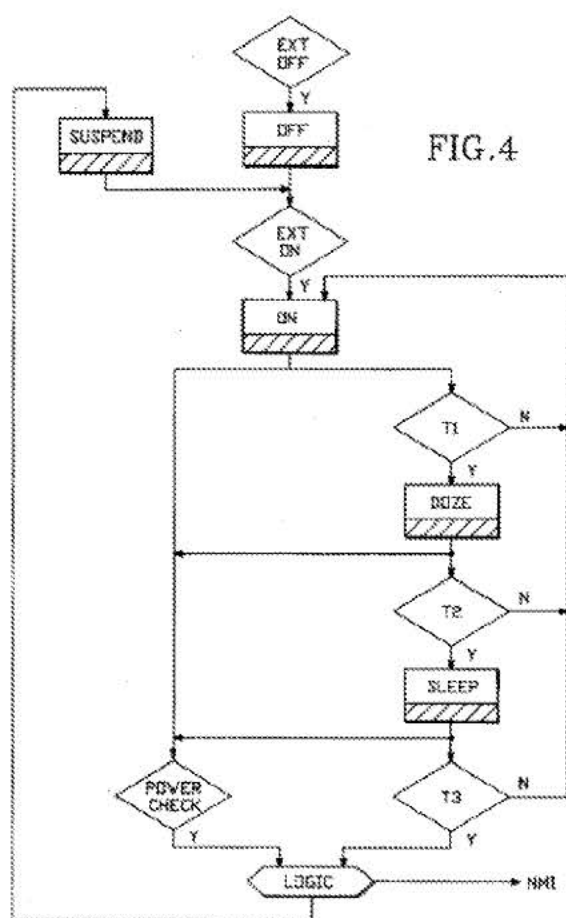
In response, the Examiner respectfully submits that argument that “timers” don’t “count or track time” is not supported by the evidence nor meaning of the terms in the art. The DOZE, SLEEP, and SUSPEND timers receive input from the Activity Monitor to “control the transitions between state in the state control unit 23 as shown in the state diagram of FIG. 4.”

A timer can be a timer that counts up from a starting value or that counts down from a starting value. Madisetti-EPR, ¶337. Either meets the claims limitation counting in a specified direction occurs.

Fung’s state transition is shown in figure 4 of Fung-929 and further outlined below:

Fung-929 has an ON state the system enters anytime activity is detected. Fung-929, 7:24-35, 15:40-53. When the system enters the ON state, a DOZE timer begins running and if it expires without any activity being detected before the expiration, the system enters the DOZE state. Fung-929, 15:48-49, 16:1-5. When the system enters the DOZE state it starts a SLEEP timer running. Fung-929, 16:31-33. If the SLEEP timer expires without any activity being detected, the system enters a SLEEP state. Fung-929, 16:31-35. On entering the SLEEP state, the system starts a SUSPEND

timer. Fung-929, 16:41-44. If the SUSPEND timer expires without any activity being detected, the system can enter a SUSPEND state. Fung-929, 16:41-44. If CPU activity is detected, the system returns to the ON state. Fung-929, 15:44-46 (ON state "is entered from DOZE or SLEEP when the activity monitor 16 detects activity with addresses in the predetermined address set."), 15:41-44 ("ON state is entered from the SUSPEND... when the *RESET is low, and also when one of EXT, RTC, or RI goes high...."), 16:52-54 ("[A]ctivity on the EXT, RI or RTC inputs can cause an exit from SUSPEND and the new state after exit will be ON.").



Patent Owner argues that **“Fung-929 teaches that the CPU sets the value of a timer register to 0 to disable that timer. But if the value of the timer register is set to 0 by the CPU, then that value cannot be “generate[d] indicative of time the processor is in the first state’ as claimed. The value of 0 is not “generat[ed]” by the counter — Fung-929 instead teaches that it is provided by the CPU. And the value of 0 is not “indicative of time the processor is in the first state’ — Fung-929 instead teaches that the value of 0 disables the timer.”**

...

“Fung-929’s timer registers cannot provide an indication of how much time has elapsed since entering the appropriate state. In other words, Fung-929’s fixed value timer registers cannot “generate[] a counter value indicative of time the processor is in the first state” as claimed.”

In response, Examiner respectfully submits that timers have both a programable duration (ex. 1-15 sec for the DOZE timer) and a current value / counter value (current time CPU is in a current state / into a timer duration).

The programable duration is described as the T1 / T2 / T3 duration in Fung-929:

- DOZE State

The DOZE state is entered from the ON state when the activity monitor 16 has not detected activity and therefore has not provided the ACTIVITY signal within the time, T1, specified by the DOZE timer 63.

- SLEEP State

The SLEEP state is entered when the PMU 15 has been in the DOZE state for the time, T2, specified by the SLEEP timer 64 and no ACTIVITY signal has occurred.

- SUSPEND State

The SUSPEND state is entered when the PMU 15 has been in the SLEEP state for the time, T3, specified by the SUSPEND timer 65 or when a power check detects low battery signals, LB or LLB.

The current value / counter value / counted time is described in Fung-929:

- Fung-929 explains that “[t]he DOZE timer 63 is retriggerable and is triggered by the activity monitor ACTIVITY output in the ON state[.]” Fung-929, 18:19-20; id., 15:48-49 (“Upon entering the ON state, the DOZE timeout timer 63 will be retriggered.”). (the SLEEP and SUSPEND timers are similarly described)

- In Fung-929, the DOZE, SLEEP, and SUSPEND timers count time when activity monitor 16 does not assert the ACTIVITY signal indicative of an active state. Thus, POSITAs would have understood that these timers count time when the CPU is in an inactive state.

POSITAs would have understood that “triggering” and “retriggering” meant resetting the timer and starting or restarting the timer count. Thus,

POSITAs would have understood that the DOZE 63 timer counts an interval since last detecting CPU activity (which would have prompted a retriggering), and that this was indicative of the CPU being in an inactive state. Madisetti- EPR, ¶375.

II.

Arguments persuasive. Claims confirmed.

While the Request and associated references do show using a BUSY indication to reset timers, neither the Request nor the references adequately show an embodiment where the Fung references uses a BUSY state indication to “generate a counter value indicative of time the processor is in the first (busy) state” / “incrementing a counter value in the counter based on the provided busy indication”.

III.

Arguments moot given dependence on confirmed claims.

IV.

Arguments persuasive. Claim confirmed.

Neither the Request nor the references show a common storage element for storing a “non-volatile counter value for each of the plurality of processors”.

Summary

Claims 1, 6-10, and 12 are hereby **REJECTED**.

Claims 2-5, 11, and 13-17 are **CONFIRMED**.

Claims 18-20 are **not subject to reexamination**.

Conclusion

THIS ACTION IS MADE FINAL.

A shortened statutory period for response to this action is set to expire 2 months from the mailing date of this action.

Extensions of time under 37 CFR 1.136(a) do not apply in reexamination proceedings. The provisions of 37 CFR 1.136 apply only to “an applicant” and not to parties in a reexamination proceeding. Further, in 35 U.S.C. 305 and in 37 CFR 1.550(a), it is required that reexamination proceedings “will be conducted with special dispatch within the Office.”

Extensions of time in reexamination proceedings are provided for in 37 CFR 1.550(c). A request for extension of time must specify the requested period of extension and it must be accompanied by the petition fee set forth in 37 CFR 1.17(g). Any request for an extension in a third party requested ex parte reexamination must be filed on or before the day on which action by the patent owner is due, and the mere filing of a request will not affect any extension of time. A request for an extension of time in a third party requested ex parte reexamination will be granted only for sufficient

cause, and for a reasonable time specified. Any request for extension in a patent owner requested ex parte reexamination (including reexamination ordered under 35 U.S.C. 257) for up to two months from the time period set in the Office action must be filed no later than two months from the expiration of the time period set in the Office action. A request for an extension in a patent owner requested ex parte reexamination for more than two months from the time period set in the Office action must be filed on or before the day on which action by the patent owner is due, and the mere filing of a request for an extension for more than two months will not affect the extension. The time for taking action in a patent owner requested ex parte reexamination will not be extended for more than two months from the time period set in the Office action in the absence of sufficient cause or for more than a reasonable time.

The filing of a timely first response to this final rejection will be construed as including a request to extend the shortened statutory period for an additional two months. In no event, however, will the statutory period for response expire later than SIX MONTHS from the mailing date of the final action. See MPEP § 2265.

The Patent Owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the patent throughout the course of this reexamination proceeding. The requester is also reminded of the ability to similarly appraise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282, and 2286.

All correspondence relating to this ex parte reexamination proceeding should be directed:

Electronically: Registered users may submit via Patent Center at
<https://patentcenter.uspto.gov/>.

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Knox Building
501 Dulany Street
Alexandria, VA 22314

For electronic transmissions, 37 CFR 1.8(a)(1)(i)(C) and (ii) states that correspondence (except for a request for reexamination and a corrected or replacement request for reexamination) will be considered timely filed if (a) it is transmitted via the USPTO patent electronic filing system in accordance with 37 CFR 1.6(a)(4), and (b) includes a certificate of transmission for each piece of correspondence stating the date of transmission, which is prior to the expiration of the set period of time in the Office action.

Any inquiry concerning this communication should be directed to Central Reexamination Unit at telephone number (571) 272-7705.

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