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Paper 9
Entered: January 3, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,
Petitioner,
v.

VALTRUS INNOVATIONS LIMITED,
Patent Owner.

IPR2022-01197
Patent 6,816,809 B2

Before JEFFREY W. ABRAHAM, KEVIN C. TROCK, and SHELDON M. McGEE, *Administrative Patent Judges*.

McGEE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. §§ 314, 325(d)

I. INTRODUCTION

Petitioner filed a Petition (Paper 2, "Pet.") for institution of an *inter partes* review of claims 1–17 of U.S. Patent No. 6,816,809 B2 (Ex. 1001, "the '809 patent").

Patent Owner filed a Preliminary Response (Paper 6, "Prelim. Resp."). The parties identify a district court action as a related matter: *Valtrus Innovations, Ltd. v. Google LLC*, No. 3:22-cv-00066-N (N.D. Tex). Pet. xi; Paper 5, 1.

Petitioner requested authorization to file a Reply to the Preliminary Response (Ex. 3001) and after a conference call was held with the parties on November 8, 2022,[1] the Board denied that request for failure to demonstrate good cause. Paper 7.

II. BACKGROUND

A. The '809 Patent (Ex. 1001)

The '809 patent relates to "pay-per-use systems and methods that use central processor metering to determine processor utilization for billing and other purposes." Ex. 1001, 1:6–8. The '809 patent discloses that "metering of processor utilization is currently accomplished by software running within the computer system's operating system," but that if the computer system has "hardware that may be partitioned, gathering processor utilization data from a hardware system requires communications between the metering application and all operating systems running within the hardware." *Id.* at 1:15–22. The '809 patent teaches that it is challenging to meter processor

[1] Petitioner filed a transcript of that conference call. Ex. 1052.

utilization in partitioned hardware because operating systems are separated and, thus, "do not have visibility to utilization data from other operating systems," and because those partitioned systems may lack a network connection between them. *Id.* at 1:23–30.

The '809 patent proposes a solution to these challenges by disclosing "a hardware based utilization metering device" and "a hardware based method for measuring processor utilization in a computer system." *Id.* at 1:49–2:4. "The apparatus and method assume that a [central processor unit, 'CPU'] may be in a first state or in a second state," and "[t]he CPU utilization may be based on a measure of time that the CPU spends in one state or the other." *Id.* at 3:19–23. One of those states may be a "busy" state where the CPU is running a process or performing useful work, where the other is an "idle" state where the CPU is not running or otherwise performing useful work. *Id.* at 3:23–27.

Figure 1A of the '809 patent, reproduced below, is illustrative:

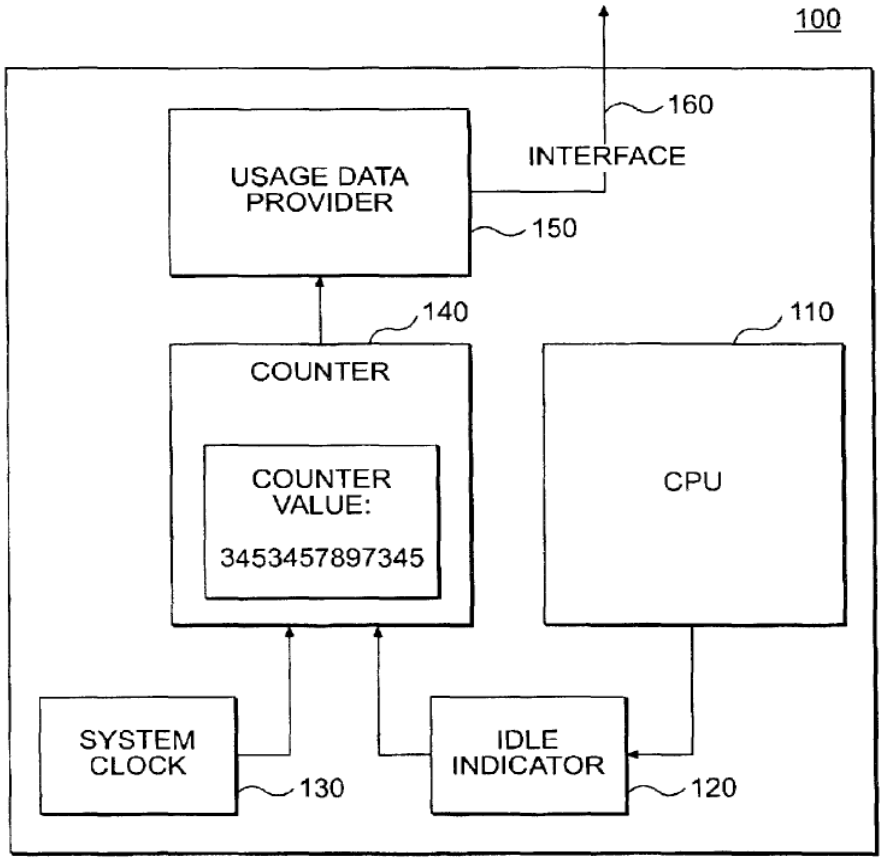


FIG. 1A

Figure 1A depicts "a basic block diagram of a computer system 100 that implements hardware based utilization metering," and includes CPU 110 with idle indicator 120 coupled thereto, counter 140, and system clock 130. Ex. 1001, 3:50–64. "The output of the idle indicator 120 is provided to a counter 140," which "also receives an output from a system clock 130." *Id.* at 3:61–64.

> Using the inputs from the system clock 130 and the idle indicator 120, the counter 140 measures CPU cycles for the CPU 110, where the CPU 110 is not in an idle state, but instead is performing a service for the user of the system 100. While the CPU 110 is powered on, the counter 140 may thus maintain a counter value as shown in FIG. 1A, with the counter value (e.g.,

> CPU cycles) updated based on the system time data and the idle indicator output.

Ex. 1001, 4:1–8.

B. Challenged Claims

We reproduce below independent claims 1 and 13 which illustrate the '809 patent's subject matter that is challenged in this proceeding:

> 1. A hardware based utilization metering device, comprising:
>
> an idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state;
>
> a counter coupled to the idle indicator and coupled to a system clock, wherein the counter receives a measure of system time from the system clock and receives data related to the indication when the processor is in the first state, and generates a counter value indicative of time the processor is in the first state; and
>
> a data usage provider coupled to the counter, wherein the data usage provider is capable of providing the counter value.
>
> 13. A hardware based method for measuring processor utilization in a computer system comprising a plurality of processors, the method comprising:
>
> determining when any of the plurality of processors is busy;
>
> providing a busy indication to a counter associated with a busy processor;
>
> receiving at the counter a measure of computer system time;
>
> incrementing a counter value in the counter based on the provided busy indication and an amount of computer system time that the processor is determined to be busy; and
>
> maintaining the counter value.

Ex. 1001, 7:30–43, 8:14–28.

C. Grounds of Unpatentability Asserted in the Petition

Petitioner advances several grounds of unpatentability asserting that the subject matter of claims 1–17 would have been unpatentable as set forth in the following table.

Claims Challenged	Statutory Basis	Reference(s)
1–3, 5, 7, 9–10, 13, 15–17	§ 102 / § 103	Ogawa[2]
6, 14	§ 103	Ogawa, Bohac[3]
6, 14	§ 103	Ogawa, McAnlis[4]
10, 12	§ 103	Ogawa, Zalewski[5] and/or Ogawa, Cellular-IRIX[6]
11	§ 103	Ogawa, Zalewski, McAnlis and/or Ogawa, Cellular-IRIX, McAnlis
1, 2, 4, 7–11, 13, 15–17	§ 103	Vea[7]
6, 14	§ 103	Vea, Bohac
10, 12	§ 103	Vea, Zalewski and/or Vea, Cellular-IRIX

Pet. 3. Petitioner's challenge is supported by the Declaration of Vijay K. Madisetti, Ph.D. (Ex. 1003).

[2] JP S60-24655, published February 7, 1985 (Ex. 1005).
[3] US 6,166,984, issued December 26, 2000 (Ex. 1007).
[4] US 4,458,307, issued July 3, 1984 (Ex. 1010).
[5] US 2002/0052914 A1, published May 2, 2002 (Ex. 1008).
[6] SilconGraphics, Cellular-IRIX™ 6.4 Technical Report, (1996) (Ex. 1009).
[7] US 4,924,428, issued May 8, 1990 (Ex. 1006).

III. ANALYSIS

We have authority to institute an *inter partes* review only where "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018). The findings and conclusions set forth in this Decision are provided for the exclusive purpose of explaining our determination that Petitioner has not met that standard on this record.

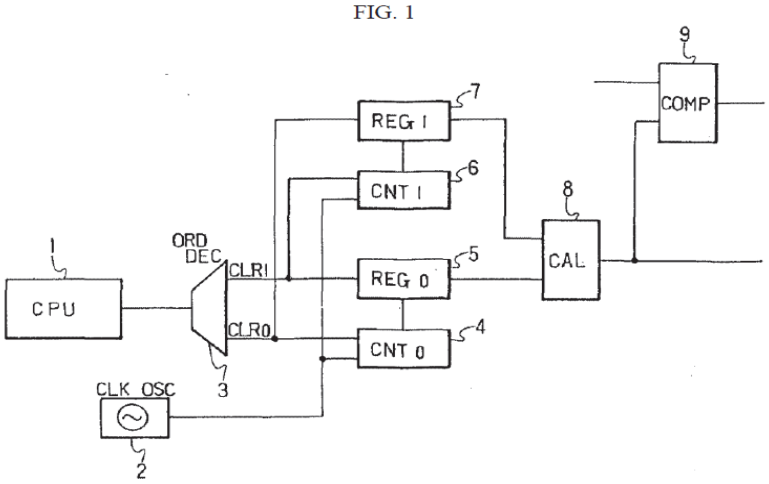
A. Overview of the Prior Art

1. Ogawa (Ex. 1005)

Ogawa discloses a device for measuring a usage rate of a central processing unit, and has "a processing format composed of a program which requires a time constraint and launches at a fixed time interval and is provided with first and second counters, first and second registers, an arithmetic circuit, and a control order decoder." Ex. 1005, 326 (UL).[8]

Ogawa's Figure 1 is illustrative and is reproduced below:

FIG. 1



[8] Like the parties, we refer to Ogawa's disclosure in the upper left quadrant of the page as "UL," the upper right as "UR," the lower left as "LL," and the lower right as "LR." *See, e.g.*, Pet. 11 n.5; Prelim. Resp. 6.

Ogawa's Figure 1 is a block diagram illustrating Ogawa's central processing unit usage rate measuring device including central processing unit 1, clock generator 2, control order decoder 3, first counter 4, second counter 6, first register 5, second register 7, arithmetic circuit 8, and comparator circuit 9. Ex. 1005, 326 (UR).

Ogawa discloses "central processing unit 1 is a processing unit . . . in which a periodic program is executed at a periodic time interval, and a clear 0 control order is sent from the central processing unit 1 to the control order decoder 3 at the start time of processing of the periodic program." Ex. 1005, 326 (LL).

> The control order decoder 3 decodes the foregoing control order, generates a CLR0 signal, and applies this to the first counter 4. Once the CLR0 signal is applied, the content of the first counter 4 is cleared, [and] the first counter 4 starts counting the clock signal sent from the first clock generator 2. Once the central processing unit 1 ends all processing of the periodic program, a clear 1 control order is sent from the central processing unit 1 to the control order decoder 3,

which then "decodes this control order, generates a CLR1 signal, and applies this to the second counter 6 and the second register 7." *Id.* "Once the CLR1 signal is applied, the content of the second counter 6 is cleared, and the second counter 6 starts counting the clock sent from the clock generator 2," and then "the first register 5 stores the content of the first counter 4." *Id.* at 326 (LL)–(LR). Ogawa discloses that "[o]nce the central processing unit 1 has again started the processing of the periodic program . . . , the clear 0 control order is again sent from the central processing unit 1." *Id.* at 326 (LR). At that point in time, first counter 4's content is cleared and begins counting the clock signal from clock signal generator 2. *Id.*

2. Vea (Ex. 1006)

Vea "relates to arrangements which measure the loading of a digital signal processor." Ex. 1006, 1:6–7. Vea teaches that "not all program code is as efficient as it could be, and even efficient code performing complex functions in real time can cause excessive processing loading." *Id.* at 1:50–53. Vea expresses a desire to measure the amount of available processing capacity under different operating conditions and describes how it achieves this measurement "by including diagnostic instructions in the processor 'idle loop'" which "consists of instructions which perform no useful function." *Id.* at 2:62–3:11. Vea's Figure 1 illustrates a digital signal processing system according to one embodiment:

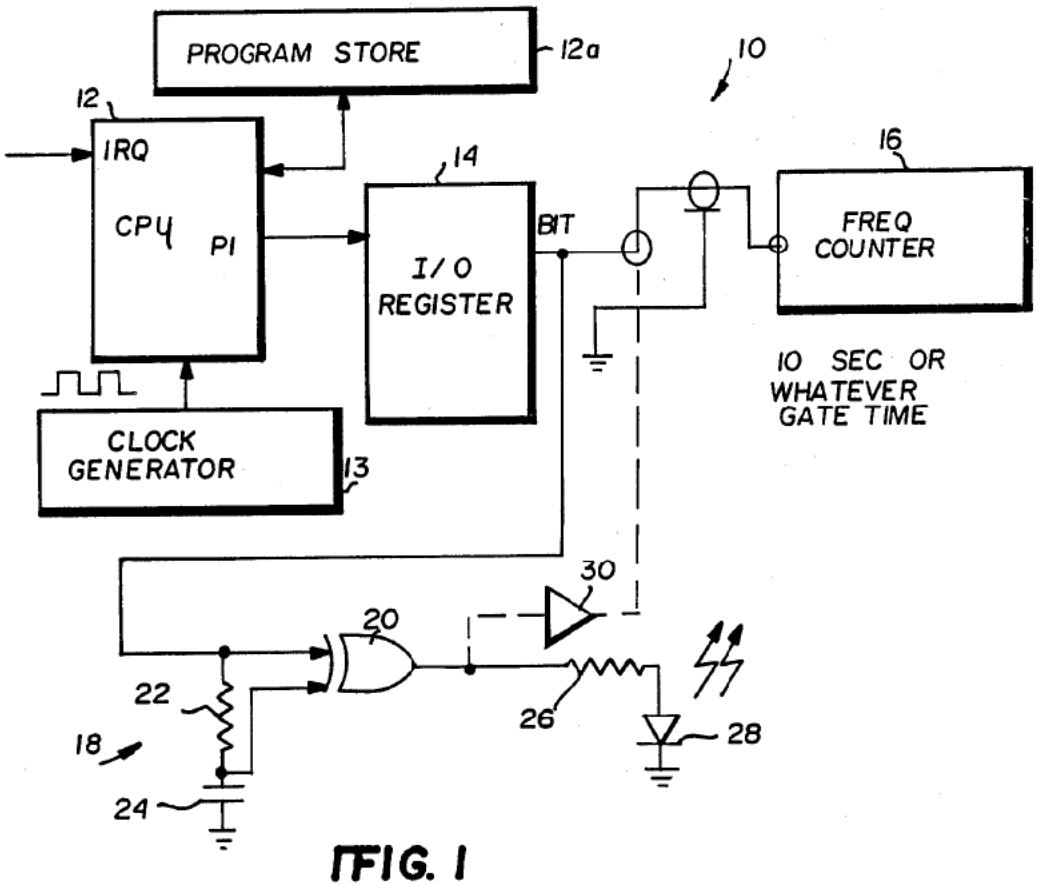


FIG. 1

Vea's Figure 1 is a schematic block diagram and depicts digital processing system 10, including, *inter alia*, central processing unit ("CPU") 12, clock signal generator 13, input/output register 14, and frequency counter 16. Ex. 1006, 4:4–42. When processor 12 is idle, it executes a loop program, where "a single loop execution will cause data output P1 to alternate once between logic level 0 and logic level 1 . . . resulting in a signal of one-quarter the processor clock frequency being generated whenever (and only when) the processor has nothing to do and is idling." *Id.* at 5:67–6:7.

B. Level of Ordinary Skill in the Art

Petitioner contends that a person having ordinary skill in the art ("POSITA") would have had "at least a Bachelor's degree in Computer Science, Computer Engineering, or a related field, with 3 years of experience in the area of distributed computer systems, including performance and/or resource optimizations. More education could substitute for experience, and vice versa." Pet. 9 (citing Ex. 1003 ¶¶ 35–39). Patent Owner does not propose a different level of skill in the art at this stage of the proceeding. *See* Prelim. Resp., *generally*.

On this record, we determine that the level of ordinary skill is reflected in the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (specific findings on the ordinary skill level are not required "where the prior art itself reflects an appropriate level and a need for testimony is not shown" (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163–64 (Fed. Cir. 1985))). A more specific definition is not necessary for purposes of deciding whether to institute review. To the extent a more specific definition is required, however, we

adopt Petitioner's proposed definition because, on this record, it is consistent with the disclosures of the asserted prior art references.

In any event, for the reasons explained below, even under Petitioner's definition, Petitioner fails to establish a reasonable likelihood of prevailing at trial with respect to any challenged claim based on the grounds of unpatentability advanced in the Petition.

C. Claim Construction

In an *inter partes* review, we construe a claim in an unexpired patent "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b) (2020). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Petitioner proffers no specific claim constructions. *See* Pet. 9 ("No claim term requires an exact outer boundary construction."). Patent Owner contends that the preambles in challenged independent claims 1 and 13 are limiting, and asserts that the parties have agreed to this in the district court action. Prelim. Resp. 4 (citing Ex. 2001, 2). According to Patent Owner, "the 'hardware based utilization metering device' or method is one where the metering function is not reliant on task-specific instructions from the processor or software characteristics of the programs." Prelim. Resp. 4–5.

Rather, Patent Owner asserts that "the hardware operates . . . in response to a state change in the processor, even if that change in state is precipitated by an instruction by the processor." *Id.* at 5. Patent Owner also asserts that "[t]he recited 'indication' received by an 'idle indicator' is one that indicates whether the processor is idle or busy." Prelim. Resp. 4–6.

After review of the preliminary record, we agree with Petitioner that no claim term requires express construction for purposes of this Decision. Pet. 9; *see Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("[C]laim terms need only be construed 'to the extent necessary to resolve the controversy.'").

D. Asserted Anticipation and/or Obviousness of Claims 1–3, 5, 7, 9, 10, 13, and 15–17 over Ogawa (Ground 1)

1. Petitioner's Assertions[9]

Petitioner asserts that Ogawa renders these claims anticipated, and by extension, obvious "because 'anticipation is the epitome of obviousness.'" Pet. 10 (citing *In re Pearson*, 494 F.2d 1399, 1402 (CCPA 1974)). Petitioner points to where it believes Ogawa discloses each limitation in these challenged claims. *Id.* at 13–30.

Specifically, regarding claim 1, Petitioner maps Ogawa's decoder 3 to the claimed "idle indicator" and asserts that "Ogawa's decoder 3 receives an indication ('clear 0') that CPU 1 is in a 'busy state' and another indication ('clear 1') that CPU 1 is in an 'idle state.'" *Id.* at 15–16 (citing Ex. 1003 ¶¶ 85–87). According to Petitioner, "[w]hile either the busy or idle state

[9] We need only discuss Petitioner's assertions relevant to our disposition of this challenge.

meets claim 1's 'first state,' . . . the first state is mapped to the 'busy' state for simplification." Pet. 16–17. Thus, Petitioner maps Ogawa's "clear 0" control order to the claimed "indication when the processor is in a first [busy] state." *Id.* at 16.

Regarding the claimed "counter" and "system clock" limitations, Petitioner asserts that "Ogawa's counter 4 meets the claimed counter when the 'first state' is the busy state," and that Ogawa's counter 4 is coupled to clock generator 2, which meets the claimed "system clock." Pet. 17. According to Petitioner, Ogawa's decoder 3 decodes the clear 0 control order, thus generating a CLR0 signal which is applied to first counter 4. *Id.* at 18. "When counter 4 receives the CLR0 signal, its content 'is cleared [and] the first counter 4 starts counting the clock signal sent from the first clock generator 2.'" *Id.* (quoting Ogawa, 326 (LL)). Petitioner asserts that "[c]ounting continues until CPU1 'ends all processing of the periodic program' and sends a 'clear 1' control order that results in decoder 3 generating a CLR1 signal that causes" counter 4's contents to be stored in register 5. *Id.* (quoting Ogawa, 326 (LL)-(LR)). According to Petitioner, counter 4's content indicates the effective processing time of CPU1, or the time that CPU1 was in the first, or busy, state. *Id.*

Regarding claim 13, Petitioner relies substantially on assertions it makes with respect to claim 1. *See* Pet. 27–29 (referring back to assertions made against claim 1 for all but one limitation for claim 13). For example, for the limitation requiring "providing a busy indication to a counter associated with a busy processor," i.e., limitation 13[B], Petitioner asserts that "Ogawa's measuring circuit provides a busy indication to counter 4

when its associated CPU is busy." *Id.* at 28 (citing previous sections of the Petition discussing elements 1[A] and 1[B]).

2. Patent Owner's Arguments

Patent Owner makes arguments pertaining to, *inter alia*, the "idle indicator" and "indication" limitations recited in claim 1, and the "indication" limitation recited in claim 13. Prelim. Resp. 12–15, 21–24.

Regarding claim 1 specifically, Patent Owner argues that Ogawa's "control orders," which are received by the decoder, are not "indication[s] when the processor is in a first [e.g., busy] state." *Id.* at 12; *see also id.* at 10 ("Ogawa's decoder 3 . . . receives 'control orders' from the CPU, not idle/busy indications as required by" the claim). According to Patent Owner, Ogawa's approach "differs from the '809 patent, in which the idle indicator receives signals that indicate what state the CPU is in, instead of task-specific commands that order components of the utilization metering device to carry out specific tasks" as in Ogawa. *Id.* at 13 (citing Ex. 1001, 4:37–45 and contending that the "idle indicator" of the '809 patent reads a "halt indication asserted on the halt pin" as either "a high or low value asserted on the pin"). Thus, Patent Owner avers that Ogawa's control order decoder 3, which the Petition maps to the claimed "idle indicator," does not meet the claim "idle indicator" limitation because it does not "receive[] an indication when the processor is in a first state." *Id.* at 15.

Regarding claim 13, Patent Owner argues, *inter alia*, that Ogawa's decoded command signal CLR0 does not meet the limitation of "providing a busy indication to a counter associated with a busy processor." Prelim. Resp. 21–22. According to Patent Owner, "[t]he CLR0 signal does

not indicate to the counter that the processor is busy, only the actions that the counter must take." *Id.* at 22.

3. Analysis

a. Claims 1–3, 5, 7, 9, and 10

After considering the parties' opposing positions and the evidence provided, we determine that Petitioner fails to establish a reasonable likelihood of prevailing with respect to these claims. Our reasoning follows.

Apparatus claim 1 requires "an idle indicator . . . [which] receives an indication when the processor is in a first state," such as a busy state. Ex. 1001, 7:32–34. Petitioner maps the "idle indicator" element to Ogawa's control order decoder 3 and the claimed "indication" to Ogawa's "clear 0 control order." Pet. 15–16. Petitioner, however, has not sufficiently explained how Ogawa's "clear 0 control order" amounts to an "indication" that Ogawa's CPU is in a busy state. By extension, Petitioner fails to sufficiently show how Ogawa's control order decoder 3 meets the "idle indicator" limitation of claim 1 because the idle indicator receives such an indication. Ex. 1001, 7:32–34.

On this point, both the '809 patent's disclosure and prosecution history are informative. Notably, the '809 patent distinguishes its hardware-based CPU utilization metering device over previous approaches that employed software running on a CPU. Ex. 1001, 1:13–45, 2:48–3:21. In particular, the '809 patent teaches that at the time of the invention, "metering of processor utilization . . . [was] accomplished by software running within the computer's operating system," and sometimes "require[d] communications between the metering application and all operating systems running within the hardware." *Id.* at 1:16–22. Such "communication with

different operating systems pose[d] significant challenges because operating systems by their design are separated from other operating systems and do not have visibility to utilization data from other operating systems." *Id.* at 1:22–26. The '809 patent teaches that its hardware based "apparatus and method for collecting CPU utilization data overcomes these problems." *Id.* at 3:18–19.

Turning now to the '809 patent's prosecution history, in the Office Action dated October 6, 2003, a previous version of claims 1–12 was rejected under pre-AIA 35 U.S.C. § 102(b) as anticipated by US Patent 6,049,798 to Bishop.[10] Ex. 1002, 41–42, 52–53. At that point in prosecution, claim 1 recited a "state indicator" rather than an "idle indicator." *Id.* at 41. In response to the anticipation rejection over Bishop, the applicant, on January 6, 2004, amended claim 1 to recite "an idle indicator coupled to a processor, wherein the idle indicator receives an indication when the processor is in a first state," which is the language recited in issued claim 1 of the '809 patent. *Compare* Ex. 1002, 59, *with* Ex. 1001, 7:32–34. Along with that amendment, the applicant presented the following arguments distinguishing the claimed "idle indicator" from the system disclosed in Bishop:

> Bishop is directed to a system resource monitor that captures data processing system internal resource utilization such as memory utilization, CPU utilization, or peripheral device availability and utilization. With respect to CPU utilization, Bishop discloses, as a means for measuring utilization, starting a *process* and assigning the *process* to a lowest priority level in the system. Thus, at least this low-priority process is always executing on the CPU, and the CPU is never idle. When more

[10] Petitioner provides a copy of this reference as Exhibit 1011.

> critical or higher priority processes are ready for execution, the low-priority process running on the CPU is halted and the higher priority processes execute. *See* Bishop, column 10, lines 51–67. To verify that the low-priority process is executing, Bishop discloses using SYSTRACE, provided by the OS2 operating system, to obtain an event trace of the low-priority process. *See* Bishop, column 11, lines 1–6. *Thus, in terms of CPU utilization, Bishop does not disclose or suggest use of an idle indicator. Instead, Bishop specifically and emphatically discloses use of a known event trace to detect operation of the low-priority process on the CPU.*
>
> In contrast to Bishop, claim 1 as amended recites an idle indicator coupled to a processor. The idle indicator is a hardware device coupled to a pin of the processor and the hardware device reads a signal asserted on the pin when the processor is idle, i.e., not executing <u>any</u> process. (*See* claim 3). As noted above, Bishop discloses a mechanism for detecting and recording occurrence of low-priority *processes* executing on a processor. Thus, Bishop does not disclose or suggest all of the features of claim 1.

Ex. 1002, 62 (italicized emphases added, underline emphasis in original).

In an Examiner interview on January 8, 2004—two days after filing the aforementioned claim amendment and arguments—the Examiner indicated that an agreement with respect to the claims was reached, and furthermore agreed that the Bishop reference did "not disclose . . . the idle indicator of processors in a busy state." *See* Ex. 1002, 66 (Interview Summary of interview conducted January 8, 2004). The Examiner also indicated that an updated search of the prior art would be conducted, with "[p]articular attention about idle indicator of CPU in busy state." *Id.* Less than three months later, on April 6, 2004, the Examiner issued a Notice of Allowance as the next Office communication. *Id.* at 71. Thus, the Examiner allowed issued claims 1–12 over the Bishop reference, which discloses

calculating CPU utilization by, *inter alia*, running a program on the CPU.

Turning to Petitioner's specific challenge here, we agree with Patent Owner that Ogawa's central processing unit (CPU) 1 sends control orders to control order decoder 3. Ex. 1005, 326 (LL); Prelim. Resp. 7. If CPU1 issues a "clear 0 control order," control decoder 3 decodes this control order and generates a CLR0 signal. Ex. 1006, 326 (LL). That CLR0 signal is applied to Ogawa's first counter 4, which clears the counter and then starts counting the clock signal sent from clock generator 2. *Id.* Thus, similar to Bishop's device, and distinct from claim 1, Ogawa runs a "program" in order to obtain the CPU's usage rate. *Compare* Ex. 1011, 10:50–67 (exemplifying four classes of data processing system tasks,[11] each with different priority levels, and tracking the amount of time the lowest priority process is executing in the system), *with* Ogawa, 326 (UL), (LL) (disclosing that the usage rate measuring device uses "a *program* which requires a time constraint and launches at a fixed time interval" and that "a clear 0 control order is sent from the central processing unit 1 to the control order decoder 3 at the start time of processing of the periodic *program*" (emphasis added)).

Significantly, Petitioner acknowledges that "[t]he '809 Patent criticizes software-based solutions" to metering CPU usage. Pet. 4 (citing Ex. 1001, 1:15–45, 2:50–3:17); *see also* Ex. 2002, 21 (Petitioner Google affirmatively stating in its claim construction briefing in the district court action that "the purpose of this invention is to *avoid* the problems of collecting usage statistics from discrete operating systems running different

[11] Bishop discloses that one of these task classes is "Regular, which is the normal class assigned to application *programs*." Ex. 1011, 10:64–65 (emphasis added).

software *by instead using hardware*" (emphasis in original)). Petitioner acknowledges the prosecution history of the '809 patent as it pertains to Bishop (Pet. 8–9), and even filed the Bishop reference as an exhibit in this proceeding (Ex. 1011). Petitioner, however, has not explained how Ogawa's reliance on a software program to obtain CPU usage is distinguishable over Bishop's use of a software program to calculate CPU activity, or demonstrated sufficiently how such reliance on software corresponds to the limitations in claim 1. Rather, Petitioner merely asserts that "Ogawa's decoder 3 receives an indication ('clear 0') that CPU 1 is in a 'busy state' and another indication ('clear 1') that CPU 1 is in an 'idle state.'" Pet. 16 (citing Ex. 1003 ¶ 87).[12] Such an explanation from Petitioner regarding how Ogawa's "control order" meets the claimed "indication" provided to the "idle indicator" of the challenged claims is particularly necessary here in view of the '809 patent's teachings and prosecution history discussed *supra*. In sum, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in this challenge of claims 1–3, 5, 7, 9, and 10.

b. Claims 13 and 15–17

After considering the parties' opposing positions and the evidence provided, we determine that Petitioner fails to establish a reasonable likelihood of prevailing with respect to these claims. Our reasoning follows.

Method claim 13 requires "providing a busy indication to a counter associated with a busy processor." Ex. 1001, 8:19–20. For this limitation, Petitioner asserts that "Ogawa's measuring circuit provides a busy indication to counter 4 when its associated CPU is busy," and points to its discussion at

[12] Dr. Madisetti's testimony here is entitled to little to no weight as it merely parrots the Petition. 37 C.F.R. § 42.65(a).

pages 15–18 of the Petition for support. Pet. 28. That disclosure, however, is insufficient to evince the step of providing a busy indication to a counter associated with a busy processor.

Here, we note that Petitioner provides a single sentence assertion with no specific mapping as to what constitutes the "busy indication" provided to Ogawa's counter. Pet. 28. As best we can understand, because of Petitioner's reliance on its earlier statements with respect to limitations in claim 1, Petitioner is mapping the "busy indication" of clam 13 to the same disclosures of Ogawa that purportedly meet the "indication" recited in claim 1. *See id.* at 16 ("Ogawa's decoder 3 receives an indication ('clear 0') that CPU 1 is in a 'busy state'"). For the reasons we have already explained, however, Petitioner has not shown sufficiently that Ogawa's "clear 0 control order" meets the claimed "indication." Those problems notwithstanding, we additionally observe that Petitioner has not explained how Ogawa's "clear 0 control order" is provided to counter 4 as is required by claim 13. Indeed, Ogawa's "clear 0 control order" is provided to control order decoder 3, not counter 4. Ex. 1005, 326 (LL).

c. Conclusion

In sum, upon reviewing Petitioner's assertions and associated citations to evidence, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail with respect to its challenge of claims 1–3, 5, 7, 9, 10, 13, and 15–17 based on Ogawa. Pet. 10–30.

E. Asserted Obviousness of Claims 1, 2, 4, and 6–17 over Vea with or without additional prior art (Grounds 6–8)

Petitioner's assertions with respect to these challenges appear at pages 41–68 of the Petition. Patent Owner asserts, *inter alia*, that we should

exercise our discretion under 35 U.S.C. § 325(d) and deny the petition because the EP counterpart to Vea, EP0320329, was already considered by the Office. Prelim. Resp. 42–43.

In evaluating matters under § 325(d), the Board uses the two-part framework set forth under *Advanced Bionics, LLC v. Med-El Electromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"). Under that framework, we must first determine whether the same or substantially the same art or arguments previously were presented to the Office. If so, we must then determine whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims. *Id.* at 8.

We consider several non-exclusive factors as set forth in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) ("*Becton, Dickinson*"), which "provide useful insight into how to apply the framework" under § 325(d). *Advanced Bionics*, 9. Those non-exclusive factors include:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;
>
> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
>
> (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and

> (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson, 17–18 (formatting added). "If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office, then factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office." *Advanced Bionics*, 10.

1. Part one of the Advanced Bionics framework

Part one of the *Advanced Bionics* framework relates to whether the same or substantially the same art or arguments were presented previously to the Office. *Advanced Bionics*, 10.

Here, we determine that substantially the same art as that relied on in Ground 6 (i.e., Vea (Ex. 1006)) was presented previously to the Office in the form of Vea's European patent counterpart—EP0320329. *Compare* Ex. 1006, *with* Ex. 1014, 26–34. The European counterpart of Vea[13] was cited in an Information Disclosure Statement filed February 24, 2004, and was considered by the Examiner on April 1, 2004. Ex. 1002, 68, 75. This European patent appears on the face of the '809 patent. Ex. 1001, code (56).

2. Part two of the Advanced Bionics framework

Because the first part of the *Advanced Bionics* framework is satisfied, we turn to whether Petitioner has demonstrated that the Office erred in a

[13] The IDS Form PTO-1449 erroneously refers to the "Name of Patentee or Applicant" of EP 0320329 as "Vee" instead of "Vea." We treat this as a harmless typographical error because the EP patent number and publication date recorded on the IDS are sufficient to correctly identify this document as the European counterpart to that relied on in this proceeding. Ex. 1001, code (56); Ex. 1002, 68, 75; Ex. 1006; Ex. 1014, 26–34.

manner material to the patentability of [the] challenged claims. *Advanced Bionics*, 8. According to *Advanced Bionics*, "[i]f . . . the petitioner fails to make a showing of material error, the Director generally will exercise discretion not to institute *inter partes* review." *Id.* at 8–9.

On this record, Petitioner fails to make a showing of material error by the Office in its consideration of EP0320329. Indeed, Petitioner does not address the Office's consideration of this reference with any degree of specificity. Pet., *generally*; *see id.* at 72 (providing a mere two sentence assertion regarding § 325(d) that "[n]one of the Ground's references were before the Office during the '809 Patent's prosecution. Discretionary denial is not warranted under § 325(d)."); *see* Prelim. Resp. 43 ("Petitioner does not assert the Office made any material errors.").

Because Petitioner fails to demonstrate material error by the Office in its previous consideration of a reference (EP0320329 to Vea, Ex. 1014, 26–34) that is substantially the same as that relied on in this challenge (US 4,924,428 to Vea, Ex. 1006), we exercise our discretion under § 325(d) to deny institution of Ground 6, as well as the other grounds that rely on Vea, i.e., Grounds 7 and 8. Here, Petitioner relies on the Bohac reference in Ground 7 and the Zelewski and/or Cellular-IRIX references in Ground 8 to evince certain limitations found in dependent claims 6, 10, 12, and 14. Pet. 66–68. The Bohac, Zelewski, and Cellular-IRIX references are not relied on by Petitioner to replace the teachings of Vea. Thus, our denial under 35 U.S.C. § 325(d) naturally extends to Grounds 7 and 8 which rely heavily on Vea's disclosures. *See Kayak Software Corp. v. IBM*, CBM2016-00075, Paper 16 at 10 (PTAB Dec. 15, 2016) (informative) (holding Petitioners' citation of a reference not considered by the Examiner solely for

"additional subject matter of certain dependent claims[] is insufficient to persuade us that exercising our discretion under 35 U.S.C. § 325(d) is inappropriate").

On a final note, we refer to Petitioner's request for Board authorization to file a Reply to the Patent Owner Preliminary Response on this particular issue. Ex. 3001, 2 (item 3). Although we denied that request after a conference call held November 8, 2022, we observe that Petitioner identified several Board cases during that call which it believed are "inconsistent" with us exercising our discretion to deny institution under § 325(d) as we have done here. Ex. 1052, 14. Specifically, Petitioner's counsel argued during that call that several Board cases stood for the proposition that "[t]he mere citation in an IDS is not enough to warrant a Section 325(d) denial." *Id.* Petitioner identified three non-precedential Board decisions from the following proceedings: IPR2022-00457, IPR2022-00309, and IPR2018-00871. We have reviewed the decisions from those cases and, as explained *infra*, find they do not control and/or are inapposite to the facts presented in this proceeding.

In IPR2022-00457, the Board declined to exercise its discretion to deny institution under § 325(d) where the same Lahetkangas reference applied in the Petition was cited in an Information Disclosure Statement and considered by the Examiner but was not applied in a rejection. *Apple Inc. v. Telefonaktiebolaget LM Ericsson*, IPR2022-00457, Paper 7 (PTAB Sept. 21, 2022), 8–9. The Board found that parts one and two of the *Advanced Bionics* framework were satisfied and that, with respect to part two, "Petitioner has presented a sufficient showing that the Examiner overlooked disclosures in Lahetkangas that render obvious the challenged claims." *Id.*

at 8. The facts of IPR2022-00457 are readily distinguishable from those presented here, however. In IPR2022-00457, Petitioner made an affirmative showing that the Office made a material error in its consideration of Lahetkangas. *Id.* Significantly, Petitioner Apple *presented an argument* that the Office materially erred in its consideration of this reference. *Apple Inc. v. Telefonaktiebolaget LM Ericsson*, IPR2022-00457, Paper 1, 18–19. Here, Petitioner makes no such argument. Pet., *generally*.

In IPR2022-00309, the Board declined to exercise its discretion to deny institution under § 325(d) after finding that the same Ueno reference applied in the Petition was cited in an Information Disclosure Statement and considered by the Examiner but was not applied in a rejection. *STMicroelectronics, Inc. v. The Trustees of Purdue University*, IPR2022-00309, Paper 14 (PTAB July 6, 2022), 12–14. During prosecution of US Patent 8,035,112 B1 which was the subject of IPR2022-00309, the applicant filed the Information Disclosure Statement citing the Ueno reference as one of twenty-five (25) references almost four months before (i.e., October 28, 2010) the Office issued the first Office Action on the merits (i.e., February 23, 2011).

Here, the applicant filed the EP counterpart of Vea as one of only three citations, and less than two months after the applicant conducted an Examiner interview where agreement had been reached on the claims after rejection, and where the Examiner affirmatively stated that an updated search would be conducted with "[p]articular attention about idle indicator of CPU in busy state and plurality [of] processors." Ex. 1002, 66, 68. Under these circumstances, we determine it is less likely that the Examiner would have failed to appreciate the contents of EP0320329 as the panel

found the Examiner did with Ueno's disclosure in IPR2022-00309, and therefore do not see how the specific facts of that case compel a different application of § 325(d) here. *STMicroelectronics, Inc.*, Paper 14 at 13.

Finally, with respect to the institution decision in IPR2018-00871, we find this particular decision inapposite for the simple reason that it predates our precedential *Advanced Bionics* decision establishing the two-part framework discussed *supra*. *See Intex Recreation Corp., et al. v. Team Worldwide Corporation*, IPR2018-00871, Paper 14 (PTAB Sept. 14, 2018).

F. Remaining Grounds (Grounds 2–5)

Petitioner's reliance on the Bohac, McAnlis, Zalewski, and Cellular-IRIX references does not address, much less remedy, the aforementioned deficiencies identified with respect to Ground 1. Pet. 30–41. Petitioner has, therefore, failed to establish a reasonable likelihood of prevailing on these challenges for substantially the same reasons provided *supra* with respect to Ground 1.

IV. CONCLUSION

Based on the information presented in the Petition and the Preliminary Response, we deny the Petition and do not institute an *inter partes* review.

V. ORDER

It is

ORDERED that the Petition is *denied* and no *inter partes* review is instituted.

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