# A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling

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***Abstract*—A PowerPC system-on-a-chip processor which makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications is described. The PowerPC core and caches achieve frequencies as high as 380 MHz at a supply of 1.8 V and active power consumption as low as 53 mW at a supply of 1.0 V. The system executes up to 500 DMIPS and can achieve standby power as low as 54 $\mu$W. Logic supply changes as fast as 10 mV/ $\mu$s are supported. A low-voltage PLL supplied by an on-chip regulator, which isolates the clock generator from the variable logic supply, allows the SOC to operate continuously while the logic supply voltage is modified. Hardware accelerators for speech recognition, instruction-stream decompression and cryptography are included in the SOC. The SOC occupies 36 mm$^2$ in a 0.18 $\mu$m, 1.8 V nominal-supply, bulk CMOS process.**

***Index Terms*—Dynamic frequency scaling, dynamic voltage scaling, low power microprocessors, phase-locked loops.**

## I. Introduction

THIS PowerPC system-on-a-chip (SOC) design platform is intended to address the high-content battery-powered market segment. This segment includes information appliances such as Web pads, advanced PDAs, cell phones and small form-factor PCs. These applications tend to have peak performance demands as high as 500 MIPS but also tend to remain idle for much of the time. During active computation their required performance tends to vary widely and quickly as a function of the workload. While their peak performance demands tend to be significant, they are also highly power constrained. During peak activity the power consumption of the processor core is best kept at or below about 500 mW. When the device is truly inactive for periods as long as four weeks, a 1200-mA·h battery supply should not be fully consumed. This constrains the standby power of the hibernated processor and the consumption of the sleep monitor.

To address the battery-powered applications we have developed a voltage scalable SOC platform in a 0.18-micron 1.8-V bulk CMOS process. The processor consists of a 32-bit PowerPC core with instruction and data caches. The SOC uses IBM's Core-Connect technology [1] to integrate a rich set of memory and I/O interfaces. In addition, on-chip hardware accelerators have been developed to improve the performance and power consumption of important tasks. A block diagram of the SOC is shown in Fig. 1. Properties of the CMOS fabrication technology are presented in Table I. Characteristics of the PowerPC core with caches are presented in Table II. Characteristics of the SOC are presented in Table III.

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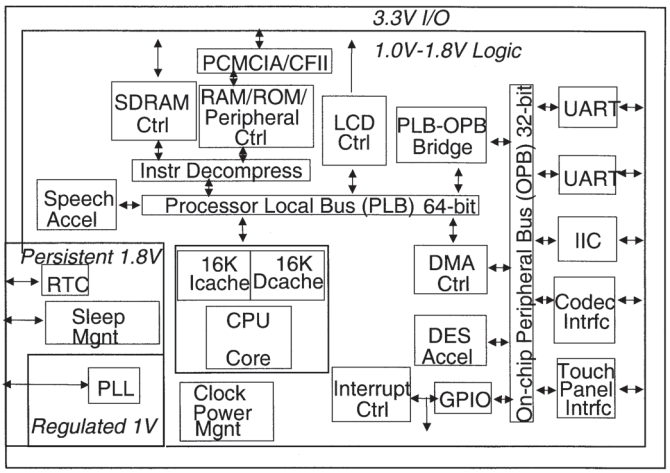


Fig. 1. PowerPC SOC structure.

TABLE I
Technology Properties

| Characteristic | Value |
|---|---|
| Process | Bulk CMOS |
| Lithography | 0.18mm |
| Leff | 0.11µm Nch<br>0.14µm Pch |
| Tox | 3.5nm |
| Interconnect | 3-6 levels copper |

## II. System Overview

This SOC design consists of a high performance 32-bit processor core, which is fully compliant with the PowerPC specification. The processor core for this design was based upon an existing, fixed voltage PowerPC 405 core [2]. The core includes a hardware multiply accumulate unit, hardware division, static

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TABLE II
CPU CORE WITH CACHES CHARACTERSITICS

| | TC1 (1.8V) | TC2 (1.0V) |
|---|---|---|
| Maximum Frequency (estimate) | 380 MHz | 152 MHz |
| Power Consumption (estimate) | 500 mW | 53 mW |

TC1 – Typical conditions: 1.8V, 55C, nominal silicon
TC2 – Typical conditions: 1.0V, 55C, nominal silicon

TABLE III
SYSTEM-ON-A-CHIP CHARACTERISTICS

| Characteristic | Value |
|---|---|
| Architecture | 32-bit PowerPC |
| Caches | 16kbyte instruction<br>16kbyte data |
| Die Size | 36 $mm^2$ |
| Transistors | 5.8 million |
| Interconnect | 5 level copper |
| Package | 316-EPBGA<br>(27 x 27) |

branch prediction support and a 64-entry, fully-associative translation lookaside buffer. The CPU pipeline is five stages deep. Single cycle access, two-way set associative, 16-kbyte SRAM instruction and data caches are connected to the processor core.

The processor core connects to external SDRAM and to external memory, storage and network through the PCMCIA/Compact Flash interface by way of the 64-bit processor local bus (PLB). An integrated LCD display controller is also attached to the PLB. Lower bandwidth I/O interfaces are included by way of the 32-bit on-chip peripheral bus. These interfaces include two UARTs, an IIC interface, the general- purpose I/O lines, an audio CODEC, and a touch panel controller interface.

A dedicated speech accelerator, an instruction decompression engine and a DES accelerator core are included on the SOC to accelerate key tasks. A low-voltage phase-locked-loop core and a real-time-clock core are on the SOC for on-chip clock generation. A clock power-management core and a sleep-management core are also included.

Fig. 2 shows a die photograph of the SOC after processing of the third level of metal. The die is 6.02 mm on a side and is ringed by peripheral I/O pads. The area of this design is constrained by the packaging image resulting in significant white space within the SOC. This device was fabricated in a 0.18-micron bulk CMOS process with 5 levels of copper interconnect.

The PowerPC processor core satisfies the performance demands of the intended applications. Capabilities to dynamically match the performance of the device with the demands of the applications are provided. This SOC additionally makes use of active power reduction techniques to dynamically match the power consumption with the requirements of the application. The active power consumption is reduced when resources demands are low through the use of dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating. In addition, dedicated hardware accelerators perform key tasks more efficiently. Finally, the system-on-a-chip integration allows this design to avoid costly off-chip accesses. Specific

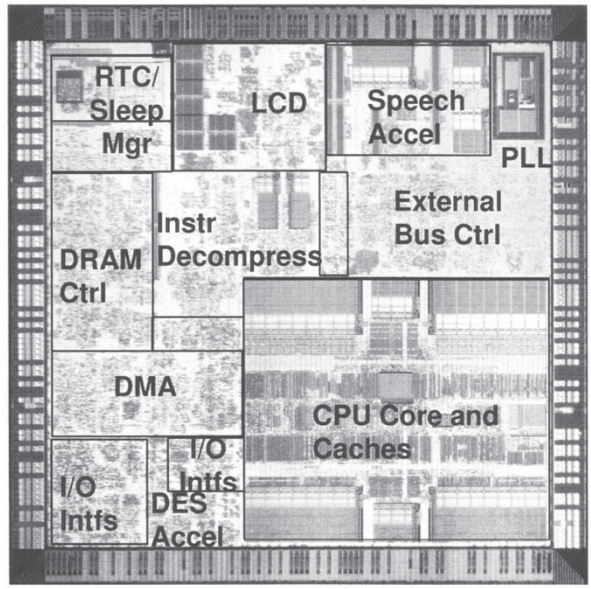


Fig. 2. PowerPC SOC die photograph.

mechanisms for these techniques and results using these techniques will now be described.

## III. DYNAMIC VOLTAGE SCALING

The primary means of matching the performance and power consumption of this device to the application is through the use of dynamic voltage scaling (DVS). Processor energy efficiency can be improved by scaling the supply voltage [3]–[5]. DVS systems adjust the supply voltage dynamically to meet the performance demands while minimizing power consumption [6]–[9]. The dynamic energy consumption is reduced quadratically with the decreasing supply while the commensurate maximum frequency decreases approximately linearly near the nominal supply and super-linearly farther from the nominal supply. For battery-powered applications where both energy efficiency and performance are crucial, voltage scaling enables a wide range of performance and power consumption.

### A. Dynamic Voltage Scaling Architecture

To support DVS in this SOC, the power distribution has been divided into four distinct domains as shown in Fig. 3. These consist of two persistent voltage domains, one dynamically voltage-scaled logic domain and one internally derived domain. The I/O drivers and receivers are powered by a persistent 3.3-V supply. The real-time clock and the logic associated with controlling the voltage of the cores is powered by a persistent, battery-backed 1.8-V supply. The logic supply for the processor core, caches, SOC cores and accelerators is dynamically varied between 1 and 1.8 V. Finally, the PLL [10] is powered by an on-chip linear regulator, which derives a constant 1-V supply from the dynamically-varying logic supply. The power domains and the signal interfaces between the domains are shown in Fig. 3.

An on-chip supervisor controls the external DC/DC converter, which provides the logic supply. Under software control, the supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation. Because the

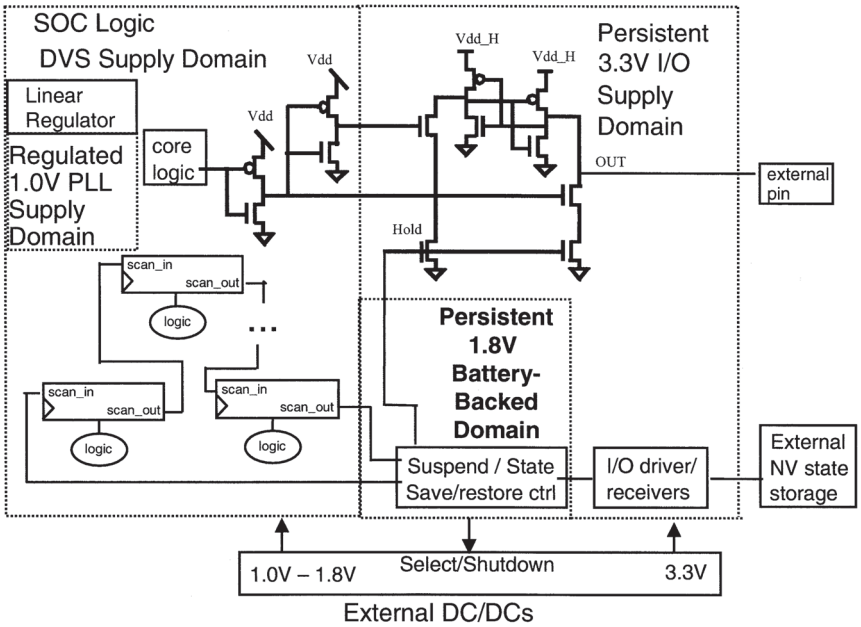


Fig. 3. Signal and state interfaces for multiple supply domains.

logic supply is not persistent, signals passing from the logic domain to a persistent domain are latched by level shifters at the interface.

### *B. Dynamic Voltage Scalable Circuits*

Significant modifications to the circuit design were required to support a logic supply which can be reduced to 55% of its nominal 1.8-V value. Whereas static CMOS logic gates quite easily tolerate the lower supply, custom arrays, latches and analog circuits do not. In addition, interfacing between different, variable supply domains necessitates changes to the I/O drivers and receivers.

In the register arrays and latches, single-ended pass gates were eliminated and replaced with full N/P-pairs, differential structures, or precharge structures with static keepers. No dynamic storage nodes were allowed. In addition, to support the lower supplies, the beta ratios of many custom circuits were increased to avoid low-voltage performance degradation.

The 1.8–3.3-V I/O drivers were modified to accommodate input signals as low as 0.9 V. Analog circuits in the PLL and touch-panel controller were designed for low voltage. The PLL was designed for supplies as low as 0.85 V. Rather than requiring the PLL to relock each time the logic supply was adjusted, we developed a low-voltage PLL whose supply is derived by a regulator off of the variable logic supply [10]. Since the regulated voltage is relatively constant, as the supply changes, the system continues to operate over the dynamic voltage and frequency scaling ranges. If PLL relocking were to be required, even a relatively fast 20 $\mu$s relock time represents a loss of about 2000–5000 instruction cycles.

Low voltage circuit behavior differs significantly from behavior at nominal supplies. Dispersion of delays amongst gates and between gate and interconnect were observed. High transistor stacks were generally avoided to minimize variation amongst gates. The interconnect RC delay component is relatively independent of supply voltage. Arrays, which used static gate timing chains to match array access paths with significant wire loads, required retuning for low voltage. For instance, to avoid failures in the TLB due to race-through of precharge events, the delay of the timing chain which generates the CAM-to-RAM strobe had to be redesigned to disable earlier.

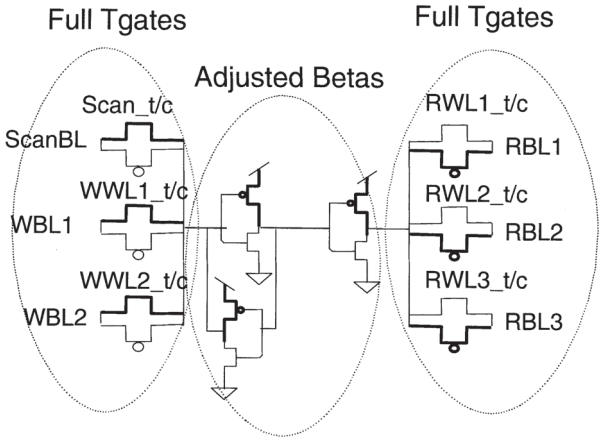


Fig. 4. Register cell modified for DVS.

Fig. 4 illustrates the sort of major modifications needed to support scalability, in this case for the 3-read port, 2 write-port, fully-scannable general-purpose register file. The register cell was modified to include full N/P-pairs on both the read and write ports, which in previous implementations were single-ended. To improve low voltage cell stability, the beta ratio of the feedback inverter within the cell was increased by about 50% and the forward inverter betas were adjusted to balance access timing.

These modifications resulted in about a 50% increase in the size of the register array. By carefully adjusting the floorplan the overall size of the processor core remained constant. At nominal supply, register reads were degraded by 7.5% due to the increased gate and interconnect capacitance. Write performance

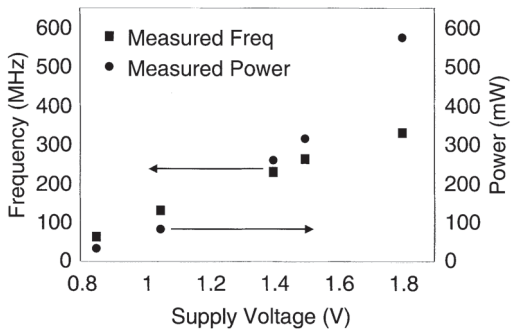


Fig. 5. Dhrystone2.1 voltage scaling measurements.

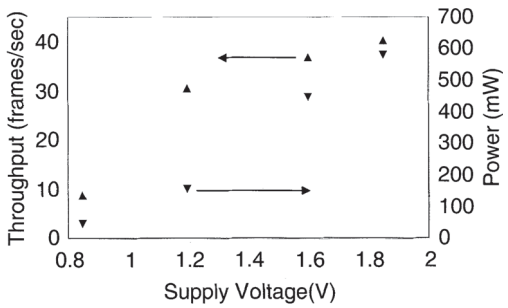


Fig. 6. MPEG-4 decode voltage scaling measurements.

was improved. The delay changes did not affect the processor core timing, as the register file read access was not in the critical path of the processor core. The processor core, when modified to support DVS, occupies the same area and achieves equivalent performance at the nominal voltage supply as the unmodified core in the same technology.

### C. Measured DVS Results

Figs. 5 and 6 present the effectiveness of voltage scaling. These data were taken on a nominal part operating at room temperature. The power consumed in the 3.3 V I/O domain is not included in these measurements. In Fig. 5 the SOC was running the Dhrystone2.1 benchmark under Linux. This benchmark tends to stress the processor core. The SOC consumed 570 mW at 333 MHz and executed 500 DMIP at the nominal supply voltage. When the supply was lowered to 0.85 V the SOC consumed 33 mW at 66 MHz. This represents a frequency range of 5:1 with a power range of 17:1.

In Fig. 6, the device was performing MPEG-4 decoding under Linux. This application makes significantly greater demands on the cache and memory, I/O interfaces and LCD core than Dhrystone2.1. The throughput of the MPEG-4 decode is varied over a range of 4:1 with a logic supply power consumption range of about 13:1.

## IV. Scalable Clocking Subsystem

As previously indicated, the clock generation subsystem is key to supporting a voltage scalable design. As shown in Fig. 7, the PLL for this SOC is powered by an on-chip linear regulator. The regulator uses an on-chip band-gap reference circuit as a 1 V reference. The regulator produces a constant 1 V output despite input supply changes as fast as 10 mV/$\mu$s. To account for differences between the regulated voltage and the logic voltage, the PLL integrates level shifting into the reference clock, feedback clock and output clock paths.

The PLL uses D-type phase/frequency detectors and a differential charge pump to generate control voltages for the VCO. The VCO is an interleaved five-stage ring oscillator [11]. The VCO tuning range is between 513 and 1017 MHz across full process corners. Duty cycle correction is accomplished through a divide-by-two performed in the output path level shifter. Adjustment to the output clock frequency can be done on-the-fly by modifying the output clock divider through a write to a control register. This allows adjustment of the frequency across a range of 1/2 to 1/128th of the VCO frequency. A glitchless output multiplexor avoids spurious clock pulses during this operation and allows for clock freezing for sleep and hibernation modes. The output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock as the processor clock source to allow for extremely low frequency operation.

These on-the-fly frequency modification techniques can be used to provide dynamic frequency scaling for additional active power reduction. When the performance demands of the application decrease, the system software can lower the operating frequency. Under software control, at a given supply voltage, the frequency of the core can be varied from the maximum frequency down to 1/64th of the maximum. This allows the frequency to be dynamically set as low as 4.2 MHz.

## V. Dynamic Voltage and Frequency Scaling Measurements

Fig. 8 presents measurements of the dynamic voltage and dynamic frequency scaling of this design. The top three overlaid traces are the SOC I/O power, the SOC logic power and the total SOC power. The middle trace is the SOC logic supply voltage. The bottom trace is an indicator which toggles when a fixed number of Dhrystone loops have been executed.

In the scenario shown in Fig. 8, initially the logic supply is at 1.8 V and the frequency is set at 266 MHz. In anticipation of lower performance demands, the clock and power management software modifies the PLL output divider value, which results in a decrease in frequency to 66 MHz at time t1. The change in frequency of the Dhrysone indicator is apparent. The effect of this frequency scaling is indicated in the top traces; the logic power falls by about 70%. The logic supply voltage is then lowered from 1.8 to 1 V over approximately 400 $\mu$s. During this change, the execution of Dhrystones is uninterrupted. The only change is a significant drop in power consumption, as shown following time t2 in the top traces. Finally, anticipating an increase in demand, the logic supply is raised to 1.8 V without interrupting execution and the clock and power management software raises the frequency via a write to the PLL control register at times t3 and t4, respectively. The mechanisms described provide full software control over the PLL and external DC/DC. These measurements were for a nominal part at room temperature executing Dhrystones under Linux. Logic supply slew rates in excess of 10 mV/$\mu$s have been verified.

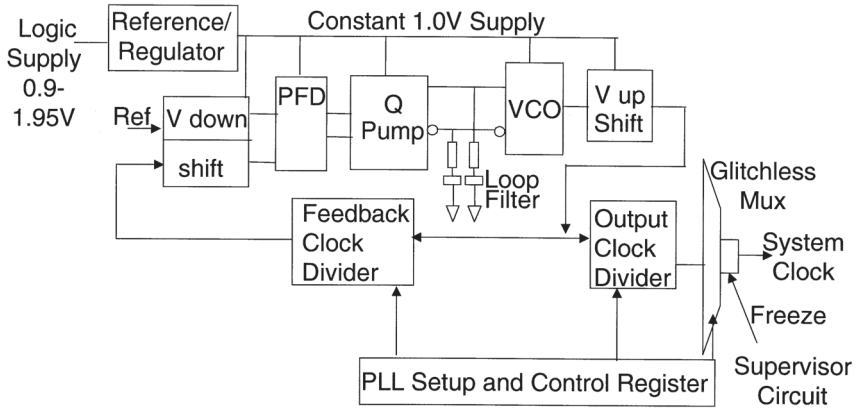


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

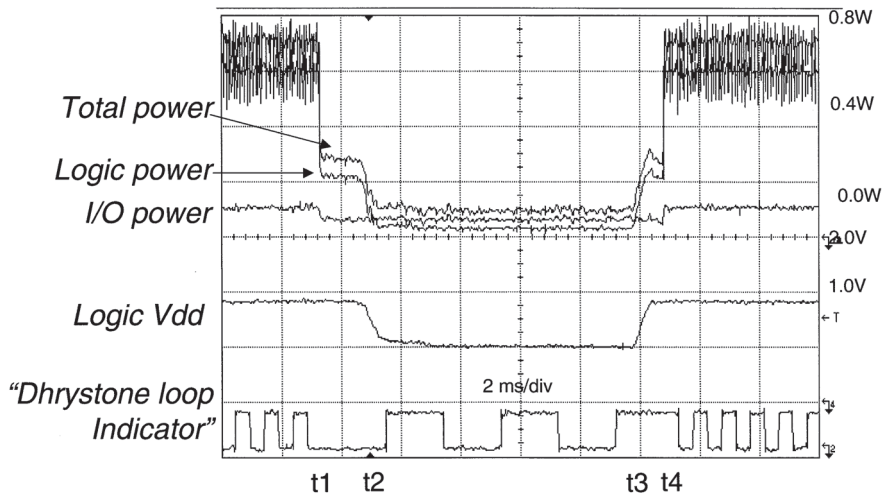


Fig. 8. Dynamic voltage and frequency scaling traces.

## VI. Active Power Management

The ability to change the output clock divider on-the-fly, without pausing the processor, allows the SOC to operate over an extremely broad range of frequencies. This allows the power consumption to be determined by the system on a very fine time scale. After dynamic voltage scaling, this dynamic frequency scaling mechanism is the second method used to reduce the active power of this processor.

Active power of the SOC can be further reduced through modification of the clock frequency within the individual cores. Cores receive clocks whose frequency is derived from the processor clock through clock dividers. The clock dividers are controlled by register values. The hazard-free clock dividers allow the clocks to the cores to be modified dynamically and individually.

Operating latches and circuits, which are not necessary for the execution of the application obviously wastes energy. Avoiding unnecessary switching lowers the dynamic power consumption of the device and extends battery life. This processor uses both fine-grained and coarse-grained disabling of inactive functions. Dynamic power is saved in this design by gating off inactive latches [12] and units. Approximately 80% of the processor registers and 50% of the SOC core registers are functionally clock gated when they are not accessed. At a higher level, the clocks to individual functional cores can also be frozen by the clock and power management software. This is done either in response to inactivity or through a force condition by the clock and power manager.

Through voltage and frequency scaling and clock gating, the performance/watt of this design can be varied by more than a factor of four. For key tasks, additional performance and power efficiency can be achieved through the use of dedicated hardware accelerators. IBM's Core Connect technology allows integration of semicustom synthesized cores and custom hard-cores into an SOC. The performance advantages of an accelerator can be extended to active power reductions if the additional performance allows both the core and the processor to be operated at a lower voltage and/or frequency. Hardware accelerators developed for this SOC include a speech recognition accelerator, a DES accelerator and an instruction stream decompression accelerator. The speech accelerator performs the speech-labeling algorithm for acoustic modeling in speech recognition applications. The cryptography core is a bulk encryptor/decryptor for DES and triple-DES algorithms. The instruction decompression accelerator performs inline tag/index decompression on a Codepack compressed instruction image [13].

Finally, the system-on-a-chip integration itself achieves a significant active power savings. A 32-bit off-chip bus access can consume as much energy as switching more than a million logic transistors. Therefore, full integration of all functionality is crucial for battery-powered systems.

## VII. Standby Power Management

Static power due to reverse-biased junction current, subthreshold leakage, gate leakage and analog current sources can limit the operating lifetime of battery-powered systems. Decreasing the standby power of the IC increases shelf-life as well as overall energy efficiency. The clock freezing and voltage-scaling capabilities of the logic domain are used to decrease the power consumption of the clock and power manager and to lower leakage. In this design, only a small sleep and clock manager is kept active during sleep. Several modes of standby operation are employed to achieve a range of standby power levels.

This design supports three classes of standby: Freeze, Hibernation and "Cryo" modes. In Freeze mode the system clock is stopped and the logic supply is decreased to its minimum value of 1.0 V. The entire state of the SOC is maintained in place. In this mode, leakage power and the power of the sleep and clock manager are consumed. Recovery from this state requires the sleep manager and clock to perform a register write, which takes about a microsecond.

In Hibernation mode, the logic supply to the processor, caches and the SOC cores is disconnected. Only the software state is maintained. This mode eliminates the leakage component of the standby power, but requires an O.S. reboot to recover. In the Cryo mode, the state of latches and register arrays in the processor core and SOC cores is transferred to nonvolatile storage prior to disconnecting the logic supply. In this way, rather than a reboot, the entire register state of the SOC can be restored prior to reactivating the system. Like the Hibernation mode, this mode avoids the leakage component of standby power.

Fig. 9 presents measured data that indicate the importance of lowering the supply voltage during Freeze mode. In Freeze mode with the voltage-controlled oscillator of the PLL active, lowering the supply from 1.8 to 0.9 V cuts the SOC standby power from 5 to 1.3 mW. Disabling the VCO lowers these numbers to 800 $\mu$W and 300 $\mu$W, respectively. The battery-backed logic in the sleep and clock manager consumes approximately 54 $\mu$W in both these situations.

The on-chip clock and power supervisor, in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to control the standby power. During Freeze mode, the supervisor software first sets a low operating frequency and then lowers the supply. The suspend controller turns off the system clocks and waits for a wakeup event—either a timeout or interrupt at which point it restores the clocks and adjusts the voltage and frequency. During Cryo mode, the software invalidates the SRAM arrays and puts the SDRAM in self-refresh mode. The suspend controller stops the clocks, freezes the I/O drivers, scans the register state out through the IIC interface to nonvolatile storage, removes logic power and waits for a wakeup event at which time it restores the supply, restores the state and restarts the clocks. Hibernation mode is similar without the register state save/restore. These modes can reduce standby power to about 300 $\mu$W in Freeze mode and 54 $\mu$W in Cryo mode.

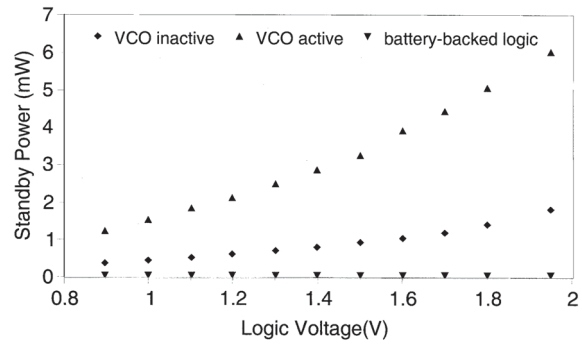


Fig. 9. Standby power reduction measurements.

## VIII. Summary

This 5.8 million transistor, 36 mm$^2$ PowerPC processor is optimized for energy efficiency. It makes use of system-on-a-chip technology to integrate the full set of devices and interfaces demanded by the battery-powered mobile market, thereby eliminating power inefficient off-chip interfaces. Under software control, both the voltage and the frequency of the processor can be modified, thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption. Unused storage and functions are not clocked, eliminating unnecessary energy consumption. This processor, under software control, can enter both a low-leakage sleep state and a state-preserving deep-sleep state to minimize standby power consumption. By applying these techniques, frequencies as high as 380 MHz can be achieved and active power consumption as low as 53 mW can be achieved, thereby dynamically adapting to the changing needs for performance and power demanded by the applications.

## Acknowledgment

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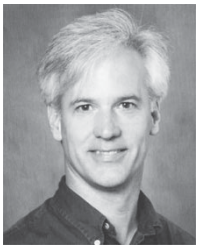

**Jeffrey L. Burns** received the B.S. degree in engineering from UCLA and the M.S. and Ph.D. degrees in electrical engineering from University of California at Berkeley

In late 1988 he joined the IBM T.J. Watson Research Center as a Research Staff Member where he worked in the areas of layout compaction, layout synthesis for control logic, CAD system architecture and microprocessor design. Since April 1996 he has been with the IBM Austin Research Laboratory, Austin, TX, where he worked initially on high-frequency microprocessor design and design-tools strategy. At present he manages the Exploratory VLSI Design department of the Austin Research Lab. His research interests are in the areas of high-end microprocessors, ultra-low-power embedded processors and high-bandwidth data communications.

Dr. Burns received an IBM Outstanding Technical Achievement Award in 1997 for his microprocessor tools and design work for IBM's S/390 products and an IBM Research Division Award for his work on IBM's 1.0-GHz PowerPC prototype disclosed in 1998.