



PowerPC 603 Microprocessor Power Management

Addressing the need for long battery life in portable applications and environmental concerns about energy consumption requires microprocessors with low power consumption as well as high performance. A primary design goal of the PowerPC 603 microprocessor was to provide sophisticated power management without compromising next-generation performance. As a result, the 603 is ideal for portable applications such as laptop computers in addition to Energy Star compliant desktop computers. The PowerPC 603 allows the system designer to control energy consumption through both hardware and software means as well as providing automatic internal power management.

PowerPC 603 Features

The 603 contains numerous power management (PM) features:

- 0.5 μ m four-layer metal CMOS process
- 3.3V power supply
- 5V or 3.3V compatible inputs
- Functional units can be dynamically powered up and down
- Four power states
- Fully static design
- Reduced-pinout mode
- 64-bit or 32-bit data bus

Dynamic Power Management

A sophisticated feature of the PowerPC 603 is dynamic power management (DPM), which automatically powers up and down the individual execution units on the chip, based on the contents of the instruction

stream. For example, if no floating-point instructions are being executed, the floating-point unit is automatically powered down. Power is not actually removed from the execution unit; instead, each execution unit has an independent clock input, which is automatically controlled on a clock-by-clock basis. Since CMOS circuits consume negligible power when they are not switching, stopping the clock to an execution unit effectively eliminates its power consumption. Setting a bit in an internal hardware register enables DPM.

Static Power States

The most unique feature of the 603 is the inclusion of four power states: Full On, Doze, Nap, and Sleep. Software selects these modes by setting one (and only one) of the three

power-saving mode bits. The 603 provides a separate interrupt and interrupt vector for power management: the System Management Interrupt (SMI). The 603 also contains a decrement timer that allows it to enter the Nap or Doze mode for a predetermined amount of time and then return to Full On operation through the Decrementer interrupt (DI). Note that the 603 cannot switch from one power management mode to another without first returning to Full On mode. The Nap and Sleep modes disable bus snooping; therefore a hardware handshake is provided to ensure data cache coherency before the 603 enters these power management (PM) modes. Table 1 summarizes the four power states, which are further detailed in the following paragraphs.

Table 1. PowerPC 603 power management states

PM mode	Functioning units	Activation method	Full On Wake Up method
Full On (with DPM)	Requested logic by demand		
Doze	Bus snooping Data cache as needed Decrementer timer	Controlled by software	External asynchronous interrupts Decrementer interrupts Reset
Nap	Decrementer timer	Controlled by hardware and software	External asynchronous interrupts Decrementer interrupts Reset
Sleep	None	Controlled by hardware and software	External synchronous interrupts Reset

Full On without DPM. Full On mode without DPM provides:

- Default state
- All functional units are operating at full processor speed at all times

Full On with DPM enabled. Full On mode with DPM provides on-chip power management without affecting the functionality or performance of the PowerPC 603.

- Required functional units are operating at full processor speed
- Functional units are clocked only when needed
- No software or hardware intervention required after mode is set
- Software/hardware and performance transparent

Doze. Doze mode disables most functional units but maintains data cache coherency by enabling the bus interface unit and snooping. A snoop hit will cause the PowerPC 603 to enable the data cache, copy the data back to memory, and then disable the cache.

- Most functional units disabled
- But snooping and time base/decrementer still enabled
- Several methods of returning to Full On mode
 - assert INT, SMI, or DI interrupts
 - hard or soft reset
- Transition to Full On state takes no more than a few processor cycles
- PLL running and locked to SYSCLK

Nap. The Nap mode disables the PowerPC 603 but still maintains the Phase Locked Loop (PLL) and the decrement timer. The timer can be used to wake up after a programmed amount of time. Because bus snooping is disabled for Nap and Sleep mode, a hardware handshake using the Quiesce request and acknowledge signals are required to maintain data cache coherency (see Sleep mode).

- Time base/decrementer still enabled
- Most functional units disabled (including bus snooping)
- All nonessential input receivers disabled
- Several methods of returning to Full On mode
 - assert INT, SMI, or DI interrupts
 - hard or soft reset
- Transition to Full On takes no more than a few processor cycles
- PLL running and locked to SYSCLK

Sleep. Sleep mode consumes the least amount of power of the four modes, since all functional units are disabled. To conserve the maximum amount of power, the PLL may be disabled and the SYSCLK may be removed. Before the PowerPC 603 enters the Nap or Sleep mode, the 603 will assert the QREQ signal to indicate that it is ready to disable bus snooping. When the system has ensured that snooping is no longer necessary, it will assert QACK and the

PowerPC 603 will enter the Sleep or Nap mode.

- All functional units disabled (including bus snooping and time base)
- All nonessential input receives disabled
 - Internal clock regenerators disabled
 - PLL still running (see following)
- Sleep mode sequence
 - set Sleep bit
 - 603 asserts quiesce request (QREQ_)
 - system asserts quiesce acknowledge (QACK_)
 - 603 enters sleep mode after several processor clocks
- Several methods of returning to Full On mode
 - assert INT or SMI interrupts
 - hard or soft reset
- PLL may instead be disabled and SYSCLK may be removed while in Sleep mode
- Return to Full On mode after PLL and SYSCLK disabled in Sleep mode
 - enable SYSCLK
 - reconfigure PLL into desired processor clock mode
 - system logic waits for PLL start-up and relock time (100 μ sec)
 - system logic asserts one of the sleep recovery signals (e.g., INT or SMI)

Power Management Mode Transitions

The PM mode transitions are typically controlled by the operating system (OS) or by the chipset hardware.

For example, as part of the OS loading/start-up process, one of the power-saving modes is selected by setting the appropriate power management mode bits. The proper power management mode is selected on the basis of whether any other devices will be performing DMA transfers that need to be snooped by the 603. If no snooping action is required, then Nap mode is chosen, otherwise Doze mode is used. If the time base is not needed either, or if its proper setting can be determined from an external source (such as a real-time clock) then the Sleep mode can be selected, offering the lowest power consumption. After setting the proper power management bit and creating whatever start-up processes are deemed necessary, the OS then creates a new low(est) priority process (an "idle" process). Now, when all the other processes are idle, this low priority process (or thread) is executed, placing the 603 in the selected power-down mode. Whenever the OS time counter (either the internal Time Base/Decrementer or an external countdown timer) expires and interrupts the processor, the 603 switches to Full On mode and processes the interrupt service routine. The interrupt service routine calls the OS scheduler to update priorities. If no other processes are active yet, the 603 then returns to the "idle" process and enters the low-power mode.

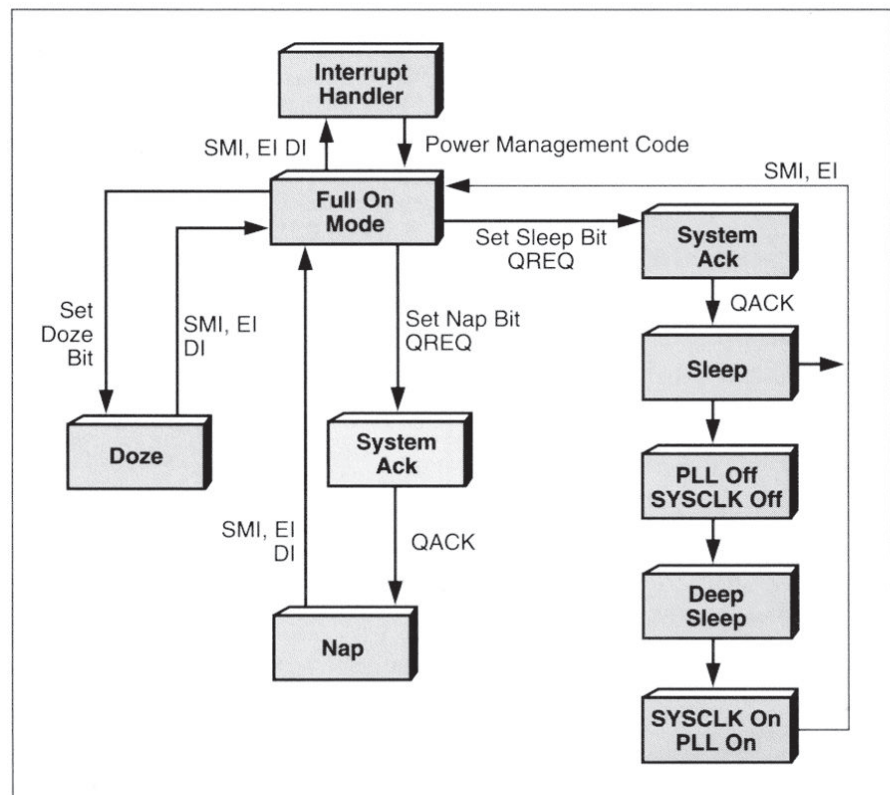
Another possible method is to rely on the PC chipset to monitor the bus activity of the 603 (similar to how most x86-based PCs currently operate). When activity timers in the chipset detect no activity by the system's components for a predetermined length of time, the chipset generates a SMI interrupt. In the interrupt handler for this routine, the 603 checks the interrupt status register in the chipset, indicating whether the interrupt was caused by a CPU or a peripheral activity timer expiring. If it was a CPU activity timer expiring, the 603 calls a routine that checks the status of the scheduler to decide whether or not the 603 was truly inactive (the 603 could have been simply executing a tight loop whose code and data spaces fit inside the on-chip caches). If the 603 was indeed inactive, the routine would then place the

Table 2. Typical power consumption

PM Mode	Frequency (Internal)		
	50 MHz	66 MHz	80 MHz
Full On no DPM	1.78 W	2.18 W	2.54 W
Full On with DPM	1.52 W	1.89 W	2.20 W
Doze	242 mW	307 mW	366 mW
Nap	89 mW	113 mW	135 mW
Sleep	66 mW	89 mW	105 mW
Sleep no PLL	15 mW	18 mW	19 mW
Sleep no PLL on SYSCLK	<5 mW	<5 mW	<5 mW

Table 3. 603 Performance

Benchmark	Frequency (Int/Ext) in MHz		
	50/50	60/66	80/40
SPECint92	47	60	75
SPECfp92	53	70	85

**Figure 1.** PowerPC 603 power management mode transitions

603 in one of the PM modes, after checking the power status of the other peripherals in the system. It should be placed into the doze mode if any other peripherals with DMA capability are still powered up. If no other peripherals with DMA capability are powered up, or it is known that no DMA activity will take place, then the 603 can be placed into either Nap or Sleep mode.

The power management mode transitions of the PowerPC 603 are shown graphically in Figure 1. Depending on the power management scheme used, a decremter interrupt, SMI, or external interrupt (EI) invokes the interrupt handler routine. To enter the Doze mode, the doze bit is set. The PowerPC 603 will remain in Doze mode until an interrupt returns it to Full On mode. The PowerPC 603 then invokes the interrupt handler to determine its next action.

Transitioning to Nap mode requires a hardware handshake, since the PowerPC 603 will not enforce data cache coherency in this mode. Once the nap bit has been set and the PowerPC 603 is ready to Nap, it indicates this by asserting QREQ. When the system has assured that snooping is no longer required, it asserts QACK. This allows the system to control when the PowerPC 603 actually enters Nap mode.

Sleep mode also requires a QACK from the system before it is entered. Since the decremter timer is not functioning in Sleep mode, only a SMI or EI will wake the part up. To conserve the maximum amount of power, it is also possible to put the PowerPC 603 into Deep Sleep by first turning off the PLL and then the SYSCLK. Before the PowerPC 603 can recognize the SMI or EI, the SYSCLK must be reapplied and then the PLL must be turned on.

32-bit data bus mode and reduced-pinout mode. The 603 supports an optional 32-bit data bus mode which is configured at reset. This mode breaks a 64-bit data access into two 32-bit bus transactions. In addition, the 603 offers a reduced pinout mode to lower power consumption (by idling the switching of numerous pins) while the 603 is running in 32-bit data bus mode.

PowerPC 603 power consumption.

How all these power management features benefit the portable system designer is perhaps illustrated more clearly by the (preliminary) typical power consumption figures given in Table 2.

Power PC 603 performance estimates. Table 3 lists the simulated benchmark results for the 603, assuming a 1MB second-level cache.

Summary

The power management features of the PowerPC 603 enable portable systems designers to provide enhanced performance for portable computers while conserving energy. ■

References

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In this article, the terms "PowerPC 603 Microprocessor" and "603" are used to denote the second microprocessor from the PowerPC Architecture family.

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