AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Eastern District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:11-cv-173	04/07/2011	for the Eastern District of Texas

PLAINTIFF	DEFENDANT
MOSAID TECHNOLOGIES, INC.	FREESCALE SEMICONDUCTOR, INC. ET AL.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,051,306		See Attached List
2	7,415,680		
3	5,577,230		
4	5,724,505		
5	5,958,036		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,141,762		
2 6,256,725		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,051,306 B2
APPLICATION NO. : 10/840893
DATED : May 23, 2006
INVENTOR(S) : Barry Alan Hoberman et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 14, Claim 12, line 6, before “comprises” insert --actions--.

In Column 14, Claim 13, line 13, after “one of the” insert --actions--.

Signed and Sealed this
Twenty-first Day of June, 2011

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee : Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell

Patent No.: 7,051,306 B2 Issued: May 23, 2006

Title: Managing Power On Integrated Circuits Using Power Islands

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

Date Signature

Typed or printed name of person signing certificate

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
Office of Patent Publication
ATTN: Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 35 U.S.C. § 254, we hereby request that a Certificate of Correction be issued for the above-referenced U.S. Letters Patent to correct errors as shown on the attached PTO/SB/44 form.

Since the errors were made by the U.S. Patent and Trademark Office and not by Patentee or Patentee's Attorney/Agent, it is understood that there are no additional fees are due for the requested Certificate of Correction.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No.: 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: May 25, 2011

1093986.1

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,051,306 B2

APPLICATION NO.: 10/840,893

ISSUE DATE : May 23, 2006

INVENTOR(S) : Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 14, Claim 12, line 6, before "comprises" insert --actions--.

In Column 14, Claim 13, line 13, after "one of the" insert --actions--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):
Hamilton, Brook, Smith & Reynolds, P.C.
530 Virginia Road P.O. Box 9133
Concord, MA 01742-9133

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	10165953
Application Number:	10840893
International Application Number:	
Confirmation Number:	8273
Title of Invention:	MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-001
Receipt Date:	25-MAY-2011
Filing Date:	07-MAY-2004
Time Stamp:	15:41:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	20372079001_Req_Cert_Corr.pdf	645995 d9219338962086563d5e4178435707c3c3c4f18c	no	2

Warnings:

Information:

Total Files Size (in bytes):	645995

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/840,893	05/07/2004	Barry Alan Hoberman	2037.2079-001

CONFIRMATION NO. 8273

POA ACCEPTANCE LETTER

21005
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

OC000000034862083

Date Mailed: 03/10/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/24/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/vvan/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/840,893	05/07/2004	Barry Alan Hoberman	ISSUED

CONFIRMATION NO. 8273

POWER OF ATTORNEY NOTICE

59893
EATON PEABODY PATENT GROUP, LLC
P.O. BOX 5249
77 Sewall Street, Suite 3000
AUGUSTA, ME 04332-5249

OC000000034862034

Date Mailed: 03/10/2009

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/24/2009.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/vvan/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

OIPE IAP21
FEB 2 4 2009
PATENT & TRADEMARK OFFICE

#10840893

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY and CHANGE OF CORRESPONDENCE ADDRESS		
	Application/Patent Number	7,051,306
	Filing/Issue Date	May 23, 2006
	First Named Inventor/Patentee	Barry Alan Hoberman
	Confirmation Number	8273
	Group Art Unit	2825
	Examiner Name	Sun J. Lin
	Attorney Docket Number	2037.2079-001

Title MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ I hereby appoint the following practitioner(s): [Not to exceed 10]

OR

☒ I hereby appoint the practitioners associated with the Customer Number: **021005**

Please change the correspondence address for the above-identified application to:

☒ **Customer Number 021005**
Hamilton, Brook, Smith & Reynolds, P.C.
530 Virginia Road
P.O. Box 9133
Concord, Massachusetts 01742-9133

☐ Other

Please direct all telephone calls and facsimiles to:

Name James M. Smith, Esq. Tel. No. 978-341-0036 Fax No. 978-341-0136

I am the:

☐ Applicant/Inventor.

☒ Authorized representative of the Assignee, MOSAID Technologies Corporation, of the entire interest. See 37 CFR § 3.71. A Statement under 37 CFR § 3.73(b) is enclosed.

☐ Authorized representative of the Assignee, [FILL IN WITH NAME OF ASSIGNEE], together with [FILL IN WITH NAME OF ASSIGNEE], of the entire interest. A Statement under 37 CFR § 3.73(b) is enclosed.

SIGNATURE of Applicant or Assignee of Record

Signature	
Name & Title	Phil Shaer - Secretary
Date	February 11, 2009

862245_1

OIPE IAP21
FEB 2 4 2009
PATENT & TRADEMARK OFFICE

Docket No. 2037.2079-001

STATEMENT UNDER 37 CFR § 3.73(b)

Applicant/Patentee: Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell

Application No./Patent No.: 7,051,306 Filed/Issue Date: May 23, 2006

For: MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS

MOSAID Technologies Corporation, a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is

A. ☒ the assignee of the entire right, title and interest in the patent application identified above; or

B. ☐ an assignee together with [ ] of the entire right, title and interest in the patent application identified above.

The right, title and interest of the above-named assignee in the patent application identified above is established by virtue of:

A. ☐ An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel [ ], Frame [ ], or a copy thereof is attached.

OR

B. ☒ A chain of title from the inventor(s) of the patent application identified above, to the current assignee as shown below:

1. From: Barry Alan Hoberman, Daniel L. Hillman & Jon Shiell
To: Virtual Silicon Technology, Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel 015345, Frame 0829-0831, or a copy thereof is attached.

2. From: Virtual Silicon Technology, Inc. To: MOSAID Delaware, Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel 017100, Frame 0155-0159, or a copy thereof is attached.

3. From: MOSAID Delaware, Inc. To: MOSAID Technologies Corporation
The document was recorded in the United States Patent and Trademark Office at
Reel 017203, Frame 0427-0429, or a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

Name: Phil Shaer

Title: Secretary

Date: February 11, 2009

862249_1

862265_1
JMS/cmm/(aeg)
February 18, 2009

PATENT APPLICATION
Docket No.: PA2258-US (2037.2079-001)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell

Patent No.: 7,051,306 Group: 2825

Issued: May 23, 2006 Examiner: Sun J. Lin

Confirmation No.: 8273

For: MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS

OIPE IAP21
FEB 24 2009
PATENT & TRADEMARK OFFICE

CERTIFICATE OF MAILING OR TRANSMISSION
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

2-20-09 Amy Green
Date Signature

Amy Green
Typed or printed name of person signing certificate

REQUEST FOR CHANGE OF DOCKET NUMBER AND CORRECTED FILING RECEIPT

Customer Correction Office
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant's attorney requests that the docket number of record for the above-referenced case be changed to 2037.2079-001. This request is made to better identify this application within our offices. Please provide a corrected Filing Receipt indicating the new attorney docket number.

Please charge Deposit Account No. 08-0380 for any fees that may be due in this matter.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By
James M. Smith
Registration No.: 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: 2/18/9

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US

CONFIRMATION NO. 8273

POA ACCEPTANCE LETTER

59893
EATON PEABODY PATENT GROUP, LLC
P.O. BOX 5249
77 Sewall Street, Suite 3000
AUGUSTA, ME 04332-5249

OC000000030948813

Date Mailed: 07/15/2008

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/07/2008.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hchristian/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US

CONFIRMATION NO. 8273

POWER OF ATTORNEY NOTICE

22830
CARR & FERRELL LLP
2200 GENG ROAD
PALO ALTO, CA 94303

OC000000030948781

Date Mailed: 07/15/2008

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/07/2008.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/hchristian/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/81 (01-06)
Approved for use through 12/31/2008. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION FORM

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Hoberman
Title	Managing Power on Integrated ...
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☑ Practitioners associated with the Customer Number: 59893

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☑ The address associated with the above-mentioned Customer Number:

OR

☐ The address associated with Customer Number: 59893

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/Inventor.

☑ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature		Date	July 3, 2008
Name	Phillip Shaer	Telephone	(613) 599-9539
Title and Company	Secretary, MOSAID Technologies Corporation		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 2 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (01-08)
Approved for use through 07/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Barry Hoberman/MOSAID Technologies Corporation

Application No./Patent No.: 10/840,893/7,051,306 Filed/Issue Date: May 7, 2004

Entitled: MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS

MOSAID Technologies Corporation, a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☑ the assignee of the entire right, title, and interest; or

2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is_____ %)

in the patent application/patent identified above by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Barry Hoberman/Daniel Hillman/Jon Shiell To: Virtual Silicon Technology, Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel 015345, Frame 0829, or for which a copy thereof is attached.

2. From: Virtual Silicon Technology, Inc. To: MOSAID Delaware, Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel 017100, Frame 0155, or for which a copy thereof is attached.

3. From: MOSAID Delaware, Inc. To: MOSAID Technologies Corporation
The document was recorded in the United States Patent and Trademark Office at
Reel 017203, Frame 0427, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☑ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	July 3, 2008 Date
Phillip Shaer Printed or Typed Name	(613) 599-9539 Telephone Number
Secretary Title	

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	3570738
Application Number:	10840893
International Application Number:	
Confirmation Number:	8273
Title of Invention:	MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	22830
Filer:	Dennis R. Haszko
Filer Authorized By:	
Attorney Docket Number:	PA2258US
Receipt Date:	07-JUL-2008
Filing Date:	07-MAY-2004
Time Stamp:	12:26:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	00354080.PDF	288938 3020158292ead72a3c3f9ff5d82883b891fdfad9c	no	1

Warnings:

Information:

2	Assignee showing of ownership per 37 CFR 3.73(b).	00354083.PDF	371013 5911d6e8322fba624b3a2e96350f3b19a38041e1	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	659951	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

OIPE IAP78
JUN 2 7 2008
PATENT & TRADEMARK OFFICE

DPW

PTO/SB/21 (01-08)
Approved for use through 02/29/2008. OMB 0651-0031
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 9

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please identify below):

1) Confirmation Postcard;
2) Request for Withdrawal as Attorney (2ppx3);
3) Copy of Client Correspondence (2pp).

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Carr & Ferrell LLP Cust. No. 22830		
Signature	Ron Rohde		
Printed name	Ronald L. Rohde		
Date	June 24, 2008	Reg. No.	45,050

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Ron Rohde		
Typed or printed name	Ronald L. Rohde, Reg. No. 45,050	Date	June 24, 2008

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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JUN 27 2008
PATENT & TRADEMARK OFFICE

Doc Code: PET.STATUS
Document Description: Petition for review/processing depending on status.

PTO/SB/83 (04-08)
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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please withdraw me as attorney or agent for the above identified patent application, and

- [ ] all the practitioners of record;
- [ ] the practitioners (with registration numbers) of record listed on the attached paper(s); or
- [x] the practitioners of record associated with Customer Number: 22830

NOTE: The immediately preceding box should only be marked when the practitioners were appointed using the listed Customer Number.

The reason(s) for this request are those described in 37 CFR :

[ ] 10.40(b)(1)	[ ] 10.40(b)(2)	[ ] 10.40(b)(3)	[x] 10.40(b)(4)
[ ] 10.40(c)(1)(i)	[ ] 10.40(c)(1)(ii)	[ ] 10.40(c)(1)(iii)	[ ] 10.40(c)(1)(iv)
[ ] 10.40(c)(1)(v)	[ ] 10.40(c)(1)(vi)	[ ] 10.40(c)(2)	[ ] 10.40(c)(3)
[ ] 10.40(c)(4)	[ ] 10.40(c)(5)	[ ] 10.40(c)(6) Please explain below:	

Certifications

Check each box below that is factually correct. WARNING: If a box is left unchecked, the request will likely not be approved.

1. [x] I/We have given reasonable notice to the client, prior to the expiration of the response period, that the practitioner(s) intend to withdraw from employment.

2. [x] I/We have delivered to the client or a duly authorized representative of the client all papers and property (including funds) to which the client is entitled.

3. [x] I/We have notified the client of any responses that may be due and the time frame within which the client must respond.

Please provide an explanation, if necessary:

Client has discharged the above attorneys of record associated with customer number 22830.

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Change the correspondence address and direct all future correspondence to:

A. ☐ The address of the inventor or assignee associated with Customer Number: _____

OR

B. ☑ Inventor or Assignee name	MOSAID Technologies Corporation		
Address 11 Hines Road			
City Kanata	State Ontario	Zip K2K 2X1	Country Canada
Telephone		Email	

I am authorized to sign on behalf of myself and all withdrawing practitioners.

Signature	Ron Rohde		
Name	Ronald L. Rohde	Registration No. 45,050	
Address 2200 Geng Road			
City Palo Alto	State CA	Zip 94303	Country USA
Date	June 24, 2008	Telephone No. 650-812-3400	

NOTE: ***Withdrawal is effective when approved rather than when received.***

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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OIPE JUN 27 2008 PATENT & TRADEMARK OFFICE

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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please withdraw me as attorney or agent for the above identified patent application, and

- [ ] all the practitioners of record;
- [ ] the practitioners (with registration numbers) of record listed on the attached paper(s); or
- [x] the practitioners of record associated with Customer Number: 22830

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[ ] 10.40(b)(1)	[ ] 10.40(b)(2)	[ ] 10.40(b)(3)	[x] 10.40(b)(4)
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Certifications

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Address 11 Hines Road			
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Telephone		Email	

I am authorized to sign on behalf of myself and all withdrawing practitioners.

Signature	Ron Rohde		
Name	Ronald L. Rohde	Registration No. 45,050	
Address 2200 Geng Road			
City Palo Alto	State CA	Zip 94303	Country USA
Date	June 24, 2008	Telephone No. 650-812-3400	

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Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

To: Commissioner for Patents
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Alexandria, VA 22313-1450

Please withdraw me as attorney or agent for the above identified patent application, and

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Telephone		Email	

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Signature	Ron Rohde		
Name	Ronald L. Rohde	Registration No. 45,050	
Address 2200 Geng Road			
City Palo Alto	State CA	Zip 94303	Country USA
Date	June 24, 2008	Telephone No. 650-812-3400	

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OIPE
JUN 27 2008
PATENT & TRADEMARK OFFICE

CARR & FERRELL LLP
ATTORNEYS AT LAW

WRITER'S DIRECT DIAL NUMBER
(650) 812-3487
RRohde@CarrFerrell.com

June 24, 2008

Daniel A. Hammond
MOSAID Technologies Incorporated
11 Hines Road
Kanata, Ontario K2K 2X 1
Canada

Your Reference	C&F Reference	Serial Number	Title	Filing Date
1181-02US-000-70	PA2258US	10/840,893	Managing Power on Integrated Circuits Using Power Islands	May 7, 2004
1185-02US-000-70	PA3286US	11/433,158	Integrated Circuit with Signal Bus Formed by Cell Abutment of Logic Cells	May 12, 2006
1188-01US-000-70	PA3578US	11/400,495	Phase-Locked Loop Filter Capacitance with a Drag Current	April 6, 2006

Dear Daniel:

As new counsel has been found to prosecute the above-referenced matters, a *Request for Withdrawal as Attorney or Agent and Change of Correspondence Address* was filed in the above-referenced matters on **June 24, 2008**. Per USPTO requirements, we listed the new correspondence address as the address of MOSAID Technologies Incorporated, which is the currently recorded assignee for all of the above-referenced matters. We will, of course, forward any correspondence that may be misdirected to us in the interim. We request that Dennis Hazsko file the necessary documents to change the correspondence address and power of attorney for these matters.

Please be advised that there is a risk of losing rights in the above-referenced patent applications if the new counsel does not respond to future communications from the Patent Office in a timely manner.

Sincerely,

Ronald L. Rohde

RLR:pxt
cc: Victoria Donnelly

Encl.: Request for Withdrawal (3)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US	8273

22830 7590 04/17/2006

CARR & FERRELL LLP
2200 GENG ROAD
PALO ALTO, CA 94303

EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

10/840893

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT	PAPER
	04132006

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

(1) Applicants's submitted IDS filed on 01/23/2006 has been reviewed (2) a copy of signed PTO 1449 Form is enclosed.

PTO Sun J Lin
Primary Examiner
Art Unit: 2825

PTO-90C (Rev.04-03)

OIPE IAP79
JAN 2 3 2006
PATENT & TRADEMARK OFFICE

PTO/SB/08B (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

	Complete if Known
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
JSR		HALTER et al., "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits", in Proc. IEEE Custom Integrated Circuits Conf., 1997, pp. 475-478.	
JSR		HORIGUCHI et al., "Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's", IEEE Journal of Solid-State Circuits, November 1993, Vol.28, No. 11.	
JSR		KAO et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits", IEEE Journal of Solid-State Circuits, July 2000, Vol. 35, No. 7.	
JSR		MUTOH, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS", IEEE Journal of Solid-State Circuits, August 1995, Vol. 30, No. 8.	

Examiner Signature	James Sun Lin	Date Considered	4-13-06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Complete and send this form, together v applicable fee(s), to: Mail Mail Stop ISS FEE
Commissioner .. / Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22830 7590 10/20/2005

CARR & FERRELL LLP
2200 GENG ROAD
PALO ALTO, CA 94303

01/24/2006 HTECKLU2 00000034 10840893

01 FC:1501 1400.00 OP
02 FC:1504 300.00 OP

OIPE IAP35 JAN 23 2006 PATENT & TRADEMARK OFFICE

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Eugene G. Kim (46267) (Depositor's name)
(Signature)
January 20, 2006 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US	8273

TITLE OF INVENTION: MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	01/20/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIN, SUN J	2825	716-006000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Carr & Ferrell LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

MOSAID Technologies Corporation Sunnyvale, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):
☒ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 06-0600 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date January 20, 2006

Typed or printed name Eugene G. Kim Registration No. 46,267

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

OIPE IAP35 JAN 23 2006 PATENT & TRADEMARK OFFICE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US
Total Number of Pages in This Submission	5

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
  - [✓] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [✓] Other Enclosure(s) (please Identify below):

1) Confirmation postcard;
2) PTOL-85 (x2);
3) Check for $1700

Remarks

Total page number does not include postcard.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Carr & Ferrell LLP Cust. No. 22830		
Signature	Eugene Kim		
Printed name	Eugene G. Kim		
Date	January 20, 2006	Reg. No.	46,267

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Eugene Kim		
Typed or printed name	Eugene G. Kim, Reg. No. 46,267	Date	January 20, 2006

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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OIPE IAP33
JAN 23 2006
PATENT & TRADEMARK OFFICE

PTO/SB/17 (12-04)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL For FY 2005

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1,700.00

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Examiner Name	Sun J. Lin
Art Unit	2825
Attorney Docket No.	PA2258US

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 06-0600 Deposit Account Name: Carr & Ferrell LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
☐ Charge fee(s) indicated below, **except for the filing fee**
☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17
☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims _____ - 20 or HP = _____ **Extra Claims** x **Fee ($)** _____ = **Fee Paid ($)** _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims _____ - 3 or HP = _____ **Extra Claims** x **Fee ($)** _____ = **Fee Paid ($)** _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims **Fee ($)** _____ **Fee Paid ($)** _____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets _____ - 100 = _____ **Extra Sheets** / 50 = _____ **Number of each additional 50 or fraction thereof** (round **up** to a whole number) x _____ **Fee ($)** = _____ **Fee Paid ($)**

4. OTHER FEE(S) **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount) _____

Other: Issue Fee ($1400); Publication Fee ($300) 1700

SUBMITTED BY

Signature	Eugene Kim	Registration No. (Attorney/Agent) 46,267	Telephone 650-812-3406
Name (Print/Type)	Eugene G. Kim		Date January 20, 2006

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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OIPE IAP79
JAN 2 3 2006
PATENT & TRADEMARK OFFICE

PTO/SB/21 (09-04)
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B

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	11

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
  - [✓] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [✓] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [✓] Other Enclosure(s) (please Identify below):

1) Confirmation postcard;
2) Duplicate of IDS;
3) Statement Under 37 CFR § 1.97(e)(2) (2pg)
4) PTO/SB/08 (x2);
5) Copies of 4 cited references;
6) Check for $180.00

Remarks

Total page number does not include postcard, check or cited references.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Carr & Ferrell LLP Cust. No. 22830		
Signature			
Printed name	Eugene G. Kim		
Date	January 19, 2006	Reg. No.	46,267

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Eugene G. Kim, Reg. No. 46,267	Date	January 19, 2006

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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OIPE IAP79
JAN 2 3 2006
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PTO/SB/17 (12-04)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☑ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 180.00

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Examiner Name	Sun J. Lin
Art Unit	2825
Attorney Docket No.	PA2258US

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 06-0600 Deposit Account Name: Carr & Ferrell LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee ($)		Fee Paid ($)
_____	- 20 or HP =	_____	x	_____	=	_____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims		Extra Claims		Fee ($)		Fee Paid ($)
_____	- 3 or HP =	_____	x	_____	=	_____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
_____	- 100 =	_____	/ 50 =	_____ (round up to a whole number)	x	_____	=	_____

4. OTHER FEE(S) **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount) _____

Other: Information Disclosure Statement 180

SUBMITTED BY

Signature	Eugene Kim	Registration No. (Attorney/Agent) 46,267	Telephone 650-812-3406
Name (Print/Type)	Eugene G. Kim		Date January 19, 2006

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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OIPE IAP78
JAN 2 3 2006
PATENT & TRADEMARK OFFICE

IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Barry Alan Hoberman et al.
SERIAL NO.:	10/840,893
FILED:	May 7, 2004
TITLE:	Managing Power on Integrated Circuits Using Power Islands
EXAMINER:	Sun J. Lin
GROUP ART UNIT:	2825
ATTY.DKT.NO.:	PA2258US

MAIL STOP ISSUE FEE
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
Under 37 C.F.R. §§ 1.56, and 1.97-1.98

SIR:

Pursuant to the provisions of 37 C.F.R. §§ 1.56 and 1.97-98 of the Rules of Practice in Patent Cases, enclosed herewith is form PTO-SB-08 listing several references, for which copies of the non-patent literature are enclosed. The Examiner is requested to make these references of official record in the application. The references cited may be material to examination of the application and are submitted in compliance with Applicants' duty of disclosure as defined by 37 C.F.R. § 1.56.

01/24/2006 BABRAHA1 00000053 10840893
01 FC:1806 180.00 OP

{00168814v1}

No representation is made or intended as to the completeness of this list, nor is the inclusion of any reference on this list an admission that it is prior art or pertinent to this application.

Applicants hereby attach the $180 fee required by 37 C.F.R. §1.17(p) with this submission. The Commissioner is hereby authorized to charge Deposit Account No. 06-0600 for any additional fees that may be required, or credit our account for any overpayment charge. A copy of this statement is submitted in duplicate for this purpose.

Respectfully submitted,
Barry Alan Hoberman et al.

Dated: January 19, 2006 By: _____

Eugene G. Kim, Reg. No. 46,267
Carr & Ferrell *LLP*
2200 Geng Road
Palo Alto, CA 94303
TEL: (650) 812-3400
FAX: (650) 812-3444

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date printed below:

Dated: January 19, 2006 By: _____
Eugene G. Kim, Reg. No. 46,267

{00168814v1}

O I P E IAP78
JAN 2 3 2006
PATENT & TRADEMARK OFFICE

IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Barry Alan Hoberman et al.
SERIAL NO.:	10/840,893
FILED:	May 7, 2004
TITLE:	Managing Power on Integrated Circuits Using Power Islands
EXAMINER:	Sun J. Lin
GROUP ART UNIT:	2825
ATTY.DKT.NO.:	PA2258US

MAIL STOP ISSUE FEE
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

STATEMENT UNDER 37 C.F.R. § 1.97(e)(2)

Applicants hereby state, pursuant to 37 C.F.R. § 1.97(e)(2), that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the information disclosure statement.

{00168812v1}

As such, Applicants contend this information disclosure statement and the references cited therein should be considered under 37 C.F.R. § 1.97(d).

Respectfully submitted,
Barry Alan Hoberman et al.

Dated: January 19, 2006 By: _____

Eugene G. Kim, Reg. No. 46,267
Carr & Ferrell *LLP*
2200 Geng Road
Palo Alto, CA 94303
TEL: (650) 812-3400
FAX: (650) 812-3444

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date printed below:

Dated: January 19, 2006 By: _____

Eugene G. Kim, Reg. No. 46,267

{00168812v1}

OIPE IAP79
JAN 2 3 2006
PATENT & TRADEMARK OFFICE

PTO/SB/08B (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

	Complete if Known
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		HALTER et al., "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits", in Proc. IEEE Custom Integrated Circuits Conf., 1997, pp. 475-478.	
		HORIGUCHI et al., "Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's", IEEE Journal of Solid-State Circuits, November 1993, Vol.28, No. 11.	
		KAO et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits", IEEE Journal of Solid-State Circuits, July 2000, Vol. 35, No. 7.	
		MUTOH, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS", IEEE Journal of Solid-State Circuits, August 1995, Vol. 30, No. 8.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

22830 7590 10/20/2005

CARR & FERRELL LLP
2200 GENG ROAD
PALO ALTO, CA 94303

EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/20/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US	8273

TITLE OF INVENTION: MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	01/20/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/05) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax **(571) 273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

22830 7590 10/20/2005

CARR & FERRELL LLP
2200 GENG ROAD
PALO ALTO, CA 94303

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US	8273

TITLE OF INVENTION: MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	01/20/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIN, SUN J	2825	716-006000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US	8273

22830 7590 10/20/2005

CARR & FERRELL LLP
2200 GENG ROAD
PALO ALTO, CA 94303

EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/20/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 07/05) Approved for use through 04/30/2007.

AK

Notice of Allowability	Application No.	Applicant(s)	
	10/840,893	HOBERMAN ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendments & Remarks filed on 09/26/2005*.

2. ☒ The allowed claim(s) is/are *1-5,7-21,23-43 and 45-54, renumbered (37CFR 1.126)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Applicants' attorney *Eugene G. Kim* gave authorization for this examiner's amendment on October 5, 2005. Based on Amendments filed on 09/26/2005, the application has been amended as follows:

Claim 1, line 6, change "an action" to **—at least one of actions—**.
Claim 1, line 8, change "the action" to **—the at least one of the actions—**.
Claim 1, line 10, before "one" insert **—the—**.
Claim 7, line 1, change "the action" to **—another one of the actions—**.
Claim 8, line 1, change "the action" to **—another one of the actions—**.
Claim 11, line 1, change "the action" to **—another one of the actions—**.
Claim 12, line 1, change "the action" to **—another one of the actions—**.
Claim 13, line 1, change "the action" to **—another one of the actions—**.
Claim 14, line 5, change "the action" to **—the at least one of the actions—**.
Claim 17, line 7 – 8, change "an action" to **—at least one of actions—**.
Claim 17, line 9, change "the action" to **—the at least one of the actions—**.
Claim 23, line 1, change "the action" to **—another one of the actions—**.
Claim 24, line 1, change "the action" to **—another one of the actions—**.
Claim 27, line 1, change "the action" to **—another one of the actions—**.
Claim 28, line 1, change "the action" to **—another one of the actions—**.
Claim 29, line 1, change "the action" to **—another one of the actions—**.
Claim 30, line 4, change "the action" to **—the at least one of the actions—**.
Claim 39, line 6, change "an action" to **—at least one of actions—**.
Claim 39, line 8, change "the action" to **—the at least one of the actions—**.
Claim 45, line 1, change "the action" to **—another one of the actions—**.
Claim 46, line 1, change "the action" to **—another one of the actions—**.
Claim 49, line 1, change "the action" to **—another one of the actions—**.
Claim 50, line 1, change "the action" to **—another one of the actions—**.
Claim 51, line 1, change "the action" to **—another one of the actions—**.
Claim 52, line 5, change "the action" to **—the at least one of the actions—**.

Reasons for Allowance

Claims 1 – 5, 7 – 21, 23 – 43 and 45 – 54 are allowed over the prior art of record. An examiner's statement of reasons for allowance is given in the following:

Claims 1 – 5, 7 – 21, 23 – 43 and 45 – 54 are allowed because the prior art does not teach or fairly suggest the following subject matter:

- A method/system/software product for managing power on an integrated circuit including a plurality of power islands comprises *performing at least one of actions to change a power consumption level of one of the power islands to a target power level where one of the actions comprises selecting a frequency for the one of the power islands* in combination with other limitations as recited in independent **Claim 1**, **Claim 17** and **Claim 39**, respectively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272 – 1899. The examiner can normally be reached on Monday to Friday from 9:30am to 6:30pm.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun J. Lin
Patent Examiner
Art Unit 2825
October 13, 2005

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/840,893	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J. Lin	2825

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
716	6	716	1	4	5				
INTERNATIONAL CLASSIFICATION									
G 0 6 F	17/50								
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	/								
	/								

~~(Assistant Examiner) (Date)~~

(Legal Instruments Examiner) 10/8/05 (Date)

LIN, SUN JAMES (10/13/2005)

(Primary Examiner) (Date)

Total Claims Allowed: 51

O.G. Print Claim(s)	O.G. Print Fig.
1	2

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	29	31		61		91		121		151		181
2	2	30	32		62		92		122		152		182
3	3	31	33		63		93		123		153		183
4	4	32	34		64		94		124		154		184
5	5	33	35		65		95		125		155		185
	6	34	36		66		96		126		156		186
6	7	35	37		67		97		127		157		187
7	8	36	38		68		98		128		158		188
8	9	37	39		69		99		129		159		189
9	10	38	40		70		100		130		160		190
10	11	39	41		71		101		131		161		191
11	12	40	42		72		102		132		162		192
12	13	41	43		73		103		133		163		193
13	14		44		74		104		134		164		194
14	15	42	45		75		105		135		165		195
15	16	43	46		76		106		136		166		196
16	17	44	47		77		107		137		167		197
17	18	45	48		78		108		138		168		198
19	19	46	49		79		109		139		169		199
19	20	47	50		80		110		140		170		200
20	21	48	51		81		111		141		171		201
	22	49	52		82		112		142		172		202
21	23	50	53		83		113		143		173		203
22	24	51	54		84		114		144		174		204
23	25		55		85		115		145		175		205
24	26		56		86		116		146		176		206
25	27		57		87		117		147		177		207
26	28		58		88		118		148		178		208
27	29		59		89		119		149		179		209
28	30		60		90		120		150		180		210

OIPE IAP19
SEP 26 2005
PATENT & TRADEMARK OFFICE

IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

OK TO ENTER
10-13-05

APPLICANTS:	Barry A. Hoberman et al.
SERIAL NO.:	10/840,893
FILING DATE:	May 7, 2004
TITLE:	Managing Power on Integrated Circuits Using Power Islands
EXAMINER:	Lin, Sun J.
ART UNIT:	2825
ATTY.DKT.NO.:	PA2258US

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date printed below:

Date: 9/23/05

Eugene G. Kim, Reg. No. 46,267

MAIL STOP AF
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed August 3, 2005, please amend the above-identified application and consider the remarks as follows.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/840,893	HOBERMAN ET AL.
Examiner	**Art Unit**
Sun J. Lin	2825

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim Final	Claim Original	Date 10/13/05							
1	1	=							
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Claim Final	Claim Original	Date 10/13/05							
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/840,893	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J. Lin	2825

SEARCHED			
Class	Subclass	Date	Examiner
716	6	10/4/2005	JSL
716	5	10/4/2005	JSL
716	4	10/4/2005	JSL
716	1	10/4/2005	JSL

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
716	**1**	**10/4/2005**	**JSL**
716	4-6	10/4/2005	JSL

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST [USPAT;US-PGPUB;EPO;JPO;DERWENT;IBM_TDB]	10/4/2005	JSL
EAST [USPAT;US-PGPUB;EPO;JPO;DERWENT;IBM_TDB]	10/13/2005	JSL
IEEE	10/13/2005	JSL

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	((power adj islands) and ((target or goal) adj (power adj level)) and (frequency)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 11:02
L2	0	((power adj islands) and ((target or goal) adj (power adj level)) and (select$4 adj frequency)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 11:02
S1	1393	716/6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:40
S2	1752	716/5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:40
S3	2263	716/4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:41
S4	1778	716/1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:42
S5	1	(716/6).ccls. and (power adj island$2) and (power adj level) and (power adj consumption) and (frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:44
S6	1	(716/5).ccls. and (power adj island$2) and (power adj level) and (power adj consumption) and (frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:44
S7	0	(716/4).ccls. and (power adj island$2) and (power adj level) and (power adj consumption) and (frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:45
S8	0	(716/1).ccls. and (power adj island$2) and (power adj level) and (power adj consumption) and (frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:45

S9	1	("716"/$).ccls. and (power adj island$2) and (power adj level) and (power adj consumption) and (frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 10:45
S10	3	(power adj island$2) and (power adj level) and (power adj consumption) and (frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 11:00
S11	1	((power adj island$2) and (power adj level) and (power adj consumption) and (frequency)). CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/04 11:00
S12	1	(power adj island) and ((target or goal) adj (power adj level)) and (select$4 adj frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 10:46
S13	0	((power adj island) and ((target or goal) adj (power adj level)) and (select$4 adj frequency)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 11:02
S14	0	((power adj island) and ((target or goal) adj (power adj level)) and (frequency)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/10/13 11:02

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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 10/840893

CLAIMS AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE (37 CFR 1.16(a))				$____	OR		$____
TOTAL CLAIMS (37 CFR 1.16(c))	minus 20 =	*	x $____ =		OR	x $____ =	
INDEPENDENT CLAIMS (37 CFR 1.16(b))	minus 3 =	*	x $____ =		OR	x $____ =	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))			+ $____ =		OR	+ $____ =	
			TOTAL		OR	TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

CLAIMS AS AMENDED – PART II

AMENDMENT A: 6/2/05

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total (37 CFR 1.16(c))	* 51	Minus	** 54	=	x $25 =		OR	x $50 =	
Independent (37 CFR 1.16(b))	* 3	Minus	*** 3	=	x $100 =		OR	x $200 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $180 =		OR	+ $360 =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B: 9/26/05

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total (37 CFR 1.16(c))	* 51	Minus	** 54	= —	x $25 =		OR	x $50 =	
Independent (37 CFR 1.16(b))	* 3	Minus	*** 3	= —	x $100 =		OR	x $200 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $180 =		OR	+ $360 =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	x $25 =		OR	x $50 =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	x $100 =		OR	x $200 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $180 =		OR	+ $360 =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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OIPE IAP19 SEP 26 2005 PATENT & TRADEMARK OFFICE

Total Number of Pages in This Submission	18

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

ENCLOSURES *(Check all that apply)*

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [x] Amendment/Reply
  - [x] After Final
  - [ ] Affidavits/declaration(s)
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- [ ] Information Disclosure Statement
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Signature	Eugene Kim		
Printed name	Eugene G. Kim		
Date	September 23, 2005	Reg. No.	46,267

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Typed or printed name	Eugene G. Kim, Reg. No. 46,267	Date	September 23, 2005

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APPLICANTS:	Barry A. Hoberman et al.
SERIAL NO.:	10/840,893
FILING DATE:	May 7, 2004
TITLE:	Managing Power on Integrated Circuits Using Power Islands
EXAMINER:	Lin, Sun J.
ART UNIT:	2825
ATTY.DKT.NO.:	PA2258US

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AMENDMENT

Sir:

In response to the Office Action mailed August 3, 2005, please amend the above-identified application and consider the remarks as follows.

IN THE CLAIMS

Please amend claims 1, 7-8, 11-17, 23-24, 27-32, 35, 39, 45-46, and 49-54.

1. (Currently Amended) A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:

determining a target power level for one of the power islands based on [[the]] needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands;

determining an action to change a power consumption level of the one of the power islands to the target power level; and

performing the action to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for one of the power islands.

2. (Original) The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit.

3. (Original) The method of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

4. (Original) The method of claim1 wherein the power islands comprise power sub-islands.

5. (Original) The method of claim 1 wherein the power islands comprises multiple clock domains.

6. (Cancelled)

7. (Currently Amended) The method of claim 1 wherein the action comprises selecting a clock for the one of the power islands.

8. (Currently Amended) The method of claim 1 wherein the action comprises modifying a first voltage for the one of the power islands.

9. (Original) The method of claim 8 wherein the first voltage comprises a source voltage.

10. (Original) The method of claim 8 wherein the first voltage comprises a threshold voltage.

11. (Currently Amended) The method of claim 1 wherein the action comprises powering on the one of the power islands.

12. (Currently Amended) The method of claim 1 wherein the action comprises powering off the one of the power islands.

13. (Currently Amended) The method of claim 1 wherein the action comprises changing the one of the power islands to a sleep mode.

14. (Currently Amended) The method of claim 1 further comprising:

monitoring the power consumption level of the one of the power islands;

determining whether a threshold level was crossed based on the power consumption level; and

performing the action based on the crossing of the threshold level.

15. (Currently Amended) The method of claim 1 further comprising saving a state of components within the one of the power islands.

16. (Currently Amended) The method of claim 1 further comprising restoring a state of components within the one of the power islands.

17. (Currently Amended) A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:

power control circuitry configured to control power for one of the power islands; and

a power manager configured to determine a target power level for the one of the power islands based on [[the]] needs and operation of the integrated circuit, determine an action to change a power consumption level of the one of the power islands to the target power level, and perform the action to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.

18. (Original) The system of claim 17 wherein the power islands are delineated based on geographic factors of the integrated circuit.

19. (Original) The system of claim 17 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

20. (Original) The system of claim 17 wherein the power islands comprise power sub-islands.

21. (Original) The system of claim 17 wherein the power islands comprise multiple clock domains.

22. (Cancelled)

23. (Currently Amended) The system of claim 17 wherein the action comprises selecting a clock for the one of the power islands.

24. (Currently Amended) The system of claim 17 wherein the action comprises modifying a first voltage for the one of the power islands.

25. (Original) The system of claim 24 wherein the first voltage comprises a source voltage.

26. (Original) The system of claim 24 wherein the first voltage comprises a threshold voltage.

27. (Currently Amended) The system of claim 17 wherein the action comprises powering on the one of the power islands.

28. (Currently Amended) The system of claim 17 wherein the action comprises powering off the one of the power islands.

29. (Currently Amended) The system of claim 17 wherein the action comprises changing the one of the power islands to a sleep mode.

30. (Currently Amended) The system of claim 17 wherein the power manager is configured to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the action based on the crossing of the threshold level.

31. (Currently Amended) The system of claim 17 wherein the power manager is configured to save a state of components within the one of the power islands.

32. (Currently Amended) The system of claim 17 wherein the power manager is configured to restore a state of components within the one of the power islands.

33. (Original) The system of claim 17 further comprising a bus coupled to the power manager and the power islands.

34. (Original) The system of claim 17 wherein the power manager comprises a master manager configured to control power of the integrated circuit.

35. (Currently Amended) The system of claim 17 wherein the power manager comprises a slave manager configured to control power of the one of the power islands.

36. (Original) The system of claim 17 wherein the power control circuitry includes clock multiplexing circuitry.

37. (Original) The system of claim 17 wherein the power control circuitry includes voltage multiplexing circuitry.

38. (Original) The system of claim 17 wherein the power control circuitry includes level shifting circuitry.

39. (Currently Amended) A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising:

power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands based on [[the]] needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands, determine an action to change a power consumption level of the one of the power islands to the target power level, and perform the action to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for <u>the</u> one of the power islands; and

a software storage medium operational to store the power management software.

40. (Original) The software product of claim 39 wherein the power islands are delineated based on geographic factors of the integrated circuit.

41. (Original) The software product of claim 39 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

42. (Original) The software product of claim 39 wherein the power islands comprise power sub-islands.

43. (Original) The software product of claim 39 wherein the power islands comprise multiple clock domains.

44. (Cancelled)

45. (Currently Amended) The software product of claim 39 wherein the action comprises selecting a clock for the one of the power islands.

46. (Currently Amended) The software product of claim 39 wherein the action comprises modifying a first voltage for the one of the power islands.

47. (Original) The software product of claim 46 wherein the first voltage comprises a source voltage.

48. (Original) The software product of claim 46 wherein the first voltage comprises a threshold voltage.

49. (Currently Amended) The software product of claim 39 wherein the action comprises powering on the one of the power islands.

50. (Currently Amended) The software product of claim 39 wherein the action comprises powering off the one of the power islands.

51. (Currently Amended) The software product of claim 39 wherein the action comprises changing the one of the power islands to a sleep mode.

52. (Currently Amended) The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the action based on the crossing of the threshold level.

53. (Currently Amended) The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within the one of the power islands.

54. (Currently Amended) The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within the one of the power islands.

REMARKS

Claims 1-5, 7-21, 23-43, and 45-54 are pending. Claims 1-5, 7-21, 23-43, and 45-54 are rejected. Applicants hereby amend claims 1, 7-8, 11-17, 23-24, 27-32, 35, 39, 45-46, and 49-54.

Claim Objections

Claims 1, 17, and 39 stand objected to because of informalities to delete the word "the" before "needs." Applicants have amended claims 1, 17, and 39 deleting the word "the" before "needs." Claims 1, 17, and 39 stand objected to because of informalities to change the phrase "the one" to "said one." Applicants respectfully traverse the objection because "the" and "said" are interchangeable. For the sake of consistency, Applicants choose the word "the."

Claims 1, 17, and 39 stand objected to because of informalities to change the phrase "where one of the actions" to "wherein the action." Applicants respectfully traverse the objection because the change alters the meaning of claim 1. Claim 1 recites, in part, "performing the action to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands." The proposed change limits the action only to selecting a frequency for the one of the power islands. There may be other actions besides selecting a frequency for the power island to change the power consumption level of the power island of claim 1. Therefore claims 1, 17, and 39 properly recite "where one of the actions" as Applicant is entitled to the broadest protection of the claims.

Claims 1, 7-8, 11-17, 23-24, 27-32, 35, 39, 45-46, and 49-54 stand objected to because of informalities to insert "said" before "one." Applicants have amended claims 1, 7-8, 11-17, 23-24, 27-32, 35, 39, 45-46, and 49-54 to insert the word "the" before "one."

35 U.S.C. § 103

Claims 1-5, 7-21, 23-43, and 45-54 stand rejected under 35 U.S.C. 103(a) as being unpatentable over an IEEE paper entitled "Managing Power and Performance for System-on-Chip Designs using Voltage Islands" by Lackey et al. (hereinafter "Lackey") in view of U.S. Patent 6,631,502 to Buffet et al. (hereinafter "Buffet"), and further in view of an IEEE paper entitled "Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor" by Akui et al. (hereinafter "Akui").

The Office Action recites that Lackey and Buffet do not teach "determining a (target) power level for the voltage island of the embedded processor based on needs and operation of the SOC." The Office Action further recites that Lackey and Buffet do not teach "performing an action to change its power consumption by selecting a frequency for the voltage island." The Office Action does recite that Akui teaches "dynamic voltage and frequency management for low-power embedded processor."

The Akui reference, in which a copy was provided with the Office Action, (hereinafter "first Akui reference") has the title of "Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor" but otherwise does not match the Akui reference listed in the "Notice of References Cited" (hereinafter "second Akui reference"). First, the order of the authorship of the first Akui reference is different. The first named author of the first Akui reference is Takahiro Seki, and not Satoshi Akui.

Second, the publication data of the first Akui reference is April 2005 and not February 2004 as cited for the second Akui reference in the "Notice of Reference Cited." Third, the first Akui reference is published by The Institute of Electronics, Information and Communication Engineers (IEICE) and not by The Institute of Electrical & Electronic Engineers (IEEE).

Applicants have obtained the second Akui reference listed in the "Notice of References Cited" accompanying the Office Action. The second Akui reference has a publication date of February 2004. Applicants filed this present U.S. Patent Application Serial No. 10/840,893 (hereinafter "Application") on May 7, 2004 claiming the benefit of U.S. Provisional Application Serial No. 60/468,742 entitled "Managing Power on Integrated Circuits Using Power Islands" filed on May 7, 2003. Neither the first Akui reference with a publication data of April 2005 nor the second Akui reference with a publication data of February 2004 have a publication date earlier than the priority date of May 7, 2003 for the Application. Therefore, both the first Akui reference and the second Akui reference are not prior art for the Application under 35 U.S.C. § 102 and § 103. Thus, Applicants respectfully request a withdrawal of the 35 U.S.C. § 103(a) rejections in view of Lackey, Buffet, and Akui.

Furthermore, neither Lackey, Buffet, nor the combination of Lackey and Buffet teach or suggest all claim limitations of claim 1. Lackey teaches voltage islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs (Abstract). In regards to claim 1, the Office Action cites Lackey and recites that "a

voltage island is a power island." Applicants respectfully traverse the assertion that a voltage island is a power island.

Claim 1 recites performing the action to change the power consumption level of the one of the power island to the target power level where one of the actions comprises selecting a frequency for the one of the power islands. Lackey teaches voltage islands where power consumption is controlled by voltage (Voltage Islands Overview section on page 195-196). The Office Action further recites that "power consumed by the voltage island is determined by Vdd and F (operation frequency)." Lackey teaches that active power (P_{active}) = C *Vdd2* F (Background section). Assuming F is the frequency of operation, Lackey teaches voltage islands with different frequencies. However, the frequencies in the voltage islands of Lackey are static. The frequencies are not changed by an action to change the power consumption level of the power island. Therefore, Lackey does not teach or suggest performing an action to change the power level consumption level of a power island wherein one of the actions comprises selecting a frequency for the power island as recited in claim 1.

Furthermore, the clock gating in Lackey does not teach or suggest the limitation of selecting a frequency for a power island as recited in claim 1. Clock gating refers to activating a clock in a logic block only when there is work to be done in order to save power. Thus, activating and deactivating a clock does not teach or suggest selecting a frequency for a power island as recited in claim 1.

Buffet teaches a method of analyzing the power distribution in a chip containing one or more voltage islands, each voltage island having a power distribution network connected to a chip-level power distribution network by one or more voltage translation

interface circuits. Buffet also does not teach or suggest performing the action to change the power consumption level of the power island to the target power level where one of the actions comprises selecting a frequency for the power island. Therefore, claim 1 is allowable over Lackey and Buffet for at least the above stated reasons.

Additionally, the Office Action recites that Lackey does not "teach a method of determining and performing an action to change the power consumption to the target power level for each voltage island." The Office Action does recite that Buffet teaches "a method of analyzing voltage island power distribution network by applying a model of chip-level power distribution network (for a SOC design) to (examine), calculate and update an appropriate input voltage for each voltage transfer interface (VTI), based on its recently obtained input voltage, in order to adaptively adjust its input voltage to generate a desired voltage for each voltage island."

FIGS. 9A and 9B in Buffet show how models and simulation are used to determine the VTI circuit voltages for the voltage islands. In Buffet, the VTI circuit output voltage is obtained in step 215 from values produced during the simulation of step 200. Claim 1 recites determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands. Simulating and modeling of voltage islands, as in Buffet, do not teach or suggest determining a target power level for one of the power islands based on the needs and operation of the integrated circuit. Therefore, claim 1 is allowable over Lackey and Buffet for at least the above stated reasons.

Claims 2-5 and 7-16 are dependent either directly or indirectly on claim 1 and are allowable for at least the same reasons as claim 1.

Claim 17 is allowable for at least the same reasons as claim 1.

Claims 18-21 and 23-38 are dependent either directly or indirectly on claim 17 and are allowable for at least the same reasons as claim 17.

Claim 39 is allowable for at least the same reasons as claim 1.

Claims 40-43 and 45-54 are dependent either directly or indirectly on claim 39 and are allowable for at least the same reasons as claim 39.

Thus, claims 1-5, 7-21, 23-43, and 45-54 are allowable. Therefore, Applicants respectfully request allowance of claims 1-5, 7-21, 23-43, and 45-54.

CONCLUSION

In view of the above remarks, this application is in condition for allowance, and the Examiner is respectfully requested to allow this application. The Examiner is invited to call Applicants' representative at the number below if the Examiner has any questions or if there are remaining outstanding issues.

Respectfully submitted,

Barry A. Hoberman et al.

Date: 9/23/05 By: Eugene Kim

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US	8273

22830 7590 08/03/2005

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EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/840,893	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J. Lin	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 26 May 2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5,7-21,23-43 and 45-54 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5,7-21,23-43 and 45-54 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 May 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03/09/05.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to applicant's Amendment and Remarks filed on 05/26/2005 regarding application 10/840,893 filed on 05/07/2004. Claims 6, 22 and 44 have been cancelled without prejudice. Claims 1 – 5, 7 – 21, 23 – 43 and 45 – 54 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 3, before "needs" delete —**the**—.
Claim 1, line 6, change "the one" to —**said one**—.
Claim 1, line 8, change "the one" to —**said one**—.
Claim 1, line 9, change "where one of the actions" to —**wherein the action**—.
Claim 1, line 10, before "one" insert —**said**—.
Claim 7, line 2, before "one" insert —**said**—.
Claim 8, line 2, before "one" insert —**said**—.
Claim 11, line 1, before "one" insert —**said**—.
Claim 12, line 1, before "one" insert —**said**—.
Claim 13, line 1, before "one" insert —**said**—.
Claim 14, line 2, before "one" insert —**said**—.
Claim 15, line 2, before "one" insert —**said**—.
Claim 16, line 2, before "one" insert —**said**—.
Claim 17, line 6, before "one" insert —**said**—.
Claim 17, line 7, before "needs" delete —**the**—.
Claim 17, line 8, change "the one" to —**said one**—.
Claim 17, line 10, change "the one" to —**said one**—.
Claim 17, line 10, change "where one of the actions" to —**wherein the action**—.
Claim 17, line 11, before "one" insert —**said**—.
Claim 23, line 2, before "one" insert —**said**—.
Claim 24, line 2, before "one" insert —**said**—.
Claim 27, line 1, before "one" insert —**said**—.
Claim 28, line 1, before "one" insert —**said**—.
Claim 29, line 1, before "one" insert —**said**—.

Claim 30, line 2, before "one" insert —**said**—.
Claim 31, line 2, before "one" insert —**said**—.
Claim 32, line 2, before "one" insert —**said**—.
Claim 35, line 2, before "one" insert —**said**—.
Claim 39, line 3, before "needs" delete —**the**—.
Claim 39, line 7, change "the one" to —**said one**—.
Claim 39, line 8, change "the one" to —**said one**—.
Claim 39, line 9, change "where one of the actions" to —**wherein the action**—.
Claim 39, line 10, before "one" insert —**said**—.
Claim 45, line 2, before "one" insert —**said**—.
Claim 46, line 2, before "one" insert —**said**—.
Claim 49, line 2, before "one" insert —**said**—.
Claim 50, line 2, before "one" insert —**said**—.
Claim 51, line 2, before "one" insert —**said**—.
Claim 52, line 3, before "one" insert —**said**—.
Claim 53, line 3, before "one" insert —**said**—.
Claim 54, line 3, before "one" insert —**said**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 5, 7 – 21, 23 – 43 and 45 – 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE paper entitled "*Managing Power and Performance for System-on-Chip using Voltage Islands*" authored by Lackey et al. over of U.S. Patent No. 6,631,502 B2 to Buffet et al. in view of IEEE paper entitled "*Dynamic Voltage and Frequency Management for Low-Power Embedded Microprocessor*" authored by Akui et al.

5. As to Claim 1, Lackey et al. show and teach the following subject matter:

- *Managing power* on an *system-on-chip (SOC)* design (i.e., *integrated circuit*) including a plurality of *voltage islands* (i.e., *power islands*) – title; abstract];
- (Active) power P_{active} consumed by circuitry on a voltage island is determined by voltage level (Vdd) and operation frequency (F) of (switching) circuitry on the voltage island – [Background; Equation 1]; Notice that (1) a *voltage island* is a *power island* (2) power consumed by a voltage island is determined by Vdd (supply voltage level) and F (operation frequency) of the circuitry on the voltage island under study;
- *Identifying* (i.e., *determining*) a *minimum voltage* (i.e., *target power level*) required for each *voltage island* (*power island*) to achieve its required performance – [page 196, Paragraph: Voltage Island Scenarios and Examples]; Notice that power consumption of SOC is independently controlled within each of the *voltage island* (*power island*).

Notice that power consumption level of a voltage island is determined by the voltage level of the *voltage island* (*power island*) on which it is operating. Therefore, Lackey et al. do teach determining a *power consumption level* of each *voltage island* (*power island*) in order to meet its operation voltage requirement, they do not teach a method of determining and performing an action to change the power consumption to the *target power level* for each *voltage island* (*power island*). But Buffet et al. teach a method of analyzing *voltage island power distribution network* by applying a model of *chip-level power distribution network* (for a SOC design) to (*examine*), ***calculate*** and ***update*** an appropriate *input voltage* for each *voltage transfer interface (VTI)*, based on its recently obtained input

voltage, in order to adaptively *adjust* its input voltage to generate a *desired voltage* for each *voltage island* – [abstract; col. 2, line 13 – 67; Figs. 1 – 10].

Notice that (1) the *desired voltage* is provided to each *voltage island* in order to achieve its *target power level* (2) applying model for *calculating*, *updating* and *adjusting* input voltage of a *VTI* is a method of determining and performing an action to change a suitable *voltage level* (i.e., *power consumption level*) of a *voltage island* in order to achieve its *target power level.*

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Buffet et al.* in analyzing *voltage island power distribution network* by applying a model of *chip-level power distribution network* for a SOC design including a plurality of *voltage islands* (*power islands*) to *calculate* and *update* an appropriate *input voltage* for each *voltage transfer interface (VTI)*, based on its recently obtained input voltage, in order to *adaptively adjust* its *input voltage* to generate a suitable *voltage level* for to achieve a *target power level* for each voltage island (power island) for use in managing power on the SOC.

Lackey et al. and *Buffet et al.* teach all subject matter given above, *Lackey et al.* also teach a voltage island for a embedded processor in the SOC, they do not teach determining a (target) power level for the voltage island of the embedded processor based on *needs* and *operation* of the SOC and performing an action to change its power consumption by selecting a frequency for the voltage island. But *Akui et al.* teach dynamic voltage and frequency management for low-power embedded microprocessor – [title].

Akui et al. teach monitoring activity of an LSI by a *power-management* software in DVC (dynamic voltage control) and DFC (dynamic frequency control) in order to determine and to perform an action to dynamically control and adaptively adjust/select voltage and system clock frequency for an embedded microprocessor thereby minimizing power consumption (to a target power level) to meet *needs and operation* of the LSI – [Section 3.5; Fig. 3.5.2; Fig. 3.5.4].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Akui et al.* in monitoring activity of the SOC by a *power-management* software in DVC (dynamic voltage

control) and DFC (dynamic frequency control) in order to determine and to perform an action to dynamically control and adaptively adjust/select voltage and system clock frequency of an processor embedded on an voltage island (voltage island) thereby minimizing power consumption (to a target power level) to meet *needs and operation* of the SOC.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claim 17, reasons are included in **[Response A]** given above.

7. As to Claim 39, in addition to reasons included in **[Response A]** given above, *Buffet et al.* show in Fig. 10 a *RAM 240* and *ROM 245*, which are *software storage medium* operational to store power management software.

8. As to Claims 2, 18 and 40, *Lackey et al.* teach subject matter regarding *geographic factors* associated with *voltage islands* (*power islands*) that (1) *voltage islands* must be *floor-planned* (placed) in close proximity with chip pins corresponding to its off-chip power source (2) On-chip power sources must also be placed within the *voltage island* – [page 201, paragraph: Physical Planning and Implementation of Structure].

9. As to Claims 3, 19 and 41, *Lackey et al.* teach subject matter regarding *functional circuitry* associated with *voltage islands* (*power islands*) that (1) partitioning of an SOC involves division and subdivision into an n-level *functional hierarchy* ... functional components (i.e., functional circuitry) (2) designing for *voltage islands* places additional requirements on the *functional partition process* – [page 199, paragraph: Functional Partitioning].

10. As to Claims 4, 20 and 42, *Lackey et al.* show in Fig. 4 and teach subject matter regarding *power sub-islands* (e.g., *child voltage islands*) that (1) *voltage islands* can be used at *different levels of design hierarchy* (2) *voltage island* capable of fine *hierarchical*

granularity – [Fig. 4; page 197, right column below Fig. 4] (3) *parent (voltage) island* – [page 198, description above Fig. 5].

For reference purposes, the explanations given above in response to Claims 4, 20 and 42 are called **[Response B]** hereinafter.

11. As to Claims 5, 7, 21, 23, 43 and 45, *Lackey et al.* show in Fig. 3 teach subject matter regarding *multiple clock domains* of voltage islands that *functional blocks* operating with *different voltage levels* in different *frequency clock domains* (e.g., 150 MHz, 400 MHz) – [Fig. 3; page 196 right column]. Notice that an appropriate *clock* and associated *clock frequency* are selected for each power island. *Akui et al.* show and teach selecting a clock for the embedded microprocessor by DFC – [Fig. 3.5.2; Fig. 3.5.4].

For reference purposes, the explanations given above in response to Claims *5 – 7, 21, 23, 43 and 45* are called **[Response C]** hereinafter.

12. As to Claims 8 – 10, 24 – 26 and 46 – 48, *Lackey et al.* teach (1) relationship between *threshold voltage (Vt)* and power leakage (2) *voltage island architecture methods* ... *multiple-threshold (voltage) design technique* (3) change *supply voltage level* associated with a low-Vt block in order to reduce its power leakage (4) completely shut off *supply voltage level* associated with a low-Vt during sleep modes to eliminate standby power – [page 197, paragraph: System-level Power management Approaches]. Notice that a first voltage can be the *supply voltage* (i.e., *source voltage*) and/or the *threshold voltage Vt*.

13. As to Claims 11 – 13, 27 – 29 and 49 – 51, *Buffet et al.* and *Lackey et al.* teach the following subject matter:

- An action of selectively *powering on* or *powering off* or *another appropriate voltage* for one of *voltage islands* (*power islands*) – [*Buffet et al.*: col. 1, line 20 – 28];
- On-chip ***power-switching circuitry***; an action of *switching* (i.e., *changing*) one of *voltage islands* (*power islands*) to a *sleep mode*, *power off state* or an *power on state* – [*Lackey et al.*: page 196, right column; page 200, right column; Fig. 4].

For reference purposes, the explanations given above in response to Claims 11 – 13, 27 – 29 and 49 – 51 are called **[Response D]** hereinafter.

14. As to Claims 14, 30 and 52, in addition to reasons included in **[Response A]** given above, *Buffet et al. teach* (1) updating *output voltage value* of *voltage translation interface* (VTI) – [col. 2, line 57 – 58] (2) *comparing* (i.e., *monitoring*) the *updated* (*output voltage*) *value* ... updating, if necessary, if (output voltage level) not converged within a *preset limit* (i.e., *preset threshold level*) – [col. 2, line 62 – 67].

15. As to Claim 15, 16, 31, 32, 53 and 54, *Lackey et al.* show and teach the subject matter regarding *save* and *restore* necessary logic states (of components) within in one of voltage islands – [Fig. 5; page 189, paragraph State-Saving]. Notice that, as shown in Fig. 5, the logic states are stored in special state-saving latches, which serve as a memory.

16. As to Claim 33, *Lackey et al.* show in Fig. 4 and teach the subject matter regarding coupling the *power management unit* (*power manager*) to the *voltage islands* V1, V11, V2, and V22. Notice that the wires utilized for performing the coupling and be grouped together as a *bus*.

17. As to Claims 34 and 35, *Lackey et al.* teach implementing *voltage islands* in *different levels of design hierarchy* in **[Response B]** given above. Notice that (1) the *voltage islands* can have many *hierarchical levels* (e.g., *parent voltage islands*, *children voltage islands*, etc.) (2) In order to effectively *control voltage levels* in different hierarchy, it is inherent that the *power manger* should comprise a *master power manager* and a *slave power manager* (3) the *master power manager* is configured to control *voltage levels* of the SOC at *higher hierarchical level* (e.g., *parent voltage islands*); whereas the *slave power manager*, which is coordinated by the *master power manager*, is configured to control *voltage levels* of *voltage islands* at a *lower hierarchical level* (e.g., *children voltage islands*).

18. As to Claim 36, in addition to *clock gating* scheme and *multiple frequency clocks* explained in **[Response A]** and **[Response C]**, respectively, *Lackey et al.* teach implementing *timing clock distribution structure* for *voltage islands* with different power sources – [Page 200, left column]. Notice that the multiply frequency clocks can be distributed using a *clock multiplexing circuitry*.

19. As to Claim 37, *Lackey et al.* show in Fig. 4 and teach implementing a *power switching circuitry* as explained in **[Response D]** given above. Notice that the (1) *power switching circuitry* can be utilized to *instantly switch* voltage of a *voltage island* to a *power-on state*, a *power-off state* or a *sleep mode* (2) *power switching circuitry* can be realized using *multiplexing circuitry* (e.g., .

20. As to Claim 38, *Lackey et al.* teach implementing *voltage level-shifting circuits* (*Level Shifters*) for *voltage islands* – [Page 200, left column].

Response to Amendment and Remarks

21. Applicants' amendments and remarks filed on 05/26/2005 have been reviewed. Applicants' arguments have been fully considered but they are not all persuasive. To overcome Examiner's cited prior art, applicants have amended independent Claims 1, 17 and 39 to add new limitations. However, new grounds of rejections have been founded and cited in this Office Action in view of additional newly discovered prior arts: IEEE paper entitled "*Dynamic Voltage and Frequency Management for Low-Power Embedded Microprocessor*" authored by *Akui et al.* Detailed responses to amended claims are prepared and given as above.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272-1899. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Patent Examiner
Art Unit 2825
July 29, 2005

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IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Barry Alan Hoberman et al.
SERIAL NO.:	10/840,893
FILED:	May 7, 2004
TITLE:	Managing Power on Integrated Circuits Using Power Islands
EXAMINER:	Sun J. Lin
GROUP ART UNIT:	2825
ATTY.DKT.NO.:	PA2258US

MAIL STOP AMENDMENT
COMMISSIONER FOR PATENTS
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ALEXANDRIA, VA 22313-1450

List of Co-Pending Patent Applications That May Be Directed Towards Similar Subject Matter

Examiner's Initials	Serial Number	First-Named Inventor	Title	Filing Date
JSL	10/996,739	Randy J. Caplan	Systems and Methods for Minimizing Static Leakage of an Integrated Circuit	November 24, 2004
Examiner's Signature:	Jamar Sun Lin			Date 7-26-05

{00138836v1}

OIPE JC858
MAR 0 9 2005
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PTO/SB/08A (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 5

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JLL		US- 6,598,148	07-22-2003	Moore et al.	
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	James Sun Lin	Date Considered	7-26-05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08B (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	2	of	5

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
JSL		GUPTA, R., et al., "Low Power Wireless Networked System Design," HotChips, August 18, 2002, Stanford, CA.	
		TSAI, Y-F et al., "Implications of Technology Scaling on Leakage Reduction Techniques," DAC 2003, June 2-6, 2003, ACM, Anaheim, CA, USA.	
		LI L. et al., "Managing Leakage Energy in Cache Hierarchies," Journal of Instruction-Level Parallelism, 2003, pp. 1-24, Vol. 5.	
		HU, J.S. et al., "Using Dynamic Branch Behavior for Power-Efficient Instruction Fetch," Proc. of IEEECS Annual Symposium on VLSI (ISVLSI 2003), February 20-21, 2003, Tampa, FL	
		ZHANG, W. et al., "Compiler Support for Reducing Leakage Energy Consumption," Proceedings of the 6th Design Automation and Test in Europe Conference (DATE-03), March, 2003, Munich, Germany.	
		DEGALAHAL, V. et al., "Analyzing Soft Errors in Leakage Optimized SRAM Design," Proceedings of 16th International Conference on VLSI Design, January 2003, New Delhi, India.	
		LI, L. et al., "Leakage Energy Management in Cache Hierarchies," 11th International Conference on Parallel Architectures and Compilation Techniques (PACT'02), September 2002.	
		DUARTE, D. et al., "Impact of Scaling on the Effectiveness of Dynamic Power Reduction Schemes," Proceedings of the 20th International Conference on Computer Design (ICCD), September 16-18, 2002, Freiberg, Germany.	
		DUARTE, D. et al., "Impact of Technology Scaling and Packaging on Dynamic Voltage Scaling Techniques," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, September 25-28, 2002, Rochester, NY.	
JSL		KIM, S et al. "Predictive Precharging for Bitline Leakage Energy Reduction," Proceedings of 15th Annual IEEE International ASIC/SOC Conference, September 25-28, 2002, Rochester, NY.	

Examiner Signature	James Jun Lin	Date Considered	7-26-05

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Sheet 3 of 5

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
JSL		RAMANARAYANAN, R. et al. "Characterizing Dynamic and Leakage Power Behavior in Flip Flops," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, September 2002.	
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Examiner Signature	Jamie Sun Lin	Date Considered	7-26-05

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Filing Date	May 7, 2004
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		FRENKIL, J. "A Multi-Level Approach to Low-Power IC Design," IEEE Spectrum, February 1998, Vo. 35, No. 2.	
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Examiner Signature	James Sun Lin	Date Considered	7-26-05

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		PANGRLE, B. "Low Power Design: A Holistic Approach in an Era of New Semiconductor Technologies," San Diego Telecom Council Semiconductor SIG, November 14, 2002.	
		RABAEY, J. "Design Aids for Low Power: Part II Architecture and System Levels," 1997.	
		GRUNWALD, D. et al. "Kool Chips Workshop," MICRO33, December 10, 2000, Monterey, CA.	
		FLYNN, J. et al., "Power Management in Complex SoC Design," Synopsys, April 2004, located at http://www.synopsys.com/sps.	

Examiner Signature		Date Considered	7-26-05

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Notice of References Cited	Application/Control No. 10/840,893	Applicant(s)/Patent Under Reexamination HOBERMAN ET AL.	
	Examiner Sun J. Lin	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	Akui et al.,"Dynamic Voltage and Frequency Management for Low-Power Embedded Microprocessor", Feb. 2004, IEEE International Solid-State Circuits Conference, Digest of Technical Papers, vol. 1, pp. 64 - 513.
	W	Talpes et al.,"Toward a Multiple Clocl/Voltage Island Design Style for Power-Aware Processors", May 2005, IEEE Transactions on Very Large Scale Integration (VLSI) system, vol. 13, iss. 5, pp. 591 - 603.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/840,893	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J. Lin	2825

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/840,893	HOBERMAN ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

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Class	Subclass	Date	Examiner
716	6	7/27/2005	JSL
716	5	7/27/2005	JSL
716	4	7/27/2005	JSL
716	1	7/27/2005	JSL

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
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IEEE	7/27/2005	JSL

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(((power adj consumption) same frequency) and (target adj (power adj level))).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:47
L2	1	(((power adj consumption) and frequency) and (target adj (power adj level))).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:47
L3	0	(((power adj consumption) and frequency) and ((power or voltage) adj island)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:51
L4	1	(((power adj consumption) and frequency) and ((power or voltage) adj islands)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:51
S1	1322	716/6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:52
S2	1674	716/5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:52
S3	12336544	"4"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:52
S4	2150	716/4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:52
S5	1691	716/1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:52
S6	41	(716/6).ccls. and ((power adj consumption) same frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:55

S7	36	(716/5).ccls. and ((power adj consumption) same frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:03
S8	54	(716/4).ccls. and ((power adj consumption) same frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:53
S9	51	(716/1).ccls. and ((power adj consumption) same frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:53
S10	227	("716"/$).ccls. and ((power adj consumption) same frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:54
S11	24191	((power adj consumption) same frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 07:54
S12	3	(716/6).ccls. and ((power adj consumption) same frequency) and ((power or voltage) adj island)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:50
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S16	7	("716"/$).ccls. and ((power adj consumption) same frequency) and ((power or voltage) adj island)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:13

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S18	2	((power adj consumption) same frequency) and ((power or voltage) adj island) and (target adj (power adj level))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:23
S19	15	((power adj consumption) same frequency) and (target adj (power adj level))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/27 08:46

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Lackey, D.E.; Zuchowski, P.S.; Bednar, T.R.; Stout, D.W.; Gould, S.W.; Cohn,
Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Confere
10-14 Nov. 2002 Page(s):195 - 202
Digital Object Identifier 10.1109/ICCAD.2002.1167534
AbstractPlus | Full Text: PDF(629 KB) **IEEE CNF**

2. **Using mobilize power management IP for dynamic and static power redu 130 nm**
Hillman, D.;
Design, Automation and Test in Europe, 2005. Proceedings
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Digital Object Identifier 10.1109/DATE.2005.324
AbstractPlus | Full Text: PDF(160 KB) **IEEE CNF**

3. **New trends in low power SoC design technologies**
Wei Hwang;
SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip]
17-20 Sept. 2003 Page(s):422
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4. **Energy-efficient low-voltage operation of digital CMOS circuits through c**
Rajapandian, S.; Zheng Xu; Shepard, K.L.;
VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on
17-19 June 2004 Page(s):330 - 333
AbstractPlus | Full Text: PDF(453 KB) **IEEE CNF**

5. **Toward a multiple clock/voltage island design style for power-aware proc**
Talpes, E.; Marculescu, D.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 13, Issue 5, May 2005 Page(s):591 - 603
Digital Object Identifier 10.1109/TVLSI.2005.844305
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IEE CNF	IEE Conference Proceeding
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1. **Dynamic frequency and voltage control for a multiple clock domain micr**
Semeraro, G.; Albonesi, D.H.; Dropsho, S.G.; Magklis, G.; Dwarkadas, S.; Sco
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM In
Symposium on
18-22 Nov. 2002 Page(s):356 - 367
Digital Object Identifier 10.1109/MICRO.2002.1176263
AbstractPlus | Full Text: PDF(485 KB) **IEEE CNF**

2. **High-speed SiGe HBT technology and applications to mm-wave circuits**
Meister, T.F.; Knapp, H.; Schafer, H.; Aufinger, K.; Stengl, R.; Boguth, S.; Schr
M.; Perndl, W.; Wurzer, M.; Bottner, T.; Bock, J.;
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Digital Object Identifier 10.1109/SMIC.2004.1398167
AbstractPlus | Full Text: PDF(682 KB) **IEEE CNF**

3. **A V-band VCO and frequency divider MMICs for phased-locked loop**
Ockgoo Lee; Jeong-Geun Kim; Sang-Hoon Jeon; Jae-Woo Park; Songchel Ho
Microwave Symposium Digest, 2004 IEEE MTT-S International
Volume 3, 6-11 June 2004 Page(s):1321 - 1324 Vol.3
Digital Object Identifier 10.1109/MWSYM.2004.1338811
AbstractPlus | Full Text: PDF(471 KB) **IEEE CNF**

4. **A completely integrated single-chip PLL with a 34 GHz VCO using 0.2 µm technology**
Lang, M.; Leber, P.; Wang, Z.G.; Lao, Z.; Rieger-Motzer, M.; Bronner, W.; Huls
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5-8 May 1997 Page(s):529 - 532
Digital Object Identifier 10.1109/CICC.1997.606682
AbstractPlus | Full Text: PDF(284 KB) **IEEE CNF**

5. **Dynamic voltage and frequency management for a low-power embedded**
Nakai, M.; Akui, S.; Seno, K.; Meguro, T.; Seki, T.; Kondo, T.; Hashiguchi, A.; I
Kumano, K.; Shimura, M.;
Solid-State Circuits, IEEE Journal of
Volume 40, Issue 1, Jan. 2005 Page(s):28 - 35

PTO/SB/06 (08-03)
Approved for use through 7/31/2006. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/840893

CLAIMS AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE (37 CFR 1.16(a))				$____	OR		$____
TOTAL CLAIMS (37 CFR 1.16(c))	minus 20 =	*	x $____ =		OR	x $____ =	
INDEPENDENT CLAIMS (37 CFR 1.16(b))	minus 3 =	*	x $____ =		OR	x $____ =	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))			+ $____ =		OR	+ $____ =	
			TOTAL		OR	TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

CLAIMS AS AMENDED – PART II

AMENDMENT A

6/2/05

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDI-TIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE
Total (37 CFR 1.16(c))	* 51	Minus	** 54	=	x $25 =		OR	x $50 =	
Independent (37 CFR 1.16(b))	* 3	Minus	*** 3	=	x $100 =		OR	x $200 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $180 =		OR	+ $360 =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDI-TIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	x $25 =		OR	x $50 =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	x $100 =		OR	x $200 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $180 =		OR	+ $360 =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDI-TIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	x $25 =		OR	x $50 =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	x $100 =		OR	x $200 =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $180 =		OR	+ $360 =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Index of Claims	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/840,893	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J. Lin	2825

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim Final	Claim Original	Date 2/22/05	Claim Final	Claim Original	Date 2/22/05	Claim Final	Claim Original
	1	√		51	√		101
	2	√		52	√		102
	3	√		53	√		103
	4	√		54	√		104
	5	√		55			105
	6	√		56			106
	7	√		57			107
	8	√		58			108
	9	√		59			109
	10	√		60			110
	11	√		61			111
	12	√		62			112
	13	√		63			113
	14	√		64			114
	15	√		65			115
	16	√		66			116
	17	√		67			117
	18	√		68			118
	19	√		69			119
	20	√		70			120
	21	√		71			121
	22	√		72			122
	23	√		73			123
	24	√		74			124
	25	√		75			125
	26	√		76			126
	27	√		77			127
	28	√		78			128
	29	√		79			129
	30	√		80			130
	31	√		81			131
	32	√		82			132
	33	√		83			133
	34	√		84			134
	35	√		85			135
	36	√		86			136
	37	√		87			137
	38	√		88			138
	39	√		89			139
	40	√		90			140
	41	√		91			141
	42	√		92			142
	43	√		93			143
	44	√		94			144
	45	√		95			145
	46	√		96			146
	47	√		97			147
	48	√		98			148
	49	√		99			149
	50	√		100			150

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry A. Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US
Total Number of Pages in This Submission	16

ENCLOSURES *(Check all that apply)*

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [x] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Carr & Ferrell LLP Cust. No. 22830		
Signature	Eugene Kim		
Printed name	Eugene G. Kim		
Date	May 24, 2005	Reg. No.	46,267

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I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Eugene Kim		
Typed or printed name	Eugene G. Kim, Reg. No. 46,267	Date	May 24, 2005

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OIPE JC130
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IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS:	Barry A. Hoberman et. al.
SERIAL NO.:	10/840,893
FILING DATE:	May 7, 2004
TITLE:	Managing Power on Integrated Circuits Using Power Islands
EXAMINER:	Lin, Sun J.
ART UNIT:	2825
ATTY.DKT.NO.:	PA2258US

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date printed below:

Date: May 24, 2005

Eugene G. Kim, Reg. No. 46,267

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AMENDMENT

Sir:

In response to the Office Action mailed February 24, 2005, please amend the above-identified application and consider the remarks as follows.

IN THE CLAIMS

Please amend claims 1, 14, and 27.

Please cancel claims 6, 22, and 44.

1. (Currently Amended) A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:

determining a target power level for one of the power islands based on the needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands;

determining an action to change a power consumption ~~power~~ level of the one of the power islands to the target power level; and

performing the action to change the power consumption ~~power~~ level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for one of the power islands.

2. (Original) The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit.

3. (Original) The method of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

4. (Original) The method of claim1 wherein the power islands comprise power sub-islands.

5. (Original) The method of claim 1 wherein the power islands comprises multiple clock domains.

6. (Cancelled)

7. (Original) The method of claim 1 wherein the action comprises selecting a clock for one of the power islands.

8. (Original) The method of claim 1 wherein the action comprises modifying a first voltage for one of the power islands.

9. (Original) The method of claim 8 wherein the first voltage comprises a source voltage.

10. (Original) The method of claim 8 wherein the first voltage comprises a threshold voltage.

11. (Original) The method of claim 1 wherein the action comprises powering on one of the power islands.

12. (Original) The method of claim 1 wherein the action comprises powering off one of the power islands.

13. (Original) The method of claim 1 wherein the action comprises changing one of the power islands to a sleep mode.

14. (Original) The method of claim 1 further comprising:

monitoring the power consumption level of one of the power islands;

determining whether a threshold level was crossed based on the power consumption level; and

performing the action based on the crossing of the threshold level.

15. (Original) The method of claim 1 further comprising saving a state of components within one of the power islands.

16. (Original) The method of claim 1 further comprising restoring a state of components within one of the power islands.

17. (Currently Amended) A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:

power control circuitry configured to control power for one of the power islands; and

a power manager configured to determine a target power level for one of the power islands based on the needs and operation of the integrated circuit, determine an action to change a power consumption ~~power~~ level of the one of the power islands to the target power level, and perform the action to change the power consumption ~~power~~ level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for one of the power islands.

18. (Original) The system of claim 17 wherein the power islands are delineated based on geographic factors of the integrated circuit.

19. (Original) The system of claim 17 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

20. (Original) The system of claim 17 wherein the power islands comprise power sub-islands.

21. (Original) The system of claim 17 wherein the power islands comprise multiple clock domains.

22. (Cancelled)

23. (Original) The system of claim 17 wherein the action comprises selecting a clock for one of the power islands.

24. (Original) The system of claim 17 wherein the action comprises modifying a first voltage for one of the power islands.

25. (Original) The system of claim 24 wherein the first voltage comprises a source voltage.

26. (Original) The system of claim 24 wherein the first voltage comprises a threshold voltage.

27. (Original) The system of claim 17 wherein the action comprises powering on one of the power islands.

28. (Original) The system of claim 17 wherein the action comprises powering off one of the power islands.

29. (Original) The system of claim 17 wherein the action comprises changing one of the power islands to a sleep mode.

30. (Original) The system of claim 17 wherein the power manager is configured to monitor the power consumption level of one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the action based on the crossing of the threshold level.

31. (Original) The system of claim 17 wherein the power manager is configured to save a state of components within one of the power islands.

32. (Original) The system of claim 17 wherein the power manager is configured to restore a state of components within one of the power islands.

33. (Original) The system of claim 17 further comprising a bus coupled to the power manager and the power islands.

34. (Original) The system of claim 17 wherein the power manager comprises a master manager configured to control power of the integrated circuit.

35. (Original) The system of claim 17 wherein the power manager comprises a slave manager configured to control power of one of the power islands.

36. (Original) The system of claim 17 wherein the power control circuitry includes clock multiplexing circuitry.

37. (Original) The system of claim 17 wherein the power control circuitry includes voltage multiplexing circuitry.

38. (Original) The system of claim 17 wherein the power control circuitry includes level shifting circuitry.

39. (Currently Amended) A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising:

power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands <u>based on the needs and operation of the integrated circuit</u> where power consumption is independently controlled within each of the power islands, determine an action to change a <u>power</u> consumption ~~power~~ level of the one of the power islands to the target power level, and perform the action to change the <u>power</u> consumption ~~power~~ level of the one of the power islands to the target power level <u>where one of the actions comprises selecting a frequency for one of the power islands</u>; and

a software storage medium operational to store the power management software.

40. (Original) The software product of claim 39 wherein the power islands are delineated based on geographic factors of the integrated circuit.

41. (Original) The software product of claim 39 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

42. (Original) The software product of claim 39 wherein the power islands comprise power sub-islands.

43. (Original) The software product of claim 39 wherein the power islands comprise multiple clock domains.

44. (Cancelled)

45. (Original) The software product of claim 39 wherein the action comprises selecting a clock for one of the power islands.

46. (Original) The software product of claim 39 wherein the action comprises modifying a first voltage for one of the power islands.

47. (Original) The software product of claim 46 wherein the first voltage comprises a source voltage.

48. (Original) The software product of claim 46 wherein the first voltage comprises a threshold voltage.

49. (Original) The software product of claim 39 wherein the action comprises powering on one of the power islands.

50. (Original) The software product of claim 39 wherein the action comprises powering off one of the power islands.

51. (Original) The software product of claim 39 wherein the action comprises changing one of the power islands to a sleep mode.

52. (Original) The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the action based on the crossing of the threshold level.

53. (Original) The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within one of the power islands.

54. (Original) The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within one of the power islands.

REMARKS

Claims 1-54 are pending. Claims 1-54 are rejected. Applicants hereby amend claims 1, 17, and 39. Applicants hereby cancel claims 6, 22, and 44.

Claim Objections

Claims 1, 17, and 39 stand objected to because of informalities with the phrase "consumption power." Applicants have amended claims 1, 17, and 39 to replace the phrase "consumption power" to "power consumption."

35 U.S.C. § 103

Claims 1-54 stand rejected under 35 U.S.C. 103(a) as being unpatentable over an IEEE paper entitled "Managing Power and Performance for System-on-Chip Designs using Voltage Islands" by Lackey et. al. (hereinafter "Lackey") in view of U.S. Patent 6,631,502 to Buffet et. al. (hereinafter "Buffet").

Neither Lackey, Buffet nor the combination of Lackey and Buffet teach or suggest all claim limitations of claim 1. Lackey teaches voltage islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs (Abstract). In regards to claim 1, the Office Action cites Lackey and recites that "a voltage island is a power island." Applicants respectfully traverse the assertion that a voltage island is a power island.

Applicants have further amended claim 1 to distinguish the differences between voltage islands and power islands. Amended claim 1 recites performing the action to

change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for one of the power islands. Lackey teaches voltage islands where power consumption is controlled by voltage (Voltage Islands Overview section on page 195-196). However, Lackey does not teach or suggest power islands that control power consumption by frequency. While a power island may control power consumption by voltage, a power island of claim 1 may also advantageously control power consumption by selecting frequency. Power consumption in a power island can be reduced by reducing the frequency used in the power island.

Applicants have cancelled claim 6 and moved limitations similar to claim 6 into claim 1. In rejecting claim 6, the Office Action recites that Lackey "show[n] in Fig. 3 teach subject matter regarding multiple clock domains of voltage islands that (1) applying clock gating to limit power active power . . .voltage islands . . . power management – [page 196, paragraph on left column below Fig. 2] (2) functional blocks operating with different voltage levels in different frequency clock domains (e.g. 150MHz, 400 MHz) – [Fig. 3; page 196 right column]. Notice that an appropriate clock and associated clock frequency are selected for each power island." The clock gating in Lackey does not teach or suggest the limitation of selecting a frequency for a power island as recited in claim 1. Clock gating refers to activating a clock in a logic block only when there is work to be done in order to save power. Thus, activating and deactivating a clock does not teach or suggest selecting a frequency for a power island as recited in claim 1. Additionally, while Lackey does teach voltage islands with different frequencies, Lackey does not teach or suggest performing an action to change the power consumption level of a power island to

a target power level where an action comprises selecting a frequency for the power island. Instead, the frequencies in the voltage islands of Lackey are static and are not changed by an action to change the power consumption level of the power island.

Buffet teaches a method of analyzing the power distribution in a chip containing one or more voltage islands, each voltage island having a power distribution network connected to a chip-level power distribution network by one or more voltage translation interface circuits. Buffet also does not teach or suggest power islands that control power consumption by frequency. Thus, claim 1 is allowable over Lackey and Buffet for at least the above stated reasons.

Additionally, the Office Action recites that Lackey does not "teach a method of determining and performing an action to change the power consumption to the target power level for each voltage island." The Office Action does recite that Buffet teaches " a method of analyzing voltage island power distribution network by applying a model of chip-level power distribution network (for a SOC design) to (examine), calculate and update an appropriate input voltage for each voltage transfer interface (VTI), based on its recently obtained input voltage, in order to adaptively adjust its input voltage to generate a desired voltage for each voltage island."

FIGS. 9A and 9B in Buffet shows how models and simulation are used to determine the VTI circuit voltages for the voltage islands. Buffet teaches where the voltage islands are modeled into passive linear circuits and current sources (step 170 and 175 in FIG 9A and 9B, col. 8 lines 37-42). In Buffet, the VTI circuit output voltage is determined in step 215. Applicants have further amended claim 1 to distinguish claim 1 over Buffet. Amended claim 1 recites determining a target power level for one of the

power islands based on the needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands. Simulating and modeling of voltage islands, as in Buffet, do not teach or suggest determining a target power level for one of the power islands based on the needs and operation of the integrated circuit. Consequently, amended claim 1 is more responsive to the actual needs and operation of the integrated circuit as compared to simulations and models. Thus, claim 1 is allowable over Lackey and Buffet for at least the above stated reasons.

Claims 2-5 and 6-16 are dependent either directly or indirectly on claim 1 and are allowable for at least the same reasons as claim 1.

Claim 17 is allowable for at least the same reasons as claim 1.

Claims 18-21 and 23-38 are dependent either directly or indirectly on claim 17 and are allowable for at least the same reasons as claim 17.

Claim 39 is allowable for at least the same reasons as claim 1.

Claims 40-43 and 45-54 are dependent either directly or indirectly on claim 39 and are allowable for at least the same reasons as claim 39.

Thus, claims 1-54 are allowable. Therefore, Applicants respectfully request allowance of claims 1-54.

CONCLUSION

In view of the above remarks, this application is in condition for allowance, and the Examiner is respectfully requested to allow this application. The Examiner is invited to call Applicants' representative at the number below if the Examiner has any questions or if there are remaining outstanding issues.

Respectfully submitted,

Barry A. Hoberman et. al.

Date: May 24, 2005 By: _____

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Palo Alto, California 94303
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PTO/SB/21 (09-04)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	19

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
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- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):
  1) Confirmation Postcard;
  2) Duplicate of IDS;
  3) PTO/SB/08 (x2);
  4) Copies of 34 Cited References;
  5) List of Copending Applications (x2)

Remarks

Total page number does not include check, postcard, or cited references.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Carr & Ferrell LLP Cust. No. 22830		
Signature	Eugene Kim		
Printed name	Eugene G. Kim		
Date	March 7, 2005	Reg. No.	46,267

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Eugene Kim		
Typed or printed name	Eugene G. Kim, Reg. No. 46,267	Date	March 7, 2005

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PTO/SB/17 (12-04v2)
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 180.00

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Examiner Name	Sun J. Lin
Art Unit	2825
Attorney Docket No.	PA2258US

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 06-0600 Deposit Account Name: Carr & Ferrell LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	**Fee ($)**	**Small Entity Fee ($)**
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims _____ - 20 or HP = **Extra Claims** _____ x **Fee ($)** _____ = **Fee Paid ($)** _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims _____ - 3 or HP = **Extra Claims** _____ x **Fee ($)** _____ = **Fee Paid ($)** _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims **Fee ($)** _____ **Fee Paid ($)** _____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets _____ - 100 = **Extra Sheets** _____ / 50 = **Number of each additional 50 or fraction thereof** _____ (round **up** to a whole number) x **Fee ($)** _____ = **Fee Paid ($)** _____

4. OTHER FEE(S) **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount) _____

Other (e.g., late filing surcharge): Information Disclosure Statement Fee 180

SUBMITTED BY

Signature	Eugene Kim	Registration No. (Attorney/Agent) 46,267	Telephone (650) 812-3406
Name (Print/Type)	Eugene G. Kim		Date March 7, 2005

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OIPE JC56
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PATENT & TRADEMARK OFFICE

IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Barry Alan Hoberman et al.
SERIAL NO.:	10/840,893
FILED:	May 7, 2004
TITLE:	Managing Power on Integrated Circuits Using Power Islands
EXAMINER:	Sun J. Lin
GROUP ART UNIT:	2825
ATTY.DKT.NO.:	PA2258US

MAIL STOP AMENDMENT
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
Under 37 C.F.R. §§ 1.56, and 1.97-1.98

SIR:

Pursuant to the provisions of 37 C.F.R. §§ 1.56 and 1.97-98 of the Rules of Practice in Patent Cases, enclosed herewith is form PTO-SB-08 listing several references, for which copies of the non-patent literature are enclosed. The Examiner is requested to make these references of official record in the application. The references cited may be material to examination of the application and are submitted in compliance with Applicants's duty of disclosure as defined by 37 C.F.R. § 1.56.

03/10/2005 SMINASS1 00000030 10840893
01 FC:1806 180.00 OP

{00138816v1}

No representation is made or intended as to the completeness of this list, nor is the inclusion of any reference on this list an admission that it is prior art or pertinent to this application.

Applicants hereby attach the $180 fee required by 37 C.F.R. §1.17(p) with this submission. The Commissioner is hereby authorized to charge Deposit Account No. 06-0600 for any additional fees that may be required, or credit our account for any overpayment charge. A copy of this statement is submitted in duplicate for this purpose.

Respectfully submitted,
Barry Alan Hoberman et al.

Dated: March 7, 2005 By: _____

Eugene G. Kim, Reg. No. 46,267
Carr & Ferrell *LLP*
2200 Geng Road
Palo Alto, CA 94303
TEL: (650) 812-3400
FAX: (650) 812-3444

CERTIFICATE OF MAILING

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Dated: March 7, 2005 By: _____

Eugene G. Kim, Reg. No. 46,267

{00138816v1}

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MAR 0 9 2005
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IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Barry Alan Hoberman et al.

SERIAL NO.: 10/840,893

FILED: May 7, 2004

TITLE: Managing Power on Integrated Circuits Using Power Islands

EXAMINER: Sun J. Lin

GROUP ART UNIT: 2825

ATTY.DKT.NO.: PA2258US

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ALEXANDRIA, VA 22313-1450

List of Co-Pending Patent Applications That May Be Directed Towards Similar Subject Matter

Examiner's Initials	Serial Number	First-Named Inventor	Title	Filing Date
	10/996,739	Randy J. Caplan	Systems and Methods for Minimizing Static Leakage of an Integrated Circuit	November 24, 2004
Examiner's Signature:				Date

{00138836v1}

OIPE JC556 MAR 0 9 2005 PATENT & TRADEMARK OFFICE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 5

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,598,148	07-22-2003	Moore et al.	
		US-			
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	2	of	5

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		GUPTA, R., et al., "Low Power Wireless Networked System Design," HotChips, August 18, 2002, Stanford, CA.	
		TSAI, Y-F et al., "Implications of Technology Scaling on Leakage Reduction Techniques," DAC 2003, June 2-6, 2003, ACM, Anaheim, CA, USA.	
		LI L. et al., "Managing Leakage Energy in Cache Hierarchies," Journal of Instruction-Level Parallelism, 2003, pp. 1-24, Vol. 5.	
		HU, J.S. et al., "Using Dynamic Branch Behavior for Power-Efficient Instruction Fetch," Proc. of IEEECS Annual Symposium on VLSI (ISVLSI 2003), February 20-21, 2003, Tampa, FL	
		ZHANG, W. et al., "Compiler Support for Reducing Leakage Energy Consumption," Proceedings of the 6th Design Automation and Test in Europe Conference (DATE-03), March, 2003, Munich, Germany.	
		DEGALAHAL, V. et al., "Analyzing Soft Errors in Leakage Optimized SRAM Design," Proceedings of 16th International Conference on VLSI Design, January 2003, New Delhi, India.	
		LI, L. et al., "Leakage Energy Management in Cache Hierarchies," 11th International Conference on Parallel Architectures and Compilation Techniques (PACT'02), September 2002.	
		DUARTE, D. et al., "Impact of Scaling on the Effectiveness of Dynamic Power Reduction Schemes," Proceedings of the 20th International Conference on Computer Design (ICCD), September 16-18, 2002, Freiberg, Germany.	
		DUARTE, D. et al., "Impact of Technology Scaling and Packaging on Dynamic Voltage Scaling Techniques," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, September 25-28, 2002, Rochester, NY.	
		KIM, S et al. "Predictive Precharging for Bitline Leakage Energy Reduction," Proceedings of 15th Annual IEEE International ASIC/SOC Conference, September 25-28, 2002, Rochester, NY.	

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	3	of	5

	Complete if Known
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		RAMANARAYANAN, R. et al. "Characterizing Dynamic and Leakage Power Behavior in Flip Flops," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, September 2002.	
		CHEN, G. et al. "Adaptive Garbage Collection for Battery-Operated Environments," Proceedings of USENIX JVM02 Symposium, August 2002.	
		CHEN, G. et al. "Energy Savings Through Compression in Embedded JavaEnvironments," Proceedings of the CODES'02, June 2002.	
		DELALUZ, V. et al. "Hardware and Software Techniques for Controlling DRAM Power Modes," IEEE Transaction on Computers, November 2001, Vol. 50.	
		DELALUZ, V. et al. "Scheduler-Based DRAM Energy Management," DAC 2002, June 10 - 14, 2002, New Orleans, LA, USA, ACM.	
		KIM, S. et al. "Partitioned Instruction Cache Architecture for Energy Efficiency" ACM Transactions on Computational Logic, July 2002, pp 1-23, Vol. V, No. N.	
		DE LA LUZ, V. et al. "Automatic Data Migration for Reducting Energy Consumption in Multi-Bank Memory Systems," DAC 2002, June 10 - 14, 2002, New Orleans, LA, USA.	
		DUARTE, D. et al. "Impact of Technology Scaling in the Clock System Power," Proceedings of the IEEE Computer Society Annual Symposium on VLSI, April 25-26, 2002, Pittsburgh, PA.	
		DUARTE, D. et al. "A Complete Phase-Locked Loop Power Consumption Model," Proceedings of the 2002 Design, Automation and Test in Europe Conference and Exhibition (DATE'02), 2002, IEEE.	
		DUARTE, D. et al. "Evaluating Run-Time Techniques for Leakage Power Reduction," Proceedings of the 15th International Conference on VLSI Design (VLSID'02) 2002, IEEE.	

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	4	of	5

	Complete if Known
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		ZHANG, W. "Exploiting VLIW Schedule Slacks for Dynamic and Leakage Energy Reduction," Proceedings of the 34th Annual International Symposium on Microarchitecture (MICRO'01), December 2001.	
		KIM, S. et al. "Energy Efficient Instruction Cache Using Page-Based Placement," Proceedings of International Conference on Compilers, Architectures and Synthesis for Embedded Systems, CASES'01, November 1-17, 2001, Atlanta, GA, USA.	
		HEZAVEI, J. et al. "Input Sensitive High-Level Power Analysis," Proceedings of the 2001 IEEE Workshop on Signal Processing Systems (SiPS), September 2001, pp. 149-156.	
		KIM, S. et al. "Power-aware Partitioned Cache Architectures," Proceedings of ACM/IEEE International Symposium on Low Power Electronics and Design, 2001, ILSPED'01, August 6-7, 2001, Huntington Beach, CA.	
		DELALUZ, V. "DRAM Energy Management Using Software and Hardware Directed Power Mode Control," Proceedings of the 7th International Symposium on High Performance Computer Architecture, January 20-24, 2001, Monterrey, Mexico.	
		DE MICHELI, G. et al. "System-Level Power Optimization: Techniques and Tools," DATE 2000.	
		MANNE, S. et al. "Cool Chips Tutorial," 32nd Annual International Symposium on Micorarchitecture, November 15, 1999, Haifa, Israel.	
		FILSETH, E. "Tally Power into Cost of 'Free' Silicon," EETimes, January 11, 1999, located at: http://www.eetimes.com/story/speakout/OEG19990111S028.	
		FRENKIL, J. "A Multi-Level Approach to Low-Power IC Design," IEEE Spectrum, February 1998, Vo. 35, No. 2.	
		"Managing Power in Ultra Deep Submicron ASIC/IC Design," May 2002, Synopsys, Inc.	

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 5 of 5

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Sun J. Lin
Attorney Docket Number	PA2258US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		PANGRLE, B. "Low Power Design: A Holistic Approach in an Era of New Semiconductor Technologies," San Diego Telecom Council Semiconductor SIG, November 14, 2002.	
		RABAEY, J. "Design Aids for Low Power: Part II Architecture and System Levels," 1997.	
		GRUNWALD, D. et al. "Kool Chips Workshop," MICRO33, December 10, 2000, Monterey, CA.	
		FLYNN, J. et al., "Power Management in Complex SoC Design," Synopsys, April 2004, located at http://www.synopsys.com/sps.	

Examiner Signature		Date Considered	

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US	8273

22830 7590 02/24/2005

CARR & FERRELL LLP
2200 GENG ROAD
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EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/840,893	HOBERMAN ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) ___ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/840,893 filed on 05/07/2004. Claims 1 – 54 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 5, change "consumption power" to **—power consumption—**.
Claim 1, line 7, change "consumption power" to **—power consumption—**.
Claim 17, line 5, change "consumption power" to **—power consumption—**.
Claim 17, line 6, change "consumption power" to **—power consumption—**.
Claim 39, line 6, change "consumption power" to **—power consumption—**.
Claim 39, line 7, change "consumption power" to **—power consumption—**.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE paper entitled "Managing Power and Performance for System-on-Chip using

Voltage Islands" authored by Lackey et al. in view of U.S. Patent No. 6,631,502 B2 to Buffet et al.

5. As to Claim 1, Lackey et al. show and teach the following subject matter:

- *Managing power* on an *system-on-chip (SOC)* design (i.e., *integrated circuit*) including a plurality of *voltage islands* (i.e., *power islands*) – title; abstract]; Notice that a *voltage island* is a *power island*;
- *Identifying* (i.e., *determining*) a *minimum voltage* (i.e., *target power level*) required for each *voltage island* (*power island*) to achieve its required performance – [page 196, Paragraph: Voltage Island Scenarios and Examples]; Notice that power consumption of SOC is independently controlled within each of the *voltage island* (*power island*).

Notice that power consumption level of a voltage island is determined by the voltage level of the *voltage island* (*power island*) on which it is operating. Therefore, Lackey et al. do teach determining a *power consumption level* of each *voltage island* (*power island*) in order to meet its operation voltage requirement, they do not teach a method of determining and performing an action to change the power consumption to the target power level for each *voltage island* (*power island*). But *Buffet et al.* teach a method of analyzing *voltage island power distribution network* by applying a model of *chip-level power distribution network* (for a SOC design) to (*examine*), ***calculate*** and ***update*** an appropriate *input voltage* for each *voltage transfer interface (VTI)*, based on its recently obtained input voltage, in order to adaptively *adjust* its input voltage to generate a *desired voltage* for each *voltage island* – [abstract; col. 2, line 13 – 67; Figs. 1 – 10].

Notice that (1) the *desired voltage* is provided to each *voltage island* in order to achieve its *target power level* (2) applying model for *calculating*, *updating* and *adjusting* input voltage of a *VTI* is a method of determining and performing an action to change a suitable *voltage level* (i.e., *power consumption level*) of a *voltage island* in order to achieve its *target power level*.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Buffet et al.* in

analyzing *voltage island power distribution network* by applying a model of *chip-level power distribution network* for a SOC design including a plurality of *voltage islands* (*power islands*) to *calculate* and *update* an appropriate *input voltage* for each *voltage transfer interface (VTI)*, based on its recently obtained input voltage, in order to *adaptively adjust* its *input voltage* to generate a suitable *voltage level* for to achieve a *target power level* for each voltage island (power island) for use in managing power on the SOC.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claim 17, in addition to reasons included in **[Response A]** given above, *Buffet et al.* and *Lackey et al.* teach the following subject matter:

- *Voltage island power distribution network* (i.e., *power control circuitry*) for integrated circuit chip (e.g., system-on-chip, SOC) design – [*Buffet et al.*: abstract; col. 1, line 13 – 20; Fig. 2];
- *Power management Unit* (i.e., *power manager*) – [*Lackey et al.*: Fig. 4]. Notice that the *Power management Unit* (*power manager*) is in charge of identifying (determining) *a* minimum voltage (*target power level*) required for each voltage island (power island) to achieve its required performance – [*Lackey et al.*: page 196, Paragraph: Voltage Island Scenarios and Examples];
- For reducing power consumption by IC chips on a SOC, function blocks, which are driven by *different voltage islands*, can be selectively *powered up* or *power down* or even *powered at voltage levels* that are different from chip-level voltages (e.g., during sleep state) – [*Buffet et al.*: col. 1, line 13 – 35].

For reference purposes, the explanations given above in response to Claim 17 are called **[Response B]** hereinafter.

7. As to Claim 39, in addition to reasons included in **[Response A]** and **[Response B]** given above, *Buffet et al.* show in Fig. 10 a *RAM 240* and *ROM 245*, which are *software storage medium* operational to store power management software.

8. As to Claims 2, 18 and 40, *Lackey et al.* teach subject matter regarding *geographic factors* associated with *voltage islands* (*power islands*) that (1) *voltage islands* must be *floor-planned* (placed) in close proximity with chip pins corresponding to its off-chip power source (2) On-chip power sources must also be placed within the *voltage island* – [page 201, paragraph: Physical Planning and Implementation of Structure].

9. As to Claims 3, 19 and 41, *Lackey et al.* teach subject matter regarding *functional circuitry* associated with *voltage islands* (*power islands*) that (1) partitioning of an SOC involves division and subdivision into an n-level *functional hierarchy* ... functional components (i.e., functional circuitry) (2) designing for *voltage islands* places additional requirements on the *functional partition process* – [page 199, paragraph: Functional Partitioning].

10. As to Claims 4, 20 and 42, *Lackey et al.* show in Fig. 4 and teach subject matter regarding *power sub-islands* (e.g., *child voltage islands*) that (1) *voltage islands* can be used at *different levels of design hierarchy* (2) *voltage island* capable of fine *hierarchical granularity* – [Fig. 4; page 197, right column below Fig. 4] (3) *parent (voltage) island* – [page 198, description above Fig. 5].

For reference purposes, the explanations given above in response to Claims 4, 20 and 42 are called **[Response C]** hereinafter.

11. As to Claims 5 – 7, 21 – 23 and 43 – 45, *Lackey et al.* show in Fig. 3 teach subject matter regarding *multiple clock domains* of voltage islands that (1) applying clock gating to limit active power ... voltage islands ... power management – [page 196, paragraph on left column below Fig. 2] (2) *functional blocks* operating with *different voltage levels* in different *frequency clock domains* (e.g., 150 MHz, 400 MHz) – [Fig. 3; page 196 right column]. Notice that an appropriate *clock* and associated *clock frequency* are selected for each power island.

For reference purposes, the explanations given above in response to Claims 5 – 7, 21 – 23 and 43 – 45 are called **[Response D]** hereinafter.

12. As to Claims 8 – 10, 24 – 26 and 46 – 48, *Lackey et al.* teach (1) relationship between *threshold voltage (Vt)* and power leakage (2) *voltage island architecture methods* ... *multiple-threshold (voltage) design technique* (3) change *supply voltage level* associated with a low-Vt block in order to reduce its power leakage (4) completely shut off *supply voltage level* associated with a low-Vt during sleep modes to eliminate standby power – [page 197, paragraph: System-level Power management Approaches]. Notice that a first voltage can be the *supply voltage* (i.e., *source voltage*) and/or the *threshold voltage Vt*.

13. As to Claims 11 – 13, 27 – 29 and 49 – 51, *Buffet et al.* and *Lackey et al.* teach the following subject matter:

- An action of selectively *powering on* or *powering off* or *another appropriate voltage* for one of *voltage islands* (*power islands*) – [*Buffet et al.*: col. 1, line 20 – 28];
- On-chip ***power-switching circuitry***; an action of *switching* (i.e., *changing*) one of *voltage islands* (*power islands*) to a *sleep mode*, *power off state* or an *power on state* – [*Lackey et al.*: page 196, right column; page 200, right column; Fig. 4].

For reference purposes, the explanations given above in response to Claims 11 – 13, 27 – 29 and 49 – 51 are called **[Response E]** hereinafter.

14. As to Claims 14, 30 and 52, in addition to reasons included in **[Response A]** and **[Response B]** given above, *Buffet et al. teach* (1) updating *output voltage value* of *voltage translation interface* (VTI) – [col. 2, line 57 – 58] (2) *comparing* (i.e., *monitoring*) the *updated* (*output voltage*) *value* .... updating, if necessary, if (output voltage level) not converged within a *preset limit* (i.e., *preset threshold level*) – [col. 2, line 62 – 67].

15. As to Claim 15, 16, 31, 32, 53 and 54, *Lackey et al.* show and teach the subject matter regarding *save* and *restore* necessary logic states (of components) within in one of voltage islands – [Fig. 5; page 189, paragraph State-Saving]. Notice that, as shown in Fig. 5, the logic states are stored in special state-saving latches, which serve as a memory.

16. As to Claim 33, *Lackey et al.* show in Fig. 4 and teach the subject matter regarding coupling the *power management unit* (*power manager*) to the *voltage islands* V1, V11, V2, and V22. Notice that the wires utilized for performing the coupling and be grouped together as a *bus*.

17. As to Claims 34 and 35, *Lackey et al.* teach implementing *voltage islands* in *different levels of design hierarchy* in **[Response C]** given above. Notice that (1) the *voltage islands* can have many *hierarchical levels* (e.g., *parent voltage islands*, *children voltage islands*, etc.) (2) In order to effectively *control voltage levels* in different hierarchy, it is inherent that the *power manger* should comprise a *master power manager* and a *slave power manager* (3) the *master power manager* is configured to control *voltage levels* of the SOC at *higher hierarchical level* (e.g., *parent voltage islands*); whereas the *slave power manager*, which is coordinated by the *master power manager*, is configured to control *voltage levels* of *voltage islands* at a *lower hierarchical level* (e.g., *children voltage islands*).

18. As to Claim 36, in addition to *clock gating* scheme and *multiple frequency clocks* explained in **[Response A]** and **[Response D]**, respectively, *Lackey et al.* teach implementing *timing clock distribution structure* for *voltage islands* with different power sources – [Page 200, left column]. Notice that the multiply frequency clocks can be distributed using a *clock multiplexing circuitry*.

19. As to Claim 37, *Lackey et al.* show in Fig. 4 and teach implementing a *power switching circuitry* as explained in **[Response E]** given above. Notice that the (1) *power switching circuitry* can be utilized to *instantly switch* voltage of a *voltage island* to a

power-on state, a *power-off state* or a *sleep mode* (2) *power switching circuitry* can be realized using *multiplexing circuitry* (e.g., .

20. As to Claim 38, *Lackey et al.* teach implementing *voltage level-shifting circuits* (*Level Shifters*) for *voltage islands* – [Page 200, left column].

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
February 22, 2005

Notice of References Cited	Application/Control No. 10/840,893	Applicant(s)/Patent Under Reexamination HOBERMAN ET AL.	
	Examiner Sun J. Lin	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,462,976 B1	10-2002	Olejniczak et al.	363/147
	B	US-6,631,502 B2	10-2003	Buffet et al.	716/4
	C	US-6,667,648 B2	12-2003	Stout et al.	327/333
	D	US-6,779,163 B2	08-2004	Bednar et al.	716/7
	E	US-6,820,240 B2	11-2004	Bednar et al.	716/1
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lackey et al. "Managing Power and Performance for System-on-Chip Design using Voltage Islands", Nov. 2002, IEEE International Conference on Computer Aided Design, pp. 195 - 202.
	V	"Sloving the Power Management Dilemma in System-On-Chip Asic Design", April 2002, IBM Technology Group.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/840,893	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J. Lin	2825

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim Final	Claim Original	Date 2/22/05								Claim Final	Claim Original	Date 2/22/05								Claim Final	Claim Original	Date							
	1	√									51	√									101								
	2	√									52	√									102								
	3	√									53	√									103								
	4	√									54	√									104								
	5	√									55										105								
	6	√									56										106								
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Bib Data Sheet

CONFIRMATION NO. 8273

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/840,893	05/07/2004 RULE	716	2825	PA2258US

APPLICANTS

Barry Alan Hoberman, Cupertino, CA;

Daniel L. Hillman, San Jose, CA;
Jon Shiell, San Jose, CA;

** CONTINUING DATA ********** Yes

This appln claims benefit of 60/468,742 05/07/2003

** FOREIGN APPLICATIONS ********** NONE

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 07/12/2004

Foreign Priority claimed ☐ yes ☑ no 35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	STATE OR COUNTRY CA	SHEETS DRAWING 13	TOTAL CLAIMS 54	INDEPENDENT CLAIMS 3

ADDRESS
22830
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2200 GENG ROAD
PALO ALTO , CA
94303

TITLE
Managing power on integrated circuits using power islands

FILING FEE RECEIVED 1512	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/840,893	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J. Lin	2825

SEARCHED

Class	Subclass	Date	Examiner
716	6	2/14/2005	JSL
716	5	2/14/2005	JSL
716	4	2/14/2005	JSL
716	1	2/14/2005	JSL

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

	DATE	EXMR
EAST [USPAT;US-PGPUB;UPO;JPO;DERWENT;IBM_TDB]	2/14/2005	JSL
EAST [USPAT;US-PGPUB;UPO;JPO;DERWENT;IBM_TDB]	2/14/2005	JSL
IEEE	2/14/2005	JSL
GOOGLE	2/14/2005	JSL

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1535	716/6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:47
S2	1788	716/5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:41
S3	2325	716/4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:41
S4	1821	716/1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:41
S5	1	(716/6).ccls. and (power adj island) and (target or threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:50
S6	2	(716/5).ccls. and (power adj island) and (target or threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:51
S7	0	(716/4).ccls. and (power adj island) and (target or threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:51
S8	0	(716/1).ccls. and (power adj island) and (target or threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:51
S9	2	("716"/$).ccls. and (power adj island) and (target or threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 14:52

S10	5	(power adj island) and (target or threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 15:00
S11	36	(power adj island)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:58
S12	2	(power adj island) and (power adj control)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 15:01
S13	10	(power adj island) and (IC or (integrated adj circuit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:18
S14	3	(power adj island) and (IC or (integrated adj circuit)) and (power adj consumption)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 15:18
S15	0	(power adj island) and (IC or (integrated adj circuit)) and (power adj mangement)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:18
S16	0	(power adj island) and (IC or (integrated adj circuit)) and (power adj mang$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:19
S17	2	(power adj island) and (IC or (integrated adj circuit)) and (power adj manag$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:26
S18	2	(power adj island) and (IC or (integrated adj circuit)) and (threshold adj voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:29
S19	0	(power adj island) and (sub adj island)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:30

S20	1	(power adj island) and (sub adj islands)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:31
S21	12	(power adj island) and (monitor$ or detect$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/14 17:34
S22	44	(power adj islands)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/14 17:59
S23	2	("6631502").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 11:21
S24	122	(voltage adj islands) or (voltage adj island)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 11:23
S25	10	((voltage adj islands) or (voltage adj island)) same (power adj management)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 13:00
S26	0	((voltage adj islands) or (voltage adj island)) same (power adj management) and monitor$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 14:18
S27	0	((voltage adj islands) or (voltage adj island)) same (target adj (power adj level))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 15:29
S28	1	((voltage adj islands) or (voltage adj island)) and (target adj (power adj level))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 15:31
S29	0	((voltage adj islands) or (voltage adj island)) and (monitor$ adj ((power or voltage) adj level))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 15:33

S30	9	((voltage adj islands) or (voltage adj island)) and (monitor$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 15:47
S31	5	((voltage adj islands) or (voltage adj island)) same (monitor$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 15:33
S32	4	((voltage adj islands) or (voltage adj island)) and (power adj (manage or control))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 15:49
S33	246	(monitoring same (power adj consumption) same threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 17:06
S34	1	("716"/$).ccls. and (monitoring same (power adj consumption) same threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 16:12
S35	1	((voltage adj island) or (voltage adj islands)) and (monitoring same (power adj consumption) same threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 16:13
S36	65	(monitoring same (power adj consumption) same level same threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 16:21
S37	7	((monitoring adj (power adj consumption)) same threshold)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/02/15 17:33

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1 **Managing power and performance for system-on-chip designs using Voltage Islands**
Lackey, D.E.; Zuchowski, P.S.; Bednar, T.R.; Stout, D.W.; Gould, S.W.; Cohn, J.M.;
Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conferen on , 10-14 Nov. 2002
Pages:195 - 202

[Abstract] [PDF Full-Text (629 KB)] **IEEE CNF**

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2 **Energy-efficient low-voltage operation of digital CMOS circuits throu charge-recycling**
Rajapandian, S.; Zheng Xu; Shepard, K.L.;
VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on , 17-19 2004
Pages:330 - 333

[Abstract] [PDF Full-Text (453 KB)] **IEEE CNF**

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3 **New trends in low power SoC design technologies**
Wei Hwang;
SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip] , Sept. 2003
Pages:422

[Abstract] [PDF Full-Text (185 KB)] **IEEE CNF**

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... a "known" state on the nets that connect other **power islands** the same circuits and also handle data communication When the **voltage islands** are powered up. ...
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... For small **power** systems, such as an **island** grid, or a weakly supported ... The **power control** interface can also use its energy storage capacity to provide voltage ...
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1 **Power bus isolation using power islands in printed circuit boards**
Chen, J.; Hubing, T.H.; Van Doren, T.P.; DuBroff, R.E.;
Electromagnetic Compatibility, IEEE Transactions on , Volume: 44 , Issue: 2 , May 2002
Pages:373 - 380

[Abstract] [PDF Full-Text (323 KB)] IEEE JNL

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2 **DC power bus noise isolation with power islands**
Cui, W.; Fan, J.; Shi, H.; Drewniak, J.L.;
Electromagnetic Compatibility, 2001. EMC. 2001 IEEE International Symposium on , Volume: 2 , Aug. 2001
Pages:899 - 903 vol.2

[Abstract] [PDF Full-Text (392 KB)] IEEE CNF

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3 **RF isolation using power islands in DC power bus design**
Jun Fan; Yong Ren; Juan Chen; Hockanson, D.M.; Hao Shi; Drewniak, J.L.; Hubing, T.H.; Van Do. T.P.; DuBroff, R.E.;
Electromagnetic Compatibility, 1999 IEEE International Symposium on , Volume: 2 , 2-6 Aug. 19
Pages:838 - 843 vol.2

[Abstract] [PDF Full-Text (468 KB)] IEEE CNF

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4 **Power bus noise reduction using power islands in printed circuit board designs**
Hubing, T.; Chen, J.; Drewniak, J.; Van Doren, T.; Ren, Y.; Fan, J.; DuBroff, R.;
Electromagnetic Compatibility, 1999 International Symposium on , 17-21 May 1999
Pages:1 - 4

[Abstract] [PDF Full-Text (204 KB)] IEEE CNF

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5 **DC power-bus noise isolation with power-plane segmentation**
Wei Cui; Jun Fan; Yong Ren; Hao Shi; Drewniak, J.L.; DuBroff, R.E.;
Electromagnetic Compatibility, IEEE Transactions on , Volume: 45 , Issue: 2 , May 2003
Pages:436 - 443

[Abstract] [PDF Full-Text (423 KB)] IEEE JNL

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6 **A multi-function relay for loss of mains protection**
Heggie, G.; Yip, H.T.;
System Implications of Embedded Generation and Its Protection and Control (Digest No. 1997/27
Colloquium on , 25 Feb. 1998

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IFW

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SEP 07 2004
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US

CONFIRMATION NO. 8273

22830
CARR & FERRELL LLP
2200 GENG ROAD
PALO ALTO, CA 94303

FORMALITIES LETTER

OC000000013214376

Date Mailed: 07/13/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

09/09/2004 MMEKONEN 00000013 10840893
01 FC:1051 130.00 OP

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Jinhehan

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Initial Patent Examination Division (703) 308-1202
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	2825
Examiner Name	Unknown
Total Number of Pages in This Submission: 12	Attorney Docket Number: PA2258US

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [x] Response to Missing Parts/ Incomplete Application
  - [x] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):
  (1) Copy of Notice to File Missing Parts;
  (2) Declaration and Power of Attorney;
  (3) Confirmation Postcard
  (4) Check for $130.00

Remarks: Total page number does not include postcard and check.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Carr & Ferrell LLP Cust. No. 22830
Signature	Eugene Kim Reg. No. 46,267
Date	September 1, 2004

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Eugene G. Kim, Reg. No. 46,267		
Signature	Eugene Kim	Date	September 1, 2004

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 130.00

Complete if Known	
Application Number	10/840,893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Examiner Name	Unknown
Art Unit	2825
Attorney Docket No.	PA2258US

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 06-0600

Deposit Account Name: Carr & Ferrell LLP

The Director is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☐ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		x		=
Independent Claims		-3** =		x		=
Multiple Dependent						=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	130
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 130.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Eugene G. Kim	*Registration No. (Attorney/Agent)*	46,267	*Telephone*	650-812-3406
Signature	Eugene Kim			*Date*	September 1, 2004

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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OIPE JC86
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PATENT & TRADEMARK OFFICE

IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Barry Alan Hoberman, et al
SERIAL NO.:	10/840,893
FILING DATE:	May 7, 2004
ART UNIT:	2825
CONF. NO.:	8273
TITLE:	Managing Power on Integrated Circuits Using Power Islands
ATTY.DKT.NO.:	PA2258US

MAIL STOP MISSING PARTS
COMMISSIONER FOR PATENTS
P.O BOX 1450
ALEXANDRIA, VA 22313-1450

RESPONSE TO NOTICE TO FILE MISSING PARTS OF AN APPLICATION

SIR:

Responsive the Notice to File Missing Parts of Nonprovisional Application, dated July 13, 2004 and received in the above-identified patent application, Applicants are enclosing:

(1) a copy of the Notice to File Missing Parts;

(2) a signed Declaration and Power of Attorney;

(3) a check for $ 130 to cover the filing fee and surcharge.

{00124214v1}

Please charge our Deposit Account No. 06-0600 for any additional fees which may be required or credit our account for any overpayment. A copy of this letter is enclosed for this purpose.

Respectfully submitted,
Barry Hoberman, et al

Date: September 1, 2004

By: _____

Eugene G. Kim, Reg. No. 46,267
Carr & Ferrell, *LLP*
2200 Geng Road
Palo Alto, CA 94303
TEL: (650) 812-3400
FAX: (650) 812-3444

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date printed below:

Date: September 1, 2004

_____
Eugene G. Kim

{00124214v1}

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PATENT & TRADEMARK OFFICE

ATTORNEY'S DOCKET NO.: PA2258US

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

"Managing Power on Integrated Circuits Using Power Islands"

which was filed in the United States Patent and Trademark Office on May 7, 2004 and assigned serial number 10/840,893.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under Title 35, United States Code §119(a)-(d) or (f) or §365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):

Number	Country	Foreign Filing Date	Priority Claimed?	Certified Copy Attached?
(Number)	(Country)	(MM/DD/YYYY)	☐ Yes ☐ No	☐ Yes ☐ No
(Number)	(Country)	(MM/DD/YYYY)	☐ Yes ☐ No	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

Prior Provisional Applications:

60/468,742	May 7, 2003
(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Prior U.S. or PCT Applications Designating the U.S.:

(Application Number)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status -- patented, pending, abandoned)

POWER OF ATTORNEY: I hereby appoint the attorney(s) and/or agent(s) associated with the customer number **22830** to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

SEND ALL CORRESPONDENCE TO:

CARR & FERRELL *LLP*
2200 Geng Road
Palo Alto, CA 94303
TEL: (650) 812-3400
FAX: (650) 812-3444

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: Barry Alan Hoberman Citizenship: U.S.A.

Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: Barry Alan Hoberman Dated: 7/29/04

(Permanent ink only) *(Date of Signature)*

Mailing Address: 10290 Palo Vista Road, Cupertino, CA 95014

(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address: Same

(if the inventor lives at a location different than his/her mailing address)

Full name of second inventor: Daniel L. Hillman Citizenship: U.S.A.

Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: Daniel L Hillman Dated: 7-28-04

(Permanent ink only) *(Date of Signature)*

Mailing Address: 6607 Winterset Way, San Jose, CA 95120

(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address: Same

(if the inventor lives at a location different than his/her mailing address)

Full name of third inventor: Jon Shiell Citizenship: U.S.A.

Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: Jon Shiell Dated: 8-04-04

(Permanent ink only) *(Date of Signature)*

Mailing Address: 801 Seabury Drive, San Jose, CA 95136

(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address:

(if the inventor lives at a location different than his/her mailing address)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US

CONFIRMATION NO. 8273

22830
CARR & FERRELL LLP
2200 GENG ROAD
PALO ALTO, CA 94303

FORMALITIES LETTER

OC000000013214376

Date Mailed: 07/14/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a Large Entity

- **$130** Late oath or declaration Surcharge.

Replies should be mailed to: Mail Stop Missing Parts
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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/840,893	05/07/2004	Barry Alan Hoberman	PA2258US

CONFIRMATION NO. 8273

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2200 GENG ROAD
PALO ALTO, CA 94303

FORMALITIES LETTER

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Date Mailed: 07/13/2004

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

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- **$130** Late oath or declaration Surcharge.

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	Unknown 10840893
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	PA2258US
Total Number of Pages in This Submission	3

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☑ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please Identify below):

1) Postcard

Remarks: Total page number does not include postcard.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Carr & Ferrell LLP Cust. No. 22830
Signature	Eric J. Worthington Reg. No. 50,910
Date	July 9, 2004

CERTIFICATE OF TRANSMISSION/MAILING

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Typed or printed name	Eric J. Worthington Reg. No. 50,910		
Signature	Eric J. Worthington	Date	July 9, 2004

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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OIPE JC142
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PATENT & TRADEMARK OFFICE

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Barry Alan Hoberman, et al.
SERIAL NO.:	Unknown
FILING DATE:	May 7, 2004
TITLE:	Managing Power on Integrated Circuits Using Power Islands
EXAMINER:	Unknown
ART UNIT:	Unknown
ATTY. DKT. NO.:	PA2258US

STATEMENT IN SUPPORT OF PETITION TO MAKE SPECIAL
UNDER 37 C.F.R 1.102(c)
ON THE BASIS OF ENERGY CONSERVATION (M.P.E.P. § 708.02 (VI))

1. I represent the inventors and applicants for the above-identified patent application.

2. With regard to energy conservation, embodiments of the invention relate to the reduction of energy consumption in industrial equipment, household appliances, etc.

3. The invention reduces power consumption of an integrated circuit by managing power on power islands in the integrated circuit. In some examples, the invention controls the voltage or frequency in the power island to more efficiently consume power and reduce the overall power consumption of the integrated circuit.

4. In a particular example, embodiments of the invention reduce power requirements for personal computers (i.e., "green PCs") and other industrial equipment, thereby reducing power drawn from electricity generation stations (i.e., AC power). Other embodiments of the invention reduce power consumption in integrated circuits for

battery-powered devices, for example, cellular phones, laptop computers, handheld gaming devices, digital cameras, and personal digital assistants (PDAs). Reduction in power consumption in these devices extends battery life and reduces the frequency of battery recharging, reducing AC power drawn by the devices.

5. Further with regard to energy conservation, embodiments of the invention lower the heat dissipation of an integrated circuit. With lower heat dissipation, the need for cooling fans or heat sinks for the integrated circuit is reduced. Reducing cooling needs (e.g., air conditioning) further reduces power drawn from electricity generation stations.

6. In summary, the cumulative effect of a reduction of power consumption on an individual integrated circuit multiplied by the vast number of integrated circuits included in devices like personal computers, cellular phones, laptop computers, handheld gaming devices, digital cameras, and PDAs materially contributes to the conservation of energy resources. Therefore, applicants respectfully request granting the petition to make the above referenced patent application special.

Date: JULY 9, 2004

Eric Worthington, Reg. No. 50,910

EV400682755US

22763 U.S. PTO 050704

PTO/SB/05 (01-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	PA2258US
First Inventor	Barry Alan Hoberman
Title	Managing Power on Integrated Circuits ...
Express Mail Label No.	EV 400682755 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Mail Stop Patent Application**
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

16834 U.S. PTO 10/840893 050704

1. ☑ Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☑ Specification [*Total Pages* 33]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☑ Drawing(s) (*35 U.S.C. 113*) [*Total Sheets* 13]
5. Oath or Declaration [*Total Sheets* 3]
   a. ☐ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 18 completed)*
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☑ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. ☑ Other: Check for $1,382.00

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: .....

Prior application information: *Examiner* _____ *Art Unit:* _____

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19. CORRESPONDENCE ADDRESS

☑ Customer Number: 22830 *OR* ☐ Correspondence address below

Name					
Address					
City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	Eugene G. Kim	*Registration No. (Attorney/Agent)*	46,267
Signature	Eugene G. Kim	*Date*	May 7, 2004

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22763 U.S. PTO
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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1,382.00

Complete if Known	
Application Number	Unknown
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Examiner Name	Unknown
Art Unit	Unknown
Attorney Docket No.	PA2258US

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 06-0600

Deposit Account Name: Carr & Ferrell LLP

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	770
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 770.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims	54	-20** =	34	x	18	=	612
Independent Claims	3	-3** =	0	x		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 612.00

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
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1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
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1453	1,330	2453	665	Petition to revive - unintentional	
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1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
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1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

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SUBTOTAL (3) ($)

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Eugene G. Kim	*Registration No. (Attorney/Agent)*	46,267	*Telephone*	650-812-3406
Signature				*Date*	May 7, 2004

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	PA2258US
First Inventor	Barry Alan Hoberman
Title	Managing Power on Integrated Circuits ...
Express Mail Label No.	EV 400682755 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Mail Stop Patent Application**
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16834 U.S. PTO 10/840893 050704

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   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
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   - Abstract of the Disclosure
4. ☑ Drawing(s) (*35 U.S.C. 113*) [*Total Sheets* 13]
5. Oath or Declaration [*Total Sheets* 3]
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      Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
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ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
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15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
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17. ☑ Other: Check for $1,382.00

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☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: .....

Prior application information: *Examiner* _____ *Art Unit:* _____

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☑ Customer Number: 22830 *OR* ☐ Correspondence address below

Name					
Address					
City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	Eugene G. Kim	*Registration No. (Attorney/Agent)*	46,267
Signature	Eugene G. Kim	*Date*	May 7, 2004

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1,382.00

Complete if Known	
Application Number	Unknown
Filing Date	May 7, 2004
First Named Inventor	Barry Alan Hoberman
Examiner Name	Unknown
Art Unit	Unknown
Attorney Docket No.	PA2258US

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 06-0600

Deposit Account Name: Carr & Ferrell LLP

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☑ Credit any overpayments

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SUBTOTAL (1) ($) 770.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
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Independent Claims	3	-3** =	0	x		=	
Multiple Dependent						=	

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FEE CALCULATION (continued)

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1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

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SUBTOTAL (3) ($)

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Eugene G. Kim	*Registration No. (Attorney/Agent)*	46,267	*Telephone*	650-812-3406
Signature				*Date*	May 7, 2004

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

MANAGING POWER

ON INTEGRATED CIRCUITS

USING POWER ISLANDS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application Serial Number 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which is hereby incorporated by reference.

BACKGROUND

1. Field of the Invention

[0002] The present invention relates generally to integrated circuits, and more particularly to managing power on integrated circuits using power islands.

2. Description of the Prior Art

[0003] One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heat dissipation of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

[0004] Some integrated circuits are designed using building blocks of library cells. These library cells are blocks of circuitry performing a function. Some examples of library cells are NAND gates, multiplexers, decoders, comparators, and memory.

[0005] In a "full-custom" flow, the integrated circuit is designed at the lowest level such as at the individual transistors, capacitors, and resistors level. The "full-custom" flow may use library cells that are internally developed. The integrated circuit can have optimal performance because the integrated circuit is designed in great detail at the lowest level. However, some problems with the "full-custom" flow are the long time and expensive costs associated with designing at such a detailed level. Furthermore, the "full-custom" flow is cumbersome because the design is at the lowest level.

[0006] In a "standard-cell" flow, the integrated circuit is designed using library cells acquired from a third party or other outside source. These library cells are standardized at the logic or function level. The design time for the standard-cell flow is reduced because the library cells are already pre-designed and pre-tested.

[0007] In one example for designing an integrated circuit, the library cells are selected, and the custom logic is specified to build the integrated circuit. The register transfer level (RTL) for the integrated circuit is then written for simulation and debugging. After simulation and debugging, the synthesis is run for the integrated circuit. Performance measurement software is executed to determine performance of the integrated circuit. The final synthesis of the integrated circuit can then be run based on the optimal performance of the integrated circuit.

[0008] One problem with many integrated circuits is that power consumption is not efficiently utilized. For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency. In another example, inactive circuitry within the integrated

circuit consumes power and increases the likelihood of leakage. Inefficient power consumption may also adversely affect performance of the integrated circuit.

[0009] With the growing complexity of integrated circuits, the reduction of power consumption is even more important when the integrated circuit employs more functionality. One example of an integrated circuit is a system-on-a-chip that includes a microprocessor, memory, I/O interfaces, and an analog-to-digital converter all in a single chip. With many different types of functionality employed within a single chip, the system-on-a-chip consumes even more power than single function integrated circuits.

[00010] Some prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption. One problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static. The voltages and the frequencies do not dynamically change based on the needs and operation of the integrated circuit.

SUMMARY OF THE INVENTION

[00011] The invention addresses the above problems by managing power in an integrated circuit using power islands. The integrated circuit includes a plurality of power islands where power consumption is independently controlled within each of the power islands. A power manager determines a target power level for one of the power islands. The power manager then determines an action to change a consumption power level of the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level. Power control circuitry controls the power of the one of the power islands.

[00012] The power islands may be delineated based on geographic factors or functional circuitry of the integrated circuit. In some embodiments, the action is selecting a clock frequency for one of the power islands or selecting a clock for one of the power islands. In some embodiments, the action is modifying voltage for one of the power islands. The action may be powering on or off one of the power islands.

[00013] In some embodiments, the power manager monitors the power consumption level of one of the power islands, determines whether a threshold level was crossed based on the power consumption level, and performs the action based on the crossing of the threshold level. In some embodiments, the power manager saves and restores a state of components within one of the power islands.

BRIEF DESCRIPTION OF THE DRAWINGS

[00014] FIG. 1 is a block diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

[00015] FIG. 2 is a diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

[00016] FIG. 3 is an illustration for low leakage circuitry for a low power standard cell logic block in an exemplary implementation of the invention;

[00017] FIG. 4 is a diagram of a power island in an exemplary implementation of the invention;

[00018] FIG. 5 is a flowchart from an application request to a slave power manager action in an exemplary implementation of the invention;

[00019] FIG. 6 is an illustration of internal circuitry for a smart power unit in an exemplary implementation of the invention;

[00020] FIG. 7 is an illustration of external circuitry for a smart power unit in an exemplary implementation of the invention;

[00021] FIG. 8 is a flowchart from an application request to a smart power unit action in an exemplary implementation of the invention;

[00022] FIG. 9 is a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention;

[00023] FIG. 10 is diagram of a system on a chip and an extended local memory in an exemplary implementation of the invention;

[00024] FIG. 11 is a flowchart for generating a "hot spot" report from an intermediate power manager to a power management control layer in an exemplary implementation of the invention.

[00025] FIG. 12 is a diagram of a system on a chip in an exemplary implementation of the invention; and

[00026] FIG. 13 is a flowchart for building a chip with power islands in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[00027] As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

[00028] FIG. 1 depicts a block diagram of a system 100 for managing power in an integrated circuit 110 in an exemplary implementation of the invention. The system 100 includes an integrated circuit 110 and a power manager 120. The integrated circuit 110 is any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit 110 is a system-on-a-chip. The integrated circuit 110 includes multiple IP units, which are blocks of circuitry performing specific functions.

[00029] The integrated circuit 110 includes four power islands 112, 114, 116, and 118. FIG. 1 only depicts four power islands 112, 114, 116, and 118 for the sake of simplicity. Other embodiments of the integrated circuit 110 include a plurality of power islands 112, 114, 116, and 118. The power islands 112, 114, 116, and 118 are coupled to a bus 125.

[00030] A power island 112, 114, 116, and 118 is any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on geographic factors of the integrated circuit 110. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on functional IP units of the integrated circuit 110. In one example depicted in FIG. 10, power islands are delineated by memory, a

microprocessor, and separate IP blocks. In some embodiments, the power islands 112, 114, 116, and 118 are asynchronous or synchronous to each other. In some embodiments, the power islands 112, 114, 116, and 118 comprise sub-islands of power to provide further specificity in controlling power in the integrated circuit 110. In some embodiments, each of the power islands 112, 114, 116, and 118 supports multiple clock domains with its own control. In some embodiments, the clocks within the power islands 112, 114, 116, and 118 are variable.

[00031] In some embodiments, each of the power islands 112, 114, 116, and 118 includes power control circuitry. Power control circuitry is any circuitry configured to control power within one of the power islands 112, 114, 116, and 118. Some examples of power control circuitry include circuitry for level shifting, signal isolation, Vdd multiplexing, clock multiplexing, and dynamic back bias. In some embodiments, the power control circuitry is included in a standard cell library for standard cell design of the integrated circuit 110.

[00032] The power manager 120 is also coupled to the bus 125. One example of the bus 125 is a power command bus described in further detail below in FIG. 10. Other embodiments of the system 100 include numerous variations in which the power manager 120 and the power islands 112, 114, 116, and 118 are interconnected. The power manager 120 is any circuitry, device, or system configured to (1) determine a target power level for one of the power islands 112, 114, 116, and 118 where power consumption is independently controlled within each of the power islands 112, 114, 116, and 118, (2) determine action to change a consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level, and (3) perform the action to change the consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level. The power manager 120 can dynamically change the power consumption of the power islands 112, 114, 116, and 118 based on the needs and operation of the integrated circuit 110. The target power level is a desired, calculated, or specified power consumption of the power islands

112, 114, 116, and 118. Some examples of the power manager 120 are the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM), which are described in further detail below. The power manager 120 may be a hierarchy or group of power managers 120. Although FIG. 1 depicts the power manager 120 as being located outside the integrated circuit 110, other embodiments may have the power manager 120 located in the integrated circuit 110. In other embodiments, the power manager 120 may be distributed among multiple power managers that are on or off the integrated circuit 110 or integrated with a CPU.

[00033] The action is any instruction, message, process, function, signal, or variable that controls power consumption in the power island 112, 114, 116, and 118. Some examples of actions are clock gating and dynamic clock selection. Another example of an action is modifying a clock frequency of one of the power islands 112, 114, 116, and 118. Another example of an action is to modify voltage of one of the power islands 112, 114, 116, and 118 such as dynamic voltage source, Vdd, selection. Another example of an action is to control dynamic leakage by controlling variable Vt transistors.

[00034] FIG. 2 depicts a diagram of a system 200 for managing power in an integrated circuit 250 in an exemplary implementation of the invention. The system 200 includes an embedded firmware stack 210 and an integrated circuit 250. The embedded firmware stack 210 includes software layers that run on a central processing unit (CPU). In some embodiments, the embedded firmware stack 210 may include an application layer 212, an operating system (OS) sub-system 216, a power management control layer (PMCL) 218, a real-time operating system (RTOS) 220, I/O drivers 222, and power manager (PM) firmware 224 for the MPM, IPM and/or SPM.

[00035] The integrated circuit 250 includes a power island 260, a power island 270, and a MPM 280. The power island 260 includes a low power standard cell logic block 262 and a SPM 264. The power island 270 includes a low power memory block 272 and a SPM 274. The low

power standard cell logic block 262 and the low power memory block are coupled to an interface 265. The MPM 280 is coupled to the PMCL 218, the SPM 264, and the SPM 274.

[00036] In some embodiments, the application layer 212 includes a global power application layer (GPAL) 214. This GPAL 214 may be useful for more complex applications. If the GPAL 214 is present, then all calls to the PMCL 218 application program interfaces (API) are first directed to the GPAL 214. Both the GPAL 214 and the PMCL 218 provide power management for the integrated circuit 250. In some embodiments, the GPAL 214 and/or the PMCL 218 monitor what load is on each power island 260 and 270. Also, the GPAL 214 and/or the PMCL 218 may build a history of power levels on the power island 260 and 270 and store the history data in a database. The GPAL 214 and the PMCL 218 may also provide data for on-demand resources interested in the power levels of the power islands 260 and 270.

[00037] In some embodiments when the GPAL 214 is present, the GPAL 214 provides guidance to the PMCL 218 in making local decisions for power management of the integrated circuit 250. In some embodiments, the GPAL 214 and the PMCL 218 include complex algorithms for a static schedule. The GPAL 214 and the PMCL 218 provide the facility for use code to interact and control power behavior and parameters including providing a database and statistics.

[00038] The PMCL 218 also collects information from the MPM 280 and provides commands to the MPM 280 for possible IPMs, SPMs 264 and 274, and the power islands 260 and 270. Some of the commands may be to power on/off, change the power level, or change the frequency of the power islands 260 and 270. In some embodiments with a smart power unit (SPU) 290, the GPAL 214 and the PMCL 218 are responsible for communication with the SPU 290 to implement a power policy and collect information on the actual power supply. The SPU 290 is described in further detail below in FIGS. 6-8. In some embodiments, the GPAL 214 and the PMCL 218 provides sockets for existing power management techniques.

[00039] The power manager firmware 224 is firmware executed by the master power manager 280, the intermediate power manager, and the slave power managers 264 and 274.

[00040] The MPM 280 is any circuitry configured to control the "global" power behavior of the entire integrated circuit 250. In some embodiments, there are multiple MPMs 280 that control the power behavior of the entire integrated circuit 250. In some embodiments, the MPM 280 communicates with existing IPMs and SPMs 264 and 274 to control power within the power islands 260 and 270. The MPM 280 may receive status information about the power islands 260 and 270 from the SPMs 264 and 274 and the IPMs. The MPM 280 may also determine power trade-offs between the IPMs and the SPMs 264 and 274.

[00041] The MPM 280 may also provide a main interface to the PMCL 218 firmware. In some embodiments, the MPM 280 communicates with the PMCL 218 to accept commands (e.g.. memory mapped commands) and provide status information about the power within the integrated circuit 250. In some embodiments, the MPM 280 communicates with the PMCL 218 through the main bus for the integrated circuit 250. The MPM 280 may also register each of the SPMs 264 and 274 and IPMs and capabilities with the PMCL 218. Some operations of the MPM 280 are described in further detail below in FIGS. 5, 8, 9, and 11. In some embodiments, the MPM 280 reads and writes scan chains for state save and restore along with the local logic analyzer ability.

[00042] Some embodiments may include an IPM (not shown) that coordinates SPMs 264 and 274 on behalf of the MPM 280. In some embodiments, the IPM controls and coordinates power behavior on portions of the area controlled by the MPM 280. In some embodiments, the IPM controls the SPMs 264 and 274 that are on a separate chip from the MPM 280.

[00043] The SPM 264 is any circuitry configured to control power within a power island 264 in the integrated circuit 250. One example of the SPM 264 is an IP block that controls power within a power island 264 in the integrated circuit 250. The SPM 264 may include signal buffering, level

shifting, and signal isolation. In some embodiments, the SPM 264 is integrated into scan chains to provide easier implementation and integration. Also, in some embodiments, the SPM 264 has a very small "footprint" with a low gate count and low power. In some embodiments, the SPM 264 comprises a command interface to communicate status information, service requests, and commands. Some of the commands are load, sleep, and idle. The SPM 264 may also recognize its own address to allow for multi-drop bussing.

[00044] In some embodiments, the SPM 264 has registration capabilities. For registration at power-up, the SPM 264 uses callback registration that is typically used for off chip SPMs and IPMs. For static registration when the integrated circuit is generated for on chip SPMs, the SPM 264 registers what the SPM 264 can do, what the IPM can do, and the type of commands that the SPM 264 or IPM can service. The SPM 264 may also have save and restore functions for power off periods. The SPM 264 may have watch-dog timer(s). In some embodiments, the SPM 264 has a debug interface coordination to the power island 260. The SPM 264 may also monitor local state and collect information for components within the power island 260. The SPM 264 may also locally control Vdd, clocks for frequency selection, and dynamic back biasing. The description for the SPM 264 also applies to the SPM 274 for the power island 270.

[00045] In some embodiments, the SPM 264 checks whether an event occurs when the collected information from the power island 260 crosses a threshold or exceeds a range. In some embodiments, the SPM 264, IPMs, or the MPM 280 monitors power consumption levels of the power island 260 to check whether the power consumption levels cross a threshold level or exceed a range. A power consumption level is any information, data, or statistic that indicate the power consumed in a power island 260. Some examples of power consumption levels are temperature and power. The threshold or range may be programmable. The SPM 264 may report the event asynchronously, or another element such as the MPM 280 may solicit whether an event has

occurred. The event may also be a multi-level test such as the conditions occur at a greater than a given, programmable frequency or exceed a given, programmable duration.

[00046] In some embodiments, the low power standard cell logic block 262 one example of a standard cell library that may be included in the power island 260. In some embodiments, the standard cell library is optimized for lower power. The standard cell library may be characterized over a range of operating voltages. In some embodiments, the standard cell library includes synchronous circuits and/or asynchronous circuits. In some embodiments, the standard cell library includes static circuits and/or encapsulated, dynamic logic circuits. The standard cell library may also include multiple voltage domain interface circuits such as level shifters and signal isolation circuits. The standard cell library may also have a multi-threshold design and characterization such as standard Vt, high Vt, low Vt, and variable Vt circuits. The standard cell library may also include data retention (shadow) circuits and anti-glitch circuits. The standard cell library may also include low leakage "sleep" circuits. FIG. 3 depicts an illustration of low leakage circuitry 300 for the low power standard cell logic block 262 in an exemplary implementation of the invention.

[00047] FIG. 4 depicts a diagram of the power island 270 in an exemplary implementation of the invention. The power island 270 includes a low power memory block 272 and the SPM 274. The low power memory block 272 includes banked architectures 410, 420, 430, and 440 for memories and sleep, power down circuitry 450. In some embodiments, the memory in the power island 270 is RAM and/or ROM. Some examples of the RAM are the SRAM compilers such as single-port, 2-port, and dual-port. Some examples of the ROM are ROM compilers. Some memories in the power island 270 are optimized for low power such as the low power memory block 272. In one embodiment, the low power memory block 272 includes multiple bank architectures via the compiler such as banked architectures 410, 420, 430, and 440. The memories in the power island 270 may also include sleep, power down circuitry 450 for low power modes such as sleep, nap, and

full power down. The memories in the power island 270 may also include programmable read/write ports. The memories in the power island 270 may also be an asynchronous and/or synchronous design.

[00048] In some embodiments, the system 200 also includes a smart power unit (SPU) 290. In some embodiments, the SPU 290 is off-chip to the integrated circuit 250. The SPU 290 is an external unit configured to control power and clock distribution to the integrated circuit. The circuitry of the SPU is described in further detail below in FIGS. 7 and 8.

[00049] FIG. 5 depicts a flowchart from an application request to an SPM action in an exemplary implementation of the invention. FIG. 5 begins in step 500. In step 502, an application is invoked such as playing a movie. In step 504, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder. In some embodiments, when the IP unit is totally asynchronous, the required frequency will be an artificial measure of performance. In some embodiments that have multiple clocks involved, the minimum performance for each clock is specified.

[00050] In step 506, the application invokes the PMCL 218 API call. One example of this call is "Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag)." In this example, the other information could be "no power off, use high Vt and clocks off instead" and "major waits are about 10 us, with a 400 ns threshold." In some embodiments with multiple clocks, the PMCL 218 API call allows the application to specify all required frequencies.

[00051] The PMCL 218 determines possible trade-offs available for the unit and selects a frequency rate, Vdd, and Vt if applicable for the unit that best meets the given requirements in step 508 and determines the applicable SPMs 264 and 274 in step 510. In some embodiments, the MPM

280 or IPM performs steps 508 and 510. In some embodiments for multiple clocks, the Vdd and Vt specified would allow for all specified clocks to meet or exceed their required frequencies.

[00052] In step 512, the PMCL 218 then writes the desired setting for the SPMs 264 and 274 to the MPM 280 (or IPM). In step 514, the MPM 280 (or IPM) converts the request into one or more commands for the SPMs 264 and 274 (or IPM) associated with the unit.

[00053] In step 516, if the application sets the wait for power up flag, the PMCL 218 then waits until the IP unit is fully powered up before returning from the call. Otherwise, the call returns as soon as the command is acknowledged, with status of 0 for okay, 1 for fast power-up, 2 for slow power-up, or 3+ for error conditions. The powered up state is when the unit is at the desired Vdd for the requested frequency, and not just that the unit is turned on.

[00054] In step 518, the MPM 280 (or IPM) sends the requests to the appropriate targets. In step 520, the MPM 280 waits for the receipt of the acknowledgements that indicate message received and executed or execution has begun. A NACK or negative acknowledgement may also be returned from the SPM 264 and 274.

[00055] In step 522, the SPM 264 receives the commands and performs the actions. Steps 524-528 are possible actions that the SPM 264 may perform. In step 524, the SPM 264 switches the Vdd mux. In step 526, the SPM 264 switches a clock mux. In some embodiments when the voltage goes down, step 526 is performed before step 524. In step 528, the SPM 264 changes the Vt on the associated transistors. After the SPM 264 performs the actions, the SPM 264 returns a status message upstream indicating acknowledgement or negative acknowledgement in step 530. FIG. 5 ends in step 532.

[00056] FIG. 6 depicts an illustration of internal circuitry 600 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the internal circuitry 600 for the SPU 290 is internal to the integrated circuit 250 of FIG. 2. The internal circuitry 600 includes an

external voltage 610, a dropout voltage regulator 620, a dropout voltage regulator 630, a logic block 640, and a logic block 650.

[00057] FIG. 7 depicts an illustration of external circuitry 700 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the external circuitry 700 for the SPU 290 is external to the integrated circuit 250 of FIG. 2. The internal circuitry 700 includes an external voltage 710, a power supply pin 720, a power supply pin 730, a power supply pin 740, a logic block 750, a logic block 760, and a logic block 770. The external circuitry 700 for the SPU 290 provides a DC/DC conversion. The DC/DC conversion provides multiple independent power supply pins 720, 730, and 740. The power supply pins 720, 730, and 740 have a variable voltage supply on each separate power pin. Also, in some embodiments, the variable voltage is within a range and in steps. In some embodiments, the PMCL 218 controls the voltage to power supply pins 720, 730, and 740.

[00058] FIG. 8 depicts a flowchart from an application request to an SPU action in an exemplary implementation of the invention. FIG. 8 begins in step 800. In step 802, an application is invoked. In step 804, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder.

[00059] In step 806, the application invokes the PMCL 218 API call. One example of this call is "Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag)." In this example, the other information could be "no power off, use high Vt and clocks off instead" and "major waits are about 10 us, with a 400 ns threshold."

[00060] The PMCL 218 determines possible trade-offs available for the unit and selects a the lowest possible Vdd that will support the requested frequency in step 808 and determines the SPMs 264 and 274 that will be affected and which power PINs to change in step 810.

[00061] In step 812, the PMCL 218 sends a command to the MPM 280 to have the SPMs 264 and 274 (and IPM) to prepare for a Vdd change. In step 814, the PMCL 218 waits for the acknowledgement from the MPM 280. In step 816, the PMCL 218 sends a command to the SPU 290 to change the Vdd on the selected power pins and waits for the affected area to "settle down." In step 818, the PMCL 218 then sends a "resume operation at a specified frequency" command to the MPM 280. In step 820, the MPM 280 propagates the resume command to all affected SPMs 264 and 274 (and IPMs). In step 822, one of the power managers (i.e. MPM 280, IPM, or SPMs 264 and 274) sets the specified frequency. In step 824, the IP unit operation resumes after the clock has settled. FIG. 8 ends in step 826. In some embodiments, the user application has the option of waiting for the entire operation to finish or to continue and either query the PMCL 218 as to the progress of the operation or wait for a "finished" interrupt from the PMCL 218.

[00062] FIG. 9 depicts a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention. FIG. 9 begins in step 900. In step 902, the user application requests that the PMCL 218 power off an IP unit and wants to save the IP unit's state. In some embodiments, the reconfiguration of the IP unit takes a long time. The request in step 902 may be accompanied by the address of an area to which the state should be saved.

[00063] In step 904, the PMCL 218 sends a "stop clock and read IP unit state" message to the MPM 280. The MPM 280 then propagates the "stop clock and read IP unit state" message to the SPMs 264 and 274 of the affected unit in step 906. In step 908, the MPM 280 uses the scan chain for the IP unit to read the state into a register or buffer for presentation to the PMCL 218. In step

910, if the PMCL 218 provided the MPM 280 with the address of the save area, the MPM 280 saves the state information directly in the specified area. In step 912, after all of the IP units' state has been saved, the PMCL 218 sends a "power off IP unit" message to the MPM 280. In step 914, the MPM 280 then propagates out the "power off IP unit" message. In step 916, the PMCL 218 returns the save state area to the user application. The save state area contains the state of the unit.

[00064] At a later time, in step 918, the user application requests that the PMCL 218 power the IP unit back up and restore the state of the IP unit. In some embodiments, the user application request includes the address of the area to which the state was saved. In step 920, the PMCL 218 sends a "power up IP unit with clocks off and restore state" message to the MPM 280. In step 922, the MPM 280 propagates the "power up IP unit with clocks off and restore state" message to the SPMs 264 and 274 of the affected IP unit. In step 924, after the IP unit is powered up, the MPM 280 uses the scan chain to reload the unit's state. In some embodiments, the reloading of the unit's state originates directly from the save area or from information passed to the MPM 280 from the PMCL 218. In step 926, the PMCL 218 sends a message to the MPM 280 to turn clock back on and report to user application that the IP unit is ready to continue operations. FIG. 9 ends in step 928.

[00065] In some embodiments, the same functionality of FIG. 9 can be used to implement an internal "logic analyzer" function, in which the IP unit in question would not be powered down after being read. If the associated SPMs 264 and 274 of the IP unit have the ability to single- or multi-step the clock, the local scan testing is performed by having the SPMs 264 and 274 "signal isolate" the IP unit. Then, use of a combination of the ability of single- or multi-step the clock and the ability to use the scan chain can read/write the IP unit's internal state.

[00066] FIG. 10 depicts a diagram of a system-on-a-chip (SOC) 1000 and an extended local memory 1004 in an exemplary implementation of the invention. The SOC 1000 is one example of the integrated circuit 250 and communicates with the embedded firmware stack 210 in FIG. 2 as

described above. The SOC 1000 includes a CPU 1010, a local memory 1020, a memory controller 1030, a mixed signal circuitry 1040, an application specific circuitry 1050, a PCI-X circuitry 1060, a MPM 1070, a real-time clock (RTC) 1075, an Ethernet circuitry 1080, and a USB circuitry 1090. The CPU 1010, the local memory 1020, the memory controller 1030, the mixed signal circuitry 1040, the application specific circuitry 1050, the PCI-X circuitry 1060, the Ethernet circuitry 1080, and the USB circuitry 1090 are all power islands in which power is controlled within the power islands by power managers. In this embodiment, the power islands are delineated by the functionality of a part of the SOC 1000.

[00067] The extended local memory 1004 includes an IPM 1006 that is coupled to the bus 1071. The CPU 1010 includes an SPM 1015 that is coupled to the bus 1071. The local memory 1020 includes an SPM 1025 that is also coupled to the bus 1071. The memory controller 1030 comprises an SPM 1035 that is coupled to the bus 1071. The mixed signal circuitry 1040 includes an SPM 1045 that is coupled to the bus 1071. The application specific circuitry 1050 includes an IPM 1055 and an SPM 1058 that are both coupled to the bus 1072. The PCI-X circuitry 1060 includes an SPM 1065 that is coupled to the bus 1072. The MPM 1070 is coupled to the bus 1071 and the bus 1072. The MPM 1070 is one example of the MPM 280 as described above. The Ethernet circuitry 1080 includes an SPM 1085 that is coupled to the bus 1072. The USB circuitry 1090 includes an SPM 1095 that is coupled to the bus 1072.

[00068] In this embodiment, power command buses comprise the bus 1071 and the bus 1072. The bus 1071 and 1072 are simple multi-drop serial buses that may cross chip boundaries and interconnect power managers. The power command bus may be a combination of serial busses, such as the bus 1071 and the bus 1072, with one per region of the chip and then multi-drop within the region. In other embodiments, the power command bus includes a parallel bus or a combination of serial and parallel busses. In some embodiments, the power command bus is the system bus. The

power command bus may contain messages with at least a unit ID with the associated payload. For a fixed point to point bus, the message does not need a unit ID only the payload.

[00069] In some embodiments, the power command bus uses an error detection scheme such as parity, ECC, or a redundant code. In some embodiments, the power command bus is a low performance bus that does not interfere with the integrated circuit design and is not visible to the user. In some embodiments, the communication between the PMCL 218 and the MPM 1070 is memory mapped and based on the main bus such as an AHB for an SOC 1000.

[00070] Some embodiments may include a separate bus for reporting status information between the power managers. In one example, this separate bus provides asynchronous "Alert" type status messages from SPMs to the MPM.

[00071] There can be various message formats for the power command bus. In one example for a basic format, the message format includes a start of message indicator, a power manager address, type code, basic command, and an end of message indicator. In one example for an extended format, the message format includes the basic format, an additional length, and additional information. In one example for a response message format, the message format includes a start of message reply indictor, a power manager address, a 3b ACK or NAK or return status (implied ACK), a payload length for return status messages, a payload for return status messages, a reason code for NAK, and an end of message indicator.

[00072] In some embodiments, the SPM 1015 or the IPM 1006 times out on replying to a command, and the MPM 1070 reissues the command a programmable number of times. If the SPM 1015 or the IPM 1006 still fails, the MPM 1070 marks the SPM 1015 or the IPM 1006 as unusable and reports back the failure to the PMCL 218. In one embodiment, the PMCL 218 has the MPM 1070 reinitialize the failing SPM 1015 or the IPM 1006 via the scan system and then retries sending the message. Other conditions such as invalid responses to commands or invalid status reports are

also handled by the re-initialization. In some embodiments, the state of the failing SPM 1015 or the IPM 1006 may be read out and saved for later analysis.

[00073] FIG. 11 depicts a flowchart for generating a "hot spot" report from an IPM 1055 to the PMCL 218 in an exemplary implementation of the invention. FIG. 11 begins in step 1100. In step 1102, the IPM 1055 monitors the temperature statistics of the SPMs. In step 1104, the IPM 1055 checks whether the mean temperature has exceeded a predetermined and programmed threshold. If the mean temperature has not exceeded the threshold, the IPM 1055 returns to step 1102 to keep monitoring. If the mean temperature has exceeded the threshold, the IPM 1055 then generates a problem ("hot spot") report message in step 1106. In step 1108, the IPM 1055 waits for the next status query the MPM 1070. In some embodiments, a logically separate bus is provided for asynchronous status reports to the MPM 280.

[00074] In step 1110, the MPM 1070 receives the hot spot report message. In step 1112, the MPM 1070 either waits for further confirmation (i.e. see that the "hot spot" last pasts a predetermined threshold) or immediately takes action to fix the problem depending on the internal logic of the MPM 1070. In some embodiments, in step 1114, the MPM 1070 takes action by posting an interrupt to the PMCL 280 that it needs attention. In other embodiments, if the PMCL 280 queries the MPM 1070 often enough, then the interrupt is not needed. In step 1116, the MPM 1070 (or IPM) fixes the problem by making a local trade-off, performing the action, or ordering the action to be performed. One example of fixing the problem is lowering the operating frequency of the hot spot area. In step 1118, the MPM 1070 reports both the problem and the fixing of the problem upstream.

[00075] In step 1120, the PMCL 218 reads the modified hot spot report from the MPM 1070. In step 1122, the PMCL 218 determines what action to take to fix the problem or notify the GPAL 214 of the problem. In step 1124, the PMCL 218 issues the appropriate commands to the MPM

1070 to fix the problem. In this step, the software will make the trade-off required to fix the problem. In some embodiments, if the GPAL 214 determines the high level fix, then the GPAL 214 sends it to the PMCL 280 to be converted into MPM commands. In step 1126, the PMCL 218 monitors the problem area for a specified time to check if the problem is fixed. FIG. 11 ends in step 1128.

[00076] In some embodiments, the type of functionality in FIG. 11 can be performed at other levels such as the PMCL 218. In one example, the PMCL 218 queries (via the MPM 1070) all the SPMs that have the desired measurement ability (and IPMs) as to their local conditions and can then, for example, build a "map" of power usage that it can then act on.

[00077] FIG. 12 depicts a diagram of a system-on-a-chip (SOC) 1200 in another exemplary implementation of the invention. The SOC 1200 is attached to a sensor link 1212, an RF link 1214, a control link 1216, a video link 1294, an audio link 1295, an interface link 1296, a control link 1297, and a power link 1298. The SOC 1200 includes clock and distribution management 1210, an IP block power island 1220, a memory power island 1230, a microprocessor power island 1240, an IP block power island 1250, a distribution power island 1260, an IP block power island 1270, an IP block power island 1280, and power and distribution management 1290.

[00078] The IP block power island 1220 includes a product standard interface IP block including an analog-to-digital converter (ADC) 1222, which includes an SPM 1224. The IP block power island 1230 includes a memory 1232, which includes an SPM 1234. The microprocessor power island 1240 includes a microprocessor 1242, which includes an SPM 1244. The IP block power island 1250 includes a product standard interface IP block including ADC 1252, which includes an SPM 1254. The distribution power island 1260 includes a data and signal distribution 1262, which includes an SPM 1264. The IP block power island 1270 includes a general purpose IP block including a digital signal processor (DSP) 1272, which includes an SPM 1274. The IP block

power island 1280 includes a product-specific IP block 1282, which includes an SPM 1284. The power and distribution management 1290 includes an MPM 1292.

[00079] FIG. 13 depicts a flowchart for building a chip with power islands in an exemplary implementation of the invention. FIG. 13 begins in step 1300. In step 1302, the IPs or library cells are selected, and the custom logic, if any, is specified to be used to build the chip. In some embodiments, the maximum and sub clock rate, % idle time, and minimum and maximum Vdd are specified. In step 1304, the register transfer level (RTL) is written. In step 1306, the RTL is simulated and debugged.

[00080] Either during or after the writing of the RTL, a software tool may be used to add annotations for the MPM, IPM, and/or SPM blocks in step 1308. In some embodiments, the desired functionality options are specified in the annotations. In some embodiments, the optional functionality is specified per SPM block. In some embodiments, the RTL is annotated with SPM configuration information on a per-module basis. In some embodiments, the proper annotation is inserted by hand on a per module basis during or after the RTL is written. In other embodiments, a separate table in the proper format is created with the module names and respective annotations. In some embodiments, a separate software tool provides the ability to interactively build the separate table. In some embodiments, the software tool adds the proper annotation to the un-annotated modules in the RTL using information from the table.

[00081] In step 1310, the synthesis is run on a power island basis, where power islands are not mixed. In step 1312, performance measurement software is run on each module for each Vdd and Vt option, and then the annotations for the MPM are added to the RTL. In some embodiments, the performance of the design is measured at all desired voltages and Vt combinations. The software tool then derives the actual frequency, Vdd, and Vt tables for each SPM and back annotates the MPM (or IPM) RTL of the SPM characteristics.

[00082] In step 1314, the final synthesis is run on a power island basis. In some embodiments, the modules are separately routed or by SPM. In step 1316, the software tool is run to hook up power and clocks to each SPM. Step 1318 is the rest of the steps to tape-out. In some embodiments, the software tool generates the finished net-list with all information. FIG. 13 ends in step 1320.

[00083] The above-described elements can be comprised of instructions that are stored on storage media. The instructions can be retrieved and executed by a processor. Some examples of instructions are software, program code, and firmware. Some examples of storage media are memory devices, tape, disks, integrated circuits, and servers. The instructions are operational when executed by the processor to direct the processor to operate in accord with the invention. Those skilled in the art are familiar with instructions, processor, and storage media.

[00084] The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

CLAIMS

What is claimed is:

1. A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:

determining a target power level for one of the power islands where power consumption is independently controlled within each of the power islands;

determining an action to change a consumption power level of the one of the power islands to the target power level; and

performing the action to change the consumption power level of the one of the power islands to the target power level.

2. The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit.

3. The method of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

4. The method of claim1 wherein the power islands comprise power sub-islands.

5. The method of claim 1 wherein the power islands comprises multiple clock domains.

6. The method of claim 1 wherein the action comprises selecting a clock frequency for one of the power islands.

7. The method of claim 1 wherein the action comprises selecting a clock for one of the power islands.

8. The method of claim 1 wherein the action comprises modifying a first voltage for one of the power islands.

9. The method of claim 8 wherein the first voltage comprises a source voltage.

10. The method of claim 8 wherein the first voltage comprises a threshold voltage.

11. The method of claim 1 wherein the action comprises powering on one of the power islands.

12. The method of claim 1 wherein the action comprises powering off one of the power islands.

13. The method of claim 1 wherein the action comprises changing one of the power islands to a sleep mode.

14. The method of claim 1 further comprising:

monitoring the power consumption level of one of the power islands;

determining whether a threshold level was crossed based on the power consumption level; and

performing the action based on the crossing of the threshold level.

15. The method of claim 1 further comprising saving a state of components within one of the power islands.

16. The method of claim 1 further comprising restoring a state of components within one of the power islands.

17. A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:

power control circuitry configured to control power for one of the power islands; and

a power manager configured to determine a target power level for one of the power islands, determine an action to change a consumption power level of the one of the power islands to the target power level, and perform the action to change the consumption power level of the one of the power islands to the target power level.

18. The system of claim 17 wherein the power islands are delineated based on geographic factors of the integrated circuit.

19. The system of claim 17 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

20. The system of claim 17 wherein the power islands comprise power sub-islands.

21. The system of claim 17 wherein the power islands comprise multiple clock domains.

22. The system of claim 17 wherein the action comprises selecting a clock frequency for one of the power islands.

23. The system of claim 17 wherein the action comprises selecting a clock for one of the power islands.

24. The system of claim 17 wherein the action comprises modifying a first voltage for one of the power islands.

25. The system of claim 24 wherein the first voltage comprises a source voltage.

26. The system of claim 24 wherein the first voltage comprises a threshold voltage.

27. The system of claim 17 wherein the action comprises powering on one of the power islands.

28. The system of claim 17 wherein the action comprises powering off one of the power islands.

29. The system of claim 17 wherein the action comprises changing one of the power islands to a sleep mode.

30. The system of claim 17 wherein the power manager is configured to monitor the power consumption level of one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the action based on the crossing of the threshold level.

31. The system of claim 17 wherein the power manager is configured to save a state of components within one of the power islands.

32. The system of claim 17 wherein the power manager is configured to restore a state of components within one of the power islands.

33. The system of claim 17 further comprising a bus coupled to the power manager and the power islands.

34. The system of claim 17 wherein the power manager comprises a master manager configured to control power of the integrated circuit.

35. The system of claim 17 wherein the power manager comprises a slave manager configured to control power of one of the power islands.

36. The system of claim 17 wherein the power control circuitry includes clock multiplexing circuitry.

37. The system of claim 17 wherein the power control circuitry includes voltage multiplexing circuitry.

38. The system of claim 17 wherein the power control circuitry includes level shifting circuitry.

39. A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising:

power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands where power consumption is independently controlled within each of the power islands, determine an action to change a consumption power level of the one of the power islands to the target power level, and perform the action to change the consumption power level of the one of the power islands to the target power level; and

a software storage medium operational to store the power management software.

40. The software product of claim 39 wherein the power islands are delineated based on geographic factors of the integrated circuit.

41. The software product of claim 39 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

42. The software product of claim 39 wherein the power islands comprise power sub-islands.

43. The software product of claim 39 wherein the power islands comprise multiple clock domains.

44. The software product of claim 39 wherein the action comprises selecting a clock frequency for one of the power islands.

45. The software product of claim 39 wherein the action comprises selecting a clock for one of the power islands.

46. The software product of claim 39 wherein the action comprises modifying a first voltage for one of the power islands.

47. The software product of claim 46 wherein the first voltage comprises a source voltage.

48. The software product of claim 46 wherein the first voltage comprises a threshold voltage.

49. The software product of claim 39 wherein the action comprises powering on one of the power islands.

50. The software product of claim 39 wherein the action comprises powering off one of the power islands.

51. The software product of claim 39 wherein the action comprises changing one of the power islands to a sleep mode.

52. The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the action based on the crossing of the threshold level.

53. The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within one of the power islands.

54. The software product of claim 39 wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within one of the power islands.

ABSTRACT OF THE DISCLOSURE

[00085] Systems and methods manage power in an integrated circuit using power islands. The integrated circuit includes a plurality of power islands where power consumption is independently controlled within each of the power islands. A power manager determines a target power level for one of the power islands. The power manager then determines an action to change a consumption power level of the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level.

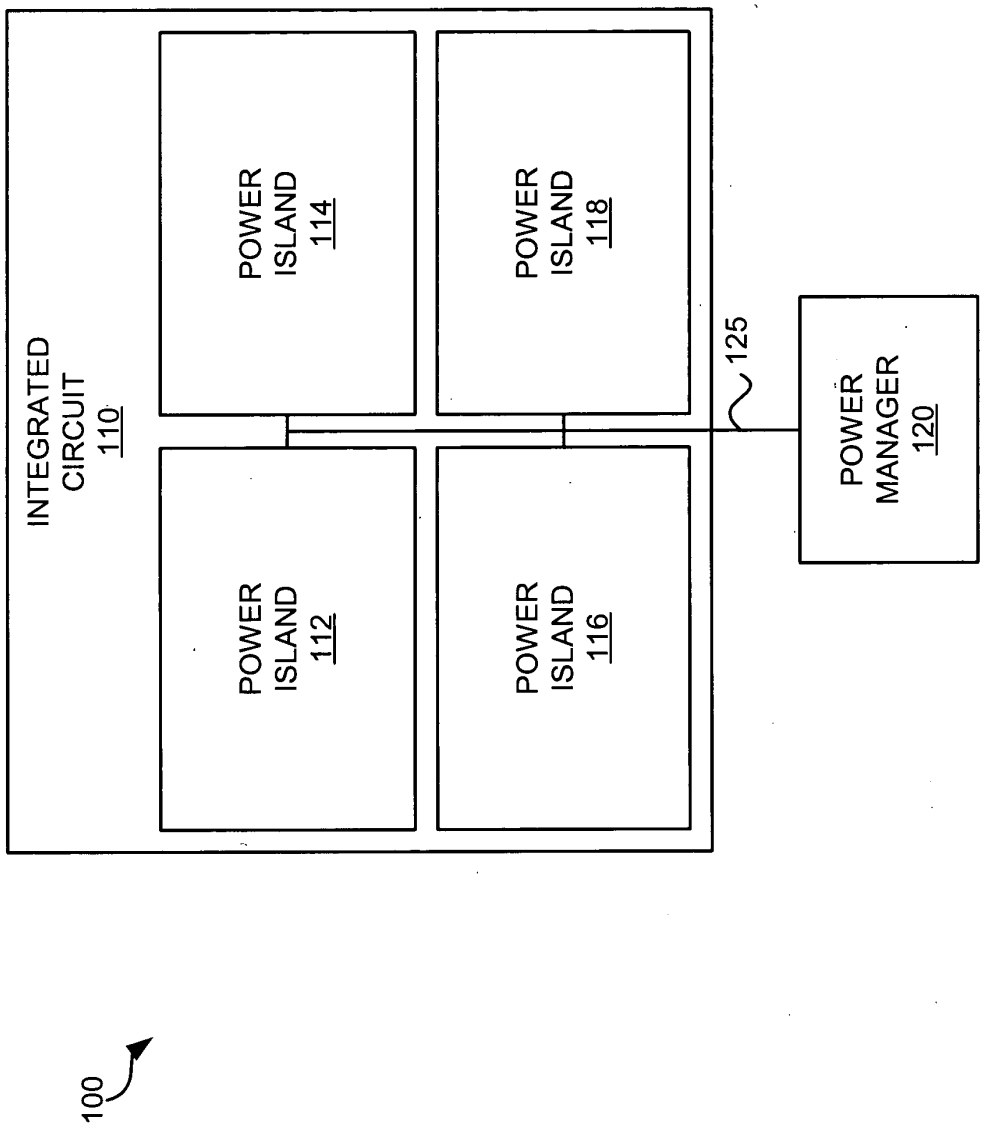
INTEGRATED CIRCUIT 110
POWER ISLAND 112
POWER ISLAND 114
POWER ISLAND 116
POWER ISLAND 118
125
POWER MANAGER 120
100

FIG. 1

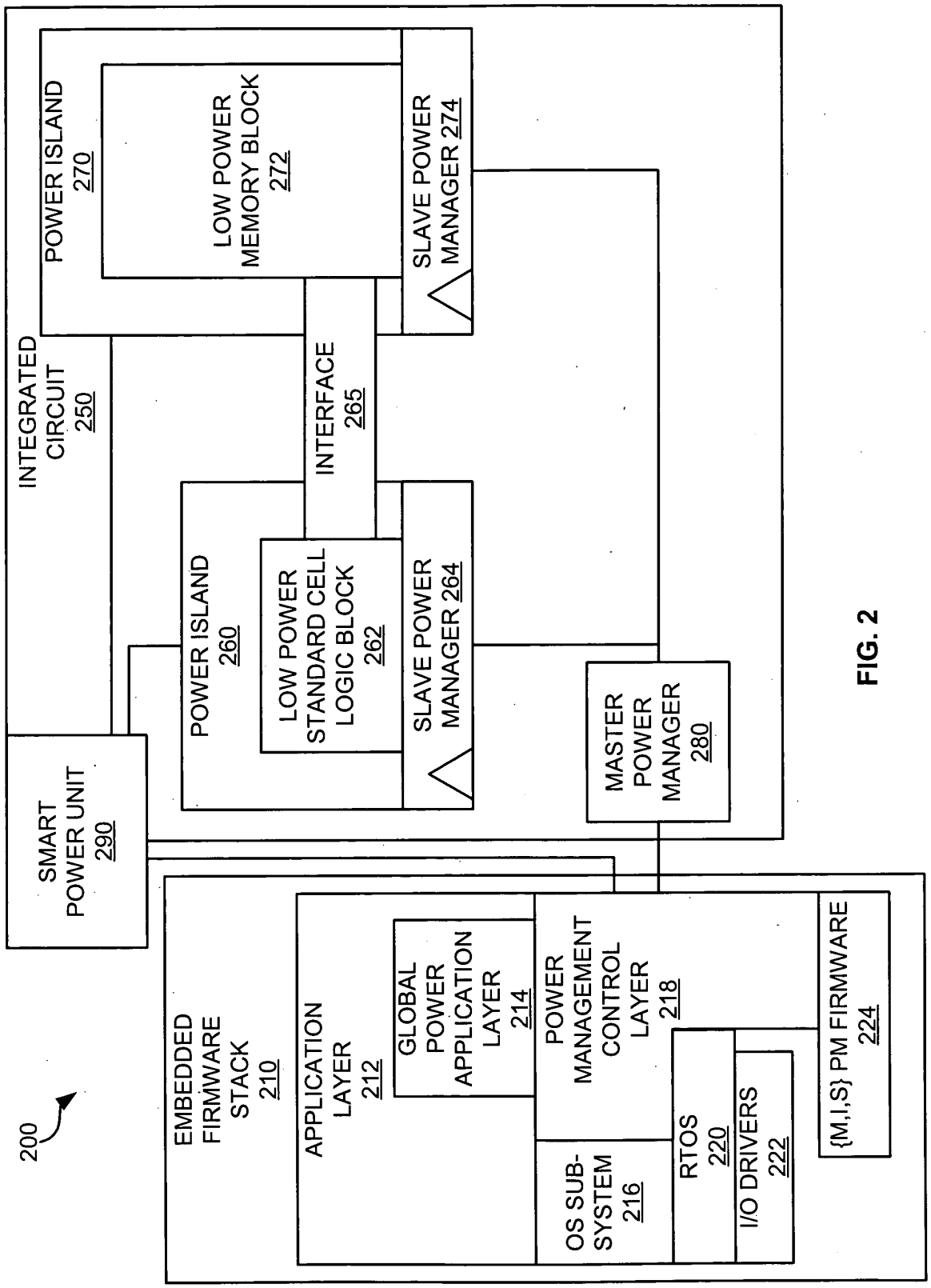
200
INTEGRATED CIRCUIT 250
POWER ISLAND 270
LOW POWER MEMORY BLOCK 272
SLAVE POWER MANAGER 274
INTERFACE 265
POWER ISLAND 260
LOW POWER STANDARD CELL LOGIC BLOCK 262
SLAVE POWER MANAGER 264
MASTER POWER MANAGER 280
SMART POWER UNIT 290
EMBEDDED FIRMWARE STACK 210
APPLICATION LAYER 212
GLOBAL POWER APPLICATION LAYER 214
POWER MANAGEMENT CONTROL LAYER 218
OS SUB-SYSTEM 216
RTOS 220
I/O DRIVERS 222
{M,I,S} PM FIRMWARE 224

FIG. 2

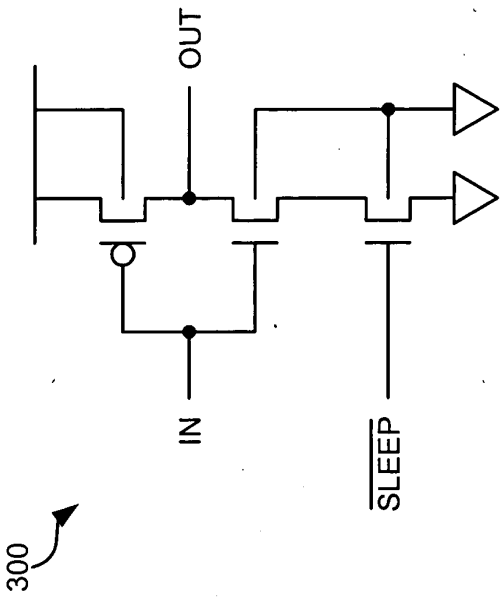

FIG. 3

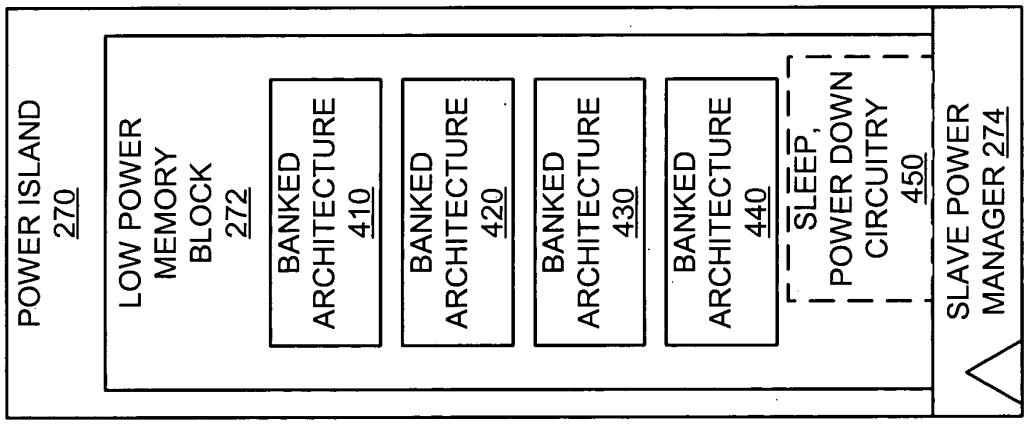
POWER ISLAND 270
LOW POWER MEMORY BLOCK 272
BANKED ARCHITECTURE 410
BANKED ARCHITECTURE 420
BANKED ARCHITECTURE 430
BANKED ARCHITECTURE 440
SLEEP, POWER DOWN CIRCUITRY 450
SLAVE POWER MANAGER 274

FIG. 4

Title: Managing Power on Integrated Circuits Using Power Islands
Inventor: Barry A. Hoberman et. al.
Attorney Docket No.: PA2258US

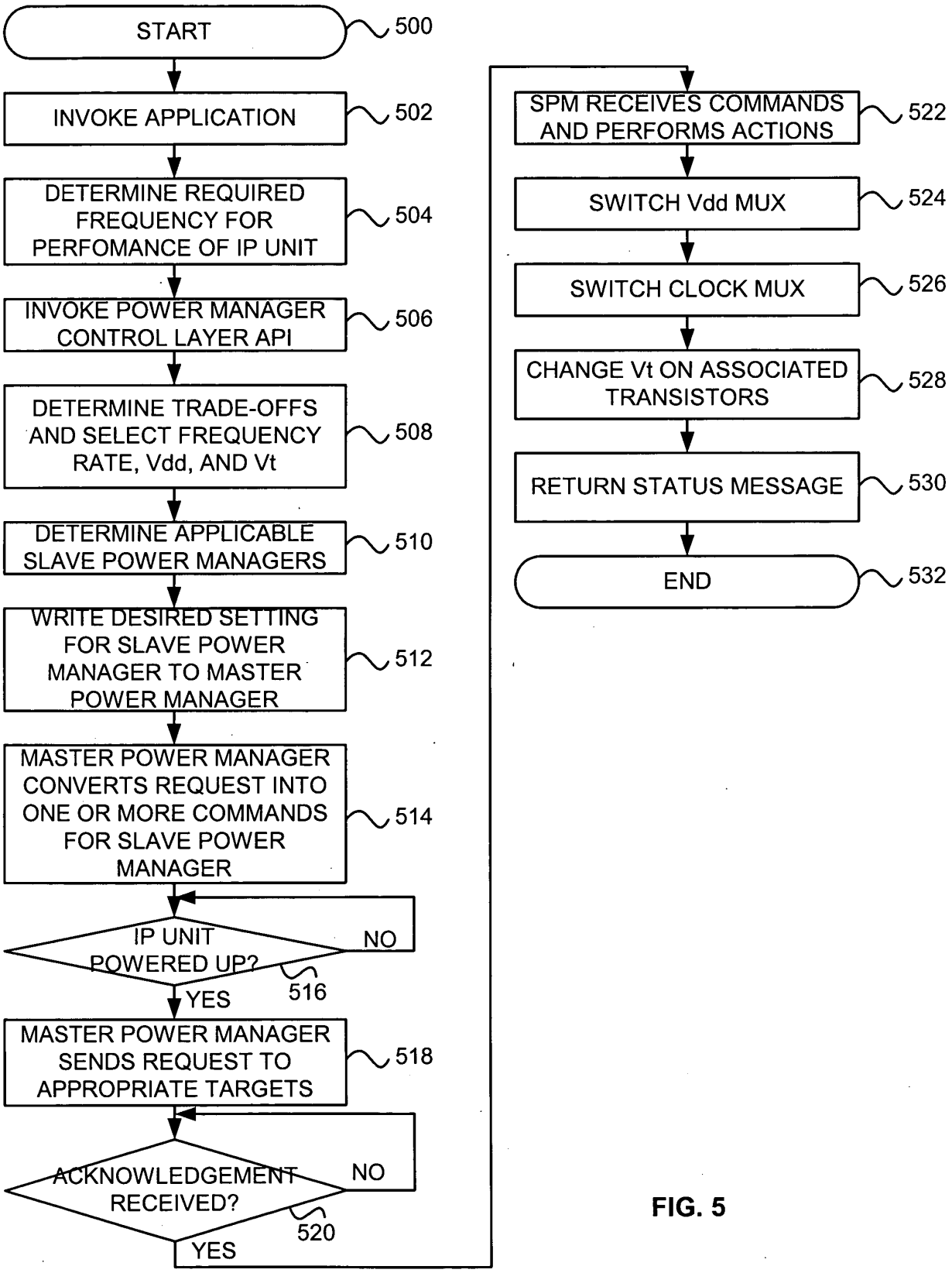

FIG. 5

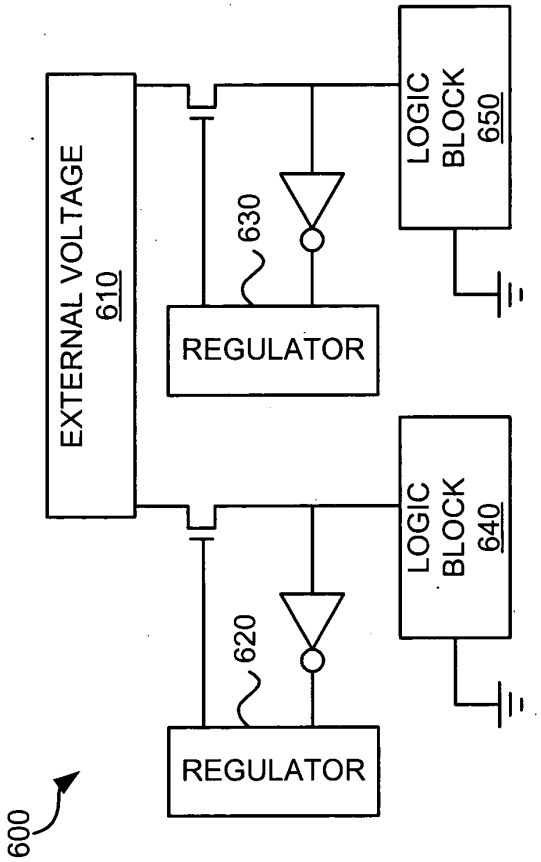
600
EXTERNAL VOLTAGE
610
REGULATOR
620
REGULATOR
630
LOGIC
BLOCK
640
LOGIC
BLOCK
650

FIG. 6

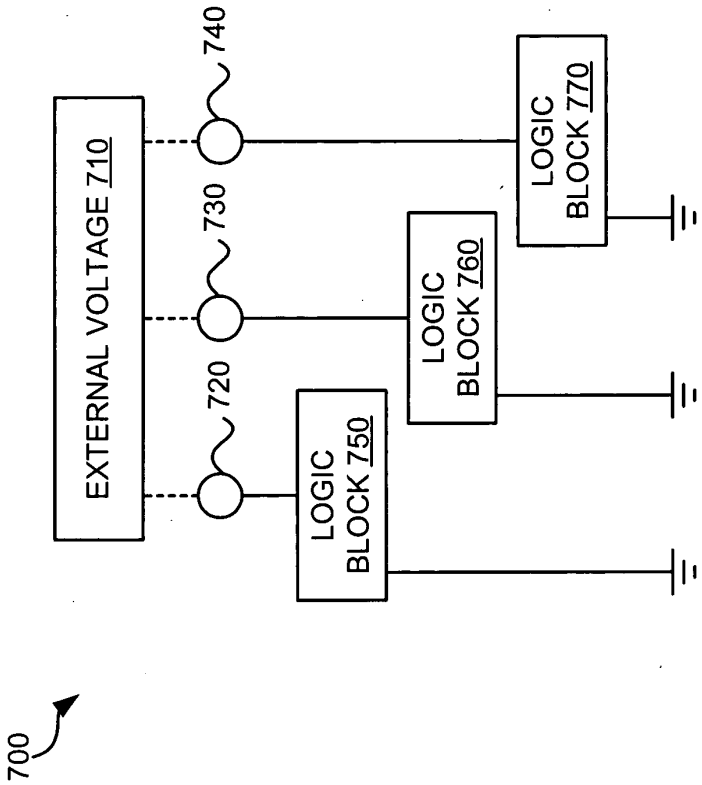
700
EXTERNAL VOLTAGE 710
720
730
740
LOGIC BLOCK 750
LOGIC BLOCK 760
LOGIC BLOCK 770

FIG. 7

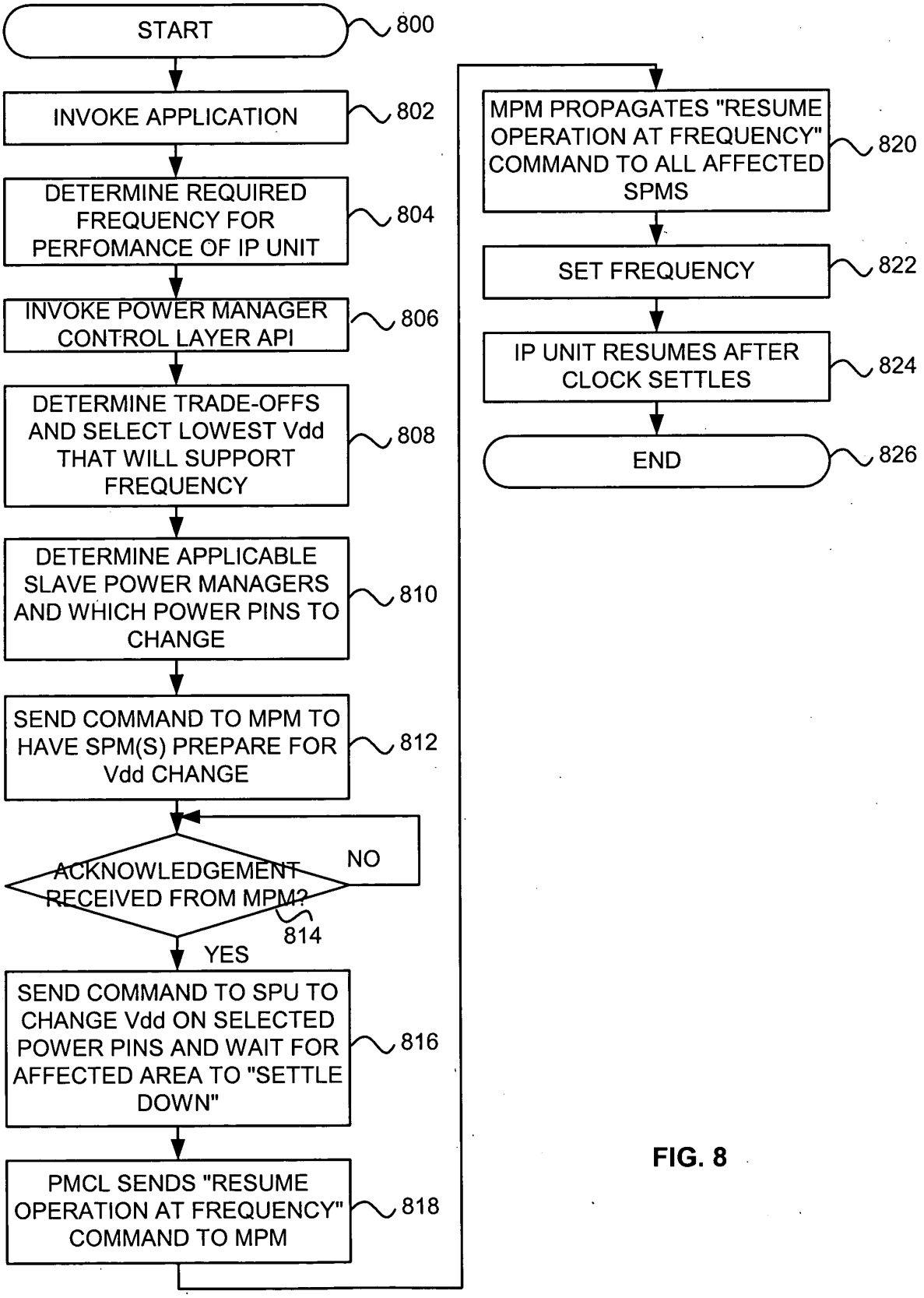
START
800
INVOKE APPLICATION
802
DETERMINE REQUIRED FREQUENCY FOR PERFOMANCE OF IP UNIT
804
INVOKE POWER MANAGER CONTROL LAYER API
806
DETERMINE TRADE-OFFS AND SELECT LOWEST Vdd THAT WILL SUPPORT FREQUENCY
808
DETERMINE APPLICABLE SLAVE POWER MANAGERS AND WHICH POWER PINS TO CHANGE
810
SEND COMMAND TO MPM TO HAVE SPM(S) PREPARE FOR Vdd CHANGE
812
ACKNOWLEDGEMENT RECEIVED FROM MPM?
814
NO
YES
SEND COMMAND TO SPU TO CHANGE Vdd ON SELECTED POWER PINS AND WAIT FOR AFFECTED AREA TO "SETTLE DOWN"
816
PMCL SENDS "RESUME OPERATION AT FREQUENCY" COMMAND TO MPM
818
MPM PROPAGATES "RESUME OPERATION AT FREQUENCY" COMMAND TO ALL AFFECTED SPMS
820
SET FREQUENCY
822
IP UNIT RESUMES AFTER CLOCK SETTLES
824
END
826

FIG. 8

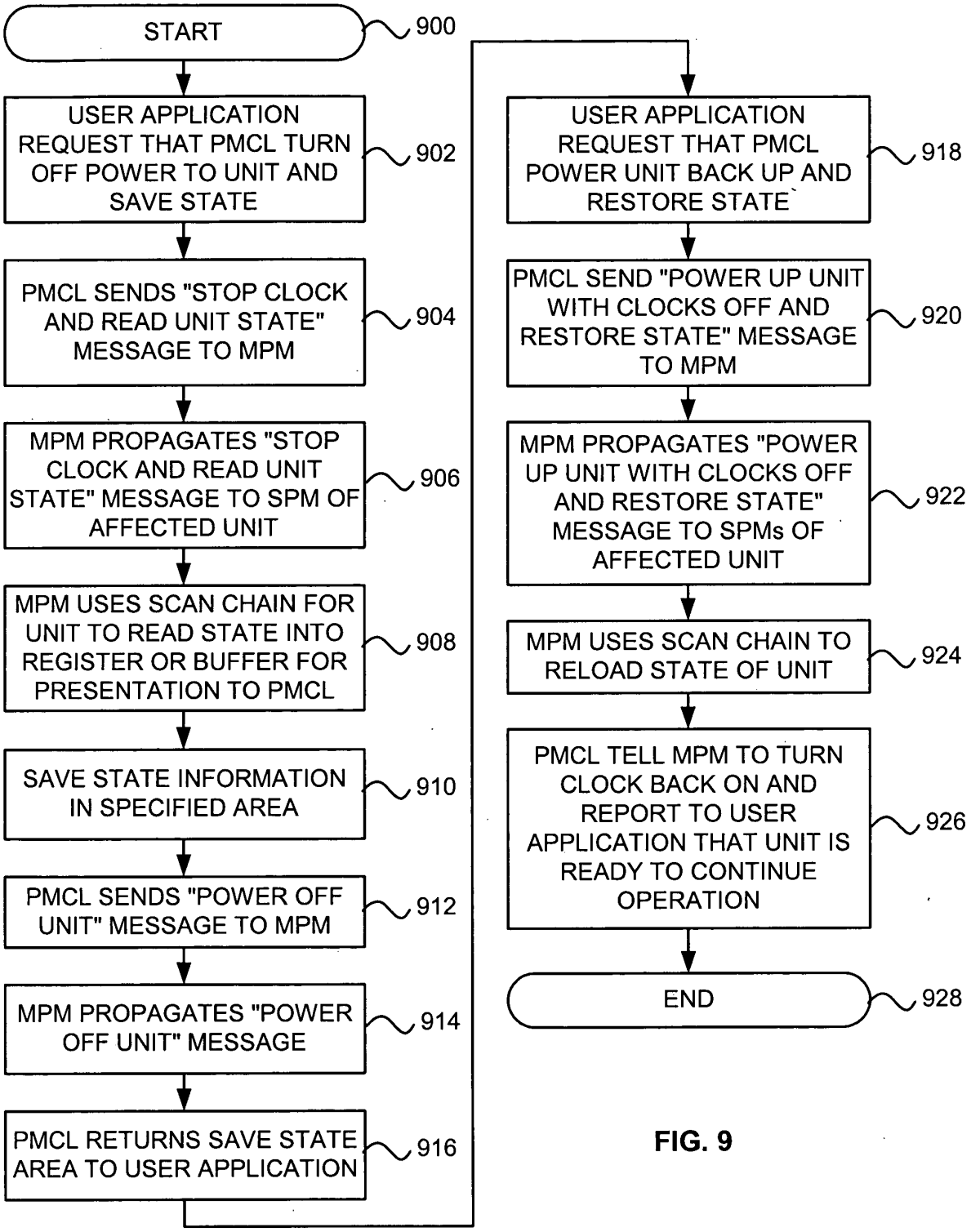
START
900
USER APPLICATION REQUEST THAT PMCL TURN OFF POWER TO UNIT AND SAVE STATE
902
PMCL SENDS "STOP CLOCK AND READ UNIT STATE" MESSAGE TO MPM
904
MPM PROPAGATES "STOP CLOCK AND READ UNIT STATE" MESSAGE TO SPM OF AFFECTED UNIT
906
MPM USES SCAN CHAIN FOR UNIT TO READ STATE INTO REGISTER OR BUFFER FOR PRESENTATION TO PMCL
908
SAVE STATE INFORMATION IN SPECIFIED AREA
910
PMCL SENDS "POWER OFF UNIT" MESSAGE TO MPM
912
MPM PROPAGATES "POWER OFF UNIT" MESSAGE
914
PMCL RETURNS SAVE STATE AREA TO USER APPLICATION
916
USER APPLICATION REQUEST THAT PMCL POWER UNIT BACK UP AND RESTORE STATE
918
PMCL SEND "POWER UP UNIT WITH CLOCKS OFF AND RESTORE STATE" MESSAGE TO MPM
920
MPM PROPAGATES "POWER UP UNIT WITH CLOCKS OFF AND RESTORE STATE" MESSAGE TO SPMs OF AFFECTED UNIT
922
MPM USES SCAN CHAIN TO RELOAD STATE OF UNIT
924
PMCL TELL MPM TO TURN CLOCK BACK ON AND REPORT TO USER APPLICATION THAT UNIT IS READY TO CONTINUE OPERATION
926
END
928

FIG. 9

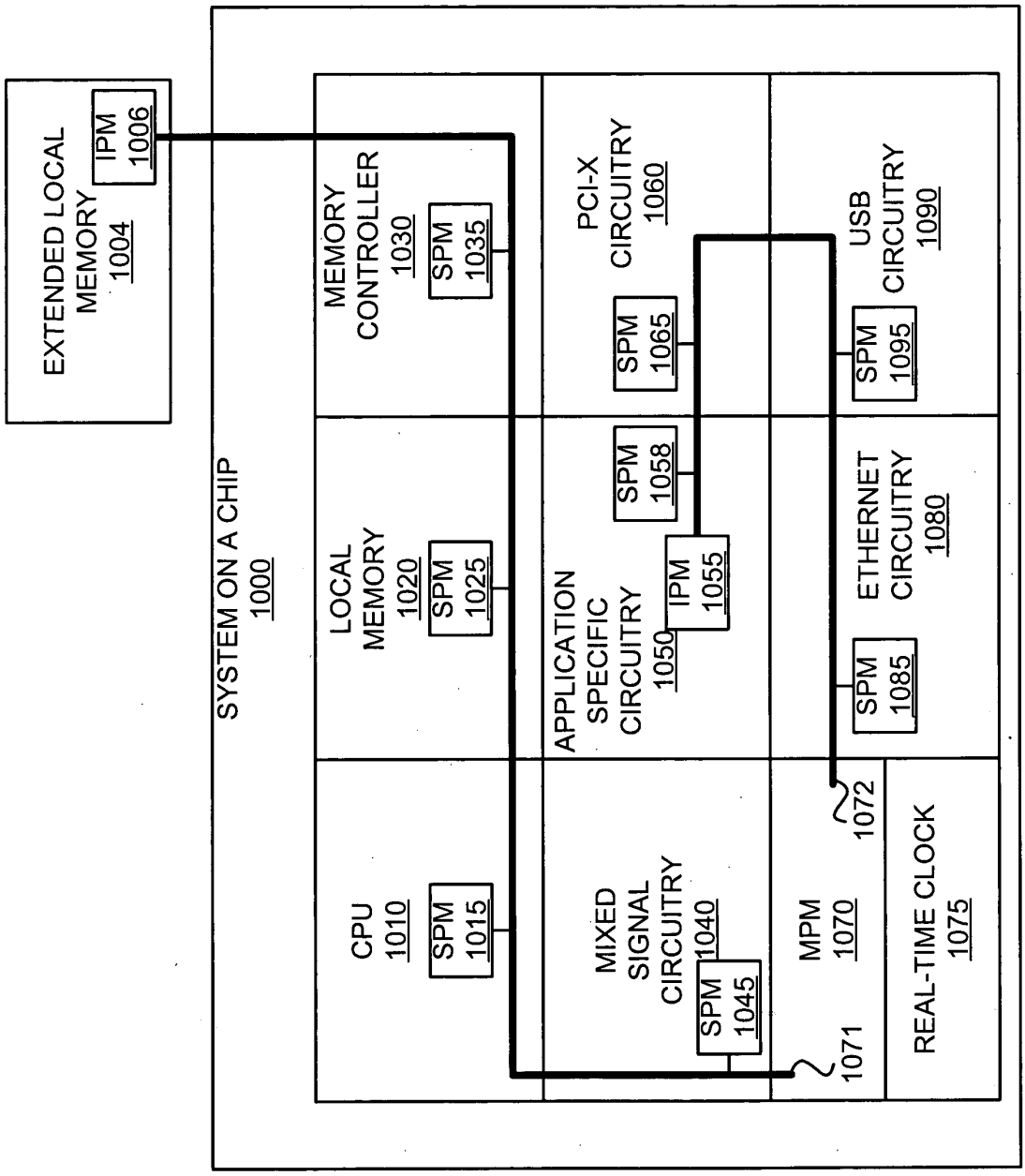
EXTENDED LOCAL MEMORY 1004
IPM 1006
SYSTEM ON A CHIP 1000
CPU 1010
SPM 1015
LOCAL MEMORY 1020
SPM 1025
MEMORY CONTROLLER 1030
SPM 1035
MIXED SIGNAL CIRCUITRY 1040
SPM 1045
APPLICATION SPECIFIC CIRCUITRY 1050
IPM 1055
SPM 1058
PCI-X CIRCUITRY 1060
SPM 1065
MPM 1070
1071
1072
ETHERNET CIRCUITRY 1080
SPM 1085
USB CIRCUITRY 1090
SPM 1095
REAL-TIME CLOCK 1075

FIG. 10

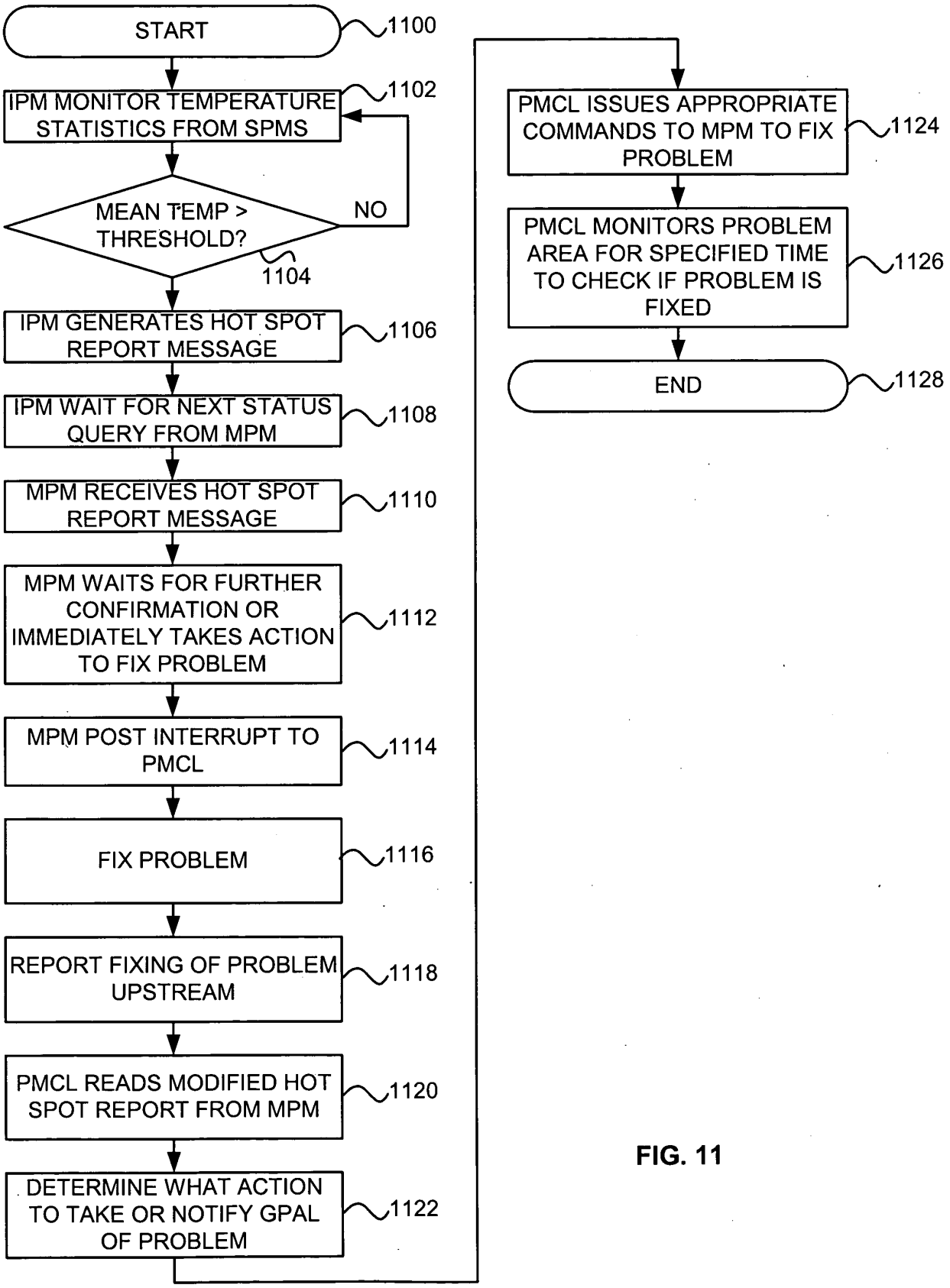
START
1100
IPM MONITOR TEMPERATURE STATISTICS FROM SPMS
1102
MEAN TEMP > THRESHOLD?
NO
1104
IPM GENERATES HOT SPOT REPORT MESSAGE
1106
IPM WAIT FOR NEXT STATUS QUERY FROM MPM
1108
MPM RECEIVES HOT SPOT REPORT MESSAGE
1110
MPM WAITS FOR FURTHER CONFIRMATION OR IMMEDIATELY TAKES ACTION TO FIX PROBLEM
1112
MPM POST INTERRUPT TO PMCL
1114
FIX PROBLEM
1116
REPORT FIXING OF PROBLEM UPSTREAM
1118
PMCL READS MODIFIED HOT SPOT REPORT FROM MPM
1120
DETERMINE WHAT ACTION TO TAKE OR NOTIFY GPAL OF PROBLEM
1122
PMCL ISSUES APPROPRIATE COMMANDS TO MPM TO FIX PROBLEM
1124
PMCL MONITORS PROBLEM AREA FOR SPECIFIED TIME TO CHECK IF PROBLEM IS FIXED
1126
END
1128

FIG. 11

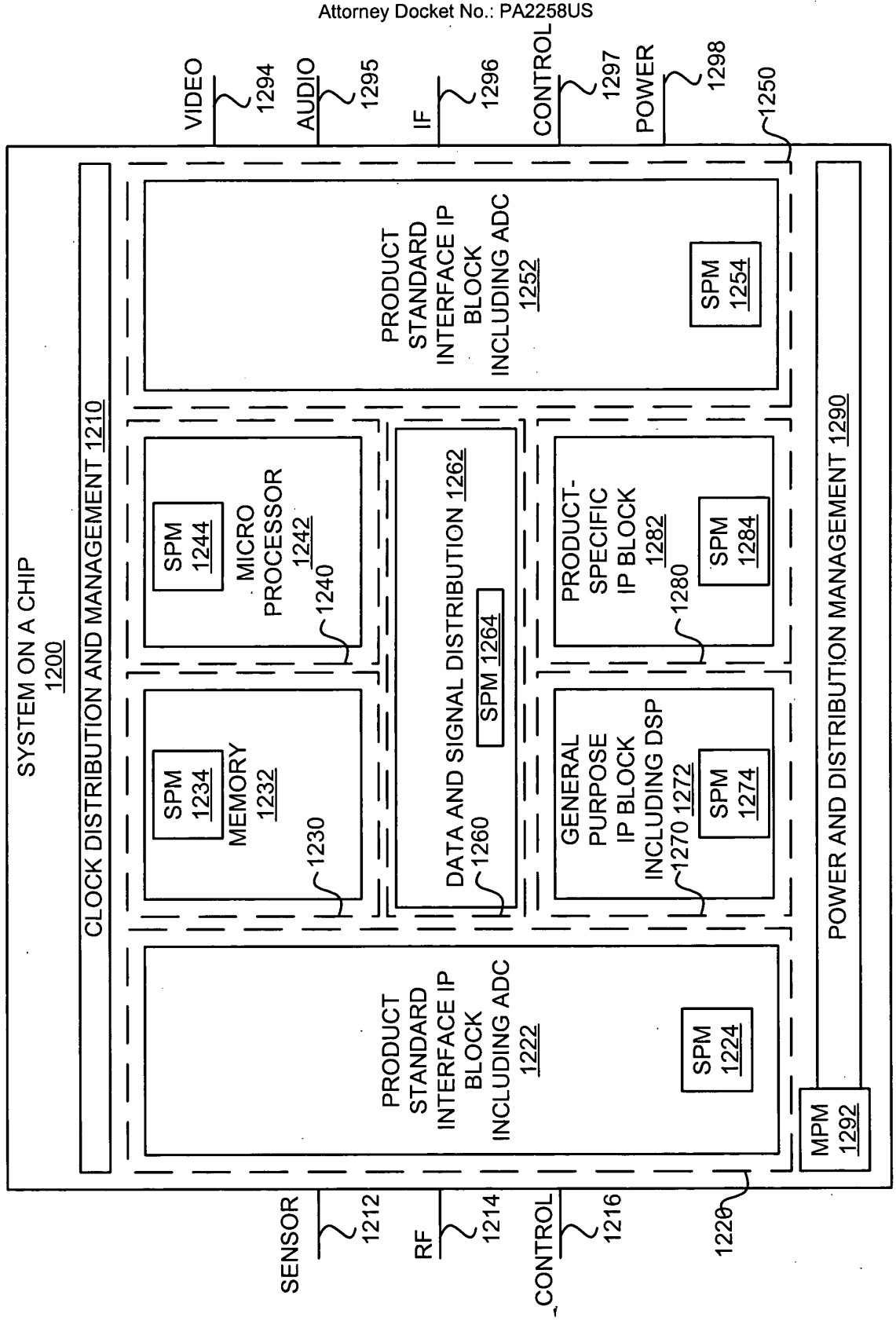
SYSTEM ON A CHIP
1200
CLOCK DISTRIBUTION AND MANAGEMENT 1210
VIDEO
1294
AUDIO
1295
IF
1296
CONTROL
1297
POWER
1298
1250
PRODUCT STANDARD INTERFACE IP BLOCK INCLUDING ADC
1252
SPM
1254
SPM
1244
MICRO PROCESSOR
1242
1240
DATA AND SIGNAL DISTRIBUTION 1262
SPM 1264
PRODUCT-SPECIFIC IP BLOCK
1282
1280
SPM
1284
SPM
1234
MEMORY
1232
1230
1260
GENERAL PURPOSE IP BLOCK INCLUDING DSP
1270 1272
SPM
1274
POWER AND DISTRIBUTION MANAGEMENT 1290
PRODUCT STANDARD INTERFACE IP BLOCK INCLUDING ADC
1222
SPM
1224
MPM
1292
SENSOR
1212
RF
1214
CONTROL
1216
1220

FIG. 12

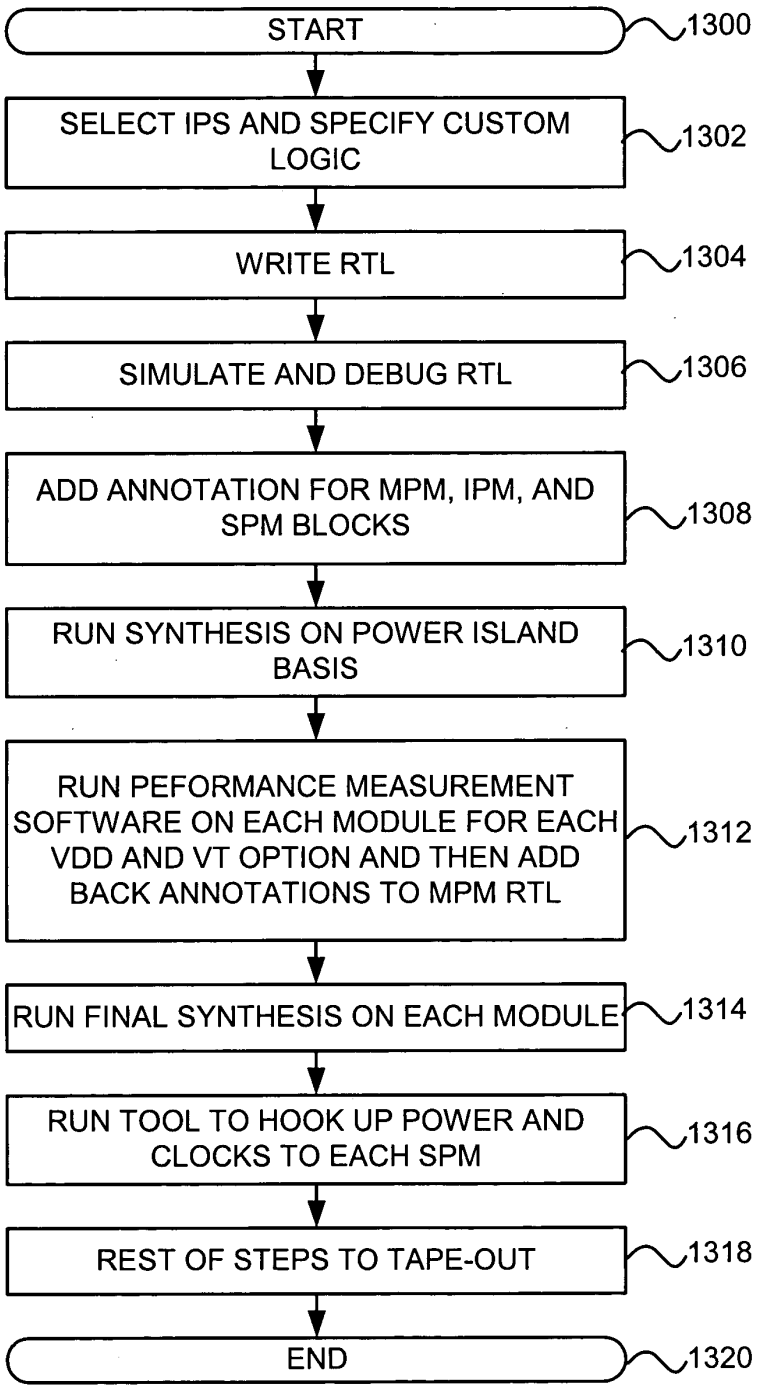
START
1300
SELECT IPS AND SPECIFY CUSTOM LOGIC
1302
WRITE RTL
1304
SIMULATE AND DEBUG RTL
1306
ADD ANNOTATION FOR MPM, IPM, AND SPM BLOCKS
1308
RUN SYNTHESIS ON POWER ISLAND BASIS
1310
RUN PEFORMANCE MEASUREMENT SOFTWARE ON EACH MODULE FOR EACH VDD AND VT OPTION AND THEN ADD BACK ANNOTATIONS TO MPM RTL
1312
RUN FINAL SYNTHESIS ON EACH MODULE
1314
RUN TOOL TO HOOK UP POWER AND CLOCKS TO EACH SPM
1316
REST OF STEPS TO TAPE-OUT
1318
END
1320

FIG. 13

ATTORNEY'S DOCKET NO.: PA2258US

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

"Managing Power on Integrated Circuits Using Power Islands"

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under Title 35, United States Code §119(a)-(d) or (f) or §365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):

Number	Country	Foreign Filing Date	Priority Claimed?	Certified Copy Attached?
(Number)	(Country)	(MM/DD/YYYY)	☐ Yes ☐ No	☐ Yes ☐ No
(Number)	(Country)	(MM/DD/YYYY)	☐ Yes ☐ No	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

Prior Provisional Applications:

60/468,742	May 7, 2003
(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Prior U.S. or PCT Applications Designating the U.S.:

(Application Number)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status -- patented, pending, abandoned)

POWER OF ATTORNEY: I hereby appoint the attorney(s) and/or agent(s) associated with the customer number **22830** to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

SEND ALL CORRESPONDENCE TO:

Eugene G. Kim
CARR & FERRELL *LLP*
2200 Geng Road
Palo Alto, CA 94303
TEL: (650) 812-3400
FAX: (650) 812-3444

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: Barry Alan Hoberman Citizenship: U.S.A.
Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: _____ Dated: _____
(Permanent ink only) *(Date of Signature)*

Mailing Address: 10290 Palo Vista Road, Cupertino, CA 95014
(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address: _____
(if the inventor lives at a location different than his/her mailing address)

Full name of second inventor: Daniel L. Hillman Citizenship: U.S.A.
Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: _____ Dated: _____
(Permanent ink only) *(Date of Signature)*

Mailing Address: 6607 Winterset Way, San Jose, CA 95120
(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address: _____
(if the inventor lives at a location different than his/her mailing address)

Full name of third inventor: Jon Shiell Citizenship: U.S.A.
Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: _____ Dated: _____
(Permanent ink only) *(Date of Signature)*

Mailing Address: 801 Seabury Drive, San Jose, CA 95136
(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address: _____
(if the inventor lives at a location different than his/her mailing address)

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number: 10840893

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	54	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	54 minus 20=	* 34
INDEPENDENT CLAIMS	3 minus 3 =	* —
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
X$ 9=		OR	X$18=	612
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	1382

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

05/11/2004 EHAILE1 00000060 10840893

01 FC:1001	770.00 OP
02 FC:1202	612.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033