

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Hoberman et al.
U.S. Patent No.: 7,051,306 Attorney Docket No.: 60246-0006IP1
Issue Date: May 23, 2006
Appl. Serial No.: 10/840,893
Filing Date: May 7, 2004
Title: MANAGING POWER ON INTEGRATED CIRCUITS
USING POWER ISLANDS

DECLARATION OF TAJANA ROSING, Ph.D.

I, Tajana Rosing, Ph.D., of San Diego, California, declare that:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of Infineon Technologies Americas Corp. (“Petitioner” or “Infineon”). I understand that Infineon is requesting that the Patent Trial and Appeal Board (“PTAB” or “Board”) institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 7,051,306 (“the ’306 patent”) (EX1001).

2. I have been asked to provide my independent analysis of the ’306 patent in light of certain prior art publications that I discuss below in Sections V-VIII. I previously offered an analysis of the ’306 patent in an earlier case (IPR2024-00598) based on many of the same prior art publications. I have been informed that the Board instituted a trial in that earlier case after finding that the ’306 patent’s claims were likely unpatentable. I further understand that the case was terminated due to a settlement between the parties before the Board reached a final decision. I stand by

and maintain my previous analysis, much of which is restated verbatim or nearly verbatim below. I have also continued to consider additional materials and further develop my understanding of the pertinent facts, as is evident throughout my discussions below in Sections V-VIII.

3. I am not currently an employee of Infineon. I received no compensation for this Declaration beyond my normal hourly compensation based on my time actually spent analyzing the '306 patent, the prior art publications cited below, and the issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the '306 patent.

II. QUALIFICATIONS

4. A summary of my background and qualifications as a technical expert for this case is provided below. A complete listing of my qualifications and background are detailed in my curriculum vitae ("CV"), which is attached hereto as Appendix A. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My curriculum vitae also includes information about my expert witness experience, with case numbers where available.

5. I am a distinguished professor, IEEE Fellow, and the Fratamico Endowed Chair in the Computer Science and Engineering Department at the University of California, San Diego, and adjunct distinguished professor in the Electrical and Computer Engineering Department at UCSD. My research focuses

on energy-efficient computing, computer architecture, embedded systems hardware, and software design. I am currently a Director of System Energy Efficiency Lab where I am leading a diverse research team on projects relating to system energy-efficiency.

6. I have over twenty-five years of academic and industry experience in applying, designing, studying, teaching, and writing about energy-efficient computing. In addition, my experience has spanned both hardware and software, operating systems and application programs, system communications and user interfaces. I received an Electrical Engineering Ph.D. degree in 2001 from Stanford University; my thesis was titled Energy Efficient System Design and Utilization. I earlier received an Electrical Engineering B.S. degree in 1992 from Northern Arizona University, an Electrical and Computer Engineering M.S. degree in 1993 from the University of Arizona, and an Engineering Management M.S. degree in 2000 from Stanford University. While at Stanford University, I worked in the same office and on the same machines where Yahoo was started, and just down the hall from the office where Google was started. After completing my M.S. in ECE, I worked at Altera Corporation as a senior design engineer for four years. During and after completing my Ph.D. degree, I worked with Stanford University and Hewlett-Packard Labs leading a team of researchers to develop products for the wireless portable devices market. At HP labs, my team's efforts also included work related

to content delivery networks, streaming video over wireless and videoconferencing using mobile platforms. A partial list of my publications during this period is below.

- T. Simunic, M. Smith, “Dynamic Power Management at HP,” Invited Paper in Special Issue of Design and Test Journal, 2001.
- G. Manjunath, V. Krishnan, T. Simunic, J. Tourrilhes, A. McReynolds, D. Das, V. Srinivasmurthy, A. Srinivasan, “Smart Edge Server: going beyond a wireless access point,” WMASH 04.
- B. Delaney, T. Simunic, N. Jayant, “Energy Aware Distributed Speech Recognition for Wireless Mobile Devices,” Special Issue on Embedded Systems for Multimedia, IEEE Design & Test, 2004.
- Acquaviva, T. Simunic, V. Deolalikar, S. Roy, “Remote Power Control of Wireless Network Interfaces,” Special Issue of Journal of Embedded Computing, No. 3, 2004.
- T. Simunic, W. Quadeer, G. De Micheli, “Managing heterogeneous wireless environments via Hotspot servers,” MMCN 05.

7. Through work with Hewlett-Packard Labs, I have been granted the following United States patents:

- U.S. Patent No. 7,272,730, titled “Application-driven method and apparatus for limiting power consumption in a processor-controlled

hardware platform,” which issued in 2007 from an application with a priority date in 2003;

- U.S. Patent No. 7,246,181, titled “Device and method for identifying a communication interface that performs an operating parameter closer to a desired performance level than another communication interface performs the operating parameter,” which issued in 2007 from an application with a priority date in 2004; and
- U.S. Patent No. 7,190,980, titled “Method and system for power control in wireless portable devices using wireless channel characteristics,” which issued in 2007 from an application with a priority date in 2004.

8. I have published over 400 publications and received a number of best paper awards and nominations. I have also been an invited speaker at numerous academic and industry conferences.

9. Since coming to UCSD, I have taught an undergraduate course on logic design, CSE 140, “Components and Design Techniques for Digital Systems,” and a graduate course in embedded systems, CSE 237a, “Introduction to Embedded Computing.” In my CSE140 course, I cover basics of transistor design, logic circuits, and components, all key components that go into design of processors, and Register-Transfer-Level design. The course ends with a design of a simple MIPS based processor. In CSE 140 I also cover how to estimate performance, and power

consumption of a logic circuit. In my graduate CSE237a course, I cover all topics related to design and validation of embedded and distributed systems. In the first third of the course, the students learn about all the key hardware components that go into today's embedded systems, including CPUs, GPUs, DSPs, FPGAs, various types of memory, interface design, sensors, actuators, ADC/DAC, communication subsystem, and control system design. The second third of the course is dedicated to embedded software, where we cover issues related to timing, real-time schedulers, and real-time operating system design, and discuss examples of embedded operating systems, including various versions of Linux & Windows used in embedded and mobile computing, Android, and embedded middleware. One of the key components we discuss in the course is audio, image and video standards for today's embedded systems. The last third of the course is focused on modeling strategies, testing and validation of embedded systems. Throughout the course, the students are expected to complete three projects. The first project requires students to build a mobile system that leverages sensors and actuators and schedules tasks using real-time scheduler implemented within a version of Linux. The second part of the course requires design of an energy efficient power manager within Linux or Android for the hardware designed in part one of the project. The last project is open for students to pick but has to involve both hardware and software for embedded systems. Many

students in my class work on projects that include video streaming and/or video conferencing.

10. Based on my experience and education, I believe that I am qualified to opine as to the knowledge and level of skill of a POSITA at the time of the '306 patent (which I further describe below), in addition to the general state of the art during that time.

III. LEGAL PRINCIPLES

11. In forming my analysis and conclusions expressed in this Declaration, I have applied the legal principles described in the following paragraphs, which were provided to me by counsel for the Petitioner.

A. Anticipation

12. It is my understanding that invalidation by “anticipation” exists only if a single alleged prior art reference discloses each and every limitation of the claim at issue, either expressly or inherently. In other words, every limitation of the claim must appear in a single prior art reference for the reference to anticipate that claim. I also understand that all elements of the claim must be disclosed in the reference as they are arranged in the claim. I also understand that to be considered anticipatory, the prior art reference must be enabling and must describe the patentee’s claimed invention sufficiently to have placed it in the possession of a person of ordinary skill in the field of invention. Under the principles of inherency, I understand that if the

prior art necessarily functions in accordance with or includes the claimed limitations, it anticipates.

13. I have been informed that a claim is invalid if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the Applicant's invention. I further have been informed that a claim is invalid if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). I have also been informed that a claim is invalid if an invention described by that claim was described in a U.S. patent granted on an application for a patent (or in a published application for a U.S. patent) that was filed by another in the U.S. before the date of invention for such a claim.

14. I understand that a dependent claim contains all of the limitations of the independent claim from which it depends. Thus, to establish anticipation, every limitation set forth in a dependent claim as well as the independent claim from which it depends must be found in an anticipatory reference.

B. Obviousness

15. I have been informed that a patent claim is invalid as "obvious" in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention ("POSITA"), taking into account (1) the scope and content of the prior art, (2) the differences between the

prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others.¹ I understand that a patent cannot be properly granted for subject matter that would have been obvious to a POSITA at the time of the alleged invention, and that a patent claim directed to such obvious subject matter is invalid under 35 U.S.C. § 103. It is also my understanding that in assessing the obviousness of claimed subject matter one should evaluate obviousness over the prior art from the perspective of a POSITA at the time the invention was made (and not from the perspective of either a layman or a genius in that art).

16. While I do not know the exact date that the alleged invention claimed in the '306 patent was made, I do know that the '306 patent was filed on May 7, 2004 (EX1001, Cover Page) and claims priority to a provisional application filed on May 7, 2003. For purposes of my analysis here, I have applied a date of May 7, 2003 (“Critical Date”) as the date of the alleged invention in my obviousness analysis, although in many cases the same analysis would hold true even if the date

¹ I understand that, at present, Patent Owner has not submitted any evidence of “secondary considerations.”

of the alleged invention occurred earlier than May 7, 2003 (especially given the earlier publication or filing dates of the cited prior art references).

17. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted (or “motivated”) a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference(s) themselves, the knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and this reason may be explicit or implicit from the prior art as a whole. I have been informed that, under the law, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

18. I understand that an obviousness determination also requires that a POSITA would have had a reasonable expectation of success. This concept has been explained to me as relating to the relative likelihood or predictability—from the perspective of a POSITA—of successfully obtaining a result within the scope of the challenged claim(s) based on the combined, modified, and/or suggested prior art

teachings at hand. I understand that the expectation of success need only be “reasonable” and, thus, does not require the absolute certainty gleaned from physically creating the prior art teachings.

C. Claim Construction

19. I understand that, for purposes of my analysis in this IPR proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history may be used to better understand a claim. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a person of ordinary skill in the art to a claim term at the relevant time of the challenged patent (i.e., the Critical Date). I have followed this approach in my analysis.

IV. PERSON OF ORDINARY SKILL IN THE ART

20. Based on my knowledge and experience in the field, my review of the ’306 patent and its file history, and my first-hand knowledge of undergraduate electrical engineering curricula at the time of the ’306 patent’s alleged priority date of May 2003, I believe a person of ordinary skill in the art (“POSITA”) at the time would have had at least a bachelor of science degree in electrical engineering,

computer engineering, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

V. MATERIALS CONSIDERED

21. My analyses set forth in this Declaration are based on my experience in the field of power management and integrated circuits. Based on my above-described experience in the field, I believe that I am an expert in the field. Also, based on my experience, I understand and know of the capabilities of persons of ordinary skill in this field during the late 1990s to early 2000s, and specifically during the time before the Critical Date (May 7, 2003) for the '306 patent. I taught, participated in organizations, and worked closely with many persons of such skill level in the field during that time frame.

22. As part of my independent analysis for this Declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the earlier claimed priority date for the '306 patent; my own knowledge and experiences gained from my work experience in the field of power management and integrated

circuits generally; my experience in teaching and advising others in such subjects; and my experience in working with others involved in the field of power management and integrated circuits or similar fields. In addition, I have analyzed the following publications and materials:

- U.S. Patent No. 7,051,306 to Hoberman et al. (“the ’306 patent”) (EX1001) and its accompanying prosecution history (EX1002);
- “A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling” by Nowka, et al. (“Nowka”) (EX1004);
- Declaration of June Ann Munford (EX1005);
- U.S. Patent No. 6,484,265 to Borkar et al. (“Borkar”) (EX1006);
- U.S. Patent No. 6,353,369 to Boerstler (“Boerstler”) (EX1007);
- U.S. Patent No. 6,141,762 to Nicol, et al. (“Nicol”) (EX1008);
- U.S. Patent No. 8,086,884 to Naffziger et al. (“Naffziger”) (EX1015);
- “Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design” by Kuroda et al. (“Kuroda”) (EX1016);
- “Dynamic Power Management: Design Techniques and CAD Tools” by Benini & De Micheli (“Dynamic Power Management”) (EX1017);
- “A Survey of Design Techniques for System-Level Dynamic Power Management” by Benini, et al. (“Benini Survey”) (EX1018)
- “Managing Power and Performance for System-on-Chip Designs using Voltage Islands” by Lackey, et al. (“Lackey”) (EX1019)
- “Policy Optimization for Dynamic Power Management” by Benini et al. (“Benini Policy Optimization”) (EX1020)

- “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling” by Semeraro et al. (“Semeraro”) (EX1021)
- “Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems” by Dutta et al. (“Dutta”) (EX1022)
- “The CoreConnect™ Bus Architecture” by IBM (“CoreConnect White Paper”) (EX1023)
- “The Computer Engineering Handbook” edited by Oklobdzija (“Computer Engineering Handbook”), excerpts (EX1024)
- “Computer Systems: Concepts and Design” by Gibson (“Gibson”), excerpts (EX1025)
- “Multimedia Information Networking” by Sharda (“Sharda”), excerpts (EX1026)
- U.S. Patent No. 6,345,362 to Bertin et al. (“Bertin”) (EX1027)
- “PowerPC 603 Microprocessor: Power Management” by Suessmith (“Suessmith”) (EX1028)

23. Although, for the sake of brevity, this Declaration refers to selected portions of the cited references, it should be understood that one of ordinary skill in the art would have viewed the references cited herein in their entirety, and in combination with other references cited herein or cited within the references themselves. The references used in this Declaration, therefore, should be viewed as being incorporated herein in their entirety.

VI. BACKGROUND INFORMATION

A. Background of the Technology

24. As of the Critical Date, power management in electronic systems, and specifically integrated circuits, was a commonly explored problem. EX1018 at 1 (“Most electronic circuits and system designs are confronted with the problem of delivering high performance with a limited consumption of electric power.”). The ’306 patent relates to power management in electronic systems, and specifically integrated circuits. EX1001, 1:19-20. In particular, the ’306 patent purports to address the problem of efficiently utilizing subparts of the integrated circuit, as not all components of the system need to be operating at the same power to execute a task. EX1001, 1:58-67.

25. Another issue that is addressed by the ’306 patent is the need for dynamic response to changing loads. EX1001, 2:11-16 (“One problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static. The voltages and the frequencies do not dynamically change based on the needs and operation of the integrated circuit.”); EX1020 at 2 (“The fundamental premise for the applicability of [dynamic power management] is that systems (and their components) experience nonuniform workloads during operation time. Such an assumption is valid for most systems, both when considered in isolation and when internetworked.”). I describe the state of the art at the time of

the alleged priority date of the '306 on these issues, with the aid of contemporary literature, below.

1. Power Consumption and Power Management

26. Around the time of the '306 patent's Critical Date, power management in integrated circuits was a widely researched topic due to the rise of portable electronics and high-performance systems. A textbook by Luca Benini and Giovanni De Micheli published in 1998 titled "Dynamic Power Management: Design Technique and CAD Tools," explains:

There has been a growing interest in techniques for designing integrated circuits and systems with low-power consumption in the last few years. Research in this field is motivated by two major markets: portable electronics and high-performance systems. In the former case, low-power circuits are needed to provide a reasonable operation time to battery-operated devices. In the latter case, environmental factors, such as heat dissipation, may pose a practical limit to the use of high-performance processors if power consumption is not controlled and limited.

EX1017 at 10. Numerous other texts at the time also highlight the rising importance of power management in portable electronics and high-performance systems. EX1019 (Lackey) at 1 ("As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption."); EX1020

(Benini Policy Optimization) at 1 (“Battery-operated portable appliances impose tight constraints on the power dissipation of their components. Such constraints are becoming tighter as complexity and performance requirements are pushed forward by user demand. Reducing power dissipation is a design objective also for stationary equipment, because excessive power dissipation implies increased cost and noise for complex cooling systems.”); EX1001, 1:19-26.

27. There are several types of power consumption at play in a CMOS (complementary metal-oxide semiconductor) circuit. Active power, also referred to as dynamic power, is the dominant form of power consumption in a CMOS circuit. *See* EX1017 at 17, 21 (“Summarizing the discussion on the contributions to power dissipation in CMOS circuits, we conclude that the dominant fraction (around 80%) of P_{avg} is attributed to $P_{dynamic}$, the dynamic power dissipation caused by switching of the gate outputs.”). Active power comes from the output switching of a CMOS gate during operation. The basic relationship between voltage, frequency, and active power ($P \propto CV^2F$) was well-understood by POSITAs at the time of the ’306 patent’s Critical Date. Hence, voltage scaling and frequency scaling were widely used to control active power. “Power consumption in clocked digital components (in CMOS technology) is roughly proportional to the clock frequency and to the square of the supply voltage. ***Power can be saved by reducing the clock frequency*** (and in the limit by stopping the clock), ***or by reducing the supply voltage*** (and in the limit by

powering off a component).” EX1018 (Benini Survey) at 12; *see also* EX1006 (Borkar), 1:19-23 (“The performance, power consumption, and temperature are typically related. The active power of a transistor is $P=CV^2F$, where C is the capacitance, V is the supply voltage, and F is the switching frequency.”); EX1015 (Naffziger), 1:52-59 (“As is well known, the switching power consumption of a chip may be generally computed utilizing the following equation: $P=C*V^2*F$, wherein P represents power consumption, C represents switching capacitance, V represents operating voltage, and F represents the clock frequency of the chip. In view of such equation, it should be understood that switching capacitance (C), voltage (V), and frequency (F) are all factors in determining the power consumption (P) of a chip.”).

28. Another power dissipation of concern is leakage power. While there are several types of leakage current, sub-threshold leakage current (caused by transistors which are nominally off but still conducting some current, especially if their threshold voltage is lower) was becoming more of a concern as supply voltages decreased. EX1017 at 20. “As power supply voltages decrease, the transistor threshold is lowered to keep turned-on transistors well within the conductive region of operation.” EX1017 at 20. One way of addressing leakage current was through tuning the transistor’s threshold voltage. EX1016 at 1 (“Lowering both the supply voltage V_{DD} and threshold voltage V_{TH} enables high-speed, low-power operation. . . . V_{TH} can be controlled through substrate bias.”); EX1006, 4:25-27

(“For example, the supply voltage and clock frequency may be decreased, and/or body bias signals changed so that the threshold voltage is raised.”).

2. Power Islands

29. It was well understood in the art that different components, or areas, of a system could be managed separately to maximize power savings. For example, it was well known in the art that multiple processors could be integrated on a single silicon chip. These processors need not be the same. In fact, it is helpful for them to have different capabilities, such as image or audio processing compared to general purpose processors. For example, the Dutta article on Philips Semiconductors’ “Viper” project describes a multiprocessor SOC containing multiple CPU cores, transport stream processor, video-processing blocks, and more. EX1022 at 1-4. Because these processors have different performance and power needs, they are amenable to separate power control. Additionally, it was known that separately controlling different components or different areas of a chip was desirable due to disparate power requirements. For example, “[i]ndividual functional blocks of the SoC design can have power characteristics unique from the rest of the design, and can be optimized accordingly.” EX1019 at 2.

30. Power islands were utilized to support separate voltage and frequency control for different parts of a chip. For example, the applicant admitted prior art (“AAPA”) identified in the ’306 patent acknowledges that “[s]ome prior integrated

circuits have employed voltage islands or multiple clocks to lower power consumption.” EX1001, 2:10-11. And indeed, power islands were well known. For example, the article “Managing Power and Performance for System-on-Chip Designs using Voltage Islands” by Lackey et al. (“Lackey”) discloses voltage islands on a system-on-chip. EX1019. A voltage island means that a particular area of the chip has a single supply voltage that is controlled separately from another voltage island. This makes it possible to set different voltage and frequency parameters to each island as a function of the needs of the component(s) in that island.

31. I note that the examiner issued obviousness rejections over Lackey during prosecution of the ’306 patent. EX1002 at 77-82 (Aug. 3, 2005 Final Rejection), 130-135 (Feb. 24, 2005 Non-Final Rejection). In response, the applicant stated that the “voltage islands” in Lackey do not disclose changing frequency in the islands. EX1002 at 68-69 (Sept. 26, 2005 Applicant Remarks), 113-14 (May 26, 2005 Applicant Remarks). Notably, the examiner issued a final rejection of the pending claims based on Lackey in combination with a supplemental reference—“Dynamic Frequency Management for Low-Power Embedded Microprocessor to Akui et al.—disclosing “dynamic frequency control.” EX1002 at 76-79 (Aug. 3, 2005 Final Rejection). The applicant never tried to distinguish the supplemental Akui reference on the merits, and instead successfully argued that the Akui reference did not qualify as prior art. EX1002 at 68-69 (Sept. 26, 2005 Applicant Remarks).

What the examiner seems to have misunderstood, however, is that Akui’s dynamic frequency control teachings are not unique. Indeed, the capability of changing frequency in power islands was widely known in the art before the Critical Date, as demonstrated by the references in the petition as well as other contemporary literature. *E.g.*, EX1004, 1444 (“V. Dynamic Voltage and ***Frequency Scaling*** Measurements.”); EX1008, 5:66-6:2 (“A separate power supply for each [processing element] in a chip overcomes this limitation by allowing the operating system to independently program ***the lowest operating frequency*** and corresponding lowest supply voltage for each PE.”). As another example, the article “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling” by Semeraro et al. (“Semeraro”) describes a chip that is “divided into several (coarse-grained) clock domains, within which independent ***voltage and frequency scaling*** can be performed.”). EX1021 at 1.

3. Dynamic Power Management

32. Those in the art around the time of the Critical Date understood that “one of the most successful approaches to power minimization is dynamic power management.” EX1017 at 221; *see also* EX1020 (Benini Policy Optimization) at 1 (“One of the most successful techniques employed by designers at the system level is dynamic power management.”). Dynamic power management (“DPM”) refers to dynamically reconfiguring an electronic system to provide the requested services

while minimizing power consumption. EX1018 at 1. “This technique reduces power dissipation by selectively turning off (or reducing the performance of) system components when they are idle (or partially unexploited).” EX1020 at 1. DPM is based on the assumption that not all components need to be at peak performance at all times, and that the varying need for different components can be reasonably predicted. EX1017 at 77-78; EX1018 at 1.

33. DPM can be implemented at different levels of abstraction. EX1017 at 221 (“Dynamic power management is a technique that spans multiple level of abstraction (from the logic level to the system level).”); EX1018 at 1 (“Dynamic power managers can have different embodiments, according to level (e.g., component, system, network) where DMP is applied[.]”). The power manager to execute DPM can take various physical implementations, such as hardware, or software supported by hardware. EX1018 at 13 (“[T]he power manager may be a hardwired or micro-programmed controller, and possibly merged with the system controller.”), 14 (“Software power managers are easy to write and to reconfigure.”).

B. Overview of the '306 Patent

34. The '306 patent relates to managing power on an integrated circuit (“IC”) using power islands. EX1001, Abstract, 2:21-24. The '306 patent explains that reducing power consumption in integrated circuits is a design goal that is increasing in importance as ICs become more complex and power consuming.

EX1001, 1:19-26, 2:1-9. One alleged problem in the existing art, according to the '306 patent, is "that power consumption is not efficiently utilized." EX1001, 1:58-59. "For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency." EX1001, 1:59-63.

35. The '306 patent explains that while "[s]ome prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption The voltages in the power island and the frequencies of the multiple clocks are static. The voltages and frequencies do not dynamically change based on the needs and operation of the integrated circuit." EX1001, 2:10-16. Therefore, the '306 patent suggests dynamically changing voltage and frequency in response to changing needs of the IC. *See* EX1001, 2:14-16, 4:28-31, 4:47-55, 7:52-56.

36. The '306 patent describes power islands whose power consumption is independently controlled. EX1001, Abstract, 2:21-24. As illustrated in Figure 1, a power island is "any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division." EX1001, 3:51-54.

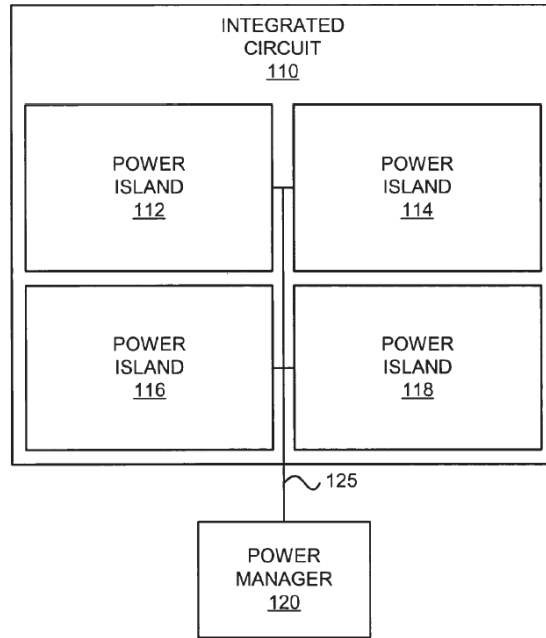


FIG. 1

EX1001, Fig. 1.

37. The system has a “power manager” that determines a target power level for one of the power islands and then determines an action to change the power consumption of that island to the target power level. EX1001, Abstract, 2:24-30. The action to change the power consumption can be selecting a clock frequency or modifying voltage for one of the power islands, among other actions. EX1001, 2:32-38, 4:45-55, 5:34-36.

38. Figure 2 of the '306 patent depicts a diagram for power management in system 200. Embedded firmware stack (210) includes power management software layers and communicates with the integrated circuit to control power of the power islands (260 and 270) through a master power manager (280) and slave power managers (264 and 274). EX1001, 4:56-5:8, 10:13-16. The master power manager

controls the global power behavior of the integrated circuit and the slave power managers control power within a power island. EX1001, 5:47-53, 6:11-14.

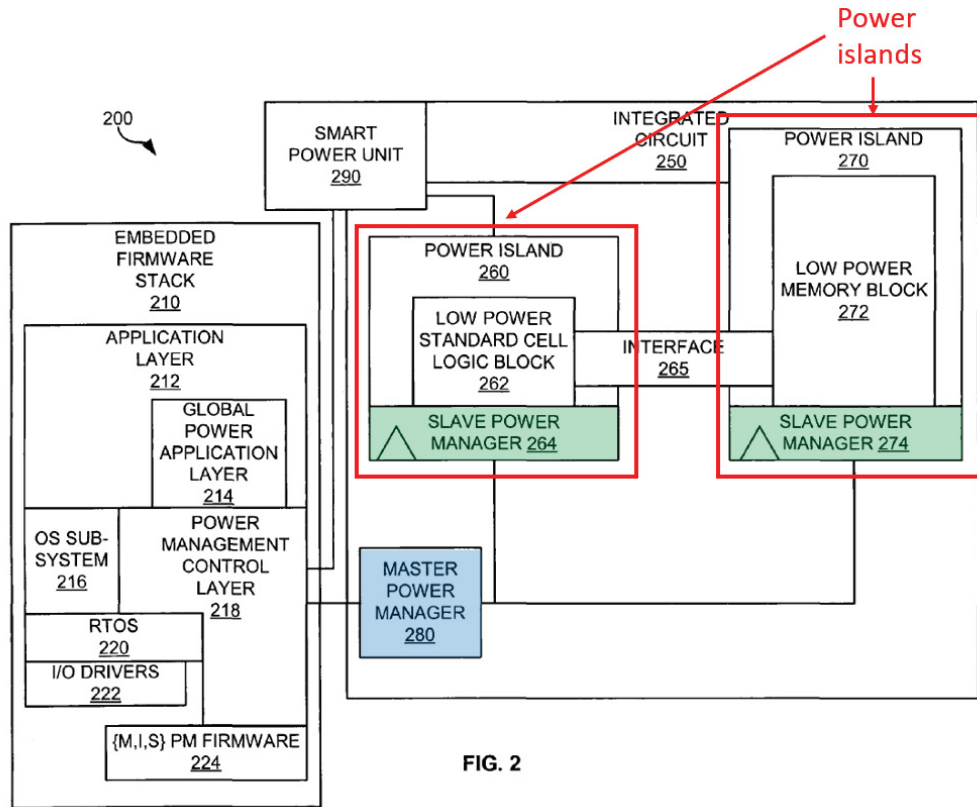


FIG. 2

EX1001, Fig. 2.

39. Figure 5 is flowchart showing an exemplary power management process. First, the system invokes an application “such as playing a movie” (502). EX1001, 7:41-42. Then, the application determines the required frequency for an IP unit, which may be a power island or a part of a power island (504). EX1001, 3:57-61, 7:42-50. The application then invokes the power management control layer (PMCL) API to send instructions with the appropriate frequencies and voltages to the master power manager, which then sends those requests to the applicable slave power manager(s) (508, 510, 512, 514, 516, 518, 520). EX1001, 7:51-8:22. The

slave power manager then performs the commanded actions, which may be switching the Vdd mux; switching a clock mux; or changing the threshold voltage (Vt) (522, 524, 526, 528). EX1001, 8:23-33.

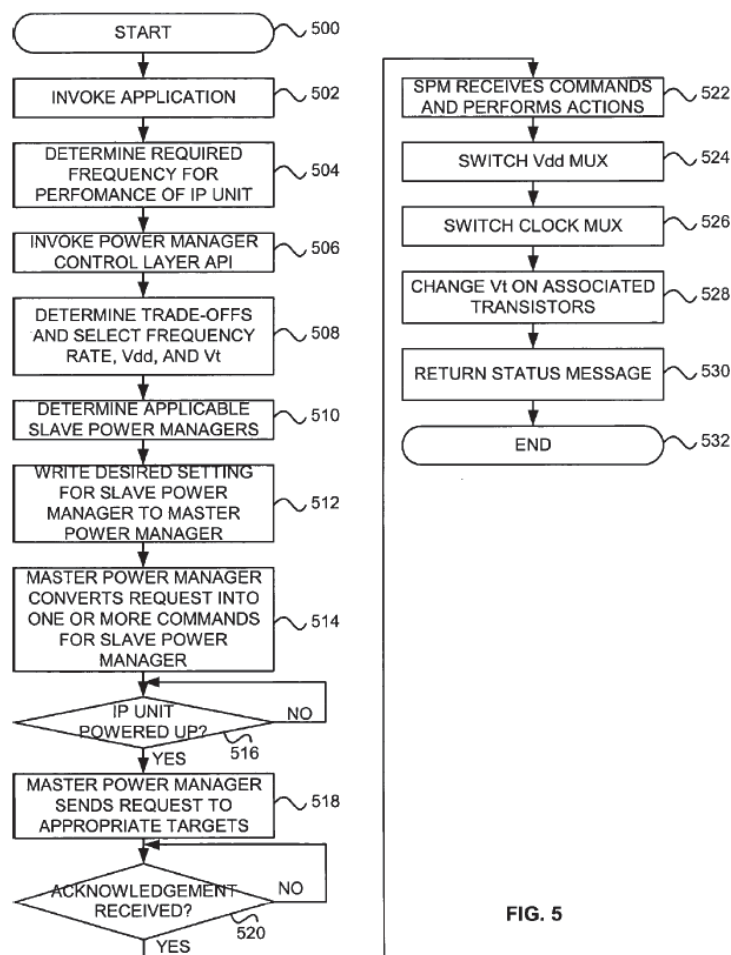


FIG. 5

EX1001, Fig. 5.

C. Prosecution History of the '306 Patent

40. U.S. Application 10/840,893, which resulted in the '306 patent, was filed May 7, 2004. The '306 patent claims priority to provisional application 60/468,742, filed May 7, 2003. EX1002, 174. The Patent Office issued one non-final rejection and one final rejection during prosecution. EX1002, 127-135 (Feb.

24, 2005 Non-Final Rejection), 73-83 (Aug. 3, 2005 Final Rejection). The Office never considered Nowka, Bertin, Nicol, Borkar, Boerstler, or Naffziger. These references render the '306 patent's claims obvious, as discussed below.

D. Interpretations of the '306 Patent Claims at Issue

41. I have followed the claim construction approach outlined above at ¶19 in my obviousness analysis below. For all of the claim terms considered in this Declaration, I have applied the plain and ordinary meaning of those terms. I understand that certain claim terms in the '306 patent were subject to construction in prior proceedings (EX1011; EX1012; EX1013). However, it is my opinion that it is not necessary for the Board to adopt any of these constructions at least because, as explained below with regard to specific claim elements, the prior art references render the '306 patent's claims obvious even if the construction were to be adopted.

VII. OVERVIEW OF CONCLUSIONS FORMED

42. I have reviewed the Petition for IPR of the '306 patent, and I agree with the analysis contained therein. In summary, it is my opinion that each and every limitation of each and every Challenged Claim (the '306 patent's claims 1-51) would have been obvious to one of ordinary skill in the art at the Critical Date in view of the prior art cited in the Petition and further explained in this Declaration. To summarize my conclusions below:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51 of the '306 patent are rendered obvious by Nowka.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 9, 13, 24, 28, 45, and 49 of the '306 patent are rendered obvious by Nowka in view of Borkar.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claim 35 of the '306 patent is rendered obvious by Nowka in view of Boerstler.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-12, 14-23, 25-27, 29-34, 36-48, 50-51 of the '306 patent are rendered obvious by Nowka in view of Bertin.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, and 47 of the '306 patent are rendered obvious by Nicol.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 6, 10, 12, 14-15, 21, 25, 27, 29-30, 34, 46, 48, 50-51 of the '306 patent are rendered obvious by Nicol in view of Nowka.

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 13, 28, and 49 of the '306 patent are rendered obvious by Nicol in view of Borkar.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claim 35 of the '306 patent is rendered obvious by Nicol in view of Naffziger.

VIII. ANALYSIS OF THE PRIOR ART

A. Analysis of Nowka with Respect to Claims 1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51

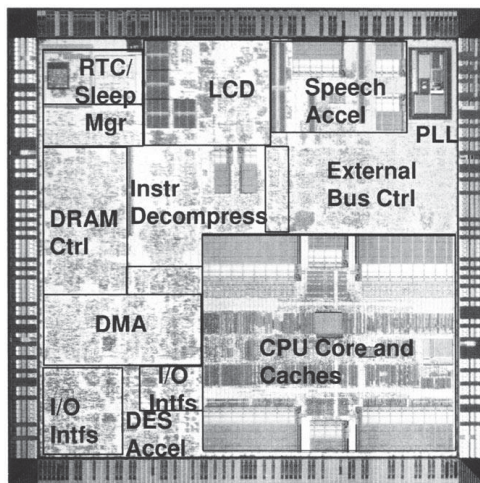
43. For the reasons articulated in detail below, and based on my review of the '306 patent and the Nowka reference, I am confident that a POSITA would have readily understood that Nowka renders obvious claims 1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51.

1. Overview of Nowka

44. Nowka is titled “A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling.” EX1004, Title. Nowka relates to a PowerPC system-on-a-chip (“SOC”) processor that “makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.” EX1004, Abstract. Nowka’s PowerPC

SOC is intended to maximize battery life for information appliances. EX1004, 1441.

Figure 2 below shows the physical layout of the SOC.



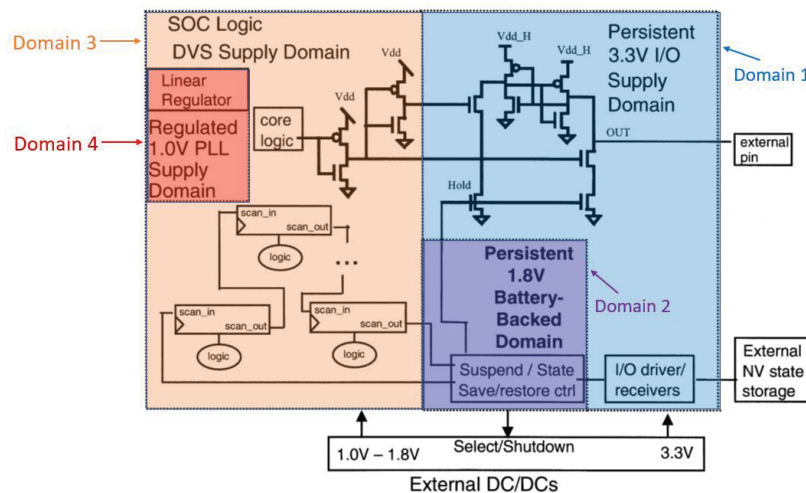
EX1004, Fig. 2.

45. Nowka explains that during “active computation,” the SOC’s “required performance tends to vary widely and quickly as a function of the workload” and that while peak performance demands high power consumption, periods of inactivity allow for minimization of power consumption. EX1004, 1441. To “match the performance and power consumption of this device to the application,” Nowka uses dynamic voltage scaling (DVS). According to Nowka, “DVS systems adjust the supply voltage dynamically to meet the performance demands while minimizing power consumption.” EX1004, 1442, Section III.C. Nowka also implements dynamic frequency scaling, clock gating, and standby modes to dynamically adjust power consumption. EX1004, Sections V, VI, VII.

46. The Nowka SOC is “divided into four distinct domains,” shown in Figure 3. These domains consist of two persistent voltage domains, one internally

derived domain, and one dynamically voltage-scaled logic domain. EX1004, 1442.

One of the persistent voltage domains operates at 3.3V and powers the I/O drivers and receivers (domain 1 below). The other persistent voltage domain operates at 1.8V and powers the real-time clock and the clock associated with controlling the voltage of the cores (domain 2 below). The phase locked loop (PLL) is powered by an on-chip linear regulator that derives its 1V supply from the dynamically-varying logic supply (domain 4 below). The dynamically-varying logic supply varies between 1V and 1.8V and powers the processor core, caches, SOC cores, and accelerators (domain 3 below). EX1004, 1442. The operating frequency of the variable voltage domain (domain 3) can also be altered for active power reduction. EX1004, 1444 (“When the performance demands of the application decrease, the system software can lower the operating frequency.”).



EX1004, Fig. 3²

² All annotations to the figures have been added unless noted otherwise.

47. During operation, the logic supply is controlled by an “on-chip supervisor” that, under software control, “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” EX1004, 1442. The supply voltage to the logic can change between 1V and 1.8V and the frequency can be varied to reduce power consumption. Nowka states that the “ability to change the output clock divider on-the-fly, without pausing the processor, allows the SOC to operate over an extremely broad range of frequencies. This allows the power consumption to be determined by the system on a very fine time scale.” EX1004, 1446. Nowka’s SOC also uses clock gating and standby modes to reduce power consumption by the logic elements. EX1004, 1445-46.

2. Claim 1

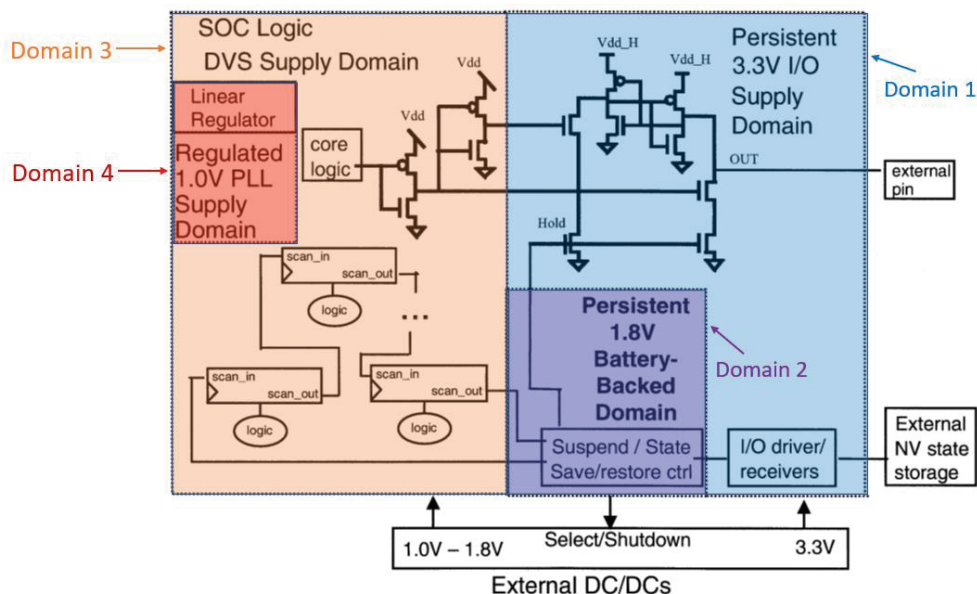
(a) Element 1[p]

48. Element 1[p] recites: “A method of managing power on an integrated circuit including a plurality of power islands, the method comprising.” Nowka discloses and/or renders obvious Element 1[p].

49. Nowka describes “a PowerPC system-on-a-chip processor” where the “power distribution has been divided into four distinct domains.” EX1004, Abstract, 1442. Nowka further describes that SOC’s “peak performance demands tend to be significant, [but] they are also highly power constrained.” EX1004, 1441. To reduce power consumption and prolong battery life in mobile applications, Nowka’s SOC

is “optimized for efficiency” where “both the voltage and the frequency of the processor can be modified, thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption.” EX1004, 1446.

50. Figure 3 of Nowka, shown below, shows four domains that are supplied different voltages. These domains correspond to the “power islands” of the ’306 patent. The ’306 patent defines “power island” as “any section, delineation, partition, or division of the integrated circuit [] where power consumption is controlled within the section, delineation, partition, or division.” EX1001, 3:51-54. Nowka’s voltage domains satisfy this definition of “power island,” as each domain is a section, delineation, partition, or division of Nowka’s SOC, and each domain receives a different power supply.



EX1004, Fig. 3.

51. Nowka further explains that the variable voltage and frequency logic domain includes multiple “cores”—e.g., a “processor core,” a “dedicated speech accelerator, an instruction decompression engine and a DES accelerator core,” and a “LCD core,” (EX1004, 1442, 1444). A POSITA would have understood and found obvious that these individual “cores” are also capable of being controlled as power islands by varying their voltage and frequency independent of the remainder of the SOC.³ For example, according to Nowka, “[a]ctive power of the SOC can be further reduced through modification of the clock frequency within the individual cores” and “the clocks to individual functional cores can also be frozen by the clock and power management software.” EX1004, 1445. Accordingly, even if the claim term “power island” were construed narrowly, as in the prior litigations,⁴ Nowka’s

³ Note that below, for example, with respect to dependent claim 4, I apply Nowka’s disclosure of individual “cores” when addressing the ’306 patent’s claimed “power sub-islands.” The cores are themselves power islands and also subordinate power islands relative to the power island of the logic domain as a whole.

⁴ *See, e.g.*, EX1013 at 23 (“[T]he The Court therefore hereby construes ‘**power islands**’ to mean ‘**a section of an integrated circuit where power consumption is capable of being controlled by independently varying its operating voltage and its frequency of operation.**’” (original emphasis)).

disclosure regarding the individual and independently controllable “cores” within the logic domain would still render the ’306 patent’s claims obvious as discussed here and throughout the remainder of my analysis.

(b) Element 1[a]

52. Element 1[a] recites: “determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands.” Nowka discloses and/or renders obvious Element 1[a].

53. A POSITA would have recognized that Nowka’s SOC determines a target power level for one of the power islands based on needs and operation of the integrated circuit. As discussed for Element 1[p], Nowka’s SOC is “optimized for energy efficiency” to allow for “performance demands of the application to be met while minimizing the dynamic power consumption.” EX1004, 1446. The “performance demands” correspond to the “needs and operation of the integrated circuit” of Element 1[a], while “minimizing the dynamic power consumption” relates to “determining a target power level” of Element 1[a]. To say it another way, like the ’306 patent, Nowka’s target power level corresponds to a “desired...power consumption,” (EX1001, 4:28-33)—the minimal power consumption necessary to satisfy the performance demands of the application, (EX1004, 1446). For example, with “applications [that] tend to have peak performance demands as high as 500

MIPS,” Nowka explains that “the power consumption of the processor core is best kept at or below about 500 mW.” EX1004, 1441. By contrast, Nowka says, “active power consumption [can also be adjusted] as low as 53 mW at a supply of 1.0 V.” EX1004, 1441.

TABLE II
CPU CORE WITH CACHES CHARACTERISTICS

	TC1 (1.8V)	TC2 (1.0V)
Maximum Frequency (estimate)	380 MHz	152 MHz
Power Consumption (estimate)	500 mW	53 mW
TC1 – Typical conditions: 1.8V, 55C, nominal silicon		
TC2 – Typical conditions: 1.0V, 55C, nominal silicon		

EX1004, Table II

Moreover, in Nowka, like the '306 patent, this minimal power consumption approach is *determined* by “software control.” EX1004, 1446; *see also* 1442 (“Under software control”), 1444 (“the clock and power management software”), 1445 (“this allows the power consumption to be *determined* by the system on a very fine time scale”), *compare with* EX1001, 4:56:67 (describing power management firmware and software), 13:14-23 (explaining that the disclosed techniques can be performed by “software” instructions).

54. In Nowka’s SOC, “[t]he active power consumption is reduced when resource demands are low through the use of dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating.” EX1004, 1442; *see also* EX1004, 1444 (“[w]hen the performance demands of the application

decrease, the system software can lower the operating frequency. . . . [a]t a given supply voltage, the frequency of the core can be varied from the maximum to $1/64^{\text{th}}$ of the maximum[.]”). In addition, Nowka discloses placing components in standby modes such as “Freeze,” “Hibernation,” and “Cryo” modes to minimize standby power. EX1004, 1446. A POSITA would have understood that the actions of dynamic voltage scaling, dynamic frequency scaling, functional clock gating, and standby modes are used to adjust the power level of a power island to a target power level, which is determined based on the needs and operation (in this example, low resource demands) of the integrated circuit. Below, I further explain how each of these actions shows “determining a target power level for one of the power islands based on needs and operation of the integrated circuit,” as recited in Element 1[a].

55. First, Nowka adjusts the voltage level in the logic domain based on the various requirements of the application being run on the system. In Section III.C, Nowka discusses the power consumption results of voltage scaling while running Dhrystone2.1 benchmark and MPEG-4 decoding on the SOC. Under Dhrystone2.1, the SOC consumed 570 mW at 333 MHz at the nominal supply voltage; when supply voltage to the logic domain was lowered, the SOC consumed 33 mW at 66 MHz. EX1004, 1444. While running MPEG-4 decoding at varying throughput rates, the supply voltage was also varied, which resulted in varying power consumption levels for the SOC. EX1004, 1444. A POSITA would have understood that the supply

voltage could be lowered at lower throughput rates to conserve power. Both of these examples demonstrate that the target power level of a power island (logic domain) is shifted in response to needs and operation of the integrated circuit (varying requirements of the application being run, or different requirements from different applications).

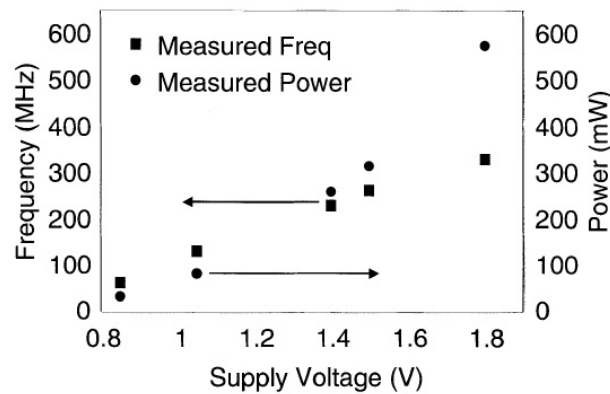


Fig. 5. Dhrystone2.1 voltage scaling measurements.

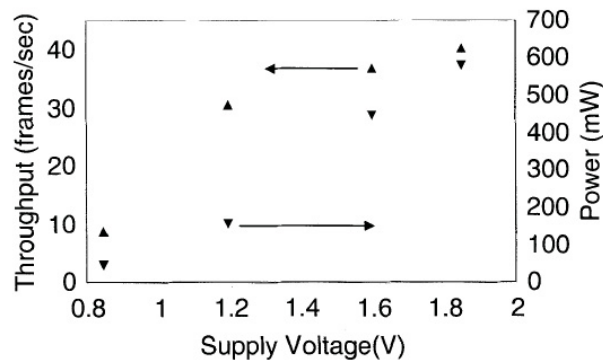


Fig. 6. MPEG-4 decode voltage scaling measurements.

EX1004, Figs. 5, 6

56. Second, Nowka also changes frequency to respond to anticipated performance demands. Figure 8 presents measurements of total power, logic power,

and I/O power in response to dynamic voltage and frequency scaling in the logic domain. EX1004, 1444.

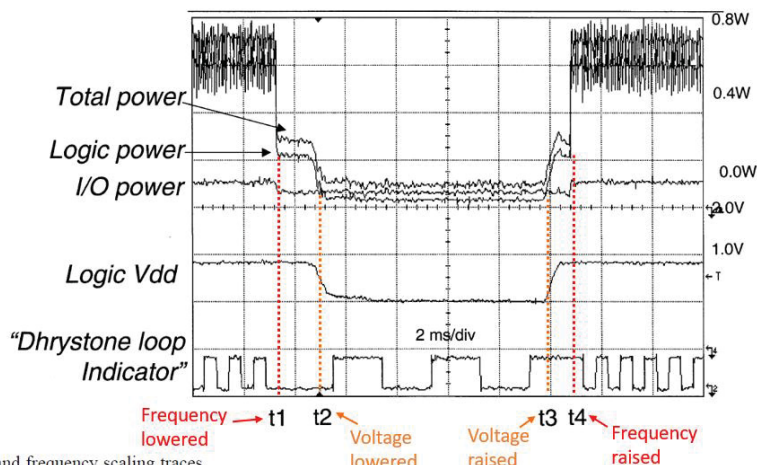


Fig. 8. Dynamic voltage and frequency scaling traces.

EX1004, Fig. 8.

In the scenario shown in Fig. 8, the logic supply starts at 1.8 V and frequency at 266 MHz. “In anticipation of lower performance demands, the clock and power management software modifies the PLL output divider value, which results in a decrease in frequency to 66 MHz at time t1.” EX1004, 1444. In response, the logic power falls by about 70%. Then, the logic supply voltage is lowered to 1 V through t2 (shown in the “Logic Vdd” trace, although there appears to be a labeling error on the right y-axis with regards to the placements of “2.0V” and “1.0V”), during which time there is a further significant drop in power consumption. EX1004, 1444. The “Dhrystone loop indicator” trace at the bottom shows the slower, albeit uninterrupted, frequency of Dhrystone loops execution. EX1004, 1444. Then, “anticipating an increase in demand, the logic supply is raised to 1.8 V without interrupting execution” at t3 and “the clock and power management software raises

the frequency” at t4. EX1004, 1444. At t3 and t4, the total power as well as logic power and I/O power all increase. Figure 8 therefore demonstrates Nowka’s SOC determining a target power level (via lower or higher frequency and voltage) based on needs and operation of the integrated circuit (lower or higher performance demands).

57. In these examples, the supply voltage and operating frequency of the logic domain are varied to adjust to the needs and operation of the SOC. A POSITA would have understood and found obvious that adjusting the operating frequency and/or supply voltage entails determining a target power level for the power island. These actions were well-understood in the art as mechanisms for dynamic power management because of power’s direct relationship with frequency and quadratic relationship with voltage. *See, e.g.*, EX1018 at 12 (“For components that are in an active state but whose response is not performance critical, **power consumption** can be traded off for performance **by reducing the clock frequency or the supply voltage**. The latter solution is usually preferred because of the quadratic dependence of power consumption on supply voltage, and it is often combined with frequency downscaling.”); EX1006, 1:19-23; EX1007, 1:52-59. Indeed, Nowka explains: “[f]or battery-powered applications where both energy efficiency and performance are crucial, **voltage scaling** enables a wide range of performance and **power consumption**.” EX1004, 1442. Further, the Nowka SOC’s ability “to operate over

an extremely broad range of frequencies “allows the *power consumption* to be determined by the system on a very fine time scale. After dynamic voltage scaling, this *dynamic frequency scaling mechanism* is the second method used to *reduce the active power* of this processor.” EX1004, 1445.

58. These examples, and additional examples discussed below, mirror the approach of the '306 patent for setting a target power level for a power island. The '306 patent broadly states that the “target power level” is “a desired, calculated, or specified power consumption of the power islands,” (EX1001, 4:31-33); and the '306 patent describes exemplary techniques that rely on the proxy relationship between parameters such as frequency and voltage to power in determining the target power level.⁵ Figure 5 in the '306 patent illustrates this approach. Figure 5 shows

⁵ Notably, the '306 patent does not explicitly discuss examples that involve measuring power consumption level via measuring current and multiplying it with voltage, which a POSITA would have understood to be a more accurate, albeit costlier, method of measuring power consumption. See EX1006 at 13:2-8 (“Different techniques may be used to not exceed power consumption levels. A simple but imprecise way is to not allow the supply voltage, threshold voltages, or frequency, to pass certain levels. A more precise way is to detect current being consumed. The power can be determined from the current and supply voltage.”).

that “[i]n step 502, an application is invoked such as playing a movie. In step 504, the application *determines the required frequency* for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder.” EX1001, 7:41-46. Then, “[t]he PMCL 218 determines possible trade-offs available for the unit and *selects a frequency rate, Vdd, and Vt* if applicable for the unit that best meets the given requirements in step 508 and determines the applicable SPMs 264 and 274 in step 510.” EX1001, 7:62-66; *see also* EX1001, 8:56-9:26, Fig. 8 (similar).

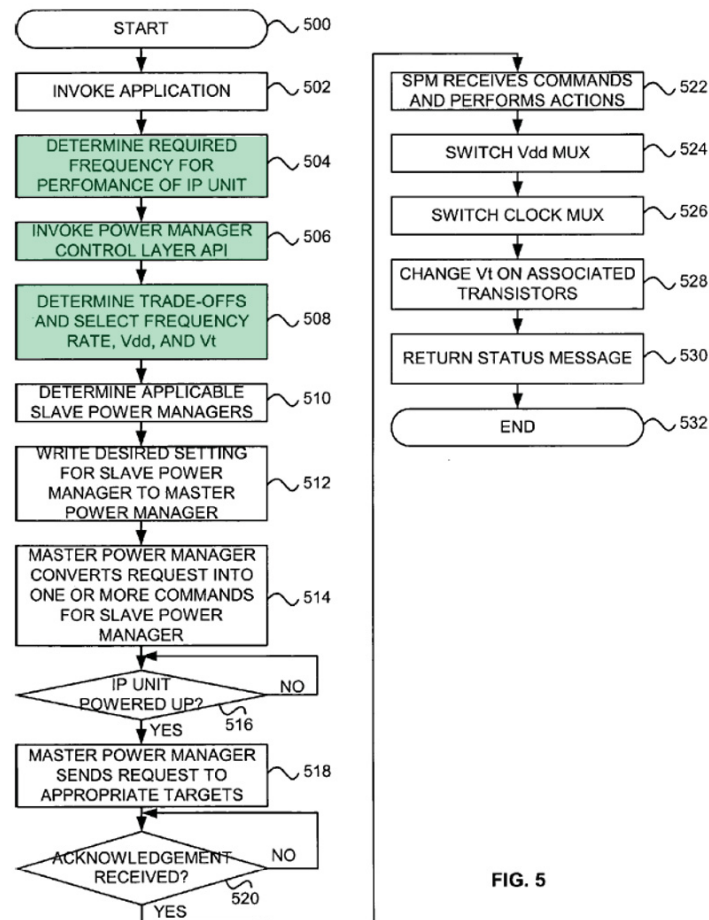


FIG. 5

EX1001, Fig. 5.

59. A POSITA would have understood that the '306 patent also illustrates determining a “target power level” through adjusting parameters such as frequency, Vdd, or Vt, relying on these parameters’ proxy relationship with power consumption. See, e.g., EX1001, 5:31-36 (“The PMCL 218 also collects information from the MPM 280 and provides commands to the MPM 280 for possible IPMs, SPMs 264 and 274, and the power islands 260 and 270. Some of the commands may be to power on/off, *change the power level*, or *change the frequency* of the power islands 260 and 270.”); 7:46-48 (“In some embodiments, when the IP unit is totally asynchronous, *the required frequency will be an artificial measure of performance*.”). Therefore, a POSITA would have understood that Nowka, like the '306 patent, provides a method for determining a target power level based on needs and operation of the integrated circuit using parameters such as frequency and voltage of the power island as a proxy for the power level.

60. Moving on to another example in addition to voltage and frequency scaling, Nowka also discloses clock gating inactive registers and cores to conserve dynamic power in the logic domain. “Approximately 80% of the processor registers and 50% of the SOC core registers are functionally clock gated when they are not accessed. At a higher level, the clocks to individual functional cores can also be frozen by the clock and power management software. This is done either in response to inactivity or through a force condition by the clock and power manager.”

EX1004, 1445. It was well-known to POSITAs at the time that clock gating was an effective means of power control. *See* EX1017 at 11 (“Sequential circuits, such as control-units, display often a large degree of idleness due to their reactive nature. Techniques based on ***clock gating*** and/or on decomposition have been shown to be successful in reducing their power consumption.”); EX1018 at 12 (“When considering possibly idle digital components, clock gating (or freezing) is the most common technique for power management. Namely, the clock of an idle component can be stopped during the period of idleness. Power savings are achieved in the registers (whose clock is halted) and in the combinational logic gates where signals do not propagate due to the freezing of data in registers.”). A POSITA would have understood that Nowka’s clock gating entails determining a target power level (lower power) based on needs and operation of the integrated circuit (not accessing certain latches, units, or registers).

61. Additionally, Nowka discloses placing the logic domain into various “standby modes” to conserve power. Nowka discusses three “classes” of standby: Freeze, Hibernation, and Cryo modes, which “achieve a range of standby power levels.” EX1004, 1446. In freeze mode, “the system clock is stopped and the logic supply is decreased to its minimum value of 1.0 V.” EX1004, 1446. In hibernation mode “the logic supply to the processor, caches and the SOC cores is disconnected. . . . This mode eliminates the leakage component of the standby power.” EX1004,

1446. In cryo mode, the logic supply is similarly disconnected. EX1004, 1446. A POSITA would have understood these standby modes are part of determining a target power level (lower standby power) based on needs and operation of the integrated circuit (full operation of logic components not needed).

62. These actions would have made it obvious to a POSITA that Nowka's system is engaging in determination of target power levels based on varying needs of the system. In this regard, the '306 patent and Nowka both discuss the ability to dynamically set target levels using frequency scaling, voltage scaling, or some other action, while not limiting the specific algorithm that must be employed. Therefore, it would have been obvious to a POSITA that Nowka provides "determining a target power level for one of the power islands based on needs and operation of the integrated circuit."

63. On the limitation on "based on needs and operation of the integrated circuit," I understand that in prior litigations involving the '306 patent, the parties in those litigations agreed to a construction of "based on future operational needs and current operating status of the integrated circuit." EX1011 at 48, EX1012 at 9; EX1013 at 26. It is my opinion that no construction of this limitation is needed because the plain and ordinary meaning suffices. The '306 patent itself does not provide explanation of this phrase aside from reciting it twice in the specification. EX1001, 2:14-16, 4:28-31. The '306 patent simply provides examples of

determining parameters such as required frequency, supply voltage, or threshold voltage, given the demands of a particular application. EX1001, 7:38-50, 8:56-62. As explained above, Nowka's disclosures mirror the approach that the '306 patent takes with respect to setting a target power level "based on needs and operation of the integrated circuit."

64. Additionally, while there is no briefing regarding the prior-agreed upon construction in the *Freescale* (EX1011), *Conversant* (EX1012), and *MediaTek* (EX1013) litigations, it is my opinion that Nowka, in light of a POSITA's knowledge, also satisfies that construction for the reasons discussed above. For example, Nowka's discussion that the system software changes frequency and voltage "*[i]n anticipation* of lower performance demands" shows that its power management is responsive to future operational needs, while Nowka's disclosure that the software, "anticipating an increase in demand, [raises] the logic supply . . . to 1.8 V *without interrupting execution*" shows that it is also responsive to the current operational status of the integrated circuit. EX1004, 1444.

65. Nowka also discloses that power consumption is independently controlled in a power island. For example, each power island shown in Figure 3 above is powered independently. Nowka states that domain 1 is powered by a persistent 3.3V supply; domain 2 is powered by a persistent, battery-backed 1.8V supply; domain 3 receives a dynamic supply varied between 1.0-1.8V which is

controlled by external DC/DC converter; domain 4 is powered by an on-chip linear regulator and receives a constant 1V supply from the dynamically-varying logic supply. EX1004, 1442, Fig. 3. A POSITA would have understood that powering these domains independently allows for independent power control, as illustrated by Nowka's dynamic voltage and frequency scaling in the logic domain even as the other domains are powered persistently. Additionally, as I discussed above at Element 1[p], Nowka teaches that the logic domain includes *power islands* in the form of multiple "cores," (EX1004, 1442, 1444), which are capable of being controlled by varying their voltage and frequency independent of the remainder of the SOC. *E.g.*, EX1004, 1445.

(c) Element 1[b]

66. Element 1[b] recites: "determining at least one of actions to change a power consumption level of the one of the power islands to the target power level." Nowka discloses and/or renders obvious Element 1[b].

67. As explained for Element 1[a], Nowka discloses various actions to change a power consumption of a power island to the target power level that minimizes power consumption while meeting application performance demands. Again, Nowka similarly provides capabilities for power management over the individual "cores" in this way. EX1004, 1445. For sake of clarity, I will reiterate a portion of my prior analysis below:

68. First, Nowka discloses varying the frequency of the system to change the power consumption level of the logic domain, and the system as a whole. EX1004, 1444, Section V (describing the scenario depicted in Figure 8 in which the frequency is lowered in anticipation of lower performance demands, and then raised in anticipation of higher performance demands), Fig. 8. As explained for Element 1[a], Nowka explains, and it would have been well-understood in the art, that changing frequency entails changing the power consumption level.

69. Second, Nowka discloses varying the logic supply voltage to change the power level. EX1004, 1444, Section III.C (describing the effect of voltage scaling during Dhrystone2.1 and MPEG-4 decoding operation as summarized in Figures 5, 6), Figs. 5-6, 1444, Section V (describing the scenario depicted in Figure 8 in which the logic supply is lowered in anticipation of lower performance demands, and then raised in anticipation of higher performance demands), Fig. 8. The voltage scaling is accomplished using a “dynamic voltage architecture” that can vary the supply voltage to the power domain that includes the processor core, caches, SOC cores, and accelerators between 1V and 1.8V. EX1004, 1442. Again, changing frequency and/or voltage were well-understood in the art as techniques for power management, and are the precise examples contemplated by the ’306 patent to change the power consumption level of a power island. *See, e.g.*, EX1001, 5:31-36, 7:34-50, 7:62-8:8, Fig. 5.

70. Third, Nowka discloses clock gating on inactive registers and cores to conserve dynamic power in the logic domain. “Approximately 80% of the processor registers and 50% of the SOC core registers are functionally clock gated when they are not accessed. At a higher level, the clocks to individual functional cores can also be frozen by the clock and power management software. This is done either in response to inactivity or through a force condition by the clock and power manager.” EX1004, 1445. Nowka states that “[t]hrough voltage and frequency scaling and clock gating, the performance/watt of this design can be varied by more than a factor of four.” EX1004, 1445. It was well-known to POSITAs at the time that clock gating was an effective means of power control. EX1017 at 11 (“Sequential circuits, such as control-units, display often a large degree of idleness due to their reactive nature. Techniques based on *clock gating* and/or on decomposition have been shown to be successful in reducing their power consumption.”); EX1018 at 12 (“When considering possibly idle digital components, clock gating (or freezing) is the most common technique for power management. Namely, the clock of an idle component can be stopped during the period of idleness. Power savings are achieved in the registers (whose clock is halted) and in the combinational logic gates where signals do not propagate due to the freezing of data in registers.”). The ’306 patent also contemplates clock gating as an example “action.” EX1001, 4:47-48.

71. Fourth, Nowka discloses placing the logic domain into various “standby modes” to conserve power. Nowka discusses three “classes” of standby: Freeze, Hibernation, and Cryo modes. EX1004, 1446. These standby modes “achieve a range of standby power levels.” EX1004, 1446. In freeze mode, “the system clock is stopped and the logic supply is decreased to its minimum value of 1.0 V. The entire state of the SOC is maintained in place. In this mode, leakage power and the power of the sleep and clock manager are consumed.” EX1004, 1446. In hibernation mode “the logic supply to the processor, caches and the SOC cores is disconnected. . . . This mode eliminates the leakage component of the standby power.” EX1004, 1446. In cryo mode, the logic supply is similarly disconnected. EX1004, 1446. All three standby modes constitute an action to change the power consumption level of a power island, the logic domain. As explained above for Element 1[a], a POSITA would have understood that an action to reduce the power consumption such as standby mode would constitute an action to change the power consumption level of a power island to a target power level. Indeed, the ’306 patent also lists “low power modes” such as “sleep” and “nap” as example actions. EX1001, 7:25-27, cls. 12, 27, 48.

72. Therefore, Nowka discloses a variety of actions to change the power level of a power island. And it would have been clear and obvious to a POSITA from the above-discussed disclosures, that a determination is made by Nowka’s

system regarding which action(s) to perform under the circumstances to accomplish this power-minimizing objective. For example, Nowka explains that the “on-chip supervisor” and “system software” execute the power management actions. EX1004, 1442. The “on-chip supervisor controls the external DC/DC converter, which provides the logic supply.” EX1004, 1442. “Under software control, the supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” EX1004, 1442. In addition, Nowka discloses that the power supervisor, “in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to the control the standby power.” EX1004, 1446. Specifically, during freeze mode, “the supervisor software first sets a low operating frequency and then lowers the supply.” EX1004, 1446; *see also* 1444 (“Under software control, at a given supply voltage, the frequency of the core can be varied from the maximum frequency down to the 1/64th of the maximum. . . . The mechanisms described provide full software control over the PLL and external DC/DC.”), 1446 (“Under software control, both the voltage and the frequency of the processor can be modified, thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption. . . . This processor, under software control, can enter both a low-leakage sleep state and a state-preserving deep-sleep state to minimize standby power consumption.”).

73. A POSITA would have understood from this disclosure that the “software control” in conjunction with other aspects of Nowka’s system determines the action to change the power level of the logic domain to the target power level. Indeed, the POSITA would have appreciated that determining the appropriate power-reducing action to take is how Nowka’s software “makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications,” (EX1004, 1441). For instance, Nowka describes a scenario where the software anticipates “lower performance demands” and, responsively, *determines* that the appropriate *action* is to “modif[y] the PLL output divider value, which results in a decrease in frequency [from 266 MHz] to 66 MHz” and makes “the logic power fall[] by about 70%.” EX1004, 1444.

(d) Element 1[c]

74. Element 1[c] recites: “performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” Nowka discloses and/or renders obvious Element 1[c].

75. As discussed for Element 1[b], a POSITA would have appreciated that Nowka’s system software facilitates performing actions such as changing *frequency*, changing voltage, clock gating, or standby mode to change the power consumption

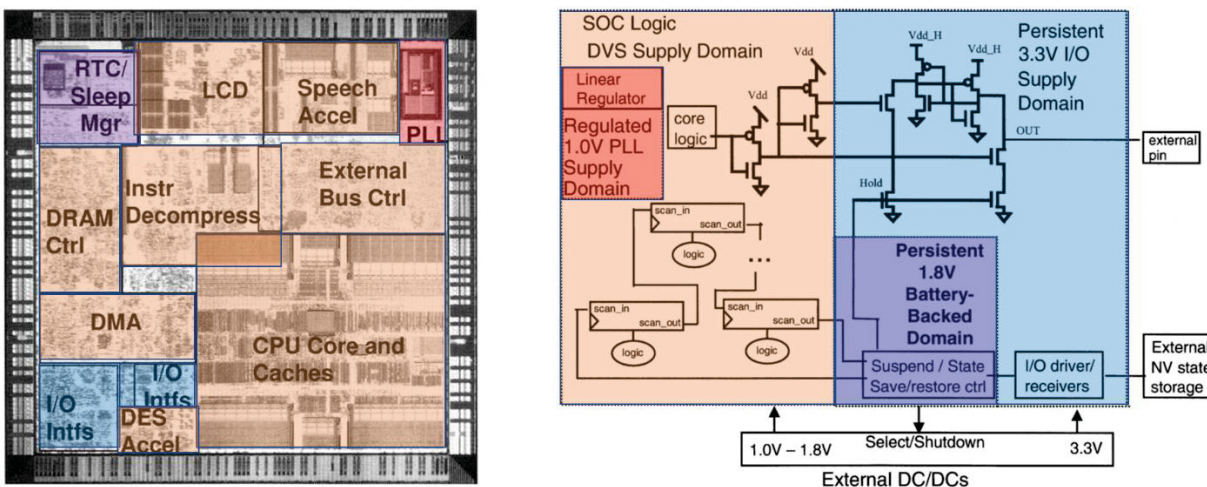
level of the logic domain and its individual cores to the target power level that minimizes power consumption while meeting application performance demands. EX1004, 1444 Section III.C (voltage scaling), 1444 Section V (*frequency* and voltage scaling), 1445 (“Active power of the SOC can be further reduced through *modification of the clock frequency* within the individual cores.”) (clock gating), 1446 (standby modes); *see supra*, ¶¶67-73. According to Nowka, “[a]djustment to the output clock *frequency* can be done on-the-fly by modifying the output clock divider through a write to a control register,” allowing “the frequency of the core [to] be varied from the maximum frequency down to 1/64th of the maximum.” EX1004, 1444. In other words, by writing to the control register, the software “set[s]” (or “selects”) a frequency.

3. Claim 2

76. Claim 2 recites: “The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit.” Nowka discloses and/or renders obvious this claim.

77. Nowka’s power islands (domains and/or individual cores) are delineated based on the physical layout on the chip. For example, below is a side-by-side comparison of Figures 2 (left) and 3 (right). Figure 2 shows a die photograph of the SOC, *i.e.* the actual physical layout, and Figure 3 schematically shows the signal and state interfaces of the “four distinct power domains” of the SOC. The

annotation on the figures demonstrates that the various functional blocks within each power island are located near other components in the same power island to optimize space usage and allow for effective signal travel.



EX1004, Figs. 2 and 3.

78. A POSITA would have understood from basic circuit design principles that power islands should be delineated based on physical proximity to minimize signal deterioration and power dissipation, for better routing of power supply and signals, and optimization of performance and power. In light of Nowka's disclosure, and basic circuit design principles understood by those in the art, it would have been obvious to a POSITA that Nowka's power islands are delineated based on geographic factors of the integrated circuit. This analysis applies equally to the four power domains (power islands) and the individual cores within the logic domain (also power islands).

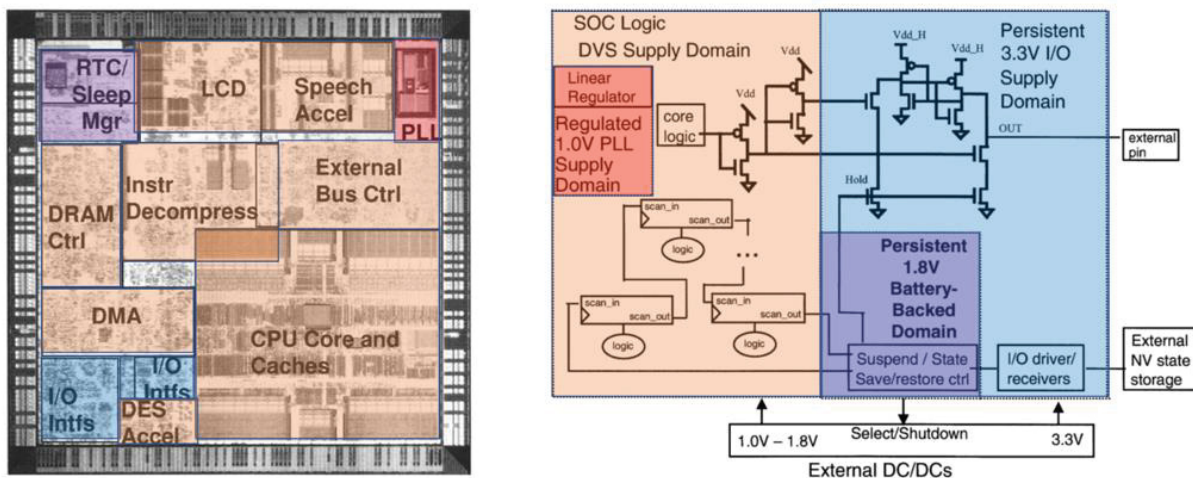
4. Claim 3

79. Claim 3 recites: “The method of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.” Nowka discloses and/or renders obvious this claim.

80. For example, the I/O drivers and receivers are in the same power domain that is powered by a persistent 3.3V supply. A POSITA would have understood that these I/O drivers and receivers receive this higher, persistent voltage because of their function (interfacing with external devices and peripherals), and therefore are grouped in one power island. Similarly, the functional circuits with dynamic power needs are grouped together in one power island, the logic domain. As for the individual cores within the logic domain, their corresponding circuitry is delineated based on the function of the core.

81. The processor core, caches, and other components which are part of this domain respond to the changing needs of the application, so dynamically adjusting the voltage for this domain allows Nowka’s SOC to balance performance and power consumption. Further, the real-time clock and the sleep management core are powered by a persistent 1.8 V battery supply, which allows the domain to retain power even when main power is off. This setup makes sense, as the real-time clock and sleep management core need to be able to keep time and allow for system wakeup, even when the rest of the system is sleeping. Finally, the PLL is supplied

by a regulated 1.0 V supply because it needs to consistently be able to operate its clock output in accordance with the dynamic frequency scaling of the system. EX1004, 1443 (“Rather than requiring the PLL to relock each time the logic supply was adjusted, we developed a low-voltage PLL whose supply is derived by a regulator off of the variable logic supply. Since the regulated voltage is relatively constant, as the supply changes, the system continues to operate over the dynamic voltage and frequency scaling ranges.”). Therefore, it would have been obvious to a POSITA that Nowka’s power islands are delineated based on functional circuitry.



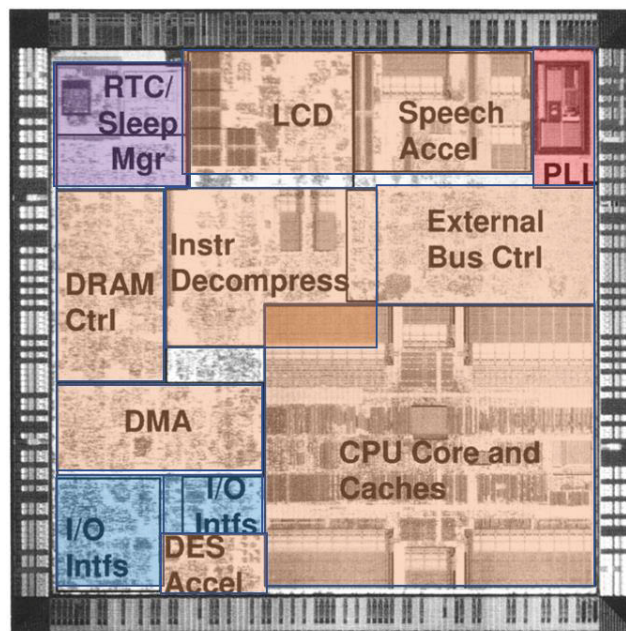
EX1004, Figs. 2, 3.

5. Claim 4

82. Claim 4 recites: “The method of claim 1 wherein the power islands comprise power sub-islands.” Nowka discloses and/or renders obvious this claim.

83. The ’306 patent states that in some embodiments, power islands comprise sub-islands to provide further specificity in controlling power in the

integrated circuit. EX1001, 3:63-66. Nowka discloses that “active power of the SOC can be further reduced through modification of the clock frequency within the individual cores.” EX1004, 1445. The individual cores (such as the CPU core, Instr Decompress, DMA controller, etc.) would be sub-islands because they are within the larger logic domain, which itself is also a power island.



EX1004, Fig. 2.

Nowka explains that the operating frequency of the cores can “be modified dynamically and individually.” EX1004, 1445. The “clocks to individual functional cores can also be frozen by the clock and power management software. This is done either in response to inactivity or through a force condition by the clock and power manager.” EX1004, 1445. In other words, the power consumption of the individual cores can be controlled independently of other cores, and changing their clock

frequency is performed to provide further specificity in controlling power in the SOC.

84. Additionally, “[d]ynamic power is saved in this design by gating off inactive latches and units.” EX1004, 1445. “Operating latches and units, which are not necessary for the execution of the application obviously wastes energy. Avoiding unnecessary switching lowers the dynamic power consumption of the device and extends battery life.” EX1004, 1445. And, “[a]pproximately 80% of the processor registers and 50% of the SOC core registers are functionally clock gated when they are not accessed.” EX1004, 1445. The latches, units, and registers are further sub-islands (at a lower level of abstraction than cores) whose power is controlled (via clock gating) for increased specificity. Therefore, a POSITA would have found it obvious that Nowka had multiple power sub-islands: the individual cores, units, registers, and latches.

6. Claim 5

85. Claim 5 recites: “The method of claim 1 wherein the power islands comprises multiple clock domains.” Nowka discloses and/or renders obvious this claim. For example, it would have been obvious to a POSITA that the power islands comprise multiple clock domains. As discussed above for claim 4, “[a]ctive power of the SOC can be further reduced through modification of the clock frequency within the individual cores.” EX1004, 1445. “Cores receive clocks whose

frequency is derived from the processor clock through clock dividers. The clock dividers are controlled by register values. The hazard-free clock dividers *allow the clocks to the cores to be modified dynamically and individually*. . . .[T]he clocks to individual functional cores can also be frozen by the clock and power management software.” EX1004, 1445. Therefore, the individual cores in Nowka can receive separate clock frequencies from clock dividers and thus comprise multiple clock domains.

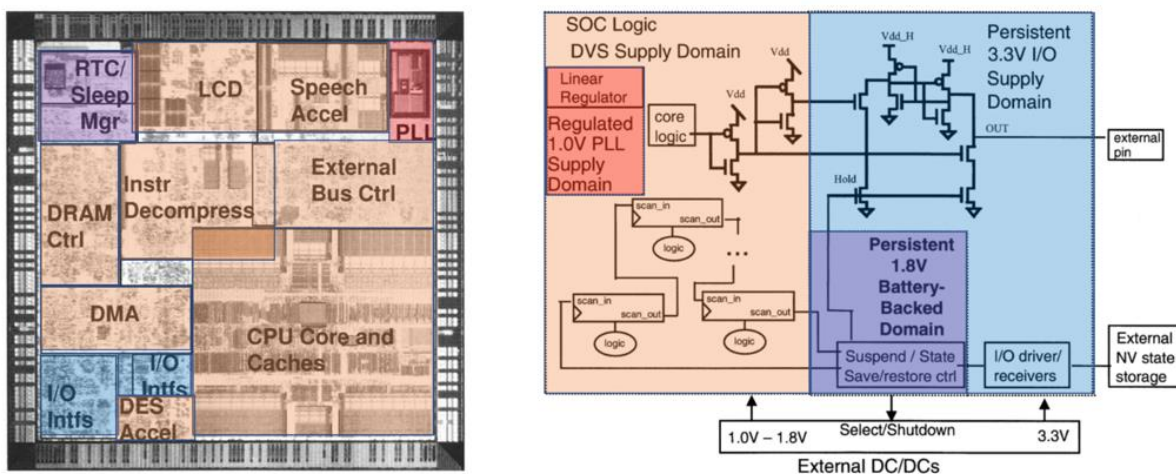
7. Claim 6

86. Claim 6 recites: “The method of claim 1 wherein another one of the actions comprises selecting a clock for the one of the power islands.” Nowka discloses and/or renders obvious claim. According to Nowka, “[t]he output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock as the processor clock source to allow for extremely low frequency operation.” EX1004, 1444. These different clocks can be selected based on the performance demands of the SOC, such as “when the performance demands of the application decrease.” EX1004, 1444. Therefore, Nowka discloses selecting a clock for a power island to change the power consumption level to the target power level.

8. Claim 7

87. Claim 7 recites: “The method of claim 1 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.” Nowka

discloses and/or renders obvious this claim. For example, Nowka discloses the use of “dynamic voltage scaling (DVS)” that can “adjust the supply voltage dynamically to meet the performance demands” of the SOC. EX1004, 1442. Specifically, Nowka teaches a logic domain whose supply can be “dynamically varied between 1 and 1.8V.” This logic domain (a power island) contains the processor core, caches, SOC cores and accelerators. EX1004, 1442.



88. Nowka discloses modifying the supply voltage for the logic domain. For example, in Figures 5 and 6, Nowka summarizes the power consumption measurements at varying levels of supply voltage to the logic domain. “Figs. 5 and 6 present the effectiveness of *voltage scaling*.” EX1004, 1445. Figure 5 shows the measured frequency and power consumption as a function of supply voltage while the SOC is running Dhrystone2.1 benchmark. EX1004, 1445. Figure 6 shows the measured throughput and power consumption as a function for supply voltage while

the SOC performs MPEG-4 decoding. EX1004, 1445. These examples show Nowka modifying a voltage for the logic domain.

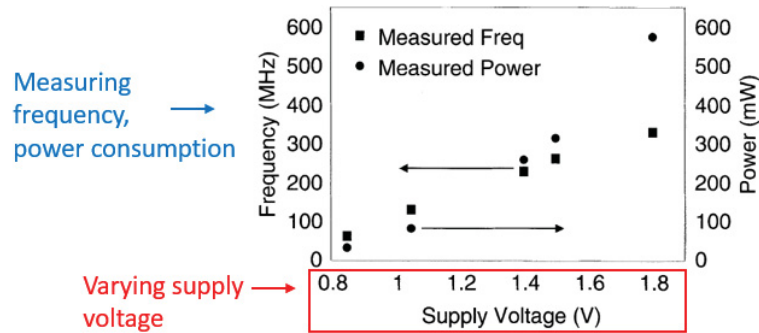


Fig. 5. Dhrystone2.1 voltage scaling measurements.

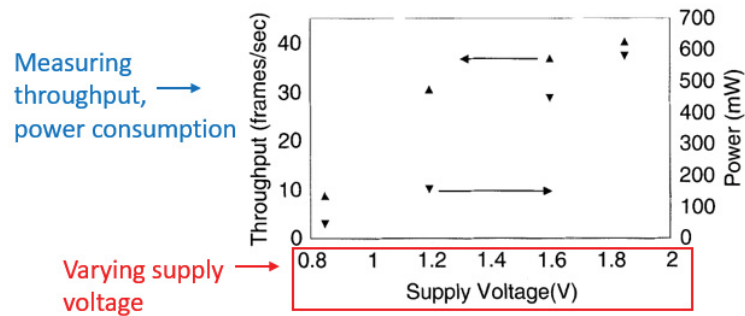


Fig. 6. MPEG-4 decode voltage scaling measurements.

EX1004, Figs. 5, 6.

89. Figure 8 presents another example of modifying a voltage for the logic domain.

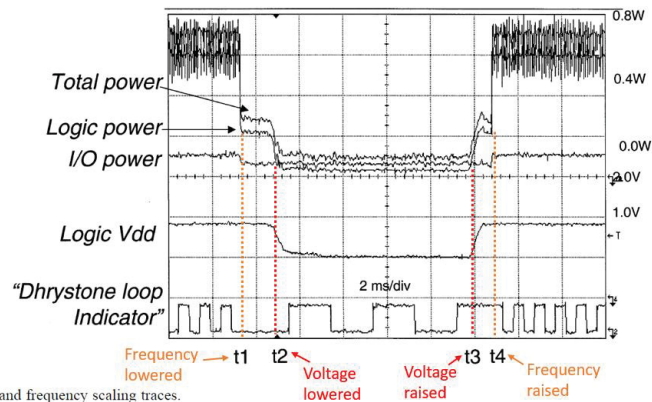


Fig. 8. Dynamic voltage and frequency scaling traces.

EX1004, Fig. 8.

As shown in Figure 8, the supply voltage is lowered at t2 in anticipation of lower performance demands, and then raised at t3 in anticipation of greater performance demands. EX1004, 1444. Therefore, Nowka amply discloses modifying a voltage for a power island.

9. Claim 8

90. Claim 8 recites: “The method of claim 7 wherein the first voltage comprises a source voltage.” Nowka discloses and/or renders obvious this claim. The ’306 patent describes the voltage labeled ‘Vdd’ as a “dynamic voltage source” that can be scaled for at least one of the power islands. EX1001, 4:51-53. Similarly, a POSITA would have understood the voltage that is varied for the logic domain in Nowka—the supply voltage—to be a source voltage because the supply voltage provides power for the power island in question. EX1004, 1443 (“Under software control, the supervisor requests changes to the *logic supply* and requests shutdown of the logic supply during hibernation.”), 1444 (“When the supply was lowered to 0.85 V the SOC consumed 33 mW at 66 MHz.”). The “supply voltage” is the voltage supplied to the SOC domains via the DC/DC converters from a voltage source. EX1004, 1443 (discussing dynamic power management in the context of “battery-powered applications” and explaining that “[a]n on-chip supervisor control the external DC/DC converter, which provides the logic power supply”).

91. For example, Figures 5 and 6 label the voltage being changed as “Supply Voltage,” while Figure 8 labels it “Logic Vdd,” similar to the “Vdd” voltage in the ’306 patent.

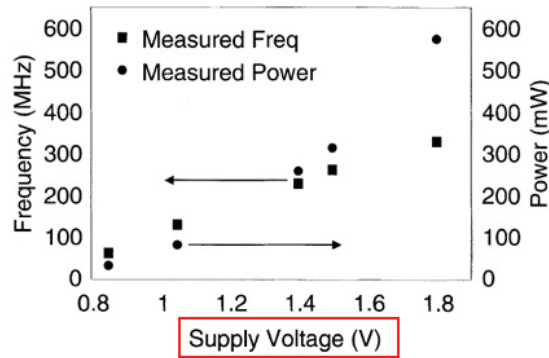


Fig. 5. Dhrystone2.1 voltage scaling measurements.

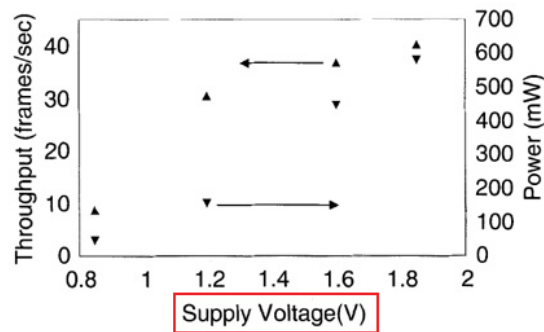
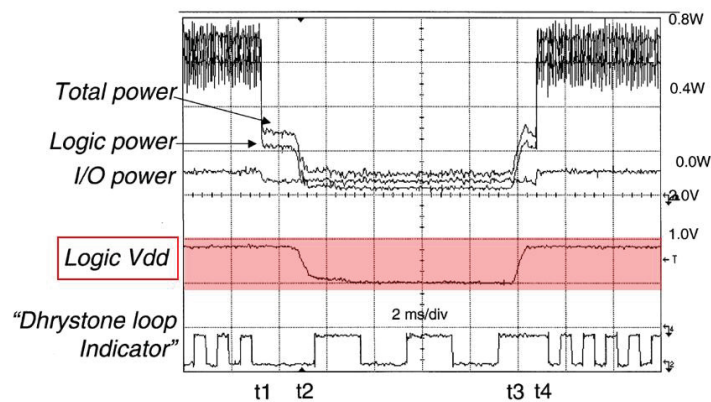


Fig. 6. MPEG-4 decode voltage scaling measurements.

EX1004, Figs. 5, 6.



EX1004, Fig. 8.

See also EX1004, 1444 (“The middle trace is the SOC logic *supply* voltage.”). A POSITA would have understood that the “supply voltage” of Nowka corresponds to the “source voltage” of the ’306 patent because the supply voltage provides power for the power island in question. To a POSITA, “supply voltage” and “source voltage” are different ways of referring to the same thing.

10. Claim 10

92. Claim 10 recites: “The method of claim 1 wherein another one of the actions comprises powering on the one of the power islands.” Nowka discloses and/or renders obvious this claim. For example, Nowka discloses low-power standby modes called “hibernation” and “cryo” where “the logic supply to the processor, caches and the SOC core is disconnected.” EX1004, 1446; *see also* 1445 (“the clocks to individual functional cores can also be frozen”). This is advantageous for power savings because disconnecting the logic supply “eliminates the leakage component of the standby power” in a power domain. EX1004, 1446. When the logic supply is shut down, the logic domain is turned off and not operating. EX1004, 1446. When hibernation or cryo mode is exited to “reactivat[e] the system” upon a “wakeup event,” the SOC “restores the [logic] supply,” which means that it powers on the logic domain for operation. EX1004, 1446. Therefore, Nowka discloses powering on a power island.

11. Claim 11

93. Claim 11 recites: “The method of claim 1 wherein another one of the actions comprises powering off the one of the power islands.” Nowka discloses and/or renders obvious this claim. As discussed above for claim 10, Nowka discloses hibernation and “cryo” modes where “the logic supply to the processor, caches and the SOC core is *disconnected*” which “eliminates the leakage component of the standby power” in a power domain. EX1004, 1446; *see also* 1445 (“the clocks to individual functional cores can also be frozen”). When entering hibernation mode, “the supervisor requests *shutdown* of the logic supply,” which powers off the power domain. EX1004, 1442. Similarly, when entering “cryo” mode, “the suspend controller . . . removes logic power and waits for a wakeup event.” EX1004, 1446. Because the supply voltage is what provides power to the power domain, shutting it down or disconnecting it connotes “powering off the one of the power islands,” as described and claimed in the ’306 patent. Such a technique was also widely known in the art. *See* EX1018 at 1 (“An example of a simple policy, ubiquitously used for laptops and palmtops, is the timeout policy, which shuts down a component after a fixed inactivity time[.]”).

12. Claim 12

94. Claim 12 recites: “The method of claim 1 wherein another one of the comprises changing the one of the power islands to a sleep mode.” Nowka discloses

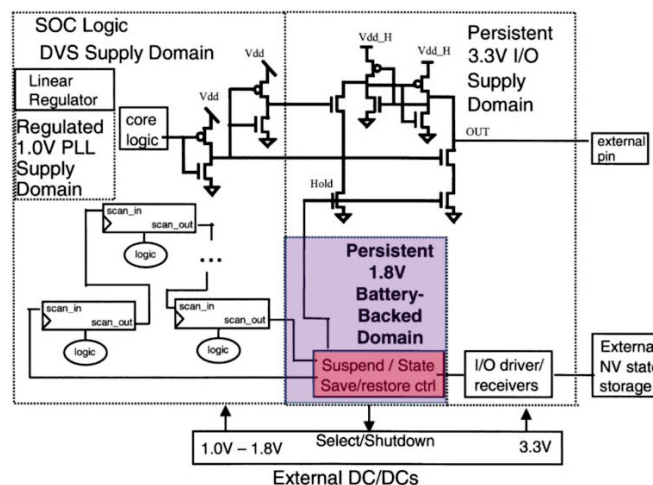
and/or renders obvious this claim. The '306 patent discloses “low power modes such as sleep, nap, and full power down.” EX1001, 7:26-27. Similarly, Nowka describes low power modes such as freeze, hibernation, and cryo modes as part of “standby power management.” These different standby modes “achieve a range of standby power levels.” EX1004, 1446. In freeze mode, “the system clock is stopped and the logic supply is decreased to its minimum value of 1.0 V. The entire state of the SOC is maintained in place. In this mode, leakage power and the power of the sleep and clock manager are consumed.” EX1004, 1446. In hibernation mode “the logic supply to the processor, caches and the SOC cores is disconnected. . . . This mode eliminates the leakage component of the standby power.” EX1004, 1446. In cryo mode, “the state of latches and register arrays in the processor core and SOC cores is transferred to nonvolatile storage prior to disconnecting the logic supply.” EX1004, 1446. A POSITA would have understood each one of these modes to satisfy the “sleep mode” of claim 12. Such low-power modes were common in the art at the time, and a POSITA would have understood that Nowka’s sleep modes comport with the description in the '306 patent. *See* EX1017, 194-195 (describing various pre-defined or customizable sleep states for components in the ACPI model).

13. Claim 14

95. Claim 14 recites: “The method of claim 1 further comprising saving a state of components within the one of the power islands.” Nowka discloses and/or

renders obvious this claim. In cryo mode, “the state of latches and register arrays in the processor core and SOC cores *is transferred to nonvolatile storage* prior to disconnecting the logic supply.” EX1004, 1446. “The suspend controller stops the clocks, freezes the I/O drivers, *scans the register state out* through the IIC interface to nonvolatile storage, removes logic power[.]” EX1004, 1446. This way, “the entire register state of the SOC can be restored prior to reactivating the system.” EX1004, 1446. Nowka thus discloses and renders obvious saving the state of the latches and register arrays, which are components in the logic domain, prior to entering cryo mode.

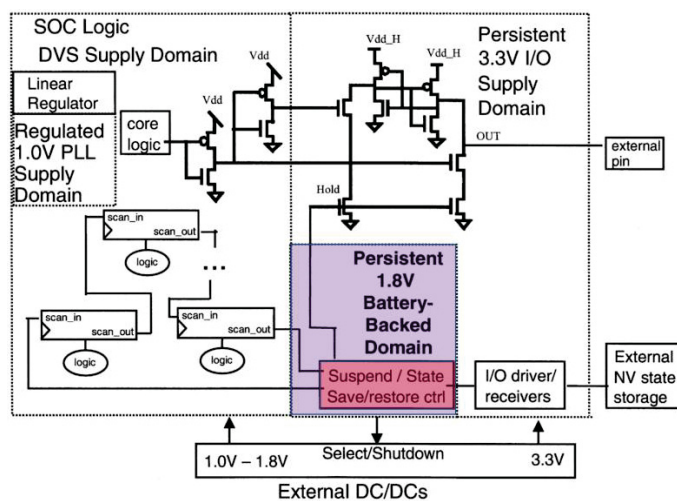
96. Figure 3 of Nowka (below) shows a block labeled “Suspend/State Save/restore ctrl” (in red) that is used to suspend, state save, and restore of the state of registers within the power island of the variable voltage power domain. EX1004, 1446, Fig. 3. A POSITA would have understood that this control block facilitates the saving of the state of logic domain components prior to entering cryo mode.



EX1004, Fig. 3.

14. Claim 15

97. Claim 15 recites: “The method of claim 1 further comprising restoring a state of components within the one of the power islands.” Nowka discloses and/or renders obvious this claim. For example, Nowka discloses that after the system has entered cryo mode, the suspend controller “waits for a wakeup event at which time it restores the supply, *restores the state* and restarts the clocks.” EX1004, 1446. “Restoring the state” refers to restoring the state of the latches and register arrays in the processor core and SOC core, which are components within the logic domain, that had been saved prior to entering cryo mode. Further, Nowka discloses that with cryo mode “the *entire register state of the SOC can be restored* prior to reactivating the system.” EX1004, 1446. Nowka thus discloses restoring a state of components of a power island. In addition, a POSITA would have understood that the control block labeled “Suspend/State Save/restore ctrl” facilitates the restoring of the state of logic domain components when exiting cryo mode and reactivating the system.



EX1004, Fig. 3.

15. Claim 16

(a) Element 16[p]

98. Element 16[p] recites: “A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising.” Nowka discloses and/or renders obvious Element 16[p] for at least the reasons I discussed above with respect to Elements 1[p]-1[a].

99. Nowka further discloses and/or renders obvious the claimed “system for an integrated circuit” by describing a “PowerPC system-on-a-chip (SOC)” that is “intended to address the high-content battery-powered market segment. This segment includes information appliances such as Web pads, advanced PDAs, cell phones and small form-factor PCs.” EX1004, 1441. Nowka’s SOC platform is fabricated via a “bulk CMOS process,” a well-known technology for constructing integrated circuits. EX1004, 1441. Accordingly, a POSITA would have recognized Nowka’s “5.8 million transistor, 36mm² PowerPC processor,” as a “system for an integrated circuit.” EX1004, 1446, Figs. 1-2.

(b) Element 16[a]

100. Element 16[a] recites: “power control circuitry configured to control power for one of the power islands.” Nowka discloses and/or renders obvious Element 16[a] for at least the reasons I discussed above with respect to Elements 1[p]-1[a]. Nowka additionally discloses and/or renders obvious the claimed “power

control circuitry.” For example, Nowka explains that the DC/DC converter (shown in Figure 3) “provid[ing] the logic supply” is power control circuitry to control power for the logic domain power island(s). EX1004, 1442. The PLL controlling the clock frequency is also part of the power control circuitry (shown in Figures 1, 7). EX1004, 1444 (“Finally, anticipating an increase in demand, the logic supply is raised to 1.8 V . . . and power management software *raises the frequency via a write to the PLL control register* at times t3 and t4, respectively. The mechanisms described provide full software control over the PLL and external DC/DC.”).

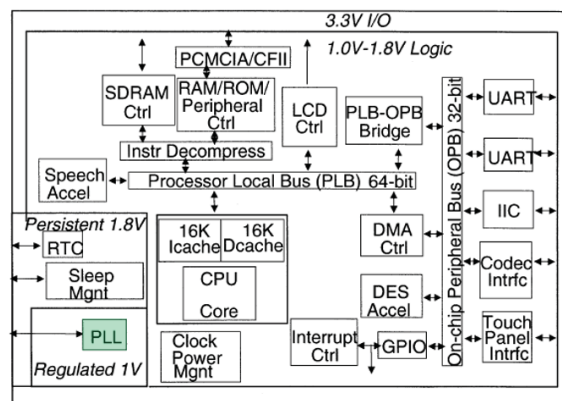
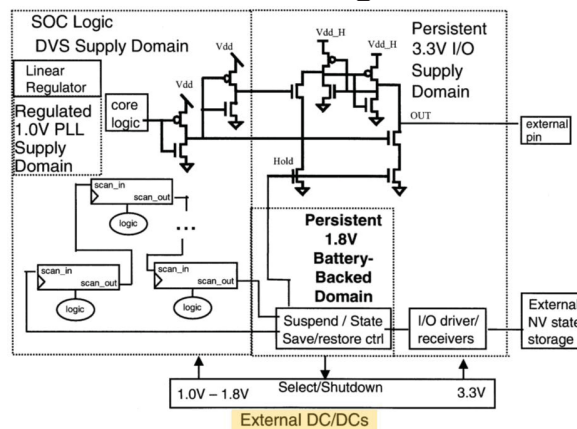


Fig. 1. PowerPC SOC structure.

EX1004, Fig. 1.



EX1004, Fig. 3.

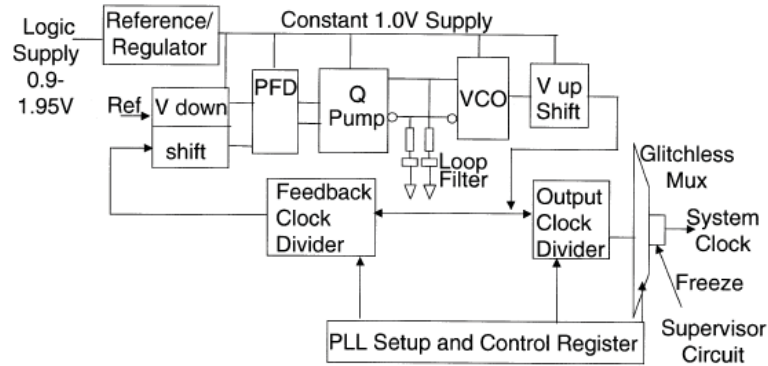


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

(c) **Element 16[b]**

101. Element 16[b] recites: “a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” Nowka discloses and/or renders obvious Element 16[b] for at least the reasons I discussed above with respect to Elements 1[a]-1[c].

102. Further, Nowka discloses and/or renders obvious the claimed “power manager” by describing an “on-chip supervisor” and “system software.” Based on instructions from the software, the “on-chip supervisor controls the external DC/DC converter, which provides the logic supply.” EX1004, 1442, 1444 (“clock and

power management software”). The supervisor can be seen in the “Clock Power Mgmt” block in Figure 1.

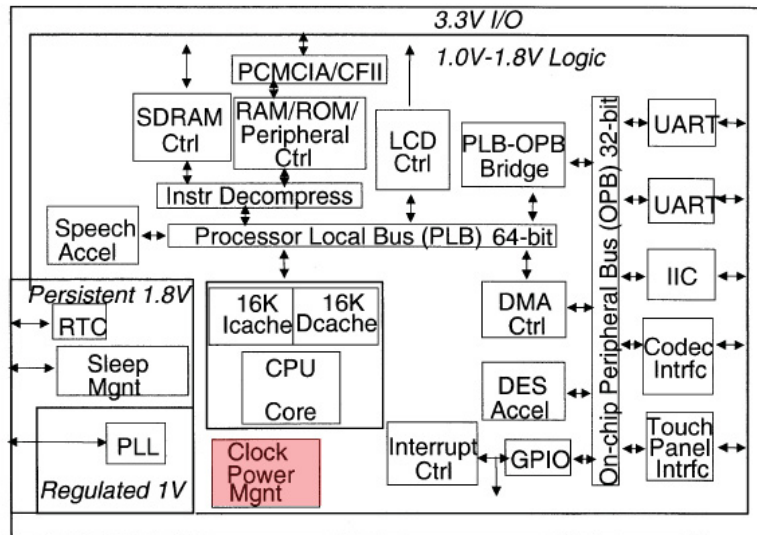


Fig. 1. PowerPC SOC structure.

EX1004, Fig. 1.

103. In tandem with the system software, the supervisor “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” EX1004, 1442. In addition, Nowka discloses that the power supervisor, “in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to the control the standby power.” EX1004, 1446. Specifically, during freeze mode, “the supervisor software first sets a low operating frequency and then lowers the supply.” EX1004, 1446.

104. Finally, Nowka’s “power manager” also includes the PLL (which controls the frequency) and the external DC/DC (which controls the supply voltage), which work with the supervisor to execute frequency and voltage scaling. “An on-

chip supervisor controls the external DC/DC converter, which provides the logic supply.” EX1004, 1442. “[P]ower management software raises the frequency via a write to the PLL control register at times t3 and t4, respectively. The mechanisms described provide full software control over the PLL and external DC/DC.” EX1004, 1444. A POSITA would also have understood that Nowka’s SOC has additional power circuitry, such as “clock dividers [] controlled by register values,” which enable “unit and register level functional clock gating.” EX1004, 1442, 1445.

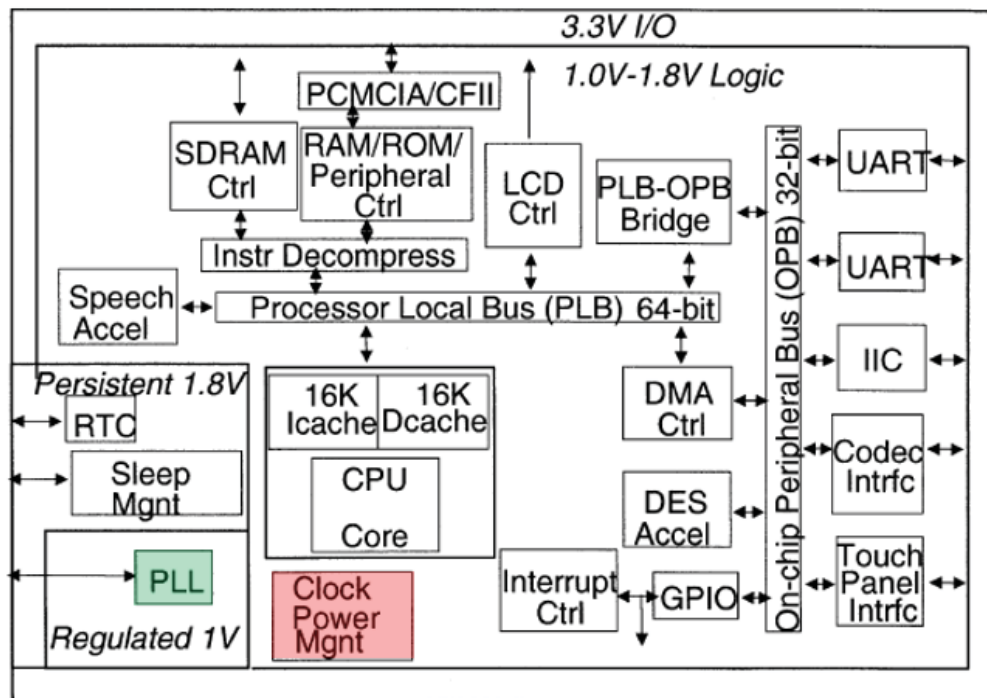
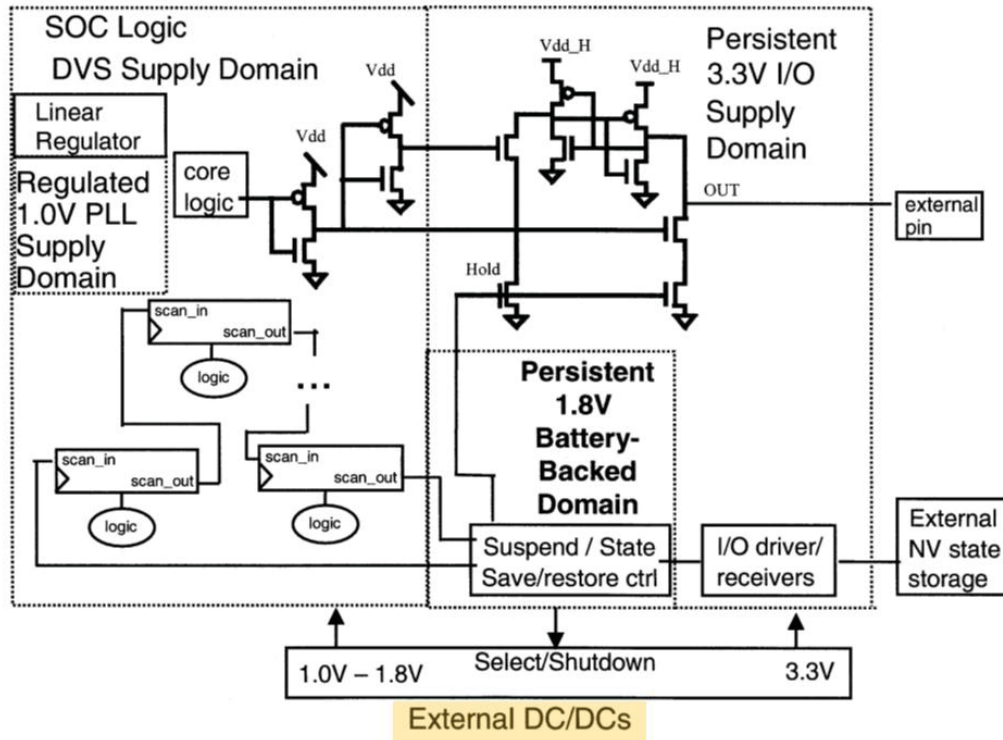


Fig. 1. PowerPC SOC structure.

EX1004, Fig. 1.



EX1004, Fig. 3.

16. Claim 17

105. Claim 17 recites: “The system of claim 16 wherein the power islands are delineated based on geographic factors of the integrated circuit.” Nowka discloses and/or renders obvious claim 17 for at least the reasons discussed above with respect to claims 2 and 16, which I incorporate herein.

17. Claim 18

106. Claim 18 recites: “The system of claim 16 wherein the power islands are delineated based on functional circuitry of the integrated circuit.” Nowka discloses and/or renders obvious claim 18 for at least the reasons discussed above with respect to claims 3 and 16, which I incorporate herein.

18. Claim 19

107. Claim 19 recites: “The system of claim 16 wherein the power islands comprise power sub-islands.” Nowka discloses and/or renders obvious claim 19 for at least the reasons discussed above with respect to claims 4 and 16, which I incorporate herein.

19. Claim 20

108. Claim 20 recites: “The system of claim 16 wherein the power islands comprise multiple clock domains.” Nowka discloses and/or renders obvious claim 20 for at least the reasons discussed above with respect to claims 5 and 16, which I incorporate herein.

20. Claim 21

109. Claim 21 recites: “The system of claim 16 wherein another one of the actions comprises selecting a clock for the one of the power islands.” Nowka discloses and/or renders obvious claim 21 for at least the reasons discussed above with respect to claims 6 and 16, which I incorporate herein.

21. Claim 22

110. Claim 22 recites: “The system of claim 16 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.” Nowka discloses and/or renders obvious claim 22 for at least the reasons discussed above with respect to claims 7 and 16, which I incorporate herein.

22. Claim 23

111. Claim 23 recites: “The system of claim 22 wherein the first voltage comprises a source voltage.” Nowka discloses and/or renders obvious claim 23 for at least the reasons discussed above with respect to claims 8 and 16, which I incorporate herein.

23. Claim 25

112. Claim 25 recites: “The system of claim 16 wherein another one of the actions comprises powering on the one of the power islands.” Nowka discloses and/or renders obvious claim 23 for at least the reasons discussed above with respect to claims 10 and 16, which I incorporate herein.

24. Claim 26

113. Claim 26 recites: “The system of claim 16 wherein another one of the actions comprises powering off the one of the power islands.” Nowka provides claim 26 for at least the reasons discussed above with respect to claims 11 and 16, which I incorporate herein.

25. Claim 27

114. Claim 27 recites: “The system of claim 16 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.” Nowka discloses and/or renders obvious claim 26 for at least the reasons discussed above with respect to claims 12 and 16, which I incorporate herein.

26. Claim 29

115. Claim 29 recites: “The system of claim 16 wherein the power manager is configured to save a state of components within the one of the power islands.” Nowka discloses and/or renders obvious claim 26 for at least the reasons discussed above with respect to claims 14 and 16, which I incorporate herein.

27. Claim 30

116. Claim 30 recites: “The system of claim 16 wherein the power manager is configured to restore a state of components within the one of the power islands.” Nowka discloses and/or renders obvious claim 26 for at least the reasons discussed above with respect to claims 15 and 16, which I incorporate herein.

28. Claim 31

117. Claim 31 recites: “The system of claim 16 further comprising a bus coupled to the power manager and the power islands.” Nowka discloses and/or renders obvious this claim. Indeed, busses were the dominant form of interconnect technology for transmitting signals to, from, and through integrated circuits at the time of the Critical Date. *See, e.g.*, EX1017 at 184 (“Busses are special devices that link several hardware resources (belonging to any of the classes described above) to the PC board.”). Using a known and ubiquitous technology like a bus to connect the known elements of Nowka’s SOC would have been exceedingly obvious to a POSITA. For example, a POSITA would have understood that the “power manager” in Nowka, which includes the on-chip power supervisor (*see supra* Element 16[b]),

would have been communicatively coupled to some form of parallel or serial bus to facilitate its functionality of “respon[ding] to software commands and timeout and interrupt events” and “manag[ing] the clocks, internal state and external power supply,” (EX1004, 1446). Stated another way, it would have been apparent or obvious to a POSITA in the context of an SOC like Nowka’s, that the power manager would utilize bus to obtain information and issue commands/instructions.

118. In addition, Nowka’s Figure 1 shows a “Processor Local Bus (PLB)” and “On-chip Peripheral Bus (OPB)” connecting various components in the logic domain (“power island[s],” per Elements 1[p]-1[a] and 16[p]-16[a]).

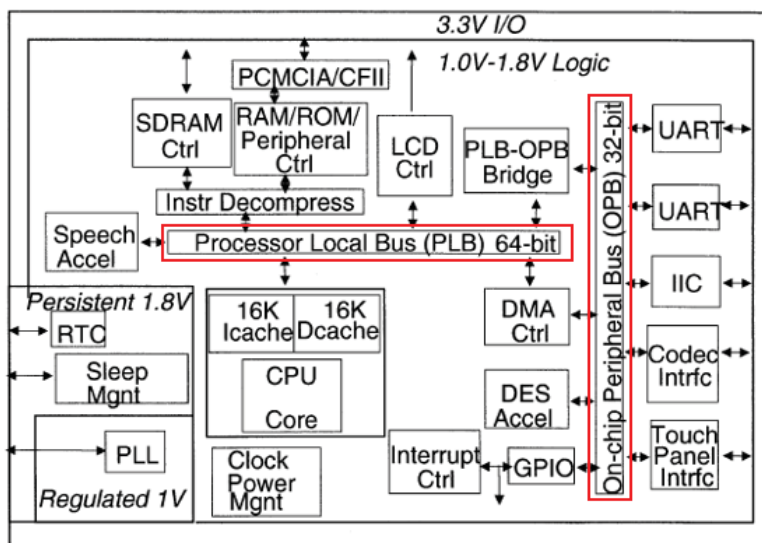


Fig. 1. PowerPC SOC structure.

EX1004, Fig. 1.

119. The presence of a bus is further confirmed and/or rendered obvious by Nowka’s disclosure that “the SOC uses IBM’s Core-Connect [1] technology to integrate a rich set of memory and I/O devices.” EX1004, 1441. The “Core-Connect

technology allows integration of semicustom synthesized cores and custom hard-cores in an SOC.” EX1004, 1445. The “Core-Connect” technology referenced by Nowka is IBM’s CoreConnect Bus Architecture, which describes a bus architecture. EX1004, 1446; EX1023; EX1005, ¶¶32-36. The IBM CoreConnect Bus Architecture White Paper, located in the link listed on Nowka’s reference [1], shows the “Reset/Clock Control/Power Mgmt” block connected to the various SOC components through a bus system. EX1023, Fig. 1. Therefore, it would have been obvious to a POSITA that Nowka’s system would comprise a bus coupled to the power manager and the power islands.

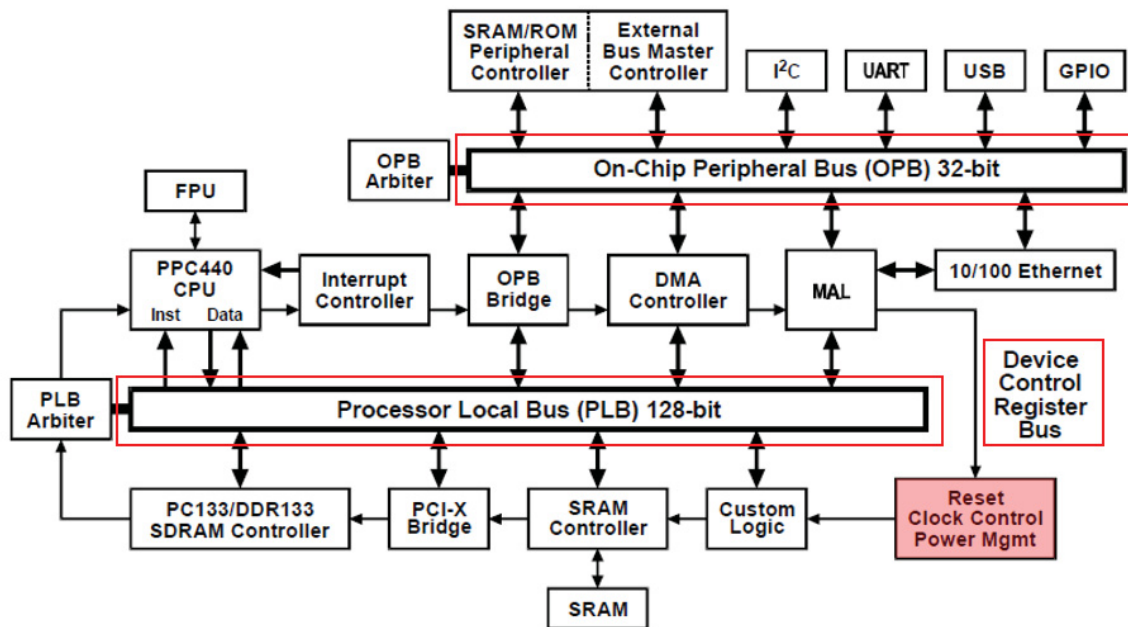


Figure 1: CoreConnect Based System-On-a-Chip.

EX1023, Fig. 1.

29. Claim 32

120. Claim 32 recites: “The system of claim 16 wherein the power manager comprises a master manager configured to control power of the integrated circuit.” Nowka discloses and/or renders obvious this claim.

121. To start, the '306 patent explains that the master manager is broadly “any circuitry configured to control the ‘global’ power behavior of the entire integrated circuit.” EX1001, 5:47-48, Fig. 2. It would have been obvious to a POSITA that Nowka’s “on-chip supervisor” acts as a master manager because it oversees the global power behavior of the entire integrated circuit. For example, Nowka discloses that the “on-chip supervisor controls the external DC/DC converter, which provides the logic supply.” EX1004, 1442.

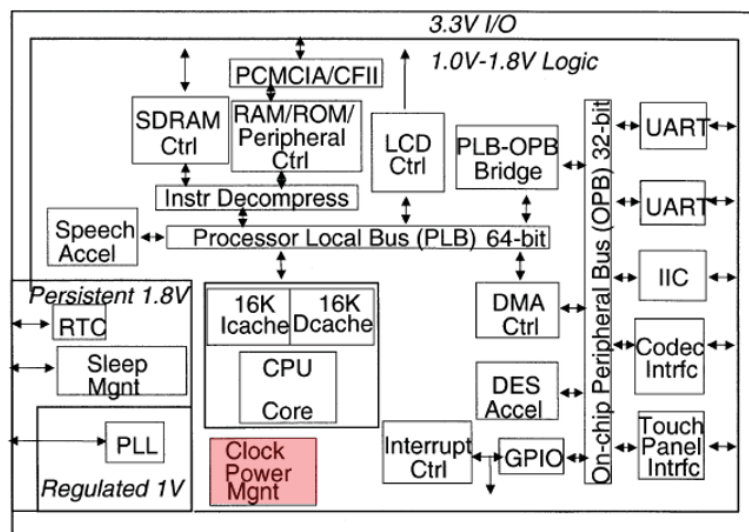


Fig. 1. PowerPC SOC structure.

EX1004, Fig. 1.

In conjunction with the system software, “the supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” EX1004, 1442. In addition, Nowka discloses that the power supervisor, “in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to the control the standby power.” EX1004, 1446. It would have been obvious to a POSITA that an on-chip supervisor that sets the voltage and shuts down the supply for a power island, and manages the system clocks, internal state and external power supply to control the standby is acting as a master manager. Similarly, the “system software” that controls this on-chip supervisor would have also been understood by the POSITA to act as a master manager, as it is equally responsible for controlling the global power behavior of the entire SOC. EX1004, 1442, 1444-46.

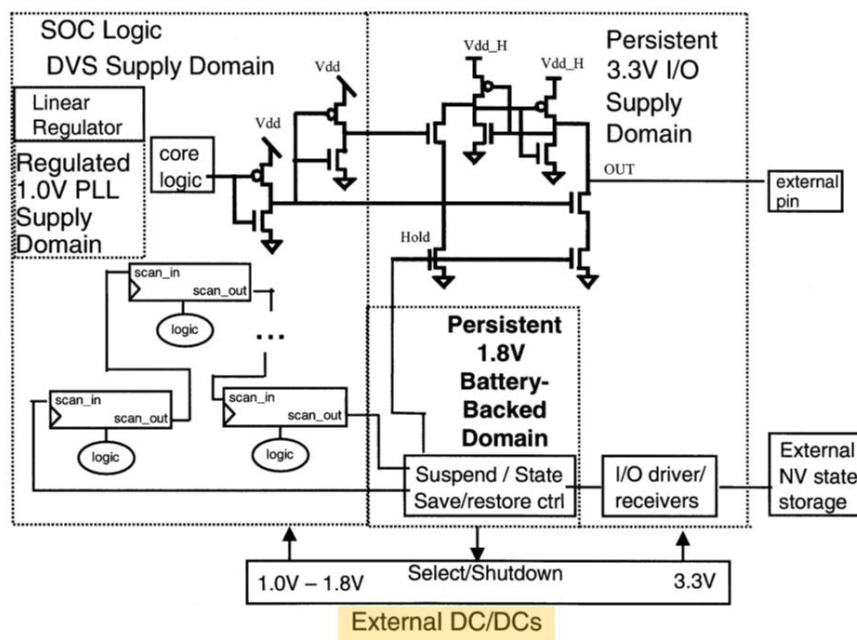
30. Claim 33

122. Claim 33 recites: “The system of claim 16 wherein the power manager comprises a slave manager configured to control power of the one of the power islands.” Nowka discloses and/or renders obvious this claim.

123. As described in the '306 patent, a slave manager is broadly “any circuitry configured to control power within a power island [] in the integrated circuit.” EX1001, 6:11-12, Figs. 2, 4, 12. Notably, the '306 patent does not

foreclose the possibility of a single component serving as both a master manager and a slave manager, depending on the context and circumstances.

124. There are multiple examples of a “slave manager” in Nowka. First, it would have been apparent and/or obvious to a POSITA that the PLL (which controls the frequency) and the external DC/DC (which controls the supply voltage) act as “slave managers” because this circuitry controls the power within the logic domain. EX1004, 1442 (“An on-chip supervisor controls the *external DC/DC converter*, which provides the logic supply.”), 1444 (“Finally, anticipating an increase in demand, the logic supply is raised to 1.8 V without interrupting execution and the clock and power management software raises the frequency *via a write to the PLL control register* at times t3 and t4, respectively.”), Fig. 3.



EX1004, Fig. 3.

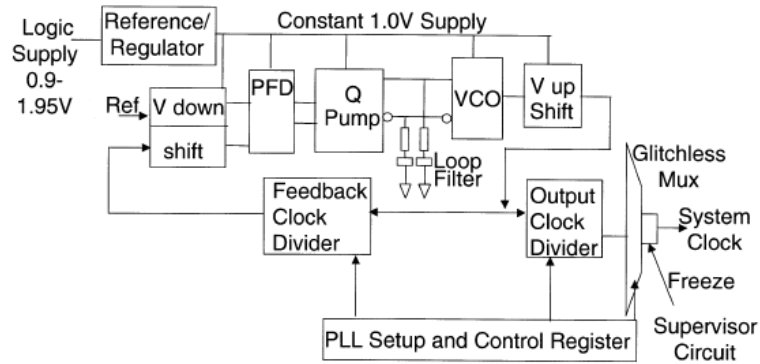


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

125. Second, Nowka discloses that “[a]ctive power of the SOC can be further reduced through modification of the clock frequency within the individual cores.” EX1004, 1445. The operating frequency of the individual cores can be modified using “clock dividers...controlled by register values.” This allows “the clocks to the cores to be modified dynamically and individually.” EX1004, 1445. The register values that control the clock dividers are changed “either in response to inactivity or through a force condition by the clock and power manager.” EX1004, 1445. A POSITA would have understood that the clock dividers and the relevant registers act as a “slave manager” that, for example, control power consumption of the individual cores of the logic domain in response to “a force condition by the clock and power manager.” EX1004, 1445.

126. Third, to the extent the “system software” is considered a master manager, per may prior analysis for claim 32, the on-chip supervisor it controls would likewise be recognized by the POSITA as a relative slave manager. That is,

the supervisor acts in a slave capacity, following the instructions of the system software, to control power of the logic domain (“power island[s]”).

31. Claim 34

127. Claim 34 recites: “The system of claim 16 wherein the power control circuitry includes clock multiplexing circuitry.” Nowka discloses and/or renders obvious this claim. For example, Nowka discloses “a glitchless output multiplexor” that is part of the phase locked loop (PLL) providing the operating frequency for the power domains. “The output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock.” EX1004, 1444. Figure 7 shows the “Glitchless Mux” integrated into the PLL that “allows adjustment of the frequency across a range of 1/2 to 1/128th of the VCO frequency.” EX1004, 1444. Consistent with my analysis above at Element 16[a], this multiplexor of the PLL is part of the power control circuitry which controls power (in this case, by controlling the clock frequency) of the logic domain.

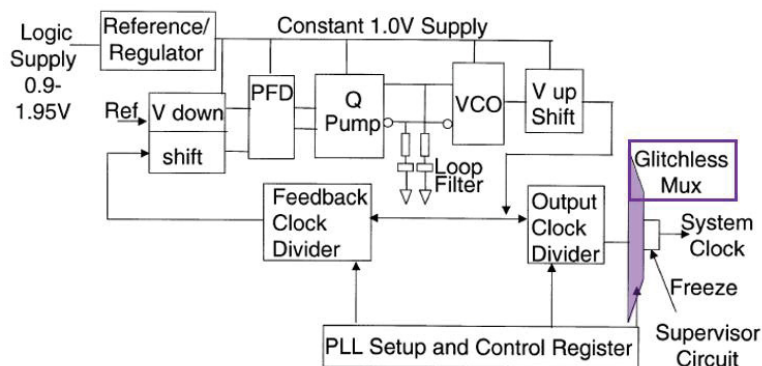


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

32. Claim 36

128. Claim 36 recites: “The system of claim 16 wherein the power control circuitry includes level shifting circuitry.” Nowka discloses and/or renders obvious this claim. For example, Nowka discloses that “because the logic supply is not persistent, signals passing from the logic domain to a persistent domain are latched by *level shifters*.” EX1004, 1442-1443. In addition, “to account for differences between the regulated voltage and logic voltage, the PLL integrates *level shifting* into the reference clock, feedback clock and output clock paths.” EX1004, 1444. Therefore, it would have been apparent and/or obvious to a POSITA that Nowka’s power control circuitry includes level shifting circuitry.

33. Claim 37

(a) Element 37[p]

129. Element 37[p] recites: “A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising.” Nowka discloses and/or renders obvious Element 37[p] for at least the reasons discussed above with respect to Element 1[p], which I incorporate herein. Further, Nowka discloses and/or renders obvious “a software product” in the form of “system software” that “requests changes to the logic supply and requests shutdown of the logic supply during hibernation,” (EX1004, 1442), “can lower the operating frequency,” (EX1004, 1444), exert “control over the PLL and external DC/DC,” (EX1004, 1444), modifies “both the voltage and the frequency of the

processor . . . thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption,” (EX1004, 1446), and causes the processor to “enter both a low-leakage sleep state and a state-preserving deep-sleep state to minimize standby power consumption.” EX1004, 1446.

(b) Element 37[a]

130. Element 37[a] recites: “power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” Nowka discloses and/or renders obvious Element 37[a] for at least the reasons discussed above with respect to Elements 1[a]-1[c] and 37[p], which I incorporate herein.

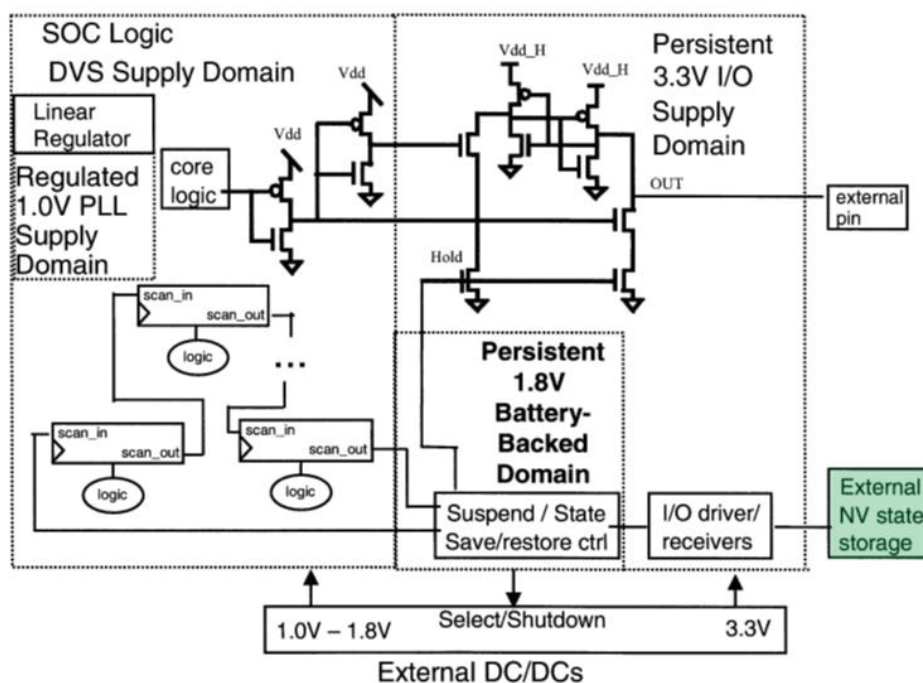
131. Nowka additionally discloses and/or renders obvious “power management software.” As explained for 37[p], Nowka’s system software executes a number of power management functions. For example, Nowka states that “***[u]nder software control***, the supervisor requests changes to the logic supply and requests

shutdown of the logic supply during hibernation.” EX1004, 1442. As for changing frequency, “the system software can lower the operating frequency” when performance demands decrease. EX1004, 1444. “*Under software control*, at a given supply voltage, the frequency of the core can be varied from the maximum frequency down to the 1/64th of the maximum.” EX1004, 1444. “The mechanisms described provide full *software control* over the PLL and external DC/DC.” EX1004, 1444. The “*power management software* modifies the PLL output divider value, which results in a decrease in frequency” and “raises the frequency via a write to the PLL control register.” EX1004, 1444. “*Under software control*, both the voltage and the frequency of the processor can be modified, thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption.” EX1004, 1446. Furthermore, Nowka’s processor, “*under software control*, can enter both a low-leakage sleep state and a state-preserving deep-sleep state to minimize standby power consumption.” EX1004, 1446. Therefore, Nowka discloses “power management software,” which directs the power management scheme.

(c) **Element 37[b]**

132. Element 37[b] recites: “a software storage medium operational to store the power management software.” Nowka discloses and/or renders obvious Element 37[b]. As discussed above at Element 37[a], Nowka discloses “power management

software” and “system software” that “provide full software control” over the operating conditions of the SOC. Further, Nowka discloses applications for its SOC including “Web pads, advanced PDAs, cell phones and small form-factor PCs.” EX1004, 1441. A POSITA would have understood that Nowka’s system includes a software storage medium for storing the power management software, such as an on-chip cache or an off-chip non-volatile memory (as shown in Figure 3).



EX1004, Fig. 3.

133. Nowka’s setup, which was common by the time of the Critical Date, is similar to that disclosed in the ’306 patent, which shows an “embedded firmware stack” connected to the integrated circuit and housing the power management software layers. *See* EX1001, 4:58-59, Fig. 2.

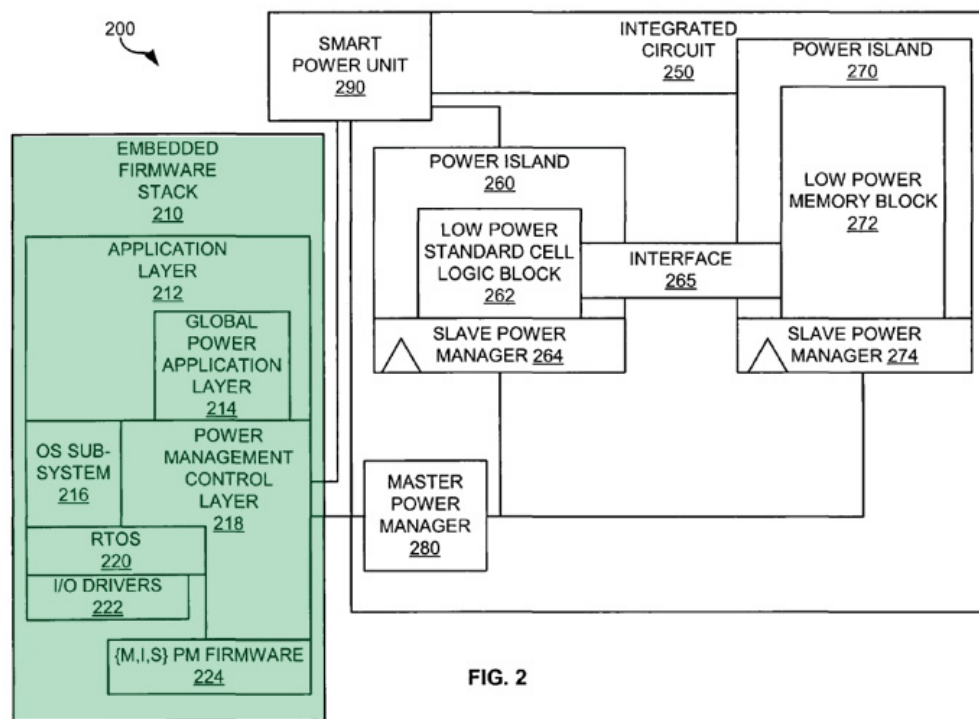


FIG. 2

EX1001, Fig. 2.

34. Claim 38

134. Claim 38 recites: “The software product of claim 37 wherein the power islands are delineated based on geographic factors of the integrated circuit.” Nowka provides claim 38 for at least the reasons discussed above with respect to claims 2 and 37, which I incorporate herein.

35. Claim 39

135. Claim 39 recites: “The software product of claim 37 wherein the power islands are delineated based on functional circuitry of the integrated circuit.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 3 and 37, which I incorporate herein.

36. Claim 40

136. Claim 40 recites: “The software product of claim 37 wherein the power islands comprise power sub-islands.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 4 and 37, which I incorporate herein.

37. Claim 41

137. Claim 41 recites: “The software product of claim 37 wherein the power islands comprise multiple clock domains.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 5 and 37, which I incorporate herein.

38. Claim 42

138. Claim 42 recites: “The software product of claim 37 wherein another one of the actions comprises selecting a clock for the one of the power islands.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 6 and 37, which I incorporate herein.

39. Claim 43

139. Claim 43 recites: “The software product of claim 37 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 7 and 37, which I incorporate herein.

40. Claim 44

140. Claim 44 recites: “The software product of claim 43 wherein the first voltage comprises a source voltage.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 8 and 37, which I incorporate herein.

41. Claim 46

141. Claim 46 recites: “The software product of claim 37 wherein another one of the actions comprises powering on the one of the power islands.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 10 and 37, which I incorporate herein.

42. Claim 47

142. Claim 47 recites: “The software product of claim 37 wherein another one of the actions comprises powering off the one of the power islands.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 11 and 37, which I incorporate herein.

43. Claim 48

143. Claim 48 recites: “The software product of claim 37 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 12 and 37, which I incorporate herein.

44. Claim 50

144. Claim 50 recites: “The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within the one of the power islands.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 14 and 37, which I incorporate herein.

45. Claim 51

145. Claim 51 recites: “The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within the one of the power islands.” Nowka discloses and/or renders obvious this claim for at least the reasons discussed above with respect to claims 15 and 37, which I incorporate herein.

B. Analysis of Nowka in view of Borkar with Respect to Claims 9, 13, 24, 28, 45, and 49

146. For the reasons articulated in detail below, and based on my review of the '306 patent and the Nowka and Borkar references, I am confident that a POSITA would have readily understood that Nowka in view of Borkar renders obvious claims 9, 13, 24, 28, 45, and 49.

1. Overview of Borkar

147. Borkar is titled “Software control of transistor body bias in controlling chip parameters.” EX1006, Title. Borkar relates to controlling various parameters,

such as performance, power consumption, and temperature in integrated circuits. EX1006, 2:2-3. The goals of the disclosed techniques include “keeping power consumption below a particular level” and “obtaining the highest performance while not exceeding a particular power consumption level.” EX1006, 12:10-15.

148. Borkar discusses controlling these parameters by “changing body bias signals applied to transistors” and changing the clock frequency and supply voltage of the circuit. EX1006, 2:49-54, Figs. 1-3, 5, 7, 9. Borkar explains that body bias, which “refers to the relationship between the voltage of the source of the field effect transistor (FET transistor) and voltage of the body (V_{bb}) of the FET transistor,” controls the threshold voltage of the transistor. EX1006, 3:33-35, 3:46-51. Borkar explains that “leakage power consumption is higher with a smaller threshold voltage and lower with a higher threshold voltage. The active power consumption may also be effected by body bias. A lower threshold allows a higher clock rate which means results in more active power.” EX1006, 3:53-57.

149. Borkar discloses some embodiments that apply these power controlling mechanisms (changing clock frequency, supply voltage, and body bias) in the context of a single-processor system, EX1006, Figs. 1-4, and some embodiments with multiple “domains.” EX1006, Figs. 5, 7. Borkar’s “domains” are groups of transistors, which can be controlled independently of each other. EX1006, 9:48-52.

Borkar also refers to these domains as “functional unit blocks.” EX1006, 9:58-59, 10:34-36.

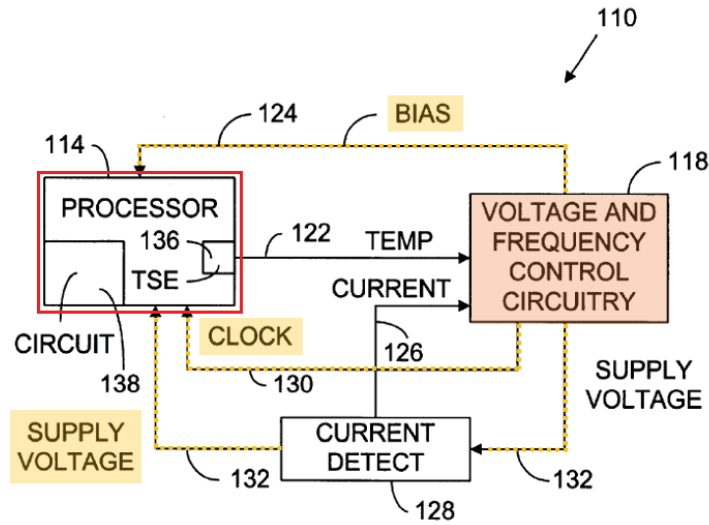


FIG. 1

EX1006, Fig. 1 (single-processor embodiment).

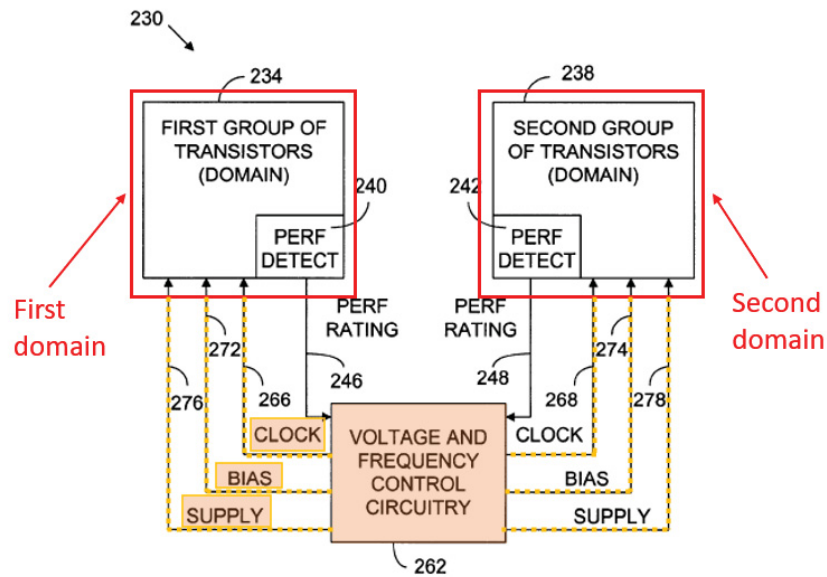
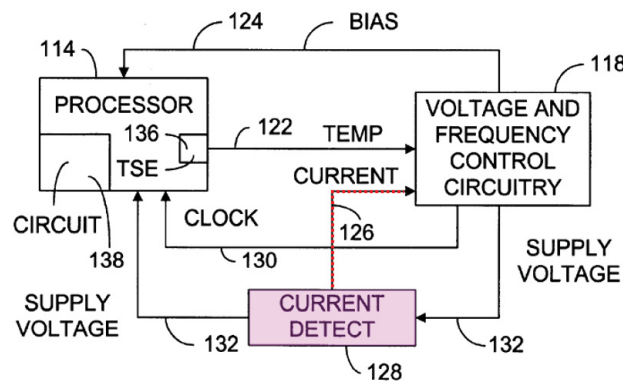


FIG. 5

EX1006, Fig. 5 (multiple-domain embodiment).

150. Borkar discloses embodiments in which “current detection circuitry” sends a current signal to the control circuitry, which can then calculate the power consumption level. EX1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7. “Control circuitry 118 may consider the current signal (which when multiplied by the supply voltage indicates the active power consumption) in deciding how to control the settings.” EX1006, 4:64-67; *see also* EX1006, 13:7-8.



EX1006, Fig. 1.

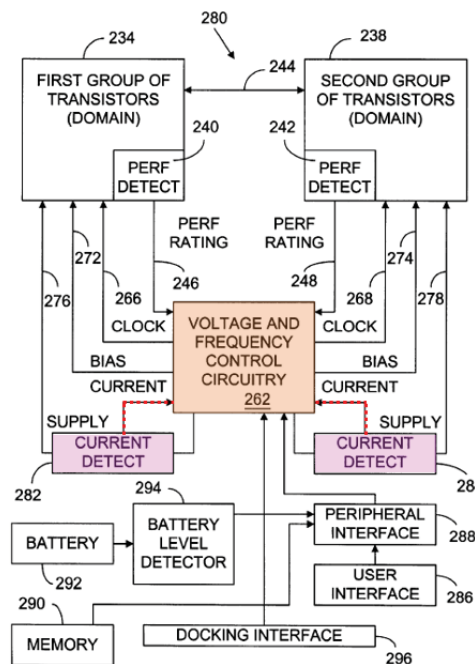


FIG. 7

EX1006, Fig. 7.

2. Combination of Nowka and Borkar

151. In my opinion, a POSITA would have been motivated to combine the teachings of Nowka and Borkar with a reasonable expectation of success for a number of reasons.

152. First, Nowka and Borkar are related to the same field: power management of integrated circuits on a chip. Nowka describes a “PowerPC system-on-a-chip processor which makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.” EX1004, Abstract. Similarly, Borkar describes “control circuitry [that] controls . . . a parameter of the processor,” such as performance, power consumption, and temperature.” EX1006, 1:60-2:3.

153. Second, and both Nowka and Borkar describe solutions to the known problem of balancing performance and power consumption in an integrated circuit. It was well known to a POSITA that lowering power consumption can lead to tradeoffs in performance. For example, Nowka states that “[w]hile [devices’] peak performance demands tend to be significant, they are also highly power constrained.” EX1004, 1441. Similarly, Borkar states that “[t]he performance, power consumption, and temperature [of an integrated circuit] are typically related.” EX1006, 1:20-21. Borkar further states that “[t]he user may specify certain power

conditions or a power versus performance tradeoff.” EX1006, 5:45-46. Therefore, both Nowka and Borkar address the need to balance performance and power consumption, and a POSITA considering Nowka’s solution would have naturally looked to Borkar for additional teachings on this common subject.

154. Third, both Nowka and Borkar disclose the concept of operating distinct parts of the integrated circuit using different operating parameters, such as frequency and voltage. Nowka states that “the power distribution has been divided into four distinct domains.” EX1004, Fig. 3, 1442. Similarly, Borkar discloses that the “first and second groups of transistors may be different function unit blocks (FUBS) on the same chip” and that, “[b]ecause of transistor parameter variations, certain performance and/or power parameters of first domain 234 may be different than that of the second domain 238.” EX1006, 10:34-39. A side-by-side comparison of Nowka’s Figure 3 (left) and Borkar’s Figure 5 (right) shows the distinct power domains in each reference.

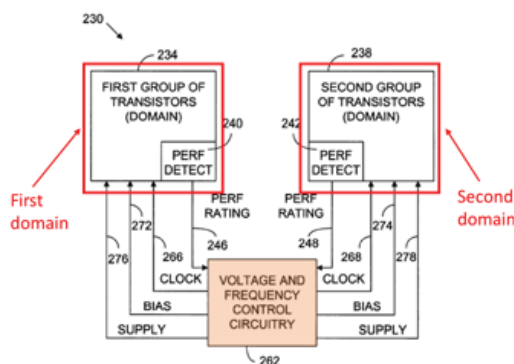
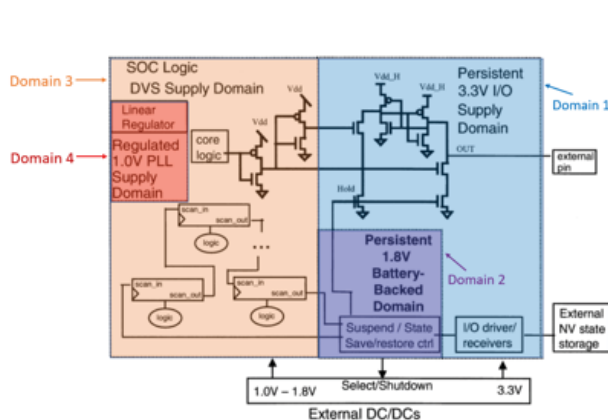


FIG. 5

155. Fourth, both Nowka and Borkar disclose the concept of controlling the power of power domains through dynamically changing variables such as frequency and voltage. Nowka states that “[t]he primary means of matching the performance and power consumption of this device to the application is through the use of dynamic voltage scaling (DVS),” (EX1004, 1442), and that “[w]hen the performance demands of the application decrease, the system software can lower the operating frequency.” EX1004, 1444. Similarly, Borkar discloses changing the body bias, supply voltage, and/or clock frequency based on power or heat conditions. “The process of selecting the body bias, supply voltage, and/or clock settings in control circuitry 114 and 144 may be iterative process involving feedback from signals indicative of levels of the parameters (such as temperature and current) and other signals indicating preference (such a [*sic*] battery level signals and user selections).” EX1006, 6:48-53; *see also* EX1006, 4:12-32, 5:25-34, 5:45-67, 7:51-59, 12:63-13:7, 13:11-18, 13:28-30, 13:31-38. Therefore, the solutions suggested by Nowka and Borkar are similar to one another and analogous to the ’306 patent, and a POSITA would have motivated to consult Borkar for additional teachings when considering techniques for Nowka’s power management functionality.

156. To the extent Nowka does not explicitly disclose comparing the power consumption to a threshold and performing an action based on the crossing of the

threshold level,⁶ a POSITA would naturally have looked to Borkar to combine with Nowka for the reasons enumerated above. Borkar describes “goals” that include “keeping power consumption below a particular level, keeping temperature in a particular range, obtaining the highest possible performance, and obtaining the highest performance while not exceeding a particular power consumption level.” EX1006, 12:11-15. For example, Nowka discloses that “during peak activity the power consumption of the processor core is best kept at or below 500 mW.” EX1004, 1441. Therefore, a POSITA would have understood that Nowka recommends implementing a power consumption threshold and would have naturally looked to a reference like Borkar, which discloses a technique for accomplishing this goal by calculating power consumption (based on voltage and current) and comparing the calculated power consumption to a threshold value.

157. In addition, a POSITA would have been motivated to supplement Nowka based on Borkar’s teachings to change a threshold voltage as a mechanism for controlling power consumption. The POSITA would have understood that changing the threshold voltage was another method—in addition to supply voltage

⁶ As discussed below in my analysis of claim 13, my opinion is that Nowka at least suggests and/or renders obvious this feature combination in a different but complementary way to Borkar.

scaling, frequency scaling, and others—to control the power consumption level. As Borkar explains, controlling threshold voltage is especially helpful for managing leakage power, (EX1006, 3:46-58, 6:16-40). Nowka also teaches that “[s]tatic power due to reverse-biased junction current, sub-threshold leakage, gate leakage and analog current sources can limit the operating lifetime of battery-powered systems. Decreasing the standby power of the IC increases shelf-life as well as overall energy efficiency.” EX1004, 1446. Therefore, a POSITA would have understood that Nowka recommends implementing techniques to reduce “static power,” which is also referred to as “leakage power.” Borkar provides such a mechanism for controlling power via controlling threshold voltage, and a POSITA would have looked to Borkar to incorporate that technique in Nowka’s SOC.

3. Claim 9

158. Claim 9 recites: “The method of claim 7 wherein the first voltage comprises a threshold voltage.” The Nowka-Borkar combination renders this claim obvious.

159. As discussed, Borkar discloses modifying a threshold voltage depending on the needs and operation of the integrated circuit. Similar to the ’306 patent’s teaching that “an example of an action is to control dynamic leakage by controlling variable V_t transistors,” (EX1001, 4:54-55), Borkar explains: “The leakage power consumption is higher with a smaller threshold voltage and lower

with a higher threshold voltage. The active power consumption may also be affected by body bias. A lower threshold allows a higher clock rate which means results [sic] in more active power.” EX1006, 3:53-57. Using this relationship between threshold voltage and power, Borkar discloses changing threshold voltage as one of the actions to change the parameters of a processor or domain. For example:

In some embodiments, if the temperature TACTUAL of processor 114 as represented in the temperature signal on conductor(s) 122 exceeds an upper temperature limit THIGH, control circuitry 118 changes the *body bias*, supply voltage, and/or clock signal settings to decrease temperature. For example, the supply voltage and clock frequency may be decreased, and/or body bias signals changed *so that the threshold voltage is raised*. In some embodiments, if TACTUAL drops below a lower temperature limit TLOW, control circuitry 118 may increase the supply voltage, increase the clock frequency, and/or the change the bias voltages *so that the threshold voltage is lowered*.

EX1006, 4:21-32. In this scenario, threshold voltage is raised or lowered to change power consumption level in response to certain temperature conditions, which indicate needs and operation of the integrated circuit (temperature too high or too low).

160. In another example, Borkar explains that “when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to *raise the threshold voltages*

of some or all of the transistors. This will reduce the power consumption to maintain the battery.” EX1006, 5:25-30. Once again, threshold voltages are changed to change the power consumption based on needs and operation of the system (battery power is low). Borkar also explains how threshold voltage can be used to balance performance and power consumption, and how changing threshold voltage can alleviate leakage power:

In some respects, performance is increased by the settings that cause a decrease in power consumption and vice versa. There are various tradeoffs and merely changing one of the supply voltage, clock frequency, or threshold voltages, without changing the others may not yield the desired results. By providing proper settings with each of supply voltage, clock frequency, *and threshold voltages*, a high processor performance can be achieved. Nevertheless, even in those embodiments in which frequency is not changed, *leakage power can still be reduced by increasing the threshold voltages*.

EX1006, 6:15-24. Therefore, the threshold voltage of Borkar is modified depending on the needs and operation of the integrated circuit.

161. A POSITA would have been motivated to integrate this technique in Nowka’s SOC with a reasonable expectation of success because (as I explained above) it was well known in the art that changing threshold voltage can minimize power consumption, including leakage power. Nowka explains: “Static power due to reverse-biased junction current, *sub-threshold leakage*, gate leakage and analog

current sources can limit the operating lifetime of battery-powered systems. Decreasing the standby power of the IC increases shelf-life as well as overall energy efficiency.” EX1004, 1446. Thus, Nowka would have motivated a POSITA to minimize static power such as sub-threshold leakage power consumption, and the desirability of doing so was well established in the art. *See* EX1017 at 20 (“Sub-threshold leakage is becoming increasingly important because of reductions in power supply. As power supply voltages, the transistor threshold is lowered to keep turned-on transistors well within the conductive region of the operation. Consequently, transistors operating in a non-conductive region are turned off only weakly, and conduct some current even in their “OFF” state.”), 27 (“[S]everal innovative CMOS devices and circuits are under active investigation [] that allow dynamic control of voltage supply and threshold voltages.”); EX1024 at 19 (“Overall, the main issue in the design of future libraries will be the static power. . . . the static power will increase significantly due to these low V_T .”). Further, integrating threshold voltage changes, as Borkar describes, in Nowka’s SOC would have been a straightforward implementation of including body bias control circuitry for the transistors in Nowka. Such technologies were implemented in CMOS circuits as early as 1998, and their implementation required no more than routine electrical and computer engineering skills and principles by the time of the Critical Date. *See, e.g.*, EX1016.

4. Claim 13

162. Claim 13 recites: “The method of claim 1 further comprising: monitoring the power consumption level of the one of the power islands; determining whether a threshold level was crossed based on the power consumption level; and performing another one of the based on the crossing of the threshold level.” The Nowka-Borkar combination renders this claim obvious.

163. Nowka discloses that “during peak activity the power consumption of the processor core is best kept at or below 500 mW.” EX1004, 1441. Therefore, a POSITA would have understood that this teaching from Nowka suggests and recommends implementing a power consumption threshold level and would have looked to a reference like Borkar disclosing such a mechanism.

164. Borkar explains that “[i]n many situations, then, control circuitry 262 may seek to obtain the highest performance that both domains can achieve at the same clock frequency and with [*sic*] exceeding a power consumption level. The actual and acceptable power consumption levels could be different for the different domains. Different techniques may be used to not exceed power consumption levels. A simple but imprecise way is to not allow the supply voltage, threshold voltages, or frequency, to pass certain levels.” EX1006, 13:1-6. As would have been apparent or obvious to a POSITA, Borkar’s “acceptable power consumption levels” correspond to the “threshold level” of the ’306 patent.

165. Borkar explains that a more precise way to keep power consumption at a certain level is “to detect current being consumed” and determining the power consumption using the current and supply voltage. EX1006, 13:6-7. Borkar discloses numerous embodiments (e.g., depicted in Figures 1-2, 4, 7) that explicitly show “current detection circuitry” which provide current signals to “voltage and frequency control circuitry.” EX1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7 (Figs. 1, 7 shown below). Because current multiplied by supply voltage is power consumption, Borkar’s system can monitor power consumption by monitoring current signal. EX1006, 4:64-67, 13:7-8. As a POSITA would have understood, by calculating the power consumption in this way, the system can monitor the power consumption and perform appropriate actions, such as changing body bias, supply voltage, and clock frequencies, in the event the power consumption approaches or crosses the threshold level. EX1006, 6:1-7, 13:2-7.

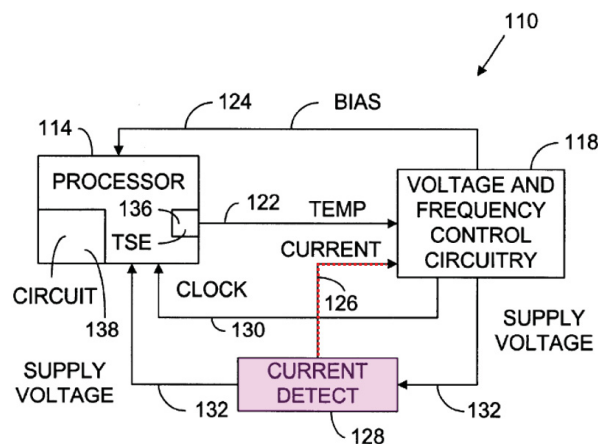


FIG. 1

EX1006, Fig. 1.

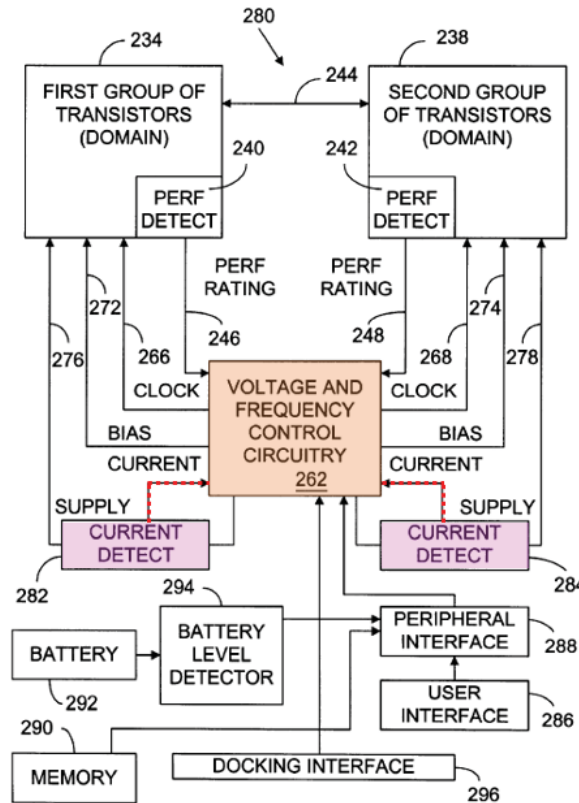


FIG. 7

EX1006, Fig. 7.

166. As I explained above, a POSITA would have been motivated to combine Borkar’s power consumption monitoring with Nowka’s voltage and frequency scaling to achieve more precise and predictable power consumption control. Where Nowka changes operating parameters based primarily performance demands, (EX1004, 1444 (“In anticipation of lower performance demands, the clock and power management software modifies the PLL output divider value...")), incorporating power monitoring from Borkar would also enable Nowka’s SOC to further “dynamically [adapt] to the changing needs for performance and power demanded by the applications,” (EX1004, 1446). This is because, as Borkar teaches,

“[i]n practice, the maximum performance may lead to an unacceptably high power consumption and heat.” EX1006, 12:63-64. Monitoring for power consumption to cross certain levels would better match the available resources to the needs of Nowka’s SOC, especially because “during active computation [the system’s] required performance tends to vary widely and quickly as a function of the workload.” EX1004, 1441.

167. In addition, Borkar discloses and/or renders obvious the features of claim 13 by describing “control circuitry” that “monitors a temperature signal...related to the temperature of [a] processor,” which a POSITA would have understood (and the ’306 patent concedes) reflects the power consumption level. EX1006, 4:12-20; *see also* EX1001, 6:47-50 (explaining that “temperature” is an example of a “power consumption level[.]”). According to Borkar, “if the temperature TACTUAL of [the] processor...exceeds an upper temperature limit THIGH,” the system, in response to this determination, performs an appropriate action—e.g., “change[s] the body bias, supply voltage, and/or clock signal settings”—“to decrease temperature.” EX1006, 4:21-46. Naturally, a POSITA would have been motivated to integrate Borkar’s temperature monitoring techniques with Nowka to provide the predictable benefit of preventing overheating. EX1006, 1:11-56.

168. A POSITA would have needed only routine electrical and computer engineering skills and principles to implement Borkar's temperature/power monitoring and threshold-comparing mechanisms in Nowka's SOC, as demonstrated by Borkar's implementation in a system analogous to Nowka's. Such a combination would predictably result in improved performance and longevity by limiting power consumption levels to the appropriate levels, which in turn prevents thermal damage and adverse effects on performance.

169. As an additional and independent reason that claim 13 is obvious, I note that Nowka teaches that "the clocks to the individual functional cores can be frozen by the clock and power management software...in response to inactivity." EX1004, 1445. A POSITA reading this aspect of Nowka would have understood that the "software" is implementing a basic and well-known control algorithm of: (i) monitoring the activity (and thus "power consumption") of the individual functional cores ("power islands", as discussed above at ¶51)), (ii) determining whether the activity level crosses below a predetermined threshold; and (iii) responsively performing the action of freezing the corresponding clock.

5. Claim 24

170. Claim 24 recites: "The system of claim 22 wherein the first voltage comprises a threshold voltage." The Nowka-Borkar combination renders this claim

obvious for at least the reasons discussed above with respect to claims 9 and 16, which I incorporate herein.

6. Claim 28

171. Claim 28 recites: “The system of claim 16 wherein the power manager is configured to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.” The Nowka-Borkar combination renders this claim obvious for at least the reasons discussed above with respect to claims 13 and 16, which I incorporate herein.

7. Claim 45

172. Claim 45 recites: “The software product of claim 43 wherein the first voltage comprises a threshold voltage.” The Nowka-Borkar combination renders this claim obvious for at least the reasons discussed above with respect to claims 9 and 37, which I incorporate herein.

8. Claim 49

173. Claim 49 recites: “The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the

threshold level.” The Nowka-Borkar combination renders this claim obvious for at least the reasons discussed above with respect to claims 13 and 37, which I incorporate herein.

C. Analysis of Nowka in view of Boerstler with Respect to Claim 35

174. For the reasons articulated in detail below, and based on my review of the '306 patent and the Nowka and Boerstler references, I am confident that a POSITA would have readily understood that Nowka in view of Boerstler renders obvious claim 35.

1. Overview of Boerstler

175. Boerstler is titled “Multiphase voltage controlled oscillator with variable gain and range.” EX1007, Title. Boerstler relates to a voltage controlled oscillator (“VCO”) for controlling timing elements that is composed of an interleaved ring oscillator, a voltage multiplexer, and true/complement generator, as shown in Figure 4. EX1007, 5:50-55.

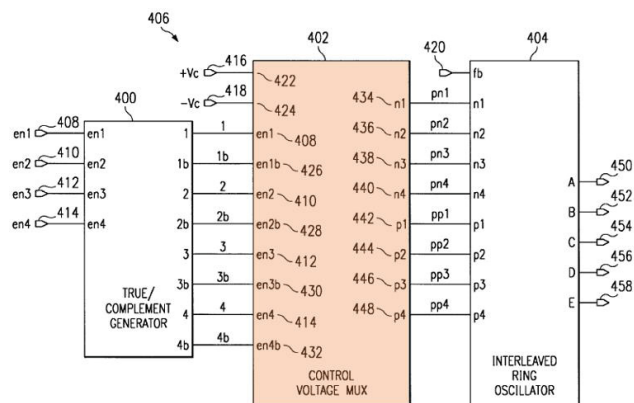


FIG. 4

EX1007, Fig. 4.

176. The multiplexer of Boerstler receives the true and complement signals, along with the control voltages 416 and 418. EX1007, 5:56-63. The multiplexer selects which transmission gates in the interleaved ring oscillator will be activated based on the true and complement signals. EX1007, 5:66-6:1. For example, Boerstler explains the scenario where en1 408, en1b 426, en2 410, and en2b 428 are selected, which when combined with control signals in the interleaved ring oscillator being turned off, will result in output n1 434 and output n2 436 having output voltage $+V_c$ and outputs p1 442 and p2 444 having output voltage $-V_c$. EX1007, 6:8-24. This operation allows the multiplexer to output different voltages depending on the input voltage and enable pins.

2. Combination of Nowka and Boerstler

177. In my opinion, a POSITA would have been motivated to combine the teachings of Nowka and Boerstler with a reasonable expectation of success for a number of reasons.

178. First, both Nowka and Boerstler resulted from work performed at the same company, IBM. EX1004, 1446 (“This chip represents the joint development of IBM’s Austin Research Laboratory, IBM’s Microelectronics Division [], as well as IBEM’s Tokyo Research Laboratory and IBM’s T.J. Watson Research Laboratory.”); EX1007, (73) (showing IBM as assignee). Second, the two are in the same field of endeavor, EX1004, 1441 (“A PowerPC system-on-a-chip processor”);

EX1007, 1:16-17 (“The present invention relates to timing of a signal in a computer system.”) They both emphasize the importance of clock generation and distribution in integrated circuits. Nowka states that “the clock generation is key to supporting a voltage scalable design.” EX1004, 1444. Similarly, Boerstler states that voltage controlled oscillators (VCOs) are “extremely important for applications such as processor clock generation and distribution, wired and wireless communication, system synchronization and frequency synthesis.” EX1007, 1:23-27.

179. Third, the solution offered by Boerstler related to multiplexers for distributing different voltage levels in VCOs is directly incorporated by Nowka. Nowka states that the VCO shown in Figure 7 and used to generate control voltages for the PLL “is an interleaved five-stage ring oscillator [11].” The reference [11] that Nowka cites is the Boerstler reference (EX1007). EX1004, 1444, 1447.

180. In my opinion, because Nowka and Boerstler provide a similar solution to a similar problem within the same field of endeavor, were both authored by or assigned to IBM, and Nowka explicitly cites Boerstler for its VCO, a POSITA would have looked at, and been motivated to combine, Nowka and Boerstler when implementing power control circuitry that requires generating different voltage levels. A POSITA would have further had a reasonable expectation of success in such a combination, as evidenced by Nowka itself using Boerstler’s VCO, which contains a multiplexer to generate various voltage levels.

3. Claim 35

181. Claim 35 recites: “The system of claim 16 wherein the power control circuitry includes voltage multiplexing circuitry.” The Nowka-Boerstler combination renders this claim obvious. For example, Nowka discloses a “voltage controlled oscillator” (VCO), highlighted in red, that is incorporated into the phase locked loop (PLL), as shown in Nowka’s Figure 7. The PLL is part of Nowka’s power control circuitry, as discussed above for claim 16 (*see* §VIII.A.15).

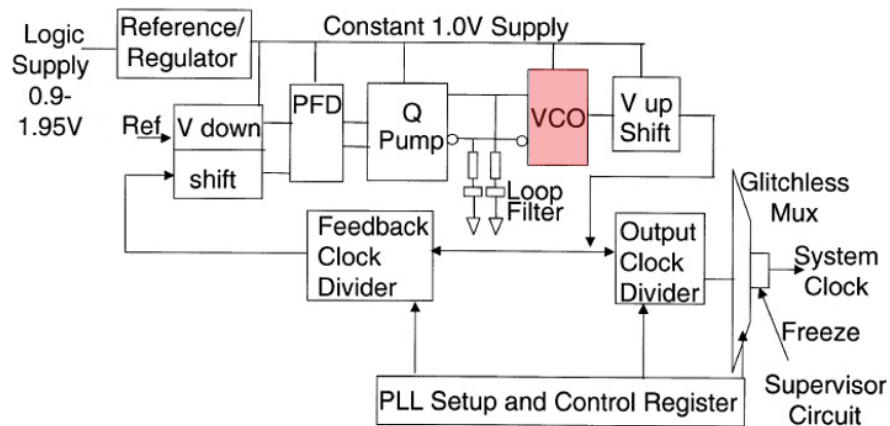


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

182. As described above, Nowka cites to Boerstler to describe its VCO. Nowka states that the VCO shown in Figure 7 and used to generate control voltages for the PLL “is an interleaved five-stage ring oscillator [11].” The reference [11] that Nowka cites is the Boerstler reference. EX1004, 1444, 1447.

183. The VCO in Boerstler, shown in Figure 4 below, includes “a true/complement generator 400, *a control voltage multiplexer 402*, and interleaved ring oscillator 404.” EX1007, 5:50-55, Fig. 4.

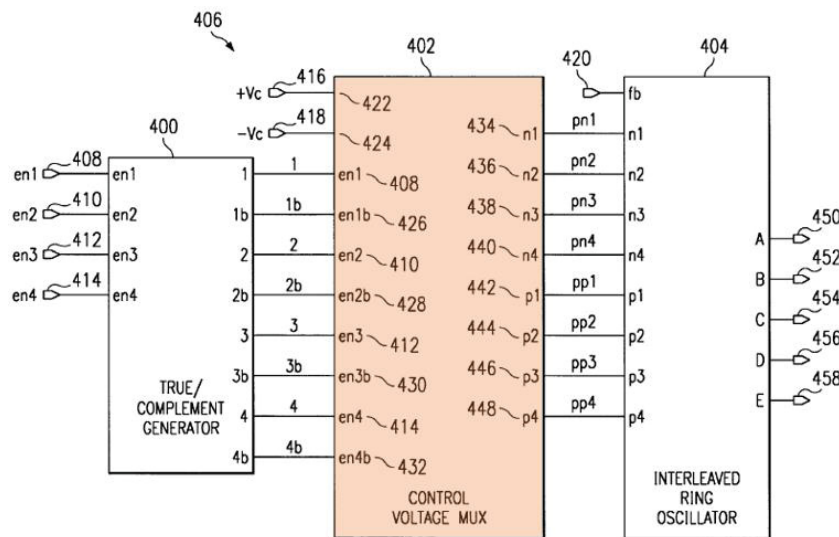


FIG. 4

EX1007, Fig. 4.

184. As explained by Boerstler, the control voltage multiplexer 402 takes as inputs true and complement signals from the true/complement generator 400, along with a control voltage of +Vc and -Vc. EX1007, 5:56-66. The control voltage multiplexer “is used to select control elements that are to be enabled within interleaved ring oscillator 404.” EX1007, 5:65-6:1. As described in the overview of Boerstler, the multiplexer determines the output voltage and logical state on outputs n1-n4 and p1-p4. “The analog control voltage is channeled to the appropriate control elements by the analog multiplexer.” EX1007, 7:2-4.

185. A voltage multiplexing circuit, such as the “control voltage multiplexer” of Boerstler, was a well-known solution in the art to produce multiple different voltage signals. Such circuitry was frequently included in VCOs, which in turn “is used in applications, such as, for example, PLLs and the like.” EX1007, 4:45-47. A POSITA would have needed only routine electrical and computer engineering principles to implement it in Nowka’s SOC, and indeed the authors of Nowka did implement it.

D. Analysis of Nowka in view of Bertin with Respect to Claims 1-12, 14-23, 25-27, 29-34, 36-48, 50-51

186. For the reasons articulated in detail below, and based on my review of the ’306 patent and the Nowka and Nicole references, I am confident that a POSITA would have readily understood that Nowka in view of Bertin renders obvious claims 1-12, 14-23, 25-27, 29-34, 36-48, 50-51.

187. Additionally, I note that integration of Bertin’s teachings does not disturb the aspects of Nowka that I previously discussed with respect to dependent claims 2-8, 10-12, 14-15, 17-23, 25-27, 29-34, 36, 38-44, 46-48, 50-51 (*see* above in Section VIII.A). I do not repeat my prior analysis of Nowka relating to these dependent claims because it is identical and fully incorporated here. Rather, I focus below on Bertin’s teachings regarding independent claims 1, 16, 37 and dependent claims 9, 24, 45.

1. Overview of Bertin

188. Bertin’s disclosure “relates to integrated circuits and more particularly intelligent power management of the integrated circuit.” EX1027, 1:14-16. As in Nowka and the ’306 patent, Bertin’s intelligent power management technique aims to “optimize[] chip power/performance” by accounting for “the demands placed on the integrated circuit” and providing “independently controllable” units “operated at one of plural power levels.” EX1027, 4:49-54, 1:63-2:11.

189. Among other things, Bertin teaches that a “power management unit [] sets the power levels for the different units” based on logic that “determines, for each functional unit, whether the power requirement and power status for the unit are in agreement.” EX1027, 5:35-39. “In the event that a power transition is necessary,” Bertin’s technique “transition[s] the performance level of that particular functional unit.” EX1027, 5:44-50; *see also* 6:4-18 (explaining that “[t]hose skilled in the art can readily adapt” and accommodate “more than two power levels per unit”). For example, Bertin’s approach places the appropriate units “in a high power state” when “[e]xecution of the [application] instruction[s] at a high rate [is] require[d].” EX1027, 2:8-11.

2. Combination of Nowka and Bertin

190. In my opinion, a POSITA would have been motivated to combine the teachings of Nowka and Bertin with a reasonable expectation of success for a

number of reasons. Specifically, the POSITA would have been motivated to implement Nowka's "software control" for dynamic voltage and frequency scaling, (EX1004, 1442, 1444, 1446), based on prescribed "power levels" (or "power state[s]") that correspond to "power requirement[s]" dictated by an application, as taught by Bertin (EX1027, 5:35-39, 2:8-11). From a POSITA's perspective, integrating the supplemental teachings of Bertin with Nowka's disclosure would have involved nothing more than applying known solutions to known problems in the field of power management for integrated circuits to achieve predictable outcomes—namely, an SOC with functionality to change between different prescribes power levels or states using dynamic frequency and voltage scaling. The fundamental aspects of Nowka's disclosure would remain intact, bolstered by the well-known and beneficial teachings of Bertin to arrive, with a reasonable expectation of success, at a system that renders obvious the '306 patent's claims.

191. Note that when discussing the Nowka-Bertin combination, I am addressing how and why a POSITA would have been motivated to combine the concepts that they teach. To be clear, I am not suggesting that Nowka's SOC would be changed to match all of the exemplary implementation details that Bertin discloses. Rather, what I am saying is that a POSITA would have been motivated to integrate Bertin's notion of using prescribed power levels to match the power

requirements of an application in the context of Nowka’s SOC with voltage and frequency scaling capabilities.

192. First, a POSITA would have been prompted to pursue the Nowka-Bertin combination based on Nowka’s teachings and suggestions to do so. For example, Nowka teaches and suggests the notion of providing prescribed maximum/minimum power levels based on the “performance demands” of “battery-powered applications.” EX1004, 1441. As discussed, with “applications [that] tend to have peak performance demands as high as 500 MIPS,” Nowka explains that “the power consumption of the processor core is best kept at or below about 500 mW”—i.e., a maximum power level or state. EX1004, 1441. By contrast, Nowka says, “active power consumption [can also be adjusted] as low as 53 mW at a supply of 1.0 V”—i.e. a minimum power level or state. *Id.*

TABLE II
CPU CORE WITH CACHES CHARACTERISTICS

	TC1 (1.8V)	TC2 (1.0V)
Maximum Frequency (estimate)	380 MHz	152 MHz
Power Consumption (estimate)	500 mW	53 mW
TC1 – Typical conditions: 1.8V, 55C, nominal silicon		
TC2 – Typical conditions: 1.0V, 55C, nominal silicon		

EX1004, Table II

193. As another example, Nowka describes a scenario where the “clock and power management software” decreases the logic power “by about 70%” “[i]n

anticipation of lower performance demands” and recovers to the original power level/state upon “anticipating an increase in demand.” EX1004, 1444; *see also id.*, 1444 (“a range of standby power levels”), 1446 (describing “a range of standby *power levels*”). Bertin’s straightforward approach of determining a prescribed power level that reflects application-based demand and taking proper actions to transition power consumption to “bring the [power] requirements and status into agreement,” (EX1027), 5:45-47), is what a POSITA would have understood Nowka to teach and suggest. Indeed, Nowka promotes the idea of providing “[c]apabilities to dynamically *match* the performance of the device with the demands of the applications[.]” EX1004, 1442.

194. Second, the technique of utilizing prescribed power levels or states to implement power management on integrated circuits was commonly implemented by the time of the Critical Date. *E.g.*, EX1017 (Dynamic Power Management) at 182 (a textbook on dynamic power management describing different “*system power states* which represent states of operation with radically different level[s] of functionality and power dissipation”). For example, in June 2000 technical paper titled “A Survey of Design Techniques for System-Level Dynamic Power Management,” the authors explain that “*Dynamic power management* (DPM) is a design methodology that dynamically reconfigures an electronic system to provide the requested services and performance levels with a minimum number of active

components or a minimum load on such components.” EX1018 (Benini Survey) at 1. Such components have “the availability of multiple *modes of operation* that span the power-performance tradeoff.” EX1018 at 2. And, accordingly, can be modeled and controlled using “a finite state representation,” where “[s]tates are the various modes of operation.” EX1018 at 2. Figure 1 of this paper, provided below, illustrates an example where three different modes/states of operation—i.e., RUN, IDLE, SLEEP—reflect different prescribed power levels. EX1018 at 2; *see also* 12 (“the system controller can choose from different levels of power savings, depending on the wake-up response time requirements”).

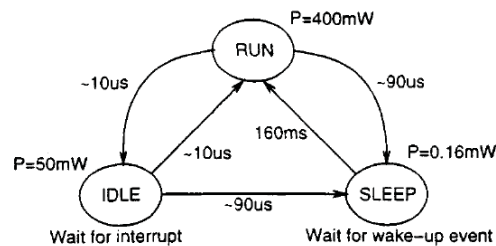


Fig. 1. Power state machine for the StrongARM SA-1100 processor.

The same is true of Figure 14, which shows the finite state representation of an IBM hard disk drive that shows three different states with three different prescribed power levels. EX1018 at 15.

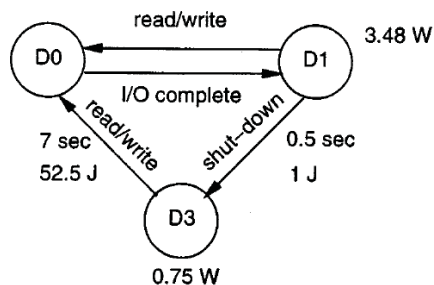


Fig. 14. PSM for IBM DTTA HDD.

195. By the time of the Critical Date in 2003, even commercially available versions of the PowerPC processor that Nowka employs (“PowerPC 405 core”) utilized multiple different power management modes, each associated with a different level of power consumption. EX1028 at 1-5. Table 2 and Figure 1 from a technical paper describing the PowerPC 603 and its “numerous power management (PM) features” demonstrate these different power modes and the prescribed power levels they reflect. EX1028 at 3.

Table 2. Typical power consumption

PM Mode	Frequency (Internal)		
	50 MHz	66 MHz	80 MHz
Full On no DPM	1.78 W	2.18 W	2.54 W
Full On with DPM	1.52 W	1.89 W	2.20 W
Doze	242 mW	307 mW	366 mW
Nap	89 mW	113 mW	135 mW
Sleep	66 mW	89 mW	105 mW
Sleep no PLL	15 mW	18 mW	19 mW
Sleep no PLL on SYCLK	<5 mW	<5 mW	<5 mW

EX1028 (Suessmith) at 3.

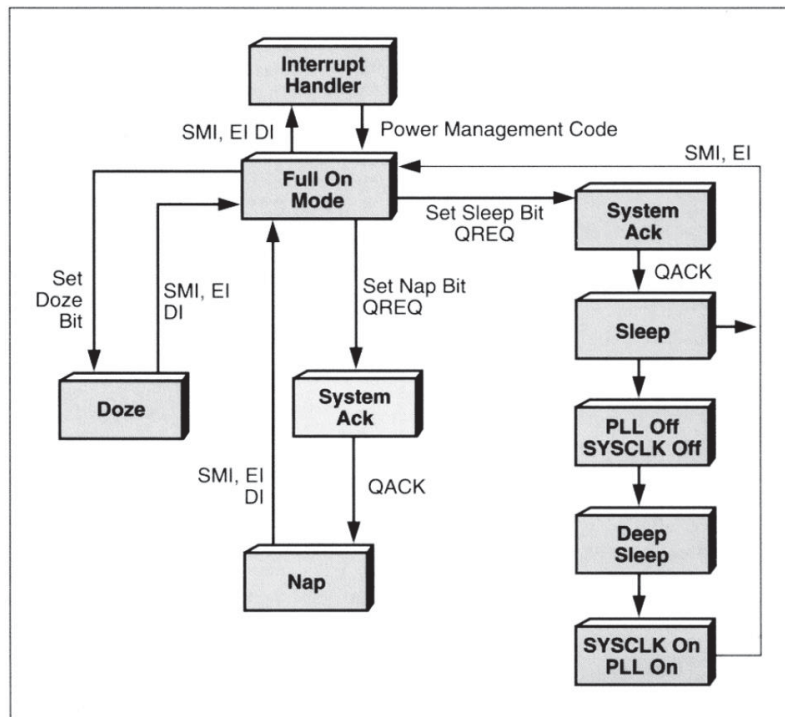


Figure 1. PowerPC 603 power management mode transitions
EX1028 (Suessmith) at 3.

196. To summarize, prescribed power levels were an exceedingly well-known solution to the equally well-known problem of balancing performance and power consumption in electronic systems, particularly battery-powered devices capable of running high-performance applications. Bertin utilizes power levels/states for this purpose, and it would have been straightforward for a POSITA to do the same in the context of Nowka's SOC with robust dynamic power management capabilities like voltage and frequency scaling.

197. Third, a POSITA would have understood that utilizing prescribed power levels or states (as taught by Bertin) provides the advantage of enabling added functionality, e.g., by facilitating communication between the application creating

the performance demands and the software/circuitry coordinating on-chip dynamic power management. See EX1017 at 187 (“The *OnNow* initiative encourages software developers to write applications that directly interact with the power management policy of the OS.”), 198 (describing how, in the ACPI standard specification, “[t]he set-power-state operation is used by the OS to put a device into one of four power states”). For example, by employing prescribed power levels, Bertin provides functionality for the application (or a user) to access the power manager and indicate one or more required power levels for specified on-chip units. EX1027, 5:35-50, 7:8-16 (“Override register 230 may be controlled by the application software to allow direct control of speed/power parameters of the chip 100.”). In this way, the application (or a user) can directly influence performance without detailed knowledge of specific parameters like voltage, frequency, etc. See EX1017 at 188 (“Thanks to communication between OS and applications, the global power policy can be based on both user and application activity in the system.”), 181 (explaining that “[a]pplications communicate with the operating system through a standardized *application programming interface* (API)” and the operating system interfaces with “hardware resources through *device drivers*” that “hide[] the details of the hardware implementation of any particular resource, and offer[] a standard interface between hardware services and system requests”).

198. Fourth, and consistent with Nowka’s teachings to independently control the power consumption of individual cores, (EX1004, 1445), a POSITA would have appreciated the effectiveness and efficiency of Bertin’s disclosed approach of utilizing prescribed power levels to independently control any given “functional unit” on the chip based on whether a coded instruction of an application will utilize that unit, (EX1027, 2:6-52, 4:39-5:6). In this way, Bertin explains, “optimized chip power/performance for that particular instruction will result by running [any unused] functional units at a lower or lowest available power level.” EX1027, 4:59–61. Bertin’s approach of using specific software instructions to dictate component power levels is consistent with the well-known principles of dynamic power management that not all components need to be at peak performance at all times, and that the varying need for different components can be reasonably predicted. EX1017 at 77-78; EX1018 at 1. Bertin proposes to predict future need based on the actual instructions that will soon be executed to carry out an ongoing application.

3. Claim 1

(a) Element 1[p]

199. Element 1[p] recites: “A method of managing power on an integrated circuit including a plurality of power islands, the method comprising.” The Nowka-Bertin combination renders obvious Element 1[p].

200. To start, Nowka discloses and/or renders obvious Element 1[p] for at least the reasons discussed above at Section VIII.A.2(a), which I incorporate herein. Additionally, Bertin’s teachings bolster my prior analysis regarding Nowka’s individual “cores” acting as “power islands.” For example, Bertin makes clear that individual functional units—like Nowka’s “cores”—have “independently controllable body voltage or threshold voltage.” EX1027, 1:63-2:11. Thus, in the Nowka-Bertin combination, there is no question that the cores within the logic domain are power islands with the capability of being controlled individually and independently with respect to both voltage scaling and frequency scaling.

201. A POSITA would have been motivated to pursue this aspect of the Nowka-Bertin combination to provide additional flexibility in the types of dynamic power management control schemes that the SOC can support. In addition, as a POSITA would have appreciated, the ability to individually and independently modify the voltage and frequency of each core is advantageous because, as both Bertin and Nowka acknowledge, different applications tend to “make[] significantly greater demands” on different subsets of components. EX1004, 1445 (explaining the that “Dhrystone2.1 benchmark under Linux...tends to stress the processor core” while “MPEG decoding under Linux...makes significantly greater demands on the cache memory, I/O interfaces and LCD core”); EX1027, 2:6-11 (“Execution of the

instruction at a high rate will require the correlated functional unit(s) to be in a high state, other functional units need not be in a high power state.”).

(b) Element 1[a]

202. Element 1[a] recites: “determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands.” The Nowka-Bertin combination renders obvious Element 1[a].

203. To start, Nowka discloses and/or renders obvious Element 1[a] for at least the reasons discussed above at Section VIII.A.2(b), which I incorporate herein. Additionally, Bertin describes a power manager that “sets the power levels for the different units” based on logic that “determines, for each functional unit, whether the power requirement and power status for the unit are in agreement.” EX1027, 5:35-39. In the Nowka-Bertin combination, Nowka’s “power management software,” (EX1004, 1444), employs Bertin’s conceptual approach and, thus: (i) determines a specified target power level for the dynamically voltage-scaled and frequency-scaled logic domain based on the “performance demands of the application,” (EX1004, 1446); and (ii) compares that target power level to the logic domain’s current power status.

(c) Element 1[b]

204. Element 1[b] recites: “determining at least one of actions to change a power consumption level of the one of the power islands to the target power level.” The Nowka-Bertin combination renders obvious Element 1[b].

205. To start, Nowka discloses and/or renders obvious Element 1[b] for at least the reasons discussed above at Section VIII.A.2(c), which I incorporate herein. Additionally, Bertin describes a power manager that “determines, for each functional unit, whether the power requirement and power status for the unit are in agreement” and, if necessary, works to “transition the performance level of [a] particular functional unit” by “provid[ing] the proper control to effect that state.” EX1027, 5:35-50, 6:52-57. In the Nowka-Bertin combination, Nowka’s “power management software” employs Bertin’s conceptual approach and, thus, utilizes the capabilities at its disposal—namely, “dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating”—to transition the logic domain and “match the power consumption [level]” with the target power level. EX1004, 1444, 1442. As a result, the power management software in the Nowka-Bertin combination renders obvious the claimed step of “determining at least one of actions to change a power consumption level of the one of the power islands to the target power level.”

(d) Element 1[c]

206. Element 1[c] recites: “performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” The Nowka-Bertin combination renders obvious Element 1[c] for at least the reasons discussed above at Sections VIII.A.2(d) (addressing Element 1[c] in view of Nowka) and VIII.D.3(c) (addressing Element 1[b] in view of Nowka-Bertin), which I incorporate herein. As I explained in these sections, the Nowka-Bertin combination involves performing dynamic frequency scaling as a mechanism to change an existing power consumption level to a target power level.

4. Claim 9

207. Claim 9 recites: “The method of claim 7 wherein the first voltage comprises a threshold voltage.” The Nowka-Borkar combination renders this claim obvious for the reasons I discussed above at Section VIII.A.7 (claim 7) and Section VIII.D.3(a) (Element 1[p]) regarding Bertin’s disclosure of changing the “threshold voltage” of individual functional units (“power islands”) to make power level adjustments. The POSITA would have understood that changing the threshold voltage was another well-known method—in addition to supply voltage scaling, frequency scaling, and others—to control the power consumption level. As Bertin explains, when “transistors achieve a high threshold voltage, [they] consume less

static power but on the other hand provide lower performance,” and vice versa. EX1027, 1:19-56. Using a known technique like modifying threshold voltage to predictably achieve the desired result of modifying power consumption would have been obvious to the POSITA.

5. Claim 16

(a) Element 16[p]

208. Element 16[p] recites: “A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising.” The Nowka-Bertin combination renders obvious Element 16[p] for at least the reasons discussed above at Sections VIII.A.2(a)-(b), VIII.A.15(a) (addressing Elements 1[p]-1[a], 16[p] in view of Nowka) and VIII.D.3(a)-(b) (addressing Elements 1[p]-1[a] in view of Nowka-Bertin), which I incorporate herein.

(b) Element 16[a]

209. Element 16[a] recites: “power control circuitry configured to control power for one of the power islands.” The Nowka-Bertin combination renders obvious Element 16[a] for at least the reasons discussed above at Sections VIII.A.2(a)-(b), VIII.A.15(b) (addressing Elements 1[p]-1[a], 16[a] in view of Nowka) and VIII.D.3(a)-(b) (addressing Elements 1[p]-1[a] in view of Nowka-Bertin), which I incorporate herein.

(c) Element 16[b]

210. Element 16[b] recites: “a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” The Nowka-Bertin combination renders obvious Element 16[b] for at least the reasons discussed above at Sections VIII.A.2(a)-(c), VIII.A.15(c) (addressing Elements 1[p]-1[c], 16[b] in view of Nowka) and VIII.D.3(b)-(d) (addressing Elements 1[a]-1[c] in view of Nowka-Bertin), which I incorporate herein.

6. Claim 24

211. Claim 24 recites: “The system of claim 22 wherein the first voltage comprises a threshold voltage.” The Nowka-Bertin combination renders obvious claim 24 for at least the reasons discussed above at Sections VIII.A.21 (addressing claim 22 in view of Nowka) and Sections VIII.D.3(a) and VIII.D.4 (addressing Element 1[p] and claim 9 in view of Nowka-Bertin), which I incorporate herein.

7. Claim 37

(a) Element 37[p]

212. Element 37[p] recites: “A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising.” The Nowka-Bertin combination renders obvious Element 37[p] for at least the reasons discussed above at Sections VIII.A.2(a)-(b), VIII.A.33(a) (addressing Elements 1[p]-1[a], 37[p] in view of Nowka) and VIII.D.3(a)-(b) (addressing Elements 1[p]-1[a] in view of Nowka-Bertin), which I incorporate herein.

(b) Element 37[a]

213. Element 37[a] recites: “power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” The Nowka-Bertin combination renders obvious Element 37[a] for at least the reasons discussed above at Sections VIII.A.2(b)-(d), VIII.A.33(b) (addressing Elements 1[a]-1[c], 37[a] in view of Nowka) and VIII.D.3(b)-(d)

(addressing Elements 1[a]-1[c] in view of Nowka-Bertin), which I incorporate herein.

(c) Element 37[b]

214. Element 37[b] recites: “a software storage medium operational to store the power management software.” Nowka discloses and/or renders obvious Element 37[b]. The Nowka-Bertin combination renders obvious Element 37[b] for at least the reasons discussed above at Sections VIII.A.2(c), VIII.A.15(c) (addressing Elements 1[b], 37[b] in view of Nowka), which I incorporate herein.

8. Claim 45

215. Claim 45 recites: “The software product of claim 43 wherein the first voltage comprises a threshold voltage.” The Nowka-Bertin combination renders obvious claim 45 for at least the reasons discussed above at Sections VIII.A.39 (addressing claim 43 in view of Nowka) and Sections VIII.D.3(a) and VIII.D.4 (addressing Element 1[p] and claim 9 in view of Nowka-Bertin), which I incorporate herein.

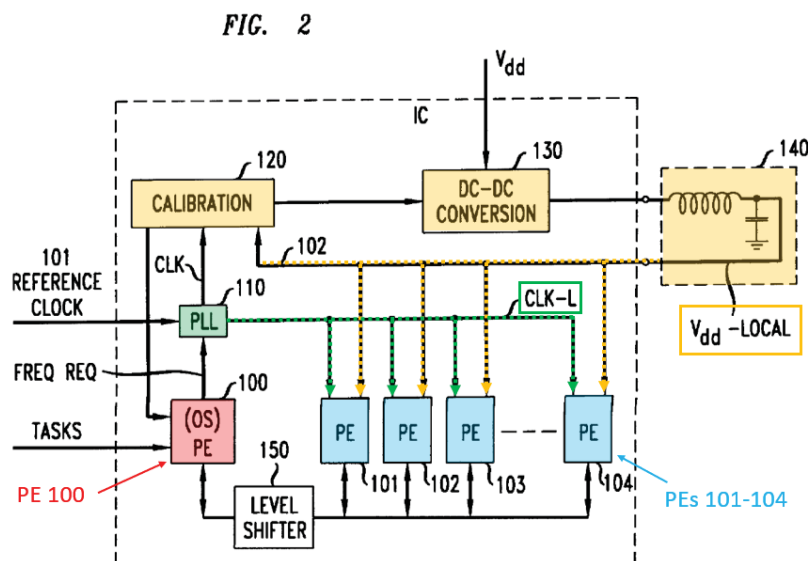
E. Analysis of Nicol with Respect to Claims 1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, 47

216. For the reasons articulated in detail below, and based on my review of the '306 patent and the Nicol reference, I am confident that a POSITA would have readily understood that Nicol renders obvious claims 1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, 47.

1. Overview of Nicol

217. Nicol is titled “Power reduction in a multiprocessor digital signal processor based on processor load.” EX1008, Title. Nicol relates to improving operation of a multi-processor chip “by dynamically controlling processing load of chips and controlling, significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption.” EX1008, Abstract.

218. In the embodiment depicted in Figure 2, Nicol’s multi-processor chip contains multiple processing elements (PEs) labeled with numbers 100, 101, 102, 103, and 104. EX1008, 2:50-53, Fig. 2. Each PE contains a central processing unit (CPU) and a local cache memory. EX1008, 2:50-53. PE 100 houses a real-time operating system that allocates tasks to the other PEs. EX1008, 2:53-56.



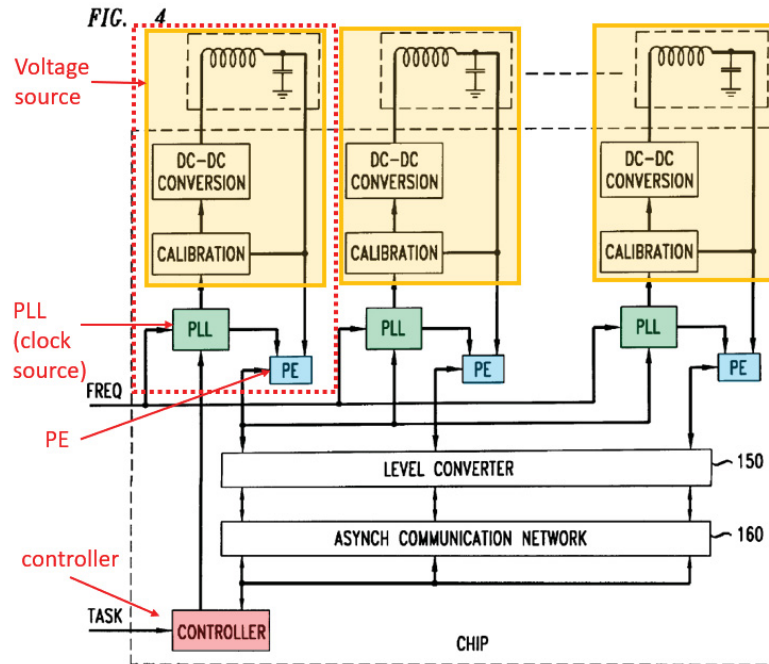
EX1008, Fig. 2.

219. Nicol explains that the load on the Figure 2 system varies with time and depends on the specific application being executed at any time. EX1008, 2:56-58. “For example, a set-top-box for a multimedia broadband access system might need to receive an HDTV signal. It could also be transmitting data from a computer, to the Internet, and responding to button requests from a remote control handset.” EX1008, 2:58-62. In other words, Nicol addresses the challenge of efficiently responding to changing demands on an electronic system.

220. When the system in Figure 2 is subject to a particular load, a scheduler within the real time operating system (RTOS) in PE 100 determines the best way to divide the tasks for that application to available PEs. EX1008, 3:10-18. “The intermediate goal [] is to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PEs.” EX1008, 3:19-21. In other words, the goal in the Figure 2 embodiment is to load the PEs as evenly as possible so that the task as a whole can be completed as fast as possible. EX1008, 3:47-49 (“That is, the presumption is that there is a certain time when the tasks assigned to the chip must be finished.”), 3:61-65 (“Thus, in a sense it is the expected completion time for the collection of assigned tasks that is controlling...”). Accordingly, the frequency for the PEs is set according to the number of PEs among which the task is divided. EX1008, 3:22-28 (“When an application that is running on the FIG. 2 system is subdivided into N concurrent task streams . . . then the clock frequency of

the FIG. 2 system can be reduced by a factor of N.”). Nicol explains that reducing the frequency in turn allows for the lowering of the supply voltage, further reducing power consumption. EX1008, 3:28-42.

221. Nicol further explains that there are applications where tasks cannot be divided into evenly-loaded threads as in Figure 2, requiring some PEs to operate at a higher operating frequency and voltage than others. EX1008, 5:60-65. The embodiment depicted in Figure 4 addresses this need by providing separate power domains and clock domains for each PE. EX1008, 5:66-6:2 (“A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.”). To this end, each PE is shown with an associated PLL (phase lock loop frequency synthesizer circuit) for clock generation, and a calibration circuit, DC-DC converter circuit and L-C circuit for voltage generation. *See* EX1008, 4:20-21, 5:66-6:11, Fig. 4. The separate PLL and voltage circuits allow individual control of the frequency and voltage of each PE. EX1008, 6:9-18, 6:29-32, 6:35-39.



EX1008, Fig. 4.

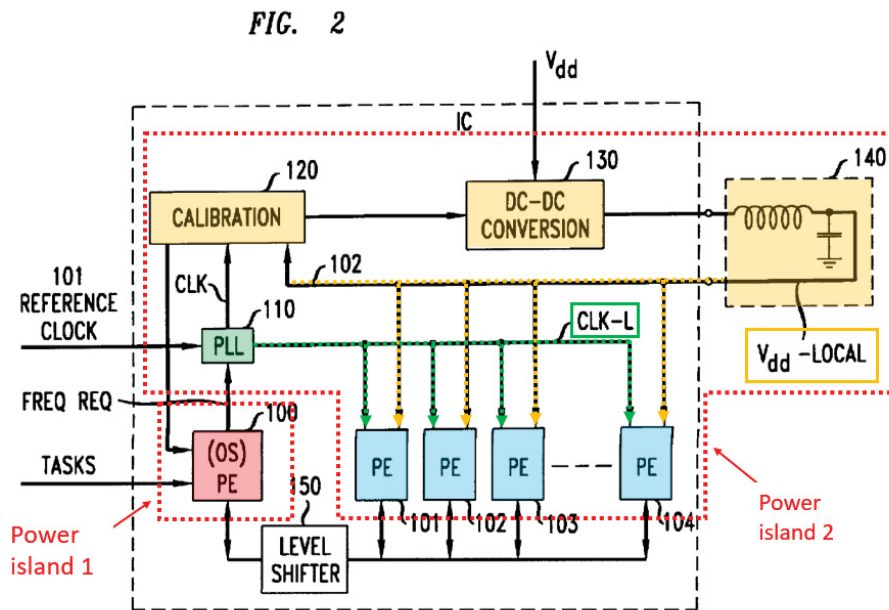
222. Unlike the embodiment in Figure 2, where there is a prescribed time within which assigned tasks must be finished and therefore the goal is to split the task completion times among the PEs as evenly as possible, EX1008, 3:47-49, 3:61-65, the goal in the Figure 4 embodiment is to minimize overall power consumption while ensuring adequate performance. For example, Nicol explains that in a computer system, a “fast memory” could be used when a new application is called, but then not be called again until a new application is opened. EX1008, 6:47-49. Therefore, the fast memory can be released at a leisurely pace in the interval at a lower frequency. EX1008, 6:50-52. This approach of adjusting the operation of components based on the needs and operation of the system results in overall power savings. EX1008, 6:52-56.

2. Claim 1

(a) Element 1[p]

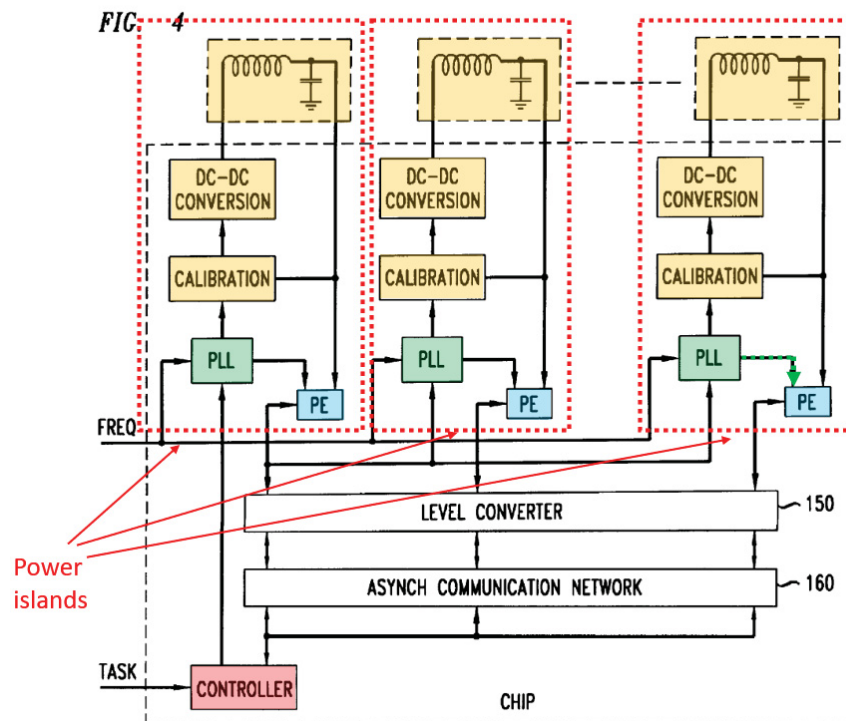
223. The preamble of claim 1 recites: “A method of managing power on an integrated circuit including a plurality of power islands, the method comprising.” Nicol discloses and/or renders obvious Element 1[p]. EX1008, 1:6-7 (“This invention relates to electronic circuits and, more particularly to power consumption within electronic circuits.”). Specifically, Nicol discloses improving performance of multi-processor chips by dynamically controlling the processing load of chips and controlling the frequencies and operating voltages of those chips to minimize overall power consumption. EX1008, Abstract, 2:18-22, 3:21-42. The “chip” refers to an integrated circuit, while “multi-processor” refers to multiple processors, or processing elements (PEs), on the integrated circuit. EX1008, 6:6-9 (“As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another *processing element* of the *integrated circuit* that contains the other processing elements.”), cl. 5 (“The method of claim 1, wherein said steps are executed in a *multiprocessor integrated circuit*.”); *see also* 7:15-19 (“It should further be noted that the power supply circuit need not have any elements outside the circuit itself (as depicted in FIG. 2). A skilled artisan would be aware that circuit design exists that can be manufactured wholly within an integrated circuit.”).

224. It would have been apparent or obvious to a POSITA that Nicol's integrated circuit includes a plurality of power islands. The '306 patent defines "power island" as "any section, delineation, partition, or division of the integrated circuit [] where power consumption is controlled within the section, delineation, partition, or division." EX1001, 3:51-54. In Figure 2, the PE 100 and PEs 101-104 form two different power islands as the two islands are powered independently. EX1008, 4:35 ("The V-local supply voltage is also applied to all of the PEs (excluding perhaps the operating system PE 100)."). Indeed, Nicol states that there is an "interface between the PEs 101-104 and PE 100[.]" EX1008, 5:46-47.



225. In the embodiment shown in Figure 4, each PE (along with its respective control circuitry) is a power island, because each has its independent voltage and clock source, allowing for independent power control by varying voltage

and frequency. EX1008, 5:66-6:2, Fig. 4. Further, a POSITA would have understood each PE (or group of PEs) as a section, delineation, partition, or division of Nicol's integrated circuit. See EX1008, Fig. 4. Nicol also explains that its discussion of "processing elements" may be applied to "components that are not typically thought of as processor elements," such as memory. EX1008, 6:34-41. A POSITA would have understood Nicol's flexible definition of "processing element" to map to the '306 patent's flexible definition of "power island." Moreover, I note that Nicol's PEs with capabilities of being independently controlled by varying both voltage and frequency also satisfy the narrow construction of "power islands" from the prior litigations. See, e.g., EX1013 at 23.



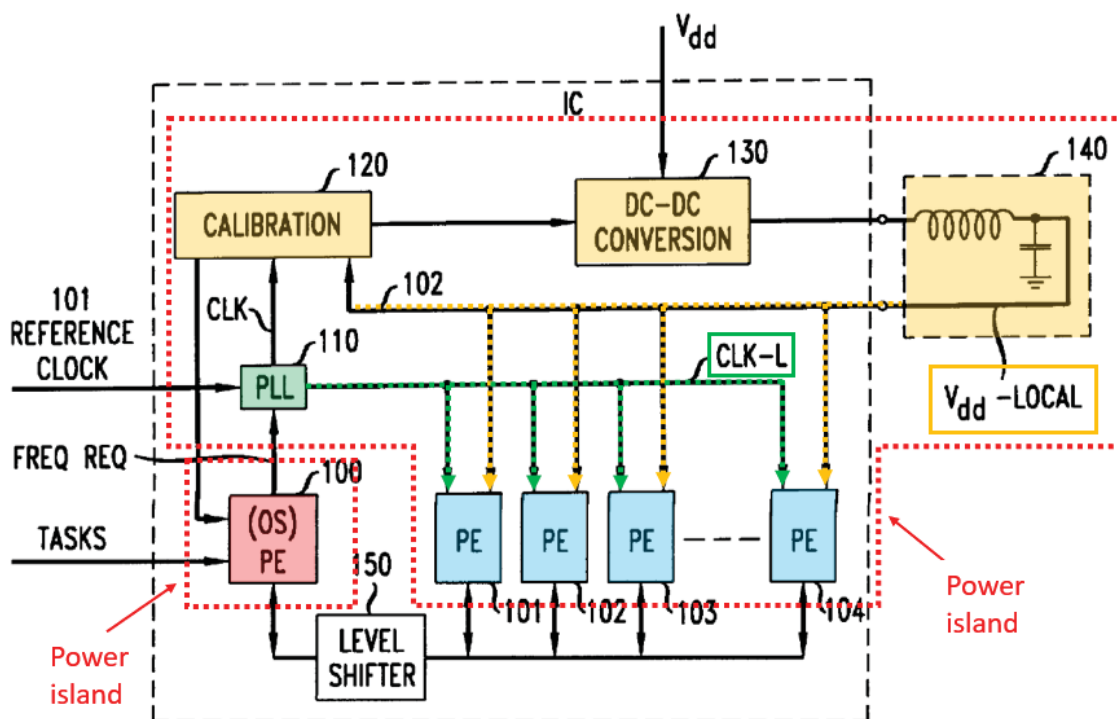
EX1008, Fig. 4.

(b) Element 1[a]

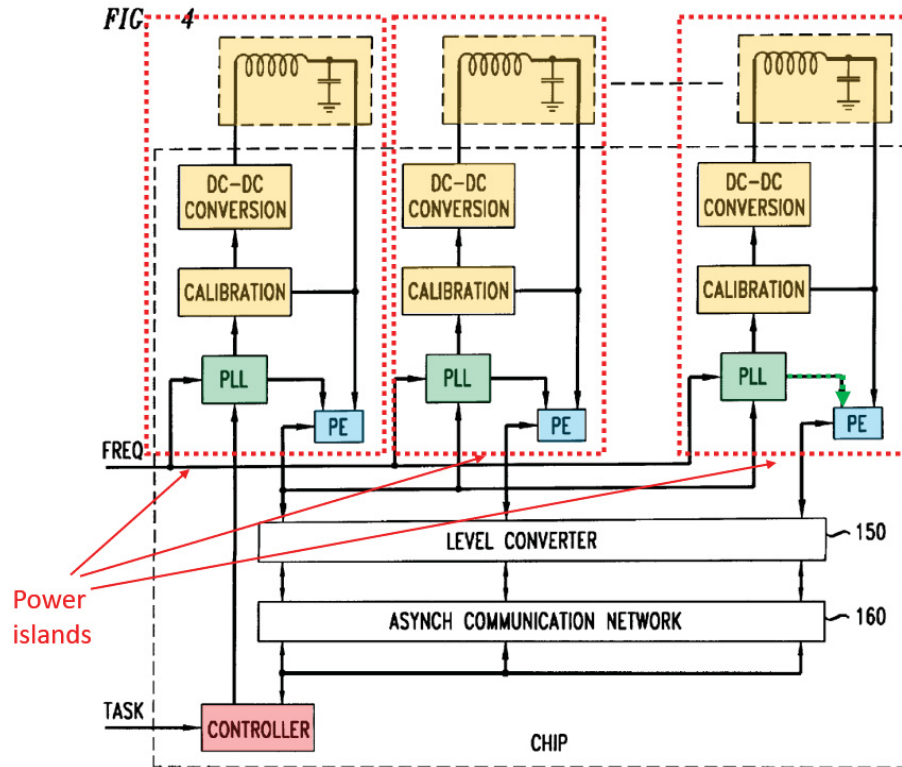
226. Claim Element 1[a] recites: “determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands.” Nicol discloses and/or renders obvious Element 1[a].

227. First, Nicol provides power islands whose power consumption is independently controlled, as discussed for Element 1[pre] and shown in the annotations in Figures 2 and 4 below.

FIG. 2



EX1008, Fig. 2.



EX1008, Fig. 4.

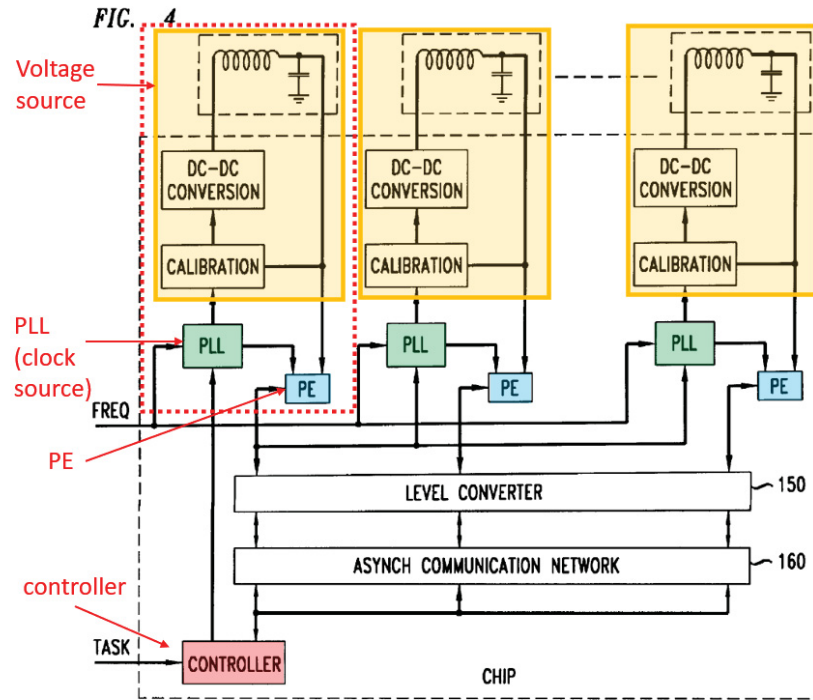
228. Nicol provides that power consumption is independently controlled within each power island. For example, Nicol explains that the frequency (line traced in green below) and/or voltage (line traced in orange below) within each power island can be altered to change the power consumption of the power island, both in the embodiment depicted in Figure 2 and in Figure 4. EX1008, 3:24-31 (“This allows the clock frequency of the PEs to be reduced . . . the clock frequency of the FIG. 2 system can be reduced by a factor of N. Reducing the frequency, as indicated above, allows reducing the necessary supply voltage, and reducing the supply voltage reduces the system’s power consumption (quadratically).”), 5:42-45 (“Of course, Vdd-local can only be reduced so far before the circuits start to fail, at

which the operating system employs gated clocking techniques to “shut down” PEs that are not needed.”), 5:66-6:2 (“A separate power supply for each PE in a chip [in FIG. 4] overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.”).

229. The ability for independent control is most explicit in the embodiment depicted in Figure 4, which shows that each PE has its own associated power and clock domains. EX1008, Fig. 4. Nicol explains:

The notion of adjusting operating frequency to load and adjusting supply voltage to track the operating frequency can be extended to allow each PE to have its own supply voltage. The benefit of this approach for some applications becomes apparent when it is realized that the chip-wise voltage scaling is most effective when the load of the computation can be evenly distributed across all of the PEs. In some applications, however, one may encounter tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE[s] within the multiprocessor would require a higher operating frequency and a higher operating voltage. This would require raising the frequency and voltage of the entire multiprocessor chip. A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.

EX1008, 5:66-6:2. Figure 4 shows the separate power supply and separate PLL for each PE, which enables the PEs to operate at distinct frequencies from others as the passage above explains.



EX1008, Fig. 4.

230. Second, Nicol provides determining a target power level for one of the power islands based on needs and operation of the integrated circuit. To start, as a general matter, with systems like Nicol’s that employ dynamic power management, the desired (and, thus, “target”) power level is the “minim[al] power under performance constraints.” EX1018 at 17; *see also* 1 (explaining that the dynamic power management methodology “reconfigures an electronic system to provide the requested services and performance levels with a minimum number of active components or a minimum load on such components”); *see* EX1001, 4:28-33

(explaining that “[t]he *target power level* is a *desired*, calculated, or specified power consumption”). Accordingly, Nicol’s disclosure seeks to achieve “[i]mproved performance of multi-processor chips...by dynamically controlling the processing load of chip and controlling...the operating voltages [and frequencies] of those chips so as to *minimize overall power consumption*.” EX1008, 2:18-22.

231. In Nicol, a POSITA would have appreciated that the determination of the target power level of a given PE is performed by the controlling operating system—e.g., the real time operating system (RTOS) in PE 100 in the Figure 2 embodiment and the operating system in the “controller” in the Figure 4 embodiment. Nicol describes the logic of determining the target power level in the Figure 2 embodiment:

Hence, the operating system of PE 100 needs to ascertain the required completion time, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and *adjust the clock frequency to insure [sic] that the most heavily loaded PE carries out its assigned tasks within the required completion time*. Once the frequency is thus determined, a minimum supply voltage can be determined.

EX1008, 3:66-4:6. So, in the Figure 2 system, the target power level is set “to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PE’s.” EX1008, 3:19-21. In other words, the objective (or

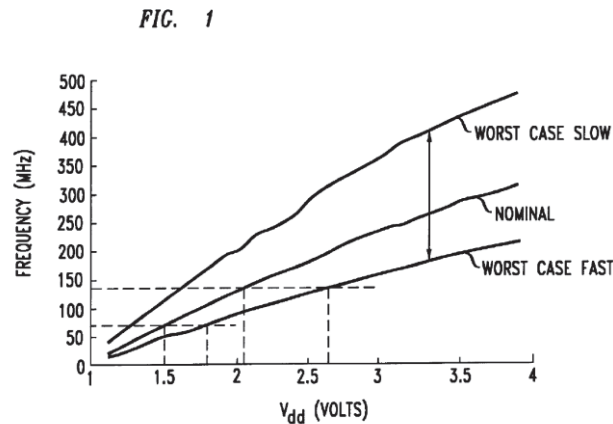
“needs and operation”) in the Figure 2 system is to load the PEs as evenly as possible so that the task in its entirety can be completed within a required amount of time. EX1008, 3:47-49 (“That is, the presumption is that there is a certain time when the tasks assigned to the chip must be finished.”), 3:61-65 (“Thus, in a sense it is the expected completion time for the collection of assigned tasks that is controlling...”). Accordingly, the frequency for the PEs is set according to the number of PEs among which the task is divided. EX1008, 3:22-28 (“When an application that is running on the FIG. 2 system is subdivided into N concurrent task streams . . . then the clock frequency of the FIG. 2 system can be reduced by a factor of N.”), 5:23-29, cl. 1 (“determining a lowest frequency”), cl. 46 (“frequency is set to a minimum level”).

232. Nicol also discusses how the target voltage can be set:

Once the frequency is thus determined, a minimum supply voltage can be determined. The supply voltage determination can be made by reference to a plot like the one shown in FIG. 1 or, advantageously, by evaluating the actual performance of the multiprocessor at hand. As indicated above, the operating system can reduce the supply voltage even further by tracking temperature and process variations. For example, when the chip is nominal in its characteristics, then it can be operated along line 20 of FIG. 1, which calls for only 1.5V supply when operating at 70 MHz.

EX1008, 4:5-16. Here, Nicol explains that the target voltage can be set based on a worst-case-slow or worst-case-fast plot like that shown in Figure 1 which maps

power parameters to desired performance levels, by evaluating the actual performance of the microprocessor, or by tracking temperature and process variations. These are all examples of “needs and operation” of the integrated circuit.



EX1008, Fig. 1.

233. In the context of the embodiment in Figure 4, Nicol discusses an example for determining a target power level in a personal computer system:

For example, there is a current often-used practice to maintain program code and data for different applications of a personal computer in a fast memory. As each new application is called, more information is stored in the fast memory, until that memory is filled. Thereafter, when a new application is called, some of the information in the fast memory is discarded, some other information is placed in the slower hard drive, and the released memory is populated with the new application. *It is possible to anticipate that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called.* When so anticipated, some of the fast memory can be released (storing some of the data that needed to be remembered) at a leisurely pace. That is,

lower clock frequency can be employed in connection with the fast memory and the hard drive, with a *corresponding lower supply voltage*, resulting in an overall power saving in both the memory's operation and in the operation of the hard drive.

EX1008, 6:39-56. This passage gives an example of setting a target power level (by lowering clock frequency and supply voltage) for a power island (fast memory, hard drive) based on needs and operation of the integrated circuit (anticipating that the memory stored in the fast memory can be discarded, such that the fast memory can be released at a leisurely pace).

234. As should by now be apparent, a POSITA would have appreciated or found obvious that Nicol's above-discussed disclosure of adjusting the operating frequency and/or supply voltage of multiple PEs in order to minimize overall power consumption while meeting certain performance constraints involves determining a target power level. Indeed, because of power's direct relationship with frequency and quadratic relationship with voltage, the kinds of voltage and frequency scaling actions that Nicol describes were well understood in the art as mechanisms for dynamic power management to reach targeted levels of power consumption. *See, e.g.,* EX1018 at 12 ("For components that are in an active state but whose response is not performance critical, *power consumption* can be traded off for performance *by reducing the clock frequency or the supply voltage*. The latter solution is usually preferred because of the quadratic dependence of power consumption on supply

voltage, and it is often combined with frequency downscaling.”); EX1006, 1:19-23; EX1007, 1:52-59. In addition, a POSITA would have understood that Nicol’s specific approach of setting and achieving a target power level is consistent with that of the ’306 patent. Like Nicol, the ’306 patent also discusses changing frequency (or other parameters such as supply voltage or threshold voltage) to accomplish changing the power consumption level of a power island to a target power level based on performance requirements. EX1001, 7:38-50, Fig. 5 (“the application determines the required frequency for performance of an IP unit” and “[t]he PMCL...selects a frequency rate, Vdd, and Vt if applicable for the unit that best meets the given requirements”).

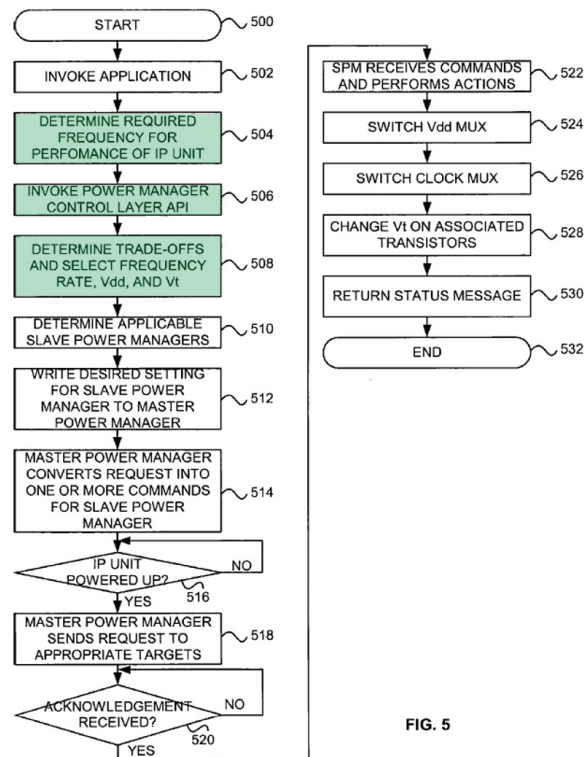


FIG. 5

EX1001, Fig. 5.

235. Figure 5 in the '306 patent shows “[i]n step 502, an application is invoked such as playing a movie. In step 504, the application *determines the required frequency* for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder.” EX1001, 7:41-46. Then, “[t]he PMCL 218 determines possible trade-offs available for the unit and *selects a frequency rate, Vdd, and Vt* if applicable for the unit that best meets the given requirements in step 508 and determines the applicable SPMs 264 and 274 in step 510.” EX1001, 7:62-66; *see also* EX1001, 8:56-9:26, Fig. 8 (similar). A POSITA would have understood that the '306 patent illustrates determining a “target power level” through adjusting parameters such as frequency, Vdd, or Vt, relying on these parameters’ proxy relationship with power consumption. *See, e.g.*, EX1001, 5:31-36 (“The PMCL 218 also collects information from the MPM 280 and provides commands to the MPM 280 for possible IPMs, SPMs 264 and 274, and the power islands 260 and 270. Some of the commands may be to power on/off, *change the power level*, or *change the frequency* of the power islands 260 and 270.”); 7:46-48 (“In some embodiments, when the IP unit is totally asynchronous, *the required frequency will be an artificial*

measure of performance.”).⁷ Therefore, a POSITA would have understood that Nicol, like the ’306 patent, provides a method for determining a target power level based on needs and operation of the integrated circuit using variables such as operating frequency or supply voltage.

236. On the limitation “based on needs and operation of the integrated circuit,” I understand that in prior litigations involving the ’306 patent, the parties in those litigations agreed to a construction of “based on future operational needs and current operating status of the integrated circuit.” EX1011 at 48; EX1012 at 9. It is my opinion that no construction of this limitation is needed because the plain and ordinary meaning suffices. The ’306 patent itself does not provide explanation of this phrase aside from reciting it twice in the specification. EX1001, 2:14-16, 4:28-

⁷ Notably, the ’306 patent does not explicitly discuss examples that involve measuring power consumption level via measuring current and multiplying it with voltage, which a POSITA would have understood to be a more accurate, albeit costlier, method of measuring power consumption. See EX1006 at 13:2-8 (“Different techniques may be used to not exceed power consumption levels. A simple but imprecise way is to not allow the supply voltage, threshold voltages, or frequency, to pass certain levels. A more precise way is to detect current being consumed. The power can be determined from the current and supply voltage.”).

31. The '306 patent simply provides examples of determining parameters such as required frequency, supply voltage, or threshold voltage, given a particular application. EX1001, 7:38-50, 8:56-62. As explained above, Nicol's disclosures mirror the approach that the '306 patent takes with respect to setting a target power level "based on needs and operation of the integrated circuit."

237. Additionally, while there is no briefing regarding the prior-agreed upon construction in the *Freescale* (EX1011), *Conversant* (EX1012), and *MediaTek* (EX1013) litigations, it is my opinion that Nicol, in light of a POSITA's knowledge, also satisfies that construction for the reasons discussed above. For example, Nicol's discussion that its system can "*anticipate* that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called" such that "lower clock frequency can be employed in connection with the fast memory and the hard drive," (EX1008, 6:39-56), shows that it responds to "future operational needs." Similarly, Nicol's explanation of the system's ability to set the lowest corresponding frequency and voltage needed for operational performance requirements shows that it responds to "current operational status" of the integrated circuit. EX1008, Abstract, 2:22-27, 4:54-6:2, cl. 1.

(c) **Element 1[b]**

238. Claim Element 1[b] recites: “determining at least one of actions to change a power consumption level of the one of the power islands to the target power level.” Nicol discloses and/or renders obvious Element 1[b].

239. Consistent with my prior explanation at Elements 1[a]-1[p] (which I incorporate herein), Nicol discloses and/or renders obvious changing the clock frequency and/or voltage of the PEs to adjust their power consumption levels to the target power level that minimizes power consumption in view of performance constraints. EX1008, 2:18-22 (“Improved performance of multi-processor chips is achieved by dynamically controlling . . . the operating voltages of those chips so as to *minimize overall power consumption*.”), 2:24-27 (“[T]he controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage.”). As Nicol explains, power consumption can be changed by altering the clock frequency and/or voltage. EX1008, 1:27-36 (“The power consumption of a CMOS circuit increases linearly with operating frequency and quadratically with supply voltage.”), 3:28-31 (“Reducing the frequency, as indicated above, allows reducing the necessary supply voltage, and reducing the supply voltage reduces the system's power consumption (quadratically).”). This principle was well understood by persons of ordinary skill in the art: that power changes linearly with frequency, and quadratically with

voltage. *See, e.g.*, EX1018 at 12 (“For components that are in an active state but whose response is not performance critical, power consumption can be traded off for performance by reducing the clock frequency or the supply voltage. The latter solution is usually preferred because of the quadratic dependence of power consumption on supply voltage, and it is often combined with frequency downscaling.”); *supra* Section VI.A.1. As explained above for Element 1[a], these actions described in Nicol—changing frequency and/or voltage—are the precise examples contemplated by the ’306 patent to change the power consumption level of a power island. *See* EX1001, 5:31-36, 7:34-50, 7:62-8:8, Fig. 5.

240. As explained for Element 1[a], in the embodiment shown in Figure 2, Nicol sets the target power level to be the lowest possible (via frequency and/or supply voltage) while ensuring that the task gets completed by the required deadline:

When an application that is running on the FIG. 2 system is subdivided into N concurrent task streams, as suggested above, each of the PEs become lightly loaded. This allows the clock frequency of the PEs to be reduced, and if the task division can be carried out perfectly, ***then the clock frequency of the FIG. 2 system can be reduced by a factor of N .*** Reducing the frequency, as indicated above, allows ***reducing the necessary supply voltage***, and reducing the supply voltage reduces the system’s power consumption (quadratically).

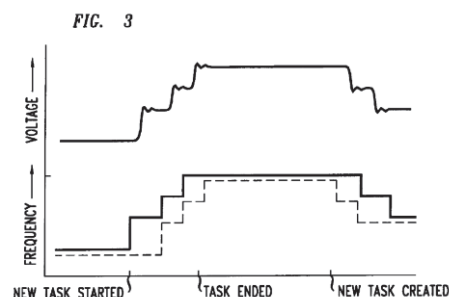
EX1008, 3:22-31. *See also* EX1008, 3:66-4:10 (similar). Nicol continues with an example:

To illustrate, if a given application that is executed on 1 PE requires operating the PE at 140 MHz, it is known from FIG. 1 that the PE can be operated at approximately a 2.7V supply. When the application is divided into two concurrent tasks and assigned to two PEs that are designed to operate at 140 MHz from a 2.7V supply, ***then the PEs can be operated at 70 MHz and at a supply voltage of 1.8V***. This reduction in operating voltage represents a power saving of 55%. Of course, it is unlikely that an application can be perfectly divided into two equal load task streams and, therefore, the 55% power saving is the maximum achievable power saving for two PEs.

EX1008, 3:31-42. Therefore, Nicol discloses determining an action, namely changing frequency and voltage, to bring the power consumption of a power island to the target minimum power level.

241. Nicol further describes the timing of changing frequency and voltage to the target power level, *i.e.*, the appropriate frequency and/or voltage to match the load when a task is being started and when the task has completed. Figure 3 “demonstrates the timing associated with increasing Clk, Clk-L and Vdd-local when a new task is created and the load on the multiprocessor is thus increased[.]”

EX1008, 4:54-58.



EX1008, Fig. 3.

“It shows the system operating at 70 MHz from a 1.8V supply when the load is increased in three steps to 140 MHz. When the 2.7V supply is stable, as shown by the supply voltage plot, the new task is enabled for execution. Some time thereafter according to Fig. 3, a task completes, which reduces the load on the multiprocessor. The reduced load permits lowering the clock frequency to 100 MHz and lowering the supply voltage to 2.1V.” EX1008, 4:54-58. This passage demonstrates how Nicol’s system determines an action (changing frequency, and subsequently voltage), to react to the load on the PE at a given time.

242. Nicol similarly determines an action to change the power consumption level to the target power level in the Figure 4 embodiment. EX1008, 5:66-6:2 (“A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to *independently program the lowest operating frequency and corresponding lowest supply voltage* for each PE.”). As discussed above, Nicol gives an example of setting a target power level (by determining a lower clock frequency) for a power island (fast memory) based on needs and operation of the integrated circuit (anticipating that the memory stored in the fast memory can be discarded, such that the fast memory can be released at a leisurely pace.). EX1008, 6:39-56.

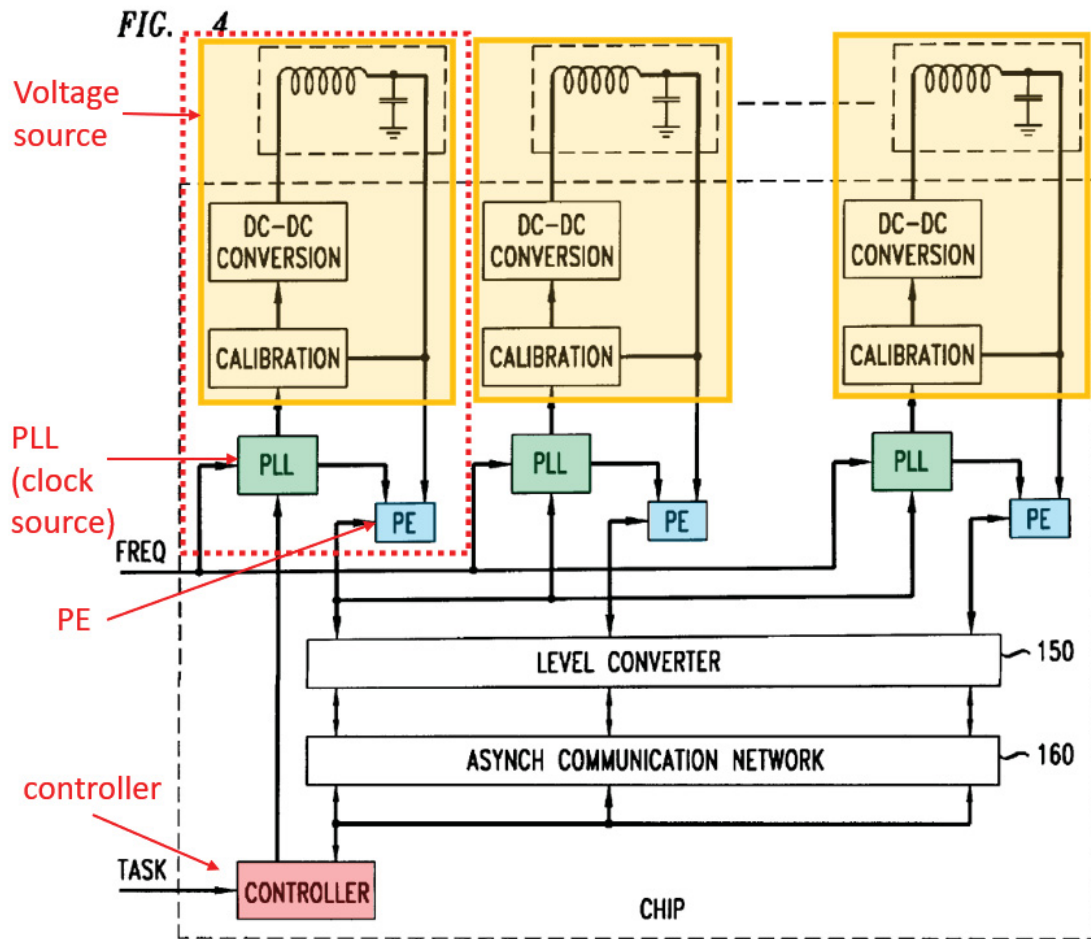
(d) **Element 1[c]**

243. Element 1[c] recites: “performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” Nicol discloses and/or renders obvious Element 1[c] for the reasons I discussed above at Element 1[b] (which I incorporate herein). Again, as discussed, Nicol teaches (or at least renders obvious) performing an action such as changing the frequency and/or voltage of the PEs to change the power consumption level to a target power level. EX1008, 3:21-31 (“When an application that is running on the FIG. 2 system is subdivided into N concurrent task streams, as suggested above, each of the PEs become lightly loaded. This *allows the clock frequency of the PEs to be reduced* . . . the clock frequency of the FIG. 2 system can be reduced by a factor of N.”), 3:66-4:6 (“Hence, the operating system of PE 100 needs to ascertain the required completion time, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and *adjust the clock frequency* to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time.”), 4:54-58 (“FIG. 3 demonstrates the timing associated with *increasing Clk, Clk-L and V_{dd-local}* when a new task is created and the load on the multiprocessor is thus increased, and the timing associated with *decreasing Clk, Clk-L and V_{dd-}*

local when the load on the multiprocessor is decreased.”), 5:66-6:2 (“A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently *program the lowest operating frequency and corresponding lowest supply voltage* for each PE.”).

3. Claim 2

244. Claim 2 recites: “The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit.” Nicol discloses and/or renders obvious this claim. For example, Figure 4 shows that each PE has its own associated power supply and clock supply, and a POSITA would have understood that each PE would have to be placed close to its respective power supply. EX1008, Fig. 4. A POSITA would have understood from basic circuit design principles that a power island should be placed geographically close to its corresponding power source to minimize signal deterioration and power dissipation, for better routing of power supply and signals, and optimization of performance and power. *See, e.g.*, EX1017 at 88 (“Moreover, the layout of power the distribution grid is often carefully designed for maximum efficiency”); EX1019 at 7 (“Voltage Islands must be floorplanned (placed) in close proximity with the chip pins corresponding to its off-chip power source.”). In my opinion, it would have been obvious to a POSITA to delineate power islands based on geographic factors of the integrated circuit to comport with basic circuit design principles.



EX1008, Fig. 4.

245. The same is true of Figure 2, where the power islands shown below would be delineated based on geographic factors because of the PEs 101-104 receiving a common clock and voltage source. Again, according to basic circuit design principles, the power island containing PEs 101-104 would be geographically grouped together to improve routing of supply and control signals. Indeed, Nicol mentions an “interface” between PEs 101-104 and PE 100, indicating that the power islands are separated by geographic factors. EX1008, 5:44-49.

[illegible]

4. Claim 3

247. First, it would have been obvious to a POSITA that Nicol's PEs (power islands in the Figure 4 embodiment) were delineated based on functional circuitry. The PEs are assigned different tasks, which means they can execute different functions and most likely vary in the type of task that they are typically assigned. See EX1008, 2:53-56 ("A real-time operating system resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications."),

3:66-4:5 (“Hence, the operating system of PE 100 needs to ascertain the required completion time, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time.”), 5:23-29 (“As more tasks are entered into the ‘to-do’ list, the operating system of PE 100 computes the correct way to balance the additional computational requirements and allocates the tasks to the processors.”). For example, one PE could be a CPU, another PE could be a microcontroller, and another PE could be a GPU. *See, e.g.*, EX1022 (Dutta) at 21-24 (describing multiprocessor SOC containing multiple CPU cores, transport stream processor, video-processing blocks, and more). Each of these processing elements are differentiated by their functional circuitry. Indeed, the ability of the processing elements to execute tasks separately motivates the provision of individual power and clock source in the first place. EX1008, 5:66-6:2 (“A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.”).

248. Further, the term “processing element” implies that each element can be defined by the particular type of processing function it performs. For example, a textbook published in 1991 defines “processing element” as “any hardware element

that is primary used for processing data (i.e., accepting data, performing some operation on the data, and returning results). EX1025 at 4. Another textbook on multimedia information network published in 1998 uses the term “processing element” as “any device that has the ability to process information,” and specifically notes that “[t]he instructions of a PE represent the processing functions that the PE can perform.” EX1026 at 3-4. The text shows a CPU, “Math Coprocessor,” and “Network Interface Card” as examples of “processing elements.” These components are well-understood to be divergent in their functional circuitry because they are specifically designed for their tasks. EX1026 at 3.

249. Additionally, it would have been obvious to a POSITA that the power islands in Figure 2 are also delineated based on functional circuitry. Because “[a] real-time operating system resides in PE 100,” (EX1008, 2:53-56), a POSITA would have understood that PE 100 would have required some functional circuitry distinct from the functional circuitry of PEs 101-104, such as a real-time operating system kernel.

5. Claim 4

250. Claim 4 recites: “The method of claim 1 wherein the power islands comprise power sub-islands.”⁸ Nicol discloses and/or renders obvious this claim.

251. In Nicol, the power island in the Figure 2 embodiment comprises PEs 101-104. It would have been obvious for a POSITA to configure the system so that each PE within the power island containing PEs 101-104 functions as a “sub-island” whose power can be further controlled. For example, “each PE contains a central processing unit (CPU) and a local cache memory (not shown).” EX1008, 2:52-53. It would have been obvious to a POSITA that each PE having its own CPU would enable individual control, e.g., by clock or power gating, in circumstances where the load between the PEs is not perfectly divided. *See* EX1008, 3:22-42 (“Of course it is unlikely that an application can be perfectly divided...”). Thus, the POSITA would have understood that establishing each PE as its own sub-power island would have been predictably advantageous in the sense of enabling more fine-grained dynamic power management policies capable of achieving greater power savings. As one example that would have been apparent to a POSITA, establishing each PE

⁸ Note that the '306 patent states that, in some embodiments, power islands comprise sub-islands to provide further specificity in controlling power in the integrated circuit. EX1001, 3:63-66.

as its own sub-power island capable of independent power management is beneficial in situations where the PEs are running different applications, some of which have higher demands than others.

252. Further, it would have been obvious to a POSITA that Nicol's processing elements (power islands in the Figure 4 embodiment) themselves comprise sub-units whose power can further be controlled. For example, a CPU is one example of a PE. *See, e.g.*, EX1026 at 3. In a CPU, there are often multiple functional units, such as cores or latches, that can be turned on and off individually. As another example, in a digital signal processor there are many functional units such as an arithmetic logic unit, memory units, or I/O interfaces, whose power can be controlled separately, such as by clock or power gating. As another example, a general-purpose processor (power island) could have multiple accelerators such as image processor or audio processor (sub-islands), each with its own frequency control. *See* EX1017 at 77 ("For instance, high-performance microprocessors contain a massive amount of hardware resources which are not always used.").

253. A POSITA would have been motivated to implement power sub-islands based on Nicol's teachings on power management at different levels. Nicol teaches that "PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage." EX1008, 6:66-7:3. This teaching is in line with the general understanding in the art that

dynamic power management could be implemented at different levels of abstraction, as discussed in the Background of the Technology Section. *Supra*, Section VI.A.3; EX1017 at 221 (“Dynamic power management is a technique that spans multiple level of abstraction (from the logic level to the system level).”); EX1018 at 2 (“A component is an atomic block in a complete system. Notice that the granularity of this definition is arbitrary, hence components can be as simple as a functional unit within a chip, or as complex as a board.”). A POSITA would have understood that it would have been beneficial, and conventional, to implement power management at different levels of Nicol’s system, including sub-components within PEs.

6. Claim 5

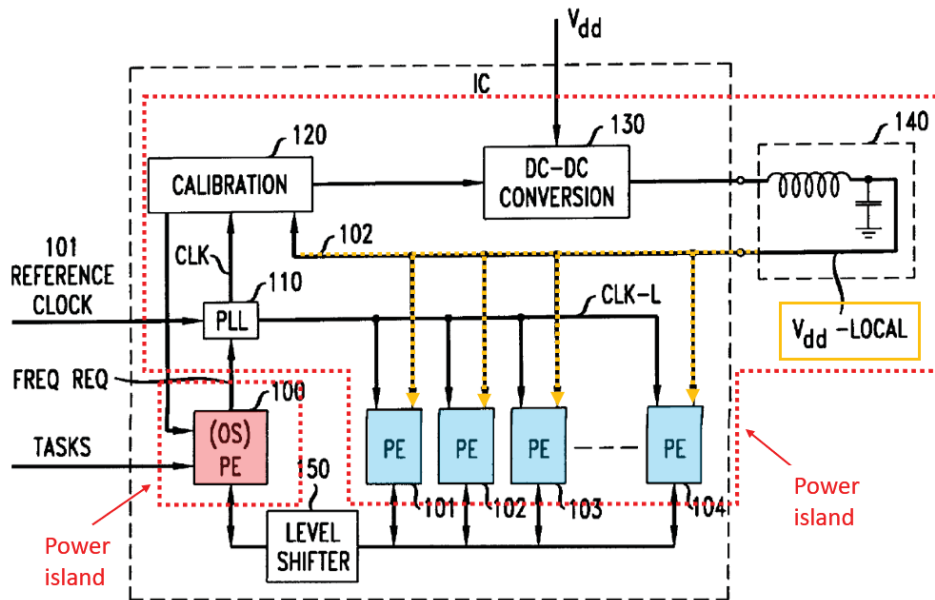
254. Claim 5 recites: “The method of claim 1 wherein the power islands comprises multiple clock domains.” Nicol discloses and/or renders obvious this claim. As discussed above for claim 4 (which I incorporate herein), a POSITA would have understood that each PE comprises multiple sub-units that can be controlled independently, such as via clock gating and frequency control. Similarly, such sub-units within the PEs would each provide multiple distinct clock domains.

7. Claim 7

255. Claim 7 recites: “The method of claim 1 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.” Nicol discloses and/or renders obvious this claim.

256. In the Figure 2 embodiment, Nicol teaches changing V_{dd} -local which supplies PEs 101-104 in the power island.

FIG. 2

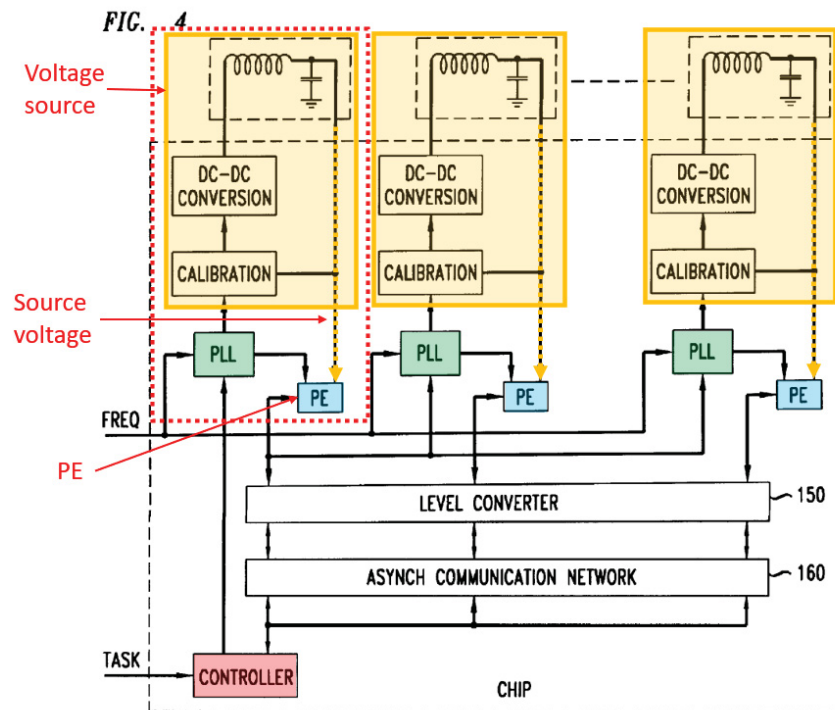


EX1008, Fig. 2.

See also EX1008, 3:28-31 (“Reducing the frequency, as indicated above, **allows reducing the necessary supply voltage**, and reducing the supply voltage reduces the system’s power consumption (quadratically).”), 3:31-42 (discussing example of lowering supply voltage from 2.7V to 1.8V to result in a power saving of 55%), 4:5-16 (discussing determining the target voltage by using a frequency-voltage “worst-case-fast” plot, by evaluating the actual performance of the multiprocessor, or by tracking temperature and process variations), 4:54-5:22 (describing process for calculating new V_{dd} -local when load on PEs is changed), 5:44-49 (“Of course, the fact that supply voltage V_{dd} -local varies as a function of load should be accounted for in the interface between the PEs 101-104 and PE 100[.]”), cl. 1 (“1. A method

executed within a system for controlling power consumption of a sub-circuit of said system comprising the steps of: ... based on characteristics of the sub-circuit, **setting a supply voltage that is applied to the sub-circuit** to a lowest level that insures proper operation of the sub-circuit at the determined frequency.”).

257. In the Figure 4 embodiment, Nicol teaches changing the supply voltage for each PE. Nicol explicitly teaches that “[a] separate power supply for each PE in a chip” allows for independently programming the “corresponding lowest supply voltage” for each PE and, thus, each power island. EX1008, 5:66-6:2, Fig. 4.

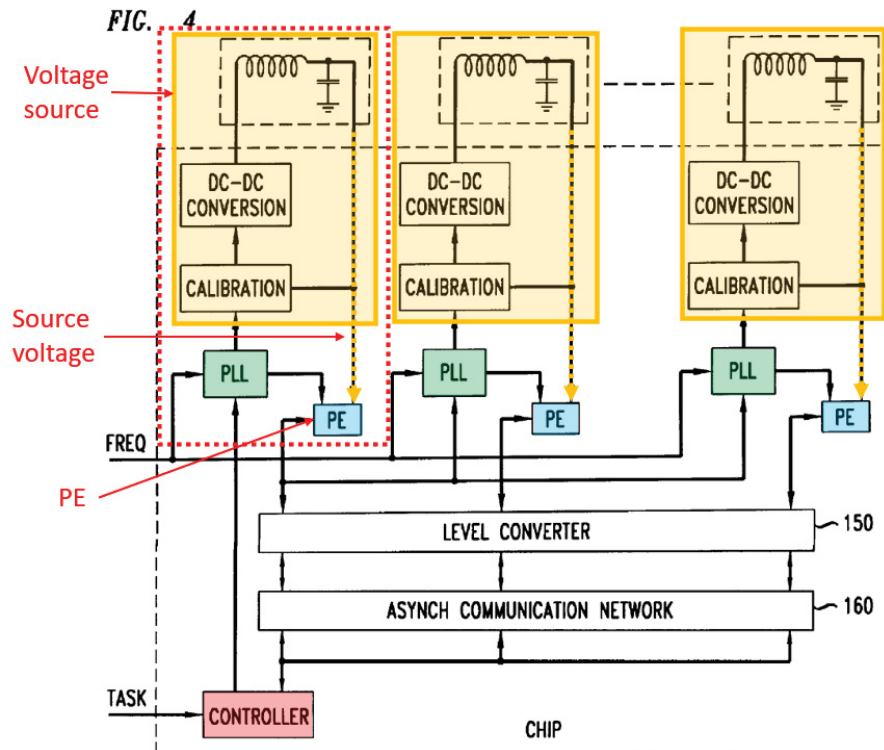


EX1008, Fig. 4.

8. Claim 8

258. Claim 8 recites: “The method of claim 7 wherein the first voltage comprises a source voltage.” Nicol discloses and/or renders obvious this claim.

259. Both V_{dd} -local in Figure 2 and the voltages supplied to each PE in Figure 4 are “source voltages.” More specifically, a POSITA would have understood that V_{dd} -local is a source voltage for PEs 101-104 which comprise a power island in Figure 2, and that the “supply voltage” provided to the PEs within the power islands of Figure 4 (annotated below) are likewise source voltages. In each case, the voltage is supplied to the PE from a source via a DC-DC converter, a calibration circuit, and an L-C circuit, which allows the PE to operate.



EX1008, Fig. 4.

See EX1008, 3:28-31 (“Reducing the frequency, as indicated above, *allows reducing the necessary supply voltage*, and reducing the supply voltage reduces the system's power consumption (quadratically).”), 3:31-42 (discussing example of

lowering supply voltage from 2.7V to 1.8V to result in a power saving of 55%), 4:5-16 (discussing determining the target supply voltage using a frequency-voltage “worst-case-fast” plot, evaluating the actual performance of the multiprocessor, or tracking temperature and process variations), 5:66-6:2 (“A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest *supply voltage* for each PE.”), cl. 1 (“1. A method executed within a system for controlling power consumption of a sub-circuit of said system comprising the steps of: ... based on characteristics of the sub-circuit, *setting a supply voltage that is applied to the sub-circuit* to a lowest level that insures proper operation of the sub-circuit at the determined frequency.”).

9. Claim 9

260. Claim 9 recites: “The method of claim 7 wherein the first voltage comprises a threshold voltage.” Nicol renders this claim obvious.

261. In my opinion, it would have been obvious to a POSITA in light of Nicol to change a threshold voltage to change the power consumption level of a power island to a target power level. In the background section, Nicol discusses “Variable Supply-Voltage Scheme for Low Power High-Speed COMS Digital Design,” by Kuroda et al. (EX1016) which demonstrates that tuning threshold voltages as supply voltage is lowered helps minimize speed degradation. EX1008,

1:65-2:6. Nicol explains that “[t]he tuning [of threshold voltages] is achieved on-chip by varying the substrate-bias voltage. These techniques are needed to ensure that the leakage current, which increasing as the threshold voltage is reduced, does not become too large.” EX1008, 2:7-10. This discussion clearly demonstrates that a POSITA would have understood the benefits of tuning the threshold voltage in power management mechanisms.

262. Even though the discussion of the Kuroda article focuses on using threshold voltage to minimize speed degradation, it was widely known in the art that threshold voltage could be changed, often in conjunction with supply voltage, as in Kuroda, to change the power consumption level of the relevant component or area. Indeed, the 2000 survey article by Benini et al. explains how threshold-voltage adjustment was used to implement dynamic voltage change: “The variable supply voltage approach can be complemented by dynamic threshold-voltage adjustment, achieved by controlling the body back bias.” EX1018 at 13. Thus, it would have been obvious to a POSITA, in light of Nicol’s discussion of the existing art and the importance of minimizing leakage power, to include changing a threshold voltage as an action to change the power level of a power island.

10. Claim 11

263. Claim 11 recites: “The method of claim 1 wherein another one of the actions comprises powering off the one of the power islands.” Nicol discloses and/or

renders obvious this claim. For example, Nicol’s claim 36 recites “The apparatus of claim 32 further comprising means within said controller for *turning supply power off* to at least one of said N processing elements.” EX1008, cl. 36. Applying this to the embodiments, a POSITA would have understood that the voltage provision circuit including DC-DC converter and L-C regulator allows for the power island consisting of PEs 101-104 in Figure 2, and each of the PE/power islands in Figure 4, to be powered off via a simple power off command. Further, Nicol explains that it teaches controlling operating voltages with “significantly greater than on/off granularity,” demonstrating that turning a component on and off was well-known in the art, and that Nicol’s frequency- and voltage-changing mechanism was providing a finer level of control than that. EX1008, Abstract, 2:18-31; *see also* EX1018 at 1 (“An example of a simple policy, ubiquitously used for laptops and palmtops, is the timeout policy, which shuts down a component after a fixed inactivity time[.]”); EX1024 at 31 (“Components can be selectively turned off to save energy; however, because turning a component on again may consume both time and energy, the decision to turn it off must be made carefully. Statistical methods based on Markov models can be used to create effective system-level power management methodologies.”). Therefore, a POSITA would have understood that Nicol’s PEs could be powered off in the power management process.

11. Claim 16

(a) Element 16[p]

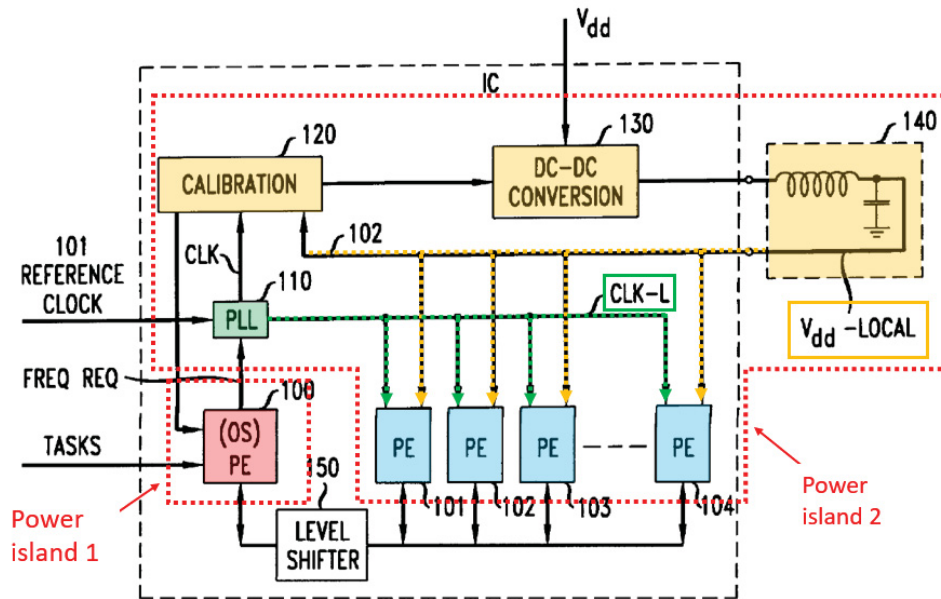
264. Element 16[p] recites: “A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising.” Nicol discloses and/or renders obvious Element 16[p] for at least the reasons discussed above with respect to claim Element 1[p] through 1[c], the discussions for which I incorporate herein. Nicol additionally discloses a “system” because it discusses not only a power management mechanism, but also the circuit(s) for carrying out said mechanism. *See* EX1008, 2:50-58 (“the FIG. 2 system”), 5:66-6:12, Figs. 2, 4, cl. 17.

(b) Element 16[a]

265. Element 16[a] recites: “power control circuitry configured to control power for one of the power islands.” Nicol discloses and/or renders obvious Element 16[a]. In Nicol’s Figure 2 embodiment, the voltage conversion circuitry (which includes the calibration circuit, DC-DC conversion, and the L-C circuit) and the PLL constitute the “power control circuitry” because they control the supply voltage and frequency, respectively, of the power island. EX1008, 4:17-37, Fig. 2. The “level shifter” also constitutes part of the power control circuitry because it “converts between the voltage level of PEs 101-104 and the voltage level of PE 100.” EX1008, 5:45-51; *see also* EX1008, 7:9-14 (“It should also be noted that level converter 150 is interposed in FIG. 2 between PE 100 and the other PEs because PE 100 is

operating off V_{dd} . PE 100 can also be operated off V_{dd} -local, in which case the level converter is interposed between PE 100 and the input/output port of the FIG. 2 circuits that interacts with PE 100.”).

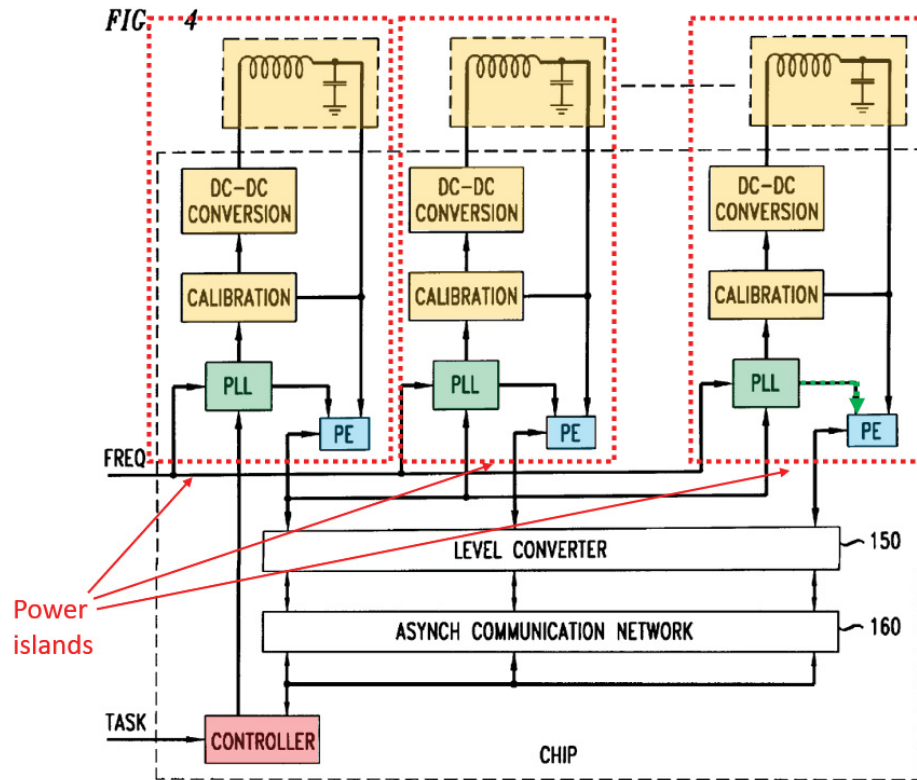
FIG. 2



EX1008, Fig. 2.

266. In Nicol’s Figure 4 embodiment, the voltage control circuitry and the PLL associated with each PE is the “power control circuitry,” as it controls the supply voltage and frequency, respectively, of each power island. EX1008, 4:17-37, Fig. 4. The “level converter” and “asynchronous communication network” are also part of the “power control circuitry,” as the level converter “converts the various voltage swings of the PEs to a fixed level swing” (EX1008, 6:29-32; *see also* EX1008, 5:49-52 (“This is accomplished with level converter 150, which is quite conventional[.]”)), and the asynchronous communication network “resolves the

issue of different clock domains” by synchronizing the clock frequency, (EX1008, 6:29-33).



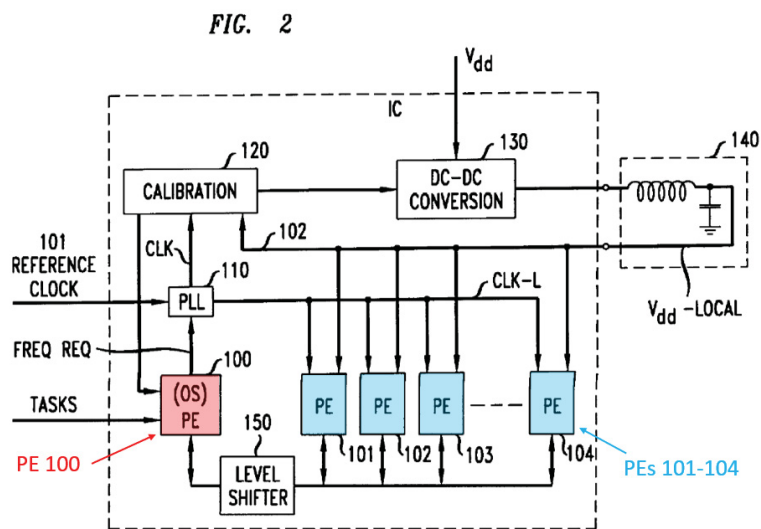
EX1008, Fig. 4.

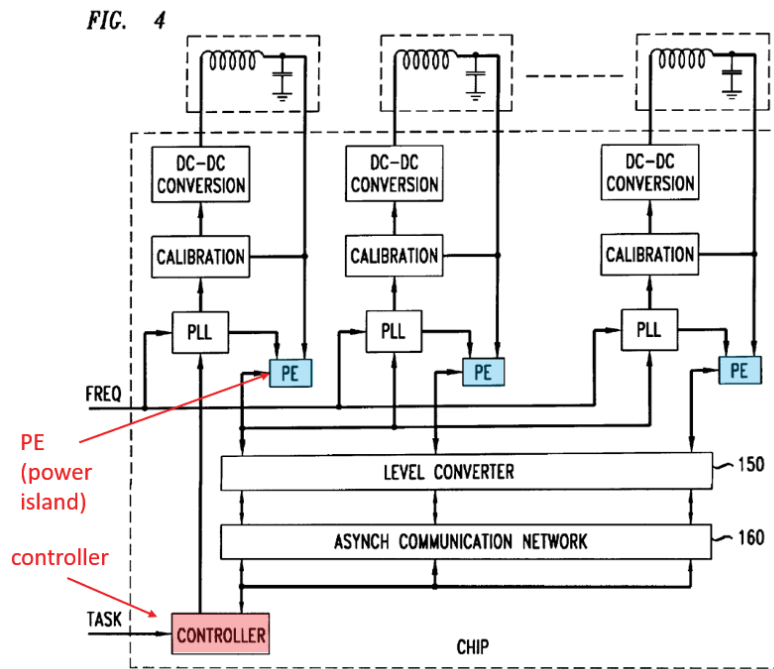
(c) Element 16[b]

267. Element 16[b] recites: “a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” Nicol discloses and/or

renders obvious Element 16[a] for at least the reasons discussed above with respect to claim Element 1[p] through 1[c], the discussions for which I incorporate herein.

268. Further, Nicol provides a “power manager”—namely, PE 100 where the “real-time operating system” resides in Figure 2 or controller/PE 200 (not shown) in Figure 4, which executes the power management scheme for the plurality of PEs. As explained for Element 1[a], PE 100 (in Figure 2) or the controller/PE 200 (in Figure 4) set the target power level. EX1008, 2:53-56 (“A real-time operating system resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications.”), 3:10-21 (similar), 6:6-13 (“As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another processing element of the integrated circuit that contains the other processing elements. . . . It also has a PE 200 that assigns the tasks given to the multi-processor chip of FIG. 4 among the PEs.”), Figs. 2, 4.





EX1008, Fig. 4.

269. Alternatively, the “power manager” in Nicol also includes the frequency and voltage circuits in both Figures 2 and 4 in addition to the “controller.”

12. Claim 17

270. Claim 17 recites: “The system of claim 16 wherein the power islands are delineated based on geographic factors of the integrated circuit.” Nicol discloses and/or renders claim 17 for at least the reasons discussed above with respect to claims 2 and 16, which I incorporate herein.

13. Claim 18

271. Claim 18 recites: “The system of claim 16 wherein the power islands are delineated based on functional circuitry of the integrated circuit.” Nicol

discloses and/or renders claim 18 for at least the reasons discussed above with respect to claims 3 and 16, which I incorporate herein.

14. Claim 19

272. Claim 19 recites: “The system of claim 16 wherein the power islands comprise power sub-islands.” Nicol discloses and/or renders claim 19 for at least the reasons discussed above with respect to claims 4 and 16, which I incorporate herein.

15. Claim 20

273. Claim 20 recites: “The system of claim 16 wherein the power islands comprise multiple clock domains.” Nicol discloses and/or renders claim 20 for at least the reasons discussed above with respect to claims 5 and 16, which I incorporate herein.

16. Claim 22

274. Claim 22 recites: “The system of claim 16 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.” Nicol discloses and/or renders claim 22 for at least the reasons discussed above with respect to claims 7 and 16, which I incorporate herein.

17. Claim 23

275. Claim 23 recites: “The system of claim 22 wherein the first voltage comprises a source voltage.” Nicol discloses and/or renders claim 23 for at least the reasons discussed above with respect to claims 8 and 16, which I incorporate herein.

18. Claim 24

276. Claim 24 recites: “The system of claim 22 wherein the first voltage comprises a threshold voltage.” Nicol discloses and/or renders claim 24 for at least the reasons discussed above with respect to claims 9 and 16, which I incorporate herein.

19. Claim 26

277. Claim 26 recites: “The system of claim 16 wherein another one of the actions comprises powering off the one of the power islands.” Nicol discloses and/or renders claim 26 for at least the reasons discussed above with respect to claims 11 and 16, which I incorporate herein.

20. Claim 31

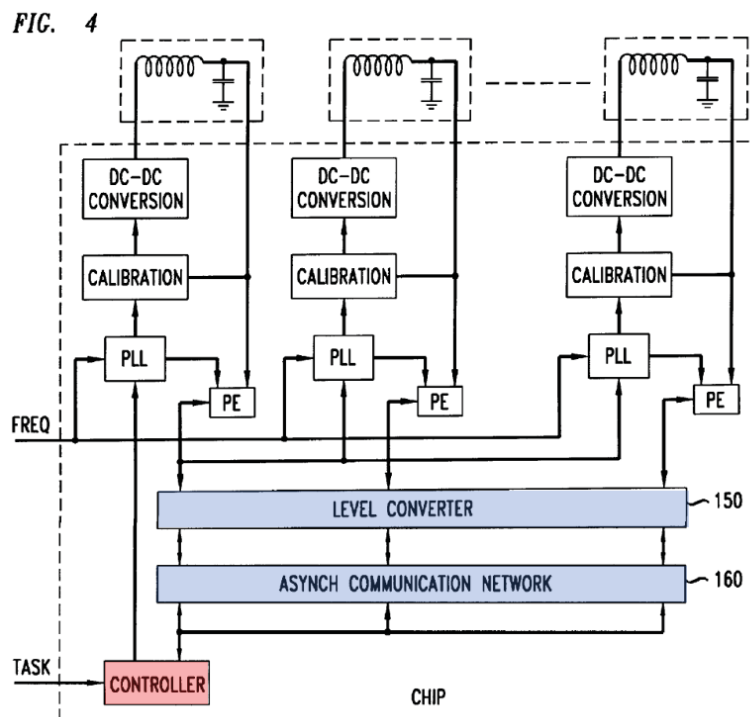
278. Claim 31 recites: “The system of claim 16 further comprising a bus coupled to the power manager and the power islands.” Nicol discloses and/or renders obvious this claim.

279. For example, Nicol references and illustrates various “lines” that connects the various components on the integrated circuit, which is at least suggestive of a bus. EX1008, 4:17-22 (“Returning the discussion to FIG. 2, the programmable-frequency clock is generated using an appropriately multiplied input reference clock (*line 101*) via a phase lock loop frequency synthesizer circuit 110[.]”), 4:31-35 (“The supply voltage command is applied to dc-dc converter 130 followed by L-C circuit 140 to cause the combination of converter 130 and L-C

circuit 140 to create the supply voltage Vdd-local, which is fed back to calibration circuit 120 via *line 102*.”), 4:42-49 (discussing line 102), 4:49-53 (“The signal on *line 121* provides information to PE 100 (yes/no) to inform the operating system of when the supply voltage is stable.”), Figures 2, 4. Although Nicol does not explicitly disclose that this line is a bus, a POSITA would have understood that it was because busses were the widely used means of communication in integrated circuits at the time of the alleged priority date of the ’306 patent. *See, e.g.*, EX1024 at 24 (“Busses are still the dominant interconnection scheme for embedded SoCs. . . . A bus provides a protocol for communication between components.”); EX1022 at Fig. 1 (showing “Fast PI bus,” “MIPS PI bus,” “Memory management interface bus,” and “TriMedia PI bus” to connect various components on SOC). As busses were the dominant form of interconnect at around the alleged priority date, it would have been obvious to a POSITA to use a bus to connect the power manager and the power islands.

280. Further, in the context of the Figure 4 embodiment, Nicol states that “a synchronization schema must be implemented when there is a need to communicate data between PEs (or with other system elements) that operate at different frequencies.” EX1008, 6:18-21. “To effect such synchronization, each PE within the FIG. 4 arrangement is in connection to an arrangement comprising elements 150 and 160. Level converter 150 converts the variable voltage swings of the PEs to a

fixed level swing, and network 160 resolves the issue of different clock domains.” EX1008, 6:29-33. A POSITA would have understood that the use of a bus to connect the power manager (controller) and the PEs would have necessitated an asynchronous communication network and a level converter to stabilize the frequency and voltage on the bus. Therefore, Nicol’s disclosure, in light of the knowledge of a POSITA at the time, renders obvious a bus coupled to the power manager and the power islands.



EX1008, Fig. 4.

21. Claim 32

281. Claim 32 recites: “The system of claim 16 wherein the power manager comprises a master manager configured to control power of the integrated circuit.”

Nicol discloses and/or renders obvious this claim.

282. As the '306 patent explains, a master manager is broadly “any circuitry configured to control the ‘global’ power behavior of the entire integrated circuit.” EX1001, 5:47-48, Fig. 2. The “controller” in Nicol (PE 100 in the embodiment shown in Figure 2, “controller” or “PE 200” in the embodiment shown in Figure 4) acts as a master manager because it communicates with the plurality of individual PEs within the power island(s) to manage the power consumption of the integrated circuit as a whole. EX1008, 2:53-56 (“A real-time operating system resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications.”), 3:10-21 (“In the FIG. 2 arrangement, in accordance with the principles disclosed herein, the applications that need to be processed are mapped to the N PEs under control of [a] real time operating system (RTOS) executed on PE 100.”), 3:66-4:10 (“Hence, the operating system of PE 100 needs to ascertain the required completion time, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time. Once the frequency is thus determined, a minimum supply voltage can be determined. The supply voltage determination can be made by reference to a plot like the one shown in FIG. 1 or, advantageously, by evaluating the actual performance of the multiprocessor at hand.”), 5:23-28 (“The FIG. 2 system uses the operating system to

react to variations in the system load. As more tasks are entered into the “to-do” list, the operating system of PE 100 computes the correct way to balance the additional computational requirements and allocates the tasks to the processors. It then computes the required operating frequency.”), 6:6-13 (“As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another processing element of the integrated circuit that contains the other processing elements. . . . It also has a PE 200 that assigns the tasks given to the multi-processor chip of FIG. 4 among the PEs.”).

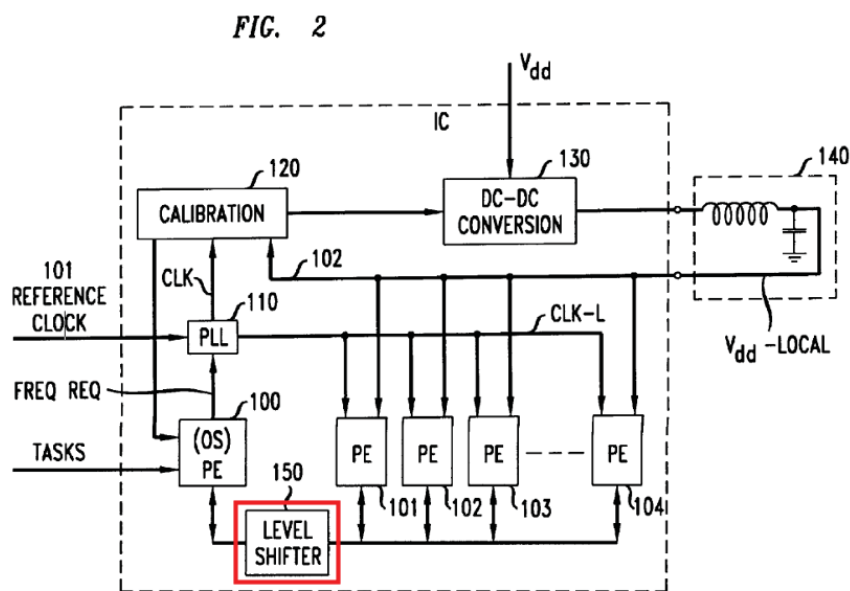
22. Claim 33

283. Claim 33 recites: “The system of claim 16 wherein the power manager comprises a slave manager configured to control power of the one of the power islands.” Nicol discloses and/or renders obvious this claim.

284. As described in the '306 patent, a slave manager is broadly “any circuitry configured to control power within a power island [] in the integrated circuit.” EX1001, 6:11-12. In the Figure 2 embodiment, the PLL and the calibration circuit, DC/DC conversion circuit, and the L-C circuit which provide frequency and voltage to PEs 101-104 act as a “slave manager” controlling power of the PEs within the power island. In the Figure 4 embodiment, the PLL and voltage circuitry associated with each PE act as the “slave managers” controlling the power of each PE and power island.

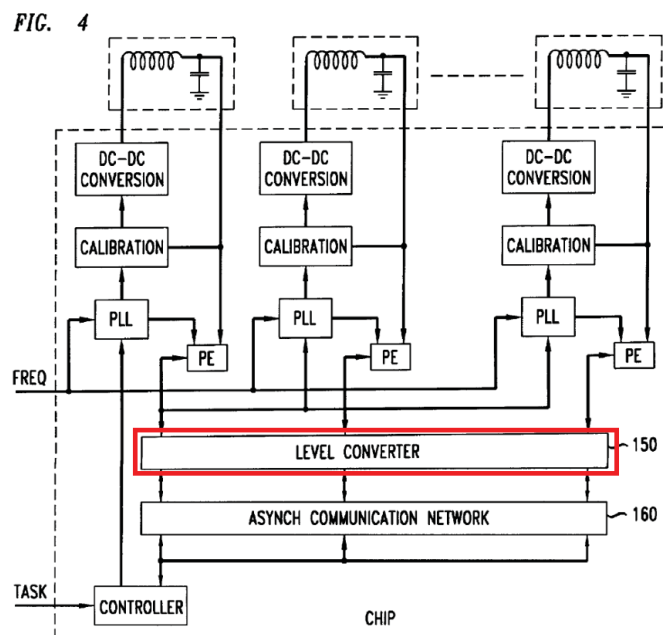
23. Claim 36

285. Claim 36 recites: “The system of claim 16 wherein the power control circuitry includes level shifting circuitry.” Nicol discloses and/or renders obvious this claim. In both the Figure 2 and Figure 4 embodiments, Nicol’s integrated circuit includes a “level shifter” or “level converter” to account for the different voltage levels being provided in the system. Figure 2 shows a “level shifter” which Nicol also refers to as “level converter,” which “converts between the voltage level of PEs 101-104 and the voltage level of PE 100.” EX1008, 5:45-51; *see also* EX1008, 7:9-14 (“It should also be noted that *level converter 150* is interposed in FIG. 2 between PE 100 and the other PEs because PE 100 is operating off V_{dd}. PE 100 can also be operated off V_{dd}-local, in which case the *level converter* is interposed between PE 100 and the input/output port of the FIG. 2 circuits that interacts with PE 100.”).



EX1008, Fig. 2.

286. Figure 4 also shows a “level converter,” which “converts the various voltage swings of the PEs to a fixed level swing[.]” EX1008, 6:29-32; *see also* EX1008, 5:49-52 (“This is accomplished with *level converter* 150, which is quite conventional[.]”). Therefore, Nicol provides level shifting circuitry in its power control circuitry.



EX1008, Fig. 4.

24. Claim 37

(a) Element 37[p]

287. Element 37[p] recites: “A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising.” Nicol discloses and/or renders obvious Element 37[p] for at least the

reasons discussed above with respect to claim Element 1[p] through 1[c], the discussions for which I incorporate herein.

288. Further, in my opinion, the notion of implementing Nicol's power management mechanism as a "software product" would have been apparent or obvious to a POSITA. For example, Nicol expressly discloses an *operating system* that executes the power management mechanism, which a POSITA would have understood to be a type of software product. See EX1008, 2:53-56 ("A *real-time operating system* resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications."), 3:10-21 (similar), 3:66-4:5 ("Hence, the *operating system* of PE 100 needs to ascertain the required completion time, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time."), 5:23-29 ("The FIG. 2 system uses the *operating system* to react to variations in the system load. As more tasks are entered into the "to-do" list, the *operating system* of PE 100 computes the correct way to balance the additional computational requirements and allocates the tasks to the processors."), 5:66-6:13 ("A separate power supply for each PE in a chip overcomes this limitation by allowing the *operating system* to independently

program the lowest operating frequency and corresponding lowest supply voltage for each PE.”).

(b) Element 37[a]

289. Element 37[a] recites: “power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.” Nicol discloses and/or renders obvious Element 37[a] for at least the reasons discussed above with respect to claim Elements 1[p] through 1[c] and 16[p], the discussions for which I incorporate herein. Further, a POSITA would have understood Nicol to disclose and/or render obvious “power management software” because its power management mechanism is executed through an operating system running on a processing element, as discussed for Element 37[p] (which, again, I incorporate here).

(c) Element 37[b]

290. Element 37[b] recites: “a software storage medium operational to store the power management software.” Nicol discloses and/or renders obvious Element 37[b]. Specifically, it would have been obvious to a POSITA that Nicol’s system would have some form of computer memory (“a software storage medium”) to store the power management software discussed above in my analysis of Elements 37[p] and 37[a]. Indeed, a real-time operating system like the one Nicol discloses (“power management software”) is typically stored—for short or long time periods—in computer memory. As one example, Nicol teaches that each PE “contains a central processing unit (CPU) and a local cache memory” and that the “real-time operating system resides in PE 100.” EX1008, 2:50-56 (“A real-time operating system resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications.”), 3:10-21 (similar), 3:66-4:5 (“Hence, the operating system of PE 100 needs to ascertain the required completion time, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time.”), 6:6-13 (“As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another processing element of the integrated circuit that contains the other processing

elements. Each processing element also requires a calibration circuit like circuit 120, and a voltage converter circuit like circuits 130 and 140. It also has a PE 200 that assigns the tasks given to the multi-processor chip of FIG. 4 among the PEs.”).

25. Claim 38

291. Claim 38 recites: “The software product of claim 37 wherein the power islands are delineated based on geographic factors of the integrated circuit.” Nicol discloses and/or renders obvious claim 38 for at least the reasons discussed above with respect to claims 2 and 37, which I incorporate herein.

26. Claim 39

292. Claim 39 recites: “The software product of claim 37 wherein the power islands are delineated based on functional circuitry of the integrated circuit.” Nicol discloses and/or renders obvious claim 39 for at least the reasons discussed above with respect to claims 3 and 37, which I incorporate herein.

27. Claim 40

293. Claim 40 recites: “The software product of claim 37 wherein the power islands comprise power sub-islands.” Nicol discloses and/or renders obvious claim 40 for at least the reasons discussed above with respect to claims 4 and 37, which I incorporate herein.

28. Claim 41

294. Claim 41 recites: “The software product of claim 37 wherein the power islands comprise multiple clock domains.” Nicol discloses and/or renders obvious

claim 41 for at least the reasons discussed above with respect to claims 5 and 37, which I incorporate herein.

29. Claim 42

295. Claim 42 recites: “The software product of claim 37 wherein another one of the actions comprises selecting a clock for the one of the power islands.” Nicol discloses and/or renders obvious claim 42 for at least the reasons discussed above with respect to claims 6 and 37, which I incorporate herein.

30. Claim 43

296. Claim 43 recites: “The software product of claim 37 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.” Nicol discloses and/or renders obvious claim 43 for at least the reasons discussed above with respect to claims 7 and 37, which I incorporate herein.

31. Claim 44

297. Claim 44 recites: “The software product of claim 43 wherein the first voltage comprises a source voltage.” Nicol discloses and/or renders obvious claim 44 for at least the reasons discussed above with respect to claims 8 and 37, which I incorporate herein.

32. Claim 45

298. Claim 45 recites: “The software product of claim 43 wherein the first voltage comprises a threshold voltage.” Nicol discloses and/or renders obvious

claim 45 for at least the reasons discussed above with respect to claims 9 and 37, which I incorporate herein.

33. Claim 47

299. Claim 47 recites: “The software product of claim 37 wherein another one of the actions comprises powering off the one of the power islands.” Nicol discloses and/or renders obvious claim 47 for at least the reasons discussed above with respect to claims 11 and 37, which I incorporate herein.

F. Analysis of Nicol in view of Nowka with Respect to Claims 6, 10, 12, 14-15, 21, 25, 27, 29-30, 34, 46, 48, 50-51

300. For the reasons articulated in detail below, and based on my review of the '306 patent and the Nicol and Nowka references, I am confident that a POSITA would have readily understood that Nicol in view of Nowka renders obvious claims 6, 10, 12, 14-15, 21, 25, 27, 29-30, 34, 46, 48, 50-51.

1. Overview of Nowka

301. I incorporate herein the overview of Nowka section above in Section VIII.A.1.

2. Combination of Nicol and Nowka

302. In my opinion, a POSITA would have been motivated to combine the teachings of Nicol and Nowka with a reasonable expectation of success.

303. Nicol and Nowka are in the same field of endeavor: power management on an integrated circuit. EX1008, Abstract; EX1004, Abstract. Both references

explain that many systems or components spend much of their time “idle” or “waiting” and only require peak performance for short portions of time. EX1008, 3:4-6 (“It may be noted that, typically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption.”); EX1004, 1441 (“These applications tend to have peak performance demands as high as 500 MIPS but also tend to remain idle for much of the time.”). Moreover, they both teach that *dynamically* responding to system conditions is beneficial for minimizing power consumption while assuring adequate performance. EX1008, 2:18-22 (“Improved performance of multi-processor chips is achieved by *dynamically controlling the processing load of chips* . . . as to minimize overall power consumption.”); EX1004, 1441 (“A PowerPC system-on-a-chip processor...adapt[s] to the *dynamically changing performance demands* and power consumption constraints of high-content, battery powered applications[.]”).

304. Nicol and Nowka both teach dynamically changing frequency and voltage to change the power consumption level of power islands on the integrated circuit. EX1008, 2:11-14 (“Thus, it is known that *varying supply voltage* to a chip can improve performance by eliminating unexpected variability in the supply voltage, and by accounting for process and operating temperature variations.”), 3:24-27 (“This allows the *clock frequency of the PEs to be reduced*[.]”); EX1004, 1442

(“DVS systems *adjust the supply voltage dynamically* to meet the performance demands while minimizing power consumption.”), 1444 (“*Adjustment to the output clock frequency* can be done on-the-fly by modifying the output clock divider through a write to a control register.”).

305. Given the identical field of endeavor and the similarity of the disclosures—e.g., Nowka describes a physical implementation of a power management scheme with frequency and voltage scaling, like in Nicol—a POSITA would have naturally been inclined to incorporate Nowka’s teachings in the context of Nicol’s disclosure. For example, a POSITA would have been motivated to integrate Nowka’s standby modes in Nicol because standby modes were known to provide the benefit and advantage of eliminating unnecessary active power, thereby minimizing overall power consumption. Such modes were commonly used in various products at the time, and in the Advanced Configuration and Power Interface (ACPI) Specification, with which a POSITA would have been familiar. *See* EX1017 at 189-196. Nicol states that “typically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption.” EX1008, 3:4-7. Where Nicol expressly suggests the solution of “scaling back” the performance via frequency and voltage reduction, a POSITA would have appreciated that such a motivation applies to standby modes as well. EX1004, 1446 (“In this design, only a small sleep and clock manager is kept

active during sleep. Several modes of standby operation are employed to achieve a range of standby power levels.”).

306. Further, a POSITA would have been motivated to incorporate Nowka’s PLL circuitry into Nicol’s PLL to allow Nicol’s system to quickly switch between clock sources, especially at extremely low frequencies. Using Nowka’s PLL, “[a]djustment to the output clock frequency can be done on-the-fly by modifying the output clock divider through a write to a control register. This allows adjustment of the frequency across a range of 1/2 to 1/248th of the VCO frequency. A glitchless output multiplexor avoids spurious clock pulses during this operation and allows for clock freezing for sleep and hibernation modes. . . . Under software control, at a given supply voltage, the frequency of the core can be varied from the maximum frequency down to 1/64th of the maximum. This allows the frequency to be dynamically set as low as 4.2 MHz.” EX1004, 1444. Because Nicol provides a variable clock frequency to its power islands, a POSITA would have been motivated to incorporate a clock multiplexor to improve the dynamic frequency-varying, allow for glitchless frequency switching, and to allow for clock freezing in sleep and hibernation modes. *See* EX1008, 4:17-22 (“[T]he programmable-frequency clock is generated using an appropriately multiplied input reference clock (line 101) via a phase lock loop frequency synthesizer circuit 110 which has a high resolution, e.g., can be altered in increments of 5 MHz.”).

3. Claim 6

307. Claim 6 recites: “The method of claim 1 wherein another one of the actions comprises selecting a clock for the one of the power islands.” The Nicol-Nowka combination renders this claim obvious. For example, Nowka specifically discloses that the “output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock as the processor clock source to allow for extremely low frequency operation.” EX1004, 1444.

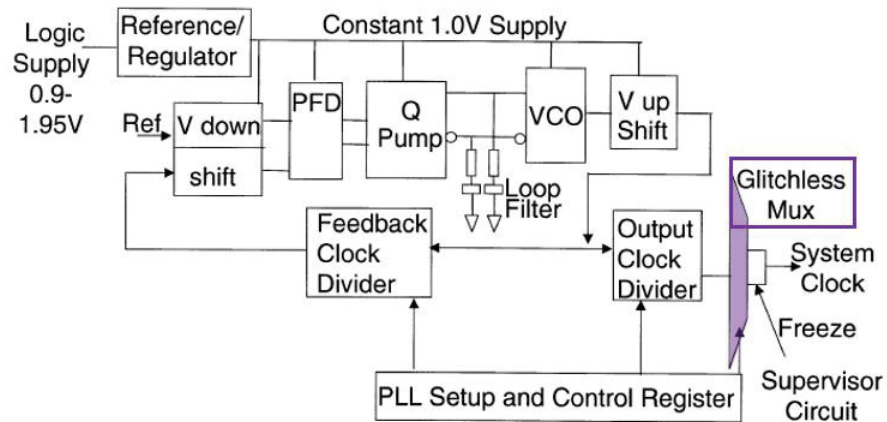


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

308. A POSITA would have been motivated to implement such a clock-selecting technique in Nicol’s PLL to enhance the ability to quickly switch between clock frequencies for a given PE or power island. As Nowka explains, “[a]djustment to the output clock frequency can be done on-the-fly by modifying the output clock divider through a write to a control register. . . . The output multiplexor can also select the real-time clock, reference clock, or auxiliary clock as the processor clock

source to allow for extremely low frequency operation.” EX1004, 1444. A POSITA would have understood that incorporating a clock divider and multiplexor into Nicol’s PLL would allow for seamless transition between frequencies, as well as allowing for alternative clock sources for extremely low-frequency operation. *See* EX1008, 5:41-44 (“Of course, Vdd-local can only be reduced so-far before the circuits start to fail, at which point the operating system employs gated clocking techniques to “shut down” PEs that are not needed.”). Implementing Nowka’s PLL structure (including the clock selection) would have required no more than routine engineering skills, namely implementing Nowka’s PLL circuitry as part of Nicol’s PLL. Because Nicol’s PE outputs two frequencies (Clk and Clk-L) and therefore requires two synthesizer circuits, EX1008, 4:17-22, the “synthesizer circuit” portion of Nowka’s PLL (the PFD, Q pump, VCO, loop filter, clock divider and clock multiplexor) would be replicated for each of the two synthesizer circuits.

4. Claim 10

309. Claim 10 recites: “The method of claim 1 wherein another one of the actions comprises powering on the one of the power islands.” The Nicol-Nowka combination renders this claim obvious.

310. For example, Nowka discloses low-power standby modes called “hibernation” and “cryo” where “the logic supply to the processor, caches and the SOC core is disconnected.” EX1004, 1446; *see also* 1442, 1445 (“the clocks to

individual functional cores can also be frozen”). This is advantageous for power savings because disconnecting the logic supply “eliminates the leakage component of the standby power” in a power domain. EX1004, 1446. When the logic supply is shut down, the logic domain is turned off and not operating. EX1004, 1446 (“In this design, only a small sleep and clock manager is kept active during sleep.”). When hibernation or cryo mode is exited to “reactivat[e] the system” upon a “wakeup event,” the SOC “restores the [logic] supply,” which means that it powers on the logic domain for operation. EX1004, 1446.

311. It would have been obvious to a POSITA to incorporate Nowka’s “hibernation” and “cryo” modes, which involve shutting off and then turning on the logic power domain, into Nicol. Such a function is beneficial for power savings because disconnecting the supply “eliminates the leakage component of the standby power” in a power domain. EX1004, 1446. Nicol also acknowledges the need to minimize leakage current in power management schemes in its background discussion. EX1008, 2:8-10 (“These techniques are needed to ensure that the leakage current, which increasing as the threshold voltage is reduced, does not become too large.”). Nicol further explains that “typically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption.” EX1008, 3:4-7. Therefore, a POSITA would have been motivated to incorporate turning off and on a power island

to conserve power. *See* EX1017 at 30 (“The nap and doze modes of operation in portable computers [] are examples of this approach to the reduction of useless switching activity. Power is reduced by stopping the clock or shutting down the power supply of parts of the system that are not required to carry out the current task.”). Incorporating a “hibernation mode” was a known technique and would have been a straightforward improvement to a similar device (Nicol’s integrated circuit) for the same objective (reducing leakage current). For example, Nicol discloses controlling operating voltages with “significantly greater than on/off granularity,” demonstrating that turning a component on and off was well-known in the art. EX1008, Abstract, 2:18-31.

5. Claim 12

312. Claim 12 recites: “The method of claim 1 wherein another one of the comprises changing the one of the power islands to a sleep mode.” The Nicol-Nowka combination renders this claim obvious. The ’306 patent lists “low power modes such as sleep, nap, and full power down.” EX1001, 7:26-27. Similarly, Nowka describes low power modes such as freeze, hibernation, and cryo modes as part of “standby power management.” These different standby modes “achieve a range of standby power levels.” EX1004, 1446. In freeze mode, “the system clock is stopped and the logic supply is decreased to its minimum value of 1.0 V. The entire state of the SOC is maintained in place. In this mode, leakage power and the

power of the sleep and clock manager are consumed.” EX1004, 1446. In hibernation mode “the logic supply to the processor, caches and the SOC cores is disconnected. . . . This mode eliminates the leakage component of the standby power.” EX1004, 1446. In cryo mode, “the state of latches and register arrays in the processor core and SOC cores is transferred to nonvolatile storage prior to disconnecting the logic supply.” EX1004, 1446. A POSITA would have understood each one of these modes to satisfy the “sleep mode” of claim 12.

313. A POSITA would have been motivated to implement Nowka’s standby modes in Nicol because such states (1) minimize leakage current during inactivity (hibernation and cryo modes) and (2) enhance the overall energy efficiency of the system. *See, e.g.*, EX1017 at 30 (“The nap and doze modes of operation in portable computers [] are examples of this approach to the reduction of useless switching activity. Power is reduced by stopping the clock or shutting down the power supply of parts of the system that are not required to carry out the current task.”). Nicol explicitly teaches that “techniques are needed to ensure that the leakage current . . . does not become too large.” EX1008, 2:8-10. Nicol further explains that “typically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption.” EX1008, 3:4-7. Nowka also explains: “[s]tatic power due to reverse-biased junction current, sub-threshold leakage, gate leakage and analog current sources can limit the

operating lifetime of battery-powered systems. Decreasing the standby power of the IC increases shelf-life as well as overall energy efficiency.” EX1004, 1446. Therefore, a POSITA would have been motivated to enable Nicol’s PEs or group of PEs (power islands) to enter into modes such as freeze, hibernation, and/or cryo modes to minimize power consumption when the particular PE or group of PEs does not need to be active.

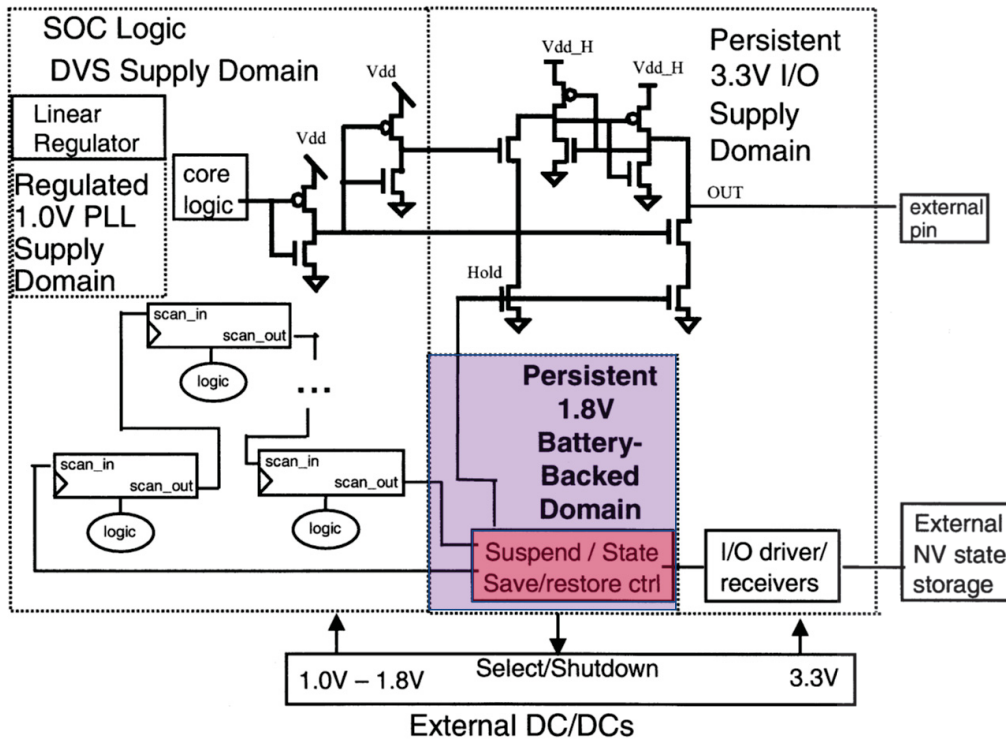
314. This modification is simply the application of a known technique (standby modes) to improve a similar device (Nicol’s integrated circuit) in the same way (to minimize leakage current and allow efficient return to full-power mode). Indeed, standby modes such as those described by the ’306 patent and Nowka were well-known and widely implemented in the art around the alleged priority date. *See, e.g.,* EX1018 at 2 (“The StrongARM SA-1100 processor . . . has three modes of operation: Run, IDLE, and SLEEP.”), 3 (“IBM’s Travelstar [4] hard disk drives have three low-power inactive states called Performance Idle, Active Idle, and Low Power Idle.”), 3 (“All major components [of the PaperClip by HP Laboratories] are power-manageable: the CPU, memory, LCD, and digitizer can be put in a low-power sleep state.”); EX1017 at 189-96 (describing various sleep states defined by Advanced Configuration and Power Interface (ACPI) Specification), 207 (“Similarly to the ACPI specification, for each service provider there is only one state, called *ON*, in

which full functionality is provided. There can be an arbitrary number N_S of sleep states[.]”).

6. Claim 14

315. Claim 14 recites: “The method of claim 1 further comprising saving a state of components within the one of the power islands.” The Nicol-Nowka combination renders this claim obvious. For example, in Nowka’s cryo mode, “the state of latches and register arrays in the processor core and SOC *cores is transferred to nonvolatile storage* prior to disconnecting the logic supply.” EX1004, 1446. The suspend controller stops the clocks, freezes the I/O drivers, *scans the register state out* through the IIC interface to nonvolatile storage, removes logic power[.]” EX1004, 1446. This way, “the entire register state of the SOC can be restored prior to reactivating the system.” EX1004, 1446. Nowka thus discloses saving the state of the latches and register arrays, which are components in the logic domain, prior to entering cryo mode.

316. Figure 3 of Nowka (below) shows a block labeled “Suspend/State Save/restore ctrl” (in red) that is used to suspend, state save, and restore of the state of registers within the power island of the variable voltage power domain. EX1004, 1446, Fig. 3. A POSITA would have understood that this control block facilitates the saving of the state of logic domain components prior to entering cryo mode.



EX1004, Fig. 3.

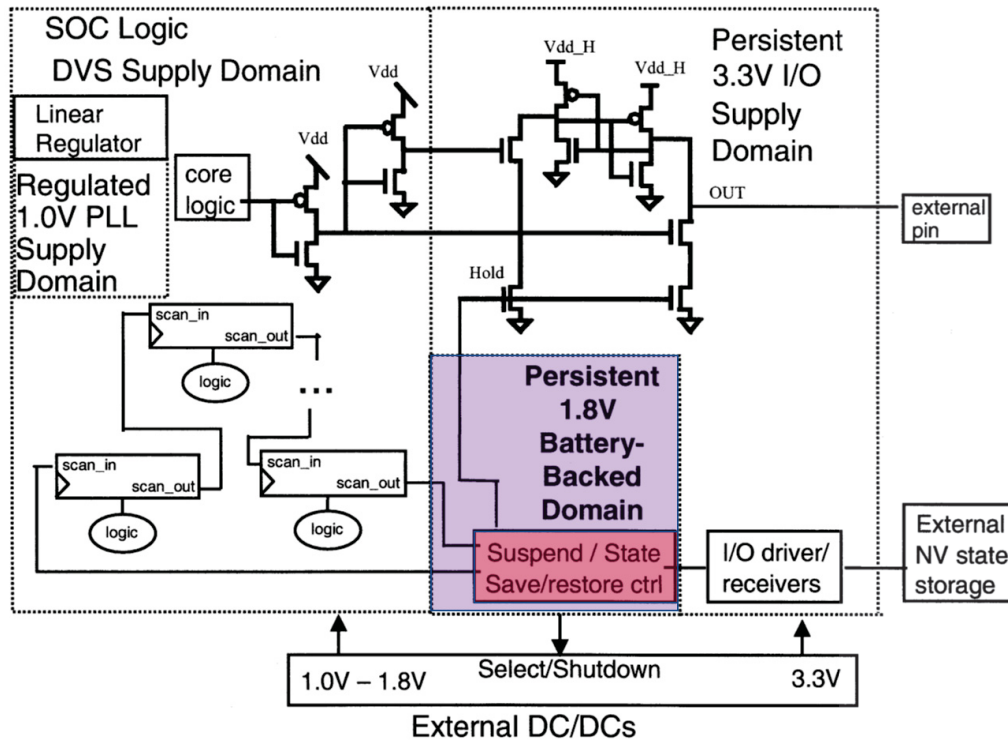
317. A POSITA would have been motivated to incorporate Nowka’s state-saving mechanism in Nicol because such a solution allows for efficient restoration of the system state (in this case, of the PE or group of PEs which is the power island) after being placed in a standby mode. See EX1017 at 194 (“A device in D1 is expected to dissipate more power than a device in D2, but *it preserves more context (hence, wake-up is faster)*. . . . Since device context and power supply are lost, devices in [D3] state cannot receive any command. Devices in state D3 have the *longest restore times.*”). Such a modification would have been a straightforward implementation of a known technique (Nowka’s state-save circuitry and function) to predictably improve the power efficiency of dynamic power management in

Nicol. Indeed, the solution of saving a state of components to restore them at return to full power was well known and commonly implemented by the time of the Critical Date. *See, e.g.*, EX1017 at 187-88 (“When the OS is preparing to transition to a sleep state, a message is broadcast to all applications which can react accordingly. Several actions can be taken: for example the application may decide to ***save some context information***, or may inform the OS that the system should not transition to the sleep state.”); EX1019 at 4 (“However, some subset of the logic state, prior to power-down, ***may need to be preserved*** to resume operation once the island is again powered up, at the end of the inactive period.”).

7. Claim 15

318. Claim 15 recites: “The method of claim 1 further comprising restoring a state of components within the one of the power islands.” The Nicol-Nowka combination renders this claim obvious. For example, Nowka discloses that after the system has entered cryo mode, the suspend controller “waits for a wakeup event at which time it restores the supply, ***restores the state*** and restarts the clocks.” EX1004, 1446. “Restoring the state” refers to restoring the state of the latches and register arrays in the processor core and SOC core, which are components within the logic domain, that had been saved prior to entering cryo mode. Further, Nowka discloses that with cryo mode “the entire register state of the SOC can be restored prior to reactivating the system.” EX1004, 1446. A POSITA would have

understood that the control block labeled “Suspend/State Save/restore ctrl” facilitates the restoring of the state of logic domain components when exiting cryo mode and reactivating the system.



EX1004, Fig. 3.

319. In incorporating Nowka into Nicol, a POSITA would have found it obvious to allow the system to restore a state of systems. Such a modification would have been a straightforward implementation of a known technique (Nowka’s state-restore circuitry and function) for the predictable result of enabling standby modes in Nicol. Indeed, the technique of saving a state of components to restore them at return to full power was well known and commonly employed by the time of the Critical Date. *See, e.g.,* EX1017 at 207 (“[T]ransitioning to a new state costs

additional power (to *save/restore context* and perform various shutdown/wakeup activities.”), 185 (“A device in D1 is expected to dissipate more power than a device in D2, but *it preserves more context (hence, wake-up is faster)*. . . . Since device context and power supply are lost, devices in [D3] state cannot receive any command. Devices in state D3 have the *longest restore times*.”).

8. Claim 21

320. Claim 21 recites: “The system of claim 16 wherein another one of the actions comprises selecting a clock for the one of the power islands.” The Nicol-Nowka combination renders obvious claim 21 for at least the reasons discussed above with respect to claims 6 and 16, which I incorporate herein.

9. Claim 25

321. Claim 25 recites: “The system of claim 16 wherein another one of the actions comprises powering on the one of the power islands.” The Nicol-Nowka combination renders obvious claim 25 for at least the reasons discussed above with respect to claims 10 and 16, which I incorporate herein.

10. Claim 27

322. Claim 27 recites: “The system of claim 16 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.” The Nicol-Nowka combination renders obvious claim 27 for at least the reasons discussed above with respect to claims 14 and 16, which I incorporate herein.

11. Claim 29

323. Claim 29 recites: “The system of claim 16 wherein the power manager is configured to save a state of components within the one of the power islands.” The Nicol-Nowka combination renders obvious claim 29 for at least the reasons discussed above with respect to claims 14 and 16, which I incorporate herein.

12. Claim 30

324. Claim 30 recites: “The system of claim 16 wherein the power manager is configured to restore a state of components within the one of the power islands.” The Nicol-Nowka combination renders obvious claim 30 for at least the reasons discussed above with respect to claims 15 and 16, which I incorporate herein.

13. Claim 34

325. Claim 34 recites: “The system of claim 16 wherein the power control circuitry includes clock multiplexing circuitry.” The Nicol-Nowka combination renders this claim obvious. Nowka discloses “a glitchless output multiplexor” as part of the phase locked loop (PLL) that provides the operating frequency for the power domains. EX1004, 1444. “The output multiplexor can also select the real-time clock, reference clock, or an auxiliary clock.” EX1004, 1444. Figure 7 shows the “Glitchless Mux” integrated into the PLL which “allows adjustment of the frequency across a range of 1/2 to 1/128th of the VCO frequency.” EX1004, 1444. As I explained above at Element 16[a], the PLL is part of the power control circuitry that controls power for the power islands in Nicol. *See* §VIII.E.11(b)).

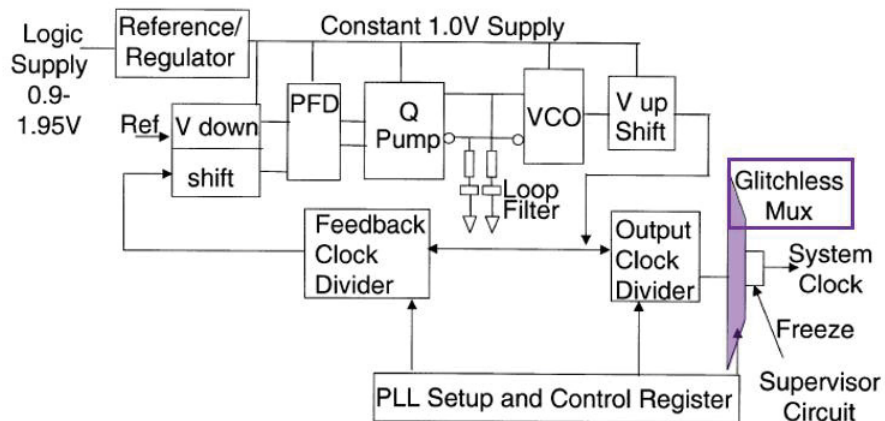


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

326. A POSITA would have been motivated to combine Nowka’s teachings regarding PLL circuitry, including the above-discussed multiplexor, with Nicol’s disclosure. Nicol similarly has a phase lock loop frequency synthesizer circuit (PLL) which provides a variable frequency to the power islands. *See* EX1008, 4:17-27, Figs. 2, 4. A POSITA would have been motivated to integrate Nowka’s multiplexor in Nicol’s PLL to enable glitchless selection of frequency. Further, the multiplexor “allows for clock freezing for sleep and hibernation modes,” EX1004, 1444, which a POSITA would have also been motivated to implement in Nicol, as discussed for claim 12 above. Such clock multiplexors were commonly known in the art, and incorporating them into Nicol’s PLL would have required no more than routine engineering skills. Because Nicol’s PE outputs two frequencies (Clk and Clk-L) and therefore requires two synthesizer circuits, EX1008, 4:17-22, the “synthesizer

circuit” portion of Nowka’s PLL (the PFD, Q pump, VCO, loop filter, clock divider and clock multiplexor) would be replicated for each of the two synthesizer circuits.

14. Claim 46

327. Claim 46 recites: “The software product of claim 37 wherein another one of the actions comprises powering on the one of the power islands.” The Nicol-Nowka combination renders obvious claim 46 for at least the reasons discussed above with respect to claims 10 and 37, which I incorporate herein.

15. Claim 48

328. Claim 48 recites: “The software product of claim 37 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.” The Nicol-Nowka combination renders obvious claim 48 for at least the reasons discussed above with respect to claims 12 and 37, which I incorporate herein.

16. Claim 50

329. Claim 50 recites: “The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within the one of the power islands.” The Nicol-Nowka combination renders obvious claim 50 for at least the reasons discussed above with respect to claims 14 and 37, which I incorporate herein.

17. Claim 51

330. Claim 51 recites: “The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the

processor to restore a state of components within the one of the power islands.” The Nicol-Nowka combination renders obvious claim 51 for at least the reasons discussed above with respect to claims 15 and 37, which I incorporate herein.

G. Analysis of Nicol in view of Borkar with Respect to Claims 13, 28, and 49

331. For the reasons articulated in detail below, and based on my review of the '306 patent and the Nicol and Borkar references, I am confident that a POSITA would have readily understood that Nicol in view of Borkar renders obvious all elements of claims 13, 28, and 49.

1. Overview of Borkar

332. I incorporate herein the overview of Borkar section above in Section VIII.C.1.

2. Combination of Nicol and Borkar

333. In my opinion, a POSITA would have been motivated to combine the teachings of Nicol and Borkar with a reasonable expectation of success for a number of reasons.

334. First, Nicol and Borkar are in the same field of endeavor: power management of integrated circuits on a chip. Nicol relates to “electronic circuits and, more particularly to power consumption within electronic circuits.” EX1008, Abstract, 1:6-7. Similarly, Borkar describes “control circuitry [that] controls a setting of a body bias signal . . . to at least partially control a parameter of the

processor. . . . Examples of the parameters include performance, power consumption, and temperature.” EX1006, 1:60-2:3.

335. Second, both Nicol and Borkar describe balancing performance and power consumption in an integrated circuit. It was well-known to a POSITA that lowering power consumption can lead to tradeoffs in performance. For example, Nicol states that “[f]or a maximally utilized system, all of the available processors ought to be operating at full speed when satisfying the maximum load encountered by the system. At such a time, the power consumption of the multiprocessor chip is at its maximum level. However, as the load requirements are lowered, the system should, advantageously, reduce its power consumption.” EX1008, 2:65-3:4. Similarly, Borkar states that “The performance, power consumption, and temperature [of an integrated circuit] are typically related.” EX1006, 1:20-21. Borkar further states that “[t]he user may specify certain power conditions or a power versus performance tradeoff.” EX1006, 5:45-46.

336. Third, both Nicol and Borkar disclose independently controlling distinct parts of the integrated circuit, including by varying the frequency and supply voltage. Nicol teaches that “[a] separate power supply for each PE in a chip [allows] the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” EX1008, 5:66-6:2. Similarly, Borkar discloses that “[t]he invention may also include changing clock frequency

signals and supply voltage signals to at least partially control a parameter.” EX1006, 2:52-54.

337. A POSITA considering Nicol would have understood that maintaining the highest performance while not exceeding a threshold power consumption level was important for safe and long-lasting circuit design. Accordingly, the POSITA would naturally have looked to Borkar to address this issue in Nicol for the reasons enumerated above, and because of Nicol’s explicit teaching in this regard. Nicol explains that “the operating system can reduce the supply voltage even further by tracking temperature and process variations.” EX1008, 4:11-13. A POSITA would have understood that temperature, as a proxy for power consumption, needs to be kept within a certain threshold to not cause damage to the electronic circuit. Borkar also directly addresses these concerns. *See* EX1006, 1:46-48 (“[T]he processor may be required to sustain a high rate of transistor switching per unit time leading to substantial power consumption and resulting temperature increase.”), 12:11-15 (“Examples of the goals include keeping power consumption below a particular level, keeping temperatures in a particular range, obtaining the highest possible performance, and obtaining the highest performance while not exceeding a particular power consumption level.”). Thus, the POSITA would have been motivated to use Borkar’s monitoring of power consumption levels in Nicol’s power management method to ensure that temperature or power dissipation did not become excessive,

compromising the integrity and performance of Nicol's system. *See* EX1017, 51-52 (“High power dissipation is associated with heat that must be adequately dissipated, otherwise temperature may raise and abruptly reduce reliability or even directly cause functional failure.”).

3. Claim 13

338. Claim 13 recites: “The method of claim 1 further comprising: monitoring the power consumption level of the one of the power islands; determining whether a threshold level was crossed based on the power consumption level; and performing another one of the based on the crossing of the threshold level.” The Nicol-Borkar combination renders this claim obvious.

339. For example, Borkar discloses that “[i]n many situations, then, control circuitry 262 may seek to obtain the highest performance that both domains can achieve at the same clock frequency and with [*sic*] exceeding a power consumption level. The acceptable power consumption levels could be different for the different domains. Different techniques may be used to not exceed power consumption levels. A simple but imprecise way is to not allow the supply voltage, threshold voltages, or frequency, to pass certain levels.” EX1006, 13:1-6. As would have been apparent or obvious to a POSITA, Borkar's “acceptable power consumption levels” correspond to the “threshold level” of the '306 patent.

340. Borkar explains that a more precise way to keep power consumption at a certain level is “to detect current being consumed” and determining the power consumption using the current and supply voltage. EX1006, 13:6-7. Borkar discloses numerous embodiments (e.g., depicted in Figures 1-2, 4, 7) that explicitly show “current detection circuitry” which provide current signals to “voltage and frequency control circuitry.” EX1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7 (Figs. 1, 7 shown below). Because current multiplied by supply voltage is power consumption, Borkar’s system can monitor power consumption by monitoring current signal. EX1006, 4:64-67, 13:7-8. As a POSITA would have understood, by calculating the power consumption in this way, the system can monitor the power consumption and perform appropriate actions, such as changing body bias, supply voltage, and clock frequencies, in the event the power consumption approaches or crosses the threshold level. EX1006, 6:1-7, 13:2-7.

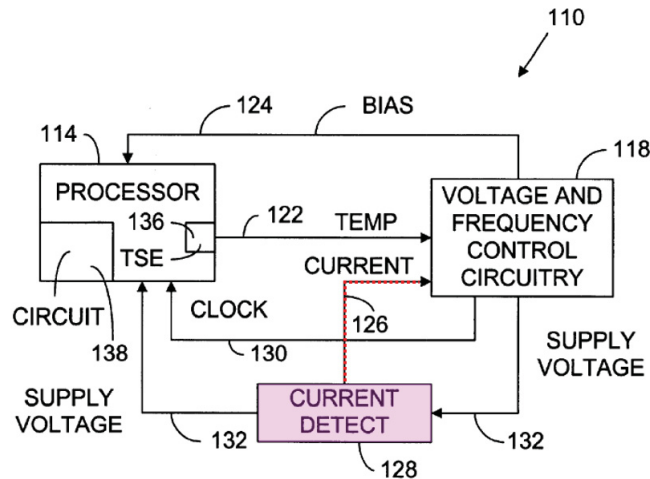


FIG. 1
EX1006, Fig. 1.

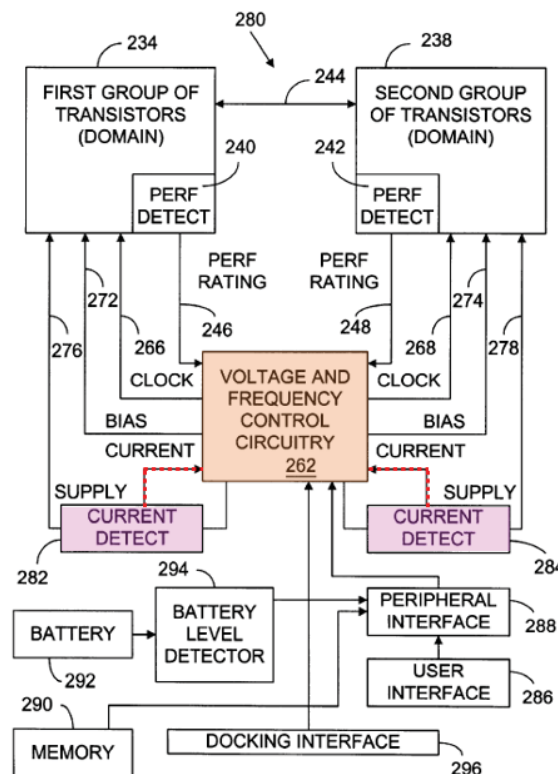


FIG. 7

EX1006, Fig. 7.

341. As I explained above, a POSITA would have been motivated to combine Borkar’s power consumption monitoring with Nicol’s system to achieve more precise and predictable power consumption control. Where Nicol changes operating parameters based primarily on the most efficient division of the application at hand, incorporating power monitoring from Borkar would allow Nicol’s system to further respond to excessive power consumption levels, similar to Nicol’s disclosure that “the operating system can reduce the supply voltage even further by tracking temperature and process variations.” EX1008, 4:11-13. A POSITA would have understood that Borkar’s current-measuring method provided

an accurate power consumption measurement, which enables better decisions in operating components on the chip.

342. In addition, Borkar discloses and/or renders obvious the features of claim 13 by describing “control circuitry” that “monitors a temperature signal...related to the temperature of [a] processor,” which a POSITA would have understood (and the ’306 patent concedes) reflects the power consumption level. EX1006, 4:12-20; *see also* EX1001, 6:47-50 (explaining that “temperature” is an example of a “power consumption level[]”). According to Borkar, “if the temperature TACTUAL of [the] processor...exceeds an upper temperature limit THIGH,” the system, in response to this determination, performs an appropriate action—e.g., “change[s] the body bias, supply voltage, and/or clock signal settings”—“to decrease temperature.” EX1006, 4:21-46. Consistent with , a POSITA would have been motivated to integrate Borkar’s temperature monitoring techniques with Nicole to provide the predictable benefit of preventing overheating. EX1006, 1:11-56.

343. A POSITA would have needed only routine electrical and computer engineering principles to implement Borkar’s temperature/power monitoring and threshold-comparing mechanisms in Nicol’s system, as demonstrated by Borkar’s description of the mechanism in a system analogous to Nicol’s. EX1006, 2:49-52 (“The invention involves changing body bias signals applied to transistors in an

integrated circuit in response to changing conditions to at least partially control a parameter of the integrated circuit.”). Such a combination would predictably result in improved performance and longevity by limiting power consumption levels to the appropriate levels.

4. Claim 28

344. Claim 28 recites: “The system of claim 16 wherein the power manager is configured to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.” The Nicol-Borkar combination renders obvious claim 28 for at least the reasons discussed above with respect to claims 13 and 16, which I incorporate herein.

5. Claim 49

345. Claim 49 recites: “The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.” The Nicol-Borkar combination renders obvious claim 49 for at

least the reasons discussed above with respect to claims 13 and 37, which I incorporate herein.

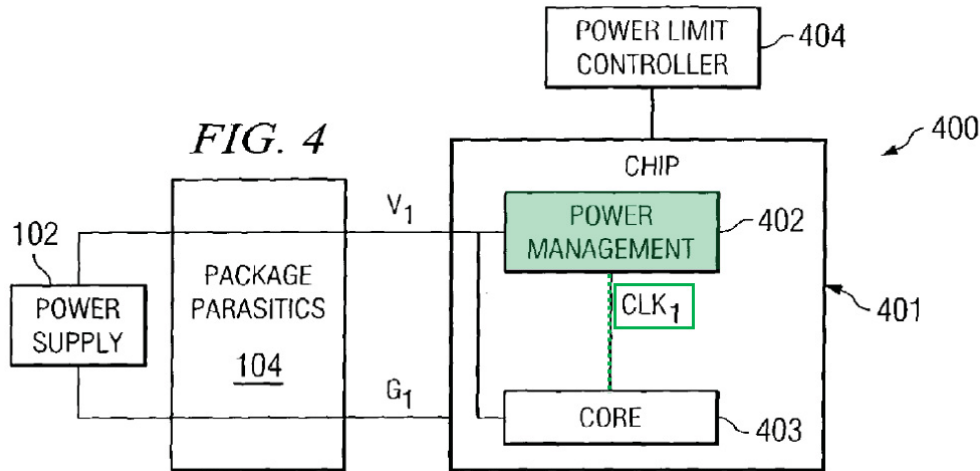
H. Analysis of Nicol in view of Naffziger with Respect to Claim 35

346. For the reasons articulated in detail below, and based on my review of the '306 patent and the Nicol and Naffziger references, I am confident that a POSITA would have readily understood that Nicol in view of Naffziger renders obvious all elements of claim 35.

1. Overview of Naffziger

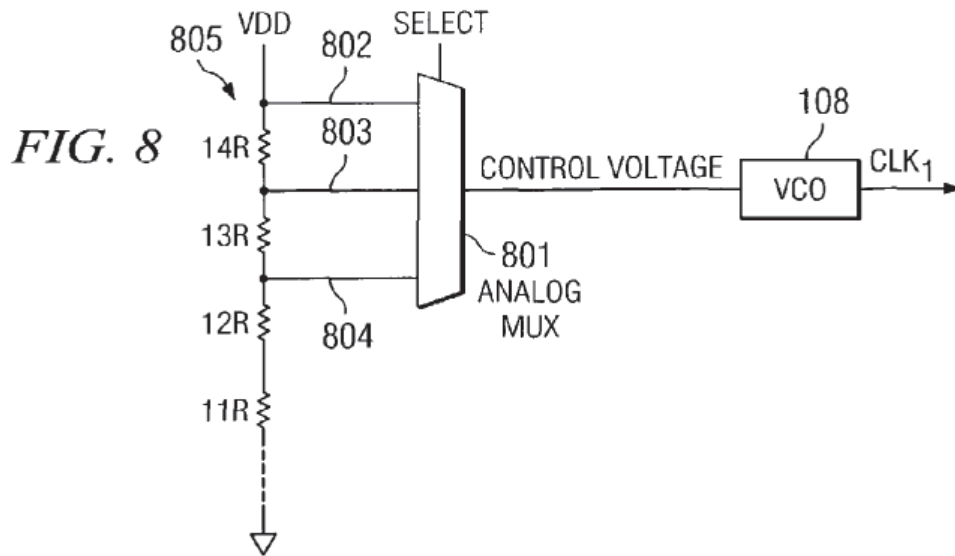
347. Naffziger is titled “System and method for implementing an integrated circuit having dynamically variable power limit.” EX1015, Title. Naffziger’s system is “capable of having its power limit dynamically varied to any of a plurality of different values. Preferably, the chip is implemented in a manner that enables any of a plurality of different measured power limits to be dynamically set for the chip.” EX1015, 5:32-36. “For example, the chip may be implemented in a notebook computer, and the chip may operate at its higher operating point as long as the notebook computer is connected to an alternating current (AC) power source and it may vary its operation to the lower operating point when the notebook computer is removed from the AC power source (e.g., to preserve the notebook computer’s battery).” EX1015, 5:50-56. Naffziger includes a “power management” logic for self-regulating power consumption. EX1015, 11:50-51. The power management

logic comprises a voltage controlled frequency oscillator that generates a clock signal for the core chip circuitry. EX1015, 11:52-58. “As described above, the frequency of such clock signal may be dynamically varied by power management logic 402 to regulate the chip’s power consumption[.]” EX1015, 11:58-61.



EX1015, Fig. 4.

348. Naffziger’s power management logic includes a voltage multiplexor in conjunction with a resistor divider to reduce the voltage to the VCO by a fixed ratio. EX1015, 19:37-41. Figure 8 shows the frequency adjustment circuitry within the power management logic which has a resistor divider, with 14 resistors in series, combined with a voltage multiplexor. EX1015, 19:45-50, Fig. 8. This setup allows for the multiplexor to choose one of multiple voltage levels to output as the control voltage, in turn allowing for a variable clock frequency output from the VCO. EX1015, 19:50-58.



EX1007, Fig. 8.

2. Combination of Nicol and Naffziger

349. In my opinion, a POSITA would have been motivated to combine the teachings of Nicol and Naffziger with a reasonable expectation of success for a number of reasons.

350. First, Nicol and Naffziger are in the same field of endeavor: power management on an integrated circuit. Nicol relates to “power consumption within electronic circuits,” including integrated circuits. EX1008, Abstract, 1:6-9. Similarly, Naffziger relates to “management of power consumption by an integrated circuit.” EX1015, 1:19-21.

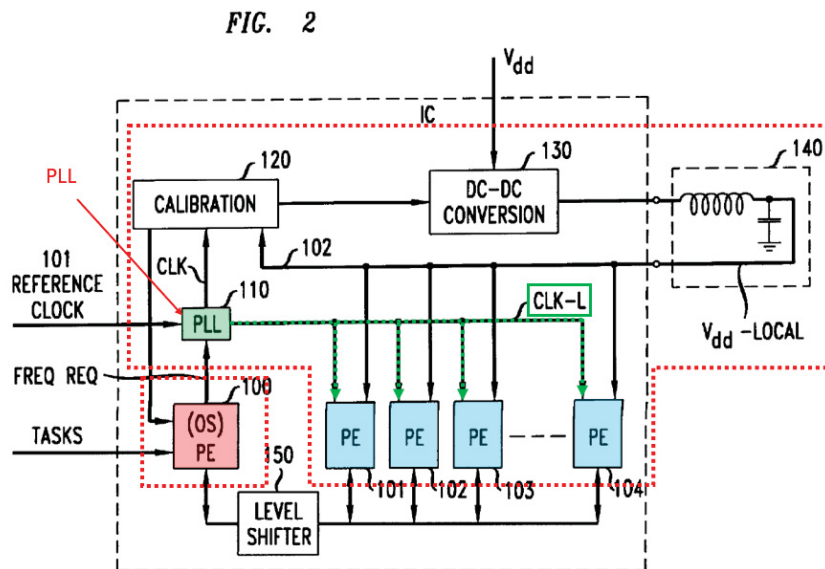
351. Second, both references Nicol and Naffziger address the same known problem—the need to balance performance with power consumption in electronic systems. For example, each of Nicol and Naffziger explain that systems or

components spend much of their time “idle” or “waiting” and only require peak performance for short portions of time. EX1008, 3:4-6 (“It may be noted that, typically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption.”); EX1015, 6:15-20 (“For instance, a microprocessor chip may be implemented in a multi-processor server system, such as a Utility Data Center, and during periods of low computational loads such microprocessor chip may not be required to be utilized and it may therefore be desirable to reduce its power limit during those periods.”).

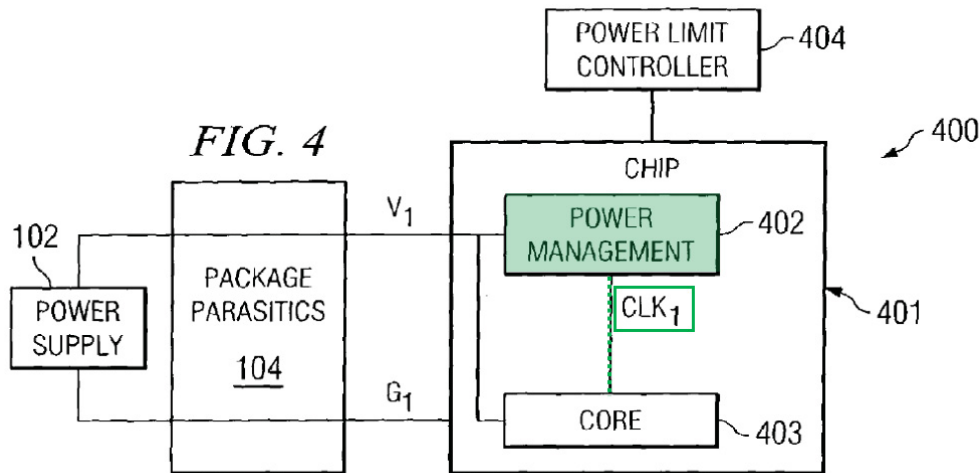
352. Third, Nicol and Naffziger both teach that *dynamically* responding to system conditions is beneficial for minimizing power consumption while assuring adequate performance. EX1008, 2:18-22 (“Improved performance of multi-processor chips is achieved by *dynamically controlling the processing load of chips* . . . as to minimize overall power consumption.”); EX1015, 2:22-27 (“It has been recognized in the prior art that if clock frequency (F) and supply voltage (V) are dynamically varied in response to computational load demands, then energy consumed per process can be reduced for the low computational periods, while retaining peak performance when required (i.e., for heavy computational periods).”).

353. Fourth, Nicol and Naffziger both teach changing frequency and voltage to change the power level of power islands on the integrated circuit. EX1008, 2:11-14 (“Thus, it is known that *varying supply voltage* to a chip can improve

performance by eliminating unexpected variability in the supply voltage, and by accounting for process and operating temperature variations.”); 3:24-27 (“This allows the *clock frequency of the PEs to be reduced*[.]”); EX1015, 6:49-51 (“For example, the chip’s *voltage* and *frequency* are preferably dynamically varied to provide optimum performance within a set power limit[.]”). To this end, Naffziger shows a “power management” block which outputs a clock to the core. EX1015, 11:50-53. A POSITA would have recognized that this “power management” block is performing the same function as the PLL in Nicol, which outputs a clock frequency to the PEs. Because Naffziger provides more detail on the circuitry in the power management block, a POSITA would have naturally looked at Naffziger to implement Nicol’s frequency scaling mechanism.



EX1008, Fig. 2.



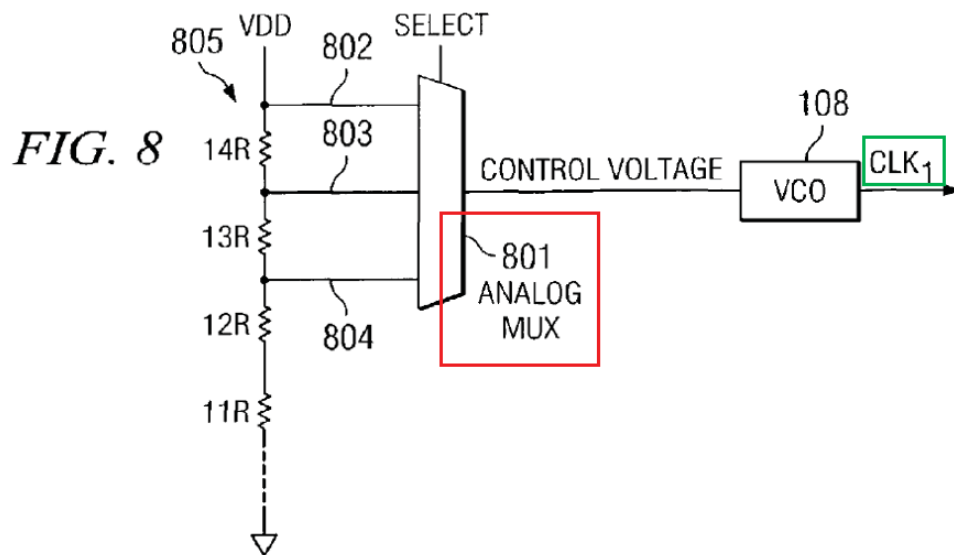
EX1015, Fig. 4.

354. Given the identical field of endeavor and the similarity of the disclosures, a POSITA would have naturally been inclined to incorporate Naffziger’s teachings in the context of Nicol’s system. In particular, a POSITA would have looked to Naffziger’s design choices for implementing a dynamically variable power limit in Nicol’s integrated circuit. Such a modification is merely the application of known techniques (conventional power management circuitry) to a known structure (Nicol’s integrated circuit) to yield predictable results (produce variable frequencies).

3. Claim 35

355. Claim 35 recites: “The system of claim 16 wherein the power control circuitry includes voltage multiplexing circuitry.” The Nicol-Naffziger combination renders this claim obvious. In its power management circuitry, Naffziger discloses a voltage multiplexor that allows choosing between various voltage levels for its

voltage-controlled oscillator (VCO). EX1015, 19:43-62, Fig. 8. Changing the control voltage for the VCO in turn changes the frequency of clock signal CLK₁.



EX1007, Fig. 8.

356. A POSITA would have been motivated to integrate Naffziger's multiplexer in Nicol to provide an efficient method for adaptively changing the voltage input to the VCO, which in turn allows for varying the clock signal frequency. Such a modification would have been a straightforward implementation of a known technique (PLL with a VCO, which incorporates voltage multiplexing) to predictably improve the frequency-switching ability in Nicol's system, resulting in overall performance and power savings improvement.

IX. ADDITIONAL REMARKS

357. I currently hold the opinions set expressed in this Declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

358. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Executed this 16th day of June, 2025

A handwritten signature in black ink, appearing to read 'Tajana Rosing', written over a horizontal line.

Tajana Rosing, Ph.D.
San Diego, California

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:
1[a]	determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands;
1[b]	determining at least one of actions to change a power consumption level of the one of the power islands to the target power level; and
1[c]	performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.
Claim 2	
2	The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit
Claim 3	
3	The method of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 4	
4	The method of claim 1 wherein the power islands comprise power sub-islands.
Claim 5	
5	The method of claim 1 wherein the power islands comprises multiple clock domains.
Claim 6	
6	The method of claim 1 wherein another one of the actions comprises selecting a clock for the one of the power islands.

Claim 7	
7	The method of claim 1 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.
Claim 8	
8	The method of claim 7 wherein the first voltage comprises a source voltage.
Claim 9	
9	The method of claim 7 wherein the first voltage comprises a threshold voltage.
Claim 10	
10	The method of claim 1 wherein another one of the actions comprises powering on the one of the power islands.
Claim 11	
11	The method of claim 1 wherein another one of the actions comprises powering off the one of the power islands.
Claim 12	
12	The method of claim 1 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 13	
13	The method of claim 1 further comprising: monitoring the power consumption level of the one of the power islands; determining whether a threshold level was crossed based on the power consumption level; and performing another one of the actions based on the crossing of the threshold level.
Claim 14	
14	The method of claim 1 further comprising saving a state of components within the one of the power islands.

Claim 15	
15	The method of claim 1 further comprising restoring a state of components within the one of the power islands.
Claim 16	
16[p]	A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:
16[a]	power control circuitry configured to control power for one of the power islands; and
16[b]	a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.
Claim 17	
17	The system of claim 16 wherein the power islands are delineated based on geographic factors of the integrated circuit.
Claim 18	
18	The system of claim 16 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 19	
19	The system of claim 16 wherein the power islands comprise power sub-islands.
Claim 20	
20	The system of claim 16 wherein the power islands comprise multiple clock domains.
Claim 21	
21	The system of claim 16 wherein another one of the actions comprises selecting a clock for the one of the power islands.

Claim 22	
22	The system of claim 16 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.
Claim 23	
23	The system of claim 22 wherein the first voltage comprises a source voltage.
Claim 24	
24	The system of claim 22 wherein the first voltage comprises a threshold voltage.
Claim 25	
25	The system of claim 16 wherein another one of the actions comprises powering on the one of the power islands.
Claim 26	
26	The system of claim 16 wherein another one of the actions comprises powering off the one of the power islands.
Claim 27	
27	The system of claim 16 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 28	
28	The system of claim 16 wherein the power manager is configured to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.
Claim 29	
29	The system of claim 16 wherein the power manager is configured to save a state of components within the one of the power islands.
Claim 30	
30	The system of claim 16 wherein the power manager is configured to restore a state of components within the one of the power islands.

Claim 31	
31	The system of claim 16 further comprising a bus coupled to the power manager and the power islands.
Claim 32	
32	The system of claim 16 wherein the power manager comprises a master manager configured to control power of the integrated circuit.
Claim 33	
33	The system of claim 16 wherein the power manager comprises a slave manager configured to control power of the one of the power islands.
Claim 34	
34	The system of claim 16 wherein the power control circuitry includes clock multiplexing circuitry.
Claim 35	
35	The system of claim 16 wherein the power control circuitry includes voltage multiplexing circuitry.
Claim 36	
36	The system of claim 16 wherein the power control circuitry includes level shifting circuitry.
Claim 37	
37[p]	A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising:
37[a]	power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands; and

37[b]	a software storage medium operational to store the power management software.
Claim 38	
38	The software product of claim 37 wherein the power islands are delineated based on geographic factors of the integrated circuit.
Claim 39	
39	The software product of claim 37 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 40	
40	The software product of claim 37 wherein the power islands comprise power sub-islands.
Claim 41	
41	The software product of claim 37 wherein the power islands comprise multiple clock domains.
Claim 42	
42	The software product of claim 37 wherein another one of the actions comprises selecting a clock for the one of the power islands.
Claim 43	
43	The software product of claim 37 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.
Claim 44	
44	The software product of claim 43 wherein the first voltage comprises a source voltage.
Claim 45	
45	The software product of claim 43 wherein the first voltage comprises a threshold voltage.
Claim 46	
46	The software product of claim 37 wherein another one of the actions comprises powering on the one of the power islands.

Claim 47	
47	The software product of claim 37 wherein another one of the actions comprises powering off the one of the power islands.
Claim 48	
48	The software product of claim 37 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 49	
49	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.
Claim 50	
50	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within the one of the power islands.
Claim 51	
51	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within the one of the power islands.

APPENDIX A

INTERESTS energy-efficient computing, computer architecture, embedded systems

PROFESSIONAL EXPERIENCE

05-pres. **UCSD** Distinguished Prof. & Fratamico Endowed Chair in the CSE & ECE; IEEE & ACM Fellow

08-pres Executive board member of San Diego Supercomputing Center

- leading a diverse research team on projects related to system energy-efficiency:
 - management and optimization of computing systems, acceleration of big data workloads
 - director of \$56M DARPA/SRC JUMP 2.0 PRISM Processing with Intelligent Storage and Memory Center
 - lead of Hyperdimensional computing work in \$40M DARPA/SRC JUMP 2.0 Cognitive Computing Center
 - hyperdimensional computing grants from DARPA, SRC, NSF; TSMC funded HDC chip tapeout
 - lead Organization & Hierarchy; and Precision Medicine in \$40M JUMP CRISP center
 - NSF AI TILOS Research Institute thrusts on chips and networks
 - head of the Large Scale Systems thrust in MuSyC center, with focus on datacenters
 - 10 year NSF ERC CIAN; lead of thrust on energy efficient datacenters; 30 companies, 12 universities
 - funded by NSF, DARPA, SRC, Oracle, Google, Microsoft, TI, Cisco, Qualcomm, CEC, Intel, Panasonic, Ericson, Broadcom, IBM and many others
 - Computing and resource management at and beyond the edge
 - director of \$16.3M AI for Healthy Living Center
 - \$28M TerraSwarm center; 22 faculty from 10 top institutions in the USA; leading the SmartCities theme
 - led context-aware distributed optimization in the Smart Grid as a part of ARPA-E NODES grant
 - NSF Early wildfire detection with drones and IoT; NSF MetaSense & CitiSense projects focused on mobile air quality sensing; coverage in NY Times and the Wall Street Journal
 - funded by DARPA, NSF, NIH, ARPA-E, DOE, LANL, CNS, Intel, IBM, TI, UTC, Raytheon, Oracle, Qualcomm, Panasonic, Broadcom, Ericson, Google, Microsoft, and others.
- published over ~420 publications; got a nomination for one of the best papers in 10 years of DATE, and TODAES journal paper was the top most downloaded paper, received many of best paper awards and nominations, and numerous invited talks in academia and industry
- led projects as a PI, co-PI or senior personnel totaling more than \$350M
- teaching embedded systems and computer engineering classes

97 – 04 STANFORD UNIVERSITY & HEWLETT-PACKARD LABS

- led a team of researchers developing products for wireless media market, interfaced with HP divisions; 5 patents
- obtained project funding for university collaborations and led collaboration at Stanford

93 – 97 ALTERA CORPORATION

- patented a testing methodology for FPLDs that enabled Altera to get to market 4 months sooner
- designed, evaluated and managed simulation and testing of 5 product families

92 – 93 UNIVERSITY OF ARIZONA

- design automation of high-speed VLSI interconnects; the simulator has been used by SRC member companies

88 – 92 NORTHERN ARIZONA UNIVERSITY

- modeled tether dynamics for orbiting stations to aid in the design of orbiting telescopes; designed an image processing environment for MRIs; designed an award-winning switched capacitor filter for TI

EDUCATION PhD in Electrical Engineering, Stanford University, 2001.

Thesis: *Energy Efficient System Design and Utilization*

MS in Engineering Management, Stanford University, 2000.

MS in Electrical and Computer Engineering, University of Arizona, 1993.

BS in Electrical Engineering, Northern Arizona University, 1992.

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3. Fatemeh Asgarinejad, Justin Morris, Tajana Rosing, Baris Aksanli, "PIONEER: Towards Highly Efficient and Accurate Hyperdimensional Computing using Learned Projections," ASPDAC'24
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49. Yeseong Kim, M. Imani, S. Gupta, M. Zhou, T. Rosing, "Massively Parallel Big Data Classification on a Programmable Processing In-Memory Architecture," ICCAD 21.
50. A. Paul, B. Khaleghi, G. Hota, Y. Xu, T. Rosing, Gert Cauwenberghs, "Attention State Classification with In-Ear EEG," BioCAS'21.
51. S. Salamat, N. Moshiri, T. Rosing, "FPGA Acceleration of Pairwise Distance Calculation for Viral Transmission Clustering" BIOCAS'21.
52. O. Gungor, B. Aksanli, T. Rosing, "CAHEROS: Constraint-Aware Heuristic Approach for Robust Sensor Placement" IEEE SENSORS'21.
53. O. Gungor, B. Aksanli, T. Rosing, "ENFES: Ensemble FEW-Shot Learning for Intelligent Fault Diagnosis with Limited Data," IEEE SENSORS'21.
54. Justin Morris, Si Thu Kaung Set, Gadi Rosen, Mohsen Imani, Baris Aksanli and Tajana Rosing, "AdaptBit-HD: Adaptive Model Bitwidth for Hyperdimensional Computing," ICCD'21
55. Yilun Hao, Saransh Gupta, Justin Morris, Behnam Khaleghi, Baris Aksanli and Tajana Rosing, "Stochastic-HD: Leveraging Stochastic Computing on Hyper-Dimensional Computing," ICCD'21.
56. A Sokolova, M Imani, A Huang, R Garcia, J Morris, T Rosing, B Aksanli, "MACcelerator: Approximate Arithmetic Unit for Computational Acceleration," ISQED'21.
57. M. Zhou, L. Wu, M. Li, N. Moshiri, K. Skadron, T. Rosing, "Ultra Efficient Acceleration for De Novo Genome Assembly via Near-Memory Computing," PACT'21
58. M. Zhou, G. Chen, M. Imani, S. Gupta, W. Zhang, T. Rosing, "PIM-DL: Boosting DNN Inference on Digital Processing In-Memory Architectures via Data Layout Optimizations," PACT'21.
59. S. Gupta, R. Camarota, T. Rosing, "Priv-PIM: Privacy-Preserved Processing in-Memory," SPSL'21.
60. Xiao Liu, Minxuan Zhou, Rachata Ausavarungnirun, Sean Eilert, Ameen Akel, Tajana Rosing, Vijaykrishnan Narayanan, Jishen Zhao, "FPRA: A Fine-grained Parallel RRAM Architecture," ISLPED'21.
61. K. Ergun, R. Ayoub, P. Mercati, T. Rosing, "Improving Mean Time to Failure of IoT Networks with Reliability-Aware Routing," CPSIoT 2021.
62. J. Ma, M. Ostertag, D. Bharadia, T. Rosing, "Frequency-aware Trajectory and Power Control for Multi-UAV Systems," INFOCOM-DroneCom'21.

63. Khaleghi B, Akel A, Curewitz K, Eno J, Eilert S, Moshiri N, Rosing T., "FPGA-based acceleration of primer trimming," 28th International Dynamics & Evolution of Human Viruses Conference 2021.
64. Kang J, Young C, Morris J, Akel A, Eilert S, Eno J, Curewitz K, Moshiri N, Rosing T., "GPU-Powered Phylogenetic Analysis for Large-scale Genomic Sequences," Int'l Dynamics & Evolution of Human Viruses Conf, 2021. Poster.
65. S. Salamat, N. Moshiri, T. Rosing, "FPGA-based acceleration of pairwise distance calculation for viral transmission clustering," International Dynamics & Evolution of Human Viruses Conf., 2021. Poster
66. O. Gungor, T. Rosing, B. Aksanli, "OPELRUL: Optimally Weighted Ensemble Learner for Remaining Useful Life Prediction of Industrial Machinery", IEEE International Conference on Prognostics and Health Management, 2021.
67. Mohsen Imani*, Zhuowen Zou, Samuel Bosch, Sanjay Anantha Rao, Sahand Salamat, Venkatesh Kumar, Yeseong Kim*, and Tajana Rosing, "Revisiting HyperDimensional Learning for FPGA and Low-Power Architectures," HPCA'21.
68. Namiko Matsumoto, Anthony Thomas, Tara Javidi and Tajana Rosing, "Hyperdimensional Computing and Spectral Learning," CogArch'21.
69. Sahand Salamat, Behnam Khaleghi, Armin Haj Aboutalebi, Joo Hwan Lee, Yang Seok Ki, Tajana Rosing, "NASCENT: Near-Storage Acceleration of Database Sort on SmartSSD," FPGA 2021.
70. M. Zhou, M. Li, M. Imani, T. Rosing, "HyGraph: Accelerating Graph Processing with Hybrid Memory-centric Computing," DATE'21.
71. Sahand Salamat, Jaeyoung Kang, Yeseong Kim, Mohsen Imani, Niema Moshiri and Tajana Rosing, "FPGA Acceleration of Protein Back-translation and Alignment," DATE'21.
72. Behnam K., Hanyang Xu, Justin Morris, Tajana S. Rosing, "tiny-HD: Ultra-Efficient Hyperdimensional Computing Engine for IoT Applications," DATE'21.
73. R. Garcia, F. Asgarinejad, B. Khaleghi, T. Rosing, M. Imani, "TruLook: A Framework for Configurable GPU Approximation", DATE, 2021.
74. Justin Morris, Kazim Ergun, Behnam Khaleghi, Mohsen Imani, Baris Aksanli, Tajana Rosing, "HyDREA: Towards More Robust and Efficient Machine Learning Systems with Hyperdimensional Computing," DATE'21.
75. M. Zhou, S. Gupta, M. Imani, Y. Kim, T. Rosing, "DP-Sim: A Full-stack Simulation Infrastructure for Digital Processing In-Memory Architecture," ASPDAC 2021.
76. S. Salamat, S. Shubhi, B. Khaleghi, T. Rosing, "Residue-Net: Multiplication-free Neural Network by In-situ, No-loss Migration to Residue Number Systems", ASP-DAC, 2021.
77. Y. Guo, S. Gupta, J. Kang, M. Imani, Y. Kim, J. Morris, T. Rosing, "HyperRec: Efficient Recommender Systems with Hyperdimensional Computing," ASPDAC 2021.
78. K. Ergun, R. Ayoub, P. Mercati, D. Liu, T. Rosing, "Energy and QoS-Aware Dynamic Reliability Management of IoT Edge Computing Systems," ASPDAC 2021.
79. Saransh Gupta, Mohsen Imani, Behnam Khaleghi, Niema Moshiri, and Tajana S. Rosing, "RAPIDx: A ReRAM Processing in-Memory Architecture for DNA Short Read Alignment," American Society of Human Genetics (ASHG), 2020. Poster
80. Salamat S, Kang J, Kim Y, Imani M, Moshiri N, Rosing T., "FPGA Acceleration of Protein Back-Translation and Alignment," American Society of Human Genetics (ASHG) 2020. Poster.
81. F. Asgarinejad, A. Thomas, T. Rosing. Detection of Epileptic Seizures from Surface EEG using Hyperdimensional Computing, EMBC, 2020.
82. B. Khaleghi, S. Salamat, T. Rosing, "Revisiting FPGA Routing under Varying Operating Conditions", FPT, 2020.
83. Y. Guo, X. Yu, K. Chaudhuri, T. Rosing, "Efficient Distributed Training in Heterogeneous Mobile Networks with Active Sampling," MSN'20.
84. X. Yu, X. Song, L. Cherkasova, T. Rosing, "Reliability-Driven Deployment in Energy-Harvesting Sensor Networks," CNSM'20.
85. K. Ergun, X. Yu, N. Nagesh, L. Cherkasova, P. Mercati, R. Ayoub, T. Rosing, "Simulating Reliability of IoT Networks with RelloT", IEEE 50th Conference on Dependable Systems and Networks (DSN), 2020.
86. K. Ergun, X. Yu, N. Nagesh, L. Cherkasova, P. Mercati, R. Ayoub, T. Rosing, "RelloT: Reliability Simulator for IoT Networks", International Conference on Internet of Things (ICIOT), 2020.
87. M. Imani, S. Pampana, S. Gupta, M. Zhou, Y. Kim, T. Rosing, "DUAL: Acceleration of Clustering Algorithms using Digital-based Processing In-Memory," MICRO 2020.

88. J. Morris, Y. Hao, S. Gupta, R. Ramkumar, J. Yu, M. Imani, B. Aksanli, T. Rosing, "Multi-label HD Classification in 3D Flash," VLSI-SOC 2020, **Invited paper**.
89. Y. Guo, M. Liu, T. Yang, T. S. Rosing, "Improved Schemes for Episodic Memory based Lifelong Learning Algorithm," NeurIPS 2020, **Spotlight presentation**.
90. O. Gungor, T. Rosing, B. Aksanli, "RESPIRE: Robust SEnSor Placement OptImization in PRobabilistic Environments," IEEE Sensors 2020. **Best paper nomination**
91. O. Gungor, J. Garnier, T. Rosing, B. Aksanli, "LENARD: Lightweight ENsemble LeARner for MeDium-term Electricity Consumption Prediction," IEEE SmartGridComm, 2020.
92. Y. Guo, X. Yu, K. Choudhuri, T. Rosing, "Efficient Distributed Training in Heterogeneous Mobile Networks with Active Sampling," IEEE Mobility, Sensing and Networking 2020.
93. Saransh Gupta, Mohsen Imani, Hengyu Zhao, Fan Wu, Jishen Zhao, and Tajana Rosing, "Implementing Binary Neural Networks in Memory with Approximate Accumulation," ISLPED 2020.
94. B. Khaleghi, S. Salamat, A. Thomas, F. Asgarinejad, Y. Kim, T. Rosing, "SHEARer: Highly-Efficient Hyperdimensional Computing by Software-Hardware Enabled Multifold AppRoximation", ISLPED, 2020.
95. Saransh Gupta, Justin Morris, Mohsen Imani, Ranganathan Ramkumar, Jeffrey Yu, Aniket Tiwari, Baris Aksanli, Tajana Rosing, "THRIFTY: Training with Hyperdimensional Computing across Flash Hierarchy," ICCAD 2020.
96. M. Ostertag, S. Al-Doweeshi, T. Rosing, "Efficient Training on Edge Devices Using Online Quantization," DATE 2020.
97. Yunhui Guo, Yandong Li, Liqiang Wang, Tajana Rosing, "AdaFilter: Adaptive Filter Fine-tuning for Deep Transfer Learning," AAAI 2020.
98. Yunhui Guo, Noel C. Codella, Leonid Karlinsky, James V. Codella, John R. Smith, Kate Saenko, Tajana Rosing, Rogerio Feris, "A Broader Study of Cross-Domain Few-Shot Learning," ECCV 2020.
99. M. Imani, M. Samragh, Y. Kim, S. Gupta, F. Koushanfar, T. Rosing "Deep Learning Acceleration with Neuron-to-Memory Transformation", HPCA, 2020.
100. Mohsen Imani*, Saikishan Pampana, Saransh Gupta, Minxuan Zhou, Yeseong Kim*, and Tajana Rosing, "DUAL: Acceleration of Clustering Algorithms using Digital-based Processing In-Memory," HPCA'20.
101. B. Khaleghi, M. Imani, T. Rosing "Prive-HD: Privacy-Preserved Hyperdimensional Computing", DAC, 2020.
102. H. Nejatollahi, S. Gupta, M. Imani, R. Cammarota*, T. Rosing, N. Dutt "CryptoPIM: In-Memory Acceleration for RLWE Lattice-based Cryptography", **best paper award**, DAC, 2020.
103. S. Gupta, M. Imani, J. Sim, A. Huang, F. Wu, H. Najafi, T. Rosing, "SCRIMP: A General Stochastic Computing Architecture using ReRAM in-Memory Processing", DATE, 2020.
104. Y. Kim, M. Imani, N. Moshiri*, T. Rosing, "GenieHD: Efficient DNA Pattern Matching Accelerator Using Hyperdimensional Computing", **best paper nomination**, DATE, 2020.
105. Behnam Khaleghi and Tajana S. Rosing, "[Thermal-Aware Design and Flow for FPGA Performance Improvement](#)", IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2019
106. B. Khaleghi, S. Salamat, M. Imani, T. Rosing, "FPGA Energy Efficiency by Leveraging Thermal Margin", ICCD, 2019.
107. K. Ergun, R. Ayoub, P. Mercati, T. Rosing, "Dynamic Optimization of Battery Health in IoT Networks", ICCD'19.
108. R. Chandrasekaran, Y. Guo, A. Thomas, M. Menarini, M. Ostertag, Y. Kim, T. S. Rosing, "Efficient Sparse Processing in Smart Home Applications," ACM SenSys ML, 2019.
109. M. Imani, J. Morris, S. Bosch, H. Shu, G. De Micheli, T. S. Rosing, "AdaptHD: Adaptive Efficient Training for Brain-Inspired Hyperdimensional Computing," BioCAS, 2019.
110. M. Imani, S. Gupta, T. Rosing "Digital-based Processing In-Memory: A Highly-Parallel Accelerator for Data Intensive Applications", ACM International Symposium on Memory Systems (MEMSYS), 2019.
111. Mohsen Imani, Tarek Nassar, Tajana Rosing, "[Moving Toward Real-Time Diagnostics using Brain-Inspired Hyperdimensional Computing](#)", AACR conference on Artificial Intelligence, Big Data, and Prediction in Cancer 2019
112. M Imani, S Gupta, Y Kim, T Rosing, "Deep Learning Acceleration using Digital-Based Processing In-Memory," SOCC 2020.
113. S. Salamat, B. Khaleghi, M. Imani, T. Rosing, "Workload-Aware Opportunistic Energy Efficiency in Multi-FPGA Platforms", ICCAD, 2019.
114. M Imani, S Bosch, M Javaheripi, B Rouhani, X Wu, F Koushanfar, T. Rosing, "Semihd: Semi-supervised learning using hyperdimensional computing," ICCAD 2019.

115. S Gupta, M Imani, T Rosing, "Exploring processing in-memory for different technologies," GLVLSI, 2019.
116. J. Morris, M. Imani, S. Bosch, A. Thomas, H. Shu, T. Rosing, "CompHD: Efficient Hyperdimensional Computing Using Model Compression". IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2019.
117. J. Sim, M. Kim, Y. Kim, S. Gupta, B. Khaleghi, T. Rosing, "Multi-bit Parallelized Sensing for Processing in Non-volatile Memory", NVMW, 2019.
118. J Sim, M Imani, W Choi, Y Kim, T Rosing, "Current-sensing efficient adder for processing-in-memory design," NVM 2019.
119. Mohsen Imani, Saransh Gupta, Yeseong Kim, and Tajana S. Rosing, "FloatPIM: In-Memory Acceleration of Deep Neural Network Training with High Precision", ISCA, 2019
120. Mohsen Imani, Yeseong Kim, Sadegh Riyazi, John Merssely, Patrick Liu, Farinaz Koushanfar, and Tajana S. Rosing, "A Framework for Collaborative Learning in Secure High-Dimensional Space", IEEE Cloud Computing (CLOUD), 2019
121. Mohsen Imani, Yeseong Kim, Thomas Worley, Saransh Gupta, and Tajana S. Rosing, "[HDCluster: An Accurate Clustering Using Brain-Inspired High-Dimensional Computing](#)", IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2019
122. Mohsen Imani, John Merssely, Fan Wu, Wang Pi, and Tajana S. Rosing, "[A Binary Learning Framework for Hyperdimensional Computing](#)", IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2019
123. Mohsen Imani, Ricardo Garcia, Andrew Huang, and Tajana S. Rosing, "[CADE: Configurable Approximate Divider for Energy Efficiency](#)", IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2019
124. Xiao Liu, Minxuan Zhou, Tajana Rosing, and Jishen Zhao, "HR3AM: A Heat Resilient Design for RRAM-based Neuromorphic Computing", ISLPED 2019
125. Minxuan Zhou, Mohsen Imani, Saransh Gupta, Yeseong Kim, and Tajana Rosing, "[Thermal-Aware Design and Management for Search-based In-Memory Acceleration](#)", IEEE/ACM Design Automation Conference (DAC), 2019
126. Mohsen Imani, Tarek Nassar, Justin Morris, Tajana Rosing, "DNA Sequencing using Brain-inspired Hyperdimensional Computing", GOMACTech Conference, 2019
127. Mohsen Imani, Yeseong Kim, Saransh Gupta, Daniel Peroni, and Tajana S. Rosing, "In-Memory Acceleration of Deep Neural Network", GOMACTech Conference, 2019
128. Mohsen Imani, Tarek Nassar, Tajana Rosing, "Brain-Inspired Hyperdimensional Computing for Real-Time Health Analysis", IEEE International Conference on Biomedical and Health Informatics (BHI), 2019
129. Mohsen Imani, Saransh Gupta, Yeseong Kim, Minxuan Zhou, and Tajana S. Rosing, "[DigitalPIM: Digital-based Processing In-Memory for Big Data Acceleration](#)", ACM Great lakes symposium on VLSI (GLSVLSI), 2019
130. Anthony Thomas, Yunhui Guo, Yeseong Kim, Baris Aksanli, Arun Kumar, and Tajana Rosing, "[Hierarchical and Distributed Machine Learning Inference Beyond the Edge](#)", IEEE International Conference on Networking, Sensing and Control (ICNSC), 2019.
131. Daniel Peroni, Mohsen Imani, Hamid Nejatollahi, Nikil Dutt, and Tajana S. Rosing, "ARGA: Approximate Reuse for GPGPU Acceleration", IEEE/ACM Design Automation Conference (DAC), 2019
132. Mohsen Imani, Alice Sokolova, Ricardo Garcia, Andrew Huang, Fan Wu, and Tajana S. Rosing, "ApproxLP: Approximate Multiplication with Linearization and Iterative Error Control", IEEE/ACM Design Automation Conference (DAC), 2019
133. Mohsen Imani, Justin Morris, John Merssely, Helen Shu, Yaobang Deng, and Tajana S. Rosing, "BRIC: Locality-based Encoding for Energy-Efficient Brain-Inspired Hyperdimensional Computing", IEEE/ACM Design Automation Conference (DAC), 2019. **Best paper nomination**
134. Mohsen Imani, Sahand Salamat, Saransh Gupta, Jiani Huang, and Tajana S. Rosing, "[FACH: FPGA-based Acceleration of Hyperdimensional Computing by Reducing Computational Complexity](#)", IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2019
135. Michael H Ostertag, Nikolay Atanasov, Tajana Simunic Rosing, "Robust Velocity Control for Minimum Steady State Uncertainty in Persistent Monitoring Applications", American Controls Conference, 2019. **Best poster award**
136. Saransh Gupta, Mohsen Imani, Behnam Khaleghi, Venkatesh Kumar, and Tajana S. Rosing, "RAPID: A ReRAM Processing in Memory Architecture for DNA Sequence Alignment", International Symposium on Low Power Electronics and Design (ISLPED), 2019

137. Mohsen Imani, Sahand Salamat, Behnam Khaleghi, Mohammad Samragh, Farinaz Koushanfar, and Tajana S. Rosing, "[SparseHD: Algorithm-Hardware Co-Optimization for Efficient High-Dimensional Computing](#)", International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2019
138. Sahand Salamat, Mohsen Imani, Behnam Khaleghi, and Tajana S. Rosing, "[F5-HD: Fast Flexible FPGA-based Framework for Refreshing Hyperdimensional Computing](#)", ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2019
139. Yunhui Guo, Honghui Shi, Abhishek Kumar, Kristen Grauman, Tajana Rosing, Rogério Schmidt Feris, "[SpotTune: Transfer Learning through Adaptive Fine-tuning](#)", In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2019
140. Yunhui Guo, Yandong Li, Liqiang Wang, Tajana Rosing, "[Depthwise Convolution is All You Need for Learning Multiple Visual Domains](#)", The Thirty-Third AAAI Conference on Artificial Intelligence (AAAI), 2019
141. Joonseop Sim, Saransh Gupta, Mohsen Imani, Yeseong Kim, and Tajana S. Rosing, "[UPIM : Unipolar Switching Logic for High Density Processing-in-Memory Applications](#)", ACM Great lakes symposium on VLSI (GLSVLSI), 2019
142. Yeseong Kim, Ankit More, Emily Shriver, and Tajana S. Rosing, "[Application Performance Prediction and Optimization Under Cache Allocation Technology](#)", IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2019
143. Joonseop Sim, Minsu Kim, Yeseong Kim, Saransh Gupta, Behnam Khaleghi and Tajana Rosing, "[MAPIM: Mat Parallelism for High Performance Processing in Non-volatile Memory Architecture](#)", IEEE International Symposium on Quality Electronic Design (ISQED), 2019
144. M. Imani, M. Samragh, Y. Kim, S. Gupta, F. Koushanfar, T. Rosing, "A Fully Digital In-Memory Acceleration of Deep Neural Network" Non-Volatile Memory Workshop (NVMW). 2019.
145. Daniel Peroni, Mohsen Imani, Tajana Rosing, "[ALook: Adaptive Lookup for GPGPU Acceleration](#)", IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2019
146. Minxuan Zhou, Mohsen Imani, Saransh Gupta, Tajana Rosing, "[GRAM: Graph Processing in a ReRAM-based Computational Memory](#)", IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2019
147. Mohsen Imani, Sahand Salamat, Jiani Huang, Saransh Gupta, Tajana Rosing, "[FACH: FPGA-based Acceleration of Hyperdimensional Computing by Reducing Computational Complexity](#)", IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2019
148. Joonseop Sim, Mohsen Imani, Woojin Choi, Yeseong Kim, Tajana Rosing, "LUPIS: Latch-Up Based Ultra Efficient Processing-in-Memory System", **Best paper nomination**, ISQED'18.
149. Minxuan Zhou, Mohsen Imani, Saransh Gupta, and Tajana Rosing, "GAS: A Heterogeneous Memory Architecture for Graph Processing," ISLPED '18.
150. Mohsen Imani, Tarek Nassar, Abbas Rahimi, Tajana Rosing "HDNA: Energy-Efficient DNA Sequencing Using Hyperdimensional Computing", IEEE International Conference on Biomedical and Health Informatics (BHI), 2018.
151. M. Imani, Y. Kim, T. Rosing, "Visual Object Recognition Accelerator Based on Approximate In-Memory Processing", Non-Volatile Memory Workshop (NVMW), 2018.
152. M. Imani, A. Rahimi, D. Kong, T. Rosing, Jan Rabaey, "Non-Volatile Associative Memory to Accelerate Brain-inspired Hyperdimensional Computing" Non-Volatile Memory Workshop (NVMW), 2018 .
153. M. Imani, S. Gupta, T. Rosing, "Accelerating Multiplication and Parallelizing Operations in Non-Volatile Memory" Non-Volatile Memory Workshop (NVMW), 2018.
154. M. Imani, C. Huang , D. Kong, T. Rosing, "Hierarchical Hyperdimensional Computing for Energy Efficient Classification", IEEE/ACM Design Automation Conference (DAC), 2018.
155. M. Imani, R. Garcia , S. Gupta, T. Rosing, "Configurable Floating Point Multiplier for Approximate Computing", IEEE/ACM Design Automation Conference (DAC), 2018.
156. S. Gupta, M. Imani, T. Rosing, "Processing In-Memory Architecture for Multiple Memory Technology", IEEE/ACM Design Automation Conference (DAC), 2018.
157. M. Imani, R. Garcia, S. Gupta, T. Rosing "RMAC: Runtime Configurable Floating Point Multiplier for Approximate Computing", IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2018.
158. M. Zhou, M. Imani, S. Gupta, T. Rosing "GAS: A Heterogeneous Memory Acceleration for Graph Processing", IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), 2018.

159. M. Imani, S. Gupta, T. Rosing, "GenPIM: Generalized Processing In-Memory to Accelerate Data Intensive Applications ", IEEE/ACM Design Automation and Test in Europe Conference (DATE), 2018.
160. S. Gupta, M. Imani, T. Rosing, "FELIX: Fast and Energy-Efficient Logic in Memory" IEEE/ACM International Conference On Computer Aided Design (ICCAD), 2018.
161. M. Imani, Y. Kim, T. Rosing, "Brain-Inspired Hyperdimensional Computing: An Efficient Classifier for Embedded Devices" IEEE/ACM International Conference On Computer Aided Design (ICCAD), 2018.
162. Y. Kim, M. Imani, T. Rosing, "Efficient Human Activity Recognition Using Hyperdimensional Computing", IEEE Conference on Internet of Things (IoT), 2018.
163. J.Sim, M. Imani, W. Choi, Y. Kim, T. Rosing, "LUPIS : Latch-Up Based Ultra Efficient Processing In-Memory System", IEEE International Symposium on Quality Electronic Design (ISQED), 2018. (Best paper nomination).
164. M. Imani, M. Masich, D. Peroni, P. Wang, T. Rosing, "CANNA: Neural Network Acceleration using Configurable Approximation on GPGPU", IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2018.
165. M. Imani, D. Peroni, T. Rosing, "Resistive Content Addressable Memory for Configurable Approximation", GOMACTech Conference, 2018.
166. M. Imani, M. Masich, T. Rosing, "Training Acceleration of Deep Neural Network on Configurable GPGPU" Techon SRC Conference, 2018 .
167. M. Imani, T. Nassar, T. Rosing, "Moving Toward Real-Time Diagnostics using Brain-Inspired Hyperdimensional Computing", AACR conference on Artificial Intelligence, Big Data, and Prediction in Cancer, 2018.
168. S. Salamat, M. Imani, S. Gupta, T. Rosing, "RNSnet: In-Memory Neural Network Acceleration Using Residue Number System" IEEE International Conference on Rebooting Computing (ICRC), 2018.
169. M. Imani, D. Peroni, T. Rosing, "Program Acceleration Using Nearest Distance Associative Search", IEEE International Symposium on Quality Electronic Design (ISQED), 2018.
170. Anthony Thomas, Yunhui Guo, Yeseong Kim, Baris Aksanli, Arun Kumar, Tajana S. Rosing. "Hierarchical and Distributed Machine Learning Inference Beyond the Edge." In Government Microcircuit Applications & Critical Technology Conference (GOMACTech), 2018.
171. Y. Kim, A. Moore, E. Shriver, T. S. Rosing, "P4: Phase-Based Power/Performance Prediction of Heterogeneous Systems via Neural Networks," ICCAD'17.
172. P. Mercati. R. Ayoub, E. Samson, F. Paterna, M. Beuchat, M. Kisnevsky, T. S. Rosing, "Multi-variable Dynamic Power Management for the GPU Subsystem," DAC'17.
173. C. Chan, M. Ostertag, A. S. Akyurek, T. S. Rosing. "Context-Aware System Design," Invited paper to SPIE 2017.
174. B. Aksanli, J. Venkatesh, C. Chan, A. S. Akyurek, T. S. Rosing, "Context-Aware and User-Centric Residential Energy Management," PerIoT, 2017.
175. N. Mousavi, B. Aksanli, A. S. Akyurek, T. S. Rosing, "Accuracy-Resource Tradeoff for Edge Devices in Internet of Things," SmartEdge 2017.
176. W. Cui, Y. Kim, T. S. Rosing, "Cross-Platform Machine Learning Characterization for Task Allocation in IoT Ecosystems," **Best paper award**, IEEE CCWC, 2017.
177. M. Imani, A. Rahimi, D. Kong, T. Rosing, J. M. Rabaey "Exploring Hyperdimensional Associative Memory", HPCA'17.
178. M. Imani, S. Gupta, T. Rosing "Ultra-Efficient Processing In-Memory for Data Intensive Applications", DAC'17.
179. M. Imani, D. Peroni, T. Rosing "CFPU: Configurable Floating Point Multiplier for Energy-Efficient Computing", DAC'17 (**Best poster at ResearchExpo**).
180. Y. Kim, M. Imani, T. Rosing "ORCHARD: Visual Object Recognition Accelerator Based on Approximate In-Memory Processing", ICCAD'17.
181. Mohsen Imani, Yeseong Kim, and Tajana S. Rosing, "Brain-Inspired Hyperdimensional Computing: An Efficient Classifier for Embedded Devices," ICCAD'17.
182. M. Imani, A. Rahimi, D. Kong, T. Rosing, J. M. Rabaey "Hardware Acceleration of Brain-inspired Hyperdimensional Computing", ICCAD VMC 2017.
183. M. Imani, D. Peroni, Y. Kim, A. Rahimi and T. Rosing, "Efficient Neural Network Acceleration on GPGPU using Content Addressable Memory," DATE'17.
184. M. Samragh, M. Imani, F. Koushanfar and T. Rosing, "LookNN: Neural Network with No Multiplication," DATE'17.
185. M. Imani, S. Gupta, A. Arredondo, T. Rosing "Efficient Query Processing in Crossbar Memory", ISLPED'17.

186. M. Imani, Y. Kim, T. Rosing, "MPIM: Multi-Purpose In-Memory Processing using Configurable Resistive Memory" ASP-DAC'17.
187. M. Imani, D. Kong, A. Rahimi, T. Rosing, "VoiceHD: Hyperdimensional Computing for Efficient Speech Recognition", ICRC'17.
188. M. Imani, Y. Kim, T. Rosing "NNeigine: Ultra-Efficient Nearest Neighbor Accelerator Based on In-Memory Computing", ICRC'17.
189. J. Sim, M. Imani, Y. Kim, T. Rosing "Enabling Efficient System Design Using Vertical Nanowire Transistor Current Mode Logic", VLSI-SoC'17.
190. M. Imani, D. Kong, A. Rahimi and T. Rosing, Jan Rabaey, "Brain-Inspired Hyperdimensional Computing: Robust, Scalable and Energy Efficient Classifier," Techcon'17.
191. Y. Kim, M. Imani and T. Rosing, "General-Purpose Online Classification Accelerator via In-Memory Computing," Techon'17.
192. M. Imani, T. Rosing, "CAP: Configurable Resistive Associative Processor for Near-Data Computing," IEEE ISQED'17.
193. M. Imani, D. Peroni, A. Rahimi, T. Rosing, "Non-volatile Content Addressable Memory for Computing Acceleration" NVMW'17.
194. M. Imani, Y. Kim, T. Rosing, "In-Memory Processing to Support Search-Based and Bitwise Computation" NVMW'17.
195. Pietro Mercati, Francesco Paterna, Andrea Bartolini, Mohsen Imani, Luca Benini, Tajana S. Rosing, "VarDroid: Online Variability Emulation in Android/Linux Platforms", GLSVLSI, 2016
196. Akanksha Maurya, Alper Sinan Akyurek, Baris Aksanli and Tajana Rosing, "Time-Series Clustering for Data Analysis in Smart Grid", SmartGridComm, 2016.
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199. Jinseok Yang, S. Tilak, T. S. Rosing, "Interactive Context-aware Power Management Technique for Optimizing Sensor Network Lifetime," SENSORNETS'16, nominated for the **Best paper award**.
200. Yeseong Kim, Pietro Mercati, and Tajana S. Rosing, "Power Efficient, Hierarchical, Introspection Framework for HPC Systems," TECHCON SRC Conference (TECHCON 2016), September 2016
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202. M. Imani, Y. Kim, A. Rahimi, T. Rosing, "ACAM: Approximate Computing Based on Adaptive Associative Memory with Online Learning" ISLPED'16.
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205. M. Imani, S. Patil, T. Rosing, "MASC: Ultra-Low Energy Multiple-Access Single-Charge TCAM for Approximate Computing" DATE'16.
206. M. Imani, Y. Cheng, T. Rosing, "Processing Acceleration with Resistive Memory-based Computation" MEMSYS'16.
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350. J. Rozenblit, T. Simunic: "Techniques for Intelligent VLSI Interconnect Design," DMC'94.
351. T. Simunic, J. Rozenblit: "Reduction of Signal Delay and Crosstalk in Electronic Packaging," EPEP'93.
352. T. Simunic, P. Hsu, J. Rozenblit, C. Wolff, J. Prince, A. Cangellaris: "An Integrated Framework for Modeling and Simulation of Electronic Packaging," TECHCON'93

PREPRINTS

1. S Gupta, R Cammarota, T Rosing, "MemFHE: End-to-End Computing with Fully Homomorphic Encryption in Memory," arXiv:2204.12557
2. R. Fielding-Miller, S. Karthikeyan, T. Gaines, T. Rosing et al., "'Wastewater and surface monitoring to detect COVID-19 in elementary school settings: The Safer at School Early Alert project", Medrxiv, 2021.
3. R Cammarota, M Schunter, A Rajan, F Boemer, Á Kiss, A Treiber, ... T. Rosing, "Trustworthy ai inference systems: An industry research view," arXiv:2008.04449
4. S Bosch, AS de la Cerda, M Imani, TS Rosing, G De Micheli, "QubitHD: A stochastic acceleration method for HD computing-based machine learning," arXiv:1911.12446
5. M Imani, M Samragh, Y Kim, S Gupta, F Koushanfar, T Rosing, "Rapidnn: In-memory deep neural network acceleration framework," arXiv:1806.05794
6. S Salamat, T Rosing, "FPGA Acceleration of Sequence Alignment: A Survey," arXiv:2002.02394

BOOK CHAPTERS

1. M. Imani, T. Rosing, "Approximate CPU and GPU design using emerging memory technologies," Approximate Circuits, Book chapter in Approximate Circuits by Springer 2019.
2. S. Patil, Y. Kim, K. Korgaonkar, I. Awwal, T. S. Rosing, "Characterization of User's Behavior Variations for Design of Replayable Mobile Workloads," in Mobile Computing, Applications, and Services, Volume 162 of the series Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering, pp 51-71, January, 2016.
3. Baris Aksanli, Jagannathan Venkatesh, Inder Monga, and Tajana Rosing, "Reable Energy Prediction for Improved Utilization and Efficiency in Datacenters and Backbone Networks," Computational Sustainability Springer Book Chapter, 2015.
4. Ayse K. Coskun, J. Ayala, D. Atienza, T. Simunic Rosing: "Thermal Modeling and Management of Liquid-Cooled 3D Stacked Architectures," Editors: J. Becker, M. Johann and R. Reis. Springer, VLSI-SoC: Technologies for Systems Integration (ISBN: 978-3-642-23119-3), p. 34-55, 2011.
5. G. Dhiman, R. Ayoub, T. Simunic Rosing, "Energy and Thermally Aware Scheduling in Datacenters," in Energy-Efficient Distributed Computing, Edited by Albert Zomaya & Young Choon Lee, Wiley-Interscience 2010.
6. N. Nikzad, P. Aghera, P. Zappi, T. Simunic Rosing, "Energy Management in Heterogeneous Wireless Healthcare Networks," in Energy-Efficient Distributed Computing, Edited by Albert Zomaya & Young Choon Lee, Wiley-Interscience 2010.
7. Ayse K. Coskun, J. Ayala, D. Atienza, T. Simunic Rosing. Thermal Modeling and Management of Liquid-Cooled 3D Stacked Architectures. Editors: J. Becker, M. Johann and R. Reis. Springer, VLSI-SoC: Technologies for Systems Integration (ISBN: 978-3-642-23119-3), p. 34-55, 2011.

8. Y. Lu, E. Chung, T. Simunic, L. Benini, G. De Micheli: "Quantitative Comparison of Power Management Algorithms", in *The Most Influential Papers of 10 Years DATE*, Edited by Lauwereins, Rudy; Madsen, Jan, Springer-Verlag, 2008.
9. J. Kim, T. Simunic Rosing, "Power-aware resource management techniques for low-power embedded systems," in *Handbook of Real-Time and Embedded Systems*, Edited by S. H. Son, I. Lee, J. Y-T Leung, Taylor-Francis Group LLC, 2006.
10. T. Simunic: "Dynamic Management of Power Consumption" in *Power Aware Computing*, Edited by R. Graybill, R. Mehlem, Kluwer Academic Publishers pp.102-125, 2002.

PATENTS

1. TS Rosing, M Imani, Y Kim, B Khaleghi, AN Moshiri, S Gupta, V Kumar, "Methods, circuits, and articles of manufacture for searching within a genomic reference sequence for queried target sequence using hyper-dimensional computing techniques," US20220059189, Priority 2021-02-24.
2. TS Rosing, J Morris, M Imani, Y Kim, J Messerly, Y Guo, B Khaleghi, "Circuits, methods, and articles of manufacture for hyper-dimensional computing systems and related applications," US20220019441A1, Priority 2020-07-14;
3. S Salamat, M Imani, B Khaleghi, T Rosing," Methods and systems configured to specify resources for hyperdimensional computing implemented in programmable devices using a parameterized template for hyperdimensional computing," US20210334703A1, Priority date 2020-02-21.
4. B Khaleghi, TS Rosing, M Imani, S Salamat, "Methods of providing trained hyperdimensional machine learning models having classes with reduced elements and related computing systems," US20210326756A1, Priority 2020-04-07.
5. M Imani, Y Kim, T Rosing, F Koushanfar, MS Riazi, "Systems, circuits and computer program products providing a framework for secured collaborative training using hyper-dimensional vector based data encoding/decoding and related," US20200410404A1, Priority 2019-06-27.
6. A. Acquaviva, B. Luca, T. Rosing, "Application-drive method and apparatus for limiting power consumption in a processor-controlled hardware platform," US 7272730, Priority 2003-07-31.
7. Tajana S Rosing, Ozgur Celebican, "Arrangement and method for estimating and optimizing energy consumption of a system including I/O devices," WO2005076166A1, Priority 2004-01-30
8. T. Simunic Rosing, "Device and method for identifying a communication interface that performs an operating parameter closer to a desired performance level than another communication interface performs the operating parameter," US7246181B2, Priority date 2004-09-14.
9. V. Deolalikar, T. Simunic: "Method and system for power control in wireless portable devices using wireless channel characteristics",US20050170801A1, Priority date 2004-01-30.
10. T. Simunic, A. Acquaviva, L. Benini, "Application-driven method and apparatus for limiting power consumption in a processor-controlled hardware platform," US7272730B1, Priority date 2003-07-31.
11. T. Simunic, N. Mehta, C. Crome : "Method and Device for Test Vector Analysis"; US6197605B1, Priority date 1996-04-10.

THESES

1. B. Khaleghi, "Hardware-Algorithm Co-design for Efficient and Privacy-Preserved Edge Computing," 2022.
2. U. Mallappa, "AI for Design Optimization and Design for AI Acceleration," 2022.
3. K. Ergun, "Energy-Efficient and Reliability-Driven Management of IoT Systems," 2022.
4. J. Morris, "Fast, Efficient, and Robust Learning with Brain-Inspired Hyperdimensional Computing," 2022.
5. S. Gupta, "Efficient and Secure Learning across Memory Hierarchy," 2021.
6. S. Salamat, "Fast and Energy Efficient Big Data Processing on FPGAs," 2021.
7. M. Imani, "Machine Learning in IoT Systems: From Deep Learning to Hyperdimensional Computing," 2020.
8. Y. Kim, "Efficient Learning in Heterogeneous Internet of Things Ecosystems," 2020.
9. Y. Guo, "Efficient Learning across Multiple Domains with Deep Neural Networks," 2020.
10. J. Sim, "Architecting Non-volatile Memory for High Bandwidth Systems," 2019.
11. D. Peroni, "Approximate Computing for GPGPU Acceleration," PhD, 2019.
12. C. Chan, "Context-aware Platform Design and Optimization," PhD, 2017.
13. A. S. Akyurek, "Optimized Energy Control in Power Distribution Systems," PhD, 2017.

14. P. Mercati, "Power, Thermal, Reliability and Variability Management of Mobile Devices," PhD, 2016.
15. J. Venkatesh, "A Context-aware Approach for Automation of End-User Elements in the Smart Grid," PhD, 2016.
16. J. Yang, "Energy Efficient Data Aggregation in Sensor Networks," PhD, 2015.
17. B. Aksanli, "Energy and Cost Efficient Datacenters," PhD, 2015.
18. R. Strong, "Low-Latency Techniques for Improving System Energy Efficiency," PhD, 2013.
19. V. Kontorinis, "Adaptive Architectures for Peak Power Management," PhD, 2013.
20. S. Sharifi, "Accurate Temperature Sensing and Efficient Dynamic Thermal Management in MPSoCs," PhD, 2011.
21. R. Ayoub, "Temperature and Cooling Management in Computing Systems," PhD, 2011.
22. G. Dhiman, "Dynamic Workload Characterization for Energy Efficient Computing," PhD, 2011.
23. R. Herrmann, "Context based energy management for sensing applications," MS, 2011.
24. A. K. Coskun, "Efficient Thermal Management for Multiprocessor Systems," PhD 2009.
25. E. Regini, "Resource management in heterogeneous wireless sensor networks," MS 2009.
26. J. Steck, "Energy and task management in energy harvesting wireless sensor networks for structural health monitoring," MS 2009.
27. C. Bergonzini, "Management of solar harvested energy in actuation based embedded systems," MS 2009.
28. D. Lim, "Distributed proxy-layer scheduling in heterogeneous wireless networks," MS 2007.
29. D. Musiani, "Design of an active sensing platform for wireless structural health monitoring," MS 2007.
30. T. Simunic, "Energy efficient system design and utilization," PhD 2001.
31. T. Simunic, "VLSI interconnect design automation using qualitative and quantitative techniques," MS 1993.

ACADEMIC COMMUNITY SERVICE

- Invited to Dagstuhl Seminar on Power and Energy-aware Computing on Heterogeneous Systems, 2022
- Keynote at iTherm, 2022
- Keynote at HPCA-CogArch 2022
- Invited to participate in National AI Research Resource Task Force, August 2021.
- IEEE Fellow Award Committee, 2021.
- DARPA Electronics Resurgence Initiative - Invited speaker & invited demo, 2020, 2021
- NeurIPS reviewer 2021
- Invited talk at Annual Symposium of Academy of Neuroscience & Architecture on Quantified Buildings, Quantified Self, 2021
- Keynote at IGCC, 2021
- Keynote at IEEE Sensors, 2021
- IEEE CEDA Kuh Early Career Award Committee 2018, 2019, 2020
- Distinguished speaker UC Riverside, 2019.
- Distinguished speaker UC Irvine 2019
- TPC track chair, DATE, 2019-2020
- DAC women in EDA invited panel speaker, 2019
- JUMP CBRIC invited speaker, 2019
- JUMP ADA Invited speaker, 2019
- DARPA ERI Invited speaker, 2019
- ICCAD TPC member, 2019
- DATE women in EDA invited panel speaker 2018
- Keynote speaker at IEEE/ACM Workshop on Variability Modeling and Characterization, 2018
- Keynote speaker at IEEE Reliability Symposium 2018
- GLOBECOMM 2015 Executive committee member, Tutorials Chair
- Invited speaker at WIC Panel, 2015.
- ISCC'2013 chair of the TPC executive committee
- DATE 2011-2012, 2012-2013 TPC Track Chair
- ISLPED 2012 TPC Track Chair
- DAC 2013 WIP Chair, ESS Chair
- Associate Editor for IEEE Transactions on Mobile Computing 2008-2012

- Associate Editor for IEEE Transactions on Circuits and Systems 2003-2005
- Invited speaker at WEED-ESSA panel on "Cross-stack Energy-optimization - Fact or Fiction?" on June 9th at ISCA, Portland.
- CRA-W workshop presentations
- Session chair for DATE, ISLPED, DAC, ICCAD
- Technical paper committee for many conferences, such as DAC, DATE, ASPLOS, IPSN, ICCAD, ISLPED, ISCA, MMCN, HotPower, SECON.
- Reviewer for a number of publications ranging from Proceedings of the IEEE, to IEEE Transactions on Computers, IEEE Transactions on VLSI, IEEE Transactions on CAD, IEEE Transactions on Mobile Computing, IEEE Computer, IEEE Transactions on Computers, IEEE Micro, ACM TECS, ACM TODAES, ACM TOSN, and conferences such as DATE, DAC, ISLPED, ICCAD, IPSN and many others
- Technical reviewer for Alfred Sloan Grant & Dutch Ministry of Economic Affairs, Estonian NSF

UNIVERSITY SERVICE

- CSE Undergraduate Program Committee, 2022-2024
- Committee on Committees, 2019-2022.
- JSOE Dean's Faculty Council, 2019-2022.
- Ad-hoc committees for endowed chair appointments, 2014-2022
- Ad-hoc committees within CSE, 2014-2022
- Invited speaker at CS PhD Information Session, 2021
- CSE Diversity Coordinator 2019-2020
- SP-SOC 2018-2019
- LPSOE recruiting committee, 2017-2019
- HDSI Faculty Member of Clusters on Data Science Theory, Methods and Tools; Cross-cutting areas and systems, Improving Quality of Life, and Enabling Scientific Discovery 2018-pres.
- Dean Pisano Performance Review Committee CSE Representative 2018
- Ad-hoc committee for two endowed chair appointments in SOE, 2018.
- LPSOE recruiting committee, 2017-2019
- SP-SOC committee member 2018-pres.
- Co-creator of Jean Ferrante diversity scholarship (with Arun Kumar) 2018
- School of Engineering Building Committee 2015-2018
- UCSD Undergraduate Council Member 2016-2018
- Precision Medicine SOE recruit committee, 2017-2018
- Chair of Undergraduate Council's Department of Math Review Committee, 2017.
- Chair of Undergraduate Council's Department of Religion Review Committee, 2018.
- Director for \$10M UCSD-IBM AI for Healthy Living Center, 2017-2018.
- Diversity Coordinator for CSE Department. 2016 - Present
- IDEA Center Board Member, 2017-pres.
- University Faculty Recruitments for Sensors, Devices, and Imaging Committee, 2017-18.
- Mental Health & Technology Center executive board faculty member, 2017-pres.
- Qualcomm Institute (CalIT2) ORU Review, 2017.
- Featured Speaker at the UCSD's Founder's Symposium, "An Evening of Nonconventional Wisdom: AI for Healthy Aging," 2017.
- Teaching faculty recruit committee, 2017-pres.
- Board member, IDEA Center, 2017-pres.
- Diversity coordinator for CSE Department, 2017-pres.
- Dean review committee 2018
- Triton Drone Racing club faculty advisor 2016-2018
- UCSD Undergraduate Council Member 2016-2018

- Involved in 10 UCSD Centers: Center for Contextual Robotics, Center for Wearable Sensors, Center for Energy Research, Center for Networked Systems, Center for Wireless and Population Health Systems, Sustainable Power and Energy Center, San Diego Supercomputing Center, Qualcomm Institute
- University Diversity in Precision Medicine Faculty Recruitments for Sensors, Devices, and Imaging Committee, 2015-16
- Eastern Europe Outreach 2015-2016
- School of Engineering Building Committee 2015-2016
- MS comprehensive exam planning committee 2015
- MS project review 2015, 2016
- CSE PhD admission committee 2014-2016
- MAS AESE Program Review 2014-2015
- Graduate students' committee 2012-2014
- Executive board member of San Diego Supercomputing Center 2008-pres.
- University energy initiatives committee, 2012-2013
- JSOE energy faculty search committee, 2012-2013
- Graduate students committee (gradcom) 2012-2013
- Member of the search committee for SDSC director 2009-pres.
- Engineering Wide Initiatives Committee, 2008-09
- Faculty Advisor, Women in Computing, 2005 – pres.
- Calit2 System-on-a-Chip Committee, Chair, 2005 – 06
- Faculty Recruiting Committee, 2005 – 06
- Computer Engineering Program Committee, 2005 – 08
- Masters Students Admissions and Affairs Committee, 2005 – 09
- Computer Engineering Space Committee, Chair, 2005 – 09

TEACHING EXPERIENCE

Fall 05 – pres.

UCSD – Full professor

- Taught an undergraduate class in logic circuit design (CSE 140); 95% of students said they recommend me as an instructor; 2005-pres.
- Designed, got funding and set up a new graduate level class and lab in embedded systems (CSE237a); 98% of students said they recommend me as instructor for the class; 2005-pres.
- Developed a graduate course on SmartGrid that attracted students, researchers and faculty across CSE, ECE, mechanical engineering, nano engineering and structural engineering departments, 2015.
- Designed and taught a course on Internet of Things, 2016.
- Designed and taught courses on Emerging Computing, and SW for Acceleration, 2018.
- Designed and taught an embedded systems class that is a part of Master of Advanced Studies program in Wireless and Embedded Systems at UCSD
- Taught a course on Hardware acceleration for bioinformatics workloads, 2019
- Designed and taught a course on Hypedimensional computing, 2022.

Winter 02

STANFORD UNIVERSITY – lecturer

- taught a graduate course on Logic Synthesis of VLSI Circuits; lead a team of TAs and graders

HONORS & AWARDS

- **SIA-SRC University Researcher Award 2022**, the first woman in history to receive one. This award recognizes lifetime research contributions to the U.S. semiconductor industry.
- **ACM Fellow**, 2022
- **Intel's 2021 Outstanding Researcher Award**, received in 2022
- **IEEE Fellow**, 2018
- Awarded John J. and Susan M. **Fratamico Endowed Chair** in CSE Department, 2014.
- Keynote at IEEE International High-Level Design Validation and Test, "Reliability and Maintainability of IoT systems," 2017.
- UCSD Sustainability Award for the Postdoc in my group, 2016.
- FISP Award 2015.
- UCSD Research Expo Best poster awards, 2010, 2012 (two honorable mention), 2013 (two honorable mention).
- Von Liebig Entrepreneurism Center Innovation Award in Information Technology for "SOPRA – A Proactive Service Oriented Self-Adaptive Framework for Data Center Resource Optimization," 2013
- CitiSense project covered in the NY Times and the Wall Street Journal, December 2012
- TODAES journal paper is the top most downloaded paper in 2010-2011
- Publication selected for inclusion in in *The Most Influential Papers of 10 Years DATE*, Edited by Lauwereins, Rudy; Madsen, Jan, 2008.
- Nominated as one of MIT's top 100 researchers in 2002
- NSF Design and Manufacturing Grantee and SRC Research Assistantship 1993
- Lowell's Award for the Best Student in Science at the Northern Arizona University 1992
- NASA Undergraduate Research Fellowship 1991

SELECT FUNDING (as PI, Co-PI, senior contributor, student support)

1. DARPA & SRC JUMP 2.0 PRISM center, \$56.5M, 2023-2028, PI and Center Director; 23 total PIs
2. DARPA & SRC JUMP 2.0 Cognitive computing center, \$40M, 2023-2028. Sole PI at UCSD, 20 PIs
3. DARPA DPRIVE subcontract, \$12.3M, 2022-2023
4. NSF MLWiNS, \$775k, 2020-2023
5. NSF Lifelong learning with HD Computing, \$800k, 2023-2028
6. Qualcomm HDnn gift, \$75k, 2021
7. NSF AI TILOS Institute, \$20M, 2021-2026
8. NSF Center for Power Management, \$375k to UCSD, 2021-2023
9. NSF CCRI: ENS: CHASE-CI, \$1.8M, 2021-24
10. NSF CCRI: ABR: Cognitive Hardware and Software Ecosystem Community Infrastructure, \$1M, 2021-23
11. NSF Prototype National Research Platform, \$6M, 2021-26
12. NSF CC*NPEO REU, \$16k, 2021-22
13. NSF REU NRI, \$14k, 2021-22
14. NSF FET HD REU, \$16k, 2021-22
15. NSF MLWiNS REU, \$16k, 2021-22
16. NSF CNS Nautilus, \$1.8M, 2021-2024
17. SRC HD, \$240k, 2020-2022
18. SRC HDnn, \$270k, 2020-2022
19. SRC FHE-PIM, \$255k, 2020-2022
20. TSMC HD chip, \$300k, 2020-2022
21. NSF RAPID Accelerating COVID-19 Analysis in HW, \$200k, 2020-2021
22. NSF REU, \$16k, 2020-2021
23. MICS Center funds, \$17k, 2020
24. Qualcomm gift for HD computing, \$150k, 2020 & 2021
25. NSF RAID COVID-19 acceleration, \$300k
26. DARPA HyDREA, HD computing, \$1M, 2020-2021
27. GRC HD computing \$240k, 2019-2022
28. NSF FET HD computing \$500k, 2019-2023

29. Russel-Sage Foundation \$175k, 2018-2020
30. Kavli Institute for Brain and Mind Innovative, \$50k, 2019-2020
31. NSF CC-NPEO, \$2.5M, 2018-2021
32. NSF NRI \$2.5M, 2018-2020
33. DARPA/SRC JUMP CRISP \$40M, 2018-2023
34. KACST IoT, \$2.9M, 2017-2019
35. GRC IoT Reliability, \$240k, 2018-2021
36. IBM-UCSD AIHL, \$16.3M, 2017-2022
37. NSF CPS CHASE-CI, \$1M, 2017-2020
38. Samsung IoT, \$300k, 2018
39. Huawei, \$100k, 2018
40. Intel, \$300k, 2016-2018.
41. ARPA-E NODES \$2.5M, 2016-2018.
42. NSF CSR \$450k
43. NSF MetaSense \$1.126M
44. Qualcomm FMA, Energy management of residences in the grid, \$75k, 2014-2015.
45. CEC EISG, Energy management in data centers, \$95k, 2013-2014.
46. NSF CSR, Energy efficient data centers, \$300k, 2013-2016.
47. FCRP center "TerraSwarm," \$27.5M, 2013-2017
48. NSF SCH: EXP SenseHealth, \$618k, 2013-2016
49. NSF MRI visualization \$2M, 2013-2016
50. Oracle gift, \$62k, 2012
51. Google gift, \$57k, 2012 CSE
52. NSF MRI optical networking \$1.06M, 2012-2014
53. NSF OCI:Sensor-Rocks, \$274k, 2012-2014.
54. NSF CCF, \$450k, 2012-2015.
55. Futurewei gift, \$117k, 2012.
56. Panasonic gift, \$100k, 2012.
57. Qualcomm FMA, \$75k, 2012-2014.
58. SRC, \$150k, 2011-2014.
59. Qualcomm membership, \$150k, 2011.
60. Oracle gift, \$100k, 2011. CNS
61. Google gift, \$75k, 2011. CNS
62. Google, \$125k, 2010. CSE
63. Qualcomm gift, \$35k, 2010.
64. Microsoft gift, \$300k, 2010
65. NSF-ERC CIAN, \$14M total, 2010-2019
66. NSF-Expedition on Variability, \$4.02M, 2010-2015
67. NSF OCI INRC: TransLight/StarLight, \$2.05M, 2010-2014
68. Qualcomm gift, \$75k, 2010-2011
69. CNS, \$75k, 2010.
70. NSF-CPS, \$1.5M, 2009-2013
71. Sun Microsystems Gift, \$120k, 2009
72. Google, \$50k, 2009.
73. Qualcomm Gift, \$15k, 2009
74. NIH PALMS, \$3.2M, 2007-2011
75. MARCO-MuSyC center, \$3M, 2009-2012
76. NSF CCF ARRA, \$476k, 2009-2013
77. NSF GreenLight, \$20M, 2008-2012
78. NSF FlashGordon, \$22M, 2011-2015
79. Cisco Gift, \$80k, 2008-2009
80. MARCO-GSRC Grant, \$154k, 2008-2009
81. CNS Grant for thermal management, \$142k, 2008-2010

82. CNS Grant for healthcare, \$116k, 2008-2010
83. Xilinx gift of 20 XUP DVKs
84. UC Micro Grant, \$30k, 2008-2010
85. Sun Microsystems Gift, \$100k, 2008-2009
86. NSF-CCF \$600k, sensing, 2007-2011
87. Sun Microsystems Gift, \$60k, 2007
88. CNS Grant, \$130k, 2006-2008
89. NSF – HPWREN, \$3M, 2005-2009.
90. LANL Structural Health Monitoring, \$7M, 2005-2009.
91. UC Micro, \$30k, 2006.
92. Sun Microsystems Gift, \$50k, 2005.
93. CNS Grant, \$60k, 2005.
94. Intel Grant, \$200k, 2005.
95. UC Graduate and Travel Grant \$11k, 2005
96. HP Labs - \$100k, 2003-2004

INVITED TALKS

1. Keynote at iTherm, 2022
2. Intel Research, OR, “Lifelong learning with HD computing,” 2022
3. Invited talk at DATE’22 special session on “Interpretable AI and Nanoelectronics-Based Designs of edge computing systems in the IoT 2.0 Era.” Title: “Hyperdimensional computing and applications,” 2022
4. Invited talk at ISCA-CogArch on “Accelerating fully homomorphic encryption in memory,” 2022
5. Micron Inc. executive leadership committee invited speaker 2022
6. SRC executive committee invited speaker 2022
7. Intel internal workshop, CA, “HD computing and applications,” 2021
8. Micron, CA, “CRISP: Bioinformatics grand challenge,” 2021
9. Terradata, CA, “Big data acceleration,” 2021
10. Merck, Germany, “Brain-inspired computing using high dimensionality,” 2021
11. Raytheon, DC, “Accelerating big data processing in hardware,” 2021
12. Xilinx, CA, “Accelerating COVID-19 analysis with FPGAs,” 2021
13. Keynote at Annual Symposium of Academy of Neuroscience & Architecture on Quantified Buildings, Quantified Self, (joint with Cognitive Sciences faculty from UCSD) 2021
14. Keynote at IGCC, 2021
15. Keynote at IEEE Sensors, 2021
16. Invited plenary speaker at the Future Chips Forum, Tsinghua University, 2021.
17. Invited to participate in National AI Research Resource Task Force, 2021.
18. DARPA Electronics Resurgence Initiative - Invited speaker & invited demo, 2020, 2021
19. Raytheon, DC, “Accelerating Fully Homomorphic Encryption with Processing in Memory” 2021.
20. Google, CA, “Accelerating big data analysis with in and near memory computing,” 2021.
21. Intel Research, OR, “Symbolic reasoning with HD computing,” 2021
22. Facebook, CA, “Brain-inspired HD computing,” 2021
23. IBM Research, NY, “Acceleration of big data workloads using in memory and in storage computing,” 2021
24. Samsung, NV at CES, “Hyperdimensional computing,” 2020.
25. MEC/DARPA Invited talk at “Analog Feature Extraction; Rethinking Analog Front-End to Accelerate Digital Inference,” Title: “Hyperdimensional computing and its acceleration,” 2020.
26. Micron, CA, “Accelerating bioinformatics workloads,” 2020.
27. IBM, NY, “Accelerating machine learning & HD computing,” 2020.
28. Qualcomm, CA, “Accelerating machine learning & HD computing,” 2020.
29. Northrop-Grumman, CA, “Accelerating machine learning & HD computing,” 2020.
30. Merck, Germany, “Accelerating workloads using in memory computing,” 2020.
31. Merck, Germany, “Acceleration of COVID-19 pipeline,” 2020.
32. Intel Research, CA, “Acceleration of COVID-19 pipeline,” 2020.
33. Leidos, CA, “HD Computing and its acceleration,” 2020.

34. ARM Inc, England, "HD computing," 2020.
35. Intel Research, OR, "Accelerating big data in storage," 2020.
36. EMD, CA, "Accelerating big data in HW," 2020.
37. NXP, CA, "HD computing," 2020.
38. DARPA ERI, DC, invited talk, "Accelerating big data in memory and storage," 2020.
39. LLNL, CA, "Accelerating bioinformatics workloads," 2020
40. Xilinx Inc, CA, "Accelerating bioinformatics workloads on FPGAs," 2020
41. Intel Research, OR, "Computational storage," 2020
42. UCSD TV, "Research Opportunities and Partnerships in the Tech Industry: Industry Panelists Share insights at the CSE Winter 2020 Research Open House," 2020.
43. VLSI-SOC invited keynote, "Acceleration of big data workloads," 2020.
44. Intel Research, OR, "Hyperdimensional computing," 2020
45. University of Wisconsin, WI, distinguished speaker "Accelerating big data workloads," 2020
46. Invited talk at NSF NDA Panel on AI/ML/Brain-inspired hardware design, 2020
47. Sony, CA, "Accelerating machine learning & HD computing using PIM," 2019.
48. ARM, CA, "Power, performance, thermal & reliability modeling and management in IoT systems," 2019.
49. Intel, OR, "Power, performance, thermal & reliability modeling and management in IoT systems," 2019.
50. EPFL, Switzerland, "Context-aware learning and acceleration," 2019.
51. Yahoo, CA, "Context-aware learning and acceleration," 2019.
52. Workshop on Brain-Inspired Architectures, NV, "Hyperdimensional Computing & Applications," 2019.
53. Non-volatile Memory Workshop, "Hyperdimensional Computing and Its Applications," 2019.
54. Altera, CA, "Accelerating Bioinformatics Workloads," 2019.
55. IBM Research, CA, "Accelerating machine learning & HD computing using PIM," 2019.
56. Huawei, CA, "Thermal management in mobiles," 2018.
57. Samsung, CA, "Context-aware management in Smart Homes," 2018.
58. IBM Research in Austin, TX, "Context-awareness for healthy aging," 2018.
59. Xconomy, CA, "Big data meets big biology: Accelerating learning for healthy living," 2018.
60. Huawei, China, "Proactive power and thermal management strategies," 2018.
61. Samsung, CA, "Smart Homes: context-aware management," 2018.
62. Intel Research, OR, "Reliability Management for IoT Systems," 2018.
63. DARPA Electronic Resurgence Initiative, CA, "JUMP CRISP Center Overview," 2018.
64. Micron, CA, "Accelerating machine learning workloads using PIM," 2018.
65. JUMP C-BRIC Center, USA, "Accelerating machine learning & HD computing using PIM," 2018.
66. JUMP ADA Center, USA, "Accelerating machine learning & HD computing using PIM," 2018.
67. TSMC, Taiwan, "Accelerating machine learning & HD computing using PIM," 2018.
68. GM, USA, "Context-aware management for IoT systems," 2018.
69. China government delegation, CA, "Context-aware learning and acceleration," 2018.
70. NSF CSR Workshop, WA, "Accelerating learning using PIM," 2018.
71. HLTV Keynote, "Reliability and Maintainability of IoT systems," 2017.
72. IBM, Austin, TX, "Context-aware IoT Systems," 2017.
73. Sony, Japan, "Context-aware IoT Systems" & "UCSD-IBM AI for Healthy Living Center", 2017.
74. D-Link, Japan, "UCSD-IBM AI for Healthy Living Center", 2017.
75. A-Star, Singapore, "UCSD-IBM AI for Healthy Living Center", 2017.
76. NRF, Singapore, "UCSD-IBM AI for Healthy Living Center", 2017.
77. NUS, Singapore, "UCSD-IBM AI for Healthy Living Center", 2017.
78. IBM, Kawasaki, Japan, "Context-aware IoT Systems, their Acceleration & Management," 2017.
79. Sony, Tokyo, Japan, "Context-aware IoT Systems, their Acceleration & Management," 2017.
80. IEEE/ACM Workshop on Variability Modeling and Characterization, Irvine, CA, "Increasing computational efficiency with novel computing paradigm," <http://www.cerc.utexas.edu/utda/vmc/>, 2017.
81. University of Melbourne, Australia, "Context-aware management for Smart Cities," 2016.
82. San Diego Port Authority, CA, "Context-aware management for Smart Cities," 2016.
83. CalTrans, CA, "Context-aware management for Smart Cities," 2016.
84. Cymer, CA, "System Energy Efficiency," 2016.

85. Hitachi, CA, "System Energy Efficiency," 2016.
86. Hewlett-Packard, CA, "System Energy Efficiency for IoT Applications," 2016.
87. IBM, CA, "Context-awareness for healthcare applications," 2016.
88. SDGE, CA, "Sensors to Grid," 2016.
89. Leidos, CA, "Improving Energy Efficiency in Smart Cities by Leveraging Context Awareness," 2016.
90. LG, CA, "System Energy Efficiency," 2016.
91. MediaTek, CA, "Context and the IoT," 2016.
92. Qualcomm, CA, "Approximate computing for IoT," 2016.
93. Raytheon, CA, "Improving system energy efficiency by leveraging context awareness," 2016.
94. UC Berkeley, "Hierarchical and context-aware management for the Smart Cities," 2015.
95. Arizona State University, AZ, "Context-aware energy and thermal management in systems," 2015.
96. University of Arizona, AZ, "Context-aware energy and thermal management in mobile systems," 2015.
97. SNU-UCSD-SDG&E MicroGrid (MG) Workshop, CA, "Leveraging Context for the Smart Cities," 2016.
98. Texas Instruments, TX, "Context-aware energy and thermal management," 2015.
99. Carnegie Mellon University, PA, "Distributed Control of Buildings Connected to a Smart Grid," 2015.
100. Fujitsu, CA, "Energy efficient datacenters and networks," 2015.
101. Intel, OR, "Distributed optimization for Smart Grid applications," 2015.
102. Intel, OR, "Approximate computing for Internet of Things applications," 2015.
103. University of Split, Croatia, "From sensors to smart cities," 2015.
104. Google, CA, "Context-aware energy management for residential applications," 2015.
105. Intel, OR, "Context and the IoT," 2015.
106. Intel, AZ, "Leveraging context-awareness for improving system energy efficiency," 2015.
107. Raytheon, Washington DC, "Ontology-Driven Context-Aware IoT Applications," 2015.
108. Intel, CA, "System Energy Efficiency," 2015.
109. Samsung, CA, "System energy efficiency," 2014.
110. IBM, NY, "Improving system energy efficiency by leveraging context awareness," 2014.
111. EPFL, Switzerland, "Context for distributed system energy efficiency," 2014.
112. Politecnico di Torino, Italy, "Context-aware energy and thermal management in mobile systems," 2014.
113. Politecnico di Milano, Italy, "Context-aware energy and thermal management in mobile systems," 2014.
114. EPFL, Switzerland, "Future Smart Environments," 2014.
115. University of Zagreb, Croatia, "Context-aware energy and thermal management in systems," 2014.
116. University of Split, Croatia, "Context-aware energy management for the Smart Grid applications," 2014.
117. Huawei, CA, "Datacenter energy efficiency," 2014.
118. Samsung, CA, "Context-aware energy and thermal management in mobile systems," 2014.
119. University of Maryland, "Context-aware energy and thermal management in mobile systems," 2014.
120. Raytheon, Washington DC, "Distributed energy management for the grid applications," 2013.
121. Intel, OR, "Distributed sensing and control for the smart grid applications," 2013.
122. Qualcomm, CA, "Modeling context in residences," 2013.
123. Qualcomm, CA, "Reliability management," 2013.
124. Intel, OR, "Energy and thermal management in mobile systems," 2013.
125. Panasonic, CA, "Using distributed batteries for energy management in residences," 2013.
126. Texas Instruments, TX, "SmartGrid and distributed batteries," 2013.
127. Google, CA, "Using batteries for peak power shaving," 2013.
128. University of Zagreb, Croatia, "Environmental sensor networks," 2013.
129. University of Split, Croatia, "Sensor networks in large scale systems," 2013.
130. Cisco, CA, "SmartGrid and sensing," 2013.
131. Intel, CA, "Mobile system energy and thermal management," 2013.
132. Qualcomm, CA, "Thermal and power management in mobile phones," 2013.
133. Raytheon, CA, "Energy management in systems," 2012.
134. Google, CA, "Peak power shaving in datacenters," 2012.
135. Fujitsu, CA, "Energy and thermal management," 2012.
136. SRCE, Croatia, "Energy management in datacenters," 2012.
137. Broadcom, CA, "Thermal management," 2012.

138. University of Maryland, MD, "Energy and thermal management," 2012.
139. Gatech, GA, "Energy and thermal management," 2012.
140. Panasonic, CA, "Energy management with batteries," 2012.
141. Flowmetrics, CA, "Cooling management in systems," 2012.
142. Qualcomm, CA, "Thermal and energy management in SoCs," 2012.
143. Oracle, CA, "Influence of fan vibrations on energy efficiency," 2012.
144. University of Arizona, AZ, "Energy management in large scale systems," 2012.
145. Arizona State University, AZ, "Energy and thermal management," 2012.
146. University of Chicago, IL, "Energy management in datacenters," 2012.
147. UIUC, IL, "Energy and thermal management," 2012.
148. Intel, CA, "Overview of energy and thermal management strategies," 2012.
149. Futurewei, TX, "Technology exchange about power-gating research," 2012.
150. Qualcomm, CA, "Power-gating and thermal management," 2012.
151. University of Zagreb, Croatia, "Energy and thermal management at the system level," 2012.
152. University of Split, Croatia, "Optimizing for energy in sensor networks," 2012.
153. Samsung, CA, "Energy and thermal management in mobile systems," 2012.
154. Texas Instruments, TX, "Sensor networks and energy management," 2012.
155. San Diego Gas and Electric, CA, "Energy management in large scale systems using batteries," 2012.
156. Synopsys, CA, "Thermal estimation in SoCs," 2012.
157. Oracle, CA, "Thermal management in servers," 2011.
158. Intel, CA, "Energy management in mobile systems," 2011.
159. IBM Labs, CA, "Optimizing system design for energy efficiency," 2011.
160. Texas Instruments, TX, "Thermal management in heterogeneous SoCs," 2011.
161. GLIF, Brasil, "Energy management in datacenters," 2011.
162. CICC panel on datacenters, CA, "Energy management in datacenters," 2011.
163. AMD, CA, "Energy and thermal management in systems," 2011.
164. Oracle, CA, "Thermal and cooling management in systems," 2011.
165. TU Dortmund, Germany, "Energy and thermal management in systems," 2011.
166. Cisco, CA, "Ultra-fast power gating," 2011.
167. Supercomputing, WA, "Using Green Energy Prediction for Energy Management in Large Scale Distributed Data Center Networks," 2011.
168. Qualcomm, CA, "Ultra-fast power gating," 2011.
169. BAE systems, CA, "System energy management," 2011.
170. Intel, OR, "Efficiency losses in mobile systems," 2011.
171. Ericsson, CA, "Thermal management at system level," 2011.
172. Qualcomm, CA, "Thermal management in heterogeneous 3D MPSOCs," 2011
173. LBNL, CA, "Energy efficient computing and networking in datacenters," 2011
174. EPFL, Switzerland, "Managing environmental variability in 2 & 3D designs," 2011.
175. Cisco, CA, "Energy efficient computing in datacenters," 2011
176. Microsoft Cloud Futures, WA, "Energy efficient computing in datacenters," 2011
177. Huawei, CA, "Energy efficient computing in datacenters," 2011
178. Ericsson, CA, "Energy efficient computing in datacenters," 2011
179. Intel, OR "Energy efficient computing in large scale systems," 2011
180. Qualcomm, "Energy and thermal management in 2 and 3D ICs", 2010.
181. Texas Instruments, "Energy and thermal management in heterogeneous multicore processors," 2010.
182. WirelessHealth 2010, "Population-aware wireless healthcare networks," 2010.
183. Microsoft Cloud Computing, "Achieving Energy Efficient Computing for Future Large Scale Applications," 2010.
184. ASU, AZ, "Energy and Thermal Management," 2010
185. SRCE, Croatia, "Energy efficient computing in datacenters," 2010.
186. UC Berkeley, CA, "Energy efficient computing," 2010.
187. Raytheon, CA, "Energy efficient computing in large scale systems," 2010
188. Microsoft, WA, "Energy efficient computing in the face of heterogeneous workloads" 2010
189. UW, WA, "CitiSense: Heterogeneous wireless sensing for healthcare applications," 2010

190. UCSB keynote, CA, "Energy efficient computing," 2010
191. Yahoo, CA, "Energy efficient computing," 2010
192. Oracle CA, "Energy efficient computing within virtualization systems," 2010
193. GE, CA, "Energy efficient computing in datacenters," 2010
194. EDF, CA, "Energy efficient computing in datacenters," 2010
195. PG&E, CA, "Energy efficient computing in datacenters," 2010
196. NSF, DC, "Population-Area Wireless Networks," NSF Workshop on Future Directions in Sensing Systems, 2009.
197. UIUC, IL, "Energy efficient computing," 2009.
198. UIC, IL, "Energy efficient computing," 2009.
199. UC Irvine, CA, "Energy efficient computing," 2009.
200. Princeton University, NJ, "Energy efficient computing," 2009.
201. Penn State University, PA, "Energy efficient computing," 2009.
202. CMU, PA, "Energy efficient computing," 2009.
203. La Jolla Research & Innovation Summit, Venture Capital panel: "Energy Efficient Systems," 2009.
204. Ericson, "Energy efficient computing," 2009.
205. IBM Research, Austin, TX, "Energy efficient computing," 2009.
206. IBM Research, TJ Watson, NY, "Energy efficient computing," 2009.
207. Lockheed Martin, San Diego, "Energy efficient computing," 2009.
208. InterDigital, "Energy efficient computing," 2009.
209. SK Telecom, "Heterogeneous wireless sensor networks," 2009.
210. On Ramp Wireless, "Heterogeneous wireless sensor networks," 2009.
211. Northrop Grumman, San Diego, "Energy efficient computing," 2009.
212. Panasonic, "Energy efficient computing," 2009.
213. Qualcomm, San Diego, "Power and thermal management in 2D and 3D multicore processors," 2009.
214. Qualcomm, VC group, "Heterogeneous wireless sensor networks," 2009.
215. Qualcomm, San Diego, "Wireless healthcare," 2009.
216. Google, Mountain View, "Energy efficient computing," 2009.
217. Google, Mountain View, "Power management in operating systems and energy efficient software," 2009.
218. Sun Microsystems, San Diego, "Energy efficient computing," 2009.
219. Sun Microsystems, Menlo Park, "Power and thermal management in multicore processors," 2009.
220. Cisco, "Energy efficient computing," 2009.
221. Cisco, "Energy management in virtualized systems," 2009.
222. Cisco, "Wireless healthcare," 2009.
223. Yahoo, "Energy efficient computing," 2009.
224. TI, "Energy efficient computing," 2009.
225. Intel, Santa Clara, "Power management in multicore processors," 2009.
226. Intel, Hillsborough, "Energy management using virtualization," 2009.
227. FER, Zagreb, Croatia, "Energy efficient computing," 2009.
228. USC, CA, "Energy efficient computing," 2009.
229. UCLA, CA, "Energy efficient computing," 2009.
230. SPAWAR, San Diego, "Energy efficient computing," 2009.
231. Workshop on mapping applications to MPSoCs, "Energy and thermal management in MPSoCs," 2009.
232. UC Berkeley, "Energy management in computing systems," 2008.
233. EPFL, Switzerland, "Resource management in heterogeneous wireless sensor networks," 2008.
234. EPFL, Switzerland, "Thermally-aware OS scheduling for MPSoCs," 2008.
235. Intel – Hillsborough, OR, "Dynamic power management in wireless systems," 2008.
236. Microsoft Research, WA, "Resource Management of Heterogeneous Wireless Embedded Systems", 2006.
237. Intel – Folsom, CA, "Resource Management of Heterogeneous Wireless Embedded Systems", 2006.
238. Sun Microsystems – Mountain View, CA, "Managing SOC power and reliability with in-situ telemetry", 2006.
239. HP Labs – Palo Alto, CA, "Resource Management of Heterogeneous Wireless Embedded Systems", 2006.
240. ARM - Irvine, CA, "Modeling power and reliability of SOCs," 2006.
241. Tensilica – Santa Clara, CA, "Modeling power and reliability of SOCs," 2006.
242. Mindspeed – Irvine, CA, "Modeling power and reliability of SOCs," 2006.

243. Sun Microsystems, CA, "Resource Management of Heterogeneous Wireless Embedded Systems", 2006.
244. Ericsson – San Diego, CA: "Heterogeneous sensor networks," 2006.
245. Intel – Santa Clara, CA: "Reliable and low power SOC design", 2005.
246. ST Micro – San Diego, CA: "Reliable and low power SOC design," 2005.
247. Intel – Portland, CA: "Resource Management of Heterogeneous Wireless Embedded Systems", 2005.
248. Freescale – Phoenix, AZ, "Reliable and low power SOC design", 2005.
249. Qualcomm – San Diego, CA, "Analysis of SOC power management," 2005.
250. Sun Microsystems – San Diego, CA: "Reliable and low power SOC design", 2005.
251. DATE'05, Germany, Special Session Invited paper: "Power management in wireless environments," 2005.
252. EPFL – Lausanne, Switzerland, "Reliable and low power SOC design", 2005.
253. IMEC – Belgium, "Resource Management of Heterogeneous Wireless Embedded Systems", 2005.
254. HP Techcon – Orlando, FL, "Managing resources of HotSpot servers," 2004.
255. University of Washington – Seattle, WA, "Resource management in embedded systems," 2003.
256. USC – Los Angeles, CA: "Resource management in embedded systems," 2003.
257. UC Berkeley – Berkeley, CA, "Energy efficient system design and utilization," 2002.
258. MIT – Cambridge, MA, "Energy efficient system design and utilization," 2002.
259. Stanford University – Stanford, CA, "Resource management in embedded systems," 2002.
260. University of Washington - Seattle, WA, "Energy efficient system design and utilization," 2001.
261. Gatech – Atlanta, GA, "Energy efficient system design and utilization," 2001.
262. UCI – Irvine, CA, "System-level power management," 2001.
263. IBM TJ Watson - Yorktown Heights, NY, "Energy efficient system design and utilization," 2001.
264. Lucent Labs - Murray Hill, NJ, "Energy efficient system design and utilization," 2001.
265. HP Labs – Palo Alto, CA, "Energy efficient system design and utilization," 2001.