

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Hoberman et al.
U.S. Patent No.: 7,051,306 Attorney Docket No.: 60246-0006IP1
Issue Date: May 23, 2006
Appl. Serial No.: 10/840,893
Filing Date: May 7, 2004
Title: MANAGING POWER ON INTEGRATED CIRCUITS
 USING POWER ISLANDS

Mail Stop Patent Board

Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,051,306 PURSUANT TO 35 U.S.C. §§311–319, 37 C.F.R. §42**

TABLE OF CONTENTS

I.	REQUIREMENTS FOR IPR	1
A.	Grounds for Standing	1
B.	Challenge and Relief Requested	1
II.	THE '306 PATENT	3
A.	Brief Description	3
B.	Summary of the Prosecution History	4
C.	Level of Ordinary Skill in the Art	4
D.	Claim Construction.....	4
III.	THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	5
A.	GROUND 1A—Claims 1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51 are obvious over Nowka	5
1.	Overview of Nowka.....	5
2.	Claim 1	8
3.	Claim 2	18
4.	Claim 3	19
5.	Claim 4	20
6.	Claim 5	20
7.	Claim 6	21
8.	Claim 7	21
9.	Claim 8	21
10.	Claim 10	22
11.	Claim 11	22
12.	Claim 12	23
13.	Claim 14	23
14.	Claim 15	24
15.	Claim 16	24
16.	Claim 17	26
17.	Claim 18	26

18.	Claim 19	27
19.	Claim 20	27
20.	Claim 21	27
21.	Claim 22	27
22.	Claim 23	27
23.	Claim 25	27
24.	Claim 26	27
25.	Claim 27	27
26.	Claim 29	27
27.	Claim 30	27
28.	Claim 31	28
29.	Claim 32	30
30.	Claim 33	30
31.	Claim 34	31
32.	Claim 36	32
33.	Claim 37	32
34.	Claim 38	34
35.	Claim 39	34
36.	Claim 40	34
37.	Claim 41	34
38.	Claim 42	34
39.	Claim 43	35
40.	Claim 44	35
41.	Claim 46	35
42.	Claim 47	35
43.	Claim 48	35
44.	Claim 50	35
45.	Claim 51	35
B.	GROUND 1B—Claims 9, 13, 24, 28, 45, and 49 are obvious over Nowka and Borkar	35
1.	Overview of Borkar	35

2.	Nowka-Borkar Combination.....	37
3.	Claim 9.....	39
4.	Claim 13.....	41
5.	Claim 24.....	44
6.	Claim 28.....	44
7.	Claim 45.....	44
8.	Claim 49.....	45
C.	GROUND 1C—Claim 35 is obvious over Nowka and Boerstler.....	45
1.	Overview of Boerstler.....	45
2.	Nowka-Boerstler Combination.....	46
3.	Claim 35.....	46
D.	GROUND 1D—Claims 1-12, 14-23, 25-27, 29-34, 36-48, 50-51 are obvious over Nowka and Bertin.....	47
1.	Overview of Bertin.....	48
2.	Nowka-Bertin Combination.....	49
3.	Claim 1.....	51
4.	Claim 9.....	53
5.	Claim 16.....	54
6.	Claim 24.....	54
7.	Claim 37.....	54
8.	Claim 45.....	55
E.	GROUND 2A—Claims 1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, 47 are obvious over Nicol.....	55
1.	Overview of Nicol.....	55
2.	Claim 1.....	57
3.	Claim 2.....	64
4.	Claim 3.....	66
5.	Claim 4.....	67
6.	Claim 5.....	68
7.	Claim 7.....	68
8.	Claim 8.....	69

9.	Claim 9.....	69
10.	Claim 11	69
11.	Claim 16.....	70
12.	Claim 17	70
13.	Claim 18.....	70
14.	Claim 19.....	71
15.	Claim 20.....	71
16.	Claim 22.....	71
17.	Claim 23	71
18.	Claim 24.....	71
19.	Claim 26.....	71
20.	Claim 31	71
21.	Claim 32.....	72
22.	Claim 33	72
23.	Claim 36.....	72
24.	Claim 37.....	74
25.	Claim 38.....	74
26.	Claim 39.....	74
27.	Claim 40.....	75
28.	Claim 41	75
29.	Claim 42.....	75
30.	Claim 43.....	75
31.	Claim 44.....	75
32.	Claim 45.....	75
33.	Claim 47	75
F.	GROUND 2B—Claims 6, 10, 12, 14-15, 21, 25, 27, 29-30, 34, 46, 48, 50-51 are obvious over Nicol and Nowka.....	75
1.	Nicol-Nowka Combination.....	75
2.	Claim 6.....	77
3.	Claim 10.....	77
4.	Claim 12.....	78

5.	Claim 14	79
6.	Claim 15	80
7.	Claim 21	80
8.	Claim 25	80
9.	Claim 27	81
10.	Claim 29	81
11.	Claim 30	81
12.	Claim 34	81
13.	Claim 46	82
14.	Claim 48	82
15.	Claim 50	82
16.	Claim 51	82
G.	GROUND 2C—Claims 13, 28, and 49 are obvious over Nicol and Borkar	82
1.	Nicol-Borkar Combination	82
2.	Claim 13	84
3.	Claim 28	87
4.	Claim 49	87
H.	GROUND 2D—Claim 35 is obvious over Nicol and Naffziger	87
1.	Overview of Naffziger	87
2.	Nicol-Naffziger Combination	88
3.	Claim 35	90
IV.	PAYMENT OF FEES	91
V.	MANDATORY NOTICES UNDER 37 C.F.R. §42.8(a)(1).....	91
A.	Real Party-In-Interest Under 37 C.F.R. §42.8(b)(1).....	91
B.	Related Matters Under 37 C.F.R. §42.8(b)(2)	91
C.	Lead And Back-Up Counsel Under 37 C.F.R. §42.8(b)(3)	92
D.	Service Information	93

LIST OF EXHIBITS

EX1001	U.S. Patent No. 7,051,306 to Hoberman et al. (“the ’306 patent”)
EX1002	Excerpts from the Prosecution History of the ’306 patent
EX1003	Declaration of Tajana Rosing, Ph.D.
EX1004	“A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling” by Nowka, et al. (“Nowka”)
EX1005	Declaration of June Ann Munford
EX1006	U.S. Patent No. 6,484,265 to Borkar et al. (“Borkar”)
EX1007	U.S. Patent No. 6,353,369 to Boerstler (“Boerstler”)
EX1008	U.S. Patent No. 6,141,762 to Nicol, et al. (“Nicol”)
EX1009	RESERVED
EX1010	RESERVED
EX1011	Claim Construction Order in <i>MOSAID Technologies Inc. v. Freescale Semiconductor, Inc.</i> , Case No. 6:11-cv-00173 (E.D. Tex. April 29, 2013)
EX1012	Claim Construction Order in <i>Conversant Intellectual Property Management Inc., et al. v. Xilinx, Inc.</i> , Case No. 6:12-cv-00847 (E.D. Tex. January 9, 2015)
EX1013	Claim Construction Order in <i>MOSAID Technologies Inc. v. MediaTek</i> , Case No. 2:23-cv-00129 (E.D. Tex. July 31, 2024)
EX1014	RESERVED
EX1015	U.S. Patent No. 8,086,884 to Naffziger et al. (“Naffziger”)

- EX1016 “Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design” by Kuroda et al. (“Kuroda”)
- EX1017 “Dynamic Power Management: Design Techniques and CAD Tools” by Benini & De Micheli (“Dynamic Power Management”)
- EX1018 “A Survey of Design Techniques for System-Level Dynamic Power Management” by Benini, et al. (“Benini Survey”)
- EX1019 “Managing Power and Performance for System-on-Chip Designs using Voltage Islands” by Lackey, et al. (“Lackey”)
- EX1020 “Policy Optimization for Dynamic Power Management” by Benini et al., (“Benini Policy Optimization”)
- EX1021 “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling” by Semeraro et al. (“Semeraro”)
- EX1022 “Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems” by Dutta et al. (“Dutta”)
- EX1023 “The CoreConnect™ Bus Architecture” by IBM (“CoreConnect White Paper”)
- EX1024 “The Computer Engineering Handbook” edited by Oklobdzija (“Computer Engineering Handbook”), excerpts
- EX1025 “Computer Systems: Concepts and Design” by Gibson (“Gibson”), excerpts
- EX1026 Multimedia Information Networking” by Sharda (“Sharda”), excerpts
- EX1027 U.S. Patent No. 6,345,362 to Bertin et al. (“Bertin”)
- EX1028 “PowerPC 603 Microprocessor: Power Management” by Suessmith (“Suessmith”)

- EX1029 IEEE Journal of Solid-State Circuits, IEEE Xplore,
<https://ieeexplore.ieee.org/xpl/aboutJournal.jsp?punumber=4>
(accessed June 16, 2025)
- EX1030 Excerpts from Document Landing Page for “A 32-bit PowerPC
system-on-a-chip with support for dynamic voltage scaling and
dynamic frequency scaling,” IEEE Xplore,
<https://ieeexplore.ieee.org/document/1046086/citations#citations>,
<https://ieeexplore.ieee.org/document/1046086/citations?tabFilter=patents#citations> (accessed June 16, 2025)
- EX1031 IEEE History, <https://www.ieee.org/about/ieee-history> (accessed
June 16, 2025)
- EX1032 IPR2024-00598, Paper 12, Institution Decision (Sep. 26, 2024)

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:
1[a]	determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands;
1[b]	determining at least one of actions to change a power consumption level of the one of the power islands to the target power level; and
1[c]	performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.
Claim 2	
2	The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit
Claim 3	
3	The method of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 4	
4	The method of claim 1 wherein the power islands comprise power sub-islands.
Claim 5	
5	The method of claim 1 wherein the power islands comprises multiple clock domains.
Claim 6	
6	The method of claim 1 wherein another one of the actions comprises selecting a clock for the one of the power islands.
Claim 7	
7	The method of claim 1 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

Claim 8	
8	The method of claim 7 wherein the first voltage comprises a source voltage.
Claim 9	
9	The method of claim 7 wherein the first voltage comprises a threshold voltage.
Claim 10	
10	The method of claim 1 wherein another one of the actions comprises powering on the one of the power islands.
Claim 11	
11	The method of claim 1 wherein another one of the actions comprises powering off the one of the power islands.
Claim 12	
12	The method of claim 1 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 13	
13	The method of claim 1 further comprising: monitoring the power consumption level of the one of the power islands; determining whether a threshold level was crossed based on the power consumption level; and performing another one of the actions based on the crossing of the threshold level.
Claim 14	
14	The method of claim 1 further comprising saving a state of components within the one of the power islands.
Claim 15	
15	The method of claim 1 further comprising restoring a state of components within the one of the power islands.

Claim 16	
16[p]	A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:
16[a]	power control circuitry configured to control power for one of the power islands; and
16[b]	a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.
Claim 17	
17	The system of claim 16 wherein the power islands are delineated based on geographic factors of the integrated circuit.
Claim 18	
18	The system of claim 16 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 19	
19	The system of claim 16 wherein the power islands comprise power sub-islands.
Claim 20	
20	The system of claim 16 wherein the power islands comprise multiple clock domains.
Claim 21	
21	The system of claim 16 wherein another one of the actions comprises selecting a clock for the one of the power islands.
Claim 22	
22	The system of claim 16 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

Claim 23	
23	The system of claim 22 wherein the first voltage comprises a source voltage.
Claim 24	
24	The system of claim 22 wherein the first voltage comprises a threshold voltage.
Claim 25	
25	The system of claim 16 wherein another one of the actions comprises powering on the one of the power islands.
Claim 26	
26	The system of claim 16 wherein another one of the actions comprises powering off the one of the power islands.
Claim 27	
27	The system of claim 16 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 28	
28	The system of claim 16 wherein the power manager is configured to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.
Claim 29	
29	The system of claim 16 wherein the power manager is configured to save a state of components within the one of the power islands.
Claim 30	
30	The system of claim 16 wherein the power manager is configured to restore a state of components within the one of the power islands.
Claim 31	
31	The system of claim 16 further comprising a bus coupled to the power manager and the power islands.

Claim 32	
32	The system of claim 16 wherein the power manager comprises a master manager configured to control power of the integrated circuit.
Claim 33	
33	The system of claim 16 wherein the power manager comprises a slave manager configured to control power of the one of the power islands.
Claim 34	
34	The system of claim 16 wherein the power control circuitry includes clock multiplexing circuitry.
Claim 35	
35	The system of claim 16 wherein the power control circuitry includes voltage multiplexing circuitry.
Claim 36	
36	The system of claim 16 wherein the power control circuitry includes level shifting circuitry.
Claim 37	
37[p]	A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising:
37[a]	power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands; and
37[b]	a software storage medium operational to store the power management software.

Claim 38	
38	The software product of claim 37 wherein the power islands are delineated based on geographic factors of the integrated circuit.
Claim 39	
39	The software product of claim 37 wherein the power islands are delineated based on functional circuitry of the integrated circuit.
Claim 40	
40	The software product of claim 37 wherein the power islands comprise power sub-islands.
Claim 41	
41	The software product of claim 37 wherein the power islands comprise multiple clock domains.
Claim 42	
42	The software product of claim 37 wherein another one of the actions comprises selecting a clock for the one of the power islands.
Claim 43	
43	The software product of claim 37 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.
Claim 44	
44	The software product of claim 43 wherein the first voltage comprises a source voltage.
Claim 45	
45	The software product of claim 43 wherein the first voltage comprises a threshold voltage.
Claim 46	
46	The software product of claim 37 wherein another one of the actions comprises powering on the one of the power islands.
Claim 47	
47	The software product of claim 37 wherein another one of the actions comprises powering off the one of the power islands.

Claim 48	
48	The software product of claim 37 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.
Claim 49	
49	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.
Claim 50	
50	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within the one of the power islands.
Claim 51	
51	The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within the one of the power islands.

CONVENTIONS OF THE PETITION

- All emphases are added unless noted otherwise;
- Bold-italic emphases correlate to claim language;
- Quotations are generally from exhibits, not claim language; and
- The phrase “as discussed” and equivalent phrases incorporate fully the analysis of the cross-cited portion of the Petition.

Petitioner Infineon Technologies Americas Corp. petitions for IPR of Claims 1-51 of U.S. Patent No. 7,051,306.

The Board previously granted institution in a prior IPR challenging the '306 patent (Case No. IPR2024-00598). Patent Owner asked the Board to terminate the instituted IPR due to a settlement with the prior petitioner, and less than three months after the Board did so, Patent Owner took aim at a different target and asserted the '306 patent against Infineon. This Petition reasserts Grounds 1A-1C and 2A-2D from the prior IPR and asks the Board to again institute review of the '306 patent, a repeatedly asserted patent that the Board has already deemed likely unpatentable.

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the '306 patent is available for IPR, and that Petitioner is not barred or estopped from requesting this review.

B. Challenge and Relief Requested

Petitioner requests IPR and cancellation of the '306 patent's Challenged Claims based on the grounds below. Petitioner submits that the cited prior art references are themselves sufficient to establish obviousness pursuant to the analysis in Section III. The Section III analysis further cites to the Declaration of Dr. Tajana Rosing for complementary corroboration and explanation. *See generally* EX1003.

Ground	Claims	Basis	References
1A	1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51	§103	Nowka
1B	9, 13, 24, 28, 45, 49	§103	Nowka and Borkar
1C	35	§103	Nowka and Boerstler
1D	1-12, 14-23, 25-27, 29-34, 36-48, 50-51	§103	Nowka and Bertin
2A	1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, 47	§103	Nicol
2B	6, 10, 12, 14-15, 21, 25, 27, 29-30, 34, 46, 48, 50-51	§103	Nicol and Nowka
2C	13, 28, 49	§103	Nicol and Borkar
2D	35	§103	Nicol and Naffziger

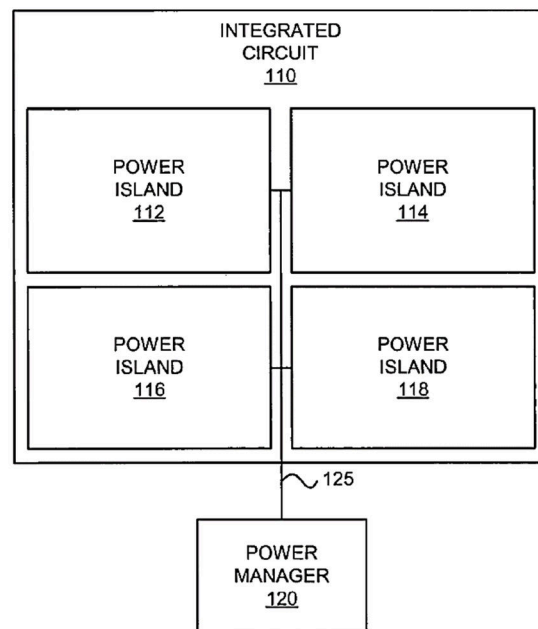
Each of these references pre-dates the '306 patent's earliest claimed priority date of May 7, 2003. Petitioner, however, does not concede that the Challenged Claims are entitled to the benefit of this priority claim.

Reference	Date	Prior Art Under
Nowka	11/2002 (published)	§102(a)
Nicol	10/31/2000 (published)	§102(b)
Bertin	02/05/2002 (published)	§102(b)
Borkar	11/19/2002 (published)	§102(a)
Boerstler	03/05/2002 (published)	§102(b)
Naffziger	12/16/2002 (filed)	§102(e)

II. THE '306 PATENT

A. Brief Description

At the time of the '306 patent, as integrated circuits were becoming increasingly more complex, reducing power consumption was a well-known design goal. EX1001, 1:19-26, 2:1-9. However, according to the '306 patent, “power consumption [was still] not efficiently utilized.” EX1001, 1:58-59. As a proposed solution, the '306 patent describes power islands whose power consumption is independently controlled. EX1001, Abstract, 2:21-24; EX1003, ¶¶34-40. For example, Figure 1 depicts a system having a “power manager” that determines a target power level for one of the power islands and then determines an action—e.g., selecting a clock frequency or modifying a voltage—to change the consumption for that island to the target power level. EX1001, Abstract, 2:24-38, 4:45-55, 5:34-36.



EX1001, Fig. 1.

B. Summary of the Prosecution History

The '306 patent was filed as U.S. Application 10/840,893 on May 7, 2004 with a priority claim identifying Provisional Application 60/468,742 (May 7, 2003). EX1002, 174. The Patent Office issued one non-final rejection and one final rejection during prosecution. EX1002, 127-135 (Feb. 24, 2005 Non-Final Rejection), 73-83 (Aug. 3, 2005 Final Rejection). The Office never considered the Nowka, Bertin, Nicol, Borkar, Naffziger, or Boerstler references that render the Challenged Claims obvious in Grounds 1A-2D below.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") would have had at least a bachelor of science degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. EX1003, ¶¶20, ¶¶24-33.

D. Claim Construction

Claim terms generally should be given their ordinary and customary meaning according to the *Phillips* standard. Petitioner submits that no claim terms require a formal construction for purposes of addressing the grounds in this Petition. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). That

said, Petitioner notes that there have been prior litigations involving the '306 patent, three of which had a claim construction order before voluntary dismissal. *See* EX1011, EX1012, EX1013. Petitioner submits that the Board does not need to address any of the prior constructions to resolve the parties' present patentability dispute here at the PTAB, and that none of the prior constructions moot the obviousness grounds in this Petition.

III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A—Claims 1-8, 10-12, 14-23, 25-27, 29-34, 36-44, 46-48, 50-51 are obvious over Nowka

1. Overview of Nowka

Nowka is a technical paper published in the November 2002 edition of the IEEE Journal of Solid-State Circuits (Volume 37, Issue 11), a journal that “publishes papers each month in the broad area of solid-state circuits with particular emphasis on transistor-level design of integrated circuits.” EX1004, 1441; EX1029. IEEE lists Nowka’s “Date of Publication” as “30 November 2002.” EX1030, p.1. IEEE was established in 1963 and is one of the world’s largest technical professional associations. EX1031. IEEE has been a prolific and exceedingly well-known publisher for decades. *Id.* Cataloging dates extracted from library MARC records further corroborate the November 2002 public availability of Nowka (EX1005, 4-5), as does the 2002 copyright date on its face (EX1004, 1441) and the many other technical papers and patents that cite to Nowka (EX1030).

Nowka describes a system-on-a-chip (“SOC”) capable of dynamic voltage and frequency scaling “to adapt to [] dynamically changing performance demands and power consumption constraints.” EX1004, Abstract; EX1003, ¶¶44-47. Nowka’s SOC features a high performance 32-bit processor core, also referred to as the “CPU core,” an integrated LCD display controller, I/O interfaces, a dedicated speech accelerator, an instruction decompression engine, a DES accelerator core, a phase-locked-loop (PLL) core, a real-time-clock core, a clock power-management core, and a sleep-management core. EX1004, 1442. Some of these components are shown in the structural diagram in Figure 1 and the die photograph in Figure 2.

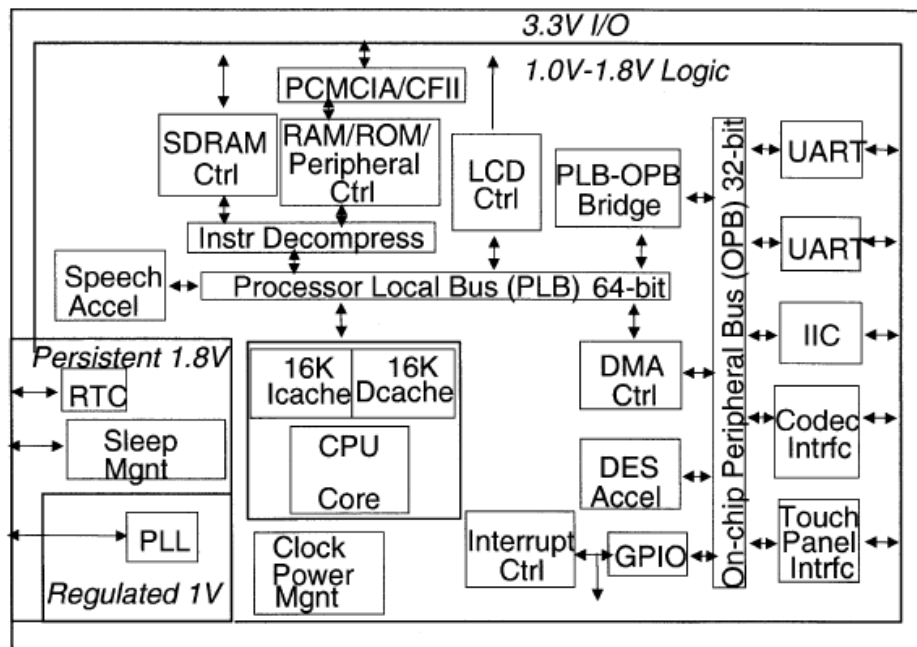
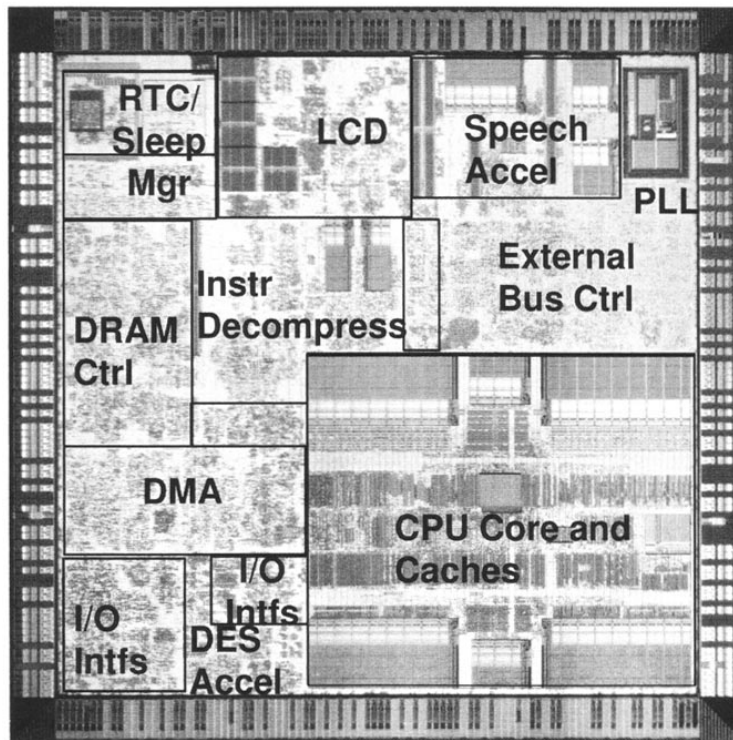


Fig. 1. PowerPC SOC structure.

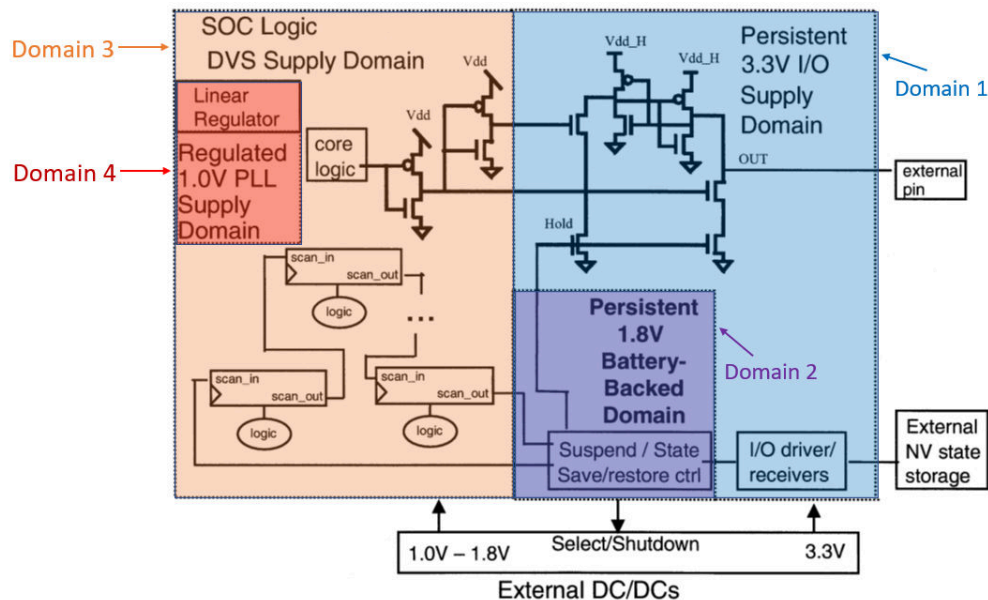
EX1004, Fig. 1.



EX1004, Fig. 2.

Nowka's SOC is divided into four power domains to enable dynamic voltage and frequency scaling. These domains—two persistent voltage domains, one dynamically voltage-scaled and frequency-scaled logic domain, and one internally derived domain—are shown in annotated Figure 3 below. The I/O drivers and receivers are in the persistent 3.3V domain (domain 1 below); the real-time clock and the logic controlling the voltage of the cores is in the persistent 1.8V domain (domain 2 below); the logic supply for the processor core, caches, SOC cores and accelerators is in the 1-1.8V variable domain (domain 3 below); and the PLL is in the constant 1V domain (domain 4 below). EX1004, 1444. The operating frequency of the variable voltage domain (domain 3) can also be altered for additional active

power reduction. EX1004, 1444 (“When the performance demands of the application decrease, the system software can lower the operating frequency.”).



EX1004, Fig. 3

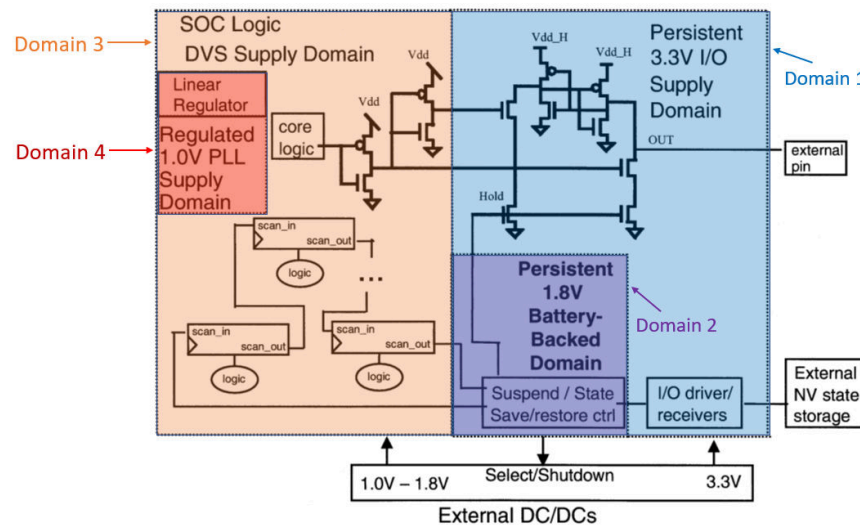
2. Claim 1

(a) Element_1[p]

To the extent the preamble is limiting, Nowka discloses and renders obvious *a method of managing power on an integrated circuit including a plurality of power islands*. EX1003, ¶¶48-51.

Nowka explains that its SOC design is “optimized for energy efficiency” by controlling voltage and frequency. EX1004, 1446. Nowka discloses multiple power domains on the integrated circuit, namely the four domains depicted in Figure 3 below, which are supplied different voltages. EX1004, 1444. A POSITA would

have understood and found obvious that the four domains are *power islands* as defined by the '306 patent because each domain is a “section, delineation, partition, or division” on the SOC where “power consumption is controlled within the section, delineation, partition, or division.” EX1001, 3:51-54; EX1003, ¶50.



EX1004, Fig. 3.

Additionally, as an independent basis for addressing Element_1[p], Nowka teaches that the variable voltage and variable frequency logic domain (*power island*) includes multiple “cores”—e.g., a “processor core,” a “dedicated speech accelerator, an instruction decompression engine and a DES accelerator core,” and an “LCD core,” (EX1004, 1442, 1444). A POSITA would have understood and found obvious that these “cores” are also capable of being controlled as *power islands* by varying

their voltage and frequency independent of the remainder of the SOC.¹ E.g., EX1004, 1445 (“modification of the clock frequency within the individual cores”) (“clocks to individual functional cores can also be frozen”); EX1003, ¶51.

(b) Element_1[a]

Nowka discloses and renders obvious *determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands*. EX1003, ¶¶52-65.

Nowka discloses that its SOC allows for “performance demands of the application to be met” (*needs and operation of the integrated circuit*) while “minimizing the dynamic power consumption” (*determining a target power level*). EX1004, 1446; EX1003, ¶53. In other words, like the ’306 patent, Nowka’s *target power level* corresponds to a “desired...power consumption,” (EX1001, 4:28-33)—the minimal power consumption necessary to satisfy the performance demands of

¹ Even if, as in the prior litigations (e.g., EX1023, 23), the term “power island” were construed more narrowly than the plain language and the above-recited definition in the ’306 patent, Nowka’s disclosure regarding the individual and independently controllable “cores” within the logic domain would still render the Challenged Claims obvious as discussed here and throughout Grounds 1A-1D.

the application, (EX1004, 1446). For example, with “applications [that] tend to have peak performance demands as high as 500 MIPS,” Nowka explains that “the power consumption of the processor core is best kept at or below about 500 mW.” EX1004, 1441. By contrast, Nowka says, “active power consumption [can also be adjusted] as low as 53 mW at a supply of 1.0 V.” *Id.*

TABLE II
CPU CORE WITH CACHES CHARACTERISTICS

	TC1 (1.8V)	TC2 (1.0V)
Maximum Frequency (estimate)	380 MHz	152 MHz
Power Consumption (estimate)	500 mW	53 mW
TC1 – Typical conditions: 1.8V, 55C, nominal silicon		
TC2 – Typical conditions: 1.0V, 55C, nominal silicon		

EX1004, Table II

Moreover, in Nowka, like the '306 patent, this minimal power consumption approach is **determined** by “software control.” EX1004, 1446; *see also* 1442 (“Under software control...”), 1444 (“the clock and power management software”), 1445 (“this allows the power consumption to be **determined** by the system on a very fine time scale”), *compare with* EX1001, 4:56:67 (describing power management firmware and software), 13:14-23 (discussing “software” instructions).

Nowka discloses multiple actions to reduce the power level “when resource demands are low” (***needs and operation of the integrated circuit***) such as “dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating,” and standby modes. EX1004, 1442, 1446; EX1003, ¶¶54-62. For example,

Nowka discusses the power consumption results of voltage scaling while running Dhrystone2.1 benchmark (Figure 5) and MPEG-4 decoding (Figure 6) on the SOC. EX1004, 1444. Both examples demonstrate that the **target power level** of a power island (target supply voltage of logic domain) is shifted in response to **needs and operation of the integrated circuit** (varying requirements of the application being run, or different requirements from different applications). EX1003, ¶55.

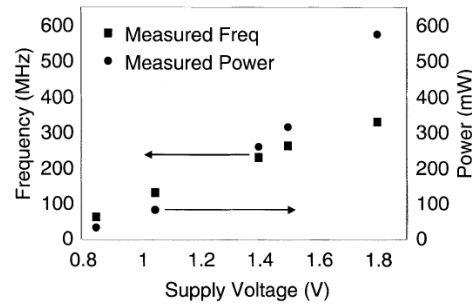


Fig. 5. Dhrystone2.1 voltage scaling measurements.

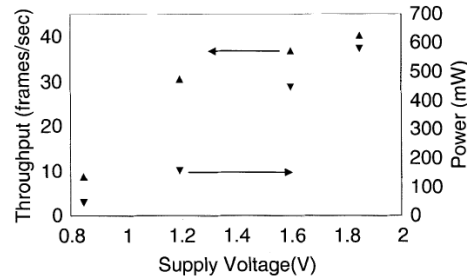


Fig. 6. MPEG-4 decode voltage scaling measurements.

EX1004, Figs. 5, 6.

Figure 8 shows the corresponding decrease and increase of power consumption in response to frequency and voltage changes, which a POSITA would have understood to be executed “in anticipation of [] performance demands” (**needs and operation of the integrated circuit**). EX1004, 1444, Fig. 8; EX1003, ¶56.

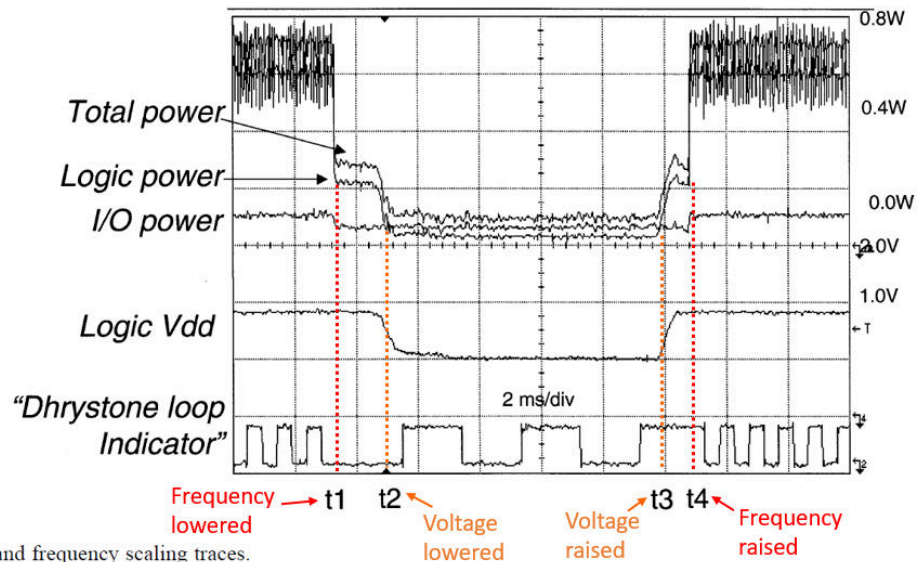


Fig. 8. Dynamic voltage and frequency scaling traces.

EX1004, Fig. 8.

As yet another example, Nowka discloses clock gating inactive registers and cores, as well as putting the system in various standby modes, which changes the power state of the logic domain, when certain registers and units, or the entire logic domain, does not need to be active. EX1004, 1445-46; EX1003, ¶¶60-61.

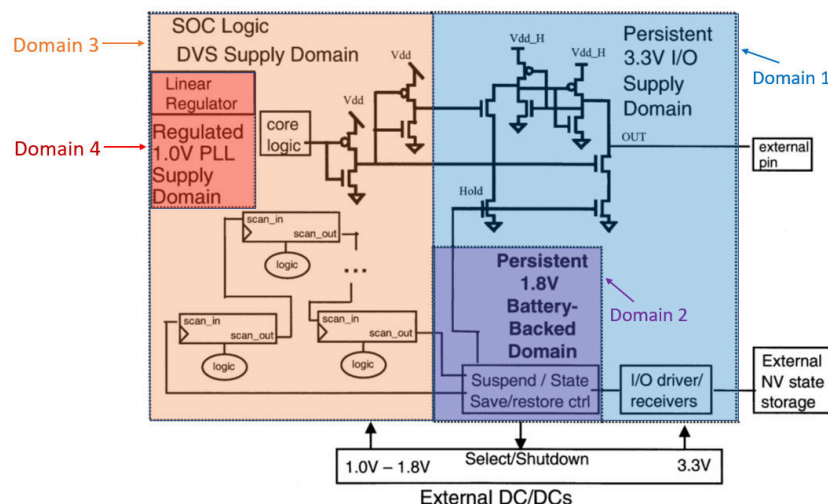
A POSITA would have found it obvious that each of these actions involves *determining a target power level*, not only for the reasons discussed above, but also because these actions were well-understood in the art as mechanisms for adjusting power levels. EX1003, ¶¶57, 62. Moreover, Nowka's above-discussed teachings on dynamic frequency and voltage scaling match the approach of the '306 patent, which describes a power manager setting the target for parameters such as frequency and voltage based on application performance demands. EX1001, 7:38-66, Fig. 5; EX1003, ¶¶58-59. To the extent Patent Owner contends Nowka does not expressly

disclose *determining a target power level based on needs and operation of the integrated circuit*, it would have been obvious to a POSITA nevertheless that the software in conjunction with the other aspects of Nowka's system makes such a determination. EX1003, ¶¶54-62.

Regarding the claim language of *based on needs and operation of the integrated circuit*, Petitioner notes that the parties in prior litigations involving the '306 patent agreed to a construction of "based on future operational needs and current operating status of the integrated circuit." EX1011, 48; EX1012, 9; EX1013, 26. For purposes of this Petition, Petitioner submits that there is no construction necessary because the plain and ordinary meaning suffices. EX1003, ¶63. The Board reached the same conclusion in Case No. IPR2024-00598 when instituting an *inter partes* review of the '306 patent in view of the same Nowka-based challenge presented here. *See* EX1032, 11-16 ("we...apply the plain and ordinary meaning"). The '306 patent does not provide further explanation of this phrase, nor a particular balancing of "needs" and "operation" that is required. Rather, it provides examples of determining parameters such as required frequency, supply voltage, or threshold voltage, given the demands of a particular application. EX1001, 7:38-50, 8:56-62 (discussing setting a "required frequency" for an IP unit in response to an application request). As discussed, Nowka's teachings match the approach of the '306 patent.

Petitioner further submits that Nowka's teachings render the Challenged Claims obvious, including Element_1[a], even under the construction that the Board previously rejected. For example, Nowka's discussion that the software changes frequency and voltage "[i]n anticipation of lower performance demands" shows that its power management is responsive to future operational needs, while Nowka's disclosure that the software, "anticipating an increase in demand, [raises] the logic supply...to 1.8 V without interrupting execution" shows that it is also responsive to the current operational status of the integrated circuit. EX1004, 1444; EX1003, ¶64.

Nowka further teaches that *power consumption is independently controlled within each of the power islands*. For example, Nowka's power domains (*power islands*) receive distinct voltage supplies, which can be controlled independently (e.g., the logic domain 3 can receive variable voltage supply while domains 1 and 2 receive a persistent voltage supply). EX1004, 1442; EX1003, ¶65.



EX1004, Fig. 3.

Additionally, as discussed at Element_1[p], Nowka teaches that the logic domain includes *power islands* in the form of multiple “cores,” (EX1004, 1442, 1444), which are capable of being controlled by varying their voltage and frequency independent of the remainder of the SOC. *E.g.*, EX1004, 1445; EX1003, ¶65.

(c) Element_1[b]

Nowka discloses and renders obvious *determining an action to change the power consumption level of one of the power islands to the target power level*. EX1003, ¶¶66-73.

As discussed at Element_1[a], Nowka discloses a number of actions such as changing frequency, changing voltage, clock gating, and standby modes, *to change the power consumption level* of the logic domain (*one of the power islands*) *to a target power level* that minimizes power consumption while meeting application performance demands. EX1003, ¶¶67-72. Nowka similarly provides capabilities for power management over the individual “cores” in this way. EX1003, ¶67; EX1004, 1445; *supra* Element_1[a].

It would have been clear and obvious to a POSITA that Nowka’s system *determines* which *action(s)* to perform under the circumstances to accomplish this power-minimizing objective. *E.g.*, EX1004, 1442 (“Under software control, the supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation.”), 1444 (“When the performance demands of the

application decrease, the system software can lower the operating frequency.”), 1446 (“The on-chip clock and power supervisor, in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to control the standby power.”); EX1003, ¶¶72-73 (Dr. Rosing explaining that “the POSITA would have appreciated that determining the appropriate power-reducing action to take is how Nowka’s system software ‘makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications,’ (EX1004, 1441).”).

(d) Element_1[c]

Nowka discloses and renders obvious *performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands*. EX1003, ¶¶74-75.

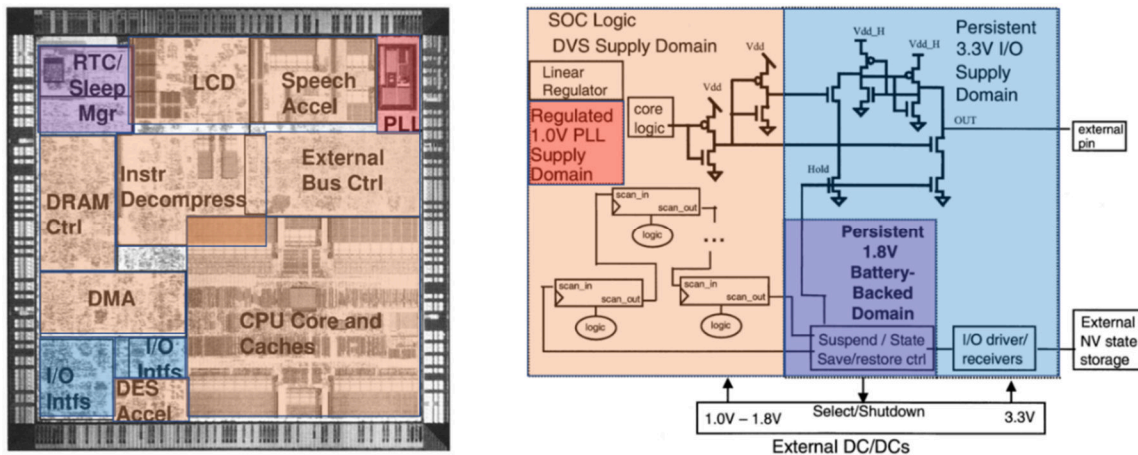
As discussed at Elements_1[a]-1[b], a POSITA would have appreciated that Nowka’s system software facilitates *performing actions* such as changing *frequency*, changing voltage, clock gating, or standby mode *to change the power consumption level* of the logic domain (*one of the power islands*) and its individual cores (also *power islands*) *to the target power level* that minimizes power consumption while meeting application performance demands. EX1004, 1444

(Section III.C) (voltage scaling), 1444 (Section V) (frequency and voltage scaling), 1445 (“Active power of the SOC can be further reduced through modification of the clock frequency within the individual cores.”) (clock gating), 1446 (standby modes); EX1003, ¶75. “Adjustment to the output clock frequency can be done on-the-fly by modifying the output clock divider through a write to a control register,” allowing “the frequency of the core [to] be varied from the maximum frequency down to 1/64th of the maximum.” EX1004, 1444. In other words, by writing to the control register, the software “set[s]” (*selects*) *a frequency*. EX1003, ¶75.

3. Claim 2

Nowka discloses and renders obvious Claim 2. Annotated Figures 2 and 3 below show that the components in Nowka’s four power domains (*power islands*) are located near other components in the same power domain.² EX1004, Figs. 2-3; EX1003, ¶¶76-77. Additionally, a POSITA would have understood and found it obvious from Nowka’s disclosure and basic circuit design principles that *power islands* would be delineated based on *geographic factors* (e.g., physical proximity) to minimize signal deterioration and power dissipation, for better routing of power supply and signals, and optimization of performance and power. EX1003, ¶78.

² This analysis applies equally to the four power domains (*power islands*) and the individual cores within the logic domain (*power islands*). *Supra* §III.A.2(a)-(b).



EX1004, Figs. 2, 3.

4. Claim 3

Nowka discloses and renders obvious Claim 3. As shown in the annotated Figure 2 below, Nowka's power domains (*power islands*) are defined by the *functional circuitry* of the constituent components. EX1003, ¶¶79-81. For example, the I/O drivers and receivers are in the persistent 3.3V supply domain because of their function, which is to interface between the SOC and external components. EX1004, 1442. Additionally, components that dynamically respond to program needs are grouped together in the variable-supply logic domain. EX1004, 1442. As for the individual cores within the logic domain (also *power islands*), their corresponding circuitry is delineated based on the function of the core. EX1003, ¶80. "The real-time clock and the logic associated with controlling the voltage of the cores" receives a persistent 1.8V supply because these functional circuits need to retain power even when other parts of the SOC are off. EX1004, 1442. The PLL, which generates the clock signal to control operation of the SOC,

receives an internally derived voltage supply to maintain a constant, well-regulated voltage. EX1004, 1442; EX1003, ¶81.

5. Claim 4

Nowka discloses and renders obvious Claim 4. Nowka discloses that “active power of the SOC can be further reduced through modification of the clock frequency within the individual cores.” EX1004, 1445. A POSITA would have understood and found obvious that the individual cores are independently controlled *power sub-islands*. EX1003, ¶¶82-83; *supra* Element 1[p]. Nowka also discloses that “[d]ynamic power is saved in this design by gating off inactive latches and units. Approximately 80% of the processor registers and 50% of the SOC core registers are functionally clock gated when they are not accessed.” EX1004, 1445. A POSITA would have understood and found obvious from this disclosure that the latches, registers, and units are also *power sub-islands*. EX1003, ¶84.

6. Claim 5

Nowka discloses and renders obvious Claim 5. For example, the individual cores (*power islands*, per Elements_1[p]-1[a], [4]) in the logic domain “receive clocks whose frequency is derived from the processor clock through clock dividers. The clock dividers are controlled by register values. The hazard-free clock dividers allow the clocks to the cores to be modified dynamically and individually.” EX1004,

1445. A POSITA would therefore have understood and found obvious that the individual cores (*power islands*) comprise *multiple clock domains*. EX1003, ¶85.

7. Claim 6

Nowka discloses and renders obvious Claim 6. Nowka discloses that a different *clock* can be selected “when the performance demands of the application decrease”—e.g., “[t]he output multiplexor can [] *select* the real-time *clock*, reference *clock*, or an auxiliary *clock* as the processor *clock* source to allow for extremely low frequency operation.” EX1004, 1444; EX1003, ¶86.

8. Claim 7

Nowka discloses and renders obvious Claim 7. The Nowka system employs “dynamic voltage scaling (DVS)” to match “the performance and power consumption of this device to the application...DVS systems adjust the supply voltage dynamically to meet the performance demands while minimizing power consumption.” EX1004, 1442; EX1003, ¶87. As discussed, the supply voltage for the logic domain (*power island*, per Elements_1[p]-1[a]) “can be varied [(*modified*)] between 1 and 1.8V.” EX1004, 1442; EX1003, ¶¶87-89.

9. Claim 8

Nowka discloses and renders obvious Claim 8. Nowka discloses that “[p]rocessor energy efficiency can be improved by scaling the supply voltage. DVS systems adjust the supply voltage dynamically to meet the performance demands

while minimizing power consumption.” EX1004, 1442. As would have been understood by a POSITA, the “supply voltage” is the **voltage** supplied to the SOC power domains via the DC/DC converters from a voltage **source**. EX1003, ¶¶90-91; EX1004, 1443; EX1001, 4:51-53.

10. Claim 10

Nowka discloses and renders obvious Claim 10. For example, Nowka discloses “Hibernation” and “Cryo” modes where “the logic supply to the processor, caches and the SOC core is disconnected.” EX1004, 1446; *see also* 1445 (“the clocks to individual functional cores can also be frozen”). When exiting Hibernation/Cryo mode and “reactivating the system” upon a “wakeup event,” the SOC “restores the [logic] supply” to **power on the power island(s)**. EX1004, 1446; EX1003, ¶92.

11. Claim 11

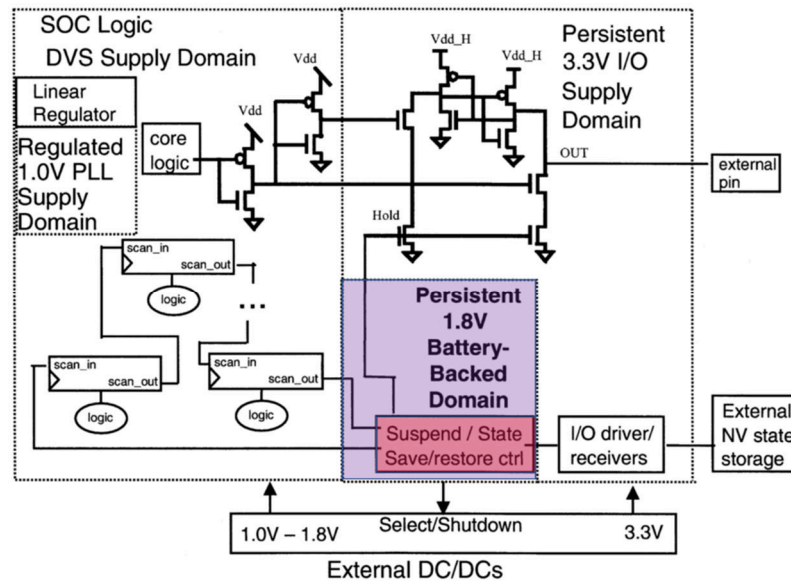
Nowka discloses and renders obvious Claim 11. For example, Nowka discloses “Hibernation mode” and “Cryo mode” where “the logic supply to the processor, caches and the SOC core is disconnected,” which **powers off the power island(s)**. EX1004, 1446; *see also* 1445 (“the clocks to individual functional cores can also be frozen”); EX1003, ¶93.

12. Claim 12

Nowka discloses and renders obvious Claim 12. For example, Nowka discloses “*sleep* and hibernation *modes*” to “minimize standby power consumption,” similar to the ’306 patent’s disclosure of “low power modes such as *sleep*, nap, and full power down.” EX1004, 1442, 1446; EX1001, 7:26-27; EX1003, ¶94. Specifically, Nowka describes Freeze, Hibernation, and Cryo modes, each of which comports with the ’306 patent’s *sleep mode*. In Freeze mode, “the system clock is stopped and the logic supply is decreased to its minimum value of 1.0 V.” EX1004, 1446. In Hibernation/Cryo modes, the logic supply voltage is disconnected to reduce standby power consumption. EX1004, 1446.

13. Claim 14

Nowka discloses and renders obvious Claim 14. For example, Nowka discloses that, in “Cryo mode,” “the state of latches and register arrays in the processor core and SOC cores is transferred to nonvolatile storage prior to disconnecting the logic supply.” EX1004, 1446. Therefore, Nowka discloses and renders obvious *saving the state* of the latches and register arrays, which are components in the logic domain. EX1003, ¶95. Figure 3 shows a block labeled “*Save/restore ctrl*” (highlighted in red) within the variable voltage power domain (*power island*), which a POSITA would have understood to facilitate *saving a state of components*. EX1003, ¶96.



EX1004, Fig. 3.

14. Claim 15

Nowka discloses and renders obvious Claim 15. According to Nowka, after entering “Cryo mode,” the suspend controller “waits for a wakeup event at which time it restores the supply, *restores the state* and restart the clocks” for components in the variable voltage power domain (*power island*). EX1004, 1446; EX1003, ¶97.

15. Claim 16

(a) Element_16[p]

Ground 1A, Element_1[p]-1[a]. Nowka further discloses and renders obvious a *system for an integrated circuit* in the form of a *system-on-a-chip* platform fabricated via a “bulk CMOS process,” a well-known technology for constructing *integrated circuits*. EX1004, 1441, 1446, Figs. 1-2; EX1003, ¶¶98-99.

(b) Element_16[a]

Ground 1A, Element_1[p]-1[a]. Nowka discloses and renders obvious **power control circuitry configured to control power for one of the power islands**. For example, Nowka explains that the DC/DC converter controls the supply voltage of the logic domain **power island(s)**, while the PLL controls the clock frequency of the **power island(s)**. EX1004, Abstract, 1442-1444, Figs. 1, 3, 7; EX1003, ¶100.

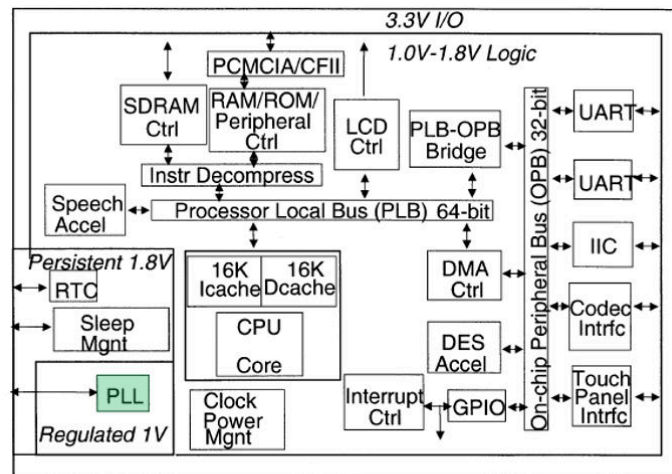
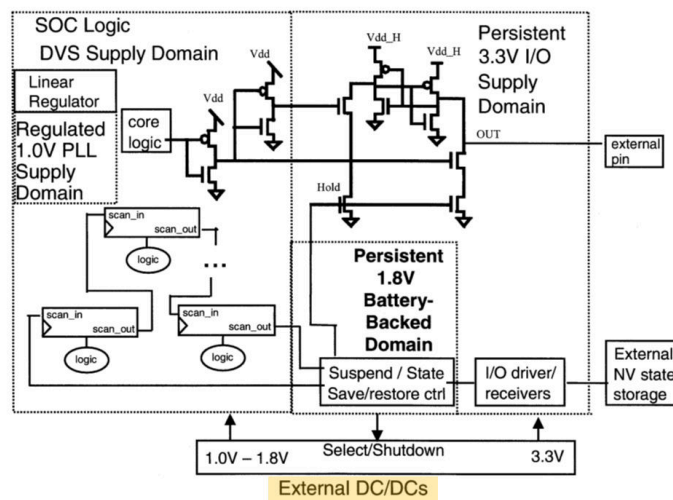


Fig. 1. PowerPC SOC structure.

EX1004, Fig. 1.



EX1004, Fig. 3.

(c) Element_16[b]

Ground 1A, Elements_1[a]-[c]. EX1003, ¶101. Nowka further discloses and renders obvious a *power manager* comprising, e.g., an “on-chip supervisor” and “system software.” EX1004, 1442, 1444 (“clock and *power management* software”); EX1003, ¶102. The “on-chip supervisor controls the external DC/DC converter, which provides the logic supply” and “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” EX1004, 1442. In addition, Nowka discloses that the power supervisor, “in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to control the standby power”; and during freeze mode, “the supervisor software first sets a low operating frequency and then lowers the supply.” EX1004, 1446; EX1003, ¶103. Nowka’s *power manager* also includes the PLL (to control the frequency) and the external DC/DC (to control the supply voltage), which work with the supervisor to execute frequency and voltage scaling, (EX1004, 1444), and clock dividers, which enable “unit and register level functional clock gating.” EX1004, 1445; EX1003, ¶104.

16. Claim 17

Ground 1A, Claim 2. EX1003, ¶105.

17. Claim 18

Ground 1A, Claim 3. EX1003, ¶106.

18. Claim 19

Ground 1A, Claim 4. EX1003, ¶107.

19. Claim 20

Ground 1A, Claim 5. EX1003, ¶108.

20. Claim 21

Ground 1A, Claim 6. EX1003, ¶109.

21. Claim 22

Ground 1A, Claim 7. EX1003, ¶110.

22. Claim 23

Ground 1A, Claim 8. EX1003, ¶111.

23. Claim 25

Ground 1A, Claim 10. EX1003, ¶112.

24. Claim 26

Ground 1A, Claim 11. EX1003, ¶113.

25. Claim 27

Ground 1A, Claim 12. EX1003, ¶114.

26. Claim 29

Ground 1A, Claim 14. EX1003, ¶115.

27. Claim 30

Ground 1A, Claim 15. EX1003, ¶116.

28. Claim 31

Nowka discloses and renders obvious Claim 31. As a POSITA would have known, busses were the dominant form of interconnect technology for transmitting signals to, from, and through integrated circuits at the time of the Critical Date. EX1003, ¶117. Using a known and ubiquitous technology like a bus to *couple* the known elements of Nowka's SOC would have been exceedingly obvious to a POSITA. *Id.* For example, Nowka's Figure 1 shows a "processor local *bus*" and an "on-chip peripheral *bus*" that connects various functional units within the logic domain (*power islands*, per Elements_1[p]-1[a], 16[p]-16[a]). EX1003, ¶118.

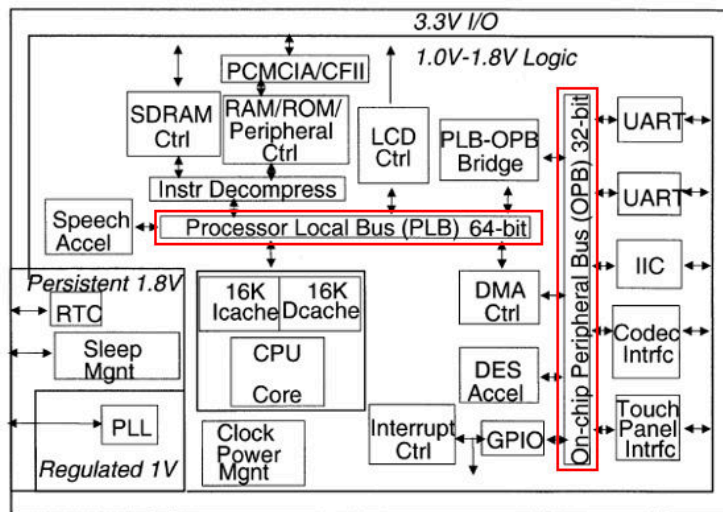


Fig. 1. PowerPC SOC structure.

EX1004, Fig. 1.

Moreover, a POSITA would have understood that the *power manager* in Nowka, which includes the on-chip power supervisor (*supra* Element_16[b]), would have been *coupled* to some form of parallel or serial *bus* to facilitate its functionality of

“respon[ding] to software commands and timeout and interrupt events” and “manag[ing] the clocks, internal state and external power supply,” (EX1004, 1446). EX1003, ¶117.

Nowka also discloses that “the SOC uses IBM’s Core-Connect [1] technology to integrate a rich set of memory and I/O devices.” EX1004, 1441. The “Core-Connect technology allows integration of semicustom synthesized cores and custom hard-cores in an SOC.” EX1004, 1445. As shown below, Figure 1 in the CoreConnect Bus Architecture White Paper shows various buses connecting the power manager (“Reset Clock Control Power Mgmt”) to the other SOC components. Accordingly, a POSITA would have understood that the Nowka provides *a bus coupled to the power manager and the power islands*. EX1003, ¶119.

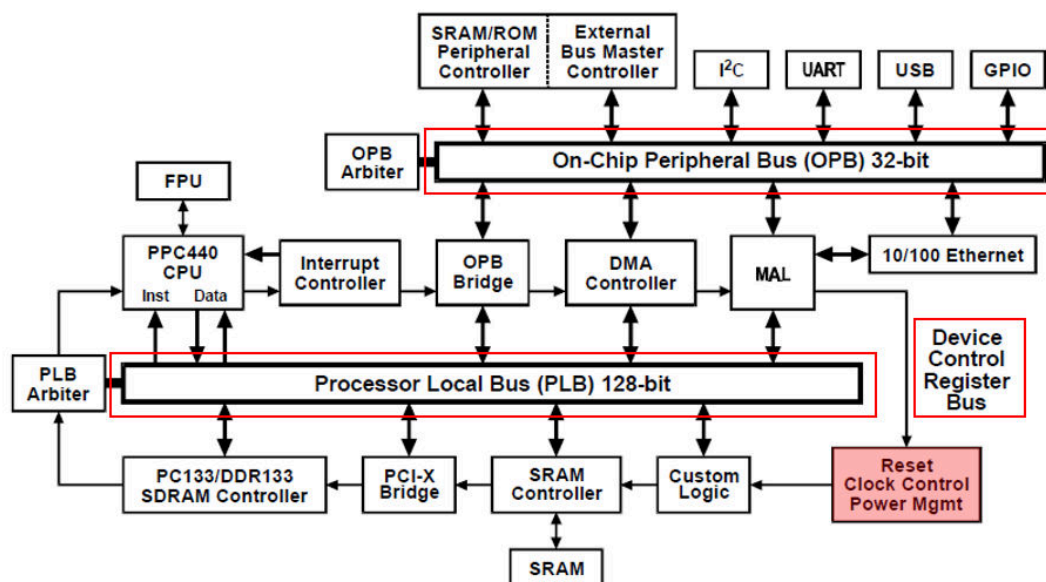


Figure 1: CoreConnect Based System-On-a-Chip.

EX1023, Fig. 1.

29. Claim 32

Nowka discloses and renders obvious Claim 32. As one example, Nowka discloses an “on-chip supervisor” that, among other things, “requests changes to the logic supply and requests shutdown of the logic supply during hibernation,” (EX1004, 1442), and “*manages* the clocks, internal state and external power supply to control the standby power,” (EX1004, 1446). EX1003, ¶¶120-121. A POSITA would have recognized the on-chip supervisor acts as a *master manager* because it oversees the global power behavior of the system. EX1001, 5:47-48; EX1003, ¶121. Similarly, the “system software” that controls the on-chip supervisor would have also been understood by the POSITA to act as a *master manager*. EX1003, ¶121; EX1004, 1442, 1444-46.

30. Claim 33

Nowka discloses and renders obvious Claim 33. First, the PLL (which controls the frequency) and the external DC/DC converters (which control the supply voltage) render obvious a *slave manager* because they control the power of the logic domain under the direction of the on-chip supervisor. EX1004, 1442, 1444, EX1003, ¶¶122-124. Second, Nowka discloses “clock dividers controlled by register values” that “allow the clocks to the cores to be modified dynamically and individually,” for example, in response to “a force condition by the clock and power manager.” EX1004, 1445. A POSITA would have understood and found obvious

that the clock dividers and the relevant registers provide additional *slave managers*. EX1003, ¶125. Third, to the extent the “system software” is deemed a master manager (*supra* Claim 32), the on-chip supervisor it controls would likewise be recognized by the POSITA as a relative *slave manager*.³ EX1003, ¶126.

31. Claim 34

Nowka discloses and renders obvious Claim 34. For example, Nowka discloses that the PLL (*power control circuitry*, per Element_16[a]) includes an “output *multiplexor*” that “allows for clock freezing for sleep and hibernation modes. The output *multiplexor* can also select the real-time *clock*, reference *clock*, or an auxiliary *clock*.” EX1004, 1444, Fig. 7; EX1003, ¶127.

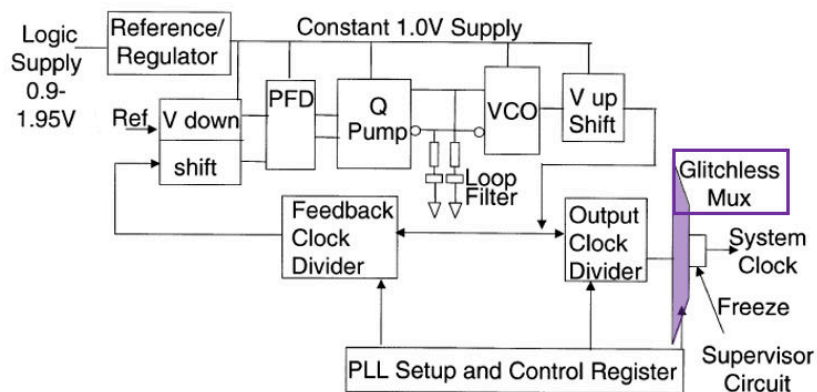


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

³ The '306 patent does not foreclose the possibility of a single component serving as both a master manager and a slave manager.

32. Claim 36

Nowka discloses and renders obvious Claim 36. Nowka discloses that “signals passing from the logic domain to the persistent domain are latched by *level shifters*.” EX1004, 1443; EX1003, ¶128. Further, “the PLL integrates *level shifting* into the reference clock, feedback clock and output clock paths.” EX1004, 1444; EX1003, ¶128.

33. Claim 37

(a) Element_37[p]

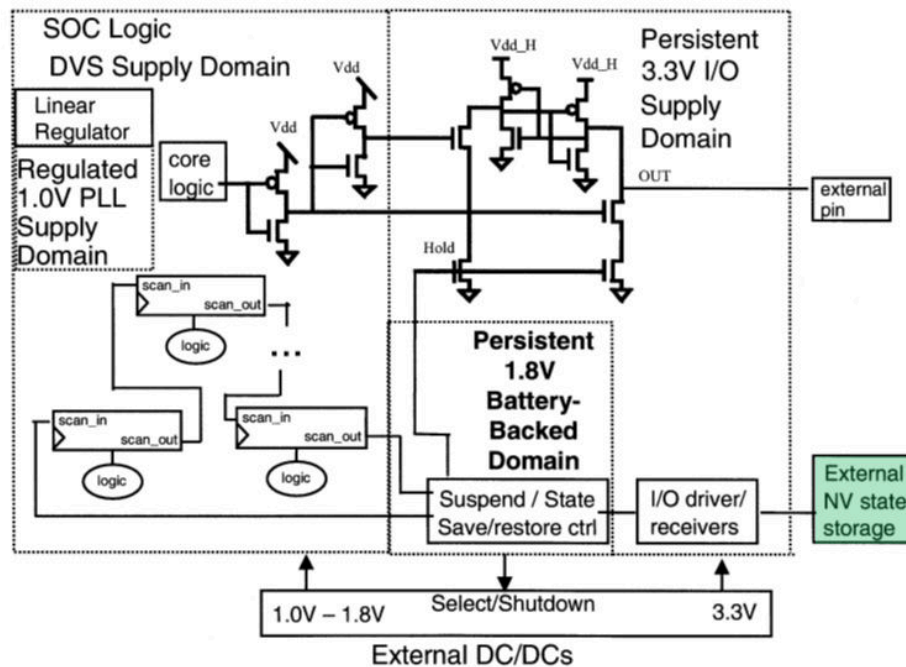
Ground 1A, Element_1[p]. Nowka also discloses and renders obvious *a software product* in the form of “system software” that requests changes to the logic supply and requests shutdown of the logic supply during hibernation,” (EX1004, 1442), “can lower the operating frequency,” (EX1004, 1444), exert “control over the PLL and external DC/DC,” (EX1004, 1444), modifies “both the voltage and the frequency of the processor...thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption,” (EX1004, 1446), and causes the processor to “enter both a low-leakage sleep state and a state-preserving deep-sleep state to minimize standby power consumption.” EX1004, 1446; EX1003, ¶129.

(b) Element_37[a]

Ground 1A, Elements_1[a]-[c], 37[p]. Nowka discloses and renders obvious *power management software* in the form of “system software” performing *power management* functions. EX1004, 1442, 1444, 1446; EX1003, ¶¶130-131.

(c) Element_37[b]

It would have been obvious to a POSITA that Nowka’s *power management software* (see Element_37[a]) would be stored in *a software storage medium*, such as an on-chip cache or an off-chip nonvolatile storage. EX1004, 1441-1443, 1446; EX1001, 4:58-59, Fig. 2; EX1003, ¶¶132-133.



EX1004 (Nowka), Fig. 3.

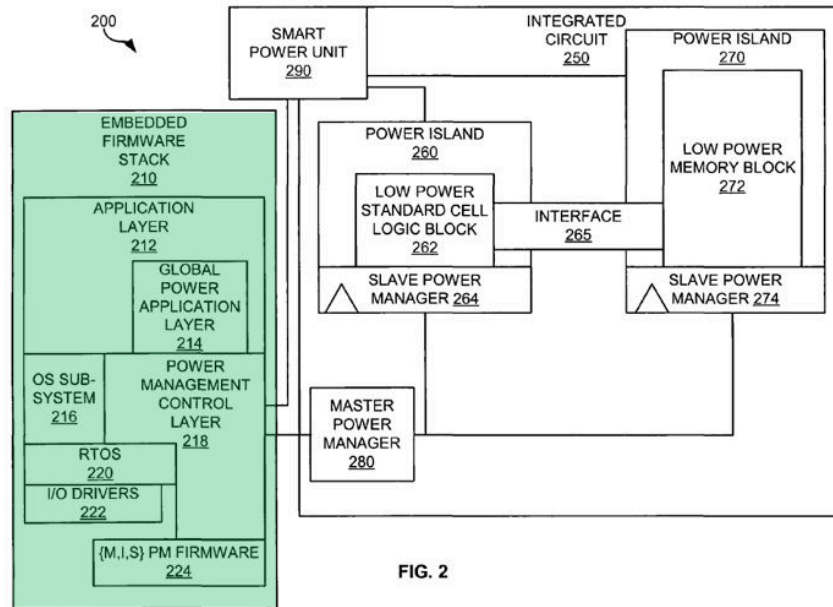


FIG. 2

EX1001 ('306 patent), Fig. 2.

34. Claim 38

Ground 1A, Claim 2. EX1003, ¶134.

35. Claim 39

Ground 1A, Claim 3. EX1003, ¶135.

36. Claim 40

Ground 1A, Claim 4. EX1003, ¶136.

37. Claim 41

Ground 1A, Claim 5. EX1003, ¶137.

38. Claim 42

Ground 1A, Claim 6. EX1003, ¶138.

39. Claim 43

Ground 1A, Claim 7. EX1003, ¶139.

40. Claim 44

Ground 1A, Claim 8. EX1003, ¶140.

41. Claim 46

Ground 1A, Claim 10. EX1003, ¶141.

42. Claim 47

Ground 1A, Claim 11. EX1003, ¶142.

43. Claim 48

Ground 1A, Claim 12. EX1003, ¶143.

44. Claim 50

Ground 1A, Claim 14. EX1003, ¶144.

45. Claim 51

Ground 1A, Claim 15. EX1003, ¶145.

B. GROUND 1B—Claims 9, 13, 24, 28, 45, and 49 are obvious over Nowka and Borkar

1. Overview of Borkar

Borkar is about controlling parameters such as performance, power consumption, and temperature in a processor. EX1006, Abstract, 2:2-3. Borkar discusses controlling these parameters by changing the clock frequency, supply voltage, and threshold voltage (via body bias signals). EX1006, 2:49-54, Figs. 1-4,

5, 7, 9; EX1003, ¶¶146-150. Specifically, Borkar explains that the goal in an integrated circuit may be “keeping power consumption below a particular level” or “obtaining the highest performance while not exceeding a particular power consumption level.” EX1006, 12:10-15. According to Borkar, “[a] simple but imprecise way [to avoid exceeding power consumption levels] is to not allow the supply voltage, threshold voltages, or frequency, to pass certain levels. A more precise way is to detect current being consumed.” EX1006, 13:4-8. For example, Figures 1 and 7 show current detection circuitry that detects current being consumed and provides that information to the voltage and frequency control circuitry. EX1006, 4:58-60, 7:39-42, 13:8-11, Figs. 2, 4. The control circuitry can then determine the power being consumed. EX1006, 4:64-67, 6:64-67, 13:7-8.

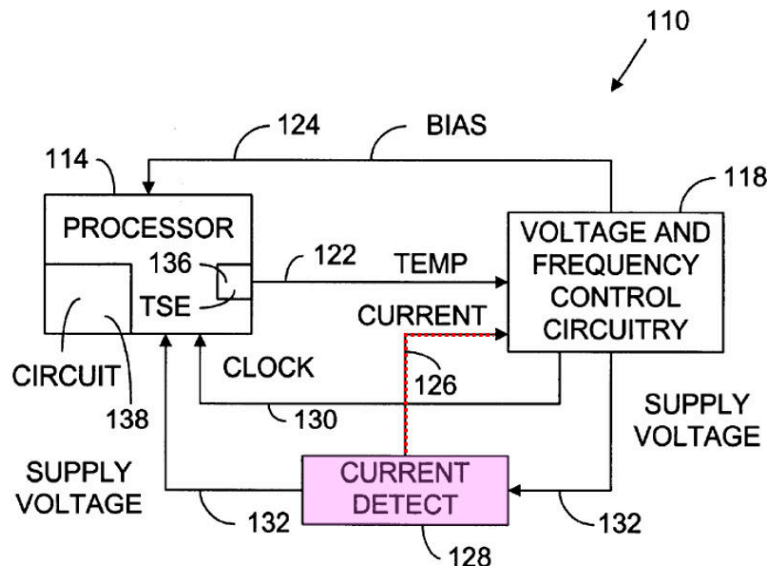


FIG. 1

EX1006, Fig. 1.

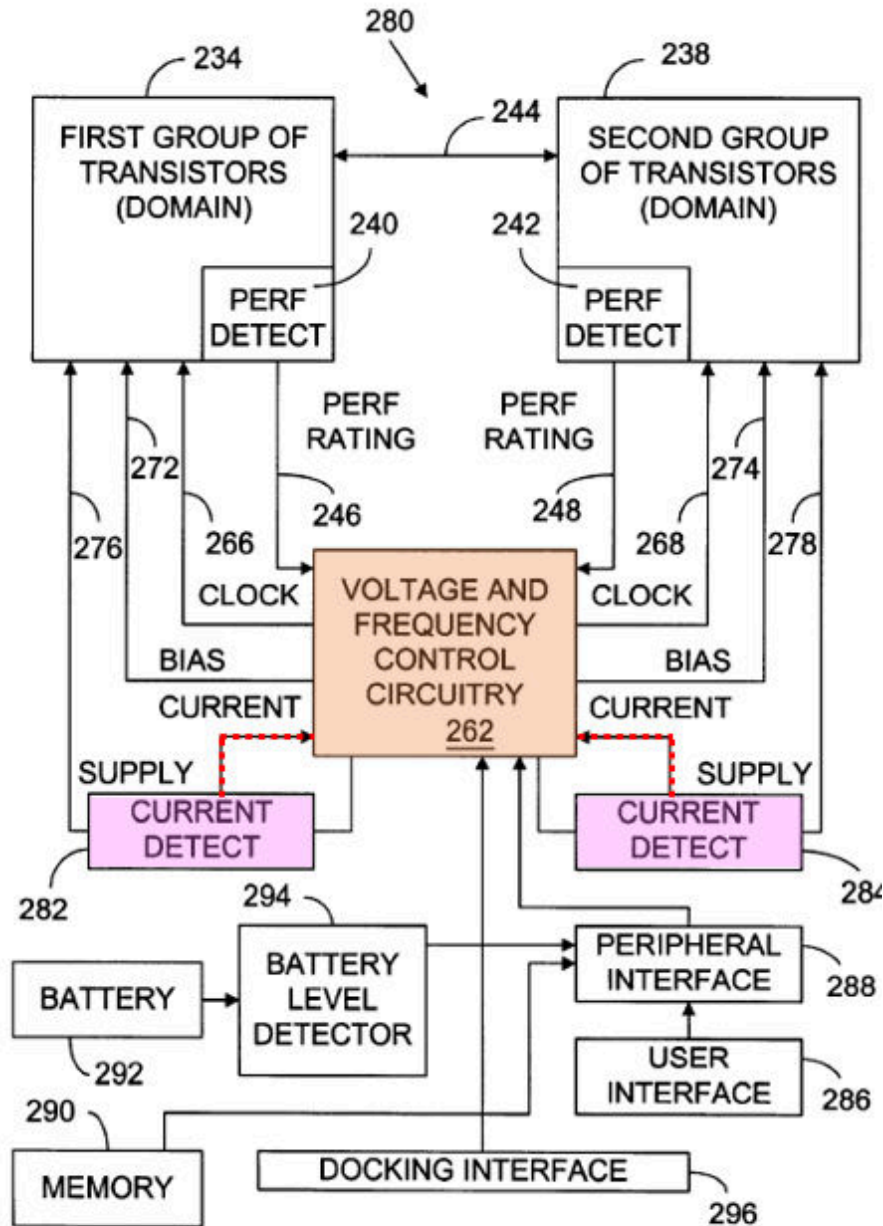


FIG. 7

EX1006, Fig. 7.

2. Nowka-Borkar Combination

A POSITA would have been motivated to incorporate the teachings of Borkar into Nowka's disclosure with a reasonable expectation of success. EX1003, ¶¶151-

157. Nowka and Borkar are in the same field of endeavor: power management on an integrated circuit. EX1004, 1441; EX1006, 2:49-57; §III.A.1 (Nowka summary), §III.B.1 (Borkar summary); EX1003, ¶152. Further, Nowka and Borkar address the same known problem—the need to balance performance with power consumption in electronic systems. EX1004, 1441 (“While [devices’] peak performance demands tend to be significant, they are also highly power constrained.”), EX1006, 1:20-21, 5:45-46 (“The user may specify certain power conditions or a power versus performance tradeoff.”); EX1003, ¶153.

Both Nowka and Borkar teach the known solution of using distinct units on an integrated circuit whose power can be independently controlled. EX1004, 1442 (“To support DVS in this SOC, the power distribution has been divided into four distinct domains as shown in Fig. 3), Fig. 3; EX1006, 10:34-39 (“The first and second groups of transistors may be different function unit blocks (FUBS) on the same chip...”); EX1003, ¶154. Nowka and Borkar also both suggest the identified, predictable solution of dynamically changing variables such as frequency and voltage according to certain needs and operation of the integrated circuit. EX1004, 1442 (“dynamic voltage scaling”); EX1006, 6:48-53 (“selecting the body bias, supply voltage, and/or clock settings in control circuitry...”); EX1003, ¶155.

Because Nowka and Borkar provide similar solutions to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and

been motivated to combine, the two references when considering techniques for Nowka's dynamic power management functionality. As one example, a POSITA would have been motivated to look to Borkar's technique for calculating power consumption based on voltage and current because, for example, Nowka teaches that "during peak activity the power consumption of the processor core is best kept at or below 500 mW." EX1004, 1441; EX1003, ¶156. In addition, Nowka explains that "[s]tatic power due to reverse-biased junction current, sub-threshold leakage, gate leakage and analog current sources can limit the operating lifetime of battery-powered systems. Decreasing the standby power of the integrated circuit increases shelf-life as well as overall energy efficiency." EX1004, 1446. Thus, a POSITA would have been motivated to look to a threshold voltage-tuning solution like the one Borkar describes to alleviate static power in Nowka's SOC. EX1003, ¶157.

3. Claim 9

The Nowka-Borkar combination renders obvious Claim 9. EX1003, ¶¶158-161. First, Borkar explains how ***threshold voltage*** interacts with performance and power consumption, and how controlling threshold voltage can alleviate leakage power consumption. *See* EX1006, 3:50-55, 6:15-24 (discussing using threshold voltage to balance performance and power consumption). Second, Borkar discloses the concept of modifying ***threshold voltage*** of transistors in response to temperature or power conditions in the integrated circuit. *See* EX1006, 4:21-32. Third, Borkar

explains that “when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the *threshold voltages* of some or all of the transistors. This will reduce the power consumption to maintain the battery.” EX1006, 5:25-30. In each of these examples, threshold voltages are changed to change the power consumption based on needs and operation of the system. EX1003, ¶¶159-160.

Nowka teaches that “[s]tatic power due to reverse-biased junction current, sub-threshold leakage, gate leakage and analog current sources can limit the operating lifetime of battery-powered systems.” EX1004, 1446. A POSITA would have been motivated to implement Borkar’s threshold voltage-tuning mechanism in Nowka based on the understanding that modifying threshold voltage helps reduce static power consumption. EX1003, ¶161; *supra* §III.B.2. For example, Borkar explains that “[t]he leakage power consumption is higher with a smaller threshold voltage and lower with a higher threshold voltage” and that “leakage power can still be reduced by increasing the threshold voltages,” and such concepts were well-understood in the art. EX1006, 3:53-55, 6:23-24; EX1003, ¶161. A POSITA would have needed only routine electrical and computer engineering principles to implement changing threshold voltages like Borkar describes. EX1003, ¶161.

4. Claim 13

The Nowka-Borkar combination renders obvious Claim 13. EX1003, ¶¶162-169. To start, Nowka discloses that “during peak activity the power consumption of the processor core is best kept at or below 500 mW.” EX1004, 1441. A POSITA would have understood that this teaching from Nowka suggests/recommends implementing a *power consumption threshold level* and would have looked to a reference like Borkar disclosing such a mechanism. EX1003, ¶163.

Borkar discloses numerous embodiments that explicitly show “current detection circuitry” providing current signals to “voltage and frequency control circuitry.” EX1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7. Because current multiplied by supply voltage is power consumption, Borkar’s system can *monitor power consumption* by monitoring current signal. EX1006, 4:64-67, 13:7-8. As a POSITA would have understood, by calculating the power consumption in this way, the system can monitor the power consumption and *perform* appropriate *actions*, such as changing body bias, supply voltage, and clock frequencies, in the event the *power consumption* approaches or *crosses the threshold level*. EX1006, 6:1-7, 13:2-7; EX1003, ¶¶164-165.

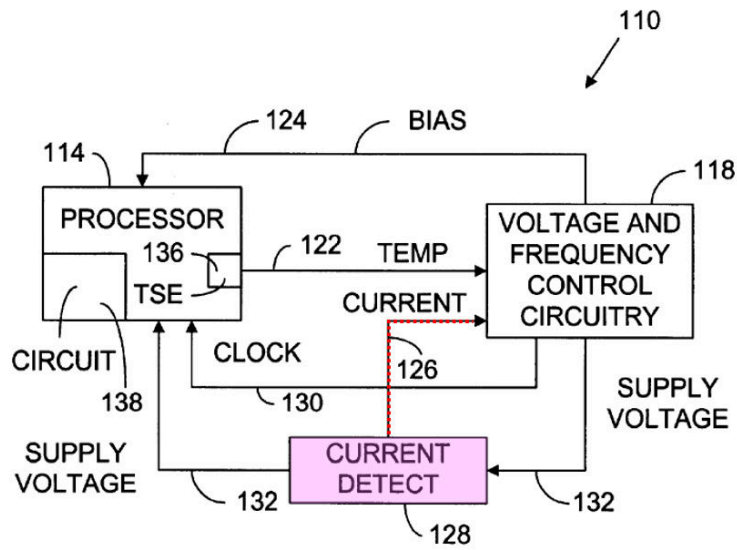


FIG. 1

EX1006, Fig. 1.

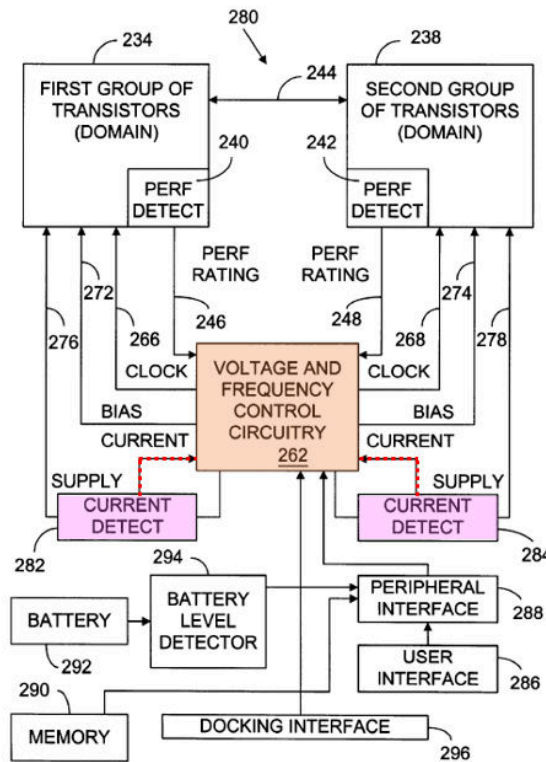


FIG. 7

EX1006, Fig. 7.

As an additional basis to establish obviousness, Borkar teaches “control circuitry” that “*monitors* a temperature signal...related to the temperature of [a] processor” (*power consumption level*). EX1006, 4:12-20; *see also* EX1001, 6:47-50 (explaining that “temperature” is an example of a “power consumption level[]”). According to Borkar, “if the temperature TACTUAL of [the] processor...exceeds an upper temperature limit THIGH” (*determining whether a threshold level was crossed*), the system responsively *performs* an appropriate *action*—e.g., “change[s] the body bias, supply voltage, and/or clock signal settings”—“to decrease temperature.” EX1006, 4:21-46; EX1003, ¶167.

A POSITA would have been motivated to combine Borkar’s power consumption monitoring with Nowka’s voltage and frequency scaling to achieve more precise and predictable power consumption control because Nowka teaches that “during active computation [the system’s] required performance tends to vary widely and quickly as a function of the workload” and “during peak activity the power consumption of the processor core is best kept at or below 500 mW.” EX1004, 1441; EX1003, ¶166; *supra* §III.B.2. Likewise, the POSITA would have been motivated to integrate Borkar’s temperature monitoring techniques with Nowka to provide the predictable benefit of preventing overheating. *E.g.*, EX1006, 1:11-56; EX1003, ¶167. The POSITA would have needed only routine electrical and computer engineering principles to implement Borkar’s temperature/power

monitoring and threshold-comparing mechanisms in Nowka's SOC, as demonstrated by Borkar's implementation in a system analogous to Nowka's. EX1006, 2:49-52; EX1003, ¶168. Such a combination would predictably result in improved performance and longevity. *Id.*

As yet another basis to establish obviousness, Nowka teaches that "the clocks to the individual functional cores can be frozen by the clock and power management software...in response to inactivity." EX1004, 1445. A POSITA reading this aspect of Nowka would have understood that the "software" is implementing a basic and well-known control algorithm of: (i) ***monitoring*** the activity (***power consumption***) of the individual functional cores (***power islands***, per Ground 1A, Element_1[p]-1[a]), (ii) ***determining whether*** the activity (***power consumption***) ***level crosses*** below a ***predetermined threshold***; and (iii) responsively ***performing the action*** of freezing the corresponding clock. EX1003, ¶169.

5. Claim 24

Ground 1B, Claim 9. EX1003, ¶170.

6. Claim 28

Ground 1B, Claim 13. EX1003, ¶171.

7. Claim 45

Ground 1B, Claim 9. EX1003, ¶172.

8. Claim 49

Ground 1B, Claim 13. EX1003, ¶173.

C. GROUND 1C—Claim 35 is obvious over Nowka and Boerstler

1. Overview of Boerstler

Boerstler relates to controlling the timing of signals in integrated circuits by using a voltage controlled oscillator. EX1007, Abstract; EX1003, ¶¶174-176. Boerstler teaches that a voltage multiplexer can be used as part of a voltage controlled oscillator (“VCO”), which is “important for applications such as processor clock generation and distribution, wired and wireless communication, system synchronization and frequency synthesis.” EX1007, 1:24-27. Boerstler’s VCO, shown in Fig. 4 below, is implemented using a control voltage multiplexer, an interleaved ring oscillator, and a true/complement generator.

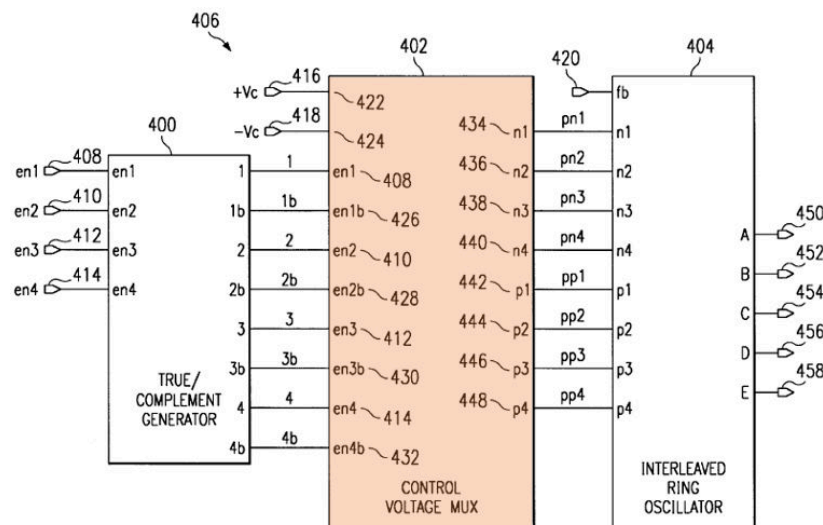


FIG. 4

EX1007, Fig. 4.

2. Nowka-Boerstler Combination

A POSITA would have been motivated to incorporate the teachings of Boerstler into Nowka's disclosure with a reasonable expectation of success. EX1003, ¶¶177-180. First, Nowka and Boerstler resulted from work performed at the same company, IBM. EX1004, 1446 ("IBM's Austin Research Laboratory..."); EX1007, (73) (showing IBM as assignee). Second, Nowka and Boerstler are in the same field of endeavor and involve similar concepts, such as clock generation and distribution in integrated circuits. EX1004, 1444 ("the clock generation subsystem is key to supporting a voltage scalable design."); EX1007, 1:23-27 (explaining that a VCO is "extremely important for applications such as processor clock generation..."); EX1003, ¶178. Third, Nowka cites Boerstler as a reference that describes the VCO architecture used in Nowka's integrated circuit. EX1004, 1447 (reference 11). Because Nowka and Boerstler provide similar solutions to a similar problem within the same field of endeavor, and because Boerstler is explicitly cited in Nowka, a POSITA would have looked at, and been motivated to combine, the two references when implementing Nowka's power control circuitry. EX1003, ¶180.

3. Claim 35

The Nowka-Boerstler combination renders obvious Claim 35. EX1003, ¶¶181-185. Nowka discloses a VCO integrated into the phase locked loop (PLL), as shown in Figure 7. EX1004, Fig. 7. The VCO is described as an "interleaved

five-stage ring oscillator” taken from reference 11 of the Nowka paper, which is Boerstler. EX1004, 1444, 1447.

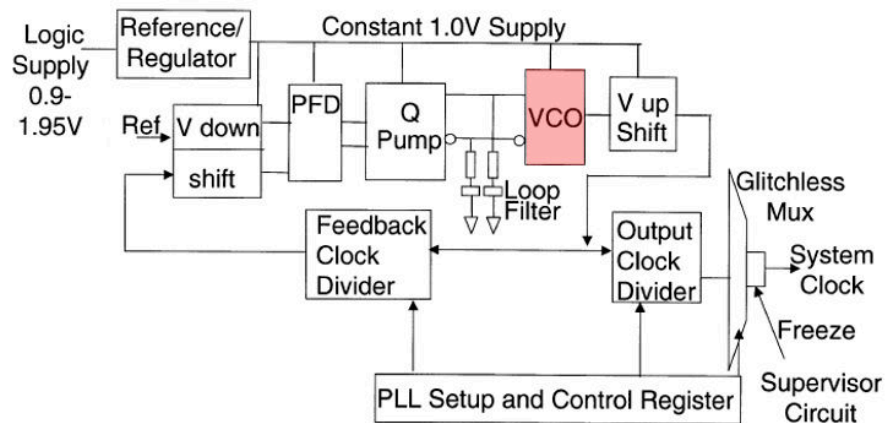


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

Boerstler’s voltage controlled oscillator (VCO) is comprised of a control *voltage multiplexor* that can be used to change the voltage level of a control voltage. EX1007, 5:50-55, Fig. 4. As explained by Boerstler, the control *voltage multiplexor* “is used to select control elements that are to be enabled within interleaved ring oscillator 404,” (EX1007, 5:65-6:1), and “the analog control voltage is channeled to the appropriate control elements by the analog multiplexer,” (EX1007, 7:2-4). EX1003, ¶¶182-185.

D. GROUND 1D—Claims 1-12, 14-23, 25-27, 29-34, 36-48, 50-51 are obvious over Nowka and Bertin

As discussed at Ground 1A, Nowka’s disclosure matches the ’306 patent’s preferred embodiments in multiple material respects. Nevertheless, if Patent Owner

attempts to rebut Ground 1A by arguing that Nowka does not *determine* an explicitly prescribed *target power level*, the Nowka-Bertin combination presented here in Ground 1D addresses this narrow view of the Challenged Claims.⁴ Integration of Bertin’s teachings does not disturb the aspects of Nowka mapped to dependent Claims 2-8, 10-12, 14-15, 17-23, 25-27, 29-34, 36, 38-44, 46-48, 50-51. To avoid repetition, the analysis of these dependent claims is not repeated below because it is identical to Ground 1A and fully incorporated here in Ground 1D. From Ground 1A, only Independent Claims 1, 16, and 37 are addressed below. Dependent Claims 9, 24, and 45, which are not challenged in Ground 1A, are also addressed below based on Bertin’s complementary teachings. EX1003, ¶¶186-187.

1. Overview of Bertin

Bertin “relates to integrated circuits and more particularly intelligent power management of the integrated circuit.” EX1027, 1:14-16; EX1003, ¶¶188-189. As in Nowka and the ’306 patent, Bertin’s intelligent power management technique aims to “optimize[] chip power/performance” by accounting for “the demands placed on the integrated circuit” and providing “independently controllable” units “operated at one of plural power levels.” EX1027, 4:49-54, 1:63-2:11.

⁴ Notably, the Board determined that Bertin anticipates and renders obvious multiple claims of a similar power management patent in IPR2015-00324 (Paper 39).

Among other things, Bertin teaches that a “power management unit [] sets the power levels for the different units” based on logic that “determines, for each functional unit, whether the power requirement and power status for the unit are in agreement.” EX1027, 5:35-39. “In the event that a power transition is necessary,” Bertin’s technique “transition[s] the performance level of that particular functional unit.” EX1027, 5:44-50; *see also* 6:4-18. For example, Bertin’s approach places the appropriate units “in a high power state” when “[e]xecution of the [application] instruction[s] at a high rate [is] require[d].” EX1027, 2:8-11.

2. Nowka-Bertin Combination

A POSITA would have been motivated to implement Nowka’s “software control” for dynamic voltage and frequency scaling, (EX1004, 1442, 1444, 1446), based on prescribed “power levels” (or “power state[s]”) that correspond to “power requirement[s]” dictated by an application, as taught by Bertin (EX1027, 5:35-39, 2:8-11). EX1003, ¶¶190-198. Integrating the supplemental teachings of Bertin with Nowka’s disclosure would have involved nothing more than applying known solutions to known problems in the field of power management for integrated circuits to achieve predictable outcomes. EX1003, ¶190. The fundamental aspects of Nowka’s disclosure would remain intact, bolstered by the well-known and beneficial teachings of Bertin to arrive, with a reasonable expectation of success, at a system within the scope of the Challenged Claims. *Id.*

First, a POSITA would have been prompted to pursue the above-discussed combination with Bertin based on Nowka's teachings and suggestions to do so. For example, as discussed at Ground 1A, Element_1[a], Nowka teaches and suggests the notion of providing prescribed maximum/minimum power levels based on the "performance demands" of "battery-powered applications." EX1004, 1441 ("the processor core is best kept at or below about 500 mW"); *see also* 1442, 1444 ("a range of standby power levels"), 1446 (describing "a range of standby power levels"); EX1003, ¶¶192-193 (Dr. Rosing detailing examples). Bertin's straightforward approach of determining a prescribed power level that reflects application-based demand and taking proper actions to transition power consumption to "bring the [power] requirements and status into agreement," (EX1027), 5:45-47), is what a POSITA would have understood Nowka to teach and suggest. EX1003, ¶¶193.

Second, the technique of utilizing prescribed power levels or states to implement power management on integrated circuits was commonly implemented by 2003. EX1003, ¶¶194-195. Prescribed power levels were an exceedingly well-known solution to the equally well-known problem of balancing performance and power consumption in electronic systems, particularly battery-powered devices capable of running high-performance applications. EX1003, ¶196. Bertin utilizes power levels/states for this purpose, and it would have been axiomatic for a POSITA

to do the same in the context of Nowka's SOC with robust dynamic power management capabilities like voltage and frequency scaling. EX1003, ¶196.

Third, a POSITA would have understood that utilizing prescribed power levels or states (as taught by Bertin) provides the advantage of facilitating communication between the application creating the performance demands and the software/circuitry coordinating on-chip dynamic power management. EX1003, ¶197; EX1027, 5:35-50, 7:8-16. Fourth, and consistent with Nowka's teachings to independently control the power consumption of individual cores, (EX1004, 1445), a POSITA would have appreciated the effectiveness and efficiency of Bertin's disclosed approach of utilizing prescribed power levels to independently control any given "functional unit" on the chip based on whether a coded instruction of an application will utilize that unit, (EX1027, 2:6-52, 4:39-5:6). EX1003, ¶198.

3. Claim 1

(a) Element_1[p]

Ground 1A, Element_1[p]. Additionally, to the extent Patent Owner argues that Nowka's "cores" within a variable voltage logic domain that can be individually frequency scaled somehow do not render obvious the claimed *power islands*, integration of Bertin's teachings further bolsters this mapping. EX1003, ¶¶199-201. For example, Bertin makes clear that individual functional units—like Nowka's "cores"—have "independently controllable body voltage or threshold voltage."

EX1027, 1:63-2:11. Thus, in the Nowka-Bertin combination, there is no question that the cores within the logic domain have the capability of being controlled individually and independently with respect to both voltage scaling and frequency scaling. EX1003, ¶200. A POSITA would have been motivated to pursue this aspect of the combination to provide additional flexibility in the types of dynamic power management control schemes that the SOC can support. EX1003, ¶201.

(b) Element_1[a]

Ground 1A, Element_1[a]. Additionally, to the extent Patent Owner argues Nowka falls short, the Nowka-Bertin combination renders obvious *determining a target power level*. EX1003, ¶¶202-203. For example, as discussed (*supra* §§III.D.1-2), Bertin teaches a power manager that “sets the *power levels* for the different units” based on logic that “*determines*, for each functional unit, whether the power requirement and power status for the unit are in agreement.” EX1027, 5:35-39. In the Nowka-Bertin combination, Nowka’s “power management software,” (EX1004, 1444), employs Bertin’s conceptual approach and, thus: (i) *determines* a specified *target power level* for the dynamically voltage-scaled and frequency-scaled logic domain based on the “performance demands of the application,” (EX1004, 1446); and (ii) compares that *target power level* to the logic domain’s current power status. EX1003, ¶203.

(c) Element_1[b]

Ground 1A, Element_1[b]. Additionally, to the extent Patent Owner argues Nowka falls short, the Nowka-Bertin combination renders obvious *determining an action to change the power consumption level of one of the power islands to the target power level*. EX1003, ¶¶204-205. In the Nowka-Bertin combination, Nowka’s “power management software” employs Bertin’s conceptual approach and, thus, utilizes the capabilities at its disposal (*determined actions*)—namely, “dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating”—to transition the logic domain and “match *the power consumption [level]*” with the *target power level* (*supra* Element_1[a]). EX1027, 5:35-50, 6:52-57; EX1004, 1444, 1442; EX1003, ¶205; *supra* §III.D.1-2.

(d) Element_1[c]

Ground 1A, Element_1[c]; Ground 1D, Element_1[b] (both identifying “*frequency* scaling” as one of the *determined actions*). EX1003, ¶206.

4. Claim 9

Ground 1A, Element_[7]; Ground 1D, Element_1[p] (discussing, per Bertin, adjusting power level by changing the “threshold voltage”). EX1003, ¶207.

5. Claim 16

(a) Element_16[p]

Ground 1A, Elements_1[p]-1[a], 16[p] (Nowka); Ground 1D, Elements_1[p]-1[a] (Nowka-Bertin combination). EX1003, ¶208.

(b) Element_16[a]

Ground 1A, Elements_1[p]-1[a], 16[a] (Nowka); Ground 1D, Elements_1[p]-1[a] (Nowka-Bertin combination). EX1003, ¶209.

(c) Element_16[b]

Ground 1A, Elements_1[a]-1[c], 16[b] (Nowka); Ground 1D, Elements_1[a]-1[c] (Nowka-Bertin combination). EX1003, ¶210.

6. Claim 24

Ground 1A, Element_[22]; Ground 1D, Element_1[p], Claim 9. EX1003, ¶211.

7. Claim 37

(a) Element_37[p]

Ground 1A, Elements_1[p]-1[a], 37[p] (Nowka); Ground 1D, Elements_1[p]-1[a] (Nowka-Bertin combination). EX1003, ¶212.

(b) Element_37[a]

Ground 1A, Elements_1[a]-1[c], 37[a] (Nowka); Ground 1D, Elements_1[a]-1[c] (Nowka-Bertin combination). EX1003, ¶213.

(c) Element_37[b]

Ground 1A, Elements_1[b], 37[b]. EX1003, ¶214.

8. Claim 45

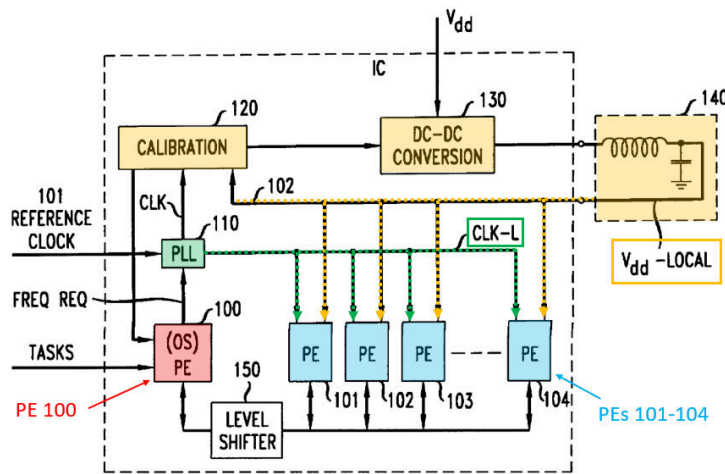
Ground 1A, Element_[43]; Ground 1D, Element_1[p], Claim 9. EX1003,
¶215.

E. GROUND 2A—Claims 1-5, 7-9, 11, 16-20, 22-24, 26, 31-33, 36-45, 47 are obvious over Nicol

1. Overview of Nicol

Nicol discloses a dynamic load-balancing mechanism that divides tasks among multiple processors and adjusts the frequency and voltage of those processors to minimize power consumption. EX1008, Abstract; EX003, ¶¶216-222. In the Figure 2 embodiment below, an application “is subdivided into N concurrent task streams” and “mapped to N PEs [(processing elements)] under control of [a] real-time operating system executed on PE 100.” EX1008, 3:10-13, 3:22-23.

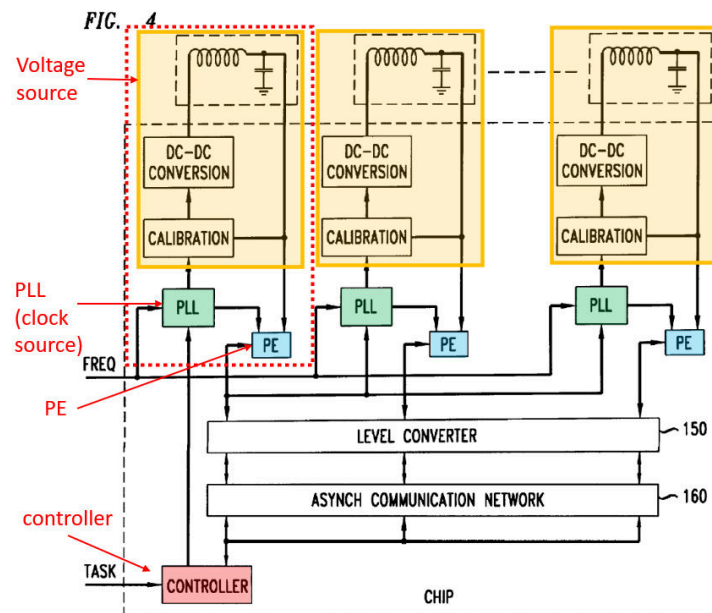
FIG. 2



EX1008, Fig. 2.

As a result, each PE can be “lightly loaded,” which “allows the clock frequency of the PEs to be reduced,” thus, “reducing the necessary supply voltage.” EX1008, 3:24-30.

Nicol also explains that there are “tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE[s] within the multiprocessor would require a higher operating frequency and a higher operating voltage.” EX1008, 5:60-65. Accordingly, Figure 4 below shows each PE with its own associated clock source and voltage source to allow “the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” EX1008, 5:66-6:3, Fig. 4.

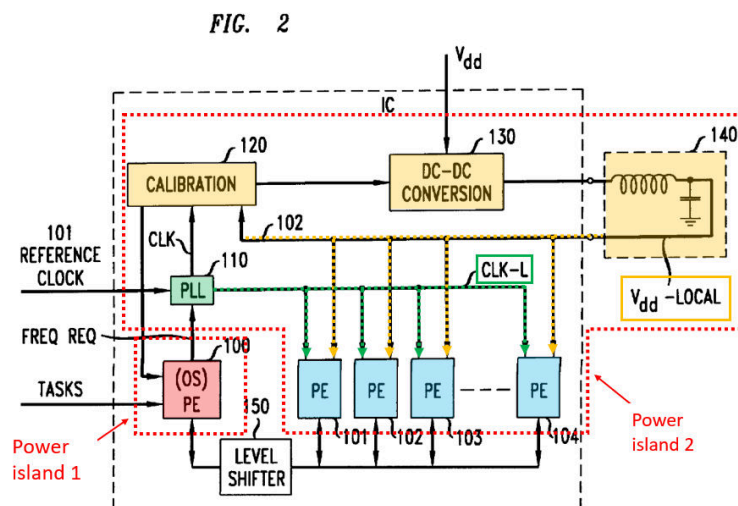


EX1008, Fig. 4.

2. Claim 1

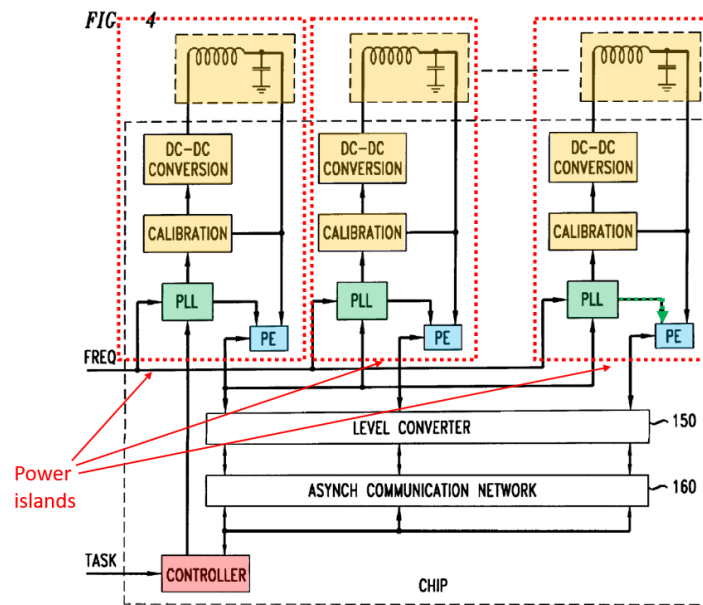
(a) Element_1[p]

To the extent the preamble is limiting, Nicol discloses and renders obvious *a method for managing power on an integrated circuit including a plurality of power islands*. EX1003, ¶¶223-225. For example, Nicol improves the performance of multi-processor chips by dynamically controlling the processing load of the chips and further controlling the frequencies/voltages to minimize power consumption. EX1008, Abstract, 2:18-22, 3:21-42. It would have been apparent or obvious to a POSITA that Nicol's integrated circuit *includes a plurality of power islands*. EX1003, ¶¶223-225; EX1001, 3:51-54. In the Figure 2 embodiment, PE 100 and PEs 101-104 form different *power islands* because they are sections, delineations, partitions, or divisions of the integrated circuit, are powered independently, and receive separate clock sources. EX1008, 4:35-37; EX1003, ¶224.



EX1008, Fig. 2.

In the Figure 4 embodiment, each PE (with its control circuitry) is a *power island* because each is a section, delineation, partition, or division of the integrated circuit and has an independent voltage and clock source, allowing for independent power control by varying supply voltage/frequency.⁵ EX1008, 5:66-6:2; EX1003, ¶225.



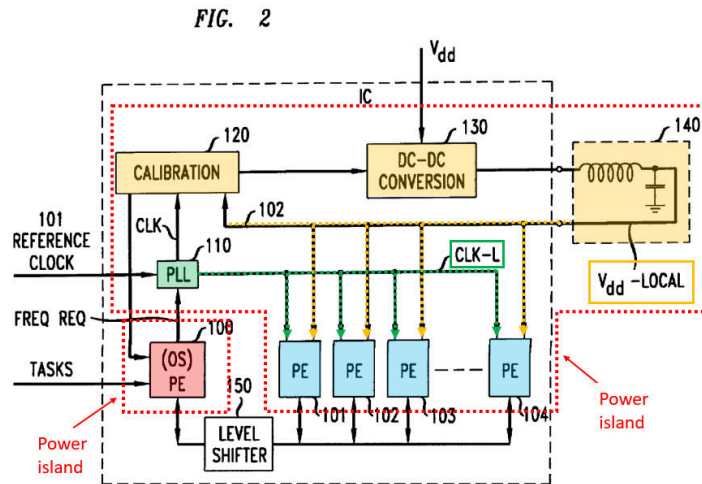
EX1008, Fig. 4.

(b) Element_1[a]

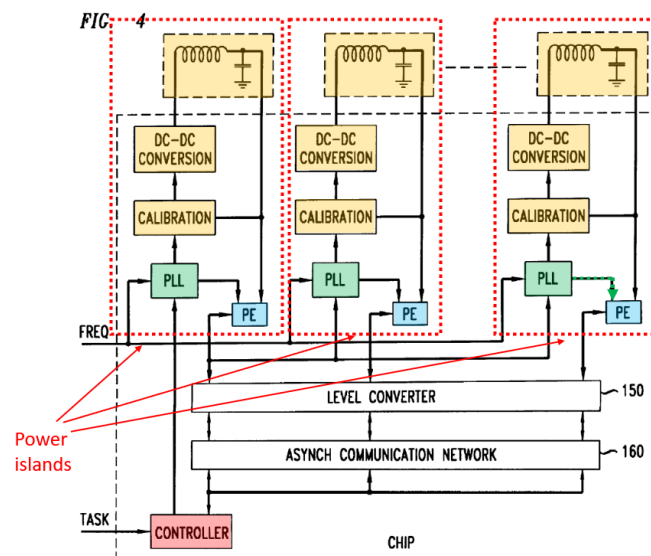
Nicol discloses and renders obvious *determining a target power level for a power island based on the needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands.* EX1003, ¶¶226-237.

⁵ This aspect of Nicol satisfies even the narrow district court “power islands” construction. EX1013, 23; EX1003, ¶225.

First, Nicol provides that *power consumption is independently controlled within each power island*. EX1008, 3:24-31, 5:42-45, 5:66-6:2; EX1003, ¶¶227-229. The ability for independent control is most explicit in the Figure 4 embodiment, where “[a] separate power supply for each PE in a chip [allows] the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” EX1008, 5:66-6:2; EX1003, ¶229.



EX1008, Fig. 2.



EX1008, Fig. 4.

Nicol discloses and renders obvious *determining a target power level for one of the power islands based on needs and operation of the integrated circuit*. EX1003, ¶¶230-236. As a POSITA would have known, with systems like Nicol’s that employ dynamic power management, the desired (*target*) *power level* is the minimum power consumption that satisfies the performance constraints. EX1003, ¶230; EX1001, 4:28-33 (explaining that “[t]he *target power level* is a *desired*, calculated, or specified power consumption”). Accordingly, Nicol’s disclosure seeks to achieve “[i]mproved performance of multi-processor chips...by dynamically controlling the processing load of chips and controlling...the operating voltages [and frequencies] of those chips so as to minimize overall power consumption.” EX1008, 2:18-22. And, in Nicol, this *determining of the target power level* is performed by the controlling operating system—e.g., the real time operating system (RTOS) in PE 100 in the Figure 2 embodiment and the operating system in the “controller” in the Figure 4 embodiment. *Id.*; EX1003, ¶231.

In the Figure 2 system, the *target power level* is set “to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PE’s.” EX1008, 3:19-21. In other words, the objective (or *needs and operation*) in the Figure 2 system is to load the PEs as evenly as possible so that the task in its entirety can be completed within a required amount of time. EX1008, 3:47-49, 3:61-65; EX1003, ¶231. Nicol’s *target power level*, then, corresponds to

the lowest frequency needed to complete the task in the required time. EX1008, 3:22-4:5, 5:23-29, cl. 1 (“determining a lowest frequency”), cl. 46 (“frequency is set to a minimum level”). In addition, Nicol sets the corresponding lowest needed supply voltage, which is another example of determining a *target power level*. EX1008, 4:5-16; EX1003, ¶232.

Referencing the Figure 4 embodiment, Nicol explains how “[i]t is possible to anticipate that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called. When so anticipated, some of the fast memory can be released (storing some of the data that needed to be remembered) at a leisurely pace. That is, lower clock frequency can be employed in connection with the fast memory and the hard drive, with a corresponding lower supply voltage, resulting in an overall power saving in both the memory’s operation and in the operation of the hard drive.” EX1008, 6:39-56. Thus, Nicol discloses and renders obvious that, *based on needs and operation of the system* (anticipating that the memory stored in the fast memory can be discarded), there is a *determination of the target power level* (reflected by the lowest frequency and voltage required for that lower performance). EX1003, ¶233.

In addition, a POSITA would have found it obvious from these examples that Nicol’s operating system is *determining a target power level based on needs and operation of the integrated circuit* because frequency is directly proportional to

power and voltage is quadratically related to power. EX1008, 1:26-29, 3:28-31; EX1003, ¶234. Nicol’s approach mirrors the disclosure in the ’306 patent in this way. EX1001, 7:38-50, Fig. 5; EX1003, ¶¶234-235.

To be clear, Nicol renders obvious *based on needs and operation of the integrated circuit* under either the plain and ordinary meaning of this limitation or the stipulated construction in the prior litigations. EX1003, ¶236. As discussed, Nicol’s disclosure mirrors the ’306 patent’s disclosure on this limitation. Moreover, that the system can “anticipate that memory...is so old as to be unlikely to be accessed before a new application is called” such that “lower clock frequency can be employed,” (EX1008, 6:39-56), shows that it responds to future operational needs, while the system’s ability to set the lowest corresponding frequency and voltage needed for operational performance requirements shows that it responds to current operational status of the integrated circuit. EX1008, Abstract, 2:22-27, 4:54-6:2, cl. 1; EX1003, ¶237.

(c) Element_1[b]

Nicol discloses and renders obvious *determining at least one of actions to change a power consumption level of one of the power islands to the target power level*. EX1003, ¶¶238-242.

To start, as discussed at Elements_1[a]-1[p], Nicol discloses and renders obvious determining a *target power level* for one or more *power islands*—e.g., a

minimum power consumption via a minimum frequency and/or supply voltage for one or more PEs to complete a given task by a required time, (*e.g.*, EX1008, 3:66-4:6), or to optimize overall power savings given the operating needs of the system, (*e.g.*, EX1008, 6:39-56). Nicol further discloses and renders obvious ***determining an action to change the power consumption level to the target power level.*** EX1003, ¶¶238-239. Namely, Nicol’s operating system “***determine[s]***” the appropriate frequency and/or supply voltage of the PEs (***power islands***) based on the ***target power level.*** EX1008, 3:66-4:10; *see also* 1:27-36 (explaining that “power consumption of a CMOS circuit increases linearly with operating frequency and quadratically with supply voltage”), 3:22-42.

For example, referencing Figure 2, Nicol discloses that after the “operating system of PE 100” “divide[s] the collection of tasks as evenly as possible (in terms of needed processing time),” it “adjust[s] the clock frequency to insure [sic] that the most heavily loaded PE carries out its assigned tasks within the required completion time. Once the frequency is thus determined, a minimum supply voltage can be determined.” EX1008, 3:66-4:6; *see also* cl. 2 (“...a frequency at which or above which the sub-circuit operates is set to said determined frequency”); EX1003, ¶240. Nicol provides further examples, including exemplary frequency and voltage levels and the timing of these actions. EX1008, 3:31-42, 4:54-5:2, Fig. 3; EX1003, ¶¶241. Nicol similarly discloses examples of setting a lower frequency and lower supply

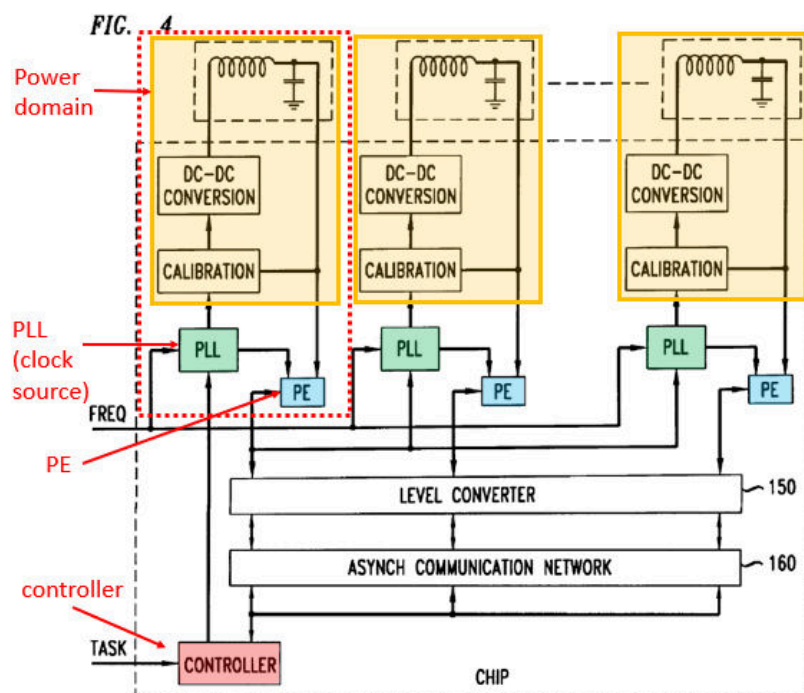
voltage to match the needs of the system in an embodiment where it is desirable for different components to operate at different speeds (such as in Figure 4). EX1008, 6:39-56; EX1003, ¶242; *supra* Element_1[a].

(d) Element_1[c]

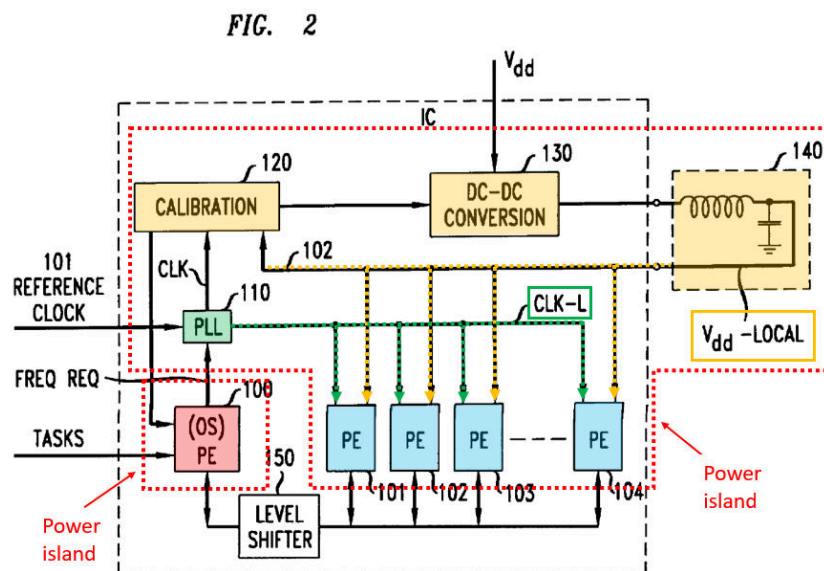
As discussed at Elements_1[a]-1[b], Nicol discloses and renders obvious the features of Element_1[c] by explaining how the operating system facilitates *performing the actions of selecting a frequency and/or voltage to change the power consumption level of one of the power islands (PEs) to the target power level* (the power to timely complete a task and/or to optimize power savings). EX1008, 3:21-4:10, 4:17-66, cl. 2; EX1003, ¶243.

3. Claim 2

Nicol discloses and renders obvious Claim 2. For example, Figure 4 shows that the PE of each *power island* (Elements_1[p]-1[a]) has its own associated power supply and clock supply, and a POSITA would have understood from basic circuit design principles that each PE would have to be placed *geographically* close to its respective power supply to minimize voltage dissipation and clock signal deterioration. EX1008, Fig. 4; EX1003, ¶244. Similarly in Figure 2, a POSITA would have understood that the *power island* containing PEs 101-104 (Elements_1[p]-1[a]) would be *geographically* grouped together to improve routing of supply and control signals. EX1008, Fig. 2; EX1003, ¶245.



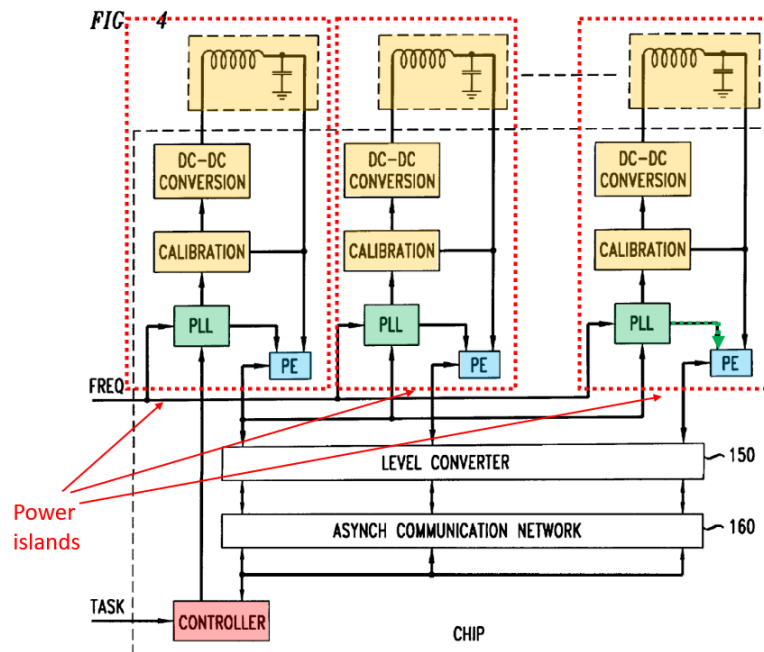
EX1008, Fig. 4.



EX1008, Fig. 2.

4. Claim 3

Nicol discloses and renders obvious Claim 3. First, a POSITA would have understood and found obvious that the *power islands* in the Nicol's Figure 4 embodiment (Elements_1[p]-1[a]) are *delineated based on functional circuitry* because each PE is capable of executing different functions. EX1008, 2:53-56, 3:66-4:5, 5:23-29; EX1003, ¶¶246-248. The ability to allocate different tasks to the PEs facilitates the provision of individual power and clock source. EX1003, ¶247.

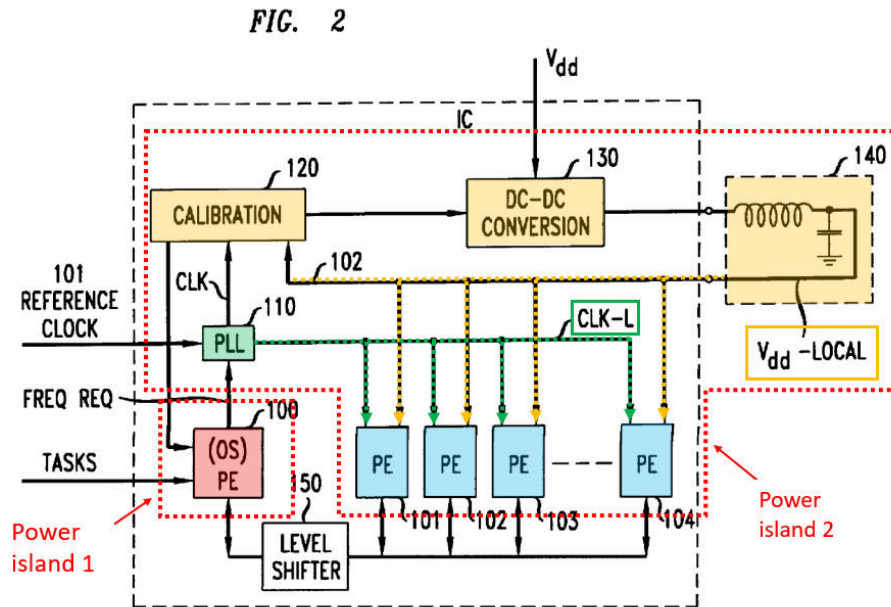


EX1008, Fig. 4.

A POSITA would have further understood and found obvious that the *power islands* in Nicol's Figure 2 embodiment (Elements_1[p]-1[a]) are *delineated based on functional circuitry* because they are separated based on PE 100's function of

hosting the real-time operating system, which allocates tasks among the other PEs.

EX1008, 2:53-56, 3:66-4:5, 4:35-37; EX1003, ¶249.



EX1008, Fig. 2.

5. Claim 4

Nicol discloses and renders obvious Claim 4. First, a POSITA would have recognized and found obvious that each PE within the *power island* in Nicol's Figure 2 embodiment constitutes a *power sub-island* capable of being power controlled. EX1008, 2:52-53; EX1003, ¶¶250-251 (explaining that each PE includes a CPU, subject to individual control for the beneficial purpose of enabling more fine-grained power management policies capable of greater power savings). Second, a POSITA would have recognized that each PE within the *power islands* in Nicol's Figure 4 embodiment comprise sub-units whose power can be further controlled (*power sub-*

islands). EX1003, ¶252. For example, one PE could be a CPU, which a POSITA would have understood to comprise sub-units such as cores or latches that can be turned on and off individually, or otherwise controlled via clock or power gating. *Id.* A POSITA would have been motivated to implement ***power sub-islands*** based on Nicol’s teaching on power management at different levels of abstraction, as well as general knowledge in the art to implement power management at various levels of abstraction. EX1008, 6:66-7:3; EX1003, ¶253, ¶33.

6. Claim 5

Nicol discloses and renders obvious Claim 5. For example, a POSITA would have understood and found obvious that each of Nicol’s PEs comprise multiple sub-units that can be independently clock gated and frequency controlled, thereby creating ***multiple clock domains***. EX1003, ¶254; *supra* analysis regarding Claim 4.

7. Claim 7

Nicol discloses and renders obvious Claim 7. For example, Nicol explains that “reduced load permits lowering the clock frequency to 100 MHz and lowering the supply voltage to 2.1V.” EX1008, 4:54-66. In Nicol’s Figure 2 embodiment, V_{dd} -local supplying the ***power island*** featuring PEs 101-104 is ***modified***. EX1008, 3:31-42, 4:5-16, 4:54-5:22, 5:35-41, 5:44-49, cl. 1; EX1003, ¶¶255-256. In Nicol’s Figure 4 embodiment, “[a] separate power supply for each PE in a chip” allows for

independently programming the “corresponding lowest supply voltage” for the PE of each *power island*. EX1008, 5:66-6:2, Fig. 4; EX1003, ¶257.

8. Claim 8

Nicol discloses and renders obvious Claim 8. For example, a POSITA would have understood that V_{dd} -local in Figure 2 and the voltages supplied to each PE in Figure 4 are *source voltages* because they supply voltage from a source and, thus, allow the PEs to operate. EX1008, 3:28-31, 3:31-42, 4:5-16, 5:66-6:2, cl. 1; EX1003, ¶¶258-259.

9. Claim 9

Nicol discloses and renders obvious Claim 9. For example, Nicol explicitly describes varying the *threshold voltage* as a known on-chip voltage scaling technique. EX1008, 1:65-2:10. This discussion in Nicol shows that changing a threshold voltage was a known technique that was routinely applied to improve performance in chips, and it would have been obvious to a POSITA in the context of Nicol’s disclosure for the purpose of controlling the power consumption level. EX1003, ¶¶260-262.

10. Claim 11

Nicol discloses and renders obvious Claim 11. *See* EX1008, Claim 36 (“The apparatus of Claim 32 further comprising means within said controller for turning supply *power off* to at least one of said N processing elements.”); EX1003, ¶263.

11. Claim 16

(a) Element_16[p]

Ground 2A, Element_1[p]. Nicol further provides a **system**. *E.g.*, EX1008, 2:50-58 (“the FIG. 2 **system**”), 5:66-6:12, Figs. 2, 4, cl. 17; EX1003, ¶264.

(b) Element_16[a]

Nicol discloses and renders obvious **power control circuitry configured to control power** for the PEs of the **power islands**. For example, a POSITA would have understood that the voltage conversion circuitry and the PLL associated with each power island in the Figure 2 and 4 embodiments are **power control circuitry** because they control the power of the power island via controlling voltage and frequency. EX1008, 4:17-37, Figs. 2, 4; EX1003, ¶¶265-266.

(c) Element_16[b]

Ground 2A, Elements_1[a]-[c]. Nicol further discloses and renders obvious a **power manager** (e.g., PE 100 where the “real-time operating system” resides in Figure 2 or “controller”/PE 200 in Figure 4) as discussed for Element_1[a]. EX1003, ¶267-269.

12. Claim 17

Ground 2A, Claim 2. EX1003, ¶270.

13. Claim 18

Ground 2A, Claim 3. EX1003, ¶271.

14. Claim 19

Ground 2A, Claim 4. EX1003, ¶272.

15. Claim 20

Ground 2A, Claim 5. EX1003, ¶273.

16. Claim 22

Ground 2A, Claim 7. EX1003, ¶274.

17. Claim 23

Ground 2A, Claim 8. EX1003, ¶275.

18. Claim 24

Ground 2A, Claim 9. EX1003, ¶276.

19. Claim 26

Ground 2A, Claim 11. EX1003, ¶277.

20. Claim 31

Nicol discloses and renders obvious Claim 31. For example, Nicol suggests the rudimentary structural element of a *bus* by describing and illustrating various “line(s)” that *couple* the functional components of the integrated circuit, including the controller/operating system and the PEs. *See* EX1008, 4:17-53, Figures 2, 4; EX1003, ¶¶278-279. To the extent Nicol does not expressly disclose or suggest employing a *bus*, it would have been obvious to a POSITA that the PEs and the controlling circuitry on the chip would be connected by a bus because busses were a dominant interconnection technology. EX1003, ¶279. This is further supported

by the presence of a “level shifter” or “level converter” in Figures 2 and 4, and “asynchronous communication network” in Figure 4, which would allow for uniform frequency/voltage signals across the bus. EX1008, 6:18-33, EX1003, ¶280.

21. Claim 32

Nicol discloses and renders obvious Claim 32. For example, it would have been apparent or obvious to a POSITA that the “controller” in Nicol (PE 100 in the embodiment shown in Figure 2, “controller” in the embodiment shown in Figure 4) acts as a *master manager* because it communicates with the plurality of individual PEs within the power island(s) to manage the power consumption of the integrated circuit as a whole. EX1008, 2:53-56, 3:10-21, 3:66-4:10, 5:23-28, 6:6-13; EX1001, 5:47-53; EX1003, ¶¶281-282.

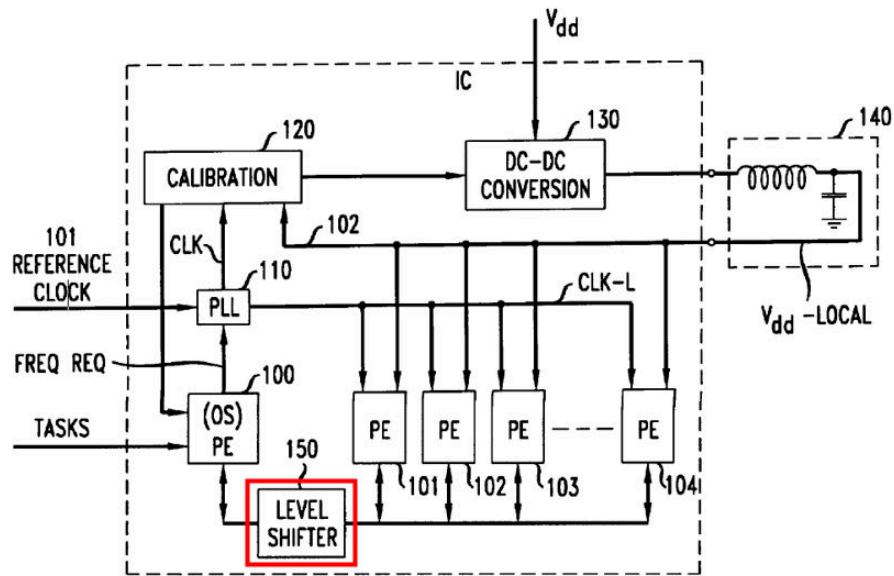
22. Claim 33

Nicol discloses and renders obvious Claim 33. For example, in each of Nicol’s embodiment, the PLL and voltage circuitry act as a *slave manager* controlling the power of the PEs within the power island(s). EX1008, 2:50-53, 6:3-6; EX1003, ¶¶283-284.

23. Claim 36

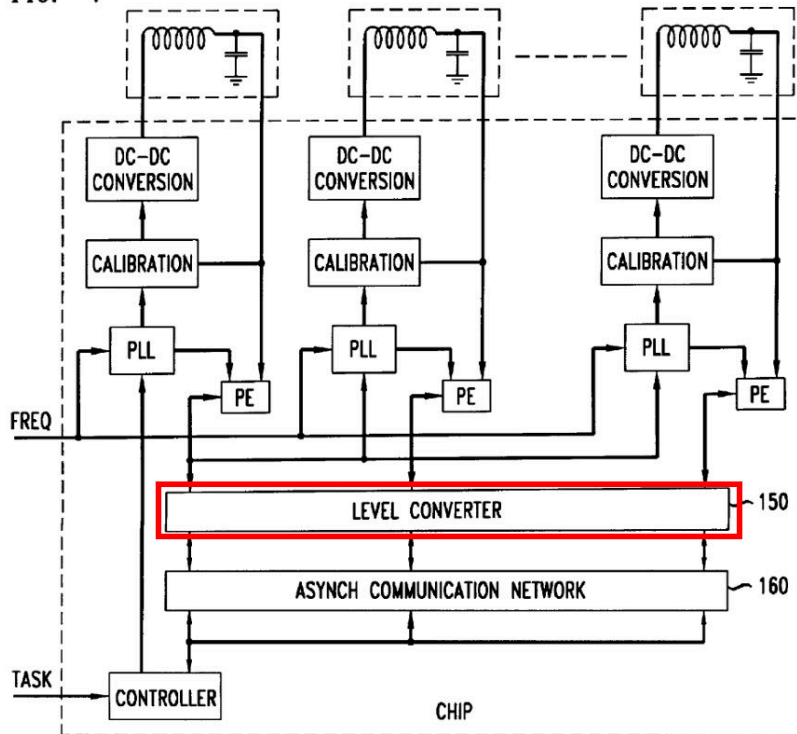
Nicol discloses and renders obvious Claim 36—e.g., by describing a “*level shifter*” or “level converter” that accounts for the different voltage levels provided in the system. EX1008, 5:49-52, 6:29-32, 7:9-11, Figs. 2, 4; EX1003, ¶¶285-286.

FIG. 2



EX1008, Fig. 2.

FIG. 4



EX1008, Fig. 4.

24. Claim 37

(a) Element_37[p]

Ground 2A, Element_1[p]. Nicol’s power management techniques can be implemented by an operating system (*software product*). EX1008, 2:53-56, 3:10-21, 3:66-4:16, 4:38-53, 5:23-29, 5:66-6:13; EX1003, ¶¶287-288.

(b) Element_37[a]

Ground 2A, Elements_1[a]-[c], 37[p]. As discussed, Nicol discloses an operating system that implements power management techniques (*power management software*) and is “*executed* on” a processing element (*processor*). EX1008, 2:50-54, 4:11-13, 6:2-13; EX1003, ¶289.

(c) Element_37[b]

It would have been apparent or obvious to a POSITA that an operating system like the one Nicol discloses (*power management software*) is typically *stored*—for short or long time periods—in computer memory (*software storage medium*). As one example, Nicol teaches that each PE “contains a central processing unit (CPU) and a local cache memory” and that the “real-time operating system resides in PE 100.” EX1008, 2:50-56, 3:10-21, 3:66-4:5, 6:6-13; EX1003, ¶290.

25. Claim 38

Ground 2A, Claim 2. EX1003, ¶291.

26. Claim 39

Ground 2A, Claim 3. EX1003, ¶292.

27. Claim 40

Ground 2A, Claim 4. EX1003, ¶293.

28. Claim 41

Ground 2A, Claim 5. EX1003, ¶294.

29. Claim 42

Ground 2A, Claim 6. EX1003, ¶295.

30. Claim 43

Ground 2A, Claim 7. EX1003, ¶296.

31. Claim 44

Ground 2A, Claim 8. EX1003, ¶297.

32. Claim 45

Ground 2A, Claim 9. EX1003, ¶298.

33. Claim 47

Ground 2A, Claim 11. EX1003, ¶299.

F. GROUND 2B—Claims 6, 10, 12, 14-15, 21, 25, 27, 29-30, 34, 46, 48, 50-51 are obvious over Nicol and Nowka

1. Nicol-Nowka Combination

A POSITA would have been motivated to incorporate the teachings of Nowka into Nicol's disclosure with a reasonable expectation of success. EX1003, ¶¶300-306. Nicol and Nowka are in the same field of endeavor: power management on an integrated circuit. EX1008, 2:18-22; EX1004, 1441; EX1003, ¶303; *supra* §III.A.1

(Nowka summary), §III.E.1 (Nicol summary). Further, Nicol and Nowka address the same known problem, the need to balance performance with power consumption in electronic systems. EX1005, 1:24-30, EX1004, 1441; EX1003, ¶303. Both teach dynamically varying parameters like frequency and voltage to control the power consumption, which was well known and predictable at the time of the '306 patent. EX1008, 2:11-14, 3:24-27; EX1004, 1442, 1444; EX1003, ¶304.

Because Nicol and Nowka provide similar solutions to a similar problem within the same field of endeavor, and because Nowka describes a physical implementation of a power-management scheme similar to Nicol's, a POSITA would have naturally looked at, and been motivated to combine, the two references when contemplating ways to bolster Nicol. EX1003, ¶305. For example, a POSITA would have been motivated to incorporate Nowka's standby modes in Nicol because such modes were known to provide the benefit/advantage of reducing unnecessary power consumption. EX1008, 3:4-7 ("[T]ypically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption."); EX1004, 1446; EX1003, ¶305.

Similarly, a POSITA would have been motivated to incorporate Nowka's PLL circuitry in Nicol's PLL to improve the resolution of the varying frequency, and to allow for glitchless frequency switching, clock freezing for hibernation modes, and

selecting alternative clock sources for extremely low-frequency operation. EX1008, 4:17-22; EX1004, 1444; EX1003, ¶306.

2. Claim 6

The Nicol-Nowka combination renders obvious Claim 6. Nowka discloses that the “output multiplexor can also *select* the real-time *clock*, reference *clock*, or an auxiliary *clock* as the processor *clock* source to allow for extremely low frequency operation.” EX1004, 1444; EX1003, ¶307. A POSITA would have been motivated to implement such a clock-selecting technique in Nicol to enhance the ability to quickly switch between clock frequencies for a given PE or power island, and to allow for alternative clock sources for extremely low-frequency operation. EX1003, ¶308. This modification is simply the application of a known technique (clock selection) to improve a similar device (Nicol’s PLL) in the same way (to provide means for selecting various frequencies). EX1003, ¶308.

3. Claim 10

The Nicol-Nowka combination renders obvious Claim 10. For example, as discussed at Ground 1A (Claim 10), Nowka discloses standby “Hibernation” and “Cryo” modes where “the logic supply to the processor, caches and the SOC core is disconnected.” EX1004, 1446; *see also* 1442, 1445; EX1003, ¶¶309-310. When exiting Hibernation/Cryo mode and “reactivating the system” upon a “wakeup

event,” the SOC “restores the [logic] supply” to *power on the power island(s)*. EX1004, 1446; EX1003, ¶310.

As discussed (*supra* §III.F.2), a POSITA would have been motivated to incorporate Nowka’s standby modes into Nicol, and with it, powering on a power island, to minimize unnecessary power consumption. EX1008, 2:8-10, 3:4-7; EX1003, ¶311. Further, Nicol discloses controlling operating voltages with “significantly greater than on/off granularity,” demonstrating that turning a component on and off was well-known and widely implemented in the art. EX1008, Abstract, 2:18-31; EX1003, ¶311.

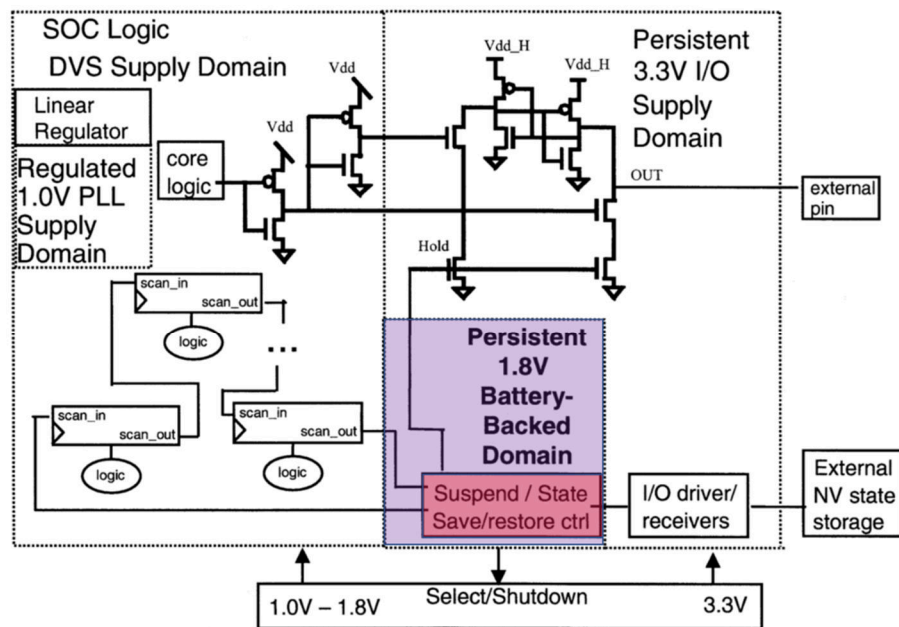
4. Claim 12

The Nicol-Nowka combination renders obvious Claim 12. Nowka discloses “*sleep* and hibernation *modes*” to “minimize standby power consumption,” similar to the ’306 patent’s “low power modes such as sleep, nap, and full power down.” EX1004, 1442, 1446; EX1001, 7:26-27; EX1003, ¶312; *supra* analysis at Ground 1A (Claim 12). As discussed (*supra* §III.F.2), a POSITA would have been motivated to incorporate Nowka’s standby modes in Nicol to “reduce the average power consumption” while PEs or groups of PEs (power islands in Nicol) are on standby, or not needed. EX1008, 3:4-7; EX1003, ¶313. Such modes were a well-known solution in the art, and incorporation into Nicol would have been no more

than a combination of familiar elements according to known methods to yield predictable results (minimize leakage and power consumption). EX1003, ¶314.

5. Claim 14

The Nicol-Nowka combination renders obvious Claim 14. For example, Nowka discloses that in “Cryo mode,” “the state of latches and register arrays in the processor core and SOC cores is transferred to nonvolatile storage prior to disconnecting the logic supply” EX1004, 1446. Therefore, Nowka discloses *saving the state* of the latches and register arrays, which are components in the logic domain. EX1003, ¶315. Additionally, Figure 3 shows a block labeled “*Save/restore ctrl*” within the variable voltage power domain (*power island*), which a POSITA would have understood to facilitate *saving a state of components*. EX1003, ¶316.



EX1004, Fig. 3.

A POSITA would have been motivated to incorporate Nowka's state-saving mechanism in Nicol because such a solution allows for efficient restoration of the component state after the power island (PE or group of PEs) have been in standby mode. EX1003, ¶317; *see also supra* §III.F.2 (motivation-to-combine regarding power management standby modes).

6. Claim 15

The Nicol-Nowka combination renders obvious Claim 15. For example, Nowka teaches that, after entering "Cryo mode," the suspend controller "waits for a wakeup event at which time it restores the supply, *restores the state* and restarts the clocks" for components in the variable voltage power domain (*power island*). EX1004, 1446. In incorporating Nowka into Nicol, a POSITA would have been motivated to allow the system to restore a state of systems (*i.e.*, of the PE or group of PEs that was placed in standby mode). EX1003, ¶¶318-319. Such a technique was known to improve wake-up time and, thus, improve energy efficiency and performance. EX1003, ¶319; *see also supra* §III.F.2 (motivation-to-combine regarding power management standby modes).

7. Claim 21

Ground 2B, Claim 6. EX1003, ¶320.

8. Claim 25

Ground 2B, Claim 10. EX1003, ¶321.

9. Claim 27

Ground 2B, Claim 12. EX1003, ¶322.

10. Claim 29

Ground 2B, Claim 14. EX1003, ¶323.

11. Claim 30

Ground 2B, Claim 15. EX1003, ¶324.

12. Claim 34

The Nicol-Nowka combination renders obvious Claim 34. For example, as discussed at Ground 1A (Claim 34), Nowka discloses that the PLL (*power control circuitry*, per Element_16[a] of both Ground 1A and Ground 2A) includes an “output *multiplexor*” in its PLL that “allows for *clock* freezing for sleep and hibernation modes. The output multiplexor can also select the real-time *clock*, reference *clock*, or an auxiliary *clock*.” EX1004, 1444; EX1003, ¶325.

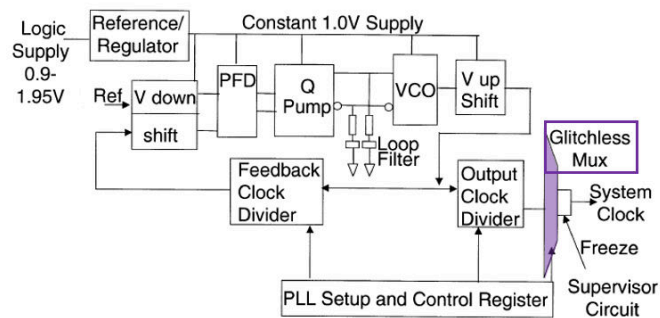


Fig. 7. Low-voltage on-the-fly frequency scalable PLL.

EX1004, Fig. 7.

As discussed (*supra* §III.F.2), a POSITA would have found it obvious to incorporate clock multiplexing circuitry into Nicol’s PLL to allow for seamless

selection of frequency in Nicol’s dynamic frequency scaling, as well as to allow for selecting from alternative clock sources. EX1008, 4:17-27, Figs. 2, 4; EX1003, ¶326. Multiplexing was conventional and well-known in the art, and this circuitry would have required only the application of routine engineering skills and design principles to implement. EX1003, ¶326.

13. Claim 46

Ground 2B, Claim 10. EX1003, ¶327.

14. Claim 48

Ground 2B, Claim 12. EX1003, ¶328.

15. Claim 50

Ground 2B, Claim 14. EX1003, ¶329.

16. Claim 51

Ground 2B, Claim 15. EX1003, ¶330.

G. GROUND 2C—Claims 13, 28, and 49 are obvious over Nicol and Borkar

1. Nicol-Borkar Combination

A POSITA would have been motivated to incorporate the teachings of Borkar into Nicol’s disclosure with a reasonable expectation of success. EX1003, ¶¶331-337. Nicol and Borkar are in the same field of endeavor: power management on an integrated circuit. EX1003, ¶334. Nicol relates to “electronic circuits and, more particularly to power consumption within electronic circuits.” EX1008, Abstract,

1:6-7. Similarly, Borkar describes “control circuitry [that] controls a setting of a body bias signal...to at least partially control a parameter of the processor...Examples of the parameters include performance, power consumption, and temperature.” EX1006, 1:60-2:3. Further, Nicol and Borkar address the same known problem—the need to balance performance with power consumption in electronic systems. EX1008, 2:65-3:9, EX1006, 1:20-21, 5:45-46; EX1003, ¶335. Both Nicol and Borkar also suggest the solution of dynamically controlling variables such as frequency and voltage in response to changing needs and operations. EX1008, 4:64-66, 5:66-6:2; EX1006, 5:25-29, 2:52-54; EX1003, ¶336.

These similarities across Nicol and Borkar’s disclosures would have led a POSITA to incorporate Borkar’s teachings in Nicol’s dynamic power management. For example, Nicol discusses the need to adjust to temperature variations “to achieve high performance at varying operating temperatures and process corners,” and existing systems that “use[] an on-chip temperature sensor and associated processing circuitry” to respond to variations in temperature. EX1008, 1:41-48; *see also* 1:65-67. A POSITA would have understood that the discussion of temperature variation is closely related to the need to monitor power consumption because, as Borkar teaches, “performance, power consumption, and temperature are typically related.” EX1006, 1:19-20; EX1003, ¶337. A POSITA would have understood that Borkar’s power consumption monitoring mechanism would provide an additional check on

the adverse effects of high power consumption (which causes high temperature) on performance that Nicol discusses. EX1003, ¶¶337.

2. Claim 13

The Nicol-Borkar combination renders obvious Claim 13. EX1003, ¶¶338-343. As discussed at Ground 1C (Claim 13), Borkar discloses embodiments that explicitly show “current detection circuitry” providing current signals to “voltage and frequency control circuitry.” EX1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7. According to Borkar, “detect[ing] current being consumed” is a precise way of tracking power consumption levels. EX1006, 13:6-7; *see also* 4:64-67.

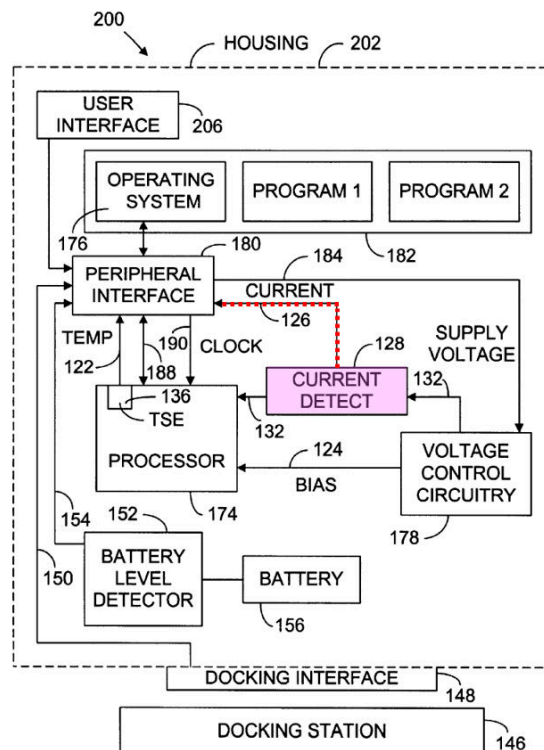


FIG. 4

EX1006, Fig. 4.

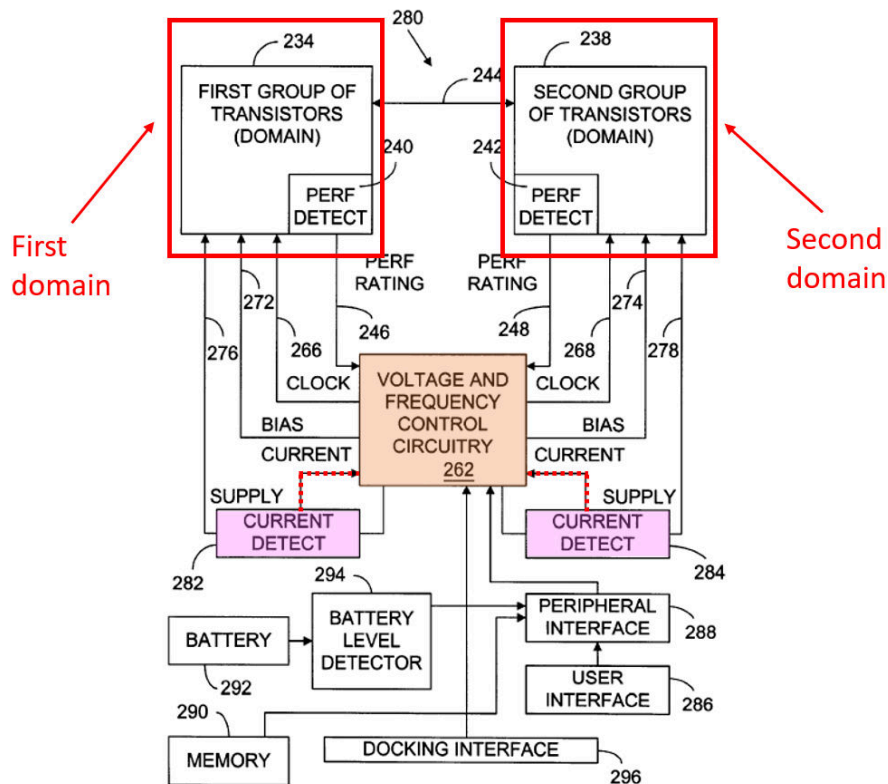


FIG. 7

EX1006, Fig. 7.

Because current multiplied by supply voltage is power consumption, Borkar's system can *monitor power consumption* by monitoring current signal. EX1006, 4:64-67, 13:7-8. As a POSITA would have understood, by calculating the power consumption in this way, the system can monitor the power consumption and *perform* appropriate *actions*, such as changing body bias, supply voltage, and clock frequencies, in the event the *power consumption* approaches or *crosses a threshold level*. EX1006, 6:1-7, 13:2-7; EX1003, ¶¶338-340.

As an additional basis to establish obviousness, Borkar teaches “control circuitry” that “*monitors* a temperature signal...related to the temperature of [a]

processor” (*power consumption level*). EX1006, 4:12-20; *see also* EX1001, 6:47-50 (explaining that “temperature” is an example of a “power consumption level[]”); EX1003, ¶342. According to Borkar, “if the temperature TACTUAL of [the] processor...exceeds an upper temperature limit THIGH” (*determining whether a threshold level was crossed*), the system responsively *performs* an appropriate *action*—e.g., “change[s] the body bias, supply voltage, and/or clock signal settings”—“to decrease temperature.” EX1006, 4:21-46.

A POSITA would have been motivated to implement Borkar’s power consumption monitoring in Nicol to achieve more precise and predictable power consumption control. Whereas Nicol changes operating parameters based primarily on the most efficient division of the application at hand, incorporating power monitoring from Borkar would allow Nicol’s system to further respond to excessive power consumption levels, similar to Nicol’s disclosure that “the operating system can reduce the supply voltage even further by tracking temperature and process variations.” EX1008, 4:11-13; EX1003, ¶341. Likewise, the POSITA would have been motivated to integrate Borkar’s temperature monitoring techniques with Nowka to provide the predictable benefit of preventing overheating. *E.g.*, EX1006, 1:11-56; EX1003, ¶342. The POSITA would have needed only routine electrical and computer engineering principles to implement Borkar’s monitoring and threshold-comparing mechanisms in Nicol, as demonstrated by Borkar’s

implementation in a system analogous to Nicol's integrated circuit. EX1006, 2:49-52; EX1003, ¶343.

3. Claim 28

Ground 2C, Claim 13. EX1003, ¶344.

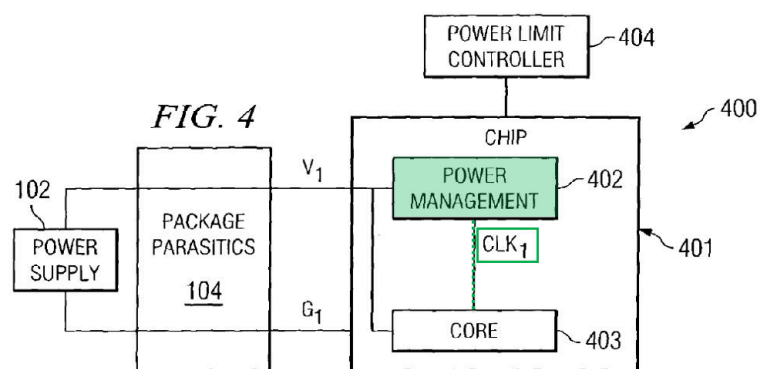
4. Claim 49

Ground 2C, Claim 13. EX1003, ¶345.

H. GROUND 2D—Claim 35 is obvious over Nicol and Naffziger

1. Overview of Naffziger

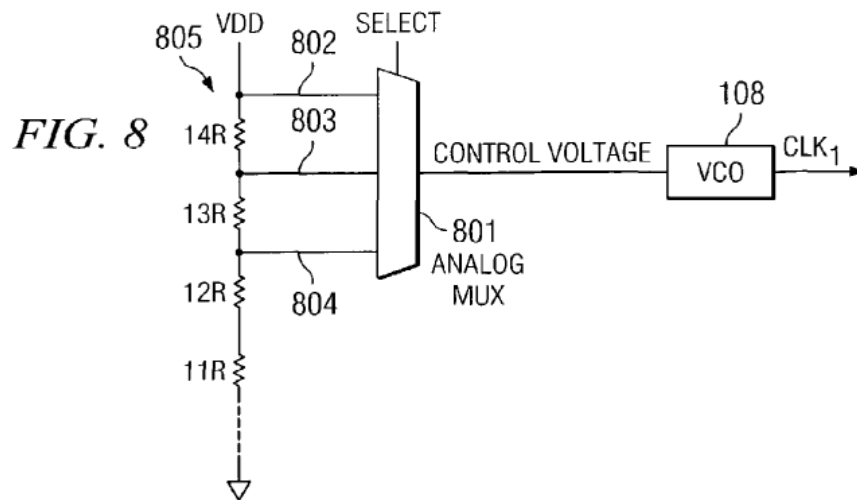
Naffziger relates to an integrated circuit with a dynamically variable power limit. EX1015, Abstract; EX1003, ¶¶346-348. Naffziger includes a “power management” logic for self-regulating power consumption. EX1015, 11:50-51; *see also* 5:32-36. The power management logic includes a voltage controlled frequency oscillator that generates a clock signal for the chip circuitry. EX1015, 11:52-61.



EX1015, Fig. 4.

Naffziger's power management logic further includes a voltage multiplexor in conjunction with a resistor divider to produce multiple voltages, which in turn

allows variable clock frequency output from the VCO. EX1015, 19:30-64. Figure 8 shows an example of resistor divider combined with a multiplexor to enable selecting from different control voltage levels.



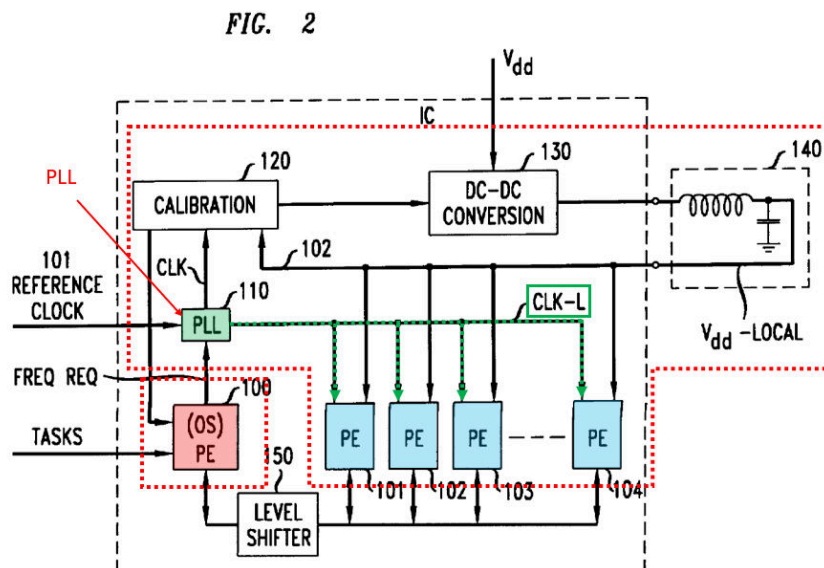
EX1007, Fig. 8.

2. Nicol-Naffziger Combination

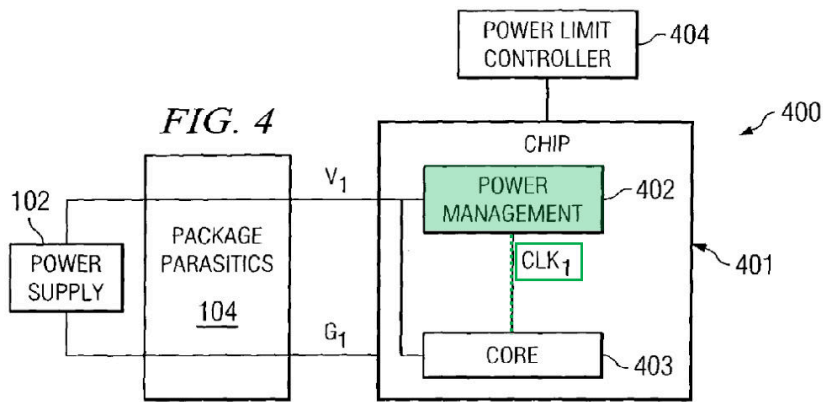
A POSITA would have been motivated to incorporate the teachings of Naffziger into Nicol's disclosure with a reasonable expectation of success. EX1003, ¶¶349-354. Nicol and Naffziger are in the same field of endeavor: power management on an integrated circuit. EX1008, 2:18-22; EX1015, 1:19-20; EX1003, ¶350. Nicol and Naffziger also address the same known problem: the need to balance performance with power consumption in electronic systems. EX1008, 2:65-3:9, 3:4-6; EX1015, 1:33-, 6:15-20; EX1003, ¶351. Both Nicol and Naffziger address that problem with the identified, predictable solution of dynamically

controlling the power in response to changing needs and operations. EX1008, 2:18-22; EX1015, 4:10-19, Fig. 3; EX1003, ¶352.

Nicol and Naffziger also both teach the concept of changing variable parameters such as frequency and voltage to change the power level. EX1008, 1:26-28, 2:11-14, 3:24-27; EX1015, 1:56-60, 6:49-51; EX1003, ¶353. To this end, Naffziger shows a “power management” block which outputs a clock to the core. EX1015, 11:50-53. A POSITA would have recognized that this “power management” block is performing the same function as the PLL in Nicol, which outputs a clock frequency to the PEs. EX1003, ¶353. Thus, a POSITA would have naturally sought to bolster Nicol’s teachings with the additional circuitry details Naffziger provides. EX1003, ¶¶353-354.



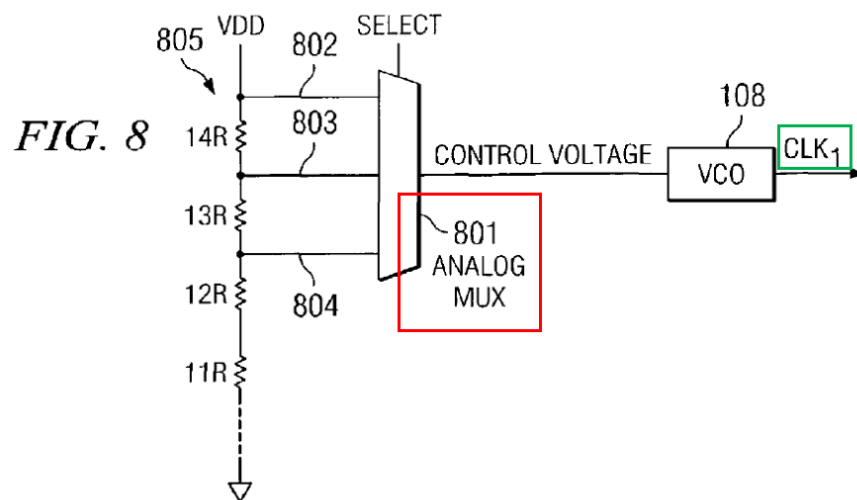
EX1008, Fig. 2.



EX1015, Fig. 4.

3. Claim 35

The Nicol-Naffziger combination renders obvious Claim 35. For example, Naffziger discloses a *voltage multiplexor* that allows choosing between various voltage levels for its voltage-controlled oscillator (VCO). EX1015, 19:43-62, Fig. 8; EX1003, ¶355. Changing the control voltage for the VCO in turn changes the frequency of clock signal CLK₁. *Id.*



EX1007, Fig. 8.

A POSITA would have been motivated to integrate Naffziger's multiplexer teachings in Nicol to provide an efficient method for adaptively changing the voltage input to the VCO, which in turn allows for varying the clock signal frequency. EX1003 ¶356.

IV. PAYMENT OF FEES

Petitioner authorizes charge of fees to Deposit Account 06-1050.

V. MANDATORY NOTICES UNDER 37 C.F.R. §42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. §42.8(b)(1)

Infineon Technologies Americas Corp. is the Petitioner, and Infineon Technologies AG is a real party-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

B. Related Matters Under 37 C.F.R. §42.8(b)(2)

Petitioner is not aware of any pertinent disclaimers or reexamination certificates. MOSAID Technologies, Inc.—the alleged Patent Owner—filed a complaint asserting the '306 patent against Petitioner on March 10, 2025 in the U.S. District Court for the Western District of Texas (Civil Action No. 1:25-cv-00358).

The '306 patent was asserted in six other district court infringement actions (*Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case No. 6:11-cv-00173 (Apr. 7, 2011, E.D. Tex.); *Conversant Intellectual Property Management Inc. v. STMicroelectronics, Inc.*, Case No. 6:12-cv-00848 (Nov. 5, 2012) (E.D. Tex.);

MOSAID Technologies Inc. v. Xilinx, Inc., Case. No. 6:12-cv-00847 (Nov. 5, 2012, E.D. Tex.); *MOSAID Technologies Inc. v. NXP Semiconductors USA, Inc.*, Case. No. 6:12-cv-00846 (Nov. 5, 2012, E.D. Tex.); *MOSAID Technologies Inc. v. ST-Ericsson, Inc.*, Case. No. 6:12-cv-00845 (Nov. 5, 2012, E.D. Tex.); *MOSAID Technologies Inc. v. MediaTek*, Case No. 2:23-cv-00129 (E.D. Tex. Mar. 28, 2023)) and subject to one declaratory judgment action (*ARM Ltd. v. MOSAID Technologies, Inc.*, Case No. 3:11-cv-03869 (Aug. 5, 2011, N.D. Cal.), transferred to *ARM Ltd. v. MOSAID Technologies, Inc.*, Case No. 6:12-cv-00008 (Jan. 9, 2012, E.D. Tex), which were all voluntarily dismissed based on settlement.

The '306 patent was previously challenged in Case No. IPR2024-00598. The Board granted institution on September 26, 2024 (Paper 12) and terminated the proceeding due to settlement on December 31, 2024 (Paper 19).

C. Lead And Back-Up Counsel Under 37 C.F.R. §42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
Kenneth Wayne Darby Jr., Reg. No. 65,068 Fish & Richardson P.C. 60 South Sixth Street Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR60246-0006IP1@fr.com	David M. Hoffman, Reg. No. 54,174 Fish & Richardson P.C. 60 South Sixth Street Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR60246-0006IP1@fr.com

D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR60246-0006IP1@fr.com.

Respectfully submitted,

Dated: June 20, 2025

/Kenneth Wayne Darby Jr./
Kenneth Wayne Darby Jr., Reg. No. 65,068
Fish & Richardson P.C.
60 South Sixth Street
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

(Control No. IPR2025-01171)

Attorney for Petitioner

CERTIFICATION UNDER 37 CFR §42.24

Under the provisions of 37 CFR §42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,904 words, which is less than the 14,000 allowed under 37 CFR §42.24.

Dated: June 20, 2025

/Kenneth Wayne Darby Jr./
Kenneth Wayne Darby Jr., Reg. No. 65,068
Fish & Richardson P.C.
60 South Sixth Street
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

Attorney for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on June 20, 2025 a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
55 Old Bedford Rd., Suite 200
LINCOLN, MA 01773
(978) 341-0036

/Crena Pacheco/
Crena Pacheco
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
pacheco@fr.com