

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INFINEON TECHNOLOGIES AMERICAS CORP.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

Case IPR2025-01171
Patent 7,051,306

PETITIONER'S UPDATED LIST OF EXHIBITS

UPDATED LIST OF EXHIBITS

EX1001	U.S. Patent No. 7,051,306 to Hoberman et al. (“the ’306 patent”)
EX1002	Excerpts from the Prosecution History of the ’306 patent
EX1003	Declaration of Tajana Rosing, Ph.D.
EX1004	“A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling” by Nowka, et al. (“Nowka”)
EX1005	Declaration of June Ann Munford
EX1006	U.S. Patent No. 6,484,265 to Borkar et al. (“Borkar”)
EX1007	U.S. Patent No. 6,353,369 to Boerstler (“Boerstler”)
EX1008	U.S. Patent No. 6,141,762 to Nicol, et al. (“Nicol”)
EX1009	RESERVED
EX1010	RESERVED
EX1011	Claim Construction Order in <i>MOSAID Technologies Inc. v. Freescale Semiconductor, Inc.</i> , Case No. 6:11-cv-00173 (E.D. Tex. April 29, 2013)
EX1012	Claim Construction Order in <i>Conversant Intellectual Property Management Inc., et al. v. Xilinx, Inc.</i> , Case No. 6:12-cv-00847 (E.D. Tex. January 9, 2015)
EX1013	Claim Construction Order in <i>MOSAID Technologies Inc. v. MediaTek</i> , Case No. 2:23-cv-00129 (E.D. Tex. July 31, 2024)
EX1014	RESERVED
EX1015	U.S. Patent No. 8,086,884 to Naffziger et al. (“Naffziger”)

- EX1016 “Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design” by Kuroda et al. (“Kuroda”)
- EX1017 “Dynamic Power Management: Design Techniques and CAD Tools” by Benini & De Micheli (“Dynamic Power Management”)
- EX1018 “A Survey of Design Techniques for System-Level Dynamic Power Management” by Benini, et al. (“Benini Survey”)
- EX1019 “Managing Power and Performance for System-on-Chip Designs using Voltage Islands” by Lackey, et al. (“Lackey”)
- EX1020 “Policy Optimization for Dynamic Power Management” by Benini et al., (“Benini Policy Optimization”)
- EX1021 “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling” by Semeraro et al. (“Semeraro”)
- EX1022 “Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems” by Dutta et al. (“Dutta”)
- EX1023 “The CoreConnect™ Bus Architecture” by IBM (“CoreConnect White Paper”)
- EX1024 “The Computer Engineering Handbook” edited by Oklobdzija (“Computer Engineering Handbook”), excerpts
- EX1025 “Computer Systems: Concepts and Design” by Gibson (“Gibson”), excerpts
- EX1026 Multimedia Information Networking” by Sharda (“Sharda”), excerpts
- EX1027 U.S. Patent No. 6,345,362 to Bertin et al. (“Bertin”)
- EX1028 “PowerPC 603 Microprocessor: Power Management” by Suessmith (“Suessmith”)

- EX1029 IEEE Journal of Solid-State Circuits, IEEE Xplore,
<https://ieeexplore.ieee.org/xpl/aboutJournal.jsp?punumber=4>
(accessed June 16, 2025)
- EX1030 Excerpts from Document Landing Page for “A 32-bit PowerPC
system-on-a-chip with support for dynamic voltage scaling and
dynamic frequency scaling,” IEEE Xplore,
<https://ieeexplore.ieee.org/document/1046086/citations#citations>,
<https://ieeexplore.ieee.org/document/1046086/citations?tabFilter=pateents#citations> (accessed June 16, 2025)
- EX1031 IEEE History, <https://www.ieee.org/about/ieee-history> (accessed
June 16, 2025)
- EX1032 IPR2024-00598, Paper 12, Institution Decision (Sep. 26, 2024)
- EX1033 July 25, 2025 Stipulation

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on July 25, 2025, a complete and entire copy of this Petitioner's Updated List of Exhibits and EX1033 were provided via email, to the Patent Owner by serving the email correspondence addresses of record as follows:

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