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STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: MONTEREY RESEARCH, LLCApplication No./Patent No.: 12/577,477 Filed/Issue Date: 10-12-2009Titled: CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTERMONTEREY RESEARCH, LLC, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: LI, GABRIEL To: CYPRESS SEMICONDUCTOR CORPORATIONThe document was recorded in the United States Patent and Trademark Office at
Reel 045731, Frame 0856, or for which a copy thereof is attached.2. From: CYPRESS SEMICONDUCTOR CORPORATION SPANSION LLC To: MORGAN STANLEY SENIOR FUNDING, INC.The document was recorded in the United States Patent and Trademark Office at
Reel 035240, Frame 0429, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

MOSAID Technologies Inc., Exhibit 2023

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IPR2025-01171, Infineon Technologies Americas Corp. v. MOSAID Technologies Inc.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: CYPRESS SEMICONDUCTOR CORPORATION SPANSION LLC To: MORGAN STANLEY SENIOR FUNDING, INC.

The document was recorded in the United States Patent and Trademark Office at
Reel 058002, Frame 0470, or for which a copy thereof is attached.

4. From: MORGAN STANLEY SENIOR FUNDING, INC. To: CYPRESS SEMICONDUCTOR CORPORATION

The document was recorded in the United States Patent and Trademark Office at
Reel 046923, Frame 0491, or for which a copy thereof is attached.

5. From: CYPRESS SEMICONDUCTOR CORPORATION To: MONTEREY RESEARCH, LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 046947, Frame 0460, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Michael Bartholomew/

2022-03-11

Signature

Date

Michael Bartholomew

60225

Printed or Typed Name

Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	45210548
Application Number:	12577477
International Application Number:	
Confirmation Number:	4345
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
First Named Inventor/Applicant Name:	Gabriel Li
Customer Number:	60909
Filer:	Michael Lee Bartholomew/Mary Keshishian
Filer Authorized By:	Michael Lee Bartholomew
Attorney Docket Number:	3693.2.51V
Receipt Date:	11-MAR-2022
Filing Date:	12-OCT-2009
Time Stamp:	19:44:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	Statement373.pdf	123161	no	3
			796ef068376f289eecb437fc7f1070f9fcd9e72		

Warnings:

MOSAID Technologies Inc., Exhibit 2023

Page 2023 - 4

Information:	
Total Files Size (in bytes):	123161
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/577,477	10/12/2009	Gabriel Li	3693.2.51V

60909
Cypress Semiconductor Corporation
Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134

CONFIRMATION NO. 4345
IMPROPER CPOA LETTER



Date Mailed: 02/22/2022

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the power of attorney filed 02/11/2022. The power of attorney in this application is not accepted for the reason(s) listed below:

- The power of attorney is from an assignee and the statement required by 37 CFR 3.73(c) has not been received.

/cvorachack/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

36491
Kunzler Bean & Adamson
50 W. Broadway
Suite 1000
Salt Lake City, UT 84101
UNITED STATES

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	12/577,477
Filing Date	10-12-2009
First Named Inventor	Gabriel Li
Title	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
Art Unit	2819
Examiner Name	CRAWFORD, JASON
Attorney Docket Number	3693.2.51V

SIGNATURE of Applicant or Patent Practitioner

Signature	/Michael L. Bartholomew/	Date (Optional)	
Name	Michael L. Bartholomew	Registration Number	60225
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Monterey Research, LLC		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐

*Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

36491

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number

OR



The address associated with Customer Number:

OR

Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Monterey Research, LLC



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

9/12/2016

Name

Keith Wilson

Title

SVP Legal - Monterey Research, LLC

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.



Total of

forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1460, Alexandria, VA 22313-1460.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	44980277
Application Number:	12577477
International Application Number:	
Confirmation Number:	4345
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
First Named Inventor/Applicant Name:	Gabriel Li
Customer Number:	60909
Filer:	Michael Lee Bartholomew/Mary Keshishian
Filer Authorized By:	Michael Lee Bartholomew
Attorney Docket Number:	CD05110C1
Receipt Date:	11-FEB-2022
Filing Date:	12-OCT-2009
Time Stamp:	17:10:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA_3693_2_51V.pdf	454854	no	2
			c958c032e3402b33bb4cea3e653fd03a523b7c52		

Warnings:

MOSAID Technologies Inc., Exhibit 2023

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Information:	
Total Files Size (in bytes):	454854
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 621-cv-936	DATE FILED 9/10/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF MONTEREY RESEARCH, LLC		DEFENDANT QUALCOMM INCORPORATED, QUALCOMM TECHNOLOGIES, INC. and QUALCOMM CDMA TECHNOLOGIES ASIA-PACIFIC PTE LTD.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,979,640	12/27/2005	MONTEREY RESEARCH, LLC
2 7,609,799	10/27/2009	MONTEREY RESEARCH, LLC
3 7,899,145	3/11/2005	MONTEREY RESEARCH, LLC
4 8,694,776	4/8/2014	MONTEREY RESEARCH, LLC
5 9,767,303	9/19/2017	MONTEREY RESEARCH, LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

MOSAID Technologies Inc., Exhibit 2023

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IPR2025-01171, Infineon Technologies Americas Corp. v. MOSAID Technologies Inc.

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 6:21-cv-936	DATE FILED 9/10/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF MONTEREY RESEARCH, LLC		DEFENDANT QUALCOMM INCORPORATED, QUALCOMM TECHNOLOGIES, INC. and QUALCOMM CDMA TECHNOLOGIES ASIA-PACIFIC PTE LTD.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,405,987	7/29/2008	MONTEREY RESEARCH, LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

MOSAID Technologies Inc., Exhibit 2023

Page 2023 - 12

IPR2025-01171, Infineon Technologies Americas Corp. v. MOSAID Technologies Inc.

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:21-cv-839	DATE FILED 8/12/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF MONTEREY RESEARCH, LLC		DEFENDANT ADVANCED MICRO DEVICES, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,979,640	12/27/2005	MONTEREY RESEARCH, LLC
2 7,609,799	10/27/2009	MONTEREY RESEARCH, LLC
3 7,899,145	3/11/2005	MONTEREY RESEARCH, LLC
4 8,694,776	4/8/2014	MONTEREY RESEARCH, LLC
5 9,767,303	9/19/2017	MONTEREY RESEARCH, LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

MOSAID Technologies Inc., Exhibit 2023

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IPR2025-01171, Infineon Technologies Americas Corp. v. MOSAID Technologies Inc.

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:21-cv-839	DATE FILED 8/12/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF MONTEREY RESEARCH, LLC		DEFENDANT ADVANCED MICRO DEVICES, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 8,572,297	10/29/2013	MONTEREY RESEARCH, LLC
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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3		
4		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

MOSAID Technologies Inc., Exhibit 2023

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IPR2025-01171, Infineon Technologies Americas Corp. v. MOSAID Technologies Inc.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/577,477	03/01/2011	7899145	CD05110C1	4345

60909 7590 02/09/2011
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Gabriel Li, San Francisco, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 10/20/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/577,477	10/12/2009	Gabriel Li	CD05110C	4345

TITLE OF INVENTION: CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	01/20/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JASON	2819	375-376000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Cypress Semiconductor Corporation

San Jose, CA.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3781 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☒ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date 1/19/11

Typed or printed name Larry J. Johnson

Registration No. 56,861

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		12577477		
Filing Date:		12-Oct-2009		
Title of Invention:		CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER		
First Named Inventor/Applicant Name:		Gabriel Li		
Filer:		Larry Joel Johnson/Hilary Link		
Attorney Docket Number:		CD05110C1		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300
		MOSAID Technologies Inc., Exhibit 2023		

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt

EFS ID:	9275771
Application Number:	12577477
International Application Number:	
Confirmation Number:	4345
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
First Named Inventor/Applicant Name:	Gabriel Li
Customer Number:	60909
Filer:	Larry Joel Johnson/Hilary Link
Filer Authorized By:	Larry Joel Johnson
Attorney Docket Number:	CD05110C1
Receipt Date:	20-JAN-2011
Filing Date:	12-OCT-2009
Time Stamp:	20:01:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1810
RAM confirmation Number	6930
Deposit Account	503781
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

MOSAID Technologies Inc., Exhibit 2023

Page 2023 - 19

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	CD05110C1_TransmittalLetter_01202011.pdf	281393 1e07b3e7a18fa11bdbeab36365bb16c5ba b58ffd	no	2

Warnings:

Information:

2	Issue Fee Payment (PTO-85B)	CD05110C1_IssueFeePage_01202011.pdf	533470 508c2e8a2429bf864c39d055e1939f45af3a 2397	no	1
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Warnings:

Information:

3	Fee Worksheet (PTO-875)	fee-info.pdf	32053 e1c1fdbc05b413f541fed48465a640a535aa a70d	no	2
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Warnings:

Information:

Total Files Size (in bytes):			846916		
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Examiner: JASON CRAWORD
	)	
Gabriel Li	)	Group Art Unit: 2819
	)	
Application No.: 12/577,477	)	Confirmation No.: 4345
	)	
Filed: October 12, 2009	)	
	)	
For: CIRCUIT, SYSTEM, AND METHOD	)	
FOR MULTIPLEXING SIGNALS	)	
WITH REDUCED JITTER	)	

ISSUE FEE TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant is in receipt of a Notice of Allowance and Fee Due Form, mailed October 20, 2010 in connection with the above-identified application. The Issue Fee is due on or before January 20, 2011. Applicant hereby submits the Issue Fee and/or the Publication Fee.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.19, 1.20 and 1.21 that may be required to issue the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

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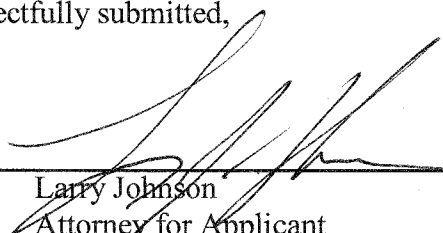
/

Customer No.: 60909

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

Dated: 1/19/11

By: 

Larry Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

Customer No.: 60909



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60909 7590 10/20/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER

CRAWFORD, JASON

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 10/20/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/577,477

10/12/2009

Gabriel Li

CD05110C

4345

TITLE OF INVENTION: CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	01/20/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60909 7590 10/20/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/577,477 10/12/2009 Gabriel Li CD05110C 4345

TITLE OF INVENTION: CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	01/20/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JASON	2819	375-376000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

MOSAID Technologies Inc., Exhibit 2023



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/577,477	10/12/2009	Gabriel Li	CD05110C	4345
60909	7590	10/20/2010	EXAMINER	
CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709			CRAWFORD, JASON	
			ART UNIT	PAPER NUMBER
			2819	
DATE MAILED: 10/20/2010				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	12/577,477	LI, GABRIEL	
	Examiner	Art Unit	
	Jason M. Crawford	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/4/2010.
2. ☒ The allowed claim(s) is/are 3-6,8-22.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. ☒ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>10/12/09,10/4/10</u> 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material | <ol style="list-style-type: none"> 5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other ____. |
|---|--|

/Jason M. Crawford/
Examiner, Art Unit 2819

DETAILED ACTION

Terminal Disclaimer

The terminal disclaimer filed on 6/4/2010 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,609,799 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Miscellaneous

The Applicant has cancelled claims 1-2 and 7, and added new claims 21-22; therefore only claims 3-6 and 8-22 remain for this Office Action.

Allowable Subject Matter

Claims 3-6 and 8-22 are allowed. The following is an examiner's statement of reasons for allowance:

In regards to claim 3, the prior art discloses of an apparatus, comprising: a plurality of power supply domains; and a plurality of logic components, each of the plurality of logic components within a different one of the plurality of power supply domains, wherein each of the plurality of logic components is configured to operate with a corresponding clock signal within a respective one of the plurality of power supply domains, however, the prior art does not disclose of wherein the plurality of power supply domains comprises first, second, third and fourth power supply domains, wherein a plurality of logic components comprises: a first logic gate arranged within the

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first power supply domain and configured to operate with a first clock signal; a second logic gate arranged within the second power supply domain and configured to operate with a second clock signal; a first logic block arranged within the third power supply domain and coupled to the first and second logic gates; and a second logic block arranged within the fourth power supply domain and coupled to the first and second logic gates, nor would it have been obvious to one of ordinary skill in the art to do so.

Claims 4-6, 8-11 and 21 are also allowed as being dependent on claim 3.

In regards to claim 12, the prior art does not disclose of a system, comprising: a circuit comprising two logic gates and a first logic block and a second logic block, each arranged within a separate power supply domain, wherein: a first of the two logic gates is operatively coupled with a first signal; a second of the two logic gates is operatively coupled with a second signal; and a second logic block operatively coupled with one of the first and second signals, depending on a state of a control signal; and a system component coupled to the second logic block, nor would it have been obvious to one of ordinary skill in the art to do so. Claims 13-17 and 22 are also allowed as being dependent on claim 12.

In regards to claim 18, the prior art does not disclose of a method, comprising: deactivating one of a first signal or a second signal by supplying a control signal to first and second logic gates; and forwarding an active one of the first or second signals to a third logic gate, wherein the first, second and third logic gates are spaced apart from one another and respectively arranged within a first, second and third power

Art Unit: 2819

supply domain, nor would it have been obvious to one of ordinary skill in the art to do so. Claims 19 and 20 are also allowed as being dependent on claim 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON CRAWFORD whose telephone number is (571)272-6004. The examiner can normally be reached on Mon-Fri 7:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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Page 5

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/James H. Cho/
Primary Examiner, Art Unit 2819

/Jason M. Crawford/
Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 12/577,477		Applicant(s)/Patent Under Reexamination LI, GABRIEL	
	Examiner Jason M. Crawford		Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0268278	12-2004	Hoberman et al.	716/005
*	B	US-5,991,135	11-1999	Saleh, Farid	361/56
*	C	US-7,030,661	04-2006	Doyle, James Thomas	327/102
*	D	US-2006/0165205	07-2006	Dally, William J.	375/371
*	E	US-2002/0089362	07-2002	Lutkemeyer, Christian A.J.	327/161
*	F	US-7,365,580	04-2008	Martin et al.	327/156
*	G	US-7,231,009	06-2007	Kim et al.	375/354
*	H	US-7,079,575	07-2006	Ho et al.	375/232
*	I	US-6,154,509	11-2000	Bishop, Wendell	375/371
*	J	US-6,292,016	09-2001	Jefferson et al.	326/39
*	K	US-6,927,604	08-2005	Boerstler et al.	326/93
*	L	US-7,042,263	05-2006	Johnson et al.	327/199
*	M	US-7,305,646	12-2007	McGrath et al.	716/12

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Search Notes 	Application/Control No. 12577477	Applicant(s)/Patent Under Reexamination LI, GABRIEL
	Examiner JASON CRAWFORD	Art Unit 2819

SEARCHED			
Class	Subclass	Date	Examiner
327	99,147,407-408	10/7/2010	JC
375	371,376	10/7/2010	JC
713	400-401,500-503,600-601	10/7/2010	JC
326	21-22,29	10/7/2010	JC

SEARCH NOTES		
Search Notes	Date	Examiner
See attached search	10/7/2010	JC

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
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CONFIRMATION NO. 4345

SERIAL NUMBER 12/577,477	FILING or 371(c) DATE 10/12/2009 RULE	CLASS 375	GROUP ART UNIT 2819	ATTORNEY DOCKET NO. CD05110C		
APPLICANTS Gabriel Li, San Francisco, CA; ** CONTINUING DATA ***** This application is a CON of 11/468,195 08/29/2006 PAT 7,609,799 JC which claims benefit of 60/713,682 09/02/2005 JC ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/22/2009						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JASON CRAWFORD/</u> Examiner's Signature		☐ Met after Allowance JC Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 5	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709 UNITED STATES						
TITLE CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

<i>Index of Claims</i> 	Application/Control No. 12577477	Applicant(s)/Patent Under Reexamination LI, GABRIEL
	Examiner JASON CRAWFORD	Art Unit 2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☒ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	03/08/2010	06/17/2010	10/07/2010					
-	1	✓	-	-					
-	2	✓	-	-					
1	3	O	=	=					
2	4	O	=	=					
3	5	O	=	=					
4	6	✓	=	=					
-	7	✓	-	-					
5	8	✓	=	=					
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8	11	✓	=	=					
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18	19	✓	=	=					
19	20	✓	=	=					
9	21		=	=					
16	22		=	=					

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L9	141	(PLL DLL ((phase delay) adj lock\$3 adj loop)) and L8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:41
L10	141	L9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:41
L11	141	L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:41
L12	500	(pll (phase adj lock\$3 adj loop\$3)) and ((power supply voltage) adj (domain island))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:42
L13	303	L12 and @ad<"20050902"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:42
L14	233	L13 not silverbrook.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:42
L15	159	L14 not print\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:42

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L17	52	L15 not L16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:42
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L19	52	L18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:42
L20	15902	326/21-22,29.ccls. 327/99,147,407-408.ccls. 375/371,376.ccls. 713/400-401,500-503,600- 601.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/10/07 13:42
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EAST Search History (Interference)

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file:///C:/Documents%20and%20Settings/jcrawford/My%20...7477/EASTIPR2025-01171717TheOneTechnologiesAmericaCorporation MOSAND Technologies Inc.

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Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

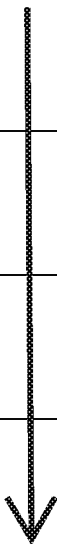
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	Filing Date		2009-10-12
	First Named Inventor	Gabriel Li	
	Art Unit	2819	
	Examiner Name	Jason Crawford	
	Attorney Docket Number	CD05110C	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
/JC/	1	7609799	B1	2009-10-27	Li, Gabriel	Entire Document	
	2	6502212	B1	2002-12-31	Coyle et al.	Entire Document	
	3	6775339	B1	2004-08-10	Wildes et al.	Entire Document	
	4	6137336	B1	2000-10-24	Baba et al.	Entire Document	
	5	6105144	B1	2000-08-15	Wu, Leon Li-Heng	Entire Document	
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	7	5731725	B1	1998-03-24	Rothenberger et al.	Entire Document	
	8	5982220	B1	1999-11-09	Kim	Entire Document	

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	Filing Date		2009-10-12			
	First Named Inventor		Gabriel Li			
	Art Unit		2819			
	Examiner Name		Jason Crawford			
	Attorney Docket Number		CD05110C			

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	12	5352987	B1	1994-10-04	Harvey	Entire Document
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	Filing Date		2009-10-12	
	First Named Inventor	Gabriel Li		
	Art Unit	2819		
	Examiner Name	Jason Crawford		
	Attorney Docket Number	CD05110C		

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	3	USPTO Non-Final Rejection for Application Number 11/468,195 (CD05110) dated 06/09/2008; 6 pages	☐
	4	USPTO Notice of Allowance for Application Number 10/222,129 (CD02069) dated 02/08/2006; 4 pages	☐
	5	USPTO Non-Final Rejection for Application Number 10/222,129 (CD02069) dated 11/01/2005; 9 pages	☐
	6	USPTO Non-Final Rejection for Application Number 10/222,129 (CD02069) dated 05/23/2005; 9 pages	☐
	7	USPTO Notice of Allowance for Application Number 09/182,556 (CD98090) dated 01/26/2001; 3 pages	☐
	8	USPTO Non-Final Rejection for Application Number 09/182,556 (CD98090) dated 09/08/2000; 7 pages	☐
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	Filing Date		2009-10-12	
	First Named Inventor	Gabriel Li		
	Art Unit	2819		
	Examiner Name	Jason Crawford		
	Attorney Docket Number	CD05110C		

/JC/	11	USPTO Notice of Allowance for Application Number 09/232,344 (CD98096) dated 11/13/2000; 2 pages	☐
↓	12	USPTO Final Rejection for Application Number 09/232,344 (CD98096) dated 09/05/2000; 8 pages	☐
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				Filing Date	Herewith	
				First Named Inventor:	Gabriel Li	
				Art Unit	Not yet assigned	
Examiner Name	Not yet assigned					
Attorney Docket Number	CD05110C					
U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US-	2006/0156205	7/06	Tomita	
		US-	2002/0089362	7/02	Lutkemeyer	
		US-	7,365,580	4/08	Martin et al.	
		US-	7,231,009	6/07	Kim et al.	
		US-	7,079,575	7/06	Ho et al.	
		US-	7,042,263	5/06	Johnson et al.	
		US-	6,927,604	8/05	Boerstler et al.	
		US-	6,154,509	11/00	Bishop	
		US-	6,292,016	9/01	Jefferson et al.	
		US-	5,574,753	11/96	Varti et al.	
		US-	5,045,714	9/3/91	Park et al.	
		US-	6,239,646	5/29/01	Navabi et al.	
		US-	6,208,193	3/27/01	Moyal et al.	
		US-	6,385,214	5/7/02	Kikuchi et al.	
		US-	7,069,458	6/27/06	Sardi et al.	
	US	2004/0120087	6/24/04	Ishii		

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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
/JC/		EP	1017193		7/5/00	TriQuint Semiconductor		
/JC/		EP	1187382		3/13/02	Agilent Technologies		

Examiner Signature	/Jason Crawford/ (10/07/2010)	Date Considered	
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				Application Number	Not yet assigned
				Filing Date	Herewith
				First Named Inventor:	Gabriel Li
				Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	2	of	2	Attorney Docket Number	CD05110C
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
/JC/		International Search Report, PCT/US2006/033947, mailed January 15, 2007.			
/JC/		International Written Opinion of International Searching Authority, dated 11/26/2008 for International Application No. PCT/US2006/033947, 6 pages.			

Examiner Signature	/Jason Crawford/ (10/07/2010)	Date Considered	
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	12/577,477	Filing Date	2009-10-12	Docket Number (if applicable)	CD05110C	Art Unit	2819
First Named Inventor	Gabriel Li			Examiner Name	Jason Crawford		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

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☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☐ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Larry Johnson/	Date (YYYY-MM-DD)	2010-08-06
Name	Larry Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	Examiner: Jason Crawford
Gabriel Li	)	
	)	Group Art Unit: 2819
Application No.: 12/577,477	)	
	)	Confirmation No.: 4345
Filed: October 12, 2009	)	
	)	
For: Circuit, System, and Method for	)	
Multiplexing Signals with Reduced	)	
Jitter	)	

REQUEST FOR CONTINUED EXAMINATION
AND INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the Request for Continued Examination to be considered with the IDS for the above referenced application. In compliance with the duty of disclosure under 37 CFR § 1.56 and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

Customer No.: 60909

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, and to credit any overpayments, to Deposit Account No. 50-3781.

Should the Patent Office have any questions regarding this submission or the application in general, the Patent Office is urged to contact the Applicant's attorney, Larry Johnson, by telephone at (408) 545-7194. All correspondence should continue to be directed to the address given below.

/

/

Respectfully submitted,

Date: _____

8/16/2010

By: _____

Larry Johnson
Attorney for Applicant
Registration No. 56,861

Cypress Semiconductor Corporation
198 Champion Court
San Jose, CA 95134
Facsimile: (408) 545-6911
Customer No.: 60909

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		12577477
	Filing Date		2009-10-12
	First Named Inventor	Gabriel Li	
	Art Unit	2819	
	Examiner Name	Jason Crawford	
	Attorney Docket Number	CD05110C	

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	Art Unit	2819		
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	9	4572967	B1	1986-02-25	Metz	Entire Document
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First Named Inventor	Gabriel Li
Art Unit	2819
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	1	USPTO Notice of Allowance for Application Number 11/468,195 (CD05110) dated 06/15/2009; 7 pages	☐
	2	USPTO Notice of Allowance for Application Number 11/468,195 (CD05110) dated 11/26/2008; 7 pages	☐
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	6	USPTO Non-Final Rejection for Application Number 10/222,129 (CD02069) dated 05/23/2005; 9 pages	☐
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	Filing Date		2009-10-12
	First Named Inventor	Gabriel Li	
	Art Unit	2819	
	Examiner Name	Jason Crawford	
	Attorney Docket Number	CD05110C	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	12577477
Filing Date	2009-10-12
First Named Inventor	Gabriel Li
Art Unit	2819
Examiner Name	Jason Crawford
Attorney Docket Number	CD05110C

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Larry Johnson/	Date (YYYY-MM-DD)	2010-08-06
Name/Print	Larry Johnson	Registration Number	56861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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(54) Logic operation circuit.

(57) A logic operation circuit includes an instruction signal generating circuit (11) for generating an instruction signal (X0 - X3) which designates a bit of a predetermined n-bit code signal ($\#0 - \#3$) in accordance with a combination of a first input logical numeral (S) and a second input logical numeral (D). The logic operation circuit also includes a bit selecting circuit (10) for selecting said bit designated by the instruction signal (X0 - X3) generated by the instruction signal generating circuit (11) and for outputting the selected bit as an output logical numeral (Q).

EP 0 314 034 A2

LOGIC OPERATION CIRCUIT

BACKGROUND OF THE INVENTION

5 The present invention generally relates to a logic operation circuit, and more particularly to a logic operation circuit, which is suitably built in a semiconductor memory for image processing.

Currently, a computer system such as a personal computer and a workstation has various functions for displaying graphic information, such as multiwindow display, popup menu, and scroll bar. However, an expansion and enrichment of graphic functions is a heavy load on software to thereby reduce an operation speed. From this viewpoint, a hardware processing called a raster operation or bit bit is employed.

10 A raster operation denotes a function in which a rectangular region formed in a display memory such as a frame buffer is designated for every one bit, and information in the designated rectangular region is transferred to a destination region. In the raster operation, a logic operation such as an AND, OR and EOR operation is carried out with respect to bit information stored in the rectangular region and bit information stored in the destination region. Such a logic operation is employed for enabling cursor display and
15 overlapping window operation.

The raster operation can be implemented by a hardware structure which includes a frame buffer and an operation circuit. The frame buffer is divided into a frame region and a window region. The frame region has a memory space corresponding to a screen of a display unit. The window region has a memory space used for allowing to arrange a plurality of windows without overlapping each other or for storing data for cursor display and icon display as necessary. Image data supplied from a host computer is transferred directly to
20 the frame buffer and is then stored in a position in the frame region or window region. Source data S and destination data D are read out from the frame buffer, and are then supplied to a logic operation circuit. In accordance with an instruction supplied from the host computer, the logic operation circuit selects an operation circuit which performs a corresponding logic expression. The selected logic circuit performs the logic operation on the source data S and the destination data D. A result of the logic operation is written into a region in which the above destination data was stored. For example, in a case where the designated logic operation is an OR operation, a logic expression "S OR D → Q" is performed, and an operation result "Q" is written into the region in which the destination data D was stored.

However, the above logic operation circuit has disadvantages described below. Since the logic
30 operation circuit is constituted by a wired logic circuit, the circuit is necessarily large in size. For this reason, it is difficult to provide the logic operation circuit on a memory chip. Further, a time it takes to perform a logic expression such as AND, OR and NOR, varies depending on a type of logic expression. This is because a signal transfer characteristic of an operation circuit in the logic operation circuit is not the same as that of another operation circuit. The above arises from a circuit structure of a logic circuit and a
35 number of gates thereof.

SUMMARY OF THE INVENTION

40 Accordingly, a general object of the present invention is to provide a logic operation circuit in which the above disadvantages of the conventional logic operation circuit are eliminated.

A more specific object of the present invention is to provide a compact logic operation circuit, in which a time taken to perform a logic operation can be kept constant irrespective of a type of logical expression.

The above objects of the present invention are achieved by a logic operation circuit which includes an instruction signal generating circuit for generating an instruction signal which designates a bit of a predetermined n-bit code signal in accordance with a combination of a first input logical numeral and a
45 second input logical numeral. The logic operation circuit also includes a bit selecting circuit for selecting said bit designated by the instruction signal generated by the instruction signal generating circuit and for outputting the selected bit as an output logical numeral.

50 Other objects, features and advantages of the present invention will become apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a block diagram of a conventional logic operation circuit which implements a raster operation;

FIG.2 is a block diagram of an operation circuit included in the logic operation circuit shown in FIG.1;

FIG.3 is a block diagram of a preferred embodiment of the present invention;

5 FIG.4 is a timing chart of signals at different portions of the structure of FIG.3;

FIG.5 is a circuit diagram of a detailed structure of the embodiment of FIG.3;

FIG.6 is a circuit diagram of another detailed structure of the embodiment of FIG.3;

FIG.7 is a block diagram of a semiconductor memory which employs a logic operation circuit of the present invention;

10 FIG.8 is a circuit diagram of a variation of the structure of FIG.5; and

FIG.9 is a circuit diagram of a variation of the structure of FIG.6.

DETAILED DESCRIPTION

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To facilitate the understanding of the present invention, a description is now given of a conventional logic operation circuit with reference to FIGS.1 and 2.

Referring to FIG.1, a frame buffer 1 is divided into a frame region and a window region. The frame region has a memory space which corresponds to a screen on a display unit. The window region has a memory region used for arranging a plurality of windows without overlapping each other or for storing information for cursor display and icon display. Image data supplied from a host computer 2 is transferred directly to the frame buffer 1, and is then stored into a position in the frame region or window region. Source data S and destination data D are read out from the frame buffer 1, and are then supplied to a logic operation circuit 3. The logic operation circuit 3 selects a logic circuit which implements a logic expression designated by an instruction supplied from the host computer 2. The selected logic circuit performs the related logic operation with respect to the source data S and the destination data D. A result of the logic operation is written into a region in which the above destination data was stored. For example, in a case where the designated logic operation is an OR operation (logical sum), a logic expression "S OR D → Q" is performed, and an operation result Q is written into the region in which the destination data D was stored.

30 FIG.2 shows a structure of the logic operation circuit 3 shown in FIG.1. The logic operation circuit 3 comprises 16 operation circuits OP0 - OP15 associated with 16 different logical expressions. Each of the operation circuits OP0 - OP15 is supplied with source data S and destination data D per bit. Output signals of the operation circuits OP0 - OP15 are supplied to a selector 4. The selector 4 selects one operation circuit from among the operation circuits OP0 - OP15 in accordance with a combination of operation codes $\phi_0 - \phi_3$ supplied from the host computer 2. A result Q of the operation is supplied to the frame buffer 1.

35 TABLE 1 shows a relationship between the logical expressions implemented by the operation circuits OP0 - OP15 and the operation codes $\phi_0 - \phi_3$.

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TABLE 1

Circuits	Operation Codes				Expressions
	σ_3	σ_2	σ_1	σ_0	
5 OP0	0	0	0	0	"0"
OP1	0	0	0	1	$D \cdot S$
OP2	0	0	1	0	$\overline{D} \cdot S$
10 OP3	0	0	1	1	S
OP4	0	1	0	0	$D \cdot \overline{S}$
OP5	0	1	0	1	D
OP6	0	1	1	0	$\overline{D} \cdot \overline{S}$
15 OP7	0	1	1	1	$D + S$
OP8	1	0	0	0	$\overline{D} \cdot \overline{S}$
OP9	1	0	0	1	$\overline{D} \cdot S$
20 OP10	1	0	1	0	$\overline{D}$
OP11	1	0	1	1	$\overline{D} + S$
OP12	1	1	0	0	$\overline{S}$
OP13	1	1	0	1	$D + \overline{S}$
25 OP14	1	1	1	0	$\overline{D} + \overline{S}$
OP15	1	1	1	1	"1"

However, the above 16 different logical expressions are implemented by using wired logic. That is, the operation circuits OP0 - OP15 are constituted by wired logic circuits. Since wired logic circuits are large in size, it is difficult to provide the logic operation circuit on a memory chip. Further, a time it takes to perform an operation varies depending on a type of logic expression. This is because a signal transfer characteristic of a operation circuit is the same as that of another operation circuit. This arises from a circuit structure of a logic circuit and a number of gates thereof.

The present invention intends to overcome the above disadvantages.

A description is given of a preferred embodiment of the present invention with reference to FIGS.3 and

4.

A logic operation circuit 10 is used in place of the logic operation circuit 3 shown in FIG.1. The logic operation circuit 10 are connected to the host computer 2 and the frame buffer 3 as shown in FIG.1. The logic operation circuit 10 comprises a decoder 11 and four transfer gates 12 - 15. The decoder 11 selects any one of output terminals X0 - X3 on the basis of a logical numeral X (source data S) and a logical numeral Y (destination data D). Then the decoder 11 sets the selected output terminal to a low level. ON/OFF control terminals 12a - 15a of the transfer gates 12 - 15 (hereinafter simply referred to as control terminals) are connected to the output terminals X0 - X3, respectively. When the control terminals 12a - 15a are supplied with the low-level signals from the respective output terminals X0 - X3, input terminals and output terminals of the transfer gates 12 - 15 are mutually connected in a low-impedance state. The input terminals of the transfer gates 12 - 15 are supplied with operation codes σ_3 - σ_0 , respectively. Values of the operation codes σ_0 - σ_3 are determined, depending on type of logical expressions. The operation codes construct an n-bit code signal (a 4-bit code signal in FIG.3). When any one of the transfer gates 12 - 15 is turned ON, one of operations codes σ_0 - σ_3 is outputted as a logic output Q (a logical numeral Z).

It can be seen from the above description that the decoder 11 has a function of producing an instruction signal (that is, a low-level signal) for selecting one bit of the n-bit code signal on the basis of a combination of the logical numerals X and Y. The transfer gates 12 - 15 have a function in which when the n-bit code signal depending on a type of a logic expression, is inputted thereto, only one of the transfer gates 12 - 15 which is designated by the instruction signal, passes the corresponding bit as a logical numeral Z.

A description is given of an operation of the structure of FIG.3 with reference to FIG.4.

The following description is with respect to a case where information which has been stored in a window region in the frame buffer 2 is designated and is then transferred to a predetermined position in a frame region (a destination region), so that the information is overwritten therein.

At the commencement of the operation, source data S and destination data D are supplied to the decoder 11 for every one bit. The decoder 11 selects one of the output terminals X0 - X3 based on a combination of the source and destination data S and D. For example, when the combination "SD" is "11", the output terminal X3 is selected. Then, the input and output terminals of the transfer gate 15 are mutually connected in a low impedance state. In a case where information in the window region is overwritten in the destination region, an OR operation is carried out between the source data S and the destination data D. The host computer 2 sets the operation codes $\phi_3 - \phi_0$ to "0111", and supplies the transfer gates 12 - 15 with the operation codes $\phi_3 - \phi_0$, respectively. At this time, since the output terminal X3 of the decoder 11 has already been selected, the operation code ϕ_0 out of the operation codes $\phi_3 - \phi_0$, or "1" is supplied, as an operation result Q, to a frame buffer such as the frame buffer 1 of FIG.1. In a case where the combination "SD" is "10" or "01", the operation result Q is "1". In a case where the combination is "00", the operation code ϕ_3 is selected, and the operation result Q is "0". That is, the operation code ϕ_3 is selected for the combination of "00", the operation code ϕ_2 is selected for "01", the operation code ϕ_1 is selected for "10", and the operation code ϕ_0 is selected for "11".

In a case where the destination data D is deleted and the source data S is newly written in place thereof, the operation codes $\phi_3 - \phi_0$ are set to "0011". As a result, the operation result Q becomes equal to the source data S, and thereby the source data S is written into the frame region.

As described above, in the present embodiment, the operation codes $\phi_0 - \phi_3$ having values which correspond to a desired logic expression are designated and are then supplied to the transfer gates 12 - 15. Further any one of the transfer gates 12 - 15 is turned ON, depending on a combination of the source data S and the destination data D, and one of the operation codes $\phi_0 - \phi_3$ is outputted as an operation result Q. Hence, it is not necessary to provide a logic circuit for each logical expression. As a result, the logic operation circuit can be extremely simplified, and a compact logic operation circuit can be obtained. Additionally, the same circuit structure can be used in common for all the logical expressions. Therefore, a difference in time between different types of logic expressions does not occur and can become fixed.

A description is given of a detailed circuit of the structure of FIG.3 with reference to FIG.5. The decoder 11 is made up of two inverters 16 and 17, and four NAND gates 18 - 21. The transfer gates 12 - 15 are constituted by P-channel MOS (metal-oxide-semiconductor) transistor 22 - 25, respectively. The source data D is supplied directly to the NAND gates 18 and 19 and the inverter 16. An output signal of the inverter 16 is supplied to the NAND gates 20 and 21. The destination data D is supplied directly to the NAND gates 18 and 20 and the inverter 17. An output signal of the inverter 17 is supplied to the NAND gates 19 and 21. Output terminals of the NAND gates 18 - 21 are connected to gates of the transistors 22 - 25, respectively. Sources of the transistors 25 - 22 are supplied with the operation codes $\phi_1 - \phi_3$, respectively. Drains of the transistors 22 - 25 are mutually connected. In operation, one of the outputs of the NAND gates 18 - 21 is switched to the low level in accordance with a combination of the source data S and the destination data D. Then the corresponding one of the transistors 22 - 25 is turned ON, and the corresponding one of the operation codes $\phi_0 - \phi_3$ is selected.

A description is given of another detailed circuit of the structure of FIG.3. In this embodiment, NOR gates 27 - 30 are employed in place of the NAND gates 18 - 21. N-channel MOS transistors 31 - 34 are used in place of the P-channel MOS transistors 22 - 25. The source data S is supplied directly to the NOR gates 29 and 30 and the inverter 16. The output signal of the inverter 16 is supplied to the NOR gates 27 and 28. The destination data is supplied directly to the NOR gates 28 and 30 and the inverter 17. The output signal of the inverter 17 is supplied to the NOR gates 27 and 29. Drains of the transistors 31 - 34 are supplied with the operation codes $\phi_0 - \phi_3$, and sources thereof are mutually connected. The structure of FIG.6 has a function which is the same as that of the structure of FIG.3.

FIG.7 shows a structure of a semiconductor memory into which the logic operation circuit of the invention is built. Input/output buffers 35 - 38 input and output 4-bit data MD₀ - MD₃ in parallel, and input control data DQ₀ - DQ₃ supplied from an external circuit such as a CPU. A control register 39 stores the control data DQ₀ - DQ₃. Logic operation circuits 40 - 43 are constituted by the logic operation circuits of FIG.3, 5 or 6. Column decoders 44 - 47 select pairs of bit lines included in respective memory cell arrays 52 - 55 in accordance with a column address supplied from an address buffer 48. Sense amplifier-I/O gates 48 - 51 (hereinafter simply referred to as sense amplifiers) amplify voltage differences of selected pairs of bit lines and then read out bit information from the respective memory cell arrays 52 - 55. Also, the sense amplifiers 48 - 51 amplify write data and write amplified write data into the memory cell array 52 - 55,

respectively. Each of the memory cell arrays 52 - 55 includes a plurality of memory cells arranged in the form of a matrix. When a memory cell is selected by column decoders 44 - 47 and a row decoder 69 described later, bit information is written into the selected memory cell or is read out bit information from the selected memory cell. Data registers 56 - 59 are supplied, at a time, with bit information which amounts to one line in a direction of a word line of the memory cell arrays 52 - 55. Pointer registers 60 - 63 sequentially designate bit information which amounts to one line per one bit in response to a serial access clock signal, whereby bit information is sequentially outputted per one bit from the data registers 56 - 59. Serial input/output buffers 64 - 67 output, as serial data, output information supplied from the data registers 56 - 59 to output terminals. The address buffer 68 produces a row address and a column address from the external address signal $A_0 - A_8$. Then the address buffer 68 supplies the column decodes 44 - 47 and the row decoder 69 with the row address and column address, respectively.

In operation, the control data $DQ0 - DQ3$ supplied from a CPU (not shown) pass through the input/output buffers 35 - 38, and are stored in the control register 39. On the other hand, the control data $DQ0 - DQ3$ are supplied, as operation codes $\#0 - \#3$, to the logic operation circuits 40 - 43. The logic operation circuits 40 - 43 perform logic operations on the source data S and the destination data D in accordance with a logical expression determined depending on combinations of the operation codes $\#0 - \#3$. The source data S are data read out from the memory cell arrays 52 - 55. The destination data D are data supplied from the input/output buffers 35 - 38. The operation results Q derived from the logic operation circuits 40 - 43 are written into the memory cell arrays 52 - 55 through the column decoders 44 - 47 and the sense amplifiers 48 - 51, respectively. It is noted that the logic operation circuits 40 - 43 can be set to a desired logic expression simply by storing the control data $DQ0 - DQ3$ in the control register 39, and the operation results Q can be written in the memory cell arrays 52 - 55. It is further noted that the integration density of the memory can be increased since the same circuit structure is employed in each logic operation circuits, and thereby the logic operation circuits can be made compact.

A variation of the structure of FIG.5 is shown in FIG.8. The structure of FIG.8 employs NOR gates 81 - 84 in place of the MOS transistors 22 - 25, and an NOR gate 85. The structure of FIG.8 operates in the same manner as the structure of FIG.5. It is noted that the variation of FIG.8 does not have a difference in operation time between different logic expressions. However, an increased number of elements are used for constructing the structure of FIG.8, compared with the structure of FIG.5.

FIG.9 shows a variation of the structure of FIG.6. The variation of FIG.9 employs NAND gates 91 - 94 in place of the MOS transistors 31 - 34 of FIG.6, and a NAND gate 95. The variation of FIG.9 operates in the same manner as the structure of FIG.6, and does not have a difference in operation time between different logic expressions. However an increased number of elements are used for constructing the structure of FIG.9, compared with the structure of FIG.6.

The present invention is not limited to the embodiments, and variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A logic operation circuit, characterized in that the logic operation circuit comprises instruction signal generating means (11) for generating an instruction signal ($X0 - X3$) which designates a bit of a predetermined n-bit code signal ($\#0 - \#3$) in accordance with a combination of a first input logical numeral (S) and a second input logical numeral (D); and bit selecting means (10) for selecting said bit designated by the instruction signal generated by the instruction signal generating means and for outputting the selected bit as an output logical numeral (Q).

2. A logic operation circuit as claimed in claim 1, characterized in that the instruction signal generating means (11) comprises decoder means (11) for decoding the first and second input logical numerals (S, D) and producing the instruction signal which consists of n-bits.

3. A logic operation circuit as claimed in any of claims 1 and 2, characterized in that the bit selecting means (10) comprises n number of transfer gates (12 - 15) each having a control terminal (12a - 15a) to which the instruction signal ($X0 - X3$) is applied, and in that the transfer gates are turned ON/OFF depending on a level of the instruction signal applied to the respective control terminal.

4. A logic operation circuit as claimed in any of claims 1 to 3, characterized in that the bit selecting means (10) comprises n number of P-channel metal-oxide-semiconductor (MOS) transistors (22 - 25); and in that sources of the MOS transistors are supplied with respective bits of the n-bit code signal ($\#0 - \#3$), and drains of the MOS transistors are mutually connected and outputs the output logical numeral (Q).

5. A logic operation circuit as claimed in claim 4, characterized in that the instruction signal generating means (11) comprises n number of NAND gates (18 - 21), and input terminals of the NAND gates are supplied with the first and second input logical numerals (S, D), and output terminals of the NAND gates are connected to gates of the respective MOS transistors 22 - 25).

5 6. A logic operation circuit as claimed in any of claims 1 and 2, characterized in that the bit selecting means (10) comprises n number of N-channel metal-oxide-semiconductor (MOS) transistors (31 - 34), and in that drains of the MOS transistors are supplied with respective bits of the n-bit code signal ($\phi_0 - \phi_3$), and sources of the MOS transistors are mutually connected and outputs the output logical numeral (Q).

7. A logic operation circuit as claimed in claim 6, characterized in that the instruction signal generating means (11) comprises n number of NOR gates (27 - 30), and input terminals of the NAND gates are supplied with the first and second input logical numerals (S, D), and output terminals of the NOR gates are connected to gates of the respective MOS transistors (31 - 34).

8. A logic operation circuit as claimed in any of claims 1 to 7, characterized in that the first and second input logical numerals (S, D) are supplied to the instruction signal generating means (11) per bit.

15 9. A logic operation circuit as claimed in claim any of claims 1 to 8, characterized in that the first and second input logical numerals (S, D) are image data.

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FIG. 1 (PRIOR ART)

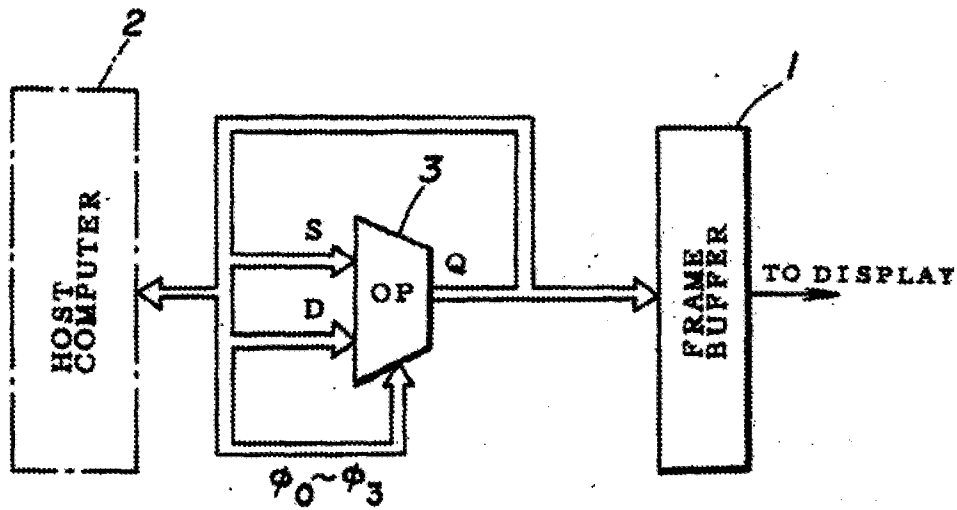


FIG. 2 (PRIOR ART)

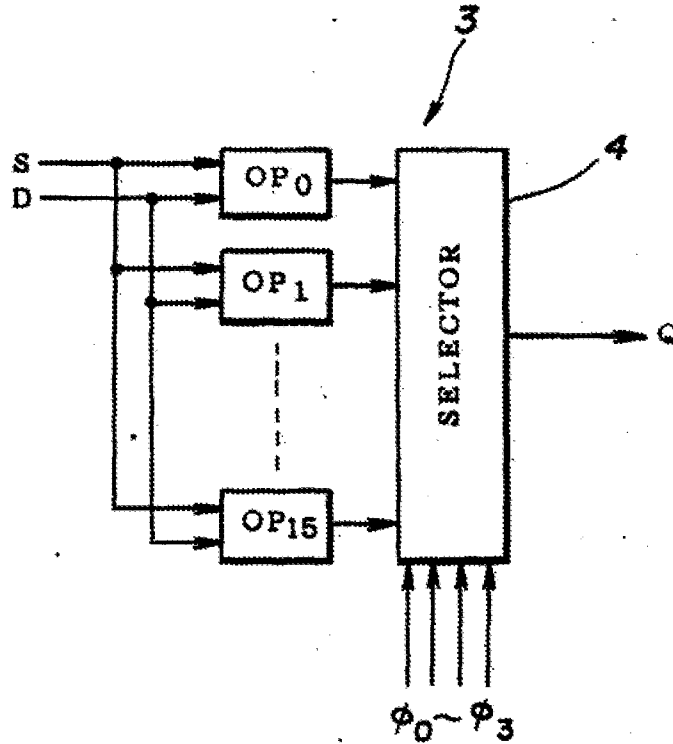


FIG. 3

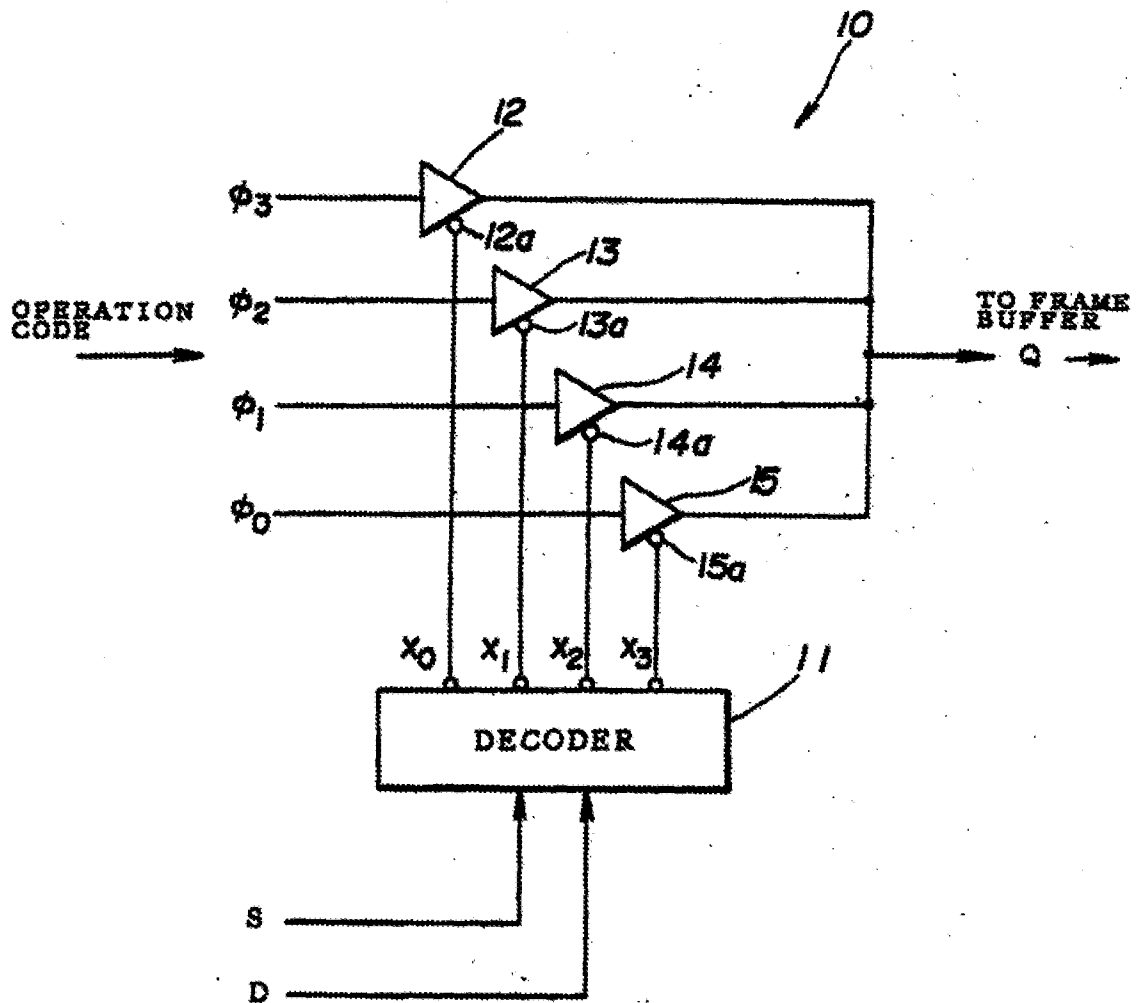


FIG. 4

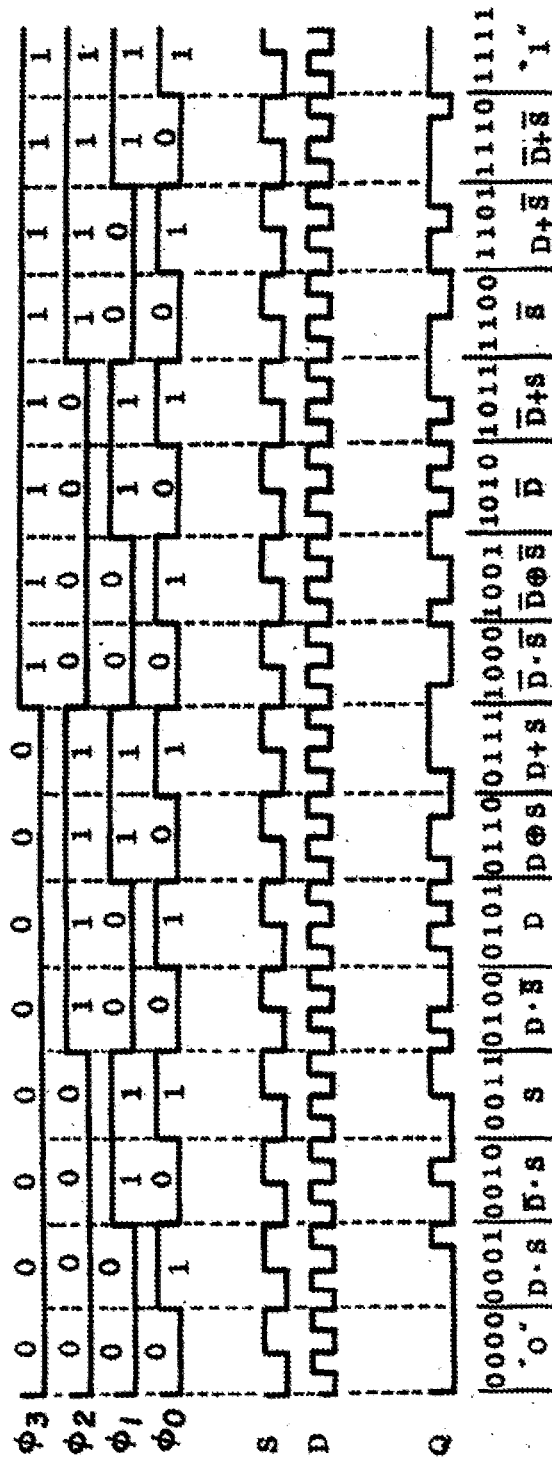


FIG. 5

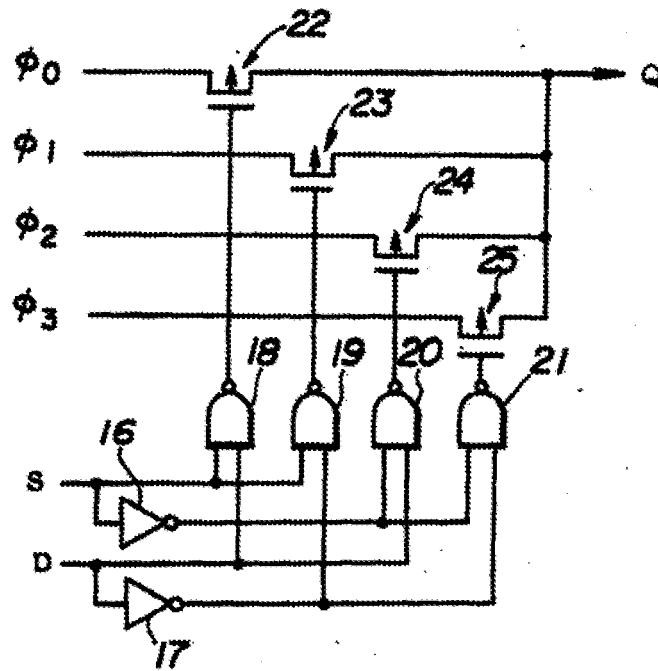


FIG. 6

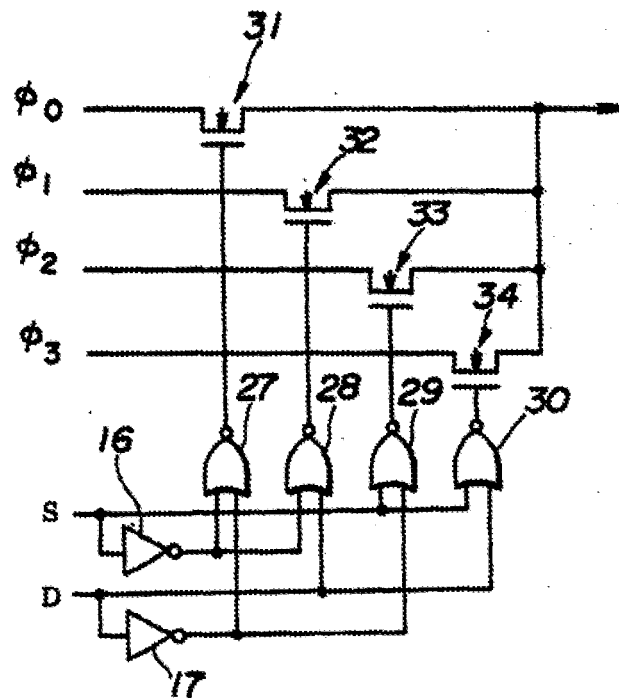
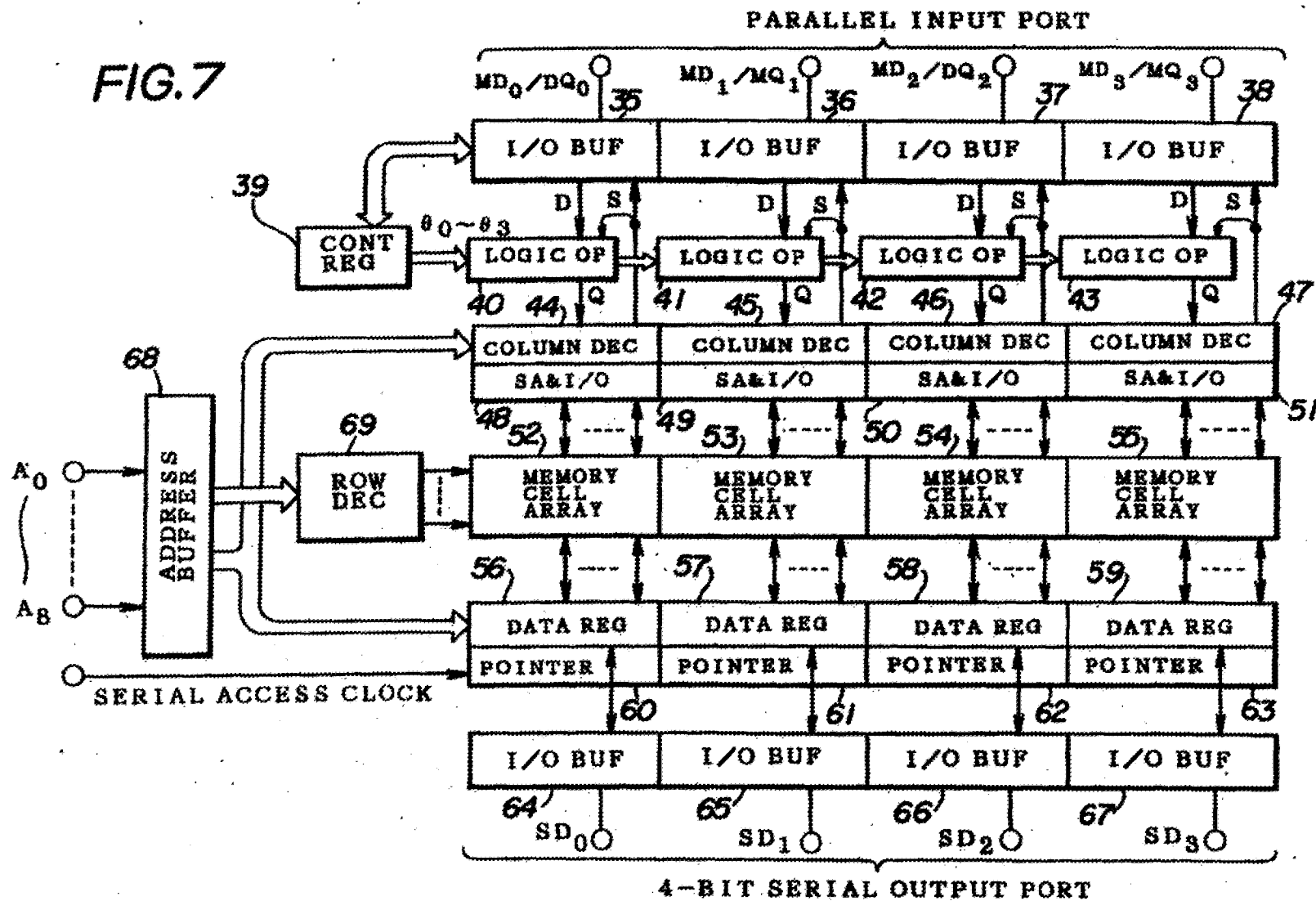


FIG. 7



EP 0 314 034 A2

FIG. 8

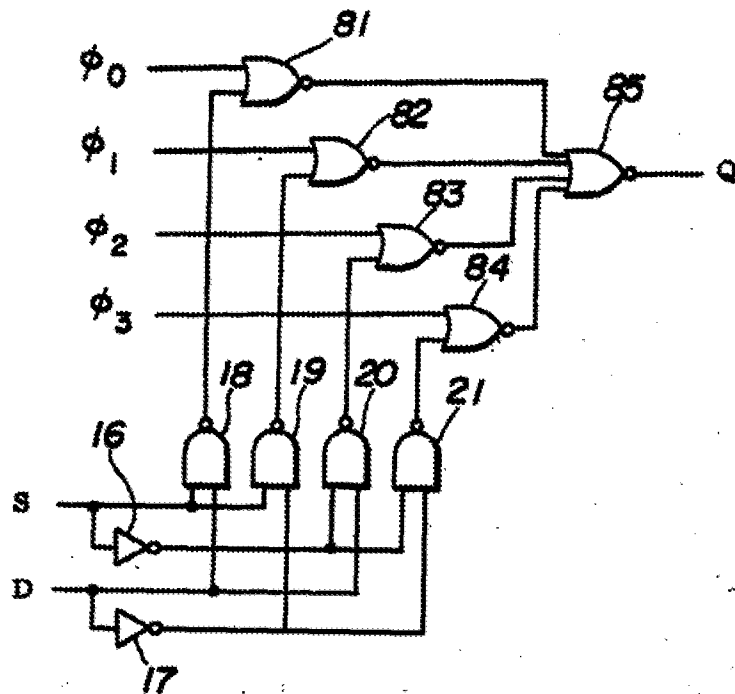
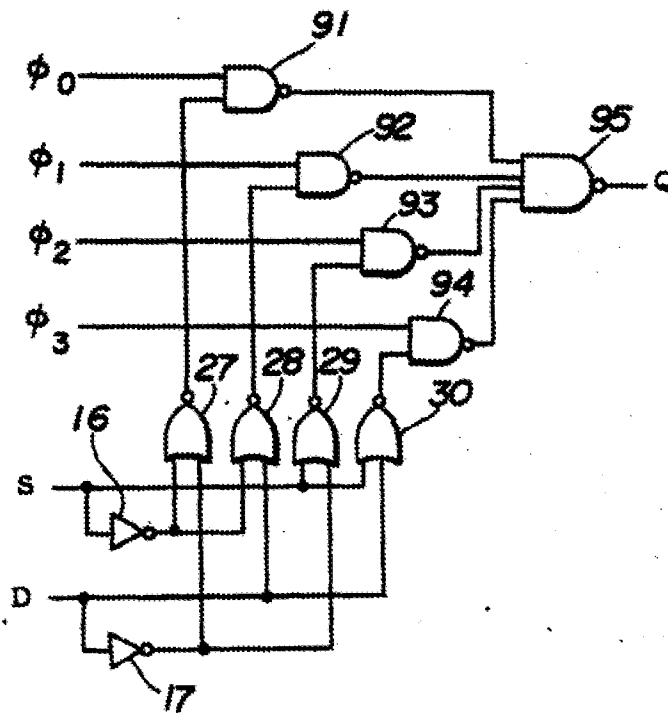


FIG. 9



Electronic Patent Application Fee Transmittal

Application Number:	12577477			
Filing Date:	12-Oct-2009			
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER			
First Named Inventor/Applicant Name:	Gabriel Li			
Filer:	Andrew J. Bateman/Hilary Link			
Attorney Docket Number:	CD05110C			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	1801	1	810	810
Total in USD (\$)				810

Electronic Acknowledgement Receipt

EFS ID:	8557854
Application Number:	12577477
International Application Number:	
Confirmation Number:	4345
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
First Named Inventor/Applicant Name:	Gabriel Li
Customer Number:	60909
Filer:	Andrew J. Bateman/Hilary Link
Filer Authorized By:	Andrew J. Bateman
Attorney Docket Number:	CD05110C
Receipt Date:	04-OCT-2010
Filing Date:	12-OCT-2009
Time Stamp:	19:02:24
Application Type:	Utility under 35 USC 111(a)

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Payment Type	Deposit Account
Payment was successfully received in RAM	\$810
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File Listing:

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Warnings:					
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2	Transmittal Letter	CD05110Ctransmittalletter.pdf	333953	no	2
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Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Filed (SB/08)	CD05110CIDSform.pdf	612947	no	6
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Warnings:					
Information:					
4	Foreign Reference	CD98090ogawaDEepForeign.pdf	2695015	no	13
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Information:					
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MOSAID Technologies Inc., Exhibit 2023 Page 2023 - 75					

17	NPL Documents	CD98096nonfinal032900.pdf	276910 4fe24417b309b2afb7668d5bb26c8d06788bd55f	no	8
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Information:					
18	Fee Worksheet (PTO-875)	fee-info.pdf	30817 f5eacb0e6757e953fbb34c9ed35788c29649ffa	no	2
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198 CHAMPION COURT
SAN JOSE, CA 95134-1709

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CRAWFORD, JASON

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 07/22/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/577,477

10/12/2009

Gabriel Li

CD05110C

4345

TITLE OF INVENTION: CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/577,477

10/12/2009

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CD05110C

4345

TITLE OF INVENTION: CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	10/22/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
CRAWFORD, JASON	2819	375-376000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

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This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/577,477	10/12/2009	Gabriel Li	CD05110C	4345
60909	7590	07/22/2010	EXAMINER	
CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709			CRAWFORD, JASON	
			ART UNIT	PAPER NUMBER
			2819	
DATE MAILED: 07/22/2010				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	12/577,477	LI, GABRIEL	
	Examiner	Art Unit	
	JASON CRAWFORD	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 6/4/2010.
2. ☒ The allowed claim(s) is/are 3-6 and 8-22.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Notice of Informal Patent Application |
| 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. |
| 3. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>10/12/09</u> | 7. ☐ Examiner's Amendment/Comment |
| 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. ☒ Examiner's Statement of Reasons for Allowance |
| | 9. ☐ Other ____. |

/JASON CRAWFORD/
Examiner, Art Unit 2819

DETAILED ACTION

Terminal Disclaimer

The terminal disclaimer filed on 6/4/2010 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,609,799 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Miscellaneous

The Applicant has cancelled claims 1-2 and 7, and added new claims 21-22; therefore only claims 3-6 and 8-22 remain for this Office Action.

Allowable Subject Matter

Claims 3-6 and 8-22 are allowed. The following is an examiner's statement of reasons for allowance:

In regards to claim 3, the prior art discloses of an apparatus, comprising: a plurality of power supply domains; and a plurality of logic components, each of the plurality of logic components within a different one of the plurality of power supply domains, wherein each of the plurality of logic components is configured to operate with a corresponding clock signal within a respective one of the plurality of power supply domains, however, the prior art does not disclose of wherein the plurality of power supply domains comprises first, second, third and fourth power supply domains, wherein a plurality of logic components comprises: a first logic gate arranged within the

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first power supply domain and configured to operate with a first clock signal; a second logic gate arranged within the second power supply domain and configured to operate with a second clock signal; a first logic block arranged within the third power supply domain and coupled to the first and second logic gates; and a second logic block arranged within the fourth power supply domain and coupled to the first and second logic gates, nor would it have been obvious to one of ordinary skill in the art to do so.

Claims 4-6, 8-11 and 21 are also allowed as being dependent on claim 3.

In regards to claim 12, the prior art does not disclose of a system, comprising: a circuit comprising two logic gates and a first logic block and a second logic block, each arranged within a separate power supply domain, wherein: a first of the two logic gates is operatively coupled with a first signal; a second of the two logic gates is operatively coupled with a second signal; and a second logic block operatively coupled with one of the first and second signals, depending on a state of a control signal; and a system component coupled to the second logic block, nor would it have been obvious to one of ordinary skill in the art to do so. Claims 13-17 and 22 are also allowed as being dependent on claim 12.

In regards to claim 18, the prior art does not disclose of a method, comprising: deactivating one of a first signal or a second signal by supplying a control signal to first and second logic gates; and forwarding an active one of the first or second signals to a third logic gate, wherein the first, second and third logic gates are spaced apart from one another and respectively arranged within a first, second and third power

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supply domain, nor would it have been obvious to one of ordinary skill in the art to do so. Claims 19 and 20 are also allowed as being dependent on claim 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON CRAWFORD whose telephone number is (571)272-6004. The examiner can normally be reached on Mon-Fri 7:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JASON CRAWFORD/
Examiner, Art Unit 2819

/Rexford N BARNIE/

Supervisory Patent Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 12/577,477		Applicant(s)/Patent Under Reexamination LI, GABRIEL	
	Examiner JASON CRAWFORD		Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0268278	12-2004	Hoberman et al.	716/005
*	B	US-5,991,135	11-1999	Saleh, Farid	361/56
*	C	US-7,030,661	04-2006	Doyle, James Thomas	327/102
*	D	US-2006/0165205	07-2006	Dally, William J.	375/371
*	E	US-2002/0089362	07-2002	Lutkemeyer, Christian A.J.	327/161
*	F	US-7,365,580	04-2008	Martin et al.	327/156
*	G	US-7,231,009	06-2007	Kim et al.	375/354
*	H	US-7,079,575	07-2006	Ho et al.	375/232
*	I	US-6,154,509	11-2000	Bishop, Wendell	375/371
*	J	US-6,292,016	09-2001	Jefferson et al.	326/39
*	K	US-6,927,604	08-2005	Boerstler et al.	326/93
*	L	US-7,042,263	05-2006	Johnson et al.	327/199
*	M	US-7,305,646	12-2007	McGrath et al.	716/12

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

~~file:///C:/Documents%20and%20Settings/jcrawford/My%20...7477/EASTHERO-2025-01-17-171TheOneTechnologies Americas Corp.~~

L16	52	L14 not L15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:26
L17	52	L16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:26
L18	0	3s108	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L19	52	L16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L20	15550	326/21-22,29.ccls. 327/99,147,407-408.ccls. 375/371,376.ccls. 713/400-401,500-503,600- 601.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L21	12349	L20 and @ad<"20050902"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L22	12349	L21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L23	4198	L22 and (mux\$3 multiplex \$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42

L24	866	L23 and ((NAND NOR) adj (logic gate function block))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L25	229	L24 and jitter\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L26	162	L25 and power	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L27	141	(PLL DLL ((phase delay) adj lock\$3 adj loop)) and L26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42
L28	141	L27	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/06/17 12:42

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L29	2	((((power supply voltage) adj (island domain)) and logic and clock\$3 and (NAND NOR)).clm.	USPAT; UPAD	OR	ON	2010/06/17 12:46
L30	36	((((power supply voltage) adj (island domain)) and logic and clock\$3).clm.	USPAT; UPAD	OR	ON	2010/06/17 12:46
L31	108	((((power supply voltage) adj (island domain)) and logic).clm.	USPAT; UPAD	OR	ON	2010/06/17 12:46

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file:///C:/Documents%20and%20Settings/jerawford/My%20...7477/EASTHERO2025-01-17 17:11:11 by Infron Technologies Americas Corp. or MOSAID Technologies Inc.

file:///C:/Documents%20and%20Settings/jerawford/My%20...7477/EASTHERO2025-01-17 17:11:11 by Infron Technologies Americas Corp. v. MOSAID Technologies Inc.

<i>Index of Claims</i> 	Application/Control No. 12577477	Applicant(s)/Patent Under Reexamination LI, GABRIEL
	Examiner JASON CRAWFORD	Art Unit 2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☒ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	03/08/2010	06/17/2010						
-	1	✓	-						
-	2	✓	-						
1	3	O	=						
2	4	O	=						
3	5	O	=						
4	6	✓	=						
-	7	✓	-						
5	8	✓	=						
6	9	✓	=						
7	10	✓	=						
8	11	✓	=						
10	12	✓	=						
11	13	✓	=						
12	14	✓	=						
13	15	✓	=						
14	16	✓	=						
15	17	✓	=						
17	18	✓	=						
18	19	✓	=						
19	20	✓	=						
9	21		=						
16	22		=						

Search Notes 	Application/Control No. 12577477	Applicant(s)/Patent Under Reexamination LI, GABRIEL
	Examiner JASON CRAWFORD	Art Unit 2819

SEARCHED			
Class	Subclass	Date	Examiner
327	99,147,407-408	6/17/2010	JC
375	371,376	6/17/2010	JC
713	400-401,500-503,600-601	6/17/2010	JC
326	21-22,29	6/17/2010	JC

SEARCH NOTES		
Search Notes	Date	Examiner
See attached search	6/17/2010	JC

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
All	of Above	6/17/2010	JC

/JASON CRAWFORD/ Examiner.Art Unit 2819	
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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known		
				Application Number	Not yet assigned	
				Filing Date	Herewith	
				First Named Inventor:	Gabriel Li	
				Art Unit	Not yet assigned	
Examiner Name	Not yet assigned					
Attorney Docket Number	CD05110C					
U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US-	2006/0156205	7/06	Tomita	
		US-	2002/0089362	7/02	Lutkemeyer	
		US-	7,365,580	4/08	Martin et al.	
		US-	7,231,009	6/07	Kim et al.	
		US-	7,079,575	7/06	Ho et al.	
		US-	7,042,263	5/06	Johnson et al.	
		US-	6,927,604	8/05	Boerstler et al.	
		US-	6,154,509	11/00	Bishop	
		US-	6,292,016	9/01	Jefferson et al.	
		US-	5,574,753	11/96	Vartti et al.	
		US-	5,045,714	9/3/91	Park et al.	
		US-	6,239,646	5/29/01	Navabi et al.	
		US-	6,208,193	3/27/01	Moyal et al.	
		US-	6,385,214	5/7/02	Kikuchi et al.	
		US-	7,069,458	6/27/06	Sardi et al.	
	US	2004/0120087	6/24/04	Ishii		

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
/JC/		EP	1017193		7/5/00	TriQuint Semiconductor		
/JC/		EP	1187382		3/13/02	Agilent Technologies		

Examiner Signature	/Jason Crawford/ (06/17/2010)	Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

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Examiner Signature	/Jason Crawford/ (06/17/2010)	Date Considered	
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¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English Translation is attached.
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.**
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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE INDICATED THROUGHOUT. /JC/



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BIB DATA SHEET

CONFIRMATION NO. 4345

SERIAL NUMBER 12/577,477	FILING or 371(c) DATE 10/12/2009 RULE	CLASS 375	GROUP ART UNIT 2819	ATTORNEY DOCKET NO. CD05110C	
APPLICANTS Gabriel Li, San Francisco, CA; ** CONTINUING DATA ***** This application is a CON of 11/468,195 08/29/2006 PAT 7,609,799 JC which claims benefit of 60/713,682 09/02/2005 JC ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/22/2009					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JASON CRAWFORD/</u> Examiner's Signature	☐ Met after Allowance JC Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 5	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709 UNITED STATES					
TITLE CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER					
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Application Number 	Application/Control No. 12/577,477	Applicant(s)/Patent under Reexamination LI, GABRIEL	

Document Code - DISQ	Internal Document – DO NOT MAIL
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TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 6/4/10	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
Janice Ford

U.S. Patent and Trademark Office

**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING
REJECTION OVER A "PRIOR" PATENT**

Attorney Docket Number
CD05110C

In re Application of: Gabriel Li

Application No.: 12/577,477

Filed: 10/12/09

For: CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

The owner*, Cypress Semiconductor Corp., of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term **prior patent** No. 7,609,799 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent **of record**. Reg. No. 41,236

/Daniel Ovanezian/
Signature 6/4/10 Date

Daniel E. Ovanezian
Typed or printed name

(408) 720-8300
Telephone Number

☒ **Terminal disclaimer fee under 37 CFR 1.20(d) is included.**

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*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification (see MPEP § 324.) Where an attorney or agent **of record** signs the Terminal Disclaimer, there is no need to provide a Statement under 37 CFR 3.73(b) (see MPEP § 1490).

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Juanita Briscoe	
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/Juanita Briscoe/	6/4/10
Signature	Date

Electronic Patent Application Fee Transmittal

Application Number:	12577477			
Filing Date:	12-Oct-2009			
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER			
First Named Inventor/Applicant Name:	Gabriel Li			
Filer:	Daniel E. Ovanezian/Juanita Briscoe			
Attorney Docket Number:	CD05110C			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Statutory disclaimer	1814	1	140	140
Total in USD (\$)				140

Electronic Acknowledgement Receipt

EFS ID:	7747638
Application Number:	12577477
International Application Number:	
Confirmation Number:	4345
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
First Named Inventor/Applicant Name:	Gabriel Li
Customer Number:	60909
Filer:	Daniel E. Ovanezian/Juanita Briscoe
Filer Authorized By:	Daniel E. Ovanezian
Attorney Docket Number:	CD05110C
Receipt Date:	04-JUN-2010
Filing Date:	12-OCT-2009
Time Stamp:	18:19:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 140
RAM confirmation Number	5161
Deposit Account	022666
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

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MOSAID Technologies Inc., Exhibit 2023

Page 2023 - 102

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		CD05110C_P687C_Amendment_S.pdf	60102	yes	10
			4bf874fa4b0b92243501ed67124a60ecc77683c2		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	6	
	Applicant Arguments/Remarks Made in an Amendment		7	10	
Warnings:					
Information:					
2	Terminal Disclaimer Filed	CD05110C_P687C_Terminal_Disclaimer.pdf	28900	no	2
			2f91691eae7189dc832f0f0572958dad3ce8222d		
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30441	no	2
			b0aba2f6ad640eb8fbf5b41e003c12c356b15c9c		
Warnings:					
Information:					
Total Files Size (in bytes):			119443		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Gabriel Li

Serial No. 12/577,477

Filed: 10/12/09

For: **CIRCUIT, SYSTEM, AND
METHOD FOR MULTIPLEXING
SIGNALS WITH REDUCED
JITTER**

EXAMINER: CRAWFORD, JASON

ART UNIT: 2819

CONFIRMATION No.: 4345

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT AND RESPONSE TO OFFICE ACTION

Sir:

In response to the Office Action mailed March 10, 2010, applicant respectfully requests the Examiner to enter the following amendments and consider the following remarks:

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

IN THE CLAIMS

Claims 1-2 (Canceled).

3. (Currently amended) ~~The apparatus of claim 2,~~ An apparatus, comprising:
a plurality of power supply domains; and
a plurality of logic components, each of the plurality of logic components within a
different one of the plurality of power supply domains, wherein each of the plurality of
logic components is configured to operate with a corresponding clock signal within a
respective one of the plurality of power supply domains, wherein the plurality of power
supply domains comprises first, second, third and fourth power supply domains, wherein
a plurality of logic components comprises:
- a first logic gate arranged within the first power supply domain and configured to
operate with a first clock signal;
 - a second logic gate arranged within the second power supply domain and
configured to operate with a second clock signal;
 - a first logic block arranged within the third power supply domain and coupled to
the first and second logic gates; and
 - a ~~third~~ second logic ~~gate~~ block arranged within the fourth power supply domain
and coupled to the first and second logic gates.

4. (Currently amended) The apparatus of claim 3, wherein the first~~[[,]]~~ and second ~~and third~~ logic gates and the second logic block each comprise either a two-input NAND gate or a two-input NOR gate.
5. (Currently amended) The apparatus of claim 3, wherein the first logic gate has a first input coupled to receive the first signal and second input coupled to receive a control signal from the first logic block, wherein the second logic gate has a first input coupled to receive the second signal and a second input coupled to receive the control signal from the first logic block,
- wherein the first logic block is configured to supply the control signal to the first and second logic gates to deactivate one of the first and second signal, and
- wherein the ~~third~~ second logic ~~gate~~ block has inputs coupled to receive outputs of the first and second logic gates and transmit either the first signal or the second signal, which has not been deactivated by the first logic block.
6. (Currently amended) The apparatus of claim ~~[[1]]~~ 3, wherein each of the plurality of power supply domains is supplied with its own power bus and physically separated from logic components arranged in other power supply domains.
7. (Canceled)
8. (Currently amended) A multiplexer comprising the apparatus of claim ~~[[1]]~~ 3.

9. (Currently amended) A clock generation device comprising the apparatus of claim [[1]] 3.
10. (Currently amended) A motherboard comprising the clock generation device of claim [[6]] 9.
11. (Currently amended) A phone comprising the apparatus of claim [[1]] 3.
12. (Currently amended) A system, comprising:
a circuit comprising two ~~three~~ logic gates and a first logic block and a second logic block, each arranged within a separate power supply domain, wherein:
a first of the two ~~three~~ logic gates is operatively coupled with a first signal;
a second of the two ~~three~~ logic gates is operatively coupled with a second signal; and
a ~~third of the three~~ second logic ~~gates~~ block operatively coupled with one of the first and second signals, depending on a state of a control signal; and
a system component coupled to the ~~third~~ second logic ~~gate~~ block.
13. (Currently amended) The system of claim 12, wherein the first[[.]] and second ~~and third~~ logic gates and the second logic block each comprise either a NAND gate or a NOR gate.

14. (Original) The system of claim 12, wherein the first and second signals comprise clock signals.

15. (Original) The system of claim 12, further comprising one or more phase shift apparatuses coupled to the circuit.

16. (Original) The system of claim 15, wherein the one or more phase shift apparatuses each comprise either a phase locked loop (PLL) device or a delay locked loop (DLL) device.

17. (Currently amended) ~~The~~ A clock network comprising the system of claim 15.

18. (Original) A method, comprising:

deactivating one of a first signal or a second signal by supplying a control signal to first and second logic gates; and

forwarding an active one of the first or second signals to a third logic gate, wherein the first, second and third logic gates are spaced apart from one another and respectively arranged within a first, second and third power supply domain.

19. (Original) The method of claim 18, wherein the first and second signals comprise clock signals.

20. (Original) The method of claim 19, wherein the first and second signals comprise data signals.

21. (New) The apparatus of claim 3, wherein the second logic block comprises a gate.

22. (New) The system of claim 12, wherein the second logic block comprises a gate.

REMARKS

Applicant respectfully requests reconsideration of this application as amended.

Office Action Summary

The drawings have been objected to as allegedly not showing the feature of the supply guard rings recited in claim 7.

Claims 12-16 and 18-20 have been rejected on the ground of nonstatutory obviousness-type double patenting as being allegedly unpatentable over claims 10-12 and 14-19 of U.S. Patent No. 7,609,799.

Claims 10 and 17 have been rejected under 35 U.S.C. 112, second paragraph, as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 2 and 6-7 have been rejected under 35 U.S.C. 102(a) as being allegedly anticipated by U.S. Publication No. 2004/0268278 of Hoberman et al. (“Hoberman”).

Claims 8-9 and 11 have been rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Hoberman in view of *Ex Parte Masham 2 USPQ F.2d 16467 (1987)* (“Masham”).

Claims 3-5 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Status of Claims

Claims 3-6, 8-13 and 17 have been amended. The amended claims are supported by the specification. Claims 21 and 22 have been added. No new matter has been added. Claims 1-2 and 7 have been canceled, without prejudice. Therefore, claims 3-6 and 8-22 are pending.

Rejections and Objections

The drawings have been objected to as allegedly not showing the feature of the supply guard rings recited in claim 7. It is submitted that claim 7 has been canceled, without prejudice, and therefore the objection is now moot.

Claims 12-16 and 18-20 have been rejected on the ground of nonstatutory obviousness-type double patenting as being allegedly unpatentable over claims 10-12 and 14-19 of U.S. Patent No. 7,609,799. Applicants are filing a terminal disclaimer herewith and, therefore, submit that the double patenting rejection has been overcome.

Claims 10 and 17 have been rejected under 35 U.S.C. 112, second paragraph, as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is submitted that the amendments to the claims overcome the rejections.

Claims 1, 2 and 6-7 have been rejected under 35 U.S.C. 102(a) as being anticipated by U.S. Publication No. 2004/0268278 of Hoberman et al. (“Hoberman”). Claims 1-2 and 7 have been canceled and the dependency of claim 6 has been amended. Therefore, it is submitted that the rejection is now moot.

Claims 8-9 and 11 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Hoberman in view of *Ex Parte Masham 2 USPQ F.2d 16467 (1987)* (“Masham”). It is submitted that the dependencies of claims 8-9 and 11 have been amended and, therefore, the rejection is now moot.

Claims 3-5 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. It is submitted that claim 3 has been amended to include limitations of its original base claim 1 and also to amend the original feature of the third logic gate to be a “second logic block.” It is submitted that claim 3 as amended is allowable for reasons similar to those provided in the Office Action. In particular, it is submitted that the prior art does not disclose an apparatus “wherein the plurality of power supply domains comprises first, second, third and fourth power supply domains, wherein a plurality of logic components comprises: a first logic gate arranged within the first power supply domain and configured to operate with a first clock signal; a second logic gate arranged within the second power supply domain and configured to operate with a second clock signal; a first logic block arranged within the third power supply domain and coupled to the first and second logic gates; and a second logic block arranged within the fourth power supply domain and coupled to the first and second logic gates” as recited in claim 3, nor would it have been obvious to one of ordinary skill in the art. Therefore, allowance of claim 3 and its dependent claims is earnestly solicited.

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. The Examiner is invited to contact Applicant's representative Larry Johnson at (408) 545-7194 if the Examiner believes such action would expedite examination of the present application.

Please charge any additional fees under 37 C.F.R. §§ 1.16, 1.17, 1.18, 1.20 and 1.21 that may be required to maintain pendency of the present application, or apply any credits to PTO deposit account number: 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: June 4, 2010

/Daniel Ovanezian/
Daniel E. Ovanezian
Registration No. 41,236

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300

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Name of Person Filing Correspondence	<u>Juanita Briscoe</u>
Signature	<u>/Juanita Briscoe/</u>
Date	<u>6/4/10</u>

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/577,477		Filing Date 10/12/2009		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A		N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR	X \$	=	X \$	=	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=	OR	X \$	=	X \$	=	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	06/04/2010	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X \$	=	OR	X \$52=	0	
Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$	=	OR	X \$220=	0	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR	X \$	=	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR	X \$	=	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/577,477

10/12/2009

Gabriel Li

CD05110C

4345

60909

7590

03/10/2010

CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

EXAMINER

CRAWFORD, JASON

ART UNIT

PAPER NUMBER

2819

MAIL DATE

DELIVERY MODE

03/10/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/577,477	Applicant(s) LI, GABRIEL	
	Examiner JASON CRAWFORD	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 October 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2 and 6-20 is/are rejected.
- 7) ☒ Claim(s) 3-5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 October 2009 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>10/12/09</u> . | 6) ☐ Other: _____ |

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the supply guard rings must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 12-16 and 18-20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 10-12 and 14-19 of U.S.

Patent No. 7,609,799. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

In regards to claim 12, the pending application claim 10 and conflicting '799 patent claim 10 both claim:

*A system, comprising:
a circuit comprising three logic gates and a logic block, each arranged within a separate
power supply domain, wherein:
a first of the three logic gates is operatively coupled with a first signal;
a second of the three logic gates is operatively coupled with a second signal; and*

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*a third of the three logic gates operatively coupled with one of the first and second signals, depending on a state of a control signal; and
a system component coupled to the third logic gate.*

Likewise, dependent claims 13-16 of the pending application are also claimed as claims 11-12 and 14-16 of the conflicting '799 patent.

In regards to claim 18, the pending application claim 18 and conflicting '799 patent claim 17 both claim:

*A method, comprising:
deactivating one of a first signal or a second signal by supplying a control signal to first and second logic gates; and
forwarding an active one of the first or second signals to a third logic gate, wherein the first, second and third logic gates are spaced apart from one another and respectively arranged within a first, second and third power supply domain.*

Likewise, dependent claims 19 and 20 of the pending application are also claimed as claims 18 and 19 of the conflicting '799 patent.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 10 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "the clock generation device" in line 1. There is insufficient antecedent basis for this limitation in the claim.

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Claim 17 recites the limitation "**The** clock network comprising the system of claim 15." in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim. Although it appears that the Applicant may have wished to claim "**A** clock network comprising the system of claim 15" appropriate correction is required to rectify the 112 rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 2 and 6-7 are rejected under 35 U.S.C. 102(a) as being anticipated by Hoberman et al. (US 2004/0268278).

In regards to claim 1, Hoberman discloses of an apparatus, comprising: a plurality of power supply domains (Power Islands 112, 114, 116 and 118); and a plurality of logic components (262 see Fig 2, logic block located within one of the Power Islands), each of the plurality of logic components within a different one of the plurality of power supply domains (Power Islands), wherein each of the plurality of logic components is configured to operate with a corresponding clock signal (Paragraph 0032) within a respective one of the plurality of power supply domains (Power Islands). (Figs 1-2, Paragraph 0030-0048)

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In regards to claim 2, Hoberman discloses of the apparatus of claim 1, wherein the plurality of power supply domains comprises at least three power supply domains (for example Power Islands 112, 114 and 116) and wherein the plurality of logic components comprise at least three logic components (262 see Fig 2, logic block located within one of the Power Islands). (Figs 1-2, Paragraph 0030-0048)

In regards to claim 6, Hoberman discloses of the apparatus of claim 1, wherein each of the plurality of power supply domains is supplied with its own power bus (126 split among the Power Islands 112, 114, 116 and 118) and physically separated (see separation in Fig 1) from logic components arranged in other power supply domains (see Fig 1). (Figs 1-2, Paragraph 0030-0048)

In regards to claim 7, Hoberman discloses of the apparatus of claim 6, wherein each of the plurality of logic components are located in different supply islands (112, 114, 116 and 118) comprising supply guard rings (see borders around the islands 112, 114, 116 and 118 in Fig 1, also see Fig 2 islands 260 and 270 with the islands and supply managers surround the logic block). (Figs 1-2, Paragraph 0030-0048)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 8-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoberman et al. (US 2004/0268278) in view of Ex Parte Masham (2 USPQ F.2d 16467 (1987)).

In regards to claims 8-9 and 11, Hoberman discloses of the apparatus as found within the explanation of claim 1 above, however, Hoberman does not disclose of a multiplexer, clock generation device and a phone comprising the apparatus of claim 1.

It has been held that a recitation within respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claims apparatus from a prior art apparatus satisfying the claimed structural limitations. (Ex Parte Masham)

Therefore, at the time the invention was made, it would have been obvious to one of ordinary skill in the art employ the apparatus of Hoberman in a multiplexer, clock generation device or phone as taught by Ex Parte Masham to achieve the desired device design and desired use of the device.

Allowable Subject Matter

5. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to claim 3, the prior art discloses of the apparatus of claim 2 as found within the explanation above, wherein the plurality of power supply domains comprises

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first, second, third and fourth power supply domains, however, the prior art does not disclose of the apparatus further comprising wherein a plurality of logic components comprises: a first logic gate arranged within the first power supply domain and configured to operate with a first clock signal; a second logic gate arranged within the second power supply domain and configured to operate with a second clock signal; a logic block arranged within the third power supply domain and coupled to the first and second logic gates; and a third logic gate arranged within the fourth power supply domain and coupled to the first and second logic gates, nor would it have been obvious to one of ordinary skill in the art to do so. Claims 4 and 5 are also objected to as being dependent on claim 3.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON CRAWFORD whose telephone number is (571)272-6004. The examiner can normally be reached on Mon-Fri 7:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JASON CRAWFORD/
Examiner, Art Unit 2819

Notice of References Cited	Application/Control No. 12/577,477		Applicant(s)/Patent Under Reexamination LI, GABRIEL	
	Examiner JASON CRAWFORD		Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0268278	12-2004	Hoberman et al.	716/005
*	B	US-5,991,135	11-1999	Saleh, Farid	361/56
*	C	US-7,030,661	04-2006	Doyle, James Thomas	327/102
*	D	US-2006/0165205	07-2006	Dally, William J.	375/371
*	E	US-2002/0089362	07-2002	Lutkemeyer, Christian A.J.	327/161
*	F	US-7,365,580	04-2008	Martin et al.	327/156
*	G	US-7,231,009	06-2007	Kim et al.	375/354
*	H	US-7,079,575	07-2006	Ho et al.	375/232
*	I	US-6,154,509	11-2000	Bishop, Wendell	375/371
*	J	US-6,292,016	09-2001	Jefferson et al.	326/39
*	K	US-6,927,604	08-2005	Boerstler et al.	326/93
*	L	US-7,042,263	05-2006	Johnson et al.	327/199
*	M	US-7,305,646	12-2007	McGrath et al.	716/12

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 12577477	Applicant(s)/Patent Under Reexamination LI, GABRIEL
	Examiner JASON CRAWFORD	Art Unit 2819

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant
☐ CPA
☐ T.D.
☐ R.1.47

CLAIM		DATE							
Final	Original	03/08/2010							
	1	✓							
	2	✓							
	3	O							
	4	O							
	5	O							
	6	✓							
	7	✓							
	8	✓							
	9	✓							
	10	✓							
	11	✓							
	12	✓							
	13	✓							
	14	✓							
	15	✓							
	16	✓							
	17	✓							
	18	✓							
	19	✓							
	20	✓							

Search Notes 	Application/Control No. 12577477	Applicant(s)/Patent Under Reexamination LI, GABRIEL
	Examiner JASON CRAWFORD	Art Unit 2819

SEARCHED			
Class	Subclass	Date	Examiner
326	99,147,407-408	3/8/2010	JC
375	371,376	3/8/2010	JC
713	400-401,500-503,600-601	3/8/2010	JC
326	21-22,29	3/8/2010	JC

SEARCH NOTES		
Search Notes	Date	Examiner
See attached search	3/8/2010	JC

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
All	of Above	3/8/2010	JC

/JASON CRAWFORD/ Examiner.Art Unit 2819	
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CONFIRMATION NO. 4345

SERIAL NUMBER 12/577,477	FILING or 371(c) DATE 10/12/2009 RULE	CLASS 375	GROUP ART UNIT 2819	ATTORNEY DOCKET NO. CD05110C		
APPLICANTS Gabriel Li, San Francisco, CA; ** CONTINUING DATA ***** This application is a CON of 11/468,195 08/29/2006 PAT 7,609,799 JC which claims benefit of 60/713,682 09/02/2005 JC ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/22/2009						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JASON CRAWFORD/</u> Examiner's Signature		☐ Met after Allowance JC Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 5	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS CYPRESS SEMICONDUCTOR CORPORATION 198 CHAMPION COURT SAN JOSE, CA 95134-1709 UNITED STATES						
TITLE CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	6	((power supply voltage) adj (island domain)) and logic and clock\$3 and (NAND NOR)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/08 09:11
L10	68	((power supply voltage) adj (island domain)) and logic and clock\$3).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/08 09:11
L9	190	((power supply voltage) adj (island domain)) and logic).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/08 09:11
L8	630	((power supply voltage) adj (island domain)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/08 09:10
L7	10	("20020089362" "20060156205" "5574753" "6154509" "6292016" "6927604" "7042263" "7079575" "7231009" "7365580").PN.	US-PGPUB; USPAT	OR	ON	2010/03/08 09:06
S117	1	S115 and clock\$3 and logic and ((power supply voltage) adj (island domain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 14:07
S116	0	S115 and clock\$3 and logic and ((power supply voltage) adj (island domain)) and (pll (phase adj lock\$3 adj loop\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 14:07

file:///C:/Documents%20and%20Settings/jcrawford/My%20...7477/EASTRIP-2025-01171771necr Technologies Americas Corp. v. MOSAID Technologies Inc.

S107	107	S105 and logic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:13
S106	105	S105 and logic	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 11:13
S105	159	S104 not print\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:12
S104	232	S103 not silverbrook.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:12
S103	299	S102 and @ad<"20050902"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:11
S102	457	(pll (phase adj lock\$3 adj loop\$3)) and ((power supply voltage) adj (domain island))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:11
S101	5	S100 and @ad<"20050902"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:09
S100	6	("20080030254" "6523150" "6584596" "6631502" "7088131" "7131074").PN. OR ("7511528").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 11:07
S99	6	S97 not S98	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:07

S98	3	S97 and @ad<"20050902"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:07
S97	9	(crawford-jason).xa. and ((power supply voltage) adj2 (domain island))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 11:06
S96	10	("20030189451" "5396527" "5504441" "5675263" "5701093" "5841299" "5986476" "6009021" "6433586" "7005893").PN. OR ("7355454").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 11:06
S95	7	S94 not (S89 S90 S83)	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 10:59
S94	9	S93 and "326"/\$.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 10:59
S93	110	S92 and logic	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 10:59
S92	142	S91 and @ad<"20050902"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 10:59
S91	324	((power supply voltage) adj2 island) and clock\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 10:58
S90	47	S89 not S83	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 10:57
S89	68	S88 and "326"/\$.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 10:57
S88	736	S87 and logic	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 10:57
S87	1040	S86 and @ad<"20050902"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 10:57

S86	1692	((power supply voltage) adj2 domain) and clock\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 10:57
S85	4	("20030094988" "6046604" "6441670" "6879191").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 10:56
S84	0	(11/171758).APP.	USPAT; USOCR	OR	ON	2010/03/05 10:53
S83	22	S82 and @ad< "20050902"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 10:51
S82	48	(326/63,68,80-81.ccls.) and ((power supply voltage) adj2 domain) and clock\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 10:51
S81	18	S80 not (S74 S75)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 09:39
S80	18	(326/21-22,29.ccls. 327/99,147,407-408.ccls. 375/371,376.ccls. 713/400-401,500-503,600-601.ccls.) and S79	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 09:39
S79	536	S78 and @ad< "20050902"	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 09:39
S78	828	S77 and logic and clock\$3	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 09:38
S77	2472	(power supply) adj2 domain	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 09:38
S76	0	S75 not S74	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 09:37

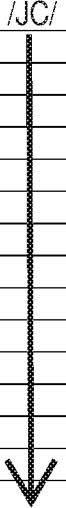
S75	16	("20020089362" "20040120087" "20060156205" "5045714" "5574753" "6154509" "6208193" "6239646" "6292016" "6385214" "6927604" "7042263" "7069458" "7079575" "7231009" "7365580").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 09:37
S74	16	("20020089362" "20040120087" "20060156205" "5045714" "5574753" "6154509" "6208193" "6239646" "6292016" "6385214" "6927604" "7042263" "7069458" "7079575" "7231009" "7365580").PN. OR ("7609799").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/05 08:58
S73	2	"20100026345".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 08:34
S72	5	"7609799".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/05 08:25

EAST Search History (Interference)

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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known		
				Application Number	Not yet assigned	
				Filing Date	Herewith	
				First Named Inventor:	Gabriel Li	
				Art Unit	Not yet assigned	
Examiner Name	Not yet assigned					
Attorney Docket Number	CD05110C					
U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US-	2006/0156205	7/06	Tomita	
		US-	2002/0089362	7/02	Lutkemeyer	
		US-	7,365,580	4/08	Martin et al.	
		US-	7,231,009	6/07	Kim et al.	
		US-	7,079,575	7/06	Ho et al.	
		US-	7,042,263	5/06	Johnson et al.	
		US-	6,927,604	8/05	Boerstler et al.	
		US-	6,154,509	11/00	Bishop	
		US-	6,292,016	9/01	Jefferson et al.	
		US-	5,574,753	11/96	Vartti et al.	
		US-	5,045,714	9/3/91	Park et al.	
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	US	2004/0120087	6/24/04	Ishii		

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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
/JC/		EP	1017193		7/5/00	TriQuint Semiconductor		
/JC/		EP	1187382		3/13/02	Agilent Technologies		

Examiner Signature	/Jason Crawford/ (03/04/2010)	Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Examiner Signature	/Jason Crawford/ (03/04/2010)	Date Considered	
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¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English Translation is attached.
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JC/
 MOSAID Technologies Inc., Exhibit 2023
 Based on Form PTO/SB/08B (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03. Page 2023 - 137
 IPR2025-01171, Infineon Technologies Americas Corp. v. MOSAID Technologies Inc.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/577,477	10/12/2009	Gabriel Li	CD05110C

CONFIRMATION NO. 4345

PUBLICATION NOTICE



OC000000040025864

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

Title:CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

Publication No.US-2010-0026345-A1

Publication Date:02/04/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/577,477	10/12/2009	Gabriel Li	CD05110C

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

CONFIRMATION NO. 4345
POA ACCEPTANCE LETTER



Date Mailed: 10/28/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/12/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tha/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/577,477	10/12/2009	2819	1090	CD05110C	20	3

CONFIRMATION NO. 4345

60909
CYPRESS SEMICONDUCTOR CORPORATION
198 CHAMPION COURT
SAN JOSE, CA 95134-1709

FILING RECEIPT



OC000000038414673

Date Mailed: 10/28/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Gabriel Li, San Francisco, CA;

Assignment For Published Patent Application

Cypress Semiconductor Corp., San Jose, CA

Power of Attorney: The patent practitioners associated with Customer Number 60909

Domestic Priority data as claimed by applicant

This application is a CON of 11/468,195 08/29/2006 PAT 7,609,799
which claims benefit of 60/713,682 09/02/2005

Foreign Applications

If Required, Foreign Filing License Granted: 10/22/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/577,477**

Projected Publication Date: 02/04/2010

Non-Publication Request: No

Early Publication Request: No

Title

CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

Preliminary Class

326

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not yet assigned
				Filing Date	Herewith
				First Named Inventor:	Gabriel Li
				Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	1	of	2	Attorney Docket Number	CD05110C

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US-	2006/0156205	7/06	Tomita	
		US-	2002/0089362	7/02	Lutkemeyer	
		US-	7,365,580	4/08	Martin et al.	
		US-	7,231,009	6/07	Kim et al.	
		US-	7,079,575	7/06	Ho et al.	
		US-	7,042,263	5/06	Johnson et al.	
		US-	6,927,604	8/05	Boerstler et al.	
		US-	6,154,509	11/00	Bishop	
		US-	6,292,016	9/01	Jefferson et al.	
		US-	5,574,753	11/96	Vartti et al.	
		US-	5,045,714	9/3/91	Park et al.	
		US-	6,239,646	5/29/01	Navabi et al.	
		US-	6,208,193	3/27/01	Moyal et al.	
		US-	6,385,214	5/7/02	Kikuchi et al.	
		US-	7,069,458	6/27/06	Sardi et al.	
		US	2004/0120087	6/24/04	Ishii	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³	Number ⁴ Kind Code ⁵ (if known)			
		EP	1017193	7/5/00	TriQuint Semiconductor	
		EP	1187382	3/13/02	Agilent Technologies	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language translation is attached.

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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER		
First Named Inventor/Applicant Name:		Gabriel Li		
Filer:		Daniel E. Ovanezian/Juanita Briscoe		
Attorney Docket Number:		CD05110C		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt

EFS ID:	6244522
Application Number:	12577477
International Application Number:	
Confirmation Number:	4345
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
First Named Inventor/Applicant Name:	Gabriel Li
Customer Number:	60909
Filer:	Daniel E. Ovanezian/Juanita Briscoe
Filer Authorized By:	Daniel E. Ovanezian
Attorney Docket Number:	CD05110C
Receipt Date:	12-OCT-2009
Filing Date:	
Time Stamp:	16:20:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	CD05110C_ADS.pdf	48898 7ddb7947e72b14363d3a7f49004c3540935ad70e	no	4

Warnings:

Information:

MOSAID Technologies Inc., Exhibit 2023

Page 2023 - 147

This is not an USPTO supplied ADS fillable form					
2		CD05110C_Continuation_Application.pdf	89367 2d8b17d31a4f6bac047436790d1b10494e662649	yes	22
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	17	
	Claims		18	21	
	Abstract		22	22	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	CD05110C_P687C_Drawings.pdf	51973 502640d37cc9eed947b53ef0c1673c2306f67be	no	5
Warnings:					
Information:					
4	Oath or Declaration filed	CD05110_Declaration.pdf	41733 96e8ceefe7ea4833fddd15c37641372c3341671d	no	1
Warnings:					
Information:					
5	Power of Attorney	CD05110C_P687C_POA.pdf	149233 1f017fadcd04840e9dc852bfd8bdcf79ba36d1e65	no	3
Warnings:					
Information:					
6	Transmittal Letter	CD05110C_IDS.pdf	25311 5585d3cf1fc94b2d4c0639cb90a052456d605467	no	3
Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Filed (SB/08)	CD05110C_1449.pdf	63046 e7a44a6fcc3ddda10177b9d68bc9c3bde8f31b92	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
8	Fee Worksheet (PTO-875)	fee-info.pdf	33305 80b6cd149f4bf5add2f9afb4f9175ae4ecedb450	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	502866
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	CD05110C
		Application Number	
Title of Invention	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Gabriel		Li		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	San Francisco	State/Province	CA	Country of Residence	US
Citizenship under 37 CFR 1.41(b)		US			
Mailing Address of Applicant:					
Address 1	359 22nd Avenue				
Address 2					
City	San Francisco	State/Province	CA		
Postal Code	94121	Country	US		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	60909		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER		
Attorney Docket Number	CD05110C	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)		Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	CD05110C
		Application Number	
Title of Invention	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER		

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	60909		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	11468195	2006-08-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	non provisional of	60713682	2005-09-02
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
Remove			
Application Number	Country ¹	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	CD05110C
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**CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING
SIGNALS WITH REDUCED JITTER**

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CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER

RELATED APPLICATIONS

5 This application is a continuation of Application No. 11/468,195, filed August 29, 2006,
which claims the benefit of U.S. Provisional Application No. 60/713,682, filed September 2,
2005.

BACKGROUND OF THE INVENTION

10 1. Field of the Invention

 This invention relates to electronic circuits and, more particularly, to circuits for
multiplexing signals from clock or data sources.

15 2. Description of the Related Art

 The following descriptions and examples are given as background only.

20 Many electronic systems include one or more synchronous components that rely on
receiving related signals at substantially the same time to maintain proper operating
characteristics of the electronic system. A computer system is one example of a synchronous
system that may include a multitude of interrelated system components, each designed to perform
a particular operation in response to a clock signal. In some cases, data transfer between system
25 components may be synchronized by one or more clock signals originating from a common
source. The system components may receive the clock signals through a clock network, which
may include clock generation and distribution circuits.

 In some cases, clock generation may be accomplished by manipulating the output of a

source, such as a crystal oscillator, to generate a plurality of clock signals in accordance with the needs of the various components within the computer system. The generated clock signals may then be fanned out to the system components via a clock distribution network. In an ideal situation, the generated clock signals may be received by each of the system components at substantially the same time. In practice, however, timing delays and uncertainties of clock signal generation and distribution may cause one or more system components to receive clock signals at slightly different instances. In some cases, even the smallest variation in the arrival of a clock signal transition relative to a data signal transition may significantly impact system performance and/or reliability. For this reason, good clock distribution is very important to the overall performance and reliability of electronic systems. Unwanted clock skew and jitter are two phenomena that may result from poor clock distribution, thus causing problems in the design and operation of the electronic systems.

As used herein, the term “skew” may be described as a variation in the arrival times of two related signals, which are specified to arrive at the same time. For example, “clock skew” may occur when an active “transition” or “edge” of the clock signal “lags” (i.e., arrives sometime after) or “leads” (i.e., arrives sometime before) the data signal transition(s) received by a system component. Clock skew may be introduced into a clock network through load mismatches, routing parasitics (i.e., interlayer dielectric thickness, interconnect thickness and channel length mismatches), and/or variations in temperature, voltage, and process (i.e., trace conductor length, width, and composition mismatches, capacitive loading, etc.).

Unfortunately, clock skew may adversely affect the timing margins of one or more components within a synchronous system. For example, it is often necessary to properly align the clock signal to the data being sampled at the input latches of a system component to achieve synchronous operation. Such alignment may ensure that the data transition occurs at the proper moment between the edges or active transitions of the clock signal. Synchronous systems, therefore, generally rely on data transitioning and remaining stable from a time, which occurs at least a “setup time” before the clock transition, until at least a “hold time” after the clock

transition. Most synchronous system components have stringent setup and hold timing requirements, which are typically specified by a manufacturer of the system component.

As operating speeds increase, the setup and hold timing margins between active transitions of the clock and data signals are reduced, thereby decreasing the window within which a data transition can be successfully latched by a clock transition. For example, edge-sensitive flip-flops may be used for sampling data signals received by a system component. In such an example, a flip-flop may successfully latch a data signal if the data signal is stable during the critical setup and hold periods on either side of the clock transition. However, if clock skew occurs, it may shift the clock transition sufficiently in time to cause a bit error when the data is sampled. As described herein, a “bit error” is a sampling error that occurs when a data signal is incorrectly sampled by a clock transition.

Jitter, on the other hand, generally results from time-varying components of noise sources, and is often defined as the cycle-to-cycle variation in the threshold crossings of a data signal. In other words, jitter may occur in data samples taken near, but not exactly at, the desired sample locations of an individual data signal, such that a sample is temporally displaced by an unknown, though usually small interval (e.g., an interval substantially less than or equal to one clock cycle). Like clock skew, jitter may cause the data signal to be shifted sufficiently in time to produce a bit error when the data signal is incorrectly sampled by the clock signal.

Techniques have been developed to minimize the effects of timing delays, such as clock skew and jitter, which degrade the performance and reliability of synchronous systems. However, most currently used techniques cannot guarantee that a data signal transition will occur at the critical moment between clock signal edges in all conditions. For example, some techniques utilize phase lock loops (PLLs) or delay-locked loops (DLLs) for adding a somewhat variable, though highly consistent amount of delay to a clock path. The added delay may be used to adjust the active edge of a clock signal before it is used for sampling a data signal. As such, a PLL or DLL device could be used to reduce clock skew by adjusting the timing of the clock

signal, so that it occurs within the data setup and hold time requirements of a system component. However, the current techniques are not without some disadvantages.

In some cases, more than one PLL or DLL device may be included within a clock network for adjusting the timing of the clock path. Multiple PLL/DLL devices enable the system to multiplex clock signals from different PLL/DLLs. For example, a multiplexer circuit may be included for selectively applying one of the PLL/DLL output signals to the clock path. However, conventional multiplexer designs add crosstalk and power supply noise to the clock path when multiplexing signals (i.e., choosing between more than one signal) from the PLL/DLLs.

The addition of crosstalk and power supply noise increases the amount of jitter on the clock path, and therefore, is very undesirable in clock networks. In some cases, the amount of jitter added to the clock path may cause a bit error when the generated clock signal is used for sampling data. Therefore, a need remains for an improved clock network that does not suffer from crosstalk or supply noise injection. Such a clock network may experience significantly less jitter than conventional networks, thereby improving the overall timing of an electronic device employing the clock network.

SUMMARY OF THE INVENTION

The following description of various embodiments of circuits, systems and methods is not to be construed in any way as limiting the subject matter of the appended claims.

5

According to one embodiment, an improved multiplexer circuit comprising a plurality of logic gates and a logic block is contemplated herein. For example, the improved multiplexer circuit may include a first logic gate coupled for receiving a first signal, a second logic gate coupled for receiving a second signal, and a third logic gate coupled to outputs of the first and
10 second logic gates for transmitting either the first signal or the second signal. For example, the logic block may be configured for deactivating one of the first and second signals by supplying a static control signal to the first and second logic gates. The logic block ensures that only one active signal (e.g., either the first signal or the second signal) is supplied to the inputs of the first, second and third logic gates. This reduces the amount of jitter within the transmitted signal by
15 eliminating crosstalk and power supply noise injection at the inputs of the logic gates.

In some cases, jitter may be further reduced by arranging the logic gates within separate power domains to further isolate the logic gate inputs. For example, the first, second and third logic gates may be separated from one another by arranging the logic gates within different power supply “islands,” each coupled to a different power bus. The common substrate provides
20 an additional amount of isolation. For example, a relatively high substrate resistance also functions to provide isolation between the power supply islands.

In some cases, the first, second and third logic gates may be implemented with NAND gates. However, the first, second and third logic gates are not limited to NAND gates, and may
25 be implemented with a substantially different combination of logic gates (e.g., NOR gates), in other embodiments of the invention. In some cases, the first and second signals may be clock signals. However, the first and second signals are not limited to clock signals, and may comprise data signals, in other embodiments of the invention.

A system comprising the improved multiplexer circuit and at least one system component is also contemplated herein. As noted above, the multiplexer circuit may include at least three logic gates and a logic block, each arranged within a separate power domain. For example, a first logic gate may be coupled for receiving a first signal, and a second logic gate may be coupled for receiving a second signal. However, a third logic gate may be coupled for receiving only one of the first and second signals, depending on a state of a control signal supplied to the first and second logic gates from the logic block. In this manner, the at least one system component may be coupled to an output of the third logic gate for receiving only one of the first and second signals.

In some cases, the multiplexer circuit may be part of a clock network, which is included within the system for adjusting the timing of a clock path. For example, the first and second signals may include clock signals supplied, e.g., from an internal system clock. In some cases, the clock network may include one or more phase shift apparatuses for supplying the first and second signals to the multiplexer circuit. For example, a phase locked loop (PLL) or delay locked loop (DLL) device may be included within the clock network for reducing clock skew by shifting a phase of the system clock signals. However, a phase shift apparatus may not be included within all embodiments of the invention.

A method for multiplexing signals with reduced jitter is also contemplated herein. For example, the method may include supplying a first signal to a first logic gate and a second signal to a second logic gate. Next, one of the first or second signals may be deactivated by supplying a control signal to the first and second logic gates. Finally, the method may include forwarding an active one of the first or second signals to a third logic gate. By supplying only one active signal to each of the logic gates, the steps of deactivating and forwarding enable the first and second signals to be multiplexed with reduced jitter.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

5

FIG. 1 is block diagram of a circuit comprising an exemplary multiplexer circuit,

FIG. 2 is a circuit diagram of an exemplary multiplexer circuit;

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FIG. 3 is a block diagram of a circuit comprising an improved multiplexer circuit having reduced crosstalk and power supply noise, according to one embodiment of the invention;

FIG. 4 is a block diagram of a circuit comprising an improved multiplexer circuit having reduced crosstalk and power supply noise, according to another embodiment of the invention;

15

FIG. 5 is a block diagram of a system comprising the improved multiplexer of FIGS. 3 or 4 and a plurality of system components; and

20

FIG. 6 is a flowchart diagram of a method for multiplexing signals with reduced crosstalk and power supply noise.

25

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

An exemplary clock network 100 is shown in FIG. 1. In the illustrated embodiment, the clock network includes a first PLL 110, a second PLL 120, a multiplexer 130, a logic block 140 and an output buffer 150. In some cases, the first and second PLLs may each be configured for generating one or more clock signals (e.g., signals A and B) for adjusting the timing of a clock path (coupled, e.g., to CLKout). In FIG. 1, the clock signals generated by the PLLs are supplied to the inputs of a multiplexer (130). The logic block supplies a control signal to the multiplexer for selecting one of the clock signals to be output from the multiplexer. In most cases, the chosen clock signal (out) is supplied to the output buffer, before it is applied to the clock path.

The clock network shown in FIG. 1 adds crosstalk and power supply noise to the clock path when multiplexing signals (i.e., choosing between more than one signal) from the PLLs. As described in more detail below, the addition of crosstalk and power supply noise increases the amount of jitter on the clock path, and thus, is very undesirable.

In some cases, crosstalk and power supply noise may be added to the clock path when two or more PLL signals are brought into close proximity at the inputs of the multiplexer. For example, a clock signal (A) from the first PLL may interfere with a clock signal (B) from the second PLL by way of capacitive coupling between the metal wire of the mux inputs and the common silicon substrate. This interference (or “crosstalk”) cannot be avoided in current multiplexer designs, due to the close proximity of the mux inputs. As described herein, circuit components arranged in “close proximity” may be located within the same “power domain” and/or coupled to the same power bus.

For example, FIG. 2 illustrates one embodiment of a multiplexer circuit (130) that may be included within the clock network (100) of FIG. 1. In the illustrated embodiment, multiplexer 130 includes a pair of two-input AND gates (200, 210), a two-input NOR gate (220) and a 1-to-2 decoder (230). Each of the AND gates is coupled for receiving a clock signal (e.g., either A or B) from the first and second PLLs (110, 120) and a select signal (e.g., either S1 or S2) from the

1-to-2 decoder (230). The AND gate outputs are coupled to the inputs of the NOR gate for generating the multiplexer output signal (out). Each of the multiplexer components is supplied with the same power bus (e.g., pwr2).

5 The multiplexer circuit shown in FIG. 2 adds crosstalk to the clock path when multiplexing clock signals A and B, due to the close proximity of the clock signals at the inputs of the multiplexer. In other words, AND gates 200 and 210 are each configured for receiving an active clock signal from the PLLs. Because the AND gates are arranged relatively close to one another, the clock signals may interfere with one another via capacitive coupling between the
10 AND gate inputs and the common substrate.

Power supply noise from the clock network components may also be shared at the inputs of the multiplexer. For example, one or more of the clock network components may be supplied with a separate power bus, as shown in FIG. 1. In the particular embodiment shown, the first
15 PLL is supplied with a first power bus (pwr1), the second PLL and the multiplexer are supplied with a second power bus (pwr2), the logic block is supplied with a third power bus (pwr3) and the output buffer is supplied with a fourth power bus (pwr4). In this manner, the first PLL, the second PLL, the logic block and the output buffer may each be implemented within a separate “power domain,” “power supply island,” or “power supply block.” It is noted that, although
20 multiplexer 130 is located with the second power supply block, it can be located within any supply block and still exhibit the following problem.

All power supplies generate some amount of noise, which propagates along the power bus as “power supply noise.” Power supply noise affects circuit components by contributing to
25 the overall noise level of the output signals generated by the components. In some cases, the noise contributions from each power domain may be combined when the output signals from multiple circuit components come in close proximity to one another (e.g., when multiplexing signals). In the embodiment of FIG. 1, the clock signals from the first and second PLLs and the control signal from the logic block contain power supply noise from power buses 1, 2 and 3. As
30 described in more detail below, the supply noises from power buses 1, 2 and 3 are combined

within the multiplexer, and pass directly to the output buffer in the fourth power domain. The fourth power domain contributes its own amount of noise, so that the final signal (CLKout) from the output buffer contains noise components from all four power domains.

5 The multiplexer circuit shown in FIG. 2 adds power supply noise to the clock path by arranging the multiplexer components within close proximity to one another and supplying active clock and control signals to the closely spaced components. This enables the noise components of one signal to interfere (or combine) with those of another signal. Since the active clock and control signals contain supply noises from power domains 1, 2 and 3, the supply noises from
10 each of these domains are combined within the multiplexer output signal (out). If the output signal is forwarded to a buffer located within another power domain (as shown in FIG. 1), the final signal (CLKout) will contain noise components from four distinct power domains.

In some cases, the amount of crosstalk and power supply noise added to the clock path may cause a bit error when the final signal (CLKout) is used for sampling data. Therefore, a
15 need remains for an improved clock network that does not suffer from crosstalk or supply noise injection. Such a clock network would experience significantly less jitter than currently available clock networks, thereby improving the overall timing of an electronic device employing the clock network.

20 One embodiment of an improved clock network 300 is shown in FIG. 3. As described in more detail below, the illustrated embodiment provides a solution for reducing the cycle-to-cycle jitter of a multiplexed (“muxed”) clock output by eliminating crosstalk and power supply noise injection between the muxed signals.

25 As shown in FIG. 3, the improved clock network (300) may include a first phase shift apparatus (PS1) 310 and a first NAND gate in a first power supply domain (PSD 1), a second phase shift apparatus (PS2) 320 and a second NAND gate in a second power supply domain (PSD 2), a logic block 340 in a third power supply domain (PSD 3), and a third NAND gate and output buffer 350 in a fourth power supply domain (PSD 4). In some cases, the phase shift
30 apparatuses may be implemented with a phase locked loop (PLL) or delay locked loop (DLL)

device. As such, the phase shift apparatuses may be included for adding a variable, though highly consistent amount of delay (i.e., phase shift) to the clock signals (CLK_{in1} , CLK_{in2}) supplied thereto. It is noted, however, that PS1 and PS2 may not be included in all embodiments of the invention. In some cases, the clock signals (CLK_{in1} , CLK_{in2}) from a clock source (such as, e.g., a crystal oscillator or external clock source) may be supplied directly to the inputs of the first and second NAND gates.

As used herein, a component may be arranged within a separate “power domain,” if that component is supplied with its own power bus and physically separated from components arranged in other power domains. For example, NAND gates 1, 2 and 3 are each arranged within a different power domain. As shown in FIG. 3, NAND gates 1, 2 and 3 are spaced apart from one another and supplied with a different power bus (e.g., pwr1, pwr2, or pwr3). In some cases, the NAND gates may be located in different supply islands, which are separated from each other by a physical distance. In some cases, the supply islands may include supply guard rings for further isolation.

In some cases, the logic gates may be implemented with two-input NAND gates, as shown in FIG. 3. In the illustrated embodiment, the output of the first phase shift apparatus is coupled to a first input of NAND gate 1 for supplying a phase-shifted clock signal (A) thereto. The second phase shift apparatus is similarly coupled for supplying another phase-shifted clock signal (B) to a first input of NAND gate 2. The first and second NAND gates are controlled by the logic block (340) in the third power supply domain. For example, the logic block is coupled for supplying a pair of control signals (cntl 1, cntl 2) to the second inputs of NAND gates 1 and 2. As described in more detail below, the control signals may eliminate crosstalk and power supply noise injection by deactivating one of the clock signals supplied to NAND gates 1 and 2. The outputs of NAND gates 1 and 2 are coupled to the inputs of NAND gate 3 in the fourth power supply domain. In some cases, the output (out) of the third NAND gate may be coupled to a buffer circuit (350), which may also be arranged in the fourth power supply domain. However, the buffer circuit may not be included in all embodiments of the invention. In some cases, the

output of the third NAND gate may be directly coupled to an internal system clock path (*see*, FIG. 5).

As shown in FIG. 3, the functionality of the multiplexer is broken up into three NAND gates, each spaced apart from one another and arranged within a separate power domain. A logic block (340), arranged within another power domain, is coupled to the first and second NAND gates for eliminating the crosstalk and supply noise created within typical multiplexer circuits. For example, the logic block is configured for supplying static control signals (either a logic 1 or logic 0) to the first and second NAND gates. Although actively switching clock signals (A and B) are supplied to the first inputs of NAND gates 1 and 2, the outputs of the NAND gates are only allowed to switch when a logic 1 control signal is supplied to the second input of the logic gate. In order to eliminate crosstalk and supply noise, only one of the first and second NAND gates is allowed to pass the actively switching clock signal. The output of the other NAND gate is rendered static by supplying a logic 0 control signal to the second input of that logic gate. Since the static signal injects no switching noise, the inputs of the NAND gates are isolated from one another.

Therefore, the improved solution shown in FIG. 3 operates by separating the multiplexing (MUX) function into three separate logic gates and distributing them across three distinct power domains. The theory of the operation is to allow only one switching input per logic gate. The control signals supplied to the first and second logic gates are static signals with one high and the other low. Instead of supplying two actively switching clock signals to the third logic gate, the control signals are used for deactivating one of the clock signals in its own power domain. This enables the invention to eliminate all crosstalk and supply noise injection at the inputs of the logic gates.

Various advantages are provided by the improved solution shown in FIG. 3. For example, crosstalk and supply noise injection are eliminated by: (i) separating the multiplexing (MUX) function into three separate logic gates distributed across three distinct power domains, and (ii) allowing only one switching input per logic gate. In other words, cross talk and supply

noise injection are eliminated since each clock signal is gated in its own power domain. The improved solution improves the cycle-to-cycle jitter of the multiplexed clock output by reducing crosstalk and supply noise injection. In addition, the improved solution provides built in delay matching by utilizing three substantially identical logic gates (e.g., NAND gates 1, 2, and 3).

5 These features are generally desirable for customers/users.

In some cases, the improved solution shown in FIG. 3 may be used in clock or other timing generation devices. Such devices are widely used in many types of electronic devices, including motherboards in personal computers and communications equipment, and in consumer
10 devices such as cell phones, digital cameras, MP3 players, and many other home and entertainment products.

In some cases, the improved solution may include a phase shift apparatus (such as a PLL or DLL) for eliminating clock skew before the clock signals are supplied to the first and second
15 logic gates. For example, phase lock loops may be used in certain applications, such as frequency synthesizers, to reduce the lock time. For example, when frequency hopping is used in modern wireless networks (e.g., 3G cellular, WCDMA, WLAN, and Bluetooth), the time to settle is considered “dead time” where no information is transmitted, and thus time is wasted. Speeding up the lock time increases the effective data rate, and thus, the value of such networks.
20 Another example would be in wireline networks, where a reduced lock time helps to minimize the amount of data lost. That is, if a long string of zeros or ones is in the data path and the PLL loses lock, reacquiring lock sooner results in more data recovered by the CDR circuitry. Overall, phase lock loops are very important building blocks of modern electronic systems. It should be noted, however, that the improved multiplexer circuit described herein does not require the use of
25 a PLL to reap the advantages mentioned above. Although the phase shift apparatuses shown in FIG. 3 may further improve the timing of the clock path by reducing clock skew, they should be considered optional features of the invention.

In addition, the multiplexer circuit shown in FIG. 3 represents only one manner in which
30 signals may be multiplexed with reduced jitter. One skilled in the art would recognize that other

embodiments exist. For example, the clocking signals shown in FIG. 3 may be multiplexed with a substantially different combination of logic gates. In one embodiment, the NAND gates shown in FIG. 3 may be replaced with NOR gates. Other combinations of logic gates not specifically mentioned herein may also be possible. In addition to clocking signals, another multiplexer circuit is provided herein for multiplexing other system critical signals (such as data signals) with reduced cycle-to-cycle jitter. One embodiment of such a circuit is shown in FIG. 4 and described in more detail below.

According to one embodiment, multiplexer circuit 400 may include a first NAND gate in a first power supply domain (PSD 1), a second NAND gate in a second power supply domain (PSD 2), a logic block 440 in a third power supply domain (PSD 3), and a third NAND gate and (optional) output buffer 450 in a fourth power supply domain (PSD 4). As such, the multiplexer circuit (400) shown in FIG. 4 differs from the circuit (300) shown in FIG. 3 by eliminating the phase shift apparatuses and supplying a pair of data signals ($DATA_{in1}$, $DATA_{in2}$) to the first and second NAND gates. The multiplexer circuit (400) shown in FIG. 4 reduces cycle-to-cycle jitter of the multiplexed data signals by eliminating crosstalk and power supply noise injection, as described above. As noted above, the multiplexing function may be alternatively provided by NOR gates, or any other combination of logic gates arranged in separate power domains and supplied with only one actively switching input.

A system comprising the improved multiplexer circuit is also contemplated herein. In addition to other circuitry, the system may include a multiplexer circuit 500 and one or more system components 510, as shown in FIG. 5. In general, the multiplexer circuit 500 may be coupled for generating an output signal (OUT) by multiplexing one or more input signals (IN) supplied thereto. In most cases, the input signals may be clock or data signals. As such, multiplexer circuit 500 may be implemented with one of the circuits shown in FIGS. 3 and 4. As noted above, the multiplexer circuit may reduce the amount of jitter within the output signal by separating the multiplexing function into three logic gates, which are distributed across three distinct power domains. As such, multiplexer circuit 500 may be coupled to at least three different power buses (PWR). In some cases, the multiplexed output signal (OUT) may be

distributed to one or more system components 510, as shown in FIG. 5. If distributed along a clock path, the multiplexer circuit may be included within an improved clock network.

A method for multiplexing signals with reduced jitter is also contemplated herein. As shown in FIG. 6, for example, the method (600) may include supplying a first signal to a first logic gate (in step 610) and a second signal to a second logic gate (in step 620). As noted above, the first and second signals may be clock or data signals. In addition, the method may include deactivating one of the first or second signals (in step 630). For example, one of the signals may be deactivated by supplying a logic low control signal (NAND implementation) or a logic high control signal (NOR implementation) to the first and second logic gates. Next, the method may include forwarding an active one of the first or second signals to a third logic gate configured for outputting an active one of the first and second signals (in step 640).

The steps of deactivating and forwarding enable the first and second signals to be multiplexed with reduced jitter. For example, the method allows only one active signal to be supplied to each of the first, second and third logic gates. As noted above, the first and second logic gates are each configured for receiving an active clock (or data) signal and a static control signal. The third logic gate is configured for receiving only one input signal, the other input is disabled in the deactivation step. In this manner, the method described herein reduces jitter by eliminating crosstalk and power supply noise injection at the inputs of the logic gates. The logic gate inputs may be further isolated, in some embodiments, by separating the logic gates within distinct power domains. In other words, the logic gates may be physically separated and supplied with different power buses to further improve the isolation there between.

Embodiments of the present invention are well suited to performing various other steps or variations of the steps recited herein, and in a sequence other than that depicted and/or described herein. In one embodiment, the process of selecting one clock source from multiple clock sources may be carried out by processors and other electrical and electronic components. For example, a processor can select one pin to be the CPU clock or PCI Express clock.

For purposes of clarity, many of the details of the improved multiplexer circuit and the methods of designing and manufacturing the same that are widely known and are not relevant to the present invention have been omitted from the following description.

5 It should be appreciated that reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Therefore, it is emphasized and should be appreciated that two or more references to “an embodiment” or “one embodiment” or “an alternative embodiment” in various portions of this
10 specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined as suitable in one or more embodiments of the invention.

 Similarly, it should be appreciated that in the foregoing description of exemplary
15 embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims
20 reflect, inventive aspects may lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

5 a plurality of power supply domains; and

a plurality of logic components, each of the plurality of logic components within a different one of the plurality of power supply domains, wherein each of the plurality of logic components is configured to operate with a corresponding clock signal within a respective one of the plurality of power supply domains.

10 2. The apparatus of claim 1, wherein the plurality of power supply domains comprises at least three power supply domains and wherein the plurality of logic components comprise at least three logic components.

15 3. The apparatus of claim 2, wherein the plurality of power supply domains comprises first, second, third and fourth power supply domains, wherein a plurality of logic components comprises:

a first logic gate arranged within the first power supply domain and configured to operate with a first clock signal;

20 a second logic gate arranged within the second power supply domain and configured to operate with a second clock signal;

a logic block arranged within the third power supply domain and coupled to the first and second logic gates; and

a third logic gate arranged within the fourth power supply domain and coupled to the first and second logic gates.

4. The apparatus of claim 3, wherein the first, second and third logic gates each comprise
5 either a two-input NAND gate or a two-input NOR gate.

5. The apparatus of claim 3, wherein the first logic gate has a first input coupled to receive the first signal and second input coupled to receive a control signal from the logic block, wherein the second logic gate has a first input coupled to receive the second signal and a second input
10 coupled to receive the control signal from the logic block,

wherein the logic block is configured to supply the control signal to the first and second logic gates to deactivate one of the first and second signal, and

wherein the third logic gate has inputs coupled to receive outputs of the first and second logic gates and transmit either the first signal or the second signal, which has not been
15 deactivated by the logic block.

6. The apparatus of claim 1, wherein each of the plurality of power supply domains is supplied with its own power bus and physically separated from logic components arranged in other power supply domains.

7. The apparatus of claim 6, wherein each of the plurality of logic components are located in different supply islands comprising supply guard rings.

8. A multiplexer comprising the apparatus of claim 1.

9. A clock generation device comprising the apparatus of claim 1.

5 10. A motherboard comprising the clock generation device of claim 6.

11. A phone comprising the apparatus of claim 1.

12. A system, comprising:

10 a circuit comprising three logic gates and a logic block, each arranged within a separate power supply domain, wherein:

a first of the three logic gates is operatively coupled with a first signal;

a second of the three logic gates is operatively coupled with a second signal; and

a third of the three logic gates operatively coupled with one of the first and second

15 signals, depending on a state of a control signal; and

a system component coupled to the third logic gate.

13. The system of claim 12, wherein the first, second and third logic gates each comprise either a NAND gate or a NOR gate.

20

14. The system of claim 12, wherein the first and second signals comprise clock signals.

15. The system of claim 12, further comprising one or more phase shift apparatuses coupled to the circuit.

16. The system of claim 15, wherein the one or more phase shift apparatuses each comprise either a phase locked loop (PLL) device or a delay locked loop (DLL) device.

17. The clock network comprising the system of claim 15.

18. A method, comprising:

deactivating one of a first signal or a second signal by supplying a control signal to first and second logic gates; and

forwarding an active one of the first or second signals to a third logic gate, wherein the first, second and third logic gates are spaced apart from one another and respectively arranged within a first, second and third power supply domain.

19. The method of claim 18, wherein the first and second signals comprise clock signals.

20. The method of claim 19, wherein the first and second signals comprise data signals.

ABSTRACT

An apparatus having a plurality of power supply domains and a plurality of logic components. Each of the plurality of logic components residing within a different one of the plurality of power supply domains. Each of the plurality of logic components is configured to operate with a corresponding clock signal within a respective one of the plurality of power supply domains.

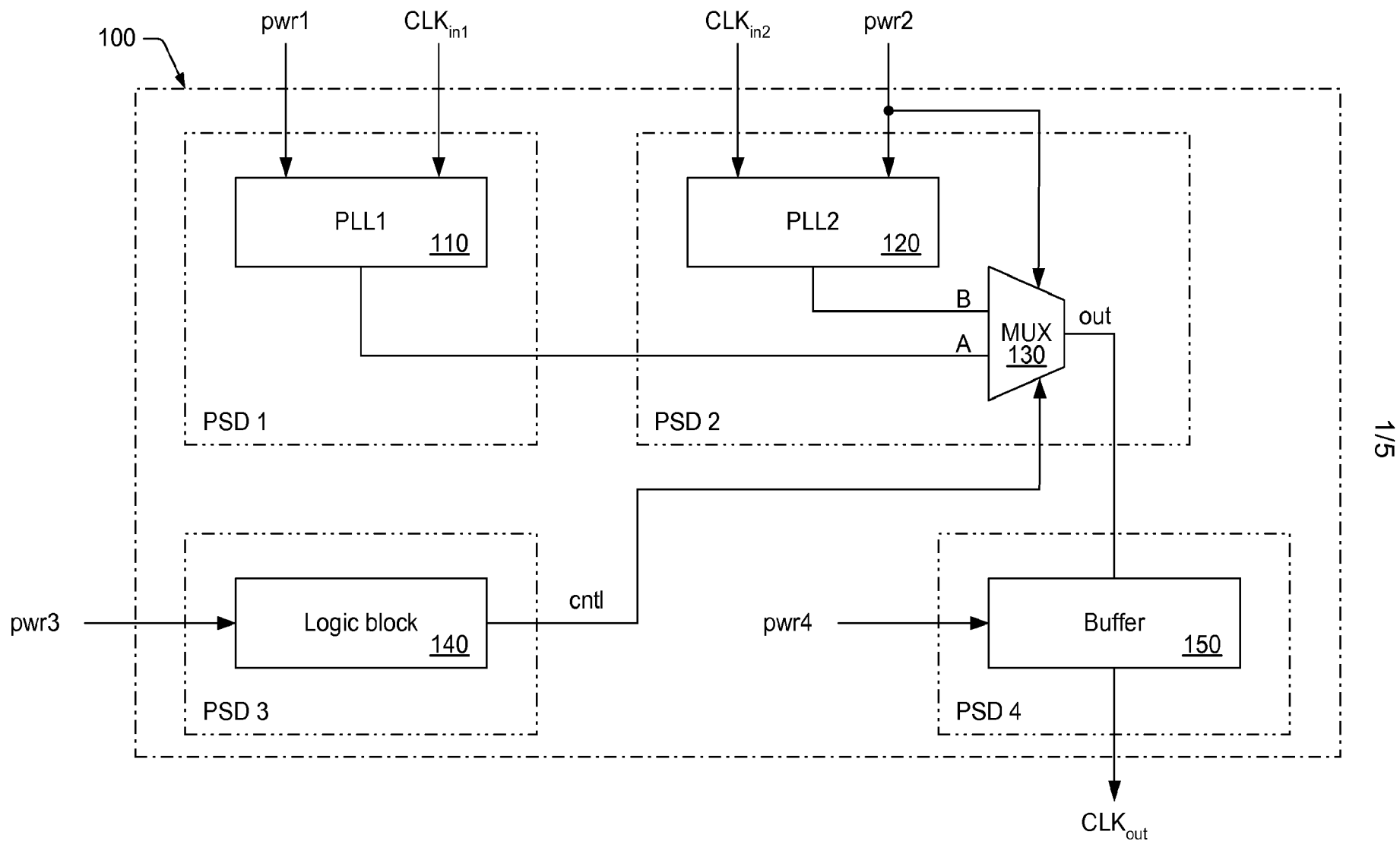
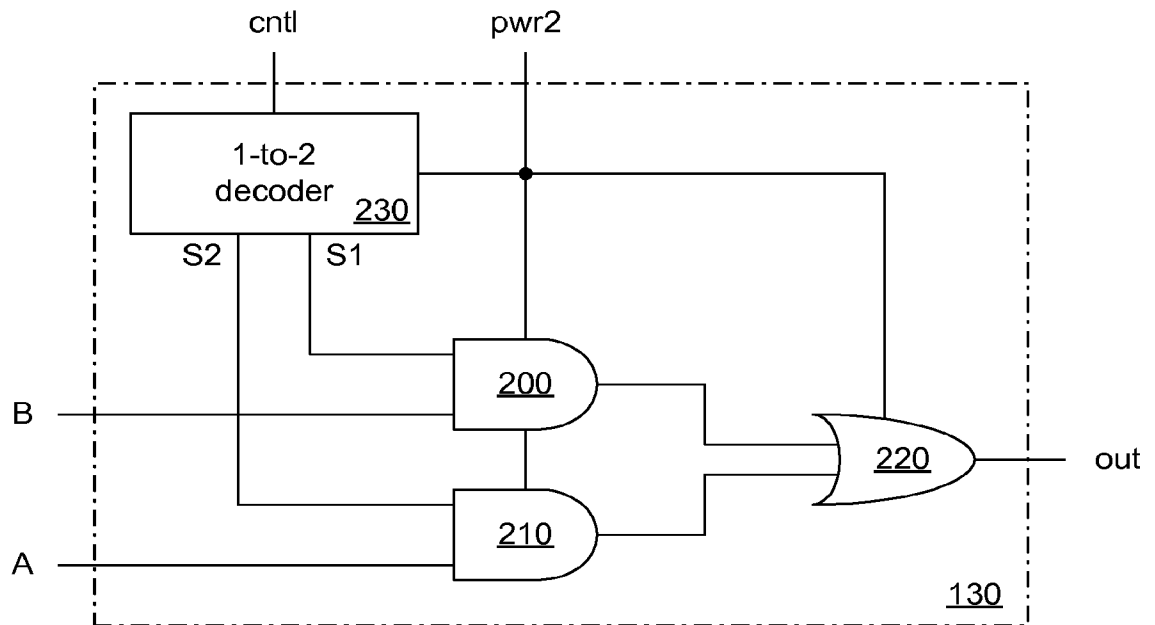
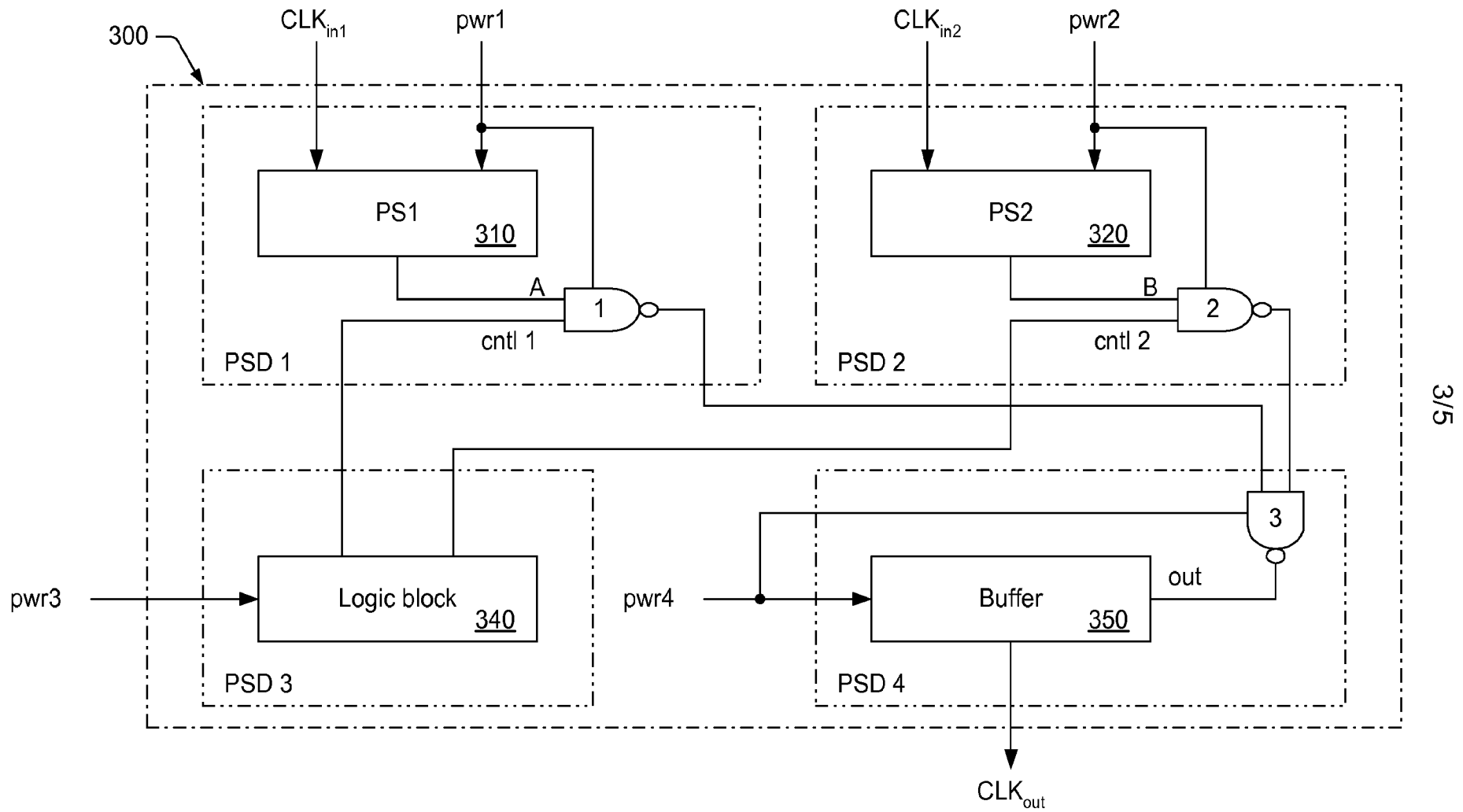


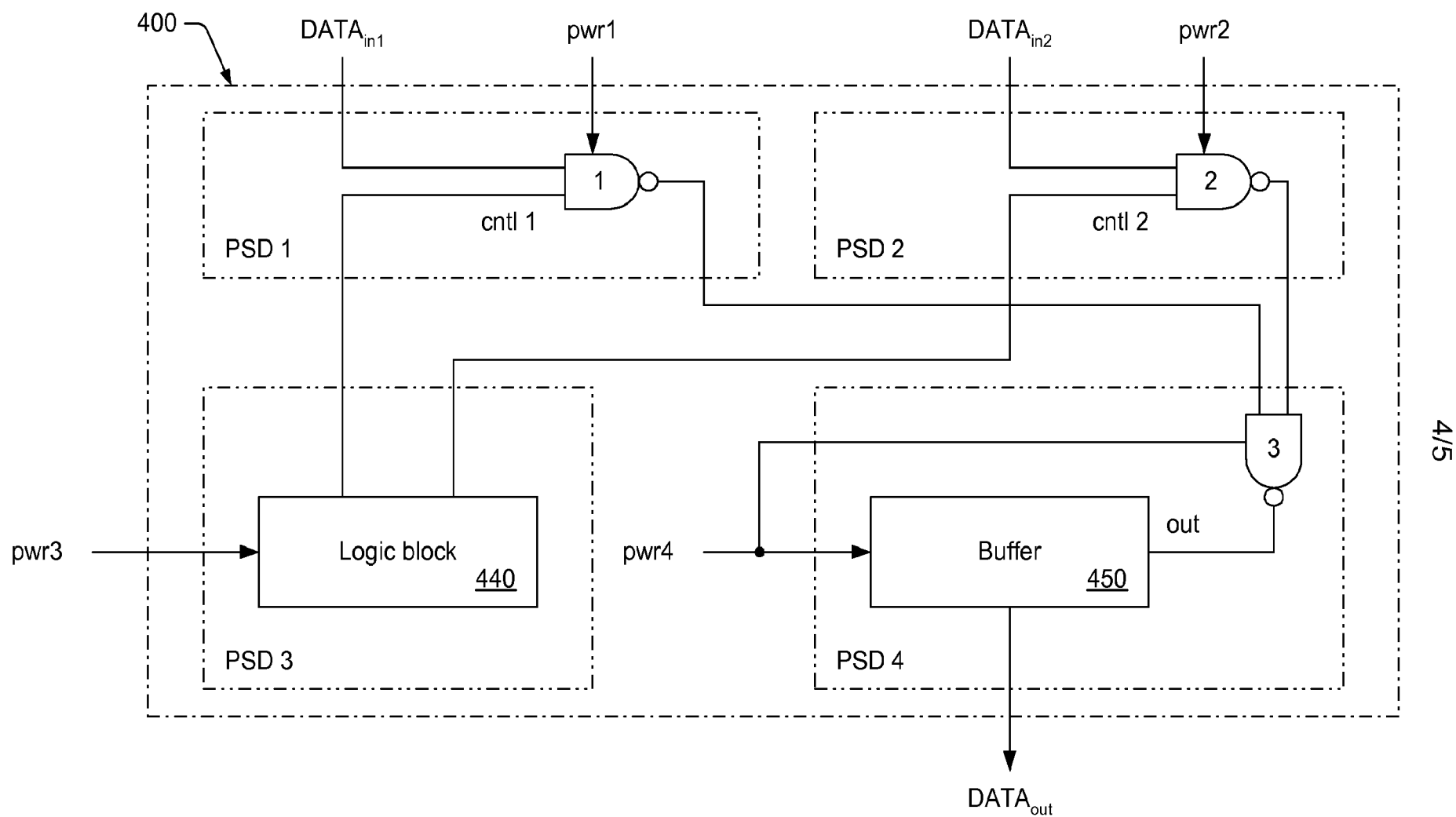
FIG. 1

**FIG. 2**



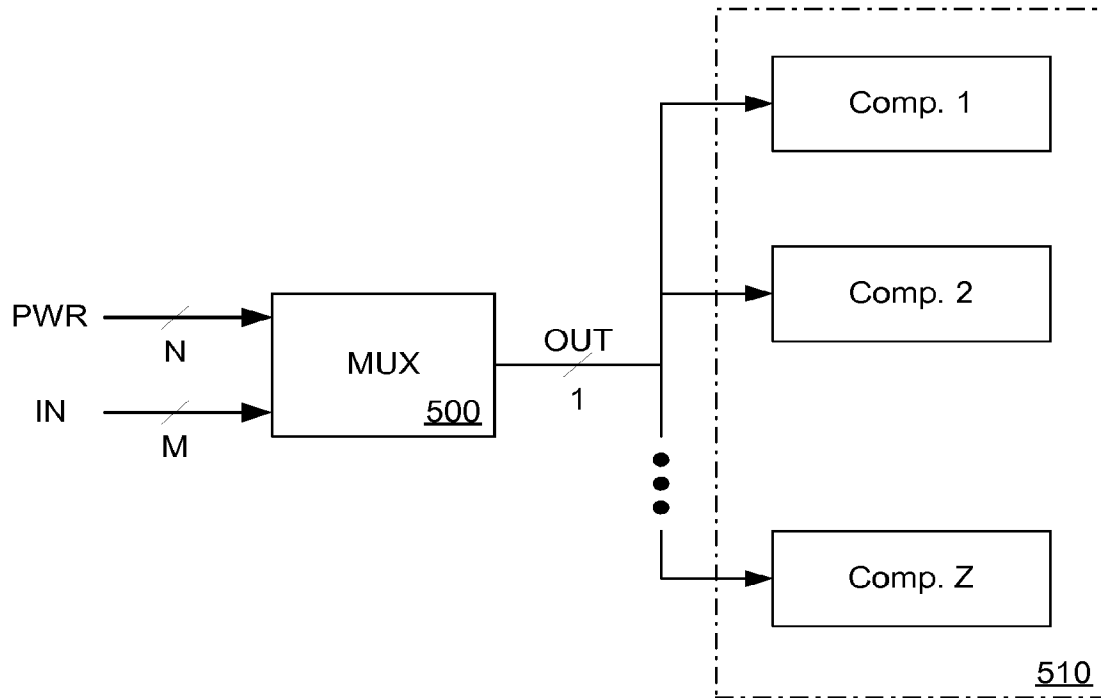
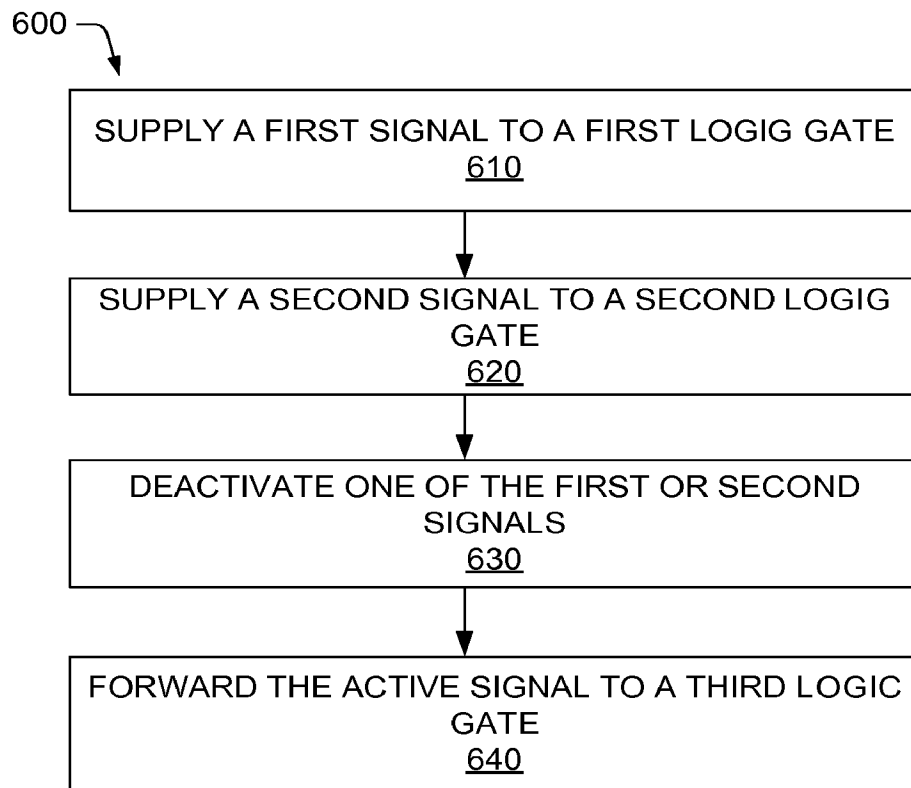
3/5

FIG. 3



4/5

FIG. 4

**FIG. 5****FIG. 6**

DECLARATION AND POWER OF ATTORNEY
FOR UTILITY APPLICATION USING AN APPLICATION DATA SHEET

As the below named inventor(s), I/we hereby declare that:

This declaration is directed to:

- ☒ The attached application entitled CIRCUIT, SYSTEM, AND METHOD FOR
MULTIPLEXING SIGNALS WITH REDUCED JITTER, or
☐ Application No. _____ filed on _____
☐ as amended on _____ (if applicable).

I/we believe I/we am/are the original first inventor(s) of the subject matter which is claimed
and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified specification,
including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the U.S. Patent and Trademark Office all
information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for
continuation-in-part applications, material information which became available between the filing
date of the prior application and the national or PCT International filing date of the continuation-in-
part application.

I hereby revoke any previous Powers of Attorney and appoint practitioners associated with
Customer Number:

35617

Please direct all communications to the address associated with Customer Number:

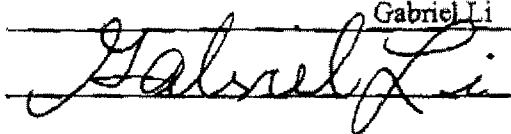
35617

I hereby declare that all statements made herein of my own knowledge are true and that all
statements made herein on information and belief are believed to be true; and further that these
statements were made with the knowledge that willful false statements and the like so made are
punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false
statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Full Name:

Gabriel Li

Inventor's Signature:



Date:

8-22-06

Citizen of:

USA

Attorney's Docket No. CD05110C

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:	)	
	)	
Gabriel Li	)	Examiner: Not yet assigned
	)	
Application No.: Not yet assigned	)	Art Unit: Not yet assigned
	)	
Filed: Herewith	)	
	)	
For: CIRCUIT, SYSTEM, AND	)	
METHOD FOR MULTIPLEXING	)	
SIGNALS WITH REDUCED	)	
JITTER	)	
	)	
	)	
a Continuation of	)	
	)	
Application No. 11/468,195	)	
	)	
Filed: 8/29/06	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

POWER OF ATTORNEY BY ASSIGNEE

Cypress Semiconductor Corp.

(Name of Assignee)

("assignee"), a company organized under the laws of the state of Delaware, having a
place of business at 198 Champion Court, San Jose, California 95134,

(Address)

hereby states that to the best of assignee's knowledge and belief it is the assignee of the entire
right, title, and interest in and to the above-referenced patent application and represents that the
undersigned is a representative authorized and empowered to sign on behalf of the assignee.

Upon information and belief, the assignment documents that evidence the placement of title in

the assignee are recorded in the U.S. Patent and Trademark Office on August 29, 2006 at Reel 018186 and Frame 0711.

Pursuant to 37 C.F.R. § 3.71, the assignee hereby appoints the practitioners associated with Customer Number 60909 as the assignee's respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Pursuant to 37 C.F.R. § 3.71, the assignee hereby states that prosecution of the above-referenced patent application is to be conducted to the exclusion of the inventor(s).

Assignee of Interest: Cypress Semiconductor Corp.
(Type or Print)
Dated: 10/09/2009 By: [Signature]
Name: Cathal Phelan
(Type or Print)

Title: Chief Technical Officer
(Type or Print)

Address of Assignee of Interest:
198 Champion Court
San Jose, California 95134

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: October 12, 2009 By /Daniel Ovanezian/
Name: Daniel E. Ovanezian
(Type)
Reg. No.: 41,236

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In Re Patent Application of:

Gabriel Li

Application No.: Not yet assigned

Filed: Herewith

Art unit: Not yet assigned

Examiner: Not yet assigned

For: CIRCUIT, SYSTEM, AND METHOD
FOR MULTIPLEXING SIGNALS WITH
REDUCED JITTER

a Continuation of

Application No.: 11/468,195

Filed: 8/29/06

Confirmation No.: Not yet assigned

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Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an “X” to the left of the appropriate paragraph):

- X 37 C.F.R. §1.97(b).
- 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
- A statement pursuant to 37 C.F.R. §1.97(e) or
- Charge Deposit Account No. 02-2666 \$180.00 for the fee under 37 C.F.R. § 1.17(p).
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- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
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Pursuant to 37 C.F.R. § 1.98(d), no copies of cited art are enclosed. The cited art has been previously cited in parent application no. 11/468,195, filed August 29, 2006.

If there are any additional charges, please charge Deposit Account No. 50-3781.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: October 12, 2009

/Daniel Ovanezian/
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Electronic Patent Application Fee Transmittal				
Application Number:		12577477		
Filing Date:				
Title of Invention:		CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER		
First Named Inventor/Applicant Name:		Gabriel Li		
Filer:		Daniel E. Ovanezian/Juanita Briscoe		
Attorney Docket Number:		CD05110C		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt

EFS ID:	6246193
Application Number:	12577477
International Application Number:	
Confirmation Number:	4345
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
First Named Inventor/Applicant Name:	Gabriel Li
Customer Number:	60909
Filer:	Daniel E. Ovanezian/Juanita Briscoe
Filer Authorized By:	Daniel E. Ovanezian
Attorney Docket Number:	CD05110C
Receipt Date:	12-OCT-2009
Filing Date:	
Time Stamp:	18:11:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1090
RAM confirmation Number	11690
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Page 2023 - 190

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (PTO-875)	fee-info.pdf	33442	no	2
			35aaba7263e6699debe5ea32484cfd9f50c43b4d		

Warnings:

Information:

Total Files Size (in bytes):

33442

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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Electronic Acknowledgement Receipt

EFS ID:	6246193
Application Number:	12577477
International Application Number:	
Confirmation Number:	4345
Title of Invention:	CIRCUIT, SYSTEM, AND METHOD FOR MULTIPLEXING SIGNALS WITH REDUCED JITTER
First Named Inventor/Applicant Name:	Gabriel Li
Customer Number:	60909
Filer:	Daniel E. Ovanezian/Juanita Briscoe
Filer Authorized By:	Daniel E. Ovanezian
Attorney Docket Number:	CD05110C
Receipt Date:	12-OCT-2009
Filing Date:	
Time Stamp:	18:11:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1090
RAM confirmation Number	11690
Deposit Account	022666
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (PTO-875)	fee-info.pdf	33442	no	2
			35aaba7263e6699debe5ea32484cfd9f50c43b4d		

Warnings:

Information:

Total Files Size (in bytes):

33442

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Filing Date: 10/12/09

Approved for use through 7/31/2006. OMB 0651-0032

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number

12/577,477

APPLICATION AS FILED – PART I

(Column 1) (Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

SMALL ENTITY

RATE (\$)	FEE (\$)
N/A	
N/A	
N/A	
x\$26	
x\$110	
195	
TOTAL	

OR

OTHER THAN SMALL ENTITY

RATE (\$)	FEE (\$)
N/A	330
N/A	540
N/A	220
x\$52	
x\$220	
390	
TOTAL	1090

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

OR

OTHER THAN SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

AMENDMENT B

(Column 1) (Column 2) (Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

OR

OTHER THAN SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

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