

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INFINEON TECHNOLOGIES AMERICAS CORP.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

Case IPR2025-01171
Patent 7,051,306

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit	Description
2001	Reserved
2002	Reserved
2003	Reserved
2004	March 10, 2025 WDTX Complaint for Patent Infringement (1:25-cv-358) [Complaint]
2005	November 3, 2017 Notice Letter to Cypress Semiconductor Corporation [11/03/17 Letter] (CONFIDENTIAL)
2006	Scheduling Order in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00358 (W.D. Tex.), Dkt. 30 (July 25, 2025) [Scheduling Order]
2007-2011	Reserved
2012	Declaration of Boris Teksler [Teksler-Decl.] (CONFIDENTIAL – ATTORNEYS' EYES ONLY)
2013	Press Release, Infineon Technologies AG completes acquisition of Cypress Semiconductor Corporation (Apr. 16, 2020) [Press-Release-Cypress]
2014	Letter from Cypress (May 5, 2019) [05/05/19 Letter] (CONFIDENTIAL)
2015	Response Presentation (April 2018) [04/18 Presentation] (CONFIDENTIAL)
2016	Claim Chart (April 2018) [04/18 PSoC Claim Chart] (CONFIDENTIAL)
2017	Response Presentation (Sept. 26, 2018) [09/26/18 Conversant Presentation] (CONFIDENTIAL)

Exhibit	Description
2018	Response Presentation (June 21, 2019) [06/21/19 Conversant Response Presentation] (CONFIDENTIAL)
2019	Response Presentation (Dec. 4, 2019) [12/04/19 Conversant Presentation] (CONFIDENTIAL)
2020	Response Presentation (July 14, 2020) [07/14/20 Conversant Response] (CONFIDENTIAL)
2021	Response to Cypress' September 9, 2020 Comments US 7,051,306 (March 11, 2021) [03/11/21 Conversant Presentation] [CONFIDENTIAL]
2022	MOSAID – Infineon/Cypress Presentation (February 28, 2023) [02/28/23 MOSAID-Infineon/Cypress Presentation] (CONFIDENTIAL)
2023	Excerpts of File History for U.S. Patent No. 7,899,145 ['145-FH]
2024	Excerpts of File History for U.S. Patent No. 8,290,109 ['109-FH]
2025	Infineon's Preliminary Invalidity Contentions in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00358 (W.D. Tex.) (served Aug. 15, 2025) [Invalidity Contentions]
2026	Letter from Cypress (August 1, 2018) [08/01/18 Letter] (CONFIDENTIAL)
2027	Patent Owner's Preliminary Response in <i>MediaTek, Inc. v. MOSAID Techs. Inc.</i> , IPR2024-00598, Paper 10 (July 1, 2024)

All emphases in quotations are added unless otherwise stated.

I. INTRODUCTION

The Petition should be denied as it fails to demonstrate a reasonable likelihood of prevailing as to at least one challenged claim. Each of the claims requires (1) an “integrated circuit including [or comprising] a plurality of power islands,” where “power consumption is independently controlled within each of the power islands,” (2) “determining a target power level for one of the power islands,” and (3) determining “at least one of actions to change a power consumption level . . . to the target power level.” Petitioner alleges, but fails to prove, that these limitations are disclosed or rendered obvious in any of its grounds.

Petitioner does not overcome the fundamental defect in its case: it never identifies “a plurality of power islands” in the cited art wherein power consumption is “independently controlled within each of the power islands.” Petitioner points to functional blocks in Nowka and Nicol but does not show that these blocks operate as independently controllable “power islands.” Instead, Petitioner repeatedly assumes that physically distinct components must have independent power control or could obviously have been made to have independent power control—an assumption that, when not expressly contrary to disclosures in the cited art, is unsupported and driven by hindsight.

Further, having effectively redefined the claims by regarding any block of circuitry as a “power island,” Petitioner then labels any action affecting power

consumption as a disclosure of “determining a target power level.” But the claims require more: independent power control of actual power islands, determinations of target power levels (based on the needs and operation of an integrated circuit of which the power islands are a part), and action(s) to “change a power consumption level” as a result of those determinations. Petitioner does not show these elements in the cited art, and institution should therefore be denied.

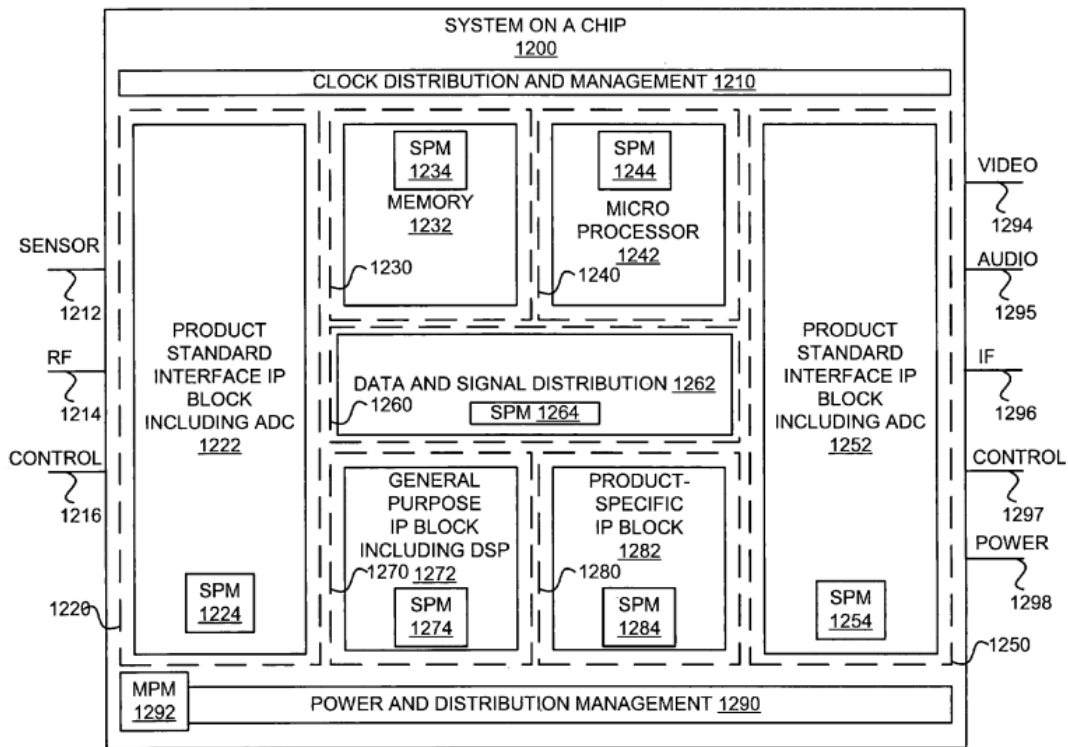
This case comes to the Board following a prior IPR (IPR2024-00598) against the same patent. The arguments presented in this preliminary response are new and were not addressed by the Board in IPR2024-00598. In that proceeding, the Board decided to institute trial after analyzing arguments not made here relating to claim constructions that the prior petitioner had stipulated to, and the Board’s decision analyzed Nowka grounds only. Broadly speaking, the present Petition—which largely recapitulates the previously filed petition, *see, e.g.*, Pet., 1 (“This Petition reasserts Grounds 1A–1C and 2A–2D from the prior IPR”), and which relies on the same expert declarant—adds an additional ground (combining Nowka with Bertin) and includes further attempts to address prior litigation constructions of the claim term “based on needs and operation of the integrated circuit” (which do not affect the arguments made here). None of these changes improve Petitioner’s position. The new Nowka material only shows that Nowka itself does not disclose relevant

limitations, and Petitioner's attempts to address claim construction issues are unrelated to the weaknesses identified in this preliminary response.

II. "POWER ISLANDS" IN THE '306 PATENT

The '306 patent describes methods and systems for reducing power consumption in integrated circuits while maintaining performance. Crucial to the methods and systems claimed in the '306 patent is the idea of "power islands," or delineations of an integrated circuit into subdivisions "where power consumption is controlled within" each subdivision. Ex. 1001 ['306] 3:51-54.

The '306 patent correspondingly describes exemplary designs where such islands are separately controlled by a "power manager" that is configured to "determine a target power level" for one of the power islands "where power consumption is individually controlled within each of the power islands," and that can "dynamically change the power consumption of the power islands . . . based on the needs and operation of the integrated circuit," *id.*, 4:18-31, for example, by "modifying a clock frequency of one of the power islands" or "modify[ing] voltage of one of the power islands," *id.*, 4:45-54. An exemplary configuration of such a design is depicted in the '306 patent's Figure 12:



Id., Fig. 12.

As seen above, “slave” power managers (“SPMs”) 1224, 1234, 1254, 1274, and 1284 are configured to separately and independently manage power consumption within their respective power islands 1220 (an “IP block power island” including an analog-to-digital converter), 1230 (an “IP block power island” including a memory), 1250 (a “product standard interface IP block” including an analog-to-digital converter), 1270 (a “general purpose IP block” including a digital signal processor), and 1280 (a “product-specific IP block”), and to do so in dialogue with a “master” power manager (“MPM”) 1292. *See, e.g., id.*, 12:23-38 (discussing these power managers), 4:33-34 (referring to a “slave power manager” as an

“SPM”). All claims of the ’306 patent correspondingly recite methods or systems involving not only a “an integrated circuit including [or comprising] a plurality of power islands” but, *inter alia*, determining (or having a component configured to determine) “a target power level for one of the power islands based on needs and operation of the integrated circuit,” where “power consumption is independently controlled within each of the power islands.” *See id.*, cls. 1-51.

The crucial point for present purposes is that “power islands” are not merely delineations of an integrated circuit, but delineations with separately controllable power. If one considers only if there exist functionally divided blocks of circuits, one may very well have “islands.” But what makes a “**power** island” is the adjective “power”—the island must be configured so as to have its power controlled independent of other components. Thus, when judging the prior art’s disclosures against the inventions of the ’306 patent, the adjective “power” in the claim term “power island,” and the separate recitation of “power consumption [being] independently controlled within each of the power islands,” mean that merely having functional blocks of circuitry is not enough—the question is whether (and how) those blocks have independent power control.

This point is where the Petition falls apart in addressing the prior art. Petitioner can perhaps argue that Nowka or Nicol disclose various distinct functional blocks of circuitry, but not that these blocks are shown to have independently

controllable power, let alone independently controllable power that is controlled as further recited in the challenged claims. Petitioner invites the Board to ignore the crucial point of a “power island”—that it is a *power* island and not merely a functional island. Petitioner is thus not engaging with the actual claim terms at all, instead focusing upon hypothetical claims where “power” is struck from the term “power island” everywhere it appears, and where the claim requirement that “power consumption is independently controlled within each of the power islands” is removed entirely. This is basic error. The references leave Petitioner no choice, of course, as neither Nowka nor Nicol disclose or suggest “power islands” with the claimed properties. But Petitioner’s plight does not change the legal requirements of a validity analysis.

Details of how the variously cited teachings of Nowka and Nicol fail to render the challenged claims obvious are addressed in the sections below. Petitioner has not shown that the cited references teach or render obvious the claimed methods or systems.

III. PETITIONER’S GROUNDS DO NOT TEACH OR RENDER OBVIOUS “A PLURALITY OF POWER ISLANDS . . . WHERE POWER CONSUMPTION IS INDEPENDENTLY CONTROLLED WITHIN EACH OF THE POWER ISLANDS” (ALL CHALLENGED CLAIMS, ALL GROUNDS).

Petitioner does not show that its grounds teach or render obvious “a plurality of power islands . . . where power consumption is independently controlled within

each of the power islands,” as recited in every challenged claim. *See, e.g.*, Ex. 1001 [’306] 13:33-39 (independent claim 1), 14:20-21 (independent claim 16), 15:22-29 (independent claim 37).

Significantly, at the institution stage in IPR2024-00598, the previous IPR against the ’306 patent, Patent Owner did not address this claim language—focusing instead upon an agreed upon construction of “based on needs and operation of the integrated circuit” that the petitioner in IPR2024-00598 had stipulated to in parallel litigation. *See, e.g.*, Ex. 1032 (Institution Decision in IPR2024-00598), 10-16 (addressing the construction of “based on needs and operation of the integrated circuit”), 19-22 (analyzing other disputes regarding elements 1[p] and 1[a]); *see also, e.g.*, Ex. 2027 (Patent Owner Preliminary Response, Paper 10 in IPR2024-00598), 3-27 (discussing claim construction issues, but not addressing whether Nowka or Nicol teach “a plurality of power islands” in the sense of the ’306 patent).

Thus, although Petitioner cites the institution decision in IPR2024-00598 in arguing that “the Board has already deemed [the ’306 patent] likely unpatentable,” Pet., 1, the Board has *never* addressed the issues presented here. Indeed, while the previous institution decision discusses unrelated aspects of Petitioner’s Nowka reference, the previous institution decision expressly did not address any arguments relating to Nicol. *See, e.g.*, Ex. 1032 (Institution Decision in IPR2024-00598), 26 (“[W]e decline at this stage to provide an explicit analysis of Petitioner’s Nicol-led

challenges.”).

A. Nowka Grounds (All Challenged Claims, Grounds 1A–1D).

All of Petitioner’s Nowka grounds depend upon its single-reference Nowka ground for “a plurality of power islands . . . where power consumption is independently controlled within each of the power islands,”¹ and in particular, upon Petitioner’s single-reference Nowka ground for claim 1.² This preliminary response accordingly focuses on Petitioner’s arguments regarding its single-reference Nowka ground for claim 1. (Petitioner separately argues that Bertin “further bolsters [its] mapping” of alleged “power islands” in Nowka in connection with its Ground 1D, *see* Pet., 51, but this argument also fails. *See* Section III.A.3, *infra*.)

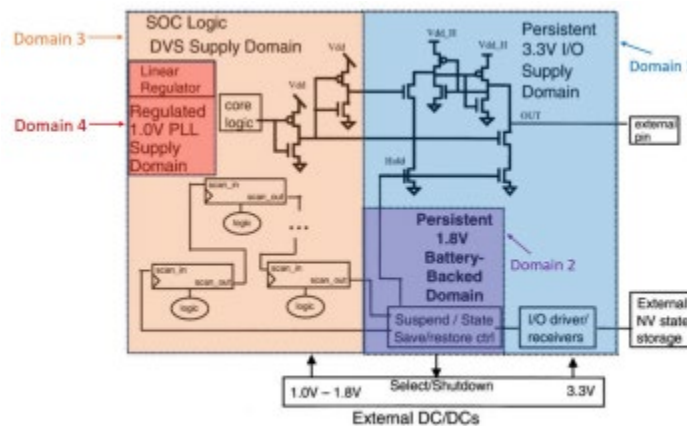
Petitioner proposes two distinct rationales for finding a purported “plurality of power islands” in Nowka, but fails to prove either one.

¹ *See generally* Pet., 39-45 (Petitioner’s Nowka-Borkar ground, addressing aspects of dependent claims only), 46-47 (Petitioner’s Nowka-Boerstler ground, addressing aspects of dependent claims only), 51 (Petitioner’s Nowka-Bertin ground citing “Ground 1A, element 1[p]” for this aspect of the independent claims),

² *See, e.g.*, Pet., 24, 32 (Petitioner’s single-reference Nowka ground referring to arguments about claim 1 for this aspect of independent claims 16 and 37).

1. Petitioner Fails To Show That The “Domains” In Nowka’s Figure 3 Are “a plurality of power islands . . . where power consumption is independently controlled within each of the power islands.”

Petitioner’s first four candidates for alleged “power islands” in Nowka are identified as “Domain 1,” “Domain 2,” “Domain 3,” and “Domain 4” in Petitioner’s annotated version of Nowka’s Figure 3:



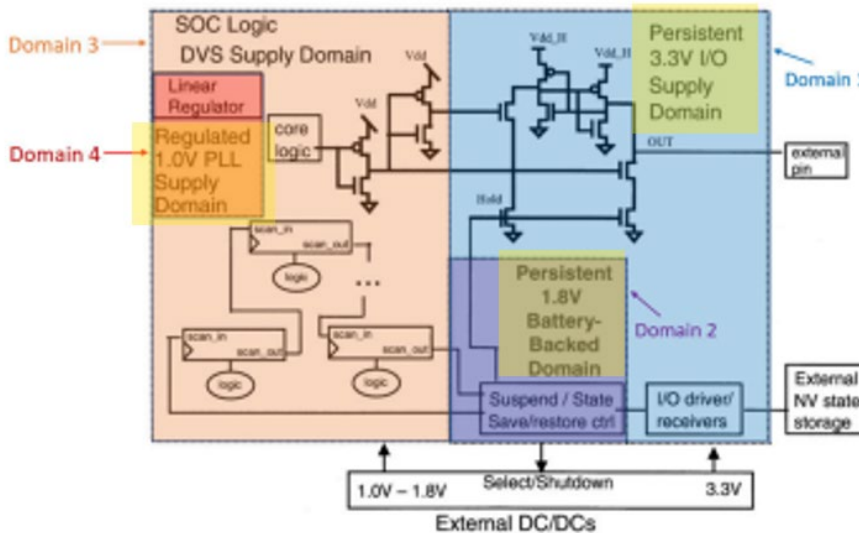
EX1004, Fig. 3.

Pet., 9 (Nowka’s Figure 3, annotated by Petitioner); *see also id.*, 8 (“Nowka discloses multiple power domains on the integrated circuit, namely the four domains depicted in Figure 3”), 9 (arguing that a POSITA would “have understood and found obvious that the four domains are power islands”). As will be seen below, in IPR2024-00718, a related IPR concerning a related patent, the Board has already rejected the argument that Nowka’s domains are “power islands.” The Board should reject this argument again in this proceeding.

Claim 1, again, expressly requires “a plurality of power islands”—*i.e.*, more than one power island—wherein power consumption is “*independently controlled*

within *each* of the power islands.” Ex. 1001 [’306] 13:37-38. In all but one of Nowka’s “domains,” by contrast, the power consumption of the “domain” is static. Consequently, Petitioner has not shown “a plurality of power islands” as required. Indeed, Petitioner never explains how supplying static voltages to different components could constitute “independent control” of the power consumptions of those components. Indeed, Petitioner makes no attempt to argue that power consumption in all but perhaps one of Nowka’s “domains” is even *variable*, let alone “independently controlled within *each*” domain as the claim requires.

Nowka describes its four “domains” as a 1.8V persistent battery backed domain, a 3.3V persistent domain, a constant 1V PLL, and a variable 1.0V-1.8V logic domain. *See, e.g.*, Ex. 1004 [Nowka] 1442 (“These [four domains] consist of two persistent voltage domains, one dynamically voltage-scaled logic domain, and one internally derived domain” where the internally derived domain “derives a constant 1-V supply”). The lack of variability in the voltages supplied to three of Nowka’s four “domains” is express in Nowka’s Figure 3, which labels the fixed-voltage domains with their fixed voltages:



Ex. 1004, Fig. 3 (as annotated by Petitioner at Pet., 9, with yellow highlighting added by Patent Owner emphasizing a “1.0V PLL Supply Domain,” a “Persistent 3.3V I/O Supply Domain,” and a “Persistent 1.8V Battery-Backed Domain”). Nowka’s logic domain—the only “domain” described by Nowka as “dynamically voltage-scaled,” *id.*, 1442—is the only domain of the four with a potentially variable supply voltage. *See id.*, 1444.

Implicitly acknowledging this fact, Petitioner never argues, for example, that the voltages supplied to domains other than Nowka’s logic domain are variable. Petitioner only states that these domains “are *supplied* different voltages.” Pet., 8. But Petitioner does not explain how domains being *supplied* “different voltages” shows that power consumption is “independently controlled within each” domain. Instead, Petitioner makes other arguments that do not address this issue.

Petitioner asserts that the “domains” of Figure 3 satisfy aspects of a

description of power islands given in the specification of the '306 patent (a line that references controlling power consumption “within” a power island, without reference to any “independent[] control[],” as recited in every challenged claim):

A POSITA would have understood and found obvious that the four domains are power islands as defined by the '306 patent because each domain is a “section, delineation, partition, or division” on the SOC where “power consumption is controlled within the section, delineation, partition, or division.”

Id., 8-9 (quoting Ex. 1001 ['306] 3:51-54). Of course, Petitioner’s mere statement that “power consumption is controlled within” the “domains” of Nowka’s Figure 3 is not a showing that this is the case, let alone a showing that “power consumption is *independently* controlled within each” domain, as claim 1 requires.

Petitioner then argues as follows:

Nowka’s power domains (power islands) *receive distinct voltage supplies*, which can be controlled independently (e.g., the logic domain 3 can receive variable voltage supply while domains 1 and 2 receive a persistent voltage supply).

Id., 15. But Petitioner’s parenthetical—the *only* support Petitioner offers for its assertion that the voltage supplies of the domains in Figure 3 “can be controlled independently”—does not show *how* power consumption “can be controlled independently” (as Petitioner phrases it), let alone how “power consumption is

independently controlled within *each*” of the “domains,” as recited for the “plurality of power islands” of claim 1. Obviousness cannot be shown by conclusory statements. *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”).

Petitioner cites its expert in connection with its bare assertion that Nowka’s domains are “can be controlled independently.” Pet. 15 (citing Ex. 1003 [Decl.] ¶ 65). But the cited testimony only describes what is immediate from Nowka itself—that each domain has its own voltage supply: domain 1 receives a static 3.3 V, domain 2 receives a static 1.8 V, domain 3 receives a 1.0–1.8 V variable supply, and domain 4 receives a static 1.0 V. *See* Ex. 1003 [Decl.] ¶ 65. The voltages supplied to the static domains do not change during any operation of Nowka’s system, as Petitioner’s expert acknowledges. *Id.* (referring to domains 1, 2, and 4 as “powered persistently”). And Petitioner does not identify *any other basis* on which the power consumptions of domains 1, 2, and 4 might *ever* change during the operation of Nowka’s system. The mere fact that the voltage supplies of these domains are distinct, or that they provide different voltages, does not mean the power consumptions of these domains are independently controlled as the claims require.

Indeed, it is not even clear that *Petitioner’s expert* takes the position that the

power consumptions of Nowka’s four domains are independently controlled. In the paragraph of declaration that is cited (but not quoted or discussed) by Petitioner, Petitioner’s expert states only that:

[a] POSITA would have understood that powering these domains independently *allows for independent power control*, as illustrated by Nowka’s dynamic voltage and frequency scaling in the logic domain *even as the other domains are powered persistently*.

Id., ¶ 65. In saying that Nowka’s design “*allows* for independent power control”—and by distinguishing the one dynamically variable domain from the three persistent/constant domains—Petitioner’s expert appears to recognize that Nowka itself might *not* itself disclose “independent power control” of all of Nowka’s domains. The Petition, by contrast, uses different wording, and wording that is arguably more suggestive of a contention that “independent power control” of Nowka’s domains is already present in Nowka. Pet., 15 (arguing that “*Nowka’s power domains* (power islands) receive distinct voltage supplies, which *can be controlled independently*”). And Petitioner does not, for example, offer any explanation of how a POSITA would modify Nowka to implement “independent power control” if this functionality is not already present in Nowka (as Petitioner apparently believes it is).

A related issue arose in IPR2024-00718, which involved whether Nowka’s

Figure 3 taught “a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled” in the sense of claim 1 of a descendant of the ’306 patent,³ and a declaration from the same expert used by Petitioner in this proceeding. There, the Board observed:

The paragraph of Dr. Rosing’s declaration cited by Petitioner as support for its contention that all of Nowka’s domains are power islands is worded a little differently than Petitioner’s arguments. Dr. Rosing opines that “Nowka’s voltage domains satisfy the ’811 patent’s definition of ‘power island,’ as each domain is a section, delineation, partition, or division of Nowka’s SOC, and each domain receives a different power supply,” and opines that receiving separate voltage supplies means that a domain can be independently controlled. This testimony is conclusory and—to the extent that it is an assertion that the ’811 patent describes “independently controlled” as encompassing the act of merely providing a separate power supply, even if that supply is not a dynamically controllable and variable power supply—lacks citation to intrinsic evidence support.

IPR2024-00718, Paper 10, 20 (Oct. 9, 2024) (denying institution) (internal citations omitted). The Board found that the petitioner in that IPR had not shown that Nowka

³ IPR2024-00718 concerned U.S. Patent No. 7,996,811, a continuation of a continuation of a continuation of the ’306 patent.

disclosed the relevant limitation. *Id.*, 21; *see also id.*, Concurring Opinion at 4 (“Petitioner fails to demonstrate how any of Nowka’s persistent 3.3V I/O supply, persistent 1.8V battery-backed, or regulated (i.e., constant) 1.0V PLL supply domains have a variable power consumption and, therefore, read on the patent’s definition of a power island”).

For essentially the same reasons, the present Petitioner merely placing the phrase “independent power control” in proximity with citation to Nowka does not evidence—let alone show—that power consumption is “independently controlled within each” domain. Both Petitioner and Petitioner’s expert’s conclusory statements to the contrary are entitled to little weight, and should be rejected. *See, e.g.*, 37 C.F.R. § 42.65(a); *see also Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15-17 (Aug. 24, 2022) (precedential) (denying institution when expert declaration “adds little to the conclusory assertion for which it is offered to support”).

2. Petitioner Fails To Show That The “cores” Within Nowka’s Logic Domain Are “a plurality of power islands . . . where power consumption is independently controlled within each of the power islands,” Such That The Remainder Of Claim 1 Is Satisfied.

As what Petitioner terms “an independent basis” for identifying a purported “plurality of power islands . . . where power consumption is independently controllable within each of the power islands,” Petitioner contends that Nowka’s

“variable voltage and variable frequency logic domain . . . includes multiple ‘cores’—e.g., a ‘processor core,’ a ‘dedicated speech accelerator, an instruction decompression engine and a DES accelerator core,’ and an ‘LCD core,’” Pet., 9, and that these “cores” could serve as a “plurality of power islands” in the sense of claim 1. *Id.*, 9-10 (“A POSITA would have understood and found obvious that these ‘cores’ ***are also capable of being controlled as power islands*** by varying their voltage and frequency independent of the remainder of the SOC.”).

As a threshold matter, and as Petitioner’s use of a garbled version of claim language (“controlled as power islands”) in this assertion highlights, the relevant inquiry is not whether a POSITA with the claim would have understood Nowka to be ***capable*** of being configured as to satisfy the claim; the relevant inquiry is whether a POSITA would have been motivated to modify Nowka in a way that satisfied the claim. *See, e.g., In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984) (“The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification.”); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”). Thus, even if, *arguendo*, Nowka were capable of being configured in this way, this would not establish that a POSITA would be motivated to modify Nowka in that fashion.

And Petitioner’s argument also fails for at least two other reasons. First, Petitioner’s statement that these cores are “capable of being controlled” as to satisfy the claim is unsupported by any reasoning or analysis; Petitioner simply pairs excerpts of sentences within Nowka with this statement. This is not enough. *See, e.g., Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (petitioner “has the burden from the onset to show with particularity why the patent it challenges is unpatentable”); *see also, e.g., Intel Corp. v. VLSI Technology LLC*, IPR2019-01196, Paper 11, 11 (Jan. 7, 2020) (reference not shown to teach limitation when “Petitioner also lists a string of citations to [a reference] but does not explain how these disclosures teach” the limitation); *Sivel Int’l. S.A. v. Sierra Wireless, Inc.*, 82 F.4th 1355, 1364 (Fed. Cir. 2023) (affirming rejection of obviousness rationales that “were too conclusory, lacked clarity, or suffered from both problems”). While Petitioner does cite to its expert declarant in support of this argument, Pet. 10 (citing Ex. 1003 [Decl.] ¶ 51), Petitioner’s expert does the same thing as Petitioner—pair citation to Nowka with claim language. *See* Ex. 1003 [Decl.] ¶ 51. But “evidence” of this sort is entitled to little weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15-17 (Aug. 24, 2022) (precedential) (denying institution when expert declaration “adds little to the conclusory assertion for which it is offered to support.”).

Petitioner’s “argument” does not, for example, explain how the “cores” it identifies are “controlled by varying their voltage and frequency independent of the remainder of the SOC,” *cf.* Pet., 9-10, even though Nowka consistently describes the components of its logic domain as being provided with a *single* voltage—one that, if varied at all, is varied for all components of the logic domain at the same time. *See, e.g.*, Ex. 1004 [Nowka] 1442 (“The logic supply for *the processor core, caches, SOC cores and accelerators* is dynamically varied between 1 and 1.8 V.”). Nor does Petitioner address the fact that Nowka consistently refers to its “on-chip supervisor” as managing the “logic supply” as a whole—not as enabling or disabling cores on an individual basis. *See, e.g., id.*, 1442 (“An on-chip supervisor controls the external DC/DC converter, which provides *the logic supply*. Under software control, the supervisor requests changes to *the logic supply* and requests shutdown of *the logic supply* during hibernation.”); *see also id.*, Abstract (“A low-voltage PLL supplied by an on-chip regulator . . . allows the SOC to operate continuously while *the logic supply voltage* is modified.”). Similarly, the experimental results reported in Nowka—relied upon by Petitioner in arguing that Nowka teaches “determining a target power level,” Pet. 11-13—do not describe the measurement of any individual cores within Nowka’s logic domain, but (to the contrary) describe a *single* power consumption and a *single* supply voltage for the logic domain *as a whole*. *See, e.g.*, Ex. 1004 [Nowka] Fig. 8 (providing “Dynamic voltage and frequency scaling traces”

including “Total power, “Logic power,” and “I/O Power”; also plotting a single “Logic Vdd”); *see also, e.g., id.*, 1444 (referring to Figure 8’s traces for a single “SOC logic power” and a single “SOC logic supply voltage”).

A second problem with Petitioner’s attempt to read individual “cores” within Nowka’s logic domain as the claimed “power islands” becomes apparent when one follows Petitioner’s identification of “cores” with “power islands” through the rest of claim 1, where these putative “power islands” are repeatedly discussed in connection with “clock gating”—that is, stopping the clock of a processing core. But, as explained further below, the Applicant made clear that clock gating does not constitute managing power within a “plurality of power islands.”

As can be seen, in connection with numerous limitations, Petitioner relies upon clock gating:

- In connection with the “determining a target power level for one of the power islands” step of claim 1 (what Petitioner labels step 1[a], Pet., 10), for example, Petitioner expressly mentions the “cores” within Nowka’s logic domain in connection with “clock gating inactive registers and cores.” Pet., 13.
- In connection with the “determining at least one of actions to change a power consumption level of the one of the power islands” step (what Petitioner labels step 1[b]), Petitioner again connects the cores within

Nowka's logic domain to "clock gating" (*id.*, 16), albeit less explicitly: after listing actions that allegedly change a power consumption level "of [Nowka's] logic domain" as a whole—a list that includes "clock gating"—Petitioner includes a statement that "Nowka similarly provides capabilities for power management over the individual 'cores' in this way." *Id.*

- In connection with the "performing at least one of the actions to change the power consumption level of the one of the power islands" step (what Petitioner labels step 1[c])—which requires "selecting a frequency for the one of the power islands," Ex. 1001 ['306] 13:46-47—Petitioner again connects the "cores" in Nowka's logic domain to "clock gating," although once again, this mapping is not explicit. Pet., 17-18. Petitioner offers a string citation of alleged examples of the "performing" step: a citation to Nowka's Section III.C for what Petitioner summarizes in a parenthetical as "voltage scaling," a citation to Nowka's Section V for what Petitioner summarizes as "frequency and voltage scaling," a citation to the quote "Active power of the SOC can be further reduced through modification of the clock frequency within the individual cores," Ex. 1004 [Nowka] 1445 for what Petitioner summarizes as "clock gating," and a citation to

Nowka's page 1446 for what Petitioner describes as "standby modes." Pet., 17-18. Of these four examples, only one of them expressly references Nowka's "cores," and does so in connection with what Petitioner calls "clock gating." *Id.* The other three cited disclosures do not discuss individual cores within Nowka's logic domain. *See* Ex. 1004 [Nowka] 1444 (Section III.C) (not discussing management of individual cores), 1444 (Section V) (same), 1446 (discussing "standby modes") (same).

Petitioner's case that individual cores within Nowka's logic domain constitute "a plurality of power islands" thus relies upon a contention that "clock gating" one or more of these cores could constitute the claimed "selecting a frequency for the one of the power islands." Petitioner identifies no other basis on which Nowka's "cores" could constitute "a plurality of power islands" such that the claim could be satisfied. But this notion is in considerable tension with the prosecution history of the '306 patent—a history that Petitioner does not address when it simply states that "[t]he Patent Office issued one non-final rejection and one final rejection during prosecution" of the '306 patent." *See* Pet., 4 (three-sentence section entitled "Summary of the Prosecution History").

During prosecution of the '306 patent, however, the Applicant overcame an obviousness rejection, Ex. 1002 ['306-FH] 77-79 (Rejections dated July 29, 2005),

by *expressly distinguishing* managing power in “a plurality of power islands” in a draft form of claim 1 from “clock gating.”

More expressly, the rejected draft claim 1 recited as follows:

A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:

determining a target power level for one of the power islands based on the needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands;

determining an action to change a power consumption level of the one of the power islands to the target power level; and

performing the action to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for one of the power islands.

Ex. 1002 [’306-FH] 57 (claims dated Sept. 23, 2005). Thus, the draft claim, like claim 1 in the issued ’306 patent, recited a step of performing an action “to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for [the] one of the power islands.” *Compare* Ex. 1001 [’306] 13:42-47 *with* Ex. 1002 [’306-FH] 57 (same, only without the bracketed “the”).

The examiner rejected this draft claim as obvious in view of, *inter alia*, disclosures in a prior art reference named Lackey. Ex. 1002 [’306-FH] 77-83

(Rejections dated July 29, 2005). But the applicant distinguished “clock gating” in Lackey from “selecting a frequency for the one of the power islands” in the sense of the draft claim:

Furthermore, the clock gating in Lackey does not teach or suggest the limitation of selecting a frequency for a power island as recited in claim 1. Clock gating refers to activating a clock in a logic block only when there is work to be done in order to save power. Thus, activating and deactivating a clock does not teach or suggest selecting a frequency for a power island as recited in claim 1.

Ex. 1002 [’306-FH] 69 (Applicant Remarks dated Sept. 23, 2005). The Examiner agreed. *Id.*, 45 (Notice of Allowability dated Oct. 13, 2005) (allowing the claims because “the prior art does not teach or fairly suggest” subject matter including “performing at least one of actions to change a power consumption level of one of the power islands to a target power level where one of the actions comprises selecting a frequency for the one of the power islands”) (emphasis in original).

Petitioner’s identification of Nowka’s individual “cores” as a putative “plurality of power islands” that satisfy the claim thus carries with it an unexplained claim construction argument: that clock gating *in Nowka* teaches or suggests the limitation of selecting a frequency for one of the claimed “power islands,” when the prosecution history makes express that clock gating *in Lackey* did not—and when the Applicant stated, in addition to its observation about Lackey, that “activating and

deactivating a clock does not teach or suggest selecting a frequency for a power island as recited” in what ultimately became claim 1. Ex. 1002 [’306-FH] 69 (Applicant Remarks dated Sept. 23, 2005).

That the prosecution history of the ’306 patent excludes “clock gating” as a method of selecting a frequency is further evidenced by a prior claim construction order concerning the “selecting a frequency” language in the ’306 patent, in which a court observed that “clock gating does not control the frequency of a signal[,] but instead effectively acts as an on/off switch for passing or blocking a frequency signal,” and that “a zero frequency signal ... [is] actually not a frequency signal at all.” Ex. 1011 [*Freescale* Claim Construction Order], 43.

Petitioner had the burden to construe the claim and demonstrate that the construed claims are satisfied. *See* 37 C.F.R. §§ 42.104(b)(3)–(4). Thus, even if it were assumed for the sake of argument that the individual “cores” within Nowka’s logic domain are “capable of being controlled as power islands” (as Petitioner contends, Pet., 9), it would not follow that Petitioner has shown that they are “power islands” *in the sense of claim 1*. Such a showing that would require Petitioner to explain, not just why these “cores” are allegedly “a plurality of power islands . . . where power consumption is independently controlled within each of the power islands,” but why the form of allegedly independent control of power consumption in these “cores”—“clock gating”—could satisfy the rest of claim 1. In not engaging

with the relevant prosecution history, and at least one prior district court construction, Petitioner does not even attempt to make such a showing.

3. Petitioner Fails To Show That Bertin Teaches Or Renders Obvious “a plurality of power islands . . . where power consumption is independently controlled within each of the power islands” In Combination With Nowka.

The Petition includes a combination of Nowka with Bertin to attempt to address “if Patent Owner attempts to rebut Ground 1A by arguing that Nowka does not determine an explicitly prescribed target power level.” Pet., 47-48. In passing, however, Petitioner argues that Bertin “bolsters” the idea that individual cores within Nowka’s logic domain are, or obviously could be, “a plurality of power islands” in the sense of claim 1. Pet., 51 (“to the extent Patent Owner argues that Nowka’s ‘cores’ . . . somehow do not render obvious the claimed power islands, integration of Bertin’s teachings further bolsters this mapping”). But Petitioner’s argument is conclusory, and does not substantively link any of Bertin’s alleged teachings to Nowka’s system.

Petitioner says that “Bertin makes clear that individual functional units—like Nowka’s ‘cores’—have ‘independently controllable body voltage or threshold voltage.’” *Id.* But Petitioner does not explain why Bertin’s reference to components with “independently controllable body voltage or threshold voltage” *in Bertin* means that this description applies without modification to components *in Nowka*. As one

example, Bertin also says that “while different functional units have been described, one functional unit need not be totally independent of another,” Ex. 1027 [Bertin] 3:23-25, and if this disclosure would not also apply to “cores” in Nowka’s logic domain, Petitioner does not explain why.

Similarly, Bertin discloses an “intelligent power control” that continually maintains both a “requirements table” (which identifies “for each instruction that [a] chip . . . is capable of executing, which functional units on the chip are required to execute that instruction”), a “status table” (which “reflects the present power status of each of the functional units on the chip”), and “logic” that analyzes “whether the power requirement and power status for the unit are in agreement,” where the logic generates “[s]ignals . . . to control the status of the associated functional unit to bring the requirements and status into agreement if necessary.” Ex. 1027 [Bertin] 5:23-47. None of these specialized components and functionalities are described in Nowka, although they are clearly central to the operation of Bertin. *See, e.g., id.*, 6:24-40 & Figs. 4A, 4B (describing Bertin’s “status table”), 6:41–7:23 (describing Bertin’s “logic”), 8:26–9:26 (describing the use of the output of Bertin’s “logic”), claim 1 (reciting a “status table” and “logic unit” with various capabilities).

And Petitioner’s proposed combination of Bertin and Nowka is described at so high a level of generality that it is unclear if Petitioner even proposes to modify Nowka by including Bertin’s “status table” or Bertin’s “logic” (let alone where, if

Petitioner is in fact proposing that). *See, e.g.*, Pet., 49 (describing the combination as “implement[ing] Nowka’s ‘software control’ for dynamic voltage and frequency scaling, based on prescribed ‘power levels’ (or ‘power state[s]’) that correspond to ‘power requirement[s]’ dictated by an application, as taught by Bertin”) (citations omitted); *see also id.* (stating that “[t]he fundamental aspects of Nowka’s disclosure would remain intact” but be “bolstered by the well-known and beneficial teachings of Bertin to arrive, with a reasonable expectation of success, at a system within the scope of the Challenged Claims”); *id.*, 51-52 (repeatedly describing Bertin as teaching “utilizing prescribed power levels or states”), 52-53 (twice stating that “[i]n the Nowka-Bertin combination, Nowka’s ‘power management software’ employs Bertin’s conceptual approach”) (citations omitted).

Relying on an underspecified “combination,” as Petitioner has done here, is sufficient reason to reject a ground. *Harmonic*, 815 F.3d at 1363 (“it was [Ppetitioner’s] burden to explain to the Board how Haskell combined with Rossmere rendered the challenged claims unpatentable.”); *Markforged Inc., v. Continuous Composites, Inc.*, IPR2022-01220, Paper 8, 36 (Jan. 11, 2023) (“Petitioner appears to be arguing that a POSITA could have combined unspecified teachings of Lipsker in unspecified ways to improve Wohrl’s method. . . . Accordingly, the Petition lacks an adequate explanation as to why a skilled artisan reading Wohrl would have looked specifically to Lipsker for its particular teachings, and how a skilled artisan would

have combined the teachings of Wohrl and Lipsker in the manner claimed.”) (denying institution).

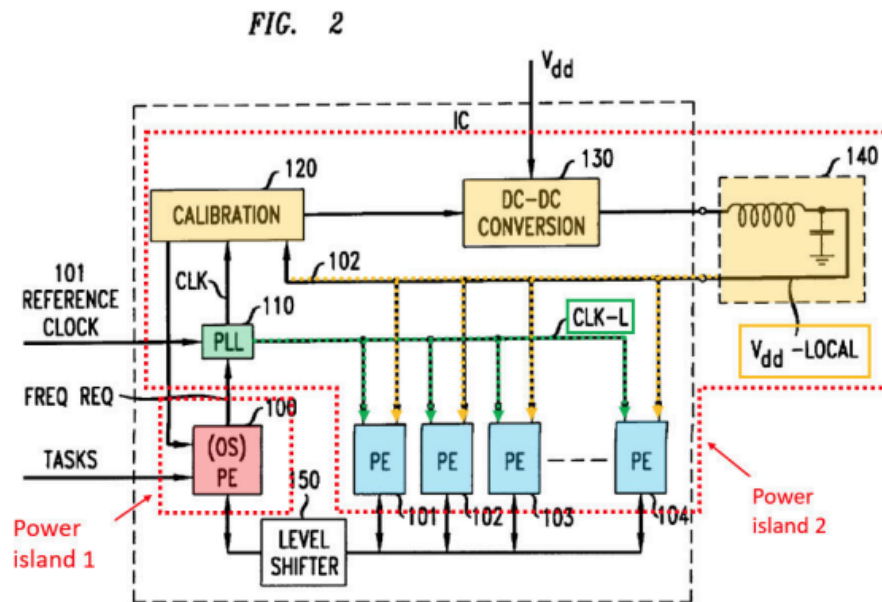
B. Nicol Grounds (All Challenged Claims, Grounds 2A–2D).

All of Petitioner’s Nicol grounds depend upon its single-reference Nicol ground for “a plurality of power islands . . . where power consumption is independently controlled within each of the power islands” (*see generally* Pet., 75-82 (Petitioner’s Nicol-Nowka ground, addressing aspects of dependent claims only), 82-87 (Petitioner’s Nicol-Borkar ground, addressing aspects of dependent claims only), 87-91 (Petitioner’s Nicol-Naffziger ground, addressing dependent claim 35 only)), and in particular, upon Petitioner’s single-reference Nicol ground for claim 1. *See, e.g., id.*, 57-64 (Petitioner’s single-reference Nicol ground for claim 1), 70 (Petitioner’s single-reference Nicol ground referring to arguments about claim 1 for this aspect of independent claims 16 and 37), 74 (same). This preliminary response accordingly focuses on Petitioner’s arguments regarding its single-reference Nicol ground.

Petitioner proposes two distinct rationales for finding purported “plurality of power islands” in Nicol, but fails to prove either one.

1. Petitioner Fails To Identify A “plurality of power islands . . . where power consumption is independently controlled within each of the power islands” In Nicol’s Figure 2 Embodiment.

Petitioner’s first identification of a purported “plurality of power islands” in Nicol’s Figure 2 is a purported pair of “power islands” consisting of the “PE 100,” on the one hand, and the group of “PEs 101-104” and related circuitry, on the other:



Pet., 57 (Nicol’s Figure 2 as annotated by Petitioner, collecting PEs 101-104 within a single “Power Island 2”). Petitioner argues, for example, that “PE 100 and PEs 101-104 form different power islands because they are sections, delineations, partitions, or divisions of the integrated circuit, are powered independently, and receive separate clock sources.” *Id.* But Petitioner never shows how power consumption “is independently controlled within each” of PE 100, on the one hand, and PEs 101-104, on the other. In particular, for example, Petitioner never discusses

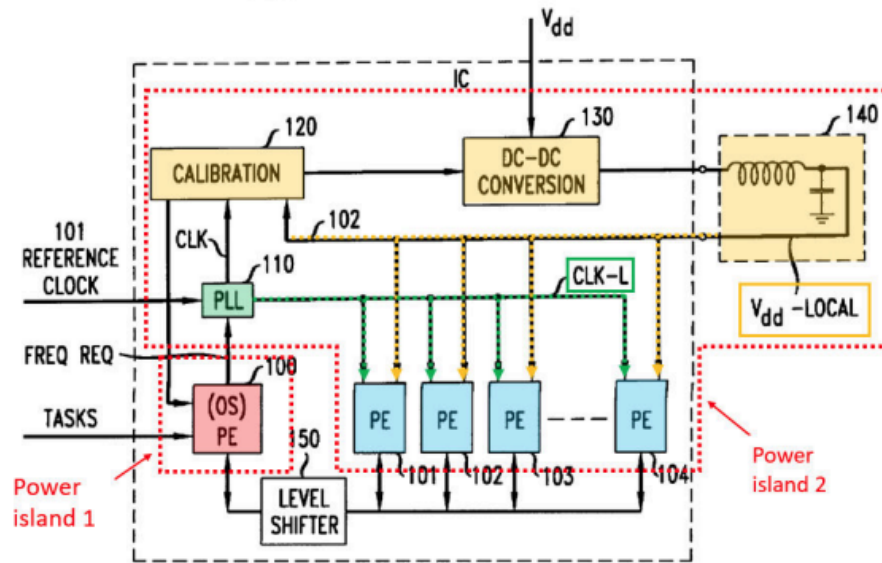
how power consumption is controlled (whether “independently” or otherwise”) within PE 100.

Immediately after asserting that “power consumption is independently controlled within each power island” in Nicol—rather than addressing this issue—Petitioner changes the subject away from Figure 2: Petitioner states that “[t]he ability for independent control is most explicit in the Figure 4 embodiment.” *Id.*, 59. Figure 4 is a distinct embodiment of Nicol, based on a different operating principle (and discussed separately below, see Section III.B.2). Petitioner provides no explanation of why the “ability for independent control” it alleges for Figure 4 would be present in the alleged “power islands” it identifies in Figure 2; Petitioner merely reproduces Nicol’s Figure 4 and Figure 2 side-by-side without comment. *Id.*

If Petitioner intends its earlier statement that the “PE 100” and “PEs 101-104” of Figure 2 are “powered independently” and “receive separate clock sources” (*id.*, 57), to evidence or demonstrate that the power consumptions of these groups in Figure 2 are ***independently controlled*** as the claim requires, Petitioner does not explain why. Nor does Nicol itself suggest that this is the case.

Nicol discloses that the PEs 101-104 of Nicol’s Figure 2 are supplied with a common supply voltage (denoted “Vdd-LOCAL” in Figure 2) and operate at a common clock frequency (denoted “CLK-L” in Figure 2):

FIG. 2



Ex. 1008 [Nicol] Fig. 2 (as annotated by Petitioner at Pet., 59) (depicting “CLK-L” and “Vdd-local” being provided to PEs 101-104). Nicol elsewhere suggests that PE 100 might operate at the *same* voltage as PEs 101-104. *See, e.g., id.* 4:17-37 (“Returning the discussion to Figure 2, ... Clk-L is applied to the PEs The Vdd-local supply voltage is also applied to all of the PEs (excluding *perhaps* the operating system PE 100)”); *see also id.*, 5:51 (referring to “the [common] voltage level of PEs 101-104” in Nicol’s Figure 2). Here Nicol’s “perhaps” suggests that even if PE 100 has a separate voltage supply line from PEs 101-104, it may be that this line is used to supply the *same* voltage that PEs 101-104 each receive, not a different voltage, let alone an independently variable voltage. Indeed, Petitioner never identifies (even in conclusory terms) *any* mechanism by which the power consumption of PE 100 is allegedly adjustable.

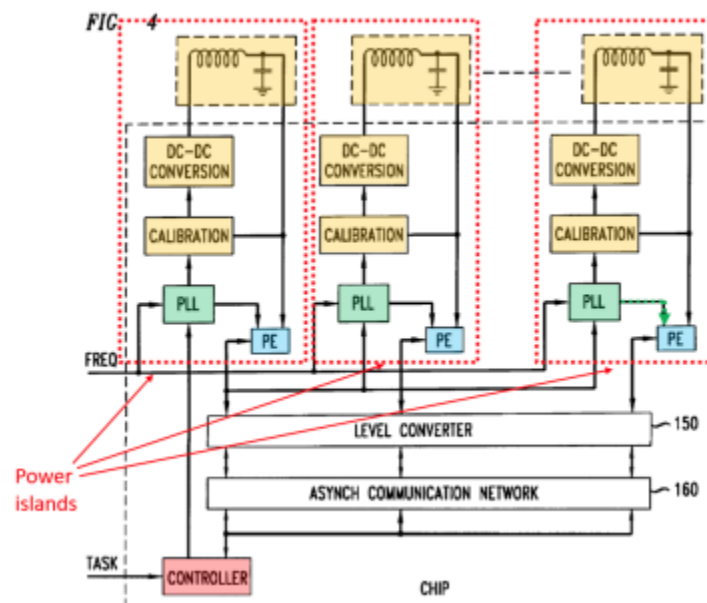
The Petition at most offers a rationale under which power consumption in *one* of Petitioner’s two alleged “power islands,” the group of PEs 101-104, is controlled. In addressing limitations other than “where power consumption is independently controlled within each of the power islands,” for example, Petitioner cites a disclosure where an operating system running on PE 100 in Nicol’s Figure 2 is described as changing the common clock frequency of PEs 101-104 so “that the most heavily loaded PE [of PEs 101-104] carries out its assigned tasks within the required completion time.” Pet., 63 (quoting Ex. 1008 [Nicol] 3:66-4:6). This disclosure does not suggest that any similar changes occur in any power characteristics of PE 100, which is the other one of only two things that Petitioner identifies as a “power island” in Nicol’s Figure 2. But the claim requires “a plurality of power islands,” and for “power consumption to be “independently controlled within *each* of the power islands”—not merely a single one of them.

Petitioner’s arguments regarding the alleged “power islands” in Nicol’s Figure 2 thus suffer from the same deficiency as its arguments concerning Nowka’s domains. Although Petitioner points to physically distinguishable components—potentially having separate voltage supply lines, or potentially having distinct clock sources—it never explains how this physical distinctness gives rise to “power consumption [being] independently controlled within *each*” of the purported plurality of “power islands.” Absent such an explanation, Petitioner has not shown

that the “power islands” it purports to identify in Figure 2 satisfy the claim, and its arguments therefore fail for similar reasons they did with respect to Petitioner’s identification of Nowka’s four “domains” as a “plurality of power islands.” See Section III.A.1.

2. Petitioner Fails To Identify A “plurality of power islands . . . where power consumption is independently controlled within each of the power islands” In Nicol’s Figure 4 Embodiment, Such That The Remainder Of Claim 1 Is Satisfied.

Petitioner’s second attempt to identify a “plurality of power islands . . . where power consumption is independently controlled within each of the power islands” begins by relying upon processing elements (“PEs”) and supporting circuitry as identified by Petitioner in its annotation of Nicol’s Figure 4:



Pet., 58 (Figure 4 of Nicol, as annotated by Petitioner); *see also*, e.g., Ex. 1008 [Nicol] 2:51(referring to “processing elements (PEs)” in discussing Figure 2); 2:44-

46 (referring to Figure 4 as a “multi-processor chip”), 6:12 (same). Petitioner asserts that “[i]n the Figure 4 embodiment, each PE (with its control circuitry) is a power island because each is a section, delineation, partition, or division of the integrated circuit and has an independent voltage and clock source, allowing for independent power control by varying supply voltage/frequency.” Pet., 58.

As explained in detail below, however, although Petitioner *begins* its Nicol analysis against claim 1 by pointing to the Figure 4 embodiment, which concerns processors and the allocation of computational tasks across multiple processors, *see, e.g.*, Pet., 56 (discussing task division among processors when introducing Nicol’s Figure 4 embodiment), Petitioner fails to adhere to this embodiment. When addressing later limitations—particularly those involving actions relating to changing power levels in power islands—Petitioner abruptly shifts to citing Nicol’s discussion of “fast memory” and a “hard drive,” as if they were “PEs” in Figure 4. *See, e.g.*, Pet., 61 (citing Ex. 1008 [Nicol] 6:39-56). But this discussion does not describe Figure 4 at all; this discussion appears after Nicol has finished describing Figure 4, and concerns “other system arrangements” in which PEs are replaced by “components that are not typically thought of as processor elements.” Ex. 1008 [Nicol] 6:38-39. This discussion of memory and hard drives also occurs in a discussion of what Nicol terms a “personal computer”—not “power islands” within an integrated circuit. *Cf.* Pet. 58 (arguing that something is a power island “because

each is a section, delineation, partition, or division of *the integrated circuit* and has an independent voltage and clock source, allowing for independent power control by varying supply voltage/frequency”).

Petitioner conflates two distinct contexts: Nicol’s disclosures of distributing computational tasks across multiple processors (the context of Nicol’s Figure 4, which is also the context of Nicol’s Figure 2), and a later hypothetical about extending certain design principles to non-processor components. But the challenged claims are not directed to abstract components of an arbitrary computer system, but to “an *integrated circuit* including a plurality of power islands.” Ex. 1001 [’306] 13:31-34. Nicol’s “fast memory” and “hard drive” are never shown to components of any integrated circuit that includes Nicol’s “PEs,” and Nicol’s discussion about a “fast memory” and “hard drive” does not involve any distribution of tasks among processors, let alone among the “PEs” of Nicol’s Figure 4.

Properly understood, Nicol’s Figure 4 addresses a limitation of its Figure 2 design in a context where a computation to be divided across multiple processing elements cannot be broken into tasks of similar processing time. *See* Section III.B.1 (describing Nicol’s Figure 2); *see also, e.g.*, Ex. 1008 [Nicol] 3:12-18 (stating that that “a scheduler within the operating system” on the PE 100 of Figure 2 might use information about “the number of instructions that need to be executed for each task” to determine “the best way to allocate the tasks to the available processors in order

to balance the computation”); *see also, e.g.*, 3:19-21 (referring to a “goal” in Nicol’s Figure 2 as being “to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PE’s”), 3:67–4:1 (describing the task of PE 100 in Nicol’s Figure 2 as being to “divide the collection of tasks as evenly as possible (in terms of needed processing time)”).

Nicol explains that where certain tasks cannot be evenly partitioned across processors, one PE may require a higher frequency and voltage to complete its tasks in a given time than other PEs. To change the frequency and voltage of a PE in Nicol’s Figure 2, however, requires scaling up the entire multiprocessor chip. *See, e.g., id.*, 5:57-65; *see also* Section III.B.1 (describing Nicol’s Figure 2). Nicol’s Figure 4 embodiment, by contrast, provides each PE in Figure 4 with its own controller, calibration circuit, and converter, *id.*, 5:67–6:12, and Nicol describes its operating system as capable of leveraging these additional layers of circuitry in contexts where a single PE might require a different frequency or voltage from others. *See id.* Nicol is silent on the details of how its operating system would actually manage task division or power consumption in an embodiment of Figure 4, *cf. id.*, 3:9-18 (describing how Figure 2 might operate “[i]f the number of instructions that need to be executed for each task is known and made available to the operating system”)—Nicol states, for example, that the Figure 4 embodiment “also has a PE 200 that assigns the *tasks given to the multi-processor chip* of FIG. 4 among the

PEs,” but does not elaborate on how PE 200 operates, or even graphically depict where “PE 200” might reside in Figure 4.⁴ *See id.*, 6:11-3. All of these disclosures, however, plainly concern processors tasked with computational loads of potentially varying processing time—as Petitioner acknowledges when introducing Nicol’s Figure 4 embodiment. *See, e.g.*, Pet., 55-56 (describing Figure 4 in terms of task division across multiple processors). These disclosures do not relate to Nicol’s operating system (or any other component of Nicol) choosing to store anything in “fast memory” or a “hard disk,” or otherwise affecting the power consumption of components that are not processors in the multi-processor chip of Figure 4.

Despite this, Petitioner’s analysis drifts away from the processors of Figure 4 when addressing the “determining a target power level” and “determining at least one of actions” steps of claim 1. For those limitations, Petitioner turns to a later discussion of “fast memory” and “hard drive” in Nicol, and even characterizes this discussion as if it is “[r]eferencing the Figure 4 embodiment.” *Id.*, 61 (citing Ex. 1008 [Nicol] 6:39-56). But Nicol itself introduces this discussion as an example of “other system arrangements,” expressly noting that it covers “components that are not typically thought of as processor elements.” Ex. 1008 [Nicol] 6:34-39. Far from

⁴ None of Nicol’s figures display any component labeled “200.” *See* Ex. 1008 [Nicol] Figs. 1-4.

describing additional features of Figure 4, this language introduces a separate discussion in which non-processor components of something other than an integrated circuit (what Nicol describes as “a personal computer,” Ex. 1008 [Nicol] 6:41) have power characteristics adjusted on some basis that does not relate to dividing tasks across processors. Petitioner’s suggestion that Figure 4’s processors and this later memory/storage passage form a single disclosure of a “an integrated circuit including a plurality of power islands” is therefore unfounded.

Petitioner’s conflation of processors in Figure 4 with unrelated examples involving memory and storage leaves it without a coherent showing of how Nicol teaches “an integrated circuit including a plurality of power islands . . . where power consumption is independently controlled within each of the power islands.” At some points, Petitioner treats the PEs of Figure 4—which are literally processors—as the alleged “power islands.” *See, e.g.,* Pet., 58-59; *see also* Pet. 57-58 (arguing that “Nicol improves the performance of *multi-processor chips* by dynamically controlling *the processing load of the chips* and further controlling the frequencies/voltages to minimize power consumption”). At others, Petitioner substitutes memory and a hard drive as alleged “power islands,” in an apparent *analogy* to the PEs of Figure 4. *See, e.g.,* Pet., 61; *see also* Pet., 64 (citing Ex. 1008 [Nicol] 6:39-56, which discusses memory and hard drives). But the claims require a consistent plurality of power islands, and Nicol does not provide one across these

different disclosures. As one example, while Nicol describes the PEs of its Figure 4 as receiving “*tasks*” from “a PE 200 that assigns the tasks given to the *multi-processor* chip of FIG. 4,” Ex. 1008 [Nicol] 6:2-13, Petitioner fails to explain how PE 200 or any other component in Figure 4 would assign “tasks” to memory or hard disk storage, or address whether and how the operation of Nicol’s “multi-processor chip of FIG. 4” would need to be modified if, as Petitioner implicitly proposes, some or all of its processing elements were to be replaced with memory and hard disk storage.

Rather than address these issues in its combination, Petitioner simply describes the memory and hard disk disclosures as (allegedly) “[r]efereencing the Figure 4 embodiment.” Pet., 61. In more detail, Petitioner states:

Referencing the Figure 4 embodiment, Nicol explains how “[i]t is possible to anticipate that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called. When so anticipated, some of the fast memory can be released (storing some of the data that needed to be remembered) at a leisurely pace. That is, lower clock frequency can be employed in connection with the fast memory and the hard drive, with a corresponding lower supply voltage, resulting in an overall power saving in both the memory’s operation and in the operation of the hard drive.”

Id. (quoting Ex. 1008 [Nicol] 6:39-56). For reference, the paragraph from Nicol that Petitioner quotes as “Referencing the Figure 4 embodiment,” *id.*, reads in full as

follows:

The principles disclosed above for a multiprocessor is [sic] extendible to *other system arrangements*. This includes systems with a plurality of separate processor elements that operate at different frequencies and operating voltages, as well as *components that are not typically thought of as processor elements*. For example, there is a current often-used practice to maintain program code and data for different applications of a *personal computer* in a fast memory. As each new application is called, more information is stored in the fast memory, until that memory is filled. Thereafter, when a new application is called, some of the information in the fast memory is discarded, some other information is placed in the slower hard drive, and the released memory is populated with the new application. It is possible to anticipate that memory stored in the fast memory is so old as to be unlikely to be accessed before a new application is called. When so anticipated, some of the fast memory can be released (storing some of the data that needed to be remembered) at a leisurely pace. That is, lower clock frequency can be employed in connection with the fast memory and the hard drive, with a corresponding lower supply voltage, resulting in an overall power saving in both the memory's operation and in the operation of the hard drive.

Ex. 1008 [Nicol] 6:34-52.

In hinting here at “other system arrangements” where “the principles disclosed above for a multiprocessor” might be applicable, *id.* at 6:34-35, Nicol is

expressly **not** describing further features of Nicol’s Figure 4, but **other** contexts where Nicol’s ideas could potentially be explored. The “fast memory” and “hard drive” of this disclosure—“components that are not typically thought of as processor elements,” *id.*, 6:38-39—are not processors in a multi-processor chip, *cf. id.*, 2:17-22 (“Summary of the Invention” beginning “Improved performance of **multi-processor chips** is achieved by dynamically controlling **the processing load of chips** and controlling, which significantly greater than on/off granularity, the operating voltages **of those chips** so as to minimize overall power consumption”). And Nicol expressly suggests that the power consumptions of the “fast memory” and “hard drive” of its hypothetical might be managed **together**, not independently. *Id.*, 6:52-56 (stating that in its hypothetical memory management context, a “lower clock frequency can be employed in connection with the fast memory **and** the hard drive, with a corresponding lower supply voltage, resulting in an overall power saving in **both** the memory’s operation and in the operation of the hard drive”).

Petitioner’s conflation of the properties of the “PEs” of Nicol’s Figure 4 with memory and hard drives in Nicol’s hypothetical recurs in Petitioner’s treatment of the claim step “determining at least one of actions to change a power consumption level of one of the power islands . . .” step of claim 1. After a page-long discussion of Figure 2’s task-based frequency- and voltage-determination mechanism (Pet., 62-63), Petitioner offers only a single sentence that “Nicol similarly discloses examples

of setting a lower frequency and lower supply voltage to match the needs of the system in an embodiment where it is desirable for different components to operate at different speeds (such as in Figure 4).” *Id.*, 63-64. Yet here, the only citation to Nicol is to the hard disk and memory passage, Ex. 1008 [Nicol] 6:39-56, not to any discussion of PEs in Figure 4. Pet., 63-64.

These disclosures are not “similar[]”—as Petitioner characterizes them—and if they were, Petitioner did not show any “plurality of power islands” in Nicol’s Figure 2 (*see* Section III.B.1), and the alleged “plurality of power islands” in Nicol’s Figure 4 (individual PEs in Figure 4) is different both from alleged “plurality of power islands” in Nicol’s Figure 2 (PE 100 of that figure, on the one hand, and the group of PEs 101-104 of that figure, on the other) and from “fast memory” and a “hard drive.” It is therefore not clear what argument Petitioner proposes to make on the basis of any alleged similarities between Nicol’s Figure 2 and Nicol’s Figure 4.

Petitioner’s failure to clearly identify the properties of the “plurality of power islands” it alleges to exist in Figure 4 dooms its obviousness case. At some times, the “power islands” are processors assigned computational tasks; at others, they are non-processor components such as memory or hard disk storage that are not even argued to be part of the same integrated circuit. Even in the context of single-reference obviousness, a motivation must exist for combining features of different embodiments or otherwise modifying the teachings of a reference. *See, e.g., In re*

Kotzab, 217 F.3d 1365, 1370 (Fed. Cir. 2000). By blending Nicol’s distinct disclosures (and by characterizing Nicol’s forward-looking hypotheticals as aspects of an embodiment) without explanation, Petitioner does not show how Nicol’s Figure 4 discloses “an integrated circuit including a plurality of power islands . . . where power consumption is independently controlled within each of the power islands,” as required by the claim.

IV. PETITIONER’S GROUNDS DO NOT TEACH OR RENDER OBVIOUS DETERMINING “A TARGET POWER LEVEL FOR ONE OF THE POWER ISLANDS” (ALL CHALLENGED CLAIMS, ALL GROUNDS).

Each claim requires determining (or involves a component configured to determine) “a target power level for one of the power islands” Ex. 1001 [’306] cls. 1, 16, 37.

A. Nowka Grounds (All Challenged Claims, Grounds 1A–1D).

As explained above, Petitioner has not shown that the four “domains” in Nowka’s Figure 3 (*see* Section III.A.1), nor that individual “cores” within Nowka’s logic domain (*see* Section III.A.2), constitute “a plurality of power islands . . . where power consumption is independently controlled within each of the power islands.” For at least this threshold reason, Petitioner cannot show that its Nowka grounds teach determining “a target power level for one of the power islands” either.

If the Board were somehow inclined to credit Petitioner’s statement that the individual “cores” within Nowka’s logic domain constitute “a plurality of power islands,” however, Petitioner’s arguments fail for the additional reason that Petitioner does not show “determining a target power level” *for these alleged power islands*: Petitioner’s discussion of this limitation focuses upon higher-level characteristics of Nowka’s system than power levels of individual cores within Nowka’s logic domain. *See* Pet., 11 (reproducing Nowka’s Table II, entitled “CPU Core With Caches Characteristics”), 12 (alleging evidence of “target power levels” in “the power consumption results of voltage scaling while running Dhrystone2.1 benchmark (Figure 5) and MPEG-4 decoding (Figure 6) on the SOC”); *see generally* Ex. 1004 [Nowka] 1444 (Section III.C, “Measured DVS Results,” discussing the benchmarks without reference to individual cores); *see also id.* (Section V, describing a Dhrystone benchmark as reported in Figure 8, but referring to changes in “the logic supply” throughout); *see also* Pet. 10-13 (citing and discussing these disclosures).

Petitioner does make passing reference to “unit and register level functional clock gating” and “standby modes” as examples of actions taken by Nowka “to reduce the power level ‘when resource demands are low,’” *id.*, 11 (quoting Ex. 1004 [Nowka] 1442), and does allege that these actions involve “determining a target power level”—but only in the most conclusory terms. After stating that Nowka

discloses “clock gating inactive registers and cores, as well as putting the system in various standby modes, which changes the power state of the logic domain, when certain registers and units, or the entire logic domain, does not need to be active,” for example, Petitioner simply says: “A POSITA would have found it obvious that each of these actions involves determining a target power level, not only for the reasons discussed above, but also because these actions were well-understood in the art as mechanisms for adjusting power levels.” *Id.*, 13.

But this logic is facially wrong. A laptop on/off switch adjusts the power level of a device but does not involve any determination of a “target power level” of the device, much less a determination “based on needs and operation of the integrated circuit” (as the challenged claims further require). And despite reciting this list of various examples of “actions” allegedly disclosed in Nowka, Petitioner does not even attempt to identify what determination of a “target power level” a POSITA might have understood to have been made in each case. Petitioner effectively says only that a POSITA would have understood that the claim language was satisfied. Being nonspecific and unsupported, this argument should be rejected. *See Novartis AG v. Torrent Pharms.*, 853 F.3d 1316, 1326 n.2 (Fed. Cir. 2017) (finding that an argument presented by one conclusory sentence “amount[ed] to little more than a request that the Board peruse the cited evidence and piece together a coherent argument on [a party’s] behalf”).

B. Nicol Grounds (All Challenged Claims, Grounds 2A–2D).

As explained above, Petitioner has not shown that the PE 100 and PEs 101-104 in Nicol’s Figure 2 embodiment constitute “a plurality of power islands” that satisfy the challenged claims (*see* Section III.B.1), nor that the “PEs” within Nicol’s Figure 4 embodiment constitute “a plurality of power islands” that satisfy the challenged claims. *See* Section III.B.2. For at least this threshold reason, Petitioner cannot show that its Nicol grounds teach determining “a target power level for one of the power islands based on needs and operation of the integrated circuit” either.

If the Board were somehow inclined to credit Petitioner’s statement that the PEs in Nicol’s Figure 4 might constitute “a plurality of power islands,” however, Petitioner’s arguments fail for the additional reason that Petitioner does not show “determining a target power level” *for these alleged power islands*. The only express identification of an alleged “target power level[s]” made by Petitioner in connection with this limitation is alleged to take place within Nicol’s Figure 2, where a target power is supposedly “set ‘to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PE’s.’” Pet., 60 (quoting Ex. 1008 [Nicol] 3:19-21); *see generally id.*, 60-61.

Petitioner states in passing that “in Nicol, this determining of the target power level is performed by the controlling operating system—e.g. the real time operating system (RTOS) in PE 100 in the Figure 2 embodiment *and the operating system in*

the ‘controller’ in the Figure 4 embodiment.” *Id.*, 60. But this remark at most identifies what **component** Petitioner suggests could be capable of determining a “target power level” in Nicol’s Figure 4, not what any “target power level” actually is in that embodiment or on what basis it is determined. And Petitioner’s ensuing discussion of the “fast memory” and “hard drive” disclosure, *id.*, 61—as if it were a disclosure about the Figure 4 embodiment, which it is not (*see* Section III.B.2)—does not close this gap, as the “fast memory” and “hard drive” components are not parts of any alleged “**integrated circuit** including a plurality of power islands” as required by the claims, and these components are not part of Nicol’s Figure 4, nor does any hypothetical action with these components involve the division of a computational task across multiple processors (as Petitioner’s earlier discussion of Nicol does).

“It is not the Board’s job to cobble together assertions from different sections of a petition or citations of various exhibits in order to infer every possible permutation of a petitioner’s arguments. Arguments in a petition must be made with particularity, not opacity.” *See Microsoft Corp. v. FG SRC, LLC*, 860 Fed. App’x. 708, 713 (Fed. Cir. 2021) (nonprecedential); *see also Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (“A petitioner may not rely on a vague, generic, and/or meandering petition and later fault the Board for failing to understand what

the petition really meant. Ultimately, it is the petitioner's burden to present a clear argument.").

As a last resort, Petitioner argues that essentially any change in frequency in any component of any system "is determining a target power level based on needs and operation of the integrated circuit because frequency is directly proportional to power and voltage is quadratically related to power." Pet., 61-62. Of course, Petitioner styles this argument as a statement particular to "Nicol's operating system," but Petitioner's reasoning is not so limited. If adopted, Petitioner's reasoning would conflate at least claim 1's "determining a target power level" step and claim 1's "performing the at least one of the actions to change the power consumption level . . . where one of the actions comprises selecting a frequency" steps, if not also the "determining at least one of actions to change a power consumption level" step. But "[d]ifferent claim terms are presumed to have different meanings," *Bd. of Regents v. BENQ Am. Corp.*, 533 F.3d 1362, 1371 (Fed. Cir. 2008), and Petitioner gives no analysis of why it would be appropriate in this case not to "giv[e] effect to all terms in the claim." See, e.g., *Becton Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1257 (Fed. Cir. 2010).

V. PETITIONER’S GROUNDS DO NOT TEACH OR RENDER OBVIOUS THE “DETERMINING AT LEAST ONE OF THE ACTIONS” AND “PERFORMING THE AT LEAST ONE OF THE ACTIONS” STEPS (ALL CHALLENGED CLAIMS, ALL GROUNDS).

The claims require not just a determination of a “target power level” “based on needs and operation of the integrated circuit” (*see* Section IV), but that there also be a determination of “at least one of actions to change a power consumption level . . . to the target power level” and “performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level” Ex. 1001 [’306] cls. 1, 16, 37.

Petitioner’s analysis of these limitations fails, for example, because the cited art already fails to teach the determination of a “target power level” in the sense required by the claims. *See* Section IV. In listing “actions” disclosed in Nowka that may affect power consumption in connection with this limitation, for example, *see, e.g.,* Pet., 16-17, or in describing adjustments to frequencies and supply voltages in Nicol, *see, e.g.,* Pet., 63-64, Petitioner is simply inviting the Board to presume that any disclosure of an “action” affecting power consumption *necessarily* involves a determination to take that action to change power consumption to a previously recited “target power level” that was determined “based on needs and operation of the integrated circuit.” But the Petition does not show that these references ever teach a “target power level” determined as the claim requires (*see* Section IV)—and

Petitioner’s arguments regarding “performing the at least one of the actions to change the power consumption level of the one of the power islands . . .” simply summarize Petitioner’s arguments about previous limitations. *See* Pet., 17 (explaining that Nowka teaches this step “[a]s discussed at Elements_1[a]-1[b]”), 64 (explaining that Nicol teaches this step “[a]s discussed at Elements_1[a]-1[b]”).

VI. CONCLUSION.

For each of the foregoing reasons, the Board should not institute trial.

Dated: October 8, 2025

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITS

This Patent Owner Preliminary Response (the “POPR”) consists of 11165 words, excluding table of contents, table of authorities, certificate of service, this certificate, and table of exhibits. The POPR complies with the type-volume limitation of 14,000 words as mandated in 37 C.F.R. § 42.24. In preparing this certificate, counsel has relied on the word count of the word-processing system used to prepare the paper (Microsoft Word).

Dated: October 8, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §42.6(e), I hereby certify that on October 8, 2025, I electronically filed the following documents:

PATENT OWNER'S PRELIMINARY RESPONSE

EXHIBIT 2027

and served a copy of the same on counsel for Petitioner at the following e-mail address, as authorized in the Petition:

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