

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK, INC.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

IPR2024-00719
Patent 7,945,885 B2

Before KEN B. BARRETT, JOHN F. HORVATH, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

MediaTek Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–64 of U.S. Patent No. 7,945,885 B2 (Ex. 1001, “the ’885 Patent”). MOSAID Technologies, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 8, “Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). For the reasons discussed below, we determine that the reasonable likelihood standard is met, and we institute *inter partes* review.

II. BACKGROUND

A. *Related Matter*

The parties identify the following district court action involving the ’885 Patent: *MOSAID Technologies Inc. v. MediaTek, Inc.*, No. 2:23-cv-00129-JRG (E.D. Tex.) (hereinafter, “the related litigation”). Pet. 101; Paper 6, 1 (Patent Owner’s updated mandatory notices).

A. *The ’885 Patent (Ex. 1001)*

The ’885 Patent is titled “Power Managers for an Integrated Circuit” and was issued based on a regular application filed July 21, 2008. Ex. 1001, codes (22), (54). The ’885 Patent lists a series of related applications, the earliest of which is a provisional application filed May 7, 2004. *Id.* at code (60). According to the ’885 Patent, “[o]ne design goal for integrated

circuits is to reduce power consumption.” *Id.* at 1:28–29. The ’885 Patent states, “[s]ome prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption,” but “[o]ne problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static” and “do not dynamically change based on the needs and operation of the integrated circuit.” *Id.* at 2:19–25.

Figure 2 of the ’885 Patent is reproduced below.

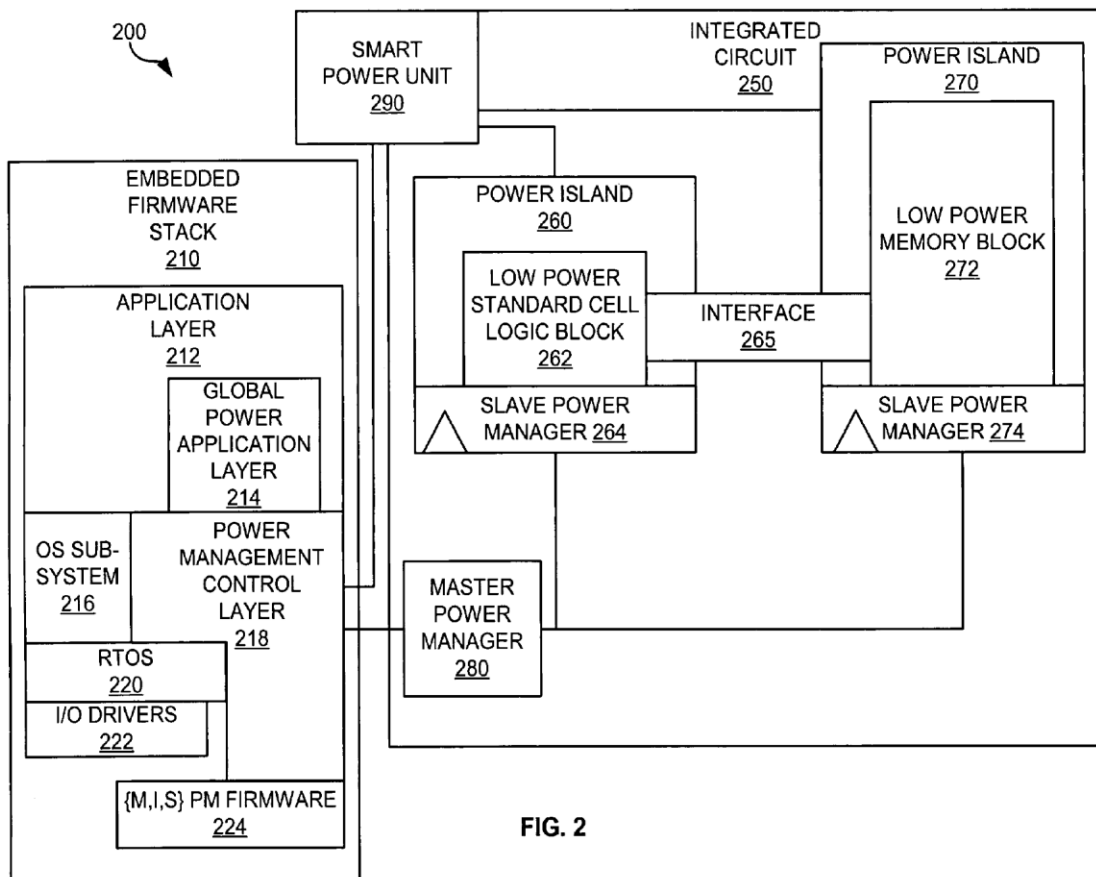


FIG. 2

Figure 2 shows a system for managing power in integrated circuit 250. Ex. 1001, 2:62–63, 4:59–61. The system includes embedded firmware stack 210, which runs on a central processing unit (CPU) and includes application layer 212 and power management control layer (PMCL) 218. *Id.* at 4:61–5:2. Integrated circuit 250 includes power islands 260 and 270,

master power manager (MPM) 280, and smart power unit (SPU) 290. *Id.* at 5:3–4, 5:38–41, Fig. 2; *see also id.* at 4:37–41 (explaining acronyms). Power island 260 includes slave power manager (SPM) 264, and power island 270 includes SPM 274. *Id.* at 5:4–7.

According to the '885 Patent, the integrated circuit may be a system-on-a-chip that includes “multiple IP units, which are blocks of circuitry performing specific functions.” Ex. 1001, 2:12–15, 3:46–49. The '885 Patent explains that a power island is “any section, delineation, partition, or division of the integrated circuit” within which “power consumption is controlled,” and the power islands may be “delineated based on geographic factors of the integrated circuit . . . [or] based on functional IP units of the integrated circuit.” *Id.* at 3:56–64.

Figure 5 of the '885 Patent is reproduced below.

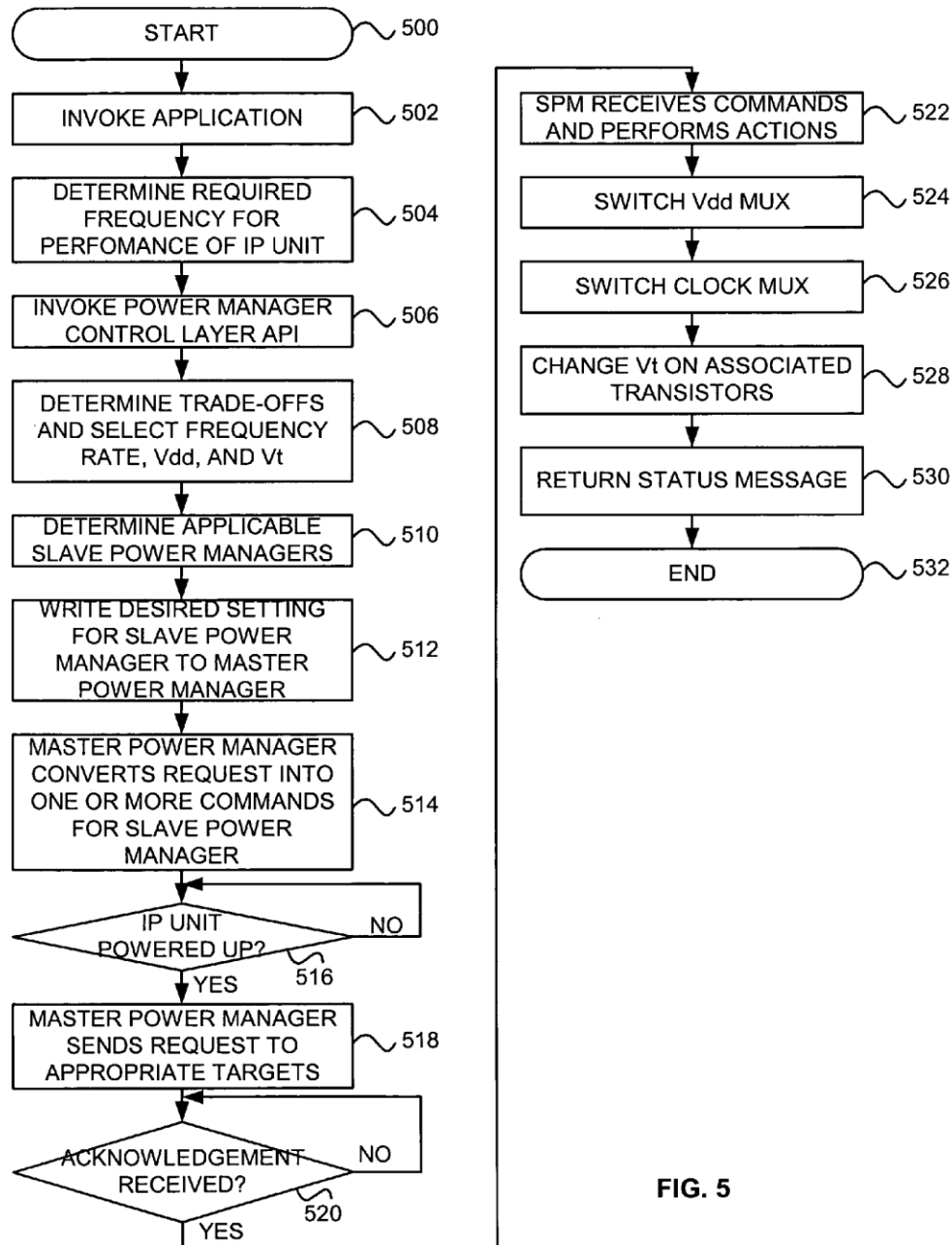


FIG. 5

Figure 5 is a flowchart from an application request to an SPM action. Ex. 1001, 3:3–5, 7:36–37. In step 502, an application is invoked, such as playing a movie. *Id.* at 7:38–39. In step 504, the application determines the required frequency for performance of an IP unit, for example, a specified frequency for an IP unit for an MPEG decoder. *Id.* at 7:39–42. In step 506, the application invokes PMCL 218 application program interface (API) call.

Id. at 7:48–49; *see also* 5:13–15 (explaining acronym). In step 508, PMCL 218 determines possible trade-offs available for the IP unit and selects a frequency rate, Vdd, and Vt that best meets the given requirements and, in step 510, determines the applicable SPMs 264 and 274. *Id.* at 7:58–62.¹ In step 512, PMCL 218 writes the selected settings for SPMs 264 and 274 to MPM 280, which converts the settings into commands (step 514) and sends them to SPMs 264 and 274 (step 518). *Id.* at 7:66–8:14, Fig. 5. In steps 522 to 528, SPM 264 performs the commanded actions by, e.g., switching a Vdd mux, switching a clock mux, or changing the Vt on the associated transistors. *Id.* at 8:19–25, Fig. 5.

Figure 8 of the '885 Patent is a flowchart from an application request to an SPU action. Ex. 1001, 3:10–12, 8:51–52. Steps 802 to 810 are similar to steps 502 to 510 of Figure 5. *Compare id.* at 7:38–63, Fig. 5 (steps 502 to 510), *with id.* at 8:53–9:3, Fig. 8 (steps 802 to 810).

B. Illustrative Claim

Petitioner challenges all 64 claims of the '885 Patent, of which claims 1, 8, 16, 23, 31, 39, 48, and 56 are independent. Claim 1 is reproduced below:

1. An integrated circuit comprising:
 - [1a] an integrated circuit chip;
 - [1b] a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

¹ “Vdd” refers to “dynamic voltage source” (Ex. 1001, 4:54–57), and Vt refers to threshold voltage (*id.* at 7:1–3).

[1c] one or more power consumption signals indicating one or more of the power consumptions;

[1d] a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

Ex. 1001, 13:19–37 (bracketed designations added to correspond with Petitioner’s identification of claim elements). Independent claims 8, 16, 23, 31, 39, 48, and 56 are similar to claim 1. *Id.* at 13:57–14:6, 14:33–50, 15:4–21, 15:47–63, 16:17–31, 16:56–17:5, 17:26–18:7.

C. Asserted Challenges and Evidence

Petitioner raises the following challenges to patentability.

Claims Challenged	35 U.S.C. § ²	References/Basis
1–64	103	Nowka, ³ Borkar ⁴

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, amended §§ 102 and 103 of Title 35, effective March 16, 2013. Because the filing date of the ’885 Patent is before this date, we refer to the pre-AIA versions of §§ 102 and 103. Ex. 1001, code (22).

³ Ex. 1004, *A 32-bit Power PC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling*, 37 (11) IEEE J. of Solid-State Circuits 1441 (2002) (“Nowka”). Petitioner contends that Nowka is prior art under § 102(a). Pet. 2.

⁴ Ex. 1006, US 6,484,265 B2, issued November 19, 2002 (“Borkar”). Petitioner contends that Borkar is prior art under § 102(e). Pet. 2.

Claims Challenged	35 U.S.C. § ²	References/Basis
1–64	103	Nicol, ⁵ Borkar

Pet. 1–2. Petitioner submits the Declaration of Tajana Rosing, Ph.D.
Ex. 1003.

III. ANALYSIS

A. *Legal Standards*

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level

⁵ Ex. 1008, US 6,141,762, issued October 31, 2000 (“Nicol”). Petitioner contends that Nicol is prior art under § 102(b). Pet. 2.

of ordinary skill in the art; and (4) when presented, objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

At this stage of the proceeding, there is no dispute about the level of ordinary skill in the art. Based on the testimony of Petitioner’s declarant, we determine that a person of ordinary skill in the art (“POSITA”) would have had a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. Ex. 1003 ¶ 21. We find that the level of ordinary skill in the art, as articulated above, is consistent with the level of technical understanding and competence reflected in the ’885 Patent Specification and the asserted prior art references.

C. Claim Construction

In an *inter partes* review, we apply the same claim construction standard as would be used by a district court to construe a claim in a civil action involving the validity or infringement of a patent. 37 C.F.R. § 42.100(b). Under that standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc); *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012). “The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

We determine that it is not necessary to provide an express construction for any claim term for purposes of deciding whether to institute review.

Patent Owner argues that the Petition should be denied for failing to address the construction of “power island.” Prelim. Resp. 11–17. We disagree. Petitioner adequately identifies the definition it applies when analyzing the prior art. Pet. 21–22 (citing Ex. 1001, 3:56–59).

D. Petitioner’s Challenge based on Nowka and Borkar

Petitioner contends that claims 1–64 are unpatentable as obvious based on Nowka and Borkar. Pet. 6–60. Patent Owner opposes. Prelim. Resp. 1–30. We begin with overviews of Nowka and Borkar.

1. *Nowka (Ex. 1004)*

Nowka is journal article titled, “A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling.” Ex. 1004, 1441.⁶ Nowka describes a system-on-a-chip (SOC) processor that uses “dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.”

Under the heading, “System Overview,” Nowka asserts that the SOC “makes use of active power reduction techniques to dynamically match the power consumption with the requirements of the application.” Ex. 1004, 1442 (lefthand column). According to Nowka, “[t]he active power consumption is reduced when resource[] demands are low through the use of dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating.” *Id.*

Under the heading, “Dynamic Voltage Scaling,” Nowka states, “[t]he primary means of matching the performance and power consumption of this device to the application is through the use of dynamic voltage scaling (DVS),” which “adjust[s] the supply voltage dynamically to meet the performance demands while minimizing power consumption.” Ex. 1004, 1442 (righthand column).

Under the subheading, “Dynamic Voltage Scaling Architecture,” Nowka discloses, “[t]o support DVS in this SOC, the power distribution has been divided into four distinct domains,” consisting of “two persistent

⁶ We refer to the original page numbers of Nowka, not those added by Petitioner.

voltage domains, one dynamically voltage-scaled logic domain and one internally derived domain.” Ex. 1004, 1442 (righthand column). The four domains are shown in Figure 3, which identifies an “SOC Logic DVS Supply Domain,” a “Regulated 1.0V PLL Supply Domain,” a “Persistent 3.3V I/O Supply Domain,” and a “Persistent 1.8V Battery-Backed Domain.” *Id.* at 1443, Fig. 3.

Under the heading, “Scalable Clocking Subsystem,” Nowka discloses that “on-the-fly frequency modification techniques can be used to provide dynamic frequency scaling for additional active power reduction.”

Ex. 1004, 1444 (righthand column). According to Nowka, “[w]hen the performance demands of the application decrease, the system software can lower the operating frequency.” *Id.* Nowka discloses that, “[u]nder software control, at a given supply voltage, the frequency of the core can be varied from the maximum frequency down to 1/64th of the maximum.” *Id.*

Nowka discusses Figure 8 under the heading, “Dynamic Voltage and Frequency Scaling Measurements.” Ex. 1004, 1444 (righthand column). Figure 8 shows voltage versus time traces for the total SOC power, the SOC logic power, the SOC I/O power, and the SOC logic supply voltage (Vdd). *Id.* at 1444–45 (righthand column, Fig. 8). Figure 8 shows how power is affected by changes in frequency⁷ and logic supply voltage under control of the clock and power management software. *Id.*

Under the heading, “Active Power Management,” Nowka states that dynamic voltage scaling and dynamic frequency scaling are used to reduce

⁷ According to Nowka, the clock and power management adjusts the frequency by modifying the output clock divider of the phase locked loop (PLL). Ex. 1004, 1444 (righthand column under the heading “Scalable Clocking Subsystem”).

the power consumption of the processor and control power consumption “on a very fine time scale.” Ex. 1004, 1445 (lefthand column). According to Nowka, “[t]hrough voltage and frequency scaling and clock gating, the performance/watt of this design can be varied by more than a factor of four.” *Id.* (righthand column).

Under the heading “Standby Power Management,” Nowka discloses that “[s]everal modes of standby operation are employed to achieve a range of standby power levels.” Ex. 1004, 1446 (lefthand column). According to Nowka, “[t]he on-chip clock and power supervisor, in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to control the standby power.” *Id.*

By way of summary, Nowka states, “[u]nder software control, both the voltage and the frequency of the processor can be modified, thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption.” Ex. 1004, 1446 (righthand column). According to Nowka, “[b]y applying these techniques,” high frequencies and low power consumption can be achieved, “thereby dynamically adapting to the changing needs for performance and power demanded by the applications.” *Id.*

2. *Borkar (Ex. 1006)*

Borkar relates to integrated circuits (also called chips) and discloses using control circuitry and software to control transistor body bias, supply voltage, and clock frequency to control chip parameters, including performance, power consumption, and temperature. Ex. 1006, code (57), 1:8–18. Borkar explains that “[b]ody bias refers to the relationship between voltage of the source (V_{source}) of a field effect transistor (FET transistor)

and voltage of the body (V_{bb}) of the FET transistor.” *Id.* at 3:34–36.

Borkar further explains that the threshold voltage (V_t) of a transistor depends on the relationship between V_{bb} and V_{source} . *Id.* at 3:46–49.

Borkar discloses control circuitry for changing the body bias, supply voltage, and/or clock signal settings to control parameters of the processor, including temperature and power consumption. Ex. 1006, 2:61–3:2, 4:3–5, 4:12–32 (responses to changes in temperature), 4:57–5:10 (power considerations), Figs. 1, 2 (voltage and frequency control circuitry 118, 144). In this context, Borkar discloses:

In some embodiments, when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the threshold voltages of some or all of the transistors. This will reduce the power consumption to maintain the battery.

Id. at 5:25–30. Borkar states there are “tradeoffs” between processor performance and power consumption and “a high processor performance can be achieved” by “providing proper settings with each of supply voltage, clock frequency, and threshold voltages.” *Id.* at 6:15–23.

Borkar discloses that determination of the body bias, supply voltage, and/or clock settings “may occur by circuitry in [the] peripheral interface . . . in response to software control of [the] operating system . . . and/or a program, rather than in hardware as in control circuitry.” Ex. 1006, 7:51–65, Figs. 3, 4. According to Borkar, the control circuitry and peripheral interface (Figs. 1–4) are “not restricted to [a] single chip” and “may also be used to control the settings for more than one chip (e.g., multiple processors).” *Id.* at 9:20–24.

Borkar also discloses “circuitry to detect mismatches of transistor parameters in different groups of transistors and to correct the mismatches by providing different signals levels to the different groups of transistors.” Ex. 1006, 9:65–10:2. Borkar explains that the fabrication process may result in transistor parameter variations between two groups of transistors or domains, “[f]or example, a first domain as a whole may perform differently than a second domain as a whole.” *Id.* at 9:25–31, 9:48–55. Borkar’s Figures 5 and 7 show domains 234 and 238 and control circuitry 262, which is used to reduce mismatch by providing a clock signal, a body bias signal, and a supply voltage signal to each domain. *Id.* at 11:22–27, 11:40–43, 11:55–58, 13:8–11, Figs. 5, 7. According to Borkar, the goals of detecting and reducing mismatch include “keeping power consumption below a particular level, keeping temperature in a particular range, obtaining the highest possible performance, and obtaining the highest performance while not exceeding a particular power consumption level.” *Id.* at 12:10–15.

3. *Analogous Art*

Petitioner asserts that “[t]he ’885 patent relates to managing power on an integrated circuit (‘IC’) using power islands.” Pet. 2. According to Petitioner, one problem addressed by the ’885 Patent is “that power consumption is not efficiently utilized.” *Id.* (citing Ex. 1001, 1:66–67).

Petitioner contends that Nowka and Borkar “are related to the same field: power management of integrated circuits on a chip” and that both references address “the need to balance performance and power consumption” in an integrated circuit. Pet. 13–14. Petitioner contends that Nowka and Borkar both teach “operating distinct parts of the integrated circuit using different operating parameters” and “controlling power

consumption by changing the same quantities: supply voltage and operating frequency.” Pet. 14, 15; *see also* Pet. 16, 21, 25–27 (asserting that “Nowka discloses a power island (logic domain)” and Borkar teaches multiple domains).

Patent Owner argues that Borkar is nonanalogous art (Prelim. Resp. 1–10), asserting that “Borkar and the ’885 patent and do not share the same field of endeavor” (*id.* at 2) and Borkar is not “reasonably pertinent to the problem the inventors of the ’885 patent were trying to solve” (*id.* at 8).

After considering the parties’ arguments and evidence, we determine that the record is sufficient to support institution. Petitioner alleges facts relevant to a determination that Borkar is analogous art. Pet. 2–3, 13–15. Although Petitioner’s contentions are framed in terms of the similarities between Nowka and Borkar, Petitioner’s contentions are also relevant to a comparison between the ’885 Patent and Borkar. *Id.* Patent Owner argues that Petitioner does not address whether the ’885 Patent and Borkar share the same field of endeavor and only contends that Borkar shares the same field with *other references*. Prelim. Resp. 6. But Petitioner was not required to anticipate and raise analogous art arguments in the Petition. *Sanofi-Aventis Deutschland GmbH v. Mylan Pharmaceuticals Inc.*, 66 F.4th 1373, 1377 (Fed. Cir. 2023).

“A prior art reference is analogous and thus can be used in an obviousness combination if it ‘is from the same field of endeavor, regardless of the problem addressed’ or ‘is reasonably pertinent to the particular problem with which the inventor is involved,’ even if it is not within the inventor’s field of endeavor.” *Tinnus Enterprises, LLC v. Telebrands Corp.*, 846 F.3d 1190, 1207 (Fed. Cir. 2017) (citing *Unwired Planet, LLC v.*

Google Inc., 841 F.3d 995, 1000–01 (Fed. Cir. 2016); *In re Clay*, 966 F.2d 656, 658–59 (Fed. Cir. 1992)).

Here, the parties agree that the '885 Patent's field of endeavor is managing power on integrated circuits using power islands. Pet. 2; Prelim. Resp. 3–4 (citing Ex. 1001, 1:23–25). We agree with Petitioner that Borkar's field of endeavor is power management of integrated circuits on a chip. Pet. 13; Ex. 1006, code (57), 1:8–18, 2:49–57. We also agree with Petitioner that Borkar's power management solution involves “using distinct units on an integrated circuit whose power can be independently controlled,” i.e., “domains” in Borkar's terminology and “power islands” in the terminology of the '885 patent. Pet. 14–15, 25–27, 62; Ex. 1001, 3:59–62; Ex. 1006, 9:48–64, 10:30–42, 12:62–13:30, Figs. 5, 7. Patent Owner asserts that Borkar focuses on transistor body bias. Prelim. Resp. 5. In our view, however, Patent Owner's characterization of Borkar's field of endeavor is overly narrow. *See Unwired Planet*, 841 F.3d at 1001 (“The field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field.”).

If Patent Owner raises a nonanalogous art argument at trial, then based upon the present record, it appears likely that Petitioner will succeed in arguing that Borkar is from the same field of endeavor as the '885 Patent. In view of this preliminary finding, we do not need to consider whether Borkar is reasonably pertinent to the particular problem addressed by the '885 Patent. *See In re Asset Guard Prod., Inc.*, No. 2021-1902, 2022 WL 1097363, at *3 (Fed. Cir. Apr. 13, 2022) (A determination that a prior art reference is from the same field of endeavor as the challenged patent “is a

sufficient basis to affirm the Board’s decision that the references are analogous art.”).

4. *Reasons to Combine*

Petitioner contends that Nowka and Borkar both relate to power management of integrated circuits on a chip and that both references describe balancing performance and power consumption, operating distinct parts of the integrated circuit using different operating parameters, and controlling power consumption by changing supply voltage and operating frequency. Pet. 13–15 (citing Ex. 1003 ¶¶ 54–57). Petitioner contends that a POSITA would have modified Nowka in view of Borkar’s teachings about multiple domains, monitoring power consumption level, and threshold voltage tuning.⁸ Pet. 16–18 (citing Ex. 1003 ¶¶ 58–61).

Patent Owner argues that Petitioner has not proven a motivation to combine Nowka and Borkar or a reasonable expectation of success, as it pertains to a “plurality of power islands” as recited in the independent claims. Prelim. Resp. 17–30.

After considering the parties’ positions, we determine that Petitioner’s contentions and evidence, as summarized above, meet the threshold for instituting review.

Patent Owner argues that Petitioner “provides no convincing account of why a POSITA would be motivated to modify Nowka’s speech accelerator in view of Borkar’s multiple domains to arrive at the claimed invention or that a POSITA could do so with a reasonable expectation of

⁸ Petitioner’s contention about threshold voltage tuning relates to dependent claims 3, 10, 18, 25, 33, 41, 50, and 58. See Ex. 1001, 13:41–44; Pet. 42–43.

success.” Prelim. Resp. 20. On the current record, we disagree. Petitioner contends that a POSITA would have expanded Nowka’s variable power domain to multiple domains, as taught by Borkar, and this modification would have provided several benefits, including “more control over the SOC’s power consumption” and “greater granularity in power control and thus improved power savings.” Pet. 16, 24. Furthermore, Petitioner contends that its proposed modification “would be straightforward to accomplish because Nowka already has a variable power domain.” Pet. 16. Petitioner contends that Nowka’s speech accelerator would have been “one way to implement” an additional variable power domain in Nowka’s SOC, and this example would have allowed “independent operation of the speech accelerator” and “more control and precision for managing the power consumption in the speech accelerator.” Pet. 16–17, 24. We disagree with Patent Owner characterization of Petitioner’s contentions as “conclusory” and “unsubstantiated.” Prelim. Resp. 27, 28. Although Petitioner’s contentions may be disputed at trial, we find they are adequate for purposes of institution.

Patent Owner argues that Borkar’s multiple domains relate to groups of mismatched transistors, that Nowka’s speech accelerator has nothing to do with mismatched transistors, and that Petitioner stitches together “ill-fitting teachings.” Prelim. Resp. 21–22. On the current record, we disagree. Petitioner identifies a number of similarities between Nowka and Borkar, including that both references are concerned with power consumption in an integrated circuit and both references disclose multiple domains. Pet. 13–14. The cited disclosures in Borkar are not limited to mismatched transistors. Pet. 10–12 (providing an overview of Borkar); Pet. 16 (discussing motivation to combine and citing Ex. 1006, 1:20–21, 2:49–57, 5:45–46,

9:19–24, 10:34–39, Fig. 5); Pet. 25–26 (addressing claim element [1b] and citing Ex. 1006, 9:58–59, 10:30–11:39, Figs. 5, 7). And Petitioner discusses Nowka’s speech accelerator as an “example of one way to implement multiple variable power domains.” Pet. 16, 24. Although reasons to combine remain an issue for trial, Petitioner’s contentions are adequate for purposes of institution.

Patent Owner argues that Petitioner incorrectly interprets a statement in Nowka and takes a quote out of context. Prelim. Resp. 29 (citing Pet. 25; Ex. 1004, 1445). We find it unnecessary at this stage of the proceeding to determine which party correctly interprets a particular statement in Nowka. We determine that Petitioner’s contentions are sufficiently supported by the evidence as a whole and adequate for purposes of institution.

Patent Owner argues that Petitioner addresses “only motivation to combine Nowka-Borkar but not reasonable expectation of success.” Prelim. Resp. 24. We disagree. Citing declarant testimony, Petitioner contends that implementation of the proposed modification would have been “straightforward.” Pet. 16, 27 (citing Ex. 1003 ¶¶ 58, 72). *See Juniper Networks, Inc. v. Correct Transmission, LLC*, No. 2023-1046, 2024 WL 3517862, at *4 (Fed. Cir. July 24, 2024) (“A party does not need to use the phrase ‘reasonable expectation of success,’ ‘likelihood of success,’ or some other set of magic words, to establish a reasonable expectation of success.”).

Disputing Petitioner’s contention, Patent Owner argues that “[s]ignificant modifications to the circuit design were required’ to support the dynamic voltage scaling system in Nowka” and “[t]hese modifications resulted in performance degradation.” Prelim. Resp. 23 (citing Ex. 1004, 1443–1444). On the current record, we disagree. Nowka’s statement about “[s]ignificant modifications” pertains to the circuit design without dynamic

voltage scaling. Ex. 1004, 1443. In contrast, Petitioner’s proposed modification pertains to Nowka’s circuit design that already includes dynamic voltage scaling. See Pet. 16 (“This would be straightforward to accomplish because Nowka already has a variable power domain.”). Furthermore, Patent Owner’s argument about performance degradation does not appear to be supported by Nowka. Ex. 1006, 1444 (“The processor core, when modified to support DVS, occupies the same area and achieves equivalent performance at the nominal voltage supply as the unmodified core in the same technology.”). Although reasonable expectation of success remains an issue for trial, Petitioner’s contentions are adequate for purposes of institution.

5. *Independent Claims 1, 8, 16, 23, 31, 39, 48, and 56*

As discussed above, claims 1, 8, 16, 23, 31, 39, 48, and 56 contain similar recitations. Although we refer explicitly to claim 1, our analysis applies equally to claims 8, 16, 23, 31, 39, 48, and 56.

a) *Claim 1 Preamble*

The claim 1 preamble recites, “An integrated circuit.”
Ex. 1001, 13:19.

Petitioner contends that Nowka and Borkar each disclose an integrated circuit. Pet. 18–19 (citing Ex. 1004, 1441, Fig. 2; Ex. 1006, 2:49–52).

Patent Owner does not dispute Petitioner’s contentions for the claim 1 preamble, which we find are sufficiently supported by the cited evidence and adequate for purposes of institution.

b) Claim Element [1a]

Claim element [1a] recites “an integrated circuit chip.” Ex. 1001, 13:20.

Petitioner contends that Nowka discloses an integrated circuit chip, and Borkar discloses an integrated circuit. Pet. 20–21 (citing Ex. 1004, Abstract, Figs. 1, 2; Ex. 1006, 2:49–60, 4:5–9).

Patent Owner does not dispute Petitioner’s contentions for claim element [1a], which we find are sufficiently supported by the cited evidence and adequate for purposes of institution.

c) Claim Element [1b]

Claim element [1b] recites “a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency.” Ex. 1001, 13:21–25.

Petitioner contends that the Nowka-Borkar combination renders obvious claim element [1b]. Pet. 21–27. Petitioner contends that Nowka’s logic domain is “a power island . . . with an associated power consumption that is independently controllable by changing a supply voltage and operating frequency.” Pet. 21–24 (citing Ex. 1004, 1442, 1444, Figs. 5, 6, 8). Cross-referencing its earlier discussion of motivation to combine, Petitioner contends that the combination of Nowka and Borkar renders it obvious to expand Nowka’s variable power domain to multiple domains, for example, to Nowka’s speech accelerator. Pet. 24–27 (citing Ex. 1003 ¶¶ 70–72, Ex. 1004, 1445; Ex. 1006, 9:58–59, 10:30–11:39, Figs. 5, 7).

Patent Owner argues that Petitioner has not proven a motivation to combine or a reasonable expectation of success, as it pertains to Nowka and Borkar and a “plurality of power islands.” Prelim. Resp. 17–30.

As discussed in Section II.D.4 above, we determine that, although reasons to combine and a reasonable expectation of success remain as issues for trial, Petitioner’s contentions for claim element [1b] are sufficiently supported by the cited evidence and adequate for purposes of institution. Aside from motivation to combine and reasonable expectation of success, Patent Owner does not dispute Petitioner’s contentions for claim element [1b], which we find are sufficiently supported by the cited evidence and adequate for purposes of institution.

d) Claim Element [1c]

Claim element [1c] recites “one or more power consumption signals indicating one or more of the power consumptions.” Ex. 1001, 13:26–27.

Petitioner contends that the Nowka-Borkar combination renders obvious claim element [1c]. Pet. 27–32. Petitioner contends that Nowka recommends maintaining power consumption at or below a threshold and that Borkar teaches a mechanism for doing so. Pet. 28 (citing Ex. 1004, 1441; Ex. 1006, 13:2–8). Petitioner contends that Borkar’s current signals and temperature signals are both “power consumption signals,” as recited in claim element [1c]. Pet. 28–32 (citing Ex. 1006, 4:13–46, 4:58–60, 4:64–67, 6:48–53, 7:39–42, 13:2–11, Figs. 1–4, 7).

Patent Owner does not dispute Petitioner’s contentions for claim element [1c], which we find are sufficiently supported by the cited evidence and adequate for purposes of institution.

e) Claim Element [1d]

Claim element [1d] recites:

a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

Ex. 1001, 13:28–37.

Petitioner contends that the Nowka-Borkar combination renders obvious claim element [1d]. Pet. 33–40. Petitioner contends that Nowka’s “on-chip supervisor” is a power management processor, as recited in claim element [1d]. Pet. 33 (citing Ex. 1004, 1446). Petitioner contends that, in the Nowka-Borkar combination, the “on-chip supervisor” “would be coupled to each of Nowka’s variable power domains.” Pet. 34 (citing Ex. 1003 ¶ 81). Petitioner contends that Borkar’s “control circuitry” is a power management processor “and/or could be incorporated into Nowka’s ‘on-chip supervisor’ to form the power management processor.” Pet. 35 (citing Ex. 1004, 1446; Ex. 1006, 4:3–5, 4:20–33, 5:45–52, 11:22–27, 11:40–43, 11:55–58).

Cross-referencing its contentions for claim element [1c], Petitioner contends that Borkar’s control circuitry is “configured to monitor the one or more power consumption signals,” as recited in claim element [1d]. Pet. 37 (citing Ex. 1006, 4:58–60, 7:39–42, 4:12–46, 4:64–67, 6:48–53, 13:8–11; Figs. 1, 2, 4, 7). Cross-referencing its contentions for claim element [1b], Petitioner contends that Nowka’s on-chip supervisor and Borkar’s control

circuitry are “dedicated to execute the power management software to individually control each of the power consumptions,” as recited in claim element [1d]. Pet. 37–38 (citing Ex. 1004, 1442, 1446; Ex. 1006, 1:63–65; 4:3–5, 4:20–33, 4:64–67, 5:20–24, 5:45–52, 5:59–64, 6:1–7, 6:12–13, 6:26–53, 11:22–35, 11:41–67, Figs. 1–5, 7). Relying on disclosures in both Nowka and Borkar, Petitioner contends that the Nowka-Borkar combination renders obvious “the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request,” as recited in claim element [1d]. Pet. 38–40 (citing Ex. 1004, 1442, 1446; Ex. 1006, 4:64–67, 13:28–30).

Patent Owner does not dispute Petitioner’s contentions for claim element [1d], which we find are sufficiently supported by the cited evidence and adequate for purposes of institution.

f) Conclusion

For the reasons discussed above, we determine that Petitioner shows a reasonable likelihood of prevailing on its challenge to independent claims 1, 8, 16, 23, 31, 39, 48, and 56 based on Nowka and Borkar.

6. Dependent Claims 2–7, 9–15, 17–22, 24–30, 32–38, 40–47, 49–55, and 57–64

Claims 2–7 depend, directly or indirectly, from claim 1; claims 9–15 depend, directly or indirectly, from claim 8; claims 17–22 depend, directly or indirectly, from claim 16; claims 24–30 depend, directly or indirectly, from claim 23; claims 32–38 depend, directly or indirectly, from claim 31; claims 40–47 depend, directly or indirectly, from claim 39; claims 49–55 depend, directly or indirectly, from claim 48; and claims 57–64 depend, directly or indirectly, from claim 56.

Petitioner challenges the dependent claims based on Nowka and Borkar. Pet. 40–60. At this stage, Patent Owner does not present arguments for the dependent claims separate from its arguments for the independent claims. See Prelim. Resp. 11 (addressing “all claims” together). In view of our determination that Petitioner shows a reasonable likelihood of prevailing on its challenge to the independent claims and in the absence of any separate argument by Patent Owner addressing the dependent claims, we decline at this stage to provide an explicit analysis of Petitioner’s challenge to the dependent claims.

E. Petitioner’s Challenge based on Nicol and Borkar

Petitioner contends that claims 1–64 are unpatentable as obvious based on Nicol and Borkar. Pet. 60–96. Patent Owner opposes. Prelim. Resp. 30–43.

In view of our determination that Petitioner shows a reasonable likelihood of prevailing on its challenge to the independent claims based on Nowka and Borkar, we decline at this stage to provide an explicit analysis of Petitioner’s Nicol-led challenges.

IV. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–64 of the ’885 Patent is instituted commencing on the entry date of this Decision; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial.

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