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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/192,486	06/24/2016	Barry Alan Hoberman	01181-US-REI	6310

68256 7590 08/04/2021

Conversant Intellectual Property Management Corp
5830 Granite Parkway #100-247
Suite 247
Plano, TX 75024

EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
3992	

NOTIFICATION DATE	DELIVERY MODE
08/04/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipadmin@conversantip.com
mcleod@conversantip.com

INFINEON 1036
Infineon v. Mosaid
IPR2025-01171

Notice of Abandonment	Application No.	Applicant(s)
	15/192,486	Hoberman et al.
	Examiner	Art Unit
	Luke S Wassum	3992

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☑ Applicant's failure to timely file a proper reply to the Office letter mailed on 29 July 2020.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 to the final rejection. (A proper reply under 37 CFR 1.113 to a final rejection consists only of:(1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) if this is utility or plant application, a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. Note that RCEs are not permitted in design applications.)
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a *bona fide* attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 8 below).
   (d) ☑ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $ _____ is insufficient. A balance of $ _____ is due.
   The issue fee required by 37CFR 1.18 is $ _____ . The publication fee, if required by 37 CFR 1.18(d), is $ _____ .
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record or other party authorized under 37 CFR 1.33 (b). See 37 CFR 1.138(b).

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34) upon the filing of a continuing application.

6. ☐ The decision by the Patent Trial and Appeal Board rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The dismissal of the appeal in an application having no allowed claims. (When an appeal is dismissed in an application having no allowed claims the application stands abandoned. See MPEP 1215.04 subsections I-V for an explanation of the reasons why an appeal is dismissed.)

8. ☐ The reason(s) below:

_____

/LUKE S WASSUM/
Primary Examiner, Art Unit 3992

Petitions to revive under 37 CFR 1.137, or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15192486
Filing Date	2016-06-24
First Named Inventor	HOBERMAN
Art Unit	3992
Examiner Name	YIGDALL, Michael J.
Attorney Docket Number	01181-US-REI

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020055961	A1	2002-05-09	CHAUVEL et al.	
	2	20020029352	A1	2002-03-07	SHEKHAR et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN
	Art Unit	3992
	Examiner Name	YIGDALL, Michael J.
	Attorney Docket Number	01181-US-REI

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN
	Art Unit	3992
	Examiner Name	YIGDALL, Michael J.
	Attorney Docket Number	01181-US-REI

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Rodney M Anderson/	Date (YYYY-MM-DD)	2020-11-13
Name/Print	Rodney M. Anderson	Registration Number	31939

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/22 (03-13)
Approved for use through 3/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) 01181-US-REI
Application Number 15/192,486	Filed 06/24/2016
For POWER MANAGERS FOR AN INTEGRATED CIRCUIT	
Art Unit 3992	Examiner YIGDALL, Michael J.

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☑ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$ 200.00
☐ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 504154.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 31939.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Rodney M Anderson/	November 13, 2020
Signature	Date
Rodney M. Anderson	214-458-4544
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	15192486
Filing Date:	24-Jun-2016
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Filer:	Rodney Michael Anderson/Julie McLeod
Attorney Docket Number:	01181-US-REI
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	220	220
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**480**

Electronic Acknowledgement Receipt	
EFS ID:	41115584
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Rodney Michael Anderson/Julie McLeod
Filer Authorized By:	Rodney Michael Anderson
Attorney Docket Number:	01181-US-REI
Receipt Date:	13-NOV-2020
Filing Date:	24-JUN-2016
Time Stamp:	11:32:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$480
RAM confirmation Number	E2020ACB32326045
Deposit Account	504154
Authorized User	Julie McLeod
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges) 37 CFR 1.20 (Post Issuance fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.16 (National application filing, search, and examination fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2020_11_13_IDS_Submission_Response.pdf	66599 773cf1a9317460d19780ce399fe42da259ecefbc	no	2
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	IDS_Submission_Filed.pdf	1034322 ea759298b289433a1fe08b31630cab73c68b68dc	no	4
Warnings:					
Information:					
3	Extension of Time	2020_11_13_EOT.pdf	188370 a51934cddf374b749f801b73735c7c683d73085c	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32676 c0e968b3cb077761c2af1e612b80758c74d7802e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1321967		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	HOBERMAN, Barry A.
Serial No.:	15/192,486
Filing Date:	June 24, 2016
Group Art Unit:	3992
Examiner:	YIGDALL, Michael J.
Confirmation No.:	6310
Title:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

An Information Disclosure Statement for this application is submitted herewith, for consideration in this application.

Notification of a final rejection in this reissue application was made on July 29, 2020. However, as certified in this Information Disclosure Statement, each cited item of information was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.[1] Specifically, these two references were cited in a "Summons to attend oral proceedings pursuant to Rule 115(1) EPC" mailed on September 9, 2020 in a counterpart European patent application[2] to this application.

These two references were indicated by the European Patent Office in that Summons as disclosing relevant prior art and describing a plurality of features which are related to the subject-

[1] 37 C.F.R. §1.97(e)(1).
[2] European Application No. 17 208 696.9.

matter of the present claims and the application in general. Neither reference was applied in a finding of lack of novelty or lack of inventive step of the claims in that counterpart application.

The fee specified by 37 C.F.R. §1.17(p) for submitting this Information Disclosure Statement is being paid herewith. Given the certification under 37 C.F.R. §1.97(e)(1) and the payment of this fee, Applicant submits that this Information Disclosure Statement is timely submitted.[3]

The filing of this Information Disclosure Statement is not to be considered as an admission by Patentee that any particular item of information cited therein is, or is considered to be, material to the patentability of any claims in this case.[4]

Consideration of this information in the examination of this application is respectfully submitted.

Respectfully submitted,

/Rodney M Anderson/

Dated: November 13, 2020

Rodney M. Anderson
Reg. No. 31939

[3] 37 C.F.R. §1.97(d).
[4] 37 C.F.R. §1.97(h).

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN
	Art Unit	3992
	Examiner Name	YIGDALL, Michael J.
	Attorney Docket Number	01181-US-REI

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020055961	A1	2002-05-09	CHAUVEL et al.	
	2	20020029352	A1	2002-03-07	SHEKHAR et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN
	Art Unit	3992
	Examiner Name	YIGDALL, Michael J.
	Attorney Docket Number	01181-US-REI

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN
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	Attorney Docket Number	01181-US-REI

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

X That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

X The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Rodney M Anderson/	Date (YYYY-MM-DD)	2020-11-12
Name/Print	Rodney M. Anderson	Registration Number	31939

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15192486
Filing Date:	24-Jun-2016
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Filer:	Rodney Michael Anderson/Julie McLeod
Attorney Docket Number:	01181-US-REI

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	220	220
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**640**

Electronic Acknowledgement Receipt	
EFS ID:	41107203
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Rodney Michael Anderson/Julie McLeod
Filer Authorized By:	Rodney Michael Anderson
Attorney Docket Number:	01181-US-REI
Receipt Date:	12-NOV-2020
Filing Date:	24-JUN-2016
Time Stamp:	14:47:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Letter specifying the conditions for filing under 37CFR1.97	2020_11_12_IDS_Submission_Response.pdf	20750 0423f71496a1ccb67282aa200573b535a631649e	no	2

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	IDS_Submission_Filed.pdf	1034324 8a081bc43cb5a184e1eb980d6306ac49b48d3fc6	no	4
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	34175 e79094c3e76c31d65aaf0a6d8f83f43b97b6a4cf	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1089249	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	HOBERMAN, Barry A.
Serial No.:	15/192,486
Filing Date:	June 24, 2016
Group Art Unit:	3992
Examiner:	YIGDALL, Michael J.
Confirmation No.:	6310
Title:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

An Information Disclosure Statement for this application is submitted herewith, for consideration in this application.

Notification of a final rejection in this reissue application was made on July 29, 2020. However, as certified in this Information Disclosure Statement, each cited item of information was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.[1] Specifically, these two references were cited in a "Summons to attend oral proceedings pursuant to Rule 115(1) EPC" mailed on September 9, 2020 in a counterpart European patent application[2] to this application.

These two references were indicated by the European Patent Office in that Summons as disclosing relevant prior art and describing a plurality of features which are related to the subject-

[1] 37 C.F.R. §1.97(e)(1).
[2] European Application No. 17 208 696.9.

matter of the present claims and the application in general. Neither reference was applied in a finding of lack of novelty or lack of inventive step of the claims in that counterpart application.

The fee specified by 37 C.F.R. §1.17(p) for submitting this Information Disclosure Statement is being paid herewith. Given the certification under 37 C.F.R. §1.97(e)(1) and the payment of this fee, Applicant submits that this Information Disclosure Statement is timely submitted.[3]

The filing of this Information Disclosure Statement is not to be considered as an admission by Patentee that any particular item of information cited therein is, or is considered to be, material to the patentability of any claims in this case.[4]

Consideration of this information in the examination of this application is respectfully submitted.

Respectfully submitted,

/Rodney M Anderson/

Dated: November 12, 2020

Rodney M. Anderson
Reg. No. 31939

[3] 37 C.F.R. §1.97(d).
[4] 37 C.F.R. §1.97(h).

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/192,486	06/24/2016	Barry Alan Hoberman	01181-US-REI	6310

68256 7590 07/29/2020

Conversant Intellectual Property Management Corp
5830 Granite Parkway #100-247
Suite 247
Plano, TX 75024

EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
3992	

NOTIFICATION DATE	DELIVERY MODE
07/29/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipadmin@conversantip.com
mcleod@conversantip.com

Office Action Summary	Application No. 15/192,486	Applicant(s) Hoberman et al.	
	Examiner Michael J Yigdall	Art Unit 3992	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 16 June 2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 23-61 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 23-61 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

1. A response to the non-final Office action mailed on January 16, 2020 was filed on June 16, 2020. Claims 41 and 43-51 are amended. Claims 1-22 are canceled. Thus, claims 23-61 are pending, of which claims 23, 34, 40 and 52 are the independent claims.

Response to Amendment

2. The rejection of the claims under 35 U.S.C. § 251 as based on a defective reissue oath or declaration is withdrawn in light of the substitute statements filed on June 16, 2020.

3. The double patenting rejections of claims 1 and 13 are withdrawn in light of the applicant's amendment canceling these claims.

4. The objection to claim 13 is withdrawn in light of the applicant's amendment. However, an objection to the listing of claims filed on June 16, 2020 is set forth below.

5. The rejections of claims 1-22 under 35 U.S.C. § 112(b) or pre-AIA 35 U.S.C. § 112, second paragraph, are withdrawn in light of the applicant's amendment canceling these claims. Likewise, the rejection of claims 41-51 as indefinite for attempting to further limit claim 39 rather than claim 40 is withdrawn in light of the amendments to claims 41 and 43-51. However, the rejection of claim 50 as indefinite for lacking antecedent basis for "the power management software" is reiterated below.

6. The rejections of claims 1-22 under pre-AIA 35 U.S.C. § 103(a) are withdrawn in light of the applicant's amendment canceling these claims.

Response to Arguments

7. With respect to the double patenting rejections set forth in the non-final Office action, the applicant states, "Applicant defers determining whether the filing of a Terminal Disclaimer is appropriate until such time as one or more independent claims are indicated as allowable." See the applicant's remarks at pages 7-9. Accordingly, the double patenting rejections of claims 23, 34, 40 and 52 are reiterated below.

8. The applicant disagrees with the examiner's interpretation of the "first power manager" and "second power manager" of claims 23-33 and 40-51 as means-plus-function limitations under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, and contends that the term "power manager" such as recited in the claims "is a term that is well-known by persons of ordinary skill in the art of PMIC (power management integrated circuit) design to have a sufficiently definite structure." The applicant states, "Power managers essentially manage power consumption—that is, power managers are known to regulate clock frequency and voltage—of integrated circuits or power islands within ICs." The applicant notes that 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, does not apply "if persons of ordinary skill in the art reading the specification understand the term to have a sufficiently definite meaning as the name for the structure that performs the function, even when the term covers a broad class of structures or identifies the structures by their function." The applicant further argues that if the "power manager" elements are construed as circuitry, then "MPEP § 2181(I)(A) states that terms for circuitry that describe the function of the circuitry connote sufficient structure to persons of ordinary skill in the art." The applicant concludes that the "power manager" elements of the

claims "sufficiently connote definite structure and, therefore, do not invoke means-plus-function interpretation." See the applicant's remarks at pages 9-10.

The examiner respectfully disagrees with the applicant's conclusions. The examiner does not dispute that the term "PMIC" or "power management IC" or "power management integrated circuit" refers to a class of structures that performs power management functions. However, none of these terms is found in the specification of the '923 patent. The claims do not recite a first power management IC and a second power management IC, but instead recite "a first power manager" and "a second power manager." The specification of the '923 patent does not define the term "power manager" as a power management IC, but instead discloses a power manager 120 that "is any circuitry, device, or system configured to" perform functions disclosed in the specification. See the '923 patent at column 4, lines 18-58. FIG. 1 of the '923 patent illustrates the power manager 120 as a black box. Moreover, the scope of "any circuitry, device, or system" is not limited to circuitry, and includes, for example, "a central processing unit (CPU)" that executes software or firmware such as "power management control layer (PMCL) 218" and "power manager (PM) firmware 224." *Id.* at column 4, line 59 to column 5, line 47. Indeed, claims 30 and 48 recite that "the second power manager comprises firmware processable on the integrated circuit," and claims 31 and 49 recite that "the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit." Claims 33 and 51 recite that "the first power manager is located outside the integrated circuit," which means that in claims 23 and 40 the first power manger is something inside *or* outside the claimed integrated circuit.

The examiner respectfully submits that the term "power manager" therefore does not connote sufficiently definite structure. Accordingly, the examiner's interpretation of the "first

power manager" and the "second power manager" under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, and the rejection of claims 23-33 and 40-51 under 35 U.S.C. § 112(b) or pre-AIA 35 U.S.C. § 112, second paragraph, are reiterated below.

9. The applicant's argument that "waiting for the source voltage ... to settle down" is not indefinite because "a person of ordinary skill in the art would know voltage 'settling down' to mean the voltage level is stabilizing" is moot in light of the applicant's amendment canceling claims 1 and 13. See the applicant's remarks at page 10.

10. With respect to the obviousness rejections, the applicant argues that Inoue and Bednar do not teach or suggest "a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit" such as claimed. Specifically, the applicant contends that Inoue merely discloses that the data processing circuit 14 and data output unit 11 "manages power based on the state of the CPU," and argues:

> While the state information may [be] based on the needs (i.e. an application that is to be run or instructions to be processed), there is no mention of the state being based on operation of the CPU such as temperature. Consequently, Inoue does not teach or suggest "a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit."

The applicant contends that Bednar and the other references "fail to remedy the deficiencies of Inoue." See the applicant's remarks at pages 10-12.

The examiner agrees that Inoue teaches or suggests managing power consumption based on "needs." However, the examiner respectfully disagrees that Inoue does not teach or suggest managing power consumption based on "needs and operation."

First, the examiner points out that the claims do not specify what constitutes "needs and operation" of the integrated circuit. The claims recite "an integrated circuit to effect power

consumptions in operation" or "an integrated circuit that effects power consumptions in operation," which Inoue discloses in terms of an integrated circuit that consumes power in operation. See Inoue at FIG. 1, column 2, lines 24-43 and column 6, lines 26-33. Inoue further discloses managing power consumption of the integrated circuit based on "internal state" or "the state of the CPU." *Id.* at column 6, line 63 to column 7, line 19. Further to the "needs" of the integrated circuit, the examiner submits that the state of the integrated circuit reflects "operation" of the integrated circuit at least because the integrated circuit is "in operation" when it consumes power. For example, Inoue discloses that "[a]s examples of the system state, there can be defined, e.g., a high-speed processing state, a low-speed processing state, and the like." *Id.* at column 8, lines 6-8. In other words, the "system state" represents a state of operation. Thus, where Inoue discloses managing power consumption based on the state of the integrated circuit, the teachings of Inoue would have suggested managing power consumption "based on needs and operation of the integrated circuit" to those of ordinary skill in the art.

Second, even if managing power consumption "based on ... operation of the integrated circuit" were construed to mean managing power consumption based on temperature, the examiner notes that, as cited in the Office action with respect to claims 40 and 52, Silvester discloses managing power consumption based on an "operating condition" such as temperature. See Silvester at column 3, lines 16-60. Thus, the combined teachings of the references would have suggested such a construction to those of ordinary skill in the art.

Claim Interpretation

11. The following is a quotation of 35 U.S.C. § 112(f):

> (f) ELEMENT IN CLAIM FOR A COMBINATION. — An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and

> such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.
>
> The following is a quotation of pre-AIA 35 U.S.C. § 112, sixth paragraph:
>
> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

12. Claims 23-33 and 40-51 include elements that are interpreted under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, because the elements recite non-structural substitutes for the term "means" together with functional language, without reciting sufficient structure for performing the claimed functions. See MPEP § 2181(I). Accordingly, these limitations are interpreted to cover the corresponding structure disclosed in the specification for performing the claimed functions, and equivalents thereof. See MPEP § 2173.01(II). The elements interpreted under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, include the "first power manager" and the "second power manager" recited in independent claims 23 and 40.

However, the specification of the '923 patent does not sufficiently disclose the structure for performing the functions of the claimed "first power manager" and "second power manager," or at least does not sufficiently link the disclosed structure to each of the claimed functions. See MPEP § 2181(III). See the rejection under 35 U.S.C. § 112(b) or pre-AIA 35 U.S.C. § 112, second paragraph, set forth below.

Double Patenting

13. The non-statutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

harassment by multiple assignees. A non-statutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (C.C.P.A. 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (C.C.P.A. 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (C.C.P.A. 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on non-statutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the "first inventor to file" provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) to 706.02(l)(3) for applications not subject to those provisions. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms that may be used. Please visit http://www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25 or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

14. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-74 of U.S. Patent No. 7,996,811 in view of U.S. Patent No. 6,968,467 to Inoue et al. ("Inoue") and U.S. Patent No. 6,820,240 to Bednar et al. ("Bednar"). Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 16, 23, 29, 44, 60 and 74 of U.S. Patent No. 7,996,811 in view of Inoue.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-74 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34. To the extent that the reference claims recite "a power manager" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 16, 23, 29, 44, 60 and 74 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52. Where claims 40 and 52 recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded," the reference claims likewise recite that the power manager monitors the power consumptions of the plurality of power islands "using temperature ... measurement." To the extent that the reference claims recite "a power manager" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

15. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-73 of U.S. Patent No. 8,782,590 in view of Inoue and Bednar. Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 4, 6, 12, 14, 19, 21, 26, 28, 33, 35, 40, 42, 47, 49, 54 and 56 of U.S. Patent No. 8,782,590 in view of Inoue.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-73 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34. To the extent that the reference claims recite "a power manager" or "a power management processor" that controls the power consumptions of

the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 4, 6, 12, 14, 19, 21, 26, 28, 33, 35, 40, 42, 47, 49, 54 and 56 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52. Where claims 40 and 52 recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded," the reference claims likewise recite that the power manager or power management processor monitors power consumption signals of the plurality of power islands, including "temperature measurement" signals. To the extent that the reference claims recite "a power manager" or "a power management processor" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those

of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

16. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-15 of U.S. Patent No. 9,166,412 in view of Bednar. Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-15 of U.S. Patent No. 9,166,412 in view of U.S. Patent No. 7,085,945 to Silvester ("Silvester").

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-15 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34.

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 1-15 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52.

The reference claims do not recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded" such as claimed. However, as Silvester suggests, monitoring temperature and managing the power consumption of a power island when a temperature threshold is exceeded would have been obvious to those of ordinary skill in the art so as to lower the temperature and prevent failure of the power island (see, e.g., column 1, lines 22-34 and column 3, lines 16-60).

17. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-16 of U.S. Patent No. 9,660,616 in view of Bednar. Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 4 and 12 of U.S. Patent No. 9,660,616.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-16 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34.

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 4 and 12 of the reference patent. The limitations of the reference

claims are analogous to those of claims 40 and 52. Where claims 40 and 52 recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded," the reference claims likewise recite that the first power manager monitors one or more power consumption signals of the plurality of power islands "wherein the one or more power consumption signals include temperature or power dissipation measurement."

18. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of U.S. Patent No. 10,243,542 in view of Bednar. Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of U.S. Patent No. 10,243,542 in view of Silvester.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-5 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34.

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 1-5 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52.

The reference claims do not recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded" such as claimed. However, as Silvester suggests, monitoring temperature and managing the power consumption of a power island when a temperature threshold is exceeded would have been obvious to those of ordinary skill in the art so as to lower the temperature and prevent failure of the power island (see, e.g., column 1, lines 22-34 and column 3, lines 16-60).

19. Claims 23 and 34 are provisionally rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of U.S. Application No. 16/226,917 in view of Bednar. Claims 40 and 52 are provisionally rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of U.S. Application No. 16/226,917 in view of Silvester.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-5 of the reference application. The limitations of the reference claims are analogous to those of claims 23 and 34.

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 1-5 of the reference application. The limitations of the reference claims are analogous to those of claims 40 and 52.

The reference claims do not recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded" such as claimed. However, as Silvester suggests, monitoring temperature and managing the power consumption of a power island when a temperature threshold is exceeded would have been obvious to those of ordinary skill in the art so as to lower the temperature and prevent failure of the power island (see, e.g., column 1, lines 22-34 and column 3, lines 16-60).

Objections to the Claims

20. The listing of claims filed on June 16, 2020 is objected to because claims 1-39, rather than only claims 1-22, are listed as canceled.

Rejections under 35 U.S.C. § 112

21. The following is a quotation of 35 U.S.C. § 112(b):

> (b) CONCLUSION. — The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.
>
> The following is a quotation of pre-AIA 35 U.S.C. § 112, second paragraph:
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

22. Claims 23-33 and 40-51 are rejected under 35 U.S.C. § 112(b) or pre-AIA 35 U.S.C. § 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention.

With respect to claims 23-33 and 40-51, the claims include one or more elements that are interpreted under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, as set forth above. However, the specification of the '923 patent does not sufficiently disclose the structure for performing the claimed functions, or at least does not sufficiently link the disclosed structure to each of the claimed functions. Thus, the claims are indefinite.

Claims 23 and 40 recite a "first power manager" configured to "manage the first power consumption based on needs and operation of the integrated circuit." Claim 40 further recites that the first power manager is configured to "determine power trade-offs between the power islands" and "monitors the plurality of power islands if a temperature threshold has been exceeded." With respect to a "power manager" such as claimed, the specification discloses a power manager 120 and "examples of the power manager 120," including "the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM)." However, the power manager 120 is disclosed in terms of its function rather than its structure. The specification discloses that the power manager "is any circuitry, device, or system configured to" perform the functions of the power manager. See the '923 patent at column 4, lines 18-58. Likewise, FIG. 1 of the '923 patent illustrates the power manager 120 as a black box. If the claimed "first power manager" is the master power manager, the specification further discloses that the MPM 280 "is any circuitry configured to control the 'global' power behavior of the entire integrated circuit 250." *Id.* at column 5, lines 48-58. However, the structure that actually performs the functions of the MPM 280 is not apparent.

The specification further discloses an embedded firmware stack 210, which "includes software layers that run on a central processing unit (CPU)," including "a power management control layer (PMCL) 218" and "a global power application layer (GPAL) 214." The embedded

firmware stack 210 includes "power manager (PM) firmware 224 for the MPM, IPM and/or SPM," which "is firmware executed by the master power manager 280, the intermediate power manager, and the slave power managers 264 and 274." *Id.* at column 4, line 59 to column 5, line 47. If the claimed "first power manager" is a CPU or processor that executes firmware to perform the claimed functions, then the corresponding structure must include an algorithm for each of the functions. See MPEP § 2181(II)(B). However, the algorithms for performing the claimed functions are not apparent.

Claims 23 and 40 recite a "second power manager" configured to "communicate with the first power manager" and "respond to a request to manage the second power consumption for the first power island." Claim 23 further recites that the second power manager responds by "stopping a clock of the first power island" and "saving a state of the first power island," and then "powering off the first power island." Claim 40 further recites that the second power manager responds by "changing a source voltage" and "changing a clock frequency of the first power island." As noted above, the specification discloses the power manager 120 in terms of its function rather than its structure. If the claimed "second power manager" is the slave power manager, the specification further discloses that the SPM 264 "is any circuitry configured to control power within a power island [260] in the integrated circuit 250," and states, "The description for the SPM 264 also applies to the SPM 274 for the power island 270." See the '923 patent at column 6, lines 11-40. However, the structure that actually performs the functions of the SPM 264 or 274 is not apparent. Likewise, if the claimed "second power manager" is a CPU or processor that executes firmware to perform the functions, the algorithms for performing each of the claimed functions are not apparent.

The applicant may (1) amend the claims so that these limitations are no longer interpreted as limitations under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, (2) amend the specification to expressly recite what structure performs each of the claimed functions, without adding new matter, or (3) amend the specification such that the disclosed structure is clearly linked to each of the claimed functions, without adding new matter. If the applicant is of the opinion that the specification already implicitly or inherently discloses the corresponding structure and clearly links the disclosed structure to each of the claimed functions, then the applicant should (1) amend the specification to expressly recite the corresponding structure and clearly link the disclosed structure to each of the claimed functions, without adding new matter, or (2) state on the record what corresponding structure implicitly or inherently set forth in the specification performs each of the claimed functions.

With respect to claim 50, the claim as amended is directed to "[t]he system of claim 40," and recites the limitation "wherein the power management software is embedded firmware in the integrated circuit." However, there is insufficient antecedent basis in the claim for "the power management software" since the term "power management software" is introduced in claim 49 rather than in claim 40.

Rejections under 35 U.S.C. § 103

23. The following is a quotation of pre-AIA 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 23-32 and 34-39 are rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,968,467 to Inoue et al. ("Inoue") in view of U.S. Patent No. 6,820,240 to Bednar et al. ("Bednar").

Claim 23

Inoue teaches or suggests a system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation);

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20);

a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1) configured to manage the first power consumption based on needs and the operation of the integrated circuit (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit); and

a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1) configured to:

a) communicate with the first power manager (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus); and

b) respond to a request to manage the second power consumption for the first power island (see, e.g., column 8, lines 12-19, describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block, including stopping the clock supply (see, e.g., column 10, lines 4-30). Inoue does not expressly disclose saving a state of the block, and therefore does not expressly disclose responding to the request by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

However, in an analogous art, Bednar teaches a system-on-a-chip comprising a plurality of voltage islands and state-saving latches 125 for saving state when a voltage island 120 is powered off (see, e.g., FIG. 1 and column 3, lines 22-46). Bednar discloses saving state in the latches before powering off the island, "eliminating the need to transfer logic states off-island and back in order to save and restore necessary logic states" (see, e.g., column 4, lines 30-53).

A person of ordinary skill in the art could have combined the teachings of Inoue and Bednar with predictable results, and would have been prompted to implement the second power manager of Inoue so as to save the state of the block before powering off the block. As Bednar suggests, "some subset of the logic state, prior to power-down, may need to be preserved to resume operation" when power is restored to the block, and the teachings of Bednar allow for saving state and resuming operation "quickly" when power is restored (see, e.g., Bednar at

column 4, lines 30-53). Thus, the combined teachings of Inoue and Bednar would have suggested responding to the request by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

Accordingly, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 24

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the second power manager is further configured to carry out the saving of the state of the first power island after the stopping (see, e.g., Bednar at column 4, lines 30-53).

Claim 25

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the first power manager is further configured to communicate the request to the second power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 26

Inoue in view of Bednar further teaches or suggests the system of claim 23 further comprising a buffer for storing the state that is saved (see, e.g., Bednar at FIG. 1 and column 4, lines 30-53, describing that the state-saving latches 125 are a buffer).

Claim 27

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the second power manager is further configured to respond to another request, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock of the first power island

(see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing powering on and starting the clock supply, and Bednar at column 4, lines 30-53, describing restoring the state of the island after powering on the island).

Claim 28

Inoue in view of Bednar further teaches or suggests the system of claim 27 further comprising a buffer for storing the state that is saved, and the buffer being accessible during the restoring (see, e.g., Bednar at FIG. 1 and column 4, lines 30-53, describing that the state-saving latches 125 are a buffer that is accessed during the restoring).

Claim 29

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Claim 30

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the second power manager comprises firmware processable on the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager is programmed).

Claim 31

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager comprises a processor and programming).

Claim 32

Inoue in view of Bednar further teaches or suggests the system of claim 31 wherein the power management software is embedded firmware in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65).

Claim 34

Inoue teaches or suggests a method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation), and the method comprising:

in a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1), managing a first power consumption based on needs and operation of the integrated circuit (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit);

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20, and see, e.g., column 10, lines 4-30, further describing supplying a clock to the block);

in a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1), communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus, and column 8, lines 12-19, further describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block, including stopping the clock supply (see, e.g., column 10, lines 4-30). Inoue does not expressly disclose saving a state of the block, and therefore does not expressly disclose responding to the request by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

However, in an analogous art, Bednar teaches a system-on-a-chip comprising a plurality of voltage islands and state-saving latches 125 for saving state when a voltage island 120 is powered off (see, e.g., FIG. 1 and column 3, lines 22-46). Bednar discloses saving state in the latches before powering off the island, "eliminating the need to transfer logic states off-island and back in order to save and restore necessary logic states" (see, e.g., column 4, lines 30-53).

A person of ordinary skill in the art could have combined the teachings of Inoue and Bednar with predictable results, and would have been prompted to implement the second power manager of Inoue so as to save the state of the block before powering off the block. As Bednar suggests, "some subset of the logic state, prior to power-down, may need to be preserved to resume operation" when power is restored to the block, and the teachings of Bednar allow for saving state and resuming operation "quickly" when power is restored (see, e.g., Bednar at column 4, lines 30-53). Thus, the combined teachings of Inoue and Bednar would have suggested responding to the request by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

Accordingly, a method such as claimed would have been obvious to those of ordinary skill in the art.

Claim 35

Inoue in view of Bednar further teaches or suggests the method of claim 34 wherein the saving of the state of the first power island is carried out after the stopping (see, e.g., Bednar at column 4, lines 30-53).

Claim 36

Inoue in view of Bednar further teaches or suggests the method of claim 34 wherein the request is communicated to the second power manager by the first power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 37

Inoue in view of Bednar further teaches or suggests the method of claim 34 wherein the state that is saved is stored in a buffer (see, e.g., Bednar at FIG. 1 and column 4, lines 30-53, describing that the state-saving latches 125 are a buffer).

Claim 38

Inoue in view of Bednar further teaches or suggests the method of claim 34 further comprising responding to another request that is received by the second power manager, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock

(see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing powering on and starting the clock supply, and Bednar at column 4, lines 30-53, describing restoring the state of the island after powering on the island).

Claim 39

Inoue in view of Bednar further teaches or suggests the method of claim 38 wherein the state that is saved is stored in a buffer accessed during the restoring (see, e.g., Bednar at FIG. 1

and column 4, lines 30-53, describing that the state-saving latches 125 are a buffer that is accessed during the restoring).

25. Claim 33 is rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of Bednar and further in view of U.S. Patent No. 7,085,945 to Silvester ("Silvester").

Claim 33

Inoue in view of Bednar teaches or suggests the system of claim 23, but does not expressly disclose the limitation wherein the first power manager is located outside the integrated circuit.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue such that the first power manager is located outside the integrated circuit with predictable results and with no change in function. For example, in an analogous art, Silvester teaches a controller 305/310 for managing the power consumption of functional unit blocks within an integrated circuit (see, e.g., column 4, line 45 to column 5, line 12). Silvester expressly discloses an embodiment where the controller 305 is inside the integrated circuit or on the same die as the functional unit blocks (see, e.g., FIG. 3A), and an embodiment where the controller 310 is outside the integrated circuit or on a different die (see, e.g., FIG. 3B). Thus, a system such as claimed would have been obvious to those of ordinary skill in the art.

26. Claims 40-45, 47-57 and 59-61 are rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of Silvester and U.S. Patent No. 6,141,762 to Nicol et al. ("Nicol").

Claim 40

Inoue teaches or suggests a system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation);

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20);

a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1) configured to:

a) manage the first power consumption based on needs and operation of the integrated circuit (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit);

b) determine power trade-offs between the power islands (see, e.g., column 11, lines 12-17 and 41-55, describing that the first power manager determines which blocks to control).

Inoue does not expressly disclose that the first power manager is configured to:

c) monitors the plurality of power islands if a temperature threshold has been exceeded.

However, in an analogous art, Silvester teaches managing the power consumption of functional unit blocks within an integrated circuit, including monitoring whether a temperature

threshold is exceeded (see, e.g., column 3, lines 16-60). The functional unit blocks represent power islands within the integrated circuit. The teachings of Silvester allow for managing the temperature of a functional unit block to prevent failure (see, e.g., column 1, lines 22-34 and column 3, lines 50-60).

A person of ordinary skill in the art could have combined the teachings of Inoue and Silvester with predictable results, and would have been prompted to implement the first power manager of Inoue so as to monitor the plurality of power islands if a temperature threshold has been exceeded. As Silvester suggests, such an implementation would allow for managing the temperature of a power island to prevent failure.

Inoue further teaches or suggests:

a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1) configured to:

a) communicate with the first power manager (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus); and

b) respond to a request to manage the second power consumption for the first power island (see, e.g., column 8, lines 12-19, describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block (see, e.g., column 10, lines 4-30). To the extent that Inoue discloses changing the clock supply to "on" or "off" rather than changing the clock frequency, Inoue does not expressly disclose responding to the request by:

i) changing a source voltage; and

ii) changing a clock frequency of the first power island.

However, in an analogous art, Nicol teaches managing the power consumption of processing elements within an integrated circuit, including changing the supply voltage and the clock frequency for each of the processing elements (see, e.g., FIG. 2, FIG. 4, column 2, lines 18-31 and column 5, line 66 to column 6, line 13). The processing elements represent power islands within the integrated circuit. Nicol discloses increasing the supply voltage, for example, and then after the new supply voltage is stable, increasing the clock frequency (see, e.g., FIG. 3, column 4, line 38 to column 5, line 2 and column 5, lines 30-41). The teachings of Nicol allow for power management with "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit (see, e.g., column 2, lines 18-31).

A person of ordinary skill in the art could have combined the teachings of Inoue and Nicol with predictable results, and would have been prompted to implement the second power manager of Inoue so as to change both the supply voltage and the clock frequency of the block. As Nicol suggests, such an implementation would allow for "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit. Thus, the combined teachings of Inoue and Nicol would have suggested responding to the request by:

i) changing a source voltage; and

ii) changing a clock frequency of the first power island.

Accordingly, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 41

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 40, wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency (see,

e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing increasing the supply voltage and the clock supply, and Nicol at column 5, lines 30-41, further describing increasing the supply voltage ahead of increasing the clock frequency).

Claim 42

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 41, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 43

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 40, wherein the first power manager is further configured to communicate the request to the second power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 44

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 40, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10,

lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 45

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 40, wherein the source voltage of the first power island is controlled by a smart power unit (see, e.g., Inoue at column 7, lines 31-44 and column 10, lines 4-30, describing that the block controls the supply voltage and the clock supply).

Claim 47

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 40, wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Claim 48

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 40, wherein the second power manager comprises firmware processable on the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager is programmed).

Claim 49

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 40, wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager comprises a processor and programming).

Claim 50

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [49], wherein the power management software is embedded firmware in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65).

Claim 51

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 40, wherein the first power manager is located outside the integrated circuit.

Namely, a person of ordinary skill in the art could have implemented the teachings of Inoue such that the first power manager is located outside the integrated circuit with predictable results and with no change in function. For example, Silvester teaches a controller 305/310 for managing the power consumption of the functional unit blocks within the integrated circuit (see, e.g., column 4, line 45 to column 5, line 12). Silvester expressly discloses an embodiment where the controller 305 is inside the integrated circuit or on the same die as the functional unit blocks (see, e.g., FIG. 3A), and an embodiment where the controller 310 is outside the integrated circuit or on a different die (see, e.g., FIG. 3B). Thus, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 52

Inoue teaches or suggests a method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation), and the method comprising:

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20, and see, e.g., column 10, lines 4-30, further describing supplying a clock to the block);

in a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1), managing the first power consumption based on needs and operation of the integrated circuit, and determining power-trade-offs between the power islands (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Inoue does not expressly disclose that the first power manager monitors the plurality of power islands if a temperature threshold has been exceeded.

However, in an analogous art, Silvester teaches managing the power consumption of functional unit blocks within an integrated circuit, including monitoring whether a temperature

threshold is exceeded (see, e.g., column 3, lines 16-60). The functional unit blocks represent power islands within the integrated circuit. The teachings of Silvester allow for managing the temperature of a functional unit block to prevent failure (see, e.g., column 1, lines 22-34 and column 3, lines 50-60).

A person of ordinary skill in the art could have combined the teachings of Inoue and Silvester with predictable results, and would have been prompted to implement the first power manager of Inoue so as to monitor the plurality of power islands if a temperature threshold has been exceeded. As Silvester suggests, such an implementation would allow for managing the temperature of a power island to prevent failure.

Inoue further teaches or suggests:

in a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1), communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus, and column 8, lines 12-19, further describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block (see, e.g., column 10, lines 4-30). To the extent that Inoue discloses changing the clock supply to "on" or "off" rather than changing the clock frequency, Inoue does not expressly disclose responding to the request by:

changing a source voltage; and

changing a clock frequency of the clock of the first power island.

However, in an analogous art, Nicol teaches managing the power consumption of processing elements within an integrated circuit, including changing the supply voltage and the clock frequency for each of the processing elements (see, e.g., FIG. 2, FIG. 4, column 2, lines 18-31 and column 5, line 66 to column 6, line 13). The processing elements represent power islands within the integrated circuit. Nicol discloses increasing the supply voltage, for example, and then after the new supply voltage is stable, increasing the clock frequency (see, e.g., FIG. 3, column 4, line 38 to column 5, line 2 and column 5, lines 30-41). The teachings of Nicol allow for power management with "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit (see, e.g., column 2, lines 18-31).

A person of ordinary skill in the art could have combined the teachings of Inoue and Nicol with predictable results, and would have been prompted to implement the second power manager of Inoue so as to change both the supply voltage and the clock frequency of the block. As Nicol suggests, such an implementation would allow for "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit. Thus, the combined teachings of Inoue and Nicol would have suggested responding to the request by:

changing a source voltage; and

changing a clock frequency of the clock of the first power island.

Accordingly, a method such as claimed would have been obvious to those of ordinary skill in the art.

Claim 53

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30,

describing increasing the supply voltage and the clock supply, and Nicol at column 5, lines 30-41, further describing increasing the supply voltage ahead of increasing the clock frequency).

Claim 54

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 53, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 55

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, wherein the request is communicated to the second power manager by the first power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 56

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response

to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 57

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, wherein the source voltage of the first power island is controlled by a smart power unit (see, e.g., Inoue at column 7, lines 31-44 and column 10, lines 4-30, describing that the block controls the supply voltage and the clock supply).

Claim 59

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Claim 60

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, further comprising, in a third power manager (see, e.g., Inoue at column 7, lines 27-30, and power management unit 32 and power control unit 33 of block 30 in FIG. 1):

i) managing a third power consumption of the power consumptions, and the plurality of power islands including a second power island having an associated power consumption that is the third power consumption (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit,

including a second power island with a third power consumption in block 30, and see, e.g., column 6, line 63 to column 7, line 19, describing that the third power manager manages the power consumption of the block); and

ii) communicating with the first power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19, describing that the third power manager communicates with the first power manager).

Claim 61

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 60, wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62).

27. Claims 46 and 58 are rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of Silvester and Nicol and further in view of U.S. Patent No. 6,895,520 to Altmejd et al. ("Altmejd").

Claim 46

Inoue in view of Silvester and Nicol teaches or suggests the system of claim 40, but does not expressly disclose the limitation wherein the source voltage of the first power island is provided by an external regulator.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue such that the source voltage of the first power island is provided by an external regulator with predictable results and with no change in function. For example, in an analogous art, Altmejd teaches managing the power consumption of functional blocks within an integrated

circuit (see, e.g., column 1, line 62 to column 2, line 6). Altmejd expressly discloses a regulated supply voltage that is "supplied externally by a voltage regulator" such as known in the art (see, e.g., column 5, lines 27-29). Thus, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 58

Inoue in view of Silvester and Nicol teaches or suggests the method of claim 52, but does not expressly disclose providing external regulation for the source voltage of the first power island.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue so as to provide external regulation for the source voltage of the first power island with predictable results and with no change in function. For example, in an analogous art, Altmejd teaches managing the power consumption of functional blocks within an integrated circuit (see, e.g., column 1, line 62 to column 2, line 6). Altmejd expressly discloses a regulated supply voltage that is "supplied externally by a voltage regulator" such as known in the art (see, e.g., column 5, lines 27-29). Thus, a method such as claimed would have been obvious to those of ordinary skill in the art.

Conclusion

28. THIS ACTION IS MADE FINAL. The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall, whose telephone number is 571-272-3707. If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Hetul Patel, is reachable at 571-272-4184. The fax phone number for the organization where this application or proceeding is assigned is 571-273-9900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL J. YIGDALL/
Primary Examiner, Art Unit 3992

Conferees:

/LUKE S WASSUM/
Primary Examiner, Art Unit 3992

/H.B.P/
Supervisory Patent Examiner, Art Unit 3992

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/192,486	Hoberman et al.
	Examiner	Art Unit
	Michael J Yigdall	3992

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/10/2019	07/15/2020							
	1	✓	-							
	2	✓	-							
	3	✓	-							
	4	✓	-							
	5	✓	-							
	6	✓	-							
	7	✓	-							
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	36	✓	✓							
	37	✓	✓							
	38	✓	✓							
	39	✓	✓							
	40	✓	✓							
	41	✓	✓							
	42	✓	✓							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/192,486	Hoberman et al.
	Examiner	**Art Unit**
	Michael J Yigdall	3992

CLAIM		DATE								
Final	Original	12/10/2019	07/15/2020							
	43	✓	✓							
	44	✓	✓							
	45	✓	✓							
	46	✓	✓							
	47	✓	✓							
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	HOBERMAN, Barry A.
Serial No.:	15/192,486
Filing Date:	June 24, 2016
Group Art Unit:	3992
Examiner:	YIGDALL, Michael J.
Confirmation No.:	6310
Title:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Mail Stop - AMENDMENT
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

RESPONSE AND REMARKS

In response to the Office Action dated January 16, 2020, Applicants respectfully request that the Examiner reconsider the rejection of the claims in view of the following [amendments and] remarks. Please amend the Application as follows:

[Listing of / Amendments to] the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

Amendments to Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-39. (Canceled)

23. (Original) A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

24. (Original) The system of claim 23 wherein the second power manager is further configured to carry out the saving of the state of the first power island after the stopping.

25. (Original) The system of claim 23 wherein the first power manager is further configured to communicate the request to the second power manager.

26. (Original) The system of claim 23 further comprising a buffer for storing the state that is saved.

27. (Original) The system of claim 23 wherein the second power manager is further configured to respond to another request, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock of the first power island.

28. (Original) The system of claim 27 further comprising a buffer for storing the state that is saved, and the buffer being accessible during the restoring.

29. (Original) The system of claim 23 wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

30. (Original) The system of claim 23 wherein the second power manager comprises firmware processable on the integrated circuit.

31. (Original) The system of claim 23 wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

32. (Original) The system of claim 31 wherein the power management software is embedded firmware in the integrated circuit.

33. (Original) The system of claim 23 wherein the first power manager is located outside the integrated circuit.

34. (Original) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

in a first power manager, managing a first power consumption based on needs and operation of the integrated circuit;

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

35. (Original) The method of claim 34 wherein the saving of the state of the first power island is carried out after the stopping.

36. (Original) The method of claim 34 wherein the request is communicated to the second power manager by the first power manager.

37. (Original) The method of claim 34 wherein the state that is saved is stored in a buffer.

38. (Original) The method of claim 34 further comprising responding to another request that is received by the second power manager, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and
iii) after the restoring, starting the clock.

39. (Original) The method of claim 38 wherein the state that is saved is stored in a buffer accessed during the restoring.

40. (New) A system comprising:
an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;
a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;
a first power manager configured to:
a) manage the first power consumption based on needs and operation of the integrated circuit;
b) determine power trade-offs between the power islands;
c) monitors the plurality of power islands if a temperature threshold has been exceeded; and

a second power manager configured to:
a) communicate with the first power manager; and
b) respond to a request to manage the second power consumption for the first power island by:
i) changing a source voltage; and
ii) changing a clock frequency of the first power island.

41. (New-Amended) The system of claim 40, wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency.

42. (New) The system of claim 41, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

43. (New-Amended) The system of claim 40, wherein the first power manager is further configured to communicate the request to the second power manager.

44. (New-Amended) The system of claim 40, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

45. (New-Amended) The system of claim 40, wherein the source voltage of the first power island is controlled by a smart power unit.

46. (New-Amended) The system of claim 40, wherein the source voltage of the first power island is provided by an external regulator.

47. (New-Amended) The system of claim 40, wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

48. (New-Amended) The system of claim 40, wherein the second power manager comprises firmware processable on the integrated circuit.

49. (New-Amended) The system of claim 40, wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

50. (New-Amended) The system of claim 40, wherein the power management software is embedded firmware in the integrated circuit.

51. (New-Amended) The system of claim 40, wherein the first power manager is located outside the integrated circuit.

52. (New) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

in a first power manager, managing the first power consumption based on needs and operation of the integrated circuit, determining power-trade-offs between the power islands, and monitors the plurality of power islands if a temperature threshold has been exceeded; and

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

changing a source voltage; and

changing a clock frequency of the clock of the first power island.

53. (New) The method of claim 52, wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency.

54. (New) The method of claim 53, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

55. (New) The method of claim 52, wherein the request is communicated to the second power manager by the first power manager.

56. (New) The method of claim 52, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

57. (New) The method of claim 52, wherein the source voltage of the first power island is controlled by a smart power unit.

58. (New) The method of claim 52, further comprising providing external regulation for the source voltage of the first power island.

59. (New) The method of claim 52, wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island.

60. (New) The method of claim 52, further comprising, in a third power manager:
i) managing a third power consumption of the power consumptions, and the plurality of power islands including a second power island having an associated power consumption that is the third power consumption; and
ii) communicating with the first power manager.

61. (New) The method of claim 60, wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers.

62 - 78. (Cancelled)

REMARKS

Applicant replies within 5 months to the Office Action dated January 16, 2020.

Claims 41 and 43-51 are hereby amended.

Reconsideration of the claims is respectfully requested. The Applicant makes the aforementioned amendments and subsequent arguments to place this application in condition for allowance. Alternatively, the Applicant makes these amendments and offers these arguments to properly frame the issues for appeal. In this Response, the Applicant makes no admission concerning any now moot rejection or objection, and affirmatively denies any position, statement or averment of the Examiner that is not specifically addressed herein.

Claim Objections

Claim 13 is canceled. As such, the objection to Claim 13 is now moot.

Double Patenting

The Examiner rejects the Claims 1-13 on the ground of nonstatutory double patenting as being unpatentable as follows:

Claims Rejected	US Patent/Publication
Claims 1-13	Claims 1-74 of U.S. Patent No. 7,996,811 in view of U.S. Patent No. 6,968,467 ("Inoue et al.")
Claims 23 and 34	Claims 1-74 of U.S. Patent No. 7,996,811 in view of U.S. Patent No. 6,968,467 ("Inoue et al.") and U.S. Patent No. 6,820,240 ("Bednar et al.")
Claims 40 and 52	Claims 16, 23, 29, 44, 60 and 74 of U.S. Patent No. 7,996,811 in view of U.S. Patent No. 6,968,467 ("Inoue et al.")

Claims 1 and 13	Claims 1-73 of U.S. Patent No. 8,782,590 in view of U.S. Patent No. 6,968,467 ("Inoue et al.") and U.S. Patent No. 6,820,240 ("Bednar et al.")
Claims 40 and 52	Claims 4, 6, 12, 14, 19, 21, 26, 28, 33, 35, 40, 42, 47, 49, 54 and 56 of U.S. Patent No. 8,782,590 in view of U.S. Patent No. 6,968,467 ("Inoue et al.")
Claims 1 and 13	Claims 1-15 of U.S. Patent No. 9,166,412
Claims 23 and 34	Claims 1-15 of U.S. Patent No. 9,166,412 in view of U.S. Patent No. 7,085,945 ("Silvester")
Claims 1 and 13	Claims 1-16 of U.S. Patent No. 9,660,616
Claims 23 and 34	Claims 1-16 of U.S. Patent No. 9,660,616 in view of U.S. Patent No. 6,820,240 ("Bednar et al.")
Claims 40 and 52	Claims 4 and 12 of U.S. Patent No. 9,660,616
Claims 1 and 13	Claims 1-5 of U.S. Patent No. 10,243,542
Claims 23 and 34	Claims 1-5 of U.S. Patent No. 10,243,542 in view of U.S. Patent No. 6,820,240 ("Bednar et al.")
Claims 40 and 52	Claims 1-5 of U.S. Patent No. 10,243,542 in view of U.S. Patent No. 7.085,945 ("Silvester")
Claims 1-13	Claims 1-5 of U.S. Application No. 16/226,917
Claims 23 and 34	Claims 1-5 of U.S. Application No. 16/226,917 in view of U.S. Patent No. 6,820,240 ("Bednar et al.")
Claims 40 and 52	Claims 1-5 of U.S. Application No. 16/226,917 in view of U.S. Patent No. 7.085,945 ("Silvester")

Applicant defers determining whether the filing of a Terminal Disclaimer is appropriate until such time as one or more independent claims are indicated as allowable.

Section 251 Rejection

The Examiner rejects Claims 1-61 under 35 U.S.C. § 251 as based on a defective reissue oath or declaration or substitute statement. Applicant submits substitute declarations, stating:

> Applicants claimed less than they were entitled to. The original claims 1-39 require waiting for the source voltage of the first power island to settle down before changing a clock frequency of the first power island. This limitation is unduly narrow and is removed from newly added claims 40-61.

As shown above, the substitute statement clearly state that the new claims enlarge the scope of the original claims, which recited narrower limitations. Consequently, Applicant respectfully requests that the rejection under 35 U.S.C. § 251 be withdrawn.

Claim Interpretation

The Examiner contends that the "first power manager" and "second power manager" are means plus function limitations. Applicant respectfully disagrees and submits that "power manager" is a term that is well-known by persons of ordinary skill in the art of PMIC (power management integrated circuit) design to have a sufficiently definite structure. See MPEP §2181(I)(A).

Applicant's understanding with regard to terms "power island" and "smart power unit" is that the Examiner is not construing these terms to be means plus function elements.

Section 112 Rejection

The Examiner rejects Claims 1-33 and 40-51 under 35 U.S.C. §112(b). The rejection as to cancelled claims 1-22 is now moot.

As discussed above, "power manager" is a term that is well-known by persons of ordinary skill in the art and does not invoke 35 U.S.C. § 112(f). Power managers essentially manage power

consumption – that is, power managers are known to regulate clock frequency and voltage – of integrated circuits or power islands within ICs.

As stated in MPEP § 2181(I)(A), means plus function interpretation will not apply if persons of ordinary skill in the art reading the specification understand the term to have a sufficiently definite meaning as the name for the structure that performs the function, even when the term covers a broad class of structures or identifies the structures by their function (e.g., "filters," "brakes," "clamp," "screwdriver," and "locks"). (emphasis added). *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1372-73, 66 USPQ2d 1444, 1451-52 (Fed. Cir. 2003); *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d at 1369, 62 USPQ2d at 1664 (Fed. Cir. 2002); *Watts v. XL Sys. Inc.*, 232 F.3d 877, 880-81, 56 USPQ2d 1836, 1839 (Fed. Cir. 2000); *Greenberg v. Ethicon E`ndo-Surgery, Inc.*, 91 F.3d 1580, 1583, 39 USPQ2d 1783, 1786 (Fed. Cir. 1996) ("Many devices take their names from the functions they perform.").

Furthermore, if "first power manager" or "second power manager" are construed as circuitry, MPEP § 2181(I)(A) states that terms for circuitry that describe the function of the circuitry connote sufficient structure to persons of ordinary skill in the art and do not invoke 35 U.S.C. 112(f). Accordingly, "first power manager" and "second power manager" sufficiently connote definite structure and, therefore, do not invoke means-plus-function interpretation.

Applicant respectfully submits that a person of ordinary skill in the art would know voltage "settling down" to mean the voltage level is stabilizing. Furthermore, "settling down" is well known colloquial expression, that generally means "stabilizing" or "calming down".

Lastly, claims 41 and 43-51 have been amended to correctly depend from independent apparatus claim 40.

Consequently, Applicant requests that the rejection under 35 U.S.C. §112(b) be withdrawn.

Section 103(a) Rejection

The Examiner rejects the followings under 35 U.S.C. §103(a) as follows:

Claims	**Unpatentable Over**	**In View of**	**Further in View of**
1-6, 8-11, 13-18 and 20-22	U.S. Patent No. 6,968,467 ("*Inoue*")	U.S. Patent No. 6,141,762 ("*Nicol*")	

7 and 19	U.S. Patent No. 6,968,467 ("*Inoue*")	U.S. Patent No. 6,141,762 ("*Nicol*")	U.S. Patent No. 6,895,520 ("*Altmejd*")
12	U.S. Patent No. 6,968,467 ("*Inoue*")	U.S. Patent No. 6,141,762 ("*Nicol*")	U.S. Patent No. 7,085,945 ("*Silvester*")
23-32 and 34-39	U.S. Patent No. 6,968,467 ("*Inoue*")	U.S. Patent No. 6,820,240 ("*Bednar*")	
33	U.S. Patent No. 6,968,467 ("*Inoue*")	U.S. Patent No. 6,820,240 ("*Bednar*")	U.S. Patent No. 7.085,945 ("*Silvester*")
40-45, 47-57 and 59-61	U.S. Patent No. 6,968,467 ("*Inoue*")	U.S. Patent No. 7.085,945 ("*Silvester*") and U.S. Patent No. 6,141,762 ("*Nicol*")	U.S. Patent No. 6,895,520 ("*Altmejd*")
46 and 58	U.S. Patent No. 6,968,467 ("*Inoue*")	U.S. Patent No. 7.085,945 ("*Silvester*") and U.S. Patent No. 6,141,762 ("*Nicol*")	

Claims 1-22 are now canceled. As such, rejections as to these claims are now moot.

The rejection of claims 23-51 are traversed.

Claim 23 recites:

> 23. A system comprising:
>
> an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;
>
> a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

Applicant respectfully submits that *Inoue* and *Bednar*, taken alone or in combination, fail to teach or suggest "a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit".

The Office Action construes the data processing circuit 14 and data output unit 11 of *Inoue* as the first power manager of Claim 23 and contends that *Inoue*, 6:63-7:19 teaches the above-quoted feature of Claim 23. Applicant respectfully disagrees.

Inoue merely discloses that the data processing circuit and data output unit monitor the state of the CPU and manages power based on the state of the CPU. While the state information may based on the needs (i.e. an application that is to be run or instructions to be processed), there is no mention of the state being based on operation of the CPU such as temperature. Consequently, *Inoue* does not teach or suggest "a first power manager configured to manage the first power consumption based on needs **and** operation of the integrated circuit"

Bednar, which is cited for teaching a plurality of power islands, fails to remedy the deficiencies of *Inoue*.

Silvester, *Nicol*, and *Altmejd* also fail to remedy the deficiencies of *Inoue*, and the Office Action does not assert otherwise.

For at least these reasons, independent Claim 23 is allowable under 35 U.S.C. §103. Similarly, independent Claims 34 and 40, and 52, which have been amended to recite the same or similar patentable features as Claim 1, are also allowable under 35 U.S.C. §103. Dependent claims 24-33, 35-39, 41-51, and 53-61 variously depend from independent claims 23, 34, 40, and 52 and are, therefore, patentable at least by virtue of dependence. Accordingly, Applicant respectfully requests that the rejection of Claims 23-61 under 35 U.S.C. §103 be withdrawn.

CONCLUSION

Applicant's arguments are made without prejudice or disclaimer. By not responding to additional statements made by the Examiner, Applicant does not acquiesce to the additional statements. The distinctions between the applied references and the claims are provided as examples only and are sufficient to overcome the rejections. Applicant reserves the right to discuss additional or other distinctions in a later response or on appeal, if appropriate.

With respect to the Examiner's assertions and reasons for obviousness, Applicant does not consider any included statements have sufficiently put the Applicant on notice of the Examiner asserting Official Notice. If the Examiner intended to take Official Notice with respect to the any of the statements, Applicant traverses and respectfully requests that the Examiner specifically make such an assertion so that proper consideration may be given to the Notice.

In view of the above remarks, Applicant respectfully requests withdrawal of all rejections of the pending claims. Accordingly, Applicant respectfully requests allowance of the pending claims. The Examiner is invited to telephone the undersigned at the Examiner's convenience, if that would help further prosecution of the subject application. The Commissioner is authorized to charge any fees due to Deposit Account No.50-4154.

Respectfully submitted,

/Do Hyung Kim/

Dated: June 16, 2020

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PTO/SB/22 (03-13)
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) 01181-US-REI
Application Number 15/192,486	Filed 06/24/2016
For POWER MANAGERS FOR AN INTEGRATED CIRCUIT	
Art Unit 3992	Examiner YIGDALL, Michael J.

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$
☑ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$ 600.00
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 504154.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 66487.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Do Hyung Kim/	June 16, 2020
Signature	Date
Do Hyung Kim	214-494-4814
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: REIS.DECL
Document Description: Reissue Declaration Filed In Accordance With MPEP 1414

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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

This statement is directed to:

☐ The attached application,

OR

☒ was filed on June 24, 2016 as reissue application number 15/192,486.

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Daniel L HILLMAN

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
San Jose	CA	US

Mailing Address (except for a deceased or legally incapacitated inventor):

6607 Winterset Way

City	State	Zip	Country
San Jose	CA	95120	US

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Relationship to the inventor to whom this substitute statement applies:

☐ Legal Representative (for deceased or legally incapacitated inventor only),

☒ Assignee, or

☐ Joint Inventor.

Circumstances permitting execution of this substitute statement:

☐ Inventor is deceased,

☐ Inventor is under legal incapacity,

☒ Inventor cannot be found or reached after diligent effort, or

☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.175.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

If there are joint inventors, please check the appropriate box below:

☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below.
(Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

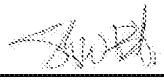
Applicants claimed less than they were entitled to. The original claims 1-39 require waiting for the source voltage of the first power island to settle down before changing a clock frequency of the first power island. This limitation is unduly narrow and is removed from newly added claims 40-61.

WARNING:

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PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Scott Burt | Date (Optional):

Signature: 

APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer.

Applicant Name: Conversant Intellectual Property Management Inc.

Title of Person Executing This Substitute Statement: SVP, Chief Intellectual Property Officer and General Counsel, Patent Licensing

The signer, whose title is supplied above, is authorized to act on behalf of the applicant.

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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Residence of the signer (unless provided in an application data sheet, PTO/SB/14 or equivalent):

City	State	County
Plano	TX	US

Mailing Address of the signer (unless provided in an application data sheet, PTO/SB/14 or equivalent):

5830 Granite Parkway #100-247, Suite 247

City	State	Zip	Country
Plano	TX	75024	US

Note: Use an additional PTO/AIA/07 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

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Doc code: REIS.DECL
Document Description: Reissue Declaration Filed In Accordance With MPEP 1414

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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

This statement is directed to:

☐ The attached application,

OR

☒ was filed on June 24, 2016 as reissue application number 15/192,486.

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Barry Alan HOBERMAN

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
Cupertino	CA	US

Mailing Address (except for a deceased or legally incapacitated inventor):

10290 Palo Vista Road

City	State	Zip	Country
Cupertino	CA	95014	US

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Relationship to the inventor to whom this substitute statement applies:

☐ Legal Representative (for deceased or legally incapacitated inventor only),

☒ Assignee, or

☐ Joint Inventor.

Circumstances permitting execution of this substitute statement:

☐ Inventor is deceased,

☐ Inventor is under legal incapacity,

☒ Inventor cannot be found or reached after diligent effort, or

☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.175.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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If there are joint inventors, please check the appropriate box below:

☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below.
(Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Applicants claimed less than they were entitled to. The original claims 1-39 require waiting for the source voltage of the first power island to settle down before changing a clock frequency of the first power island. This limitation is unduly narrow and is removed from newly added claims 40-61.

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PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Scott Burt | Date (Optional):

Signature: 

APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer.

Applicant Name: Conversant Intellectual Property Management Inc.

Title of Person Executing This Substitute Statement: SVP, Chief Intellectual Property Officer and General Counsel, Patent Licensing

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5830 Granite Parkway #100-247, Suite 247

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[Page 3 of 3]

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Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

This statement is directed to:

☐ The attached application,

OR

☒ was filed on June 24, 2016 as reissue application number 15/192,486.

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Jon SHIELL

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
San Jose	CA	US

Mailing Address (except for a deceased or legally incapacitated inventor):

801 Seabury Drive

City	State	Zip	Country
San Jose	CA	95136	US

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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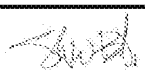
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Applicant Name: Conversant Intellectual Property Management Inc.

Title of Person Executing This Substitute Statement: SVP, Chief Intellectual Property Officer and General Counsel, Patent Licensing

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Electronic Patent Application Fee Transmittal	
Application Number:	15192486
Filing Date:	24-Jun-2016
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Filer:	Do Hyung Kim/Julie McLeod
Attorney Docket Number:	01181-US-REI
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
			Total in USD ($)	**600**

Electronic Acknowledgement Receipt	
EFS ID:	39739732
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Do Hyung Kim/Julie McLeod
Filer Authorized By:	Do Hyung Kim
Attorney Docket Number:	01181-US-REI
Receipt Date:	16-JUN-2020
Filing Date:	24-JUN-2016
Time Stamp:	23:30:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$600
RAM confirmation Number	E20206FN31143282
Deposit Account	504154
Authorized User	Julie McLeod
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2020_06_16_Response_Filed.pdf	73427 e80b8d754b3f80eeec022f0b3bfaea799f5f9928	yes	13
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	6	
	Applicant Arguments/Remarks Made in an Amendment		7	13	
Warnings:					
Information:					
2	Extension of Time	2020_06_16_EOT.pdf	188368 3355bc1487d0f49339b1a2b8eea60263ba638605	no	2
Warnings:					
Information:					
3	Oath or Declaration filed	Execurted_HILLMAN_Substitute_Statement.pdf	158487 382127fcac48940afbe9dd2abfff4228f7b9db3b	no	4
Warnings:					
Information:					
4	Oath or Declaration filed	Executed_HOBERMAN_Substitute_Statement.pdf	158520 c9e3e5c37edf58b54df9acb0765be624b00a24f9	no	4
Warnings:					
Information:					
5	Oath or Declaration filed	Executed_SHIELL_Substitute_Statement.pdf	158538 affa1f2a4b5f226ee9972f35ae62469f7535d01b	no	4

Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	31059 c0f138c698e8fac34fa80353c010db81083d5871	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	768399		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/192,486	Filing Date 06/24/2016	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	06/16/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 39	Minus	** 61	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 6	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/TYWANA P LOVELACE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/192,486	06/24/2016	Barry Alan Hoberman	01181-US-REI	6310

68256 7590 01/16/2020

Conversant Intellectual Property Management Corp
5830 Granite Parkway #100-247
Suite 247
Plano, TX 75024

EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
3992	

NOTIFICATION DATE	DELIVERY MODE
01/16/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipadmin@conversantip.com
mcleod@conversantip.com

Office Action Summary	Application No. 15/192,486	Applicant(s) Hoberman et al.	
	Examiner Michael J Yigdall	Art Unit 3992	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 24 June 2016.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-61 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-61 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 24 June 2016 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 8/31/2016, 1/31/2019, 8/20/2019.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

1. For reissue applications filed before September 16, 2012, all references to 35 U.S.C. § 251 and 37 CFR 1.172, 1.175 and 3.73 are to the law and rules in effect on September 15, 2012. Where specifically designated, these are "pre-AIA" provisions.

For reissue applications filed on or after September 16, 2012, all references to 35 U.S.C. § 251 and 37 CFR 1.172, 1.175 and 3.73 are to the current provisions.

2. The present application was filed on June 24, 2016 as a reissue application of U.S. Patent No. 8,762,923 ("the '923 patent").

The '923 patent issued on June 24, 2014 with claims 1-39. A preliminary amendment was filed in the present application on June 24, 2016 adding new claims 40-78. A second preliminary amendment was filed on September 21, 2016 canceling claims 62-78. Thus, claims 1-61 are pending and presented for examination.

Priority

3. The '923 patent resulted from U.S. Application No. 13/473,129, which was filed on May 16, 2012 as a division of U.S. Application No. 13/164,362, now U.S. Patent No. 8,782,590, which was filed on June 20, 2011 as a continuation of U.S. Application No. 12/332,529, now U.S. Patent No. 7,996,811, which was filed on December 11, 2008 as a continuation of U.S. Application No. 12/176,645, now U.S. Patent No. 7,945,885, which was filed on July 21, 2008 as a continuation of U.S. Application No. 11/336,097, now U.S. Patent No. 7,415,680, which was filed on January 20, 2006 as a continuation of U.S. Application No. 10/840,893, now U.S. Patent No. 7,051,306, which was filed on May 7, 2004 and claims the benefit of a provisional application filed on May 7, 2003.

Because the effective filing date of the '923 patent is before March 16, 2013, the present application is subject to the pre-AIA "first to invent" provisions.

In the event the determination of the status of the application as subject to pre-AIA 35 U.S.C. §§ 102 and 103 (or as subject to AIA 35 U.S.C. §§ 102 and 103) is incorrect, correction of the statutory basis for a rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same.

Reissue Oath/Declaration

4. The reissue declaration by the assignee filed on November 15, 2016 and the substitute statements in lieu of a reissue oath or declaration filed on November 15, 2016 on behalf of the inventors named on the '923 patent are defective. See 37 CFR 1.175 and MPEP § 1414.

The reissue declaration by the assignee is defective because an application for reissue may be made and sworn to by the assignee of the entire interest only if the application does not seek to enlarge the scope of the claims of the original patent or, for reissue applications filed on or after September 16, 2012, the application for the original patent was filed by the assignee of the entire interest under 37 CFR 1.46. See MPEP § 1412.03.

The substitute statements filed on behalf of the inventors named on the '923 patent are defective because they do not properly identify an error upon which the present application for reissue is based. The applicant states, "Applicants claimed less than they were entitled to." However, rather than identifying language in the original claims that renders the scope of the claims too narrow, the applicant states, "The original claims 1-39 recite subject matter related to power management systems for a integrated circuits [*sic*] using power islands, but do not recite monitoring temperatures of the plurality of power islands as newly added claims 30-41 do, and which Applicants are entitled to." For a broadening reissue, a general statement that the new

claims enlarge the scope of the original claims is not sufficient. The declaration or substitute statement must identify a claim that the application seeks to broaden, the language in which the error is found and how it renders the original patent wholly or partly inoperative or invalid. See MPEP § 1414(II). The examiner further notes that claims 30-39 are not new claims.

Claim Interpretation

5. The following is a quotation of 35 U.S.C. § 112(f):

> (f) ELEMENT IN CLAIM FOR A COMBINATION. — An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.
>
> The following is a quotation of pre-AIA 35 U.S.C. § 112, sixth paragraph:
>
> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

6. Claims 1-12, 23-33 and 40-51 include one or more limitations that are interpreted under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, because the limitations recite non-structural substitutes for the term "means" together with functional language, without reciting sufficient structure for performing the claimed functions. See MPEP § 2181(I). Accordingly, these limitations are interpreted to cover the corresponding structure disclosed in the specification for performing the claimed functions, and equivalents thereof. See MPEP § 2173.01(II). The elements interpreted under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, include the "first power manager" and the "second power manager" recited in each of independent claims 1, 23 and 40.

However, the specification of the '923 patent does not sufficiently disclose the structure for performing the functions of the claimed "first power manager" and "second power manager," or at least does not clearly link the disclosed structure to each of the claimed functions. See MPEP § 2181(III). See the rejections under 35 U.S.C. § 112(b) or pre-AIA 35 U.S.C. § 112, second paragraph, set forth below.

7. The term "power island" recited in the claims is interpreted as "any section, delineation, partition, or division of the integrated circuit [] where power consumption is controlled within the section, delineation, partition, or division" such as defined in the specification of the '923 patent at column 3, lines 56-59. See MPEP § 2111.01.

8. The term "smart power unit" recited in claims 6, 18, 45 and 57 is interpreted as circuitry that "control[s] power and clock distribution to the integrated circuit" such as defined in the specification of the '923 patent at column 7, lines 30-35. See MPEP § 2111.01.

Double Patenting

9. The examiner notes that a terminal disclaimer with respect to U.S. Patent No. 7,051,306, U.S. Patent No. 7,415,680 and U.S. Patent No. 7,945,885 was filed in the application for the '923 patent (i.e., U.S. Application No. 13/473,129) and was accepted.

10. The non-statutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A non-statutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not

patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (C.C.P.A. 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (C.C.P.A. 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (C.C.P.A. 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on non-statutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the "first inventor to file" provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) to 706.02(l)(3) for applications not subject to those provisions. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms that may be used. Please visit http://www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25 or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

11. Claims 1 and 13 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-74 of U.S. Patent No. 7,996,811 in view of U.S. Patent No. 6,968,467

to Inoue et al. ("Inoue"). Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-74 of U.S. Patent No. 7,996,811 in view of Inoue and U.S. Patent No. 6,820,240 to Bednar et al. ("Bednar"). Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 16, 23, 29, 44, 60 and 74 of U.S. Patent No. 7,996,811 in view of Inoue.

With respect to independent claims 1 and 13, the claimed invention would have been obvious over each of claims 1-74 of the reference patent. The limitations of the reference claims are analogous to those of claims 1 and 13. To the extent that the reference claims recite "a power manager" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-74 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34. To the extent that the reference claims recite "a power manager" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a

plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 16, 23, 29, 44, 60 and 74 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52. Where claims 40 and 52 recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded," the reference claims likewise recite that the power manager monitors the power consumptions of the plurality of power islands "using temperature ... measurement." To the extent that the reference claims recite "a power manager" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

12. Claims 1 and 13 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-73 of U.S. Patent No. 8,782,590 in view of Inoue. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-73 of U.S. Patent No. 8,782,590 in view of Inoue and Bednar. Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 4, 6, 12, 14, 19, 21, 26, 28, 33, 35, 40, 42, 47, 49, 54 and 56 of U.S. Patent No. 8,782,590 in view of Inoue.

With respect to independent claims 1 and 13, the claimed invention would have been obvious over each of claims 1-73 of the reference patent. The limitations of the reference claims are analogous to those of claims 1 and 13. To the extent that the reference claims recite "a power manager" or "a power management processor" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-73 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34. To the extent that the reference claims recite "a power manager" or "a power management processor" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the

art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 4, 6, 12, 14, 19, 21, 26, 28, 33, 35, 40, 42, 47, 49, 54 and 56 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52. Where claims 40 and 52 recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded," the reference claims likewise recite that the power manager or power management processor monitors power consumption signals of the plurality of power islands, including "temperature measurement" signals. To the extent that the reference claims recite "a power manager" or "a power management processor" that controls the power consumptions of the plurality of power islands rather than "a first power manager" and "a second power manager" such as claimed, such an arrangement would have been obvious to those of ordinary skill in the art. For example, Inoue teaches or suggests an arrangement where one power manager "operates as a master" and a plurality of other power managers "operate as

slaves," allowing every power island to "manage the power of its own" (see, e.g., FIG. 1, column 6, lines 56-62 and column 7, lines 31-46).

13. Claims 1 and 13 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-15 of U.S. Patent No. 9,166,412. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-15 of U.S. Patent No. 9,166,412 in view of Bednar. Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-15 of U.S. Patent No. 9,166,412 in view of U.S. Patent No. 7,085,945 to Silvester ("Silvester").

With respect to independent claims 1 and 13, the claimed invention would have been obvious over each of claims 1-15 of the reference patent. The limitations of the reference claims are analogous to those of claims 1 and 13.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-15 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34.

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 1-15 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52.

The reference claims do not recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded" such as claimed. However, as Silvester suggests, monitoring temperature and managing the power consumption of a power island when a temperature threshold is exceeded would have been obvious to those of ordinary skill in the art so as to lower the temperature and prevent failure of the power island (see, e.g., column 1, lines 22-34 and column 3, lines 16-60).

14. Claims 1 and 13 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-16 of U.S. Patent No. 9,660,616. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-16 of U.S. Patent No. 9,660,616 in view of Bednar. Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 4 and 12 of U.S. Patent No. 9,660,616.

With respect to independent claims 1 and 13, the claimed invention would have been obvious over each of claims 1-16 of the reference patent. The limitations of the reference claims are analogous to those of claims 1 and 13.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-16 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34.

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island

would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 4 and 12 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52. Where claims 40 and 52 recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded," the reference claims likewise recite that the first power manager monitors one or more power consumption signals of the plurality of power islands "wherein the one or more power consumption signals include temperature or power dissipation measurement."

15. Claims 1 and 13 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of U.S. Patent No. 10,243,542. Claims 23 and 34 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of U.S. Patent No. 10,243,542 in view of Bednar. Claims 40 and 52 are rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of U.S. Patent No. 10,243,542 in view of Silvester.

With respect to independent claims 1 and 13, the claimed invention would have been obvious over each of claims 1-5 of the reference patent. The limitations of the reference claims are analogous to those of claims 1 and 13.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-5 of the reference patent. The limitations of the reference claims are analogous to those of claims 23 and 34.

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 1-5 of the reference patent. The limitations of the reference claims are analogous to those of claims 40 and 52.

The reference claims do not recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded" such as claimed. However, as Silvester suggests, monitoring temperature and managing the power consumption of a power island when a temperature threshold is exceeded would have been obvious to those of ordinary skill in the art so as to lower the temperature and prevent failure of the power island (see, e.g., column 1, lines 22-34 and column 3, lines 16-60).

16. Claims 1 and 13 are provisionally rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of pending U.S. Application No. 16/226,917. Claims 23 and 34 are provisionally rejected on the ground of non-statutory double patenting as

unpatentable over claims 1-5 of pending U.S. Application No. 16/226,917 in view of Bednar. Claims 40 and 52 are provisionally rejected on the ground of non-statutory double patenting as unpatentable over claims 1-5 of pending U.S. Application No. 16/226,917 in view of Silvester.

With respect to independent claims 1 and 13, the claimed invention would have been obvious over each of claims 1-5 of the reference application. The limitations of the reference claims are analogous to those of claims 1 and 13.

With respect to independent claims 23 and 34, the claimed invention would have been obvious over each of claims 1-5 of the reference application. The limitations of the reference claims are analogous to those of claims 23 and 34.

The reference claims do not recite "saving a state of the first power island" such as claimed. However, saving the state of a power island before powering off the power island would have been obvious to those of ordinary skill in the art so as to restore the state of the power island after powering on the power island. For example, Bednar teaches or suggests saving the state of a power island in state-saving latches that "consume minimal power" in the power island, so that the power island "can be quickly returned to normal operation" when powered on (see, e.g., FIG. 1, column 3, lines 28-46 and column 4, lines 30-53).

With respect to independent claims 40 and 52, the claimed invention would have been obvious over each of claims 1-5 of the reference application. The limitations of the reference claims are analogous to those of claims 40 and 52.

The reference claims do not recite that the first power manager "monitors the plurality of power islands if a temperature threshold has been exceeded" such as claimed. However, as Silvester suggests, monitoring temperature and managing the power consumption of a power

island when a temperature threshold is exceeded would have been obvious to those of ordinary skill in the art so as to lower the temperature and prevent failure of the power island (see, e.g., column 1, lines 22-34 and column 3, lines 16-60).

Objections to the Claims

17. Claim 13 is objected to for including "~~a~~the" rather than "the" in the step, "in a first power manager, managing ~~a~~the first power consumption based on needs and operation of the integrated circuit." See MPEP § 1453.

Rejections under 35 U.S.C. § 251

18. Claims 1-61 are rejected under 35 U.S.C. § 251 as based upon a defective reissue oath or declaration or substitute statement as set forth above. See 37 CFR 1.175.

Rejections under 35 U.S.C § 112

19. The following is a quotation of 35 U.S.C. § 112(b):

> (b) CONCLUSION. — The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.
>
> The following is a quotation of pre-AIA 35 U.S.C. § 112, second paragraph:
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

20. Claims 1-33 and 40-51 are rejected under 35 U.S.C. § 112(b) or pre-AIA 35 U.S.C. § 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention.

With respect to claims 1-12, 23-33 and 40-51, the claims include one or more limitations that are interpreted under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, as set forth above. However, the specification of the '923 patent does not sufficiently disclose the structure for performing the claimed functions, or at least does not clearly link the disclosed structure to each of the claimed functions. Thus, the claims are indefinite.

Claims 1, 23 and 40 recite a "first power manager" configured to "manage the first power consumption based on needs and operation of the integrated circuit." Claim 40 further recites that the first power manager is configured to "determine power trade-offs between the power islands" and "monitors the plurality of power islands if a temperature threshold has been exceeded." With respect to a "power manager" such as claimed, the specification discloses a power manager 120 and "examples of the power manager 120," including "the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM)." However, the power manager 120 is disclosed in terms of its function rather than its structure. The specification discloses that the power manager "is any circuitry, device, or system configured to" perform the functions of the power manager. See the '923 patent at column 4, lines 18-58. If the claimed "first power manager" is the master power manager, the specification discloses that the MPM 280 "is any circuitry configured to control the 'global' power behavior of the entire integrated circuit 250." *Id.* at column 5, lines 48-58. However, the structure that actually performs the functions of the MPM 280 is not apparent.

The specification further discloses an embedded firmware stack 210, which "includes software layers that run on a central processing unit (CPU)," including "a power management control layer (PMCL) 218" and "a global power application layer (GPAL) 214." The embedded firmware stack 210 includes "power manager (PM) firmware 224 for the MPM, IPM and/or

SPM," which "is firmware executed by the master power manager 280, the intermediate power manager, and the slave power managers 264 and 274." *Id.* at column 4, line 59 to column 5, line 47. If the claimed "first power manager" is a CPU or processor that executes firmware to perform the claimed functions, then the corresponding structure must include an algorithm for each of the functions. See MPEP § 2181(II)(B). However, the algorithms for performing the claimed functions are not apparent.

Claims 1, 23 and 40 recite a "second power manager" configured to "communicate with the first power manager" and "respond to a request to manage the second power consumption for the first power island." Claim 1 further recites that the second power manager responds by "changing a source voltage of the first power island," then "waiting for the source voltage of the first power island to settle down" and "changing a clock frequency of the first power island." Claim 23 further recites that the second power manager responds by "stopping a clock of the first power island" and "saving a state of the first power island," and then "powering off the first power island." Claim 40 further recites that the second power manager responds by "changing a source voltage" and "changing a clock frequency of the first power island." As noted above, the specification discloses the power manager 120 in terms of its function rather than its structure. If the claimed "second power manager" is the slave power manager, the specification discloses that the SPM 264 "is any circuitry configured to control power within a power island [260] in the integrated circuit 250," and states, "The description for the SPM 264 also applies to the SPM 274 for the power island 270." See the '923 patent at column 6, lines 11-40. However, the structure that actually performs the functions of the SPM 264 or 274 is not apparent. Likewise, if the claimed "second power manager" is a CPU or processor that executes firmware to perform the functions, the algorithms for performing each of the claimed functions are not apparent.

The applicant may (1) amend the claims so that these limitations are no longer interpreted as limitations under 35 U.S.C. § 112(f) or pre-AIA 35 U.S.C. § 112, sixth paragraph, (2) amend the specification to expressly recite what structure performs each of the claimed functions, without adding new matter, or (3) amend the specification such that the disclosed structure is clearly linked to each of the claimed functions, without adding new matter. If the applicant is of the opinion that the specification already implicitly or inherently discloses the corresponding structure and clearly links the disclosed structure to each of the claimed functions, then the applicant should (1) amend the specification to expressly recite the corresponding structure and clearly link the disclosed structure to each of the claimed functions, without adding new matter, or (2) state on the record what corresponding structure implicitly or inherently set forth in the specification performs each of the claimed functions.

With respect to claims 1-22, each of claims 1 and 13 recites "waiting for the source voltage of the first power island to settle down." It is not apparent what constitutes the source voltage "settling down." The specification of the '923 patent discloses:

> In step 816, the PMCL 218 sends a command to the SPU 290 to change the Vdd on the selected power pins and waits for the affected area to "settle down."

Column 9, lines 7-10. However, the specification does not define the term "settle down," nor does the specification include examples or disclose some standard for measuring whether or not the source voltage "settled down." See MPEP § 2173.05(b). Claims 2-12 and 14-22 are dependent on claims 1 and 13 and therefore are indefinite for the same reason.

With respect to claims 41-51, each of dependent claims 41 and 43-51 attempts to further limit "[t]he system of claim 39." However, claim 40 is the preceding independent claim directed to a system, whereas claim 39 is directed to a method. Claim 42 is dependent on claim 41 and

therefore is indefinite for the same reason. With further respect to claim 50, the claim recites the limitation "wherein the power management software is embedded firmware in the integrated circuit." However, there is insufficient antecedent basis in the claim for "the power management software" since the term "power management software" is introduced in claim 49 rather than in claim 39 or claim 40.

Rejections under 35 U.S.C. § 103

21. The following is a quotation of pre-AIA 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 1-6, 8-11, 13-18 and 20-22 are rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,968,467 to Inoue et al. ("Inoue") in view of U.S. Patent No. 6,141,762 to Nicol et al. ("Nicol").

Claim 1

Inoue teaches or suggests a system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation);

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20);

a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1) configured to manage the first power consumption based on needs and operation of the integrated circuit (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit); and

a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1) configured to:

a) communicate with the first power manager (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus); and

b) respond to a request to manage the second power consumption for the first power island (see, e.g., column 8, lines 12-19, describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block (see, e.g., column 10, lines 4-30). To the extent that Inoue discloses changing the clock supply to "on" or "off" rather than changing the clock frequency, Inoue does not expressly disclose responding to the request by:

i) changing a source voltage of the first power island;

ii) after the changing, waiting for the source voltage of the first power island to settle down; and

iii) after the waiting, changing a clock frequency of the first power island.

However, in an analogous art, Nicol teaches managing the power consumption of processing elements within an integrated circuit, including changing the supply voltage and the clock frequency for each of the processing elements (see, e.g., FIG. 2, FIG. 4, column 2, lines 18-31 and column 5, line 66 to column 6, line 13). The processing elements represent power islands within the integrated circuit. Nicol discloses increasing the supply voltage, for example, and then after the new supply voltage is stable, increasing the clock frequency (see, e.g., FIG. 3, column 4, line 38 to column 5, line 2 and column 5, lines 30-41). The teachings of Nicol allow for power management with "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit (see, e.g., column 2, lines 18-31).

A person of ordinary skill in the art could have combined the teachings of Inoue and Nicol with predictable results, and would have been prompted to implement the second power manager of Inoue so as to change both the supply voltage and the clock frequency of the block. As Nicol suggests, such an implementation would allow for "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit. Thus, the combined teachings of Inoue and Nicol would have suggested responding to the request by:

i) changing a source voltage of the first power island;

ii) after the changing, waiting for the source voltage of the first power island to settle down; and

iii) after the waiting, changing a clock frequency of the first power island.

Accordingly, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 2

Inoue in view of Nicol further teaches or suggests the system of claim 1 wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing increasing the supply voltage and the clock supply, and Nicol at column 5, lines 30-41, further describing increasing the supply voltage ahead of increasing the clock frequency).

Claim 3

Inoue in view of Nicol further teaches or suggests the system of claim 2 wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 4

Inoue in view of Nicol further teaches or suggests the system of claim 1 wherein the first power manager is further configured to communicate the request to the second power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 5

Inoue in view of Nicol further teaches or suggests the system of claim 1 wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 6

Inoue in view of Nicol further teaches or suggests the system of claim 1 wherein the source voltage of the first power island is controlled by a smart power unit (see, e.g., Inoue at column 7, lines 31-44 and column 10, lines 4-30, describing that the block controls the supply voltage and the clock supply).

Claim 8

Inoue in view of Nicol further teaches or suggests the system of claim 1 wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Claim 9

Inoue in view of Nicol further teaches or suggests the system of claim 1 wherein the second power manager comprises firmware processable on the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager is programmed).

Claim 10

Inoue in view of Nicol further teaches or suggests the system of claim 1 wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager comprises a processor and programming).

Claim 11

Inoue in view of Nicol further teaches or suggests the system of claim 10 wherein the power management software is embedded firmware in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65).

Claim 13

Inoue teaches or suggests a method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation), and the method comprising:

in a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1), managing the first power consumption based on needs and operation of the integrated circuit (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit);

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20, and see, e.g., column 10, lines 4-30, further describing supplying a clock to the block);

providing a source voltage to the first power island (see, e.g., column 10, lines 4-30, describing supplying a voltage to the block); and

in a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1), communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus, and column 8, lines 12-19, further describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block (see, e.g., column 10, lines 4-30). To the extent that Inoue discloses changing the clock supply to "on" or "off" rather than changing the clock frequency, Inoue does not expressly disclose responding to the request by:

changing the source voltage of the first power island;

after the changing, waiting for the source voltage of the first power island to settle down; and

after the waiting, changing a clock frequency of the clock.

However, in an analogous art, Nicol teaches managing the power consumption of processing elements within an integrated circuit, including changing the supply voltage and the clock frequency for each of the processing elements (see, e.g., FIG. 2, FIG. 4, column 2, lines 18-31 and column 5, line 66 to column 6, line 13). The processing elements represent power islands within the integrated circuit. Nicol discloses increasing the supply voltage, for example, and then after the new supply voltage is stable, increasing the clock frequency (see, e.g., FIG. 3, column 4, line 38 to column 5, line 2 and column 5, lines 30-41). The teachings of Nicol allow for power management with "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit (see, e.g., column 2, lines 18-31).

A person of ordinary skill in the art could have combined the teachings of Inoue and Nicol with predictable results, and would have been prompted to implement the second power manager of Inoue so as to change both the supply voltage and the clock frequency of the block. As Nicol suggests, such an implementation would allow for "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit. Thus, the combined teachings of Inoue and Nicol would have suggested responding to the request by:

changing the source voltage of the first power island;

after the changing, waiting for the source voltage of the first power island to settle down; and

after the waiting, changing a clock frequency of the clock.

Accordingly, a method such as claimed would have been obvious to those of ordinary skill in the art.

Claim 14

Inoue in view of Nicol further teaches or suggests the method of claim 13 wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing increasing the supply voltage and the clock supply, and Nicol at column 5, lines 30-41, further describing increasing the supply voltage ahead of increasing the clock frequency).

Claim 15

Inoue in view of Nicol further teaches or suggests the method of claim 14 further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 16

Inoue in view of Nicol further teaches or suggests the method of claim 13 wherein the request is communicated to the second power manager by the first power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 17

Inoue in view of Nicol further teaches or suggests the method of claim 13 further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 18

Inoue in view of Nicol further teaches or suggests the method of claim 13 wherein the source voltage of the first power island is controlled by a smart power unit (see, e.g., Inoue at column 7, lines 31-44 and column 10, lines 4-30, describing that the block controls the supply voltage and the clock supply).

Claim 20

Inoue in view of Nicol further teaches or suggests the method of claim 13 wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Claim 21

Inoue in view of Nicol further teaches or suggests the method of claim 13 further comprising, in a third power manager (see, e.g., Inoue at column 7, lines 27-30, and power management unit 32 and power control unit 33 of block 30 in FIG. 1):

i) managing a third power consumption of the power consumptions, and the plurality of power islands including a second power island having an associated power consumption that is the third power consumption (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a second power island with a third power consumption in block 30, and see, e.g., column 6, line 63 to column 7, line 19, describing that the third power manager manages the power consumption of the block); and

ii) communicating with the first power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19, describing that the third power manager communicates with the first power manager).

Claim 22

Inoue in view of Nicol further teaches or suggests the method of claim 21 wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62).

23. Claims 7 and 19 are rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of Nicol and further in view of U.S. Patent No. 6,895,520 to Altmejd et al. ("Altmejd").

Claim 7

Inoue in view of Nicol teaches or suggests the system of claim 1, but does not expressly disclose the limitation wherein the source voltage of the first power island is provided by an external regulator.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue such that the source voltage of the first power island is provided by an external regulator with predictable results and with no change in function. For example, in an analogous art, Altmejd teaches managing the power consumption of functional blocks within an integrated circuit (see, e.g., column 1, line 62 to column 2, line 6). Altmejd expressly discloses a regulated supply voltage that is "supplied externally by a voltage regulator" such as known in the art (see, e.g., column 5, lines 27-29). Thus, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 19

Inoue in view of Nicol teaches or suggests the method of claim 13, but does not expressly disclose providing external regulation for the source voltage of the first power island.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue so as to provide external regulation for the source voltage of the first power island with predictable results and with no change in function. For example, in an analogous art, Altmejd teaches managing the power consumption of functional blocks within an integrated circuit (see, e.g., column 1, line 62 to column 2, line 6). Altmejd expressly discloses a regulated supply voltage that is "supplied externally by a voltage regulator" such as known in the art (see, e.g.,

column 5, lines 27-29). Thus, a method such as claimed would have been obvious to those of ordinary skill in the art.

24. Claim 12 is rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of Nicol and further in view of U.S. Patent No. 7,085,945 to Silvester ("Silvester").

Claim 12

Inoue in view of Nicol teaches or suggests the system of claim 1, but does not expressly disclose the limitation wherein the first power manager is located outside the integrated circuit.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue such that the first power manager is located outside the integrated circuit with predictable results and with no change in function. For example, in an analogous art, Silvester teaches a controller 305/310 for managing the power consumption of functional unit blocks within an integrated circuit (see, e.g., column 4, line 45 to column 5, line 12). Silvester expressly discloses an embodiment where the controller 305 is inside the integrated circuit or on the same die as the functional unit blocks (see, e.g., FIG. 3A), and an embodiment where the controller 310 is outside the integrated circuit or on a different die (see, e.g., FIG. 3B). Thus, a system such as claimed would have been obvious to those of ordinary skill in the art.

25. Claims 23-32 and 34-39 are rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of U.S. Patent No. 6,820,240 to Bednar et al. ("Bednar").

Claim 23

Inoue teaches or suggests a system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation);

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20);

a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1) configured to manage the first power consumption based on needs and the operation of the integrated circuit (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit); and

a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1) configured to:

a) communicate with the first power manager (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus); and

b) respond to a request to manage the second power consumption for the first power island (see, e.g., column 8, lines 12-19, describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block, including stopping the clock supply (see,

e.g., column 10, lines 4-30). Inoue does not expressly disclose saving a state of the block, and therefore does not expressly disclose responding to the request by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

However, in an analogous art, Bednar teaches a system-on-a-chip comprising a plurality of voltage islands and state-saving latches 125 for saving state when a voltage island 120 is powered off (see, e.g., FIG. 1 and column 3, lines 22-46). Bednar discloses saving state in the latches before powering off the island, "eliminating the need to transfer logic states off-island and back in order to save and restore necessary logic states" (see, e.g., column 4, lines 30-53).

A person of ordinary skill in the art could have combined the teachings of Inoue and Bednar with predictable results, and would have been prompted to implement the second power manager of Inoue so as to save the state of the block before powering off the block. As Bednar suggests, "some subset of the logic state, prior to power-down, may need to be preserved to resume operation" when power is restored to the block, and the teachings of Bednar allow for saving state and resuming operation "quickly" when power is restored (see, e.g., Bednar at column 4, lines 30-53). Thus, the combined teachings of Inoue and Bednar would have suggested responding to the request by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

Accordingly, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 24

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the second power manager is further configured to carry out the saving of the state of the first power island after the stopping (see, e.g., Bednar at column 4, lines 30-53).

Claim 25

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the first power manager is further configured to communicate the request to the second power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 26

Inoue in view of Bednar further teaches or suggests the system of claim 23 further comprising a buffer for storing the state that is saved (see, e.g., Bednar at FIG. 1 and column 4, lines 30-53, describing that the state-saving latches 125 are a buffer).

Claim 27

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the second power manager is further configured to respond to another request, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock of the first power island

(see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing powering on and starting the clock supply, and Bednar at column 4, lines 30-53, describing restoring the state of the island after powering on the island).

Claim 28

Inoue in view of Bednar further teaches or suggests the system of claim 27 further comprising a buffer for storing the state that is saved, and the buffer being accessible during the restoring (see, e.g., Bednar at FIG. 1 and column 4, lines 30-53, describing that the state-saving latches 125 are a buffer that is accessed during the restoring).

Claim 29

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Claim 30

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the second power manager comprises firmware processable on the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager is programmed).

Claim 31

Inoue in view of Bednar further teaches or suggests the system of claim 23 wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager comprises a processor and programming).

Claim 32

Inoue in view of Bednar further teaches or suggests the system of claim 31 wherein the power management software is embedded firmware in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65).

Claim 34

Inoue teaches or suggests a method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation), and the method comprising:

in a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1), managing a first power consumption based on needs and operation of the integrated circuit (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit);

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20, and see, e.g., column 10, lines 4-30, further describing supplying a clock to the block);

in a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1), communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus, and column 8, lines 12-19, further describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block, including stopping the clock supply (see, e.g., column 10, lines 4-30). Inoue does not expressly disclose saving a state of the block, and therefore does not expressly disclose responding to the request by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

However, in an analogous art, Bednar teaches a system-on-a-chip comprising a plurality of voltage islands and state-saving latches 125 for saving state when a voltage island 120 is powered off (see, e.g., FIG. 1 and column 3, lines 22-46). Bednar discloses saving state in the

latches before powering off the island, "eliminating the need to transfer logic states off-island and back in order to save and restore necessary logic states" (see, e.g., column 4, lines 30-53).

A person of ordinary skill in the art could have combined the teachings of Inoue and Bednar with predictable results, and would have been prompted to implement the second power manager of Inoue so as to save the state of the block before powering off the block. As Bednar suggests, "some subset of the logic state, prior to power-down, may need to be preserved to resume operation" when power is restored to the block, and the teachings of Bednar allow for saving state and resuming operation "quickly" when power is restored (see, e.g., Bednar at column 4, lines 30-53). Thus, the combined teachings of Inoue and Bednar would have suggested responding to the request by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

Accordingly, a method such as claimed would have been obvious to those of ordinary skill in the art.

Claim 35

Inoue in view of Bednar further teaches or suggests the method of claim 34 wherein the saving of the state of the first power island is carried out after the stopping (see, e.g., Bednar at column 4, lines 30-53).

Claim 36

Inoue in view of Bednar further teaches or suggests the method of claim 34 wherein the request is communicated to the second power manager by the first power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 37

Inoue in view of Bednar further teaches or suggests the method of claim 34 wherein the state that is saved is stored in a buffer (see, e.g., Bednar at FIG. 1 and column 4, lines 30-53, describing that the state-saving latches 125 are a buffer).

Claim 38

Inoue in view of Bednar further teaches or suggests the method of claim 34 further comprising responding to another request that is received by the second power manager, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock

(see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing powering on and starting the clock supply, and Bednar at column 4, lines 30-53, describing restoring the state of the island after powering on the island).

Claim 39

Inoue in view of Bednar further teaches or suggests the method of claim 38 wherein the state that is saved is stored in a buffer accessed during the restoring (see, e.g., Bednar at FIG. 1

and column 4, lines 30-53, describing that the state-saving latches 125 are a buffer that is accessed during the restoring).

26. Claim 33 is rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of Bednar and further in view of Silvester.

Claim 33

Inoue in view of Bednar teaches or suggests the system of claim 23, but does not expressly disclose the limitation wherein the first power manager is located outside the integrated circuit.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue such that the first power manager is located outside the integrated circuit with predictable results and with no change in function. For example, in an analogous art, Silvester teaches a controller 305/310 for managing the power consumption of functional unit blocks within an integrated circuit (see, e.g., column 4, line 45 to column 5, line 12). Silvester expressly discloses an embodiment where the controller 305 is inside the integrated circuit or on the same die as the functional unit blocks (see, e.g., FIG. 3A), and an embodiment where the controller 310 is outside the integrated circuit or on a different die (see, e.g., FIG. 3B). Thus, a system such as claimed would have been obvious to those of ordinary skill in the art.

27. Claims 40-45, 47-57 and 59-61 are rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of Silvester and Nicol.

Claim 40

Inoue teaches or suggests a system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation);

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20);

a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1) configured to:

a) manage the first power consumption based on needs and operation of the integrated circuit (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit);

b) determine power trade-offs between the power islands (see, e.g., column 11, lines 12-17 and 41-55, describing that the first power manager determines which blocks to control).

Inoue does not expressly disclose that the first power manager is configured to:

c) monitors the plurality of power islands if a temperature threshold has been exceeded.

However, in an analogous art, Silvester teaches managing the power consumption of functional unit blocks within an integrated circuit, including monitoring whether a temperature threshold is exceeded (see, e.g., column 3, lines 16-60). The functional unit blocks represent power islands within the integrated circuit. The teachings of Silvester allow for managing the

temperature of a functional unit block to prevent failure (see, e.g., column 1, lines 22-34 and column 3, lines 50-60).

A person of ordinary skill in the art could have combined the teachings of Inoue and Silvester with predictable results, and would have been prompted to implement the first power manager of Inoue so as to monitor the plurality of power islands if a temperature threshold has been exceeded. As Silvester suggests, such an implementation would allow for managing the temperature of a power island to prevent failure.

Inoue further teaches or suggests:

a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1) configured to:

a) communicate with the first power manager (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus); and

b) respond to a request to manage the second power consumption for the first power island (see, e.g., column 8, lines 12-19, describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block (see, e.g., column 10, lines 4-30). To the extent that Inoue discloses changing the clock supply to "on" or "off" rather than changing the clock frequency, Inoue does not expressly disclose responding to the request by:

i) changing a source voltage; and

ii) changing a clock frequency of the first power island.

However, in an analogous art, Nicol teaches managing the power consumption of processing elements within an integrated circuit, including changing the supply voltage and the

clock frequency for each of the processing elements (see, e.g., FIG. 2, FIG. 4, column 2, lines 18-31 and column 5, line 66 to column 6, line 13). The processing elements represent power islands within the integrated circuit. Nicol discloses increasing the supply voltage, for example, and then after the new supply voltage is stable, increasing the clock frequency (see, e.g., FIG. 3, column 4, line 38 to column 5, line 2 and column 5, lines 30-41). The teachings of Nicol allow for power management with "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit (see, e.g., column 2, lines 18-31).

A person of ordinary skill in the art could have combined the teachings of Inoue and Nicol with predictable results, and would have been prompted to implement the second power manager of Inoue so as to change both the supply voltage and the clock frequency of the block. As Nicol suggests, such an implementation would allow for "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit. Thus, the combined teachings of Inoue and Nicol would have suggested responding to the request by:

i) changing a source voltage; and

ii) changing a clock frequency of the first power island.

Accordingly, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 41

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [40], wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing increasing the supply voltage and the

clock supply, and Nicol at column 5, lines 30-41, further describing increasing the supply voltage ahead of increasing the clock frequency).

Claim 42

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim 41, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 43

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [40], wherein the first power manager is further configured to communicate the request to the second power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 44

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [40], wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power

management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 45

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [40], wherein the source voltage of the first power island is controlled by a smart power unit (see, e.g., Inoue at column 7, lines 31-44 and column 10, lines 4-30, describing that the block controls the supply voltage and the clock supply).

Claim 47

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [40], wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Claim 48

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [40], wherein the second power manager comprises firmware processable on the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager is programmed).

Claim 49

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [40], wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65, describing that the second power manager comprises a processor and programming).

Claim 50

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [49], wherein the power management software is embedded firmware in the integrated circuit (see, e.g., Inoue at column 9, lines 48-65).

Claim 51

Inoue in view of Silvester and Nicol further teaches or suggests the system of claim [40], wherein the first power manager is located outside the integrated circuit.

Namely, a person of ordinary skill in the art could have implemented the teachings of Inoue such that the first power manager is located outside the integrated circuit with predictable results and with no change in function. For example, Silvester teaches a controller 305/310 for managing the power consumption of the functional unit blocks within the integrated circuit (see, e.g., column 4, line 45 to column 5, line 12). Silvester expressly discloses an embodiment where the controller 305 is inside the integrated circuit or on the same die as the functional unit blocks (see, e.g., FIG. 3A), and an embodiment where the controller 310 is outside the integrated circuit or on a different die (see, e.g., FIG. 3B). Thus, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 52

Inoue teaches or suggests a method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption (see, e.g., FIG. 1 and column 2, lines 24-43, describing a power management system for an integrated circuit, where the integrated circuit effects power consumptions in operation and each of blocks 20, 30 and 40 effects a power consumption in operation), and the method comprising:

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption (see, e.g., FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, including a first power island with a second power consumption in block 20, and see, e.g., column 10, lines 4-30, further describing supplying a clock to the block);

in a first power manager (see, e.g., data processing circuit 14 and data output unit 11 of block 10 in FIG. 1), managing the first power consumption based on needs and operation of the integrated circuit, and determining power-trade-offs between the power islands (see, e.g., column 6, line 63 to column 7, line 19, describing that the first power manager manages the power consumption of the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Inoue does not expressly disclose that the first power manager monitors the plurality of power islands if a temperature threshold has been exceeded.

However, in an analogous art, Silvester teaches managing the power consumption of functional unit blocks within an integrated circuit, including monitoring whether a temperature

threshold is exceeded (see, e.g., column 3, lines 16-60). The functional unit blocks represent power islands within the integrated circuit. The teachings of Silvester allow for managing the temperature of a functional unit block to prevent failure (see, e.g., column 1, lines 22-34 and column 3, lines 50-60).

A person of ordinary skill in the art could have combined the teachings of Inoue and Silvester with predictable results, and would have been prompted to implement the first power manager of Inoue so as to monitor the plurality of power islands if a temperature threshold has been exceeded. As Silvester suggests, such an implementation would allow for managing the temperature of a power island to prevent failure.

Inoue further teaches or suggests:

in a second power manager (see, e.g., power management unit 22 and power control unit 23 of block 20 in FIG. 1), communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island (see, e.g., column 6, lines 44-49, describing that the second power manager communicates with the first power manager over a bus, and column 8, lines 12-19, further describing that the second power manager responds to power management data from the first power manager).

Inoue discloses that the second power manager controls the supply voltage and the clock supply to manage the power consumption of the block (see, e.g., column 10, lines 4-30). To the extent that Inoue discloses changing the clock supply to "on" or "off" rather than changing the clock frequency, Inoue does not expressly disclose responding to the request by:

changing a source voltage; and

changing a clock frequency of the clock of the first power island.

However, in an analogous art, Nicol teaches managing the power consumption of processing elements within an integrated circuit, including changing the supply voltage and the clock frequency for each of the processing elements (see, e.g., FIG. 2, FIG. 4, column 2, lines 18-31 and column 5, line 66 to column 6, line 13). The processing elements represent power islands within the integrated circuit. Nicol discloses increasing the supply voltage, for example, and then after the new supply voltage is stable, increasing the clock frequency (see, e.g., FIG. 3, column 4, line 38 to column 5, line 2 and column 5, lines 30-41). The teachings of Nicol allow for power management with "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit (see, e.g., column 2, lines 18-31).

A person of ordinary skill in the art could have combined the teachings of Inoue and Nicol with predictable results, and would have been prompted to implement the second power manager of Inoue so as to change both the supply voltage and the clock frequency of the block. As Nicol suggests, such an implementation would allow for "significantly greater than on/off granularity" to minimize the power consumption of the integrated circuit. Thus, the combined teachings of Inoue and Nicol would have suggested responding to the request by:

changing a source voltage; and

changing a clock frequency of the clock of the first power island.

Accordingly, a method such as claimed would have been obvious to those of ordinary skill in the art.

Claim 53

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30,

describing increasing the supply voltage and the clock supply, and Nicol at column 5, lines 30-41, further describing increasing the supply voltage ahead of increasing the clock frequency).

Claim 54

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 53, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 55

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, wherein the request is communicated to the second power manager by the first power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19).

Claim 56

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island (see, e.g., Inoue at FIG. 5 and column 10, lines 4-30, describing decreasing the supply voltage and the clock supply in response

to power management data, and Nicol at column 5, lines 30-41, further describing lowering the clock frequency ahead of decreasing the supply voltage).

Claim 57

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, wherein the source voltage of the first power island is controlled by a smart power unit (see, e.g., Inoue at column 7, lines 31-44 and column 10, lines 4-30, describing that the block controls the supply voltage and the clock supply).

Claim 59

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit, and column 11, lines 12-17 and 41-55, further describing that the first power manager determines which blocks to control).

Claim 60

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 52, further comprising, in a third power manager (see, e.g., Inoue at column 7, lines 27-30, and power management unit 32 and power control unit 33 of block 30 in FIG. 1):

i) managing a third power consumption of the power consumptions, and the plurality of power islands including a second power island having an associated power consumption that is the third power consumption (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62, describing that each of blocks 20, 30 and 40 represents a power island within the integrated circuit,

including a second power island with a third power consumption in block 30, and see, e.g., column 6, line 63 to column 7, line 19, describing that the third power manager manages the power consumption of the block); and

ii) communicating with the first power manager (see, e.g., Inoue at column 6, line 63 to column 7, line 19, describing that the third power manager communicates with the first power manager).

Claim 61

Inoue in view of Silvester and Nicol further teaches or suggests the method of claim 60, wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers (see, e.g., Inoue at FIG. 1 and column 6, lines 56-62).

28. Claims 46 and 58 are rejected under pre-AIA 35 U.S.C. § 103(a) as unpatentable over Inoue in view of Silvester and Nicol and further in view of Altmejd.

Claim 46

Inoue in view of Silvester and Nicol teaches or suggests the system of claim [40], but does not expressly disclose the limitation wherein the source voltage of the first power island is provided by an external regulator.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue such that the source voltage of the first power island is provided by an external regulator with predictable results and with no change in function. For example, in an analogous art, Altmejd teaches managing the power consumption of functional blocks within an integrated circuit (see, e.g., column 1, line 62 to column 2, line 6). Altmejd expressly discloses a regulated

supply voltage that is "supplied externally by a voltage regulator" such as known in the art (see, e.g., column 5, lines 27-29). Thus, a system such as claimed would have been obvious to those of ordinary skill in the art.

Claim 58

Inoue in view of Silvester and Nicol teaches or suggests the method of claim 52, but does not expressly disclose providing external regulation for the source voltage of the first power island.

Nonetheless, a person of ordinary skill in the art could have implemented the teachings of Inoue so as to provide external regulation for the source voltage of the first power island with predictable results and with no change in function. For example, in an analogous art, Altmejd teaches managing the power consumption of functional blocks within an integrated circuit (see, e.g., column 1, line 62 to column 2, line 6). Altmejd expressly discloses a regulated supply voltage that is "supplied externally by a voltage regulator" such as known in the art (see, e.g., column 5, lines 27-29). Thus, a method such as claimed would have been obvious to those of ordinary skill in the art.

Conclusion

29. Applicant is reminded that any subsequent amendment to the specification and/or claims must comply with 37 CFR 1.173.

30. Applicant is reminded of the continuing obligation under 37 CFR 1.178(b) to timely apprise the Office of any prior or concurrent proceeding in which the '923 patent is or was involved. These proceedings would include any trial at the Patent Trial and Appeal Board, interferences, reissues, reexaminations, supplemental examinations and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56 to timely apprise the Office of any information that is material to patentability of the claims under consideration in the present reissue application.

These obligations rest with each individual associated with the filing and prosecution of the present application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall, whose telephone number is 571-272-3707. If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Hetul Patel, is reachable at 571-272-4184. The fax phone number for the organization where this application or proceeding is assigned is 571-273-9900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL J. YIGDALL/
Primary Examiner, Art Unit 3992

Conferees:

/LUKE S WASSUM/
Primary Examiner, Art Unit 3992

/H.B.P/
Supervisory Patent Examiner, Art Unit 3992

Notice of References Cited	Application/Control No. 15/192,486	Applicant(s)/Patent Under Reexamination Hoberman et al.	
	Examiner Michael J Yigdall	Art Unit 3992	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6141762-A	10-2000	Nicol; Christopher J.	G06F1/3203	713/300
*	B	US-6820240-B2	11-2004	Bednar; Thomas R.	G06F17/5045	716/113
*	C	US-6895520-B1	05-2005	Altmejd; Morrie	G06F1/3203	713/324
*	D	US-6968467-B2	11-2005	Inoue; Akihiko	G06F1/3203	713/320
*	E	US-7085945-B2	08-2006	Silvester; Kelan C.	G06F1/206	713/320
	F					
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	J					
	K					
	L					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/192,486	Hoberman et al.
	Examiner	Art Unit
	Michael J Yigdall	3992

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/10/2019								
	1	✓								
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	4	✓								
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	41	✓								
	42	✓								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/192,486	Hoberman et al.
	Examiner	**Art Unit**
	Michael J Yigdall	3992

CLAIM		DATE								
Final	Original	12/10/2019								
	43	✓								
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/192,486	Hoberman et al.
	Examiner	Art Unit
	Michael J Yigdall	3992

CPC - Searched*		
Symbol	**Date**	**Examiner**
H03K 3/012	12/10/2019	MY
H02J 4/00	12/10/2019	MY
G06F 1/3296, 1/324, 1/3203	12/10/2019	MY
H01L 2924/00, 2924/0002	12/10/2019	MY
Y02D 10/172, 10/126, 50/20	12/10/2019	MY
Y10T 307/406, 307/414	12/10/2019	MY

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
H03K 3/012; H02J 4/00; G06F 1/3296, 1/324, 1/3203; H01L 2924/00, 2924/0002; Y02D 10/172, 10/126, 50/20; Y10T 307/406, 307/414 (see search history printout)	12/10/2019	MY
Review of patent file history and cited references	12/10/2019	MY
Litigation search	12/10/2019	MY
EAST text search	12/10/2019	MY
Inventor name search	12/10/2019	MY

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/192,486	Hoberman et al.
	Examiner	Art Unit
	Michael J Yigdall	3992

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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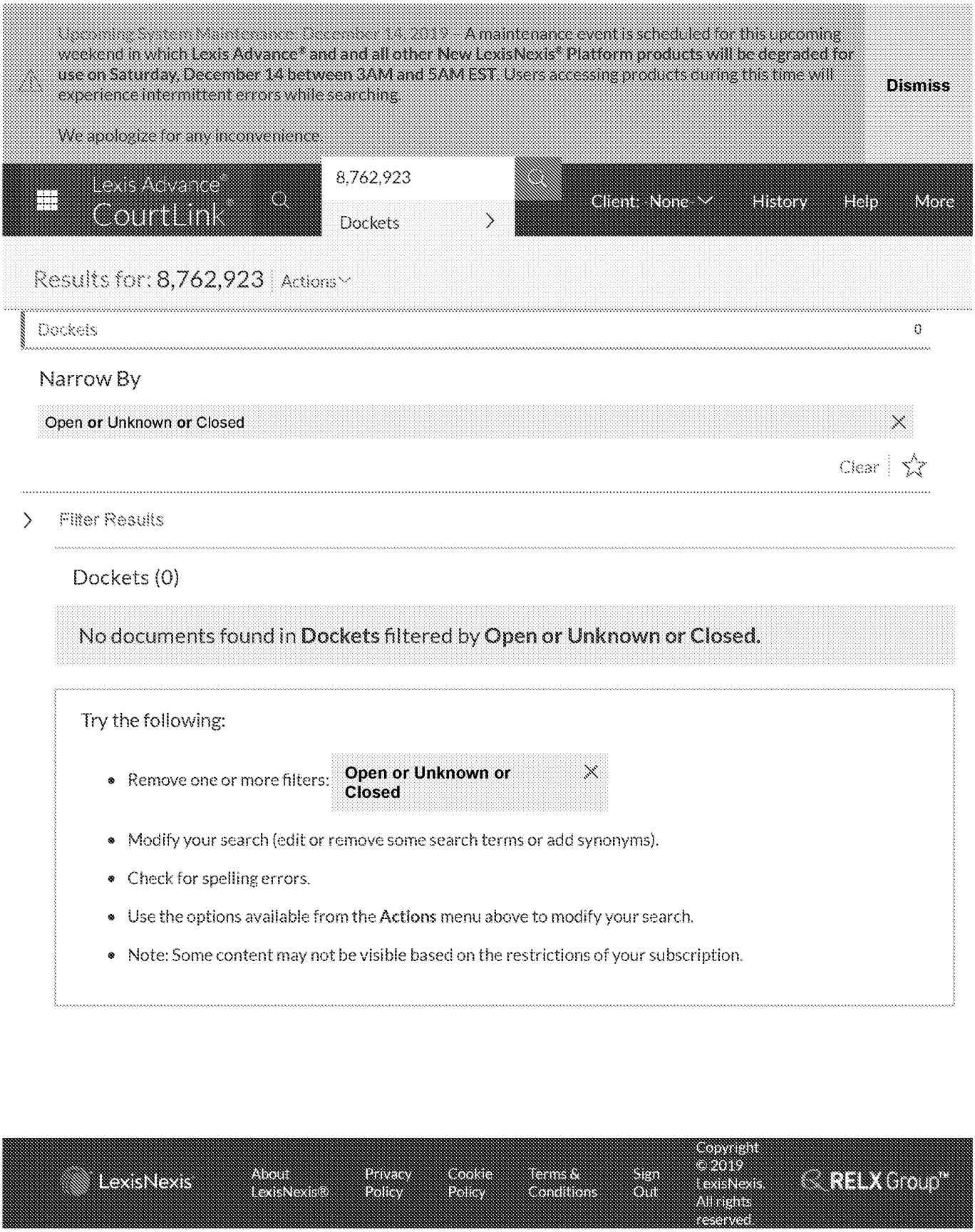
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Document: 6:12cv845, Mosaid Technologies Inc. V. St-Ericsson, Inc. Actions

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6:12cv845, Mosaid Technologies Inc. V. St-Ericsson, Inc.

US District Court Docket

US District Court for the Eastern District of TEXAS [LIVE]

(Tyler)

This case was retrieved on 12/12/2019

Header

Case Number: 6:12cv845
Date Filed: 11/05/2012
Assigned To: Judge Michael H. Schneider
Nature of Suit: Patent (830)
Cause: Patent Infringement
Lead Docket: None
Other Docket: None
Jurisdiction: Federal Question

Class Code: Closed
Closed: 10/07/2013
Statute: 35:271
Jury Demand: Both
Demand Amount: $0
NOS Description: Patent

Litigants Attorneys

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Proceedings

Retrieve Document(s)

	Availability	#	Date	Proceeding Text	Source
	Free	1	11/05/2012	COMPLAINT against ST-ERICSSON, INC (Filing fee $ 350 receipt number 0540-3860047.), filed by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A-G, # 2 Civil Cover Sheet)(Capshaw, Sidney) (Entered: 11/05/2012)	
	Online	2	11/05/2012	Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (Capshaw, Sidney) (Entered: 11/05/2012)	

	Availability	#	Date	Proceeding Text	Source
	Online	3	11/05/2012	CORPORATE DISCLOSURE STATEMENT filed by Mosaid Technologies Inc. (Capshaw, Sidney) (Entered: 11/05/2012)	
	Runner		11/05/2012	Judge Leonard Davis added. (mll,) (Entered: 11/06/2012)	
	Online	4	01/15/2013	Order reassigning this case to United States District Judge Michael H. Schneider per General Order 13-3. Please see Appendix D: Addendum Regarding Cases Assigned to Judge Schneider. Judge Leonard Davis no longer assigned to the case. (mjc,) (Entered: 01/15/2013)	
	Free	5	02/27/2013	AMENDED COMPLAINT for Patent Infringement against Mosaid Technologies Inc., filed by Mosaid Technologies Inc..(DeRieux, Elizabeth) (Entered: 02/27/2013)	
	Online	6	02/27/2013	ORDER for Plaintiff to file a notice of readiness for scheduling conference. Signed by Judge Michael H. Schneider on 2/27/2013. (gsg) (Entered: 02/28/2013)	
	Free	7	02/28/2013	SUMMONS Issued as to ST-ERICSSON, INC. and emailed to pltf for service. (klb) (Entered: 02/28/2013)	
	Free	8	03/19/2013	Defendant's Unopposed First Application for Extension of Time to Answer Complaint re ST-ERICSSON, INC..(Dacus, Deron) (Entered: 03/19/2013)	
	Online	9	04/02/2013	SUMMONS Returned Executed by Mosaid Technologies Inc. ST-ERICSSON, INC. served on 2/28/2013, answer due 3/21/2013. (mjc,) (Entered: 04/04/2013)	
	Runner		04/05/2013	Defendant's Unopposed First Application for Extension of Time to Answer Complaint is granted pursuant to Local Rule CV-12 for ST-ERICSSON, INC. to 5/6/2013. 45 Days Granted for Deadline Extension.(gsg) (Entered: 04/05/2013)	
	Online	10	05/03/2013	NOTICE of Attorney Appearance by David John Palmer on behalf of ST-ERICSSON, INC. (Palmer, David) (Entered: 05/03/2013)	
	Online	11	05/03/2013	NOTICE of Attorney Appearance by Kelly Dean Hine on behalf of ST-ERICSSON, INC. (Hine, Kelly) (Entered: 05/03/2013)	
	Online	12	05/03/2013	Agreed MOTION for Extension of Time to File Answer (Second Request) by ST-ERICSSON, INC.. (Attachments: # 1 Exhibit A, # 2 Text of Proposed Order Proposed Order)(Palmer, David) (Entered: 05/03/2013)	
	Online	13	05/06/2013	NOTICE of Attorney Appearance - Pro Hac Vice by Chad S Campbell on behalf of ST-ERICSSON, INC.. Filing fee $ 100, receipt number 0540-4125662. (Campbell, Chad) (Entered: 05/06/2013)	
	Online	14	05/07/2013	ORDER granting 12 Motion for Extension of Time to Answer. Defendants shall have to 6-20-2013 to respond to the Amended Complaint. Signed by Judge Michael H. Schneider on 05/07/13. (mll,) (Entered: 05/08/2013)	
	Free	15	06/20/2013	ANSWER to Complaint 5 Amended Complaint by ST-ERICSSON, INC..(Campbell, Chad) (Entered: 06/20/2013)	
	Online	16	07/03/2013	NOTICE by Mosaid Technologies Inc. of Readiness for Scheduling Conference (DeRieux, Elizabeth) (Entered: 07/03/2013)	

	Availability	#	Date	Proceeding Text	Source
	Online	17	08/09/2013	NOTICE of Attorney Appearance by Steven G Hill on behalf of Mosaid Technologies Inc. (Hill, Steven) (Entered: 08/09/2013)	
	Online	18	08/09/2013	NOTICE by Mosaid Technologies Inc. of Compliance with P.R. 3-1 and 3-2 (Hill, Steven) (Entered: 08/09/2013)	
	Online	19	08/13/2013	NOTICE of Attorney Appearance - Pro Hac Vice by Douglas R Kertscher on behalf of Mosaid Technologies Inc.. Filing fee $ 100, receipt number 0540-4263746. (Kertscher, Douglas) (Entered: 08/13/2013)	
	Online	20	08/13/2013	NOTICE of Attorney Appearance - Pro Hac Vice by Blake H Frye on behalf of Mosaid Technologies Inc.. Filing fee $ 100, receipt number 0540-4263833. (Frye, Blake) (Additional attachment(s) added on 10/2/2013: # 1 SEALED ATTACHMENT (pkb,). (Entered: 08/13/2013)	
	Online	21	08/13/2013	NOTICE of Attorney Appearance - Pro Hac Vice by Julie H Burke on behalf of Mosaid Technologies Inc.. Filing fee $ 100, receipt number 0540-4263931. (Burke, Julie) (Main Document 21 replaced on 8/13/2013) (pkb,). (Entered: 08/13/2013)	
	Online	22	08/27/2013	NOTICE by Mosaid Technologies Inc. of Further Compliance with P.R. 3-2 (Hill, Steven) (Entered: 08/27/2013)	
	Free	23	09/06/2013	MOTION for Leave to File Plaintiff Mosaid's Motionto Join Involuntary Plaintiffs and Leave to File Second Amended Complaint, and Memorandum of Law In Support by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Text of Proposed Order Proposed Order)(Kertscher, Douglas) (Entered: 09/06/2013)	
	Online	24	09/23/2013	Unopposed MOTION to Seal Document 23 MOTION for Leave to File Plaintiff Mosaid's Motionto Join Involuntary Plaintiffs and Leave to File Second Amended Complaint, and Memorandum of Law In Support (Unopposed Motion for Leave to File Exhibit A to Plaintiff Mosaid's Motion to Join Involuntary Plaintiffs and Leave to File Second Amended Complaint, and Memorandum of Law in Support (Dkt. 23) Under Seal) by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(DeRieux, Elizabeth) (Entered: 09/23/2013)	
	Free	25	09/23/2013	RESPONSE to Motion re 23 MOTION for Leave to File Plaintiff Mosaid's Motionto Join Involuntary Plaintiffs and Leave to File Second Amended Complaint, and Memorandum of Law In Support filed by ST-ERICSSON, INC.. (Campbell, Chad) (Entered: 09/23/2013)	
	Free	26	10/01/2013	Agreed MOTION to Dismiss with Prejudice by Mosaid Technologies Inc., ST-ERICSSON, INC.. (Attachments: # 1 Text of Proposed Order)(Kertscher, Douglas) (Additional attachment(s) added on 10/3/2013: # 2 Corrected Proposed Order) (pgo,). (Entered: 10/01/2013)	
	Online	27	10/07/2013	ORDER granting 26 Motion to Dismiss. All claims asserted by Plaintiff MOSAID in this action are hereby dismissed with prejudice. All attorneys' fees and costs are to be borne by the party that incurred them. Signed by Judge Michael H. Schneider on 10/07/13. (mll,) (Entered: 10/07/2013)	

	Availability	#	Date	Proceeding Text	Source
	Free	28	10/07/2013	FINAL JUDGMENT. All relief not previously granted is DENIED. Signed by Judge Michael H. Schneider on 10/07/13. (mll,) (Entered: 10/07/2013)	

Retrieve Document(s)

Patents

Number	Title	Issued	Class	Subclass
7,051,306	Managing power on integrated circuits using power islands	05/23/2006	716	127
5,577,230	Apparatus and method for computer processing using an enhanced Harvard architecture utilizing dual memory buses and the arbitration for data/instruction fetch	11/19/1996	711	150
5,724,505	Apparatus and method for real-time program monitoring via a serial interface	03/03/1998	714	45
5,958,036	Circuit for arbitrating interrupts with programmable priority levels	09/28/1999	710	262
6,256,725	Shared datapath processor utilizing stack-based and register-based storage spaces	07/03/2001	712	200
7,945,885	Power managers for an integrated circuit	05/17/2011	716	133
7,996,811	Power managers for an integrated circuit	08/09/2011	716	133

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2:15cv281, Conversant Intellectual Property Management, Inc. Et Al V. Samsung Electronics Co., Ltd. Et Al

US District Court Docket

US District Court for the Eastern District of TEXAS [LIVE]

(Marshall)

This case was retrieved on 12/12/2019

Header

Case Number: 2:15cv281
Date Filed: 02/26/2015
Assigned To: Judge Rodney Gilstrap
Referred To: Magistrate Judge Roy S. Payne
Nature of Suit: Patent (830)
Cause: Patent Infringement
Lead Docket: None
Other Docket: None
Jurisdiction: Federal Question

Class Code: Closed
Closed: 06/16/2015
Statute: 35:271
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

Litigants

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Defendant

Samsung Electronics America, Inc.
Defendant

Samsung Telecommunications America, LLC
Defendant

Samsung Semiconductor, Inc.
Defendant

Samsung Austin Semiconductor, LLC
Defendant

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Proceedings

#	Date	Proceeding Text	Source
1	02/26/2015	COMPLAINT against Samsung Austin Semiconductor, LLC, Samsung Electronics America, Inc., Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Samsung Telecommunications America, LLC (Filing fee $ 400 receipt number 0540-5075329.), filed by Conversant Intellectual Property Management, Inc., Conversant IP NB 868 Inc.. (Attachments: # 1 Civil Cover Sheet)(Hill, Jack) (Entered: 02/26/2015)	
	02/26/2015	Case assigned to Judge Rodney Gilstrap. (ch,) (Entered: 02/26/2015)	
2	02/26/2015	ORDER REFERRING CASE to Magistrate Judge Roy S. Payne. Signed by Judge Rodney Gilstrap on 2/26/2015. (ch,) (Entered: 02/26/2015)	
	02/26/2015	In accordance with the provisions of 28 USC Section 636(c), you are hereby notified that a U.S. Magistrate Judge of this district court is available to conduct any or all proceedings in this case including a jury or non-jury trial and to order the entry of a final judgment. The form Consent to Proceed Before Magistrate Judge is available on our website. All signed consent forms, excluding pro se parties, should be filed electronically using the event Notice Regarding Consent to Proceed Before Magistrate Judge. (ch,) (Entered: 02/26/2015)	
3	02/27/2015	DEMAND for Trial by Jury by Conversant IP NB 868 Inc., Conversant Intellectual Property Management, Inc.. (Hill, Jack) (Entered: 02/27/2015)	
4	02/27/2015	***FILED IN ERROR PER ATTORNEY***Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (Hill, Jack) Modified on 2/27/2015 (ch,). (Entered: 02/27/2015)	
5	02/27/2015	Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (Hill, Jack) (Entered: 02/27/2015)	
	02/27/2015	***FILED IN ERROR. PER ATTORNEY Document # 4, 4.	

#	Date	Proceeding Text	Source
		PLEASE IGNORE.*** (ch,) (Entered: 02/27/2015)	
6	02/27/2015	SUMMONS Issued as to Samsung Austin Semiconductor, LLC (Attachments: # 1 Samsung Electronics America Inc, # 2 Samsung Electronics Co Ltd, # 3 Samsung Semiconductor Inc, # 4 Samsung Telecommunications Amerca LLC)(ch,) (Entered: 02/27/2015)	
7	03/02/2015	NOTICE of Attorney Appearance - Pro Hac Vice by Bryan J Vogel on behalf of All Plaintiffs. Filing fee $ 100, receipt number 0540-5080637. (Vogel, Bryan) (Entered: 03/02/2015)	
8	03/02/2015	CORPORATE DISCLOSURE STATEMENT filed by Conversant IP NB 868 Inc., Conversant Intellectual Property Management, Inc. identifying Corporate Parent 7577800 Canada Inc. for Conversant Intellectual Property Management, Inc.; Corporate Parent Conversant Intellectual Property Management, Inc. for Conversant IP NB 868 Inc.. (Hill, Jack) (Entered: 03/02/2015)	
9	06/11/2015	NOTICE of Voluntary Dismissal by Conversant IP NB 868 Inc., Conversant Intellectual Property Management, Inc. (Attachments: # 1 Text of Proposed Order)(Hill, Jack) (Entered: 06/11/2015)	
10	06/16/2015	ORDER DISMISSING CASE without prejudice. Signed by Magistrate Judge Roy S. Payne on 6/14/16. (ch,) (Entered: 06/16/2015)	

Patents

Number	Title	Issued	Class	Subclass
6,223,331	Semiconductor circuit design method for employing spacing constraints and circuits thereof	04/24/2001	438	128
7,915,933	Circuit for clamping current in a charge pump	03/29/2011	327	157
7,940,081	Low leakage and data retention circuitry	05/10/2011	326	38
7,945,885	Power managers for an integrated circuit	05/17/2011	716	133
7,982,532	Systems and methods for minimizing static leakage of an integrated circuit	07/19/2011	327	544
7,996,811	Power managers for an integrated circuit	08/09/2011	716	133
8,253,438	Low leakage and data retention circuitry	08/28/2012	326	27
RE44,218	Semiconductor memory device for controlling write recovery time	05/14/2013	365	203
5,796,675	Synchronous memory device having dual input registers of pipeline structure in data path	08/18/1998	365	230.08
6,107,138	Method for fabricating a semiconductor device having a tapered contact hole	08/22/2000	438	254
6,209,056	Semiconductor memory device having a plurality of bank sections distributed in a plurality of divided memory cell arrays	03/27/2001	711	5
6,306,743	Method for forming a gate electrode on a semiconductor substrate	10/23/2001	438	592
6,313,029	Method for forming multi-layer interconnection of a semiconductor device	11/06/2001	438	637
6,943,602	Delay locked loop and locking method thereof	09/13/2005	327	158
7,101,791	Method for forming conductive line of semiconductor device	09/05/2006	438	664

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End of Document

Upcoming System Maintenance: December 14, 2019 - A maintenance event is scheduled for this upcoming weekend in which Lexis Advance® and and all other New LexisNexis® Platform products will be degraded for use on Saturday, December 14 between 3AM and 5AM EST. Users accessing products during this time will experience intermittent errors while searching.

We apologize for any inconvenience.

Dismiss

Lexis Advance CourtLink

7,945,885

Dockets

Client: -None- History Help More

Document: 2:15cv281, Conversant Intellectual Property Management, Inc. Et Al V. Sams... Actions

Go to

1 of 2 Results list

2:15cv281, Conversant Intellectual Property Management, Inc. Et Al V. Samsung Electronics Co., Ltd. Et Al

US District Court Docket

US District Court for the Eastern District of TEXAS (LIVE)

(Marshall)

This case was retrieved on 12/12/2019

Header

Case Number: 2:15cv281
Date Filed: 02/26/2015
Assigned To: Judge Rodney Gilstrap
Referred To: Magistrate Judge Roy S. Payne
Nature of Suit: Patent (830)
Cause: Patent Infringement
Lead Docket: None
Other Docket: None
Jurisdiction: Federal Question

Class Code: Closed
Closed: 06/16/2015
Statute: 35:271
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

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Litigants

Conversant IP NB 868 Inc.
Plaintiff

Samsung Electronics Co., Ltd.
Defendant

Samsung Electronics America, Inc.
Defendant

Samsung Telecommunications America, LLC
Defendant

Samsung Semiconductor, Inc.
Defendant

Samsung Austin Semiconductor, LLC
Defendant

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Proceedings

Retrieve Document(s)

	Availability	#	Date	Proceeding Text	Source
	Free	1	02/26/2015	COMPLAINT against Samsung Austin Semiconductor, LLC, Samsung Electronics America, Inc., Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Samsung Telecommunications America, LLC (Filing fee $ 400 receipt number 0540-5075329.), filed by Conversant Intellectual Property Management, Inc., Conversant IP NB 868 Inc.. (Attachments: # 1 Civil Cover Sheet). (Hill, Jack) (Entered: 02/26/2015)	
	Runner		02/26/2015	Case assigned to Judge Rodney Gilstrap. (ch,) (Entered: 02/26/2015)	
	Online	2	02/26/2015	ORDER REFERRING CASE to Magistrate Judge Roy S. Payne. Signed by Judge Rodney Gilstrap on 2/26/2015. (ch,) (Entered: 02/26/2015)	
	Runner		02/26/2015	In accordance with the provisions of 28 USC Section 636(c), you are hereby notified that a U.S. Magistrate Judge of this district court is available to conduct any or all proceedings in this case including a jury or non-jury trial and to order the entry of a final judgment. The form Consent to Proceed Before Magistrate Judge is available on our website. All signed consent forms, excluding pro se parties, should be filed electronically using the event Notice Regarding Consent to Proceed Before Magistrate Judge. (ch,) (Entered: 02/26/2015)	
	Online	3	02/27/2015	DEMAND for Trial by Jury by Conversant IP NB 868 Inc., Conversant Intellectual Property Management, Inc.. (Hill, Jack) (Entered: 02/27/2015)	

	Availability	#	Date	Proceeding Text	Source
	Online	4	02/27/2015	***FILED IN ERROR PER ATTORNEY***Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office (Hill, Jack) Modified on 2/27/2015 (ch,). (Entered: 02/27/2015)	
	Online	5	02/27/2015	Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (Hill, Jack) (Entered: 02/27/2015)	
	Runner		02/27/2015	***FILED IN ERROR. PER ATTORNEY Document # 4, 4. PLEASE IGNORE.*** (ch,) (Entered: 02/27/2015)	
	Online	6	02/27/2015	SUMMONS Issued as to Samsung Austin Semiconductor, LLC (Attachments: # 1 Samsung Electronics America Inc, # 2 Samsung Electronics Co Ltd, # 3 Samsung Semiconductor Inc, # 4 Samsung Telecommunications America LLC)(ch,) (Entered: 02/27/2015)	
	Online	7	03/02/2015	NOTICE of Attorney Appearance - Pro Hac Vice by Bryan J Vogel on behalf of All Plaintiffs. Filing fee $ 100, receipt number 0540-5080637. (Vogel, Bryan) (Entered: 03/02/2015)	
	Online	8	03/02/2015	CORPORATE DISCLOSURE STATEMENT filed by Conversant IP NB 868 Inc., Conversant Intellectual Property Management, Inc. identifying Corporate Parent 7577800 Canada Inc. for Conversant Intellectual Property Management, Inc.; Corporate Parent Conversant Intellectual Property Management, Inc. for Conversant IP NB 868 Inc.. (Hill, Jack) (Entered: 03/02/2015)	
	Free	9	06/11/2015	NOTICE of Voluntary Dismissal by Conversant IP NB 868 Inc., Conversant Intellectual Property Management, Inc. (Attachments: # 1 Text of Proposed Order)(Hill, Jack) (Entered: 06/11/2015)	
	Free	10	06/16/2015	ORDER DISMISSING CASE without prejudice. Signed by Magistrate Judge Roy S. Payne on 6/14/16. (ch,) (Entered: 06/16/2015)	

Retrieve Document(s)

Patents

Number	Title	Issued	Class	Subclass
6,223,331	Semiconductor circuit design method for employing spacing constraints and circuits thereof	04/24/2001	438	128
7,915,933	Circuit for clamping current in a charge pump	03/29/2011	327	157
7,940,081	Low leakage and data retention circuitry	05/10/2011	326	38
7,945,885	Power managers for an integrated circuit	05/17/2011	716	133
7,982,532	Systems and methods for minimizing static leakage of an integrated circuit	07/19/2011	327	544
7,996,811	Power managers for an integrated circuit	08/09/2011	716	133
8,253,438	Low leakage and data retention circuitry	08/28/2012	326	27
RE44,218	Semiconductor memory device for controlling write recovery time	05/14/2013	365	203
5,796,675	Synchronous memory device having dual input registers of pipeline structure in data path	08/18/1998	365	230.08
6,107,138	Method for fabricating a semiconductor device having a tapered contact hole	08/22/2000	438	254
6,209,056	Semiconductor memory device having a plurality of bank sections distributed in a plurality of divided memory cell arrays	03/27/2001	711	5
6,306,743	Method for forming a gate electrode on a semiconductor substrate	10/23/2001	438	592
6,313,029	Method for forming multi-layer interconnection of a semiconductor device	11/06/2001	438	637
6,943,602	Delay locked loop and locking method thereof	09/13/2005	327	158
7,101,791	Method for forming conductive line of semiconductor device	09/05/2006	438	664

3:11cv3869, Arm Ltd. Et Al V. Mosaid Technologies, Inc.

US District Court Docket

US District Court for the California Northern District

(San Francisco)

This case was retrieved on 12/12/2019

Header

Case Number: 3:11cv3869
Date Filed: 08/05/2011
Assigned To: Honorable Charles R. Breyer
Nature of Suit: Patent (830)
Cause: Fed. Question
Lead Docket: None
Other Docket: None
Jurisdiction: Federal Question

Class Code: Closed
Closed: 01/04/2012
Statute: 28:1331
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

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MOSAID Technologies, Inc. **Defendant**	Kevin E Cadwell LEAD ATTORNEY;ATTORNEY TO BE NOTICED Kelley Drye & Warren LLP 515 Post Oak Blvd Suite 900 Houston, TX 77027

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Proceedings

#	Date	Proceeding Text	Source
1	08/05/2011	COMPLAINT against MOSAID Technologies, Inc. (Filing fee $ 350, receipt number 34611063096.). Filed byARM, Inc., ARM Ltd.. (Attachments: # 1 Civil Cover Sheet)(vlk, COURT STAFF) (Filed on 8/5/2011) (Entered: 08/10/2011)	
	08/05/2011	CASE DESIGNATED for Electronic Filing. (vlk, COURT STAFF) (Filed on 8/5/2011) (Entered: 08/10/2011)	
2	08/05/2011	Summons Issued as to MOSAID Technologies, Inc.. (vlk, COURT STAFF) (Filed on 8/5/2011) (Entered: 08/10/2011)	
3	08/05/2011	Initial Disclosures by ARM Ltd., ARM, Inc. (vlk, COURT STAFF) (Filed on 8/5/2011) (Entered: 08/10/2011)	
4	08/05/2011	ADR SCHEDULING ORDER: Case Management Statement due by 11/9/2011. Case Management Conference set for 11/16/2011 01:30 PM. (Attachments: # 1 Standing Order)(vlk, COURT STAFF) (Filed on 8/5/2011) (Entered: 08/10/2011)	
5	08/10/2011	NOTICE of Appearance by Dirk van Ausdall (van Ausdall, Dirk) (Filed on 8/10/2011) (Entered: 08/10/2011)	
6	08/16/2011	MOTION of Karin Hessler for leave to appear in Pro Hac Vice (Filing fee $ 275, receipt number 44611007457.) filed by ARM Ltd., ARM, Inc.. (Attachments: # 1 Proposed Order)(vlk, COURT STAFF) (Filed on 8/16/2011) (Entered: 08/17/2011)	

#	Date	Proceeding Text	Source
7	08/16/2011	MOTION of Kevin Anderson for leave to appear in Pro Hac Vice (Filing fee $ 275, receipt number 44611007456.) filed by ARM Ltd., ARM, Inc.. (Attachments: # 1 Proposed Order)(vlk, COURT STAFF) (Filed on 8/16/2011) (Entered: 08/17/2011)	
8	08/17/2011	ORDER granting 6 Karin Hessler's Motion for Admission Pro Hac Vice by Magistrate Judge Donna M. Ryu (ig, COURT STAFF) (Filed on 8/17/2011) (Entered: 08/18/2011)	
9	08/17/2011	ORDER granting 7 Kevin Anderson's Motion for Admission Pro Hac Vice by Magistrate Judge Donna M. Ryu (ig, COURT STAFF) (Filed on 8/17/2011) (Entered: 08/18/2011)	
10	08/26/2011	AMENDED COMPLAINT for Declaratory Judgment with Jury Demand, against MOSAID Technologies, Inc.. Filed by ARM, Inc., ARM Ltd.. (Anderson, Kevin) (Filed on 8/26/2011) Modified on 8/29/2011 (jlm, COURT STAFF). (Entered: 08/26/2011)	
11	08/26/2011	STIPULATION to Extend Time for Mosaid to Respond to First Amended Complaint, filed by ARM Ltd., ARM, Inc., (Attachments: # 1 Proposed Order)(Anderson, Kevin) (Filed on 8/26/2011) Modified on 8/29/2011 (jlm, COURT STAFF). (Entered: 08/26/2011)	
12	08/26/2011	ORDER ADOPTING STIPULATION TO EXTEND TIME for MOSAID Technologies, Inc. to Respond to Amended Complaint. Responsive pleading due by 10/10/11. Signed by Magistrate Judge Donna M. Ryu, on 8/26/2011. (dmrlc2, COURT STAFF) (Filed on 8/26/2011) Modified on 8/29/2011 (jlm, COURT STAFF). (Entered: 08/26/2011)	
13	09/30/2011	NOTICE of Appearance by Jon Vensel Swenson for MOSAID Technologies, Inc. (Swenson, Jon) (Filed on 9/30/2011) (Entered: 09/30/2011)	
14	09/30/2011	NOTICE of Appearance by Kevin E Cadwell for MOSAID Technologies, Inc. (Cadwell, Kevin) (Filed on 9/30/2011) (Entered: 09/30/2011)	
15	09/30/2011	Declination to Proceed Before a U.S. Magistrate Judge by MOSAID Technologies, Inc.. (Cadwell, Kevin) (Filed on 9/30/2011) (Entered: 09/30/2011)	
16	10/03/2011	CLERK'S NOTICE of Impending Reassignment to U.S. District Judge (vlk, COURT STAFF) (Filed on 10/3/2011) (Entered: 10/03/2011)	
17	10/04/2011	ORDER REASSIGNING CASE. Case reassigned to Judge Hon. Charles R. Breyer for all further proceedings. Magistrate Judge Donna M. Ryu no longer assigned to the case. Signed by the Executive Committee on October 4, 2011. (cjl, COURT STAFF) (Filed on 10/4/2011) (Entered: 10/04/2011)	
18	10/10/2011	MOTION to Dismiss MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative, MOTION to Transfer Case filed by MOSAID Technologies, Inc.. Motion Hearing set for 12/9/2011 10:00 AM in Courtroom 6, 17th Floor, San Francisco before Hon. Charles R. Breyer. Responses due by 10/24/2011. Replies due by 10/31/2011. (Attachments: # 1 Proposed Order)(Cadwell, Kevin) (Filed on 10/10/2011) (Entered: 10/10/2011)	
19	10/10/2011	Declaration of Kevin E. Cadwell In Support of MOSAID Technologies Inc.'s Motion to Dismiss or in the Alternative Motion to Transfer filed byMOSAID Technologies, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Exhibit N)(Cadwell, Kevin) (Filed on 10/10/2011) (Entered: 10/10/2011)	

#	Date	Proceeding Text	Source
20	10/24/2011	RESPONSE (re 18 MOTION to Dismiss MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative MOTION to Transfer Case) filed byARM Ltd., ARM, Inc.. (Attachments: # 1 Proposed Order)(King, Edward) (Filed on 10/24/2011) (Entered: 10/24/2011)	
21	10/24/2011	RESPONSE (re 18 MOTION to Transfer MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative MOTION to Transfer Case) (Opposition to Motion to Transfer) filed byARM Ltd., ARM, Inc. (Attachments: # 1 Proposed Order)(King, Edward) (Filed on 10/24/2011) Modified on 10/25/2011 (mcl, COURT STAFF). (Entered: 10/24/2011)	
22	10/24/2011	DECLARATION of Kevin P. Anderson in Opposition to 18 Motion to Dismiss, Motion to Transfer, filed byARM Ltd., ARM, Inc. (Attachments: # 1 Exhibit A1, # 2 Exhibit A2, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F1, # 8 Exhibit F2, # 9 Exhibit F3, # 10 Exhibit F4, # 11 Exhibit F5, # 12 Exhibit F6, # 13 Exhibit F7, # 14 Exhibit F8, # 15 Exhibit F9, # 16 Exhibit F10, # 17 Exhibit F11, # 18 Exhibit F12, # 19 Exhibit F13, # 20 Exhibit F14, # 21 Exhibit F15, # 22 Exhibit F16, # 23 Exhibit F17, # 24 Exhibit F18, # 25 Exhibit G, # 26 Exhibit H, # 27 Exhibit I, # 28 Exhibit J, # 29 Exhibit K, # 30 Exhibit L, # 31 Exhibit M, # 32 Exhibit N, # 33 Exhibit O, # 34 Exhibit P, # 35 Exhibit Q, # 36 Exhibit R, # 37 Exhibit S)(Related document(s) 20 , 21) (King, Edward) (Filed on 10/24/2011) Modified on 10/25/2011 (mcl, COURT STAFF). (Entered: 10/24/2011)	
23	10/26/2011	CLERKS NOTICE Initial Case Management Conference set for 12/9/2011 10:00 AM in Courtroom 6, 17th Floor, San Francisco. (Attachments: # 1 Standing Order) (beS, COURT STAFF) (Filed on 10/26/2011) (Entered: 10/26/2011)	
24	10/28/2011	MOTION for leave to appear in Pro Hac Vice (Kurt M. Pankratz) (Filing fee $ 275, receipt number 34611066334.) filed by MOSAID Technologies, Inc. (Attachments: # 1 Proposed Order)(mcl, COURT STAFF) (Filed on 10/28/2011) (Entered: 10/28/2011)	
25	10/31/2011	Administrative Motion to File Under Seal Exhibit R to the Declaration of Kevin Cadwell in Support of MOSAID Technologies, Inc.'s Reply in Support of its Motion to Dismiss or in the Alternative Motion to Transfer filed by MOSAID Technologies, Inc.. (Attachments: # 1 Declaration, # 2 Proposed Order)(Cadwell, Kevin) (Filed on 10/31/2011) (Entered: 10/31/2011)	
26	10/31/2011	REPLY (re 18 MOTION to Dismiss MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative MOTION to Transfer Case) filed byMOSAID Technologies, Inc.. (Cadwell, Kevin) (Filed on 10/31/2011) (Entered: 10/31/2011)	
27	10/31/2011	Declaration of Kevin E. Cadwell in Support of 26 Reply to Opposition/Response in Support of Motion to Dismiss or in the Alternative Motion to Transfer filed byMOSAID Technologies, Inc.. (Attachments: # 1 Exhibit O, # 2 Exhibit P, # 3 Exhibit Q)(Related document(s) 26) (Cadwell, Kevin) (Filed on 10/31/2011) (Entered: 10/31/2011)	
28	10/31/2011	MOTION for leave to appear in Pro Hac Vice (David M. Schlitz) (Filing fee $ 275, receipt number 34611066441.) filed by MOSAID Technologies, Inc. (Attachments: # 1 Proposed Order)(mcl, COURT STAFF) (Filed on 10/31/2011) (Entered: 11/01/2011)	
29	11/07/2011	ORDER by Judge Charles R. Breyer granting 28 Motion for Pro Hac Vice (D M Schlitz) (beS, COURT STAFF) (Filed on 11/7/2011) (Entered: 11/07/2011)	
30	11/07/2011	ORDER by Judge Charles R. Breyer granting 24 Motion for Pro Hac Vice (K M Pankratz) (beS, COURT STAFF) (Filed on 11/7/2011) (Entered: 11/07/2011)	

#	Date	Proceeding Text	Source
31	12/02/2011	CASE MANAGEMENT STATEMENT (JOINT); RULE 26(f) REPORT filed by ARM Ltd., ARM, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(King, Edward) (Filed on 12/2/2011) (Entered: 12/02/2011)	
32	12/09/2011	Minute Entry: Motion Hearing held on 12/9/2011 before Charles R. Breyer (Date Filed: 12/9/2011) re 18 MOTION to Dismiss MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative MOTION to Transfer Case filed by MOSAID Technologies, Inc.. (Court Reporter Belle Ball.) (beS, COURT STAFF) (Date Filed: 12/9/2011) (Entered: 12/13/2011)	
33	01/04/2012	ORDER by Judge Charles R. Breyer granting 18 Motion to Transfer Case. (crblc1, COURT STAFF) (Filed on 1/4/2012) (Entered: 01/04/2012)	
	01/05/2012	Case transferred to U.S. District Court, Eastern District of Texas via ECF. (mcl, COURT STAFF) (Entered: 01/09/2012)	
	01/09/2012	Receipt for new case number in Eastern District of Texas via ECF - 6:12-cv-00008. (mcl, COURT STAFF) (Entered: 01/09/2012)	
34	04/11/2012	Transcript of Proceedings held on December 9, 2011, before Judge Charles R. Breyer. Court Reporter/Transcriber Belle Ball, CSR, RMR, CRR, Telephone number (415)373-2529, belle_ball@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 7/10/2012. (Ball, Belle) (Filed on 4/11/2012) (Entered: 04/11/2012)	

Patents

Number	Title	Issued	Class	Subclass
5,577,230	Apparatus and method for computer processing using an enhanced Harvard architecture utilizing dual memory buses and the arbitration for data/instruction fetch	11/19/1996	711	150
5,724,505	Apparatus and method for real-time program monitoring via a serial interface	03/03/1998	714	45
5,958,036	Circuit for arbitrating interrupts with programmable priority levels	09/28/1999	710	262
6,141,762	Power reduction in a multiprocessor digital signal processor based on processor load	10/31/2000	713	300
6,256,725	Shared datapath processor utilizing stack-based and register-based storage spaces	07/03/2001	712	200
7,415,680	Power managers for an integrated circuit	08/19/2008	716	133
7,051,306	Managing power on integrated circuits using power islands	05/23/2006	716	127

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*** THIS DATA IS FOR INFORMATIONAL PURPOSES ONLY ***

6:11cv173, Mosaid Technologies Inc. V. Freescale Semiconductor, Inc. Et Al

US District Court Docket

US District Court for the Eastern District of TEXAS [LIVE]

(Tyler)

This case was retrieved on 12/12/2019

Header

Case Number: 6:11cv173
Date Filed: 04/07/2011
Assigned To: Judge Michael H. Schneider
Nature of Suit: Patent (830)
Cause: Patent Infringement
Lead Docket: None
Other Docket: None
Jurisdiction: Federal Question

Class Code: Closed
Closed: 08/30/2013
Statute: 15:1126
Jury Demand: Both
Demand Amount: $0
NOS Description: Patent

Litigants

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Proceedings

#	Date	Proceeding Text	Source
1	04/07/2011	COMPLAINT against Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation (Filing fee $ 350 receipt number 0540-2975282.), filed by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A - '306 Patent, # 2 Exhibit B - '680 Patent, # 3 Exhibit C - '230 Patent, # 4 Exhibit D - '505 Patent, # 5 Exhibit E - '036 Patent, # 6 Exhibit F - '762 Patent, # 7 Exhibit G - '725 Patent, # 8 Civil Cover Sheet)(Schlitz, David) (Entered: 04/07/2011)	
2	04/07/2011	CORPORATE DISCLOSURE STATEMENT filed by Mosaid Technologies Inc. (Schlitz, David) (Entered: 04/07/2011)	
3	04/07/2011	Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (Schlitz, David) (Entered: 04/07/2011)	
4	04/07/2011	NOTICE of Attorney Appearance by Sidney Calvin Capshaw, III on behalf of Mosaid Technologies Inc. (Capshaw, Sidney) (Entered: 04/07/2011)	
	04/07/2011	Judge Leonard Davis added. (mll,) (Entered: 04/07/2011)	
5	04/07/2011	NOTICE of Attorney Appearance by Matthew Colagrosso on behalf of Mosaid Technologies Inc. (Colagrosso, Matthew) (Entered: 04/07/2011)	
6	04/07/2011	NOTICE of Attorney Appearance by Kurt Max Pankratz on behalf of Mosaid Technologies Inc. (Pankratz, Kurt) (Entered: 04/07/2011)	
7	04/07/2011	NOTICE of Attorney Appearance by Chad Christian Walters on behalf of Mosaid Technologies Inc. (Walters, Chad) (Entered: 04/07/2011)	
8	04/08/2011	E-GOV SEALED SUMMONS Issued as to Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation. (Attachments: # 1 Summons(es), # 2 Summons(es))(kls,) (Entered: 04/08/2011)	
9	04/15/2011	Return of Service Executed as to Interphase Corporation on 4/11/2011, by personal service; answer due: 5/2/2011. (mll,) (mll,). (Entered: 04/19/2011)	
10	04/15/2011	Return of Service Executed as to Freescale Semiconductor, Inc. on 4/11/2011, by personal service; answer due: 5/2/2011. (mll,)	

#	Date	Proceeding Text	Source
		(Entered: 04/19/2011)	
11	04/15/2011	Return of Service Executed as to NVIDIA Corporation on 4/11/2011, by personal service; answer due: 5/2/2011. (mll,) (Entered: 04/19/2011)	
12	04/21/2011	Defendant's Unopposed First Application for Extension of Time to Answer Complaint re NVIDIA Corporation.(Ainsworth, Jennifer) (Entered: 04/21/2011)	
13	04/22/2011	Defendant's Unopposed First Application for Extension of Time to Answer Complaint re Interphase Corporation.(Wright, Thomas) (Entered: 04/22/2011)	
	04/26/2011	Defendant's Unopposed First Application for Extension of Time to Answer Complaint 12 is granted pursuant to Local Rule CV-12 for NVIDIA Corporation to 6/1/2011. 30 Days Granted for Deadline Extension.(mll,) (Entered: 04/26/2011)	
	04/26/2011	Defendant's Unopposed First Application for Extension of Time to Answer Complaint 13 is granted pursuant to Local Rule CV-12 for Interphase Corporation to 6/1/2011. 30 Days Granted for Deadline Extension.(mll,) (Entered: 04/26/2011)	
14	04/27/2011	Defendant's Unopposed First Application for Extension of Time to Answer Complaint re Freescale Semiconductor, Inc..(Witcoff, David) (Entered: 04/27/2011)	
	04/29/2011	Defendant's Unopposed First Application for Extension of Time to Answer Complaint 14 is granted pursuant to Local Rule CV-12 for Freescale Semiconductor, Inc. to 6/1/2011. 30 Days Granted for Deadline Extension.(mll,) (Entered: 04/29/2011)	
15	05/25/2011	NOTICE of Attorney Appearance by David M Barkan on behalf of NVIDIA Corporation (Barkan, David) (Entered: 05/25/2011)	
16	05/26/2011	NOTICE of Attorney Appearance by David Michael Hoffman on behalf of NVIDIA Corporation (Hoffman, David) (Entered: 05/26/2011)	
17	05/31/2011	APPLICATION to Appear Pro Hac Vice by Attorney Kevin Su for NVIDIA Corporation. (mll,) (Entered: 06/01/2011)	
18	06/01/2011	ANSWER to 1 Complaint, Affirmative Defenses, COUNTERCLAIM against Mosaid Technologies Inc. by NVIDIA Corporation.(Ainsworth, Jennifer) (Entered: 06/01/2011)	
19	06/01/2011	CORPORATE DISCLOSURE STATEMENT filed by NVIDIA Corporation identifying Corporate Parent None for NVIDIA Corporation. (Ainsworth, Jennifer) (Entered: 06/01/2011)	
20	06/01/2011	NOTICE of Attorney Appearance by Emily Merkler Wood on behalf of Freescale Semiconductor, Inc. (Wood, Emily) (Entered: 06/01/2011)	
21	06/01/2011	NOTICE of Attorney Appearance by Emily Merkler Wood on behalf of Interphase Corporation (Wood, Emily) (Entered: 06/01/2011)	
22	06/01/2011	NOTICE of Attorney Appearance by Timothy J. Heverin on behalf of Freescale Semiconductor, Inc. (Heverin, Timothy) (Entered: 06/01/2011)	
23	06/01/2011	NOTICE of Attorney Appearance by Timothy J. Heverin on behalf of Interphase Corporation (Heverin, Timothy) (Entered: 06/01/2011)	
24	06/01/2011	NOTICE of Attorney Appearance by Mark Christopher Howland on behalf of Freescale Semiconductor, Inc. (Howland, Mark) (Entered: 06/01/2011)	
25	06/01/2011	NOTICE of Attorney Appearance by Mark Christopher Howland on behalf of Interphase Corporation (Howland, Mark) (Entered: 06/01/2011)	
26	06/01/2011	NOTICE of Attorney Appearance by David L. Witcoff on behalf of	

#	Date	Proceeding Text	Source
		Interphase Corporation (Witcoff, David) (Entered: 06/01/2011)	
27	06/01/2011	ANSWER to 1 Complaint,, COUNTERCLAIM against Mosaid Technologies Inc. by Freescale Semiconductor, Inc..(Witcoff, David) (Entered: 06/01/2011)	
28	06/01/2011	ANSWER to 1 Complaint,, COUNTERCLAIM against Mosaid Technologies Inc. by Interphase Corporation.(Witcoff, David) (Entered: 06/01/2011)	
29	06/01/2011	CORPORATE DISCLOSURE STATEMENT filed by Interphase Corporation (Witcoff, David) (Entered: 06/01/2011)	
30	06/03/2011	NOTICE by Mosaid Technologies Inc. of Readiness for Scheduling Conference (Capshaw, Sidney) (Entered: 06/03/2011)	
31	06/07/2011	CORPORATE DISCLOSURE STATEMENT filed by Freescale Semiconductor, Inc. identifying Corporate Parent Freescale Semiconductor Holdings V Inc, Corporate Parent Freescale Scmiconductor Holdings I Ltd, Corporate Parent Freescale Holdings LP for Freescale Semiconductor, Inc.. (Wood, Emily) (Entered: 06/07/2011)	
32	06/22/2011	ANSWER to 27 Answer to Complaint, Counterclaim (MOSAID Technologies Inc.'s Answer to Freescale Semiconductor, Inc.s Counterclaim) by Mosaid Technologies Inc..(Schlitz, David) (Entered: 06/22/2011)	
33	06/22/2011	ANSWER to 28 Answer to Complaint, Counterclaim (MOSAID Technologies Inc.'s Answer to Interphase Corporation's Counterclaim) by Mosaid Technologies Inc..(Schlitz, David) (Entered: 06/22/2011)	
34	06/22/2011	ANSWER to 18 Answer to Complaint, Counterclaim (MOSAID Technologies Inc.'s Answer to NVIDIA Corporation's Counterclaim) by Mosaid Technologies Inc..(Schlitz, David) (Entered: 06/22/2011)	
35	07/08/2011	ORDER setting Status Conference for 8/9/2011 01:30 PM before Judge Leonard Davis. Signed by Judge Leonard Davis on 07/08/11. cc:attys 7-11-11(mll,) (Entered: 07/11/2011)	
36	07/18/2011	MOTION to Seal Defendants' Motion To Dismiss Under Federal R. Civ. P. 12(b)(1) For Lack of Standing by Freescale Semiconductor, Inc.. (Attachments: # 1 Text of Proposed Order)(Witcoff, David) (Entered: 07/18/2011)	
37	07/18/2011	SEALED MOTION To Dismiss Under Fed. R. Civ. P. 12(b)(1) for Lack of Standing by Freescale Semiconductor, Inc.. (Attachments: # 1 Text of Proposed Order, # 2 Exhibit Exhibit 1, # 3 Exhibit Exhibit 2)(Witcoff, David) (Entered: 07/18/2011)	
38	07/19/2011	Unopposed MOTION to Seal (corrected) by Freescale Semiconductor, Inc.. (Attachments: # 1 Text of Proposed Order)(Wood, Emily) (Entered: 07/19/2011)	
39	07/19/2011	ORDER granting 36 Freescale's Unopposed Motion for Leave to File under Seal. Signed by Judge Leonard Davis on 7/19/2011. (kls,) (Entered: 07/19/2011)	
40	07/20/2011	ORDER granting 38 Motion to Seal Defendants Motion to Dismiss. Signed by Judge Leonard Davis on 7/20/11. (mjc,) (Entered: 07/20/2011)	
41	07/25/2011	NOTICE of Attorney Appearance by Elizabeth L DeRieux on behalf of Mosaid Technologies Inc. (DeRieux, Elizabeth) (Entered: 07/25/2011)	
42	08/04/2011	Unopposed MOTION to Seal Response to Defendants Motion To Dismiss Under Fed. R. Civ. P. 12(B)(1) by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 08/04/2011)	
43	08/04/2011	***DOCUMENT FILED IN ERROR. PLEASE DISREGARD.***SEALED RESPONSE to Motion re 37 SEALED	

#	Date	Proceeding Text	Source
		MOTION To Dismiss Under Fed. R. Civ. P. 12(b)(1) for Lack of Standing filed by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) Modified on 8/8/2011 (mjc,). (Entered: 08/04/2011)	
	08/08/2011	NOTICE of Deficiency regarding the 43 Sealed Response to Motion submitted by Mosaid Technologies Inc. Document does not contain a Certificate of Authorization to File Under Seal. Correction should be made by one business day. (mjc,) (Entered: 08/08/2011)	
44	08/08/2011	SEALED RESPONSE to Motion re 37 SEALED MOTION To Dismiss Under Fed. R. Civ. P. 12(b)(1) for Lack of Standing filed by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order Denying Motion to Dismiss)(Pankratz, Kurt) (Entered: 08/08/2011)	
48	08/09/2011	Minute Entry for proceedings held before Judge Leonard Davis: Status Conference held on 8/9/2011. (Court Reporter Shea Sloan.) (Attachments: # 1 Attorney Sign-In Sheet) (rlf,) (Entered: 08/16/2011)	
45	08/15/2011	NOTICE of Discovery Disclosure by Mosaid Technologies Inc. re P.R. 3-1 and 3-2 (DeRieux, Elizabeth) (Entered: 08/15/2011)	
46	08/15/2011	AMENDED COMPLAINT against Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation, filed by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A - 306 Patent, # 2 Exhibit B - 680 Patent, # 3 Exhibit C - 885 Patent, # 4 Exhibit D - 811 Patent, # 5 Exhibit E - 230 Patent, # 6 Exhibit F - 505 Patent, # 7 Exhibit G - 036 Patent, # 8 Exhibit H - 762 Patent, # 9 Exhibit I - 725 Patent)(DeRieux, Elizabeth) (Additional attachment(s) added on 8/17/2011: # 10 Exhibit A Searchable, # 11 Exhibit B Searchable, # 12 Exhibit C Searchable, # 13 Exhibit D Searchable, # 14 Exhibit E Searchable) (mjc,). (Additional attachment(s) added on 8/17/2011: # 15 Exhibit F Searchable, # 16 Exhibit G Searchable, # 17 Exhibit H Searchable, # 18 Exhibit I Searchable) (mjc,). (Entered: 08/15/2011)	
47	08/15/2011	Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (DeRieux, Elizabeth) (Entered: 08/15/2011)	
49	08/17/2011	ORDER - Markman Hearing set for 10/4/2012 09:00 AM in Ctrm 361 (Tyler) before Judge Leonard Davis. Final Pretrial Conference set for 8/22/2013 09:00 AM in Ctrm 361 (Tyler) before Judge Leonard Davis. Jury Selection set for 9/3/2013 09:00 AM in Ctrm 361 (Tyler) before Judge Leonard Davis. Jury Trial set for 9/9/2013 09:00 AM in Ctrm 361 (Tyler) before Judge Leonard Davis. Signed by Judge Leonard Davis on 8/16/11. (mjc,) (Entered: 08/17/2011)	
50	08/18/2011	APPLICATION to Appear Pro Hac Vice by Attorney Edward Alexander Eaton-Salners for NVIDIA Corporation (mll,) (Entered: 08/18/2011)	
51	08/19/2011	Unopposed MOTION to Seal Reply in Support of Defendant's Motion to Dismiss by Freescale Semiconductor, Inc.. (Attachments: # 1 Text of Proposed Order)(Wood, Emily) (Entered: 08/19/2011)	
52	08/19/2011	Unopposed MOTION for Leave to File Excess Pages by Freescale Semiconductor, Inc.. (Attachments: # 1 Text of Proposed Order)(Wood, Emily) (Entered: 08/19/2011)	
53	08/19/2011	SEALED REPLY to Response to Motion re 37 SEALED MOTION To Dismiss Under Fed. R. Civ. P. 12(b)(1) for Lack of Standing filed by Freescale Semiconductor, Inc.. (Wood, Emily) (Entered: 08/19/2011)	
54	08/22/2011	ORDER granting 52 Motion for Leave to File Excess Pages.	

#	Date	Proceeding Text	Source
		Signed by Judge Leonard Davis on 08/22/11. cc:attys 8-23-11 (mll,) (Entered: 08/23/2011)	
55	08/22/2011	ORDER granting 51 Motion to Seal. Defendants are granted leave to file under seal Defendants Reply In Support Of Defendants Motion to Dismiss Under Fed. R. Civ. P. 12(B)(1) for Lack of Standing. Signed by Judge Leonard Davis on 08/22/11. cc:attys 8-23-11 (mll,) (Entered: 08/23/2011)	
56	08/25/2011	NOTICE of Attorney Appearance by Edward Alexander Eaton-Salners on behalf of NVIDIA Corporation (Eaton-Salners, Edward) (Entered: 08/25/2011)	
57	08/26/2011	Agreed MOTION for Extension of Time to File Proposed Agreed Docket Control and Discovery Orders by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(DeRieux, Elizabeth) (Entered: 08/26/2011)	
58	08/29/2011	ORDER granting 57 Motion for Extension of Time. The deadline for parties to submit agreed proposed docket control and discovery orders is extended to 9-02-2011. Signed by Judge Leonard Davis on 08/29/11. cc:attys 8-29-11 (mll,) (Entered: 08/29/2011)	
59	08/29/2011	ANSWER to 46 Amended Complaint,,, Affirmative Defenses, Amended COUNTERCLAIM against Mosaid Technologies Inc. by NVIDIA Corporation.(Hoffman, David) (Entered: 08/29/2011)	
60	08/30/2011	Unopposed MOTION to Seal Sur-Reply in Opposition to Defendants Motion To Dismiss Under Fed. R. Civ. P. 12(B)(1) by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 08/30/2011)	
61	08/30/2011	Unopposed MOTION for Leave to File Excess Pages (Plaintiff MOSAID Technologies, Inc.'s Unopposed Motion to File Its Sur-Reply Exceeding Page Limits) by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 08/30/2011)	
62	08/30/2011	SEALED PATENT SUR-REPLY to Reply to Response to PATENT Motion re 37 SEALED MOTION To Dismiss Under Fed. R. Civ. P. 12(b)(1) for Lack of Standing filed by Mosaid Technologies Inc.. (Pankratz, Kurt) (Entered: 08/30/2011)	
63	08/30/2011	ORDER granting 42 Motion to Seal. Signed by Judge Leonard Davis on 08/30/11. cc:attys 8-31-11 (mll,) (Entered: 08/31/2011)	
64	08/31/2011	ORDER denying 61 Motion for Leave to File Excess Pages. MOSAID Technologies Inc. may refile its Sur-Reply in Opposition to Defendants Motion To Dismiss For Lack Of Standing in compliance with the page limits rules within one business day, otherwise the Court will only consider the Sur-Reply to the extent it complies with the local rules. Signed by Judge Leonard Davis on 08/31/11. cc:attys 8-31-11 (mll,) (Entered: 08/31/2011)	
65	08/31/2011	ORDER granting 60 Motion to Seal. Signed by Judge Leonard Davis on 08/31/11. cc:attys 8-31-11 (mll,) (Entered: 08/31/2011)	
66	09/01/2011	SEALED PATENT SUR-REPLY to Reply to Response to PATENT Motion re 37 SEALED MOTION To Dismiss Under Fed. R. Civ. P. 12(b)(1) for Lack of Standing filed by Mosaid Technologies Inc.. (Pankratz, Kurt) (Entered: 09/01/2011)	
67	09/01/2011	ANSWER to 46 Amended Complaint,,, Affirmative Defenses, Amended COUNTERCLAIM against Mosaid Technologies Inc. by Freescale Semiconductor, Inc..(Witcoff, David) (Entered: 09/01/2011)	
68	09/01/2011	ANSWER to 46 Amended Complaint,,, Affirmative Defenses, Amended COUNTERCLAIM against Mosaid Technologies Inc. by Interphase Corporation.(Witcoff, David) (Entered: 09/01/2011)	
69	09/02/2011	MOTION to Sever Defendants' Motion to Sever and Transfer to	

#	Date	Proceeding Text	Source
		the Northern District of California by Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation. (Attachments: # 1 Exhibit A to Defendants Motion to Sever, # 2 Exhibit B to Defendants Motion to Sever, # 3 Exhibit C to Defendants Motion to Sever, # 4 Exhibit D to Defendants Motion to Sever, # 5 Exhibit E to Defendants Motion to Sever, # 6 Exhibit F to Defendants Motion to Sever, # 7 Exhibit G to Defendants Motion to Sever, # 8 Exhibit H to Defendants Motion to Sever, # 9 Exhibit I to Defendants Motion to Sever, # 10 Exhibit J to Defendants Motion to Sever, # 11 Text of Proposed Order Proposed Order Granting Defendants Motion to Sever)(Eaton-Salners, Edward) (Entered: 09/02/2011)	
70	09/02/2011	Joint MOTION for Leave to File Docket Control Order and Rule on Disputed Issues in Discovery Order by Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Agreed Docket Control Order, # 2 Agreed and Disputed Discovery Order)(Pankratz, Kurt) (Entered: 09/02/2011)	
71	09/07/2011	NOTICE of Discovery Disclosure by Mosaid Technologies Inc. re Asserted Claims for '811 Patent (DeRieux, Elizabeth) (Entered: 09/07/2011)	
72	09/08/2011	ORDER re 70 Joint MOTION for Leave to File Docket Control Order and Rule on Disputed Issues in Discovery Order filed by NVIDIA Corporation, Interphase Corporation, Mosaid Technologies Inc., Freescale Semiconductor, Inc. Parties shall submit an updated proposed Discovery Order by 9-14-2011. Signed by Judge Leonard Davis on 09/08/11. cc:attys 9-09-11(mll,) (Entered: 09/09/2011)	
73	09/09/2011	JOINT DOCKET CONTROL ORDER. Signed by Judge Leonard Davis on 09/09/11. cc:attys 9-09-11(mll,) (Entered: 09/09/2011)	
	09/09/2011	Deadlines set per 73 Joint Docket Control Order: Amended Pleadings due by 7/19/2012; Respond to Amended Pleadings by 8-02-2012. Fact Discovery due by 1/7/2013; Expert Discovery due by 1-28-2013. Expert Witness List due by 11/28/2012. Identify trial witnesses by 2/1/2013; Rebuttal Trial Witnesses identified by 2-12-2013. Jury instructions due by 6/28/2013. Dispositive Motions due by 2/15/2013; Response to Dispositive Motions due 3-01-2013. Proposed Pretrial Order due by 6/28/2013. Gary McGowan is appointed as Mediator in this cause. Jury Selection set for 9/3/2013 09:00AM before Judge Leonard Davis. Jury Trial set for 9/9/2013 09:00 AM before Judge Leonard Davis. Markman Hearing set for 10/4/2012 09:30 AM before Judge Leonard Davis. Pretrial Conference set for 8/22/2013 09:00 AM before Judge Leonard Davis. (mll,) (Entered: 09/19/2011)	
	09/09/2011	CASE REFERRED to Mediator. Gary McGowan is appointed Mediator in this case. (mll,) (Entered: 09/19/2011)	
74	09/13/2011	Joint MOTION for Leave to File Discovery Order by Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Discovery Order)(Pankratz, Kurt) (Entered: 09/13/2011)	
75	09/13/2011	Unopposed MOTION for Extension of Time to File Response/Reply as to 69 MOTION to Sever Defendants' Motion to Sever and Transfer to the Northern District of California by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 09/13/2011)	
76	09/13/2011	Unopposed MOTION for Extension of Time to File Response/Reply as to 59 Answer to Amended Complaint, Counterclaim, 67 Answer to Amended Complaint, Counterclaim by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed	

#	Date	Proceeding Text	Source
		Order)(Pankratz, Kurt) (Entered: 09/13/2011)	
77	09/14/2011	ORDER granting 74 Motion for Leave to File Discovery Order and entering Discovery Order in furtherance of the management of the Court's docket. Signed by Judge Leonard Davis on 9/14/11. (mjc,) (Entered: 09/14/2011)	
78	09/14/2011	ORDER granting 75 Motion for Extension of Time to File Response/Reply re 75 Unopposed MOTION for Extension of Time to File Response/Reply as to 69 MOTION to Sever Defendants' Motion to Sever and Transfer to the Northern District of California. Responses due by 9/30/2011. Signed by Judge Leonard Davis on 9/14/11. (mjc,) (Entered: 09/14/2011)	
79	09/14/2011	ORDER granting 76 Motion for Extension of Time to File Response/Reply re 76 Unopposed MOTION for Extension of Time to File Response/Reply as to 59 Answer to Amended Complaint, Counterclaim, 67 Answer to Amended Complaint, Counterclaim. Responses due by 10/14/2011. Signed by Judge Leonard Davis on 9/14/11. (mjc,) (Entered: 09/14/2011)	
80	09/15/2011	Mosaid Technologies Inc.'s Answer to Defendant Interphase Corporation's Counterclaim ANSWER to 68 Answer to Amended Complaint, Counterclaim by Mosaid Technologies Inc..(Pankratz, Kurt) (Entered: 09/15/2011)	
81	09/19/2011	NOTICE of Discovery Disclosure by Mosaid Technologies Inc. re Infringement Contentions for '811 Patent (Pankratz, Kurt) (Entered: 09/19/2011)	
82	09/30/2011	***DOCUMENT FILED IN ERROR. PLEASE DISREGARD.***SEALED RESPONSE to Motion re 69 MOTION to Sever Defendants' Motion to Sever and Transfer to the Northern District of California filed by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Text of Proposed Order)(Pankratz, Kurt) Modified on 9/30/2011 (mjc,). (Entered: 09/30/2011)	
83	09/30/2011	RESPONSE in Opposition re 69 MOTION to Sever Defendants' Motion to Sever and Transfer to the Northern District of California filed by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Text of Proposed Order)(Pankratz, Kurt) (Entered: 09/30/2011)	
84	10/05/2011	ORDER to meet and confer and resubmit an agreed Docket Control Order incorporating letter brief deadlines. Signed by Judge Leonard Davis on 10/5/11. (mjc,) (Entered: 10/05/2011)	
85	10/06/2011	NOTICE of Discovery Disclosure by Mosaid Technologies Inc. (Pankratz, Kurt) (Entered: 10/06/2011)	
86	10/06/2011	NOTICE of Discovery Disclosure by NVIDIA Corporation (Eaton-Salners, Edward) (Entered: 10/06/2011)	
87	10/06/2011	NOTICE of Discovery Disclosure by Freescale Semiconductor, Inc. (Wood, Emily) (Entered: 10/06/2011)	
88	10/06/2011	NOTICE of Discovery Disclosure by Interphase Corporation (Wood, Emily) (Entered: 10/06/2011)	
89	10/11/2011	REPLY to Response to Motion re 69 MOTION to Sever Defendants' Motion to Sever and Transfer to the Northern District of California filed by Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Hoffman, David) (Entered: 10/11/2011)	
90	10/12/2011	First Amended ANSWER to 46 Amended Complaint,,, Affirmative	

#	Date	Proceeding Text	Source
		Defenses, COUNTERCLAIM against Mosaid Technologies Inc. by NVIDIA Corporation.(Hoffman, David) (Entered: 10/12/2011)	
91	10/13/2011	First Amended ANSWER to 46 Amended Complaint,,,, COUNTERCLAIM against Mosaid Technologies Inc. by Freescale Semiconductor, Inc..(Witcoff, David) (Entered: 10/13/2011)	
92	10/18/2011	NOTICE of Attorney Appearance by Jonathan Bell Rubenstein on behalf of Mosaid Technologies Inc. (Rubenstein, Jonathan) (Entered: 10/18/2011)	
93	10/21/2011	SUR-REPLY to Reply to Response to Motion re 69 MOTION to Sever Defendants' Motion to Sever and Transfer to the Northern District of California filed by Mosaid Technologies Inc.. (Pankratz, Kurt) (Entered: 10/21/2011)	
94	10/24/2011	NOTICE of Discovery Disclosure by NVIDIA Corporation Notice of Service of First Supplemental Initial Disclosure (Eaton-Salners, Edward) (Entered: 10/24/2011)	
95	10/24/2011	NOTICE of Discovery Disclosure by Mosaid Technologies Inc. (Plaintiff MOSAID Technologies, Inc.'s Notice of Service of Damages Disclosure) (Pankratz, Kurt) (Entered: 10/24/2011)	
96	10/24/2011	NOTICE by NVIDIA Corporation [NVIDIA Corporation's Notice of Service of Additional Disclosures] (Eaton-Salners, Edward) (Entered: 10/24/2011)	
97	10/31/2011	MOTION to Dismiss and Strike Freescale Semiconductor Inc.s and NVIDIA Corporation Inc.s Affirmative Defenses and Counterclaims of Inequitable Conduct by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 10/31/2011)	
98	10/31/2011	ANSWER to 90 Answer to Amended Complaint, Counterclaim by Mosaid Technologies Inc..(Pankratz, Kurt) (Entered: 10/31/2011)	
99	10/31/2011	ANSWER to 91 Answer to Amended Complaint, Counterclaim by Mosaid Technologies Inc..(Pankratz, Kurt) (Entered: 10/31/2011)	
100	11/17/2011	RESPONSE in Opposition re 97 MOTION to Dismiss and Strike Freescale Semiconductor Inc.s and NVIDIA Corporation Inc.s Affirmative Defenses and Counterclaims of Inequitable Conduct filed by Freescale Semiconductor, Inc., NVIDIA Corporation. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3)(Hoffman, David) (Entered: 11/17/2011)	
101	11/22/2011	NOTICE of Discovery Disclosure by NVIDIA Corporation re Invalidity Contentions (Hoffman, David) (Entered: 11/22/2011)	
102	11/28/2011	NOTICE of Discovery Disclosure by Freescale Semiconductor, Inc. (Wood, Emily) (Entered: 11/28/2011)	
103	11/28/2011	NOTICE of Discovery Disclosure by Interphase Corporation (Wood, Emily) (Entered: 11/28/2011)	
104	11/28/2011	REPLY to Response to Motion re 97 MOTION to Dismiss and Strike Freescale Semiconductor Inc.s and NVIDIA Corporation Inc.s Affirmative Defenses and Counterclaims of Inequitable Conduct filed by Mosaid Technologies Inc.. (Pankratz, Kurt) (Entered: 11/28/2011)	
105	12/02/2011	Joint MOTION for Leave to File Amended Docket Control Order by Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Amended Joint Docket Control Order)(Pankratz, Kurt) (Entered: 12/02/2011)	
106	12/06/2011	AMENDED DOCKET CONTROL ORDER. Amended Pleadings due by 7/19/2012; Respond to Amended Pleadings by 8-02-2012. Expert Discovery due by 1/28/2013; Fact Discovery due 1-07-2013. Expert Witness List due by 11/28/2012. Identify trial witnesses by 2/1/2013; Rebuttal Trial Witnesses identified by 2-12-2013. Jury instructions due by 6/28/2013. Dispositive Motions	

#	Date	Proceeding Text	Source
		due by 2/15/2013; Response to Dispositive Motions due 3-01-2013. Proposed Pretrial Order due by 6/28/2013. Jury Selection set for 9/3/2013 09:00AM before Judge Leonard Davis. Jury Trial set for 9/9/2013 09:00 AM before Judge Leonard Davis. Markman Hearing set for 10/4/2012 09:30 AM before Judge Leonard Davis. Pretrial Conference set for 8/22/2013 09:00 AM before Judge Leonard Davis. Signed by Judge Leonard Davis on 12/06/11. cc:attys 12-06-11(mll,) (Entered: 12/06/2011)	
107	12/07/2011	SUR-REPLY to Reply to Response to Motion re 97 MOTION to Dismiss and Strike Freescale Semiconductor Inc.s and NVIDIA Corporation Inc.s Affirmative Defenses and Counterclaims of Inequitable Conduct filed by Freescale Semiconductor, Inc., NVIDIA Corporation. (Hoffman, David) (Entered: 12/07/2011)	
108	12/09/2011	NOTICE by Mosaid Technologies Inc. re 83 Response in Opposition to Motion, (Notice and Supplement to MOSAID's Opposition to Defendants' Motion to Sever and Transfer) (Pankratz, Kurt) (Entered: 12/09/2011)	
109	01/17/2012	NOTICE of Discovery Disclosure by Mosaid Technologies Inc. Notice of Compliance with P.R. 4-1 (Pankratz, Kurt) (Entered: 01/17/2012)	
110	01/17/2012	NOTICE of Discovery Disclosure by Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation Notice of Compliance with P.R. 4-1 (Hoffman, David) (Entered: 01/17/2012)	
111	02/16/2012	MOTION to Compel Reduction in Number of Asserted Claims and to Compel Detailed Infringement Contentions by Freescale Semiconductor, Inc., NVIDIA Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Text of Proposed Order)(Hoffman, David) (Entered: 02/16/2012)	
112	03/05/2012	RESPONSE in Opposition re 111 MOTION to Compel Reduction in Number of Asserted Claims and to Compel Detailed Infringement Contentions filed by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A, # 2 Text of Proposed Order)(Pankratz, Kurt) (Entered: 03/05/2012)	
113	03/14/2012	RESPONSE in Support re 111 MOTION to Compel Reduction in Number of Asserted Claims and to Compel Detailed Infringement Contentions filed by Freescale Semiconductor, Inc., NVIDIA Corporation. (Hoffman, David) (Entered: 03/14/2012)	
114	03/19/2012	Joint MOTION for Ruling on Disputed Issues Regarding Source Code Provisions by Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Exhibit A)(Pankratz, Kurt) (Additional attachment(s) added on 3/20/2012: # 2 Text of Proposed Order) (gsg,). (Entered: 03/19/2012)	
115	03/22/2012	ORDER granting 114 Joint Motion for Ruling on Disputed Issues Regarding Source Code Provisions. Issue 1: The Court adopts Defendants' proposal regarding the disclosure and production of source code printouts. Issue 2: The Court adopts Defendants' proposal regarding printing page limits. Issue 3: A printer shall be provided at the source code review location for the reviewing party to print on demand within the printing page limits. The Court ORDERS the parties to submit thier agreed Protective Order in compliance with this order within 10 days. Signed by Judge Leonard Davis on 3/22/2012. (leh,) (Entered: 03/22/2012)	
116	03/26/2012	SUR-REPLY to Reply to Response to Motion re 111 MOTION to Compel Reduction in Number of Asserted Claims and to Compel Detailed Infringement Contentions filed by Mosaid Technologies Inc.. (Pankratz, Kurt) (Entered: 03/26/2012)	
117	03/28/2012	MOTION for Protective Order (Agreed Motion for Entry of	

#	Date	Proceeding Text	Source
		Protective Order) by Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Protective Order, # 2 Appendix A - Source Code Provisions, # 3 Text of Proposed Order)(Pankratz, Kurt) (Entered: 03/28/2012)	
118	04/02/2012	PROTECTIVE ORDER. Signed by Judge Leonard Davis on 4/2/2012. (leh,) (Entered: 04/02/2012)	
119	04/09/2012	NOTICE of Attorney Appearance by Jamie Roy Lynn on behalf of Mosaid Technologies Inc. (Lynn, Jamie) (Entered: 04/09/2012)	
120	04/12/2012	Unopposed MOTION to Withdraw as Attorney (MOSAID Technologies, Inc.s Unopposed Motion for Withdrawal of Counsel) by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 04/12/2012)	
121	04/16/2012	MOTION to Limit Defendants' Invalidity Defenses by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Text of Proposed Order)(Pankratz, Kurt) (Entered: 04/16/2012)	
122	04/19/2012	ORDER granting 120 Motion to Withdraw as Attorney. Attorney Matthew Colagrosso terminated. Signed by Judge Leonard Davis on 04/19/12. cc:attys 4-19-12 (mll,) (Entered: 04/19/2012)	
123	04/26/2012	MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 04/26/2012)	
124	05/04/2012	RESPONSE in Opposition re 121 MOTION to Limit Defendants' Invalidity Defenses filed by Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7, # 8 Exhibit 8, # 9 Exhibit 9, # 10 Text of Proposed Order Order)(Witcoff, David) (Entered: 05/04/2012)	
125	05/14/2012	RESPONSE to Motion re 123 MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) Partial Opposition filed by Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation. (Hoffman, David) (Additional attachment(s) added on 5/16/2012: # 1 Text of Proposed Order) (gsg,). (Entered: 05/14/2012)	
126	05/14/2012	REPLY to Response to Motion re 121 MOTION to Limit Defendants' Invalidity Defenses filed by Mosaid Technologies Inc.. (Pankratz, Kurt) (Entered: 05/14/2012)	
127	05/14/2012	RESPONSE in Opposition re 123 MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) filed by ARM LTD., Arm, Inc.. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7, # 8 Exhibit 8, # 9 Exhibit 9, # 10 Exhibit 10, # 11 Text of Proposed Order)(Anderson, Kevin) (Entered: 05/14/2012)	
128	05/14/2012	ORDER granting in part and denying in part 37 Sealed Motion to Dismiss for Lack of Standing. LSI Logic Corporation shall have 10 days to join as a plaintiff in this civil action. Signed by Judge Leonard Davis on 05/14/12. cc:attys 5-15-12 (mll,) Modified on 5/15/2012 (mll,). (Entered: 05/15/2012)	
129	05/21/2012	REPLY to Response to Motion re 123 MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) filed by Mosaid Technologies Inc.. (Attachments: # 1 Appendix /Declaration of Jonathan B. Rubenstein, # 2 Exhibit s A-D (articles and print-outs ISO Reply))(Pankratz, Kurt) (Entered:	

#	Date	Proceeding Text	Source
		05/21/2012)	
130	05/24/2012	SUR-REPLY to Reply to Response to Motion re 121 MOTION to Limit Defendants' Invalidity Defenses filed by Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation. (Attachments: # 1 Exhibit 10 - invalidity chart, # 2 Exhibit 11 - invalidity chart, # 3 Exhibit 12 - invalidity chart, # 4 Exhibit 13 - invalidity chart, # 5 Exhibit 14 - invalidity chart, # 6 Exhibit 15 - invalidity chart, # 7 Exhibit 16 - invalidity chart, # 8 Exhibit 17 - invalidity chart)(Witcoff, David) (Entered: 05/24/2012)	
131	05/24/2012	AMENDED COMPLAINT (Second Amended Complaint) against Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation, filed by Mosaid Technologies Inc., Agere Systems Inc., LSI Corporation.(Pankratz, Kurt) (Entered: 05/24/2012)	
132	05/25/2012	NOTICE of Attorney Appearance by Bruce S Sostek on behalf of Agere Systems Inc., LSI Corporation (Sostek, Bruce) (Entered: 05/25/2012)	
133	05/25/2012	NOTICE of Attorney Appearance by Bruce S Sostek on behalf of Agere Systems Inc., LSI Corporation (Sostek, Bruce) (Entered: 05/25/2012)	
134	05/25/2012	CORPORATE DISCLOSURE STATEMENT filed by Agere Systems Inc., LSI Corporation (Sostek, Bruce) (Entered: 05/25/2012)	
135	05/29/2012	***FILED IN ERROR. SEE ENTRY 136 FOR CORRECTED FILING.*** CORPORATE DISCLOSURE STATEMENT filed by Mosaid Technologies Inc. identifying Corporate Parent 7577800 Canada Inc., Corporate Parent MTI Luxco S.a.r.l. for Mosaid Technologies Inc.. (Pankratz, Kurt) Modified on 5/30/2012 (gsg). (Entered: 05/29/2012)	
136	05/30/2012	CORPORATE DISCLOSURE STATEMENT filed by Mosaid Technologies Inc. identifying Corporate Parent 7577800 Canada Inc., Corporate Parent MTI Luxco S.a.r.l. for Mosaid Technologies Inc.. (Pankratz, Kurt) (Entered: 05/30/2012)	
	05/30/2012	NOTICE of Deficiency regarding the Corporate Disclosure Statement, entry 135. No certificate of service. See entry 136 for corrected filing. (gsg) (Entered: 05/30/2012)	
137	05/31/2012	SUR-REPLY to Reply to Response to Motion re 123 MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) filed by ARM LTD., Arm, Inc.. (Anderson, Kevin) (Entered: 05/31/2012)	
138	06/05/2012	MOTION for Leave to File Supplement In Support Of Defendants' Motion to Sever and Transfer to the Northern District of California by Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation. (Attachments: # 1 Supplement In Support Of Defendants' Motion to Sever and Transfer to the Northern District of California, # 2 Text of Proposed Order)(Hoffman, David) (Entered: 06/05/2012)	
139	06/06/2012	MOTION for Protective Order Requiring Complete Expert Disclosure Under Paragraph 9(e) of the Protective Order by Freescale Semiconductor, Inc., NVIDIA Corporation. (Attachments: # 1 Errata 1, # 2 Exhibit 2, # 3 Text of Proposed Order)(Hoffman, David) (Entered: 06/06/2012)	
140	06/07/2012	RESPONSE to Motion re 138 MOTION for Leave to File Supplement In Support of Defendants' Motion to Sever and Transfer to the Northern District of California (MOSAID's Non-Opposition to Defendants' Motion to File Supplement in Support of their Motion to Sever and Transfer) filed by Mosaid Technologies Inc.. (Pankratz, Kurt) (Entered: 06/07/2012)	

#	Date	Proceeding Text	Source
141	06/11/2012	***FILED IN ERROR. PLEASE DISREGARD.*** Joint MOTION for Extension of Time to Complete Discovery to Extend the Deadline for Privilege Logs by Agere Systems Inc., Freescale Semiconductor, Inc., Interphase Corporation, LSI Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order Proposed Order)(Witcoff, David) Modified on 6/11/2012 (gsg). (Entered: 06/11/2012)	
142	06/11/2012	ANSWER to 131 Amended Complaint , Affirmative Defenses, COUNTERCLAIM against Agere Systems Inc., LSI Corporation, Mosaid Technologies Inc. by Freescale Semiconductor, Inc..(Witcoff, David) (Entered: 06/11/2012)	
143	06/11/2012	ANSWER to 131 Amended Complaint , Affirmative Defenses, COUNTERCLAIM against Agere Systems Inc., LSI Corporation, Mosaid Technologies Inc. by Interphase Corporation.(Witcoff, David) (Entered: 06/11/2012)	
144	06/11/2012	ANSWER to 131 Amended Complaint Affirmative Defenses, COUNTERCLAIM against Agere Systems Inc., LSI Corporation, Mosaid Technologies Inc. by NVIDIA Corporation.(Hoffman, David) (Entered: 06/11/2012)	
	06/11/2012	NOTICE of Deficiency regarding the Joint Motion, entry 141 submitted. No certificate of conference. (gsg) (Entered: 06/11/2012)	
145	06/11/2012	MOTION to Withdraw 139 MOTION for Protective Order Requiring Complete Expert Disclosure Under Paragraph 9(e) of the Protective Order MOTION for Protective Order Requiring Complete Expert Disclosure Under Paragraph 9(e) of the Protective Order by Freescale Semiconductor, Inc., NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(Hoffman, David) (Entered: 06/11/2012)	
146	06/11/2012	Joint MOTION for Extension of Time to Complete Discovery and Serve Privilege Logs by Agere Systems Inc., Freescale Semiconductor, Inc., Interphase Corporation, LSI Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(Witcoff, David) (Entered: 06/11/2012)	
147	06/12/2012	NOTICE by NVIDIA Corporation of Compliance with P.R. 4-2 (Hoffman, David) (Entered: 06/12/2012)	
148	06/12/2012	ORDER granting 145 Motion to Withdraw; and withdrawing 139 Motion for Protective Order. Signed by Judge Leonard Davis on 06/12/12. cc:attys 6-12-12 (mll,) (Entered: 06/12/2012)	
149	06/12/2012	ORDER granting 146 Motion for Extension of Time to Complete Discovery. Signed by Judge Leonard Davis on 06/12/12. cc:attys 6-12-12 (mll,) (Entered: 06/12/2012)	
150	06/12/2012	NOTICE by Mosaid Technologies Inc. Plaintiff Mosaid Technologies Inc.'s Notice of Compliance with P.R. 4-2 (Lynn, Jamie) (Entered: 06/12/2012)	
151	06/13/2012	NOTICE by Freescale Semiconductor, Inc., Interphase Corporation of Compliance with P.R. 4-2 (Witcoff, David) (Entered: 06/13/2012)	
152	06/28/2012	ANSWER to 142 Answer to Amended Complaint, Counterclaim of Freescale Semiconductor, Inc. by Agere Systems Inc., LSI Corporation.(Corcoran, Peter) (Entered: 06/28/2012)	
153	06/28/2012	ANSWER to 143 Answer to Amended Complaint, Counterclaim of Interphase Corporation by Agere Systems Inc., LSI Corporation.(Corcoran, Peter) (Entered: 06/28/2012)	
154	06/28/2012	Mosaid Technologies Inc.'s Answer to Defendant Interphase Corporation's Counterclaim ANSWER to 143 Answer to Amended Complaint, Counterclaim by Mosaid Technologies Inc..(Pankratz, Kurt) (Entered: 06/28/2012)	

#	Date	Proceeding Text	Source
155	06/28/2012	Mosaid Technologies Inc.'s Answer to Defendant Freescale Semiconductor, Inc.'s Counterclaims to Second Amended Complaint ANSWER to 142 Answer to Amended Complaint, Counterclaim by Mosaid Technologies Inc..(Pankratz, Kurt) (Entered: 06/28/2012)	
156	06/28/2012	Mosaid Technologies Inc.'s Answer to Defendant Nvidia Corporation's Counterclaims to Second Amended Complaint ANSWER to 59 Answer to Amended Complaint, Counterclaim by Mosaid Technologies Inc..(Pankratz, Kurt) (Entered: 06/28/2012)	
157	07/10/2012	Joint MOTION for Extension of Time to Complete Discovery and Serve Privilege Logs by Agere Systems Inc., Freescale Semiconductor, Inc., Interphase Corporation, LSI Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 07/10/2012)	
158	07/11/2012	ORDER granting 157 Motion for Extension of Time to Complete Discovery. The deadline for serving Privilege Logs is extended to 8-03-2012. Signed by Judge Leonard Davis on 07/11/12. cc:attys 7-12-12 (mll,) (Entered: 07/12/2012)	
159	07/16/2012	JT CLAIM CONSTRUCTION AND PREHEARING STATEMENT filed by Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Exhibit A - Disputed Claim Constructions)(Hoffman, David) (Entered: 07/16/2012)	
160	07/26/2012	Joint MOTION for Extension of Time to File /Submit Proposed Technical Advisors by Agere Systems Inc., Freescale Semiconductor, Inc., Interphase Corporation, LSI Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Hoffman, David) (Additional attachment(s) added on 7/30/2012: # 1 Corrected Proposed Order) (gsg,). (Entered: 07/26/2012)	
161	08/01/2012	ORDER granting 160 Motion for Extension of Time. The deadline for Proposed Technical Advisors is extended to 8-02-2012. Signed by Judge Leonard Davis on 08/01/12. cc:attys 8-01-12 (mll,) (Entered: 08/01/2012)	
162	08/02/2012	NOTICE by Mosaid Technologies Inc. of Agreed Technical Advisor (Attachments: # 1 Exhibit A - McLemore C.V.)(Capshaw, Sidney) (Entered: 08/02/2012)	
163	08/06/2012	NOTICE of Discovery Disclosure by Mosaid Technologies Inc. re Privilege Log (Capshaw, Sidney) (Entered: 08/06/2012)	
164	08/06/2012	NOTICE by NVIDIA Corporation of Compliance re Privilege Log (Hoffman, David) (Entered: 08/06/2012)	
165	08/07/2012	NOTICE of Attorney Appearance by Chijioke E Offor on behalf of Freescale Semiconductor, Inc. (Offor, Chijioke) (Entered: 08/07/2012)	
166	08/07/2012	NOTICE by Freescale Semiconductor, Inc. of Compliance Regarding Privilege Log (Offor, Chijioke) (Entered: 08/07/2012)	
167	08/09/2012	Unopposed MOTION Name Change by Agere Systems Inc.. (Attachments: # 1 Text of Proposed Order Proposed Order)(Dominguez, Adrienne) (Additional attachment(s) added on 8/13/2012: # 2 Text of Proposed Order) (gsg,). (Entered: 08/09/2012)	
168	08/10/2012	Letter Brief filed by Freescale Semiconductor, Inc. (Attachments: # 1 Exhibit Letter Brief)(Wood, Emily) (Entered: 08/10/2012)	
169	08/10/2012	ORDER granting 167 Motion to change the name of pltf Agere Systems Inc to Agere Systems LLC. Signed by Judge Leonard Davis on 08/10/12. cc:attys 8-13-12 (mll,) Modified on 8/13/2012 (mll,). (Entered: 08/13/2012)	
170	08/13/2012	Unopposed MOTION to Substitute Attorney by Interphase Corporation. (Attachments: # 1 Text of Proposed Order)(Howland,	

#	Date	Proceeding Text	Source
		Mark) (Additional attachment(s) added on 8/15/2012: # 2 Corrected Proposed Order) (gsg,). (Entered: 08/13/2012)	
171	08/14/2012	Joint MOTION to Amend/Correct 159 Claim Construction Brief by Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Exhibit 1 - Amended 4-3 Exhibit A, # 2 Text of Proposed Order)(Hoffman, David) (Entered: 08/14/2012)	
172	08/14/2012	ORDER granting 170 Motion to Substitute Attorney. Added attorney Terrell Richard Miller for Interphase Corporation; Attorney Thomas C Wright terminated. Signed by Judge Leonard Davis on 08/14/12. cc:attys 8-15-12 (mll,) (Entered: 08/15/2012)	
173	08/15/2012	ORDER that parties meet and confer to reduce the number of disputed terms to a reasonable number. The Court further ORDERS parties to file an amended P.R.4-3 Statement by 8-20-2012. The Court also reminds the parties that the page limits governing dispositive motions pursuant to Local Rule CV-7(a) apply to claim construction briefing and will not be extended absent a showing of good cause. Signed by Judge Leonard Davis on 08/15/12. cc:attys 8-15-12(mll,) (Entered: 08/15/2012)	
174	08/20/2012	Amended Joint CLAIM CONSTRUCTION & Prehearing Statement - Amended Exfiled by Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Exhibit 1-Mosaid's Proposal re Claim Terms for Construction, # 2 Exhibit 3-Defendants' Statement re Number of Claim Terms at Issue)(Hoffman, David) (Entered: 08/20/2012)	
175	08/21/2012	ORDER Setting Hearing on Motion 111 MOTION to Compel Reduction in Number of Asserted Claims and to Compel Detailed Infringement Contentions, 121 MOTION to Limit Defendants' Invalidity Defenses, 171 Joint MOTION to Amend/Correct 159 Claim Construction BriefJoint MOTION to Amend/Correct 159 Claim Construction Brief : Motion Hearing set for 8/23/2012 01:30 PM before Judge Leonard Davis.. Signed by Judge Leonard Davis on 08/21/12. cc:attys 8-21-12(mll,) (Entered: 08/21/2012)	
176	08/21/2012	ORDER appointing Michael McLemore as the technical advisor to the Court in this action, with his costs to be assessed equally between Plaintiff and Defendants and timely paid as billed. Signed by Judge Leonard Davis on 08/21/12. cc:attys 8-21-12(mll,) (Entered: 08/21/2012)	
177	08/22/2012	NOTICE of Attorney Appearance by Jennifer Parker Ainsworth on behalf of Freescale Semiconductor, Inc., Interphase Corporation (Ainsworth, Jennifer) (Entered: 08/22/2012)	
178	08/23/2012	NOTICE by Mosaid Technologies Inc. of Submission of Technology Tutorial (Capshaw, Sidney) (Entered: 08/23/2012)	
179	08/23/2012	NOTICE by Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation Defedants' Notice of Compliance Regarding Tutorial (Eaton-Salners, Edward) (Entered: 08/23/2012)	
181	08/23/2012	Minute Entry for proceedings held before Judge Leonard Davis: Motion Hearing held on 8/23/2012 re 123 MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) filed by Mosaid Technologies Inc., 111 MOTION to Compel Reduction in Number of Asserted Claims and to Compel Detailed Infringement Contentions filed by NVIDIA Corporation, Freescale Semiconductor, Inc., 121 MOTION to Limit Defendants' Invalidity Defenses filed by Mosaid Technologies Inc., 171 Joint MOTION to Amend/Correct 159 Claim Construction BriefJoint MOTION to Amend/Correct 159 Claim Construction Brief filed by NVIDIA Corporation, Interphase Corporation, Mosaid	

#	Date	Proceeding Text	Source
		Technologies Inc., Freescale Semiconductor, Inc. (Court Reporter Shea Sloan.) (Attachments: # 1 Attorney Sign In Sheet) (rlf) (Entered: 08/28/2012)	
180	08/24/2012	RESPONSE to 168 Notice of Compliance - Letter Brief by LSI Corporation, Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A - Response to Letter Brief)(Capshaw, Sidney) (Entered: 08/24/2012)	
182	08/28/2012	ORDER denying as moot 111 Motion to Compel Reduction in Number of Asserted Claims; denying as moot 121 Motion to Limit Defendants' Invalidity Defenses; denying as moot 171 Motion to Amend/Correct Claim Construction Brief; and granting in part 123 Motion to Consolidate Cases. Civil Actions 6:11cv173 and 6:12cv08 are hereby CONSOLIDATED for both pretrial and trial matters. All future filings should be filed under 6:11cv173, as the Lead Case. Signed by Judge Leonard Davis on 08/28/12. cc:attys 8-28-12 (mll,) (Entered: 08/28/2012)	
	08/28/2012	Added Consolidated Defendants Arm Ltd and Arm Inc from Civil Action 6:12cv08 per 182 Order of Consolidation. (mll,) (Entered: 08/28/2012)	
183	08/28/2012	NOTICE by Mosaid Technologies Inc. re 182 Order on Motion to Compel, Order on Motion for Miscellaneous Relief, Order on Motion to Consolidate Cases, Order on Motion to Amend/Correct,,,,,,,, of Compliance (Capshaw, Sidney) (Entered: 08/28/2012)	
184	08/29/2012	Letter Brief filed by Freescale Semiconductor, Inc. (Attachments: # 1 Exhibit)(Wood, Emily) (Entered: 08/29/2012)	
185	09/05/2012	NOTICE by ARM Inc., ARM LTD., Freescale Semiconductor, Inc., Interphase Corporation, NVIDIA Corporation re 182 Order on Motion to Compel, Order on Motion for Miscellaneous Relief, Order on Motion to Consolidate Cases, Order on Motion to Amend/Correct,,,,,,,, Notice of Compliance (Hoffman, David) (Entered: 09/05/2012)	
186	09/05/2012	Revised P.R. 4-3 Joint Claim Construction and Prehearing Statement filed by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A - Chart)(Capshaw, Sidney) (Entered: 09/05/2012)	
187	09/05/2012	Plaintiff's CLAIM CONSTRUCTION BRIEF filed by Mosaid Technologies Inc.. (Attachments: # 1 Declaration of Jamie R. Lynn, # 2 Exhibit 1, # 3 Exhibit 2, # 4 Exhibit 3, # 5 Exhibit 4, # 6 Exhibit 5, # 7 Exhibit 6, # 8 Exhibit 7, # 9 Exhibit 8, # 10 Exhibit 9, # 11 Exhibit 10, # 12 Exhibit 11, # 13 Exhibit 12, # 14 Exhibit 13, # 15 Exhibit 14, # 16 Exhibit 15, # 17 Exhibit 16)(Pankratz, Kurt) (Entered: 09/05/2012)	
188	09/05/2012	Submission of Proposed Agreed Docket Control/Scheduling order by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Capshaw, Sidney) (Entered: 09/05/2012)	
189	09/07/2012	NOTICE OF FILING OF OFFICIAL TRANSCRIPT of Motion Hearing Proceedings held on 8/23/12 before Chief Judge Leonard Davis. Court Reporter: Shea Sloan, shea_sloan@txed.uscourts.gov NOTICE RE REDACTION OF TRANSCRIPTS: The parties have seven (7) business days to file with the Court a Notice of Intent to Request Redaction of this transcript. If no such Notice is filed, the transcript will be made remotely electronically available to the public without redaction after 90 calendar days. The policy is located on our website at www.txed.uscourts.gov Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Transcriber before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER.. Redaction Request due 10/1/2012. Redacted Transcript Deadline	

#	Date	Proceeding Text	Source
		set for 10/11/2012. Release of Transcript Restriction set for 12/10/2012. (sms,) (Entered: 09/07/2012)	
190	09/12/2012	AMENDED DOCKET CONTROL ORDER. Signed by Judge Leonard Davis on 09/12/12. cc:attys 9-12-12(mll,) (Entered: 09/12/2012)	
191	09/12/2012	ORDER granting 168 Notice of Compliance - Letter Brief request to file a motion for summary judgment of invalidity filed by Freescale Semiconductor, Inc. Signed by Judge Leonard Davis on 09/12/12. cc:attys 9-12-12(mll,) (Entered: 09/12/2012)	
192	09/13/2012	ORDER referring this case for claim construction and Defendants' Motion forSummary Judgment of Indefiniteness only to United States Magistrate Judge Keith F. Giblin for disposition. The undersigned will continue to oversee allother matters. Signed by Judge Leonard Davis on 09/13/12. cc:attys 9-13-12(mll,) (Entered: 09/13/2012)	
	09/13/2012	NOTICE of Hearing: Markman Hearing set for 10/4/2012 at 9:30 a.m. before Judge Davis is ***RESCHEDULED*** to 10/16/2012 at 9:00 AM in Ctrm 6 (Beaumont) before Magistrate Judge Keith F. Giblin. (sal) (Entered: 09/13/2012)	
193	09/14/2012	MOTION for Summary Judgment of Invalidity for Indefiniteness by Freescale Semiconductor, Inc.. (Attachments: # 1 Text of Proposed Order)(Witcoff, David) (Entered: 09/14/2012)	
194	09/20/2012	Defendants' Responsive 187 Claim Construction Brief, filed by ARM Inc., ARM LTD., Freescale Semiconductor, Inc., NVIDIA Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I)(Hoffman, David) (Entered: 09/20/2012)	
195	09/26/2012	NOTICE by Mosaid Technologies Inc. re 162 Notice (Other) Corrected Agreed Notice Regarding Technical Advisor (Capshaw, Sidney) (Entered: 09/26/2012)	
196	09/26/2012	CORRECTED CLAIM CONSTRUCTION BRIEF (Replaces Doc. 194) filed by Freescale Semiconductor, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I)(Witcoff, David) Modified on 10/11/2012 (sal,). (Entered: 09/26/2012)	
197	09/27/2012	ORDER denying 69 Motion to Sever NVIDIA Corporation Inc and Freescale Semiconductor Inc and Transfer to the Northern District of California. Signed by Judge Leonard Davis on 09/27/12. cc:attys 9-27-12 (mll,) (Entered: 09/27/2012)	
198	09/27/2012	ORDER granting in part and denying in part 97 Motion to Dismiss and Strike Freescale Semiconductor Inc's and NVIDIA Corporation Inc's Affirmative Defenses and Counterclaims of Inequitable Conduct. The Court grants Freescale and NVIDIA leave to amend their affirmative defenses and counterclaims within the next 14 days. Signed by Judge Leonard Davis on 09/27/12. cc:attys 9-27-12 (mll,) (Entered: 09/27/2012)	
199	09/27/2012	Plaintiff's REPLY 187 Claim Construction Brief, filed by Mosaid Technologies Inc.. (Attachments: # 1 Declaration of Jamie R. Lynn, # 2 Exhibit 17)(Pankratz, Kurt) (Entered: 09/27/2012)	
200	09/27/2012	CLAIM CONSTRUCTION CHART filed by ARM Inc., ARM LTD., Arm, Inc., Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Exhibit Claim Construction Chart)(DeRieux, Elizabeth) (Entered: 09/27/2012)	
201	09/27/2012	NOTICE by ARM Inc., ARM LTD., Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation (Joint Notice Regarding Time for Markman Hearing) (Pankratz, Kurt) (Entered: 09/27/2012)	

#	Date	Proceeding Text	Source
202	09/28/2012	RESPONSE in Opposition re 193 MOTION for Summary Judgment of Invalidity for Indefiniteness filed by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 09/28/2012)	
203	10/01/2012	***FILED IN ERROR PER ATTORNEY. SEE ENTRY 204 FOR CORRECTED FILING.***REPLY to Response to Motion re 193 MOTION for Summary Judgment of Invalidity for Indefiniteness filed by Freescale Semiconductor, Inc.. (Attachments: # 1 Text of Proposed Order)(Witcoff, David) Modified on 10/2/2012 (gsg). (Entered: 10/01/2012)	
204	10/01/2012	REPLY to Response to Motion re 193 MOTION for Summary Judgment of Invalidity for Indefiniteness [Corrected] filed by Freescale Semiconductor, Inc.. (Attachments: # 1 Text of Proposed Order)(Witcoff, David) (Entered: 10/01/2012)	
205	10/01/2012	ORDER granting 138 Motion for Leave to File Supplement in Support of Defendants' Motion to Sever and Transfer. Signed by Judge Leonard Davis on 10/01/12. cc:attys 10-02-12 (mll,) (Entered: 10/02/2012)	
206	10/02/2012	***FILED IN ERROR PER ATTORNEY. DISREGARD.***Corrected P.R. 4-5(c)Reply CLAIM CONSTRUCTION BRIEF filed by Mosaid Technologies Inc.. (DeRieux, Elizabeth) Modified on 10/2/2012 (gsg). (Entered: 10/02/2012)	
207	10/02/2012	Corrected P.R. 4-5(c) REPLY CLAIM CONSTRUCTION BRIEF filed by Mosaid Technologies Inc.. (DeRieux, Elizabeth) (Entered: 10/02/2012)	
208	10/03/2012	MOTION to Compel Production of Documents from NVIDIA Corporation by Mosaid Technologies Inc.. (Attachments: # 1 Declaration of Jonathan B. Rubenstein, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Text of Proposed Order)(Rubenstein, Jonathan) (Entered: 10/03/2012)	
210	10/16/2012	Minute Entry for proceedings held before Magistrate Judge Keith F. Giblin: Markman Hearing held on 10/16/2012. (Court Reporter Tonya Jackson) (ksd) (Entered: 10/17/2012)	
211	10/16/2012	Exhibit List by Freescale Semiconductor, Inc.(ksd) (Entered: 10/17/2012)	
209	10/17/2012	ORDER to pay Michael T. McLemore, technical consultant, $39,675.00 for services rendered through 10/17/2012, with payment to be divided equally between plaintiff and defendants. Signed by Magistrate Judge Keith F. Giblin on 10/17/12. (mjc,) (Entered: 10/17/2012)	
212	10/22/2012	RESPONSE in Opposition re 208 MOTION to Compel Production of Documents from NVIDIA Corporation filed by NVIDIA Corporation. (Hoffman, David) (Additional attachment(s) added on 10/25/2012: # 1 Text of Proposed Order) (gsg,). (Entered: 10/22/2012)	
213	10/26/2012	***DEFICIENT FILING. SEE ENTRY 218 FOR CORRECTED DOCUMENT.*** SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. by NVIDIA Corporation. (Attachments: # 1 Exhibit A-1, # 2 Exhibit A-2, # 3 Exhibit A-3, # 4 Exhibit B-1, # 5 Exhibit B-2, # 6 Exhibit B-3, # 7 Text of Proposed Order)(Hoffman, David) Modified on 11/2/2012 (gsg). (Entered: 10/26/2012)	
214	10/26/2012	MOTION to Compel Production of Documents from Mosaid Technologies Inc. (Public Version) by NVIDIA Corporation. (Attachments: # 1 Exhibit B-2, # 2 Exhibit B-3, # 3 Text of Proposed Order)(Hoffman, David) (Entered: 10/26/2012)	
215	10/26/2012	Agreed MOTION to Amend/Correct 190 Order by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed	

#	Date	Proceeding Text	Source
		Order)(Capshaw, Sidney) (Entered: 10/26/2012)	
216	10/29/2012	SEALED REPLY to Response to Motion re 208 MOTION to Compel Production of Documents from NVIDIA Corporation filed by Mosaid Technologies Inc.. (Attachments: # 1 Declaration of Jonathan B. Rubenstein, # 2 Exhibit E)(Rubenstein, Jonathan) (Entered: 10/29/2012)	
217	10/29/2012	AMENDED DOCKET CONTROL ORDER. Signed by Judge Leonard Davis on 10/29/12. cc:attys 10-29-12(mll,) (Entered: 10/29/2012)	
218	11/01/2012	SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. - Corrected by NVIDIA Corporation. (Attachments: # 1 Exhibit A-1, # 2 Exhibit A-2, # 3 Exhibit A-3, # 4 Exhibit B-1, # 5 Exhibit B-2, # 6 Exhibit B-3, # 7 Text of Proposed Order)(Hoffman, David) (Entered: 11/01/2012)	
219	11/01/2012	MOTION to Compel Production of Documents from Mosaid Technologies Inc. (Public Version) - Corrected by NVIDIA Corporation. (Attachments: # 1 Exhibit B-2, # 2 Exhibit B-3, # 3 Text of Proposed Order)(Hoffman, David) (Entered: 11/01/2012)	
	11/02/2012	NOTICE of Deficiency regarding the Motion to Compel, entries 213 and 214 submitted. No certificate of conference. See entries 218 and 219 for corrected filings. (gsg) (Entered: 11/02/2012)	
220	11/08/2012	SUR-REPLY to Reply to Response to Motion re 208 MOTION to Compel Production of Documents from NVIDIA Corporation filed by NVIDIA Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Hoffman, David) (Entered: 11/08/2012)	
221	11/12/2012	RESPONSE in Opposition re 218 SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. - Corrected filed by Mosaid Technologies Inc.. (Rubenstein, Jonathan) (Additional attachment(s) added on 11/13/2012: # 1 Text of Proposed Order) (gsg,). (Entered: 11/12/2012)	
222	11/19/2012	ORDER Setting Hearing on Motion 208 MOTION to Compel Production of Documents from NVIDIA Corporation, 218 SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. - Corrected : Motion Hearing set for 12/18/2012 01:30 PM before Judge Leonard Davis. Parties are ordered to meet and confer and attempt to resolve their discovery disputes prior to the hearing. Parties shall file a joint notice regarding the status of every pending motion no later than 12-11-2012. Signed by Judge Leonard Davis on 11/19/12. cc:attys 11-19-12(mll,) (Entered: 11/19/2012)	
223	11/26/2012	REPLY to Response to Motion re 218 SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. - Corrected filed by NVIDIA Corporation. (Hoffman, David) (Entered: 11/26/2012)	
224	11/26/2012	RESPONSE in Support re 218 SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. - Corrected (CORRECTED VERS. OF 223 NVIDIA'S RESPONSE) filed by NVIDIA Corporation. (Hoffman, David) (Entered: 11/26/2012)	
225	12/04/2012	SUR-REPLY to Reply to Response to Motion re 218 SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. - Corrected filed by Mosaid Technologies Inc.. (Rubenstein, Jonathan) (Entered: 12/04/2012)	
	12/10/2012	NOTICE of Hearing on Motion 208 MOTION to Compel Production of Documents from NVIDIA Corporation, 218 SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. : Motion Hearing set for 12/18/2012 at 1:30 PM HAS BEEN CONTINUED AND MOTION HEARING IS RESET TO	

#	Date	Proceeding Text	Source
		1/23/2013 at 10:00 AM before Judge Leonard Davis. (rlf) (Entered: 12/10/2012)	
226	12/11/2012	NOTICE by ARM Inc., ARM LTD., Freescale Semiconductor, Inc., Interphase Corporation, Mosaid Technologies Inc., NVIDIA Corporation re 222 Order Setting Hearing on Motion,, (Joint Notice Regarding the Status of All Pending Motions) (Rubenstein, Jonathan) (Entered: 12/11/2012)	
227	01/08/2013	***FILED IN ERROR. SEE 228 FOR CORRECT PLEADING.*** NOTICE of Attorney Appearance - Pro Hac Vice by Bryan A Blumenkopf on behalf of NVIDIA Corporation. Filing fee $ 100, receipt number 0540-3943987. (Blumenkopf, Bryan) Modified on 1/8/2013 (mll,). (Entered: 01/08/2013)	
228	01/08/2013	NOTICE of Attorney Appearance - Pro Hac Vice by Bryan A Blumenkopf on behalf of NVIDIA Corporation. Filing fee $ 100, receipt number 0540-3944051. (Blumenkopf, Bryan) (Entered: 01/08/2013)	
229	01/08/2013	NOTICE of Attorney Appearance - Pro Hac Vice by Christopher Scott Marchese on behalf of NVIDIA Corporation. Filing fee $ 100, receipt number 0540-3944213. (Marchese, Christopher) (Entered: 01/08/2013)	
230	01/09/2013	NOTICE of Attorney Appearance by Anthony Van Nguyen on behalf of NVIDIA Corporation (Nguyen, Anthony) (Entered: 01/09/2013)	
231	01/15/2013	***DEFICIENT FILING. DISREGARD.*** MOTION to Withdraw as Attorney of E. Alexander Eaton-Salners by NVIDIA Corporation. (Eaton-Salners, Edward) Modified on 1/18/2013 (gsg). (Entered: 01/15/2013)	
232	01/15/2013	Order reassigning this case to United States District Judge Michael H. Schneider per General Order 13-3. Please see Appendix D: Addendum Regarding Cases Assigned to Judge Schneider. Judge Leonard Davis no longer assigned to the case. (tlh,) (Entered: 01/15/2013)	
233	01/15/2013	NOTICE of Attorney Appearance - Pro Hac Vice by Thomas B Manuel on behalf of NVIDIA Corporation. Filing fee $ 100, receipt number 0540-3956092. (Manuel, Thomas) (Entered: 01/15/2013)	
	01/16/2013	NOTICE OF CANCELLATION OF HEARING: The hearing on Motions to Compel previously set for 1/23/2013 at 10:00 AM are hereby CANCELLED pending further notification from the Court. (lgp,) (Entered: 01/16/2013)	
	01/18/2013	NOTICE of Deficiency regarding the Motion to Withdraw, entry 231 submitted. No certificate of conference, no proposed order. Correction should be made by 1 business day. (gsg) (Entered: 01/18/2013)	
234	01/18/2013	Unopposed MOTION to Withdraw as Attorney E. Alexander Eaton-Salners by NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(Hoffman, David) (Entered: 01/18/2013)	
235	01/25/2013	Unopposed MOTION for Entry of Amended Docket Control Order by NVIDIA Corporation. (Attachments: # 1 Exhibit A - Amended Joint Docket Control Order)(Hoffman, David) (Entered: 01/25/2013)	
236	02/05/2013	ORDER granting 234 Motion to Withdraw as Attorney. Attorney Edward Alexander Eaton-Salners terminated. Signed by Judge Michael H. Schneider on 2/5/13. (mjc,) (Entered: 02/05/2013)	
237	02/21/2013	AMENDED DOCKET CONTROL ORDER. Signed by Judge Michael H. Schneider on 02/21/13. cc:attys 2-22-13 (mll,) (Entered: 02/22/2013)	
238	02/25/2013	Agreed MOTION to Dismiss Freescale Semiconductor, Inc. and Interphase Corporation by Agere Systems LLC, Freescale	

#	Date	Proceeding Text	Source
		Semiconductor, Inc., Interphase Corporation, LSI Corporation, Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Additional attachment(s) added on 2/25/2013: # 2 REVISED ORDER) (sm,). (Entered: 02/25/2013)	
239	02/28/2013	Joint MOTION to Withdraw 208 MOTION to Compel Production of Documents from NVIDIA Corporation, 218 SEALED MOTION to Compel Production of Documents from Mosaid Technologies Inc. - Corrected by Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(Rubenstein, Jonathan) (Entered: 02/28/2013)	
240	02/28/2013	ORDER OF DISMISSAL. ORDERED that all claims against Freescale by MOSAID, and against Interphase by MOSAID herein are dismissed with prejudice. ORDERED that to the extent that Freescale and Interphase allege that any claims were asserted against them by LSI and Agere, such claims are dismissed with prejudice. ORDERED that all claims against MOSAID, LSI and Agere by Freescale, and against MOSAID, LSI and Agere by Interphase herein are dismissed with prejudice. Signed by Judge Michael H. Schneider on 2/28/2013. (gsg) (Entered: 03/01/2013)	
241	03/04/2013	ORDER granting 239 Motion to Withdraw; withdrawing 208 Motion to Compel; withdrawing 218 Sealed Motion to Compel; withdrawing 219 Motion to Compel. Signed by Judge Michael H. Schneider on 03/04/13. cc:attys 3-05-13 (mll,) (Entered: 03/05/2013)	
242	03/05/2013	NOTICE of Attorney Appearance by Ruffin B Cordell on behalf of NVIDIA Corporation (Cordell, Ruffin) (Entered: 03/05/2013)	
243	03/07/2013	***DEFICIENT DOCUMENT, PLEASE IGNORE***MOTION to Withdraw as Attorney and Request for Termination of Electronic Notices by Freescale Semiconductor, Inc., Interphase Corporation. (Attachments: # 1 Text of Proposed Order Text of Proposed Order)(Witcoff, David) Modified on 3/7/2013 (sm,). (Entered: 03/07/2013)	
	03/07/2013	NOTICE of DEFICIENCY regarding the #243 Motion to withdraw submitted by Freescale Semiconductor, Inc., Interphase Corporation. No certificate of conference was included. Correction should be made by 1 business day and refiled. Motion now TERMINATED. (sm,) (Entered: 03/07/2013)	
244	03/18/2013	NOTICE of Discovery Disclosure by NVIDIA Corporation Notice of Compliance with P.R. 3-7 (Hoffman, David) (Entered: 03/18/2013)	
245	03/18/2013	NOTICE of Discovery Disclosure by NVIDIA Corporation Revised Initial Disclosures (Hoffman, David) (Entered: 03/18/2013)	
246	03/29/2013	Agreed MOTION to Amend/Correct 237 Order on Motion for Miscellaneous Relief Docket Control Order by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(DeRieux, Elizabeth) (Entered: 03/29/2013)	
247	04/15/2013	Unopposed MOTION to Withdraw Peter J. Corcoran, III, as Counsel by Agere Systems LLC, LSI Corporation. (Attachments: # 1 Text of Proposed Order)(Dominguez, Adrienne) (Entered: 04/15/2013)	
248	04/16/2013	ORDER granting 247 Motion to Withdraw Peter J Corcoran III as Counsel for LSI Corporation and Agere Systems LLC. Signed by Judge Michael H. Schneider on 04/16/13. (mll,) (Entered: 04/17/2013)	
249	04/24/2013	AMENDED DOCKET CONTROL ORDER. Mediation Completion due by 9/27/2013. Pretrial Conference and Trial Setting set for 2/3/2014 09:00 AM before Judge Michael H. Schneider. Motions terminated: 246 Agreed MOTION to Amend/Correct 237 Docket Control Order filed by Mosaid Technologies Inc. Signed by Judge Michael H. Schneider on 04/24/13. (mll,) (Entered: 04/25/2013)	

#	Date	Proceeding Text	Source
250	04/26/2013	SEALED MOTION for Protective Order Quashing "Apex" Depositions of Jeff Richardson and Jean F. Rankin by LSI Corporation. (Attachments: # 1 Exhibit 1-5, # 2 Text of Proposed Order)(Brandt, Jane) (Entered: 04/26/2013)	
251	04/29/2013	REPORT AND RECOMMENDATIONS recommending 193 MOTION for Summary Judgment of Invalidity for Indefiniteness filed by Freescale Semiconductor, Inc., be denied, because Claim 8 is not indefinite. Signed by Magistrate Judge Keith F. Giblin on 04/29/13. (mll,) (Entered: 04/29/2013)	
252	04/29/2013	MEMORANDUM OPINION AND ORDER. The above-cited claim terms of the patents-in-suit shall be construed in accordance with this Order. Signed by Magistrate Judge Keith F. Giblin on 04/29/13. (mll,) (Entered: 04/29/2013)	
253	05/01/2013	NOTICE OF FILING OF OFFICIAL TRANSCRIPT of Claim Construction Hearing held on 10.16.2012 before Magistrate Judge Keith Giblin. Court Reporter: Tonya B. Jackson, Telephone number: 409.654.2833. NOTICE RE REDACTION OF TRANSCRIPTS: The parties have seven (7) business days to file with the Court a Notice of Intent to Request Redaction of this transcript. If no such Notice is filed, the transcript will be made remotely electronically available to the public without redaction after 90 calendar days. The policy is located on our website at www.txed.uscourts.gov Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Transcriber before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER.. Redaction Request due 5/27/2013. Redacted Transcript Deadline set for 6/6/2013. Release of Transcript Restriction set for 8/2/2013. (tj,) (Entered: 05/01/2013)	
254	05/07/2013	NOTICE OF FILING OF **CORRECTED** OFFICIAL TRANSCRIPT of Claim Construction Hearing held on 10.16.2012 before Judge Keith Giblin (corrected to reflect the correct address of Mr. David Hoffman on page 2). Court Reporter: Tonya Jackson, Telephone number: 409.654.2833. NOTICE RE REDACTION OF TRANSCRIPTS: The parties have seven (7) business days to file with the Court a Notice of Intent to Request Redaction of this transcript. If no such Notice is filed, the transcript will be made remotely electronically available to the public without redaction after 90 calendar days. The policy is located on our website at www.txed.uscourts.gov Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Transcriber before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER.. Redaction Request due 5/31/2013. Redacted Transcript Deadline set for 6/10/2013. Release of Transcript Restriction set for 8/8/2013. (tj,) (Entered: 05/07/2013)	
255	05/13/2013	MOTION for Reconsideration re 252 Memorandum & Opinion Plaintiff's Objections and Motion for Reconsideration of the Claim Construction Opinion (Dkt. #252) by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit Exhibit A, # 2 Exhibit Exhibit B, # 3 Text of Proposed Order Proposed Order)(Pankratz, Kurt) (Entered: 05/13/2013)	
256	05/13/2013	MOTION for Reconsideration and Objections to Magistrate Giblins Claim Construction Order by ARM LTD., NVIDIA Corporation. (Attachments: # 1 Exhibit K to Defendants Objections to Magistrate Giblins Claim Construction Order and Motion for Reconsideration of Same, # 2 Text of Proposed Order)(Hoffman, David) (Entered: 05/13/2013)	
257	05/13/2013	Sealed Document. Exhibit J to Defendants Objections to Magistrate Giblins Claim Construction Order and Motion for	

#	Date	Proceeding Text	Source
		Reconsideration of Same(Hoffman, David) (Entered: 05/13/2013)	
258	05/13/2013	SEALED RESPONSE to Motion re 250 SEALED MOTION for Protective Order Quashing "Apex" Depositions of Jeff Richardson and Jean F. Rankin filed by ARM LTD., Arm, Inc.. (Attachments: # 1 Affidavit, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Exhibit O, # 17 Text of Proposed Order)(Anderson, Kevin) (Entered: 05/13/2013)	
259	05/24/2013	SEALED REPLY to Response to Motion re 250 SEALED MOTION for Protective Order Quashing "Apex" Depositions of Jeff Richardson and Jean F. Rankin filed by LSI Corporation. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4)(Brandt, Jane) (Entered: 05/24/2013)	
260	05/24/2013	RESPONSE in Opposition re 256 MOTION for Reconsideration and Objections to Magistrate Giblins Claim Construction Order filed by Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 05/24/2013)	
261	05/24/2013	SEALED PATENT MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS by Mosaid Technologies Inc.. (Attachments: # 1 Affidavit Lynn, # 2 Exhibit 1 - March 3, 2013 Correspondence, # 3 Exhibit 2 - April 19, 2013 Correspondence, # 4 Exhibit 3 - April 26, 2013 Correspondence, # 5 Exhibit 4 - Cover Sheet, # 6 Exhibit 5 - Franz Deposition, # 7 Exhibit 6 - PPW Project Update, # 8 Exhibit 7 - Kepler PMU Internal Architecture Specification, # 9 Exhibit 8 - December 28, 2012 Correspondence, # 10 Exhibit 9 - January 14, 2013 Correspondence, # 11 Exhibit 10 - Williams Declaration, # 12 Exhibit 11 - Amended Contentions for '230, # 13 Exhibit 12 - Amended Contentions for '505, # 14 Exhibit 13 - Amended Contentions for '036, # 15 Exhibit 14 - Amended Contentions for '762, # 16 Exhibit 15 - Amended Contentions for '725, # 17 Exhibit 16 - Amended Contentions for '306, # 18 Exhibit 17 - Amended Contentions for '680, # 19 Exhibit 18 - Amended Contentions for '885, # 20 Exhibit 19 - Amended Contentions for '811, # 21 Exhibit 20 - Gabriel Deposition, # 22 Exhibit 21 - Original Infringement Contentions, # 23 Exhibit 22 - Dewey Deposition, # 24 Exhibit 23 - September 19, 2011 Correspondence, # 25 Exhibit 24 - nVidia Production Chart, # 26 Exhibit 25 - August 13, 2012 Correspondence, # 27 Exhibit 26 - August 15, 2012 Correspondence, # 28 Exhibit 27 - Motion Hearing Transcript, # 29 Exhibit 28 - August 24, 2012 Correspondence, # 30 Exhibit 29 - August 27, 2012 Correspondence, # 31 Exhibit 30 - September 28, 2012 Correspondence, # 32 Exhibit 31 - October 1, 2012 Correspondence, # 33 Exhibit 32 - November 14, 2012 Correspondence, # 34 Exhibit 33 - Gap Chart, # 35 Exhibit 34 - December 3, 2012 Correspondence, # 36 Exhibit 35 - December 6, 2012 Correspondence, # 37 Exhibit 36 - January 5, 2013 Correspondence, # 38 Exhibit 37 - February 12, 2013 Correspondence, # 39 Exhibit 38 - February 18, 2013 Correspondence, # 40 Exhibit 39 - First Set of Interrogatories, # 41 Exhibit 40 - nVidia Objections and Answers to Interrogatories, # 42 Exhibit 41 - May 20, 2013 Correspondence, # 43 Text of Proposed Order)(DeRieux, Elizabeth) (Entered: 05/24/2013)	
262	05/24/2013	RESPONSE in Opposition re 255 MOTION for Reconsideration re 252 Memorandum & Opinion Plaintiff's Objections and Motion for Reconsideration of the Claim Construction Opinion (Dkt. #252) MOTION for Reconsideration re 252 Memorandum & Opinion Plaintiff's Objections and Motion for Reconsideration of the Claim Construction Opinion (Dkt. #252) filed by ARM Inc., ARM LTD.,	

#	Date	Proceeding Text	Source
		NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(Hoffman, David) (Entered: 05/24/2013)	
263	05/24/2013	***DEFICIENT DOCUMENT, PLEASE IGNORE***Sealed Document. Exhibit L to Defendants' Response to Plaintiff's Motion for Reconsideration of the Claim Construction Opinion (DKT #255)(Hoffman, David) Modified on 5/24/2013 (sm,). (Entered: 05/24/2013)	
	05/24/2013	NOTICE of DEFICIENCY regarding the #263 Sealed Document by Dfts (Exhibit L) submitted No certificate of authority to seal and wrong event used to file. Correction should be made by 1 business day and refiled. (sm,) (Entered: 05/24/2013)	
264	05/28/2013	SEALED ADDITIONAL ATTACHMENTS to Main Document: 262 Response in Opposition to Plaintiff's Motion for Reconsideration of the Claim Construction Opinion. (Attachments: # 1 Exhibit L - Argade Deposition)(Hoffman, David) (Entered: 05/28/2013)	
265	06/03/2013	REPLY to Response to Motion re 256 MOTION for Reconsideration and Objections to Magistrate Giblins Claim Construction Order filed by ARM Inc., ARM LTD., NVIDIA Corporation. (Hoffman, David) (Entered: 06/03/2013)	
266	06/03/2013	SEALED SUR-REPLY to Reply to Response to 250 SEALED MOTION for Protective Order Quashing "Apex" Depositions of Jeff Richardson and Jean F. Rankin filed by ARM Inc., ARM LTD.. (Attachments: # 1 Declaration of Kevin P. Anderson, # 2 Exhibit 1, # 3 Exhibit 2)(Anderson, Kevin) (Entered: 06/03/2013)	
267	06/03/2013	SEALED PATENT REPLY to Response to PATENT Motion re 255 MOTION for Reconsideration re 252 Memorandum & Opinion Plaintiff's Objections and Motion for Reconsideration of the Claim Construction Opinion (Dkt. #252) MOTION for Reconsideration re 252 Memorandum & Opinion Plaintiff's Objections and Motion for Reconsideration of the Claim Construction Opinion (Dkt. #252) filed by Mosaid Technologies Inc.. (Attachments: # 1 Declaration of Jamie R. Lynn, # 2 Exhibit 1, # 3 Exhibit 2)(Lynn, Jamie) (Entered: 06/03/2013)	
268	06/07/2013	Unopposed MOTION for Extension of Time to File Response/Reply as to 261 SEALED PATENT MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS by NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(Hoffman, David) (Entered: 06/07/2013)	
269	06/14/2013	Joint MOTION to Stay Deadlines by ARM Inc., ARM LTD., Agere Systems LLC, Arm, Inc., LSI Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(DeRieux, Elizabeth) (Entered: 06/14/2013)	
270	06/17/2013	ORDER denying as moot 269 Motion to Stay. All parties or their counsel shall submit to the Court all papers necessary for the closing of this case by 7-12-2013. Signed by Judge Michael H. Schneider on 06/17/13. (mll,) (Entered: 06/17/2013)	
271	06/21/2013	Joint MOTION to Dismiss by Agere Systems LLC, LSI Corporation, Mosaid Technologies Inc., NVIDIA Corporation. (Attachments: # 1 Text of Proposed Order)(Lynn, Jamie) (Entered: 06/21/2013)	
272	07/11/2013	Joint MOTION to Dismiss by ARM Inc., ARM LTD., Mosaid Technologies Inc.. (Attachments: # 1 Text of Proposed Order)(Lynn, Jamie) (Entered: 07/11/2013)	
273	08/28/2013	ORDER granting 271 Motion to Dismiss. All claims and counterclaims between Plaintiffs and Defendant NVIDIA Corporation are dismissed with prejudice. All attorneys' fees, costs of court and expenses shall be borne by each party incurring the same. Signed by Judge Michael H. Schneider on 08/28/13. (mll,) (Entered: 08/28/2013)	

#	Date	Proceeding Text	Source
274	08/28/2013	ORDER granting 272 Motion to Dismiss. All claims and counterclaims between Plaintiffs and Defendants ARM Inc and ARM Ltd are dismissed without prejudice. All attorneys' fees, costs of court and expenses shall be borne by each party incurring the same. Signed by Judge Michael H. Schneider on 08/28/13. (mll,) (Entered: 08/28/2013)	
275	08/30/2013	FINAL JUDGMENT. All relief not previously granted is DENIED. Signed by Judge Michael H. Schneider on 08/30/13. (mll,) (Entered: 08/30/2013)	

Patents

Number	Title	Issued	Class	Subclass
7,051,306	Managing Power on Integrated Circuits Using Power Islands	05/23/2006	716	127
7,415,680	Power Managers for an Integrated Circuit	08/19/2008	716	133
5,577,230	Apparatus and Method for Computer Processing Using an Enhanced Harvard Architecture Utilizing Dual Memory Buses and the Arbitration for Data/Instruction Fetch	11/19/1996	711	150
5,724,505	Apparatus and Method for Real-Time Program Monitoring via a Serial Interface	03/03/1998	714	45
5,958,036	Circuit for Arbitrating Interrupts with Programmable Priority Levels	09/28/1999	710	262
6,141,762	Power Reduction in a Multiprocessor Digital Signal Processor based on Processor Load	10/31/2000	713	300
6,256,725	Shared Datapath Processor Utilizing Stack-Based and Register-Based Storage Spaces	07/03/2001	712	200

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7,051,306

Dockets

Client: -None- History Help More

Document: 6:12cv846, Mosaid Technologies Inc. V. Nxp Semiconductors Usa, Inc. | Actions

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6:12cv846, Mosaid Technologies Inc. V. Nxp Semiconductors Usa, Inc.

US District Court Docket

US District Court for the Eastern District of TEXAS (LIVE)

(Tyler)

This case was retrieved on 12/12/2019

Header

Case Number: 6:12cv846
Date Filed: 11/05/2012
Assigned To: Judge Michael H. Schneider
Nature of Suit: Patent (830)
Cause: Patent Infringement
Lead Docket: None
Other Docket: None
Jurisdiction: Federal Question

Class Code: Closed
Closed: 03/04/2013
Statute: 35:271
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

Litigants

Mosaid Technologies Inc.
Plaintiff

NXP Semiconductors USA, Inc.
Defendant

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Proceedings

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	Availability	#	Date	Proceeding Text	Source

	Availability	#	Date	Proceeding Text	Source
	Free	1	11/05/2012	COMPLAINT against NXP Semiconductors USA, Inc. (Filing fee $ 350 receipt number 0540-3860068.), filed by Mosaid Technologies Inc.. (Attachments: # 1 Exhibit A-F, # 2 Civil Cover Sheet)(Capshaw, Sidney) (Entered: 11/05/2012)	
	Online	2	11/05/2012	Notice of Filing of Patent/Trademark Form (AO 120). AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (Capshaw, Sidney) (Entered: 11/05/2012)	
	Online	3	11/05/2012	CORPORATE DISCLOSURE STATEMENT filed by Mosaid Technologies Inc. (Capshaw, Sidney) (Entered: 11/05/2012)	
	Runner		11/05/2012	Judge Leonard Davis added. (mll,) (Entered: 11/06/2012)	
	Online	4	01/15/2013	Order reassigning this case to United States District Judge Michael H. Schneider per General Order 13-3. Please see Appendix D: Addendum Regarding Cases Assigned to Judge Schneider. Judge Leonard Davis no longer assigned to the case. (tlh,) (Entered: 01/15/2013)	
	Free	5	02/27/2013	NOTICE by Mosaid Technologies Inc. (Notice of Dismissal Without Prejudice Pursuant to Federal Rule of Civil Procedure 41(a)) (DeRieux, Elizabeth) (Entered: 02/27/2013)	
	Online	6	02/27/2013	ORDER for Plaintiff to file a notice of readiness for s Scheduling Conference. Signed by Judge Michael H. Schneider on 2/27/2013 (gsg) (Entered: 02/28/2013)	
	Free	7	03/04/2013	FINAL JUDGMENT. All relief not previously granted is hereby DENIED. Signed by Judge Michael H. Schneider on 03/04/13. cc:attys 3-05-13(mll,) (Entered: 03/05/2013)	

Retrieve Document(s)

Patents

Number	Title	Issued	Class	Subclass
7,051,306	Managing power on integrated circuits using power islands	05/23/2006	716	127
5,577,230	Apparatus and method for computer processing using an enhanced Harvard architecture utilizing dual memory buses and the arbitration for data/instruction fetch	11/19/1996	711	150
5,724,505	Apparatus and method for real-time program monitoring via a serial interface	03/03/1998	714	45
5,958,036	Circuit for arbitrating interrupts with programmable priority levels	09/28/1999	710	262
6,256,725	Shared datapath processor utilizing stack-based and register-based storage spaces	07/03/2001	712	200
6,446,193	Method and apparatus for single cycle processing of data associated with separate accumulators in a dual multiply-accumulate architecture	09/03/2002	712	35

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7,415,680

Dockets

Client: -None- History Help More

Document: 6:12cv8, Arm Ltd. Et Al V. Mosaid Technologies, Inc. Actions

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6:12cv8, Arm Ltd. Et Al V. Mosaid Technologies, Inc.

US District Court Docket

US District Court for the Eastern District of TEXAS (LIVE)

(Tyler)

This case was retrieved on 12/12/2019

Header

Case Number: 6:12cv8
Date Filed: 01/09/2012
Assigned To: Judge Michael H. Schneider
Nature of Suit: Patent (830)
Cause: Fed. Question
Lead Docket: None
Other Docket: California Northern, 3:11-cv-03869
Jurisdiction: Federal Question

Class Code: Closed
Closed: 08/28/2013
Statute: 28:1331
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

Litigants Attorneys

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Proceedings

Retrieve Document(s)

	Availability	#	Date	Proceeding Text	Source
	Free	1	08/05/2011	COMPLAINT against MOSAID Technologies, Inc. (Filing fee $ 350, receipt number 34611063096.). Filed byARM, Inc., ARM Ltd.. (Attachments: # 1 Civil Cover Sheet)(vlk, COURT STAFF) (Filed on 8/5/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/10/2011)	
	Purnar		08/05/2011	CASE DESIGNATED for Electronic Filing. (vlk, COURT STAFF) (Filed on 8/5/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/10/2011)	
	Online	2	08/05/2011	Summons Issued as to MOSAID Technologies, Inc.. (vlk, COURT STAFF) (Filed on 8/5/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/10/2011)	
	Online	3	08/05/2011	Initial Disclosures by ARM Ltd., ARM, Inc. (vlk, COURT STAFF) (Filed on 8/5/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/10/2011)	
	Online	4	08/05/2011	ADR SCHEDULING ORDER: Case Management Statement due by 11/9/2011. Case Management Conference set for 11/16/2011 01:30 PM. (Attachments: # 1 Standing Order)(vlk, COURT STAFF) (Filed on 8/5/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/10/2011)	
	Online	5	08/10/2011	NOTICE of Appearance by Dirk van Ausdall (van Ausdall, Dirk) (Filed on 8/10/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/10/2011)	
	Online	6	08/16/2011	MOTION of Karin Hessler for leave to appear in Pro Hac Vice (Filing fee $ 275, receipt number 44611007457.) filed by ARM Ltd., ARM, Inc.. (Attachments: # 1 Proposed Order)(vlk, COURT STAFF) (Filed on 8/16/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/17/2011)	

	Availability	#	Date	Proceeding Text	Source
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	Online	8	08/17/2011	ORDER granting 6 Karin Hessler's Motion for Admission Pro Hac Vice by Magistrate Judge Donna M. Ryu (lg, COURT STAFF) (Filed on 8/17/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/18/2011)	
	Online	9	08/17/2011	ORDER granting 7 Kevin Anderson's Motion for Admission Pro Hac Vice by Magistrate Judge Donna M. Ryu (lg, COURT STAFF) (Filed on 8/17/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 08/18/2011)	
	Online	10	08/26/2011	AMENDED COMPLAINT for Declaratory Judgment with Jury Demand, against MOSAID Technologies, Inc.. Filed by ARM, Inc., ARM Ltd.. (Anderson, Kevin) (Filed on 8/26/2011) Modified on 8/29/2011 (jlm, COURT STAFF). [Transferred from California Northern on 1/9/2012.] (Entered: 08/26/2011)	
	Free	11	08/26/2011	STIPULATION to Extend Time for Mosaid to Respond to First Amended Complaint, filed by ARM Ltd., ARM, Inc., (Attachments: # 1 Proposed Order)(Anderson, Kevin) (Filed on 8/26/2011) Modified on 8/29/2011 (jlm, COURT STAFF). [Transferred from California Northern on 1/9/2012.] (Entered: 08/26/2011)	
	Online	12	08/26/2011	ORDER ADOPTING STIPULATION TO EXTEND TIME for MOSAID Technologies, Inc. to Respond to Amended Complaint. Responsive pleading due by 10/10/11. Signed by Magistrate Judge Donna M. Ryu, on 8/26/2011. (dmrlc2, COURT STAFF) (Filed on 8/26/2011) Modified on 8/29/2011 (jlm, COURT STAFF). [Transferred from California Northern on 1/9/2012.] (Entered: 08/26/2011)	
	Online	13	09/30/2011	NOTICE of Appearance by Jon Vensel Swenson for MOSAID Technologies, Inc. (Swenson, Jon) (Filed on 9/30/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 09/30/2011)	
	Online	14	09/30/2011	NOTICE of Appearance by Kevin E Cadwell for MOSAID Technologies, Inc. (Cadwell, Kevin) (Filed on 9/30/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 09/30/2011)	
	Online	15	09/30/2011	Declination to Proceed Before a U.S. Magistrate Judge by MOSAID Technologies, Inc.. (Cadwell, Kevin) (Filed on 9/30/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 09/30/2011)	
	Online	16	10/03/2011	CLERK'S NOTICE of Impending Reassignment to U.S. District Judge (vlk, COURT STAFF) (Filed on 10/3/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/03/2011)	
	Online	17	10/04/2011	ORDER REASSIGNING CASE. Case reassigned to Judge Hon. Charles R. Breyer for all further proceedings. Magistrate Judge Donna M. Ryu no longer assigned to the case. Signed by the Executive Committee on October 4, 2011. (cjl, COURT STAFF) (Filed on 10/4/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/04/2011)	
	Online	18	10/10/2011	MOTION to Dismiss MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative, MOTION to Transfer Case filed by MOSAID Technologies, Inc.. Motion Hearing set for 12/9/2011 10:00 AM in Courtroom 6, 17th Floor, San Francisco before Hon. Charles R. Breyer. Responses due by 10/24/2011. Replies due by 10/31/2011. (Attachments: # 1 Proposed Order (Cadwell, Kevin) (Filed on 10/10/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/10/2011)	

	Availability	#	Date	Proceeding Text	Source
	Online	19	10/10/2011	Declaration of Kevin E. Cadwell In Support of MOSAID Technologies Inc.'s Motion to Dismiss or in the Alternative Motion to Transfer filed byMOSAID Technologies, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Exhibit N, (Cadwell, Kevin) (Filed on 10/10/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/10/2011)	
	Online	20	10/24/2011	RESPONSE (re 18 MOTION to Dismiss MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative MOTION to Transfer Case) filed byARM Ltd , ARM, Inc.. (Attachments: # 1 Proposed Order)(King, Edward) (Filed on 10/24/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/24/2011)	
	Online	21	10/24/2011	RESPONSE (re 18 MOTION to Transfer MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative MOTION to Transfer Case) (Opposition to Motion to Transfer) filed byARM Ltd., ARM, Inc. (Attachments: # 1 Proposed Order)(King, Edward) (Filed on 10/24/2011) Modified on 10/25/2011 (mcl, COURT STAFF). [Transferred from California Northern on 1/9/2012.] (Entered: 10/24/2011)	
	Free	22	10/24/2011	DECLARATION of Kevin P. Anderson in Opposition to 18 Motion to Dismiss, Motion to Transfer, filed byARM Ltd., ARM, Inc. (Attachments: # 1 Exhibit A1, # 2 Exhibit A2, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F1, # 8 Exhibit F2, # 9 Exhibit F3, # 10 Exhibit F4, # 11 Exhibit F5, # 12 Exhibit F6, # 13 Exhibit F7, # 14 Exhibit F8, # 15 Exhibit F9, # 16 Exhibit F10, # 17 Exhibit F11, # 18 Exhibit F12, # 19 Exhibit F13, # 20 Exhibit F14, # 21 Exhibit F15, # 22 Exhibit F16, # 23 Exhibit F17, # 24 Exhibit F18, # 25 Exhibit G, # 26 Exhibit H, # 27 Exhibit I, # 28 Exhibit J, # 29 Exhibit K, # 30 Exhibit L, # 31 Exhibit M, # 32 Exhibit N, # 33 Exhibit O, # 34 Exhibit P, # 35 Exhibit Q, # 36 Exhibit R, # 37 Exhibit S)(Related documents(s): 20 , 21) (King, Edward) (Filed on 10/24/2011) Modified on 10/25/2011 (mcl, COURT STAFF). [Transferred from California Northern on 1/9/2012.] (Entered: 10/24/2011)	
	Online	23	10/26/2011	CLERKS NOTICE Initial Case Management Conference set for 12/9/2011 10:00 AM in Courtroom 6, 17th Floor, San Francisco. (Attachments: # 1 Standing Order)(bas, COURT STAFF) (Filed on 10/26/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/26/2011)	
	Online	24	10/28/2011	MOTION for leave to appear in Pro Hac Vice (Kurt M. Pankratz) (Filing fee $ 275, receipt number 34611066334.) filed by MOSAID Technologies, Inc. (Attachments: # 1 Proposed Order)(mcl, COURT STAFF) (Filed on 10/28/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/28/2011)	
	Online	25	10/31/2011	Administrative Motion to File Under Seal Exhibit R to the Declaration of Kevin Cadwell in Support of MOSAID Technologies, Inc.'s Reply in Support of its Motion to Dismiss or in the Alternative Motion to Transfer filed by MOSAID Technologies, Inc.. (Attachments: # 1 Declaration, # 2 Proposed Order)(Cadwell, Kevin) (Filed on 10/31/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/31/2011)	
	Online	26	10/31/2011	REPLY (re 18 MOTION to Dismiss MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative MOTION to Transfer Case) filed byMOSAID Technologies, Inc.. (Cadwell, Kevin) (Filed on 10/31/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/31/2011)	

	Availability	#	Date	Proceeding Text	Source
	Online	27	10/31/2011	Declaration of Kevin E. Cadwell in Support of 26 Reply to Opposition/Response in Support of Motion to Dismiss or in the Alternative Motion to Transfer filed byMOSAID Technologies, Inc. (Attachments: # 1 Exhibit O, # 2 Exhibit P, # 3 Exhibit Q)(Related document(s): 26) (Cadwell, Kevin) (Filed on 10/31/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 10/31/2011)	
	Online	28	10/31/2011	MOTION for leave to appear in Pro Hac Vice (David M. Schlitz) (Filing fee $ 275, receipt number 34611066441.) filed by MOSAID Technologies, Inc. (Attachments: # 1 Proposed Order)(md, COURT STAFF) (Filed on 10/31/2011) (Transferred from California Northern on 1/9/2012.) (Entered: 11/01/2011)	
	Online	29	11/07/2011	ORDER by Judge Charles R. Breyer granting 28 Motion for Pro Hac Vice (D M Schlitz) (beS, COURT STAFF) (Filed on 11/7/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 11/07/2011)	
	Online	30	11/07/2011	ORDER by Judge Charles R. Breyer granting 24 Motion for Pro Hac Vice (K M Pankratz) (beS, COURT STAFF) (Filed on 11/7/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 11/07/2011)	
	Online	31	12/02/2011	CASE MANAGEMENT STATEMENT (JOINT); RULE 26(f) REPORT filed by ARM Ltd., ARM, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(King, Edward) (Filed on 12/2/2011) (Transferred from California Northern on 1/9/2012.) (Entered: 12/02/2011)	
	Online	32	12/09/2011	Minute Entry: Motion Hearing held on 12/9/2011 before Charles R. Breyer (Date Filed: 12/9/2011) re 18 MOTION to Dismiss MOSAID Technologies Inc.'s Notice of Motion and Motion to Dismiss or in the Alternative MOTION to Transfer Case filed by MOSAID Technologies, Inc.. (Court Reporter Belle Ball.) (beS, COURT STAFF) (Date Filed: 12/9/2011) [Transferred from California Northern on 1/9/2012.] (Entered: 12/13/2011)	
	Free	33	01/04/2012	ORDER by Judge Charles R. Breyer granting 18 Motion to Transfer Case. (crbic1, COURT STAFF) (Filed on 1/4/2012) [Transferred from California Northern on 1/9/2012.] (Entered: 01/04/2012)	
	Free	34	01/09/2012	Case transferred in from District of California Northern; Case Number 3:11-cv-03869. Original file certified copy of transfer order and docket sheet received. (Entered: 01/09/2012)	
	Free	35	01/09/2012	NOTICE OF CASE ASSIGNMENT. cc:attys 1-09-12 (mll,) (Entered: 01/09/2012)	
	Free	36	04/26/2012	MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) by MOSAID Technologies, Inc.. (Attachments: # 1 Text of Proposed Order)(Pankratz, Kurt) (Entered: 04/26/2012)	
	Free	37	05/14/2012	RESPONSE in Opposition re 36 MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) filed by ARM LTD , Arm, Inc.. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7, # 8 Exhibit 8, # 9 Exhibit 9, # 10 Exhibit 10, # 11 Text of Proposed Order)(Anderson, Kevin) (Entered: 05/14/2012)	

	Availability	#	Date	Proceeding Text	Source
	Free	38	05/21/2012	REPLY to Response to Motion re 36 MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) filed by MOSAID Technologies, Inc.. (Attachments: # 1 Affidavit /Declaration of Jonathan Rubenstein, # 2 Exhibit A-D (articles and print out ISO Reply)(Pankratz, Kurt) (Entered: 05/21/2012)	
	Online	39	05/29/2012	***FILED IN ERROR. SEE ENTRY 40 FOR CORRECTED FILING *** CORPORATE DISCLOSURE STATEMENT filed by MOSAID Technologies, Inc. Identifying Corporate Parent 7577600 Canada Inc., Corporate Parent MTI Luxco S.a.r.l. for MOSAID Technologies, Inc.. (Pankratz, Kurt) Modified on 5/30/2012 (gsg) (Entered: 05/29/2012)	
	Online	40	05/30/2012	CORPORATE DISCLOSURE STATEMENT filed by MOSAID Technologies, Inc. identifying Corporate Parent 7577600 Canada Inc., Corporate Parent MTI Luxco S.a.r.l. for MOSAID Technologies, Inc.. (Pankratz, Kurt) (Entered: 05/30/2012)	
	Runner		05/30/2012	NOTICE of Deficiency regarding the Corporate Disclosure Statement, entry 39, submitted. No certificate of service. See entry 40 for corrected filing. (gsg) (Entered: 05/30/2012)	
	Free	41	05/31/2012	SUR-REPLY to Reply to Response to Motion re 36 MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) MOTION to Consolidate Cases (MOSAID Technologies, Inc.s Motion to Consolidate the MOSAID Case and the ARM Case, and to Limit the Scope of the ARM Case) filed by ARM LTD , Arm, Inc.. (Anderson, Kevin) (Entered: 05/31/2012)	
	Free	42	08/28/2012	ORDER granting 36 Motion to Consolidate Cases. This civil action is hereby CONSOLIDATED with cause 6:11cv173 for both pretrial and trial matters. All future filings should be filed under 6:11cv173, as the Lead Case. Signed by Judge Leonard Davis on 08/28/12. cc:attys 8-28-12 (mll,) (Entered: 08/28/2012)	
	Free	43	01/15/2013	Order reassigning this case to United States District Judge Michael H. Schneider per General Order 13-3. Please see Appendix D: Addendum Regarding Cases Assigned to Judge Schneider. Judge Leonard Davis no longer assigned to the case. (mjc,) (Entered: 01/15/2013)	
	Free	44	08/28/2013	ORDER DISMISSING CASE. All claims and counter-claims between the parties are hereby DISMISSED without prejudice. All attorneys' fees, costs of court and expenses shall be borne by each party incurring the same. Signed by Judge Michael H. Schneider on 08/28/13. (mll,) (Entered: 08/28/2013)	

Retrieve Document(s)

Patents

Number	Title	Issued	Class	Subclass
5,577,220	Apparatus and method for computer processing using an enhanced Harvard architecture utilizing dual memory buses and the arbitration for data/instruction fetch	11/19/1996	711	150
5,724,505	Apparatus and method for real-time program monitoring via a serial interface	03/03/1998	714	45
5,958,036	Circuit for arbitrating interrupts with programmable priority levels	09/28/1999	710	262
6,141,762	Power reduction in a multiprocessor digital signal processor based on processor load	10/31/2000	713	300
6,256,725	Shared datapath processor utilizing stack-based and register-based storage spaces	07/03/2001	712	200

Number	Title	Issued	Class	Subclass
7,051,306	Managing power on integrated circuits using power islands	05/23/2006	716	127
7,415,680	Power managers for an integrated circuit	08/19/2008	716	133

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4:11cv3869, ARM Ltd et al v. Mosaid Technologies, Inc

US District Court Docket

US District Court for the Northern District of California

(Oakland)

This case was retrieved on 10/03/2011

Header

Case Number: 4:11cv3869
Date Filed: 08/05/2011
Assigned To: Magistrate Judge Donna M RYU
Nature of Suit: Patent (830)
Cause: Fed. Question
Lead Docket: None
Other Docket: None
Jurisdiction: Federal Question

Class Code: Open
Statute: 28:1331
Jury Demand: Plaintiff
Demand Amount: $0
NOS Description: Patent

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ARM, Inc **PLAINTIFF**	Dirk Van Ausdall [COR LD NTC] King and Kelleher LLP Four Embarcadero Center17TH Floor San Francisco, CA 94111 USA 415-781-2888Email: DVANAUSDALL@KINGANDKELLEHER.COM Edward Vincent King , Jr [COR LD NTC] King & Kelleher, LLP Four Embarcadero Center17TH Floor San Francisco, CA 94111 USA 415-781-2888Fax: 415-781-3011Email: EVKING@KINGANDKELLEHER.COM Karin Hessler [COR LD NTC] Wiley Rein LLP 1776 K Street, NW Washington, DC 20006 USA (202) 719-7000<i>pro Hac Vice</ I>Email: Khessler@wileyrein.com Kevin Anderson [COR LD NTC] Wiley Rein LLP 1776 K Street, NW Washington, DC 20006 USA (202) 719-7000Fax: (202) 719-7049<i>pro Hac Vice</ I>Email: KANDERSON@WILEYREIN.COM Kevin Paul Anderson [COR LD NTC] Wiley Rein LLP 1776 K Street, NW Washington, DC 20006 USA 202-719-3586<i>pro Hac Vice</ I>Email:

4:11cv3869, ARM Ltd et al v. Mosaid Technologies, Inc

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DEFENDANT

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Proceedings

#	Date	Proceeding Text	Source
1	08/05/2011	COMPLAINT against MOSAID Technologies, Inc. (Filing fee $ 350, receipt number 34611063096.). Filed byARM, Inc., ARM Ltd.. (Attachments: # (1 Civil Cover Sheet)(vlk, COURT STAFF) (Filed on 8/5/2011) (Entered: 08/10/2011)	
--	08/05/2011	CASE DESIGNATED for Electronic Filing. (vlk, COURT STAFF) (Filed on 8/5/2011) (Entered: 08/10/2011)	
2	08/05/2011	Summons Issued as to MOSAID Technologies, Inc.. (vlk, COURT STAFF) (Filed on 8/5/2011) (Entered: 08/10/2011)	
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#	Date	Proceeding Text	Source
		Demand, against MOSAID Technologies, Inc.. Filed by ARM, Inc., ARM Ltd.. (Anderson, Kevin) (Filed on 8/26/2011) Modified on 8/29/2011 (jlm, COURT STAFF). (Entered: 08/26/2011)	
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15	09/30/2011	Declination to Proceed Before a U.S. Magistrate Judge by MOSAID Technologies, Inc.. (Cadwell, Kevin) (Filed on 9/30/2011) (Entered: 09/30/2011)	
16	10/03/2011	CLERK'S NOTICE of Impending Reassignment to U.S. District Judge (vlk, COURT STAFF) (Filed on 10/3/2011) (Entered: 10/03/2011)	

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5,724,505	Apparatus and method for real-time program monitoring via a serial interface	03/03/1998	714	45
5,958,036	Circuit for arbitrating interrupts with programmable priority levels	09/28/1999	710	262
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6,256,725	Shared datapath processor utilizing stack-based and register-based storage spaces	07/03/2001	712	200
7,051,306	Managing power on integrated circuits using power islands	05/23/2006	716	127
7,415,680	Power managers for an integrated circuit	08/19/2008	716	133

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Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15192486
Filing Date	2016-06-24
First Named Inventor	HOBERMAN
Art Unit	2851
Examiner Name	TBD
Attorney Docket Number	6310

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /MY/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN
	Art Unit	2851
	Examiner Name	TBD
	Attorney Docket Number	6310

	1	SARWAR Abdul, "CMOS Power Consumption And Cpd Calculation", Texas Instruments - SCAA035B, June 1997, 16 pgs

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To: Michael Yigdall Location: RND-5A31 Art Unit: N/A Thursday, December 12, 2019 Case Serial Number: 15192486	From: Diane Jackson Location: EIC2800 JEF-4B68 Phone: (571)272-3260 diane.jackson@uspto.gov

Search Notes

Hi,

RE: Serial Number 15192486 – Patents:
8762923, 8782590, 7996811, 7945885, 7415680 and 7051306

Attached are litigation search results in Courtlink, Dialog Solutions (ProQuest) and Lexis Advance.

Litigation was found.

If you have any questions, please feel free to contact me.

Thanks,

Diane

Application Number Information

Application Number: **15/192486** Assignments
Filing or 371(c) Date: **06/24/2016** PAY
Effective Date: **06/24/2016**
Application Received: **06/24/2016**
Patent Number:
Issue Date: **00/00/0000**
Date of Abandonment: **00/00/0000**
Attorney Docket Number: **01181-US-REI**
Status: **30 /DOCKETED NEW CASE - READY FOR EXAMINATION**
Confirmation Number: **6310**
Title of Invention: **POWER MANAGERS FOR AN INTEGRATED CIRCUIT**

AIA (First Inventor to File): **NO**
Examiner Number: **80002 /** YIGDALL, MICHAEL
Group Art Unit: 3992
Class/Subclass: **716/133.000**
Interference Number:
Unmatched Petition: **NO**
L&R Code, Secrecy Code:**1**
Third Level Review: **NO**

Oral Hearing: **NO**

TYPE ENT: **U**
IFW Mantras / eDAS

Waiting for Response Desc.
Prior Art Filed
Prior Art Filed
Prior Art Filed

Secrecy Order: **NO**
Status Date: **11/28/2016**
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Continuity/Reexam Information for 15/192486

Parent Data

15192486, filed 06/24/2016 is a reissue of 13473129, filed 05/16/2012 ,now U.S. Patent #8762923 and having 2 RCE-type filings therein
13473129 is a division of 13164362, filed 06/20/2011 ,now U.S. Patent #8782590 and having 2 RCE-type filings therein
13164362 is a continuation of 12332529, filed 12/11/2008 ,now U.S. Patent #7996811 and having 1 RCE-type filing therein
12332529 is a continuation of 12176645, filed 07/21/2008 ,now U.S. Patent #7945885 and having 1 RCE-type filing therein
12176645 is a continuation of 11336097, filed 01/20/2006 ,now U.S. Patent #7415680
11336097 is a continuation of 10840893, filed 05/07/2004 ,now U.S. Patent #7051306
10840893 Claims Priority from Provisional Application 60468742, filed 05/07/2003

Child Data

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Apparatus and method for computer processing using an enhanced Harvard architecture utilizing dual memory buses and the arbitration for data/instruction fetch

Argade, Pramod V; Betker, Michael R (Inventors). AT&T Corp (Assignee). **US 5577230**. (Published 19 Nov 1996).

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Assignee	AT&T Corp
Inventor	Argade, Pramod V Betker, Michael R
Publication number	US 5577230 (19 November 1996)
Related patent	US 5724505 US 5958036 US 6141762 US 6256725 US 7051306 US 7415680 US 7945885 US 7996811
US classification	711/150: electrical computers and digital processing systems: memory
Plaintiff	ARM LTD ARM INC
Defendant	MOSAID TECHNOLOGIES INC
Court and docket number	Texas, Eastern Dist (Docket: 6:12CV00008)
Court filing date	09 January 2012
Action	CAUSE - 28 USC 1331 - COMPLAINT FOR PATENT INFRINGEMENT
Language	English

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US8762923B2 - Power managers for an integrated circuit

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Bibliographic information

Publication number and date
US8762923B2 06/24/2014
Granted

Application number and date
US13473129 05/16/2012

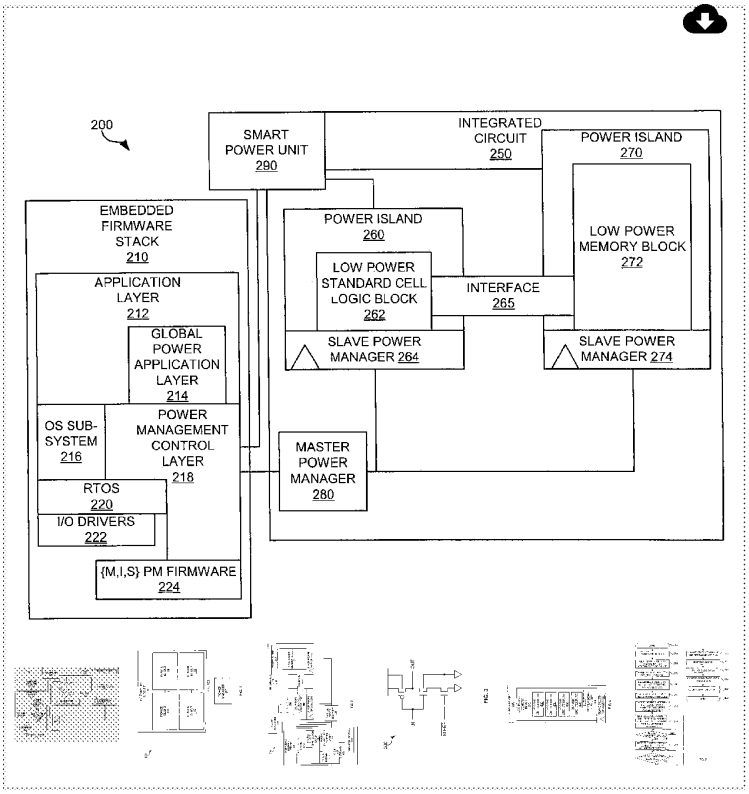
Priority number and date
US13473129 05/16/2012

Original assignee
Conversant Intellectual Property Management Inc.

Current assignee
VIRTUAL SILICON TECHNOLOGY, INC.

Inventor
Barry Alan Hoberman

Legal representative
Dennis R. Haszko



Abstract

A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

Description

5 .5. The system of wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

6 .6. The system of wherein the source voltage of the first power island is controlled by a smart power

Total of 100% of claims loaded.

Classifications

IPC

G06F17/50
G06F9/45
H01L

CPC

H03K3/012
G06F1/3203
G06F1/324
G06F1/3296
H01L2924/00
H01L2924/0002
H02J4/00
Y02D10/126
Y02D10/172
Y02D50/20

Families

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Extended (51)	Complete (2)	Main (2)	Domestic (2)	Application number	Pu

"ARM Ltd. and ARM, Inc.'s Frist Amended Complaint for Declaratory Judgment," ARM, Ltd. and ARM, Inc. v. Mosaid Techonologies Inc., Case No. 11-CV-3869, Document 10, filed Aug. 26, 2011.
"Defendant Nvidia Corporation's Answer, Affirmative Defenses and Counterclaims to Plaintiff Mosaid Technologies Inc.'s First Amended Complaint," Mosaid Technologies Inc., v. Freescale Semiconductor, Inc., et al., Civil Action No. 6:11-cv-00173-LED, Docuement 59, filed Aug. 29, 2011.
"Defendants' L.P.R. 3-3 Invalidity Contentions," MOSAID Technologies Inc. v. Freescale Semiconductor, Inc., et al., Civil Action No. 6:11-CV-173, In the United States District Court for the Eastern District of Texas Tyler Division, served on Nov. 21, 2011.
"Exhibit 306-E-1, Invalidity Contentions for U.S. Patent No. 7,051,306 in light of System-Level Power Optimization: Techniques and Tools ("Benini") as Base Reference," Defendants' L.P.R. 3-3 Invalidity Contentions, MOSAID Technologies Inc. v. Freescale Semiconductor, Inc., et al., Civil Action No. 6:11-CV-173, In the United States District Court for the Eastern District of Texas Tyler Division, served on Nov. 21, 2011, 97 pages.
"Exhibit 306-E-2, Invalidity Contentions for U.S. Patent No. 7,051,306 in light of U.S. Patent No. 6,836,849 ("Brock") as Base Reference," Defendants' L.P.R. 3-3 Invalidity Contentions, MOSAID Technologies Inc. v. Freescale Semiconductor, Inc., et al., Civil Action No. 6:11-CV-173, In the United States District Court for the Eastern District of Texas Tyler Division, served on Nov. 21, 2011, 73 pages.
"Exhibit 306-E-3, Invalidity Contentions for U.S. Patent No. 7,051,306 in light of Managing Power and

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Original	Standardized	Normalized
Conversant Intellectual Property Management Inc. Ottawa, Canada, CA	CONVERSANT IP	CONVERSANT IP

Current Assignees

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VIRTUAL SILICON TECHNOLOGY, INC.	VIRTUAL SILICON TECHNOLOGY	
CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP

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Daniel L. Hillman San Jose, California, United States of America, US
Jon Shiell San Jose, California, United States of America, US

Legal representative(s)

Original	Standardized	Normalized

Original	Standardized	Normalized
Dennis R. Haszko		

Legal information

Status

Event	Date
Granted	06/24/2014
Filed	05/16/2012

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10/07/2005	11/11/2005	MOSAID DELAWARE, INC.	MOSAID	MOSAID
08/04/2004	08/04/2004	SHIELL, JON	SHIELL JON	
07/29/2004	07/29/2004	HOBERMAN, BARRY ALAN	HOBERMAN BARRY ALAN	
07/29/2004		VIRTUAL SILICON TECHNOLOGY, INC.	VIRTUAL SILICON TECHNOLOGY	
07/28/2004	07/28/2004	HILLMAN, DANIEL L.	HILLMAN DANIEL L	

Payment status

Date	Payment status	Description
12/07/2017	Fee paid	PAYMENT OF MAINTENANCE FEE, 4TH YEAR, LARGE ENTITY.

Litigation

Date	Docket number	Comments	Judgement

US Patent Issued to Conversant Intellectual Property Management on June 24 for "Power managers for an integrated circuit" (California Inventors)

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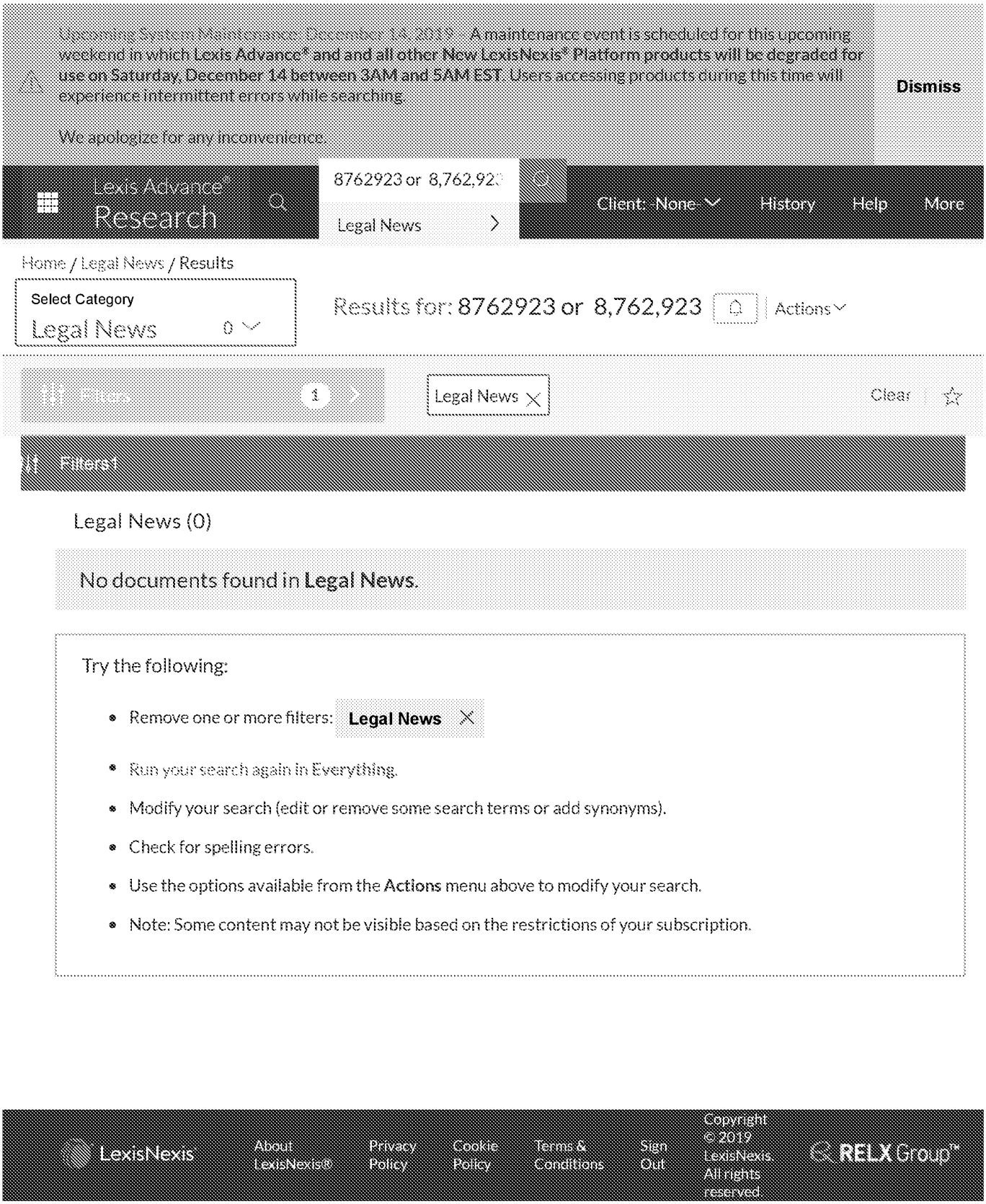
ALEXANDRIA, Va., June 24 -- United States Patent no. ***8,762,923***, issued on June 24, was assigned to Conversant Intellectual Property Management Inc. (Ottawa).

"Power managers for an integrated circuit" was invented by Barry Alan Hoberman (Cupertino, Calif.), Daniel L. Hillman (San Jose, Calif.) and Jon Shiell (San Jose, Calif.). According to the abstract* released ...

... operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands." The patent was filed on May 16, 2012, under Application No. 13/473,129. *For further information, including images, charts and tables, please visit: http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&p=1&u=%2Fnetahtml%2FPTO%2Fsearch-bool.html&r=1&f=G&l=50&co1=AND&d=PTXT&s1=8762923&OS=8762923&RS=8762923 For any query with respect to this article ***or*** any other content requirement, please contact Editor at hisyndication@hindustantimes.com

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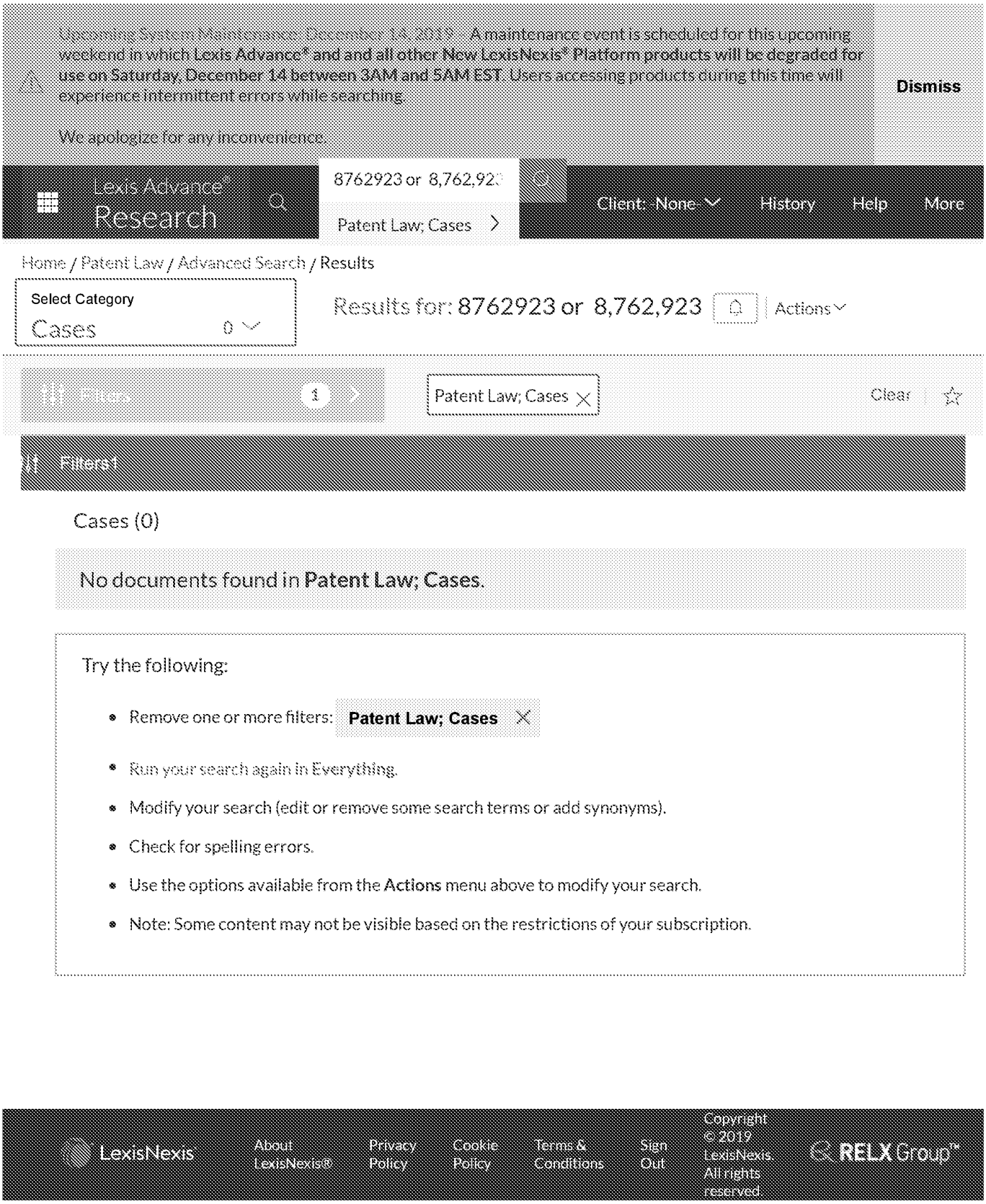
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US8782590B2 - Power managers for an integrated circuit

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Bibliographic information

Publication number and date
US8782590B2 07/15/2014
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Application number and date
US13164362 06/20/2011

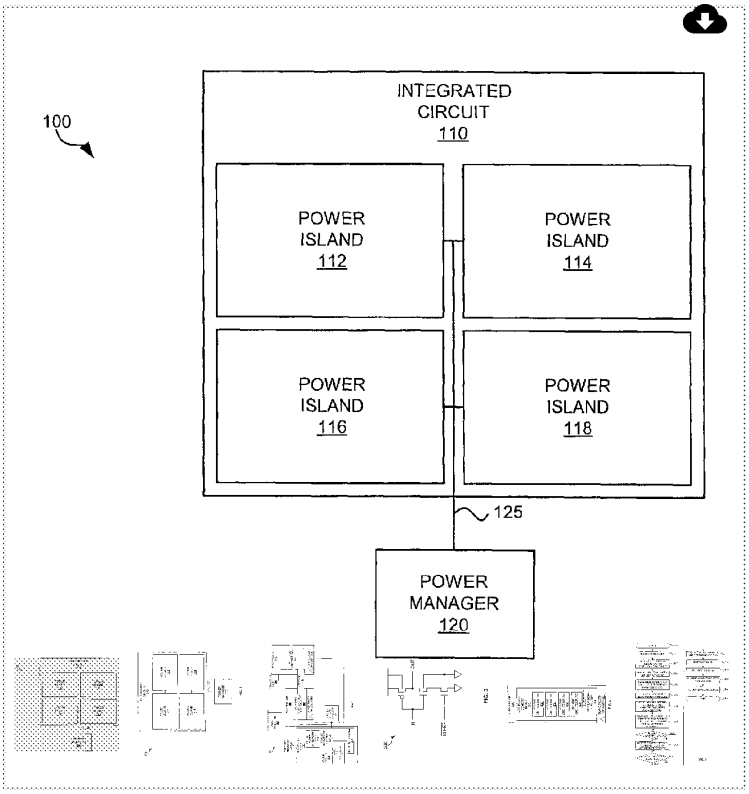
Priority number and date
US13164362 06/20/2011

Original assignee
Conversant Intellectual Property Management Inc.

Current assignee
VIRTUAL SILICON TECHNOLOGY, INC.

Inventor
Barry Alan Hoberman

Legal representative
Dennis R. Haszko



Abstract

A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

Description

6 .6. The system of wherein the power consumption signal of the at least one of the power islands includes temperature measurement.

7 .7. The system of wherein the power consumption signal of the at least one of the power islands includes power dissipation measurement.

8 .8. A processor implemented method comprising: employing a power management processor that is

Total of 100% of claims loaded.

Classifications

IPC

H02J1/00
G06F9/45
G06F17/50
H01L

CPC

H03K3/012
G06F1/3203
G06F1/324
G06F1/3296
H01L2924/00
H01L2924/0002
H02J4/00
Y02D10/126
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Extended (51)	Complete (2)	Main (2)	Domestic (2)	Application number	Pu

Nowka et al., “A 0.9V to 1.95V Dynamic Voltage-Scalable and Frequency-Scalable 32b PowerPC Processor”, Feb. 2002, IEEE International Solid-State Circuits Conference, Digest of Technical Papers, vol. 1, pp. 340-342.
Nowka et al., “A 0.9V to 1.95V Dynamic Voltage-Scalable and Frequency-Scalable 32b PowerPC Processor”, Feb. 2002, IEEE International Solid-State Circuits Conference, Digest of Technical Papers, vol. 2, pp. 272, 273, 503.
“First Amended Complaint,” Mosaid Technologies Inc., v. Freescale Semiconductor, Inc., et al., Civil Action No. 6:11-cv-00173-LED, Document 46, filed Aug. 15, 2011.
“Defendant Nvidia Corporation's Answer, Affirmative Defenses and Counterclaims to Plaintiff Mosaid Technologies Inc.'s First Amended Complaint,” Mosaid Technologies Inc., v. Freescale Semiconductor, Inc., et al., Civil Action No. 6:11-cv-00173-LED, Docuement 59, filed Aug. 29, 2011.
“Interphase Corporation's Answer to Plaintiff's First Amended Complaint,” Mosaid Technologies Inc., v. Freescale Semiconductor, Inc., et al., Civil Action No. 6:11-cv-00173-LED, Document 68, filed Sep. 1, 2011.
“Freescale Semiconductor, Inc.'s Answer to Plaintiffs First Amended Complaint,” Mosaid Technologies Inc., v. Freescale Semiconductor, Inc., et al., Civil Action No. 6:11-cv-00173-LED, Document 67, filed Sep. 1, 2011.
“ARM Ltd. and ARM, Inc.'s Frist Amended Complaint for Declaratory Judgment,” ARM, Ltd. and ARM, Inc. v. Mosaid Techonologies Inc., Case No. 11-CV-3869, Document 10, filed Aug. 26, 2011.

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Original	Standardized	Normalized
Conversant Intellectual Property Management Inc. Ottawa, Canada, CA	CONVERSANT IP	CONVERSANT IP

Current Assignees

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VIRTUAL SILICON TECHNOLOGY, INC.	VIRTUAL SILICON TECHNOLOGY	
CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP

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Daniel L. Hillman San Jose, California, United States of America, US
Jon Shiell San Jose, California, United States of America, US

Legal representative(s)

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Event	Date
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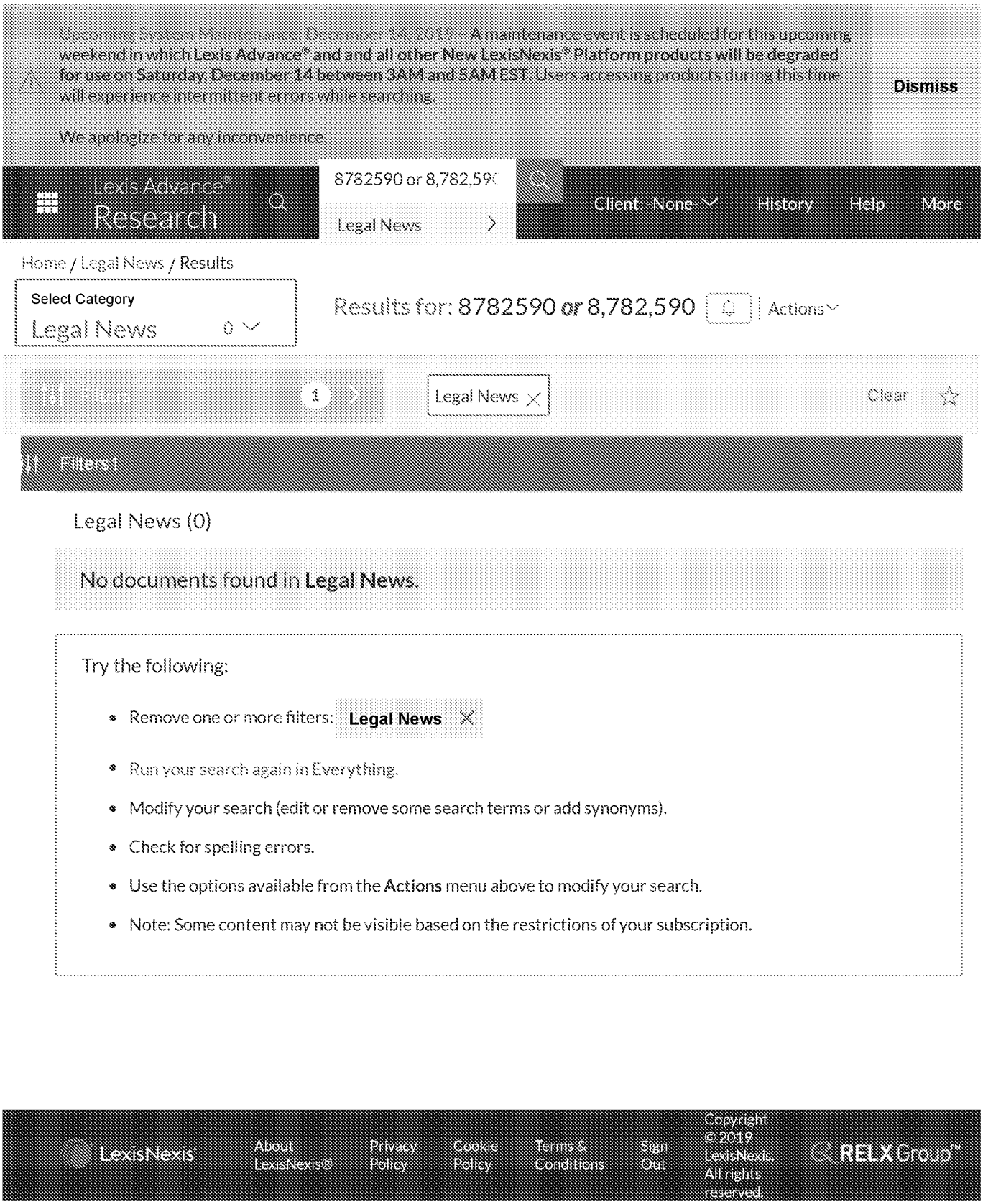
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07/29/2004	07/29/2004	HOBERMAN, BARRY ALAN	HOBERMAN BARRY ALAN	
07/29/2004		VIRTUAL SILICON TECHNOLOGY, INC.	VIRTUAL SILICON TECHNOLOGY	
07/28/2004	07/28/2004	HILLMAN, DANIEL L.	HILLMAN DANIEL L	

Payment status

Date	Payment status	Description
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Litigation

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US Patent Issued to Conversant Intellectual Property Management on July 15 for "Power managers for an integrated circuit" (California Inventors)

US Fed News

July 15, 2014 Tuesday 11:27 PM EST

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Length: 211 words

Dateline: ALEXANDRIA, Va.

... Body

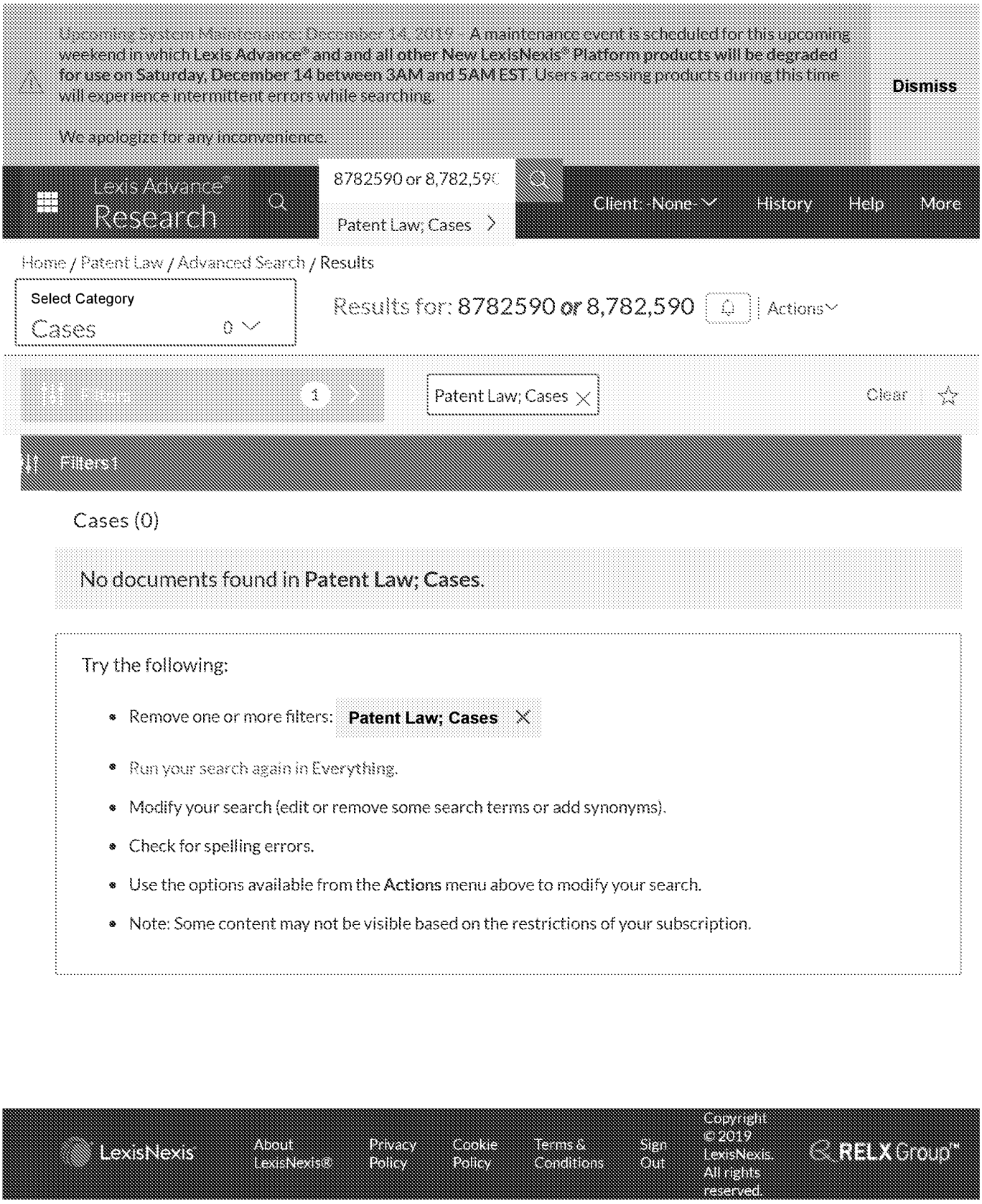
ALEXANDRIA, Va., July 15 -- United States Patent no. ***8,782,590***, issued on July 15, was assigned to Conversant Intellectual Property Management Inc. (Ottawa).

"Power managers for an integrated circuit" was invented by Barry Alan Hoberman (Cupertino, Calif.), Daniel L. Hillman (San Jose, Calif.) and Jon Shiell (San Jose, Calif.). According to the abstract* released ...

... operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands." The patent was filed on June 20, 2011, under Application No. 13/164,362. *For further information, including images, charts and tables, please visit: http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&p=1&u=%2Fnetahtml%2FPTO%2Fsearch-bool.html&r=1&f=G&l=50&co1=AND&d=PTXT&s1=8782590&OS=8782590&RS=8782590 For any query with respect to this article or any other content requirement, please contact Editor at htsyndication@hindustantimes.com

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US7996811B2 - Power managers for an integrated circuit

Granted

Last viewed: December 12 2019, 02:40 PM

Bibliographic information

Publication number and date
US7996811B2 08/09/2011
Granted

Application number and date
US12332529 12/11/2008

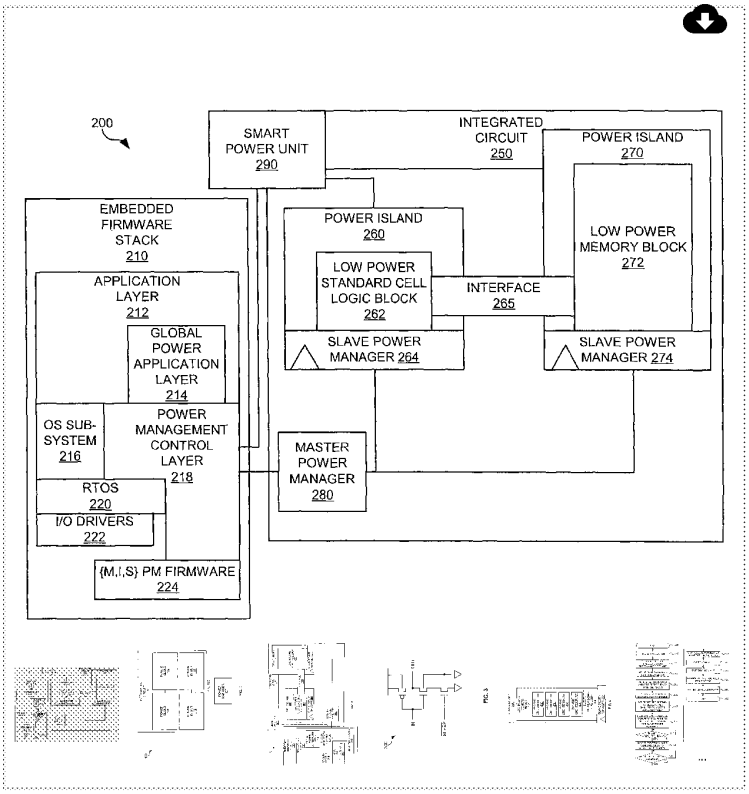
Priority number and date
US12332529 12/11/2008

Original assignee
MOSAID Technologies Incorporated

Current assignee
VIRTUAL SILICON TECHNOLOGY, INC.

Inventor
Barry Alan Hoberman

Legal representative
Hamilton, Brook, Smith & Reynolds, P.C.



Abstract

A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

Description

.7. The system as claimed in wherein the internal regulator is configured to be controlled by the power manager.

.8. The system as claimed in wherein the at least one of the power islands is configured to have the one of plural threshold voltages selected during operation of the integrated circuit.

.9. The system as claimed in wherein the integrated circuit is configured to have the supply voltage changed by regulation of a voltage provided to the at least one of the power islands from a source

Total of 100% of claims loaded.

Classifications

IPC

G06F17/50
G06F9/45
H01L

CPC

H03K3/012
G06F1/3203
G06F1/324
G06F1/3296
H01L2924/00
H01L2924/0002
H02J4/00
Y02D10/126
Y02D10/172
Y02D50/20

Families

INPADOC (https://worldwide.espacenet.com/publi CC=US&NR=7996811B2&KC=B2&FT=D&N

This section contains all family relations of this particular document. For more information about the different families please refer to the Manual (Glossary/Families).

(https://worldwide.espacenet.com/publicationDetails/inpadocPatentFamily?CC=US&NR=7996811B2&KC=B2&FT=D&ND=&date=20110809&DB=&locale=)

Extended (51)	Complete (2)	Main (2)	Domestic (2)	Application number	Pu

Non-patent literature

Nowka, et al., "A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling," IEEE Journal of Solid-State Circuits , vol. 37, No. 11, pp. 1441-1447 (Nov. 2002). (http://www.scopus.com/record/display.url?eid=2-s2.0-0036858657&origin=inward)
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Notice of Allowance dated Feb. 17, 2011 for U.S. Appl. No. 12/176,645.
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Notice of Allowance dated Mar. 31, 2011 for U.S. Appl. No. 12/176,645.
"Solving the Power Management Dilemma in System-On-Chip ASIC Design," Apr. 2002, IBM Technology Group.

Persons

Original Assignees

Original	Standardized	Normalized
MOSAID Technologies Incorporated Ottawa, Ontario, Canada, CA	MOSAID TECHNOLOGIES	MOSAID

Current Assignees

Original	Standardized	Normalized
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CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP

Inventor(s)

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Legal representative(s)

Original	Standardized	Normalized
Hamilton, Brook, Smith & Reynolds, P.C.		

Legal information

Status

Event	Date
Granted	08/09/2011
Filed	12/11/2008

Ownership

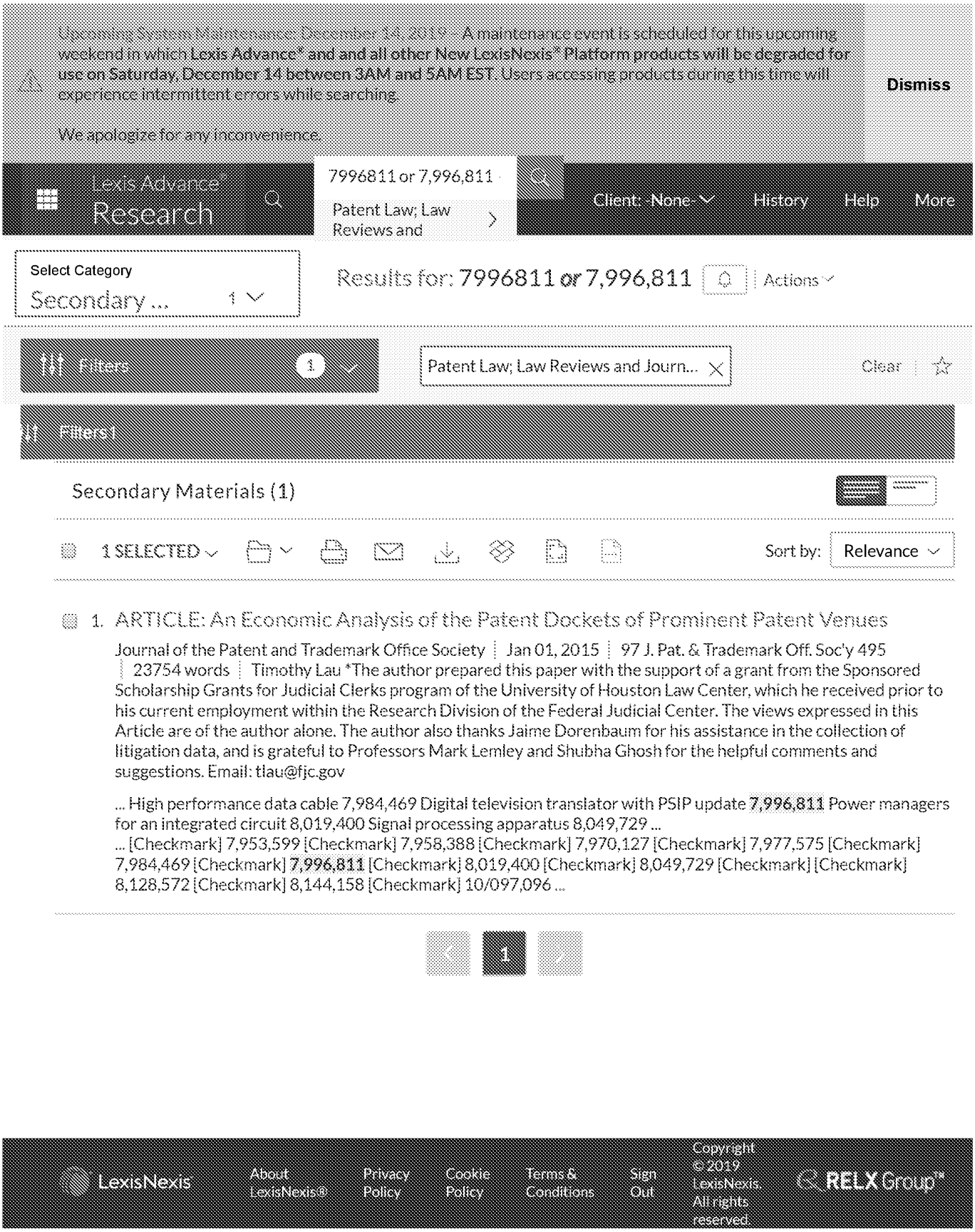
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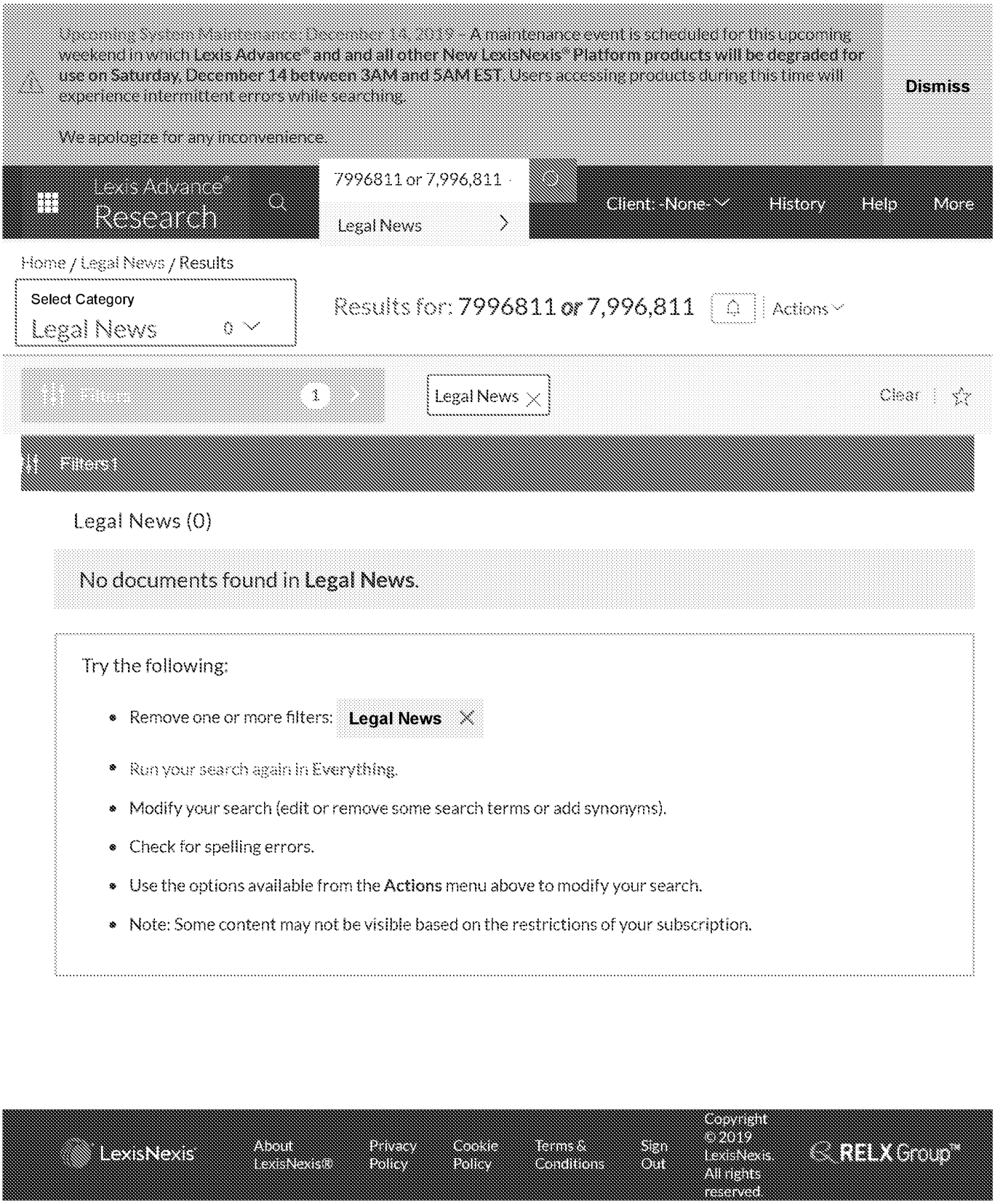
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01/21/2015	Fee paid	PAYMENT OF MAINTENANCE FEE, 4TH YEAR, LARGE ENTITY.

Litigation

Date	Docket number	Comments	Judgement
02/26/2015	2:15cv281	Conversant Intellectual Property Management, Inc. et al v. Samsung Electronics Co., Ltd. et al, Filed February 26, 2015, D.C. E.D. Texas, Doc. No. 2:15cv281	
11/05/2012	6:12cv845	Mosaid Technologies Inc. v. St-Ericsson, Inc., Filed November 5, 2012, D.C. E.D. Texas, Doc. No. 6:12cv845	


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Journal of the Patent and Trademark Office Society | Jan 01, 2015 | 97 J. Pat. & Trademark Off. Soc'y 495 | 23754 words | Timothy Lau *The author prepared this paper with the support of a grant from the Sponsored Scholarship Grants for Judicial Clerks program of the University of Houston Law Center, which he received prior to his current employment within the Research Division of the Federal Judicial Center. The views expressed in this Article are of the author alone. The author also thanks Jaime Dorenbaum for his assistance in the collection of litigation data, and is grateful to Professors Mark Lemley and Shubha Ghosh for the helpful comments and suggestions. Email: tlau@fjc.gov
... High performance data cable 7,984,469 Digital television translator with PSIP update 7,996,811 Power managers for an integrated circuit 8,019,400 Signal processing apparatus 8,049,729 ...
... [Checkmark] 7,953,599 [Checkmark] 7,958,388 [Checkmark] 7,970,127 [Checkmark] 7,977,575 [Checkmark] 7,984,469 [Checkmark] 7,996,811 [Checkmark] 8,019,400 [Checkmark] 8,049,729 [Checkmark] [Checkmark] 8,128,572 [Checkmark] 8,144,158 [Checkmark] 10/097,096 ...
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Results for: **7996811 or 7,996,811 -**

Cases

1. Mosaid Techs., Inc. v. Freescale Semiconductor, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Apr 29, 2013 | 2013 U.S. Dist. LEXIS 60866

... 5,577,230; 5,724,505; 5,958,036 ; 6,141,762; 6,256,725; 7,051,306 ; 7,415,680; 7,945,885; AND **7,996,811** This claim construction opinion construes the disputed claim terms in United ...
... 6,256,725 ; 7,051,306 ; 7,415,680 ; 7,945,885 ; and **7,996,811** , as asserted in the above captioned case. A Markman hearing ...

2. Conversant Intellectual Prop. Mgmt. v. Xilinx, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Jan 09, 2015 | 2015 U.S. Dist. LEXIS 2374

... 7,051,306 ("the '306 Patent") , 7,945,885 ("the '885 Patent") , and **7,996,811** ("the '811 Patent") . STMicroelectronics, Inc. is the only remaining Defendant. ...
... States Patents No. 5,577,230 , 5,968,036 , 7,051,306 , 7,945,885 , **7,996,811** . Plaintiff filed an opening brief (Doc. No. 115), Defendant filed ...
... DISPUTED TERMS IN U.S. PATENTS NO. 7,051,306 , 7,945,885 , AND **7,996,811** A. "power island(s)" B. "power manager" C. "power consumption signals indicating ...
... DISPUTED TERMS IN U.S. PATENTS NO. 7,051,306 , 7,945,885 , AND **7,996,811** The '306 Patent , titled "Managing Power on Integrated Circuits Using ...

3. Mosaid Techs., Inc. v. Freescale Semiconductor, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Sep 27, 2012 | 2012 U.S. Dist. LEXIS 189803

... infringement of U.S. Patent Nos. 7,015,306 ; 7,415,680 ; 7,945,885 ; **7,996,811** ; 5,577,230 ; 5,724,505 ; 5,958,036 ; 6,141,762 ; and ...
... the claims of the 7,945, 885 ("the '885 Patent ") and **7,996,811** ("the '811 Patent ") were unenforceable due to inequitable conduct. Docket ...

US Patent Issued to MOSAID Technologies Incorporated on AUG 09 for "Power managers for an integrated circuit".

US Official News

August 16, 2011

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... Body

ALEXANDRIA, Va: United States Patent no. ***7,996,811***, issued on AUG 09, was assigned to MOSAID Technologies Incorporated.

"Power managers for an integrated circuit" was invented by Hoberman; Barry Alan (Cupertino, CA), Hillman; Daniel L. (San Jose, CA), Shiell; Jon (San Jose, CA).

According to the abstract released by the U.S. Patent & Trademark ...

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US7945885B2 - Power managers for an integrated circuit

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Bibliographic information

Publication number and date
US7945885B2 05/17/2011
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Application number and date
US12176645 07/21/2008

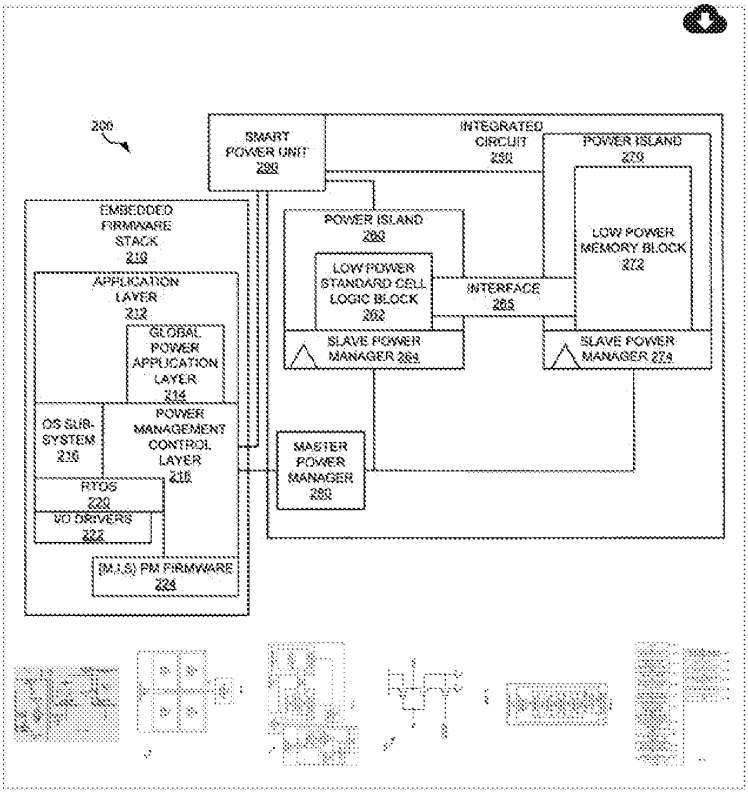
Priority number and date
US12176645 07/21/2008

Original assignee
MOSAID Technologies Incorporated

Current assignee
VIRTUAL SILICONTECHNOLOGY, INC.

Inventor
Barry Alan Hoberman

Legal representative
Hamilton, Brook, Smith & Reynolds, P.C.



Abstract

A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 11/336,097 filed on Jan. 20, 2006 entitled "Power Managers for an Integrated Circuit" and which issued on Aug. 19, 2008 as U.S. Pat. No. 7,415,680, which is a continuation of U.S. application Ser. No. 10/840,893 filed on May 7, 2004 and entitled "Managing Power on Integrated Circuits Using Power Islands" and which issued on May 23, 2006 as U.S. Pat. No. 7,051,306 which claims the benefit of U.S. Provisional Application Ser. No. 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which are each hereby incorporated by reference.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present invention relates generally to integrated circuits, and more particularly to managing power on integrated circuits using power islands.

[0004] 2. Description of the Prior Art

[0005] One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heat dissipation of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

[0006] Some integrated circuits are designed using building blocks of library cells. These library cells are blocks of circuitry performing a function. Some examples of library cells are NAND gates, multiplexers, decoders, comparators, and memory.

Total of 100% of description loaded.

Claims

.1. An integrated circuit comprising: an integrated circuit chip; a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency; one or more power consumption signals indicating one or more of the power consumptions; a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

.2. The integrated circuit as claimed in wherein the power management software is embedded firmware in the integrated circuit.

.3. The integrated circuit as claimed in wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

.4. The integrated circuit as claimed in wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

.5. The integrated circuit as claimed in wherein each of the power consumptions is further controlled by stopping a clock.

.6. The integrated circuit as claimed in wherein stopping the clock comprises clock gating.

.7. The integrated circuit as claimed in wherein the one or more power consumption signals include temperature or power dissipation measurement.

.8. An integrated circuit comprising: an integrated circuit chip; a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency and one or more power

Total of 100% of claims loaded.

Classifications

IPC

G06F17/50
G06F9/45
H01L

CPC

H03K3/012
G06F1/3203
G06F1/324
G06F1/3296
H01L2924/00
H01L2924/0002
H02J4/00
Y02D10/126
Y02D10/172
Y02D50/20

Families

INPADOC (https://worldwide.espacenet.com/publi CC=US&NR=7945885B2&KC=B2&FT=D&N

This section contains all family relations of this particular document. For more information about the different families please refer to the Manual (Glossary/Families).

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Extended (51)	Complete (2)	Main (2)	Domestic (2)	Application number	Pu

Extended (51)	Complete (2)	Main (2)	Domestic (2)	Application number	Pul
05/07/2003 Priority claims EP1623349 IN3310CHENP2005 IN4762CHENP2008 US10840893 US11336097 US12176645 US12332529 US13164362 US13473129 US14324297 US14865905 US15490557 US16226917 US60468742	12/20/2018 Priority claims US10840893 US11336097 US12176645 US12332529 US13164362 US14324297 US14865905 US15490557 US16226917 US60468742	12/20/2018 Priority claims US10840893 US11336097 US12176645 US12332529 US13164362 US14324297 US14865905 US15490557 US16226917 US60468742	12/20/2018	16226917 US16226917	US
	04/18/2017 Priority claims US10840893 US11336097 US12176645 US12332529 US13164362 US14324297 US14865905 US15490557 US60468742	04/18/2017 Priority claims US10840893 US11336097 US12176645 US12332529 US13164362 US14324297 US14865905 US15490557 US60468742	04/18/2017	15490557 US15490557	US
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				15490557 US15490557	US

Citations

Citation	Authority	Normalized number	Application date	Publication number	Publication date
backward	US	5778237	12/14/1995	US5778237A	07/07/1998
backward	US	5996084	01/17/1997	US5996084A	11/30/1999
backward	US	6307281	08/24/1999	US6307281B1	10/23/2001
backward	US	6438635	07/24/1998	US6438635B1	08/20/2002
backward	US	6462976	03/02/2000	US6462976B1	10/08/2002

Non-patent literature

Nowka, et al., "A 0.9V to 1.95V Dynamic Voltage-Scalable and Frequency-Scalable 32b PowerPC Processor," IEEE International Solid-State Circuits Conference 20.4 (Feb. 6, 2002).
"Solving the Power Management Dilemma in System-On-Chip ASIC Design," Apr. 2002, IBM Technology Group.
Lackey et al., "Managing Power and Performance for System-on-Chip Designs using Voltage Islands," IEEE International Conference on Computer Aided Design, Technical Paper, Nov. 2002, pp. 195-202.
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Li, L. et al., "Managing Leakage Energy in Cache Hierarchies," Journal of Instruction-Level Parallelism,

Persons

Original Assignees

Original	Standardized	Normalized
MOSAID Technologies Incorporated Ottawa, Ontario, Canada, CA	MOSAID TECHNOLOGIES	MOSAID

Current Assignees

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CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP

Inventor(s)

Original
Barry Alan Hoberman Cupertino, California, United States of America, US
Daniel L. Hillman San Jose, California, United States of America, US
Jon Shiell San Jose, California, United States of America, US

Legal representative(s)

Original	Standardized	Normalized
Hamilton, Brook, Smith & Reynolds, P.C.		

Legal information

Status

Event	Date
Granted	05/17/2011
Filed	07/21/2008

Ownership

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08/20/2014		CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP
01/01/2014	08/20/2014	CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP
08/01/2008	01/01/2014	MOSAID TECHNOLOGIES INCORPORATED	MOSAID TECHNOLOGIES	MOSAID
07/21/2008	01/01/2014	MOSAID TECHNOLOGIES INCORPORATED	MOSAID TECHNOLOGIES	MOSAID
11/15/2005	08/01/2008	MOSAID TECHNOLOGIES CORPORATION	MOSAID TECHNOLOGIES	MOSAID
10/07/2005	11/15/2005	MOSAID DELAWARE, INC.	MOSAID	MOSAID
08/04/2004	08/04/2004	SHIELL, JON	SHIELL JON	
07/29/2004	07/29/2004	HOBERMAN, BARRY ALAN	HOBERMAN BARRY ALAN	
07/29/2004		VIRTUAL SILICONTECHNOLOGY, INC.	VIRTUAL SILICONTECHNOLOGY	
07/28/2004	07/28/2004	HILLMAN, DANIEL L.	HILLMAN DANIEL L	

Payment status

Date	Payment status	Description
11/01/2018	Fee paid	PAYMENT OF MAINTENANCE FEE, 8TH YEAR, LARGE ENTITY.
10/22/2014	Fee paid	PAYMENT OF MAINTENANCE FEE, 4TH YEAR, LARGE ENTITY.

Litigation

Date	Docket number	Comments	Judgement

Date	Docket number	Comments	Judgement
02/26/2015	2:15cv281	Conversant Intellectual Property Management, Inc. et al v. Samsung Electronics Co., Ltd. et al, Filed February 26, 2015, D.C. E.D. Texas, Doc. No. 2:15cv281	
11/05/2012	6:12cv845	Mosaid Technologies Inc. v. St-Ericsson, Inc., Filed November 5, 2012, D.C. E.D. Texas, Doc. No. 6:12cv845	

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Results for: **7945885 or 7,945,885**

News

1. MOSAID Technologies Assigned Patent

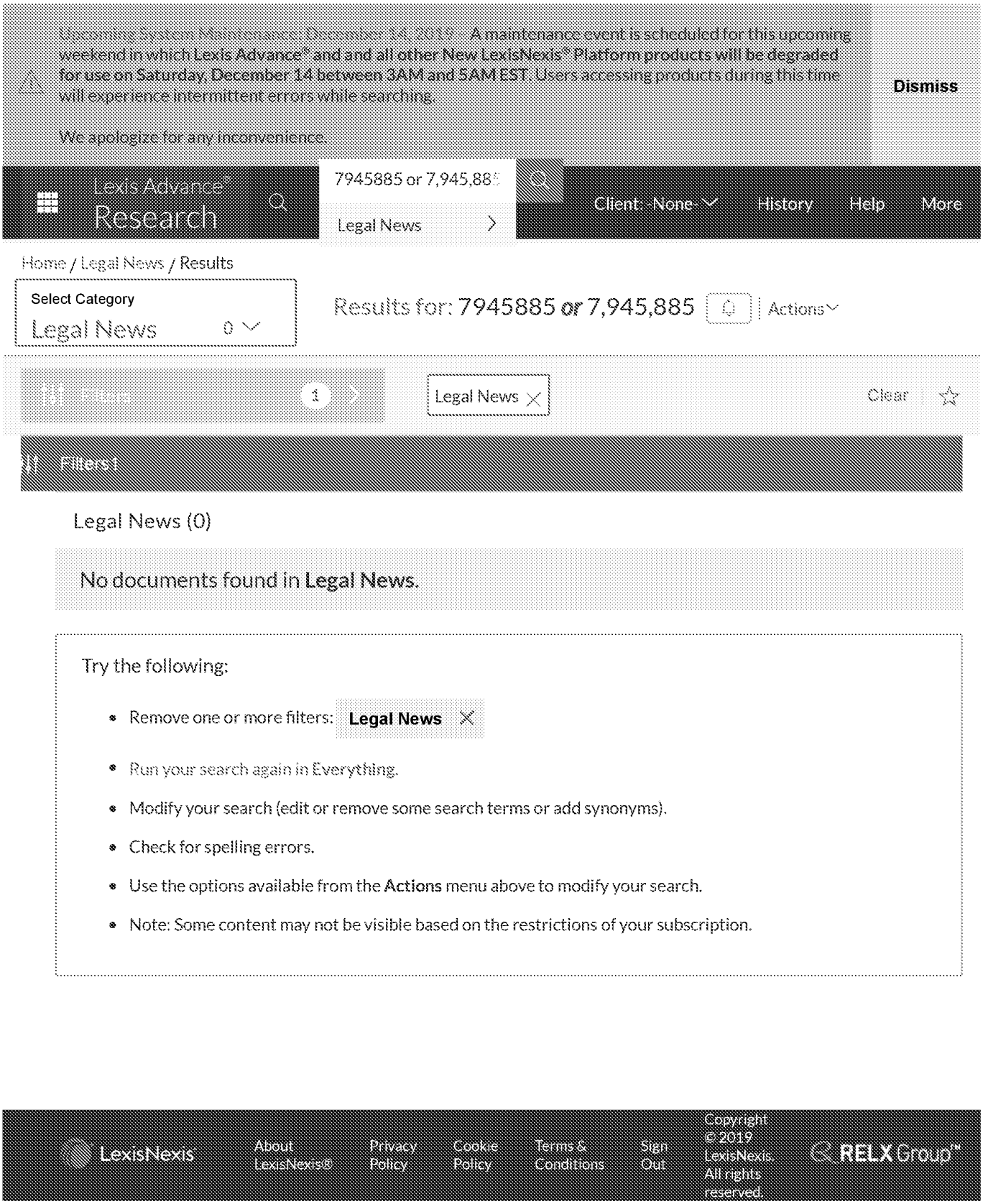
Targeted News Service | May 18, 2011 | 214 | Targeted News Service

... (12/176,645). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&p=1&u=%2Fnetahtml%2FPTO%2Fsearch-bool.html&r=1&f=G&l=50&co1=AND&d=PTXT&s1= **7945885**.PN.&OS=PN/**7945885**&RS=PN/**7945885** Written by Kusum Sangma; edited by Jaya Anand. For more information ...
... -- MOSAID Technologies , Ottawa, has been assigned a patent (**7,945,885**) developed by Barry Alan Hoberman, Cupertino , Calif. , Daniel ...

2. US Patent Issued to MOSAID Technologies on May 17 for "Power Managers for an Integrated Circuit" (California Inventors)

US Fed News | May 20, 2011 | 201

... 2008, under Application No. 12/176,645. For further information please visit: http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&p=1&u=%2Fnetahtml%2FPTO%2Fsearch-bool.html&r=1&f=G&l=50&co1=AND&d=PTXT&s1= **7945885**&OS=**7945885**&RS=**7945885** For any query with respect to this article or any other ...
... Va. , May 20 -- United States Patent no. **7,945,885** , issued on May 17, was assigned to MOSAID Technologies Inc. ...


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Results for: 7945885 or 7,945,885
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Cases (3)

7945885 or 7,945,885

Sort by: Relevance

1. Mosaid Techs., Inc. v. Freescale Semiconductor, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Apr 29, 2013 | 2013 U.S. Dist. LEXIS 60866

Opinions

Terms: Opinion

... 6,141,762 ; 6,256,725 ; 7,051,306 ; 7,415,680 ; 7,945,885 ; and 7,996,811 , as asserted in the above captioned case. A ...

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2. Conversant Intellectual Prop. Mgmt. v. Xilinx, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Jan 09, 2015 | 2015 U.S. Dist. LEXIS 2374

Opinions

Terms: Opinion

... (" the '036 Patent "), 7,051,306 ("the '306 Patent") , 7,945,885 ("the '885 Patent") , and 7,996,811 ("the '811 Patent") . STMicroelectronics, Inc. is the only remaining Defendant....

View this passage in full document

3. Mosaid Techs., Inc. v. Freescale Semiconductor, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Sep 27, 2012 | 2012 U.S. Dist. LEXIS 189803

Opinions

Terms: Opinion

... and Interphase Corporation, alleging infringement of U.S. Patent Nos. 7,015,306 ; 7,415,680 ; 7,945,885 ; 7,996,811 ; 5,577,230 ; 5,724,505 ; 5,958,036 ; ...

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Results for: **7945885 or 7,945,885**

Secondary Materials

1. ARTICLE: An Economic Analysis of the Patent Dockets of Prominent Patent Venues

Journal of the Patent and Trademark Office Society | Jan 01, 2015 | 97 J. Pat. & Trademark Off. Soc'y 495 | 23754 | Timothy Lau *The author prepared this paper with the support of a grant from the Sponsored Scholarship Grants for Judicial Clerks program of the University of Houston Law Center, which he received prior to his current employment within the Research Division of the Federal Judicial Center. The views expressed in this Article are of the author alone. The author also thanks Jaime Dorenbaum for his assistance in the collection of litigation data, and is grateful to Professors Mark Lemley and Shubha Ghosh for the helpful comments and suggestions. Email: tlau@fjc.gov

... television translator with PSIP update 7,812,828 Ellipse fitting for multi-touch surfaces **7,945,885** Power managers for an integrated circuit 7,953,599 System, method and computer ...
... [Checkmark] 7,746,321 [Checkmark] [Checkmark] 7,756,129 [Checkmark] [Checkmark] 7,761,893 [Checkmark] 7,812,828 [Checkmark] **7,945,885** [Checkmark] 7,953,599 [Checkmark] 7,958,388 [Checkmark] 7,970,127 [Checkmark] 7,977,575 [Checkmark] 7,984,469 [Checkmark] ...

US7415680B2 - Power managers for an integrated circuit

Granted

Last viewed: December 12 2019, 03:42 PM

Bibliographic information

Publication number and date
US7415680B2 08/19/2008

Granted

Application number and date
US11336097 01/20/2006

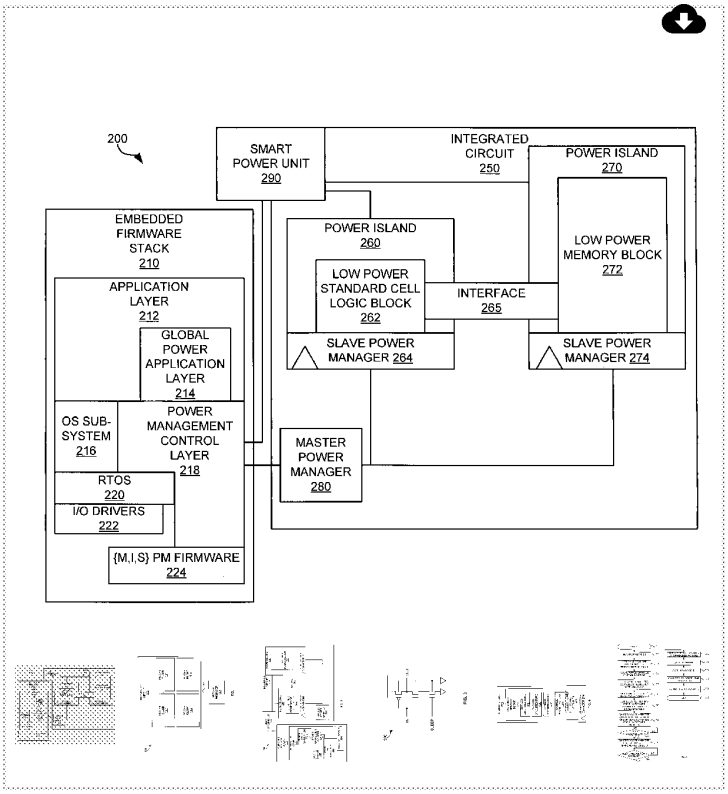
Priority number and date
US11336097 01/20/2006

Original assignee
MOSAID Technologies Corporation

Current assignee
VIRTUAL SILICONTECHNOLOGY, INC.

Inventor
Barry Alan Hoberman

Legal representative
Dennis R. Haszko



Abstract

A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

Description

change the second power consumption for the one of the power islands.

.8. The system of wherein the second power manager is configured to collect information from components of the one of the power islands.

.9. The system of wherein the second power manager is configured to determine whether the second power consumption crosses a threshold.

Total of 100% of claims loaded.

Classifications

IPC

G06F17/50
G06F9/45
H01L

CPC

H03K3/012
G06F1/3203
G06F1/324
G06F1/3296
H01L2924/00
H01L2924/0002
H02J4/00
Y02D10/126
Y02D10/172
Y02D50/20

Families

INPADOC (https://worldwide.espacenet.com/pub
CC=US&NR=7415680B2&KC=B2&FT=D&

This section contains all family relations of this particular document. For more information about the different families please refer to the Manual (Glossary/Families).

(https://worldwide.espacenet.com/publicationDetails/inpadocPatentFamily?CC=US&NR=7415680B2&KC=B2&FT=D&ND=&date=20080819&DB=&locale=)

Extended (51)	Complete (2)	Main (2)	Domestic (2)	Application number

Non-patent literature

"Solving the Power Management Dilemma in System-On-Chip ASIC Design", Apr. 2002, IBM Technology Group.
Lackey et al.,"Managing Power and Performance for System-on-Chip Designs using Voltage Islands", Nov. 2002, IEEE International Conference on Computer Aided Design, Technical Paper pp. 195-202.
Semeraro et al., "Dynamic Frequency and Voltage Control for Multiple Clock Domain Microarchitecture", Nov. 2002, 35 th Annual IEEE/ACM International Symposium on Microarchitecture, Proceedings pp. 356-367.

Persons

Original Assignees

Original	Standardized	Normalized
MOSAID Technologies Corporation Sunnyvale, California, United States of America, US	MOSAID TECHNOLOGIES	MOSAID

Current Assignees

Original	Standardized	Normalized
VIRTUAL SILICONTECHNOLOGY, INC.	VIRTUAL SILICONTECHNOLOGY	
CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP

Inventor(s)

Original
Barry Alan Hoberman Cupertino, California, United States of America, US
Daniel L. Hillman San Jose, California, United States of America, US
Jon Shiell San Jose, California, United States of America, US

Legal representative(s)

Original	Standardized	Normalized
Dennis R. Haszko		

Legal information

Status

Event	Date
Granted	08/19/2008
Filed	01/20/2006

Ownership

Date from	Date to	Name	Standardized	Normalized
08/20/2014		CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP
01/01/2014	08/20/2014	CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP
05/05/2010	01/01/2014	MOSAID TECHNOLOGIES INCORPORATED	MOSAID TECHNOLOGIES	MOSAID
02/09/2009	01/01/2014	MOSAID TECHNOLOGIES INCORPORATED	MOSAID TECHNOLOGIES	MOSAID
01/20/2006	05/05/2010	MOSAID TECHNOLOGIES CORPORATION	MOSAID TECHNOLOGIES	MOSAID
01/20/2006	01/01/2014	MOSAID TECHNOLOGIES INCORPORATED	MOSAID TECHNOLOGIES	MOSAID
11/15/2005	11/15/2005	MOSAID DELAWARE, INC.	MOSAID	MOSAID
11/15/2005	05/05/2010	MOSAID TECHNOLOGIES CORPORATION	MOSAID TECHNOLOGIES	MOSAID
10/07/2005	11/15/2005	MOSAID DELAWARE, INC.	MOSAID	MOSAID
07/29/2004		VIRTUAL SILICONTECHNOLOGY, INC.	VIRTUAL SILICONTECHNOLOGY	

Payment status

Date	Payment status	Description
02/03/2016	Fee paid	PAYMENT OF MAINTENANCE FEE, 8TH YEAR, LARGE ENTITY.
09/20/2011	Fee paid	PAYMENT OF MAINTENANCE FEE, 4TH YEAR, LARGE ENTITY.

Litigation

Date	Docket number	Comments	Judgement
01/09/2012	6:12cv8	Arm Ltd. et al v. Mosaid Technologies, Inc., Filed January 9, 2012, D.C. E.D. Texas, Doc. No. 6:12cv8	
08/05/2011	4:11cv3869	ARM Ltd et al v. Mosaid Technologies, Inc, Filed August 5, 2011, D.C. N.D. California, Doc. No. 4:11cv3869	
08/05/2011	3:11cv3869	Arm Ltd. et al v. Mosaid Technologies, Inc., Filed August 5, 2011, D.C. N.D. California, Doc. No. 3:11cv3869	

Date	Docket number	Comments	Judgement
04/07/2011	6:11cv173	Mosaid Technologies Inc. v. Freescale Semiconductor, Inc. et al, Filed April 7, 2011, D.C. E.D. Texas, Doc. No. 6:11cv173	

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Secondary Materials (1)

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1. ARTICLE: An Economic Analysis of the Patent Dockets of Prominent Patent Venues

Journal of the Patent and Trademark Office Society | Jan 01, 2015 | 97 J. Pat. & Trademark Off. Soc'y 495 | 23754 words | Timothy Lau *The author prepared this paper with the support of a grant from the Sponsored Scholarship Grants for Judicial Clerks program of the University of Houston Law Center, which he received prior to his current employment within the Research Division of the Federal Judicial Center. The views expressed in this Article are of the author alone. The author also thanks Jaime Dorenbaum for his assistance in the collection of litigation data, and is grateful to Professors Mark Lemley and Shubha Ghosh for the helpful comments and suggestions. Email: tlau@fjc.gov

... method 7,415,530 System and methods for accelerated data storage and retrieval 7,415,680 Power managers for an integrated circuit Industry 2013 Litigation Data* Classification ...
... [Checkmark] 7,349,540 [Checkmark] 7,352,300 [Checkmark] 7,353,367 [Checkmark] 7,397,363 [Checkmark] 7,415,530 [Checkmark] 7,415,680 [Checkmark] Industry Classification & Patent Data BEA BEA Title Code & ...

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U.S. Patents Awarded to Inventors in California (Aug. 21)

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... first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands."

The inventors were issued U.S. Patent No. ***7,415,680*** on Aug. 19.

The patent has been assigned to MOSAID Technologies Corp., Sunnyvale, Calif.

The original application was filed on Jan. 20, 2006, and is available at: http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=7,415,680.PN.&OS=PN/7,415,680&RS=PN/7,415,680.

***

California Inventor Develops Ornamental Design for Heel-Toe Shifter

ALEXANDRIA, Va., Aug. 21 -- Fred M. Huston of Simi Valley, Calif., has developed an ornamental design for a heel-toe shifter, the U.S. Patent & Trademark Office announced.

The inventor was issued U.S. Patent No. D575,038 on Aug. ...

End of Document

Inventors Develop Integrated Circuit Power Manager

US Fed News

August 21, 2008 Thursday 1:00 AM EST

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Length: 204 words

Byline: US Fed News

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... first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands."

The inventors were issued U.S. Patent No. ***7,415,680*** on Aug. 19.

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The original application was filed on Jan. 20, 2006, and is available at: *http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=7,415,680.PN.&OS=PN/7,415,680&RS=PN/7,415,680*.

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Cases (3)

7415680 or 7,415,680

Sort by: Relevance

1. Mosaid Techs., Inc. v. Freescale Semiconductor, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Apr 29, 2013 | 2013 U.S. Dist. LEXIS 60866

Opinions

Terms: Opinion

... 5,958,036 ; 6,141,762 ; 6,256,725 ; 7,051,306 ; 7,415,680 ; 7,945,885 ; and 7,996,811 , as asserted in the above captioned case. A ...

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2. Conversant Intellectual Prop. Mgmt. v. Xilinx, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Jan 09, 2015 | 2015 U.S. Dist. LEXIS 2374

Opinions

Terms: Opinion

... first power manager and manages a second power consumption for one of the power islands. The '885 Patent is a continuation of United States Patent No. 7,415,680 ("the '680 Patent") , which in turn is a continuation of the ...

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3. Mosaid Techs., Inc. v. Freescale Semiconductor, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Sep 27, 2012 | 2012 U.S. Dist. LEXIS 189803

Opinions

Terms: Opinion

... and Interphase Corporation, alleging infringement of U.S. Patent Nos. 7,015,306 ; 7,415,680 ; 7,945,885 ; 7,996,811 ; 5,577,230 ; 5,724,505 ; ...

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US7051306B2 - Managing power on integrated circuits using power islands

Granted

Last viewed: December 12 2019, 04:24 PM

Bibliographic information

Publication number and date
US7051306B2 05/23/2006

Granted

Application number and date
US10840893 05/07/2004

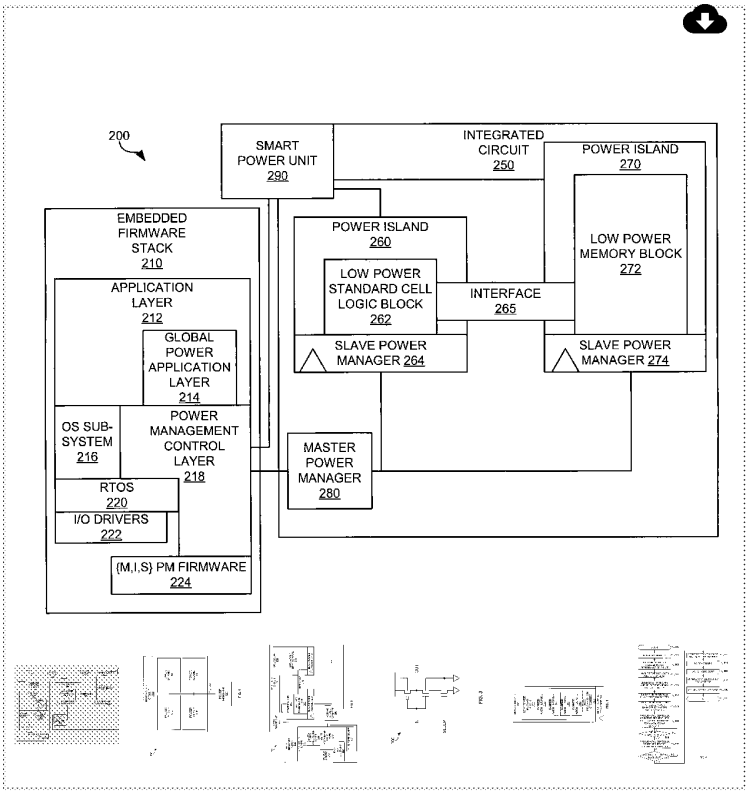
Priority number and date
US10840893 05/07/2004

Original assignee
MOSAID Technologies Corporation

Current assignee
VIRTUAL SILICON TECHNOLOGY, INC.

Inventor
Barry Alan Hoberman

Legal representative
Carr & Ferrell LLP



Abstract

Systems and methods manage power in an integrated circuit using power islands. The integrated circuit includes a plurality of power islands where power consumption is independently controlled within each of the power islands. A power manager determines a target power level for one of the power islands. The power manager then determines an action to change a consumption power level of the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level.

Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application Ser. No. 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which is hereby incorporated by reference.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present invention relates generally to integrated circuits, and more particularly to managing power on integrated circuits using power islands.

[0004] 2. Description of the Prior Art

[0005] One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heat dissipation of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

[0006] Some integrated circuits are designed using building blocks of library cells. These library cells are blocks of circuitry performing a function. Some examples of library cells are NAND gates, multiplexers, decoders, comparators, and memory.

[0007] In a "full-custom" flow, the integrated circuit is designed at the lowest level such as at the individual transistors, capacitors, and resistors level. The "full-custom" flow may use library cells that are internally developed. The integrated circuit can have optimal performance because the integrated circuit is designed in great detail at the lowest level. However, some problems with the "full-custom" flow are the long time and expensive costs associated with designing at such a detailed level. Furthermore, the

Total of 100% of description loaded.

Claims

.1. A method of managing power on an integrated circuit including a plurality of power islands, the method comprising: determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands; determining at least one of actions to change a power consumption level of the one of the power islands to the target power level; and performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.

.2. The method of wherein the power islands are delineated based on geographic factors of the integrated circuit.

.3. The method of wherein the power islands are delineated based on functional circuitry of the integrated circuit.

.4. The method of wherein the power islands comprise power sub-islands.

.5. The method of wherein the power islands comprises multiple clock domains.

.6. The method of wherein another one of the actions comprises selecting a clock for the one of the power islands.

.7. The method of wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

.8. The method of wherein the first voltage comprises a source voltage.

.9. The method of wherein the first voltage comprises a threshold voltage.

.10. The method of wherein another one of the actions comprises powering on the one of the power islands.

Total of 100% of claims loaded.

Classifications

IPC

G06F17/50
G06F9/45
H01L

CPC

H03K3/012
G06F1/3203
G06F1/324
G06F1/3296
H01L2924/00
H01L2924/0002
H02J4/00
Y02D10/126
Y02D10/172
Y02D50/20

Families

INPADOC (https://worldwide.espacenet.com/publi
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This section contains all family relations of this particular document. For more information about the different families please refer to the Manual (Glossary/Families).

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Extended (51)	Complete (2)	Main (2)	Domestic (2)	Application number	Pu

Extended (51)	Complete (2)	Main (2)	Domestic (2)	Application number	Pul
05/07/2003 Priority claims EP1623349 IN3310CHENP2005 IN4762CHENP2008 US10840893 US11336097 US12176645 US12332529 US13164362 US13473129 US14324297 US14865905 US15490557 US16226917 US60468742	12/20/2018 Priority claims US10840893 US11336097 US12176645 US12332529 US13164362 US14324297 US14865905 US15490557 US16226917 US60468742	12/20/2018 Priority claims US10840893 US11336097 US12176645 US12332529 US13164362 US14324297 US14865905 US15490557 US16226917 US60468742	12/20/2018	16226917 US16226917	US
	04/18/2017 Priority claims US10840893 US11336097 US12176645 US12332529 US13164362 US14324297 US14865905 US15490557 US60468742	04/18/2017 Priority claims US10840893 US11336097 US12176645 US12332529 US13164362 US14324297 US14865905 US15490557 US60468742	04/18/2017	15490557 US15490557	US
				15490557 US15490557	US

Citations

Citation	Authority	Normalized number	Application date	Publication number	Publication date
backward	US	6462976	03/02/2000	US6462976B1	10/08/2002
backward	US	6598148	07/29/1998	US6598148B1	07/22/2003
backward	US	6631502	01/16/2002	US6631502B2	10/07/2003
backward	US	6667648	04/23/2002	US6667648B2	12/23/2003
backward	US	6779163	09/25/2002	US6779163B2	08/17/2004

Page: ...

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Persons

Original Assignees

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MOSAID Technologies Corporation Sunnyvale, California, United States of America, US	MOSAID TECHNOLOGIES	MOSAID

Current Assignees

Original	Standardized	Normalized
VIRTUAL SILICON TECHNOLOGY, INC.	VIRTUAL SILICON TECHNOLOGY	
CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP

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Original	Standardized	Normalized

Original	Standardized	Normalized
Carr & Ferrell LLP		

Legal information

Status

Event	Date
Granted	05/23/2006
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Ownership

Date from	Date to	Name	Standardized	Normalized
08/20/2014		CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP
01/01/2014	08/20/2014	CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	CONVERSANT IP	CONVERSANT IP
05/05/2010	01/01/2014	MOSAID TECHNOLOGIES INCORPORATED	MOSAID TECHNOLOGIES	MOSAID
02/09/2009	01/01/2014	MOSAID TECHNOLOGIES INCORPORATED	MOSAID TECHNOLOGIES	MOSAID
11/15/2005	05/05/2010	MOSAID TECHNOLOGIES CORPORATION	MOSAID TECHNOLOGIES	MOSAID
10/07/2005	11/15/2005	MOSAID DELAWARE, INC.	MOSAID	MOSAID
07/29/2004		VIRTUAL SILICON TECHNOLOGY, INC.	VIRTUAL SILICON TECHNOLOGY	
05/07/2004	07/29/2004	HOBERMAN, BARRY ALAN	HOBERMAN BARRY ALAN	
05/07/2004	07/28/2004	HILLMAN, DANIEL L.	HILLMAN DANIEL L	
05/07/2004	08/04/2004	SHIELL, JON	SHIELL JON	
05/07/2004	05/05/2010	MOSAID TECHNOLOGIES CORPORATION	MOSAID TECHNOLOGIES	MOSAID
05/07/2004	01/01/2014	MOSAID TECHNOLOGIES INCORPORATED	MOSAID TECHNOLOGIES	MOSAID

Payment status

Date	Payment status	Description
11/09/2017	Fee paid	PAYMENT OF MAINTENANCE FEE, 12TH YEAR, LARGE ENTITY.
12/03/2013	Fee paid	PAYMENT OF MAINTENANCE FEE, 8TH YEAR, LARGE ENTITY.
10/21/2009	Fee paid	PAYMENT OF MAINTENANCE FEE, 4TH YEAR, LARGE ENTITY.

Litigation

Date	Docket number	Comments	Judgement
11/05/2012	6:12cv848	Conversant Intellectual Property Management Inc v. Stmicroelectronics, Inc., Filed November 5, 2012, D.C. E.D. Texas, Doc. No. 6:12cv848	
11/05/2012	6:12cv846	Mosaid Technologies Inc. v. Nxp Semiconductors Usa, Inc., Filed November 5, 2012, D.C. E.D. Texas, Doc. No. 6:12cv846	
11/05/2012	6:12cv845	Mosaid Technologies Inc. v. St-Ericsson, Inc., Filed November 5, 2012, D.C. E.D. Texas, Doc. No. 6:12cv845	
01/09/2012	6:12cv8	Arm Ltd. et al v. Mosaid Technologies, Inc., Filed January 9, 2012, D.C. E.D. Texas, Doc. No. 6:12cv8	
08/05/2011	4:11cv3869	ARM Ltd et al v. Mosaid Technologies, Inc, Filed August 5, 2011, D.C. N.D. California, Doc. No. 4:11cv3869	
08/05/2011	3:11cv3869	Arm Ltd. et al v. Mosaid Technologies, Inc., Filed August 5, 2011, D.C. N.D. California, Doc. No. 3:11cv3869	
04/07/2011	6:11cv173	Mosaid Technologies Inc. v. Freescale Semiconductor, Inc. et al, Filed April 7, 2011, D.C. E.D. Texas, Doc. No. 6:11cv173	

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Recent patent infringement/false patent marking cases filed in the Eastern District of Texas

Southeast Texas Record

April 12, 2011 Tuesday

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Length: 734 words

Byline: Michelle Massey, East Texas Bureau

... John Ward is assigned to the case.Case No. 2:11-cv-00203Tyler Division April 7<li>Mosaid Technologies Inc. v. Freescale Semiconductor Inc., et al.Mosaid is a Canadian corporation with a place of business in Plano.The defendants are Freescale Semiconductor, Interphase Corp. and NVIDIA Corp.The defendants are accused of infringing on: U.S. Patent No. **7,051,306** issued May 23, 2006, for Managing Power on Integrated Circuits Using Power Islands; U.S. Patent No. 7,415,680 issued Aug. 19, 2008, for Power Managers for an Integrated Circuit;<li>U.S. Patent No. 5,577,230 issued Nov. 19, 1996, for Apparatus and Method for Computer Processing Using an Enhanced Harvard Architecture Utilizing ...

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California Inventors Develop Integrated Circuit Power Management Method

US Fed News

May 25, 2006 Thursday 2:15 PM EST

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Length: 228 words

Byline: US Fed News

Dateline: Alexandria, Va.

... action to change a consumption power level of the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level."

The inventors were issued U.S. Patent No. **7,051,306** on May 23.

The patent has been assigned to MOSAID Technologies Corp., Sunnyvale, Calif.

The original application was filed on May 7, 2004, and is available at: http://patft1.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&p=2&u=%2Fnetahtml%2FPTO%2Fsearch-bool.html&r=65&f=G&l=50&co1=AND&d=PTXT&s1=20060523.PD.&OS=ISD/05/23/2006.

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Cases (2)

7051306 or 7,051,306

1 SELECTED Sort by: Relevance

1. Conversant Intellectual Prop. Mgmt. v. Xilinx, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Jan 09, 2015 | 2015 U.S. Dist. LEXIS 2374

Opinions

Terms: Opinion

... first and second registers" C. "register" CONSTRUCTION OF DISPUTED TERMS IN U.S. PATENTS NO. 7,051,306 , 7,945,885 , AND 7,996,811 A. "power island(s)" B. "power manager"...

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2. Mosaid Techs., Inc. v. Freescale Semiconductor, Inc.

United States District Court for the Eastern District of Texas, Tyler Division | Apr 29, 2013 | 2013 U.S. Dist. LEXIS 60866

Opinions

Terms: Opinion

... MEMORANDUM OPINION AND ORDER CONSTRUING CLAIM TERMS OF UNITED STATES PATENT NOS. 5,577,230; 5,724,505; 5,958,036 ; 6,141,762; 6,256,725; 7,051,306 ; 7,415,680; 7,945,885; AND 7,996,811 This claim construction opinion construes the disputed claim terms in ...

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ARTICLE: An Economic Analysis of the Patent Dockets of Prominent Patent Venues, 97 J. Pat. & Trademark Off. Soc'y 495

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Highlight

Abstract

It is now accepted as an article of faith that patents play a significant role in the national economy and that adjustments to the patent system could lead to improvements in employment. Missing in the discussion is an analysis as to how patents actually relate to the economic activities within the United States.

This article presents a comparison of the patent dockets of the prominent venues of the Eastern District of Texas, the District of Delaware, and the Federal Circuit with the economic and trade data of the nation. The analysis shows that, as a whole, the litigated patents implicate only a small fraction of the economic activities of the United States and involve mainly high-wage earners. The primary effect of U.S. patents actually falls on foreign conduct relating to its regulatory effects on the merchandise imported into the United States.

[*496] I. Introduction

In recent years, there has been growing interest in leveraging the patent system in order to promote employment and improve the economy. [1] In the 2011 State of the Union address, President Obama articulated the following vision:

> The first step in winning the future is encouraging American innovation . . . . What we can do--what America does better than anyone else--is spark the creativity and imagination of our people. We're the nation that put cars in driveways and computers in offices; the nation of Edison and the Wright brothers; of Google and Facebook. In America, innovation doesn't just change our lives. *It is how we make our living.* [2]

This focus on the potential economic benefits of the patent system now permeates justifications for proposals about the patent system. For example, in another 2011 speech, President Obama stated that:

> Through patent reform, we can cut the red tape that stops too many inventors and entrepreneurs from quickly turning new ideas into thriving businesses--*which holds our whole economy back.* [3]

Beneath all of these statements is an assumption that patents really do govern a large, meaningful sector of the U.S. economy. But is that true?

[*497] The vast majority of patents are never enforced. [4] Only a tiny minority reaches litigation, and, even then, only a fraction ever leads to any judicial action. [5] The number of U.S. patents that ever have any actual effect is so low that, as Professor Lemley argues, market participants in what he terms "component industries" generally ignore patents until forced to confront them in a lawsuit. [6]

To the extent then that U.S. patents have any voice on the national economy, it is concentrated within the small chorus of litigated patents, upon which the courts pronounce judgment and articulate the contours of patent law through binding precedents. In this study, we attempt to connect patent litigation data with economics and trade data to identify how patents, as they are used within the United States, relate to economic activities.

II. Methodology

A. Litigation Data Collection

To obtain patent litigation statistics, we first require a database of the patents litigated within the courts. In this study, we focus on the three prominent patent litigation venues of the Eastern District of Texas, the District of Delaware, and the Federal Circuit. We identified the patents and applications litigated in the three courts by conducting searches for orders and opinions on Google Scholar issued between January 1 and November 30 of 2013. [7] For district court data, we used the terms "'judgment as a matter of law' and patent," "'summary judgment' and patent," "12(b)(6) and patent," and "'claim construction and patent." For the Federal Circuit data, we used the term "patent." The patents-in-suit and applications-in-suit were identified either by explicit citation within the documents or through extrinsic research.

Currently, the USPTO maintains a concordance to link the technological classifications it assigns to patents with the NAICS groups. [9] In principle, this concordance **[*498]** should allow for a quick and easy way to sort patents and applications into the proper NAICS group. However, this concordance, the traditional tool for classifying patents by economic sector, is not suitable for the analysis of patent dockets.

The primary problem with the concordance is that it limits patent analysis only to those industries deemed "Manufacturing" within the NAICS scheme. [10] If one seeks to understand the patent prosecution process by studying the source of the underlying intellectual property, then such a concordance may be helpful because an inventor is likely a member of the R&D department of an organization hoping to bring a service or product to market.

But the difficulty of classifying litigated patents only by the "Manufacturing" NAICS categories is illustrated in the case of U.S. Patent No. 6,174,237, entitled "Method for a Game of Skill Tournament." The patent is asserted against Game Show Network and Worldwinner.com for offering an infringing online game on their websites. [11] It does not contribute to an understanding of the patent's place within the overall patent docket and the national economy to force the subject matter of the patent into one of the "Manufacturing" groups, where more appropriate categories outside "Manufacturing" such as "Amusements, Gambling, & Recreation Industries" and "Data Processing, Internet Publishing, & Other Information Services" are available under the NAICS classification system.

In addition, the USPTO's concordance does not provide for the classification of design patents and plant patents. [12] While these patents constitute only a small minority of the patent docket, [13] it is inappropriate to simply ignore them.

Accordingly, we empirically classify each patent we have identified in accordance with Section 2.1 into one NAICS industrial group. In this process, we take into consideration both the claim language and also the identities of the likely and actual defendants.

We note that a certain subjectivity, informed by the author's own experience with the technology, patent litigation, and patent prosecution, is unavoidable. At the outset, the NAICS categories do overlap each other and some patents arguably fall into more than one NAICS category. This problem is most salient within the sectors that the Bureau of Economic Analysis collectively refers to as the "Information-Communications-Technology-Producing Industries." Patents pertaining to these industries typically belong to the NAICS categories of:

. "Computer & Electronic Products";

. "Publishing Industries, except Internet (Includes Software)";

. "Broadcasting & Telecommunications"; and

. "Data Processing, Internet Publishing, & Other Information Services."

The categories reflect the traditional understanding of the industry as divided between these four market players:

[*499] . device maker;

iPhones, and providing maps and music to the iPhones. Furthermore, Apple must cooperate with the carriers to ensure the iPhones could operate on their networks, and, in some ways, behaves as if a carrier. Any patent asserted against Apple for the iPhone therefore could implicate Apple in its participation in any of these four sectors. Understanding the economic impact of any asserted patent therefore requires teasing out the specific industrial role the patent performs.

Furthermore, the problem with the classification of patents into industrial groups is complicated by the broad definition of infringement to span players on every level of the chain from supplier to end-user. The Patent Act defines a direct infringer as follows:

> whoever without authority makes, uses, offers to sell, or sells any patented invention, within the United States or imports into the United States any patented invention during the term of the patent therefor, infringes the patent. [14]

In other words, the infringer need not be the manufacturer who *makes* a patented invention; it suffices for liability that he *uses, sells, offers to sell*, or *imports* the invention. The indirect infringement doctrines of inducement and contributory infringement further expand the breath of potential defendants and the potential economic reach of an asserted patent. [15] By law, all of the infringers are considered joint tort-feasors, and the owner of the patent can pick the defendant so long as he obtains one satisfaction for infringement. [16]

As an illustration, we could consider the problem of classifying U.S. Patent No. 6,253,075, entitled "Method and Apparatus for Incoming Call Rejection." As the preamble of independent claim 1 states, the patent is concerned with "[a] method of selectably rejecting an incoming call to a mobile phone." The patent can in principle be asserted against the user of the mobile phone who rejects calls, the retailer of that phone that possesses the capability to reject calls, the programmer of that capability, or the manufacturer of that mobile phone.

Nonetheless, common sense informs us that, for every act of infringement where liability is joint and shared, there is always a defendant who is the most culpable or most likely to be accused. Indeed, patent law recognizes the existence of "true defendants." [17] The "true defendant" can be thought of as the mastermind of the act of infringement, **[*500]** and generally is the provider of the service or the maker of the goods. The concept is particularly useful in identifying the NAICS group that an asserted patent should be classified within.

Returning to the above example, U.S. Patent No. 6,253,075 was asserted against Apple, maker of the iPhone, by a corporation formed by Nokia, Sony, and MPEG LA. [18] Applying the concept of the "true defendant," we understand that such call rejection capabilities would be provided by the *programmer* of the operating system and of the capabilities of the phone. The asserted patent as such implicates operating systems and is classified under the NAICS umbrella group of "Publishing Industries, except Internet (Includes Software)."

Finally, it must be noted that the NAICS groups may make sense from an *economic* point of view, but they may not be appropriate from a *technological* point of view, the natural lens from which to understand patents. For example, within the "Finance, Insurance, Real Estate, Rental, & Leasing" umbrella, the NAICS distinguishes between such industries as "Securities, Commodity Contracts, & Investments" and "Funds, Trusts, & Other Financial Vehicles." But given that both industries use essentially the same technology to buy and sell, it would not be appropriate to blindly assign patents

A. Data Summary

A total of 857 patents and patent applications were identified as being litigated within the three courts specified using the methodology described in Section 2.1. These patents and applications were then classified within the NAICS categories, and the results are presented in Appendix A1.

A summary of this litigation data is presented in Appendix A2. Plot of the data can be found in Figure 1.

B. Differences in the Patent Dockets

Prior to comparing the patent litigation data with the economic data, it is worthwhile to first focus on the litigation data by itself.

It is evident from Figure 1 that the "tech" industry, which we understand to include at least "Computer & Electronic Products," "Publishing Industries, except Internet (Includes Software)," "Broadcasting & Telecommunications," and "Data Processing, Internet Publishing, & Other Information Services," constitute a large proportion of the dockets. This finding is at least consistent with that of Professor Allison, who found in his survey of 2008 district court cases that more than 45% were what was termed "software and electronics cases." [20]

[*501] Figure 1: Patents litigated in each venue classified by industry from January 1 to November 30, 2013.

[*502] What is particularly striking is that the Federal Circuit docket shows considerably more diversity than that of the two district courts. In principle, a more technologically diverse patent docket is one that spans more industries than a less diverse docket. That is, from a visual perspective, a diverse portfolio would be spread across the entire spectrum of industries, even if some industries may dominate others in economic size and influence.

From a glance, it can be observed that the Federal Circuit's patent docket is far more diverse than that of the District of Delaware, which is in turn more diverse than that of the Eastern District of Texas. Unlike the district court spectra, which are dominated by the peaks at "Computer & Electronic Products," the industrial group contributing the highest number of patents within the Federal Circuit docket is actually "Chemical Products." This group "is based on the transformation of organic and inorganic raw materials by a chemical process and the formulation of products" and includes the pharmaceutical industry. [21] Likewise, there is an entire subset of the Federal Circuit docket based on industries, most notably "Machinery," which barely register at all in the dockets of the two district courts.

Because the cases of the district courts feed into the appellate docket of the Federal Circuit, these discrepancies are noteworthy. It may be that the difference is accounted for by the dockets of the district courts not analysed in this article. It is beyond the capability of this author to analyse such a large number of patent dockets. Nonetheless, there does not appear any feature distinguishing the other district courts from the Eastern District of Texas and the District of Delaware that could satisfactorily explain how the dockets of the other district courts would contribute to this diversity.

A better explanation is likely provided by Professor Allison in his investigation of the behaviour and success rates of patent litigants in different industries. As he noted, the patent holders in electronic

than that of the district courts. Given that the Federal Circuit has exclusive jurisdiction over patent appeals [23] and by its unique position possesses control of the development and evolution of substantive patent law, the fear that judicial precedent is adversely affected by a selection bias **[*503]** towards a "technologically uneven" set of litigated patents does not appear substantiated.

Nonetheless, the number of industry categories that a docket spans is not an adequate measure of the docket. After all, the definition of the industry categories is artificial, and the number of existing categories must also be artificial. A better understanding of the patent dockets necessarily takes into account the economics of the underlying industries, which we now examine.

IV. Patent Litigation, Economics, and Trade

A. Data Summary

The Bureau of Economic Analysis provides data for the value added, full-time equivalent ("FTE") employees, and wages and salaries per FTE employee for industries as classified under the NAICS. [24] The economic data for 2013 is summarized in Appendix and plotted below in Figure 2.

The International Trade Administration provides data concerning the trade of merchandise in accordance with the NAICS classification. [25] The import data for 2013 is summarized in Appendix and plotted below in Figure 3.

[*504] Figure 2: 2013 economic data classified by industry.

[*505] Figure 3: 2013 merchandise import data in accordance with NAICS classification.

[*506] B. Comparison of Patent Docket Statistics with the Economic and Trade Data

As can be observed from a visual comparison of the spectra of patent dockets in Figure 1 with the spectra of economic data in Figure 2, there is a complete disconnect between industries which are high value added or create the most employment and the industries which encounter the most patent litigation. Conversely, the industries which are most heavily involved with patent suits tend not to be industries that either provide high value added or high numbers of employment. The scatterplots of the economic and litigation data, seen in Figure 4, emphasize these observations.

Figure 4: Plots of industry economic data against patent litigation data.

The number of patents which pertain to the most economically NAICS significant groups, such as "Government," "Wholesale Trade," "Retail Trade," "Real Estate," "Finance & Insurance," "Construction," and "Food Services & Drinking Places," are minuscule in comparison to the entirety of the dockets. "Health Care" is arguably the *only* one of the top industries within the U.S. economy that is involved with patent litigation. Even then, that sector only accounts for 19 of the 857 of the patents and applications analyzed.

The Federal Circuit has repeatedly emphasized, "[i]t is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is only entitled the right to exclude.'" [26] Patents thus operate as a set of regulations which define the technological activities that one may not practice without a license. From our economic analysis, however, we can safely conclude that patents, as they are litigated in the United States, have virtually no direct regulatory effect on the vast majority of economic activity and employment within the United States. [27] For example,

As we stated earlier, the industries with heavy patent litigation support a relatively small proportion of the value added and number of the employees of the United States. The regulatory effects of patents as such are limited in terms of activities happening within the United States. That does not mean, however, that the patents have no impact at all.

The trade data shows how patents interact with imported merchandise. In Figure 3, we observe a much better correlation of the patent litigation data with the value of imported merchandise than that of the litigation data with domestic economic statistics. The scatterplot presented in Figure 5, actually suggests the possibility of a linear relationship between the number of patents litigated and the value of imported merchandise, or, in other words, more imports, more litigation.

[*508] Because of the legal effect of patentability doctrines, the correlation between the two sets of data is actually better in reality than it first appears. For example, under 35 U.S.C. § 101, "'laws of nature, natural phenomena, and abstract ideas' are not patentable." [28] These doctrines in effect exclude the imports of entire industries, such as "Mining," from any U.S. patent protection, because the products of mining are very much "natural phenomena." [29] Likewise, "Apparel & Leather & Allied Products," another significant import category, is unlikely to be the subject of much patent protection. Even conceding the amount of innovation within the fashion industry, we have to suspect that there is few, if any, of their imported merchandise which could be found novel or non-obvious within the meaning of patent law. Other industries such as "Primary Metals" and "Petroleum & Coal Products" are likely susceptible to similar patentability effects. Should the appropriate "discounts" be made to the import statistics of these industries, a better fit with the patent litigation statistics would likely result. This is evident when we focus solely on the "Manufacturing" categories as a crude approximation, since such merchandise is presumably more likely to be patenteligible. [30] However, actual numerical corrections would require detailed knowledge about the specific merchandise imported within the United States, and the data we have is insufficient for this analysis.

The dire state of manufacturing in America is hardly news; indeed, President Obama, in his 2014 State of the Union Address, noted that it was only in 2013 when the "manufacturing sector add[ed] jobs for the first time since the 1990s." [31] But a comparison of the patent litigation statistics with the economics and trade data shows clearly that much of patent litigation, as it exists within the United States, is about regulating **[*509]** what workers in foreign lands are making. [32] The dominant industry within the U.S. patent dockets is "Computer & Electronic Products." This is also the dominant category within the imports, which actually exceed in dollar amount the value added within the United States. It is difficult to conclude that patent litigation and by extension the patent system as a whole actually provides much economic benefit to the bulk of U.S. employees as compared to foreign workers. [33]

But for those few of the U.S. public that participate in those industrial sectors which heavily feature in the patent dockets, the patent system appears to bear some correlation to their own economic well-being. Figure 6 is a scatterplot of the industry wage statistics and the litigation data. Our analysis is again plagued by the aforementioned problem that the services and products of different industries are not all equal from a patentability point of view. Nonetheless, looking only to the "Manufacturing" industries as an approximation, we do see that those industries that litigate more patents tend to be those that pay higher wages.

earn more on average than those who outside of these industries. [34]

[*510] Figure 6: Plots of industry wage data against patent litigation data. Darker points denote industries regarded as "Manufacturing."

C. Implications on Patent Policies

Our conclusions here strongly suggest that patents, as they are currently used within the federal courts, have little impact on the economic life of much of the U.S. population. What they do control is foreign behavior, through their effect on imported products, and they have an effect mainly because of the power and size of the U.S. consumer market.

To that end, patents have in effect become a component of international trade. Loosening patentability requirements, for example, is equivalent to lowering barriers on importation. It may lead to cheaper and more products for the American consumers, but is unlikely to directly lead to more employment within the United States. Rather, the economic effects would likely be observed in factories overseas, and, if anything, such a change would adversely impact the balance of trade because of the greater amount of importation it would encourage.

If the patent system were to be armed with an ability to positively impact the national economy, it would require building into patent doctrines some direct nexus with economic activities within the borders. That is, patent law must be built to somehow encourage and benefit those who choose to practice their patents within the United States.

Such a concept is not as revolutionary as it seems. In the early versions of the Patent Act, there was a working requirement for domestic use, as the Supreme Court explained in *Continental Paper Bag v. Eastern Paper Bag*:

> [The Patent Act of 1832] extended the privilege of the patent law to aliens, but required them "to introduce into public use in the United States the **[*511]** invention or improvement within one year from the issuing thereof," and indulged no intermission of the public use for any period longer than six months. A violation of the law rendered the patent void. The act was repealed in 1836. It is manifest, as is said in Walker on Patents, § 106, that Congress has not "overlooked the subject of non-user of patented inventions." And another fact may be mentioned. In some foreign countries the right granted to an inventor is affected by non-use. This policy, we must assume, Congress has not been ignorant of nor of its effects. It has, nevertheless, selected another policy; it has continued that policy through many years. We may assume that experience has demonstrated its wisdom and beneficial effect upon the arts and sciences. [35]

Although the working requirement has long been repealed, there are still vestiges of bias towards domestic use of patents within U.S. patent law. For example, Congress has limited access to the International Trade Commission as a patent litigation forum to those who can show "an industry *in the United States*, relating to the articles protected by the [asserted] patent . . . exists or is in the process of being established." [36] But as a whole, U.S. patent law as it is now is not geared to encourage economic activities within U.S. borders. [37] A discussion as to whether such solutions as a new working requirement are advisable, however, is outside the scope of this article.

V. Conclusions

In this article, we have also compared the patent dockets of the Federal Circuit, the Eastern District of Texas, and the District of Delaware. As the data show, the patents that reach appellate review are actually more diverse in terms of technology and industries. In effect, the process of litigation serves to increase the diversity of the patents that reach the Federal Circuit, and, so doing, ensures that the development of patent law doctrines that affect all technology is not overly reliant on cases from any particular industry.

[*512] A1: Patents and Applications Analysed

The 857 patents and applications analyzed in this article are listed below, organized by the industry of classification along with the courts in which they were litigated:

Industry Classification & Patent Data BEA Code 39 & Pat. No.	BEA Title & Patent Title
11	Agriculture, Forestry, Fishing, & Hunting
111CA	Farms
5,554,798	Fertile glyphosate-resistant transgenic corn plants
5,750,871	Transformation and foreign gene expression in Brassica species
6,025,545	Methods and compositions for the production of stably transformed, fertile monocot plants and cells thereof
6,040,497	Glyphosate resistant maize lines
6,083,878	Use of N-(phosphonomethyl) glycine and derivatives thereof
6,753,463	Transformed cotton plants
6,825,400	Corn plants comprising event PV-ZMGT32(nk603)
11/076,7	Transgenic soybean seeds having reduced
33	activity of lipoxygenases
113FF	Forestry, Fishing, & Related Activities
21	Mining
22	Utilities
23	Construction
6,414,010	Pestitidal pyrazoles and derivatives
6,835,743	Pestitidal pyrazoles and derivatives
6,892,861	Destination call control for modernizing elevator installation
6,935,465	Method for modernization of an elevator installation
11/235,3	System and method for determining

& Pat. No.	
44	variance in building structures
31G	Manufaturing
321	Wood Products
5,562,137	Method and apparatus for retaining a flitch for cutting
5,678,619	Method and apparatus for cutting veneer from a tapered flitch
5,694,995	Method and apparatus for preparing a flitch for cutting
5,701,938	Method and apparatus for retaining a flitch for cutting
5,819,828	Method and apparatus for preparing a flitch for cutting
7,395,843	Method and apparatus for retaining a flitch for cutting
327	Nonmetallic Mineral Products
5,411,797	Nanophase diamond films
5,478,650	Nanophase diamond films
6,193,856	Sputtering target comprising a substrate and a target material formed on the substrate, wherein the target material comprises a metal oxide of the chemical formula mox as the main component, wherein mox is a metal oxide deficient in oxygen
RE34, 162	Controlled surface electrical resistance carbon fiber sheet product
331	Primary Metals
6,296,805	Hot-rolled coated steel sheet comprising hot-rolled steel sheet coated with aluminum or aluminum alloy coating, having very high mechanical resistance after thermal treatment and high corrosion resistance from aluminum coating
RE44, 153	Coated hot- and cold-rolled steel sheet comprising a very high resistance after thermal treatment
332	Fabricated Metal Products
5,409,057	Heat exchange element
5,551,504	Heat exchange element
6,325,617	Child-resistant utility lighter incorporating a cam mechanism and a lever spring lock
6,418,936	Tobacco pipe
6,473,973	Disposable cutting head for clippers

Industry Classification & Patent Data	2013 Litigation Data 38		
BEA	Fed.	E. D.	D. Del.

& Pat. No.			
11			
111CA			
5,554,798	[checkmark]		
5,750,871	[checkmark]		
6,025,545	[checkmark]		
6,040,497	[checkmark]		
6,083,878	[checkmark]		
6,753,463	[checkmark]		
6,825,400	[checkmark]		
11/076,7			[checkmark]
33			
113FF			
21			
22			
23			
6,414,010	[checkmark]		
6,835,743	[checkmark]		
6,892,861			[checkmark]
6,935,465			[checkmark]
11/235,3	[checkmark]		
44			
31G			
321			
5,562,137	[checkmark]		
5,678,619	[checkmark]		
5,694,995	[checkmark]		
5,701,938	[checkmark]		
5,819,828	[checkmark]		
7,395,843	[checkmark]		
327			
5,411,797		[checkmark]	
5,478,650		[checkmark]	
6,193,856			[checkmark]

& Pat. No.				
RE34, 162	[checkmark]			
331				
6,296,805				[checkmark]
RE44, 153				[checkmark]
332				
5,409,057			[checkmark]	
5,551,504			[checkmark]	
6,325,617	[checkmark]			
6,418,936	[checkmark]			
6,473,973	[checkmark]			

[*513]

Industry Classification & Patent Data BEA Code & Pat. No.	BEA Title & Patent Title
6,814,569	Child-resistant utility lighter incorporating a cam mechanism and a lever spring lock
10/306,057	Element with a shank and a holding element connected to it for connecting to a rod
333	Machinery
4,924,257	Scan and repeat high resolution projection lithography system
5,011,339	Process for distribution of pieces such as rivets, and apparatus for carrying out the process
5,143,216	Process for distribution of pieces such as rivets, and apparatus for carrying out the process

Code & Pat. No.	& Patent Title
5,228,916	Apparatus for creating a gelatin coating
5,285,236	Large-area, high-throughput, high-resolution projection imaging system
5,291,240	Nonlinearity-compensated large-area patterning system
5,353,530	Quick mounting snow plow assembly
5,436,026	Discharge and transfer system for apparatus for gelatin coating tablets
5,490,569	Directional boring head with deflection shoe and method of boring
5,577,618	Mobile aggregate material processing plant
5,679,406	Tablet dipping systems for apparatus for gelatin coating tablets
5,831,220	Automated package shipping machine
5,985,347	Cheese processing vat and method
6,105,014	Automated package shipping machine
6,118,894	Integrated circuit probe card inspection system
6,476,351	Laser marking system
6,523,680	Radius conveyor belt with structure for the prevention of pinched fingers
6,619,168	Method and apparatus for automatic precision cutting of graphics areas from sheets
6,672,187	Method and apparatus for rapid precision cutting of graphics areas from sheets
6,826,298	Automated wafer defect inspection system and a process of performing such inspection
6,944,978	Snowplow and mount assembly
7,140,443	Pipe handling device, method and system
7,373,877	Wire strapper for waste material baler
7,377,324	Pipe handling device, method and system
7,412,992	Wire strapper for waste material baler
7,707,828	Method and apparatus for manipulating and diluting internal combustion engine exhaust gases
10/906,508	Method and apparatus for verifying memory testing software
11 /407,778	Device for stirring a liquid and for injecting a gas into this liquid, suitable for shallow basins
11/514,620	LOW-VOLUME SYSTEM FOR TESTING BIOLOGICAL OR CHEMICAL AGENTS, AND METHOD OF TESTING
11 /533,826	POINT-OF-USE PROCESS CONTROL BLENDER SYSTEMS AND CORRESPONDING METHODS
RE35,700	Removable snowplow assembly with pivotable lift stand
334	Computer & Electronic Products
4,811,075	High voltage MOS transistors
4,876,555	Resonance label and method for its fabrication
4,916,635	Shaping command inputs to minimize unwanted dynamics
4,930,158	Selective video playing system
4,930,160	Automatic censorship of video programs
5,131,006	Carrier detection for a wireless local area network
5,151,920	Radio LAN station with improved frame delimiter detection in a spread spectrum environment

Code & Pat. No.	& Patent Title
5,214,409	ulti-memory electronic identification tag
5,241,497	VLSI memory with increased memory access speed, increased memory cell density and decreased parasitic capacitance
5,247,434	Method and apparatus for kidney dialysis
5,282,222	Method and apparatus for multiple access between transceivers in wireless communications using OFDM spread spectrum
5,299,313	Network interface with host independent buffer management
5,307,459	Network adapter with host indication optimization
5,337,745	Device and method for in vivo qualitative or quantative measurement of blood chromophore concentration using blood pulse spectrophotometry
5,337,753	Heart rate monitor
5,396,519	Method and apparatus for adaptively providing precoding and preemphasis conditioning to signal data for transfer over a communication channel
5,412,730	Encrypted data transmission system employing means for randomly altering the encryption keys
5,422,887	Medium access protocol for wireless local area network
5,434,872	Apparatus for automatic initiation of data transmission
5,490,170	Coding apparatus for digital signal
5,499,017	Multi-memory electronic identification tag
5,507,035	Diversity transmission strategy in mobile /indoor cellula radio communications

Industry Classification & Patent Data	2013 Litigation Data		
BEA Code & Pat. No.	Fed. Cir.	E.D. Tex.,	D. Del.
6,814,569	[Checkmark]		
10/306,057	[Checkmark]		
333			
4,924,257	[Checkmark]		
5,011,339	[Checkmark]		
5,143,216	[Checkmark]		

Code & Pat. No.	Cir.	Tex.,
5,228,916	[Checkmark]	
5,285,236	[Checkmark]	
5,291,240	[Checkmark]	
5,353,530	[Checkmark]	
5,436,026	[Checkmark]	
5,490,569	[Checkmark]	
5,577,618	[Checkmark]	
5,679,406	[Checkmark]	
5,831,220	[Checkmark]	
5,985,347	[Checkmark]	
6,105,014	[Checkmark]	
6,118,894	[Checkmark]	
6,476,351		
6,523,660	[Checkmark]	
6,619,168	[Checkmark]	
6,672,187	[Checkmark]	
6,826,298	[Checkmark]	
6,944,978	[Checkmark]	
7,140,443	[Checkmark]	
7,373,877	[Checkmark]	
7,377,324	[Checkmark]	
7,412,992	[Checkmark]	
7,707,828		[Checkmark]
10/906,508	[Checkmark]	
11 /407,778	[Checkmark]	
11/514,620	[Checkmark]	
11 /533,826	[Checkmark]	
RE35,700	[Checkmark]	
334		
4,811,075	[Checkmark]	
4,876,555	[Checkmark]	
4,916,635	[Checkmark]	
4,930,158		[Checkmark$
4,930,160		[Checkmark$
5,131,006		[Checkmark$
5,151,920		[Checkmark$

Code & Pat. No.	Cir.	Tex.,	
5,214,409	[Checkmark]		
5,241,497	[Checkmark]		
5,247,434	[Checkmark]		
5,282,222		[Checkmark	)
5,299,313		[Checkmark	)
5,307,459		[Checkmark	)
5,337,745			[Checkmark]
5,337,753	[Checkmark]		
5,396,519			[Checkmark]
5,412,730		[Checkmark	)
5,422,867		[Checkmark	)
5,434,872		[Checkmark	)
5,490,170			[Checkmark]
5,499,017	[Checkmark]		
5,507,035			[Checkmark]

[*514]

Industry Classification & Patent Data BEA Code & Pat. No.	BEA Title & Patent Title
5,517,407	Device for including enhancing information with printed information and method for electronic searching thereof
5,521,737	Optical amplifier and optical communication system with optical amplifier using pumping light beam
5,526,163	Optical amplifier and optical communication system with optical amplifier using pumping light beam

Code & Pat. No.	& Patent Title
5,530,874	Network adapter with an indication signal mask and an interrupt signal mask
5,541,654	Focal plane array imaging device with random access architecture
5,577,230	Apparatus and method for computer processing using an enhanced Harvard architecture utilizing dual memory buses and the arbitration for data/instruction fetch
5,613,130	Card voltage switching and protection
5,630,163	Computer having a single bus supporting multiple bus architectures operating with different bus parameters
5,632,272	Signal processing apparatus
5,648,674	Array circuitry with conductive lines, contact leads, and storage capacitor electrode all formed in layer that includes highly conductive metal
5,675,808	Power control of circuit modules within an integrated circuit
5,687,325	Application specific field programmable gate array
5,694,322	Method and apparatus for determining tax of a vehicle
5,706,428	Multirate wireless data communication system
5,710,906	Predictive snooping of cache memory for master-initiated accesses
5,710,929	Multi-state power management for computer systems
5,724,505	Apparatus and method for real-time program monitoring via a serial interface
5,732,094	Method for automatic initiation of data transmission
5,742,840	General purpose, multiple precision parallel operation, programmable media processor
5,758,175	Multi-mode power switching for computer systems
5,790,516	Pulse shaping for data transmission in an orthogonal frequency division multiplexed system
5,794,061	General purpose, multiple precision parallel operation, programmable media processor
5,796,046	Communication cable having a striated cable jacket
5,796,978	Data processor having an address translation buffer operable with variable page sizes
5,812,531	Method and apparatus for bridging wireless LAN to a wired LAN
5,819,201	Navigation system with vehicle service information
5,822,610	Mappable functions from single chip /multi-chip processors for computers
5,831,669	Facility monitoring system with image memory and correlation
5,859,547	Dynamic logic circuit
5,862,511	Vehicle navigation system and method
5,878,368	Navigation system with user definable cost values
5,879,958	Method of producing an electro-optical device
5,892,959	Computer activity monitor providing idle thread and other event sensitive clock and power control
5,896,119	Removable backlighting assembly for flat panel display subsystem
5,915,105	Integrated circuit I/O using a high performance bus interface
5,920,802	System and method to improve power distribution in a coaxial cable amplifier

Code & Pat. No.	Patent Title
5,926,237	Computer having liquid crystal display
5,953,263	Synchronous memory device having a programmable register and method of controlling same
5,954,804	Synchronous memory device having an internal register
5,955,955	Drive-bay mounted cooling device
5,958,006	Method and apparatus for communicating summarized data
5,958,036	Circuit for arbitrating interrupts with programmable priority levels
5,961,617	System and technique for reducing power consumed by a data transfer operations during periods of update inactivity
5,976,063	Smart spacers for active matrix liquid crystal projection light valves
5,983,002	Defective floppy diskette controller detection apparatus and method
5,987,019	Multi-rate radiocommunication systems and terminals
5,991,885	Method and apparatus for detecting the presence of a remote device and providing power thereto
5,995,443	Synchronous memory device
6,002,390	Text input device and method
6,002,952	Signal processing apparatus and method
6,006,318	General purpose, dynamic partitioning, programmable media processor
6,009,488	Computer having packet-based interconnect channel
6,029,111	Vehicle navigation system and method using GPS velocities
6,032,214	Method of operating a synchronous memory device having a variable data output length
6,032,215	Synchronous memory device utilizing two external clocks
6,034,918	Method of operating a memory having a variable data output length and a programmable register

Industry Classification & Patent Data	2013 Litigation Data		
BEA Code & Pat. No.	Fed. Cir.	E.D. Tex.,	D. Del.
5,517,407			[Checkmark]
5,521,737	[Checkmark]		

Code & Pat. No.	Cir.	Tex.,	
5,526,163	[Checkmark]		
5,530,874		[Checkmark]	
5,541,654			[Checkmark]
5,577,230		[Checkmark]	
5,613,130			[Checkmark]
5,630,163			[Checkmark]
5,632,272			[Checkmark]
5,648,674	[Checkmark]		
5,675,808			[Checkmark]
5,687,325			[Checkmark]
5,694,322			[Checkmark]
5,706,428		[Checkmark]	
5,710,906		[Checkmark]	
5,710,929			[Checkmark]
5,724,505		[Checkmark]	
5,732,094		[Checkmark]	
5,742,840		[Checkmark]	
5,758,175			[Checkmark]
5,790,516		[Checkmark]	
5,794,061		[Checkmark]	
5,796,046			[Checkmark]
5,796,978		[Checkmark]	
5,812,531			[Checkmark]
5,819,201			[Checkmark]
5,822,610			[Checkmark]
5,831,669		[Checkmark]	
5,859,547			[Checkmark]
5,862,511			[Checkmark]
5,878,368			[Checkmark]
5,879,958		[Checkmark]	
5,892,959			[Checkmark]
5,896,119			[Checkmark]

BEA Code & Pat. No.	Cir.	Tex.,	
5,915,105			[Checkmark]
5,920,802	[Checkmark]		
5,926,237	[Checkmark]		
5,953,263			[Checkmark]
5,954,804			[Checkmark]
5,955,955	[Checkmark]		
5,958,006	[Checkmark]		
5,958,036		[Checkmark]	
5,961,617			[Checkmark]
5,978,063	[Checkmark]		
5,983,002	[Checkmark]		
5,987,019		[Checkmark]	
5,991,885			[Checkmark]
5,995,443			[Checkmark]
6,002,390			[Checkmark]
6,002,952			[Checkmark]
6,006,318		[Checkmark]	
6,009,488		[Checkmark]	
6,029,111			[Checkmark]
6,032,214			[Checkmark]
6,032,215			[Checkmark]
6,034,918			[Checkmark]

[*515]

Industry Classification & Patent Data BEA Code & Pat. No.	BEA Title & Patent Title

& Pat. No.	
6,038,195	Synchronous memory device having a delay time register and method of operating same
6,047,165	Wireless, frequency-agile spread spectrum ground link-based aircraft data communication system
6,047,354	Data processor for implementing virtual pages using a cache and register
6,074,503	Making enhanced data cable with cross-twist cabled core profile
6,079,025	System and method of computer operating mode control for power consumption reduction
6,091,671	Time interval analyzer having interpolator with constant current capacitor control
6,092,172	Data processor and data processing system having two translation lookaside buffers
6,119,181	I/O and memory bus system for DFPs and units with two- or multi-dimensional programmable cell architectures
6,121,960	Touch screen systems and methods
6,141,762	Power reduction in a multiprocessor digital signal processor based on processor load
6,154,637	Wireless ground link-based aircraft data communication system with roaming feature
6,157,850	Signal processing apparatus
6,163,269	Navigation system with anti-alias map display
6,169,515	Navigation information system
6,181,649	Time interval analyzer having current boost
6,221,686	Method of making a semiconductor image sensor
6,226,231	Time interval analyzer having multiple measurement circuits
6,234,598	Shared multiple terminal ground returns for an inkjet printhead
6,256,725	Shared datapath processor utilizing stack-based and register-based storage spaces
6,260,087	Embedded configurable logic ASIC
6,260,097	Method and apparatus for controlling a synchronous memory device
6,263,222	Signal processing apparatus
6,266,321	Method for transmitting two parallel channels using code division and an apparatus realizing the method
6,271,884	Image flicker reduction with fluorescent lighting
6,272,646	Programmable logic device having an integrated phase lock loop
6,294,475	Crystallographic wet chemical etching of III-nitride material
6,308,045	Wireless ground link-based aircraft data communication system with roaming feature
6,309,053	Ink jet printhead having a ground bus that overlaps transistor active regions
6,314,473	System for removing selected unwanted frequenices in accordance with altered settings in a user interface of a data storage device
6,324,120	Memory device having a variable data output length
6,326,978	Display method for selectively rotating windows on a computer display

& Pat. No.	
6,330,435	Data packet discard notification
6,334,938	Target and process for its production, and method for forming a film having a high refractive index
6,335,678	Electronic device, preferably an electronic book
6,338,106	I/O and memory bus system for DFPS and units with two or multi-dimensional programmable cell architectures
6,345,323	Computer interconnection system
6,360,167	Vehicle navigation system with location-based multi-media annotation
6,374,180	Points of interest for a navigation system
6,378,020	System having double data transfer rate and intergrated circuit therefor
6,398,347	Energy balanced ink jet printhead
6,402,279	Inkjet printhead and method for the same
6,404,734	Scalable network restoration device
6,405,291	Predictive snooping of cache memo for master-initiated accesses
6,424,625	Method and apparatus for discarding packets in a data network having automatic repeat request
6,426,916	Memory device having a variable data output length and a programmable register
6,427,078	Device for personal communications, data collection and data processing, and a circuit card
6,441,828	Image display apparatus
6,452,863	Method of operating a memory device having a variable data input length
6,466,568	Multi-rate radiocommunication systems and terminals
6,481,817	Method and apparatus for ejecting ink
6,512,480	System and method for narrow beam antenna diversity in an RF data transmission system
6,519,223	System and method for implementing a semi reliable retransmission protocol
6,542,076	Control, monitoring and /or security apparatus and method
6,542,077	Monitoring apparatus for a vehicle and/or a premises
6,563,786	Orthogonal frequency division multiplexing system with selectable rate
6,621,454	Adaptive beam pattern antennas system and method for interference

Industry Classification & Patent Data	2013 Litigation Data*		
BEA Code & Pat.	Fed. Cir.	E.D. Tex.	D. Del.

& Pat. No.				
6,038,195				[Checkmark]
6,047,165	[Checkmark]			
6,047,354			[Checkmark]	
6,074,503				[Checkmark]
6,079,025				[Checkmark]
6,091,671	[Checkmark]			
6,092,172			[Checkmark]	
6,119,181			[Checkmark]	
6,121,960				[Checkmark]
6,141,762			[Checkmark]	
6,154,637	[Checkmark]			
6,157,850				[Checkmark]
6,163,269				[Checkmark]
6,169,515				[Checkmark]
6,181,649	[Checkmark]			
6,221,686				[Checkmark]
6,226,231	[Checkmark]			
6,234,598	[Checkmark]			
6,256,725			[Checkmark]	
6,260,087				[Checkmark]
6,260,097	[Checkmark]			
6,263,222				[Checkmark]
6,266,321			[Checkmark]	
6,271,884			[Checkmark]	
6,272,646				[Checkmark]
6,294,475				[Checkmark]
6,308,045	[Checkmark]			
6,309,053	[Checkmark]			
6,314,473	[Checkmark]			
6,324,120				[Checkmark]
6,326,978			[Checkmark]	

& Pat. No.				
6,330,435			[Checkmark]	
6,334,938				[Checkmark]
6,335,678				[Checkmark]
6,338,106			[Checkmark]	
6,345,323		[Checkmark]		
6,360,167				[Checkmark]
6,374,180				[Checkmark]
6,378,020				[Checkmark]
6,396,347		[Checkmark]		
6,402,279		[Checkmark]		
6,404,734		[Checkmark]		
6,405,291			[Checkmark]	
6,424,625			[Checkmark]	
6,426,916				[Checkmark]
6,427,078				[Checkmark]
6,441,828				[Checkmark]
6,452,863				[Checkmark]
6,466,568			[Checkmark]	
6,481,817		[Checkmark]		
6,512,460				[Checkmark]
6,519,223			[Checkmark]	
6,542,076				[Checkmark]
6,542,077				[Checkmark]
6,563,786			[Checkmark]	
6,621,454				[Checkmark]

[*516]

Industry Classification & Patent Data	
BEA	BEA Title

Code & Patent No.	Title
	mitigation in point to multipoint RF data transmissions
6,629,207	Method for loading instructions or data into a locked way of a cache memory
6,643,765	Programmable processor with group floating point operations
6,647,450	Multiprocessor computer systems with command FIFO buffer at each target device
6,650,284	Information system
6,697,347	Method and apparatus for controlling transmission of packets in a wireless communication system
6,699,194	Signal processing apparatus and method
6,708,259	Programmable wake up of memory transfer controllers in a memory transfer engine
6,725,155	Method and apparatus for information processing, and medium for information processing
6,725,356	System with wide operand architecture, and method
6,757,322	Space diversity and coding, spread-spectrum antenna and method
6,772,215	Method for minimizing feedback responses in ARQ protocols
6,785,903	Digital television translator with PSIP update
6,788,959	Method and apparatus for transmitting and receiving dynamic configuration parameters in a third generation cellular telephone network
6,792,277	Arranging control signallings in telecommunications system
6,816,145	Large area wide aspect ratio flat panel monitor having high resolution for high information content display
6,838,651	High sensitivity snap shot CMOS image sensor
6,838,715	CMOS image sensor arrangement with reduced pixel light shadowing
6,856,459	Apparatus and method for controlling polarization of an optical signal
6,874,049	Semaphores with interrupt mechanism
6,882,771	Apparatus and method for providing gain equalization
6,900,463	Semiconductor device
6,940,647	Apparatus and method for controlling polarization of an optical signal
6,973,229	Node architecture for modularized and reconfigurable optical networks, and methods and apparatus therefor
6,979,587	Image sensor and method for fabricating the same
6,990,058	Structure and method for storing data on optical disks
6,990,319	Wireless, ground link-based aircraft data communication method
6,992,972	Frequency division multiplexing system with selectable rate
6,993,669	Low power docking systems and methods
7,051,306	Managing power on integrated circuits using power islands
7,058,150	High-speed serial data transceiver and related methods
7,064,768	Bad pixel correction while preserving features
7,072,190	High efficiency power converter
7,109,535	Semiconductor device for isolating a photodiode to reduce junction leakage
7,116,862	Apparatus and method for providing gain equalization
7,135,641	Data cable with cross-twist cabled core profile

Code & Patent No.	Title
7,156,717	situ finishing aid control
7,161,506	Systems and methods for data compression such as content dependent data compression
7,190,966	Method and apparatus for performing an access procedure
7,197,662	Methods and systems for a storage system
7,213,131	Programmable processor and method for partitioned group element selection operation
7,215,984	Signal processing apparatus
7,216,217	Programmable processor with group floating-point operations
7,248,181	Automated meter reading system
7,250,105	Measurement of substances in liquids
7,263,143	System and method for statistically directing automatic gain control
7,269,034	High efficiency power converter
7,272,021	Power converter with isolated and regulated stages
7,286,123	LED driver circuit having temperature compensation
7,286,847	Method and apparatus for performing an access procedure
7,287,109	Method of controlling a memory device having a memory core
7,292,151	Human movement measurement system
7,313,647	Storage and reproduction apparatus
7,315,257	Automated meter reader having high product delivery rate alert generator
7,339,714	Variable blazed grating based signal processing
7,349,012	Imaging apparatus with higher and lower resolution converters and a compression unit to compress decreased resolution image data
7,349,540	Generation of user equipment identification specific scrambling code for high speed shared control channel
7,352,300	Data compression systems and methods
7,353,367	System and software for catenated group shift instruction
7,397,363	Control and/or monitoring apparatus and method
7,415,530	System and methods for accelerated data storage and retrieval
7,415,680	Power managers for an integrated circuit

Industry Classification & Patent Data BEA Code & Pat. No.	2013 Litigation Data* Fed. Cir.	E.D. Tex.	D. Del.

& Pat. No.				
6,629,207			[Checkmark]	
6,643,765			[Checkmark]	
6,647,450				[Checkmark]
6,650,284				[Checkmark]
6,697,347			[Checkmark]	
6,699,194				[Checkmark]
6,708,259				[Checkmark]
6,725,155				[Checkmark]
6,725,356			[Checkmark]	
6,757,322				[Checkmark]
6,772,215			[Checkmark]	
6,785,903	[Checkmark]			
6,788,959			[Checkmark]	
6,792,277			[Checkmark]	
6,816,145				[Checkmark]
6,838,651			[Checkmark]	
6,838,715			[Checkmark]	
6,856,459			[Checkmark]	
6,874,049				[Checkmark]
6,882,771			[Checkmark]	
6,900,463	[Checkmark]			
6,940,647			[Checkmark]	
6,973,229				[Checkmark]
6,979,587				[Checkmark]
6,990,058				[Checkmark]
6,990,319	[Checkmark]			
6,992,972			[Checkmark]	
6,993,669				[Checkmark]
7,051,306			[Checkmark]	
7,058,150	[Checkmark]			
7,064,768			[Checkmark]	
7,072,190	[Checkmark]			
7,109,535			[Checkmark]	
7,116,862			[Checkmark]	
7,135,641				[Checkmark]
7,156,717				[Checkmark]
7,161,506			[Checkmark]	

& Pat. No.				
7,190,966	[Checkmark]			
7,197,662				[Checkmark]
7,213,131			[Checkmark]	
7,215,984				[Checkmark]
7,216,217			[Checkmark]	
7,248,181			[Checkmark]	
7,250,105	[Checkmark]			
7,263,143				[Checkmark]
7,269,034	[Checkmark]			
7,272,021	[Checkmark]			
7,286,123				[Checkmark]
7,286,847	[Checkmark]			
7,287,109	[Checkmark]			
7,292,151	[Checkmark]			
7,313,647				[Checkmark]
7,315,257			[Checkmark]	
7,339,714			[Checkmark]	
7,349,012				[Checkmark]
7,349,540	[Checkmark]			
7,352,300			[Checkmark]	
7,353,367			[Checkmark]	
7,397,363				[Checkmark]
7,415,530			[Checkmark]	
7,415,680			[Checkmark]	

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Industry Classification & Patent Data BEA Code & Pat. No.	BEA Title & Patent Title
7,426,387	Wireless, ground link-based aircraft data communication system with roaming feature

& Pat. No.	
7,428,412	Wireless, ground link-based aircraft data communication system with roaming feature
7,429,965	Apparatus for the display of embedded information
7,444,146	Wireless, ground link-based aircraft data communication system with roaming feature
7,447,181	Method and apparatus for improving a mobile station cell change operation in the general packet radio system (GPRS)
7,457,250	System for communicating with electronic equipment
7,487,533	Digital television translator with PSIP update
7,492,268	Human movement measurement system
7,502,406	Automatic power control system for a code division multiple access (CDMA) communications system
7,509,154	Signal processing apparatus
7,509,366	Multiplier array processing system with enhanced utilization at lower precision
7,529,271	Method and device for transferring data over GPRS network
7,530,949	Dual-mode pulse oximeter
7,530,955	Signal processing apparatus
7,536,013	User equipment identification specific scrambling
7,543,177	Methods and systems for a storage system
7,558,083	High efficiency power converter
7,564,702	High efficiency power converter
7,606,910	Method for indicating a UE that it must register
7,616,970	Dual mode unit for short range, high rate and long range, lower rate data communications
7,653,806	Method and apparatus for performing improved group floating-point operations
7,660,972	Method and software for partitioned floating-point multiply-add operation
7,660,973	System and apparatus for group data operations
7,663,061	High performance data cable
7,663,607	Multipoint touchscreen
7,706,332	Method and subscriber unit for performing power control
7,730,287	Method and software for group floating-point arithmetic operations Virtual reality camera
7,733,368	Easily deployable interactive direct-pointing system and presentation control system and calibration method therefor
7,746,321	Personal area network with automatic attachment and detachment
7,756,129	Digital television translator with PSIP update
7,761,893	Ellipse fitting for multi-touch surfaces
7,812,828	Power managers for an integrated circuit
7,945,885	System, method and computer program product for adding voice activation and voice control to a media player
7,953,599	Methods and systems for a storage system
7,958,388	User equipment identification specific scrambling
7,970,127	High performance data cable
7,977,575	Digital television translator with PSIP update
7,984,469	Power managers for an integrated circuit
7,996,811	Signal processing apparatus
8,019,400	Easily deployable interactive direct-pointing system and presentation control system and calibration method therefor
8,049,729	Signal processing apparatus
8,128,572	

& Pat. No.	
8,144,158	Display system having floating point rasterization and point framebuffering
10/097,096	Method and system for detecting colorimetric abnormalities in vivo
10/968,448	Capturing Input Device Data in Computer Systems
11/432,583	Movement Disorder Recovery System and Method
D504,889	Electronic device
D593,087	Electronic device
D618,677	Electronic device
RE37,802	Multicode direct sequence spread spectrum
RE42,219	Multiple-input multiple-output (MIMO) spread spectrum system and method
335	Electrical equipment, appliances, and components
6,107,851	Offline converter with integrated softstart and frequency jitter
6,229,366	Offline converter with integrated softstart and frequency jitter
6,249,876	Frequency jittering control for varying the switching frequency of a power supply
6,719,434	Foldable light diffusion box with frame assembly
6,830,014	Animal collar
7,110,270	Method and apparatus for maintaining a constant load current with line voltage in a switch mode power supply
7,259,972	Primary-side-control power converter having a switching controller

Industry Classification & Patent Data	2013 Litigation Data*		
BEA Code & Pat. No.	Fed. Cir.	E.D. Tex.	D. Del.
7,426,387	[Checkmark]		
7,428,412	[Checkmark]		
7,429,965			[Checkmark]
7,444,146	[Checkmark]		
7,447,181		[Checkmark]	
7,457,250			[Checkmark]
7,467,533	[Checkmark]		

& Pat. No.				
7,492,268	[Checkmark]			
7,502,406	[Checkmark]			
7,509,154				[Checkmark]
7,509,366			[Checkmark]	
7,529,271			[Checkmark]	
7,530,949				[Checkmark]
7,530,955				[Checkmark]
7,536,013	[Checkmark]			
7,543,177				[Checkmark]
7,558,083	[Checkmark]			
7,564,702	[Checkmark]			
7,606,910			[Checkmark]	
7,616,970	[Checkmark]			
7,653,806			[Checkmark]	
7,660,972			[Checkmark]	
7,660,973			[Checkmark]	
7,663,061				[Checkmark]
7,663,607	[Checkmark]			
7,706,332	[Checkmark]			
7,730,287			[Checkmark]	
7,733,368				[Checkmark]
7,746,321	[Checkmark]		[Checkmark]	
7,756,129	[Checkmark]		[Checkmark]	
7,761,893	[Checkmark]			
7,812,828	[Checkmark]			
7,945,885			[Checkmark]	
7,953,599			[Checkmark]	
7,958,388				[Checkmark]
7,970,127	[Checkmark]			
7,977,575				[Checkmark]
7,984,469	[Checkmark]			
7,996,811			[Checkmark]	
8,019,400				[Checkmark]
8,049,729	[Checkmark]		[Checkmark]	
8,128,572				[Checkmark]
8,144,158				[Checkmark]
10/097,096	[Checkmark]			
10/968,448	[Checkmark]			
11/432,583	[Checkmark]			
D504,889	[Checkmark]			
D593,087	[Checkmark]			
D618,677	[Checkmark]			

& Pat. No.				
RE37,802			[Checkmark]	
RE42,219				[Checkmark]
335				
6,107,851		[Checkmark]		[Checkmark]
6,229,366		[Checkmark]		[Checkmark]
6,249,876		[Checkmark]		[Checkmark]
6,719,434		[Checkmark]		
6,830,014		[Checkmark]		
7,110,270				[Checkmark]
7,259,972				[Checkmark]

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Industry Classification & Patent Data	
BEA Code & Pat. No.	**BEA Title & Patent Title**
	using frequency hopping and voltage and current control loops
7,267,082	Animal collar
7,352,595	Primary-side controlled switching regulator
7,417,382	High-efficiency adaptive DC/AC converter
7,525,259	Primary side regulated power supply system with constant current output
7,834,605	Method and apparatus for maintaining a constant load current with line voltage in a switch mode power supply
7,876,587	Method and apparatus providing a multi-function terminal for a power supply controller
7,947,928	Slow cooker
7,952,895	Method and apparatus for implementing an unregulated dormant mode in a power converter
7,995,359	Method and apparatus for implementing an unregulated dormant mode with an event counter in a power converter
8,115,457	Method and apparatus for implementing a power converter input terminal voltage discharge circuit
336	Transportation equipment

& Pat. No.	
5,113,780	Automatic boat trim tab control
5,265,562	Internal combustion engine with limited temperature cycle
5,437,354	Tilt control apparatus for vehicles
5,529,153	Tilt control apparatus for vehicles
6,058,904	Internal combustion engine with limited temperature cycle
6,292,974	Glass wiper blade for motor vehicles
6,313,749	Sleepiness detection for vehicle driver or machine operator
6,478,711	Apparatus for changing speed of bicycles
6,675,434	Wiper blade for the glass surfaces of motor vehicles with an elongated, spring-elastic support element
6,944,905	Wiper blade for cleaning screens in particular on motor vehicles
6,978,512	Wiper blade for cleaning vehicle windows
7,214,017	System and method for partitioning cargo areas
337	Furniture & Related Products
339	Miscellaneous (Durable Goods) Manufacturing
5,275,616	Insertion assembly and method of inserting a vessel plug into the body of a patient
5,304,143	Valve system for introducing objects into anatomical body portions
5,622,375	Push-chair
5,653,760	Method and apparatus for managing macromolecular distribution
5,685,854	Valve system for introducing objects into anatomical body portions
5,712,327	Soft gas permeable contact lens having improved clinical performance
5,716,375	Insertion assembly and method of inserting a vessel plug into the body of a patient
5,737,054	Auxiliary lenses for eyeglasses
5,741,510	Adhesive patch for applying analgesic medication to the skin
5,936,624	Male connector with a continous surface for a guide wire and method therefor
6,012,811	Eyeglass frames with magnets at bridges for attachment
6,077,281	Septal defect closure device
6,077,291	Septal defect closure device
6,086,604	Stent having a multiplicity of undulating longitudinals
6,092,896	Eye-wear with magnets
6,112,598	Pressure sensor and guide wire assembly for biological pressure measurements
6,167,763	Pressure sensor and guide wire assembly for biological pressure measurements
6,196,980	Male connector with a continuous surface for a guide wire, and method therefor
6,248,083	Device for pressure measurements
6,270,464	Biopsy localization method and device
6,318,992	Slide-safety button child-resistant utility lighter
6,356,782	Subcutaneous cavity marking device and method
6,547,817	Stent having a multiplicity of undulating longitudinals
6,699,205	Biopsy localization method and device
6,716,240	Stent having a multiplicity of undulating longitudinals
6,746,773	Coatings for medical devices
6,976,965	Ultra miniature pressure sensor

& Pat. No.	
7,008,439	Device and method for sealing puncture wounds
7,080,768	Spring energized desktop stapler
7,128,744	Bone plating system
7,178,709	Spring energized desktop stapler
7,290,692	Stapler safety device to limit motion of striker
7,429,270	Intervertebral implant
7,591,844	Medical devices, drug coatings and methods for maintaining the drug coatings thereon
7,785,302	Access port identification systems and methods
7,785,334	Implantable prosthesis
7,806,905	Implantable prosthesis

Industry Classification & Patent Data BEA Code & Pat. No.	2013 Litigation Data* Fed. Cir.	E.D. Tex.	D. Del.
7,267,082	[Checkmark]		
7,352,595			
7,417,382	[Checkmark]		
7,525,259			[Checkmark]
7,834,605			[Checkmark]
7,876,587			[Checkmark]
7,947,928	[Checkmark]		
7,952,895			[Checkmark]
7,995,359			[Checkmark]
8,115,457			[Checkmark]
336			
5,113,780	[Checkmark]		
5,265,562	[Checkmark]		
5,437,354			[Checkmark]
5,529,153			[Checkmark]
6,058,904	[Checkmark]		
6,292,974	[Checkmark]		
6,313,749	[Checkmark]		

& Pat. No.				
6,478,711	[Checkmark]			
6,675,434	[Checkmark]			
6,944,905	[Checkmark]			
6,978,512	[Checkmark]			
7,214,017	[Checkmark]			
337				
339				
5,275,616	[Checkmark]			
5,304,143		[Checkmark]		
5,622,375	[Checkmark]			
5,653,760	[Checkmark]			
5,685,854		[Checkmark]		
5,712,327	[Checkmark]			
5,716,375	[Checkmark]			
5,737,054	[Checkmark]			
5,741,510				[Checkmark]
5,938,624				[Checkmark]
6,012,811	[Checkmark]			
6,077,261	[Checkmark]			
6,077,291	[Checkmark]			
6,086,604	[Checkmark]			
6,092,896	[Checkmark]			
6,112,598				[Checkmark]
6,167,763				[Checkmark]
6,196,980				[Checkmark]
6,248,083				[Checkmark]
6,270,464				[Checkmark]
6,318,992	[Checkmark]			
6,356,782				[Checkmark]
6,547,817	[Checkmark]			
6,699,205				[Checkmark]
6,716,240	[Checkmark]			
6,746,773	[Checkmark]			
6,976,965				[Checkmark]
7,008,439	[Checkmark]			
7,080,768	[Checkmark]			
7,128,744	[Checkmark]			
7,176,709	[Checkmark]			
7,290,692	[Checkmark]			
7,429,270	[Checkmark]			
7,591,844	[Checkmark]			

& Pat. No.		
7,785,302	[Checkmark]	
7,785,334		[Checkmark]
7,806,905		[Checkmark]

[*519]

Industry Classification & Patent Data	
BEA Code & Pat. No.	**BEA Title & Patent Title**
7,824,420	Implantable prosthesis
7,846,207	Intervertebral implant
7,862,616	Intervertebral implant
7,875,076	Intervertebral implant
7,947,022	Access port identification systems and methods
7,959,615	Access port identification systems and methods
8,021,324	Venous access port assembly with X-ray discernable indicia
10/766,295	Composite flexible endoscope insertion shaft with tubular substructure
12/220,804	MOTORIZED WHEELCHAIR AUXILARY SOLAR CAPACITY CHARGING SYSTEM
RE33,372	Tennis racket
RE42,379	Gas-tight seal accomodating surgical instruments with a wide range of diameters
311FT	Food & Beverage & Tobacco Products'
6,606,938	Two step puncturing and venting of single serve filter cartridge in a beverage brewer
6,610,344	Process for making a shaped snack chip
7,165,488	Brew chamber for a single serve beverage brewer
10/151,106	Personal nutrition control method
11/627,227	PERSONAL NUTRITION CONTROL METHOD
313TT	Textile Mills & Textile Product Mills
5,673,464	Cargo securement system and tie down strap
D596,439	Towel tote
315AL	Apparel & Leather & Allied Products
5,830,237	Gel and cushioning devices
6,385,779	Infant sock
D598,163	Slipper

& Pat. No.	
322	Paper Products
6,207,242	Paperboard packaging that is environmentally friendly, and has enhanced stiffness, strength, graphic and a white interior
7,348,067	Composite paperboards and method of making composite
323	paperboards Printing & Related Support Activities
6,213,703	Electronic bookstore vending machine
09/541,845	Method of image transfer on a colored base
324	Petroleum & Coal Products
325	Chemical Products
4,820,522	Oral sustained release acetaminophen formulation and process
4,968,509	Oral sustained release acetaminophen formulation and process
5,004,613	Oral sustained release pharmaceutical formulation and process
5,100,899	Methods of inhibiting transplant rejection in mammals using rapamycin and derivatives and prodrugs thereof
5,322,938	DNA sequence for enhancing the efficiency of transcription
5,344,691	Spatially modified elastic laminates
5,352,605	Chimeric genes for transforming plant cells using viral promoters
5,362,865	Enhanced expression in plants using non-translated leader sequences
5,378,619	Promoter for transgenic plants
5,424,412	Enhanced expression in plants
5,468,428	Spatially modified elastic laminates
5,502,077	Fatty acid composition
5,510,471	Chimeric gene for the transformation of plants
5,516,781	Method of treating restenosis with rapamycin
5,530,196	Chimeric genes for transforming plant cells using viral promoters
5,563,146	Method of treating hyperproliferative vascular disease
5,565,467	Androstenone derivative
5,593,874	Enhanced expression in plants
5,633,448	Chimeric gene for the transformation of plants
5,648,497	Retroviral protease inhibiting compounds
5,656,667	Fatty acid composition
5,658,589	Subcoated simulated capsule-like medicament
5,659,122	Enhanced expression in plants using non-translated leader sequences
5,700,460	Methods of attracting and combatting insects
5,710,023	IL-13 cytokine receptor chain
5,717,084	Chimaeric gene coding for a transit peptide and a heterologous peptide
5,728,925	Chimaeric gene coding for a transit peptide and a heterologous polypepfide
5,750,703	Piperidine derivatives and process for their production
5,789,395	Method of using tetracycline compounds for inhibition of endogenous nitric oxide production
5,792,930	Chimeric gene for the transformation of plants
5,800,808	Copolymer-1 improvements in compositions of copolymers
5,849,522	Enhancer for eukaryotic expression systems
5,859,347	Enhanced expression in plants

& Pat. No.			
7,824,420			[Checkmark]
7,846,207			[Checkmark]
7,862,616			[Checkmark]
7,875,076			[Checkmark]
7,947,022	[Checkmark]		
7,959,615	[Checkmark]		
8,021,324	[Checkmark]		
10/766,295	[Checkmark]		
12/220,804	[Checkmark]		
RE33,372	[Checkmark]		
RE42,379	[Checkmark]		
	[Checkmark]		
311FT 6,606,938	[Checkmark]		
6,610,344	[Checkmark]		
7,165,488		[Checkmark]	
10/151,106	[Checkmark]		
11/627,227	[Checkmark]		
313TT 5,673,464	[Checkmark]		
D596,439	[Checkmark]		
315AL 5,830,237	[Checkmark]		
6,385,779	[Checkmark]		
D598,183	[Checkmark]		
322 6,207,242	[Checkmark]		
7,348,067	[Checkmark]		
323 6,213,703	[Checkmark]		
09/541,845	[Checkmark]		
324			
325	[Checkmark]		
4,820,522	[Checkmark]		
4,968,509	[Checkmark]		
5,004,613	[Checkmark]		
5,100,899	[Checkmark]		
			[Checkmark]
5,322,938	[Checkmark]		
5,344,691	[Checkmark]		
5,352,605	[Checkmark]		
5,362,865	[Checkmark]		
5,378,619	[Checkmark]		

& Pat. No.			
5,424,412	[Checkmark]		
5,468,428	[Checkmark]		
5,502,077	[Checkmark]		
5,510,471			[Checkmark]
5,516,781	[Checkmark]		
5,530,196	[Checkmark]		
5,563,146	[Checkmark]		
5,565,467			[Checkmark]
5,593,874	[Checkmark]		
5,633,448			[Checkmark]
5,648,497			[Checkmark]
5,656,667	[Checkmark]		
5,658,589	[Checkmark]		
5,659,122	[Checkmark]		
5,700,460	[Checkmark]		
5,710,023	[Checkmark]		
5,717,084	[Checkmark]		
5,728,925	[Checkmark]		
5,750,703	[Checkmark]		
5,789,395	[Checkmark]		
5,792,930			[Checkmark]
5,800,808	[Checkmark]		
5,849,522	[Checkmark]		
5,859,347	[Checkmark]		

[*520]

Industry Classification & Patent Data		
BEA Code & Pat. No.	BEA Title & Patent Title	
5,860,283	8-alkoxyquinolonecarboxylic add hydrate with excellent stability and process for producing the same	
5,919,775	Method for inhibiting expression of inducible nitric oxide synthase with tetracycline	
5,981,589	Copolymer-1 improvements in compositions of copolymers	

& Pat. No.	
6,037,157	Method for improving pharmacokinetics
6,048,898	Copolymer-1 improvements in compositions of copolymers
6,051,753	Figwort mosaic virus promoter and uses
6,054,430	Copolymer-1 improvements in compositions of copolymers
6,153,401	Microorganisms and plasmids for 2,4-dichlorophenoxyacetic add (2,4-D) monooxygenase formation and process for the production of these plasmids and strains
6,200,604	Sublingual buccal effervescent
6,218,140	Enhancer for eukaryotic expression systems
6,239,113	Topical treatment or prevention of ocular infections
6,268,480	Amino add sequence of interleukin-13bc protein; recombinant production; drug screening of binding inhibitors
6,313,282	Isolated DNA sequence which can serve as terminator region in a chimeric gene capable of being used for the transformation of plants
6,331,415	Methods of producing immunoglobulins, vectors and transformed host cells for use therein
6,333,045	Gatifloxadn or its salt and disodium EDTA to prevent coloration; eye, ear or nose drops
6,338,961	Isolated DNA sequence capable of serving as regulatory element in a chimeric gene which can be used for the transformation of plants
6,342,476	Copolymer-1 improvements in compositions of copolymers
6,344,215	Methylphenidate modified release formulations
6,362,161	Copolymer-1 improvements on compositions of copolymers
6,362,396	Chimeric gene for the transformation of plants
6,372,494	Methods of making conditioned cell culture medium compositions
6,444,673	Optically active 5H-pyrrolo3,4-bpyrazine derivative, its preparation and pharmaceutical compositions containing it
6,465,504	Substituted 3,5-diphenyl-1,2,4-triazoles and their use as pharmaceutical metal chelators
6,506,400	Antiinfective free intramammary veterinary composition
6,566,587	Mutated 5-enolpyruvylshikimate-3-phosphate synthase, gene coding for said protein and transformed plants containing said gene
6,569,443	Topical treatment or prevention of ocular infections
6,596,750	Substituted 3,5-diphenyl-1,2,4-triazoles and their use as pharmaceutical metal chelators
6,598,603	Method for treating respiratory diseases
6,620,847	Copolymer-1 improvements in compositions of copolymers
6,677,358	NIDDM regimen
6,703,403	Method for improving pharmacokinetics
6,753,013	Pharmaceutical composition
6,893,662	Pharmaceutical dosage form with multiple coatings for reduced impact of coating fractures
6,939,539	Copolymer-1 improvements in compositions of copolymers
6,974,590	Sublingual buccal effervescent
7,030,149	Combination of brimonidine timolol for topical ophthalmic use
7,056,704	RNA interference mediating small RNA molecules
7,078,196	RNA interference mediating small RNA molecules
7,101,574	Pharmaceutical composition containing fenofibrate and the preparation method

& Pat. No.	
7,118,746	Conditioned cell culture medium compositions and methods of use
7,132,570	Method for the production of crystalline forms and crystalline forms of optical enantiomers of modafinil
7,148,359	Polymorph of a pharmaceutical
7,199,098	Copolymer-1 improvements in compositions of copolymers
7,211,267	Methods of treating acne
7,232,572	Methods of treating rosacea
7,320,976	Combination of brimonidine and timolol for topical ophthalmic use
7,323,463	Combination of brimonidine and timolol for topical ophthalmic use
7,344,568	Tear resistant gels, composites, and liner articles
7,348,362	Bronchodilating β-agonist compositions and methods
7,364,752	Solid dispersion pharamaceutical formulations
7,387,793	Modified release dosage forms of skeletal muscle relaxants
7,462,645	Bronchodilating beta-agonist compositions and methods
7,465,756	Bronchodilating beta-agonist compositions and methods
7,473,710	Bronchodilating beta-agonist compositions and methods
7,524,834	Sterile powders, formulations, and methods for producing the same
7,541,385	Bronchodilating β-agonist compositions and methods
7,544,372	Modified release dosage forms of skeletal muscle relaxants
7,597,910	Compositions and methods for treating prostate disorders
7,601,685	Growth factor modified protein matrices for tissue engineering
7,642,258	Combination of brimonidine and timolol for topical ophthalmic use
7,682,612	Treatment of hematologic malignandes assoaated with circulating

Industry Classification & Patent Data	2013 Litigation Data*		
BEA Code & Pat. No.	Fed. Cir.	E.D. Tex.	D. Del.
5,880,263			[Checkmark]
5,919,775	[Checkmark]		
5,981,589	[Checkmark]		
6,037,157			[Checkmark]
6,048,898	[Checkmark]		

& Pat. No.		
6,051,753	[Checkmark]	
6,054,430	[Checkmark]	
6,153,401	[Checkmark]	
6,200,604	[Checkmark]	
6,218,140	[Checkmark]	
6,239,113	[Checkmark]	
6,268,480	[Checkmark]	
6,313,282		[Checkmark]
6,331,415	[Checkmark]	
6,333,045		[Checkmark]
6,338,961		[Checkmark]
6,342,476	[Checkmark]	
6,344,215		[Checkmark]
6,362,161	[Checkmark]	
6,362,396		[Checkmark]
6,372,494	[Checkmark]	
6,444,673	[Checkmark]	
6,465,504		[Checkmark]
6,506,400	[Checkmark]	
6,566,587		[Checkmark]
6,569,443	[Checkmark]	
6,596,750		[Checkmark]
6,598,603	[Checkmark]	
6,620,847	[Checkmark]	
6,677,358	[Checkmark]	
6,703,403		[Checkmark]
6,753,013	[Checkmark]	
6,893,662		[Checkmark]
6,939,539	[Checkmark]	
6,974,590	[Checkmark]	
7,030,149	[Checkmark]	
7,056,704	[Checkmark]	
7,078,196	[Checkmark]	
7,101,574	[Checkmark]	
7,118,746	[Checkmark]	

& Pat. No.		
7,132,570		[Checkmark]
7,148,359		[Checkmark]
7,199,098	[Checkmark]	
7,211,267	[Checkmark]	
7,232,572	[Checkmark]	
7,320,976	[Checkmark]	
7,323,463	[Checkmark]	
7,344,568	[Checkmark]	
7,348,362	[Checkmark]	
7,364,752		[Checkmark]
7,387,793	[Checkmark]	
7,462,645	[Checkmark]	
7,465,756	[Checkmark]	
7,473,710	[Checkmark]	
7,524,834	[Checkmark]	
7,541,385	[Checkmark]	
7,544,372	[Checkmark]	
7,597,910		[Checkmark]
7,601,685	[Checkmark]	
7,642,258	[Checkmark]	
7,682,612	[Checkmark]	

[*521]

Industry Classification & Patent Data BEA Code" & Pat. No.	BEA Title & Patent Title
	tumor cells using chimeric anti-CD20 antibody
7,713,723	Alpha-amylase mutants with altered properties
7,749,532	Once daily formulations of tetracyclines
7,851,188	Fermentive production of four carbon alcohols
7,851,504	Enhanced bimatoprost ophthalmic solution

Code" & Pat. No.	& Patent Title
7,863,331	Pharmaceutical composition containing fenofibrate and method for the preparation thereof
7,879,930	Colored oxygen scavenging polymers
7,897,372	I-I meganuclease variants with modified specificity, method of preparation and uses thereof
7,923,221	Methods of making antibody heavy and light chains having specificity for a desired antigen
7,993,889	Fermentive production of four carbon alcohols
8,008,338	Ketorolac tromethamine compositions for treating or preventing ocular pain
8,017,375	Yeast organism producing isobutanol at a high yield
8,017,376	Methods of increasing dihydroxy acid dehydratase activity to improve production of fuels, chemicals, and amino adds
8,026,276	Parenteral CCI-779 formulations containing cosolvents, an antioxidant, and a surfactant
8,033,120	Compositions and methods containing fluorine substituted olefins
8,065,882	Compositions containing fluorine substituted olefins
8,067,361	Methods and compositions for increasing the anaerobic working capacity in tissues
8,133,890	Combination of brimonidine and timolol for topical ophthalmic use
8,187,344	Fuel composition for a diesel engine
8,206,740	Once daily formulations of tetracyclines
8,207,215	Ketorolac tromethamine compositions for treating or preventing ocular pain
8,212,094	Process for the manufacture of diesel range hydrocarbons
8,232,089	Cytosolic isobutanol pathway localization for the production of isobutanol
8,276,353	Enhanced bimatoprost ophthalmic solution
8,283,505	Recovery of higher alcohols from dilute aqueous solutions
8,299,118	Enhanced bimatoprost ophthalmic solution
8,354,409	Combination of brimonidine and timolol for topical ophthalmic use
8,377,982	Ketorolac tromethamine compositions for treating or preventing ocular pain
10/529,984	Enteric composition for the manufacture of soft capsule wall
10/650,509	Enzyme-mediated modification of fibrin for tissue engineering
11/358,951	Prevention of protein aggregation
RE37,516	Acetamide derivative having defined particle size
RE37,564	Composition for contraception
RE38,115	Treating chronic or intractable pain, for treating tinnitus and for treating sexual dysfunction
RE38,825	Genes encoding a glyphosate oxidoreductase enzyme; useful in producing transformed bacteria and plants which degrade glyphosate herbicide; crop plants which are tolerant to glyphosate herbicide

BEA Code" & Pat. No.	Patent Title
RE39,247	isolated DNA molecule encoding an EPSPS enzyme, producing transformed bacteria and plants which are tolerant to glyphosate herbicide while maintaining suitable phosphopyruvic acid ranges
326	Plastics & Rubber Products
4,848,437	Sunblind
5,176,774	Processes for manufacturing multilayer plastic sheet
5,199,592	Container with latchable hinged sidewall gate
5,501,679	Elastomeric laminates with microtextured skin layers
5,676,990	Method of food article dipping and wiping in a condiment container
5,691,034	Elastomeric laminates with microtextured skin layers
6,305,570	Closure assembly for a drinking vessel
6,433,264	Compensated nut for a stringed instrument
6,597,854	Optical cable exit trough
6,607,097	Collapsible bag for dispensing liquids and method
6,851,579	Collapsible bag for dispensing liquids and method
6,868,220	Optical cable exit trough
6,925,242	Optical cable exit trough
7,112,764	Disposable liner for cookware
7,120,963	Paint roller mounting assembly
7,152,840	Book holder
7,204,386	No-spill drinking cup apparatus
7,243,814	No-spill drinking cup apparatus
7,401,366	Children's play yard and elastic, removable liner
7,716,132	Fragrance product, dispenser, and dispenser assembly
7,722,819	Fragrance product, dispenser, and dispenser assembly
7,789,263	No-spill drinking cup apparatus

Industry Classification & Patent Data BEA Code" & Pat. No.	2013 Litigation Data Fed. Cir.	E.D. Tex	D. Del.
7,713,723	[checkmark]		
7,749,532	[checkmark]		[checkmark]
7,851,188			[checkmark]

Code"	Cir.	Tex		
& Pat. No.				
7,851,504			[checkmark]	
7,863,331	[checkmark]			
7,879,930				[checkmark]
7,897,372				[checkmark]
7,923,221	[checkmark]			
7,993,689				[checkmark]
8,008,338			[checkmark]	
8,017,375				[checkmark]
8,017,376				[checkmark]
8,026,276				[checkmark]
8,033,120	[checkmark]			
8,065,862	[checkmark]			
8,067,381				[checkmark]
8,133,890			[checkmark]	
8,187,344				[checkmark]
8,206,740				[checkmark]
8,207,215			[checkmark]	
8,212,094				[checkmark]
8,232,089				[checkmark]
8,278,353			[checkmark]	
8,283,505				[checkmark]
8,299,118			[checkmark]	
8,354,409			[checkmark]	
8,377,982			[checkmark]	
10/529,984	[checkmark]			
10/650,509	[checkmark]			
11/358,951	[checkmark]			
RE37,516	[checkmark]			
RE37,564	[checkmark]			
RE38,115				[checkmark]
RE38,825	[checkmark]			

BEA Code" & Pat. No.	Cir.	Tex			
RE39,247	[checkmark]				
326					
4,848,437	[checkmark]				
5,176,774	[checkmark]				
5,199,592	[checkmark]				
5,501,679	[checkmark]				
5,676,990	[checkmark]				
5,691,034	[checkmark]				
6,305,570		[checkmark]			
6,433,264	[checkmark]				
6,597,854	[checkmark]				
6,607,097					[checkmark]
6,851,579					[checkmark]
6,868,220	[checkmark]				
6,925,242	[checkmark]				
7,112,764		[checkmark]			
7,120,963	[checkmark]				
7,152,840	[checkmark]				
7,204,386		[checkmark]			
7,243,814		[checkmark]			
7,401,366	[checkmark]				
7,718,132	[checkmark]				
7,722,819	[checkmark]				
7,789,263		[checkmark]			

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Industry Classification & Patent Data BEA Code" & Pat. No.	BEA Title & Patent Title
7,789,264	No-spill drinking cup apparatus

Code" & Pat. No.	& Patent Title
7,919,159	Method to make single-layer PET bottles with high barrier and improved clarity
7,943,216	Method to make single-layer pet bottles with high barrier and improved clarity
8,044,942	Touch screen protector
08 /981,6 65	DEVICE FOR THE COLLECTION, TESTING AND SHIPMENT OF BODY FLUID SAMPLES
09/515,9 78	Compound mold and structured surface articles containing geometric structures with compound faces and method of making same
11 /061,3 27	Compound mold and structured surface articles containing geometric structures with compound faces and method of making same
11 /249,0 93	Vial for test strips
29/253,1 72	Portion of a Bottle
0572,961	Slip cover for play yard
RE43,077	No-spill drinking cup apparatus
42	Wholesale Trade
44RT	Retail Trade
5,576,951	Automated sales and services system
5,715,314	Network sales system
5,717,866	Method for comparative analysis of consumer response to product promotions
5,909,492	Network sales system
5,924,078	Consumer-provided promotional code actuatable point-of-sale discounting system
6,067,525	Integrated computerized sales force automation system
6,141,658	Computer system and method for managing sales information
6,553,350	Method and apparatus for pricing products in multi-level product and organizational groups
6,978,253	Systems and methods for transacting business over a global communications network such as the internet
7,941,341	Sales force automation system and method
8,112,359	Pre-sale data broadcast system and method
48TW	Transportation & Warehousing
481	Air Transportation
482	Rai Transportation
483	Water Transportation
484	Truck Transportation
485	Transit & Ground Passenger Transportation
486	Pipeline Transportation
487OS	Other Transportation & Support Activities
6,401,078	Bill of lading transmission and processing system for less than a load carriers
493	Warehousing & Storage

Code" & Pat. No.	& Patent Title
51	Information
511	Publishing Industries, except Internet (Includes Software)
5,394,140	Method and apparatus for pre-programmed call-back-number-determined alert
5,544,360	Method for accessing computer files and data, using linked categories assigned to each data file record on entry of the data file record
5,664,133	Context sensitive menu system / menu behavior
5,737,394	Portable telephone apparatus having a plurality of selectable functions activated by the use of dedicated and / or soft keys
5,915,239	Voice-controlled telecommunication terminal
5,978,791	Data processing system using substantially unique identifiers to identify data items, whereby identical data items have the same identifiers
6,015,088	Decoding of real time video imaging
6,070,068	Communication terminal device and method for controlling a connecting state of a call into a desired connection state upon a predetermined operation by a user
6,167,520	System and method for protecting a client during runtime from hostile downloadables
6,173,316	Wireless communication device with markup language based man-machine interface
6,181,836	Method and system for non-destructive image editing
6,195,662	System for transforming and exchanging data between distributed heterogeneous computer systems
6,253,075	Method and apparatus for incoming call rejection
6,308,565	System and method for tracking and assessing movement skills in multidimensional space
6,393,430	Method and system for automatically recording music data files by using the hard drive of a personal computer as an intermediate storage medium

Industry Classification & Patent Data	2013 Litigation Data		
BEA Code" & Pat. No.	Fed. Cir.	E.D. Tex	D. Del.

Code"	Cir.	Tex	
& Pat. No.			
7,789,264		[checkmark]	
7,919,159			[checkmark]
7,943,216			[checkmark]
8,044,942	[checkmark]		
08 /981,6 65	[checkmark]		
09/515,9 76	[checkmark]		
11 /061,3 27	[checkmark]		
11 /249,0 93	[checkmark]		
29/253,1 72	[checkmark]		
0572,961	[checkmark]		
RE43,077		[checkmark]	
42			
44RT			
5,576,951		[checkmark]	
5,715,314	[checkmark]		
5,717,866			[checkmark]
5,909,492	[checkmark]		
5,924,078			[checkmark]
6,067,525		[checkmark]	
6,141,658	[checkmark]		
6,553,350	[checkmark]		
6,978,253	[checkmark]		
7,941,341		[checkmark]	
8,112,359			[checkmark]
48TW			
481			
482			
483			
484			
485			
486			
487OS			
6,401,078	[checkmark]		

Code"	Cir.	Tex		
& Pat.				
No.				
493				
51				
511				
5,394,140	[checkmark]			
5,544,360	[checkmark]			
5,664,133	[checkmark]			
5,737,394				[checkmark]
5,915,239				i
5,978,791			[checkmark]	
6,015,088				[checkmark]
6,070,068				[checkmark]
6,167,520	[checkmark]			
6,173,316			[checkmark]	
6,181,836				[checkmark]
6,195,662	[checkmark]			
6,253,075				[checkmark]
6,308,565				[checkmark]
6,393,430				[checkmark]

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Industry Classification & Patent Data	
BEA Code & Pat.	BEA Title & Patent Title

& Pat. No.	
6,430,997	System and method for tracking and assessing movement skills in multidimensional space
6,446,080	Method for creating, modifying, and playing a custom playlist, saved as a virtual CD, to be played by a digital audio/visual actuator device
6,466,236	System and method for displaying and manipulating multiple calendars on a personal digital assistant
6,513,058	Distribution of motion control commands over a network
6,516,236	Motion control systems
6,658,418	Authoring system for computer-based information delivery system
6,760,477	Method and apparatus for entering data strings including Hangul (Korean) and ASCII characters
6,760,728	Method and apparatus for importing and exporting directory and calendar information to and from personal information management applications
6,765,726	System and method for tracking and assessing movement skills in multidimensional space
6,826,762	Radio interface layer in a cell phone with a set of APIs having a hardware-independent proxy layer and a hardware-specific driver layer
6,876,496	System and method for tracking and assessing movement skills in multidimensional space
6,934,945	Method and apparatus for controlling communications
6,941,543	Motion control system and method
7,076,275	Method and system for single-step enablement of telephony functionality for a portable computer system
7,155,451	Automated browsing system for publishers and users on networks serving internet and remote devices
7,266,186	Method and apparatus for improved paging receiver and system
7,302,683	Method and apparatus for controlling communications
7,310,416	Method and apparatus for improved personal communication devices and systems
7,359,121	System and method for tracking and assessing movement skills in multidimensional space
7,461,353	Scalable display of internet content on mobile devices
7,469,381	List scrolling and document translation, scaling, and rotation on a touch-screen display
7,506,064	Handheld computer system that attempts to establish an alternative network link upon failing to establish a requested network link
7,583,197	Programmable communicator
7,644,376	Flexible architecture for notifying applications of state changes
7,676,411	Click based trading with intuitive grid display of market depth
7,685,055	System and method for automatic repositioning of market information in a graphical user interface
7,693,768	Click bawd trading with intuitive grid display of market depth
7,791,808	System and method for tracking and assessing movement skills

& Pat. No.	
	in multidimensional space
7,831,926	Scalable display of internet content on mobile devices
7,844,915	Application programming interfaces for scrolling operations
7,864,163	Portable electronic device, method, and graphical user interface for displaying structured electronic documents
7,904,374	Click based trading with intuitive grid display of market depth
7,945,544	Similarity-based access control of data in a data processing system
7,949,662	De-duplication of data in a data processing system
8,001,096	Computer file system using content-dependent file identifiers
8,073,557	Motion control systems
8,094,010	Programmable communicator
8,099,420	Accessing data in a data processing system
D604,305	Graphical user interface for a display screen or portion thereof
RE39,231	Communication terminal equipment and call incoming control method
RE40,081	Fast signal transforms with lifting steps
512	Motion Picture & Sound Recording Industries
7,346,545	Method and system for payment of intellectual property royalties by interposed sponsor on behalf of consumer over a telecommunications network
10/086,089	System and method for accessing authorized recordings
513	Broadcasting & Telecommunications
5,351,285	Multiple format telephonic interface control system
5,359,643	Telecommunications device with simplified calling procedures
5,563,883	Dynamic channel management and signalling method and apparatus
5,590,403	Method and system for efficiently providing two way communication between a central network and mobile unit
5,592,491	Wireless modem
5,661,516	System and method for selectively distributing commercial messages over a communications network
5,844,596	Two-way RF communication at points of convergence of wire pairs from separate internal telephone networks
6,021,433	System and method for transmission of data
6,195,551	Idle handoff controlling method in cellular communication system

Industry Classification & Patent Data	2013 Litigation Data		
BEA Code	Fed. Cir.	E.D. Tex.	D. Del.

& Pat. No.				
6,430,997				[checkmark]
6,446,080				[checkmark]
6,466,236			[checkmark]	
6,513,058			[checkmark]	
6,516,236			[checkmark]	
6,658,418			[checkmark]	
6,760,477				[checkmark]
6,760,728			[checkmark]	
6,765,726				[checkmark]
6,826,762	[checkmark]			
6,876,496				[checkmark]
6,934,945			[checkmark]	
6,941,543			[checkmark]	
7,076,275			[checkmark]	
7,155,451				[checkmark]
7,266,186	[checkmark]			
7,302,683			[checkmark]	
7,310,416	[checkmark]			
7,359,121				[checkmark]
7,461,353				[checkmark]
7,469,381	[checkmark]			
7,506,064			[checkmark]	
7,583,197				[checkmark]
7,644,376	[checkmark]			
7,676,411	[checkmark]			
7,685,055	[checkmark]			
7,693,768	[checkmark]			
7,791,808				[checkmark]

& Pat. No.				
7,831,926				[checkmark]
7,844,915	[checkmark]			
7,864,163	[checkmark]			
7,904,374	[checkmark]			
7,945,544			[checkmark]	
7,949,662			[checkmark]	
8,001,096			[checkmark]	
8,073,557			[checkmark]	
8,094,010				[checkmark]
8,099,420			[checkmark]	
D604,305	[checkmark]			
RE39,231				[checkmark]
RE40,081				[checkmark]
512				
7,346,545	[checkmark]			
10/086,089	[checkmark]			
513				
5,351,285	[checkmark]			
5,359,643				[checkmark]
5,563,883			[checkmark]	
5,590,403			[checkmark]	
5,592,491			[checkmark]	
5,661,516				[checkmark]
5,844,596				[checkmark]
6,021,433			[checkmark]	
6,195,551			[checkmark]	

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Industry Classification & Patent Data	
BEA Code	BEA Title & Patent Title

& Pat. No.	
6,237,025	Multimedia collaboration system
6,243,446	Distributed splitter for data transmission over twisted wire pairs
6,262,992	System and method for transporting a call in a telecommunication network
6,298,064	Broadband telecommunications system
6,343,084	Broadband telecommunications system
6,351,762	Method and system for log-in-based video and multimedia calls
6,430,395	Wireless private branch exchange (WPBX) and communicating between mobile units and base stations
6,452,932	Method, system and apparatus for telecommunications control
6,463,052	Method, system and apparatus for telecommunications control
6,473,429	Broadband telecommunications system
6,542,585	Distributed splitter for data transmission over twisted wire pairs
6,574,267	Rach ramp-up acknowledgement
6,587,441	Method and apparatus for transportation of data over a managed wireless network using unique communication protocol
6,633,561	Method, system and apparatus for telecommunications control
6,680,923	Communication system and method
6,873,694	Telephony network optimization method and system
6,947,748	OFDMA with adaptive subcarrier-cluster configuration and selective loading
6,978,143	Method and arrangement for managing packet data transfer in a cellular system
7,012,916	Method and apparatus for accessing communication data relevant to a target entity identified by a number string
7,035,914	System and method for transmission of data
7,185,054	Participant display and selection in video conference calls
7,206,304	Method and apparatus for determining a telephone number for accessing a target entity
7,359,427	Rach ramp-up acknowledgement
7,454,212	OFDMA with adaptive subcarrier-cluster configuration and selective loading
7,525,484	Gateway and hybrid solutions for wireless location
7,706,830	Method and subscriber unit for performing an access procedure
7,764,231	Wireless location using multiple mobile station location techniques
7,783,299	Advanced triggers for location-based service applications in a wireless location system
7,903,641	Method and apparatus for accessing communication data relevant to a target entity identified by a number string
8,170,008	Method and apparatus for accessing communication data relevant to a target entity identified by a number string
8,189,565	Method and apparatus for accessing communication data relevant to a target entity identified by a number string
8,204,046	Method and apparatus for accessing service resource items that are for use in a telecommunications system
8,223,752	Method for accessing service resource items that are for use in a telecommunications system
514	Data Processing, Internet Publishing, Sr Other Information

& Pat. No.	
	Services
5,603,054	Method for triggering selected machine event when the triggering properties of the system are met and the triggering conditions of an identified user are perceived
5,771,354	Internet online backup system provides remote storage for customers using IDs and passwords which were interactively established when signing up for backup services
5,805,804	Method and apparatus for scalable, high bandwidth storage retrieval and transportation of multimedia data on a network
5,825,891	Key management for network communication
5,884,270	Method and system for facilitating an employment search incorporating user-controlled anonymous communications
5,884,272	Method and system for establishing and maintaining user-controlled anonymous communications
5,901,228	Commercial online backup service that provides transparent extended storage to remote customers over telecommunications links
5,930,474	Internet organizer for accessing geographically and topically based information
5,940,834	Automatic web page generator
5,944,839	System and method for automatically maintaining a computer system
5,999,908	Customer-based product design module
5,999,939	System and method for displaying and entering interactively modified stream data into a structured form
6,023,683	Electronic sourcing system and method
6,091,956	Situation information system
6,092,074	Dynamic insertion and updating of hypertext links for internet servers
6,151,309	Service provision system for communications networks
6,182,219	Apparatus and method for authenticating the dispatch and contents of documents
6,199,014	System for providing driving directions with visual cues
6,200,216	Electronic trading card

Industry Classification & Patent Data	2013 Litigation Data		
BEA Code & Pat. No.	Fed. Cir.	E.D. Tex.	D. Del.
6,237,025			[checkmark]
6,243,446			[checkmark]

& Pat. No.				
6,262,992				[checkmark]
6,298,064				[checkmark]
6,343,084				[checkmark]
6,351,762				[checkmark]
6,430,395	[checkmark]			
6,452,932				[checkmark]
6,463,052				[checkmark]
6,473,429				[checkmark]
6,542,585				[checkmark]
6,574,267				[checkmark]
6,587,441				[checkmark]
6,633,561				[checkmark]
6,680,923			[checkmark]	
6,873,694				[checkmark]
6,947,748			[checkmark]	
6,978,143			[checkmark]	
7,012,916				[checkmark]
7,035,914			[checkmark]	
7,185,054				[checkmark]
7,206,304				[checkmark]
7,359,427				[checkmark]
7,454,212			[checkmark]	
7,525,484			[checkmark]	
7,706,830	[checkmark]			
7,764,231			[checkmark]	
7,783,299				[checkmark]
7,903,641				[checkmark]
8,170,008				[checkmark]
8,189,565				[checkmark]
8,204,046				[checkmark]
8,223,752				[checkmark]
514				
5,603,054				[checkmark]

& Pat. No.				
5,771,354	[checkmark]			
5,805,804	[checkmark]			
5,825,891				[checkmark]
5,884,270				[checkmark]
5,884,272				[checkmark]
5,901,228	[checkmark]			
5,930,474			[checkmark]	[checkmark]
5,940,834				[checkmark]
5,944,839				[checkmark]
5,999,908			[checkmark]	
5,999,939				[checkmark]
6,023,683	[checkmark]			
6,091,956			[checkmark]	
6,092,074				[checkmark]
6,151,309				[checkmark]
6,182,219			[checkmark]	
6,199,014				[checkmark]
6,200,216			[checkmark]	

[*525]

Industry Classification & Patent Data	
BEA Code & Pat No.	**BEA Title & Patent Title**
6,397,040	Telecommunications apparatus and method
6,411,943	Internet online backup system provides remote storage for customers using IDs and passwords which were interactively established when signing up for backup services

No.	
6,415,280	Identifying and requesting data in network using identifiers which are based on contents of data
6,446,045	Method for using computers to facilitate and control the creating of a plurality of functions
6,446,111	Method and apparatus for client-server communication using a limited capability client over a low-speed communications link
6,490,525	Systems and methods for distributing real-time site-specific weather information
6,526,219	Picture-based video indexing system
6,549,942	Enhanced delivery of audio data for portable playback
6,571,334	Apparatus and method for authenticating the dispatch and contents of documents
6,578,054	Method and system for supporting offline mode of operation and synchronization using resource state information
6,578,079	Communications node for providing network based information service
6,581,065	Dynamic insertion and updating of hypertext links for internet servers
6,631,449	Dynamic distributed data system and method
6,738,799	Methods and apparatuses for file synchronization and updating using a signature list
6,826,598	Storage and retrieval of location based information in a distributed network of data storage devices
6,826,744	System and method for generating web sites in an arbitrary object framework
6,918,014	Dynamic distributed data system and method
6,925,481	Technique for enabling remote data access and manipulation from a pervasive device
6,928,442	Enforcement and policing of licensed content using content-based identifiers
6,963,908	System for transferring customized hardware and software settings from one computer to another computer to provide personalized operating environments
6,996,561	System and method for interactively entering data into a database
7,010,508	Automated multimedia data processing network
7,032,089	Replica synchronization using copy-on-read technique
7,065,637	System for configuration of dynamic computing

No.	
	environments using a visual interface
7,072,943	System and method for granting deposit-contingent E-mailing rights
7,080,051	Internet download systems and methods providing software to internet computer users for local execution
7,222,078	Methods and systems for gathering information from units of a commodity across a network
7,240,025	Internet advertising system and method
7,249,059	Internet advertising system and method
7,254,621	Technique for enabling remote data access and manipulation from a pervasive device
7,272,639	Internet server access control and monitoring systems
7,292,685	Pro-active features for telephony
7,366,709	System and method for managing questions and answers using subject lists styles
7,409,428	Systems and methods for messaging to multiple gateways
7,421,470	Method for real-time communication between plural users
7,433,921	System for real-time communication between plural users
7,441,196	Apparatus and method of manipulating a region on a wireless device screen for viewing, zooming and scrolling internet content
7,499,903	Semantic to non-semantic routing for locating a live expert
7,596,784	Method system and apparatus for providing pay-per-use distributed computing resources
7,620,565	Customer-based product design module
7,624,044	System for marketing goods and services utilizing computerized central and remote facilities
7,631,191	System and method for authenticating a web page
7,636,756	System and method for granting deposit-contingent e-mailing rights
7,707,624	System for, and method of, proving the transmission, receipt and content of a reply to an electronic message
7,716,629	System and method for generating web sites in an arbitrary object framework
7,725,546	System and method for granting deposit-contingent e-mailing rights
7,730,132	Storing and accessing media files
7,734,251	Signal processing apparatus and methods
7,756,855	Search phrase refinement by search term

No.	
	replacement
7,797,717	Signal processing apparatus and methods
7,802,310	Controlling access to data in a data processing system
7,822,813	Storing and accessing media files
7,831,663	Storage and playback of media files

Industry Classification & Patent Data BEA Code & Pat No.	2013 Litigation Data. Fed. Cir.	E.D. Tex.	D. Del.
6,397,040			[checkmark]
6,411,943	[checkmark]		
6,415,280		[checkmark]	
6,446,045	[checkmark]		
6,446,111	[checkmark]		
6,490,525	[checkmark]		
6,526,219		[checkmark]	
6,549,942			[checkmark]
6,571,334		[checkmark]	
6,578,054	[checkmark]		
6,578,079			[checkmark]
6,581,065			[checkmark]
6,631,449			[checkmark]
6,738,799			[checkmark]

No.			
6,826,598			[checkmark]
6,826,744		[checkmark]	
6,918,014			[checkmark]
6,925,481			[checkmark]
6,928,442		[checkmark]	
6,963,908			[checkmark]
6,996,561			[checkmark]
7,010,508		[checkmark]	
7,032,089			[checkmark]
7,065,637			[checkmark]
7,072,943			[checkmark]
7,080,051	[checkmark]		
7,222,078		[checkmark]	
7,240,025	[checkmark]		
7,249,059	[checkmark]		
7,254,621			
7,272,639	[checkmark]		
7,292,685			[checkmark]
7,366,709			[checkmark]
7,409,428	[checkmark]		
7,421,470			[checkmark]
7,433,921			[checkmark]
7,441,196		[checkmark]	

No.		
7,499,903		[checkmark]
7,596,784		[checkmark]
7,620,565	[checkmark]	
7,624,044	[checkmark]	
7,631,191	[checkmark]	
7,636,756		[checkmark]
7,707,624	[checkmark]	
7,716,629	[checkmark]	
7,725,546		[checkmark]
7,730,132		[checkmark]
7,734,251	[checkmark]	
7,756,855		[checkmark]
7,797,717	[checkmark]	
7,802,310	[checkmark]	
7,822,813		[checkmark]
7,831,663		[checkmark]

[*526]

Industry Classification & Patent Data	
BEA Code & Pat No.	**BEA Title & Patent Title**
7,836,474	Method and apparatus for preprocessing and postprocessing content in an interactive information distribution system
7,860,131	Signal processing apparatus and methods
7,865,557	System and method for verifying delivery and integrity of electronic messages
7,870,599	Multichannel device utilizing a centralized

No.	
	out-of-band authentication system (COBAS)
7,908,638	Signal processing apparatus and methods
7,941,357	Trading system
7,945,539	Distributing and accessing data in a data processing system
7,958,059	System and method for interactively entering data into a database
7,958,204	Community-selected content
7,962,561	System and method for granting deposit-contingent e-mailing rights
7,966,372	System and method for verifying delivery and integrity of electronic messages
7,992,172	Method and systems for multicast using multiple transport streams
8,150,239	Picture-based video indexing system
8,203,568	Sharing a graphical processing unit between a plurality of programs
11 /003,123	Accessing accessibility process
RE40,459	Method and apparatus for communicating information over low bandwidth communications networks
FIRE	Finance, Insurance, Real Estate, Rental, & Leasing
521C1-25	Finance & Insurance, including: > Federal Reserve Banks, Credit Intermediation, &' Related Activities; > Securities, Commodity Contracts, & Investments; > Insurance Carriers & Related Activities; and > Funds, Trusts, & Other Financial Vehicles
5,970,479	Methods and apparatus relating to the formulation and trading of risk management contracts
5,974,390	System and method for assuring predictable gains
6,000,608	Multifunction card system
6,189,787	Multifunctional card system
6,912,510	Methods of exchanging an obligation
6,945,457	Automated transaction machine
7,013,264	Component based interface to handle tasks during claim processing
7,096,003	Transaction security apparatus
7,149,720	Systems for exchanging an obligation
7,567,925	Point of service transaction management for service facilities
7,571,850	Automated transaction machine
7,575,158	Automated transaction machine
7,591,420	Automated transaction machine
7,597,248	Automated transaction machine
7,597,251	Automated transaction machine
7,600,677	Automated transaction machine
7,617,973	Automated transaction machine
7,621,444	Automated transaction machine
7,644,019	Safe transaction guaranty
7,699,220	Automated transaction machine

No.	
7,725,375	Systems and computer program products for exchanging an obligation
7,793,830	Automated transaction machine
7,802,718	Automated transaction machine
7,837,101	Automated transaction machine
7,912,740	System and method for processing work products for vehicles via the world wide web
8,200,513	System and method for processing work products for vehicles via the world wide web
11/871,992	Automated Qualifying of a Customer To Receive a Cash Loan at an Automated Teller Machine
531	Real Estate
5,032,989	Real Estate search and location system and method
532RL '	Rental & Leasing Services & Lessors of Intangible Assets
PROF	Professional & Business Services
5411	Legal Services
12/218,144	Methods for discriminately selecting U.S. patents and published U.S. patent applications for submission to the EUSPIDI in compliance with an applicant's duty of disclosure.
5415	Computer Systems Design & Related Services
4,956,835	Method and apparatus for self-restoring and self-provisioning communication networks
5,369,702	Distributed cryptographic object method
5,495,607	Network management system having virtual catalog overview of files distributively stored across network domain
5,511,122	Intermediate network authentication
5,680,452	Distributed cryptographic object method

Industry Classification & Patent Data	2013 Litigation Data.		
BEA Code & Pat No.	Fed. Cir.	E.D. Tex.	D. Del.
7,836,474			[checkmark]
7,860,131		[checkmark]	
7,865,557		[checkmark]	

No.			
7,870,599			[checkmark]
7,908,638		[checkmark]	
7,941,357			[checkmark]
7,945,539		[checkmark]	
7,958,059			[checkmark]
7,958,204		[checkmark]	
7,962,561			[checkmark]
7,966,372		[checkmark]	
7,992,172			[checkmark]
8,150,239		[checkmark]	
8,203,568			[checkmark]
11 /003,123	[checkmark]		
RE40,459		[checkmark]	
FIRE 521C1-25			
5,970,479	[checkmark]		
5,974,390			[checkmark]
6,000,608	[checkmark]	[checkmark]	
6,189,787		[checkmark]	
6,912,510	[checkmark]		
6,945,457			[checkmark]
7,013,284	[checkmark]		
7,096,003			[checkmark]
7,149,720	[checkmark]		
7,567,925			[checkmark]
7,571,850			[checkmark]
7,575,158			[checkmark]
7,591,420			[checkmark]
7,597,248			[checkmark]
7,597,251			[checkmark]
7,600,677			[checkmark]
7,617,973			[checkmark]
7,621,444			[checkmark]

No.		
7,644,019		[checkmark]
7,699,220		[checkmark]
7,725,375	[checkmark]	
		[checkmark]
7,793,830		[checkmark]
7,802,718		[checkmark]
7,837,101		[checkmark]
7,912,740		
8,200,513		[checkmark]
11/871,992	[checkmark]	
531		
5,032,989	[checkmark]	
532RL '		
PROF		
5411		
12/218,144	[checkmark]	
5415		
4,956,835	[checkmark]	
5,369,702	[checkmark]	
5,495,607		[checkmark]
5,511,122	[checkmark]	
5,660,452	[checkmark]	

[*527]

Industry Classification & Patent Data		
BEA Code & Pat. No.	BEA Title & Patent Title	

& Pat. No.	
5,850,505	Method for preconfiguring a network to withstand anticipated failures
5,898,781	Distributed cryptographic object method
6,061,796	Multi-access virtual private network
6,158,011	Multi-access virtual private network
6,321,338	Network surveillance
6,377,543	Path restoration of networks
6,421,349	Distributed preconfiguration of spare capacity in closed paths for network restoration
6,654,379	Integrated ring-mesh network
6,891,838	System and method for monitoring and controlling residential devices
6,914,880	Protection of routers in a telecommunications network
7,103,511	Wireless communication networks for providing remote monitoring of devices
7,260,059	Evolution of a telecommunications network from ring to mesh structure
7,580,974	Systems and methods for content type classification
7,697,492	Systems and methods for monitoring and controlling remote devices
7,979,543	Systems and methods for categorizing network traffic content
8,051,483	Systems and Methods for Updating Content Detection Devices and Systems
8,056,135	Systems and methods for updating content detection devices and systems
8,204,933	Systems and methods for content type classification
8,276,205	Systems and Methods for Updating Content Detection Devices and Systems
5412OP	Miscellaneous Professional, Scientific, & Technical Services
6,629,135	Affiliate commerce system and method
6,993,572	System and method for facilitating internet commerce with outsourced websites
7,818,399	Methods of expanding commercial opportunities for internet websites through coordinated offsite marketing
55	Management of Companies & Enterprises
561	Administrative & Support Services
6,744,858	System and method for supporting multiple call centers
6,990,458	System and method for computer-aided technician dispatch and communication
7,454,361	Individual seat selection ticketing and reservation system
7,548,866	Individual seat selection ticketing and reservation system
7,548,869	System and method for selecting and reserving sets of seats
7,660,728	System and method for selecting and reserving airline seats
7,725,344	System and method for computer-aided technician dispatch and communication
7,904,326	Method and apparatus for performing collective validation of credential information
7,908,304	Method and system for managing distributor information
7,958,024	Method and apparatus for processing sales transaction data
562	Waste Management & Remediation Services
4,737,356	Immobilization of lead and cadmium in solid residues from the combustion of refuse using lime and phosphate

& Pat. No.	
5,245,114	Immobilization of lead in bottom ash
5,424,944	System and methods for controlled asset disposition
5,430,233	Immobilization of lead in solid residues from reclaiming metals
10/413,849	Clarification of water and wastewater
6	Educational Services, Health Care, & Social Assistance
61	Educational Services
621-23	Health Care including: > Ambulatory Health Care Services; > Hospitals; and > Nursing & Residential Care Facilities
5,601,557	Anchoring and manipulating tissue
6,258,540	Non-invasive prenatal diagnosis
6,797,470	Detection of nucleic acid sequence differences using coupled ligase detection and polymerase chain reactions
7,083,917	Detection of nucleic acid sequence differences using the ligase detection reaction with addressable arrays
7,166,434	Detection of nucleic acid sequence differences using coupled ligase detection and polymerase chain reactions
7,171,277	System and method for controlling the delivery of medication to a patient
7,229,417	Methods for marking a biopsy site
7,312,039	Detection of nucleic acid sequence differences using coupled ligase detection and polymerase chain reactions
7,320,865	Detection of nucleic acid sequence differences using coupled ligase detection and polymerase chain reactions
7,332,285	Detection of nucleic acid sequence differences using coupled ligase detection and polymerase chain reactions
7,364,858	Detection of nucleic acid sequence differences using coupled ligase

Industry Classification & Patent Data	2013 Litigation Data		
BEA Code & Pat. No.	Fed. Cir.	E.D. Tex.	D. Del.
5,850,505	[checkmark]		
5,898,781	[checkmark]		
6,061,796		[checkmark]	
6,158,011		[checkmark]	

& Pat. No.				
6,321,338	[checkmark]			
6,377,543	[checkmark]			
6,421,349	[checkmark]			
6,654,379	[checkmark]			
6,891,838		[checkmark]		
6,914,880	[checkmark]			
7,103,511		[checkmark]		
7,260,059	[checkmark]			
7,580,974				[checkmark]
7,697,492		[checkmark]		
7,979,543				[checkmark]
8,051,483				[checkmark]
8,056,135				[checkmark]
8,204,933				[checkmark]
8,276,205				[checkmark]
5412OP				
6,629,135		[checkmark]		
6,993,572		[checkmark]		
7,818,389		[checkmark]		
55				
561				
6,744,858		[checkmark]		
6,990,458	[checkmark]			
7,454,361	[checkmark]			
7,548,866	[checkmark]			
7,548,869	[checkmark]			
7,660,728	[checkmark]			
7,725,344	[checkmark]			
7,904,326				[checkmark]
7,908,304				[checkmark]
7,958,024				[checkmark]
562				
4,737,356	[checkmark]			
5,245,114	[checkmark]			
5,424,944		[checkmark]		
5,430,233	[checkmark]			
10/413,849	[checkmark]			

& Pat. No.			
6 61 621-23			
5,601,557	[checkmark]		
6,258,540	[checkmark]		
6,797,470			[checkmark]
7,083,917			[checkmark]
7,166,434			[checkmark]
7,171,277			[checkmark]
7,229,417			[checkmark]
7,312,039			[checkmark]
7,320,865			[checkmark]
7,332,285			[checkmark]
7,364,858			[checkmark]

[*528]

Industry Classification & Patent Data	
BEA Code & Pat. No.	**BEA Title & Patent Title**
	detection and polymerase chain reactions
7,386,093	Gene for identifying individuals with familial dysautonomia
7,407,756	Methods for detecting mutations associated with familial dysautonomia
7,429,453	Detection of nucleic acid sequence differences using coupled ligase detection and polymerase chain reactions
7,625,397	Methods for defining and marking tissue
7,892,746	Detection of nucleic acid sequence differences using the

& Pat. No.	
	ligase detection reaction with addressable arrays
7,892,747	Detection of nucleic acid sequence differences using the ligase detection reaction with addressable arrays
7,893,233	Detection of nucleic acid sequence differences using the ligase detection reaction with addressable arrays
11/491,718	Method for prevention and treatment of Alzheimer's
624	Social Assistance
7	Arts, Entertainment, Recreation, Accommodation, & Food Services
711AS	Performing Arts, Spectator Sports, Museums, & Related Activities
713	Amusements, Gambling, & Recreation Industries
6,174,237	Method for a game of skill tournament
7,056,215	Slot machine game and system with improved jackpot feature
7,108,603	Slot machine game and system with improved jackpot feature
721	Accommodation
722	Food Services & Drinking Place
6,585,516	Method and system for computerized visual behavior analysis, training, and planning
81	Other Services, except Government
G	Government
09/832,440	Method and Apparatus for the Furnishing of Benefits Information and Benefits

Industry Classification & Patent Data	2013 Litigation Data		
BEA Code & Pat. No.	Fed. Cir.	E.D. Tex.	D. Del.
7,388,093	[checkmark]		
7,407,756	[checkmark]		
7,429,453			[checkmark]
7,625,397			[checkmark]
7,892,746			[checkmark]
7,892,747			[checkmark]

& Pat. No.				
7,893,233				[checkmark]
11/491,718	[checkmark]			
624				
7				
711AS				
713				
6,174,237				[checkmark]
7,056,215	[checkmark]			
7,108,603	[checkmark]			
721				
722				
6,585,516			[checkmark]	
81				
G				
09/832,440	[checkmark]			

[*529] A2: Summary of Economic, Trade, and Litigation Data

The following table summarizes the data of Appendix 0 along with the economic and trade data provided by the Bureau of Economic Analysis and the International Trade Administration: [40 &]

Industry Classification		2013 Economic & Trade Data	
BEA Code [42 &]	BEA Title	Value Added (Billions)	FTE [43 &] Employees (Thousands)
11	Agriculture, Forestry, Fishing, & Hunting	227	1161
111CA	Farms	192	676
113FF	Forestry, Fishing & Related Activities	35	485
21	Mining	430	795
22	Utilities	277	540
23	Construction	620	5809
31G	Manufacturing	2026	11749

321	Wood Products	2028	11749
327	Nonmetallic Mineral Products	40	365
331	Primary Metals	64	394
332	Fabricated Metal Product	140	1400
333	Machinery	145	1086
334	Computer & Electronic Products	255	1049
335	Electrical equipment, appliances, and components	51	366
336	Transportation equipment	261	1499
337	Furniture & Related Product	25	351
339	Miscellaneous (Durable Goods) Manufacturing	82	562
311FT	Food & Beverage & Tobacco Products	235	1597
313TT	Textile Mills & Textile Product Mills	17	223
315AL	Apparel & Leather & Allied Products	10	168
322	Paper Products	52	367
323	Printing & Related Support Activities	37	441
324	Petroleum & Coal Products	170	110
325	Chemical Products	346	786
326	Plastics & Rubber Products	73	644
42	Wholesale Trade	908	5554
44RT	Retail Trade	971	13078

Industry Classification		2013 Economic & Trade Data [41]	
BEA Code [42]	**BEA Title**	**Wages & Salaries Per FTE Employee**	**Import (Billions)**
11	Agriculture, Forestry, Fishing, & Hunting	36660	54
111CA	Farms	39460	537
113FF	Forestry, Fishing & Related Activities	32754	17
21	Mining	100002	292
22	Utilities	98904	
23	Construction	36056	
31G	Manufacturing	63625	1834
321	Wood Products	63625	1834
327	Nonmetallic Mineral	53753	19

		Employee	
	Products		
331	Primary Metals	64339	92
332	Fabricated Metal Product	53732	62
333	Machinery	66644	147
334	Computer & Electronic Products	103590	351
335	Electrical equipment, appliances, and components	65331	94
336	Transportation equipment	71509	334
337	Furniture & Related Product	42294	31
339	Miscellaneous (Durable Goods) Manufacturing	61481	108
311FT	Food & Beverage & Tobacco Products	46684	73
313TT	Textile Mills & Textile Product Mills	41746	27
315AL	Apparel & Leather & Allied Products	39199	122
322	Paper Products	65515	20
323	Printing & Related Support Activities	47900	5
324	Petroleum & Coal Products	108896	91
325	Chemical Products	91041	195
326	Plastics & Rubber Products	50573	47
42	Wholesale Trade	72362	
44RT	Retail Trade	33522	

Industry Classification		2013 Litigation Data			
BEA Code	BEA Title	Fed Cir.	E.D. Tex	D. Del.	Combined 44 &
11	Agriculture, Forestry, Fishing, & Hunting	7	0	1	8
111CA	Farms	7	0	1	8
113FF	Forestry, Fishing & Related Activities	0	0	0	0
21	Mining	0	0	0	0
22	Utilities	0	0	0	0
23	Construction	3	0	2	5
31G	Manufacturing	280	106	170	549
321	Wood Products	280	106	170	349
327	Nonmetallic Mineral Products	1	2	1	4
331	Primary Metals	0	0	2	2
332	Fabricated Metal Product	5	2	0	7

333	Machinery	30	1	0	31
334	Computer & Electronic Products	70	83	96	246
335	Electrical equipment, appliances, and components	8	0	12	17
336	Transportation equipment	10	0	2	12
337	Furniture & Related Product	0	0	0	0
339	Miscellaneous (Durable Goods) Manufacturing	30	2	16	48
311FT	Food & Beverage & Tobacco Products	4	1	0	5
313TT	Textile Mills & Textile Product Mills	2	0	0	2
315AL	Apparel & Leather & Allied Products	3	0	0	3
322	Paper Products	2	0	0	2
323	Printing & Related Support Activities	2	0	0	2
324	Petroleum & Coal Products	0	0	0	0
325	Chemical Products	85	8	37	129
326	Plastics & Rubber Products	22	7	4	33
42	Wholesale Trade	0	0	0	0
44RT	Retail Trade	5	3	3	11

Industry Classification		2013 Economic & Trade Data		
BEA Code 42 &	BEA Title	Value Added (Billions)	FTE 43 & Employees (Thousands)	
48TW	Transportation & Warehousing	481	4250	
481	Air Transportation	80	425	
482	Rail Transportation	44	189	
483	Water Transportation	16	63	
484	Truck Transportation	131	1323	
485	Transit & Ground Passenger Transportation	31	434	
486	Pipeline Transportation	21	41	
487OS	Other Transportation & Support Activities	109	1105	
493	Warehousing & Storage	50	670	
51	Information	779	2535	
511	Publishing Industries, except Internet (Includes Software)	207	759	
512	Motion Picture & Sound Recording Industries	115	333	

513	Broadcasting & Telecommunications	380	1107
514	Data Processing, Internet Publishing, & Other Information Services	77	335
FIRE	Finance, Insurance, Real Estate, Rental, & Leasing	3382	7607
521C	Finance & Insdrance, I-25 including: > Federal Reserve Banks, Credit Intermediation, & Related Activities; > Securities, Commodity Contracts, & Investments; > Insurance CarrierS & Related Activities; and > Funds; Trusts, & Other Financial Vehicles	1207	5720
531	Rental Estate	1989	1382
532RL	Rental & Leasing Services & Lessors of Intangible Assets	186	505
PROF	Professional & Business Services	1982	17406
5411	Legal Service	225	1090
5415	Computer Systems Design & Related Services	235	1624
5412OP	Miscellaneous Professional, Scientific, & Technical Services	696	5087
55	Management of Companies & Enterprises	323	1976
561	Administrative & Support Services	461	7266
562	Waste Management & Remediation Services	43	362
6	Educational Services, Health Care, & Social Assistance	1380	19156
61	Educational Services	185	3026
621-23	Heal Care, including: > Ambulatorylealth Care Services; > Hospitals; and > Nursing & Residential Care Facilities	1093	13265
624	Social Assistance	103	2865
7	Arts, Entertainment, Recreation, Accommodation, & Food Services	622	11534
711AS	Performing Arts, Spectator Sports, Museums, & Related Activities	90	478
713	Amusements, Gambling, &	73	1220

	Recreation Industries		
721	Accommodation	133	1687
722	Food Services & Drinking Places	325	8149
81	Other Services, except Government	369	5738
G	Government	2212	20074
	TOTAL	16768	126985

Industry Classification		2013 Economic & Trade Data 41 &	
BEA Code 42	**BEA Title**	**Wages & Salaries Per FTE Employee**	**Import (Billions)**
48T W	Transportation & Warehousing	5359	
481	Air Transportation	77984	
482	Rail Transportation	93688	
483	Water Transportation	84372	
484	Truck Transportation	48893	
485	Transit & Ground Passenger Transportation	32474	
486	Pipeline Transportation	124282	
487O S	Other Transportation & Support Activities	51618	
493	Warehousing & Storage	45578	
51	Information	94354	
511	Publishing Industries, except Internet (Includes Software)	112215	
512	Motion Picture & Sound Recording Industries	73889	
513	Broadcasting & Telecommunications	62205	
514	Data Processing, Internet Publishing, & Other Information Services	114360	
FIRE	Finance, Insurance, Real Estate, Rental, & Leasing	85443	
521C	Finance & Insurance, I-25 including: > Federal Reserve Banks, Credit Intermediation, & Related Activities; > Securities, Commodity Contracts, & Investments; > Insurance CarrierS &	95586	

		Employee
	Related Activities; and > Funds; Trusts, & Other Financial Vehicles	
531	Rental Estate	54696
532RL	Rental & Leasing Services & Lessors of Intangible Assets	55349
PROF	Professional & Business Services	70270
5411	Legal Service	90958
5415	Computer Systems Design & Related Services	106475
5412OP	Miscellaneous Professional, Scientific, & Technical Services	82651
55	Management of Companies & Enterprises	117063
561	Administrative & Support Services	38358
562	Waste Management & Remediation Services	56720
6	Educational Services, Health Care, & Social Assistance	49443
61	Educational Services	43667
621-23	Heal Care, including: > Ambulatoryllealth Care Services; > Hospitals; and > Nursing & Residential Care Facilities	55964
624	Social Assistance	25357
7	Arts, Entertainment, Recreation, Accommodation, & Food Services	28281
711AS	Performing Arts, Spectator Sports, Museums, & Related Activities	83148
713	Amusements, Gambling, & Recreation Industries	29973
721	Accommodation	35468
722	Food Services & Drinking Places	23320
81	Other Services, except Government	38926
G	Government	60183
	TOTAL	2180

Industry Classification		2013 Litigation Data			
BEA	BEA Title	Fed	E.D.	D.	Combined 44 &

48T W	Transportation & Warehousing	1	0	0	1
481	Air Transportation	0	0	0	0
482	Rail Transportation	0	0	0	0
483	Water Transportation	0	0	0	0
484	Truck Transportation	0	0	0	0
485	Transit & Ground Passenger Transportation	0	0	0	0
486	Pipeline Transportation	0	0	0	0
487O S	Other Transportation & Support Activities	1	0	0	1
493	Warehousing & Storage	0	0	0	0
51	Information	37	58	94	188
511	Publishing Industries, except Internet (Includes Software)	17	17	22	56
512	Motion Picture & Sound Recording Industries	2	0	0	2
513	Broadcasting & Telecommunications	3	12	27	42
514	Data Processing, Internet Publishing, & Other Information Services	15	29	45	88
FIRE	Finance, Insurance, Real Estate, Rental, & Leasing	8	2	19	28
521C	Finance & Insurance, I-25 including: > Federal Reserve Banks, Credit Intermediation, & Related Activities; > Securities, Commodity Contracts, & Investments; > Insurance CarrierS & Related Activities; and > Funds; Trusts, & Other Financial Vehicles	7	2	19	27
531	Rental Estate	1	0	0	1
532RL	Rental & Leasing Services & Lessors of Intangible Assets	0	0	0	0
PROF	Professional & Business Services	23	10	10	43
5411	Legal Service	1	0	0	1
5415	Computer Systems Design & Related Services	12	5	7	24
5412OP	Miscellaneous Professional, Scientific, & Technical Services	0	3	0	3
55	Management of Companies & Enterprises	0	0	0	0
561	Administrative & Support Services	6	1	3	10
562	Waste Management & Remediation Services	4	1	0	5
6	Educational Services, Health Care, & Social	5	0	14	19

	Assistance				
61	Educational Services	0	0	0	0
621-23	Heal Care, including: > Ambulatoryllealth Care Services; > Hospitals; and > Nursing & Residential Care Facilities	5	0	14	19
624	Social Assistance	0	0	0	0
7	Arts, Entertainment, Recreation, Accommodation, & Food Services	2	1	1	4
711AS	Performing Arts, Spectator Sports, Museums, & Related Activities	0	0	0	0
713	Amusements, Gambling, & Recreation Industries	2	0	1	3
721	Accommodation	0	0	0	0
722	Food Services & Drinking Places	0	1	0	1
81	Other Services, except Government	0	0	0	0
G	Government	1	0	0	1
	TOTAL	372	180	314	857

45

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Footnotes

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Email: tlau@fjc.gov

1 U.S. PAT. & TRADEMARK OFF., INTELLECTUAL PROPERTY AND THE U.S. ECONOMY: INDUSTRIES IN FOCUS 50 (2014).

President Barack H. Obama, Statement by the President (Aug. 2, 2011), *available at*http://www.whitehouse.gov/the-press-office/2011/08/02/statement-president (emphasis added).

4 Mark A. Lemley, *Rational Ignorance at the Patent Office*, 95 NW. U. L. REV. 1495, 1507 (2001).

5 John R. Allison, Mark A. Lemley, Sr David L. Schwartz, *Our Divided Patent System*, 82 U. CHI. L. REV. (forthcoming 2015).

6 Mark A. Lemley, *Ignoring Patents*, 2008 MICH. ST. L. REV. 19, 21 (2008).

7 We assume that the courts effectuate the economic power of patents through some substantive adjudication related to patents.

8 *See, e.g.*, BUREAU OF ECON. ANALYSIS, GDP BY INDUSTRY / VA, GO, II (2014), http://www.bea.gov/industry/xls/ io-annual/GDPbyInd_VA_NAICS_1997-2013.xlsx.

9 ECONOMICS & STAT. ADMIN. & U.S. PAT. & TRADEMARK OFF., INTELLECTUAL PROPERTY AND THE U.S. ECONOMY: INDUSTRIES IN FOCUS 5 (2012) [hereinafter *IP Report*], http://www.uspto.gov/news/publications/IP_Report_March_2012.pdf. For a discussion of the use of concordances to correlate patents with economic data, see Travis J. Lybbert & Nikolas J. Zolas,*Getting patents and economic data to speak to each other: An 'Algorithmic Links with Probabilities' Approach for Joint Analyses of Patenting and Economic Activity*, 43 RES. POL'Y 530 (2014).

10 *IP Report, supra* note 9, at 5.

11 Stephenson v. Game Show Network, LLC, 933 F. Supp. 2d 674 (D. Del. 2013).

12 *IP Report, supra* note 9, at 5.

15 35 U.S.C. § 271(b)-(c).

16 Shockley v. Arcan, Inc., 248 F.3d 1349, 1364 (Fed. Cir. 2001).

17 Codex Corp. v. Milgo Elec. Corp., 553 F.2d 735, 737-38 (1st Cir. 1977). *See also In re Nintendo of America, Inc.*, __ F.3d __ (Fed. Cir. 2014).

18 MobileMedia Ideas, LLC v. Apple Inc., 885 F. Supp. 2d 700, 702 (D. Del. 2012).

19 Allison, *supra* note 5.

20 Allison, *supra* note 5.

21 CENSUS BUREAU, *325 Chemical Manufacturing*, NORTH AMERICAN INDUSTRY CLASSIFICATION SYSTEM, http://www.census.gov/cgi-bin/sssd/naics/naicsrch?code=325&search=2012.

22 Allison, *supra* note 5.

23 28 U.S.C. § 1295.

24 BUREAU OF ECON. ANALYSIS, *supra* note 8.

25 INT'L TRADE ADMIN., PRODUCT PROFILES OF U.S. MERCHANDISE TRADE WITH A SELECTED MARKET, http://tse.export.gov/TSE/TSEReports.aspx?DATA=NTD.

26 Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (citation omitted).

assumptions rather than the data related to patents.

28 *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S __ (2012) (citation omitted).

29 That does not mean that mining as practiced within the United States is exempt from patent protection, because mining within the United States can be regulated by patents on mining technologies or methods. Unlike the products of mining, mining technologies or methods are not "natural phenomena."

30 The same thinking is applied by the USPTO when it assumes that all patents fall within the "Manufacturing" categories of the NAICS.

31 President Barack H. Obama, State of the Union Address (Jan. 28, 2014), *available at*http://www.whitehouse.gov/the-press-office/2014/01/28/president-barack-obamas-state-union-address.

32 n32 For a numerical comparison, we can look to the value added and import data of the top five litigated industries within the Federal Circuit:

Industry	Value Added (Billions)	Imports (Billions)
Chemical Products	346	195
Computer & Electronic Products	255	351
Machinery	145	147
Miscellaneous (Durable Goods) Manufacturing	82	108
Plastics & Rubber Products	73	47
TOTAL	901	849

It may be tempting to think that, because the total value added exceeds the value of the imported merchandise, the U.S. patents as litigated have more effect on domestic behavior than on foreign behavior. To begin with, it is safe to assume that the cost of production is much lower overseas. For example, it has been estimated that "[m]anufacturing an iPhone in the United States would cost about $ 65 more than manufacturing it in China, where it costs an estimated $ 8." Henry Blodget, *This Article Explains Why Apple Makes iPhones In China And Why The US Is Screwed*, BUSINESS INSIDER, Jan. 22, 2012, http://www.businessinsider.com/you-simply-must-read-this-article-that-explains-why-apple-makes-iphones-in-china-and-why-the-us-is-screwed-2012-1.

[34] U.S. PAT. & TRADEMARK OFF., INTELLECTUAL PROPERTY AND THE U.S. ECONOMY: INDUSTRIES IN FOCUS 50 (2014).

[35] 210 U.S. 405, 429-30 (1908).

[36] 19 U.S.C. § 1337(a)(2)-(3) (emphasis added).

[37] A useful comparison may be had with The Patents Act of India, which allows for the grant of compulsory licenses "if the working of the patented invention in the territory of India on a commercial scale is being prevented or hindered by the importation from abroad of the patented article." The Patents Act, No. 39 of 1970; India Code (2005), § 84.

[39] The BEA code is derived from the NAICS codes.

[38] As explained in Section 2.1, this data spans between January 1 and November 30 of 2013.

[39] The BEA code is derived from the NAICS codes.

[40] BUREAU OF ECON. ANALYSIS, *supra* note 9; INT'L TRADE ADMIN., *supra* note 27.

[43] FTE is "Full-Time Equivalent."

[42] The BEA codes are derived from the NAICS codes.

[41] As explained in Section 2.1, this data spans between January 1 and November 30 of 2013.

[43] FTE is "Full-Time Equivalent."

[42] The BEA codes are derived from the NAICS codes.

[41] As explained in Section 2.1, this data spans between January 1 and November 30 of 2013.

[42] The BEA codes are derived from the NAICS codes.

[44] "Combined" is not a simple sum of "Fed. Cir.," "E.D. Tex.," and "D. Del." because any patent can be litigated in more than one venue.

[45] Not including NAICS groups 980, "Goods Returned to Canada (Exports Only); U.S. Goods Returned & Reimported Items (Imports Only);" 980, "Special Classification Provisions"; 930, "Used or Second-Hand Merchandise"; and 910, "Waste & Scrap." These four account for $ 88 B.

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EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"8762923".pn.	US-PGPUB; USPAT	OR	ON	2019/12/12 11:52
S2	19	"33452226".fmid.	US-PGPUB; USPAT	OR	ON	2019/12/12 11:53
S3	76	(Hoberman-Barry-$ or Hillman-Daniel-$ or Shiell-Jon).in.	US-PGPUB; USPAT	OR	ON	2019/12/12 11:58
S4	1	("20020147932").PN.	US-PGPUB; USPAT	OR	ON	2019/12/12 12:22
S5	4	("20020188828"|"6166985"|"6535056"|"6785826").PN.	US-PGPUB; USPAT	OR	ON	2019/12/12 12:22
S6	52	("6047248"|"6076141"|"6711447"|"6820240"|"7111179"|"7642836"|"6513124"|"6076141"|"6779163"|"7111178"|"7279956"|"6717434"|"6968467"|"7058834"|"6908227"|"5996084"|"6141762"|"6438635"|"6667648"|"7051306"|"5778237"|"7415680"|"6631502"|"6779163"|"6883152"|"7085945"|"RE36839"|"5996083"|"20020140467"|"6631502"|"6779169"|"6883152"|"6345362"|"6411156"|"6415388"|"20020087904"|"20020140467"|"6523150"|"6598148"|"6889330"|"20020087904"|"6667648"|"6836849"|"6976182"|"7085945"|"5485127"|"5918061"|"5585745"|"7279956"|"7996811"|"5485127"|"6047248"|"6523150"|"6711447"|"6820240"|"6513124"|"6779169"|"7415680"|"7945885"|"5585745"|"6141762"|"6307281"|"6438635"|"7996811"|"6307281"|"6462976"|"6976182"|"7111178"|"5996084"|"6598148"|"6889330"|"7642836"|"5996083"|"7222244"|"0036839"|"5778237"|"6836849"|"6717434"|"7222244"|"6462976"|"7051306"|"7111179"|"7945885"|"RE36839"|"7254721"|"5719800"|"6477654"|"6484265"|"6496729"|"6895520").PN.	US-PGPUB; USPAT	OR	ON	2019/12/12 12:31
S7	412762	(H03K3/012 or H02J4/00 or G06F1/3203 or G06F1/324 or G06F1/3296 or H01L2924/00 or Y02D50/20 or Y02D10/126 or Y02D10/172 or Y10T307/414 or Y10T307/406 or H01L2924/0002).cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/14 12:31
S8	415	S7 and (power or voltage) near island	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/14 12:43
S9	625	S7 and dynamic$4 with (manag$5 or control$4) with (power or voltage or clock or frequency) with (island or domain or region or area or partition)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/14 12:57

EAST Search History (Prior Art)

S10	125	S7 and (plural$3 or multiple) near (power or voltage) near (manager or controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/14 13:11
S11	75	(S8 or S9 or S10) and @ad<"20040507"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/14 13:12
S12	796	(integrated near circuit or IC or SOC or chip) with (power or voltage) near island	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 17:38
S13	624	S12 and (power or voltage or clock or frequency) with (manag$5 or control$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 17:39
S14	190	S13 and (hierarch$4 or master or slave)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 17:43
S15	339	S13 and (plural$3 or multiple) with (manag$5 or control$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 17:46
S16	203607	(integrated near circuit or IC or SOC or chip) with power with (manag$5 or control$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 17:57
S17	11217	S16 and dynamic$4 with (manag$5 or control$4) with (power or voltage or clock or frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 17:58
S18	1757	S17 and (plural$3 or multiple or different) with (power or voltage or clock or frequency) with (island or domain or region or area or partition or section or block or unit) with (integrated near circuit or IC or SOC or chip)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 18:14
S19	769	S18 and (chang$3 or adjust$3) with voltage and (chang$3 or adjust$3) with (frequency or clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 18:15
S20	100	S19 and @ad<"20040507"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 18:16
S21	125	S13 and global and local	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/16 18:34

EAST Search History (Prior Art)

S22	203702	(integrated near circuit or IC or SOC or chip) with power with (manag$5 or control$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/17 14:00
S23	5449	S22 and power with (manag$5 or control$4) with (send$3 or receiv$3 or communicat$4) with (request or message)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/17 14:02
S24	916	S23 and (chang$3 or adjust$3) with voltage and (chang$3 or adjust$3) with (frequency or clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/17 14:03
S25	71	S24 and @ad<"20040507"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/17 14:06
S26	796	(integrated near circuit or IC or SOC or chip) with (power or voltage) near island	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/17 14:16
S27	137	S26 and (chang$3 or adjust$3) with voltage and (chang$3 or adjust$3) with (frequency or clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/17 14:16
S28	296	S26 and dynamic$4 with (power or voltage or clock or frequency)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/17 14:21
S30	127	S26 and (send$3 or receiv$3 or communicat$4) with (request or message)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2019/12/17 14:23

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Doc description: Information Disclosure Statement (IDS) Filed

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Filing Date	2016-06-24
First Named Inventor	HOBERMAN, Barry A.
Art Unit	2851
Examiner Name	Unknown
Attorney Docket Number	01181-US-REI

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	Art Unit	2851
	Examiner Name	Unknown
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Examiner Signature	/MICHAEL J. YIGDALL/	Date Considered	12/16/2019

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Doc description: Information Disclosure Statement (IDS) Filed

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Art Unit	2851
Examiner Name	TBD
Attorney Docket Number	01181-US-REI

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	1	6785826	B1	2004-08-31	DURHAM	
	2	6535056	B2	2003-03-18	MIZUNO	
	3	6166985		2000-12-26	MCDANIEL	

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	1	20020188828	A1	2002-12-12	SUGIMOTO	

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	1	1182548	EP	A2	2002-02-27	Texas Instruments France		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN, Barry A.
	Art Unit	2851
	Examiner Name	TBD
	Attorney Docket Number	01181-US-REI

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	1	Texas Instruments, "CMOS Power Consumption and Cpd Calculation", June 1997, pgs 16	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN
	Art Unit	2851
	Examiner Name	TBD
	Attorney Docket Number	6310

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	1	SARWAR Abdul, "CMOS Power Consumption And Cpd Calculation", Texas Instruments - SCAA035B, June 1997, 16 pgs	

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EFS ID:	36923132
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Do Hyung Kim/Julie McLeod
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Attorney Docket Number:	01181-US-REI
Receipt Date:	20-AUG-2019
Filing Date:	24-JUN-2016
Time Stamp:	12:32:40
Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2019_08_20_IDS_Submission.pdf	1034268 37cf0b8ad4e09c27ec60390653484d2bcefd6c9d	no	4

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Art Unit	2851
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Attorney Docket Number	01181-US-REI

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	2	6535056	B2	2003-03-18	MIZUNO	
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	1	1182548	EP	A2	2002-02-27	Texas Instruments France		

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(54) Dynamic hardware control for energy management systems using task attributes

(57) A multiprocessor system (10) includes a plurality of processing modules, such as MPUs (12), DSPs (14), and coprocessors/DMA channels (16). Power management software (38) in conjunction with profiles (36) for the various processing modules and the tasks to executed are used to build scenarios which meet predetermined power objectives, such as providing maximum operation within package thermal constraints or using minimum energy. Actual activities associated with the tasks are monitored during operation to ensure compatibility with the objectives. The allocation of tasks may be changed dynamically to accommodate changes in environmental conditions and changes in the task list. As each task in a scenario is executed, a control word associated with the task can be used to enable/disable circuitry, or to set circuits to an optimum configuration.

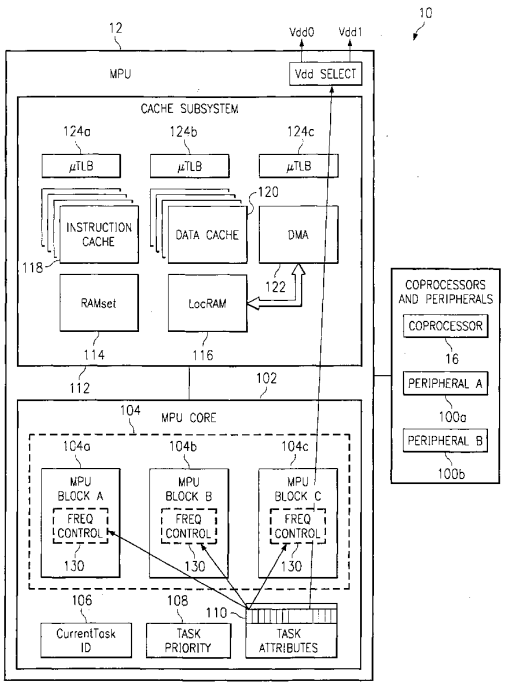


FIG. 12

EP 1 182 548 A2

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Description

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

[0001] This invention relates in general to integrated circuits and, more particularly, to managing energy in a processor.

2. DESCRIPTION OF THE RELATED ART

[0002] For many years, the focus of processor design, including designs for microprocessor units (MPUs), co-processors and digital signal processors (DSPs), has been to increase the speed and functionality of the processor. Presently, energy consumption has become a serious issue. Importantly, maintaining low energy consumption, without seriously impairing speed and functionality, has moved to the forefront in many designs. Energy consumption has become important in many applications because many systems, such as smart phones, cellular phones, PDAs (personal digital assistants), and handheld computers operate from a relatively small battery. It is desirable to maximize the battery life in these systems, since it is inconvenient to recharge the batteries after short intervals.

[0003] Currently, approaches to minimizing energy consumption involve static energy management; i.e., designing circuits which use less energy. In some cases, dynamic actions have been taken, such as reducing clock speeds or disabling circuitry during idle periods.

[0004] While these changes have been important, it is necessary to continuously improve energy management, especially in systems where size and, hence, battery size, is important to the convenience of using a device.

[0005] In addition to overall energy savings, in a complex processing environment, the ability to dissipate heat from the integrated circuit becomes a factor. An integrated circuit will be designed to dissipate a certain amount of heat. If tasks (application processes) require multiple hardware systems on the integrated circuit to draw high levels of current, it is possible that the circuit will overheat, causing system failure.

[0006] In the future, applications executed by integrated circuits will be more complex and will likely involve multiprocessing by multiple processors, including MPUs, DSPs, coprocessors and DMA channels in a single integrated circuit (hereinafter, a "multiprocessor system"). DSPs will evolve to support multiple, concurrent applications, some of which will not be dedicated to a specific DSP platform, but will be loaded from a global network such as the Internet. Accordingly, the tasks that a multiprocessor system will be able to handle without overheating will become uncertain.

[0007] Accordingly, a need has arisen for a method and apparatus for managing energy in a circuit without seriously impacting performance.

BRIEF SUMMARY OF THE INVENTION

[0008] In the present invention, a processing device is provided including a processing module coupled to one or more associated circuits for supporting the processing module, where the processing module is capable of multitasking multiple tasks. A memory stores a control word for selectively enabling or disabling the associated circuits, wherein each task has an associated control word which is stored in the memory while the task is being executed by the processing module.

[0009] The present invention provides significant advantages over the prior art by providing for a fully dynamic energy management. As the tasks executed in the processing system change, circuits that are not needed by the task can be disabled, thereby conserving energy.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0010] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

Figure 1 illustrates a block diagram of a multiprocessor system;

Figure 2 illustrates a software layer diagram for the multiprocessor system;

Figure 3 illustrates an example showing the advantages of energy management for a multiprocessor system;

Figures 4a and 4b illustrate flow diagrams showing preferred embodiments for the operation of the energy man-

agement software of Figure 2;

Figure 5 illustrates the building system scenario block of Figure 4;

Figure 6 illustrates the activities estimate block of Figure 4;

Figure 7 illustrates the power compute block of Figure 4;

Figure 8 illustrates the activity measure and monitor block of Figure 4;

Figure 9 illustrates a block diagram showing the multiprocessor system with activity counters;

Figure 10 illustrates a block diagram of a portion of a processing system showing a capability to manage power to various subcomponents;

Figure 11 illustrates the block diagram of Figure 10 during execution of a task to disable circuitry not needed by the task;

Figure 12 illustrates the block diagram of Figure 10 during execution of a task to configure certain circuits during operation of a task;

Figures 13a and 13b illustrate the configuration of a processing device to optimize the data bandwidth to the processing device;

Figure 14 illustrates the organization of a task attributes control word;

Figure 15 illustrates a functional depictions of the loading of the task attribute register (and other registers) in connection with a context switch; and

Figure 16 illustrates a mobile communications device using processing circuitry including the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0011] The present invention is best understood in relation to Figures 1-16 of the drawings, like numerals being used for like elements of the various drawings.

[0012] Figure 1 illustrates a general block diagram of a general multiprocessor system 10, including an MPU 12, one or more DSPs 14 and one or more DMA channels or coprocessors (shown collectively as DMA/Coprocessor 16). In this embodiment, MPU 12 includes a core 18 and a cache 20. The DSP 14 includes a processing core 22 and a local memory 24 (an actual embodiment could use separate instruction and data memories, or could use a unified instruction and data memory). A memory interface 26 couples a shared memory 28 to one or more of the MPU 12, DSP 14 or DMA/Coprocessor 16. Each processor (MPU 12, DSPs 14) can operate in full autonomy under its own operating system (OS) or real-time operating system (RTOS) in a real multiprocessor system, or the MPU 12 can operate the global OS that supervises shared resources and memory environment.

[0013] Figure 2 illustrates a software layer diagram for the multiprocessor system 10. As shown in Figure 1, the MPU 12 executes the OS, while the DSP 14 executes an RTOS. The OS and RTOSs comprise the OS layer 30 of the software. A distributed application layer 32 includes JAVA, C++ and other applications 34, power management tasks 38 which use profiling data 36 and a global tasks scheduler 40. A middleware software layer 42 communicates between the OS layer 30 and the applications in the distributed application layer 32.

[0014] Referring to Figures 1 and 2, the operation of the multiprocessor system 10 is discussed. The multiprocessor system 10 can execute a variety of tasks. A typical application for the multiprocessor system 10 would be in a smartphone application where the multiprocessor system 10 handles wireless communication, video and audio decompression, and user interface (i.e., LCD update, keyboard decode). In this application, the different embedded systems in the multiprocessor system 10 would be executing multiple tasks of different priorities. Typically, the OS would perform the task scheduling of different tasks to the various embedded systems.

[0015] The present invention integrates energy consumption as a criterion in scheduling tasks. In the preferred embodiment, the power management application 38 and profiles 36 from the distributed applications layer 32 are used to build a system scenario, based on probabilistic values, for executing a list of tasks. If the scenario does not meet predetermined criteria, for example if the power consumption is too high, a new scenario is generated. After an ac-

ceptable scenario is established, the OS layer monitors the hardware activity to verify that the activity predicted in the scenario was accurate.

[0016] The criteria for an acceptable task scheduling scenario could vary depending upon the nature of the device. One important criterion for mobile devices is minimum energy consumption. As stated above, as electronic communication devices are further miniaturized, the smaller battery allocation places a premium on energy consumption. In many cases during the operation of a device, a degraded operating mode for a task may be acceptable in order to reduce power, particularly as the batteries reach low levels. For example, reducing the LCD refresh rate will decrease power, albeit at the expense of picture quality. Another option is to reduce the MIPs (millions of instructions per second) of the multiprocessor system 10 to reduce power, but at the cost of slower performance. The power management software 38 can analyze different scenarios using different combinations of degraded performance to reach acceptable operation of the device.

[0017] Another objective in managing power may be to find the highest MIPs, or lowest energy for a given power limit setup.

[0018] Figures 3a and 3b illustrate an example of using the power management application 38 to prevent the multiprocessor system 10 from exceeding an average power dissipation limit. In Figure 3a, the DSP 14, DMA 16 and MPU 12 are concurrently running a number of tasks. At time t1, the average power dissipation of the three embedded systems exceeds the average limit imposed on the multiprocessor system 10. Figure 3b illustrates a scenario where the same tasks are executed; however, an MPU task is delayed until after the DMA and DSP tasks are completed in order to maintain an acceptable average power dissipation profile.

[0019] Figure 4a illustrates a flow chart describing operation of a first embodiment of the power management tasks 38. In block 50, the power management tasks are invoked by the global scheduler 40, which could be executed on the MPU 12 or one of the DSPs 14; the scheduler evaluate the upcoming application and splits it into tasks with associated precedence and exclusion rules. The task list 52 could include, for example, audio/video decoding, display control, keyboard control, character recognition, and so on. In step 54, the task list 52 is evaluated in view of the task model file 56 and the accepted degradations file 58. The task model file 56 is part of the profiles 36 of the distributed applications layer 32. The task model file 56 is a previously generated file that assigns different models to each task in the task list. Each model is a collection of data, which could be derived experimentally or by computer aided software design techniques, which defines characteristics of the associated task, such as latency constraints, priority, data flows, initial energy estimate at a reference processor speed, impacts of degradations, and an execution profile on a given processor as a function of MIPs and time. The degradation list 58 sets forth the variety of degradations that can be used in generating the scenario.

[0020] Each time the task list is modified (i.e., a new task is created or a task is deleted) or when a real time event occur, based on the task list 52 and the task model 56 in step 54, a scenario is built. The scenario allocates the various tasks to the modules and provides priority information setting the priority with which tasks are executed. A scenario energy estimate 59 at a reference speed can be computed from the tasks' energy estimate. If necessary or desirable, tasks may be degraded; i.e., a mode of the task that uses fewer resources may be substituted for the full version of a task. From this scenario, an activities estimate is generated in block 60. The activities estimate uses task activity profiles 62 (from the profiling data 36 of the distributed application layer 32) and a hardware architectural model 64 (also from the profiling data 36 of the distributed application layer 32) to generate probabilistic values for hardware activities that will result from the scenario. The probabilistic values include each module's wait/run time share (effective MHz), accesses to caches and memories, I/O toggling rates and DMA flow requests and data volume. Using a period T that matches the thermal time constant, from the energy estimate 59 at a reference processor speed and the average activities derived in step 60 (particularly, effective processors speeds), it is possible to compute an average power dissipation that will be compared to thermal package model. If the power value exceeds any thresholds set forth in the package thermal model 72, the scenario is rejected in decision block 74. In this case, a new scenario is built in block 54 and steps 60, 66 and 70 are repeated. Otherwise, the scenario is used to execute the task list.

[0021] During operation of the tasks as defined by the scenario, the OS and RTOSs track activities by their respective modules in block 76 using counters 78 incorporated in the hardware. The actual activity in the modules of the multiprocessor system 10 may vary from the activities estimated in block 60. The data from the hardware counters are monitored on a T periodic basis to produce measured activity values. These measured activity values are used in block 66 to compute an energy value for this period, and hence, an average power value in block 66, as described above, and are compared to the package thermal model in block 72. If the measured values exceed thresholds, then a new scenario is built in block 54. By continuously monitoring the measured activity values, the scenarios can be modified dynamically to stay within predefined limits or to adjust to changing environmental conditions.

[0022] Total energy consumption over T for the chip is calculated as:

$$E = \int_T \sum_{\text{modules}} \left[\alpha \cdot Cpd \cdot f \cdot V_{dd}^2\right] \cdot dt \equiv \sum_{\text{modules}} \left[\sum_T (\alpha \cdot)\right] \cdot Cpd \cdot f \cdot V_{dd}^2$$

where, f is the frequency, V_{dd} is the supply voltage and α is the probabilistic (or measured, see discussion in connection with block 76 of this figure) activity. In other words, $\Sigma_T(\alpha) * Cpd * f * V_{dd}^2$ is the energy corresponding to a particular hardware module characterized by equivalent dissipation capacitance Cpd ; counters values give $\Sigma_T(\alpha)$ and E is the sum of all energies for all modules in the multiprocessor system 10 dissipated within T. Average system power dissipation W = E/T. In the preferred embodiment, measured and probabilistic energy consumption is calculated and the average power dissipation is derived from the energy consumption over period T. In most cases, energy consumption information will be more readily available. However, it would also be possible to calculate the power dissipation from measured and probabilistic power consumption.

[0023] Figure 4b is a flow chart describing operation of a second embodiment of the power management tasks 38. The flow of Figure 4b is the same as that of Figure 41, except when the scenario construction algorithm is invoked (new task, task delete, real time event) in step 50, instead of choosing one new scenario, *n* different scenarios that match the performances constraints can be pre-computed in advance and stored in steps 54 and 59, in order to reduce the number of operations within the dynamic loop and provide faster adaptation if the power computed in the tracking loop leads to current scenario rejection in block 74. In Figure 4b, if the scenario is rejected, another pre-computed scenario is selected in block 65. Otherwise the operation is the same as shown in Figure 4a.

[0024] Figures 5 - 8 illustrate the operation of various blocks of Figure 3 in greater detail. The build system block 54 is shown in Figure 5. In this block, a task list 52, a task model 56, and a list of possible task degradations 58 are used to generate a scenario. The task list is dependent upon which tasks are to be executed on the multiprocessor system 10. In the example of Figure 5, three tasks are shown: MPEG4 decode, wireless modem data receive and keyboard event monitor. In an actual implementation, the tasks could come from any number of sources. The task model sets forth conditions which must be taken in consideration in defining the scenario, such as latency and priority constraints, data flow, initial energy estimates, and the impact of degradations. Other conditions could also be used in this block. The output of the build system scenario block is a scenario 80, which associates the various tasks with the modules and assigns priorities to each of the tasks. In the example shown in Figure 5, for example, the MPEG4 decode task has a priority of 16 and the wireless modem task has a priority of 4.

[0025] The scenarios built in block 54 could be based on a number of different considerations. For example, the scenarios could be built based on providing the maximum performance within the packages thermal constraints. Alternatively, the scenarios could be based on using the lowest possible energy. The optimum scenario could change during operation of a device; for example, with fully charged batteries a device may operate at a maximum performance level. As the power in the batteries diminished below a preset level, the device could operate at the lowest possible power level to sustain operation.

[0026] The scenario 80 from block 54 is used by the activities estimate block 60, shown in Figure 6. This block performs a probabilities computation for various parameters that affect power usage in the multiprocessor system 10. The probabilistic activities estimate is generated in conjunction with task activity profiles 62 and hardware architectural models 64. The task activity profiles include information on the data access types (load/store) and occurrences for the different memories, code profiles, such as the branches and loops used in the task, and the cycles per instruction for instructions in the task. The hardware architectural model 64 describes in some way the impact of the task activity profiles 62 on the system latencies, that will permit computation of estimated hardware activities (such as processor run/wait time share). This model takes into account the characteristics of the hardware on which the task will be implemented, for example, the sizes of the caches, the width of various buses, the number of I/O pins, whether the cache is write-through or write back, the types of memories used (dynamic, static, flash, and so on) and the clock speeds used in the module. Typically, the model can consist of a family of curves that represent MPU and DSP effective frequency variations with different parameters, such as data cacheable/non-cacheable, read/write access shares, number of cycles per instruction, and so on. In the illustrated embodiment of Figure 6, values for the effective frequency of each module, the number of memory accesses, the I/O toggling rates and the DMA flow are calculated. Other factors that affect power could also be calculated.

[0027] The power compute block 66 is shown in Figure 8. In this block, the probabilistic activities from block 60 or the measured activities from block 76 are used to compute various energy values and, hence, power values over a period T. The power values are computed in association with hardware power profiles, which are specific to the hardware design of the multiprocessor system 10. The hardware profiles could include a Cpd for each module, logic design style (D-type flip-flop, latches, gated clocks and so on), supply voltages and capacitive loads on the outputs. Power computations can be made for integrated modules, and also for external memory or other external devices.

[0028] Activity measure and monitor block 76 is shown in Figure 8. Counters are implemented throughout the multiprocessor system 10 to measure activities on the various modules, such as cache misses, TLB (translation lookaside

buffer) misses, non-cacheable memory accesses, wait time, read/write requests for different resources, memory overhead and temperature. The activity measure and monitor block 76 outputs values for the effective frequency of each module, the number of memory accesses, the I/O toggling rates and the DMA flow. In a particular implementation, other values may also be measured. The output of this block is sent to the power compute block 66.

[0029] Figure 9 illustrates and example of a multiprocessor system 10 using power/energy management software. In this example, the multiprocessor system 10 includes a MPU 12, executing an OS, and two DSPs 14 (individually referenced as DSP1 14a and DSP2 14b), each executing a respective RTOS. Each module is executing a monitor task 82, which monitors the values in various activity counters 78 throughout the multiprocessor system 10. The power compute task is executed on DSP 14a. The various monitor tasks retrieve data from associated activity counters 78 and pass the information to DSP 14a to calculate a power value based on measured activities. The power management tasks, such as power compute task 84 and monitor task 82, can be executed along with other application tasks.

[0030] In the preferred embodiment, the power management tasks 38 and profiles 36 are implemented as JAVA class packages in a JAVA real-time environment.

[0031] The embodiment shown above provides significant advantages over the prior art. First, it provides for a fully dynamic power management. As the tasks executed in the multiprocessor system 10 change, the power management can build new scenarios to ensure that thresholds are not exceeded. Further, as environmental conditions change, such as battery voltages dropping, the power management software can re-evaluate conditions and change scenarios, if necessary. For example, if the battery voltage (supply voltage) dropped to a point where Vdd could not be sustained at its nominal value, a lower frequency could be established, which would allow operation of the multiprocessor system 10 at a lower Vdd. New scenarios could be built which would take the lower frequency into account. In some instances, more degradations would be introduced to compensate for the lower frequency. However, the lower frequency could provide for continued operation of the device, despite supply voltages that would normally be insufficient. Further, in situations where a lower frequency was acceptable, the device could operate at a lower Vdd (with the availability of a switched mode supply) in order to conserve power during periods of relatively low activity.

[0032] The power management software is transparent to the various tasks that it controls. Thus, even if a particular task does not provide for any power management, the power management software assumes responsibility for executing the task in a manner that is consistent with the power capabilities of the multiprocessor system 10.

[0033] The overall operation of the power management software can be used with different hardware platforms, with different hardware and tasks accommodated by changing the profiles 36.

[0034] Figure 10 illustrates a portion of a processing system 10, showing a detailed block diagram of an autonomous processor (MPU 12), coupled to a coprocessor 16 along with other peripheral devices 100a and 100b. MPU 12 includes core circuitry 102, comprised of various core blocks 104a, 104b, and 104c. Core 102 further includes a Current Task ID register 106, a Task Priority register 108 and a Task Attributes register 110. Core 102 is coupled to a cache subsystem 112, including and instruction RAMset cache 114, a local RAM 116, an *n*-way instruction cache 118, an *n*-way data cache 120, a DMA (direct memory access) channel 122, and microTLB (translation lookaside buffer) caches 122a, 122b, and 122c. MPU 12 further includes voltage select circuitry 124 for selecting between two (or more) voltages to power the MPU 12.

[0035] The cache subsystem 112 shown in Figure 10 has several different caching circuits. The microTLBs 124a-c are a small TLB structures that cache a few entries, used where a larger TLB (typically providing 64 entries or more) would penalize the speed of the processor. The *n*-way caches 118 and 120 can be of conventional design (or could be a direct mapped cache). A RAMset cache is designed to cache a contiguous block of memory starting from a chosen main memory address location. The RAMset cache 114 can be designed as part of the *n*-way cache; for example, a 3-way instruction cache 118 could be configured as one RAM set cache and a 2-way set associative cache. The particulars of the cache subsystem shown in Figure 10 are provided only as an example; the cache subsystem could be varied by a circuit designer as desired.

[0036] For a given task, certain of the cache components may not be needed, or the cache components may be configured for optimal operation. For example, for a certain task, it may be desirable to configure a 4-way instruction cache as a RAMset cache 114 and a 3-way set associative cache, while the data cache 120 was configured as a direct mapping cache.

[0037] The voltage select circuitry 126 provides a supply voltage to the MPU 12. As is well known in the art, the voltage needed to support processing circuitry is dependent upon several factors; temperature and frequency are two of the more significant factors. For tasks where a high frequency is not needed, the voltage can be lowered to reduce energy consumption in the processing system 10.

[0038] One or more coprocessors and other peripheral devices may be used by the MPU 12 for various functions. The coprocessor 16 is used to provide high speed mathematical computations. Peripheral A 100a could be a input/output port, for example. Peripheral B could be a pointing device interface, such as a touch screen interface.

[0039] The MPU core 102 provides the processing function for MPU 12. This processing function is broken into multiple discrete blocks 104. Each block performs a function that may or may not be needed for a given task. For

example, floating point arithmetic unit, a multiplier, auxiliary accumulator, saturated arithmetic unit, count-leading-zeros logic, and so on, could each be treated as a MPU Block 104.

[0040] The Current Task ID register 106 stores a unique identifier for the current task being executed on the MPU 12. Other autonomous processors would also have a Current Task ID register 106 and may be executing a task different from the current task executed by the MPU 12. The Task Priority register 108 associates a priority with the task. The Task Attributes register 110 stores a control word having fields which can enable/ disable circuitry or configure circuitry to an optimum configuration.

[0041] The operation of the Task Attributes register 110 to enable or disable circuitry is shown in connection with Figure 11. The data stored in the Task Attributes register 110 has multiple fields which map to associated devices. For a simple on/off attribute, the field could be a single bit. Multiple bit fields can be provided for other functions, such as choosing between three or four voltages in the voltage select circuit 126.

[0042] Each of the components shown in Figure 11 as being mapped to the Task Attributes register 110 has circuitry that is responsive to a respective control field 128 in the register. For the voltage select circuit 126, one of multiple voltages is selected based on the value of the respective field 128. In Figure 11, Vdd0 could be chosen if the field is a "0" and Vdd1 could be chosen if the field is a "1". For a voltage select circuit with four possible voltages, Vdd0 could be chosen if the field is a "00" and Vdd1 could be chosen if the field is a "01", Vdd2 could be chosen if the field is a "10" and Vdd3 could be chosen if the field is a "11".

[0043] Coprocessor 16 is shown as disabled (power off), along with peripheral A 100a, while peripheral B 100b is shown as enabled. Each of these devices has an associated power switching circuit that supplies power to the component responsive to the value of the associated field in Task Attributes register 110. Disabling power to a component that is not used in a task can significantly reduce the overall power consumed by the processing system 10. Similarly, MPU block A 104a and MPU block C 104c are enabled, while MPU block B 104b is disabled.

[0044] In some cases, a hardware resource may be coupled to multiple autonomous processors. For example, a Level 2 shared memory may be coupled to both the MPU and the DSP. In cases where a hardware resource is shared between two or more autonomous processors, the resource can be coupled to the Task Attributes register 110 of each processor, and the subsystem can be enabled or disabled based on a logical operation on the associated bit values. For example, assuming that a bit value of "1" represented an "on" state for the hardware subsystem, a logical OR operation on the task attribute bits would enable the resource if either processor was executing a task that needed the resource.

[0045] Using the task attribute register as shown in Figure 11 can significantly reduce the power consumed by the processing system 10 by disabling circuitry which is not used by a specific task.

[0046] Figure 12 illustrates a second scenario where the voltage to the MPU 12 is reduced. In Figure 12, the Task Attributes register 110 provides voltage Vdd0 to MPU 12. It is assumed that Vdd0<Vdd1. To compensate for the reduction in supply voltage, the Task Attributes register 110 also configures the MPU blocks 104 to operate a lower frequency. Other subsystems in the MPU 12 may also be switched to a lower frequency due to the lower supply voltage.

[0047] This aspect of the invention can significantly reduce power consumption where a processing element can perform a task at a frequency lower than its maximum frequency.

[0048] Figures 13a and 13b illustrate the use of the Task Attributes register 110 to alter the configuration of the processing device 10 for more efficient operation. In this embodiment, the MPU Core 102 and Cache subsystem 112 are substantially the same as shown in Figures 10-12. A cache interface 130 couples the cache subsystem 112 to a traffic controller 132. Traffic controller 130 and cache interface 132 control the flow of traffic between the system buses and the components of the cache subsystem 112.

[0049] Importantly, cache interface 130 and traffic controller 132 are designed such that the bandwidth to components in the cache subsystem can be varied as desired. For example, Figure 13a illustrates a configuration where the currently executed task is computation intensive. In this configuration, the Task Attributes register 110 is set to provide a 64-bit instruction path to the instruction cache 118 and the microTLB register 124a and a 128-bit bi-directional path to the microTLB 124b, data cache 120 and local RAM 116. MicroTLB 124c, DMA 122 and RAMset cache 114 are turned off.

[0050] In Figure 13b, a new task is being executed resulting in a change in the task attribute register. The task shown in Figure 13b allocates high bandwidth to DMA transfer management, and a lower bandwidth for data and instruction transfers. Accordingly, a 64-bit input bus is shared between the microTLB 124a/RAMset 114 instruction caches and the microTLB 124b/local RAM 116 data caches. The 128-bit bi-directional bus is coupled to microTLB 124c and DMA circuit 122.

[0051] In addition to the bus configuration set by the cache interface 130 and traffic controller 132, the Task Attributes register 110 could also configure the cache architecture. In Figure 13b, cache resources can be allocated between the instruction cache 118 and RAMset cache 114. For example, the cache resources could be allocated as a 3-way set associative cache with a RAMset cache 114, a 2-way set associative cache with a larger RAMset cache, a 4-way set associative cache with no RAMset cache (as shown) or as a direct mapped cache with or without a RAMset cache 114. Depending upon the task (or scenario), the most efficient cache architecture could be chosen. Other hardware

could be configured for maximum efficiency as well.

[0052] As shown in Figure 14, some fields 128 in the Task Attributes register 110 may configure the processing device 10 for a given scenario while others configure the device 10 for on each task. Scenario specific attribute fields 128a remain the same while tasks are switched. For example, certain attributes, such as the core voltage to the processing device 10 or a system DMA controller, may be set for a scenario including several tasks which are being simultaneously executed by one or more processors. When the scenario changes, for example when a new task is executed or when of the current tasks is terminated, a new scenario is created, and the scenario specific attributes may change.

[0053] The task specific attribute fields 128b of Task Attributes register 110, on the other hand, may switch during multitasking of several tasks in a scenario. Each time a task becomes the active task in a processing element of the processing system 10, the attribute fields of that task overwrite the task specific attribute fields of the previous active task (scenario specific attribute fields 128a unchanged).

[0054] The task attribute fields for a given scenario and for each task in the scenario can be generated by the global tasks scheduler 40 based on the task list 52 and associated profiles 36, as shown in Figures 4a and 4b. The energy savings provided by the ability to enable/disable hardware and to configure hardware for optimum performance are taken into account in generating the scenario. An attribute word is computed for each task and stored as part of the task's context information. Upon a context switch, the attribute word for the active task is loaded into the Task Attributes register 110. The Current Task ID register 106 and Task Priority register 108 are also loaded at this time.

[0055] Figure 15 illustrates a function diagram showing the creation of the data used for the Task Attributes register 110. Upon the creation or deletion of a task, the global task scheduler 40 builds a scenario based on the task list 52 and associated models and profiles. Using this information, power and configuration attributes are computed for the run-time environment (the scenario attributes 128a) and also computes the priority information and the power and configuration attributes for the individual tasks in the scenario. For each task, the priority and attributes are stored in a respective task control block 129. Upon a context switch, where tasks are changed for a given processor, the information in the task control block for the new task are loaded into the appropriate registers. Task control blocks 129 may also contain other state information for the task that is restored upon the context switch.

[0056] Figure 16 illustrates an implementation of a mobile communications device 130 with microphone 132, speaker 134, keypad 136, display 138 and antenna 140. Internal processing circuitry 142 includes one or more processing devices with the energy saving features described herein. It is contemplated, of course, that many other types of communications systems and computer systems may also benefit from the present invention, particularly those relying on battery power. Examples of such other computer systems include personal digital assistants (PDAS), portable computers, personal digital assistants (PDAs), smart phones, web phones, and the like. As power dissipation is also of concern in desktop and line-powered computer systems and micro-controller applications, particularly from a reliability standpoint, it is also contemplated that the present invention may also provide benefits to such line-powered systems.

[0057] Telecommunications device 130 includes microphone 132 for receiving audio input, and speaker 134 for outputting audible output, in the conventional manner. Microphone 132 and speaker 134 are connected to processing circuitry 142, which receives and transmits audio and data signals.

[0058] Although the Detailed Description of the invention has been directed to certain exemplary embodiments, various modifications of these embodiments, as well as alternative embodiments, will be suggested to those skilled in the art. The invention encompasses any modifications or alternative embodiments that fall within the scope of the Claims.

Claims

1. A processing device comprising:

   a processing module capable of multitasking multiple tasks;
   one or more associated circuits, which may be selectively enabled and disabled responsive to a control signal, coupled to said processing module for supporting the processing module;
   a memory storing a control word for enabling and disabling the associated circuits, wherein each task has an associated control word which is stored in the memory while the task is being executed by the processing module.

2. The processing device of claim 1 wherein said control word comprises a plurality of fields.

3. The processing device of claim 2 wherein each of said associated circuits has an associated field.

4. The processing device of claim 3 wherein each of said associated circuits has power circuitry for either enabling

or disabling the associated circuit responsive to a value stored in said associated field.

5. The processing device of claim 1 wherein said processing module includes a plurality of processing subsystems which may be selectively enabled or disabled by said control word.

6. The processing device of claim 1 wherein said processing module is a microprocessor module.

7. The processing device of claim 1 wherein said processing module is a digital signal processor.

8. The processing device of claim 1 wherein at least one of said associated circuits is a caching circuit.

9. The processing device of claim 1 wherein one of said associated circuits is a coprocessor.

10. The processing device of claim 1 wherein said processing module comprises a first processing module, and further comprising one or more additional processing modules.

11. A method of operating a processing device including a processing module capable of multitasking multiple tasks coupled to one or more associated circuits, comprising the steps of:

identifying a current task; and
storing a control word associated with said current task in a memory; and
enabling the associated circuits during execution of said current task responsive to said control word.

12. The method of claim 11 wherein said storing step comprises the step of storing a control word having a plurality of predefined fields.

13. The method of claim 12 wherein each of said associated circuits has an associated field in said control word.

14. The method of claim 13 wherein said enabling or disabling step comprises the step of enabling or disabling each of the associated circuits responsive to a value stored in said associated field.

15. The method of claim 11 wherein said processing module includes a plurality of processing subsystems and further comprising the step of enabling or disabling said processing subsystems responsive to said control word.

16. The method of claim 11 wherein said processing module is a microprocessor module.

17. The method of claim 11 wherein said processing module is a digital signal processor.

18. The method of claim 11 wherein at least one of said associated circuits is a caching circuit.

19. The method of claim 11 wherein one of said associated circuits is a coprocessor.

20. The method of claim 11 wherein said processing module comprises a first processing module, and further comprising one or more additional processing modules.

21. A processing device comprising:

multiple processing modules each capable of multitasking multiple tasks;
one or more associated circuits shared between two or more processing modules, which may be selectively enabled and disabled responsive to a control signal, coupled to said processing modules for supporting the processing module;
multiple memories associated with respective processing modules for storing a control word for enabling and disabling the associated circuits, wherein each task has an associated control word which is stored in the memory while the task is being executed by the processing module.

22. A mobile communications device comprising:

an antenna for receiving and transmitting signals; and

receiver/transmitter circuitry for receiving and transmitting audio and data signals, said receiver/transmitter circuitry comprising:

a processing module capable of multitasking multiple tasks;
one or more associated circuits, which may be selectively enabled and disabled responsive to control signal, coupled to said processing module for supporting the processing module; and
a memory storing a control word for enabling and disabling the associated circuits, wherein each task has an associated control word which is stored in the memory while the task is being executed by the processing module.

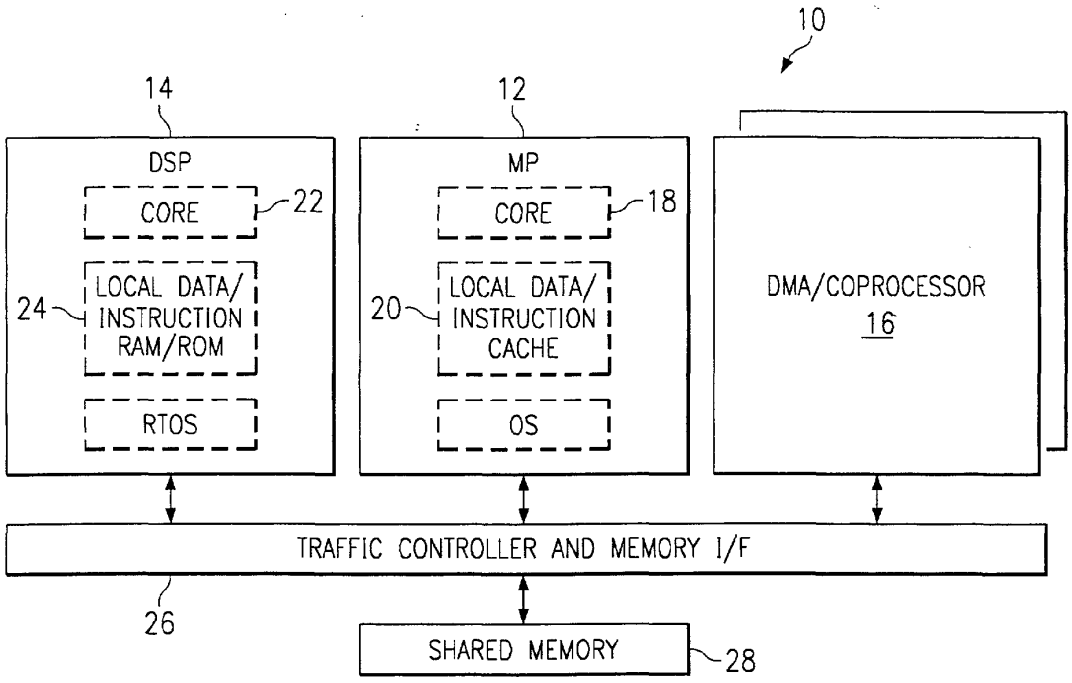

10
14
12
DSP
MP
CORE
22
CORE
18
LOCAL DATA/
INSTRUCTION
RAM/ROM
24
LOCAL DATA/
INSTRUCTION
CACHE
20
DMA/COPROCESSOR
16
RTOS
OS
TRAFFIC CONTROLLER AND MEMORY I/F
26
SHARED MEMORY
28

FIG. 1

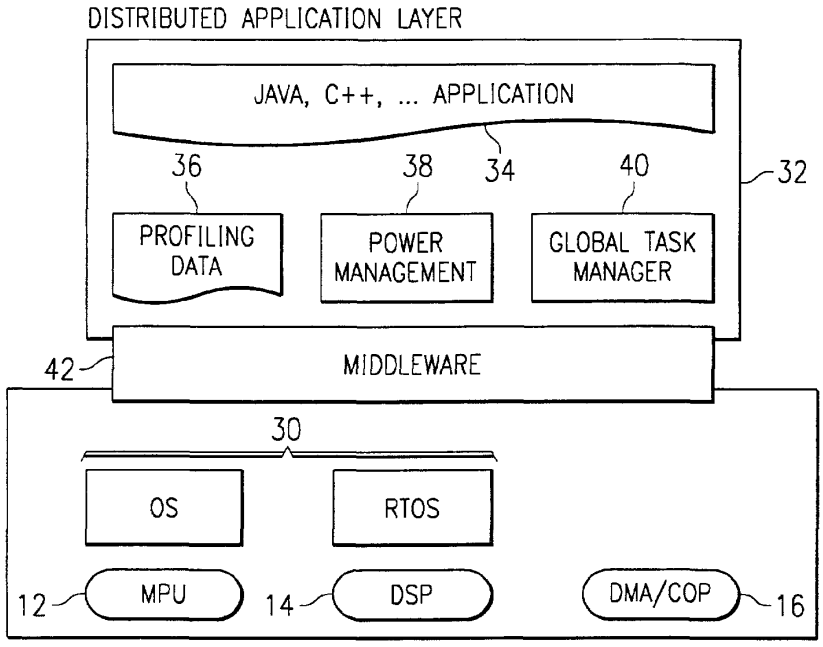

DISTRIBUTED APPLICATION LAYER
JAVA, C++, ... APPLICATION
36
38
34
40
32
PROFILING
DATA
POWER
MANAGEMENT
GLOBAL TASK
MANAGER
42
MIDDLEWARE
30
OS
RTOS
12
MPU
14
DSP
DMA/COP
16

FIG. 2

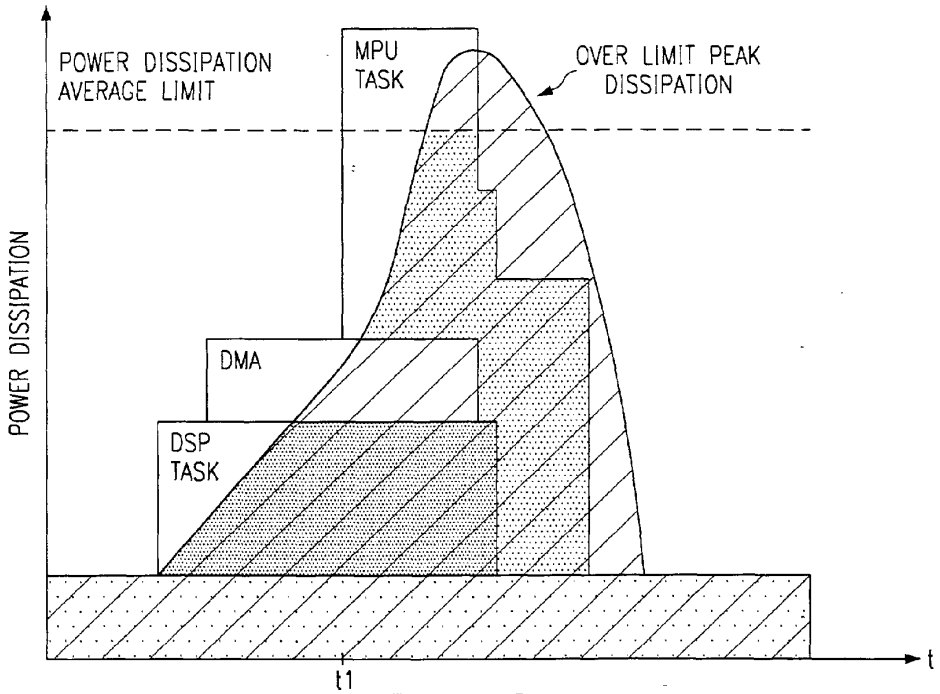

POWER DISSIPATION
AVERAGE LIMIT
MPU
TASK
OVER LIMIT PEAK
DISSIPATION
POWER DISSIPATION
DMA
DSP
TASK
t1
t

FIG. 3a

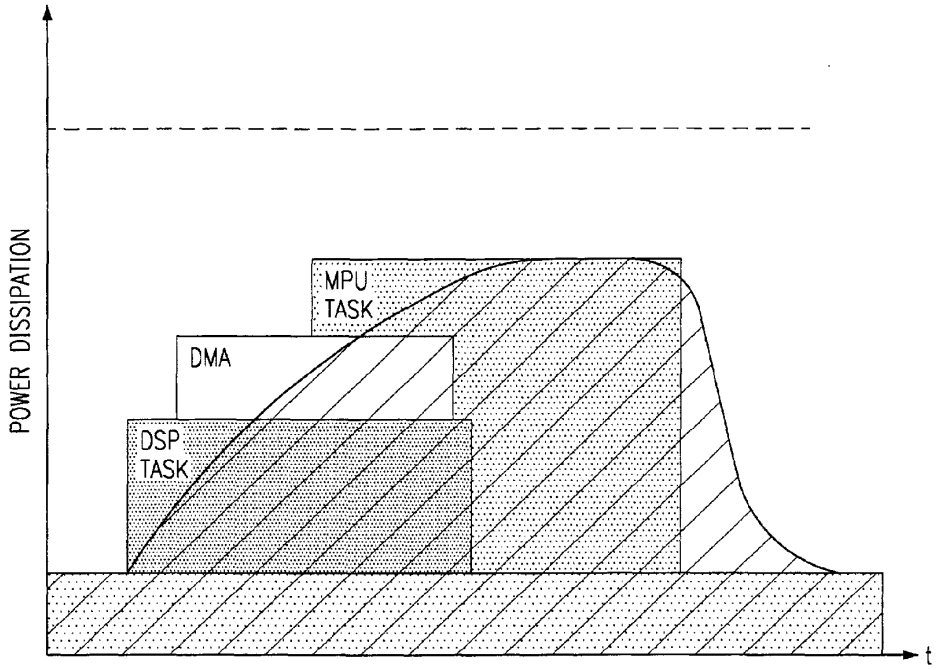

POWER DISSIPATION
MPU
TASK
DMA
DSP
TASK
t

FIG. 3b

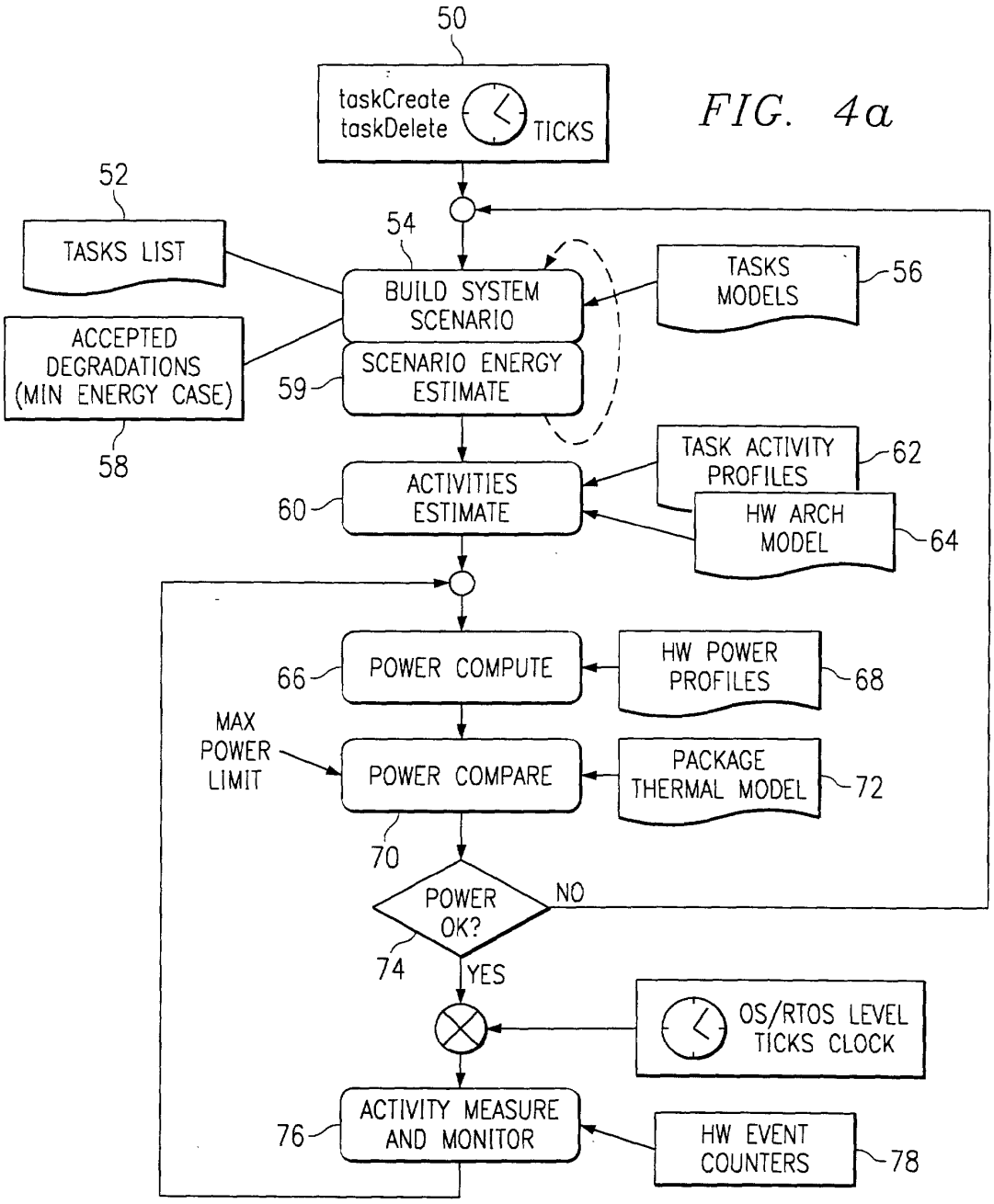

50
taskCreate
taskDelete
TICKS
52
TASKS LIST
54
BUILD SYSTEM SCENARIO
TASKS MODELS
56
ACCEPTED DEGRADATIONS (MIN ENERGY CASE)
58
59
SCENARIO ENERGY ESTIMATE
TASK ACTIVITY PROFILES
62
60
ACTIVITIES ESTIMATE
HW ARCH MODEL
64
66
POWER COMPUTE
HW POWER PROFILES
68
MAX POWER LIMIT
POWER COMPARE
PACKAGE THERMAL MODEL
72
70
POWER OK?
NO
74
YES
OS/RTOS LEVEL TICKS CLOCK
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78

FIG. 4a

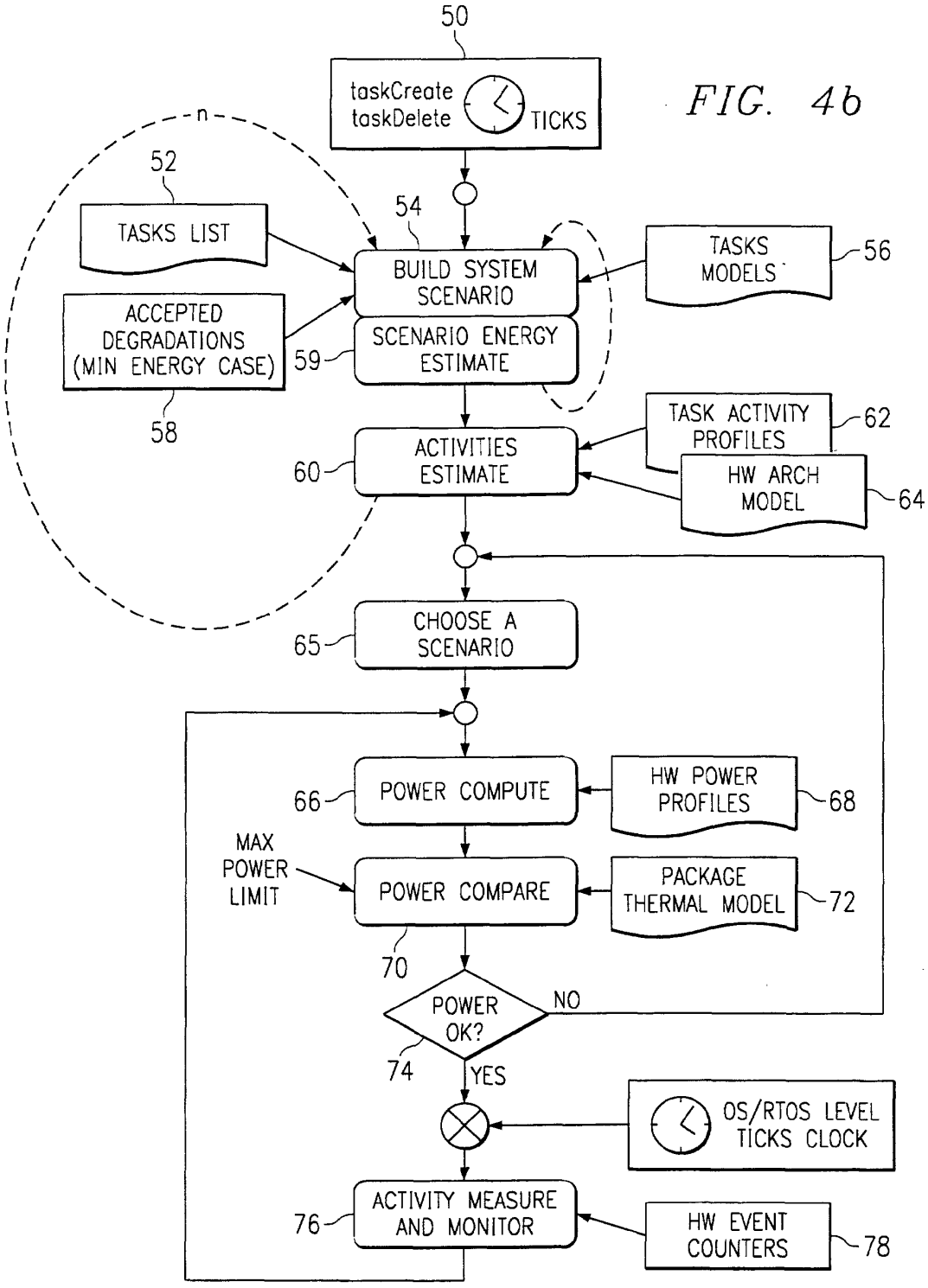

50
taskCreate
taskDelete
TICKS
n
52
TASKS LIST
54
BUILD SYSTEM SCENARIO
TASKS MODELS
56
ACCEPTED DEGRADATIONS (MIN ENERGY CASE)
58
59
SCENARIO ENERGY ESTIMATE
TASK ACTIVITY PROFILES
62
60
ACTIVITIES ESTIMATE
HW ARCH MODEL
64
65
CHOOSE A SCENARIO
66
POWER COMPUTE
HW POWER PROFILES
68
MAX POWER LIMIT
POWER COMPARE
PACKAGE THERMAL MODEL
72
70
POWER OK?
NO
74
YES
OS/RTOS LEVEL TICKS CLOCK
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78

FIG. 4b

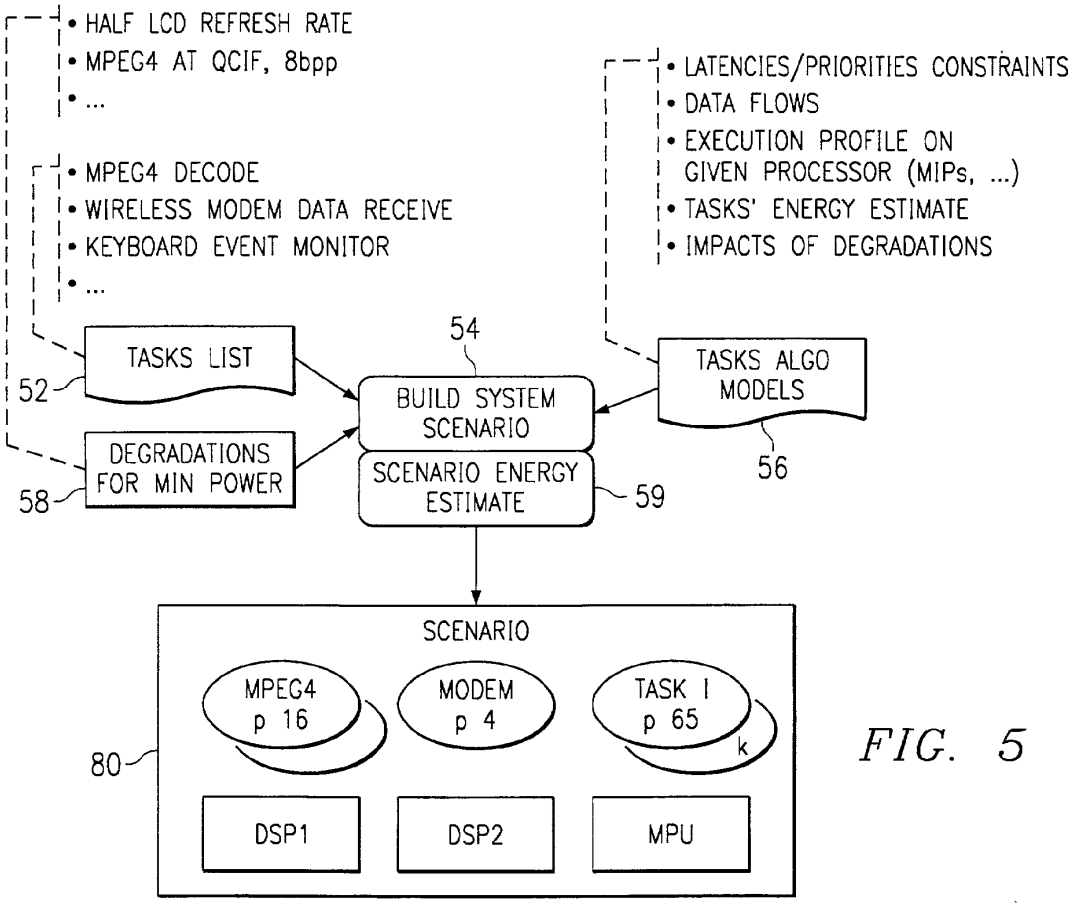

• HALF LCD REFRESH RATE
• MPEG4 AT QCIF, 8bpp
• ...
• MPEG4 DECODE
• WIRELESS MODEM DATA RECEIVE
• KEYBOARD EVENT MONITOR
• ...
• LATENCIES/PRIORITIES CONSTRAINTS
• DATA FLOWS
• EXECUTION PROFILE ON GIVEN PROCESSOR (MIPs, ...)
• TASKS' ENERGY ESTIMATE
• IMPACTS OF DEGRADATIONS
TASKS LIST
52
54
BUILD SYSTEM SCENARIO
TASKS ALGO MODELS
56
DEGRADATIONS FOR MIN POWER
58
SCENARIO ENERGY ESTIMATE
59
SCENARIO
MPEG4 p 16
MODEM p 4
TASK I p 65
k
80
DSP1
DSP2
MPU

FIG. 5

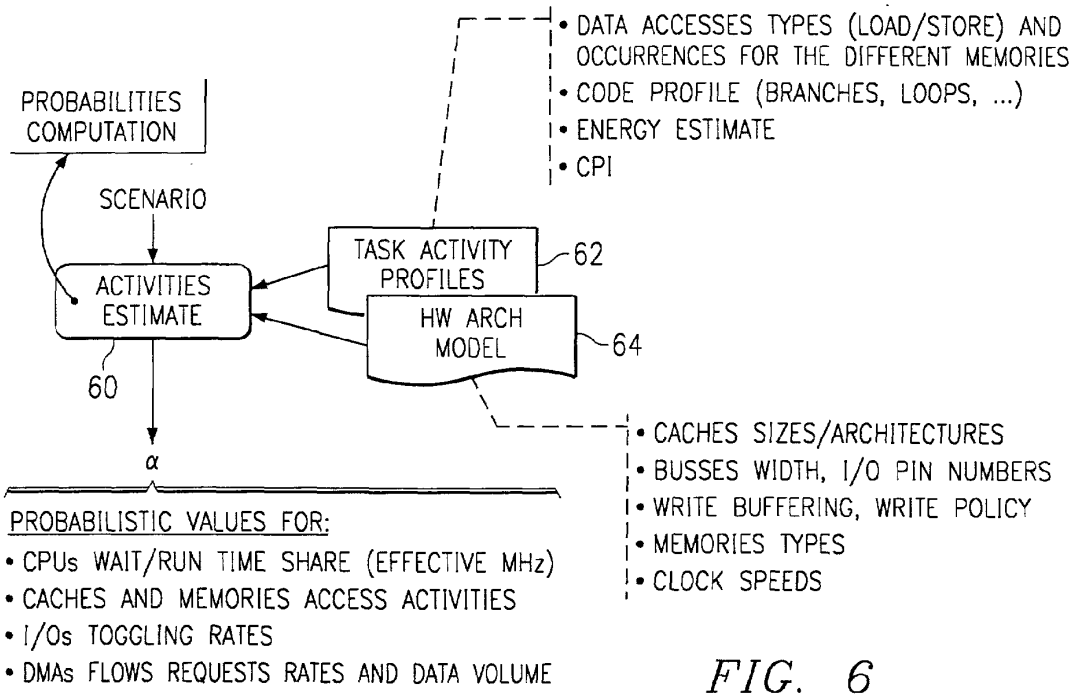

• DATA ACCESSES TYPES (LOAD/STORE) AND OCCURRENCES FOR THE DIFFERENT MEMORIES
• CODE PROFILE (BRANCHES, LOOPS, ...)
• ENERGY ESTIMATE
• CPI
PROBABILITIES COMPUTATION
SCENARIO
TASK ACTIVITY PROFILES
62
ACTIVITIES ESTIMATE
HW ARCH MODEL
64
60
α
• CACHES SIZES/ARCHITECTURES
• BUSSES WIDTH, I/O PIN NUMBERS
• WRITE BUFFERING, WRITE POLICY
• MEMORIES TYPES
• CLOCK SPEEDS
PROBABILISTIC VALUES FOR:
• CPUs WAIT/RUN TIME SHARE (EFFECTIVE MHz)
• CACHES AND MEMORIES ACCESS ACTIVITIES
• I/Os TOGGLING RATES
• DMAs FLOWS REQUESTS RATES AND DATA VOLUME

FIG. 6

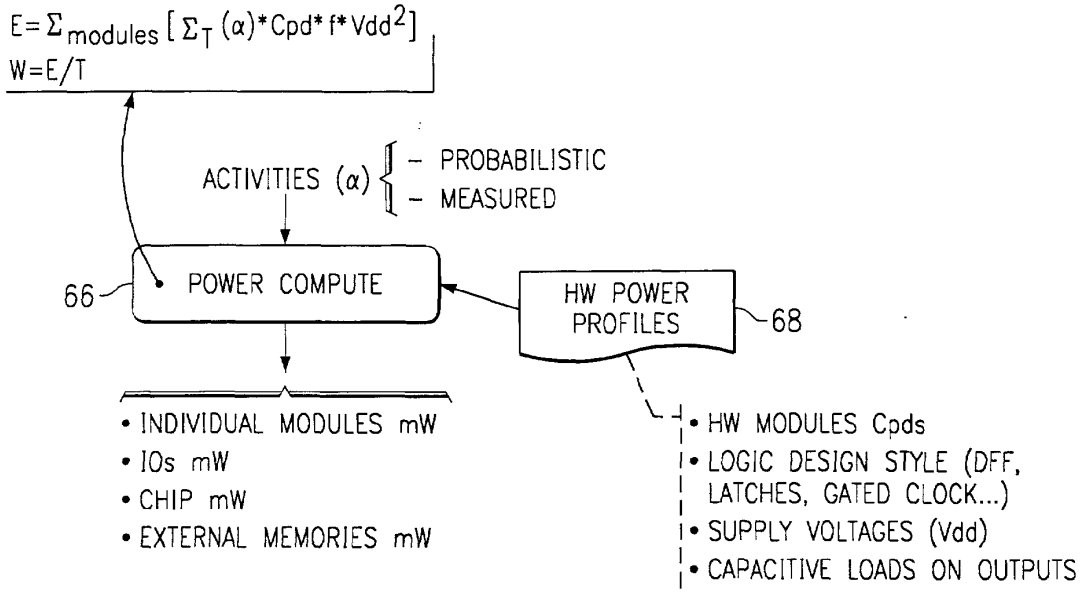

E=Σmodules [ΣT (α)*Cpd* f* Vdd2]
W=E/T
ACTIVITIES (α)
– PROBABILISTIC
– MEASURED
66
POWER COMPUTE
HW POWER PROFILES
68
• INDIVIDUAL MODULES mW
• IOs mW
• CHIP mW
• EXTERNAL MEMORIES mW
• HW MODULES Cpds
• LOGIC DESIGN STYLE (DFF, LATCHES, GATED CLOCK...)
• SUPPLY VOLTAGES (Vdd)
• CAPACITIVE LOADS ON OUTPUTS

FIG. 7

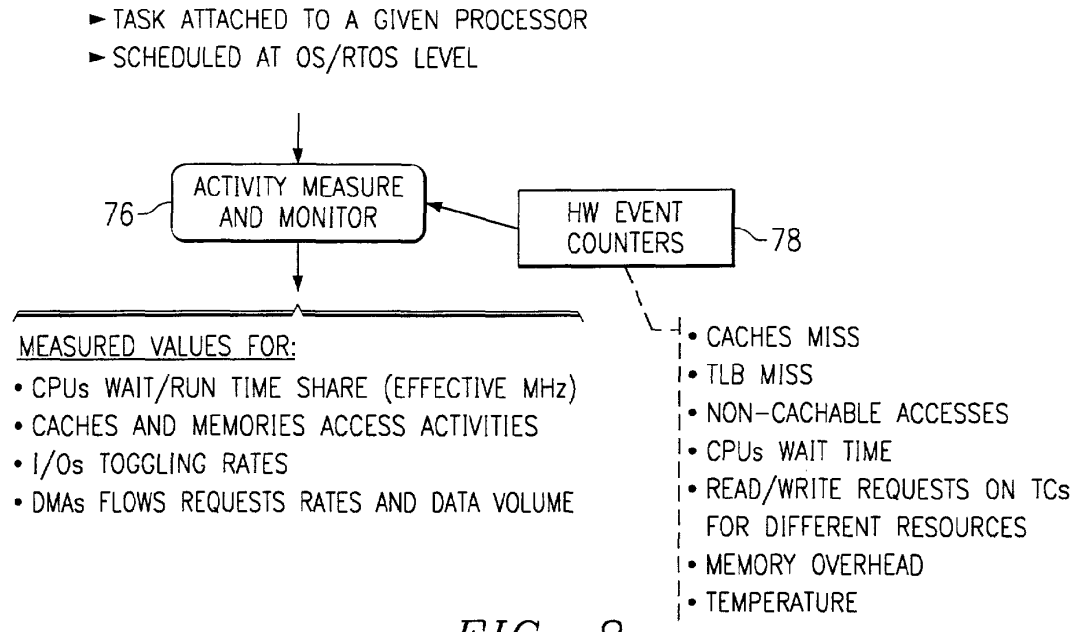

► TASK ATTACHED TO A GIVEN PROCESSOR
► SCHEDULED AT OS/RTOS LEVEL
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78
MEASURED VALUES FOR:
• CPUs WAIT/RUN TIME SHARE (EFFECTIVE MHz)
• CACHES AND MEMORIES ACCESS ACTIVITIES
• I/Os TOGGLING RATES
• DMAs FLOWS REQUESTS RATES AND DATA VOLUME
• CACHES MISS
• TLB MISS
• NON-CACHABLE ACCESSES
• CPUs WAIT TIME
• READ/WRITE REQUESTS ON TCs FOR DIFFERENT RESOURCES
• MEMORY OVERHEAD
• TEMPERATURE

FIG. 8

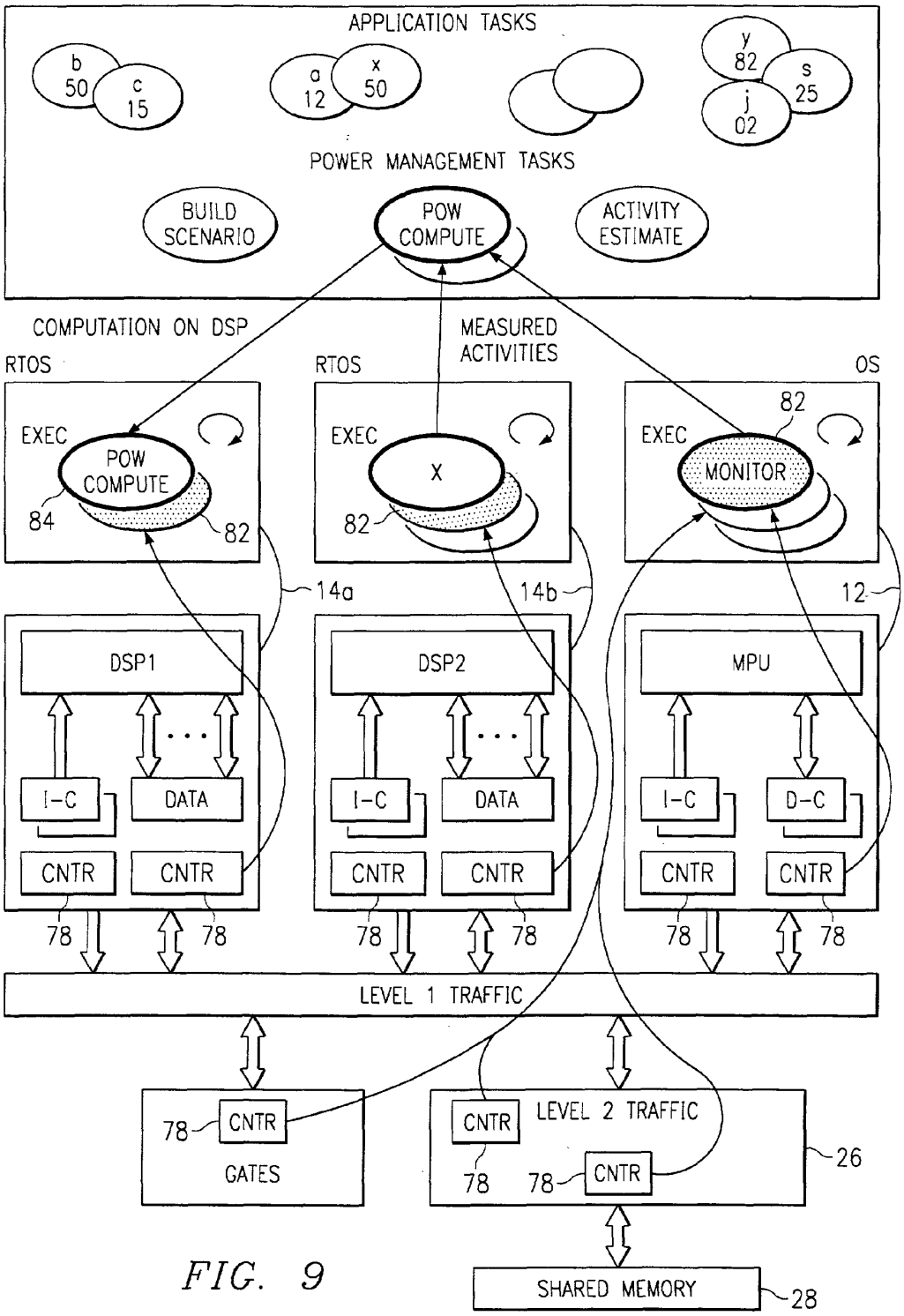

APPLICATION TASKS
b
50
c
15
a
12
x
50
y
82
s
25
j
02
POWER MANAGEMENT TASKS
BUILD SCENARIO
POW COMPUTE
ACTIVITY ESTIMATE
COMPUTATION ON DSP
MEASURED ACTIVITIES
RTOS
RTOS
OS
EXEC
POW COMPUTE
84
82
EXEC
X
82
EXEC
82
MONITOR
14a
14b
12
DSP1
DSP2
MPU
I-C
DATA
I-C
DATA
I-C
D-C
CNTR
CNTR
CNTR
CNTR
CNTR
CNTR
78
78
78
78
78
78
LEVEL 1 TRAFFIC
78
CNTR
GATES
CNTR
LEVEL 2 TRAFFIC
78
78
CNTR
26
SHARED MEMORY
28

FIG. 9

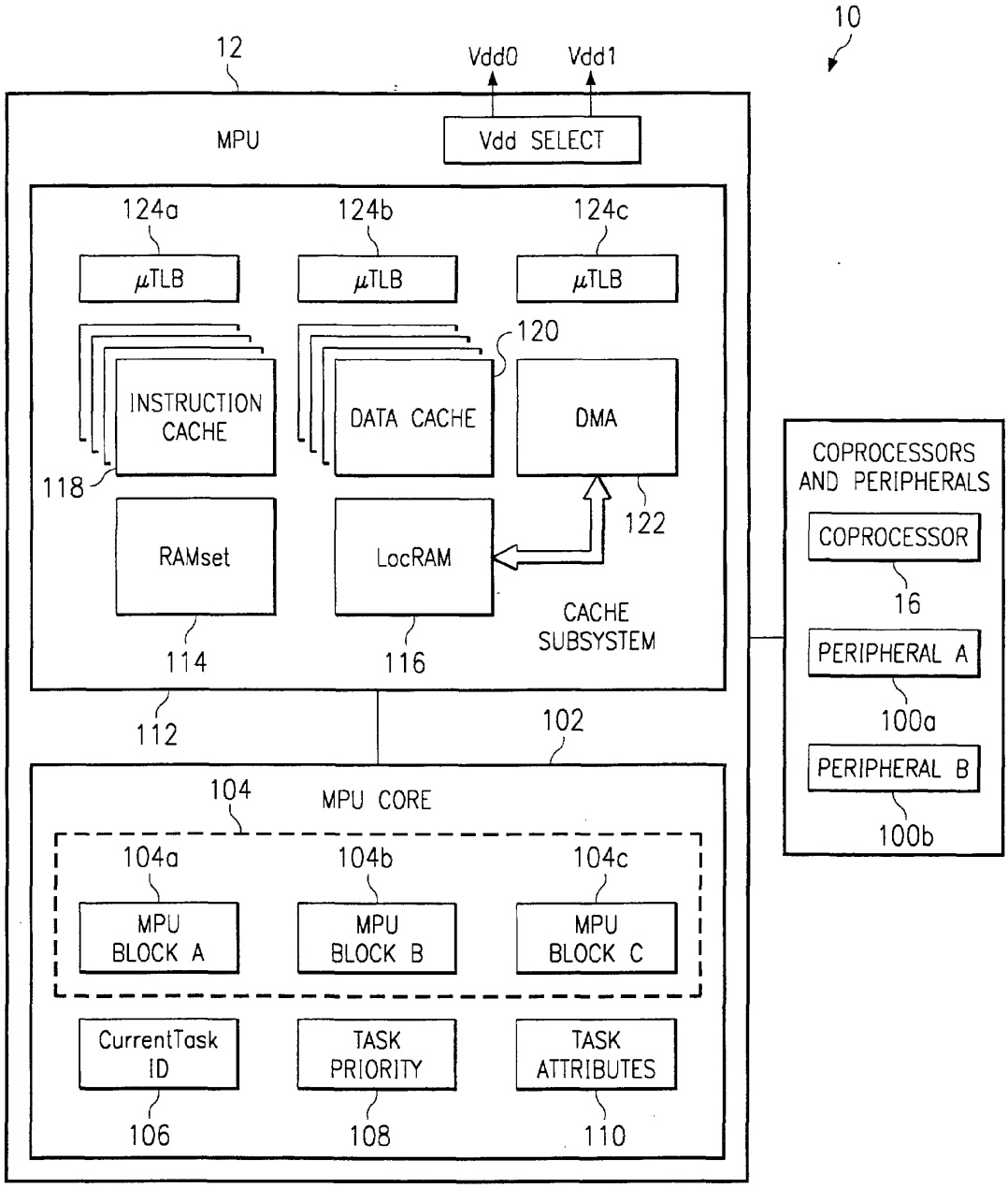

10
12
Vdd0
Vdd1
MPU
Vdd SELECT
124a
124b
124c
μTLB
μTLB
μTLB
120
INSTRUCTION CACHE
DATA CACHE
DMA
118
122
RAMset
LocRAM
CACHE SUBSYSTEM
114
116
112
102
104
MPU CORE
104a
104b
104c
MPU BLOCK A
MPU BLOCK B
MPU BLOCK C
CurrentTask ID
TASK PRIORITY
TASK ATTRIBUTES
106
108
110
COPROCESSORS AND PERIPHERALS
COPROCESSOR
16
PERIPHERAL A
100a
PERIPHERAL B
100b

FIG. 10

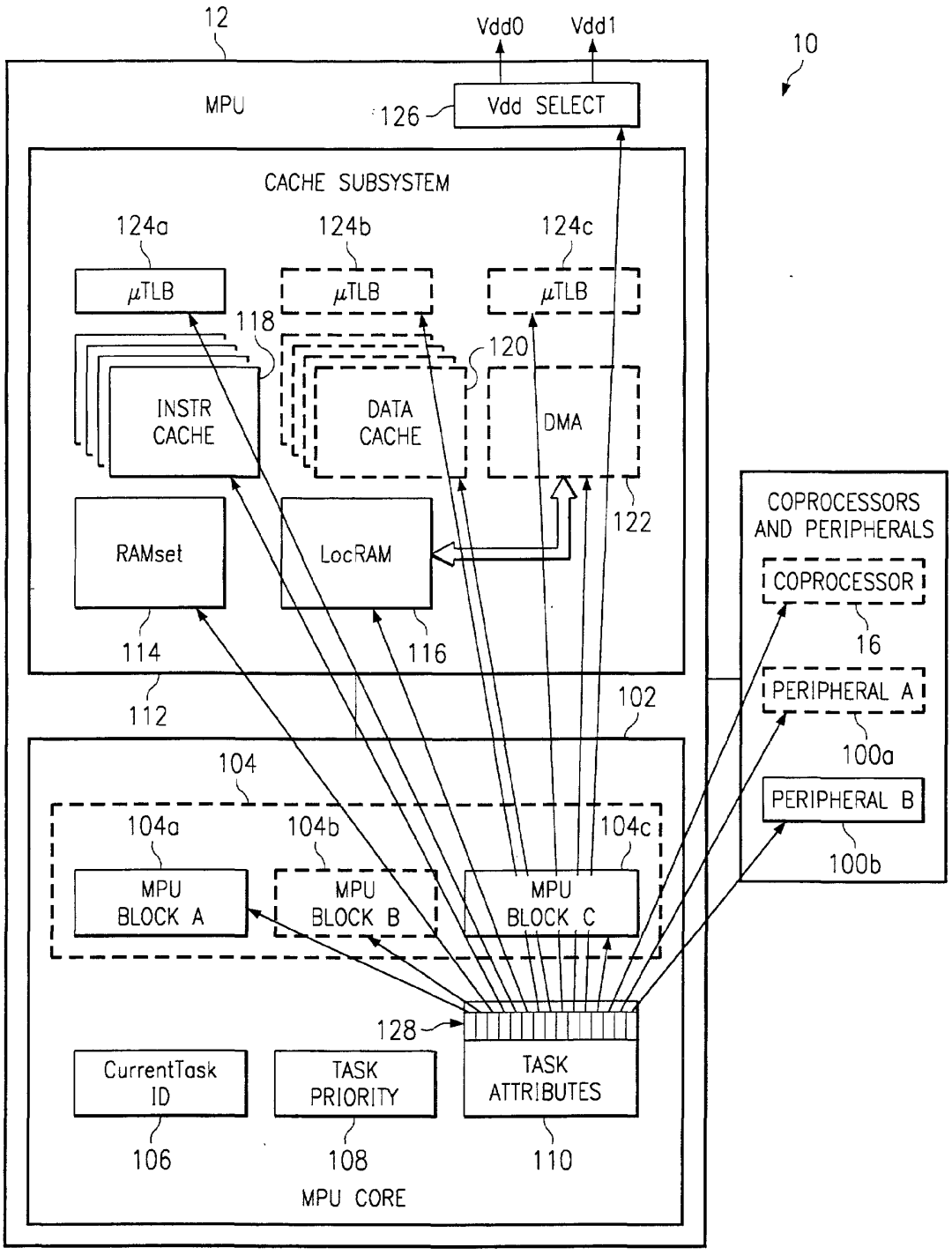

12
Vdd0
Vdd1
10
MPU
126
Vdd SELECT
CACHE SUBSYSTEM
124a
124b
124c
μTLB
μTLB
μTLB
118
120
INSTR CACHE
DATA CACHE
DMA
122
RAMset
LocRAM
114
116
112
102
104
104a
104b
104c
MPU BLOCK A
MPU BLOCK B
MPU BLOCK C
128
CurrentTask ID
TASK PRIORITY
TASK ATTRIBUTES
106
108
110
MPU CORE
COPROCESSORS AND PERIPHERALS
COPROCESSOR
16
PERIPHERAL A
100a
PERIPHERAL B
100b

FIG. 11

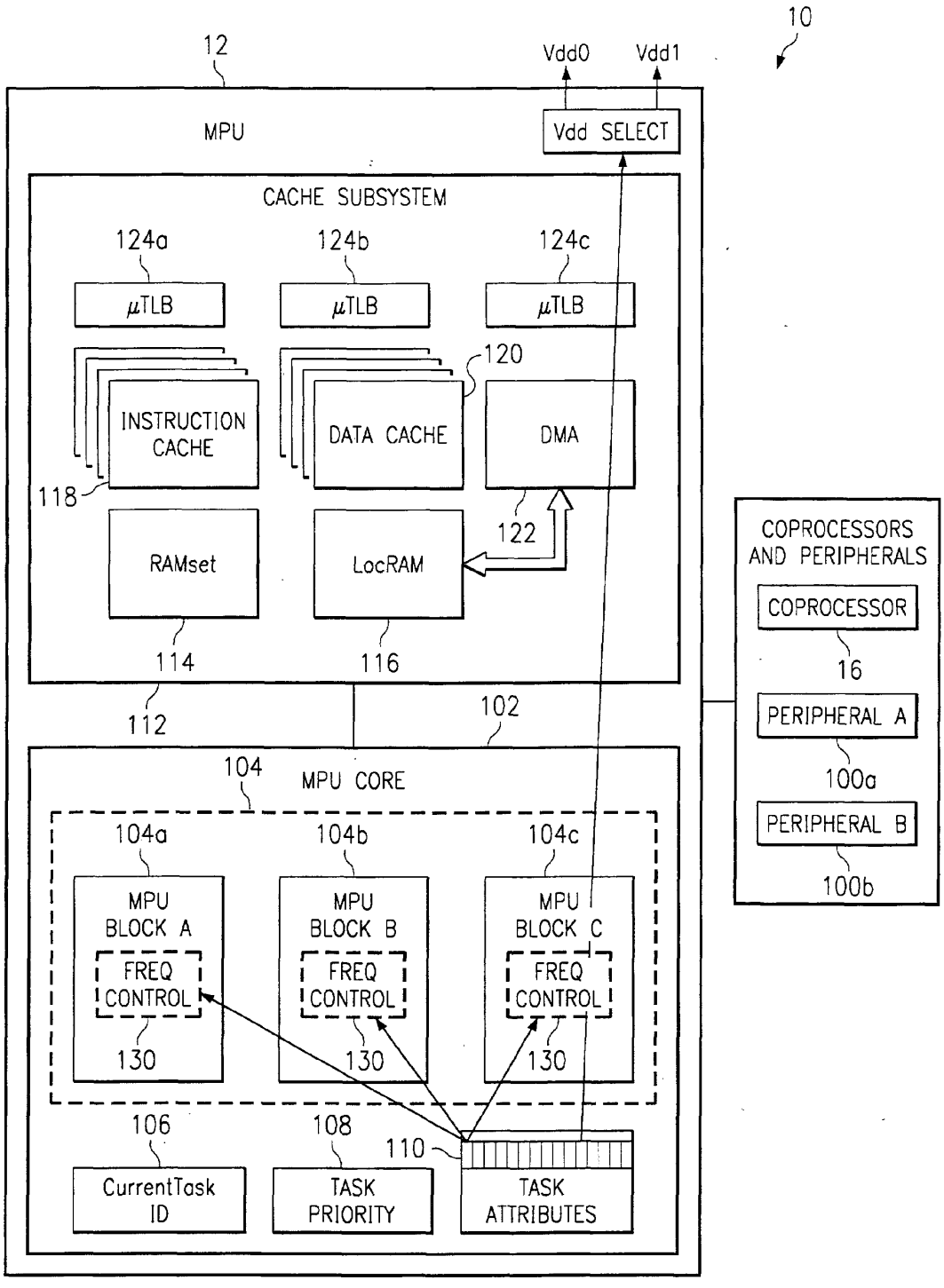

10
12
Vdd0
Vdd1
MPU
Vdd SELECT
CACHE SUBSYSTEM
124a
124b
124c
μTLB
μTLB
μTLB
120
INSTRUCTION CACHE
DATA CACHE
DMA
118
122
RAMset
LocRAM
114
116
112
102
104
MPU CORE
104a
104b
104c
MPU BLOCK A
MPU BLOCK B
MPU BLOCK C
FREQ CONTROL
FREQ CONTROL
FREQ CONTROL
130
130
130
106
108
110
CurrentTask ID
TASK PRIORITY
TASK ATTRIBUTES
COPROCESSORS AND PERIPHERALS
COPROCESSOR
16
PERIPHERAL A
100a
PERIPHERAL B
100b

FIG. 12

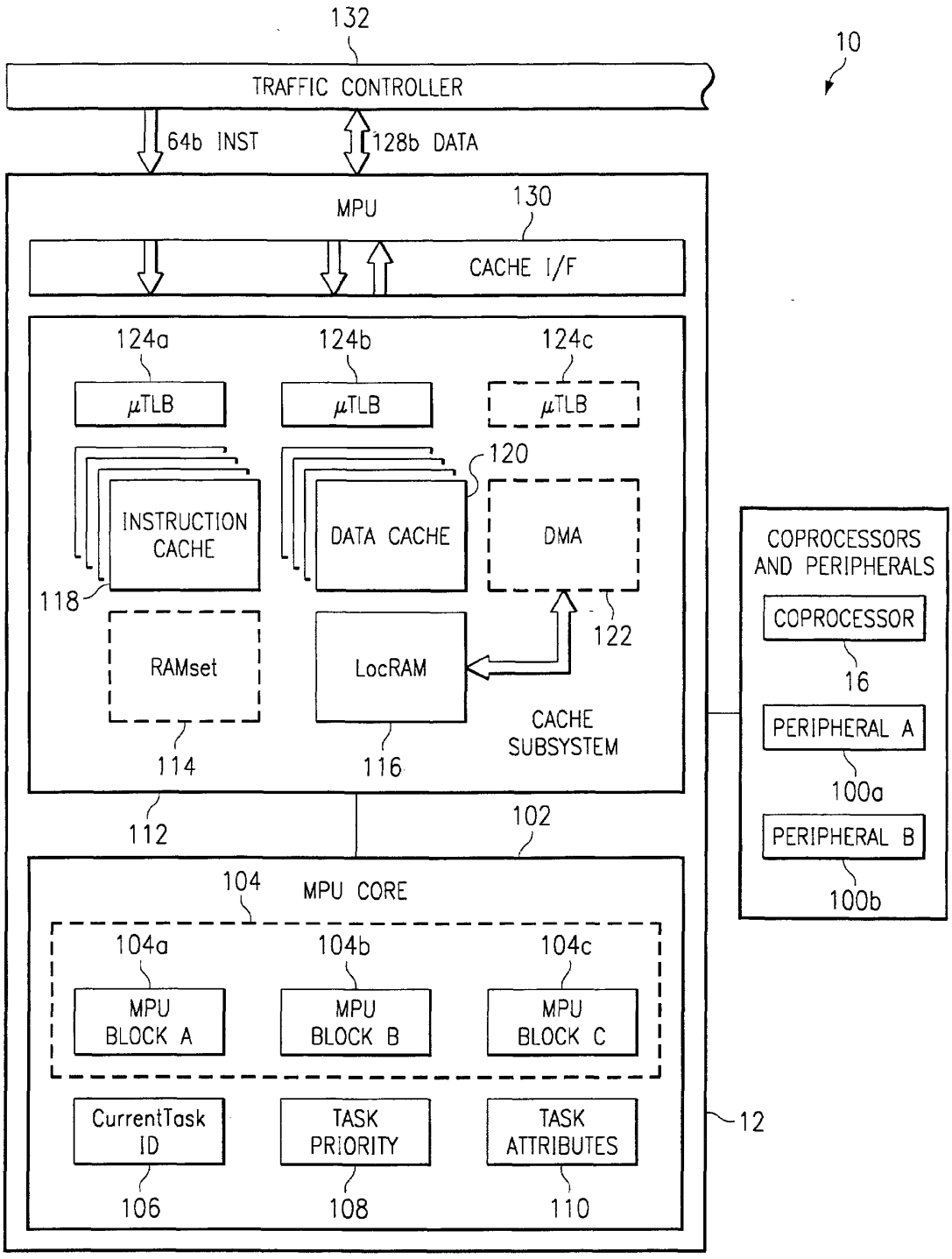

132
TRAFFIC CONTROLLER
10
64b INST
128b DATA
MPU
130
CACHE I/F
124a
124b
124c
μTLB
μTLB
μTLB
120
INSTRUCTION CACHE
DATA CACHE
DMA
118
RAMset
LocRAM
122
CACHE SUBSYSTEM
114
116
112
102
104
MPU CORE
104a
104b
104c
MPU BLOCK A
MPU BLOCK B
MPU BLOCK C
CurrentTask ID
TASK PRIORITY
TASK ATTRIBUTES
106
108
110
12
COPROCESSORS AND PERIPHERALS
COPROCESSOR
16
PERIPHERAL A
100a
PERIPHERAL B
100b

FIG. 13a

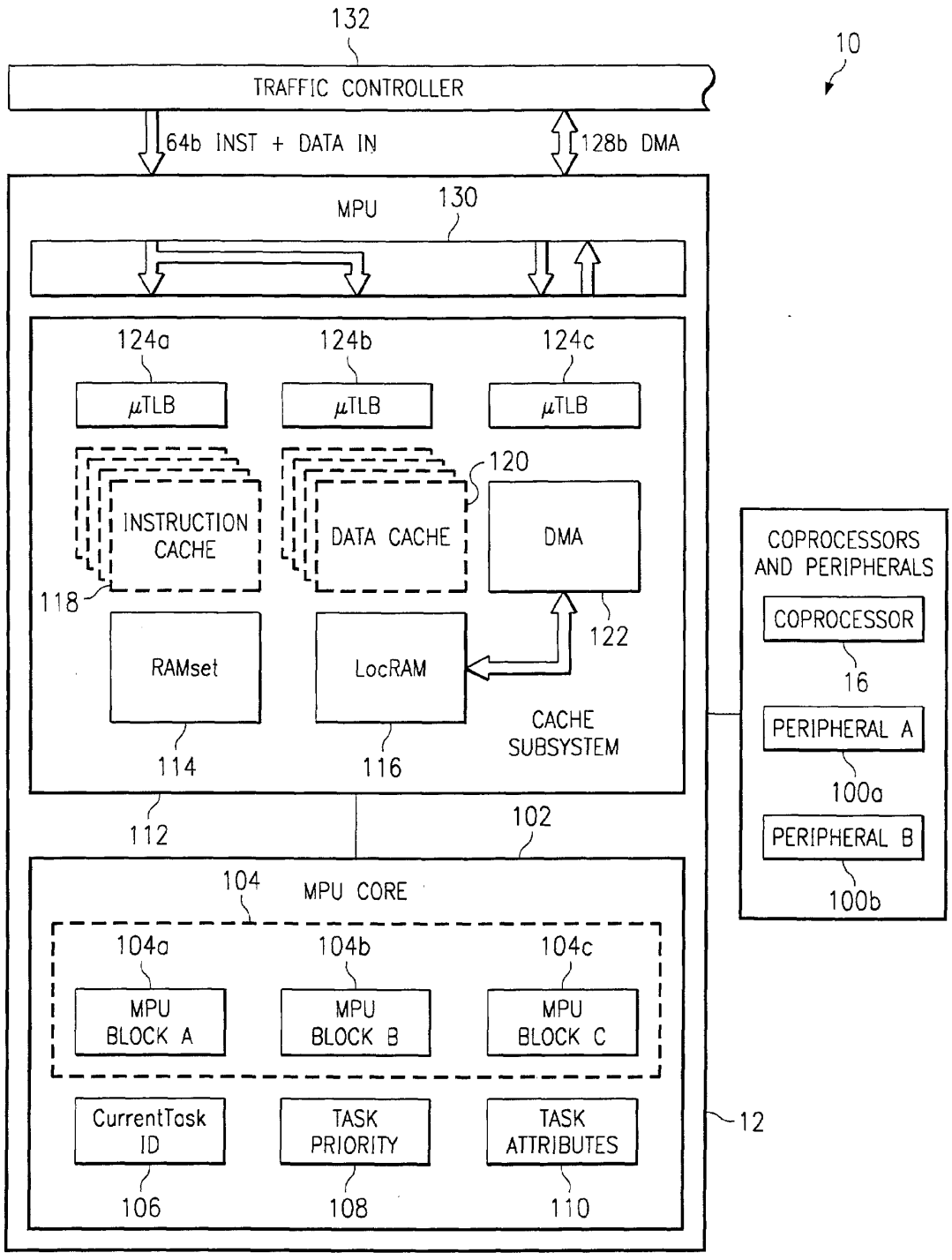

132
TRAFFIC CONTROLLER
10
64b INST + DATA IN
128b DMA
MPU
130
124a
124b
124c
μTLB
μTLB
μTLB
120
INSTRUCTION CACHE
DATA CACHE
DMA
118
122
RAMset
LocRAM
CACHE SUBSYSTEM
114
116
112
102
104
MPU CORE
104a
104b
104c
MPU BLOCK A
MPU BLOCK B
MPU BLOCK C
CurrentTask ID
TASK PRIORITY
TASK ATTRIBUTES
106
108
110
12
COPROCESSORS AND PERIPHERALS
COPROCESSOR
16
PERIPHERAL A
100a
PERIPHERAL B
100b

FIG. 13b

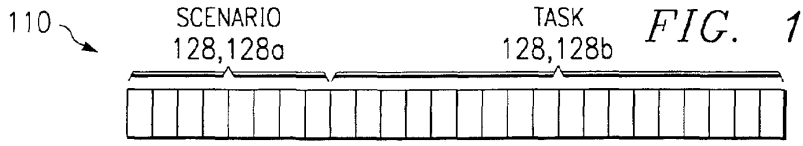


FIG. 14

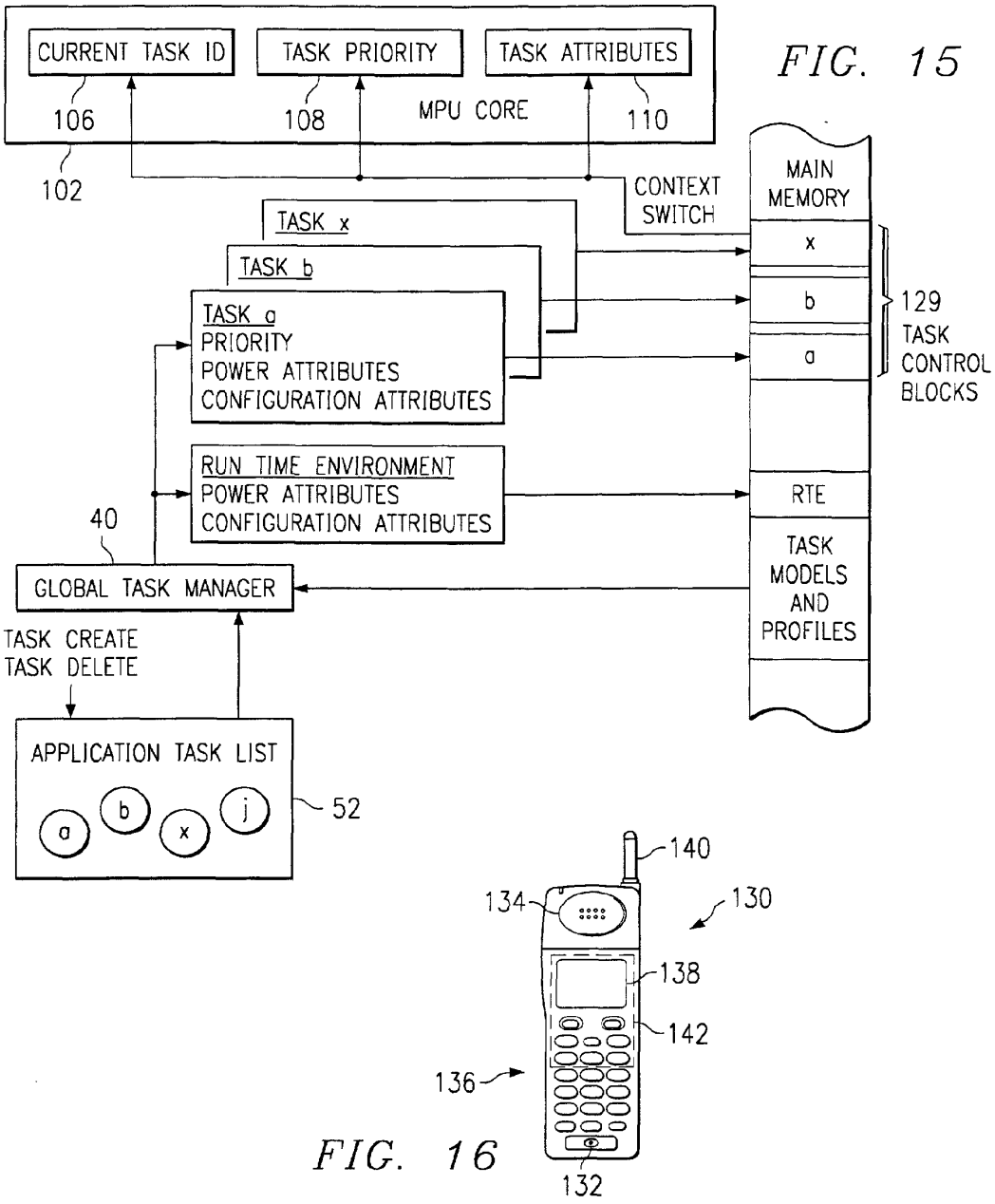


FIG. 15

FIG. 16

Electronic Acknowledgement Receipt	
EFS ID:	35015909
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Do Hyung Kim/Julie McLeod
Filer Authorized By:	Do Hyung Kim
Attorney Docket Number:	01181-US-REI
Receipt Date:	31-JAN-2019
Filing Date:	24-JUN-2016
Time Stamp:	11:04:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	IDS_Submission.pdf	1034477 8b08ae6d265536dfac6920c09296c5bbb44cd988	no	4

Warnings:

Information:					
2	Foreign Reference	EP1182548A2.pdf	519390 b761f829e3b7dde346634990b97db45d92e5e936	no	24
Warnings:					
Information:					
3	Non Patent Literature	CMOS_Power_Consumption_Texas_Instruments.pdf	1158745 7e3baa55ca93e135d05830f634ad719b8f3473c5	no	16
Warnings:					
Information:					
		Total Files Size (in bytes):	2712612		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/192,486

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	2160
TOTAL CLAIMS (37 CFR 1.16(i))	61 minus 20 =	* 41			OR	x 80 =	3280
INDEPENDENT CLAIMS (37 CFR 1.16(h))	6 minus 3 =	* 3				x 420 =	1260
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	7580

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/192,486	06/24/2016	Barry Alan Hoberman	01181-US-REI

CONFIRMATION NO. 6310

68256
Conversant Intellectual Property Management Inc.
5601 Granite Parkway
Suite 1300
Plano, TX 75024

INFORMAL NOTICE

OC000000087460663

Date Mailed: 11/28/2016

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cmhaywood/

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/192,486	06/24/2016	2851	7720	01181-US-REI	61	6

CONFIRMATION NO. 6310

UPDATED FILING RECEIPT

68256
Conversant Intellectual Property Management Inc.
5601 Granite Parkway
Suite 1300
Plano, TX 75024

OC000000087480662

Date Mailed: 11/28/2016

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Barry Alan Hoberman, Cupertino, CA;
Daniel L. Hillman, San Jose, CA;
Jon Shiell, San Jose, CA;

Applicant(s)

Conversant Intellectual Property Management Inc., Ottawa, CANADA, Assignee (with 37 CFR 1.172 Interest);

Assignment For Published Patent Application

Conversant Intellectual Property Management Inc., Ottawa, CANADA

Power of Attorney: The patent practitioners associated with Customer Number 68256

Domestic Priority data as claimed by applicant

This application is a REI of 13/473,129 05/16/2012 PAT 8762923
which is a DIV of 13/164,362 06/20/2011 PAT 8782590
which is a CON of 12/332,529 12/11/2008 PAT 7996811
which is a CON of 12/176,645 07/21/2008 PAT 7945885
which is a CON of 11/336,097 01/20/2006 PAT 7415680
which is a CON of 10/840,893 05/07/2004 PAT 7051306
which claims benefit of 60/468,742 05/07/2003

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 07/11/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/192,486**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Preliminary Class

716

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

ATTORNEY DOCKET No.
01181-US-REI

PATENT APPLICATION
15/192,486

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	HOBERMAN, Barry A.
Serial No.:	15/192,486
Filing Date:	June 24, 2016
Group Art Unit:	2851
Examiner:	Unknown
Confirmation No.:	6310
Title:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Mail Stop – MISSING PARTS
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia
22314-1450
U.S.A.

Dear Sir:

Reply to Notice of Incomplete Reply (Reissue)

In response to the Notice of Incomplete Reply dated October 11, 2016, Applicants submit the following documents:

1. Executed Substitute Statement in Lieu of an Oath or Declaration for inventors:
   a) Hillman
   b) Hoberman
   c) Shiell
2. Executed Consent of Assignee
3. Executed Assignee Declaration
4. 37 373(c) Statement

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 504154.

Respectfully submitted,

/Do Hyung Kim/

Dated: November 15, 2016

Do Hyung Kim
Reg. No. 66487

Conversant IP Management Corp
5601 Granite Parkway, Suite 1300
Plano, Texas 75024
Phone: 214-494-4814 Fax: 214-436-4683
Email: kimd@core-wireless.com

Electronic Patent Application Fee Transmittal

Application Number:	15192486
Filing Date:	24-Jun-2016
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Filer:	Do Hyung Kim/Julie McLeod
Attorney Docket Number:	01181-US-REI

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
			Total in USD ($)	**600**

Electronic Acknowledgement Receipt	
EFS ID:	27521307
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Do Hyung Kim/Julie McLeod
Filer Authorized By:	Do Hyung Kim
Attorney Docket Number:	01181-US-REI
Receipt Date:	15-NOV-2016
Filing Date:	24-JUN-2016
Time Stamp:	17:45:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$600
RAM confirmation Number	111616INTEFSW00005049504154
Deposit Account	504154
Authorized User	Julie McLeod
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	2016_11_15_Extension.pdf	187680 413a4df17c4c8960befe6be65a91512973fff5e8	no	2
Warnings:					
Information:					
2	Assignee showing of ownership per 37 CFR 3.73	2016_10_21_373C_Filed.pdf	123969 37a0e4781849fc29f4f51262a53d24f5fb8e6dd0	no	4
Warnings:					
Information:					
3	Consent of Assignee accompanying the declaration	Applicant_Consent.pdf	92688 25ab5a194021822f7c8c59976d803f0fd632260a	no	2
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
4	Reissue dec filed in accordance with MPEP 1414	Assignee_Declaration.pdf	129195 cf213d2e5603dc52d8a3dc6c3c01cc5b3a74cc2c	no	3
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
5	Oath or Declaration filed	Substitute_Statement_HILLMAN.pdf	154902 59c1cd546050653d29e69970f957c9c8b854ca1c	no	4
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					

6	Oath or Declaration filed	Substitute_Statement_Hoberman.pdf	156102 1d33c79b111e8a3a5edce8f056d2b029a6263c6e	no	4
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
7	Oath or Declaration filed	Substitute_Statement_SHIELL.pdf	154132 f9f2f63e095f5d077cd3ad2b7b14db7fd8d8864f	no	4
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
8	Applicant Response to Pre-Exam Formalities Notice	2016_11_15_Response.pdf	20069 e7775ab7ea82465d3b50a0fb8df41e91164585cb	no	1
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	31058 e69709cd92f8ed338dae2437839ca9fbd131e2c1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1049795		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/22 (03-13)
Approved for use through 3/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): 01181-US-REI

Application Number: 15/192,486

Filed: 06/24/2016

For: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Art Unit: 2851

Examiner: Unknown

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$
☑ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$ 600.00
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☐ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number _____.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 66487.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Do Hyung Kim/ — Signature

November 15, 2016 — Date

Do Hyung Kim — Typed or printed name

214-494-4814 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Conversant Intellectual Property Management Inc.

Application No./Patent No.: 15/192,486 Filed/Issue Date: 06/24/2016

Titled: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Conversant Intellectual Property Management Inc., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Barry Alan, Hoberman; Daniel L. Hillman and Jon Shiell To: Virtual Silicon Technology, Inc.

The document was recorded in the United States Patent and Trademark Office at Reel 028269, Frame 0957, or for which a copy thereof is attached.

2. From: Virtual Silicon Technology, Inc. To: Mosaid Delaware, Inc.

The document was recorded in the United States Patent and Trademark Office at Reel 028270, Frame 0368, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: Mosaid Delaware Inc. To: Mosaid Technologies Corporation

The document was recorded in the United States Patent and Trademark Office at
Reel 028275, Frame 0794, or for which a copy thereof is attached.

4. From: Mosaid Technologies Corporation To: Mosaid Technologies Incorporation

The document was recorded in the United States Patent and Trademark Office at
Reel 028271, Frame 0856, or for which a copy thereof is attached.

5. From: Mosaid Technologies Incorporated To: Mosaid Technologies Incorporated..

The document was recorded in the United States Patent and Trademark Office at
Reel 028275, Frame 0471, or for which a copy thereof is attached.

6. From: Mosaid Technologies Incorporated To: Conversant Intellectual Property Management Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 032439, Frame 0638, or for which a copy thereof is attached.

☑ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Do Hyung Kim/	November 15, 2016
Signature	Date
Do Hyung Kim	66487
Printed or Typed Name	Title or Registration Number

7. From: **Conversant Intellectual Property Management Inc.** To: **Conversant Intellectual Property Management Inc.** The document was recorded in the United States Patent and Trademark Office at Reel **033678**, Frame **0096** or for which a copy thereof is attached.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/53 (09-12)
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REISSUE APPLICATION: CONSENT OF ASSIGNEE; STATEMENT OF NON-ASSIGNMENT	Docket Number (Optional) 01181-US-REI

This is part of the application for a reissue patent based on the original patent identified below.

Name of Patentee(s)

Conversant Intellectual Property Management Inc.

Patent Number	Date Patent Issued
8,762,923	June 24, 2014

Title of Invention

POWER MANAGERS FOR AN INTEGRATED CIRCUIT

1. ☑ Filed herein is a statement under 37 CFR 3.73(c). (Form PTO/AIA/96)

2. ☐ Ownership of the patent is in the inventor(s), and no assignment of the patent is in effect.

One of boxes 1 or 2 above must be checked. If multiple assignees, complete this form for each assignee. If box 2 is checked, skip the next entry and go directly to "Name of Assignee."

The written consent of all assignees and inventors owning an undivided interest in the original patent is included in this application for reissue.

The assignee(s) owning an undivided interest in said original patent is/are Conversant IP Management Inc., and the assignee(s) consents to the accompanying application for reissue.

Name of assignee/inventor (if not assigned)

Signature	Date
	Oct 21-16

Typed or printed name and title of person signing for assignee (if assigned)

Scott Burt - SVP, Chief Intellectual Property Officer, and General Counsel, Patent Licensing

This collection of information is required by 37 CFR 1.172. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: REIS.DECL
Document Description: Reissue Declaration Filed In Accordance With MPEP 1414

PTO/AIA/06 (05-12)
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REISSUE APPLICATION DECLARATION BY THE ASSIGNEE	Docket Number (optional) 01181-US-REI

I hereby declare that:

The residence and mailing address of the inventor or joint inventors are stated below.

I am authorized to act on behalf of the following assignee: Conversant Intellectual Property Management Inc.

The entire title to the patent identified below is vested in said assignee.

Inventor HOBERMAN, Barry A.

Residence: City	State	Country
Cupertino	CA	USA

Mailing Address
10290 Palo Vista Road

City	State	Zip	Country
Cupertino	CA	95014	USA

☑ Additional inventors are named on separately numbered sheets attached hereto.

Patent Number 8,762,923	Date of Patent Issued 06/24/2014

I believe said inventor(s) to be the original inventor or original joint inventors of the subject matter which is described and claimed in said patent, for which a reissue patent is sought on the invention titled:

POWER MANAGERS FOR AN INTEGRATED CIRCUIT

the specification of which

☐ is attached hereto.

☑ was filed on June 24, 2016 as reissue application number 15/192,486.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below.
(Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

This collection of information is required by 37 CFR 1.175. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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REISSUE APPLICATION DECLARATION BY THE ASSIGNEE	Docket Number (Optional)

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified and the box below must be checked:

Applicants claimed less than they were entitled to. The original claims 1-39 recite subject matter related to power management systems for a integrated circuits using power islands, but do not recite monitoring temperatures of the plurality of power islands as newly added claims 30-41 do, and which Applicants are entitled to.

[Attach additional sheets, if needed.]

☐ **The application for the original patent was filed under 37 CFR 1.46 by the assignee of the entire interest.**

I hereby appoint:

☑ Practitioners associated with Customer Number: 68256

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 68256

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Signature	Date (Optional)
Full name of person signing (given name, family name) Scott Burt	
Address of Assignee 515 Leggett Drive, Suite 704, Ottawa, Ontario K2K 3G4	

Privacy Act Statement

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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

This statement is directed to:

☐ The attached application,

OR

☒ was filed on June 24, 2016 as reissue application number 15/192,486

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Daniel L HILLMAN

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
San Jose	CA	US

Mailing Address (except for a deceased or legally incapacitated inventor):

6607 Winterset Way

City	State	Zip	Country
San Jose	CA	95120	US

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Relationship to the inventor to whom this substitute statement applies:

☐ Legal Representative (for deceased or legally incapacitated inventor only),

☒ Assignee, or

☐ Joint Inventor.

Circumstances permitting execution of this substitute statement:

☐ Inventor is deceased,

☐ Inventor is under legal incapacity,

☒ Inventor cannot be found or reached after diligent effort, or

☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.175.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

If there are joint inventors, please check the appropriate box below:

☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below.
(Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

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WARNING:

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PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Scott Burt

Date (Optional):

Signature:

APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer.

Applicant Name: Conversant Intellectual Property Management Inc.

Title of Person Executing This Substitute Statement: SVP, Chief Intellectual Property Officer, and General Counsel, Patent Licensing

The signer, whose title is supplied above, is authorized to act on behalf of the applicant.

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Residence of the signer (unless provided in an application data sheet, PTO/SB/14 or equivalent):

City	State	County
Ottawa	Ontario	CA

Mailing Address of the signer (unless provided in an application data sheet, PTO/SB/14 or equivalent):

515 Legget Drive, Suite 704

City	State	Zip	Country
Ottawa	Ontario	K2K 3G4	CA

Note: Use an additional PTO/AIA/07 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

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Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

This statement is directed to:

☐ The attached application,

OR

☒ was filed on June 24, 2016 as reissue application number 15/192,486

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Barry Alan HOBERMAN

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
Cupertino	CA	US

Mailing Address (except for a deceased or legally incapacitated inventor):

10290 Palo Vista Road

City	State	Zip	Country
Cupertino	CA	95014	US

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

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Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Scott Burt

Date (Optional):

Signature:

APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer.

Applicant Name: Conversant Intellectual Property Management Inc.

Title of Person Executing This Substitute Statement: SVP, Chief Intellectual Property Officer, and General Counsel, Patent Licensing

The signer, whose title is supplied above, is authorized to act on behalf of the applicant.

PTO/AIA/07 (09-13)
Approved for use through 01/31/2014. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Residence of the signer (unless provided in an application data sheet, PTO/SB/14 or equivalent):

City	State	County
Ottawa	Ontario	CA

Mailing Address of the signer (unless provided in an application data sheet, PTO/SB/14 or equivalent):

515 Legget Drive, Suite 704

City	State	Zip	Country
Ottawa	Ontario	K2K 3G4	CA

Note: Use an additional PTO/AIA/07 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: REIS.DECL
Document Description: Reissue Declaration Filed In Accordance With MPEP 1414

PTO/AIA/07 (09-13)
Approved for use through 04/30/2017. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

This statement is directed to:

☐ The attached application,

OR

☒ was filed on June 24, 2016 as reissue application number 15/192,486.

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Jon SHIELL

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
San Jose	CA	US

Mailing Address (except for a deceased or legally incapacitated inventor):

801 Seabury Drive

City	State	Zip	Country
San Jose	CA	95136	US

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Relationship to the inventor to whom this substitute statement applies:

☐ Legal Representative (for deceased or legally incapacitated inventor only),

☒ Assignee, or

☐ Joint Inventor.

Circumstances permitting execution of this substitute statement:

☐ Inventor is deceased,

☐ Inventor is under legal incapacity,

☒ Inventor cannot be found or reached after diligent effort, or

☐ Inventor has refused to execute the oath or declaration under 37 CFR 1.175.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/07 (09-13)
Approved for use through 01/31/2014. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR REISSUE PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

If there are joint inventors, please check the appropriate box below:

☒ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below.
(Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Applicants claimed less than they were entitled to. The original claims 1-39 recite subject matter related to power management systems for a integrated circuits using power islands, but do not recite monitoring temperatures of the plurality of power islands as newly added claims 30-41 do, and which Applicants are entitled to.

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PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Scott Burt

Date (Optional):

Signature:

APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer.

Applicant Name: Conversant Intellectual Property Management Inc.

Title of Person Executing This Substitute Statement: SVP, Chief Intellectual Property Officer, and General Counsel, Patent Licensing

The signer, whose title is supplied above, is authorized to act on behalf of the applicant.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/192,486

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	2160
TOTAL CLAIMS (37 CFR 1.16(i))	61 minus 20 =	* 41			OR	x 80 =	3280
INDEPENDENT CLAIMS (37 CFR 1.16(h))	6 minus 3 =	* 3				x 420 =	1260
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	7580

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/192,486	06/24/2016	Barry Alan Hoberman	01181-US-REI

CONFIRMATION NO. 6310

68256
Conversant Intellectual Property Management Inc.
5601 Granite Parkway
Suite 1300
Plano, TX 75024

FORMALITIES LETTER

OC000000086373683

Date Mailed: 10/11/2016

NOTICE OF INCOMPLETE REPLY (REISSUE)

Filing Date Granted

The U.S. Patent and Trademark Office has received your reply on 09/21/2016 to the Notice to File Missing Parts (Notice) mailed 07/21/2016 and it has been entered into the reissue application. The reply, however, does not include the following items required in the Notice.

The period of reply remains as set forth in the Notice. You may, however, obtain EXTENSIONS OF TIME under the provisions of 37 CFR 1.136 (a) accompanied by the appropriate fee (37 CFR 1.17(a)).

A complete reply must be timely filed to prevent ABANDONMENT of the above-identified application.

The required items noted below SHOULD be filed along with any items required above. The filing date of this reissue application will be the date of receipt of the items required above.

- The inventor's oath or declaration has not been submitted.
- Consent of assignee is missing. 37 CFR 1.172 requires that a reissue oath/declaration be accompanied by the written consent of all assignees.
- Assignee's statement under 37 CFR 3.73(c) establishing ownership of the patent is missing. 37 CFR 1.172 requires that all assignees consenting to the reissue application establish their ownership interest in the patent by filing in the reissue application a statement in accordance with 37 CFR 3.73(c).
- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Barry Alan Hoberman
  Daniel L. Hillman
  Jon Shiell

  An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 (and 37 CFR 1.175) executed by or with respect to each inventor is required. For a reissue application, the inventor's oath or declaration must be submitted prior to examination and cannot be postponed. See 37 CFR 1.175(e). An assignee of the entire interest can execute the oath or declaration if: (1) the application does not seek to enlarge the scope of the claims of the original patent; or (2) the application for the original patent was filed under 37 CFR 1.46 by the assignee of the entire interest. A substitute statement under 37 CFR 1.64 in lieu of an oath or declaration may be submitted in the circumstances provided for in 35 U.S.C. 115(d) and 37 CFR 1.64.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's

oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/cmhaywood/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	HOBERMAN, Barry A.
Serial No.:	15/192,486
Filing Date:	June 24, 2016
Group Art Unit:	2851
Examiner:	Unknown
Confirmation No.:	6310
Title:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Mail Stop – MISSING PARTS
Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia
22314-1450
U.S.A.

Dear Sir:

Reply to Notice of Missing Parts

In response to the Notice to File Missing Parts dated July 21, 2016, for which a response is due by the due date of September 21, 2016 and based on the preliminary amendment submitted under separate cover, Applicant submits the following outstanding fees:

- **Basic Filing Fee: $280**
- **Search Fee: $600**
- **Examination Fee: $2160**
- **Late Surcharge Fee: $140**
- **3 Independent Claim: $1260**
- **41 Claims over 20: $3280**

The required fees totalling $**7720.00** are being submitted electronically.

Based on the preliminary amendment filed under separate cover, the fees have been reduced to reflect the cancelled claims.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 504154.

Respectfully submitted,

/Do Hyung Kim/

Dated: September 21,2016

Do Hyung Kim
Reg. No. 66487

Conversant IP Management Corp
5601 Granite Parkway, Suite 1300
Plano, Texas 75024
Phone: 214-494-4867 Fax: 214-436-4683
Email: kim@core-wireless.com

Electronic Patent Application Fee Transmittal

Application Number:	15192486
Filing Date:	24-Jun-2016
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Filer:	Do Hyung Kim/Julie McLeod
Attorney Docket Number:	01181-US-REI

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY REISSUE BASIC	1014	1	280	280
DESIGN AND UTILITY REISSUE BASIC	1114	1	600	600
DESIGN AND UTILITY REISSUE BASIC	1314	1	2160	2160
Pages:				
Claims:				
REISSUE CLAIMS IN EXCESS OF 20	1205	41	80	3280
INDEPENDENT CLAIMS REISSUE	1204	3	420	1260
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**7720**

Electronic Acknowledgement Receipt	
EFS ID:	26995383
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Do Hyung Kim/Julie McLeod
Filer Authorized By:	Do Hyung Kim
Attorney Docket Number:	01181-US-REI
Receipt Date:	21-SEP-2016
Filing Date:	24-JUN-2016
Time Stamp:	16:45:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$7720
RAM confirmation Number	092216INTEFSW00003975504154
Deposit Account	504154
Authorized User	Julie McLeod
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016_09_21_Preliminary_Amendment_Filed.pdf	57132 7548e0f7487fa3ccefdecc96bef888bf1cc74249	yes	15
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Preliminary Amendment		1	1	
	Preliminary Amendment		2	14	
	Preliminary Amendment		15	15	
Warnings:					
Information:					
2	Applicant Response to Pre-Exam Formalities Notice	2016_09_21_Missing_Parts_Response.pdf	23212 17ef9fd00d7ac179e8d4811739ff34c2fcf4193b	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	40286 309eb0455dd90eaba5c081b80dcc9b7e7f3d4e4f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	120630		

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	HOBERMAN, Barry A.
Serial No.:	15/192,486
Filing Date:	June 24, 2016
Group Art Unit:	2851
Examiner:	Unknown
Confirmation No.:	6310
Title:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Mail Stop - AMENDMENT
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

SECOND PRELIMINARY AMENDMENT

Prior to examination on the merits, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 15 of this paper.

Amendments to Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) changing a source voltage of the first power island;

ii) after the changing, waiting for the source voltage of the first power island to settle down; and

iii) after the waiting, changing a clock frequency of the first power island.

2. (Original) The system of claim 1 wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency.

3. (Original) The system of claim 2 wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

4. (Original) The system of claim 1 wherein the first power manager is further configured to communicate the request to the second power manager.

5. (Original) The system of claim 1 wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

6. (Original) The system of claim 1 wherein the source voltage of the first power island is controlled by a smart power unit.

7. (Original) The system of claim 1 wherein the source voltage of the first power island is provided by an external regulator.

8. (Original) The system of claim 1 wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

9. (Original) The system of claim 1 wherein the second power manager comprises firmware processable on the integrated circuit.

10. (Original) The system of claim 1 wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

11. (Original) The system of claim 10 wherein the power management software is embedded firmware in the integrated circuit.

12. (Original) The system of claim 1 wherein the first power manager is located outside the integrated circuit.

13. (Original) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

in a first power manager, managing ~~a~~the first power consumption based on needs and operation of the integrated circuit;

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

providing a source voltage to the first power island; and

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

changing the source voltage of the first power island;

after the changing, waiting for the source voltage of the first power island to settle down; and

after the waiting, changing a clock frequency of the clock.

14. (Original) The method of claim 13 wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency.

15. (Original) The method of claim 14 further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

16. (Original) The method of claim 13 wherein the request is communicated to the second power manager by the first power manager.

17. (Original) The method of claim 13 further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

18. (Original) The method of claim 13 wherein the source voltage of the first power island is controlled by a smart power unit.

19. (Original) The method of claim 13 further comprising providing external regulation for the source voltage of the first power island.

20. (Original) The method of claim 13 wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island.

21. (Original) The method of claim 13 further comprising, in a third power manager:

i) managing a third power consumption of the power consumptions, and the plurality of power islands including a second power island having an associated power consumption that is the third power consumption; and

ii) communicating with the first power manager.

22. (Original) The method of claim 21 wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers.

23. (Original) A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

24. (Original) The system of claim 23 wherein the second power manager is further configured to carry out the saving of the state of the first power island after the stopping.

25. (Original) The system of claim 23 wherein the first power manager is further configured to communicate the request to the second power manager.

26. (Original) The system of claim 23 further comprising a buffer for storing the state that is saved.

27. (Original) The system of claim 23 wherein the second power manager is further configured to respond to another request, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock of the first power island.

28. (Original) The system of claim 27 further comprising a buffer for storing the state that is saved, and the buffer being accessible during the restoring.

29. (Original) The system of claim 23 wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

30. (Original) The system of claim 23 wherein the second power manager comprises firmware processable on the integrated circuit.

31. (Original) The system of claim 23 wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

32. (Original) The system of claim 31 wherein the power management software is embedded firmware in the integrated circuit.

33. (Original) The system of claim 23 wherein the first power manager is located outside the integrated circuit.

34. (Original) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

in a first power manager, managing a first power consumption based on needs and operation of the integrated circuit;

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

35. (Original) The method of claim 34 wherein the saving of the state of the first power island is carried out after the stopping.

36. (Original) The method of claim 34 wherein the request is communicated to the second power manager by the first power manager.

37. (Original) The method of claim 34 wherein the state that is saved is stored in a buffer.

38. (Original) The method of claim 34 further comprising responding to another request that is received by the second power manager, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock.

39. (Original) The method of claim 38 wherein the state that is saved is stored in a buffer accessed during the restoring.

40. (New) A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to:

a) manage the first power consumption based on needs and operation of the integrated circuit;

b) determine power trade-offs between the power islands;

c) monitors the plurality of power islands if a temperature threshold has been exceeded; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) changing a source voltage; and

ii) changing a clock frequency of the first power island.

41. (New) The system of claim 39, wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency.

42. (New) The system of claim 41, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

43. (New) The system of claim 39, wherein the first power manager is further configured to communicate the request to the second power manager.

44. (New) The system of claim 39, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

45. (New) The system of claim 39, wherein the source voltage of the first power island is controlled by a smart power unit.

46. (New) The system of claim 39, wherein the source voltage of the first power island is provided by an external regulator.

47. (New) The system of claim 39, wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

48. (New) The system of claim 39, wherein the second power manager comprises firmware processable on the integrated circuit.

49. (New) The system of claim 39, wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

50. (New) The system of claim 39, wherein the power management software is embedded firmware in the integrated circuit.

51. (New) The system of claim 39, wherein the first power manager is located outside the integrated circuit.

52. (New) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

in a first power manager, managing the first power consumption based on needs and operation of the integrated circuit, determining power-trade-offs between the power

islands, and monitors the plurality of power islands if a temperature threshold has been exceeded; and

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

changing a source voltage; and

changing a clock frequency of the clock of the first power island.

53. (New) The method of claim 52, wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency.

54. (New) The method of claim 53, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

55. (New) The method of claim 52, wherein the request is communicated to the second power manager by the first power manager.

56. (New) The method of claim 52, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

57. (New) The method of claim 52, wherein the source voltage of the first power island is controlled by a smart power unit.

58. (New) The method of claim 52, further comprising providing external regulation for the source voltage of the first power island.

59. (New) The method of claim 52, wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island.

60. (New) The method of claim 52, further comprising, in a third power manager:

i) managing a third power consumption of the power consumptions, and the plurality of power islands including a second power island having an associated power consumption that is the third power consumption; and

ii) communicating with the first power manager.

61. (New) The method of claim 60, wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers.

62 - 78. (Cancelled)

REMARKS

Claims 1-39 were originally issued.

Claims 40-61 were previously added.

Claims 62-78 are hereby canceled.

Claims 1-61 remain pending in the application.

It is submitted that no new matter has been added by the amendments made by this preliminary amendment. Early consideration of the application as amended is respectfully requested.

Respectfully submitted,

/Do Hyung Kim/

Dated: September 21, 2016

Do Hyung Kim
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/192,486	Filing Date 06/24/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT

06/24/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 78	Minus	** 20	= 58	X $80 =	4640
Independent (37 CFR 1.16(h))	* 8	Minus	***3	= 5	X $420 =	2100
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**6740**

AMENDMENT

09/21/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 61	Minus	** 78	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 6	Minus	*** 8	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**0**

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
MONIQUE BRUNSON

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15192486
Filing Date	2016-06-24
First Named Inventor	HOBERMAN, Barry A.
Art Unit	2851
Examiner Name	Unknown
Attorney Docket Number	01181-US-REI

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	1	20020147932	A1	2002-10-10	BROCK, et al.	

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	1	03/021409	WO	A2	2003-03-13	ANALOG DEVICES INC.		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN, Barry A.
	Art Unit	2851
	Examiner Name	Unknown
	Attorney Docket Number	01181-US-REI

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15192486
	Filing Date	2016-06-24
	First Named Inventor	HOBERMAN, Barry A.
	Art Unit	2851
	Examiner Name	Unknown
	Attorney Docket Number	01181-US-REI

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Do Hyung Kim/	Date (YYYY-MM-DD)	2016-08-31
Name/Print	Do Hyung Kim	Registration Number	66487

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
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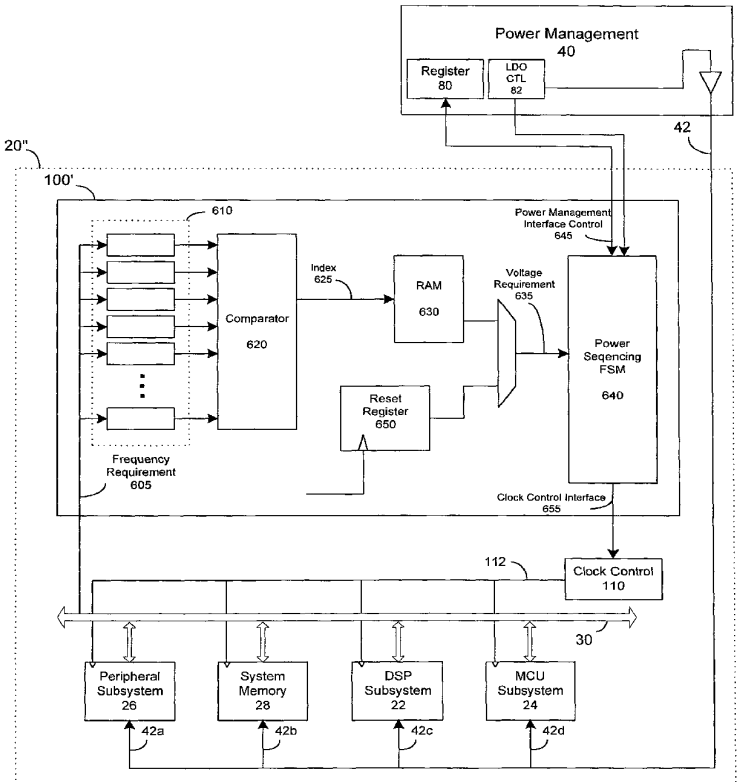
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(54) Title: DYNAMIC VOLTAGE CONTROL METHOD AND APPARATUS



(57) Abstract: A dynamic power controller is provided that identifies a clock frequency requirement of a processor and determines a voltage requirement to support the clock frequency requirement. The dynamic power controller transitions the processor to a power state defined by the clock frequency requirement and the voltage requirement. In particular, a voltage level indicated by the voltage requirement is supplied to the processor and the frequency distribution indicated by the frequency requirement is provided to the clocks signals of the processor.

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DYMNAMIC VOLTAGE CONTROL METHOD AND APPARATUS

This application claims the benefit of U.S. Provisional Application 60/315,655 under 35 U.S.C. §119(e) filed August 29, 2001, entitled "DIGITAL BASEBAND PROCESSOR," by Allen, et al. The entirety of the above provisional application is hereby incorporated by reference.

Field of the Invention

This invention relates to reducing the power consumption in processors and, more particularly, to methods and apparatus for dynamically controlling the voltage level supplied to a processor based on the processing state and/or computational demands of the processor by determining the clock frequency requirement and a corresponding voltage requirement of the processor.

Background of the Invention

Power consumption and management is a design concern for developers of processors, digital devices, computer systems etc. In battery powered devices such as cellular phones, laptop computers, person digital assistants (PDAs), and other portable and handheld devices, power consumption may be a significant contributor to the length of time during which a device may operate before the device must either be recharged and/or connected to an alternate power source. As such, power consumption may significantly impact the utility of these devices.

In some computer systems and/or digital devices, power control may provide a binary power state wherein the first power state corresponds to an idle processor and the second power state corresponds to an active processor. However, the processor in a digital device, for example, may have a variety of active processing states with computational demands that require varying levels of power to support the processing state.

However, conventional power control methods may not consider differing power demands of the processor. As such, depending on the computational requirements of the processor, a device may be consuming power in excess of that required to perform the computational tasks and/or functions of the processor.

Summary of the Invention

One embodiment according to the present invention includes a method of dynamic power control in a system having at least one processor, the at least one processor including at least one clock signal capable of operating at a plurality of frequencies. The method comprises acts of determining a clock frequency requirement of the at least one processor, determining a voltage requirement to support the clock frequency requirement, operating the at least one clock signal according to the clock frequency requirement, and providing a voltage to supply the at least one processor according to the voltage requirement.

Another embodiment according to the present invention includes a processor including at least one clock signal operating at a plurality of frequencies. The processor comprises one or more clocked components receiving the at least one clock signal, and a controller coupled to at least one of the components to determine a clock frequency requirement of the processor, the controller adapted to determine a voltage requirement based on the clock frequency requirement of the processor and to sequence a transition to a power state defined by the clock frequency requirement and the voltage requirement.

Another embodiment according to the present invention includes a controller to dynamically control the power to a processor. The controller comprises a plurality of registers to store information indicating a clock frequency requirement of the processor, a comparator coupled to the plurality of registers, the comparator configured to determine a voltage requirement based on the information stored in the plurality of registers, and a sequencer coupled to the comparator to receive the voltage level signal, the sequencer configured to transition the processor to a power state defined by the clock frequency requirement and the voltage requirement.

Another embodiment according to the present invention includes a low power device comprising at least one processor having a plurality of clocked components operating with a plurality of clock signals, a power supply adapted to provide a variable voltage to the at least one processor, a clock controller adapted to control the frequency of the plurality of clock signals, and a dynamic power controller connected to the power supply and the clock controller, the dynamic power controller adapted to monitor the at least one processor to

determine a clock frequency requirement of the at least one processor and to determine a voltage requirement based on the frequency requirement, the dynamic power controller configured to transition the power supply and the clock controller to a power state defined by the clock frequency requirement and the voltage requirement.

Brief Description of the Drawings

Fig. 1 illustrates a block diagram various subsystems of an exemplary processor;

Fig. 2 illustrates a clocking scheme and control to generate and distribute clock signals to the various components of the processor illustrated in Fig. 1;

Fig. 3 illustrates a diagram of how exemplary clock signals of a processor may vary as a function of time in different operating modes;

Fig. 4 illustrates a processor having dynamic power control capabilities according to one embodiment the present invention;

Fig. 5 illustrates a method of providing dynamic power control to a processor according to one embodiment of the present invention;

Fig. 6 illustrates one embodiment of a dynamic power controller according to the present invention; and

Fig. 7 illustrates another embodiment of a dynamic power controller according to the present invention.

Detailed Description

In many devices, particularly battery powered devices, it is advantageous to reduce the amount of time in which the device's processor is consuming excess power. A processor is considered to be consuming excess power when the computational tasks, functions, and operations of the processor may be performed, and/or the processing demands met, at a lower power state. The term "processor" refers, generally, to any apparatus that performs logic operations, computational tasks, control functions, etc. A processor may include one or more subsystems, components, and/or other processors. A processor will typically include various logic components that operate using a clock signal to latch data, advance and/or sequence logic states, synchronize computations and logic operations, and/or provide other timing functions.

Applicant has observed that the power consumption of a device is related to the square of the voltage supplied to the device's processor and proportional to the frequency at which the processor operates. The power consumption of a device may be expressed as:

$$P_D = cV^2F \qquad \text{(Equation 1)}$$

where,

V = the voltage supplied to the device (i.e., the difference between Vdd and Gnd)

F = the frequency (e.g., the clock frequency of a device)

c = a constant determined by the circuits operating at V and F.

In addition, Applicant has recognized that the voltage needed to operate the processor may be a function of the clock frequency or frequencies being provided and distributed to the processor. Accordingly, one way to reduce the power consumption of a device is to dynamically adjust the frequency of the clock signals provided to a processor to reflect the clock frequency requirement of the processor.

The term "clock frequency requirement" refers generally to the clock frequency or set of clock frequencies provided to a processor that are necessary to support the tasks, functions, and/or computational requirements of a processor. Typically, a clock signal or clock signals having a frequency below the clock frequency requirement are not sufficient to operate the logic gates, flips-flops, other clocked circuitry and components to which the clock signal is provided, and are not sufficient to complete tasks in the required amount of time, and/or incapable of performing one or more operations of the processor.

As noted above, the voltage required by the processor may be a function of the clock frequency or set of clock frequencies (i.e., the clock frequency requirement) provided and distributed to the processor. As such, when the computational demands of a processor are low, the processor may have a reduced clock frequency requirement. Therefore, the voltage necessary to support the clock frequency requirement, that is, the voltage requirement, may be reduced accordingly.

The term "voltage requirement" refers, generally, to the voltage level or levels supplied to a processor to support a given clock frequency requirement. In particular, a

voltage requirement indicates a voltage value or level sufficient to drive the various clock signals of a processor according to the clock frequency requirement without causing the clocked components to operate erroneously (e.g., memory access failures, timing violations, delays in critical speed paths, etc.). While there may be many voltage levels that will support a clock frequency requirement (e.g. voltages exceeding some minimum voltage), the voltage requirement typically refers to a voltage level that more closely meets the needs of the clock frequency requirement.

As the computational demands on a processor vary with time, there may be opportunities to reduce both the clock signal frequencies and the voltage level applied to the processor (i.e., the processor may be transitioned into a lower power state). Thus, the power consumption of the device can be dynamically adjusted to reflect the processing requirements of the processor. Accordingly, one embodiment according to the present invention includes identifying a clock frequency requirement of a processor and adjusting the voltage supplied to the processor to support the identified clock frequency requirement.

Fig. 1 illustrates a block diagram of an exemplary processor 20. Processor 20 may, for instance, be fabricated on a single semiconductor chip. Processor 20 includes a digital signal processor (DSP) subsystem 22, a microcontroller (MCU) subsystem 24, system memory 28, and peripheral subsystem 26. The various subsystems of the processor are connected to a system bus 30 in order to communicate and/or transfer data between the various components, such as, operands or instructions, addresses and/or control signals, etc.

DSP subsystem 22 may include a high speed digital signal processor. Operation of a digital signal processor is often characterized by real-time performance, computationally intensive and often time critical tasks, frequent memory accesses, etc. The MCU subsystem 24, for instance, may carry out various control functions, coordinate system events, execute system software, etc., and may operate at a lower clock frequency than the DSP. System memory 28 may be an on-chip memory, such as a RAM, providing a memory resource shared by the various subsystems of processor 20. Peripheral subsystem 26 may include the various interfaces and logic required for the processor to communicate with off-chip devices or other processors. For example, peripheral subsystem 26 may communicate with an off-chip power management chip or access an off-chip memory. In addition, the peripheral

subsystem may include interfaces to support various communication standards such as serial, Infrared Data Association (IrDA), Universal Serial Bus (USB), SIM interfaces, etc.

The processor depicted in Fig. 1 and similar variants will be used herein to illustrate and demonstrate various aspects of the present invention, however, it should be appreciated that the components and subsystems of the processor here and throughout are merely exemplary. The invention is not limited to or by the number, type, or configuration of the components in a processor implementation. Any device, processor, and/or logic circuitry having a clock frequency requirement that may vary with time is considered to be within the scope of the invention.

As an example, DSP subsystem 22 may also include a variety of components including a scratch memory, a coprocessor, interrupt controller, a dedicated bus, etc. The various components of the DSP subsystem itself may have independent clock frequency requirements. Likewise, the other processor components such as MCU subsystem 24 and peripheral subsystem 26 may contain a variety of clock frequency requirements. As such, the clock frequency requirement of the processor may vary frequently, that is, the active state of the processor may have numerous operating modes.

As such, processor 20 may have a clock frequency requirement that varies with time. For instance, in some operating modes, the DSP may be in an idle state. As such, the high frequency clock signal required by the DSP to perform certain computational tasks may not be necessary in such operating modes. The term "operating mode" characterizes a processing state or set of processing states of the various components of a processor that give rise to a particular clock frequency requirement of the processor. Typically, an operating mode characterizes a processing state of the processor in which it may be possible to transition to a different power state.

In order to provide a processor with the various clock signals that it requires, a single low frequency clock, referred to herein as the system clock, is often provided to the processor as a clock reference. The various clock frequencies required by the processor are then generated from the system clock and distributed appropriately to the subsystems and/or components of the processor. The various clock frequencies required by the processor are often generated from the system clock by a phase locked loop (PLL) multiplier, such that the

clock signals distributed to the components of the processor are in-phase with the common reference clock. That is, the clock signals distributed throughout the processor are synchronized.

Fig. 2 illustrates an exemplary system clocking scheme, for example, that distributes the clock signals at the required frequencies to the various components of processor 20. An exemplary set of components that may be part of processor 20 are illustrated in Fig. 2, including DSP 22a, coprocessor 22b, DSP bus 22c (e.g., a dedicated bus that interconnects the DSP subsystem 22), DSP SRAM 22d (e.g., a cache, scratch memory, etc.), MCU 24a, system memory (SMEM) 28, peripheral bus 26a, and external bus (EBUS) 26b. The term clock domain refers generally to a clock signal and a set of frequencies at which the clock signal normally operates. Typically, components operating in a clock domain will have one or more clocked elements (e.g., logic gates, flip-flops, etc.) that operate at the set of frequencies of the respective clock domain. A component may operate in more than one clock domain and, conversely, a clock domain may service more than one component.

The various clock signals and clock signal frequencies required by processor 20 are provided and distributed by the components of clock control 110. In particular, clock control 110 includes a system clock signal 82 and system PLL multiplier 114. System clock signal 82, or simply the system clock, is provided as a reference to synchronize the various other clock signals distributed to the processor. System PLL multiplier 114 receives the system clock signal 82 and provides a high frequency clock signal 84 and locks it in-phase with the system clock signal. Typically, clock signal 84 is some multiple of the system clock.

Fig. 2 illustrates three major clock domains generated from system clock signal 82 and the PLL clock signal 84; clock domain 90a, clock domain 90b, and clock domain 90c. The components of processor 20 operate within these clock domains. For example, DSP 22a and coprocessor 22b may operate in clock domain 90a. DSP bus 22c, and DSP SRAM may operate within clock domain 90b. MCU 24a, SMEM 28, peripheral bus 26a, and external bus (EBUS) 26b, may operate within clock domain 90c.

The clock signals in each clock domain are provided by various select, divider, and gating logic and distributed to the components of the processor via a plurality of clock trees

50a-50h. For example, clock control 110 includes multiplexers in each of clock domains (e.g., multiplexers 70a, 70b, and 70c, respectively) which may independently select whether clock signal 84 is required in order to operate the components in the corresponding clock domain. Otherwise, clock signal 84 may be bypassed and the system clock signal 82 may be provided to the appropriate components of the processor.

Additionally, clock control 110 may divide the frequency of clock signal 84 in order to provide the components of the processor with clocks signals having reduced frequencies in order to meet the clock frequency requirement of the processor. In particular, dividers 62 and 64 allow the frequency of clock signal 84 to be reduced in frequency. For example, divider 62 may provide the clocked components operating in clock domain 90b with a clock signal having half the frequency of clock signal 84 when the clock signal from the system PLL multiplier is selected. Similarly, divider 64 may provide the clocked components operating in clock domain 90c with a clock signal having a frequency reduced by factors of 2, 4, 6, 8, 10, 12, and 14. Dividers 62 and 64 may be, for instance, divide-by-n counters or equivalent components for reducing the frequency of a clock signal. The various divider factors selected for each clock domain may be selected, for example, by divider select 66.

In the clocking scheme illustrated in Fig. 2, there are multiple stages where power is being consumed. System PLL multiplier 114, for example, may include a voltage controlled oscillator (VCO) in order to generate clock signal 84. As is known in the art, a voltage controlled oscillator provides a voltage to an oscillator to produce a signal having a frequency proportional to the provided voltage. As such, the power consumed in generating clock signal 84 is proportional to the frequency being generated.

In addition, in order to provide clock signals to the various clocked circuits, logic gates, flip-flops, etc. of the processor, clock distribution trees, or simply clock trees, are provided within the components and/or subsystems of the processor. For example, clock tree 50a drives the clock signal of clock domain 90a and distributes it to the low level components of DSP 22a. Similarly, clock tree 50e drives the clock signal of clock domain 90c and distributes it to the low level logic components of MCU 24a. Power is required to charge the various clock trees, thus, power may be conserved if the clock trees may be disabled when the associated components are in an idle state. Moreover, further clock

gating logic may be included within the clock trees in order to control power consumption at a finer granularity, that is, to gate off certain portions of the clock tree distribution network.

As such, by recognizing the clock frequency requirement of the processor, clock control 100 may configure the frequency distribution to reduce the intervals when excess clock frequencies are being generated. In addition, clock control 110 may control the disabling of various clock trees or portions of clock trees according to the clock frequency requirement of the processor.

It should be appreciated that the clocking scheme illustrated in Fig. 2 is merely exemplary and is meant to illustrate one scheme by which the various clock signals required by a processor may be controlled and distributed to the components and/or subsystems of the processor. However, various system clocking schemes will occur to those skilled in the art to satisfy a particular set of clocking requirements. For instance, the system clock is shown as being multiplexed with the clock signal provided by the PLL multiplier. However, the system clock may be considered and distributed as a separate clock domain independent of the PLL clock signal. The particular design choice for a system clocking scheme is not limiting and the various alternatives, modifications, and improvements are considered to be within the scope of the invention.

Fig. 3 is a diagram illustrating how the various clock frequencies distributed to a processor might vary over time. Plot 300 shows exemplary frequency values of four clock domains of a system clocking scheme of a baseband processor as they might vary in time. The baseband processor producing the exemplary clock frequency requirement function illustrated in Fig. 3 may be similar to processor 20 illustrated in Fig. 1. Clock domain 310, denoted by the dotted line, and clock domain 320, denoted by the regular solid line, may be similar to clock domains 90a and 90c of Fig. 2, respectively. Clock domain 330, denoted by the dashed line, may be, for instance, a system clock domain. In addition, the baseband processor includes baseband clock domain 340, denoted by the bold line, to provide the baseband clock to the appropriate components of the processor. Often processors used in wireless communication will be synchronized to external and often remote devices operate via a low frequency baseband clock.

Labeled across the top of plot 300, are a series of operating modes indicated as O1-O9. It should be appreciated that the operating modes may be demarcated in any number of ways and will depend upon the design of a processor and the level of desired granularity. For instance, each change in frequency in one of the clock domains may be considered a different operating mode.

In operating mode O1, the only enabled clock is the baseband clock 330. All other clocks may be disabled. For instance, if the baseband processor is used in a cellular phone, for example, operation mode 1 may occur when the cellular phone is on but not being used (i.e., in a standby mode). At some time t_1, an event occurs requiring the processing power of, for example, the DSP. As such, the system clock 330 is enabled, supplied to the PLL which generates the maximum clock rate. The event triggering a transition into the second operating mode may require processing from components in clock domains 310, and 320. As such, all the clock trees may be enabled. Over time, the performance demands may decrease and the clock frequencies may be stepped down (e.g., the frequency of the clock signal generated from a system PLL multiplier may be reduced).

At a time t_2 the task or tasks requiring clock domains 310 and 320 may be completed and the computational demands of the processor reduced. As such, the system PLL multiplier may be bypassed, leaving only the system clock and the baseband clock enabled. At a time t_3, another event may occur wherein the processing requirements yield a configuration of active clock domains illustrated in operating mode O4. Similarly, operating modes O5-O9 illustrate further processing states that may give rise to the corresponding clock requirements illustrated in Fig. 2.

Accordingly, as the computational demands vary with time, the reduced processing requirements may provide opportunities where the clock signal frequencies may be reduced. Moreover, certain clock domains may be unnecessary during certain operating modes such that the associated clock trees may be disabled. In response to the changing clock frequency requirement, the voltage supplied to the processor may be adjusted to support the changing needs of the clock frequency requirement. As such, reduced clock frequency requirements may have reduced voltage requirements.

Applicants have identified and appreciated that by monitoring the clock frequency requirement of a processor, the voltage supplied to the processor can be dynamically controlled such that the processor spends less time supplying a voltage to the processor in excess of the requirement.

Fig. 4 illustrates one embodiment according to the present invention including a processor 20' having dynamic power control (DPC) capabilities. For purposes of illustration, processor 20' includes the subsystems as shown and described in connection with Fig. 1.

During operation of processor 20', the computational demands on the subsystems may vary with time. As such, the clock frequency requirement of the processor may also change as the various components and subsystems transition into different processing states. Dynamic power control (DPC) 100 may be connected to system bus 30 in order to communicate with the various subsystems of processor 20'. Dynamic power controller 100 may, alternatively, communicate with the subsystems in various other ways, such as shared registers having appropriate interconnections, etc.

In Fig. 4, processor 20' is supplied power by off-chip power management 40. Although, power management 40 is illustrated as residing off-chip, it may alternatively be located on the same semiconductor chip as the processor. Power management 40 may be any component capable of providing a source of power, typically, by providing a voltage level that may be specified by the component receiving power. For example, power management 40 may include a read/write register that may be accessed and written to in order to request a particular voltage level.

DPC 100 is connected to register 180 in order to indicate to power management the voltage level to be supplied to the processor. Power management may be, for instance, a low dropout (LDO) voltage regulator. Power management may include LDO control 182 to indicate when the voltage level specified in register 180 is stable and may be provided on supply line 142.

In addition, DPC 100 is connected to clock control 110. Processor 20' may, for example, have a system clocking scheme substantially the same as that illustrated in Fig. 2. As such, clock control 110 may include various components and logic gates to distribute

clock signals to the various subsystems of the processor. For example, clock control 110 may include a system PLL multiplier, bypass multiplexers, divider selects, disable logic, clock trees, etc., as illustrated in Fig. 2.

Clock control 110 may include a writeable register coupled to the system PLL multiplier to store the frequency to be output by the system PLL multiplier. This register, may alternatively, store a voltage value required of the VCO to produce the desired frequency, a multiplier ratio of the input clock signal required to provide the desired frequency, or some other value indicative of the desired frequency of the high frequency output clock signal produced by the system PLL multiplier. In addition, clock control may include registers or other control means by which the desired divider factors of the dividers in the various clock domains may be controlled. For instance, divider select may include a bank of registers with which to store the desired divider factors. In addition, clock control 110 may include logic that allows the various clock domains to be gated off, the clock trees independently disabled, and/or portions of the clock trees disabled.

DPC 100 monitors processor 20' to determine the processing states of the components and/or subsystems in order to determine a current clock frequency requirement of the processor. In response to the clock frequency requirement, DPC 100 determines a voltage level required to support the clock frequency requirement. DPC 100 then instructs power management 40 to adjust the voltage supplied to the processor and instructs clock control 110 to provide the frequency distribution accorded by the clock frequency requirement of the processor to the various subsystems and components.

It should be appreciated that a controller (e.g., dynamic power controller 100) may be implemented in numerous ways, such as with dedicated hardware (e.g., various circuitry, preprogrammed logic arrays, finite state machines (FSMs), etc.), or using one or more processors that are programmed using software (e.g., microcode) to perform the various functions of the controller. It also should be appreciated that implementations of a controller according to various embodiments of the present invention may include hardware, firmware, and software oriented elements.

Fig. 5 illustrates a flow chart depicting one method of dynamically adjusting the power supplied to a processor according to the present invention. For instance, the method

described below may be used by DPC 100 in order dynamically control the voltage supply to processor 20'.

In step 210, a DPC monitors the clock frequency requirement of the processor. A change in the clock frequency requirement may indicate that the voltage level supplied to the processor may be reduced or it may indicate that the processing demands of the processor now require additional voltage in order to support the new clock frequency requirement. As such, in step 220, the clock frequency requirement is evaluated in order to determine a voltage requirement necessary to support the new clock frequency requirement.

For example, the clock frequency requirement may represent the minimum frequency that each clock domain requires in order to perform the functions and/or computational tasks of the components operating in that clock domain. As such, the DPC may select the maximum value, referred to as the maximum-minimum frequency value, in order to determine the voltage requirement of the system.

Other methods of determining a voltage requirement from a clock frequency requirement of the processor will occur to those skilled in the art and may depend on the clocking scheme of a particular processor implementation. For instance, the DPC may consider which clock trees may be disabled under the new clock frequency requirement when determining the voltage requirement. The DPC may also consider more than the maximum minimum value of the clock frequency requirement when determining the voltage. The various methods for determining a voltage requirement from a given clock frequency requirement are considered to be within the scope of the present invention.

In step 230, a voltage level sufficient to support the clock frequency requirement is determined. In step 240, the current voltage level being supplied to the processor is compared to the voltage requirement determined in step 240 to determine the required voltage change, or delta, required to provide the voltage requirement.

If the sign of the voltage change is positive (i.e., the voltage requirement is greater than the current voltage level), then the sequence of events to transition to the higher power state follows that indicated in step 250a and 260a. As such, the voltage level indicated by the voltage requirement is first transitioned. For example, the DPC may request that power management increase the supply voltage to meet the voltage requirement of the processor.

After the new voltage level has been fully transitioned (i.e., the new supply voltage is stable), the new frequency distribution as indicated by the clock frequency requirement may be applied to the various subsystems of the processor. For example, the DPC may instruct clock control to distribute clock signals according to the clock frequency requirement to the processor.

If the sign of the voltage change is negative (i.e., the voltage requirement is less than the voltage level), then the sequence of events to transition to the lower power state follows that indicated in step 250b and 260b. As such, the frequency distribution indicated by the clock frequency requirement is first provided to the subsystems and components of the processor. When the processor is operating according the new clock frequency requirement, the voltage supplied to the processor is reduced to the voltage level indicated by the voltage requirement determined in step 230.

The voltage and frequency transitions may be sequenced in the order described above to avoid erroneous operation of the processor. For example, consider the clock frequency requirement for accessing memory. As the frequency increases for a fixed voltage, there may be a point at which memory access fails. As such, to avoid such potential problems during power state transitions, when going to a higher power state, the voltage may be stepped up before the clock frequency is increased. When going to a lower power state, frequency may be first decreased before reducing the voltage supplied to the processor.

The method described in connection with Fig. 5 may be realized in a number of ways and by various designs and implementations. Figure 6 illustrates one embodiment of a DPC according to the present invention. The schematic illustrates a hardware solution to dynamic power control. DPC 100' includes a bank of registers 610, a comparator 620, random access memory (RAM) 630, and power sequencing finite state machine (FSM) 640, and reset register 650. DPC 100' is illustrated as controlling the subsystems of processor 20'', which, for clarity, include those subsystems, components, and clocking scheme previously described. Power is supplied to the processor by power management 40.

Registers 610 store information indicating the clock frequency requirement of processor 20''. For instance, registers 610 may store frequency values required for each

clock domain. In addition, there may be a register associated with each subsystem operating in a clock domain to indicate the clock frequency required by each subsystem from each of the clock domains. The particular number, arrangement and association of the registers is a matter of design choice and any variation that adequately indicates the processor frequency requirement is considered to be within the scope of the invention.

Comparator 620 compares the frequency values stored in the registers in registers 610 in order to determine a voltage required to support the distribution of clock frequencies as indicated in the register bank. One method of determining the voltage requirement is to choose the largest frequency from the register bank (i.e., the comparator selects the maximum minimum value from the clock frequency requirement of the processor) to determine the voltage requirement. This frequency value, for example, may indicate the frequency required of the clock signal provided by the system PLL multiplier. The voltage requirement may then be based, at least in part, on the voltage level that the signal generator (e.g., a voltage controlled oscillator) of the system PLL multiplier needs to generate the indicated frequency.

RAM 630 may, for example, store a lookup table containing voltage values required to support various clock frequency requirements of the processor. As such, comparator 620 may map the selected frequency value or otherwise map the frequency requirement indicated in registers 610 to a location in RAM 630. The voltage level obtained from RAM 630 corresponds to the voltage requirement associated with the processor frequency requirement.

It should be appreciated that various methods of encoding the clock frequency requirement to determine a voltage level that will support the processor operating at a particular clock frequency requirement will occur to those skilled in the art. The design of the processor, clocking scheme, and other processor requirement and considerations may guide the particular mapping scheme from clock frequency requirement to voltage requirement. However, these variations do not depart from the scope of the invention.

The voltage value obtained from RAM 630 is then provided to the power sequencing finite state machine (FSM). The power sequencing FSM then transitions the processor to the power state indicated by the clock frequency and voltage requirements. For example,

the power sequencing FSM may check the current voltage level being supplied to the processor by reading the voltage value stored in register 180 in order to determine the sign of the voltage change required to meet the voltage requirement of the processor (e.g., the voltage level obtained from RAM 630).

If the sign of the voltage change is positive, the power sequencing FSM may first instruct power management 40 to supply the desired voltage level (i.e., DPC 100' may write the desired voltage level into register 180). After power management 40 has indicated that the voltage level has been transitioned and is stable (i.e., power management 40 may indicate that the voltage is stable via line 184), the power sequencing FSM may then instruct clock control 110 to increase the frequency of the various clock domains in order to meet the clock frequency requirement of the processor.

For example, power sequencing FSM may instruct clock control 110 to increase the frequency of the clock signal output from the system PLL multiplier. Alternatively, power sequencing FSM may have access to a register that indicates to the system PLL mulitplier what clock frequency should be output.

If the sign of the voltage change is negative, the power sequencing FSM may first instruct clock control 110 to reduce the clock frequency of the various clock domains to reflect the clock frequency requirement of the processor. Once the frequencies have been reduced, the power sequencing FSM may instruct the power management to modify the voltage supplied to the processor according to the voltage level obtained from RAM. As such, the power sequencing FSM insures that power state transitions are sequenced in an order that avoids potential operation errors of the processor.

Reset register 650 provides power sequencing FSM 640 with valid voltage levels during startup/reset. Since the information stored in RAM 630 may not be dependable during startup/reset, reset register 650 insures that a voltage sufficient to support the tasks involved in reset/startup, various boot events, etc., will be provided to the processor. As such, the value or values stored in reset register 650 might only be selected during startup/reset.

Each time that one of the values in the register bank changes, the comparator may re-evaluate the clock frequency requirement of the processor in order to determine whether or

not the voltage level can or should be changed in order to accommodate the new clock frequency requirement (e.g., comparator 620 decides if the processor can transition to a new power state). The bank of registers 610 may be written to, for example, by software that runs on the processor (e.g., the DSP or the MCU). As an example, referring to processor 20", consider an operating mode in which the DSP is processing a high priority task that requires a 300 MHz frequency clock. The MCU is concurrently processing a task requiring a 60 MHz frequency clock.

As such, software running on the DSP and/or MCU may write the frequency required by the various clocks domains into the associated register in register bank 610 (e.g., the register associated with clock domain 310 may store a frequency value of 300 MHz and the register associated with clock domain 320 may store a value of 60 MHz).

The comparator 620 may implement a maximum minimum selection method. Accordingly, the comparator would select the 300 MHz frequency value as a basis for determining the voltage requirement of the processor. An index into RAM 630 may be derived from the maximum minimum value, for instance, a value of 300 MHz may map to a location in memory storing a voltage value of 1.5 volts. As such, the power management may be supplying the processor with 1.5 volts in order to support the current clock frequency requirement of the processor.

At some point in time, the processor may complete its high priority task, and the computational demands of the processor may be reduced. For instance, the DSP may require only a 180 MHz clock in order to meet the processing demands of the current computation. Software running on the DSP, for instance, may identify this reduced clock frequency requirement of the DSP and write the new frequency value into the appropriate register. DPC 100'' then detects a change in one of the values stored in the register bank. Accordingly, comparator 620 may reevaluate the processor's clock frequency requirement and determine that the new maximum-minimum frequency value is 180 MHz. This new value may map, for instance, to a value of 1.2 volts in RAM 630.

Power sequencing FSM receives this new voltage value and determines that a negative voltage transition is required to reflect the voltage requirement needed to support the new clock frequency requirement of the processor. As such, the power sequencing FSM

may instruct the multiplier select value of the system PLL multiplier to be reduced in order to supply a 180 MHz clock signal. After the reduced frequency is provided by the PLL, the power sequencing FSM may write a value of 1.2 volts into register 180. Power management 40 then reads this value and supplies the new reduced voltage level to the processor. As such, the processor will operate in a reduced power state reflecting clock frequency requirement of the processor.

The comparator need not determine the index into the lookup table based on the maximum-minimum value. For instance, the comparator may consider the various clock frequencies stored in the register bank in a variety of ways. For example, the 180 MHz clock frequency of clock domain 310, may be able to be supported by a lower voltage, for instance, .09 volts. However, it may be the case that .9 volts isn't sufficient to support the processor clock frequency requirement because of the requirements of the other clock domains (e.g., 75 MHz for clock domain 320 and a 26 MHz system clock distribution). The comparator may be configured to recognize that the clock frequency requirement cannot be supported by .9 volts, and as such, and the clock frequency requirement described above may map to a voltage requirement of 1.2 volts, even though the maximum minimum value could itself be supported by a lower voltage.

At some later instant, the MCU may finish its task and require only a 45 MHz clock in order to meet the computational demands of the current processing state. Software running on the MCU, for instance, may identify the new processing state and write the new frequency value into the appropriate register.

In response to a change in a register value, the comparator may determine that the clock frequency requirement of the processor has been modified, even though the maximum-minimum value remains the same (e.g., 180 MHz). For instance, the new clock frequency requirement may map to a voltage level of .9 volts. The power sequencing FSM may then transition to the reduced power state according to the sequence described above. However, the change in frequency required by the MCU (e.g., 45 MHz) may be generated by adjusting the divider factor of the appropriate clock domain. As such, the multiplier select value of the PLL may not be reduced in some power state transistions.

At some later instant, the DSP may need to process another high priority task. As such, software may identify the new clock frequency requirement of the DSP, for instance, 240 MHz and write this value into the appropriate register. The comparator may then reevaluate the clock frequency requirement of the processor and determine that a new voltage requirement is necessary to support the current clock frequency requirement of the processor. The comparator then indexes into memory and a corresponding voltage value, for instance, 1.5 volts is issued to the power sequencing FSM. The power sequencing FSM determines that a positive change in the voltage level is required to meet the new voltage requirement.

As such, the FSM may first write the new voltage value into register 180 in order to transition the voltage supplied to the processor. After power management 40 has read the value and indicated that the voltage has been transitioned and stabilized, the FSM begins sequencing clock control in order to provide the higher clock frequency requirement (e.g., power sequencing FSM may modify or instruct clock control to modify the multiplier select value to increase the frequency of the clock signal generated by the system PLL multiplier).

There may be other factors and/or processing conditions that influence a voltage level required to support a particular clock frequency requirement. For example, the number of clock trees that may be disabled entirely may influence the voltage requirement. As such, DPC 100'' may consider more than just frequency values. For example, a DPC may consider which clock domains or which clock trees within a clock domain may be disabled during a given operating mode.

Fig. 7 illustrates another embodiment according to the present invention. Registers 610' store information indicating the frequency requirement of the processor. Registers 610' may, for example, include a register for each of the main subsystems of the processor. Each register may store a binary indication as to whether the associated subsystem requires a particular clock signal, or the clock signal of a particular clock domain.
As such, the width W of the registers 610' be related to the number of clock signals provided and distributed to the processor.

For example, assume that register 610a' corresponds to the frequency requirement of the DSP subsystem. According to the computational demands of the subsystem, the DSP

may indicate which clock signals it requires in order to meet the current processing demands. The DSP may, for instance, before transitioning to an idle state, indicate such a clock frequency requirement by writing a zero into each bit of register 610a'. Alternatively, if the DSP still requires a system clock signal, for instance, even when in an idle state, the DSP may indicate a 1 in the bit corresponding to the system clock. The other subsystems of the processor would similarly indicate which clock signals are required in order to perform the functions and/or computational tasks of a particular operating mode.

As such, comparator 620' may map the binary clock indications to a location in memory storing a voltage level to support the clock signal configuration indicated by the frequency requirement stored in registers 610'. In one embodiment, each clock domain may have an associated frequency with which it operates when a subsystem indicates that it is required. For example, the maximum clock rate may be considered when the DSP subsystem indicates that it requires the clock signal, for example, in clock domain 310 illustrated in Fig. 3.

In one aspect of this embodiment, comparator 620' includes software that considers the clock signal configuration indicated by registers 610' and determines the clock frequencies that are required. For instance, if both the MCU subsystem and the DSP subsystem require the clock signal in domain 310, the software may recognize that the frequency requirement is guided by the DSP. If the MCU indicates that the clock signal in clock domain 310 is required, but the DSP indicates that it is not required, the software may determine that the frequency of the clock signal may be reduced due to the fact that the MCU will guide the requirement. The frequency requirement determined by software may then be mapped into a location in memory storing a voltage level capable of supporting the clock frequency requirement.

Alternatively, registers 610a' may include a pair of registers for each subsystem. The first register may include a bit for each clock signal in the processor that indicates whether the subsystem requires the clock signal when in an active state. The second register may include a bit for each clock signal in the processor that indicates whether the subsystem requires the clock signal when in an idle state.

In some embodiments, RAM 630 may be replaced with a programmable logic array PLA. For example, a comparator may map information provided about the clock frequency requirement of the processor (e.g., as stored in a register bank, memory, etc.) to an encoded input. The programmable logic array may be programmed to provide an output from the encoded input indicative of a voltage level required to support the clock frequency requirement. The encoding from clock frequency requirement to an input to the PLA, as noted in the foregoing, may depend on the various design considerations of the processor.

One method of achieving a higher level of granularity in power control involves including a clock frequency requirement of a particular task, process, and/or set of related tasks in the profile of the task. For instance, when a particular task or job is to be processed, a process scheduler, for instance, may extract the frequency requirement from the task profile and update the registers of a DPC. This update may invoke a power transition of the processor. As such, a processor may operate in a power state reflecting the demands of the processor at the task or process level.

Other modifications, variations and improvements in providing power control to a processor to reduce the time the processor operates with excess power will occur to those skilled in the art and are considered to be within the scope of the invention.

Having described several embodiments of the invention in detail, various modifications and improvements will readily occur to those skilled in the art. Such modifications and improvements are intended to be within the scope of the invention. Accordingly, the foregoing description is by way of example only, and is not intended as limiting. The invention is limited only as defined by the following claims and the equivalents thereto.

What is claimed is:

CLAIMS

1. In a system including at least one processor having at least one clock signal capable of operating at a plurality of frequencies, a method of dynamic power control comprising acts of:

determining a clock frequency requirement of the at least one processor;

determining a voltage requirement to support the clock frequency requirement;

operating the at least one clock signal according to the clock frequency requirement; and

providing a voltage to supply the at least one processor according to the voltage requirement.

2. The method of claim 1, wherein the act of determining the voltage requirement includes the act of determining a maximum minimum clock frequency of the clock frequency requirement.

3. The method of claim 1, further comprising an act of determining a sign of a voltage difference between a current voltage supplied to the at least one processor and a voltage according to the voltage requirement.

4. The method of claim 3, wherein the act of providing the voltage to supply the at least one processor according to the voltage requirement is enacted before the act of operating the at least one clock signal according to the clock frequency requirement when the sign of the voltage difference is positive.

5. The method of claim 3, wherein the act of operating the at least one clock signal according to the clock frequency requirement is enacted before the act of providing the voltage to supply the at least one processor according to the voltage requirement when the sign of the voltage difference is negative.

6. The method of claim 1, wherein the at least one processor has a plurality of clock domains, each clock domain providing a clock signal at a plurality of frequencies to a plurality of components of the at least one processor; and

wherein the act of determining the clock frequency requirement includes determining the minimum clock frequency required in each of the plurality of clock domains.

7. The method of claim 6, further comprising an act of comparing the minimum clock frequency required in each of the plurality of clock domains.

8. The method of claim 7, wherein the act of comparing includes comparing the minimum clock frequency required in each of the plurality of clock domains to determine a maximum minimum clock frequency required by the plurality of clock domains.

9. The method of claim 8, wherein the act of determining the voltage requirement includes determining the voltage requirement from the maximum minimum clock frequency.

10. The method of claim 1, wherein the at least one processor has a plurality of clock domains, each clock domain providing a clock signal to a plurality of components of the processor, each clock signal having at least one associated frequency; and

wherein determining the clock frequency requirement includes determining whether each of the plurality of clock domains is required to be enabled.

11. The method of claim 10, wherein the act of determining the voltage requirement includes an act of determining the voltage requirement based on the at least one associated frequency of the clock domains that are required to be enabled.

12. A processor including at least one clock signal operating at a plurality of frequencies, the processor comprising:

one or more components receiving the at least one clock signal; and

a controller coupled to at least one of the components to identify a clock frequency requirement of the processor, the controller adapted to determine a voltage requirement based on the clock frequency requirement of the processor and to sequence a transition to a power state defined by the clock frequency requirement and the voltage requirement.

13. The processor of claim 12, wherein the controller is coupled to at least one component by a plurality of registers, the plurality of registers storing information indicating the clock frequency requirement of the processor.

14. The processor of claim 13, wherein the controller further comprises a comparator coupled to the plurality of registers, the comparator configured to determine the voltage requirement based on the information stored in the plurality of registers.

15. The processor of claim 14, wherein the processor includes a plurality of clock signals, operating at a plurality of frequencies, and provided to the one or more clocked components.

16. The processor of claim 15, wherein the plurality of registers store values corresponding to the clock frequency requirement of each of the plurality of clock signals.

17. The processor of claim 16, wherein the comparator determines the maximum value stored in the plurality of registers to determined the clock frequency requirement.

18. The processor of claim 14, wherein the controller further comprises a memory to store a plurality of voltage values.

19. The processor of claim 18, wherein the comparator maps the information stored in the plurality of registers to a location in memory storing a voltage value sufficient to support the clock frequency requirement of the processor.

20. The processor of claim 19, wherein the controller includes a finite state machine to sequence a transition to the power state defined by the clock frequency requirement and voltage requirement.

21. The processor of claim 20, wherein the finite state machine receives the voltage value obtained from the memory and determines a sign of a difference between a current voltage level being supplied to the processor and the obtained voltage value.

22. The processor of claim 21, wherein the finite state machine transitions the processor to operate with the obtained voltage value and then transitions the processor to operate with the clock frequency requirement when the sign of the difference is positive.

23. The processor of claim 21, wherein the finite state machine transitions the processor to operate with the clock frequency requirement and then transitions the processor to operate with the obtained voltage value when the sign of the difference is negative.

24. The processor of claim 13, wherein the at least one clock signal includes a plurality of clock signals provided to the one or more clocked components includes a plurality of clocked components.

25. The processor of claim 24, wherein the plurality of registers store a frequency value for each of the plurality of clock signals required by each of the plurality of clocked components.

26. The processor of claim 24, wherein the plurality of registers store a binary value to indicate whether each of the plurality of clocked components requires each of the plurality of clock signals.

27. A controller to dynamically control the power to a processor having a plurality of clock signals, the controller comprising:

a plurality of registers to store information indicating a clock frequency requirement of the processor;

a comparator coupled to the plurality of registers, the comparator configured to determine a voltage requirement based on the information stored in the plurality of registers; and

a sequencer coupled to the comparator and configured to transition the processor to a power state defined by the clock frequency requirement and the voltage requirement.

28. The controller of claim 27, wherein the plurality of registers store a plurality of frequency values required by a plurality of components of the processor.

29. The controller of claim 27, wherein each of the plurality of registers contain a bit for each of the plurality of clock signals provided to the processor, the bit indicating whether the corresponding clock signal is required to be enabled.

30. The controller of claim 28, wherein the comparator includes a memory to store a plurality of voltage values and wherein the comparator is configured to map the plurality of frequency values stored in the plurality of registers to a location in the memory storing a voltage value sufficient to support the clock frequency requirement indicated by the plurality of frequency values.

31. The controller of claim 28, wherein the comparator includes a programmable logic array, the comparator adapted to map the plurality of frequency values stored in the plurality of registers to an input to the programmable logic array, the programmable logic array programmed to provide an output to the sequencer indicative of a voltage value required to support the clock frequency requirement.

32. The controller of claim 27, wherein the sequencer is a finite state machine.

33. The controller of claim 27 in combination with the processor, the processor further including a plurality of components.

34. The combination of claim 33, wherein each of the plurality of components indicates via a respective one of the plurality of registers a clock frequency requirement of the component.

35. The combination of claim 27, wherein the plurality of registers include a bit corresponding to each of the plurality of clock signals.

36. The combination of claim 35, wherein each of the plurality of components is associated with at least one of the plurality of registers and each of the plurality of components indicate, via the bit corresponding to each of the plurality of clocks signals, whether the respective clock signal is required.

37. A device comprising:

at least one processor having a plurality of components operating with a plurality of clock signals;

a power supply adapted to provide a variable level voltage to the at least one processor;

a clock controller adapted to control a frequency of the plurality of clock signals; and

a dynamic power controller, connected to the power supply and the clock controller, adapted to monitor the at least one processor to determine a clock frequency requirement of the at least one processor and to determine a voltage requirement based on the clock frequency requirement, and configured to transition the power supply and the clock controller to a power state defined by the clock frequency requirement and the voltage requirement.

38. The low power device of claim 37, wherein the plurality of clock signals includes a system clock signal.

39. The low power device of claim 38, wherein the clock controller includes a phase locked loop (PLL) frequency multiplier to provide a high frequency clock signal synchronized to the system clock signal.

40. The low power device of claim 39, wherein the plurality of clock signals are derived from the system clock signal and the high frequency clock signal.

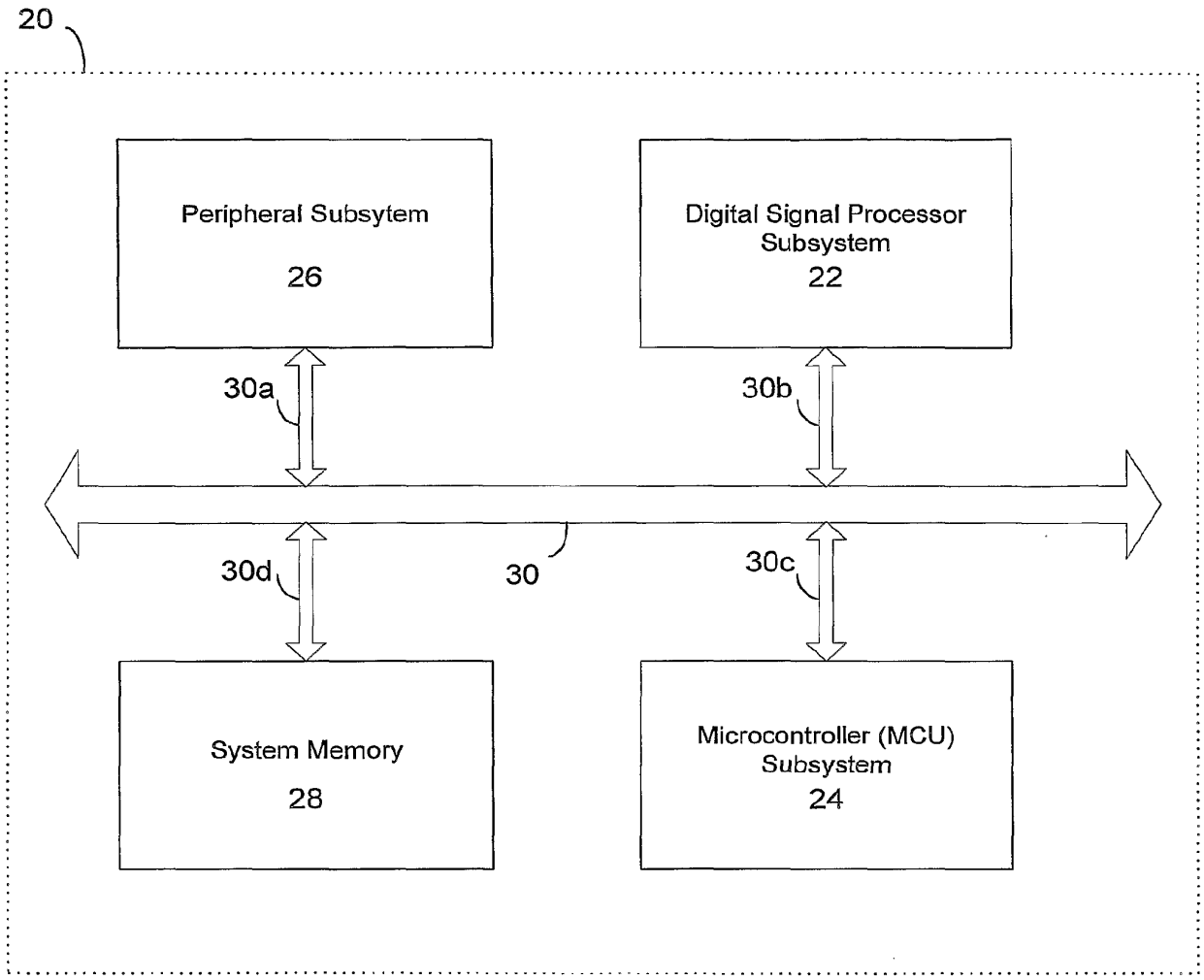

20
Peripheral Subsytem
26
Digital Signal Processor Subsystem
22
30a
30b
30
30d
30c
System Memory
28
Microcontroller (MCU) Subsystem
24

Fig. 1

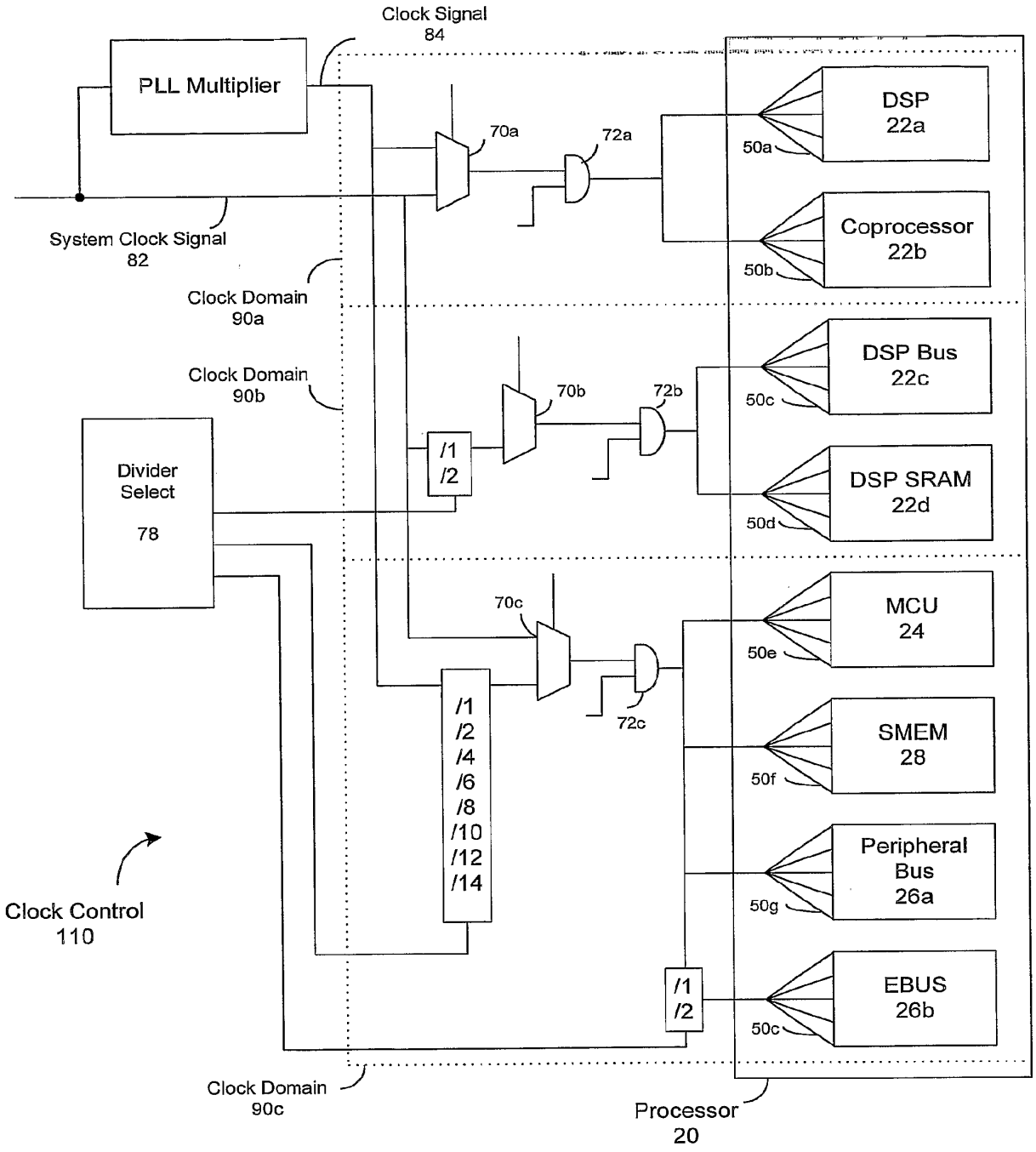

Clock Signal
84
PLL Multiplier
System Clock Signal
82
Clock Domain
90a
Clock Domain
90b
Clock Domain
90c
Divider
Select
78
70a
72a
70b
72b
70c
72c
/1
/2
/1
/2
/4
/6
/8
/10
/12
/14
/1
/2
Clock Control
110
DSP
22a
50a
Coprocessor
22b
50b
DSP Bus
22c
50c
DSP SRAM
22d
50d
MCU
24
50e
SMEM
28
50f
Peripheral
Bus
26a
50g
EBUS
26b
50c
Processor
20

Fig. 2

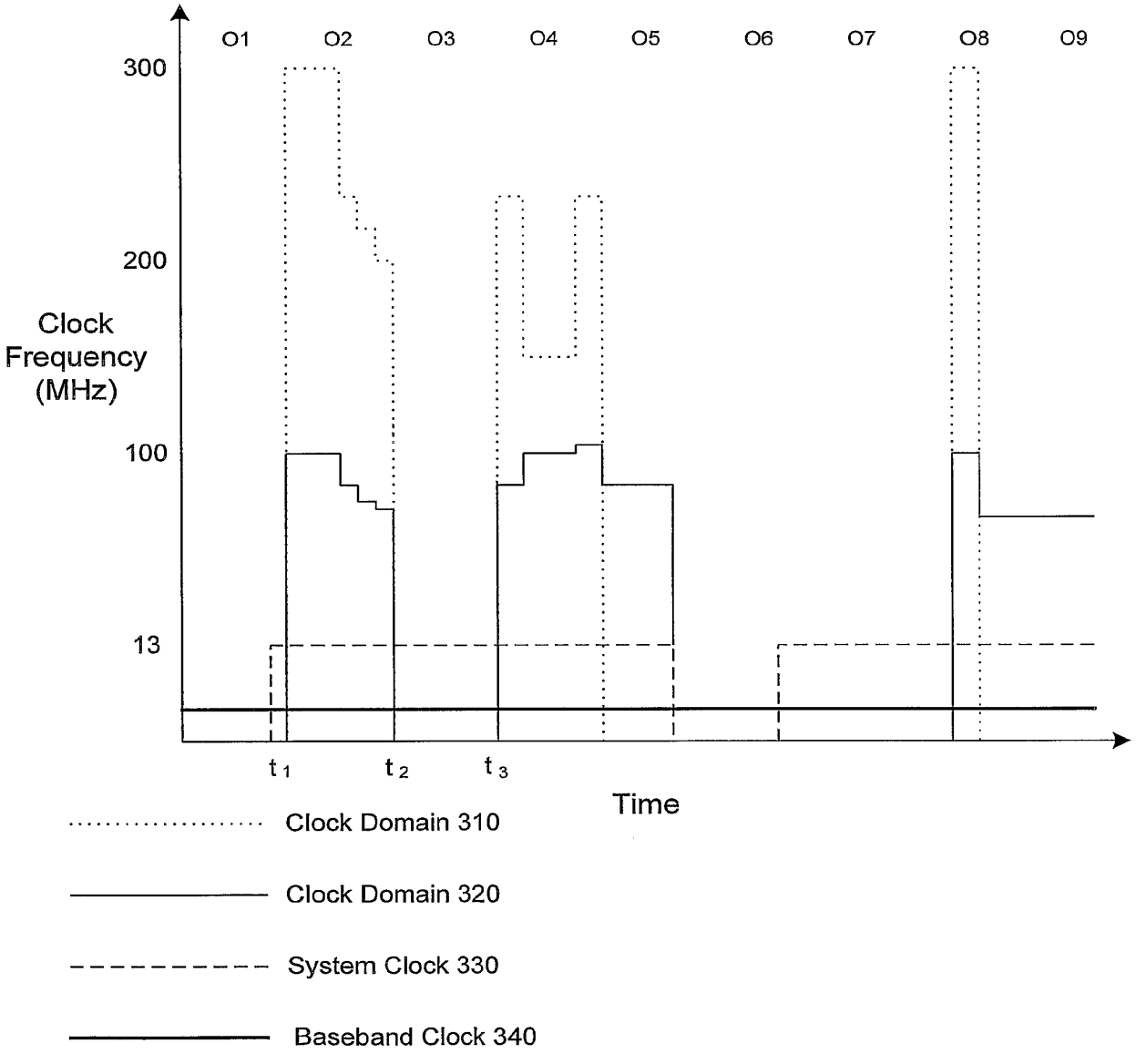

O1
O2
O3
O4
O5
O6
O7
O8
O9
300
200
100
13
Clock Frequency (MHz)
t 1
t 2
t 3
Time
Clock Domain 310
Clock Domain 320
System Clock 330
Baseband Clock 340

Fig. 3

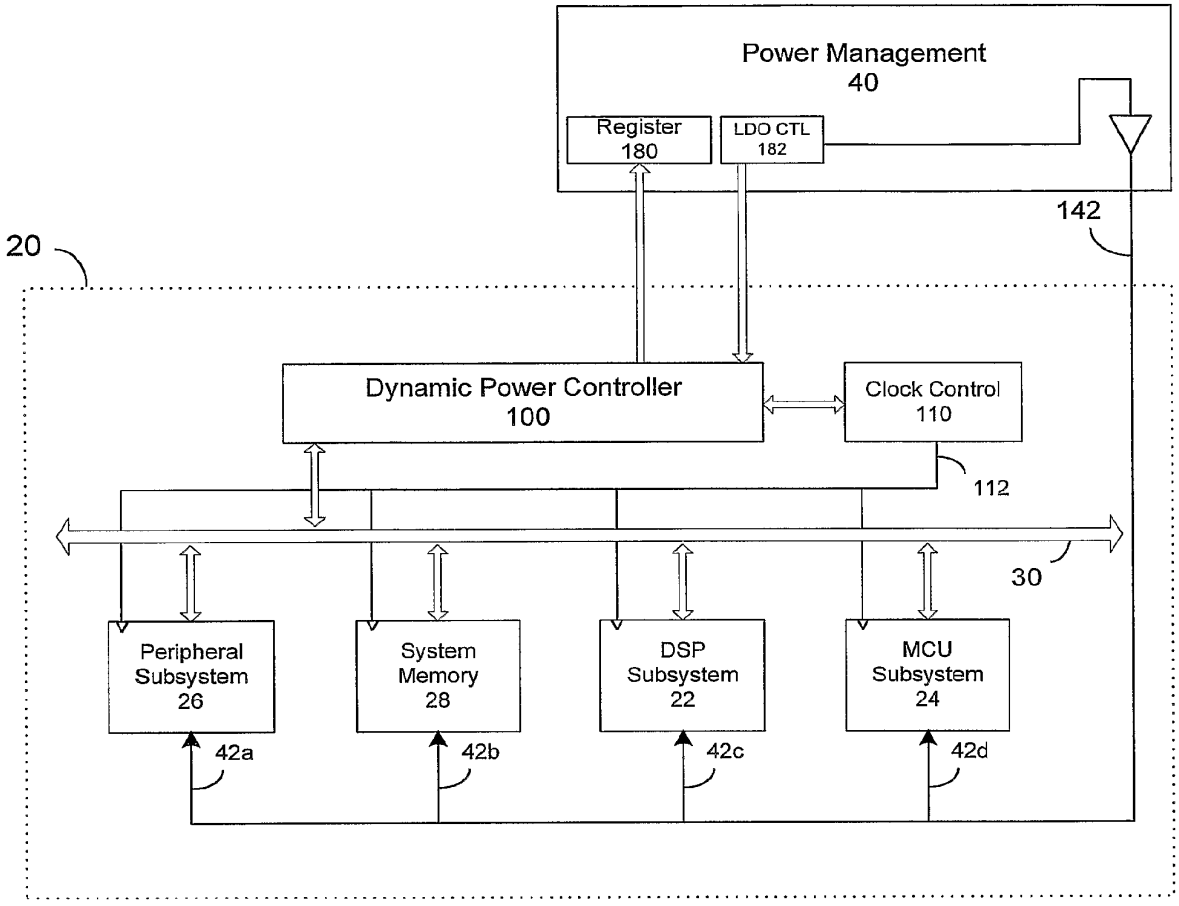

Power Management
40
Register
180
LDO CTL
182
142
20
Dynamic Power Controller
100
Clock Control
110
112
30
Peripheral
Subsystem
26
System
Memory
28
DSP
Subsystem
22
MCU
Subsystem
24
42a
42b
42c
42d

Fig. 4

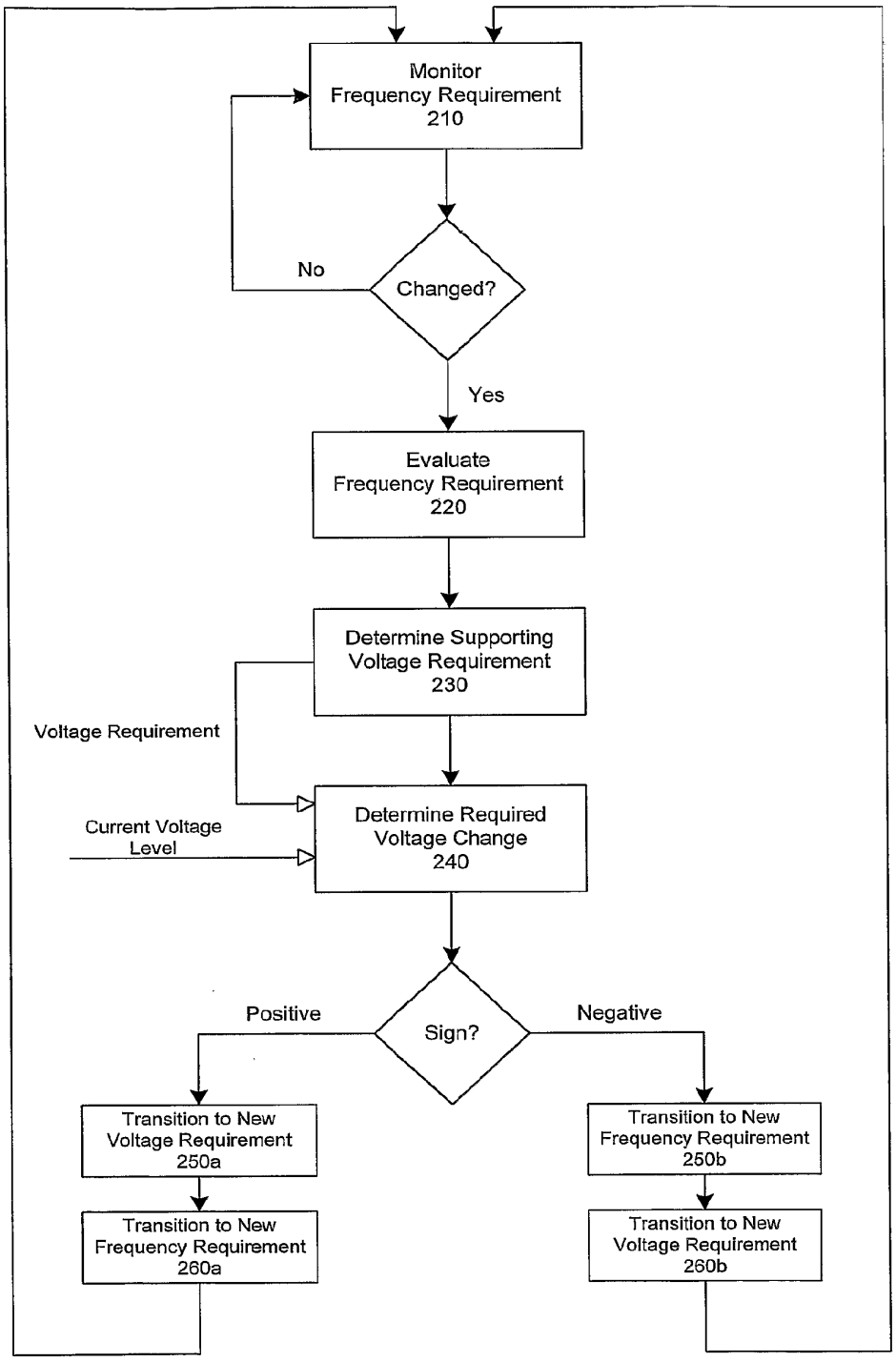

Monitor
Frequency Requirement
210
Changed?
No
Yes
Evaluate
Frequency Requirement
220
Determine Supporting
Voltage Requirement
230
Voltage Requirement
Current Voltage
Level
Determine Required
Voltage Change
240
Sign?
Positive
Negative
Transition to New
Voltage Requirement
250a
Transition to New
Frequency Requirement
260a
Transition to New
Frequency Requirement
250b
Transition to New
Voltage Requirement
260b

Fig. 5

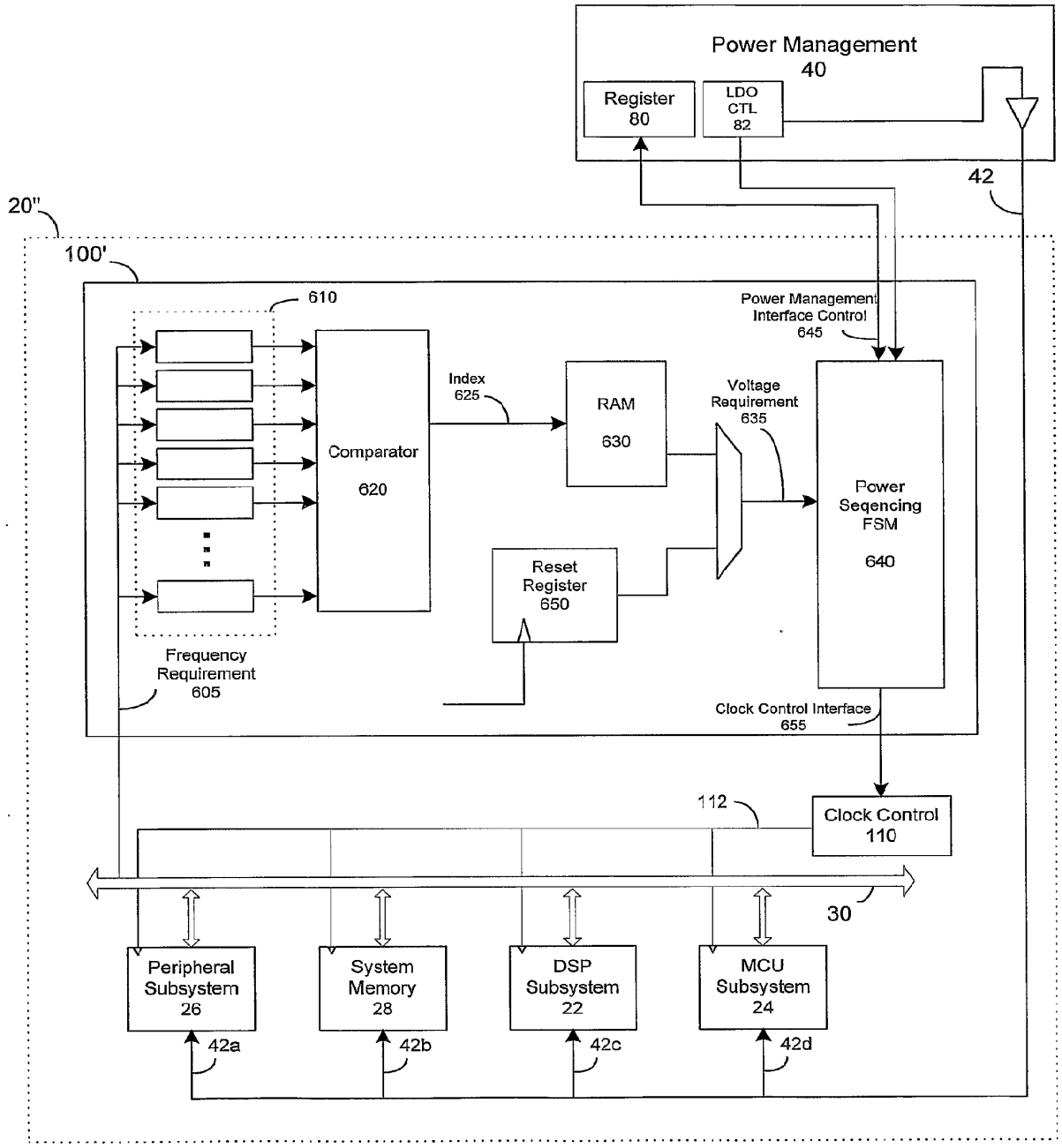

Power Management
40
Register
80
LDO
CTL
82
42
20"
100'
610
Power Management
Interface Control
645
Index
625
RAM
630
Voltage
Requirement
635
Comparator
620
Power
Seqencing
FSM
640
Reset
Register
650
Frequency
Requirement
605
Clock Control Interface
655
112
Clock Control
110
30
Peripheral
Subsystem
26
System
Memory
28
DSP
Subsystem
22
MCU
Subsystem
24
42a
42b
42c
42d

Fig. 6

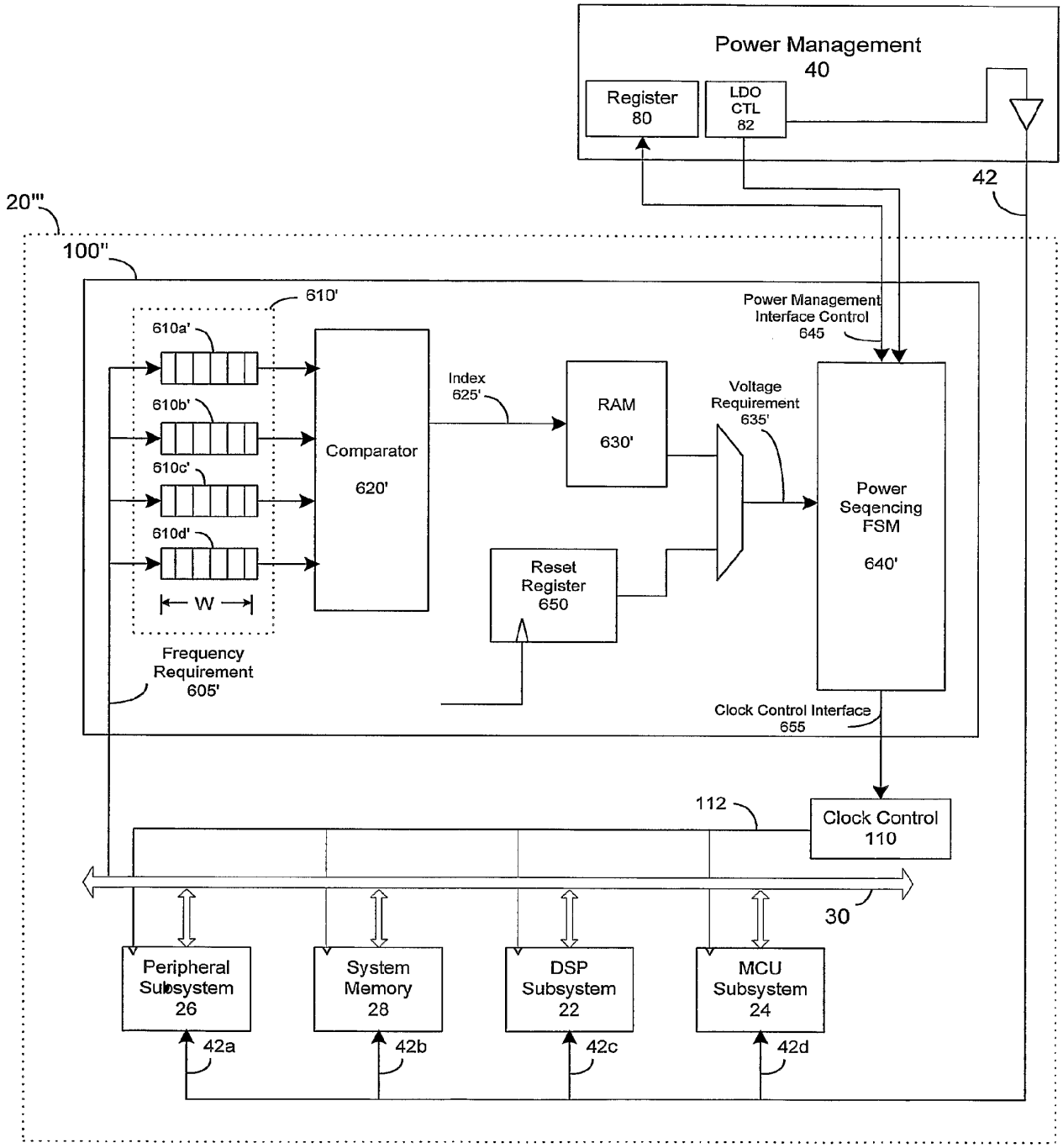

Power Management
40
Register
80
LDO
CTL
82
42
20'''
100''
610'
610a'
610b'
610c'
610d'
W
Frequency
Requirement
605'
Comparator
620'
Index
625'
RAM
630'
Power Management
Interface Control
645
Voltage
Requirement
635'
Power
Seqencing
FSM
640'
Reset
Register
650
Clock Control Interface
655
112
Clock Control
110
30
Peripheral
Subsystem
26
System
Memory
28
DSP
Subsystem
22
MCU
Subsystem
24
42a
42b
42c
42d

Fig. 7

Electronic Acknowledgement Receipt

EFS ID:	26803142
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Do Hyung Kim/Julie McLeod
Filer Authorized By:	Do Hyung Kim
Attorney Docket Number:	01181-US-REI
Receipt Date:	31-AUG-2016
Filing Date:	24-JUN-2016
Time Stamp:	16:11:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	IDS.pdf	1034999 83b328bae4b02d939738ae95bbf7aa28f5d1e87d	no	4

Warnings:

Information:					
2	Foreign Reference	WO2003021409.pdf	1721348 12f1cf07bfde5245ee7a9acdbe95296a9400d418	no	37
Warnings:					
Information:					
			Total Files Size (in bytes):	2756347	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/192,486	06/24/2016	Barry Alan Hoberman	01181-US-REI

CONFIRMATION NO. 6310

68256
Conversant Intellectual Property Management Inc.
5601 Granite Parkway
Suite 1300
Plano, TX 75024

FORMALITIES LETTER

OC000000084512012

Date Mailed: 07/21/2016

NOTICE TO FILE MISSING PARTS OF REISSUE APPLICATION

Filing Date Granted

An application number and filing date have been accorded to this reissue application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- The inventor's oath or declaration has not been submitted.
- Assignee's statement under 37 CFR 3.73(c) establishing ownership of the patent is missing. 37 CFR 1.172 requires that all assignees consenting to the reissue application establish their ownership interest in the patent by filing in the reissue application a statement in accordance with 37 CFR 3.73(c).
- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Barry Alan Hoberman
  Daniel L. Hillman
  Jon Shiell

  An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 (and 37 CFR 1.175) executed by or with respect to each inventor is required. For a reissue application, the inventor's oath or declaration must be submitted prior to examination and cannot be postponed. See 37 CFR 1.175(e). An assignee of the entire interest can execute the oath or declaration if: (1) the application does not seek to enlarge the scope of the claims of the original patent; or (2) the application for the original patent was filed under 37 CFR 1.46 by the assignee of the entire interest. A substitute statement under 37 CFR 1.64 in lieu of an oath or declaration may be submitted in the circumstances provided for in 35 U.S.C. 115(d) and 37 CFR 1.64.

- Additional claim fees of $ **6740** as an undiscounted entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **280** basic filing fee.
- $ **140** surcharge.
- $ **600** search fee.
- $ **2160** examination fee.
- $ **2100** for **5** independent claims over the original patent.
- $ **4640** for **58** total claims over the higher of 20, or the amount in the original patent.
- $(**0**) previous unapplied payment amount.
- $ **9920** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

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/cmhaywood/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/192,486

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	2160
TOTAL CLAIMS (37 CFR 1.16(i))	78 minus 20 =	* 58			OR	x 80 =	4640
INDEPENDENT CLAIMS (37 CFR 1.16(h))	8 minus 3 =	* 5				x 420 =	2100
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	9780

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/192,486	06/24/2016	2851	0.00	01181-US-REI	78	8

CONFIRMATION NO. 6310

68256
Conversant Intellectual Property Management Inc.
5601 Granite Parkway
Suite 1300
Plano, TX 75024

FILING RECEIPT

OC000000084512011

Date Mailed: 07/21/2016

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Barry Alan Hoberman, Cupertino, CA;
Daniel L. Hillman, San Jose, CA;
Jon Shiell, San Jose, CA;

Applicant(s)

Conversant Intellectual Property Management Inc., Ottawa, CANADA, Assignee (with 37 CFR 1.172 Interest);

Assignment For Published Patent Application

Conversant Intellectual Property Management Inc., Ottawa, CANADA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a REI of 13/473,129 05/16/2012 PAT 8762923
which is a DIV of 13/164,362 06/20/2011 PAT 8782590
which is a CON of 12/332,529 12/11/2008 PAT 7996811
which is a CON of 12/176,645 07/21/2008 PAT 7945885
which is a CON of 11/336,097 01/20/2006 PAT 7415680
which is a CON of 10/840,893 05/07/2004 PAT 7051306
which claims benefit of 60/468,742 05/07/2003

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 07/11/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/192,486**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Preliminary Class

716

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentees:	Barry A. HOBERMAN, *et al.*	)	Serial No.: 13/473,129
Patent No.:	8,762,923	)	Filing Date: May 16, 2012
Issue Date:	June 24, 2014	)	Title: POWER MANAGERS FOR AN INTEGRATED CIRCUIT
Assignee:	Conversant Intellectual Property Management Inc.	)	

Mail Stop Reissue
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PRELIMINARY AMENDMENT UNDER 37 C.F.R. § 1.173(b)

Dear Sir:

This is a broadening reissue application. Reissue of U.S. Patent No. 8,762,923 is respectfully requested. Prior to examination of the above-identified reissue application, consideration of the accompanying remarks and preliminary amendment is requested as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 20 of this paper.

Status of Claims and Support for Claim Changes appear on page 20 of this paper

Statement under 37 C.F.R. 1.178(b) appears on page 20 of this paper

AMENDMENTS TO THE CLAIMS

What is claimed is:

1. (Original) A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) changing a source voltage of the first power island;

ii) after the changing, waiting for the source voltage of the first power island to settle down; and

iii) after the waiting, changing a clock frequency of the first power island.

2. (Original) The system of claim 1 wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency.

3. (Original) The system of claim 2 wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

4. (Original) The system of claim 1 wherein the first power manager is further configured to communicate the request to the second power manager.

5. (Original) The system of claim 1 wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

6. (Original) The system of claim 1 wherein the source voltage of the first power island is controlled by a smart power unit.

7. (Original) The system of claim 1 wherein the source voltage of the first power island is provided by an external regulator.

8. (Original) The system of claim 1 wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

9. (Original) The system of claim 1 wherein the second power manager comprises firmware processable on the integrated circuit.

10. (Original) The system of claim 1 wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

11. (Original) The system of claim 10 wherein the power management software is embedded firmware in the integrated circuit.

12. (Original) The system of claim 1 wherein the first power manager is located outside the integrated circuit.

13. (Original) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

in a first power manager, managing ~~a~~the first power consumption based on needs and operation of the integrated circuit;

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

providing a source voltage to the first power island; and

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

changing the source voltage of the first power island;

after the changing, waiting for the source voltage of the first power island to settle down; and

after the waiting, changing a clock frequency of the clock.

14. (Original) The method of claim 13 wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency.

15. (Original) The method of claim 14 further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

16. (Original) The method of claim 13 wherein the request is communicated to the second power manager by the first power manager.

17. (Original) The method of claim 13 further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by:

lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

18. (Original) The method of claim 13 wherein the source voltage of the first power island is controlled by a smart power unit.

19. (Original) The method of claim 13 further comprising providing external regulation for the source voltage of the first power island.

20. (Original) The method of claim 13 wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island.

21. (Original) The method of claim 13 further comprising, in a third power manager:

i) managing a third power consumption of the power consumptions, and the plurality of power islands including a second power island having an associated power consumption that is the third power consumption; and

ii) communicating with the first power manager.

22. (Original) The method of claim 21 wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers.

23. (Original) A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

24. (Original) The system of claim 23 wherein the second power manager is further configured to carry out the saving of the state of the first power island after the stopping.

25. (Original) The system of claim 23 wherein the first power manager is further configured to communicate the request to the second power manager.

26. (Original) The system of claim 23 further comprising a buffer for storing the state that is saved.

27. (Original) The system of claim 23 wherein the second power manager is further configured to respond to another request, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock of the first power island.

28. (Original) The system of claim 27 further comprising a buffer for storing the state that is saved, and the buffer being accessible during the restoring.

29. (Original) The system of claim 23 wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

30. (Original) The system of claim 23 wherein the second power manager comprises firmware processable on the integrated circuit.

31. (Original) The system of claim 23 wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

32. (Original) The system of claim 31 wherein the power management software is embedded firmware in the integrated circuit.

33. (Original) The system of claim 23 wherein the first power manager is located outside the integrated circuit.

34. (Original) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

in a first power manager, managing a first power consumption based on needs and operation of the integrated circuit;

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

35. (Original) The method of claim 34 wherein the saving of the state of the first power island is carried out after the stopping.

36. (Original) The method of claim 34 wherein the request is communicated to the second power manager by the first power manager.

37. (Original) The method of claim 34 wherein the state that is saved is stored in a buffer.

38. (Original) The method of claim 34 further comprising responding to another request that is received by the second power manager, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock.

39. (Original) The method of claim 38 wherein the state that is saved is stored in a buffer accessed during the restoring.

40. (New) A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to:

a) manage the first power consumption based on needs and operation of the integrated circuit;

b) determine power trade-offs between the power islands;

c) monitors the plurality of power islands if a temperature threshold has been exceeded; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) changing a source voltage; and

ii) changing a clock frequency of the first power island.

41. (New) The system of claim 39, wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency.

42. (New) The system of claim 41, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

43. (New) The system of claim 39, wherein the first power manager is further configured to communicate the request to the second power manager.

44. (New) The system of claim 39, wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

45. (New) The system of claim 39, wherein the source voltage of the first power island is controlled by a smart power unit.

46. (New) The system of claim 39, wherein the source voltage of the first power island is provided by an external regulator.

47. (New) The system of claim 39, wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

48. (New) The system of claim 39, wherein the second power manager comprises firmware processable on the integrated circuit.

49. (New) The system of claim 39, wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

50. (New) The system of claim 39, wherein the power management software is embedded firmware in the integrated circuit.

51. (New) The system of claim 39, wherein the first power manager is located outside the integrated circuit.

52. (New) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

in a first power manager, managing the first power consumption based on needs and operation of the integrated circuit, determining power-trade-offs between the power islands, and monitors the plurality of power islands if a temperature threshold has been exceeded; and

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

changing a source voltage; and

changing a clock frequency of the clock of the first power island.

53. (New) The method of claim 52, wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency.

54. (New) The method of claim 53, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock

frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

55. (New) The method of claim 52, wherein the request is communicated to the second power manager by the first power manager.

56. (New) The method of claim 52, further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by: lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

57. (New) The method of claim 52, wherein the source voltage of the first power island is controlled by a smart power unit.

58. (New) The method of claim 52, further comprising providing external regulation for the source voltage of the first power island.

59. (New) The method of claim 52, wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island.

60. (New) The method of claim 52, further comprising, in a third power manager:

i) managing a third power consumption of the power consumptions, and the plurality of power islands including a second power island having an associated power consumption that is the third power consumption; and

ii) communicating with the first power manager.

61. (New) The method of claim 60, wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers.

62. (New) A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to:

a) manage the first power consumption based on needs and operation of the integrated circuit;

b) determine power trade-offs between the power islands;

c) monitors the plurality of power islands if a temperature threshold has been exceeded; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

63. (New) The system of claim 62, wherein the second power manager is further configured to carry out the saving of the state of the first power island after the stopping.

64. (New) The system of claim 62, wherein the first power manager is further configured to communicate the request to the second power manager.

65. (New) The system of claim 62, further comprising a buffer for storing the state that is saved.

66. (New) The system of claim 62, wherein the second power manager is further configured to respond to another request, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock of the first power island.

67. (New) The system of claim 66, further comprising a buffer for storing the state that is saved, and the buffer being accessible during the restoring.

68. (New) The system of claim 62, wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

69. (New) The system of claim 62, wherein the second power manager comprises firmware processable on the integrated circuit.

70. (New) The system of claim 62, wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

71. (New) The system of claim 70, wherein the power management software is embedded firmware in the integrated circuit.

72. (New) The system of claim 62, wherein the first power manager is located outside the integrated circuit.

73. (New) A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

in a first power manager, managing a first power consumption based on needs and operation of the integrated circuit, determining power trade-offs between the power islands, and monitoring the plurality of power islands if a temperature threshold has been exceeded; and

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

74. (New) The method of claim 73, wherein the saving of the state of the first power island is carried out after the stopping.

75. (New) The method of claim 73, wherein the request is communicated to the second power manager by the first power manager.

76. (New) The method of claim 73, wherein the state that is saved is stored in a buffer.

77. (New) The method of claim 73, further comprising responding to another request that is received by the second power manager, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock.

78. (New) The method of claim 77, wherein the state that is saved is stored in a buffer accessed during the restoring.

REMARKS

This is a broadening reissue application of U.S. Patent No. 8,762,923, which issued on June 24, 2014.

Statement of the Status of the Claims and Support for Amendments

Pursuant to 37 C.F.R. 1.173(c), Applicant states that the status of claims and support for claim changes relative to the patented claims is as follows:

Claims 1-78 are pending, of which claims 1-39 are original patent claims, and claims 40-78 are new and at least some of the new claims 40-78 are broadened relative to the original patent claims. No new matter has been added.

The support for new claims 40-78 is provided at least by original claims 1-39, respectively, and the specification as originally filed. For example, see col. 2, lines 38-55 and col. 11, lines 19-32.

Statement under 37 C.F.R. 1.178(b)

There are no prior or concurrent proceedings in which the patent for which reissue is hereby requested is or was involved.

CONCLUSION

Early and favorable consideration with respect to this application is respectfully requested. Should any questions arise in connection with this application, the undersigned respectfully requests that he be contacted at the number indicated below.

In the event that there are any questions concerning this amendment or the application in general, the Examiner is respectfully requested to telephone the undersigned so that prosecution of the application may be expedited.

The Commissioner is hereby authorized to charge any additional fees, and credit any overpayment, to Deposit Account No. 504154.

Respectfully submitted,

/ Po-Wei CHEN /

Date: June 24, 2016

Po-Wei CHEN
Reg. No. 61,767
Telephone: (214) 494-4842
Facsimile: (214) 436-4683

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Barry	Alan	Hoberman	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Inventor 2

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
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Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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City	San Jose	State/Province	CA
Postal Code	95120	Country [i]	US

Inventor 3

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jon		Shiell	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	San Jose	**State/Province**	CA	**Country of Residence** i	US

Mailing Address of Inventor:

Address 1	801 Seabury Drive		
Address 2			
City	San Jose	**State/Province**	CA
Postal Code	95136	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	68256		
Email Address	ipadmin@conversantip.com	Add Email	Remove Email

Application Information:

Title of the Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT		
Attorney Docket Number	01181-US-REI	**Small Entity Status Claimed**	☐
Application Type			
Subject Matter			
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	68256		

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					
Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					

Additional Representative Information blocks may be generated within this form by selecting the **Add** button.

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
	reissued of	13473129	2012-05-16	8762923	2014-06-24

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13473129	Division of	13164362	2011-06-20	8782590	2014-07-15

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13164362	Continuation of	12332529	2008-12-11	7996811	2011-08-09

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12332529	Continuation of	12176645	2008-07-21	7945885	2011-05-17

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12176645	Continuation of	11336097	2006-01-20	7415680	2008-08-19

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11336097	Continuation of	10840893	2004-05-07	7051306	2006-05-23

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
10840893	Claims benefit of provisional	60468742	2003-05-07

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	

If the Applicant is an Organization check here. ☒

Organization Name	Conversant Intellectual Property Management Inc.

Mailing Address Information For Applicant:

Address 1	515 Legget Drive, Suite 704		
Address 2			
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Country [i]	CA	Postal Code	K2K3G4
Phone Number	613-576-3000	Fax Number	613-591-8148
Email Address	ipadmin@conversantip.com		

Additional Applicant Data may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Conversant Intellectual Property Management Inc.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	515 Legget Drive, Suite 704		
Address 2			
City	Ottawa	**State/Province**	OT
Country i	CA	Postal Code	K2K3G4
Phone Number	613-576-3000	Fax Number	613-591-8148
Email Address	ipadmin@conversantip.com		

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	01181-US-REI
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Po-wei CHEN/			Date (YYYY-MM-DD)	
First Name	Po-wei	Last Name	CHEN	Registration Number	61767

Additional Signature may be generated within this form by selecting the Add button.

Electronic Acknowledgement Receipt	
EFS ID:	26167517
Application Number:	15192486
International Application Number:	
Confirmation Number:	6310
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan Hoberman
Customer Number:	68256
Filer:	Po-Wei Chen/Ronan O'Byrne
Filer Authorized By:	Po-Wei Chen
Attorney Docket Number:	01181-US-REI
Receipt Date:	24-JUN-2016
Filing Date:	
Time Stamp:	16:41:09
Application Type:	Reissue (Utility)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Specification.pdf	1836408 069688ef8bb4f42358ae7f45b76295b4f980bf7b	yes	28

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	7
	Drawings-only black and white line drawings	8	20
	Specification	21	26
	Claims	27	28

Warnings:					
Information:					
2	Terminal Disclaimer Filed	Terminal_Disclaimer_from_Parent.pdf	51719 d018548ff7fca623bac7b39df21529c6a5abb404	no	1
Warnings:					
Information:					
3		Preliminary_Amendment.pdf	135028 7d138ccde964256740d6e9ae1a2560912c5d2031	yes	21

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	19
	Applicant Arguments/Remarks Made in an Amendment	20	21

Warnings:					
Information:					
4	Application Data Sheet	WebADS.pdf	160482 05387a01d51102bd8e2ee4b6413a229e8561812f	no	9
Warnings:					
Information:					
		Total Files Size (in bytes):	2183637		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

US008762923B2

(12) **United States Patent**
Hoberman et al.

(10) **Patent No.: US 8,762,923 B2**
(45) **Date of Patent: *Jun. 24, 2014**

(54) **POWER MANAGERS FOR AN INTEGRATED CIRCUIT**

(75) Inventors: **Barry Alan Hoberman**, Cupertino, CA (US); **Daniel L. Hillman**, San Jose, CA (US); **Jon Shiell**, San Jose, CA (US)

(73) Assignee: **Conversant Intellectual Property Management Inc.**, Ottawa (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **13/473,129**

(22) Filed: **May 16, 2012**

(65) **Prior Publication Data**

US 2012/0256485 A1 Oct. 11, 2012

Related U.S. Application Data

(60) Division of application No. 13/164,362, filed on Jun. 20, 2011, which is a continuation of application No. 12/332,529, filed on Dec. 11, 2008, now Pat. No. 7,996,811, which is a continuation of application No. 12/176,645, filed on Jul. 21, 2008, now Pat. No. 7,945,885, which is a continuation of application No. 11/336,097, filed on Jan. 20, 2006, now Pat. No. 7,415,680, which is a continuation of application No. 10/840,893, filed on May 7, 2004, now Pat. No. 7,051,306.

(60) Provisional application No. 60/468,742, filed on May 7, 2003.

(51) **Int. Cl.**
G06F 17/50 (2006.01)

(52) **U.S. Cl.**
USPC **716/133**; 716/100; 716/120; 716/126; 716/127

(58) **Field of Classification Search**
CPC G06F 1/3203; G06F 1/324; G06F 1/3296; G06F 1/26; Y02B 60/1217; Y02B 60/1285
USPC 716/100, 120, 126, 127, 132, 133
See application file for complete search history.

(56) **References Cited**

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5,485,127 A 1/1996 Bertoluzzi et al.
5,585,745 A 12/1996 Simmons et al.

(Continued)

FOREIGN PATENT DOCUMENTS

CN 1353454 6/2002
JP 07105174 4/1995

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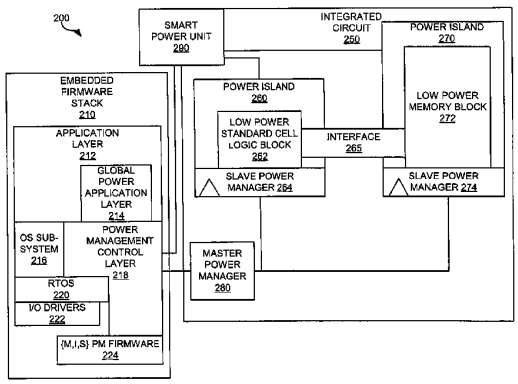
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(57) **ABSTRACT**

A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

39 Claims, 13 Drawing Sheets



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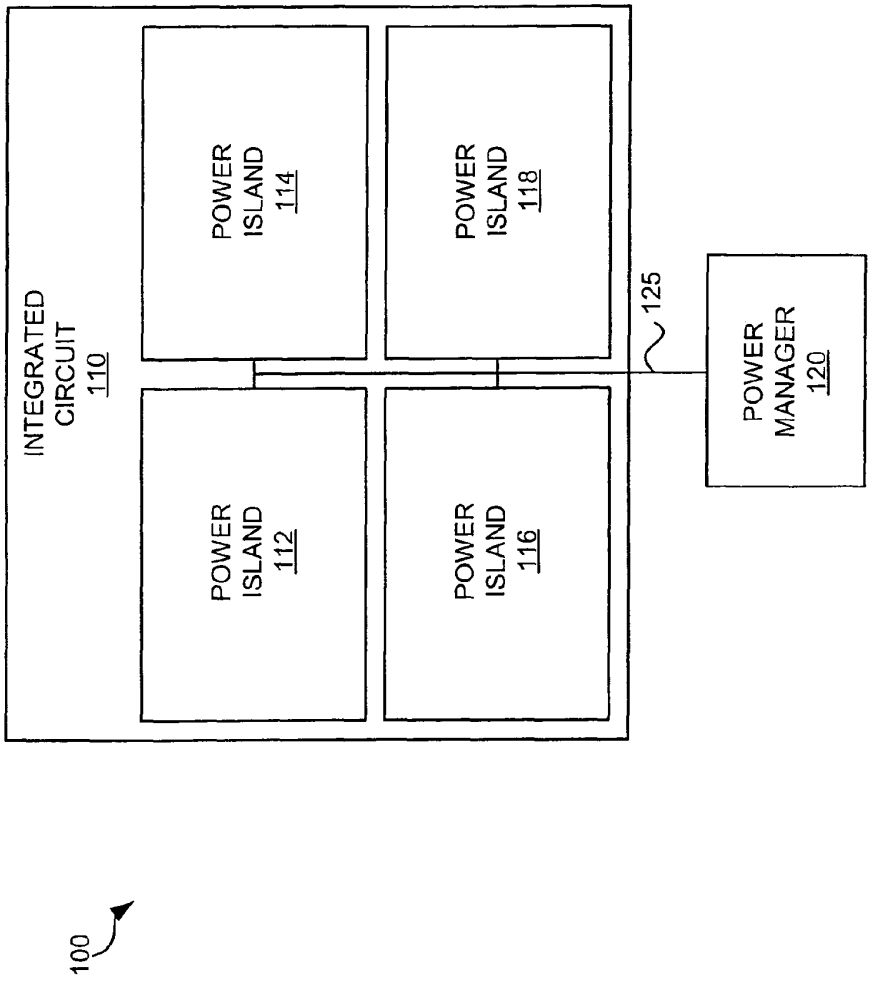

INTEGRATED CIRCUIT 110
POWER ISLAND 112
POWER ISLAND 114
POWER ISLAND 116
POWER ISLAND 118
125
POWER MANAGER 120
100

FIG. 1

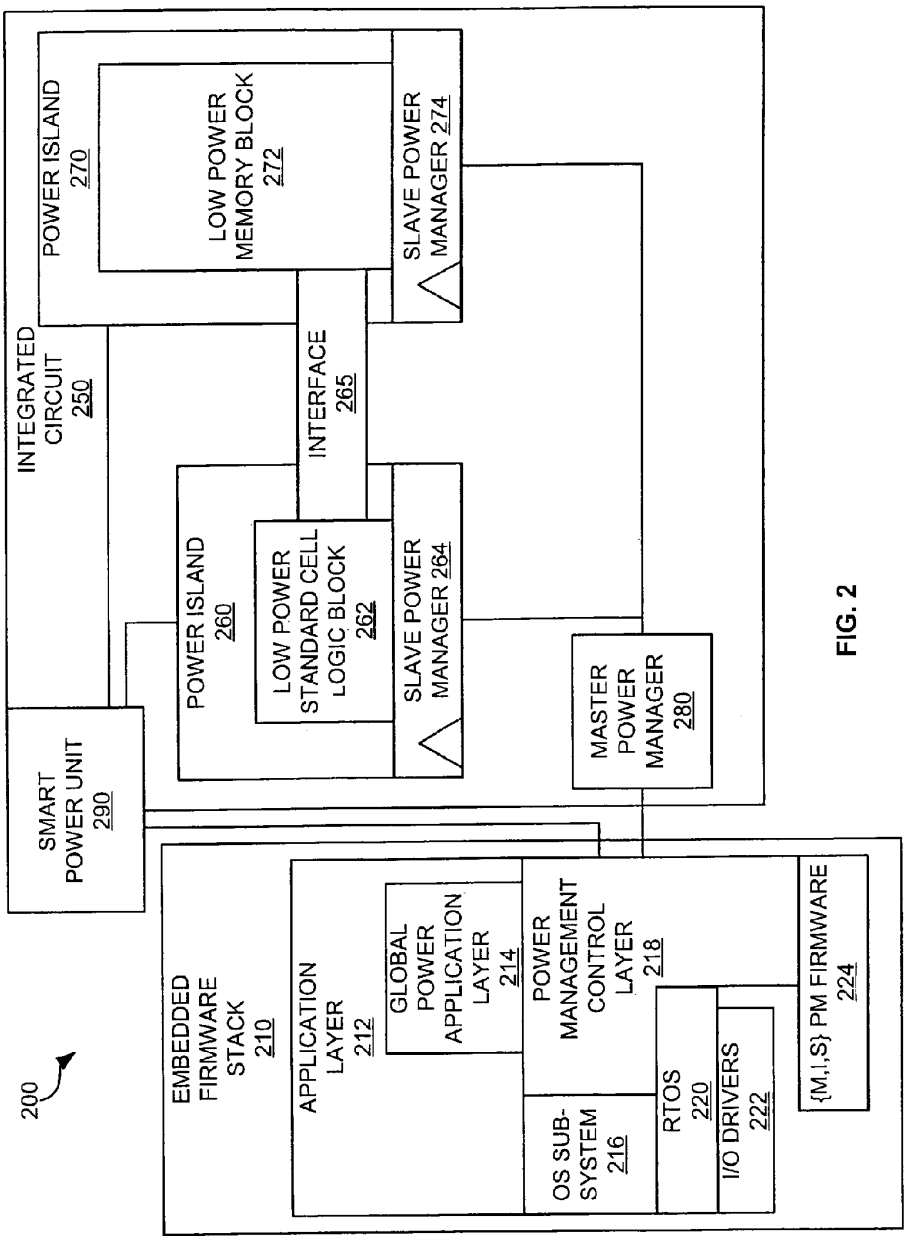

200
EMBEDDED FIRMWARE STACK 210
APPLICATION LAYER 212
GLOBAL POWER APPLICATION LAYER 214
POWER MANAGEMENT CONTROL LAYER 218
OS SUB-SYSTEM 216
RTOS 220
I/O DRIVERS 222
{M,I,S} PM FIRMWARE 224
SMART POWER UNIT 290
INTEGRATED CIRCUIT 250
POWER ISLAND 260
LOW POWER STANDARD CELL LOGIC BLOCK 262
SLAVE POWER MANAGER 264
INTERFACE 265
POWER ISLAND 270
LOW POWER MEMORY BLOCK 272
SLAVE POWER MANAGER 274
MASTER POWER MANAGER 280

FIG. 2

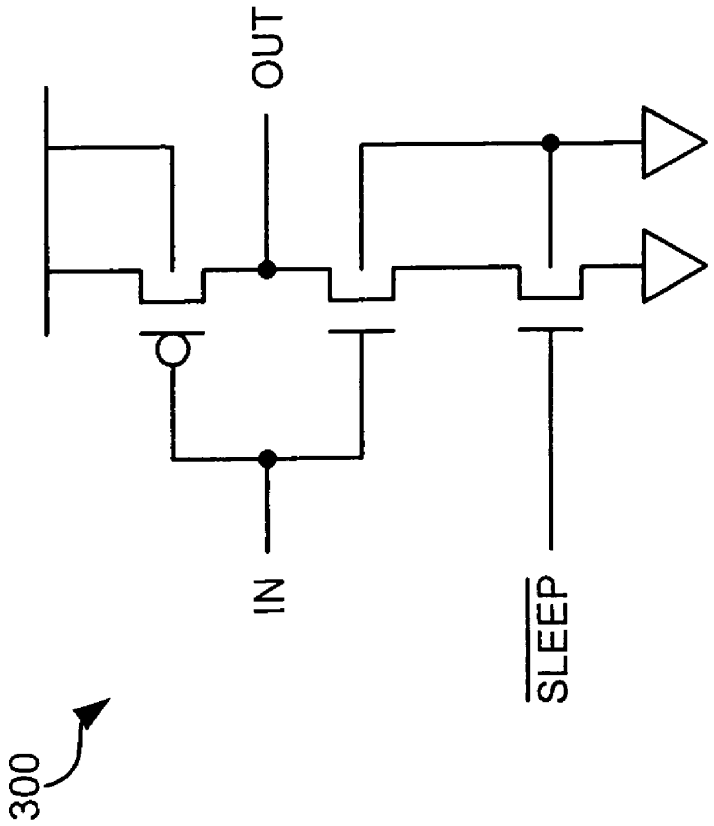


FIG. 3

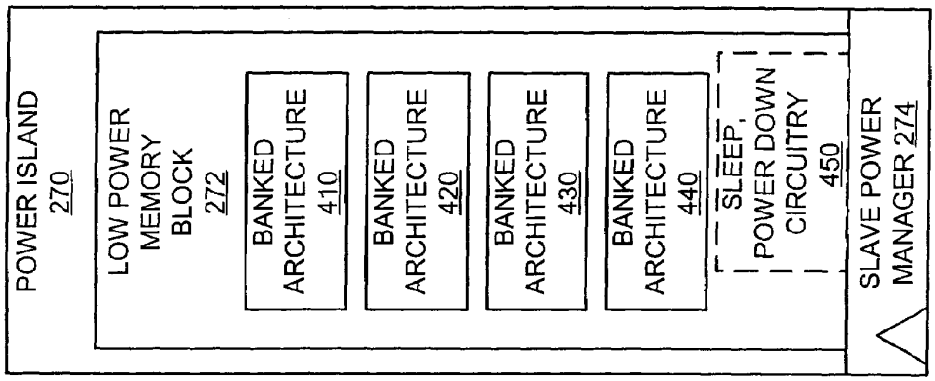

POWER ISLAND
270
LOW POWER
MEMORY
BLOCK
272
BANKED
ARCHITECTURE
410
BANKED
ARCHITECTURE
420
BANKED
ARCHITECTURE
430
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ARCHITECTURE
440
SLEEP,
POWER DOWN
CIRCUITRY
450
SLAVE POWER
MANAGER 274

FIG. 4

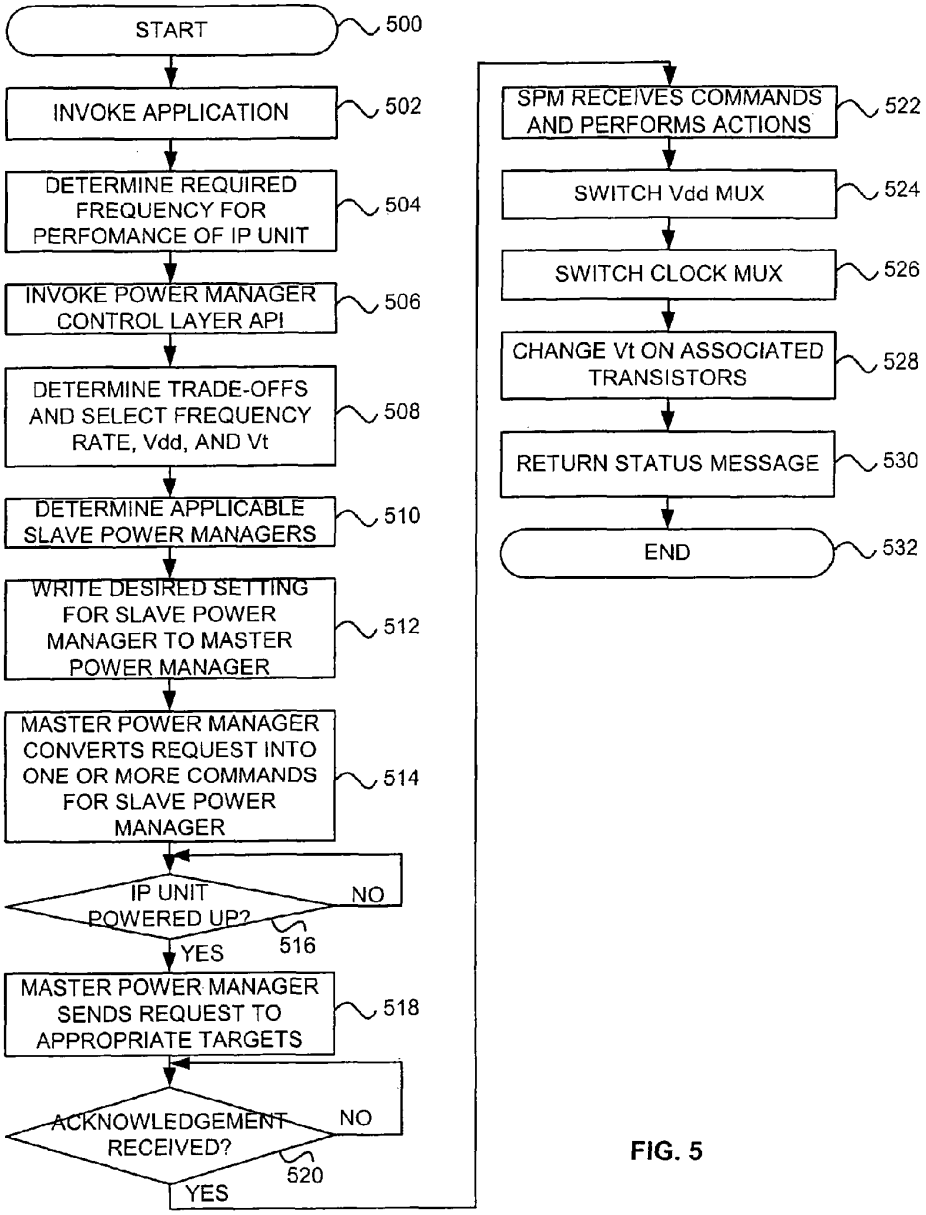

START
500
INVOKE APPLICATION
502
DETERMINE REQUIRED FREQUENCY FOR PERFOMANCE OF IP UNIT
504
INVOKE POWER MANAGER CONTROL LAYER API
506
DETERMINE TRADE-OFFS AND SELECT FREQUENCY RATE, Vdd, AND Vt
508
DETERMINE APPLICABLE SLAVE POWER MANAGERS
510
WRITE DESIRED SETTING FOR SLAVE POWER MANAGER TO MASTER POWER MANAGER
512
MASTER POWER MANAGER CONVERTS REQUEST INTO ONE OR MORE COMMANDS FOR SLAVE POWER MANAGER
514
IP UNIT POWERED UP?
NO
YES
516
MASTER POWER MANAGER SENDS REQUEST TO APPROPRIATE TARGETS
518
ACKNOWLEDGEMENT RECEIVED?
NO
YES
520
SPM RECEIVES COMMANDS AND PERFORMS ACTIONS
522
SWITCH Vdd MUX
524
SWITCH CLOCK MUX
526
CHANGE Vt ON ASSOCIATED TRANSISTORS
528
RETURN STATUS MESSAGE
530
END
532

FIG. 5

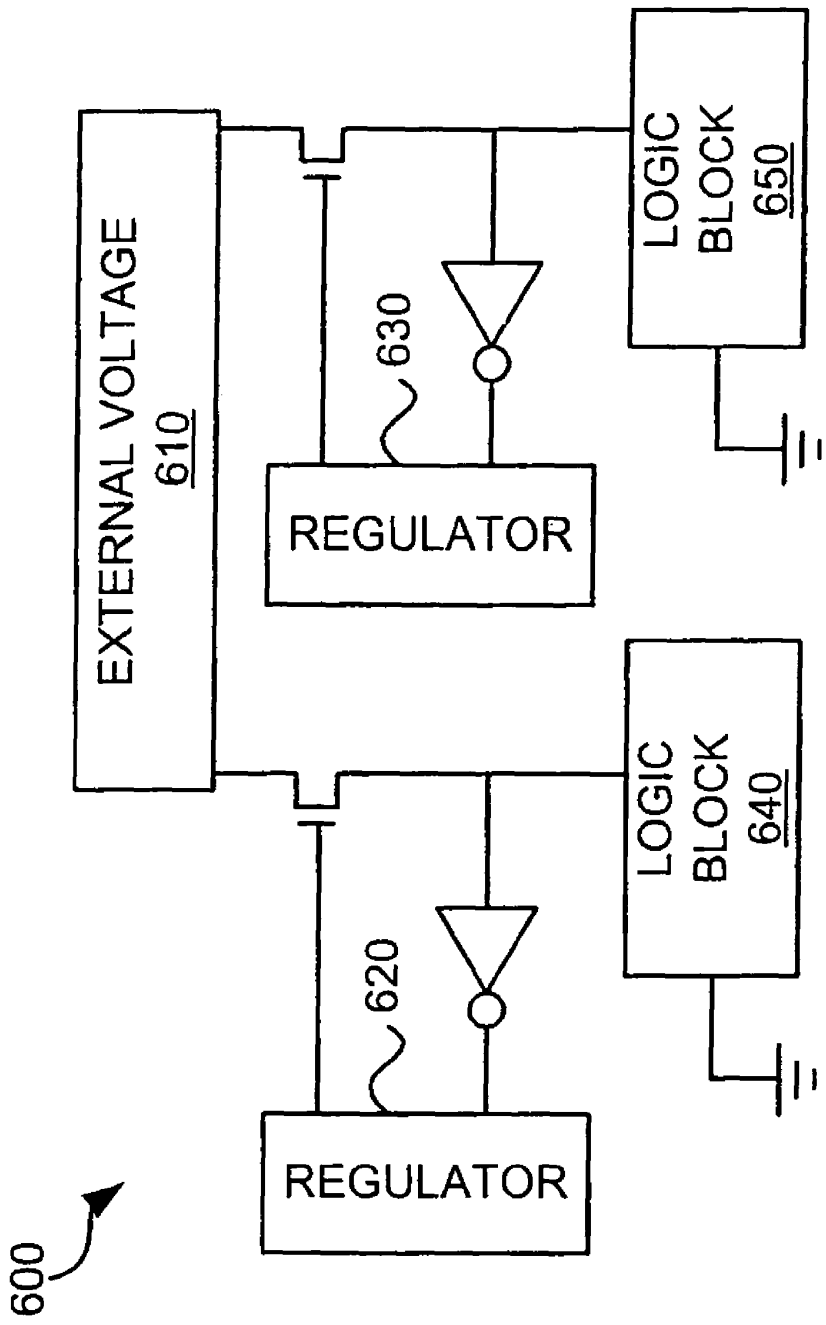

EXTERNAL VOLTAGE
610
630
REGULATOR
LOGIC
BLOCK
650
620
REGULATOR
LOGIC
BLOCK
640
600

FIG. 6

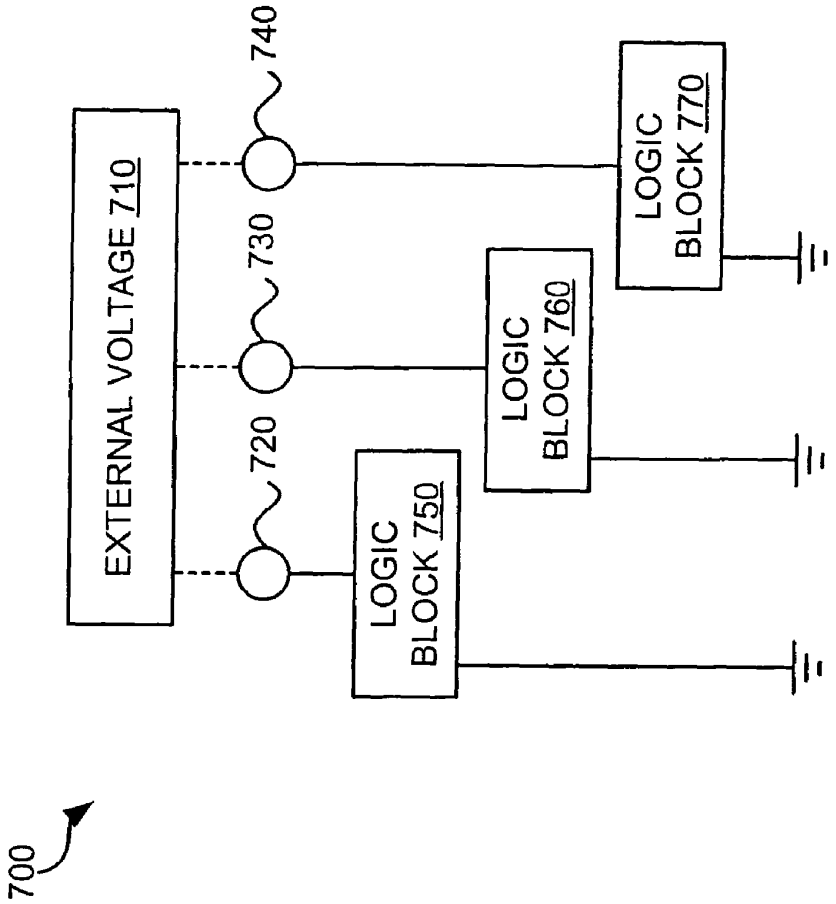

700
EXTERNAL VOLTAGE 710
720
730
740
LOGIC BLOCK 750
LOGIC BLOCK 760
LOGIC BLOCK 770

FIG. 7

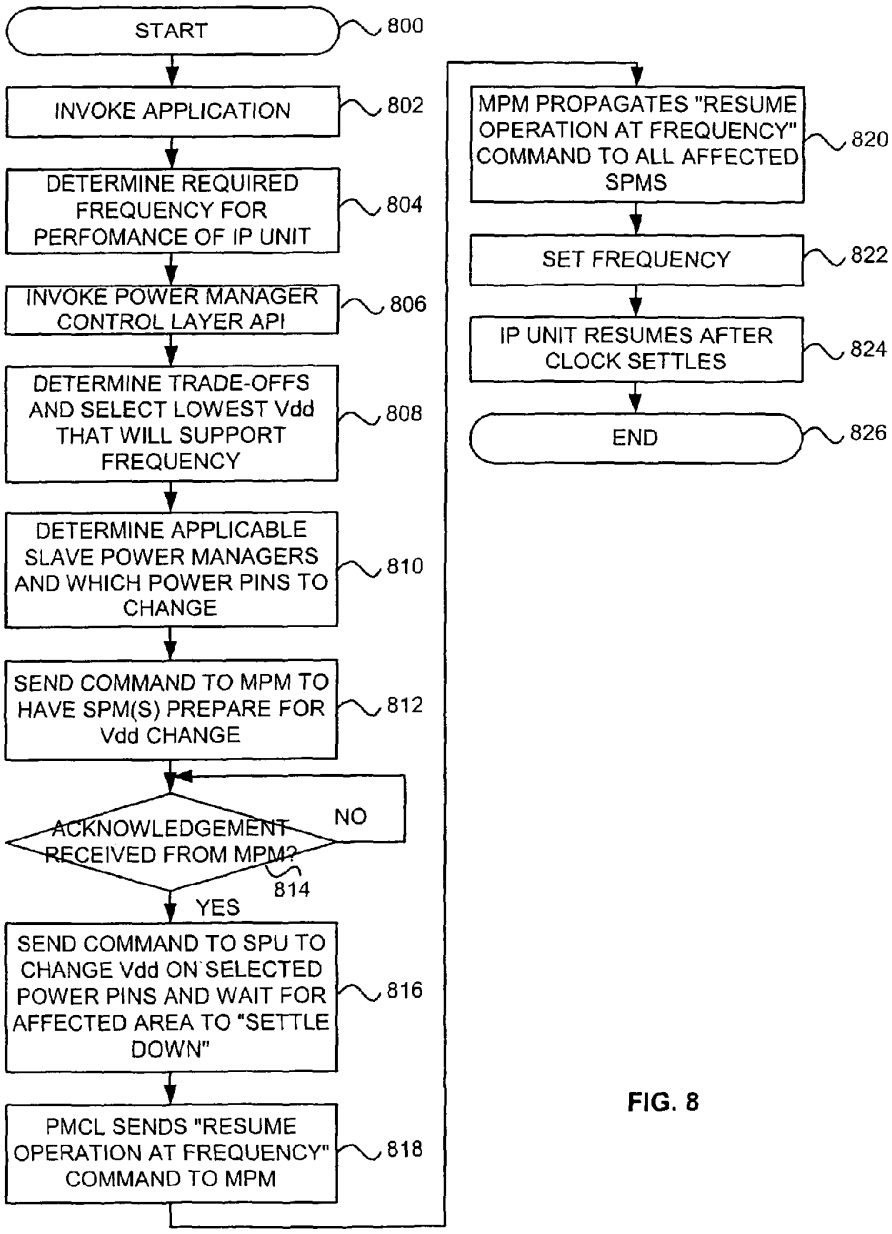

START
800
INVOKE APPLICATION
802
DETERMINE REQUIRED FREQUENCY FOR PERFOMANCE OF IP UNIT
804
INVOKE POWER MANAGER CONTROL LAYER API
806
DETERMINE TRADE-OFFS AND SELECT LOWEST Vdd THAT WILL SUPPORT FREQUENCY
808
DETERMINE APPLICABLE SLAVE POWER MANAGERS AND WHICH POWER PINS TO CHANGE
810
SEND COMMAND TO MPM TO HAVE SPM(S) PREPARE FOR Vdd CHANGE
812
ACKNOWLEDGEMENT RECEIVED FROM MPM?
814
NO
YES
SEND COMMAND TO SPU TO CHANGE Vdd ON SELECTED POWER PINS AND WAIT FOR AFFECTED AREA TO "SETTLE DOWN"
816
PMCL SENDS "RESUME OPERATION AT FREQUENCY" COMMAND TO MPM
818
MPM PROPAGATES "RESUME OPERATION AT FREQUENCY" COMMAND TO ALL AFFECTED SPMS
820
SET FREQUENCY
822
IP UNIT RESUMES AFTER CLOCK SETTLES
824
END
826

FIG. 8

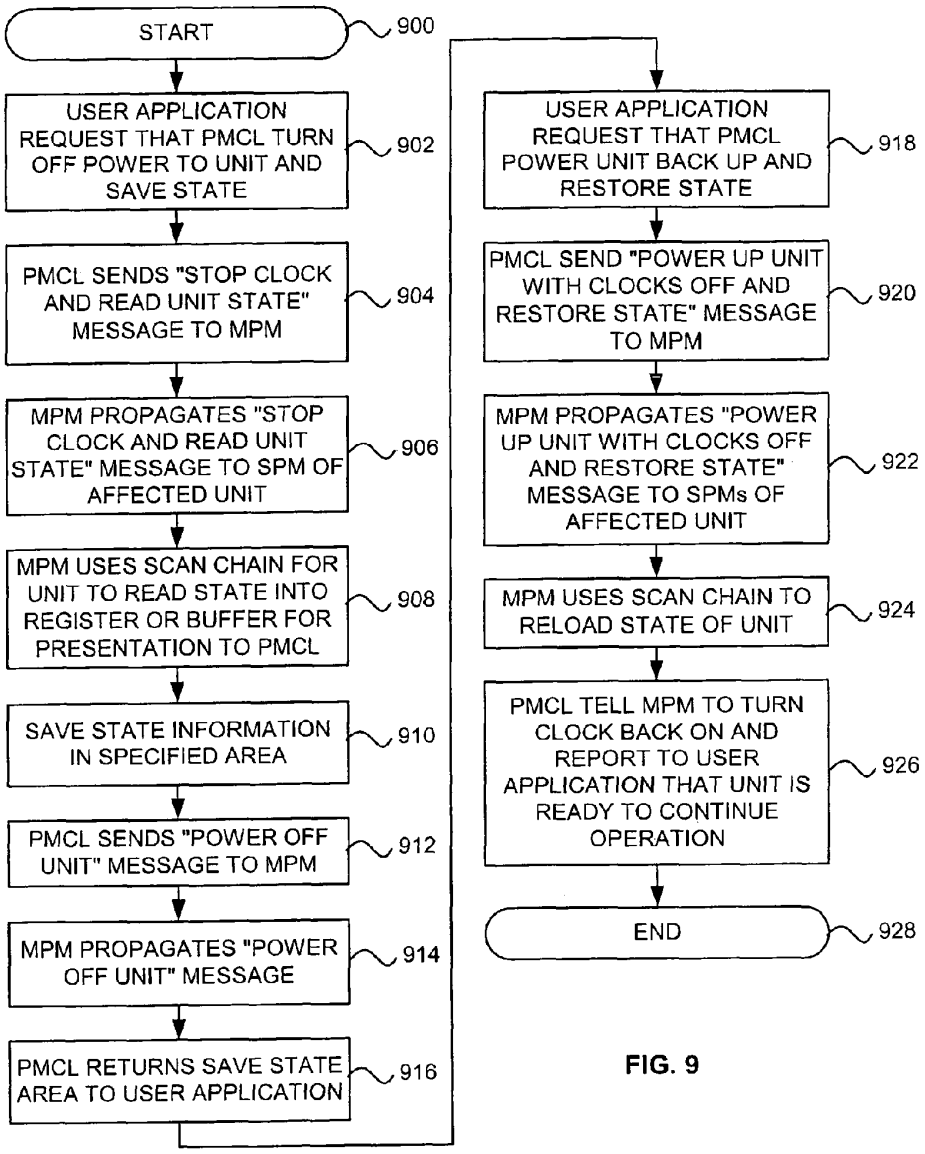

START
900
USER APPLICATION REQUEST THAT PMCL TURN OFF POWER TO UNIT AND SAVE STATE
902
PMCL SENDS "STOP CLOCK AND READ UNIT STATE" MESSAGE TO MPM
904
MPM PROPAGATES "STOP CLOCK AND READ UNIT STATE" MESSAGE TO SPM OF AFFECTED UNIT
906
MPM USES SCAN CHAIN FOR UNIT TO READ STATE INTO REGISTER OR BUFFER FOR PRESENTATION TO PMCL
908
SAVE STATE INFORMATION IN SPECIFIED AREA
910
PMCL SENDS "POWER OFF UNIT" MESSAGE TO MPM
912
MPM PROPAGATES "POWER OFF UNIT" MESSAGE
914
PMCL RETURNS SAVE STATE AREA TO USER APPLICATION
916
USER APPLICATION REQUEST THAT PMCL POWER UNIT BACK UP AND RESTORE STATE
918
PMCL SEND "POWER UP UNIT WITH CLOCKS OFF AND RESTORE STATE" MESSAGE TO MPM
920
MPM PROPAGATES "POWER UP UNIT WITH CLOCKS OFF AND RESTORE STATE" MESSAGE TO SPMs OF AFFECTED UNIT
922
MPM USES SCAN CHAIN TO RELOAD STATE OF UNIT
924
PMCL TELL MPM TO TURN CLOCK BACK ON AND REPORT TO USER APPLICATION THAT UNIT IS READY TO CONTINUE OPERATION
926
END
928

FIG. 9

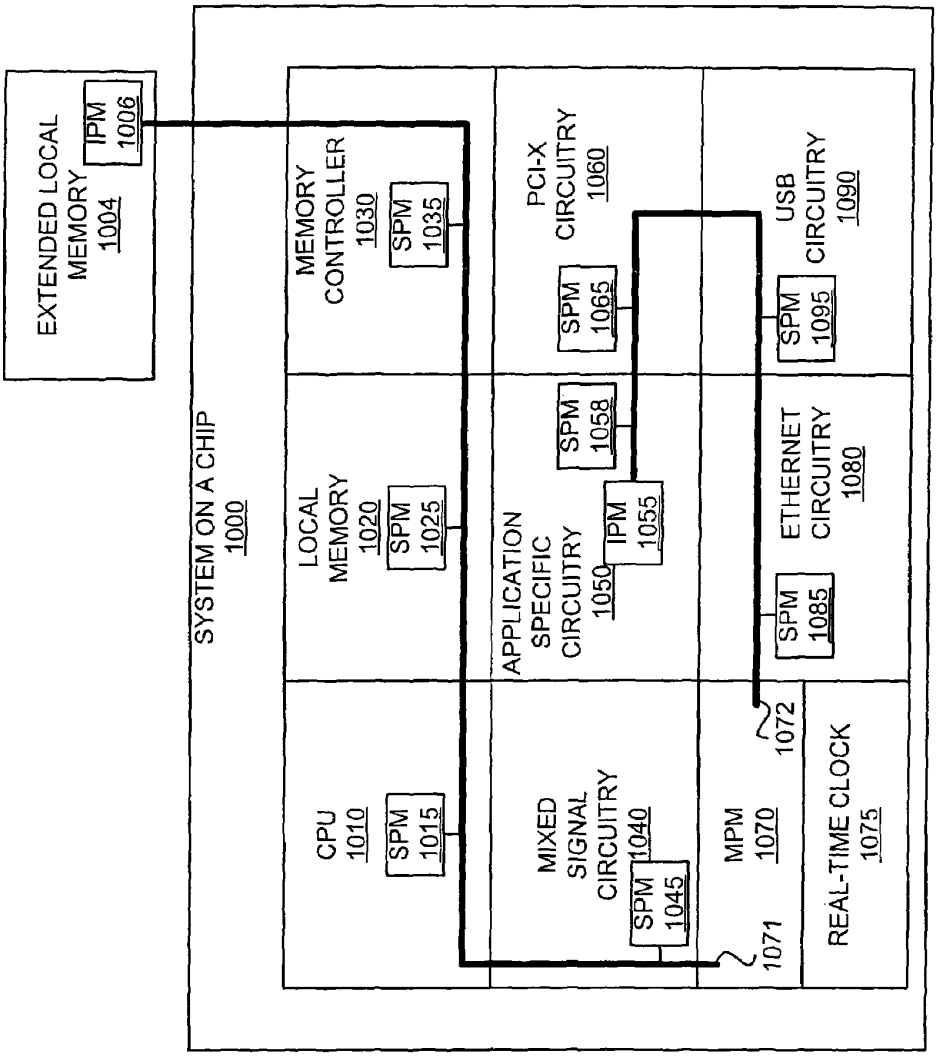

EXTENDED LOCAL MEMORY 1004
IPM 1006
SYSTEM ON A CHIP 1000
CPU 1010
SPM 1015
LOCAL MEMORY 1020
SPM 1025
MEMORY CONTROLLER 1030
SPM 1035
MIXED SIGNAL CIRCUITRY 1040
SPM 1045
APPLICATION SPECIFIC CIRCUITRY 1050
IPM 1055
SPM 1058
PCI-X CIRCUITRY 1060
SPM 1065
MPM 1070
1071
1072
SPM 1085
ETHERNET CIRCUITRY 1080
USB CIRCUITRY 1090
SPM 1095
REAL-TIME CLOCK 1075

FIG. 10

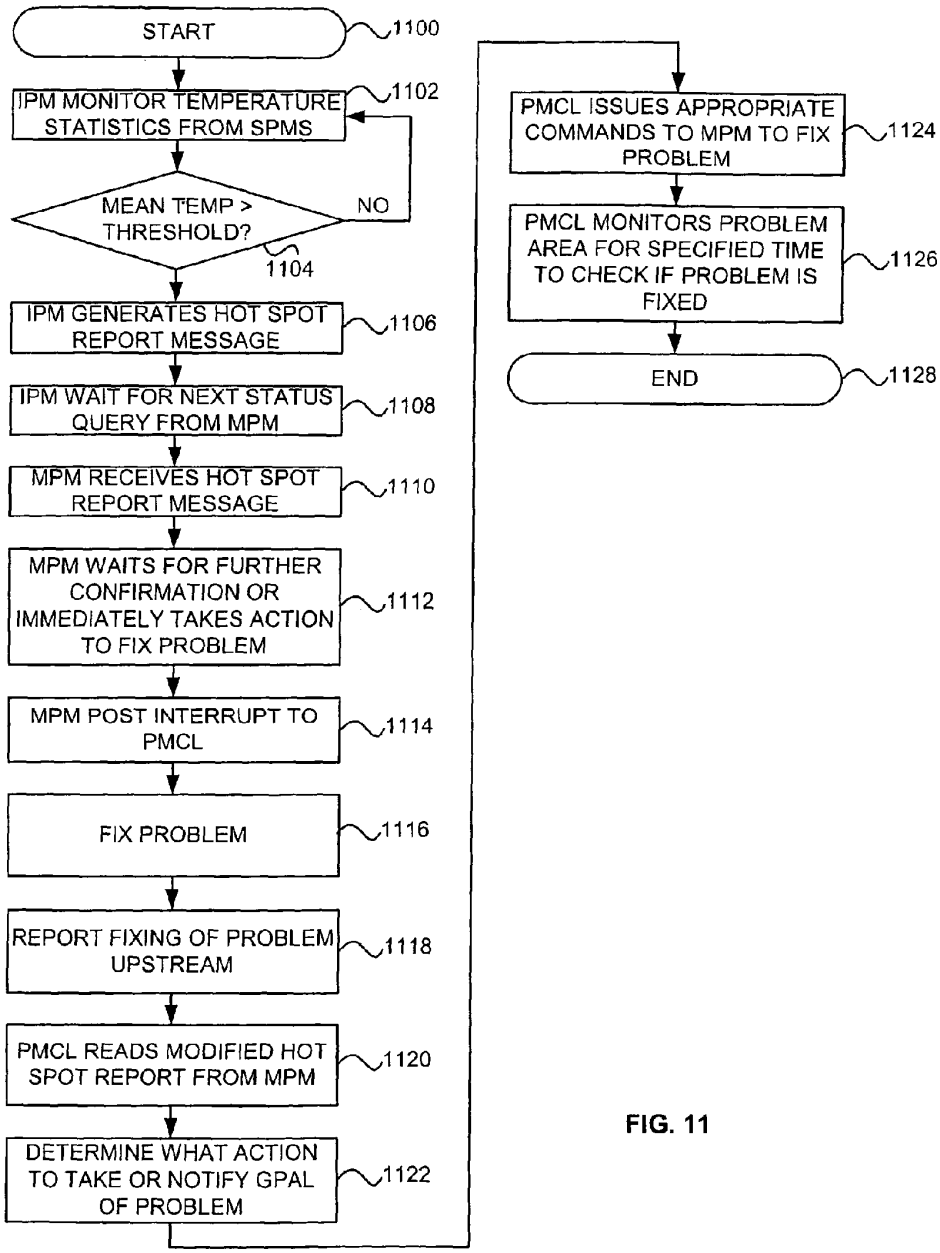

START
1100
IPM MONITOR TEMPERATURE STATISTICS FROM SPMS
1102
MEAN TEMP > THRESHOLD?
NO
1104
IPM GENERATES HOT SPOT REPORT MESSAGE
1106
IPM WAIT FOR NEXT STATUS QUERY FROM MPM
1108
MPM RECEIVES HOT SPOT REPORT MESSAGE
1110
MPM WAITS FOR FURTHER CONFIRMATION OR IMMEDIATELY TAKES ACTION TO FIX PROBLEM
1112
MPM POST INTERRUPT TO PMCL
1114
FIX PROBLEM
1116
REPORT FIXING OF PROBLEM UPSTREAM
1118
PMCL READS MODIFIED HOT SPOT REPORT FROM MPM
1120
DETERMINE WHAT ACTION TO TAKE OR NOTIFY GPAL OF PROBLEM
1122
PMCL ISSUES APPROPRIATE COMMANDS TO MPM TO FIX PROBLEM
1124
PMCL MONITORS PROBLEM AREA FOR SPECIFIED TIME TO CHECK IF PROBLEM IS FIXED
1126
END
1128

FIG. 11

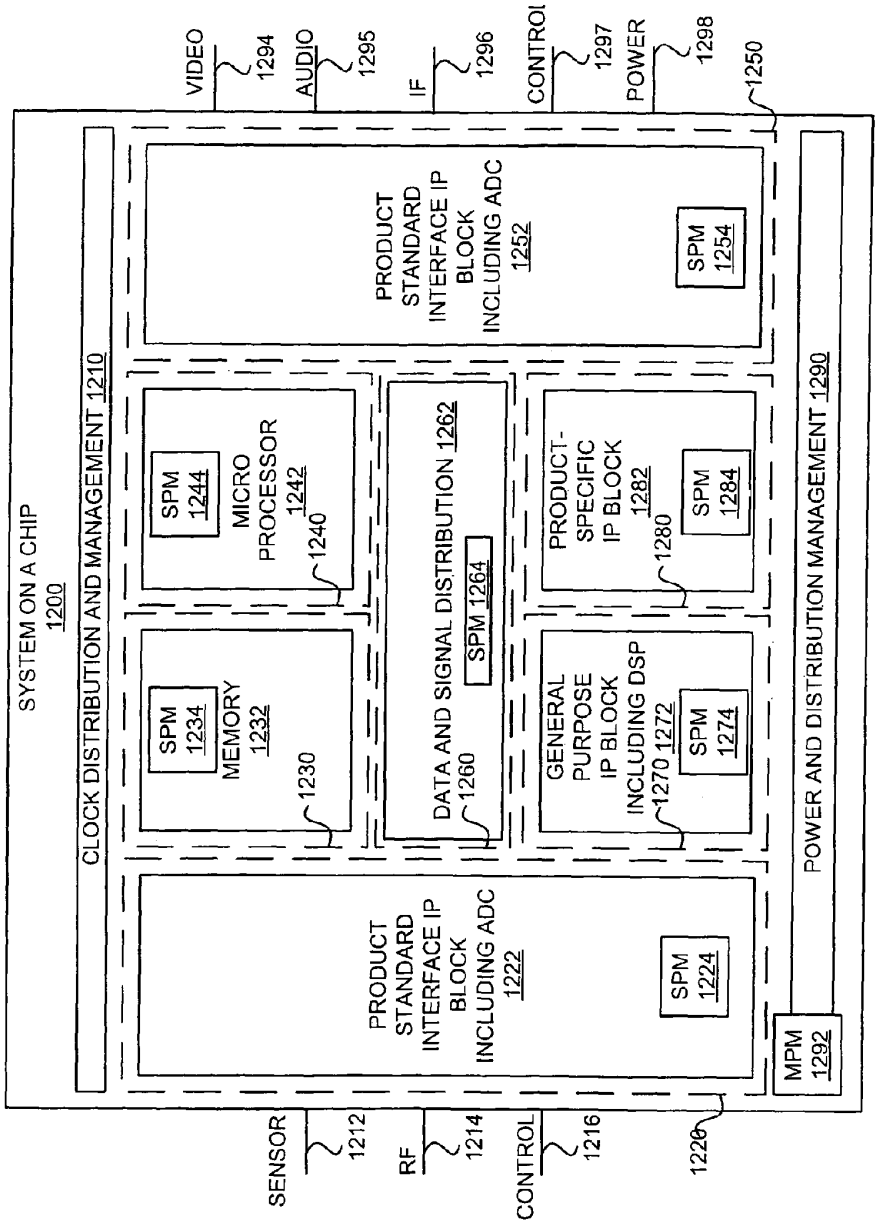

SYSTEM ON A CHIP
1200
CLOCK DISTRIBUTION AND MANAGEMENT 1210
SPM 1234
MEMORY 1232
1230
SPM 1244
MICRO PROCESSOR 1242
1240
DATA AND SIGNAL DISTRIBUTION 1262
1260
SPM 1264
GENERAL PURPOSE IP BLOCK INCLUDING DSP
1270 1272
SPM 1274
PRODUCT-SPECIFIC IP BLOCK 1282
1280
SPM 1284
PRODUCT STANDARD INTERFACE IP BLOCK INCLUDING ADC 1252
SPM 1254
PRODUCT STANDARD INTERFACE IP BLOCK INCLUDING ADC 1222
SPM 1224
POWER AND DISTRIBUTION MANAGEMENT 1290
MPM 1292
VIDEO 1294
AUDIO 1295
IF 1296
CONTROl 1297
POWER 1298
1250
SENSOR 1212
RF 1214
CONTROL 1216
1220

FIG. 12

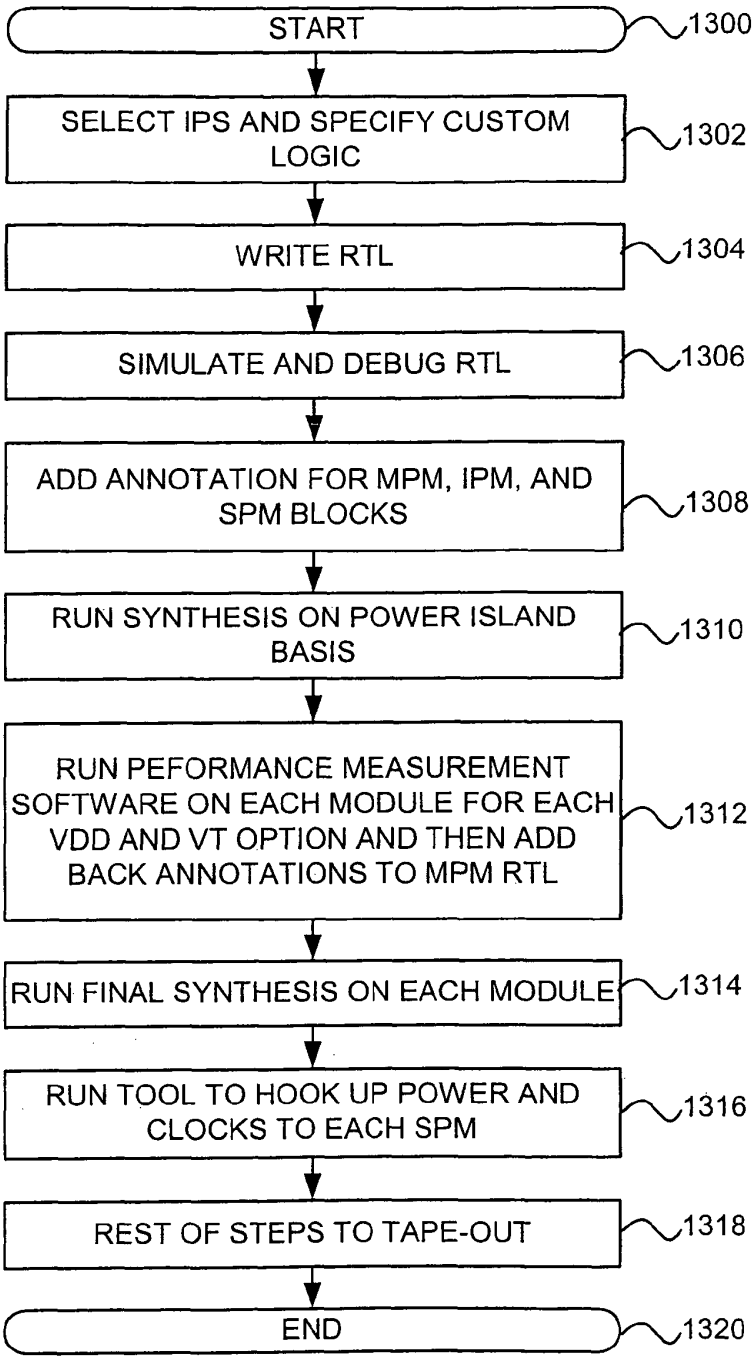

START
1300
SELECT IPS AND SPECIFY CUSTOM LOGIC
1302
WRITE RTL
1304
SIMULATE AND DEBUG RTL
1306
ADD ANNOTATION FOR MPM, IPM, AND SPM BLOCKS
1308
RUN SYNTHESIS ON POWER ISLAND BASIS
1310
RUN PEFORMANCE MEASUREMENT SOFTWARE ON EACH MODULE FOR EACH VDD AND VT OPTION AND THEN ADD BACK ANNOTATIONS TO MPM RTL
1312
RUN FINAL SYNTHESIS ON EACH MODULE
1314
RUN TOOL TO HOOK UP POWER AND CLOCKS TO EACH SPM
1316
REST OF STEPS TO TAPE-OUT
1318
END
1320

FIG. 13

POWER MANAGERS FOR AN INTEGRATED CIRCUIT

RELATED APPLICATIONS

This application is a divisional of U.S. application Ser. No. 13/164,362, filed Jun. 20, 2011, which is a continuation of U.S. application Ser. No. 12/332,529, filed Dec. 11, 2008, now U.S. Pat. No. 7,996,811, which is a continuation of U.S. application Ser. No. 12/176,645, filed Jul. 21, 2008, now U.S. Pat. No. 7,945,885, which is a continuation of U.S. application Ser. No. 11/336,097, filed Jan. 20, 2006, now U.S. Pat. No. 7,415,680, which is a continuation of U.S. application Ser. No. 10/840,893, filed May 7, 2004, now U.S. Pat. No. 7,051,306, which claims the benefit of U.S. Provisional Application No. 60/468,742, filed May 7, 2003.

The entire teachings of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to integrated circuits, and more particularly to managing power on integrated circuits using power islands.

2. Description of the Prior Art

One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heat dissipation of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

Some integrated circuits are designed using building blocks of library cells. These library cells are blocks of circuitry performing a function. Some examples of library cells are NAND gates, multiplexers, decoders, comparators, and memory.

In a "full-custom" flow, the integrated circuit is designed at the lowest level such as at the individual transistors, capacitors, and resistors level. The "full-custom" flow may use library cells that are internally developed. The integrated circuit can have optimal performance because the integrated circuit is designed in great detail at the lowest level. However, some problems with the "full-custom" flow are the long time and expensive costs associated with designing at such a detailed level. Furthermore, the "full-custom" flow is cumbersome because the design is at the lowest level.

In a "standard-cell" flow, the integrated circuit is designed using library cells acquired from a third party or other outside source. These library cells are standardized at the logic or function level. The design time for the standard-cell flow is reduced because the library cells are already pre-designed and pre-tested.

In one example for designing an integrated circuit, the library cells are selected, and the custom logic is specified to build the integrated circuit. The register transfer level (RTL) for the integrated circuit is then written for simulation and debugging. After simulation and debugging, the synthesis is run for the integrated circuit. Performance measurement software is executed to determine performance of the integrated circuit. The final synthesis of the integrated circuit can then be run based on the optimal performance of the integrated circuit.

One problem with many integrated circuits is that power consumption is not efficiently utilized. For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency. In another example, inactive circuitry within the integrated circuit consumes power and increases the likelihood of leakage. Inefficient power consumption may also adversely affect performance of the integrated circuit.

With the growing complexity of integrated circuits, the reduction of power consumption is even more important when the integrated circuit employs more functionality. One example of an integrated circuit is a system-on-a-chip that includes a microprocessor, memory, I/O interfaces, and an analog-to-digital converter all in a single chip. With many different types of functionality employed within a single chip, the system-on-a-chip consumes even more power than single function integrated circuits.

Some prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption. One problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static. The voltages and the frequencies do not dynamically change based on the needs and operation of the integrated circuit.

SUMMARY OF THE INVENTION

The invention addresses the above problems by providing power managers for an integrated circuit. A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

The first power manager may determine power trade offs between the power islands. The second power manager may determine status information about the one of the power islands and may transmit the status information to the first power manager. The first power manager may receive the status information and may manage the first power consumption for the integrated circuit using the status information. The first power manager may determine status information about the integrated circuit and may transmit the status information to power interface software. The first power manager may receive a message from power interface software to change the first power consumption for the integrated circuit. The first power manager may transmit a message to the second power manager and the second power manager may receive and process the message to change the second power consumption for the one of the power islands. The second power manager may register capabilities of the second power manager with the first power manager.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

FIG. **2** is a diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

FIG. **3** is an illustration for low leakage circuitry for a low power standard cell logic block in an exemplary implementation of the invention;

FIG. **4** is a diagram of a power island in an exemplary implementation of the invention;

FIG. **5** is a flowchart from an application request to a slave power manager action in an exemplary implementation of the invention;

FIG. **6** is an illustration of internal circuitry for a smart power unit in an exemplary implementation of the invention;

FIG. **7** is an illustration of external circuitry for a smart power unit in an exemplary implementation of the invention;

FIG. **8** is a flowchart from an application request to a smart power unit action in an exemplary implementation of the invention;

FIG. **9** is a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention;

FIG. **10** is diagram of a system on a chip and an extended local memory in an exemplary implementation of the invention;

FIG. **11** is a flowchart for generating a "hot spot" report from an intermediate power manager to a power management control layer in an exemplary implementation of the invention.

FIG. **12** is a diagram of a system on a chip in an exemplary implementation of the invention; and

FIG. **13** is a flowchart for building a chip with power islands in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

FIG. **1** depicts a block diagram of a system **100** for managing power in an integrated circuit **110** in an exemplary implementation of the invention. The system **100** includes an integrated circuit **110** and a power manager **120**. The integrated circuit **110** is any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit **110** is a system-on-a-chip. The integrated circuit **110** includes multiple IP units, which are blocks of circuitry performing specific functions.

The integrated circuit **110** includes four power islands **112**, **114**, **116**, and **118**. FIG. **1** only depicts four power islands **112**, **114**, **116**, and **118** for the sake of simplicity. Other embodiments of the integrated circuit **110** include a plurality of power islands **112**, **114**, **116**, and **118**. The power islands **112**, **114**, **116**, and **118** are coupled to a bus **125**.

A power island **112**, **114**, **116**, and **118** is any section, delineation, partition, or division of the integrated circuit **110** where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands **112**, **114**, **116**, and **118** are delineated based on geographic factors of the integrated circuit **110**. In some embodiments, the power islands **112**, **114**, **116**, and **118** are delineated based on functional IP units of the integrated circuit **110**. In one example depicted in FIG. **10**, power islands are delineated by memory, a microprocessor, and separate IP blocks. In some embodiments, the power islands **112**, **114**, **116**, and **118** are asynchronous or synchronous to each other. In some embodiments, the power islands **112**, **114**, **116**, and **118** comprise sub-islands of power to provide further specificity in controlling power in the integrated circuit **110**. In some embodiments, each of the power islands **112**, **114**, **116**, and **118** supports multiple clock domains with its own control. In some embodiments, the clocks within the power islands **112**, **114**, **116**, and **118** are variable.

In some embodiments, each of the power islands **112**, **114**, **116**, and **118** includes power control circuitry. Power control circuitry is any circuitry configured to control power within one of the power islands **112**, **114**, **116**, and **118**. Some examples of power control circuitry include circuitry for level shifting, signal isolation, Vdd multiplexing, clock multiplexing, and dynamic back bias. In some embodiments, the power control circuitry is included in a standard cell library for standard cell design of the integrated circuit **110**.

The power manager **120** is also coupled to the bus **125**. One example of the bus **125** is a power command bus described in further detail below in FIG. **10**. Other embodiments of the system **100** include numerous variations in which the power manager **120** and the power islands **112**, **114**, **116**, and **118** are interconnected. The power manager **120** is any circuitry, device, or system configured to (1) determine a target power level for one of the power islands **112**, **114**, **116**, and **118** where power consumption is independently controlled within each of the power islands **112**, **114**, **116**, and **118**, (2) determine action to change a consumption power level of the one of the power islands **112**, **114**, **116**, and **118** to the target power level, and (3) perform the action to change the consumption power level of the one of the power islands **112**, **114**, **116**, and **118** to the target power level. The power manager **120** can dynamically change the power consumption of the power islands **112**, **114**, **116**, and **118** based on the needs and operation of the integrated circuit **110**. The target power level is a desired, calculated, or specified power consumption of the power islands **112**, **114**, **116**, and **118**. Some examples of the power manager **120** are the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM), which are described in further detail below. The power manager **120** may be a hierarchy or group of power managers **120**. Although FIG. **1** depicts the power manager **120** as being located outside the integrated circuit **110**, other embodiments may have the power manager **120** located in the integrated circuit **110**. In other embodiments, the power manager **120** may be distributed among multiple power managers that are on or off the integrated circuit **110** or integrated with a CPU. The action is any instruction, message, process, function, signal, or variable that controls power consumption in the power island **112**, **114**, **116**, and **118**. Some examples of actions are clock gating and dynamic clock selection. Another example of an action is modifying a clock frequency of one of the power islands **112**, **114**, **116**, and **118**. Another example of an action is to modify voltage of one of the power islands **112**, **114**, **116**, and **118** such as dynamic voltage source, Vdd, selection. Another example of an action is to control dynamic leakage by controlling variable Vt transistors.

FIG. **2** depicts a diagram of a system **200** for managing power in an integrated circuit **250** in an exemplary implementation of the invention. The system **200** includes an embedded firmware stack **210** and an integrated circuit **250**. The embedded firmware stack **210** includes software layers that run on a central processing unit (CPU). In some embodiments, the embedded firmware stack **210** may include an application layer **212**, an operating system (OS) sub-system **216**, a power management control layer (PMCL) **218**, a real-time operating

system (RTOS) **220**, I/O drivers **222**, and power manager (PM) firmware **224** for the MPM, IPM and/or SPM.

The integrated circuit **250** includes a power island **260**, a power island **270**, and a MPM **280**. The power island **260** includes a low power standard cell logic block **262** and a SPM **264**. The power island **270** includes a low power memory block **272** and a SPM **274**. The low power standard cell logic block **262** and the low power memory block are coupled to an interface **265**. The MPM **280** is coupled to the PMCL **218**, the SPM **264**, and the SPM **274**.

In some embodiments, the application layer **212** includes a global power application layer (GPAL) **214**. This GPAL **214** may be useful for more complex applications. If the GPAL **214** is present, then all calls to the PMCL **218** application program interfaces (API) are first directed to the GPAL **214**. Both the GPAL **214** and the PMCL **218** provide power management for the integrated circuit **250**. In some embodiments, the GPAL **214** and/or the PMCL **218** monitor what load is on each power island **260** and **270**. Also, the GPAL **214** and/or the PMCL **218** may build a history of power levels on the power island **260** and **270** and store the history data in a database. The GPAL **214** and the PMCL **218** may also provide data for on-demand resources interested in the power levels of the power islands **260** and **270**.

In some embodiments when the GPAL **214** is present, the GPAL **214** provides guidance to the PMCL **218** in making local decisions for power management of the integrated circuit **250**. In some embodiments, the GPAL **214** and the PMCL **218** include complex algorithms for a static schedule. The GPAL **214** and the PMCL **218** provide the facility for use code to interact and control power behavior and parameters including providing a database and statistics.

The PMCL **218** also collects information from the MPM **280** and provides commands to the MPM **280** for possible IPMs, SPMs **264** and **274**, and the power islands **260** and **270**. Some of the commands may be to power on/off, change the power level, or change the frequency of the power islands **260** and **270**. In some embodiments with a smart power unit (SPU) **290**, the GPAL **214** and the PMCL **218** are responsible for communication with the SPU **290** to implement a power policy and collect information on the actual power supply. The SPU **290** is described in further detail below in FIGS. **6-8**. In some embodiments, the GPAL **214** and the PMCL **218** provides sockets for existing power management techniques.

The power manager firmware **224** is firmware executed by the master power manager **280**, the intermediate power manager, and the slave power managers **264** and **274**.

The MPM **280** is any circuitry configured to control the "global" power behavior of the entire integrated circuit **250**. In some embodiments, there are multiple MPMs **280** that control the power behavior of the entire integrated circuit **250**. In some embodiments, the MPM **280** communicates with existing IPMs and SPMs **264** and **274** to control power within the power islands **260** and **270**. The MPM **280** may receive status information about the power islands **260** and **270** from the SPMs **264** and **274** and the IPMs. The MPM **280** may also determine power trade-offs between the IPMs and the SPMs **264** and **274**.

The MPM **280** may also provide a main interface to the PMCL **218** firmware. In some embodiments, the MPM **280** communicates with the PMCL **218** to accept commands (e.g., memory mapped commands) and provide status information, about the power within the integrated circuit **250**. In some embodiments, the MPM **280** communicates with the PMCL **218** through the main bus for the integrated circuit **250**. The MPM **280** may also register each of the SPMs **264** and **274** and IPMs and capabilities with the PMCL **218**. Some operations of the MPM **280** are described in further detail below in FIGS. **5**, **8**, **9**, and **11**. In some embodiments, the MPM **280** reads and writes scan chains for state save and restore along with the local logic analyzer ability.

Some embodiments may include an IPM (not shown) that coordinates SPMs **264** and **274** on behalf of the MPM **280**. In some embodiments, the IPM controls and coordinates power behavior on portions of the area controlled by the MPM **280**. In some embodiments, the IPM controls the SPMs **264** and **274** that are on a separate chip from the MPM **280**.

The SPM **264** is any circuitry configured to control power within a power island **264** in the integrated circuit **250**. One example of the SPM **264** is an IP block that controls power within a power island **264** in the integrated circuit **250**. The SPM **264** may include signal buffering, level shifting, and signal isolation. In some embodiments, the SPM **264** is integrated into scan chains to provide easier implementation and integration. Also, in some embodiments, the SPM **264** has a very small "footprint" with a low gate count and low power. In some embodiments, the SPM **264** comprises a command interface to communicate status information, service requests, and commands. Some of the commands are load, sleep, and idle. The SPM **264** may also recognize its own address to allow for multi-drop bussing.

In some embodiments, the SPM **264** has registration capabilities. For registration at power-up, the SPM **264** uses callback registration that is typically used for off chip SPMs and IPMs. For static registration when the integrated circuit is generated for on chip SPMs, the SPM **264** registers what the SPM **264** can do, what the IPM can do, and the type of commands that the SPM **264** or IPM can service. The SPM **264** may also have save and restore functions for power off periods. The SPM **264** may have watch-dog timer(s). In some embodiments, the SPM **264** has a debug interface coordination to the power island **260**. The SPM **264** may also monitor local state and collect information for components within the power island **260**. The SPM **264** may also locally control Vdd, clocks for frequency selection, and dynamic back biasing. The description for the SPM **264** also applies to the SPM **274** for the power island **270**.

In some embodiments, the SPM **264** checks whether an event occurs when the collected information from the power island **260** crosses a threshold or exceeds a range. In some embodiments, the SPM **264**, IPMs, or the MPM **280** monitors power consumption levels of the power island **260** to check whether the power consumption levels cross a threshold level or exceed a range. A power consumption level is any information, data, or statistic that indicate the power consumed in a power island **260**. Some examples of power consumption levels are temperature and power. The threshold or range may be programmable. The SPM **264** may report the event asynchronously, or another element such as the MPM **280** may solicit whether an event has occurred. The event may also be a multi-level test such as the conditions occur at a greater than a given, programmable frequency or exceed a given, programmable duration.

In some embodiments, the low power standard cell logic block **262** one example of a standard cell library that may be included in the power island **260**. In some embodiments, the standard cell library is optimized for lower power. The standard cell library may be characterized over a range of operating voltages. In some embodiments, the standard cell library includes synchronous circuits and/or asynchronous circuits. In some embodiments, the standard cell library includes static circuits and/or encapsulated, dynamic logic circuits. The standard cell library may also include multiple voltage domain interface circuits such as level shifters and

signal isolation circuits. The standard cell library may also have a multi-threshold design and characterization such as standard Vt, high Vt, low Vt, and variable Vt circuits. The standard cell library may also include data retention (shadow) circuits and anti-glitch circuits. The standard cell library may also include low leakage "sleep" circuits. FIG. **3** depicts an illustration of low leakage circuitry **300** for the low power standard cell logic block **262** in an exemplary implementation of the invention.

FIG. **4** depicts a diagram of the power island **270** in an exemplary implementation of the invention. The power island **270** includes a low power memory block **272** and the SPM **274**. The low power memory block **272** includes banked architectures **410**, **420**, **430**, and **440** for memories and sleep, power down circuitry **450**. In some embodiments, the memory in the power island **270** is RAM and/or ROM. Some examples of the RAM are the SRAM compilers such as single-port, 2-port, and dual-port. Some examples of the ROM are ROM compilers. Some memories in the power island **270** are optimized for low power such as the low power memory block **272**. In one embodiment, the low power memory block **272** includes multiple bank architectures via the compiler such as banked architectures **410**, **420**, **430**, and **440**. The memories in the power island **270** may also include sleep, power down circuitry **450** for low power modes such as sleep, nap, and full power down. The memories in the power island **270** may also include programmable read/write ports. The memories in the power island **270** may also be an asynchronous and/or synchronous design.

In some embodiments, the system **200** also includes a smart power unit (SPU) **290**. In some embodiments, the SPU **290** is off-chip to the integrated circuit **250**. The SPU **290** is an external unit configured to control power and clock distribution to the integrated circuit. The circuitry of the SPU is described in further detail below in FIGS. **7** and **8**.

FIG. **5** depicts a flowchart from an application request to an SPM action in an exemplary implementation of the invention. FIG. **5** begins in step **500**. In step **502**, an application is invoked such as playing a movie. In step **504**, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder. In some embodiments, when the IP unit is totally asynchronous, the required frequency will be an artificial measure of performance. In some embodiments that have multiple clocks involved, the minimum performance for each clock is specified.

In step **506**, the application invokes the PMCL **218** API call. One example of this call is "Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag)." In this example, the other information could be "no power off, use high Vt and clocks off instead" and "major waits are about 10 us, with a 400 ns threshold." In some embodiments with multiple clocks, the PMCL **218** API call allows the application to specify all required frequencies.

The PMCL **218** determines possible trade-offs available for the unit and selects a frequency rate, Vdd, and Vt if applicable for the unit that best meets the given requirements in step **508** and determines the applicable SPMs **264** and **274** in step **510**. In some embodiments, the MPM **280** or IPM performs steps **508** and **510**. In some embodiments for multiple clocks, the Vdd and Vt specified would allow for all specified clocks to meet or exceed their required frequencies.

In step **512**, the PMCL **218** then writes the desired setting for the SPMs **264** and **274** to the MPM **280** (or IPM). In step **514**, the MPM **280** (or IPM) converts the request into one or more commands for the SPMs **264** and **274** (or IPM) associated with the unit.

In step **516**, if the application sets the wait for power up flag, the PMCL **218** then waits until the IP unit is fully powered up before returning from the call. Otherwise, the call returns as soon as the command is acknowledged, with status of 0 for okay, 1 for fast power-up, 2 for slow power-up, or 3+ for error conditions. The powered up state is when the unit is at the desired Vdd for the requested frequency, and not just that the unit is turned on.

In step **518**, the MPM **280** (or IPM) sends the requests to the appropriate targets. In step **520**, the MPM **280** waits for the receipt of the acknowledgements that indicate message received and executed or execution has begun. A NACK or negative acknowledgement may also be returned from the SPM **264** and **274**.

In step **522**, the SPM **264** receives the commands and performs the actions. Steps **524**-**528** are possible actions that the SPM **264** may perform. In step **524**, the SPM **264** switches the Vdd mux. In step **526**, the SPM **264** switches a clock mux. In some embodiments when the voltage goes down, step **526** is performed before step **524**. In step **528**, the SPM **264** changes the Vt on the associated transistors. After the SPM **264** performs the actions, the SPM **264** returns a status message upstream indicating acknowledgement or negative acknowledgement in step **530**. FIG. **5** ends in step **532**.

FIG. **6** depicts an illustration of internal circuitry **600** for an SPU **290** in an exemplary implementation of the invention. In this embodiment, the internal circuitry **600** for the SPU **290** is internal to the integrated circuit **250** of FIG. **2**. The internal circuitry **600** includes an external voltage **610**, a dropout voltage regulator **620**, a dropout voltage regulator **630**, a logic block **640**, and a logic block **650**.

FIG. **7** depicts an illustration of external circuitry **700** for an SPU **290** in an exemplary implementation of the invention. In this embodiment, the external circuitry **700** for the SPU **290** is external to the integrated circuit **250** of FIG. **2**. The internal circuitry **700** includes an external voltage **710**, a power supply pin **720**, a power supply pin **730**, a power supply pin **740**, a logic block **750**, a logic block **760**, and a logic block **770**. The external circuitry **700** for the SPU **290** provides a DC/DC conversion. The DC/DC conversion provides multiple independent power supply pins **720**, **730**, and **740**. The power supply pins **720**, **730**, and **740** have a variable voltage supply on each separate power pin. Also, in some embodiments, the variable voltage is within a range and in steps. In some embodiments, the PMCL **218** controls the voltage to power supply pins **720**, **730**, and **740**.

FIG. **8** depicts a flowchart from an application request to an SPU action in an exemplary implementation of the invention. FIG. **8** begins in step **800**. In step **802**, an application is invoked. In step **804**, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder.

In step **806**, the application invokes the PMCL **218** API call. One example of this call is "Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag)." In this example, the other information could be "no power off, use high Vt and clocks off instead" and "major waits are about 10 us, with a 400 ns threshold."

The PMCL **218** determines possible trade-offs available for the unit and selects a the lowest possible Vdd that will

support the requested frequency in step **808** and determines the SPMs **264** and **274** that will be affected and which power PINs to change in step **810**.

In step **812**, the PMCL **218** sends a command to the MPM **280** to have the SPMs **264** and **274** (and IPM) to prepare for a Vdd change. In step **814**, the PMCL **218** waits for the acknowledgement from the MPM **280**. In step **816**, the PMCL **218** sends a command to the SPU **290** to change the Vdd on the selected power pins and waits for the affected area to "settle down." In step **818**, the PMCL **218** then sends a "resume operation at a specified frequency" command to the MPM **280**. In step **820**, the MPM **280** propagates the resume command to all affected SPMs **264** and **274** (and IPMs). In step **822**, one of the power managers (i.e. MPM **280**, IPM, or SPMs **264** and **274**) sets the specified frequency. In step **824**, the IP unit operation resumes after the clock has settled. FIG. **8** ends in step **826**. In some embodiments, the user application has the option of waiting for the entire operation to finish or to continue and either query the PMCL **218** as to the progress of the operation or wait for a "finished" interrupt from the PMCL **218**.

FIG. **9** depicts a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention. FIG. **9** begins in step **900**. In step **902**, the user application requests that the PMCL **218** power off an IP unit and wants to save the IP unit's state. In some embodiments, the reconfiguration of the IP unit takes a long time. The request in step **902** may be accompanied by the address of an area to which the state should be saved.

In step **904**, the PMCL **218** sends a "stop clock and read IP unit state" message to the MPM **280**. The MPM **280** then propagates the "stop clock and read IP unit state" message to the SPMs **264** and **274** of the affected unit in step **906**. In step **908**, the MPM **280** uses the scan chain for the IP unit to read the state into a register or buffer for presentation to the PMCL **218**. In step **910**, if the PMCL **218** provided the MPM **280** with the address of the save area, the MPM **280** saves the state information directly in the specified area. In step **912**, after all of the IP units' state has been saved, the PMCL **218** sends a "power off IP unit" message to the MPM **280**. In step **914**, the MPM **280** then propagates out the "power off IP unit" message. In step **916**, the PMCL **218** returns the save state area to the user application. The save state area contains the state of the unit.

At a later time, in step **918**, the user application requests that the PMCL **218** power the IP unit-back up and restore the state of the IP unit. In some embodiments, the user application request includes the address of the area to which the state was saved. In step **920**, the PMCL **218** sends a "power up IP unit with clocks off and restore state" message to the MPM **280**. In step **922**, the MPM **280** propagates the "power up IP unit with clocks off and restore state" message to the SPMs **264** and **274** of the affected IP unit. In step **924**, after the IP unit is powered up, the MPM **280** uses the scan chain to reload the unit's state. In some embodiments, the reloading of the unit's state originates directly from the save area or from information passed to the MPM **280** from the PMCL **218**. In step **926**, the PMCL **218** sends a message to the MPM **280** to turn clock back on and report to user application that the IP unit is ready to continue operations. FIG. **9** ends in step **928**.

In some embodiments, the same functionality of FIG. **9** can be used to implement an internal "logic analyzer" function, in which the IP unit in question would not be powered down after being read. If the associated SPMs **264** and **274** of the IP unit have the ability to single- or multi-step the clock, the local scan testing is performed by having the SPMs **264** and **274** "signal isolate" the IP unit. Then, use of a combination of the ability of single- or multi-step the clock and the ability to use the scan chain can read/write the IP unit's internal state.

FIG. **10** depicts a diagram of a system-on-a-chip (SOC) **1000** and an extended local memory **1004** in an exemplary implementation of the invention. The SOC **1000** is one example of the integrated circuit **250** and communicates with the embedded firmware stack **210** in FIG. **2** as described above. The SOC **1000** includes a CPU **1010**, a local memory **1020**, a memory controller **1030**, a mixed signal circuitry **1040**, an application specific circuitry **1050**, a PCI-X circuitry **1060**, a MPM **1070**, a real-time clock (RTC) **1075**, an Ethernet circuitry **1080**, and a USB circuitry **1090**. The CPU **1010**, the local memory **1020**, the memory controller **1030**, the mixed signal circuitry **1040**, the application specific circuitry **1050**, the PCI-X circuitry **1060**, the Ethernet circuitry **1080**, and the USB circuitry **1090** are all power islands in which power is controlled within the power islands by power managers. In this embodiment, the power islands are delineated by the functionality of a part of the SOC **1000**.

The extended local memory **1004** includes an IPM **1006** that is coupled to the bus **1071**. The CPU **1010** includes an SPM **1015** that is coupled to the bus **1071**. The local memory **1020** includes an SPM **1025** that is also coupled to the bus **1071**. The memory controller **1030** comprises an SPM **1035** that is coupled to the bus **1071**. The mixed signal circuitry **1040** includes an SPM **1045** that is coupled to the bus **1071**. The application specific circuitry **1050** includes an IPM **1055** and an SPM **1058** that are both coupled to the bus **1072**. The PCI-X circuitry **1060** includes an SPM **1065** that is coupled to the bus **1072**. The MPM **1070** is coupled to the bus **1071** and the bus **1072**. The MPM **1070** is one example of the MPM **280** as described above. The Ethernet circuitry **1080** includes an SPM **1085** that is coupled to the bus **1072**. The USB circuitry **1090** includes an SPM **1095** that is coupled to the bus **1072**.

In this embodiment, power command buses comprise the bus **1071** and the bus **1072**. The bus **1071** and **1072** are simple multi-drop serial buses that may cross chip boundaries and interconnect power managers. The power command bus may be a combination of serial busses, such as the bus **1071** and the bus **1072**, with one per region of the chip and then multi-drop within the region. In other embodiments, the power command bus includes a parallel bus or a combination of serial and parallel busses. In some embodiments, the power command bus is the system bus. The power command bus may contain messages with at least a unit ID with the associated payload. For a fixed point to point bus, the message does not need a unit ID only the payload.

In some embodiments, the power command bus uses an error detection scheme such as parity, ECC, or a redundant code. In some embodiments, the power command bus is a low performance bus that does not interfere with the integrated circuit design and is not visible to the user. In some embodiments, the communication between the PMCL **218** and the MPM **1070** is memory mapped and based on the main bus such as an AHB for an SOC **1000**.

Some embodiments may include a separate bus for reporting status information between the power managers. In one example, this separate bus provides asynchronous "Alert" type status messages from SPMs to the MPM.

There can be various message formats for the power command bus. In one example for a basic format, the message format includes a start of message indicator, a power manager address, type code, basic command, and an end of message indicator. In one example for an extended format, the message format includes the basic format, an additional length, and additional information. In one example for a response mes-

sage format, the message format includes a start of message reply indictor, a power manager address, a 3b ACK or NAK or return status (implied ACK), a payload length for return status messages, a payload for return status messages, a reason code for NAK, and an end of message indicator.

In some embodiments, the SPM **1015** or the IPM **1006** times out on replying to a command, and the MPM **1070** reissues the command a programmable number of times. If the SPM **1015** or the IPM **1006** still fails, the MPM **1070** marks the SPM **1015** or the IPM **1006** as unusable and reports back the failure to the PMCL **218**. In one embodiment, the PMCL **218** has the MPM **1070** reinitialize the failing SPM **1015** or the IPM **1006** via the scan system and then retries sending the message. Other conditions such as invalid responses to commands or invalid status reports are also handled by the re-initialization. In some embodiments, the state of the failing SPM **1015** or the IPM **1006** may be read out and saved for later analysis.

FIG. **11** depicts a flowchart for generating a "hot spot" report from an IPM **1055** to the PMCL **218** in an exemplary implementation of the invention. FIG. **11** begins in step **1100**. In step **1102**, the IPM **1055** monitors the temperature statistics of the SPMs. In step **1104**, the IPM **1055** checks whether the mean temperature has exceeded a predetermined and programmed threshold. If the mean temperature has not exceeded the threshold, the IPM **1055** returns to step **1102** to keep monitoring. If the mean temperature has exceeded the threshold, the IPM **1055** then generates a problem ("hot spot") report message in step **1106**. In step **1108**, the IPM **1055** waits for the next status query the MPM **1070**. In some embodiments, a logically separate bus is provided for asynchronous status reports to the MPM **280**.

In step **1110**, the MPM **1070** receives the hot spot report message. In step **1112**, the MPM **1070** either waits for further confirmation (i.e. see that the "hot spot" last pasts a predetermined threshold) or immediately takes action to fix the problem depending on the internal logic of the MPM **1070**. In some embodiments, in step **1114**, the MPM **1070** takes action by posting an interrupt to the PMCL **280** that it needs attention. In other embodiments, if the PMCL **280** queries the MPM **1070** often enough, then the interrupt is not needed. In step **1116**, the MPM **1070** (or IPM) fixes the problem by making a local trade-off, performing the action, or ordering the action to be performed. One example of fixing the problem is lowering the operating frequency of the hot spot area. In step **1118**, the MPM **1070** reports both the problem and the fixing of the problem upstream.

In step **1120**, the PMCL **218** reads the modified hot spot report from the MPM **1070**. In step **1122**, the PMCL **218** determines what action to take to fix the problem or notify the GPAL **214** of the problem. In step **1124**, the PMCL **218** issues the appropriate commands to the MPM **1070** to fix the problem. In this step, the software will make the trade-off required to fix the problem. In some embodiments, if the GPAL **214** determines the high level fix, then the GPAL **214** sends it to the PMCL **280** to be converted into MPM commands. In step **1126**, the PMCL **218** monitors the problem area for a specified time to check if the problem is fixed. FIG. **11** ends in step **1128**.

In some embodiments, the type of functionality in FIG. **11** can be performed at other levels such as the PMCL **218**. In one example, the PMCL **218** queries (via the MPM **1070**) all the SPMs that have the desired measurement ability (and IPMs) as to their local conditions and can then, for example, build a "map" of power usage that it can then act on.

FIG. **12** depicts a diagram of a system-on-a-chip (SOC) **1200** in another exemplary implementation of the invention. The SOC **1200** is attached to a sensor link **1212**, an RF link **1214**, a control link **1216**, a video link **1294**, an audio link **1295**, an interface link **1296**, a control link **1297**, and a power link **1298**. The SOC **1200** includes clock and distribution management **1210**, an IP block power island **1220**, a memory power island **1230**, a microprocessor power island **1240**, an IP block power island **1250**, a distribution power island **1260**, an IP block power island **1270**, an IP block power island **1280**, and power and distribution management **1290**.

The IP block power island **1220** includes a product standard interface IP block including an analog-to-digital converter (ADC) **1222**, which includes an SPM **1224**. The IP block power island **1230** includes a memory **1232**, which includes an SPM **1234**. The microprocessor power island **1240** includes a microprocessor **1242**, which includes an SPM **1244**. The IP block power island **1250** includes a product standard interface IP block including ADC **1252**, which includes an SPM **1254**. The distribution power island **1260** includes a data and signal distribution **1262**, which includes an SPM **1264**. The IP block power island **1270** includes a general purpose IP block including a digital signal processor (DSP) **1272**, which includes an SPM **1274**. The IP block power island **1280** includes a product-specific IP block **1282**, which includes an SPM **1284**. The power and distribution management **1290** includes an MPM **1292**.

FIG. **13** depicts a flowchart for building a chip with power islands in an exemplary implementation of the invention. FIG. **13** begins in step **1300**. In step **1302**, the IPs or library cells are selected, and the custom logic, if any, is specified to be used to build the chip. In some embodiments, the maximum and sub clock rate, % idle time, and minimum and maximum Vdd are specified. In step **1304**, the register transfer level (RTL) is written. In step **1306**, the RTL is simulated and debugged.

Either during or after the writing of the RTL, a software tool may be used to add annotations for the MPM, IPM, and/or SPM blocks in step **1308**. In some embodiments, the desired functionality options are specified in the annotations. In some embodiments, the optional functionality is specified per SPM block. In some embodiments, the RTL is annotated with SPM configuration information on a per-module basis. In some embodiments, the proper annotation is inserted by hand on a per module basis during or after the RTL is written. In other embodiments, a separate table in the proper format is created with the module names and respective annotations. In some embodiments, a separate software tool provides the ability to interactively build the separate table. In some embodiments, the software tool adds the proper annotation to the un-annotated modules in the RTL using information from the table.

In step **1310**, the synthesis is run on a power island basis, where power islands are not mixed. In step **1312**, performance measurement software is run on each module for each Vdd and Vt option, and then the annotations for the MPM are added to the RTL. In some embodiments, the performance of the design is measured at all desired voltages and Vt combinations. The software tool then derives the actual frequency, Vdd, and Vt tables for each SPM and back annotates the MPM (or IPM) RTL of the SPM characteristics.

In step **1314**, the final synthesis is run on a power island basis. In some embodiments, the modules are separately routed or by SPM. In step **1316**, the software tool is run to hook up power and clocks to each SPM. Step **1318** is the rest of the steps to tape-out. In some embodiments, the software tool generates the finished net-list with all information. FIG. **13** ends in step **1320**.

The above-described elements can be comprised of instructions that are stored on storage media. The instructions can be retrieved and executed by a processor. Some examples of instructions are software, program code, and firmware. Some examples of storage media are memory devices, tape, disks, integrated circuits, and servers. The instructions are operational when executed by the processor to direct the processor to operate in accord with the invention. Those skilled in the art are familiar with instructions, processor, and storage media.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to manage the first power consumption based on needs and operation of the integrated circuit; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) changing a source voltage of the first power island;

ii) after the changing, waiting for the source voltage of the first power island to settle down; and

iii) after the waiting, changing a clock frequency of the first power island.

2. The system of claim **1** wherein the changing a source voltage of the first power island is raising the source voltage, and the changing a clock frequency of the first power island is increasing the clock frequency.

3. The system of claim **2** wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

4. The system of claim **1** wherein the first power manager is further configured to communicate the request to the second power manager.

5. The system of claim **1** wherein the second power manager is further configured to respond to another request, the another request being to decrease the clock frequency and the source voltage of the first power island by: lowering the clock frequency of the first power island and, after the lowering, decreasing the source voltage of the first power island.

6. The system of claim **1** wherein the source voltage of the first power island is controlled by a smart power unit.

7. The system of claim **1** wherein the source voltage of the first power island is provided by an external regulator.

8. The system of claim **1** wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

9. The system of claim **1** wherein the second power manager comprises firmware processable on the integrated circuit.

10. The system of claim **1** wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

11. The system of claim **10** wherein the power management software is embedded firmware in the integrated circuit.

12. The system of claim **1** wherein the first power manager is located outside the integrated circuit.

13. A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

in a first power manager, managing the first power consumption based on needs and operation of the integrated circuit;

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

providing a source voltage to the first power island; and

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

changing the source voltage of the first power island;

after the changing, waiting for the source voltage of the first power island to settle down; and

after the waiting, changing a clock frequency of the clock.

14. The method of claim **13** wherein the changing the source voltage is raising the source voltage, and the changing a clock frequency is increasing the clock frequency.

15. The method of claim **14** further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by:

lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

16. The method of claim **13** wherein the request is communicated to the second power manager by the first power manager.

17. The method of claim **13** further comprising responding to another request that is received by the second power manager, the another request being to decrease the clock frequency of the clock and decrease the source voltage of the first power island by:

lowering the clock frequency of the clock and, after the lowering, decreasing the source voltage of the first power island.

18. The method of claim **13** wherein the source voltage of the first power island is controlled by a smart power unit.

19. The method of claim **13** further comprising providing external regulation for the source voltage of the first power island.

20. The method of claim **13** wherein the plurality of power islands includes a second power island, and the first power manager determines power trade offs between the first power island and the second power island.

21. The method of claim **13** further comprising, in a third power manager:

i) managing a third power consumption of the power consumptions, and the plurality of power islands including

a second power island having an associated power consumption that is the third power consumption; and

ii) communicating with the first power manager.

22. The method of claim **21** wherein the second and third power managers are at a same hierarchical level, and the first power manager is at a higher hierarchical level as compared to the second and third power managers.

23. A system comprising:

an integrated circuit to effect power consumptions in operation, the power consumptions including a first power consumption and a second power consumption;

a plurality of power islands of the integrated circuit including a first power island having an associated power consumption, the associated power consumption of the first power island being the second power consumption;

a first power manager configured to manage the first power consumption based on needs and the operation of the integrated circuit; and

a second power manager configured to:

a) communicate with the first power manager; and

b) respond to a request to manage the second power consumption for the first power island by:

i) stopping a clock of the first power island;

ii) saving a state of the first power island; and

iii) after the saving, powering off the first power island.

24. The system of claim **23** wherein the second power manager is further configured to carry out the saving of the state of the first power island after the stopping.

25. The system of claim **23** wherein the first power manager is further configured to communicate the request to the second power manager.

26. The system of claim **23** further comprising a buffer for storing the state that is saved.

27. The system of claim **23** wherein the second power manager is further configured to respond to another request, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock of the first power island.

28. The system of claim **27** further comprising a buffer for storing the state that is saved, and the buffer being accessible during the restoring.

29. The system of claim **23** wherein the plurality of power islands includes a second power island, and the first power manager is further configured to determine power trade offs between the first power island and the second power island.

30. The system of claim **23** wherein the second power manager comprises firmware processable on the integrated circuit.

31. The system of claim **23** wherein the second power manager comprises a power management processor dedicated to execute power management software, the power management processor being located in the integrated circuit.

32. The system of claim **31** wherein the power management software is embedded firmware in the integrated circuit.

33. The system of claim **23** wherein the first power manager is located outside the integrated circuit.

34. A method carried out in a system that includes an integrated circuit that effects power consumptions in operation, the power consumptions including a first power consumption and a second power consumption, and the method comprising:

in a first power manager, managing a first power consumption based on needs and operation of the integrated circuit;

providing a clock to a first power island of a plurality of power islands of the integrated circuit, and the first power island having an associated power consumption that is the second power consumption;

in a second power manager, communicating with the first power manager, and responding to a request to manage the second power consumption for the first power island by:

stopping the clock;

saving a state of the first power island; and

after the saving, powering off the first power island.

35. The method of claim **34** wherein the saving of the state of the first power island is carried out after the stopping.

36. The method of claim **34** wherein the request is communicated to the second power manager by the first power manager.

37. The method of claim **34** wherein the state that is saved is stored in a buffer.

38. The method of claim **34** further comprising responding to another request that is received by the second power manager, the another request being to enter a powered up state by:

i) powering on the first power island;

ii) after the powering on, restoring the state of the first power island; and

iii) after the restoring, starting the clock.

39. The method of claim **38** wherein the state that is saved is stored in a buffer accessed during the restoring.

* * * * *

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A PRIOR PATENT

In re Application of: Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell

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For: Power Managers For An Integrated Circuit

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The undersigned is an attorney or agent of record.

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MTEKLEMI ADJ #00000004 Mailroom Dt: 06/24/2016
Seq No: 8 Sales Acctg Dt: 07/11/2016 504154 15192486

01	FC : 1011	280.00	CR
02	FC : 1111	600.00	CR
03	FC : 1311	720.00	CR
04	FC : 1201	2100.00	CR
05	FC : 1202	4640.00	CR
06	FC : 1051	140.00	CR