

National Entry Form (PatentsApplication2006-532832)

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[Document Name]National Entry Form

[Date of submission]November 7, 2005

[Recipient] Commissioner of the Japan Patent Office: Makoto Nakajima

[Indication of Application]

[International application number]PCT/US2004/014205

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[Deposit account number]002989

[Payment amount]16000 yen

 Inquiry of history information**Written Amendment (voluntary/content) (PatentsApplication2006-532832)***** NOTICES ***

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[Document Name]Written Amendment

[Date of submission]July 22, 2011

[Recipient] Commissioner of the Japan Patent Office: Yoshiyuki Iwai

[Indication of case]

[Application number]Japanese Patent Application No. 2006 / 532832

[Person who submits written amendment]

[Identification Number]507007430

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[Amendment 1]

[Document name for target of amendment]Patent Claims

[Item name for target of amendment]Full Text

[Amendment type]Change

[Content of amendment]

[Document Name]Patent Claims

[Claim 1]

A method of managing power in an integrated circuit having a plurality of power islands, comprising: determining a target power level of one of the power islands based on needs and operation of the integrated circuit in which power consumption is independently controlled in each of the power islands; monitoring a power consumption level of the one power island; determining at least one operation from a plurality of operations to change the power consumption level of the one power island to the target power level of the one power island, wherein one operation of the plurality of operations comprises selecting a frequency of the one power island and another operation of the plurality of operations comprises selecting a voltage of the one power island; and performing the at least one operation to change the power consumption level of the one power island to the target power level of the one power island.

[Claim 2]

The method of claim 1, further comprising: determining whether a threshold level has been crossed based on the power consumption level; and performing the at least one action based on crossing the threshold level.

[Claim 3]

The method of claim 1, wherein the island of power is represented based on one of a group comprising a geographic factor of the integrated circuit and a functional circuit of the integrated circuit.

[Claim 4]

The method of claim 1, wherein the island of power comprises one of a group of sub-islands of power and a plurality of clock domains.

[Claim 5]

The method of claim 1, wherein yet another one of the plurality of operations comprises one of the group of selecting a clock of the one power island, turning on power of the one power island, turning off power of the one power island, putting the one power island into a sleep mode, saving a state of a component of the one power island, and restoring a state of a component of the one power island.

[Claim 6]

The method of claim 1, wherein the voltage of the one power island comprises one of the group of a source voltage and a threshold voltage.

[Claim 7]

A system for an integrated circuit having a plurality of power islands in which power consumption is independently controlled in each of the power islands, the system comprising: a power control circuit configured to control power of one of the power islands; and a power manager configured to determine a target power level of the one power island based on needs and operations of the integrated circuit, monitor a power consumption level of the one power island, determine at least one of a plurality of operations to change the power consumption level of the one power island to the target power level of the one power island, and perform the at least one operation to change the power consumption level of the one power island to the target power level of the one power island, wherein one of the plurality of operations comprises selecting a frequency of the one power island and another of the plurality of operations comprises selecting a voltage of the one power island.

[Claim 8]

The system of claim 7, wherein the power manager is configured to determine whether a threshold level has been crossed based on the power consumption level, and to perform the at least one operation based on the crossing of the threshold level.

[Claim 9]

The system of claim 7, wherein the island of power is represented based on one of a group comprising a geographical factor of the integrated circuit and a functional circuit of the integrated circuit.

[Claim 10]

The system of claim 7, wherein the island of power comprises one of a group of sub-islands of power and a plurality of clock domains.

[Claim 11]

The system of claim 7, wherein yet another one of the plurality of operations comprises one of the group of selecting a clock of the one power island, turning on power of the one power island, turning off power of the one power island, putting the one power island into a sleep mode, saving a state of a component of the one power island, and restoring a state of a component of the one power island.

[Claim 12]

The system of claim 7, wherein the voltage of the one power island comprises one of the group of a source voltage and a threshold voltage.

[Claim 13]

The system of claim 7, further comprising a bus coupled to the power manager and the power island.

[Claim 14]

The system of claim 7, wherein the power manager comprises one of a group comprising: a master manager configured to control power of the integrated circuit; and a slave manager configured to control power of the one power island.

[Claim 15]

The system of claim 7, wherein the power control circuit comprises one of a group comprising a clock multiplexing circuit, a voltage multiplexing circuit, and a level shifting circuit.

[Claim 16]

The method of claim 1, further comprising restoring a state of a component of one of the power islands.

[Claim 17]

A system for an integrated circuit having a plurality of power islands in which power consumption is independently controlled in each of the power islands, comprising: a power control circuit configured to control power in one of the power islands; and a power manager configured to determine a target power level of the one power island, monitor a power consumption level of the one power island, determine at least one of a plurality of actions to change the power consumption level of the one power island to the target power level of the one power island, the plurality of actions including selecting a voltage of the one power island, and perform the at least one of the plurality of actions to change the power consumption level of the one power island to the target power level of the one power island.

[Claim 18]

The system of claim 17, wherein the island of power is represented based on a geographic factor of the integrated circuit.

[Claim 19]

The system of claim 17, wherein the power island is represented based on a functional circuit of the integrated circuit.

[Claim 20]

The system of claim 17, wherein the island of power comprises a sub-island of power.

[Claim 21]

The system of claim 17, wherein the power island comprises a plurality of clock domains.

[Claim 22]

The system of claim 17, wherein the plurality of operations comprises selecting a clock frequency of one of the power islands.

[Claim 23]

The system of claim 17, wherein the plurality of operations comprises selecting a clock of one of the power islands.

[Claim 24]

The system of claim 17, wherein the plurality of operations comprises changing a first voltage of one of the power islands.

[Claim 25]

The system of claim 24, wherein the first voltage comprises a source voltage.

[Claim 26]

The system of claim 24, wherein the first voltage comprises a threshold voltage.

[Claim 27]

The system of claim 17, wherein the plurality of operations comprises turning on power in one of the power islands.

[Claim 28]

The system of claim 17, wherein the plurality of operations comprises turning off power in one of the power islands.

[Claim 29]

The system of claim 17, wherein the plurality of operations comprises changing one of the power islands to a sleep mode.

[Claim 30]

The system of claim 17, wherein the power manager is configured to: determine whether a threshold level has been crossed based on the power consumption level; and perform the action based on crossing the threshold level.

[Claim 31]

The system of claim 17, wherein the power manager is configured to save a state of a component of one of the power islands.

[Claim 32]

The system of claim 17, wherein the power manager is configured to restore a state of a component of one of the power islands.

[Claim 33]

The system of claim 17, further comprising a bus coupled to the power manager and the power island.

[Claim 34]

The system of claim 17, wherein the power manager comprises a master manager configured to control power of the integrated circuit.

[Claim 35]

The system of claim 17, wherein the power manager comprises a slave manager configured to control power of one of the islands of power.

[Claim 36]

The system of claim 17, wherein the power control circuit comprises a clock multiplexing circuit.

[Claim 37]

The system of claim 17, wherein the power control circuit comprises a voltage multiplexing circuit.

[Claim 38]

The system of claim 17, wherein the power control circuit comprises a level shift circuit.

[Claim 39]

A program, stored on a software storage medium, for managing power in an integrated circuit having a plurality of power islands, the program, when executed by a processor, causing the processor to function as a power manager that performs the following operations: determining a target power level of one of the power islands whose power consumption is independently controlled in each of the power islands; monitoring a power consumption level of the one power island; and determining at least one of a plurality of operations to change the power consumption level of the one power island to the target power level of the one power island, the plurality of operations including selecting a voltage of the one power island.

[Claim 40]

The article of manufacture of claim 39, wherein the island of power is represented based on a geographic factor of the integrated circuit.

[Claim 41]

The article of manufacture of claim 39, wherein the power island is represented based on a functional circuit of the integrated circuit.

[Claim 42]

The article of manufacture of claim 39, wherein the island of power comprises a sub-island of power.

[Claim 43]

The article of manufacture of claim 39, wherein the power island comprises a plurality of clock domains.

[Claim 44]

The article of manufacture of claim 39, wherein the plurality of operations comprises selecting a clock frequency for one of the power islands.

[Claim 45]

The program product of claim 39, wherein the plurality of operations comprises selecting a clock of one of the power islands.

[Claim 46]

The article of manufacture of claim 39, wherein the plurality of operations comprises changing a first voltage of one of the power islands.

[Claim 47]

The computer program product of claim 46, wherein the first voltage comprises a source voltage.

[Claim 48]

The computer program product of claim 46, wherein the first voltage comprises a threshold voltage.

[Claim 49]

The article of manufacture of claim 39, wherein the plurality of operations comprises turning on power in one of the power islands.

[Claim 50]

The article of manufacture of claim 39, wherein the plurality of operations comprises turning off power in one of the power islands.

[Claim 51]

The article of manufacture of claim 39, wherein the plurality of operations comprises changing one of the power islands to a sleep mode.

[Claim 52]

The article of manufacture of claim 39, wherein the power manager, when executed by the processor, is operable to: determine whether a threshold level has been crossed based on the power consumption level; and perform the action based on crossing the threshold level.

[Claim 53]

The article of manufacture of claim 39, wherein the power manager, when executed by the processor, is operative to save a state of a component of one of the power islands.

[Claim 54]

The program of claim 39, wherein the power manager, when executed by the processor, is operative to restore a state of a component of one of the power islands.

[Amendment 2]

[Document name for target of amendment]Description

[Item name for target of amendment]0007

[Amendment type]Change

[Content of amendment]

[0007]In one example of designing an integrated circuit, a library cell is selected, custom logic is identified, and the integrated circuit is built. The register transfer level (RTL:register transfer level) of the IC is then written for simulation and debugging. After simulation and debugging, synthesis is performed on the integrated circuit. Performance measurement software is executed to determine the performance of the integrated circuit. The final synthesis of the integrated circuit may be performed based on the optimal performance of the integrated circuit.

[Patent document 1]The description of US Patent No. 5,778,237

[Patent document 2]The description of US Patent No. 6,779,169

[Patent document 3]The description of US Patent No. 6,820,240

[Patent document 4]The description of US Patent No. 6,883,152

 Inquiry of history information**Decision of Refusal (PatentsApplication2006-532832)***** NOTICES ***

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Decision of Refusal

Patent Application Number: Japanese Patent Application No. 2006 to 532832

Proposed: August 18, 2011

Examiner: IDE Wasui 9072 5C00

Title of the invention:Managing power on integrated circuits using power islands

Patent Applicant: Mosaid Technologies Corporation

Agent: Tadahiko ITO (and 2 others)

This application should be refused for the reason mentioned in the Notice of Reasons for Refusal dated 1/19/Heisei 23. In addition, although the contents of the written opinion have been examined, sufficient grounds for overturning the reasons for refusal cannot be found.

Remarks

The applicant submitted a written amendment, but the amendment made in this written amendment was dismissed on the same date as this decision.

The argument by the applicant has been examined, but it is based on the matter added by the above rejected amendment and cannot be adopted.

The applicant who is dissatisfied with the examiner's decision, may file a request for a trial to the Commissioner of the Japan Patent Office within three months (where overseas resident, within four months) from the date when the copy of the examiner's decision has been served (Patent Act Article 121 (1)).

(Explanation based on the Administrative Case Litigation Act Article 46 (2))

The applicant may not file an action for the revocation of an administrative disposition against the examiner's decision. The applicant may file a suit against the trial decision regarding the demand for the trial of this examiner's decision (Patent Act Article 178 (6)).

Director / Deputy, Chief Reviewer / Deputy, Reviewer, Assistant Reviewer Yoshiyuki Kusaka, Hiroshi Kitaoka, Wasui Ide, 8323 8940 9072

Decision of Dismissal of Amendment (PatentsApplication2006-532832)

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Decision of Dismissal of Amendment

Patent Application Number: Japanese Patent Application No. 2006 to 532832

Proposed: August 18, 2011

Examiner: IDE Wasui 9072 5C00

Title of the invention:Managing power on integrated circuits using power islands

Patent Applicant: Mosaid Technologies Corporation

Agent: Tadahiko ITO (and 2 others)

[Conclusion]

The amendments to the description, scope of claims, or drawings in the written amendment dated July 22, 2011 are dismissed for the following reasons.

Reason

According to the above written amendment, the applicant has amended the recitation in Claim 1 that "at least one operation for changing the power consumption level of the aforementioned one power island to the aforementioned target power level is determined from a plurality of operations, and one operation of the aforementioned plurality of operations has selected the frequency of the aforementioned one power island" to "at least one operation is determined from a plurality of operations for changing the power consumption level of the aforementioned one power island to the aforementioned target power level of the aforementioned one power island, one operation of the aforementioned plurality of operations has selected the frequency of the aforementioned one power island, and the other operation of the aforementioned plurality of operations has selected the voltage of the aforementioned one power island."This amendment newly adds the operation of selecting the voltage without selecting the frequency in the operation of setting the power consumption level of the power island to the target power level, and does not limit the matters for specifying the invention. Therefore, this amendment is not intended for the matters listed in the Patent Act Article 17-2 (4) (ii). In addition, this amendment is not intended for any of the matters listed in the Patent Act Article 17-2 (4) (i), (iii), and (iv). Therefore, since the amendment by the above-mentioned written amendment does not satisfy the requirements as provided in the Patent Act Article 17-2, the decision is made as described above under the provisions of the Patent Act Article 53 (1).

In addition, it is assumed that the above-mentioned amendment is intended for the matters listed in the Patent Act Article 17-2 (4) (ii). In this case, the invention according to the amended Claim 1 must be granted a patent independently at the time of filing the patent application under the provisions of the Patent Act Article 126 (5) as applied mutatis mutandis pursuant to the Patent Act Article 17-2 (5). However, as described below, the invention according to the amended Claim 1 cannot be granted a patent independently at the time of filing the patent application under the provisions of the Patent Act Article 29 (2). That is, when the invention according to the amended Claim 1 is compared with the invention described in the following Cited Document 1, there is no significant difference between the two except for the points listed below. Difference 1: In the operation related to the frequency for changing the power consumption of one power island, the frequency is selected in the invention according to Claim 1, whereas the operation is performed by turning the clock on / off in the invention described in Cited Document 1. Difference 2: In the candidate operation for changing the power consumption of one power island, the invention according to Claim 1 includes the operation of selecting the voltage of the power island in addition to the operation related to the frequency described in Difference 1, whereas the invention described in Cited Document 1 does not specify the control of the voltage. The different feature(s) will be examined as follows. Whether the clock frequency in the state where the power consumption is lowered from the normal state is set to 0, that is, the clock is turned off, or is set to a frequency higher than 0 but lower than the normal state is merely a matter of design change that could have been appropriately set by a person skilled in the art according to the configuration and the like such as whether the internal logic can withstand the clock being turned off. Therefore, the inventive step cannot be affirmed by Difference 1. It is merely a technical matter well known to a person skilled in the art to

simultaneously reduce the clock frequency and the power supply voltage for a specific circuit portion in order to reduce power consumption, as described in Cited Documents 2 and 3. Thus, the technical matter relating to Difference 2 is merely a technical matter already well known to a person skilled in the art at the time of the filing of the present application, and in the invention described in Cited Document 1, as a method of power management control of the block, paragraph [0285] It is not particularly difficult to adopt this well-known technique instead of the on / off of the clock described in ~ [0287], and it does not have a remarkable effect sufficient to affirm the inventive step. Therefore, even under the above assumptions, it should be noted that the amendment by the above written amendment does not satisfy the requirements as provided in the Patent Act Article 17-2 (4) and (5), and is rejected under the provisions of the Patent Act Article 53 (1).

[Cited Documents, etc.] Document 1: JP H11 - 054225 a Document 2: JP 2003 - 086693 a Document 3: JP 2001 - 238190 a

Director / Deputy, Chief Reviewer / Deputy, Reviewer, Assistant Reviewer Yoshiyuki Kusaka, Hiroshi Kitaoka, Wasui Ide, 8323 8940 9072

 Inquiry of history information

Notice of Withdrawal of Application (PatentsApplication2006-532832)*** NOTICES ***

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[Document Name] Notice of Withdrawal of Application

[Date of submission] December 9, 2011

[Recipient] Commissioner of the Japan Patent Office: Yoshiyuki Iwai

[Indication of case]

[Application number] Japanese Patent Application No. 2006 / 532832

[Patent applicant]

[Identification Number] 507007430

[Name] Mosaid Technologies Corporation

[Representative]

[Identification Number] 100070150

[Patent attorney]

[Name] Tadahiko Ito

[Tel No.] 03-5424-2511

[The list of submitted documents]

[Document name] Power of attorney 1 [Indication of incorporation] Reference is made to the submission of the general power of attorney filed on January 9, 2019.