

3.5 Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor

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High-performance and low-power microprocessors are key to PDA applications. In Fig. 3.5.1, dynamic voltage and frequency management (DVFM) scheme with leakage-compensation effect is introduced in a microprocessor with wideband embedded DRAM. Our DVFM scheme autonomously controls the clock frequency from 8MHz to 123MHz in 0.5MHz step and adaptively controls voltage from 0.9V to 1.6V in 5mV steps, achieving 82% power reduction in a personal information manager (PIM) application for a low-power embedded microprocessor.

Dynamic voltage and/or frequency control schemes have been reported in [1-5]. Our approach offers both dynamic frequency control (DFC) and dynamic voltage control (DVC). Clock frequency is autonomously and dynamically controlled while voltage is adaptively controlled resulting in the leakage power compensation effect. This DVFM approach achieved 82% power reduction in PIM application.

Figure 3.5.2 shows the DVFM block consisting of the DFC and DVC units. The DFC controls the clock frequency at the required minimum value by monitoring LSI activity autonomously without special power-management software. The activity monitor circuit unit calculates the total LSI activity periodically from activity information of CPU, bus and embedded DRAM. The frequency-adjuster circuit unit calculates optimum clock frequency based on the activity value derived from the activity monitor to reserve the required inactive margin cycles within the monitoring period and indicates the next clock frequency to clock generator. The clock generator has eight base-clocks, and dynamically creates the system clock between 8MHz and 123MHz in 0.5MHz steps. LSI can operate continuously without PLL reload or system reset when the clock frequency changes.

Figure 3.5.3 shows the DVC block that consists of two major parts: the delay synthesizer that emulates the critical path of the LSI and the delay detector. The delay characteristic of the actual LSI is composed of not only simple transistor delay factor but also wire delay and other factors. The delay synthesizer consists of gate delay, wire delay and rise / fall delay programmable components. And desired delay characteristic can be synthesized by combining those delay factors.

The measured frequency-voltage characteristics over the full range of process deviation from Vth minimum to maximum for the delay synthesizer of DVC and the main logic of LSI is shown in the figure with the delay synthesizer. As seen in Fig. 3.5.3, the delay synthesizer greatly improves the accuracy of critical path tracking. This proves that the DVC has an excellent correlation with the main logic of LSI for emulation.

Detect pulse from the pulse generator propagates through the delay synthesizer and reaches the delay detector. The delay detector consists of a delay line and flip-flops. This pulse is latched at cycle time of input clock and digitizes delay-propagation.

The minimum operating voltage from 0.9V to 1.6V in 5mV steps is always supplied by controlling off-chip DC-DC converter to adjust the digitized value to target, that is, to maintain LSI operation correctly at the given clock frequency.

Figure 3.5.4 describes the operation of the DVFM. When the clock frequency is required to increase, the DVC reference clock is switched to the next higher frequency in advance and DFC directs the DC-DC converter to raise the supply voltage rapidly (Fig. 3.5.4 (1)). The main logic clock frequency is changed after the DVC confirms the voltage has increased enough (Fig. 3.5.4 (2)). When the clock frequency is lowered, both the DVC reference clock and the system clock are changed simultaneously and at the same time, the supply voltage starts to decrease (Fig. 3.5.4 (3)). The feedback loop of the DVC maintains the supply voltage at the minimum level needed for device operation at each clock frequency. A measured system-clock transition waveform and the system-clock generation scheme are also illustrated. The system clock is selected from the eight base-clocks, then thinned out to attain the frequency between them and is switched seamlessly from frequency to frequency. Example is given for a frequency transition from 24.5 to 48.5MHz. These thinned out system-clock frequencies, 24.5MHz and 48.5MHz, are generated from 32MHz and 64MHz base-clocks, respectively.

The most notable feature of the DVC is its ability to effectively compensate for leakage power over process deviation that becomes more critical as process technology shrinks. As shown in Fig. 3.5.5, in fixed supply voltage schemes, the supply voltage is determined by Vth-max while maximum total power consumption is determined by Vth-min. DVC results in decreased supply voltage for smaller value of Vth. This results in lower maximum total power consumption. Therefore both leakage power and active power decrease. That is, our DVC adaptively compensates leakage power with minimizing supply voltage depending on process deviation and temperature fluctuation.

Figure 3.5.6 shows comparisons of power consumption between this work and a conventional design for MPEG4-decoding and PIM applications. The DVFM achieved 82% power reduction with another 38% reduction by wideband embedded DRAM in the PIM application.

The chip is implemented using 0.18μm CMOS embedded DRAM process with 4 poly and 5 metal layers. A micrograph of the chip is shown in Fig. 3.5.7. Chip size is 10.93x13.18mm².

In conclusion, the DVFM scheme with leakage compensation is introduced. Our DVFM scheme controls autonomously the clock frequency from 8MHz to 123MHz in 0.5MHz steps and adaptively controls voltage from 0.9V to 1.6V in 5mV steps. In PIM application for a low-power embedded microprocessor, 82% power reduction is achieved. As process technology shrinks, this adaptive leakage compensation scheme will become more effective to realize high-performance and low-power mobile consumer applications.

Acknowledgements:

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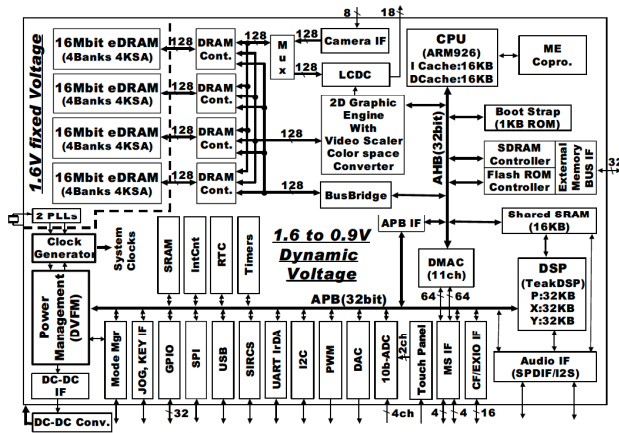


Figure 3.5.1: LSI block diagram.

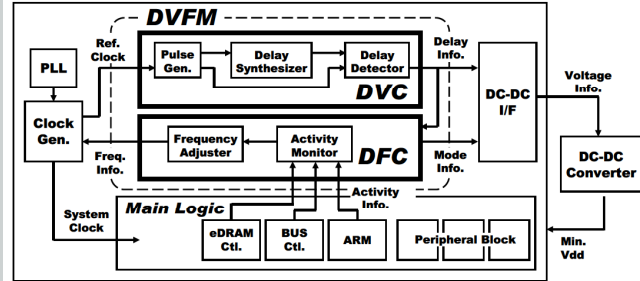


Figure 3.5.2: DVFM block diagram.

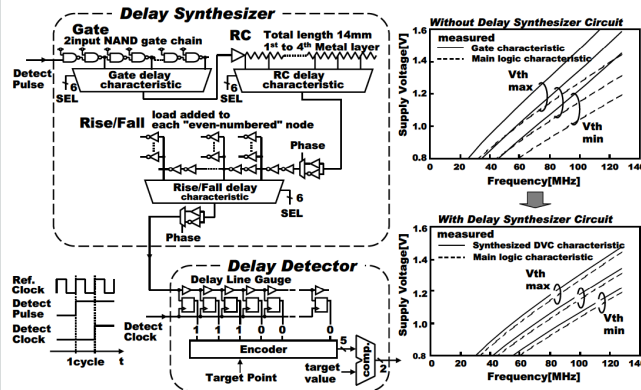


Figure 3.5.3: DVC block diagram and correlation.

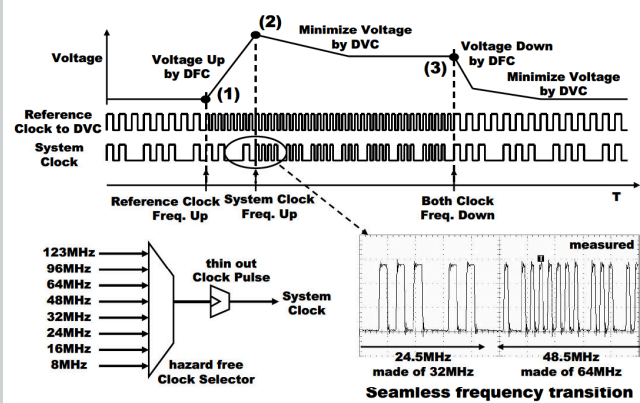


Figure 3.5.4: Frequency/voltage control scenarios in DVFM and measured system clock transition.

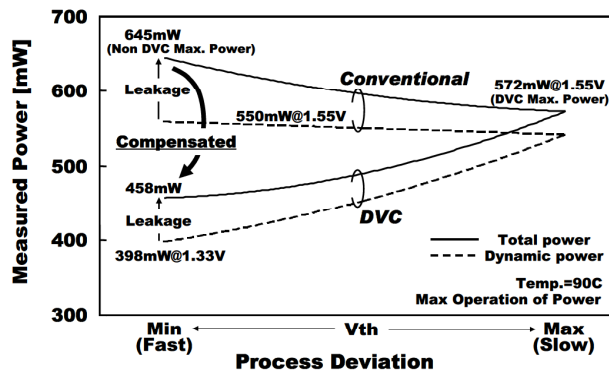


Figure 3.5.5: Leakage compensation effect.

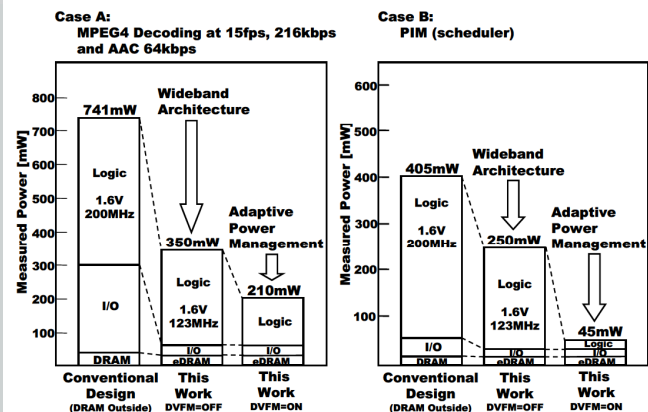


Figure 3.5.6: Comparison of power consumption.

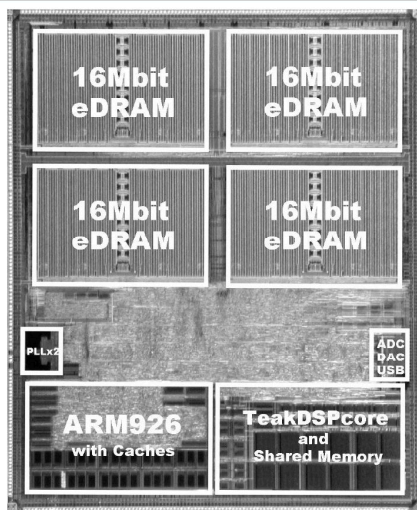


Figure 3.5.7: Micrograph of the chip.

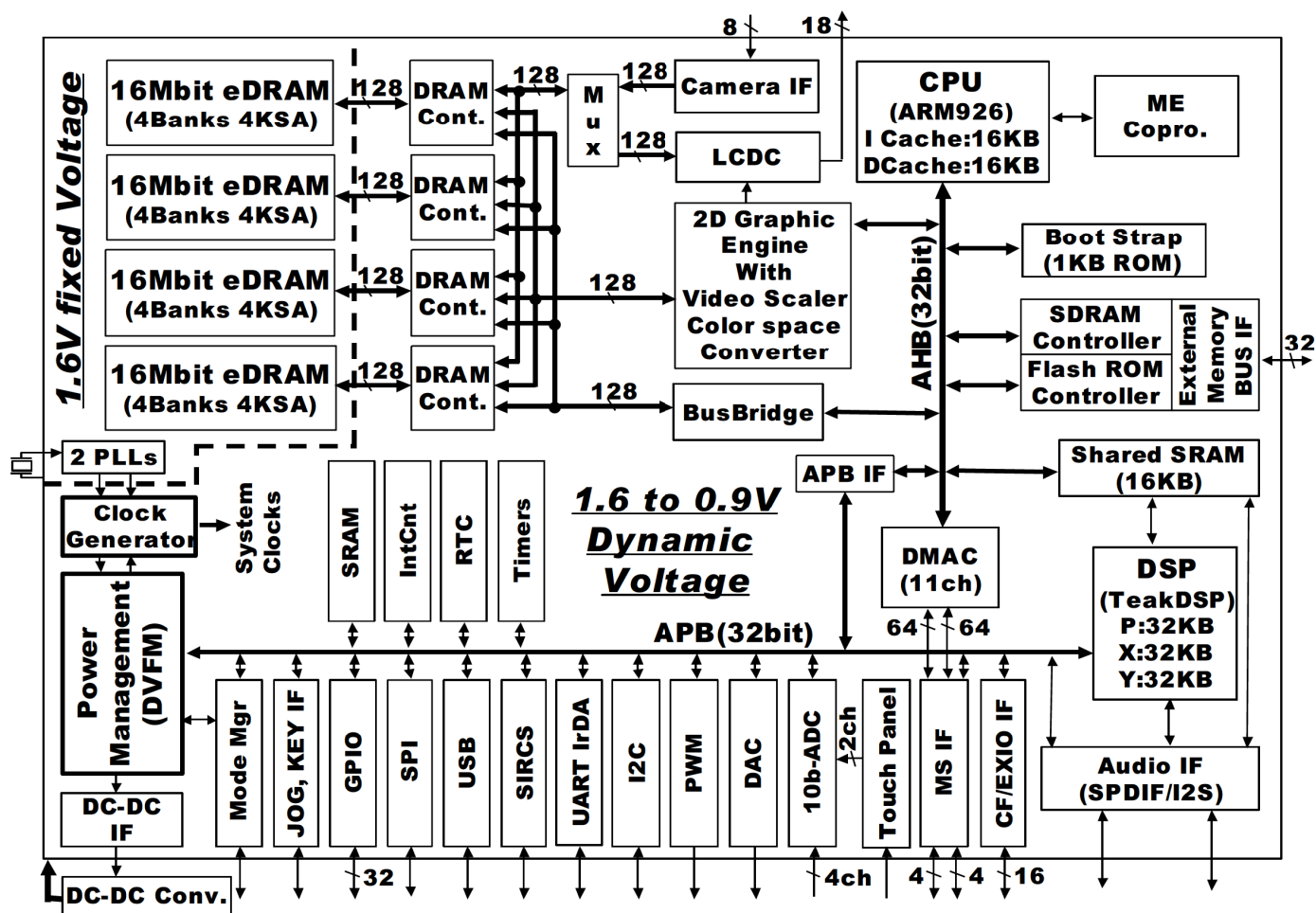


Figure 3.5.1: LSI block diagram.

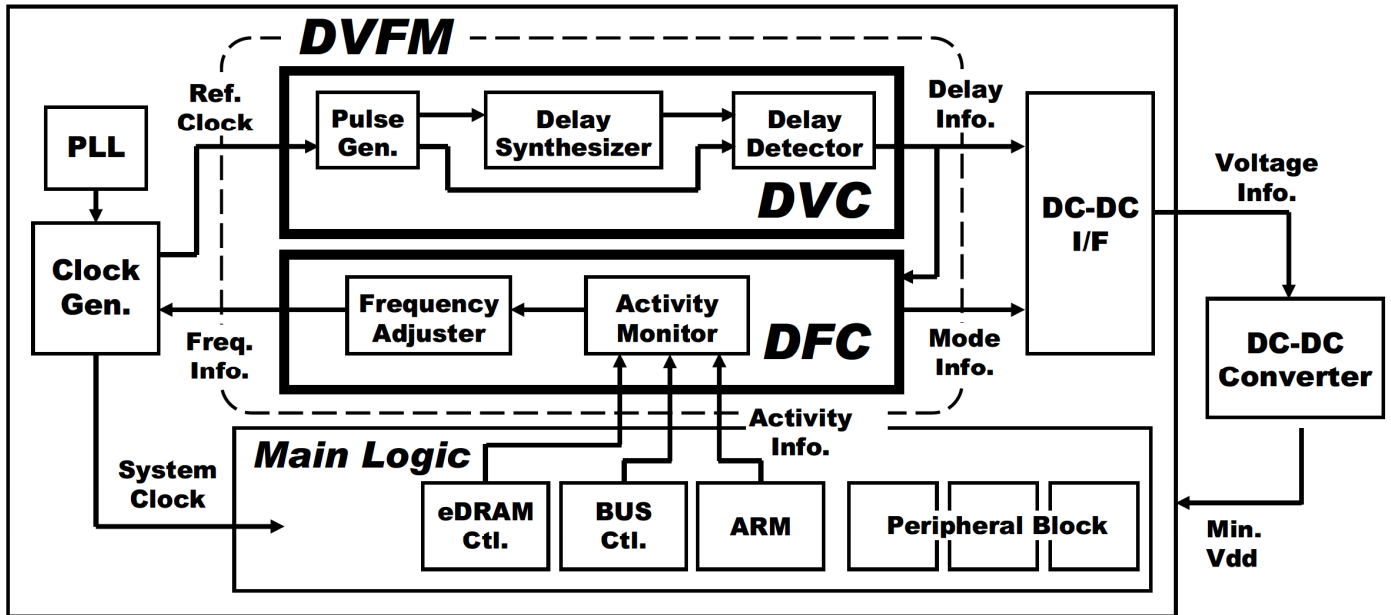


Figure 3.5.2: DVFM block diagram.

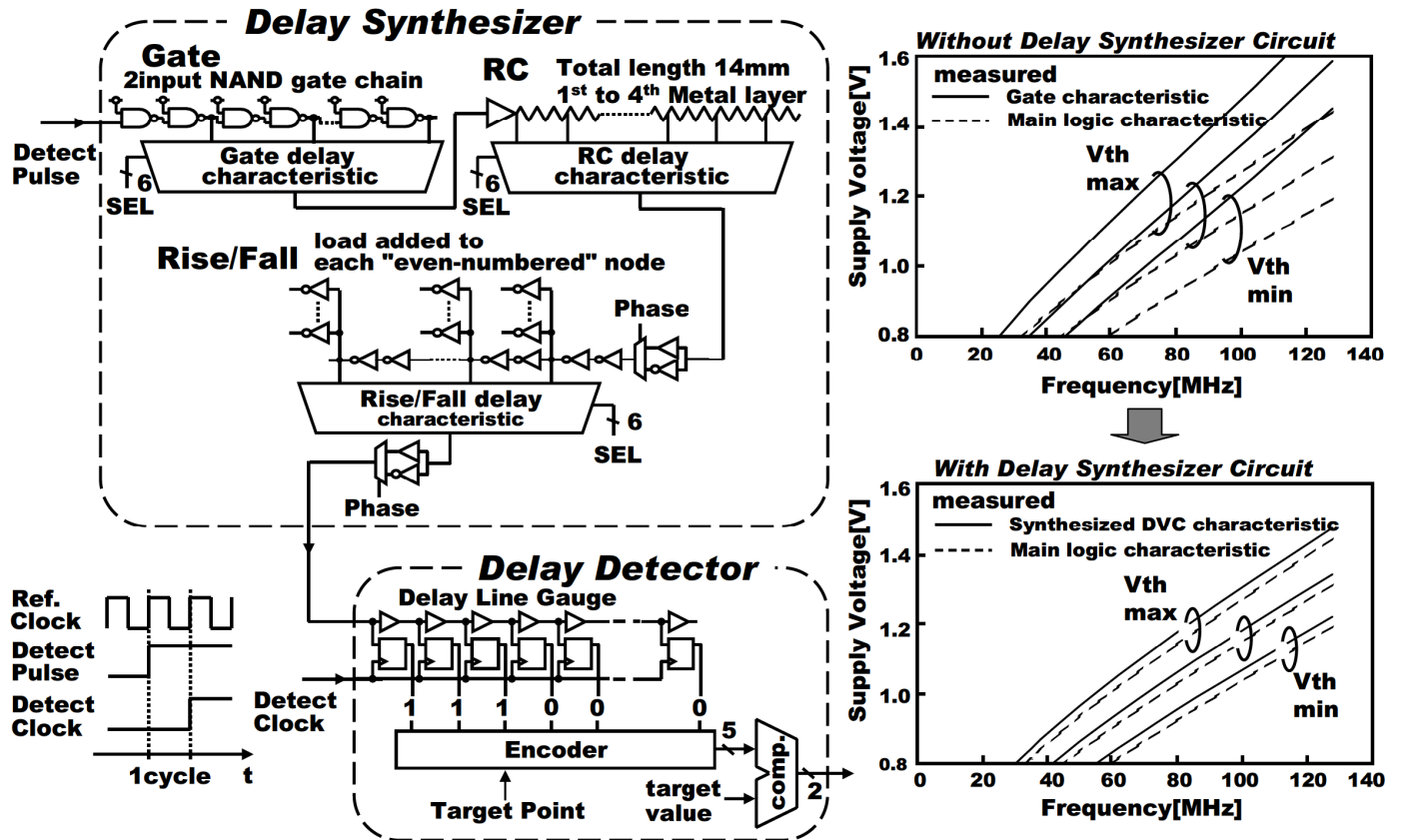


Figure 3.5.3: DVC block diagram and correlation.

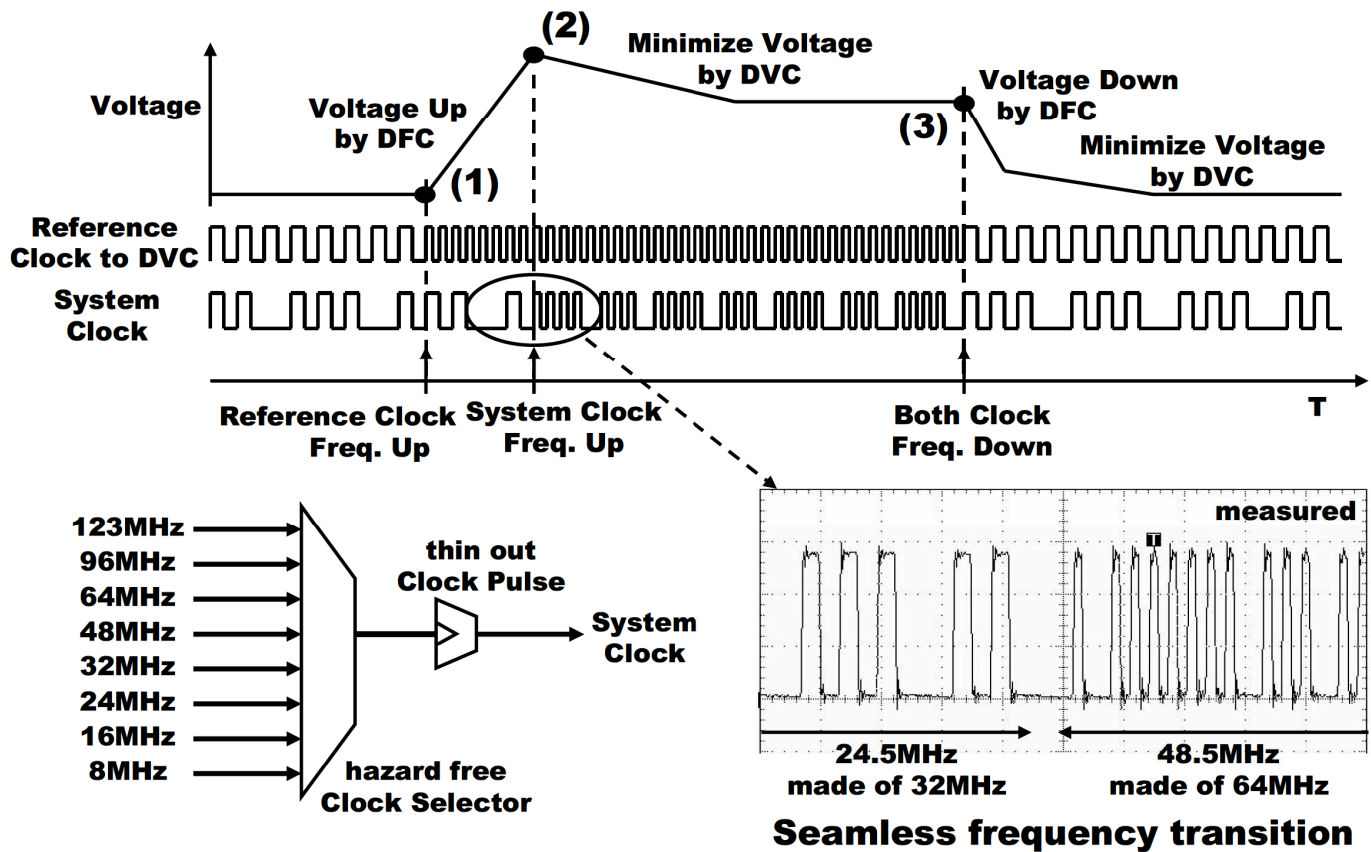


Figure 3.5.4: Frequency/voltage control scenarios in DVFM and measured system clock transition.

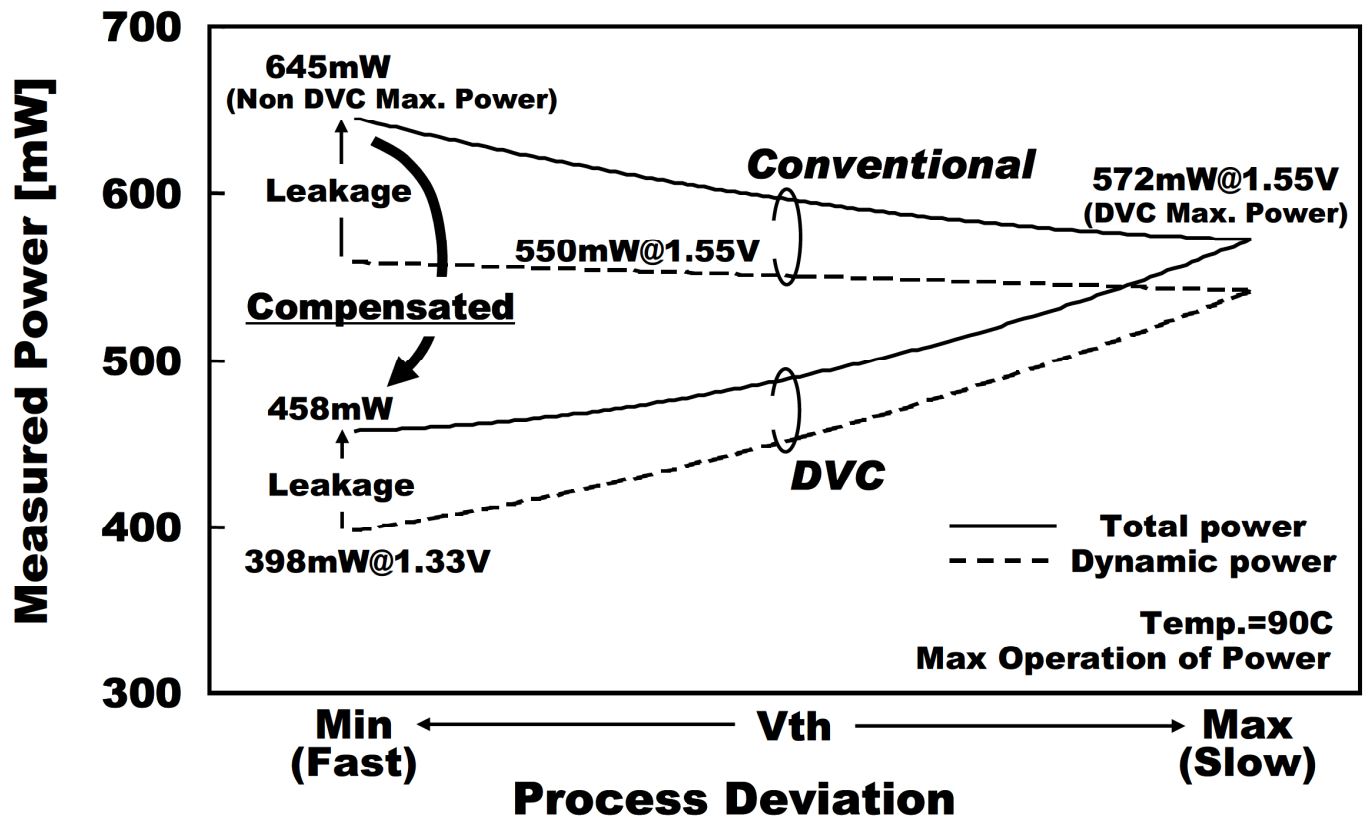
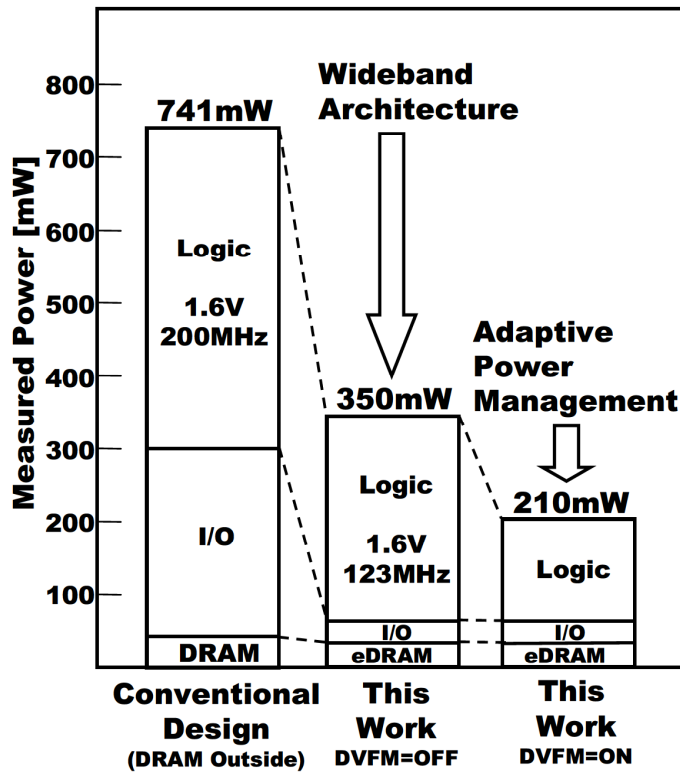


Figure 3.5.5: Leakage compensation effect.

Case A:
MPEG4 Decoding at 15fps, 216kbps
and AAC 64kbps



Case B:
PIM (scheduler)

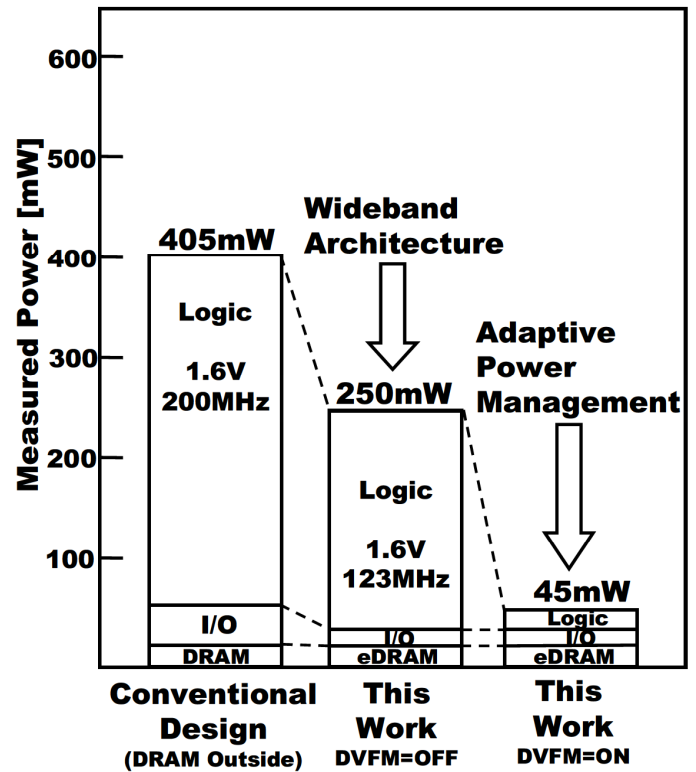


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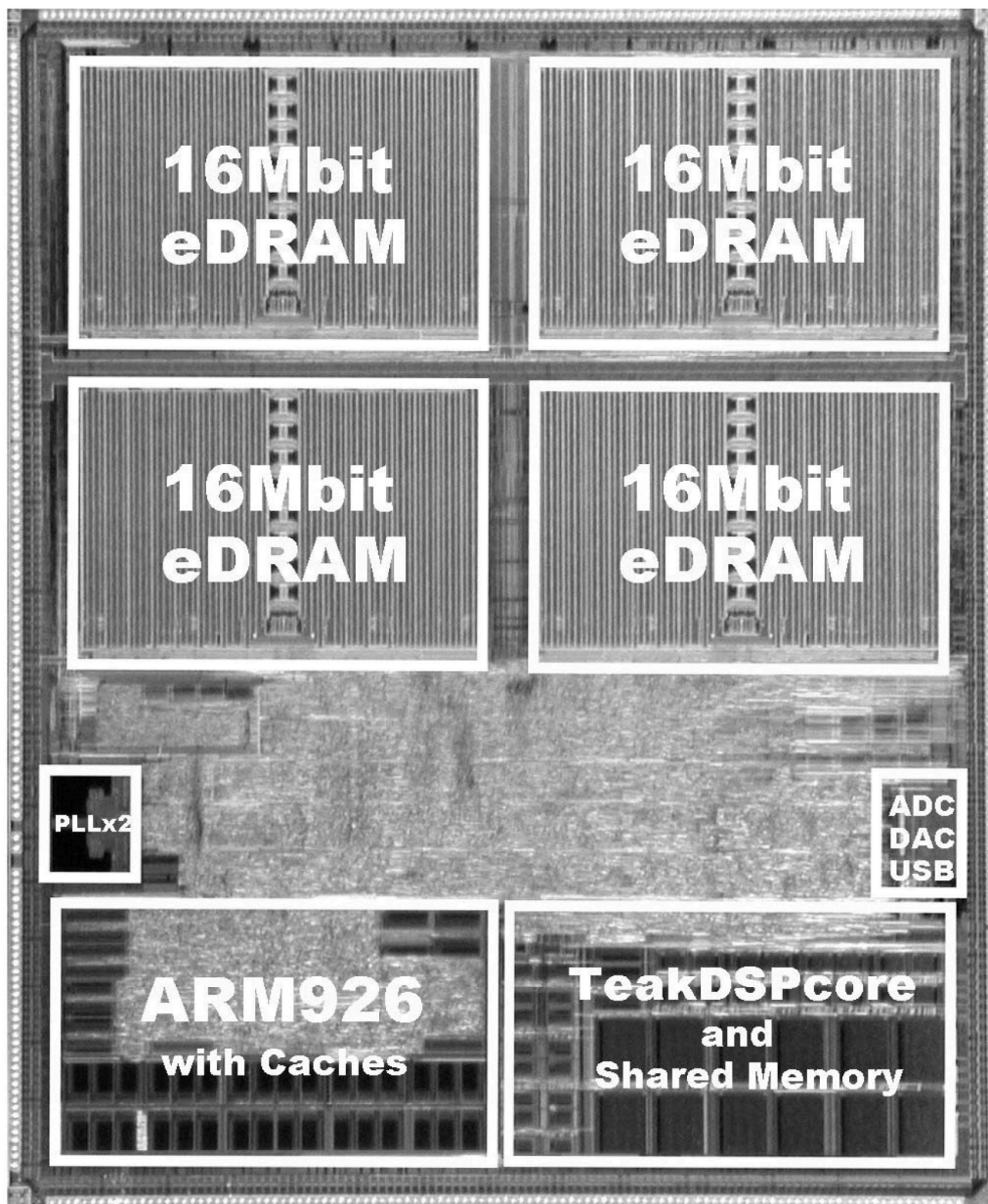


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