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PTO/SB/16 (02-01)
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EV 194331372 US EV194331372US

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Barry	Hoberman	Cupertino, CA

☐ *Additional inventors are being named on the ___ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (280 characters max)

System and Method for Managing Power in Integrated Circuits

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* 29

☐ Drawing(s) *Number of Sheets*

☐ Application Data Sheet. See 37 CFR 1.76

☐ CD(s), Number

☒ Other (specify) return postcard

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant claims small entity status. See 37 CFR 1.27.

☒ A check or money order is enclosed to cover the filing fees

☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 06-0600

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE AMOUNT ($) $160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE Wendi R Schepler

Date 5/7/2003

TYPED or PRINTED NAME Wendi R. Schepler

REGISTRATION NO. *(if appropriate)* 43,091

Docket Number: PA2258PRV

TELEPHONE 650-812-3400

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This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

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INFINEON 1041
Infineon v. Mosaid
IPR2025-01171

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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 160.00

Complete if Known	
Application Number	
Filing Date	May 7, 2003
First Named Inventor	Barry Hoberman
Examiner Name	
Art Unit	
Attorney Docket No.	PA2258PRV

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 06-0600

Deposit Account Name: Carr & Ferrell, LLP

The Director is authorized to: *(check all that apply)*

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	160

SUBTOTAL (1) ($) 160

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below		Fee Paid
Total Claims	- 20 =		x	=	0
Independent Claims	- 3 =		x	=	0
Multiple Dependent				=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Wendi R. Schepler	*Registration No. (Attorney/Agent)*	43,091	*Telephone*	650-812-3400
Signature	Wendi R Schepler			*Date*	5/7/2003

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[redacted]

Provisional Patent Application for:

System and Method for Managing Power in Integrated Circuits

TERM USAGE:

For the purposes of this presentation, an integrated circuit means an electronic device instantiated into silicon and/or related manufacturing materials, as known in the art. Used by way of example in this presentation is that form of integrated circuit often referred to as an "SOC," which may be any of:

- A system on a single chip, as the term is currently used in the art,
- Or a multi-chip system in a single chip package (including but not limited to those chips referred to as a CSP or SIP or MCM) , as known in the art,
- Or other muti-chip or single chip system (such as a processor with attached memory system) as known in the art.

For the purposes of this presentation the term "CPU" is intended in the generic sense to include all types of processors of which there may be multiplicity present in an SOC.

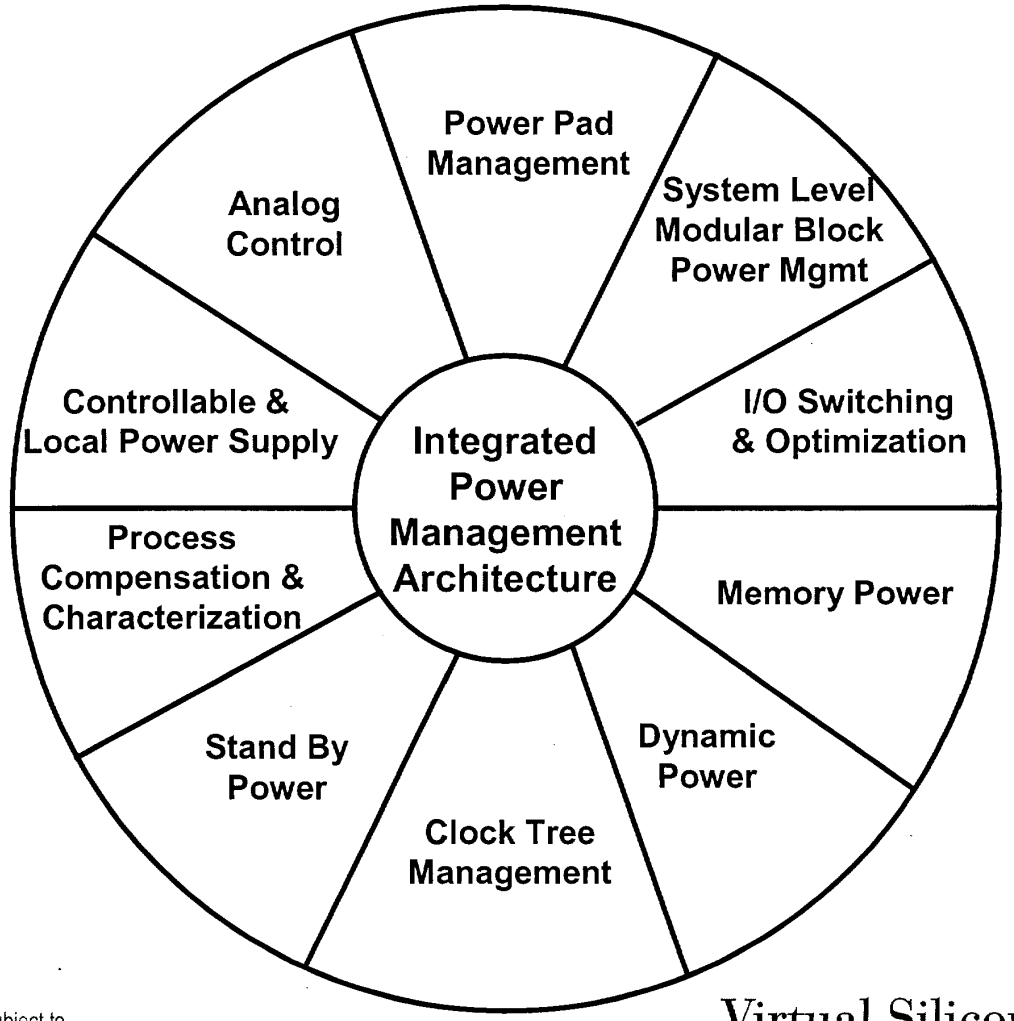
For the purposes of this presentation the term "IP" is used the same way as in the Chip design business, I.e. to refer to a block of circuitry performing a function.

For the purposes of this presentation the term "Tool" refers to a either an software program or a script (or series of scripts) controlling one or more software programs. These programs and scripts may be either standard ones as known in the art or new ones designed to perform specific functions as called out in this presentation. The term "EDA Tool" has the same meaning as "Tool" but the software is programs that perform electronic design automation. The term "Development Tool" has the same meaning as "Tool" but the software is programs that assist in the development of software or firmware. The term "Configuration Tool" has the same meaning as "Tool" but the software is programs that assist in the configuration of the power system.

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SVSC-0946-2005

Opportunities For Power Management in a System such as a Processor, SOC, SIP, CSP, or etc.



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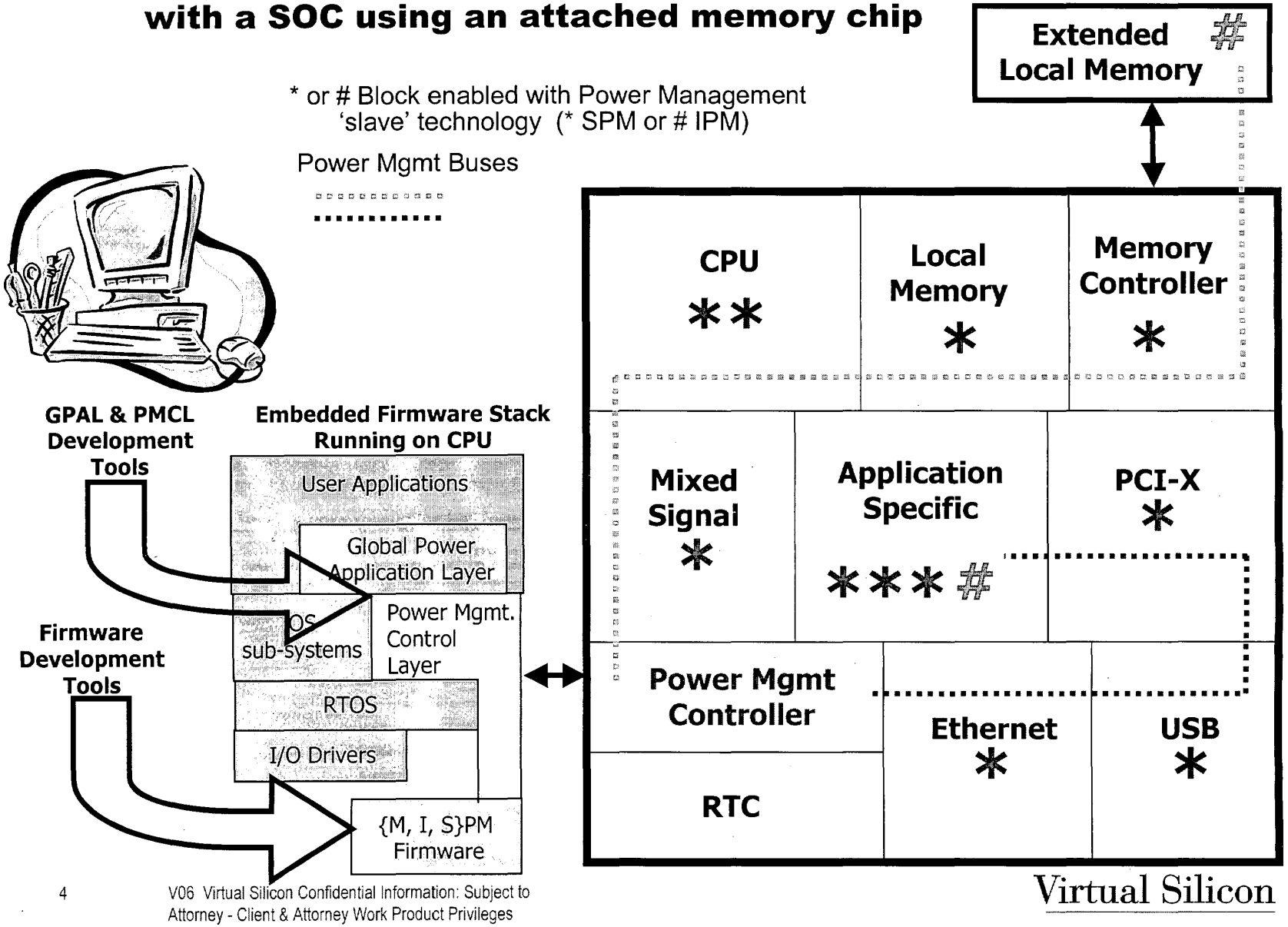
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- Integrated Power Management Architecture
  - Power Management SW in one or more of: drivers, PMCL , apps, etc.
  - What if analysis tools
    - Trade offs for dynamic and standby vs power,area,etc
- System Level Module Block
  - Save & restore of module state, use existing scan chains, to read or write the module state and present it to the processor for save or get it from the processor for restore
  - Special High Vt or variable Vt registers/latches and ability to create powered sub-islands in a powered off voltage island.
  - Clock rate change
  - Sentry/wake up control blocks
- Controllable & Local Power Supply
  - Fine tunable voltage regulators
  - Multiple power domains
  - Power switches (distributed minis)
  - Power mux'ing
- Power Pad Management
  - On/off power branches to modules
  - SSO/SSI analysis
  - Pad placement tool
  - Power Supply library
- Analog Control
  - Provide power state digital signals (run, standby, sleep, deep sleep, off)
- I/O Switching & Optimization
  - Minimize crowbar current
  - PVT control
  - Resistance control
  - ESD (SCR) smaller
- Memory Power
  - Distributed bank control & decode
  - Low power architecture
  - Voltage islands
  - Low power bit cells
  - Change access time (slower => lower power)
- Dynamic Power
  - Voltage islands
  - Feedback drivers
  - Low power FF
  - Low drive cells
  - Multi phase clock
- Standby Power
  - Low leakage cell
  - Back bias substrate
  - Voltage islands
  - Split rails
  - Longer channel length
- Clock Tree Management
  - Gated clocks
  - Micro PLLs in each block
  - Variable clock frequency
  - Clock mux'ing and localized clock divide
  - Better placement
- Process Characterization & Compensation
  - Change voltage based on process & temp
  - Characterize library at ultra low voltages

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SAMSUNG EXHIBIT 1005

Example of system Level Power Management Architecture with a SOC using an attached memory chip

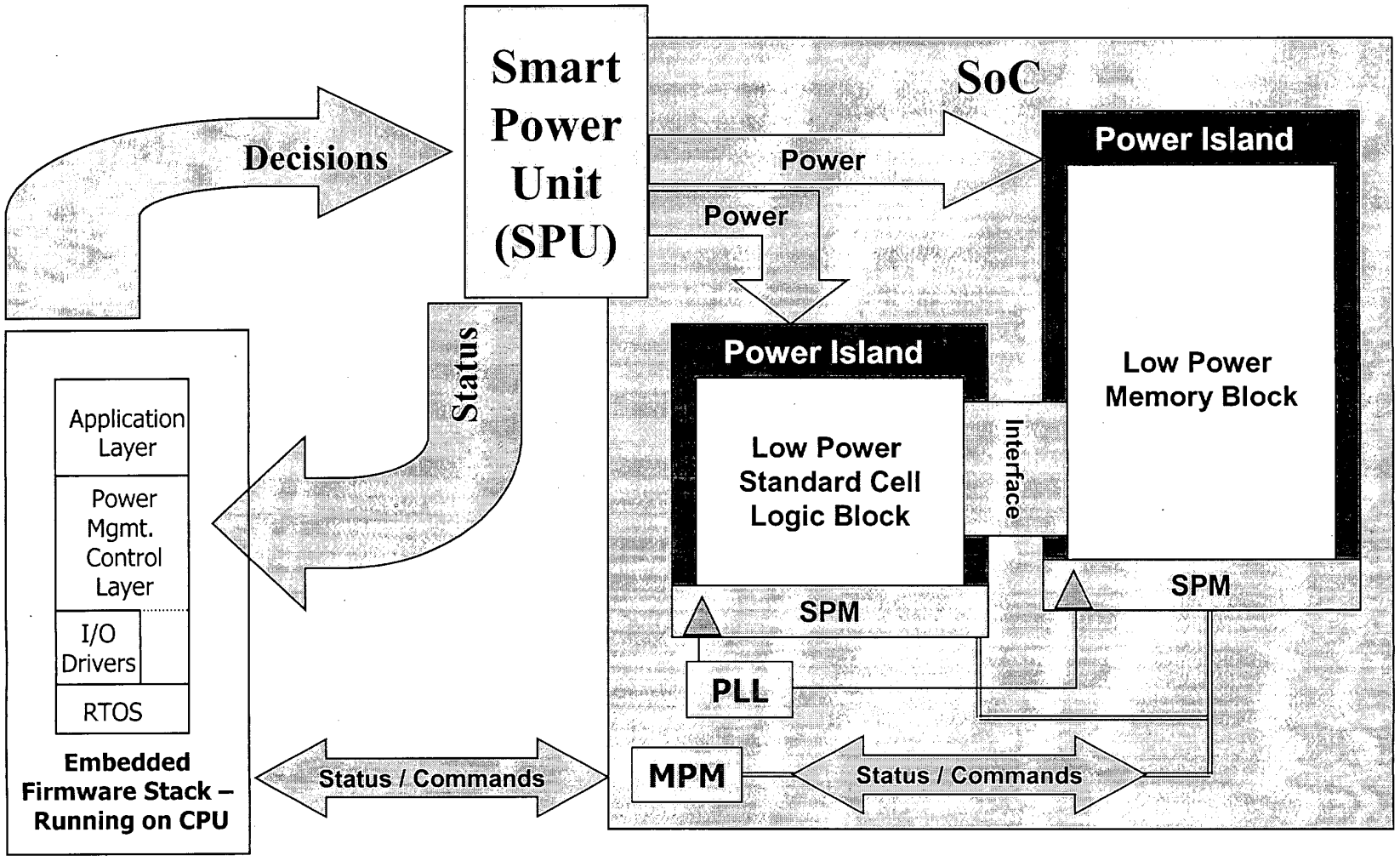


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Exhibit 2150, p. 9 of 48

Solution: Functional Level, with optional SPU



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SYNOPSYS, Inc. Exhibit 2045, Page 7 of 45

Methodology and IP based solution for power management and reduction

- SoC Architectural partitioning to **Power Island**
  - Functional & Geographic hierarchy
  - Voltage islands
  - Islands of Synchronicity (locally synchronous), typically asynchronous between islands, but can add special logic to detect when different islands can run synchronously and allow for it without all of the asynchronous overhead.
  - Should maintain strong overlap between types of hierarchy
  - Islands can have individual clock and optional dynamic back bias controls
- Hardware IP
  - Slave (client) Power Manager (SPM) for each island
  - Master Power Manager (MPM) to control SoC power behavior
  - Power Smart Foundation IP
    - I.e. Level shifting, Signal isolation, Vdd mux'ing, Clock mux'ing, dynamic back bias.
- Software IP help centralized control for decision making
  - APIs and bus standards to communicate power (control) information between the SPM and power control software
  - Command Level Interface (CLI) between SPM and MPM
  - Policy based power schedule
- Power regulation
  - Off-chip DC/DC conversion, or
  - On-chip voltage dropout regulator
- Island-Autonomous implementation of power management
  - Independent power and clock distribution to islands
  - Plug and play

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SDV-OSD-2nd-Spring

- On-Chip IP and Components
  - Power Island
  - Slave Power Manager (SPM)
    - Wrapper. Control and coordinate Power behavior of each island
  - Intermediate Power Manager (IPM)
    - Coordinates a number of SPMs on behalf of an MPM
    - Optionally can control and coordinate power behavior of a portions of the area controlled by a MPM
  - Master Power Manager (MPM)
    - Control and coordinate power behavior of SoC, or in some cases part of (multiple MPMs)
    - In some applications, the functionality/circuitry of the MPM may be integrated with a CPU
  - Power Command Bus
- Software
  - Command APIs
    - Communication between SPM, IPM, MPM and PMCL
  - Power Management Control Layer (PMCL)
    - Firmware used to provide power control facilities, and optionally power control, to the application layer
  - Application Layer
    - Where decisions are made about power schedule or requests for levels of performance are make to the PMCL
- Off-Chip IP and Components, may include
  - Smart Power Unit (SPU)
    - External unit used to control power and clock distribution to SoC
- Foundation IP
  - Requirements and support

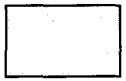
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Islands: SPM and MPM



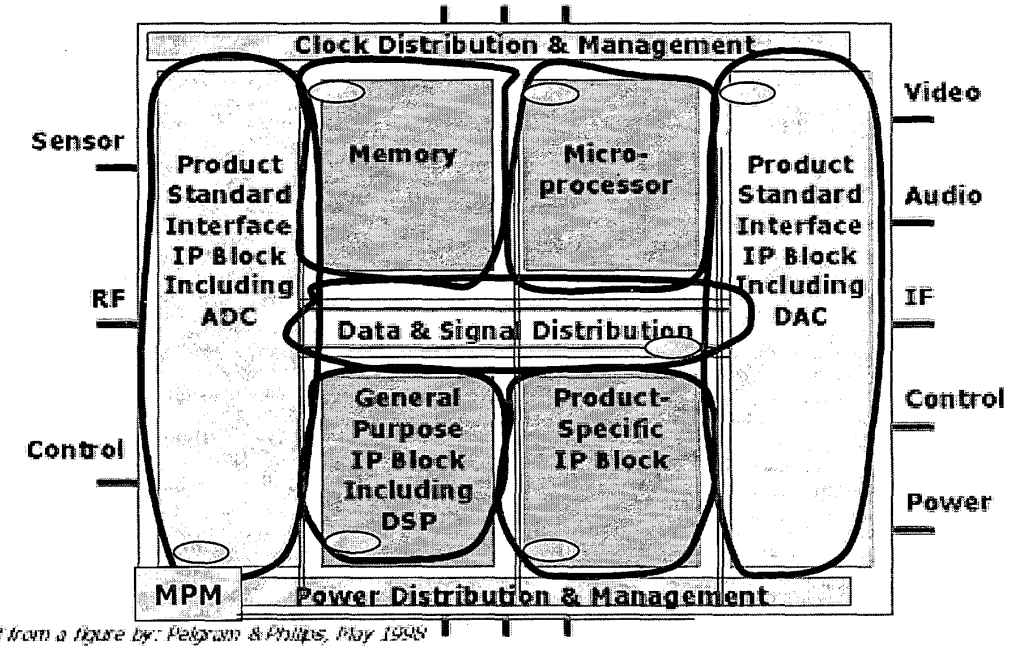
SPM Block



MPM Block

- Each Power Island includes a Slave Power Manager (SPM) IP Block
  - Normally small: low gate count
  - Fully integrated into design and implementation flow
- Each SoC has at least one Master Power Manager (MPM)
- SPM blocks are optional and may be "folded" into the MPM in some cases.
- All communication between a MPM and separate SPMs (or IPMs) is command based, commands are issued by the MPM or an IPM and executed by the IPMs or SPMs
- SPMs and IPMs may report status back to the MPM or other units.

Additionally one or more units known as IPMs (an Intermediate Power manager) may be used to coordinate a number of SPMs. The typical use of an IPM is control of the SPMs on a separate chip from the MPM(s) that the IPM reports to.



Adapted from a figure by: Philips & Philips, May 1998

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SPM, IPM and MPM are typically connected using simple logically serial bus, with optional error detecting functionality, such as parity or a redundant code.

SPM

- Commands to/from MPM
- Information collection & delivery
- Level conversion for signals

IPM

- If present acts as an intermediary between a group of SPMs and MPMs
- May include any combination of functionality from either a MPM or a SPM
- May act as in intermediate data collection and reduction point between a MPM and a group of SPMs
- For a multi-chip complex, for example the working memory for the SOC is on a 2nd (slave) chip, an IPM would be the normal interface to the primary chips MPM.

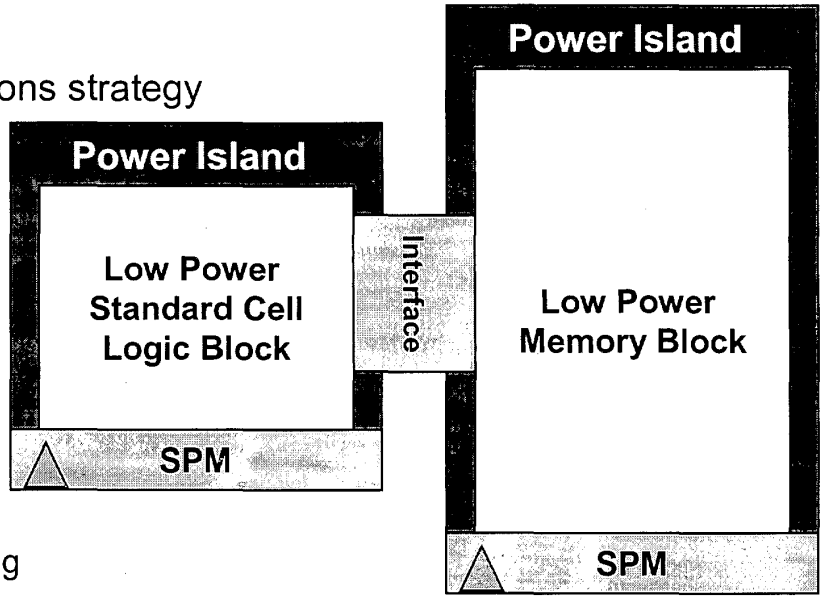
MPM

- Acts as a distribution center
- Accepts and sends commands
- Collect and transport information
- May make intelligent power trade-off between IPMs and SPMs under it's control

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Power Islands

- Independent sections of an SoC; Typically one or more functional unit
- A power Island is typically locally synchronous, but globally asynchronous
  - Functional communication between Islands using signal buffers, and memory
- Island may employ different (and additional) techniques in implementation of power reductions strategy
  - As appropriate for a each Island, such as:
    - Clock gating
    - Dynamic Clock selection
    - Dynamic Vdd selection, ie voltage is variable
    - Dynamic Leakage control, for example variable Vt transistors



- Each Island can support multiple clock domains, each with it's own control
  - Clock may be variable
  - May use Multiple PLLs with optional clock dividing
    - Either local, remote or both
- A Power Island may contain sub-Islands.
  - A sub-island by remain powered on even if the Power Island is powered off Normally used for saving state.

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SNPS0004-0000004-0000

Slave Power Manager (SPM)

- IP block that coordinates the power behavior in Power Island
  - Including SPM hierarchy
  - Normally includes Signal buffering, Level shifting and signal isolation
- Easy to implement and integrate
  - Normally Integrated into Scan chains
  - Normally Very small foot print, low gate count and low power
- Uses command interface to communicate status and commands
  - Recognizes it's address, allowing multi-drop bussing
  - Command Examples:
    - Load, Sleep, Idle, etc
  - Service requests (from other resources)
- Registration of capabilities:
  - Either at power-up – using call back registration (typically used for off chip SPMs and IPMs),
  - or Static when the SoC is generated (Typically used for on chip SPMs
    - What can this block (SPM) or set of blocks (IPM) do
    - What type of commands this block (SPM) or set of blocks (IPM) can service
- Abilities, optional
  - Save and restore (for power off periods)
  - Watch-dog timer(s)
  - Debug interface coordination to Island
  - Local State monitoring, information collection
  - Local control of: Vdd, Clocks (frequency selection), Dynamic back baising
- Optional ability to check locally collected information against a threshold or range (normally programmable) and optionally report if it exceeds the threshold or falls out of a range. This may be a multi level test where the conditions must occur at greater then a given (normally programmable) frequency or exceed a given duration (normally programmable), to be reported either asynchronously or solicited. Note that if it falls below the level where it would be reported asynchronously it may still be reported in the next solicited report.

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SAMSUNG EXHIBIT 1009

Examples of SPM control/configuration information

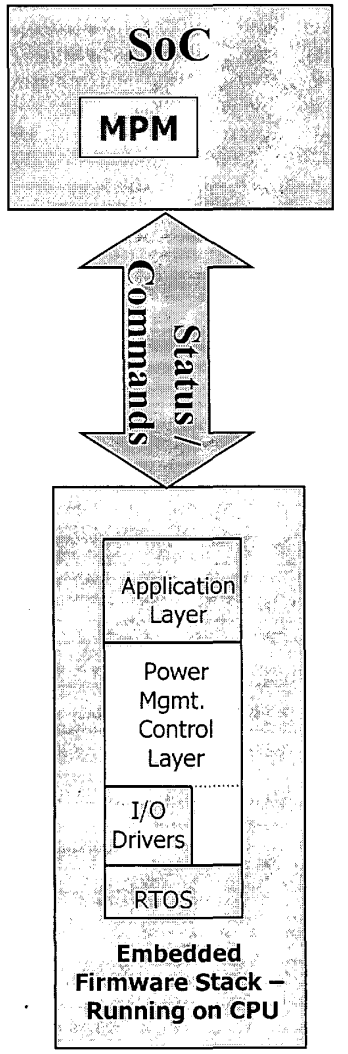
- SPM address (hardwired)
- Voltage Control, examples
  - Vdd mux: Source values are specified with associated performance loss
  - Vdd fixed to Power (pin/bus) N
  - Vdd fixed to Power (pin/bus) N but has power off option
  - Vdd fixed to Power (pin/bus) N but has power off and fixed voltage drop options (amount of drop is specified, along with associated performance loss)
- Number of clocks (Note: could be 0 for a totally asynchronous unit)
- Clock Control (per clock), examples
  - Clock mux: Source values are specified
  - Clock fixed to line M
  - Clock has own PLL(s) (specifications supplied)
  - Clock can be single (multi) stepped for logic analyzer functionality
- Dynamic back bias
  - Not supplied
  - Vt Steps and associated performance loss
- Local state monitoring, with either asynchronous or solicited reporting
  - Data collection quantum size (normally in cycles)
  - Types of information collected.
    - Local temp, local Vdd, performance of local ring oscillator, number of clock gated cycles, etc.
  - Size and configuration of report, optional programmability of report aspects.

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SYNOPSYS 2004 0946

Master Power Manager (MPM)

- SoC global power behavior manager
  - Collects all information from SPM
  - Command distribution
- Main interface to PMCL firmware
  - Send / provide status to SW
  - Use SoC main bus
  - Use memory mapped commands
  - Registration with PMCL
    - Each SPM/IPM
    - Capabilities
- Optionally able to Read/Write scan chains for state save and restore along with local logic analyzer ability
- (In some applications, the functionality/circuitry of the MPM may be integrated with a CPU)



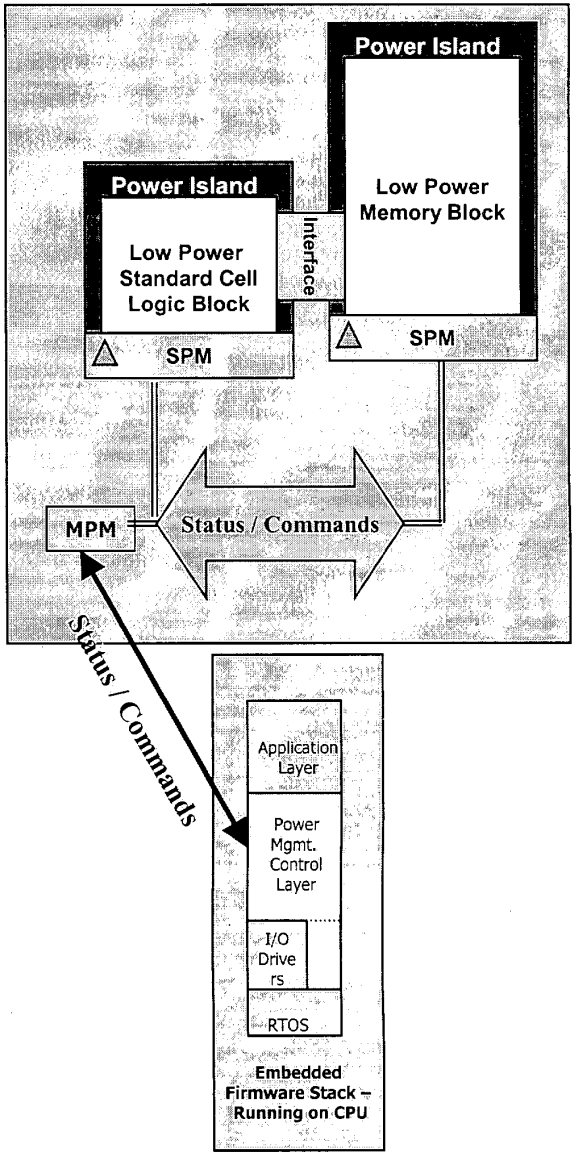
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SAMSUNG-2019-00005

Command API

- MPM / IPM / SPM Protocol
  - Actions (examples)
    - Sleep / Idle
    - Step down / Step up
    - Start / Save / Restore
    - Timer / Timeout / Wait
  - Data & Registration
    - Idle levels / Step levels
    - Timers
    - Save / Restore
  - Very low level – Not visible to user
- MPM and PMCL Commands
  - Software callable commands
    - Memory mapped
  - Operate at Power Island level



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SNPS_VSI_0000016

Power Command Bus

- Logically a simple multi-drop serial bus, that may cross chip boundaries, used to connect the SPM(s) to an IPM or a MPM and IPM(s) to a MPM.
- Typically a combination of serial busses, one per region of the chip and then multi-drop within the region. Note however that nothing prevents the use of parallel buses or a mix of the two. Or any other form of "bus" as known in the art.
- Message is at least a unit ID with associated payload, unless the link is a fixed point to point bus, then no unit ID is required, only a payload.
- Optionally uses an error detection scheme such as parity, ECC or an redundant code.
- Low performance bus
  - Does not interfere with the design
  - Not visible to the user (as the system software level)
- Communication between MPM and PMCL is, normally memory mapped, and based on the SoC main bus (AHB, for example). But can also be implemented in other forms as known in the art.
- Some systems may elect to implement a separate status reporting bus (like the Power command bus) that is used to provide asynchronous "Alert" type status messages from SPMs (and IPMs) that belong to the MPM.

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Examples of Power Command Bus Message Formats

Basic format:

- Start of message indicator
- SPM (or IPM) Address, typically 7 bits (normally individual power command busses have 127 or less drops)
- Type code, typically 5 bits (only 4 bits used, msb is 0)
- Basic command, between 1 and 4 nibbles (4 to 16 bits) depending on type
- End of message indicator

Extended format:

- Start of message indicator
- SPM (or IPM) Address, typically 7 bits
- Type code, typically 5 bits
- Basic command, between 1 and 4 nibbles (4 to 16 bits) depending on type
- Additional length, typically 8 bits
- Additional information
- End of message indicator

Response message format:

- Start of reply message indicator
- SPM (or IPM) Address, typically 7 bits
- 3b ACK or NAK or Return status (implied ACK) (one hot)
- Optional payload length for Return status messages , typically 8 bits
- Optional payload for Return status messages
- Optional reason code for NAK, typically 6 bits
- End of message indicator

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Exhibit 2018, Page 18 of 25

Power Command Bus Error handling

- If an SPM or IPM times out on replying to a command, the MPM (or IPM) will reissue it a programmable number of times then if it still fails the MPM will report back the failure to the PMCL and will mark the SPM or IPM as unusable.
- The PMCL may have the MPM reinitialize the failing SPM or IPM via the scan system and then retry sending the message.
- Other conditions such as invalid responses to commands or invalid status reports are also handled by re-initialization

In all cases the state of the failing SPM or IPM may be read out and saved for (later) analysis.

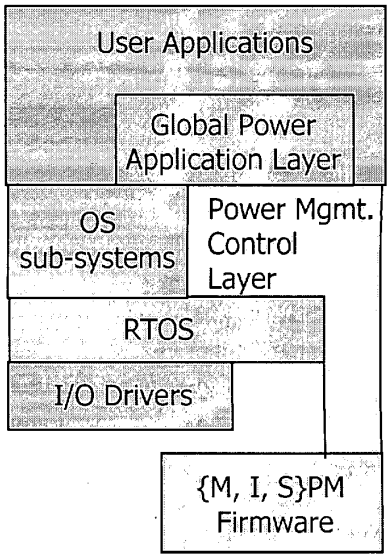
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Power Management Control Layer (PMCL) and Global Power Application Layer (GPAL)

- Power management software layers
  - Optional Global Power Application Layer for more complex applications
  - If GPAL is present then all "PMCL" API calls are actually first routed to the GPAL.
- Where decisions are made about power management of SoC
  - When both layers present the PMCL makes local decisions under guidance from the GPAL
- Can include complex algorithms of static schedule (or no schedule)
- Provide facility to user code to interact and control power behavior and parameters
  - Database & Statistics
- Decision making
  - What is the load at each island
  - Build a history and database
  - Provide data: Demand on resources
- PMCL: Collect information from MPM and convey commands to MPM
  - Change the state of one or more SPMs and IPMs
    - Power off, power on, change power level, change frequency, etc.
- Application (SoC) specific
- Responsible for Communication with SPU (if there is one)
  - Implementation of power policy
  - Collection of information on actual power supply
- Provide sockets for existing power management techniques

Embedded Firmware Stack Running on CPU



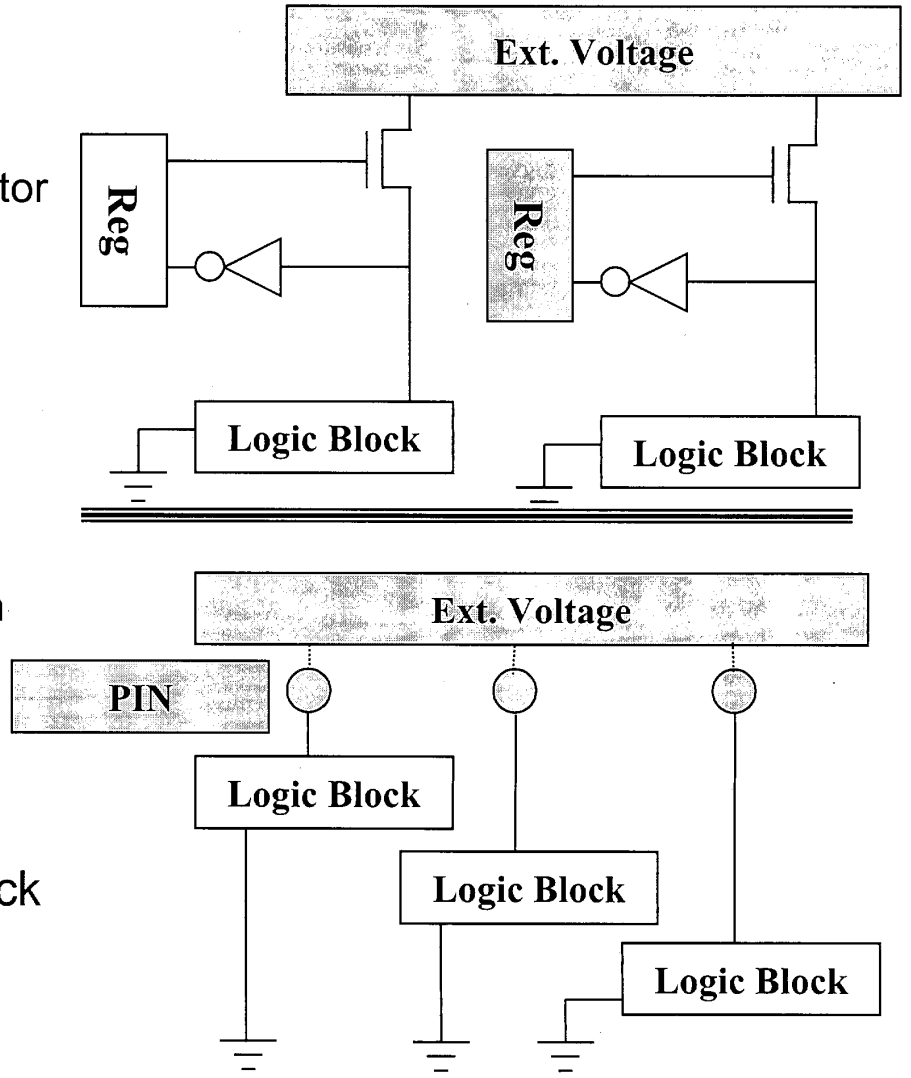
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Smart Power Unit – Example Configuration

- Several options
  - Internal: Dropout Voltage regulator
  - External to SoC :DC/DC Conversion
- DC/DC conversion
  - Provide multiple independent power supply pins
  - Variable Voltage supply on each separate power pin
    - Within range and in steps
  - Controlled by PMCL
- Not normally responsible for clock distribution

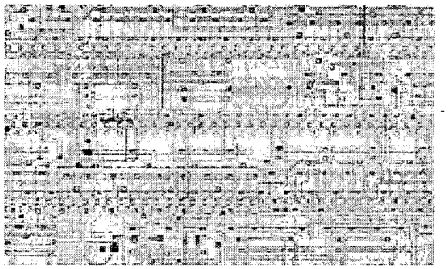


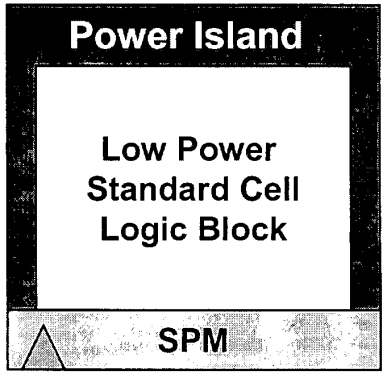
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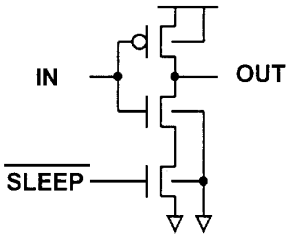
SNPS_0000_0000

Foundation IP – Standard Cell Library

- Standard Library Cells
  - Normally optimized for low power
  - Characterized over a range of operating voltages
  - Synchronous circuits and optionally asynchronous circuits
  - Static circuits and optionally (encapsulated) dynamic logic circuits
  - Multiple voltage domain interface circuits
    - Level Shifters & signal isolation circuits
  - Multi-threshold design & characterization
    - Standard Vt, High Vt, Low Vt, and variable Vt circuits
    - High Vt thick oxide circuits
  - Data retention (shadow) circuits
  - Anti-glitch circuits
  - Low leakage "Sleep" circuits





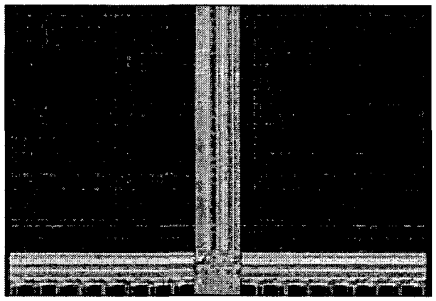


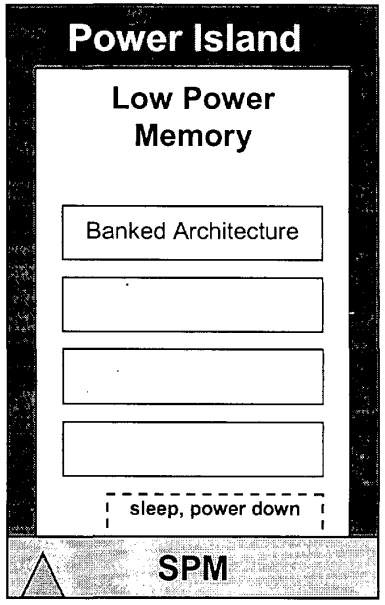
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SAMSUNG Exhibit 1015 Page 0022

Foundation IP - Memories

- RAM & ROM
  - SRAM compilers (single-port, 2-port, dual-port)
  - ROM compilers
  - Optimized for low power
  - Multiple bank architectures (via compiler)
  - Supports low power modes
    - sleep, nap, full power down
  - Programmable R/W ports
  - Synchronous & Asynchronous design
  - Architecture coupled with Power Island



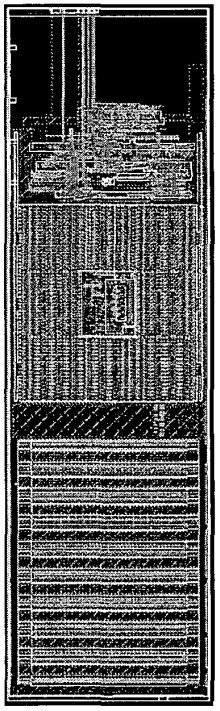


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Foundation IP – I/O, Mixed Signal

- IO
  - Optimized for low power
  - Power off/down mode(s)
  - Controllable output slew-rate
- PLLs (Phase-Locked Loops) and DLLs (Delay-Locked Loops)
  - Compiler-based
  - Localized and dynamically controllable
  - Voltage controlled, software and/or firmware controlled
  - Sleep mode
- Power Functions
  - Embedded power controllers
  - Embedded voltage regulators
    - Analog regulator
    - Digital regulator
- Clock and Vdd Muxes
  - Localized and dynamically controllable
  - Voltage controlled, software and/or firmware controlled



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EDS/DSD: 2th/28th/09

Design Flow

- Partition SoC to Power Islands
  - Vdd pins
  - Clock distribution
- Instance wrapper SPM for each block
  - Manifest signal interconnect between blocks
  - Power supply for each power blocks
  - Provide static registration information on abilities of the SPM to the MPM or IPM unit
- Initiate dynamic registration of callback of ability at IPM generation.
- Instance MPM(s) and IPM(s) in SoC
  - Instance power command buses
- PMCL
  - Build into the boot sequence
  - SoC specific – build the database of SPM/IPM/MPM abilities across all chips
  - Implement power control policy

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Sample Flow from Application request to SPM action:

- Application is invoked to perform action X (I.e. show a movie) , which it determines requires N MHz of performance from IP unit Y (I.e. an MPEG decoder) Note if the unit in question is totally asynchronous then "N MHz" will be an artificial measure of required performance. Or if there are multiple clocks involved the minimum performance for each would be specified.
- Application then invokes the PMCL API call "Set_Rate(unit Y, N MHz, Degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM tradeoffs, starting back bias for SPMs with dynamic bias, wait for power up flag)", this other information for example could be "no power off, use high Vt and clocks off instead" and "Major waits are about 10 us, with a 400ns threshold". For units with multiple clocks a varent of the call would be used that allows the application to specify all required frequencies.
- The PMCL code (or the MPM or IPM, as desired) looks at the possible tradeoffs available for the unit and selects a MHz rate, Vdd and if applicable Vt for the unit (or for different portions of the unit) that best meets the given requirements and determines the applicable SPM(s). (For multiple clock cases the Vdd & Vt would the ones that allow all specified clocks to meet or exceed their required frequencies)
- The PMCL code then writes the desired setting for the SPM(s) to the MPM (or IPM). The MPM (or IPM) then converts the request into one or more commands for the SPM(s) (or IPM) associated with the unit.
- If the application sets the wait for power up flag and the unit is not powered up then the PMCL will wait until the unit has fully powered up before returning from the call, otherwise the call returns as soon as the command is "ACK'ed", with status of 0 (ok), 1 (fast power-up), 2 (slow power-up) or 3+ (error conditions). Note powered up in this context is the unit is at the desired Vdd for the requested MHz, not just the unit is turned on.
- The MPM (or IPM) sends the request(s) to the appropriate target(s) and waits for "ACKs", indicating message received and executed (or execution has begun). Note a "NAK" with an error code is the other possible return from the SPM(s).
- The SPM(s) that eventually receives the command(s) then perform actions as required to implement the actions; such as switching a Vdd mux, a Clock mux and changing the Vt on the associated transistors. After which it returns status (ACK or NAK) upstream.

Sample Flow from Application request to SPU action:

- Application is invoked to perform action X (I.e. show a movie) , which it determines requires N MHz of performance from IP unit Y (I.e. an MPEG decoder)
- Application then invokes the PMCL API call "Set_Rate(unit Y, N MHz, Degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM tradeoffs, starting back bias for SPMs with dynamic bias, W4PU)", this other information for example could be "no power off, use high Vt and clocks off instead" and "Major waits are about 10 us, with a 400ns threshold".
- The PMCL code (or the Global Power Application, as desired) looks at the possible tradeoffs available for the unit and selects the lowest Vdd that will support the requested MHz. Then the PMCL code determines the SPMs (and IPMs) that will be affected, and which power PIN(s) to change.
- It then sends a command to the MPM to have the SPMs (and IPMs) prepare for a Vdd change. And waits for the ACK from the MPM.
- Then the PMCL sends a command to the SPU to change the Vdd on the selected power PIN(s), and waits for a the affected area to "settle down".
- The PMCL then sends a "resume operation at freq N MHz" command to the MPM, the MPM propagates the resume command to all affected SPMs (and IPMs). Depending on the configuration either the MPM or one or more IPMs or SPMs will handle setting the freq to N MHz. Unit operation resumes after the clock has settled.
- Note that again the User application has the option of waiting for the entire operation to finish or to continue and either query the PMCL as to the progress of the operation or wait for a "finished" interrupt from the PMCL.

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Example Flow of a "Hot spot" report from an IPM to the PMCL/GPAL:

- An IPM in the course of monitoring temperature statistics from its SPMs "sees" that the mean temperature has exceeded a predetermined (and programmed) threshold. At which point it builds a problem ("HOT SPOT") report message and waits for the next status query from the MPM. Note as an option a logically separate "bus" could be provided for (asynchronous) status reports to the MPM.
- The MPM receives the "HOT SPOT" report and depending on it's internal logic may either wait for further confirmation (I.e. see that the "HOT SPOT" lasts past a predetermined threshold) or immediately take action. Normally this action will consist of posting an interrupt to the PMCL that it needs attention or if the PMCL queries the MPM often enough an interrupt may not be needed.
  In some cases the MPM (or even an IPM) maybe allowed to make a local trade off and perform the action, or order the action to be performed, to fix the "problem. Such as lowering the operating frequency of the "HOT SPOT" area. In this case both the problem and it's fix should be reported "upstream".
- When the PMCL reads the (modified) "HOT SPOT" report from the MPM it may either decide what action to take to fix the problem it's self or may "kick the problem upstairs" to the GPAL. In either case the software will make the tradeoff required to fix the problem and the PMCL will issue the appropriate commands to the MPM(s). If the GPAL determines the high level fix, it will then send it to the PMCL to be converted into MPM commands, etc.
- The PMCL will after a time monitor the the problem area to insure the problem has been fixed.

Note: this type of functionality can also be provided at other levels, such as the PMCL, in which case the PMCL will query (via the MPM) all SPMs that have the desired measurement ability (and IPMs) as to their local conditions and can then, for example, build a "map" of power usage that it can then act on.

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Example Flow of saving a units state prior to powering it off then restoring it after power on:

- A user application requests that the PMCL power off a unit X, but wants the state saved and restored, as it takes a long time to configure the unit. This request is normally accompanied by the address of an area to save the state to.
- The PMCL sends a "stop clocks and read Unit X state" message to the MPM which propagates it to the SPMs of the affected unit. After it gets the "ACKs" back, it uses the Scan chain(s) for the unit (or that contain the unit) to read the state into a register or buffer for presentation to the PMCL If the PMCL provided the MPM with the address of the save area the MPM will write the state directly into the area. Otherwise the PMCL can read the information from the MPM in fixed or vbl. Sized units, normally the word size of the processor the PMCL is running on, then the PMCL saves the information into the area.
- After all of the units state been saved the PMCL sends a "Power off unit X" message to the MPM, which propagates it out.
- The PMCL returns the save state area to the user application, now containing the state of the unit.
- Later the user application can request that the PMCL power the unit X back up and restore the state. This request would be accompanied by the address of the area the state was saved to.
- The PMCL will send a "Power up Unit X with clocks off and restore it's state" message to the MPM which propagates it to the SPMs of the affected unit. After the unit has been powered up either the MPM will again use the scan chain(s) to reload the units state, either directly from the save area or from information passed to it piecewise by the PMCL.
- Once the unit has had it's state reloaded, the PMCL can tell the MPM to have it's clock(s) turned back on and report back to the user application that the unit is ready to continue operation.

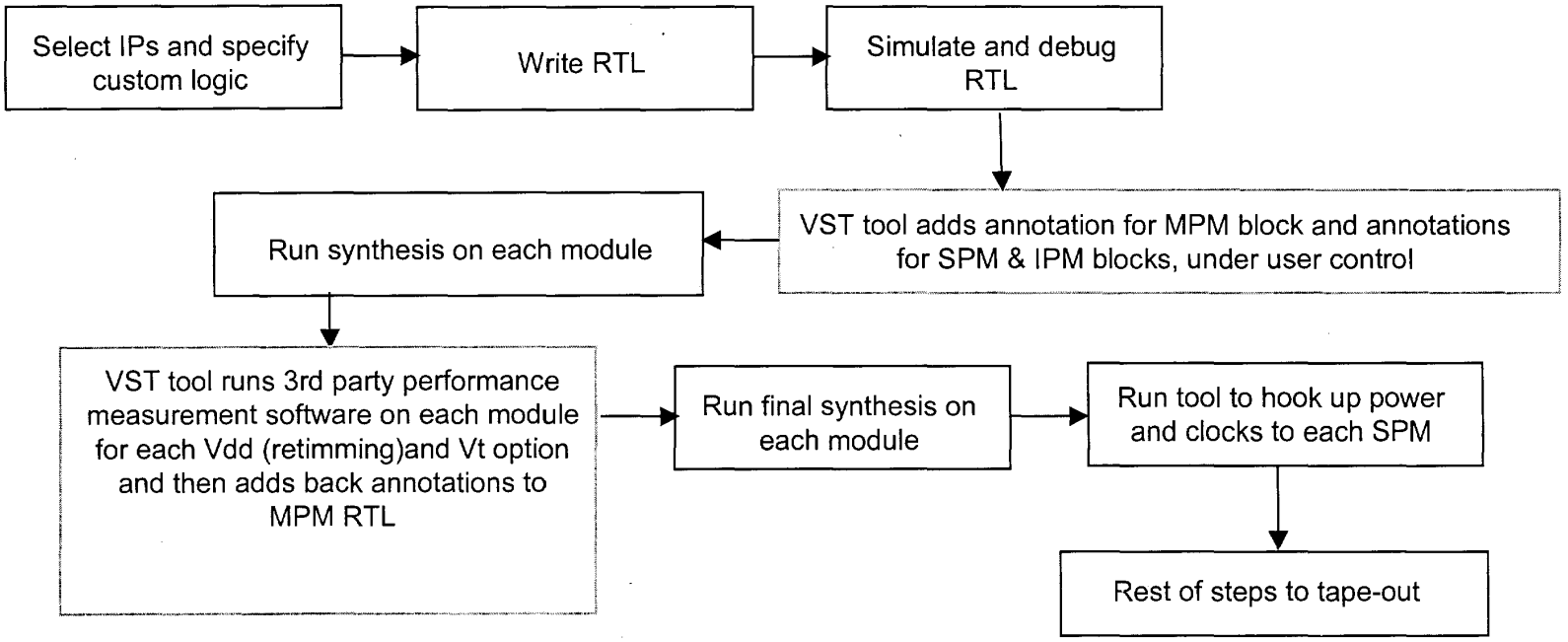
Side note: This same functionality can be used to implement an internal "logic analyzer" function, in which case the unit in question would not be powered down after being read. Also if the associated SPM(s) has the ability single (multi) step the clock then in effect local "SCAN" testing can be performed by having the SPM(s) "signal isolate" the unit; then using a combination of the ability single (multi) step the clock with the ability to use the scan chain(s) to read/write the units internal state.

Example 1 Flow of how to build a chip using this technology

- Select IPs and specify custom logic that will be used to build the chip
    - Specify for each piece things like maximum and sub clock rates and % idle time, min & max Vdd
- At some point in writing the RTL add the proper annotation for MPM block(s) and if needed IPM block(s)
    - Specify the desired functionality options
- Either as the RTL is written for each module or afterwards; the RTL needs to be annotated with SPM configuration information on a per module basis. There are a number of ways to do this including:
    - Insert proper annotation by hand on a per module basis as or after the RTL is written
    - Create a separate table (in the proper format) with the module names and respective annotations.
    - Use the VST supplied tool to interactively build the separate table
- Additionally the above procedure will also be used to specify which optional functionality is desired per SPM block.
- Except where all modules were annotated by hand, then run the VST supplied tool to add the proper annotation to the un-annotated modules in the RTL, using information from the table (can be done automatically from the VST tool).
- Synthesize the design on a power island basis (don't mix islands)
- Optionally measure the performance of design at all desired voltages and optionally Vt combinations, a VST supplied tool derives the actual MHz to Vdd (& Vt) tables for each SPM and back annotates the RTL (provides the table(s) needed by the MPM and IPM(s) of SPM characteristics.
- Run final synthesis on the design on a power island basis (don't mix islands)
- Route modules separately or by SPM (VST supplied tool can do this)
- Attach each module to the proper power and clock connections (VST supplied tool can do this)
- VST supplied tool generates the finished net-list with all information

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Example 2 Flow of how to build a chip using this technology



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