

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

IPR2025-01210

U.S. Patent No. 7,632,751

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,632,751**

TABLE OF CONTENTS

EXHIBIT LIST	v
LIST OF CHALLENGED CLAIMS.....	viii
I. RELIEF REQUESTED	1
II. STATE OF THE ART	1
A. Interconnects and Dual Damascene	2
B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength.....	4
III. THE '751 PATENT.....	6
A. Overview	6
B. Prosecution History	8
C. Claim Construction.....	8
IV. ORDINARY SKILL	8
V. PRIOR ART	9
VI. DETAILED EXPLANATION OF GROUNDS	9
A. GROUNDS 1A/1B: Watanabe anticipates (Ground 1A) and renders obvious (Ground 1B) Claims 1-2, 5-8, 10-13, 18, and 20.....	9
1. Watanabe	10
2. Claim 1	14
3. Claim 2	28
4. Claim 5	32
5. Claim 6	33
6. Claim 7	35

7.	Claim 8.....	37
8.	Claim 10.....	38
9.	Claim 11	40
10.	Claim 12.....	42
11.	Claim 13.....	44
12.	Claim 18.....	46
13.	Claim 20.....	46
B.	GROUND 2: Watanabe combined with Kamoshima renders Claims 3-4 and 15-16 unpatentable.....	50
1.	Kamoshima	50
2.	Claim 3.....	51
3.	Claim 4.....	55
4.	Claim 15.....	56
5.	Claim 16.....	56
C.	GROUND 3: Watanabe combined with Kamoshima and Fukazawa renders Claim 17 unpatentable.....	57
1.	Fukazawa	57
2.	Claim 17.....	58
D.	GROUND 4: Watanabe combined with Iizuka renders Claim 9 unpatentable.....	62
1.	Iizuka.....	62
2.	Claim 9.....	62
E.	GROUND 5: Hasunuma anticipates Claims 1, 5-6, 9, 11-14, and 18-19.....	64
1.	Hasunuma.....	64

2.	Claim 1	66
3.	Claim 5	72
4.	Claim 6	72
5.	Claim 9	73
6.	Claim 11	75
7.	Claim 12	76
8.	Claim 13	77
9.	Claim 14	79
10.	Claim 18	80
11.	Claim 19	81
F.	GROUND 6: Hasunuma combined with Kurashima renders Claims 2 and 20 obvious	83
1.	Kurashima	83
2.	Claim 2	85
3.	Claim 20	90
G.	GROUND 7: Hasunuma combined with Watanabe renders Claims 2, 8, and 10 unpatentable	94
1.	Claim 2	94
2.	Claim 8	95
3.	Claim 10	97
H.	GROUND 8: Aoyagi renders obvious Claims 1, 3-4, 7, 14-16, and 19	100
1.	Aoyagi	100
2.	Claim 1	104

3.	Claim 3	112
4.	Claim 4	115
5.	Claim 7	116
6.	Claim 14	117
7.	Claim 15	118
8.	Claim 16	120
9.	Claim 19	121
I.	GROUND 9: Aoyagi combined with Fukazawa renders Claim 17 unpatentable.....	124
1.	Claim 17	124
VII.	GROUNDS FOR STANDING	130
VIII.	MANDATORY NOTICES AND FEES	130
A.	Real Party-In-Interest	130
B.	Related Matters.....	130
C.	Counsel and Service Information.....	131
D.	Payment of Fees	131
IX.	CONCLUSION.....	132

EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,632,751
1002	File History of U.S. Patent No. 7,632,751 (“’751 File History”)
1003	Declaration of Dr. Reinhold Dauskardt
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. (“Watanabe”)
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. (“Hasunuma”)
1006	U.S. Patent Publication No. 2001/0019180 to Aoyagi et al. (“Aoyagi”)
1007	U.S. Patent No. 6,717,267 to Kunikiyo (“Kunikiyo”)
1008	U.S. Patent No. 5,250,465 to Iizuka et al. (“Iizuka”)
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. (“Kamoshima”)
1010	JP2002299437 (“Fukazawa”) and Certified Translation of Fukazawa with Certification of Translation
1011	U.S. Patent No. 7,042,099 to Kurashima (“Kurashima”)
1012	P. Andricacos, “Copper On-Chip Interconnections,” <i>Interface, The Electrochemical Society</i> , pp. 32-37, 1999
1013	U.S. Patent No. 5,885,857 to Yamaha et al. (“Yamaha”)
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi (“Igarashi”)

1015	U.S. Patent No. 6,717,268 to Hau-Riege (“Hau-Riege”)
1016	U.S. Patent No. 6,468,894 to Yang (“Yang”)
1017	U.S. Patent No. 6,022,808 to Nogami (“Nogami”)
1018	Reserved
1019	Kaanta et al., “Dual Damascene: A ULSI Wiring Technology,” <i>VMIC Conference</i> , IEEE, Jun. 11-12, 1991, pp. 144-152
1020	U.S. Patent No. 5,032,890 to Ushiku (“Ushiku”)
1021	Reserved
1022	U.S. Patent No. 6,582,976 to Watanabe (“Watanabe’976”)
1023	S. Middleman et al., <i>Process Engineering Analysis in Semiconductor Device Fabrication</i> , pp. 260-61 (excerpted), McGraw-Hill, 1993 (“Middleman”)
1024	U.S. Patent No. 6,156,660 to Liu et al. (“Liu”)
1025	U.S. Patent No. 5,798,298 to Yang (“Yang 2”)
1026	T. I. Bao et al., “90 nm Generation Cu/CVD Low-k ($k < 2.5$) Interconnect Technology,” <i>Digest. International Electron Devices Meeting</i> , San Francisco, CA, USA, 2002, pp. 583-586
1027	A. Loke, “Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects, Dissertation,” Stanford University (1999)
1028	K.N. Tu, “Recent advances on electromigration in very-large-scale-integration of interconnects,” <i>Applied Physics Review – Focused Review, Journal of Applied Physics</i> , Vol. 94, No. 9, pp. 5451-5473 (November 1, 2003)

1029	T. C. Huang, et al., “Numerical Modeling and Characterization of the Stress Migration Behaviour Upon Various 90 nanometer Cu/Low k Interconnects,” <i>Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)</i> , Burlingame, CA, USA, 2003 (added to IEEE Xplore 8-11-2003), pp. 207-209
1030	Reserved
1031	Reserved
1032	JP2000012688 to Nasu (“Nasu”) and Certified Translation of Nasu with Certification of Translation
1033	U.S. Patent Publication No. 2001/0030365 to Otsuka et al. (“Otsuka”)
1034	Wolf, Stanley, <i>Silicon Processing for the VLSI Era: Deep-Submicron Process Technology</i> , Lattice Press, 2002 (excerpted) (“Wolf”)
1035	U.S. Patent No. 6,858,944 to Huang et al. (“Huang”)
1036	Reserved
1037	Reserved
1038	U.S. Patent No. 6,215,189 to Toyoda et al. (“Toyoda”)
1039	U.S. Patent No. 6,238,850 to Bula et al. (“Bula”)

LIST OF CHALLENGED CLAIMS

Claim Element	Claim Language
1[pre]	A method for fabricating a semiconductor device comprising the steps of:
1[a]	(a) forming a first interconnect on a semiconductor substrate;
1[b]	(b) forming a first insulating film on the first interconnect;
1[c]	(c) forming in the first insulating film, a via hole connected to the first interconnect, a dummy hole which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench connected to the via hole and the dummy hole; and
1[d]	(d) depositing a conductive material in the via hole, the dummy hole and the interconnect trench, thereby forming a via, a dummy via and a second interconnect.
2[a]	The method of claim 1, wherein in the step (a) a first dummy interconnect is simultaneously formed on the semiconductor substrate, and
2[b]	in the step (c) the dummy hole is connected to the first dummy interconnect.
3[a]	The method of claim 1, wherein in the step (c) the interconnect trench is comprised of a first interconnect trench portion and a second interconnect trench portion whose width is smaller than that of the first interconnect trench portion and which branches from the first interconnect trench portion, and
3[b]	the via hole and the dummy hole are connected to the interconnect trench.

4	The method of claim 3, wherein in the step (c) the dummy hole is connected to the branch point between the first and second interconnect trench portions or to the interconnect trench near the branch point.
5	The method of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO ₂ film.
6	The method of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode.
7	The method of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect.
8	The method of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect.
9	The method of claim 1, wherein the via and the dummy via are substantially circular in a plan view.
10	The method of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square.
11	The method of claim 1, wherein the first interconnect and the second interconnect extend in a same direction.

12	The method of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends.
13	The method of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less.
14	The method of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via.
15[a]	The method of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and
15[b]	the via is connected to the second interconnect portion.
16	The method of claim 15, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions.
17[a]	The method of claim 15, wherein the dummy via is substantially rectangular in a plan view, and
17[b]	a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction.
18	The method of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film.

19	The method of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.
20	The method of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film.

I. RELIEF REQUESTED

Applying the following grounds, Petitioner petitions for *Inter Partes* Review (“IPR”) of U.S. Patent No. 7,632,751 (“the ’751 patent”) and cancellation of claims 1-20:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A/1B	1-2, 5-8, 10-13, 18, 20	102/103	Watanabe
2	3-4, 15-16	103	Watanabe, Kamoshima
3	17	103	Watanabe, Kamoshima, Fukazawa
4	9	103	Watanabe, Iizuka
5	1, 5-6, 9, 11-14, 18-19	102	Hasunuma
6	2, 20	103	Hasunuma, Kurashima
7	2, 8, 10	103	Hasunuma, Watanabe
8	1, 3-4, 7, 14-16, 19	103	Aoyagi
9	17	103	Aoyagi, Fukazawa

This petition is supported by the declaration of Dr. Reinhold Dauskardt, an expert in the field of interconnect technology. TSMC-1003, ¶¶1-39.

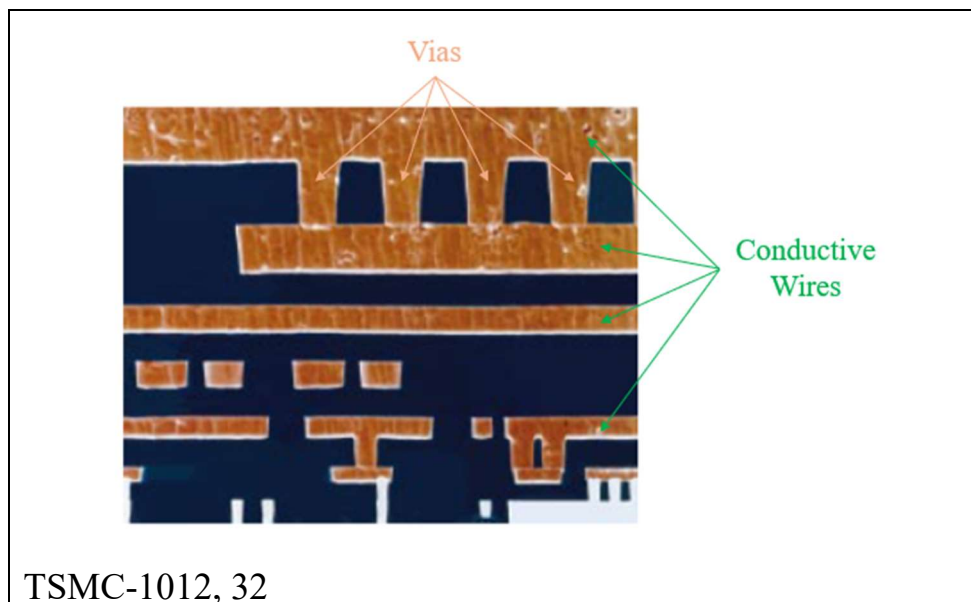
II. STATE OF THE ART

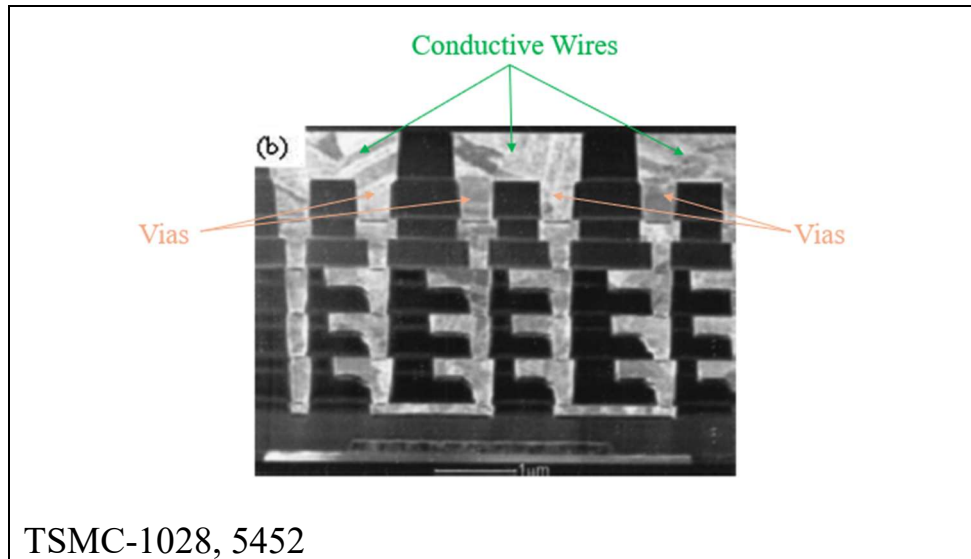
The ’751 patent describes the use of dummy structures to reduce stress migration and void formation in interconnect structures. Such dummy structures,

for the same purposes, and associated methods of manufacturing interconnect structures were already known. *Id.*, ¶¶40-46.

A. Interconnects and Dual Damascene

Semiconductor chips have multiple levels of conductive wires (“interconnects”) for controlling chip operation, with vias connecting wires between different levels when needed; such interconnect structures are commonly made of aluminum or copper. TSMC-1015, 1:13-24; *see also* TSMC-1012, 32; TSMC-1017, 2:53-58. Exemplary interconnect structures are shown below:





Dual damascene is a manufacturing process where patterns of trenches and underlying via holes are filled with conductive metal(s) to simultaneously form the interconnects on a given level and the vias below that level. TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract; TSMC-1034, 671-76. This process is illustrated below:

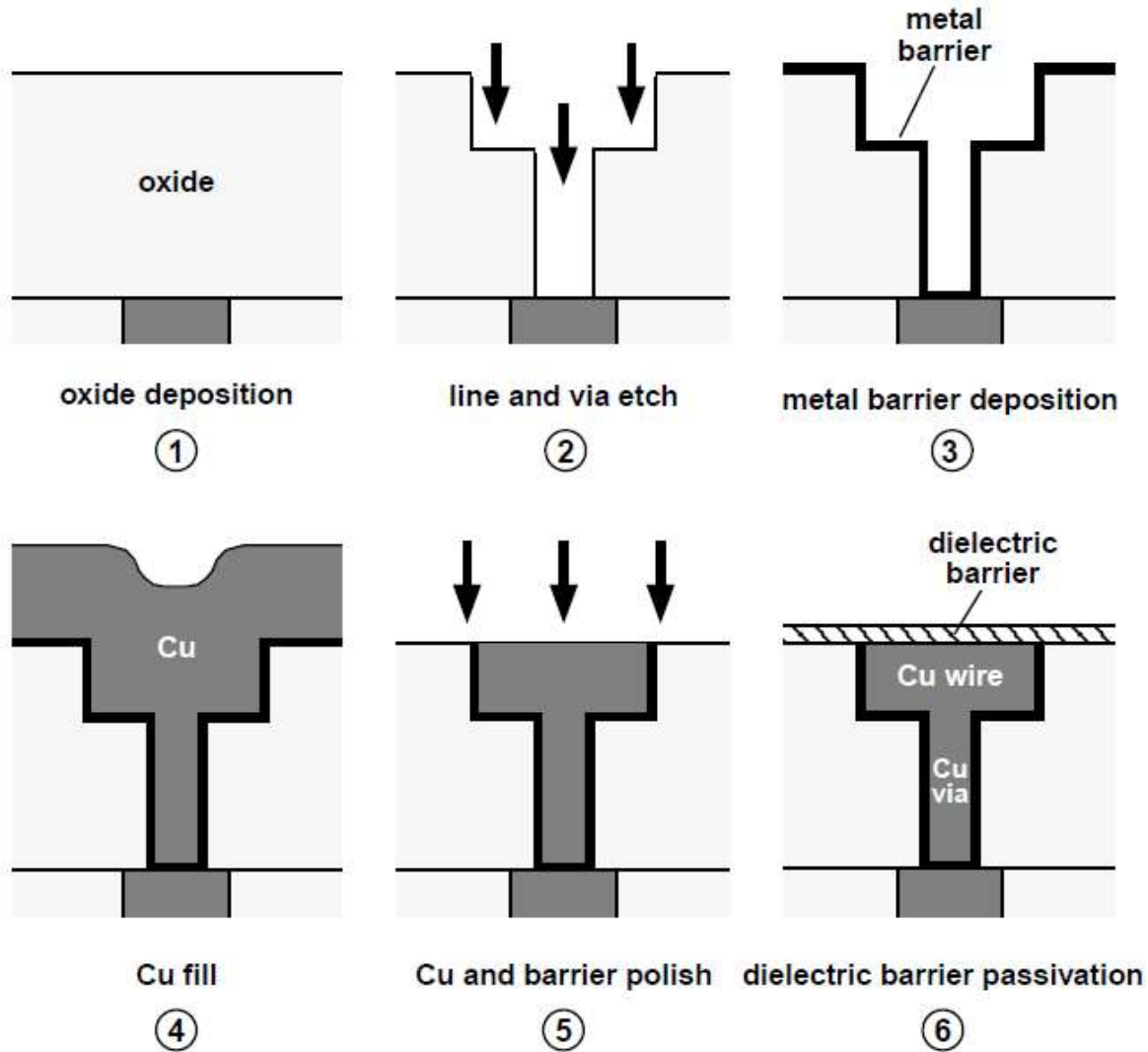


Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects.

TSMC-1027, 25. Steps ④→⑤ are typically performed using chemical mechanical polishing (“CMP”). TSMC-1034, 322-24, 675.

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength

Stress migration and electromigration involve the movement of metal atoms and vacancies within the interconnect structure; because vacancies tend to

aggregate in/under vias, voids can form and cause electrical disconnects. TSMC-1029, 207; TSMC-1028, 5455-56, 5458-59; TSMC-1015, 1:32-37, 2:61-63. In addition, insulating films, especially low k materials, can have lower mechanical strength and poorer adhesion that make them susceptible to damage, for example during CMP. TSMC-1016, 1:53-2:7; TSMC-1026, 583.

As replete in the art, dummy structures have been used well before the '751 patent for addressing these problems. For example, dummy vias have been added near active vias to arrest stress-induced vacancy migration and void formation. TSMC-1029, Abstract, 208; TSMC-1015, 2:64-3:14. Dummy structures have been known to address electromigration reliability concerns, including dummy plugs that act as reservoirs for metallic ions and reduce mechanical stress caused by electromigration. *See* TSMC-1015, 1:66-2:11; TSMC-1032, ¶¶[0012]-[0016]. Migrating vacancies/microvoids get distributed between vias and dummy vias, reducing their concentration in/under the vias. TSMC-1029, 208; TSMC-1009, ¶[0088]. Dummy vias were also well-known to improve mechanical strength, such as to prevent damage during CMP. TSMC-1016, 4:42-47; TSMC-1026, 584-85.

Similar to dummy vias, dummy wirings also improve mechanical properties, helping adhesion across multiple insulating layers and leading to improved planarization after CMP by reducing dishing. TSMC-1020, Abstract; TSMC-1024, 2:55-58; TSMC-1025, Abstract; TSMC-1026, 584-85. Connecting dummy wirings

to dummy vias was well-known to increase the mechanical strength of the combined insulating layer and upper-level wiring, as well as enhance the durability of multi-layered insulating films during CMP and other manufacturing steps.

TSMC-1011, 8:35-54.

III. THE '751 PATENT

A. Overview

As Dr. Dauskardt explains (TSMC-1003, ¶¶47-51), the '751 patent relates to a method of fabricating a semiconductor device having multilevel interconnection structures. TSMC-1001, 6:22-7:43. A first interconnect 102A (and optionally a dummy interconnect 102B) is formed in insulating film 101. *Id.*, 11:21-26, Figs. 1A, 2B. After forming intermediate insulating layers 103-105, interconnect trench 107, via hole 106A and dummy via hole 110B are formed therein, followed by deposition of barrier film 108/copper film 109 in holes 106A, 106B and trench 107 to form via 110A, dummy via 110B, and second interconnect 111 in a dual damascene process. *Id.*, 11:1-11:37, Figs. 1B-1C, 2A-2B.

FIG. 1B

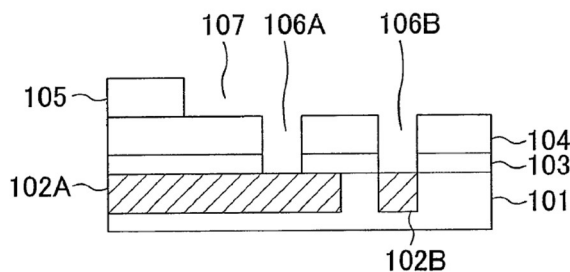
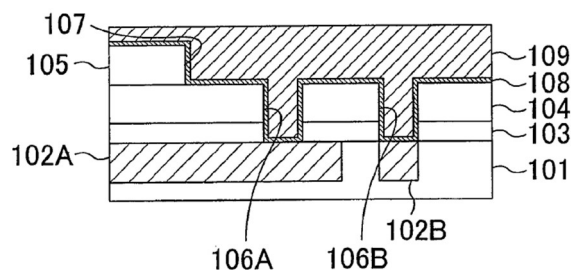


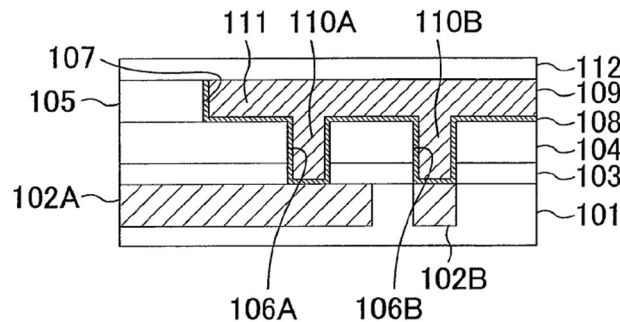
FIG. 1C



Via 110A connects first interconnect 102A and second interconnect 111.

Id., 11:31-37. Dummy via 110B connects dummy interconnect 102B and second interconnect 111, but is not connected to first interconnect 102A. *Id.*, 11:31-37; Figs. 2A-2B.

FIG. 2B



First interconnect 102A, via 110A and second interconnect 111 constitute part of a closed circuit during device operation, while neither dummy interconnect 102B nor dummy via 110B does. *Id.*, 10:40-44. That is, the device remains operable even if dummy interconnect 102B and dummy via 110B are omitted. *Id.*, 10:44-48.

According to the '751 patent, vacancies in copper film 109 of second interconnect 111 are divided and flow into via 110A and dummy via 110B, reducing the total vacancies flowing into via 110A and thereby reducing the associated stress gradient to via 110A. *Id.*, 11:47-54. The '751 patent says this suppresses occurrences of voids in via hole 106A. *Id.*, 11:57-62.

B. Prosecution History

The '751 application claims priority to a U.S. application filed December 2, 2004, and a Japanese application filed December 3, 2003.

During prosecution, a first action Notice of Allowance issued, with the following reasons for allowance:

Claim 27 [issued claim 1] recites...forming a dummy hole which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench connected to the via hole and the dummy hole. These limitations...are neither taught nor suggested in the prior art.

TSMC-1002, 166.

C. Claim Construction

The Board construes claims under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For purposes of this proceeding, Petitioner does not believe that any claim terms need construction to resolve the unpatentability issues presented in this Petition. TSMC-1003, ¶52.

IV. ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing.

TSMC-1003, ¶37. Additional graduate education could substitute for work

experience, and additional work experience/training could substitute for formal education. *Id.*

V. PRIOR ART¹

Reference	Filed	Published	Pre-AIA Prior Art Qualification
Watanabe	12/4/2002 (USPTO)	6/26/2003	§§102(a),(b),(e)
Hasunuma	9/3/2003 (USPTO)	6/17/2004	§102(e)
Aoyagi	3/20/2001 (USPTO)	9/6/2001	§§102(a),(b),(e)
Kurashima	8/14/2003 (USPTO)	5/9/2006	§102(e)
Iizuka	1/24/1992 (USPTO)	10/5/1993	§§102(a),(b),(e)
Kamoshima	9/9/2003 (USPTO)	9/9/2004	§102(e)
Fukazawa	3/29/2001 (JPO)	10/11/2002	§§102(a),(b)

VI. DETAILED EXPLANATION OF GROUNDS

A. GROUNDS 1A/1B: Watanabe anticipates (Ground 1A) and renders obvious (Ground 1B) Claims 1-2, 5-8, 10-13, 18, and 20

Watanabe anticipates and renders obvious claims 1-2, 5-8, 10-13, 18, and 20.

TSMC-1003, ¶¶94-187.

¹ All references are prior art regardless of any priority claim to the Japanese application filed December 3, 2003. Petitioner does not acquiesce that any claims are so entitled.

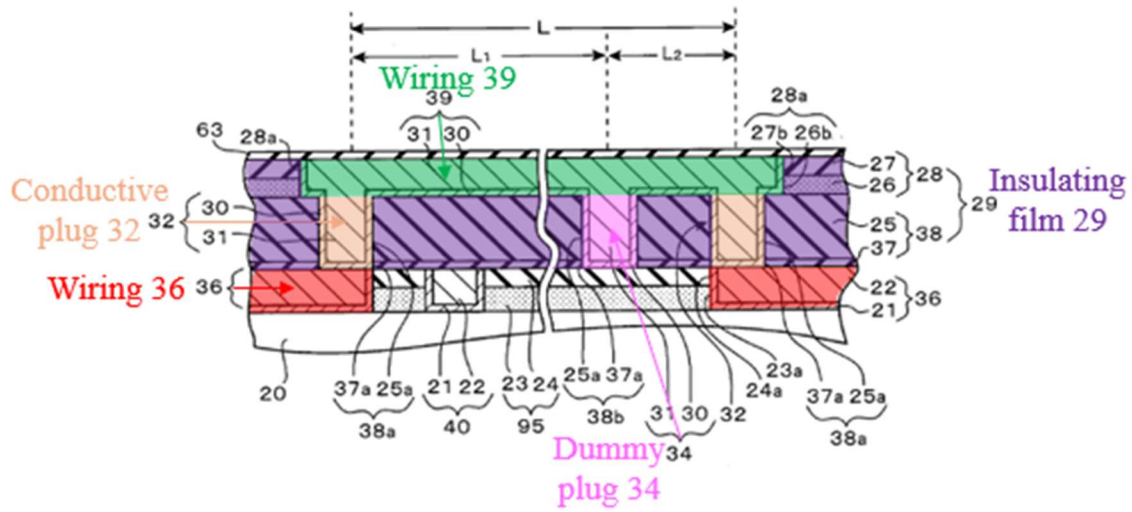
1. Watanabe

Because Watanabe is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 patent purports to address (e.g., interconnect reliability), Watanabe is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1004, ¶¶[0005], [0016]-[0018]; TSMC-1003, ¶¶54-70.

Watanabe discloses semiconductor devices having multilevel dual-damascene interconnection structures that address via reliability problems caused by stress-induced void migration and electromigration. TSMC-1004, ¶¶[0012]-[0019], [0022]-[0024], [0077]. Watanabe incorporates non-functional dummy vias and dummy interconnects formed concurrently with the functional structures. *Id.*, Abstract, ¶¶[0026]-[0028].

Watanabe's first embodiment (Figs. 1-2) discloses wiring 36, overlying insulating film 29, and wiring 39 formed along with conductive plug 32 and dummy plug 34 using a dual damascene process. *Id.*, Fig. 1, ¶¶[0065]-[0074].

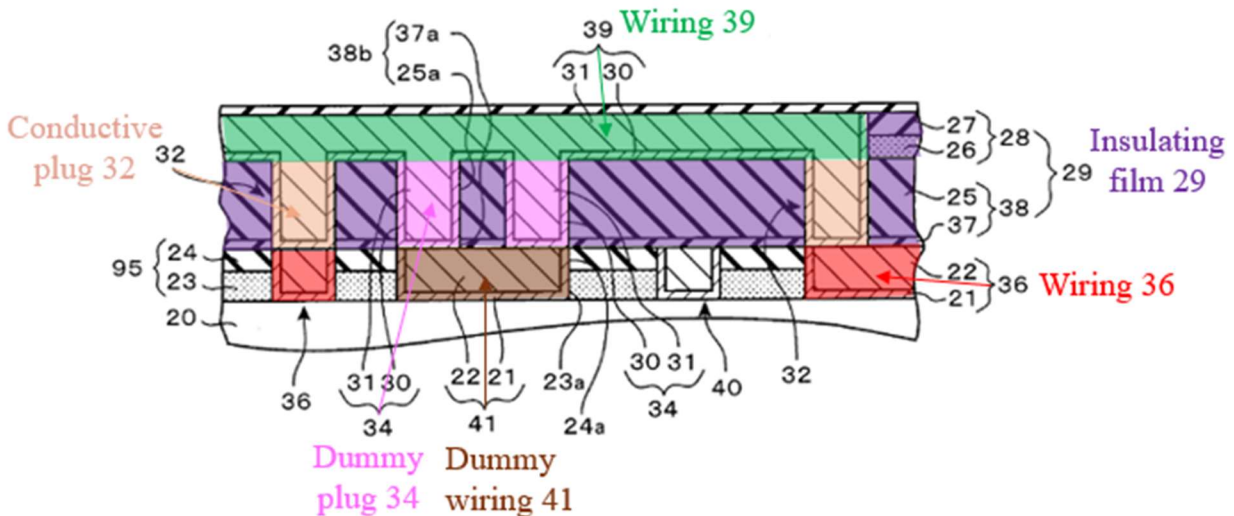
FIG. 1



Conductive plug 32 connects wiring 36 and wiring 39. Dummy plug 34 connects to wiring 39, but its other end extends to insulating film 95 in a “non-forming region.” *Id.*, Fig. 1, ¶¶[0067], [0079]. This dummy plug 34 reduces stress migration problems, provides a source of copper atoms to mitigate electromigration, and enhances support for insulating film 29/wiring 39. *Id.*, ¶¶[0026], [0070]-[0079].

Watanabe's second embodiment (Figures 3-4) adds, among other structures, a dedicated, isolated dummy wiring 41. *Id.*, Fig. 3, ¶¶[0028], [0090].

FIG. 3



Dummy wiring 41 resides in the same insulating film 95 as wiring 36. *Id.*, Fig. 3.

Watanabe asserts that this structure adds mechanical strength and uniformity during CMP. *Id.*, ¶¶[0028]-[0029], [0091].

Overall, Watanabe discloses multiple embodiments, including:

- a “first embodiment” in Figures 1-2 (*see* ¶¶[0059]-[0087]);
- a “second embodiment” in Figures 3-4 (*see* ¶¶[0088]-[0092]);
- a “third embodiment” in Figures 5A-5C (*see* ¶¶[0093]-[0108]);
- a “fourth embodiment” in Figures 6-7 (*see* ¶¶[0109]-[0114]);

- a “fifth embodiment”² in Figures 8-11 (*see* ¶¶[0115]-[0133]); and
- a more generic embodiment in Figure 14 (*see* ¶¶[0172]-[0181]).

See, e.g., id., ¶¶[0038]-[0049], [0051].

Watanabe discloses a method of manufacturing in Figures 12A-12N for the foregoing embodiments. *Id.*, ¶[0049] (“method of manufacturing the semiconductor device **according to the embodiments of the present invention.**”)³; *see also id.*, ¶¶[0072], [0134]-[0170]; TSMC-1003, ¶¶57-70, 97.

The first through fifth embodiments (Figures 1-9) use common reference numerals as Figures 12A-12N. *See* TSMC-1004, ¶¶[0089], [0116], [0135]. Moreover, Watanabe discloses in introducing Figure 14 that the method can be repeated to obtain any number of wirings. *Id.*, ¶¶[0171]-[0173].

² Watanabe’s fifth embodiment includes a three-level interconnect structure that satisfies claim 1 in multiple ways. TSMC-1004, ¶¶[0115]-[0133]; TSMC-1003, ¶96, n.2. Watanabe’s fifth embodiment (Figures 8-9) includes a similar structure and satisfies claim 1 in the same way as its first embodiment (Figures 1-2), which is a first mapping of Watanabe’s fifth embodiment. Because the following discussions of Watanabe’s first embodiment apply equally to this first mapping of the fifth embodiment, the first mapping is not discussed separately. Under a second mapping, Watanabe’s fifth embodiment meets claim 1 based on its second and third level interconnects. All discussions of Watanabe’s fifth embodiment below apply this second mapping.

³ All emphases throughout Petition are added.

Additionally, it was obvious to use the dual damascene method of manufacturing of Figures 12A-12N to create respective wiring layers for any of Watanabe's embodiments. TSMC-1003, ¶¶98-100. A POSITA was motivated to do so by the increased efficiency, simplified processing, reduced cost, and increased reliability benefits of the dual damascene process, and could have easily implemented such a process given its already disclosed use in Watanabe and widespread general use at the time. *Id.*; *see also* TSMC-1034, 583-84, 671-76, 718, 723-26; TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-151; TSMC-1027, 25; TSMC-1028, 5458-59.

2. Claim 1⁴

a) 1[pre]

Watanabe discloses “a semiconductor device manufactured by the damascene process.” TSMC-1004, ¶¶[0003], [0038], [0051], [0135]-[0136], [0170]-[0173]; Title; Abstract; Figs. 1-9, 12A-12N, 14; TSMC-1003, ¶¶95-97.

b) 1[a]

Embodiments 1-3

Watanabe's Figs. 12C-12D teach depositing “barrier metal layer 21” and “copper film 22” on underlying layer 20, followed by chemical mechanical polishing (“CMP”) to form “wiring 36” (i.e., “a first interconnect”) on a

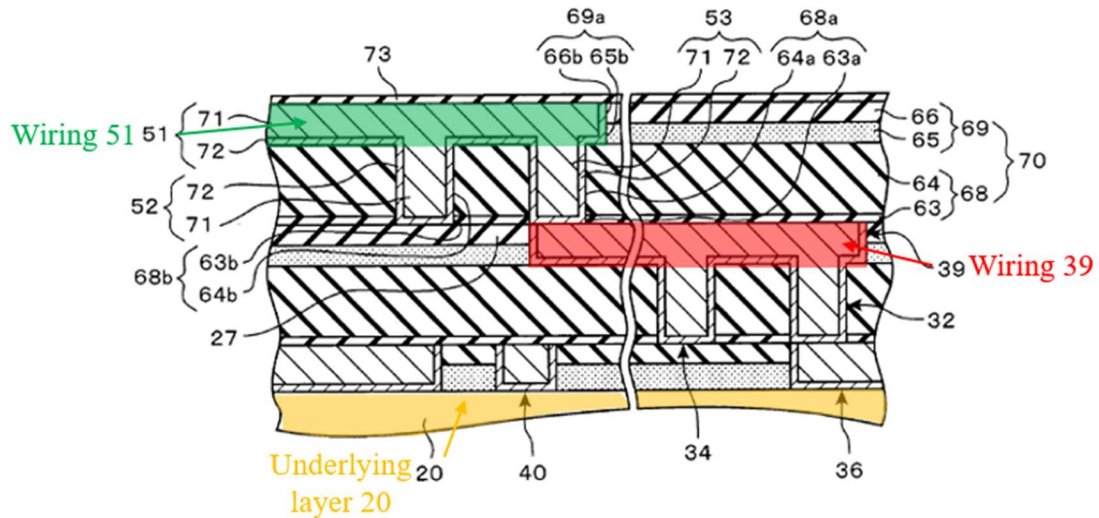
⁴ See List of Challenged Claims for all claim language.

A cross-sectional view of a semiconductor device 100. The device features a wiring layer 36 (red) and an underlying layer 20 (yellow). The wiring layer 36 contains wiring 36 and is positioned above the underlying layer 20. The underlying layer 20 is positioned below the wiring layer 36. The device includes various layers and structures, including a top layer 27, a middle layer 26, a bottom layer 25, and a base layer 21. The device also includes a wiring layer 36 and an underlying layer 20. The device is shown in a cross-sectional view, with various layers and structures labeled with reference numerals.

Embodiment 5

-16-

FIG. 8



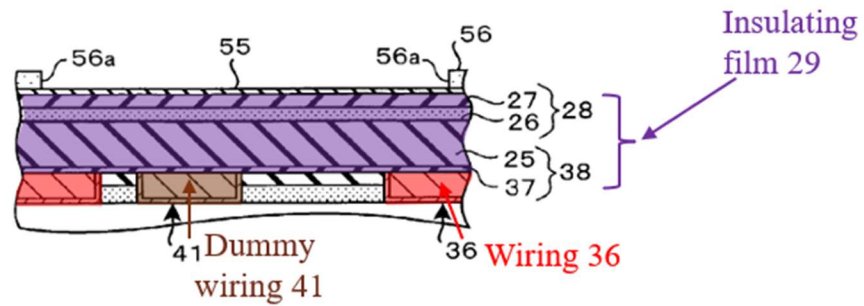
TSMC-1003, ¶104.

c) 1[b]

Embodiments 1-3

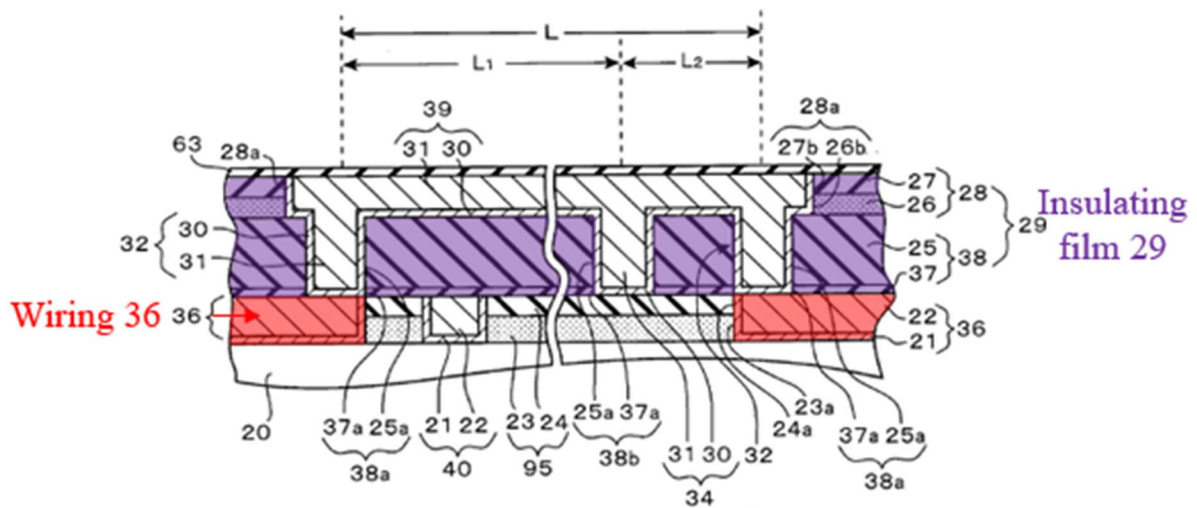
Watanabe discloses forming a first insulating film (e.g., “insulating film 29”) on the first interconnect (e.g., “wiring 36”). TSMC-1004, ¶¶[0066], [0149]-[0152], Figs. 12E, 1, 3; TSMC-1003, ¶¶105-08. More particularly, with reference to Figure 12E, silicon nitride film 37 is formed to cover wiring 36 and dummy wiring 41, then silicon oxide film 25, low-dielectric insulating film 26, and silicon oxide film 27 are deposited on silicon nitride film 37. TSMC-1004, ¶¶[0149]-[0151].

FIG. 12E



Figures 1 (first embodiment) and 3 (second embodiment) disclose insulating film 29 (which include lower insulating film 38 and upper insulating film 28) formed on wiring 36:

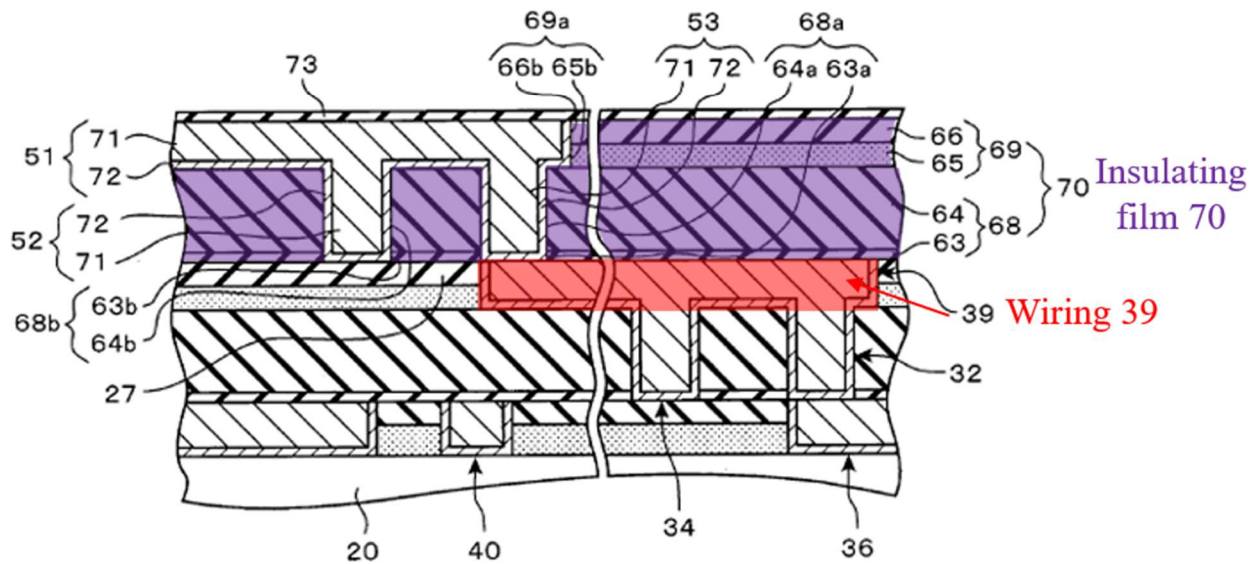
FIG. 1



Embodiment 5

-19-

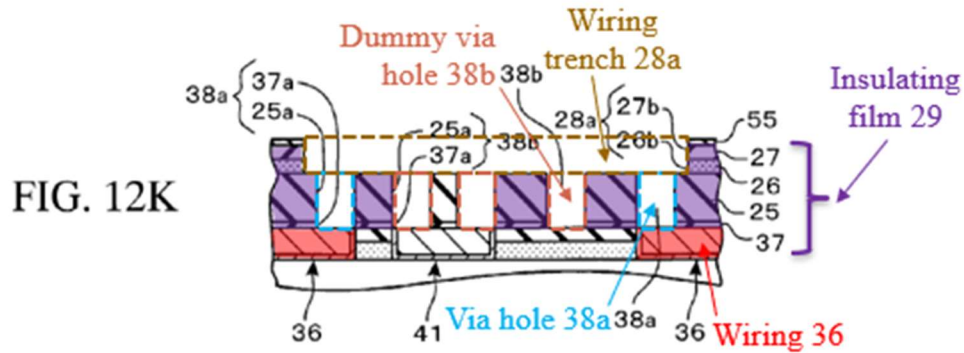
FIG. 8



d) 1[c]

Embodiments 1-3

Watanabe discloses forming in the first insulating film (e.g., “insulating film 29”), a via hole (e.g., “via hole 38a”) connected to the first interconnect (e.g., “wiring 36”), a dummy hole (e.g., “dummy via hole 38b”) which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench (e.g., “wiring trench 28a”) connected to the via hole and the dummy hole. TSMC-1004, ¶¶[0067], [0159]-[0165], Figs. 12J-12K; TSMC-1003, ¶¶110-18. Figure 12K discloses these components:



Watanabe discloses etching silicon nitride film 37 to form “openings 37a...in the silicon nitride film 37.” TSMC-1004, ¶[0162]. Watanabe forms “via holes 38a,” “dummy via holes 38b,” and “wiring trench 28a,” where “via holes 38a are formed to extend from the wiring trench 28a to the first wiring 36,” “dummy via holes 38b may be formed to reach the non-forming region of the first wiring 36 or reach the dummy wiring 41,” and “wiring trench 28a is constructed by the openings 27b and 26b.” *Id.*, ¶¶[0067], [0164]-[0165]; *see id.*, ¶[0079].

Figures 1 (first embodiment) and 3 (second embodiment) disclose these features:

FIG. 1

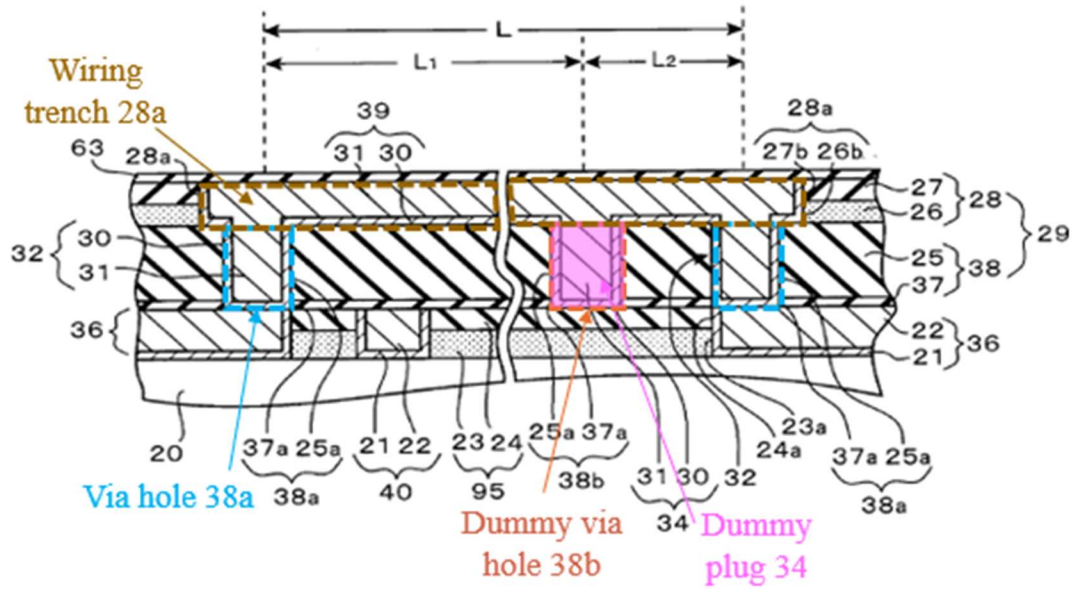
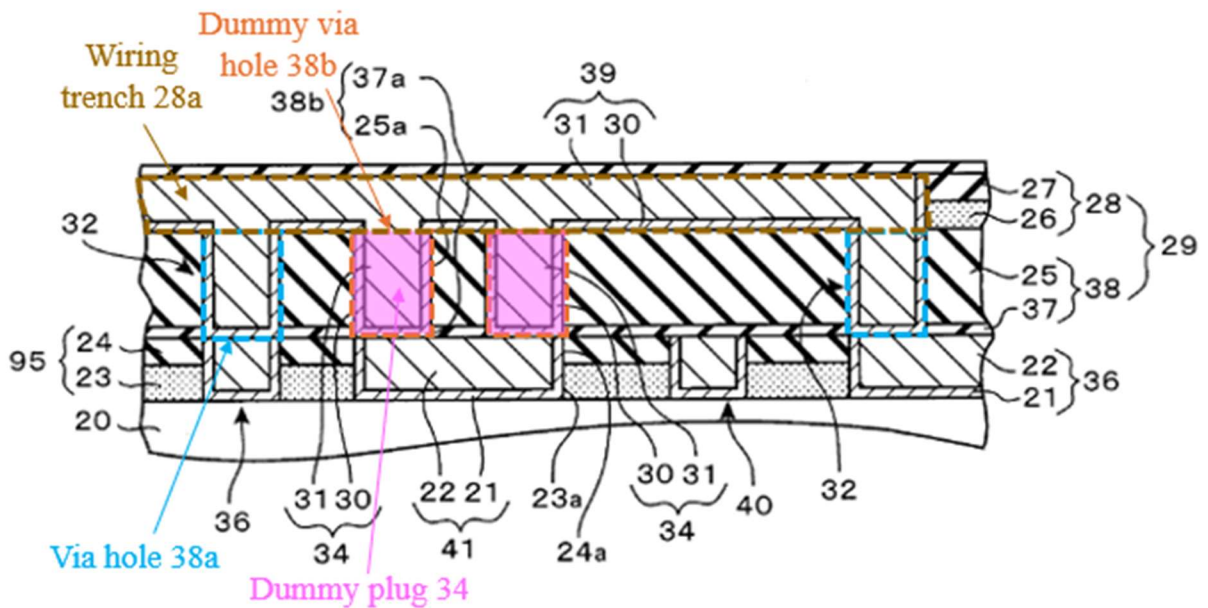


FIG. 3



As outlined for limitation 1[d], wiring 39 is formed in via hole 38a, dummy via hole 38b, and wiring trench 28a. *Infra*, §VI(A)(2)(e). The portion of wiring 39 in dummy via hole 38b serves as a dummy plug 34. TSMC-1004, ¶[0168].

“Dummy via holes 38b” and “dummy plugs 34” are “arranged so as to be incapable of having current flow therethrough.” TSMC-1003, ¶¶115-18. The ’751 specification states that dummy vias and dummy interconnects “do not constitute a closed circuit in actual use of a device with an interconnection structure including these via and interconnect (i.e., no current flows therein during actual use of the device.)” and the circuit is operable even if dummy via and dummy interconnect are omitted in the interconnection structure. TSMC-1001, 3:17-21; 10:42-48.

Dummy plugs 34 in dummy holes 38b are only connected on one end to an active circuit element (i.e., “wiring 39”), and not the other end which instead ends at insulating film 95. TSMC-1004, Figs. 1, 3, 5, 8-9; TSMC-1003, ¶116.

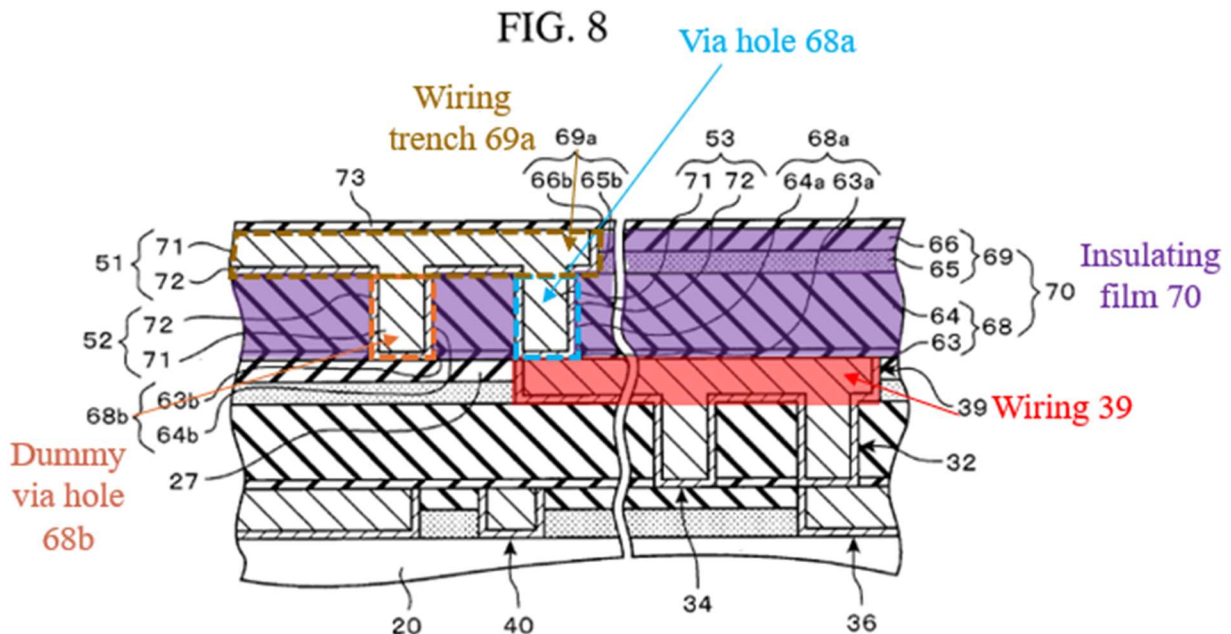
“Dummy” via holes 38b and “dummy” plugs 34 do not constitute part of a closed circuit in actual use of the device; that is no current flows therein during actual device use. TSMC-1003, ¶116. In the second embodiment shown in Figure 3, dummy interconnect 41 (relevant for claim 2) does not have current flow therethrough. No current flows through dummy plugs 34 (or 52) due to this lack of connection to a second active circuit element. *Id.*

Instead, current flows between Watanabe’s wiring 36 and wiring 39 through conductive plugs 32, which constitute parts of a closed circuit during device operation. *See* TSMC-1004, ¶[0073]. And Watanabe’s device would still be operable without dummy via holes 38b and dummy plugs 34, because current

would still flow through wirings 36 and 39 through plugs 32 during actual device use. TSMC-1003, ¶117.

Embodiment 5

Applying the same Figures 12A-12N process for wiring 51 in the fifth embodiment device, Watanabe forms in the first insulating film (e.g., “insulating film 70”), a via hole (e.g., “via hole 68a”) connected to the first interconnect (e.g., “wiring 39”), a dummy hole (e.g., “dummy via hole 68b”) which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench (e.g., “wiring trench 69a”) connected to the via hole and the dummy hole. TSMC-1004, ¶¶[0118]-[0121], [0159]-[0165], Fig. 8; TSMC-1003, ¶¶119-20.



Just like dummy via holes 38b, dummy via holes 68b are likewise incapable of current flow. TSMC-1003, ¶120. Figure 14 shows the same, plus additional dummy plug 52 similarly connected to wiring 51 immediately above.

e) 1[d]

Embodiments 1-3

Watanabe discloses depositing a conductive material (e.g., “copper film 31,” “barrier metal layer 30”) in the via hole (e.g., “via hole 38a”), the dummy hole (e.g., “dummy via hole 38b”) and the interconnect trench (e.g., “wiring trench 28a”), thereby forming a via (e.g., “conductive plug 32”), a dummy via (e.g., “dummy plug 34”) and a second interconnect (e.g., “wiring 39”). TSMC-1004, ¶¶[0166]-[0169], [0068]-[0072], Figs. 12L-12N, Figs. 1, 3; TSMC-1003, ¶¶121-24.

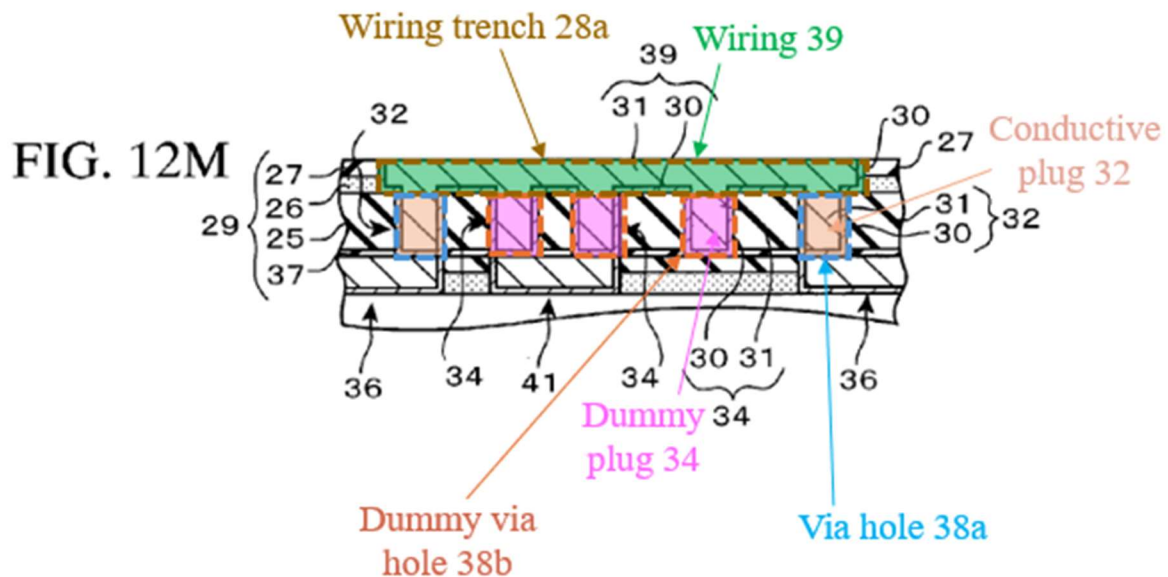
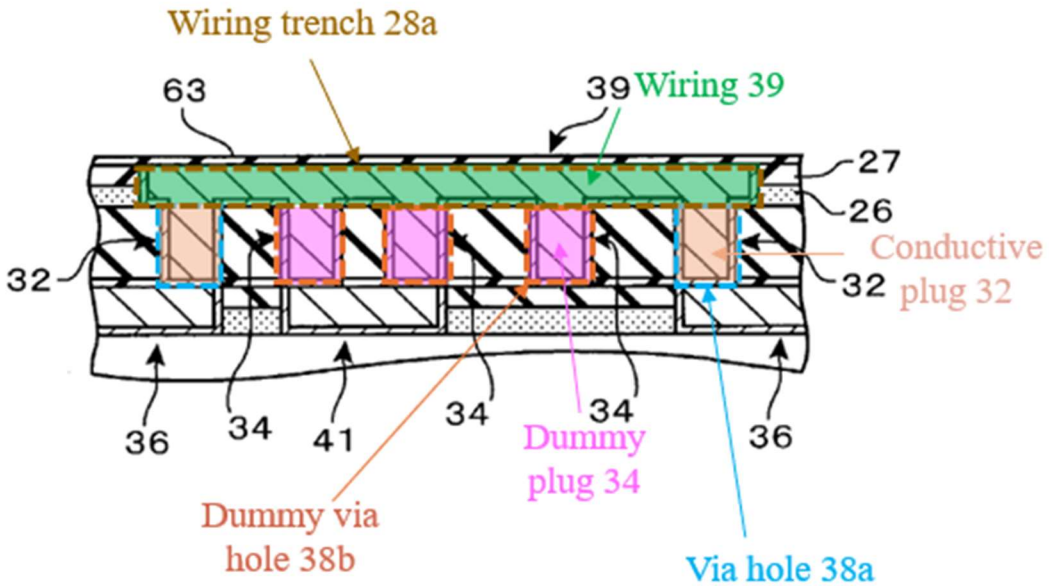


FIG. 12N

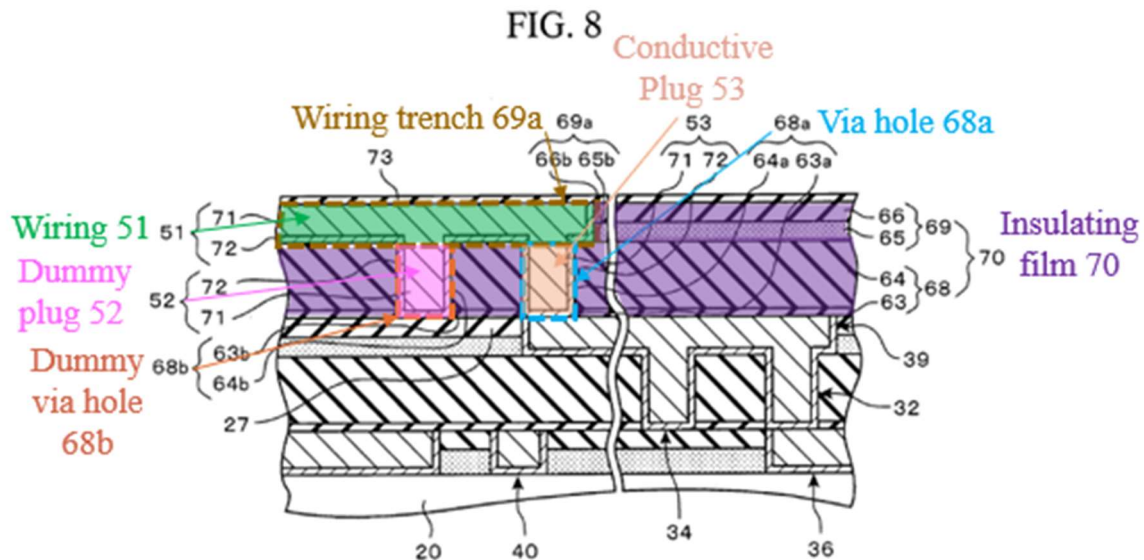


Watanabe explains that “barrier metal layer 30 is formed” and then “copper film 31 is formed” on “barrier metal layer 30.” *Id.*, ¶¶ [0166]-[0167]. “[B]arrier metal layer 30 and the copper film 31...constitute the second wiring 39” and “the portion of the second wiring 39, which is buried in the via hole 38*a*, is served as the plug, and the portion of the second wiring 39, which is buried in the dummy via hole 38*b*, is served as the dummy plug.” *Id.*, ¶[0168]. Wiring 39, conductive plug 32, and dummy plug 34 are formed with a “dual damascene process.” *Id.*, ¶¶[0072], [0135].

Figures 1, 3, and 5 each disclose the via (e.g., “conductive plug 32”), dummy via (e.g., “dummy plug 34”), and second interconnect (e.g., “wiring 39”). TSMC-1003, ¶124; *see* TSMC-1004, ¶¶0135].

Embodiment 5

Applying the same Figures 12A-12N process for wiring 51 in the fifth embodiment device, Watanabe discloses depositing a conductive material (e.g., “copper film 71,” “barrier metal layer 72”) in the via hole (e.g., “via hole 68a”), the dummy hole (e.g., “dummy via hole 68b”) and the interconnect trench (e.g., “wiring trench 69a”), thereby forming a via (e.g., “conductive plug 53”), a dummy via (e.g., “dummy plug 52”) and a second interconnect (e.g., “wiring 51”) as shown below. TSMC-1004, ¶¶[0117]-[0122], [0166]-[0170], Figs. 8-9; TSMC-1003, ¶125.



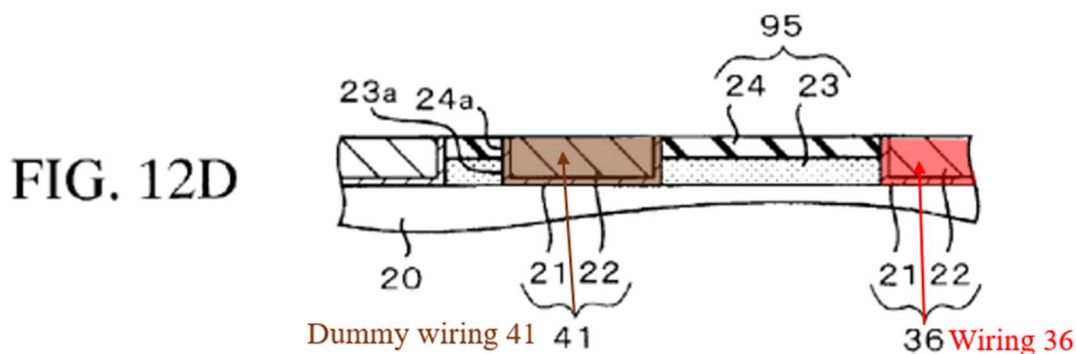
At least Watanabe's second and fifth embodiments satisfy claim 2.

Embodiment 2

-28-

device, i.e., no current flows therein during use, and Watanabe's device would still be operable if dummy wiring 41 was omitted. *Id.* Indeed, Watanabe states that “as shown in FIG. 3, a dummy wiring 41 is provided *in the non-forming region* of the first wiring 36.” TSMC-1004, ¶[0090].

As part of depositing barrier metal layer 21/copper film 22 and planarizing copper film 22, the “residual copper film 22 and the barrier metal layer 21 constitute the first wiring 36 and the dummy wiring 41,” i.e., wiring 36 and dummy wiring 41 are simultaneously formed. TSMC-1004, ¶[0144], Figs. 12A-12D; TSMC-1003, ¶130.

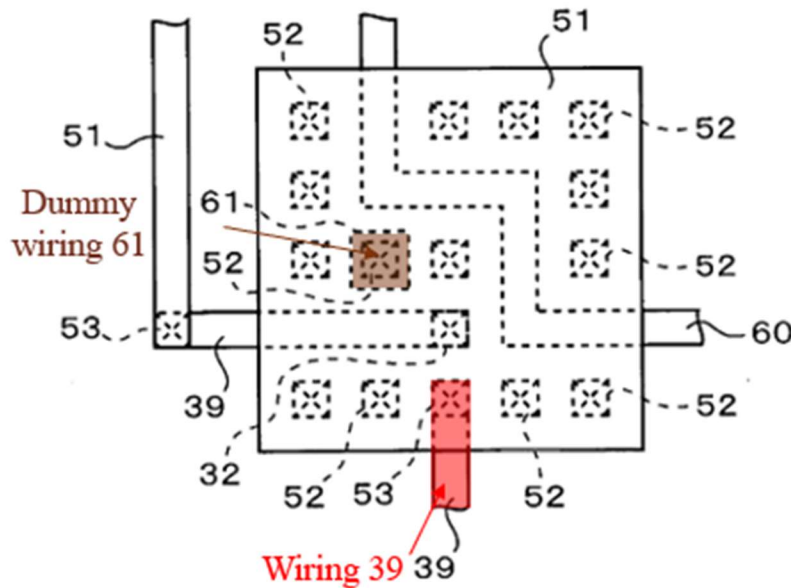


Embodiment 5

For the fifth embodiment, Watanabe discloses simultaneously forming a first dummy interconnect (e.g., “dummy wiring 61”) with wiring 39 on the semiconductor substrate (“underlying layer 20”), stating that “dummy wiring 61” is “formed in the same layer as the second wiring 39.” TSMC-1004, ¶[0127], Fig. 9; *see also id.*, ¶[0171] (“Although the structure of two wiring layers (the first

wiring 36 and the second wiring 39) is obtained in the above, any number of wirings can be laminated by repeating the method”); TSMC-1003, ¶¶132-33. Thus, following Figures 12A-12N, dummy wiring 61 and wiring 39 are formed simultaneously. Figure 9 discloses these features:⁵

FIG. 9



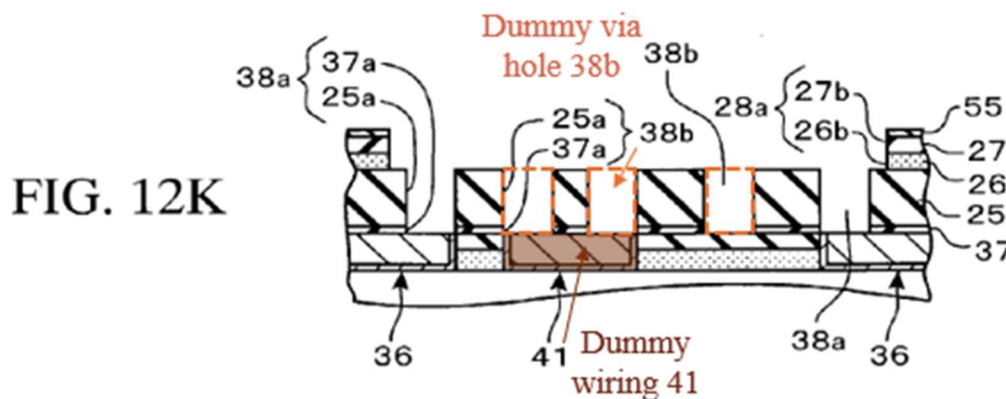
For the same reasons discussed for “dummy wiring 41,” a POSITA would understand “dummy wiring 61” is a “dummy interconnect.” TSMC-1003, ¶133.

b) [2b]

⁵ Figure 8 omits “dummy wiring 61,” apparently because of its optional nature or because it shows a different cross-section that does not include dummy wiring 61. TSMC-1003, ¶132, n.4.

Embodiment 2

Regarding its second embodiment, Watanabe discloses that, in step (c), the dummy hole (e.g., “dummy via hole 38b”) is connected to the first dummy interconnect (e.g., “dummy wiring 41”). Watanabe explains that “dummy via holes 38b may be formed to reach...dummy wiring 41.” TSMC-1004, ¶[0165]; *see id.*, ¶[0090], Figs. 12J-12N, 3; TSMC-1003, ¶135; *supra*, §VI(A)(2)(d).



Embodiment 5

Watanabe’s fifth embodiment discloses, in step (c), connecting the dummy hole (e.g., “dummy via hole 68b”) to the first dummy interconnect (e.g., “dummy wiring 61”). TSMC-1003, ¶¶136-37; *see* TSMC-1004, ¶¶[0121]-[0122], [0127], Fig. 9. Thus, Watanabe’s “dummy via hole (dummy connection hole) [68b] is formed in the lower insulating film 68 to reach the non-forming region of the second wiring 39.” TSMC-1004, ¶[0121]. The portion of “wiring 51...buried in the dummy via hole 68b...is called a dummy plug 52,” which “may be connected

to...dummy wiring 61.” *Id.*, ¶¶[0122], [0127]. Dummy via hole 68b is connected to the first dummy interconnect (“dummy wiring 61”). TSMC-1003, ¶137.

4. Claim 5

At least Watanabe’s first through third and fifth embodiments satisfy claim 5.

For the first through third embodiments, Watanabe’s first insulating film (e.g., “insulating film 29”) includes a multilayer lower insulating film 38 constituted by a SiN film (e.g., “silicon nitride film 37”) and a SiO₂ film (e.g., “silicon oxide film 25”). TSMC-1004, ¶¶[0066], [0089], [0150], [0184], Figs. 1, 3, 12E, 12M; TSMC-1003, ¶¶139-41.

FIG. 12E

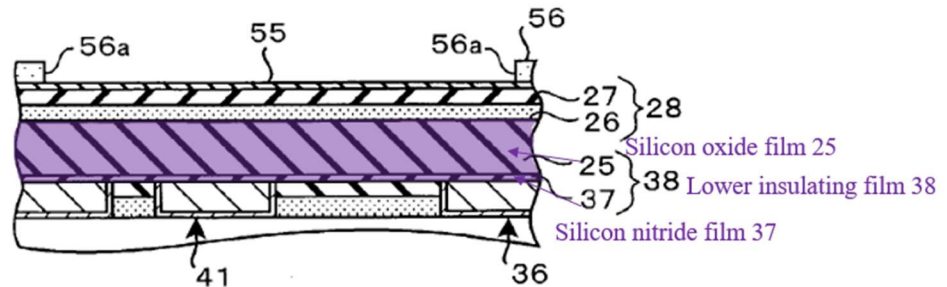
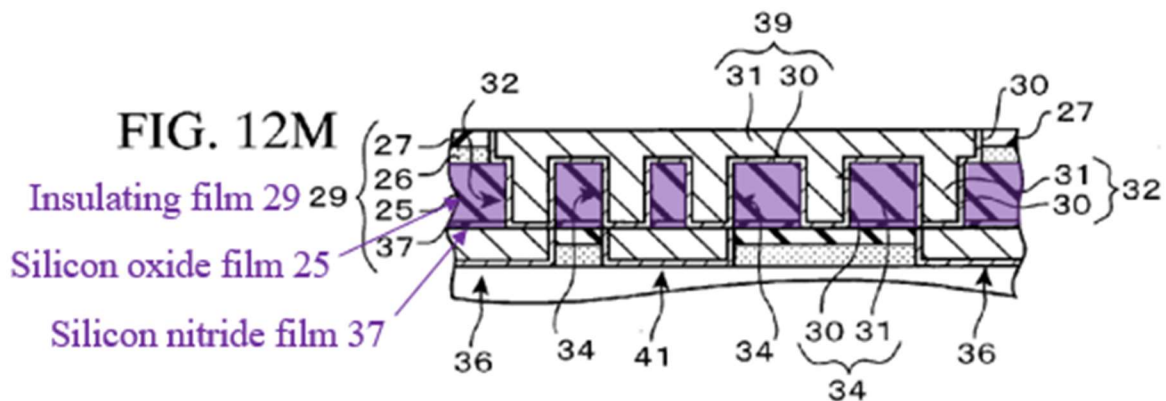
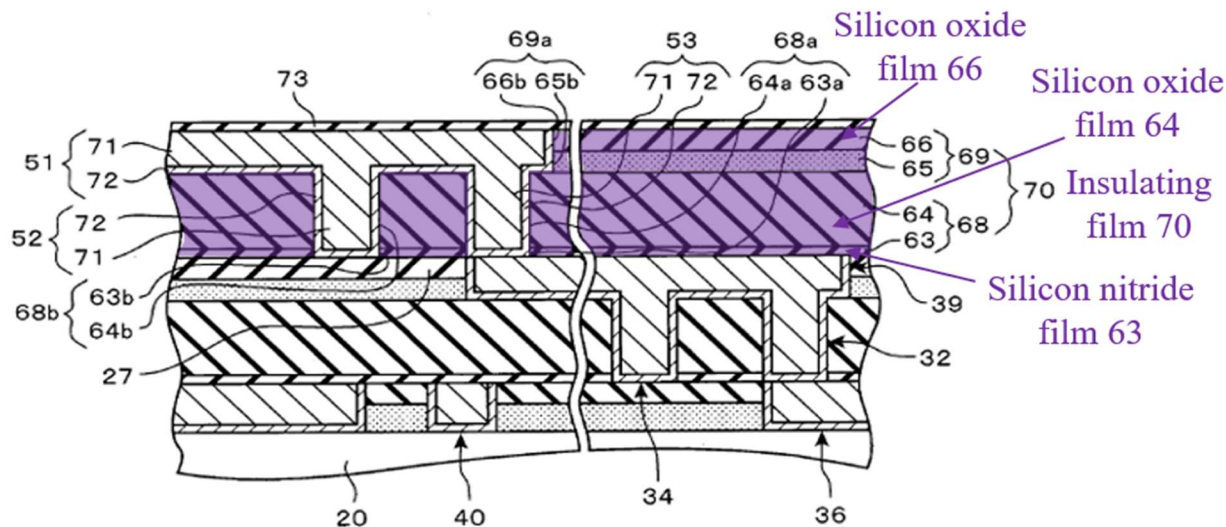


FIG. 12M



In Watanabe's fifth embodiment, the first insulating film (e.g., "insulating film 70") has a multilayer structure including "silicon nitride film 63" and "silicon oxide film 64" (TSMC-1004, ¶[0119], Fig. 8; TSMC-1003, ¶142):

FIG. 8

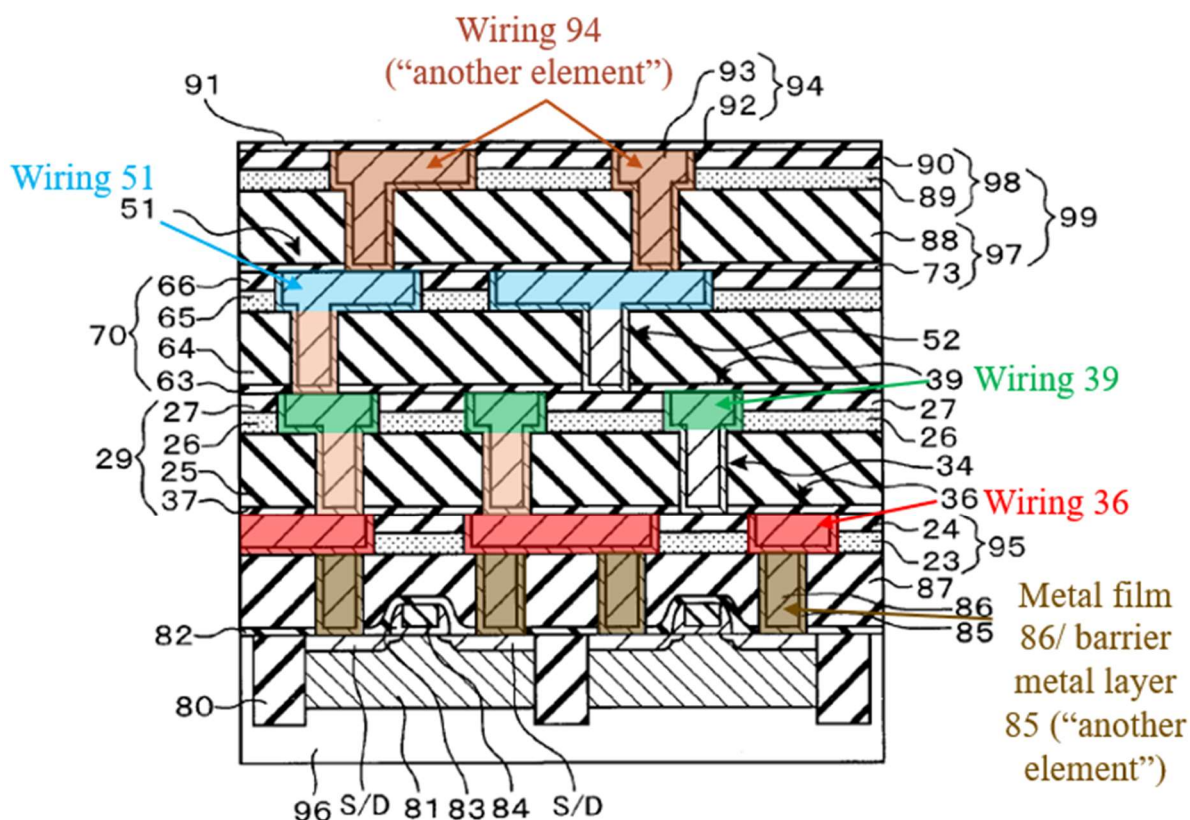


5. Claim 6

In the first to third and fifth embodiments, each of the first and second interconnects (e.g., "wiring 36," "wiring 39," "wiring 51") is connected to another element or an external electrode. TSMC-1003, ¶¶144-52. Watanabe explains that, while a two-wiring structure (wiring 36 and wiring 39) is disclosed, any number of wiring layers can be laminated by repeating the same method (of Figures 12A-12M). TSMC-1004, ¶[0171]; TSMC-1003, ¶146. Watanabe's Figure 14 illustrates a structure having four layers of wirings (including wirings 36, 39, and 51), which are each connected to other elements. *See id.*, ¶¶[0051], [0172]-[0181]. For

example, for the first to third embodiments, wiring 36 is connected to metal film 86 and wiring 39 is connected to wiring 51 by a conductive plug. *Id.* For the fifth embodiment, wiring 39 is connected to wirings 36 and 51 by conductive plugs, and wiring 51 is connected to wiring 94 by another conductive plug, which constitute “other elements”:

FIG. 14



TSMC-1003, ¶146.

Additionally, in each embodiment, underlying layer 20 includes semiconductor transistors as seen in Figure 14, including gate electrodes 84, source/drain regions S/D on silicon substrate 96, and conductive plugs (having

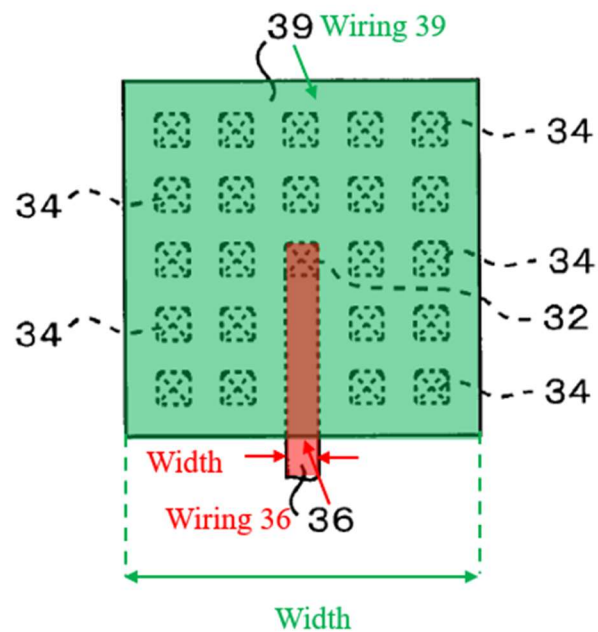
barrier metal layer 85 and metal film 86), which are connected to wirings 36, 39, 51 as shown above. TSMC-1004, ¶¶[0173]-[0178]; *see id.*, ¶¶[0061] (underlying layer 20 has a structure with MOSFETs formed in an active region of the silicon wafer), [0089], [0094], [0116]; TSMC-1003, ¶¶148-49. Accordingly, given that wirings 36, 39 and wirings 39, 51 are first and second interconnects for the first through third and fifth embodiments, respectively (*supra*, §§VI(A)(2)(b), VI(A)(2)(e)), each of these wirings/interconnects is connected to another element or external electrode, satisfying this claim. TSMC-1003, ¶¶147-51.

6. Claim 7

At least Watanabe's third and fifth embodiments meet claim 7.

In the third embodiment, Figure 5A discloses the first interconnect (e.g., “wiring 36”) having a width smaller than that of the second interconnect (e.g., “wiring 39”). TSMC-1004, ¶¶[0094]-[0095], Figs. 5A-5C; TSMC-1003, ¶¶153-55.

FIG. 5A



In the fifth embodiment, the first interconnect (e.g., “wiring 39”) also has a width smaller than that of the second interconnect (e.g., “wiring 51”). TSMC-1004, ¶¶[0125]-[0126], Fig. 9; TSMC-1003, ¶¶156-57.

At least Watanabe's fifth embodiment meets claim 8.

-37-

[illegible]

8. Claim 10

For the first through third and fifth embodiments, Watanabe discloses that plug 32 and dummy plug 34 each have a planar shape that is substantially square, exemplified in Figures 2, 5A, and 9:

FIG. 2

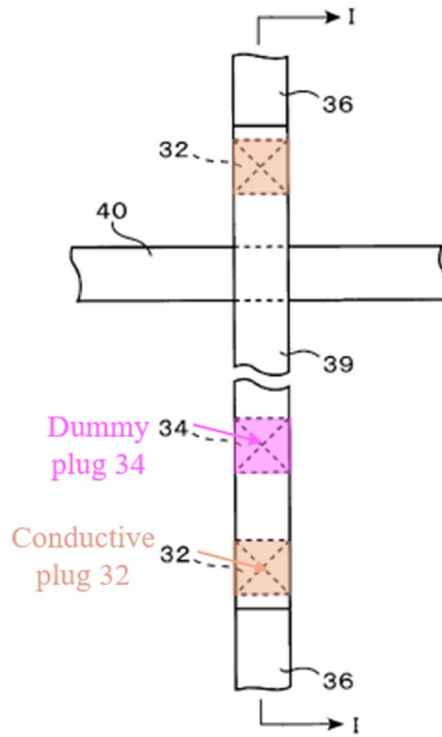


FIG. 5A

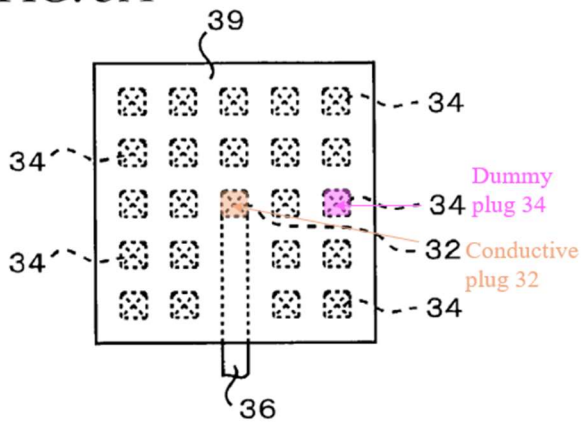
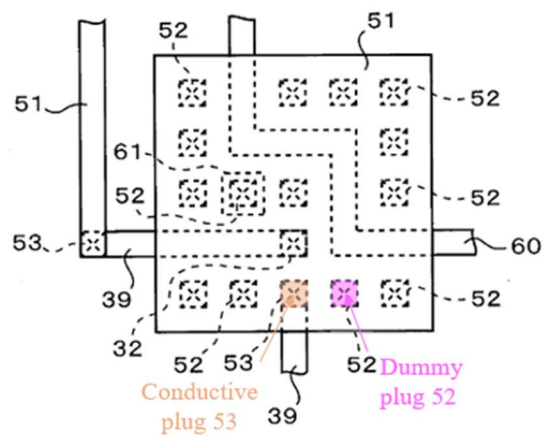


FIG. 9



TSMC-1003, ¶¶161-64; *see also* TSMC-1004, ¶¶[0039], [0041]-[0042], [0046], [0070], [0098], [0124]-[0127], Figs. 2, 4-5C, 9. Indeed, square vias were a well-

known, common option for via shape. TSMC-1003, ¶165; *see also* TSMC-1008, 9:45-47 (“[T]he opening of the via-hole may have any configuration, such as a square....”), 10:8-11; TSMC-1013, 9:45-49; TSMC-1039, 5:27-32.

9. Claim 11

For the first through third and fifth embodiments, Watanabe’s first interconnect (e.g., wiring 36, 39) and second interconnect (e.g., wiring 39, 51) extend in a same direction (e.g., along “L” direction”). TSMC-1004, Figs. 1-2, 4-5C, 9, ¶¶[0095], [0111]; TSMC-1003, ¶¶166-68. Figures 1-2 (first embodiment), 5A (third embodiment), and 9 (fifth embodiment) disclose these features (TSMC-1003, ¶167):

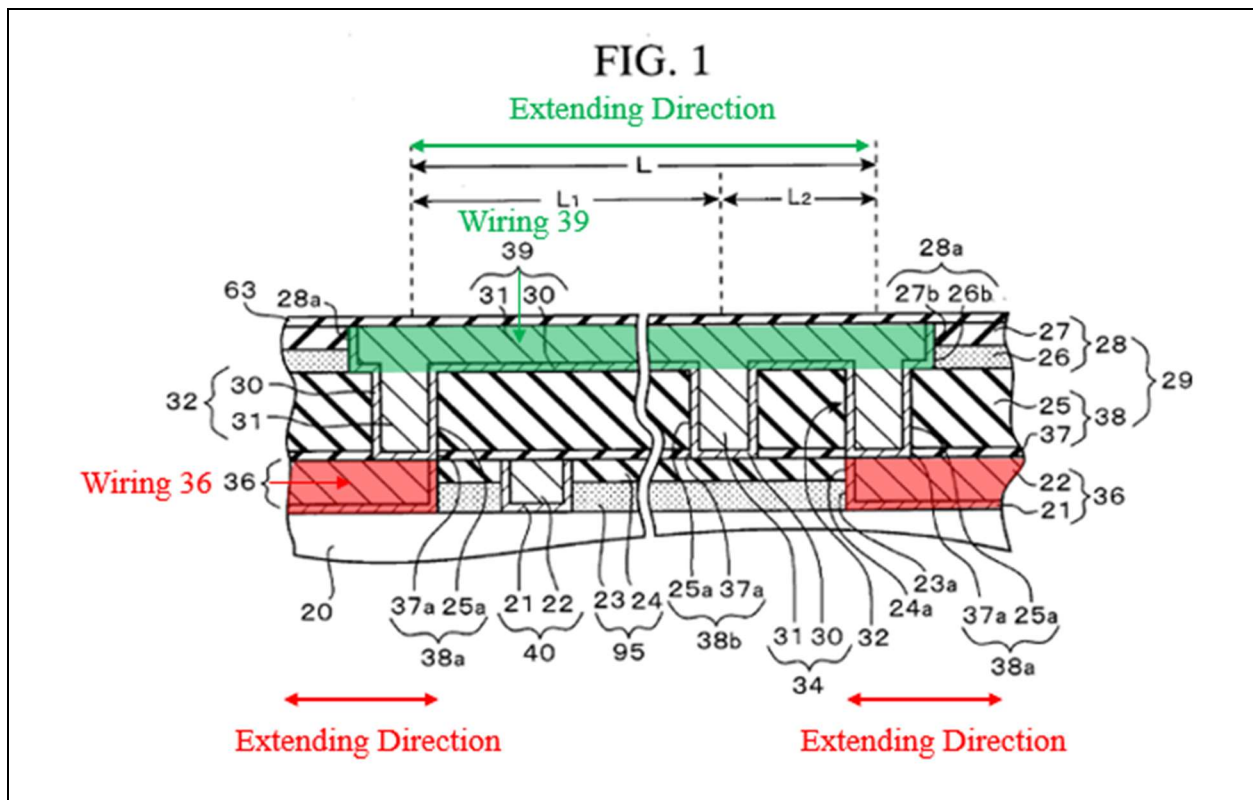


FIG. 2

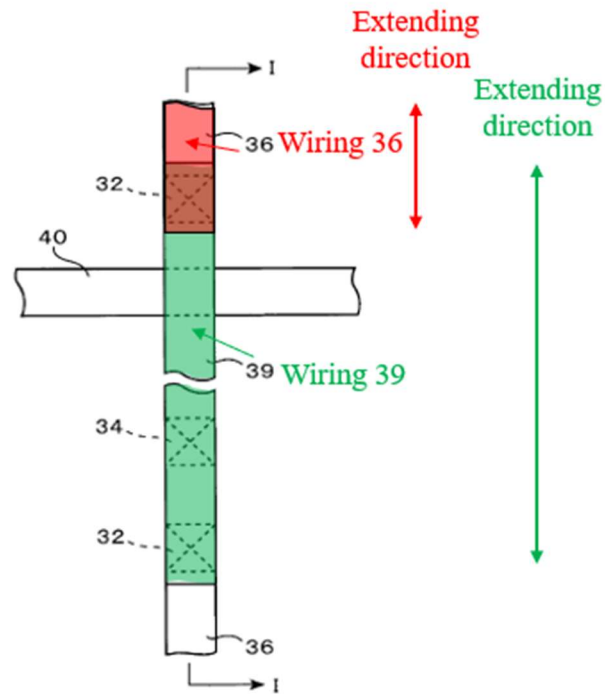


FIG. 5A

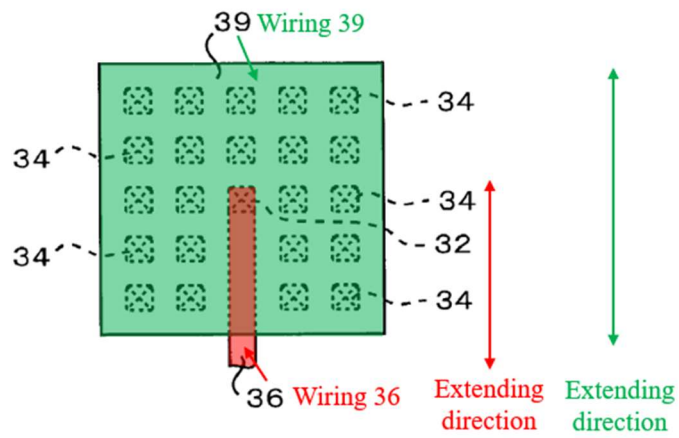
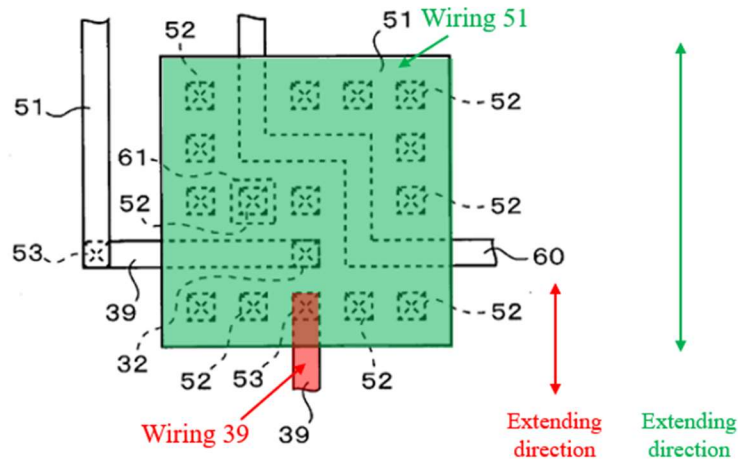


FIG. 9



10. Claim 12

For the first through third and fifth embodiments, Watanabe's dummy via (e.g., dummy plug 34) is provided on an extended line along which the first interconnect (e.g., wiring 36) extends (TSMC-1004, Figs. 2, 4-5C, 9; TSMC-1003, ¶¶169-71):

FIG. 2

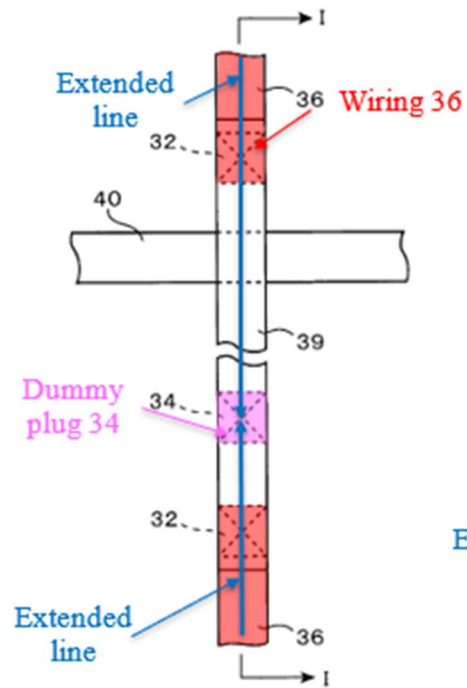


FIG. 4

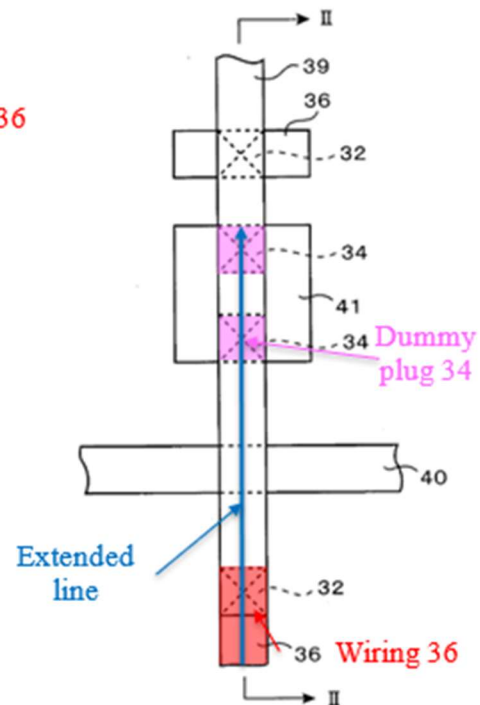


FIG. 5A

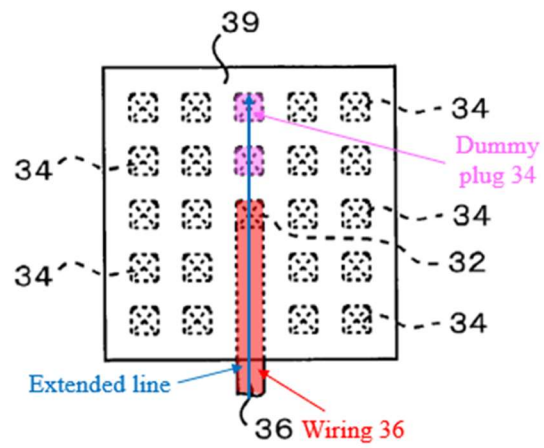
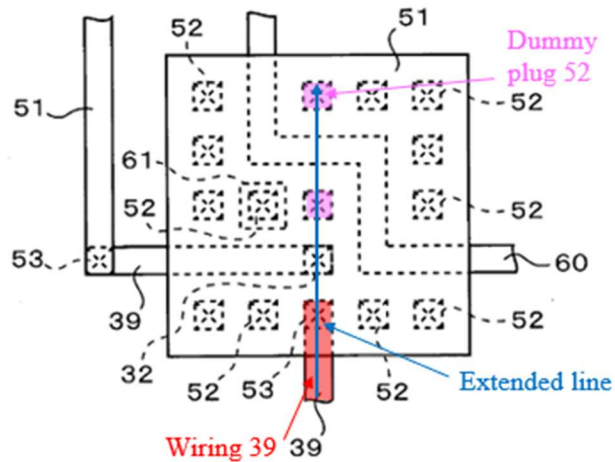


FIG. 9



11. Claim 13

The '751 patent refers to the “space” between a via and dummy via as corresponding to the distance from an edge of the via and a closest edge of an adjacent dummy via. TSMC-1001, 4:21-25. Applicable to each of Watanabe’s embodiments, Watanabe discloses that its via (e.g., “plug 32”) and dummy via (e.g., “dummy plug 34”) are spaced at a distance of 25 μm or less, teaching, for example, that “the interval between the neighboring plugs (including the plug 32 and the dummy plug 34) was fixed to 0.3 μm .”). TSMC-1004, ¶¶[0100]-[0105], [0081], [0086]-[0087]; Figs. 15A-17C; TSMC-1003, ¶¶172-77. This interval/pitch “ p_2 ” is shown below:

FIG. 16B

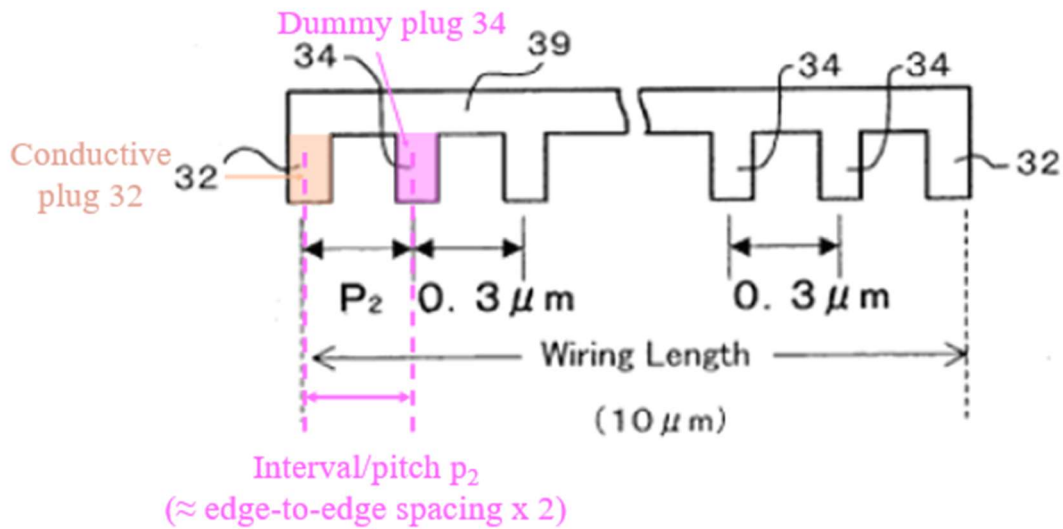
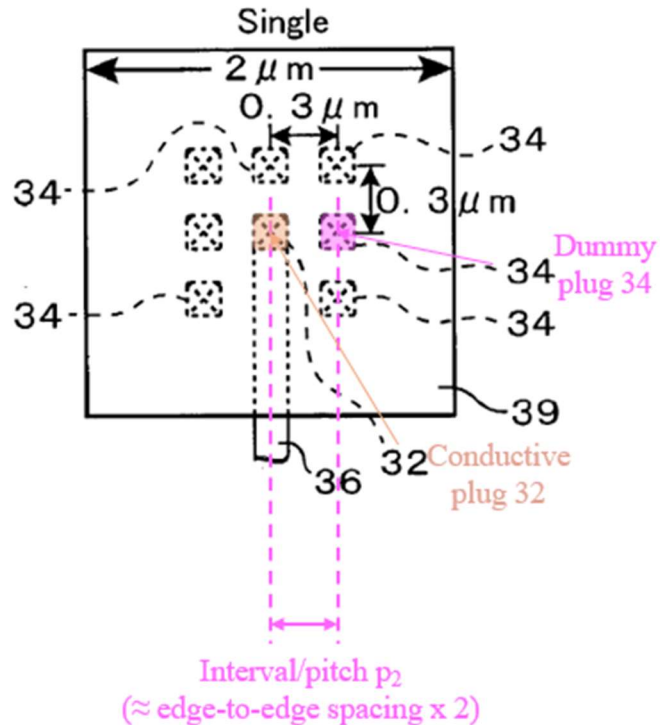


FIG. 17B



TSMC-1003, ¶174.

As shown above, the interval/pitch “ p_2 ” in Watanabe is the interval from a center of a via to a center of an adjacent dummy via, so, for example, the spacing from a right edge of the annotated conductive plug 32 to a left edge of the adjacent

annotated dummy plug 34 is necessarily less than the interval/pitch p_2 —in Watanabe’s case, the edge-to-edge spacing is approximately half the pitch interval. *Id.*

Additionally, Watanabe teaches that to prevent stress-migration, it is preferable that pitch p_2 is less than 1 μm , and more preferably less than 0.6 μm . TSMC-1004, ¶¶[0032]-[0033], [0086]-[0087], [0053], [0190]-[0191], [0193], Fig. 16A; TSMC-1003, ¶176.

12. Claim 18

In the first through third and fifth embodiments, Watanabe’s dummy via(s) (e.g., dummy plugs 34, 52) and second interconnect(s) (e.g., wirings 39, 51) are made of the same conductive film (e.g., “copper film 31,” “barrier metal layer 30”). TSMC-1004, ¶¶[0166]-[0168], [0067]-[0070], [0072], [0118], Figs. 12L-12M; TSMC-1003, ¶¶178-81. “The barrier metal layer 30 and the copper film 31...constitute the second wiring 39” and “the portion of the second wiring 39...in the dummy via hole 38*b*...is the dummy plug.” TSMC-1004, ¶[0168]; *see id.*, ¶¶[0118], [0122] (wiring buried in dummy via hole 68*b* is dummy plug 52).

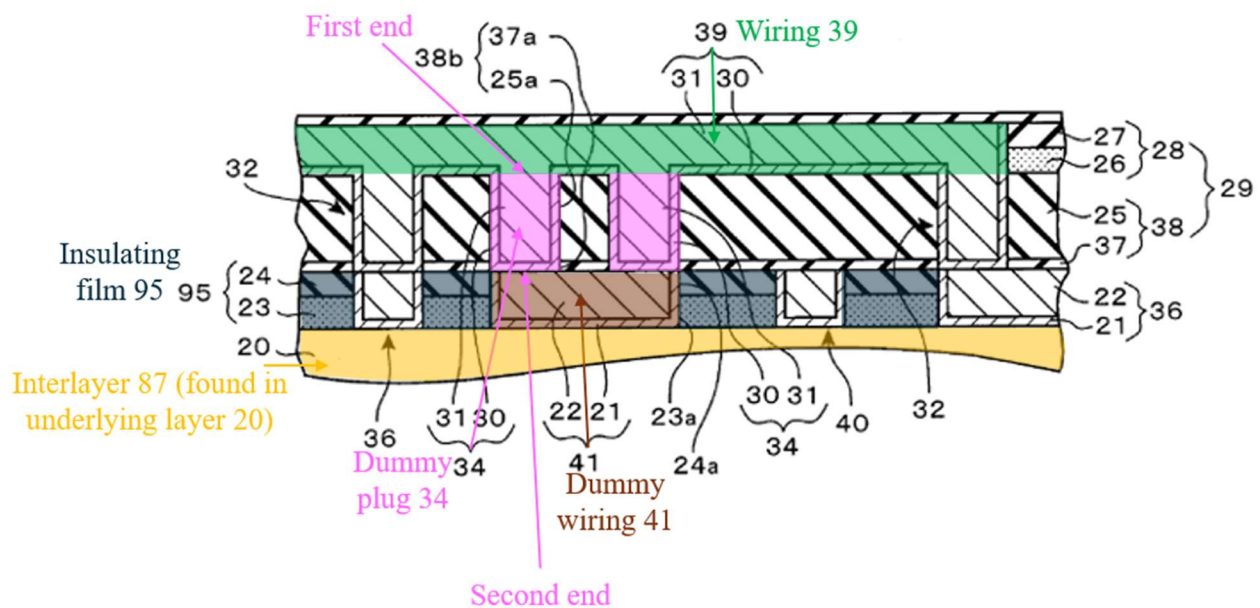
13. Claim 20

At least Watanabe’s second and fifth embodiments meet claim 20.

Embodiment 2

[illegible]

FIG. 3



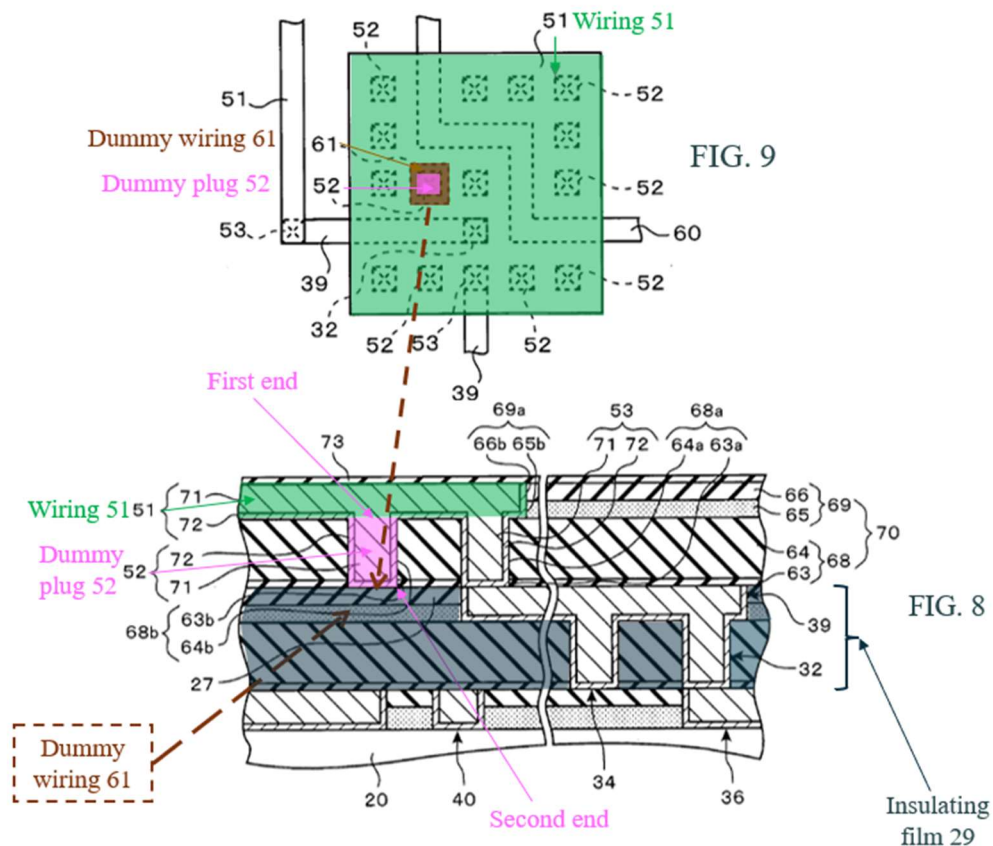
TSMC-1004, ¶¶[0089]-[0090], [0140]-[0144], Figs. 3, 12B-12D, 12M; TSMC-1003, ¶¶182-84. Underlying layer 20 also includes interlayer insulating film 87 beneath dummy wiring 41 (TSMC-1004, ¶[0173], Fig. 14), thus further surrounding dummy wiring 41 with an insulating film (i.e., interlayer insulating film 87 and insulating film 95, collectively). TSMC-1003, ¶¶183-84.

Embodiment 5

In Watanabe's fifth embodiment, the dummy via (e.g., "dummy plug 52") has a first end connected to the second interconnect (e.g., "wiring 51") and a second end connected to the first dummy interconnect (e.g., "dummy wiring 61"), the first dummy interconnect surrounded by a second insulating film (e.g., "insulating film 29"). TSMC-1004, ¶¶[0127], [0116]-[0123], [0140]-[0144], Figs. 8-9, 12B-12D, 12M; TSMC-1003, ¶¶185-87; *see also supra*, §§VI(A)(2)(e), VI(A)(3).

As explained above, dummy wiring 61 is formed in the same layer as wiring 39 with dummy plug 52 connected to dummy wiring 61. TSMC-1004, ¶[0127]. Wiring 39 is formed in insulating film 29. *Supra*, §§VI(A)(2)(c), VI(A)(3)(a). "Dummy wiring 61" is formed in the same insulating film (e.g.,

“insulating film 29”)⁶ as wiring 39 in Figure 8. TSMC-1003, ¶186. Annotated Figures 8-9 show the approximate location of “dummy wiring 61” when the cross-sectional view otherwise shown in Figure 8 is drawn through dummy wiring 61. Dummy wiring 61 is surrounded by insulating film 29 (TSMC-1004, Figs. 8-9; TSMC-1003, ¶186):



⁶ Watanabe's Figure 8 is similar to the first-fourth embodiments, and adds third layer wiring 51. *See* TSMC-1004, ¶¶[0116]-[0117]. Films 25 and 26 are labeled in the first and second embodiments (e.g., Figures 1, 3) and manufacturing process (e.g., Figures 12A-12d). TSMC-1003, ¶186, n.7; *see* TSMC-1004, ¶¶[0066]-[067], [0150]-[0152], *supra*, §VI(A)(2)(c).

B. GROUND 2: Watanabe combined with Kamoshima renders Claims 3-4 and 15-16 unpatentable

Claims 3-4 and 15-16 are obvious over Watanabe and Kamoshima. TSMC-1003, ¶¶188-226.

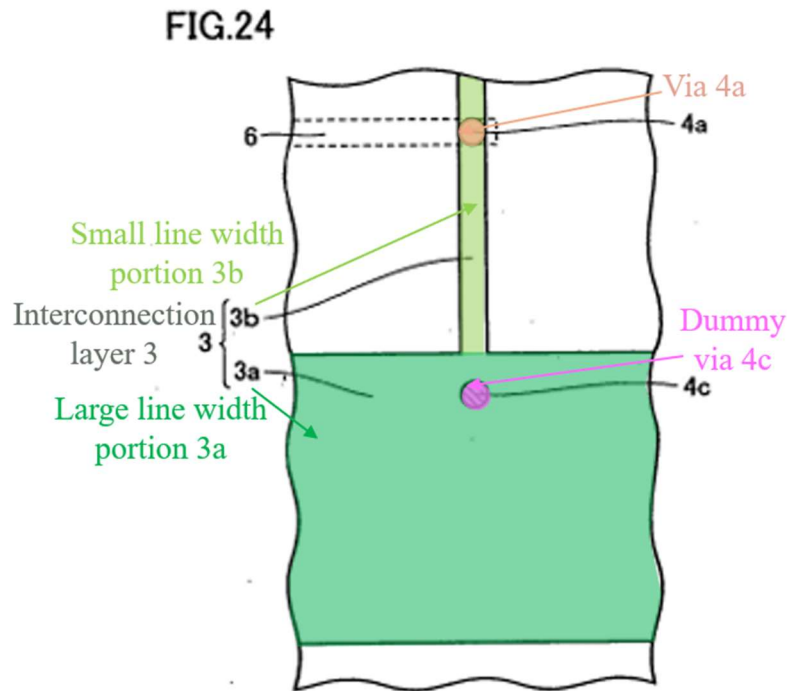
1. Kamoshima

Because Kamoshima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 patent purports to address (e.g., interconnect reliability), Kamoshima is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1009, ¶¶[0002], [0004]-[0007]; TSMC-1003, ¶¶81-84.

Kamoshima discloses interconnection structures for semiconductor devices that “suppress concentration of voids in an interconnection under a via due to stress migration.” TSMC-1009, ¶¶[0002], [0008]. Kamoshima uses dummy vias so that microvoids in an interconnection layer 3 are distributed between a via and dummy via, to suppress the concentration of microvoids in the area under the via. *Id.*, ¶¶[0088], [0097]-[0098].

Kamoshima forms interconnection layer 3 by depositing conductive material (e.g., “barrier metal layer 2,” “copper layer 3”) in an interconnect trench formed in “insulating layer 1.” *Id.*, ¶¶[0043]-[0044]. Interconnection layer 3 can have different shapes, with Figure 15 disclosing a constant width interconnection layer 3, and Figures 23-27 disclosing interconnection layer 3 having an interconnection portion with a small line width 3b branching off an interconnection portion with a

large line width 3a. *See id.*, ¶¶[0094]-[0103], Figs. 23-27. Kamoshima teaches arranging via 4a (for connection to another interconnect layer) along small line width portion 3b and arranging dummy via 4c in the vicinity of a “connection portion” between interconnection portions 3a, 3b (*id.*, ¶¶[0095], [0099], Fig. 24):

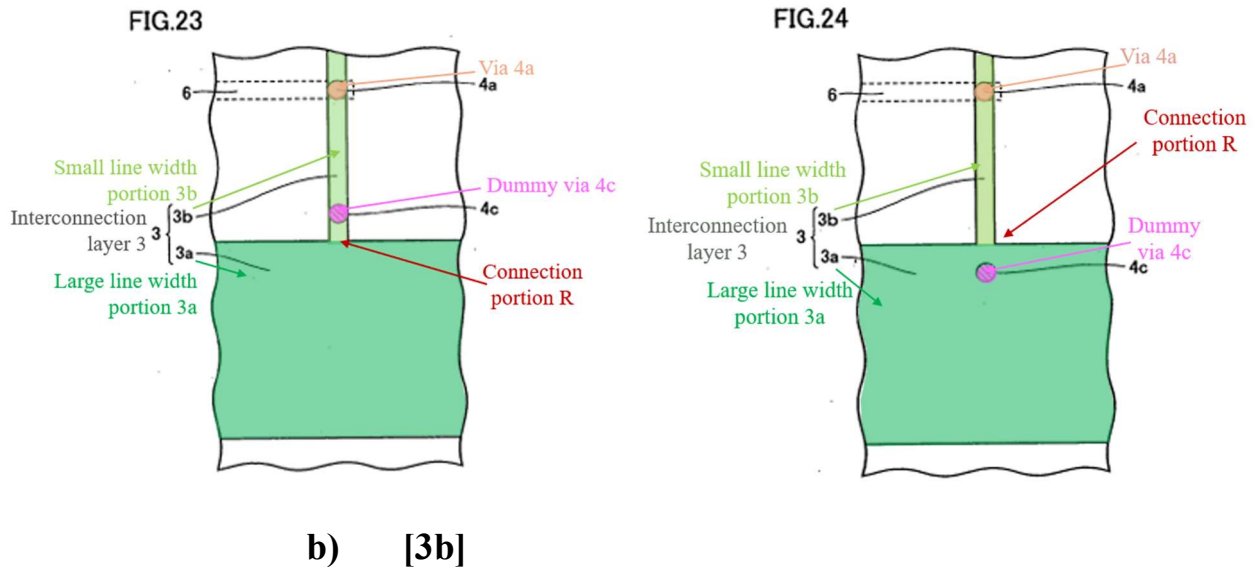


2. Claim 3

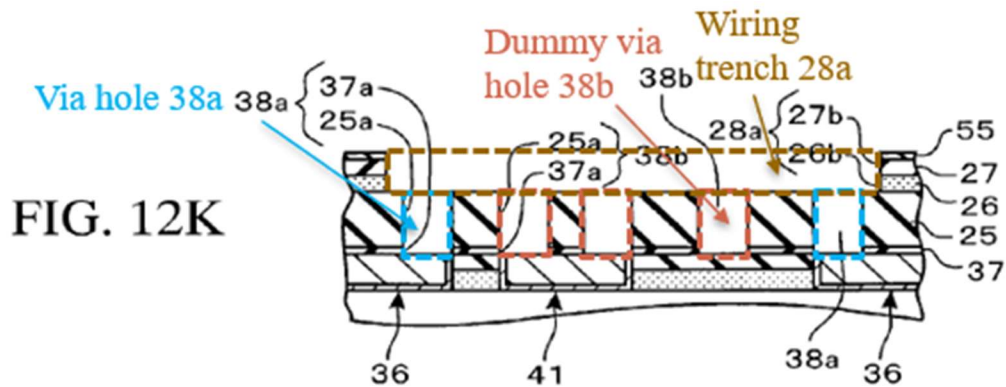
a) [3a]

Kamoshima discloses an interconnection layer shape with large line width portion 3a and small line width portion 3b, and as understood by a POSITA, an interconnect trench with a first interconnect trench portion and a second, smaller width interconnect trench portion to form large line width and small line width portions 3a, 3b, respectively. TSMC-1009, ¶¶[0002], [0094]-[0103], Abstract,

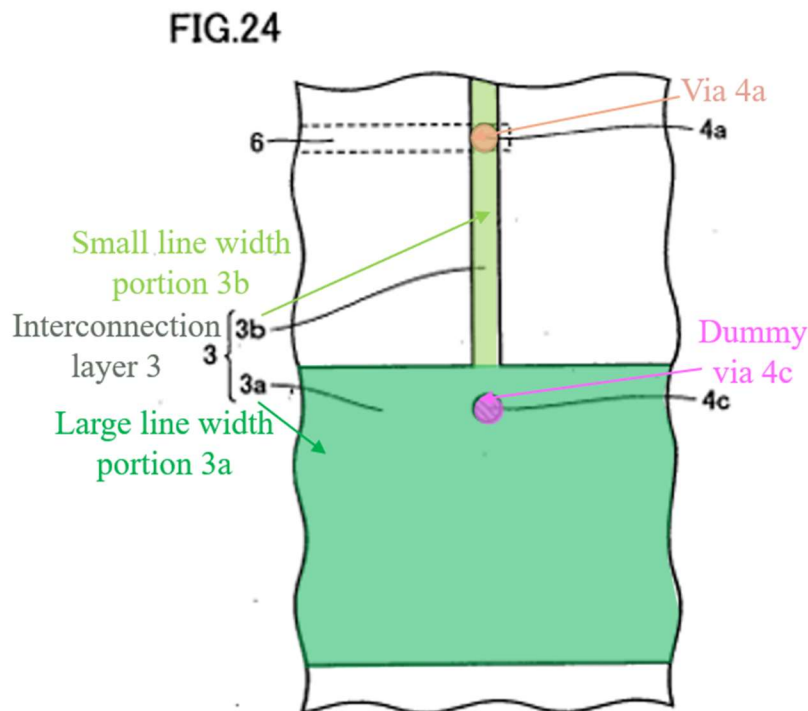
Figs. 23-27; TSMC-1003, ¶¶189-94. Kamoshima further discloses interconnection formation by depositing conductive material, such as a barrier metal layer and copper layer, in an interconnect trench formed in an insulating layer. *See* TSMC-1009, ¶¶[0043]-[0044]; TSMC-1003, ¶191. Moreover, Kamoshima teaches having via 4a in small line width portion 3b and dummy via 4c in the vicinity of “connection portion R” between the two interconnection portions 3a, 3b (*see* TSMC-1009, Figs. 23-24):



Watanabe discloses that the via hole (e.g., “via hole 38a,” “via hole 68a”) and the dummy hole (e.g., “dummy via hole 38b,” “dummy hole 68b”) are connected to the interconnect trench (e.g., “wiring trench 28a,” “wiring trench 69a”). TSMC-1004, ¶¶[0118]-[0121], [0159]-[0165], Figs. 1, 3, 8, 12J-12K; TSMC-1003, ¶201; *supra*, §VI(A)(2)(d).



Kamoshima similarly teaches via 4a and dummy via 4c connected to interconnection layer 3. TSMC-1009, Fig. 24; TSMC-1003, ¶¶202-03, *supra*, §VI(B)(1).



Kamoshima motivates a POSITA to use an interconnection layer with large and small width portions – formed using an associated interconnect trench design – and positioning the via (for connection to another interconnect) along the small

line width portion and the dummy via in the vicinity of the connection point between the respective interconnect portions. TSMC-1003, ¶¶195-98, 204.

Kamoshima teaches that such an interconnect/via/dummy via arrangement causes microvoids that would otherwise distribute between the via and the dummy via to further concentrate under the dummy via before reaching the via in the small line width portion. *Id.*; TSMC-1009, ¶¶[0088], [0097]-[0099]. Thus, Kamoshima teaches a known design choice for suppressing microvoids. TSMC-1003, ¶197.

Following Kamoshima's teachings, a POSITA would update Watanabe's step of forming in the first insulating film (e.g., "insulating film 29," "insulating film 70"),...an interconnect trench (e.g., "wiring trench 28a," "wiring trench 69a") shaped to create an interconnect (e.g., "wiring 39," "wiring 51") with first and second interconnect trench portions corresponding to a large line width portion and a small line width portion branched therefrom analogous to Kamoshima's interconnection layer 3 from Figures 23-24. *Id.*, ¶¶198, 200. Watanabe's plug 32/53 would be connected to the small line width portion and dummy plug 34/52 would be connected in the vicinity of "connection portion R" between the two interconnection portions 3a, 3b. *Id.* By virtue of its branched interconnect shape, Kamoshima's design further enhances the suppression of microvoids in addition to Watanabe's design in any of the first to third and fifth embodiments. *Id.*; *see also* TSMC-1033, ¶¶[0056]-[0057], [0112]-[0114] ("A sample without the narrow

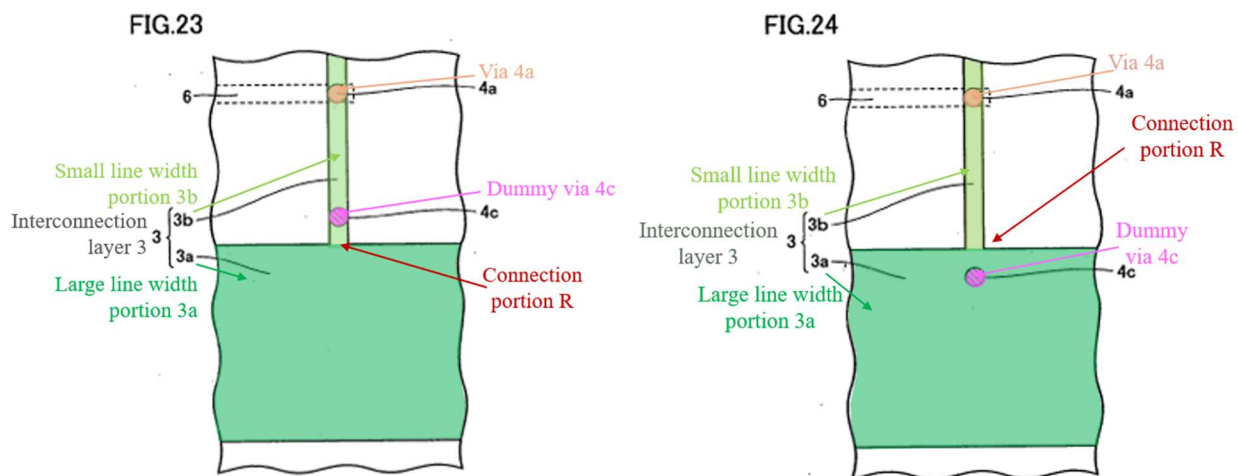
wiring and a sample having the narrow wiring length of 2 μm was checked.... The sample without the narrow wiring showed the defective factor of about 1%. The sample with the narrow wiring of about 2 μm in length showed the defective factor of about 0%.”).

A POSITA would have expected success when modifying Watanabe in this manner. Both Watanabe and Kamoshima relate to forming an interconnect connected to both a via (to connect to another interconnect) and dummy via, where the dummy via is present to suppress voids from concentrating in the via. *See* TSMC-1004, ¶¶[0070]-[0073], [0117]-[0122], Figs. 1-5C, 8-9; TSMC-1009, ¶¶[0085]-[0086], [0088], [0094]-[0099], Figs. 15-16, 23-27; TSMC-1003, ¶199. Further, the modification would have been straightforward, involving etching the interconnect trench in the desired branched shape with appropriate trench portion widths, which was well within the capabilities of a POSITA at the time and taught by Kamoshima, and readily achieved with the manufacturing processes already used in Watanabe. TSMC-1003, ¶199.

3. Claim 4

Kamoshima teaches that the dummy hole for dummy via 4c is connected to the branch point (e.g., “connection point R”) between the first and second interconnect trench portions (e.g., different size trench portions associated with “interconnection portion with a large line width 3a” and “interconnection portion

with a small line width 3b,” respectively) or to the interconnect trench near the branch point (e.g., “connection portion R”). TSMC-1009, ¶¶[0094]-[0095], [0099]; TSMC-1003, ¶205. Figures 23 and 24 disclose these features (and *cf.* with dummy vias 110B in Figure 4 of ’751 patent):



It was obvious to combine these teachings of Kamoshima and Watanabe for the reasons discussed above. *Supra*, §VI(B)(2); TSMC-1003, ¶206.

4. Claim 15

Claim 15 recites the shape of the second interconnect analogous to the shape of the interconnect trench in claim 3, and the via is connected to the second interconnection portion of the second interconnect, just like claim 3. Claim 15 was obvious based on Watanabe and Kamoshima according to the same analysis presented for claim 3. *Supra*, §VI(B)(2); TSMC-1003, ¶¶208-21.

5. Claim 16

Claim 16 recites the location of the dummy via at or near the branch point between the first and second interconnect portions, like claim 4. Claim 16 was obvious based on Watanabe and Kamoshima according to the same analysis presented for claim 4. *Supra*, §VI(B)(3); TSMC-1003, ¶¶222-26.

C. GROUND 3: Watanabe combined with Kamoshima and Fukazawa renders Claim 17 unpatentable

Claim 17 is obvious over Watanabe in view of Kamoshima and Fukazawa. TSMC-1003, ¶¶227-37.

1. Fukazawa

As described above, both Watanabe and Kamoshima disclose dummy vias connected to an interconnect. *Supra*, §§VI(A)-(B). Fukazawa provides the additional teaching of a rectangularly-shaped via positioned such that its longer side is along a same direction as a longer side of an interconnect portion to which it is connected. Because Fukazawa is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 patent purports to address (e.g., interconnect reliability), Fukazawa is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1010, Abstract, ¶¶[0001], [0004]-[0007]; TSMC-1003, ¶¶89-92.

More specifically, Fukazawa discloses dummy contact 43, which is a dummy via, connected to an upper layer interconnect (e.g., “upper layer Cu wiring 41”), and not connected to a lower layer interconnect. TSMC-1010, ¶[0017], Fig.

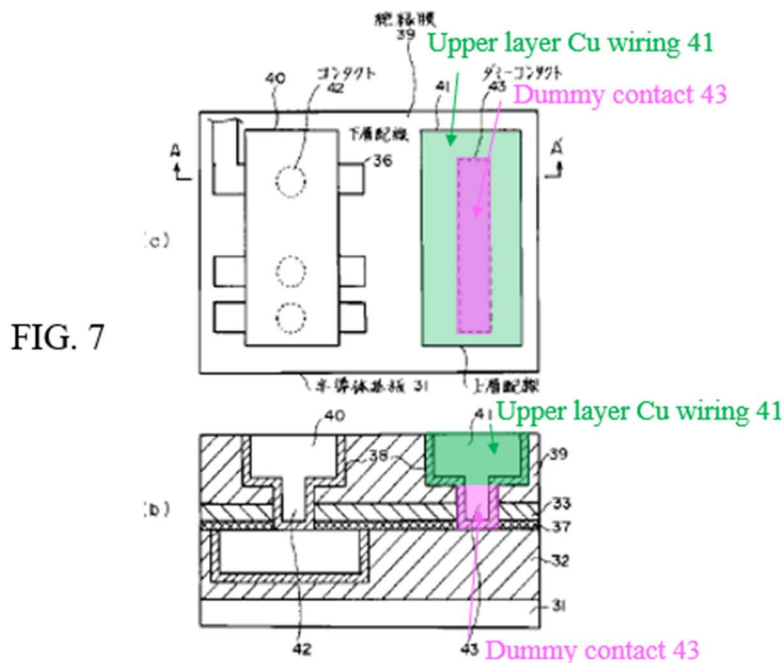
7. To enhance mechanical strength, Fukazawa's dummy contact 43 is arranged in a rectangular shape (described as "column-shaped") in a plan view, shown in Figure

7. *Id.*, ¶¶[0017]-[0018] ("the dummy contacts are column-shaped"), Fig. 7.

2. Claim 17

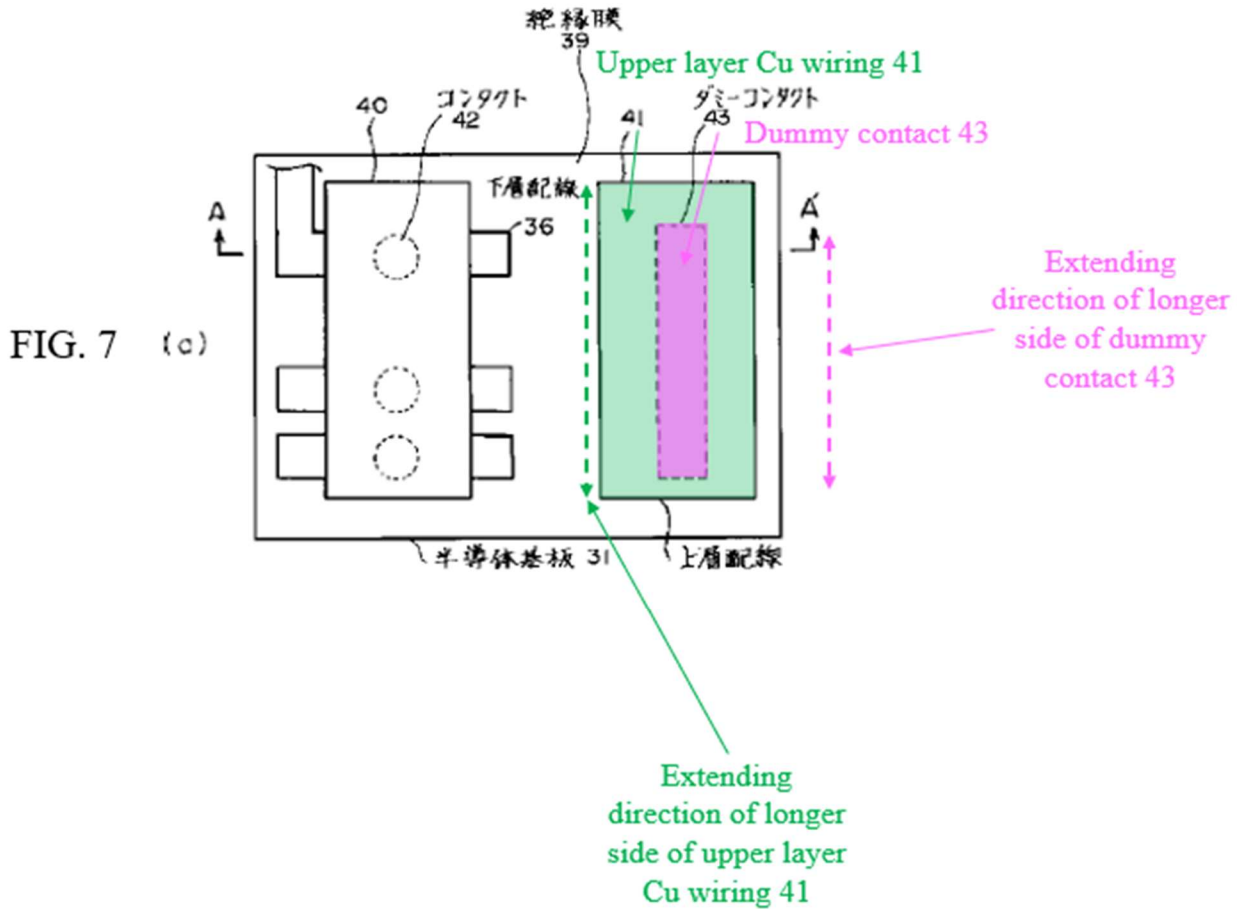
a) [17a]

Fukazawa discloses a dummy via (e.g., "dummy contact 43" and "barrier metal layer 38," hereafter collectively "dummy contact 43") connected to an upper layer interconnect (e.g., "upper layer Cu wiring 41" and "barrier metal layer 38," hereafter collectively "upper layer Cu wiring 41"). TSMC-1010, ¶[0017], Fig. 7; TSMC-1003, ¶230. Fukazawa's "dummy contact 43" has a substantially rectangular shape in a plan view (TSMC-1010, ¶¶[0017]-[0018], Fig. 7; TSMC-1003, ¶230):



b) [17b]

A longer side of dummy contact/via 43 is provided along a same direction as a longer side of a correspondingly rectangular interconnect (“upper layer Cu wiring 41”) (TSMC-1010, ¶¶[0017]-[0018], Figure 7; TSMC-1003, ¶231):

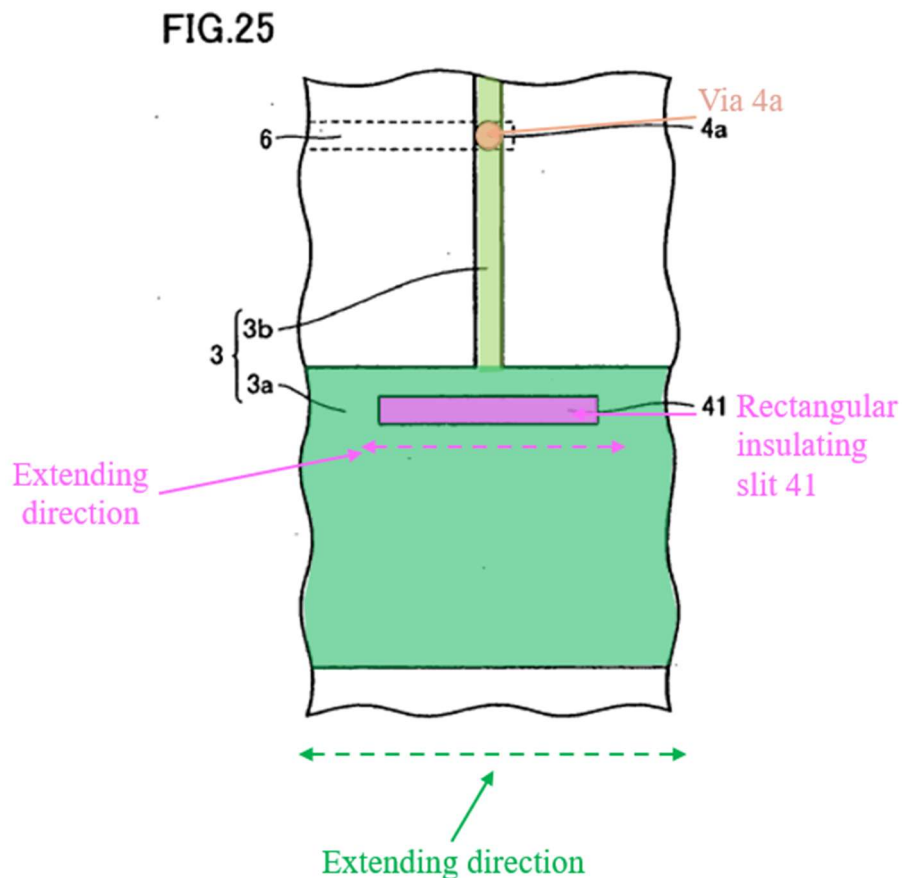


c) Combining Watanabe, Kamoshima, and Fukazawa

In view of Fukazawa, it was obvious to use a rectangularly-shaped via in the wider interconnect portion of Watanabe’s second interconnect (after modified in view of Kamoshima to have a branched interconnect structure – *supra*, §§VI(B)(2), VI(B)(4)). A POSITA was motivated to use the rectangularly-shaped via and to

position it along a longer side of the wider portion of the branched interconnect to further reduce the migration of vacancies to (and thus the formation of voids within) a real via positioned on the narrow branch of the interconnect. TSMC-1003, ¶¶232-37.

Indeed, Kamoshima teaches using a rectangular structure (e.g., insulating slit 41) positioned in such a manner (such that a longer side of the rectangular structure extends in a same direction as a longer side of the wider interconnect portion) to suppress vacancy migration to via 4a (see TSMC-1009, ¶¶[0102]-[0105], Fig. 25; TSMC-1003, ¶233):



A POSITA understood that positioning a rectangular dummy via in the same position as insulating film 41 would have similarly suppressed vacancy migration (similar to dummy vias 4c in Kamoshima's Figures 23-24 embodiments), with the added benefit of providing a larger area of vacancy interception due to the rectangular shape and its position along a length of the wider portion of the interconnect (and thus perpendicular to the narrow branch portion). TSMC-1003, ¶234.

Additionally, a POSITA was motivated by the increased mechanical strength afforded to the overall wiring structure by the rectangular (i.e., column-shaped) dummy via, as taught by Fukazawa. *Id.*, ¶235; TSMC-1010, ¶[0018] (“[T]he contacts are column-shaped.... Because of this structure, sufficient mechanical strength is ensured even when the insulating film comes off, thereby improving the strength of the wiring structure.”).

Such a modification had a reasonable expectation of success. TSMC-1003, ¶236. As described previously, a POSITA was capable of creating a branched interconnect. *Id.* Claim 17 merely adds that the dummy via has a rectangular shape and is connected to the wider interconnect portion analogous to the position of insulating slit 41 in Kamoshima's Figure 25 embodiment. *Id.* This would have been reliably accomplished using standard processing techniques at the time. *Id.* Indeed, other references at the time demonstrate that rectangular vias were known

and used and that positioning them where desired was easily achieved. *See* TSMC-1008, 9:45-47 (“the opening of the via-hole may have any configuration, such as a square, rectangle or circle.”); TSMC-1013, 9:45-49, 10:1-4 (“[D]ummy via holes of only rectangles or lines may also be formed.”).

D. GROUND 4: Watanabe combined with Iizuka renders Claim 9 unpatentable

Claim 9 is obvious over Watanabe and Iizuka. TSMC-1003, ¶¶238-47.

1. Iizuka

Because Iizuka is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the ’751 patent purports to address (e.g., interconnect reliability), Iizuka is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1008, 1:7-14; 2:39-45; TSMC-1003, ¶¶85-86.

Iizuka describes methods for manufacturing semiconductor devices, specifically focused on improving the filling of small-diameter via holes to form reliable conductive plugs between interconnect layers. TSMC-1008, Abstract, 1:7-14, 2:39-45. Iizuka acknowledges that via-holes can have various planar configurations, stating: “the opening of the via-hole may have any configuration, such as a square, rectangle or circle.” *Id.*, 9:45-47.

2. Claim 9

Watanabe discloses both vias (e.g., “conductive plug 32”) and dummy vias (e.g., “dummy plug 34”). TSMC-1004, ¶[0083]; TSMC-1003, ¶¶239-40; *supra*,

§VI(A)(2)(e). Along with Watanabe’s plan view figures disclosing these features as square, Watanabe’s simulation model explicitly describes both conductive plug 32 and dummy conductive plug 34 as a “circular cylinder,” thus disclosing circular vias and dummy vias. TSMC-1004, ¶[0083], Figs. 1, 3.

Iizuka confirms that vias (and thus dummy vias) can have various planar shapes, such as a square, rectangle, or circle, and that selecting a specific shape was a simple design choice. TSMC-1008, 9:45-47 (“[T]he opening of the via-hole may have any configuration, such as a square, rectangle or circle.”); TSMC-1003, ¶¶241-42. Iizuka’s description of via-hole 6 having a “diameter” (TSMC-1008, 6:60-63) similarly discloses a circular via shape, since the geometrical term “diameter” corresponds with circular shapes. TSMC-1003, ¶241.

A POSITA, considering Watanabe’s device structure and its disclosed use of circular vias in simulation models, would have found it obvious to implement both Watanabe’s conductive plug 32 and dummy plug 34 with a substantially circular shape in a plan view. *Id.*, ¶242-47. This modification would have been based on Iizuka’s explicit teaching that circular vias were a known, interchangeable design alternative to square or rectangular vias as well as the widespread knowledge of this at the time. *Id.* Motivations for selecting a circular shape included simple design choice, advantages in manufacturing process control (such as more uniform etching and filling characteristics), more favorable stress distribution around a

circular opening, or consistency with Watanabe's own simulation models. *Id.*, ¶¶243-45; *see also* TSMC-1038, 7:61-67.

Additionally, the '751 patent taught no criticality associated with having a circular via or dummy via shape, and a POSITA would have expected circular-shaped vias to operate substantially the same as other shapes. *Id.*, ¶¶244, 246.

Furthermore, a POSITA would have expected success when implementing circular vias. As demonstrated by Iizuka (and other references) as well as the modeling of Watanabe, circular vias (including dummy vias) were standard in the industry and their fabrication was well understood. *Id.*, ¶247; *see* TSMC-1013, 8:47-52; TSMC-1014, ¶¶0091]-[0092]; TSMC-1038, 7:61-67.

E. GROUND 5: Hasunuma anticipates Claims 1, 5-6, 9, 11-14, and 18-19

Hasunuma anticipates claims 1, 5-6, 9, 11-14, and 18-19. TSMC-1003, ¶¶248-305.

1. Hasunuma

Because Hasunuma is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 patent purports to address (e.g., interconnect reliability), Hasunuma is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1005, ¶¶[0003], [0005], [0079]-[0086]; TSMC-1003, ¶¶71-74.

Hasunuma teaches forming a semiconductor device having substrate 1, a first interconnect comprising conductive layer 14, an overlying insulating film

comprising SiCN film 3, low relative dielectric constant film 4, and SiC film 2, and a second interconnect comprising conductive layer 26 formed within that insulating film. TSMC-1005, Figs. 1A-8, ¶¶[0090]-[0108]. A functional via (conductive via plug 27), a dummy via (reinforcing plug 28), and the second interconnect (conductive layer 26) are simultaneously formed in corresponding recesses in the insulating film using a dual damascene process. *Id.*, ¶¶[0101], [0106]-[0109], Figs. 7-8.

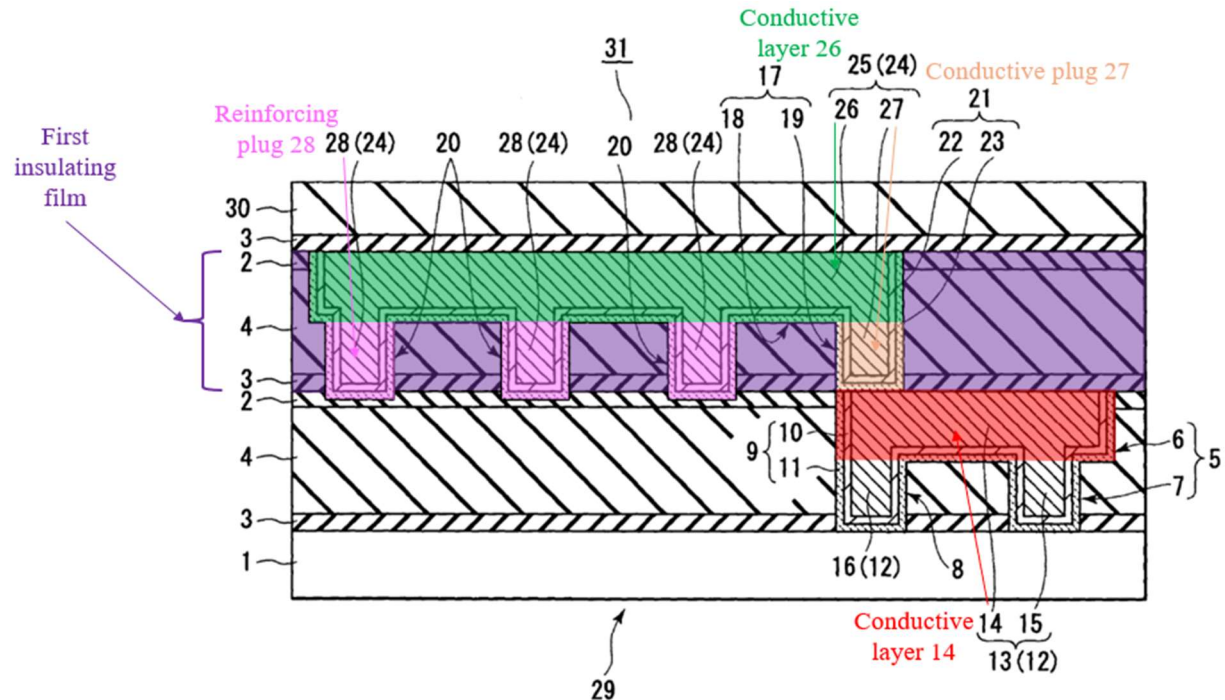


FIG. 8

Like the '751 patent, Hasunuma addresses reliability problems arising from stresses in interconnect structures. *Id.*, ¶¶[0079]-[0086]; TSMC-1001, 2:23-40. Hasunuma similarly incorporates dummy vias (reinforcing plugs 28) to address

these stresses, although with the express intent to reinforce/strengthen the structure rather than absorb vacancies as in the '751 patent. *See* TSMC-1005, ¶[0114].

2. Claim 1

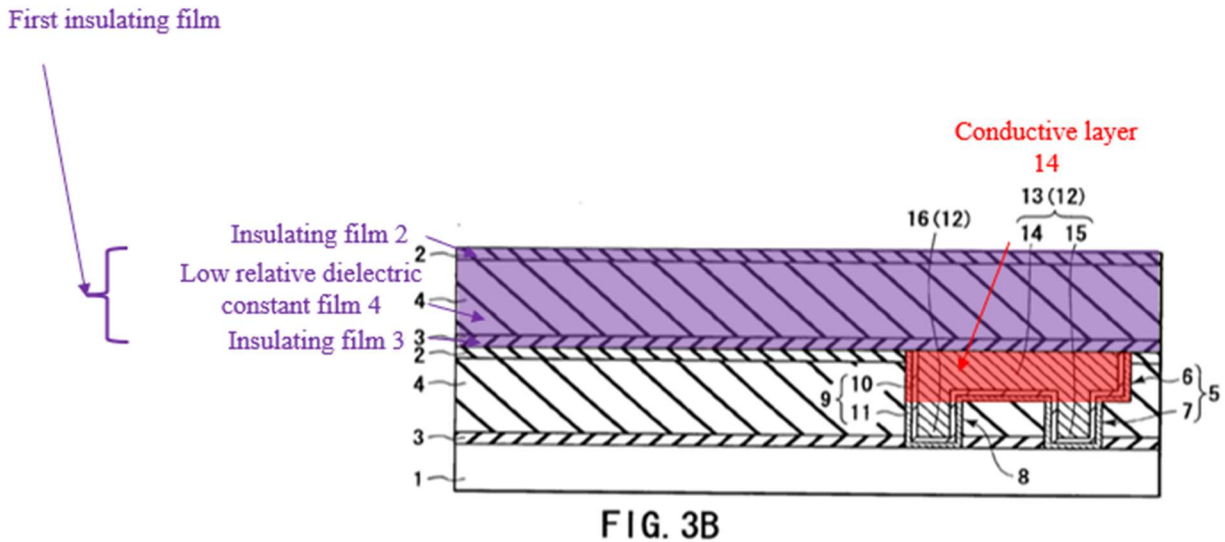
a) 1[pre]

Hasunuma teaches a “method for manufacturing [a] semiconductor device,” satisfying claim 1’s preamble. TSMC-1005, ¶[0088], Abstract, Figs. 1A-8; TSMC-1003, ¶249.

b) 1[a]

Hasunuma discloses forming a first interconnect (e.g., “conductive layer 14” and “barrier metal film 9,” hereinafter collectively “conductive layer 14”) on a semiconductor substrate (e.g., “Si substrate 1”). TSMC-1005, ¶¶[0094]-[0098], Figs. 2A-3A; TSMC-1003, ¶¶250-52.

Hasunuma explains that “Si substrate 1...is fed into a treatment chamber of a sputtering device...for forming a plating seed layer (film) 12a which is a base (substrate) of the conductive layer 14. Thereafter, materials forming the conductive layer 14...are provided on the surface of the Ta film 10.” TSMC-1005, ¶[0096]. “As a result,...Cu wiring layer 13 of the first layer including the Cu conductive layer 14...[is] formed.” *Id.*, ¶[0098], Fig. 3A.



d) 1[c]

Hasunuma discloses forming in the first insulating film (e.g., combination of films 3, 4, 2), a via hole (e.g., “recess [for conductive plug] 19”) connected to the first interconnect (e.g., “conductive layer 14”), a dummy hole (e.g., “recess [for reinforcing plug] 20”) arranged so as to be incapable of having current flow therethrough, and an interconnect trench (e.g., “recess [for the conductive layer] 18”) connected to the via hole and the dummy hole. *Id.*, ¶¶[0101]-[0104], Fig. 4; TSMC-1003, ¶¶255-60. Hasunuma explains that “a recess for the wiring layer 17 of the second layer is formed for forming a conductive layer 26 and conductive plug 27....” TSMC-1005, ¶[0101]. “[R]ecess 17 is formed in the two-stage structure including a **recess for the conductive layer 18** in the top and a **recess for the conductive plug 19** in the bottom.” *Id.* “[T]hree **recesses for the first**

reinforcing plugs 20 for forming the first reinforcing plugs 28 are formed integrally with the recess 18.” *Id.*, ¶[0103].

FIG. 4

Indeed, no current would flow through recesses 20 or “reinforcing plugs 28” formed therein. TSMC-1003, ¶257. These “dummy” recesses 20 and “dummy” reinforcing plugs 28 are only connected on one end to an active circuit element (i.e., “conductive layer 26”), while the other end is not connected to a second active circuit element. TSMC-1005, ¶[0104] (“there is no problem as long

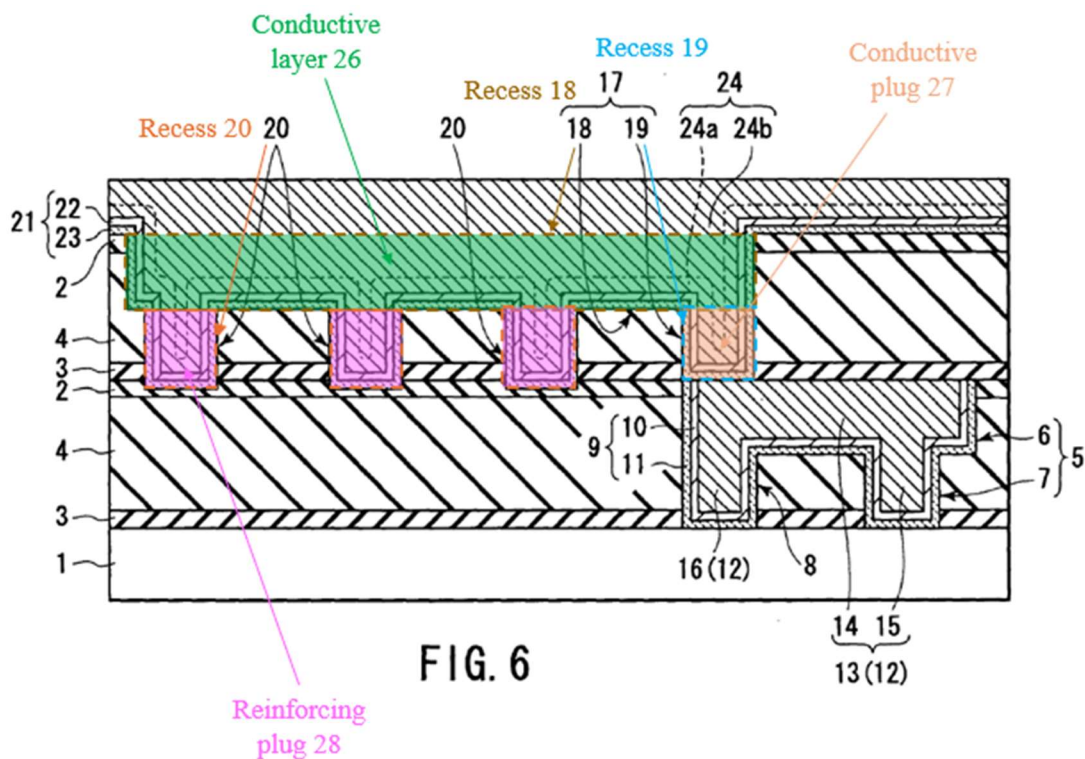
as...first reinforcing plug 28...**is not electrically connected** to the essential wiring layer...provided below the plug.”), Figs. 4, 8. Thus, dummy recesses 20 and dummy plugs 28 do not constitute parts of a closed circuit in actual use of the device. TSMC-1003, ¶257. Instead, current flows between Hasunuma’s conductive layer 14 and conductive layer 26 through conductive plug 27 (formed in recess 19), which constitute parts of a closed circuit in actual use of the device. *See* TSMC-1005, ¶[0101] (“conductive plug 27...is formed to be electrically connected to the conductive layer 26..., and comprises the conduction path to be actually energized together with the conductive layer 26. That is, the conductive layer 26 and conductive plug 27 comprise a wiring layer...25 which is actually energized to function as the essential wiring.”). Moreover, Hasunuma’s device would still be operable if dummy recesses 20 and dummy plugs 28 were omitted, because current would still flow through the active circuit elements, i.e., conductive layers 14 and 26 and conductive plug 27, during actual use of the device. TSMC-1003, ¶258.

In sum, in addition to Hasunuma describing reinforcing plugs 28 in recesses 20 as “dummy” plugs (*see* TSMC-1005, ¶[0109]), recesses 20 are “arranged so as to be incapable of having current flow,” because they do not constitute parts of a closed circuit in actual use of the device and Hasunuma’s device would still function even if dummy recesses 20 were omitted. TSMC-1003, ¶259.

e) $1[d]$

Hasunuma discloses depositing a conductive material (e.g., “Cu film 24” having “Cu plating seed layer 24a” and “Cu plating film 24b,” and “barrier metal film 21”) in the via hole (e.g., “recess 19”), the dummy hole (e.g., “recess 20”) and the interconnect trench (e.g., “recess 18”), thereby forming a via (e.g., “conductive plug 27” and “barrier metal film 21,” hereafter collectively “conductive plug 27”), a dummy via (e.g., “reinforcing plug 28” and “barrier metal film 21,” hereafter collectively “reinforcing plug 28”) and a second interconnect (e.g., “conductive layer 26” and “barrier metal film 21,” hereafter collectively “conductive layer 26”).

TSMC-1005, ¶¶[0104]-[0110], Figs. 5-8; TSMC-1003, ¶¶261-62.



Hasunuma explains that “Cu plating film 24b is provided on the surface of the Cu plating seed layer 24a.... Cu plating film 24b is formed integrally with the Cu plating seed layer 24a. Accordingly,...Cu film 24 of the second layer is formed which is the forming material of the conductive layer 26, conductive plug 27, and first reinforcing plugs 28.” TSMC-0105, ¶[0107].

3. Claim 5

Hasunuma’s first insulating film (e.g., combination of layers 3, 4, 2) has a multilayer structure including a SiN film and a SiO₂ film. TSMC-0105, ¶[0299] (“instead of the SiC film 2, an **SiO₂ film** may also be used”; “instead of the SiCN film 3, an **SiN film** may also be used”); *see also id.*, ¶¶[0091]-[0092], [0100], [0293] (explaining that insulating films 2 and 3 can constitute SiO₂ and SiN films); TSMC-1003, ¶¶264-66; *supra*, §VI(E)(2)(c).

4. Claim 6

Each of Hasunuma’s first and second interconnects (e.g., “conductive layer 14,” “conductive layer 26”) is connected to another element (e.g., “contact plug 15,” “electronic circuit,” and other active components of the active circuit formed with the first and second interconnects) or an external electrode. TSMC-1003, ¶¶267-271. Together “wiring layer 13” (which includes first interconnect/ “conductive layer 14”) and “wiring layer 25” (which includes second

interconnect/“conductive layer 26”) form an “effective wiring area 29” that “actually functions as the wiring” of Hasunuma’s device. TSMC-1005, ¶[0110].

Hasunuma’s first interconnect (“conductive layer 14”) is formed on a semiconductor (silicon) substrate that includes active electronic circuits, where conductive plug 15 of the first interconnect secures “the conduction to the electronic circuit formed in the Si substrate 1.” *Id.*, ¶¶[0090], [0092]-[0093], Fig. 3A.

Hasunuma’s second interconnect (“conductive layer 26”) is connected to the first interconnect by the via/conductive plug 27, and thus to the “electronic circuits.” *Supra*, §VI(E)(2)(e). Furthermore, Hasunuma’s second interconnect is part of a functional multi-level wiring scheme that creates a circuit by virtue of a connection to other elements (e.g., other wiring layers, vias, or circuit components) or external electrodes (e.g., electrodes connected/bonded to Al pad 136). TSMC-1005, ¶¶[0089], [0128], [0209]-[0212], [0298], Figs. 3A, 21A; TSMC-1003, ¶270.

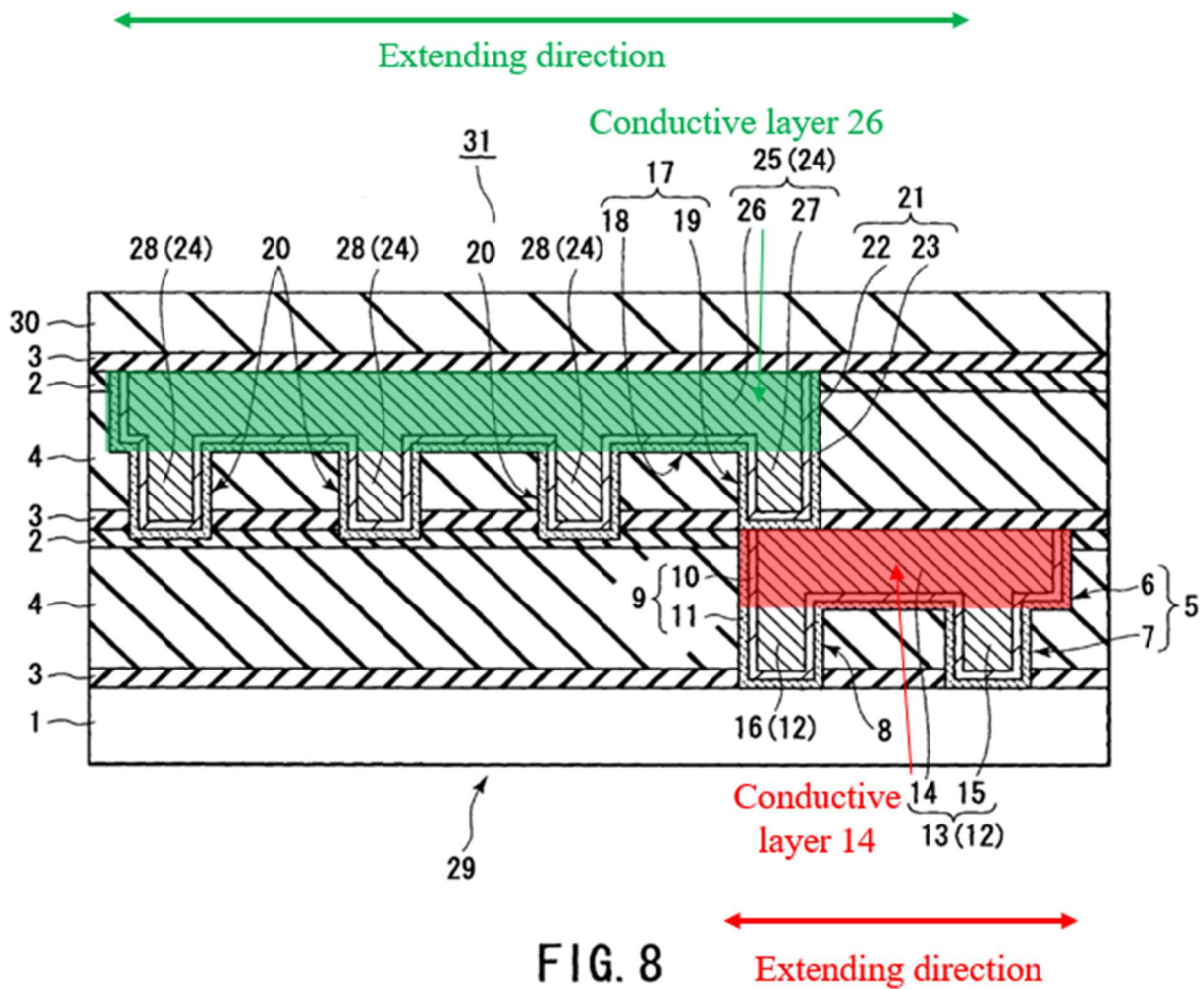
5. Claim 9

Hasunuma discloses many via structures with circular plan views, for example in Figure 19A, which shows various dummy reinforcing plugs 125 and conductive plugs 27 as circular:

that Hasunuma's reference to the "diameters" of its vias and dummy vias discloses that these structures likewise have a substantially circular cross section in plan view, just as shown in Figure 19A. *Id.*, ¶¶273-75.

6. Claim 11

Figure 8 discloses Hasunuma's first interconnect (e.g., "conductive layer 14") extending in a same direction as Hasunuma's second interconnect (e.g., "conductive layer 26"):



TSMC-1003, ¶¶277-79. Hasunuma's interconnects are described as having identical widths matching the width of the vias (TSMC-1005, ¶[0127]; *see also* Fig. 14), such that Figure 8's first and second interconnects must extend across the page in the same lengthwise direction. TSMC-1003, ¶¶280-82. Additionally, both interconnects extend in a same direction into/out of the page of Figure 8. *Id.*, ¶¶278-79.

7. Claim 12

Hasunuma's dummy via (e.g., "reinforcing plug 28") is provided on an extended line along which the first interconnect (e.g., "conductive layer 14") extends (TSMC-1005, Fig. 8; TSMC-1003, ¶¶284-86):

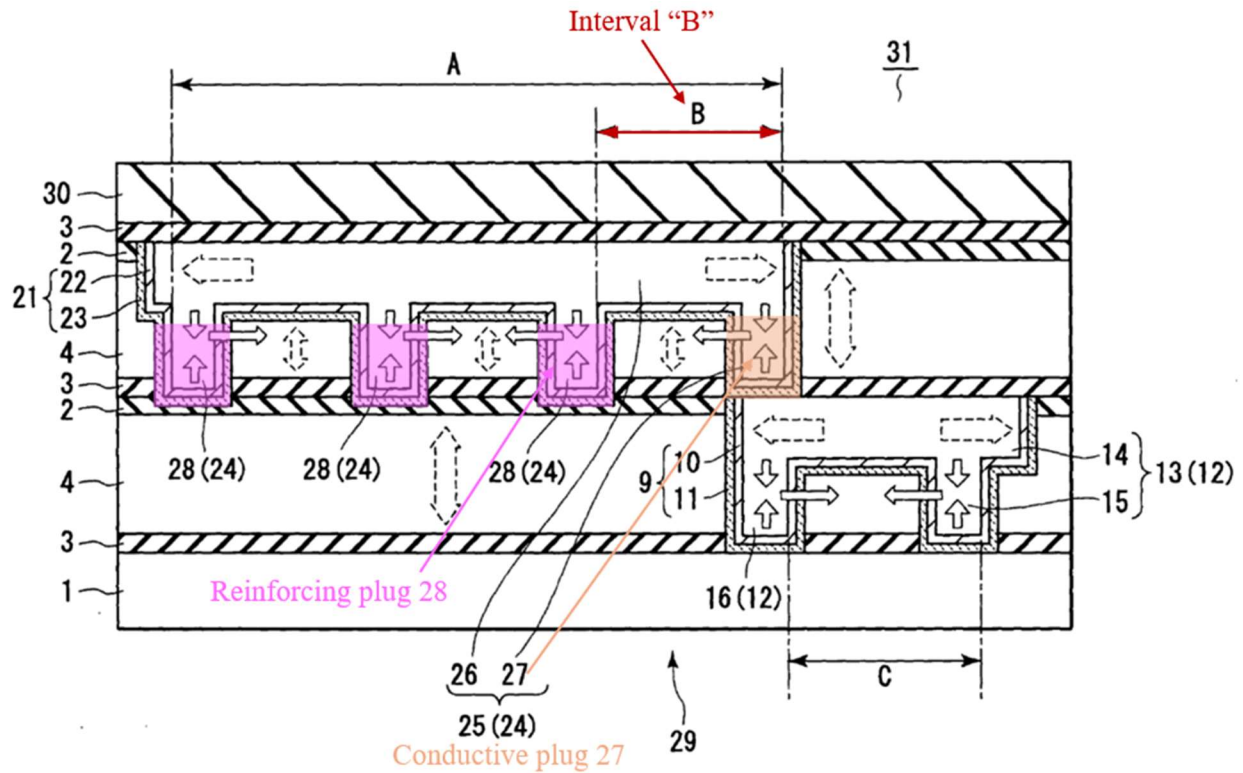


FIG. 9

As seen from Figure 9, interval “B” is effectively equal to the center-to-center spacing between the via and dummy via, which is larger than the edge-to-edge spacing between the via and dummy via (e.g., the spacing between the right edge of reinforcing plug 28 and the adjacent left edge of conductive plug 27). TSMC-1003, ¶289.

Hasunuma teaches that a preferred interval B is about 1 μm or less, and shows such tested values in Tables 1-3. TSMC-1005, ¶[0137], Tables 1-3. Since B represents an even greater distance than the edge-to-edge spacing between the via and dummy via, this teaching for B satisfies the claim limitation of 25 μm or less. TSMC-1003, ¶¶289-90.

9. Claim 14

Hasunuma teaches that a bottom of its dummy vias (e.g., “reinforcing via plug 28”) is deeper than a bottom of its functional vias (e.g., “conductive plug 27”). TSMC-1005, ¶¶[0104], [0109], [0176]-[0178], Figs. 8, 14; TSMC-1003, ¶¶292-95. Figure 8 discloses “reinforcing plug 28” extending into underlying “SiC film 2” while “conductive plug 27” extends only to the upper surface of “conductive layer 14” (TSMC-1005, Fig. 8, ¶¶[0109], [0104]; TSMC-1003, ¶293):

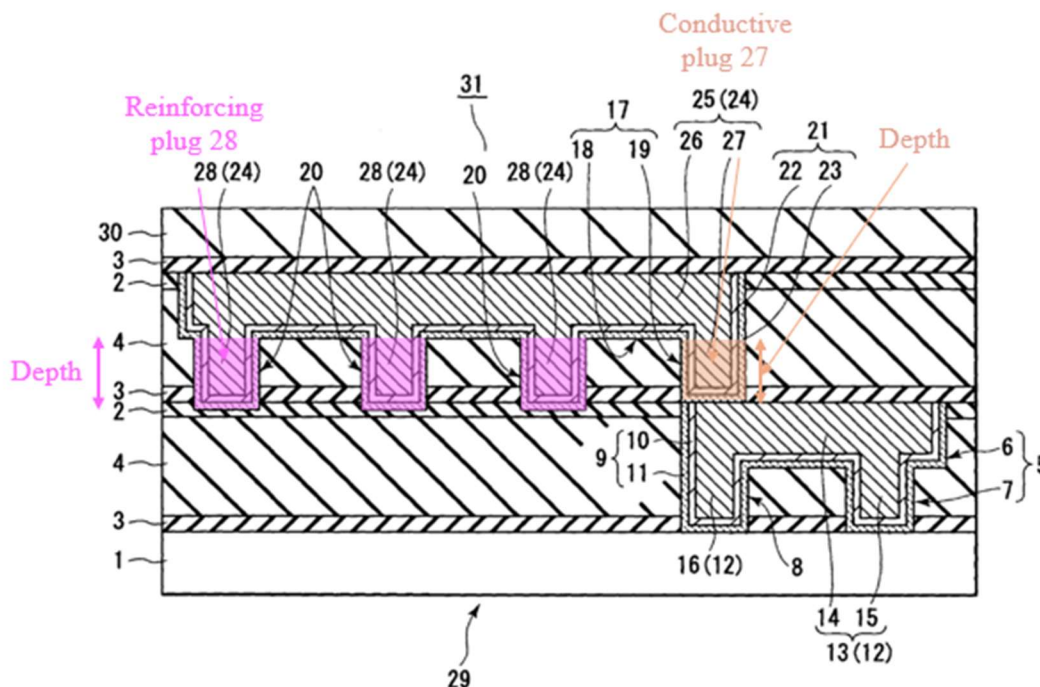


FIG. 8

Additionally, Figure 14 is directed to a further embodiment that includes the same components as the embodiment of Hasunuma’s Figures 1-8 relied on for claim 1. TSMC-1005, ¶[0176]; TSMC-1003, ¶294. As such, the same analysis

described herein for Figures 1-8 (including its mapping to claim 1) applies equally to Figure 14 throughout this Petition. Figure 14 discloses “reinforcing plugs 28” extending into underlying “low dielectric constant film (interlayer insulating film) 4” while “conductive plug 27” extends to the upper surface of “conductive layer 14” (TSMC-1005, Fig. 14; TSMC-1003, ¶294):

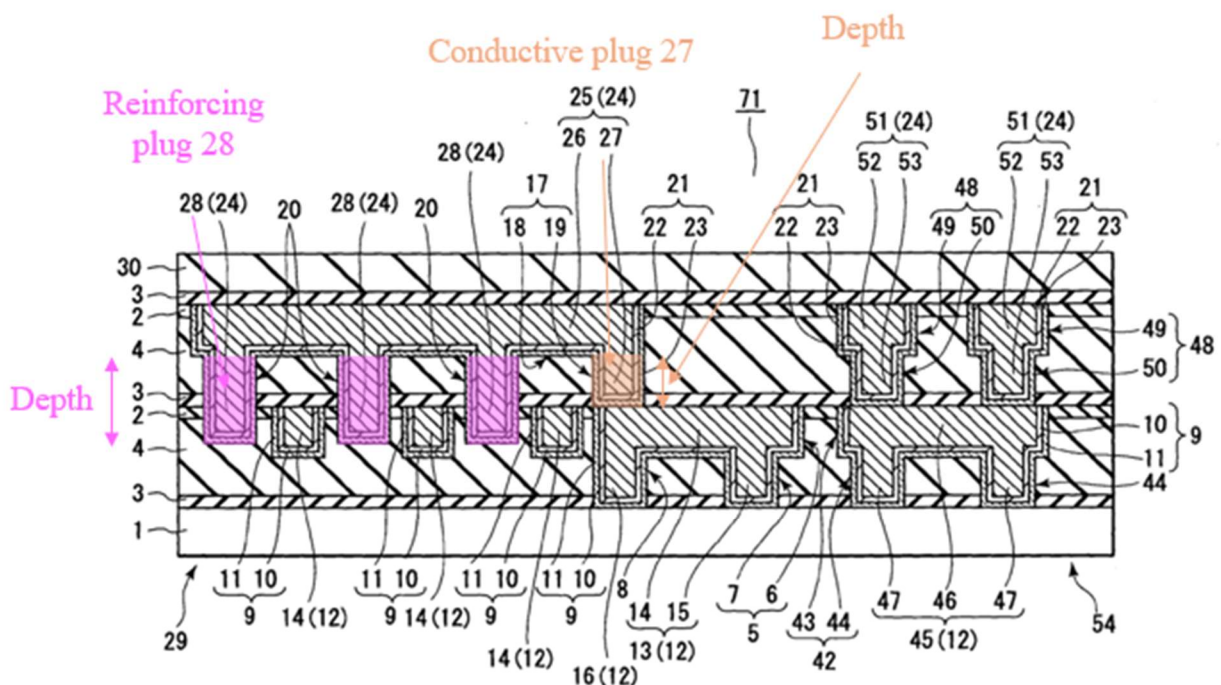


FIG. 14

Thus, Hasunuma satisfies claim 14 based on each of the Figure 8 and Figure 14 embodiments.

10. Claim 18

Hasunuma’s dummy via (e.g., “reinforcing plug 28”) and second interconnect (e.g., “conductive layer 26”) are both made from the same conductive

film (e.g., “Cu film 24” and/or “barrier metal film 21”) (TSMC-1005, ¶¶[0105]-[0108], Fig. 8; TSMC-1003, ¶¶296-99):

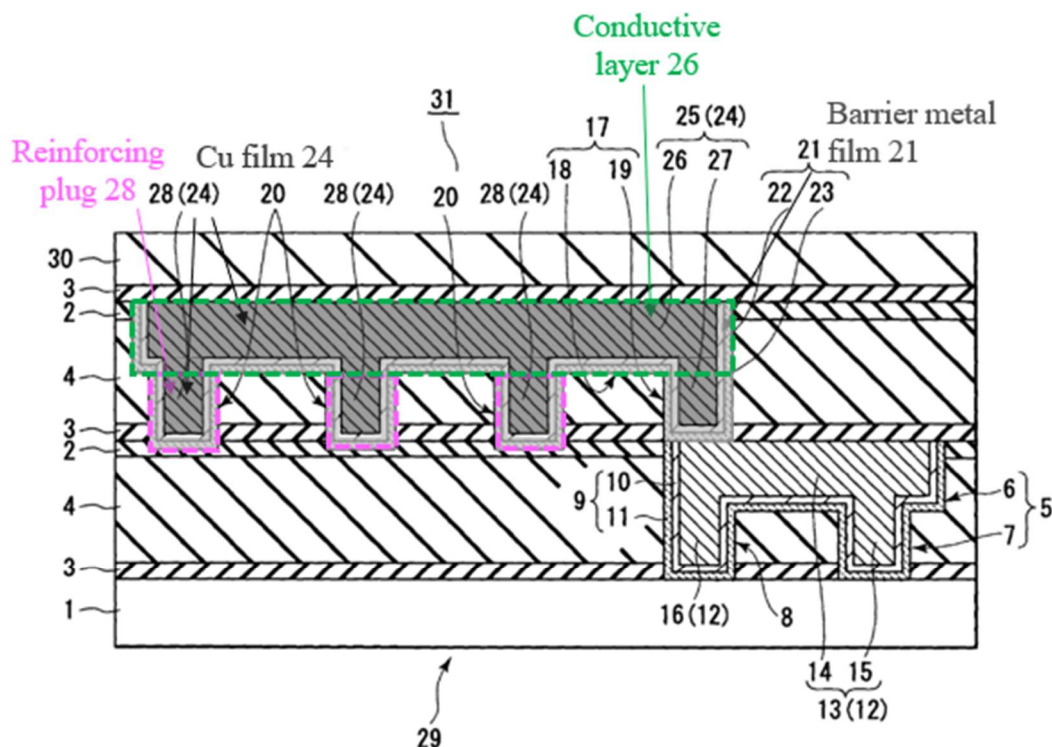


FIG. 8

Indeed, Hasunuma’s dual damascene process simultaneously forms the dummy via (reinforcing plug 28) and the second interconnect (conductive layer 26) by filling integrally formed recesses (recess 20, recess 18) first with the same barrier metal film 21 and then with the same bulk Cu film 24. *See* TSMC-1005, Figs. 4-7, ¶¶[0105]-[0108]; TSMC-1003, ¶298.

11. Claim 19

Hasunuma discloses dummy vias (e.g., “reinforcing plugs 28”) with a first end and second end, the first end connected to the second interconnect (e.g.,

“conductive layer 26”) and the second end surrounded by a second insulating film (e.g., “low relative dielectric constant film 4” and/or lower layer “film 2”). TSMC-1005, ¶¶[0103]-[0104], [0109], [0177]-[0178], Figs. 4, 8, 14; TSMC-1003, ¶¶300-05. Figure 8 discloses the second (bottom) end of dummy/reinforcing plug 28 surrounded by insulating film 2 (alone or as part of the combination of insulating films 2,3,4) (TSMC-1005, ¶[0104] (explaining that, due to over-etching, “bottom portions of the recesses 20 extend below the surface of the SiC film 2 of the first layer”); TSMC-1003, ¶¶303-04):

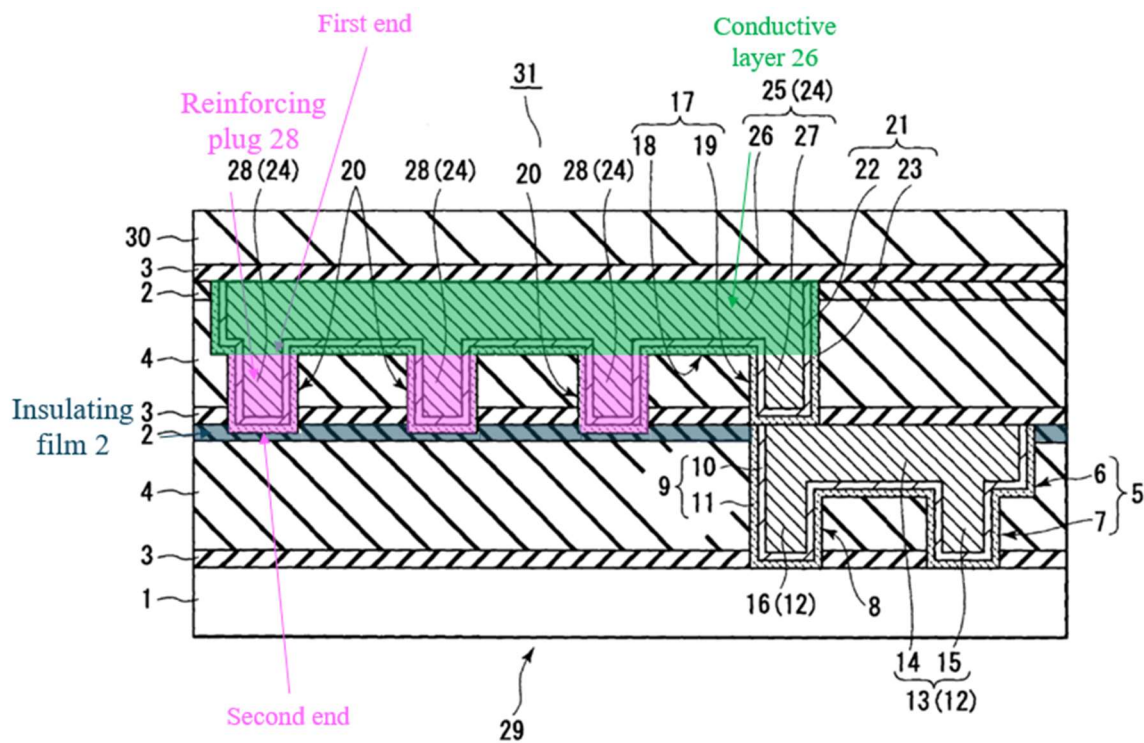


FIG. 8

Additionally, Figure 14 (directed to an embodiment having the same relevant components as Hasunuma’s Figures 1-8 embodiment) (see TSMC-1005, ¶[0176];

supra, §VI(E)(9)) discloses “the lower end of each Cu reinforcing via plug 28 projects into the low relative dielectric constant film (interlayer insulating film) 4 of the first layer,” (TSMC-1005, ¶[0177]), such that the second ends of reinforcing plugs 28 are surrounded by insulating film 4:

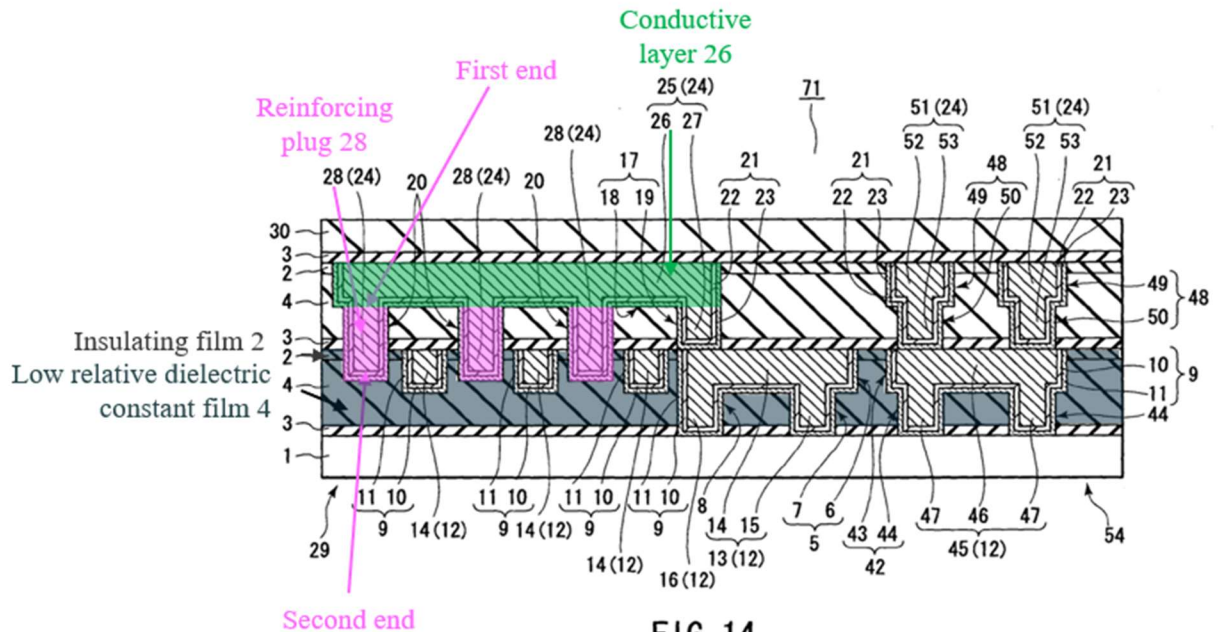


FIG. 14

TSMC-1003, ¶¶303, 305.

F. **GROUND 6: Hasunuma combined with Kurashima renders Claims 2 and 20 obvious**

Claims 2 and 20 are obvious over Hasunuma and Kurashima. TSMC-1003, ¶¶306-23.

1. **Kurashima**

Because Kurashima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 patent purports to address (e.g.,

interconnect reliability), Kurashima is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1011, 1:15-22, 1:49-67; TSMC-1003, ¶¶87-88.

Kurashima discloses a semiconductor device and manufacturing method aimed at enhancing the durability of insulating films, particularly low-relative-dielectric-constant films, against Chemical Mechanical Polishing (CMP) stress to prevent film peeling. TSMC-1011, 1:15-22, 1:49-67. As illustrated in its first embodiment (Figs. 1B-1D), Kurashima teaches forming an effective Cu-wire 9 in a first layer and, in parallel, Cu-dummy wire 10 in a spaced-apart area within the same first layer's interlayer insulating film 4. *Id.*, 4:50-6:32, Figs. 1B-1D. Subsequently, a second-layer effective Cu-wire 16 is formed connecting to first-layer Cu-wire 9. *Id.*, 6:58-8:35, Figs. 2A-3A. Concurrently, a second-layer Cu-dummy wire 17 is formed in contact with first-layer Cu-dummy wire 10, thereby providing a reinforcing effect and enhancing interfacial adhesion and CMP durability, and reducing peeling of layers during CMP. *Id.*, 6:58-8:54, 9:16-23.

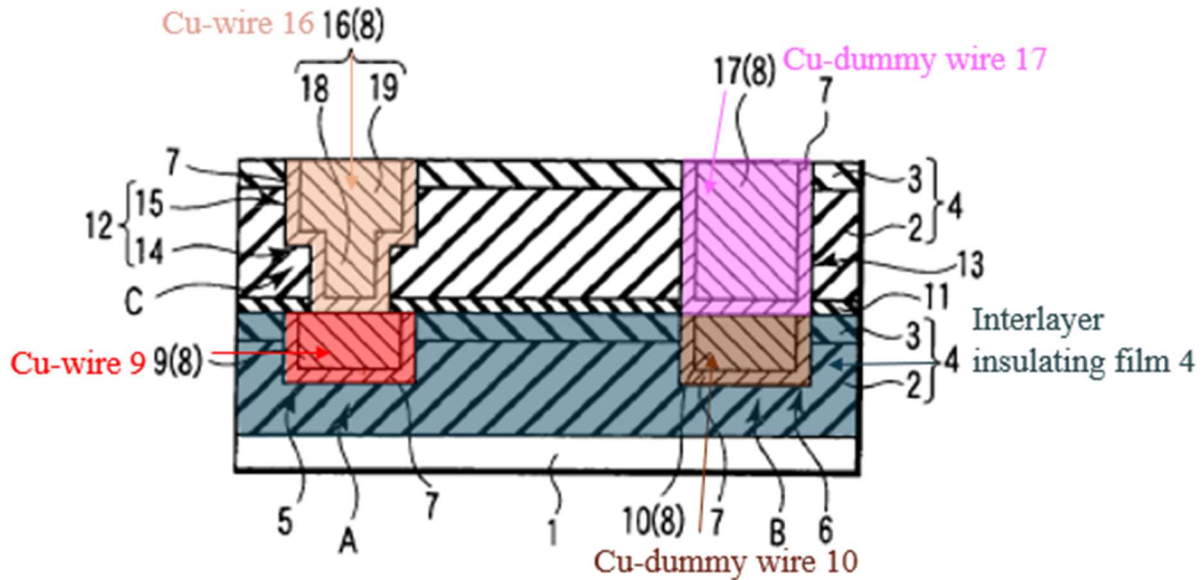


FIG. 3A

2. Claim 2

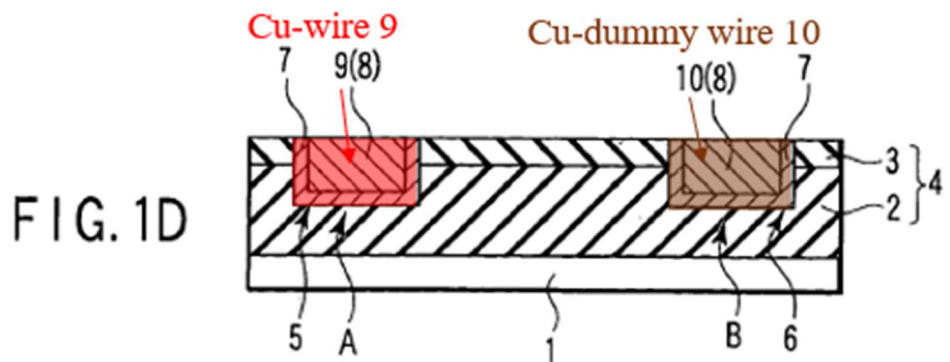
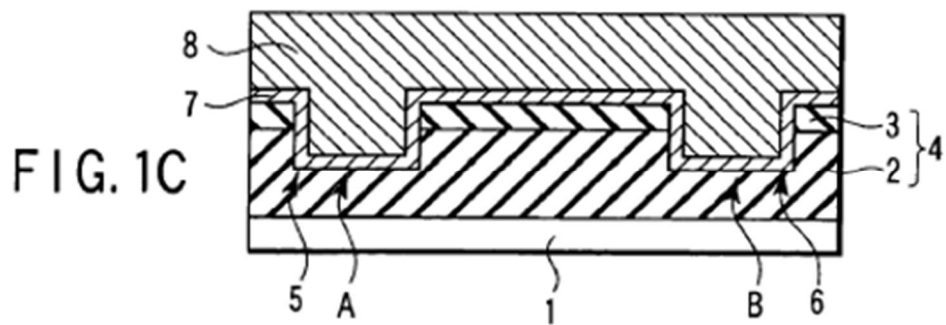
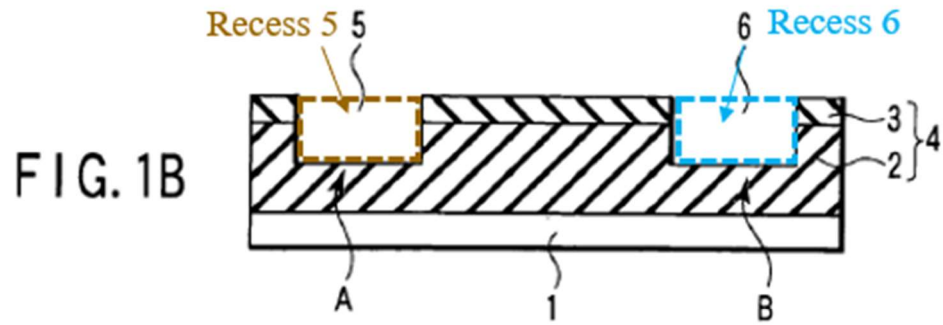
a) [2a]

Kurashima discloses simultaneously forming both a first interconnect (e.g., “Cu-wire 9” and “TaN-film 7,” hereafter collectively “Cu-wire 9”) and a first dummy interconnect (e.g., “Cu-dummy wire 10” and “TaN-film 7,” hereafter collectively “Cu-dummy wire 10”) on a semiconductor substrate (e.g., “semiconductor substrate 1”). TSMC-1011, 4:12-21, 4:50-6:57, Figs. 1B-1D; TSMC-1003, ¶¶307-09.

Kurashima discloses a “manufacturing method of [a] semiconductor device” in which a first dummy interconnect (“Cu-dummy wire 10”) is connected to a dummy via (“Cu-dummy wire 17”). TSMC-1011, 4:7-21, Fig. 3A. “Cu-dummy wire 10” is a dummy interconnect both because of its description as a “dummy”

structure and its purpose, which is consistent with the '751 patent's description of a "dummy interconnect." TSMC-1003, ¶308; *see supra*, §VI(A)(2)(d). Specifically, Cu-dummy wire 10 does not constitute part of a closed circuit in actual use of the device, i.e., no current flows therein during use. TSMC-1011, 4:58-61. Rather, Kurashima uses Cu-dummy wire 10 (and its direct connection to a dummy via, i.e., "Cu-dummy wire 17") to reduce film peels. *Id.*, 5:63-6:32, 9:16-23. Additionally, Kurashima's device would still be operable if Cu-dummy wire 10 was omitted, because it serves no part in routing current flow. TSMC-1003, ¶308.

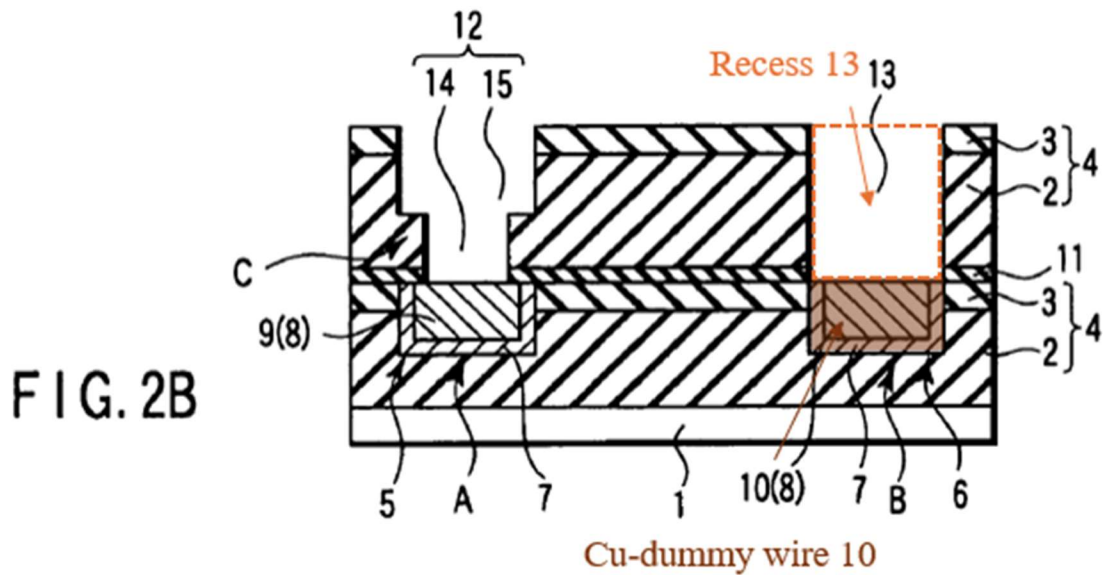
Additionally, as shown in Figures 1B-1D, Kurashima discloses forming recess 5 for an interconnect ("Cu-wire 9") and recess 6 for the dummy interconnect ("Cu-dummy wire 10") simultaneously, and forming Cu-wire 9 and Cu-dummy wire 10 simultaneously (TSMC-1011, 4:50-61):



TSMC-1003, ¶309.

b) [2b]

As shown in Figure 2B, Kurashima's dummy hole (e.g., "recess [for dummy wire] 13") is connected to the dummy interconnect (e.g., "Cu-dummy wire 10") (TSMC-1011, 7:11-8:13, Figs. 2B-3A; TSMC-1003, ¶310):

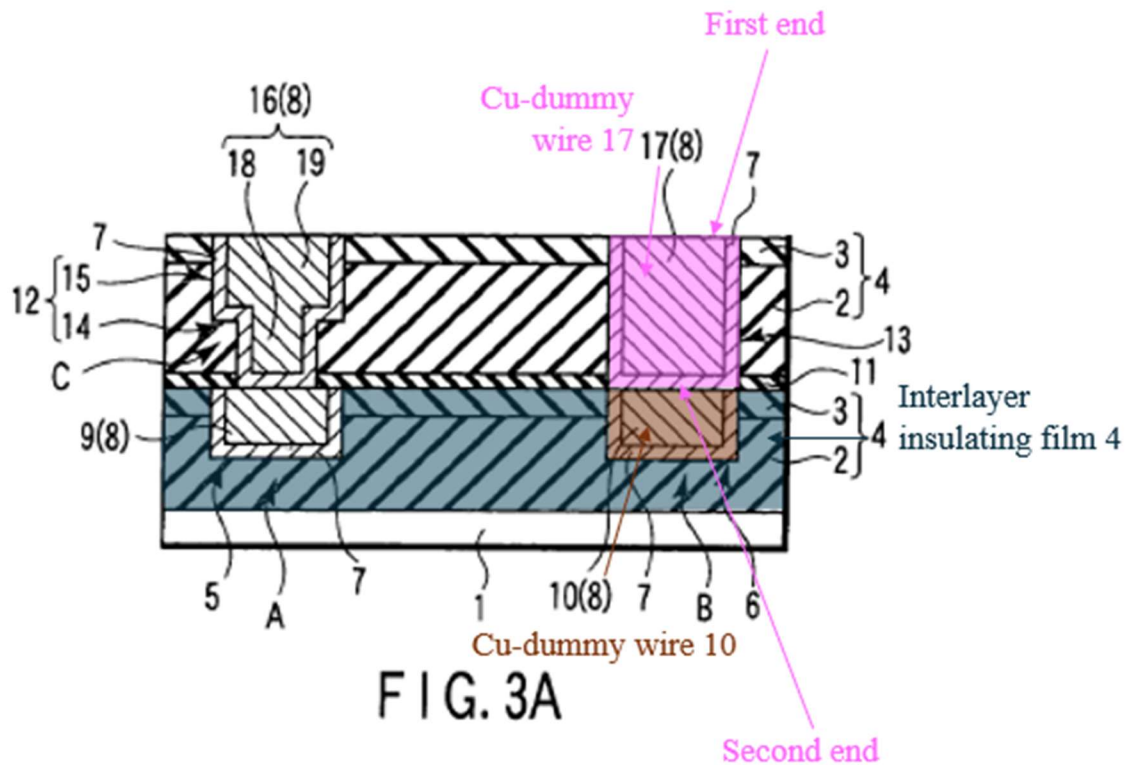


Accordingly, when incorporating a dummy interconnect (similar to Kurashima’s “Cu-dummy wire 10”) into Hasunuma’s device, the dummy interconnect would be formed at the same time as first interconnect 14, and the dummy hole (“recess 20”) formed in Hasunuma’s insulating film (e.g., “low relative dielectric constant film 4”) would be connected to the dummy interconnect so that the dummy via (e.g., Hasunuma’s “reinforcing plug 28”/Kurashima’s “Cu-dummy wire 17”) formed therein would be connected to the dummy interconnect (as in Kurashima) (TSMC-1003, ¶311):

A POSITA would have expected success when incorporating a dummy plug-dummy interconnect structure into Hasunuma's device. TSMC-1003, ¶316. A POSITA understood that the dummy interconnect connected to the dummy plug could be reliably positioned beneath Hasunuma's dummy vias/reinforcing plug(s) 28. *Id.* Creation of the dummy interconnect and connection of reinforcing plug 28 thereto could have been easily accomplished using the same processing steps already utilized in Hasunuma to create its first interconnect layer ("conductive layer 14") and connect "conductive plug 27" thereto. *Id.*

3. Claim 20

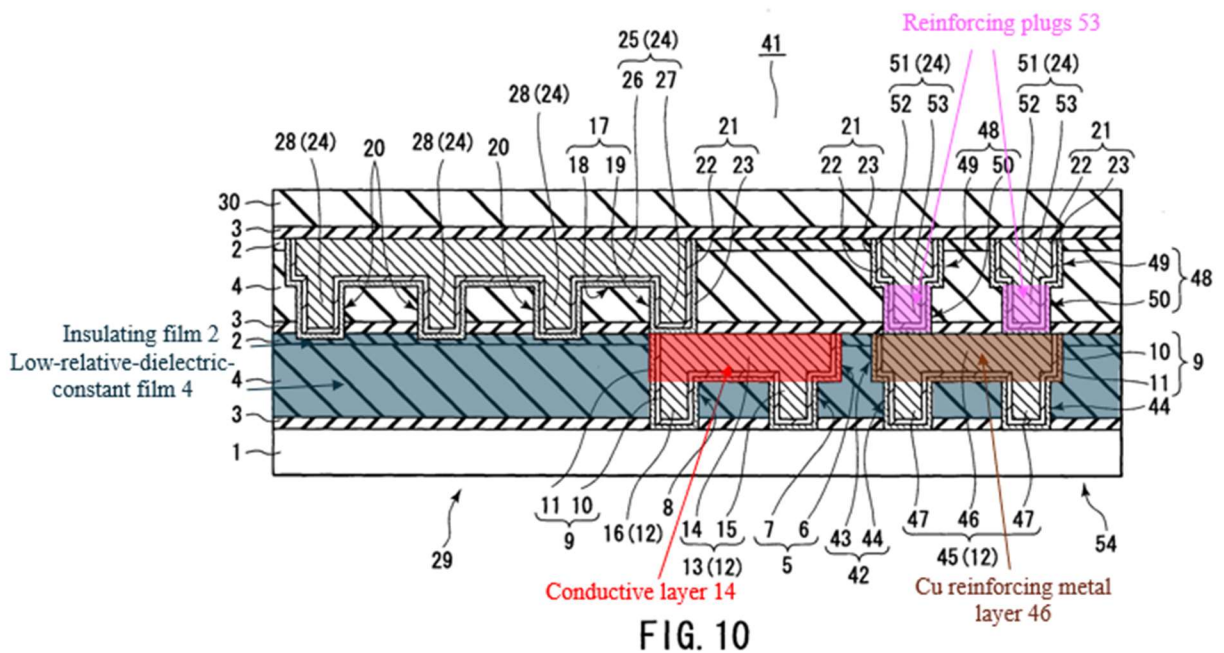
Kurashima discloses that the dummy via (e.g., "Cu-dummy wire 17" and "TaN-film 7," hereafter collectively "Cu-dummy wire 17") includes a first and second end, the second end connected to a dummy interconnect (e.g., "Cu-dummy wire 10"), the dummy interconnect being surrounded by a second insulating film (e.g., "interlayer insulating film 4"). TSMC-1011, 4:50-6:14, Figs. 1B-1D, 3A, 4A; TSMC-1003, ¶317.



In Figure 7, Hasunuma similarly discloses an interconnect (“conductive layer 14”) formed in a layer including “low relative dielectric constant film 4” (and “film 2”) and a dummy via (“reinforcing plug 28”) having a second end that terminates just above this layer and has a first end connected to a second interconnect (“conductive layer 26”) (TSMC-1005, ¶¶[0101]-[0110], Figs. 7, 1A-3A; TSMC-1003, ¶318):

surrounded by a second insulating film (e.g., “film 4” and/or “film 2”). TSMC-1003, ¶¶320.

A POSITA was motivated to create such a structure in this manner and would have expected success for the same reasons as discussed for claim 2. *Supra*, §VI(F)(2)(c). Following Kurashima, the dummy interconnect could be easily formed in Hasunuma’s film 4 (and/or film 2) in parallel with conductive layer 14. TSMC-1003, ¶¶321-23. Indeed, as shown in Figure 10, Hasunuma already teaches connecting separate dummy vias (e.g., “reinforcing plugs 53”) to underlying dummy interconnects (e.g., “Cu reinforcing metal layer 46”) that are formed in the same level and in the same film 4/film 2 as conductive layer 14:



Id.

G. GROUND 7: Hasunuma combined with Watanabe renders Claims 2, 8, and 10 unpatentable

Claims 2, 8, and 10 are obvious over Hasunuma and Watanabe. TSMC-1003, ¶¶324-46.

1. Claim 2

a) 2[a]/2[b]

Watanabe's second and fifth embodiments disclose elements 2[a] and 2[b]. *Supra*, §VI(A)(3).

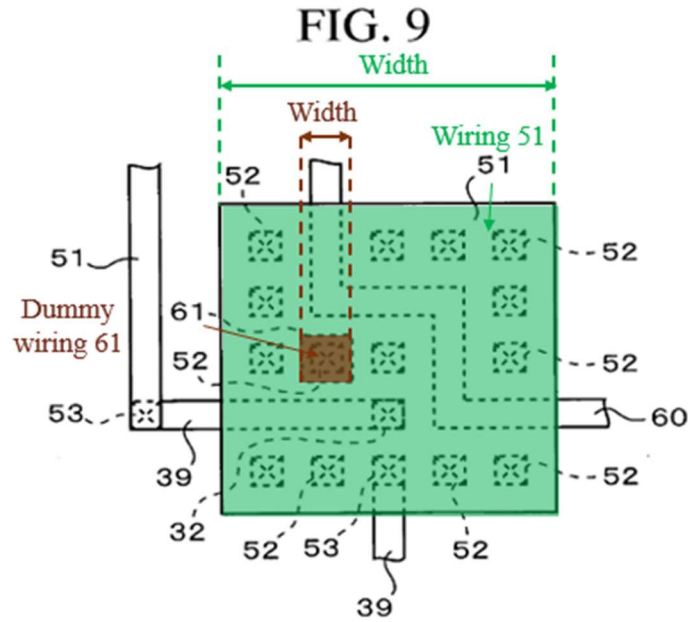
b) Combining Hasunuma and Watanabe

It was obvious in view of Watanabe to incorporate a dummy interconnect into Hasunuma's device for the same reasons discussed above for combining Hasunuma and Kurashima. *Supra*, §VI(F)(2); TSMC-1003, ¶¶326-28. Indeed, Watanabe expressly discusses the known benefit of enhanced mechanical strength afforded by incorporating a dummy interconnect into a semiconductor device, which would have been achieved when incorporating such a dummy interconnect into Hasunuma's device. *See* TSMC-1004, ¶¶[0091], [0127]; TSMC-1003, ¶327; *see also* TSMC-1011, 5:63-6:32, 8:14-34, Figs. 5A-5B. Additionally, a POSITA was further motivated to incorporate such a dummy plug-dummy interconnect structure to establish additional structural support for the polishing step, thereby reducing dishing of the copper wiring layers. TSMC-1003, ¶327; *see* TSMC-1007, 4:12-44; TSMC-1024, 2:55-58.

Additionally, for the same reasons discussed above, a POSITA would have expected success when incorporating a dummy plug-dummy interconnect structure into Hasunuma's device. TSMC-1003, ¶328. A POSITA understood that a dummy interconnect such as that in Watanabe could be reliably positioned beneath and connected to Hasunuma's dummy via/reinforcing plug 28. *Id.* Indeed, Hasunuma already teaches connecting dummy plugs to dummy interconnects. *Id.*; *see supra*, §VI(F)(3); TSMC-1005, Fig. 10.

2. Claim 8

The combination of Hasunuma and Watanabe teaches a first dummy interconnect and a second interconnect. *Supra*, §§VI(G)(1), VI(E)(2)(e), VI(A)(3). Watanabe further teaches a dummy interconnect (e.g., “dummy wiring 61”) with a smaller width than an upper level (second) interconnect (e.g., “wiring 51”) (TSMC-1004, Fig. 9, ¶¶[0125], [0105]; TSMC-1003, ¶¶329-31):



It was obvious to simply substitute such relative widths in Hasunuma's modified structure outlined above for claim 2. TSMC-1003, ¶¶331-36. Indeed, the '751 patent teaches no criticality associated with these relative widths. *Id.*, ¶332.

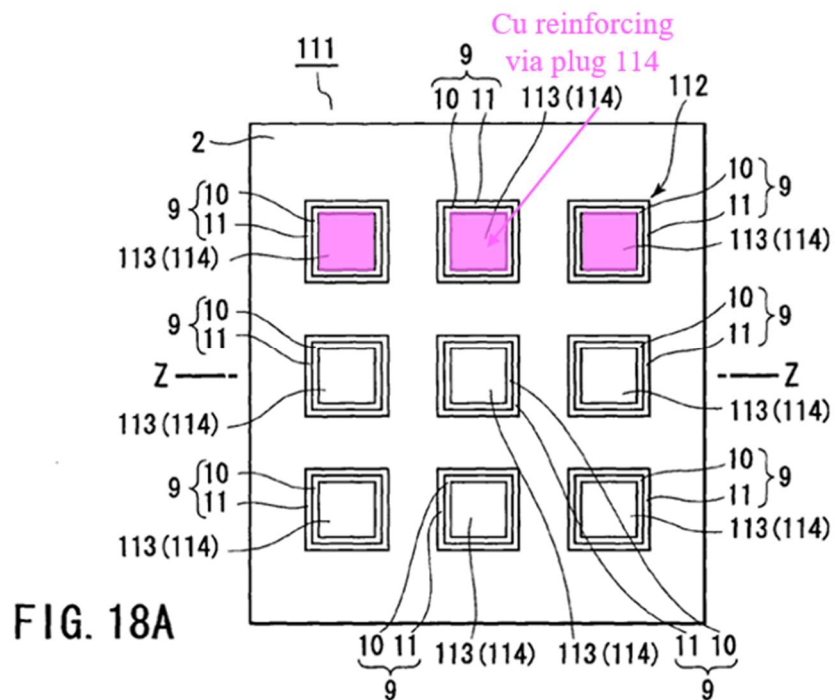
A POSITA was motivated to use such relative widths to provide more space on the second interconnect for via connections and thus connections to other circuit elements, see, e.g., Watanabe's Figure 9. *Id.*, ¶333. A POSITA was further so motivated because smaller-width dimensions are generally required lower in the interconnect structure to achieve a greater concentration/density of wiring. *Id.*, ¶¶334-35; TSMC-1034, 585-86, 591, Figs. 12-17, 12-18. Dummy interconnects and active wires at lower levels should maintain the same general dimensions to maintain pitch requirements and allow for efficient routing and wiring density. TSMC-1003, ¶¶334-35. In contrast, higher level interconnects typically carry more

current and need better heat dissipation, requiring relatively wider interconnect widths higher in the structure. *Id.*; TSMC-1012, 34; TSMC-1034, 594. Accordingly, it was a simple design choice—encouraged by existing design parameters for widths of lower-level interconnects versus upper-level interconnects—to form the dummy interconnect with a smaller width than the second interconnect. TSMC-1003, ¶¶331-35.

A POSITA would have expected success given that this modification merely requires changing the relative sizes of the dummy and second interconnects, which was easily achievable using standard processing techniques, including Hasunuma's. *Id.*, ¶336; *see also* TSMC-1016, 6:14-29.

3. Claim 10

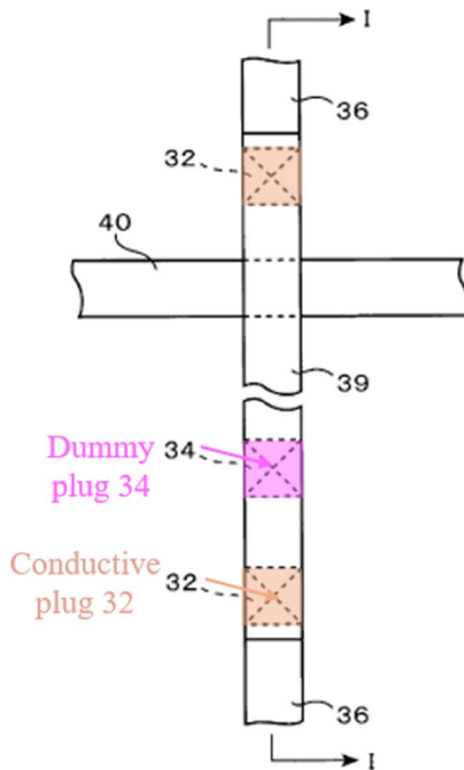
Hasunuma discloses dummy vias (e.g., “Cu reinforcing via plug 114”) in planar shapes that are square (see, e.g., Figure 18A):



Thus, Hasunuma discloses substantially square-shaped vias as a known design option for the vias and dummy via in any of its embodiments. TSMC-1003, ¶¶337-39.

Additionally, Watanabe discloses square-shaped vias and dummy vias (*supra*, §VI(A)(8), see, e.g., Fig. 2):

FIG. 2



It was obvious in view of Hasunuma's and Watanabe's disclosures of square vias and the knowledge of a POSITA at the time to make the planar shape of both vias and dummy vias in Hasunuma's various embodiments substantially square. Prior to the '751 patent, both vias and dummy vias were commonly designed and fabricated with square cross-sections. TSMC-1003, ¶¶165, 340; TSMC-1008, 9:45-47 ("the via-hole may have any configuration, such as a square, rectangle or circle."), 10:8-11; TSMC-1013, 9:45-49.

Thus, substantially square vias were an obvious design option that could have been easily implemented with a reasonable expectation of success. TSMC,

1003, ¶¶341-45; *supra*, §§VI(A)(8), VI(D)(2). Additionally, square-shaped vias provided the added advantage of increased contact area with interconnects above and below the vias. TSMC-1003, ¶343; TSMC-1039, 5:27-32. Accordingly, it was obvious in view of Hasunuma's and Watanabe's disclosures of square vias and the state of the art to make both the vias and dummy vias in Hasunuma substantially square in a planar shape.

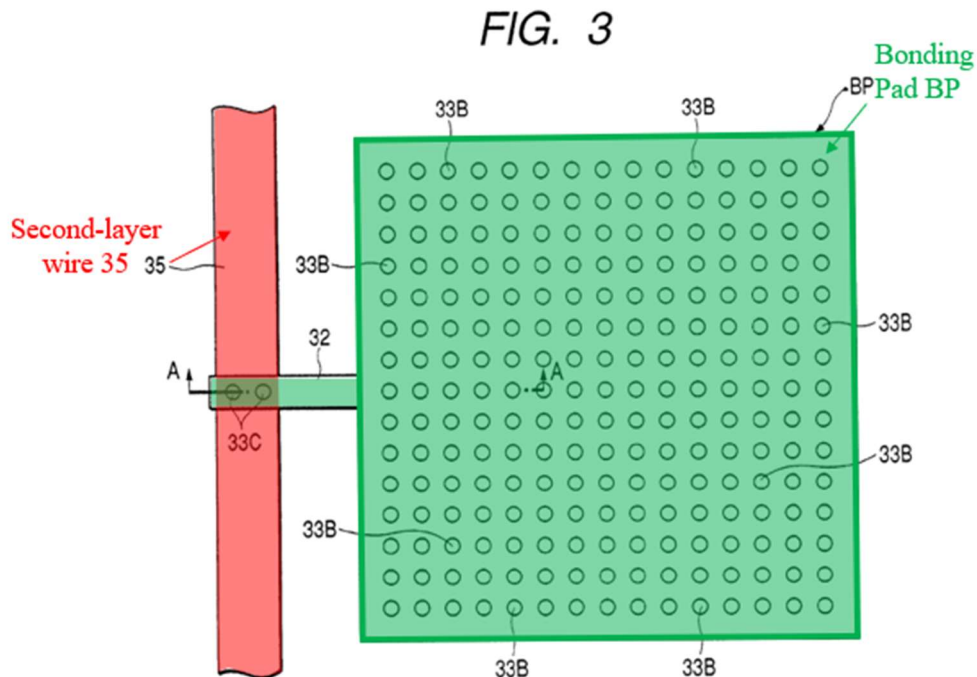
H. GROUND 8: Aoyagi renders obvious Claims 1, 3-4, 7, 14-16, and 19

1. Aoyagi

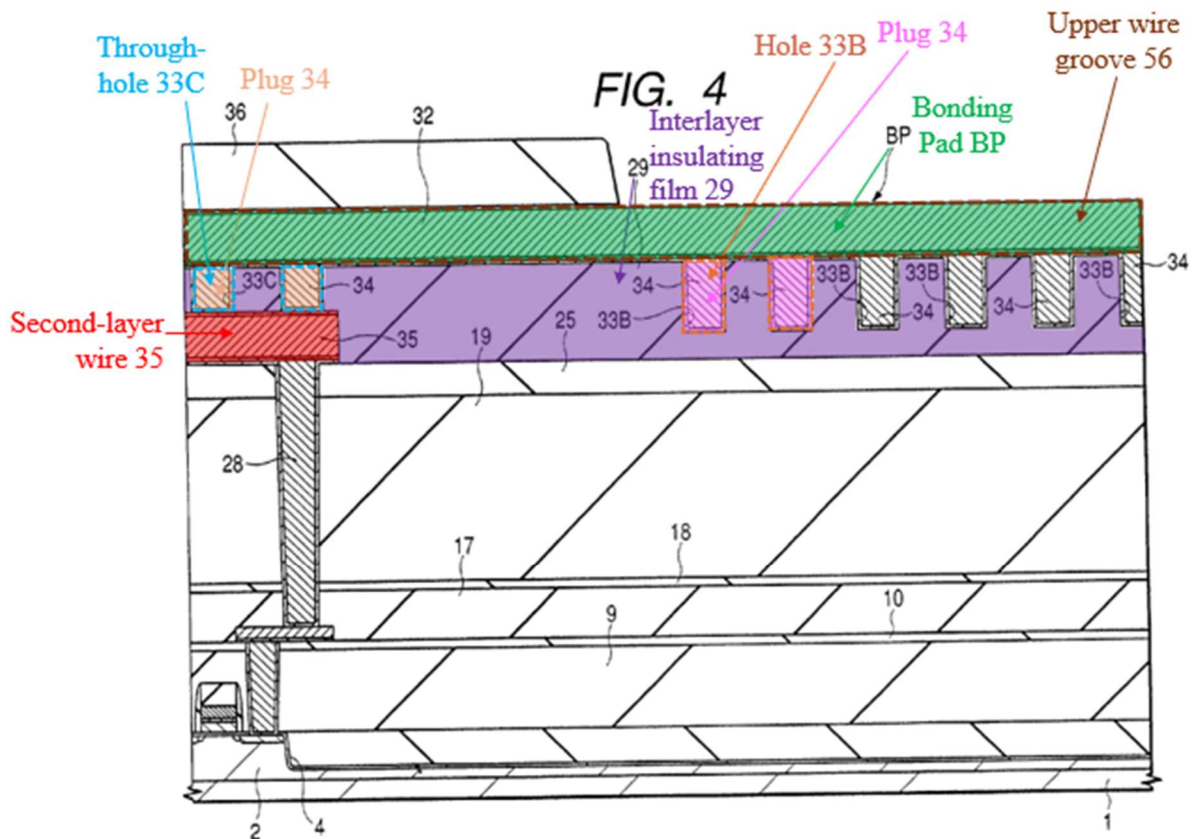
Because Aoyagi is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 patent purports to address (e.g., interconnect reliability), Aoyagi is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1006, Abstract, ¶¶[0001], [0004]-[0005]; TSMC-1003, ¶¶75-80.

Aoyagi discloses in Figures 2-12 and 19, and their supporting description, a method of fabricating a semiconductor device and the resulting device. The method includes: (i) forming second-layer wire 35 on substrate 1, (ii) forming insulating film 29 on second-layer wire 35, (iii) forming via holes 33A, 33C, dummy via holes 33B, and upper wire groove 56 in insulating film 29, and (iv) depositing conductive material into holes 33A, 33B, 33C and groove 56, thereby forming vias 34 (in holes

33A, 33C), dummy vias 34 (in holes 33B), and third-layer wire 31/bonding pad BP⁹ in upper wire groove 56. TSMC-1006, ¶¶[0050]-[0055], [0077], [0079]. Aoyagi's dummy vias 34 (in holes 33B) are for promoting adhesion between bonding pad BP and insulating film 29, not for operational current flow to underlying layers. *Id.*, ¶¶[0050]-[0056], [0079].

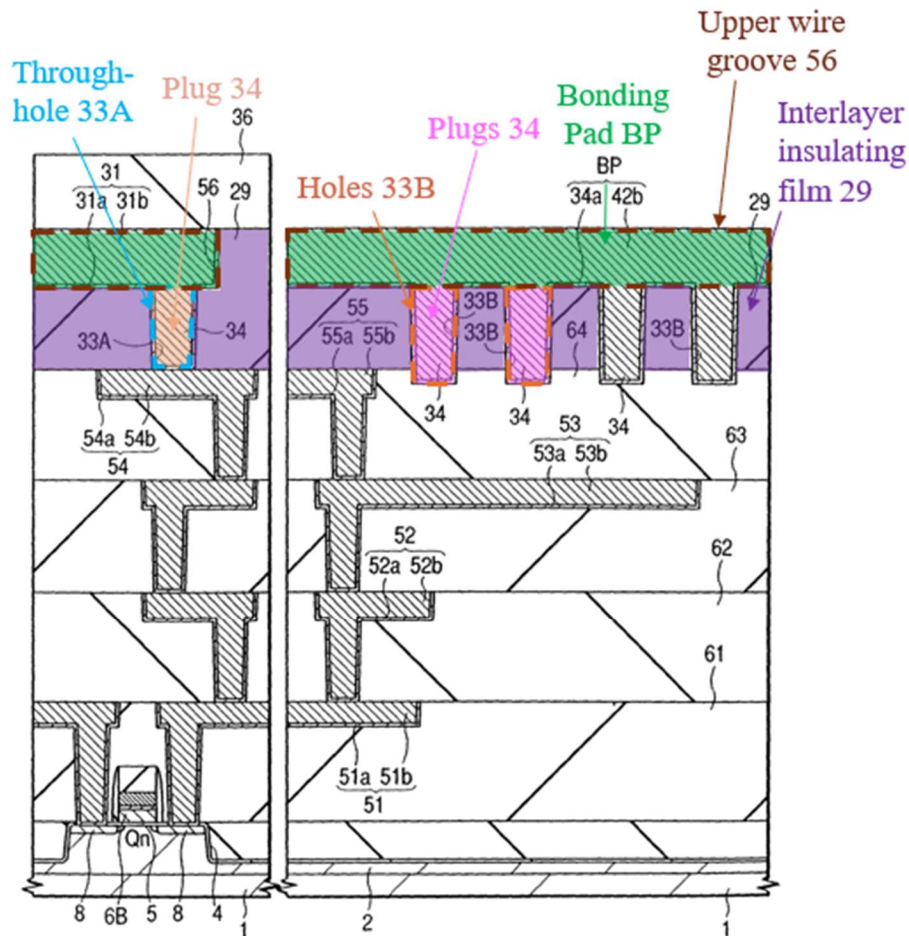


⁹ As demonstrated by Figures 3-4, “bonding pad BP” and “lead wire 32” together form a single, integral component, and as such discussion of “bonding pad BP” herein is intended to include “lead wire 32” unless specified otherwise. *See* TSMC-1006, Figs. 3-4.



Aoyagi's Figure 19 teaches using a dual damascene process for interconnect/via fabrication, noting that "upper wire 31 (*including the bonding pad BP*)" may be formed by depositing conductive material into holes 33A, 33B and wire groove 56. *Id.*, ¶[0077], Fig. 19. This dual damascene process applies equally to forming the interconnects (e.g., second-layer wire 35 and third-layer wire 31 that includes bonding pad BP) and the functional and dummy vias (e.g., plugs 34 in holes 33C, 33B) of Figures 3-4. TSMC-1003, ¶78.

FIG. 19



Additionally, given Aoyagi's discussion of using a dual damascene process to form wire 31/bonding pad BP and deposit conductive material in holes 33A and 33B and upper wire groove 56, it was obvious to use a dual damascene process to form bonding pad BP/lead wire 32 and the vias formed in through-holes 33C in the structure of Figures 3-4. *Id.*, ¶79. A POSITA was motivated to use a dual damascene process to simplify manufacturing, increase efficiency, reduce costs, and increase reliability, and could have easily implemented such a process given its

widespread use (including in Aoyagi). *Id.*; *supra*, §VI(A)(1); TSMC-1034, 583-84, 671-76, 718, 723-26.

Accordingly, Aoyagi renders claims 1, 3-4, 7, 14-16, and 19 obvious. TSMC-1003, ¶¶347-90.

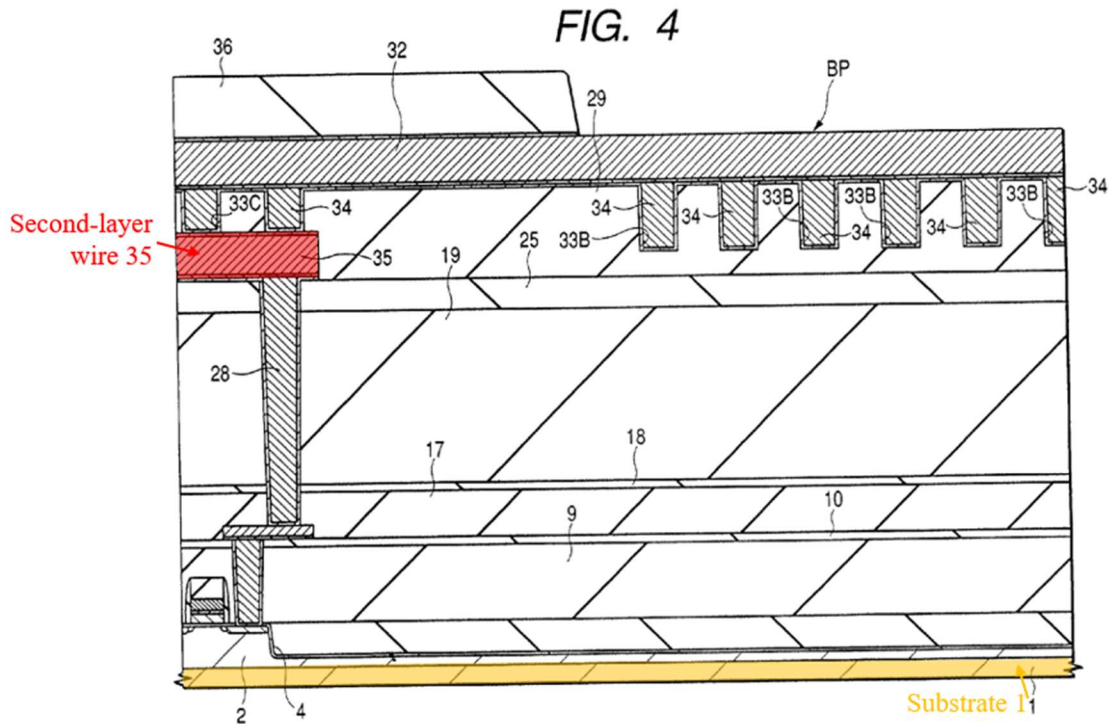
2. Claim 1

a) 1[pre]

Aoyagi is directed to a “technique of manufacturing” “a semiconductor [] device,” satisfying claim 1’s preamble. TSMC-1006, ¶¶[0001], [0012]-[0017], Figs. 4-12, 19; TSMC-1003, ¶348.

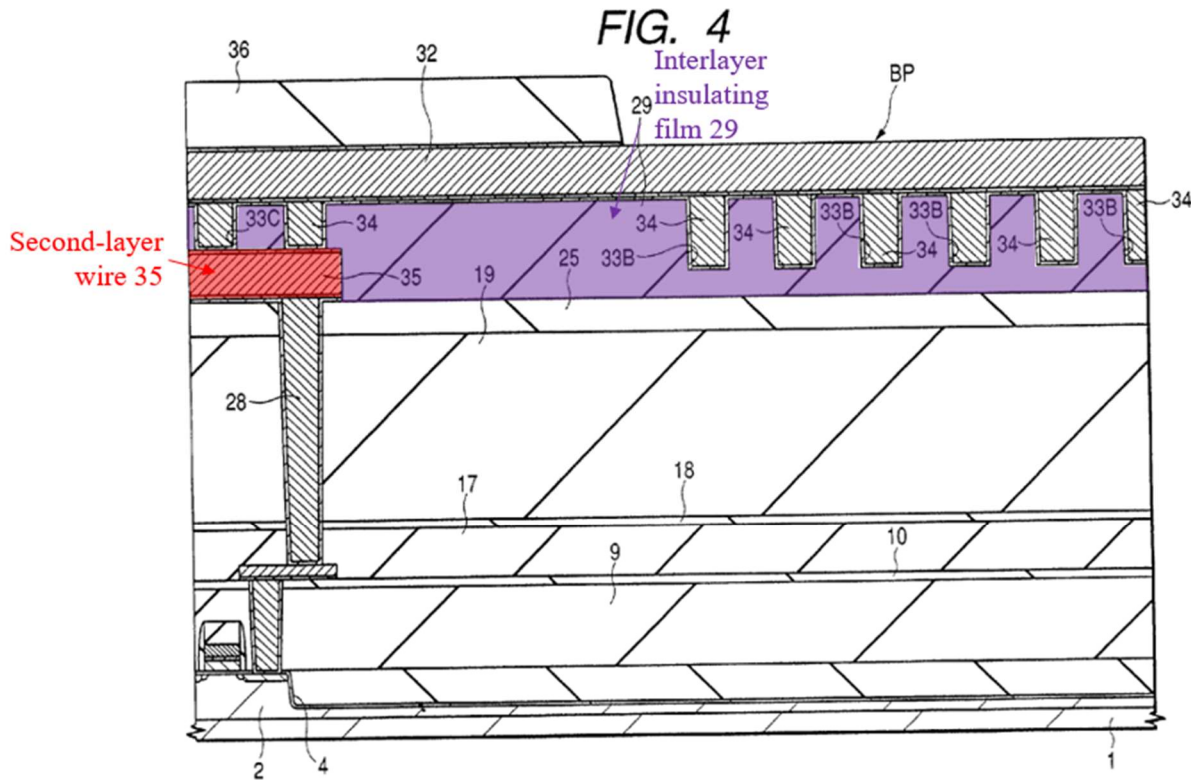
b) 1[a]

Aoyagi discloses forming a first interconnect (e.g., “second-layer wire 35”) on a semiconductor substate (e.g., “substrate 1”) (TSMC-1006, ¶¶[0055], [0040], [0043], [0061], Figs. 4, 7-8; TSMC-1003, ¶¶349-51):



c) 1[b]

Aoyagi discloses forming a first insulating film (e.g., “interlayer insulating film 29”) on the first interconnect (e.g., “second-layer wire 35”). TSMC-1006, ¶¶[0049], [0062], Fig. 4; TSMC-1003, ¶¶352-53. Aoyagi’s “insulating film (first interlayer insulating film) 29...is formed over the **second-layer wires** 26, 27.” TSMC-1006, ¶[0049]. Understood together with Fig. 2, that includes second-layer wire 35, shown in Figure 4:



Thus, given the common layers in Aoyagi's figures and common reference "second-layer wire" for wires 26, 27, 35, "insulating film 29" is formed on "second-layer wire 35" just like "second-layer wires 26, 27." TSMC-1003, ¶353.

d) 1[c]

Aoyagi teaches forming in the first insulating film (e.g., "insulating film 29"), a via hole (e.g., "through-hole 33C") connected to the first interconnect (e.g., "second-layer wire 35"), a dummy hole (e.g., "hole 33B") arranged so as to be incapable of having current flow therethrough, and an interconnect trench (e.g., "upper wire groove 56") connected to the via hole and the dummy hole. TSMC-1006, ¶¶[0077], [0055]-[0056], Figs. 4, 19; TSMC-1003, ¶¶354-63.

Regarding formation of via and dummy holes, Aoyagi discloses

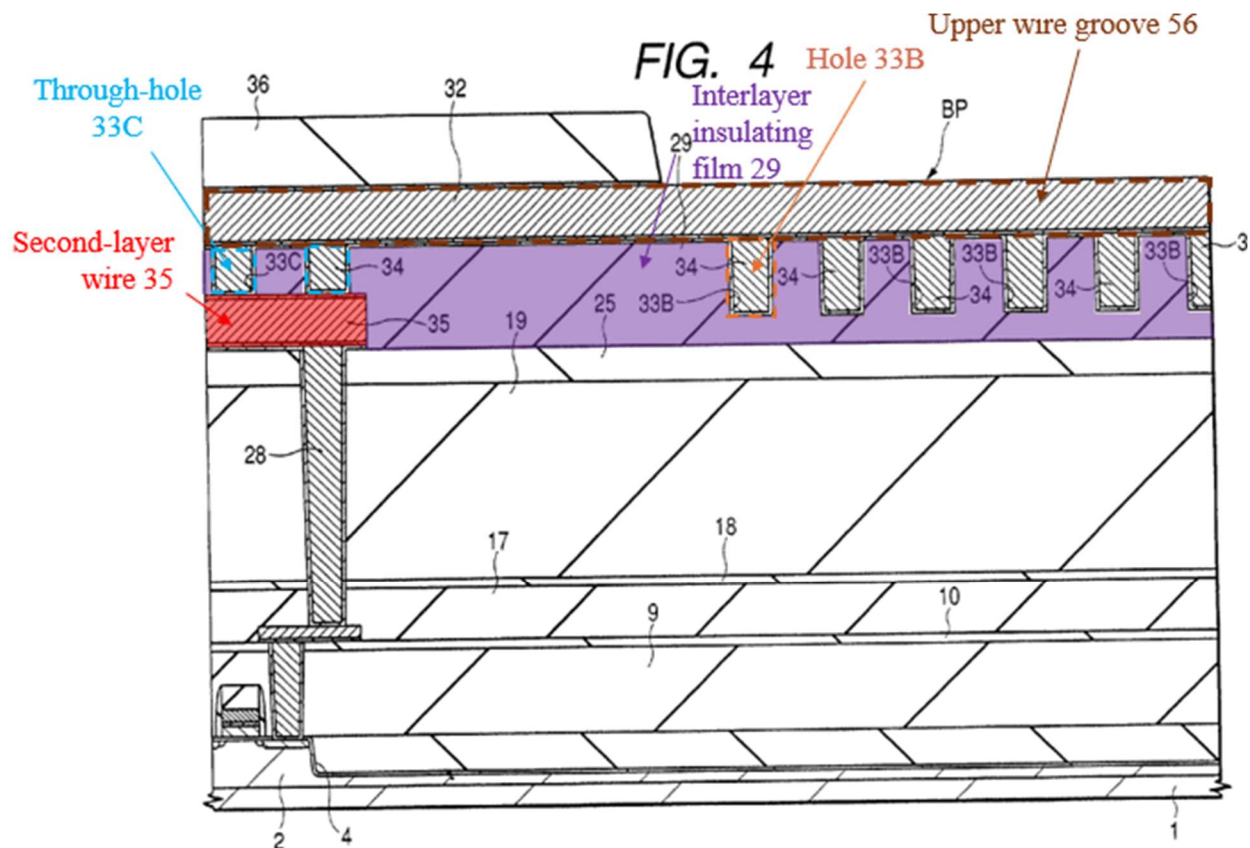
“[i]n...insulating film 29 beneath the bonding pad BP, a plurality of **holes 33B** are formed....” TSMC-1006, ¶[0052]. Also, “through-hole 33A” and “through-hole 33C” are “formed in the interlayer insulating film 29.” *Id.*, ¶¶[0050], [0055], Fig. 4. Thus, all holes 33A, 33B, 33C are formed in insulating film 29. TSMC-1003, ¶355.

Given Aoyagi’s discussion of using a dual damascene process to form wire 31/bonding pad BP and deposit conductive material in holes 33A and 33B, Aoyagi teaches and/or suggests using a dual damascene process to form bonding pad BP (with lead wire 32) as well as the vias formed in holes 33C and the dummy vias in holes 33B in the structure of Figures 3-4 as discussed above. TSMC-1003, ¶¶356-57; *supra*, §§VI(A)(1), VI(H)(1). A POSITA was motivated by the increased efficiency, reduced cost, and increased reliability benefits of the dual damascene process, and could have easily implemented such a process given its widespread use. *Id.*

Regarding formation of an interconnect trench, for the dual damascene approach, Aoyagi discloses upper wire groove 56 formed in insulating film 29. TSMC-1006, ¶[0077], Fig. 19; *see also id.*, ¶¶[0050]-[0055]. “Third-layer wire 31”/“upper wire 31” – which includes bonding pad BP – is deposited in wire

groove 56. *Id.*, ¶[0077], Fig. 19; TSMC-1003, ¶¶358-59; *see also* TSMC-1015, 3:63-4:22.

For Aoyagi’s dual damascene approach when applied to the Figure 4 device, upper wire groove 56 (for upper wire 31/bonding pad BP) would connect via holes 33C and dummy holes 33B (TSMC-1003, ¶359):¹⁰



Additionally, holes 33B are “arranged so as to be incapable of having current flow therethrough.” TSMC-1003, ¶¶360-62. As illustrated in Figures 4 and 19,

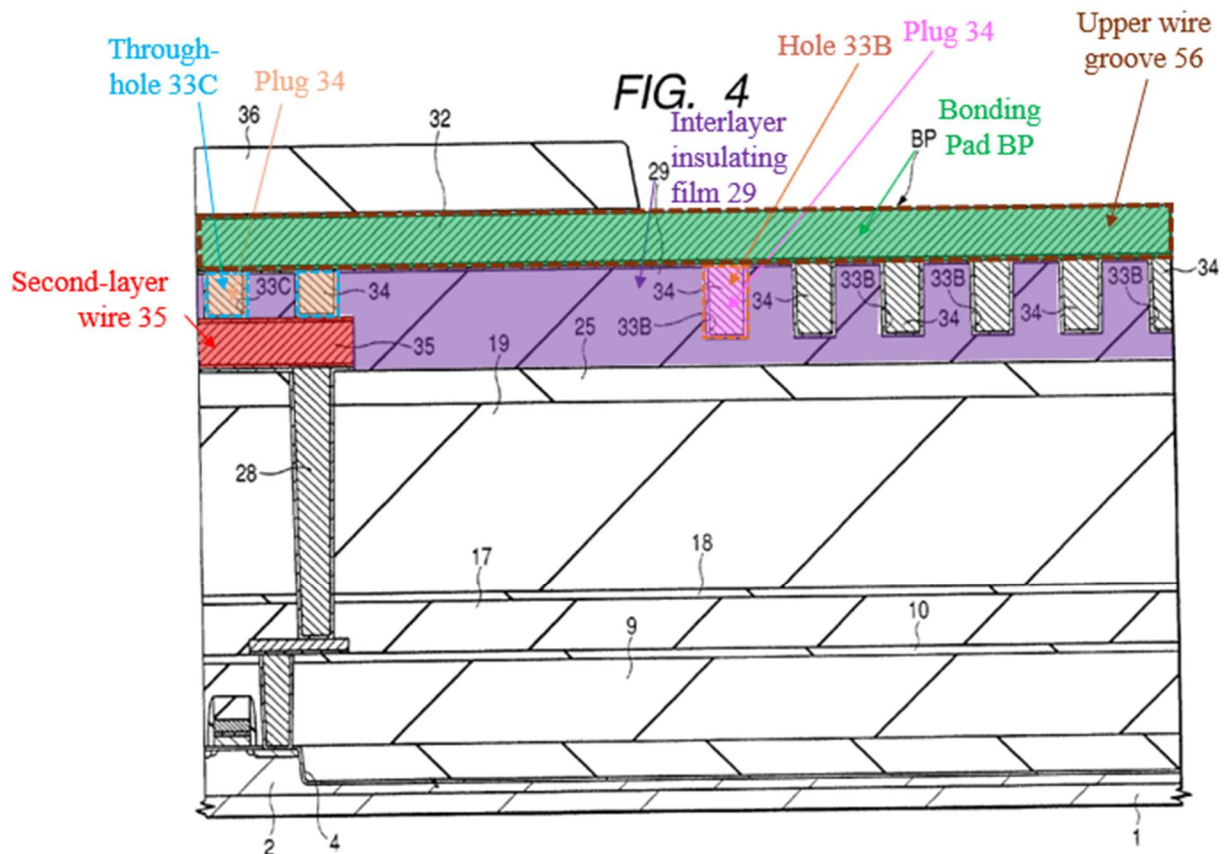
¹⁰ For dual damascene as in Figure 19, second-layer wire 35 is in the insulating film just underneath insulating film 29. TSMC-1003, ¶359, n.11.

holes 33B and plugs 34 therein are formed entirely within one or more insulating films. These “dummy” holes 33B and “dummy” plugs 34 are only connected on one end to an active circuit element (i.e., “bonding pad BP”), while the other end is not connected to a second active circuit element. Dummy holes 33B and associated plugs 34 therein improve “adhesion” between bonding pad BP and insulating film 29. TSMC-1006, ¶¶[0053], [0079]; Fig. 4. Thus, no current flows through Aoyagi’s dummy holes 33B or (dummy plugs 34 formed therein) due to this lack of connection to a second active circuit element. TSMC-1003, ¶360. Instead, current flows between Aoyagi’s second-layer wire 35 and bonding pad BP through plugs formed in holes 33C, which constitute parts of a closed circuit in actual use of the device. TSMC-1006, ¶[0055] (“[B]onding pad BP is connected at one side thereof with one end of a lead wire 32. The lead wire 32 is connected, at the other end, with a lower (second-layer) wire 35 via 33C...”), Figs. 3-4; TSMC-1003, ¶360.

Moreover, Aoyagi’s device would still be operable if holes 33B and plugs 34 therein were omitted, because current would flow through the active circuit elements (i.e., bonding pad BP, holes 33C and plugs 34 therein, and second-layer wiring 35) during actual use of the device. TSMC-1003, ¶361. Accordingly, holes 33B and plugs 34 therein do not constitute parts of a closed circuit during actual use of the device and the device would function without them. *Id.*

e) 1[d]

Aoyagi discloses depositing a conductive material (e.g., “barrier metal film 34a,” “Al alloy film 31b, 42b”) in the via hole (e.g., “through-hole 33C”), the dummy hole (e.g., “hole 33B”) and the interconnect trench (e.g., “upper wire groove 56”), thereby forming a via (e.g., “plug 34” in “hole 33C”), a dummy via (e.g., “plug 34” in “hole 33B”) and a second interconnect (e.g., “bonding pad BP” in “upper wire groove 56”). TSMC-1006, ¶¶[0050]-[0055], [0077], Figs. 2-4, 19; TSMC-1003, ¶¶364-67.

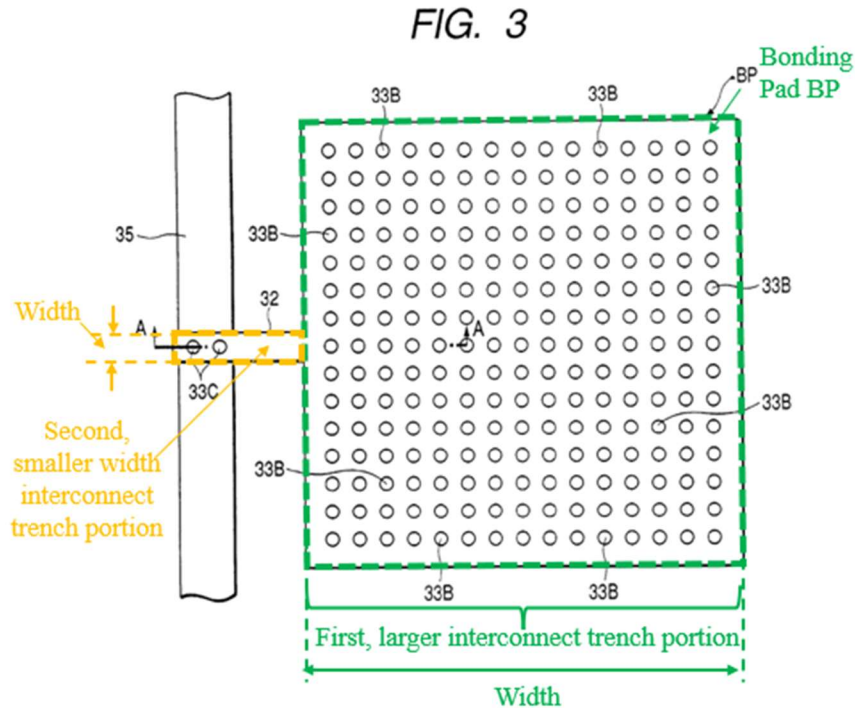


When utilizing the dual damascene process in this manner, conductive material (e.g., “barrier metal film 34a,” “Al alloy film 31b, 42b”) is deposited in hole 33C, dummy hole 33B, and upper wire groove 56, thereby forming a via (e.g., “plug 34” in “hole 33C”), a dummy via (e.g., “plug 34” in “hole 33B”) and a second interconnect (e.g., “bonding pad BP”), satisfying limitation 1[d]. TSMC-1003, ¶367.

3. Claim 3

a) [3a]

Aoyagi’s bonding pad BP (with lead wire 32) includes a first interconnect portion and a second interconnect portion having a smaller width than the first interconnect portion and that branches from the first interconnect portion (TSMC-1003, ¶¶369-70):

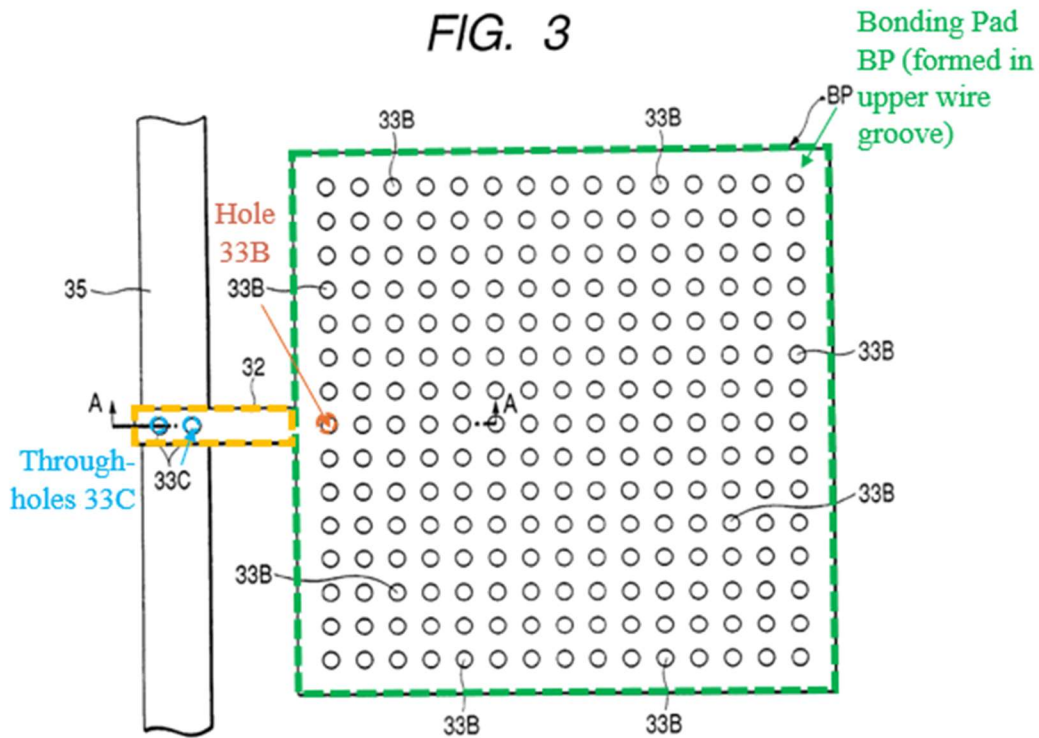


Aoyagi discloses a dual damascene process for forming third-layer wiring that includes bonding pad BP. *Supra*, §§VI(H)(1)-(2). The shape of the wire groove/trench mirrors the shape of the resulting bonding pad BP (with lead wire). TSMC-1003, ¶371. Accordingly, the wire groove/trench is shaped to form bonding pad BP in Aoyagi’s Figure 3, satisfying limitation 3[a]. *Id.*

b) [3b]

Via holes (e.g., “through-holes 33C”) and dummy holes (e.g., “holes 33B”) are connected to the interconnect trench (i.e., wire groove 56 used to form bonding pad BP) (TSMC-1006, ¶¶[0054]-[0056], Fig. 3; TSMC-1003, ¶¶372-73; *supra*, §VI(H)(2)(d)):

FIG. 3



As shown in Figure 4, via holes 33C and dummy holes 33B are connected to bonding pad BP, and thus holes 33B, 33C are likewise connected to the interconnect trench (e.g., “upper wire groove 56”) when forming bonding pad BP using Aoyagi’s disclosed dual damascene process (TSMC-1003, ¶373):

FIG. 3

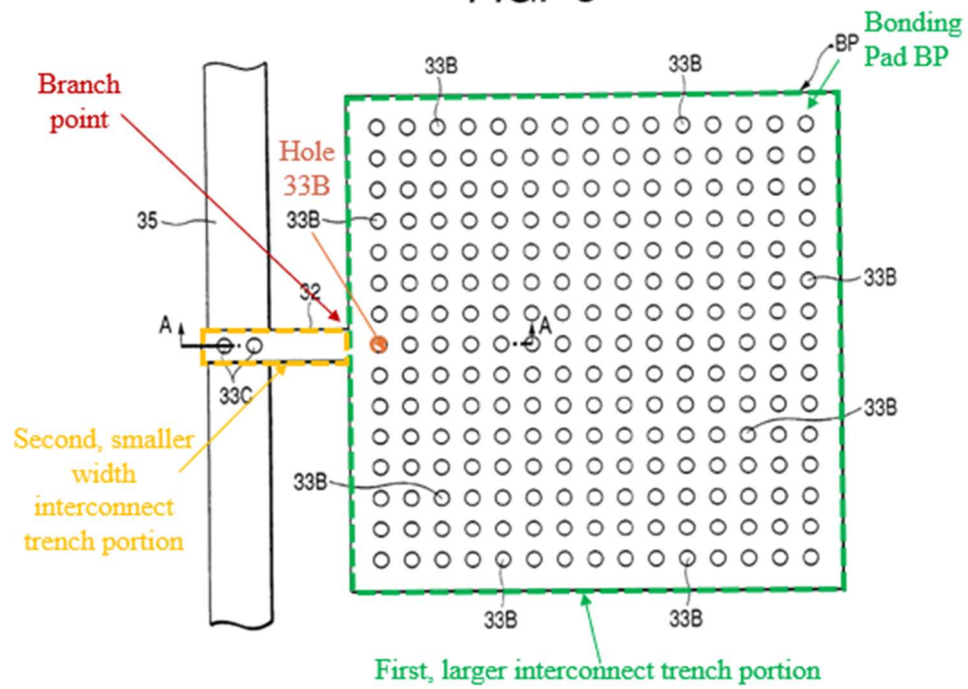
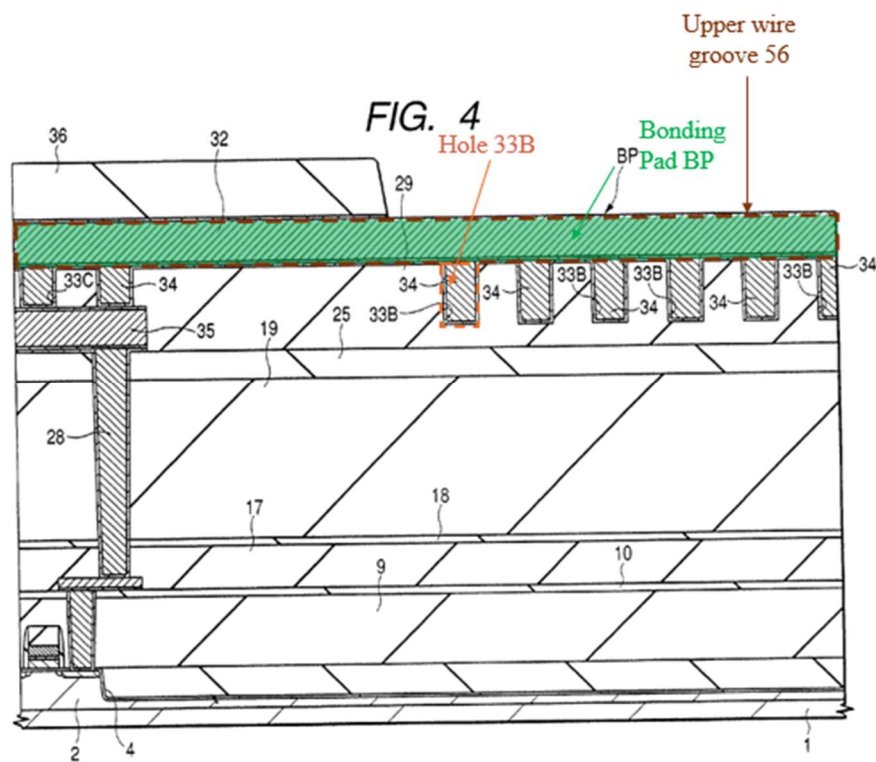
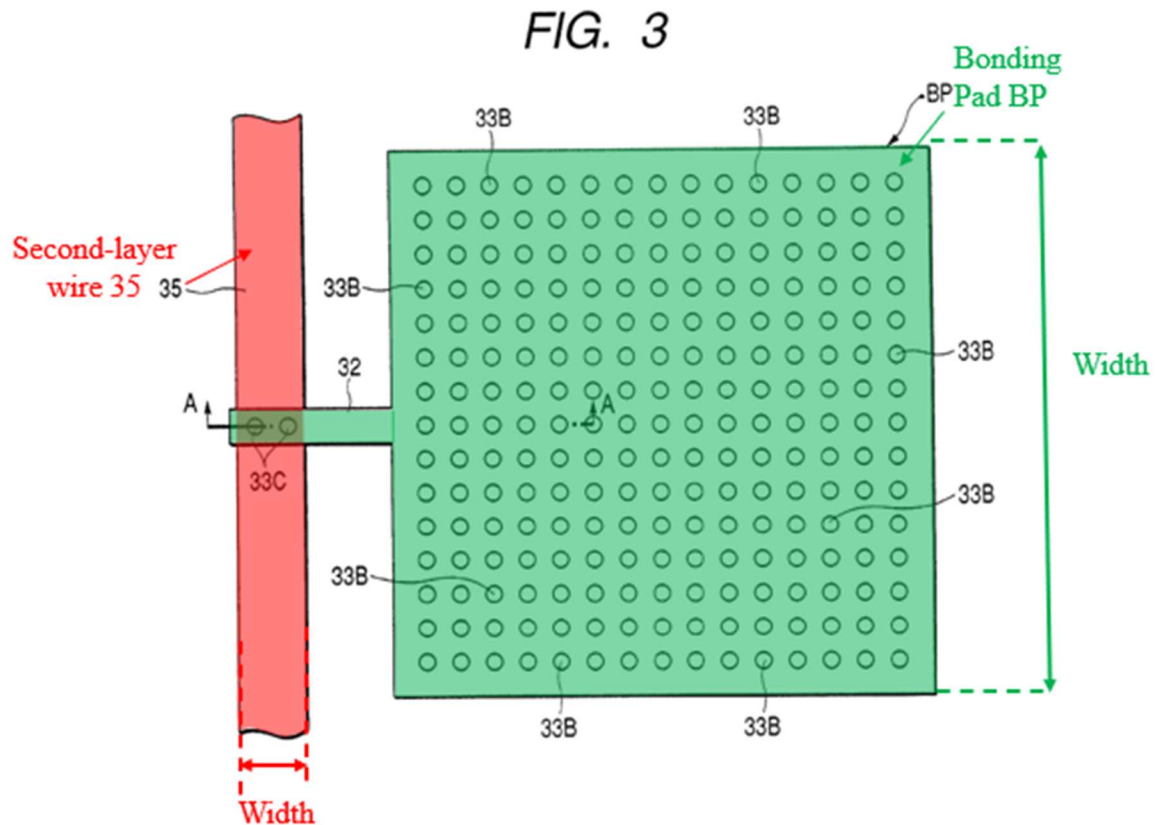


FIG. 4



5. Claim 7

Aoyagi's first interconnect (e.g., "second-layer wire 35") has a width smaller than that of the second interconnect (e.g., "bonding pad BP") (TSMC-1006, Fig. 3; TSMC-1003, ¶¶377-78):

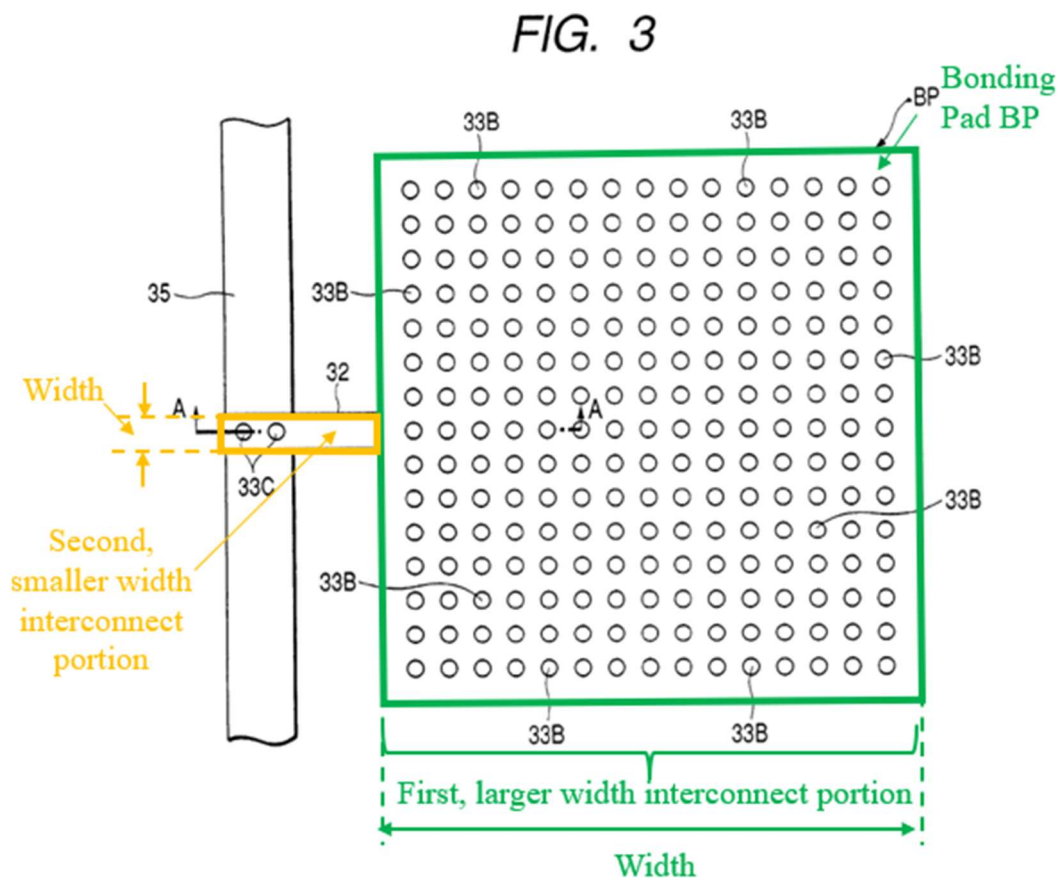


6. Claim 14

As shown below, a bottom of Aoyagi's dummy via (plug 34 within hole 33B) is located deeper than a bottom of the via (e.g., plug 34 within hole 33C) (TSMC-1006, ¶[0062], Figs. 4, 19; TSMC-1003, ¶¶379-80):

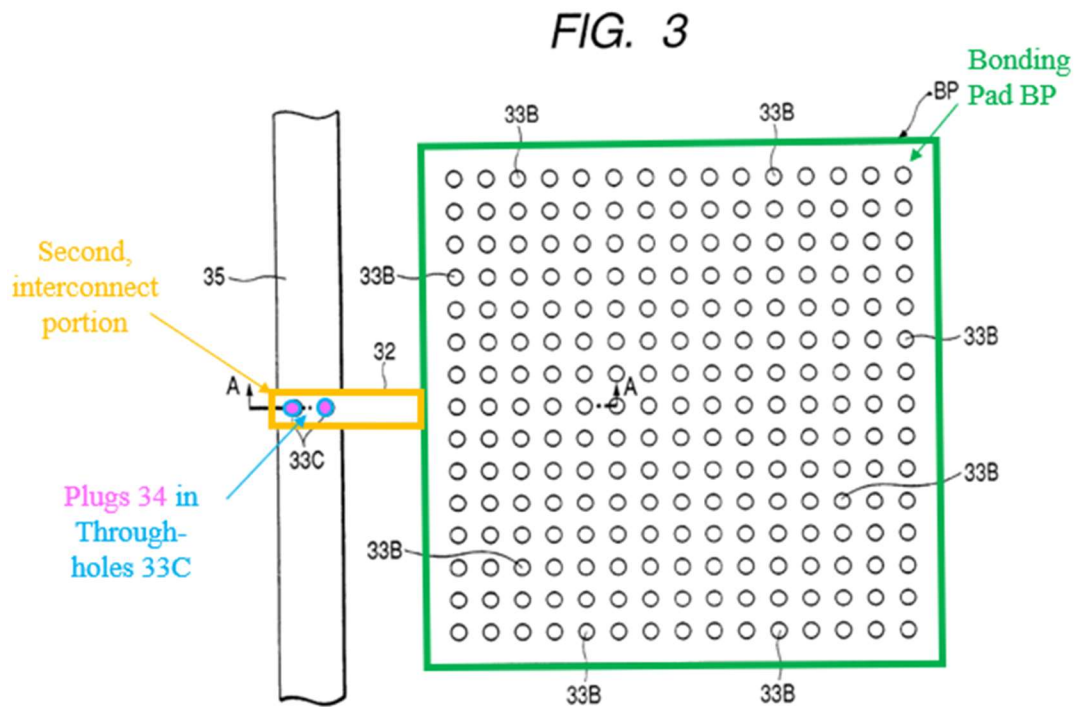
a) [15a]

As shown in Figure 3, Aoyagi discloses a second interconnect (e.g., “bonding pad BP” with “lead wire 32”) having a first interconnect portion (wider portion of “bonding pad BP”) and a second interconnect portion with a smaller width and branching from the first interconnect portion (“lead wire 32” portion of “bonding pad BP”) (TSMC-1003, ¶¶381-82; TSMC-1006, Fig. 3, ¶[0055]):



b) [15b]

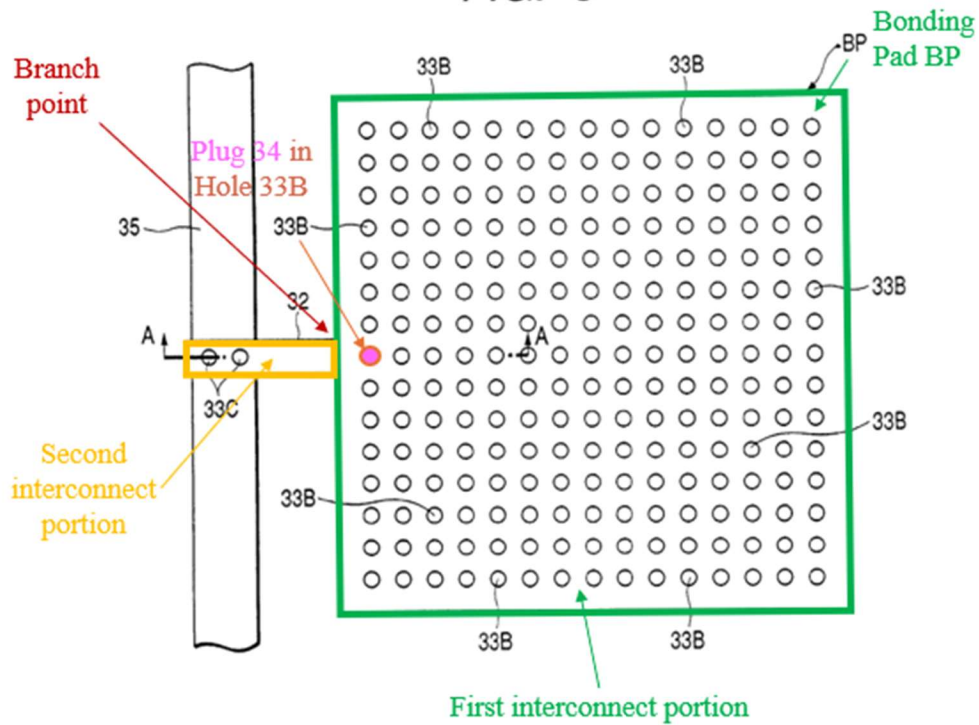
Aoyagi’s vias (e.g., plugs 34 in holes 33C) are connected to the second interconnect portion (e.g., lead wire 32 portion of bonding pad BP). TSMC-1006, ¶[0054]-[0055], Fig. 3; TSMC-1003, ¶383.



8. Claim 16

Dummy hole 33B (and plug 34 therein) is formed near the branch point between the first and second portions (wider bonding pad BP portion, lead wire 32 portion, respectively) of the second interconnect (bonding pad BP) (TSMC-1003, ¶384; TSMC-1006, Fig. 3):

FIG. 3



9. Claim 19

Aoyagi's dummy via (e.g., plug 34 in hole 33B) includes a first and second end, the first end connected to the second interconnect (e.g., bonding pad BP) (TSMC-1006, ¶¶[0050]-[0056], [0077], Figs. 4, 19; TSMC-1003, ¶¶385-86):

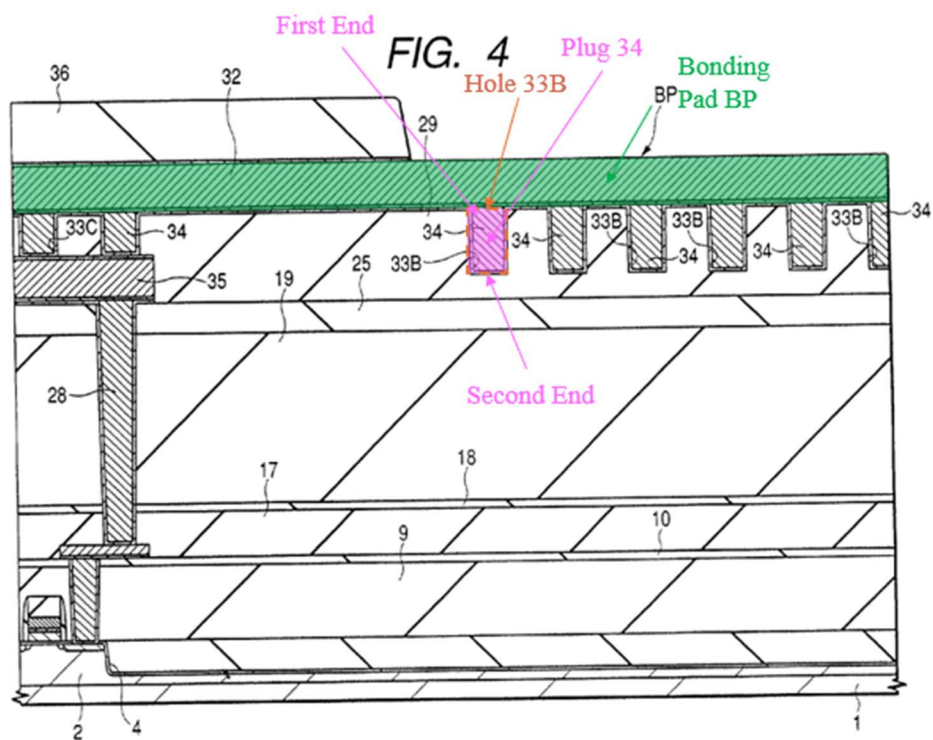
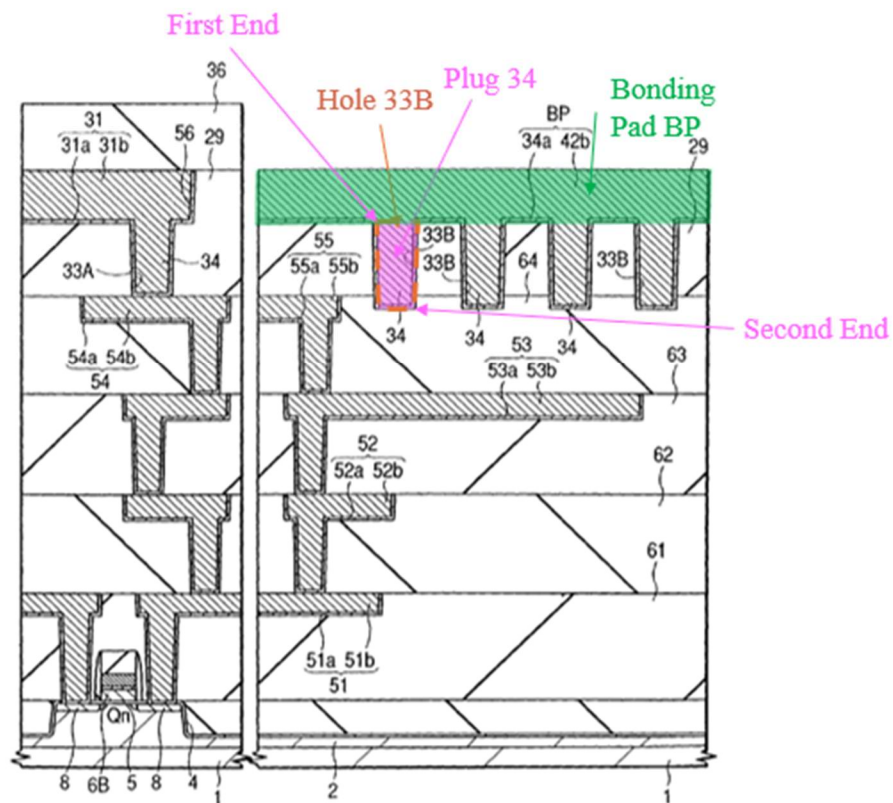
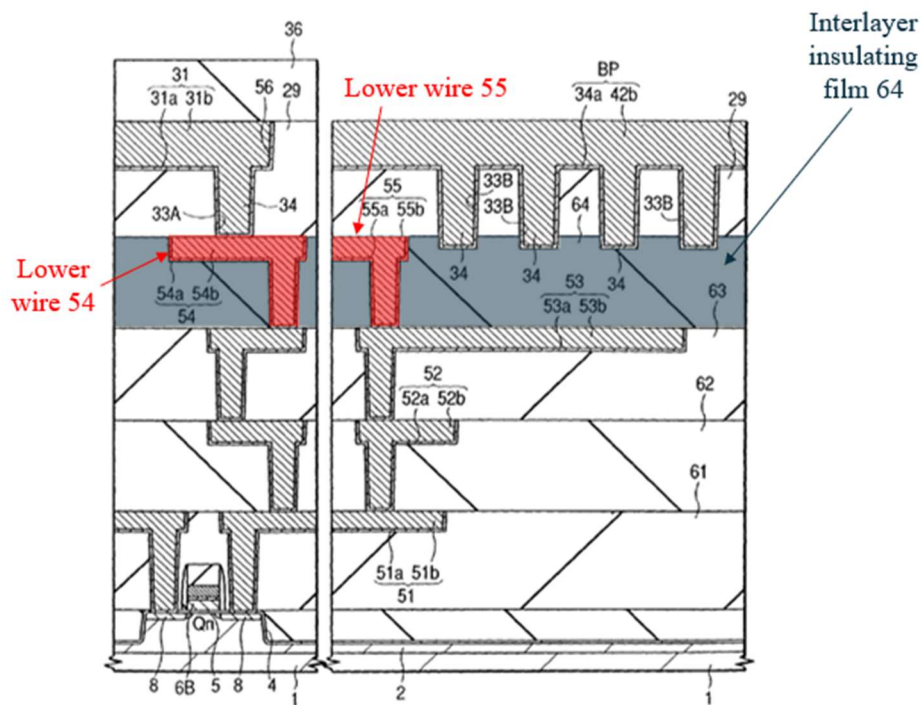


FIG. 19



The respective, common cross-hatching in each layer of the device of Figure 19 indicates that each wiring layer and its corresponding vias are formed by a dual damascene process. TSMC-1003, ¶387. Thus, a POSITA understood that when implementing Aoyagi's dual damascene process, each wiring layer is formed within a respective insulating layer as shown generally below for lower wires 54/55 and their underlying vias (*id.*):

FIG. 19



Accordingly, when wire 35 of Figure 4 is formed by dual damascene just as lower wires 54/55 are in Figure 19, wire 35 resides in an insulating film separate from insulating film 29 (in which interconnect 32/bonding pad BP and holes 33C

are formed), similar to lower wiring layers 51-54 of Figure 19. *Id.*, ¶¶388-89.

Subsequently, over-etching results in holes 33B extending below an upper surface of wire 35 and into “the second insulating film” in which wire 35 is formed in the dual damascene process. *Id.* Thus, as demonstrated in Figure 19 above, when implementing dual damascene processing, the second end of Aoyagi’s dummy via (“plug 34” in “hole 33B”) would be surrounded by a second insulating film (e.g., similar to “interlayer insulating film 64”). *Id.*; see TSMC-1006, ¶¶[0048], [0055]-[0056], [0060]-[0061], [0077], Fig. 19.

Thus, given Aoyagi’s discussion of dual damascene processing to form wire 31/bonding pad BP and form plugs 34 in holes 33A and 33B, it was obvious to use the dual damascene process to form bonding pad BP along with the dummy vias formed in holes 33B in the structure of Figures 3-4 as discussed above. TSMC-1003, ¶390; *supra*, §VI(H)(1). Doing so would result in dummy vias having lower ends that are surrounded by a second, lower layer insulating film in a similar manner as in Figure 19. TSMC-1003, ¶390.

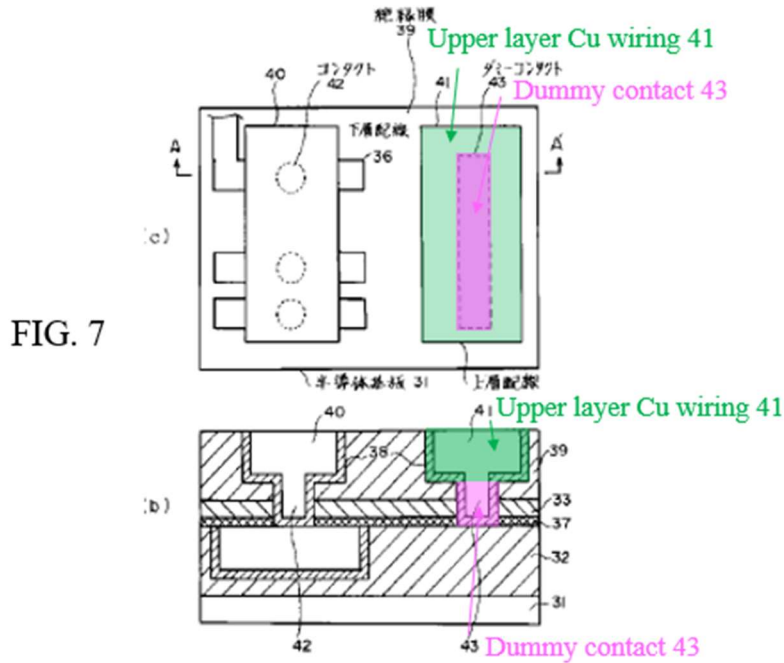
I. GROUND 9: Aoyagi combined with Fukazawa renders Claim 17 unpatentable

Claim 17 is obvious over Aoyagi and Fukazawa. TSMC-1003, ¶¶391-402.

1. Claim 17

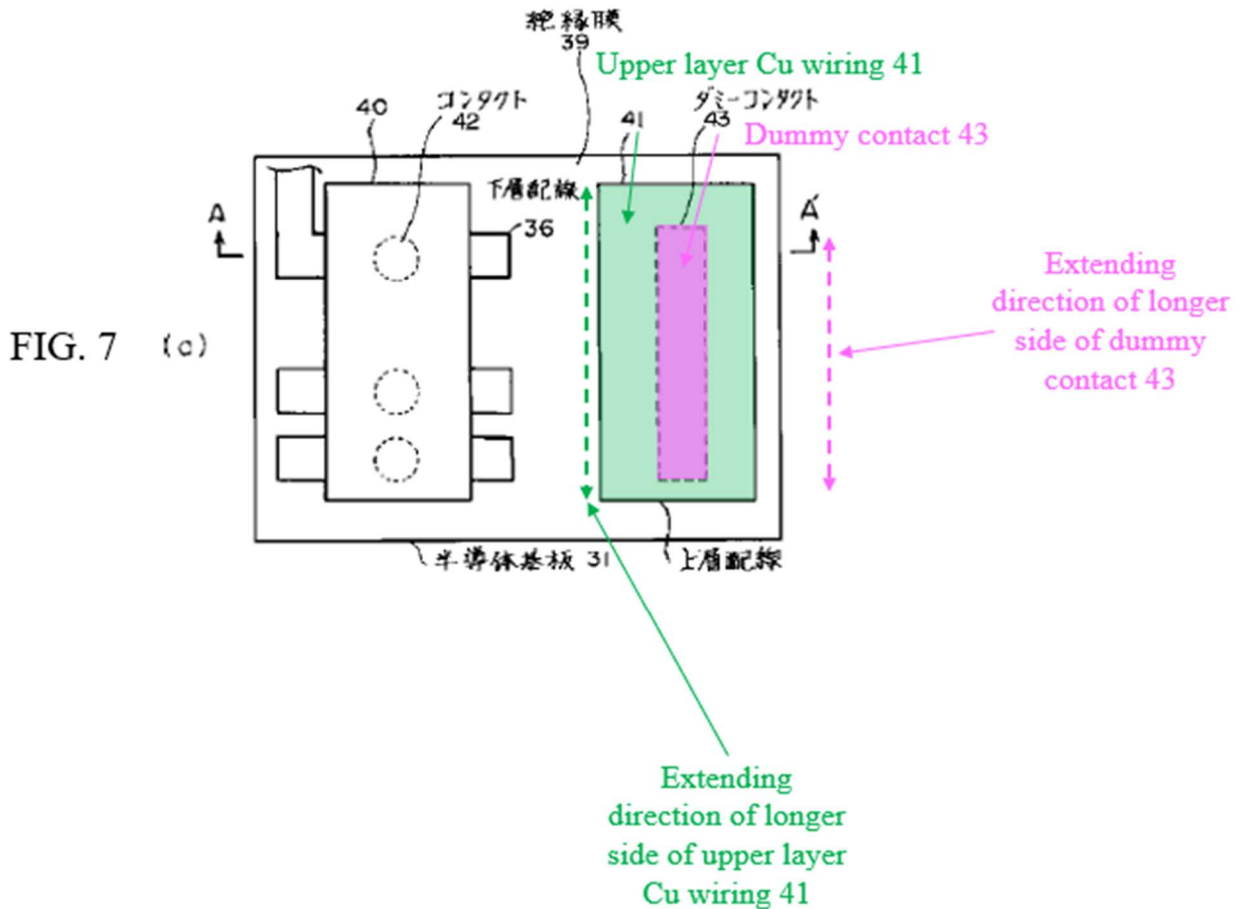
a) [17a]

Fukazawa's dummy via (e.g., “dummy contact 43”) has a substantially rectangular shape in a plan view (*supra*, §VI(C)(2)(a); TSMC-1003, ¶392):



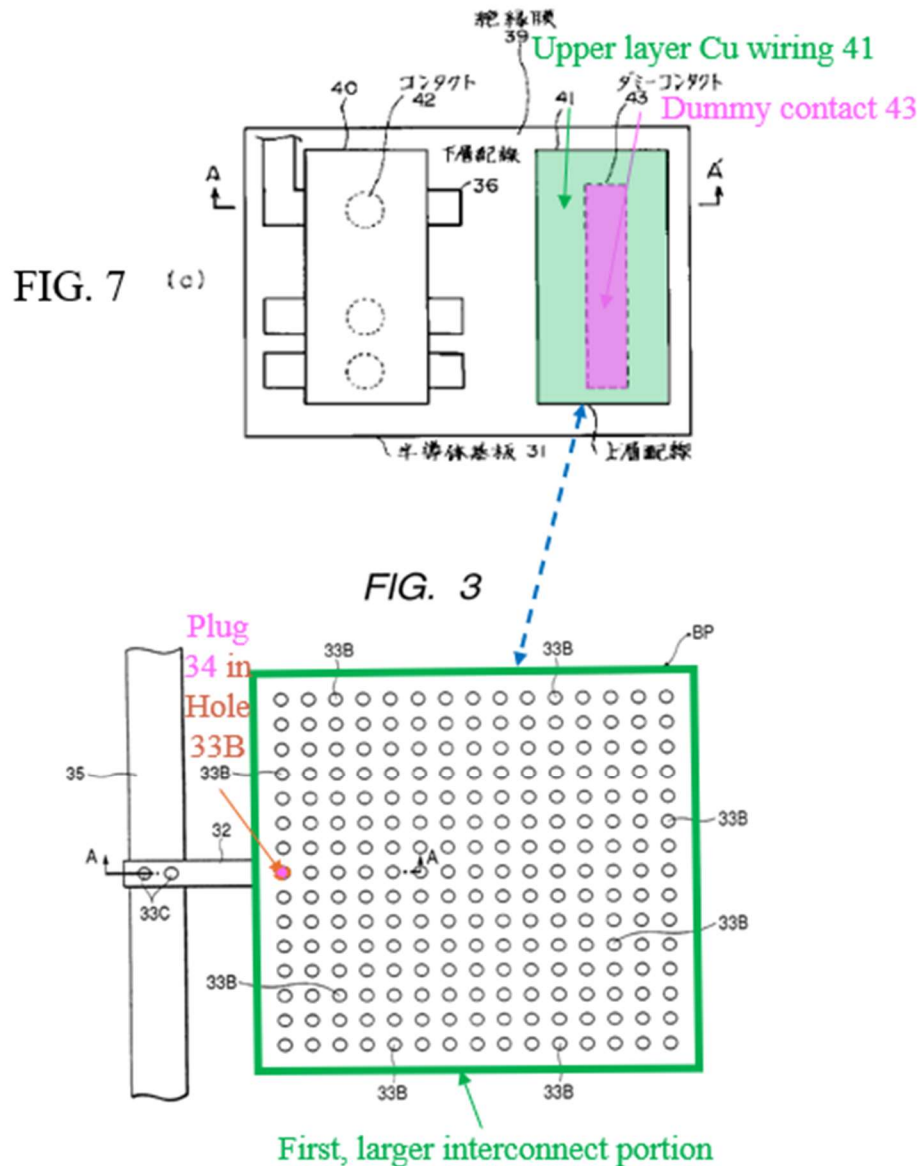
b) [17b]

A longer side of dummy contact/via 43 is provided along a same direction as a longer side of a rectangular interconnect (“upper layer Cu wiring 41”) (*supra*, §VI(C)(2)(b); TSMC-1003, ¶393):



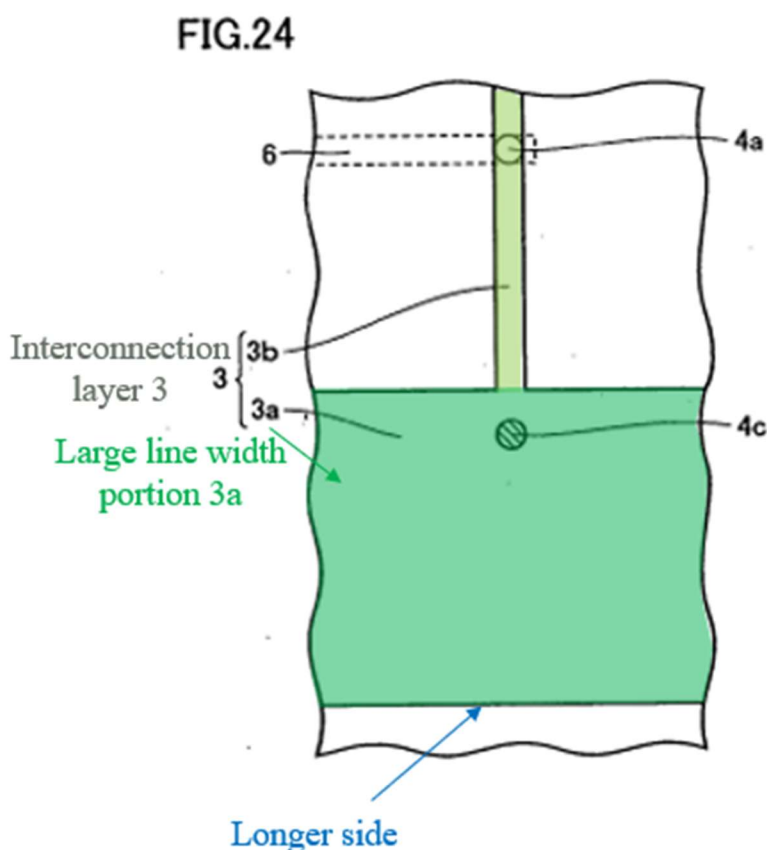
c) Combining Aoyagi and Fukazawa

It was obvious to make the larger width first interconnect portion of Aoyagi's bonding pad BP into a rectangular shape (similar to Fukazawa's wirings 40/41) and to incorporate a rectangularly-shaped dummy via (similar to Fukazawa's dummy contact 43) in place of one or more of Aoyagi's circular dummy vias in holes 33B in the very orientation taught in Fukazawa (i.e., such that a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction) as shown below (TSMC-1003, ¶¶394-402):



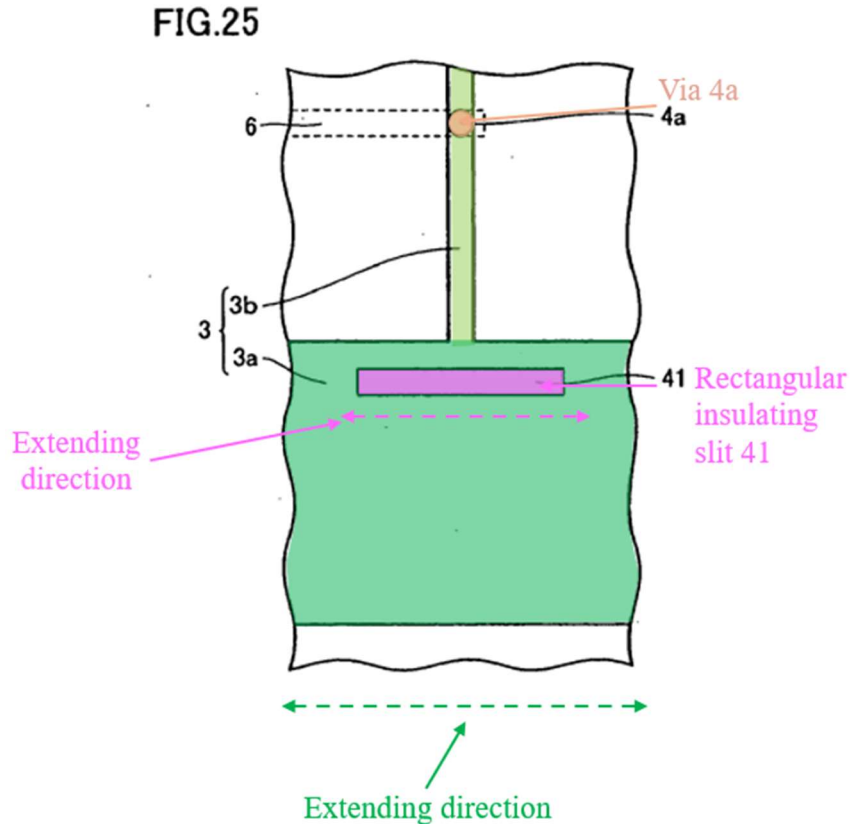
As shown above, Fukazawa discloses the common rectangular shape of interconnects such that they have “longer” sides. *See also* TSMC-1035, 1:26-28 (“Typical bonding pads in the prior art have...a rectangular or square configuration”). Changing the shape of the larger width portion of bonding pad BP to a more rectangular shape having a longer side perpendicular to the narrower portion/lead wire 32 was thus an obvious design choice. TSMC-1003, ¶395. A

POSITA would have used a rectangular shape wherever that shape was amenable to the circuit design, space constraints and desired surface area for bonding pad BP according to the requirements of the device being designed. *Id.* Kamoshima demonstrates the understanding at the time that such a rectangular shape was a suitable design option for a wide portion of a branched interconnect (*Id.*; TSMC-1009, Figs. 23-26):



A POSITA was further motivated to use a rectangular via with such an interconnect for increased strength as discussed above. *Supra*, §VI(C)(2)(c); TSMC-1003, ¶396; TSMC-1010, ¶[0018]. Additionally, a POSITA recognized the benefits of using the rectangular shape and positioning it along a longer side of the

wider portion of the branched interconnect to further reduce vacancy migration to (and thus void formation within) a via in the narrow branch of the interconnect. TSMC-1003, ¶397. Indeed, Kamoshima teaches a rectangular structure in this orientation and for this reason (*id.*):



Positioning a rectangular dummy via in the same position as insulating film 41 would have suppressed vacancy migration (similar to dummy vias 4c in Kamoshima's Figure 23-24 embodiments) and provided a larger area of vacancy interception through a rectangular shape via positioned along a length of the wider portion of the interconnect (and thus perpendicular to the narrow branch portion). *Id.*, ¶398.

Such a modification had a reasonable expectation of success. *Id.*, ¶¶399-402. A POSITA was capable of substituting a rectangular via for Aoyagi's circular dummy vias and extending a length of bonding pad BP to accommodate a rectangular via, which could have been reliably achieved using standard patterning techniques. *Id.*; *supra*, §VI(C)(2)(c). Rectangular vias were known and used and positioning them where desired was easily achieved. *Id.*

VII. GROUNDS FOR STANDING

Petitioner certifies the '751 patent is available for *Inter Partes* Review and Petitioner is not barred or estopped from requesting Review on the identified grounds.

VIII. MANDATORY NOTICES AND FEES

A. Real Party-In-Interest

The real party-in-interest here is Taiwan Semiconductor Manufacturing Company Limited. No other parties directed, controlled, or funded this *Inter Partes* Review proceeding.

B. Related Matters

The '751 patent is asserted in *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Case No. 2:25-cv-00324 (E.D. Tex.).

C. Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3) and 42.10(a), Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. §42.10(b), a Power of Attorney accompanies this Petition.

LEAD COUNSEL	BACK-UP COUNSEL
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Petitioner consents to electronic service directed to the following email address: Foley_TSMC_751_IPR2025-01210@foley.com.

D. Payment of Fees

The Office is authorized to charge fees for this Petition to Deposit Account No. 19-0741. Any additional fees that might be due are also authorized.

IX. CONCLUSION

Petitioner requests IPR be instituted for the Challenged Claims.

Date: July 15, 2025

Respectfully submitted,

By: /Nicholas Lagerwall/

Nicholas Lagerwall

Reg. No. 63,272

FOLEY & LARDNER LLP

Counsel for Petitioner

**CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION,
TYPEFACE REQUIREMENTS, AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,975 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. §42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. §42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

Date: July 15, 2025

By: /Nicholas Lagerwall/

Nicholas Lagerwall
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FOLEY & LARDNER LLP
Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on July 15, 2025, true and correct copies of the foregoing document and supporting materials were served in its entirety on the Patent Owner at the following address of record listed on the USPTO's Patent Center via overnight service:

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Courtesy copies of the same documents were served electronically on prosecution counsel and Patent Owner's litigation counsel by email at the following addresses:

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