

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

U.S. Patent No. 7,632,751

Title: SEMICONDUCTOR DEVICE HAVING VIA CONNECTING BETWEEN
INTERCONNECTS

Inter Partes Review No. IPR2025-01210

**DECLARATION OF DR. REINHOLD DAUSKARDT IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,632,751**

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I, Dr. Reinhold Dauskardt, declare as follows:

I. INTRODUCTION

1. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in connection with a petition for *inter partes* review of U.S. Patent No. 7,632,751 (“’751 patent”), which I understand is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-20 of the ’751 patent (“Challenged Claims”). Claims 1-20 of the ’751 patent are included in attached Appendix B.

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the basis for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the ’751 patent is unpatentable for at least the reasons I discuss below.

II. BACKGROUND AND QUALIFICATIONS

A. Education and Career

5. I have summarized in this section my educational background, career history, and other relevant qualifications.

6. My technical background and experience are summarized in my curriculum vitae and listing of publications included below in Appendix C.

7. I am currently the Ruth G. and William K. Bowes Professor of Materials Science and Engineering in the Department of Materials Science and Engineering at Stanford University. I have additional appointments as Professor in the Department of Mechanical Engineering, the Biodesign Institute and in the Department of Surgery, Stanford School of Medicine. I am also a Visiting Professor in the School of Materials Science and Engineering at the Nanyang Technological University in Singapore.

8. I earned a B.Sc. (1980) and M.Sc. (1983) in Physics, Mathematics and Materials from the University of the Witwatersrand, South Africa. Thereafter, I earned a Ph.D. in Materials Science and Engineering from the University of California at Berkeley / University of the Witwatersrand in 1988.

9. Based on my 28 years of experience in the field of materials science, particularly in connection with the thermomechanical reliability and manufacturing processes of microelectronic devices, and based on the acceptance of my publications and professional recognition by societies in this field, I believe that I

am an expert in the technology at issue in this proceeding and am qualified to provide an opinion in this declaration.

10. I have extensive experience in integrating new materials into emerging microelectronic devices and I am an internationally recognized expert on the design and thermomechanical reliability of engineering structures and semiconductor device technologies. My experience includes semiconductor device and packaging processing operations and processing environments (including plasma processing, chemical mechanical planarization, and a wide range of deposition techniques) and their effects on device materials, structures and their properties.

11. I teach several undergraduate and graduate classes in the School of Engineering at Stanford University on materials science topics. These classes include detailed discussions of structure-property relationship of materials, semiconductor device structures, their manufacturing processes and reliability.

12. My interdisciplinary research includes interaction with researchers in academia and industry. I have served as an editor and reviewer for a number of journals and books including Nature, Science, Acta Materialia, the Journal of Applied Physics, and the Journal of Microelectronics and Electronic Packaging. I am a frequent reviewer of proposals for U.S. federal and international funding agencies, I have organized international conferences and symposia in the area of

materials and electronic devices, and have published over 350 articles in the scientific literature.

13. I am a named inventor on over 30 provisional and granted United States patents. I have served as the research advisor of 67 doctoral students who have graduated under my supervision and mentorship and currently have 14 doctoral graduate students in my research group and 2 postdoctoral scholars. I have also supervised the research programs of more than 26 master's students and mentored more than 46 post-doctoral fellows, medical residents and medical fellows along with several visiting scientists and engineers.

14. I am an internationally recognized expert on the semiconductor devices and their manufacturing processes for which I was awarded the prestigious Semiconductor Industry Association University Researcher Award in 2010 for "research which has provided substantive and sustained contributions to semiconductor industry science and technology." This research includes studies of the adhesion and cohesion of interfaces and layers in materials, and the causes and mechanisms of fracture, delamination, stress migration, voiding, fatigue and mechanical reliability of microelectronic devices and their packages, and similar studies of the materials used in the manufacture of electronic device technologies. For my research directed to CMP processing, I was awarded the VLSI/ULSI

Multilevel Interconnection (VMIC) International Conference Award in 2008 for “Optimized Curing and CMP of Nanostructured Ultra-low-k Films,” Fremont, CA.

15. My research group is well known internationally for pioneering studies of the synergistic effects of mechanical forces, chemical environments, temperature and other forms of degradation on thermomechanical stresses and the processes of fracture and defect evolution that determine the reliability of materials and devices. Our experimental studies are complimented with a range of computational and theoretical modelling capabilities.

16. I have won a number of awards including the U.S. Dept. of Energy Outstanding Scientific Accomplishment Award (1989), the Alexander von Humboldt Research Award (2002), the ASM International Silver Medal (2003), an IBM Faculty Award (2006), the TMS Structural Materials Distinguished Scientist/Engineer Award (2010), the Semiconductor Industry Association University Researcher Award (2010), the H. Maso Award for fundamental contributions to skin science (2011), and the IBM Shared University Research Award (2011).

17. I have contributed significantly to leadership in Stanford's multidisciplinary materials and microelectronic device efforts which spans several schools and the Stanford Hospital. I am also a Fellow of ASM International and a Fellow of the American Ceramic Society.

B. Publications

18. I have authored over 300 peer-reviewed academic journal publications, and I am a named inventor on at least 7 granted U.S. patents. Some examples of relevant publications to the technology at issue in this proceeding are:

- a) M. Lane, N. Krishna, I. Hashim, and R. H. Dauskardt, “Adhesion and Reliability of Copper Interconnects with Ta and TaN Barrier Layers,” *Journal of Materials Research*, 15 [1] 203-211, 2000.
- b) D. M. Gage, A.D.W. Thiel, R. H. Dauskardt, M. K. Haas, L.M. Matz, M. L. O’Neill, T. M. Wieder, G. Banerjee and M. B. Rao, “Impact of CMP polish and pCMP Cleaning on adhesion of SiCN capping layer on PECVD-derived Porous OSG and Copper” *Solid State Phenomena*, 145-146, 377-380, 2009.
- c) Ryan Birringer, Roey Shaviv, Roy H. Geiss, David Read, and Reinhold Dauskardt, “Effects of Barrier Composition and Electroplating Chemistry on Adhesion and Voiding in Copper / Dielectric Diffusion Barrier Films,” *Journal of Applied Physics*, 110, 044312, 2011.
- d) Qiran Xiao, Brian Watson and Reinhold H. Dauskardt, “Organothioliol-Based Hybrid-Layer Strategy for High-Performance Copper Adhesion and Stress-Migration via Simultaneous Oxide Reduction,” *Advanced Materials Interfaces*, 3, 14, 2016.

- e) Michael T. Barako, Scott G. Isaacson, Feifei Lian, Eric Pop, Reinhold H. Dauskardt, Kenneth E. Goodson, and Jesse Tice, “Dense Vertically Aligned Copper Nanowire Composites as High Performance Thermal Interface Materials,” *ACS Applied Materials and Interfaces*, 9 (48), pp 42067–42074, 2017. DOI: 10.1021/acsami.7b12313.
- f) Markus D. Ong, Vincent Jousseau, Sylvain Maitrejean, Reinhold H. Dauskardt: “Fracture Properties of Porous MSSQ Films: Impact of Porogen Loading and Burnout, in *Materials, Technology and Reliability of Low-k Dielectrics and Copper Interconnects*,” edited by Ting Y. Tsui, Young-Chang Joo, Lynne Michaelson, Michael Lane, Alex A. Volinsky (Mater. Res. Soc. Symp. Proc. 914, Warrendale, PA, 2006), 0914-F04-07.
- g) Ryan Birringer, Roey Shaviv, Tom Mountsier, Jon Reid, Jian Zhou, Roy H. Geiss, David Read, and Reinhold Dauskardt, “Adhesion, Cu Voiding, and Debonding Kinetics of Copper / Dielectric Diffusion Barrier Films,” *Advanced Metallization Conference*, Baltimore, 2009.
- h) M. Lane, W. Ni, R. H. Dauskardt, Q. Ma, H. Fujimoto and N. Krishna, “Effects of Interface Nonplanarity on the Interface Fracture Energy on the TiN/SiO₂ System,” in *Thin Film Stresses and Mechanical Properties VII*, vol. 516, Editors: T. Marieb, J. Bravman, M.A. Korhonen, J.R. Lloyd, *Proceedings of MRS Annual Meeting*, Boston, MA, pp. 357 – 362, 1998.

- i) Taek-Soo Kim, Qiping Zhong, Maria Peterson, Halbert Tam, Tomohisa Konno, and Reinhold H. Dauskardt, “Stress and Slurry Chemistry Effects on CMP Damage of Ultra-Low-k Dielectrics,” IEEE International Interconnect Technology Conference Proceedings, June 2007.
- j) Reinhold H. Dauskardt, Taek-Soo Kim, Qiping Zhong, Maria Peterson, Halbert Tam, and Tomohisa Konno, “Stress and Slurry Chemistry Effects on Cracking and Damage Evolution during CMP: Implications for Next Technology Nodes,” Twelfth International Conference on Chemical-Mechanical Polish (CMP) Planarization for ULSI Multilevel Interconnection (CMP-MIC), Fremont, California, 2006.
- k) M. Lane, A. Vainchtein, H. Gao, and R. H. Dauskardt, “Plasticity Contributions to Interface Adhesion in Thin-Film Interconnect structures,” Journal of Materials Research, 15 [12], 2758-2769, 2000.
- l) Ryan Birringer, Roey Shaviv, Paul Besser and Reinhold Dauskardt, “Environmentally Assisted Debonding of Copper / Barrier Interfaces,” Acta Materialia, 60, 2219–2228, 2012.

C. Compensation

19. I am being compensated for services provided in this matter at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of my work in this matter. My compensation is not contingent upon the

results of my study or analysis, the substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '751 patent.

III. MATERIALS REVIEWED

20. In forming my opinions regarding the '751 patent, I reviewed the materials discussed in this declaration, including the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

IV. LEGAL STANDARDS

21. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '751 patent are patentable, I understand that I am obliged to follow existing law.

A. Anticipation

22. I understand the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I understand that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

23. I understand that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

24. I understand that under 35 U.S.C. §103(a), “[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in §102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I understand that, in inter partes review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

25. When considering the issues of obviousness, I understand that I am to do the following:

- a. Determine the scope and content of the prior art;
- b. Ascertain the differences between the prior art and the claims at issue;
- c. Resolve the level of ordinary skill in the pertinent art; and
- d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

26. I understand that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have been asked to assume is just before the earliest claimed priority date of the '751 patent (i.e., December 3, 2003).

27. I understand that obviousness is a determination of law based on underlying determinations of fact. I understand that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of obviousness or non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the '751 patent).

28. I understand that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also understand that a person of ordinary skill in the art is presumed to know all relevant prior art. I understand that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

29. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I understand

that the following principles may be considered, and I have been asked to consider them:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

30. I understand that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I understand that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I understand that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

31. I understand the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I understand that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I understand it would be improper to consider only the specific problem the patentee was trying to solve.

32. I understand that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I understand that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I understand that in many fields,

there may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I understand that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

33. I understand that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine them. But I also understand that any “teaching, suggestion, or motivation” present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I understand this “teaching, suggestion, or motivation” test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

34. I understand that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

35. I understand that when there is a known technique to address a known problem using prior art elements according to their established functions, then a person of ordinary skill in the art would have had a motivation to combine.

36. I understand that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I understand that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. LEVEL OF ORDINARY SKILL IN THE ART

37. In my opinion, a person of ordinary skill in the art (hereinafter “POSITA”) would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

38. I understand that I am to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

39. I have not analyzed the priority date of the ’751 patent, but I note that the earliest claim of priority listed on the face of the ’751 patent is December 3, 2003. I have also treated this date as the date from which to assess the knowledge available to a person of ordinary skill in the art.

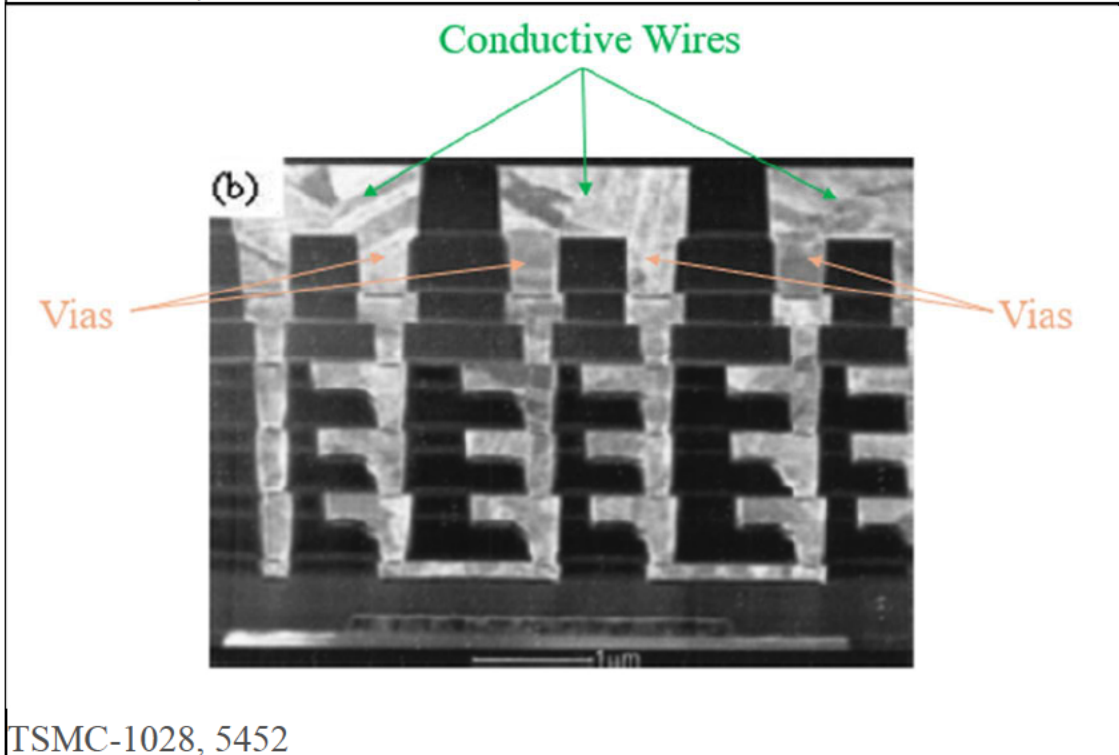
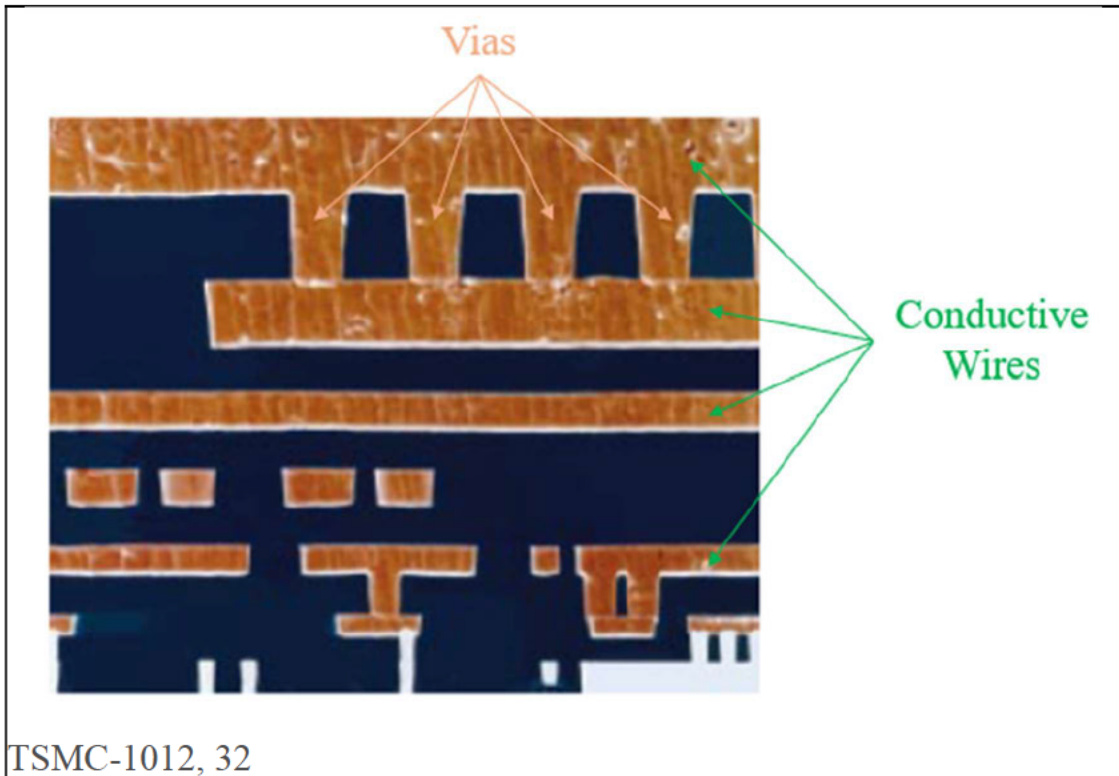
VI. TECHNOLOGY BACKGROUND

40. In my opinion, all the elements of the claims in the '751 patent were well known before December 3, 2003.

41. A person of ordinary skill in the art in the timeframe relevant to the '751 patent would have been familiar with the background information described in subsections A and B below. The '751 patent relates to the use of dummy structures to reduce stress migration and void formation in interconnect structures. Such dummy structures, for the same purposes asserted by the '751 patent, and associated methods of manufacture interconnect structures were already known.

A. Interconnects and Dual Damascene

42. Semiconductor chips have multiple levels of conductive wires ("interconnects") for controlling chip operation, with vias connecting wires between different levels when needed. TSMC-1015, 1:13-24; *see also* TSMC-1012, 32. Aluminum and copper are known interconnect materials, with copper commonly used in VLSI interconnect metallizations. TSMC-1015, 1:13-24; TSMC-1012, 32; TSMC-1017, 2:53-58. Exemplary multi-level copper wiring (interconnect) structures are shown below:



43. Introduced by the early 1990s, dual damascene is a manufacturing process where patterns of trenches and underlying via holes are filled with conductive metal(s) to simultaneously form the interconnects on a given level and the vias below that level. TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract; TSMC-1034, 671-76. The dual damascene process is illustrated below:

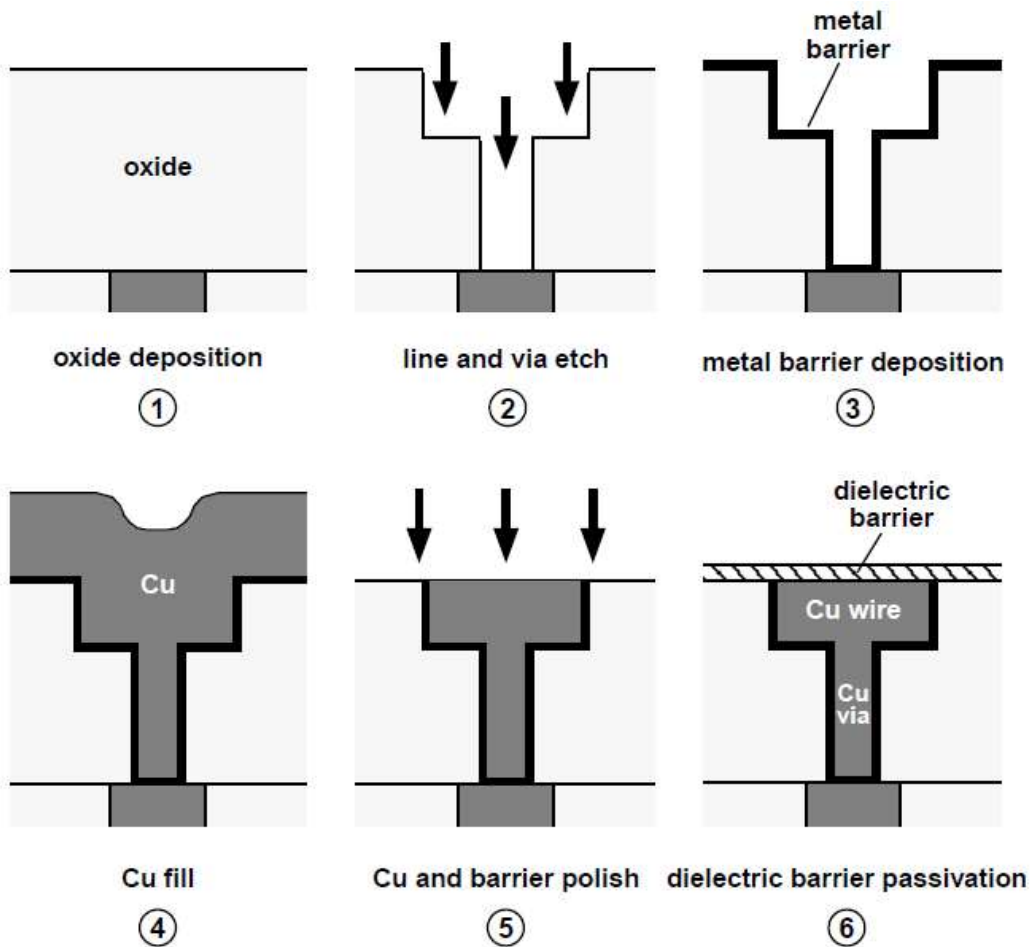


Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects.

TSMC-1027, 25. In the above process flow, steps 4→5 are typically performed using Chemical Mechanical Polishing (“CMP”). TSMC-1034, 322-24, 675.

B. Use of Dummy Structures to Improve Strength, Address Stress Migration and Void Mitigation

44. Stress migration and electromigration involve the movement of metal atoms and vacancies within the interconnect structure; because vacancies tend to aggregate in/under vias, voids can form and cause electrical disconnects. TSMC-1029, 207; TSMC-1028, 5455-56, 5458-59; TSMC-1015, 1:32-37, 2:61-63. In addition, insulating films, especially low k materials, can have lower mechanical strength and poorer adhesion that make them susceptible to damage, for example during CMP. TSMC-1016, 1:53-2:7; TSMC-1026, 583.

45. As replete in the art, dummy structures have been used well before the ’751 patent for addressing these problems. For example, dummy vias have been added near active vias to arrest stress-induced vacancy migration and void formation. TSMC-1029, Abstract, 208; TSMC-1015, 2:64-3:14. Dummy structures have been known to address electromigration reliability concerns, including dummy plugs that act as reservoirs for metallic ions and reduce mechanical stress caused by electromigration. *See* TSMC-1015, 1:66-2:11; TSMC-1032, ¶¶[0012]-[0016]. Migrating vacancies/microvoids get distributed between vias and dummy vias, reducing their concentration in/under the vias. TSMC-1029, 208; TSMC-1009,

¶[0088]. Dummy vias were also well-known to improve mechanical strength, such as to prevent damage during CMP. TSMC-1016, 4:42-47; TSMC-1026, 584-85.

46. Similar to dummy vias, dummy wirings also improve mechanical properties, helping adhesion across multiple insulating layers and leading to improved planarization after CMP by reducing dishing. TSMC-1020, Abstract; TSMC-1024, 2:55-58; TSMC-1025, Abstract; TSMC-1026, 584-85. Connecting dummy wirings to dummy vias was well-known to increase the mechanical strength of the combined insulating layer and upper-level wiring, as well as enhance the durability of multi-layered insulating films during CMP and other manufacturing steps. TSMC-1011, 8:35-54.

VII. THE '751 PATENT

A. Overview

47. The '751 patent relates to a method of fabricating a semiconductor device having multilevel interconnection structures. TSMC-1001, 6:22-7:43. A first interconnect 102A (and optionally a dummy interconnect 102B) is formed in insulating film 101. *Id.*, 11:21-26, Figs. 1A, 2B. After forming intermediate insulating layers 103-105, interconnect trench 107, via hole 106A and dummy via hole 110B are formed therein, followed by deposition of barrier film 108/copper film 109 in holes 106A, 106B and trench 107 to form via 110A, dummy via 110B, and

second interconnect 111 in a dual damascene process. *Id.*, 11:1-11:37, Figs. 1B-1C, 2A-2B.

FIG. 1B

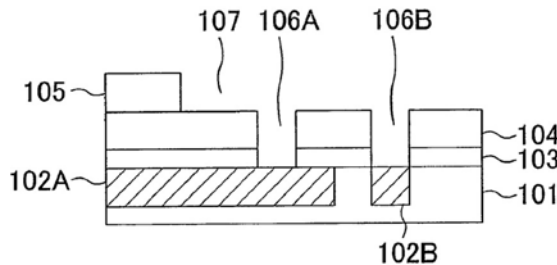
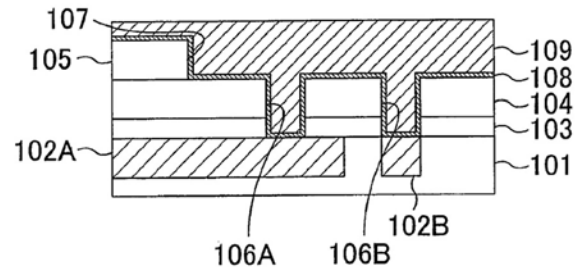
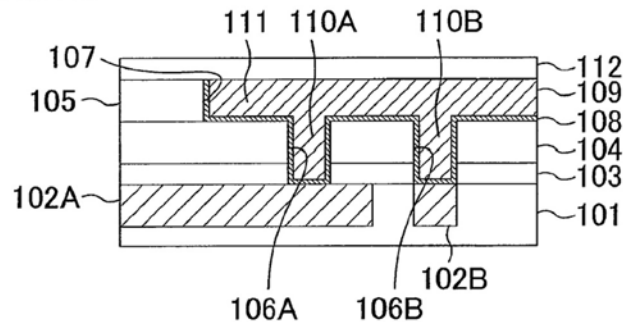


FIG. 1C



48. Via 110A connects first interconnect 102A and second interconnect 111. *Id.*, 11:31-37. Dummy via 110B connects dummy interconnect 102B and second interconnect 111, but is not connected to first interconnect 102A. *Id.*, 11:31-37; Figs. 2A-2B.

FIG. 2B



49. First interconnect 102A, via 110A and second interconnect 111 constitute part of a closed circuit during device operation, while neither dummy interconnect 102B nor dummy via 110B does. *Id.*, 10:40-44. That is, the device remains operable even if dummy interconnect 102B and dummy via 110B are omitted. *Id.*, 10:44-48. According to the '751 patent, vacancies in the copper film

109 of the second interconnect 111 are divided and respectively flow into the via 110A and dummy via 110B, reducing vacancies flowing into the via 110A and thereby reducing the associated stress gradient to the via 110A. *Id.*, 11:47-54. The '751 patent says this suppresses occurrences of voids in the via hole 106A. *Id.*, 11:57-62.

B. Prosecution History

50. The '751 application claims priority to a U.S. application filed December 2, 2004, and a Japanese application filed December 3, 2003.

51. During prosecution of the '751 patent, a first action Notice of Allowance, with reasons for allowance stating:

Claim 27 recites the limitation forming a dummy hole which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench connected to the via hole and the dummy hole. These limitations as well as the other limitations as set forth in the claims are neither taught nor suggested in the prior art.

TSMC-1002, 166.

C. Claim Construction

52. I have not been made aware of any specific claim construction to apply to the claims. I will apply the plain and ordinary understanding of the claims to a POSITA.

VIII. PRIOR ART

53. I have been informed that the following references qualify as prior art:

Reference	Filed	Published
Watanabe	12/4/2002 (USPTO)	6/26/2003
Hasunuma	9/3/2003 (USPTO)	6/17/2004
Aoyagi	3/20/2001 (USPTO)	9/6/2001
Kurashima	8/14/2003 (USPTO)	5/9/2006
Iizuka	1/24/1992 (USPTO)	10/5/1993
Kamoshima	9/9/2003 (USPTO)	9/9/2004
Fukazawa	3/29/2001 (JPO)	10/11/2002

IX. SUMMARY OF PRIOR ART REFERENCES**A. Watanabe – U.S. Patent App. Pub. No. 2003/0116852 (TSMC-1004)**

54. Because Watanabe is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 Patent purports to address (e.g., interconnect reliability), Watanabe is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1004, ¶¶[0005], [0016]-[0018].

55. Watanabe identifies the same problem of stress-related via failures in dual-damascene interconnects later addressed by the '751 patent, specifically citing stress migration leading to via lift-off or connection failure. TSMC-1004, ¶¶[0012]-[0019], [0022]-[0024]. To address stress migration, Watanabe also proposed the

same solution later claimed in the '751 patent: incorporating non-functional dummy vias formed concurrently with the functional structures using the dual damascene process. *Id.*, Abstract, ¶¶[0026]-[0028]. Watanabe further teaches that such dummy structures provide a source of copper atoms to mitigate electromigration, and enhance support for insulating film 29/second wiring 39. *Id.*, ¶¶[0026], [0070]-[0079].

56. Watanabe discloses several embodiments of semiconductor devices, and discloses a method of manufacturing (Figures 12A-12N) that applies to the device embodiments. Watanabe discloses the following embodiments:

- a “first embodiment” in Figures 1-2 (*see* ¶¶[0059]-[0087]);
- a “second embodiment” in Figures 3-4 (*see* ¶¶[0088]-[0092]);
- a “third embodiment” in Figures 5A-5C (*see* ¶¶[0093]-[0108]);
- a “fourth embodiment” in Figures 6-7 (*see* ¶¶[0109]-[0114]);
- a “fifth embodiment” in Figures 8-11 (*see* ¶¶[0115]-[0133]); and
- a more generic embodiment in Figure 14 (*see* ¶¶[0172]-[0181]).

See id., ¶¶[0038]-[0049].

57. As understood by a POSITA and as stated by Watanabe, like reference numbers in Watanabe’s figures refer to the same structures in the first to fifth embodiments, and each figure does not necessarily show all the components. In describing the second embodiment, Watanabe states that “[i]n FIG. 3, the same

reference numerals as those in FIG. 1 are affixed to the members explained in FIG. 1 and their explanation will be omitted hereunder.” *Id.*, ¶[0089]. In describing the third embodiment (Figs. 5A-5C), Watanabe notes that “[i]n these figures, in order to make the planar arrangement of each plugs and the planar shape of the second wiring 39 easy to see, the underlying layer 20 (see FIGS. 1 and 3) and each insulating films are omitted.” *Id.*, ¶[0094]. Regarding the method of manufacturing in Figures 12A-12N, Watanabe states that the method is applicable for manufacturing “the semiconductor device according to the embodiments of the present invention.” *Id.*, ¶[0135]. Regarding the embodiment of the semiconductor device in Figure 14, Watanabe states regarding its members that “[t]he underlying layer 20 in the present embodiment and each embodiments of the present invention is constructed by above members, for example.” *Id.*, ¶[0173]. The POSITA understands, therefore, that the same underlying layer 20 and insulating films as illustrated Figures 1, 3, and 14 exist in the Figure 5A-5C device structure, but are not shown in Figures 5A-5C figures.

58. Watanabe says the same for the fifth embodiment shown in Figs. 8 and 9: “In FIG. 8, reference numerals similar to those in the above are affixed to the members explained already in the above, and thus their explanation will be omitted here under.” *Id.*, ¶[0116].

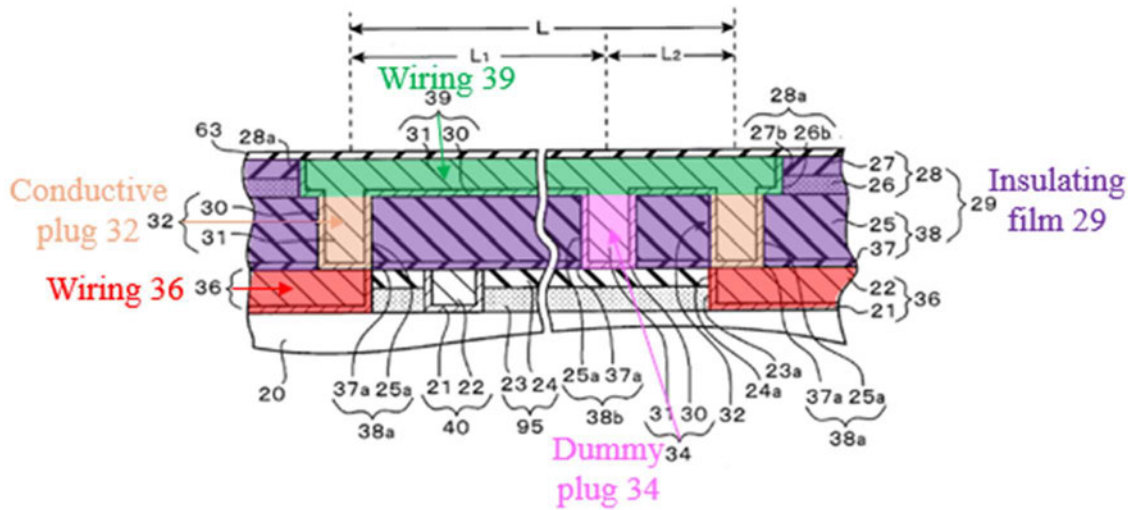
59. Watanabe teaches that the Figure 14 embodiment includes further layers built using the same manufacturing process. In introducing Figure 14,

Watanabe explains that: “Although the structure of two wiring layers (the first wiring 36 and the second wiring 39) is obtained in the above, any number of wirings can be laminated by repeating the method same to described above. The case where four layers are laminated will be explained in the following.” *Id.*, ¶[0171].

60. Watanabe describes a method of manufacturing in Figures 12A-12N, which applies to the first to fifth embodiments. Watanabe states that “a method of manufacturing the above semiconductor device will be explained with reference to FIGS. 12A to 12N hereunder. FIGS. 12A-12N are sectional views showing the method of manufacturing the semiconductor devices according to the embodiments of the present invention.” *Id.*, ¶[0135]; *see id.*, ¶[0049]. This method of manufacturing is referenced earlier when Watanabe describes the first embodiment: “[a]s will be described later, this semiconductor device is manufactured by the dual damascene process.” *Id.*, ¶[0072]. Further, Figures 12A-12N use the same reference numerals as earlier figures. While the specific device shown in Figures 12A-12N matches the second embodiment, the POSITA would recognize that the same overall process applies to the other embodiments – indeed, Watanabe states that “This manufacturing method is the so-called dual damascene process in which the wirings and the plugs are formed integrally.” *Id.*, ¶[0135].

61. Watanabe’s First Embodiment (Figs. 1, 2) discloses a structure manufactured in a manner directly analogous to that claimed in the ’751 patent.

FIG. 1

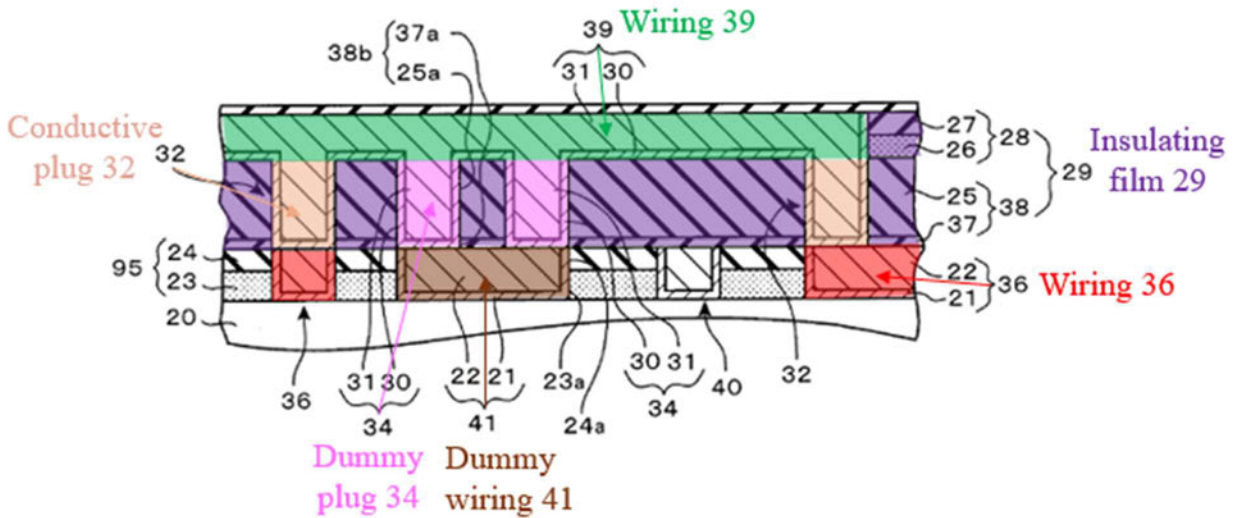


It includes a first interconnect (first wiring 36), an overlying insulating film (second insulating film 29), and a second interconnect (second wiring 39) connected by a functional via (Watanabe's conductive plug 32). Crucially, it also includes a dummy via (Watanabe's dummy conductive plug 34) formed simultaneously by dual damascene. *Id.*, Fig. 1, ¶¶[0070]-[0072]. Like the '751 patent's dummy via, Watanabe's dummy via 34 connects to the second interconnect (39) above but lands on the lower insulating layer (Watanabe's first insulating film 95) in a "non-forming region" below, rendering it incapable of carrying functional current. *Id.*, Fig. 1, ¶¶[0067], [0079]. Watanabe teaches that this dummy via reduces stress migration by shortening the effective wiring length between support points. *Id.*, ¶¶[0026], [0075], identical to the '751 patent's approach of using a simultaneously formed, non-functional dummy via connected to the upper interconnect to improve reliability

of the functional (i.e., non-dummy) via. Watanabe describes its interconnects using the term “wiring” (e.g., “wiring 36,” “wiring 39,” “wiring 51”). A POSITA understood that such wirings constitute “interconnects” as those terms are understood in the art because a wiring is a structure formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:21-28. Wiring/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:37-39.

62. Figures 3-4 disclose Watanabe’s second embodiment, which adds, among other structure, a dedicated, isolated dummy wiring 41. *Id.*, ¶¶[0028], [0090]-[0091], Fig. 3.

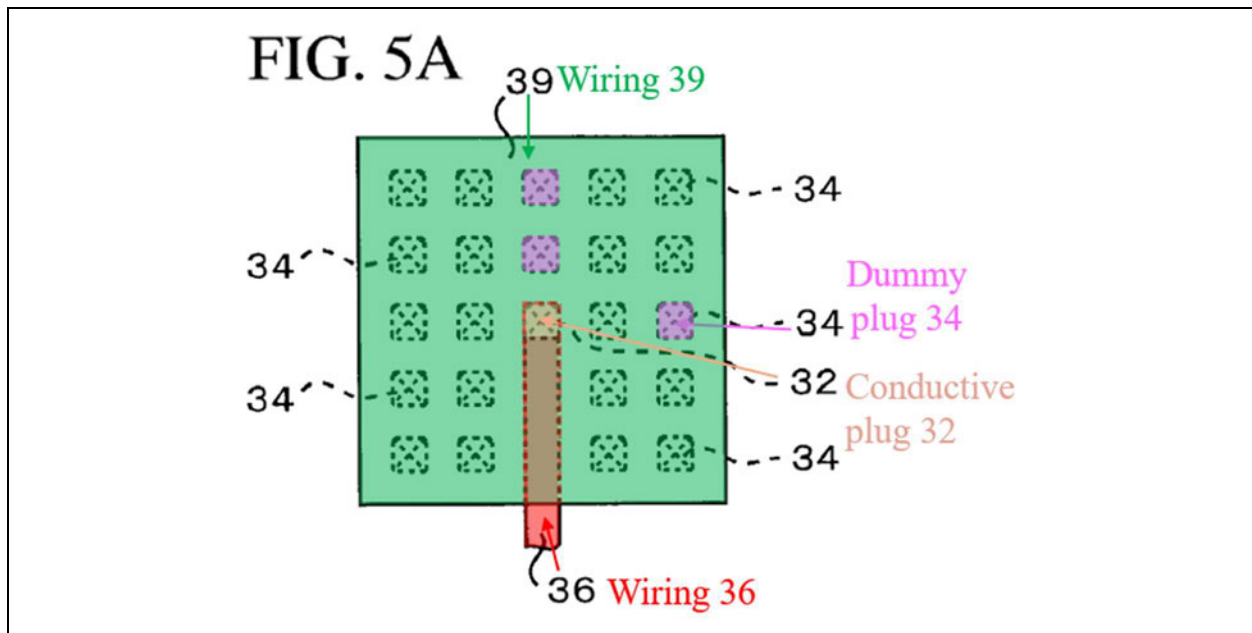
FIG. 3

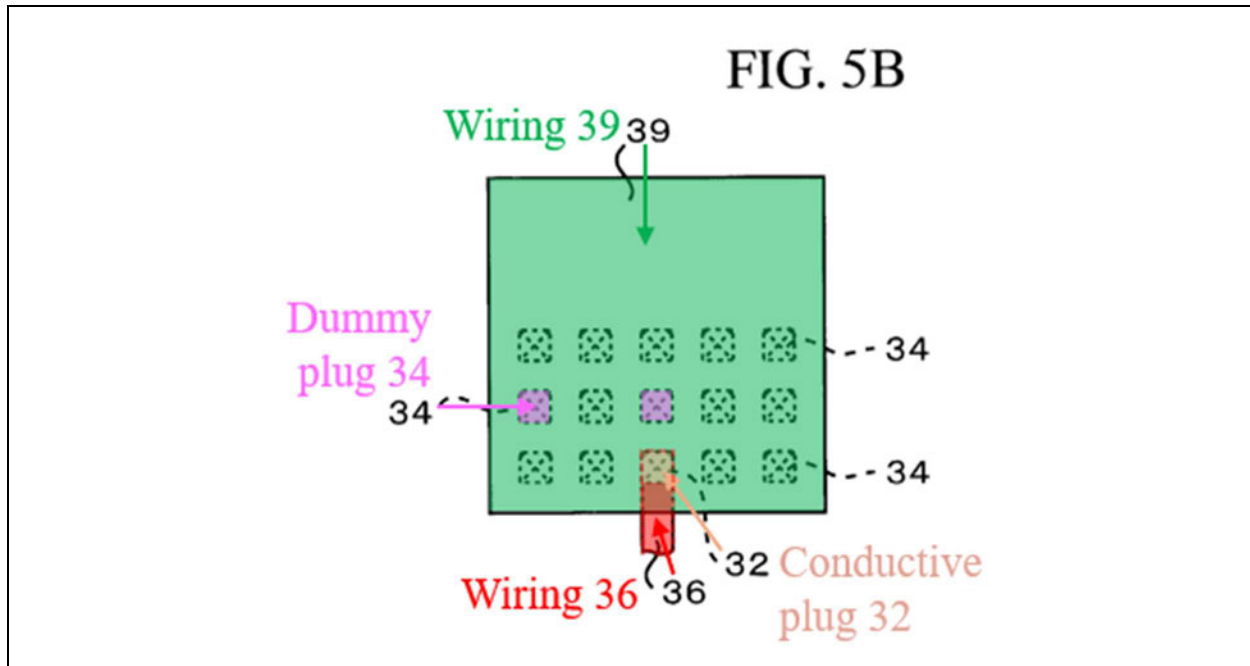


The dummy wiring 41 resides in the same first insulating film 95 as first wiring 36. *Id.*, Fig. 3. Watanabe teaches that this structure adds mechanical strength and uniformity during CMP. *Id.*, ¶¶[0028]-[0029], [0091]. Watanabe’s dummy wiring 41 is directly analogous to the ’623 patent’s “first dummy interconnect” and resides in the same lower insulating layer (Watanabe’s first insulating film 95) as the functional first interconnect (36). *Id.*, Fig. 3. Watanabe teaches that this structure offers the same stress reduction benefits plus added mechanical support. *Id.*, ¶[0091].

63. Figures 5A-5C disclose Watanabe’s third embodiment. Watanabe’s third embodiment is the same as Watanabe’s first and second embodiments in relevant part, with Watanabe’s third embodiment showing that the shape of the second wiring 39 can be varied, along with the position of plugs 32 and the positions

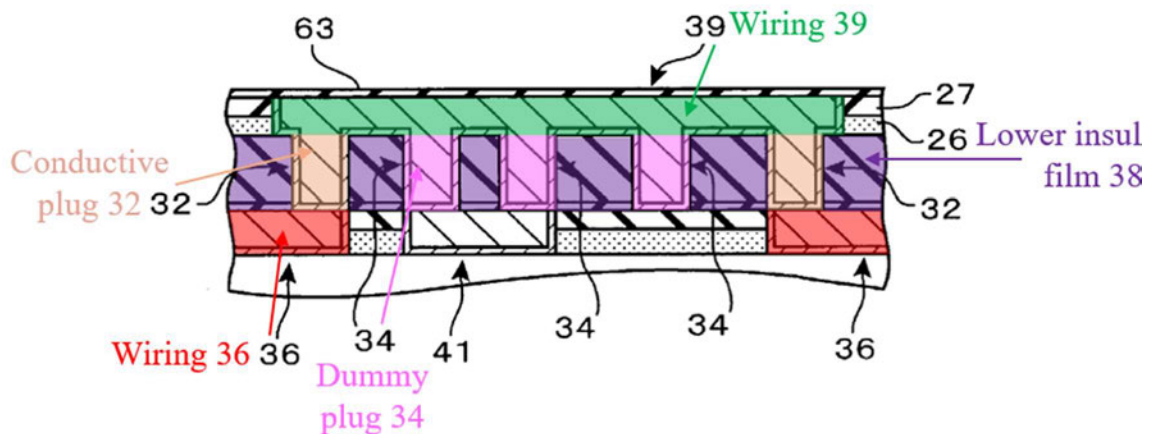
and numbers of dummy plugs 34. *Id.*, ¶¶[0093]-[0099], Figs. 5A-5C. Watanabe's third embodiment is the same in relevant respects as the first and second embodiments, with the third embodiment showing an alternative shape for the wiring 39 and different positions of plug 32 and different positions and numbers of dummy plugs 34, as exemplified in Figures 5A and 5B below:





Id., ¶¶[0093]-[0099], Figs. 5A-5C. In Watanabe’s Figures 5A-5C, a POSITA would have understood that each of the hatched squares not otherwise labeled as a conductive plug 32 constitutes a dummy plug 34, even though I highlight only a few exemplary dummy plugs 34 in the above annotations. *Id.*, ¶¶[0096]-[0098]. Also, given Watanabe’s express statement that Figure 12 represents “sectional views showing the method of manufacturing the semiconductor device according to the embodiments of the present invention,” (*id.*, ¶¶[0049], [0135] (emphasis added); *see also id.*, ¶[0094] (noting the omission of various layers in Figure 5 for easier understanding)), a POSITA understood that the cross-section of Figure 12N discloses the basic structure of Watanabe’s third embodiment (e.g., Figure 5B):

FIG. 12N



64. Figures 8-9 disclose Watanabe's fifth embodiment. Watanabe's fifth embodiment illustrates a semiconductor device having a three-level interconnect structure, as disclosed in Figure 8 (cross-section) and Figure 9 (plan view). *Id.*, ¶¶[0115]-[0133], Figs. 8-9. In Watanabe's fifth embodiment, the same numbers identifying the same elements as previously described with respect to Figure 1 are applicable to Figure 8.

65. As with the first-through-third embodiments, Watanabe's fifth embodiment structure is formed on a semiconductor substrate that is part of the underlying layer 20. *Id.*, ¶[0136], Fig. 8; *see also id.* ¶¶[0172]-[0173], Fig. 14 (showing the actual semiconductor devices formed in the semiconductor (silicon) substrate 96).

66. Moreover, Watanabe's fifth embodiment includes an additional interconnect level. *Id.*, Fig. 8. Watanabe's fifth embodiment includes the second wiring 39, the lower insulating film 68 and the third wiring 51. *Id.* Watanabe's

conductive plug 53 is formed within via hole 68a through the lower insulating film 68 and connects the third wiring 51 to the second wiring 39. *Id.*, ¶¶[0120], [0122], Fig. 8. Watanabe's dummy plug 52 is connected to the third wiring 51. *Id.*, ¶[0122], Figs. 8-9.

67. The dummy plug 52 is conductive, being composed of the same barrier metal layer 72 and copper film 71 as the third wiring 51, yet is arranged to be incapable of having current flow therethrough because it terminates in insulating layer 70 (or 68) in a non-forming region (i.e., where there is no second wiring 39) or toward an isolated dummy wiring 61. *Id.*, ¶¶[0121], [0126]-[0127], Figs. 8-9. The dummy wiring 61 is not shown in Figure 8, but it is shown in Figure 9, and Watanabe explains that the dummy wiring 61 is formed in the same layer as the second wiring 39 and that the dummy plug 52 may be connected to this dummy wiring. *Id.* Consistent with Watanabe's overall manufacturing approach using a dual damascene process (*id.*, ¶[0135]), the third wiring 51 forms a dual damascene structure simultaneously with both the conductive plug 53 and the dummy plug 52. *Id.*, ¶[0135], Fig. 8.

68. Figures 12A-12N disclose Watanabe's method of manufacturing a semiconductor device that is applicable to all the embodiments. *Id.*, ¶¶[0049], [0134]-[0170], Figs. 12A-12N. The method uses the dual damascene process to form the wiring and the plugs integrally. *Id.*

69. Figure 14 discloses a four wiring layer embodiment, where the initial structure is like that shown in Figure 1, and then further wiring layers are formed by repeating the method from Figure 12. *See id.*, ¶¶[0171]-[0181]. Figure 14 further discloses members in the underlying layer 20. *Id.*, ¶[0173], Fig. 14. The underlying layer 20 includes the gate electrode 84 and corresponding source/drain (S/D) regions, the interlayer insulating film 87, and conductive plugs formed from the barrier metal layer 85 and a metal film 86. *Id.* Watanabe explains that those members in the underlying layer 20 in Figure 14 apply to the other embodiments as well. *Id.*

70. Additionally, it was obvious to use the dual damascene method of manufacturing of Figs. 12A-12N to create respective wiring layers for any of the embodiments of Watanabe. A POSITA was motivated to do so by the increased efficiency and reduced cost benefits of the dual damascene process, and could have easily implemented such a process given its already disclosed use in Watanabe and widespread general use at the time. *See* TSMC-1034, 583-84, 671-76, 718, 723-26; TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-147; TSMC-1027, 25; TSMC-1028; 5458.

B. Hasunuma – U.S. Patent App. Pub. No. 2004/0113238 (TSMC-1005)

71. Hasunuma discloses the method of fabricating a semiconductor device recited in the '751 patent. For example, Hasunuma teaches forming a semiconductor

device having a substrate 1, a first interconnect comprising conductive layer 14, an overlying first insulating film comprising SiCN film 3, low relative dielectric constant film 4, and SiC film 2, and a second interconnect comprising conductive layer 26 formed within that first insulating film. TSMC-1005, Figs. 1A-8, ¶¶[0090]-[0108]. Hasunuma describes its interconnects using the term “conductive layer” (e.g., “conductive layer 14,” “conductive layer 26”). A POSITA understood that such conductive layers constitute “interconnects” as those terms are understood in the art because Hasunuma’s conductive layers are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:21-28. Conductive layers/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:37-39. A functional via (conductive via plug 27), a dummy via (reinforcing plug 28), and the second interconnect (conductive layer 26) are simultaneously formed in corresponding recesses in the first insulating film using a dual damascene process. *Id.*, ¶¶[0101], [0106]-[0109], Figs. 7-8.

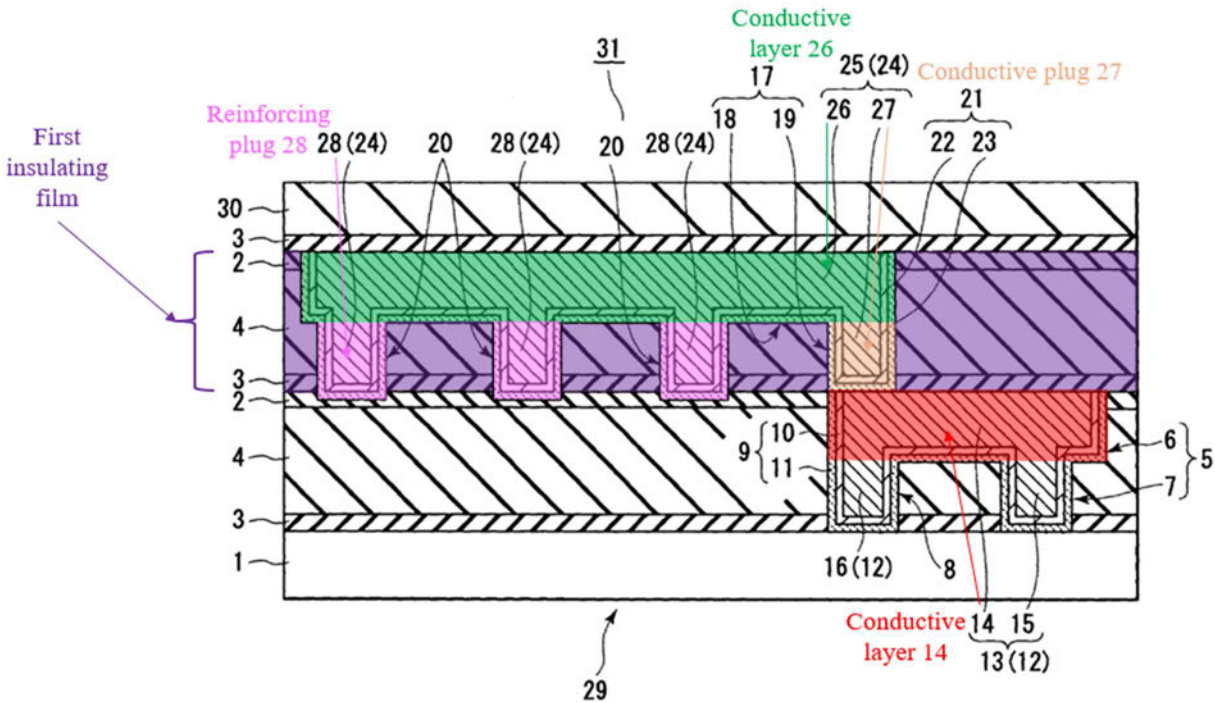


FIG. 8

72. Regarding, the dual damascene process, Hasunuma describes forming the recess for the Cu conductive layer 18 (second interconnect) and the recess for the Cu conductive via plug 19 (functional via) together within recess 17, and explicitly forms the recess for the first reinforcing plug 20 (dummy via) “integrally with the recess 18” for the second interconnect. All these recesses (17 and 20) are then filled simultaneously with the same barrier metal film 21 (including Ta film 22 and TaN film 23) and Cu film 24. TSMC-1004, Fig. 4, [0101]-[0103], [0105]-[0108].

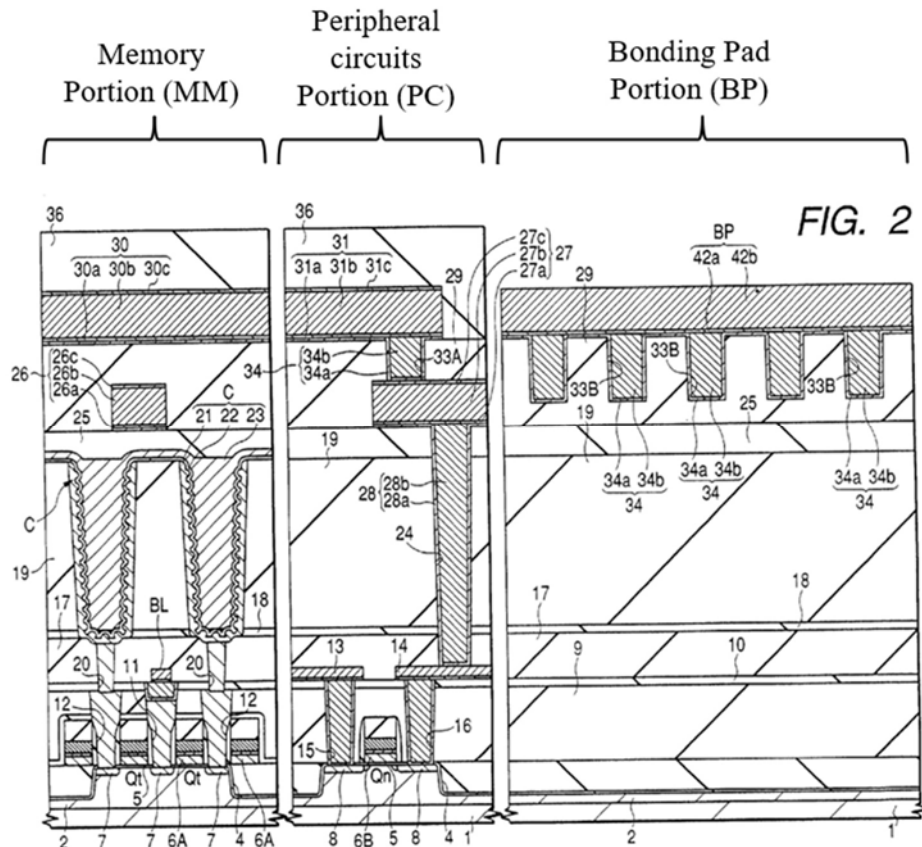
73. Both the '751 patent and Hasunuma address reliability problems arising from stresses inherent in interconnect structures. TSMC-1004, [0079]-[0086];

TSMC-1001, 2:23-40. Hasunuma's solution for mitigating these stress-related issues, similar to the '751 patent, involves incorporating the non-functional, concurrently formed Cu first reinforcing plug 28 (dummy via) adjacent to the functional Cu conductive via plug 27 (functional via) to address these stresses, although with the express intent to reinforce/strengthen the structure rather than absorb vacancies as in the '751 patent. *See* TSMC-1005, ¶[0114].

74. Because Hasunuma is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 Patent purports to address (e.g., interconnect reliability), Hasunuma is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1005, ¶¶[0003], [0005], [0079]-[0086].

C. Aoyagi – U.S. Patent App. Pub. No. 2001/0019180 (TSMC-1006)

75. Aoyagi discloses in Figures 2-12 and 19, and their supporting description, a method of fabricating a semiconductor device and the resulting device. More specifically, Figure 2 discloses a memory portion, peripheral circuit portion, and bonding pad forming region:



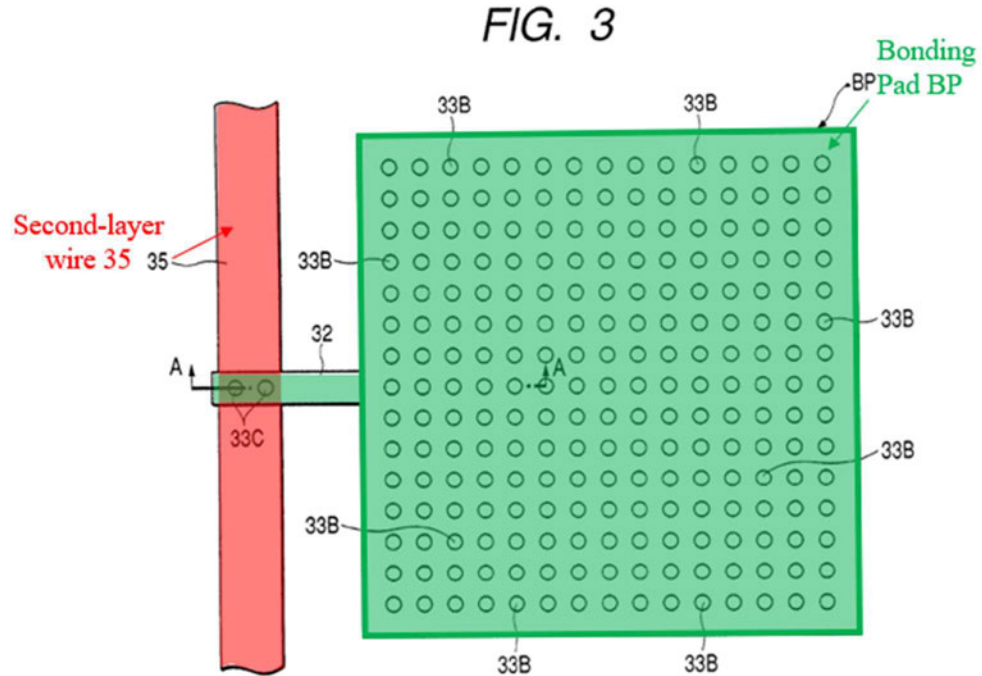
TSMC-1006, ¶¶[0038]-[0039].

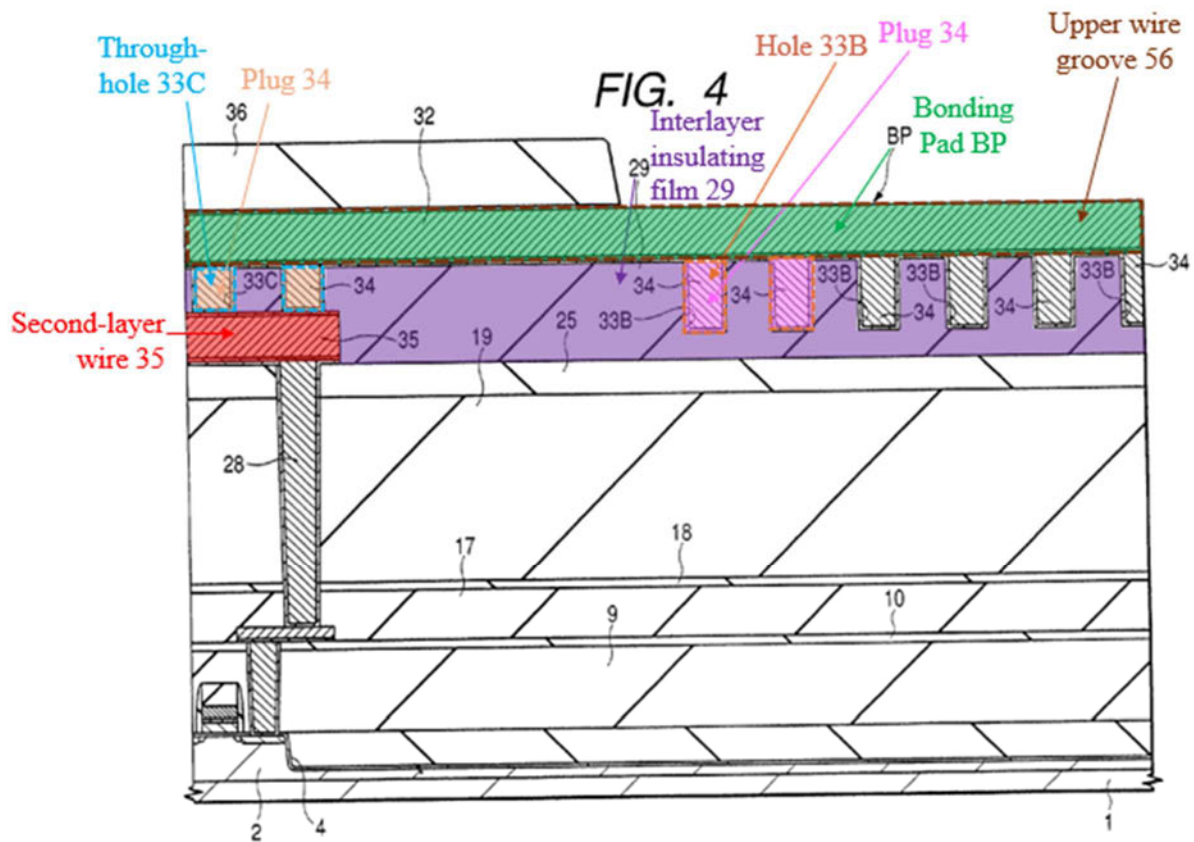
76. Figures 3 and 4 disclose the bonding pad region and a lead wire 32 from one end of the bonding pad and connecting to a second-layer wire 35. *Id.*, ¶[0055]. A POSITA would understand the bonding pad and Aoyagi's various "wires" to be "interconnects." Indeed, throughout Aoyagi, its interconnects are described using the term "wire" or "bonding pad" (e.g., "first-layer wire," "second-layer wire," "third-layer wire," "bonding pad BP"). A POSITA understood that such wires and bonding pad BP of Aoyagi constitute "interconnects" as those terms are understood in the art because both Aoyagi's wires and bonding pad BP are structures formed of

conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:21-28. Wires/bonding pads/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:37-39. Figures 5-12 disclose a manufacturing process, and Figure 19 shows using dual damascene method for wiring formation that is applicable to the device shown in Figures 2-4. The method includes: (i) forming second-layer wire 35 on substrate 1, (ii) forming insulating film 29 on second-layer wire 35, (iii) forming via holes 33A, 33C, dummy via holes 33B, and upper wire groove 56 in insulating film 29, and (iv) depositing conductive material into holes 33A, 33B, 33C and into groove 56, thereby forming vias 34 (in holes 33A, 33C), dummy vias 34 (in holes 33B), and third-layer wire 31/bonding pad BP¹ in upper wire groove 56. TSMC-1006, ¶¶[0050]-[0055], [0077], [0079]. Aoyagi's dummy vias 34 (in holes 33B) are for promoting adhesion between bonding pad BP and

¹ As demonstrated by Figures 3-4, “bonding pad BP” and “lead wire 32” together form a single, integral component, and as such discussion of “bonding pad BP” herein is generally intended to include “lead wire 32” unless specified otherwise. *See* TSMC-1006, Figs. 3-4.

insulating film 29, not for operational current flow to underlying layers. TSMC-1006, ¶¶[0050]-[0055], [0079].

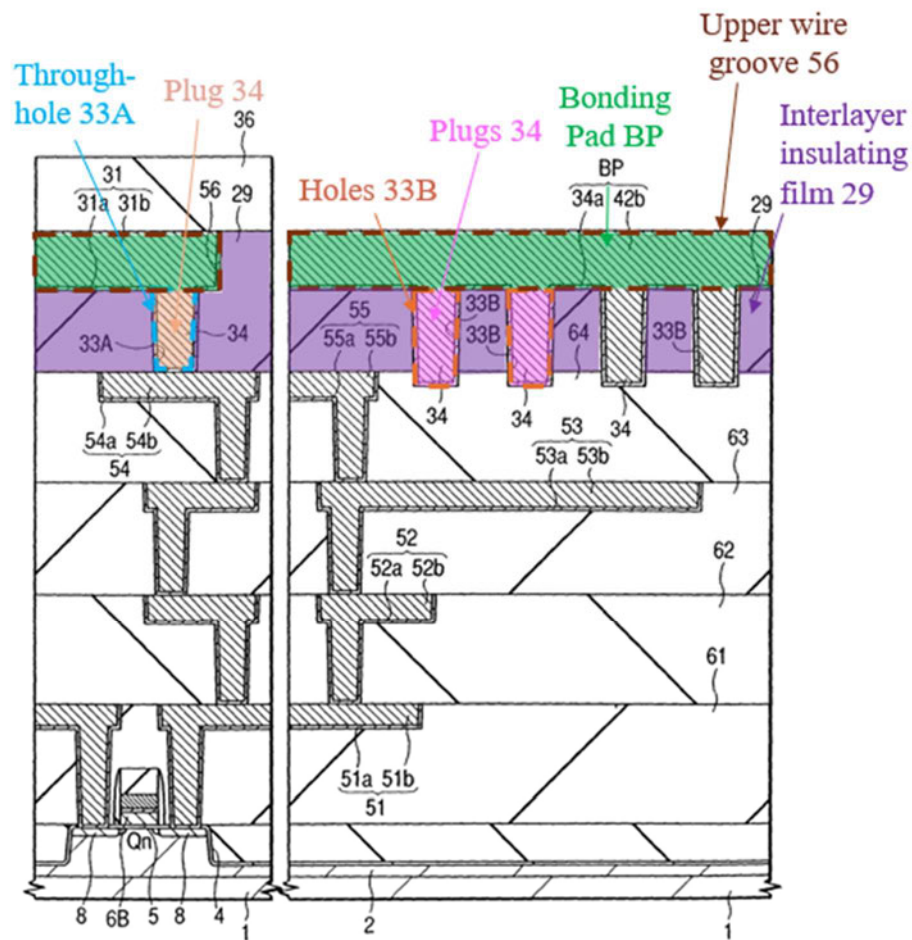




77. By their labeling and the depictions in the figures, the “second-layer” wires 26, 27, and 35 are formed at the same level, in the same insulating film 29 in Figures 2-4. Further, third-layer wires 30, 31 are formed over the insulating film 29. *Id.*, ¶[0050]. The bonding pad is formed “by use of the wire formed in the same step as the third-layer wires 30, 31.” *Id.*, ¶[0051]. In the case of dual damascene, as shown in Figure 19 and discussed below, second-layer wires are formed into the insulating film that is underneath the insulating film 29, and the third-layer wires such as third-layer wire 31, which includes the bonding pad BP, are formed in the insulating film 29. *Id.*, ¶[0077].

78. Aoyagi's Figure 19 teaches using the dual damascene process for interconnect/via fabrication, noting that "upper wire 31 (*including the bonding pad BP*)" may be formed by depositing conductive material into holes 33A, 33B and wire groove 56. TSMC-1006, ¶[0077], Fig. 19. As described above, this dual damascene process applies equally to forming the interconnects (e.g., second-layer wire 35 and third-layer wire 31 that includes bonding pad BP) and the functional and dummy vias (e.g., plugs 34 in holes 33C, 33B) of Figures 3-4.

FIG. 19



79. Additionally, given Aoyagi's discussion of using a dual damascene process to form wire 31/bonding pad BP and to deposit conductive material in holes 33A and 33B and upper wire groove 56, a POSITA would have found it obvious to use the dual damascene process to form bonding pad BP/lead wire 32 and the vias formed in through-holes 33C in the structure of Figures 3-4. A POSITA would have been motivated to use the dual damascene process in order to increase efficiency and reduce costs of manufacturing as was well-known at the time. The nature of and advantages associated with dual damascene were well understood in the art. See, e.g., TSMC-1019, 146-147 (stating that dual damascene enhances density and performance and promotes reliability and improves manufacturability, including manufacturing yield); TSMC-1027, 25 (noting dual damascene forms Cu wires and vias with one metal fill and one CMP step, providing process simplification allowing for reduced cost and improved manufacturability); TSMC-1028, 5458 (discussing that, with making one level of lines and one level of vias together, can build more levels of Cu interconnects with same number of processing steps); *see also* TSMC-1034, 583-84, 671-76, 718, 723-26. Additionally, a POSITA could have easily implemented such a process given its already disclosed use in Aoyagi and its widespread use in industry at the time. *See* TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-147; TSMC-1034, 583-84, 671-76, 718, 723-26.

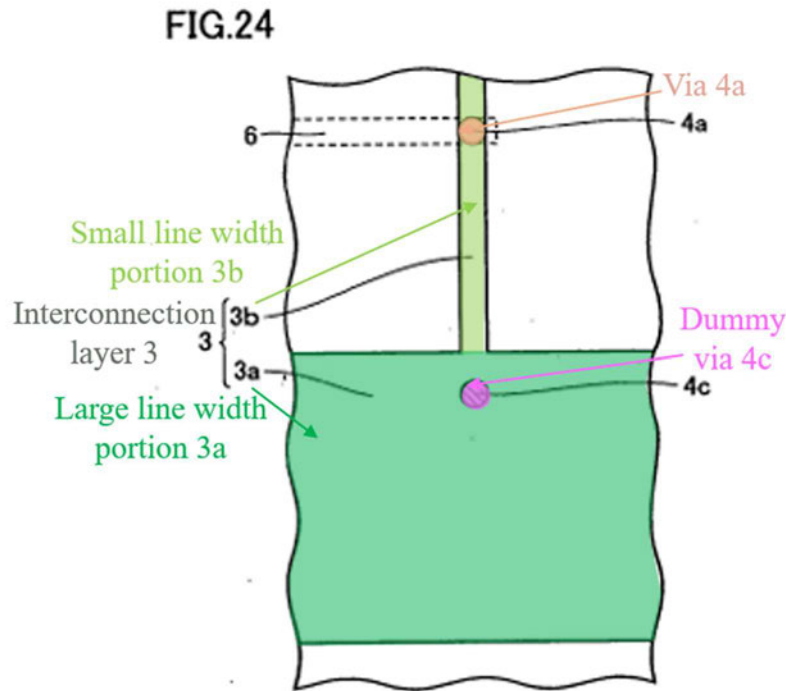
80. Because Aoyagi is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 Patent purports to address (e.g., interconnect reliability), Aoyagi is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1006, Abstract, ¶¶[0001], [0004], [0005].

D. Kamoshima – U.S. Patent App. Pub. No. 2004/0173905 (TSMC-1009)

81. Kamoshima discloses interconnection structures for semiconductor devices that “suppress concentration of voids in an interconnection under a via due to stress migration.” TSMC-1009, ¶¶[0002], [0008]. Kamoshima uses dummy vias so that microvoids in interconnection layer 3 are distributed between a via and dummy via, to suppress the concentration of microvoids in the area under the via. TSMC-1009, ¶¶[0088], [0097]-[0098].

82. Kamoshima forms an interconnection layer 3 by depositing conductive material (e.g., “barrier metal layer 2,” “copper layer 3”) in an interconnect trench (e.g., “groove 1a”) formed in “insulating layer 1.” TSMC-1009, ¶¶[0043]-[0044]. The interconnection layer 3 can have different shapes, with Figure 15 disclosing a constant width interconnection layer 3, and Figures 23-27 disclosing interconnection layer 3 having a first interconnection portion with a small line width 3b branching off a second interconnection portion with a large line width 3a. *See id.*, ¶¶[0094]-[0103], Figs. 23-27. Kamoshima teaches arranging via 4a (for connection to another

interconnect layer) along small line width portion 3b and arranging dummy via 4c in the vicinity of a “connection portion” between interconnection portions. *Id.*, ¶¶[0095], [0099]. Annotated Figure 24 discloses these features:



83. Kamoshima employs multiple trench portions (e.g., “groove 1a,” “groove 1b”) to form the interconnection portions with different widths. *See id.*, ¶[0062] (groove 1a for interconnection with small line width and groove 1b for interconnection with large line width); *see also id.*, ¶¶[0068]-[0069], Figs. 8-9.

84. Because Kamoshima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the ’751 Patent purports to address (e.g., interconnect reliability), Kamoshima is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1009, ¶¶[0002], [0004]-[0007].

E. Iizuka – U.S. Patent No. 5,250,465 (TSMC-1008)

85. Like the '751 patent, Iizuka describes methods for manufacturing semiconductor devices, specifically focused on improving the filling of small diameter via-holes (e.g., not greater than 0.6 μm) to form reliable conductive plugs between interconnect layers. TSMC-1008, Abstract, 1:7-14, 2:39-45. Iizuka explicitly acknowledges that via-holes can have various planar configurations, stating: “It will also be understood that the opening of the via-hole may have any configuration, such as a square, rectangle or circle.” *Id.*, 9:44-47. A POSITA would have understood this teaching in Iizuka to refer to the shape of the via-hole viewed in plan view (i.e., from above) or as a cross-section, which then dictates the shape of the resulting via when the via-hole is filled (typically with a conductive metal such as aluminum or copper). Furthermore, Iizuka’s Example 1 discloses a via-hole 6 having a “diameter” of 0.5 μm (EX1008, 6:60-63), which a POSITA would have understood as disclosing and resulting in a via with a circular shape (*see also id.*, Fig. 5A (showing a circular via)). Iizuka demonstrates that circular, square, and rectangular vias were known and interchangeable design alternatives, thereby teaching obvious via-shape alternatives for similar prior art structures. *Id.*, 9:41-47.

86. Because Iizuka is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 Patent purports to address (e.g.,

interconnect reliability), Iizuka is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1008, 1:7-14; 2:39-45.

F. Kurashima – U.S. Patent No. 7,042,099 (TSMC-1011)

87. Kurashima enhances durability of insulating films, particularly low-relative-dielectric-constant films, against Chemical Mechanical Polishing (CMP) stresses to prevent film peeling in multi-layered wiring structures. TSMC-1011, 1:15-22, 1:49-67. In its first embodiment (Figs. 1A-1D, 2A-2C, 3A-3B), Kurashima teaches forming in parallel a Cu-wire 9 and a Cu-dummy wire 10 in spaced-apart areas in a first layer interlayer insulating film 4. *Id.*, 4:50-6:32, Figs. 1B-1D, 3A-3B. Then a second-layer Cu-wire 16 is formed connecting to the first-layer Cu-wire 9. *Id.*, 6:58-8:35, Figs. 2A-3A. Concurrently, a second-layer Cu-dummy wire 17 is formed in contact with first-layer Cu-dummy wire 10, providing a reinforcing effect and enhancing interfacial adhesion and CMP durability, thereby reducing peeling of layers during CMP. *Id.*, 6:11-32; 6:58-8:54, 9:16-23, Figs. 2C, 3A. Kurashima teaches forming functional wires and dummy wires with substantially the same width within the same layer. *Id.*, 4:50-63, Figs. 1D, 3A, 3B. Annotated Figure 3A discloses these features, where each feature is colored to include barrier metal film 7:

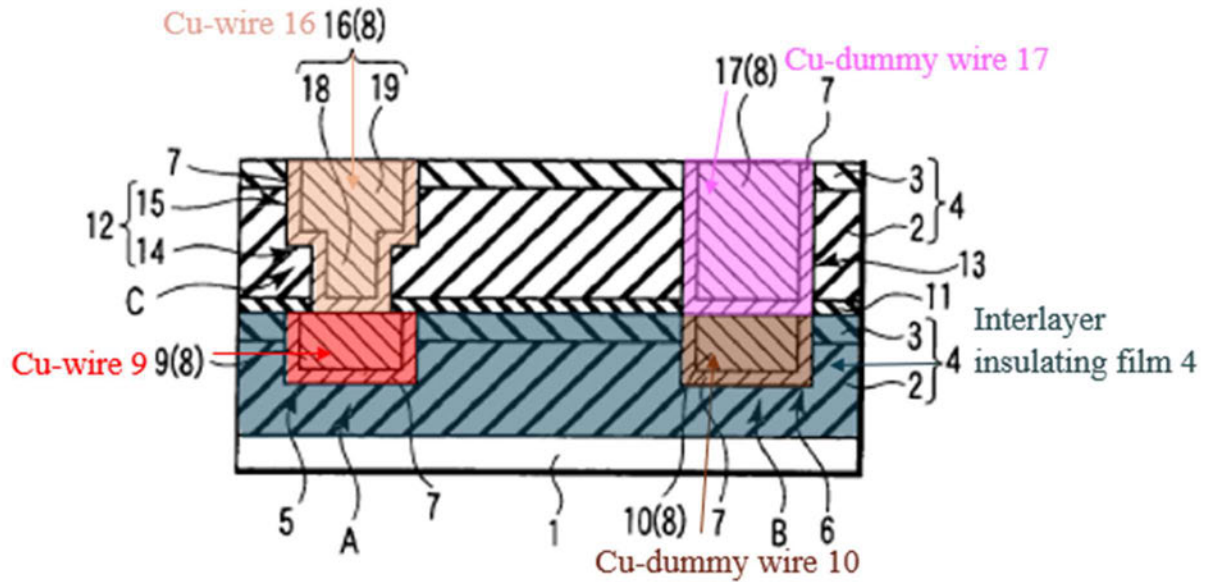


FIG. 3A

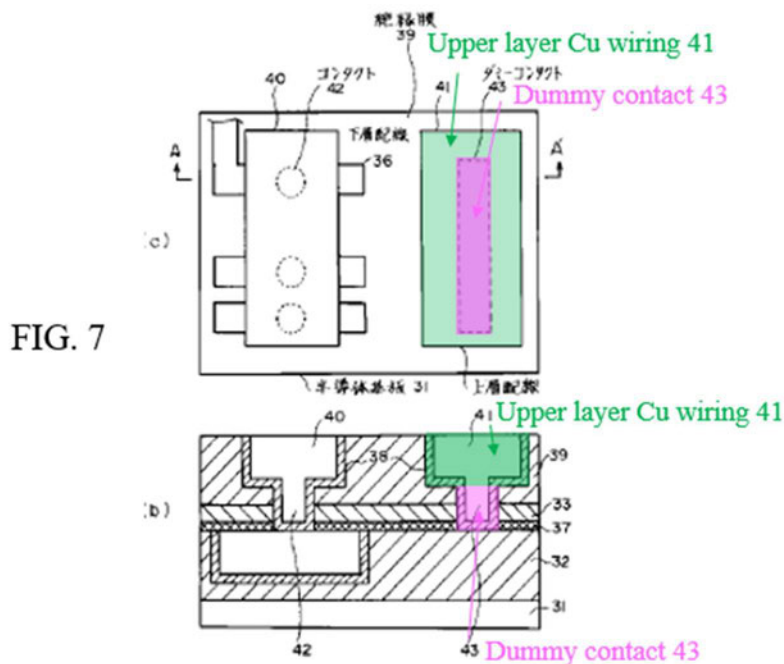
88. Because Kurashima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 Patent purports to address (e.g., interconnect reliability), Kurashima is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1011, 1:16-22 and 49-67.

G. Fukazawa – JP2002299437 (TSMC-1010)

89. Fukazawa is directed to a method for manufacturing a semiconductor device, including for forming Cu wiring embedded in a low-dielectric constant insulating film. TSMC-1010, ¶[0001]. Fukazawa discloses a dummy contact 43, which is a dummy via, connected to an upper layer interconnect (e.g., “upper layer Cu wiring 41”), and not connected to a lower layer interconnect. TSMC-1010, ¶[0017], Fig. 7. To enhance mechanical strength, Fukazawa’s dummy contact 43 is arranged in a substantially rectangular shape (described as “column-shaped”) in a

plan view, shown in Fig. 7. *Id.*, ¶¶[0017]-[0018] (“the dummy contacts are column-shaped”), Fig. 7.

90. Fukazawa discloses a longer side of a dummy via and a longer side of a first interconnect portion are provided along a same direction in Figure 7 where a longer side of the dummy contact/via 43 extends along a same direction as a longer side of a corresponding rectangular interconnect (“upper layer Cu wiring 41”). *Id.*



91. Fukazawa teaches that, with such structure, the mechanical strength is sufficiently secured even when the insulating film is peeled off, so that the strength of the wiring structure is improved. *Id.*, ¶[0018]. Thus, Fukazawa demonstrates that it was known and provides a motivation for having a rectangularly-shaped dummy

via as well as positioning such a rectangular via such that its long side is parallel to a long side of an interconnect to which the via is connected.

92. Because Fukazawa is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '751 Patent purports to address (e.g., interconnect reliability), Fukazawa is analogous art. TSMC-1001, 1:15-16, 2:41-45; TSMC-1010, Abstract, ¶¶[0001], [0004]-[0007].

X. CLAIMS 1-20 ARE UNPATENTABLE

93. In my opinion, claims 1-20 are unpatentable as explained below for the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A/1B	1-2, 5-8, 10-13, 18, 20	102/103	Watanabe
2	3-4, 15-16	103	Watanabe, Kamoshima
3	17	103	Watanabe, Kamoshima, Fukazawa
4	9	103	Watanabe, Iizuka
5	1, 5-6, 9, 11-14, 18-19	102	Hasunuma
6	2, 20	103	Hasunuma, Kurashima
7	2, 8, 10	103	Hasunuma, Watanabe
8	1, 3-4, 7, 14-16, 19	103	Aoyagi
9	17	103	Aoyagi, Fukazawa

A. GROUNDS 1A/1B: Watanabe anticipates (Ground 1A) and renders obvious (Ground 1B) Claims 1-2, 5-8, 10-13, 18, and 20

94. I believe Watanabe discloses as well as renders obvious each element of Claims 1-2, 5-8, 10-13, 18, and 20 as discussed below.

1. Claim 1

1[pre] “A Method for Fabricating a Semiconductor Device”

95. The preamble of claim 1 calls for a “method of fabricating a semiconductor device.” Watanabe discloses this preamble, as it “relates to a semiconductor device and, more particularly, to a semiconductor device manufactured by the damascene process.” TSMC-1004, ¶[0003]; *see also id.*, Abstract, ¶¶[0049], [0134]-[0173], Fig. 14. A POSITA would understand that this is a “method for fabricating a semiconductor device.”

96. Watanabe discloses multiple semiconductor device embodiments all formed using claim 1’s method, including:

- a “first embodiment” in Figures 1-2 (*see* ¶¶[0059]-[0087]);
- a “second embodiment” in Figures 3-4 (*see* ¶¶[0088]-[0092]);
- a “third embodiment” in Figures 5A-5C (*see* ¶¶[0093]-[0108]);
- a “fourth embodiment” in Figures 6-7 (*see* ¶¶[0109]-[0114]); and

- a “fifth embodiment”² in Figures 8-11 (*see* ¶¶[0115]-[0133]).

See, e.g., TSMC-1004, ¶¶[0038]-[0049], [0171]-[0181] (discussing Fig. 14).

97. Specifically, in describing Figures 12A-12N, Watanabe teaches a “method of manufacturing the semiconductor device **according to the embodiments of the present invention.**”³ *Id.*, ¶¶[0049], [0072], [0134]-[0170]; *see also id.* ¶¶[0172]-[0173] (explaining that the semiconductor devices shown in more detail in Figure 14 are included in “layer 20” of the disclosed embodiments). Moreover, the first through fifth embodiments use common reference numerals as depicted in Figures 12A-12N. *See id.*, ¶[0089]; *compare* Figs. 12A-12N to Figs. 1-9. A POSITA would thus readily understand that the manufacturing process

² Watanabe’s fifth embodiment includes a three-level interconnect structure that satisfies claim 1 in multiple ways. TSMC-1004, ¶¶[0115]-[0133]. First, Watanabe’s fifth embodiment (Figures 8-9) includes a similar lower layer, first level interconnect structure as Watanabe’s first embodiment (Figures 1-2). This is a first mapping of Watanabe’s fifth embodiment and satisfies claim 1 for the same reasons presented below for the first embodiment. Because the following discussions of Watanabe’s first embodiment apply equally to this first mapping of the fifth embodiment, this first mapping of the fifth embodiment is not discussed separately. Under a second mapping, Watanabe’s fifth embodiment meets claim 1 based on its second and third level interconnect structures. All discussions of Watanabe’s fifth embodiment below apply this second mapping.

³ All emphases throughout this declaration are added.

disclosed in Figures 12A-12N applies to manufacturing the semiconductor devices in all five embodiments. Moreover, Watanabe discloses in introducing Figure 14 that the method can be repeated to obtain any number of wirings. *Id.*, ¶[0171]; *see also id.*, ¶¶[0172]-[0173].

98. Additionally, a POSITA would have found it obvious to use the dual damascene method of manufacturing of Figs. 12A-12N to create respective wiring layers for any of the embodiments of Watanabe. A POSITA would have been motivated to do so by the well-known benefits associated with the dual damascene process, which include increased manufacturing simplicity and efficiency (afforded by forming the vias and interconnects simultaneously rather than serially), the resulting reduced cost, and a reduced risk of electromigration failure. *See* TSMC-1034, 583-84, 671-76, 695, 698, 718, 723-26; TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-151; TSMC-1027, 25; TSMC-1028; 5458-59.

99. Indeed, the nature of and advantages associated with dual damascene were well understood in the art. *See, e.g.*, TSMC-1019, 146-147 (stating that dual damascene enhances density and performance and promotes reliability and improves manufacturability, including manufacturing yield); TSMC-1027, 25 (noting dual damascene forms Cu wires and vias with one metal fill and one CMP step, providing process simplification allowing for reduced cost and improved manufacturability);

TSMC-1028, 5458 (discussing that, with making one level of lines and one level of vias together, can build more levels of Cu interconnects with same number of processing steps). Regarding simplified and more efficient manufacturing, a POSITA was aware that: “The dual-damascene process offers the advantage of reducing the number of process steps” (TSMC-1034, 673); “The reduction in the number of processing steps is another of the benefits that have driven the development of dual-damascene processes” (*id.*, 676). The foregoing benefits are easily recognized when compared to other manufacturing process (e.g., single damascene) where interconnect trenches and vias are independently formed one step at a time, a much more time consuming and thus oftentimes expensive process.

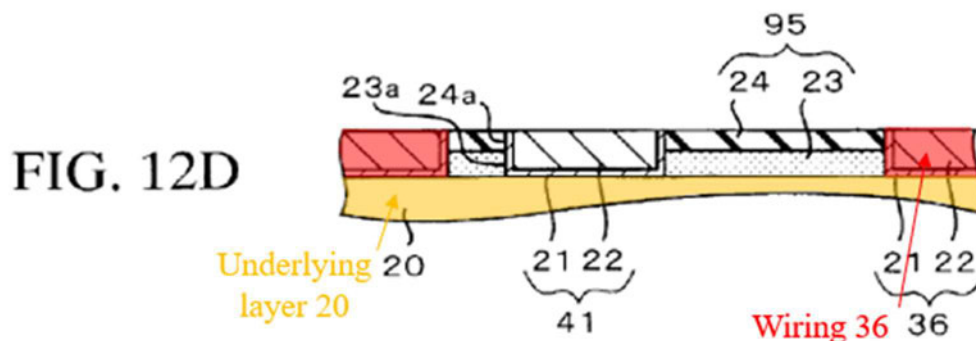
100. A POSITA would have further recognized that use of the dual damascene process in this manner could have been easily implemented given its already disclosed use in Watanabe and its general widespread use in industry at the time as widely recognized in the various contemporary references discussed above. *See also* TSMC-1015, 3:63-4:22; TSMC-1034, 583-84, 671-76, 718, 723-26 (explaining development, implementation, and advantages of the dual-damascene process); *supra*, §VI(A).

1[a] “Forming a First Interconnect”

101. Element 1[a] calls for “forming a first interconnect on a semiconductor substrate,” which Watanabe discloses.

Watanabe – Embodiments 1-3

102. Watanabe's Figs. 12A-12D teach forming a first interconnect (e.g., "first wiring 36") on a semiconductor substate (e.g., "underlying layer 20" or, alternatively, a semiconductor substrate included as part of "underlying layer 20"). TSMC-1004, ¶¶[0059]-[0061], [0136]-[0148], [0172]-[0174], Figs. 12A-12D; *see also id.*, Fig. 14. Thereafter, Watanabe teaches depositing a "barrier metal layer 21" and "copper film 22" on the underlying layer 20, followed by chemical mechanical polishing ("CMP"), to thereby form "first wiring 36" (i.e., "a first interconnect"). *See* TSMC-1004, ¶¶[0142]-[0144] ("as shown in FIG. 12C, the barrier metal layer 21...is formed on the overall exposed surface.... Then, the copper film 22 is formed on this barrier metal layer 21.... The residual copper film 22 and the barrier metal layer 21 constitute the first wiring 36...."), Figs. 12C-12D. Annotated Fig. 12D discloses these features:



103. For the first and second embodiments, Figures 1 and 3 (annotated below) each disclose “first wiring 36” formed on “underlying layer 20”:

FIG. 1

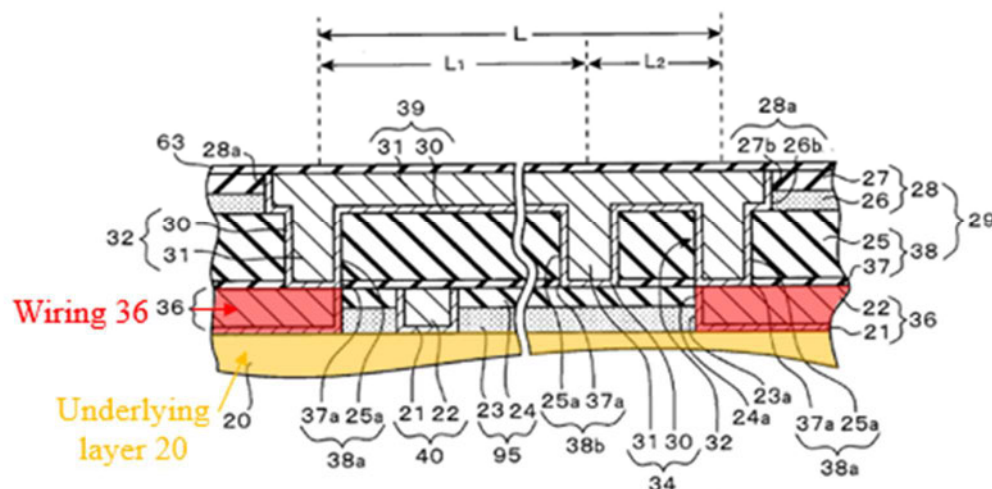
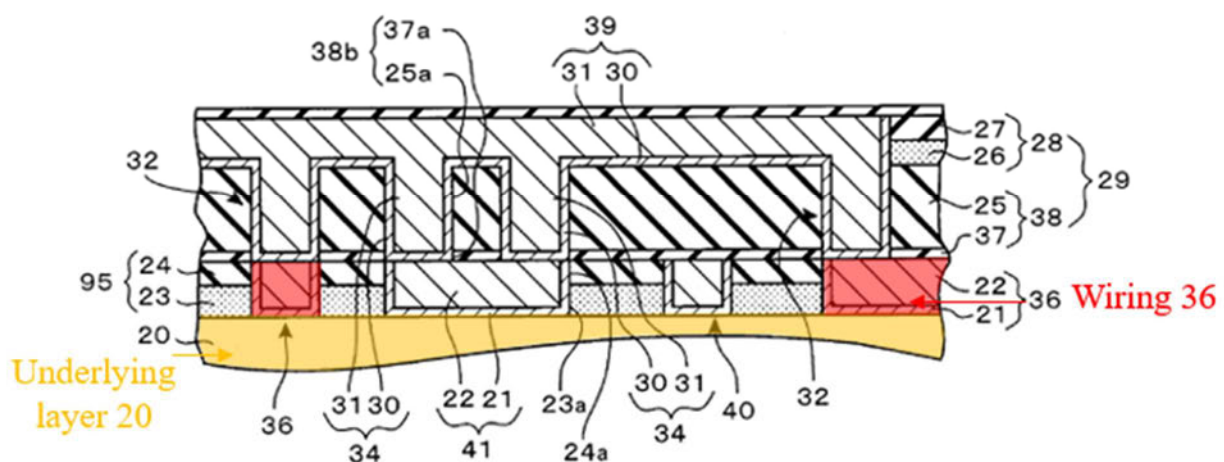


FIG. 3



Figures 5A-5C disclose a top-down view of a third embodiment also having a first wiring 36, with Watanabe explaining that the “underlying layer 20” (referencing

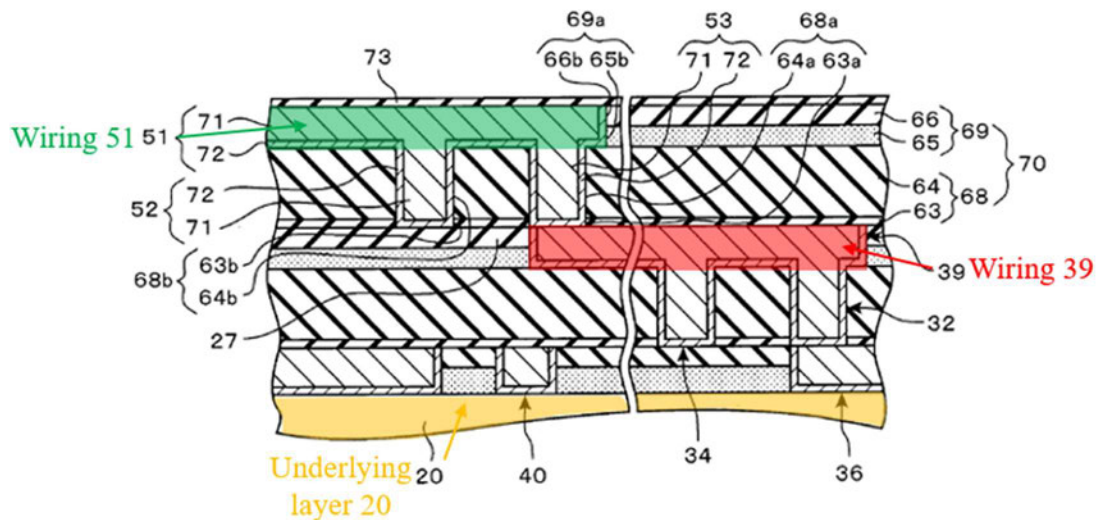
Figs. 1 and 3) and “insulating films” are intentionally omitted. TSMC-1004, ¶[0094]. A POSITA would understand that “first wiring 36” in Figures 5A-5C is likewise formed on a semiconductor substrate such as “underlying layer 20” (or, alternatively, a semiconductor substrate therein), as with the embodiments in Figs. 1 and 3. Watanabe describes its interconnects using the term “wiring” (e.g., “wiring 36,” “wiring 39,” “wiring 51”). A POSITA understood that such wirings constitute “interconnects” as those terms are understood in the art because a wiring is a structure formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.,* TSMC-1001, 1:21-28. Wiring/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:37-39.

Watanabe – Embodiment 5

104. Regarding Watanabe’s fifth embodiment shown in Figures 8-9, Watanabe discloses forming additional interconnects (e.g., “second wiring 39,” “third wiring 51”) on layer 20, which includes a semiconductor substate. TSMC-1004, ¶¶[0116]-[0117], [0059]-[0062], [0136]-[0148], Figs. 8-9; *see also id.*, Fig.

14. For purposes of claim 1, Figure 8 (annotated) discloses the wiring 39 is a “first interconnect” that is formed on “underlying layer 20” (semiconductor substrate):

FIG. 8



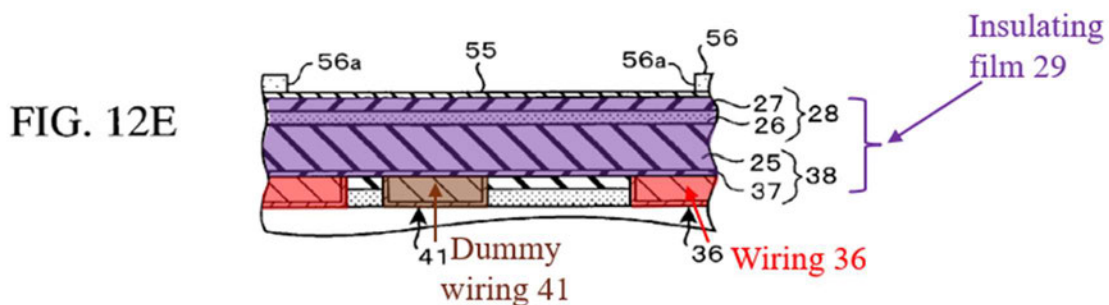
1[b] “Forming a First Insulating Film”

105. Element 1[b] calls for “forming a first insulating film on the first interconnect,” which Watanabe discloses.

Embodiments 1-3

106. Watanabe discloses forming a first insulating film (e.g., “insulating film 29,” which is a combination of “lower insulating film 38” and “upper insulating film 28”) on the first interconnect (e.g., “first wiring 36”). TSMC-1004, ¶¶[0066], [0149]-[0152], Figs. 12E, 1, 3. “The first wiring 36 is covered with the second insulating film 29. The second insulating film 29 is constituted by laminating a lower

insulating film 38 and an upper insulating film 28.” TSMC-1004, ¶[0066]. “Lower insulating film 38” includes a “silicon oxide film 25” formed on a “silicon nitride film 37,” and “upper insulating film 28” includes a “low-dielectric insulating film 26” and a “silicon oxide film 27.” *Id.* With reference to Fig. 12E (annotated below), Watanabe explains “the silicon nitride film 37...is formed to cover the first wiring 36 and the dummy wiring 41.... Then, the silicon oxide film 25...is formed on the silicon nitride film 37.... Then, the low-dielectric insulating film 26..., the silicon oxide film 27..., and a metal film 55 are laminated on the silicon oxide film 25. The upper insulating film 28 is constructed by the low-dielectric insulating film 26 and the silicon oxide film 27.” *Id.*, ¶¶[0149]-[0151].



107. For the first and second embodiments, Figures 1 and 3 (annotated below) disclose insulating film 29 (including both lower insulating film 38 and upper insulating film 28) formed on the first wiring 36:

FIG. 1

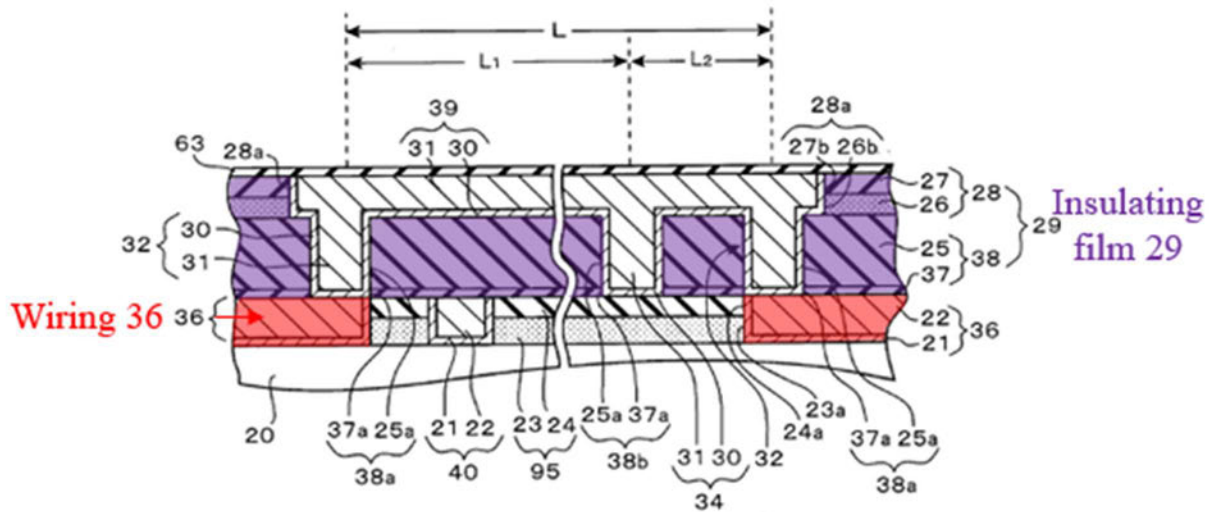
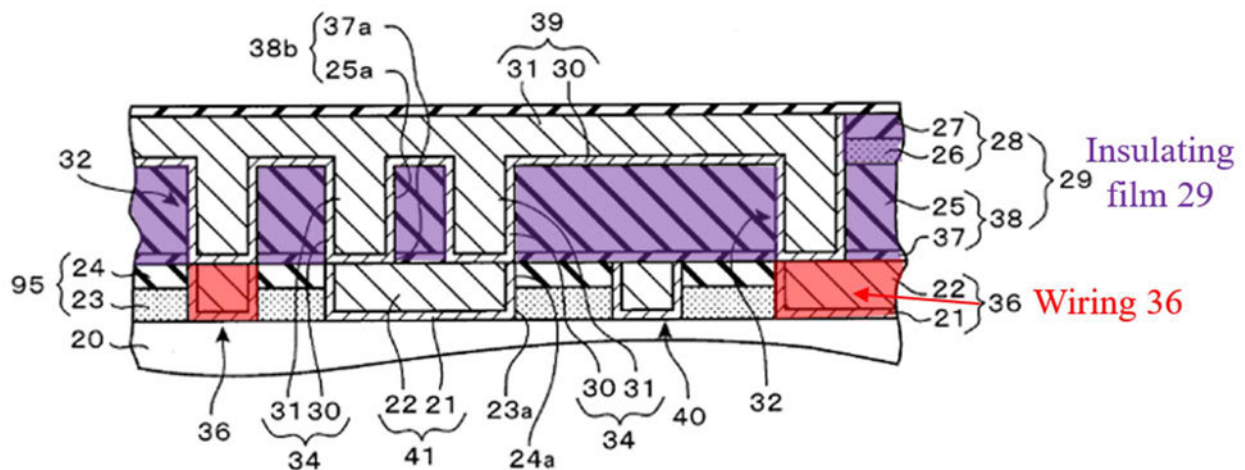


FIG. 3

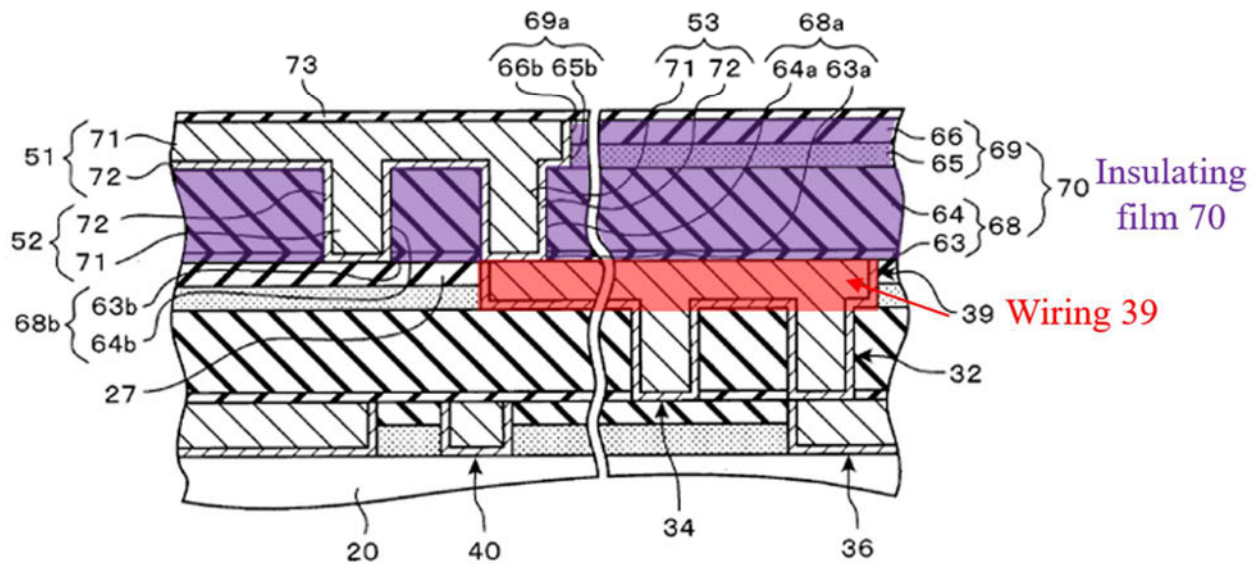


108. For the third embodiment (Figures 5A-5C), Watanabe intentionally omits depicting the underlying layer 20 and insulating films, while referencing Figures 1 and 3. *Id.*, ¶[0094]. As understood by a POSITA, the third embodiment forms an insulating film on the first interconnect following the first and second embodiments.

Embodiment 5

109. Regarding Watanabe's fifth embodiment (Figures 8-9), Watanabe discloses forming a first insulating film (e.g., "insulating film 70," which is a combination of "lower insulating film 68" and "upper insulating film 69," or any one or more constituent layers of "insulating film 70") on the first interconnect (e.g., "second wiring 39"). TSMC-1004, ¶¶[0119]-[0120], [0123], Fig. 8; *see also id.*, Fig. 14. Watanabe explains "insulating film 70 is constructed by the lower insulating film 68 and the upper insulating film 69." TSMC-1004, ¶[0123]. "Lower insulating film 68" includes "silicon nitride film 63" and "silicon oxide film 64" and "upper insulating film 69" includes "low-dielectric insulating film 65" and "silicon oxide film 66." TSMC-1004, ¶¶[0118]-[0120]. Figure 8 (annotated) discloses these features:

FIG. 8



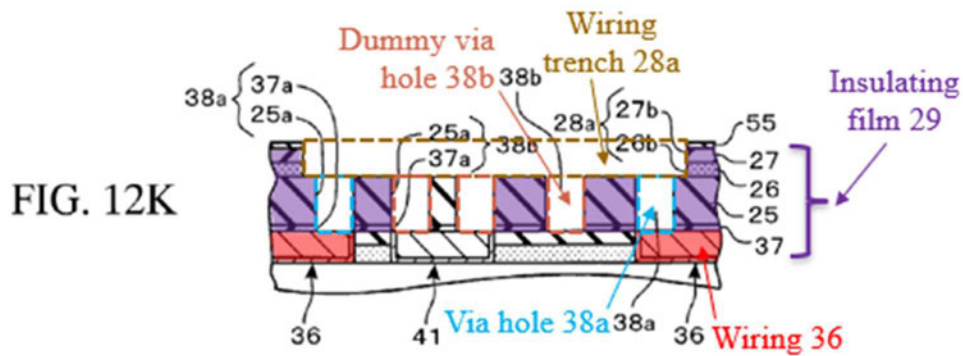
1[c] “Forming in the First Insulating Film, a Via Hole, a Dummy Hole and an Interconnect Trench”

110. Element 1[c] calls for “forming in the first insulating film, a via hole connected to the first interconnect, a dummy hole which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench connected to the via hole and the dummy hole.” Watanabe discloses forming each of these structures in the first insulating film for each of Embodiments 1-3 and 5.

Embodiments 1-3

111. Watanabe discloses forming in the first insulating film (e.g., “insulating film 29”), a via hole (e.g., “via hole 38a”) connected to the first interconnect (e.g.,

“first wiring 36”), a dummy hole (e.g., “dummy via hole 38b”) which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench (e.g., “wiring trench 28a”) connected to the via hole and the dummy hole. TSMC-1004, ¶¶[0067], [0159]-[0165], Figs. 12J-12K. Figure 12K (annotated below) discloses these components:



112. For example, Watanabe states that “silicon nitride film 37 is etched by using the silicon oxide film 25 as an etching gas. The openings 25a in the silicon oxide film 25 are transferred onto the silicon nitride film 37 and thus the openings 37a are formed in the silicon nitride film 37.” TSMC-1004, ¶[0162]. Thus, “formations of the via holes 38a, the dummy via holes 38b, and the wiring trench 28a are completed. The wiring trench 28a is constructed by the openings 27b and 26b. While, the via hole 38 a and the dummy via hole 38b are each constructed by the openings 25a and 37a. The via holes 38a are formed to extend from the wiring trench 28a to the first wiring 36. Then, the dummy via holes 38b may be formed to

reach the nonforming region of the first wiring 36 or reach the dummy wiring 41.”

Id., ¶¶[0164]-[0165]; *see also id.*, ¶¶[0067], [0079].

113. The same process is used to form the via hole (e.g., “via hole 38a”), dummy hole (e.g., “dummy via hole 38b”), and interconnect trench (e.g., “wiring trench 28a”) in each of embodiments 1-3. *See* TSMC-1004, ¶[0135] (“FIGS. 12A to 12N...show[] the method of manufacturing the semiconductor device according to the embodiments of the present invention.”). Figures 1 and 3 (annotated below) disclose via hole 38a, dummy via hole 38b, and wiring trench 28a:

FIG. 1

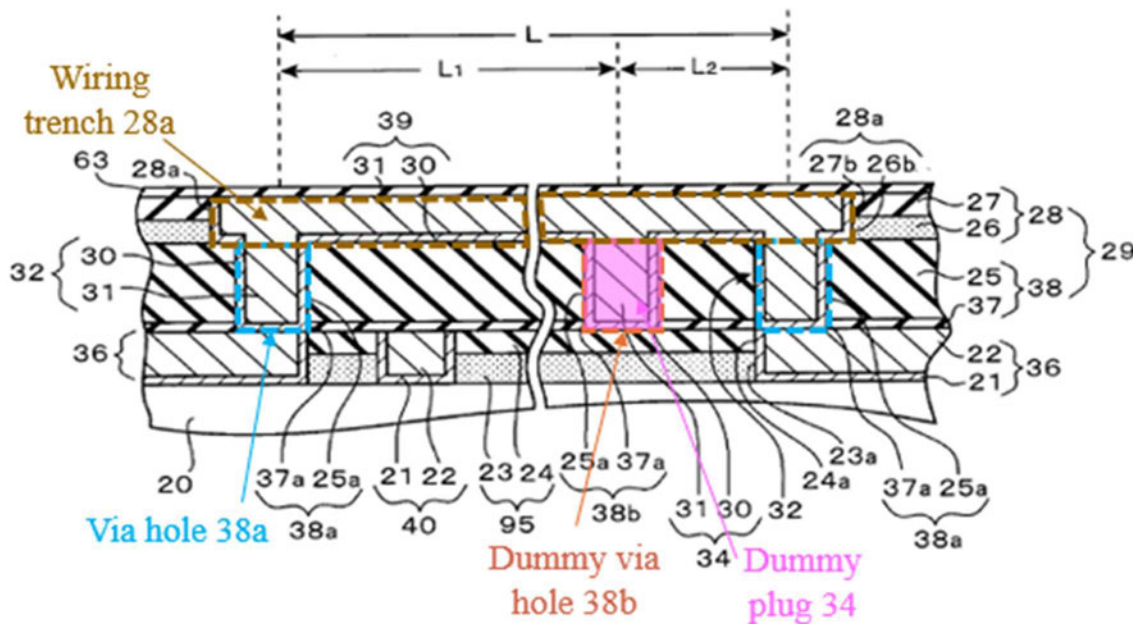
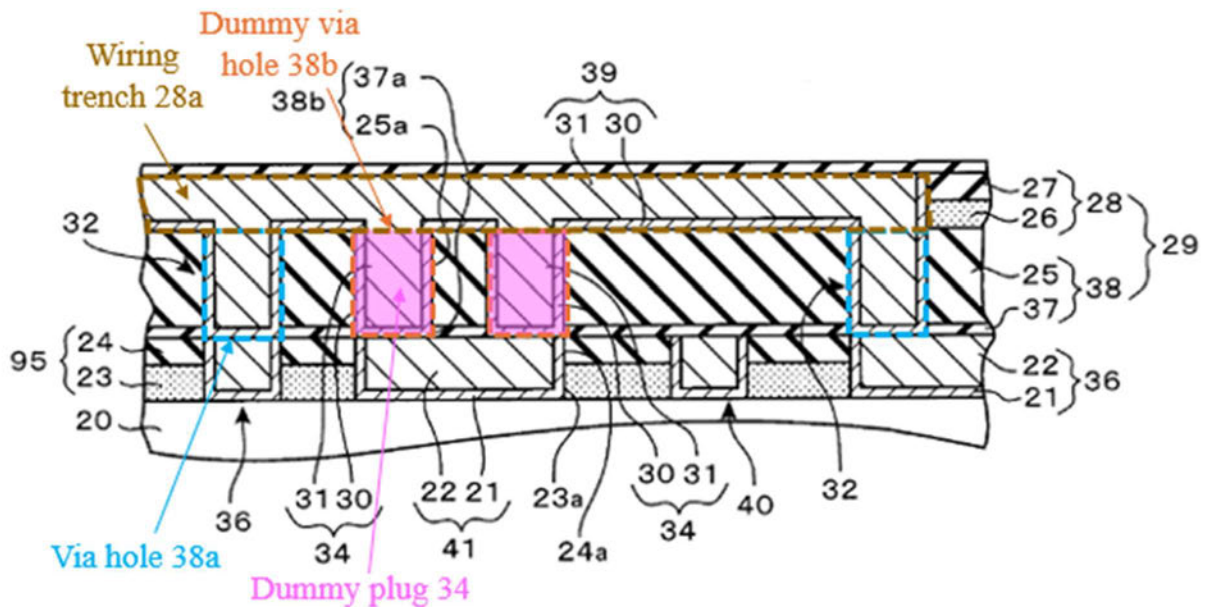


FIG. 3



114. As further outlined for limitation 1[d], following formation of via hole 38a, dummy via hole 38b, and wiring trench 28a, a second wiring 39 is formed, which includes a barrier metal layer 30 and a copper film 31, in the via hole 38a, dummy via hole 38b, and wiring trench 28a. *Infra*, §IX(A)(1[d]). The portion of second wiring 39 in the dummy via hole 38b serves as a dummy conductive plug 34.

115. A POSITA would understand that “dummy via holes 38b” and “dummy plugs 34” are “arranged so as to be incapable of having current flow therethrough.” In this regard, the ’751 patent specification states:

A dummy via and a dummy interconnect herein means a pseudo via or a pseudo interconnect which do not constitute a closed circuit in actual use of a device with an interconnection structure including these via and

interconnect (i.e., no current flows therein during actual use of the device.)

TSMC-1001, 3:17-21. The '751 patent goes on to explain that:

[N]either the dummy interconnect 102B nor the dummy via 110B constitutes a closed circuit in actual use. That is, *even if the dummy interconnect 102B and the dummy via 110B are omitted* in the interconnection structure shown in FIG. 2B, *a device with this interconnection structure is operable at least immediately after fabrication.*

Id., 10:42-48.

116. As understood by a POSITA, in Watanabe, the “dummy” via holes 38b and “dummy” plugs 34 do not constitute part of a closed circuit in actual use of the device, i.e., no current flows therein during actual use of the device. As illustrated in Figures 1 and 3, these “dummy” via holes 38b and “dummy” plugs 34 are only connected on one end to an active circuit element (i.e., “second wiring 39”), while the other end is not connected to a second active circuit element (it instead ends at insulating film 95). In the Figure 3 embodiment, dummy interconnect 41 does not have current flow therethrough. Figure 14 shows the same general configuration, plus additional dummy plugs 52 similarly connected to the third wiring 51 immediately above. A POSITA would recognize that no current can flow through

Watanabe's dummy via holes 38b or dummy plugs 34 (or 52) due to the lack of connection to a second active circuit element.

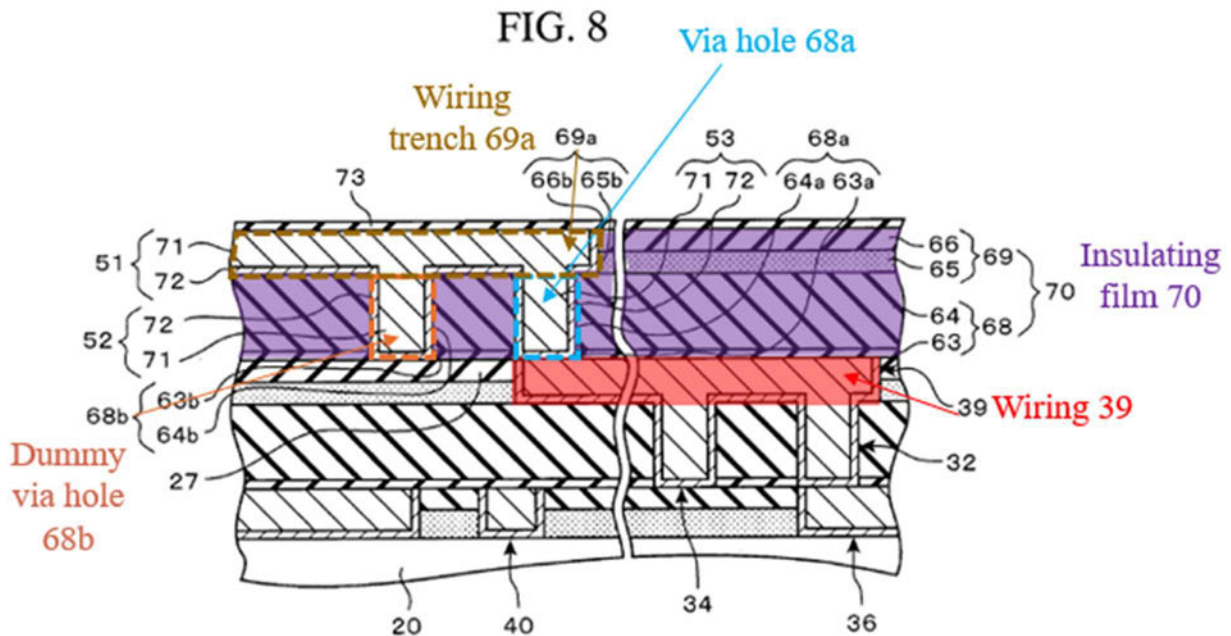
117. Instead, current flows between Watanabe's first wiring 39 and second wiring 39 through conductive plugs 32 (formed in via holes 38a), which constitute parts of a closed circuit during device operation. *See* TSMC-1004, ¶[0073]. Moreover, consistent with the '751 patent's description of dummy via and dummy interconnect, Watanabe's device would still be operable if dummy via holes 38b and dummy plugs 34 were omitted, where current would still flow through the active circuit elements, i.e., first and second wirings 36 and 39 and via plugs 32, during actual use of the device.

118. Thus, in addition to Watanabe describing holes 38b as "dummy" holes, a POSITA would have understood that they are "arranged so as to be incapable of having current flow" as claimed due to their lack of current-carrying function and because the semiconductor device would still function even if the dummy holes 38b were omitted.

Embodiment 5

119. Based on Watanabe's statement that Figures 12A-12N disclose the manufacturing method for the embodiments and common reference numerals for the fifth embodiment semiconductor device, a POSITA would recognize that the same manufacturing process is used for the fifth embodiment of Watanabe to form the via

hole, dummy hole, and interconnect components associated with the added third wiring layer. *See* TSMC-1004, ¶[0117]. Specifically, Watanabe discloses forming in the first insulating film (e.g., “insulating film 70”), a via hole (e.g., “via hole 68a”) connected to the first interconnect (e.g., “second wiring 39”), a dummy hole (e.g., “dummy via hole 68b”) which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench (e.g., “wiring trench 69a”) connected to the via hole and the dummy hole. TSMC-1004, ¶¶[0118]-[0121], [0159]-[0165], Fig. 8. Annotated Figure 8 discloses these features:



120. For the same reasons as dummy via holes 38b, dummy via holes 68b are likewise incapable of current flow.

1[d] “Depositing a Conductive Material in the Via Hole, the Dummy Hole and the Interconnect Trench”

121. Element 1[d] calls for “depositing a conductive material in the via hole, the dummy hole and the interconnect trench, thereby forming a via, a dummy via and a second interconnect.” Each of Watanabe’s embodiments 1-3 and 5 discloses this limitation.

Embodiments 1-3

122. Watanabe discloses depositing a conductive material (e.g., “copper film 31,” “barrier metal layer 30”) in the via hole (e.g., “via hole 38a”), the dummy hole (e.g., “dummy via hole 38b”) and the interconnect trench (e.g., “wiring trench 28a”), thereby forming a via (e.g., “conductive plug 32”), a dummy via (e.g., “dummy plug 34”) and a second interconnect (e.g., “second wiring 39”). TSMC-1004, ¶¶[0166]-[0169], [0068]-[0072], Figs. 12L-12N, Figs. 1, 3. See Annotated Figures 12M-12N below:

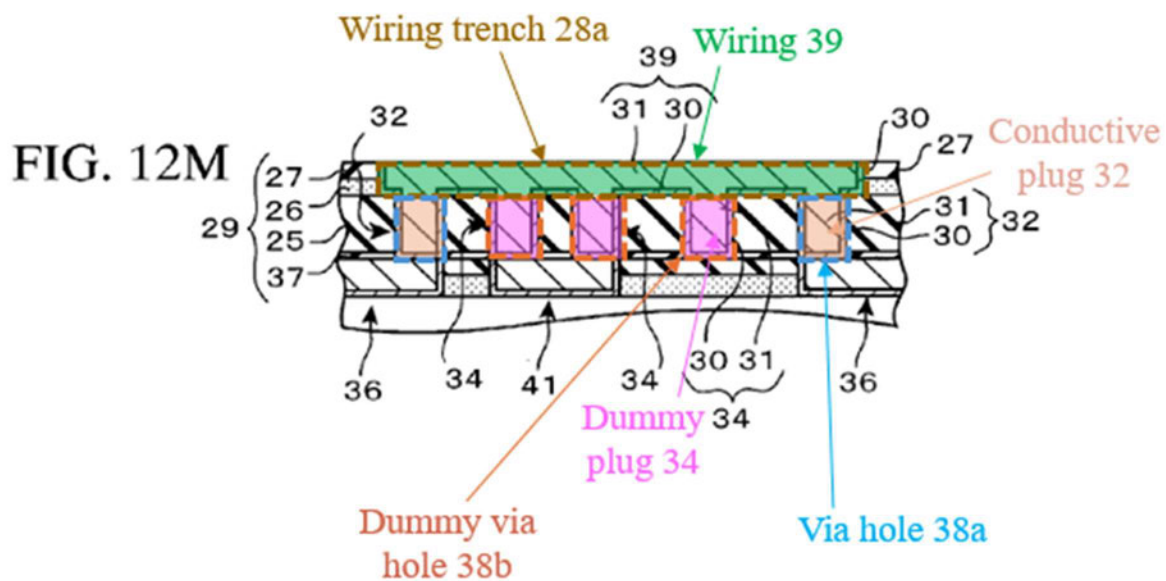
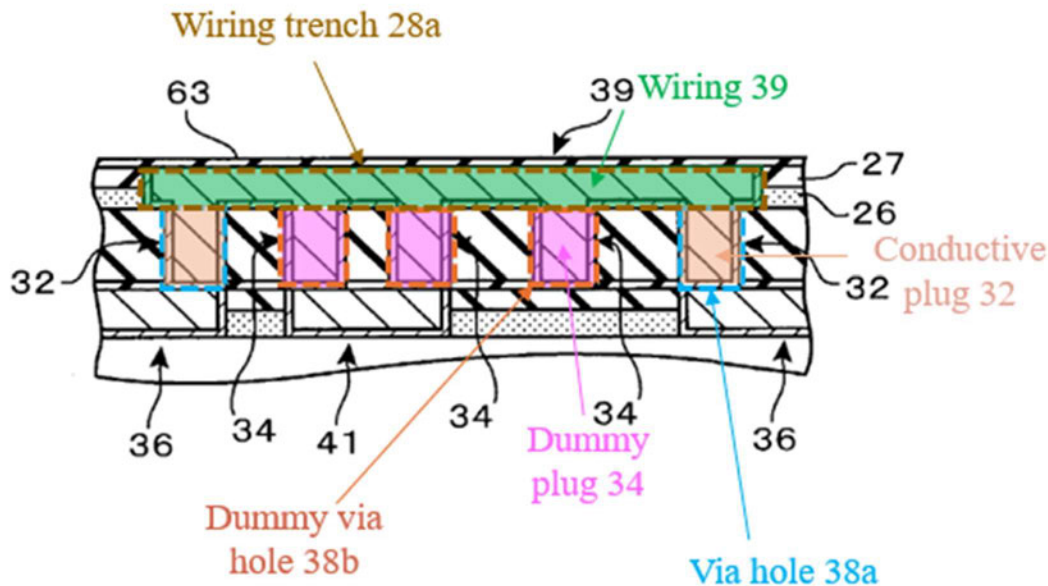


FIG. 12N



123. “The forming areas of the barrier metal layer 30 are on the metal film 55, inner walls of the wiring trench 28a, inner walls (including bottom surfaces) of the via holes 38a, and inner walls (including bottom surfaces) of the dummy via holes 38b.... Then, the copper film 31...is formed on the barrier metal layer 30 by the sputtering.” TSMC-1004, ¶[0168]. “The **barrier metal layer 30 and the copper film 31**, which are not polished and left behind, **constitute the second wiring 39**. Then, the **portion of the second wiring 39, which is buried in the via hole 38a, is served as the plug, and the portion of the second wiring 39, which is buried in the dummy via hole 38b, is served as the dummy plug.**” *Id.*

124. Figures 1, 3, and 5 each disclose the via (e.g., “conductive plug 32”), dummy via (e.g., “dummy plug 34”), and second interconnect (e.g., “second wiring 39”). See TSMC-1004, ¶[0135] (“FIGS. 12A to 12N...show[] the method of

manufacturing the semiconductor device according to the embodiments of the present invention.”).

Embodiment 5

125. For the fifth embodiment, Watanabe provides a third wiring 51 above the second wiring 39. A POSITA would recognize that the process of Figures 12A-12N is used in the fifth embodiment of Watanabe to form the via (e.g., “conductive plug 53”), dummy via (e.g., “dummy plug 52”), and second interconnect (e.g., “third wiring 51”) associated with the third wiring layer. *See* TSMC-1004, ¶[0117]. Specifically, Watanabe discloses depositing a conductive material (e.g., “copper film 71,” “barrier metal layer 72”) in the via hole (e.g., “via hole 68a”), the dummy hole (e.g., “dummy via hole 68b”) and the interconnect trench (e.g., “wiring trench 69a”), thereby forming a via (e.g., “conductive plug 53”), a dummy via (e.g., “dummy plug 52”) and a second interconnect (e.g., “third wiring 51”) as shown below in annotated Figures 8 and 9 (appreciating that I have only highlighted some exemplary dummy plugs 52 in Figure 9 below). TSMC-1004, ¶¶[0117]-[0122], [0166]-[0170], Figs. 8-9.

FIG. 8

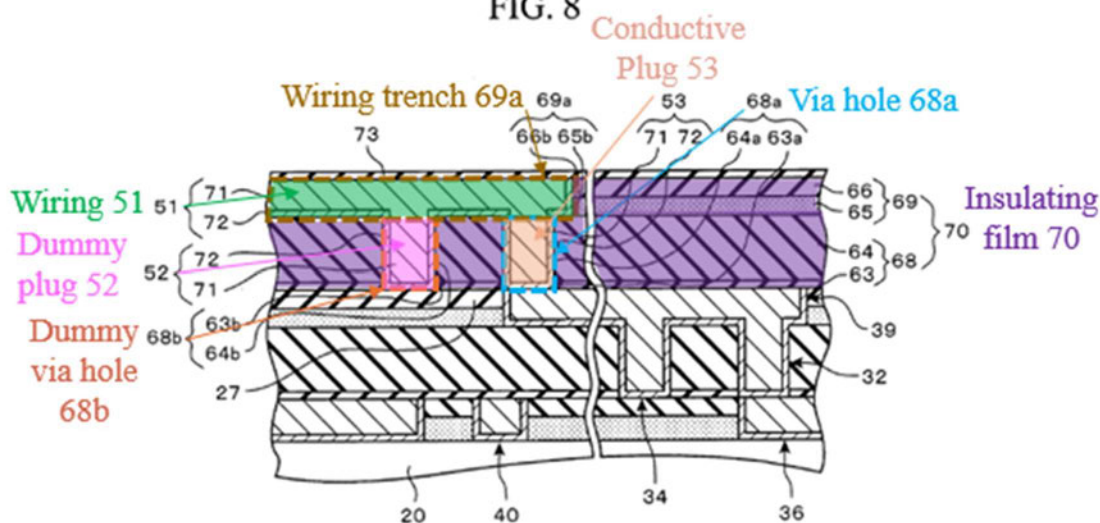
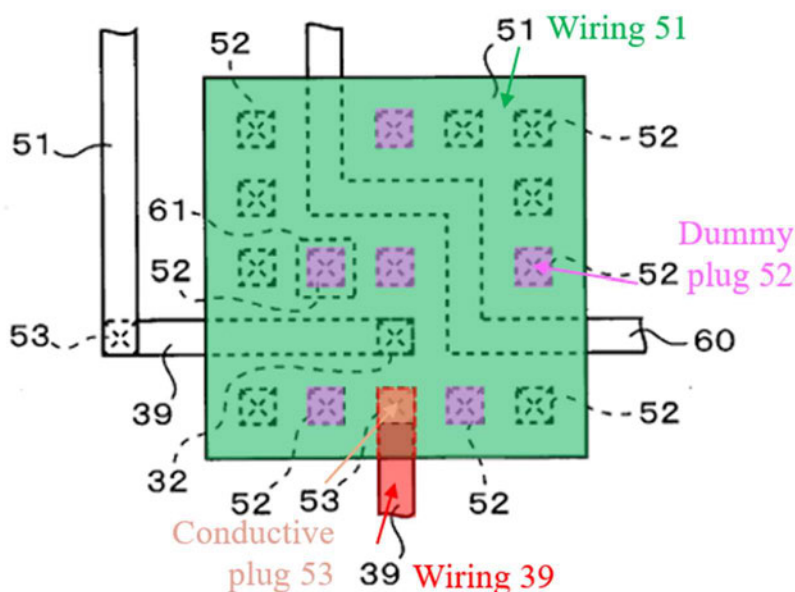


FIG. 9



126. Thus, Watanabe discloses limitation 1[d]. Accordingly, Watanabe discloses all limitations of and thus anticipates claim 1 for the disclosed method of manufacturing as applied to at least each of Embodiments 1-3 and 5.

2. Claim 2

127. At least Watanabe's second and fifth embodiments meet claim 2.

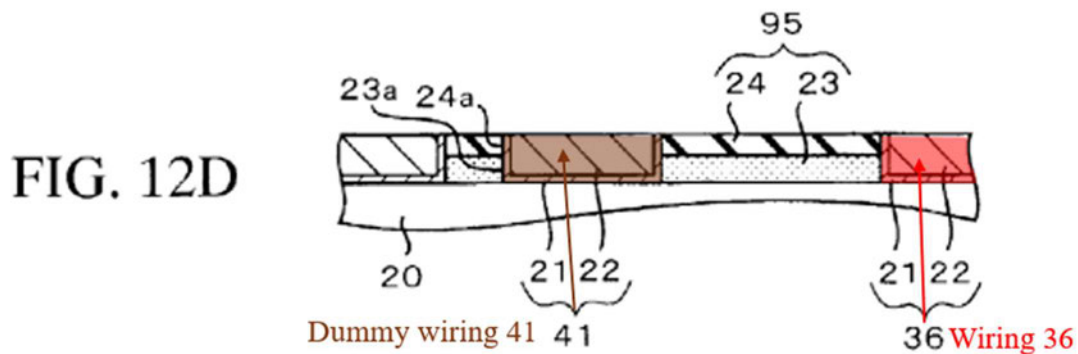
[2a] The method of claim 1, wherein in the step (a) a first dummy interconnect is simultaneously formed on the semiconductor substrate, and

128. Element 2[a] recites that “in the step (a) a first dummy interconnect is simultaneously formed on the semiconductor substrate.”

129. For its second embodiment, Watanabe discloses that in step (a) a first dummy interconnect (e.g., “dummy wiring 41”) is simultaneously formed on the semiconductor substrate. TSMC-1004, ¶¶[0059]-[0061], [0089]-[0091], [0136]-[0148], Figs. 12A-12D, 3; *see also id.*, Fig. 14. A POSITA would understand that “dummy wiring 41” is a “dummy interconnect” both because of its description as a “dummy” and its structure, which is consistent with the ’751 patent’s description of a “dummy interconnect.” *See supra*, §X(A)(1)(1[c]). Specifically, a POSITA would recognize that dummy wiring 41 does not constitute part of a closed circuit during actual use of the device, i.e., no current flows therein during use, and Watanabe’s device would still be operable if dummy wiring 41 was omitted. As discussed previously, the purpose of Watanabe’s dummy wiring 41 is merely to add additional structural support/strength to the overall device, not to serve as active circuitry or otherwise conduct current flow. Indeed, Watanabe states that “as shown in FIG. 3, a dummy wiring 41 is provided ***in the non-forming region*** of the first wiring 36,”

further demonstrating to a POSITA that the dummy wiring cannot pass current. *See* TSMC-1004, ¶[0090].

130. In connection with Figures 12C-12D, Watanabe discloses depositing barrier metal layer 21 and copper film 22, and then planarizing the copper film 22, such that the “residual copper film 22 and the barrier metal layer 21 constitute the first wiring 36 and the dummy wiring 41.” TSMC-1004, ¶[0144], Figs. 12A-12D.

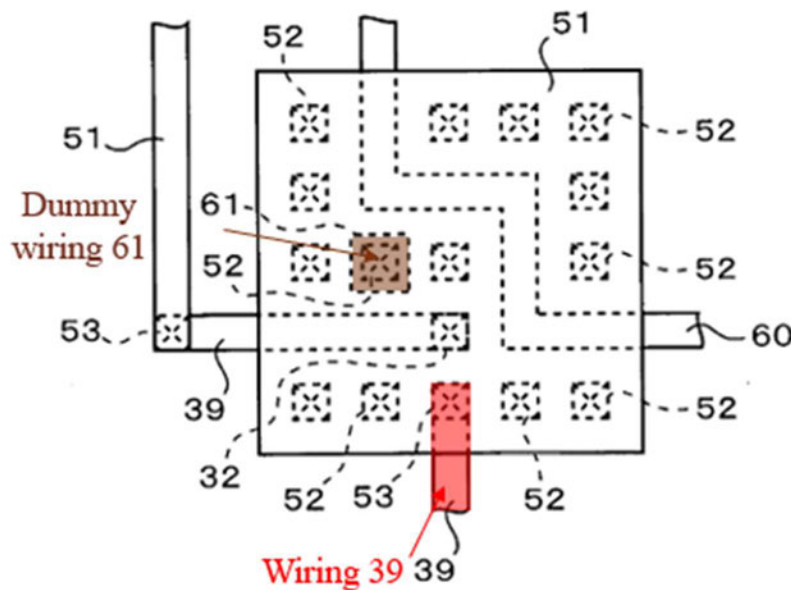


131. Thus, at least given that they are formed from the same material in the same step and at the same time, a POSITA would understand that “dummy wiring 41” is formed simultaneously with “first wiring 36,” satisfying limitation 2[a].

132. The same process is used in Watanabe’s fifth embodiment to simultaneously form a first dummy interconnect (e.g., “dummy wiring 61”) with third wiring layer 39 on the semiconductor substrate (“underlying layer 20”). *See* TSMC-1004, [0127], Fig. 9. “Dummy wiring 61” is “**formed in the same layer as the second wiring 39.**” The dummy plug 52 may be connected to this dummy wiring 61. If they are connected in this manner, the mechanical strength of the laminated

body consisting of the silicon oxide film 64 (see FIG. 8) and the third wiring 51 can be enhanced by the same reason as the second embodiment.” TSMC-1004, [0127]. Thus, just like dummy wiring 41 and first wiring 36, dummy wiring 61 and second wiring 39 are formed in the same layer and, following Figs. 12A-12N for the third wiring, are formed simultaneously. *See id.*, Figs. 12A-12D for dummy interconnect (“dummy wiring 41”) and first interconnect (“first wiring 36”). Annotated Figure 9 discloses “dummy wiring 61” and “second wiring 39”:⁴

FIG. 9



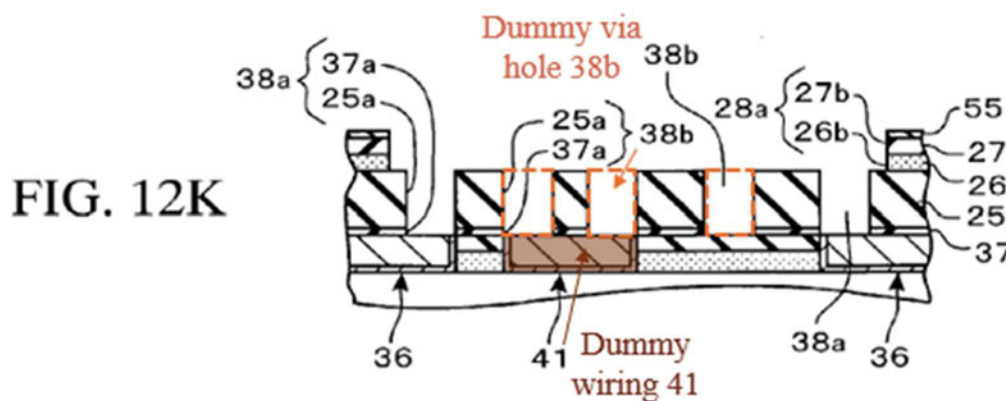
⁴ Figure 8 omits “dummy wiring 61,” apparently because of its optional nature or because it discloses a different cross-section that does not include dummy wiring 61.

133. Just like the “dummy wiring 41” and for the same reasons, a POSITA would understand that “dummy wiring 61” is a “dummy interconnect.” *Supra*, §X(A)(2)(2[a]).

134. Thus, each of at least Watanabe’s second and fifth embodiments satisfy limitation 2[a].

[2b] in the step (c) the dummy hole is connected to the first dummy interconnect.

135. For its second embodiment, Watanabe discloses that in step (c) the dummy hole (e.g., “dummy via hole 38b”) is connected to the first dummy interconnect (e.g., “dummy wiring 41”). Watanabe explains that “**dummy via holes 38b may be formed to reach...dummy wiring 41.**” TSMC-1004, ¶[0165], [0090], Figs. 12K-12N, 3. Dummy via holes 38b are connected to dummy wiring 41 via formation through “lower insulating film 38,” which occurs in step (c). *Supra*, §X(A)(1)(1[c]); TSMC-1004, ¶¶[0159]-[0165], [0090]-[0091], Figs. 12J-12K, 3.



136. The same process involving “step (c)” is further used in Watanabe’s fifth embodiment to connect the dummy hole (e.g., “dummy via hole 68b”) to the first dummy interconnect (e.g., “dummy wiring 61”). See TSMC-1004, ¶¶[0121]-[0122], [0127], Fig. 9.

137. For example, Watanabe’s “dummy via hole (dummy connection hole) [68b] is formed in the lower insulating film 68 to reach the non-forming region of the second wiring 39. Such dummy via hole 68b is constructed by openings 63b, 64b formed in the silicon nitride film 63 and the silicon oxide film 64.” TSMC-1004, ¶[0121]. In addition, Watanabe explains that the portion of the “third wiring 51, which is buried in the dummy via hole 68b, is called a dummy plug 52.” *Id.*, ¶[0122]. “The dummy plug 52 may be connected to...dummy wiring 61.” *Id.*, ¶[0127]. Thus, as understood by a POSITA, dummy via hole 68b is connected to the first dummy interconnect (“dummy wiring 61”).

138. Accordingly, each of at least Watanabe’s second and fifth embodiments satisfy limitation 2[b], and thus Watanabe anticipates claim 2.

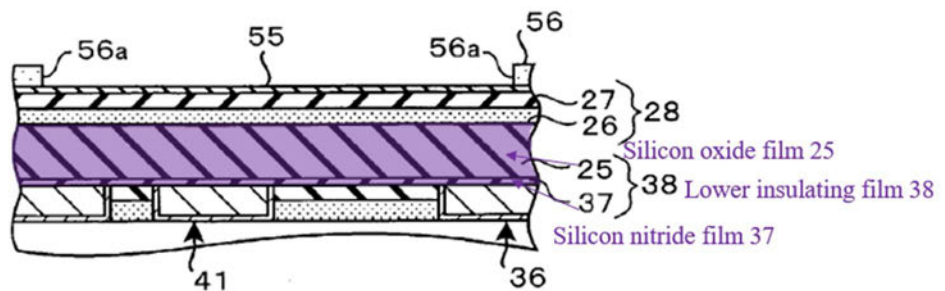
3. Claim 5 - *The method of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film.*

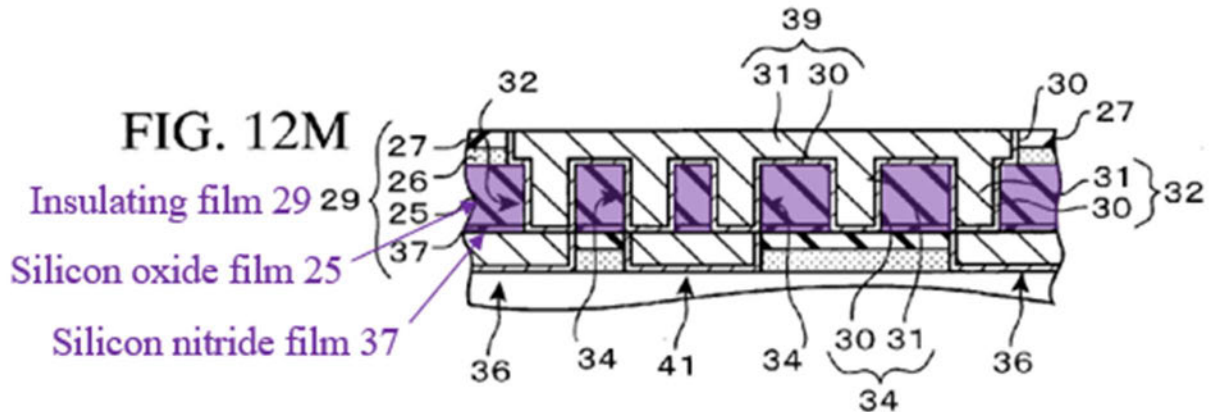
139. At least each of Watanabe’s first through third and fifth embodiments meet claim 5.

140. Claim 5 recites the “semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film,” which Watanabe discloses.

141. Watanabe's first insulating film (e.g., "insulating film 29" of the first through third embodiments (which includes "lower insulating film 38") and "insulating film 70" of the fifth embodiment (which includes "lower insulating film 68")) has a multilayer structure including a SiN film (e.g., "silicon nitride film 37," "silicon nitride film 63") and a SiO₂ film (e.g., "silicon oxide film 25," "silicon oxide film 64"). TSMC-1004, ¶¶[0066], [0119], [0150], [0184], Figs. 1, 3, 8, 12E. "The lower insulating film 38 is constructed by the silicon nitride film 37 and the remaining silicon oxide film 25." TSMC-1004, ¶[0150]. Similarly, "insulating film 68" includes "silicon nitride film 63" and "silicon oxide film 64." *Id.*, ¶[0119]. See annotated Figures 12E and 12M below:

FIG. 12E





A POSITA would have understood that “SiN” refers to “silicon nitride.” A POSITA would also have understood that “SiO₂” encompasses “silicon oxide” because “silicon oxide” is a common term of art used in this field to refer to SiO₂ films, or at least films comprising predominantly SiO₂. For example, in another contemporaneous patent of his, Watanabe’976⁵, Watanabe expressly equates “silicon nitride” to “SiN” and “silicon oxide” to “SiO₂.” TSMC-1022, 2:48-49 (describing “a silicon nitride (SiN) film” and “a silicon oxide (SiO₂) film”).

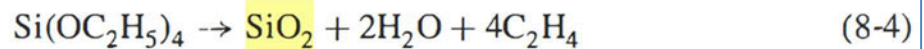
⁵ Watanabe’976 is directed to a semiconductor device and manufacturing method relating to the formation of vias/via holes to be formed through an insulating film on a wiring layer. TSMC-1022, 1:15-21. Because Watanabe’976 is in the same field (interconnection/wiring structures) and pertinent to a problem the ’623 patent purports to address (e.g., interconnect manufacture and reliability), Watanabe’976 is analogous art. TSMC-1001, 1:14-16, 2:39-42; TSMC-1022, Title, 1:15-21, 3:15-30, 9:33-39, 10:25-32, 12:25-32, Fig. 11.

Contemporaneous textbooks likewise show that the term “silicon oxide” was commonly used to refer to SiO₂:

Silicon oxide is also produced by chemical vapor deposition (CVD). In this method the silicon is supplied along with an oxygen-bearing compound, and the oxide is grown *on* the wafer rather than within the wafer, as in thermal oxidation. Various chemical systems have been used in oxide growth. Two examples are the dichlorosilane–nitrous oxide system



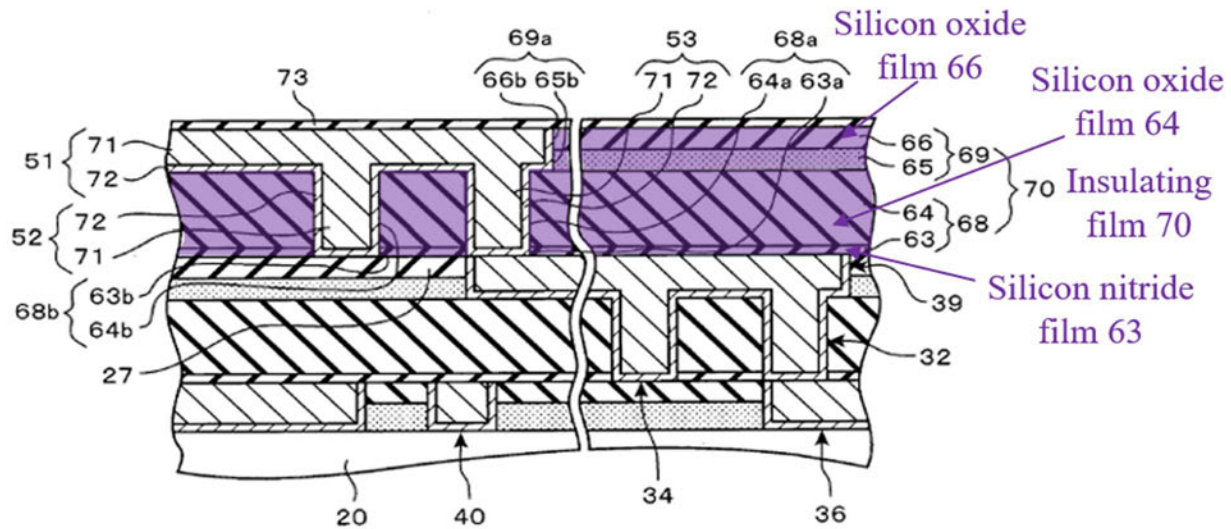
and the TEOS (tetraethylorthosilicate) system



TSMC-1023, 261. Thus, a POSITA would have understood Watanabe’s disclosures of silicon nitride and silicon oxide films as part of lower insulating film 38 to disclose the limitations of claim 11.

142. Annotated Figure 8 below discloses, in Watanabe’s fifth embodiment, the first insulating film (e.g., “insulating film 70”) having a multilayer structure including “silicon nitride film 63” and “silicon oxide film 64” (TSMC-1004, ¶[0119], Fig. 8):

FIG. 8



143. Thus, each of Watanabe's first through third and fifth embodiments satisfy claim 5.

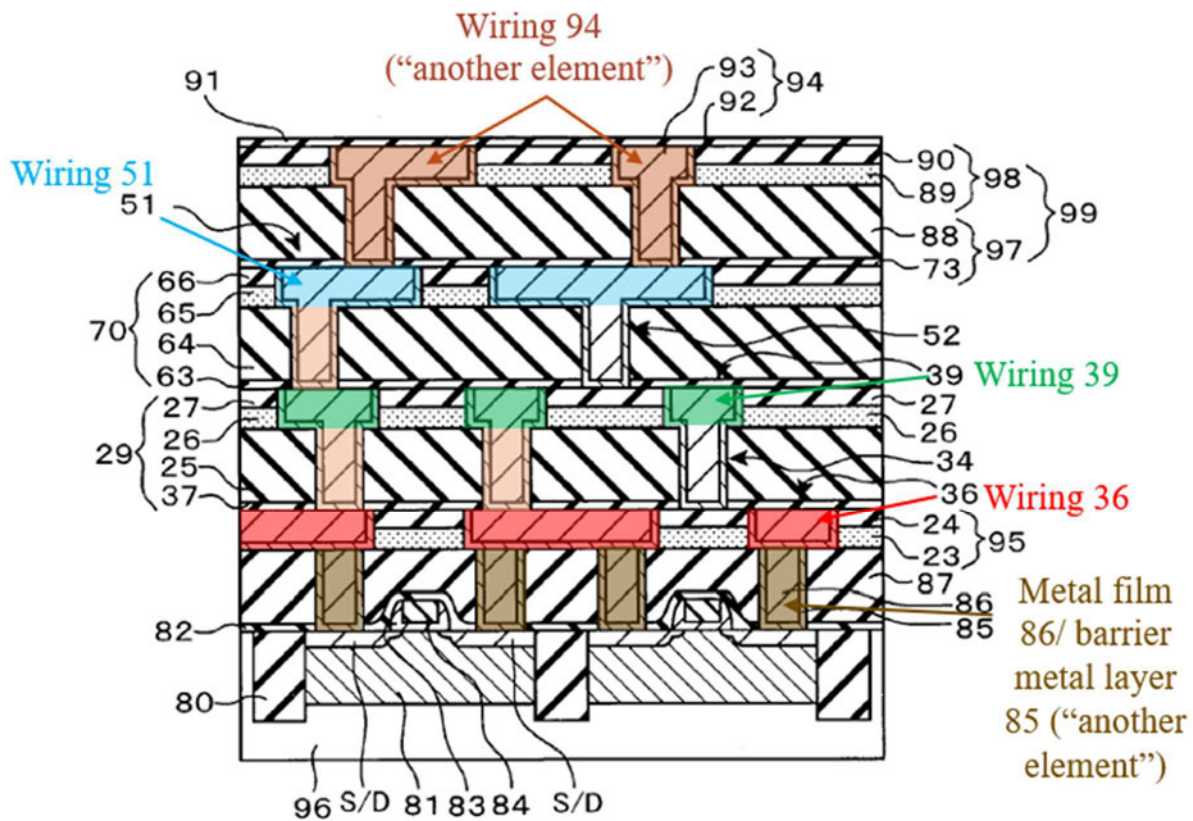
4. Claim 6 - *The method of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode.*

144. At least each of Watanabe's first through third and fifth embodiments meet claim 6.

145. Watanabe's first, second, third, and fifth embodiments disclose wiring 36 and wiring 39 as the claimed "first and second interconnects." *Supra*, §§X(A)(1)(1[a]), 1[d]. Watanabe's fifth embodiment additionally discloses wiring 39 and wiring 51 as the "first and second interconnects," respectively. *Id.*

146. A POSITA would understand that each of Watanabe's first and second interconnects (e.g., "wiring 36," "wiring 39," "wiring 51") is connected to another element or an external electrode. Watanabe explains that, while a two-wiring structure (wiring 36 and wiring 39) is disclosed, any number of wiring layers can be laminated by repeating the same method (of Figures 12A-12M). TSMC-1004, ¶[0171]. Watanabe's Figure 14 illustrates having a structure with four layers of wirings, including wiring 36, wiring 39, and wiring 51, which are each connected to other elements. *Id.*, ¶¶[0051], [0172]-[0181], Fig. 14. For example, for the first to third embodiments, wiring 36 is connected to a metal film 86 and wiring 39 is connected to wiring 51 by a conductive plug (which a POSITA would understand to be conductive plugs 32/53). *Id.* For the fifth embodiment, wiring 39 is connected to wirings 36 and 51 by conductive plugs (e.g., conductive plugs 32/53), and wiring 51 is connected to wiring 94 by another conductive plug, each of which constitute "other elements." *Id.* These connections are shown for example in annotated Figure 14 below:

FIG. 14



147. A POSITA would understand that each of the first to third and fifth embodiments provides a semiconductor device where wirings 36, 39, and 51 form a circuit to convey electrical signals/current to other elements. The specific components and connection/wiring configurations would depend on the design criteria/objectives for the device, which a POSITA would have readily and easily customized as required to meet such objectives.

148. Additionally, in describing its various embodiments, Watanabe states that the structures (like wiring 36, wiring 39, and wiring 51) are formed upon an underlying layer 20. *Id.*, ¶[0061], Figs. 1, 3, 8. Watanabe explains that the

underlying layer can include a MOSFET formed on a semiconductor substrate and conductive plugs through an insulating film. *Id.*, ¶¶[0089], [0094], [0116], [0173]. While Figures 1, 3, and 8 disclose this underlying layer 20 generically, Watanabe later shows the detailed composition of the underlying layer 20 in Figure 14 when discussing the broader applicability of its manufacturing method and resulting structures. *Id.*, ¶[0173].

149. Specifically, Watanabe states that the underlying layer 20 in each of the embodiments include the semiconductor transistor components shown in Figure 14, such as gate electrodes 84, source/drain regions S/D on a silicon substrate 96, and conductive plugs (comprising barrier metal layer 85 and metal film 86) connecting to these active device components. *Id.*, ¶¶[0061], [0089], [0094], [0016], [0173]-[0178]. These transistor components expressly shown in Figure 14 are representative of example circuit connections for all the embodiments discussed, including the first, second, third, and fifth embodiments. Thus, while Figures 1, 3, and 8 disclose this underlying layer 20 generically, Watanabe later shows the detailed composition of the underlying layer 20 in Figure 14 when discussing the broader applicability of its manufacturing method and resulting structures. *Id.*, ¶[0173].

150. Thus, for embodiments like the first, second, and third, Watanabe's wiring 36 is formed on this underlying layer 20 and connects to its elements, such

as the metal film 86 of the conductive plugs that connect to the S/D regions for the gate electrodes 84. *Id.*, ¶[0173]-[0174], Fig. 14. The wiring 39 is formed above and connected to the wiring 36 via conductive plug 32. *Id.*, Figs. 1, 3, 8, 14. Watanabe further discloses that any number of wiring layers can be stacked, and Figure 14 discloses a multi-level structure where the wiring 36 is connected to underlying device elements, and the wiring 39 is connected to the wiring 36 and can be connected to further elements like a wiring 51. *Id.*, ¶[0173]-[0178], Fig. 14.

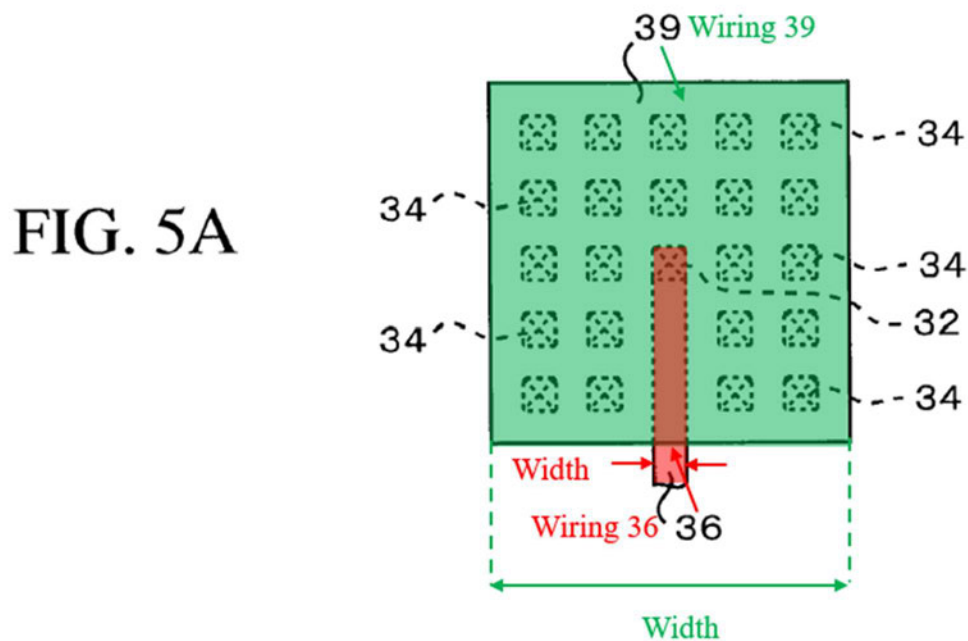
151. Thus, the wiring 39 is connected downwards to the wiring 36 via conductive plug 32; the wiring 36, in turn, connects to the underlying active members in underlying layer 20 as described above; and the wiring 51 is connected downwards to the wiring 39 via conductive plug 53. *Id.* These connections demonstrate that each of these interconnects is connected to another element (another wiring layer or underlying device members). In addition, a POSITA would understand that, in a semiconductor device, it is necessary that the functional wiring layers ultimately must be connected to other circuit elements or to external electrodes for the device to operate. *Id.*, ¶[0006], [0073].

152. Accordingly, Watanabe anticipates claim 6.

5. Claim 7 - *The method of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect.*

153. At least each of Watanabe's third and fifth embodiments discloses claim 7.

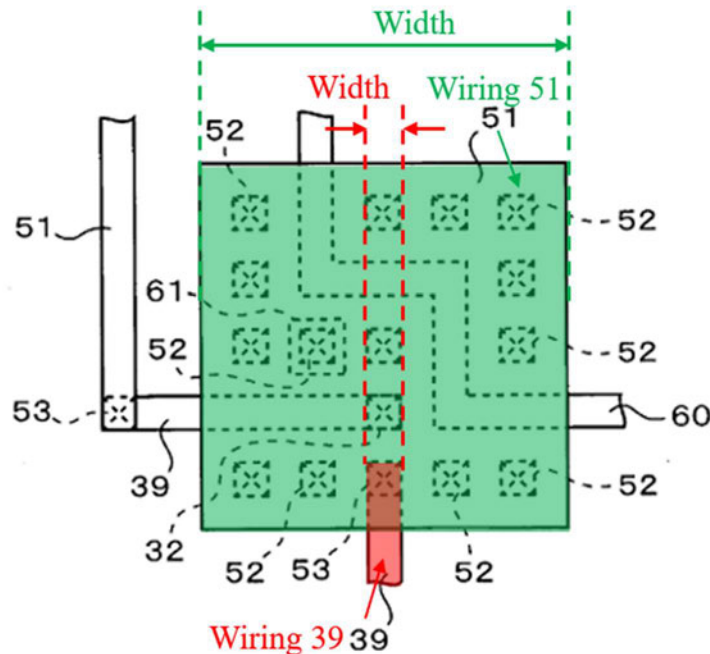
154. Annotated Figure 5A (third embodiment) below discloses the first interconnect (e.g., "wiring 36") as having a width smaller than that of the second interconnect (e.g., "wiring 39"). TSMC-1004, ¶¶[0094]-[0095], Figs. 5A-5C.



155. In the third embodiment, "wiring 39" may have a wider planar shape as opposed to the generally "linear shape" of the first and second embodiments. *See also* TSMC-1004, ¶¶[0042], [0049], [0094].

156. Similarly, the first interconnect (e.g., "wiring 39") of Watanabe's fifth embodiment has a width smaller than that of the second interconnect (e.g., "wiring 51") as disclosed in annotated Figure 9 below (TSMC-1004, ¶[0125], Fig. 9):

FIG. 9



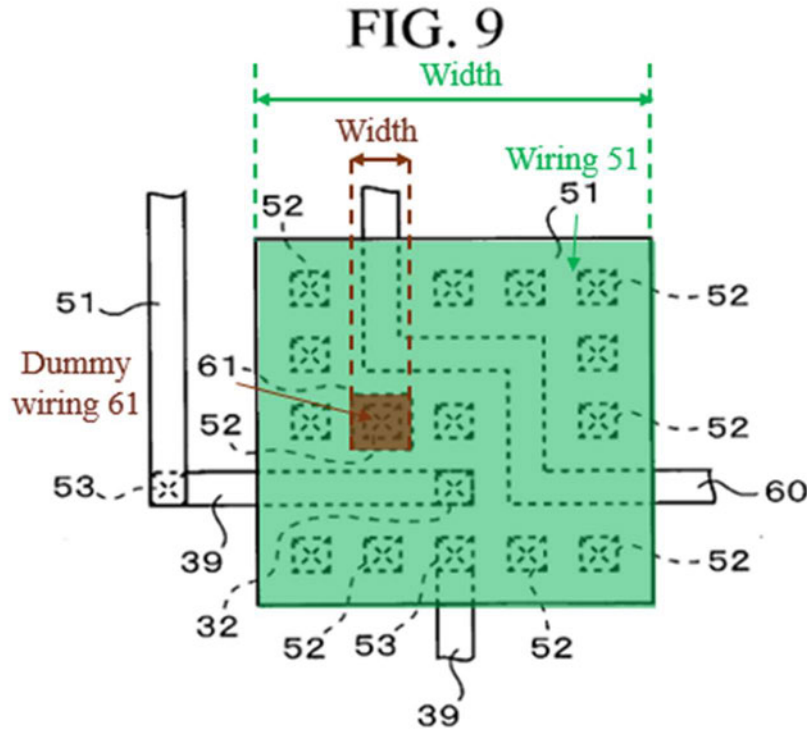
157. Like the third embodiment, the fifth embodiment similarly describes a narrower, linear first interconnect on a layer below a wider, planar second interconnect. TSMC-1004, ¶¶[0124]-[0125]. Thus, each of at least Watanabe’s third and fifth embodiments satisfies claim 7.

6. Claim 8 - *The method of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect.*

158. At least Watanabe’s fifth embodiment discloses claim 8.

159. As described for claims 1 and 2, Watanabe’s fifth embodiment discloses a first dummy interconnect (e.g., “dummy wiring 61”) and a second interconnect (e.g., “wiring 51”). *Supra*, §§X(A)(1), X(A)(2). In Watanabe’s fifth embodiment, the dummy wiring 61 (the “first dummy interconnect”) has a smaller

width than wiring 51 (the “second interconnect”), as shown in the plan view in annotated Figure 9 below:



160. As described in the discussion of claim 1, the fifth embodiment of Figures 8-9 discloses devices manufactured according to the process of Figures 12A-12N similar to those in the first to third embodiments except to add a third wiring layer (“wiring 51”). *Supra*, §X(A)(1); TSMC-1004, ¶¶[0116]-[0117]. Thus, at least the fifth embodiment meets all the elements of claims 1, 2, and 8.

7. Claim 10 - *The method of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square.*

161. At least Watanabe’s first-to-third and fifth embodiments meet claim 10.

162. Watanabe's plan view figures consistently disclose both the conductive plug 32 ("via") and the dummy conductive plug 34 ("dummy via") with substantially square outlines, thus indicating substantially square planar shapes. TSMC-1004, Fig. 2. For example, Figure 2 of Watanabe, which is described as a plan view showing the semiconductor device according to the first embodiment, shows two conductive plugs 32 and the dummy conductive plug 34 as squares. *Id.*, ¶[0039], [0070], Fig. 2. Similarly, Figure 4 of Watanabe (plan view of the second embodiment) also discloses two conductive plugs 32 and two dummy conductive plugs 34 as squares. *Id.*, [0041], Fig. 4. Figures 5A, 5B, and 5C of Watanabe (plan views of the third embodiment) further illustrate conductive plug 32 and various arrangements of dummy conductive plugs 34, all represented with substantially square planar shapes. *Id.*, ¶[0098], Figs. 5A, 5B, 5C.

163. In Watanabe's fifth embodiment, the plan view in Figure 9 discloses conductive plug 53 ("via") and dummy plugs 52 ("dummy via") with outlines consistent with a square planar shape. *Id.*, ¶[0124]-[0127], Fig. 9. Given the consistent representation across multiple embodiments in plan view, a POSITA would understand a substantially square planar shape to be a disclosed option for both the via and the dummy via.

164. Therefore, for each of first-to-third and fifth embodiments, Watanabe discloses that plug 32 and dummy plug 34 each have a planar shape that is

substantially square, exemplified in annotated Figures 2, 5A, and 9 (*see id.*, TSMC-1004, ¶[0039], Figs. 4, 5A-5C, 9):

FIG. 2

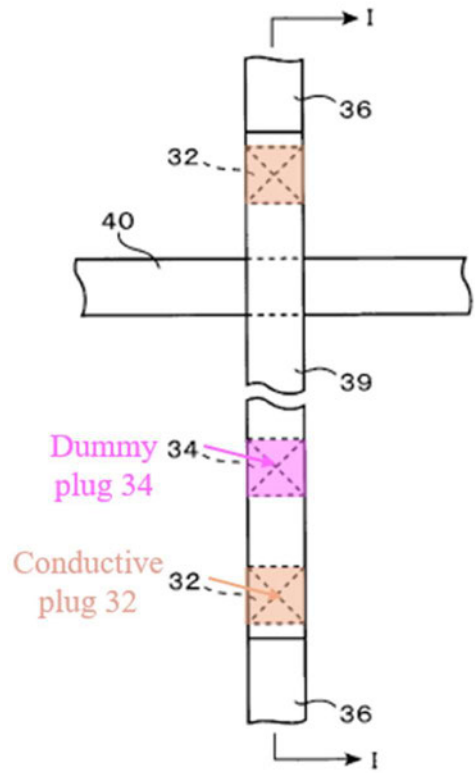


FIG. 5A

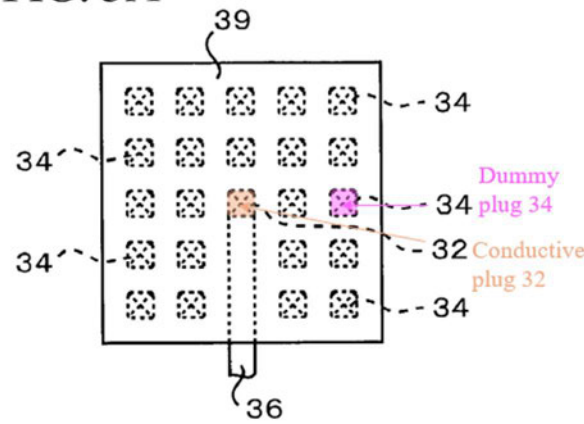
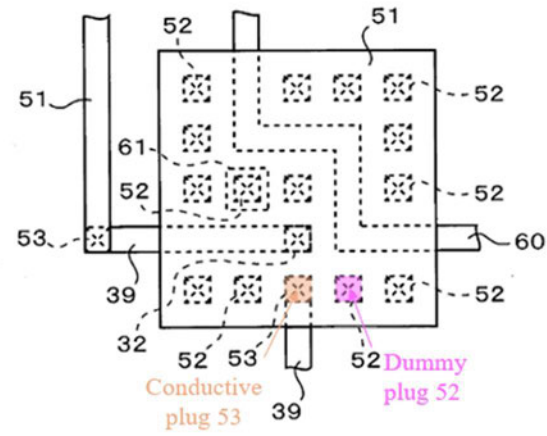


FIG. 9



165. Moreover, a POSITA understood at the time that square vias (both dummy and functional) were a known option for the via shape. *See also* TSMC-1008, 9:45-47 (“It will be also understood that the opening of the via-hole may have any configuration, such as a square, rectangle or circle.”), 10:8-11; TSMC-1013, 9:45-49 (“[T]he shape of dummy via holes are indicated by squares, rectangles, and line patterns. The shapes of the dummy wiring patterns and dummy via holes may take other shapes.”); TSMC-1039, 5:27-32 (noting the greater contact area achieved with square vias). Thus, Watanabe discloses substantially square cross-sections to be a disclosed shape for both the plugs 32 and dummy plugs 34.

8. Claim 11 - *The method of claim 1, wherein the first interconnect and the second interconnect extend in a same direction.*

166. Each of the first through third and fifth embodiments of Watanabe discloses claim 11.

167. As shown for example in each of annotated Figures 1 and 2 below, Watanabe discloses that the first interconnect (e.g., “first wiring 36”) and the second interconnect (e.g., “second wiring 39”) extend in a same direction (e.g., along the “L” direction in Fig. 1). TSMC-1004, Figs. 1-4, ¶[0095]. For example, the cross-sectional views in Figures 1 and 3 (as well as Figure 8) show both first wiring 36 and second wiring 39 as parallel interconnects extending across the page (i.e., the “same direction” “L”), as confirmed in the corresponding plan views in Figures 2

and 4. Annotated Figures 1 and 2 below disclose the wirings 36 and 39 extending in the same direction:

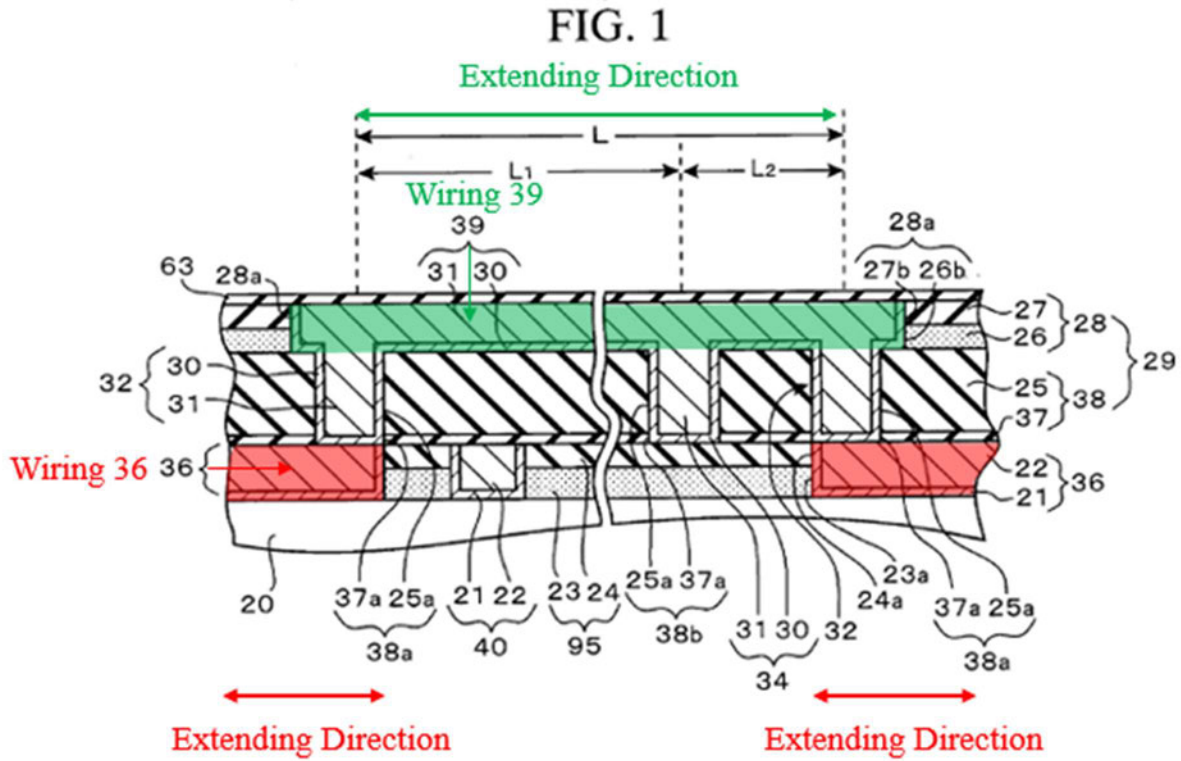
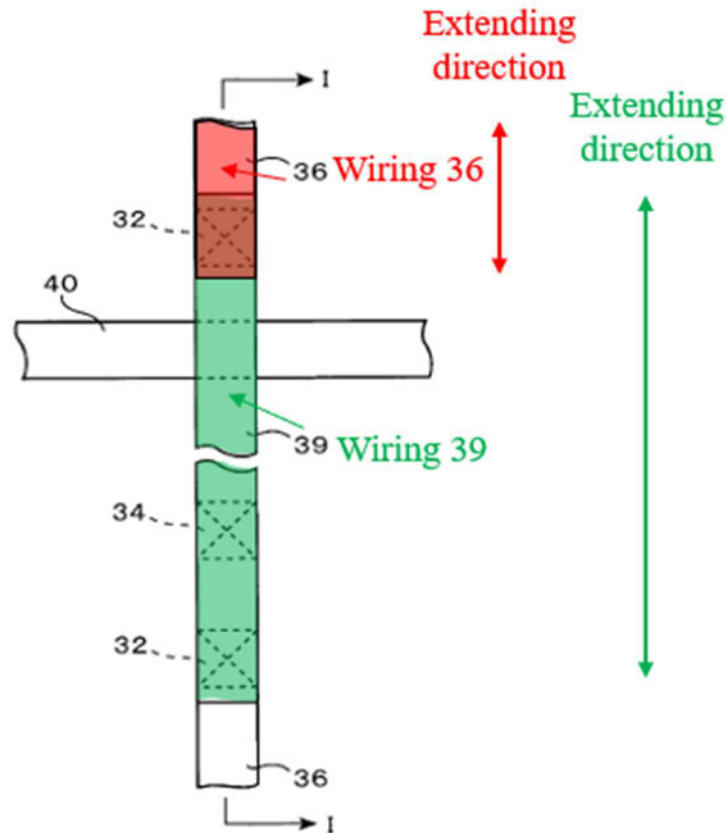


FIG. 2



168. Figure 5A also discloses first wiring 36 and second wiring 39 extending in the same direction (*id.*, Figs. 5A-5C, ¶¶[0095], [0111]), as does Figure 9 for wiring 39 and 51, as shown in the annotated figures below:

FIG. 5A

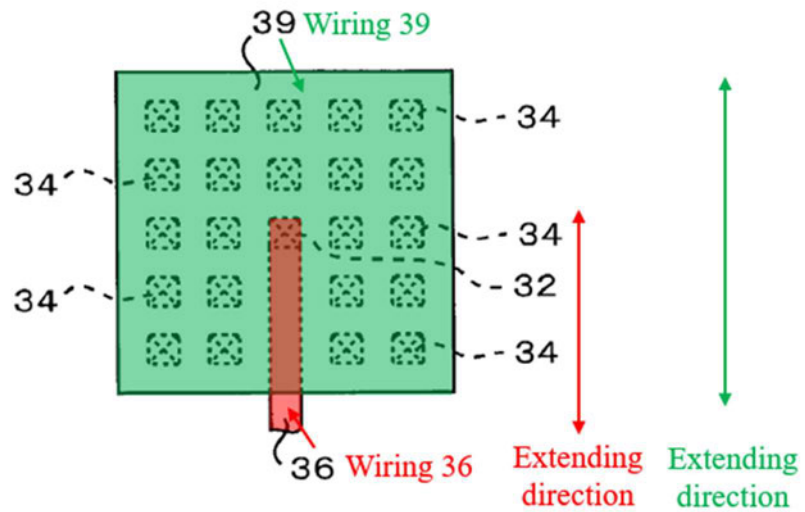
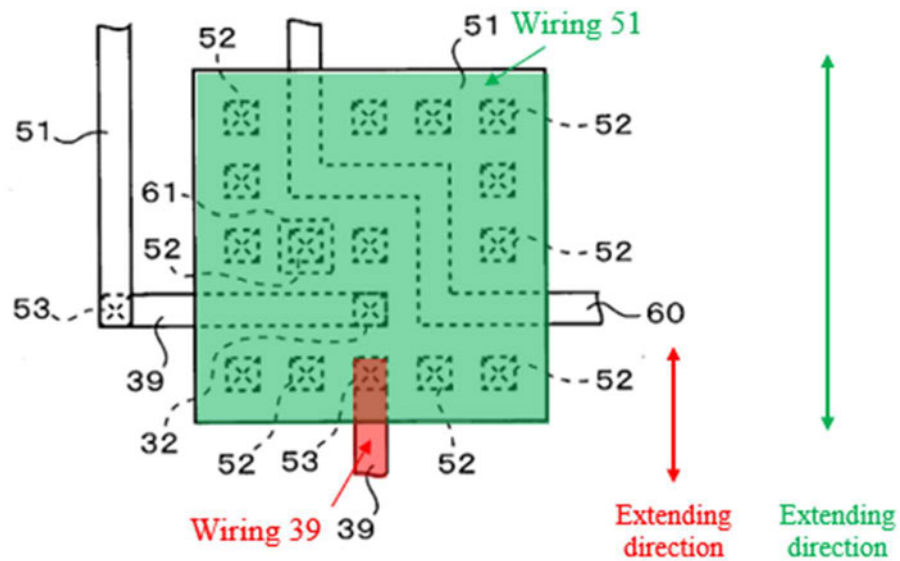


FIG. 9



9. Claim 12 - *The method of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends.*

169. Each of the first through third and fifth embodiments of Watanabe discloses claim 12.

170. Watanabe's plan view figures show dummy conductive plugs 34 (or 52 in Figure 9) ("dummy vias") positioned along an extended line along which the first wiring 36 (or 39 in Figure 9) (i.e., the claimed "first interconnect") extends. For instance, Figures 2, 4, and 5A-C of Watanabe disclose the dummy conductive plug 34 aligned directly along an extended line along which the first wiring 36 extends, as exemplified in the annotated figures below:

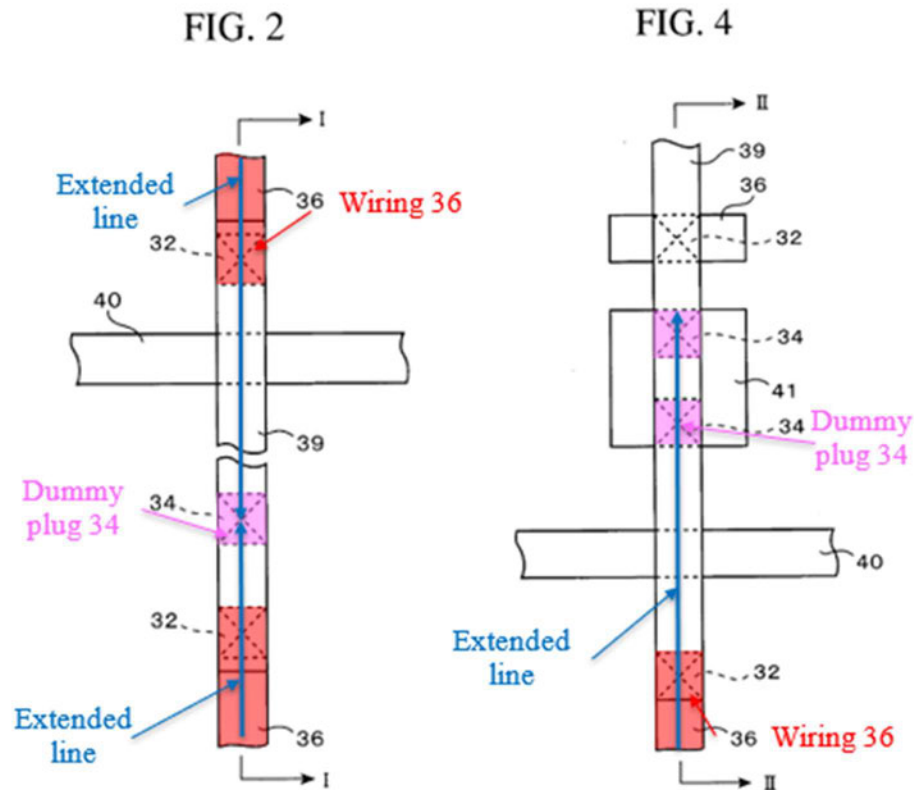
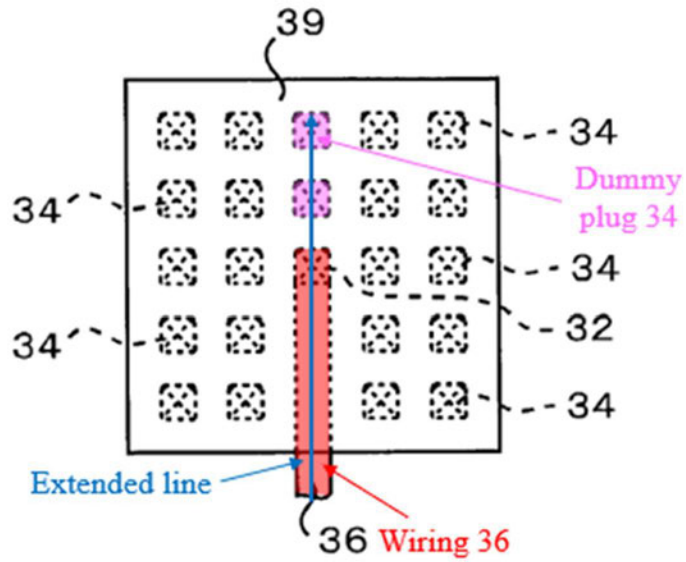
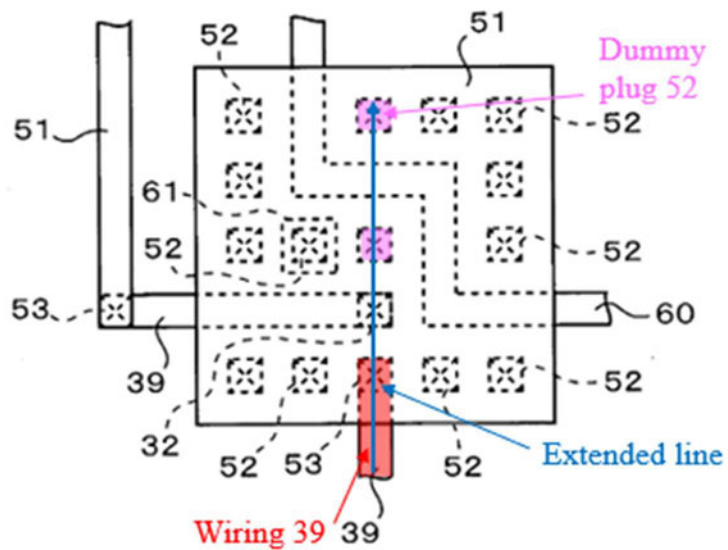


FIG. 5A



171. Similarly, Figure 9 of Watanabe discloses dummy conductive plugs 52 situated on an extended line along which the first wiring 39 extends as shown in the annotated figure below:

FIG. 9



10. Claim 13 - *The method of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less.*

172. Each of Watanabe's embodiments satisfies claim 13.

173. The '751 patent refers to the "space" between a via and dummy via as corresponding to the distance from an edge of the via and a closest edge of an adjacent dummy via. TSMC-1001, 4:21-25. Watanabe expressly discusses and analyzes the distances between the conductive plug 32 ("via") and the dummy conductive plug 34 ("dummy via"). TSMC-1004, ¶¶[0081], [0086]-[0087], [0100]-[0105], Figs. 15A-17C. Specifically, Watanabe discloses that the via (e.g., plug 32) and the dummy via (e.g., dummy plug 34) are spaced at a distance of 25 μm or less (e.g., 0.3 μm). TSMC-1004, ¶[0105] ("the interval between the neighboring plugs (including the plug 32 and the dummy plug 34) was fixed to 0.3 μm ."), Figs. 15A-17C.

174. Watanabe provides an example where the interval between the neighboring plugs (including the plug 32 and the dummy plug 34) was fixed to 0.3 μm for simulations involving the models shown in Figures 17B-17C. *Id.*, ¶[0105], Figs. 17B-17C. This interval/pitch "p₂" is disclosed in the annotated figures 16B and 17B below:

FIG. 16B

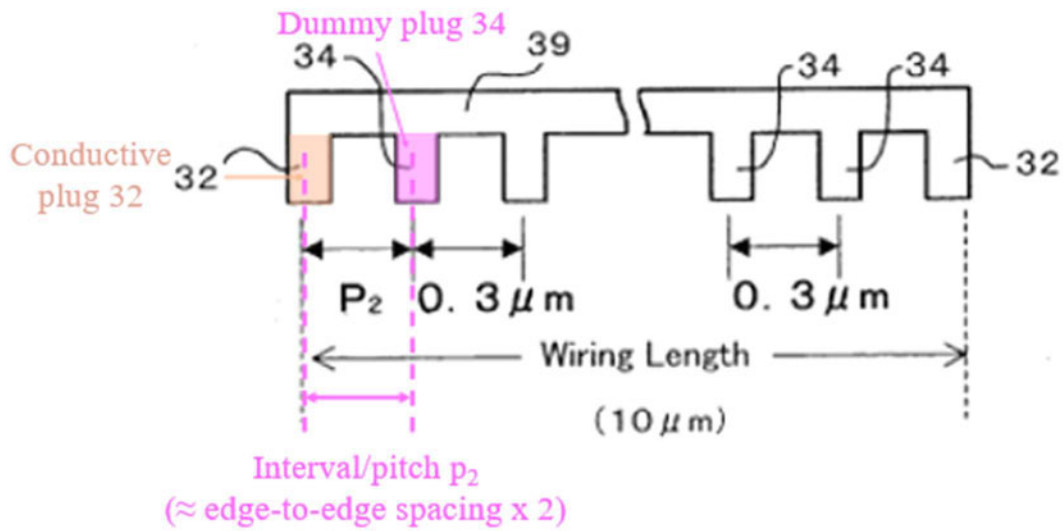
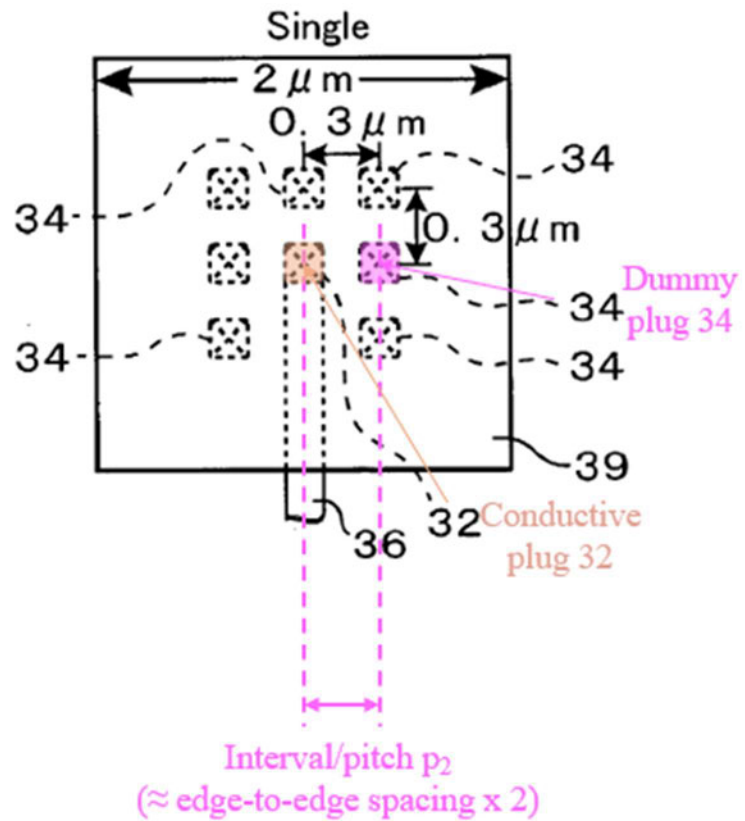


FIG. 17B



175. As shown in annotated Figure 16B above, the interval/pitch “ p_2 ” in Watanabe is the interval from a center of a via to a center of an adjacent dummy via,

so the spacing from an edge of the via to an edge of the adjacent dummy plug is necessarily less than the interval/pitch p_2 —in Watanabe’s case, the edge-to-edge spacing is approximately half the pitch interval. So as an example, the spacing distance between the right side of the conductive plug 32 annotated above in Figures 16B and 17B and the left side of the nearest dummy plug 34 is less than the interval or pitch between those same plugs. Thus, because this 0.3 μm interval/pitch between plugs 32 and 34 satisfies the 25 μm or less requirement of claim 13, the edge-to-edge spacing between the same plugs necessarily satisfies this requirement as well.

176. Indeed, Watanabe explicitly discusses and analyzes the spacing between the conductive plug 32 (“via”) and the dummy conductive plug 34 (“dummy via”). TSMC-1004, ¶¶[0032]-[0033], [0053], [0086]-[0087], [0100]-[0105], [0190]-[0191], [0193], Figs. 16A, 17B, 17C. In the simulation results shown in Figure 16A, Watanabe investigates the effect of varying the pitch p_2 (an interval between the conductive plug 32 and the adjacently arranged dummy conductive plug 34) on stress migration. *Id.*, ¶¶[0086]-[0087], Fig. 16A. All data points evaluated in Figure 16A entail a pitch p_2 of 1.0 μm or less. *Id.* Watanabe concludes that in order to prevent the stress-migration, it is preferable that the first pitch p_2 is less than 1 μm , and more preferably less than 0.6 μm . *Id.*, ¶[0087]. A spacing of less than 1 μm or 0.6 μm satisfies the condition of being 25 μm or less.

177. A POSITA would have interpreted these teachings from Figures 16 and 17 as applying to the arrangements in Watanabe's first-through-third and fifth embodiments, as disclosed in Figures 1-5 and 8-9.

11. Claim 18 - *The method of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film.*

178. Each of Watanabe's first through third and fifth embodiments satisfies claim 18.

179. Watanabe's dummy via (e.g., "dummy plugs 34" in the first through third embodiments and "dummy plugs 52" in the fifth embodiment) and the second interconnect (e.g., "second wiring 39" in the first through third embodiments; "third wiring 51" in the fifth embodiment) are made of the same conductive film (e.g., "copper film 31," "barrier metal layer 30"). TSMC-1004, ¶¶[0067]-[0070], [0072], [0166]-[0168], Figs. 12L-12M. Watanabe explains "The barrier metal layer 30 and the copper film 31 ...constitute the second wiring 39. Then, the portion of the second wiring 39, which is buried in the via hole 38 a, is served as the plug, and the portion of the second wiring 39, which is buried in the dummy via hole 38 b, is served as the dummy plug." TSMC-1004, ¶[0168]. Thus, both the dummy vias and the interconnect above them are lined with barrier metal layer 30 and then filled with copper film 31, i.e., the same conductive film.

180. In Watanabe's fifth embodiment, the same principle applies. The dummy plug 52 ("dummy via") and the third wiring 51 ("second interconnect") are also formed from the same conductive film (i.e. barrier metal layer 72 and copper film 71). *Id.*, ¶¶[0121]-[0122] (wiring buried in dummy via hole 68b is dummy plug 52), Fig. 8.

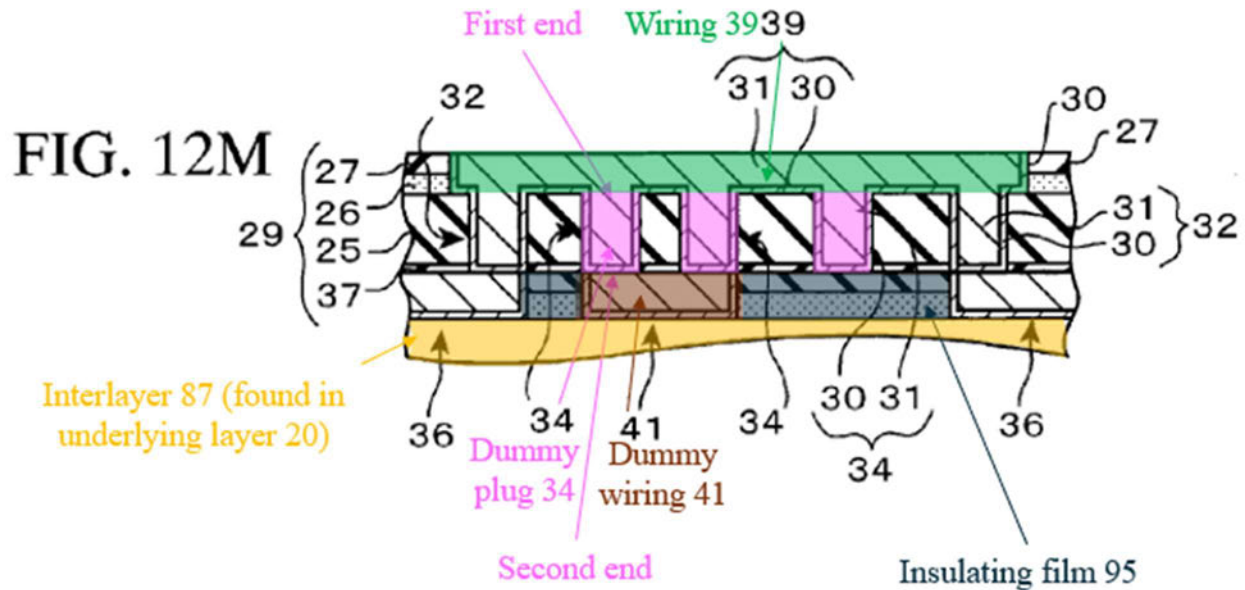
181. Watanabe thus anticipates claim 18.

12. Claim 20 - *The method of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film.*

182. At least Watanabe's second and fifth embodiments meet claim 20.

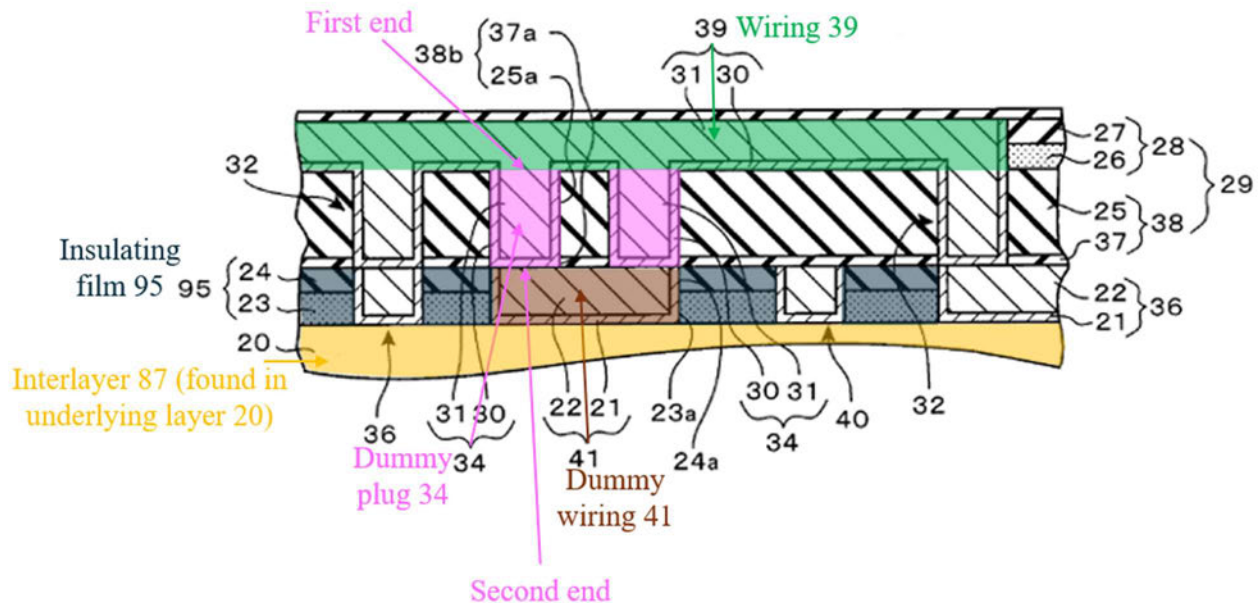
183. Watanabe's second embodiment discloses that a dummy via (e.g., "dummy plug 34") includes a first end and a second end, the first end connected to the second interconnect (e.g., "wiring 39") and the second end connected to a first dummy interconnect (e.g., "dummy wiring 41"), where the first dummy interconnect is surrounded by a second insulating film, e.g., insulating film 95, optionally

including interlayer insulating film 87.⁶ TSMC-1004, ¶¶[0089]-[0090], [0140]-[0144], [0172]-0174], Figs. 3, 12B-12D, 12M, 14. Annotated Figs. 12M and 3 disclose these features:



⁶ Underlying layer 20 may also include an insulating film such as interlayer insulating film 87 that would be beneath dummy wiring 41. See TSMC-1004, ¶[0173], Fig. 14.

FIG. 3



184. As illustrated above, insulating film 95 surrounds a periphery of the second, lower end of dummy 41. More specifically, the first end of dummy plug 34 is connected to the wiring 39 (the claimed “second interconnect”), as they are formed integrally in a dual damascene process. *Id.*, ¶¶[0072], [0167]-[0168], Figs. 3, 12K-12M. The second (bottom) end of dummy plug 34 is connected to a dummy wiring 41 (the claimed “first dummy interconnect”). *Id.*, ¶[0090], Figs. 3, 12M. This dummy wiring 41 is formed within a trench in the first insulating film 95 (comprising low-dielectric insulating film 23 and silicon oxide film 24), which corresponds to the claimed “second insulating film” in the context of claim 42. *Id.*, Figs. 12B-12D. The dummy wiring 41 is also on the underlying layer 20, which is described as including an insulating film, shown in Figure 14 as including an interlayer insulating film 87. *Id.*, ¶¶[0061], [0173], Figs. 3, 12D, 14. Thus, interlayer insulating film 87

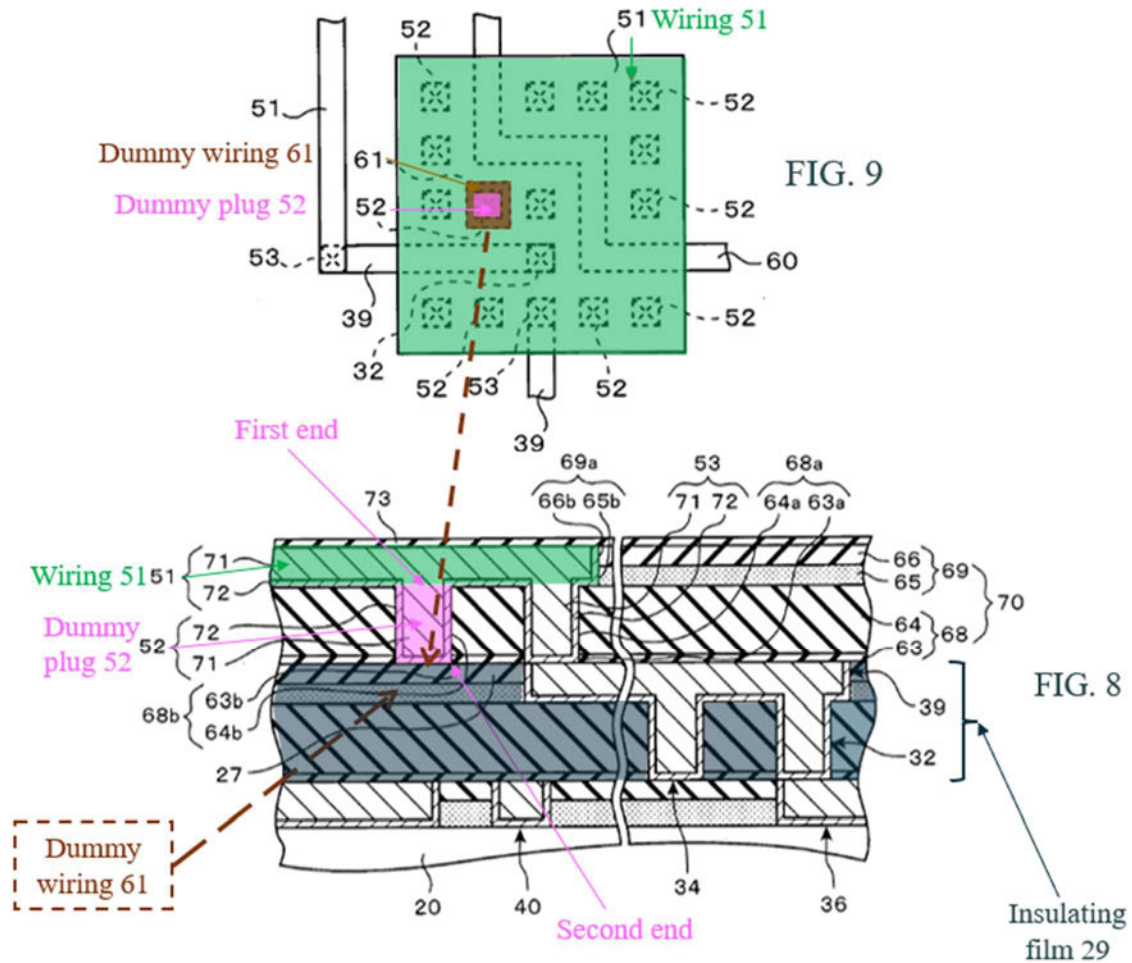
of the underlying layer 20 could also be considered part of the claimed “second insulating film” in the context of claim 20. The dummy wiring 41 is thus laterally confined by the insulating material of first insulating film 95 and supported underneath by the interlayer insulating film 87 of the underlying layer 20, meaning it is surrounded by a “second insulating film” collectively comprising insulating films 95 and 87. *Id.*, Figs. 3, 12d, 14.

185. In Watanabe’s fifth embodiment dummy via (e.g., “dummy plug 52”) has a first end connected to the second interconnect (e.g., “wiring 51”) and a second end connected to a first dummy interconnect (e.g., “dummy wiring 61”), the first dummy interconnect being surrounded by a second insulating film (e.g., “insulating film 29”). TSMC-1004, ¶¶[0127], [0116]-[0123], [0140]-[0144], Figs. 8-9, 12B-12D, 12M; *see also supra*, §§X(A)(1)(1[d]), X(A)(2).

186. As also outlined above, dummy wiring 61 would be formed in the same layer as wiring 39, and dummy plug 52 is connected to dummy wiring 61. Watanabe explains that “dummy wiring [61] [is] formed in the same layer as the second wiring 39. The dummy plug 52 may be connected to this dummy wiring 61.” TSMC-1004, ¶[0127]. Together with Watanabe’s method of manufacturing (*see id.*, [0144], Figs. 12A-12D), a POSITA would understand that “dummy wiring 61” is formed in the

same insulating film (e.g., “insulating film 29”)⁷ as “wiring 39” in Figure 8. Annotated Figures 8 and 9 below disclose the approximate location of “dummy wiring 61” when the cross-sectional view otherwise in Figure 8 is drawn through dummy wiring 61. As demonstrated, dummy wiring 61 is surrounded by insulating film 29 (*id.*, Figs. 8-9):

⁷ Watanabe explains that Figure 8 is similar to the first to fourth embodiments, and adds third wiring layer 51. *See* TSMC-1004, ¶¶[0116]-[0117]. Films 25 and 26 are labeled in the first and second embodiments (e.g., Figures 1 and 3) and the manufacturing process figures (e.g., Figures 12A-12d). *See id.*, ¶¶[0066]-[067], [0150]-[0152], *supra*, §X(A)(1)(1[b]).



187. As illustrated above, insulating film 29 in the fifth embodiment as disclosed in Figures 8-9 of Watanabe surrounds a second, lower end of dummy wiring 61.

B. Ground 2: Watanabe combined with Kamoshima renders Claims 3-4 and 15-16 unpatentable

188. For the reasons detailed below, I believe Claims 3-4 and 15-16 are obvious over Watanabe in view of Kamoshima.

1. Claim 3

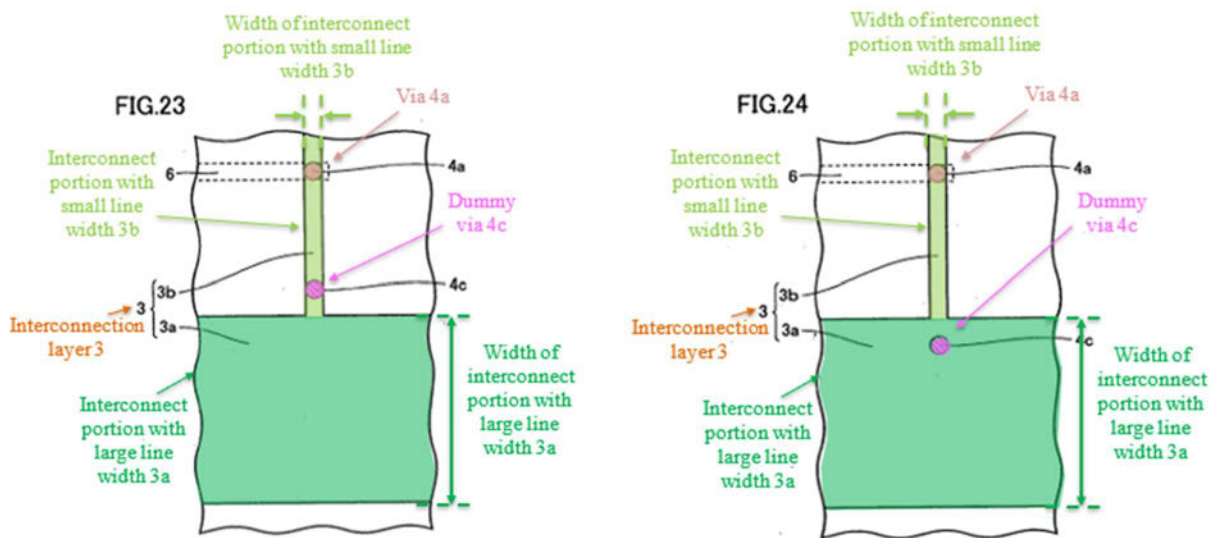
[3a] The method of claim 1, wherein in the step (c) the interconnect trench is comprised of a first interconnect trench portion and a second interconnect trench portion whose width is smaller than that of the first interconnect trench portion and which branches from the first interconnect trench portion, and

189. As described for claim 1, Watanabe discloses step (c), which includes forming in the first insulating film (e.g., “insulating film 29,” “insulating film 70”), ...an interconnect trench (e.g., “wiring trench 28a,” “wiring trench 69a”) connected to the via hole and the dummy hole. *Supra*, §X(A)(1)(1[c]).

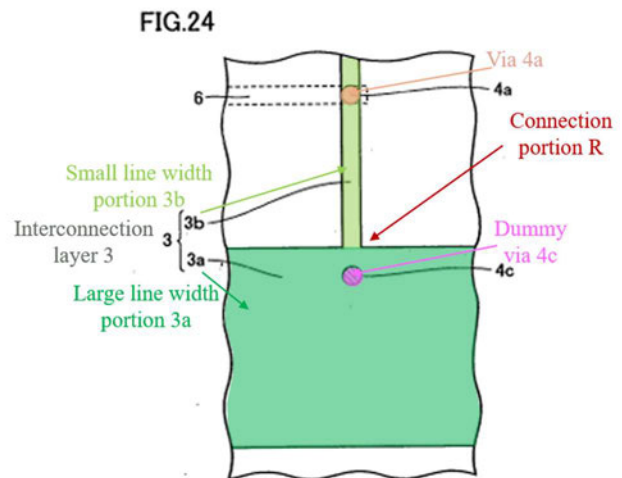
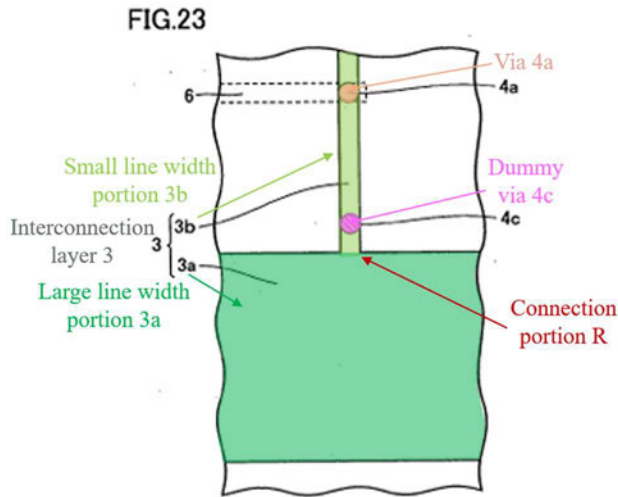
190. Element 3[a] recites that the “interconnect trench is comprised of a first interconnect trench portion and a second interconnect trench portion whose width is smaller than that of the first interconnect trench portion and which branches from the first interconnect trench portion.” Kamoshima discloses such a shaped interconnect trench, which is used to form a correspondingly shaped interconnect (e.g., “interconnection layer 3” having an “interconnection portion with a large line width 3a” and an “interconnection portion with a small line width 3b”). TSMC-1009, ¶¶[0002], [0062], [0094]-[0103], Abstract, Figs. 8-9, 23-27.

191. In its first embodiment, Kamoshima discloses forming an interconnect (“interconnection layer 3”) by depositing conductive material (e.g., “barrier metal layer,” “copper layer”) in an interconnect trench (e.g., “groove 1a”) formed in

“insulating layer 1.” *Id.*, ¶¶[0043]-[0044]. In Figures 23-27, Kamoshima discloses various possible shapes in which interconnection layer 3 may be formed, including shapes corresponding to the trench configuration recited in claim 3 in which a narrower portion (e.g., “interconnection portion with a small line width 3b”) branches off a wider portion (e.g., “interconnection portion with a large line width 3a”) (*see id.*, ¶¶[0094]-[0103], Figs. 23-27):

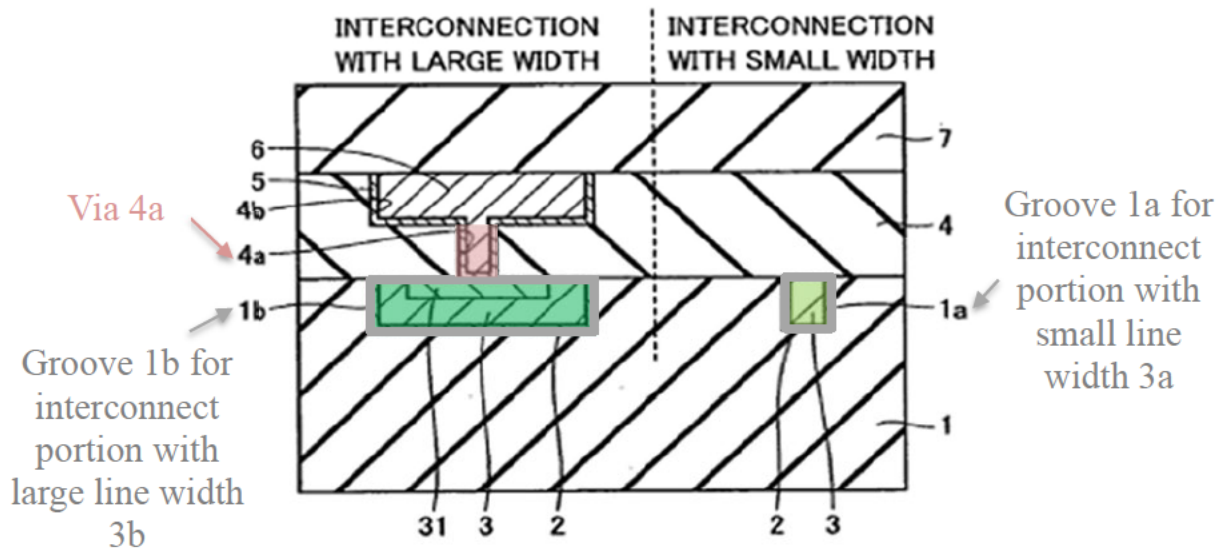


192. These small and large line width portions are connected to a branch point (“connection point R”) formed in the vicinity of dummy via 4c as shown in further annotated Figures 23 and 24 below:



193. A POSITA would recognize that when forming the interconnection layer 3 from Figures 23-24 respective trench portions conforming to the small line width portion 3b and the large line width portion 3b would be formed and used. Indeed, Kamoshima explains that multiple trench portions (e.g., “groove 1a,” “groove 1b”) may be used to form the first and second interconnection portions having different respective widths. *See id.*, ¶¶[0062], [0068]-[0069], Figs. 8-9. These trench portions include a first, wider trench portion (e.g., “groove 1b for an interconnection portion with a large line width (wide interconnection)”) and a second, narrower trench portion (e.g., “groove 1a for an interconnection portion with a small line width (narrow interconnection)”). *Id.*, ¶[0062] (“Referring to FIG. 8, interlayer insulating layer 1 is formed on the semiconductor substrate (not shown). Groove 1a for an interconnection with a small line width (narrow interconnection) and a groove 1b for an interconnection with a large line width (wide interconnection) are formed on the surface of interlayer insulating layer 1.”).

FIG.8



194. Accordingly, reading Kamoshima as a whole, a POSITA would understand that the corresponding wide and narrow portions (e.g., “interconnection portion with a large line width 3a” and “interconnection portion with a small line width 3b”) of “interconnection layer 3” in the embodiments of Figures 23-24 are created by forming similar corresponding interconnect trench portions (e.g., “grooves”) and filling those trench portions with conductive material (e.g., a barrier metal layer and a copper layer). This is similar to how wiring 39 (and the other “second interconnects” of Watanabe) is formed in Watanabe (e.g., by first forming “wiring trench 28a” in which conductive material is later deposited to create “wiring 39,” etc.). *Supra*, §X(A)(1)(1[c]). These interconnect trench portions include a wide portion, and a narrow portion that branches off the wide portion. *See* TSMC-1009,

Figs. 23-24. Thus, Kamoshima meets the interconnect trench shape recited in claim 3.

195. Accordingly, in view of Kamoshima (e.g., Figures 23-24), a POSITA would have understood the claimed branched shape (with a narrower portion extending from a wider portion) was a known design option for the shape of any of Watanabe's wirings that correspond to the claimed "second interconnect" (e.g., "wiring 39," "wiring 51") (and thus also for the trenches used to form such wirings, e.g., wiring trench 28a, wiring trench 69a). Thus, it was obvious to a POSITA for Watanabe's wiring trenches 28a or 69a to be similarly shaped so as to create an interconnect having a branched configuration similar to Kamoshima's "interconnection layer 3" of Figures 23-24. Doing so would simply involve changing Watanabe's step of forming in the first insulating film (e.g., "insulating film 29," "insulating film 70"), ...an interconnect trench (e.g., "wiring trench 28a," "wiring trench 69a") connected to the via hole and the dummy hole (*supra*, §X(A)(1)(1[c])) so that the wiring trenches 28a/69a included a similar shape for the trench/grooves used to create Kamoshima's interconnection layer(s) 3 from Figures 23-24.

196. Moreover, because Kamoshima's interconnection layer 3 is ***connected to both a real via (i.e., via 4a) and a dummy via*** (i.e., via 4c) (*see, e.g., TSMC-1009, Figs 22-24*), a POSITA would have understood that the shape of Kamoshima's

“interconnection layer 3” was an option for Watanabe’s upper layer wirings (e.g., “second wiring 39” and “third wiring 51”), which likewise are common interconnects that are connected to both a real via (e.g., “conductive plug 32”) and a dummy via (e.g., “dummy plug 34”). TSMC-1004, ¶¶[0070]-[0073], [0117]-[0122], Figs. 1-5C, 8-9. Accordingly, when considering potential shapes for Watanabe’s “second wiring 39” and “third wiring 51,” a POSITA would have considered the shapes of Kamoshima’s “interconnection layer 3” as potential options given their similarity in connections (e.g., to both real and dummy vias).

197. Given that such a shape was a known design option, a POSITA would have been motivated to select that shape wherever the design objectives for the corresponding device would have found that shape advantageous. For example, a POSITA further would have been motivated to implement such an interconnect shape (and thus a corresponding shape for the trench portions) so as to create a narrow branch through which microvoids would need to flow to reach real via 4a, as expressly taught by Kamoshima. The foregoing branched interconnect shape allows a dummy via to be located near the branchpoint between the narrow and wide portions of the interconnect so as to block such microvoids from reaching the real via, and thus further suppresses the concentration of voids under the real via positioned on the narrow portion/branch. Kamoshima expressly notes that such an interconnect design offered the foregoing benefit of further suppressing void

concentrations in the narrower branch, where the real via could be located. *See* TSMC-1009, ¶[0098] (“A large number of microvoids in interconnection layer with a large line width $3a$ tend to *concentrate in the area under dummy via 4c before reaching the area under via 4a*. **Therefore, concentration of voids in the area under via 4a can further be suppressed.**”); *see also id.*, ¶¶[0088],[0097]-[0099]. Thus, Kamoshima teaches a known design choice of an interconnect shape that has the added benefit of further suppressing microvoids under functional vias.

198. Accordingly, a POSITA would have been motivated to modify Watanabe in view of Kamoshima such that Watanabe’s plug 32/53 would be connected to the small line width portion and dummy plug 34/52 would be connected to the large line width portion of the interconnect trench. This modification would enhance suppression of the microvoids under plug 32 as well as other functional vias in Watanabe’s design in any of the first to fifth embodiments. *See also* TSMC-1033, ¶¶[0056]-[0057], [0112]-[0114] (“A sample without the narrow wiring and a sample having the narrow wiring length of $2\text{ }\mu\text{m}$ was checked.... The sample without the narrow wiring showed the defective factor of about 1%. The sample with the narrow wiring of about $2\text{ }\mu\text{m}$ in length showed the defective factor of about 0%.”). Watanabe already teaches address stress migration, and the POSITA would recognize that incorporating Kamoshima’s interconnect shape and corresponding

via/dummy via configuration teaching would further enhance the suppression of microvoids.

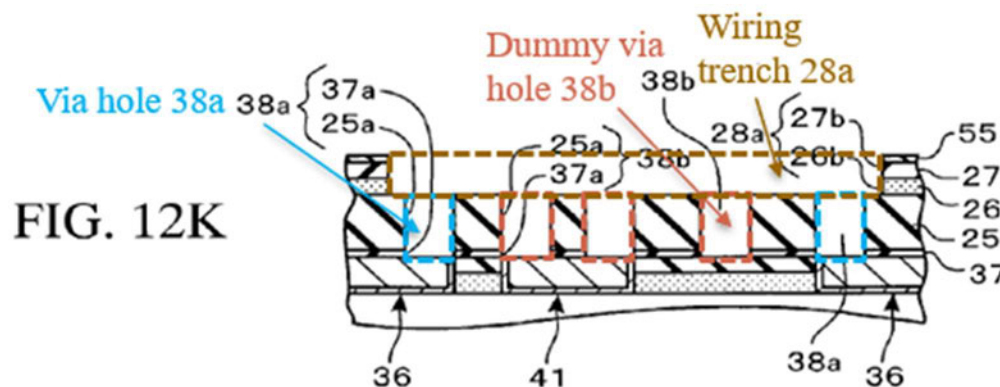
199. A POSITA would have found this modification easy to implement and thus would have had a reasonable expectation of success when doing so. As demonstrated above, both Watanabe and Kamoshima relate to forming an interconnect connected to both a via (to connect to another interconnect) and dummy via, where the dummy via is present to suppress voids from concentrating in the via. Implementing such a configuration would have merely involved etching the trench in the desired branched shape with appropriate trench portion widths and then filling such trenches with appropriate conductive material (e.g., barrier metal layer and bulk copper layer) to form the interconnect and via holes, which was well within the capabilities of a POSITA at the time of the alleged invention, and easily achieved with the manufacturing processes already used in Watanabe to construct its interconnects.

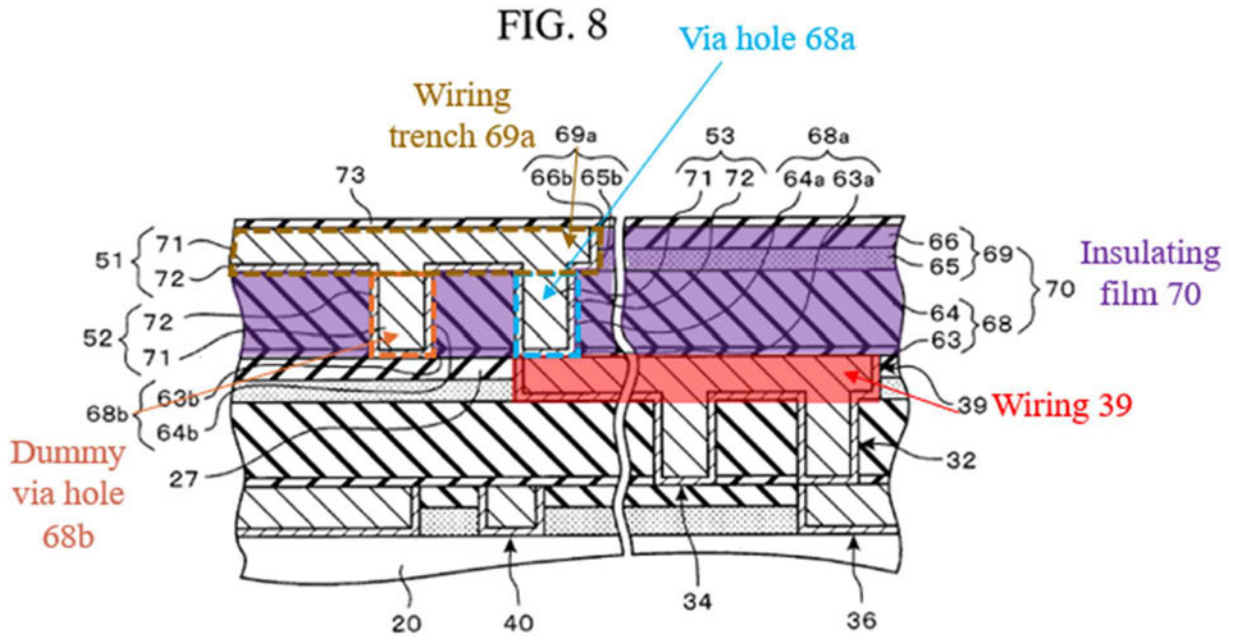
200. Accordingly, a POSITA would have found it obvious in view of Kamoshima to modify the shape of Watanabe's wiring trenches 28a and 69a (and indeed the wiring trenches used to form the "second interconnects" in any of the embodiments of Watanabe discussed previously – *see supra*, §X(A)(1)) such that element 3[a] of "in the step (c) the interconnect trench is comprised of a first interconnect trench portion and a second interconnect trench portion whose width is

smaller than that of the first interconnect trench portion and which branches from the first interconnect trench portion” was satisfied.

[3b] the via hole and the dummy hole are connected to the interconnect trench.

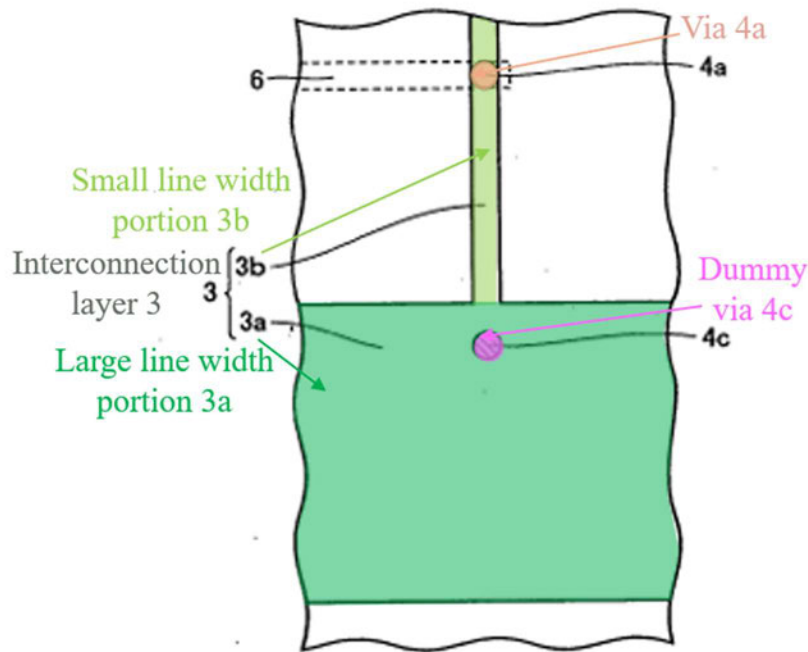
201. Watanabe discloses that the via hole (e.g., “via hole 38a,” “via hole 68a”) and the dummy hole (e.g., “dummy via hole 38b,” “dummy hole 68b”) are connected to the interconnect trench (e.g., “wiring trench 28a,” “wiring trench 69a”). TSMC-1004, ¶¶[0067], [0118]-[0121], [0159]-[0165], Figs. 1, 3, 8, 12J-12K; *supra*, §X(A)(1)(1[c]). Annotated Figures 12K and 8 below disclose these features:





202. In addition, as shown in annotated Figure 24 below, Kamoshima teaches via 4a and dummy via 4c connected to interconnection layer 3 (TSMC-1009, Fig. 24):

FIG.24



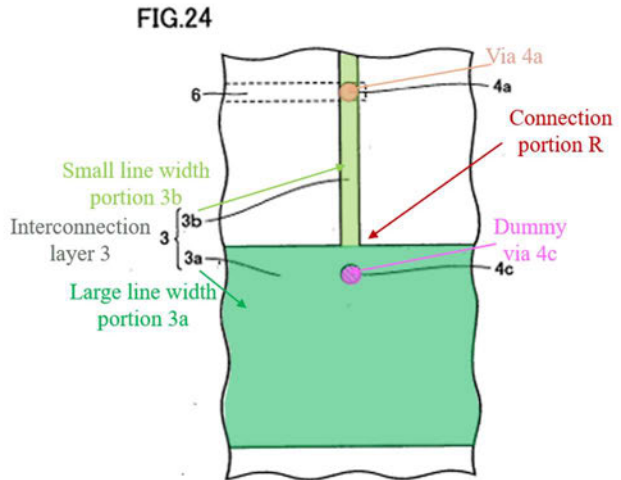
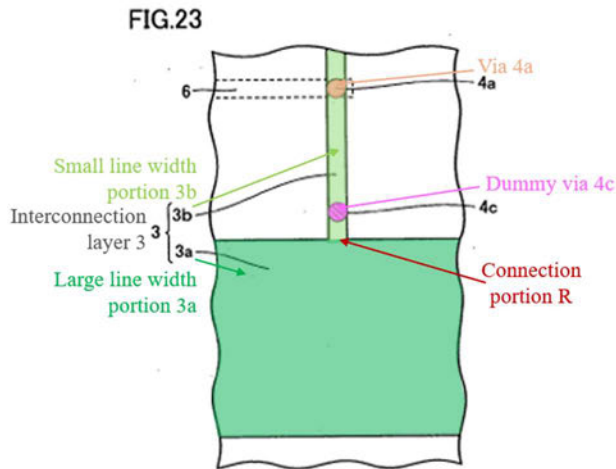
203. Thus, a POSITA would recognize that the via holes (e.g., via holes 38a, 68a) and the dummy hole (e.g., dummy via holes 38b, 68b) would be connected to the interconnect trench (e.g., wiring trenches 28a, 69a) with its modified shape according to Kamoshima and would have expected success in making such a structure.

204. It was obvious to combine Kamoshima and Watanabe's teachings such that Watanabe's via and dummy vias were similarly located and connected to the interconnect trench. *See also supra*, §X(B)(1)(3[a]). As discussed above, Kamoshima motivates the POSITA to arrange a real via on the narrow branch and the dummy via near a branchpoint between the narrow and wide portions of the interconnect, to further suppresses void concentrations under the real via due to

stress migration. TSMC-1009, ¶[0098]. As such, the combination of Watanabe and Kamoshima renders element 3[b], and indeed the entirety of claim 3, obvious.

2. **Claim 4 - *The method of claim 3, wherein in the step (c) the dummy hole is connected to the branch point between the first and second interconnect trench portions or to the interconnect trench near the branch point.***

205. Kamoshima discloses that the dummy hole (e.g., hole associated with dummy via 4c) is connected to the branch point between the first and second interconnect trench portions (e.g., grooves similar to grooves 1a, 1b associated with “interconnection portion with a large line width 3a” and “interconnection portion with a small line width 3b”) or to the interconnect trench near the branch point (e.g., “connection portion R”). TSMC-1009, ¶¶[0094]-[0095], [0099] (“Even when dummy via 4c is arranged on interconnection layer with a large line width 3a as shown in FIG. 24, an effect as described above can be attained, **so long as dummy via 4c is arranged in the vicinity of connection portion R of interconnection portion with a large line width 3a and interconnection portion with a small line width 3b.**”), Figs. 23-24. Annotated Figures 23 and 24 below disclose the dummy hole, branch point, and first and second interconnect trench portions, illustrating that the dummy hole is connected to the interconnect trench at least near the branch point:



206. Once again, as discussed above, a POSITA would have been motivated to place the dummy via (and thus associated dummy hole) in this location to suppress the concentration of voids in the area under the real via that is due to stress migration. A POSITA would have found locating the dummy vias (and thus dummy holes) in this location simple and routine, as it would utilize the same processing steps already disclosed in Watanabe as further discussed above and, therefore, would have expected success.

207. Accordingly, when modified to include the interconnect and via configuration of taught in Kamoshima, Watanabe would satisfy claim 4. Thus, the combination of Kamoshima and Watanabe renders claim 4 obvious.

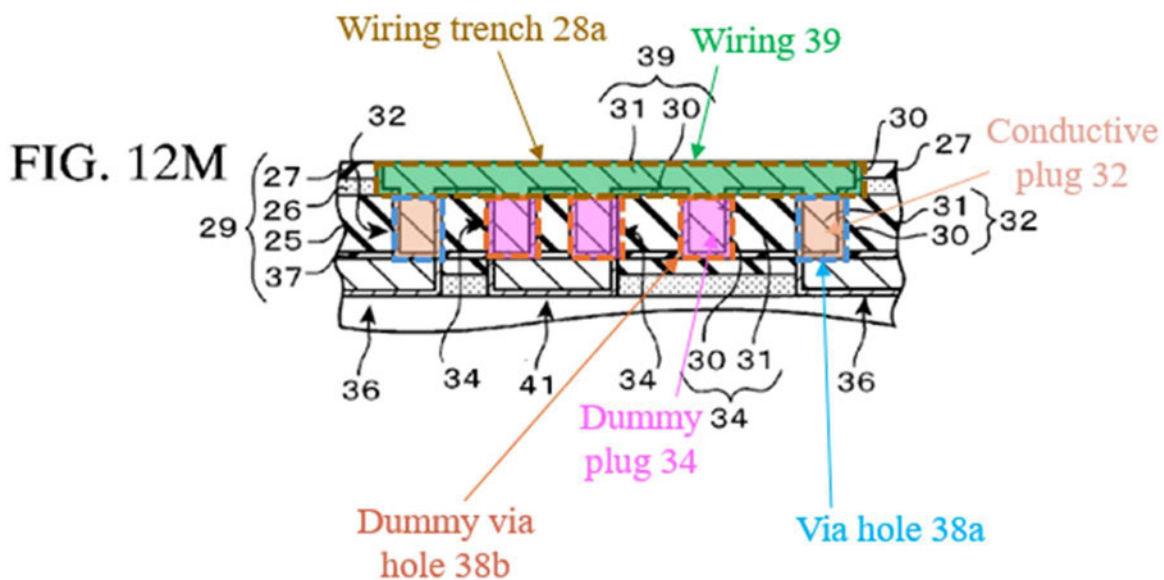
3. Claim 15

[15a] The method of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first

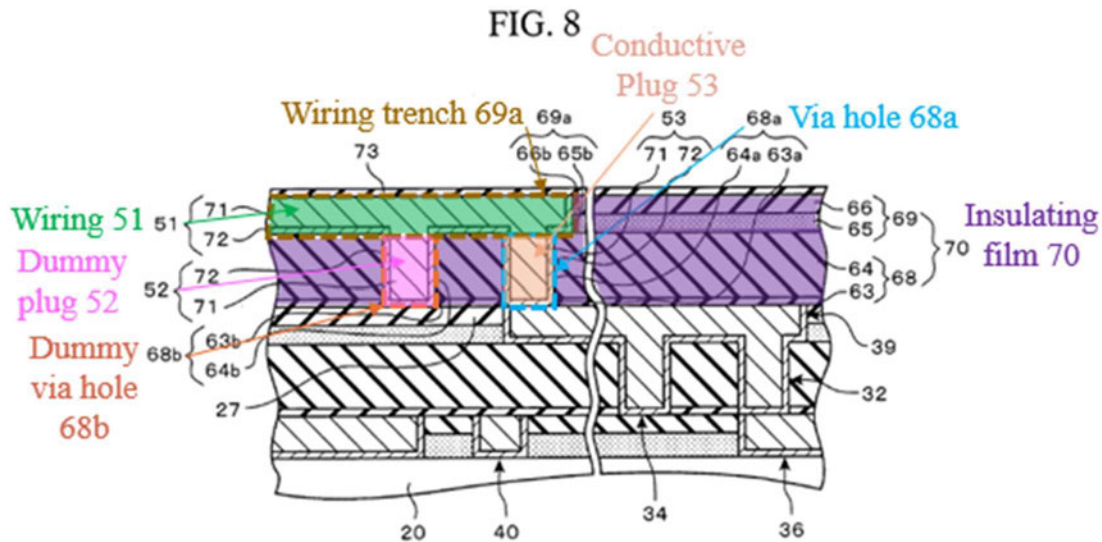
interconnect portion and which branches from the first interconnect portion, and

208. Claim 15 basically recites that the second interconnect (once formed in the trench described in claim 3) has the same shape as the trench of claim 3, which clearly would be the case given that the trench defines the shape of the ultimate interconnect. Thus, the same analysis from claim 3 applies to claim 15.

209. As discussed previously, the first through third and fifth embodiments of Watanabe disclose forming a second interconnect (e.g., “second wiring 39,” “third wiring 51”). *Supra*, §X(A)(1)(1[d]). See annotated Fig. 12M below:



Additionally, Watanabe’s fifth embodiment discloses forming a second interconnect (e.g., “third wiring 51”). *Supra*, §X(A)(1)(1[d]). See annotated Fig. 8 below:



210. Element 15[a] further defines a specific shape of the “second interconnect,” specifically that “the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion.” Kamoshima discloses a similarly shaped interconnect (e.g., “interconnection layer 3” having an “interconnection portion with a large line width 3a” and an “interconnection portion with a small line width 3b”). TSMC-1009, ¶¶[0094]-[0103], Figs. 23-27.

211. For example, in Figures 23-27, Kamoshima discloses various possible shapes in which interconnection layer 3 may be formed, including shapes corresponding to the interconnect configuration recited in claim 15 in which a narrower portion (e.g., “interconnection portion with a small line width 3b”)

branches off a wider portion (e.g., “interconnection portion with a large line width 3a”) (see *id.*, ¶¶[0094]-[0103], Figs. 23-27):

FIG.23

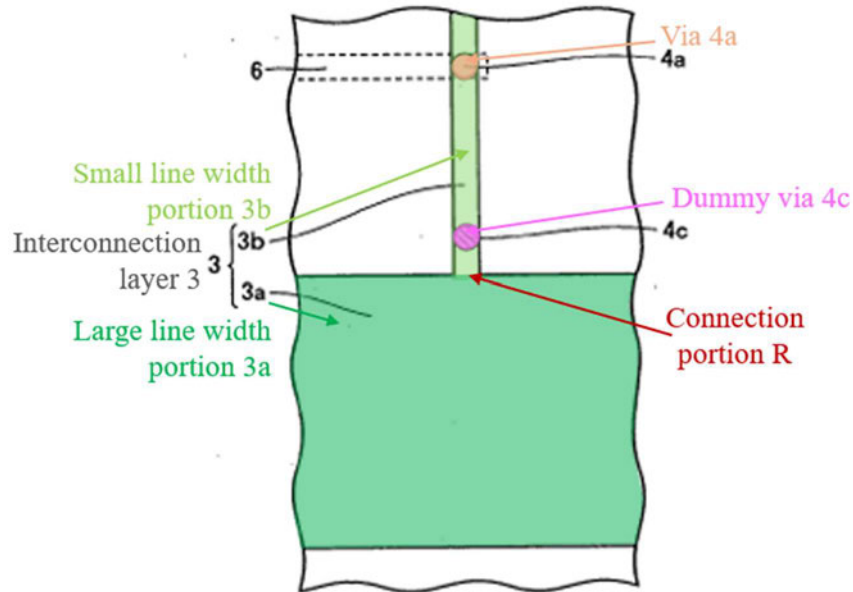
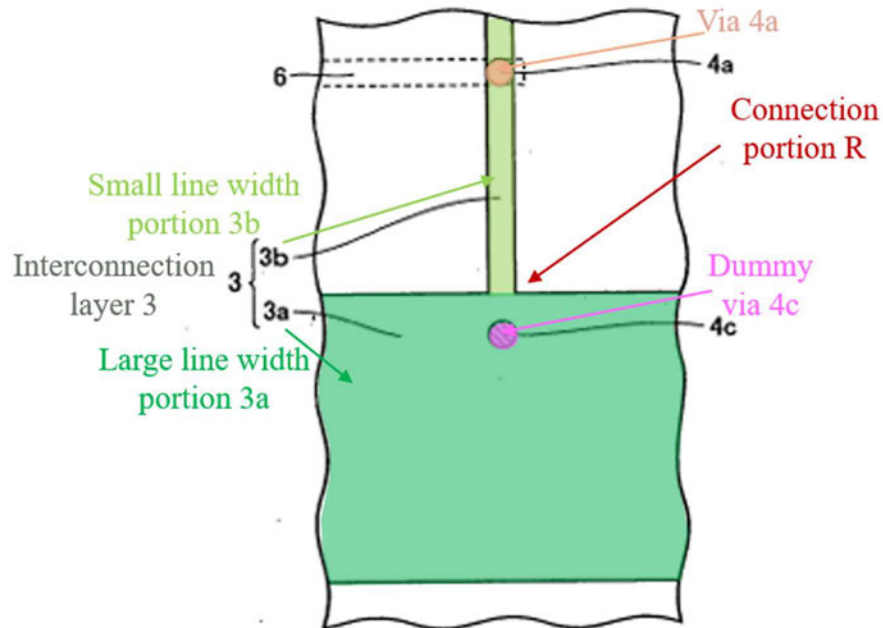


FIG.24



212. It was obvious for Watanabe's second interconnect (e.g., "second wiring 39" in the first through third embodiments; "third wiring 51" in the fifth embodiment) to be similarly shaped so as to have a branched configuration with a narrower portion extending from a wider portion similar to Kamoshima's "interconnection layer 3" from any of Figures 23-27 for the same reasons discussed above for claim 3. *Supra*, §X(B)(1).

213. Accordingly, a POSITA would have found it obvious in view of Kamoshima to modify the shape of Watanabe's second interconnect such that "the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion," thereby satisfying element 15[a].

214. A POSITA would have been motivated to combine the teachings of Watanabe and Kamoshima because the references address the identical problem of stress-induced voiding with complementary solutions that operate on different scales. Watanabe teaches a global approach, using dummy conductive plugs to reduce overall stress across the interconnect area. Kamoshima's use of a small line width portion (3b) provides a local, targeted protection for the most vulnerable point—the functional via—by creating a bottleneck to prevent voids from reaching it. A POSITA would have found it obvious to apply Kamoshima's geometric protection

to Watanabe's structure to create a more robust design that benefits from both the global stress relief of Watanabe and the targeted via protection of Kamoshima.

215. Furthermore, a POSITA would have had a reasonable expectation of success in this combination, as the two approaches are complementary and leverage standard, well-understood fabrication techniques. The benefits would be seen as additive; a skilled artisan would expect Watanabe's dummy plugs to continue to provide global stress relief in the wide interconnect portion, while simultaneously expecting Kamoshima's narrow bottleneck to effectively isolate the functional via from void migration.

[15b] the via is connected to the second interconnect portion.

216. Claim 15 basically recites that the second interconnect (once formed in the trench described in claim 3) has the same shape as the trench of claim 3 (including the same via connection locations), which obviously would be the case given that the trench defines the shape of the ultimate interconnect. Thus, the same analysis from limitation 3[b] applies to claim 15[b].

217. Kamoshima discloses that the via (e.g., "via 4a") is connected to the second interconnect portion (e.g., "interconnection portion with a small line width 3b"). TSMC-1009, ¶¶[0095] ("Interconnection layer 3 includes an interconnection portion with a large line width 3a, and an interconnection portion with a small line width 3b. Interconnection layer 6 is electrically **connected to interconnection**

portion with a small line width 3b of interconnection layer 3 through via 4a.”),

[0098], Figs. 23-24.

FIG.23

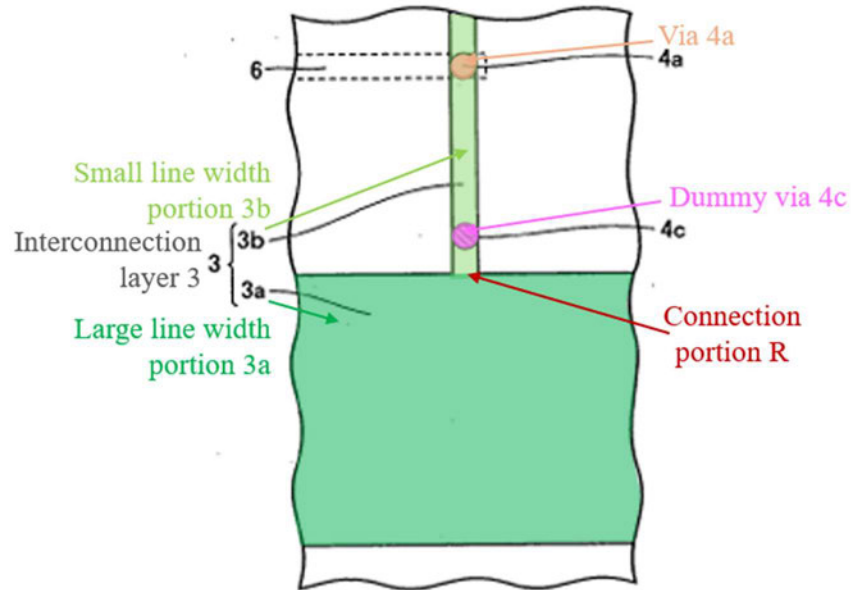
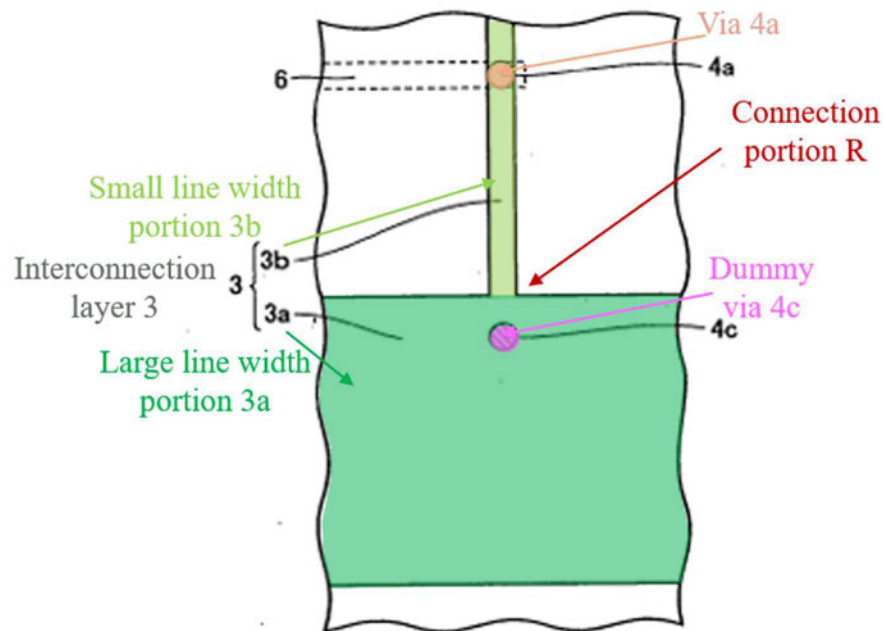


FIG.24



218. For the same reasons discussed above for element 3[b], it was obvious to connect Watanabe's real via (e.g., conductive plug 32, conductive plug 53) to the second, narrow interconnect portion when Watanabe was modified to include the branched shape for the second interconnect as taught in Kamoshima. Indeed, a POSITA was motivated to do so to achieve the benefit of suppressing the concentration of voids due to stress migration. *See* TSMC-1009, ¶¶[0097]-[0098], [0105], [0109], [0111].

219. For example, the functional vias (conductive plugs 32, 53) in the combination would be connected to the small line width portion for the specific reason disclosed in Kamoshima: to protect the via from stress-induced voiding. Kamoshima identifies that a primary cause of this type of failure is the migration of microvoids from a large area interconnect portion, which acts as a large reservoir for such defects. The solution taught by Kamoshima is to physically isolate the functional via from this large reservoir. Therefore, placing Watanabe's functional via on this narrow portion directly applies Kamoshima's protective teaching, using the geometry to starve the critical area under the via from the main source of failure-causing voids.

220. A POSITA would have found such a modification of Watanabe easy to implement and thus would have expected success, as it would merely involve selecting the location of the via/plug such that it was located in the narrow

interconnect portion, and forming the via/plug using the same processes already taught in Watanabe.

221. As such, the combination of Watanabe and Kamoshima renders element 15[b], and indeed the entirety of claim 15, obvious.

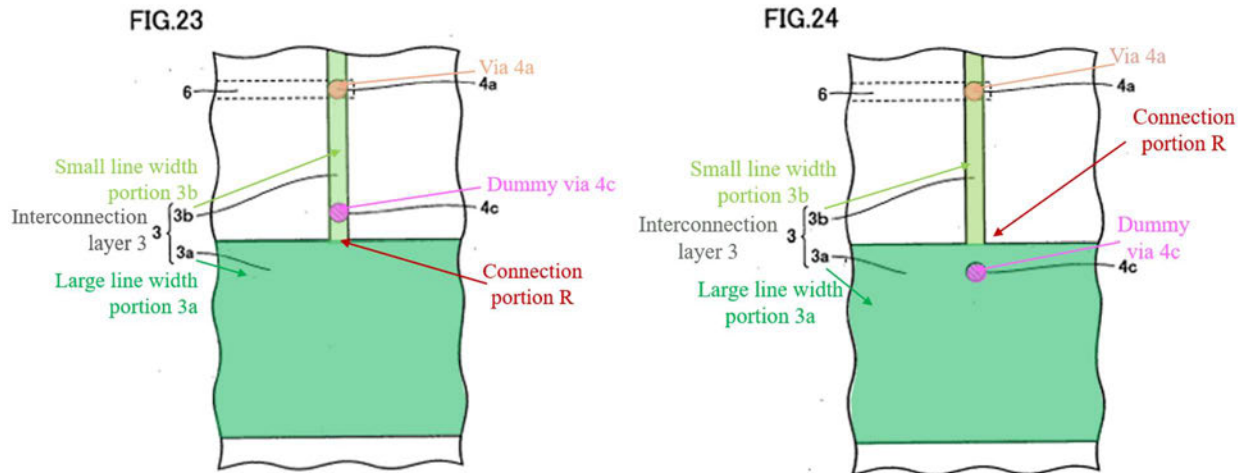
4. Claim 16 - *The method of claim 15, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions.*

222. Claim 16 basically recites that the second interconnect (once formed in the trench described in claim 4) has the same shape and dummy via connections/locations as described with respect to the trench and dummy hole of claim 4, which obviously would be the case given that the trench and dummy hole define the shape of the ultimate interconnect and location of the dummy via, respectively. Thus, the same analysis from claim 4 applies to claim 16.

223. Kamoshima discloses that the dummy via (e.g., dummy via 4c) is formed at or near the branch point (e.g., “connection point R”) between the first and second interconnect portions (e.g., point at the intersection of “interconnection portion with a large line width 3a” and “interconnection portion with a small line width 3b”). TSMC-1009, ¶[0099] (“Even when dummy via 4c is arranged on interconnection layer with a large line width 3a as shown in FIG. 24, an effect as described above can be attained, so long as dummy via 4c is arranged in the

vicinity of connection portion R of interconnection portion with a large line width 3a and interconnection portion with a small line width 3b.”), Figs. 23-24.

Annotated Figures 23 and 24 below disclose the dummy via 4c at or near the branch point (e.g., “connection point R”):



224. For the same reasons discussed for claims 3 and 4, a POSITA would have been motivated to place the dummy via in this location to suppress the concentration of voids in the area under the real via that is due to stress migration. A POSITA would have found locating the dummy vias in this location simple and routine as discussed above as it would simply utilize standard processing techniques at the time including those already disclosed in Watanabe, and, thus, would have expected success.

225. Kamoshima explains a technical reason for placing the dummy via at or near the branch point, teaching that a large number of microvoids from the wide interconnect (3a) will concentrate under the dummy via (4c) before they can reach

the functional via (4a), thereby improving reliability. This establishes the dummy via's role as a "void trap." A POSITA, having already combined Watanabe and Kamoshima to arrive at the structure of claim 15, would then look to Kamoshima for guidance on optimizing the placement of Watanabe's dummy via (dummy plug 34 or 52) and would be directly taught to place it at or near the branch point to achieve this specific void-trapping benefit.

226. Accordingly, when modified to include the interconnect and via configuration of taught in Kamoshima, Watanabe would satisfy claim 16. Thus, a POSITA would have found claim 16 obvious in view of the combination of Kamoshima and Watanabe.

C. Ground 3: Watanabe combined with Kamoshima and Fukazawa renders Claim 17 unpatentable

227. I believe claim 17 is obvious over Watanabe in view of Kamoshima and Fukazawa as discussed below.

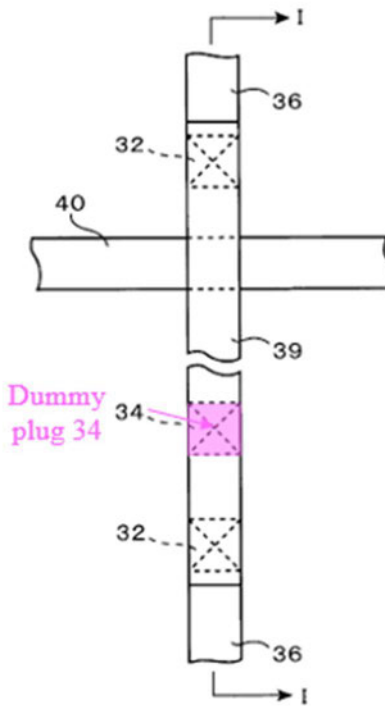
1. Claim 17 - *The method of claim 15, wherein the dummy via is substantially rectangular in a plan view, and a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction*

228. The combination of which Watanabe, Kamoshima, and Fukazawa renders claim 17 obvious.

[17.a] – “wherein the dummy via is substantially rectangular in a plan view”

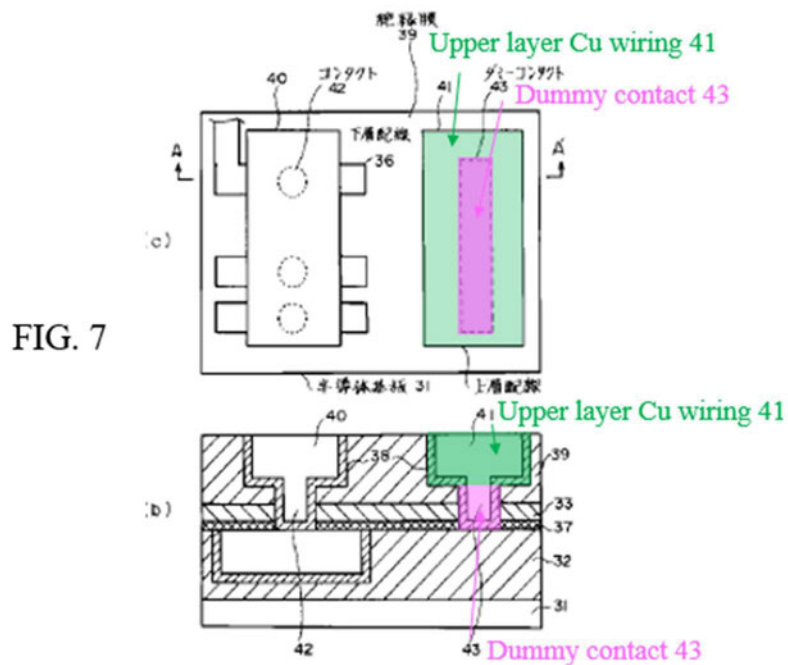
229. As discussed previously *supra*, §X(A)(7), Watanabe discloses dummy plugs 34/52 that are substantially square (TSMC-1004, Figs. 2, 4, 9), such as in annotated Figure 2 below:

FIG. 2



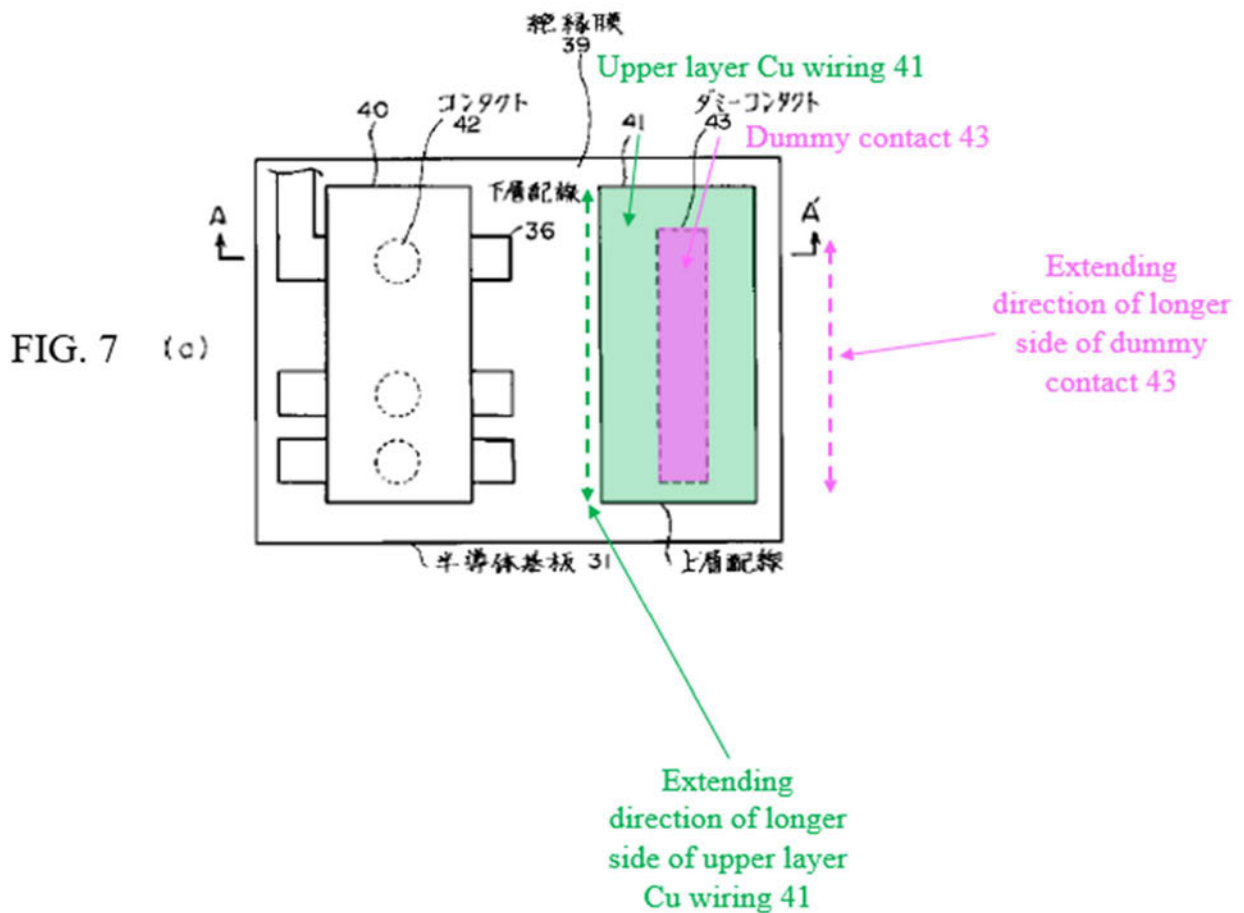
230. A POSITA would recognize that Fukazawa discloses a dummy via (e.g., “dummy contact 43” and “barrier metal layer 38,” hereafter collectively “dummy contact 43”) connected to an upper layer interconnect (e.g., “upper layer Cu wiring 41” and “barrier metal layer 38,” hereafter collectively “upper layer Cu wiring 41”). TSMC-1010, ¶[0017], Fig. 7. A POSITA would understand

Fukazawa's dummy contact 43 to be a dummy via, both because of its label as a "dummy" structure and because of its configuration within Fukazawa's device. Specifically, dummy contact 43 is connected to an upper layer interconnect (e.g., "upper layer Cu wiring 41") but not connected to a lower layer or second interconnect, and thus would be capable of current flow. TSMC-1010, ¶[0017], Fig. 7. To enhance mechanical strength, Fukazawa's dummy contact 43 is arranged in a substantially rectangular shape (which Fukazawa describes as "column-shaped") in a plan view. *Id.*, ¶[0017]-[0018] ("the dummy contacts are column-shaped"), Fig. 7. The rectangular shape of Fukazawa's "dummy contact 43" in a plan view is clearly disclosed in annotated Figure 7 below (*see id.*, ¶[0017]-[0018], Fig. 7):



[17.b] – “a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction”

231. Fukazawa discloses a longer side of the rectangular dummy contact/via 43 is provided along a same direction as a longer side of a correspondingly rectangular interconnect (“upper layer Cu wiring 41”). TSMC-1010, ¶¶[0017]-[0018], Figure 7. This is disclosed in annotated Figure 7 below:

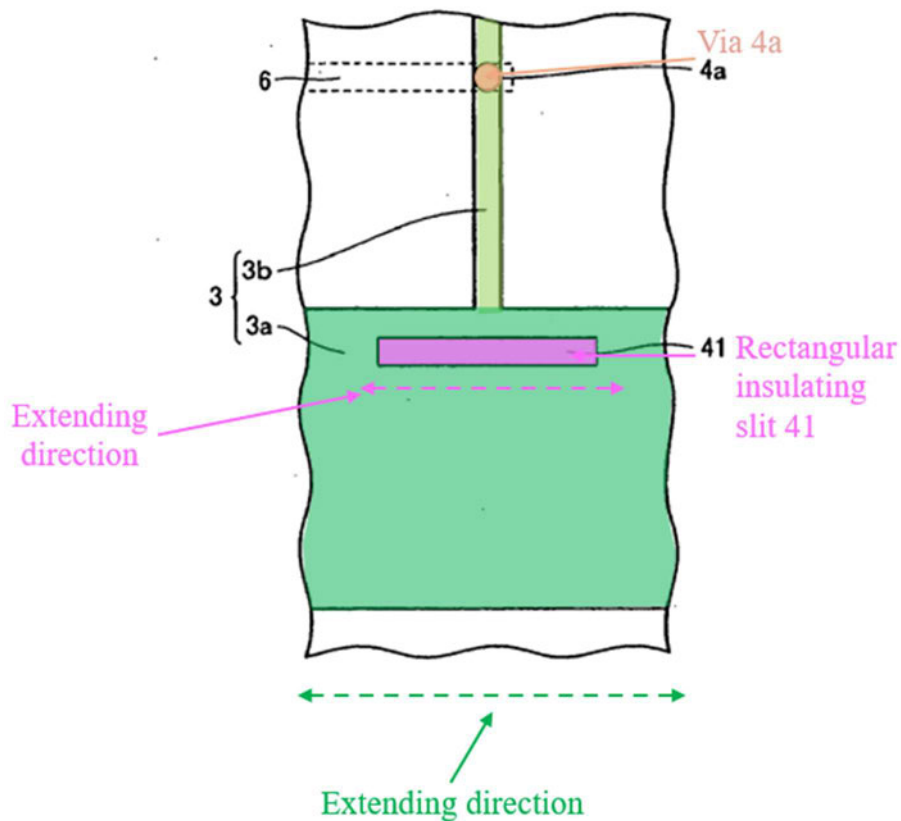


Obviousness of Combining Watanabe, Kamoshima, and Fukazawa

232. In view of Fukazawa, it was obvious to a POSITA at the time to use a rectangularly-shaped via (e.g., shaped similarly to Fukazawa's dummy contact 43) in the wider first interconnect portion of Watanabe's second interconnect (after it was modified in view of Kamoshima to have a branched interconnect structure – *see supra*, §X(B)(1), (3)). Following Fukazawa's teaching of rectangular-shaped vias and Kamoshima's teaching of a branched interconnect structure, a POSITA would have been motivated to use the rectangularly-shaped via and to position it along a longer side of the wider portion of the branched interconnect to further reduce the migration of vacancies to (and thus the formation of voids within) a real, functional via positioned on the narrow branch of the interconnect. Indeed, as discussed previously *supra*, §IX(A), Watanabe already seeks to address stress-induced vacancy migration and thus a POSITA seeking to improve Watanabe's design would have looked to additional known ways of addressing this issue.

233. Kamoshima teaching using a rectangular structure (e.g., insulating slit 41) positioned in the claimed manner (a longer side extending in a same direction as a longer side of the wider interconnect portion) and for the express reason of suppressing migration of vacancies to via 4a (*see* TSMC-1009, ¶¶[0102]-[0105], Fig. 25):

FIG.25



234. A POSITA understood that positioning a rectangular dummy via in the same position as insulating film 41 would have similarly suppressed vacancy migration (similar to dummy vias 4c in Kamoshima's Figure 23-24 embodiments), with the added benefit of providing a larger area of vacancy interception due to the rectangular shape and its position along a length of the wider portion of the interconnect (and thus perpendicular to the narrow branch portion). Indeed, by virtue of the ends of the rectangular slit expanding well beyond the width of the narrow branching portion, a more tortuous path is created by which vacancies would

need to travel to get to functional via 4a, thus reducing the number of vacancies that reach via 4a.

235. Additionally, a POSITA would have been motivated by the increased mechanical strength afforded to the overall wiring structure by the rectangular (i.e., column-shaped) dummy via. Indeed, Fukazawa expressly notes that such a shaped-via increases the mechanical strength of the structure. TSMC-1010, ¶¶[0017]-[0018] (“the dummy contacts are column-shaped like the contacts, but the dummy contacts are not connected to the lower layer wiring or the semiconductor substrate.... [T]he contacts are column-shaped, and the column-shaped bodies are plate-shaped bodies that are connected continuously. Because of this structure, sufficient mechanical strength is ensured even when the insulating film comes off, thereby improving the strength of the wiring structure”).

236. A POSITA would have found such a modification, which merely changes the shape and relative locations of via and an interconnect to which it is connected, to have had a reasonable expectation of success. Indeed, as described above, a POSITA was clearly capable of creating a branched interconnect. The additional elements of claim 17 merely require that a dummy via be constructed with a rectangular shape and connected to the wider interconnect portion in the same relative position as insulating slit 41 in Kamoshima’s Figure 25 embodiment. This would have been easily and reliably accomplished using standard processing

techniques at the time. Indeed, prior to the '751 patent rectangular vias were well-known and used and positioning them where desired was easily achievable. This is demonstrated by numerous references pre-dating the '751 patent that describe the interchangeable use of various via shapes. *See* TSMC-1008, 9:45-47 (“It will be also understood that the opening of the via-hole may have any configuration, such as a square, rectangle or circle.”); TSMC-1013, 9:45-49, 10:1-4 (“[D]ummy via holes of only rectangles or lines may also be formed.”).

237. Thus, claim 17 was obvious over the combination of Watanabe, Kamoshima, and Fukazawa.

D. Ground 4: Watanabe combined with Iizuka renders Claim 9 unpatentable

238. I believe claim 9 is obvious over Watanabe in view of Iizuka as discussed below.

1. Claim 9 - *The method of claim 1, wherein the via and the dummy via are substantially circular in a plan view.*

239. Claim 9 recites that “the via and the dummy via are substantially circular in a plan view,” which Watanabe in view of Iizuka renders obvious.

240. As discussed above, Watanabe discloses both vias (e.g., “plug 32”) and dummy vias (e.g., “dummy plug 34”). *Supra*, §X(A)(1)(1[d]). Watanabe’s plan view figures disclose square vias and dummy vias. Watanabe also discloses a

simulation model with plug 32 (“via”) and dummy plug 34 (“dummy via”) as a “circular cylinder,” i.e., disclosing them to the POSITA as substantially circular in plan view. TSMC-1004, ¶[0083], Figs. 1, 3. A POSITA would recognize that the same applies to dummy plugs 52 in all of Watanabe’s embodiments. *E.g., id.*, Fig. 9. Disclosing the circular cylinder shape for its simulation model suggests circular vias to a POSITA for Watanabe’s devices, since this is the shape on which Watanabe’s modeling was done. A POSITA would thus interpret Watanabe as disclosing vias having circular cross-sections in plan view, in addition to the square vias disclosed in the figures.

241. Like Watanabe, Iizuka is directed to a “semiconductor device” in which “via-holes” are formed. *See* TSMC-1008, Abstract. Iizuka demonstrates that it was well-known prior to the ’751 patent that vias could have many polygonal cross-sectional shapes and that the selection of a specific shape was simply a design choice. For example, Iizuka teaches the common nature of circular via-holes and the interchangeability with other common shapes such as squares: “the opening of the via-hole may have any configuration, such as a **square**, rectangle **or circle**.” *Id.*, 9:45-47 (emphasis added); *see also id.*, 6:60-63, Fig. 5A (disclosing “diameter” of via, which given the common understanding of “diameter” as a standard geometrical term describing the distance around a circle further illustrates the use of circular vias).

242. Thus, a POSITA understood that circular shaped vias were common, as evidenced by Iizuka, and would have understood that the dummy plug 34 in Watanabe could be made to be substantially circular in a plan view. *See also*, TSMC-1005, ¶[0200], Fig. 19A (showing circular-shaped dummy vias 125); TSMC-1013, 8:47-52 (noting that circular vias may be used, among other shapes). Indeed, Igarashi teaches circular vias as the default shape for all via connections, except where square vias or other shapes are needed for a given overlap of the upper and lower interconnects. TSMC-1014, ¶¶[0091]-[0092], Figs. 8, 14 (teaching circular vias as a default shape, and square vias as preferred for certain interconnect junctions). Thus, a POSITA would have viewed the square and circular shapes as among a finite number of common, interchangeable design choices, expressly taught by Iizuka and within a POSITA's general understanding.

243. In addition, particular via shapes, such as square or circular, each provide known advantages applicable to a given situation. For example, circular vias can provide for greater manufacturing process control (e.g., more uniform etching and filling characteristics for circular shapes compared to sharp-cornered squares), more favorable stress distribution around a circular opening, and design simplicity. *See, e.g.*, TSMC-1014, ¶¶[0091]-[0092], Figs. 8, 14; TSMC-1038, 7:62-67 (teaching that vias having circular cross-sections benefit from more precisely controlled etching, improved coverage of barrier metal in the via opening, and easier

fill-in of the via opening with a metal film). Circular-shaped vias also provide improved reliability due to the lack of sharp corners that can concentrate stress and cause damage in the form of dielectric cracking and the like.

244. While there can sometimes be operational or design considerations that lead to a preference for circular or square vias, a POSITA nonetheless recognized that the fundamental stress-relieving function of Watanabe's dummy via (or the electrical connection function of Watanabe's via) in terms of attracting and sequestering vacancies and providing a surplus of copper atoms, would be essentially the same with both circular and square dummy vias. That is because these functions do not depend on the exact cross-sectional shape of the dummy via. In this regard, I note that the '751 patent teaches no criticality or surprising or unexpected results with respect to the cross-sectional shape of its vias or dummy vias, reinforcing my opinion that such shapes were nothing more than a matter of routine design choice.

245. Further, because a POSITA was aware of these shapes, and was aware of the role of the dummy vias in addressing stress-induced voiding and electromigration problems as taught, for example, by Watanabe (*supra*, §IX.A), it would have been a matter of routine optimization to choose the via shape that works best for a given overall design. With a few basic shapes to choose from (e.g., circular, square, rectangular), it would not have required an undue amount of

experimentation to arrive at the optimal via shape. Thus, it was obvious to make both plugs 32 and dummy plugs 34 of Watanabe substantially circular, as such a shape was merely one of a finite number of known, optional shape configurations for such vias/plugs.

246. A POSITA understood that there was no criticality associated with having a circular via or dummy via shape and that such circular-shaped vias would have operated substantially the same as other shapes. That is, there was no surprising or unexpected performance benefit associated with circular vias as opposed to other shaped-vias. Any difference in performance was well understood and something that a POSITA would have balanced with other considerations (such as manufacturing limitations, costs, etc.) when choosing the appropriate shape for the functional and dummy vias for a given application.

247. A POSITA would have had a reasonable expectation of success in implementing such circularly-shaped vias and dummy vias. Indeed, as demonstrated by Iizuka (and other references at the time) as well as the modeling of Watanabe, circular vias (including dummy vias) were routinely used in semiconductor devices and thus their fabrication was well understood. *See* TSMC-1005, Fig. 19A; TSMC-1014, ¶[0091]; TSMC-1013, 8:47-52; TSMC-1038, 7:62-67. Thus, a POSITA would not have expected any significant hurdles or problems when implementing such a shape.

E. Ground 5: Hasunuma anticipates Claims 1, 5-6, 9, 11-14, and 18-19

248. I believe that Hasunuma discloses all the elements of each of claims 1, 5-6, 9, 11-14, and 18-19 as discussed below.

1. Claim 1

1[pre] “A Method for Fabricating a Semiconductor Device”

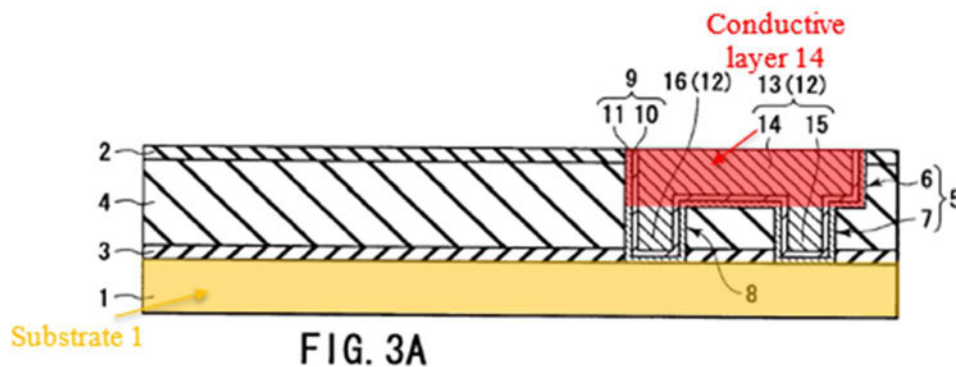
249. Hasunuma is directed to a “method for manufacturing” a semiconductor device (i.e., a “method for fabricating”), and thus satisfies claim 1’s preamble. TSMC-1005, Abstract, ¶[0088], Figs. 1A-8.

1[a] “Forming a First Interconnect”

250. Hasunuma discloses forming a first interconnect (e.g., “conductive layer 14” and “barrier metal film 9,” hereinafter collectively “conductive layer 14”) on a semiconductor substate (e.g., “Si substrate 1”). TSMC-1005, ¶¶[0094]-[0098], Figs. 2A-3A. Hasunuma describes its interconnects using the term “conductive layer” (e.g., “conductive layer 14,” “conductive layer 26”). A POSITA understood that such conductive layers constitute “interconnects” as those terms are understood in the art because Hasunuma’s conductive layers are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:21-28. Conductive layers/interconnects on different levels can be electrically connected by

vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:37-39.

251. Hasunuma forms conductive layer 14, comprising barrier metal film 9 and copper film 12, within an insulating stack that is deposited over the silicon substrate 1. TSMC-1005, ¶[0098], Figs. 3A, 8. The resulting conductive layer 14 is thus formed on the semiconductor substrate to form the claimed “first interconnect,” as seen below:

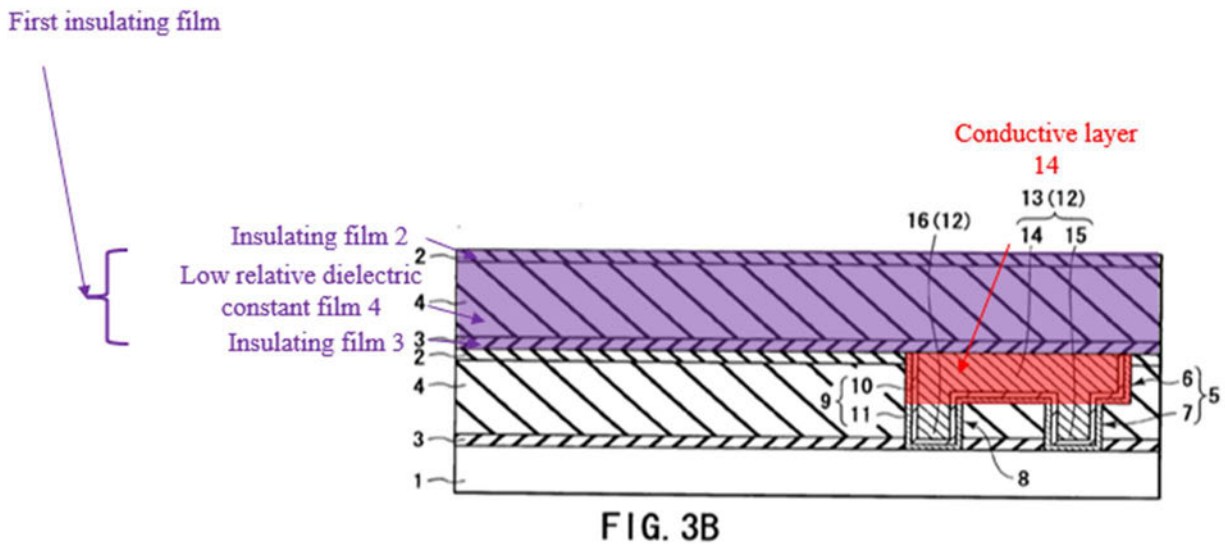


252. More specifically, Hasunuma explains that “Si substrate 1 is conveyed in high vacuum so as to prevent the Si substrate 1 in which the barrier metal film 9 is formed from being exposed to the atmosphere, and is fed into a treatment chamber of a sputtering device (not shown) for forming a plating seed layer (film) 12a which is a base (substrate) of the conductive layer 14. Thereafter, materials forming the conductive layer 14, conductive plug 15, and first reinforcing plug 16 are provided on the surface of the Ta film 10.” TSMC-1005, ¶[0096]. “As a result, to

extend over the SiCN film 3 of the first layer from the SiC film 2 of the first layer, the Cu wiring layer 13 of the first layer including the Cu conductive layer 14 and Cu conductive plug (Cu conductive contact plug) 15, and the first reinforcing plug 16 of the first layer are formed.” *Id.*, ¶[0098], Fig. 3A.

1[b] “Forming a First Insulating Film”

253. Hasunuma forms an insulating film (i.e., “first insulating film”) on the second level of its device, which comprises insulating films 3, 4 (a low dielectric constant film), and 2, all successively stacked on conductive layer 14 (*id.*, ¶[0100], Fig. 3B):



254. Hasunuma thus discloses forming a first insulating film (e.g., the combination of “SiCN film 3”/“low relative dielectric constant film 4”/“SiC film 2”) on the first interconnect (e.g., “conductive layer 14”). TSMC-1005, ¶[0100], Fig. 3B. Hasunuma explains that “on the SiC film 2 and Cu wiring layer 13 [which

includes “conductive layer 14”] of the first layer, the SiCN film 3, the low relative dielectric constant film 4, and the SiC film (capping layer of a second layer) 2 of the second layer are successively stacked.” *Id.*, ¶[0100]. A POSITA would understand each of SiCN film 3, the low relative dielectric constant film 4, and the SiC film (capping layer of a second layer) 2 (as well as any films that may be substituted for these particular films) to be insulating films. Indeed, Hasunuma expressly refers to films 2, 3, and 4 as “insulating films.” *See id.*, ¶¶[0090]-[0091] (“as shown in FIG. 1A, on a silicon substrate (semiconductor substrate) 1 in which an active area and underlayer wiring comprising various electronic circuits (not shown) are formed, an insulating film 3, interlayer insulating film (inter-level dielectrics: ILD) 4, and another insulating film 2 are successively stacked. Concretely, first on the surface of the Si substrate 1, for example, a CVD process is used to deposit the insulating film 3 whose Young's modulus is about 30 GPa or more in a film thickness of about 50 nm. This insulating film 3 functions as a first reinforcing film (reinforcing material), and in the present embodiment, for example, an SiCN film is employed as the insulating film 3. Subsequently, on the surface of this SiCN film 3, the CVD process is used to deposit the interlayer insulating film 4....”). A POSITA would further recognize that any individual one of the constituent layers 2-4 of this combination (or any sub-combination of layers 2-4) also satisfies the “insulating film” element of this limitation.

1[c] “Forming In the First Insulating Film, a Via Hole, a Dummy Hole and an Interconnect Trench”

255. Hasunuma discloses forming in the first insulating film (e.g., the combination of “SiCN film 3,” “low relative dielectric constant film 4,” “SiC film 2”), a via hole (e.g., “recess [for conductive plug] 19”) connected to the first interconnect (e.g., “conductive layer 14”/“wiring layer 13”), a dummy hole (e.g., “recess [for the first reinforcing plugs] 20”) which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench (e.g., “recess [for the conductive layer] 18”) connected to the via hole and the dummy hole. TSMC-1005, ¶¶[0101]-[0104], Fig. 4. Hasunuma explains that “a recess for the wiring layer 17 of the second layer is formed for forming a conductive layer 26 and conductive plug 27 of the second layer described later.” TSMC-1005, ¶[0101]. “[R]ecess 17 is formed in the two-stage structure including a **recess for the conductive layer 18** in the top and a **recess for the conductive plug 19** in the bottom.” *Id.* “[T]hree **recesses for the first reinforcing plugs 20** for forming the first reinforcing plugs 28 are formed integrally with the recess 18.” *Id.*, ¶[0103]. The various recesses are illustrated below in annotated Figure 4 of Hasunuma:

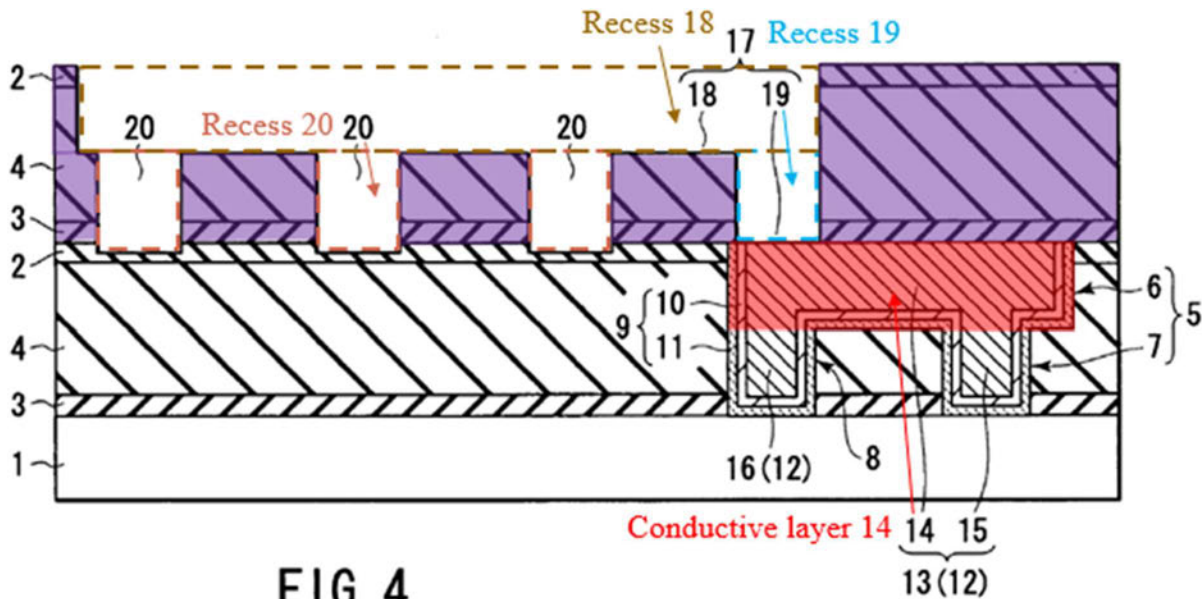


FIG. 4

256. “Recesses 20,” which are used to form “reinforcing plugs 28” discussed below, are “arranged so as to be incapable of having current flow therethrough.” Indeed, the structure and function of Hasunuma’s “recesses 20” matches the ’751 patent’s description of dummy components in which no current flows therethrough. *See supra*, §X(A)(1)(1[c]); TSMC-1001, 3:17-21, 10:42-48.

257. A POSITA would recognize that no current would flow through recesses 20 or the “reinforcing plugs 28” formed therein. These “dummy” recesses 20 and “dummy” reinforcing plugs 28 are only connected on one end to an active circuit element (i.e., “conductive layer 26”), while the other end is not connected to a second active circuit element. TSMC-1005, ¶[0104] (“there is no problem as long as each the recess 20 has a depth to such an extent that the first reinforcing plug 28 of the second layer formed in the recess 20 **is not electrically connected** to the essential

wiring layer (not shown) provided below the plug.”), Figs. 4, 8. Thus, a POSITA would recognize that the dummy recesses 20 and dummy plugs 28 do not constitute parts of a closed circuit in actual use of the device. Instead, current flows between Hasunuma’s conductive layer 14 and conductive layer 26 through conductive plug 27 (formed in recess 19), which constitute parts of a closed circuit in actual use of the device. *See* TSMC-1005, ¶[0101] (“In the same manner as the conductive layer 14 and conductive plug 15 of the first layer, the conductive plug 27 of the second layer is formed to be electrically connected to the conductive layer 26 of the second layer, and comprises the conduction path to be actually energized together with the conductive layer 26. That is, the conductive layer 26 and conductive plug 27 comprise a wiring layer (effective wiring layer) 25 which is actually energized to function as the essential wiring.”).

258. Moreover, Hasunuma’s device would still be operable if dummy recesses 20 and dummy plugs 28 were omitted, where current would still flow through the active circuit elements, i.e., conductive layers 14 and 26 and conductive plug 27, during actual use of the device.

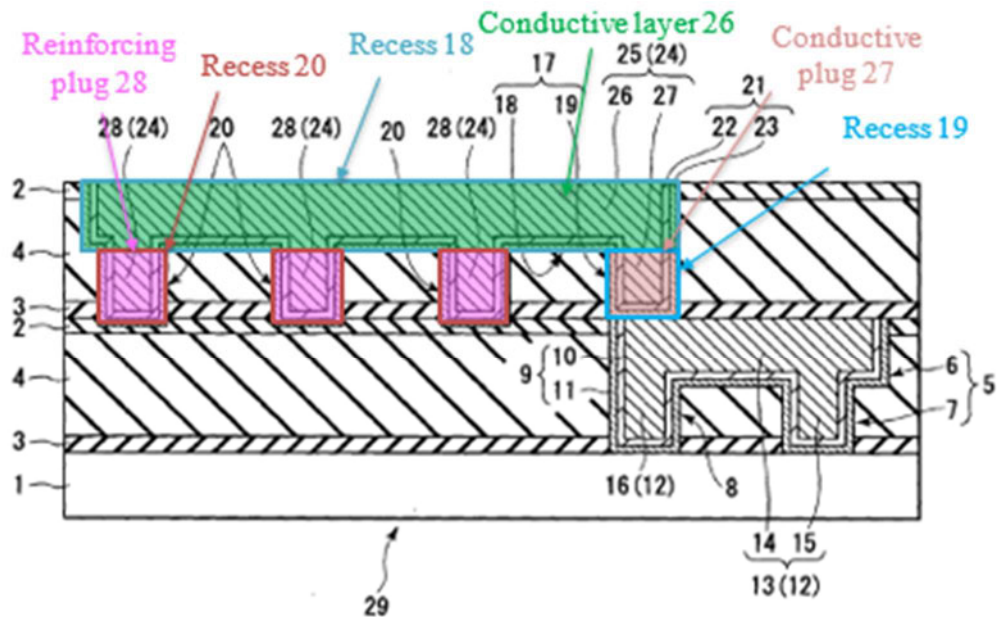
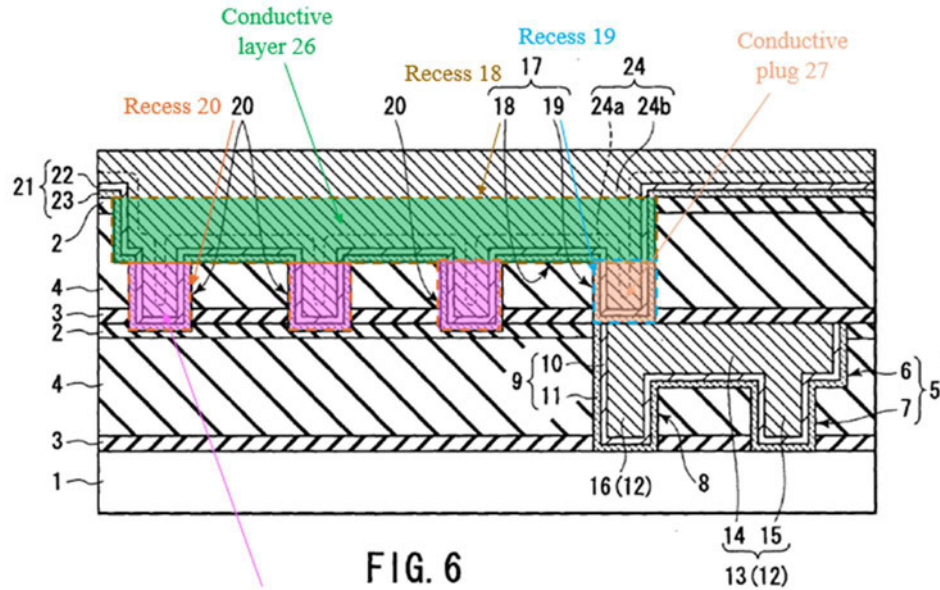
259. Thus, in addition to Hasunuma describing the reinforcing plugs 28 arranged in recesses 20 as “dummy” plugs (see TSMC-1005, ¶[0109]), a POSITA would have understood that recesses 20 are “arranged so as to be incapable of having current flow” because they do not constitute parts of a closed circuit in actual use of

the device and Hasunuma's device would still function even if the dummy recesses 20 were omitted.

260. Thus, Hasunuma satisfies limitation 1[c].

1[d] “Depositing a Conductive Material in the Via Hole, the Dummy Hole and the Interconnect Trench”

261. Hasunuma discloses depositing a conductive material (e.g., “Cu film 24” having “Cu plating seed layer 24a” and “Cu plating film 24b,” and “barrier metal film 21”) in the via hole (e.g., “recess 19”), the dummy hole (e.g., “recess 20”) and the interconnect trench (e.g., “recess 18”), thereby forming a via (e.g., “conductive plug 27” and “barrier metal film 21,” hereafter collectively “conductive plug 27”), a dummy via (e.g., “reinforcing plug 28” and “barrier metal film 21,” hereafter collectively “reinforcing plug 28”) and a second interconnect (e.g., “conductive layer 26” and “barrier metal film 21,” hereafter collectively “conductive layer 26”). TSMC-1005, ¶¶[0104]-[0110], Figs. 5-7. These features are disclosed below in annotated Figures 6 and 7 of Hasunuma:



262. Hasunuma explains that “as shown in FIG. 6, a Cu plating film 24b is provided on the surface of the Cu plating seed layer 24a. In the same manner as the Cu plating film 12b of the first layer, the Cu plating film 24b is formed using the

electrolytic plating process. The Cu plating film 24*b* is formed integrally with the Cu plating seed layer 24*a*. Accordingly, on the surface of the Ta film 22, a Cu film 24 of the second layer is formed which is the forming material of the conductive layer 26, conductive plug 27, and first reinforcing plugs 28.” TSMC-0105, ¶[0107].

263. Accordingly, Hasunuma satisfies each of the elements of claim 1.

2. Claim 5 - *The method of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film.*

264. Claim 5 recites “wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film,” which Hasunuma discloses.

265. Hasunuma’s first insulating film (e.g., combination of layers 2, 3, 4) has a multilayer structure including a SiN film and a SiO₂ film, thus satisfying claim 5. TSMC-0105, ¶[0299] (“instead of the SiC film 2, an SiO₂ film may also be used”; “instead of the SiCN film 3, an SiN film may also be used”).

266. The claimed “first insulating film” in Hasunuma can comprise the entire second-level insulating stack of insulating film 3, the low relative dielectric constant film 4, and insulating film 2, or a sub-combination of these layers. *Supra*, §X(E)(1)(1[b]). Hasunuma explicitly teaches that materials for these insulating layers can be substituted. *See* TSMC-1005, ¶¶[0091], [0293], [0299]. Specifically, Hasunuma states that “instead of the SiC film 2, an SiO₂ film may also be used” and “instead of the SiCN film 3, an SiN film may also be used.” *Id.*, ¶[0299]. Hasunuma

also discloses those substitutions in paragraph [0293], where Hasunuma teaches that for the films having a Young's modulus of 30 GPa or more, such as the SiCN film or SiC film, other materials can be used including SiN and SiO₂. *Id.*, ¶[0293]. Those films having a Young's modulus of 30 GPa or more are the SiCN film 3 and the SiC film 2, which are described by Hasunuma as having the Young's modulus of 30 GPa or more. *Id.*, ¶¶[0091]-[0092], [0100]. Applying these explicitly taught substitutions, the second-level insulating stack ("first insulating film") would comprise a SiN film (substituted for SiCN film 3) and an SiO₂ film (substituted for SiC film 2). *Id.*, ¶¶[0293], [0299]. This resulting multilayer stack serving as the claimed "first insulating film," thus includes both a SiN film and a SiO₂ film.

3. Claim 6 - *The method of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode.*

267. Claim 6 recites the "each of the first and second interconnects is connected to another element or an external electrode," which Hasunuma discloses.

268. A POSITA would understand that each of Hasunuma's first and second interconnects (e.g., "conductive layer 14" and "conductive layer 26") is connected to another element (e.g., "contact plug 15," "electronic circuit on substrate 1," and other active components of the active circuit formed together with the first and second interconnects) or an external electrode. Together "wiring layer 13" (which

includes first interconnect/“conductive layer 14”) and “wiring layer 25” (which includes second interconnect/“conductive layer 26”) form an “effective wiring area 29” that “actually functions as the wiring” of Hasunuma’s device. TSMC-1005, ¶[0110]. A POSITA understood that the wiring in such a semiconductor device includes a multitude of circuit elements connected together to form the wiring/circuit, including transistors or other devices on the substrate and external electrodes or connections for facilitating electrical connection of the wiring/circuit to an external component.

269. Hasunuma’s first interconnect (“conductive layer 14”) is indeed formed on a semiconductor (silicon) substrate that includes such active circuit elements, e.g., where conductive plug 15 of the first interconnect secures “the conduction to the electronic circuit formed in the Si substrate 1.” *See id.*, ¶¶[0090], [0092]-[0093] (“It is to be noted that the conductive plug 15 of the first layer is formed as the contact plug 15 for securing the conduction to the electronic circuit formed in the Si substrate 1.”).

270. Hasunuma’s second interconnect (“conductive layer 26”) is connected to the first interconnect by the via/conductive plug 27, and thus to the “electronic circuits.” Furthermore, a POSITA would recognize that Hasunuma’s second interconnect (“conductive layer 26”) is part of a functional multi-level wiring scheme that creates a circuit by virtue of a connection to additional other elements

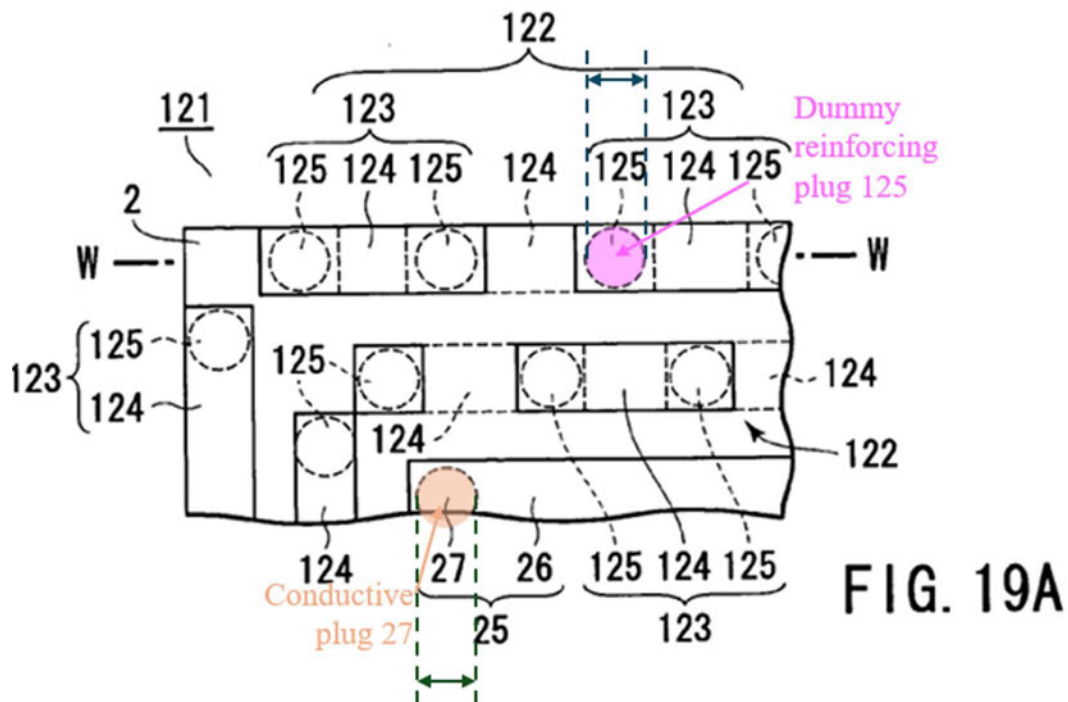
(e.g., other wiring layers, vias, or circuit components) or external electrodes (e.g., electrodes connected/bonded to Al pad 136). *Id.*, ¶¶[0089], [0128], [0209]-[0212], [0298], [0005], Fig. 21A. In addition, a POSITA understood that, in a semiconductor device, it is necessary that such functional wiring layers, such as Hasunuma's first and second interconnects, be connected to other circuit elements and/or to external electrodes for the device to operate. Indeed without connections to other circuit elements, no circuit is created and the active interconnects would serve no purpose and the overall device itself would be useless.

271. Thus, Hasunuma satisfies claim 6.

4. Claim 9 - *The method of claim 1, wherein the via and the dummy via are substantially circular in a plan view.*

272. Claim 9 recites that "the via and the dummy via are substantially circular in a plan view," which Hasunuma discloses.

273. Hasunuma discloses circular vias (in plan view) in various figures, including Figure 19A as annotated below (*see, e.g.*, TSMC-1005, Figs. 19A, 22A-22C, 24A-27C, ¶[0200]):



274. Additionally, when describing tests performed on such structures, Hasunuma discusses the “diameter” of both conductive and reinforcing plugs, further demonstrating Hasunuma’s disclosure of a circular shape for both its vias and dummy vias. *See id.*, ¶¶[0127] (“each diameter of the Cu conductive contact plug 15, Cu reinforcing contact plug 16, Cu conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 μm.”), [0133], [0201], [0216], [0010]. A POSITA would have understood that describing the vias’ “diameter” in this context discloses a circular shape for both conductive plug 27 and reinforcing plug 28 (i.e., via and dummy via), since “diameter” is the standard dimensional term for circular features.

275. The express disclosure of circular vias in, *inter alia*, Figure 19A, reinforces that Hasunuma's reference to the "diameters" of its vias and dummy vias discloses that these structures likewise have a substantially circular cross section in plan view, just as shown in Figure 19A. In view of the foregoing, a POSITA would have readily understood Hasunuma to disclose substantially circular-shaped vias as an option for any of its vias or dummy vias.

276. Accordingly, Hasunuma discloses claim 9.

5. Claim 11 - *The method of claim 1, wherein the first interconnect and the second interconnect extend in a same direction.*

277. Claim 11 recites "the first interconnect and the second interconnect extend in a same direction," which Hasunuma discloses.

278. A POSITA would understand that first interconnect (e.g., "conductive layer 14") and second interconnect (e.g., "conductive layer 26") each extend in multiple directions that are the same. For example, Hasunuma's first interconnect (e.g., "conductive layer 14") extends in a same lengthwise direction (e.g., across the page) as Hasunuma's second interconnect (e.g., "conductive layer 26"), as disclosed in annotated Figure 8 (TSMC-1005, Fig. 8):

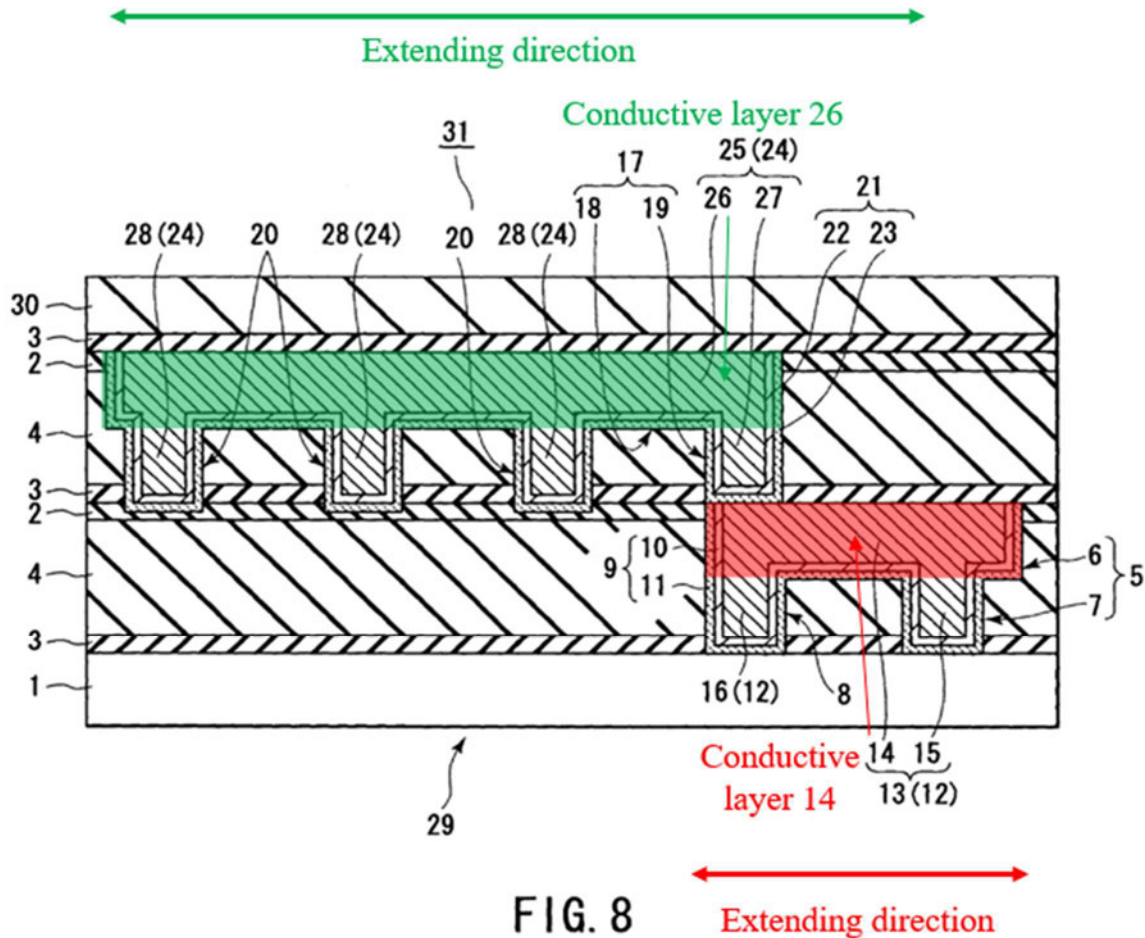


FIG. 8

279. Additionally, a POSITA would understand that both interconnects extend in a same widthwise direction into/out of the page.

280. A POSITA would further recognize and discern between these lengthwise and widthwise directions based on the description in Hasunuma's specification of the dimensions of the vias and conductive layers as well as Hasunuma's figures. For example, both conductive layers 14 and 26 (which are part of Cu wiring layers 13, 25) are described as having a same width as conductive plug 27 and reinforcing plugs 28. See TSMC-1005, ¶[0127] ("Additionally, each

diameter of the Cu conductive contact plug 15, Cu reinforcing contact plug 16, Cu conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 um.... Furthermore, each of the Cu wiring layers 13, 25 was formed as a single wiring. In this case, a wiring width of a wiring pattern of each of the Cu wiring layers 13, 25 was set to about 0.13 um....”). This further demonstrates to a POSITA that the cross-sectional views in Figure 8 of Hasunuma disclose a length of both conductive layer 26 and conductive layer 14, because the distances of these layers across the page are both different from each other, and different from and much greater than the width of the individual plugs 27 and 28 (which are described as having a same width). This confirms that Figure 8’s cross section must be showing the lengthwise direction of conductive layers 14 and 26, and that these lengthwise directions extend in the same direction across the page.

281. Additionally, Figure 14 discloses multiple first conductive layers 14, one extending in a lengthwise direction across the page and the other three extending in a lengthwise direction into/out of the page:

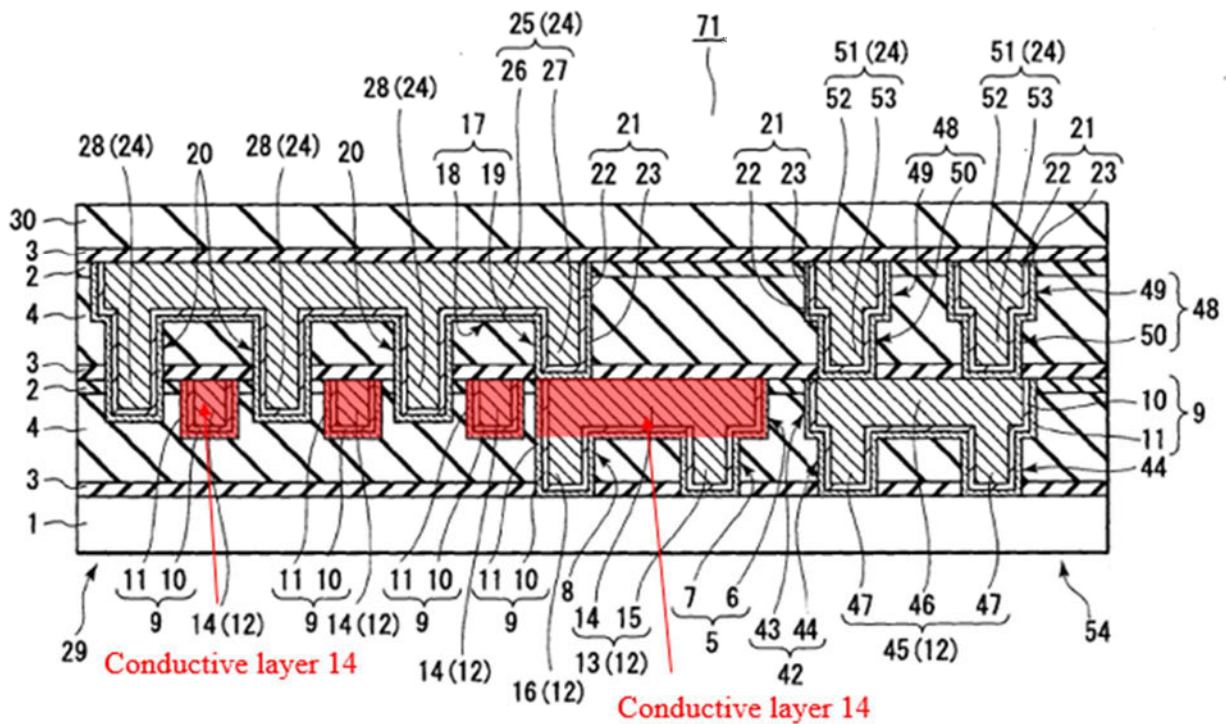


FIG. 14

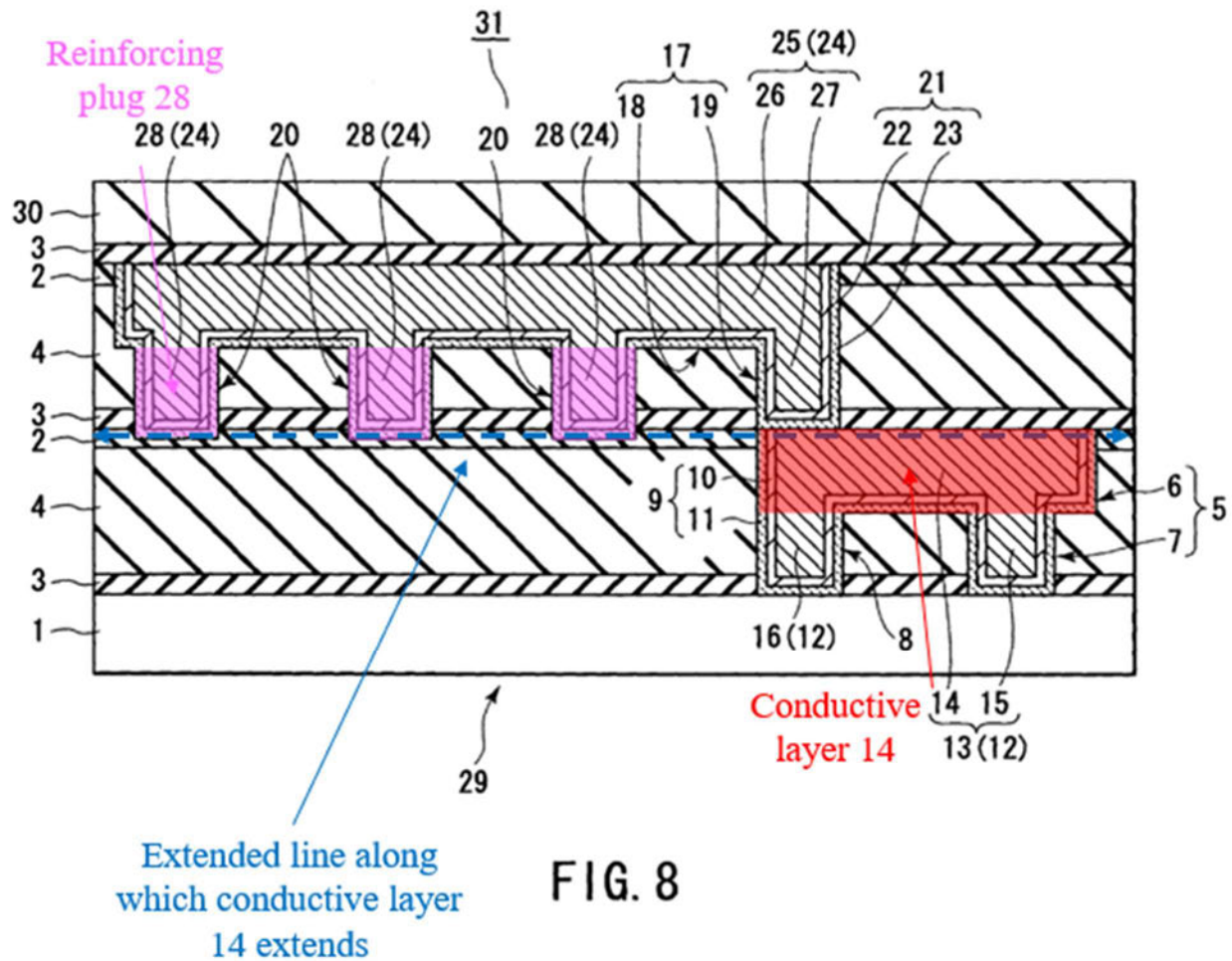
282. As shown in Figure 14, the three conductive layers 14 on the left side of Figure 14 extend a same distance across the page as the reinforcing plugs 28 and conductive plug 27, and thus a POSITA would recognize that dimension of the conductive layers 14 to be the width (since it is approximately equal to that of reinforcing plugs 28 and conductive plug 27 just as called for in paragraph 127). In contrast, the conductive layer 14 on the right would be recognized by a POSITA to extend in a lengthwise direction across the page given its much greater extent across the page as compared to that of the other conductive layers 14 and the conductive plug 27 and reinforcing plugs 28.

283. Accordingly, Hasunuma satisfies claim 11.

6. Claim 12 - *The method of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends.*

284. Claim 12 recites “the dummy via is provided on an extended line along which the first interconnect extends,” which Hasunuma discloses.

285. In Hasunuma’s cross-sectional views, such as Figure 8, the first interconnect (conductive layer 14) is disclosed as a generally horizontal layer, shown to extend across the page (e.g., from right to left). Hasunuma’s dummy via (e.g., “reinforcing plug 28”) is provided on an extended line along which the first interconnect (e.g., “conductive layer 14”) extends. This is shown below in annotated Figure 8 (*see* TSMC-1005, Fig. 8):



286. Accordingly, Hasunuma satisfies claim 12.

7. **Claim 13** - *The method of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less.*

287. Claim 13 recites that “the via and the dummy via are spaced at a distance of 25 μm or less.”

288. Hasunuma's Figure 9⁸ and Tables 1-3 provide values for "plug interval" between conductive plug 27 and an adjacent reinforcing plug 28 (TSMC-1005, ¶¶[0127], [0130]-[0137]), labeled as "B" in Figure 9):

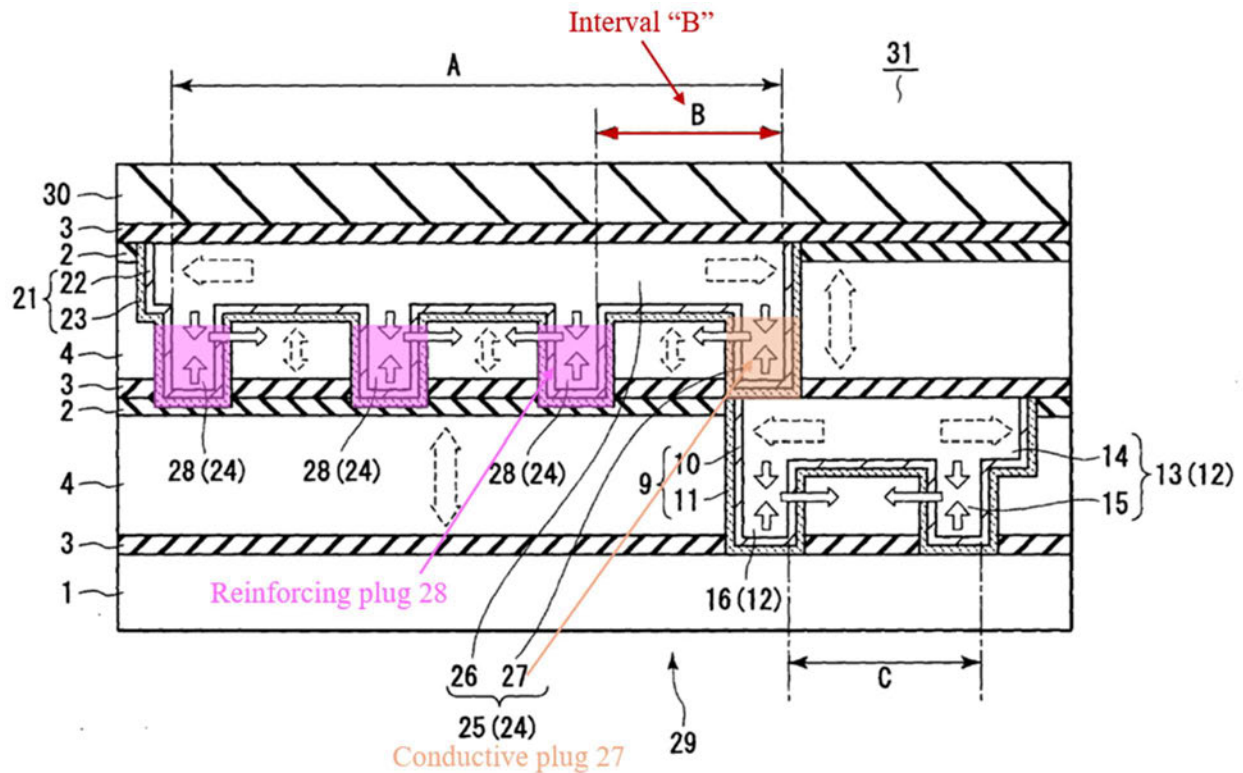


FIG. 9

289. As seen from Figure 9, interval "B" is portrayed as the right edge-to-right edge spacing, which is effectively equal to the center-to-center spacing between the via and dummy via. As clearly seen from Figure 9, this right edge-to-right edge

⁸ A POSITA would recognize that Hasunuma's Figure 9 discloses the same device as in Hasunuma's first embodiment and Figure 8, but adds illustrations of various stresses (e.g., thermal stresses) within the device. TSMC-1005, ¶¶[0022], [0112].

or center-to-center spacing is larger than the adjacent edge-to-adjacent edge spacing between the via and dummy via (e.g., the spacing between the right edge of reinforcing plug 28 and the adjacent left edge of conductive plug 27).

290. Hasunuma discloses a preferred interval B of less than 1 μm or of less than 5 μm or less, and tested intervals up to 20 μm , each of which is less than 25 μm for the larger right edge-to-right edge or center-to-center spacing. TSMC-1005, ¶¶[0137] (“Cu conductive plugs 15, 27 and Cu reinforcing plugs 16, 28 are preferably provided so that the plug interval B, C is about 1 μm or less”), [0159] (“it has been found that the plug interval B provided in the Cu wiring layer 25 is preferably about 5 μm or less”), Tables 1-3 (disclosing plug intervals of 0.26 μm , 0.39 μm , etc.). As noted above, the spacing distance between the right side of the reinforcing plug 28 annotated above in Figure 9 and the left side of the adjacent conductive plug 27 is less than the plug interval B between those same plugs. Since B represents an even greater distance than this right edge-to-left edge spacing between the via (conductive plug 27) and dummy via (reinforcing plug 28), this teaching for B satisfies the claim limitation of 25 μm or less.

291. Accordingly, Hasunuma satisfies claim 13.

8. Claim 14 - *The method of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via.*

292. Claim 14 recites that “a bottom of the dummy via is located deeper than a bottom of the via,” which Hasunuma discloses.

293. Hasunuma teaches that a bottom of its dummy vias (e.g., “reinforcing via plug 28”) is located deeper than a bottom of the real, functional via (e.g., “conductive plug 27”). TSMC-1005, ¶¶[0104] (“Even when this overetching phenomenon occurs, there is no problem as long as each the recess 20 has a depth to such an extent that the first reinforcing plug 28 of the second layer formed in the recess 20 is not electrically connected to the essential wiring layer (not shown) provided below the plug.”), [0109] (“The three Cu first reinforcing plugs 28 are formed substantially extending through the SiCN film 3 of the second layer to indirectly contact the SiC film 2 of the first layer via the barrier metal film 21. That is, each Cu first reinforcing plug 28 is formed to be substantially connected to the SiCN film 3 of the second layer having a Young's modulus of about 30 GPa or more and the SiC film 2 of the first layer via the barrier metal film 21 in the lower end (bottom portion).”), [0176]-[0178], Figs. 8, 14. As annotated below, Figure 8 discloses “reinforcing plugs 28” extending into underlying “SiC film 2” while “conductive plug 27” extends only to the upper surface of “conductive layer 14” (*id.*, ¶¶[0104], [0109], Fig. 8):

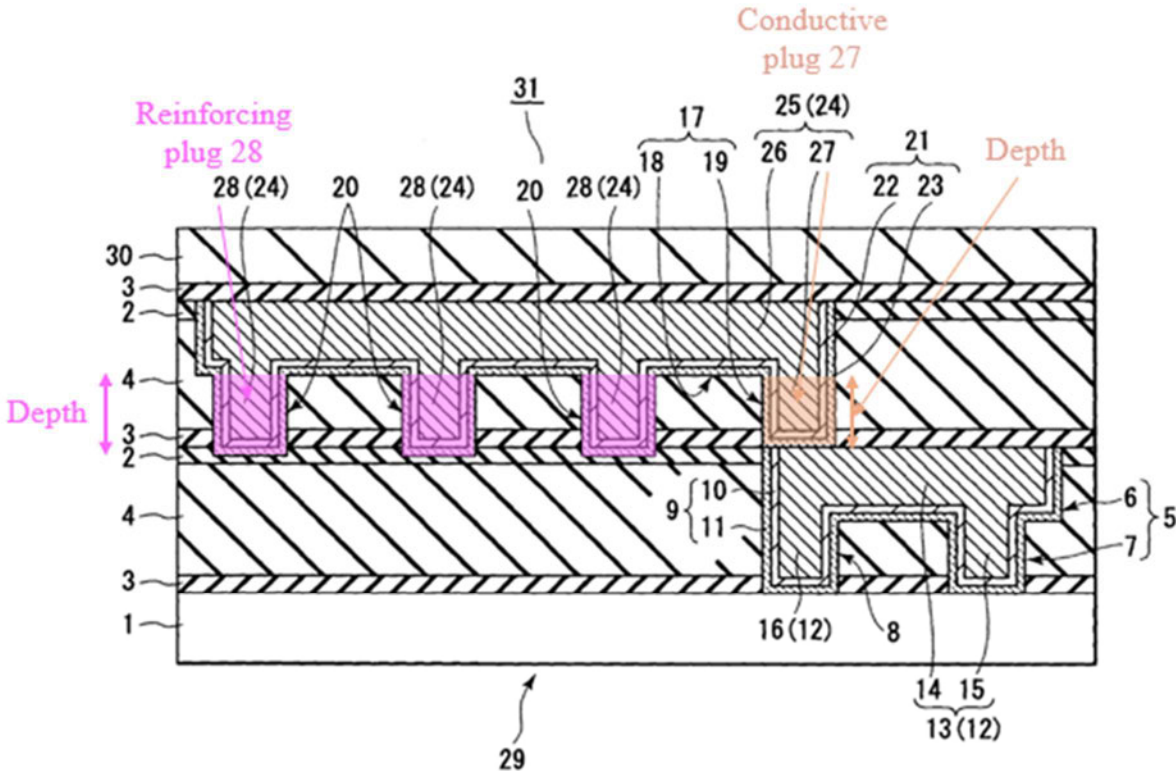


FIG. 8

Thus, a bottom of “reinforcing plug 28” extends deeper than a bottom of “conductive plug 27.”

294. In addition, Figure 14⁹ is directed to a further embodiment that includes the same components as the embodiment of Hasunuma’s Figures 1-8 relied on for

⁹ Figure 14 is directed to a “fourth embodiment,” but includes the same components as the first embodiment of Hasunuma’s Figures 1-8 relied on for claim 1. TSMC-1005, ¶[0176]; *supra*, §X(E)(1). Accordingly, my analysis above of the Figure 8 embodiment for claim 1 (including its mapping to the elements of claim 1) applies equally to Figure 14, which discloses the elements of claim 1 for the same reasons as Figure 8 discussed above.

claim 1. *Id.*, ¶[0176]. As disclosed in annotated Figure 14 below, “reinforcing plugs 28” extend into underlying “low dielectric constant film (interlayer insulating film) 4” while “conductive plug 27” extends up to the upper surface of “conductive layer 14”:

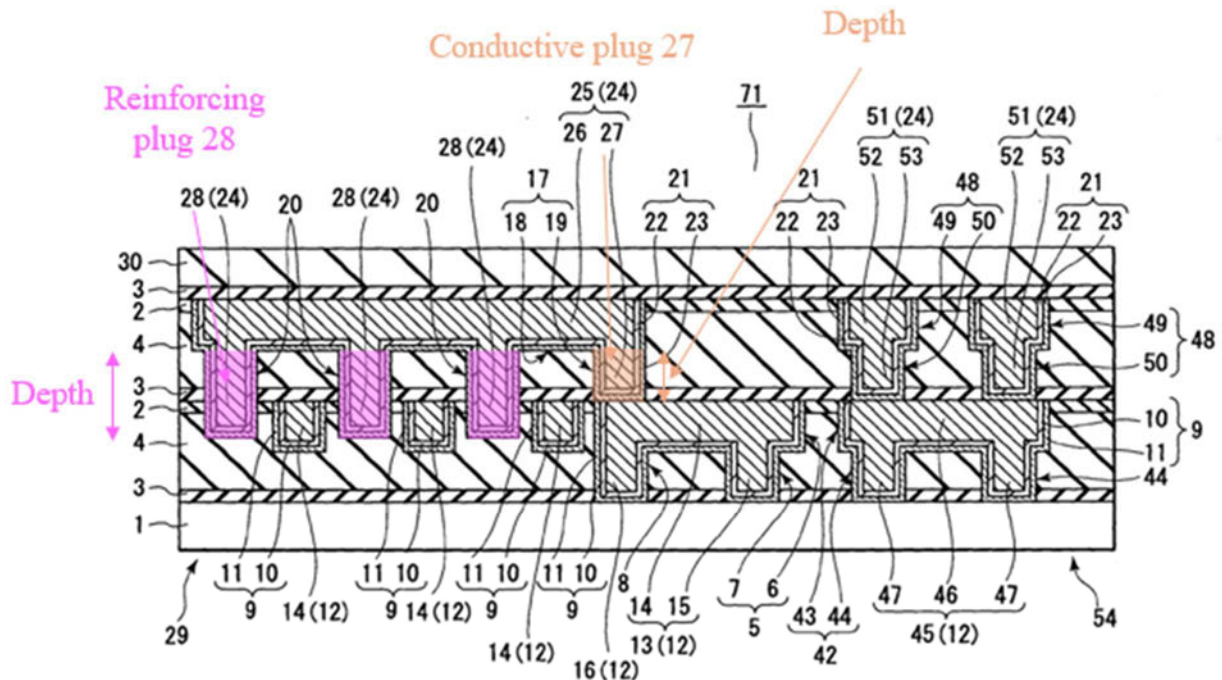


FIG. 14

Thus, once again, a bottom of “reinforcing plug 28” extends deeper than a bottom of “conductive plug 27.”

295. Thus, Hasunuma satisfies claim 14 based on each of the Figure 8 and Figure 14 embodiments.

9. Claim 18 - *The method of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film.*

296. Claim 18 recites that “the dummy via and the second interconnect are made of the same conductive film,” which Hasunuma discloses.

297. Hasunuma’s dummy via (e.g., “reinforcing plug 28”) and second interconnect (e.g., “conductive layer 26”) are both made from the same conductive film (e.g., “Cu film 24” and/or “barrier metal film 21”) (TSMC-1005, ¶¶[0105]-[0108], Fig. 8):

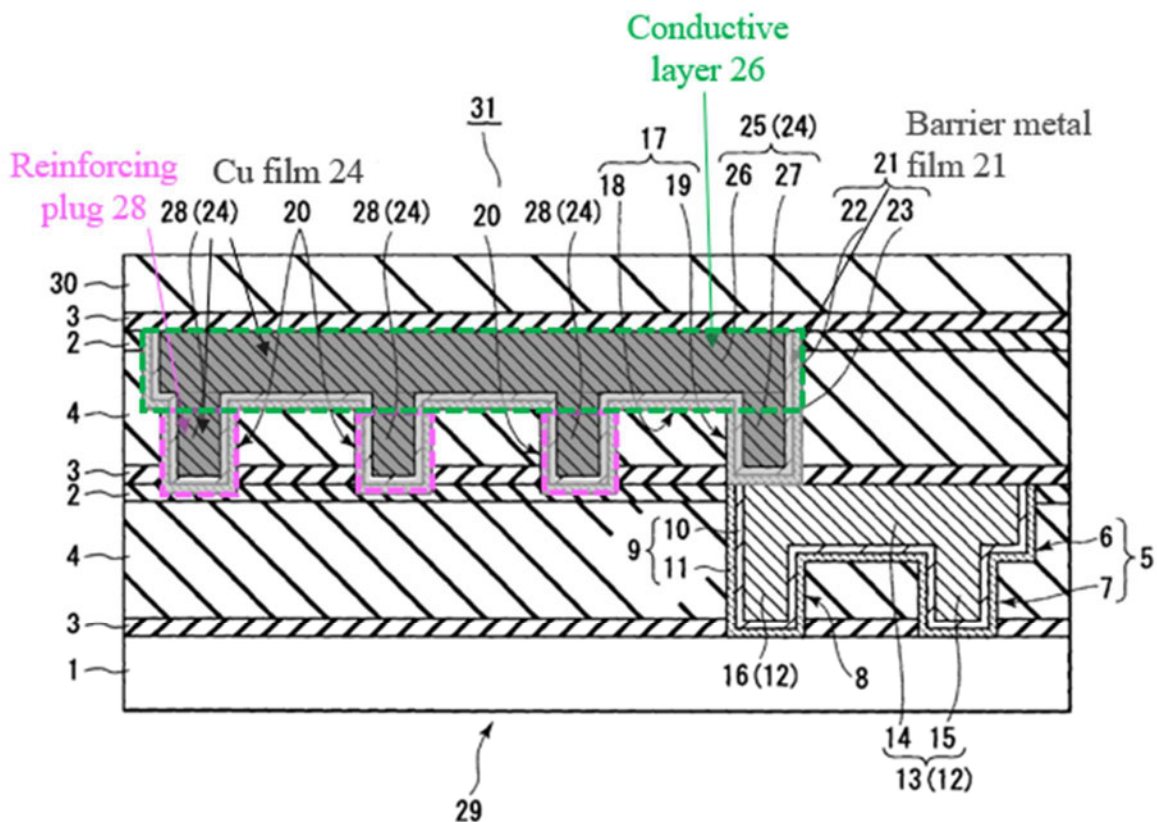


FIG. 8

298. Indeed, a POSITA would understand that Hasunuma’s dual damascene process for forming its interconnects and vias forms the dummy via (Cu reinforcing plug 28) and the second interconnect (Cu conductive layer 26) by simultaneously

filling integrally formed recesses (recess for the first reinforcing plug 20, recess for the conductive layer 18) first with the same barrier metal film 21 and then with the same bulk Cu film 24. *See* TSMC-1005, Figs. 4-7, ¶¶[0105]-[0108]. Thus, both the dummy via and the second interconnect are made of a same conductive film, namely the barrier metal film 21 and copper film 24.

299. Accordingly, Hasunuma satisfies claim 18.

10. Claim 19 - *The method of claim 1, wherein the dummy via includes a first end and a second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.*

300. Claim 19 recites that “the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film,” which Hasunuma discloses.

301. Hasunuma discloses dummy vias (e.g., “reinforcing plug 28”) with a first end and a second end, the first end connected to the second interconnect (e.g., “conductive layer 26”) and the second end surrounded by a second insulating film (e.g., lower layer “SiC film 2” or lower layer “low relative dielectric constant film 4”). TSMC-1005, ¶¶[0103]-[0104], [0109], [0177]-[0178], Figs. 4, 8, 14.

302. Hasunuma’s dummy via (reinforcing plug 28) is a vertical structure with a first (top) end and a second (bottom) end. *Id.*, Fig. 8. The dummy via’s top

end is connected to the second interconnect (conductive layer 26), resulting from the dual damascene process where the dummy via is formed integrally with the second interconnect. *Id.*, ¶[0108], Figs. 4-7.

303. The second end of Hasunuma's dummy via (e.g., "reinforcing plug 28") is surrounded by a second insulating film (e.g., "low relative dielectric constant film 4" and/or lower layer "film 2" alone or as part of the combination of the lower layer insulating films 2, 3, 4). TSMC-1005, ¶¶[0103]-[0104]. During manufacture, recess 20 extends through insulating film 3 (of the second-level insulating layer) and terminates in the underlying, lower insulating film 2 (of the first insulating layer). *Id.*, ¶[0104], Figs. 4-7. Dummy via is then created in recess 20, such that the dummy via's bottom end is surrounded by a second insulating film, as seen in Figures 8 and 14 below. Hasunuma explains that "each ... recess 20 is formed extending through the SiCN film 3 of the second layer so as to expose the surface of the SiC film 2 of the first layer. It is to be noted that in the actual RIE process, as shown in FIG. 4, there is a possibility of occurrence of a so-called overetching phenomenon in which the bottom portions of the recesses 20 extend below the surface of the SiC film 2 of the first layer. Even when this overetching phenomenon occurs, there is no problem as long as each the recess 20 has a depth to such an extent that the first reinforcing plug 28 of the second layer formed in the recess 20 is not electrically connected to the essential wiring layer (not shown) provided below the plug." *Id.*,

¶¶[0103]-[0104]; *see also id.*, [0109], [0177]-[0178] (“each Cu reinforcing via plug 28 is extended downwards, and formed completely extending through the SiCN film 3 of the second layer and the SiC film 2 of the first layer. Moreover, the lower end of each Cu reinforcing via plug 28 projects into the low relative dielectric constant film (interlayer insulating film) 4 of the first layer.”), Figs. 4, 8, 14.

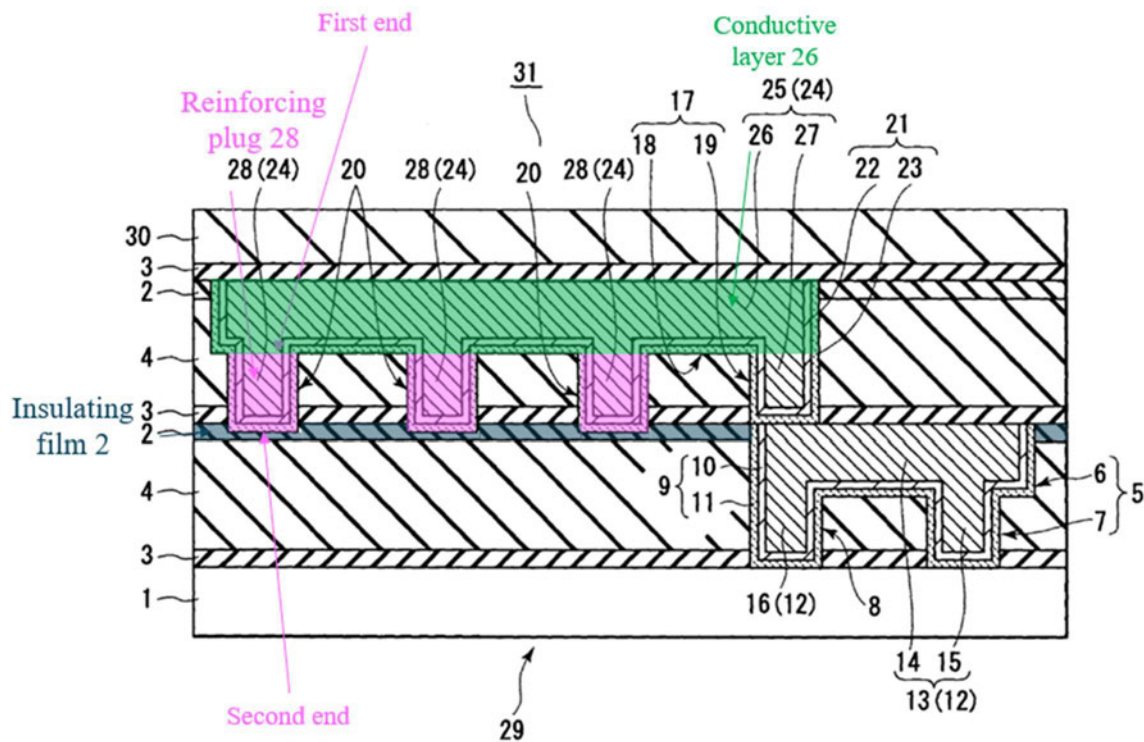
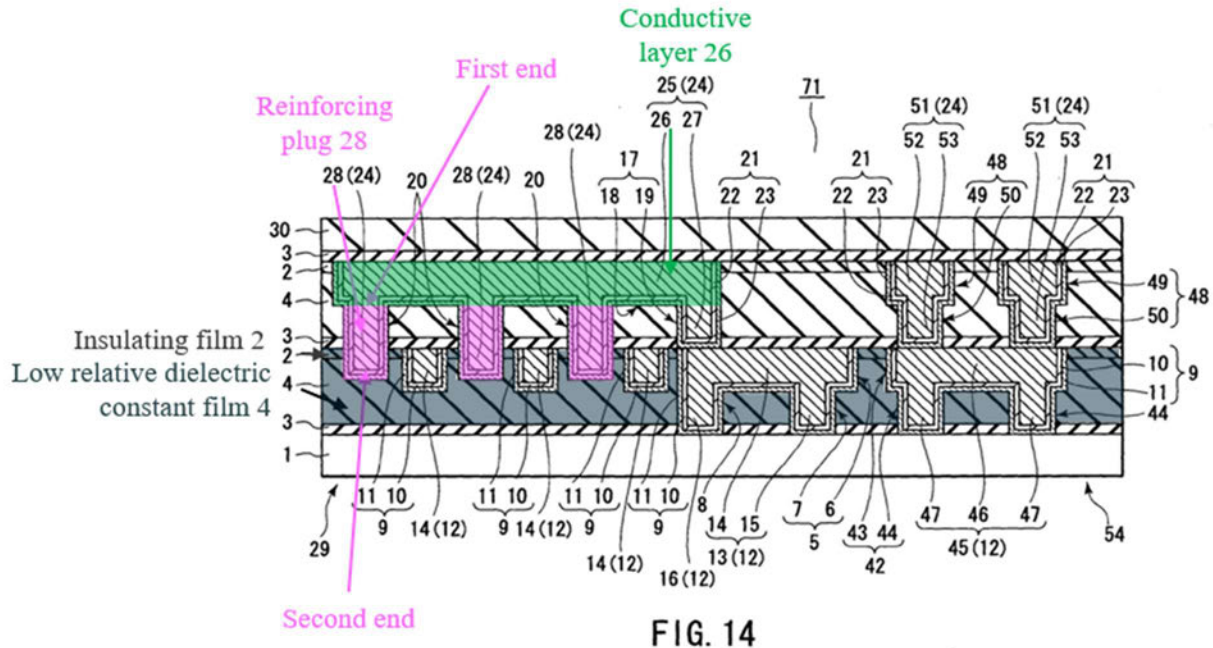


FIG. 8



304. As disclosed in Figure 8 above, the second (bottom) end of dummy/reinforcing plug 28 extends into and is surrounded by SiC insulating film 2.

305. As disclosed in Figure 14 above, the second (bottom) end of dummy/reinforcing plug 28 is surrounded by insulating films 2 and/or 4, thus satisfying claim 19. A POSITA would further understand that the concept of extending plugs 28 into underlying layer 4 as shown in Figure 14 is equally applicable to Figure 8's device given the like numbering of the plugs and insulating layers and its similar overall structure. Moreover, as discussed above, Figure 14 includes the same relevant components that I mapped in the claim 1 discussion above to the limitations of claim 1 of the '751 patent. Thus, Figure 14 satisfies claim 1 for the same reasons as discussed above for the embodiment of Figures 1-8.

F. Ground 6: Hasunuma combined with Kurashima renders Claims 2 and 20 obvious

306. I believe claims 2 and 20 of the '751 patent are obvious over Hasunuma and Kurashima as discussed below.

1. Claim 2

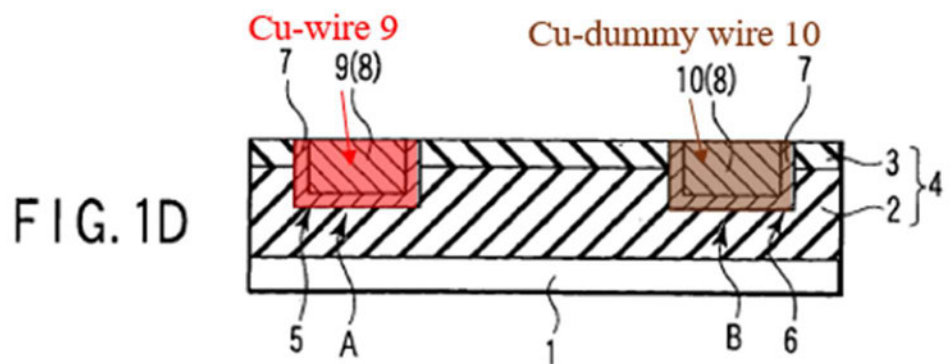
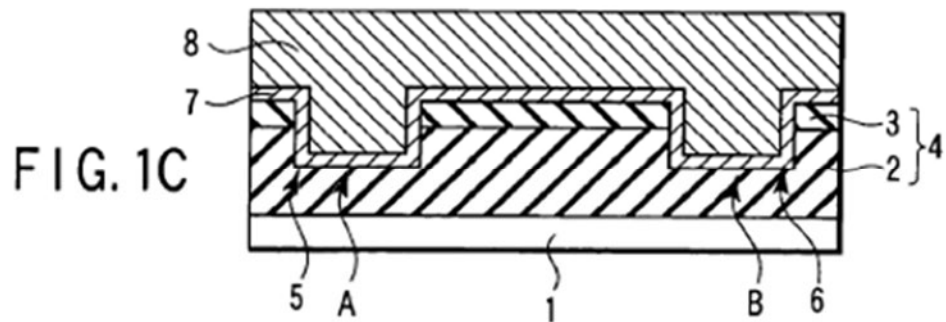
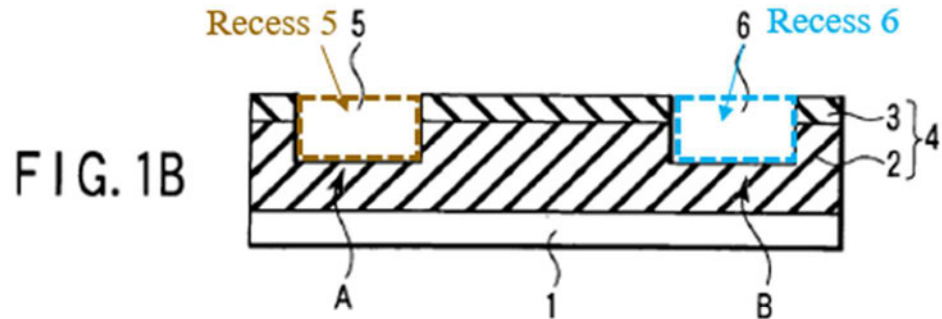
[2a] The method of claim 1, wherein in the step (a) a first dummy interconnect is simultaneously formed on the semiconductor substrate, and

307. Kurashima discloses simultaneously forming both a first interconnect (e.g., “Cu-wire 9” and “TaN-film 7,” hereafter collectively “Cu-wire 9”) and a first dummy interconnect (e.g., “Cu-dummy wire 10” and “TaN-film 7,” hereafter collectively “Cu-dummy wire 10”) on a semiconductor substrate (e.g., “semiconductor substrate 1”). TSMC-1011, 4:12-21, 4:50-6:57, Figs. 1B-1D.

308. For example, Kurashima discloses a “manufacturing method of [a] semiconductor device” in which a first dummy interconnect (“Cu-dummy wire 10”) is connected to a dummy via (“Cu-dummy wire 9”). TSMC-1011, 4:7-21, Fig. 3A. A POSITA would understand that “Cu-dummy wire 10” is a dummy interconnect both because of its description as a “dummy” structure and its purpose (i.e., to add structural support to the device and prevent peeling of layers rather than as an active circuit element), which is consistent with the '751 patent’s description of a “dummy

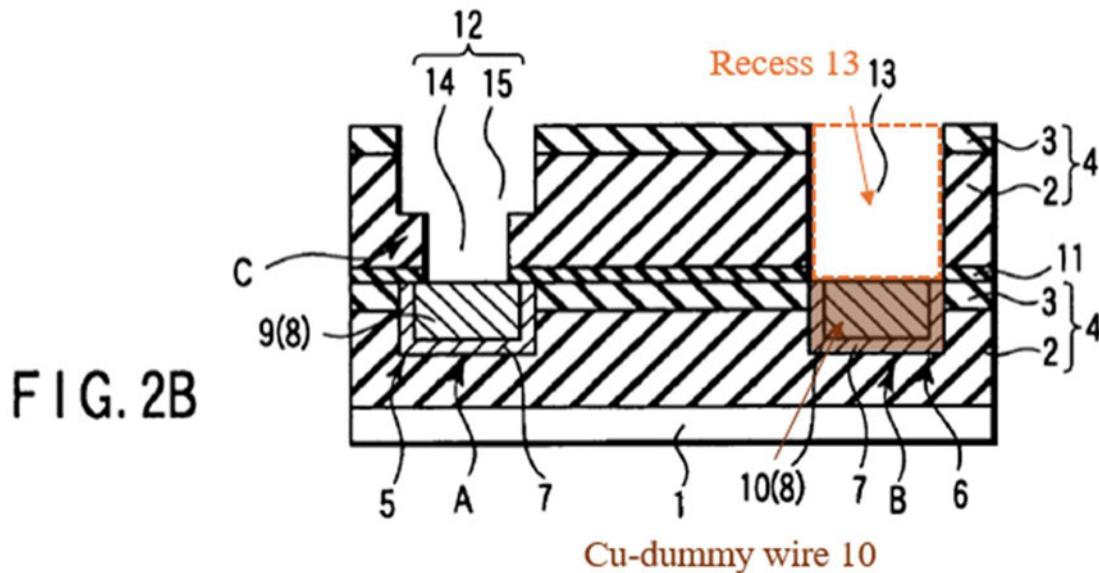
interconnect.” *See supra*, §X(E)(1)(1[c]). Specifically, Cu-dummy wire 10 does not constitute part of a closed circuit in actual use of the device, i.e., no current flows therein during use. *See* TSMC-1011, 4:58-61. Rather, Kurashima uses Cu-dummy wire 10 (and its direct connection to a dummy via, i.e., “Cu-wire 9”) to add structural support to the device and thereby reduce film peels. *Id.*, 5:63-6:32 (“Therefore, the SiC film 3 is substantially connected to the low-relative-dielectric-constant film 2 via the Cu-dummy wire 10 and TaN-film 7. Accordingly, the adhesion at the interface between the SiC-film 3 and low-relative-dielectric-constant film 2 is enhanced to a size that can bear a physical load of CMP. That is, the durability of the interlayer insulating film 4 against the mechanical stress in the CMP process is enhanced in forming the Cu-wire 9 and Cu-dummy wire 10 of the first layer. Accordingly, the film peels in the layer are reduced.”), 9:16-23 (“In this manner, the Cu-dummy wire 17 of the second layer formed to continue to the Cu-dummy wire 10 of the first layer enhances the durability of the SiC-film 11 of the first layer, the low-relative-dielectric-constant film 2 of the second layer, and the SiC-film 3 of the second layer with respect to the CMP. As a result, not only the film peel in the second layer but also the film peel between the first layer and the second layer are reduced.”). Additionally, Kurashima’s device would still be operable if Cu-dummy wire 10 was omitted, because it serves no part in routing current flow as part of the actual operation of the device.

309. Additionally, as shown in annotated Figures 1B-1D below, Kurashima discloses forming a recess for an interconnect (wire 9) and a recess for the dummy interconnect (wire 10) simultaneously, and forming wire 9 and dummy wire 10 simultaneously. TSMC-1011, 4:50-61.



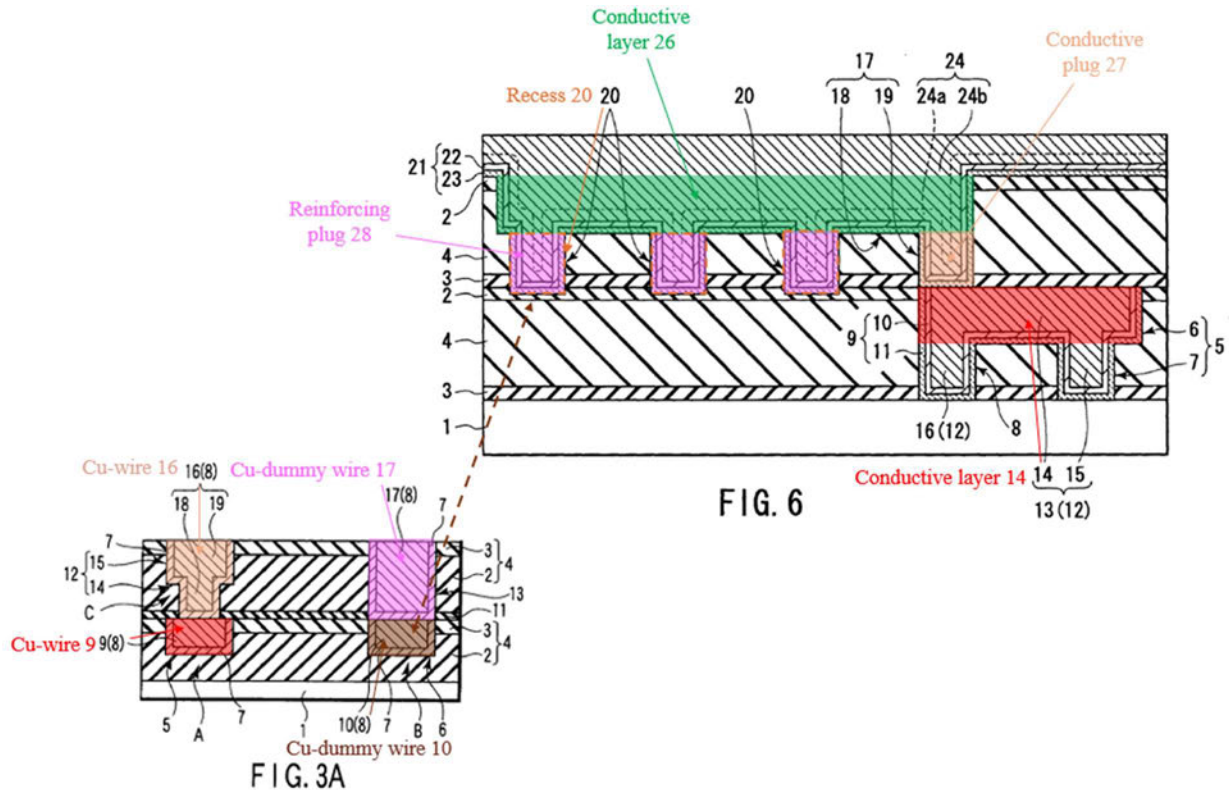
[2b] in the step (c) the dummy hole is connected to the first dummy interconnect.

310. As shown in annotated Figure 2B below, Kurashima's dummy hole (e.g., "recess [for a dummy wire] 13") is connected to the dummy interconnect (e.g., "Cu-dummy wire 10"). TSMC-1011, 7:11-8:13, Figs. 2B-3A.



311. Accordingly, a POSITA would have understood that, when incorporating a dummy interconnect (similar to Kurashima's "Cu-dummy wire 10") into Hasunuma's device, the dummy interconnect would be formed at the same time as first interconnect 14 (similar to the simultaneous formation of Kurashima's Cu-dummy wire 10 and Cu-wire 9), and that dummy hole 28 formed in Hasunuma's insulating film (e.g., "low relative dielectric constant film 4") would be connected to the dummy interconnect so that the dummy via (e.g., Hasunuma's "reinforcing

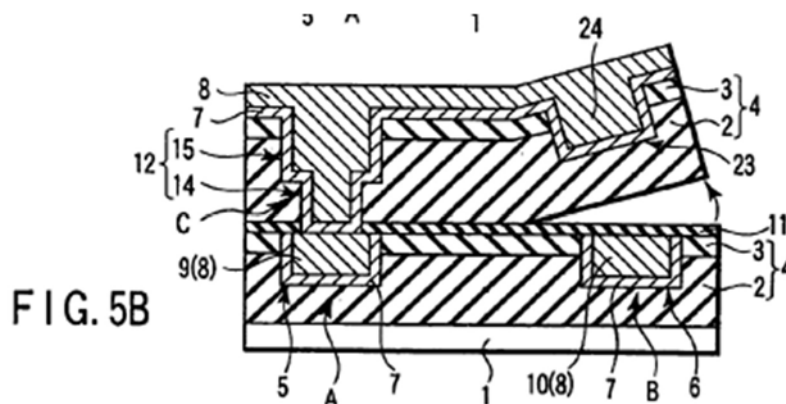
plug 28”/Kurashima’s “Cu-dummy wire 17”) formed therein would be connected to the dummy interconnect similar to that in Kurashima). This modification is shown graphically in the combination of annotated Figure 6 of Hasunuma and annotated Figure 3A of Kurashima:



Obviousness of Combining Hasunuma and Kurashima

312. It was obvious to incorporate such a dummy interconnect into Hasunuma’s device in view of Kurashima. A POSITA would have been motivated to do so in order to increase the interlayer strength of the semiconductor device and thereby reduce the likelihood of layer peeling or film separation including between Hasunuma’s lowermost insulating films 4 and 2 (i.e., its low-k film 4 and the

overlying insulating film 2), as expressly discussed by Kurashima in regard to its low-k film 2 and overlying insulating film 3. See TSMC-1011, 5:63-6:32 (“According to experiments conducted by the present inventors, when the Cu-dummy wire 10 is not formed, as shown in FIG. 5A, during the first polishing, a film peel was generated at an interface between the low-relative-dielectric-constant film 2 and SiC-film 3. Additionally, in the present embodiment in which the Cu dummy wire 10 is formed, as shown in FIG. 1D, even when not only the first polishing but also the second polishing end, the film peel was hardly generated in the interface between the low-relative-dielectric-constant film 2 and SiC-film 3.”), 8:14-34, 9:16-23, Figs. 5A-5B. Kurashima expressly discusses the significance of extending the overlying dummy via such that it contacts the dummy interconnect, in discussing how film peel may still occur when the overlying dummy via is not extended to the dummy interconnect. *Id.*, 8:14-34, Fig. 5B.



313. A POSITA would have readily recognized that implementing a dummy interconnect connected in Hasunuma such that it was connected to a dummy

reinforcing plug 28 would have helped prevent separation of layers of Hasunuma's device (e.g., the lower layer, e.g., in Fig. 8, which includes the combination of insulating films 3, 4, 2 and "conductive layer 14," from the upper layer, which includes another combination of insulation films 3, 4, 2 and "conductive layer 26" as well as between Hasunuma's low-dielectric constant film 4 and the insulating film 2 directly on top of it) similar to the corresponding structure of Kurashima.

314. Additionally, a POSITA would have been further motivated to incorporate such a dummy plug-dummy interconnect structure to establish additional structural support for the polishing step, thereby reducing dishing of the copper wiring layers. *See* TSMC-1007, 4:12-44; TSMC-1024, 2:55-58; TSMC-1011, 5:63-6:32. Use of dummy structures to prevent dishing was widely known and utilized prior to the '751 patent. As noted for example in Figure 8 below, there is a large vacant space in the insulating film beside conductive layer 14:

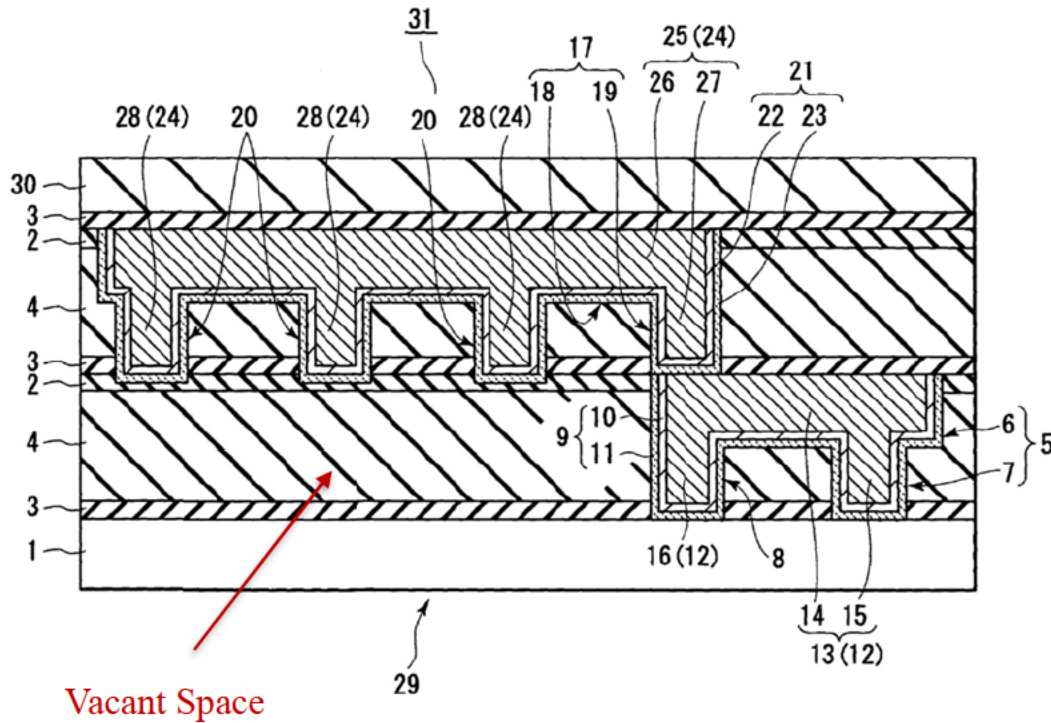


FIG. 8

315. A POSITA would have readily recognized that adding a dummy interconnect connected to dummy plugs 28 in this space would have helped prevent dishing that may otherwise occur during the polishing step (*see* TSMC-1005, Fig. 3A, ¶[0098]) for the formation of the conductive layer 14. *See also* TSMC-1024, 2:55-58 (“This application of dummy patterns results in better fill in bulk metal circuit lines with subsequent improved planarization after CMP and in the elimination of dishing or surface concavity after CMP of large open areas.”).

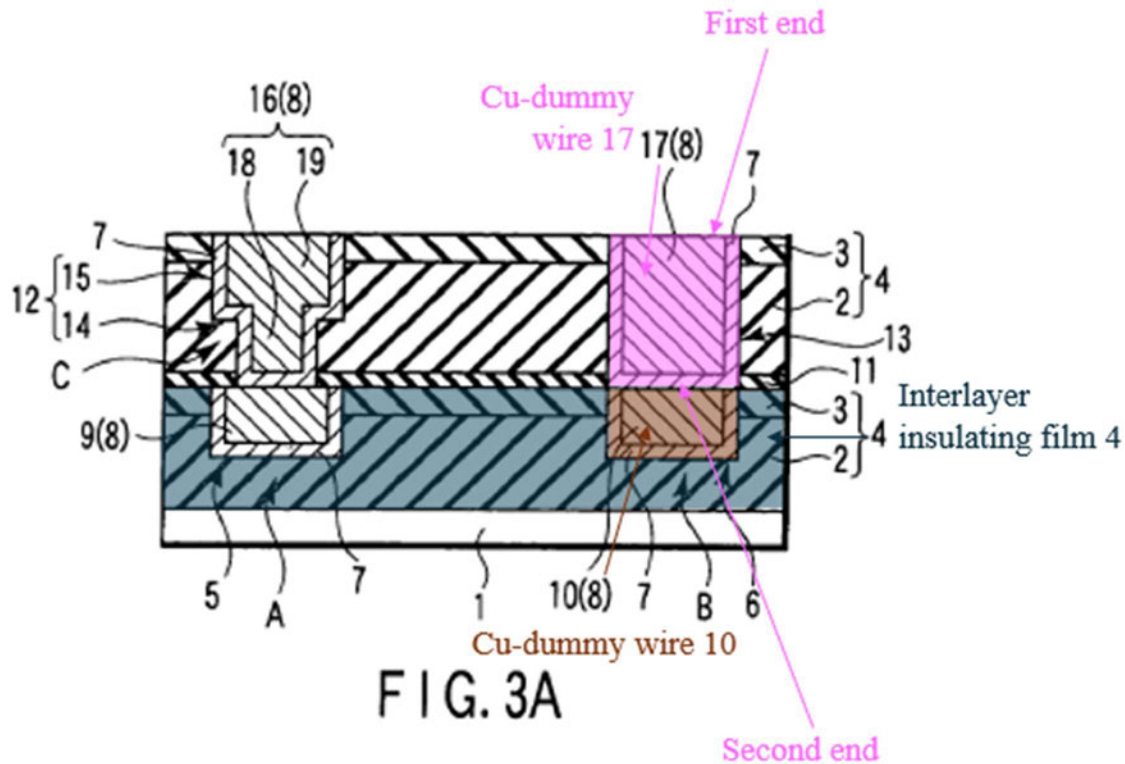
316. A POSITA would have expected success when incorporating a dummy plug-dummy interconnect structure into Hasunuma’s device. A POSITA would have understood that the dummy interconnect connected to the dummy plug could

be reliably positioned beneath one or more of the dummy vias/reinforcing plugs 28 of Hasunuma. Creation of the dummy interconnect could have been easily accomplished using the same processing steps already utilized in Hasunuma to create its first interconnect layer (“conductive layer 14”) and connect “conductive plug 27” thereto. *See, e.g., id.*, ¶¶[0090]-[0099], Figs. 1A-3A. For example, a POSITA would have readily recognized that the dummy interconnect need merely be patterned and created in the same layer and manner as conductive layer 14 using the same processing techniques already used in Hasunuma to create conductive layer 14. Reinforcing plug 28 could then have been easily connected to the dummy interconnect using the same processing techniques already disclosed in Hasunuma as being used to create reinforcing plug 28 and conductive plug 27 (whereby conductive plug 27 is connected to conductive layer 14).

2. Claim 20 - *The method of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film.*

317. As shown in annotated Figure 3A, Kurashima discloses that the dummy via (e.g., “Cu-dummy wire 17” and “Ta_N-film 7,” hereafter collectively “Cu-dummy wire 17”) includes a first and second end, the second end connected to a dummy

interconnect (e.g., “Cu-dummy wire 10”), the dummy interconnect being surrounded by a second insulating film (e.g., “low-relative-dielectric-constant film 2”). TSMC-1011, 4:50-6:14, Figs. 1B-1D, 3A, 4A.



318. In Figure 7, Hasunuma similarly discloses an interconnect (“conductive layer 14”) formed in a layer including a “low relative dielectric constant film 4” (and/or “film 2”) and a dummy via (“reinforcing plug 28”) having a second (bottom) end that terminates just above this layer and a first (top) end that is connected to the second interconnect (“conductive layer 26”) (TSMC-1005, ¶¶[0101]-[0110], Fig. 4):

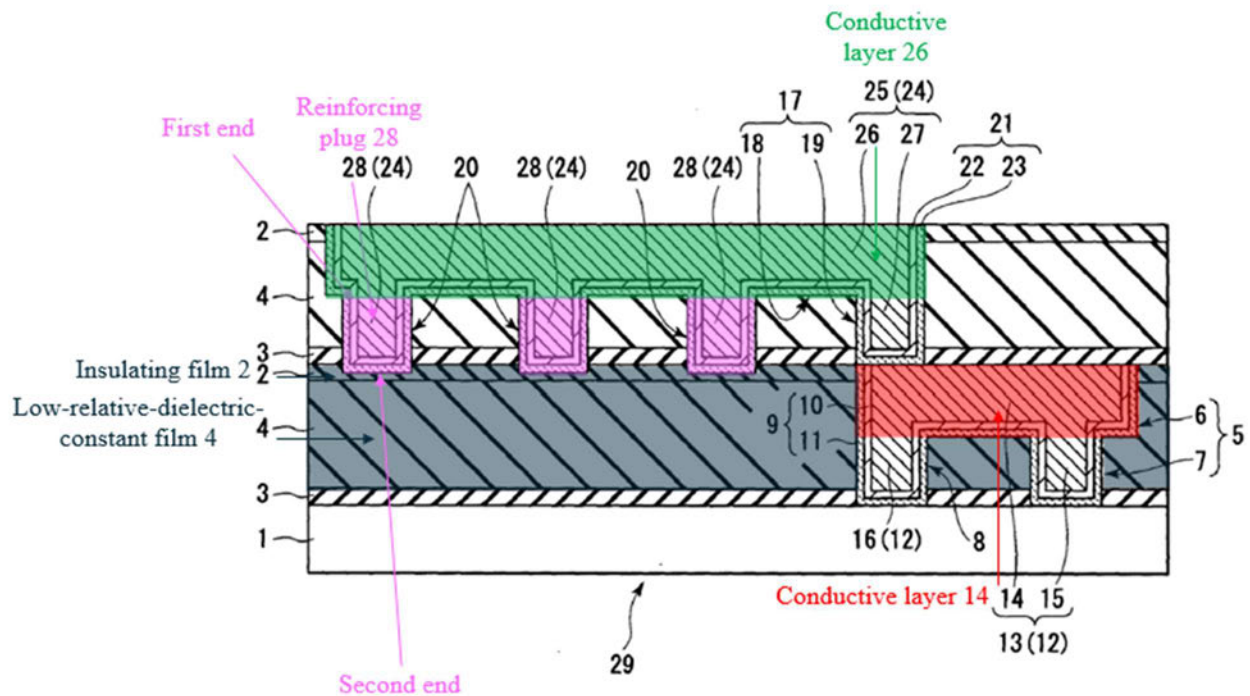


FIG. 7

A POSITA would understand that either one or the combination of both “low relative dielectric constant film 4” and “film 2” could be considered analogous to the “second insulating film” recited in Claim 20.

319. Following Kurashima’s teaching, a POSITA would form a dummy interconnect underneath and connected with the reinforcing plug 28 in Hasunuma. Indeed, Kurashima teaches forming the dummy wiring in parallel with forming the wiring at the same level. TSMC-1011, 4:50-61, Figs. 1B-1D. Thus, following Kurashima’s teaching, a POSITA seeking to implement such a dummy wiring in Hasunuma would form the dummy interconnect in film 4 (and/or SiC film 2 on film 4) in parallel with conductive layer 14, for example using the same processing steps

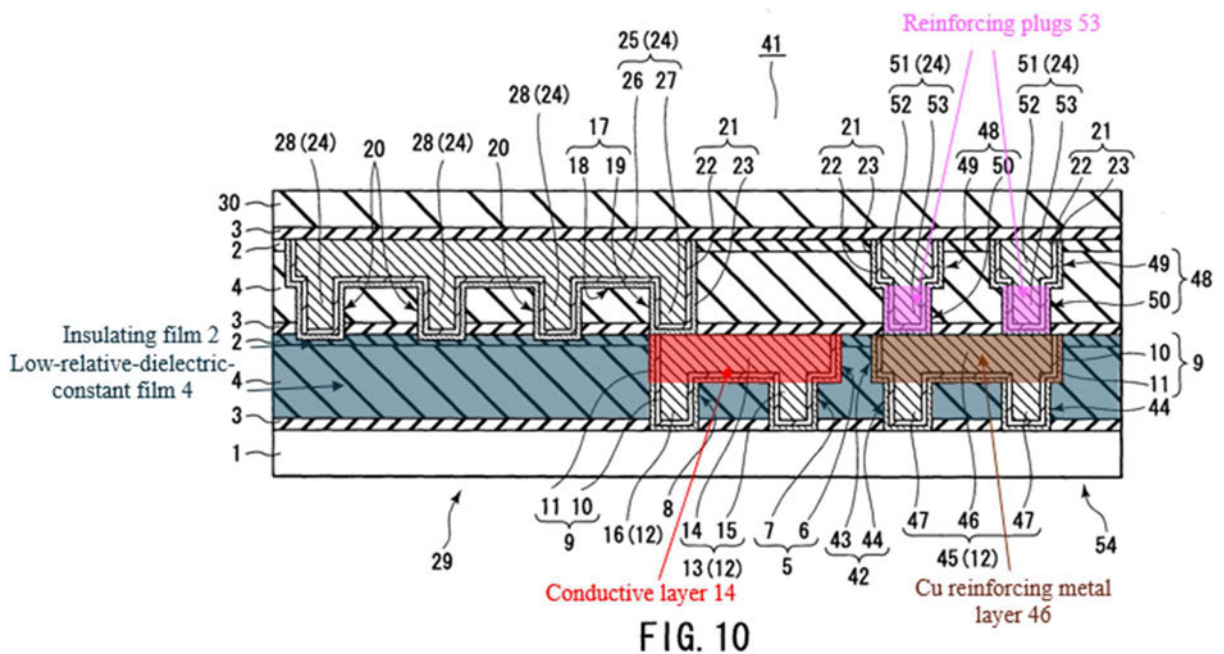
described of forming conductive layer 14 (*see, e.g.*, TSMC-1005, ¶¶[0090]-[0099], Figs. 1A-3A).

320. Thus, the resulting modified structure of Hasunuma would include a dummy via (e.g., “reinforcing plug 28”) connected on its first end to the second interconnect (“conductive layer 26”) and connected on its second end to the dummy interconnect (e.g., added per Kurashima’s “Cu-dummy wire 10” and/or Hasunuma’s “Cu reinforcing metal layer 46”), the dummy interconnect being surrounded by a second insulating film (e.g., “low relative dielectric constant film 4” and/or “SiC film 2”).

321. A POSITA was motivated to create such a structure in this manner and would have expected success for the same reasons as discussed for claim 2 above. *Supra*, §X(F)(1). Indeed, a POSITA would have been motivated to do so in order to increase the interlayer strength of the semiconductor device and thereby reduce the likelihood of layer or film separation and to provide additional strength for the polishing step.

322. Connecting dummy vias to a dummy interconnect and positioning the dummy interconnect such that it is surround by an insulating film would have been easily accomplished using the same processing techniques already disclosed in Hasunuma and, thus, a POSITA would have expected success. In accordance with Kurashima’s teaching, a POSITA would have recognized that the dummy

interconnect could be easily formed in Hasunuma's film 4 (and/or film 2) in parallel with conductive layer 14. Indeed, as shown in Figure 10, Hasunuma already teaches connecting separate dummy vias (e.g., "reinforcing plugs 53") connected to underlying dummy interconnects (e.g., "Cu reinforcing metal layer 46") that are formed in the same level and in the same film 4 as conductive layer 14:



323. Thus, a POSITA would have recognized that one could simply connect a similar dummy interconnect to reinforcing plugs 28 in the same manner.

G. Ground 7: Hasunuma combined with Watanabe renders Claims 2, 8, and 20 unpatentable

324. I believe claims 2, 8, and 10 are obvious over Hasunuma and Watanabe as discussed below.

1. Claim 2

325. As discussed previously above, Watanabe's second and fifth embodiments disclose elements 2[a] and 2[b]. *Supra*, §X(A)(2).

326. It was obvious in view of Watanabe to incorporate a dummy interconnect into Hasunuma's device. Indeed, the same reasons apply for combining Hasunuma and Watanabe as I discussed above for combining Hasunuma and Kurashima. *Supra*, §X(F).

327. Additionally, Watanabe expressly discusses the known benefit of enhanced mechanical strength afforded by incorporating a dummy interconnect into a semiconductor device, which a POSITA understood would have been achieved when incorporating such a dummy interconnect into Hasunuma's device. *See* TSMC-1004, ¶¶[0127] (“[R]eference numeral 61 denotes a dummy wiring formed in the same layer as the second wiring 39. The dummy plug 52 may be connected to this dummy wiring 61. If they are connected in this manner, the mechanical strength of the laminated body consisting of the silicon oxide film 64 (see FIG. 8) and the third wiring 51 can be enhanced by the same reason as the second embodiment.”), [0091] (“According to this, since the second wiring 39 can be firmly supported by the dummy plugs 34 that uses the dummy wiring 41 as its foundation, the mechanical strength of the laminated body consisting of the second insulating film 29 and the second wiring 39 can be enhanced. Such advantage is

particularly useful for the situation where the low-dielectric insulating film of SiLK, or the like is employed in place of the silicon oxide film 25 to lower the overall dielectric constant of the second insulating film 29. If the present embodiment is applied to this case, the reduction in the strength of the laminated body consisting of the low-dielectric insulating film and the second wiring 39 due to the weakness of the mechanical strength of the low-dielectric insulating film can be prevented.”), [0150]; *see also* TSMC-1011, 5:63-6:32, 8:14-34, 9:16-23, Figs. 5A-5B. Thus, Watanabe’s own disclosure suggests and motivates a POSITA to use a dummy interconnect in connection with a dummy via. Still further, a POSITA would have been further motivated to incorporate such a dummy plug-dummy interconnect structure to establish additional structural support for the polishing step, thereby reducing dishing of the copper wiring layers. *See* TSMC-1007, 4:12-44; TSMC-1024, 2:55-58.

328. Additionally, for the same reasons discussed above, a POSITA would have expected success when incorporating a dummy plug-dummy interconnect structure into Hasunuma’s device. *See supra*, §X(F). For example, a POSITA would have understood that a dummy interconnect such as that disclosed in Watanabe could be reliably positioned beneath and connected to a dummy via/reinforcing plug 28 of Hasunuma. Indeed, as noted above, Hasunuma already teaches connecting dummy plugs to dummy interconnects. *See supra*, §X(F);

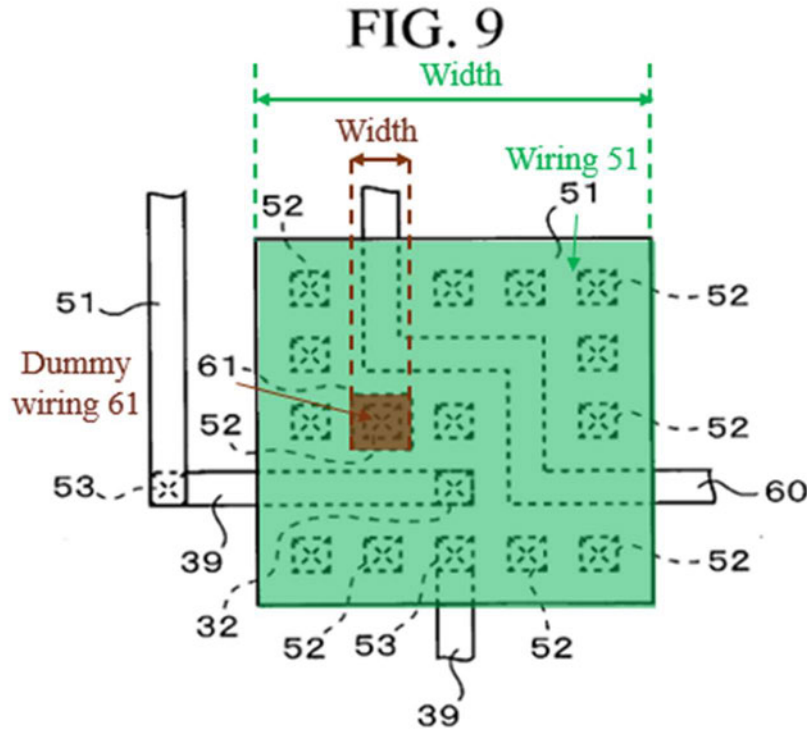
TSMC-1005, Fig. 10. Positioning the dummy interconnect beneath Hasunuma's dummy via/reinforcing plug 28 would merely have involved patterning and creating the dummy interconnect in the same layer and manner as conductive layer 14 using the same processing techniques already used in Hasunuma to create conductive layer 14. Reinforcing plug 28 could then have been easily connected to the dummy interconnect using the same processing techniques already disclosed in Hasunuma as being used to create reinforcing plug 28 and conductive plug 27 (whereby conductive plug 27 is connected to conductive layer 14).

2. Claim 8 - *The method of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect.*

329. Claim 8 recites that “the first dummy interconnect has a width smaller than that of the second interconnect.” As described above for claim 2, the combination of Hasunuma and Watanabe teaches a first dummy interconnect and a second interconnect. *Supra*, §§X(E)(1)(1[d]), X(F)(1).

330. Watanabe teaches the well-known understanding of a POSITA at the time that interconnects and dummy interconnects can have a variety of sizes and shapes depending on the design requirements for the specific device at issue. In particular, Watanabe teaches that a dummy interconnect could be configured to have a smaller width than an upper level interconnect (such as the claimed “second interconnect”). Annotated Figure 9 of Watanabe discloses a dummy interconnect

(e.g., “dummy wiring 61”) having a smaller width than the second interconnect (e.g., “wiring 51”) (TSMC-1004, Fig. 9, ¶[0125]; *see also id.*, ¶[0105]):



331. Thus, as clearly shown in Figure 9 above, Watanabe teaches that the specific relative sizing (including relative widths) of dummy interconnects and functional upper level interconnects, including the functional upper level interconnect being larger than dummy interconnect such as in Figure 9, was a mere design choice that a POSITA was well aware was a design option at the time. Indeed, a POSITA would have recognized that implementing such relative sizing of dummy interconnect and second interconnect into Hasunuma’s device could simply be accomplished by substituting interconnects having such relative sizes/widths into

Hasunuma's devices (including the device discussed above for claim 2 resulting from the obvious combination of Hasunuma and Watanabe).

332. The '751 patent does not appear to give any express reason for the such relative sizing between the dummy interconnect and second interconnect, and thus a POSITA would not have gleaned any criticality or unexpected results associated with these relative feature sizes from the discussion in the '751 patent.

333. A POSITA would have been further motivated in certain instances to use a wider width second interconnect (as compared to the dummy interconnect) to provide a relatively larger and wider "second interconnect" which would have provided more space for additional via connections and thus connections to other circuit elements. Having a larger, wider upper interconnect enables connection to more functional vias and corresponding wirings, thus enabling more complex circuits and expanding the design options available to the circuit/device designer. Thus, in situations where the circuit design required such additional space for the second interconnect, a POSITA would have chosen such wider interconnects for use in the semiconductor device. Figure 9 of Watanabe discloses such a larger upper interconnect, which is useful for additional connections and dummy vias. Indeed, as demonstrated above, have a wider upper interconnect permits space for a much greater number of dummy vias, which will accumulate for vacancies as compared to

smaller, narrower interconnects having fewer dummy vias, thus further mitigating vacancies from migrating to functional vias.

334. It was common prior to the '751 patent for higher-level interconnects to be relatively larger than lower-level interconnects (including dummy interconnects) to accommodate more connections, carry more current, reduce resistance, and meet electromigration rules. TSMC-1034, 585-86, 591, Figs. 12-17, 12-18. Additionally, dummy interconnects on the same level as the first interconnect (i.e., closer to the semiconductor substrate) can more easily be made with relatively smaller widths than interconnects on the next level up. Smaller width dimensions are also desired lower in the interconnect structure because a greater concentration/density of wiring is needed to connect to transistors in the semiconductor substrate, thus necessitating features having smaller widths to achieve the needed layout density at lower layers. See, e.g., TSMC-1034, 585-86, 591, Figs. 12-17, 12-18. Dummy interconnects at the lower interconnect levels likewise have to maintain the same general dimensions as the active wires at that same level to maintain pitch requirements and allow for efficient routing and wiring density. In contrast, higher levels typically carry more current and need better heat dissipation, giving rise to relatively wider interconnect widths higher in the structure. TSMC-1012, 34; TSMC-1034, 594. This need to implement smaller features at the

lower interconnect levels would have applied equally to the first interconnects as well as dummy interconnects.

335. Still further, it was typical for interconnect widths to increase when moving up levels in an interconnect structure because as the levels build on top of each other, it can become more challenging for CMP to produce surfaces having the same level of smoothness as lower levels. And surface smoothness impacts the lithography resolution that can be achieved, such that minimum interconnect widths are typically larger the higher up one is in the interconnect structure. The specific desired width for any given application would take into account known design considerations, and Watanabe provides one such example that demonstrates the known nature of an active interconnect (wiring 51) being wider than the dummy interconnect 61.

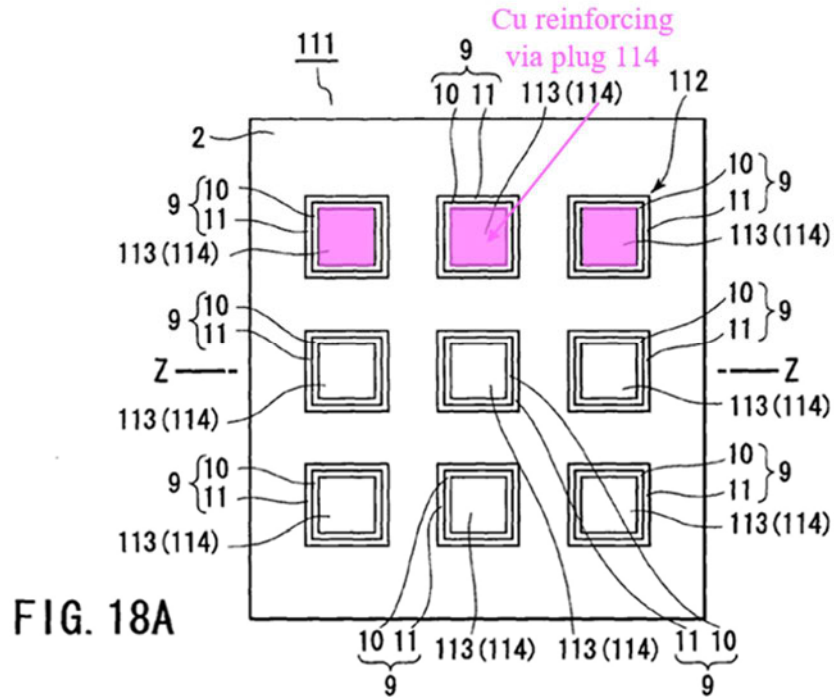
336. A POSITA would have considered such a modification likely to be successful, given that it merely requires changing the relative sizes of the dummy and second interconnects, which would have been easily achieved using standard processing techniques at the time. Both Kurashima and Watanabe teach adding dummy interconnects with different widths relative to interconnects, demonstrating that width selection was merely a design choice that depended on the intended device application and circuit design considerations. A POSITA would have understood that such interconnects could be easily created by merely etching trenches to the

appropriate desired size in the insulating film in which the interconnects were formed. *See, e.g.*, TSMC-1016, 6:14-29; TSMC-1028, 5458. Tailoring the size, location, etc., of such trenches (and thus the resulting interconnect formed in trench) was routinely performed. Indeed, it was and is performed for the fabrication of every such semiconductor device.

3. Claim 10 – The method of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square

337. Claim 10 recites that “a planar shape of each of the via and the dummy via is substantially a square,” which Hasunuma in view of Watanabe renders obvious.

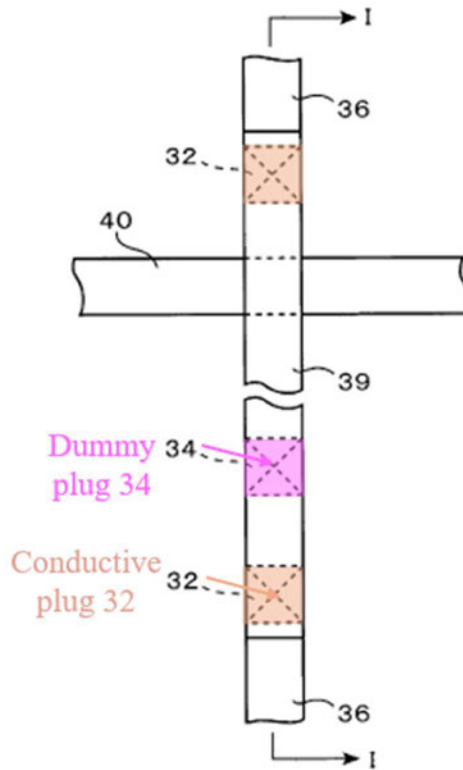
338. Hasunuma discloses planar views of dummy vias 114 that are square, for example, in Figure 18A (TSMC-1005, Fig. 18A):



339. Thus, given Hasunuma's clear disclosure of square-shaped vias in Figure 18A and the common usage at the time of square-shaped vias, a POSITA would have understood Hasunuma to disclose substantially square-shaped vias as an option for any of the vias or dummy via in any of its embodiments.

340. Additionally, Watanabe's plan view figures (e.g., Figures 2, 4, and 9) consistently disclose square vias and dummy vias (plugs 32 and dummy plugs 34, respectively). *Supra*, §X(A)(7). As one example, annotated Figure 2 of Watanabe is shown below with the square-shaped vias and dummy vias denoted:

FIG. 2



341. It was obvious in view of both Hasunuma's and Watanabe's disclosures of square vias and the knowledge of a POSITA at the time to make both the planar shape of the vias and the dummy vias in Hasunuma's various embodiments substantially square.

342. Both Hasunuma and Watanabe address similar problems (reliability in damascene interconnect structures) with similar foundational solutions (dummy vias extending from the interconnect above). It would have been nothing more than a simple substitution to adopt Watanabe's specific via/dummy via shapes. For example, choosing specific shapes (e.g., square) as taught by Watanabe would be

routine design choices to meet particular layout or process requirements within Hasunuma's framework. Indeed, Iizuka teaches square cross-sectional shapes for vias: "the opening of the via-hole may have any configuration, such as a square, rectangle or circle," and a circular/square pattern means the resulting via formed in a circular/square hole would have a substantially circular/square shape. TSMC-1008, 9:44-47, 10:17-22.

343. In addition, via shapes, such as square or circular, each provide known advantages applicable to a given situation. For example, square-shaped vias align more efficiently with orthogonal interconnect lines, leading to a more compact layout and better utilization of area compared to circular vias in such scenarios to achieve increased contact area with interconnects above and below the via. *See, e.g.*, TSMC-1014, ¶[0092], Figs. 8, 14 (teaching square vias as preferred for certain interconnect junctions); TSMC-1039, 5:27-32 (noting the increased electrical contact area achieved by square vias). A POSITA would have recognized that the fundamental mechanical strength enhancing function of Hasunuma's dummy vias (as well as the electrical-connection function of Hasunuma's active vias), would be achieved with vias having square cross-sections.

344. Further, because a POSITA was aware of the basic available via shapes, and was aware of the role of the dummy vias in providing a mechanical strengthening function (*supra*, §IX.B) as well as reducing stress-induced voiding

and electromigration problems as taught, for example, by Watanabe (*supra*, §IX.A), it would have been a matter of routine optimization to choose the via shape that works best for a given overall design. With a few basic shapes to choose from (e.g., circular, square, rectangular), it would not have required an undue amount of experimentation to arrive at the optimal via shape.

345. A POSITA would have had a reasonable expectation of success in implementing Hasunuma's vias (both functional and dummy) with a square cross-sectional shape, as this would easily be accomplished using the standard patterning and manufacturing techniques used to make the interconnect structure in general. Certainly it was well known how to pattern via holes having square cross-sections using masks, photolithography, and etching, and such square patterns subsequently result in square vias when conductive material is deposited into the patterned vias holes. TSMC-1004, Figs. 2, 4, 5, 9; TSMC-1005, Fig. 18A; TSMC-1014, ¶[0092], Figs. 8, 14; TSMC-1039, 5:27-32.

346. Accordingly, claim 10 is obvious over Hasunuma and Watanabe.

H. Ground 8: Aoyagi renders obvious Claims 1, 3-4, 7, 14-16, and 19

347. I believe that each of claims 1, 3-4, 14-16, and 19 is obvious over Aoyagi for at least the reasons discussed below.

1. Claim 1

1[pre] "A Method for Fabricating a Semiconductor Device"

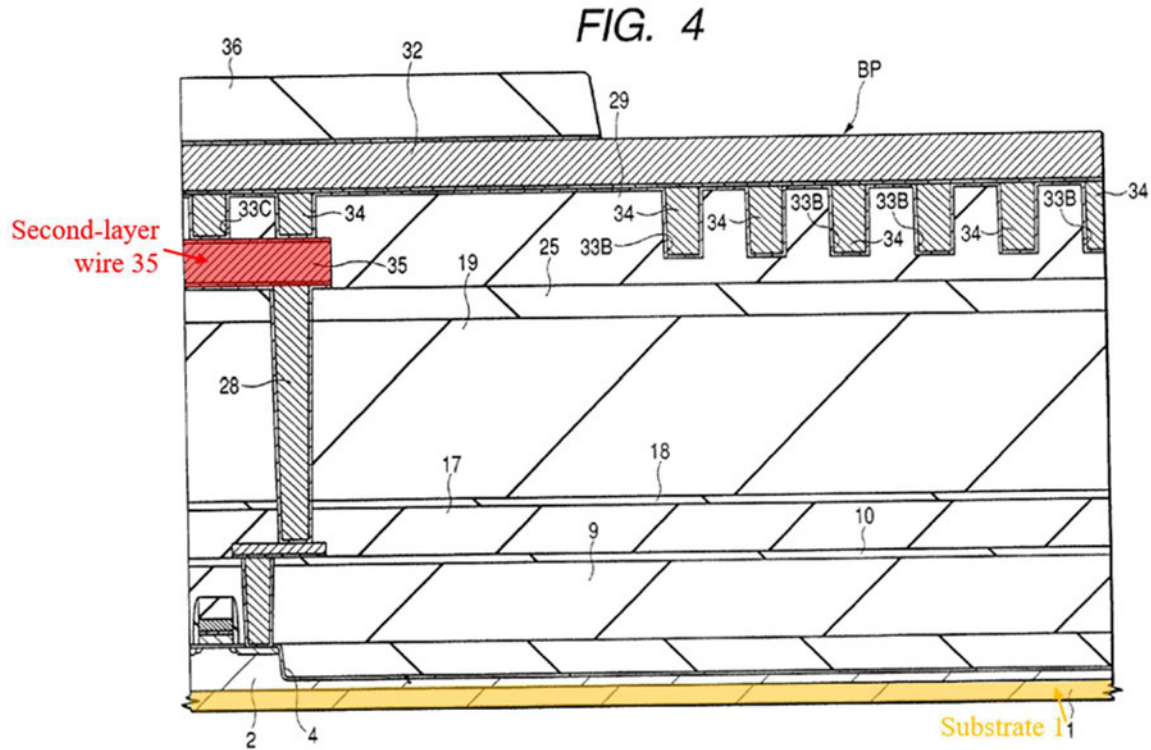
348. Aoyagi is directed to a “technique of manufacturing” a semiconductor device, and thus satisfies claim 1’s preamble. TSMC-1006, ¶¶[0001], [0012]-[0017], Figs. 4-12, 19.

1[a] “Forming a First Interconnect”

349. Aoyagi discloses forming a first interconnect (e.g., “second-layer wire 35”) on a semiconductor substate (e.g., “substrate 1”). TSMC-1006, ¶¶[0055], [0040], [0043], [0061], Figs. 4, 7-8. Aoyagi describes its interconnects using the term “wire” or “bonding pad” (e.g., “first-layer wire,” “second-layer wire,” “third-layer wire,” “bonding pad BP”). A POSITA understood that such wires and bonding pad BP of Aoyagi constitute “interconnects” as those terms are understood in the art because both Aoyagi’s wires and bonding pad BP are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:21-28. Wires/bonding pads/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:37-39.

350. Aoyagi explains that “lead wire 32 is connected, at the other end, with a **lower (second-layer) wire 35** via 33C in the interlayer insulating film 29”

(TSMC-1006, ¶[0055]), which is formed on “substrate 1” as disclosed in annotated Figure 4:¹⁰



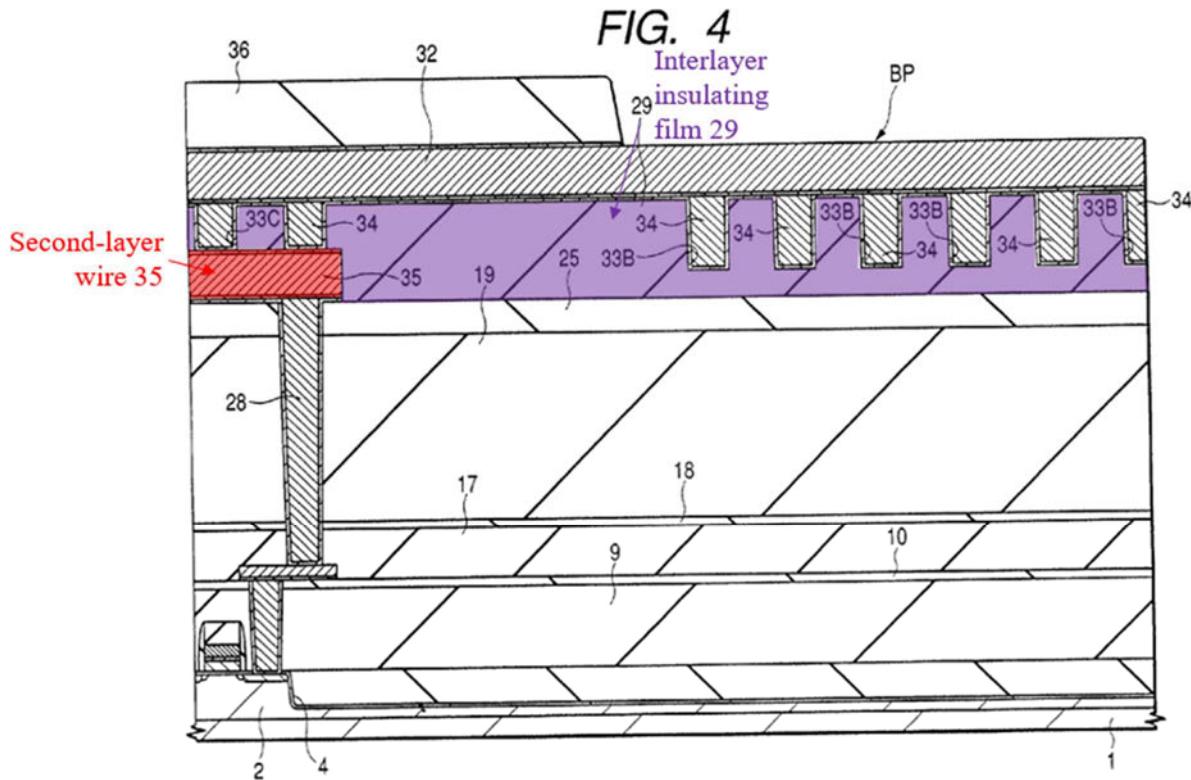
351. Paragraph [0061] of Aoyagi further explains that “second-layer wire 26 is formed on the silicon oxide film 25 at the memory portion, and a second-layer wire 27 is formed on the silicon oxide film 25 at the peripheral circuit portion.” Figure 19 discloses a “lower wire 54,” which a POSITA would understand to be analogous to “second-layer 35” given that it is similarly formed in the immediate

¹⁰ For the dual damascene embodiment in Figure 19, the second-layer wire 35 is formed in the insulating film that is underneath insulating film 29.

layer under bonding pad BP and connected to bonding pad BP by vias. *See id.*, Fig. 19, ¶¶[0074], [0077].

1[b] “Forming a First Insulating Film”

352. Aoyagi discloses forming a first insulating film (e.g., “interlayer insulating film 29”) on the first interconnect (e.g., “second-layer wire 35”). TSMC-1006, ¶¶[0049], [0062], Fig. 4. Aoyagi explains that “interlayer insulating film (first interlayer insulating film) 29, which is made of a three-layered insulating multi-layered film consisting, for example, of a silicon oxide film, a spin-on-glass (spin coating) film and a silicon oxide film, is formed over the **second-layer wires** 26, 27.” TSMC-1006, ¶[0049]. A POSITA, considering this disclosure together with Fig. 2, would understand that ***second-layer*** wire 35 is similarly formed with respect to interlayer insulating film 29 as “second-layer” wires 26, 27. This is shown in annotated Figure 4:



353. Thus, given the common layers in Aoyagi's figures and common reference "second-layer wire" for each of wires 26, 27, and 35, a POSITA would recognize that the "interlayer insulating film 29" is formed on the "second-layer wire 35" just like is formed on "second-layer wires 26, 27." Indeed, a POSITA would understand that each layer of the device is formed using a common fabrication technique applied commonly to the various similar components on that layer, and thus each wire formed on the second layer would be formed in the same manner.

1[c] "Forming in the First Insulating Film, a Via Hole, a Dummy Hole and an Interconnect Trench"

354. Aoyagi teaches forming in the first insulating film (e.g., "interlayer insulating film 29"), a via hole (e.g., "through-hole 33C") connected to the first

interconnect (e.g., “second-layer wire 35”), a dummy hole (e.g., “hole 33B”) which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench (e.g., “upper wire groove 56”) connected to the via hole and the dummy hole. TSMC-1006, ¶¶[0077], [0055]-[0056], Figs. 4, 19.

355. Regarding formation of via and dummy holes, Aoyagi explains that “[i]n the interlayer insulating film 29 beneath the bonding pad BP, a plurality of **holes 33B** are formed at certain intervals.” TSMC-1006, ¶[0052]. In addition, “a through-hole 33A [is] formed in the interlayer insulating film 29.” *Id.*, ¶[0050]. Likewise, “through-hole 33C” is “formed in the interlayer insulating film 29.” *Id.*, ¶[0055], Fig. 4. In short, all holes 33A, 33B, 33C are formed in the insulating film 29.

356. Given Aoyagi’s discussion of using a dual damascene process to form wire 31/bonding pad BP and deposit conductive material in holes 33A and 33B, a POSITA would understand Aoyagi to teach and/or suggest using a dual damascene process to form bonding pad BP (with lead wire 32) as well as the vias formed in holes 33C and the dummy vias in holes 33B in the structure of Figures 3-4 as discussed above. *Supra*, §IX(C). A POSITA was motivated to do so by the well-known benefits associated with the dual damascene process, which include manufacturing simplicity and increased efficiency (afforded by forming the vias and interconnects simultaneously rather than serially), reduced cost, and increased

reliability. *Supra*, §§X(A)(1)(1[pre]), IX(C). Additionally, a POSITA would have certainly recognized that use of the dual damascene process in this manner could have been easily implemented given its already disclosed use in Aoyagi and its general widespread use in industry at the time and, thus, would have expected success in using the dual damascene process in this manner. *See* TSMC-1034, 583-84, 671-76, 695, 698, 718, 723-26; TSMC-1015, 3:63-4:23; *supra*, §§VI(A); X(A)(1)(1[pre]); *see also* TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-150; TSMC-1027, 25; TSMC-1028, 5458.

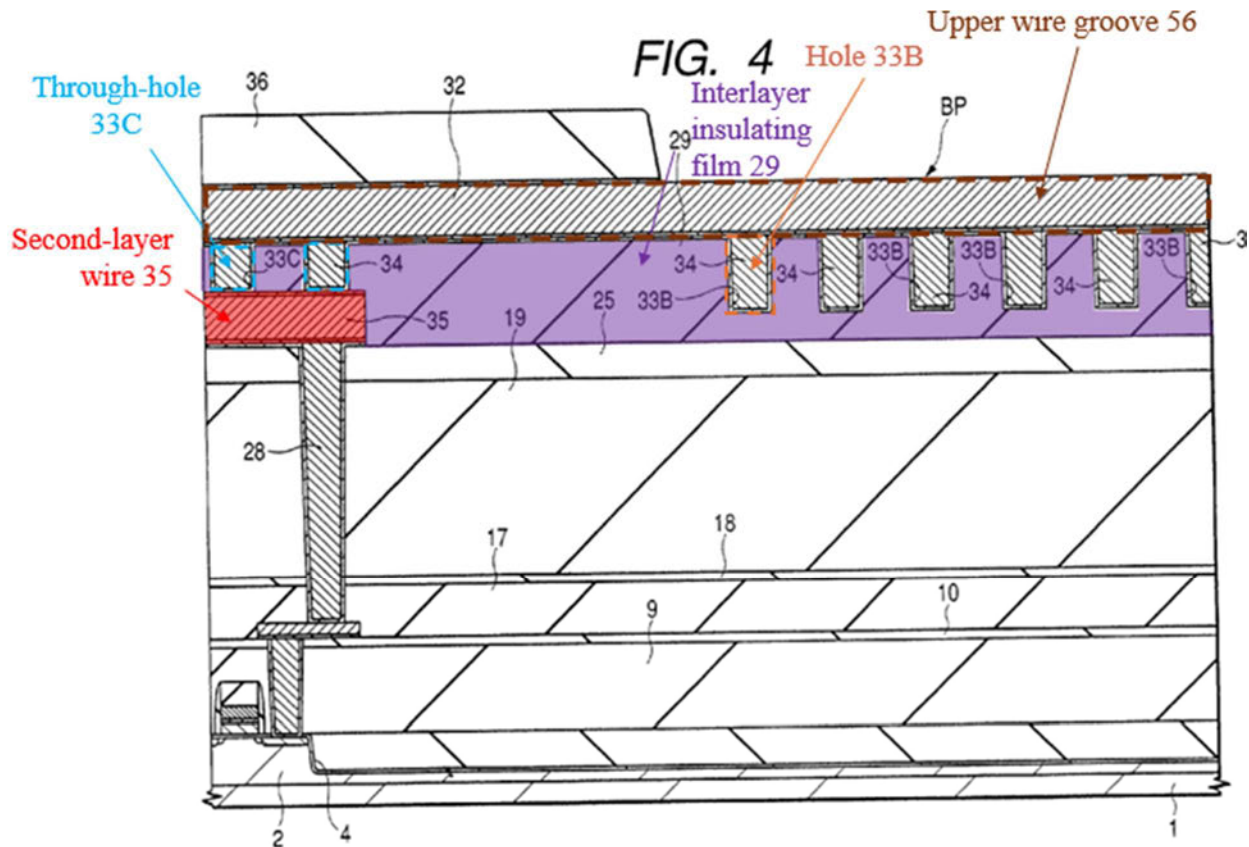
357. Indeed, the nature of and advantages associated with dual damascene were well understood in the art. *See, e.g.*, TSMC-1019, 146-147 (stating that dual damascene enhances density and performance and promotes reliability and improves manufacturability, including manufacturing yield); TSMC-1027, 25 (noting dual damascene forms Cu wires and vias with one metal fill and one CMP step, providing process simplification allowing for reduced cost and improved manufacturability); TSMC-1028, 5458 (discussing that, with making one level of lines and one level of vias together, can build more levels of Cu interconnects with same number of processing steps). Regarding simplified and more efficient manufacturing, a POSITA was aware that: “The dual-damascene process offers the advantage of reducing the number of process steps” (TSMC-1034, 695); “The reduction in the number of processing steps is another of the benefits that have driven the

development of dual-damascene processes” (*id.*, 698). The foregoing benefits are easily recognized when compared to other manufacturing process (e.g., single damascene) where interconnect trenches and vias are independently formed one step at a time, a much more time consuming and thus oftentimes expensive process.

358. Regarding formation of an interconnect trench, for the dual damascene approach, Aoyagi discloses an upper wire groove 56 formed in the insulating film 29. TSMC-1006, ¶[0077], Fig. 19. A “third-layer wire 31” or “upper wire 31” – which includes the bonding pad BP – is deposited in wire groove 56. *Id.*; *see also* TSMC-1015, 3:63-4:22.

359. A POSITA would recognize that, for Aoyagi’s dual damascene approach, the upper wire groove 56 (for upper wire 31 and bonding pad BP) would connect the via holes 33B and dummy holes 33C. The holes 33B and 33C are illustrated in annotated Figure 4:¹¹

¹¹ In the case where the Figure 19 dual damascene approach is utilized to create the second-layer wirings, the second-layer wire 35 is in a separate insulating film that is just underneath the insulating film 29.



360. A POSITA would understand that Aoyagi's holes 33B are "arranged so as to be incapable of having current flow therethrough." As illustrated in Figures 4 and 19, holes 33B and plugs 34 therein are formed entirely within the insulating film 29. As illustrated in Figures 4 and 19, these "dummy" holes 33B and "dummy" plugs 34 are only connected on one end to an active circuit element (i.e., "bonding pad BP"), while the other end is not connected to a second active circuit element. The purpose of the dummy holes 33B (and the associated plugs 34 formed therein) is so that "adhesion between the bonding pad BP and the lower interlayer insulating film 29 can be improved." TSMC-1006, ¶[0053]; Fig. 4. Thus, a POSITA would recognize that no current can flow through Aoyagi's dummy holes 33B or (dummy

plugs 34 formed therein) due to this lack of connection to a second active circuit element. Instead, current flows between Aoyagi's second-layer wire 35 and bonding pad BP through plugs formed in vias/holes 33C, which constitute parts of a closed circuit in actual use of the device. *See id.*, ¶[0055] ("The bonding pad BP is connected at one side thereof with one end of a lead wire 32. The lead wire 32 is connected, at the other end, with a lower (second-layer) wire 35 via 33C formed in the interlayer insulating film 29."), Figs. 3-4.

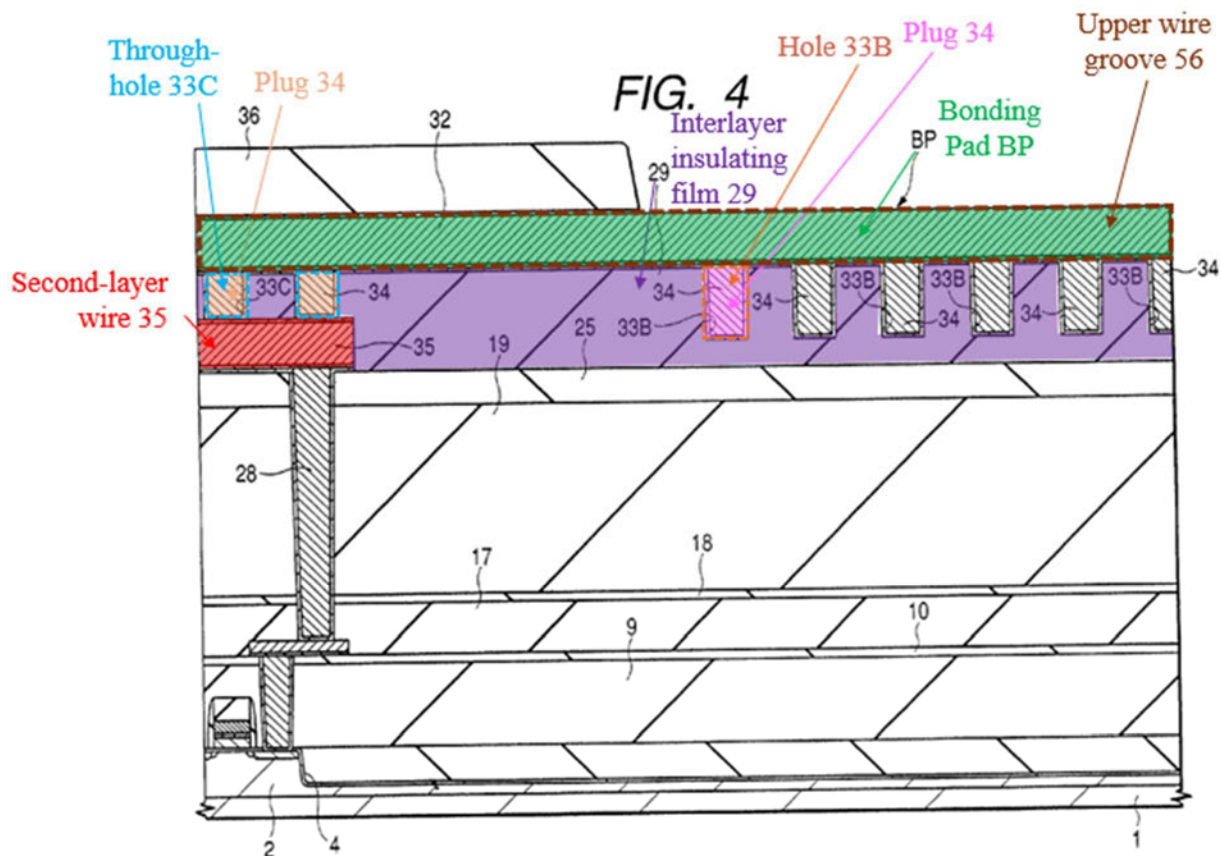
361. Moreover, a POSITA would understand that Aoyagi's device would still be operable if holes 33B (and the plugs therein) were omitted, because current would still flow through the active circuit elements (i.e., bonding pad BP, holes 33C (and plugs 34 therein), and second-layer wiring 35) during actual use of the device. Indeed, holes 33B and their associate plugs have no impact on the actual operation of the circuit.

362. Thus, a POSITA would have understood that holes 33B and plugs 34 therein are "arranged so as to be incapable of having current flow" as claimed because they do not constitute parts of a closed circuit during actual use of the device and the conductor device would function without them.

363. Thus, Aoyagi satisfies limitation 1[c].

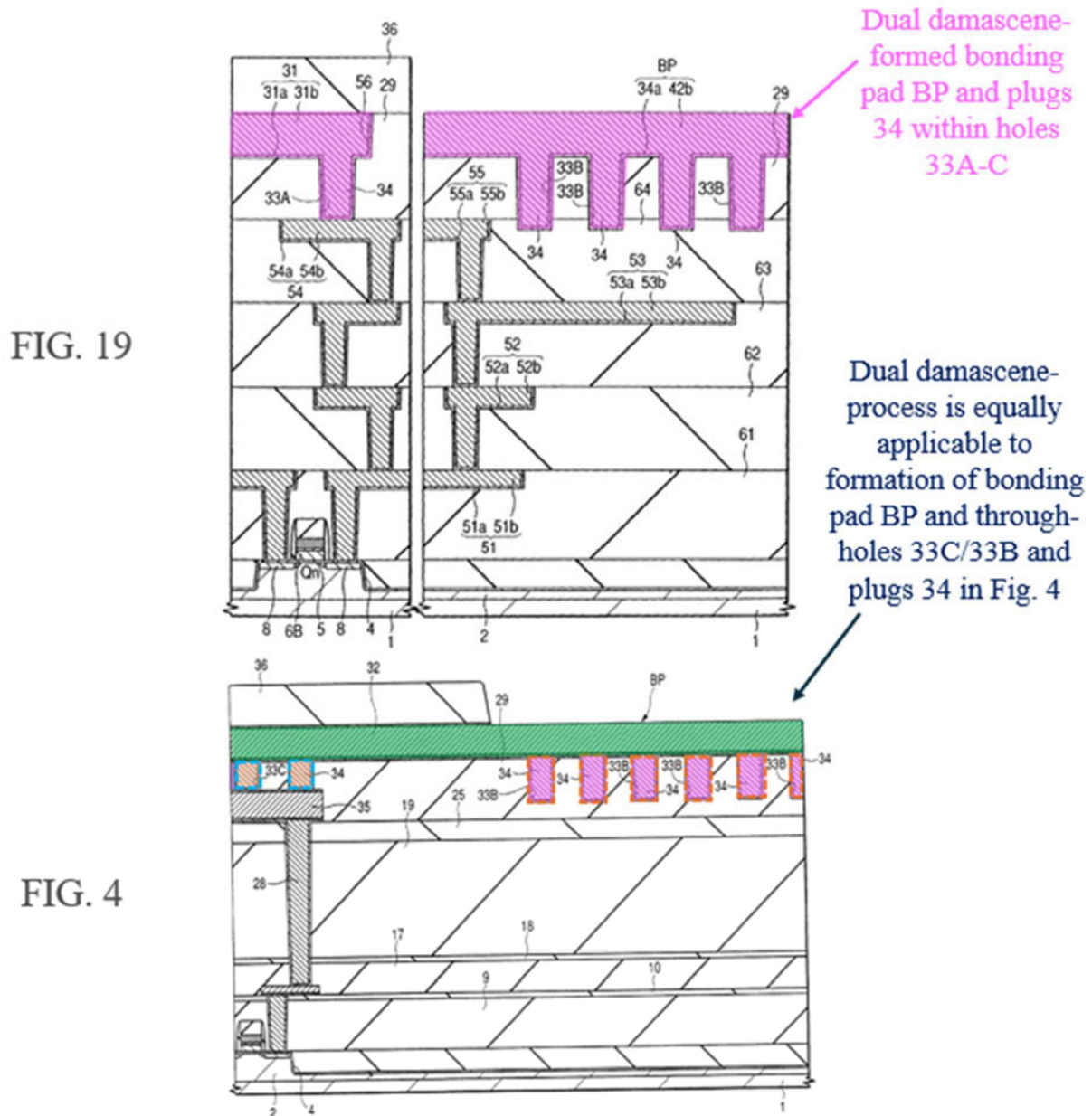
1[d] "Depositing a Conductive Material in the Via Hole, the Dummy Hole and the Interconnect Trench"

364. Aoyagi discloses depositing a conductive material (e.g., “barrier metal film 34a,” “Al alloy film 31b, 42b”) in the via hole (e.g., “through-hole 33C), the dummy hole (e.g., “hole 33B”) and the interconnect trench (e.g., “upper wire groove”), thereby forming a via (e.g., “plug 34” in “hole 33C”), a dummy via (e.g., “plug 34” in “hole 33B”) and a second interconnect (e.g., “bonding pad BP”). TSMC-1006, ¶¶[0050]-[0055], [0077], Figs. 2-4, 19.



365. Employing Aoyagi’s dual damascene process, a barrier metal film 34a and “Al alloy film 31b (42b)” is deposited in the upper groove 56, to form third-layer (upper) wire 31 and plugs 34 in holes 33B, 33C. TSMC-1006, ¶¶[0055],

[0077]. Indeed, a POSITA would have understood that Figure 4's bonding pad BP/lead wire 32 and its associated vias in holes 33C are likewise integrally formed in the dual damascene process together with dummy vias (plugs 34) in holes 33B. This is illustrated in annotated Figures 4 and 19 below:



366. Such a process would result in a similar final structure as shown in Figures 3-4 of Aoyagi except that there would be no thin film layer (e.g., layer 42a in Figs. 2, 4)) between the primary conductive materials in bonding pad BP and the various plugs 34. Indeed, given Aoyagi's discussion of using a dual damascene process to form wire 31/bonding pad BP and to deposit conductive material in holes 33A and 33B and upper wire groove 56, it was certainly obvious to use the dual damascene process to form bonding pad BP/lead wire 32 and the vias formed in holes 33C and 33B in the structure of Figures 3-4, and a POSITA would have expected success in using the dual damascene process. A POSITA would have been motivated to do so by the simplified manufacturing, increased efficiency, reduced cost, and increased reliability benefits of the dual damascene process, and could have easily implemented such a process given its already disclosed use in Aoyagi (and indeed widespread use throughout industry at the time given its associated, well-known benefits). *Supra*, §§X(A)(1)(1[pre]), IX(C), VI(A); *see also* TSMC-1034, 583-84, 671-76, 718, 723-26; TSMC-1015, 3:63-4:22; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract.

367. When utilizing the dual damascene process in this manner, conductive material (e.g., "barrier metal film 34a," "Al alloy film 31b, 42b") is deposited in hole 33C, dummy hole 33B, and upper wire groove 56, thereby forming a via (e.g., "plug

34” in “hole 33C”), a dummy via (e.g., “plug 34” in “hole 33B”) and a second interconnect (e.g., “bonding pad BP”), which satisfies limitation 1[d].

368. Accordingly, Aoyagi satisfies each this limitation of claim 1, rendering claim 1 obvious to a POSITA.

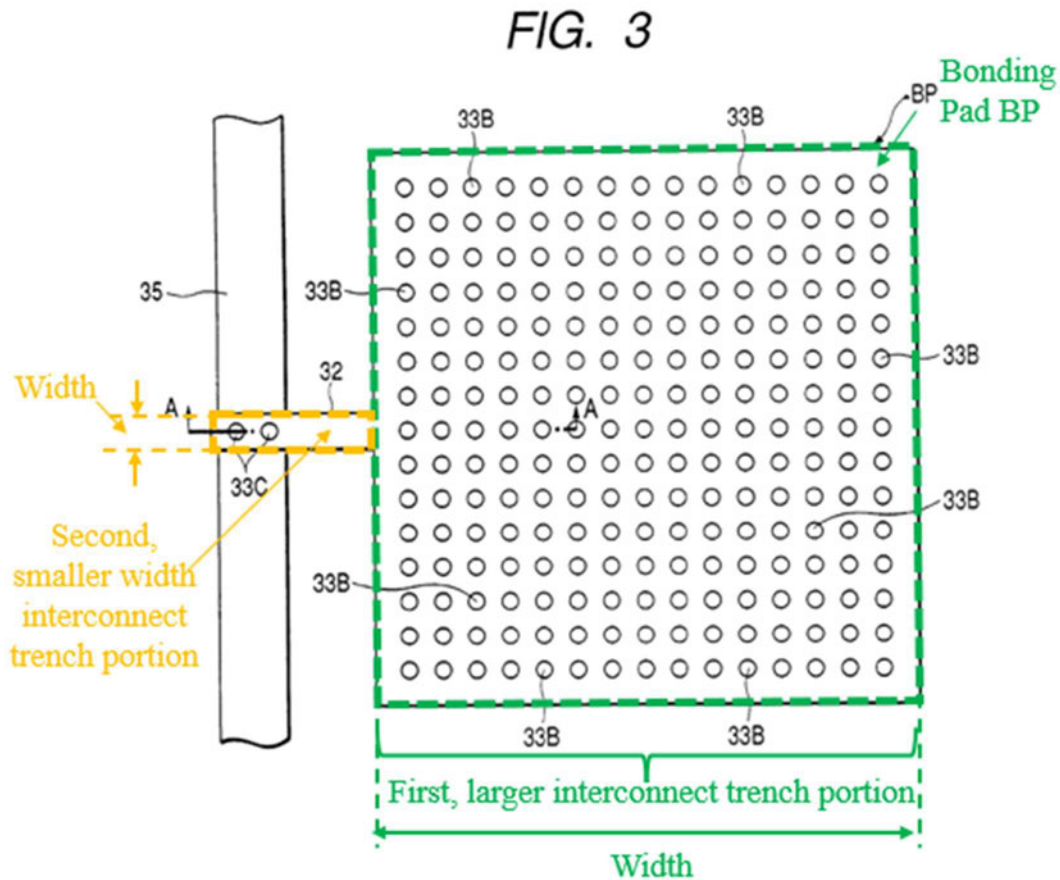
2. Claim 3

[3a] The method of claim 1, wherein in the step (c) the interconnect trench is comprised of a first interconnect trench portion and a second interconnect trench portion whose width is smaller than that of the first interconnect trench portion and which branches from the first interconnect trench portion, and

369. As described for claim 1, Aoyagi discloses step (c), which includes forming in the first insulating film (e.g., “insulating film 29”), ...an interconnect trench (e.g., “upper wire groove”) connected to the via hole and the dummy hole. *Supra*, §X(H)(1)(1[c]). Element 3[a] further defines a specific shape of the “interconnect trench,” specifically that the “interconnect trench is comprised of a first interconnect trench portion and a second interconnect trench portion whose width is smaller than that of the first interconnect trench portion and which branches from the first interconnect trench portion.”

370. As illustrated in Figure 3, Aoyagi’s bonding pad BP includes a first interconnect portion and a second interconnect portion having a smaller width than

the first interconnect portion and branches from the first interconnect portion as required by claim 3:

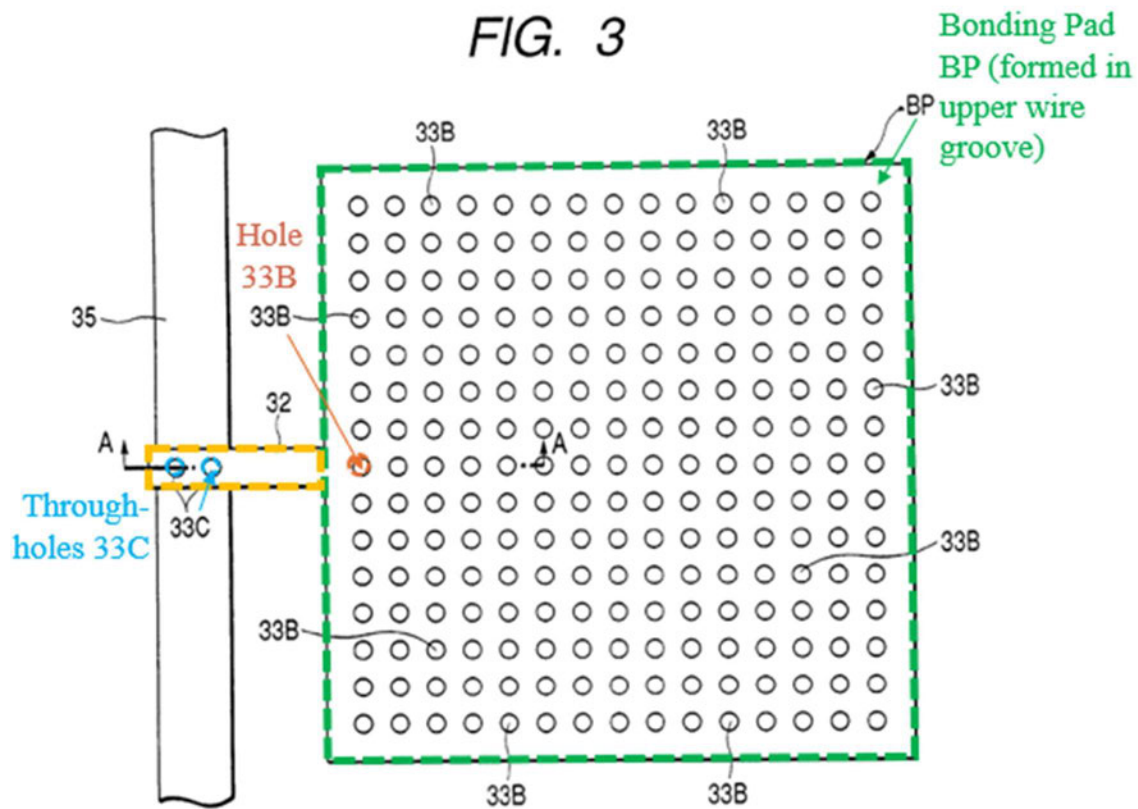


371. As discussed above, Aoyagi discloses a dual damascene process for forming the third-layer wiring that includes bonding pad BP, which would require the creation of a wire groove/interconnect trench in which conductive material is deposited to form the bonding pad/interconnect. The shape of the wire groove/trench would mirror the shape of the resulting interconnect/bonding pad given that the point of the groove/trench is to create a space in the insulating film in which the interconnect is formed. Accordingly, the wire groove/trench used to form

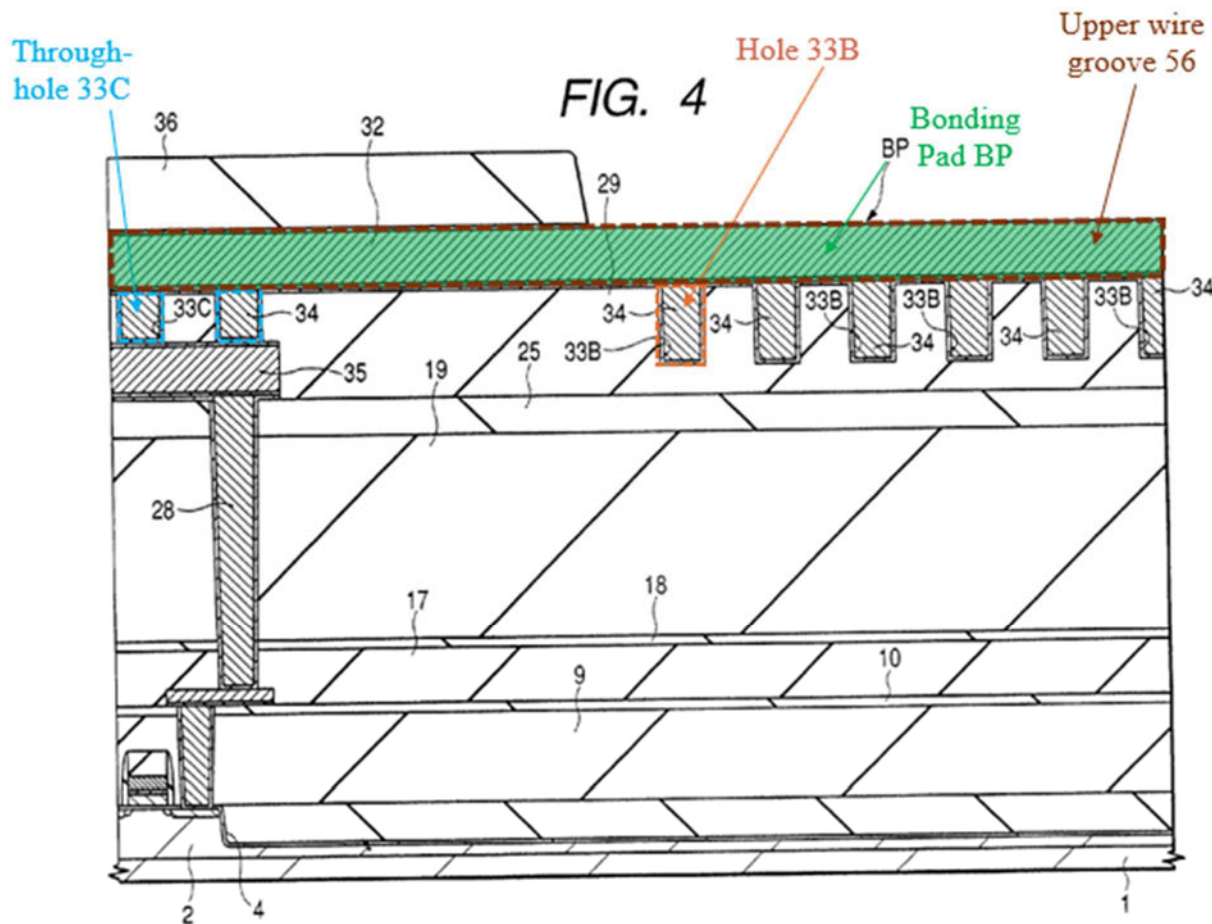
the bonding pad BP disclosed in Aoyagi's Figure 3 would have the same shape as the bonding pad BP, and the POSITA would have expected success in creating the wire groove/trench, thus satisfying claim 3.

[3b] the via hole and the dummy hole are connected to the interconnect trench.

372. As disclosed in Aoyagi's Figure 3, via holes (e.g., "through-holes 33C") and dummy holes (e.g., "holes 33B") are connected to the interconnect trench (i.e., wire groove 56) that is used to form bonding pad BP (TSMC-1006, ¶¶[0054]-[0056], Fig. 3; *supra*, §X(H)(1)(1[c])):



373. As shown below in annotated Figure 4, and indeed as required by the very nature of the dual damascene process itself, the via hole (e.g., “hole 33B”) and the dummy hole (e.g., “through-hole 33C”) are connected to the interconnect trench (e.g., “upper wire groove 56”) when the bonding pad BP and associated vias and dummy vias are formed using the dual damascene process described by Aoyagi.



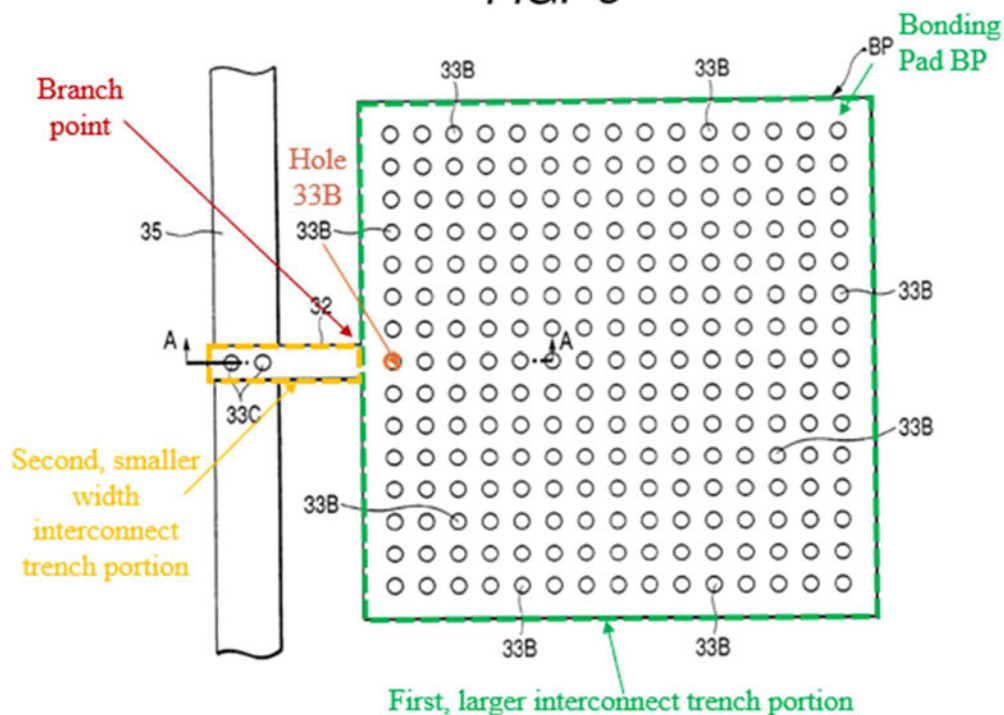
374. Thus, Aoyagi satisfies limitation 3[b].

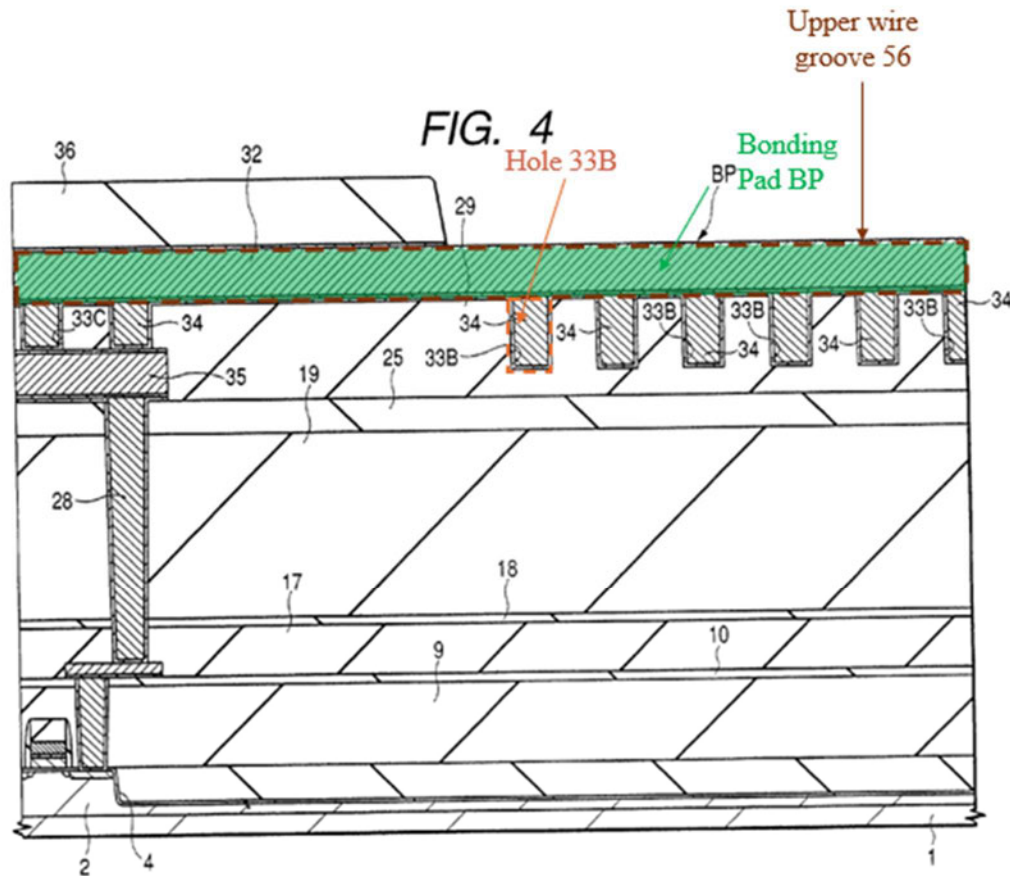
3. **Claim 4 - The method of claim 3, wherein in the step (c) the dummy hole is connected to the branch point between the first and**

second interconnect trench portions or to the interconnect trench near the branch point.

375. As shown in annotated Figures 3 and 4, dummy holes 33B are connected to the upper wire groove 56 used to form bonding pad BP. The dummy holes 33B and upper wire groove 56 are connected at a location near the corresponding branch point between the first and second portions of the upper wiring groove that form bonding pad BP as shown in annotated Figures 3 and 4 (*see* TSMC-1006, Figs. 3-4):

FIG. 3



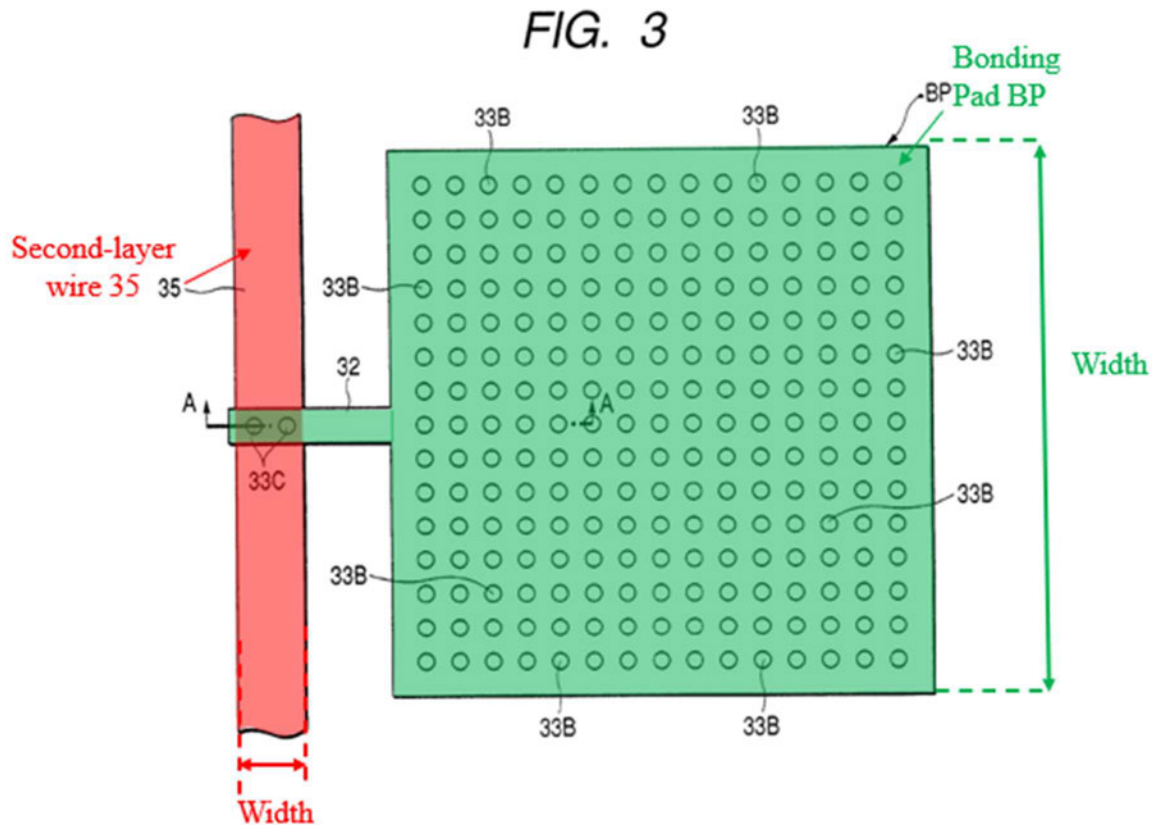


376. In view of the disclosed location of dummy holes 33B relative to the first and second portions of the upper wire groove/bonding pad BP and the branch point therebetween, a POSITA would understand that, during step (c), such dummy holes 33B are connected to the interconnect trench used to form the upper wire groove (in which bonding pad BP is formed) at a corresponding location near the branch point, and the POSITA would have expected success, thus satisfying claim 4.

4. **Claim 7 - The method of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect.**

377. Claim 7 recites that “the first interconnect has a width smaller than that of the second interconnect,” which Aoyagi discloses.

378. As demonstrated in annotated Figure 3 below, a POSITA would plainly recognize from this figure that Aoyagi’s first interconnect (second layer wire 35) has a width smaller than either width of the second interconnect (bonding pad BP)”



TSMC-1006, Fig. 3.

5. **Claim 14 - *The method of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via.***

379. As disclosed in annotated Figures 4 and 19 below, a bottom of Aoyagi’s dummy via (“plug 34” formed within “hole 33B”) is located deeper than a bottom

of the via (e.g., “plug 34” formed with “hole 33C”) (TSMC-1006, ¶[0062], Figs. 4, 19), which satisfies claim 14:

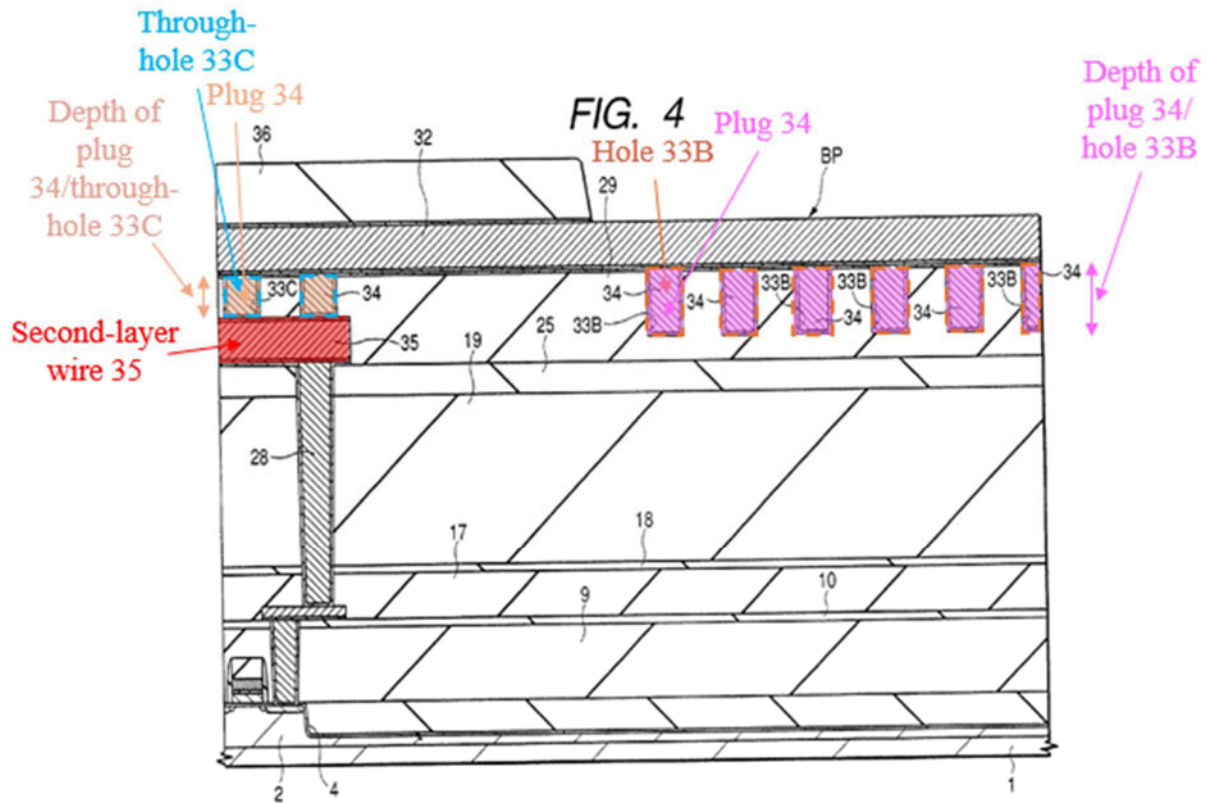
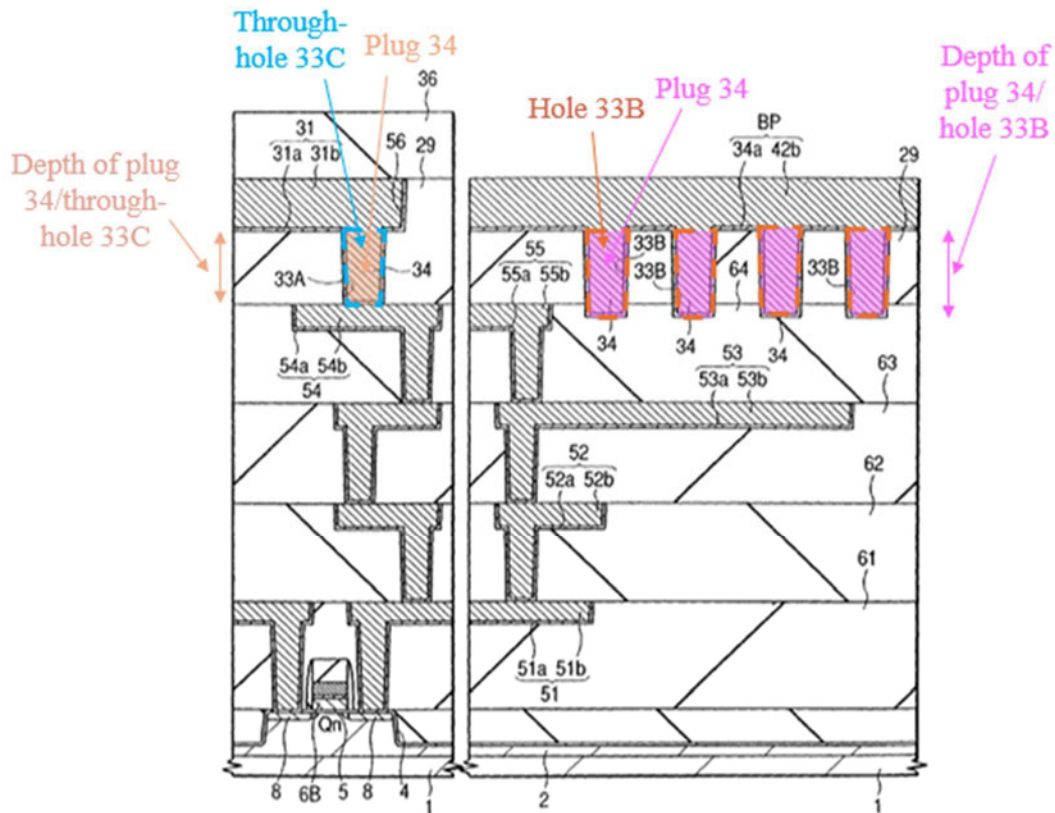


FIG. 19



380. This is due to the overetching process described in Aoyagi, which applies to each of holes 33A, 33B, 33C. For example, Aoyagi explains that “[o]veretching is performed in order to completely remove the interlayer insulating film 29 from the bottom (at the upper portion of the wire 27) of the through-hole 33A, so that the interlayer insulating film 29 at the bottom of the hole 33B, below which no wire is formed, is excessively etched, resulting in the depth of the hole 33B larger than that of the through-hole 33A.” *Id.*, ¶[0062]. Given the similar nature, construction, structure, labeling, and discussion of through-holes 33A and through-holes 33C, a POSITA would readily recognize that through-holes 33C are created in

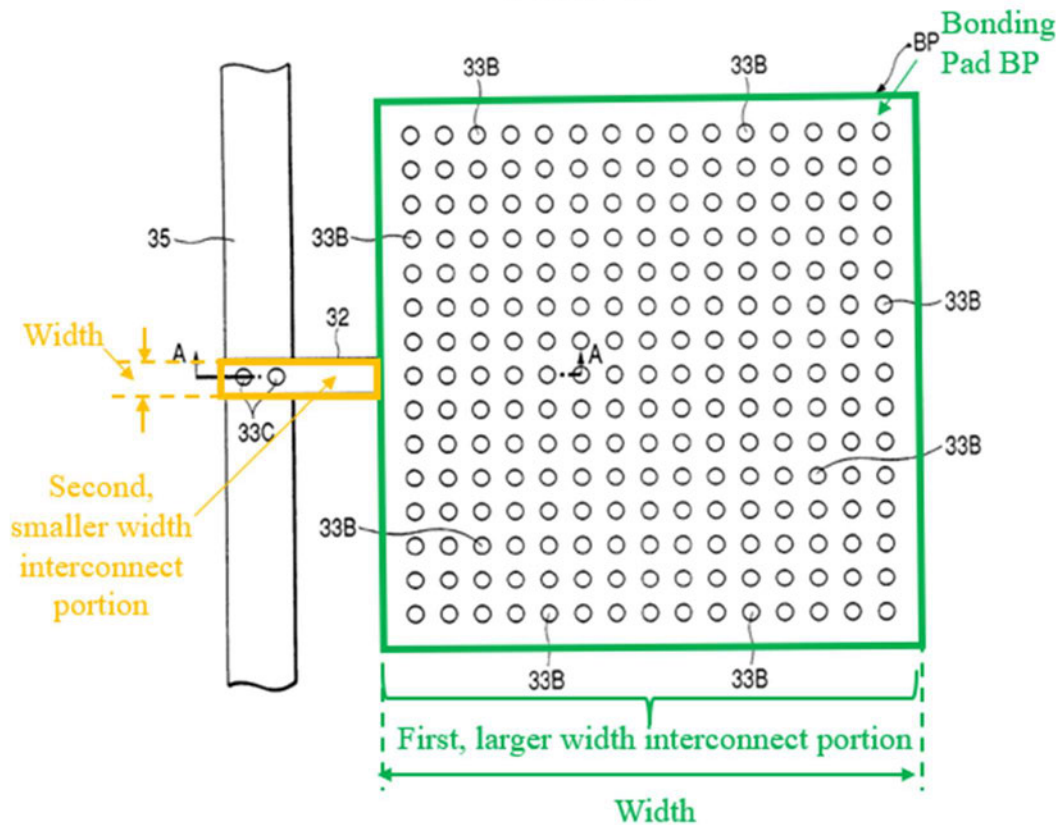
the same manner as through-holes 33A and thus extending to a similar deeper location relative to holes 33B.

6. Claim 15

[15a] The method of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and

381. Element [15a] recites that “the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion,” which Aoyagi discloses.

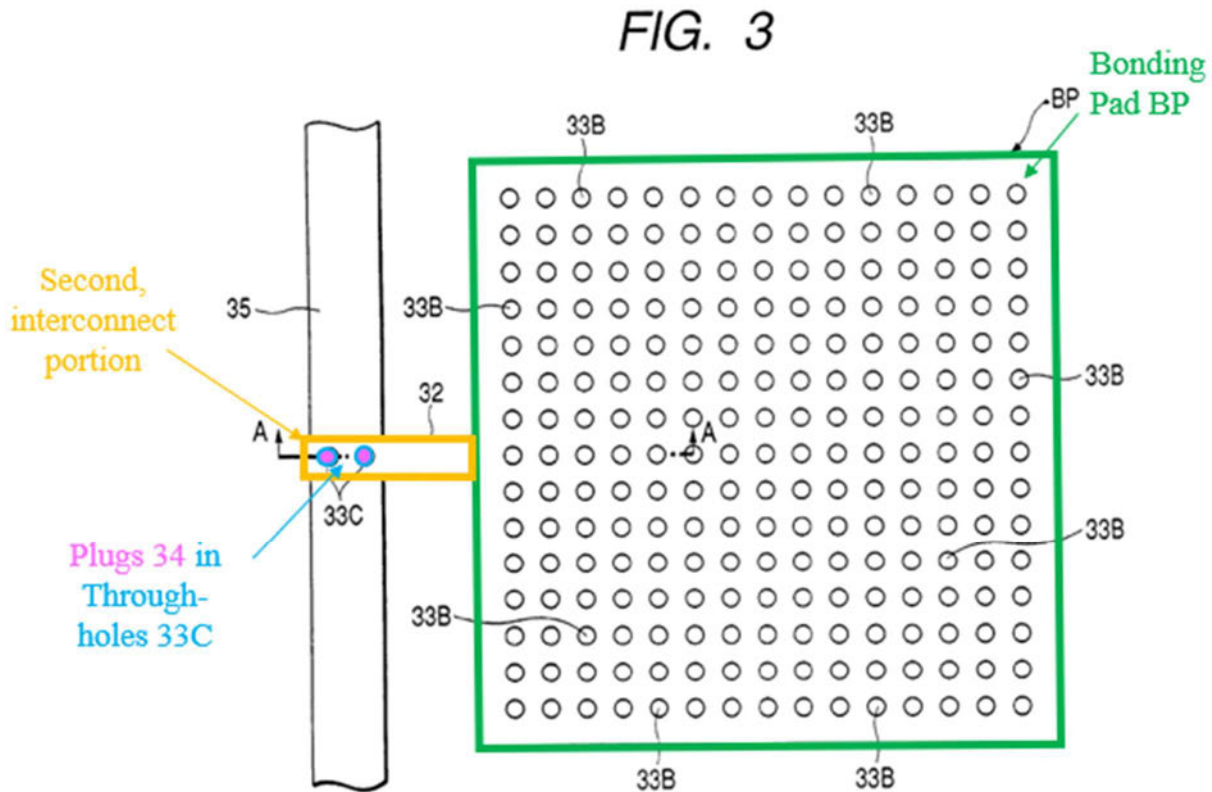
382. As disclosed in annotated Figure 3, Aoyagi discloses a second interconnect (e.g., “bonding pad BP” with “lead wire 32”) having a first interconnect portion (wider portion of “bonding pad BP”) and a second interconnect portion with a smaller width and branching from the first interconnect portion (“lead wire 32” portion of “bonding pad BP”) (TSMC-1006, Fig. 3):

FIG. 3

TSMC-1006, ¶[0055], Fig. 3.

[15b] the via is connected to the second interconnect portion.

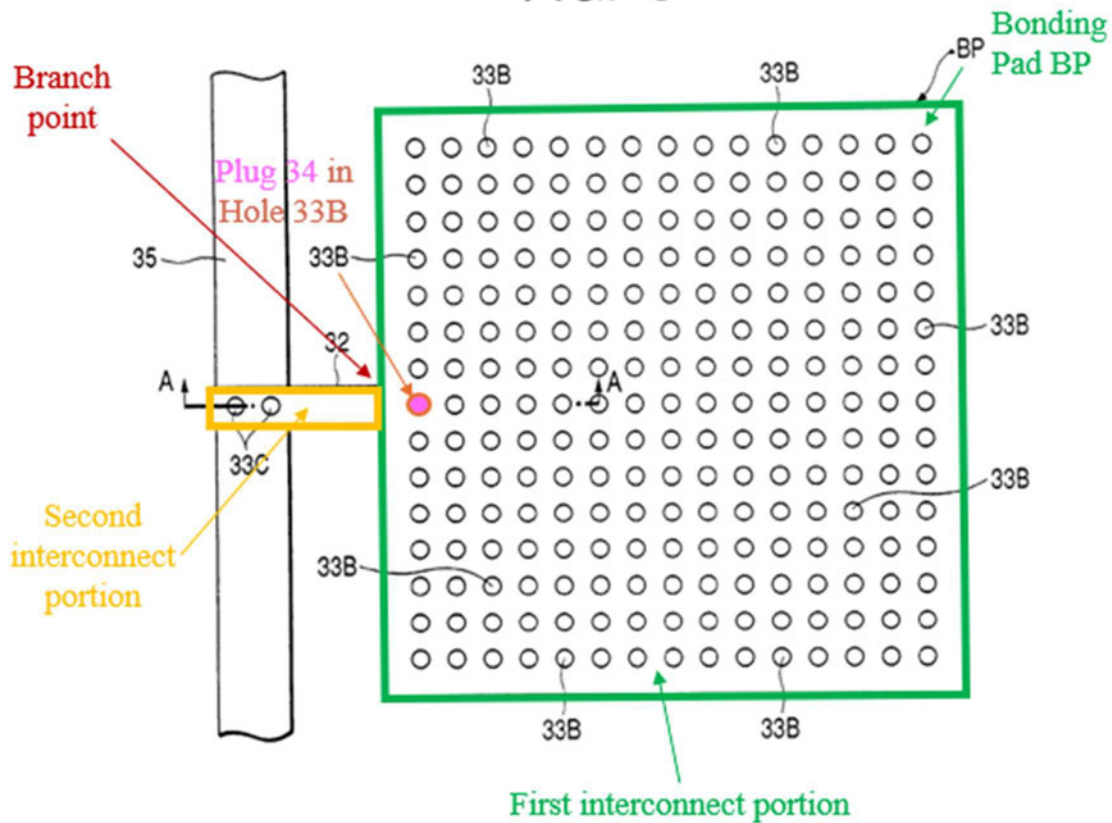
383. Element [15b] states that “the via is connected to the second interconnect portion,” which Aoyagi discloses. As disclosed in annotated Figure 3 below, Aoyagi’s vias (e.g., “plugs 34” formed in “holes 33C”) are connected to the second interconnect portion (e.g., lead wire 32 portion of bonding pad BP). TSMC-1006, ¶¶[0054]-[0055], Fig. 3.



7. **Claim 16 - *The method of claim 15, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions.***

384. Claim 16 recites that “the dummy via is formed at or near the branch point between the first and second interconnect portions,” which Aoyagi discloses. For example, as shown in annotated Figure 3 below, dummy hole 33B (and thus plug 34 therein) is formed near the branch point between the first and second portions (wider bonding pad BP portion, lead wire 32 portion, respectively) of the second interconnect (bonding pad BP), which satisfies claim 16 (TSMC-1006, Fig. 3):

FIG. 3



8. Claim 19 - *The method of claim 1, wherein the dummy via includes a first end and a second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.*

385. Claim 19 recites that “the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film,” which Aoyagi discloses.

386. As disclosed in annotated Figures 4 and 19 below, Aoyagi’s dummy via (e.g., “plug 34” in “hole 33B”) includes a first end and a second end, the first

end connected to the second interconnect (e.g., “bonding pad BP”). TSMC-1006, ¶¶[0050]-[0056], [0077], Figs. 4, 19. Indeed, when formed using the dual damascene process as described above, the first (top) end of the various dummy vias (plugs 34 in holes 33B) would necessarily have to be connected to the bonding pad BP/second interconnect due to the very nature of the dual damascene process.

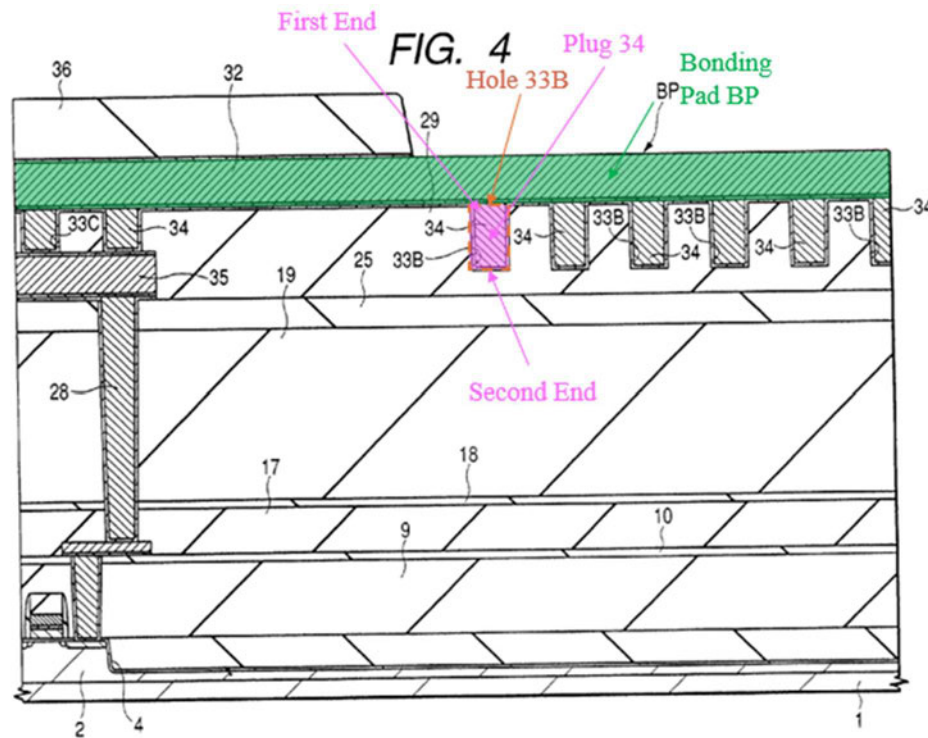
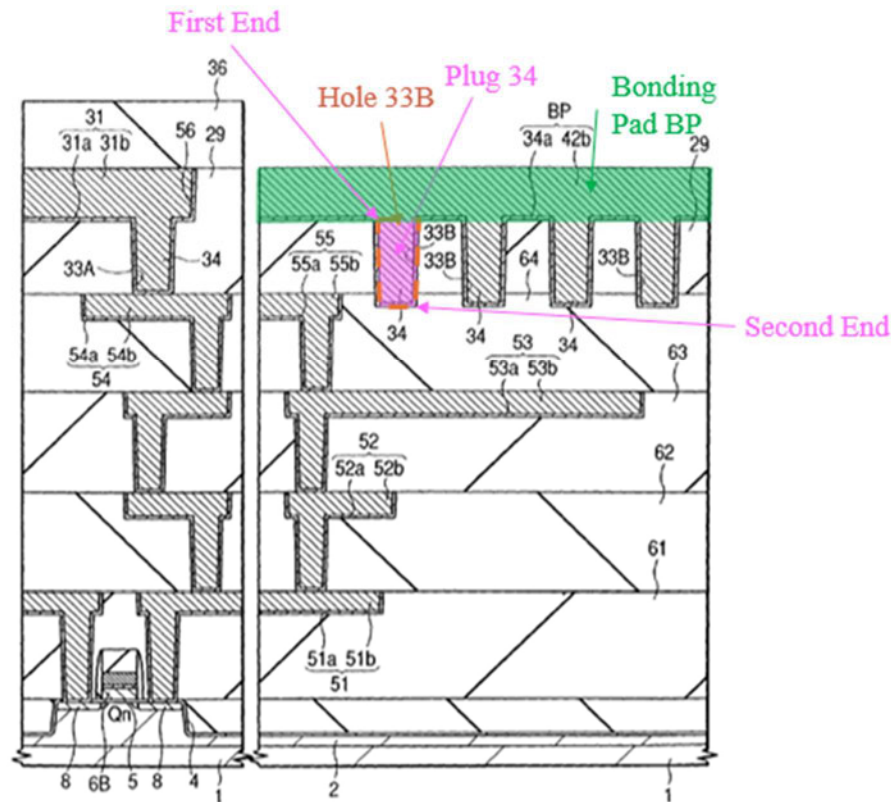


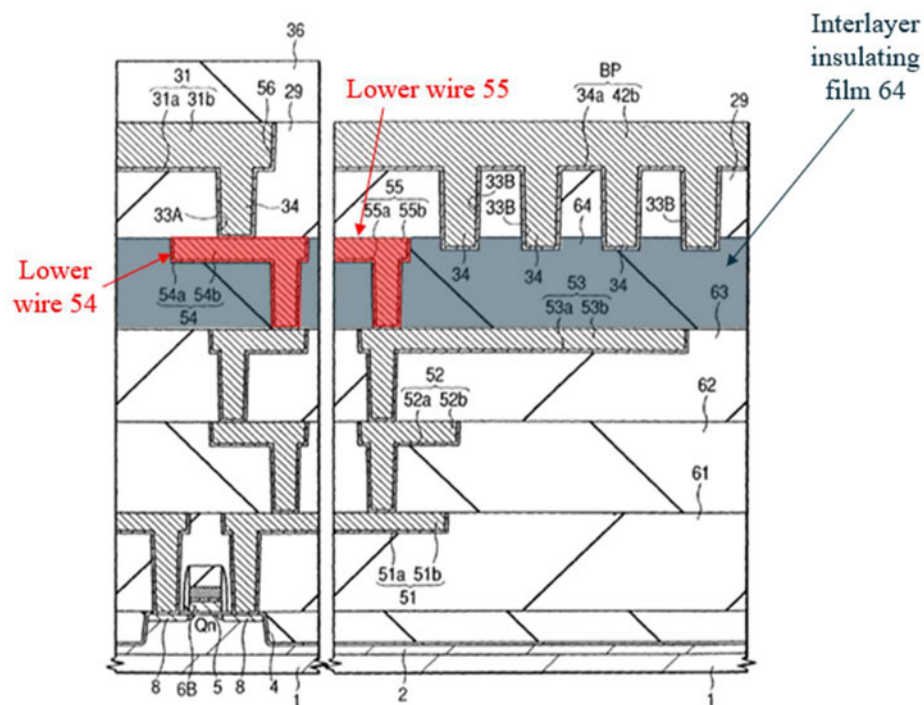
FIG. 19



387. A POSITA would further understand the respective, common cross-hatching shown in each layer of the device of Aoyagi's Figure 19 to indicate that each wiring layer and its corresponding vias are formed by a dual damascene process. Indeed, the common cross-hatching denotes to a POSITA that a same conductive material was applied in a single process (i.e., the dual damascene process) to form the corresponding wiring including both the interconnect and the underlying vias connected to the interconnect. Thus, a POSITA would have understood that when implementing Aoyagi's dual damascene process, each wiring

layer is formed within a respective insulating layer as disclosed generally below for lower wires 54/55 and their underlying vias:

FIG. 19



388. Accordingly, when wire 35 of Figure 4 is formed by dual damascene just as lower wires 54/55 are in Figure 19 (which as discussed above is disclosed by Aoyagi and also obvious), wire 35 will reside in an insulating film separate from insulating film 29 (in which interconnect 32/bonding pad BP and holes 33C are formed), similar to how lower wiring layers 51-54 of Figure 19 reside in respective interlayer insulating films 61-64, respectively. Subsequently, the over-etching of through-holes 33C results in holes 33B extending below an upper surface of wire 35 and into “the second insulating film” in which wire 35 is formed during the dual

damascene process. *See* TSMC-1006, ¶[0062] (“The diameter of the through-hole 33A is made substantially equal to that of the hole 33B, under which etching conditions can be made uniform. Overetching is performed in order to completely remove the interlayer insulating film 29 from the bottom (at the upper portion of the wire 27) of the through-hole 33A, so that the interlayer insulating film 29 at the bottom of the hole 33B, below which no wire is formed, is excessively etched, resulting in the depth of the hole 33B larger than that of the through-hole 33A.”).

389. As demonstrated in Figure 19 above, when implementing dual damascene manufacturing (including for the structure in Aoyagi’s Figure 4), the second end of Aoyagi’s dummy via (“plug 34” in “hole 33B”) would be surrounded by a second insulating film (e.g., similar to “interlayer insulating film 64”). *See* TSMC-1006, ¶¶[0048], [0055]-[0056], [0060]-[0061], Fig. 19. As demonstrated by Figure 19, that second insulating film similar to interlayer insulating film 64” would be different from the insulating film above it in which the bonding pad BP and upper portions of the dummy vias would be formed.

390. Thus, given Aoyagi’s discussion of dual damascene processing to form wire 31/bonding pad BP and form plugs 34 in holes 33A and 33B, it was obvious to use the dual damascene process to form bonding pad BP along with the dummy vias formed in holes 33B in the structure of Figures 3-4 as discussed above, and a POSITA would have expected success in doing so. *Supra*, §§IX(C), X(H)(1). Doing

so would result in dummy vias having lower ends that are surrounded by a second, lower layer insulating film (e.g., similar to interlayer insulating film 64) in a similar manner as in Figure 19, thus satisfying claim 19.

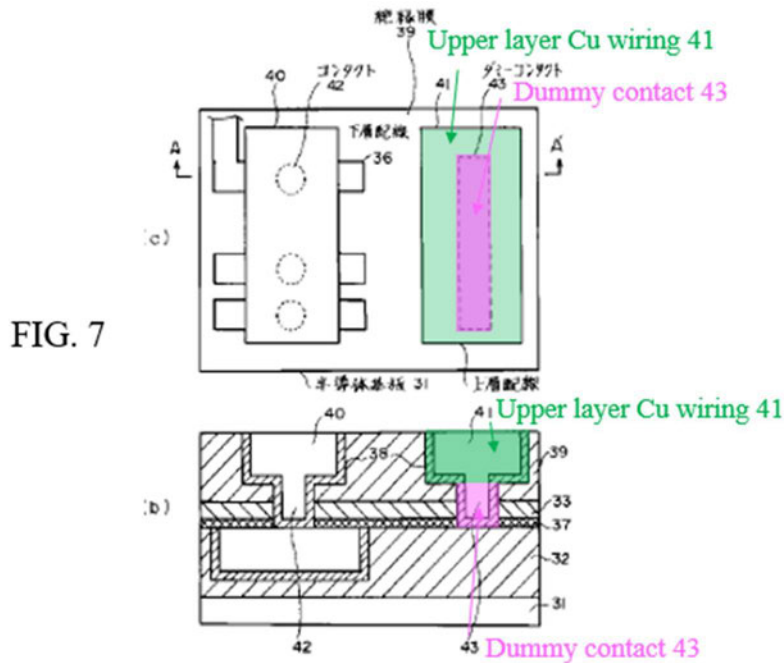
I. Ground 9: Aoyagi combined with Fukazawa renders Claim 17 unpatentable

391. I believe claim 17 is obvious over Aoyagi and Fukazawa as discussed below.

1. Claim 17

[17a] The method of claim 15, wherein the dummy via is substantially rectangular in a plan view, and

392. As discussed *supra*, §X(C)(1), Fukazawa discloses a dummy via (e.g., “dummy contact 43”) having a substantially rectangular shape (described as “column-shaped”) in a plan view (*see id.*, ¶¶[0017]-[0018] (“the dummy contacts are column-shaped”), Fig. 7). This rectangular shaped via is shown below in annotated Figure 7 of Fukazawa:



[17b] a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction.

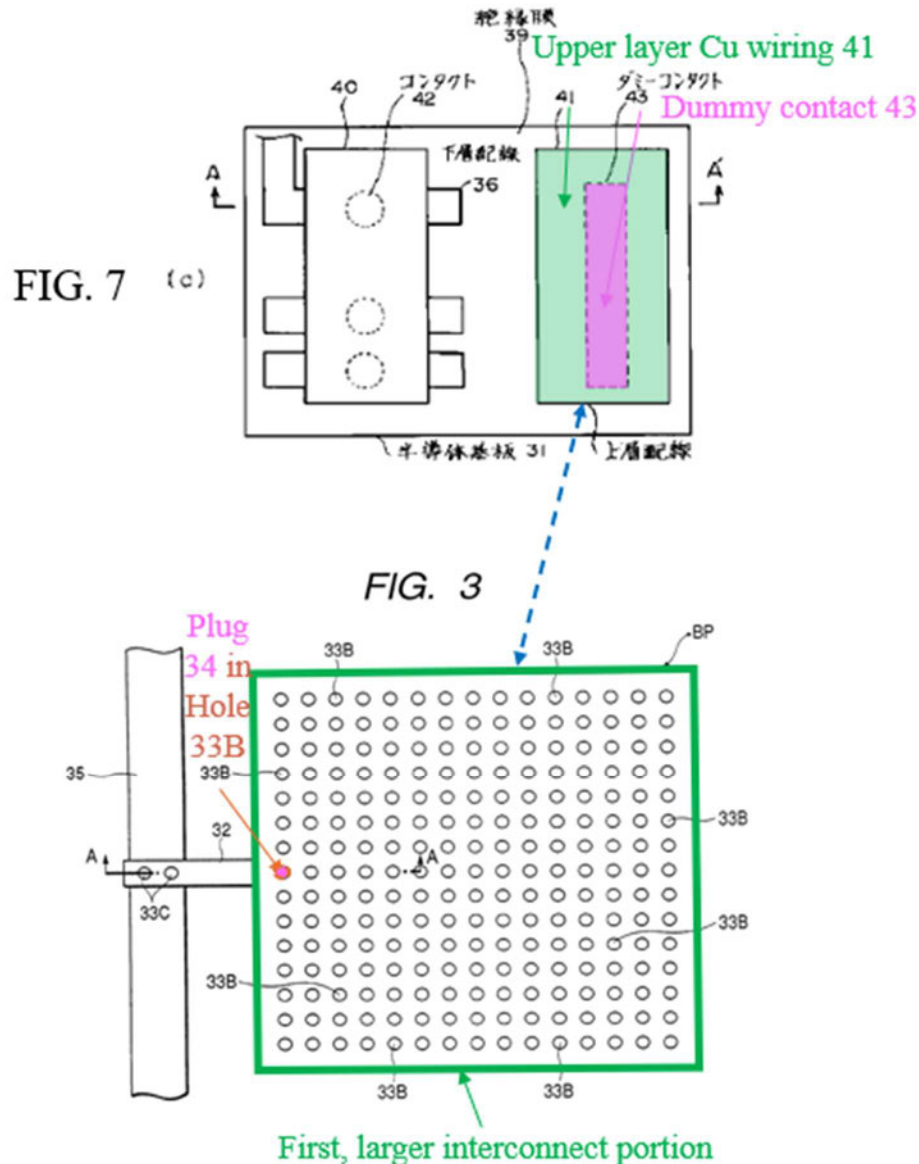
393. As discussed *supra*, §X(C)(1), and as disclosed in Fukazawa’s Figure 7 as annotated below, a longer side of its dummy contact/via 43 is provided along a same direction as a longer side of a correspondingly rectangular interconnect (“upper layer Cu wiring 41”) (TSMC-1010, ¶¶[0017]-[0018], Figure 7):



Obviousness of Combining Aoyagi and Fukazawa

394. A POSITA would have found it obvious to make the wider first interconnect portion of Aoyagi's bonding pad BP into a rectangular shape similar to the shape of wirings 40/41 of Fukazawa and further obvious to incorporate a rectangularly-shaped dummy via similar to Fukazawa's dummy contact 43 in place of one or more of Aoyagi's circular dummy vias in holes 33B in the very orientation taught in Fukazawa (i.e., such that a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction). This

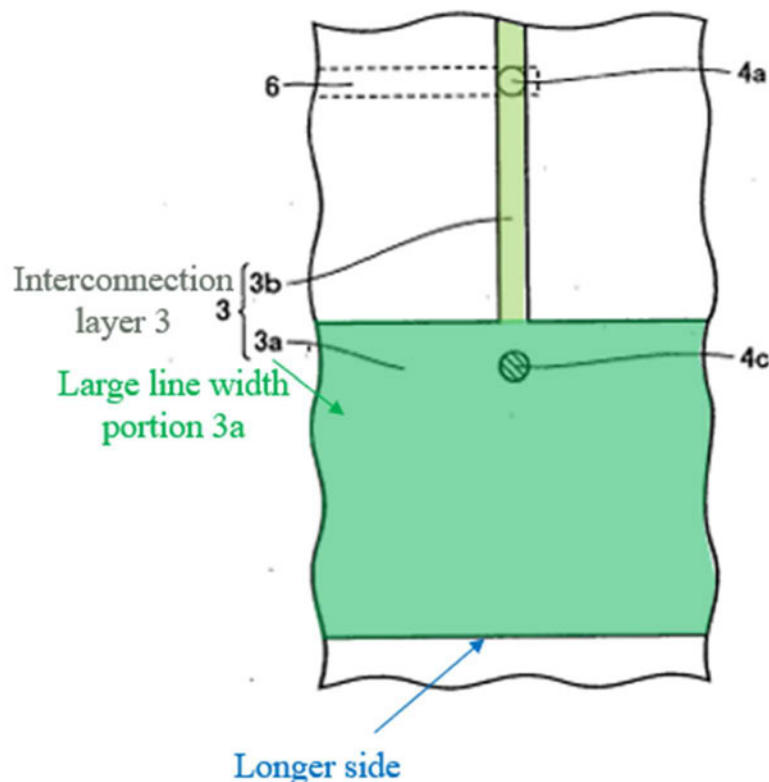
modification is represented below in the combination of annotated Figure 7 from Fukazawa and annotated Figure 3 from Aoyagi:



395. As shown the annotated combination of figures above, Fukazawa discloses the common rectangular shape of interconnects such that they have “longer” sides. *See also*, TSMC-1035, 1:26-28 (“Typical bonding pads in the prior art have...a rectangular or square configuration”). A POSITA would have

recognized prior the '751 patent, that merely changing the shape of the wider portion of bonding pad BP to a more rectangular shape having a longer side perpendicular to the narrower portion/lead wire 32 was thus an apparent option/shape choice that would have been selected for use whenever appropriate. A POSITA would have used such a rectangular shape wherever that shape was amenable to the circuit design, space constraints and desired surface area for bonding pad BP according to the requirements of the specific device being designed. Kamoshima further illustrates this point, demonstrating the well-known understanding to a POSITA at the time that such a rectangular shape was a known and suitable design option for a wide portion of a branched interconnect (see TSMC-1009, Figs. 23-26):

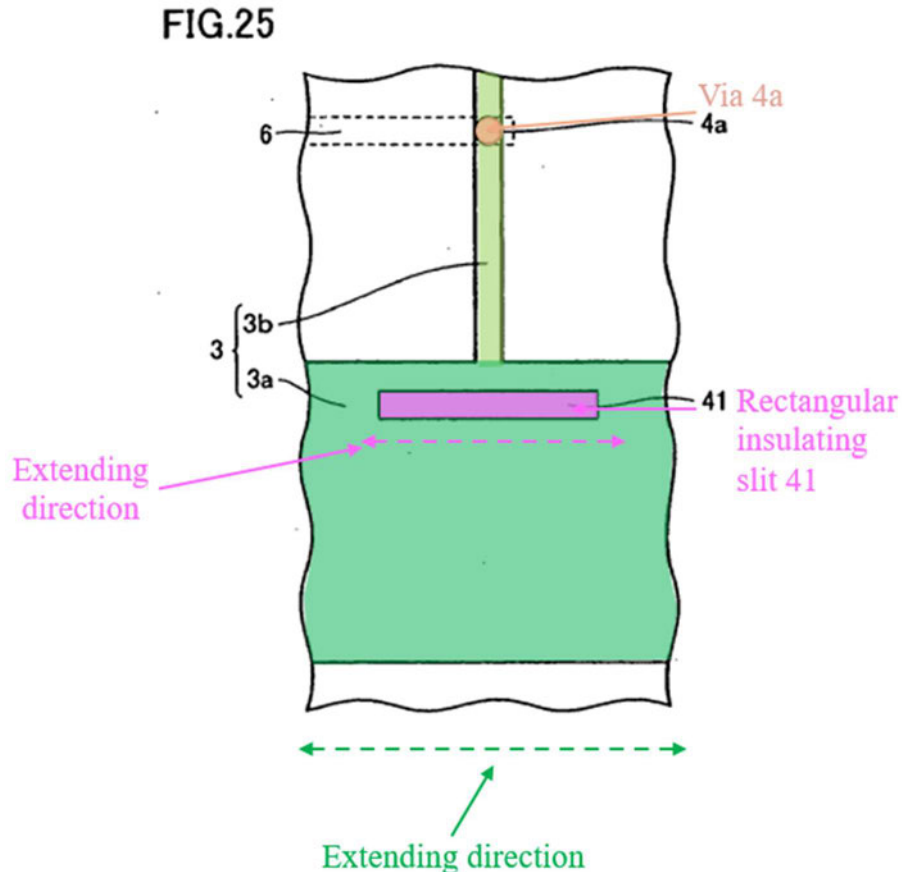
FIG.24



396. A POSITA was further motivated to use a rectangularly-shaped via with such a branched interconnect in order to accrue the known associated benefit of the increased mechanical strength afforded to the overall structure by such rectangularly-shaped vias. Indeed, Fukazawa expressly notes this benefit. TSMC-1010, ¶¶[0017]-[0018] (“the dummy contacts are column-shaped like the contacts, but the dummy contacts are not connected to the lower layer wiring or the semiconductor substrate.... [T]he contacts are column-shaped, and the column-shaped bodies are plate-shaped bodies that are connected continuously. Because of this structure, sufficient mechanical strength is ensured even when the insulating film comes off, thereby improving the strength of the wiring structure”). A POSITA understood that a rectangular via as taught in Fukazawa increases the strength of the structure as compared to the use of other shaped vias due to the increased interface surface area between the via, interconnect, and surrounding insulating films. The larger interface, particular in the longitudinal direction (given the increased area available for the interface and thus larger interface area) of the rectangle strengthens the structure relative to the use of circular or square vias.

397. Additionally, a POSITA would have been motivated to use the rectangular shape and to position it along a longer side of the wider portion of the branched interconnect to further reduce the migration of vacancies to (and thus the formation of voids within) a via arranged perpendicular to the narrow branch of the

interconnect. Indeed, Kamoshima similarly uses a rectangular structure (e.g., insulating slit 41) positioned in such a manner (a longer side extending in a same direction as a longer side of the wider interconnect portion) to suppress migration of vacancies to via 4a (*supra*, §X(C)):



398. A POSITA understood that positioning a rectangular dummy via in the same position as insulating film 41 would have suppressed vacancy migration (similar to dummy vias 4c in Kamoshima's Figure 23-24 embodiments), with the added benefit of providing a larger area of vacancy interception due to the rectangular shape and its position along a length of the wider portion of the

interconnect (and thus perpendicular to the narrow branch portion). *See also supra*, §X(C).

399. Both Aoyagi and Fukazawa are directed to interconnect and via designs for semiconductor devices. It would have been nothing more than a simple substitution to adopt Fukazawa's specific rectangular via/dummy via sizes and rectangularly shaped wide interconnect portion relative to the interconnect (bonding pad BP) and dummy vias in Aoyagi's device. For example, choosing specific shapes (e.g., rectangular) and placement (dummy via location relative to the long side of a wide interconnect portion) would be routine design choices to meet particular layout or process requirements within Aoyagi's device framework.

400. Furthermore, it would have been obvious to a POSITA to combine specific advantageous embodiments or features from one known approach (Fukazawa) into another (Aoyagi) if it led to an improved or more optimized overall design. The underlying physics of stress-induced vacancy migration and mechanical reinforcement in both Aoyagi's and Fukazawa's devices are similar or the same, such that a POSITA would have appreciated that dummy via placement and relative interconnect shape/layout helps with both mitigation stress-induced migration issues and mechanical stability for the interconnect structure and device as a whole. Accordingly, it would have been routine optimization for a POSITA to determine the beneficial shape (e.g., rectangle) and relative sizes (e.g., rectangular/longer side

dimensions) of the dummy vias and interconnects, as well as dummy via placement relative to the second interconnect.

401. Moreover, a POSITA, starting with Aoyagi's semiconductor device (which already includes dual-damascene-formed dummy vias), would have been motivated to incorporate the specific structural and dimensional details taught by Aoyagi for design optimization and flexibility.

402. A POSITA would have found such a modification to have had a reasonable expectation of success. Indeed, as described above, a POSITA would have been easily capable of substituting a rectangular via for the circular dummy vias of Aoyagi and extending a length of bonding pad BP to accommodate a rectangular via (or otherwise extend bonding pad BP along its length), which could have been reliably achieved using standard patterning techniques at the time. Indeed, other contemporary references at the time demonstrate that rectangular vias were known and used and positioning them where desired was easily achieved. *Supra*, §X(C). Contemporaneous references demonstrate that rectangular vias were known and used and that positioning them where desired was easily achieved. *Supra*, §X(C).

XI. CONCLUSION

403. As discussed above, it is my opinion that the Challenged Claims of the '751 patent are unpatentable because they are anticipated by the prior art, because

they would have been obvious to a person of ordinary skill in view of the prior art, or both.

404. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

405. I reserve the right to supplement my opinions in the future to respond to any arguments raised by the Patent Owner or the Patent Trial and Appeal Board, and to account for new information as it becomes available to me.

406. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Declaration of Dr. Reinhold Dauskardt

Executed on this 15th day of July, 2025, in Sunnyvale CA.

By:

A handwritten signature in black ink, appearing to read 'Reinhold H. Dauskardt', with a large, stylized flourish at the end.

Dr. Reinhold H. Dauskardt

Appendix A

Exhibit No.	Description
1001	U.S. Patent No. 7,632,751
1002	File History of U.S. Patent No. 7,632,751 (“751 File History”)
1003	Declaration of Dr. Reinhold Dauskardt
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. (“Watanabe”)
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. (“Hasunuma”)
1006	U.S. Patent Publication No. 2001/0019180 to Aoyagi et al. (“Aoyagi”)
1007	U.S. Patent No. 6,717,267 to Kunikiyo (“Kunikiyo”)
1008	U.S. Patent No. 5,250,465 to Iizuka et al. (“Iizuka”)
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. (“Kamoshima”)
1010	JP2002299437 (“Fukazawa”) and Certified Translation of Fukazawa with Certification of Translation
1011	U.S. Patent No. 7,042,099 to Kurashima (“Kurashima”)
1012	P. Andricacos, “Copper On-Chip Interconnections,” <i>Interface, The Electrochemical Society</i> , pp. 32-37, 1999
1013	U.S. Patent No. 5,885,857 to Yamaha et al. (“Yamaha”)
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi (“Igarashi”)

1015	U.S. Patent No. 6,717,268 to Hau-Riege (“Hau-Riege”)
1016	U.S. Patent No. 6,468,894 to Yang (“Yang”)
1017	U.S. Patent No. 6,022,808 to Nogami (“Nogami”)
1018	Reserved
1019	Kaanta et al., “Dual Damascene: A ULSI Wiring Technology,” <i>VMIC Conference</i> , IEEE, Jun. 11-12, 1991, pp. 144-152
1020	U.S. Patent No. 5,032,890 to Ushiku (“Ushiku”)
1021	Reserved
1022	U.S. Patent No. 6,582,976 to Watanabe (“Watanabe’976”)
1023	S. Middleman et al., <i>Process Engineering Analysis in Semiconductor Device Fabrication</i> , pp. 260-61 (excerpted), McGraw-Hill, 1993 (“Middleman”)
1024	U.S. Patent No. 6,156,660 to Liu et al. (“Liu”)
1025	U.S. Patent No. 5,798,298 to Yang (“Yang 2”)
1026	T. I. Bao et al., “90 nm Generation Cu/CVD Low-k ($k < 2.5$) Interconnect Technology,” <i>Digest. International Electron Devices Meeting</i> , San Francisco, CA, USA, 2002, pp. 583-586
1027	A. Loke, “Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects, Dissertation,” Stanford University (1999)
1028	K.N. Tu, “Recent advances on electromigration in very-large-scale-integration of interconnects,” <i>Applied Physics Review – Focused Review, Journal of Applied Physics</i> , Vol. 94, No. 9, pp. 5451-5473 (November 1, 2003)

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1039	U.S. Patent No. 6,238,850 to Bula et al. (“Bula”)

Appendix B

Claim Element	Claim Language
1[pre]	A method for fabricating a semiconductor device comprising the steps of:
1[a]	(a) forming a first interconnect on a semiconductor substrate;
1[b]	(b) forming a first insulating film on the first interconnect;
1[c]	(c) forming in the first insulating film, a via hole connected to the first interconnect, a dummy hole which is arranged so as to be incapable of having current flow therethrough, and an interconnect trench connected to the via hole and the dummy hole; and
1[d]	(d) depositing a conductive material in the via hole, the dummy hole and the interconnect trench, thereby forming a via, a dummy via and a second interconnect.
2[a]	The method of claim 1, wherein in the step (a) a first dummy interconnect is simultaneously formed on the semiconductor substrate, and
2[b]	in the step (c) the dummy hole is connected to the first dummy interconnect.
3[a]	The method of claim 1, wherein in the step (c) the interconnect trench is comprised of a first interconnect trench portion and a second interconnect trench portion whose width is smaller

	than that of the first interconnect trench portion and which branches from the first interconnect trench portion, and
3[b]	the via hole and the dummy hole are connected to the interconnect trench.
4	The method of claim 3, wherein in the step (c) the dummy hole is connected to the branch point between the first and second interconnect trench portions or to the interconnect trench near the branch point.
5	The method of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO ₂ film.
6	The method of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode.
7	The method of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect.
8	The method of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect.

9	The method of claim 1, wherein the via and the dummy via are substantially circular in a plan view.
10	The method of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square.
11	The method of claim 1, wherein the first interconnect and the second interconnect extend in a same direction.
12	The method of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends.
13	The method of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less.
14	The method of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via.
15[a]	The method of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and

15[b]	the via is connected to the second interconnect portion.
16	The method of claim 15, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions.
17[a]	The method of claim 15, wherein the dummy via is substantially rectangular in a plan view, and
17[b]	a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction.
18	The method of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film.
19	The method of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.
20	The method of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy

	interconnect, the first dummy interconnect being surrounded by a second insulating film.
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Appendix C

Reinhold H. Dauskardt, Ph.D.

email: dauskardt@stanford.edu

website: <http://dauskardt.stanford.edu>

Reinhold Dauskardt is the Ruth G. and William K. Bowes Professor in the Department of Materials Science and Engineering and has additional appointments as Professor in Mechanical Engineering, the Biodesign Institute and the Department of Surgery, Stanford School of Medicine. Dauskardt is a member of Stanford Bio-X, the Cardiovascular Institute, the Wu Tsai Human Performance Alliance, and the Wu Tsai Neurosciences Institute, and an affiliate of the Precourt Institute for Energy and the Stanford Woods Institute for the Environment. He is also a Visiting Professor in the School of Materials Science and Engineering at the Nanyang Technological University in Singapore.

The underlying theme of his research is to enable innovation and design of high-performance materials and devices by exploiting the fundamental connection between device materials, design, and processing and resulting device performance, function and reliability under use conditions.

Dauskardt and his group have worked extensively on integrating new nano and molecular materials into emerging technologies that include semiconductor, nanoscience and energy technologies, high-performance laminates, biomaterials and soft tissues.

He is an internationally recognized expert on the design and thermomechanical reliability of engineering structures, solar, battery and electronic device technologies for which he was awarded the prestigious Semiconductor Industry Association University Researcher Award in 2010 for “research which has provided substantive and sustained contributions to semiconductor industry science and technology.” The Dauskardt Lab has a unique combination of internationally recognized materials and device processing capabilities, scalable manufacturing, reliability physics, high resolution characterization, accelerated testing and modeling capabilities. These capabilities include advanced sol-gel processing and open-air spray plasma deposition of semiconductor, solar and battery materials, along with accelerated testing and reliability modeling. He is also well known for his studies of the effects of semiconductor device and packaging processing operations and processing environments (including plasma processing, chemical mechanical planarization (CMP), and a wide range of deposition techniques) on device structures and their properties. Experimental studies are complimented with a range of multi-scale mechanics and molecular computational modeling capabilities.

His research on soft tissues and wound healing has concentrated on establishing a biomechanics framework to understand and control the biological processes that determine the effects of treatments and exposures on barrier function and the biomechanics of human skin and other soft tissues for which he was awarded the Henry Maso Award for fundamental contributions to the advancement of cosmetic and skin science, and scar formation in healing cutaneous wounds. A major theme in his labs current research involves wearable device technologies. The interdisciplinary nature of his research is reflected in his appointments in the Stanford Biodesign Institute and in the Department of Surgery, Stanford School of Medicine.

His interdisciplinary research includes interaction with researchers in academia, industry, and clinical practice. He has served as an editor and reviewer for a number of journals and books including Nature, Science, Energy and Environmental Sciences, Nanoletters, Acta Materialia, the Journal of Applied Physics, PANS and the New England Journal of Medicine. He has co-organized international technical conferences and symposia in his areas of research. He has published over

400 articles in the scientific literature and holds more than 30 U.S. and International Patents. Dauskardt has contributed significantly to leadership in Stanford's multidisciplinary materials efforts which spans several departments, schools, and the SSRL.

Education: B.Sc. (1980) and M.Sc. (1983) Physics, Mathematics and Materials – U. Witwatersrand, South Africa, Ph.D. Materials Science and Eng. - U.C. Berkeley/ U. Witwatersrand (1988).

Recognition and Awards: 2016: Visiting Professor, Nanyang Technological University. 2013: appointed the Ruth G. and William K. Bowes Professor in the School of Engineering, Stanford University. 2011: H. Maso Award for fundamental contributions to skin science, Int. Fed. Soc. Cos. Chem.; IBM Shared University Research Award. 2010: Semiconductor Industry Assoc. Univ. Researcher Award for substantive contributions to semiconductor industry sci. & tech.; TMS Struct. Mat. Distinguished Scientist Award; Fellow ASM Int. 2008: Fellow Am. Ceram. Soc.; VLSI/ULSI Multilevel Interconnection Int. Conf. Award for “Optimized Curing and CMP of Nanostructured Ultra-low-k Films”; Am. Vac. Soc. Thin-Film User Group Special Award. 2006: Distinguished Speaker Award, Dept. MSE, Penn State; IBM Faculty Award, Yorktown Heights. 2003: ASM Int. Silver Medal. 2002: Alexander von Humboldt Research Award. 1989: U.S. DoE Outstanding Sci. Accomplishment Award.

Advisory Boards and Board of Directors: Advisory Board, National Inst. Materials Science, Tsukuba, Japan; Advisory Board, School of Mat. Sci. Eng. Nanyang Tech. U., Singapore; Advisory Board, Singapore Institute of Manufacturing Technology (SimTech), A-Star, Singapore; Co-founder, Neodyne Biosciences Inc. (medical devices), Palo Alto, CA.

Professional Activities: Dauskardt has been involved in a range of university academic and materials research leadership roles at Stanford. He is an established international leader in the broader materials and device technical and scientific communities where he has managed several large multidisciplinary research activities. He has served as organizer of a range of international conferences and symposia.

He serves as a consultant and technical advisor to a range of leading international technology companies, materials suppliers, and equipment vendors. He is well known for his work providing technical expert services in trial, by declaration, and/or deposition for litigation and regarding both validity and infringement analysis in US and International patent cases.

Doctoral Students and Post Doctoral Fellows: Dauskardt has supervised 66 doctoral students and 48 post-doctoral fellows, medical residents and medical fellows. He currently has 16 doctoral students, 2 masters student, and 2 post docs in his research group along with visiting professors and industry researchers.

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