US007439623B2

(12) **United States Patent**
**Harada**

(10) **Patent No.: US 7,439,623 B2**
(45) **Date of Patent: Oct. 21, 2008**

(54) **SEMICONDUCTOR DEVICE HAVING VIA CONNECTING BETWEEN INTERCONNECTS**

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(73) Assignee: **Matsushita Electric Industrial Co., Ltd.**, Osaka (JP)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 306 days.

(21) Appl. No.: **11/000,904**

(22) Filed: **Dec. 2, 2004**

(65) **Prior Publication Data**

US 2005/0121792 A1 Jun. 9, 2005

(30) **Foreign Application Priority Data**

Dec. 3, 2003 (JP) ..... 2003-404437

(51) **Int. Cl.**
***H01L 29/40*** (2006.01)

(52) **U.S. Cl.** ..... **257/758**; 257/750; 257/752; 257/758; 257/773; 257/774; 257/775; 257/776; 257/E23.145; 257/E29.119; 438/598; 438/601; 438/623

(58) **Field of Classification Search** ..... 257/750, 257/752, 758, 773, 774, 775, 776, E23.145, 257/E29.119

See application file for complete search history.

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*Primary Examiner*—Thanh V Pham
(74) *Attorney, Agent, or Firm*—McDermott Will & Emery LLP

(57) **ABSTRACT**

A first insulating film is provided between a lower interconnect and an upper interconnect. The lower interconnect and the upper interconnect are connected to each other by way of a via formed in the first insulating film. A dummy via or an insulating slit is formed on/in the upper interconnect near the via.

**48 Claims, 18 Drawing Sheets**

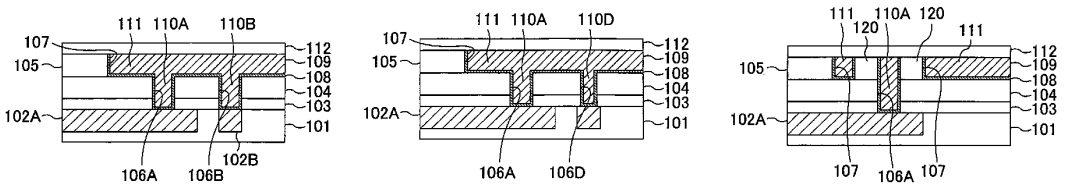


FIG. 1A

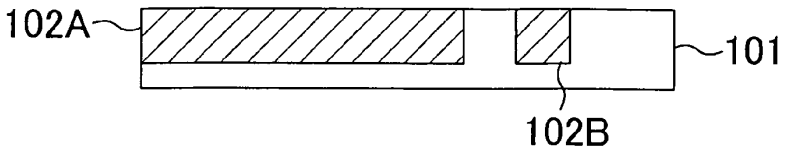



FIG. 1B

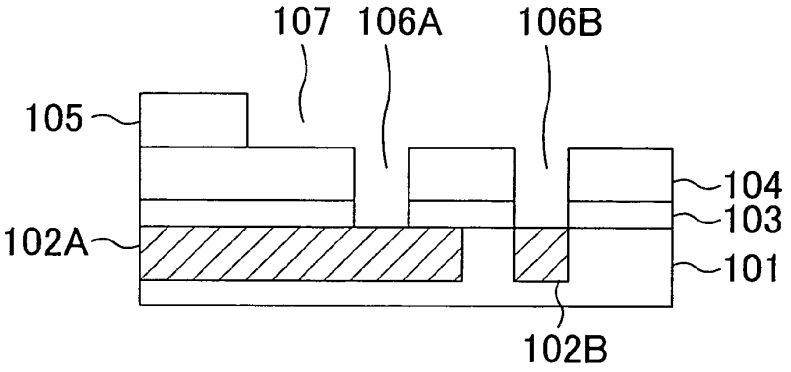



FIG. 1C

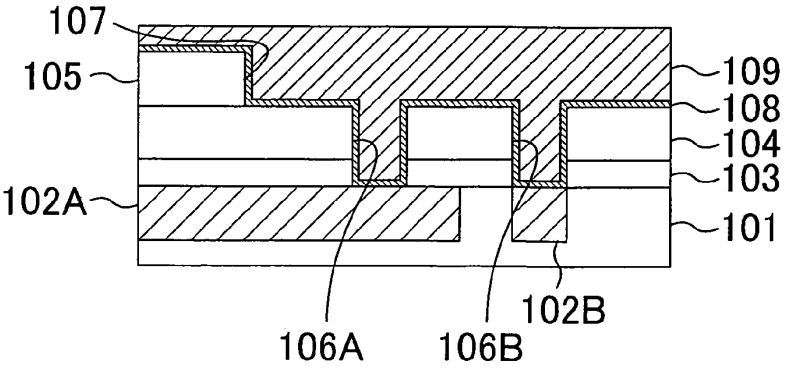


FIG. 2A

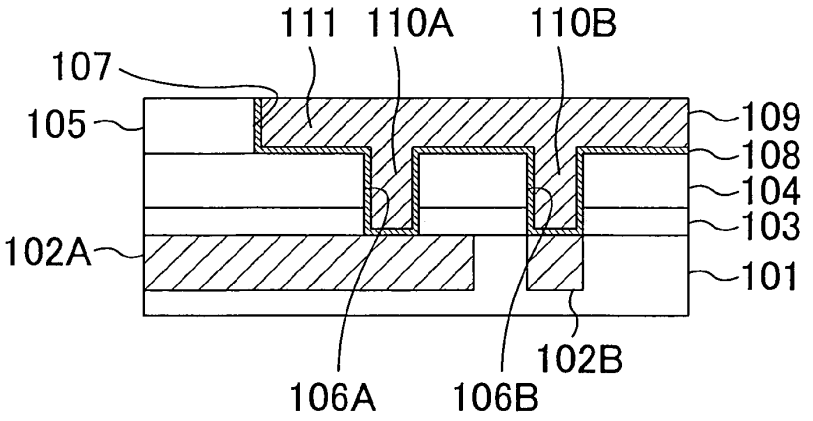



FIG. 2B

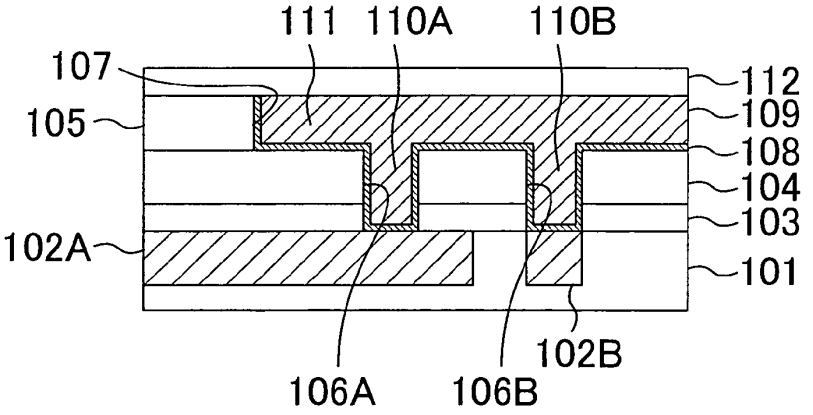



FIG. 2C

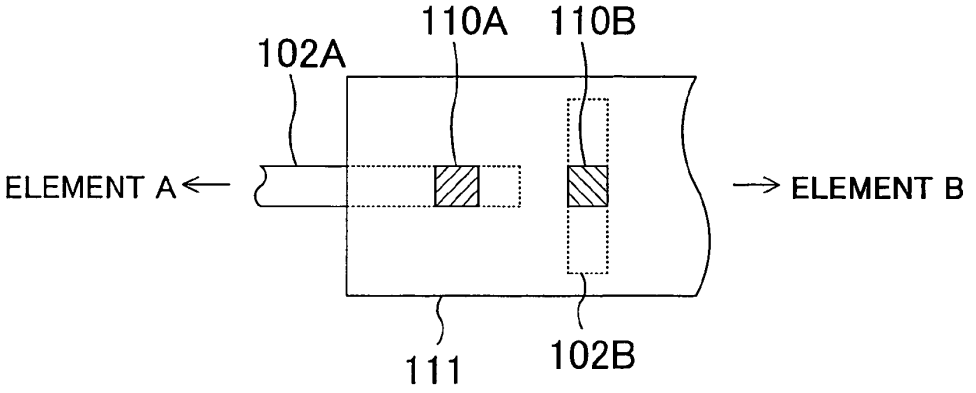


FIG. 3

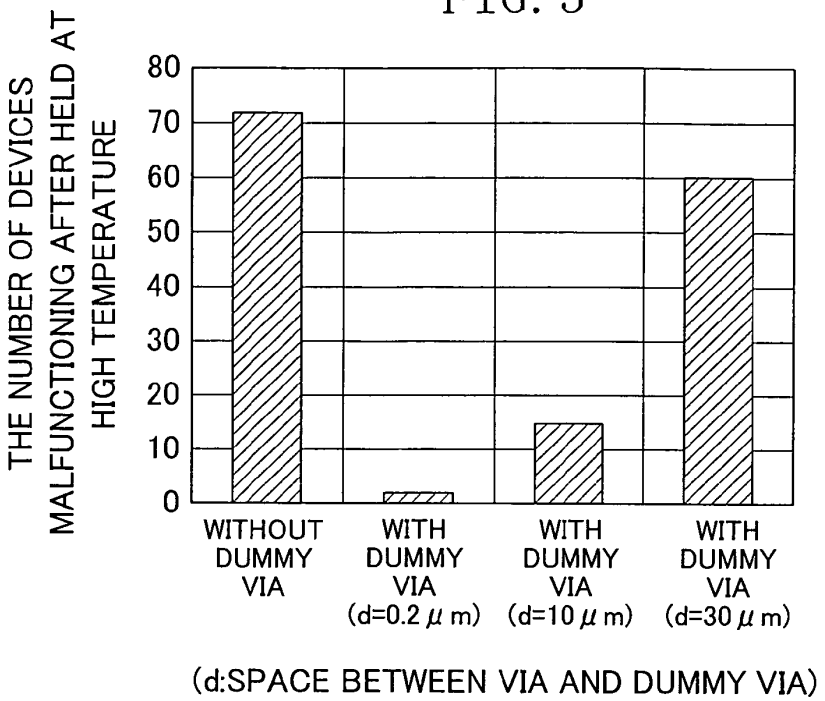

THE NUMBER OF DEVICES MALFUNCTIONING AFTER HELD AT HIGH TEMPERATURE
80
70
60
50
40
30
20
10
0
WITHOUT DUMMY VIA
WITH DUMMY VIA (d=0.2 μm)
WITH DUMMY VIA (d=10 μm)
WITH DUMMY VIA (d=30 μm)
(d:SPACE BETWEEN VIA AND DUMMY VIA)

FIG. 4

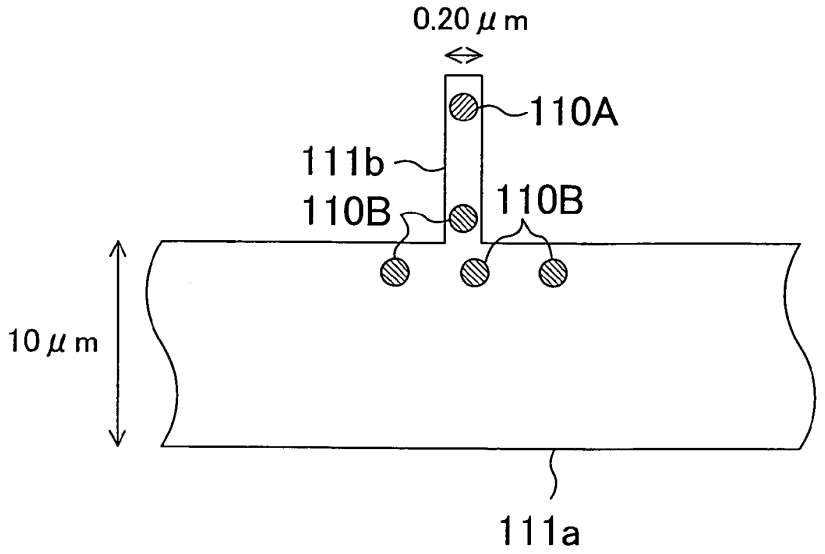
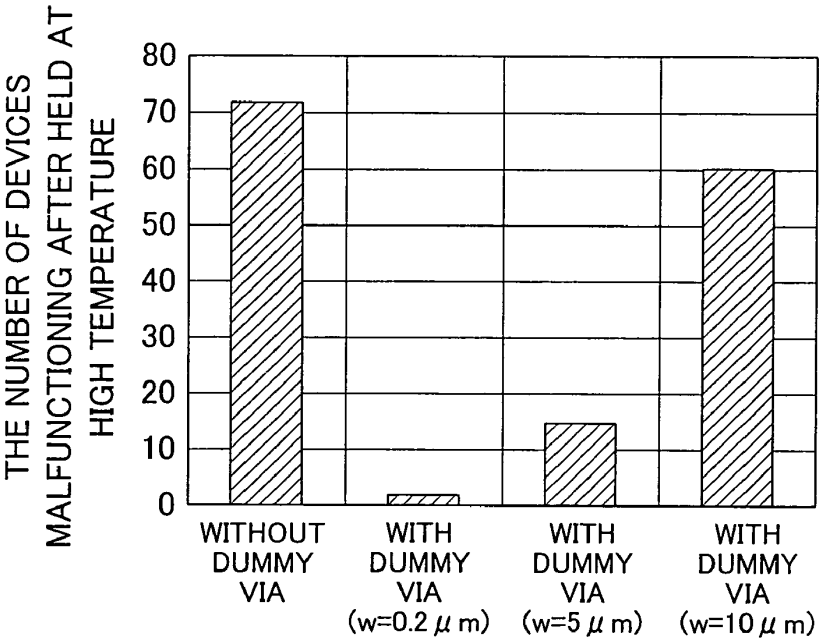

0.20 μm
110A
111b
110B
110B
10 μm
111a

FIG. 5




(w:WIDTH OF INTERCONNECT WHERE VIA IS FORMED)

FIG. 6A

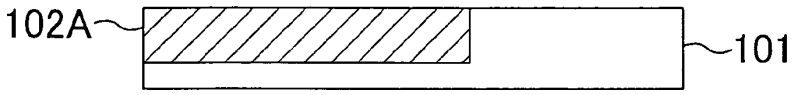



FIG. 6B

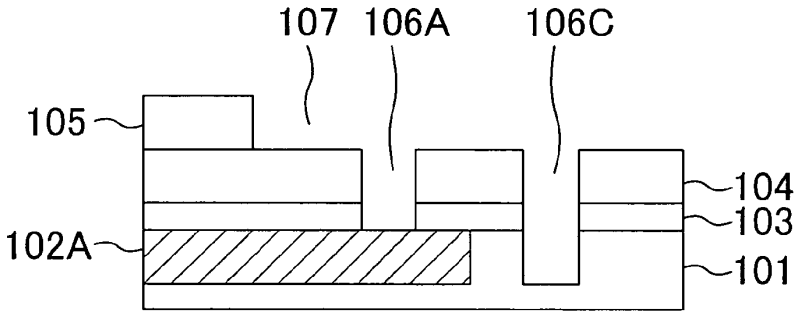



FIG. 6C

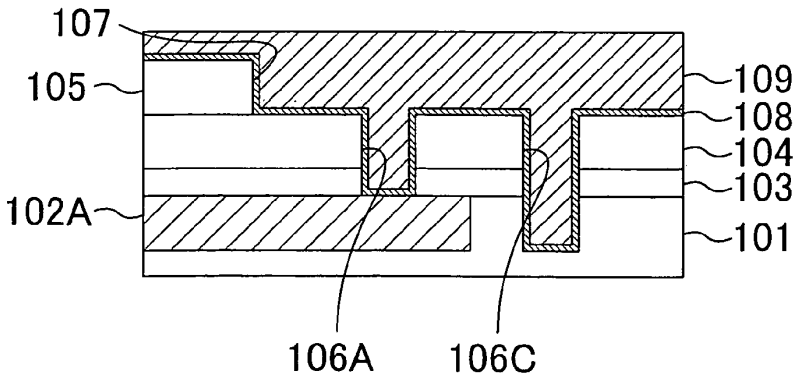


FIG. 7A

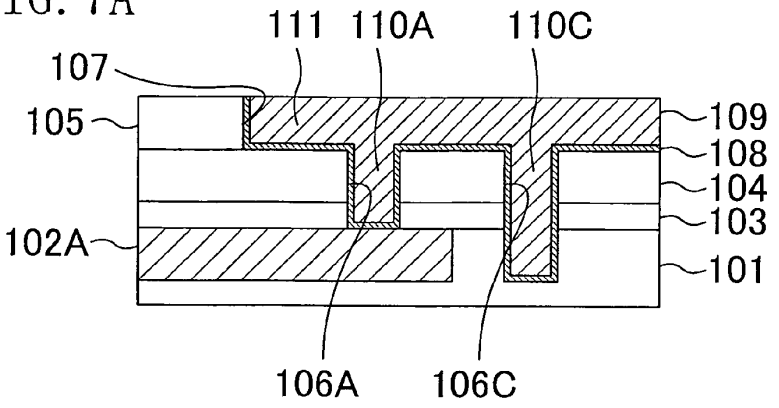



FIG. 7B

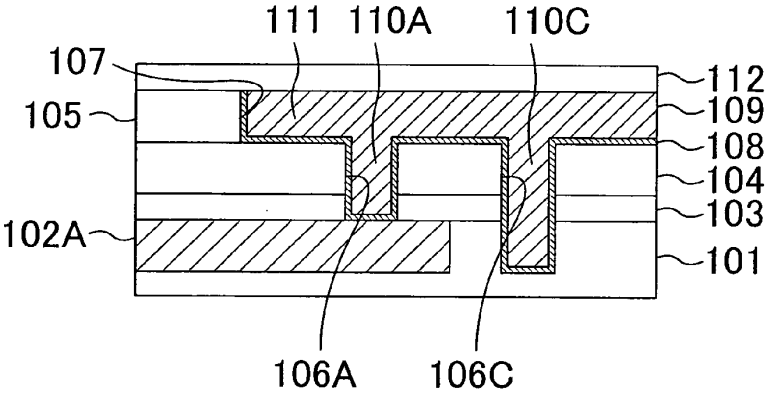



FIG. 7C

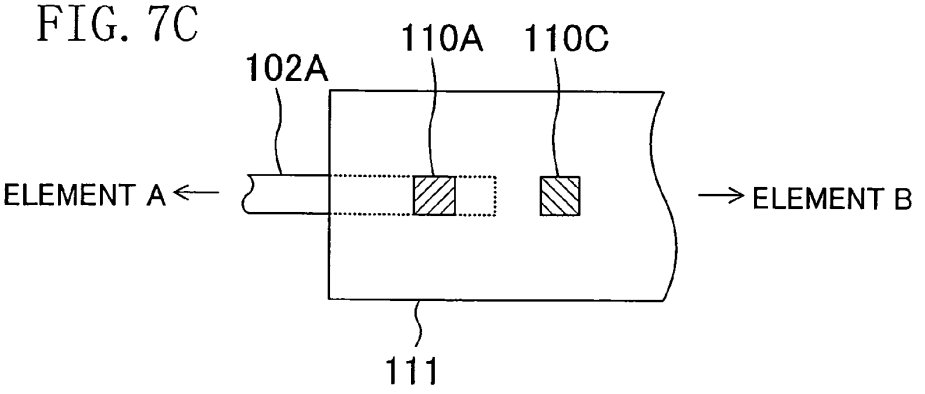


FIG. 8A

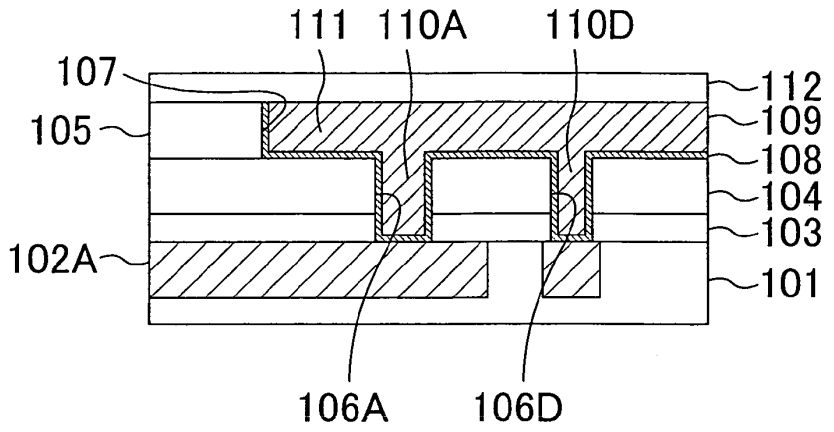

111
110A
110D
107
105
112
109
108
104
103
102A
101
106A
106D

FIG. 8B

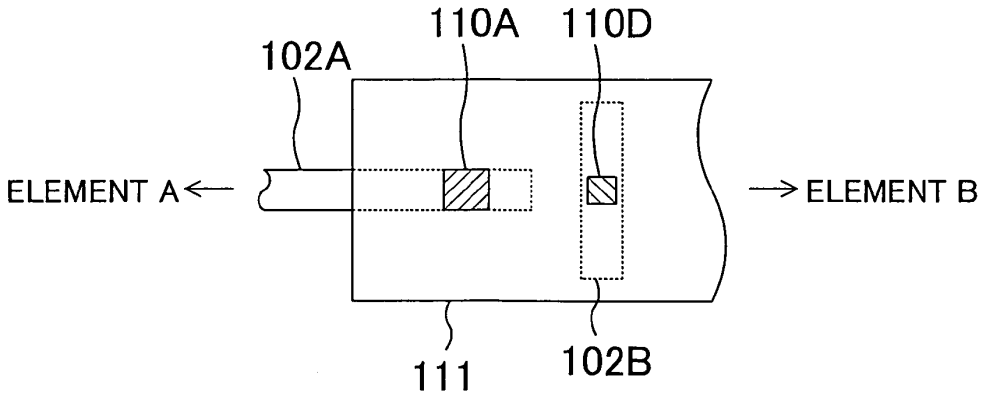

110A
110D
102A
ELEMENT A
ELEMENT B
111
102B

FIG. 9A

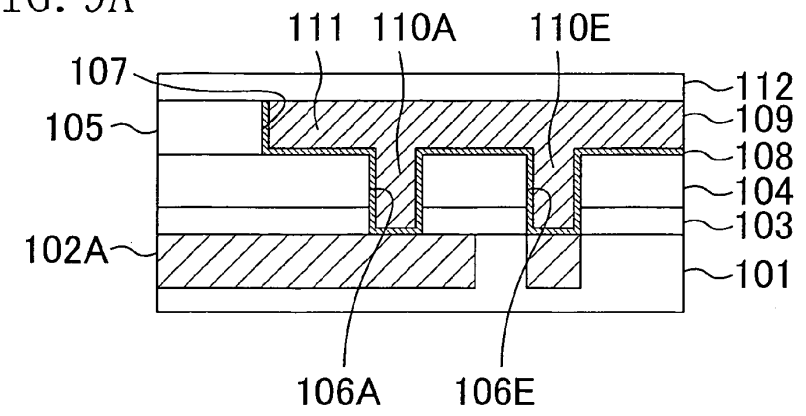



FIG. 9B

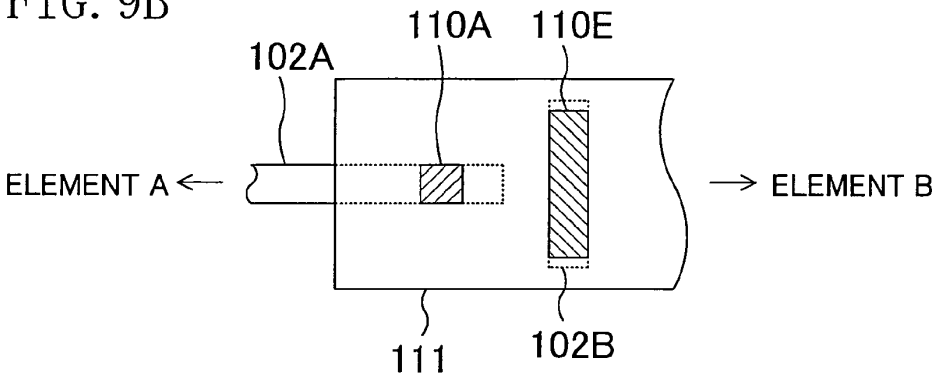



FIG. 10

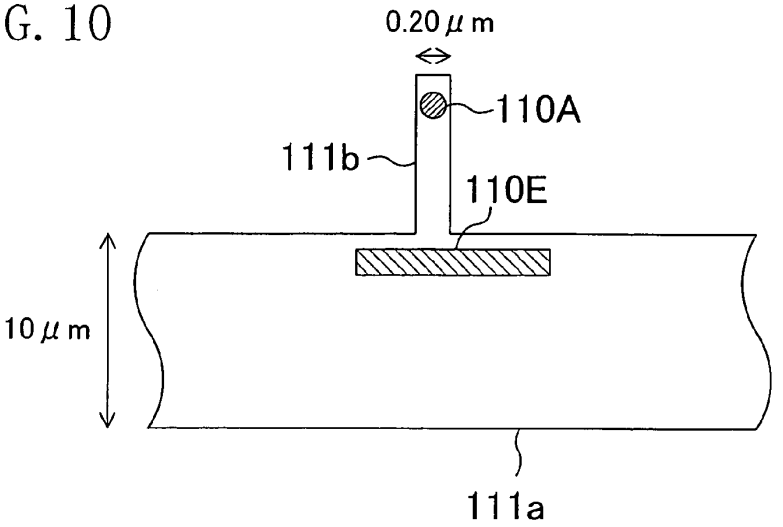


FIG. 11A

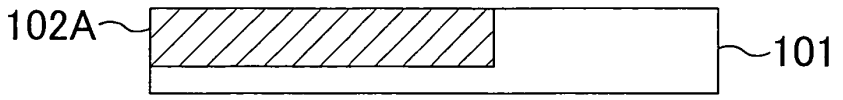



FIG. 11B

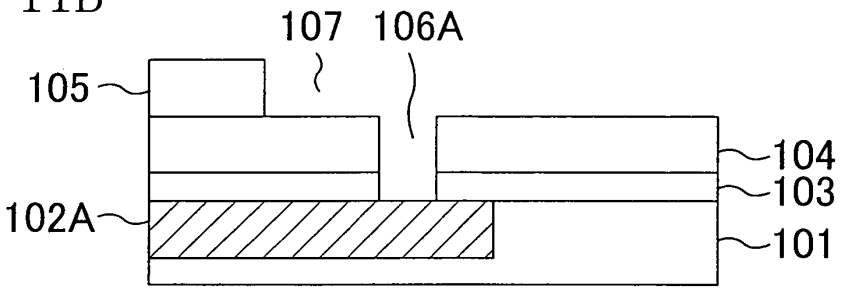



FIG. 11C

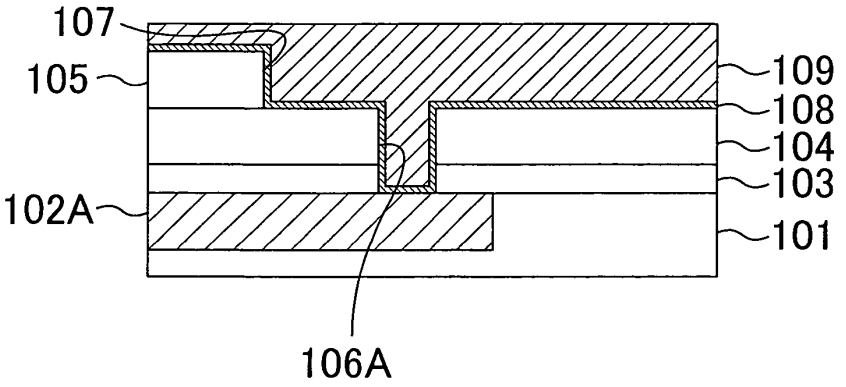


FIG. 12A

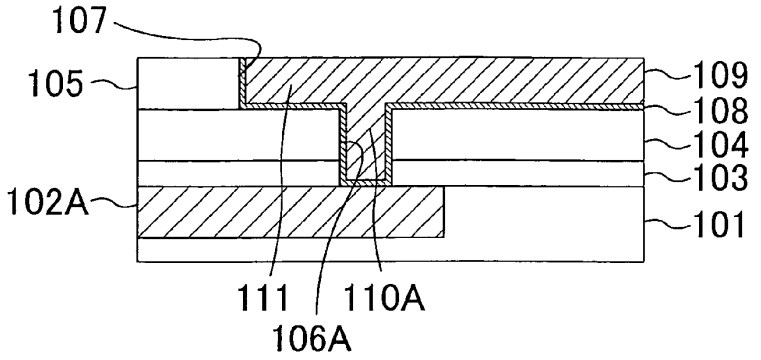



FIG. 12B

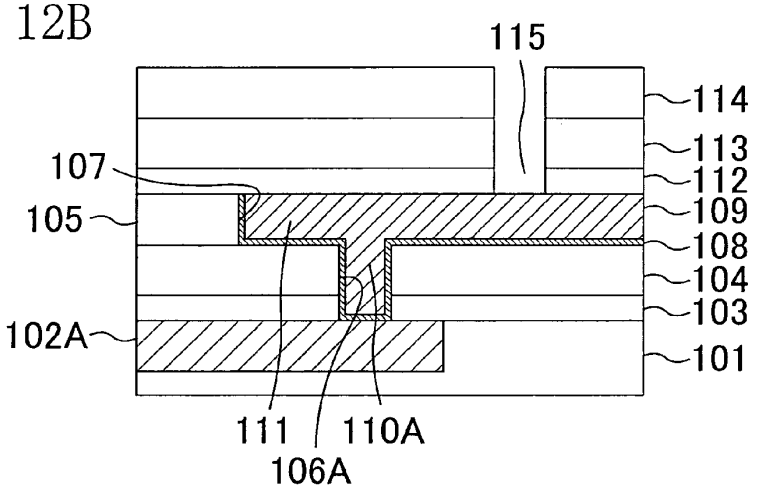



FIG. 12C

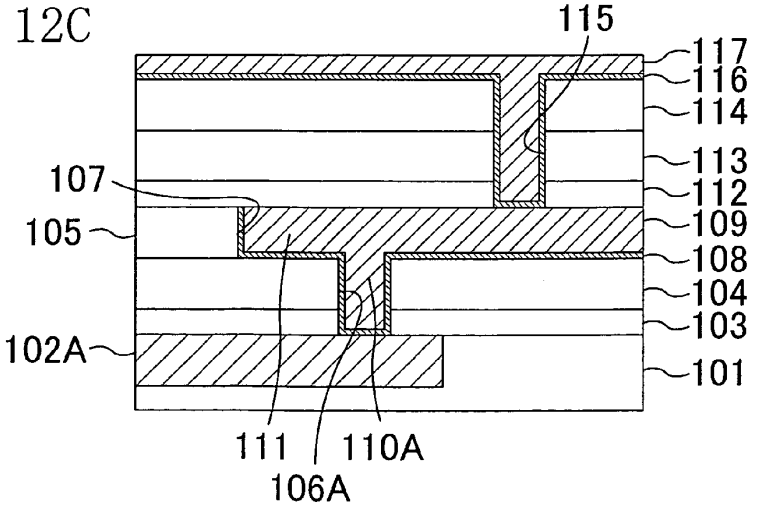


FIG. 13A

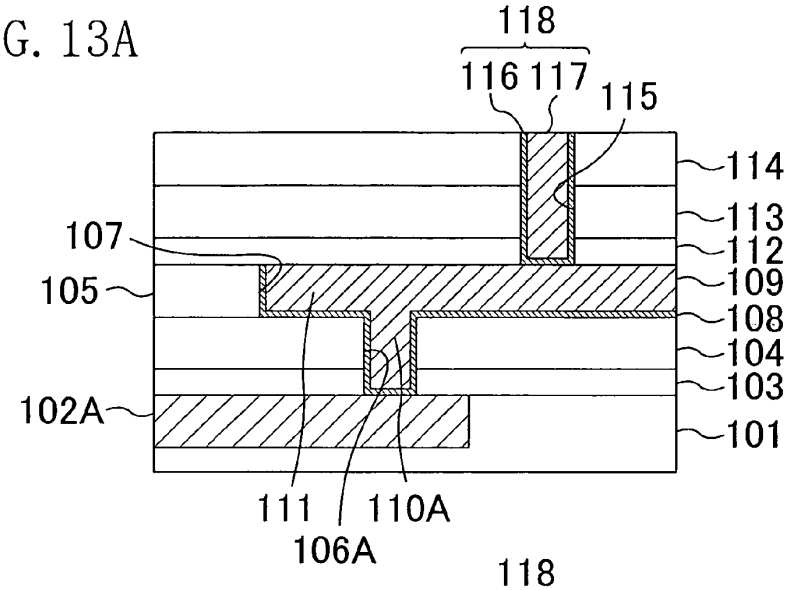



FIG. 13B

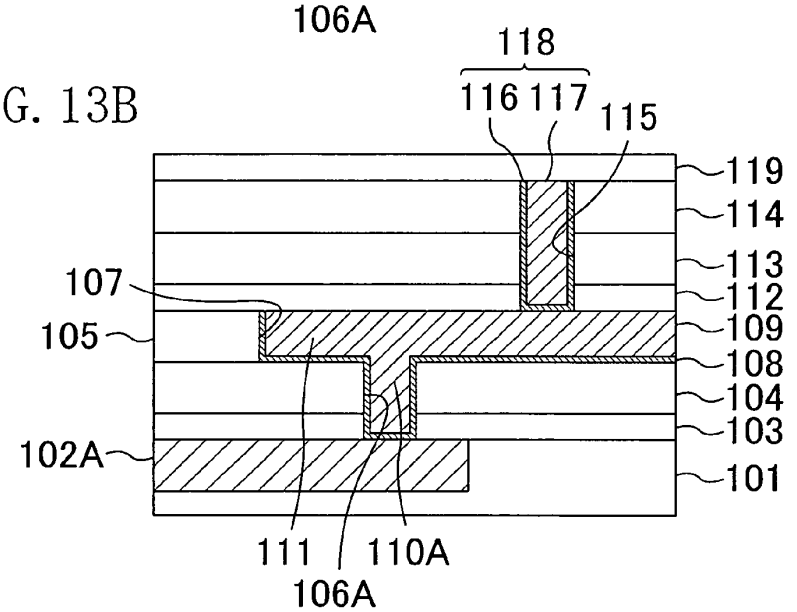



FIG. 13C

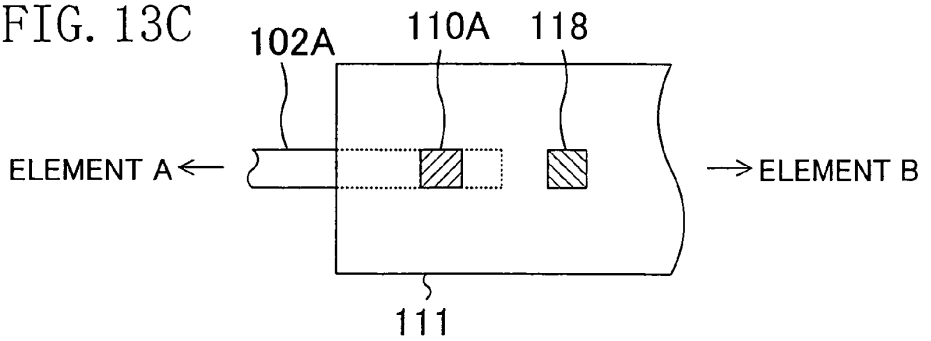


FIG. 14A

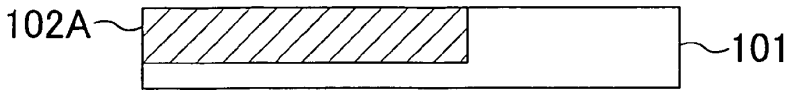



FIG. 14B

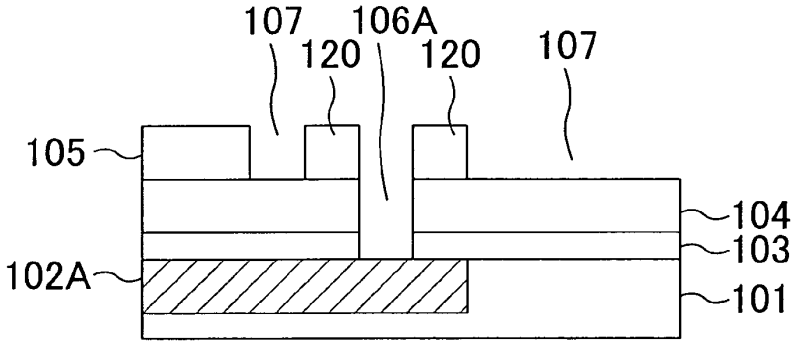



FIG. 14C

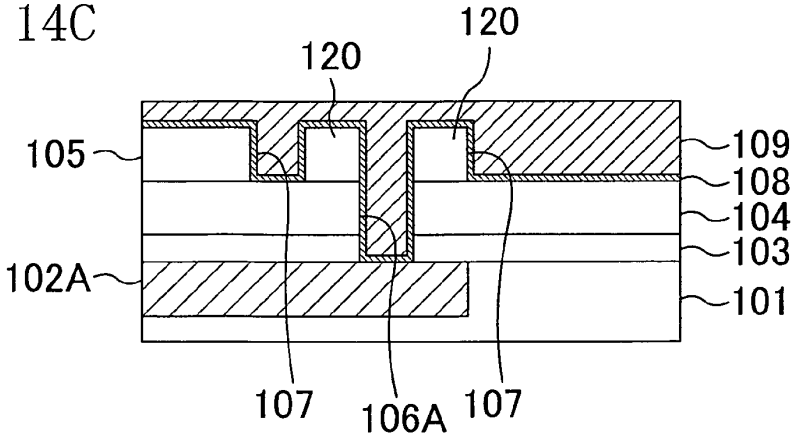


FIG. 15A

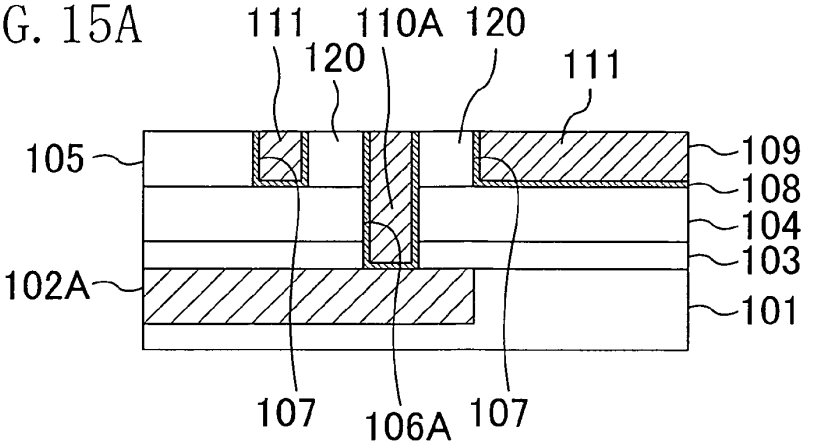



FIG. 15B

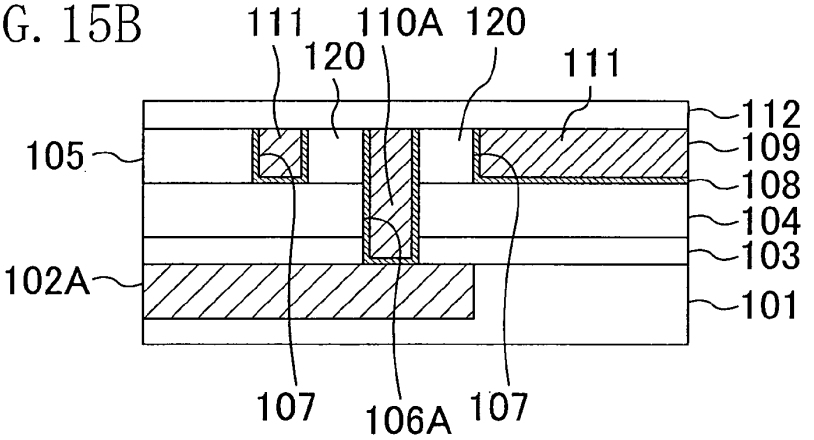



FIG. 15C

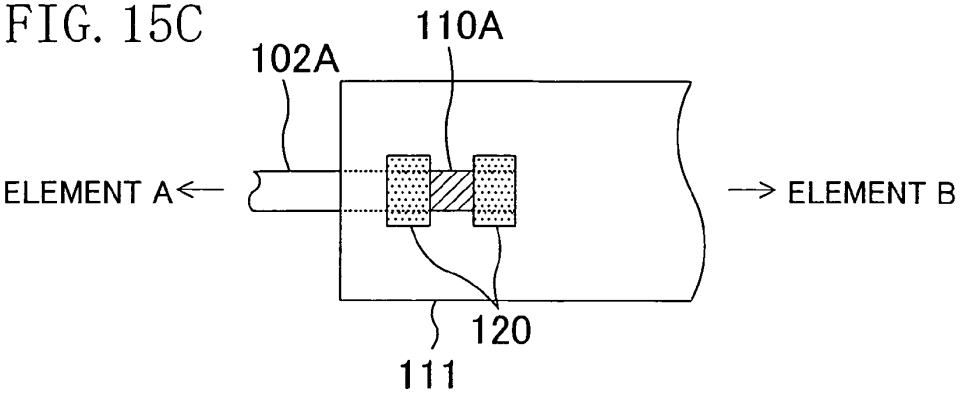


FIG. 16

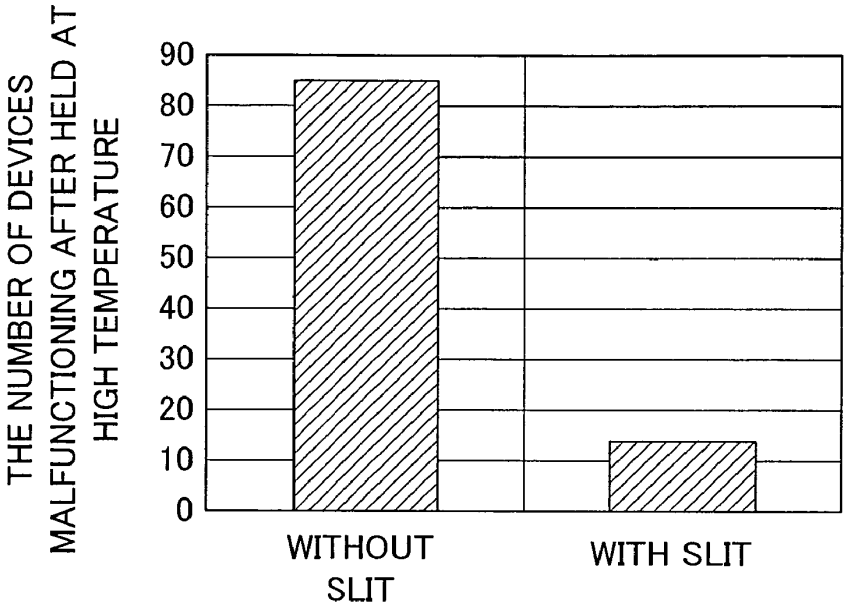

THE NUMBER OF DEVICES MALFUNCTIONING AFTER HELD AT HIGH TEMPERATURE
90
80
70
60
50
40
30
20
10
0
WITHOUT SLIT
WITH SLIT

FIG. 17A

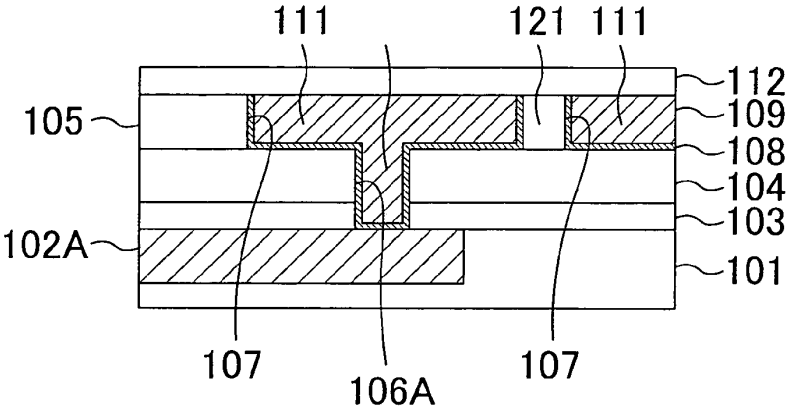



FIG. 17B

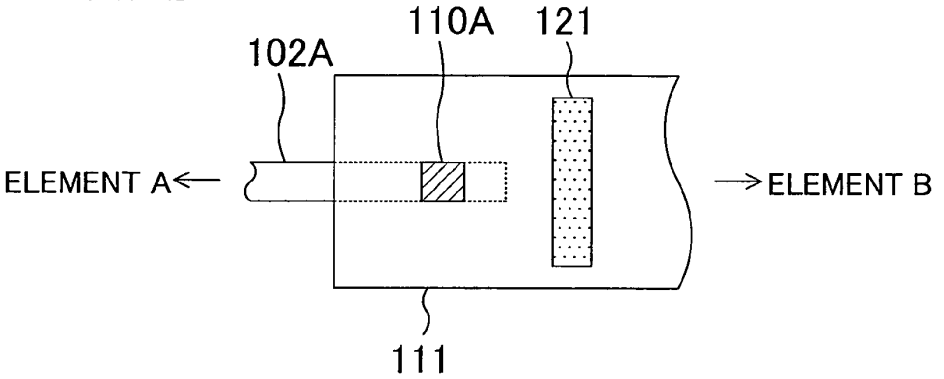


FIG. 18A
PRIOR ART

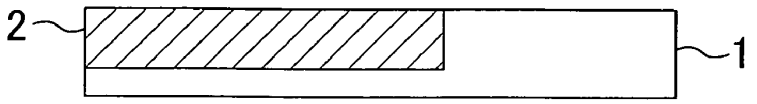



FIG. 18B
PRIOR ART

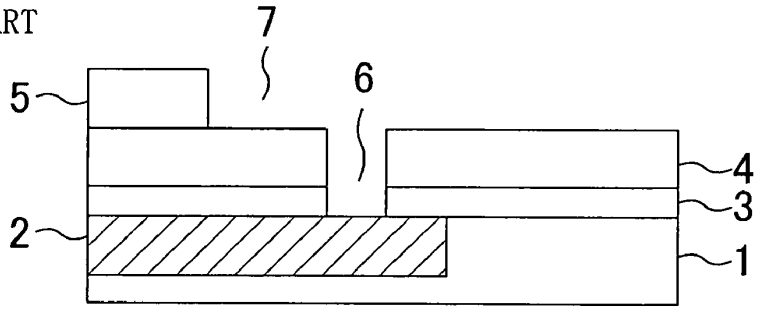



FIG. 18C
PRIOR ART

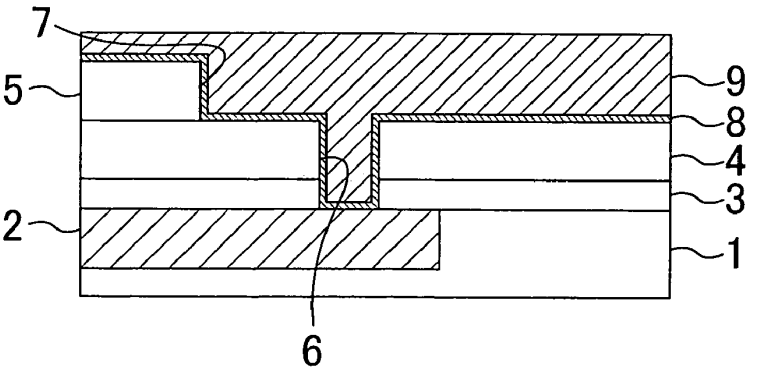


FIG. 19A
PRIOR ART

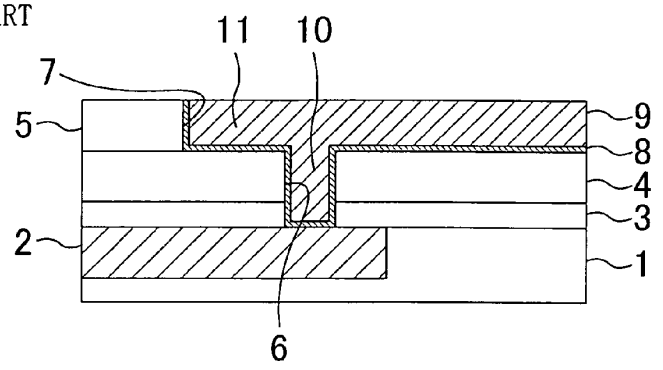



FIG. 19B
PRIOR ART

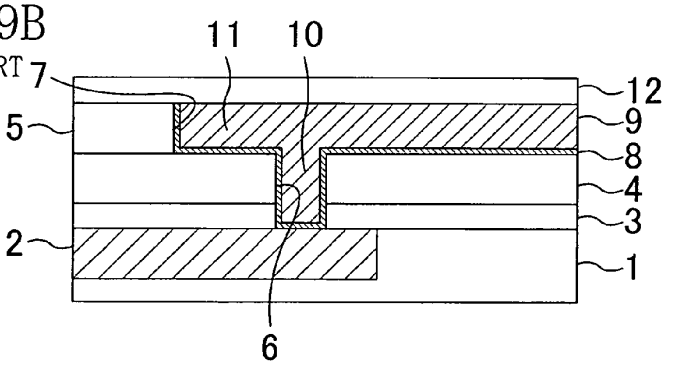



FIG. 19C
PRIOR ART

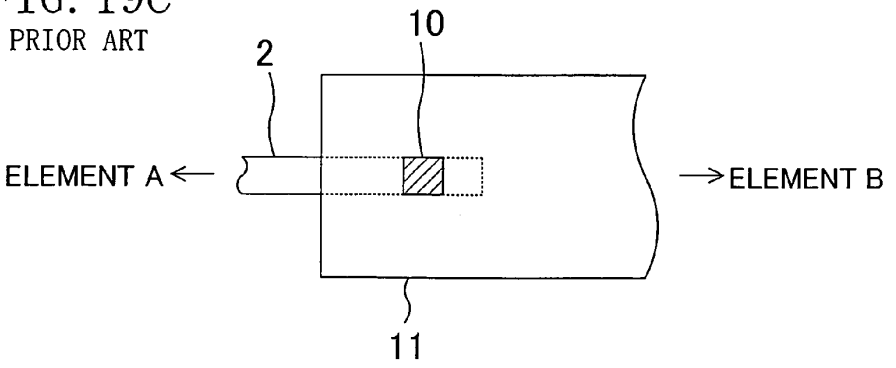


FIG. 20A
PRIOR ART

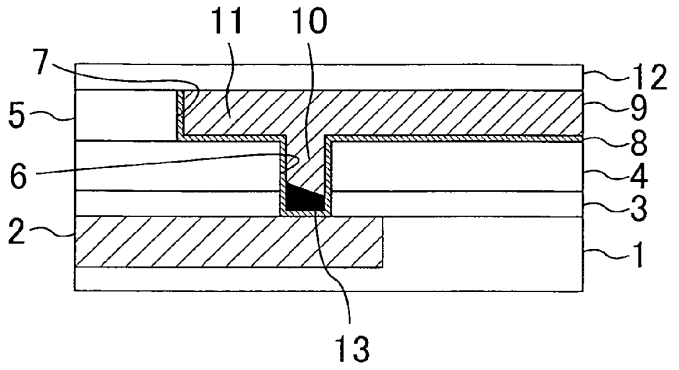
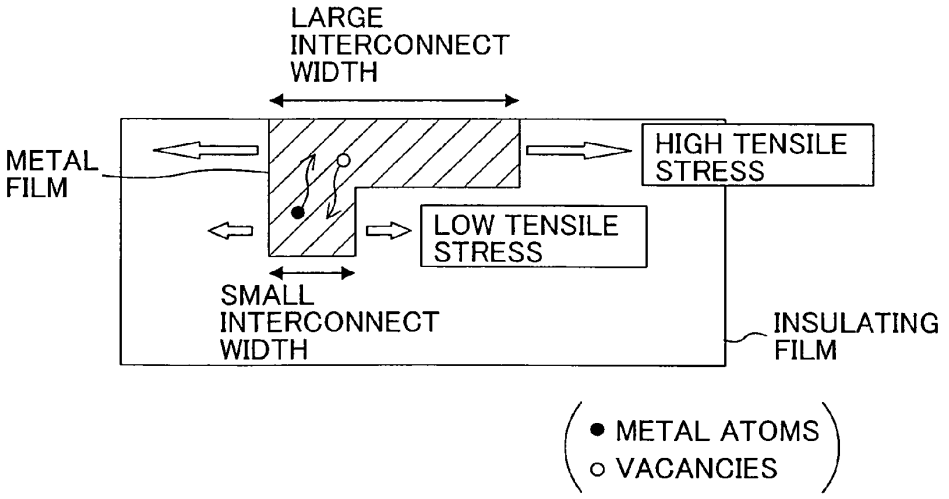



FIG. 20B



# SEMICONDUCTOR DEVICE HAVING VIA CONNECTING BETWEEN INTERCONNECTS

## CROSS-REFERENCE TO RELATED APPLICATION

The disclosure of Japanese Patent Application No. 2003-404437 filed on Dec. 3, 2003 including specification, drawings and claims is incorporated herein by reference in its entirety.

## BACKGROUND OF THE INVENTION

The present invention relates to interconnection structures and methods for forming the structures.

To meet recent increase in the speed and integration density of electronic devices such as semiconductor devices, copper (Cu) having low resistance has been more frequently used as an interconnect material.

FIG. **19**B is a cross-sectional view showing an example of a conventional multilevel interconnection structure formed by using Cu. As shown in FIG. **19**B, a first interconnect **2** is buried in an insulating film **1** formed on a semiconductor substrate (not shown), and a SiN film **3**, a $SiO_2$ film **4** and a FSG (fluorine-doped silicate glass, i.e., fluorine-doped silicon oxide) film **5** are formed in this order over the insulating film **1** and the first interconnect **2**. A via hole **6** is formed through the $SiO_2$ film **4** and the SiN film **3** to reach the first interconnect **2**. An interconnect trench **7** is formed in the FSG film **5** to reach the via hole **6**. A barrier film **8** and a Cu film **9** are buried in this order in the via hole **6** and the interconnect trench **7**, thereby forming a via **10** and a second interconnect **11** in the via hole **6** and the interconnect trench **7**, respectively. A SiN film **12** is formed on the FSG film **5** and the second interconnect **11**.

As shown in FIG. **19**B, the first interconnect **2** and the second interconnect **11** are electrically connected to each other by way of the via **10**. Each of the first interconnect **2** and the second interconnect **11** is electrically connected to another element (now shown) or an external electrode (not shown.) In this manner, the first interconnect **2**, the via **10** and the second interconnect **11** constitute part of a closed circuit in actual use.

FIG. **19**C is a plan view showing the multilevel interconnection structure shown in FIG. **19**B when viewed above. As shown in FIG. **19**C, the first interconnect **2** has a width smaller than that of the second interconnect **11**. Specifically, the width of the first interconnect **2** is 0.2 μm, the diameter of the via **10** (the via hole **6**) is 0.20 μm, and the width of the second interconnect **11** is 10 μm.

FIGS. **18**A through **18**C and **19**A are cross-sectional views showing respective process steps of a conventional method for forming the multilevel interconnection structure shown in FIG. **19**B (see Japanese Unexamined Patent Publication (Kokai) No. 2000-331991.)

First, as shown in FIG. **18**A, an insulating film **1** is formed on the surface of a semiconductor substrate (not shown), and then a first interconnect **2** is formed in the insulating film **1**.

Next, as shown in FIG. **18**B, a SiN film **3**, a $SiO_2$ film **4** and a FSG film **5** are formed in this order over the insulating film **1** and the first interconnect **2** by a plasma chemical vapor deposition (plasma CVD) process. Thereafter, lithography and dry etching are alternately performed twice (i.e., lithography and dry etching are each performed twice), thereby forming a via hole **6** through the $SiO_2$ film **4** and the SiN film **3** to reach the first interconnect **2** and also forming an interconnect trench **7** in the FSG film **5** to reach the via hole **6**.



Then, as shown in FIG. **18**C, a barrier film **8** is deposited by a physical vapor deposition (PVD) process to fill the via hole **6** and the interconnect trench **7**. Then, a Cu film **9** is formed by a plating process on the barrier film **8** to completely fill the via hole **6** and the interconnect trench **7**.

Thereafter, as shown in FIG. **19**A, parts of the barrier film **8** and the Cu film **9** extending off the interconnect trench **7** are removed by a chemical/mechanical polishing (CMP) process. In this manner, a second interconnect **11** is formed in the interconnect trench **7**, and a via **10** connecting the first interconnect **2** and the second interconnect **11** to each other is formed in the via hole **6**.

Lastly, a SiN film **12** is deposited over the FSG film **5** and the second interconnect **11** (the Cu film **9**), thus completing the multilevel interconnection structure shown in FIG. **19**B.

## SUMMARY OF THE INVENTION

However, this conventional multilevel interconnection structure has the following drawbacks. A large number of vacancies are present in the Cu film **9** deposited by plating. When the multilevel interconnection structure is held at high temperature, these vacancies move along the gradient of stress. Specifically, if compressive stress inside the via **10** is higher than compressive stress inside the second interconnect **11**, i.e., if tensile stress inside the via **10** is lower than tensile stress inside the second interconnect **11**, vacancies flow from the second interconnect **11** into the via **10**. In particular, in a multilevel interconnection structure as shown in FIGS. **19**B and **19**C, the volume of the second interconnect **11** is much greater than that of the via **10**, so that a large number of vacancies flow from the second interconnect **11** into the via **10**. As a result, as shown in FIG. **20**A, plastic deformation occurs in a part of the Cu film **9** constituting the via **10**, so that a void **13** is created in the via hole **6**. If the electrical connection between the first interconnect **2** and the second interconnect **11** is broken by this void **13**, the device malfunctions.

It is therefore an object of the present invention to achieve a highly-reliable multilevel interconnection structure which does not cause malfunction even when the structure is held at high temperature.

To achieve the object, a first interconnection structure according to the present invention includes: a lower interconnect; an upper interconnect; a first insulating film provided between the lower interconnect and the upper interconnect; and a second insulating film provided under the first insulating film, wherein the lower interconnect and the upper interconnect are connected to each other by way of a via formed in the first insulating film, at least one dummy via is connected to the upper interconnect, the lower interconnect is formed in the second insulating film, and the bottom of the dummy via is located in the second insulating film.

In the first interconnection structure, the dummy via is provided on the upper interconnect near the via, so that vacancies in a part of a conductive film constituting the upper interconnect are divided and respectively flow into the via and the dummy via. That is, the dummy via reduces the stress gradient from the upper interconnect to the via. Accordingly, even when the interconnection structure is held at high temperature, flowing of vacancies from the upper interconnect to the via is suppressed. As a result, plastic deformation of a part of the conductive film constituting the via, i.e., occurrence of a void inside the via hole, is suppressed, so that a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented.

In addition, in the first interconnection structure, the bottom of the dummy via is located in the second insulating film below the first insulating film. Therefore, a hole for forming the dummy via is deeper than a hole for forming the via (i.e., a via hole.) Accordingly, the stress gradient between the upper interconnect and the dummy via is steeper than that between the upper interconnect and the via. As a result, flowing of vacancies from the part of the conductive film constituting the upper interconnect into the dummy via precedes that into the via. This more effectively suppresses plastic deformation of the part of the conductive film constituting the via, i.e., occurrence of a void in the via hole. As a result, the reliability of the multilevel interconnection structure is further enhanced.

A dummy via and a dummy interconnect herein means a pseudo via or a pseudo interconnect which do not constitute a closed circuit in actual use of a device with an interconnection structure including these via and interconnect (i.e., no current flows therein during actual use of the device.)

In the first interconnection structure, the bottom of the dummy via may be connected to a dummy interconnect formed in the second insulating film. Then, a hole for forming a dummy via is easily formed by etching the first insulating film with the dummy interconnect used as an etching stopper.

In the first interconnection structure, a third insulating film may be formed on the upper interconnect, and the dummy via may be formed in the third insulating film such that the bottom of the dummy via is connected to the upper interconnect.

In the first interconnection structure, the dummy via preferably has a diameter smaller than that of the via.

Then, the diameter of the hole for the dummy via is smaller than that of the hole for the via (i.e., the via hole). In other words, the volume of the dummy via is smaller than that of the via. Accordingly, the stress gradient between the upper interconnect and the dummy via is steeper than that between the upper interconnect and the via. As a result, flowing of vacancies from a part of the conductive film constituting the upper interconnect into the dummy via precedes that into the via. This more effectively suppresses plastic deformation of a part of the conductive film constituting the via, i.e., occurrence of a void in the via hole. As a result, the reliability of the multilevel interconnection structure is further enhanced.

In the first interconnection structure, the dummy via is preferably substantially rectangular in a plan view, and the length of the dummy via and the width of the upper interconnect are provided along the same direction in the plan view.

Then, vacancies which are present in a part of the conductive film constituting the upper interconnect opposite the via with respect to the dummy via flow into the dummy via, so that it is possible to prevent these vacancies from reaching the via. This more effectively suppresses plastic deformation of a part of the conductive film constituting the via, i.e., occurrence of a void in the via hole. As a result, the reliability of the multilevel interconnection structure is further enhanced.

In the first interconnection structure, the via may be substantially circular in a plan view, and the dummy via may have a shape different from that of the via in the plan view.

In the first interconnection structure, the dummy via is preferably closer to a center of the upper interconnect than the via is. In other words, the distance between the via and the end of the upper interconnect opposite the via with respect to the dummy via (which will be also referred to as the end of the upper interconnect toward the dummy via) is preferably longer than the distance between the via and the other end of the upper interconnect, i.e., the end of the upper interconnect toward the via.

Then, the distance between the via and the end of the upper interconnect toward the dummy via is longer than the distance between the via and the other end of the upper interconnect. In other words, a first region in the upper interconnect between the end thereof toward the dummy via and the via is larger than a second region in the upper interconnect between the other end thereof and the via. Therefore, the first region contains a larger number of vacancies than the second region. In addition, the dummy via is provided in this first region, so that vacancies more effectively flow into the dummy via. This more effectively suppresses plastic deformation of a part of the conductive film constituting the via, i.e., occurrence of a void in the via hole. As a result, the reliability of the multilevel interconnection structure is further enhanced.

In the first interconnection structure, the via and the dummy via are preferably spaced at a distance of 1 μm or less.

Then, the effect of making part of vacancies which are to flow into the via flow into the dummy via is ensured. The space between a via (a via hole) and a dummy via (a dummy hole) herein means the space between the edge of the via toward the dummy via and the edge of the dummy via toward the via. The minimum space is set in accordance with the minimum isolation width between interconnects or vias defined by the design rule, for example.

A second interconnection structure according to the present invention includes: a lower interconnect; an upper interconnect; and a first insulating film provided between the lower interconnect and the upper interconnect, wherein the lower interconnect and the upper interconnect are connected to each other by way of a via formed in the first insulating film, and at least one insulating slit is formed in the upper interconnect.

In the second interconnection structure, the insulating slit is provided in the upper interconnect near the via, so that the tensile stress on a part of the upper interconnect near the via is lower than that on the other part of the upper interconnect. That is, the insulating slit reduces the stress gradient from the upper interconnect to the via. Accordingly, even when the interconnection structure is held at high temperature, flowing of vacancies from the upper interconnect toward the via is suppressed. In addition, the insulating slit is made of a material different from that for a conductive film constituting the upper interconnect and the via, so that the insulating slit acts as a barrier against movement of atoms or vacancies in the conductive film. This prevents convection of atoms inside the upper interconnect and the via or accumulation of vacancies on the bottom of the via. As a result, plastic deformation of a part of the conductive film constituting the via, i.e., occurrence of a void inside the via hole, is suppressed, so that a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented.

In the second interconnection structure, the insulating slit may be a part of the first insulating film provided between the lower interconnect and the upper interconnect, for example.

In the second interconnection structure, the insulating slit may be in contact with a portion of the upper interconnect connected to the via. In such a case, if the insulating slit is substantially rectangular in a plan view, the length of the insulating slit is greater than or equal to twice and less than or equal to four times as large as the diameter of the via in the plan view, and a longer side of the insulating slit in the plan view is in contact with the portion of the upper interconnect connected to the via, the foregoing advantages are obtained.

In the second interconnection structure, it is preferable that the insulating slit is substantially rectangular in a plan view, the length of the insulating slit is greater than or equal to twice

and less than or equal to ten times as large as the diameter of the via in the plan view, and the length of the insulating slit and the width of the upper interconnect are provided along the same direction in the plan view.

Then, even in a case where the insulating slit is apart from a portion of the upper interconnect connected to the via, the following advantage is obtained. Flowing of vacancies which are present in a part of a conductive film constituting the upper interconnect opposite the via with respect to the insulating slit is blocked by the insulating slit, so that these vacancies do not reach the via. In addition, the insulating slit is closer to the center of the upper interconnect than the via is. In other words, the distance between the via and the end of the upper interconnect opposite the via with respect to the insulating slit (which will be also referred to as the end of the upper interconnect toward the insulating slit) is longer than the distance between the via and the other end of the upper interconnect, i.e., the end of the upper interconnect toward the via, so that a first region in the upper interconnect between the end thereof toward the insulating slit and the via is larger than a second region in the upper interconnect between the other end thereof and the via. Therefore, the first region contains a larger number of vacancies than the second region. In addition, the insulating slit is provided in this first region, so that movement of vacancies is more effectively prevented by the insulating slit. This more effectively suppresses plastic deformation of a part of the conductive film constituting the via, i.e., occurrence of a void in the via hole. As a result, the reliability of the multilevel interconnection structure is further enhanced.

In the second interconnection structure, the insulating slit is preferably closer to a center of the upper interconnect than the via is.

In the second interconnection structure, the via and the insulating slit are preferably spaced at a distance of 1 μm or less.

Then, the effect of preventing movement of vacancies which are to flow into the via by using the insulating slit is obtained. The space between a via (a via hole) and an insulating slit herein means the space between the edge of the via toward the insulating slit and the edge of the insulating slit toward the via. As described above, the insulating slit may be in contact with the portion of the upper interconnect connected to the via. In this case, the space between the via and the insulating slit is zero.

A third interconnection structure according to the present invention includes: a lower interconnect; an upper interconnect; and a first insulating film provided between the lower interconnect and the upper interconnect, wherein the lower interconnect and the upper interconnect are connected to each other by way of a via formed in the first insulating film, the upper interconnect is divided into a first interconnect portion having a relatively large interconnect width and a second interconnect portion having a relatively small interconnect width, the via is connected to the second interconnect portion, at least one dummy portion connected to the upper interconnect is provided on the first insulating film, and a distance between the dummy portion and a branch point between the first interconnect portion and the second interconnect portion is smaller than a distance between the dummy portion and an edge of the second interconnect portion opposite to the branch point.

In the third interconnection structure, not only advantages similar to those obtained by the first interconnection structure but also the following advantage is obtained. Vacancies which are to enter a second interconnect portion (a narrow interconnect portion) from a first interconnect portion (a wide interconnect portion) and flow into the via are effectively captured in the dummy portion. As a result, the number of devices malfunctioning when being held at high temperature is further reduced.

In the third interconnection structure, the dummy portion may be connected to the first interconnect portion or the second interconnect portion, and a distance between the dummy portion and the branch point may be smaller than a distance between the dummy portion and an edge of the second interconnect portion opposite to the branch point. The distance between the dummy portion and the branch point may be 1 μm or less. The dummy portion may have a shape similar to that of the via or be substantially rectangular in a plan view.

In the third interconnection structure, if the second interconnect portion has an interconnect width of 0.20 μm or less, the foregoing advantages are more remarkable than those in a conventional interconnection structure.

A first method for forming an interconnection structure according to the present invention includes the steps of: depositing a first insulating film on a lower interconnect; forming, in the first insulating film, a via hole reaching the lower interconnect, at least one dummy hole located near the via hole, and an upper interconnect trench connected to the via hole and the dummy hole; and depositing a conductive material in the upper interconnect trench, the via hole and the dummy hole, thereby forming an upper interconnect, a via for connecting the lower interconnect and the upper interconnect to each other, and a dummy via connected to the upper interconnect and insulated from the lower interconnect, wherein the lower interconnect is formed in a second insulating film under the first insulating film, and the dummy hole is formed such that the bottom of the dummy hole is located in the second insulating film.

With the first method, the first interconnection structure according to the present invention is formed, so that advantages similar to those obtained by the first interconnection structure are obtained. To form a via or an upper interconnect, a damascene process such as a dual damascene process or other processes may be used.

A second method for forming an interconnection structure according to the present invention includes the steps of: depositing a first insulating film on a lower interconnect; forming, in the first insulating film, a via hole reaching the lower interconnect and an upper interconnect trench connected to the via hole; depositing a conductive material in the upper interconnect trench and the via hole, thereby forming an upper interconnect and a via for connecting the lower interconnect and the upper interconnect to each other; depositing a second insulating film on the upper interconnect; forming, in the second insulating film, a dummy hole reaching the upper interconnect and located near the via; and depositing a conductive material in the dummy hole, thereby forming at least one dummy via.

With the second method, the first interconnection structure according to the present invention is formed, so that advantages similar to those obtained by the first interconnection structure are obtained. To form a via or an upper interconnect, a damascene process such as a dual damascene process or other processes may be used.

In the first or second method, the via hole and the dummy hole are preferably spaced at a distance of 1 μm or less.

Then, part of vacancies which are to flow into the via flow into the dummy via.

A third method for forming an interconnection structure according to the present invention includes the steps of: depositing a first insulating film on a lower interconnect;

forming, in the first insulating film, a via hole reaching the lower interconnect and an upper interconnect trench connected to the via hole; and depositing a conductive material in the upper interconnect trench and the via hole, thereby forming an upper interconnect and a via for connecting the lower interconnect and the upper interconnect to each other, wherein the step of forming the via hole and the upper interconnect trench includes the step of leaving part of the first insulating film in the upper interconnect trench near the via hole, thereby forming an insulating slit.

With the third method, the second interconnection structure according to the present invention is formed, so that advantages similar to those obtained by the second interconnection structure are obtained. To form a via or an upper interconnect, a damascene process such as a dual damascene process or other processes may be used.

A fourth method for forming an interconnection structure according to the present invention includes the steps of: depositing a first insulating film on a lower interconnect; forming, in the first insulating film, a via hole reaching the lower interconnect, an upper interconnect trench connected to the via hole and divided into a first trench with a relatively large width and a second trench with a relatively small width, and a recess provided near a branch point between the first trench and the second trench; and depositing a conductive material in the upper interconnect trench, the via hole and the recess, thereby forming an upper interconnect, a via for connecting the lower interconnect and the upper interconnect to each other and a dummy portion connected to the upper interconnect and insulated from the lower interconnect, wherein a first interconnect portion constituting the upper interconnect is formed in the first trench and a second interconnect portion constituting the upper interconnect is formed in the second trench.

With the fourth method, the third interconnection structure according to the present invention is formed, so that advantages similar to those obtained by the third interconnection structure are obtained. To form a via or an upper interconnect, a damascene process such as a dual damascene process or other processes may be used.

As described above, according to the present invention, a dummy via or an insulating slit is provided on/in the upper interconnect near via, so that it is possible to prevent flowing of vacancies from an upper interconnect toward a via constituting a closed circuit together with the upper interconnect in actual use. Accordingly, plastic deformation of a part of a conductive film constituting the via, i.e., occurrence of a void in a via hole, is suppressed, resulting in a highly-reliable multilevel interconnection structure. The present invention relates to interconnection structures and methods for forming the structures, and is useful especially when applied to electronic devices such as semiconductor devices.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A through **1**C are cross-sectional views showing respective process steps of a method for forming an interconnection structure according to a first embodiment of the present invention.

FIGS. **2**A and **2**B are cross-sectional views showing respective process steps of the method for forming the interconnection structure of the first embodiment, and FIG. **2**C is a plan view showing the interconnection structure of the first embodiment.

FIG. **3** is a graph showing how an effect achieved by the first embodiment (i.e., the effect of suppressing malfunction after a device has been held at high temperature) depends on a via-to-dummy via space.

FIG. **4** is a plan view showing an interconnection structure according to a modified example of the first embodiment.

FIG. **5** is a graph showing how an effect achieved by the modified example of the first embodiment (i.e., the effect of suppressing malfunction after a device has been held at high temperature) depends on an interconnect width (i.e., the width of a narrow interconnect on which a via is formed.)

FIGS. **6**A through **6**C are cross-sectional views showing respective process steps of a method for forming an interconnection structure according to a second embodiment of the present invention.

FIGS. **7**A and **7**B are cross-sectional views showing respective process steps of the method for forming the interconnection structure of the second embodiment, and FIG. **7**C is a plan view showing the interconnection structure of the second embodiment.

FIG. **8**A is a cross-sectional view showing an interconnection structure according to a third embodiment of the present invention, and FIG. **8**B is a plan view showing the interconnection structure of the third embodiment.

FIG. **9**A is a cross-sectional view showing an interconnection structure according to a fourth embodiment of the present invention, and FIG. **9**B is a plan view showing the interconnection structure of the fourth embodiment.

FIG. **10** is a plan view showing an interconnection structure according to a modified example of the fourth embodiment.

FIGS. **11**A through **11**C are cross-sectional views showing respective process steps of a method for forming an interconnection structure according to a fifth embodiment of the present invention.

FIGS. **12**A through **12**C are cross-sectional views showing respective process steps of the method for forming the interconnection structure of the fifth embodiment.

FIGS. **13**A and **13**B are cross-sectional views showing respective process steps of the method for forming the interconnection structure of the fifth embodiment, and FIG. **13**C is a plan view showing the interconnection structure of the fifth embodiment.

FIGS. **14**A through **14**C are cross-sectional views showing respective process steps of a method for forming an interconnection structure according to a sixth embodiment of the present invention.

FIGS. **15**A and **15**B are cross-sectional views showing respective process steps of the method for forming the interconnection structure of the sixth embodiment, and FIG. **15**C is a plan view showing the interconnection structure of the sixth embodiment.

FIG. **16** is a graph showing an effect achieved by the sixth embodiment (i.e., the effect of suppressing malfunction after a device has been held at high temperature).

FIG. **17**A is a cross-sectional view showing an interconnection structure according to a seventh embodiment of the present invention, and FIG. **17**B is a plan view showing the interconnection structure of the seventh embodiment.

FIGS. **18**A through **18**C are cross-sectional views showing respective process steps of a conventional method for forming an interconnection structure.

FIGS. **19**A and **19**B are cross-sectional views showing respective process steps of the conventional method for forming an interconnection structure, and FIG. **19**C is a plan view showing the conventional interconnection structure.

FIG. **20**A is a view for explaining problems in the conventional interconnection structure, and FIG. **20**B is an illustration for explaining a result of an examination carried out by the present inventor on problems in the conventional interconnection structure.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

(Principle of the Present Invention)

First, for a phenomenon in which a void occurs in a via hole in a conventional multilevel interconnection structure, a result of an examination carried out by the present inventor (i.e., a mechanism of this phenomenon) will be described.

A metal film is affected by its surrounding films depending on an interconnection structure including the metal film. For example, as shown in FIG. **20**B, a metal film (e.g., a Cu film) formed in part of an interconnect trench with a narrow interconnect width provided in an insulating film is slightly stretched by its surrounding insulating films. That is, this Cu film is under relatively low tensile stress. On the other hand, a Cu film formed in part of the interconnect trench with a wide interconnect width in the insulating film is strongly stretched by its surrounding insulating films. That is, this Cu film is under relatively high tensile stress. Such tensile stress occurs mainly because of the difference in a thermal expansion coefficient between a metal film and an insulating film or because of shrinkage of the metal film resulting from thermal load in a subsequent step. The tensile stress greatly changes depending on the shapes of the interconnect trench and the via hole, the placement density and others.

A metal film made of Cu or another metal generally has a crystal structure in which atoms are relatively regularly arranged immediately after formation of the film. To form a Cu film, which is mainly used as an interconnect material, is generally formed by electroplating. The Cu film formed by electroplating contains a large number of vacancies. In addition, in the interconnection structure shown in FIG. **20**B, vacancies contained in the Cu film are more likely to gather in a portion of the Cu film where tensile stress is low than in a portion thereof where tensile stress is high. This is because stress applied from the neighboring insulating films to the crystal structure of the Cu film is relaxed by entering of vacancies into the portion of the Cu film with low tensile stress, i.e., entering of Cu atoms into the portion of the Cu film with high tensile stress.

Accordingly, when the flexibility of Cu atoms and vacancies is enhanced by, for example, application of heat to the interconnection structure, vacancies move along the stress gradient in the Cu film, i.e., move from the portion of the Cu film with high tensile stress to the portion of the Cu film with low tensile stress (where the direction of movement of Cu atoms is opposite to that of vacancies.) As a result, vacancies readily gather in part of the interconnection structure with a narrow interconnect width or the bottom or corners of the interconnect, and thus voids readily occur.

Based on the foregoing finding, the following embodiments of the present invention are made to implement a technical idea in which the stress gradient in a conductive film serving as an interconnect is reduced so as to suppress the movement of vacancies in the conductive film and thereby to avoid occurrence of a void in the interconnect after formation thereof.

### Embodiment 1

### A Case where a Via and a Dummy Via are Provided in the Same Layer (Basic Structure)

Hereinafter, an interconnection structure and a method for forming the structure according to a first embodiment of the present invention will be described with reference to the drawings.

FIG. **2**B is a cross-sectional view showing the interconnection structure of the first embodiment. As shown in FIG. **2**B, a first interconnect **102**A and a dummy interconnect **102**B are buried in an insulating film **101** formed on the semiconductor substrate (not shown). A SiN film **103**, a $SiO_2$ film **104** and an FSG film **105** are stacked over the insulating film **101**, the first interconnect **102**A and the dummy interconnect **102**B. A via hole **106**A and a dummy via hole (dummy hole) **106**B are formed in the $SiO_2$ film **104** and the SiN film **103** to reach the first interconnect **102**A and the dummy interconnect **102**B, respectively. An interconnect trench **107** is formed in the FSG film **105** to be connected to the via hole **106**A and the dummy hole **106**B. A barrier film **108** and a Cu film **109** are buried in this order in the via hole **106**A, the dummy hole **106**B and the interconnect trench **107**, thereby forming a via **110**A, a dummy via **10**B, and a second interconnect **111** in the via hole **106**A, the dummy hole **106**B and the interconnect trench **107**, respectively. The dummy via **110**B is connected to the second interconnect **111** near the via **110**A. A SiN film **112** is formed on the FSG film **105** and the second interconnect **111**.

As shown in FIG. **2**B, the first interconnect **102**A and the second interconnect **111** are electrically connected to each other by way of the via **110**A. Each of the first interconnect **102**A and the second interconnect **111** is electrically connected to another element (now shown) or an external electrode (not shown.) In this manner, the first interconnect **102**A, the via **110**A and the second interconnect **111** constitute part of a closed circuit in actual use. On the other hand, neither the dummy interconnect **102**B nor the dummy via **110**B constitutes a closed circuit in actual use. That is, even if the dummy interconnect **102**B and the dummy via **110**B are omitted in the interconnection structure shown in FIG. **2**B, a device with this interconnection structure is operable at least immediately after fabrication.

FIG. **2**C is a plan view showing the multilevel interconnection structure shown in FIG. **2**B when viewed above. As shown in FIG. **2**C, in this embodiment, each of the first interconnect **102**A and the dummy interconnect **102**B has a width smaller than that of the second interconnect **111**. Specifically, the width of each of the first interconnect **102**A and the dummy interconnect **102**B is, for example, 0.2 μm, the diameter of each of the via **110**A (the via hole **106**A) and the dummy via **110**B (the dummy hole **106**B) is, for example, 0.20 μm, and the width of the second interconnect **111** is, for example, 10 μm. The space between the via **110**A and the dummy via **110**B, more specifically, the space between the edge of the via **110**A toward the dummy via **110**B and the edge of the dummy via **110**B toward the via **110**A is 0.2 μm, for example. In the present invention, if the planar shape (the shape in plan view) of a via (via hole) is a circle, the diameter of the via (via hole) is the diameter of this circle whereas if the planar shape of the via (via hole) is a square, the diameter of the via (via hole) is the length of a side of this square.

FIGS. **1**A through **1**C and FIG. **2**A are cross-sectional views showing respective process steps of a method for forming the multilevel interconnection structure shown in FIG. **2**B according to the first embodiment.

First, as shown in FIG. **1**A, an insulating film **101** is formed on the surface of a semiconductor substrate (not shown), and then a first interconnect **102**A and a dummy interconnect **102**B are formed in the insulating film **101**.

Next, as shown in FIG. **1**B, a SiN film **103**, a $SiO_2$ film **104** and a FSG film **105** are formed in this order over the insulating film **101**, the first interconnect **102**A and the dummy interconnect **102**B by a plasma CVD process, for example. Thereafter, lithography and dry etching are alternately performed twice (i.e., lithography and dry etching are each performed twice), thereby forming a via hole **106**A and a dummy hole **106**B in the $SiO_2$ film **104** and the SiN film **103** to reach the

first interconnect **102**A and the dummy interconnect **102**B, respectively, and also forming an interconnect trench **107** in the FSG film **105** to reach the via hole **106**A and the dummy hole **106**B.

Then, as shown in FIG. **1**C, a barrier film **108** is deposited by a PVD process, for example, to partly fill the via hole **106**A, the dummy hole **106**B and the interconnect trench **107**. Then, a Cu film **109** is formed by a plating process, for example, on the barrier film **108** to completely fill the via hole **106**A, the dummy hole **106**B and the interconnect trench **107**.

Thereafter, as shown in FIG. **2**A, parts of the barrier film **108** and the Cu film **109** extending off the interconnect trench **107** are removed by a CMP process, for example. In this manner, a second interconnect **111** is formed in the interconnect trench **107**. In addition, a via **110**A is formed in the via hole **106**A to connect the first interconnect **102**A and the second interconnect **111** to each other, and a dummy via **110**B is formed in the dummy hole **106**B to connect the dummy interconnect **102**B and the second interconnect **111** to each other. The dummy via **110**B is not connected to the first interconnect **102**A.

Lastly, a SiN film **112** is deposited over the FSG film **105** and the second interconnect **111** (the Cu film **109**), thus completing the multilevel interconnection structure shown in FIG. **2**B.

With the foregoing interconnection structure and the method for forming the structure according to the first embodiment, a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented. This is because of the following reasons. The dummy via **110**B is provided on the second interconnect **111** near the via **110**A, so that vacancies in a part of the conductive film (the Cu film **109**) constituting the second interconnect **111** are divided and respectively flow into the via **110**A and the dummy via **110**B. That is, the dummy via **110**B reduces the number of vacancies flowing into each via so that the stress gradient from the second interconnect **111** to the via **110**A is reduced. Accordingly, even when the interconnection structure is held at high temperature, flowing of vacancies from the second interconnect **111** into the via **110**A is suppressed. As a result, plastic deformation of a part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void inside the via hole **106**A, is suppressed, so that a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented.

In the first embodiment, the dummy interconnect **102**B is provided under the dummy via **110**B (the dummy hole **106**B). Accordingly, the dummy hole **106**B is easily formed by etching the $SiO_2$ film **104** and the SiN film **103** with the dummy interconnect **102**B used as an etching stopper.

In the first embodiment, the space between the via **110**A and the dummy via **110**B (i.e., the space between the via hole **106**A and the dummy hole **106**B: hereinafter referred to as a via-to-dummy via space) is preferably as small as possible. To obtain the effect of reducing the number of vacancies flowing into the via **110**A by using the dummy via **110**B, the via-to-dummy via space is preferably 25 μm or less and is more preferably 1 μm or less. The minimum via-to-dummy via space can be set in accordance with the minimum isolation width (e.g., 0.2 μm) between interconnects or vias defined by the design rule, for example. If the minimum isolation width between interconnects is set substantially equal to the minimum interconnect width, the minimum via-to-dummy via space may be set in accordance with the minimum interconnect width.

FIG. **3** shows how an effect achieved by the present invention (i.e., the effect of suppressing malfunction after a device has been held at high temperature) depends on a via-to-dummy via space. In FIG. **3**, the ordinate indicates "the number of devices malfunctioning after being held at high temperature" and the abscissa indicates "via-to-dummy via space (μm)". The "without dummy via" in the abscissa corresponds to a case where the via-to-dummy via space is unlimited. As shown in FIG. **3**, as the via-to-dummy via space decreases, the number of malfunctioning devices decreases. In other words, the effect of the present invention becomes remarkable. This is because as the via-to-dummy via space decreases, vacancies which are to gather in the via are more likely to be absorbed in the dummy via.

However, as shown in FIG. **3**, when the via-to-dummy via space is 30 μm or more, it is difficult to effectively suppress occurrence of a void in the via by using the dummy via. This is because of the following reason. Vacancies moves within a limited range and therefore it is difficult for the dummy via to absorb vacancies which are to enter the via when the via-to-dummy via space is large. Accordingly, when the via-to-dummy via space is large, especially when the via-to-dummy via space greatly exceeds 30 μm, the incidence of voids is substantially equal to that in the case of "without dummy via". As a result, the number of devices malfunctioning after being held at high temperature is not sufficiently reduced.

In the first embodiment, the number of dummy vias **110**B provided for one via **110**A is preferably as large as possible. Specifically, it is preferable to provide dummy vias **110**B as many as possible on a part of the second interconnect **111** where the dummy vias **110**B do not affect circuit operation.

## Modified Example of Embodiment 1

Hereinafter, an interconnection structure and a method for forming the structure according to a modified example of the first embodiment will be described with reference to the drawings.

FIG. **4** is a plan view showing the interconnection structure of the modified example of the first embodiment.

As shown in FIG. **4**, this modified example is different from the first embodiment (see FIG. **2**C) in the following ways. First, the second interconnect **111** includes: a wide interconnect portion **111***a* having a width of 10 μm, for example; and a narrow interconnect portion **111***b* having a width of 0.20 μm, for example, and branching off from the wide interconnect portion **111***a*. Second, the via **110**A (the via hole **106**A) is connected to the narrow interconnect portion **111***b*. Third, a plurality of dummy vias **110**B (the dummy holes **106**B) are connected to the branch point between the wide interconnect portion **111***a* and the narrow interconnect portion **111***b* and to portions of the wide interconnect portion **111***a* near the branch point.

That is, the method for forming the interconnection structure according to this modified example is different from that of the first embodiment in that in the process step shown in FIG. **1**B, the interconnect trench **107** divided into a first trench with a relatively large width is formed and a second trench with a relatively small width and the dummy holes **106**B are also formed near the branch point between the first trench and the second trench.

In this modified example, not only the advantages obtained by the first embodiment but also the following advantage is obtained. Vacancies which are to enter the narrow interconnect portion **111***b* from the wide interconnect portion **111***a* and flow into the via **110**A are effectively captured in the

dummy vias **110**B. As a result, the number of devices malfunctioning when being held at high temperature is further reduced.

In this modified example, one or more dummy vias **110**B (dummy holes **106**B) may be connected to the branch point between the wide interconnect portion **111***a* and the narrow interconnect portion **111***b* or portions of the wide interconnect portion **111***a* near the branch point. However, the dummy vias **110**B are not necessarily provided only at the branch point or its neighboring portions. For example, if a dummy via **110**B is located in part of the narrow interconnect portion **111***b* relatively near the wide interconnect portion **111***a*, most of vacancies which are to enter the via **110**A are captured in the dummy via **110**B before reaching the via **110**A. Accordingly, it is possible to prevent occurrence of a void in the via **110**A.

In this modified example, the distance between the branch point and each of the dummy vias **110**B is preferably smaller than the distance between an edge of the wide interconnect portion **111***a* opposite to the branch point and each of the dummy vias **110**B.

In this modified example, dummy vias **110**B each having substantially the same shape as that of the via **110**A in plan view are provided. Alternatively, dummy portions each having a shape (e.g., a rectangle) different from that of the via **110**A in plan view may be provided.

FIG. **5** shows how an effect achieved by the dummy via **110**B of this modified example (i.e., a dummy portion formed in part of the wide interconnect portion **111***a* near the branch point, for example) depends on a via-formed interconnect width (i.e., the width of the narrow interconnect portion **111***b* where the via **110**A is formed.) In FIG. **5**, the ordinate indicates "the number of devices malfunctioning after being held at high temperature" and the abscissa indicates "via-formed interconnect width (μm)". The "without dummy via" in the abscissa corresponds to a case where no dummy via **110**B is provided on the wide interconnect portion **11***a* near the branch point. As shown in FIG. **5**, in a case where the width of the interconnect portion **11***b* on which the via **110**A is formed is about 10 μm, i.e., the width of the interconnect portion **111***b* is substantially equal to that of the interconnect portion **111***a* to which the interconnect portion **111***b* is connected, even if a dummy via (dummy portion) is formed near the branch point between these interconnect portions, the number of malfunctioning devices does not change greatly. That is, if the width of the interconnect portion **111***b* on which the via **110**A is formed is relatively large, the interconnect portion **111***b* contains a large amount of metal. Accordingly, this interconnect portion **111***b* is likely to contain a large number of defects such as voids caused by the presence of metal. As a result, the number of malfunctioning devices is relatively large depending on the amount of metal contained in the interconnect portion **111***b*.

On the other hand, as the width of the interconnect portion **111***b* on which the via **110**A is formed decreases, the amount of metal contained in the interconnect portion **111***b* decreases. Accordingly, the number of defects occurring in the interconnect portion **111***b* due to the presence of metal slightly decreases. However, as the interconnect portion **111***b* becomes narrower, the diameter of the via **110**A provided on the interconnect portion **111***b* decreases, so that defects such as voids are more likely to concentrate in the via **110**A. In view of this, as shown in FIG. **4**, the dummy via (dummy portion) **110**B is formed near the branch point between the narrow interconnect portion **111***b* on which the via **110**A is formed and the wide interconnect portion **111***a*. In this manner, the incidence of malfunction is reduced in accordance with reduction of the interconnect width of the narrow interconnect portion **111***b*, as shown in FIG. **5**. This is because the number of defects occurring in the metal film decreases with reduction of the interconnect width and, in addition, defects which are to concentrate in the via are absorbed in the dummy vias in advance. Specifically, as the width of the interconnect portion **111***b* on which the via **110**A is formed decreases, i.e., the diameter of the via **110**A decreases, a larger number of defects are absorbed in the dummy vias **110**B. This absorbing effect is remarkable especially when the width of the narrow interconnect portion **111***b* is about 0.20 μm or less, as shown in FIG. **5**.

## Embodiment 2

### A Case where a Via and a Dummy Via are Provided in the Same Layer

(Without a Dummy Interconnect)

Hereinafter, an interconnection structure and a method for forming the structure according to a second embodiment of the present invention will be described with reference to the drawings.

FIG. **7**B is a cross-sectional view showing the interconnection structure of the second embodiment. FIG. **7**C is a plan view showing the multilevel interconnection structure shown in FIG. **7**B when viewed from above. In FIGS. **7**B and **7**C, components already described in the first embodiment with reference to FIGS. **1**A through **1**C and **2**A through **2**C are denoted by the same reference numerals, and detailed description thereof will be omitted.

As shown in FIGS. **7**B and **7**C, the second embodiment is different from the first embodiment in the following ways. The dummy interconnect **102**B is not provided, a dummy hole **106**C deeper than the dummy hole **106**B is provided instead of the dummy hole **106**B, and a dummy via **110**C is formed in the dummy hole **106**C instead of the dummy via **110**B. That is, the bottom of the dummy via **110**C (the dummy hole **106**C) is located in an insulating film **101**, and the dummy hole **106**C is deeper than a via hole **106**A.

In this embodiment, the dummy via **110**C is also connected to a second interconnect **111** near the via **110**A.

As shown in FIG. **7**B, the dummy via **110**C does not constitute a closed circuit in actual use. In other words, even if the dummy hole **106**C is omitted in the interconnection structure shown in FIG. **7**B, a device with this interconnection structure is operable at least immediately after fabrication.

In addition, in this embodiment, a first interconnect **102**A has a width smaller than that of the second interconnect **111**, as shown in FIG. **7**C. Specifically, the width of the first interconnect **102**A is, for example, 0.2 μm, the diameter of each of the via **110**A (the via hole **106**A) and the dummy via **110**C (the dummy hole **106**C) is, for example, 0.20 μm, and the width of the second interconnect **111** is, for example, 10 μm. The space between the via **110**A and the dummy via **110**C, more specifically, the space between the edge of the via **110**A toward the dummy via **110**C and the edge of the dummy via **110**C toward the via **110**A is 0.2 μm, for example.

FIGS. **6**A through **6**C and **7**A are cross-sectional views showing respective process steps of a method for forming the multilevel interconnection structure shown in FIG. **7**B according to the second embodiment.

First, as shown in FIG. **6**A, an insulating film **101** is formed on the surface of a semiconductor substrate (not shown), and then a first interconnect **102**A is formed in the insulating film **101**.

Next, as shown in FIG. **6**B, a SiN film **103**, a $SiO_2$ film **104** and a FSG film **105** are formed in this order over the insulating film **101** and the first interconnect **102**A by a plasma CVD process, for example. Thereafter, lithography and dry etching are alternately performed twice (i.e., lithography and dry etching are each performed twice), thereby forming a via hole **106**A in the $SiO_2$ film **104** and the SiN film **103** to reach the first interconnect **102**A and also forming a dummy hole **106**C in the $SiO_2$ film **104**, the SiN film **103** and the insulating film **101**. In addition, an interconnect trench **107** is formed in the FSG film **105** to reach the via hole **106**A and the dummy hole **106**C.

Then, as shown in FIG. **6**C, a barrier film **108** is deposited by a PVD process, for example, to partly fill the via hole **106**A, the dummy hole **106**C and the interconnect trench **107**. Then, a Cu film **109** is formed by a plating process, for example, on the barrier film **108** to completely fill the via hole **106**A, the dummy hole **106**C and the interconnect trench **107**.

Thereafter, as shown in FIG. **7**A, parts of the barrier film **108** and the Cu film **109** extending off the interconnect trench **107** are removed by a CMP process, for example. In this manner, a second interconnect **111** is formed in the interconnect trench **107**. In addition, a via **110**A is formed in the via hole **106**A to connect the first interconnect **102**A and the second interconnect **111** to each other. A dummy via **110**C connected only to the second interconnect **111** is formed in the dummy hole **106**C. In other words, the dummy via **110**C is not connected to the first interconnect **102**A.

Lastly, a SiN film **112** is deposited over the FSG film **105** and the second interconnect **111** (the Cu film **109**), thus completing the multilevel interconnection structure shown in FIG. **7**B.

With the foregoing interconnection structure and the method for forming the structure according to the second embodiment, a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented. This is because of the following reasons. The dummy via **110**C is provided on the second interconnect **111** near the via **110**A, so that vacancies in a part of the conductive film (the Cu film **109**) constituting the second interconnect **111** are divided and respectively flow into the via **110**A and the dummy via **110**C. That is, the dummy via **110**C reduces the number of vacancies flowing into each via so that the stress gradient from the second interconnect **111** to the via **110**A is reduced. Accordingly, even when the interconnection structure is held at high temperature, flowing of vacancies from the second interconnect **111** into the via **110**A is suppressed. As a result, plastic deformation of a part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void inside the via hole **106**A, is suppressed, so that a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented.

In the second embodiment, the resultant multilevel interconnection structure is more reliable than that obtained in the first embodiment. This is because of the following reasons. In this embodiment, the dummy hole **106**C is deeper than the via hole **106**A. Accordingly, the stress gradient between the second interconnect **111** and the dummy via **110**C is steeper than that between the second interconnect **111** and the via **110**A, so that flowing of vacancies from the part of the conductive film (the Cu film **109**) constituting the second interconnect **111** into the dummy via **110**C precedes that into the via **110**A. This more effectively suppresses plastic deformation of the part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void in the via hole **106**A. As a result, the resultant multilevel interconnection structure is more reliable than that obtained in the first embodiment.

In the second embodiment, the space between the via **110**A and the dummy via **110**C (i.e., the space between the via hole **106**A and the dummy hole **106**C: hereinafter referred to as a via-to-dummy via space) is preferably as small as possible. To obtain the effect of reducing the number of vacancies flowing into the via **110**A by using the dummy via **110**C., the via-to-dummy via space is preferably 25 μm or less and is more preferably 1 μm or less. Then, the effect of making part of vacancies which are to flow into the via **110**A flow into the dummy via **110**C is ensured. The minimum via-to-dummy via space can be set in accordance with the minimum isolation width (e.g., 0.2 μm) between interconnects or vias defined by the design rule, for example. If the minimum isolation width between interconnects is set substantially equal to the minimum interconnect width, the minimum via-to-dummy via space may be set in accordance with the minimum interconnect width.

In the second embodiment, the number of dummy vias **110**C provided for one via **110**A is preferably as large as possible. Specifically, it is preferable to provide dummy vias **10**C as many as possible on a part of the second interconnect **111** where the dummy vias **110**C do not affect circuit operation.

In addition, in the second embodiment, if the second interconnect **111** includes a wide interconnect portion having a width of, for example, about 10 μm and a narrow interconnect portion having a width of, for example, about 0.20 μm or less and branching off from the wide interconnect portion and if the via **110**A (the via hole **106**A) is connected to the narrow interconnect portion, one or more dummy vias **110**C (dummy holes **106**C) are preferably connected to the branch point between the wide interconnect portion and the narrow interconnect portion or to part of the wide interconnect portion near the branch point. Then, vacancies which are to enter the narrow interconnect portion from the wide interconnect portion and flow into the via **110**A are effectively captured in the dummy vias **110**C. The dummy vias **110**C are not necessarily provided only at the branch point or its neighboring portions. For example, if a dummy via **110**C is located in part of the narrow interconnect portion relatively near the wide interconnect portion, most of vacancies which are to enter the via **110**A are captured in the dummy via **110**C before reaching the via **110**A. Accordingly, it is possible to prevent occurrence of a void in the via **110**A. As a result, the number of devices malfunctioning when held at high temperature is further reduced.

## Embodiment 3

### A Case where a Via and a Dummy Via are Provided in the Same Layer

(With a Smaller Dummy Via)

Hereinafter, an interconnection structure and a method for forming the structure according to a third embodiment of the present invention will be described with reference to the drawings.

FIG. **8**A is a cross-sectional view showing the interconnection structure of the third embodiment. FIG. **8**B is a plan view showing the multilevel interconnection structure shown in FIG. **8**A when viewed from above. In FIGS. **8**A and **8**B, components already described in the first embodiment with reference to FIGS. **1**A through **1**C and **2**A through **2**C are denoted by the same reference numerals, and detailed description thereof will be omitted.

As shown in FIGS. **8**A and **8**B, the third embodiment is different from the first embodiment in the following ways. Instead of the dummy hole **106**B, a dummy hole **106**D with a diameter smaller than that of the dummy hole **106**B is provided and a dummy via **110**D is provided in the dummy hole **106**D instead of the dummy via **110**B. That is, in this embodiment, the diameter of the dummy hole **106**D (the dummy via HOD) is smaller that of a via hole **106**A (a via **110**A).

In this embodiment, the dummy via **110**D is connected to a second interconnect **111** near the via **110**A.

As shown in FIG. **8**A, neither a dummy interconnect **102**B nor the dummy via **110**D constitutes a closed circuit in actual use. In other words, even if the dummy via **110**D is omitted in the interconnection structure shown in FIG. **8**A, a device with this interconnection structure is operable at least immediately after fabrication.

In addition, in this embodiment, the width of each of a first interconnect **102**A and the dummy interconnect **102**B is smaller than that of the second interconnect **111**, as shown in FIG. **8**B. Specifically, the width of each of the first interconnect **102**A and the dummy interconnect **102**B is, for example, 0.2 μm, the diameter of the via **110**A (the via hole **106**A) is, for example, 0.20 μm, the diameter of the dummy via **110**D (the dummy hole **106**D) is, for example, 0.16 μm, and the width of the second interconnect **111** is, for example, 10 μm. The space between the via **110**A and the dummy via **110**D, more specifically, the space between the edge of the via **110**A toward the dummy via **110**D and the edge of the dummy via **110**D toward the via **110**A is 0.24 μm, for example.

A method for forming the multilevel interconnection structure shown in FIG. **8**A according to the third embodiment is different from that of the first embodiment (shown in FIGS. **1**A through **1**C, **2**A and **2**B) only in that the dummy hole **106**D reaching the dummy interconnect **102**B and having a diameter smaller than that of the dummy hole **106**B is formed instead of the dummy hole **106**B in the process step shown in FIG. **1**B. That is, the layout of a mask pattern for forming the dummy hole only needs to be changed.

With the foregoing interconnection structure and the method for forming the structure according to the third embodiment, a highly-reliable multilevel interconnection structure which hardly causes malfunction even when held at high temperature is implemented. This is because of the following reasons. The dummy via **110**D is provided on the second interconnect **111** near the via **110**A, so that vacancies in a part of the conductive film (the Cu film **109**) constituting the second interconnect **111** are divided and respectively flow into the via **110**A and the dummy via **110**D. That is, the dummy via **110**D reduces the number of vacancies flowing into each via so that the stress gradient from the second interconnect **111** to the via **110**A is reduced. Accordingly, even when the interconnection structure is held at high temperature, flowing of vacancies from the second interconnect **111** into the via **110**A is suppressed. As a result, plastic deformation of a part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void inside the via hole **106**A, is suppressed, so that a highly-reliable multilevel interconnection structure which hardly causes malfunction even when held at high temperature is implemented.

In the third embodiment, the resultant multilevel interconnection structure is more reliable than that obtained in the first embodiment. This is because of the following reasons. In this embodiment, the diameter of the dummy hole **106**D (the dummy via **10**D) is smaller than that of the via hole **106**A (the via **110**A). In other words, the volume of the dummy via **110**D is smaller than that of the via **110**A. Accordingly, the stress gradient between the second interconnect **111** and the dummy via **110**D is steeper than that between the second interconnect **111** and the via **110**A, so that flowing of vacancies from the part of the conductive film (the Cu film **109**) constituting the second interconnect **111** into the dummy via **110**D precedes that into the via **110**A. This more effectively suppresses plastic deformation of the part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void in the via hole **106**A. As a result, the resultant multilevel interconnection structure is more reliable than that obtained in the first embodiment.

In addition, in the third embodiment, the dummy interconnect **102**B is provided under the dummy via **110**D (the dummy hole **106**D). Accordingly, the dummy hole **106**D is easily formed by etching the $SiO_2$ film **104** and the SiN film **103** with the dummy interconnect **102**B used as an etching stopper.

In the third embodiment, the space between the via **110**A and the dummy via **110**D (i.e., the space between the via hole **106**A and the dummy hole **106**D: hereinafter referred to as a via-to-dummy via space) is preferably as small as possible. To obtain the effect of reducing the number of vacancies flowing into the via **110**A by using the dummy via **110**D, the via-to-dummy via space is preferably 25 μm or less and is more preferably 1 μm or less. Then, part of vacancies which are to flow into the via **110**A flow into the dummy via **110**D. The minimum via-to-dummy via space can be set in accordance with the minimum isolation width (e.g., 0.2 μm) between interconnects or vias defined by the design rule, for example. If the minimum isolation width between interconnects is set substantially equal to the minimum interconnect width, the minimum via-to-dummy via space may be set in accordance with the minimum interconnect width.

In the third embodiment, the number of dummy vias **110**D provided for one via **110**A is preferably as large as possible. Specifically, it is preferable to provide dummy vias **110**D as many as possible on a part of the second interconnect **111** where the dummy vias **110**D do not affect circuit operation.

In addition, in the third embodiment, if the second interconnect **111** includes a wide interconnect portion having a width of, for example, about 10 μm and a narrow interconnect portion having a width of, for example, about 0.20 μm or less and branching off from the wide interconnect portion and if the via **110**A (the via hole **106**A) is connected to the narrow interconnect portion, one or more dummy vias **110**D (dummy holes **106**D) are preferably connected to the branch point between the wide interconnect portion and the narrow interconnect portion or to part of the wide interconnect portion near the branch point. Then, vacancies which are to enter the narrow interconnect portion from the wide interconnect portion and flow into the via **110**A are effectively captured in the dummy via **110**D. The dummy vias **110**D are not necessarily provided only at the branch point or its neighboring portions. For example, if a dummy via **110**D is located on the narrow interconnect portion relatively near the wide interconnect portion, most of vacancies which are to enter the via **110**A are captured in the dummy via **110**D before reaching the via **110**A. Accordingly, it is possible to prevent occurrence of a void in the via **110**A. As a result, the number of devices malfunctioning when held at high temperature is further reduced.

Moreover, in the third embodiment, instead of the dummy interconnect **102**B, the dummy via **110**D (the dummy hole **106**D) may be formed such that the bottom of the dummy via **110**D is located in the insulating film **101**. Then, the dummy hole **106**D is deeper than the via hole **106**A. This makes the stress gradient between the second interconnect **111** and the dummy via **110**D much steeper than that between the second

interconnect **111** and the via **110**A as compared to the first embodiment. Accordingly, flowing of vacancies from the part of the conductive film (the Cu film **109**) constituting the second interconnect **111** into the dummy via **110**D precedes that into the via **110**A. This more effectively suppresses plastic deformation of the part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void in the via hole **106**A. As a result, the reliability of the resultant multilevel interconnection structure is further enhanced.

## Embodiment 4

### A Case where a Via and a Dummy Via are Provided in the Same Layer

(Where the Shape of a Dummy Via is Changed)

Hereinafter, an interconnection structure and a method for forming the structure according to a fourth embodiment of the present invention will be described with reference to the drawings.

FIG. **9**A is a cross-sectional view showing the interconnection structure of the fourth embodiment. FIG. **9**B is a plan view showing the multilevel interconnection structure shown in FIG. **9**A when viewed from above. In FIGS. **9**A and **9**B, components already described in the first embodiment with reference to FIGS. **1**A through **1**C and **2**A through **2**C are denoted by the same reference numerals, and detailed description thereof will be omitted.

As shown in FIGS. **9**A and **9**B, the fourth embodiment is different from the first embodiment in the following ways. Instead of the dummy hole **106**B, a dummy trench **106**E which has a shape different from that of the dummy hole **106**B (i.e., the via hole **106**A), more specifically, which is longer than the via hole **106**A in a plan view, is provided. In addition, instead of the dummy via **110**B, a dummy portion **110**E is provided in the dummy trench **106**E. The dummy trench **106**E (the dummy portion **110**E) is rectangular, for example, in the plan view. The length (i.e., the longer sides) of the dummy portion **110**E and the width (i.e., the shorter sides) of a second interconnect **111** are provided along the same direction in the plan view. The dummy portion **110**E is connected to the second interconnect **111** near a via **110**A (the via hole **106**A). The dummy portion **110**E is closer to the center of the second interconnect **111** than the via **110**A is. In other words, the distance between the via **110**A and the end of the second interconnect **111** opposite the via **110**A with respect to the dummy portion **110**E is longer than the distance between the via **110**A and the other end of the second interconnect **111**, i.e., the end of the second interconnect **111** toward the via **110**A.

As shown in FIG. **9**A, neither the dummy interconnect **102**B nor the dummy portion **110**E constitutes a closed circuit in actual use. In other words, even if the dummy portion **110**E is omitted in the interconnection structure shown in FIG. **9**A, a device with this interconnection structure is operable at least immediately after fabrication.

In addition, in this embodiment, the width of each of a first interconnect **102**A and a dummy interconnect **102**B is smaller than that of the second interconnect **111**, as shown in FIG. **9**B. Specifically, the width of each of the first interconnect **102**A and the dummy interconnect **102**B is, for example, 0.2 μm, the diameter of the via **110**A (the via hole **106**A) is, for example, 0.20 μm, the length and width of the rectangular dummy portion **110**E (the dummy trench **106**E) are, for example, 0.8 μm and 0.20 μm, respectively, and the width of the second interconnect **111** is, for example, 10 μm. The space between the via **110**A and the dummy portion **110**E, more specifically, the space between the edge of the via **110**A toward the dummy portion **110**E and the edge of the dummy portion **110**E toward the via **110**A is 0.2 μm, for example.

A method for forming the multilevel interconnection structure shown in FIG. **9**A according to the fourth embodiment is different from that of the first embodiment (shown in FIGS. **1**A through **1**C, **2**A and **2**B) only in that the dummy trench **106**E reaching the dummy interconnect **102**B and having a rectangular shape in a plan view is formed instead of the dummy hole **106**B in the process step shown in FIG. **1**B. That is, the layout of a mask pattern for forming the dummy hole only needs to be changed.

With the foregoing interconnection structure and the method for forming the structure according to the fourth embodiment, a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented. This is because of the following reasons. The dummy portion **110**E is provided on the second interconnect **111** near the via **110**A, so that vacancies in a part of a conductive film (a Cu film **109**) constituting the second interconnect **111** are divided and respectively flow into the via **110**A and the dummy portion **110**E. That is, the dummy portion **110**E reduces the number of vacancies flowing into each via so that the stress gradient from the second interconnect **111** to the via **110**A is reduced. Accordingly, even when the interconnection structure is held at high temperature, flowing of vacancies from the second interconnect **111** into the via **110**A is suppressed. As a result, plastic deformation of a part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void inside the via hole **106**A, is suppressed, so that a highly-reliable multilevel interconnection structure which hardly causes malfunction even when held at high temperature is implemented.

In the fourth embodiment, the resultant multilevel interconnection structure is more reliable than that obtained in the first embodiment. This is because of the following reasons. In this embodiment, the dummy trench **106**E (the dummy portion **110**E) is longer than the via hole **106**A (the via **110**A) in a plan view and the length of the dummy portion **110**E and the width of the second interconnect **111** are provided along the same direction in the plan view. Accordingly, vacancies which are present in a part of the conductive film (the Cu film **109**) constituting the second interconnect **111** opposite the via **110**A with respect to the dummy portion **110**E flow into the dummy portion **110**E, so that it is possible to prevent these vacancies from reaching the via **110**A. This more effectively suppresses plastic deformation of the part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void in the via hole **106**A. As a result, the resultant multilevel interconnection structure is more reliable than that obtained in the first embodiment.

In addition, in the fourth embodiment, the dummy portion **110**E is closer to the center of the second interconnect **111** than the via **110**A is. In other words, the distance between the via **110**A and the end of the second interconnect **111** opposite the via **110**A with respect to the dummy portion **110**E is longer than the distance between the via **110**A and the other end of the second interconnect **111**, i.e., the end of the second interconnect **111** toward the via **110**A. Accordingly, the following advantage is obtained. A first region in the second interconnect **111** between the via **110**A and the end of the second interconnect **111** toward the dummy portion **110**E is larger than a second region in the second interconnect **111** between the other end thereof and the via **110**A, so that the first region contains a larger number of vacancies than the second region. The dummy portion **110**E is provided on this

first region in the second interconnect **111**, and thus vacancies more effectively flow into the dummy portion **110**E. This more effectively suppresses plastic deformation of the part of the conductive film (the Cu film **109**) constituting the via **111**A, i.e., occurrence of a void in the via hole **106**A. As a result, the reliability of the resultant multilevel interconnection structure is further enhanced.

In addition, in the fourth embodiment, the dummy interconnect **102**B is provided under the dummy portion **110**E (the dummy trench **106**E). Accordingly, the dummy trench **106**E is easily formed by etching the $SiO_2$ film **104** and the SiN film **103** with the dummy interconnect **102**B used as an etching stopper.

In the fourth embodiment, the space between the via **110**A and the dummy portion **110**E (i.e., the space between the via hole **106**A and the dummy trench **106**E: hereinafter referred to as a via-to-dummy via space) is preferably as small as possible. To obtain the effect of reducing the number of vacancies flowing into the via **110**A by using the dummy portion **110**E, the via-to-dummy via space is preferably 25 μm or less and is more preferably 1 μm or less. Then, the effect of making part of vacancies which are to flow into the via **110**A flow into the dummy portion **110**E is ensured. The minimum via-to-dummy via space can be set in accordance with the minimum isolation width (e.g., 0.2 μm) between interconnects or vias defined by the design rule, for example. If the minimum isolation width between interconnects is set substantially equal to the minimum interconnect width, the minimum via-to-dummy via space may be set in accordance with the minimum interconnect width.

In the fourth embodiment, the number of dummy portions **110**E provided for one via **110**A is preferably as large as possible. Specifically, it is preferable to provide dummy portions **110**E as many as possible on a part of the second interconnect **111** where the dummy portions **110**E do not affect circuit operation.

In the fourth embodiment, the dummy interconnect **102**B is not necessarily provided, and the dummy portion **110**E (the dummy trench **106**E) may be formed instead such that the bottom thereof is located in the insulating film **101**.

In the fourth embodiment, the planar shape of the via hole **106**A (the via **110**A) different from that of the dummy trench **106**E (the dummy portion **11**E) is not limited specifically, and may be a circle or a square, for example.

## Modified Example of Embodiment 4

Hereinafter, an interconnection structure and a method for forming the structure according to a modified example of the fourth embodiment will be described with reference to the drawings.

FIG. **10** is a plan view showing the interconnection structure according to the modified example of the fourth embodiment.

As shown in FIG. **10**, this modified example is different from the fourth embodiment (see FIG. **9**B) in the following ways. First, the second interconnect **111** includes: a wide interconnect portion **111***a* having a width of 10 μm, for example; and a narrow interconnect portion **111***b* having a width of 0.20 μm, for example, and branching off from the wide interconnect portion **111***a*. Second, the via **110**A (the via hole **106**A) is connected to the narrow interconnect portion **111***b*. Third, the dummy portion **110**E (the dummy trench **106**E) is connected to the wide interconnect portion **111***a* near the branch point between the wide interconnect portion **111***a* and the narrow interconnect portion **111***b*. In a case where the narrow interconnect portion **111***b* extends from a longer side of the wide interconnect portion **111***a* as in this modified example, the length of the dummy portion **110**E and the length of the wide interconnect portion **111***a* are provided along the same direction in the plan view, as shown in FIG. **10**.

That is, the method for forming the interconnection structure according to this modified example is different from that of the fourth embodiment in that in the process step shown in FIG. **1**B, the interconnect trench **107** divided into a first trench with a relatively large width and a second trench with a relatively small width is formed and the dummy trench **106**E is also formed near the branch point between the first trench and the second trench.

In this modified example, not only the advantages obtained by the fourth embodiment but also the following advantage is obtained. Vacancies which are to enter the narrow interconnect portion **111***b* from the wide interconnect portion **111***a* and flow into the via **110**A are effectively captured in the dummy portion **110**E. As a result, the number of devices malfunctioning when being held at high temperature is further reduced.

In addition, the advantage of this modified example obtained by using the dummy portion **110**E (i.e., suppression of malfunction after a device has been held at high temperature) is remarkable especially when the width of the narrow interconnect portion **111***b* is about 0.20 μm or less, as in the modified example of the first embodiment.

## Embodiment 5

### A Case where a Via and a Dummy Via are Provided in Different Layers

Hereinafter, an interconnection structure and a method for forming the structure according to a fifth embodiment of the present invention will be described with reference to the drawings.

FIG. **13**B is a cross-sectional view showing the interconnection structure of the fifth embodiment. FIG. **13**C is a plan view showing the multilevel interconnection structure shown in FIG. **13**B when viewed from above. In FIGS. **13**B and **13**C, components already described in the first embodiment with reference to FIGS. **1**A through **1**C and **2**A through **2**C or the second embodiment with reference to FIGS. **6**A through **6**C and **7**A through **7**C, for example, are denoted by the same reference numerals, and detailed description thereof will be omitted.

As shown in FIGS. **13**B and **13**C, a first interconnect **102**A is buried in an insulating film **101** formed on a semiconductor substrate (not shown), and a SiN film **103**, a $SiO_2$ film **104** and an FSG film **105** are formed in this order over the insulating film **101** and the first interconnect **102**A. A via hole **106**A is formed through the $SiO_2$ film **104** and the SiN film **103** to reach the first interconnect **102**A. An interconnect trench **107** is formed through the FSG film **105** to reach the via hole **106**A. A barrier film **108** and a Cu film **109** are buried in this order in the via hole **106**A and the interconnect trench **107**, thereby forming a via **100**A and a second interconnect **111** in the via hole **106**A and the interconnect trench **107**, respectively.

A SiN film **112**, a $SiO_2$ film **113** and an FSG film **114** are formed over the FSG film **105** and the second interconnect **111**. A dummy via hole (dummy hole) **115** is formed through the FSG film **114**, the $SiO_2$ film **113** and the SiN film **112** to reach the second interconnect **111**. A barrier film **116** and a Cu film **117** are buried in this order in the dummy hole **115**, thereby forming a dummy via **118** in the dummy hole **115**. The dummy via **118** is connected to the second interconnect

111 near the via 111A. A SiN film 119 is formed over the FSG film 114 and the dummy via 118.

As described above, this embodiment is greatly different from the first through fourth embodiments in that the dummy hole 115 (the dummy via 118) is not provided under the second interconnect 111 but is provided above the second interconnect 111.

As shown in FIG. 13B, the dummy via 118 does not constitute any closed circuit in actual use. In other words, even if the dummy via 118 is omitted in the interconnection structure shown in FIG. 13B, a device with this interconnection structure is operable at least immediately after fabrication.

In addition, as shown in FIG. 13C, in this embodiment, the first interconnect 102A has a width smaller than that of the second interconnect 111. Specifically, the width of the first interconnect 102A is, for example, 0.2 μm, the diameter of each of the via 110A (the via hole 106A) and the dummy via 118 (the dummy hole 115) is, for example, 0.20 μm, and the width of the second interconnect 111 is, for example, 10 μm. The space between the via 110A and the dummy via 118, more specifically, the space between the edge of the via 110A toward the dummy via 118 and the edge of the dummy via 118 toward the via 110A is 0.2 μm, for example.

FIGS. 11A through 11C, 12A through 12C and 13A are cross-sectional views showing respective process steps of a method for forming the multilevel interconnection structure shown in FIG. 13B according to the fifth embodiment.

First, as shown in FIG. 11A, an insulating film 101 is formed on the surface of a semiconductor substrate (not shown), and then a first interconnect 102A is formed in the insulating film 101.

Next, as shown in FIG. 11B, a SiN film 103, a $SiO_2$ film 104 and a FSG film 105 are formed in this order over the insulating film 101 and the first interconnect 102A by a plasma CVD process, for example. Thereafter, lithography and dry etching are alternately performed twice (i.e., lithography and dry etching are each performed twice), thereby forming a via hole 106A in the $SiO_2$ film 104 and the SiN film 103 to reach the first interconnect 102A and also forming an interconnect trench 107 in the FSG film 105 to reach the via hole 106A.

Then, as shown in FIG. 11C, a barrier film 108 is deposited by a PVD process, for example, to partly fill the via hole 106A and the interconnect trench 107. Then, a Cu film 109 is formed by a plating process, for example, on the barrier film 108 to completely fill the via hole 106A and the interconnect trench 107.

Thereafter, as shown in FIG. 12A, parts of the barrier film 108 and the Cu film 109 extending off the interconnect trench 107 are removed by a CMP process, for example. In this manner, a second interconnect 111 is formed in the interconnect trench 107. In addition, a via 110A is formed in the via hole 106A to connect the first interconnect 102A and the second interconnect 111 to each other.

Subsequently, as shown in FIG. 12B, a SiN film 112, a $SiO_2$ film 113 and an FSG film 114 are formed in this order by, for example, a plasma CVD process over the FSG film 105 and the second interconnect 111. Thereafter, lithography and dry etching are performed, and thereby a dummy hole 115 is formed through the FSG film 114, the $SiO_2$ film 113 and the SiN film 112 to reach the second interconnect 111.

Then, as shown in FIG. 12C, a barrier film 116 is formed by, for example, a PVD process to partly fill the dummy hole 115. Thereafter, a Cu film 117 is formed by, for example, a plating process on the barrier film 116 to completely fill the dummy hole 115.

Subsequently, as shown in FIG. 13A, parts of the barrier film 116 and the Cu film 117 extending off the dummy hole 115 are removed by, for example, a CMP process. In this manner, a dummy via 118 connected to the second interconnect 111 is formed in the dummy hole 115.

Lastly, a SiN film 119 is deposited over the FSG film 114 and the dummy via 118 (the Cu film 117), thus completing the multilevel interconnection structure shown in FIG. 13B.

With the foregoing interconnection structure and the method for forming the structure according to the fifth embodiment, a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented. This is because of the following reasons. The dummy via 118 is provided on the second interconnect 111 near the via 110A, so that vacancies in a part of the conductive film (the Cu film 109) constituting the second interconnect 111 are divided and respectively attracted to the via 110A and the dummy via 118. Specifically, in a portion of the second interconnect 111 connected to the dummy via 118, tensile stress on a part of the Cu film 109 constituting the second interconnect 111 is lower than that on its surrounding portions. Accordingly, vacancies inside the Cu film 109 are attracted to the dummy via 118, so that even when the interconnection structure is held at high temperature, flowing of vacancies from the second interconnect 111 into the via 110A is suppressed. As a result, plastic deformation of a part of the conductive film (the Cu film 109) constituting the via 110A, i.e., occurrence of a void inside the via hole 106A, is suppressed, so that a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented.

In the fifth embodiment, the space between the via 110A and the dummy via 118 (i.e., the space between the via hole 106A and the dummy hole 115: hereinafter referred to as a via-to-dummy via space) is preferably as small as possible. To obtain the effect of reducing the number of vacancies flowing into the via 110A by using the dummy via 118, the via-to-dummy via space is preferably 25 μm or less and is more preferably 1 μm or less. The minimum via-to-dummy via space can be set in accordance with the minimum isolation width (e.g., 0.2 μm) between interconnects or vias defined by the design rule, for example. If the minimum isolation width between interconnects is set substantially equal to the minimum interconnect width, the minimum via-to-dummy via space may be set in accordance with the minimum interconnect width.

In the fifth embodiment, the number of dummy vias 118 provided for one via 110A is preferably as large as possible. Specifically, it is preferable to provide dummy vias 118 as many as possible on a part of the second interconnect 111 where the dummy vias 118 do not affect circuit operation.

In the fifth embodiment, the top of the dummy via 118 is located in the insulating films. Alternatively, the top of the dummy via 118 may be connected to a dummy interconnect. In such a structure, after a hole for forming the dummy via 118 has been formed by etching, etching for forming a dummy interconnect trench is performed, thus ensuring removal of residues of the insulating film remaining on the bottom of the hole. Accordingly, connection of the dummy via 118 to the second interconnect 111 is ensured, resulting in that advantages of this embodiment are also obtained in this case.

In the fifth embodiment, if the diameter of the dummy via 118 (the dummy hole 115) is smaller than that of the via 110A (the via hole 106A), advantages similar to those of the third embodiment are obtained.

In addition, in the fifth embodiment, if the dummy via 118 is rectangular in a plan view and the length of this dummy via 118 and the width of the second interconnect 111 are provided

along the same direction in the plan view, advantages similar to those of the fourth embodiment are obtained. In such a case, the dummy via **118** is preferably closer to the center of the second interconnect **111** than the via **110**A is. In other words, if the distance between the via **110**A and the end of the second interconnect **111** opposite the via **110**A with respect to the dummy via **118** is longer than the distance between the via **110**A and the other end of the second interconnect **111**, i.e., the end of the second interconnect **111** toward the via **110**A, the foregoing advantages become more remarkable. In such a case, the planar shape of the via hole **106**A (the via **110**A) is not specifically limited, and may be a circle or a square, for example.

Embodiment 6

Insulating Slit **1**

Hereinafter, an interconnection structure and a method for forming the structure according to a sixth embodiment of the present invention will be described with reference to the drawings.

FIG. **15**B is a cross-sectional view showing the interconnection structure of the sixth embodiment. FIG. **15**C is a plan view showing the multilevel interconnection structure shown in FIG. **15**B when viewed from above. In FIGS. **15**B and **15**C, components already described in the first embodiment with reference to FIGS. **1**A through **1**C and **2**A through **2**C or the second embodiment with reference to FIGS. **6**A through **6**C and **7**A through **7**C, for example, are denoted by the same reference numerals, and detailed description thereof will be omitted.

As shown in FIGS. **15**B and **15**C, a first interconnect **102**A is buried in an insulating film **101** formed on a semiconductor substrate (not shown), and a SiN film **103**, a $SiO_2$ film **104** and an FSG film **105** are formed in this order over the insulating film **101** and the first interconnect **102**A. A via hole **106**A is formed through the $SiO_2$ film **104** and the SiN film **103** to reach the first interconnect **102**A. An interconnect trench **107** is formed through the FSG film **105** to reach the via hole **106**A. A barrier film **108** and a Cu film **109** are buried in this order in the via hole **106**A and the interconnect trench **107**, thereby forming a via **110**A and a second interconnect **111** in the via hole **106**A and the interconnect trench **107**, respectively.

A characteristic of this embodiment is that a pair of insulating slits **120** is provided in the second interconnect **111** to sandwich a portion of the second interconnect **111** connected to the via **110**A (a portion of the second interconnect **111** on the via **110**A.) In this embodiment, the insulating slits **120** are made of part of the FSG film **105** as an interlayer dielectric film. A SiN film **112** is formed over the FSG film **105** including the insulating slits **120** and the second interconnect **111**.

As shown in FIG. **15**C, in this embodiment, the first interconnect **102**A has a width smaller than that of the second interconnect **111**. Specifically, the width of the first interconnect **102**A is, for example, 0.2 μm, the diameter of the via **110**A (the via hole **106**A) is, for example, 0.20 μm, and the width of the second interconnect **111** is, for example, 10 μm. The shape of each of the insulating slits **120** is rectangular in a plan view, and the length of each of the insulating slits **120** is greater than or equal to twice and less than or equal to four times as large as the diameter of the via **110**A in the plan view. For example, the length and width of each of the insulating slits **120** in the plan view is 0.4 μm and 0.2 μm, respectively. In this embodiment, a longer side of each of the insulating slits **120** is in contact with the portion of the second interconnect **111** connected to the via **110**A.

FIGS. **14**A through **14**C and FIG. **15**A are cross-sectional views showing respective process steps of a method for forming the multilevel interconnection structure shown in FIG. **15**B according to the sixth embodiment.

First, as shown in FIG. **14**A, an insulating film **101** is formed on the surface of a semiconductor substrate (not shown), and then a first interconnect **102**A is formed in the insulating film **101**.

Next, as shown in FIG. **14**B, a SiN film **103**, a $SiO_2$ film **104** and a FSG film **105** are formed in this order over the insulating film **101** and the first interconnect **102**A by a plasma CVD process, for example. Thereafter, lithography and dry etching are alternately performed twice (i.e., lithography and dry etching are each performed twice), thereby forming a via hole **106**A in the $SiO_2$ film **104** and the SiN film **103** to reach the first interconnect **102**A and also forming an interconnect trench **107** in contact with the via hole **106**A in the FSG film **105**. In this embodiment, in forming the interconnect trench **107**, part of the FSG film **105** is left in the interconnect trench **107** to surround the via hole **106**A, thereby forming insulating slits **120**. Specifically, in a lithography process for forming the interconnect trench **107**, a resist pattern covering not only the part of the FSG film **105** except for a region where the interconnect trench **107** is to be formed but also a part of the FSG film **105** to be the insulating slits **120** is used. Then, the FSG film **105** is etched using the resist pattern as a mask.

Then, as shown in FIG. **14**C, a barrier film **108** is deposited by a PVD process, for example, to partly fill the via hole **106**A and the interconnect trench **107**. Then, a Cu film **109** is formed by a plating process, for example, on the barrier film **108** to completely fill the via hole **106**A and the interconnect trench **107**.

Thereafter, as shown in FIG. **15**A, parts of the barrier film **108** and the Cu film **109** extending off the interconnect trench **107** are removed by a CMP process, for example. In this manner, a second interconnect **111** is formed in the interconnect trench **107**. In addition, a via **110**A is formed in the via hole **106**A to connect the first interconnect **102**A and the second interconnect **111** to each other.

Lastly, a SiN film **112** is deposited over the FSG film **105** including the insulating slits **120** and the second interconnect **111** (the Cu film **109**), thus completing the multilevel interconnection structure shown in FIG. **15**B.

With the foregoing interconnection structure and the method for forming the structure according to the sixth embodiment, a highly-reliable multilevel interconnection structure which hardly causes malfunction even when held at high temperature is implemented. This is because of the following reasons. The insulating slits **120** are provided near a portion of the second interconnect **111** connected to the via **110**A. This portion of the second interconnect **111** will be also referred to as a via-connected portion. Specifically, the insulating slits **120** are provided in the second interconnect **111** to be in contact with the via-connected portion of the second interconnect **111**. Accordingly, tensile stress on a part of the second interconnect **111** near the via-connected portion is lower than that on the other part of the second interconnect **111**. The insulating slits **120** reduce the number of vacancies flowing into each via, so that the stress gradient from the second interconnect **111** to the via **110**A is reduced, so that even when the interconnection structure is held at high temperature, flowing of vacancies from the second interconnect **111** into the via **110**A is suppressed. In addition, the insulating slits **120** are made of a material different from that for the conductive film (the Cu film **109**) constituting the second

interconnect **111** and the via **110**A, so that the insulating slits **120** act as barriers against movement of atoms or vacancies in the conductive film. This prevents convection of atoms inside the second interconnect **111** and the via **110**A or accumulation of vacancies on the bottom of the via **110**A. As a result, plastic deformation of a part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void inside the via hole **106**A, is suppressed, so that a highly-reliable multilevel interconnection structure which hardly causes malfunction even when held at high temperature is implemented.

FIG. **16** is a graph for explaining effects of this embodiment. In FIG. **16**, the ordinate indicates "the number of devices malfunctioning after being held at high temperature" and the abscissa indicates "the presence of an insulating slit". The case of "with slit" corresponds to this embodiment and the case of "without slit" corresponds to a conventional example. As shown in FIG. **16**, in the case of "with insulating slit" in this embodiment, "the number of devices malfunctioning when being held at high temperature" is reduced to about one-eighth of that in the case of "without slit". This is because a slit made of an insulating film prevents a phenomenon in which atoms in a conductive film for interconnection move and vacancies in the conductive film gather in a via. Specifically, if a slit made of an insulating material different from a material for an interconnect is present in an conductive film for interconnection, this slit acts as a barrier against movement of atoms in the conductive film and also suppresses formation of a void resulting from gathering of vacancies from the conductive film in a via. Accordingly, in the case of "with insulating slit" in this embodiment, the number of devices malfunctioning when being held at high temperature" is reduced.

In addition, in the sixth embodiment, each of the insulating slits **120** is rectangular in a plan view. The length of each of the insulating slits **120** is greater than or equal to twice and less than or equal to four times as large as the diameter of the via **110**A in the plan view. A longer side of each of the respective insulating slits **120** in the plan view is in contact with a portion of the second interconnect **111** connected to the via **110**A. Accordingly, the foregoing advantages are ensured.

In the sixth embodiment, the shape and the number of the insulating slits **120** (the number of the insulating slits **120** provided for one via **110**A) are not specifically limited.

In the sixth embodiment, part of the FSG film **105** is used as the insulating slits **120**. Alternatively, other insulating materials may be used instead. The insulating slits **120** may be replaced with slits made of another conductive material different from a conductive material constituting the second interconnect **111** and the via **110**A.

Further, in the sixth embodiment, the insulating slits **120** are not necessarily in contact with the portion of the second interconnect **111** connected to the via **111**A. However, in a case where the insulating slits **120** and the via-connected portion of the second interconnect **111** are apart from each other, the space between each of the insulating slits **120** and the via-connected portion of the second interconnect **111**, i.e., the space between each of the insulating slits **120** and the via **110**A, is preferably 1 μm or less in order to ensure the foregoing advantages.

Furthermore, in the sixth embodiment, in a case where the second interconnect **111** includes: a wide interconnect portion having a width of about 10 μm, for example; and a narrow interconnect portion having a width of about 0.20 μm or less, for example, and branching off from the wide interconnect portion and if the via **110**A (the via hole **106**A) is connected to the narrow interconnect portion, one or more insulating slits **120** are preferably connected to the branch point between the wide interconnect portion and the narrow interconnect portion or a part of the wide interconnect portion near the branch point. Then, vacancies which are to enter the narrow interconnect portion from the wide interconnect portion and flow into the via **110**A are effectively captured in the insulating slits **120**. As a result, the number of devices malfunctioning when being held at high temperature is further reduced.

## Embodiment 7

### Insulating Slit **2**

Hereinafter, an interconnection structure and a method for forming the structure according to a seventh embodiment of the present invention will be described with reference to the drawings.

FIG. **17**A is a cross-sectional view showing the interconnection structure of the seventh embodiment. FIG. **17**B is a plan view showing the multilevel interconnection structure shown in FIG. **17**A when viewed from above. In FIGS. **17**A and **17**B, components already described in the first embodiment with reference to FIGS. **1**A through **1**C and **2**A through **2**C or the sixth embodiment with reference to FIGS. **14**A through **14**C and **15**A through **15**C, for example, are denoted by the same reference numerals, and detailed description thereof will be omitted.

As shown in FIGS. **17**A and **17**B, the seventh embodiment is different from the sixth embodiment in the following ways. Instead of the insulating slits **120** in contact with a portion of the second interconnect **111** connected to the via **110**A, an insulating slit **121** longer than the insulating slits **120** is provided in the second interconnect **111** near the via-connected portion of the second interconnect **111**. In other words, the insulating slit **121** of this embodiment is not in contact with the via-connected portion of the second interconnect **111**. Specifically, the insulating slit **121** is rectangular, for example, in a plan view and the length of the insulating slit **121** and the width of the second interconnect **111** are provided along the same direction in the plan view. The insulating slit **121** is provided in the second interconnect **111** near a portion of the second interconnect **111** connected to the via **110**A (the via hole **106**A) and is closer to the center of the second interconnect **111** than the via **110**A is. In other words, the distance between the via **110**A and the end of the second interconnect **111** opposite the via **110**A with respect to the insulating slit **121** is longer than the distance between the via **110**A and the other end of the second interconnect **111**, i.e., the end of the second interconnect **111** toward the via **110**A.

As shown in FIG. **17**B, in this embodiment, the first interconnect **102**A has a width smaller than that of the second interconnect **111**. Specifically, the width of the first interconnect **102**A is, for example, 0.2 μm, the diameter of the via **110**A (the via hole **106**A) is, for example, 0.20 μm, and the width of the second interconnect **111** is, for example, 10 μm. The length of the insulating slit **121** is greater than or equal to twice and less than or equal to ten times as large as the diameter of the via **110**A in a plan view. For example, the length and width of the insulating slit **121** in the plan view is 0.8 μm and 0.2 μm, respectively. The space between the via **110**A and the insulating slit **121**, more specifically, the space between the edge of the via **110**A toward the insulating slit **121** and the edge of the insulating slit **121** toward the via **110**A is 0.2 μm, for example.

A method for forming the multilevel interconnection structure shown in FIG. **17**A according to the seventh embodiment is different from that of the sixth embodiment (see FIGS. **14**A

through **14**C, **15**A and **15**B) in the following ways. In the process step shown in FIG. **14**B, more specifically, in forming the interconnect trench **107**, part of the FSG film **105** is left in the interconnect trench **107** to be slightly apart from the via hole **106**A, thereby forming the insulating slit **121** longer than the insulating slit **120**, instead of the insulating slit **120**. Specifically, in a lithography process for forming the interconnect trench **107**, the layout of a mask pattern for forming the insulating silt only needs to be changed.

With the foregoing interconnection structure and the method for forming the structure according to the seventh embodiment, a highly-reliable multilevel interconnection structure which does not cause malfunction even when held at high temperature is implemented. This is because of the following reasons. The insulating slit **121** is provided near a portion of the second interconnect **111** connected to the via **110**A, so that tensile stress on a portion near the via-connected portion of the second interconnect **111** is lower than that on the other part of the second interconnect **111**. The insulating slit **121** reduces the number of vacancies flowing into each via, so that the stress gradient from the second interconnect **111** to the via **110**A is reduced. Accordingly, even when the interconnection structure is held at high temperature, flowing of vacancies from the second interconnect **111** into the via **110**A is suppressed. In addition, the insulating slit **121** is made of a material different from that for the conductive film (the Cu film **109**) constituting the second interconnect **111** and the via **110**A, so that the insulating slit **121** acts as a barrier against movement of atoms or vacancies in the conductive film. This prevents convection of atoms inside the second interconnect **111** and the via **110**A or accumulation of vacancies on the bottom of the via **110**A. As a result, plastic deformation of a part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void inside the via hole **106**A, is suppressed, so that a highly-reliable multilevel interconnection structure which hardly causes malfunction even when held at high temperature is implemented.

In the seventh embodiment, the reliability of the multilevel interconnection structure is further enhanced because of the following reasons. In this embodiment, the insulating slit **121** is rectangular in a plan view and the length of the insulating slit **121** and the width of the second interconnect **111** are provided along the same direction in the plan view. The insulating slit **121** is located near the portion of the second interconnect **111** connected to the via **110**A. Accordingly, flowing of vacancies which are present in a part of the conductive film (the Cu film **109**) constituting the second interconnect **111** opposite the via **110**A with respect to the insulating slit **121** is blocked by the insulating slit **121**, so that these vacancies do not reach the via **110**A. In addition, in this embodiment, the insulating slit **121** is closer to the center of the second interconnect **111** than the via **10**A is. In other words, a first region in the second interconnect **111** between the via **110**A and the end of the second interconnect **111** opposite the via **110**A with respect to the insulating slit **121** is larger than a second region in the second interconnect **111** between the via **110**A and the other end of the second interconnect **111**, i.e., the end of the second interconnect **111** toward the via **110**A. Therefore, the first region contains a larger number of vacancies than the second region. In addition, the insulating slit **121** is provided in this first region, so that movement of vacancies is more effectively prevented. This more effectively suppresses plastic deformation of the part of the conductive film (the Cu film **109**) constituting the via **110**A, i.e., occurrence of a void in the via hole **106**A. As a result, the reliability of the resultant multilevel interconnection structure is further enhanced.

In the seventh embodiment, the space between the via **110**A (the via hole **106**A) and the insulating slit **121** is preferably as small as possible. To obtain the effect of reducing the number of vacancies flowing into the via **110**A by using the insulating slit **121**, this space is preferably 1 μm or less. The insulating slit **121** may be in contact with a portion of the second interconnect **111** connected to the via **110**A.

In the seventh embodiment, the shape and the number of the insulating slit **121** (the number of insulating slits **121** provided for one via **110**A) are not specifically limited.

In the seventh embodiment, part of the FSG film **105** is used as the insulating slit **121**. Alternatively, other insulating materials may be used. The insulating slit **121** may be replaced with a slit made of another conductive material different from a conductive material constituting the second interconnect **111** and the via **110**A.

Moreover, in the seventh embodiment, if the second interconnect **111** includes a wide interconnect portion having a width of, for example, about 10 μm and a narrow interconnect portion having a width of, for example, about 0.20 μm or less and branching off from the wide interconnect portion and if the via **110**A (the via hole **106**A) is connected to the narrow interconnect portion, the insulating slit **121** is preferably connected to the wide interconnect portion near the branch point between the wide interconnect portion and the narrow interconnect portion. In such a case, if the narrow interconnect portion extends from a longer side of the wide interconnect portion, the length of the insulating slit **121** and the length of the wide interconnect portion are provided along the same direction in the plan view. Then, vacancies which are to enter the narrow interconnect portion from the wide interconnect portion and flow into the via **110**A are effectively captured in the insulating slit **121**. As a result, the number of devices malfunctioning when held at high temperature is further reduced.

In the first through seventh embodiments, a $SiO_2$ film (e.g., the $SiO_2$ film **104**) and an FSG film (e.g., the FSG film **105**) are used as interlayer dielectric films between interconnects. However, the types of the interlayer dielectric films are not specifically limited.

In the first through seventh embodiments, a Cu film (e.g., the Cu film **109**) is used as an interconnect material. However, the type of the interconnect material is not specifically limited. A material for a barrier film (e.g., the barrier film **108**) is not specifically limited, either.

In the first through seventh embodiments, a SiN film (e.g., the SiN film **112**) is formed as a protective film over a damascene interconnect (e.g., the first interconnect **102**A or the second interconnect **111**). However, this SiN film may not be formed.

The dummy vias and the insulating slits of the first through seventh embodiments may be, of course, combined in various manners in order to achieve a technical idea of the present invention, "movement of vacancies in a conductive film for an interconnect is suppressed so that occurrence of a void in the interconnect after formation thereof is prevented."

What is claimed is:

**1**. A semiconductor device comprising:

a semiconductor substrate;

a first interconnect formed on the semiconductor substrate;

a first insulating film formed on the first interconnect;

a second interconnect formed on the first insulating film;

a via formed through the first insulating film and connecting between the first and second interconnects; and

a dummy via connected to the second interconnect,

wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough;

the second interconnect and the via form a dual damascene structure, and

the second interconnect and the dummy via from a dual damascene structure.

**2**. The semiconductor device of claim **1** further comprising a second insulating film formed on the semiconductor substrate,

wherein the first interconnect is formed on the second insulating film, and

the dummy via is connected to a first dummy interconnect formed on the second insulating film.

**3**. The semiconductor device of claim **2**, wherein the first dummy interconnect has a width smaller than that of the second interconnect.

**4**. The semiconductor device of claim **2**, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other.

**5**. The semiconductor device of claim **2**, wherein the dummy via is substantially circular in a plan view, and

a diameter of the dummy via is substantially equal to a width of the first dummy interconnect.

**6**. The semiconductor device of claim **2**, wherein a planar shape of the dummy via is substantially a square, and

a side of the dummy via is substantially equal to a width of the first dummy interconnect.

**7**. The semiconductor device of claim **2**, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film.

**8**. The semiconductor device of claim **2**, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle.

**9**. The semiconductor device of claim **2**, wherein the dummy via is substantially circular in a plan view, and

a diameter of the dummy via is smaller than a width of the first dummy interconnect.

**10**. The semiconductor device of claim **2**, wherein a planar shape of the dummy via is substantially a square, and

a side of the dummy via is smaller than a width of the first dummy interconnect.

**11**. The semiconductor device of claim **1**, wherein the first insulating film has a multilayer structure including a SiN film and a $SiO_2$ film.

**12**. The semiconductor device of claim **1**, wherein the second interconnect includes a first barrier film and a first conductive film.

**13**. The semiconductor device of claim **12**, wherein the first conductive film includes copper.

**14**. The semiconductor device of claim **1**, wherein each of the first and second interconnects is connected to another element or an external electrode.

**15**. The semiconductor device of claim **1**, wherein the first interconnect, the second interconnect and the via constitute part of a closed circuit, and

the dummy via does not constitute a closed circuit.

**16**. The semiconductor device of claim **1**, wherein the first interconnect has a width smaller than that of the second interconnect.

**17**. The semiconductor device of claim **1**, wherein the via and the dummy via are substantially circular in a plan view.

**18**. The semiconductor device of claim **17**, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other.

**19**. The semiconductor device of claim **1**, wherein a planar shape of each of the via and the dummy via is substantially a square.

**20**. The semiconductor device of claim **19**, wherein a length of a side of the via and a length of a side of the dummy via are substantially equal to each other.

**21**. The semiconductor device of claim **1**, wherein the first interconnect and the second interconnect extend in a same direction.

**22**. The semiconductor device of claim **1**, wherein the dummy via is provided on an extended line along which the first interconnect extends.

**23**. The semiconductor device of claim **1**, wherein the via is substantially circular in a plan view, and

a diameter of the via is substantially equal to a width of the first interconnect.

**24**. The semiconductor device of claim **1**, wherein a planar shape of the via is substantially a square, and

a side of the via is substantially equal to a width of the first interconnect.

**25**. The semiconductor device of claim **1**, wherein the via and the dummy via are spaced at a distance of 25 μm or less.

**26**. The semiconductor device of claim **1**, wherein the via and the dummy via are spaced at a distance of 1 μm or less.

**27**. The semiconductor device of claim **1**, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width.

**28**. The semiconductor device of claim **1**, wherein the dummy via is provided in plural.

**29**. The semiconductor device of claim **1**, wherein the via and the dummy via are substantially circular in a plan view, and

a diameter of the dummy via is smaller than a diameter of the via.

**30**. The semiconductor device of claim **1**, wherein a planar shape of each of the via and the dummy via is substantially a square, and

a side of the dummy via is smaller than a side of the via.

**31**. The semiconductor device of claim **1**, wherein the dummy via is substantially rectangular in a plan view, and

a longer side of the dummy via in a plan view and a shorter side of the second interconnect are provided along a same direction.

**32**. The semiconductor device of claim **1**, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect and shorter than a distance between the via and the other end of the second interconnect.

**33**. The semiconductor device of claim **1**, wherein the dummy via is connected to the upper surface of the second interconnect.

**34**. The semiconductor device of claim **33**, wherein the dummy via is formed in a third insulating film formed on the second interconnect.

**35**. The semiconductor device of claim **34**, wherein the third insulating film has a multilayer structure including a SiN film and a $SiO_2$ film.

**36**. The semiconductor device of claim **33**, wherein the dummy via includes a second barrier film and a second conductive film.

**37**. The semiconductor device of claim **36**, wherein the second conductive film includes copper.

**38**. The semiconductor device of claim **33**, wherein a second dummy interconnect is provided on the dummy via so as to come in contact with a top of the dummy via.

**39**. The semiconductor device of claim **1**, wherein the dummy via and the second interconnect are made of the same conductive film.

**40**. The semiconductor device of claim **1**, wherein the dummy via and the second interconnect include a Cu film.

**41**. The semiconductor device of claim **1**, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.

**42**. The semiconductor device of claim **1**, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film.

**43**. The semiconductor device of claim **1**, wherein a bottom of the dummy via is located deeper than a bottom of the via.

**44**. The semiconductor device of claim **1** further comprising a second insulating film formed on the semiconductor substrate,

wherein the first interconnect is formed on the second insulating film, and

a bottom of the dummy via is located in the second insulating film.

**45**. The semiconductor device of claim **1**, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and

the via is connected to the second interconnect portion.

**46**. The semiconductor device of claim **45**, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions.

**47**. The semiconductor device of claim **45**, wherein a width of the second interconnect portion is 0.2 μm or less.

**48**. The semiconductor device of claim **45**, wherein the dummy via is substantially rectangular in a plan view, and

a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction.

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