APPLIED PHYSICS REVIEWS—FOCUSED REVIEW

Recent advances on electromigration in very-large-scale-integration of interconnects

K. N. Tu
Department of Materials Science and Engineering, University of California, Los Angeles, Los Angeles, California 90095-1595

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Today, the price of building a factory to produce submicron size electronic devices on 300 mm Si wafers is over billions of dollars. In processing a 300 mm Si wafer, over half of the production cost comes from fabricating the very-large-scale-integration of the interconnect metallization. The most serious and persistent reliability problem in interconnect metallization is electromigration. In the past 40 years, the microelectronic industry has used Al as the on-chip conductor. Due to miniaturization, however, a better conductor is needed in terms of resistance–capacitance delay, electromigration resistance, and cost of production. The industry has turned to Cu as the on-chip conductor, so the question of electromigration in Cu metallization must be examined. On the basis of what we have learned from the use of Al in devices, we review here what is current with respect to electromigration in Cu. In addition, the system of interconnects on an advanced device includes flip chip solder joints, which now tend to become weak links in the system due to, surprisingly, electromigration. In this review, we compare the electromigration in Al, Cu, and solder on the basis of the ratio of their melting point to the device operating temperature of 100 °C. Accordingly, grain boundary diffusion, surface diffusion, and lattice diffusion dominate, respectively, the electromigration in Al, Cu, and solder. In turn, the effects of microstructure, solute, and stress on electromigration in Al, Cu, and solder are different. The stress induced by electromigration in Cu/low-k interconnects will be a very serious issue since the low-k dielectric (with a value of k around 2) tends to be weak mechanically. In a multilevel interconnect, a electromigration force due to current crowding, acting normal to current flow, has been proposed to explain why many electromigration induced damages occur away from the high current density region. In mean-time-to-failure analysis, the time taken to nucleate a void is found to be much longer than the growth of the void in Al and solder interconnects. This is not the case for Cu interconnects for the nucleation of a void on a surface. On accelerated tests of electromigration in Cu interconnects, the results gathered above 300 °C will be misleading since the mass transport will have a large contribution of grain boundary diffusion, which is irrelevant to electromigration failure in real devices induced by surface diffusion. © *2003 American Institute of Physics.*
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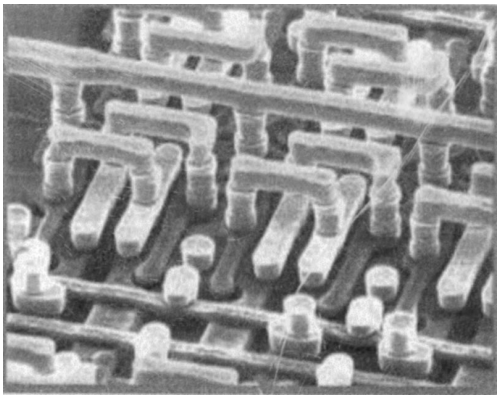

FIG. 1. SEM image of two-level Al(Cu) interconnect lines with W-plug vias on a Si surface. The image was taken after etching away the interlevel dielectric. The width of the line and the spacing between them is 0.5 μm (Ref. 10).

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I. INTRODUCTION

An ordinary household extension cord conducts electricity without mass transport because the electric current density in the cord is low, about 10^2 A/cm^2. The free-electron model of conductivity of metals assumes that the conduction electrons are free to move in the metal, unconstrained by the perfect lattice of ions except for scattering interactions due to phonon vibration. The scattering is the cause of electrical resistance and Joule heating. When an ion is out of its equilibrium position, for example, a diffusing atom at the activated state, it possesses a very large scattering cross section. Nevertheless, the scattering does not enhance displacement of the ion and it has no net effect on the diffusion of the ion when the electric current density is low. However, the scattering by a high current density, above 10^4 A/cm^2, enhances atomic displacement in the direction of electron flow. The enhanced atomic displacement and the accumulated effect of mass transport under the influence of electric field (mainly, electric current) are called electromigration. It is worth noting that a household cord is allowed to carry only a low current density, otherwise joule heating will burn the fuse. A thin film interconnect in a device can carry a much higher current density, which facilitates electromigration, because the Si substrates on which interconnects are built are very good heat conductors. On the other hand, in a device having a very dense integration of circuits, the heat management is a serious issue. Typically, a device is cooled by a fan or other means in order to maintain the operation temperature around 100 °C.

In very-large-scale-integration of circuits on a device, assuming an Al or Cu thin film line 0.5 μm wide and 0.2 μm thick carrying a current of 1 mA, for example, the current density will be 10^6 A/cm^2. Such current density can cause mass transport in the line at the device operation temperature of 100 °C and lead to void formation at the cathode and extrusion at the anode. These defects are the most persistent and serious reliability failures in thin film integrated circuits. As device miniaturization demands smaller and smaller interconnects, the current density goes up, so does the probability of circuit failure induced by electromigration. This is a subject which has demanded and attracted much attention.[1–7] In Ref. 7 a rather long list of literature (with titles) about experimental studies of electromigration in Al and Cu interconnects is given.

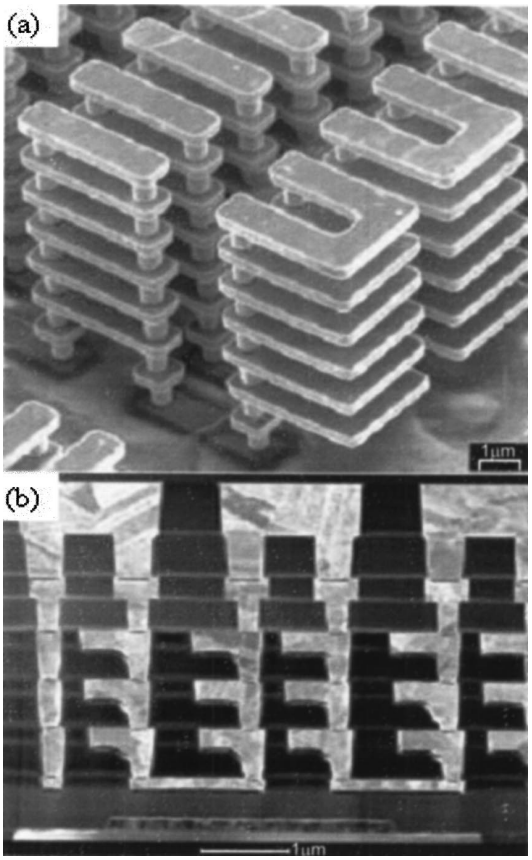

FIG. 2. (a) SEM image of an eight-level Cu interconnect structure taken after the interlevel dielectric was etched away. (Courtesy of Dr. Jeffrey Su, Institute of Microelectronics, Singapore. This image was suggested by Dr. Ahila Krishnamoorthy, Institute of Microelectronics, Singapore.) (b) Cross-sectional TEM image of a six-layered dual damascene Cu interconnect structure on a Si surface. The diameter of the narrowest Cu via is 0.25 μm. There is a liner between a via and the line below it. (Courtesy of Dr. L. C. Hsia, Chartered Semiconductor Manufacturing, Singapore.)

In the past 40 years, Al has been the interconnect conductor in the microelectronic industry. A small amount of Cu, 1–2 at. %, has been added to Al to improve its resistance to electromigration,[8] and the Al(Cu) interconnect has been used without serious reliability problems. Due to the trend of miniaturization, however, a better interconnect conductor than Al(Cu) is needed in terms of resistance–capacitance delay, electromigration resistance, and cost of fabrication. The industry has turned to Cu as the interconnect conductor, so the

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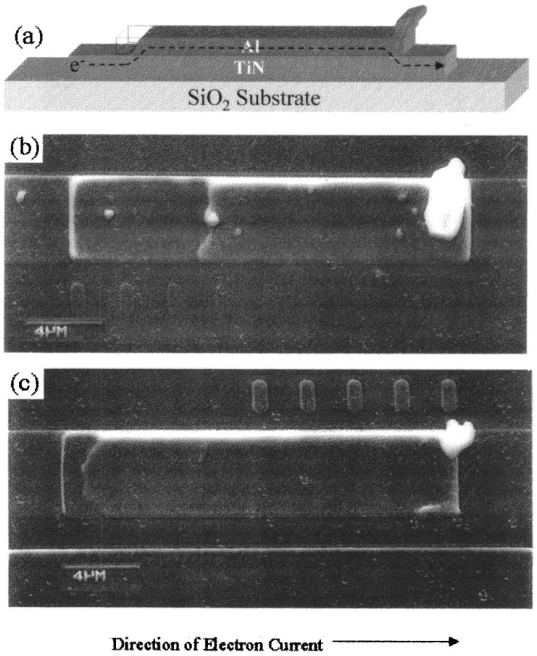

FIG. 3. (a) Schematic diagram of the Blech structure consisting a short Al strip on TiN base line for electromigration tests. A void at the cathode and a hillock at the anode are depicted. (b) SEM image of the top view of a Cu strip tested for 99 h at 350 °C with current density of 5×10^5 A/cm^2. (c) SEM image of the top view of a Cu(2 wt % Sn) strip tested at the same condition (Ref. 13).

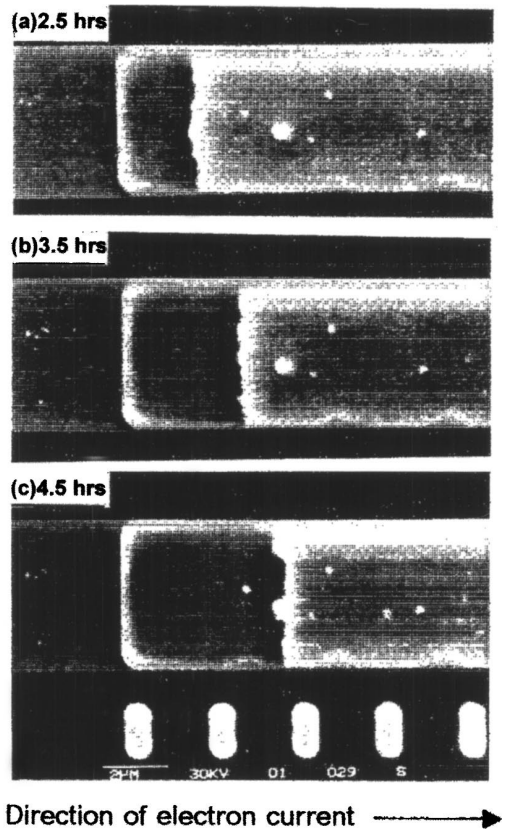

FIG. 4. (a) SEM image of mass depletion at cathode of a Cu strip at 2.5 h at 400 °C with current density of 2.1×10^6 A/cm^2, (b) at 3.5 h, and (c) at 4.5 h. The drift velocity is about 2 μm/h as measured from the three images (Ref. 13).

question of electromigration in Cu metallization must be examined. We shall review what have we learned from the previous studies and use of Al interconnect in devices. We ask what is current with respect to electromigration behavior in Cu interconnects. Since the system of interconnects in a device includes solder joints on one end that link to packaging circuits and also silicide contacts on the other end that link to active Si transistors, we should also examine electromigration in solder joints and silicide contacts. Because the geometry and eutectic compositions of solder joints are unique, electromigration in solder joints is different from that in Al and Cu. More importantly, it has become a reliability issue.[9] We shall examine it here, too. Electromigration in silicide contacts will not be reviewed.

Figure 1 shows a scanning electron microscopy (SEM) image of a two-level Al interconnect on a Si surface after the insulating dielectric has been etched away.[10] The width of the Al lines is 0.5 μm and the spacing between them is 0.5 μm, so the pitch is 1 μm. On 1 cm$\times$1 cm area, we can have 10^4 lines and each of them has a length of 1 cm, so the total length of interconnects in such a layer is 100 m. When we build six such layers on a chip of the size of our fingernail, the total length, if we include that of interlevel vias, is over 1 km. Figure 2(a) shows a SEM image of an eight-level Cu interconnect structure taken after the interlevel dielectric was etched away. Figure 2(b) shows a cross-sectional transmission electron microscopic (TEM) image of a six-level Cu interconnect structure built on a Si surface. There, the width of the narrowest interconnect via is 0.25 μm. It is worth mentioning that a factory that can build this kind of structure on a 200 or 300 mm wafer would cost over billions of dollars. More than half of the production cost in processing a wafer now is spent to make the interconnect metallization.

One of the important differences between the Al interconnect shown in Fig. 1 and the Cu interconnect shown in Fig. 2 is the vias between lines. In the Al interconnect, the via is a W plug, so there are interfaces between Al and W. But in the Cu interconnect, the via is Cu; typically, a via and the line above it are made in one step by electroplating using the dual damascene process, so there is no interface between them. On the other hand, there is an interface between a via and the line below it in the multilevel Cu interconnects. This is due to the use of the liner to improve the adhesion of Cu to the dielectric walls and the use of chemical–mechanical polishing to build the multilevel structure. In the three-dimensional structure, if electromigration induces an opening in any part of it, the device fails. We note that the three-dimensional interconnect turns up and down and also left and right. There is current crowding at a turn where electromigration is enhanced. We shall address the effect of current crowding on electromigration in Sec. V.

The phenomenon of electromigration can be observed from the response of a short Al or Cu strip on a base line of TiN as shown in Fig. 3(a). This structure is called the Blech structure for electromigration tests.[11,12] Figures 3(b) and 3(c) show, respectively, scanning electron microscope images of

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TABLE I. Melting point and diffusivities of Cu, Al, and eutectic SnPb.

	Melting point (K)	Temperature ratio 373 K/T m	Diffusivities at 100 °C (cm^2/s)	Diffusivities at 350 °C (cm^2/s)
Cu	1356	0.275	Lattice $D_l = 7\times10^{-28}$	$D_l = 5\times10^{-17}$
			Grain boundary $D_{gb} = 3\times10^{-15}$ Surface $D_s = 10^{-12}$	$D_{gb} = 1.2\times10^{-9}$ $D_s = 10^{-8}$
Al	933	0.4	Lattice $D_l = 1.5\times10^{-19}$	$D_l = 10^{-11}$
			Grain boundary $D_{gb} = 6\times10^{-11}$	$D_{gb} = 5\times10^{-7}$
Eutectic SnPb	456	0.82	Lattice $D_l = 2\times10^{-9} - 2\times10^{-10}$	Molten state $D_l > 10^{-5}$

the morphology of a Cu strip and an alloyed Cu strip with 2 wt% Sn in electromigration with current density of 5×10^5 A/cm^2 at 350 °C for 99 h.[13,14] At the cathode end of the strips, a depleted region can be seen, but at the anode end, an extrusion is seen. By conservation of mass, both depletion (void) and extrusion occurs in the same strip. These short strips were sandwiched between Ta thin films and were deposited and patterned on a long W base line which was deposited on an oxidized Si wafer. The applied electric current in the W line took a detour to go along the strip because the latter is a path of low resistance. When the current and temperature are high enough, atomic displacement occurs and void and extrusion formations can be observed directly. We can measure the rate of depletion at the cathode and calculate the drift velocity. Figure 4 is a set of SEM images of the depletion at the cathode of a Cu strip taken at different intervals at 400 °C with current density of 2.1×10^6 A/cm^2. The drift velocity is about 2 μm/h. It is important to note that the atomic displacement and mass transport are in the same direction as the electron flow.

Electromigration is the result of a combination of thermal and electrical effects on mass transport. If the conducting line is kept at a very low temperature (e.g., liquid nitrogen temperature), electromigration cannot occur because there is no atomic mobility. The contribution of thermal effects can be recognized by the fact that electromigration in a bulk metal such as a eutectic solder bump occurs at about three quarters of its melting point in absolute temperature, and electromigration in a polycrystalline Al thin film line occurs at less than one half of its melting point in absolute temperature. At these temperatures, there are atoms which undergo random walks in the bulk of the solder bump and in the grain boundaries of the Al thin film line, respectively, and these are the atoms which take part in electromigration under the applied field. It is interesting to note that when the width of a thin film line is reduced to the submicron range, the grain size in the line is comparable to the line width. The grains then become bamboo like in morphology so a continuous grain boundary path of diffusion does not exist. When a Cu thin film line possesses a bamboo-like microstructure, electromigration takes place on the surface of the line at about one quarter of the melting point of Cu in absolute temperature. Indeed, we can assume the Si device operation temperature to be 100 °C, which is about three quarters of the melting point of solders, about slightly less than half of the melting point of Al, and about one quarter of the melting point of Cu. In this temperature scale, lattice diffusion, grain boundary diffusion, and surface diffusion occur predominantly at $\frac{3}{4}$, $\frac{1}{2}$, and $\frac{1}{4}$ of the absolute temperature of a metal, respectively.[15]

Table I lists the melting points and diffusivities which are relevant to the electromigration behaviors in Cu, Al, and eutectic SnPb. The diffusivities for Cu and Al were calculated on the basis of the following equations from the master $\log D$ vs T_m/T plot for face-centered-cubic metals, see Fig. 15 in Ref. 16:

$$D_l = 0.5\exp(-34T_m/RT),$$
$$D_{gb} = 0.3\exp(-17.8T_m/RT), \quad (1)$$
$$D_s = 0.014\exp(-13T_m/RT),$$

where D_l, D_{gb}, and D_s are, respectively, lattice diffusivity, grain boundary diffusivity, and surface diffusivity.[16,17] T_m is the melting point, and the units of 34, 17.8, and 13 T_m are in cal/mol. As shown in Table I, at 100 °C the lattice diffusivity of Cu and Al is insignificantly small, and the grain boundary diffusivity of Cu is three orders of magnitude smaller than the surface diffusivity of Cu. At 350 °C the difference between surface and grain boundary diffusivity of Cu is much less, indicating that we cannot ignore the latter. The lattice diffusivity of eutectic SnPb (not a face-centered-cubic metal) at 100 °C given in Table I is an average value of tracer diffusivity of Pb and Sn in the alloy.[18] It depends strongly on the lamellar microstructure of the eutectic sample. Since a solder joint has, typically, a few large grains, the smaller diffusivity is better for our consideration. The surface diffusivity of Cu, grain boundary diffusivity of Al, and lattice diffusivity of the solder are actually rather close at 100 °C. To compare atomic fluxes transported by these three kinds of diffusion in a metal, we should have multiplied the diffusivity by their corresponding cross-sectional area of path of diffusion. But the outcome is the same.

In face-centered-cubic metals such as Al and Cu, atomic diffusion is mediated by vacancies. A flux of Al atoms driven by electromigration to the anode, requires a flux of vacancies to the cathode in the opposite direction. If we can stop the vacancy flux, we stop electromigration. To maintain a va-

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cancy flux we must supply vacancies continuously. Hence, we can stop a vacancy flux by removing the sources or supplies of vacancies. Within a metal interconnect, dislocations and grain boundaries are sources of vacancies, but the free surface is generally the most important and effective source of vacancies. For Al, its native oxide is protective, which means that the interface between the metal and its oxide is not a good source or sink of vacancies. This is also true for Sn. It is known that an anodized Al line has a better electromigration resistance than those that are not anodized.

If the atomic or vacancy flux is continuous in the interconnect, i.e., the anode can supply vacancies and the cathode can accept them continuously, and if there is no flux divergence in between, there will be no electromigration induced damage such as void and extrusion formation. In other words, without mass flux divergence no electromigration damage occurs in an interconnect when fluxes of atoms and vacancies can pass through it smoothly. Hence, atomic or mass flux divergence is a necessary condition concerning electromigration failure in real devices. The most common mass flux divergences are the triple points of grain boundaries and interfaces between dissimilar materials.

In summary, electromigration involves atomic and electron fluxes. Their distribution in interconnects is the most important concern in electromigration damage. In a region where both distributions are uniform, there will be no electromigration damage. Concerning atomic or vacancy fluxes, the most important factor is the temperature scale shown in Table I. Atomic diffusion must be thermally activated. The second is the design and processing of the interconnect structure. For example, the difference in via structure between Al and Cu metallization is important. Nonuniform distribution or divergence occurs at microstructure irregularities such as grain boundary triple points and interphase interfaces in interconnects, and they are the sites of failure initiation. In Secs. II, III, and IV, the effect of microstructure, solute, and stress on electromigration in Al, Cu, and solder interconnects will be discussed, respectively. In Sec. VI, mean-time-to-failure analysis on the basis of void and hillock formation due to flux divergence will be discussed.

Concerning the electron flux, the current density must be high enough for electromigration to occur. Because transistors in devices are turned on by pulsed direct current, we consider only electromigration under direct current. A brief review of electromigration by pulsed direct current can be found in Ref. 4. While a uniform current distribution is expected in straight lines, nonuniform current distribution occurs at corners where a conducting line turns, at interfaces where conductivity changes, and also around voids or precipitates in a matrix. In Secs. IV A and V, the effect of current crowding on electromigration will be discussed.

Besides electrical forces due to the applied electric field, there are gradients of mechanical stress, chemical potential, and temperature acting on atomic diffusion in interconnects. How these forces act together is of interest. In Secs. II C, III C, and IV D, the interaction between electrical and mechanical forces will be reviewed. In Sec. IV C, the interaction between electrical and chemical forces will be discussed.

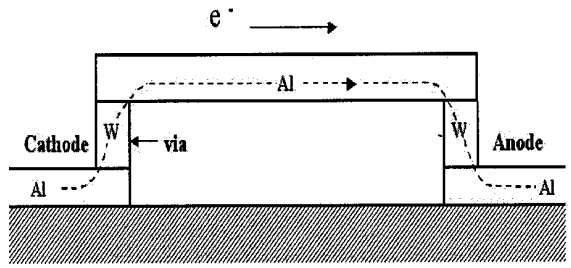

FIG. 5. Schematic diagram depicting a two-level Al interconnect with W vias. The broken curve arrow indicates the direction of electron flow. A void is expected to form above the W plug on the left-hand side or the cathode side.

II. ELECTROMIGRATION IN Al INTERCONNECTS

The microelectronic industry has used Al as the interconnect conductor for 40 years even though Cu is a better electrical conductor.[1–4] This is because Al has certain advantages in lithographic processing. It has good adhesion to the SiO_2 surface. It can be deposited by e-beam evaporation or sputtering, and it can be patterned by dry or reactive ion etching. It does not poison Si as Cu does, so Al can be deposited directly on Si to serve as contact metallization on Si devices. Electromigration damage in Al lines was discovered in the 1960s and was soon recognized to occur by grain boundary diffusion. The recognition has led to two major trends in the study of electromigration in Al; the effect of microstructure and the effect of solute.

A. Effect of microstructure on electromigration

The triple points of grain boundaries can serve as centers of atomic flux divergence. They lead to supersaturation of vacancies and become locations of void nucleation and growth near cathodes. Similarly, extrusions occur near anodes. Hence, the mechanism of void formation at a triple point and growth into an opening along a grain boundary were studied. Consequently, the processing of Al interconnects with a bamboo-type microstructure, containing no grain boundary triple points and no continuous grain boundary path, attracted much attention. Interestingly, it was soon recognized that when the linewidth becomes smaller than the grain size, the microstructure naturally becomes bamboo like. But it was also found to be very hard to fabricate a line having a perfect or 100% bamboo-type microstructure.

When a single level of Al interconnect was advanced to a multilevel Al interconnect, atomic flux divergence shifted from grain boundary triple points to the interface between an Al line and a W via. The interfacial divergence is due to the fact that atomic diffusivities in Al and W are very different. Figure 5 is a schematic diagram depicting a two-level Al interconnect with W vias. The curved arrow in Fig. 5 indicates the electron flow direction. Considering the W via in the left-hand side, we expect Al atoms to depart from the Al/W interface, so vacancies will accumulate above the interface and become supersaturated and eventually form a void. When the void grows as big as the via, it becomes an opening in the circuit. This phenomenon has been called the "wear-out" mode of failure. In actual devices having the

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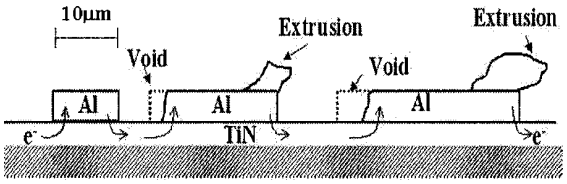

FIG. 6. Schematic diagram of a set of Al strips of different lengths patterned on a base line of TiN. The longer the length, the larger the depletion at the cathode. Below the critical length, there is no electromigration damage as depicted by the last one on the left-hand side.

multilevel structure of Al lines and W vias, the lifetime has been found to be reduced by a factor of 50 as compared to that of single level Al interconnects due to flux divergence at the interface. We shall reconsider this issue in Sec. V when we discuss current crowding at the Al/W interfaces.

B. Effect of solute on electromigration

Methods for reducing grain boundary diffusion in Al in order to improve its resistance to electromigration have stimulated much study, especially concerning the structure and atomic jump processes in grain boundaries. It is very difficult to specify the atomic positions in an arbitrary large angle grain boundary, even with the help of atomic resolution transmission electron microscopy and computer simulation. In turn, the activated configuration and activation energy of grain boundary diffusion cannot be defined. Therefore, an educated guess of grain boundary diffusion is based on our knowledge of lattice diffusion.[15,16]

In bulk alloys, certain solutes have the effect of retarding or enhancing solvent diffusion. For example, solute atoms of Cu in bulk Al are known to enhance the lattice diffusion of Al solvent atoms. This effect can be calculated on the basis of atomic jump frequencies around a pair of Cu–vacancy in an Al lattice. By this reasoning, of the use of alloying to retard grain boundary diffusion of Al, we would not choose Cu. However, when a small amount of Cu was co-deposited with Al, the co-deposited thin film sample actually showed much less electromigration.[8] Now, it is a general practice in industry to add 1 at. % or so of Cu to Al, and the lifetime improvement against electromigration can be orders of magnitude better than that of pure Al. The excess Cu forms Al_2Cu precipitates in Al grain boundaries. These precipitates dissolve and serve as sources of Cu to replenish the loss of Cu in grain boundaries when electromigration depletes them by driving them to the anode. Why Cu is capable of retarding grain boundary electromigration in Al has been a question of keen interest. Again, because of the difficulty in knowing the grain boundary structure precisely, no definitive answer has been given. Most likely, the answer is either a reduction of driving force or a reduction of kinetics or both. Kinetically, Cu may either reduce the concentration of vacancies in the grain boundary or increase the activation energy of grain boundary diffusion of Al. What is important to industrial manufacturing is the finding that the process of adding Cu to Al is forgiving, meaning that it tends to work well.

C. Effect of stress on electromigration and vice versa

The interconnect structure shown in Fig. 1 has many short segments. Electromigration in a short segment tends to induce back stress. This was first recognized by Blech and Herring using a set of short Al strips patterned on a base line of TiN as depicted in Fig. 6.[11,12] It was found that the longer the strip, the more the depletion at the cathode side in electromigration. Below a ''critical length,'' there was no observable depletion. The dependence of depletion on strip length was explained by the effect of back stress. In essence, when electromigration transports Al atoms in a strip from cathode to anode, the latter will be in compression and the former in tension. On the basis of the Nabarro–Herring model of equilibrium vacancy concentration in a stressed solid,[19] the tensile region has more and the compressive region has less vacancies than the unstressed region, so there is a vacancy concentration gradient decreasing from cathode to anode. The gradient induces an atomic flux of Al diffusing from anode to cathode, and it opposes the Al flux driven by electromigration from cathode to anode. The vacancy concentration gradient depends on the length of the strip; the shorter the strip, the greater the gradient. At a certain length defined as the critical length, the gradient is large enough to balance electromigration so no depletion at the cathode nor extrusion at the anode occurs.

In analyzing this stress effect, irreversible processes have been proposed by combining electrical and mechanical forces on atomic diffusion. The electrical force proposed by Huntington and Grone is taken to be[20]

$$F_{\mathrm{em}} = Z^* eE = (Z^*_{\mathrm{el}} + Z^*_{\mathrm{wd}})eE, \tag{2}$$

where e is the charge of an electron and E is the electric field ($E=\rho j$, and ρ is resistivity and j is current density). Z^*_{el} can be regarded as the nominal valence of the diffusing ion in the metal when the dynamic screening effect is ignored; it is responsible for the field effect and $Z^*_{\mathrm{el}}eE$ is called the direct force. Z^*_{wd} is the charge number representing the momentum exchange effect and $Z^*_{\mathrm{wd}}eE$ is called the electron wind force, and it is generally found to be of the order of 10 for a good conductor, so the electron wind force is much greater than the direct force for electromigration in metals. Z^* is the effective charge number of electromigration. For a discussion of the electrical force, see the review by Ho and Kwok,[4] and other papers.[21–25]

The mechanical force is taken as the gradient of chemical potential in a stressed solid,

$$F_{\mathrm{me}} = -\nabla\mu = -\frac{d\sigma\Omega}{dx}, \tag{3}$$

where σ is hydrostatic stress in the metal and Ω is atomic volume. Thus, we have a pair of phenomenological equations for atomic and electron fluxes,

$$J_{\mathrm{em}} = -C\frac{D}{kT}\frac{d\sigma\Omega}{dx} + C\frac{D}{kT}Z^* eE, \tag{4a}$$

$$J_e = -L_{21}\frac{d\sigma\Omega}{dx} + n\mu_e eE, \tag{4b}$$

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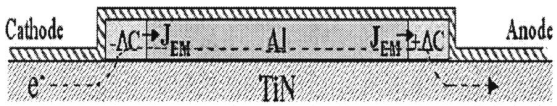

FIG. 7. Schematic diagram of a short strip confined by rigid walls. Compressive stress will build up at the anode as more and more atoms are being driven into the anode by electromigration.

where J_{em} is atomic flux in units of atoms/cm^2 s, and J_e is electron flux in units of coulomb/cm^2 s. C is the concentration of atoms per unit volume, and n is the concentration of conduction electrons per unit volume. D/kT is atomic mobility and μ_e is electron mobility. L_{21} is the phenomenological coefficient of irreversible processes and it contains the deformation potential.[26]

In Eq. (4a), if we assume $J_{em}=0$, i.e., there is no net electromigration flux or damage, we obtain the expression for the critical length as

$$\Delta x=\frac{\Delta\sigma\Omega}{Z^*eE}. \tag{5}$$

Since the resistance of the conductor can be taken to be constant at a constant temperature, we have, instead, the "critical product" or "threshold product" of "$j\Delta x$" by moving the current density from the right-hand to the left-hand side of the equation.

$$j\Delta x=\frac{\Delta\sigma\Omega}{Z^*e\rho}. \tag{6}$$

Under a constant applied current density, a bigger value of critical product in Eq. (6) means a longer critical length, in turn, a larger back stress in Eq. (5). For Al and Cu interconnects, we take $j=10^6$ A/cm^2 and $\Delta x=10\ \mu$m, we have a typical value of critical product about 1000 A/cm.

It has been proposed that if we can design interconnects in a device to have a product of $j\Delta x$ less than the critical product, we will have no electromigration. This might be practical for devices approaching the nanoscale, but it has not been widely explored except in certain test samples. We note that while the back stress in the above is induced by electromigration, the interaction between an applied stress and electromigration is the same; for example, an applied compressive stress at the anode will retard electromigration.

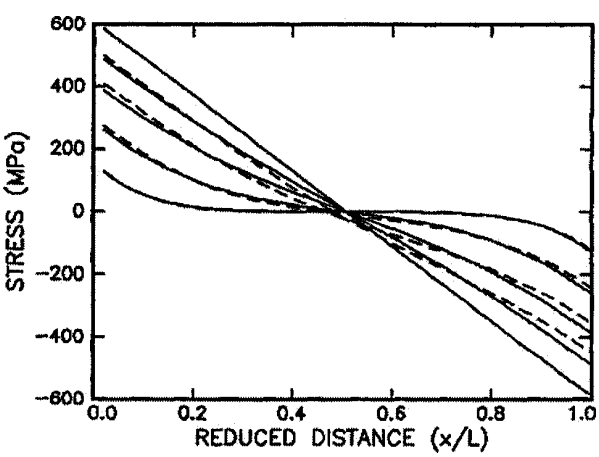

FIG. 8. Solutions for stress evolution in a finite line as a function of time under electromigration (Ref. 27).

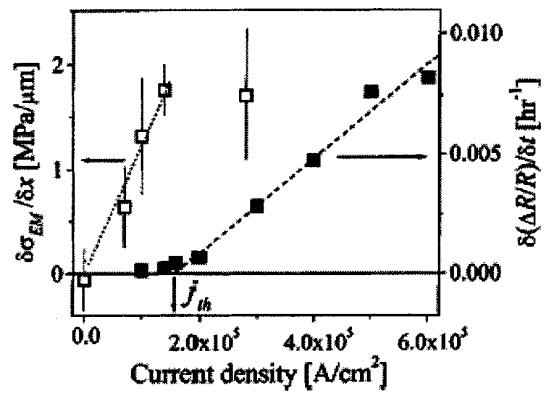

FIG. 9. Rate of resistance change of an Al line vs current density is shown by the solid squares. The electromigration induced steady-state compressive stress gradient vs current density is shown by the open squares (Ref. 29). (Courtesy of Professor. G. S. Cargill III, Lehigh University.)

The Blech structure has been used very often in experimental studies of electromigration for the following reasons. We can observe the damage directly and measure the drift velocity by measuring the rate of depletion at the cathode. Also, we can study the effect of back stress. Nevertheless, there has been a question about the nature of the back stress. If we confine a short strip by rigid walls as shown in Fig. 7, we can envisage easily the compressive stress at the anode induced by electromigration. Thus, we consider a fixed volume at the anode and we add atoms into it by electromigration, the stress change in the volume is

$$\Delta\sigma=-B\frac{\Delta C}{C}, \tag{7}$$

where B is the bulk modulus. And the time dependence of stress buildup in a short strip by electromigration can be obtained by solving the continuity equation since stress is energy density and a density function obeys the continuity equation,[27,28]

$$\frac{C}{B}\frac{\partial\sigma}{\partial t}=-\frac{D}{kT}\frac{\partial^2\sigma}{\partial x^2}-\frac{D}{BkT}\left(\frac{\partial\sigma}{\partial x}\right)^2-\frac{CDZ^*eE}{BkT}\frac{\partial\sigma}{\partial x}. \tag{8}$$

The solution for a finite line and the manner of stress buildup as a function of time is shown in Fig. 8. Clearly, in the beginning of electromigration the back stress is nonlinear along the length of the strip; the curved lines. In reality, the buildup is asymmetrical since the hydrostatic tensile stress at the cathode can hardly be developed.

In a fixed volume with a rigid wall, the compressive stress increases with the addition of atoms. However, in short strip experiments, there are no rigid walls to cover the Al strips, except native oxide. How can the back stress build up at the anode if the native oxide is not a rigid wall? One plausible explanation is that the Al native oxide has removed the source of vacancies from the surface, therefore, when electromigration drives atoms into the anode region, the outdiffusion of vacancies will reduce the vacancy concentration

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in the anode region if there is no source to replenish it. It is easy to envision the physical picture that under compression there is less equilibrium vacancies, but the reverse situation is not so easy to envision, i.e., when there is less equilibrium vacancies in a region, the region is in compression. We are not used to this latter concept. Furthermore, if we consider Au, which forms no oxide, and an unconfined Au strip with a clean surface, it is hard to imagine how a back stress can be developed in the strip under electromigration. This is because Au atoms can diffuse to the free surface at the anode to relieve the stress. It is equally hard to imagine the back stress in Cu short strips. Since Cu grows a nonprotective oxide, its surface can act as a source and sink for vacancies, although it may not be as active as a free surface in ultrahigh vacuum. More intriguingly, if electromigration in Cu interconnects occurs by surface diffusion, how surface diffusion can produce a back stress is unclear. We shall discuss this point later in Sec. III C.

A serious effort has been dedicated to measuring the back stress in Al strips during electromigration. It is not an easy task since the strip is thin and narrow; typically, it is only a few hundred nanometers thick and a few microns wide, so a very high intensity and focused x-ray beam is needed in order to determine the strain in Al grains by precision lattice parameter measurement.[29–35] Alternatively, a focused laser beam has been used to measure the Raman frequency shift from the Si underneath the Al line due to the piezospectroscopic property of Si.[36]

Microdiffraction x-ray beams using synchrotron radiation have been employed to study the back stress. White x rays of 10 μm$\times$10 μm beam from the National Synchrotron Light Source (NSLS) at National Brookhaven Laboratory were used to study electromigration induced stress distribution in pure Al lines.[29] The line was 200 μm long, 10 μm wide, and 0.5 μm thick with a 1.5 μm SiO_2 passivation layer on top, 10 nm Ti/60 nm TiN shunt layer at the bottom, and 0.2 μm thick W pads at both ends which connect the line to contact pads. The electromigration tests were performed at 260 °C. The results of the steady state rate of resistance increase, $\delta(\Delta R/R)/\delta t$, and the electromigration induced steady state compressive stress gradient, $\delta\sigma_{\mathrm{EM}}/\delta x$, versus current density are shown in Fig. 9. No electromigration occurred below the threshold current density "j_{th}" of 1.6 $\times 10^5$ A/cm^2. Below the threshold current density, the electromigration induced steady state stress gradient increased linearly with current density, wherein the electron wind force was counterbalanced by the mechanical force, so no electromigration drift was observed.

The x-ray microdiffraction apparatus at the Advanced Light Source (ALS) in Lawrence Berkeley National Laboratory is capable of delivering white x-ray beams (6–15 keV) focused to 0.8–1 μm by a pair of elliptically bent Kirkpatrick–Baez mirrors.[34,35] In the apparatus, the beam can be scanned over an area of 100 μm by 100 μm in steps of 1 μm. Since the diameter of the grains in the strip is about 1 μm, each grain can be treated as a single crystal with respect to the microbeam. Structural information such as stress/strain and orientation can be obtained by using white beam Laue diffraction. Laue patterns were collected with a large area (9×9 cm^2) charge-coupled-device detector with an exposure time of 1 s or longer, from which the orientation and strain tensor of each illuminated grain can be deduced and displayed by software. The resolution of the white beam Laue technique is 0.005% strain. In addition, a four-crystal monochromator can be inserted into the beam to produce monochromatic light for diffraction. The combined white and monochromatic beam diffractions are capable of determining the total strain–stress tensor in each grain. The technique and applications of scanning x-ray microdiffraction has been described by MacDowell *et al.*[34,35]

III. ELECTROMIGRATION IN Cu INTERCONNECTS

Although the Al(Cu) alloy has performed well as an interconnect conductor for a long time, the trend of miniaturization has recently demanded a change due to the following reasons.[37] First is the resistance–capacitance (RC) delay in signal transmission in fine lines. Second is the high cost of building a multilayered interconnect structure. Third is the concern of electromigration.[5–7,38–47] For the use of narrower and narrower lines, not only the line resistance increases, but also the capacitance between lines will drag down signal propagation. If we choose to maintain the dimensions of the Al interconnect without change, we must add more layers of Al, from six to eight or ten. To make more layers of metallization on Si is very undesirable because of cost. Moreover, if we have to add two more layers of interconnects, the additional processing steps can reduce yield. This is another reason why the dual-damascene processing of Cu is attractive. It has combined the steps of making one level of lines and one level of vias together, so most of the steps of making vias have been removed. Using the same number of processing steps, we can build more levels of Cu than Al interconnects.

Since Cu has a much higher melting point (1083 °C) than Al (660 °C), atomic diffusion should be much slower in Cu than Al at the same device operation temperature. So, electromigration is expected to be much less in Cu interconnects. Surprisingly, the benefit is not as big as expected. As we have stated in the beginning, electromigration in Cu occurs by surface diffusion which has a lower activation energy than grain boundary diffusion. Why has electromigration changed from grain boundary diffusion in Al to surface diffusion, on Cu? Ironically, this is because of the use of the damascene process to fabricate the Cu interconnect. In addition, it is because Cu intrinsically does not adhere to oxide surfaces. Why do we have to use damascene processes to produce Cu interconnects? This is because Cu cannot be etched or patterned by dry or reactive ion etching. Therefore, we have to form Cu lines by electrolytic plating of Cu into trenches in dielectric,[48] followed by a wet process of chemical–mechanical polishing (CMP) to planarize Cu with its surrounding dielectric. On the polished flat surface we repeat the process and build the multilevel Cu interconnect shown in Fig. 2. In the damascene process, via holes are etched together with trenches in the dielectric layer, followed by electroplating Cu into the trenches and via holes simultaneously. Compared to the process of making Al lines and

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W-plug vias, the dual damascene process has saved the step of making vias. In filling Cu into the trenches and via holes in the dielectric, we need to improve the adhesion of Cu to the dielectric, so a liner such as Ta, TaN, or TiN is used to cover the bottom and sidewalls of the trenches and holes before the electroplating of Cu.[7] To plate the Cu, a seeding layer of electroless Cu or vapor-phase deposited Cu is needed before the electrolytic plating.

Then, CMP is used to polish the top surface of Cu, which has no liner, and it is followed by the deposition of a dielectric layer so that the dual damascene process of building another interconnect layer of vias and lines can be repeated. Thus, CMP produces a top surface of Cu interconnect which does not adhere to the dielectric layer over it. Atomic diffusion on the top surface of the Cu interconnect becomes the ''built-in'' path for electromigration. Furthermore, the liner between a Cu via and the Cu line below it is an interface of flux divergence.[47] These are the two weak places for electromigration failure to occur. Which is the weaker one may depend on process control and it can lead to early failure, resulting in a bimodal distribution of failures. Nevertheless, the mechanism of how surface diffusion can lead to void formation in a via is intriguing. It may be that a certain amount of interfacial diffusion can occur between Cu and its liner. Then, the nucleation of a via–void could be thermal stress induced due to poor adhesion. Moreover, the third mode of failure is stress-induced extrusion at the anodes, resulting in dielectric delamination or fracture, especially for long interconnects with low-*k* dielectric insulation.

A. Effect of microstructure on electromigration

Because electromigration in Al interconnects takes place along grain boundaries, the effect of microstructure is a key issue. The knowledge leant from Al was applied to Cu interconnects with the intention to improve electromigration resistance, but with less success. For example, no significant difference in electromigration failure was found between polygranular and very long-grained bamboo Cu interconnects.[41] The microstructure of electrolytic Cu has the unusual property that it undergoes abnormal grain growth or recrystallization near room temperature. It has a strong [111] texture in the as-plated state, yet the abnormal grain growth has weakened the texture due to twin formation.[49] Why some of the grain boundaries in the electrolytic Cu have high mobility is unclear; it could be due to a minute amount of the organic and inorganic additives from the plating bath. Also, whether grain boundary diffusivity along these grain boundaries is the same as that given in Table I is of interest. Both grain size and impurity may affect electrical conductivity and good conductivity is the first requirement of interconnect metallization. So far, this is not an issue for electrolytic Cu. The minute amount of additives from the plating bath has little effect on the conductivity and the grain size is, typically, about 0.1 μm before grain growth.

The room temperature grain growth has led to a nonuniform distribution of large grains and clusters of small grains in the interconnect. The large grains are bamboo like and their grain boundaries to smaller grains have triple points. Hence, the microstructure is undesirable if electromigration is dominated by grain boundary diffusion. But, it becomes irrelevant when electromigration occurs by surface diffusion.[47] On a surface, the triple point is not an effective flux divergence point. The surface plane of the [111] oriented grains and their twins is of interest since it affects surface diffusion.

TABLE II. Conductivity of Al and Cu thin film interconnects.

Film	Resistivity ($\mu\Omega$ cm) at 20 °C
Sputtered Cu	2.1
Al (2 wt % Cu)	3.2
Cu (0.5 wt % Sn)	2.4
Cu (1 wt % Sn)	2.9

The microstructure of the seeding layer of electroless or vapor-phase deposited Cu is also interesting since its grain size is linearly proportional to its thickness. The grain growth during deposition is called flux-driven grain growth,[50] yet after deposition the grains do not grow at room temperature as those in the electrolytic Cu. Nevertheless, when electrolytic Cu is plated on the seeding layer, the microstructure of the latter is lost due to ripening. The interaction between these two types of Cu film is interesting, and it seems that the organic and inorganic additives in the electrolytic Cu might have diffused into the seeding layer to enhance its grain boundary mobility.

The divergence at Al/W interfaces is no longer an issue in Cu interconnects due to the dual damascene process. Nevertheless, the interface between a via and the line beneath it can still be an interfacial discontinuity due to the liner. Besides adhesion, the liner also serves as a diffusion barrier to prevent Cu from reaching Si. As a diffusion barrier, the thicker the better. A thick liner will increase the resistance of the interconnect, so actually, the thinner the better. While a cleaning of via holes is performed before depositing the liner, if the cleaning is not done properly, it affects the adhesion between a Cu via and the Cu line beneath it. Hence, besides being a flux divergence plane, the liner between a via and a line is of reliability concern due to poor adhesion under thermal stress.

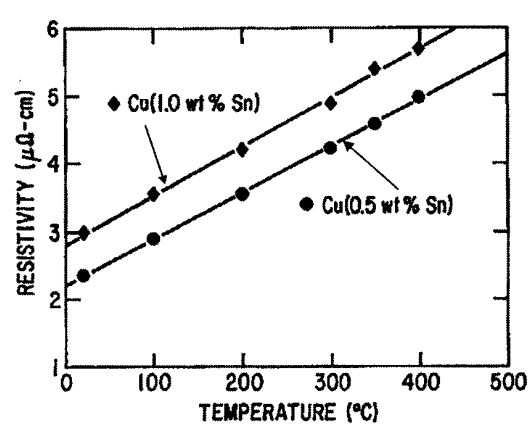

FIG. 10. Resistivity of Cu(0.5 wt % Sn) and Cu(1 wt % Sn) alloy thin films as a function of temperature (Ref. 13).

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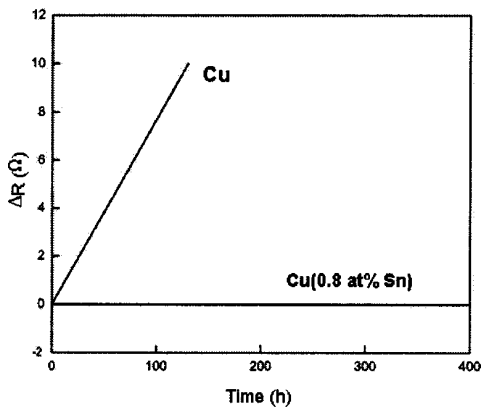

FIG. 11. Resistance change of Cu(0.8 at. % Sn) and pure Cu thin films in the electromigration test at 250 °C with current density of 10^6 A/cm^2 (Ref. 14).

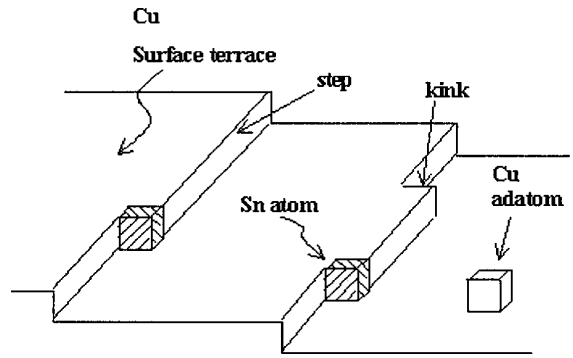

FIG. 13. Schematic diagram of surface steps and kinks on a Cu surface. The shaded atoms at the kinks are Sn atoms.

B. Effect of solute on electromigration

Since the solute effect of Cu is beneficial to electromigration resistance in Al, we ask if a similar solute effect can be found in Cu and what is the beneficial solute? Again, if we try to find a solute to slow down grain boundary diffusion of Cu, it is irrelevant as we really need a solute that can slow down surface diffusion of Cu. There is no guideline to find such a solute until we realize that electromigration in Cu interconnects is dominated by surface diffusion. To sustain a continuous surface atomic flux of Cu, we must be able to release Cu atoms from kink sites on surface steps continuously. In other words, the mechanism and energy needed to dissociate Cu atoms from kink sites, as in desorption and low temperature sublimation of atoms from a solid surface,[51,52] are important in the consideration of surface electromigration.

After adding and testing many elements in Cu, Sn was found to show a significant effect in resisting electromigration in Cu.[13,14] Table II compares the conductivity of Al and Cu interconnects. Figure 10 shows the resistivity of Cu (0.5 wt % Sn) and Cu (1.0 wt % Sn) alloys as a function of temperature using Van der Pauw test structures. Figure 11 shows the resistance change of Cu(Sn) and pure Cu thin films under electromigration at 250 °C and 10^6 A/cm^2. While the resistance of the Cu in testing changed quickly with time, the resistance of the Cu(Sn) remained unchanged. Figure 12 shows a comparison of the measured edge displacement versus time for 150-μm-long and 5-μm-wide Cu and Cu(Sn) test strips with a current density of 2.1×10^6 A/cm^2 at 300 °C. The slope of the edge displacement vs. time gives the average drift velocity for the Cu mass transport during electromigration. The average drift velocity of the Cu mass transport in the Cu(Sn) alloys strips is small at the beginning of testing, then it increases slowly with time, and eventually reaches a value comparable to that of pure Cu.

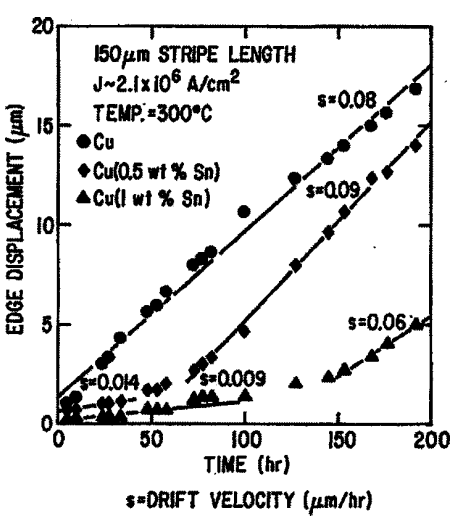

FIG. 12. Plots to show the comparison of edge displacements vs time for 150-μm-long strips of Cu and Cu(Sn) alloys at 300 °C with current density of 2.1×10^6 A/cm^2. The measured drift velocity "s" is given in the figure (Ref. 13).

Why Sn is beneficial in resisting electromigration in Cu is unclear. Since electromigration in Cu interconnects is known to occur by surface diffusion, it is likely that somehow surface diffusivity of Cu is slowed down by Sn, and more importantly, the supply of surface flux of Cu atoms is reduced, especially, if the dissociation of Cu atoms from the kinks on Cu surface steps is retarded due to a strong binding of Sn atoms to the kinks. Figure 13 is a schematic diagram of surface steps and kinks on a Cu surface. The shaded atoms at kinks represent Sn atoms. If we assume a strong binding there, the release of Cu atoms from the surface steps will be blocked. Moreover, when Sn segregates to Cu surfaces and forms an oxide bond with the top dielectric layer that improves the adhesion between the Cu and the top dielectric layer, it may further retard surface dissociation and diffusion of Cu.

The device operation temperature is around 100 °C, which is only about 0.275 of the absolute melting temperature of Cu. So, at 100 °C we can ignore both lattice and grain boundary diffusion in Cu. We may still be able to ignore both of them at a testing temperature of 250 °C. But at 350 °C, which is about 0.46 of the absolute melting temperature of Cu, we cannot ignore grain boundary diffusion in Cu. Hence, the finding that there is no electromigration in Cu(Sn) up to 250 °C (see Fig. 11), yet some has occurred at 350 °C (see Fig. 4), tends to indicate that while Sn may be effective in retarding surface diffusion of Cu, it is less effective in retard-

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ing grain boundary diffusion. More importantly, what is the proper temperature range for conducting an accelerated electromigration test for a Cu interconnect? On the basis of the fact that in devices the electromigration in Cu interconnects is dominated by surface diffusion, we may conduct the tests at 250 °C but not at 350 °C. The result at 350 °C is misleading since it may include grain boundary diffusion.

C. Effect of stress on electromigration and vice versa

The effect of applied compressive stress on electromigration in Cu is expected to be the same as that in Al; it retards electromigration at the anode. But, the effect of back stress on electromigration in Cu is unclear.[7] The first question is whether there is any back stress to be induced by electromigration in Cu strips at a temperature below 250 °C. If a Cu strip is not covered by a liner such as Ta, nor confined by rigid walls, it is hard to envision how back stress can be generated under electromigration by surface diffusion. This is because a free surface is the most effective source and sink of vacancies, so stress will be relaxed easily and will not build up. Hence, definitive experimental measurements on back stress in Cu interconnects will be needed.[13,43–46]

In devices, the Cu interconnect is embedded in an interlayer dielectric, so it is confined. Electromigration will induce extrusion or hillock formation at the anode end, even though the electromigration occurs by surface diffusion. The extrusion can deform the surrounding dielectric if it is soft, cause delamination if its adhesion is poor, or crack the dielectric if it is brittle. The effect of electromigration induced stress in Cu/low-*k* interconnects is unclear. This will be a serious reliability issue when a low dielectric constant insulation having a constant near or below 2 is integrated with Cu metallization. On the other hand, if the dielectric is rigid, electromigration can lead to plastic deformation of the confined strip.

IV. ELECTROMIGRATION IN FLIP CHIP SOLDER JOINTS

Flip chip technologies and flip chip solder joints have been discussed in a recent article,[53] so they will not be repeated here. However, we need to discuss why electromigration in flip chip solder joints is of concern. In today's circuit design, each solder joint will carry 0.2 A and it will be doubled in the near future. At present, the diameter of a solder joint is about 100 μm and it will be reduced to 50 μm soon. In the most advanced device today, there are already over 7000 solder joints on a chip. We can place 10 000 solder joints on a 1 cm$\times$1 cm chip if the diameter of the solder bumps and the spacing in between them is 50 μm. The average current density in such a 50 μm joint is about 10^4 A/cm^2 when a current of 0.2 A is applied. This current density is about two orders of magnitude smaller than that in Al and Cu interconnects. Electromigration does occur in flip chip solder joints at such a low current density and it occurs by lattice diffusion.[9,54,55] Often, it is explained by the low melting point or fast diffusion of solder. However, Table I shows that at device operation temperature of 100 °C, lattice diffusion in solder is not much faster than grain boundary diffusion in Al or surface diffusion of Cu from the point of view of electromigration. While the total atomic flux in lattice diffusion is much bigger, so is the volume of a void required to fail a solder joint. Therefore, a low melting point or fast diffusion is not the answer. Why electromigration occurs in flip chip solder joints at such low current densities will be explained below.

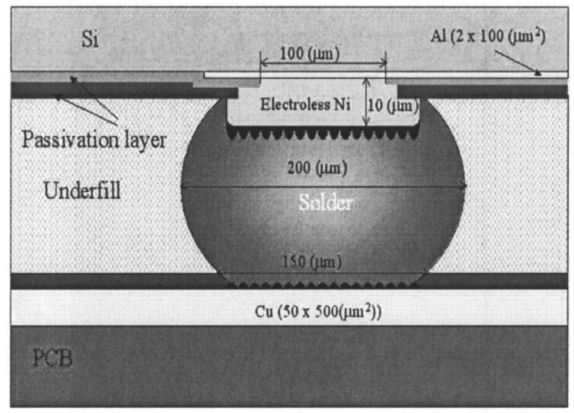

FIG. 14. Schematic diagram of a flip chip solder bump joining an interconnect line on the chip side (top) and a conducting trace on the board (bottom). The teeth-like structures depict the scallop-type intermetallic compounds formed between the solder and conducting metals.

We recall the critical product in Eq. (6). If we replace $\Delta\sigma$ by $Y\Delta\varepsilon$, where Y is Young's modulus and $\Delta\varepsilon = 0.2\%$ is the elastic limit, we see in Eq. (9) that the critical product is a function of Young's modulus, resistivity, and effective charge number of the interconnect material:

$$j\Delta x = \frac{Y\Delta\varepsilon\Omega}{Z^* e\rho}. \tag{9}$$

To compare the value of the critical product among Cu, Al, and eutectic SnPb, we note that eutectic SnPb has a resistivity that is one order of magnitude larger than those of Al and Cu. The Young's modulus of eutectic SnPb (30 Gpa) is a factor of 2–4 smaller that those of Al (69 Gpa) and Cu (110 Gpa).[56] The effective charge number of eutectic SnPb (Z^* of lattice diffusion)[2,57,58] is about one order of magnitude larger than those of Al (Z^* of grain boundary diffusion)[26] and Cu (Z^* of surface diffusion).[7,13] Therefore, in Eq. (9), if we keep Δx constant for comparison, we find that the current density needed to cause electromigration in eutectic SnPb solder is two orders of magnitude smaller than that needed for Al and Cu interconnects. This is the major reason why electromigration in flip chip solder joints can be serious.

Furthermore, due to the unique geometry of a flip chip joint, current crowding occurs at the contact interface between the solder bump and interconnect wire (to be discussed in the next section). The high current density due to current crowding is about one order of magnitude higher than the average current density in the joint. The low threshold of the current density needed to have electromigration in solder and the high current density due to current crowding are the key reasons why electromigration in flip chip solder

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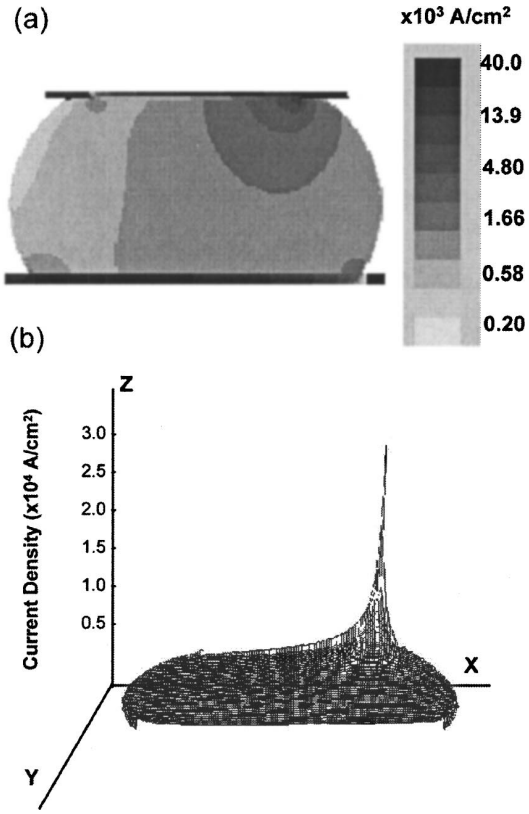

FIG. 15. (a) 2D simulation of current distribution in a solder joint. (b) Display of current density distribution in the cross section of a solder joint which is plotted on the $x-y$ plane and the intensity of the current density is plotted along the z axis (Ref. 59).

joints can compete with electromigration in Al and Cu interconnects as the major reliability problem in microelectronic devices.

In addition, owing to the eutectic composition of solder alloys and the thin film metallization used at the interfaces of a joint, the nature of electromigration in flip chip solder joints is very different from that in Al and Cu interconnects.[54–62] This will be discussed below.

A. Effect of current crowding on electromigration

Figure 14 is a schematic diagram depicting the geometry of a flip chip solder bump joining an interconnect line on the chip side (top) and a conducting trace on the board or module side (bottom).[55–60] Because the cross section of the line on the chip side is about two orders of magnitude smaller than that of the solder bump, there is a very large current density change at the contact between the bump and the line since the same current is passing between them. The change leads to current crowding at the entrance into the solder bump, so the current density there is about one order of magnitude higher than the average current density in the middle of the bump. It will be 10^5 A/cm^2 when the average current density in the bump is 10^4 A/cm^2. Figure 15(a) is a two-dimensional (2D) simulation of current distribution in a solder joint. Figure 15(b) is a display of current density distribution in the joint, where the cross section of the joint is plotted on the $x-y$ plane and the current density is plotted

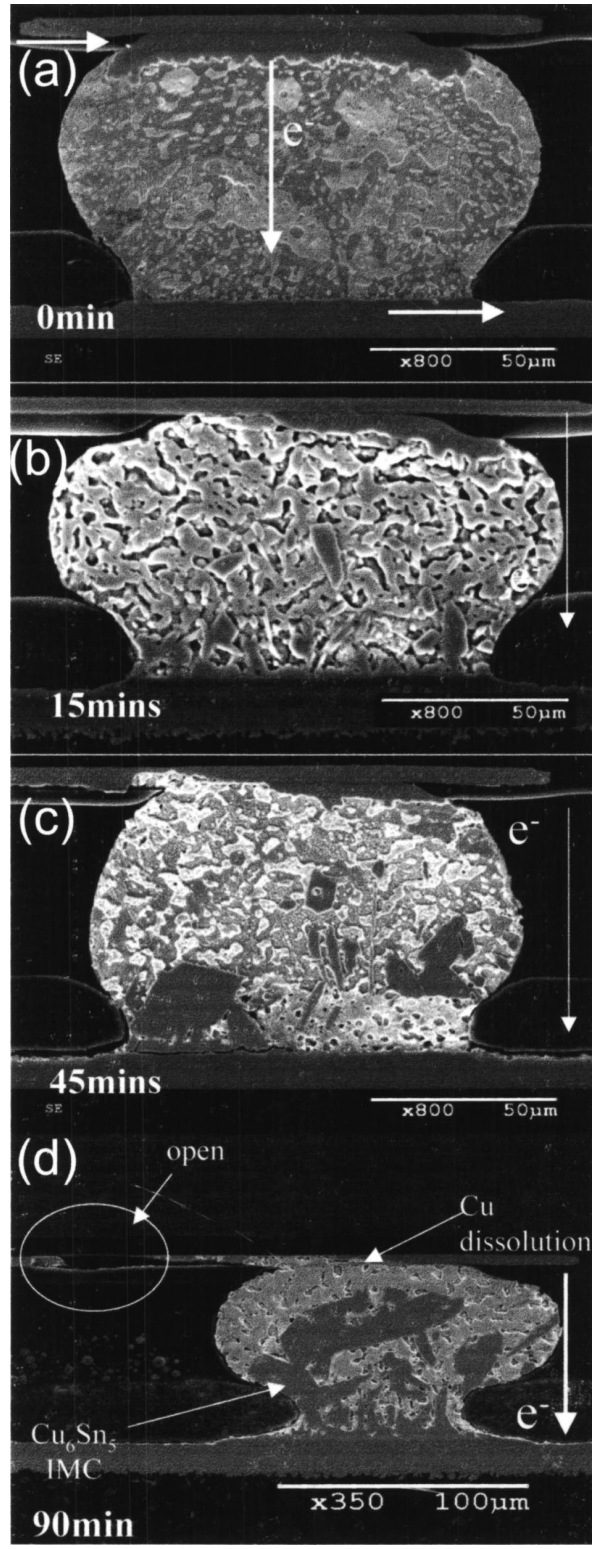

FIG. 16. Cross-sectional SEM images of asymmetrical dissolution of a thick Cu UBM due to current crowding by electromigration at 125 °C with an applied current of 1.2 A: (a) 0 min, (b) 15 min, (c) 45 min, and (d) 90 min. The electron current entered the bump from the upper-left corner. As the solder replaced the Cu at the upper-left corner, more and more intermetallic Cu_6Sn_5 formed inside the solder bump near the anode. (Courtesy of Professor C. R. Kao, National Central University, Taiwan.)

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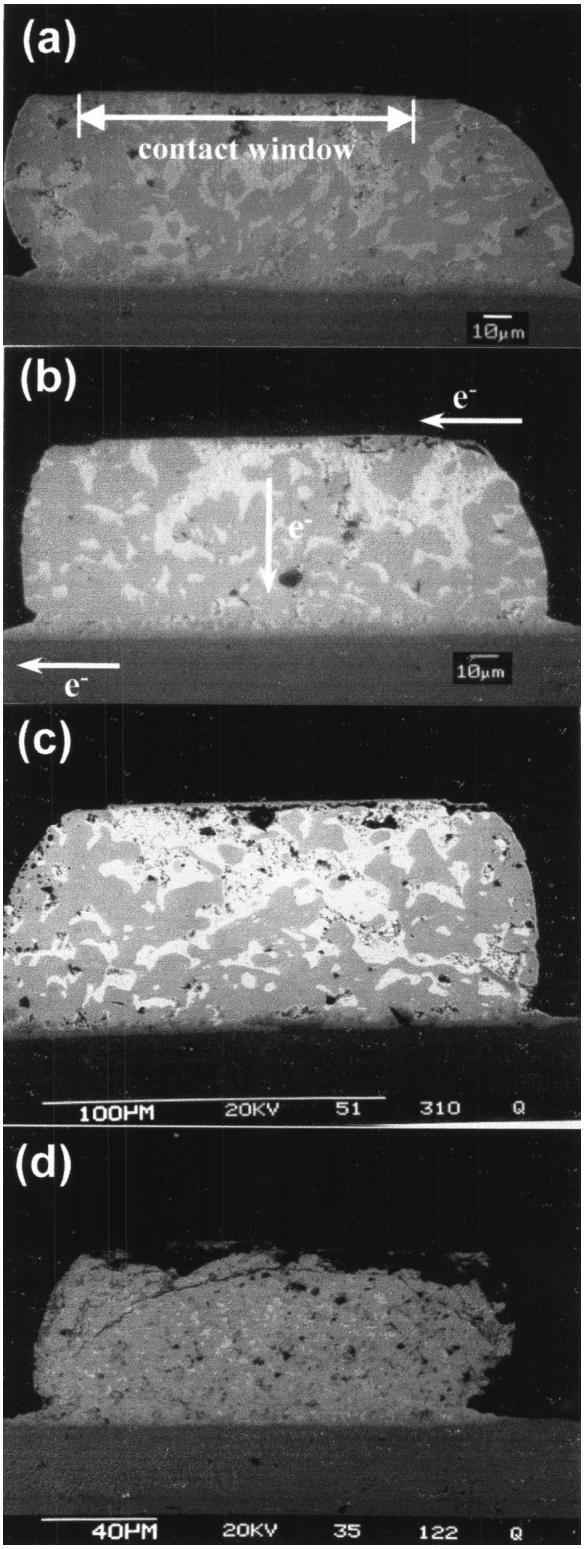

FIG. 17. Cross-sectional SEM images of electromigration failure of a flip chip solder joint due to void formation and propagation along the contact interface between the thin film Cu/Ni(V)/Al UBM and the eutectic SnPb solder bump: (a) 37 h, (b) 38 h, (c) 40 h, and (d) 43 h at 125 °C with current density of 2.25×10^4 A/cm^2 (Ref. 59).

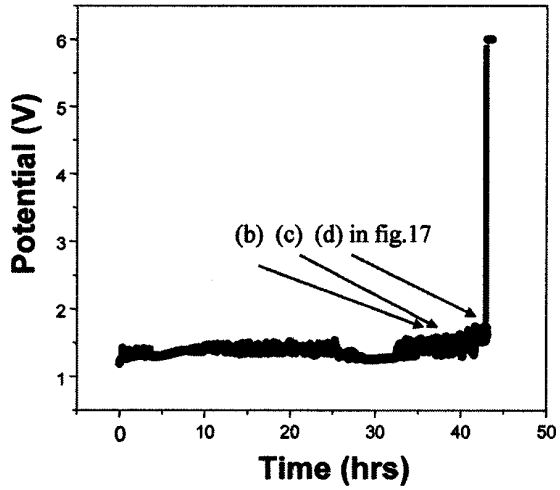

FIG. 18. Corresponding voltage vs time curve of the solder joint shown in Fig. 16 (Ref. 59).

along the z axis.[59,60] It is the current crowding or the high current density shown at the upper-right corner in Figs. 15(a) and 15(b) that leads to electromigration damage in the solder joint, not the average current density in the bulk of the joint. Consequently, electromigration damage occurs near the contact between the line and the bump.

Figure 16 displays a set of scanning electron microscopic images at several different stages of a flip chip solder joint in electromigration. Figure 16(a) shows the cross section of the joint before electromigration. A very thick Cu underbump metallization (UBM) is at the upper interface. The electron flow comes from the upper-left-hand interconnect and enters the bump at the upper-left corner. Figures 16(b), 16(c) and 16(d) are images of the cross section of the solder joint after 15, 45, and 90 min, respectively, powered at 1.25 A at 125 °C. The left-hand side of the Cu UBM disappeared gradually and was replaced by solder. Correspondingly, more and more Cu_6Sn_5 intermetallic compound was formed inside the solder bump. The asymmetrical dissolution of the Cu UBM is clearly due to the fact that the electron current entered the solder bump from the upper-left corner so current crowding occurred there. Why the Cu UBM can be

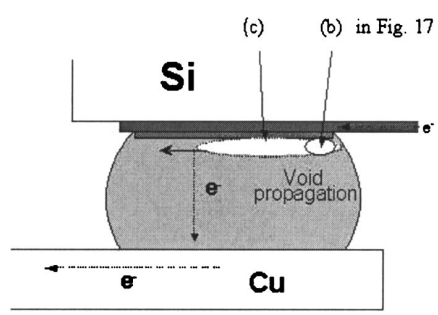

FIG. 19. Schematic diagram depicting the effect of void formation and propagation on the current entering the solder bump. While the current is being displaced to the front of the void, there is little change in resistance. Only when the void has propagated across the entire contact interface, the resistance will jump abruptly (Ref. 59).

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TABLE III. Electromigration test of solder joints vs Al and Cu interconnects.

	Al or Cu interconnects	Solder bumps
Cross section	$0.5\times 0.2\ \mu m^2$	$100\times 100\ \mu m^2$
Resistance	1–10 Ω	10^{-3} Ω
Current	10^{-3}A	1 A
Current density	10^6 A/cm^2	10^3–10^4 A/cm^2

TABLE IV. Intersititial Diffusion of noble and near-noble metals in Group IV elements.

Cu, Ag, Au, Ni, Pd, Pt .....↓..... Si, Ge, Sn, Pb	Interstitial Diffusion

dissolved and why a large amount of intermetallic compound can be formed in the solder joint will be discussed in Sec. IV B.

Figure 17 displays another set of SEM images of the damage in a flip chip solder joint caused by electromigration. The upper interface of the solder joint consisted of a set of thin films of Cu/Ni(V)/Al.[59] The total thickness of the thin film UBM is about 1 μm, hence, it is not resolved in the SEM image. Electrons of the applied current entered the bump from the upper-right corner of the joint. Up to 37 h at 125 °C with a current density of 2.25×10^4 A/cm^2, no damage was observed as shown in Fig. 17(a). Yet, after 38 and 40 h, voids are seen at the upper-right interface, and the voids propagated along the interface from right to left, shown in Figs. 17(b) and 17(c), respectively. After 43 h, the joint failed by having a large void across the entire interface, shown in Fig. 17(d). The corresponding curve of potential change versus time is shown in Fig. 18. In the curve, the potential change is insensitive to the void formation until the end, where it showed an abrupt jump when the void has extended across the entire interface. The arrows in Fig. 18 indicate the corresponding ''time'' when the images in Fig. 17 were taken. Why the potential or resistance change of the solder joint is insensitive to void formation and propagation can be explained by two reasons. The first is shown in Fig. 19, where a schematic diagram depicts the cross section of a solder joint with a void formation at the upper interface. The formation and propagation of the void displaced the current to the front of the void, so very little change in resistance is affected by the void formation. An abrupt change occurs only when the void has extended across the entire joint or when the contact becomes an opening. The second reason is given in Table III, where a comparison of the electrical behavior between the Al (or Cu) interconnect and solder joint is given. The resistance of a cubic piece of solder of 100 μm $\times$100 μm$\times$100 μm (the size of a solder joint) is about 1 mΩ. The resistivities of Sn and Pb are, respectively, 11 and 22 $\mu\Omega$ cm. The resistance of an Al or Cu line 100 μm long with a 1 μm$\times$0.2 μm cross section is about 10 Ω. So, the solder joint is a low resistance conductor, but the interconnect is a high resistance conductor. While the resistance of the latter is sensitive to a slight microstructure change, the former is not. Often, a solder joint may contain a huge spherical void due to residue flux in the solder paste, yet the void has little effect on the resistance of the solder joint.

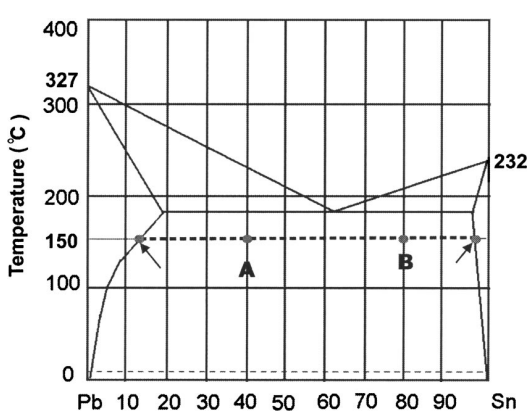

FIG. 20. Schematic binary eutectic phase diagram of Sn–Pb. Along the broken line at constant 150 °C, there is no chemical potential change as a function of composition. Hence, we can have phase separation along the broken line driven by electromigration.

B. Effect of eutectic composition on electromigration

A major advantage of flip chip technology is that thousands of solder joints or electrical leads can be formed simultaneously by low temperature heating in forming gas. Also, many joints can be placed near the center of a chip in order to avoid the voltage drop from a lead located at the edge of the chip. The technology does require that all the joints melt or solidify at the same temperature, so a eutectic alloy is favored as solder. However, a eutectic alloy has a unique property that at a constant pressure and temperature (below the eutectic temperature), it has a two-phase microstructure and there is no chemical potential gradient as a function of alloy composition. A schematic diagram of the binary phase diagram of Sn–Pb is depicted in Fig. 20 to illustrate the effect of eutectic composition. If we consider at ambient pressure and 150 °C, any composition along the broken line shown in Fig. 20 will decompose into the two end phases at the two points indicated by the arrows. These two phases are at equilibrium with each other, independent of the amount of each phase. Consider the two alloys at points ''A'' and ''B'' as shown in Fig. 20 to form a diffusion couple. Upon annealing at 150 °C, we find that there is no interdiffusion or no homogenization, except some ripening. Thus, if we subject a homogeneous (in average composition) two-phase eutectic alloy to electromigration, it becomes inhomogeneous by driving one of the phases to the anode and the other to the cathode. We can have phase separation and a large amount of up-hill diffusion and yet there exists no concentration gradient force to oppose it.[62] This eutectic effect is different from the classic Soret effect,[15] in which a homogeneous single phase alloy becomes inhomogeneous under a temperature gradient. The difference is not because a eutectic alloy is a two-phase alloy, rather that in the Soret effect, there is a chemical potential or composition gradient to resist the

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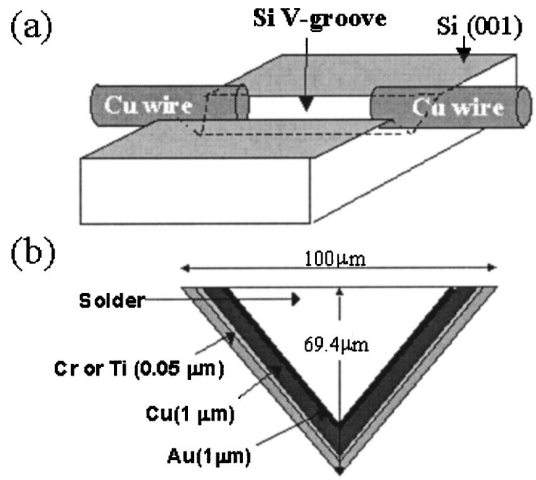

FIG. 21. Schematic diagram of (a) V groove along ⟨110⟩ direction on the Si(001) surface with two Cu wires at two ends, and (b) cross-section view of a V-groove solder sample (Ref. 57).

effect. But in a eutectic alloy, there is no chemical potential gradient to resist phase separation driven by electromigration or other forces.

If we examine the binary phase diagram of Sn–Cu or Sn–Ni, we find that Sn and Cu_6Sn_5 as well as Sn and Ni_3Sn_4 form eutectic couples. This means that below their eutectic temperature we can form a large amount of these compounds in a Sn matrix, and the compounds will be in equilibrium with the matrix. Indeed, this has been observed in electromigration in solder joints. Since both Cu and Ni are being used as UBM in solder joints, they can be dissolved by electromigration into the solder joint and form a large amount of intermetallic compounds (IMCs) near the anode, especially, the Pb-free solders which are Sn based. The dissolution rate is surprisingly fast due to the fact that noble and near-noble metals diffuse interstitially in group IV elements as shown in Table IV.[63,64] Electromigration of these metals in Sn and Pb are very fast.[65–68]

C. Polarity effect of electromigration on chemical reactions at cathodes and anodes in solder joints

Both noble and near-noble metals react with Sn to form IMCs at room temperature due to fast interstitial diffusion.[69] Since the IMCs formed at the solder joint interfaces are an integral part of the joint, they must be considered together with the solder bump in electromigration. Because of fast diffusion and rapid reaction, the chemical and electrical forces interact at these interfaces.[70] However, the interactions at the cathode and the anode are different due to the polarity effect. At the cathode, the electrons flow from the IMC to solder, but at the anode the flow direction is reversed. While electromigration enhances IMC formation at the anode, it enhances IMC dissolution at the cathode.

To investigate the polarity effect, we have designed test samples of V-groove solder lines with Cu electrodes at the two ends.[57,71,72] Figures 21(a) and 21(b) show schematic diagrams of a V-groove sample and its cross-sectional view,

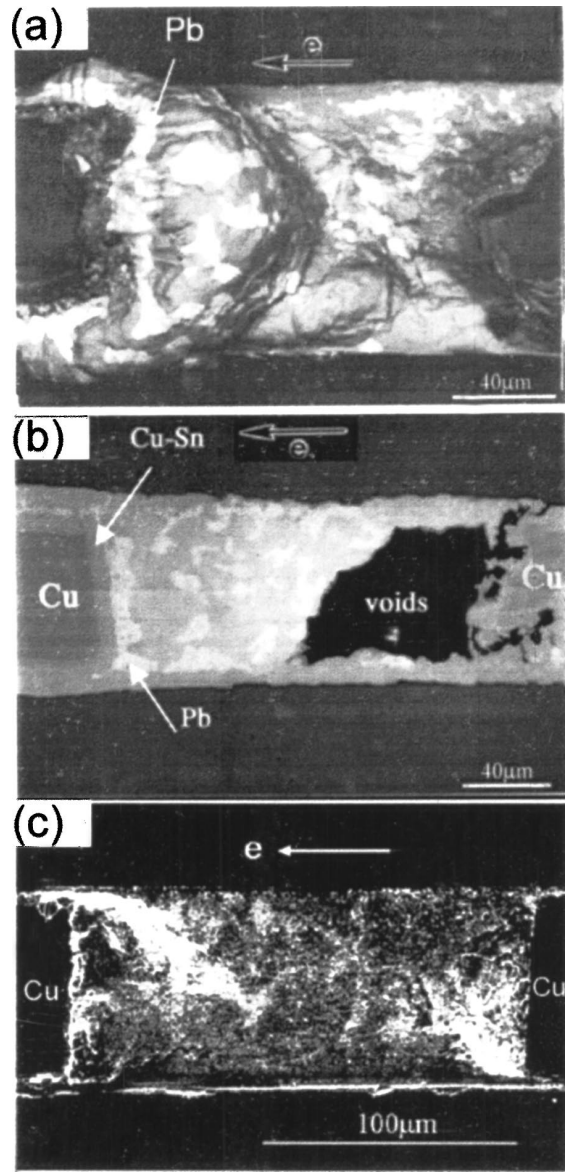

FIG. 22. SEM images of morphological changes on a eutectic SnPb solder line due to electromigration: (a) large lump formation at the anode after applying 2.8×10^4 A/cm^2 at 150 °C for 8 days; (b)void at the cathode in a top-down cross section of the sample shown in (a); and (c) a sample at room temperature with 5.7×10^4 A/cm^2 for 12 days (Refs. 57 and 62).

respectively. The V-shaped grooves with a width of 100 μm and a length along the [110] direction on a 4-in.-diam (001) silicon wafer were processed by standard lithography and etching techniques. Following wet oxidation of a thin SiO_2 layer of 0.1 μm, metal layers of 0.05 μm of Ti, 1 μm of Cu, and 0.05 μm of Au were deposited sequentially by e-beam evaporation. The wafer was cut into small pieces with a V-groove line in the middle. For each piece, two Cu wires were placed at the two ends of the V groove as electrodes, then eutectic SnPb and Pb-free solder of $SnAg_{3.8}Cu_{0.7}$ were regrown into the V groove between the two copper wires using mildly activated resin flux.

Electromigration in eutectic SnPb V-groove solder lines has been studied at 150 °C and room temperature.[57,62] At

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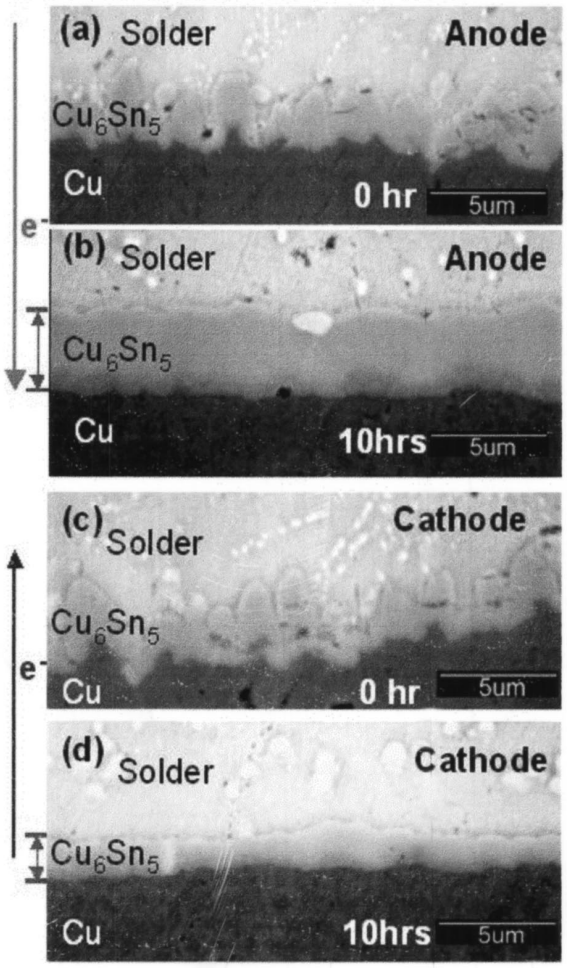

FIG. 23. SEM images of thickness change at the anode and cathode, after current stressing of (a) 0 h at the anode, (b) 10 h at the anode, (c) 0 h at the cathode, and (d) 10 h at the cathode with current density of 3.2×10^4 A/cm^2 at 180 °C (Refs. 71 and 72).

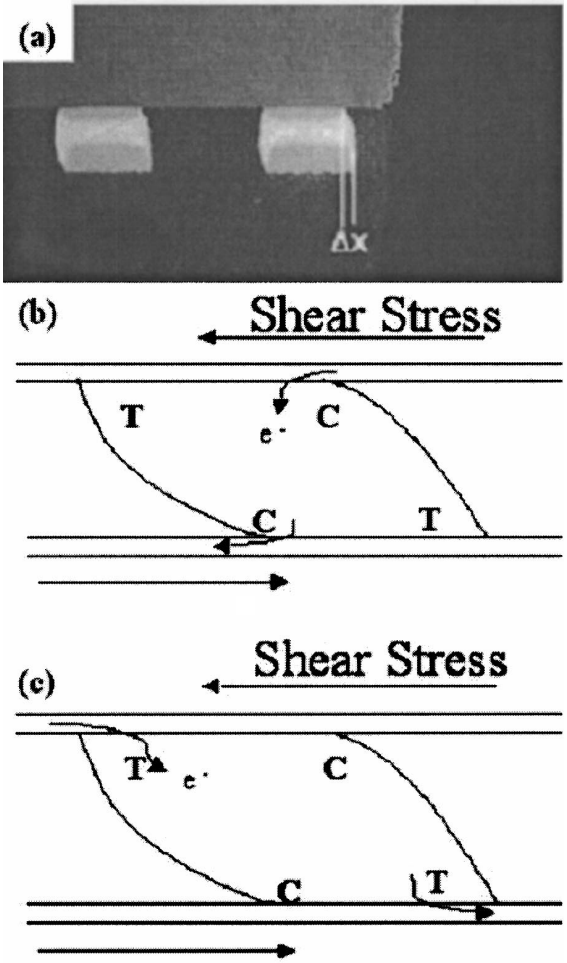

FIG. 24. (a) Cross-sectional SEM image of a flip chip corner solder joint joining a chip to a board. Relative displacement of 10 μm due to shear between the chip and the board can be seen. (b) Schematic diagram of a sheared solder joint in which the electron current enters the joint from the compressive "C" region. (c) Electron current enters the joint from the tensile "T" region.

150 °C, the extrusion at the anode became very apparent after 8 days' stressing with current density of 2.8×10^4 A/cm^2, as shown in Fig. 22(a). The void at the cathode is seen more clearly after polishing away a 10 μm layer from the surface, see Fig. 22(b). The extrusion at the anode side is a big lump, rather than small hillocks as in the anodes of Al or Cu thin film interconnects.

The morphological change due to electromigration is less obvious at room temperature, as shown in Fig. 22(c), although the stressing time is longer, 12 days, and current density is more than doubled.

Redistribution of Sn and Pb in eutectic SnPb solder lines was examined by x-ray dispersive analysis. At 150 °C, a significant accumulation of Pb occurs at the anode side, with a maximum concentration reaching 95 wt % Pb. In contrast, at room temperature Sn accumulates at the anode side, with a maximum concentration of about 92 wt % Sn. These phenomena suggest that in the SnPb system Pb is the dominant diffusion species at 150 °C, but Sn is the dominant diffusion species at room temperature. These results are in agreement with those of Gupta *et al.*[18] obtained from tracer diffusions of ^{210}Pb and ^{113}Sn in eutectic SnPb solder, that Pb diffusion is faster than Sn at temperatures above 120 °C, and Sn diffuses quicker than Pb at temperatures below 120 °C.

Knowing the volume of mass transport (the volume of the extrusion at the anode or void at the cathode), we can obtain the flux of electromigration, J_{em}, by assuming that $V_{em}=\Omega J_{em}At$, where V_{em} is the volume of mass transport, Ω is the atomic volume, A is the cross section of the solder line, and t is the time of electromigration. Then, the effective charge number, Z^*, can be calculated. The average values of Z^* in high temperature and room temperature electromigration in eutectic SnPb are calculated to be 33 and 39, respectively, which are close to the reported values of 47 and 18 for self-electromigration in bulk Pb and bulk Sn, respectively.[2]

The polarity effect of electromigration on the thickness and morphology changes of IMCs at the cathode and anode in $SnAg_{3.8}Cu_{0.7}$ V-groovesolder lines has been investigated at 150 and 180 °C, with current density in the range of 10^3-10^4 A/cm^2.[71,72] The same IMC of Cu_6Sn_5 and Cu_3Sn

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form at solder/Cu interfaces with or without applying electric current. The IMC formed after the initial reflow had a scallop-type morphology and transformed into layer-type morphology in solid state aging, with or without electromigration.

Electromigration enhances the growth of IMCs at the anode and inhibits the growth at the cathode as compared with the no-current case. As shown in Figs. 23(a) and 23(b), for the sample under current density of 3.2×10^4 A/cm^2 at 180 °C, both Cu_6Sn_5 and Cu_3Sn layers keep growing at the anode side with the application of current. The total thickness approaches 9 μm after 87 h. This thickness is comparable with that grown for 200 h at 180 °C without current. At the cathode side, shown in Figs. 23(c) and 23(d), the IMC grew much slower than that at the anode side and the IMC also became layer like. Voids started to appear in the solder part just in front of the solder/IMC cathode interface after 21 h.[71,72] The growth of IMC at the anode obeys the parabolic growth rate, and the back stress in IMC might have played a significant role in the parabolic growth.

The polarity effect of electromigration on IMC formation in eutectic SnPb solder, as a function of temperature, is of interest because of the temperature dependence of the dominant diffusing species in the solder. For example, we can use Ni instead of Cu as electrodes and the formation of IMC will be different. Then, the length of the solder line might affect IMC formation at the cathode and anode, too.

D. Effect of stress on electromigration and vice versa

In flip chip devices, the solder joints at the corners of a chip are subjected to large shear during thermal cycles because of different thermal expansion coefficients between the chip and its substrate. In Fig. 24(a), an SEM image of a corner solder joint in a flip chip is shown, where the upper part of the joint is sheared to the left with respect to the lower part of the joint. The shear displacement "x" was measured to be 10 μm. The height "h" of the solder in the joint is about 30 μm, so the shear ($s=x/h$) is very large. To demonstrate the relationship between the shear and electromigration, a schematic diagram of the cross section of a solder joint under shear is shown in Fig. 24(b). In the diagram a letter "T" is used to indicate the tensile region and a letter "C" to indicate the compressive region. There are a pair of "T" and a pair of "C" in the sheared joint. We note that the electrons can enter the joint from a "C" region as shown in Fig. 24(b) or a "T" region as shown in Fig. 24(c). Similarly, it can get out of a joint from either a "C" or "T" region. Generally speaking, at the cathode, electromigration is enhanced by tension but retarded by compression. At the anode, the interaction is opposite. Hence, a favorable condition should be the electron current entering the joint from the "C" region and leaving from the "T" region. We note that there are no experimental data to verify the effect yet. If this effect is true, we should be able to take advantage of it in designing the circuit in packaging.

The question of back stress in flip chip solder joints is interesting, yet no measurement has been conducted to investigate it. Under the constraints of underfill, back stress may build up in a flip chip solder joint. How the back stress interacts with the thermal shear stress is also of interest.

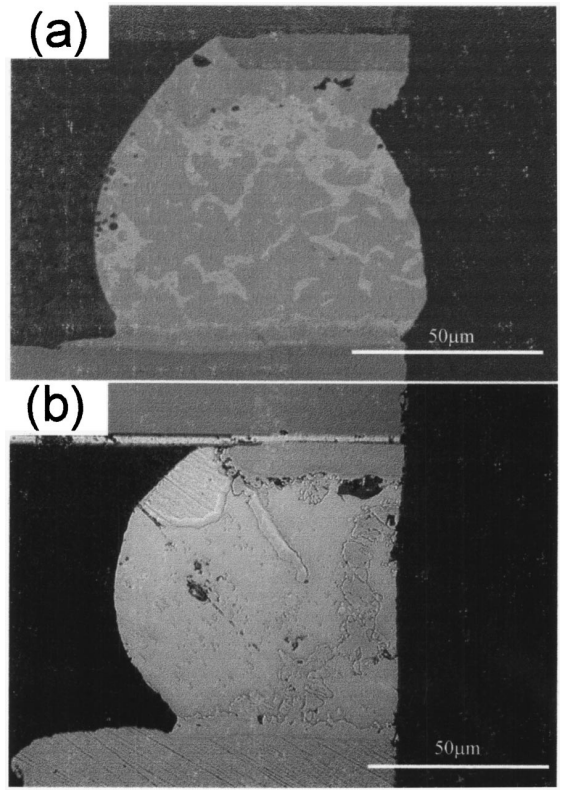

FIG. 25. (a) Cross-section SEM image of a side view of a eutectic SnPb solder joint after electromigration. A dimple in the cathode side and a bump in the anode side can be seen, (b) Cross-section optical image of a side view of a eutectic SnAgCu solder joint after electromigration. The surface remains flat, indicating that the electromigration damage is very little (Refs. 58 and 73).

E. Effect of solder composition on electromigration

The electronic industry has been searching for Pb-free solders for benign manufacturing. Tentatively, eutectic SnAgCu has been recommended to replace eutectic SnPb. The composition of Sn in a solder joint is an interesting issue in electromigration. For example, in eutectic SnAgCu, the composition of Sn is about 96 wt % and it matrix is essentially Sn. In eutectic SnPb, the composition of Sn is about 60 wt %. In high-Pb solders, which have been widely used in mainframe computers to join chips to ceramic modules, the composition of Sn is 3 wt % and its matrix is essentially Pb. Generally speaking, if we assume atomic diffusivity is proportional to melting point of the solder, we expect electromigration in eutectic SnPb to be the fastest, next will be the eutectic SnAgCu, and the slowest will be the high Pb. At the moment, we have preliminary data to show that indeed electromigration in eutectic SnAgCu is slower than that in eutectic SnPb.[58,73]

Figures 25(a) and 25(b) show, respectively, sideview SEM images of eutectic SnPb and eutectic SnAgCu solder joints after electromigration. The test temperature was 120 °C and the applied current was 1.5 A. In Fig. 25(a) a

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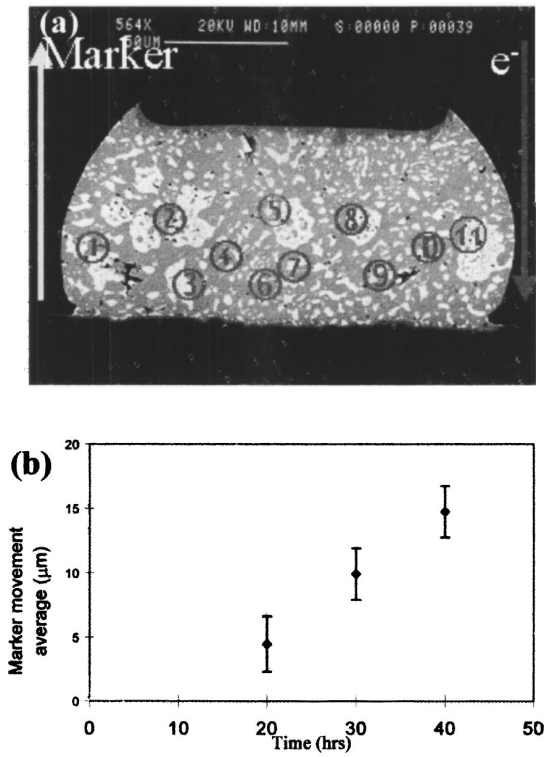

FIG. 26. (a) Cross-section SEM image of a front view of a eutectic SnPb solder joint after electromigration. Surface markers are indicated by the small circles with numbers. (b) Marker displacement plotted against time (Refs. 58 and 73).

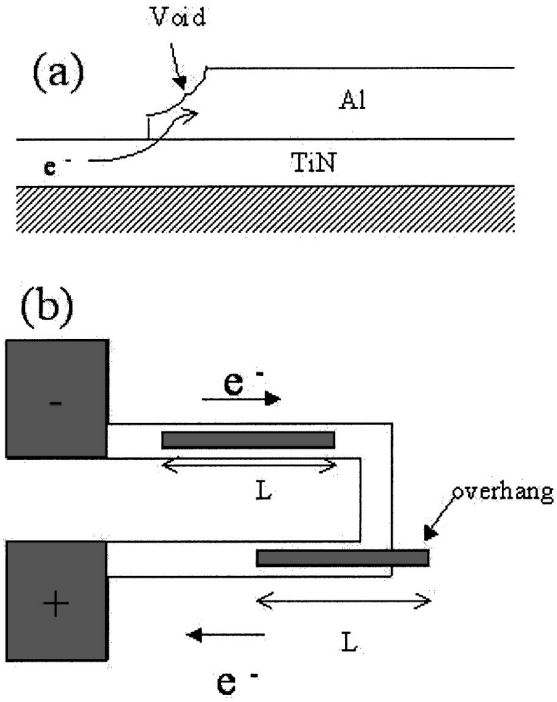

FIG. 27. (a) Schematic diagram of the cross section of an Al short strip on TiN and the formation of a void at the upper-left corner where current density is low. (b) Schematic diagram of the top view of a TiN base line having a U-turn and an Al short strip having an overhang (Refs. 74 and 75).

dimple in the cathode side and a bump in the anode side can be seen after 40 h. In Fig. 25(b), the surface remains flat after 200 h, indicating almost no obvious damage by electromigration.

Figure 26(a) shows a cross-sectional SEM image of the front view of a eutectic SnPb solder joint after electromigration. On the polished surface, embedded debris (polishing powder) was found which served as diffusion markers for the study of atomic flux migration during electromigration. The arrow in Fig. 26(a) indicates that electrons flowed downward, the same as the atomic flux of electromigration, hence, the markers migrated upward. The marker displacements have been measured as a function of time and they are shown in Fig. 26(b). The displacement is linear with time. Knowing the displacement and the average cross-sectional area, the volume displaced by electromigration, in turn the effective charge number of electromigration, can be calculated as discussed in Sec. IV C. The obtained Z^* values are in agreement. Using the same marker measurement, the rate of displacement was found to be much less in eutectic SnAgCu.

For electromigration in the high-Pb solder, there are little published data for comparison. Since the lattice diffusivity of eutectic SnPb solder is about two orders of magnitude faster than that in the high-Pb solder, electromigration in the latter is expected to be two orders of magnitude slower than the former, assuming the other parameters as given in Eq. (9) are the same. Atomic diffusivity in a eutectic SnPb alloy is affected by microstructure. Below the eutectic temperature, eutectic SnPb alloy has a lamellar structure consisting of primary Pb and primary Sn phases. Atomic diffusion along the lamellar interfaces has been found not to be as fast as expected due to habit or a semicoherent relationship between the lamellae.[18] The activation energy of the interfacial diffusion is about 80%, not 50%, of that of lattice diffusion in the primary phases. Then, in solid state aging of solder joints, large grains of primary Pb and primary Sn are formed and the interfaces are disconnected and reduced, so the interfacial diffusion is less dominant. Therefore, electromigration in a eutectic SnPb solder joint is sensitive to the thermal history of the joint, since it was very different after reflow as compared to solid state aging, especially when we consider electromigration at the device temperature of 100 °C.

V. CURRENT CROWDING

In Sec. IV A, we discussed current crowding in a flip chip solder joint and its effect on electromigration. We expect to find current crowding in a multilevel structure of Al and Cu interconnects due to interfaces, turns, and vias. We review below experimental observations of the effect of current crowding, and we introduce a driving force of electromigration on the basis of the current density gradient. We emphasize that this force is normal to the direction of electron flow, while the classic electron wind force is parallel to electron flow.

Several observations of unexpected void formation in low current density regions in electromigration tests have been reported. Using the Blech structure of short Al strips on a TiN base line as sketched in Fig. 27(a), Okabayashi and

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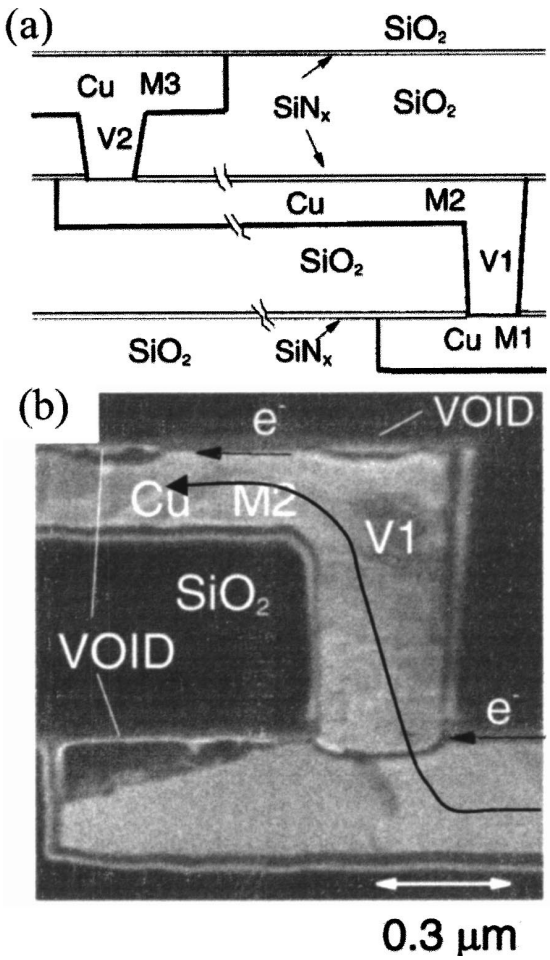

FIG. 28. (a) Schematic diagram of a two-level Cu dual damascene interconnect. The electron current direction is indicated by a curve arrow. (b) SEM image of void formation in the upper surface of the Cu interconnect and also a large void formation in the overhang at the left-hand bottom of the Cu interconnect (Ref. 40). (Courtesy of Dr. C. K. Hu, *et al.*, IBM T. J. Watson Research Center, Yorktown Heights, NY.)

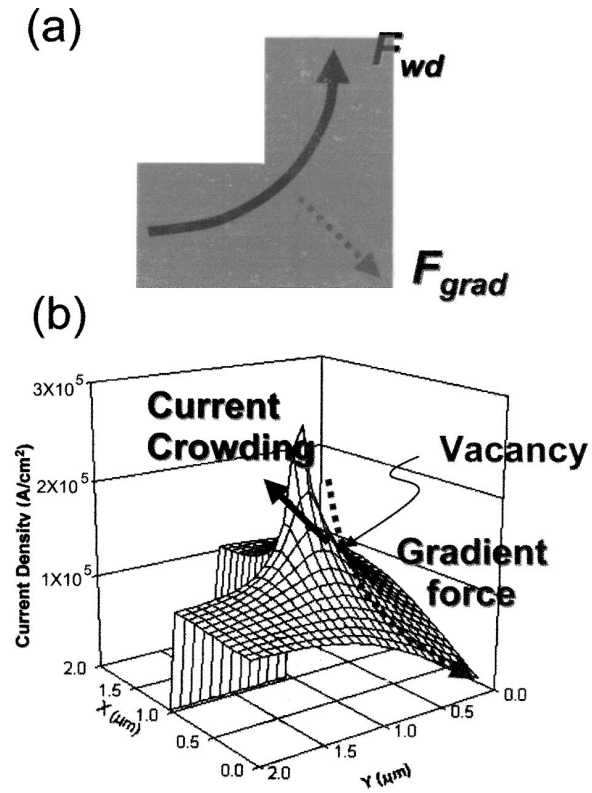

FIG. 29. (a) Schematic diagram of a 90° turn in an interconnect, where F_{wd} is electron wind force and F_{grad} is current density gradient force. (b) Current distribution in the 90° turn, in which current crowding occurs at the inner corner (Ref. 76).

co-workers observed void formation to start at the upper-left corner of the strip where current density is low.[74] The measurement was performed by sidewise cross-sectional TEM. After a long period of testing time when the anode side has formed a large hillock, they reversed the current direction and found that voids started to form at the tip of the hillock. Again, the voids were found in the region of nearly no current density. Figure 27(b) shows a schematic diagram of the top view of a Blech structure of the Al strip on TiN having a U turn, and it was used to study electromigration by Shingubara and co-workers.[75] Some of the Al strips had an overhang outside the TiN and the overhang should have very little current. Nevertheless, voids were found in the overhang.

In Figs. 28(a) and 28(b), respectively, a schematic diagram and SEM image of electromigration damage in a multilevel Cu interconnect are shown.[40] The direction of electron flow is indicated by the long and curved arrow. Two kinds of damage were observed. First, surface void formation was observed in the upper surface of the Cu interconnect. Second, a huge void formation was found at the lower extension of the Cu interconnect. The extension should have had very little current density, nevertheless, a large void was found there.

In the above three cases, voids were found to form in the low current density region. The explanation given was that vacancies were driven by a stress gradient to the low current density region. Such an explanation is unsatisfactory because it has ignored the fact that void formation requires nucleation that in turn requires a supersaturation of vacancies. We reconsider the case shown in Fig. 27(a) or 3(a). According to the classic electron wind force of electromigration, vacancies are driven to the cathode in the opposite direction of electron flow, hence, vacancies should accumulate at the lower-right corner. Thus, there is a vacancy concentration gradient decreasing from the lower corner to the upper corner, which may induce a flux of vacancies to go from the lower corner to the upper corner. What is hard to explain by this reasoning is why vacancies can reach supersaturation at the upper corner and nucleate a void there, since the vacancy gradient is from the lower corner (high concentration) to the upper corner (low concentration). Vacancies should have reached supersaturation at the lower corner first and nucleated a void there. A different explanation has been offered on the basis of a new driving force of electromigration.[76]

A. Driving force of electromigration

In Figs. 29(a) and 29(b), schematic diagrams of an interconnect having a 90° turn and a current density distribution

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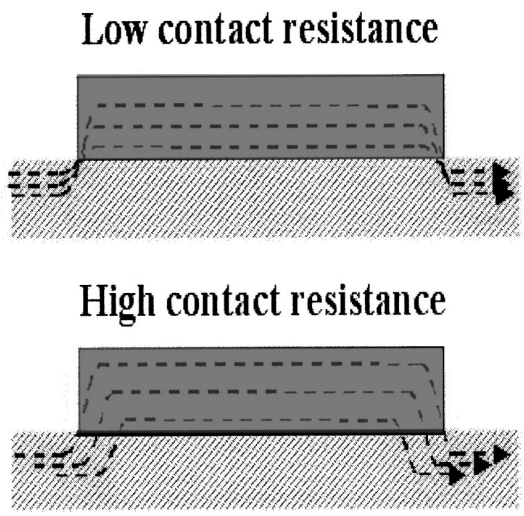

FIG. 30. Effect of contact resistance on current crowding is to reduce it by current spreading (Refs. 80 and 81).

at the turn are shown, respectively. A very high current density exists at the inner edge of the turn, and there is a current density gradient that decreases from the inner edge to the outer edge of the turn. If a potential is applied to the gradient, it produces a force acting down the gradient. Consider a vacancy in the high current density region, it will be pushed down the current density gradient by a force, F, because the vacancy is a high resistance or a high potential entity:

$$F=-\frac{dP}{dr}, \tag{10}$$

where $P=q_v jA\Delta\rho_v$, and q_v is the effective charge of the vacancy ($=Z_v^* e$ and Z_v^* is the effective charge number), j is the current density, A is the scattering cross section of the vacancy, and $\Delta\rho_v$ is the resistance of the vacancy in the lattice.[76–78] The vacancy flux driven by the gradient force will be given as

$$J_{\mathrm{gm}}=\Delta C_v \frac{D}{kT}\left(-\frac{dP}{dr}\right), \tag{11}$$

where ΔC_v is the excess vacancy concentration in the current crowding region relative to the constant current density region.

Another way to envision the gradient force is to compare the scattering on the two sides of a vacancy. The scattering on the higher current density side is greater than that on the lower current density side, hence, there is a net force pushing the vacancy down the gradient. While the scattering of a lattice atom can be calculated, the resistance of a lattice atom is only about one hundredth of that of a vacancy,[79] so the gradient force on an atom is much less. Besides, the mobility of a vacancy is much higher than an atom.

On the basis of scattering, it is expected that the force should have a square dependence on current density. The force by scattering depends on the momentum of electrons and the number of electrons scattered by an atom per unit time; both are proportional to current density. This has been shown in Black's equation of mean-time to failure of interconnects, which will be discussed in Sec. VI A.

In Eq. (10) and also in Huntington's equation of electromigration, which is shown below,

$$J_{\mathrm{em}}=C\frac{D}{kT}Z^* e\rho j, \tag{12}$$

the force is linear with current density. The discrepancy could be due to the fact that in Huntington's derivation,[20] the effect of momentum exchange between electrons and diffusing atoms has been lumped into "Z^*," the effective charge number, although Z^* does not appear to depend on current density explicitly. This is not so. Because electrons scatter on (or very near) the Fermi surface, and their momentum transfer per collision is on the order of the Fermi momentum and not the electron drift velocity (which is proportional to electron current density). Therefore, Z^* contains the momentum exchange, but it does not contain the current density. The force is linearly proportional to electron current density.[25]

Combining the classic electron wind force and the current density gradient force in the cathode side of the Al short strip shown in Fig. 3(a), we have a vector sum of

$$J_{\mathrm{sum}}=J_{\mathrm{em}}+J_{\mathrm{gm}}=C_v\frac{D_v}{kT}(-Z_v^* eE)+\Delta C_v\frac{D}{kT}\left(-\frac{dP}{dr}\right), \tag{13}$$

where the first term is due to electromigration driven by the electron wind force and the second term by the current density gradient force. Hence, in Figs. 3(a) and 5, vacancies will be pushed towards the upper corner before they reach the lower corner. This will lead to accumulation and supersaturation of vacancies in the upper corner. A void will nucleate, grow, and eventually deplete the entire cathode end of the strip. In comparison, if a void were nucleated at the lower corner, it would not be able to deplete the entire cathode end of the strip.[76]

B. Effect of contact resistance on current crowding

Current crowding can be diffused or spread by contact resistance as shown in Fig. 30.[80,81] By changing the contact resistance between the Al strip and TiN base line, we found that a spreading of the current entering or leaving the Al can be achieved, resulting in a reduction of current crowding.

The beneficial effect of contact resistance can be applied to vias and to flip chip solder joints. In the latter, we can use a thick underbump metallization such as a thick Cu or electroless Ni(P). It will move the high current density region from the solder to the UBM. However, the high current density in the UBM might enhance the dissolution of the UBM as shown in Sec. IV A.

VI. ANALYSIS OF MEAN TIME TO FAILURE

A. Effect of current density

The electronic industry uses the mean-time-to-failure (MTTF) analysis to predict the lifetime of a device. In 1969, Black provided the following equation to analyze failure in Al interconnects caused by electromigration:[82]

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$$\mathrm{MTTF}=A\frac{1}{j^n}\exp\left(\frac{Q}{kT}\right). \tag{14}$$

The derivation of the equation was based on an estimate of the rate of forming a void across an Al interconnect. The most interesting feature of the equation is the dependence of the MTTF on the square power of current density, i.e., $n=2$.

In the MTTF equation, whether the exponent n is 1, 2, or a larger number has been controversial, especially when the effect of Joule heating is taken into account. However, assuming that mass flux divergence is required for failure and the nucleation and growth of a void requires vacancy supersaturation, Shatzkes and Lloyd have proposed a model by solving the time-dependence diffusion equation and obtained a solution for MTTF in which the square power dependence on current density is also obtained.[83] Nevertheless, whether Black's equation can be applied to MTTF in Cu interconnects and flip chip solder joints deserves careful examination.

B. Effect of activation energy of diffusion

Although the effect of microstructure was not taken into account in obtaining the MTTF equation, Black has studied three kinds of Al films with different microstructures and obtained three different values of activation energy "Q" in the MTTF equation.[82] It is clear that as linewidth has been reduced from 25 to 10 μm (in Black's samples) to less than half a micron today, the distribution of grain size and the dominant diffusion path in interconnects have changed. The changes will affect the activation energy "Q" in the MTTF equation. To determine the activation energy, accelerated tests at high temperatures are performed. We must pay attention to the temperature range in which lattice diffusion might overlap grain boundary diffusion and also grain boundary diffusion might overlap surface diffusion. For example, while an accelerated test at 350 °C for Al interconnects is acceptable, it is not for Cu interconnects since grain boundary diffusion cannot be ignored at 350 °C for Cu as shown in Table I, although Cu has a higher melting point than Al. For eutectic SnPb solder, it is more complicated because of the change of dominant diffusion species above and below 100 °C.

C. Effect of void nucleation and growth at cathodes

The formation of a void requires nucleation. If we ignore at this moment the barrier of nucleation of a void, we can just consider the growth of a void by vacancies driven to the void or by atoms driven away from the void. We assume the volume of the void to be $V=\Omega J_{\mathrm{em}}A_d t$, where Ω is the atomic volume of an atom or a single vacancy; J_{em} is the atomic or vacancy flux driven by electromigration; A_d is the effective cross-sectional area of the diffusion flux, which is different for lattice diffusion, grain boundary diffusion, and surface diffusion; and t is time. To define the volume of the void that is large enough to become an opening, we consider a void in an Al line above a W via and we take the void volume to be equal to the cross section of the via times the thickness of the Al line. Ignoring nucleation, the time needed to fail a test strip is the time needed to transport enough vacancies to grow the void of volume V:

$$t=\frac{V}{\Omega J_{\mathrm{em}}A_d}. \tag{15}$$

We recall that J_{em} depends on back stress as shown in Eq. 4(a). On the other hand, a simpler way to estimate the time of growth of such a void is to divide the diameter of the via by the drift velocity measured from the Blech strip shown in Fig. 4 or the two-level test structure shown in Fig. 5,

$$t=\frac{d}{v_{\mathrm{drift}}}. \tag{16}$$

In measuring the drift velocity in Al(Cu) strips using the two-level test structure, it was found that there is a long incubation time before void growth. The incubation time is due to the depletion of Cu and nucleation of a void in the cathode end. After that the void growth by electromigration in the pure Al cathode is very fast. This behavior is also found in the testing of Cu(Sn) samples shown in Fig. 12, as compared to that of pure Cu in Fig. 12. Since the grain boundary diffusivity in Al and surface diffusivity in Cu as shown in Table I are close to each other and their corresponding cross-sectional area of diffusion is also comparable, we expect their drift velocity near the device operation temperature to be similar.

The above calculation indicates that the time needed to grow a void to the size of an opening above a via in Al interconnects is only a small fraction of the measured MTTF. Therefore, the bulk part of the MTTF is taken up by the time needed to deplete the Cu solute from the cathode and to overcome the nucleation barrier of a void. In other words, even in the heterogeneous nucleation of a void in Al interconnects, the supersaturation of vacancies needed to overcome the nucleation barrier is important as assumed in the model of Shatzkes and Lloyd.[83]

However, the case of the Cu interconnect is different. If we consider surface diffusion, it is hard to imagine why the nucleation of a void on a surface requires much supersaturation. On the other hand, the growth of a void on a surface may not be a localized event since it can spread out and thin down the entire or a large portion of the interconnect. In such a case, it is the growth not nucleation that will take most of the time to fail the device. Furthermore, a void spreading out between a via and the line below it is much more serious than a void spreading out in the middle or other part of the line far away from a via.

In the case of a flip chip solder joint, Fig. 18 shows that the time to failure is controlled not by the propagation of a void across the contact interface, but by void nucleation. The latter takes about 90% of the time before failure. The propagation of the void across the entire contact takes only about 10% of the time. Furthermore, as shown in Secs. IV A and V, the effect of current crowding cannot be ignored in the analysis of MTTF. Black did point out the importance of the cur-

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rent or temperature gradient on interconnect failure, although he did not take them into account in his equation explicitly.[82] On the basis of the failure mode of a flip chip solder joint as shown in Figs. 16 and 17, the major effects of current crowding are to increase greatly the current density at the entrance of the solder joint and also to increase the local temperature due to Joule heating.

The above discussion indicates that we may not apply Black's equation directly to predict MTTF for Cu interconnects and flip chip solder joints. While Black's basic assumptions are correct, we need to revise the equation for the failure in Cu interconnects and flip chip solder joints. The distribution of failure time due to electromigration in a large number of interconnects has been found to obey a log–normal function. Why such a distribution function is obeyed is unclear since no mathematical derivation of such a distribution function has been given.

D. Effect of hillock and whisker formation at anodes

The extrusion of hillocks and whiskers at anodes is another mode of interconnect failure. Such extrusion can become a short or crack the interlayer dielectric. The latter is a concern for Cu/low-*k* technology. Because of current crowding, the one-dimensional compressive stress distribution as presented in Fig. 8 for a short strip is inadequate. We expect a stress center at the lower-right corner (anode) in Fig. 3(a) or 7 due to current crowding where current exits the strip. While the electron wind force pushes atoms to the lower-right corner, there should be a current density gradient force to push atoms to the upper-right corner. Nevertheless, the gradient force on an atom is small as we have discussed in Sec. V, so the effect of the gradient force at the anode is different from that at the cathode. We must use a two-dimensional stress distribution to model the stress at the anode. Measurement of the two-dimensional stress distribution is a challenging problem.

The atomic mechanism of growth of hillocks and whiskers at the anode is of interest. Typically, spontaneous whiskers grow from the bottom by pushing up or by extrusion.[84] This is also true for hillock growth since the electron wind force drives atoms to the bottom where the current exits the strip at the anode end. If adhesion between the interconnect and its bottom dielectric is weak, extrusion occurs at the bottom interface. If the bottom adhesion is good, extrusion of hillocks occurs on the top surface of the strip, and a crack of the surface oxide (Al strip) is required. Vacancies can come in from the crack to mediate the diffusion of atoms. By using focused ion beams, we can cut a thin slice of the anode and use transmission electron microscopy to study the microstructure change and the growth mechanism.

A strip of Sn grows whiskers at the anode driven by electromigration.[55] On the other hand, it is well known that Sn whiskers grow spontaneously on a thin coating of Sn on Cu.[85,86] But, whether the mechanism of growth of these two kinds of Sn whiskers is the same or not is unknown. While both are driven by a compressive stress, it is unclear whether the stress distribution in the root area of a whisker is the same.

VII. SUMMARY

We have compared the electromigration behaviors in Al and Cu interconnects and solder joints on the basis of the ratio of their melting point to the device operating temperature of 100 °C. Accordingly, grain boundary diffusion, surface diffusion, and lattice diffusion dominate, respectively, in electromigration in Al, Cu, and solder. In turn, the effects of microstructure, solute, and stress on electromigration are different in Al, Cu, and solder. For example, while the triple point of grain boundaries has been an important issue in electromigration in Al, it is not so in Cu interconnects because a triple point on the surface is not an effective mass flux divergence. Therefore, while Cu solute in Al has reduced grain boundary diffusion of Al, we will need a solute in Cu which can retard the surface diffusion of Cu. So far, Sn has been found to be very effective in retarding electromigration in Cu. For the damascene process, improving the adhesion of the Cu to the dielectric layer above it is a most challenging issue of device fabrication because otherwise the surface is the built-in mass transport path of electromigration. For Cu/low-*k* interconnects, the compressive stress at the anodes induced by electromigration will be a very serious issue since the low-*k* dielectric (with a value *k* around 2) tends to be weak mechanically. Several experimental observations have shown that void formation in electromigration occurs in low current density regions accompanying current crowding. A electromigration force is proposed; the current density gradient force, acting normal to current flow, can explain why electromigration damage occurs away from the high current density region. In mean-time-to-failure analysis, the time taken to nucleate a void is more important in Al interconnects and flip chip solder joints than that on the surface of a Cu interconnect. For accelerated tests of electromigration, the temperature range must be relevant to the real failure mechanism in actual devices, e.g., 350 °C is too high for Cu interconnects.

Finally, there are still many unanswered questions about electromigration, therefore, much more study will be needed. At the moment, the microelectronic industry is working on the integration of ultra-low-*k* dielectrics with Cu metallization. The question of what is beyond Cu will be challenging.

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