IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

IPR2025-01211

U.S. Patent No. 7,439,623

DECLARATION OF DR. REINHOLD DAUSKARDT IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 7,439,623

TSMC-1003
TSMC Ltd.
IPR2025-01211

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I, Dr. Reinhold Dauskardt, declare as follows:

I. INTRODUCTION

1. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited ("TSMC") in connection with a petition for *inter partes* review of U.S. Patent No. 7,439,623 ("'623 patent"), which I understand is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 5-6, 10, 19-20, 23-24, 27, 29-31, 33-38, 41, 43-44, and 48 of the '623 patent ("Challenged Claims"). These claims of the '623 patent are included in attached Appendix B.

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the basis for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the '623 patent is unpatentable for at least the reasons I discuss below.

II. BACKGROUND AND QUALIFICATIONS

A. Education and Career

5. I have summarized in this section my educational background, career history, and other relevant qualifications.

6. My technical background and experience are summarized in my curriculum vitae and listing of publications included below in Appendix C.

7. I am currently the Ruth G. and William K. Bowes Professor of Materials Science and Engineering in the Department of Materials Science and Engineering at Stanford University. I have additional appointments as Professor in the Department of Mechanical Engineering, the Biodesign Institute and in the Department of Surgery, Stanford School of Medicine. I am also a Visiting Professor in the School of Materials Science and Engineering at the Nanyang Technological University in Singapore.

8. I earned a B.Sc. (1980) and M.Sc. (1983) in Physics, Mathematics and Materials from the University of the Witwatersrand, South Africa. Thereafter, I earned a Ph.D. in Materials Science and Engineering from the University of California at Berkeley / University of the Witwatersrand in 1988.

9. Based on my 28 years of experience in the field of materials science, particularly in connection with the thermomechanical reliability and manufacturing processes of microelectronic devices, and based on the acceptance of my

publications and professional recognition by societies in this field, I believe that I am an expert in the technology at issue in this proceeding and am qualified to provide an opinion in this declaration.

10. I have extensive experience in integrating new materials into emerging microelectronic devices and I am an internationally recognized expert on the design and thermomechanical reliability of engineering structures and semiconductor device technologies. My experience includes semiconductor device and packaging processing operations and processing environments (including plasma processing, chemical mechanical planarization, and a wide range of deposition techniques) and their effects on device materials, structures and their properties.

11. I teach several undergraduate and graduate classes in the School of Engineering at Stanford University on materials science topics. These classes include detailed discussions of structure-property relationship of materials, semiconductor device structures, their manufacturing processes and reliability.

12. My interdisciplinary research includes interaction with researchers in academia and industry. I have served as an editor and reviewer for a number of journals and books including Nature, Science, Acta Materialia, the Journal of Applied Physics, and the Journal of Microelectronics and Electronic Packaging. I am a frequent reviewer of proposals for U.S. federal and international funding agencies, I have organized international conferences and symposia in the area of

materials and electronic devices, and have published over 350 articles in the scientific literature.

13. I am a named inventor on over 30 provisional and granted United States patents. I have served as the research advisor of 67 doctoral students who have graduated under my supervision and mentorship and currently have 14 doctoral graduate students in my research group and 2 postdoctoral scholars. I have also supervised the research programs of more than 26 master's students and mentored more than 46 post-doctoral fellows, medical residents and medical fellows along with several visiting scientists and engineers.

14. I am an internationally recognized expert on the semiconductor devices and their manufacturing processes for which I was awarded the prestigious Semiconductor Industry Association University Researcher Award in 2010 for "research which has provided substantive and sustained contributions to semiconductor industry science and technology." This research includes studies of the adhesion and cohesion of interfaces and layers in materials, and the causes and mechanisms of fracture, delamination, stress migration, voiding, fatigue and mechanical reliability of microelectronic devices and their packages, and similar studies of the materials used in the manufacture of electronic device technologies. For my research directed to CMP processing, I was awarded the VLSI/ULSI

Multilevel Interconnection (VMIC) International Conference Award in 2008 for "Optimized Curing and CMP of Nanostructured Ultra-low-k Films," Fremont, CA.

15. My research group is well known internationally for pioneering studies of the synergistic effects of mechanical forces, chemical environments, temperature and other forms of degradation on thermomechanical stresses and the processes of fracture and defect evolution that determine the reliability of materials and devices. Our experimental studies are complimented with a range of computational and theoretical modelling capabilities.

16. I have won a number of awards including the U.S. Dept. of Energy Outstanding Scientific Accomplishment Award (1989), the Alexander von Humboldt Research Award (2002), the ASM International Silver Medal (2003), an IBM Faculty Award (2006), the TMS Structural Materials Distinguished Scientist/Engineer Award (2010), the Semiconductor Industry Association University Researcher Award (2010), the H. Maso Award for fundamental contributions to skin science (2011), and the IBM Shared University Research Award (2011).

17. I have contributed significantly to leadership in Stanford's multidisciplinary materials and microelectronic device efforts which spans several schools and the Stanford Hospital. I am also a Fellow of ASM International and a Fellow of the American Ceramic Society.

B. Publications

18. I have authored over 300 peer-reviewed academic journal publications, and I am a named inventor on at least 7 granted U.S. patents. Some examples of relevant publications to the technology at issue in this proceeding are:

a) M. Lane, N. Krishna, I. Hashim, and R. H. Dauskardt, "Adhesion and Reliability of Copper Interconnects with Ta and TaN Barrier Layers," Journal of Materials Research, 15 [1] 203-211, 2000.

b) D. M. Gage, A.D.W. Thiel, R. H. Dauskardt, M. K. Haas, L.M. Matz, M. L. O'Neill, T. M. Wieder, G. Banerjee and M. B. Rao, "Impact of CMP polish and pCMP Cleaning on adhesion of SiCN capping layer on PECVD-derived Porous OSG and Copper" Solid State Phenomena, 145-146, 377-380, 2009.

c) Ryan Birringer, Roey Shaviv, Roy H. Geiss, David Read, and Reinhold Dauskardt, "Effects of Barrier Composition and Electroplating Chemistry on Adhesion and Voiding in Copper / Dielectric Diffusion Barrier Films," Journal of Applied Physics, 110, 044312, 2011.

d) Qiran Xiao, Brian Watson and Reinhold H. Dauskardt, "Organothiol-Based Hybrid-Layer Strategy for High-Performance Copper Adhesion and Stress-Migration via Simultaneous Oxide Reduction," Advanced Materials Interfaces, 3, 14, 2016.

e) Michael T. Barako, Scott G. Isaacson, Feifei Lian, Eric Pop, Reinhold H. Dauskardt, Kenneth E. Goodson, and Jesse Tice, "Dense Vertically Aligned Copper Nanowire Composites as High Performance Thermal Interface Materials," ACS Applied Materials and Interfaces, 9 (48), pp 42067–42074, 2017. DOI: 10.1021/acsami.7b12313.

f) Markus D. Ong, Vincent Jousseaume, Sylvain Maitrejean, Reinhold H. Dauskardt: "Fracture Properties of Porous MSSQ Films: Impact of Porogen Loading and Burnout, in Materials, Technology and Reliability of Low-k Dielectrics and Copper Interconnects," edited by Ting Y. Tsui, Young-Chang Joo, Lynne Michaelson, Michael Lane, Alex A. Volinsky (Mater. Res. Soc. Symp. Proc. 914, Warrendale, PA, 2006), 0914-F04-07.

g) Ryan Birringer, Roey Shaviv, Tom Mountsier, Jon Reid, Jian Zhou, Roy H. Geiss, David Read, and Reinhold Dauskardt, "Adhesion, Cu Voiding, and Debonding Kinetics of Copper / Dielectric Diffusion Barrier Films," Advanced Metallization Conference, Baltimore, 2009.

h) M. Lane, W. Ni, R. H. Dauskardt, Q. Ma, H. Fujimoto and N. Krishna, "Effects of Interface Nonplanarity on the Interface Fracture Energy on the TiN/SiO_2 System," in Thin Film Stresses and Mechanical Properties VII, vol. 516, Editors: T. Marieb, J. Bravman, M.A. Korhonen, J.R. Lloyd, Proceedings of MRS Annual Meeting, Boston, MA, pp. 357 – 362, 1998.

i) Taek-Soo Kim, Qiping Zhong, Maria Peterson, Halbert Tam, Tomohisa Konno, and Reinhold H. Dauskardt, "Stress and Slurry Chemistry Effects on CMP Damage of Ultra-Low-k Dielectrics," IEEE International Interconnect Technology Conference Proceedings, June 2007.

j) Reinhold H. Dauskardt, Taek-Soo Kim, Qiping Zhong, Maria Peterson, Halbert Tam, and Tomohisa Konno, "Stress and Slurry Chemistry Effects on Cracking and Damage Evolution during CMP: Implications for Next Technology Nodes," Twelfth International Conference on Chemical-Mechanical Polish (CMP) Planarization for ULSI Multilevel Interconnection (CMP-MIC), Fremont, California, 2006.

k) M. Lane, A. Vainchtein, H. Gao, and R. H. Dauskardt, "Plasticity Contributions to Interface Adhesion in Thin-Film Interconnect structures," Journal of Materials Research, 15 [12], 2758-2769, 2000.

l) Ryan Birringer, Roey Shaviv, Paul Besser and Reinhold Dauskardt, "Environmentally Assisted Debonding of Copper / Barrier Interfaces," Acta Materialia, 60, 2219–2228, 2012.

C. Compensation

19. I am being compensated for services provided in this matter at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of my work in this matter. My compensation is not contingent upon the

results of my study or analysis, the substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '623 patent.

III. MATERIALS REVIEWED

20. In forming my opinions regarding the '623 patent, I reviewed the materials discussed in this declaration, including the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

IV. LEGAL STANDARDS

21. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '623 patent are patentable, I understand that I am obliged to follow existing law.

A. Anticipation

22. I understand the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I understand that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

23. I understand that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

24. I understand that under 35 U.S.C. §103(a), "[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in §102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." I understand that, in inter partes review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

25. When considering the issues of obviousness, I understand that I am to do the following:

a. Determine the scope and content of the prior art;

b. Ascertain the differences between the prior art and the claims at issue;

c. Resolve the level of ordinary skill in the pertinent art; and

d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

26. I understand that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have been asked to assume is just before the earliest claimed priority date of the ’623 patent (i.e., December 3, 2003).

27. I understand that obviousness is a determination of law based on underlying determinations of fact. I understand that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of obviousness or non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the ’623 patent).

28. I understand that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also understand that a person of ordinary skill in the art is presumed to know all relevant prior art. I understand that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

29. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I understand

that the following principles may be considered, and I have been asked to consider them:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success"—not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

30. I understand that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I understand that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I understand that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

31. I understand the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I understand that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I understand it would be improper to consider only the specific problem the patentee was trying to solve.

32. I understand that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I understand that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I understand that in many fields, there

may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I understand that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

33. I understand that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine them. But I also understand that any "teaching, suggestion, or motivation" present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I understand this "teaching, suggestion, or motivation" test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

34. I understand that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

35. I understand that when there is a known technique to address a known problem using prior art elements according to their established functions, then a person of ordinary skill in the art would have had a motivation to combine.

36. I understand that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I understand that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. LEVEL OF ORDINARY SKILL IN THE ART

37. A person of ordinary skill in the art (hereinafter "POSITA") had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

38. I understand that I am to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

39. I have not analyzed the priority date of the '623 patent, but I note that the earliest claim of priority listed on the face of the '623 patent is December 3, 2003. I have also treated this date as the date from which to assess the knowledge available to a person of ordinary skill in the art.

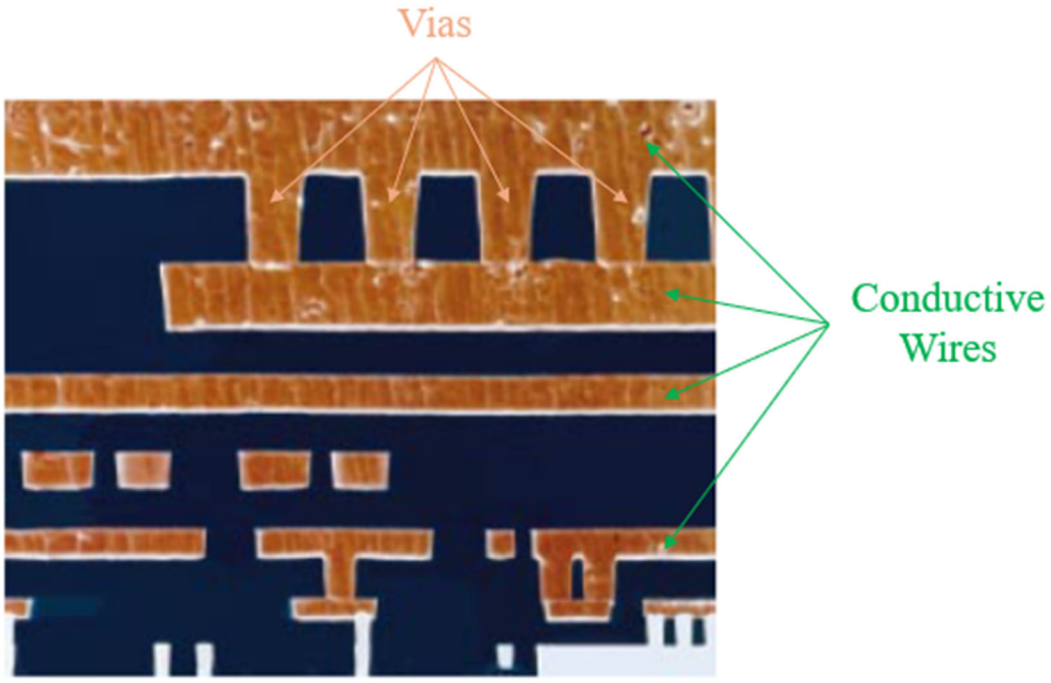
VI. TECHNOLOGY BACKGROUND

40. In my opinion, all the elements of the claims in the ’623 patent were well known before December 3, 2003.

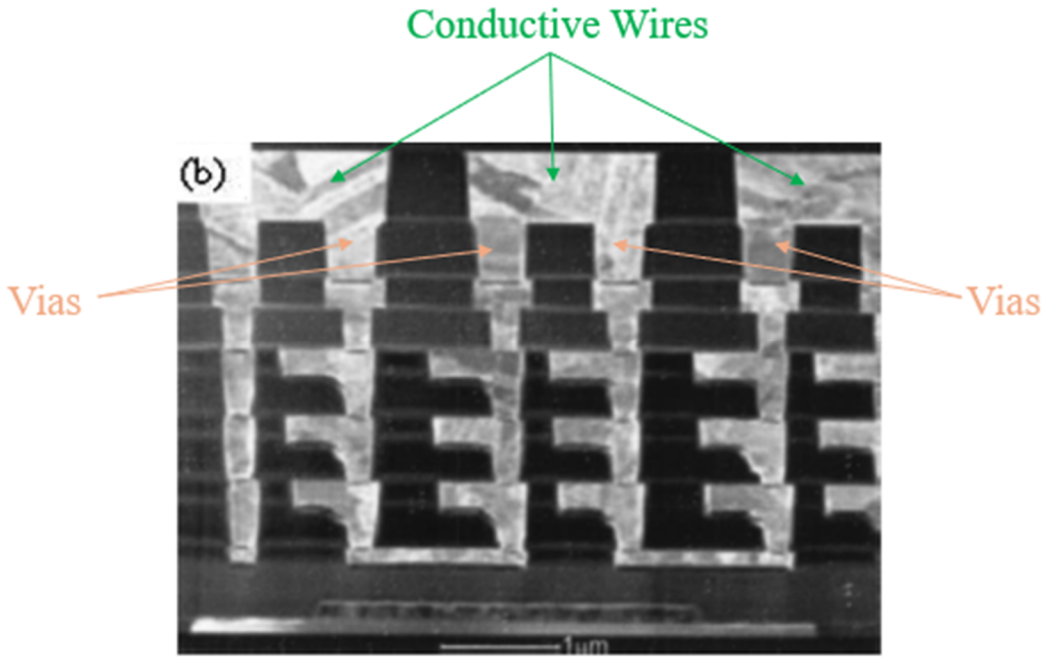
41. A person of ordinary skill in the art in the timeframe relevant to the ’623 patent would have been familiar with the background information described below.

A. Interconnects and Dual Damascene

42. Semiconductor chips have multiple levels of conductive wires (“interconnects”) for controlling chip operation, with vias connecting wires between different levels when needed. TSMC-1015, 1:13-24; *see also* TSMC-1012, 32. Aluminum and copper are known interconnect materials, with copper commonly used in VLSI interconnect metallizations. TSMC-1015, 1:13-24; TSMC-1012, 32; TSMC-1017, 2:53-58. Exemplary multi-level copper wiring structures are shown below:



TSMC-1012, 32



TSMC-1028, 5452

43. Introduced by the early 1990s, dual damascene is a manufacturing process where patterns of trenches and underlying via holes are filled with conductive metal(s) to simultaneously form the interconnects on a given level and the vias below that level. TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract; TSMC-1034, 671-76. Dual damascene is illustrated below:

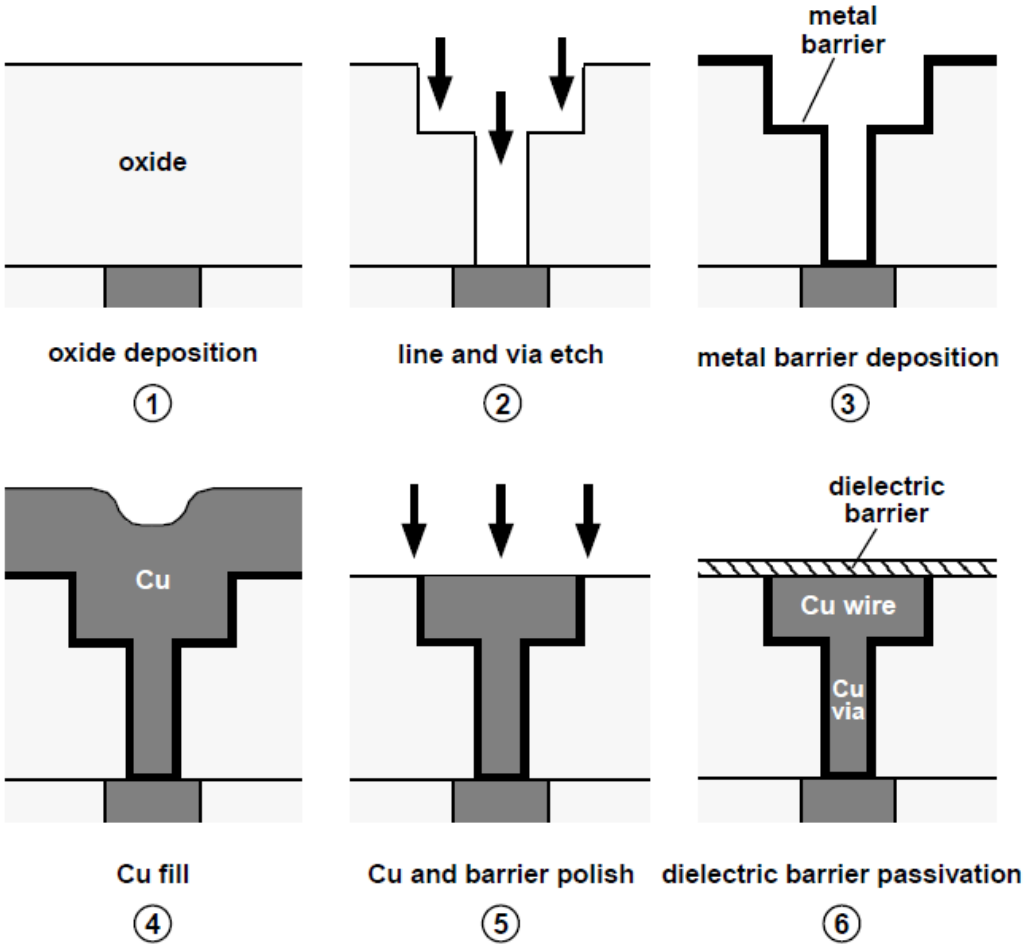


Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects.

TSMC-1027, 25. In the above process flow, step 4→5 is typically accomplished using Chemical Mechanical Polishing ("CMP"). TSMC-1034, 322-34, 675.

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength

44. Stress migration and electromigration involve the movement of metal atoms and vacancies within the interconnect structure; because vacancies tend to aggregate in/under vias, voids can form and cause electrical disconnects. TSMC-1029, 207; TSMC-1028, 5455-56, 5458-59; TSMC-1015, 1:32-37, 2:61-63. In addition, insulating films, especially low k materials, can have lower mechanical strength and poorer adhesion that makes them susceptible to damage, for example during CMP. TSMC-1016, 1:53-2:7; TSMC-1026, 583.

45. As replete in the art, dummy structures have been used well before the '623 patent for addressing these problems. For example, dummy vias have been added near active vias to arrest stress-induced vacancy migration and void formation. TSMC-1029, Abstract, 208; TSMC-1015, 2:64-3:14. Dummy structures have been known to address electromigration reliability concerns, including dummy plugs that act as reservoirs for metallic ions and reduce mechanical stress caused by electromigration. *See* TSMC-1015, 1:66-2:11; TSMC-1032, ¶¶[0012]-[0016]. Migrating vacancies/microvoids get distributed between vias and dummy vias, reducing their concentration in/under the vias. TSMC-1029, 208; TSMC-1009,

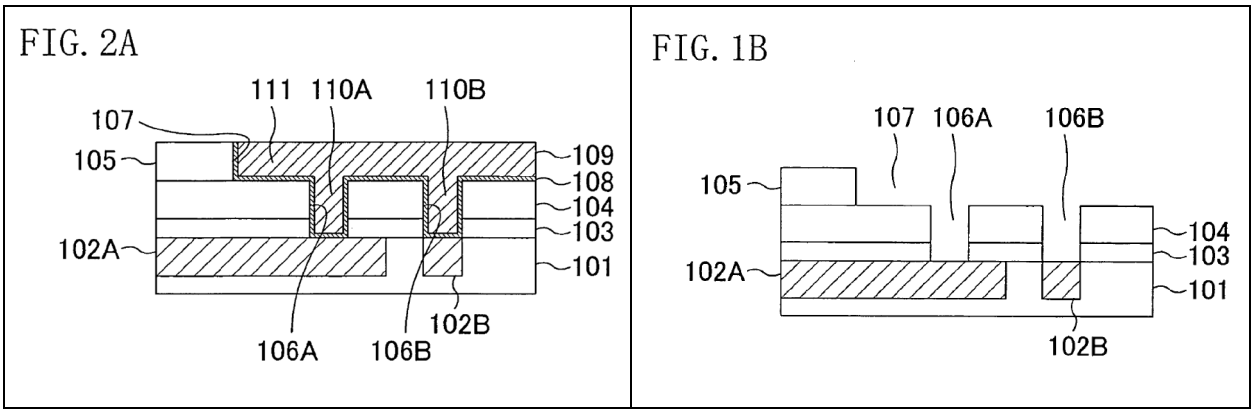
¶[0088]. Dummy vias were also well-known to improve mechanical strength, such as to prevent damage during CMP. TSMC-1016, 4:42-47; TSMC-1026, 584-85.

46. Similar to dummy vias, dummy wirings also improve mechanical properties, helping adhesion across multiple insulating layers and leading to improved planarization after CMP by reducing dishing. TSMC-1020, Abstract; TSMC-1024, 2:55-58; TSMC-1025, Abstract; TSMC-1026, 584-85. Connecting dummy wirings to dummy vias was well known to increase the mechanical strength of the combined insulating layer and upper-level wiring, as well as enhancing the durability of multi-layered insulating films during CMP and other manufacturing steps. TSMC-1011, 8:35-54.

VII. THE ’623 PATENT

A. Overview

47. The ’623 patent relates to a semiconductor device having multilevel interconnection structures. TSMC-1001, 7:47-50. A first interconnect 102A is formed in an insulating film 101, along with an optional dummy interconnect 102B. *Id.*, 10:56-63, Figs. 1A, 2B. After applying insulating layers 103, 104, and 105 on top of 102A and 102B, the dual damascene process is used to form second interconnect 111 on/in the insulation layer stack, which is connected to first interconnect 102A by via 110A:



Id., 11:5-21; 6:38-40, Figs. 1B-1C, 2A-2B. A dummy via 110B, formed in dummy hole 106B simultaneously with via 110A and interconnect 111, connects dummy interconnect 102B with second interconnect 111. *Id.*, 11:15-21; Figs. 2A-2B.

48. The first interconnect 102A, via 110A and second interconnect 111 constitute part of a closed-circuit during device operation, while neither the dummy interconnect 102B nor dummy via 110B does. *Id.*, 10:24-28. That is, the device remains operable even if the dummy interconnect 102B and dummy via 110B are omitted from the structure. *Id.*, 10:28-32.

49. According to the ’623 patent, vacancies in the copper film 109 of second interconnect 111 are divided and respectively flow into the via 110A and dummy via 110B, thereby reducing vacancies flowing into the via 110A and reducing the associated stress gradient. *Id.*, 11:36-42. The ’623 patent says this suppresses occurrences of voids in the via hole 106A. *Id.*, 11:38-45.

B. Prosecution History

50. The ’623 application was filed in the USPTO on December 2, 2004, claiming priority to a Japanese application filed December 3, 2003.

51. After a restriction and election requirement (01/05/2007), Applicant elected the figure 2B species (03/05/2007), canceled claims 1-26, and added and elected new claims 27-86 (of which claim 27 was independent). TSMC-1002, 207-19.

52. In a non-final Office Action (05/22/2007), the Examiner withdrew claims 55-56, and rejected claim 27 as anticipated by He (U.S. Patent No. 6,919,637), identifying He’s dielectric pillar 55 as the claimed dummy via. *Id.*, 240. The Examiner further rejected other claims reciting interconnect widths and via diameters and their spacing, stating that “one of ordinary skill in the art would have been led to the recited shapes, sizes and dimensions through routine experimentation and optimization.” *Id.*, 244-45.

53. Applicant responded (08/22/2007) by amending claim 27 to recite that the dummy via be made of a conductive film. *Id*., 266. In a Final Office Action (10/12/2007), the Examiner maintained the rejections, asserting that He’s copper via 68 met the recited “dummy” feature. *Id*., 285-97. Through an RCE (01/11/2008), Applicant amended claim 27 to require that the second interconnect form a dual damascene structure with each of the via and the dummy via. *Id*., 301.

54. After another non-final Office Action (02/11/2008) maintained the rejections over He (*id*., 320-29), Applicant's response (06/11/2008) amended claim 27 by removing the dual damascene limitations, and adding that the dummy via be "arranged so as to be incapable of having current flow therethrough." *Id*., 331. Applicant argued that He's via 68 is arranged to allow current to flow therethrough as part of a closed circuit. *Id.*, 340-41.

55. A Notice of Allowance (08/01/2008) followed, including an Examiner's Amendment re-inserting the dual damascene limitations into claim 27. The reasons for allowance states that the prior art "does not disclose or suggest all of the claimed elements in the present application wherein, amongst other limitations, the formed dummy vis made of a conductive film and being arranged as in the context of claim 27." *Id.*, 354-55.

56. The '623 patent issued on October 21, 2008.

C. Claim Construction

57. I have not been made aware of any specific claim construction to apply to the claims. I will apply the plain and ordinary understanding of the claims to a POSITA.

VIII. PRIOR ART

58. I have been informed that the following references are prior art as follows:

Reference	Filed	Published
Watanabe	12/4/2002 (USPTO)	6/26/2003
Hasunuma	9/3/2003 (USPTO)	6/17/2004
Iizuka	1/24/1992 (USPTO)	10/5/1993
Kurashima	8/14/2003 (USPTO)	5/9/2006
Nasu	6/24/1998 (JPO)	1/14/2000
Fujii	10/8/1997 (JPO)	8/11/1998
Kamoshima	9/9/2003 (USPTO)	9/9/2004
Fukazawa	3/29/2001 (JPO)	10/11/2002

IX. SUMMARY OF PRIOR ART REFERENCES

A. Watanabe – U.S. Patent App. Pub. No. 2003/0116852

59. Watanabe identifies the same problem of stress-related via failures in dual damascene interconnects later addressed by the ’623 patent, specifically citing stress migration leading to via lift-off (i.e., void formation) and connection failure. TSMC-1004, ¶¶[0012]-[0019], [0022]-[0024], Fig. 20 (showing voids formed by lifting up of the metal film). To address stress migration, Watanabe also proposed the same solution proposed in the ’623 patent: incorporating non-functional dummy vias formed concurrently with the functional structures using the dual damascene

process. *Id*., Abstract, ¶¶[0026]-[0028]. Watanabe further teaches that such dummy structures provide a source of copper atoms to mitigate electromigration, and enhance support for insulating film 29/second wiring 39. *Id*., ¶¶[0026], [0070]-[0079].

60. Watanabe discloses several embodiments of semiconductor devices, and discloses a method of manufacturing (Figures 12A-12N) that applies to the device embodiments. Watanabe discloses the following embodiments:

- a "first embodiment" in Figures 1-2 (*see* ¶¶[0059]-[0087]);
- a "second embodiment" in Figures 3-4 (*see* ¶¶[0088]-[0092]);
- a "third embodiment" in Figures 5A-5C (*see* ¶¶[0093]-[0108]);
- a "fourth embodiment" in Figures 6-7 (*see* ¶¶[0109]-[0114]);
- a "fifth embodiment" in Figures 8-11 (*see* ¶¶[0115]-[0133]); and
- a more generic embodiment in Figure 14 (*see* ¶¶[0171]-[0181]).

See, e.g., TSMC-1004, ¶¶[0038]-[0049], [0051].

61. As understood by a POSITA and as stated by Watanabe, like reference numbers in Watanabe's figures refer to the same structures in the first to fifth embodiments, and each figure does not necessarily show all the components. In describing the second embodiment, Watanabe states that "[i]n FIG. 3, the same reference numerals as those in FIG. 1 are affixed to the members explained in FIG.

1 and their explanation will be omitted hereunder." *Id.*, ¶[0089]. In describing the third embodiment (Figs. 5A-5C), Watanabe notes that "[i]n these figures, in order to make the planar arrangement of each plugs and the planar shape of the second wiring 39 easy to see, the underlying layer 20 (see FIGS. 1 and 3) and each insulating films are omitted." *Id.*, ¶[0094]. Regarding the method of manufacturing in Figures 12A-12N, Watanabe states that the method is applicable for manufacturing "the semiconductor device according to the embodiments of the present invention." *Id*., ¶[0135]. Regarding the embodiment of the semiconductor device in Figure 14, Watanabe states regarding its members that "[t]he underlying layer 20 in the present embodiment and each embodiments of the present invention is constructed by above members, for example." *Id*., ¶[0173]. The POSITA understands, therefore, that the same underlying layer 20 and insulating films as illustrated Figures 1, 3, and 14 exist in the Figure 5A-5C device structure, but are not shown in Figures 5A-5C figures.

62. Watanabe says the same for the fifth embodiment shown in Figs. 8 and 9: "In FIG. 8, reference numerals similar to those in the above are affixed to the members explained already in the above, and thus their explanation will be omitted here under." *Id.*, ¶[0116].

63. Watanabe teaches that the Figure 14 embodiment includes further layers built using the same manufacturing process. In introducing Figure 14, Watanabe explains that: "Although the structure of two wiring layers (the first wiring

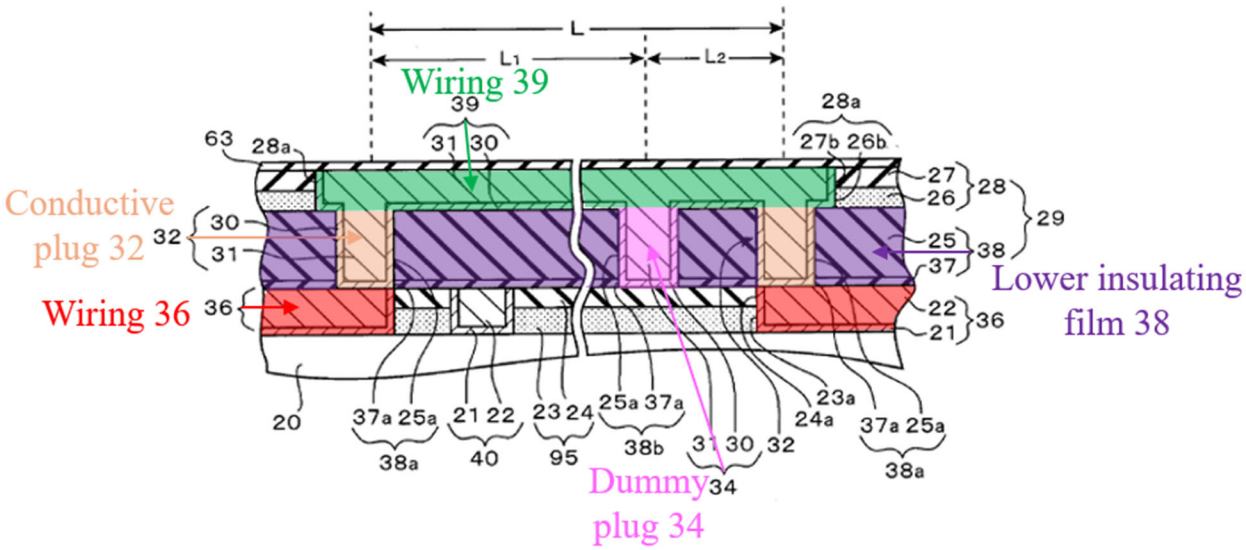
36 and the wiring 39) is obtained in the above, any number of wirings can be laminated by repeating the method same to described above. The case where four layers are laminated will be explained in the following." *Id.*, ¶[0171].

64. Watanabe describes a method of manufacturing in Figures 12A-12N, which applies to the first to fifth embodiments. Watanabe states that "a method of manufacturing the above semiconductor device will be explained with reference to FIGS. 12A to 12N hereunder. FIGS. 12A-12N are sectional views showing the method of manufacturing the semiconductor devices according to the embodiments of the present invention." *Id.*, ¶[0135]; *see id.*, ¶[0049]. This method of manufacturing is referenced earlier when Watanabe describes the first embodiment: "[a]s will be described later, this semiconductor device is manufactured by the dual damascene process." *Id.*, ¶[0072]. Further, Figures 12A-12N use the same reference numerals as earlier figures. While the specific device shown in Figures 12A-12N matches the second embodiment, the POSITA would recognize that the same overall process applies to the other embodiments – indeed, Watanabe states that "This manufacturing method is the so-called dual damascene process in which the wirings and the plugs are formed integrally." *Id.*, ¶[0135]. Watanabe also discloses that the method can be repeated to obtain any number of wirings. *Id.*, ¶[0171].

65. Figures 1-2 show Watanabe's first embodiment. It discloses a structure directly analogous to that claimed in the '623 patent. The interconnect structure

includes a wiring 36 (an interconnect), an insulating film 29 (which is made of multiple films), and a wiring 39 (another interconnect) connected to the wiring 36 by a conductive plug 32, which is a functional via. *Id.*, ¶¶[0065]-[0074], Figs. 1, 2. Crucially, it also includes a dummy via (Watanabe's dummy conductive plug 34), where the wiring 39, plug 32, and dummy plug 34 are simultaneously formed by a dual damascene process. *Id.*, ¶¶[0070], [0072], Fig. 1. See annotated Figure 1 below:

FIG. 1

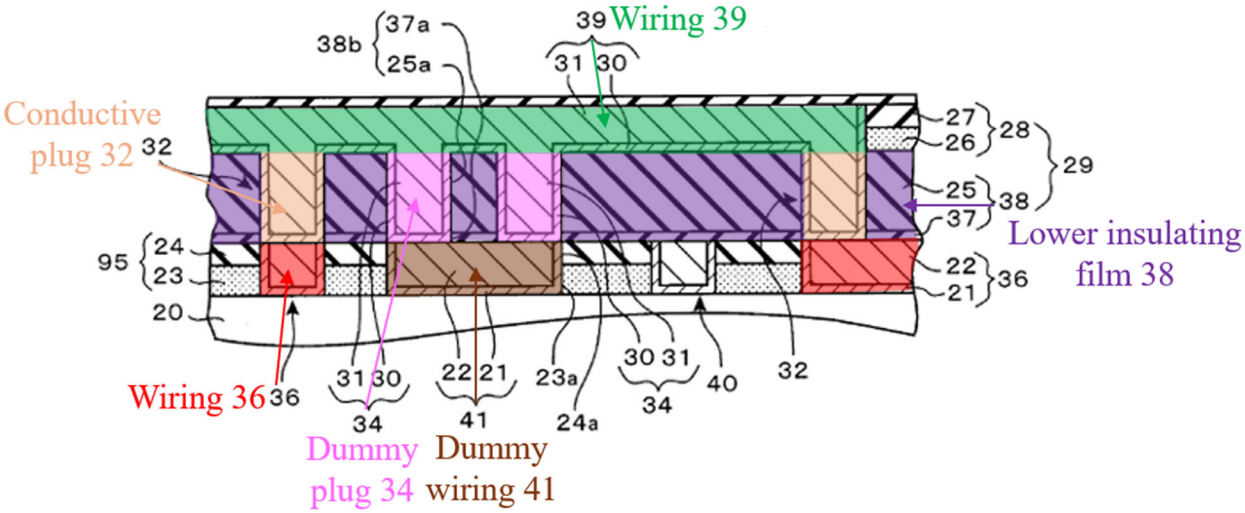


66. Conductive plug 32 connects wiring 36 and wiring 39. Like the '623 patent's dummy via 110A, Watanabe's dummy via 34 connects to the second interconnect (39) above but lands on the lower insulating layer (Watanabe's first insulating film 95) in a "non-forming region" below, rendering it incapable of carrying functional current. *Id.*, Fig. 1, ¶¶[0067], [0079]. Watanabe teaches that the

dummy plugs 34 reduce stress migration problems, provide a source of copper atoms to mitigate electromigration, and enhance support for insulating film 29/wiring 39. *Id*., ¶¶[0026], [0028], [0070]-[0079], [0091]. Watanabe describes its interconnects using the term "wiring" (e.g., "wiring 36," "wiring 39," "wiring 51"). A POSITA understood that such wirings constitute "interconnects" as those terms are understood in the art because a wiring is a structure formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g*., TSMC-1001, 1:20-27. Wiring/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g*., *id*., 1:36-38.

67. Figures 3-4 disclose Watanabe's second embodiment, which adds, among other structure, a dedicated, isolated dummy wiring 41. TSMC-1004, ¶¶[0028], [0090]-[0091], Fig. 3. See annotated Figure 3 below:

FIG. 3

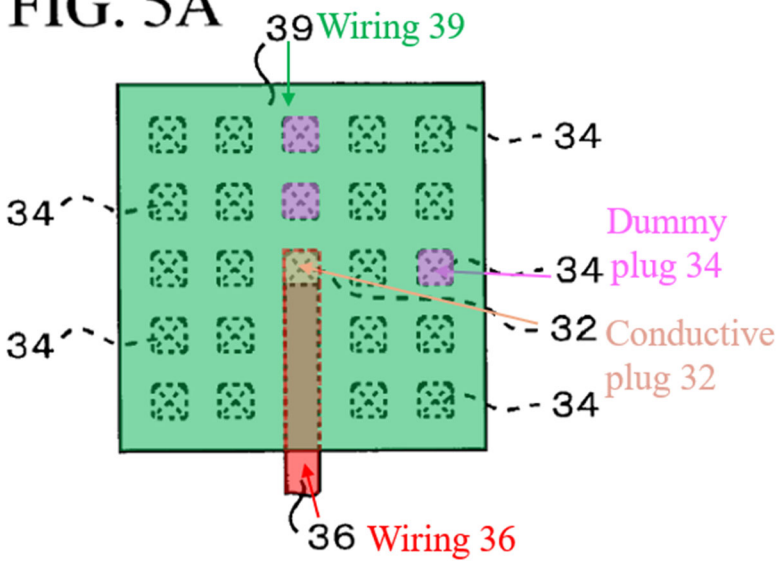


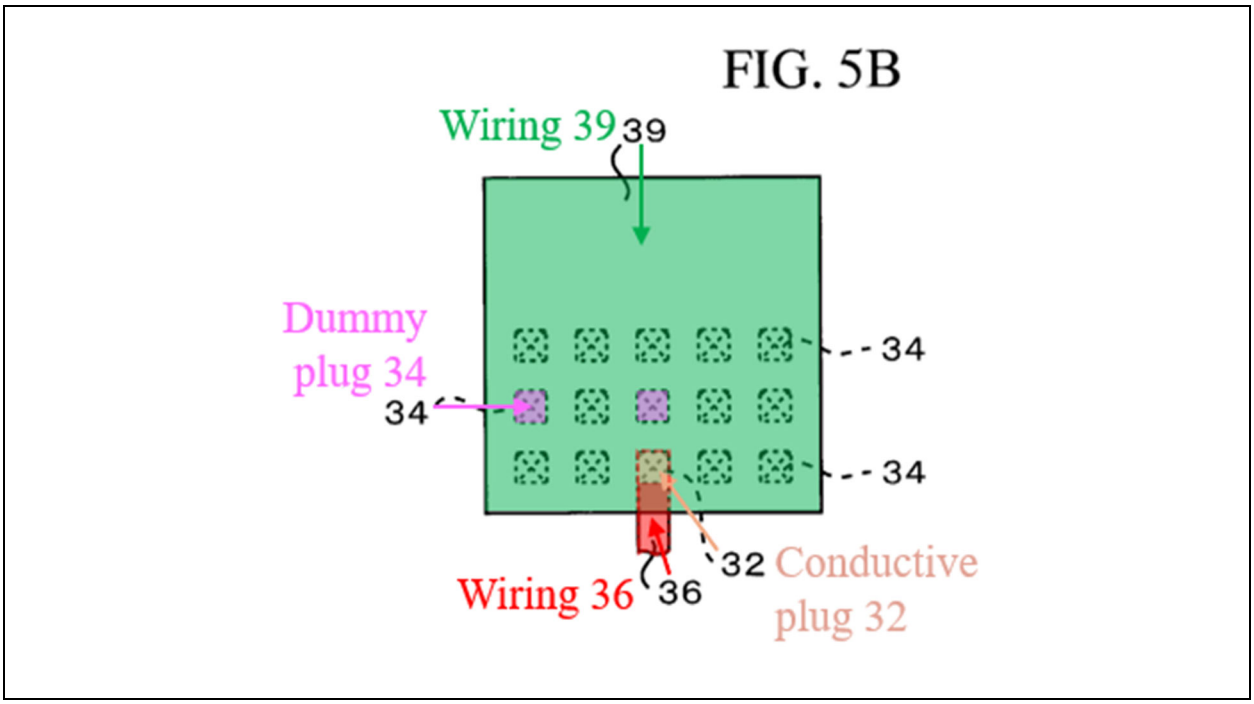
68. The dummy wiring 41 resides in the same insulating film 95 as wiring 36. *Id*., Fig. 3. Watanabe teaches that this structure adds mechanical strength and uniformity during CMP. *Id*., ¶¶[0028]-[0029], [0090]-[0091]; Figs. 3-4. Watanabe's dummy wiring 41 is directly analogous to the '623 patent's "first dummy interconnect" and resides in the same lower insulating layer (Watanabe's insulating film 95) as the functional first interconnect (36). *Id*., Fig. 3. Watanabe teaches that this structure adds mechanical support and uniformity during CMP. *Id*., ¶¶[0028]-[0029], [0091].

69. Figures 5A-5C disclose Watanabe's third embodiment. Watanabe's third embodiment is the same as Watanabe's first and second embodiments in relevant part, with Watanabe's third embodiment showing that the shape of the wiring 39 can be varied, along with the position of plug 32 and the positions and

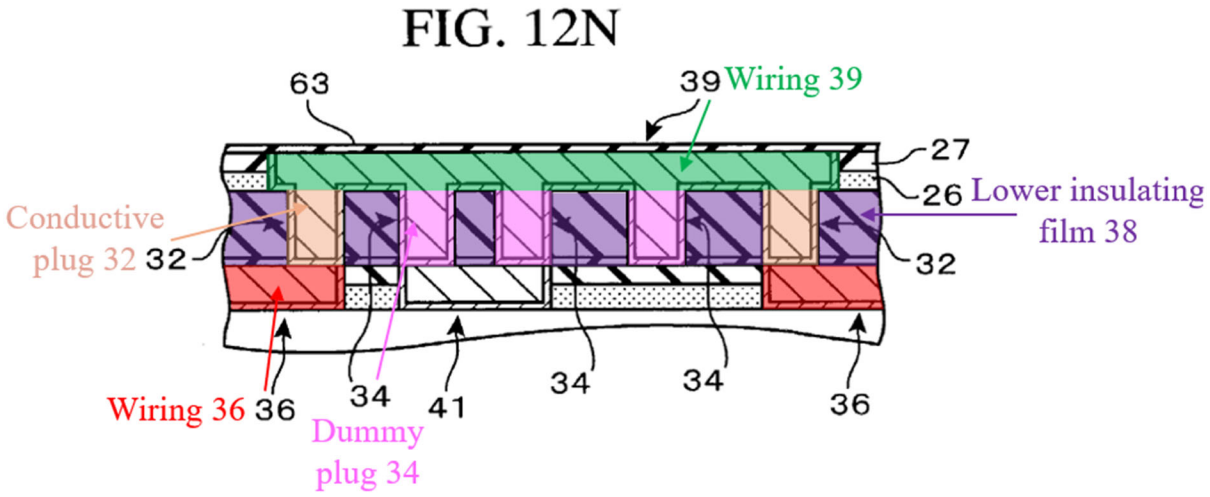
number of dummy plugs 34. *Id.*, ¶¶[0093]-[0099], Figs. 5A-5C. Watanabe's third embodiment is the same in relevant respects as the first and second embodiments, with the third embodiment showing an alternative shape for the wiring 39 and different positions of plug 32 and different positions and numbers of dummy plugs 34, as exemplified in Figures 5A and 5B below:

FIG. 5A





Id., ¶¶[0093]-[0099], Figs. 5A-5C. In Watanabe's Figures 5A-5C, a POSITA would have understood that each of the hatched squares not otherwise labeled as a conductive plug 32 constitutes a dummy plug 34, even though I highlight only a few exemplary dummy plugs 34 in the above annotations. *Id.*, ¶¶[0096]-[0098]. Also, given Watanabe's express statement that Figure 12 represents "sectional views showing the method of manufacturing the semiconductor device according to the embodiments of the present invention," (*id.*, ¶¶[0049], [0135] (emphasis added); *see also id.*, ¶[0094] (noting the omission of various layers in Figure 5 for easier understanding)), a POSITA understood that the cross-section of Figure 12N discloses the basic structure of Watanabe's third embodiment (e.g., Figure 5B):

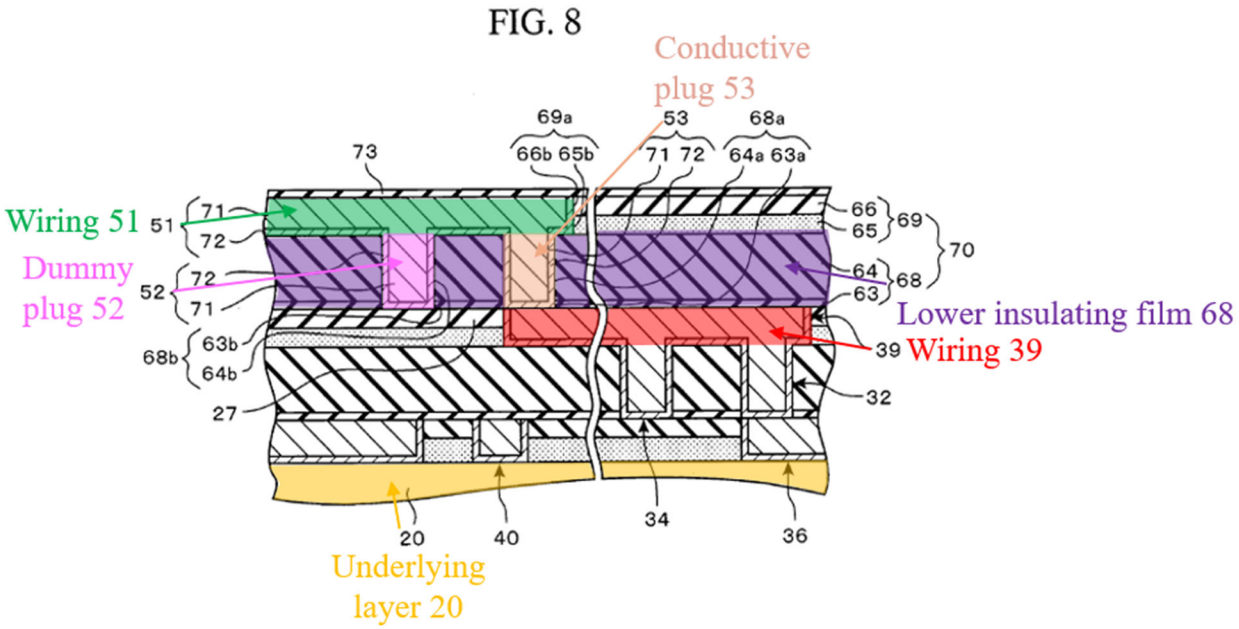


70. Figures 8-9 depict Watanabe's fifth embodiment. Watanabe's fifth embodiment illustrates a semiconductor device having a three-level interconnect structure, as disclosed in Figure 8 (cross-section) and Figure 9 (plan view). *Id.*, ¶¶[0115]-[0133], Figs. 8-9. In Watanabe's fifth embodiment, the same numbers identifying the same elements as previously described with respect to Figures 1-5 are applicable to Figures 8-9.

71. As with the first-through-third embodiments, Watanabe's fifth embodiment structure is formed on a semiconductor substrate that is part of the underlying layer 20. *Id.*, ¶[0136], Fig. 8; *see also id.* ¶¶[0172]-[0173], Fig. 14 (showing the actual semiconductor devices formed in the semiconductor (silicon) substrate 96).

72. Moreover, Watanabe's fifth embodiment includes an additional interconnect level. *Id.*, Fig. 8. Watanabe's fifth embodiment includes the wiring 39,

the lower insulating film 68 and the wiring 51. *Id.* Watanabe's conductive plug 53 is a "via," formed within via hole 68a through the lower insulating film 68 and connects the wiring 51 to the wiring 39. *Id.*, ¶¶[0120], [0122], Figs. 8-9; *see also id.*, ¶¶[0172]-[0178], Fig. 14. Watanabe's dummy plug 52 is connected to the wiring 51. *Id.*, ¶[0122], Figs. 8-9. See annotated Figure 8 below:



73. The dummy plug 52 is conductive, being composed of the same barrier metal layer 72 and copper film 71 as the wiring 51, yet is arranged to be incapable of having current flow therethrough because it terminates between insulating layers 27 and 68 in a non-forming region (i.e., where there is no wiring 39) or toward an isolated dummy wiring 61. *Id.*, ¶¶[0121], [0126]-[0127], [0185]-[0186], Figs. 8-9. The dummy wiring 61 is not shown in Figure 8, but it is shown in Figure 9, and Watanabe explains that the dummy wiring 61 is formed in the same layer as the

wiring 39 and that the dummy plug 52 may be connected to this dummy wiring. *Id*. Consistent with Watanabe's overall manufacturing approach using a dual damascene process, the wiring 51 forms a dual damascene structure simultaneously with both the conductive plug 53 and the dummy plug 52. *Id*., ¶[0135], Fig. 8.

74. Figures 12A-12N disclose Watanabe's method of manufacturing a semiconductor device that is applicable to all the embodiments. *Id*., ¶¶[0049], [0072], [0134]-[0170], Figs. 12A-12N. The method uses the dual damascene process to form the wiring and the plugs integrally. *Id*. The first-fifth embodiments (Figs. 1-9) use common reference numerals as Figures 12A-12N. *Id*., ¶¶[0089], [0116], [0135].

75. Figure 14 discloses a four wiring layer embodiment, where the initial structure is like that shown in Figure 1, and then further wiring layers are formed by repeating the method from Figure 12. *See id*., ¶¶[0171]-[0181]. When introducing Figure 14, Watanabe discloses that the method can be repeated to obtain any number of wirings. *Id.*, ¶¶[0171]-[0173]. Figure 14 further discloses members in the underlying layer 20. *Id.*, ¶[0173], Fig. 14. The underlying layer 20 includes the gate electrode 84 and corresponding source/drain (S/D) regions, the interlayer insulating film 87, and conductive plugs formed from the barrier metal layer 85 and a metal film 86. *Id*. Watanabe explains that those members in the underlying layer 20 in Figure 14 apply to the other embodiments as well. *Id*.

76. Each of the disclosed first to third and fifth embodiments discloses a dual damascene structure of the interconnect with the active via and with the dummy via, respectively. Along with Watanabe's disclosure, this is evidenced by Watanabe's figures themselves. In each of cross-sectional Figures 1, 3, and 8, the wiring 39,51 is a dual damascene structure with conductive plugs 32,53 and dummy plugs 34,52, respectively. A POSITA would appreciate that Watanabe's barrier metal layer 30,72 conformally coats the outer sides of the plugs 32,53, dummy plugs 34,52, and wiring 39,51, all a single, continuous layer. With this conformal barrier layer coating, copper film 31,71 is added to fill the recesses for the plugs 32,53, dummy plugs 34,52, and trench for wiring 39,51 to form a single, unitary copper structure. A POSITA would have recognized this configuration shown in Figures 1, 3, and 8 as a dual-damascene structure, especially in view of Watanabe's description (*e.g., id.*, ¶¶[0072], [0135], [0161]-[0171], Figs. 12K-12M). A POSITA well understood the dual damascene process and its widespread general use at the time, along with motivations such as increased efficiency and reduced cost benefits. *See* TSMC-1034, 583-84, 671-76, 718, 723-26; TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-147; TSMC-1027, 25; TSMC-1028; 5458.

77. Because Watanabe is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address

(e.g., interconnect reliability), Watanabe is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1004, ¶¶[0005], [0016]-[0018].

B. Hasunuma – U.S. Patent App. Pub. No. 2004/0113238

78. Hasunuma addresses reliability problems arising from stresses inherent in interconnect structures by incorporating non-functional, concurrently formed reinforcing plugs 28, which are dummy vias. TSMC-1005, ¶¶[0079]-[0086], [0103], [0108]-[0109], [0114], [0121]-[0125], Figs. 8-9, 14. Similar to the '623 patent, Hasunuma's solution for mitigating stress-related problems involves incorporating non-functional, concurrently formed Cu reinforcing plugs 28 ("dummy vias") extending from a given interconnect. *Id.*, Figs. 8, 14.

79. In Figure 8, Hasunuma discloses a semiconductor device having silicon substrate 1, first interconnect comprising a conductive layer 14, a first insulating film including film 3, film 4, and film 2 on the conductive layer 14, and second interconnect conductive layer 26. *Id.*, ¶¶[0090]-[0111], Fig. 8. Hasunuma describes its interconnects using the term "conductive layer" (e.g., "conductive layer 14," "conductive layer 26"). A POSITA understood that such conductive layers constitute "interconnects" as those terms are understood in the art because Hasunuma's conductive layers are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from

one point to another. *See, e.g.*, TSMC-1001, 1:20-27. Conductive layers/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g.*, *id*., 1:36-38. A conductive plug 27, which is a functional via, connects the two interconnects through the insulating film (TSMC-1005, ¶¶[0101], [0108], Fig. 8), and the reinforcing plugs 28 extend from the conductive layer 26 and are each described by Hasunuma as a "dummy plug (sacrifice plug)" that do not function as wiring (*id*., ¶¶[0106]-[0109]). *Id*., Fig. 8. Hasunuma utilizes a dual damascene process for forming the conductive layer 26, plug 27, and reinforcing plugs 28. *Id*., ¶¶[0101]-[0103], [0106]-[0109]; Figs. 5-8, 14. Hasunuma uses a dual damascene process for each level, as seen in annotated Figure 8 below:

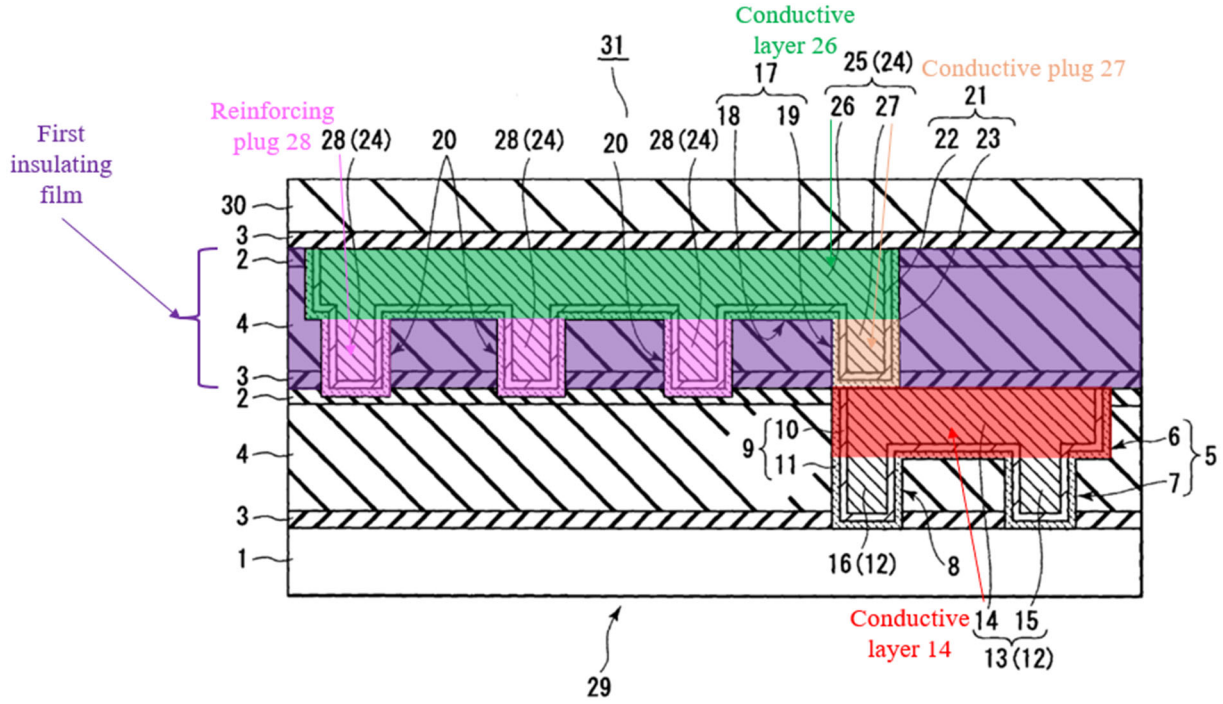


FIG. 8

Id. While not shown, Figure 14 shows similar relevant features as Figure 8.

80. Hasunuma describes forming the recess 18 for the conductive layer 26 and the recess 19 for the conductive via plug 27 together, and explicitly forms the recesses 20 for the reinforcing plugs 28 "integrally with the recess 18" for the conductive layer 26. *Id*., ¶¶[0101]-[0104], Fig. 4. All these recesses (18, 19, and 20) are then filled simultaneously with the same barrier metal film 21 (including Ta film 22 and TaN film 23) and Cu film 24. *Id*., ¶¶[0101]-[0103], [0105]-[0108], Figs. 4-6. This directly teaches the dual damascene formation of the conductive layer 26 together with the conductive plug 27 and the reinforcing plugs 28. *Id*.

81. Like the purported problem mentioned in the ’623 patent, Hasunuma addresses reliability problems arising from stresses inherent in interconnect structures. *Id*., ¶¶[0079]-[0086]; TSMC-1001, 2:19-38. Hasunuma’s solution for mitigating these stress-related issues, just as was later discussed in the ’623 patent, involved incorporating the non-functional, concurrently formed reinforcing plugs 28, which are dummy vias, adjacent to the functional conductive via plug 27. TSMC-1005, ¶¶[0114], Fig. 8. This structure was designed by Hasunuma to manage mechanical stresses and to address stress-induced phenomena. *Id*., ¶¶[0114], [0121]-[0125].

82. Because Hasunuma is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the ’623 patent purports to address (e.g., interconnect reliability), Hasunuma is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1005, ¶¶[0003], [0005], [0079]-[0086].

C. Kurashima – U.S. Patent No. 7,042,099

83. Kurashima enhances durability of insulating films, particularly low-relative-dielectric-constant films, against Chemical Mechanical Polishing (CMP) stresses to prevent film peeling in multi-layered wiring structures. TSMC-1011, 1:15-22, 1:49-67. In its first embodiment (Figs. 1A-1D, 2A-2C, 3A-3B), Kurashima teaches forming a Cu-wire 9 and a Cu-dummy wire 10 simultaneously in spaced-apart areas in a first layer interlayer insulating film 4. *Id*., 4:50-6:32, Figs. 1B-1D,

3A-3B. Then a second-layer Cu-wire 16 is formed connecting to the first-layer Cu-wire 9. *Id*., 6:58-8:35, Figs. 2A-3A. Concurrently, a second-layer Cu-dummy wire 17 is formed in contact with first-layer Cu-dummy wire 10, providing a reinforcing effect and enhancing interfacial adhesion and CMP durability, thereby reducing peeling of layers during CMP. *Id*., 6:11-32; 6:58-8:54, 9:16-23, Figs. 2C, 3A. Kurashima teaches forming functional wires and dummy wires with substantially the same width within the same layer. *Id*., 4:50-63, Figs. 1D, 3A, 3B. Annotated Figure 3A discloses these features, where each feature is colored to include barrier metal film 7:

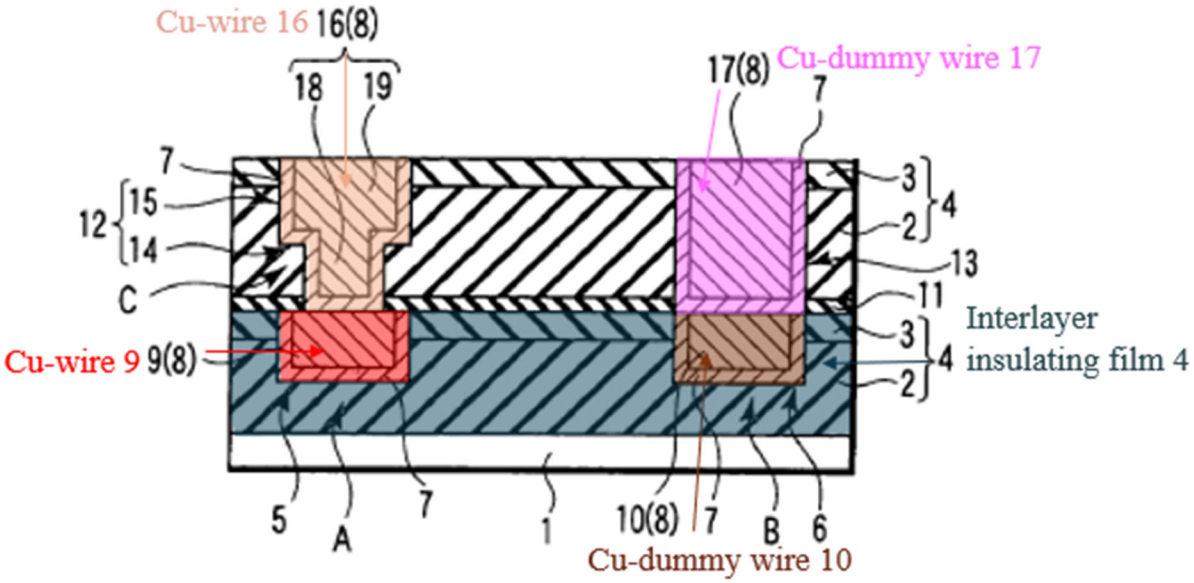


FIG. 3A

84. Because Kurashima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address

(e.g., interconnect reliability), Kurashima is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1011, 1:15-22, 1:49-67.

D. Iizuka – U.S. Patent No. 5,250,465

85. Like the '623 patent, Iizuka describes methods for manufacturing semiconductor devices, specifically focused on improving the filling of small diameter via-holes (e.g., not greater than 0.6 μm) to form reliable conductive plugs between interconnect layers. TSMC-1008, Abstract, 1:7-14, 2:39-45. Iizuka explicitly acknowledges that via-holes can have various planar configurations, stating "It will also be understood that the opening of the via-hole may have any configuration, such as a square, rectangle or circle." *Id*., 9:45-47; *see also id*., 10:17-22. A POSITA would have understood this teaching in Iizuka to refer to the shape of the via-hole viewed in plan view (i.e., from above) or as a cross-section, which then dictates the shape of the resulting via when the via-hole is filled (typically with a conductive metal such as aluminum or copper).

86. Thus, Iizuka teaches that via-holes themselves can be manufactured having various planar configurations, such as a square, rectangle or circle. *Id*. Iizuka's Example 1 describes forming a "via-hole 6 having a diameter of 0.5 micrometers" (*id*., 6:60-63), which a POSITA would have understood as disclosing and resulting in a via with a circular shape (*see also id*., Fig. 5A (showing a circular via)). Iizuka demonstrates that circular, square, and rectangular vias were known

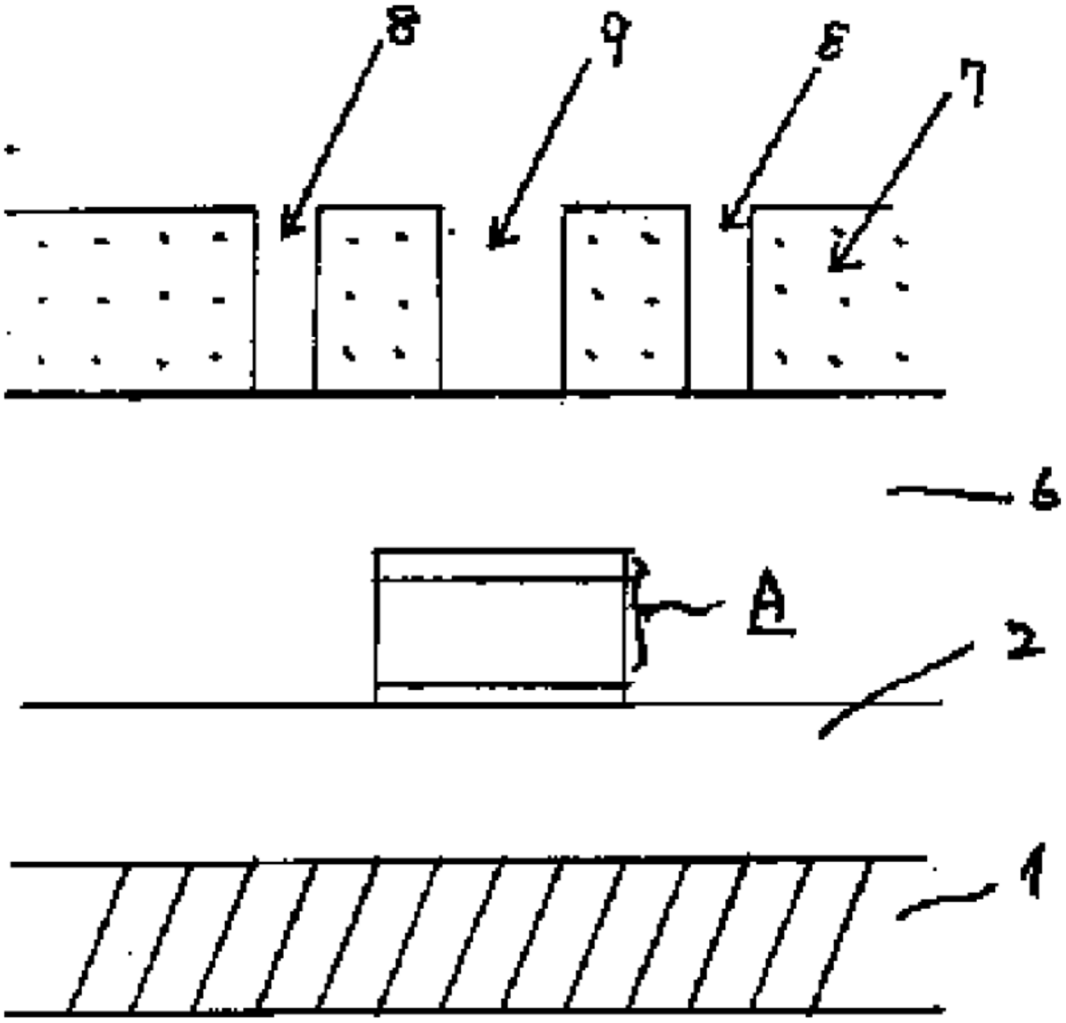
and interchangeable design alternatives, thereby teaching obvious via-shape alternatives for similar prior art structures. *Id*., 9:41-47.

87. Because Iizuka is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Iizuka is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1008, 1:7-14; 2:39-45.

E. Nasu – JP2000012688

88. Nasu discloses improving wiring reliability, specifically targeting electromigration (EM). TSMC-1032, Abstract. Nasu's wiring structure includes lower and upper wirings, where upper layer wiring B connects to lower wiring A through a via in via hole 11. *Id*., ¶¶[0022]-[0028], Figs. 1, 5. To address electromigration, Nasu teaches forming one or more dummy vias in dummy holes 10 near via hole 11, along the pattern of upper layer wiring B, to serve as a supply source for Al or Cu atoms, thereby enhancing EM resistance. *Id*., Abstract, ¶¶[0012]-[0013], Figs. 2-3.

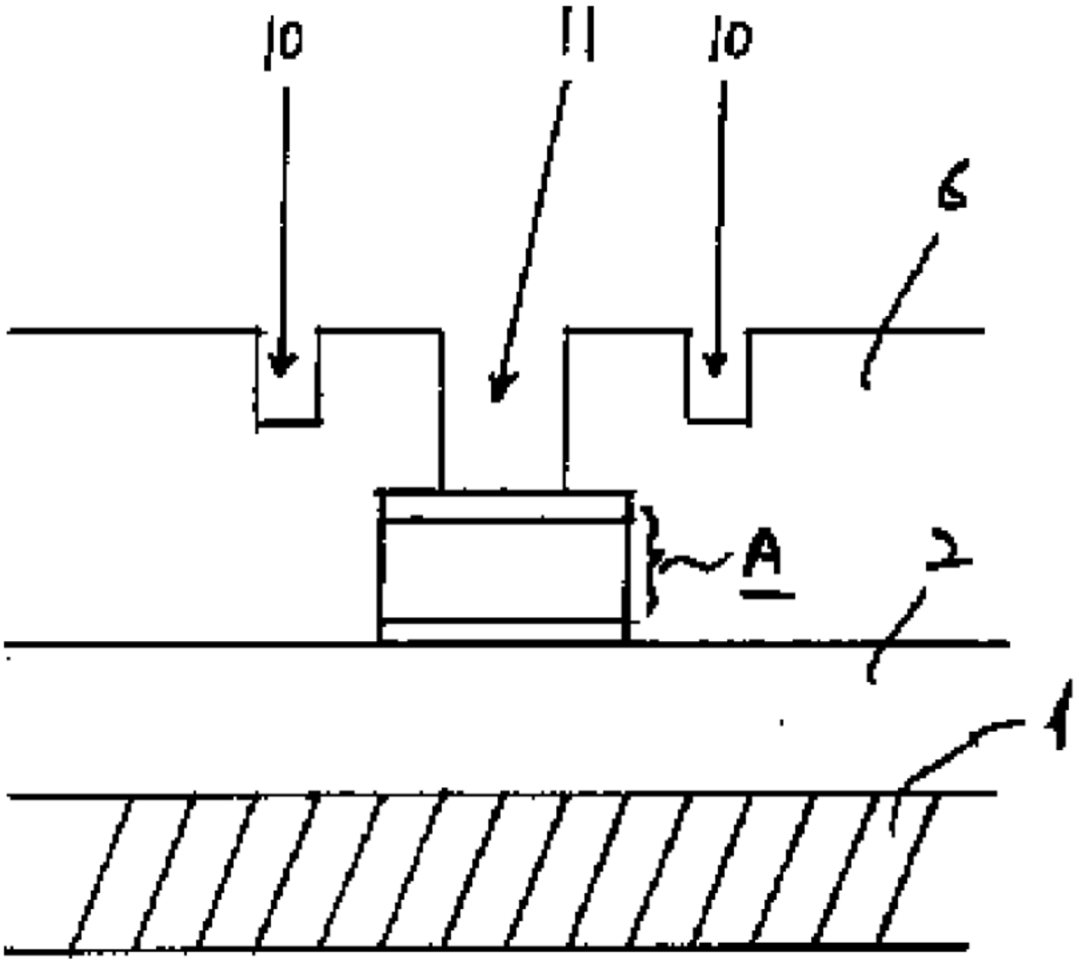
89. Nasu specifically teaches forming dummy vias that have a smaller diameter than the active via. To accomplish this, Nasu teaches using a dummy hole pattern 8 having a smaller diameter than via hole pattern 9 in the photoresist film 7, as seen in Figure 2:



Id., ¶[0023], Fig. 2. As an example, Nasu discloses hole pattern 9 having an opening with a diameter of 0.45 μm, while the dummy hole pattern 8 has an opening diameter of 0.30 μm or less. *Id*. Nasu's reference to "diameter" indicates that these via openings and vias formed in them are circular in their planar shape. *Id*.

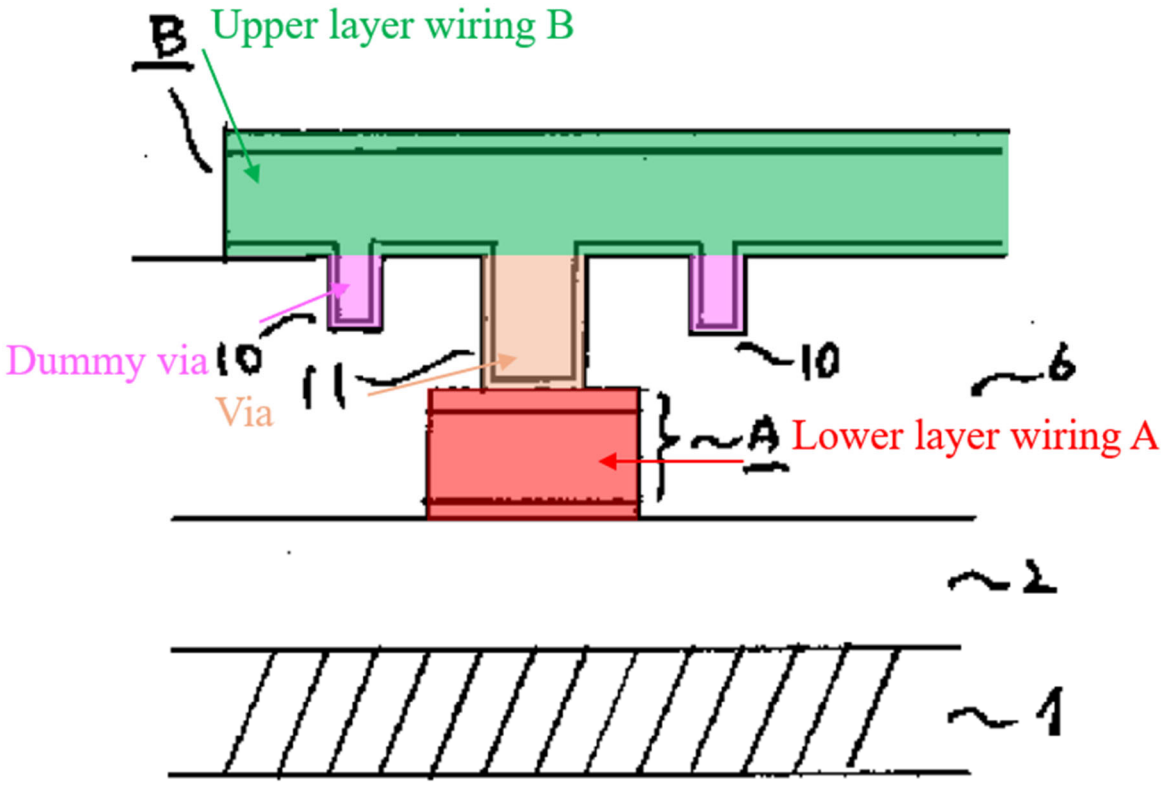
90. When the photoresist pattern seen in Figure 2 above, including photoresist hole patterns 8 and 9, is used to etch the underlying insulating layer 6, holes 10 and 11 are simultaneously etched in insulating layer 6. However, due to

the micro-loading effect during etching, the smaller diameter of dummy via holes 10 (resulting from the smaller patterned openings 8 in the photoresist film 7 as compared to opening 9) causes these dummy via holes 10 to etch more slowly, such that they end up being shallower than the via hole 11. *Id*., ¶¶[0024], [0028], Fig. 3. This is illustrated in Nasu's Figure 3:



91. As can be seen above, while via hole 11 reaches the underlying wiring A, the dummy holes 10 do not extend down to the level of lower wiring A. When the dummy via holes 10 and via hole 11 are filled with conductive metal (e.g.,

aluminum or copper), the via is formed in via hole 11 and dummy vias are formed in dummy holes 10. *Id.*, ¶¶[0012], [0016], [0026]. The resulting structure comprising an upper layer wiring B that is connected to lower layer wiring A by the via in via hole 11, and dummy vias in dummy holes 10 connected to and extending downward from upper layer wiring B that do not extend as deeply as the via in via hole 11, as seen in annotated Figure 5:



Id., ¶¶[0024], [0027]-[0028], Figs. 2, 3, 5.

92. Accordingly, Nasu teaches the formation of dummy vias having a smaller diameter/width than the active vias, where the dummy vias extend to a shallower depth in the underlying insulating film as compared to the active vias. *Id.*,

¶¶[0023]-[0024], Figs. 1-5. Specifically, the dummy vias are fabricated intentionally so as to not reach the underlying wiring level, unlike the active vias meant to form an electrical connection between the upper and lower level wiring layers. *Id*., ¶¶[0013]-[0014], [0017]-[0018], Figs. 1-5.

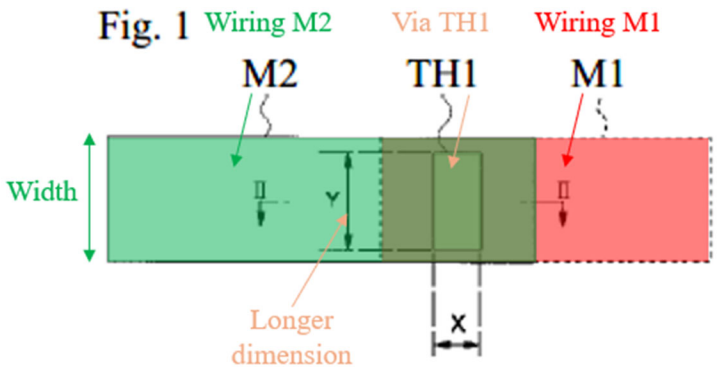
93. Because Nasu is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Nasu is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1032, Abstract ¶¶[0001]-[0002], [0013].

F. Fujii – JPH10214893

94. Fujii improves EM (electromigration) resistance in connection holes (TH1, TH2, etc.), which are vias, and their vicinity. TSMC-1030, Abstract. Specifically, Fujii teaches rectangular-shaped vias having a longer dimension in the direction orthogonal to the current flow (i.e., parallel to the interconnect width), so that current approaches the longer side dimension of the via. *Id*., ¶¶[0016], [0064]-[0066]. For current flowing in interconnects, this configuration allows current to be dispersed, suppressing local high current density. *Id*. In particular, the larger surface perpendicular to the horizontal direction of current flow distributes the current flow across the connection hole TH1, and reduces metal atom movement out of connection hole TH1, thus preventing void formation around the connection hole/via. *Id.* Fig. 1 discloses a connection hole (TH1) with a rectangular plan view,

with its longer dimension (Y) oriented parallel to the width of wiring M2. *Id.*, ¶¶[0051]-[0067], Fig. 1. Fujii, therefore, teaches the desirability of a rectangular via in which the longer dimension of the rectangular via is in the direction orthogonal to the current flow in the interconnect to which the via is connected. *Id.* Fujii further teaches that the wiring can be copper (with a barrier film) that otherwise experiences a similar problem with discontinuities. *Id.*, ¶[0197].

95. Annotated Figure 1 discloses this structure:



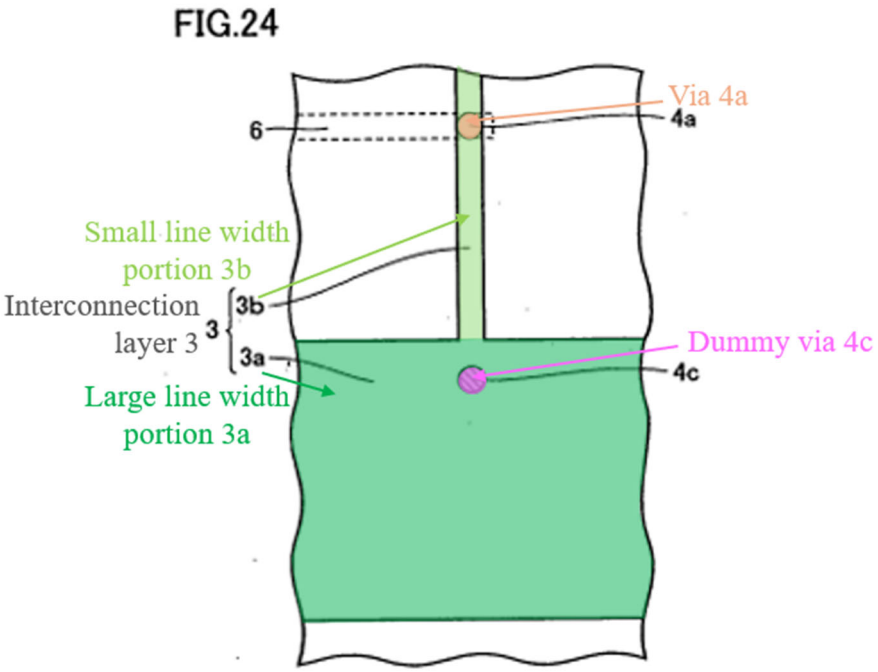
96. Because Fujii is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Fujii is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1030, Abstract, ¶¶[0001], [0009]-[0012].

G. Kamoshima – U.S. Patent App. Pub. No. 2004/0173905

97. Kamoshima discloses interconnection structures for semiconductor devices that "suppress concentration of voids in an interconnection under a via due to stress migration." TSMC-1009, ¶¶[0002], [0008]. Kamoshima teaches

interconnect structures having multiple copper interconnect levels separated by an insulator, vias connecting the interconnect layers, and one or more dummy vias. *Id.*, ¶¶[0043]-[0044], [0088]-[0090]; Figs. 16, 22. The dummy vias cause microvoids in interconnection layer 3 to distribute between a via and dummy via, suppressing the concentration of microvoids in the area under the via due to stress migration. *Id.*, ¶¶[0088], [0097]-[0098].

98. The interconnection layer 3 can have different shapes, with Figure 15 disclosing a constant width interconnection layer 3, and Figures 23-27 disclosing interconnection layer 3 having a first interconnection portion with a small line width 3b branching off a second interconnection portion with a large line width 3a. *See id.*, ¶¶[0094]-[0103], Figs. 23-27. Kamoshima teaches having via 4a (for connection to another interconnect layer) arranged along small line width portion 3b and dummy via 4c arranged in vicinity of a "connection portion" between the two interconnection portions. *Id.*, ¶¶[0095], [0099]. Annotated Figure 24 discloses these features:



99. Kamoshima further discloses that the dummy vias can be connected to the top surface of an interconnect, and that the dummy vias can be further connected at their upper end to a dummy interconnect. *Id.*, ¶[0090], Figs. 16, 22. Kamoshima shows in Figure 22 that the dummy via 4c can be connected to a top surface of the interconnection layer 3, and that a top of the dummy via 4c can be connected to the dummy interconnection layer 6. *Id.*, ¶[0090], Fig. 22. Kamoshima confirms that dummy interconnection layer 6 "does not electrically connect interconnection layer 3 to another element." *Id.*

100. Because Kamoshima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address

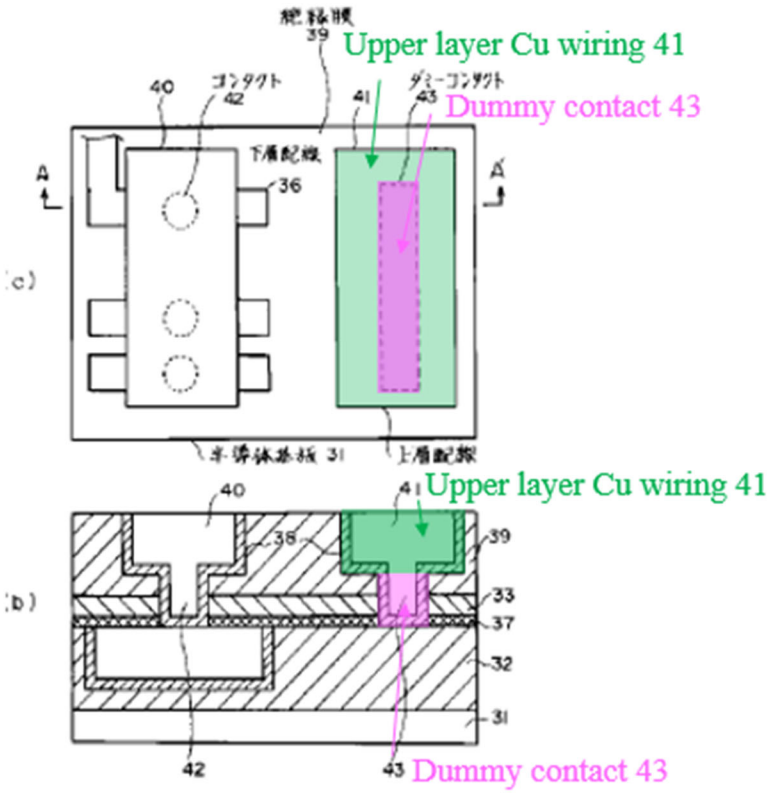
(e.g., interconnect reliability), Kamoshima is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1009, ¶¶[0002], [0004]-[0007].

H. Fukazawa – JP2002299437

101. Fukazawa is directed to a method for manufacturing a semiconductor device, including for forming Cu wiring embedded in a low-dielectric constant insulating film. TSMC-1010, ¶[0001]. Fukazawa discloses a dummy contact 43, which is a dummy via, connected to an upper layer interconnect ("upper layer Cu wiring 41"), and not connected to a lower layer interconnect. *Id*., ¶[0017], Fig. 7. To enhance mechanical strength, Fukazawa's dummy contact 43 is arranged in a substantially rectangular shape (described as "column-shaped") in a plan view, shown in Fig. 7. *Id*., ¶¶[0017]-[0018] ("the dummy contacts are column-shaped"), Fig. 7.

102. Fukazawa discloses a longer side of a dummy via and a longer side of a first interconnect portion are provided along a same direction in Figure 7 where a longer side of the dummy contact/via 43 extends along a same direction as a longer side of a corresponding rectangular interconnect ("upper layer Cu wiring 41"). *Id*.

FIG. 7



103. Fukazawa teaches that, with such structure, the mechanical strength is sufficiently secured even when the insulating film is peeled off, so that the strength of the wiring structure is improved. *Id*., ¶[0018]. Thus, Fukazawa demonstrates that it was known and provides a motivation for having a rectangularly-shaped dummy via as well as positioning such a rectangular via such that its long side is parallel to a long side of an interconnect to which the via is connected.

104. Because Fukazawa is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 Patent purports to address (e.g., interconnect reliability), Fukazawa is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1010, Abstract, ¶¶[0001], [0004]-[0007].

X. CLAIMS 5-6, 10, 19-20, 23-24, 27, 29-31, 33-38, 41, 43-44, AND 48 ARE UNPATENTABLE

105. In my opinion, claims 5-6, 10, 19-20, 23-24, 27, 29-31, 33-38, 41, 43-44, and 48 are unpatentable on the grounds outlined below:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	10, 19-20, 24, 27	102	Watanabe
1B	27	103	Watanabe
2	23	103	Watanabe + Iizuka
3	5	103	Watanabe + Iizuka + Kurashima
4	6	103	Watanabe + Kurashima
5	29-30	103	Watanabe + Nasu
6	31	103	Watanabe + Fujii
7	48	103	Watanabe + Kamoshima + Fukazawa
8	23, 27, 41, 43-44	102	Hasunuma
9	5	103	Hasunuma + Kurashima
10	6	103	Hasunuma + Kurashima + Iizuka
11	19-20	103	Hasunuma + Watanabe

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
12	24	103	Hasunuma + Iizuka
13	29-30	103	Hasunuma + Nasu
14	33-38	103	Hasunuma + Kamoshima

A. Ground 1A: Watanabe Anticipates Claims 10, 19-20, 24, and 27[1]

106. I believe that Watanabe anticipates Claims 10, 19-20, 24, and 27 as detailed below. I previously summarized Watanabe. *Supra*, §IX.A.

1. Claim 1[2]

107. Watanabe's first embodiment is applied to the elements of claim 1 immediately below, and then the subsequent sections apply Watanabe's other embodiments to claim 1 thereafter.

a) Watanabe's First Embodiment Discloses Claim 1

(1) [1.pre] – "*A semiconductor device*"

108. The preamble of claim 1 calls for a "semiconductor device," which Watanabe discloses. As examples, Figures 1, 12A-12N, and 14 each disclose a

[1] *See* Appendix B for all challenged claim language.

[2] I analyze claim 1 here because the challenged claims depend from claim 1.

semiconductor device. TSMC-1004, Title, Abstract, ¶¶[0003], [0038], [0051], [0135]-[0136], [0170]-[0173].

109. Figures 1 and 14 of Watanabe, showing a semiconductor device, are reproduced below:

FIG. 1

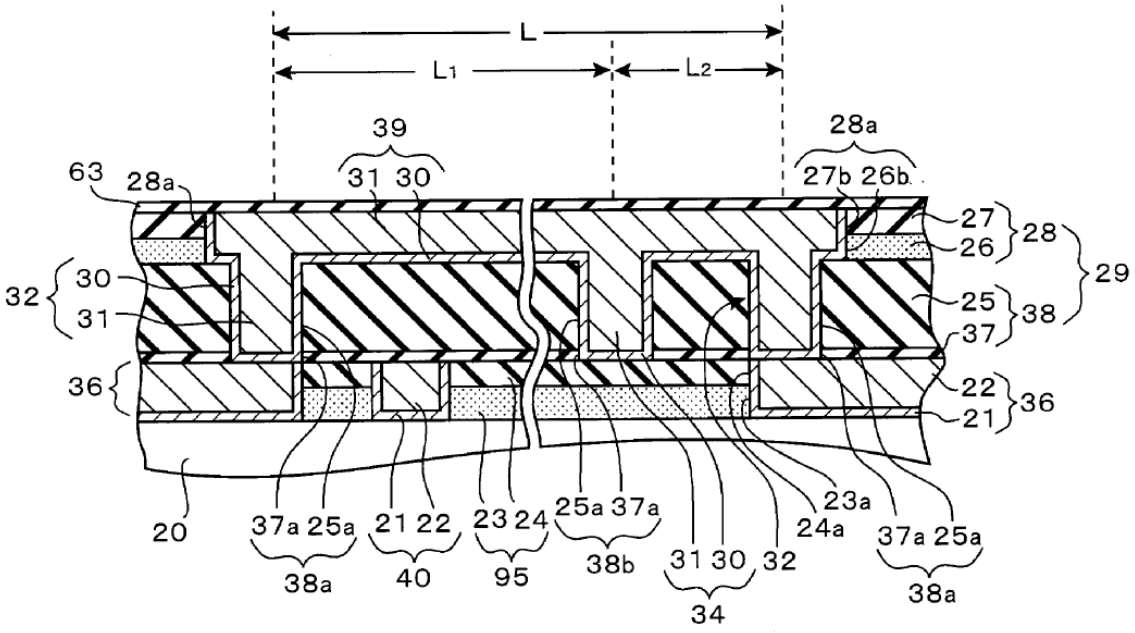
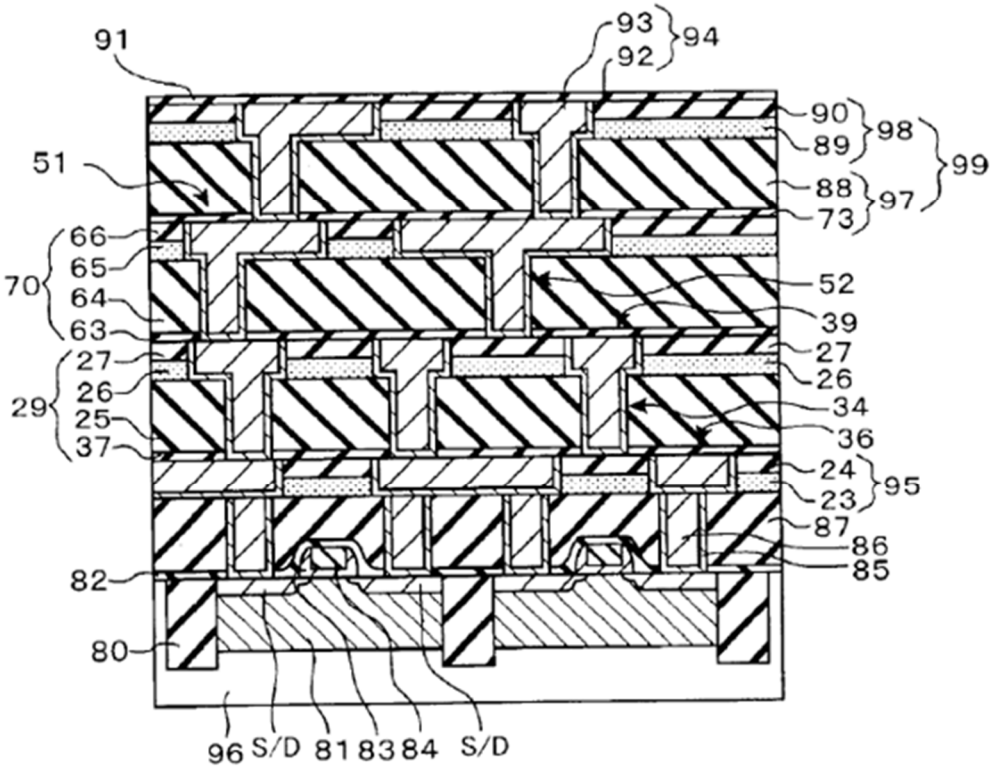


FIG. 14



See id., ¶¶[0172]-[0173] (explaining that "layer 20" in the disclosed embodiments represents or includes the devices fabricated in/on semiconductor (silicon) substrate 96, as disclosed in more detail in Figure 14).

(2) [1.a] – "*a semiconductor substrate*"

110. Element [1.a] calls for a "semiconductor substrate," which Watanabe discloses.

111. Watanabe's Figure 1 discloses structures formed upon underlying layer 20 that includes a "silicon wafer (semiconductor substrate)." TSMC-1004,

¶¶[0061], Fig. 1; *see also id.* ¶¶[0051], [0135]-[0136], [0172]-[0173], Figs. 12A, 14.

Annotated Figures 1 and 14 each disclose this feature:

FIG. 1

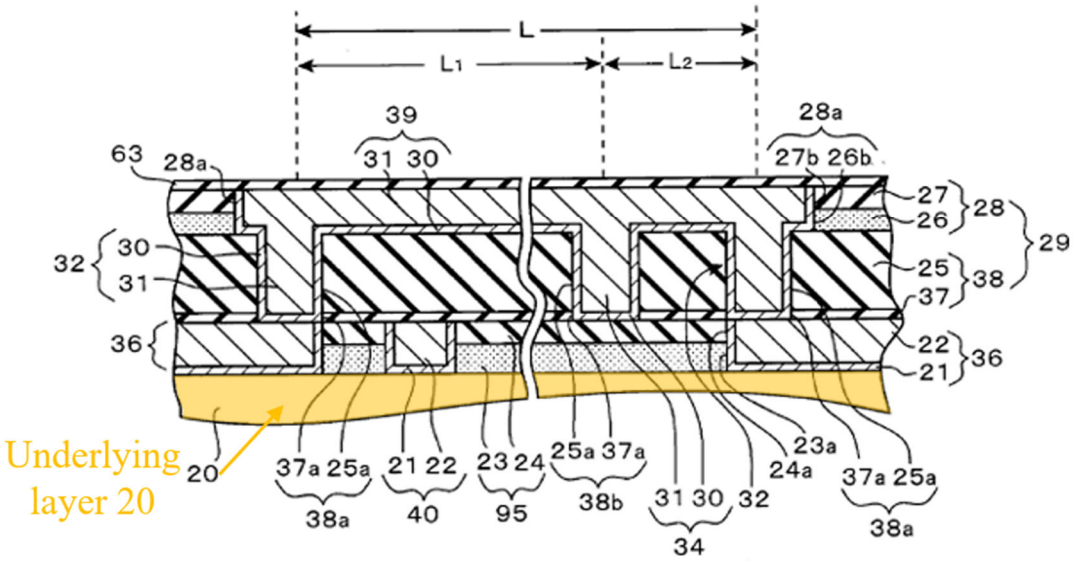
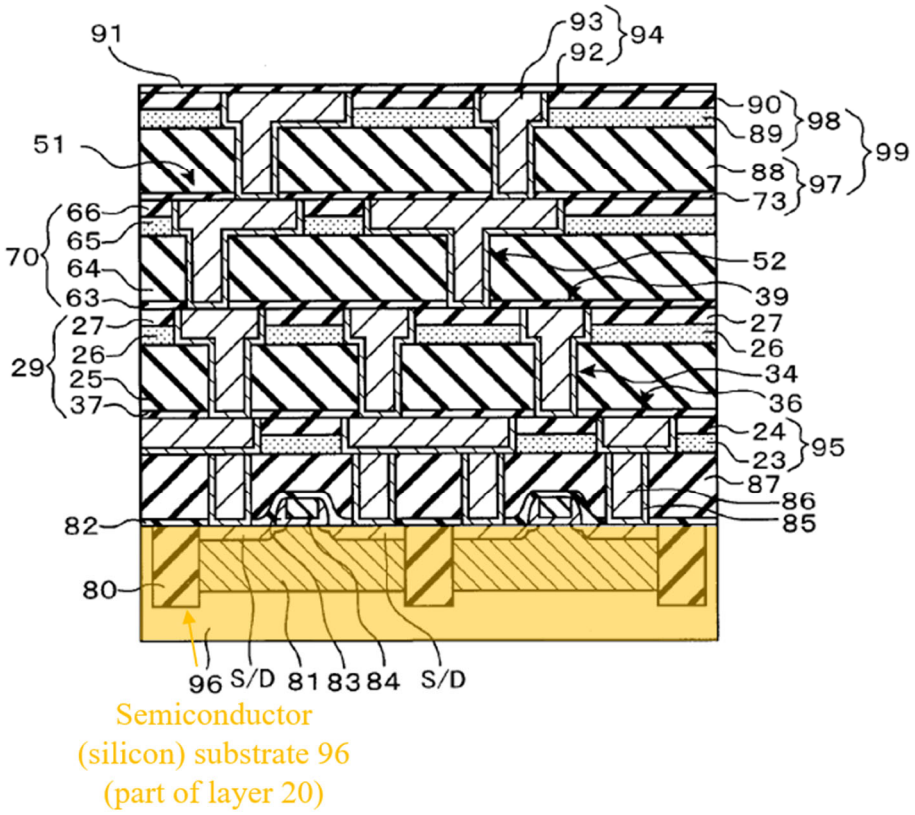


FIG. 14



Id., Figs. 1, 14 (annotated).

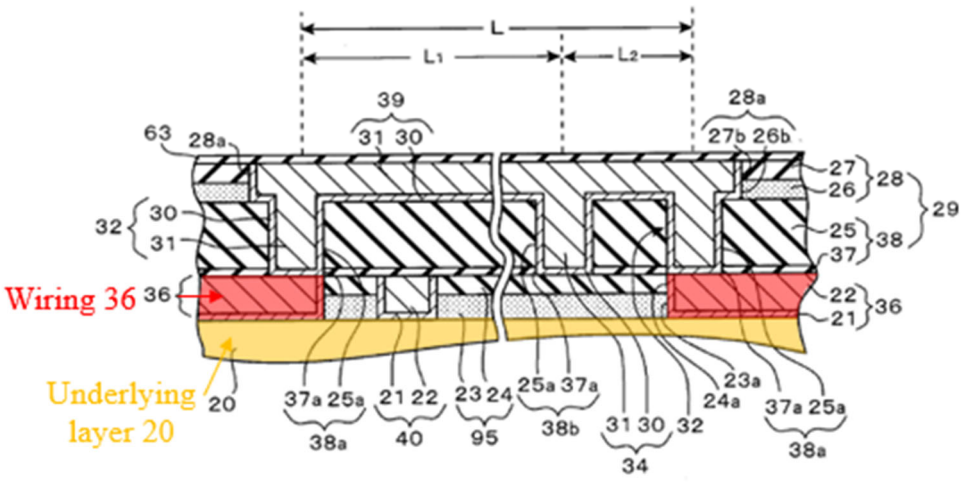
(3) [1.b] – "*a first interconnect formed on the semiconductor substrate*"

112. Element [1.b] calls for "a first interconnect formed on the semiconductor substrate," which Watanabe discloses with its wiring 36.

113. Watanabe describes its interconnects using the term "wiring" (e.g., "wiring 36," "wiring 39," "wiring 51"). A POSITA understood that such wirings constitute "interconnects" as those terms are understood in the art because a wiring

is a structure formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:20-25. Wiring/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g.*, *id.*, 1:36-38. Watanabe's wiring 36 is formed within insulating film 95, which rests on the underlying layer 20 that includes the semiconductor substrate, so the wiring 36 is an interconnect formed on the semiconductor substrate. TSMC-1004, ¶¶[0051], [0061], [0064]-[0065], [0136]-[0144], [0174], Figs. 1-9, 12A-12D, 14. Annotated Figure 1 shows these features:

FIG. 1



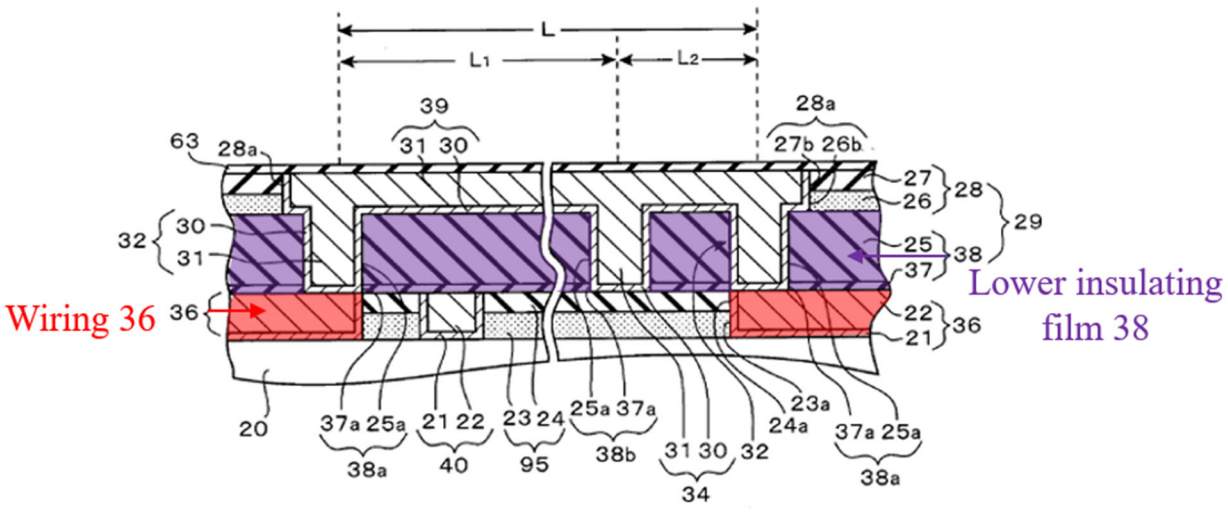
Id., Fig. 1 (annotated).

(4) [1.c] – "*a first insulating film formed on the first interconnect*"

114. Element [1.c] calls for "a first insulating film formed on the first interconnect," which Watanabe discloses with its lower insulating film 38 as one example.

115. Watanabe's lower insulating film 38 is formed on the wiring 36, as seen in Figures 1 and 14. TSMC-1004, ¶¶[0066], [0149]-[0150], [0175], Figs. 1, 3, 12E, 12M, 14. This lower insulating film 38 includes a silicon nitride film 37 and a silicon oxide film 25. It is formed on the wiring 36. *Id*. Annotated Figure 1 below shows these features:

FIG. 1



Id., Fig. 1 (annotated).

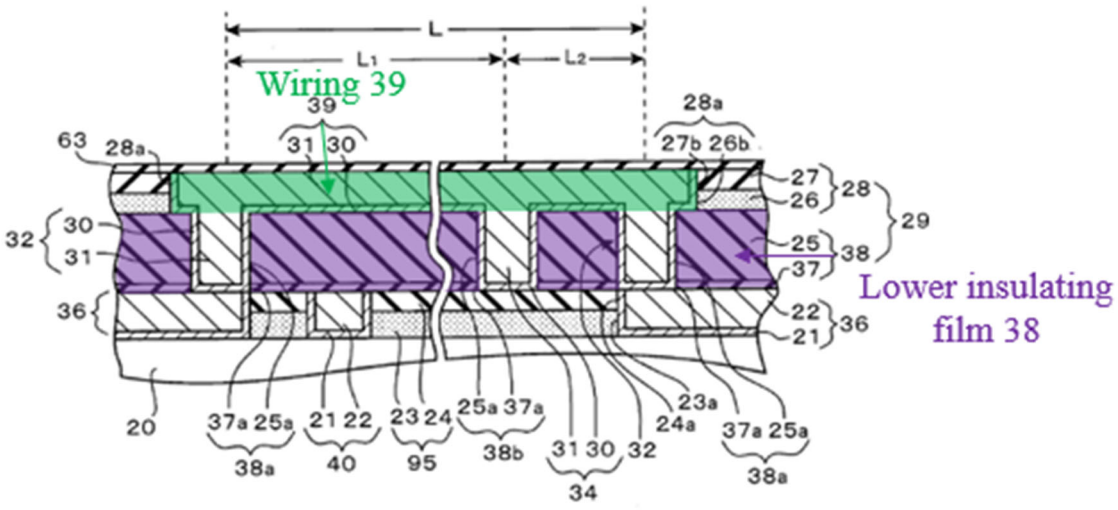
116. Additionally, for purposes of applying Watanabe to the challenged claims, the "first insulating film" could also be read on Watanabe's entire insulating film stack 29, which includes upper and lower insulating films 28 and 38. *Id*., ¶¶[0149]-[0152].

(5) [1.d] - "*a second interconnect formed on the first insulating film*"

117. Element [1.d] calls for "a second interconnect formed on the first insulating film," which Watanabe discloses with its wiring 39.

118. The wiring 39 is formed on Watanabe's lower insulating film 38 (corresponding to the claimed "first insulating film"). TSMC-1004, ¶¶[0067], [0069], [0153]-[0168], [0175], Figs. 1, 12E-12M, 14. An annotated version of Figure 1 highlighting the wiring 39 on lower insulating film 38 (the claimed "first insulating film") is reproduced below:

FIG. 1



Id., Fig. 1 (annotated).

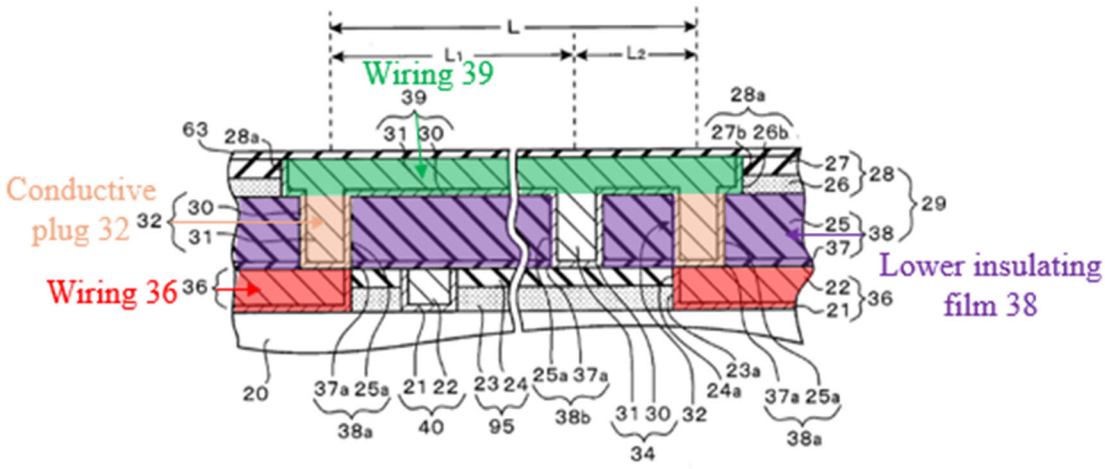
(6) [1.e] - "*a via formed through the first insulating film and connecting between the first and second interconnects*"

119. Element [1.e] calls for "a via formed through the first insulating film and connecting between the first and second interconnects," which Watanabe discloses with its conductive plug 32 formed within via hole 38a.

120. Watanabe's via hole 38a extends through the lower insulating film 38 in via hole 38a, and is filled with conductive metal to form conductive plug 32. TSMC-1004, ¶¶[0067]-[0070], [0173], [0155]-[0168], Figs. 1, 12G-12M, 14. Conductive plug 32 is thus a "via" that is through the claimed "first insulating film" (i.e. lower insulating film 38), and this conductive plug electrically connects the

wiring 36 and the wiring 39 (which are the "first interconnect" and "second interconnect," respectively). *Id.*, ¶¶[0073], [0168]. An annotated version of Figure 1 highlighting this structure is reproduced below:

FIG. 1



Id., Fig. 1 (annotated).

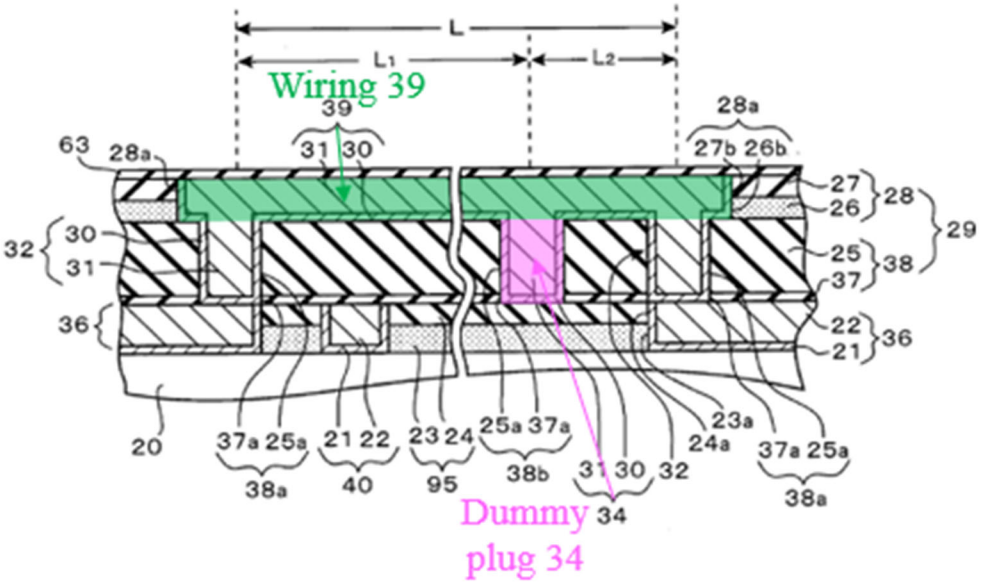
(7) [1.f] - "*a dummy via connected to the second interconnect*"

121. Element [1.f] calls for "a dummy via connected to the second interconnect," which Watanabe discloses with its dummy plug 34 formed within dummy via hole 38b.

122. Dummy via hole 38b extends through the lower insulating film 38 (which are constituted by films 37 and 25). TSMC-1004, ¶¶[0067]-[0072], [0079], [0164]-[0168], Figs. 1, 12G-12M, 14. Dummy via hole 38b is filled with conductive

metal to form dummy plug 34, which is formed integrally with the wiring 39 (using dual damascene) and thus connected to the claimed "second interconnect." *Id*. An annotated version of Figure 1 highlighting the dummy plug 34 connected to the wiring 39 is reproduced below:

FIG. 1



Id., Fig. 1 (annotated).

(8) [1.g] - "*wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough*"

123. Element [1.g] calls for "wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough," which Watanabe discloses with its dummy plug 34.

124. Watanabe's dummy plug 34 is formed integrally with the wiring 39 (using dual damascene) and includes a conductive barrier metal layer 30 and conductive copper film 31. TSMC-1004, ¶¶[0067]-[0072], [0164]-[0168], [0185], Figs. 1, 12K-12M, 14. The dummy plug 34, therefore, plainly made of conductive film. *Id*.

125. Watanabe's dummy via hole 38b extends to a "non-forming region of the first wiring 36." *Id*., ¶¶[0067], [0079], Figs. 1, 12K-12M, 14. The dummy plug 34 extends to and terminates in a "non-forming region" of insulating film 95, i.e., it is not connected to a second active circuit element such as wiring 36 or wiring 40. *Id*., ¶¶[0061], [0067], [0079], [0165], Figs. 1, 12K-12M, 14.

126. A POSITA would understand that Watanabe's "dummy plugs 34" are "arranged so as to be incapable of having current flow therethrough." In this regard, the '623 patent specification states:

> A dummy via and a dummy interconnect herein means a pseudo via or a pseudo interconnect which do not *constitute a closed circuit in actual use of a device* with an interconnection structure including these via and interconnect (i.e., **no current flows therein** during actual use of the device.)

TSMC-1001, 3:14-18 (emphasis added).

127. The '623 patent goes on to explain that:

> [N]either the dummy interconnect 102B nor the dummy via 110B constitutes a closed circuit in actual use. That is, *even if the dummy interconnect 102B and the dummy via 110B are omitted* in the interconnection structure shown in FIG. 2B, *a device with this interconnection structure is operable at least immediately after fabrication*.

Id., 10:26-32 (emphasis added).

128. Watanabe's "dummy" plugs 34 do not constitute part of a closed circuit in actual use of the device, i.e., no current flows through dummy plugs 34 during actual use of the device. As seen in Figure 1, these "dummy" plugs 34 are only connected at one end to an active element (i.e., "wiring 39"), while the other end is not connected to a second active circuit element (it instead ends at insulating film 95). A POSITA would recognize that no current flows through the dummy plugs 34 due to this lack of connection to a second active circuit element.

129. Also, Watanabe's device would still be operable if dummy plugs 34 were omitted because dummy plugs 34 do not carry current/signals as part of a closed circuit during actual use of the device. Instead, current flows between the wiring 36 and wiring 39 through conductive plugs 32, forming a closed circuit for operation of the device. TSMC-1004, ¶[0073], Figs. 1, 14.

(9) [1.h] - "*the second interconnect and the via form a dual damascene structure*"

130. Element [1.h] calls for "the second interconnect and the via form a dual damascene structure," which Watanabe discloses.

131. Watanabe discloses that the wiring 39 (which is the claimed "second interconnect) and the conductive plug 32 (which is the claimed "via") are formed using a "dual damascene process" and, thus, they form a dual damascene structure. TSMC-1004, ¶¶[0067]-[0072], [0135], [0153]-[0168], Figs. 1, 12E-12M, 14. Watanabe specifically describes the simultaneous, integral formation of the wiring 39 ("second interconnect") and the plug 32 ("via") by filling the wiring trench 28a and the via hole 38a with the barrier metal layer 30 and the copper film 31, as disclosed in Figures 12K-12M. See annotated Figure 12K,12M below:

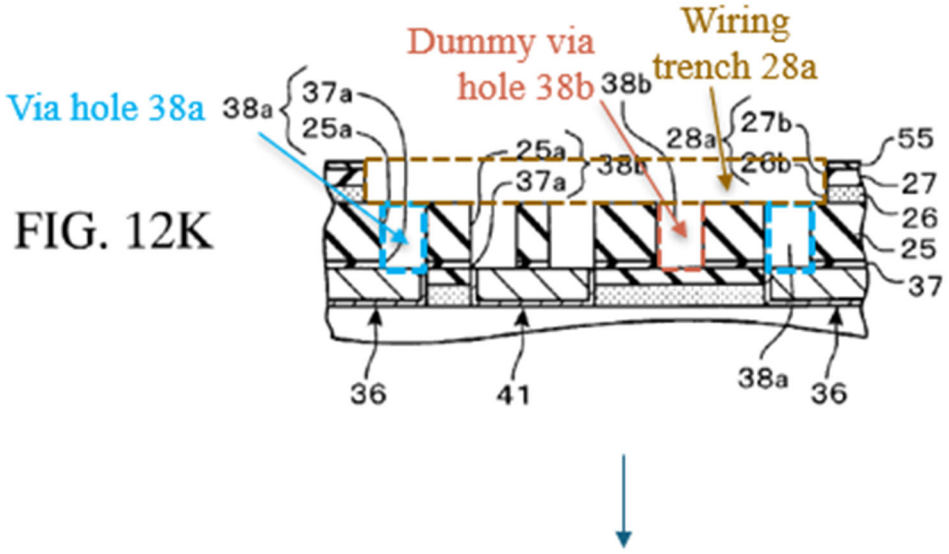
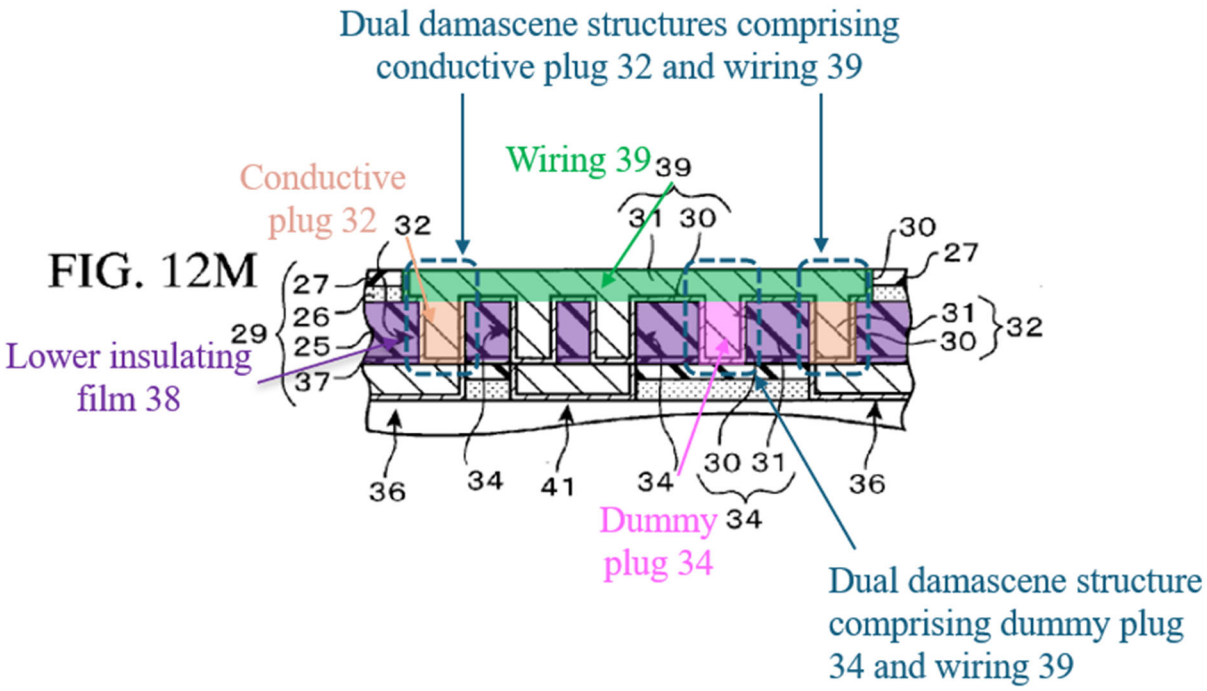


FIG. 12K



Id., ¶¶[0067]-[0068], [0072], [0166]-[0168], Figs. 12K-12M.

132. Accordingly, a POSITA would understand that Watanabe's second wiring layer 39 and conductive plug 32 (the claimed second interconnect and via, respectively) form a dual damascene structure. The same applies to the structures in Figure 14. *Id.*, Fig. 14.

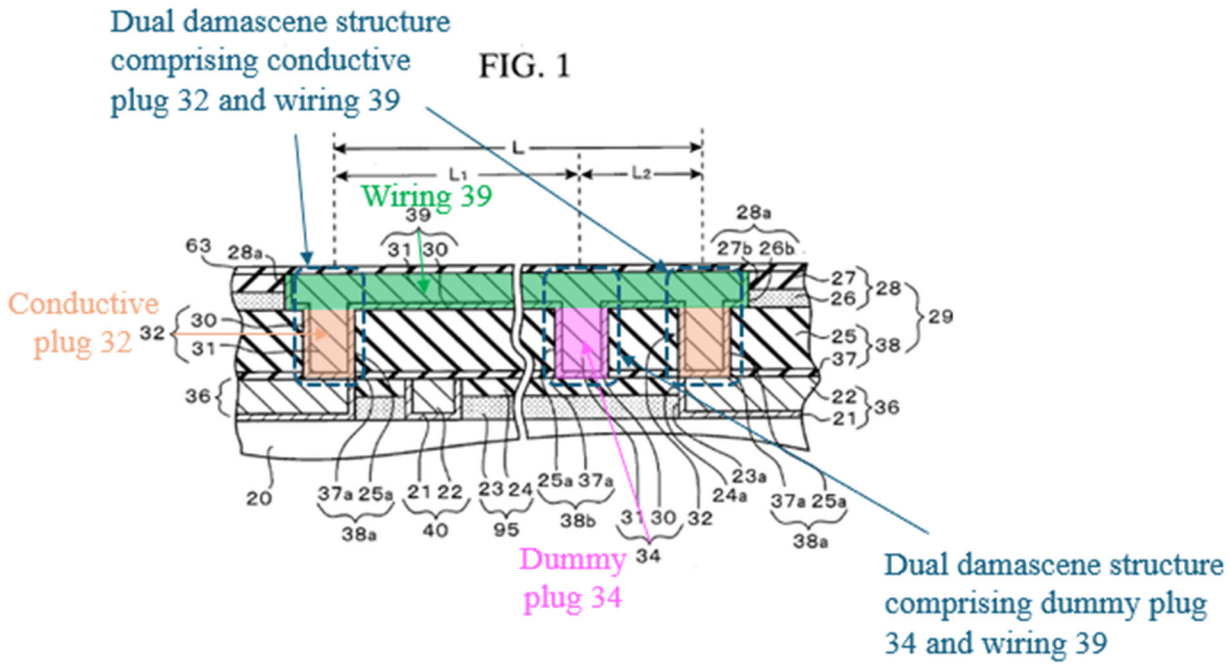
(10) [1.i] - "*the second interconnect and the dummy via from a dual damascene structure*"

133. Element [1.i] calls for "the second interconnect and the dummy via from a dual damascene structure," which Watanabe discloses.

134. The same dual damascene process already described above, in connection with element [1.h], also forms the dummy plug 34 (which is the claimed

"dummy via") simultaneously and integrally with the wiring 39 (which is the claimed "second interconnect"), by filling the wiring trench 28a and the dummy via hole 38b with the barrier metal layer 30 and the copper film 31, as illustrated above in annotated Figures 12K,12M above. TSMC-1004, ¶¶[0067]-[0072], [0135], [0153]-[0168], Figs. 1, 12E-12M, 14.

135. Annotated Figure 1 discloses the completed device, with wiring 39 and plug 32, as well as wiring 39 and dummy plug 34 forming dual damascene structures (*see also supra*, ¶76):



136. Accordingly, a POSITA would understand that Watanabe's second wiring layer 39 and dummy plug 34 (the claimed second interconnect and dummy

via) form a dual damascene structure. The same applies to the structures in Figure 14. *Id*., Fig. 14.

b) Watanabe's Second Embodiment Discloses Claim 1

137. Watanabe's second embodiment, shown in Figure 3 (cross-section) and Figure 4 (plan view) and described at paragraphs ¶¶[0088]-[0092], also discloses all limitations of claim 1.

138. Just as with the first embodiment, Watanabe's second embodiment includes a semiconductor substrate (the substrate of underlying layer 20), a first interconnect (the wiring 36), a first insulating film (the lower insulating film 38), a second interconnect (the wiring 39), a functional via (the plug 32), and a dummy via (the dummy plug 34). TSMC-1004, ¶¶[0089]-[0092], Figs. 3-4; *supra*, §§X.A.1.a.(1)-a.(10). Thus, these common features in the second embodiment meet their respective claim elements like the first embodiment.

139. In Watanabe's second embodiment, instead of the lower end of dummy plug 34 terminating at insulating layer 95 as in the first embodiment, there is an added feature that at least some of the dummy plugs 34 connect to an isolated "dummy wiring 41" at their lower end. This is seen in annotated Figures 3 and 4:

FIG. 3

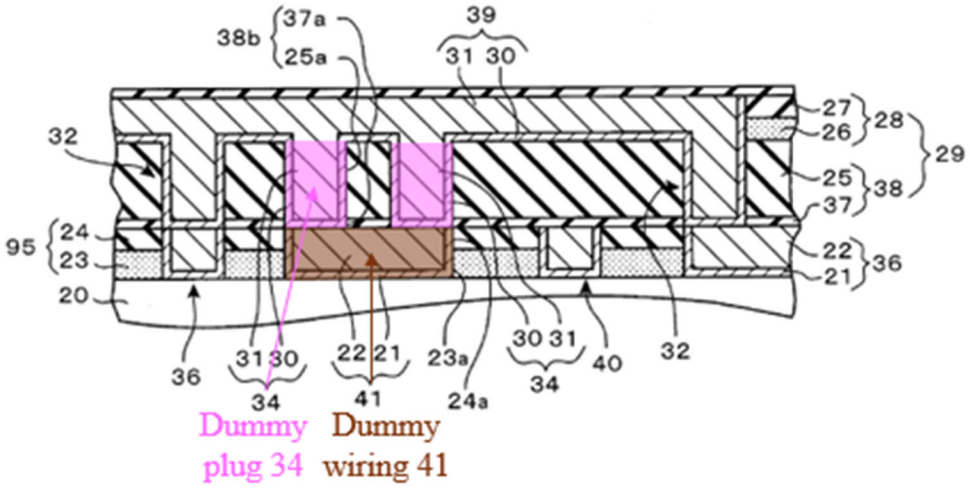
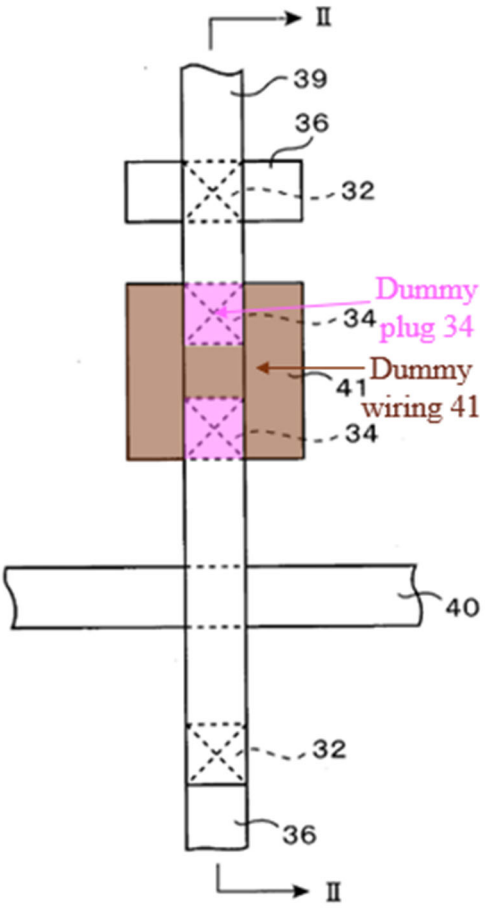

38b
37a
25a
39
31 30
27
26
28
29
32
25
38
37
95
24
23
22
21
36
20
36
31 30
34
22 21
41
23a
24a
30 31
34
40
32
Dummy
plug 34
Dummy
wiring 41

FIG. 4


II
39
36
32
Dummy
plug 34
34
Dummy
wiring 41
41
34
40
32
36
II

Id., ¶¶[0090]-[0092], [0165], [0186], Figs. 3-4, 12E, 12K-12M.

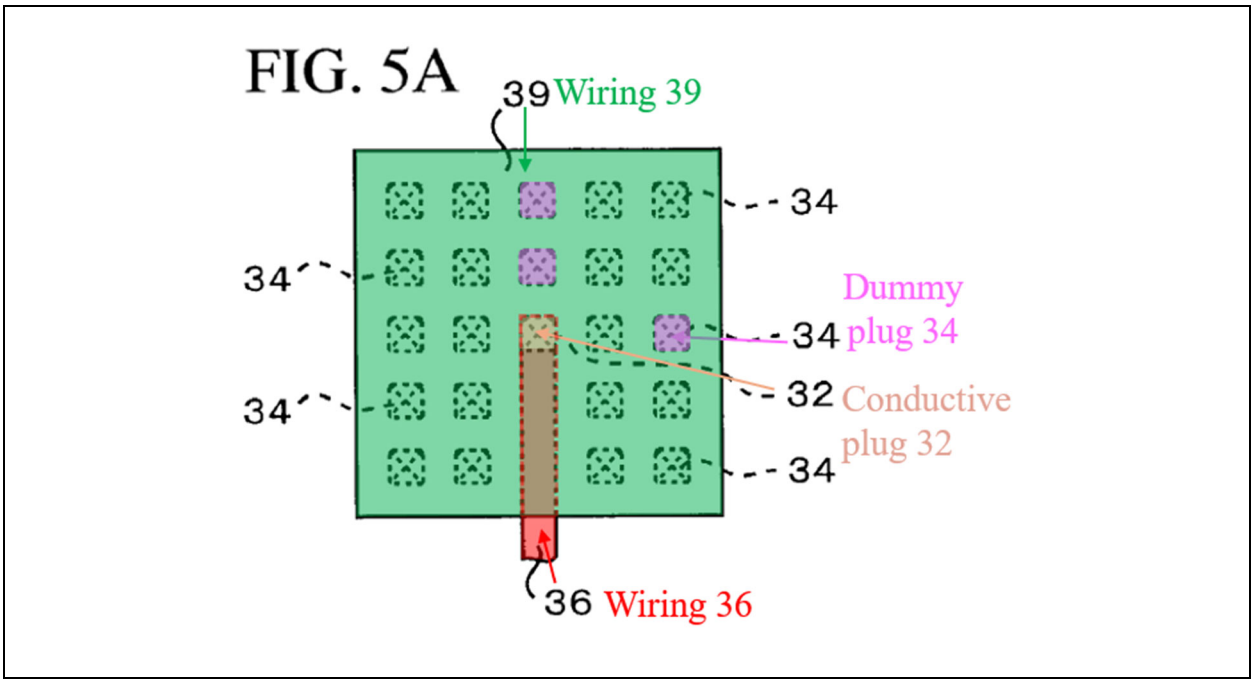
140. Just like Watanabe's first embodiment, a POSITA would understand that the "dummy plugs 34" in Watanabe's second embodiment are likewise "arranged so as to be incapable of having current flow therethrough." In this regard, the wiring 41 is itself "dummy" wiring that does not connect to any other active circuit element to form part of a closed circuit during actual device use. *Id.*, ¶¶[0089], [0135], [0166]-[0168], [0186]. As Watanabe explains, "the dummy wiring is provided in the non-forming region of the first wiring." *Id*., ¶¶[0028]-[0029], [0090], [0186]. The dummy wiring 41 is for enhancing mechanical strength. *Id.*, ¶¶[0091], [0186]-[0187].

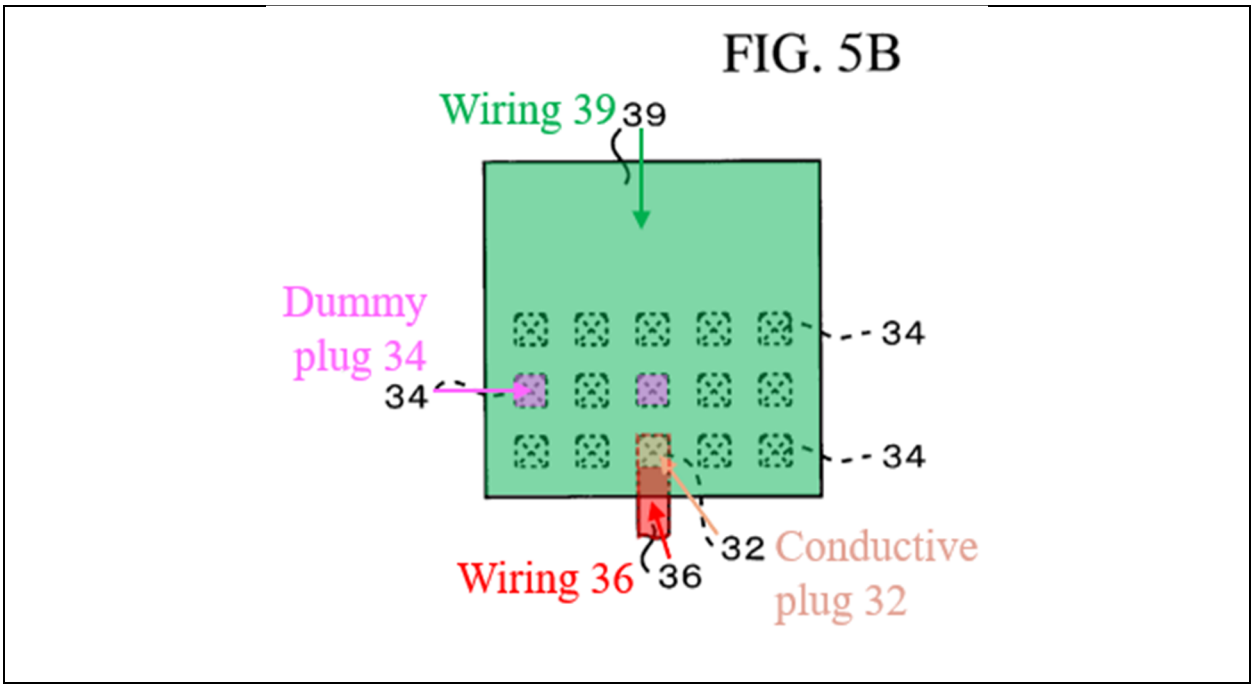
141. Additionally, both the dummy plugs 34 and dummy wiring 41 could be omitted from Watanabe's structure without affecting device operation, since the current/signals are carried between wirings 36 and 39 through conductive plugs 32 as part of a closed circuit during actual device use. *Id*.

142. Also, the second embodiment uses the same dual damascene process as with the first embodiment, resulting in integral formation of the second interconnect (the wiring 39) with both the functional vias (plugs 32) and the dummy vias (dummy plugs 34). *Id*., Fig. 3, ¶¶[0089], [0135], [0166]-[0168].

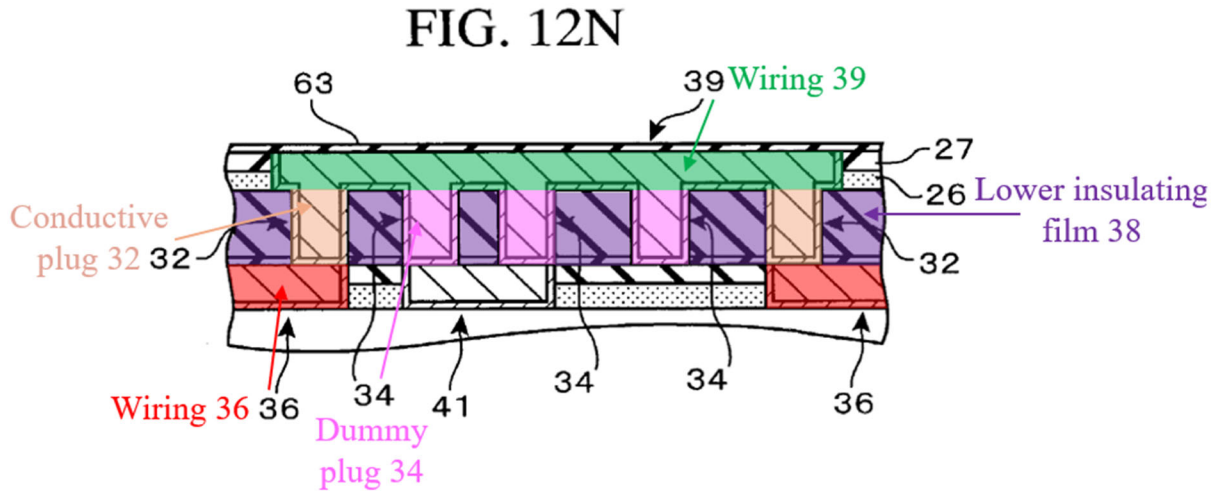
c) Watanabe's Third Embodiment Discloses Claim 1

143. Watanabe's third embodiment is the same in relevant aspects as the first and second embodiments, with the third embodiment showing an alternative shape for the wiring 39 and different positions of plug 32 and different positions and numbers of dummy plugs 34, as exemplified in Figures 5A and 5B below:





TSMC-1004, ¶¶[0093]-[0099], Figs. 5A-5C. In Watanabe's Figures 5A-5C, a POSITA would have understood that each of the hatched squares not otherwise labeled as a conductive plug 32 constitutes a dummy plug 34, even though I highlight only a few exemplary dummy plugs 34 in the above annotations. *Id.*, ¶¶[0096]-[0098]. Also, given Watanabe's express statement that Figure 12 represents "sectional views showing a method of manufacturing the semiconductor device according to the embodiments of the present invention," (*id.*, ¶¶[0049], [0135] (emphasis added); *see also id.*, ¶[0094] (noting the omission of various layers in Figure 5 for easier understanding)), a POSITA understood that the cross-section of Figure 12N discloses the basic structure of Watanabe's third embodiment (e.g., Figure 5B):



144. For the third embodiment (Figures 5A-5C), Watanabe intentionally omits depicting the underlying layer 20 and insulating films, while referencing Figures 1 and 3. *Id.*, ¶[0094]. As the foregoing figures confirm, Watanabe's third embodiment similarly discloses claim 1 for the same reasons as Watanabe's first and second embodiments.

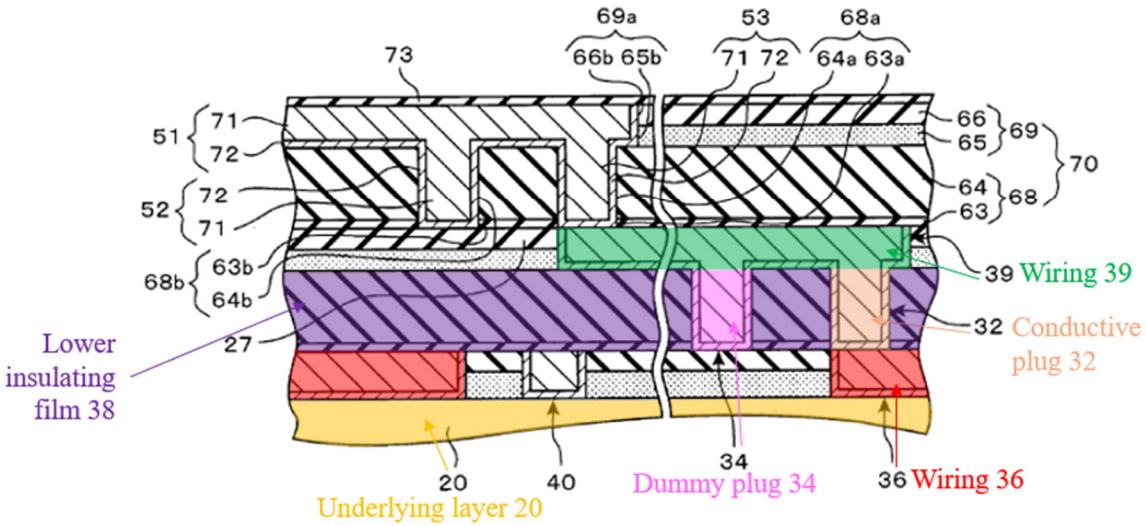
d) Watanabe's Fifth Embodiment Discloses Claim 1

145. Watanabe's fifth embodiment illustrates a semiconductor device having a three-level interconnect structure, as disclosed in Figure 8 (cross-section) and Figure 9 (plan view). TSMC-1004, ¶¶[0115]-[0133], Figs. 8-9. The fifth embodiment also discloses claim 1.

146. Watanabe's fifth embodiment includes the same structure as shown in Figure 1. Therefore, as one basis, the fifth embodiment discloses claim 1 based on

the same analysis that I laid out above for claim 1, as shown in Figure 8 below (a first mapping). *See supra*, §§X.A.1.a.(1)-a.(10).

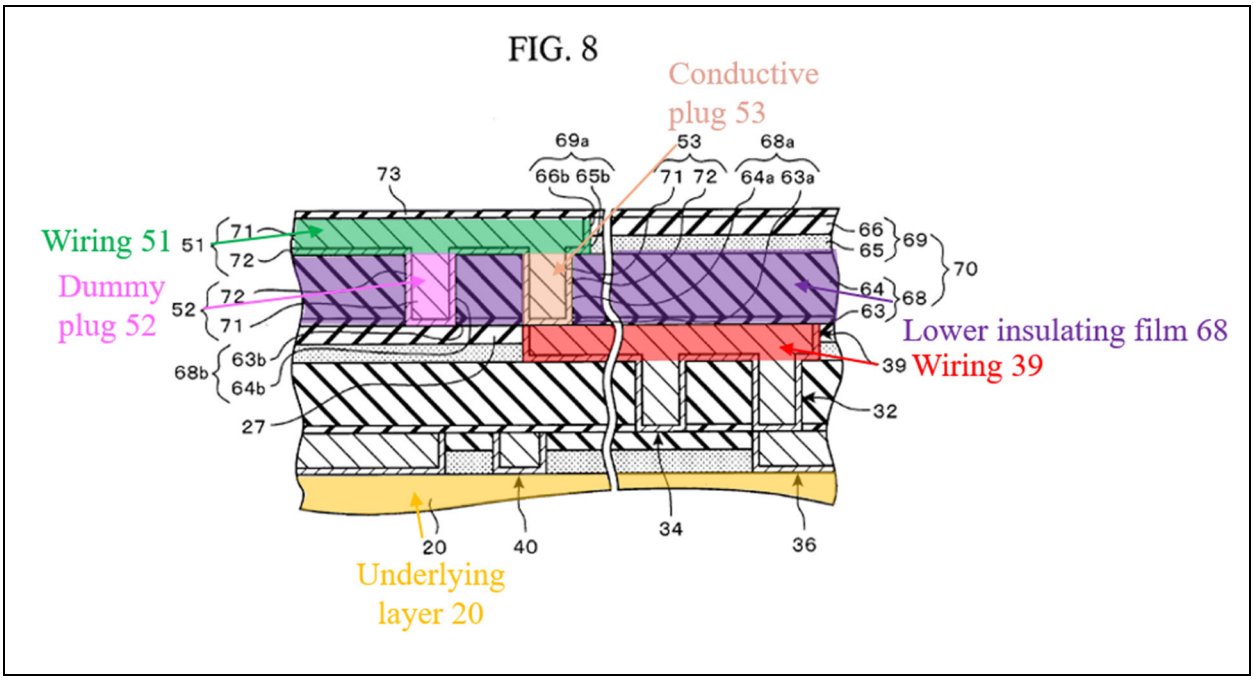
FIG. 8



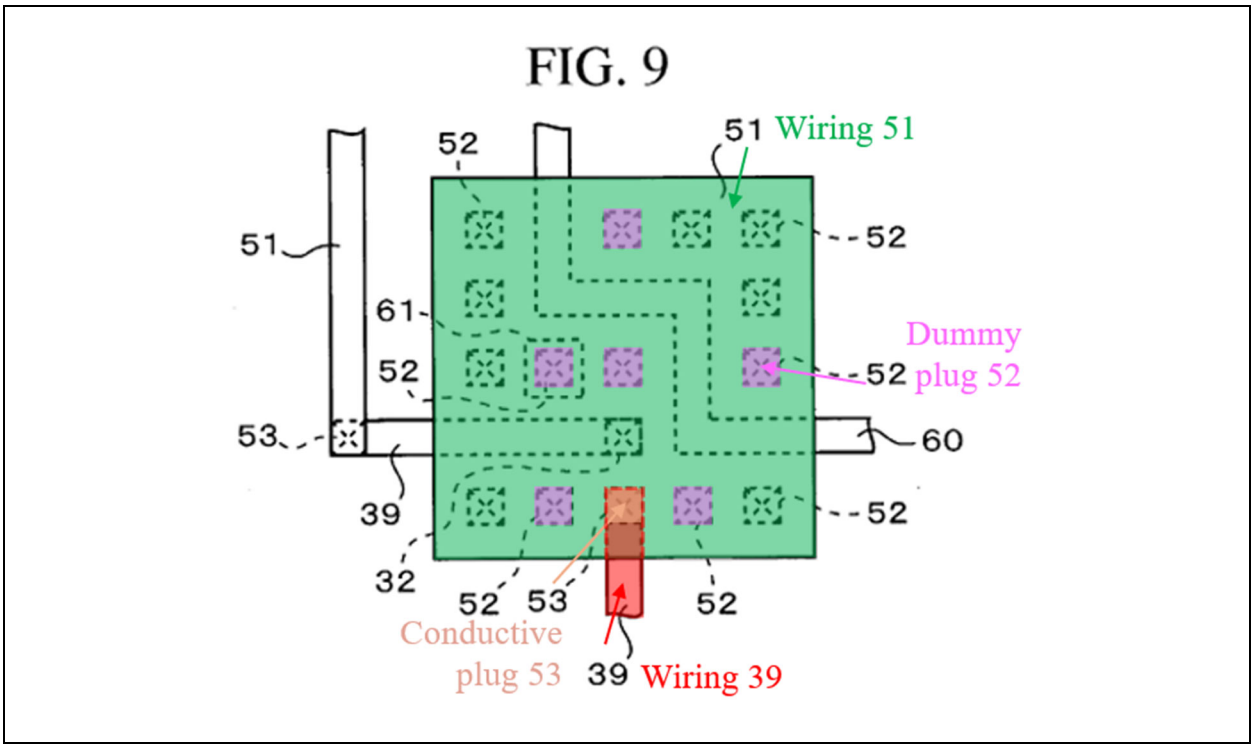
147. In addition, Watanabe's fifth embodiment includes an additional interconnect level, and the second and third level interconnect structure also discloses claim 1 as follows. To start with, Watanabe's fifth embodiment structure is formed on a semiconductor substrate that is part of the underlying layer 20. *Id.*, ¶[0136], Fig. 8; *see also id.* ¶¶[0172]-[0173], Fig. 14 (showing the actual semiconductor devices formed in the semiconductor (silicon) substrate 96).

148. In this alternative mapping, the claimed "first interconnect" corresponds to Watanabe's wiring 39; the claimed "first insulating film" corresponds to Watanabe's lower insulating film 68; and the claimed "second interconnect"

corresponds to Watanabe's wiring 51. TSMC-1004, ¶¶[0117]-[0122], [0172]-[0178], Figs. 8-9, 14. Similarly, Watanabe's conductive plug 53 is the claimed "via," formed within via hole 68a through the lower insulating film 68 and connecting the wiring 51 to the wiring 39. *Id.*, ¶¶[0120]-[0122], Figs. 8-9. Further, dummy plug 52 is a "dummy via," and is connected to the wiring 51. *Id.*, ¶[0122], Figs. 8-9. Annotated versions of Figures 8 and 9 highlighting this alternative, second mapping[3] is illustrated below (appreciating that I have only highlighted some exemplary dummy plugs 52 in Figure 9 below):



[3] When Watanabe's first embodiment of Figures 1-2 is applied against a claim, the first mapping of Watanabe's fifth embodiment of Figures 8-9 applies equally and is not separately discussed hereinafter. Further discussions of Watanabe's fifth embodiment below apply the second mapping from Figures 8-9.



149. The dummy plug 52 is conductive, being composed of the same barrier metal layer 72 and copper film 71 as the wiring 51. *Id.*, ¶¶[0118], [0122]. It is arranged to be incapable of having current flow therethrough because it extends to and terminates in a "non-forming region" of the insulating film 27 (i.e., where there is no wiring 39) or toward an isolated dummy wiring 61. *Id.*, ¶¶[0118]-[0122], [0127], [0185]-[0186], Figs. 8-9. A POSITA would have understood Watanabe's dummy plugs 52 (whether or not connected to dummy wiring 61) to constitute the claimed "dummy plug" for the same reasons that I explained previously. *See supra*, §§X.A.1.a.(7)-a.(8). Thus, the dummy plugs 52 do not constitute part of a closed circuit in actual use of the device, and the device would still be operable if they were

omitted. Instead, current flows between wiring 39 and wiring 51 through conductive plug 53, which constitute parts of a closed circuit during device operation.

150. Consistent with Watanabe's overall manufacturing approach using a dual damascene process (¶[0135]), the wiring 51 forms a dual damascene structure simultaneously with both the plug 53 and the dummy plug 52. *Id*., ¶[0135], Fig. 8,12A-12N, ¶¶[0049], [0118]-[0123], [0134]-[0171]. Thus, a POSITA would have understood that the wiring 51 and conductive plug 53 (i.e., the claimed "first interconnect" and "via") form a dual damascene structure, as do wiring 51 and dummy plug(s) 52 (i.e., the claimed "first interconnect" and "dummy via"). *Id*., ¶¶[0072], [0171]. Indeed, each of the disclosed first to third and fifth embodiments discloses a dual damascene structure of the interconnect with the active via and with the dummy via, respectively. Along with Watanabe's disclosure, this is evidenced by Watanabe's figures themselves. In each of cross-sectional Figures 1, 3, and 8, the wiring 39,51 is a dual damascene structure with conductive plugs 32,53 and dummy plugs 34,52, respectively. A POSITA would appreciate that Watanabe's barrier metal layer 30,72 conformally coats the outer sides of the plugs 32,53, dummy plugs 34,52, and wiring 39,51, all a single, continuous layer. With this conformal barrier layer coating, copper film 31,71 is added to fill the recesses for the plugs 32,53, dummy plugs 34,52, and trench for wiring 39,51 to form a single, unitary copper structure. A POSITA would have recognized this configuration

shown in Figures 1, 3, and 8 as a dual-damascene structure, especially in view of Watanabe's description (*e.g., id.*, ¶¶[0072], [0135], [0161]-[0171], Figs. 12K-12M).

151. Accordingly, Watanabe's fifth embodiment discloses claim 1. *Id*.

2. Claim 2[4]

152. At least each of Watanabe's second and fifth embodiments discloses claim 2.

a) [2.a] – "*semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate*"

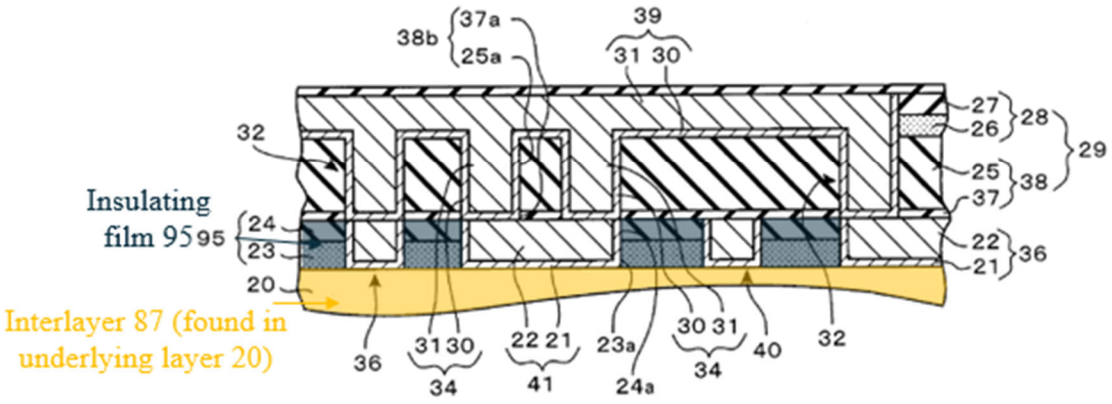
153. Element [2.a] recites the "semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate," which Watanabe discloses with its insulating film 95 and interlayer insulating film 87, collectively (or optionally insulating film 87 alone) (second embodiment) and insulating film 29 (fifth embodiment).

154. Watanabe's second embodiment (Figures 3-4) discloses an insulating film 95 that includes a low-dielectric insulating film 23 and silicon oxide film 24. TSMC-1004, ¶¶[0061], [0089], Fig. 3. Further, in connection with Figure 14,

[4] I analyze claim 2 here because some of the challenged claims depend from claim 2.

Watanabe discloses that the underlying layer 20 includes certain components, including the interlayer insulating film 87 underneath the insulating film 95, and then states that "[t]he underlying layer 20 in the present embodiment and each embodiments of the present invention is constructed by above members, for example." *Id.*, ¶¶[0172]-[0174], Fig. 14. Therefore, the Figure 3 embodiment includes an interlayer insulating film 87 and an insulating film 95 which, collectively constitute the claimed "second insulating film," or optionally interlayer insulating film 87 alone, that is on the semiconductor substrate. See annotated Figure 3 below:

FIG. 3

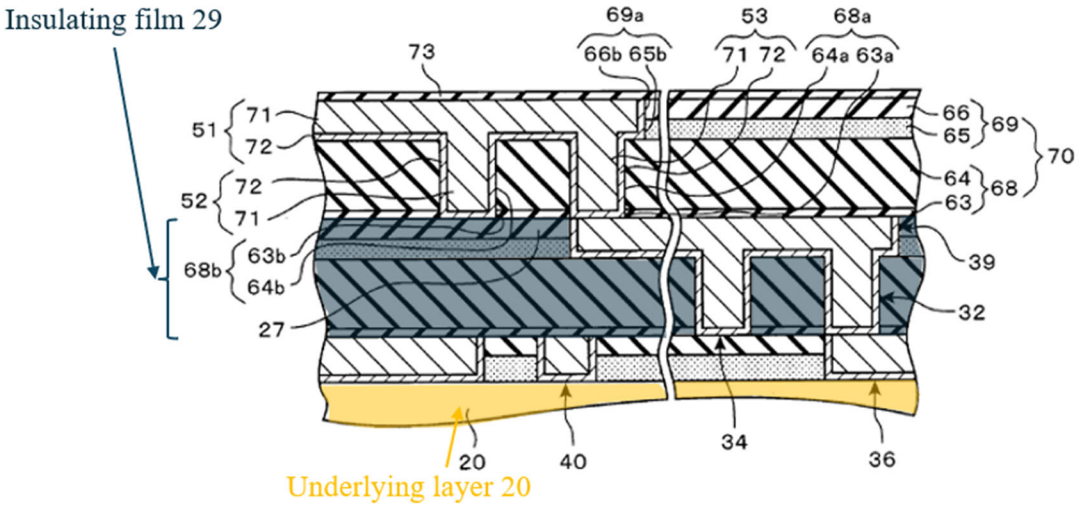


Id., ¶¶[0173]-[0174], [0061], [0089], [0094], [0116].

155. Watanabe's fifth embodiment (Figures 8-9), which builds on Figures 1-2, discloses insulating film 29, which includes the upper insulating film 28 and the lower insulating film 38 (together "second insulating film"; alternatively just lower insulating film 38). *Id.*, ¶¶[0066]-[0067], [0116]-[0117], [0172]-[0175], Figs. 1, 8,

14. Insulating film 29 is formed on a semiconductor substrate (which is part of underlying layer 20; and which is expressly shown as "silicon substrate 96" in Figure 14). *Id*. ¶¶[0061], [0172]-[0175]; Figs. 1, 8, 14. Insulating film 29 is indicated in annotated Figure 8 below:

FIG. 8



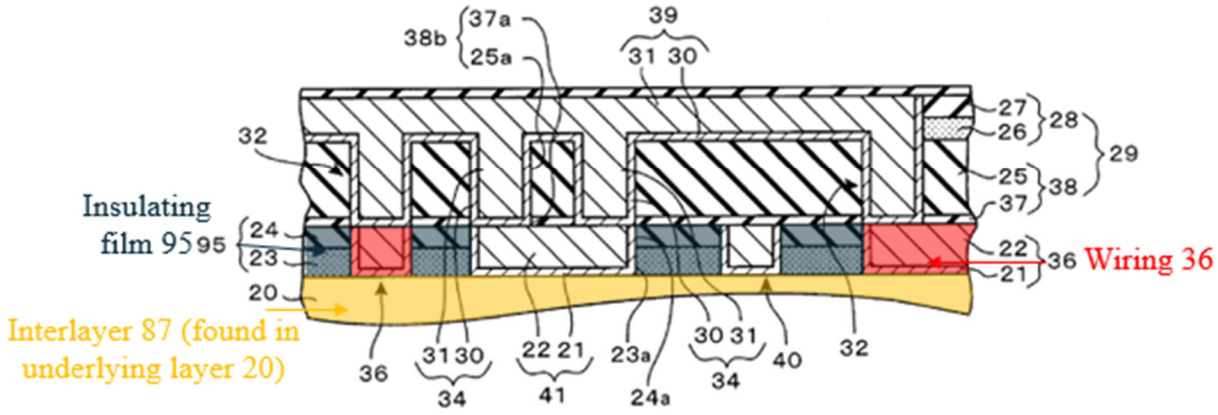
Along with film 27 of insulating film 29 being expressly labeled in Watanabe's Figure 8, a POSITA would understand that insulating film 29 comprises films 37, 25, 26, and 27 based on the common hatching, film thicknesses, and consistency with Figures 1, 3, 12, and 14, which all show the constituent sub-layers of insulating film 29. Additionally, for purposes of claim 2 and Watanabe's fifth embodiment, the "first insulating film" could be comprised of either or both of the films 37 and 25 residing directly above wiring 36 (e.g., lower insulating film 38 as described and annotated in the context of Figure 1 at *supra*, §X.A.1.(a).(4)).

b) [2.b] – "*wherein the first interconnect is formed on the second insulating film*"

156. Element [2.b] calls for "wherein the first interconnect is formed on the second insulating film," which Watanabe discloses.

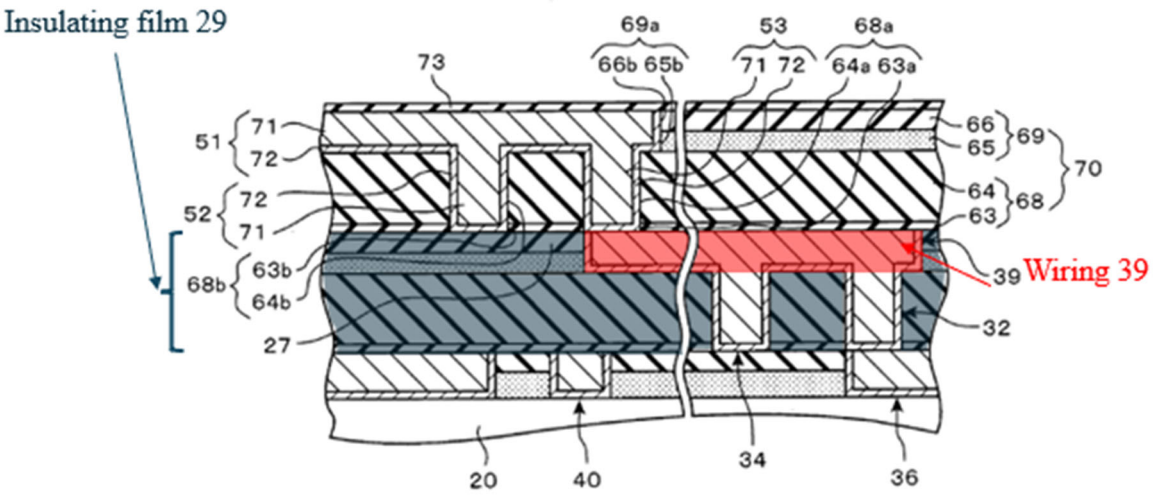
157. In Watanabe's second embodiment (Figures 3-4), the wiring 36 (the "first interconnect") is formed on the insulating film 95/interlayer insulating film 87 (the "second insulating film"; or optionally interlayer insulating film 87). TSMC-1004, ¶¶[0061], [0089], [0172]-[0174], Figs. 3, 14. See annotated Figure 3 below:

FIG. 3



158. In Watanabe's fifth embodiment (Figures 8-9), the wiring 39 (which is the "first interconnect") is formed on the insulating film 29, or the sublayers 37 and 25 (together, lower insulating film 38), with either film 29 or 38 being the "second insulating film." *Id.*, ¶¶[0066]-[0069], [0116]-[0117], [0172]-[0175], Figs. 1, 3, 8, 12, 14. Insulating film 29 is highlighted in the annotations to Figure 8 below:

FIG. 8



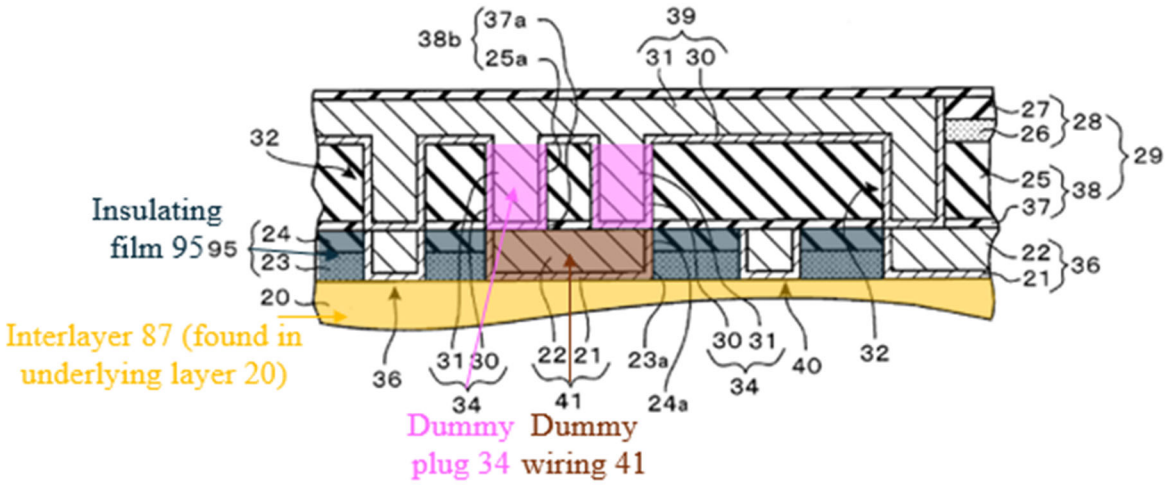
c) [2.c] – "*the dummy via is connected to a first dummy interconnect formed on the second insulating film*"

159. Element [2.c] calls for "the dummy via is connected to a first dummy interconnect formed on the second insulating film," which Watanabe discloses with its dummy wiring 41 (second embodiment) or dummy wiring 61 (fifth embodiment).

160. In the second embodiment, Figure 3 illustrates a dummy wiring 41 (which is the "first dummy interconnect"). TSMC-1004, ¶¶[0090]-[0091], Fig. 3. The dummy wiring 41 is formed on the interlayer insulating film 87/insulating film 95, which is the "second insulating film"; or alternatively interlayer insulating film 87 alone. *Id.*, ¶¶[0061], [0089]-[0091], [0144]-[0149], [0165], [0172]-[0174], Figs. 3, 12A-12M, 14. The dummy plug 34 (which is the claimed "dummy via") is

connected to the dummy wiring 41. *Id.*, ¶¶[0090]-[0091], Fig. 3. See annotated Figure 3 below:

FIG. 3



161. A POSITA would understand that "dummy wiring 41" is a "dummy interconnect" both because of its description as a "dummy" and its structure, which is consistent with the '623 patent's description of a "dummy interconnect." Specifically, a POSITA would recognize that dummy wiring 41 does not constitute part of a closed circuit during actual use of the device, i.e., no current flows therein during use, and Watanabe's device would still be operable if dummy wiring 41 was omitted. As discussed previously, the purpose of Watanabe's dummy wiring 41 is merely to add additional structural support/strength to the overall device, not to serve as active circuitry or otherwise conduct current flow. Indeed, Watanabe states that "as shown in FIG. 3, a dummy wiring 41 is provided ***in the non-forming region*** of

the first wiring 36," further demonstrating to a POSITA that the dummy wiring cannot pass current. *See* TSMC-1004, ¶[0090] (emphasis added).

162. In the fifth embodiment, Figures 8-9 illustrate a dummy wiring 61 (which is the claimed "first dummy interconnect") formed on the insulating film 29, as well as on lower insulating film 38 (comprising films 37 and 25 per §X.A.2.(a), *supra*), with either film 29 or 38 being the "second insulating film." *Id*., ¶[0127], Figs. 1, 3, 8, 9, 12, 14. In particular, dummy wiring 61 and wiring 39 are in the same layer and are on the same insulating film (e.g., insulating film 29). *Id*., ¶[0127]; *supra*, X.A.1.(a).(5). Annotated Figures 8-9 disclose the approximate location of dummy wiring 61 when Figure 8 accounts for dummy wiring 61, demonstrating that dummy wiring 61 is on insulating film 29 (or insulating film 38 (not annotated)):

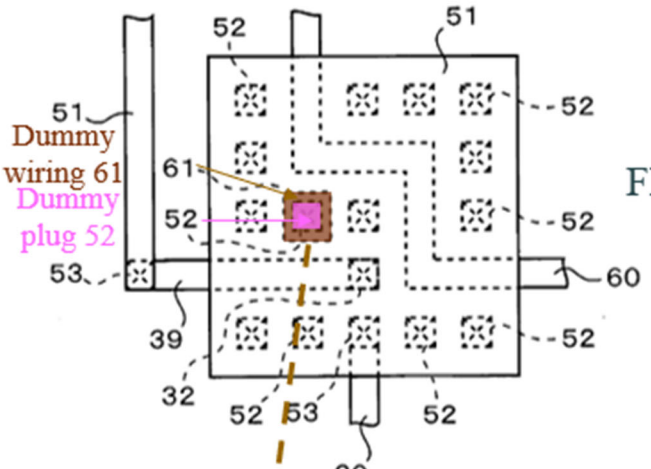


FIG. 9

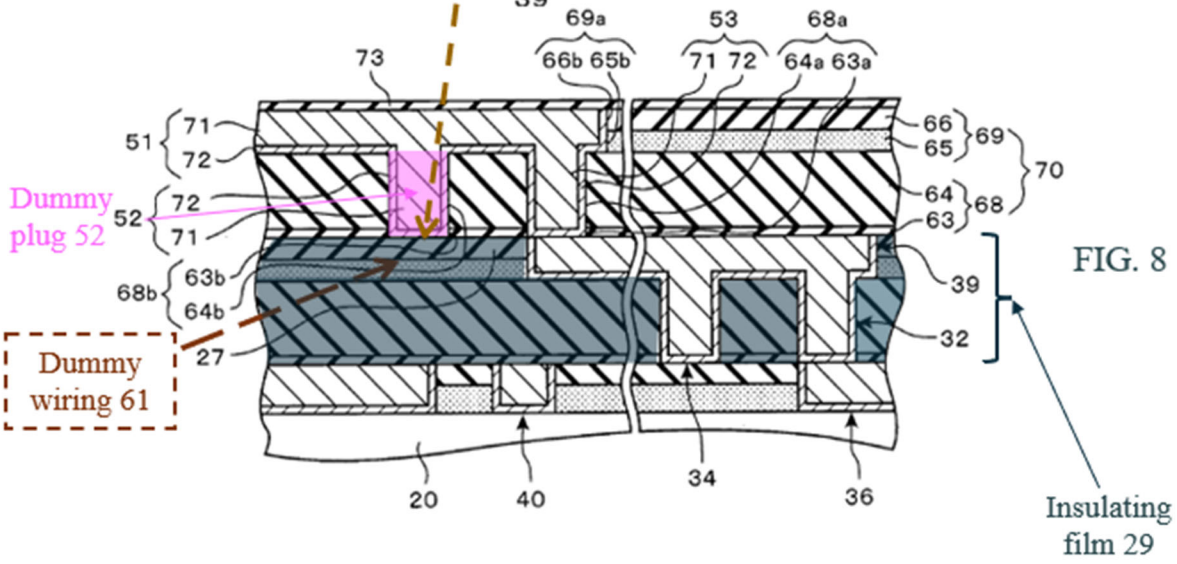


FIG. 8

.

163. The dummy plug 52 (which is the claimed "dummy via") is connected to the dummy wiring 61. TSMC-1004, ¶[0127]. Just like the "dummy wiring 41" and for the same reasons discussed above with respect to the second embodiment for this claim limitation, a POSITA would understand that "dummy wiring 61" is a "dummy interconnect."

3. Claim 10

a) [10.a] – "*semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square*"

164. At least each of Watanabe's second and fifth embodiments discloses claim 10.

165. Element [10.a] recites the "semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square," which Watanabe discloses for its dummy plug 34 and its dummy plug 52.

166. Watanabe discloses in annotated Figures 4 and 9 (which are the second and fifth embodiments) that the dummy plug 34 and dummy plug 52 ("dummy via") (as well as plug 32 or plug 53 ("via")) each have a substantially square planar shape:

FIG. 4

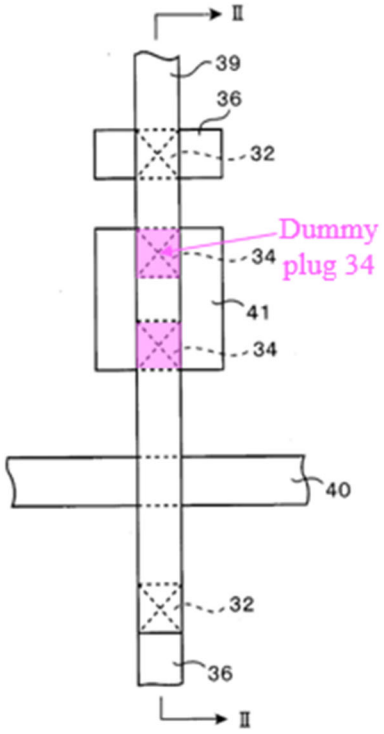
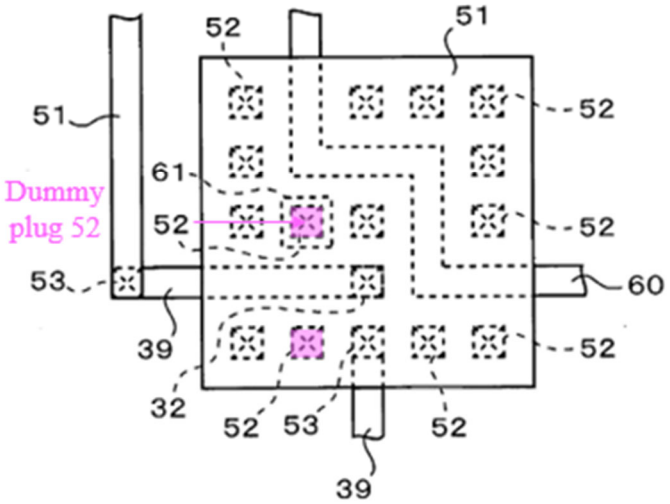

II
39
36
32
Dummy
plug 34
34
41
34
40
32
36
II

FIG. 9


52
51
51
52
61
Dummy
plug 52
52
52
53
60
39
52
32
52
53
52
39

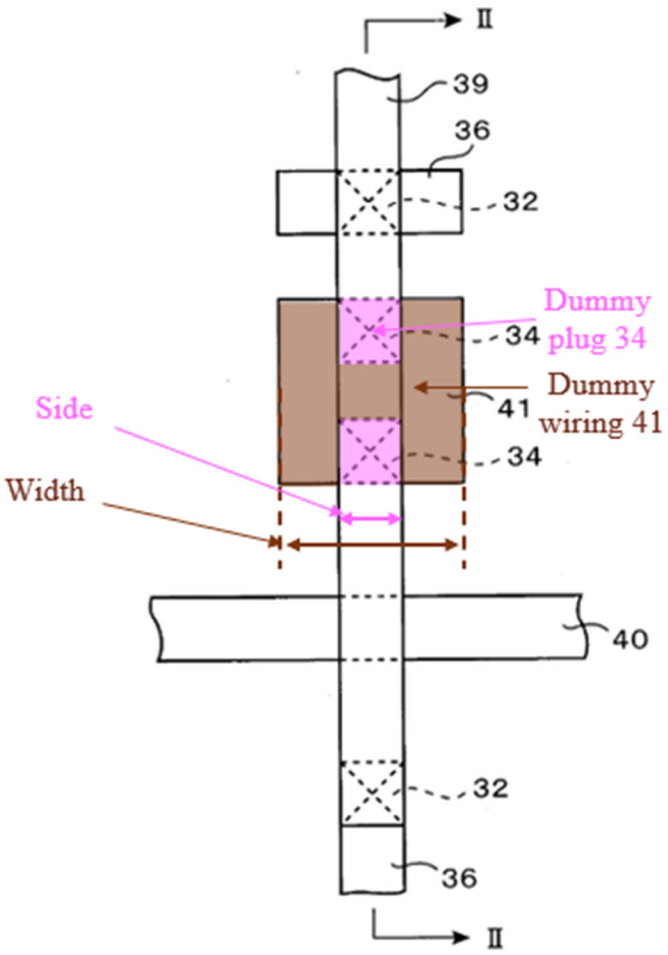
167. In addition, a POSITA understood that square shapes were a known via shape option. *See, e.g.*, TSMC-1008, 9:45-47 ("The opening of the via-hole may have any configuration, such as a square...."), 10:17-22; TSMC-1013, 9:45-49; TSMC-1039, 5:27-32 (noting the greater contact area achieved with square vias).

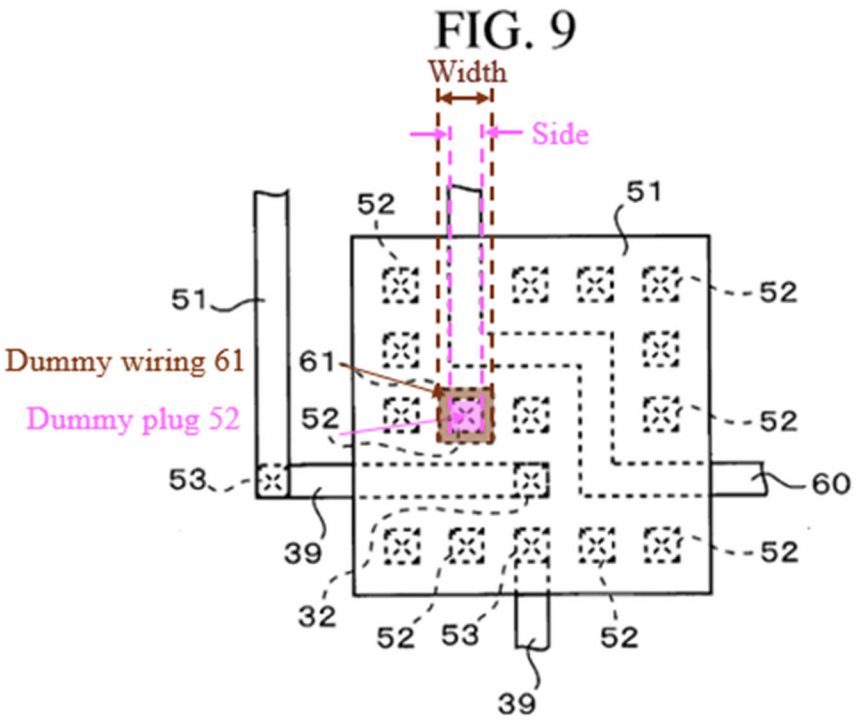
b) [10.b] – "*a side of the dummy via is smaller than a width of the first dummy interconnect*"

168. Element [10.b] calls for "a side of the dummy via is smaller than a width of the first dummy interconnect," which Watanabe discloses.

169. In the second embodiment in Figure 4, a side of the dummy plug 34 (the "dummy via") is smaller than a width of the dummy wiring 41 (the "first dummy interconnect"). TSMC-1004, Fig. 4. In the fifth embodiment in Figure 9, a side of the dummy plug 52 (the "dummy via") is smaller than a width of the dummy wiring 61 (the "first dummy interconnect"). *Id*., Fig. 9. These are shown in the annotated figures 4 and 9 below:

FIG. 4


II
39
36
32
Dummy plug 34
34
Dummy wiring 41
41
34
Side
Width
40
32
36
II



4. Claim 19 – "*semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square*"

170. At least Watanabe's first-to-third and fifth embodiments meet claim 19.

171. Watanabe's plan view figures consistently disclose both the conductive plug 32 ("via") and the dummy conductive plug 34 ("dummy via") with substantially square outlines, thus disclosing substantially square planar shapes. TSMC-1004, Fig. 2. For example, Figure 2 of Watanabe, which is described as a plan view showing the semiconductor device according to the first embodiment, shows two conductive plugs 32 and the dummy conductive plug 34 as squares. *Id*., ¶[0039], [0070], Fig. 2. Similarly, Figure 4 of Watanabe (plan view of the second

embodiment) also discloses two conductive plugs 32 and two dummy conductive plugs 34 as squares. *Id*., [0041], Fig. 4. Figures 5A, 5B, and 5C of Watanabe (plan views of the third embodiment) further illustrate conductive plug 32 and various arrangements of dummy conductive plugs 34, all disclosed as substantially square planar shapes. *Id*., ¶¶[0096]-[0098], Figs. 5A, 5B, 5C.

172. In Watanabe's fifth embodiment, the plan view in Figure 9 discloses plug 53 ("via") and dummy plugs 52 ("dummy via") with outlines consistent with a square planar shape. *Id*., ¶¶[0124]-[0127], Fig. 9. Given the consistent representation across multiple embodiments in plan view, a POSITA would understand a substantially square planar shape to be a disclosed option for both the via and the dummy via.

173. Therefore, for each of first-to-third and fifth embodiments, Watanabe discloses that plug 32 and dummy plug 34 each have a planar shape that is substantially square, exemplified in annotated Figures 2, 5A, and 9 (*see id.*, TSMC-1004, ¶[0039], Figs. 2, 4, 5A-5C, 9):

FIG. 2

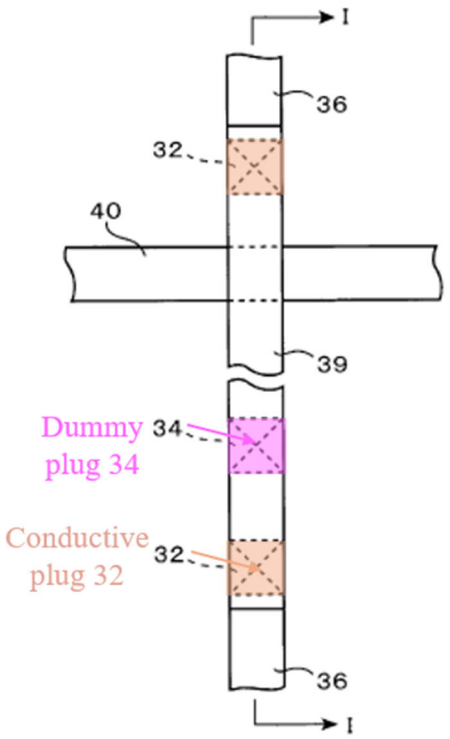


FIG. 5A

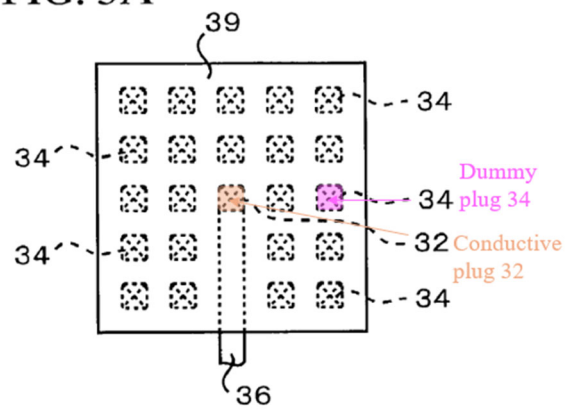
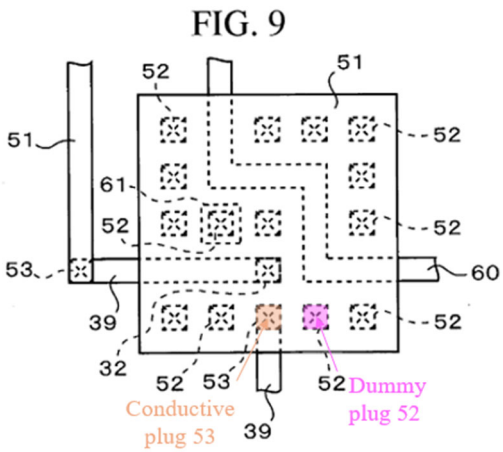


FIG. 9



174. Moreover, a POSITA understood at the time that square vias (both dummy and functional) were a known option for the via shape. *See also* TSMC-1008, 9:45-47 ("It will be also understood that the opening of the via-hole may have any configuration, such as a square, rectangle or circle."), 10:8-11; TSMC-1013,

9:45-49 ("[T]he shape of dummy via holes are indicated by squares, rectangles, and line patterns. The shapes of the dummy wiring patterns and dummy via holes may take other shapes."); TSMC-1039, 5:27-32 (noting the greater contact area achieved with square vias). Thus, Watanabe discloses substantially square cross-sections to be a disclosed shape for both the plugs 32 and dummy plugs 34.

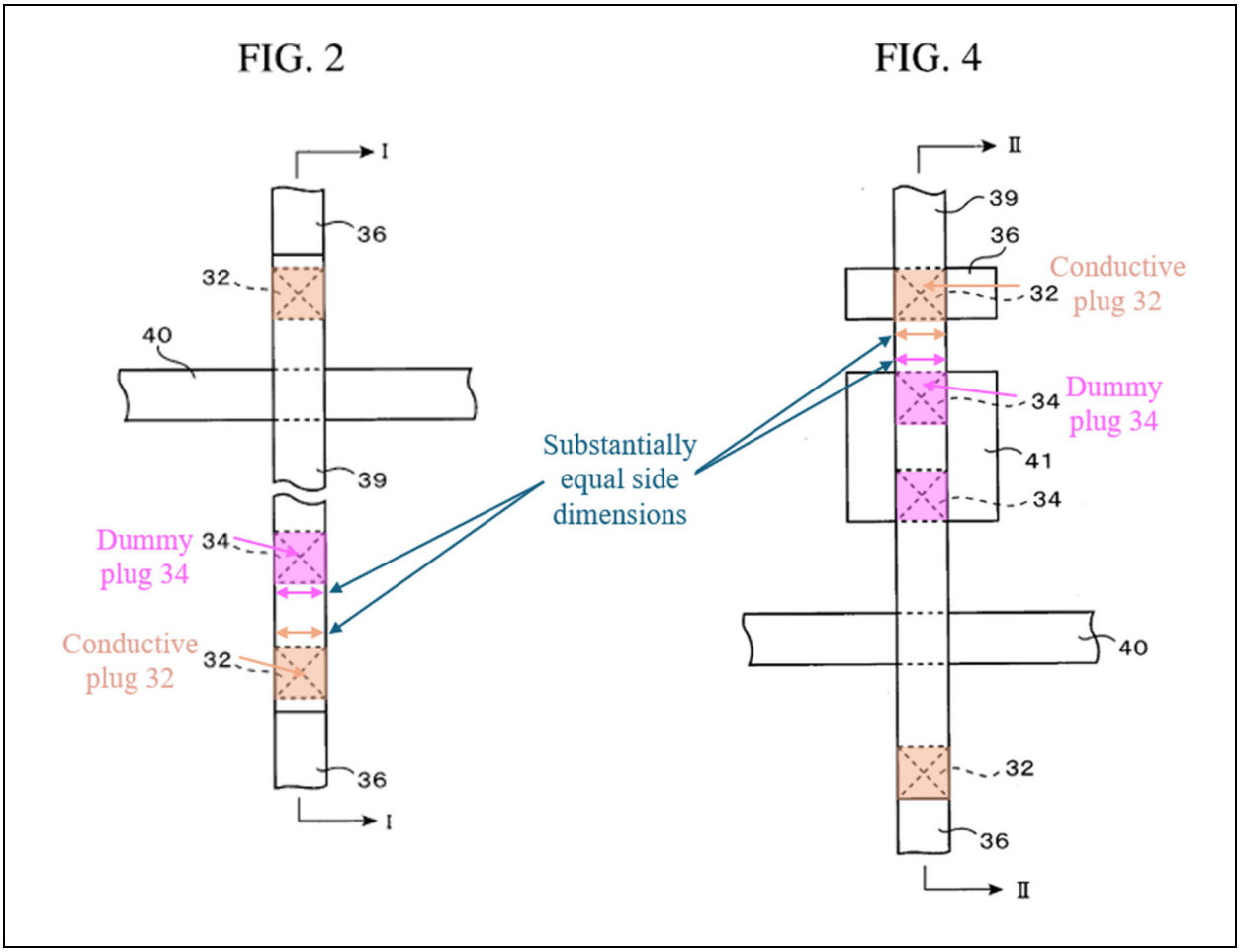
5. Claim 20 – "*semiconductor device of claim 19, wherein a length of a side of the via and a length of a side of the dummy via are substantially equal to each other*"

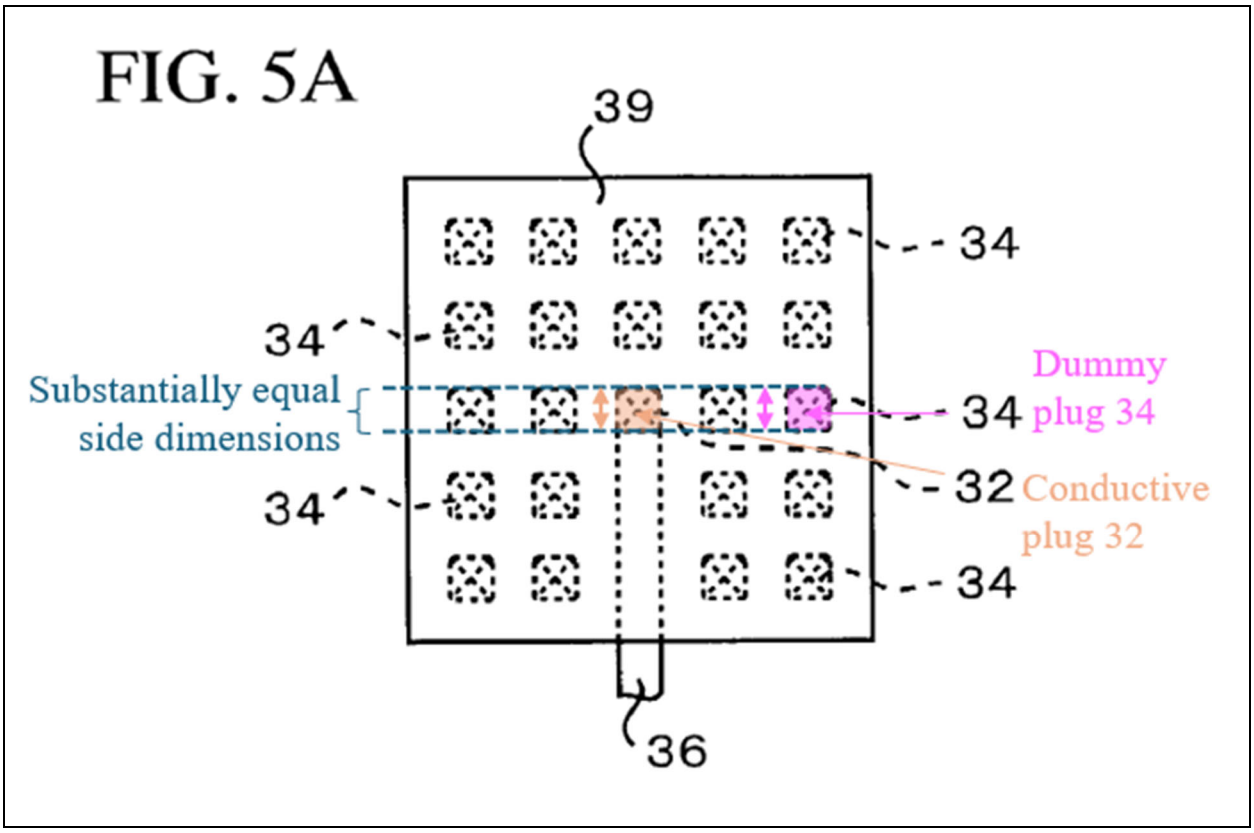
175. At least Watanabe's first-to-third and fifth embodiments meet claim 20.

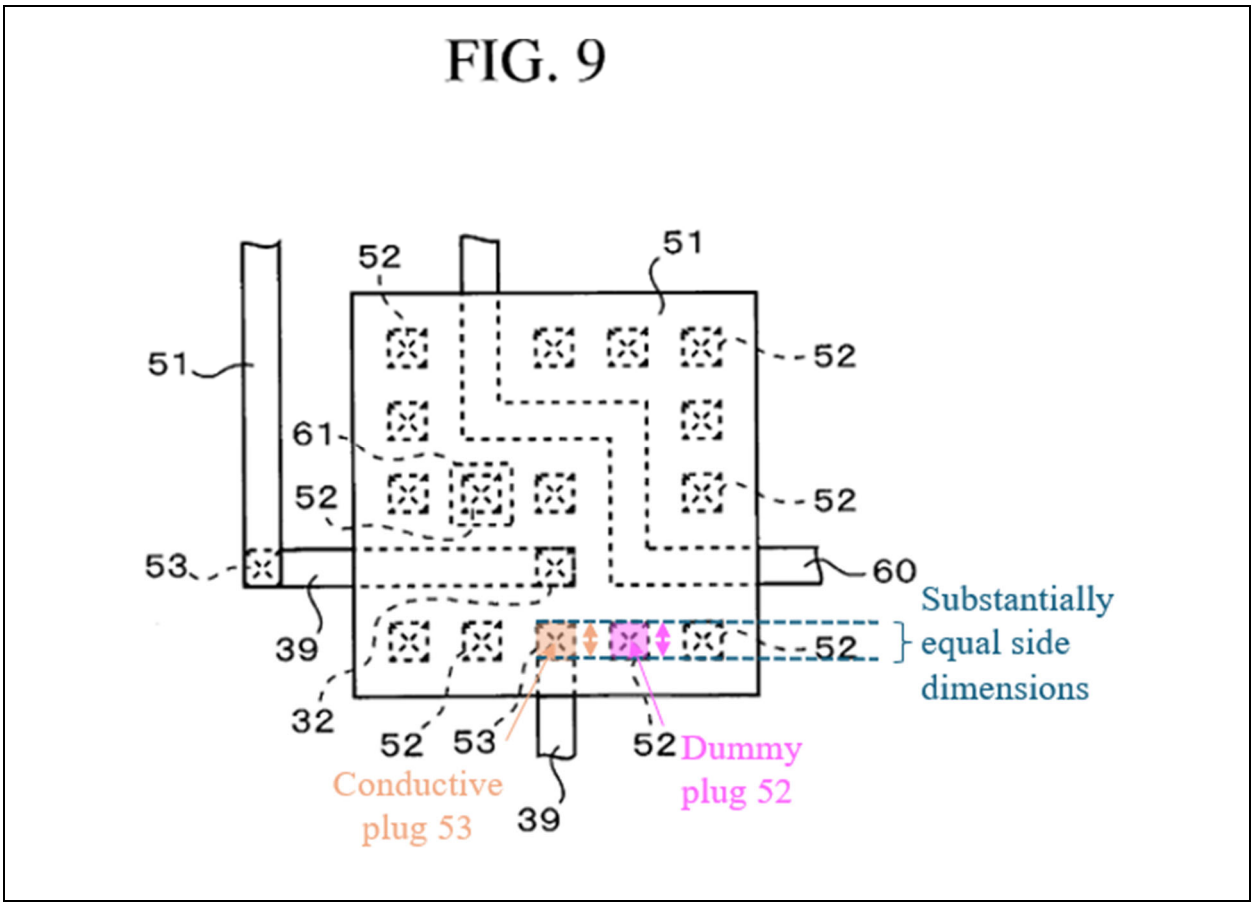
176. Claim 20 recites the "semiconductor device of claim 19, wherein a length of a side of the via and a length of a side of the dummy via are substantially equal to each other," which Watanabe discloses.

177. The disclosure of claims 1 and 19 by Watanabe is established above. Watanabe's plan view figures, such as Figures 2, 4, 5A-5C, and 9, consistently disclose that the conductive plug 32 ("via") and the dummy conductive plug 34 ("dummy via") have substantially equal side lengths/dimensions. TSMC-1004, Figs. 2, 4, 5A-5C, 9. Furthermore, Watanabe's simulation model describes employing a conductive plug 32 and a dummy conductive plug 34 as circular cylinders with an identical diameter of 0.15 μm. *Id.*, ¶[0083]. This further confirms the substantially equal lengths of the respective components.

178. Annotated Figures 2, 4, 5A-5C, and 9 are shown below:




FIG. 5A
39
34
34
Substantially equal
side dimensions
34
Dummy
plug 34
32
Conductive
plug 32
34
36



6. Claim 24

a) [24.a] – "*semiconductor device of claim 1, wherein a planar shape of the via is substantially a square*"

179. At least Watanabe's first-to-third and fifth embodiments meet claim 24.

180. Element [24.a] recites the "semiconductor device of claim 1, wherein a planar shape of the via is substantially a square," which Watanabe discloses.

181. The disclosure of claim 1 by Watanabe is established above. Watanabe's plan view figures consistently disclose the conductive plug 32 ("via")

with substantially square outlines, thus indicating substantially square planar shapes. TSMC-1004, Fig. 2. For example, Figure 2 of Watanabe, a plan view of the semiconductor device according to the first embodiment, shows two conductive plugs 32 as squares. *Id*., ¶[0039], [0070], Fig. 2. Similarly, Figure 4 of Watanabe (plan view of the second embodiment) also discloses two conductive plugs 32 as squares. *Id*., [0041], Fig. 4. Figures 5A, 5B, and 5C of Watanabe (plan views of the third embodiment) further disclose that conductive plug 32 has a substantially square planar shape. *Id*., ¶¶[0096]-[0098], Figs. 5A, 5B, 5C.

182. In Watanabe's fifth embodiment, the plan view in Figure 9 discloses plug 53 ("via") as a square planar shape. *Id*., ¶[0124]-[0127], Fig. 9. A POSITA further understood that square vias were a known shape for vias in semiconductor devices at the time.

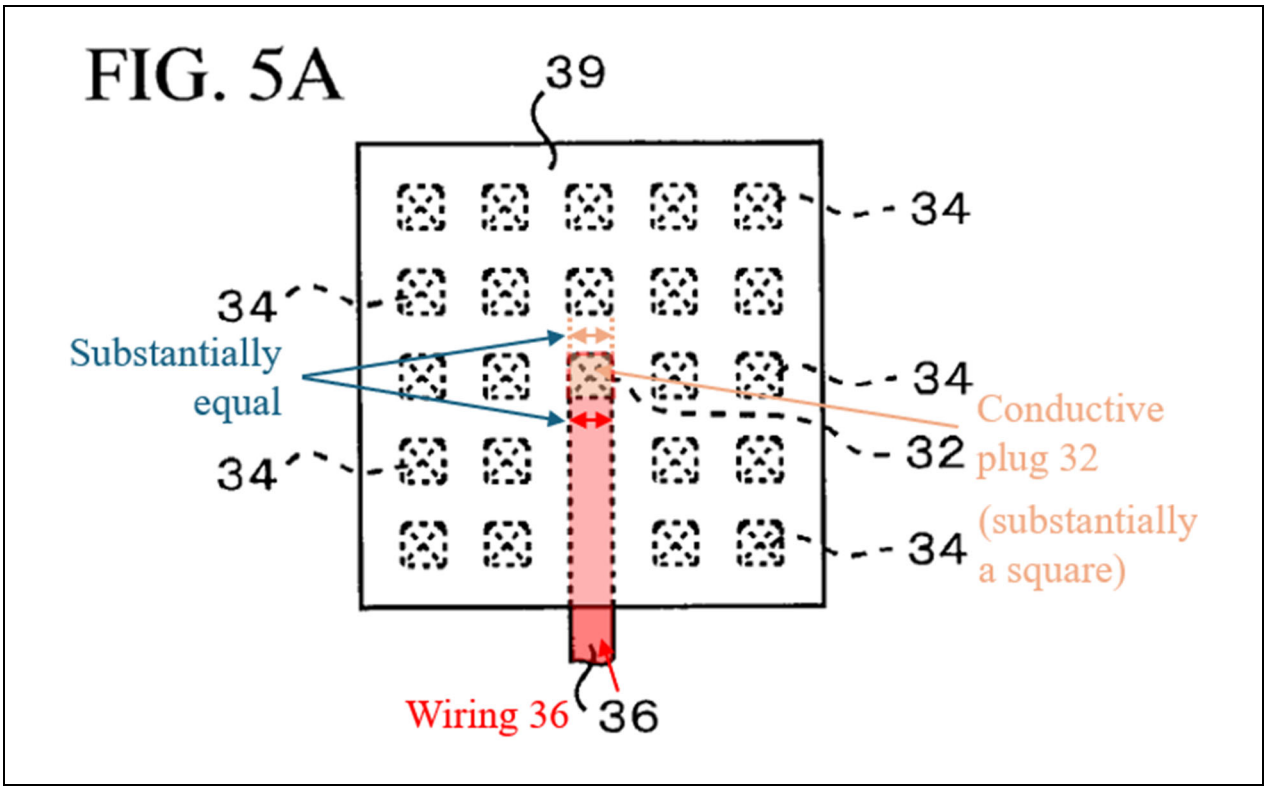
183. Therefore, Watanabe discloses vias (e.g., plugs 34 and 53) having a substantially square shape, as shown in Figures 2, 4, 5A-5C, and 9. *Supra*, §§X.A.3-5.

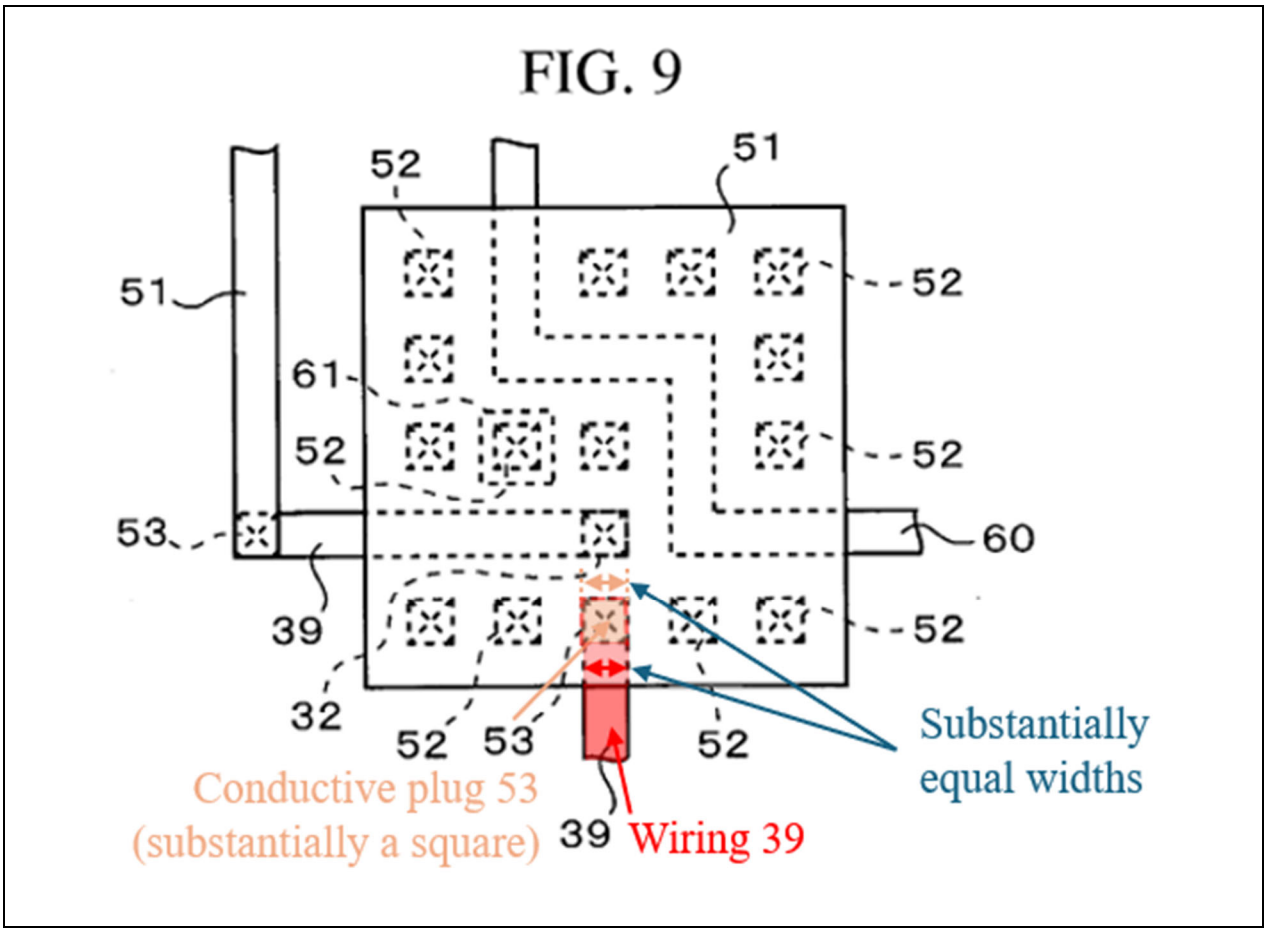
b) [24.b] – "*a side of the via is substantially equal to a width of the first interconnect*"

184. Element [24.b] calls for "a side of the via is substantially equal to a width of the first interconnect," which Watanabe discloses.

185. In Watanabe's first, second, and third embodiments, the plan views (Figures 2, 4, and 5A-5C) consistently disclose the side length of the schematic square representing conductive plug 32 ("via") as spanning the width of the wiring 36 ("first interconnect") to which it connects. TSMC-1004, Figs. 2, 4, 5A-5C.

186. In Watanabe's fifth embodiment, the claimed "via" is conductive plug 53, and the claimed "first interconnect" is wiring 39. Figure 9 of Watanabe, the plan view for this embodiment, shows the square conductive plug 53 connecting to the linear wiring 39. *Id*., Fig. 9. As disclosed, the side of the conductive plug 53 is substantially equal to the width of the wiring 39. *Id*. A POSITA would further understand this configuration ensures a robust electrical connection. Exemplary annotated Figures 5A and 9 are shown below:


FIG. 5A
39
34
34
Substantially
equal
34
34
32
Conductive
plug 32
(substantially
a square)
Wiring 36
36



187. Therefore, Watanabe's Figures 2, 4, 5A-5C, and 9 disclose conductive plugs 32 and 53 having side dimensions equal to the width of "first" wirings 36 and 39 (in first-to-third and fifth embodiments, respectively). TSMC-1004, Figs. 2, 4, 5A-5C, 9.

7. Claim 27 – "*semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width*"

188. At least Watanabe's first-to-third and fifth embodiments meet claim 27.

189. Claim 27 recites the "semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width," which Watanabe discloses.

190. The disclosure of claim 1 by Watanabe is established above. Watanabe's conductive plug 32 corresponds to the claimed "via," and Watanabe's dummy conductive plug 34 corresponds to the claimed "dummy via." Watanabe's wiring 36 corresponds to an interconnect, and its depicted width in the context of the plan views represents a "minimum interconnect width."

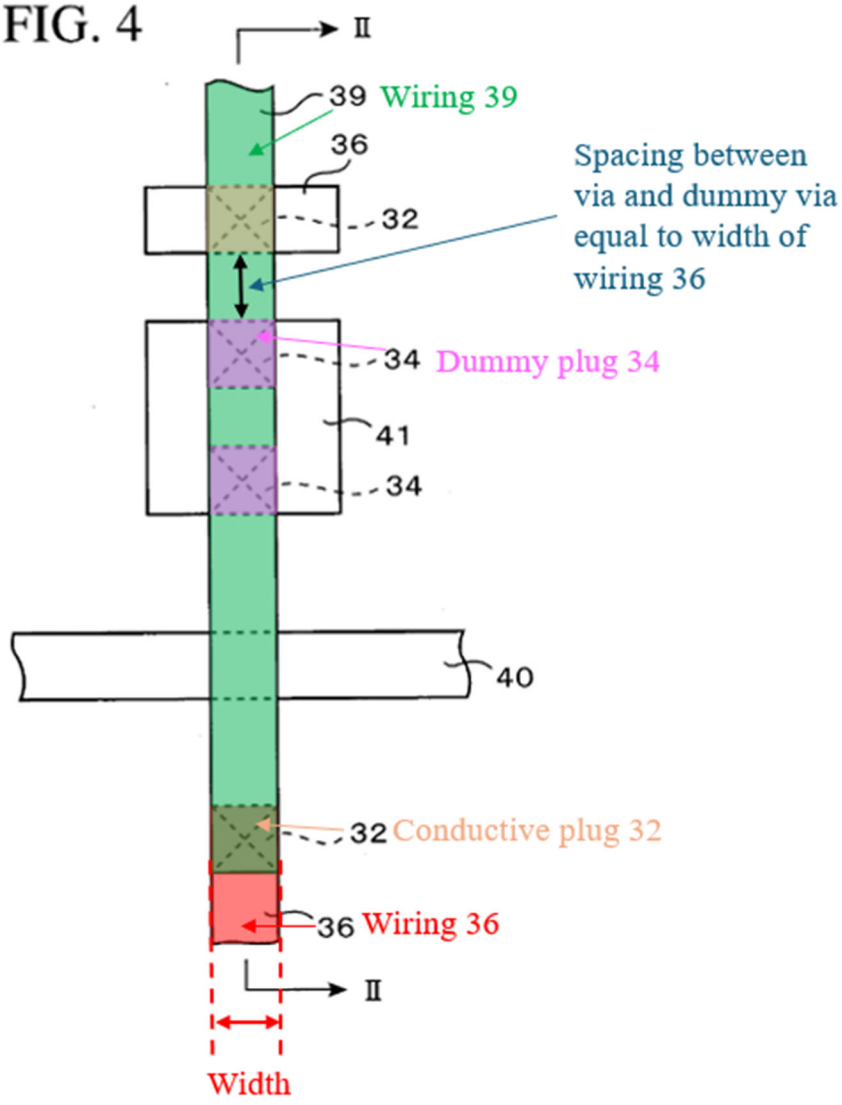
191. Watanabe's plan view figures illustrate these features and their relative dimensions. For example, Figure 4 of Watanabe, a plan view of the second embodiment, discloses the wiring 36 at the top of the figure with a conductive plug 32 situated on it, and a dummy conductive plug 34 positioned adjacent to the conductive plug 32. TSMC-1004, Fig. 4. In this depiction, the width of the wiring 36 (representing a minimum interconnect width) is shown, and the distance (spacing) between the edge of the conductive plug 32 and the facing edge of the adjacent dummy conductive plug 34 is also visually represented. *Id*. Figure 4 shows that this edge-to-edge spacing between conductive plug 32 and an adjacent dummy conductive plug 34 is substantially equal to the disclosed width of the wiring 36. *Id*. As understood by a POSITA, this discloses the proportional relationship that the

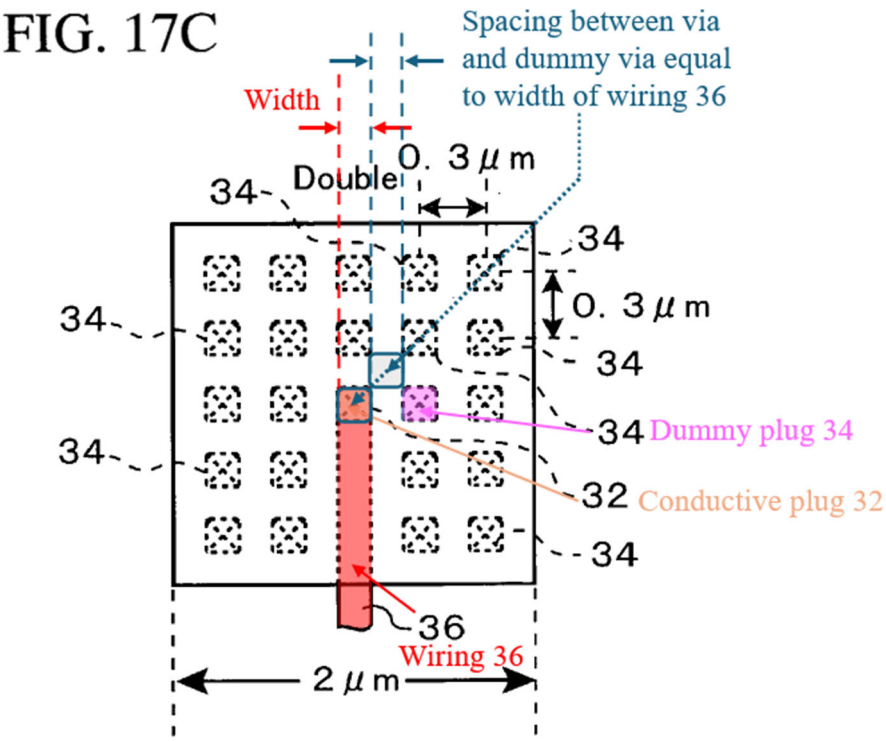
distance between the via and the dummy via is substantially equal to a minimum interconnect width.

192. Therefore, Watanabe discloses that the via-to-dummy-via spacing is substantially equal to a minimum interconnect width. Figure 14 discloses wiring 36 as the first interconnect layer above the MOSFET devices, and a POSITA understood that the wiring layer closest to the MOSFET devices need to be at the minimum interconnect width to minimize density and parasitic capacitance. *See* TSMC-1012, 34 ("[T]he lower wiring levels are at a minimum possible pitch and thickness to minimize capacitance and maximize wiring density.").

193. Watanabe's annotated Figures 4 and 17 disclose plugs 32 on wiring 36, where the wiring 36 width (representing a minimum interconnect width, as noted above) is equal to the spacing between plug 32 and adjacent dummy plug 34, as illustrated below:

FIG. 4


II
39 Wiring 39
36
32
Spacing between via and dummy via equal to width of wiring 36
34 Dummy plug 34
41
34
40
32 Conductive plug 32
36 Wiring 36
II
Width



194. A POSITA would thus have understood that Watanabe teaches a distance between vias (e.g., plugs 32) and dummy vias (e.g., dummy plugs 34) that is substantially equal to a minimum interconnect width.

B. Ground 1B: Claim 27 Is Obvious in View of Watanabe

195. In addition to being anticipated by Watanabe, claim 27 is also obvious in view of Watanabe as detailed below.

1. Claim 27 – "*semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width*"

196. Claim 27 recites the "semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width," which is also obvious in view of Watanabe.

197. Watanabe discloses claim 1 as established in Ground 1A. In addition, Watanabe further teaches that reducing the pitch (p_2) between conductive plug 32 and the adjacent dummy conductive plug 34 to their minimum spacing distance is desirable for improving stress migration resistance. TSMC-1004, ¶¶[0032]-[0033], [0086]-[0087], [0190]-[0191], Figs. 15A-18. Specifically, Watanabe's simulations teach that the stress difference ($\Delta\sigma$)—which is indicative of stress-migration susceptibility—generally decreases as the pitch p_2 decreases, with good results shown below 1 μm, and especially below 0.6 μm. *Id*. Furthermore, Watanabe recognizes the general trend and requirement for miniaturization and increasing integration density in semiconductor devices, as well as maintaining adequate mechanical strength of the device, which are likewise achieved by minimizing the spacing between elements, such as between vias and dummy vias, which likewise improves mechanical strength. *Id*., ¶¶[0015], [0028], [0033], [0186]. The edge-to-edge spacing of the conductive plug 32 to the adjacent dummy conductive plug 34 is reduced as the pitch (center-to-center spacing) is reduced.

198. For example, in the simulation results shown in Figure 16A, Watanabe investigates the effect of varying the pitch p_2 (an interval between the conductive

plug 32 and the adjacently arranged dummy conductive plug 34) on stress migration. *Id.*, ¶¶[0086]-[0087], Fig. 16A. All data points evaluated in Figure 16A entail a pitch p_2 of 1.0 µm or less. *Id.* Watanabe provides an example where the interval between the neighboring plugs (including the plug 32 and the dummy plug 34) was fixed to 0.3 µm for simulations involving the models shown in Figures 17B-17C. *Id.*, ¶[0105], Figs. 17B-17C. This interval/pitch "p_2" is disclosed in the annotated Figures 16B and 17B below:

FIG. 16B

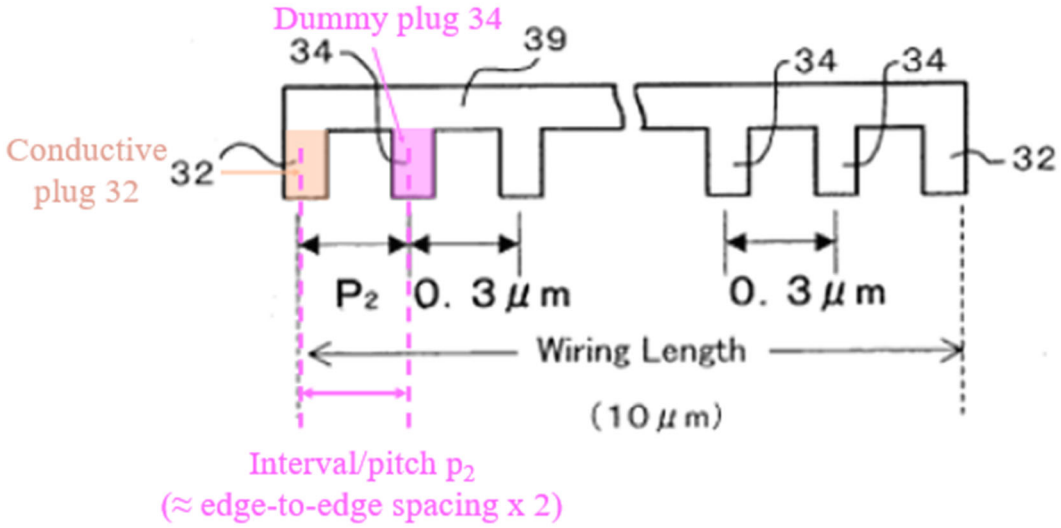
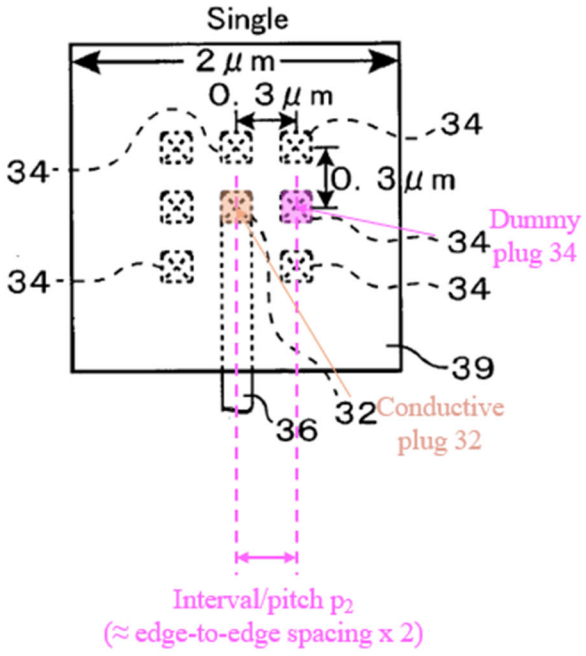


FIG. 17B



199. As shown in annotated Figure 16B above, the interval/pitch "p_2" in Watanabe is the interval from a center of a via to a center of an adjacent dummy via, so the spacing from a right edge of the annotated conductive plug 32 to a left edge of the adjacent annotated dummy plug 34 is necessarily less than the interval/pitch p_2—in Watanabe's case, the edge-to-edge spacing is approximately half the pitch interval.

200. So as an example, the spacing distance between the right side of the conductive plug 32 annotated above in Figures 16B and 17B and the left side of the nearest dummy plug 34 is less than the interval or pitch between those same plugs. Thus, because this 0.3 μm interval/pitch between plugs 32 and 34 satisfies the 25 μm or less requirement of claim 25, the edge-to-edge spacing between the same plugs necessarily satisfies this requirement as well. Watanabe concludes that in

order to prevent the stress-migration, it is preferable that the first pitch p_2 is less than 1 μm, and more preferably less than 0.6 μm. *Id*., ¶¶[0032]-[0033], [0053], [0086]-[0087], [0190]-[0191], [0193], Fig. 16A.

201. A POSITA designing a semiconductor device, motivated by Watanabe's teaching to minimize the via-to-dummy-via pitch (p_2) for improved reliability and mechanical strength, and simultaneously driven by the standard industry goal of maximizing layout density (as acknowledged by Watanabe (*id*., ¶[0005]; *see also* TSMC-1012, 34)), would seek to place the dummy plug 34 as close as possible to the conductive plug 32.

202. The minimum possible spacing between vias in a semiconductor layout is dictated by the design rules for the specific manufacturing process technology node being used. These design rules define minimum feature sizes and minimum spacing requirements to ensure manufacturability and avoid electrical shorts, other failures, and undesirable "crosstalk" resulting from parasitic capacitances and the like. *See* TSMC-1034, 585 (discussing arranging multilevel interconnect structures in tier and using finest metal-pitch allowed by design rules being employed for the tiers). Therefore, it would have been obvious to a POSITA seeking to implement Watanabe's stress-reducing and mechanically-enhancing dummy vias in the most space-efficient manner while maximizing their effectiveness (by minimizing the pitch/effective interconnect length (*see* TSMC-1004, ¶¶[0020]-[0022], [0026]-

[0028], [0074]-[0076], [0083]-[0092], [0108])), to place the dummy conductive plug 34 adjacent to the conductive plug 32 at the minimum spacing allowed by the applicable design rules.

203. A POSITA knew that design rules for minimum spacing between features (like vias) and minimum widths of features (like interconnects) are intrinsically linked within a given technology node; they typically scale together since they are dictated by the available resolution at a given interconnect level and/or for a given planarization uniformity. Placing the dummy via at the minimum allowed spacing would naturally result in a distance "substantially equal to" the minimum interconnect width for that technology generation at that interconnect level, especially given that the limits for both are typically limited by the achievable lithography resolution for a given level/surface planarization.

204. A POSITA would have had a reasonable expectation of success in achieving improved stress migration resistance (which Watanabe teaches as a result of closer spacing/lower "effective wiring lengths"), as well as improved processing and high layout density, by employing this minimum design rule spacing. By definition, this is the minimum spacing that could be reliably implemented and achieved for a given manufacturing process, ensuring that it could be attained. *Id*.

C. Ground 2: Claim 23 Is Obvious Over Watanabe and Iizuka

205. Watanabe and Iizuka render claim 23 obvious to a POSITA.

206. Claim 23 depends from claim 1. The analysis in Ground 1A demonstrates how Watanabe discloses claim 1.

1. Claim 23

207. Watanabe and Iizuka render claim 23 obvious.

a) [23.a] – "*semiconductor device of claim 1, wherein the via is substantially circular in a plan view*"

208. Element [23.a] recites the "semiconductor device of claim 1, wherein the via is substantially circular in a plan view," which Watanabe in view of Iizuka renders obvious.

209. Watanabe discloses a simulation model with conductive plug 32 ("via") and dummy plug 34 ("dummy via") described as a "circular cylinder," i.e., disclosing them to the POSITA as substantially circular in plan view. TSMC-1004, ¶[0083] ("as the model of the plug 32 and the dummy plug 34, a **circular cylinder** whose diameter is 0.15 um and whose height is 0.42 um was employed."), Figs. 1, 3. A POSITA would recognize that the same applies to conductive plugs 53 and dummy plugs 52 in all of Watanabe's embodiments. *E.g.*, *id*., Fig. 9. Disclosing the circular cylinder shape for its simulation model suggests circular vias to a POSITA for Watanabe's devices, since this is the shape on which Watanabe's modeling was done. A POSITA would thus interpret Watanabe as disclosing vias having circular cross-sections in plan view, in addition to the square vias disclosed in the figures.

210. Like Watanabe, Iizuka is directed to a "semiconductor device" in which "via-holes" are formed. *See* TSMC-1008, Abstract. Iizuka demonstrates that it was well-known prior to the '623 patent that vias could have many polygonal cross-sectional shapes and that the selection of a specific shape was simply a design choice. For example, Iizuka teaches the common nature of circular via-holes and the interchangeability with other common shapes such as squares: "the opening of the via-hole may have any configuration, such as a **square, rectangle or circle**." *Id*., 9:45-47 (emphasis added). Iizuka's description of via-hole 6 as having a "diameter" similarly discloses a circular via shape, since the geometrical term "diameter" corresponds with circular shapes. *Id*., 6:60-63, Fig. 5A.

211. Thus, a POSITA understood that circular shaped vias were common and standard in the industry, as evidenced by Iizuka, and would have understood that the conductive plugs 32/53 and dummy plugs 34/52 in Watanabe could be made to be substantially circular in a plan view. This is further evidenced, for example, by Hasunuma, which shows circular vias/dummy vias in various embodiments. *See, e.g.*, TSMC-1005, ¶[0200], Fig. 19A (showing circular-shaped dummy vias 125); *see also* TSMC-1013, 8:47-52 (noting that circular vias may be used, among other shapes). Also, Igarashi teaches circular vias as the default shape for all via connections, except where square vias or other shapes are needed for a given overlap of the upper and lower interconnects. TSMC-1014, ¶¶[0091]-[0092], Figs. 8, 14

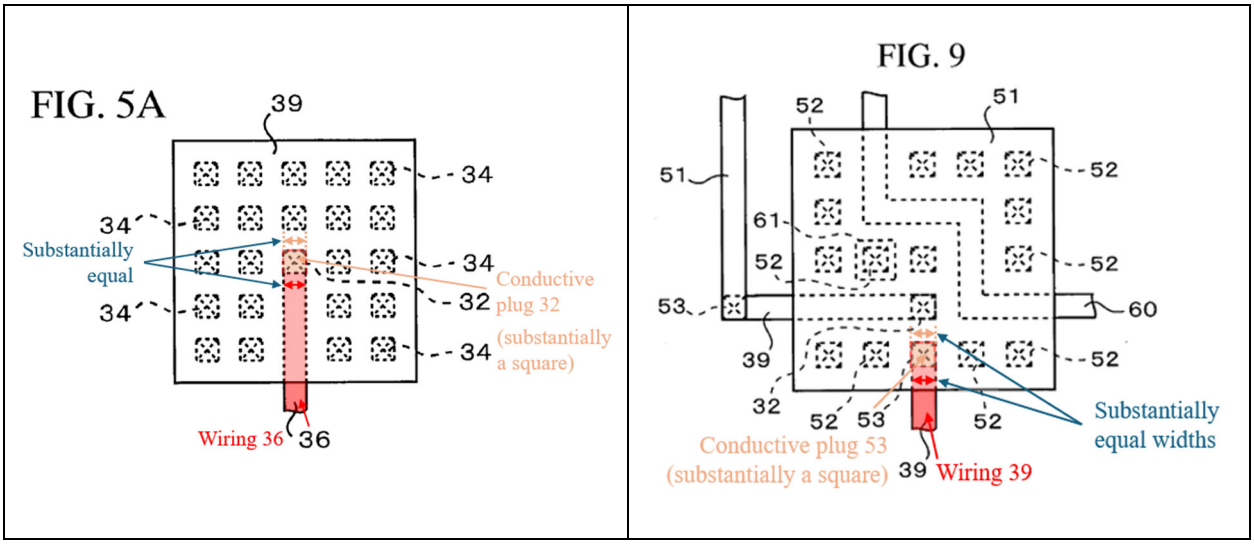
(teaching circular vias as a default shape, and square vias as preferred for certain interconnect junctions). Thus, a POSITA understood that square and circular shapes are among a finite number of common, interchangeable design choices for via/dummy via shapes, and circular vias were well-known, as expressly taught by Iizuka, among others. Given Watanabe's own simulation model, Iizuka's teaching that via shapes (circular, square, rectangular) were interchangeable design options, other prior art known to a POSITA, and the additional reasons discussed below, it was obvious to implement Watanabe's conductive plugs 32/53 and dummy plugs 34/52 with a substantially circular shape given Iizuka's teaching that circular vias were a known, interchangeable design alternative, as well as the widespread knowledge of this at the time. *Infra*, §X.C.2; TSMC-1005, Figs. 19A, 22A; TSMC-1013, 8:48-52; TSMC-1014, ¶[0091]. A POSITA would have had a reasonable expectation of success in doing so. *Id.*

b) [23.b] – "*a diameter of the via is substantially equal to a width of the first interconnect*"

212. Element [23.b] calls for "a diameter of the via is substantially equal to a width of the first interconnect," which the combination of Watanabe and Iizuka renders obvious.

213. Watanabe's plan view figures consistently disclose vias (conductive plug 32, 53) that span the width of the first interconnect (wirings 36, 39) to which

the via connects at its bottom end. TSMC-1004, Figs. 2, 4, 5A, 9. For example, annotated Figures 5A and 9 are shown below:



214. A POSITA, having found it obvious to implement vias with a circular shape (as discussed for element [23.a]), would further have found it obvious to maintain this full-width contact by making the diameter of circular conductive plugs 32, 53 substantially equal to the width of the underlying wiring (e.g., wirings 36, 39). Such sizing is a standard design practice that maximizes the electrical contact area and ensures a robust connection between a via and an underlying interconnect line. Indeed, a POSITA recognized that by making the via the same width as the underlying interconnect, the designer maximizes the available contact area/interface between the via and interconnect.

215. A POSITA would have had a high expectation of success in achieving such a dimensionally matched connection, as this represents a routine design consideration for reliable via-to-line interconnections. A POSITA would simply have designated the vias to have the same size as the underlying interconnect line, and the standard manufacturing process (including the same processes already disclosed in Watanabe) would then build them as such.

2. Combination of Watanabe and Iizuka

216. Watanabe's simulation model describes its vias and dummy vias as "circular cylinders," thereby disclosing vias having circular cross-sections, as alternatives to the square vias disclosed in Watanabe's figures. TSMC-1004, ¶[0083]; *supra*, §X.C.1.(a). Iizuka's explicit teaching that vias can be circular, square, or rectangular confirms that a POSITA would have viewed these shapes as a finite number of readily interchangeable design choices given Iizuka's express teaching to this effect and a POSITA's general understanding. *See* TSMC-1008, 9:45-47 ("the opening of the via-hole may have any configuration, such as a square, rectangle or circle."). As such, it was obvious to implement Watanabe's conductive plugs 32/53 and dummy plugs 34/52 with a substantially circular shape.

217. Particular via shapes, such as square or circular, each provide known advantages applicable to a given situation. *See, e.g.*, TSMC-1014, ¶¶[0091]-[0092], Figs. 8, 14 (disclosing the use of circular and square vias, depending on the specifics

of the interconnect junction). A POSITA would have been motivated to use circular vias for a number of design specific reasons. For example, the motivation to use circular vias, as known from Iizuka and general practice, included advantages in manufacturing process control (e.g., more uniform etching and filling characteristics for circular shapes compared to sharp-cornered squares), more favorable stress distribution around a circular opening, and design simplicity. TSMC-1038, 7:61-67 (teaching that vias having circular cross-sections benefit from more precisely controlled etching, improved coverage of barrier metal in the via opening, and easier fill-in of the via opening with a metal film). Additionally, circular-shaped vias also provide improved reliability due to the lack of sharp corners that can concentrate stress and cause damage in the form of dielectric cracking and the like.

218. While there can sometimes be operational or design considerations that lead to a preference for circular or square vias, a POSITA nonetheless recognized that the fundamental stress-relieving function of Watanabe's dummy via (or the electrical connection function of Watanabe's via) in terms of attracting and sequestering vacancies, preventing void formation, and providing a surplus of copper atoms, would be roughly the same with both circular and square dummy vias. That is because these functions do not generally depend on the exact cross-sectional shape of the dummy via. To the extent some minor differences in performance exist, implementing circular vias would have promoted greater consistency with

Watanabe's simulation results which were based on circular-shaped vias. A POSITA would have further recognized that neither the structural strengthening functions of Watanabe's dummy via, nor the electrical connection function of Watanabe's functional via, would be materially altered by adopting a circular cross-section versus a square. Indeed, both circular and square vias would still strengthen the overall layers of Watanabe's device and reduce the mechanical stress exhibited at the functional vias.

219. Further, because a POSITA was aware of these shapes, and was aware of the role of the dummy vias in mitigating stress-induced voiding and electromigration problems as taught, for example, by Watanabe (*supra*, §IX.A), it would have been a matter of routine optimization to choose the via shape that works best for a given overall design. I understand that the Examiner suggested the same during prosecution. TSMC-1002, 244-45, 292-96. With a few basic shapes to choose from (e.g., circular, square, rectangular), it would not have required an undue amount of experimentation to arrive at the optimal via shape.

220. A POSITA understood that there was no criticality associated with having a circular via or dummy via shape and that such circular-shaped vias would have operated substantially the same as other shapes. That is, there was no surprising or unexpected performance benefit associated with circular vias as opposed to other shaped-vias. Any difference in performance was well understood and something

that a POSITA would have balanced with other considerations (such as manufacturing limitations, costs, etc.) when choosing the appropriate shape for the functional and dummy vias for a given application. In this regard, I note that the '623 patent teaches no criticality or surprising or unexpected results with respect to the cross-sectional shape of its vias or dummy vias, reinforcing my opinion that such shapes were nothing more than a matter of routine design choice.

221. A POSITA would have had a reasonable expectation of success in implementing Watanabe's vias (both functional and dummy) with circular shapes. Circular vias were standard in the industry. Indeed, as demonstrated by Iizuka (and other references at the time) as well as the modeling of Watanabe discussed above, circular vias (including dummy vias) were routinely used in semiconductor devices and thus their fabrication and associated techniques was well understood. *See also* TSMC-1005, Fig. 19A; TSMC-1014, ¶[0091]; TSMC-1013, 8:47-52; TSMC-1038, 7:62-67. Iizuka itself teaches both circular vias and methods for successfully filling such small-diameter via holes, as far back as its 1993 publication date. TSMC-1008. A POSITA would view the choice of via shape as a routine design parameter (subject to routine optimization as noted by the Examiner during prosecution (TSMC-1002, 244-45, 292-96)). Indeed, for each semiconductor design a POSITA would understand the various via shape options (e.g., square, circle, rectangle) and would select from those known shapes basically on the specific application design needs.

Modifying Watanabe's square vias (or implementing its modeled circular vias) to be explicitly circular would not have involved any inventive step while being readily achievable using known fabrication techniques. Indeed, as discussed repeatedly herein, circular vias (both functional and dummy) were well-known and widely used and thus a POSITA would not have expected any significant hurdles or problems when implementing them.

D. Ground 3: Claim 5 Is Obvious Over Watanabe, Iizuka, and Kurashima

222. Watanabe, Iizuka, and Kurashima renders claim 5 obvious to a POSITA.

223. Claim 5 depends from claim 2 (which depends from claim 1). The analysis in Ground 1A demonstrates how Watanabe discloses both claims 1 and 2.

1. Claim 5

a) [5.a] – "*semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view*"

224. Element [5.a] recites the "semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view," which Watanabe, Kurashima, and Iizuka render obvious.

225. For the same reasons I already discussed above for limitation 23.a (*supra*, §X.C.1-2), it was obvious to form Watanabe's dummy plugs 34/52 (i.e.,

dummy vias) with a substantially circular shape in a plan view. Watanabe discloses a simulation model with conductive plug 32 ("via") and dummy plug 34 ("dummy via") as a "circular cylinder," i.e., disclosing them to the POSITA as substantially circular in plan view. TSMC-1004, ¶[0083], Figs. 1, 3. A POSITA would recognize that the same applies to dummy plugs 52 in all of Watanabe's embodiments. *E.g.*, *id*., Fig. 9. Disclosing the circular cylinder shape for its simulation model suggests circular vias to a POSITA for Watanabe's devices, since this is the shape on which Watanabe's modeling was done. A POSITA would thus interpret Watanabe as disclosing vias having circular cross-sections in plan view, in addition to the square vias disclosed in the figures.

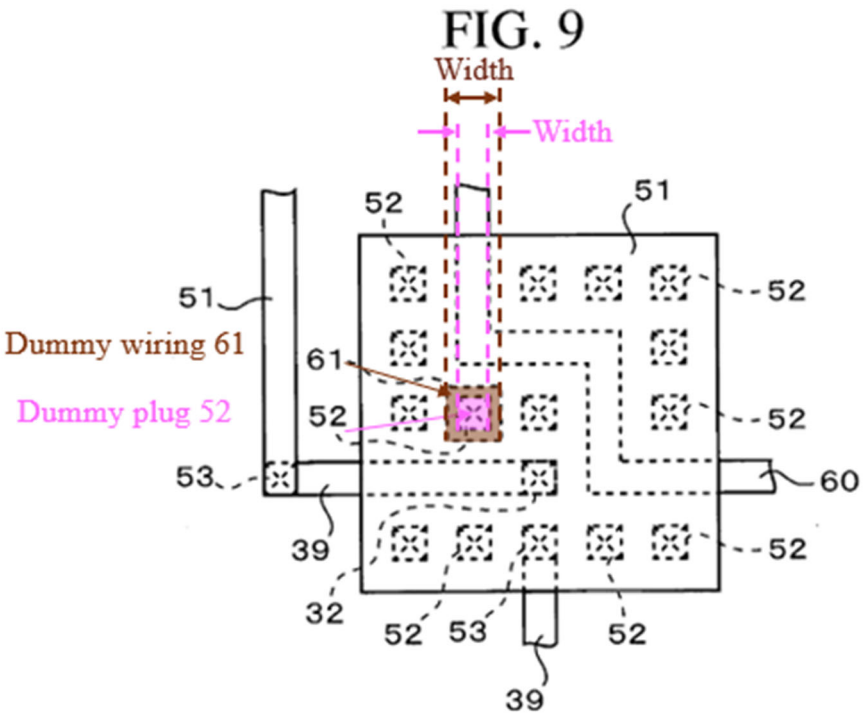
226. Like Watanabe, Iizuka is directed to a "semiconductor device" in which "via-holes" are formed. *See* TSMC-1008, Abstract. Iizuka demonstrates that it was well-known prior to the '623 patent that vias could have many polygonal cross-sectional shapes and that the selection of a specific shape was simply a design choice. For example, Iizuka teaches the common nature of circular via-holes and the interchangeability with other common shapes such as squares: "the opening of the via-hole may have any configuration, such as a **square**, rectangle **or circle**." *Id*., 9:45-47 (emphasis added). Iizuka's description of via-hole 6 as having a "diameter" similarly discloses a circular via shape, since the geometrical term "diameter" corresponds with circular shapes. *Id*., 6:60-63, Fig. 5A.

227. Thus, a POSITA understood that circular-shaped vias were common and standard in the industry, as evidenced by Iizuka, and would have understood that the dummy plugs 34 and 52 in Watanabe could be made to be substantially circular in a plan view. This is further evidenced, for example, by Hasunuma, which shows circular vias/dummy vias in various embodiments. *See, e.g.*, TSMC-1005, ¶[0200], Fig. 19A (showing circular-shaped dummy vias 125); *see also* TSMC-1013, 8:47-52 (noting that circular vias may be used, among other shapes). Also, Igarashi teaches circular vias as the default shape for all via connections, except where square vias or other shapes are needed for a given overlap of the upper and lower interconnects. TSMC-1014, ¶¶[0091]-[0092], Figs. 8, 14 (teaching circular vias as a default shape, and square vias as preferred for certain interconnect junctions). Thus, a POSITA understood that square and circular shapes are among a finite number of common, interchangeable design choices for via/dummy via shapes, and circular vias were well-known, as expressly taught by Iizuka, among others. For the additional reasons discussed previously, it was obvious to implement Watanabe's dummy plugs 34/52 with a substantially circular shape given Iizuka's teaching that circular vias were a known, interchangeable design alternative, as well as the widespread knowledge of this at the time. *Supra*, §X.C.2.

b) [5.b] – "*a diameter of the dummy via is substantially equal to a width of the first dummy interconnect*"

228. Element [5.b] calls for "a diameter of the dummy via is substantially equal to a width of the first dummy interconnect," which Watanabe and Kurashima and Iizuka render obvious.

229. Watanabe's fifth embodiment in annotated Figure 9 discloses dummy plug 52 ("dummy via") with a width that is slightly smaller than a width of the dummy wiring 61 ("first dummy interconnect") to which it connects:



TSMC-1004, ¶[0127], Fig. 9.

230. Kurashima shows an example in annotated Figure 3A where the dummy wire 17 has a width that is equal to a width of the Cu-dummy wire 10 beneath it to which it connects:

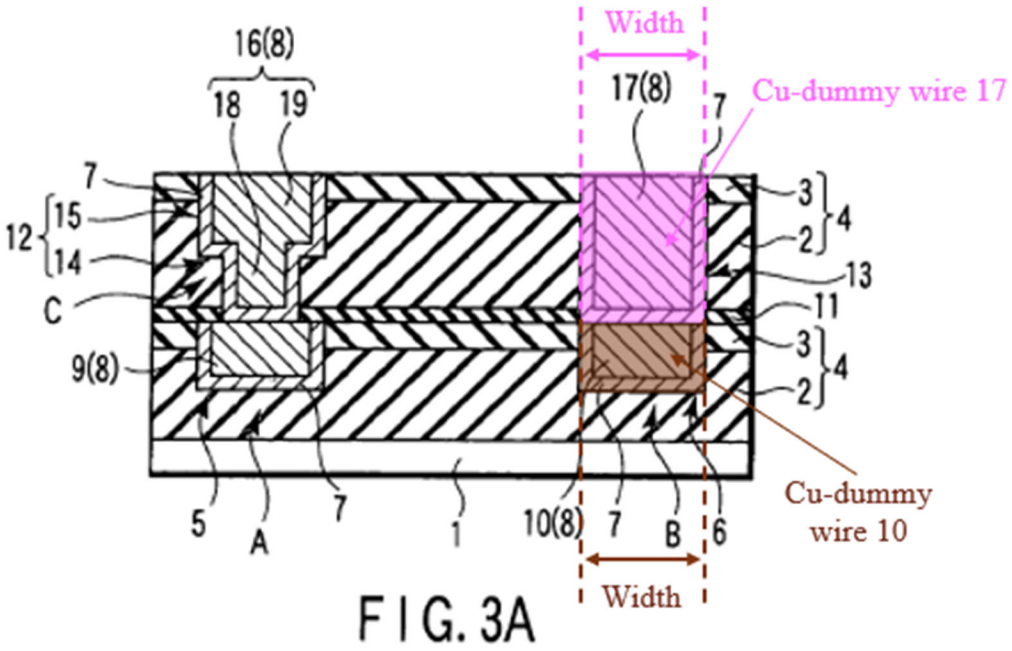


FIG. 3A

TSMC-1011, Fig. 3A. As understood by the POSITA, Kurashima teaches that the width of the dummy wire ("dummy via") is the same as the width of the dummy wire ("dummy interconnect") beneath it to which it connects. For the reasons discussed the section immediately below, it was obvious, in view of Kurashima, for Watanabe's dummy plug 52 ("dummy via") to have a diameter/width matching the width of underlying dummy wiring 61 ("first dummy interconnect").

2. Combination of Watanabe, Iizuka, and Kurashima

231. It would have been obvious to a POSITA, based on Kurashima, to match a diameter of Watanabe's resulting circular dummy vias (dummy plugs 34/52) to the width of an underlying first dummy interconnect (dummy wiring 61) to which the dummy via connects. A POSITA understood that dummy via dimensions

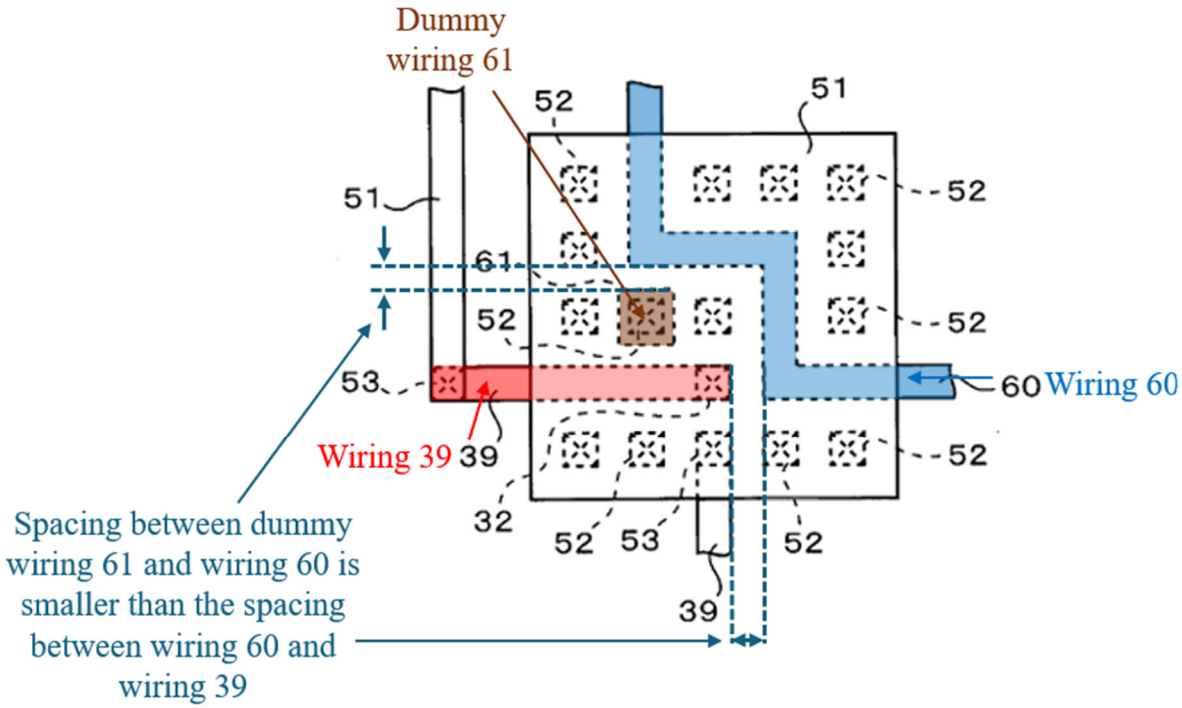
matching the width of the underlying dummy interconnect would allow for ensuring a secure connection while minimizing the space taken up by the underlying dummy wiring and minimizing undesired parasitic capacitance and cross-talk with adjacent, active wirings. Indeed, Kurashima's approach is a natural design choice commonly recognized by the POSITA.

232. Watanabe already discloses that its conductive plugs 53, dummy plugs 52, and wirings 39 and 51 (the left-hand-most wiring 51 in Figure 9) all have equal widths, suggesting that the choice of the dummy wiring 61 width is based on common design choices, and that it would have promoted uniformity and simplicity to make its width equal to the other elements such as the dummy plugs 52. Furthermore, a POSITA would have been affirmatively motived to make dummy wiring 61's width match that of dummy plug 52 to reduce unwanted parasitic capacitance and crosstalk between adjacent structures that are not electrically connected/not at the same potential.

233. In Watanabe's Figure 9, dummy wiring 61 and interconnect 60 are not shown to be electrically connected to each other, such that a POSITA would presume they are not so connected and experience different potentials during device operation. However, as Figure 9 shows, the upper edge of dummy wiring 61 is actually closer to interconnect 60 as compared to the spacings of all other features

shown, such as the spacing between interconnects 39 and 60, for example, which are also not electrically connected:

FIG. 9



234. This closer spacing between the upper edge of dummy wiring 61 (which is at the same potential as active interconnect 51 given their connection to each other from dummy plug 52) and interconnect 60 would lead to more parasitic capacitance and crosstalk between them as compared to two structures held at a greater spacing apart, such as the spacing between wirings 39 and 60. Watanabe itself expressly acknowledges this problem of inter-wiring capacitance. TSMC-1004, ¶[0034]. A POSITA would have been motivated to reduce the size of dummy wiring 61 to have the same dimension of dummy plug 52 (and thereby the same dimension as the first

interconnect 39) so that a uniform spacing is achieved between dummy wiring 61 and interconnect 60, i.e., the same spacing as seen between interconnect 39 and interconnect 60. Accordingly, a POSITA would have appreciated the benefits of reducing the size of Watanabe's dummy wiring 61 to match the width of the dummy plug 52 to which it is attached (which itself has the same width as wirings 39, 60) for the purpose of minimizing parasitic capacitances and crosstalk between wiring 60 and dummy wiring 61 (which is at the potential of the second interconnect 51). This would result in dummy wiring 61 having a width that matches the width of both the dummy plug 52 and the first level interconnect 39 (and wiring 60).

235. In addition, a POSITA would have appreciated that the dimensions of Watanabe's dummy wiring 61 and the dummy plug 52 to which it is connected could be made equal simply by enlarging dummy plug 52 to match dummy wiring 61 as shown in Watanabe's Figure 9. A motivation for making this modification would be to achieve better interfacial adhesion between dummy wiring 61 and dummy plug 52 due to their increased contact area under this scenario for greater mechanical stability, as taught by Kurashima. TSMC-1011, 6:11-32; 6:58-8:54, 9:16-23, Figs. 2C, 3A. This would be easily achieved by adding more dummy wirings under dummy plugs like dummy wiring 61 shown in Figure 9, but with the dummy wiring dimensions matching those of the dummy plugs 52.

236. Either approach described above (widening dummy plug 52 to match wiring 61's width, or reducing wiring 61's width to match dummy plug 52) would avoid sharp corners where the dummy plug connects to the dummy wiring, having the benefit of reducing stress concentration at their junction.

237. Coupled with Watanabe's and Iizuka's teaching of circular shaped vias (TSMC-1004, ¶[0083]; TSMC-1008, 9:45-47), the resulting combination would be a circular-shaped dummy via (dummy plug 52) with a diameter equal to the width of the dummy interconnect (dummy wiring 61).

238. A POSITA would have had a reasonable expectation of success in implementing Watanabe's dummy vias with circular shapes having diameters substantially equal to the dummy interconnect because Iizuka confirms that circular-shaped vias were standard. TSMC-1008; 9:45-47; *see also* TSMC-1005, ¶[0200], Fig. 19A; TSMC-1013, 8:47-52; TSMC-1014, ¶[0091]; TSMC-1038, 7:62-67. This configuration would have been easily accomplished using the standard patterning and manufacturing techniques used to make the interconnect structure in general. *Id*. These references show that it was well known how to pattern via holes having circular cross-sections using masks, photolithography, and etching, and such round patterns subsequently result in circular vias when conductive material is deposited into the patterned vias holes. It was likewise straightforward to set the via diameter equal to the dummy interconnect width, as Kurashima taught.

239. Such sizing was a standard design practice that was achievable with the same manufacturing process disclosed in Watanabe, and thus a POSITA would have expected implementing same size/width/diameter vias and interconnects to succeed. Slightly modifying the resulting diameter of a circular dummy via to be equal to a width of the dummy interconnect would at most involve routine optimization to arrive at a configuration where the dummy via and dummy interconnect have the same cross-sectional dimension, which was already demonstrated to be known by Kurashima. At a minimum, the dummy via width relative to the dummy interconnect dimension would impact the contacting surface area between the two, and thus the strength of their adhesion to each other. The size of each also impact parasitic capacitance and cross talk with adjacent structures.

240. Such a design would have been readily achievable with Watanabe's existing manufacturing processes. Accordingly, it would have been obvious for a planar shape of each of Watanabe's dummy plugs 52 ("dummy vias") to be substantially a circle, and have substantially the same diameter as the width of the dummy wiring 61 ("first dummy interconnect").

E. Ground 4: Claim 6 Is Obvious Over Watanabe and Kurashima

241. Watanabe and Kurashima render claim 6 obvious to a POSITA. Watanabe discloses claims 1 and 2, as outlined above.

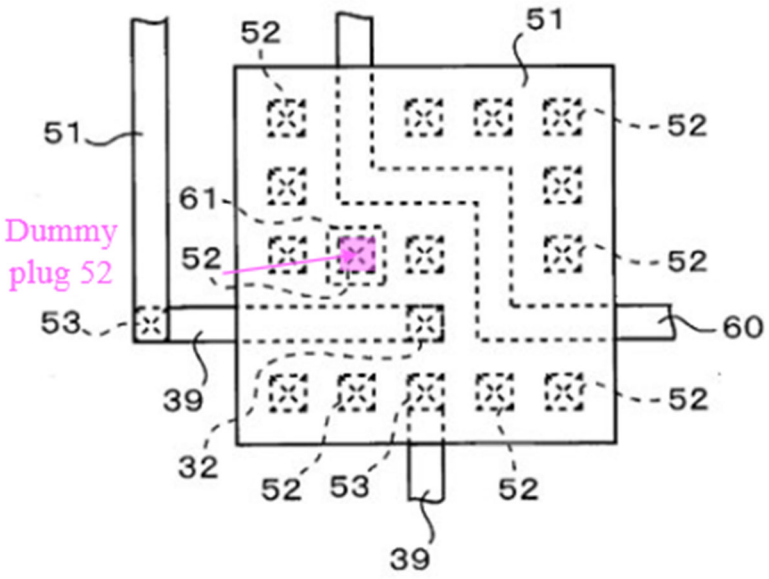
1. Claim 6

a) [6.a] – "*semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square*"

242. Element [6.a] recites the "semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square," which Watanabe and Kurashima render obvious.

243. Figure 9 of Watanabe (fifth embodiment) discloses dummy plug 52 ("dummy via") with a square planar shape:

FIG. 9



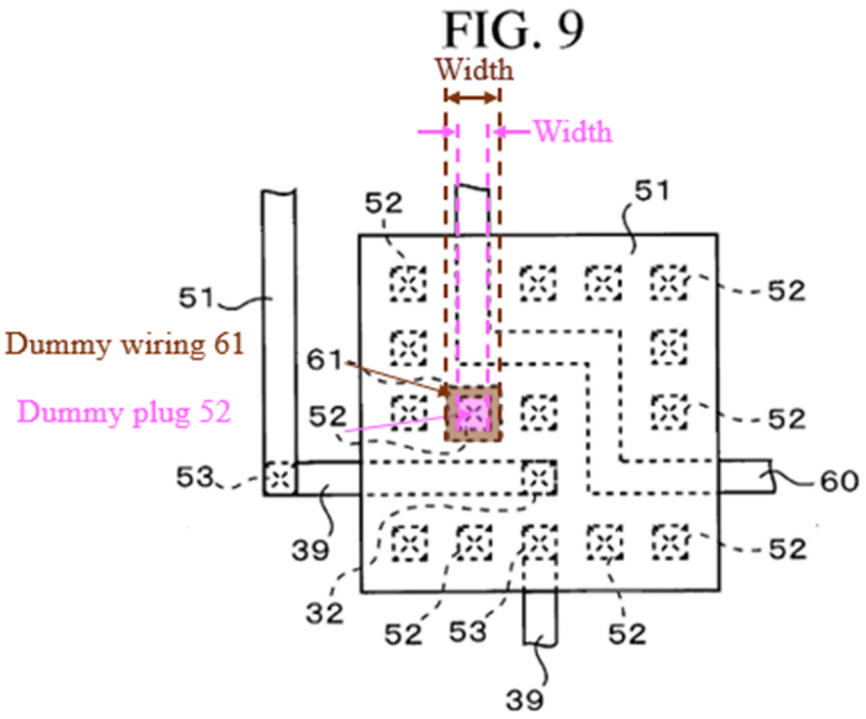
TSMC-1004, Fig. 9. Moreover, a POSITA understood the common nature of square shaped vias. *See also* TSMC-1008, 9:45-47 ("It will be also understood that the opening of the via-hole may have any configuration, such as a square, rectangle or circle."), 10:8-11; TSMC-1013, 9:45-49 ("[T]he shape of dummy via holes are indicated by squares, rectangles, and line patterns. The shapes of the dummy wiring

patterns and dummy via holes may take other shapes."); TSMC-1039, 5:27-32 (noting the greater contact area achieved with square vias). Thus, Watanabe discloses substantially square cross-sections to be a disclosed shape for dummy plugs 52 (and 34).

b) [6.b] – "*a side of the dummy via is substantially equal to a width of the first dummy interconnect*"

244. Element [6.b] calls for "a side of the dummy via is substantially equal to a width of the first dummy interconnect," which Watanabe and Kurashima render obvious.

245. In Watanabe's fifth embodiment, annotated Figure 9 discloses dummy plug 52 ("dummy via") with a width that is slightly smaller than a width of the dummy wiring 61 ("first dummy interconnect") to which it connects (TSMC-1004, ¶[0127], Fig. 9):



246. Kurashima shows an example in annotated Figure 3A where the dummy wire 17 has a width that is equal to a width of the Cu-dummy wire 10 beneath it to which it connects (TSMC-1011, Fig. 3A):

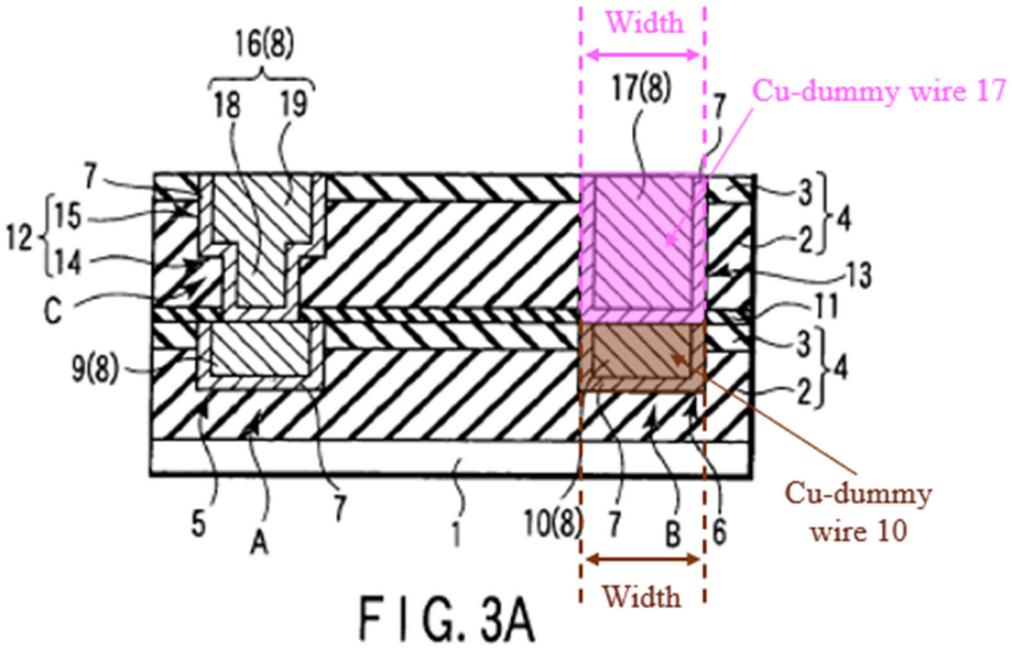


FIG. 3A

247. As recognized by a POSITA, Kurashima discloses that the width of the dummy wire ("dummy via") is the same as the width of the dummy wire ("dummy interconnect") beneath it to which it connects. A POSITA understood that a dummy via width matching that of an underlying dummy interconnect facilitates a secure connection between them (i.e., good adhesion) while minimizing the space taken up by the underlying dummy interconnect. Kurashima's approach is a natural design choice commonly recognized by the POSITA. It would have been obvious to employ such a design approach in Watanabe. *Supra*, §X.D.2.

248. As outlined above in connection with claim 5, Watanabe already discloses that its plug 53, dummy plugs 52, and wirings 39 and 51 (the left-hand-most wiring 51 in Figure 9) all have equal widths, suggesting that the choice of the

dummy wiring 61 width is based on common design choices, and that it would have promoted uniformity and simplicity to make its width equal to the other elements such as the dummy plugs 52. Furthermore, a POSITA would have been affirmatively motivated to make dummy wiring 61's width match that of dummy plug 52 for the same reasons I described previously as to claim 5 – namely to reduce unwanted parasitic capacitance and crosstalk between adjacent structures that are not electrically connected/not at the same potential. *Supra*, §X.D.2. Specifically, a POSITA would have appreciated the benefits of reducing the size of Watanabe's dummy wiring 61 to match the width of the dummy plug 52 to which it is attached (which itself has the same width as wirings 39, 60) for the purpose of minimizing parasitic capacitances and crosstalk between wiring 60 and dummy wiring 61 (which is at the potential of the second interconnect 51). *Supra*, §X.D.2. This would result in dummy wiring 61 having a width that matches the width of both the dummy plug 52 and the first level interconnect 39 (and wiring 60).

249. In addition, a POSITA would have appreciated that the dimensions of Watanabe's dummy wiring 61 and the dummy plug 52 to which it is connected could be made equal simply by enlarging dummy plug 52 to match dummy wiring 61 as shown in Watanabe's Figure 9. A motivation for making this modification would be to achieve better interfacial adhesion between dummy wiring 61 and dummy plug 52 due to their increased contact area under this scenario for greater mechanical

stability. This would be easily achieved by adding more dummy wirings under dummy plugs like dummy wiring 61 shown in Figure 9, but with the dummy wiring dimensions matching those of the dummy plugs 52.

250. As another approach, Watanabe's dummy plugs 52 could be widened to match the dimension of dummy wiring 61 to further improve the interfacial adhesion between the two, as taught by Kurashima. TSMC-1011, 6:11-32; 6:58-8:54, 9:16-23, Figs. 2C, 3A.

251. Either approach described above (widening dummy plug 52 to match wiring 61's width, or reducing wiring 61's width to match dummy plug 52) would avoid sharp corners where the dummy plug connects to the dummy wiring, having the benefit of reducing stress concentration at their junction.

252. There would have been a reasonable expectation of success in implementing such equal widths, because Kurashima demonstrates that a POSITA would have known how to implement the sizing change and Watanabe already discloses vias/interconnects with equal widths. There would be a high expectation of success, because Kurashima shows that a POSITA would have known how to implement the sizing change. *See also supra*, §X.D.2.

F. Ground 5: Claims 29 and 30 Are Obvious Over Watanabe and Nasu

253. Watanabe and Nasu render claims 29 and 30 obvious as detailed below.

1. Claim 29

a) [29.a] – "*semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view*"

254. Element [29.a] recites the "semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view," which Watanabe in view of Nasu discloses.

255. Watanabe's simulation model describes its conductive plugs 32 ("vias") and dummy plugs 34 ("dummy vias") as "circular cylinders." TSMC-1004, ¶[0083]. As established previously for claims 5 and 23, given Watanabe's own simulation model and other prior art known to a POSITA (e.g., Iizuka), it would have been obvious to a POSITA to form Watanabe's functional conductive plugs 32 (vias) and dummy plugs 34 (dummy vias) with a circular shape, and a POSITA would have had a reasonable expectation of success in doing so. *Supra*, §§X.C.1-2, X.D.1-2..

256. Nasu also describes vias and dummy vias having specific "diameters." TSMC-1032, ¶[0023]. Nasu's consistent reference to the "diameter" of both via hole pattern 9 and dummy hole pattern 8 indicates to a POSITA that these via openings, and thus the vias formed within them, are circular in their planar shape, given that "diameter" is the standard dimensional term for features having a circular shape.

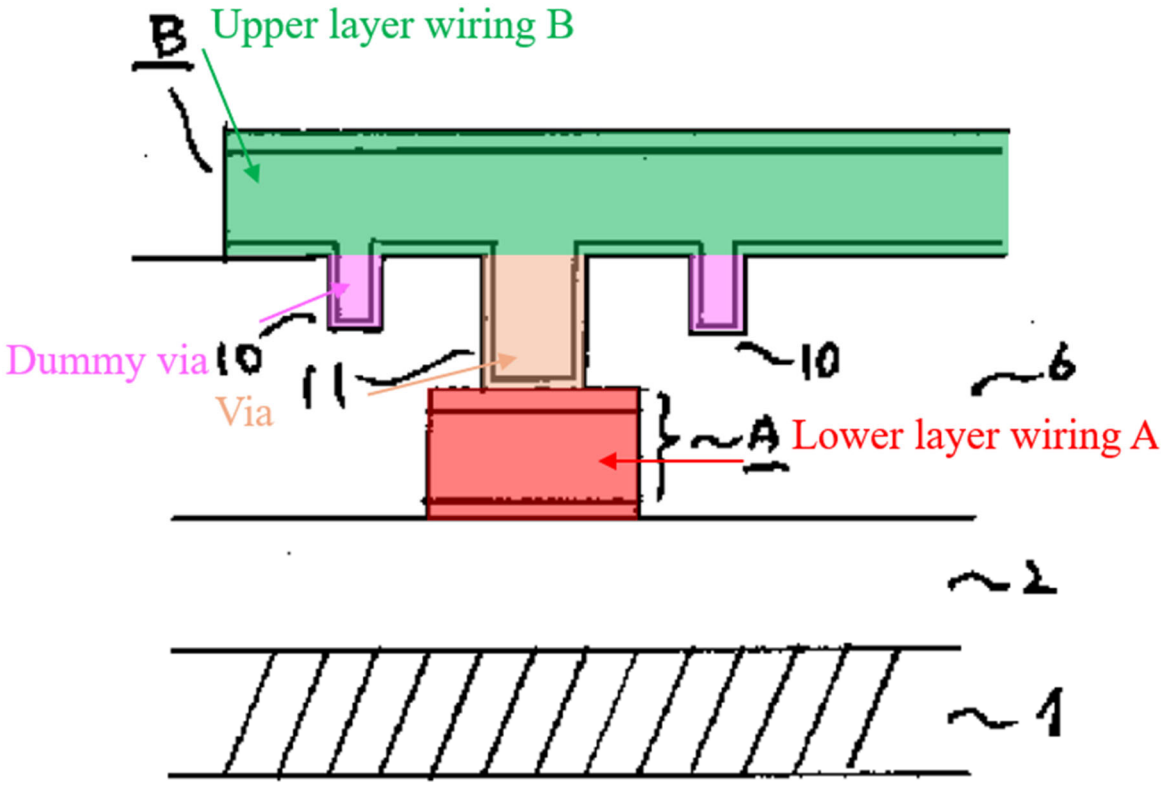
257. Given Watanabe's own use of circular models, Nasu's teaching of circular vias, and the obviousness of circular vias in general (*supra*, §§X.C.1-2), it was obvious to implement both the functional via and the dummy via of Watanabe with substantially circular planar shapes, for the reasons discussed *supra*, §§X.C.1-2, X.D.1-2, and *infra*, §X.F.3. The motivation would be design choice, manufacturing or stress benefits, and/or consistency with Watanabe's simulation models, with a high expectation of success as circular vias were standard.

b) [29.b] – "*a diameter of the dummy via is smaller than a diameter of the via*"

258. Element [29.b] calls for "a diameter of the dummy via is smaller than a diameter of the via," which Watanabe in view of Nasu renders obvious.

259. Nasu discloses improving wiring reliability, with a specific focus on electromigration (EM). *Id*., Abstract. Nasu's wiring structure includes lower and upper wirings, where upper layer wiring B connects to lower wiring A through the via in via hole 11. *Id*., ¶¶[0022]-[0028], Figs. 1, 5. To address electromigration, Nasu teaches forming one or more dummy vias by embedding part of upper layer wiring B in dummy holes 10 that are placed along the upper layer wiring B near via hole 11; these dummy vias serve as a supply source for Al or Cu atoms to help replace metal atoms that have "migrated" away due to the flowing electron current, thereby protecting the structures against void formation due to electromigration. *Id*.,

Abstract, ¶[0013], Figs. 2-3. Notably, Nasu teaches that its dummy holes 10 do not reach lower wiring A because they are less deep than the active via in via hole 11, as seen below:



Id., ¶¶[0024], [0027], Figs. 3, 5.

260. Nasu achieves this by forming dummy hole pattern 8 with a smaller diameter than via hole pattern 9 (which is used to create the active via). *Id.*, ¶[0023]. For example, Nasu discloses a hole pattern 9 diameter of 0.45 µm and a dummy hole pattern 8 diameter of 0.30 µm or less. *Id.* Nasu's reference to "diameter" indicates that these via openings are circular in their planar shape, which a POSITA would understand to lead to vias/dummy vias formed within those holes also having a

substantially circular planar shape. *Id*. When holes 10 and 11 are etched into the insulating layer through the hole patterns 8 and 9, the smaller diameter of dummy hole pattern 8 causes the hole to etch more slowly than those through hole pattern 9, due to the micro-loading effect. *Id*., ¶¶[0024], [0028], Fig. 3. This slower etching rate for the smaller-diameter holes results in shallower dummy holes 10 as compared to via hole 11 (i.e., dummy via holes 10 end up less deep than the via hole 11).

261. A POSITA, looking to apply this teaching to Watanabe's structure for improved wiring reliability as taught by Nasu, would have found it obvious to make Watanabe's dummy plugs 34 with a smaller diameter than its conductive plugs 32, as expressly taught by Nasu and discussed further below (*infra*, §X.F.3)..

262. A POSITA would have had a reasonable expectation of success in making the dummy plugs 34 in Watanabe with a smaller diameter than the conductive plugs 32, because Nasu shows how to use hole patterns with different diameters to make a dummy via with a smaller diameter than a via, and this was easily achieved by a POSITA using standard and well-known patterning and processing techniques.

2. Claim 30

a) [30.a] – "*semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square*"

263. Element [30.a] recites the "semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square," which Watanabe in view of Nasu renders obvious.

264. Watanabe's plan view figures (e.g., Figures 2, 4, 5A-5C, 9) consistently disclose square vias and square dummy vias. TSMC-1004, Figs. 2, 4, 5A-5C, 9. In particular, the plugs 32, dummy plugs 34, dummy plug 52, and plug 53 are all disclosed as having a substantially square shape in Watanabe. *Id*. Square vias were also a generally known shape for vias that was preferred in many instances. TSMC-1005, Fig. 18A; TSMC-1014, ¶[0092] (disclosing square vias as preferred for certain interconnect junction geometries), Figs. 8, 14; TSMC-1039, 5:27-32 (noting the increased electrical contact area achieved by square vias).

265. Nasu also discloses square-shaped via holes 11 and square dummy holes 10 as demonstrated in annotated Figure 6 below:

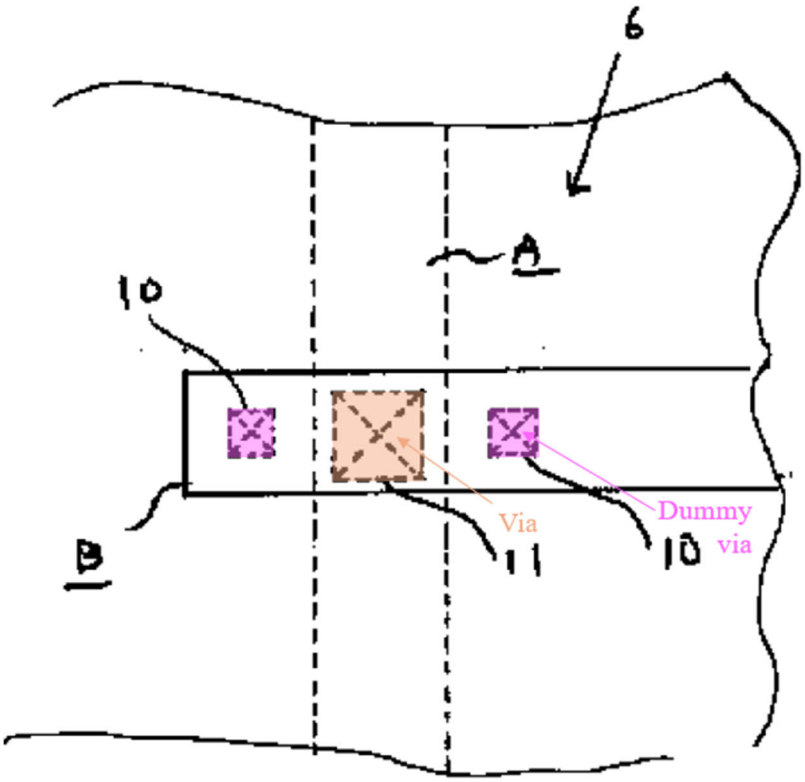


FIG. 6

TSMC-1032, Fig. 6.

b) [30.b] – "*a side of the dummy via is smaller than a side of the via*"

266. Element [30.b] calls for "a side of the dummy via is smaller than a side of the via," which Watanabe in view of Nasu renders obvious.

267. Although Watanabe discloses vias and dummy vias having the same size, a POSITA would have found it obvious to apply Nasu's teaching of making the dummy vias smaller than the functional vias. TSMC-1032, ¶¶[0023], [0028].

Indeed, Nasu discloses in annotated Figure 6 vias and dummy vias, where the dummy vias 10 are smaller than the via 11:

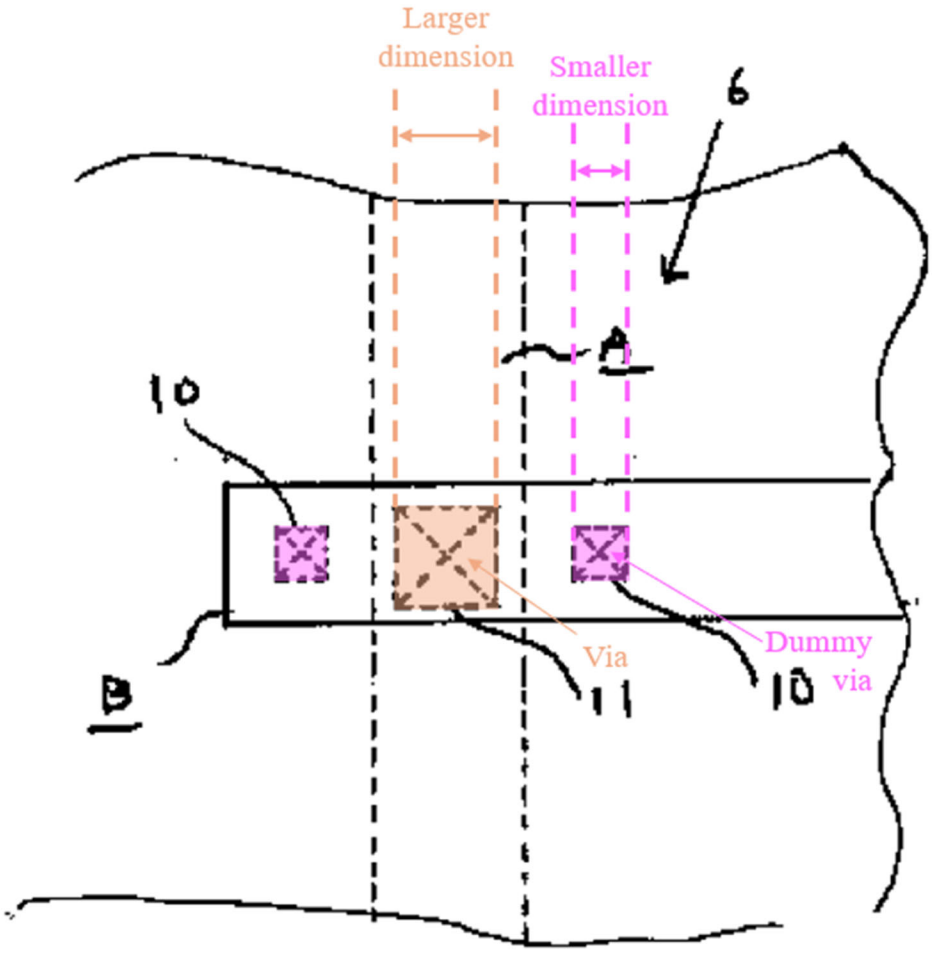


FIG. 6

Id., Fig. 6. A POSITA would thus have understood that Nasu's teachings on relative sizing applied regardless of whether the via is circular or square.

268. If both the via and dummy via are square as in Watanabe, and the dummy via is made dimensionally smaller than the functional via per Nasu's teaching, then a side of the dummy via would necessarily be smaller than a side of

the functional via. This modification would be motivated by the reasons discussed in Nasu for having a dummy via smaller than a via, including improving wiring reliability. *Id*., Abstract, ¶¶[0013], [0022]-[0028], Figs. 1-3, 5. A POSITA would have had a high expectation of success in making a side of the dummy via smaller than a side of the via, because Nasu demonstrates that fabricating vias of different, controlled sizes in the same device was a known capability, and it could have been accomplished using Watanabe's basic manufacturing process.

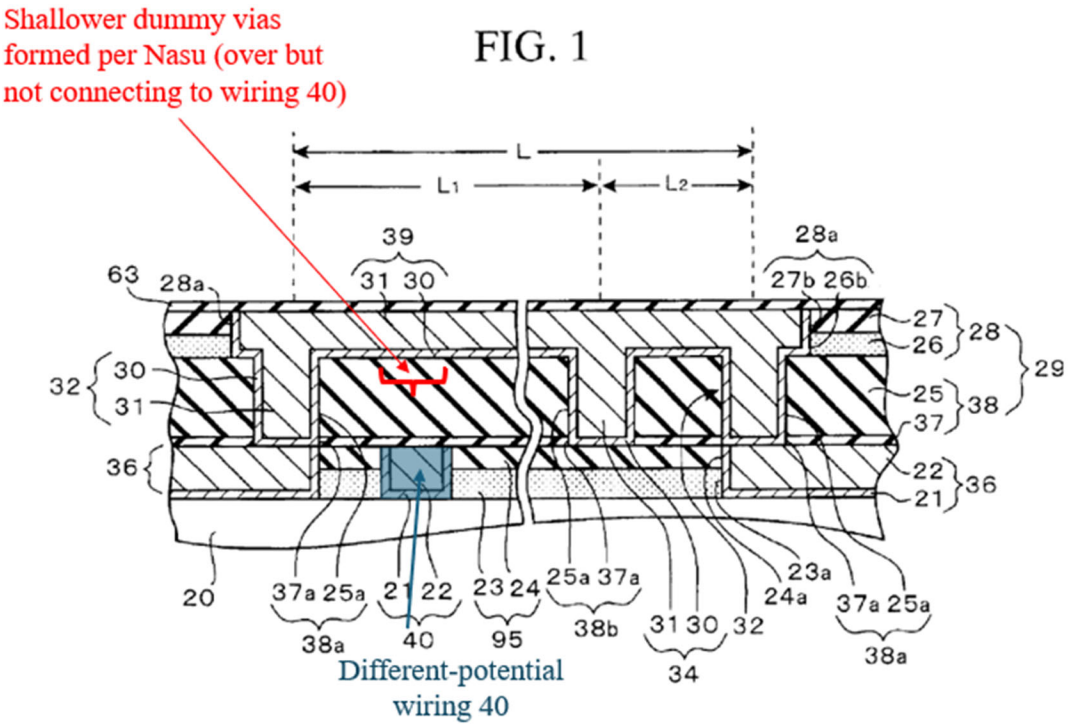
3. Combination of Watanabe and Nasu

269. Whether implemented with circle or square shapes, a POSITA would have been motivated to combine the teachings of Nasu with Watanabe to enhance the reliability of Watanabe's multilayer interconnect structures. Both references address reliability issues by incorporating dummy via structures near functional vias. *Supra*, §§IX.A, IX.E. Watanabe provides a robust framework for dummy vias formed concurrently alongside functional vias, aimed at mitigating both stress migration and electromigration. TSMC-1004, ¶¶[0016]-[0017], [0022], [0026], [0077].

270. Nasu likewise specifically teaches forming dummy vias, but with smaller sizes than the functional vias. TSMC-1032, ¶¶[0022]-[0028], Figs. 1-6. Nasu explains that a smaller dimension for the dummy via hole, results in shallower dummy features when the holes for the vias and dummy vias are simultaneously

etched, allowing the dummy vias do not reach the lower wiring while still serving as "material reservoirs" to assist in preventing electromigration (*id*.), a problem expressly recognized likewise by Watanabe (TSMC-1004, ¶[0077]).

271. A POSITA would have been motivated to implement Nasu's smaller-sized dummy vias (whether having circular or square cross sections) in Watanabe's structure because Nasu's teachings help optimize dummy via layout density. For example, forming dummy vias having a shallower depth than the functional vias allows dummy vias to be formed in areas over lower-level interconnects that cannot be electrically connected to the upper-level interconnect from which the dummy vias depend. Watanabe's Figure 1 illustrates an example of this, where lower interconnect 40 is intended to be electrically isolated from interconnects 36 and 39 (TSMC-1004, ¶[0079]):



Similarly, implementing Nasu's smaller diameter—and therefore shallower—dummy vias would also allow dummy vias (i.e., Watanabe's dummy plugs 52) to be added to the second interconnect 51 of Watanabe's fifth embodiment (Figure 9) in areas directly over interconnect 60. Watanabe's Figures 5 and 9 show a desire to include many dummy vias, and implementing Nasu's teachings further promotes this goal by allowing dummy vias to also be placed where they otherwise could not be due to underlying interconnects.

272. Furthermore, while active vias are typically sized to match the width of the underlying interconnect (*infra*, §X.L.1.(b)), and must meet a minimum threshold size to carry sufficient current for device, dummy vias by definition carry no current, and thus are free to be made smaller than the active vias. A POSITA appreciated

that via stress gradients increase inversely with via diameter. TSMC-1036, 319 (nothing that "the stress gradient across the bottom of the via is roughly doubled as via dimension is halved," and "the stress gradient will scale inverse to the via size").

273. A POSITA thus also appreciated that vias/dummy vias with a smaller diameter have a higher stress gradient, which was known to attract more vacancies migrating in the interconnect, since vacancies tend to travel to areas of high stress. *Id*., 315 ("[T]he stress gradient region [] is where a significant driving force exists to compel vacancies to migrate towards a specific voiding site."). Indeed, the prior art specifically reports using dummy vias to attract vacancies (*e.g*., TSMC-1009, ¶¶[0017], [0085]-[0088]), and studies have confirmed that smaller vias attract more vacancies, particularly in regard to a fixed interconnect size (TSMC-1037, 163, 165, Figs. 8, 14 (noting the increasing via failure rate due to stress-induced voiding (i.e., vacancy accumulation) as vias size decreases)).

274. Accordingly, a POSITA would have appreciated that Nasu's approach of using smaller-sized dummy vias (compared to the active vias) has the added benefit of better attracting and sequestering vacancies so that they do not reach/accumulate in active vias where void formation can be fatal to device operation. A POSITA was therefore motivated to implement Nasu's teachings to further refine the dummy via's role in managing material diffusion or local stress

within Watanabe's device by expanding the ability to create tailored reservoir-like structures that better attract vacancies and reduce void formation at active vias.

275. Fabricating vias/dummy vias of different, controlled sizes in the same device was a known capability as demonstrated by Nasu, leading to a high expectation of success in implementing such a combination. While Nasu teaches both circular and square vias, choosing a basic via shape (circular vs. square) was a routine design parameter, and a POSITA considering the via shape would understand Nasu's teachings on relative sizing are applicable regardless of whether the via is circular or square.

G. Ground 6: Claim 31 Is Obvious Over Watanabe and Fujii

276. Watanabe and Fujii render claim 31 obvious to a POSITA.

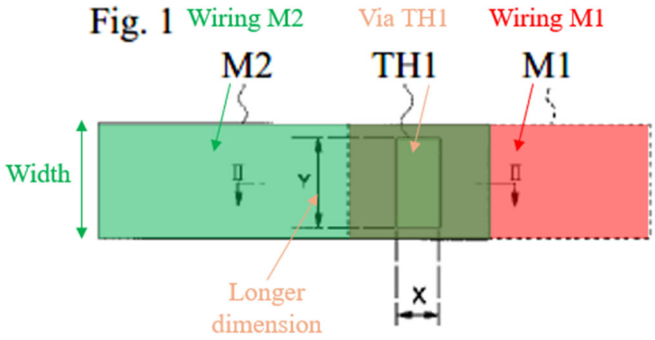
1. Claim 31

a) [31.a] – "*semiconductor device of claim 1, wherein the dummy via is substantially rectangular in a plan view*"

277. Element [31.a] recites the "semiconductor device of claim 1, wherein the dummy via is substantially rectangular in a plan view," which Watanabe and Fujii render obvious.

278. Watanabe discloses in each of Figures 2, 4, and 9 (embodiments 1, 2, and 5) that dummy plug 34 or dummy plug 52 ("dummy via") each have a substantially square planar shape. TSMC-1004, Figs. 2, 4, 9.

279. Fujii teaches forming a rectangular connection hole/via having its longer dimension (Y) oriented along the upper-level wiring (M2)/second interconnect's width (i.e., its shorter side), i.e., orthogonal to current flow, as shown in annotated Figure 1:



TSMC-1030, ¶¶[0016], [0052], Fig. 1.

280. Indeed, such rectangular shapes were commonplace and, thus, a POSITA would have expected success making the dummy via substantially rectangular in a plan view. Yamaha discloses rectangular dummy vias: "The cross section of a dummy via hole is not limited to a particular shape shown in the figure, but any shape may be used…. For example, a rectangle … may be used." TSMC-1013, 8:48-52. Iizuka likewise discloses rectangular via shapes: "the opening of the via-hole may have any configuration, such as a square, **rectangle** or circle." TSMC-1008, 9:45-47 (emphasis added).

b) [31.b] – "*a longer side of the dummy via in a plan view and a shorter side of the second interconnect are provided along a same direction*"

281. Element [31.b] calls for "a longer side of the dummy via in a plan view and a shorter side of the second interconnect are provided along a same direction," which Watanabe and Fujii render obvious.

282. Figures 2 and 9 of Watanabe disclose an elongated wiring 39 (second interconnect), and dummy vias (dummy plugs 34,52). TSMC-1004, Figs. 2, 9.

283. Watanabe's dummy vias not only mitigate stress migration, but also electromigration by providing a source of copper atoms to replace those swept away by the electric current traveling through the interconnect. TSMC-1004, ¶¶[0012]-[0019], [0022]-[0024], [0075], [0077]; *see also* TSMC-1015, 1:25-41, 1:66-2:11. Fujii teaches an improved approach for improving electromigration resistance at a via by having an elongated via (e.g., rectangular) with the longer side in the direction of the wiring width (orthogonal to the main wiring length). TSMC-1030, Abstract, ¶¶[0016], [0064]-[0066].

284. A POSITA would have been motivated to modify Watanabe's dummy vias using Fujii's alternative, known via shape that enhances the overall reliability of the interconnect structure. Specifically, Fujii discloses relative geometries for interconnect lines and vias to mitigate the formation and growth of voids, specifically by using a rectangular via with the longer side intersecting the direction of current in an interconnect to suppress EM. *Id*., ¶¶[0016], [0051]-[0067].

285. A POSITA would have recognized that Fujii's teaching – using rectangular vias to further suppress void creation in vias between interconnects – suggests employing a rectangular shape for Watanabe's dummy plug 34 with the longer side in the same direction as the shorter side of the second interconnect to reduce voids forming in plug 32 (via).

286. A POSITA was motivated to modify Watanabe's dummy vias to take advantage of Fujii's teachings, specifically orienting known rectangular-shaped dummy vias perpendicular to the interconnect length so that they can more effectively replace copper atoms across the entire width of the interconnect in response to electromigration. Just as in Fujii, the larger surface perpendicular to the current flow direction provides a more even distribution of copper atoms across the interconnect, thus mitigating void formation due to electromigration, while simultaneously capturing migrating vacancies across the interconnect width.

287. Implementing Fujii's disclosed rectangular via shape, with its long side paralleling the interconnect width, was a known alternative for Watanabe's dummy vias, one that reduces void formation stemming from stress migration. *Id*., ¶¶[0066]-[0067]; *see also* TSMC-1008, 9:45-47 (noting that standard via shapes include rectangular cross-sections); TSMC-1013, 8:48-52 (same). Moreover, Watanabe itself recognizes that employing dummy plug 34 also addresses electromigration by providing a source of copper atoms to replace those swept away by the electric

current traveling through the interconnect: "since this dummy plug 34 can also act as a source of copper atoms that move in the wiring 39 together with the electrons, the situation where the wiring 39 is disconnected because of the lack of the copper atoms, i.e., the so-called electromigration, can also be prevented." TSMC-1004, ¶[0077]. A POSITA would have found it obvious to further address electromigration by Fujii's suggestion to have a rectangular-shaped via. Moreover, Fujii states that its teachings are readily applied to copper wirings as well, just like what Watanabe discloses. TSMC-1030, ¶[0197].

288. Moreover, given that rectangular vias were one of several commonly-recognized shapes (TSMC-1008, 9:45-47; TSMC-1013, 8:48-52), and in view of Fujii's teachings regarding the importance of rectangular via orientation relative to the interconnection direction, a POSITA would have arrived at claim 31's limitation through simple, routine optimization regarding the dummy via shape and orientation.

289. A POSITA would have had a reasonable expectation of success in making Watanabe's dummy vias 34, 52 rectangular and oriented relative to the second interconnect as taught by Fujii, given Fujii's recognition of their standard nature. Additionally, configuring vias/interconnects with the foregoing shapes/orientations would have merely required patterning of correspondingly shaped and located via holes/interconnect trenches, which would have been easily achieved at the time with the same manufacturing processes disclosed in Watanabe.

H. Ground 7: Claim 48 Is Obvious Over Watanabe, Kamoshima, and Fukazawa

290. Watanabe, Kamoshima, and Fukazawa render claim 48 obvious to a POSITA. I first outline the disclosures of these references relative to claim 45, and then provide motivation to combine the teachings of Watanabe and Kamoshima. I then further discuss the additional teachings provided by Fukazawa in the context of claim 48 and then provide motivation to further combine Fukazawa with the combined teachings of Watanabe and Kamoshima.

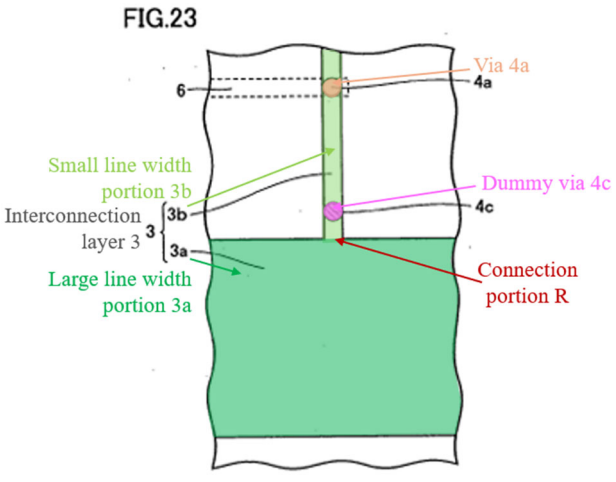
1. Claim 45[5]

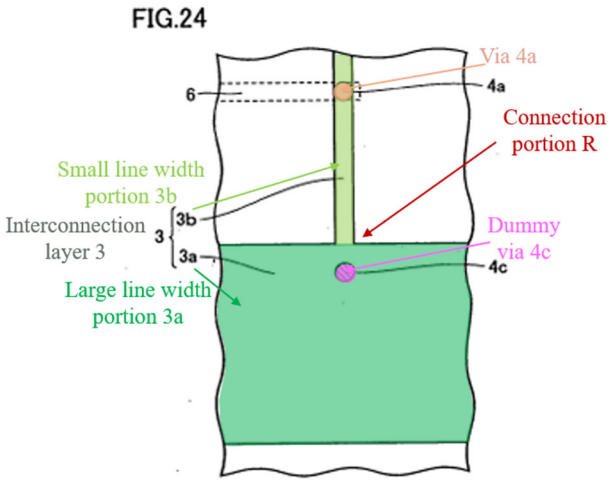
a) [45.a] – "*semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion*"

291. Element [45.a] recites the "semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion," which Watanabe and Kamoshima render obvious.

[5] I analyze claim 45 here because challenged claim 48 depends from claim 45.

292. Kamoshima discloses interconnections having a constant width, such as interconnection layer 3 (Figure 3), Kamoshima also discloses an interconnection with a branched shape including a large line width portion 3a and a small line width portion 3b. TSMC-1009, ¶¶[0002], [0062], [0068]-[0069], [0094]-[0103], Abstract, Figs. 8-9, 23-27. For example, in Figures 23-27, Kamoshima discloses a second interconnect (e.g., "interconnection layer 3) that is comprised of a first interconnect portion (e.g., "large line width portion 3a") and a second interconnect portion (e.g., "small line width portion 3b") whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion. See annotated Figures 23 and 24 below (*see id.*, ¶¶[0094]-[0103], Figs. 23-27):





293. Kamoshima teaches having via 4a in small line width portion 3b and dummy via 4c in the vicinity of the "connection portion R" between the two interconnection portions 3a, 3b (*see id.*, Figs. 23-24). Kamoshima's approach

provides a local, targeted protection for the most vulnerable point—the functional via—by creating a bottleneck with the small line width portion 3b to prevent voids from reaching it.

b) [45.b] – "*the via is connected to the second interconnect portion*"

294. Element [45.b] calls for "the via is connected to the second interconnect portion," which Watanabe and Kamoshima render obvious.

295. Watanabe's vias (plugs 32, 53) are likewise connected to the second interconnect (e.g., wirings 36, 39). TSMC-1004, ¶¶[0067]-[0073], [0118]-[0122], [0159]-[0165], Figs. 1, 3, 8-9, 12J-12K. See annotated Figures 2 and 9 below:

FIG. 2

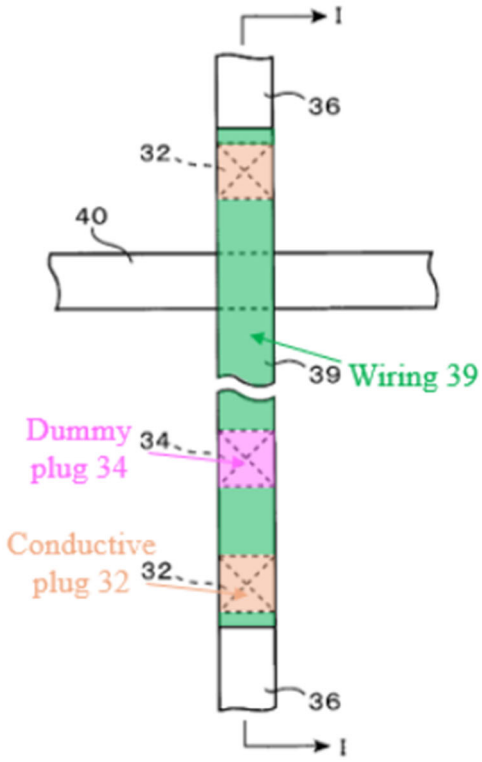
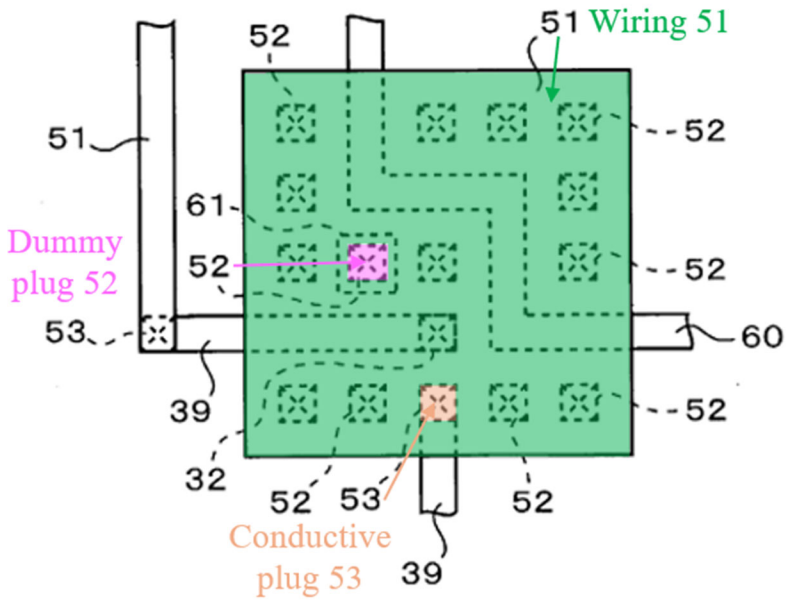
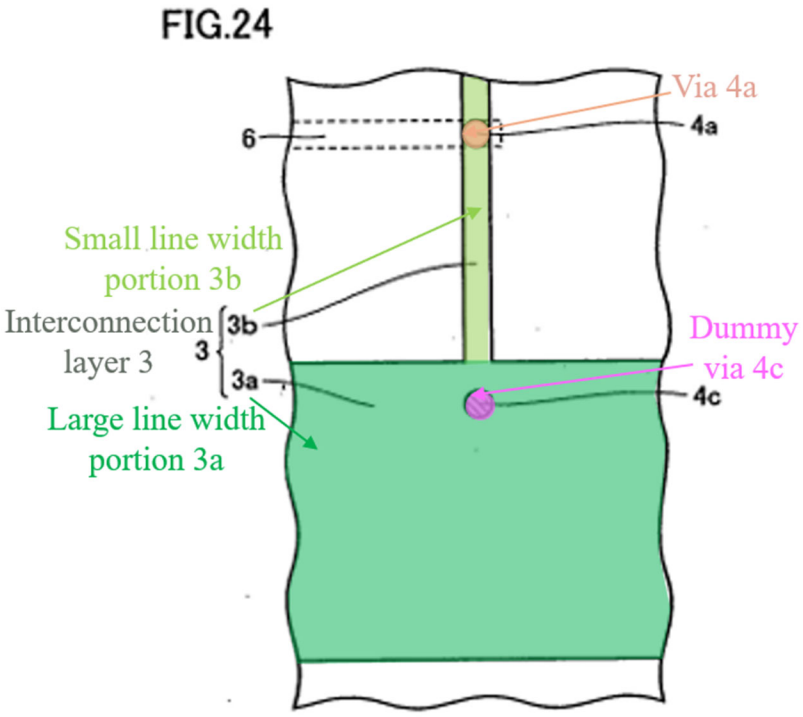

I
36
32
40
39 Wiring 39
Dummy plug 34
34
Conductive plug 32
32
36
I

FIG. 9



296. Kamoshima discloses that the via (e.g., "via 4a") is connected to the second interconnect portion (e.g., "interconnection portion with a small line width 3*b*"). TSMC-1009, ¶¶[0095] ("Interconnection layer 3 includes an interconnection portion with a large line width 3*a*, and an interconnection portion with a small line width 3*b*. Interconnection layer 6 is electrically **connected to interconnection portion with a small line width 3*b* of interconnection layer 3 through via 4*a***."), [0098], Figs. 23-24. See annotated Figure 23:



c) Obviousness of Combining Watanabe and Kamoshima

297. As discussed previously, the first through third and fifth embodiments of Watanabe disclose a second interconnect (e.g., "wiring 39," "wiring 51"). *Supra*, §§X.A.1.a.(5), X.A.1.(b)-(d). As examples, annotated Figure 1 (first embodiment) discloses wiring 39 and Figure 8 (fifth embodiment) discloses wiring 51:

FIG. 1

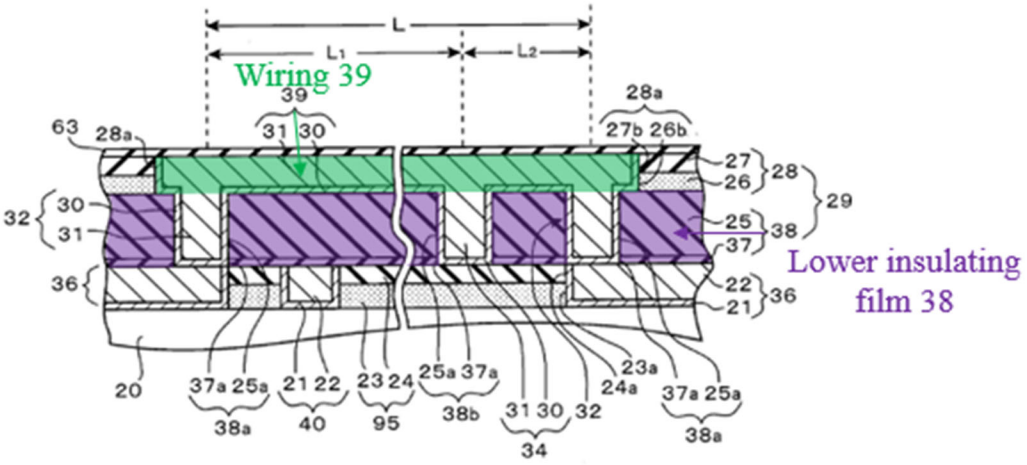
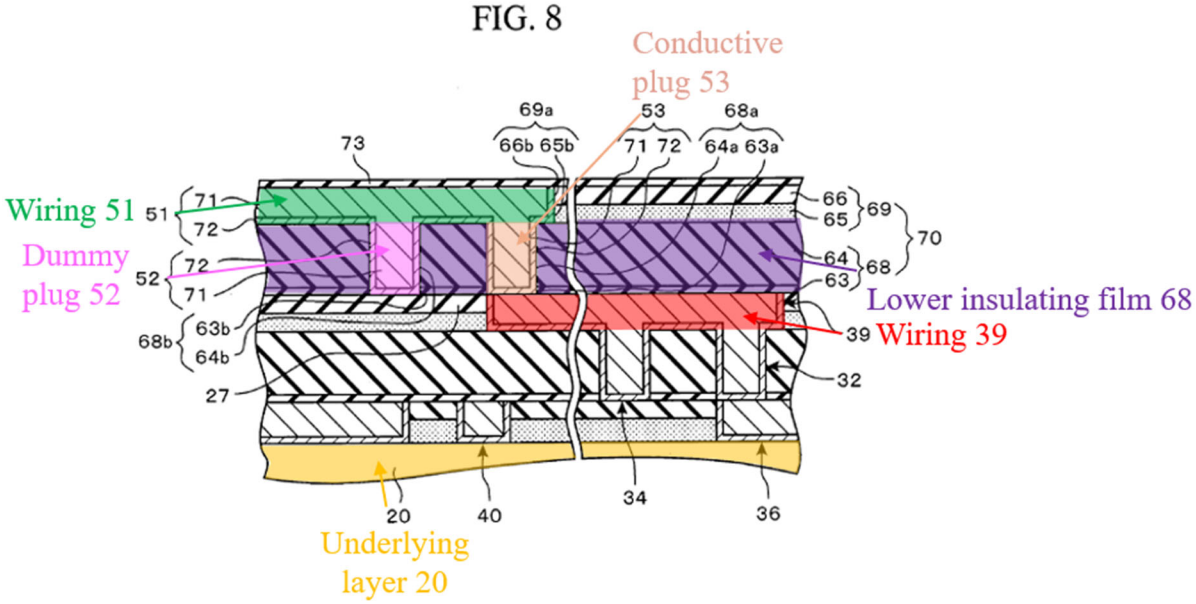


FIG. 8



298. In view of Kamoshima (e.g., Figures 23-24), a POSITA would have understood the claimed branched shape (with a narrower portion extending from a wider portion) was a known design option for the shape of any of Watanabe's wirings that correspond to the claimed "second interconnect" (e.g., "wiring 39," "wiring 51"). Thus, it was obvious to a POSITA for Watanabe's second

interconnects (e.g., wiring 39, wiring 51) (in any of the first-to-third and fifth embodiments) to be similarly shaped so as to create an interconnect having a branched configuration similar to Kamoshima's "interconnection layer 3" of Figures 23-24. Doing so would simply involve changing Watanabe's "wiring trench 28a" (or "wiring trench 69a") in "insulating film 29" (or "insulating film 70") so that the wiring trenches 28a (or 69a) included a similar shape as Kamoshima's interconnection layer 3 from Figures 23-24.

299. Moreover, because Kamoshima's interconnection layer 3 is connected to both a real via (i.e., via 4a) and a dummy via (i.e., via 4c) (see, e.g., TSMC-1009, Figs 22-24), a POSITA would have understood that the shape of Kamoshima's "interconnection layer 3" was an option for Watanabe's upper layer wirings (e.g., "second wiring 39" and "third wiring 51"), which likewise are common interconnects that are connected to both a real via (e.g., "conductive plug 32") and a dummy via (e.g., "dummy plug 34"). TSMC-1004, ¶¶[0070]-[0073], [0117]-[0122], Figs. 1-5C, 8-9. Accordingly, when considering potential shapes for Watanabe's "second wiring 39" and "third wiring 51," a POSITA would have considered the shapes of Kamoshima's "interconnection layer 3" as potential options given their similarity in connections (e.g., to both real and dummy vias).

300. Given that such a shape was a known design option, a POSITA would have been motivated to select that shape wherever the design objectives for the

corresponding device would have found that shape advantageous. For example, Kamoshima motivates a POSITA to use an interconnection layer with large and small width portions, and positioning the via (for connection to another interconnect) along the small line width portion and dummy via in vicinity of the connection portion between these interconnect portions, to cause microvoids that would otherwise distribute between the via and the dummy via to further concentrate under the dummy via before reaching the via. *See* TSMC-1009, ¶¶[0088], [0097]-[0099]. Such an interconnect design thus further suppresses the concentration of voids under the real via positioned on the narrow portion/branch. Kamoshima expressly notes that such an interconnect design offered the foregoing benefit of further suppressing void concentrations in the narrower branch, where the real via could be located. *See See id.*, ¶[0098] ("A large number of microvoids in interconnection layer with a large line width 3*a* tend to ***concentrate in the area under dummy via 4c before reaching the area under via 4a***. **Therefore, concentration of voids in the area under via 4*a* can further be suppressed**."); *see also id.*, ¶¶[0088],[0097]-[0099]. Thus, Kamoshima teaches a known design choice of an interconnect shape that has the added benefit of further suppressing microvoids under functional vias. Kamoshima motivates the design to suppress the concentration of voids due to stress migration. *See id.*, ¶¶[0097]-[0098], [0105], [0109], [0111].

301. Following Kamoshima's teachings, a POSITA would update Watanabe's second interconnect 39, 51 to include a large line width portion and a small line width portion branched therefrom, analogous to Kamoshima's interconnection layer 3 from Figures 23-24. Watanabe's plug 32/53 would be connected to the small line width portion and dummy plug 34/52 would be connected to the large line width portion. This branched interconnect shape would further enhance suppression of the microvoids in Watanabe's design in any of its first-to-third and fifth embodiments. *See also* TSMC-1033, ¶¶[0056]-[0057], [0112]-[0114] ("A sample without the narrow wiring and a sample having the narrow wiring length of 2 μm was checked…. The sample without the narrow wiring showed the defective factor of about 1%. The sample with the narrow wiring of about 2 μm in length showed the defective factor of about 0%."); TSMC-1037, 162-63, 165, Figs. 9, 14. Watanabe already teaches address stress migration, and the POSITA would recognize that incorporating Kamoshima's interconnect shape and corresponding via/dummy via configuration teaching would further enhance the suppression of microvoids.

302. A POSITA would have been motivated to combine the teachings of Watanabe and Kamoshima because the references address the identical problem of stress-induced voiding with complementary solutions that operate on different scales. Watanabe teaches a global approach, using dummy conductive plugs to

reduce overall stress across the interconnect area. Kamoshima's use of a small line width portion (3b) provides a local, targeted protection for the most vulnerable point–the functional via–by creating a bottleneck to prevent voids from reaching it. Kamoshima identifies the issue migration of microvoids from a large area interconnect portion, which acts as a large reservoir for such defects. The solution taught by Kamoshima is to physically isolate the functional via from this large reservoir. Therefore, placing Watanabe's functional via on this narrow portion directly applies Kamoshima's protective teaching, using the geometry to starve the critical area under the via from the main source of failure-causing voids. A POSITA would have found it obvious to apply Kamoshima's geometric protection to Watanabe's structure to create a more robust design that benefits from both the global stress relief of Watanabe and the targeted via protection of Kamoshima. The benefits would be seen as additive; a POSITA would expect Watanabe's dummy plugs to continue to provide global stress relief in the wide interconnect portion, while simultaneously expecting Kamoshima's narrow bottleneck to effectively isolate the functional via from void migration.

303. A POSITA would have found this modification easy to implement and thus would have had a reasonable expectation of success when doing so. Both Watanabe and Kamoshima relate to forming an interconnect connected to both a via (to connect to another interconnect) and dummy via, where the dummy via is present

to suppress voids from concentrating in the via. *See* TSMC-1004, ¶¶[0012]-[0019], [0070]-[0073], [0075], [0117]-[0122], Figs. 1-5C, 8-9; TSMC-1009, ¶¶[0085]-[0086], [0088], [0094]-[0099], Figs. 15-16, 23-27.

304. The foregoing modification to Watanabe would merely involve selecting the location of the via/plug such that it was located in the narrow interconnect portion, and forming the via/plug using the same processes already taught in Watanabe. Indeed, implementing the foregoing interconnect configuration would have merely involved etching the wiring trench in the desired branched shape with appropriate trench portion widths and then filling such trenches with appropriate conductive material (e.g., barrier metal layer and bulk copper layer) to form the interconnect and via holes, which was well within the capabilities of a POSITA at the time of the alleged invention. The modification would be readily achieved with Watanabe's manufacturing process by using appropriate trench portion widths/shapes.

2. Claim 48

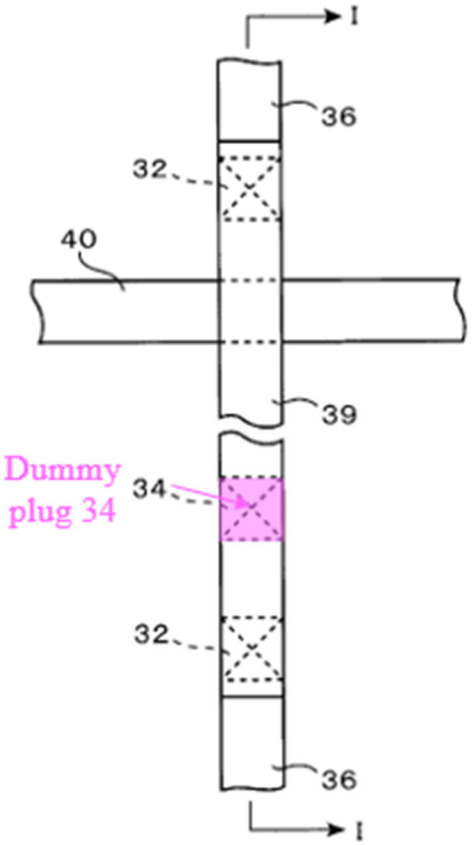
305. Watanabe, Kamoshima, and Fukazawa render claim 48 obvious to a POSITA

a) [48.a] – "*semiconductor device of claim 45, wherein the dummy via is substantially rectangular in a plan view*"

306. Element [48.a] recites that "the dummy via is substantially rectangular in a plan view," which Watanabe, Kamoshima, and Fukazawa render obvious.

307. Watanabe discloses dummy plugs 34/52 that are substantially square (TSMC-1004, Figs. 2, 4, 9), such as illustrated below in annotated Figure 2:

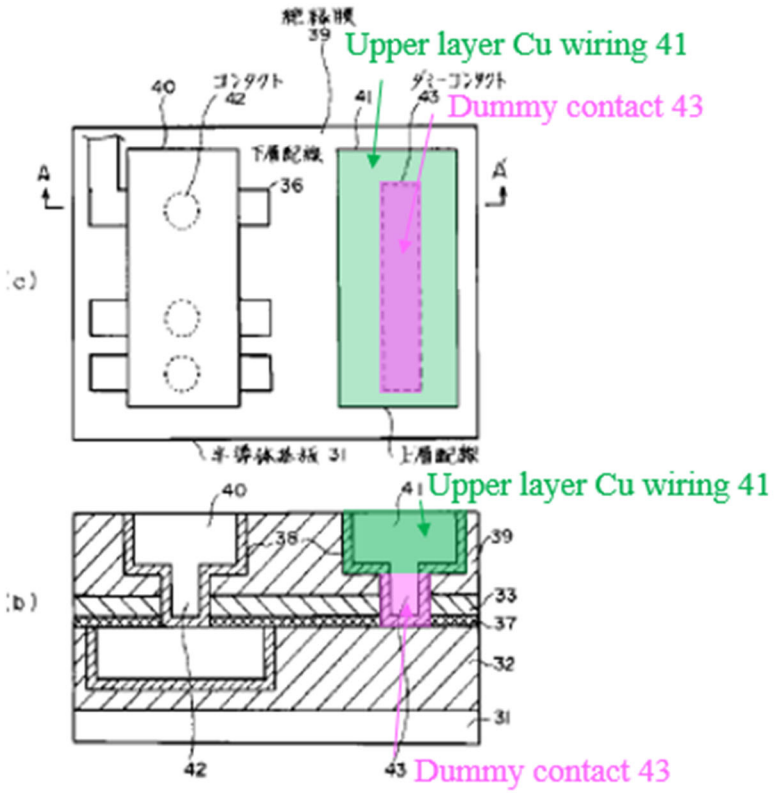
FIG. 2



308. A POSITA would recognize that Fukazawa discloses a dummy via (e.g., "dummy contact 43" and "barrier metal layer 38," hereafter collectively "dummy contact 43") connected to an upper layer interconnect (e.g., "upper layer

Cu wiring 41" and "barrier metal layer 38," hereafter collectively "upper layer Cu wiring 41"). TSMC-1010, ¶[0017], Fig. 7. A POSITA would understand Fukazawa's dummy contact 43 to be a dummy via, both because of its label as a "dummy" structure and because of its configuration within Fukazawa's device. Specifically, dummy contact 43 is connected to an upper layer interconnect (e.g., "upper layer Cu wiring 41") but not connected to a lower layer or second interconnect, and thus would be capable of current flow. TSMC-1010, ¶[0017], Fig. 7. To enhance mechanical strength, Fukazawa's dummy contact 43 is arranged in a substantially rectangular shape (which Fukazawa describes as "column-shaped") in a plan view. *Id*., ¶¶[0017]-[0018] ("the dummy contacts are column-shaped"), Fig. 7. The rectangular shape of Fukazawa's "dummy contact 43" in a plan view is clearly disclosed in annotated Figure 7 below (*see id.*, ¶¶[0017]-[0018], Fig. 7):

FIG. 7



b) [48.b] – "*a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction*"

309. Element [48.b] recites "a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction," which Watanabe, Kamoshima, and Fukazawa render obvious.

310. Indeed, Fukazawa discloses a longer side of the rectangular dummy contact/via 43 is provided along a same direction as a longer side of a correspondingly rectangular interconnect ("upper layer Cu wiring 41"). TSMC-1010, ¶¶[0017]-[0018], Figure 7. This is disclosed in annotated Figure 7 below:

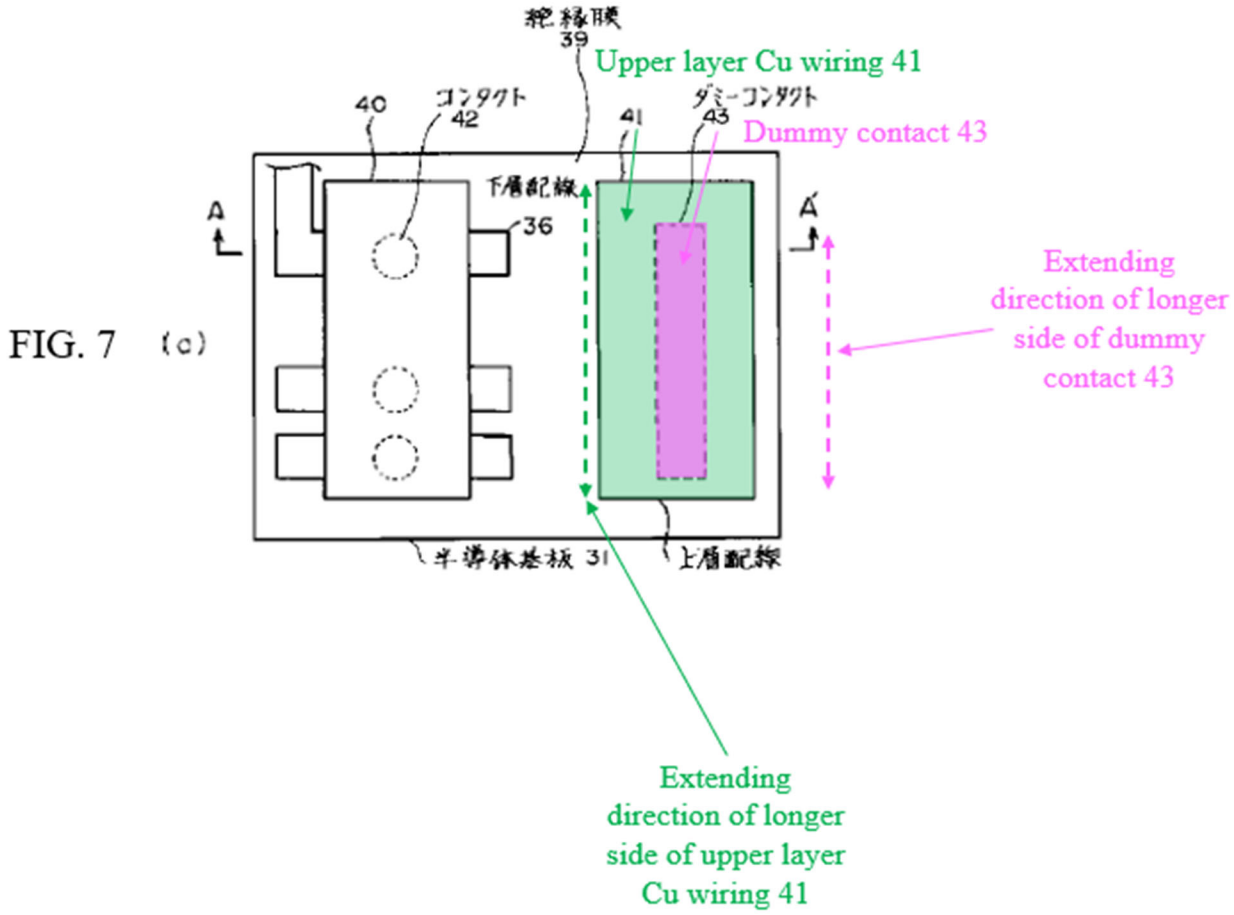


FIG. 7 (c)

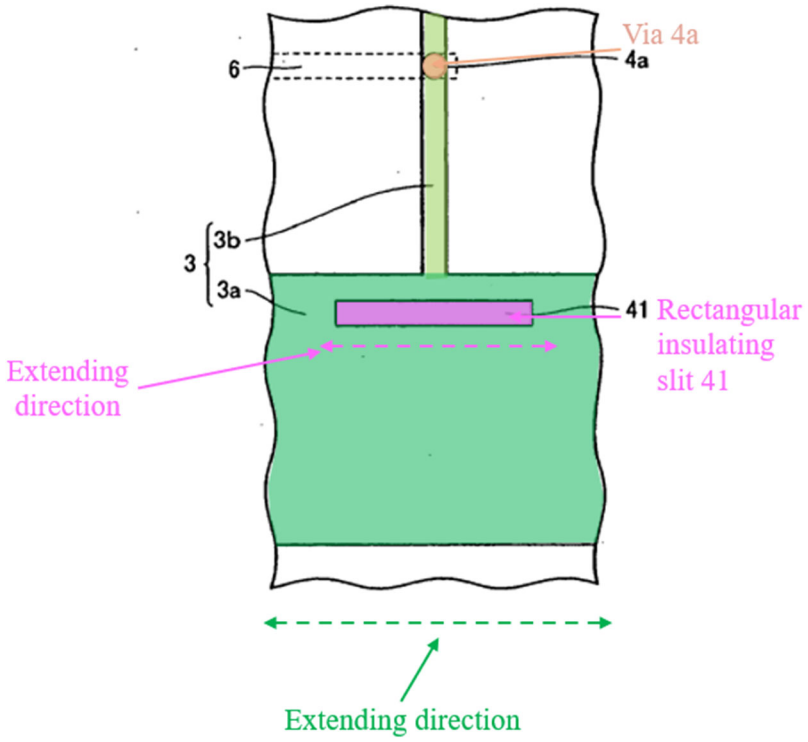
c) Obviousness of Combining Watanabe, Kamoshima, and Fukazawa

311. In view of Fukazawa, it was obvious to a POSITA at the time to use a rectangularly-shaped dummy via (e.g., shaped similarly to Fukazawa's dummy contact 43) in the wider first interconnect portion of Watanabe's second interconnect (after it was modified in view of Kamoshima to have a branched interconnect structure – *see supra*, §X.H.1). Following Fukazawa's teaching of rectangular-shaped dummy vias and Kamoshima's teaching of a branched interconnect structure,

a POSITA would have been motivated to use the rectangularly-shaped dummy via and to position it along a longer side of the wider portion of the branched interconnect to further reduce the migration of vacancies to (and thus the formation of voids within) a real, functional via positioned on the narrow branch of the interconnect. Indeed, as discussed previously *supra*, §IX.A, Watanabe already seeks to address stress-induced vacancy migration and thus a POSITA seeking to improve Watanabe's design would have looked to additional known ways of addressing this issue.

312. Kamoshima teaching using a rectangular structure (e.g., insulating slit 41) positioned in the claimed manner (a longer side extending in a same direction as a longer side of the wider interconnect portion) and for the express reason of suppressing migration of vacancies to via 4a (*see* TSMC-1009, ¶¶[0102]-[0105], Fig. 25):

FIG.25



313. A POSITA understood that positioning a rectangular dummy via in the same position as insulating film 41 would have similarly suppressed vacancy migration (similar to dummy vias 4c in Kamoshima's Figure 23-24 embodiments), with the added benefit of providing a larger area of vacancy interception due to the rectangular shape and its position along a length of the wider portion of the interconnect (and thus perpendicular to the narrow branch portion). Indeed, by virtue of the ends of the rectangular slit expanding well beyond the width of the narrow branching portion, a more tortuous path is created by which vacancies would need to travel to get to functional via 4a, thus reducing the number of vacancies that reach via 4a.

314. Additionally, a POSITA would have been motivated by the increased mechanical strength afforded to the overall wiring structure by the rectangular (i.e., column-shaped) dummy via. Indeed, Fukazawa expressly notes that such a shaped-via increases the mechanical strength of the structure. TSMC-1010, ¶¶[0017]-[0018] ("the dummy contacts are column-shaped like the contacts, but the dummy contacts are not connected to the lower layer wiring or the semiconductor substrate…. [T]he contacts are column-shaped, and the column-shaped bodies are plate-shaped bodies that are connected continuously. Because of this structure, sufficient mechanical strength is ensured even when the insulating film comes off, thereby improving the strength of the wiring structure").

315. A POSITA would have found such a modification, which merely changes the shape and relative locations of via and an interconnect to which it is connected, to have had a reasonable expectation of success. Indeed, as described above, a POSITA was clearly capable of creating a branched interconnect. The additional elements of claim 48 merely require that a dummy via be constructed with a rectangular shape and connected to the wider interconnect portion in the same relative position as insulating slit 41 in Kamoshima's Figure 25 embodiment. This would have been easily and reliably accomplished using standard processing techniques at the time. Indeed, prior to the '623 patent rectangular vias were well-known and used and positioning them where desired was easily achievable. This is

demonstrated by numerous references pre-dating the '623 patent that describe the interchangeable use of various via shapes. *See* TSMC-1008, 9:45-47 ("It will be also understood that the opening of the via-hole may have any configuration, such as a square, rectangle or circle."); TSMC-1013, 9:45-49, 10:1-4 ("[D]ummy via holes of only rectangles or lines may also be formed."); *see also supra*, §X.G.1.(a).

316. Thus, claim 48 was obvious over the combination of Watanabe, Kamoshima, and Fukazawa.

I. Ground 8: Claims 23, 27, 41, and 43-44 Are Anticipated by Hasunuma

317. I believe that Hasunuma anticipates Claims 23, 27, 41, and 43-44 as detailed below. I summarized Hasunuma's teachings previously. *Supra*, §IX.B. Claim 1 is discussed below because each of claims 23, 27, 41, and 43-44 depend from it.

1. Claim 1

a) [1.pre] – "*semiconductor device*"

318. The preamble of claim 1 calls for a "semiconductor device," which Hasunuma discloses.

319. Hasunuma's Figure 8 discloses semiconductor device 31, and thus satisfies claim 1's preamble. TSMC-1005, ¶¶Abstract, [0021], [0111].[6]

b) [1.a] – "*a semiconductor substrate*"

320. Element 1[a] calls for "a semiconductor substrate," which Hasunuma discloses.

321. Hasunuma's Figure 8 discloses silicon substrate 1 (i.e., a "semiconductor substrate") for its semiconductor device 31. TSMC-1005, ¶[0090], Figs. 1-8.

c) [1.b] – "*a first interconnect formed on the semiconductor substrate*"

322. Element 1[b] calls for "a first interconnect formed on the semiconductor substrate," which Hasunuma discloses.

323. Hasunuma discloses a first interconnect (e.g., "Cu conductive layer 14" and "barrier layer 9," hereinafter collectively referred to as "conductive layer 14" or "first interconnect") formed on the semiconductor substrate. TSMC-1005, ¶¶[0094], [0098], Figs. 3A, 8. Hasunuma describes its interconnects using the term

[6] Hasunuma's Figure 14 embodiment meets the challenged claims just like the first embodiment that includes Figure 8. Although my analysis here focuses primarily on Figure 8, the same analysis would apply to Hasunuma's Figure 14.

"conductive layer" (e.g., "conductive layer 14," "conductive layer 26"). A POSITA understood that such conductive layers constitute "interconnects" as those terms are understood in the art because Hasunuma's conductive layers are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:20-27. Conductive layers/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g.*, *id*., 1:36-38. Hasunuma's conductive layer 14, comprising barrier metal film 9 and copper film 12, is formed within an insulating film deposited over substrate 1, as seen in annotated Figure 8 below:

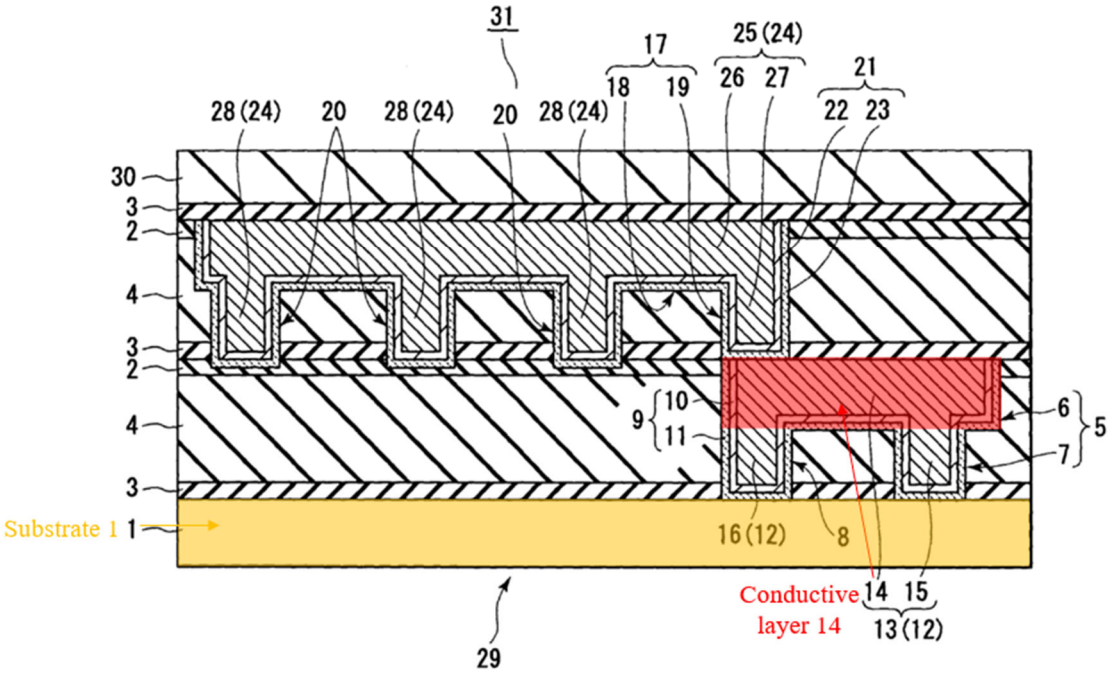


FIG. 8

TSMC-1005, Fig. 3A, 8.

d) [1.c] – "*a first insulating film formed on the first interconnect*"

324. Element 1[c] calls for "a first insulating film formed on the first interconnect," which Hasunuma discloses.

325. Hasunuma discloses a second-level insulating film comprising insulating films 3, 4 (a low dielectric constant film), and 2 stacked on the first interconnect, as shown in annotated Figure 8 below:

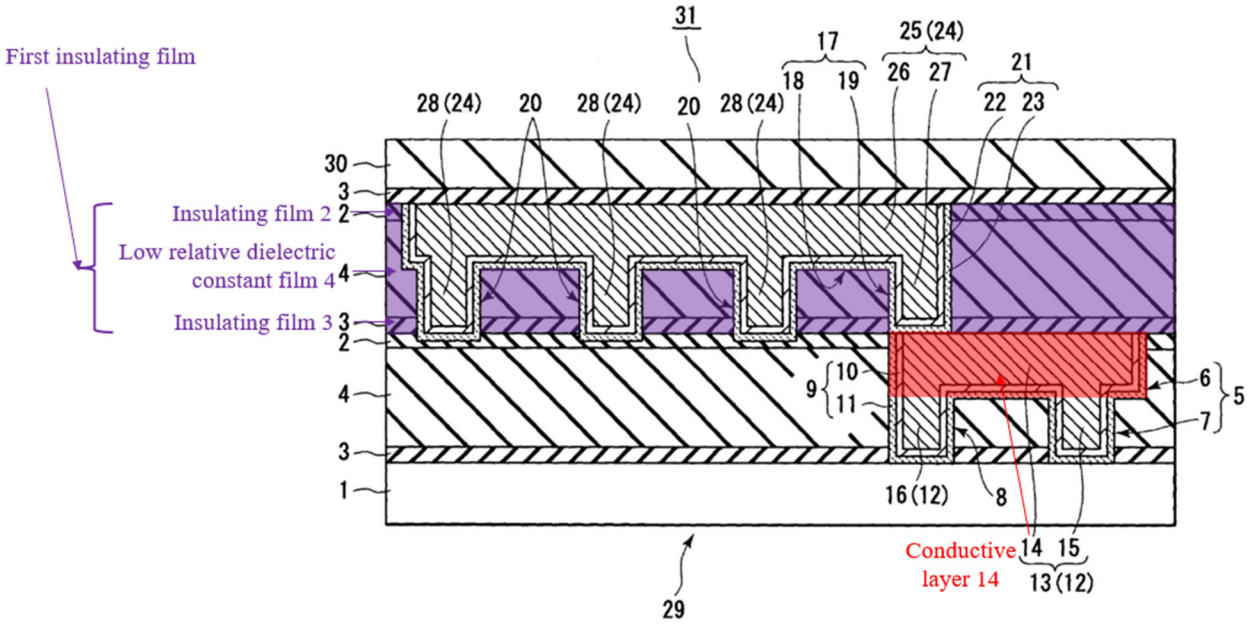


FIG. 8

TSMC-1005, ¶[0100], Figs. 3A-8.

326. As shown in Figure 8 above, Hasunuma discloses depositing an insulating stack over the Cu conductive layer 14, which insulating stack includes an insulating film 3, a low relative dielectric film 4, and an insulating film 2. *Id.*, Figs. 3B, 8, ¶[0100]. Hasunuma explains that "on the SiC film 2 and Cu wiring layer 13 of the first layer, the SiCN film 3, the low relative dielectric constant film 4, and the SiC film (capping layer of a second layer) 2 of the second layer are successively stacked." *Id.*, ¶[0100]. A POSITA would understand each of SiCN film 3, the low relative dielectric constant film 4, and the SiC film (capping layer of a second layer) 2 (as well as any films that may be substituted for these particular films) to be insulating films. Indeed, Hasunuma expressly refers to films 2, 3, and 4 as

"insulating films." *See id.*, ¶¶[0090]-[0091] ("as shown in FIG. 1A, on a silicon substrate (semiconductor substrate) 1 in which an active area and underlayer wiring comprising various electronic circuits (not shown) are formed, an insulating film 3, interlayer insulating film (inter-level dielectrics: ILD) 4, and another insulating film 2 are successively stacked. Concretely, first on the surface of the Si substrate 1, for example, a CVD process is used to deposit the insulating film 3 whose Young's modulus is about 30 GPa or more in a film thickness of about 50 nm. This insulating film 3 functions as a first reinforcing film (reinforcing material), and in the present embodiment, for example, an SiCN film is employed as the insulating film 3. Subsequently, on the surface of this SiCN film 3, the CVD process is used to deposit the interlayer insulating film 4…."). A POSITA would understand that the combination of films 3, 4, and 2, or either or both of films 3 and 4, can constitute the "first insulating film."

e) [1.d] – "*a second interconnect formed on the first insulating film*"

327. Element 1[d] calls for "a second interconnect formed on the first insulating film," which Hasunuma discloses.

328. Hasunuma discloses a second interconnect, formed by filling recess 18 in the "first insulating film" with barrier metal film 21 and copper film 24 (having

"Cu plating seed layer 24a" and "Cu plating film 24b") to form, collectively "conductive layer 26," as seen in annotated Figure 8 below:

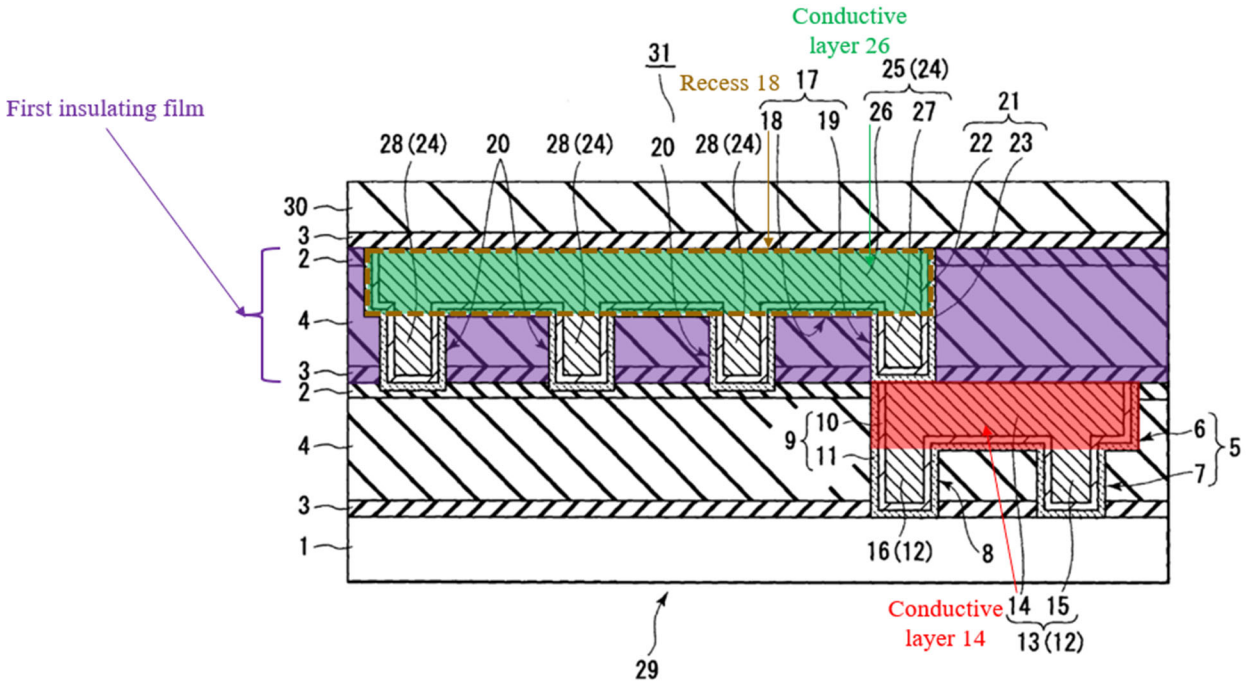


FIG. 8

TSMC-1005, ¶¶[0101], [0105]-[0108], [0110], Figs. 4-8.

329. A POSITA would recognize that the second interconnect is formed on the first insulating film, regardless of whether the first insulating film comprises all of insulating films 3, 4, and 2, or either or both of films 3 and 4. For example, the first insulating film could be considered to be the combination of insulating films 3 and 4 or either film 3 or 4 individually, on each of which the conductive layer 26 is formed.

f) [1.e] – "*a via formed through the first insulating film and connecting between the first and second interconnects*"

330. Element 1[e] calls for "a via formed through the first insulating film and connecting between the first and second interconnects," which Hasunuma discloses.

331. Hasunuma discloses a via, formed by filling recess 19 with barrier metal layer 21 and copper film 24 to form, collectively "conductive plug 27," that extends through the first insulating film from the second interconnect (conductive layer 26) to the first interconnect (conductive layer 14). TSMC-1005, ¶¶[0101]-[0110], Figs. 4-8. This is shown below in annotated Figure 8:

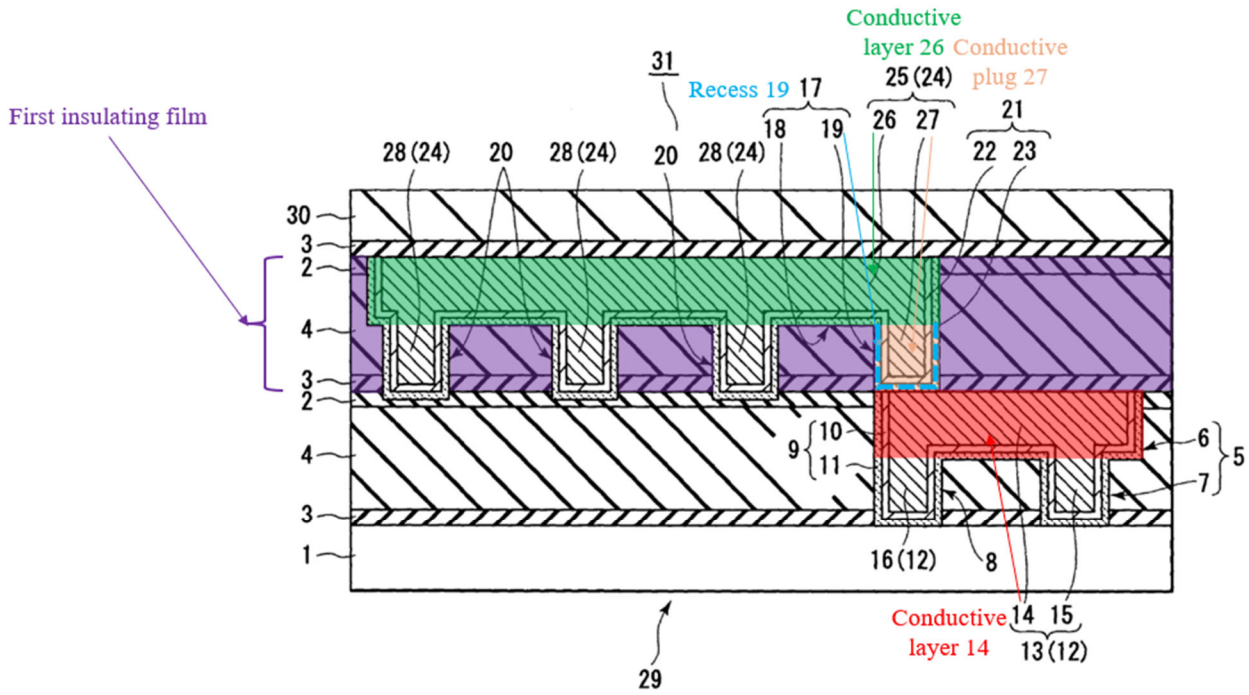


FIG. 8

Id.

332. The conductive plug 27 constitutes the claimed "via." The conductive plug 27 connects the conductive layer 14 (first interconnect) and the conductive layer 26 (second interconnect). *Id*., ¶¶[0101], [0110], Fig. 8. Conductive plug 27 connects the first and second interconnects through the first insulating film, regardless of whether insulating films 3, 4, and 2, or either or both of films 3 and 4, constitute the first insulating film.

g) [1.f] – "*a dummy via connected to the second interconnect*"

333. Element 1[f] calls for "a dummy via connected to the second interconnect," which Hasunuma discloses.

334. For example, Hasunuma discloses dummy vias (e.g., reinforcing plugs 28) connected to the second interconnect (e.g., conductive layer 26). Hasunuma's dummy vias/reinforcing plugs 28, formed by filling recesses 20 with barrier metal film 21 and copper film 24 to form, that extend from the second interconnect (conductive layer 26), as seen in annotated Figure 8:

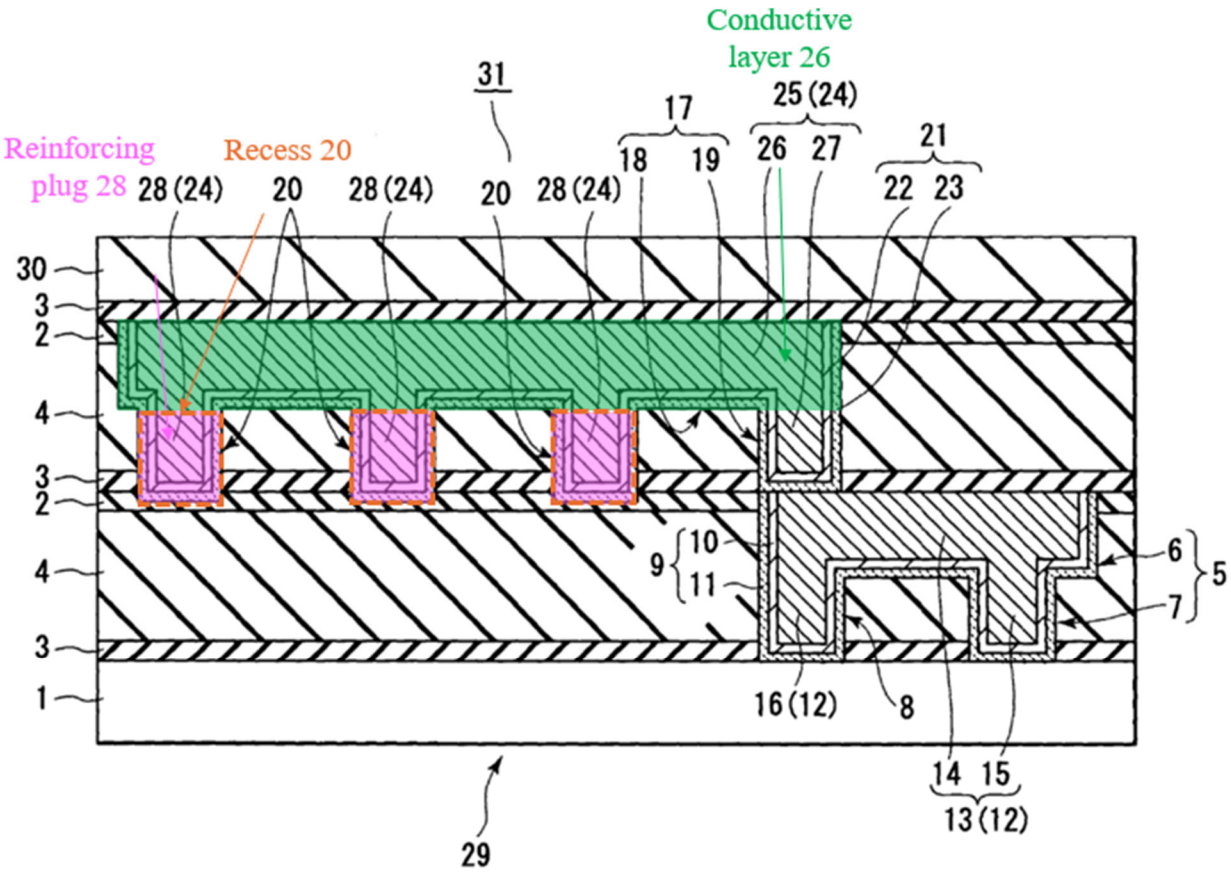


FIG. 8

TSMC-1005, ¶¶[0103]-[0108], Figs. 4-8.

335. Regarding its dummy vias/reinforcing plugs 28, Hasunuma discloses forming multiple recesses 20 integrally with the recess 18, and at the same time as recess 19. *Id.*, ¶[0103]. Thus, using a RIE process, recess 20 is formed extending down through SiCN film 3 to expose the surface of SiC film 2 of the insulating stack. *See id.* Hasunuma notes that, with the RIE process used, the bottom portions of the recesses 20 may extend below the SiC film 2. *Id.*, ¶[0104]. Thus, in this

embodiment, the first reinforcing plugs 28 extend through the SiCN film 3 to contact the SiC film 2 via the barrier metal film 21. *Id.*, ¶[0109].

336. The first reinforcing plugs 28 are connected to the conductive layer 26. *Id.*, Figs 7, 8. Indeed, Hasunuma explains that "the Cu wiring layer 25 of the second layer including the Cu conductive layer 26 and Cu conductive plug (Cu conductive contact plug) 27, and three Cu first reinforcing plugs 28 of the second layer are formed. The Cu wiring layer 25 is a so-called Cu dual damascene wiring." *Id.*, ¶[0108].

337. Each of the first reinforcing plugs 28 constitutes a "dummy via" as explained further in connection with the next limitation [1.g] below.

h) [1.g] – "*wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough*"

338. Element 1[g] calls for "wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough," which Hasunuma discloses.

339. Hasunuma's dummy vias (reinforcing plugs 28) are formed from barrier metal film 21 and copper film 24, which are "conductive films." TSMC-1005, ¶¶[0103]-[0109]. Thus, a POSITA would recognize that the dummy vias/reinforcing plugs 28 are made of a conductive film.

340. Additionally, a POSITA would recognize that the dummy vias/reinforcing plugs 28 are arranged so as to be incapable of having current flow therethrough. For example, the lower end of reinforcing plugs 28 are connected only to insulating films 2 and 3, and Hasunuma explicitly describes reinforcing plug 28 as a non-functional "**dummy** plug (sacrifice plug)" which does not function as the wiring. *Id*., ¶¶[0104], ("[T]here is no problem as long as each the recess 20 has a depth to such an extent that the first reinforcing plug 28 of the second layer formed in the recess 20 **is *not* electrically connected** to the essential wiring layer (not shown) provided below the plug."), [0109], Fig. 8; *see also id*. Fig. 14 (locating reinforcing plugs 28 in between and not in contact with conductive layers 14). Hasunuma further describes the Cu first reinforcing plug 28 as a non-functional "dummy plug (sacrifice plug) which does not substantially function as the wiring." *Id.*, ¶[0109]. Hasunuma also states that "the Cu first reinforcing plug 28 of the second layer may also be referred to as the Cu reinforcing via plug or Cu sacrifice via plug." *Id*.

341. A POSITA would thus understand that reinforcing plugs 28 do not conduct current as part of active device operation, and that they could be omitted from the structure without any impact on the device's circuit diagram. Indeed, because they serve no purpose with respect to the current flow associated with any operational circuits of the device, the omission of reinforcing plugs 28 would not

impact circuit operation. Thus, the first reinforcing plugs 28 are "incapable of having current flow therethrough" as claimed.

342. As previously outlined, the '623 patent specification states:

> A dummy via and a dummy interconnect herein means a pseudo via or a pseudo interconnect which do not *constitute a closed circuit in actual use of a device* with an interconnection structure including these via and interconnect (i.e., **no current flows therein** during actual use of the device.)

TSMC-1001, 3:14-18 (emphasis added).

343. The '623 patent goes on to explain that:

> [N]either the dummy interconnect 102B nor the dummy via 110B constitutes a closed circuit in actual use. That is, *even if the dummy interconnect 102B and the dummy via 110B are omitted* in the interconnection structure shown in FIG. 2B, *a device with this interconnection structure is operable at least immediately after fabrication*.

Id., 10:26-32 (emphasis added).

344. As understood by the POSITA, Hasunuma's "first reinforcing plugs 28" do not constitute part of a closed circuit in actual use of the device, i.e., no current flows through the first reinforcing plugs 28 during actual use of the device. As seen in Figures 7-8, these "first reinforcing plugs 28" are only connected at their

upper end to an active element (i.e., "conductive layer 26"), while the other end is not connected to another active circuit element. TSMC-1005, Figs. 7-8. A POSITA would recognize that no current flows through the first reinforcing plugs 28 due to this lack of connection to a second active circuit element.

345. Also, Hasunuma's device would still be operable if first reinforcing plugs 28 were omitted because they do not carry current/signals as part of a closed circuit during actual use of the device. On the other hand, current flows occur between the conductive layer 14 and conductive layer 26 through conductive plug 27, which do constitute a closed circuit for operation of the device. A POSITA would readily understand the similarity between this configuration and that of interconnect 111 and via 110A (and corresponding recess in which via 110A is formed) in the '623 patent. See TSMC-1001, 10:10-48, Figs. 2A-2B.

i) [1.h]/[1.i] – "*the second interconnect and the via form a dual damascene structure*"/"*the second interconnect and the dummy via from a dual damascene structure*"

346. Element [1.h] calls for "the second interconnect and the via form a dual damascene structure" and element [1.i] calls for "the second interconnect and the dummy via from a dual damascene structure," both of which Hasunuma discloses.

347. Hasunuma states that wiring layer 25 (which comprises the second interconnect (conductive layer 26) and via (conductive plug 27)) is "formed in the

dual damascene structure." TSMC-1005, ¶¶[0101], [0108], Fig. 8. Hasunuma similarly states that its second interconnect (conductive layer 26) and dummy vias (reinforcing plugs 28) are "formed in the dual damascene structure." *Id*., ¶[0103].

348. This is consistent with Hasunuma forming the second interconnect, via, and dummy vias integrally when recesses 18-20 are simultaneously filled with barrier metal film 21 and copper film 24. *Id*., ¶¶[0101], [0103], [0105]-[0109], Figs. 4-8. Thus, Hasunuma's second interconnect (conductive layer 26) and via (conductive plug 27) forms a dual damascene structure. Additionally, Hasunuma's second interconnect (conductive layer 26) and the dummy vias (reinforcing plugs 28). This is shown in annotated Figure 8 below:

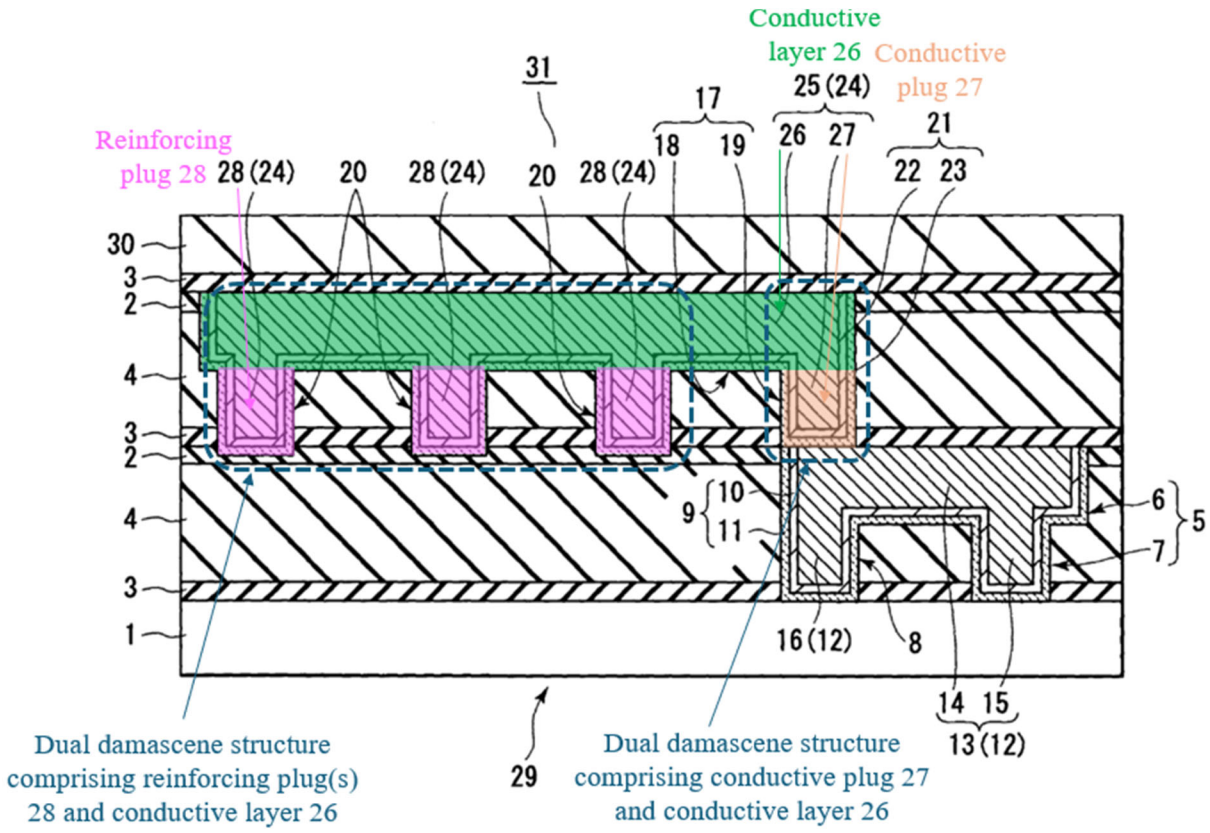


FIG. 8

That Hasunuma's second interconnect (conductive layer 26) and via (conductive plug 27) form a dual damascene structure, as does Hasunuma's second interconnect and its dummy vias (reinforcing plugs 28), is further evidenced by Figure 8 itself. Specifically, a POSITA would appreciate that Hasunuma's barrier metal film 21 conformally coats the outer sides of the conductive film 26, the plug 27 and the reinforcing plugs 28, all as one single, continuous layer. Within this conformal barrier layer coating, copper film 24 is added to fill the recesses for the vias and dummy vias and trench for the interconnect to form the vias, dummy vias, and interconnect from a single, unitary copper structure. A POSITA would have

recognized this configuration shown in Figure 8 as a dual-damascene structure, especially in conjunction with Hasunuma's description (*e.g., id*., ¶¶[0105]-[0108], Figs. 4-7.

2. Claim 23

a) [23.a] – "*semiconductor device of claim 1, wherein the via is substantially circular in a plan view*"

349. Element 23[a] recites the "semiconductor device of claim 1, wherein the via is substantially circular in a plan view," which Hasunuma discloses.

350. Hasunuma discloses circular vias (in plan view) in various figures, including Figure 19A as annotated below (*see, e.g.,* TSMC-1005, Figs. 19A, 22A-22C, 24A-27C, ¶[0200]):

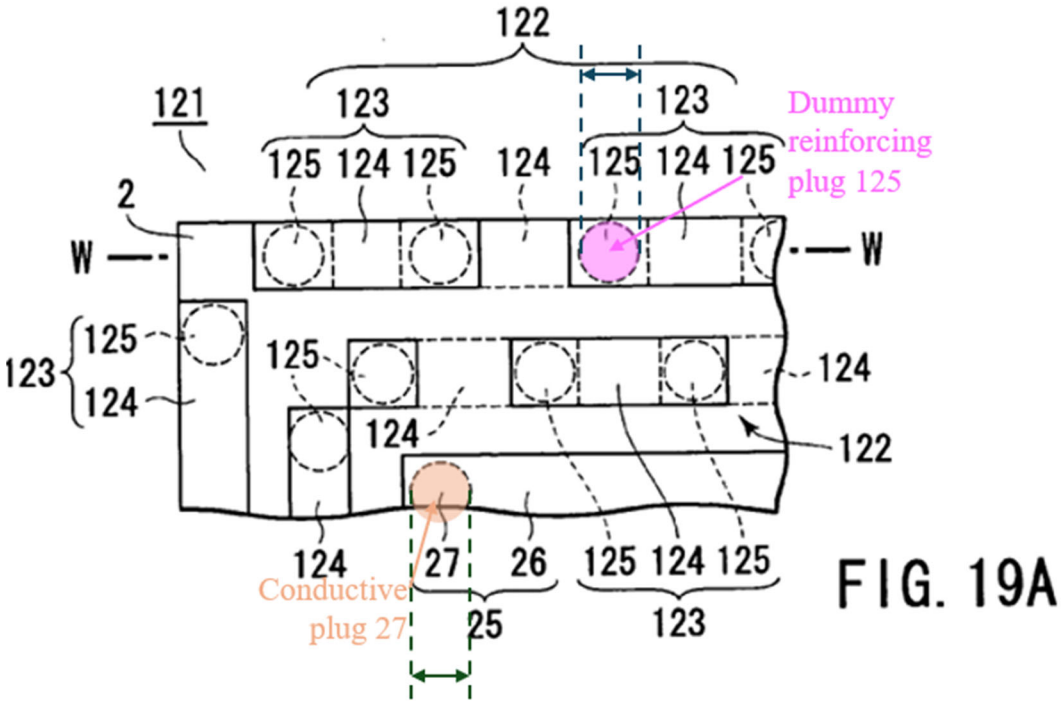


FIG. 19A

351. Additionally, when describing tests performed on such structures, Hasunuma discusses the "diameter" of both conductive and reinforcing plugs, further demonstrating Hasunuma's disclosure of a circular shape for both its vias and dummy vias. *See id.*, ¶¶[0127] ("each diameter of the Cu conductive contact plug 15, Cu reinforcing contact plug 16, Cu conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 μm."), [0133], [0201], [0216], [0010]. A POSITA would have understood that describing the vias' "diameter" in this context discloses a circular shape for both conductive plug 27 and reinforcing plug 28 (i.e., via and dummy via), since "diameter" is the standard dimensional term for circular features.

352. The express disclosure of circular vias in, *inter alia*, Figure 19A, reinforces that Hasunuma's reference to the "diameters" of its vias and dummy vias discloses that these structures likewise have a substantially circular cross section in plan view, just as shown in Figure 19A. In view of the foregoing, a POSITA would have readily understood Hasunuma to disclose substantially circular-shaped vias as an option for any of its vias or dummy vias.

b) [23.b] – "*a diameter of the via is substantially equal to a width of the first interconnect*"

353. Element 23[b] calls for "a diameter of the via is substantially equal to a width of the first interconnect," which Hasunuma discloses.

354. Hasunuma discloses that a diameter of the conductive plug 27 (via) can be "about 0.13 μm" and discloses that "a wiring width of a wiring pattern of each of the Cu wiring layers 13 [which includes conductive layer 14], 25 was set to about 0.13 μm." TSMC-1005, ¶[0127]. In other words, both the conductive plug 27 (via) and the width of the conductive layer 14 (first interconnect) are "about 0.13 μm." The via diameter and first interconnect width (as part of wiring 13) are therefore substantially equal.

3. Claim 27 – "*semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width*"

355. Claim 27 recites the "semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width," which Hasunuma discloses.

356. As discussed throughout my declaration, Hasunuma's functional conductive plug (e.g., via plug 27 in Figs. 8, 9) corresponds to the "via," and Hasunuma's adjacent first reinforcing plug (e.g., reinforcing via plug 28 in Figs. 8, 9) corresponds to the "dummy via." TSMC-1005, Figs. 8, 9. Hasunuma explicitly discloses an example where each diameter of the Cu conductive via plug 27 and Cu reinforcing via plug 28 was formed to be 0.13 μm. *Id*., ¶[0127]. In the same context, Hasunuma teaches a wiring width for wiring layer 13 (which includes the first

interconnect (conductive layer 14)) and wiring layer 25 (which includes the second interconnect (conductive layer 26)) of about 0.13 μm, establishing this as "a minimum interconnect width." *Id*.

357. Hasunuma's Figure 9 illustrates an "interval B" for the conductive via plug 27 and the adjacent reinforcing (dummy) via plug 28. For example, Hasunuma's Figure 9[7] and Tables 1-3 provide values for a "plug interval" between conductive plug 27 and an adjacent reinforcing plug 28 (*id*., ¶¶[0127], [0130]-[0137]), labeled as "B" in Figure 9):

[7] A POSITA would recognize that Hasunuma's Figure 9 discloses the same device as in Hasunuma's first embodiment and Figure 8, but adds illustrations of various heat stresses within the device. TSMC-1005, ¶¶[0022], [0112].

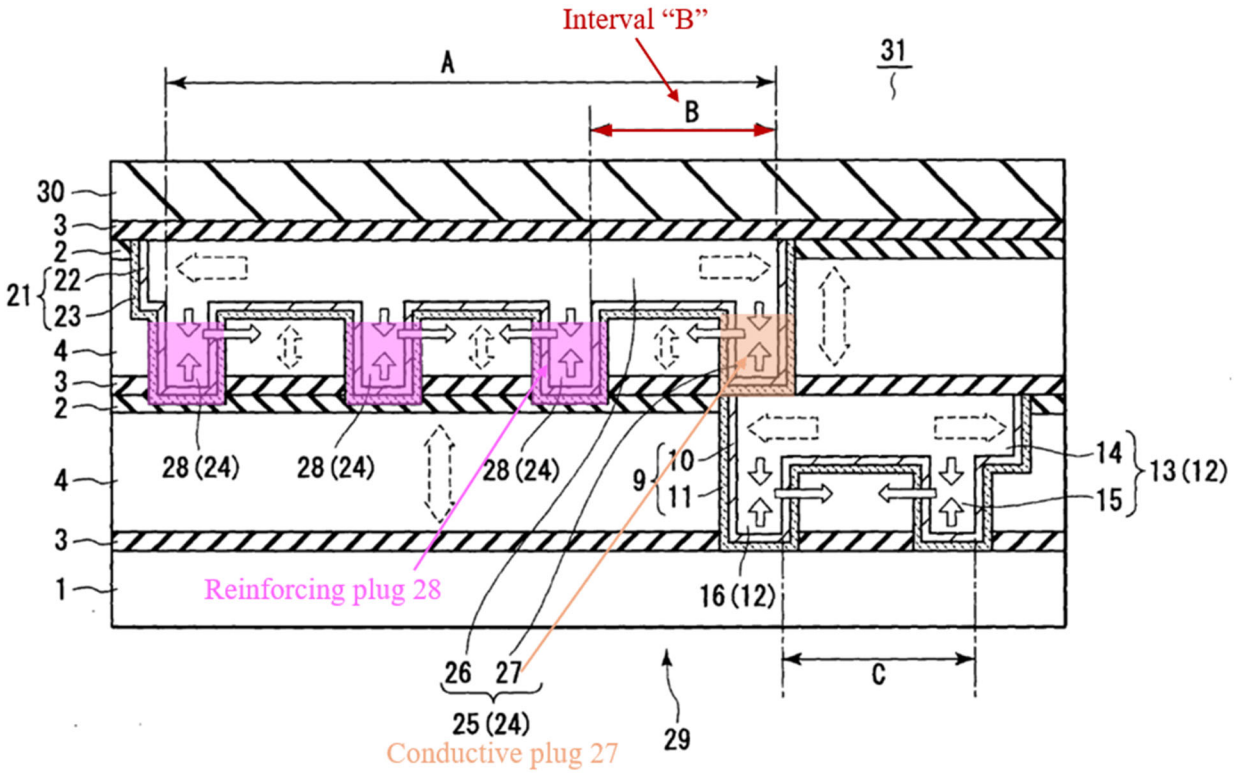


FIG. 9

358. As seen from Figure 9, interval "B" is portrayed as the right edge-to-right edge spacing, which is effectively equal to the center-to-center spacing between the via and dummy via. As clearly seen from Figure 9, this right edge-to-right edge or center-to-center spacing is larger than the adjacent edge-to-adjacent edge spacing between the via and dummy via (e.g., the spacing between the right edge of reinforcing plug 28 and the adjacent left edge of conductive plug 27).

359. Hasunuma discloses a preferred interval B of less than 1 μm or of less than 5 μm or less, and tested intervals up to 20 μm, each of which is less than 25 μm for the larger right edge-to-right edge or center-to-center spacing. *Id.*, ¶¶[0137] ("Cu

conductive plugs 15, 27 and Cu reinforcing plugs 16, 28 are preferably provided so that the plug interval B, C is about 1 μm or less"), [0159] ("it has been found that the plug interval B provided in the Cu wiring layer 25 is preferably about 5 μm or less"), Tables 1-3 (disclosing plug intervals of 0.26 μm, 0.39 μm, etc.). As noted above, the spacing distance between the right side of the reinforcing plug 28 annotated above in Figure 9 and the left side of the adjacent conductive plug 27 is less than the plug interval B between those same plugs.

360. Table 1, associated with the experiments for Fig. 9, lists tested "Plug interval (μm)" values, including 0.26 μm. *Id*., Table 1, Fig. 9. The plug interval B is shown in Fig. 9 to include not only the distance between Cu conductive via plug 27 and Cu reinforcing via plug 28, but also the width of Cu conductive via plug 27. Given a plug diameter of 0.13 μm as stated in ¶[0127], the plug interval B of 0.26 μm results in a closest edge-to-closest edge distance between Cu conductive via plug 27 and Cu reinforcing via plug 28 of 0.13 μm. *Id*., ¶[0127], Table 1, Fig. 9. The closest edge-to-closest edge spacing between the via and dummy via can be calculated as interval B (0.26 μm) minus the via diameter (= 0.13 μm (*id*., ¶[0127])), which results in a closest edge-to-closest edge spacing of 0.13 μm. This closest edge-to-closest edge spacing distance of 0.13 μm between the Cu conductive via plug 27 and Cu reinforcing via plug 28 is equal to Hasunuma's disclosed minimum interconnect width of 0.13 μm. *Id*.

4. Claim 41 – "*semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film*"

361. Claim 41 recites the "semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film," which Hasunuma discloses.

362. Hasunuma discloses dummy vias (e.g., "reinforcing plugs 28") with a first end and a second end, the first end connected to the second interconnect (e.g., "conductive layer 26") and the second end surrounded by a second insulating film (e.g., lower layer insulating film 2 or lower layer "low relative dielectric constant film 4"). TSMC-1005, ¶¶[0103]-[0104], [0109], [0177]-[0178], Figs. 4, 8, 14.

363. Hasunuma's dummy via (reinforcing plug 28) is a vertical structure with a first (top) end and a second (bottom) end. *Id*., Fig. 8. The dummy via's top end is connected to the second interconnect (conductive layer 26), resulting from the dual damascene process where the dummy via is formed integrally with the second interconnect. *Id*., ¶[0108], Figs. 4-7.

364. The second end of Hasunuma's dummy via (e.g., "reinforcing plug 28") is surrounded by a second insulating film (e.g., "low relative dielectric constant film

4" and/or lower layer insulating film 2, alone or as part of the combination of the lower layer insulating films 2, 3, 4). *Id*., ¶¶[0103]-[0104]. During manufacture, recess 20 extends through insulating film 3 (of the second-level insulating layer) and terminates in the underlying, lower insulating film 2 (of the first insulating layer). *Id*., ¶[0104], Figs. 4-7. Dummy via is then created in recess 20, such that the dummy via's bottom end is surrounded by a second insulating film, as seen in Figures 8 and 14 below.

365. Hasunuma explains that:

> each recess 20 is formed extending through the SiCN film 3 of the second layer so as to expose the surface of the SiC film 2 of the first layer. It is to be noted that in the actual RIE process, as shown in FIG. 4, there is a possibility of occurrence of a so-called overetching phenomenon in which the bottom portions of the recesses 20 extend below the surface of the SiC film 2 of the first layer. Even when this overetching phenomenon occurs, there is no problem as long as each the recess 20 has a depth to such an extent that the first reinforcing plug 28 of the second layer formed in the recess 20 is not electrically connected to the essential wiring layer (not shown) provided below the plug.

Id., ¶¶[0103]-[0104]; *see also id*, [0109], [0177]-[0178] ("each Cu reinforcing via plug 28 is extended downwards, and formed completely extending through the SiCN film 3 of the second layer and the SiC film 2 of the first layer. Moreover, the lower

end of each Cu reinforcing via plug 28 projects into the low relative dielectric constant film (interlayer insulating film) 4 of the first layer."), Figs. 4, 8, 14. See annotated Figures 8 and 14 below:

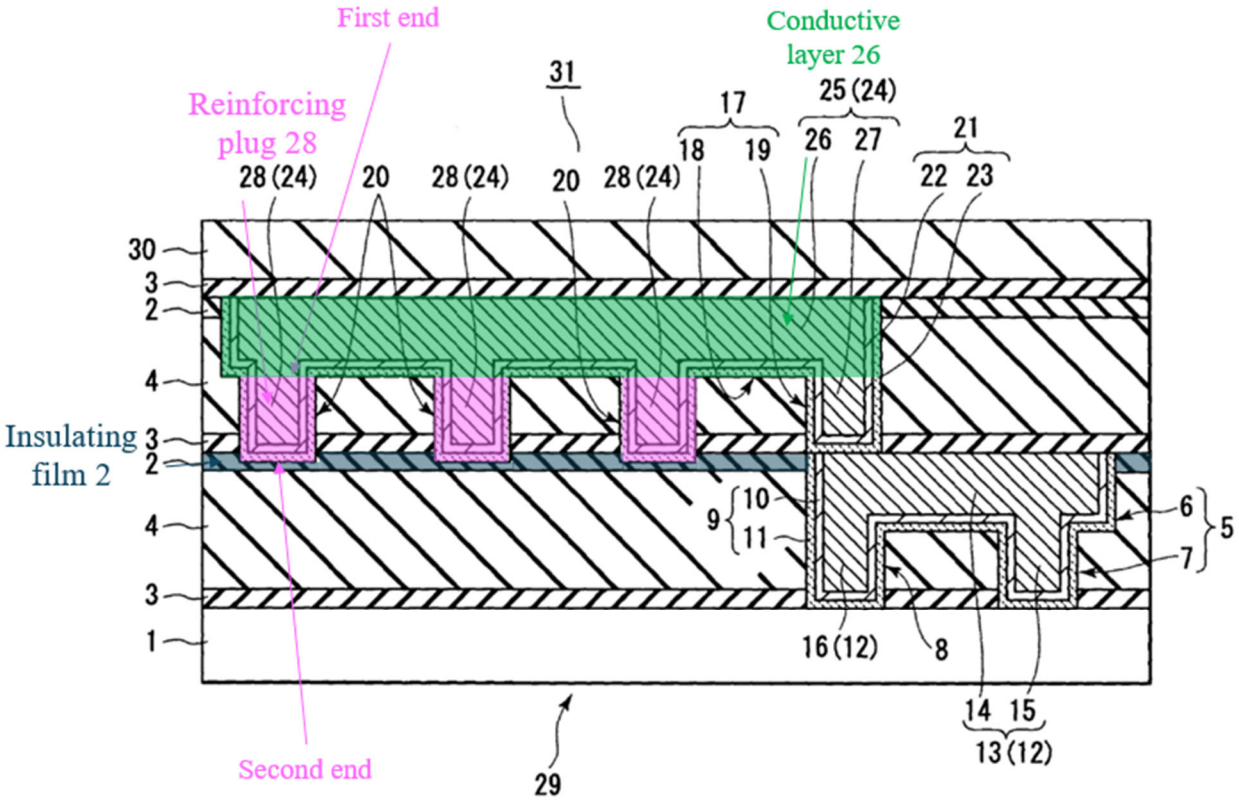


FIG. 8

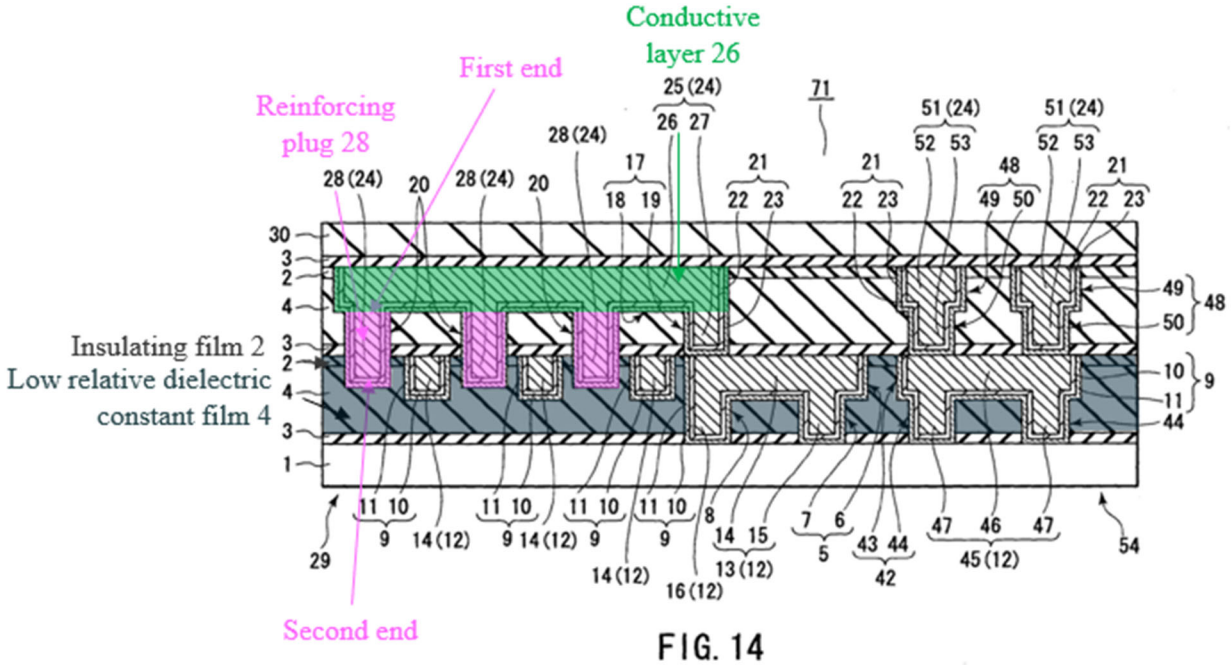


FIG. 14

366. As disclosed in Figure 8 above, the second (bottom) end of dummy/reinforcing plug 28 extends into and is surrounded by insulating film 2.

367. As disclosed in Figure 14 above, the second (bottom) end of dummy/reinforcing plug 28 is surrounded by insulating films 2 and/or 4, thus satisfying claim 41. A POSITA would further understand that the concept of extending plugs 28 into underlying layer 4 as shown in Figure 14 is equally applicable to Figure 8's device given the like numbering of the plugs and insulating layers and its similar overall structure. Moreover, as discussed above, Figure 14 includes the same relevant components that I mapped in the claim 1 discussion above to the limitations of claim 1 of the '623 patent. Thus, Figure 14 satisfies claim 1 for the same reasons as discussed above for the embodiment of Figures 1-8.

5. Claim 43 – "*semiconductor device of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via*"

368. Claim 43 recites the "semiconductor device of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via," which Hasunuma discloses.

369. Hasunuma teaches that a bottom of its dummy vias (reinforcing plugs 28) is located deeper than a bottom the real, functional via (conductive plug 27). TSMC-1005, ¶¶[0104] ("Even when this overetching phenomenon occurs, there is no problem as long as each the recess 20 has a depth to such an extent that the first reinforcing plug 28 of the second layer formed in the recess 20 is not electrically connected to the essential wiring layer (not shown) provided below the plug"), [0109] ("The three Cu first reinforcing plugs 28 are formed substantially extending through the SiCN film 3 of the second layer to indirectly contact the SiC film 2 of the first layer via the barrier metal film 21. That is, each Cu first reinforcing plug 28 is formed to be substantially connected to the SiCN film 3 of the second layer having a Young's modulus of about 30 GPa or more and the SiC film 2 of the first layer via the barrier metal film 21 in the lower end (bottom portion)."), [0176]-[0178], Figs. 8, 14. As the annotations below show, Figure 8 discloses "reinforcing plugs 28" extending into underlying insulating film 2, while "conductive plug 27" extends only to the upper surface of "conductive layer 14" (*id*., Fig. 8, ¶¶[0109], [0104]):

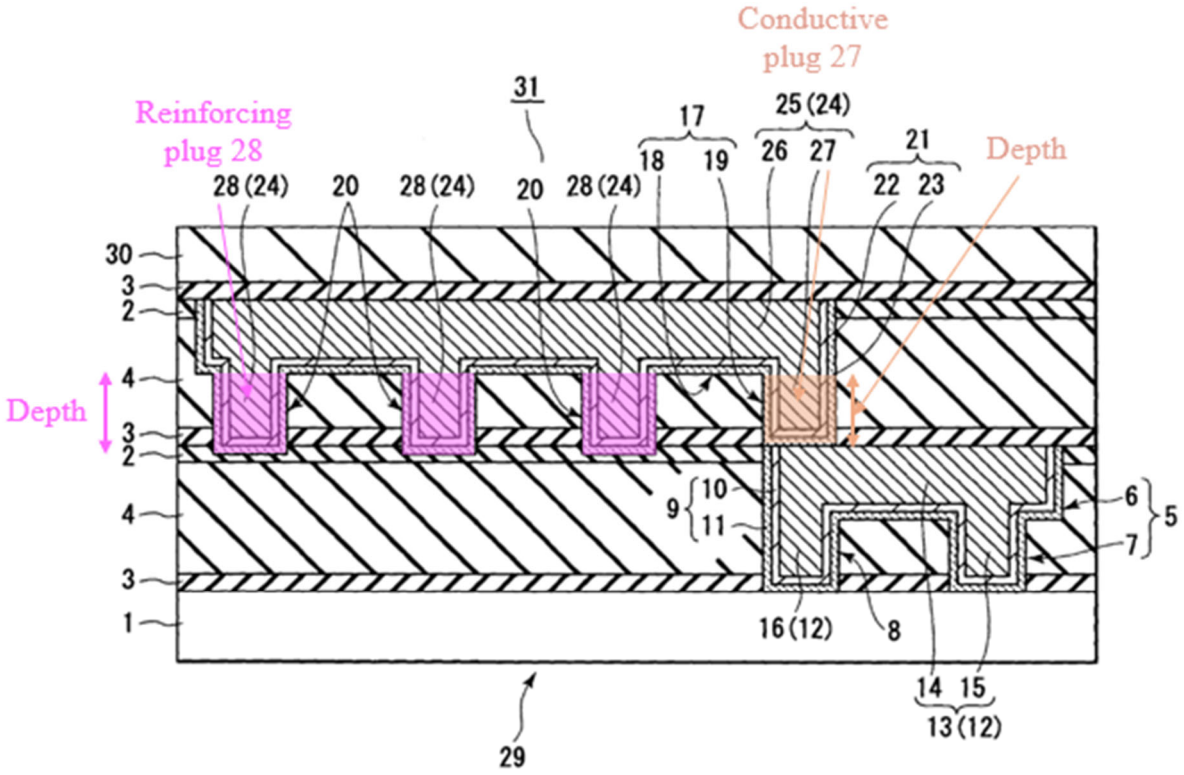


FIG. 8

Thus, a bottom of "reinforcing plug 28" extends deeper than a bottom of "conductive plug 27."

370. In addition, Figure 14[8] is directed to a further embodiment that includes the same components as the embodiment of Hasunuma's Figures 1-8 relied on for

[8] Figure 14 is directed to a "fourth embodiment," but includes the same components as the first embodiment of Hasunuma's Figures 1-8 relied on for claim 1. TSMC-1005, ¶[0176]. Accordingly, my analysis above of the Figure 8 embodiment for claim 1 (including its mapping to the elements of claim 1) applies

claim 1. *Id.*, ¶[0176]. As disclosed in annotated Figure 14 below, "reinforcing plugs 28" extend into underlying "low dielectric constant film (interlayer insulating film) 4" while "conductive plug 27" extends to the upper surface of "conductive layer 14":

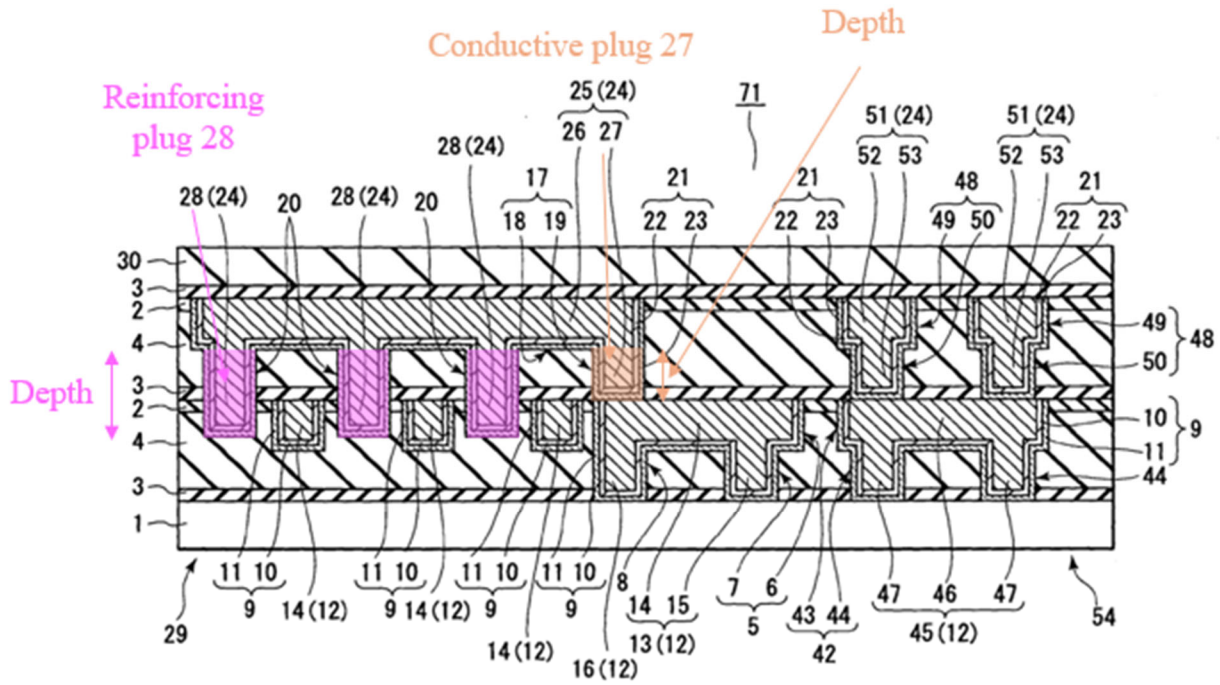


FIG. 14

Thus, once again, a bottom of "reinforcing plug 28" extends deeper than a bottom of "conductive plug 27."

371. Thus, Hasunuma satisfies claim 43 based on each of the Figure 8 and Figure 14 embodiments.

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equally to Figure 14, which discloses the elements of claim 1 for the same reasons as Figure 8 discussed above.

6. Claim 44

a) [44.a] – "*semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate*"

372. Element [44.a] recites the "semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate," which Hasunuma discloses.

373. Hasunuma discloses a "second insulating film" (e.g., insulating films 3, 4, and 2) on substrate 1. TSMC-1005, ¶¶[0090]-[0091], Figs. 1A, 8, 14. The second insulating film is disclosed in Figures 8 and 14 as demonstrated by the annotations below:

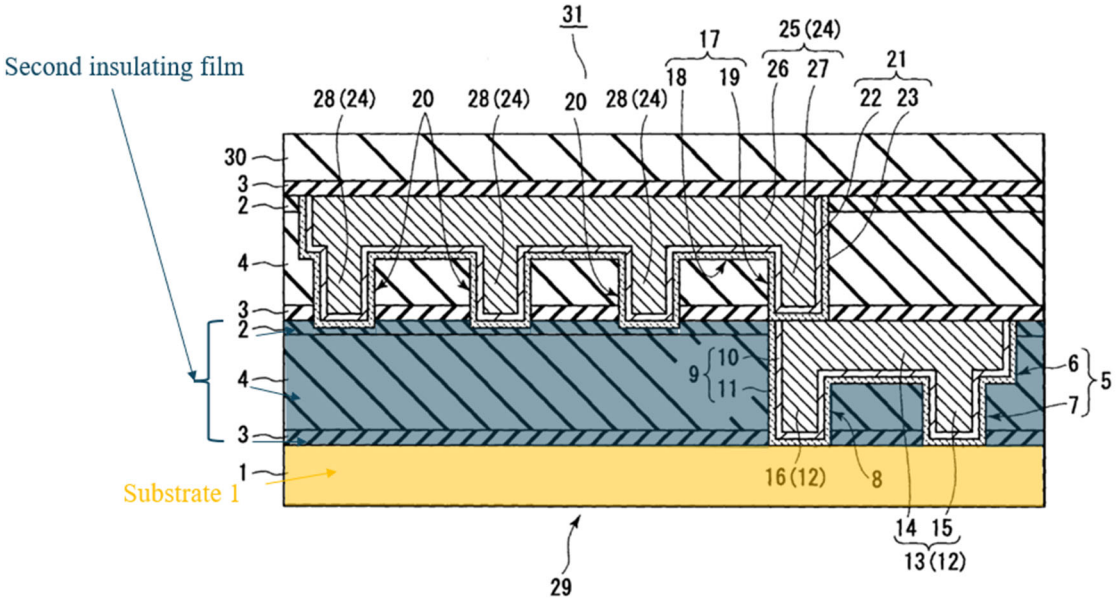


FIG. 8

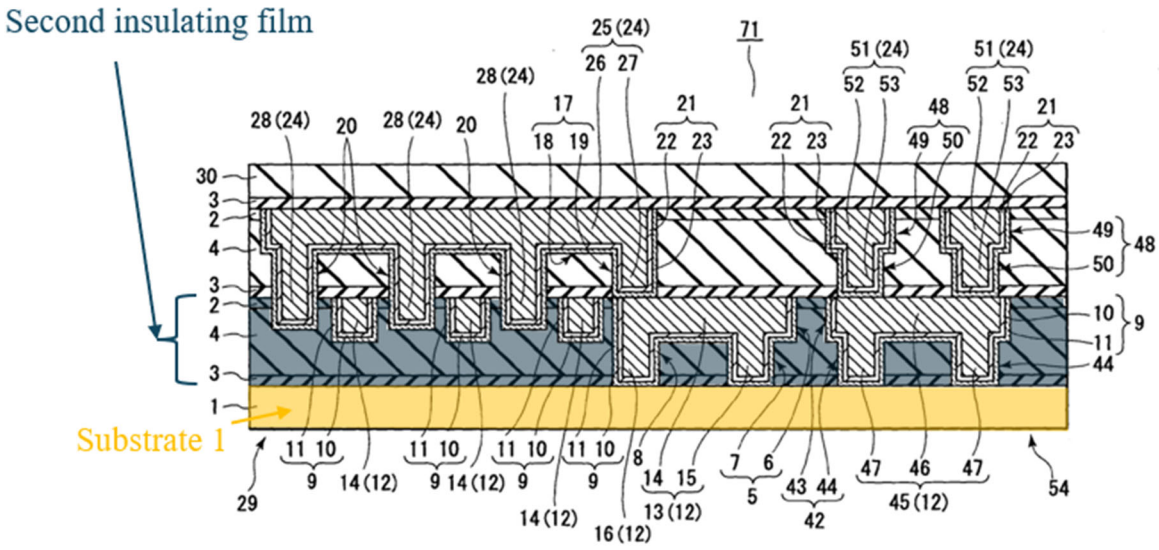


FIG. 14

b) [44.b] – "*wherein the first interconnect is formed on the second insulating film*"

374. Element [44.b] calls for "wherein the first interconnect is formed on the second insulating film," which Hasunuma discloses.

375. Hasunuma's first interconnect (conductive layer 14) is formed on the second insulating film. TSMC-1005, ¶¶[0092]-[0098], Figs. 3A, 8, 14. Conductive layer 14 is further shown in annotated Figures 8 and 14 below:

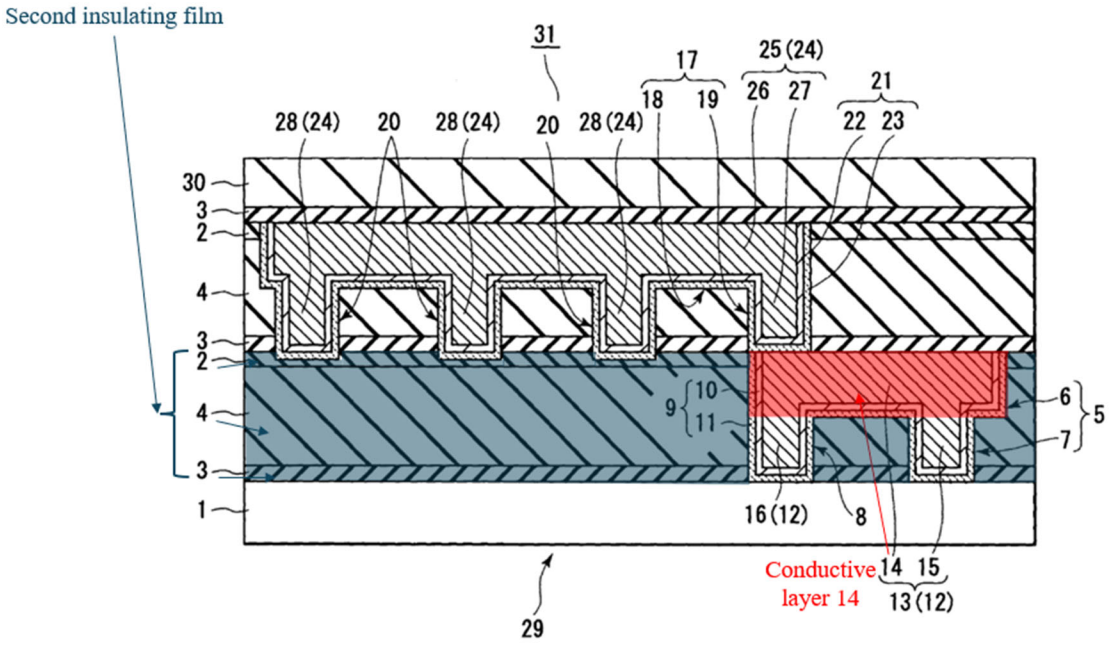


FIG. 8

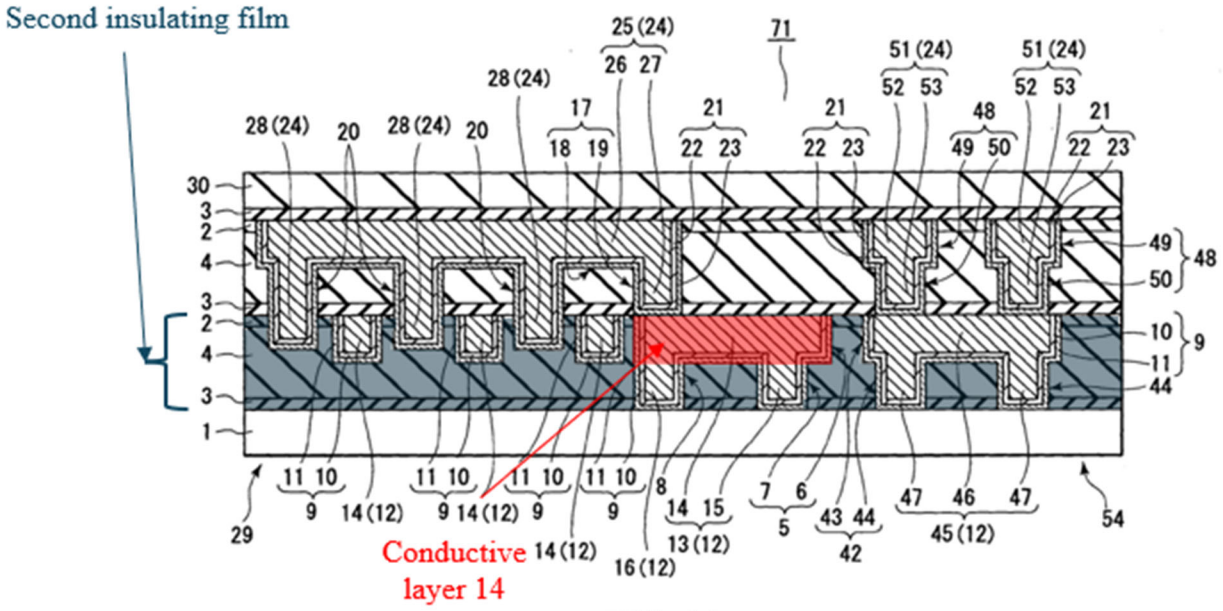


FIG. 14

c) [44.c] – "*a bottom of the dummy via is located in the second insulating film*"

376. Element [44.c] calls for "a bottom of the dummy via is located in the second insulating film," which Hasunuma discloses.

377. As explained for claim 41 *supra* §X.I.4, a bottom of Hasunuma's dummy vias (reinforcing plugs 28) extends into the second insulating film (collectively, insulating films 3, 4, 2), as seen in annotated Figure 8 below:

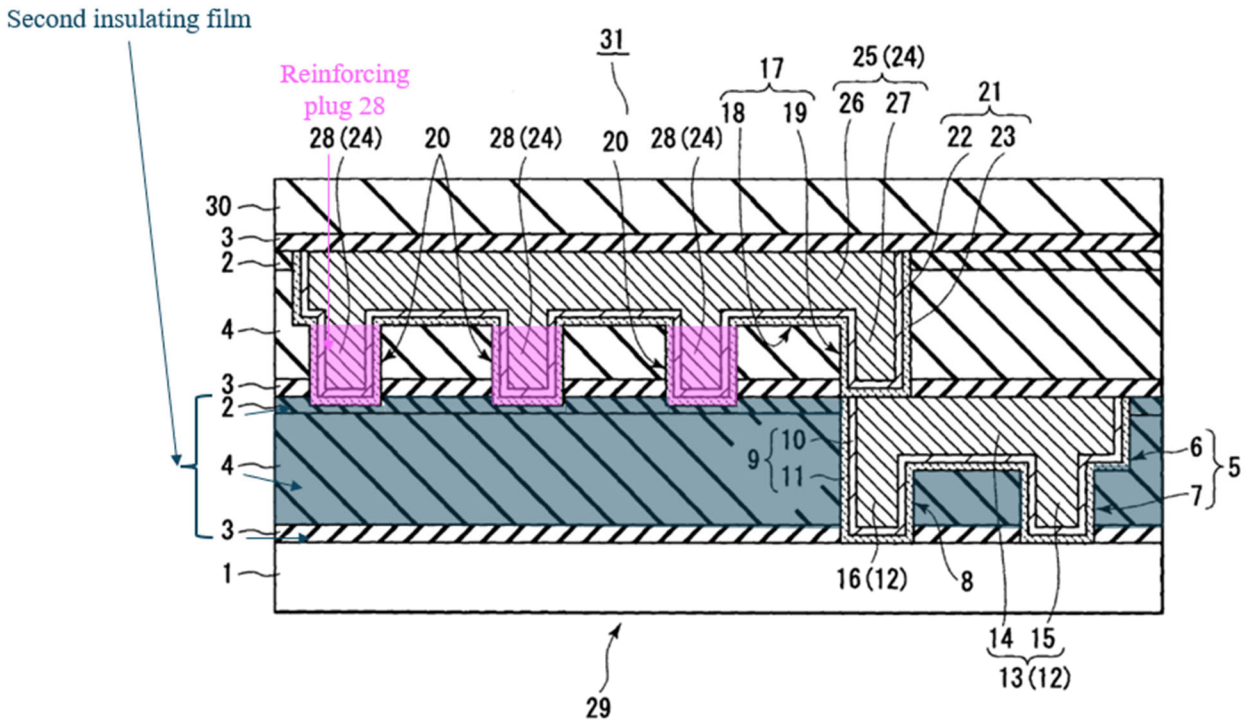


FIG. 8

TSMC-1005, ¶¶[0090], [0092], [0103]-[0104], Fig. 8.

378. The same analysis for Hasunuma's Figure 8 applies to its Figure 14 embodiment. Annotated Figure 14 is shown below, which discloses dummy vias extending even further into the second insulating film:

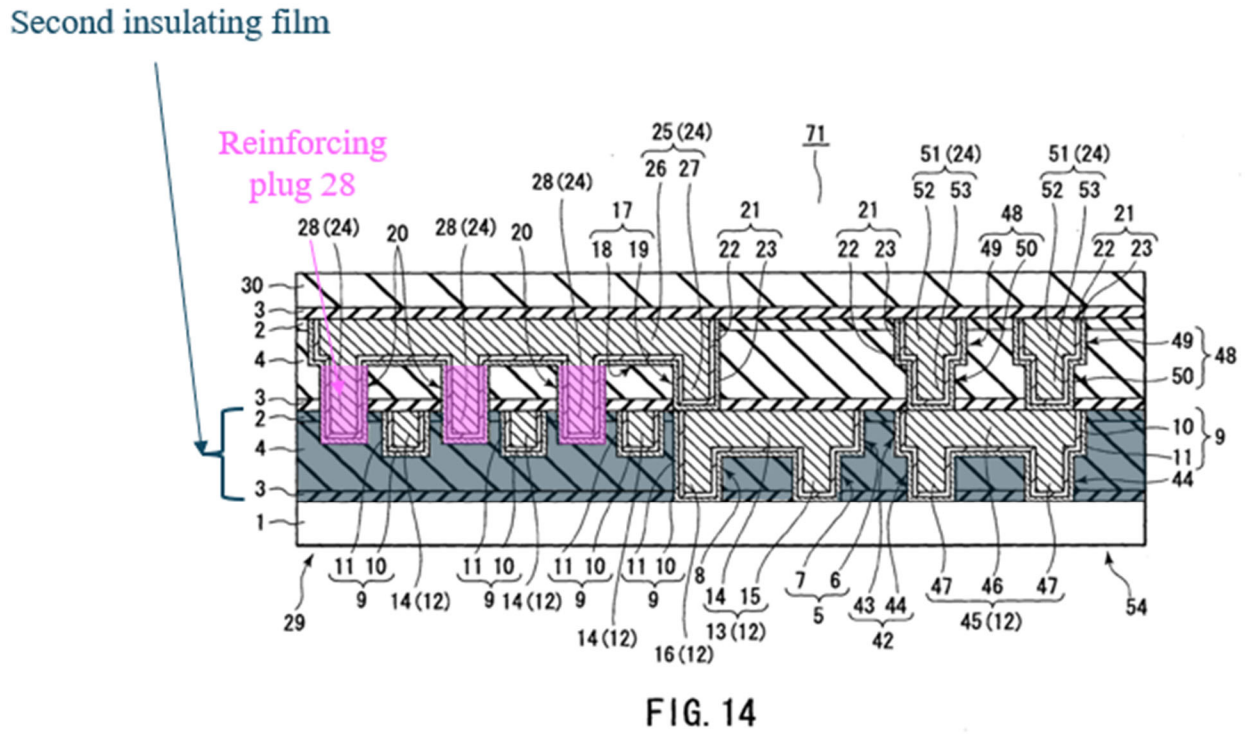


FIG. 14

Id., ¶¶[0176]-[0178], Fig. 14.

379. The Figure 14 embodiment also meets claims 1 and 44 with the "second insulating film" being Hasunuma's lower layer films 3 and 4 or lower layer films 2 and 4.

J. Ground 9: Claim 5 Is Obvious Over Hasunuma and Kurashima

380. Hasunuma and Kurashima render claim 5 obvious to a POSITA. Claim 2 is discussed below, because challenged claim 5 (as well as claim 6 in ground 9 below) depends from it.

1. Claim 2

a) [2.a] – "*semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate*"

381. Element [2.a] recites the "semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate," which Hasunuma discloses.

382. Hasunuma discloses a second insulating film (e.g., the stack of insulating films 3, 4, and 2 in Figure 3A)[9], on silicon substrate 1, as seen in annotated Figure 8:

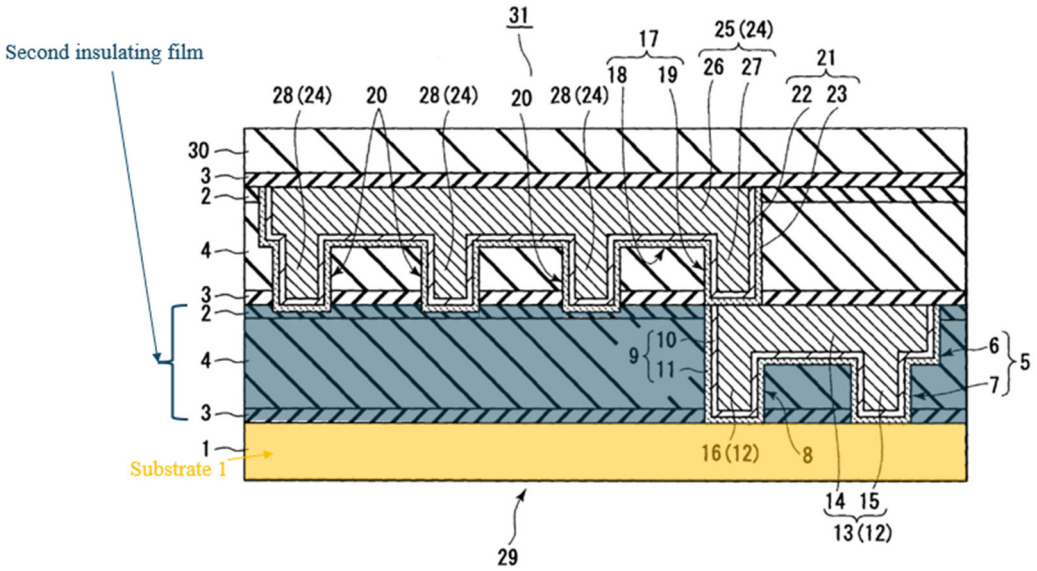


FIG. 8

[9] In the alternative, any or both of films 3 and 4 also satisfies the "second insulating film" element, as each of these films/combinations is on the substrate and otherwise satisfies the requirements of claim 2.

TSMC-1005, ¶¶[0090]-[0091], Figs. 8, 14.

b) [2.b] – "*wherein the first interconnect is formed on the second insulating film*"

383. Element [2.b] calls for "wherein the first interconnect is formed on the second insulating film," which Hasunuma discloses.

384. Hasunuma discloses first interconnect (e.g., conductive layer 14) on the second insulating film, as seen in annotated Figure 8:

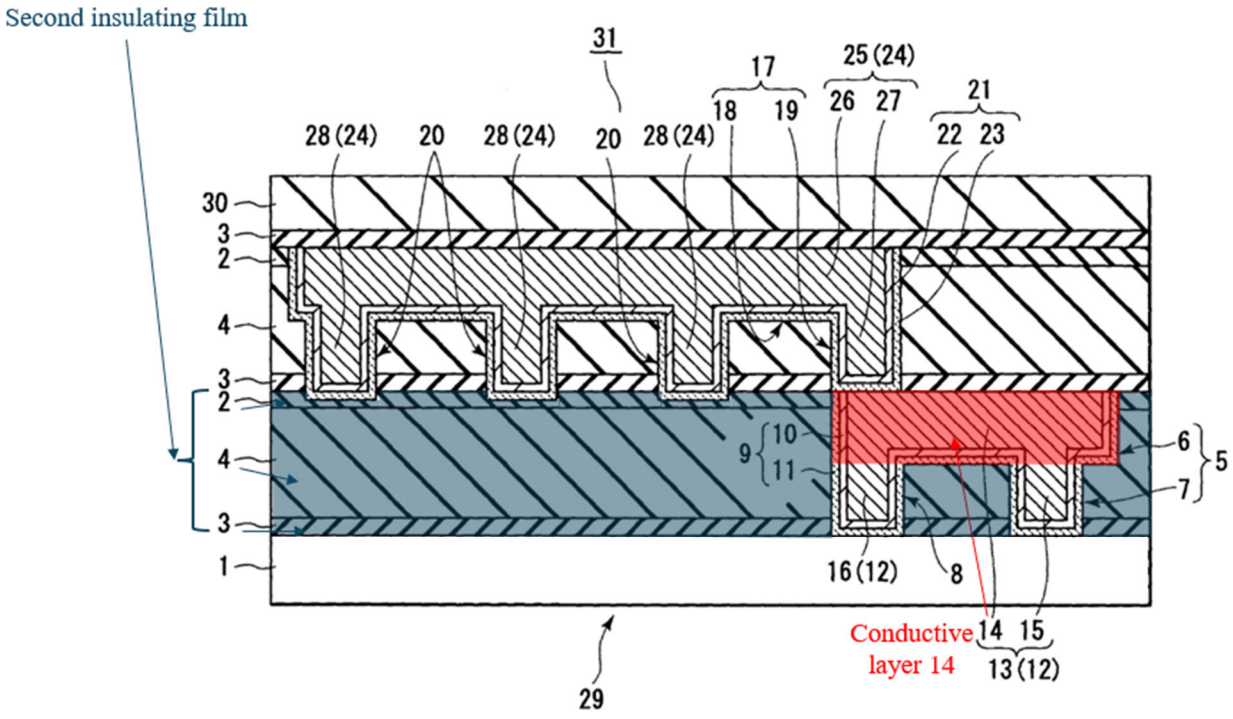


FIG. 8

TSMC-1005, ¶¶[0092]-[0098], Figs. 3A, 8, 14.

c) [2.c] – "*the dummy via is connected to a first dummy interconnect formed on the second insulating film*"

385. Element [2.c] calls for "the dummy via is connected to a first dummy interconnect formed on the second insulating film," which Hasunuma and Kurashima disclose.

386. Hasunuma discloses dummy vias (e.g., "reinforcing plugs 28"), as seen in annotated Figure 8:

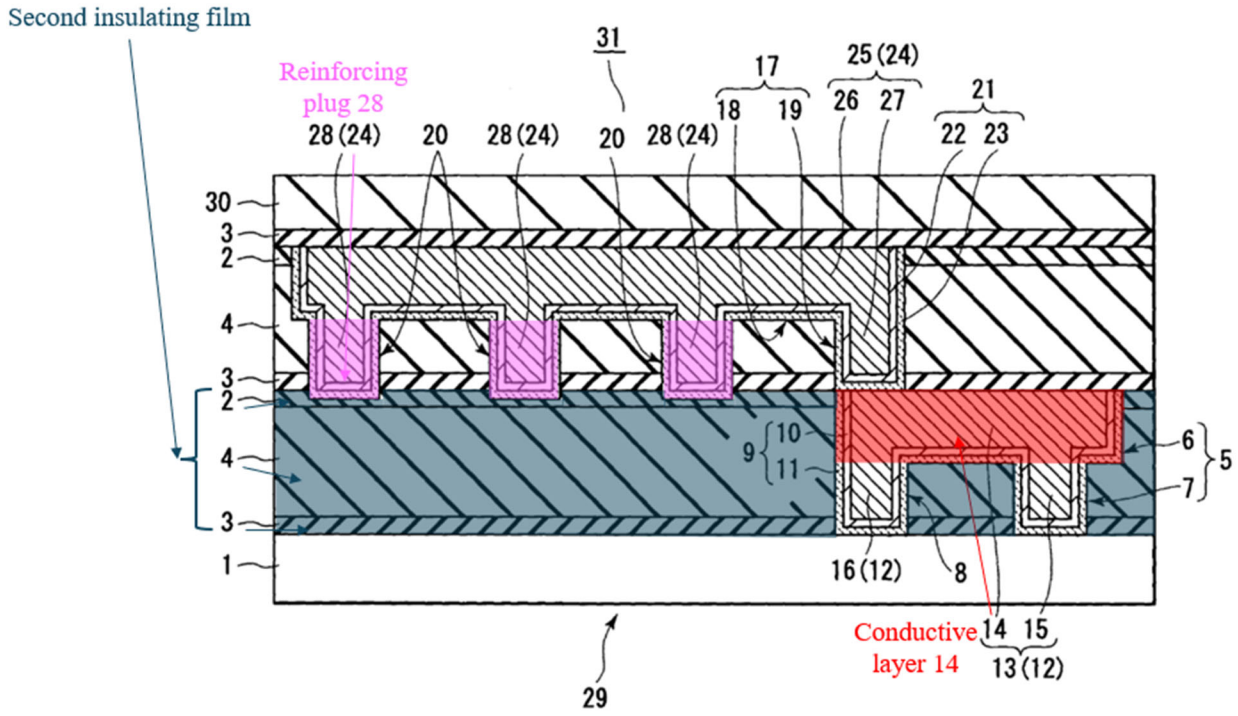


FIG. 8

TSMC-1005, Fig. 8.

387. Kurashima discloses simultaneously forming both a first interconnect (e.g., "Cu-wire 9" and "TaN-film 7," hereafter collectively "Cu-wire 9") and a first dummy interconnect (e.g., "Cu-dummy wire 10" and "TaN-film 7," hereafter collectively "Cu-dummy wire 10") on a semiconductor substrate (e.g.,

"semiconductor substrate 1"). TSMC-1011, 4:12-21, 4:50-6:57, Figs. 1B-1D. For example, Kurashima teaches forming dummy wire 10 in first interlayer insulating film 4, and then dummy wire/via 17 is formed connecting to dummy wire 10, as seen in annotated Figure 3A:

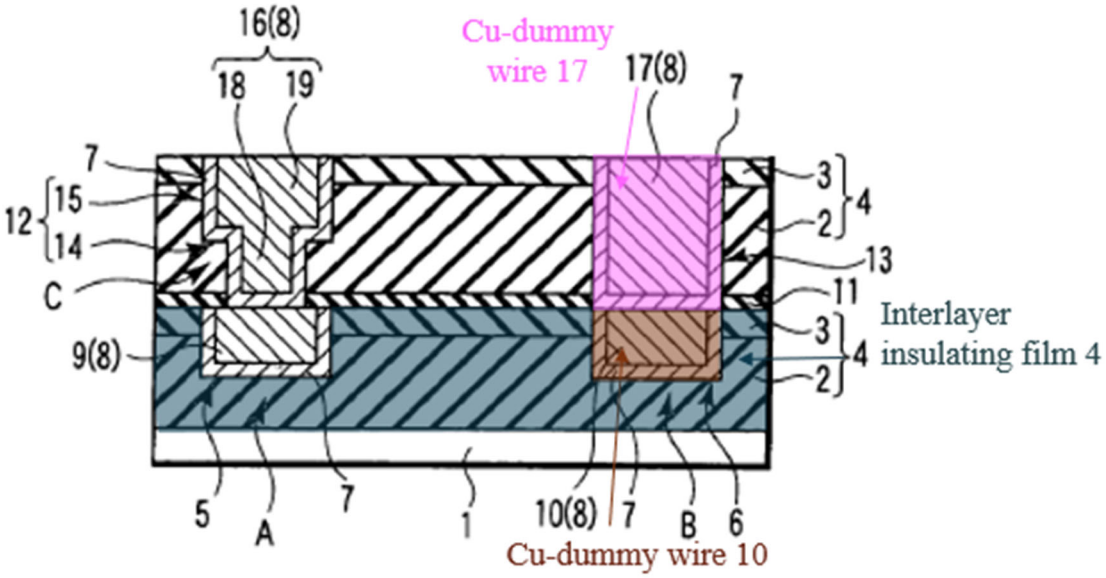


FIG. 3A

Id., Fig. 3A.

388. A POSITA would understand that dummy wire 10 is a dummy interconnect both because of its description as a "dummy" structure and its purpose (i.e., to add structural support to the device and prevent peeling of layers rather than as an active circuit element), which is consistent with the '623 patent's description of a "dummy interconnect." Specifically, dummy wire 10 does not constitute part of a closed circuit in actual use of the device, i.e., no current flows therein during use. *Id.*, 4:58-61. Rather, Kurashima uses dummy wire 10 (and its direct connection

to a dummy via, i.e., "Cu-wire 9") to add structural support to the device and thereby reduce film peels. *Id*., 5:63-6:32 ("Therefore, the SiC film 3 is substantially connected to the low-relative-dielectric-constant film 2 via the Cu-dummy wire 10 and TaN-film 7. Accordingly, the adhesion at the interface between the SiC-film 3 and low-relative-dielectric-constant film 2 is enhanced to a size that can bear a physical load of CMP. That is, the durability of the interlayer insulating film 4 against the mechanical stress in the CMP process is enhanced in forming the Cu-wire 9 and Cu-dummy wire 10 of the first layer. Accordingly, the film peels in the layer are reduced."). Thus, the connection between dummy wire 10 and dummy wire 17 enhances the adhesion between insulating layers (especially at the interface with a low-dielectric film like Kurashima's low dielectric film 2) and improves durability against CMP-induced stress. Additionally, Kurashima's device would still be operable if dummy wire 10 was omitted, because it serves no part in routing current flow as part of the actual operation of the device.

d) Combination of Hasunuma and Kurashima

389. A POSITA was motivated to improve the mechanical strength of Hasunuma's structure by applying Kurashima's teaching to connect Hasunuma's reinforcing plug(s) 28 to a dummy interconnect beneath them. Kurashima's suggested addition from Figure 3A of dummy wire 10 to Hasunuma's Figure 8 structure is illustrated below:

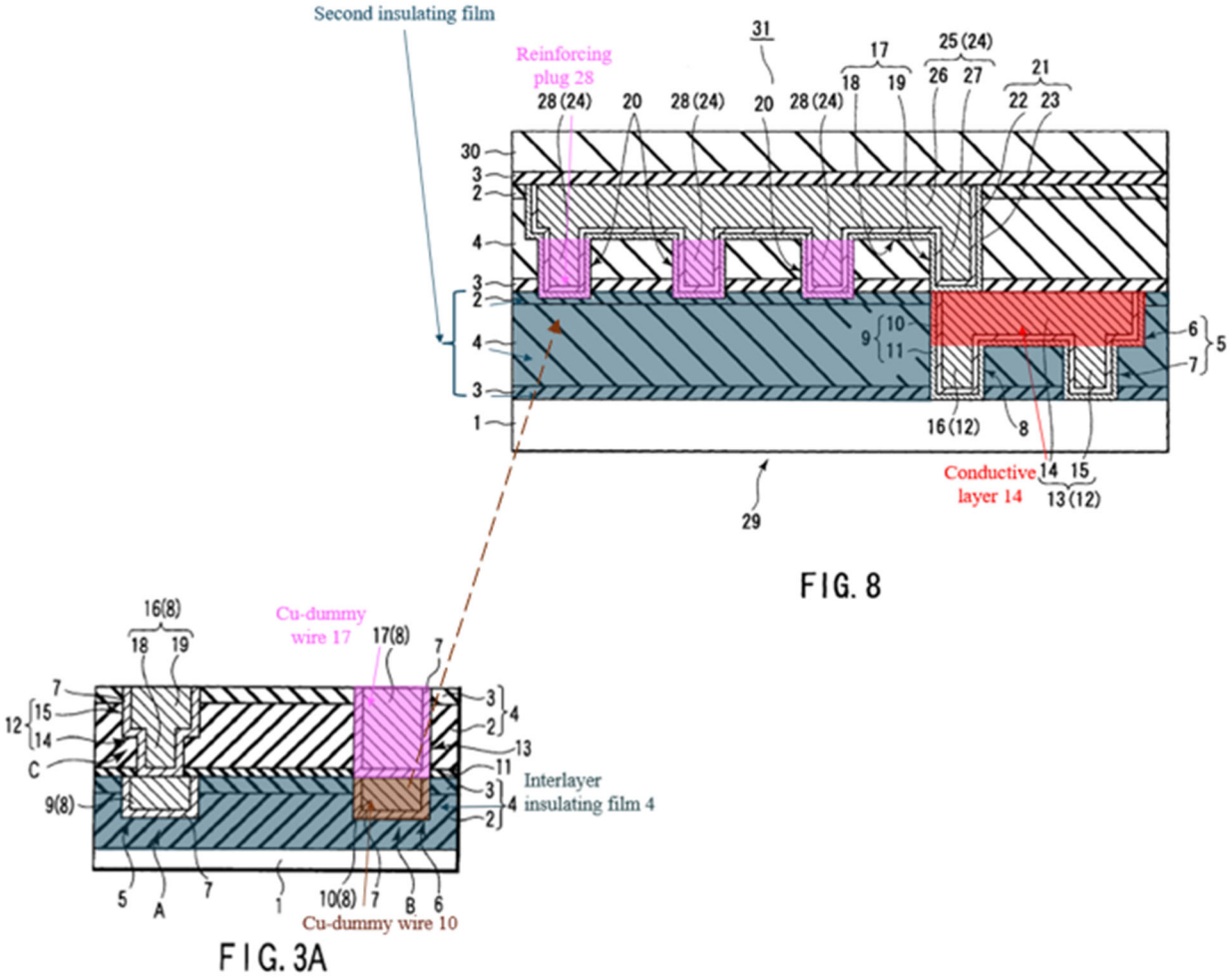


FIG. 8

FIG. 3A

390. A POSITA was motivated to incorporate Kurashima's dummy interconnect(s) into Hasunuma's device to increase the interlayer strength of the semiconductor device to reduce the likelihood of layer peeling or film separation between Hasunuma's lowermost insulating films 4 and 2 (i.e., its low-k film 4 and the overlying insulating film 2), as expressly discussed by Kurashima in regard to its low-k film 2 and overlying insulating film 3. *See* TSMC-1011, 5:63-6:32 ("According to experiments conducted by the present inventors, when the Cu-dummy wire 10 is not formed, as shown in FIG. 5A, during the first polishing, a film

peel was generated at an interface between the low-relative-dielectric-constant film 2 and SiC-film 3. Additionally, in the present embodiment in which the Cu dummy wire 10 is formed, as shown in FIG. 1D, even when not only the first polishing but also the second polishing end, the film peel was hardly generated in the interface between the low-relative-dielectric-constant film 2 and SiC-film 3."), 8:14-34, Figs. 5A-5B.

391. Kurashima expressly discusses the significance of extending the overlying dummy via such that it contacts the dummy interconnect, in discussing how film peel may still occur when the overlying dummy via is not extended to the dummy interconnect, as depicted in Figure 5B:

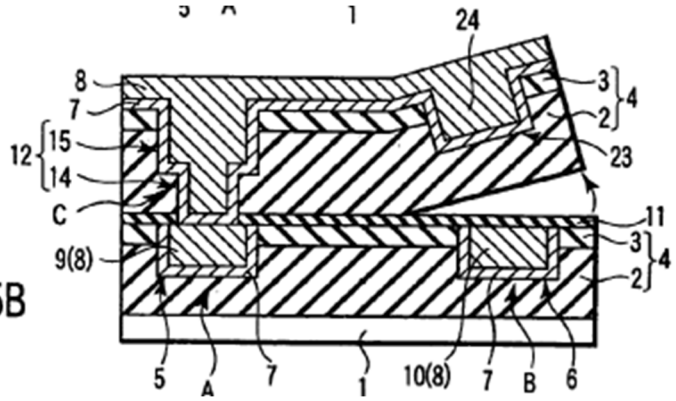


FIG. 5B

Id., 8:14-34, Fig. 5B.

392. A POSITA would have readily recognized that implementing a dummy interconnect connected in Hasunuma such that it was connected to a dummy reinforcing plug 28 would have helped prevent separation with the first insulating layer stack of Hasunuma's device (i.e., as between Hasunuma's low-dielectric

constant film 4 and the insulating film 2 directly on top of it) similar to the corresponding structure of Kurashima.

393. Additionally, a POSITA would have been further motivated to incorporate such a dummy plug-dummy interconnect structure to establish additional structural support and uniformity during the polishing step to reduce dishing. *See id.*, 5:63-6:32; TSMC-1007, 4:12-44. Use of dummy structures to prevent dishing was widely known and utilized prior to the '623 patent. As noted for example in Figure 8 of Hasunuma below, there is a large vacant space in the insulating film beside conductive layer 14:

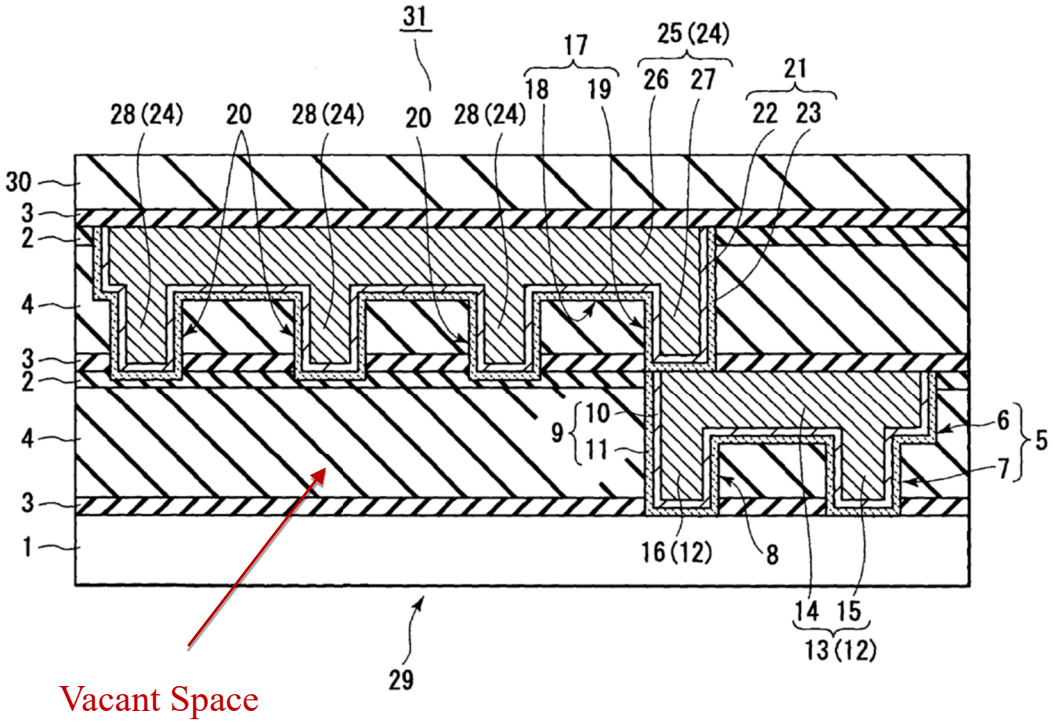


FIG. 8

394. A POSITA would have readily recognized that adding a dummy interconnect connected to dummy plugs 28 in this space would have helped prevent dishing that may otherwise occur during the polishing step (*see* TSMC-1005, Fig. 3A, ¶[0098]) for the formation of the conductive layer 14. *See also* TSMC-1024, 2:55-58 ("This application of dummy patterns results in better fill in bulk metal circuit lines with subsequent improved planarization after CMP and in the elimination of dishing or surface concavity after CMP of large open areas.").

395. A POSITA would have expected success when incorporating Kurashima's dummy plug-dummy interconnect structure into Hasunuma's device, which entailed only the positioning of a dummy interconnect beneath one or more of the dummy vias/reinforcing plugs 28 of Hasunuma. Creation of the dummy interconnect could have been easily accomplished using the same processing steps already utilized in Hasunuma to create its first interconnect layer ("conductive layer 14"), with the dummy via ("first reinforcing plug 28") connected thereto as part of building the next level in Hasunuma's Figure 8 structure. *See, e.g.,* TSMC-1005, ¶¶[0090]-[0099], Figs. 1A-3A. For example, a POSITA would have readily recognized that the dummy interconnect need merely be patterned and created in the same layer and manner as conductive layer 14 using the same processing techniques already used in Hasunuma to create conductive layer 14. Reinforcing plug 28 could then have been easily connected to the dummy interconnect using the same

processing techniques already disclosed in Hasunuma as being used to create reinforcing plug 28 and conductive plug 27 (whereby conductive plug 27 is connected to conductive layer 14).

2. Claim 5

a) [5.a] – "*semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view*"

396. Element [5.a] recites the "semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view," which Hasunuma and Kurashima render obvious.

397. Hasunuma discloses that its dummy vias ("reinforcing via plugs") can be circular, such as shown in Figures 19A, 22A-22C, and 24A-27C. TSMC-1005, Figs. 19A, 22A-22C, 24A-27C. Annotated Figs. 22A-22C show this via shape:

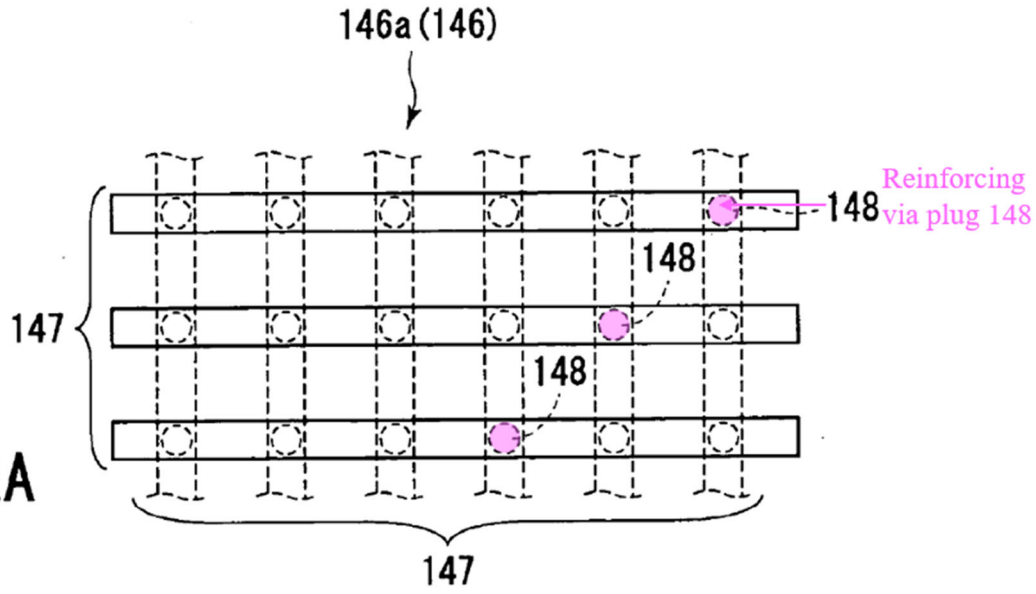


FIG. 22A

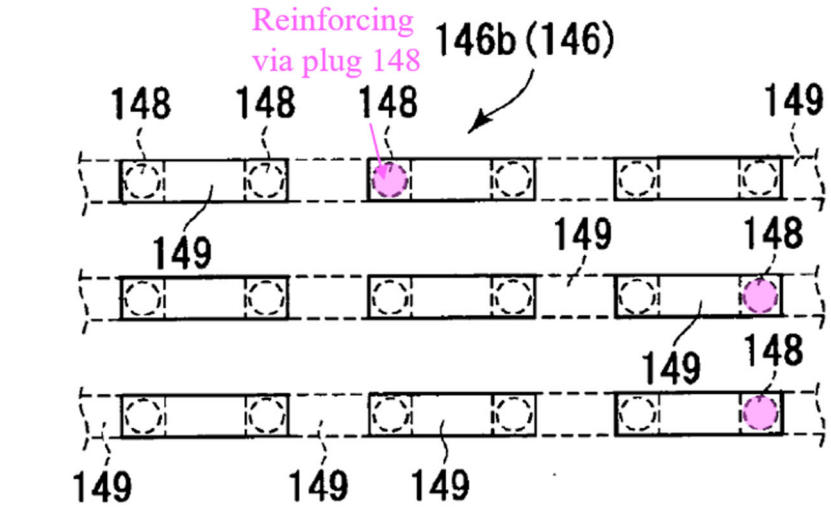


FIG. 22B

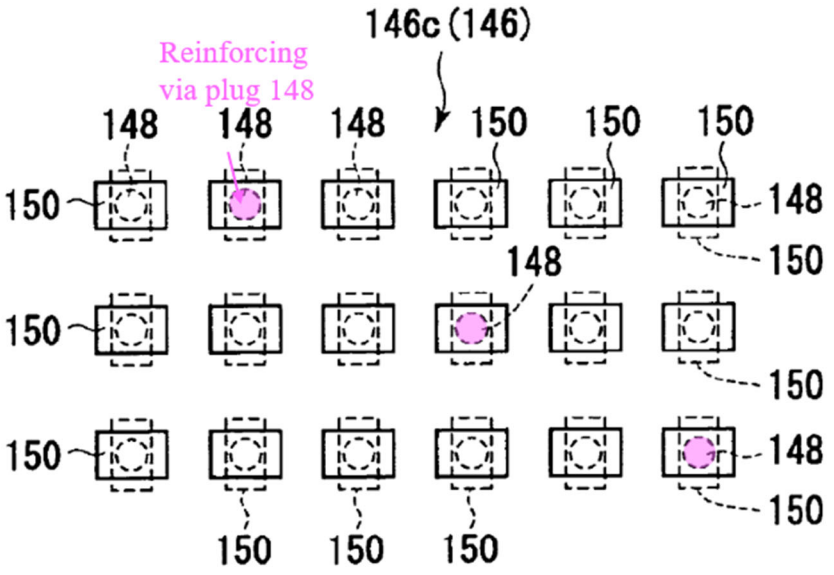


FIG. 22C

Id., Figs. 22A-22C.

398. It would have been obvious to utilize these round dummy vias in the Figure 8 embodiment because the choice of via shape is a mere design choice, with circular shapes being well-known as illustrated by Iizuka. *See, e.g.*, TSMC-1008, 9:44-47 ("[T]he opening of the via-hole may have any configuration, such as a

square, rectangle or circle."); *see also* TSMC-1013, 8:47-52 (noting that circular vias may be used, among other shapes). Circular-shaped vias were also easier to process. TSMC-1038, 7:62-67.

399. Hasunuma also discusses the "diameter" of the dummy via ("reinforcing via plug 28"), thus indicating that it is circular shaped. TSMC-1005, ¶[0127]. In addition to Hasunuma's express disclosure of circular vias, use of this shape was obvious for the reasons I discussed for Claim 23 in Ground 2 and Claim 5 in Ground 3 (*supra*, §§X.C.1-2, X.D.1-2). Circular vias were an easily achieved design choice, being both well-known and easier to process and, thus, a POSITA would have expected success in making circular vias. *Supra*, §§X.C.1-2, X.D.1-2.

b) [5.b] – "*a diameter of the dummy via is substantially equal to a width of the first dummy interconnect*"

400. Element [5.b] calls for "a diameter of the dummy via is substantially equal to a width of the first dummy interconnect," which Hasunuma and Kurashima render obvious.

401. Hasunuma's reinforcing plug 28 ("dummy via") has a diameter of 0.13 μm, substantially equal to the width of its reinforcing layers, such as shown in Figures 22A and 24A. TSMC-1005, ¶[0127], Figs. 22A, 24A.

402. The combination of Hasunuma and Kurashima results in the width of Hasunuma's plug 28 ("dummy via") being substantially equal to the width of the

first dummy interconnect, as expressly disclosed by Kurashima. Accordingly, when combined for the reasons discussed *supra* §X.J.1.(d), Hasunuma and Kurashima satisfy claim 5.

403. A POSITA would have had a reasonable expectation of success in implementing Hasunuma's dummy vias in its Figure 8 embodiment with circular shapes having diameters substantially equal to the dummy interconnect because Iizuka confirms that circular-shaped vias were standard. TSMC-1008; 9:45-47; *see also* TSMC-1005, ¶[0200], Fig. 19A; TSMC-1013, 8:47-52; TSMC-1014, ¶[0091]; TSMC-1038, 7:62-67. This configuration would have been easily accomplished using the standard patterning and manufacturing techniques used to make the interconnect structure in general. *Id*. These references show that it was well known how to pattern via holes having circular cross-sections using masks, photolithography, and etching, and such round patterns subsequently result in circular vias when conductive material is deposited into the patterned vias holes. It was likewise straightforward to set the via diameter equal to the dummy interconnect width, as Kurashima taught.

K. Ground 10: Claim 6 Is Obvious Over Hasunuma, Kurashima and Iizuka

404. Hasunuma, Kurashima and Iizuka render claim 6 obvious to a POSITA. Hasunuma and Kurashima render claim 2 obvious as discussed above, from which claim 6 depends.

1. Claim 6

a) [6.a] – "*semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square*"

405. Element [6.a] recites the "semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square," which Hasunuma, Kurashima and Iizuka render obvious. As discussed above, Hasunuma discloses the elements of claim 1, and Hasunuma and Kurashima render claim 2 obvious. *Supra*, §§X.I.1, X.J.1.

406. Hasunuma discloses square dummy vias (e.g., "Cu reinforcing via plug 114") as shown in Figure 18A, annotated below:

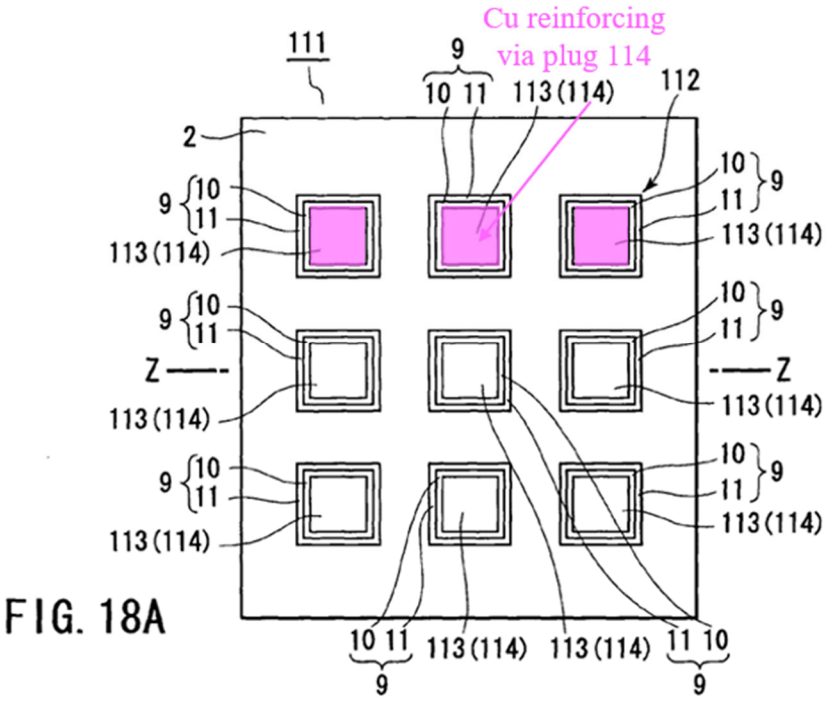


FIG. 18A

TSMC-1005, Fig. 18A.

407. Iizuka likewise teaches vias having square shapes, making square shapes a well-known design option that could be easily implemented for dummy vias. TSMC-1008, 9:45-47 ("the opening of the via-hole may have any configuration, such as **a square**, rectangle or circle.") (emphasis added); TSMC-1004, Figs. 2, 5, 9; TSMC-1013, 9:45-49. Additionally, square-shaped vias align more efficiently with orthogonal interconnect lines, leading to a more compact layout and better utilization of area compared to circular vias in such scenarios to achieve increased contact area with interconnects above and/or below the via. *See, e.g.*, TSMC-1014, ¶¶[0092], Figs. 8, 14 (teaching square vias as preferred for certain

interconnect junctions); TSMC-1039, 5:27-32 (noting the increased electrical contact area achieved by square vias).

408. Thus, it was obvious to implement Hasunuma's vias (conductive plugs 27) and dummy vias (reinforcing plugs 28) with this common planar square shape, as disclosed by Hasunuma and taught by Iizuka, which would have been easily achieved. *See also infra*, §§X.L.1, 3.

409. Further, because a POSITA was aware of the basic available via shapes, and was aware of the role of the dummy vias in improving mechanical stability (*supra*, §IX.B) as well as reducing stress-induced voiding and electromigration problems as taught, for example, by Watanabe (*supra*, §IX.A), it would have been a matter of routine optimization to choose the via shape that works best for a given overall design. With a few basic shapes to choose from (e.g., circular, square, rectangular), it would not have required an undue amount of experimentation to arrive at the optimal via shape, and a POSITA would have expected success in forming the dummy via with a planar shape that is substantially a square.

b) [6.b] – "*a side of the dummy via is substantially equal to a width of the first dummy interconnect*"

410. Element [6.b] calls for "a side of the dummy via is substantially equal to a width of the first dummy interconnect," which Hasunuma, Kurashima, and Iizuka render obvious.

411. Hasunuma teaches vias having a dimension of "about 0.13 μm," and in the same paragraph, teaches that wiring layer 13 (which includes the first interconnect (conductive layer 14)) also has a width of "about 0.13 μm." TSMC-1005, ¶[0127].

412. It was obvious to a POSITA, when implementing the square via shape shown in Hasunuma's Figure 18A and taught by Iizuka, to utilize a square dummy via having a side dimension equal to the width of the first dummy interconnect (as suggested by both Hasunuma (*id.*) as well as by Kurashima (*supra*, §§X.D.1-2)), given that both Hasunuma and Kurashima teach equal sizes for their via and first interconnect. TSMC-1005, ¶[0127]. Arriving at the claimed configuration would have at most amounted to routine optimization, just as the Examiner suggested during prosecution. TSMC-1002, 244-45, 292-96.

413. A POSITA would have been motivated by the same advantages I already discussed above for implementing equal width dummy vias and dummy interconnects, including ensuring a secure connection while minimizing the dummy wiring footprint and undesired parasitic capacitance and cross-talk with adjacent wirings. *Supra*, §§X.D.1-2. Additionally, a POSITA would have expected success given that square vias were common as recognized by, *inter alia*, Iizuka and Hasunuma, and that sizing the landing wire relative to the via was a standard design consideration, as confirmed by Hasunuma teaching a via having a same size (0.13

μm) as the width (0.13 μm) of the interconnect connected to the via (TSMC-1005, ¶[0127]).

L. Ground 11: Claims 19-20 Are Obvious Over Hasunuma and Watanabe

414. Hasunuma discloses claim 1 as discussed above, from which claims 19-20 depend. Hasunuma and Watanabe render claims 19-20 obvious as detailed below.

1. Claim 19 – "*semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square*"

415. Claim 19 recites the "semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square," which Hasunuma in view of Watanabe renders obvious.

416. Hasunuma discloses planar views of dummy vias 114 that are square, for example, in Figure 18A (TSMC-1005, Fig. 18A):

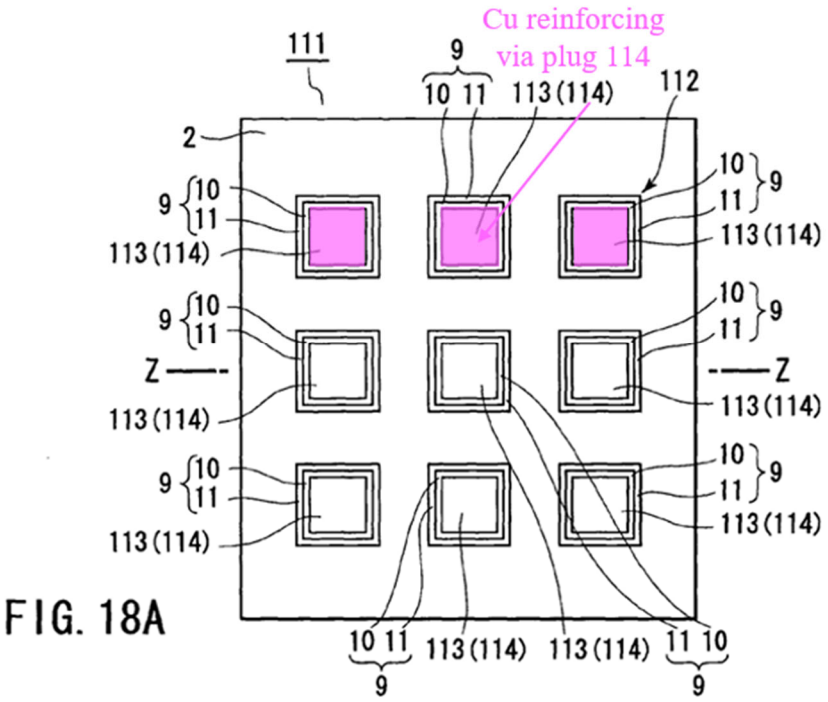
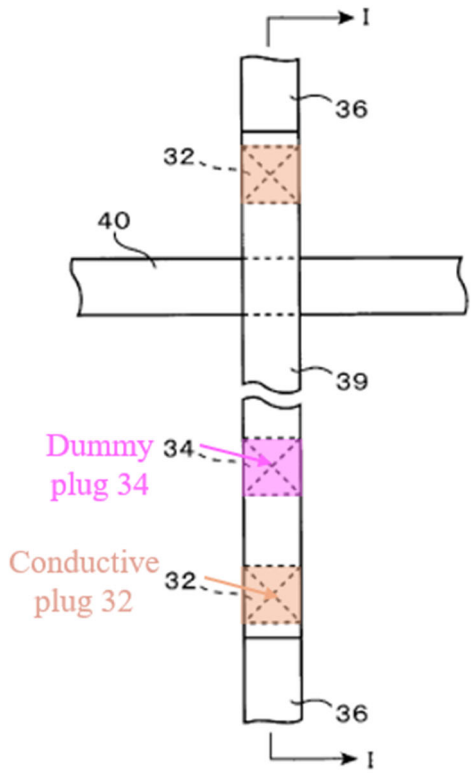


FIG. 18A

417. Thus, given Hasunuma's clear disclosure of square-shaped vias in Figure 18A and the common usage at the time of square-shaped vias, a POSITA would have understood Hasunuma to disclose substantially square-shaped vias as a known design option for any of the vias or dummy via in any of its embodiments.

418. Additionally, Watanabe's plan view figures (e.g., Figures 2, 4, and 9) consistently disclose square vias and dummy vias (plugs 32 and dummy plugs 34, respectively). *Supra*, §X.A.4. As one example, annotated Figure 2 of Watanabe is shown below with the square-shaped vias and dummy vias denoted:

FIG. 2



419. It was obvious in view of both Hasunuma's and Watanabe's disclosures of square vias and the knowledge of a POSITA at the time to make both the planar shape of the vias and the dummy vias in Hasunuma's various embodiments substantially square.

420. Both Hasunuma and Watanabe address similar problems (reliability in damascene interconnect structures) with similar foundational solutions (dummy vias extending from the interconnect above). It would have been nothing more than a simple substitution to adopt Watanabe's specific via/dummy via shapes. For

example, choosing specific shapes (e.g., square) as taught by Watanabe would be routine design choices to meet particular layout or process requirements within Hasunuma's framework. Indeed, Iizuka teaches square cross-sectional shapes for vias: "the opening of the via-hole may have any configuration, such as a square, rectangle or circle," and a circular/square pattern means the resulting via formed in a circular/square hole would have a substantially circular/square shape. TSMC-1008, 9:44-47, 10:17-22.

421. In addition, via shapes, such as square or circular, each provide known advantages applicable to a given situation. For example, square-shaped vias align more efficiently with orthogonal interconnect lines, leading to a more compact layout and better utilization of area compared to circular vias in such scenarios to achieve increased contact area with interconnects above and below the via. *See, e.g.,* TSMC-1014, ¶[0092], Figs. 8, 14 (teaching square vias as preferred for certain interconnect junctions); TSMC-1039, 5:27-32 (noting the increased electrical contact area achieved by square vias). A POSITA would have recognized that the fundamental mechanical strength enhancing function of Hasunuma's dummy vias (as well as the electrical-connection function of Hasunuma's active vias), would be achieved with vias having square cross-sections.

422. Further, because a POSITA was aware of the basic available via shapes, and was aware of the role of the dummy vias in providing a mechanical

strengthening function as well as reducing stress-induced voiding and electromigration problems as taught, for example, by Watanabe, it would have been a matter of routine optimization to choose the via shape that works best for a given overall design. With a few basic shapes to choose from (e.g., circular, square, rectangular), it would not have required an undue amount of experimentation to arrive at the optimal via shape.

423. A POSITA would have had a reasonable expectation of success in implementing Hasunuma's vias (both functional and dummy) with a square cross-sectional shape, as this would easily be accomplished using the standard patterning and manufacturing techniques used to make the interconnect structure in general. Certainly it was well known how to pattern via holes having square cross-sections using masks, photolithography, and etching, and such square patterns subsequently result in square vias when conductive material is deposited into the patterned vias holes. TSMC-1004, Figs. 2, 4, 5, 9; TSMC-1005, Fig. 18A; TSMC-1014, ¶[0092], Figs. 8, 14; TSMC-1039, 5:27-32.

424. Accordingly, claim 19 is obvious over Hasunuma and Watanabe.

2. Claim 20 – "*semiconductor device of claim 19, wherein a length of a side of the via and a length of a side of the dummy via are substantially equal to each other*"

425. Claim 20 recites the "semiconductor device of claim 19, wherein a length of a side of the via and a length of a side of the dummy via are substantially equal to each other," which Hasunuma in view of Watanabe renders obvious.

426. As discussed *supra* §X.L.1, Hasunuma in view of Watanabe shows that square vias and dummy vias were obvious. Moreover, Hasunuma's Figure 8 shows vias and dummy vias as having identical widths:

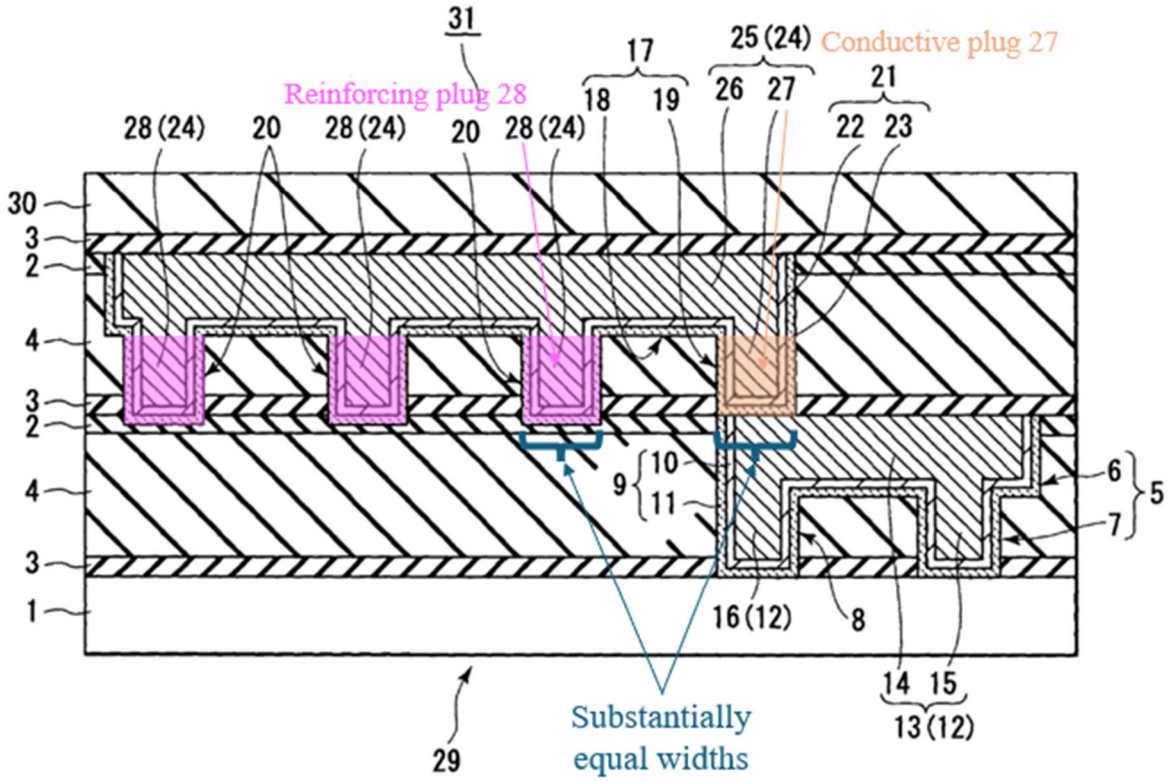


FIG. 8

TSMC-1005, Fig. 8.

427. Watanabe's plan view figures (e.g., Figures 2, 4, 5A, 9) also consistently disclose square vias and dummy vias having identical side lengths.

FIG. 2

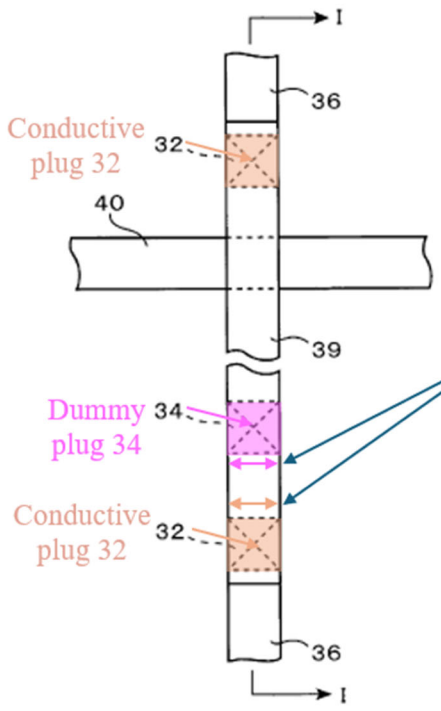
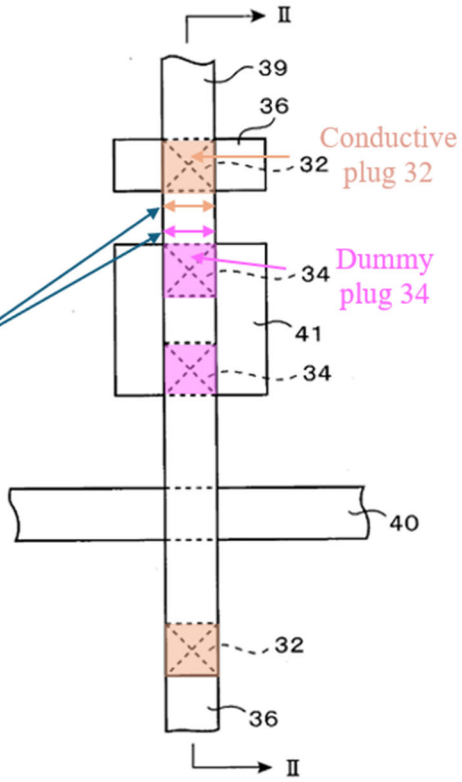
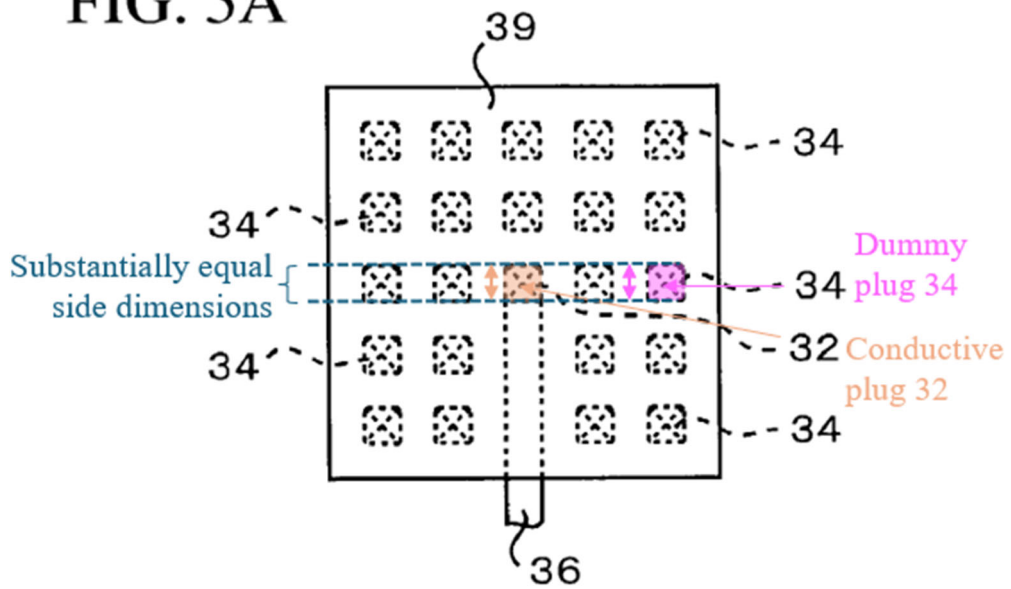


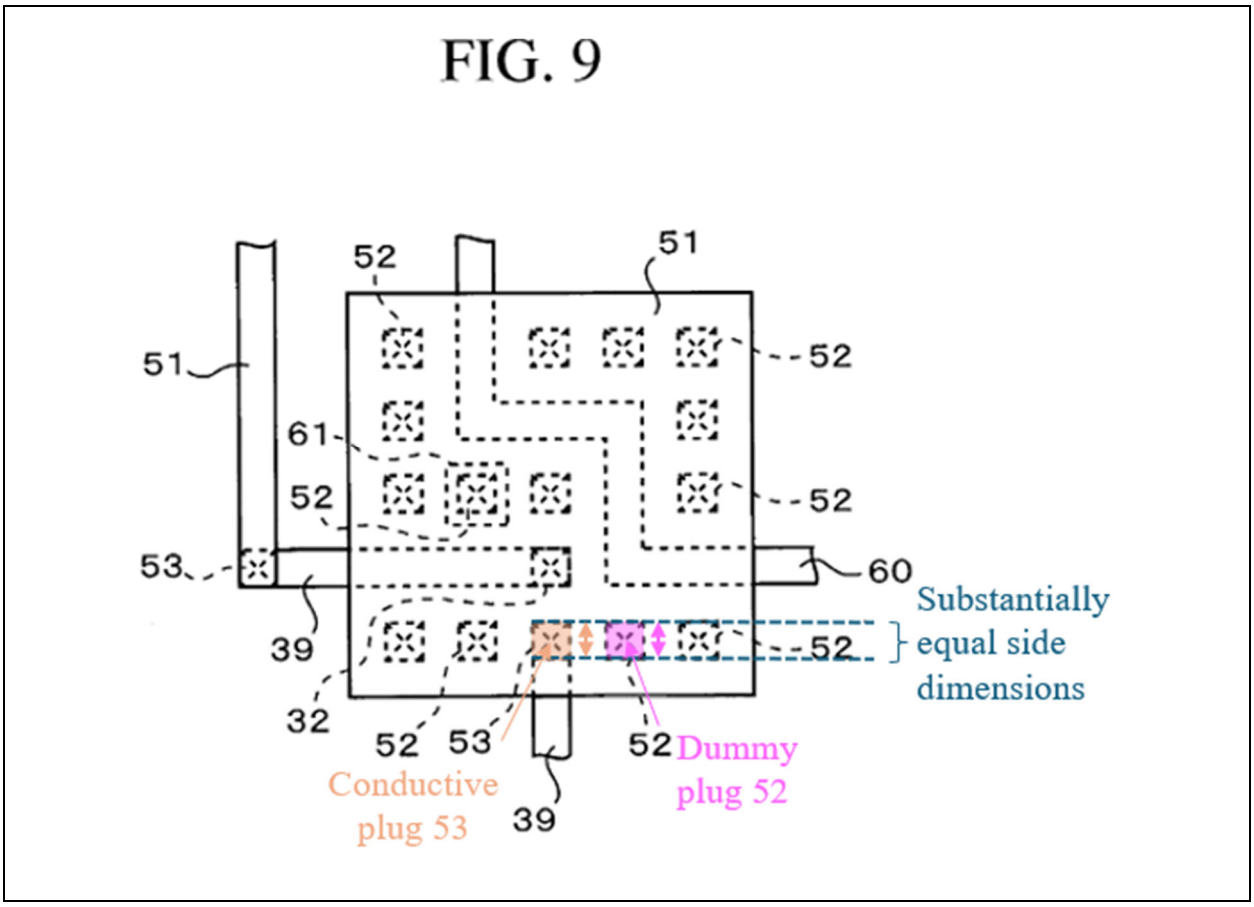
FIG. 4



Substantially equal side dimensions

FIG. 5A





TSMC-1004, Figs. 2, 4, 5A, 9.

428. Hasunuma's example assigns identical dimensions (0.13 µm) to both its conductive via plug 27 and its reinforcing via plug 28. TSMC-1005, ¶[0127]. Similarly, Watanabe's simulation model likewise assigns identical dimensions (0.15 µm) to both its functional and dummy vias (TSMC-1004, ¶[0083]), further teaching that the vias and dummy vias have an identical side dimension.

429. In implementing Hasunuma's vias and dummy vias as squares, it was obvious to make the vias and dummy vias substantially the same size (with

substantially the same side lengths), especially for design consistency and process commonality, as directly suggested by Watanabe's figures and modeling. Indeed, using consistent sizing allows for the same processing to be performed across the device, which simplifies the manufacturing process, reduces costs, and generally leads to increased reliability. A POSITA would have expected success, because both Hasunuma and Watanabe already teach to have vias and dummy vias with identical dimensions. And a POSITA would have logically understood that the same patterning/etching processes used to make holes for vias of one size could be used to make dummy vias of the same size (or vice versa).

3. Combination of Hasunuma and Watanabe

430. Both Hasunuma and Watanabe address similar problems (reliability in damascene-built interconnect structures) with similar foundational solutions (dummy vias extending from the interconnects). It would have been nothing more than a simple substitution to adopt Watanabe's specific via/dummy via sizes and shapes in Hasunuma's device. For example, choosing specific shapes (e.g., square) and dimensional relationships (via and dummy via sizes) as taught by Watanabe would have been routine design choices to meet particular layout or process requirements within Hasunuma's framework. This is further evidenced by other art at the time including Iizuka (as discussed elsewhere in my declaration), which teaches square cross-sectional shapes for vias: "the opening of the via-hole may have

any configuration, such as **a square**, rectangle or circle," and a circular/square pattern means the resulting via formed in a circular/square hole would have a substantially circular/square shape. TSMC-1008, 9:44-47, 10:17-22.

431. Furthermore, a POSITA recognized that it was obvious to combine specific advantageous embodiments or features from one known approach (Watanabe) into another (Hasunuma) whenever such features led to an improved or more optimized overall design. The underlying physics of stress migration, electromigration, and mechanical reinforcement in both Watanabe's and Hasunuma's devices are similar or the same (see, e.g., TSMC-1004, ¶¶[0016]-[0019], [0022]-[0033], [0071]-[0078], [0087], [0091]; TSMC-1005, ¶¶[0084]-[0089], [0103], [0115]-[0125]), such that a POSITA would have appreciated that dummy via geometry helps with both stress migration issues and mechanical stability for the interconnect structure. Accordingly, it would have been at most routine optimization for a POSITA to determine the beneficial shape (e.g., square) and relative sizes (e.g., square side dimensions) of the vias and dummy vias. *see also* TSMC-1002, 244-45, 292-96. As described above, example advantages for square shapes and equal via sizes are discussed above (including more efficient and compact layouts, increased contact area, increased mechanical strength, and improved processing).

432. Additionally, there would have been a high expectation of success in combining these teachings of Watanabe and Hasunuma. Both references describe conventional semiconductor materials and dual-damascene manufacturing processes. Incorporating Watanabe's specific via/dummy via shapes and dimensional relationships into Hasunuma's device would involve standard layout/patterning modifications using identical process steps, all well within a POSITA's capabilities. Indeed, a POSITA would have readily recognized that the same processes already disclosed in both Watanabe and Hasunuma could have been used to implement square vias and dummy vias having the same sizes/side lengths. Further, the functions of Hasunuma's and Watanabe's dummy vias are congruent, making their features readily combinable.

M. Ground 12: Claim 24 Is Obvious Over Hasunuma and Iizuka

433. Hasunuma discloses claim 1 as I discussed above, from which claim 24 depends. Hasunuma and Iizuka render claim 24 obvious as detailed below.

1. Claim 24

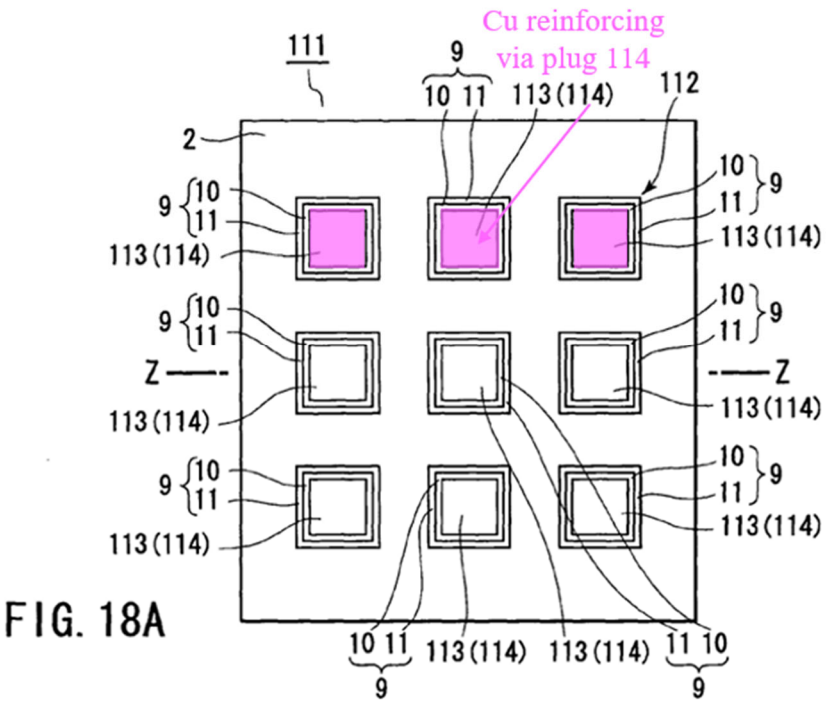
a) [24.a] – "*semiconductor device of claim 1, wherein a planar shape of the via is substantially a square*"

434. Element [24.a] recites the "semiconductor device of claim 1, wherein a planar shape of the via is substantially a square," which Hasunuma in view of Iizuka renders obvious.

435. In confirmation of what was well-known to a POSITA at the time, Iizuka expressly teaches that vias can have a square cross-sectional shape. TSMC-1008, 9:45-47 ("the opening of the via-hole may have any configuration, such as **a square**, rectangle or circle.").

436. It was obvious to a POSITA to implement Hasunuma's vias (i.e., conductive plugs 27) with this common square shape, as taught by Iizuka.

437. For the same reasons discussed for Claims 19-20 in the preceding section, choosing square-shaped vias was a simple design choice, and indeed, Hasunuma itself discloses square vias in some plan-view figures, such as in Figure 18A, indicating that square vias were a known design option (TSMC-1005, Fig. 18A):



438. Thus, given Hasunuma's clear disclosure of square-shaped vias in Figure 18A and the common usage at the time of square-shaped vias, a POSITA would have understood Hasunuma to disclose substantially square-shaped vias as an option for any of the vias or dummy via in any of its embodiments.

439. Additionally, in view of Iizuka's express teaching square vias, it was obvious in view of both Hasunuma's and Iizuka's disclosures of square vias and the knowledge of a POSITA at the time to make both the planar shape of the vias and the dummy vias in Hasunuma's various embodiments substantially square.

440. A POSITA would have recognized that it would have been nothing more than a simple substitution to adopt Iizuka's specific via/dummy via shapes. For example, choosing specific shapes (e.g., square) as taught by Iizuka would amount to simple and routine design choices chosen to meet particular layout or process requirements within Hasunuma's framework.

441. In addition, via shapes, such as square or circular, each provide potential known advantages applicable to a given situation. For example, in the case of square-shaped vias, such vias align more efficiently with orthogonal interconnect lines, leading to a more compact layout and better utilization of area compared to circular vias in such scenarios to achieve increased contact area with interconnects above and below the via. *See, e.g.*, TSMC-1014, ¶[0092], Figs. 8, 14 (teaching square vias as preferred for certain interconnect junctions); TSMC-1039, 5:27-32

(noting the increased electrical contact area achieved by square vias). A POSITA would have recognized that the fundamental mechanical strength enhancing function of Hasunuma's dummy vias (as well as the electrical-connection function of Hasunuma's active vias), would be achieved with vias having square cross-sections.

442. Further, because a POSITA was aware of the basic available via shapes, and was aware of the role of the dummy vias in providing a mechanical strengthening function as well as reducing stress-induced voiding and electromigration problems as taught, for example, by Watanabe, it would have been a matter of routine optimization to choose the via shape that works best for a given overall design. With a few basic shapes to choose from (e.g., circular, square, rectangular), it would not have required an undue amount of experimentation to arrive at the optimal via shape.

443. A POSITA would have had a reasonable expectation of success in implementing Hasunuma's vias (both functional and dummy) with a square cross-sectional shape, as this would easily be accomplished using the standard patterning and fabrication techniques used to make the interconnect structure in general. Certainly it was well known how to pattern via holes having square cross-sections using masks, photolithography, and etching, and such square patterns subsequently result in square vias when conductive material is deposited into the patterned vias

holes. TSMC-1004, Figs. 2, 4, 5, 9; TSMC-1005, Fig. 18A; TSMC-1014, ¶[0092], Figs. 8, 14; TSMC-1039, 5:27-32.

b) [24.b] – "*a side of the via is substantially equal to a width of the first interconnect*"

444. Element [24.b] calls for "a side of the via is substantially equal to a width of the first interconnect," which Hasunuma in view of Iizuka renders obvious.

445. Hasunuma teaches vias (conductive via plug 27) having a dimension of "about 0.13 μm," and in the same paragraph, teaches that wiring layer 13 (which includes the first interconnect (conductive layer 14)) also has a width of "about 0.13 μm." TSMC-1005, ¶[0127], Fig. 8. Thus, Hasunuma teaches that the via has a dimension equal to a width of the first interconnect. *Id*.

446. A POSITA, implementing the square via shape for the conductive via plug 27 in Hasunuma as expressly taught by Iizuka as well as shown in Hasunuma's Figure 18A, would have found it obvious to utilize a square via having a side dimension equal to the width of the first interconnect, especially given that Hasunuma expressly taught equal sizes for its via (conductive via plug 27) and first interconnect (conductive layer 14 in wiring layer 13). *Id*., ¶[0127]. Furthermore, it was common practice (and indeed a standard design practice at the time) to design vias with the same width as the underlying "first" interconnect. *See, e.g*., TSMC-1004, Figs. 2, 4, 9 (disclosing square vias having the same side dimension as the

underlying interconnect). This ensures that the vias make robust, full-width contact for good electrical connection with the underlying interconnect. Indeed, a POSITA recognized that by making the via the same width as the underlying interconnect, the designer maximizes the available contact area/interface between the via and interconnect. A POSITA therefore would have found it obvious to apply this standard design practice to Hasunuma's vias and underlying interconnect, including when used with square vias. It would have been at most routine optimization for a POSITA to determine the beneficial shape (e.g., square) and relative sizes (e.g., square side dimensions) of the vias and interconnect. *Id*.; *see also* TSMC-1002, 244-45, 292-96.

447. A POSITA would have had a high expectation of success in achieving such a dimensionally matched connection, as this represents a routine design consideration for reliable via-to-line interconnections. A POSITA would simply have designated the vias to have the same size as the underlying interconnect line, and the standard manufacturing process (including the same processes already disclosed in Hasunuma) would then build them as such.

N. Ground 13: Claims 29 and 30 Are Obvious Over Hasunuma and Nasu

448. Hasunuma discloses claim 1 as discussed *supra* §X.I.1, from which claims 29-30 depend. Hasunuma and Nasu render claims 29 and 30 obvious as detailed below.

1. Claim 29

a) [29.a] – "*semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view*"

449. Element [29.a] recites the "semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view," which Hasunuma in view of Nasu renders obvious.

450. Hasunuma discloses circular-shaped vias. *Supra*, §X.I.2.(a). Specifically, Hasunuma discloses vias (e.g. conductive via plug 27) and dummy vias (e.g. reinforcing via plugs 28) having circular cross sections, such as by providing an example in which they have a "diameter" of 0.13 μm. TSMC-1005, ¶[0127].

451. Nasu also consistently refers to the "diameter" of its via openings, which is the standard dimensional term for circular features. TSMC-1032, ¶[0023]. The vias formed within circular via openings will likewise be circular in their planar shape. *Id*.

452. Moreover, the choice of via shape is a mere design choice, with circular via shapes being well-known as illustrated by Iizuka. *See, e.g*., TSMC-1008, 9:44-

47 ("[T]he opening of the via-hole may have any configuration, such as a square, rectangle or **circle**."). Circular-shaped vias were also easier to process. TSMC-1038, 7:62-67. Accordingly, it was obvious to implement Hasunuma's vias and dummy vias with a circular planar shape, and this was easily accomplished using standard manufacturing techniques, so a POSITA would have had a high expectation of success.

b) [29.b] – "*a diameter of the dummy via is smaller than a diameter of the via*"

453. Element [29.b] calls for "a diameter of the dummy via is smaller than a diameter of the via," which Hasunuma in view of Nasu renders obvious.

454. Nasu teaches dummy hole pattern 8 having smaller diameters than the diameter of the via hole pattern 9. TSMC-1032, ¶¶[0024], [0028]. As explained previously, this leads to dummy vias having a smaller diameter than the active via. *Supra*, §X.F.1.(b).

455. A POSITA would have been motivated to apply Nasu's teaching of using circular, smaller-diameter dummy vias compared to the functional vias to enhance the reliability of multilayer interconnect structures, as further explained *infra*, §X.N.3.

456. Fabricating vias of different, controlled sizes in the same device was a known capability as demonstrated by Nasu, as was fabricating circular vias/dummy

vias as seen in both Hasunuma and Nasu, leading to a high expectation of success in implementing such a combination to arrive at claim 29.

2. Claim 30

a) [30.a] – "*semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square*"

457. Element [30.a] recites the "semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square," which Hasunuma in view of Nasu renders obvious.

458. Hasunuma discloses square vias/dummy vias in some plan-view figures, such as annotated Figure 18A, indicating that square vias were a known design option (TSMC-1005, Fig. 18A):

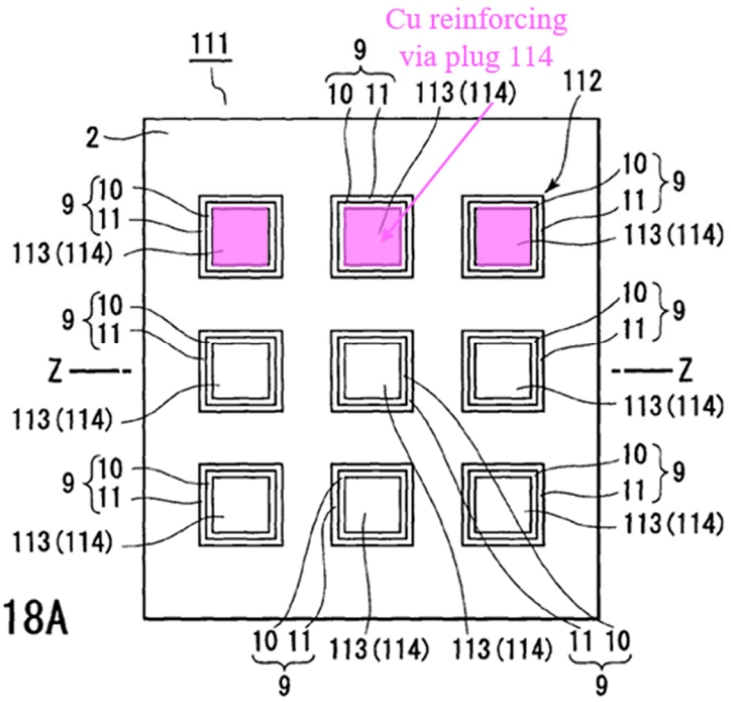


FIG. 18A

459. As previously discussed, Nasu also discloses square via holes and square dummy holes 10:

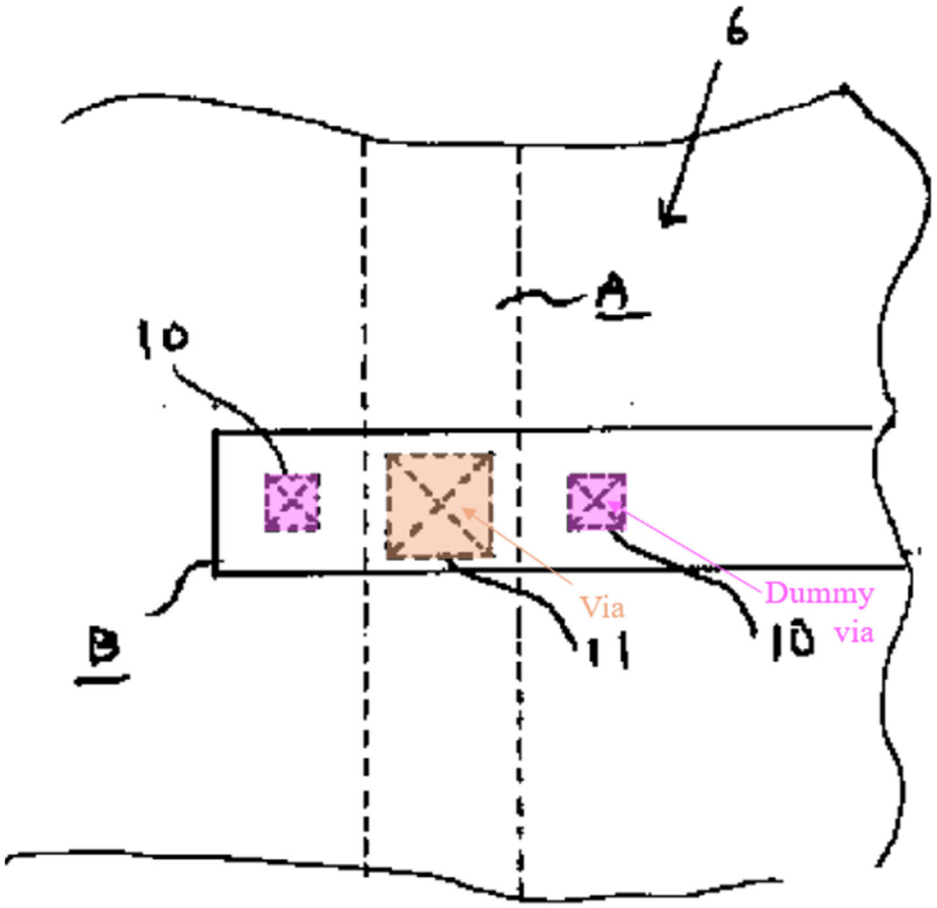


FIG. 6

TSMC-1032, ¶¶[0024], [0028], Fig. 6.

460. Square vias/dummy vias were well-known in the art, and were beneficial for increasing the contact area between the via/dummy via and the interconnect above and/or below the via/dummy via. *See, e.g.,* TSMC-1008, 9:45-47; TSMC-1039, 5:27-32.

461. In view of the above, it would have been obvious to a POSITA to implement Hasunuma's via (e.g. conductive via plug 27) and dummy vias (e.g. reinforcing via plugs 28) with a planar shape that is substantially a square. *See also*

supra, §§X.C.1-2, X.K.1.(a), X.L.1-3. The choice of via shape is a mere design choice, with square via shapes being well-known. *Id*.; TSMC-1004, Figs. 2, 4, 5, 9; TSMC-1008, 9:45-47; TSMC-1014, ¶[0092], Figs. 8, 14. A POSITA would also have had a high expectation of success in using a square via because it was a known substitution option and was known to work.

b) [30.b] – "*a side of the dummy via is smaller than a side of the via*"

462. Element [30.b] calls for "a side of the dummy via is smaller than a side of the via," which Hasunuma in view of Nasu renders obvious.

463. As previously discussed, Nasu teaches making the dummy vias smaller than the functional vias, with dummy holes 10 having a smaller side dimension than via hole 11:

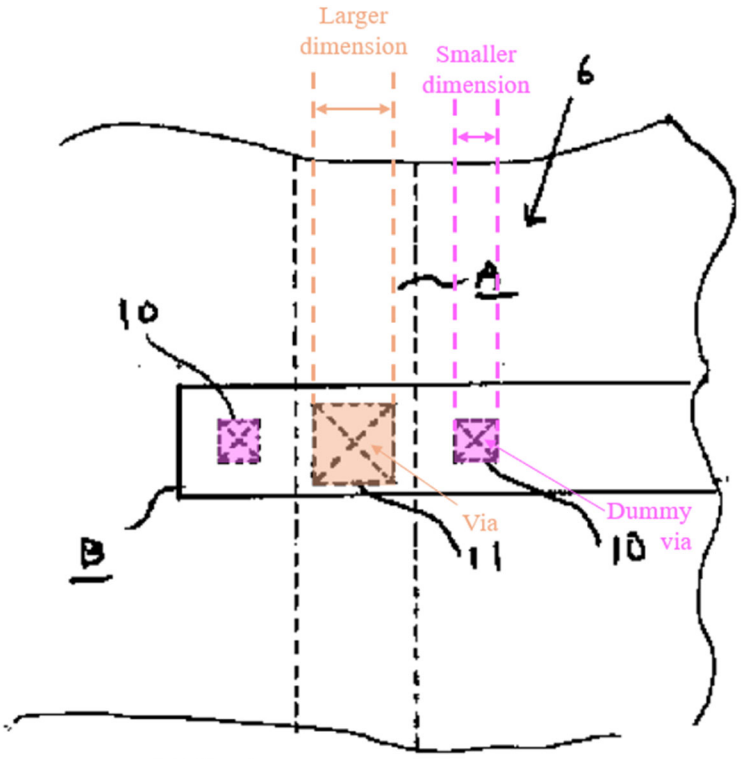


FIG. 6

TSMC-1032, ¶¶[0024], [0028], Fig. 6

464. It was obvious to implement into Hasunuma square vias and dummy vias, with the dummy vias having a smaller side dimension than the vias, as taught by Nasu, as further discussed *infra*, §X.M.3.

3. Combining Hasunuma and Nasu

465. Whether implemented with circle or square shapes, a POSITA would have been motivated to combine the teachings of Nasu with Hasunuma to enhance the reliability of Hasunuma's multilayer interconnect structures. Both references address reliability issues by incorporating dummy via structures near functional vias. *Supra*, §§IX.B, IX.E. Specifically, Hasunuma addresses reliability problems arising

from stresses inherent in interconnect structures by incorporating non-functional, concurrently formed reinforcing plugs 28, which are dummy vias. TSMC-1005, ¶¶[0079]-[0086], [0103], [0108]-[0109], [0113]-[0114], [0121]-[0125], Figs. 8-9.

466. Nasu likewise specifically teaches forming dummy vias, but with smaller sizes than the functional vias. TSMC-1032, ¶¶[0022]-[0028], Figs. 1-6. Nasu explains that a smaller dimension for the dummy via hole, results in shallower dummy features when the holes for the vias and dummy vias are simultaneously etched, allowing the dummy vias to not reach the lower wiring while still serving as "material reservoirs" to assist in preventing electromigration (*id*.), a problem expressly recognized in the art (*see, e.g*., TSMC-1004, ¶[0077]).

467. A POSITA would have been motivated to implement Nasu's smaller-sized dummy vias (whether having circular or square cross sections) in Hasunuma's structure because Nasu's teachings help optimize dummy via layout density. Specifically, forming dummy vias having a shallower depth than the functional vias allows dummy vias to be formed in areas over lower-level interconnects that cannot be electrically connected to the upper-level interconnect from which the dummy vias depend. For example, Hasunuma's Figure 14 shows additional first-level interconnects 14 below the second interconnect (conductive film 26). Making Hasunuma's reinforcing plugs 28 shorter/less deep would allow them to be placed

over these first level interconnects without forming an undesired electrical connection between these first level interconnects and the second level interconnect. Indeed, Hasunuma's Figures 8 and 14 show a desire to include many dummy vias, and implementing Nasu's teachings further promotes this goal by allowing dummy vias to also be placed where they otherwise could not be due to underlying interconnects.

468. Furthermore, while active vias are typically sized to match the width of the underlying interconnect (*infra*, §X.L.1.(b)), and must meet a minimum threshold size to carry sufficient current for device, dummy vias by definition carry no current, and thus are free to be made smaller than the active vias. A POSITA appreciated that via stress gradients increase inversely with via diameter. TSMC-1036, 319 (nothing that "the stress gradient across the bottom of the via is roughly doubled as via dimension is halved," and "the stress gradient will scale inverse to the via size").

469. A POSITA thus also appreciated that vias/dummy vias with a smaller diameter have a higher stress gradient, which was known to attract more vacancies migrating in the interconnect, since vacancies tend to travel to areas of high stress. *Id*., 315 ("[T]he stress gradient region [] is where a significant driving force exists to compel vacancies to migrate towards a specific voiding site."). Indeed, the prior art specifically reports using dummy vias to attract vacancies (*e.g*., TSMC-1009, ¶¶[0017], [0085]-[0088]), and studies have confirmed that smaller vias attract more

vacancies, particularly in regard to a fixed interconnect size (TSMC-1037, 163, 165, Figs. 8, 14 (noting the increasing via failure rate due to stress-induced voiding (i.e., vacancy accumulation) as vias size decreases)).

470. Accordingly, a POSITA would have appreciated that Nasu's approach of using smaller-sized dummy vias (compared to the active vias) has the added benefit of better attracting and sequestering vacancies so that they do not reach/accumulate in active vias where void formation can be fatal to device operation. A POSITA was therefore motivated to implement Nasu's teachings to further refine the dummy via's role in managing material diffusion or local stress within Hasunuma's device by expanding the ability to create tailored reservoir-like structures that better attract vacancies and reduce void formation at active vias.

471. Fabricating vias/dummy vias of different, controlled sizes in the same device was a known capability as demonstrated by Nasu, leading to a high expectation of success in implementing such a combination. A POSITA would have had a high expectation of success in using a square via because it was a known substitution option and was known to work. While Nasu teaches both circular and square vias, choosing a basic via shape (circular vs. square) was a routine design parameter, and a POSITA considering the via shape would understand Nasu's teachings on relative sizing are applicable regardless of whether the via is circular or square.

O. Ground 14: Claims 33-38 Are Obvious Over Hasunuma and Kamoshima

472. Claims 33-38 are obvious over Hasunuma and Kamoshima, as outlined below.

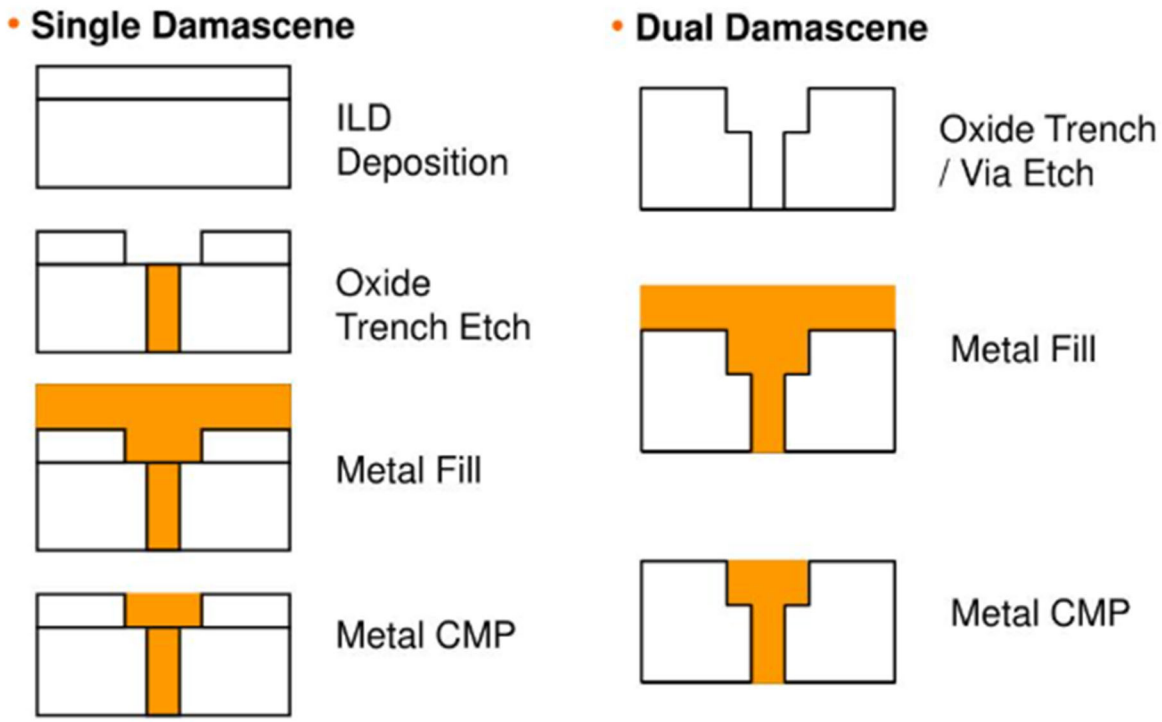
1. Dual Damascene Process and Structures

473. A "Damascene" process is a method for fabricating integrated circuit (IC) interconnects. TSMC-1004, ¶¶[0006]-[0011], Fig. 19; TSMC-1034, 671-72, Fig. 15-2. Unlike traditional "subtractive" methods where a metal layer is deposited and then etched to form the wiring, the Damascene technique inlays the metal into patterns that have already been etched into an insulating layer. *Id*. In the Damascene process, a film is deposited to fill recessed regions and is then polished back until the film is removed from the surface, leaving it only in the recesses. *Id*. Thus, after the metal (e.g., copper) and any necessary barrier layers are deposited to fill the trenches, the excess metal is removed from the top surface using Chemical Mechanical Polishing (CMP), leaving the metal lines embedded in the insulating material. *Id*.

474. A "Dual-Damascene" process extends the single-damascene concept by forming two features at once: the horizontal interconnect line (in a trench) and the vertical via connection to the level below. TSMC-1004, ¶¶[0012]-[0014], Fig. 20; TSMC-1034, 674-76. This is in contrast to a single-damascene process, which

would form only one of these features at a time. The dual-damascene approach, therefore, provides for the simultaneous filling of both the trench and the via with metal in a single deposition step. *Id*. This creates a monolithic, continuous metal structure comprising both the line and the via. TSMC-1004, Fig. 20; TSMC-1034, Fig. 15-3(d).

475. Schematically, the different structures resulting from the single and dual damascene processes can be illustrated as below:



As seen above, one characteristic of a dual-damascene structure is the continuous nature of the interconnect and associated via. TSMC-1004, ¶[0014], Fig. 20; TSMC-1034, 674-76, Fig. 15-3(d). Because the trench and via are filled in the same process step, the resulting copper interconnect is a single, seamless piece of metal typically

surrounded on its periphery by a barrier metal layer, which is a direct outcome of the manufacturing process. *Id*. The structure resulting from the dual damascene process is thus characterized by comprising continuous, monolithic metal structure (usually, and preferably, copper), meaning no barrier layer separates the interconnect line and the via because they are formed as one piece. *Id*.; *see also* TSMC-1012, 33. This is in contrast to copper structures formed by the single damascene process in which a layer of barrier metal separates the interconnects from the vias both above and below the interconnect.

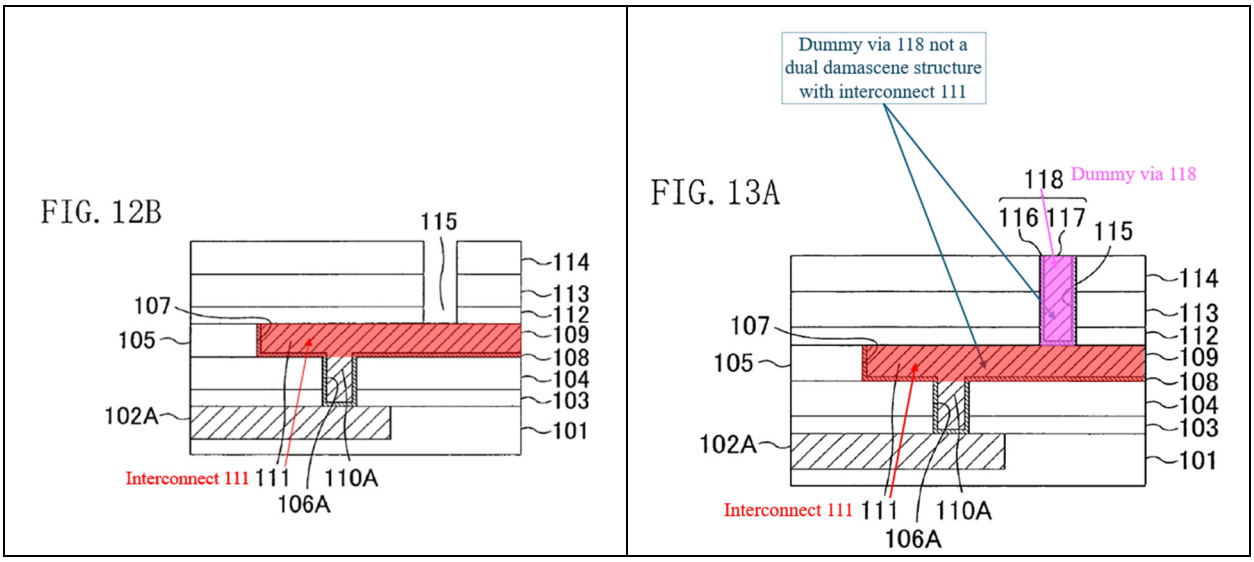
476. To my knowledge, a via connecting to a top surface of an interconnect line cannot be formed as a dual-damascene structure with the interconnect. Instead, the interconnect must be formed first, then covered with an insulating layer that is subsequently etched with openings that are then filled with metal to forms vias connected to the top surface of the interconnect. Because the metal filling steps for the interconnect and the via above it are not carried out simultaneously, and will typically be separated by a layer of barrier metal between them, such an interconnect and via would not be understood by a POISTA to form a dual damascene structure. TSMC-1004, ¶¶[0006]-[0014], Figs. 19-20; TSMC-1034, 671-77, Figs. 15-2, 15-3.

2. Lack of Written Description Support in the ’623 Patent

477. The ’623 patent lacks written description support for claim 33 and, thus, also for claims 34-38 that depend from claim 33. Claim 33 requires that the dummy

via is connected to the "upper surface"' of the second interconnect. Claim 33 depends from claim 1, and claim 1 requires that the "second interconnect and the dummy via from a dual damascene structure." The only embodiment in the '623 patent that shows a dummy via connected to the upper surface of a second interconnect is Embodiment 5 of Figure 13B, which is made according to the method shown in Figures 11A-11C, 12A-12C, and 13A. TSMC-1001, 22:27-24:6.

478. Embodiment 5, however, forms the dummy via 118 only after completing the formation of the second interconnect 111 and, thus, the second interconnect 111 and the dummy via 118 are not formed simultaneously and are separated by a layer of barrier metal layer 116 (*id*., 22:64-65). Thus, in this embodiment, the second interconnect and dummy via do not form a dual damascene structure, which is in direct conflict with claim 1's requirement. *Id*., 22:47-23:2, Figs. 12A-13B. The lack of a dual damascene structure/formation is understood from Figures 12B and 13A, which show the dummy via 118 made in a completely different step from the second interconnect 111, and separated from each other by barrier layer 116.



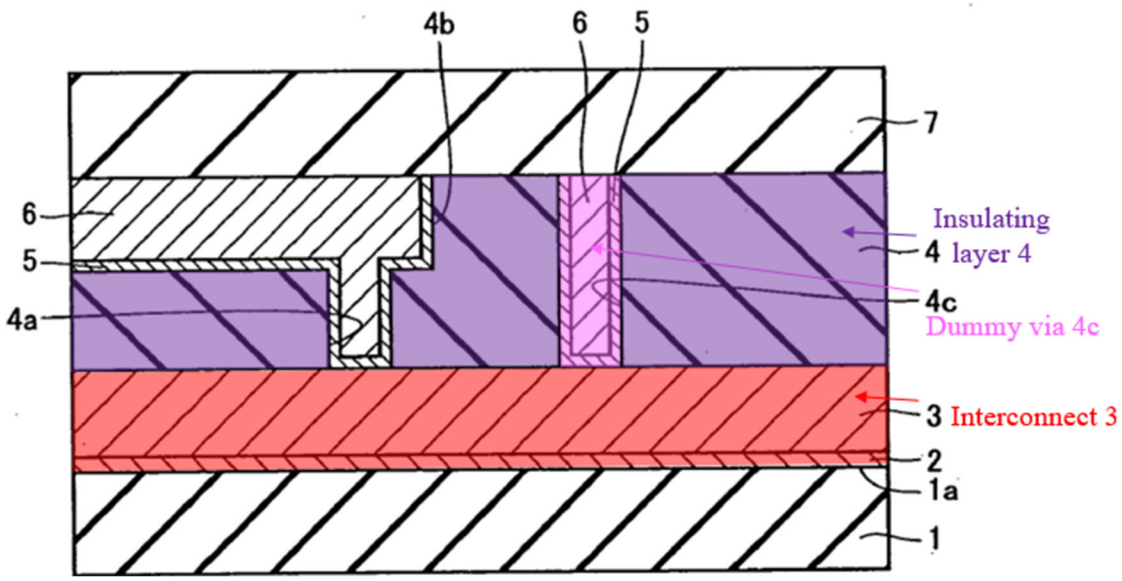
Id., 22:60-23:7, Figs. 12B, 13A. Consequently, the '623 patent specification fails to describe a device that satisfies both claim 1's dual-damascene limitation for the second interconnect and dummy via, and claim 33's requirement that the dummy via connect to the top surface of the second interconnect.

479. If claim 33 is interpreted as reading on Embodiment 5/Figure 13A in the '623 patent (despite the irreconcilable conflict between claims 1 and 33), then claims 33-38 are rendered obvious by Hasunuma and Kamoshima, as explained below.

3. Kamoshima

480. Kamoshima discloses dummy vias extending from the top surface of an interconnect, as seen in annotated Figure 16:

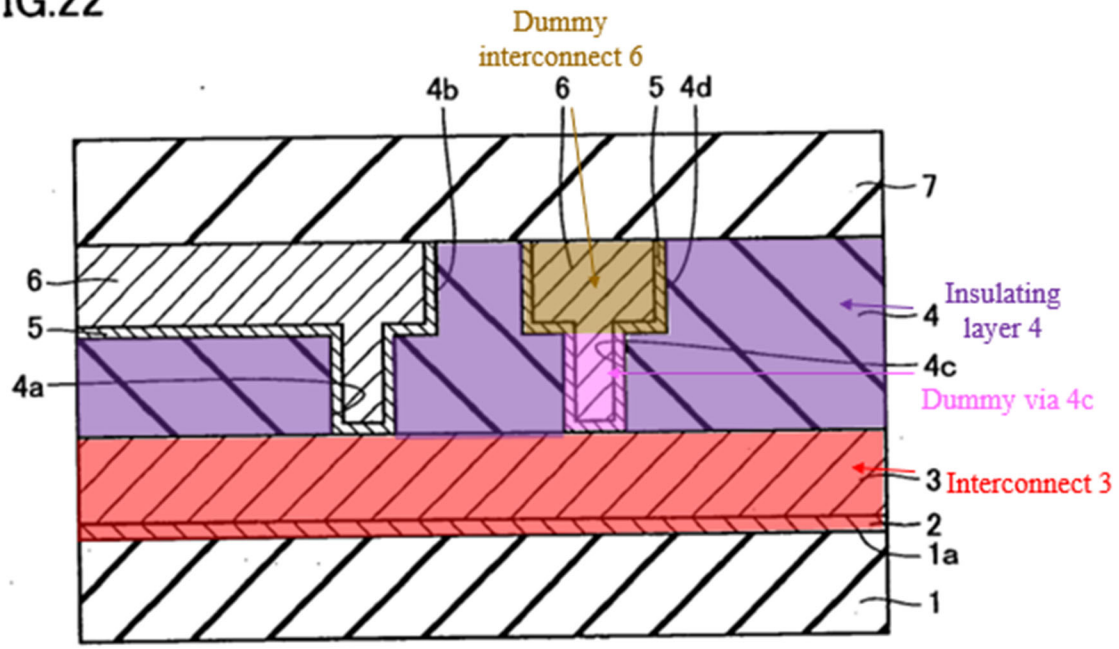
FIG.16



TSMC-1009, ¶¶[0085]-[0086], Fig. 16.

481. Kamoshima further discloses a dummy interconnect 6 on and in contact with the top of its upwardly-directed dummy via 4c, as seen in annotated Figure 22:

FIG.22



TSMC-1009, ¶¶[0090]-[0091], Fig. 22.

482. One goal Kamoshima sought to achieve with its dummy vias was to collect microvoids and prevent their concentration in/under active vias. *Id*., ¶¶[0017], [0088]. According to Kamoshima, the presence of dummy vias helps change the distribution of microvoids, the idea being that microvoids collected at the dummy via will not contribute to microvoid aggregation at active vias. *Id*.

4. Claim 33 – "*semiconductor device of claim 1, wherein the dummy via is connected to the upper surface of the second interconnect*"

483. Claim 33 recites the "semiconductor device of claim 1, wherein the dummy via is connected to the upper surface of the second interconnect," which Hasunuma and Kamoshima render obvious.

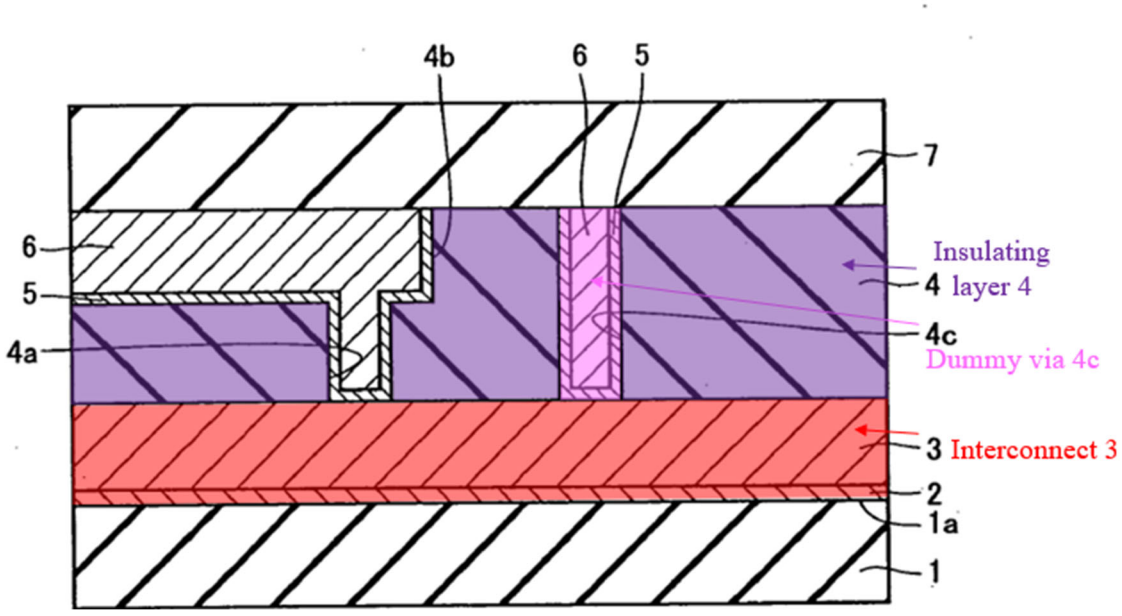
484. As previously established at *supra* §X.I.1, Hasunuma discloses all elements of claim 1.

485. In Hasunuma's Figure 8, the dummy via (reinforcing plug 28) is connected to a bottom surface of the second interconnect (conductive layer 26). TSMC-1005, Fig. 8. However, Hasunuma also discloses additional options for all embodiments that "can appropriately be combined, used, or carried out." *Id*., ¶[0290]. One of these is for "the reinforcing plug to be connected to the upper

surface of the conductive layer or the reinforcing metal layer may separately be provided so as to be connected to the reinforcing material provided above." *Id.*, ¶[0291] (emphasis added). In other words, Hasunuma teaches an alternative where the reinforcing plug (dummy via) extends from the upper surface of the interconnect, such as Hasunuma's conductive layer 26, which satisfies the limitation of claim 33 (if interpreted as reading on Embodiment 5/Figure 13A in the '623 patent). *Id.*, ¶¶[0290]-[0291], Fig. 8.

486. Kamoshima likewise discloses dummy via 4c from a top surface of interconnection layer 3:

FIG.16



TSMC-1009, ¶¶[0017], [0085]-[0088], Fig. 16. Kamoshima includes such dummy vias for the express purpose of helping to collect microvoids from the interconnect,

and thereby prevent them from aggregating at or under an active via and thereby disrupt the operation of the active via. *Id*., ¶¶[0017], [0088], [0092].

487. Thus, Hasunuma teaches to have the reinforcing plug (dummy via) on the upper surface of the second interconnect (conductive layer 26), and Kamoshima teaches how to make a dummy via (e.g. dummy via 4c) extending from an interconnect's top surface, as well as providing an additional motivation for such a structure, so a POSITA would have had a high expectation of success in making a dummy via extending from an interconnect's top surface. It would have been obvious to a POSITA to implement Hasunuma's teaching from paragraph [0291], per Kamoshima's additional disclosure, to so modify Hasunuma's Figure 8 embodiment:

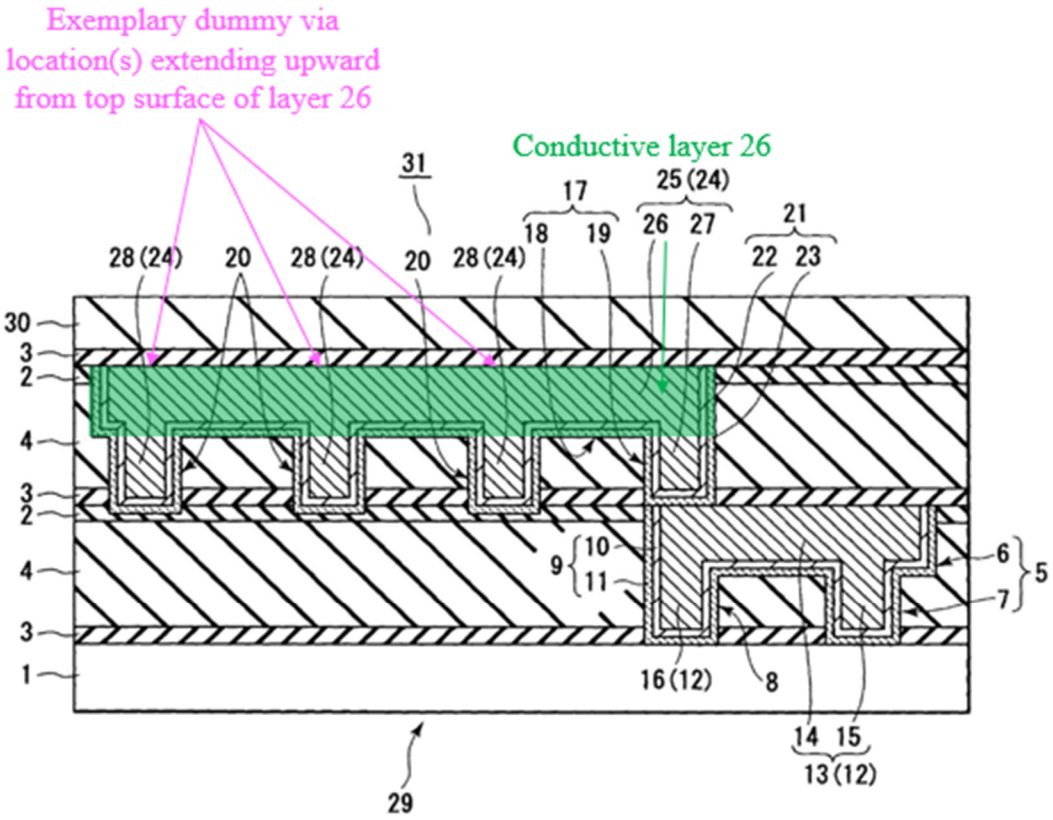


FIG. 8

TSMC-1005, Fig. 8; *see infra*, §X.O.10.

5. Claim 34 – "*semiconductor device of claim 33, wherein the dummy via is formed in a third insulating film formed on the second interconnect*"

488. Claim 34 recites the "semiconductor device of claim 33, wherein the dummy via is formed in a third insulating film formed on the second interconnect," which Hasunuma and Kamoshima render obvious.

489. Hasunuma discloses that a third insulating film (e.g., film 3) is formed on top of conductive layer 26. TSMC-1005, ¶[0111], Fig. 8. Hasunuma also

explains that the number of layers in the embodiment of Figure 8 is not limited, and that more layers may be stacked on top. *Id.*, ¶¶[0297]-[0298]. When building additional interconnect and via layers on top of the Figure 8 embodiment, another low relative dielectric constant film 4 and another insulating film 2 would be stacked on top of the topmost insulating film 3 to form a "third insulating film" on top of the second interconnect as indicated below, because those films 3, 4, and 2 are provided for each interconnect/via layer:

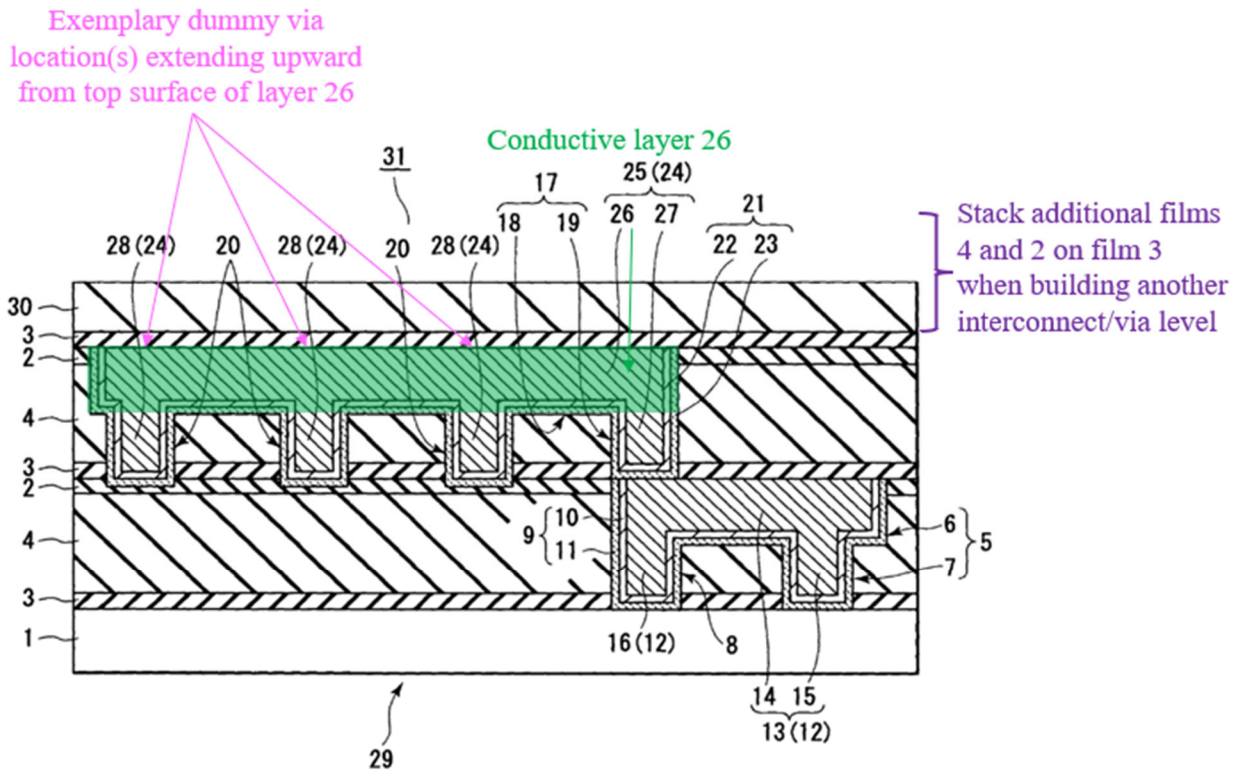


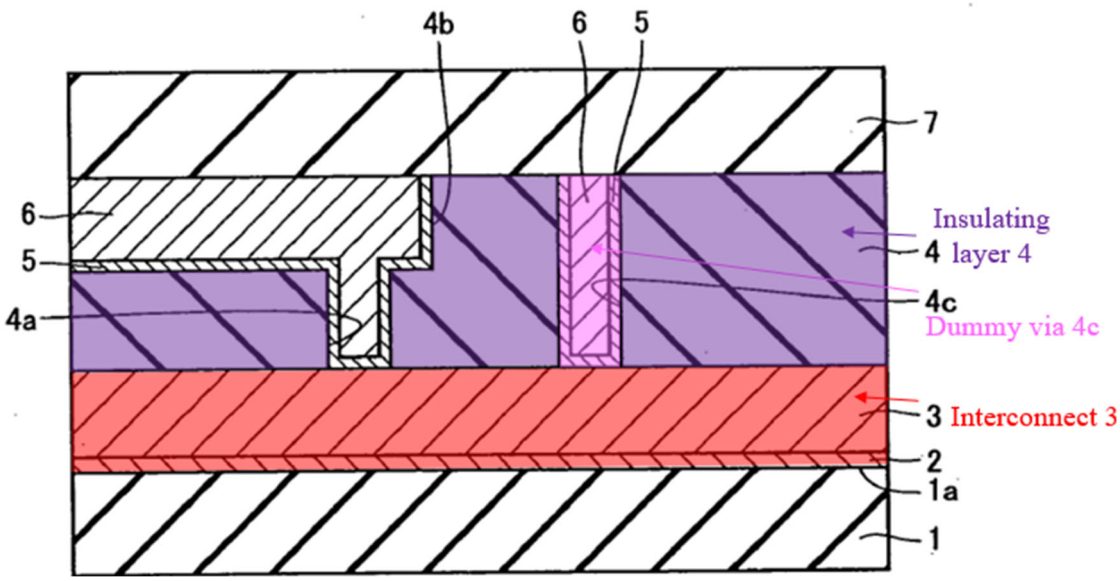
FIG. 8

Id., Fig. 8. The addition of such insulating films is just the natural result of adding another layer to the top of Hasunuma's device shown in Figure 8, as Hasunuma says

can be done. *Id*., ¶¶[0297]-[0298]. Indeed, some interconnect structures have as many as six or more interconnect layers, which will always be separated from each other by (and built on top of) an insulating layer. *Supra*, §VI.A.

490. Dummy vias (reinforcing plugs) extending upward from the second interconnect (conductive layer 26) surface would be formed in the additional 3-4-2 insulating film stack added onto conductive layer 26, such that the resulting dummy via will be formed in a "third insulating film" on the second interconnect. Such a "third insulating film" is a necessary part of building another dummy via on top of the second interconnect. This arrangement is analogous to Kamoshima's formation of dummy via 4c in insulating layer 4, which is formed on interconnection layer 3, as seen below:

FIG.16



TSMC-1009, Fig. 16.

491. Thus, when a dummy via is connected to and extends upward from the upper surface of a second interconnect, such as Hasunuma's conductive layer 26, it would have been at least obvious (and I would argue, necessary) for the dummy via to be formed in a third insulating film formed on the second interconnect, in the same way that Kamoshima's dummy via 4c is built into insulating layer 4 residing on interconnect 3. Kamoshima shows how to make the dummy via 4c built into insulating layer 4 residing on interconnect 3, so a POSITA would have had a high expectation of success in adding the insulating film to the device of Hasunuma.

6. Claim 35 – "*semiconductor device of claim 34, wherein the third insulating film has a multilayer structure including a SiN film and a SiO_2 film*"

492. Claim 35 recites the "semiconductor device of claim 34, wherein the third insulating film has a multilayer structure including a SiN film and a SiO_2 film," which Hasunuma and Kamoshima render obvious.

493. As noted for claim 34 above, when adding additional levels to Hasunuma's Figure 8 embodiment, another film 4 and film 2 would be stacked on top of the topmost film 3 seen in Figure 8. Thus, the third insulating film would have a multilayer structure of films 3-4-2.

494. Hasunuma explains that film 3 can be a SiN film, and that film 2 can be a SiO_2 film. TSMC-1005, ¶¶[0293], [0299]. Thus, Hasunuma teaches that the multilayer insulating film structure including films 2 and 3 can be formed with a SiN film and a SiO_2 film. *Id*. It would have been obvious for a POSITA to use these materials because Hasunuma explicitly lists them as materials that can be used for those films 2 and 3 (as part of the repeating 3-4-2 film structure), and they are commonly used in interconnect structures, so a POSITA would have had a high expectation of success in using those materials. *Id*.

7. Claim 36 – "*semiconductor device of claim 33, wherein the dummy via includes a second barrier film and a second conductive film*"

495. Claim 36 recites the "semiconductor device of claim 33, wherein the dummy via includes a second barrier film and a second conductive film," which Hasunuma and Kamoshima render obvious.

496. Hasunuma forms its reinforcing plugs 28 (dummy vias) with barrier metal film 21 and a Cu film 24, which is conductive. TSMC-1005, ¶¶[0105]-[0108], Fig. 8. Likewise, Kamoshima's dummy plug 4c comprises barrier metal layer 5 and copper layer 6. TSMC-1009, ¶[0086], Fig. 16. Kamoshima's arrangement is identical to the barrier film liner and conductive film core disclosed for upwardly-extending dummy via 118 in Figure 13B of the '623 patent.

497. A POSITA would have therefore found it obvious for a dummy via extending from the top surface of Hasunuma's interconnect layer 26 (as discussed above for claim 33 and taught in paragraph [0291] of Hasunuma) to comprise a barrier film and a conductive film ("second barrier film" and "second conductive film"), just as with all of the other dummy vias in Hasunuma, and as seen in Kamoshima's Figure 16 for dummy via 4c. In addition to the express teachings of Hasunuma and Kamoshima to this effect, I also note that it is common when forming vias (or plugs) to use a barrier film combined with a conductive film—especially when the conductive film is the more preferrable conductor, copper— making this a common design choice and, therefore, a POSITA would have had a high expectation of success in using a barrier film combined with a conductive film. *See, e.g.*, TSMC-1004, ¶¶[0009], [0013]; TSMC-1012, 33; TSMC-1027, 25; TSMC-1034, 674-677.

8. Claim 37 – "*semiconductor device of claim 36, wherein the second conductive film includes copper*"

498. Claim 37 recites the "semiconductor device of claim 36, wherein the second conductive film includes copper," which Hasunuma and Kamoshima render obvious.

499. Both Hasunuma's and Kamoshima's dummy vias include copper. TSMC-1005, ¶¶[0105]-[0108], Fig. 8; TSMC-1009, ¶[0086], Figs. 1, 16. For example, reinforcing plugs 28 in Hasunuma include Cu film 24. TSMC-1005,

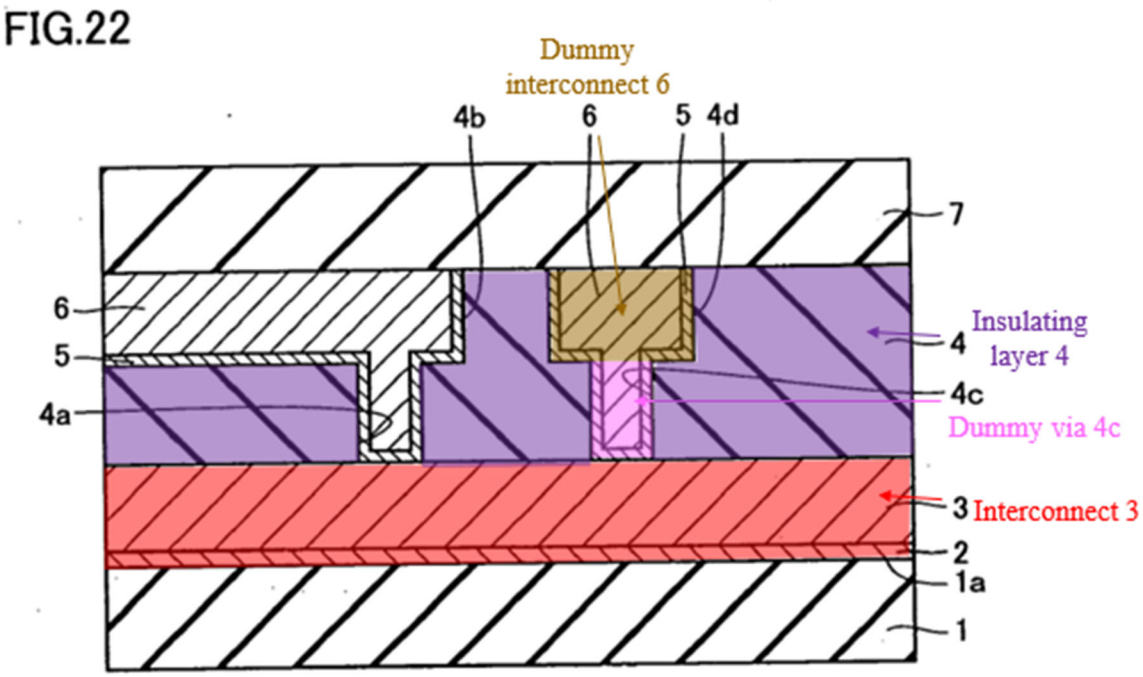
¶[0108], Fig. 8. A POSITA would have understood and found it obvious that Hasunuma's dummy via (reinforcing plug) would include copper even when extending from the top surface of the interconnect (as discussed above for claim 33 and taught in paragraph [0291] of Hasunuma), and as taught by Kamoshima regarding its dummy via 4c. *See also supra*, §§VI.A, X.O.3. Both Hasunuma and Kamoshima show how to make dummy vias that include copper, so a POSITA would have had a high expectation of success in using copper for this purpose.

9. Claim 38 – "*semiconductor device of claim 33, wherein a second dummy interconnect is provided on the dummy via so as to come in contact with a top of the dummy via*"

500. Claim 38 recites the "semiconductor device of claim 33, wherein a second dummy interconnect is provided on the dummy via so as to come in contact with a top of the dummy via," which Hasunuma and Kamoshima render obvious.

501. Hasunuma teaches that "the reinforcing plug to be connected to the upper surface of the conductive layer … may separately be provided so as to be connected to the reinforcing material provided above." TSMC-1005, ¶[0291] (emphasis added). Thus, Hasunuma expressly teaches that the reinforcing plug (dummy via) is connected at its top end to a second dummy interconnect (reinforcing material provided above).

502. Kamoshima also teaches such a structure with a dummy interconnect (dummy interconnection layer 6) on top of its upward-extending dummy via 4c, as illustrated in annotated Figure 22 below:



TSMC-1009, ¶[0090] (noting that "dummy interconnection layer 6 does not electrically connect interconnection layer 3 to another element"), Fig. 22; *see also id.*, Figs 1-8.

503. Thus, both Hasunuma and Kamoshima teach the added limitation of claim 38, and its implementation into Hasunuma's Figure 8 embodiment was obvious to a POSITA given Kamoshima's express illustration of such a structure. The dummy interconnect, such as that shown above in Kamoshima's Figure 22, would simply be manufactured as part of the interconnect structure already being

built at that level, and would have required nothing more than a pattern modification to build as part of the standard manufacturing process, so a POSITA would have had a high expectation of success in manufacturing the dummy interconnect.

10. Combination of Hasunuma with Kamoshima

504. A POSITA would have been motivated to add a reinforcing plug (dummy via) to the top surface of Hasunuma's conductive layer 26 in order to achieve more symmetrical reinforcement and stress distribution in the structure. Hasunuma's reinforcing plugs 28 shown in Figure 8 anchor the conductive layer 26 downwards to the film 2 below. TSMC-1005, Fig. 8. A POSITA would have appreciated that adding one or more reinforcing plugs extending upwards into the third insulating film, and including attachment to a reinforcing metal layer (i.e., dummy interconnect) above when present, would clamp the conductive layer 26 between two mechanically strong layers. *Id*.; *see also* TSMC-1011, 8:35-54.

505. In addition, as taught by Kamoshima, dummy vias attached to the top surface of a given interconnect help protect against microvoid aggregation under an adjacent active/functional via (i.e., a via that is needed for device operation). TSMC-1009, ¶¶[0017], [0085]-[0088]. For example, when another level of vias and interconnects are added on top of Hasunuma's Figure 8 embodiment (TSMC-1005, ¶¶[0291], [0297]-[0298]), Hasunuma's interconnect layer 26 will have one or more active vias connecting it to the interconnect level above. Placing dummy vias

extending upward from the top surface of interconnect layer 26 will thus achieve Kamoshima's stated benefit of reducing the concentration of voids under such active vias, including when a dummy interconnect is in contact with the top of the dummy via, as shown in Kamoshima's Figure 22. TSMC-1009, ¶¶[0085]-[0092].

506. A POSITA would also have appreciated that incorporating Kamoshima's dummy interconnect, as seen in its Figure 22, into Hasunuma's structure would have had the added benefit of better and more uniform CMP processing. *Supra*, §VI.B; *see also* TSMC-1004, ¶¶[0029], [0145]-[0146] (explaining the benefits of incorporating dummy wiring to improve CMP planarization).

507. A POSITA would have had a high expectation of success in implementing dummy vias connected top surface of the conductive layer as taught in Hasunuma (along with dummy interconnects on top of the dummy vias, when desired) given Hasunuma's express disclosure of such structures (TSMC-1005, ¶[0291]) and given Kamoshima's teachings and figures showing how to make such structures using standard fabrication processing steps. Hasunuma explains that the number of layers in the Figure 8 embodiment is not limited, and that more layers may be stacked on top. *Id*., ¶¶[0297]-[0298]. Adding such structures into Hasunuma's device would have involved nothing more than adjustments to the

masking patterns such that the dummy vias and dummy interconnects get built simultaneously with the corresponding active vias and interconnects.

XI. CONCLUSION

508. As discussed above, it is my opinion that the Challenged Claims of the ’623 patent are unpatentable because they are anticipated by the prior art, because they would have been obvious to a person of ordinary skill in view of the prior art, or both.

509. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

510. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

511. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false

statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 24th day of July, 2025, in Stanford, CA.



By: _____

Dr. Reinhold H. Dauskardt

Appendix A

Exhibit No.	Description
1001	U.S. Patent No. 7,439,623
1002	File History of U.S. Patent No. 7,439,623 ("the '623 File History")
1003	Declaration of Dr. Reinhold Dauskardt
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. ("Watanabe")
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. ("Hasunuma")
1006	Reserved
1007	U.S. Patent No. 6,717,267 to Kunikiyo ("Kunikiyo")
1008	U.S. Patent No. 5,250,465 to Iizuka et al. ("Iizuka")
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. ("Kamoshima")
1010	JP2002299437 ("Fukazawa") and Certified Translation of Fukazawa with Certification of Translation
1011	U.S. Patent No. 7,042,099 to Kurashima ("Kurashima")
1012	P. Andricacos, "Copper On-Chip Interconnections," *Interface, The Electrochemical Society*, pp. 32-37, 1999
1013	U.S. Patent No. 5,885,857 to Yamaha et al. ("Yamaha")
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi *et al*. ("Igarashi")

Exhibit No.	Description
1015	U.S. Patent No. 6,717,268 to Hau-Riege ("Hau-Riege")
1016	U.S. Patent No. 6,468,894 to Yang ("Yang")
1017	U.S. Patent No. 6,022,808 to Nogami ("Nogami")
1018	AICP'S P.R. 3-1 Disclosure of Asserted Claims and Infringement Contentions and P.R. 3-2 Document Production Against TSMC (cover document only)
1019	Kaanta et al., "Dual Damascene: A ULSI Wiring Technology," *VMIC Conference*, IEEE, Jun. 11-12, 1991, pp. 144-152
1020	U.S. Patent No. 5,032,890 to Ushiku ("Ushiku")
1021	Reserved
1022	Reserved
1023	Reserved
1024	U.S. Patent No. 6,156,660 to Liu et al. ("Liu")
1025	U.S. Patent No. 5,798,298 to Yang ("Yang 2")
1026	T. I. Bao *et al*., "90 nm Generation Cu/CVD Low-k (k < 2.5) Interconnect Technology," *Digest. International Electron Devices Meeting*, San Francisco, CA, USA, 2002, pp. 583-586
1027	A. Loke, "Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects," Dissertation, Stanford University (1999)
1028	K.N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *Applied Physics Review* –

Exhibit No.	Description
	Focused Review, *Journal of Applied Physics*, Vol. 94, No. 9 (November 1, 2003), pp. 5451-5473
1029	T. C. Huang, *et al*., "Numerical Modeling and Characterization of the Stress Migration Behaviour Upon Various 90 nanometer Cu/Low k Interconnects," *Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)*, Burlingame, CA, USA, 2003 (added to IEEE Xplore 8-11-2003), pp. 207-209
1030	JPH10214893 to Fujii ("Fujii") and Certified Translation of Fujii with Certification of Translation
1031	Reserved
1032	JP2000012688 to Nasu ("Nasu") and Certified Translation of Nasu with Certification of Translation
1033	U.S. Patent Publication No. 2001/0030365 to Otsuka et al. ("Otsuka")
1034	Wolf, Stanley, *Silicon Processing for the VLSI Era: Deep-Submicron Process Technology*, Lattice Press, 2002 (excerpted) ("Wolf")
1035	Reserved
1036	E.T. Ogawa et al., "Stress-Induced Voiding Under Vias Connected To Wide Cu Metal Leads," IEEE 02CH37320, *40th Annual International Reliability Physics Symposium*, Dallas, Texas, 2002, pp. 312-21
1037	A. von Glasow et al., "Geometrical Aspects of Stress-Induced Voiding in Copper Interconnects," *Proceedings of the Advanced Metallization Conference 2002* (AMC 2002), San Diego, CA, October 1-3, 2002, Tokyo, Japan, October 29-30, 2002, Materials Research Society, pp. 161-67

Exhibit No.	Description
1038	U.S. Patent No. 6,215,189 to Toyoda et al. (“Toyoda”)
1039	U.S. Patent No. 6,238,850 to Bula et al. (“Bula”)

Appendix B

Claim Element	Claim Language
[1.pre][10]	A semiconductor device comprising:
[1.a]	a semiconductor substrate;
[1.b]	a first interconnect formed on the semiconductor substrate;
[1.c]	a first insulating film formed on the first interconnect;
[1.d]	a second interconnect formed on the first insulating film;
[1.e]	a via formed through the first insulating film and connecting between the first and second interconnects; and
[1.f]	a dummy via connected to the second interconnect,
[1.g]	wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough;
[1.h]	the second interconnect and the via form a dual damascene structure, and
[1.i]	the second interconnect and the dummy via from a dual damascene structure.
[2.a]	The semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,
[2.b]	wherein the first interconnect is formed on the second insulating film, and

[10] Claims 1, 2, and 45 are listed for purposes of challenged claims.

[2.c]	the dummy via is connected to a first dummy interconnect formed on the second insulating film.
[5.a]	The semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view, and
[5.b]	a diameter of the dummy via is substantially equal to a width of the first dummy interconnect.
[6.a]	The semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square, and
[6.b]	a side of the dummy via is substantially equal to a width of the first dummy interconnect.
[10.a]	The semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square, and
[10.b]	a side of the dummy via is smaller than a width of the first dummy interconnect.
19	The semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square.
20	The semiconductor device of claim 19, wherein a length of a side of the via and a length of a side of the dummy via are substantially equal to each other.

[23.a]	The semiconductor device of claim 1, wherein the via is substantially circular in a plan view, and
[23.b]	a diameter of the via is substantially equal to a width of the first interconnect.
[24.a]	The semiconductor device of claim 1, wherein a planar shape of the via is substantially a square, and
[24.b]	a side of the via is substantially equal to a width of the first interconnect.
27	The semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width.
[29.a]	The semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view, and
[29.b]	a diameter of the dummy via is smaller than a diameter of the via.
[30.a]	The semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square, and
[30.b]	a side of the dummy via is smaller than a side of the via.

[31.a]	The semiconductor device of claim 1, wherein the dummy via is substantially rectangular in a plan view, and
[31.b]	a longer side of the dummy via in a plan view and a shorter side of the second interconnect are provided along a same direction.
33	The semiconductor device of claim 1, wherein the dummy via is connected to the upper surface of the second interconnect.
34	The semiconductor device of claim 33, wherein the dummy via is formed in a third insulating film formed on the second interconnect.
35	The semiconductor device of claim 34, wherein the third insulating film has a multilayer structure including a SiN film and a SiO_2 film.
36	The semiconductor device of claim 33, wherein the dummy via includes a second barrier film and a second conductive film.
37	The semiconductor device of claim 36, wherein the second conductive film includes copper.

38	The semiconductor device of claim 33, wherein a second dummy interconnect is provided on the dummy via so as to come in contact with a top of the dummy via.
41	The semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.
43	The semiconductor device of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via
[44.a]	The semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,
[44.b]	wherein the first interconnect is formed on the second insulating film, and
[44.c]	a bottom of the dummy via is located in the second insulating film.
[45.a]	The semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and
[45.b]	the via is connected to the second interconnect portion.

[48.a]	The semiconductor device of claim 45, wherein the dummy via is substantially rectangular in a plan view, and
[48.b]	a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction.

Appendix C

Reinhold H. Dauskardt, Ph.D.

email: dauskardt@stanford.edu website: http://dauskardt.stanford.edu

Reinhold Dauskardt is the Ruth G. and William K. Bowes Professor in the Department of Materials Science and Engineering and has additional appointments as Professor in Mechanical Engineering, the Biodesign Institute and the Department of Surgery, Stanford School of Medicine. Dauskardt is a member of Stanford Bio-X, the Cardiovascular Institute, the Wu Tsai Human Performance Alliance, and the Wu Tsai Neurosciences Institute, and an affiliate of the Precourt Institute for Energy and the Stanford Woods Institute for the Environment. He is also a Visiting Professor in the School of Materials Science and Engineering at the Nanyang Technological University in Singapore.

The underlying theme of his research is to enable innovation and design of high-performance materials and devices by exploiting the fundamental connection between device materials, design, and processing and resulting device performance, function and reliability under use conditions.

Dauskardt and his group have worked extensively on integrating new nano and molecular materials into emerging technologies that include semiconductor, nanoscience and energy technologies, high-performance laminates, biomaterials and soft tissues.

He is an internationally recognized expert on the design and thermomechanial reliability of engineering structures, solar, battery and electronic device technologies for which he was awarded the prestigious Semiconductor Industry Association University Researcher Award in 2010 for “research which has provided substantive and sustained contributions to semiconductor industry science and technology." The Dauskardt Lab has a unique combination of internationally recognized materials and device processing capabilities, scalable manufacturing, reliability physics, high resolution characterization, accelerated testing and modeling capabilities. These capabilities include advanced sol-gel processing and open-air spray plasma deposition of semiconductor, solar and battery materials, along with accelerated testing and reliability modeling. He is also well known for his studies of the effects of semiconductor device and packaging processing operations and processing environments (including plasma processing, chemical mechanical planarization (CMP), and a wide range of deposition techniques) on device structures and their properties. Experimental studies are complimented with a range of multi-scale mechics and molecular computational modeling capabilities.

His research on soft tissues and wound healing has concentrated on establishing a biomechanics framework to understand and control the biological processes that determine the effects of treatments and exposures on barrier function and the biomechanics of human skin and other soft tissues for which he was awarded the Henry Maso Award for fundamental contributions to the advancement of cosmetic and skin science, and scar formation in healing cutaneous wounds. A major theme in his labs current research involves wearable device technologies. The interdisciplinary nature of his research is reflected in his appointments in the Stanford Biodesign Institute and in the Deptment of Surgery, Stanford School of Medicine.

His interdisciplinary research includes interaction with researchers in academia, industry, and clinical practice. He has served as an editor and reviewer for a number of journals and books including Nature, Science, Energy and Environmental Sciences, Nanoletters, Acta Materialia, the Journal of Applied Physics, PANS and the New England Journal of Medicine. He has co-organized international technical conferences and symposia in his areas of research. He has published over

400 articles in the scientific literature and holds more than 30 U.S. and International Patents. Dauskardt has contributed significantly to leadership in Stanford's multidisciplinary materials efforts which spans several departments, schools, and the SSRL.

Education: B.Sc. (1980) and M.Sc. (1983) Physics, Mathematics and Materials – U. Witwatersrand, South Africa, Ph.D. Materials Science and Eng. - U.C. Berkeley/ U. Witwatersrand (1988).

Recognition and Awards: 2016: Visiting Professor, Nanyang Technological University. 2013: appointed the Ruth G. and William K. Bowes Professor in the School of Engineering, Stanford University. 2011: H. Maso Award for fundamental contributions to skin science, Int. Fed. Soc. Cos. Chem.; IBM Shared University Research Award. 2010: Semiconductor Industry Assoc. Univ. Researcher Award for substantive contributions to semiconductor industry sci. & tech.; TMS Struct. Mat. Distinguished Scientist Award; Fellow ASM Int. 2008: Fellow Am. Ceram. Soc.; VLSI/ULSI Multilevel Interconnection Int. Conf. Award for "Optimized Curing and CMP of Nanostructured Ultra-low-k Films"; Am. Vac. Soc. Thin-Film User Group Special Award. 2006: Distinguished Speaker Award, Dept. MSE, Penn State; IBM Faculty Award, Yorktown Heights. 2003: ASM Int. Silver Medal. 2002: Alexander von Humboldt Research Award. 1989: U.S. DoE Outstanding Sci. Accomplishment Award.

Advisory Boards and Board of Directors: Advisory Board, National Inst. Materials Science, Tsukuba, Japan; Advisory Borad, School of Mat. Sci. Eng. Nanyang Tech. U., Singapore; Advisory Board, Singapore Institute of Manufacturing Technology (SimTech), A-Star, Singapore; Co-founder, Neodyne Biosciences Inc. (medical devices), Palo Alto, CA.

Professional Activities: Dauskardt has been involved in a range of university academic and materials research leadership roles at Stanford. He is an established international leader in the broader materials and device technical and scientific communities where he has managed several large multidisciplinary research activities. He has served as organizer of a range of international conferences and symposia.

He serves as a consultant and technical advisor to a range of leading international technology companies, materials suppliers, and equipment vendors. He is well known for his work providing technical expert services in trial, by declaration, and/or deposition for litigation and regarding both validity and infringement analysis in US and International patent cases.

Doctoral Students and Post Doctoral Fellows: Dauskardt has supervised 66 doctoral students and 48 post-doctoral fellows, medical residents and medical fellows. He currently has 16 doctoral students, 2 masters student, and 2 post docs in his research group along with visiting professors and industry researchers.

PUBLICATIONS

Book Editing:

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2. Kemal Levi and Reinhold H. Dauskardt, "Biomechanics of the Barrier Function of Human Stratum Corneum," **The Art and Science of Moisturizers**, 2011.

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2. R. H. Dauskardt, R. D. Pendse and R. O. Ritchie, "Effects of Pre-Existing Grain Boundary Microvoid Distributions on Crack Growth under Monotonic and Cyclic Loading," **Acta Metallurgica et Materialia**, **35** [9] 2227-42, 1987.

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