

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

IPR2025-01211

U.S. Patent No. 7,439,623

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,439,623**

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,439,623
1002	File History of U.S. Patent No. 7,439,623 (“the ’623 File History”)
1003	Declaration of Dr. Reinhold Dauskardt
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. (“Watanabe”)
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. (“Hasunuma”)
1006	Reserved
1007	U.S. Patent No. 6,717,267 to Kunikiyo (“Kunikiyo”)
1008	U.S. Patent No. 5,250,465 to Iizuka et al. (“Iizuka”)
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. (“Kamoshima”)
1010	JP2002299437 (“Fukazawa”) and Certified Translation of Fukazawa with Certification of Translation
1011	U.S. Patent No. 7,042,099 to Kurashima (“Kurashima”)
1012	P. Andricacos, “Copper On-Chip Interconnections,” <i>Interface, The Electrochemical Society</i> , pp. 32-37, 1999
1013	U.S. Patent No. 5,885,857 to Yamaha et al. (“Yamaha”)
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi et al. (“Igarashi”)

Exhibit No.	Description
1015	U.S. Patent No. 6,717,268 to Hau-Riege (“Hau-Riege”)
1016	U.S. Patent No. 6,468,894 to Yang (“Yang”)
1017	U.S. Patent No. 6,022,808 to Nogami (“Nogami”)
1018	AICP’S P.R. 3-1 Disclosure of Asserted Claims and Infringement Contentions and P.R. 3-2 Document Production Against TSMC (cover document only)
1019	Kaanta et al., “Dual Damascene: A ULSI Wiring Technology,” <i>VMIC Conference</i> , IEEE, Jun. 11-12, 1991, pp. 144-152
1020	U.S. Patent No. 5,032,890 to Ushiku (“Ushiku”)
1021	Reserved
1022	Reserved
1023	Reserved
1024	U.S. Patent No. 6,156,660 to Liu et al. (“Liu”)
1025	U.S. Patent No. 5,798,298 to Yang (“Yang 2”)
1026	T. I. Bao <i>et al.</i> , “90 nm Generation Cu/CVD Low-k ($k < 2.5$) Interconnect Technology,” <i>Digest. International Electron Devices Meeting</i> , San Francisco, CA, USA, 2002, pp. 583-586
1027	A. Loke, “Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects,” Dissertation, Stanford University (1999)
1028	K.N. Tu, “Recent advances on electromigration in very-large-scale-integration of interconnects,” <i>Applied Physics Review</i> –

Exhibit No.	Description
	<i>Focused Review, Journal of Applied Physics</i> , Vol. 94, No. 9 (November 1, 2003), pp. 5451-5473
1029	T. C. Huang, <i>et al.</i> , “Numerical Modeling and Characterization of the Stress Migration Behaviour Upon Various 90 nanometer Cu/Low k Interconnects,” <i>Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)</i> , Burlingame, CA, USA, 2003 (added to IEEE Xplore 8-11-2003), pp. 207-209
1030	JPH10214893 to Fujii (“Fujii”) and Certified Translation of Fujii with Certification of Translation
1031	Reserved
1032	JP2000012688 to Nasu (“Nasu”) and Certified Translation of Nasu with Certification of Translation
1033	U.S. Patent Publication No. 2001/0030365 to Otsuka <i>et al.</i> (“Otsuka”)
1034	Wolf, Stanley, <i>Silicon Processing for the VLSI Era: Deep-Submicron Process Technology</i> , Lattice Press, 2002 (excerpted) (“Wolf”)
1035	Reserved
1036	Ogawa, E.T., <i>et al.</i> , “Stress-Induced Voiding Under Vias Connected To Wide Cu Metal Leads,” IEEE 02CH37320, <i>40th Annual International Reliability Physics Symposium</i> , Dallas, Texas, 2002, pp. 312-21
1037	von Glasow, A., <i>et al.</i> , “Geometrical Aspects of Stress-Induced Voiding in Copper Interconnects,” <i>Proceedings of the Advanced Metallization Conference 2002 (AMC 2002)</i> , San Diego, CA, October 1-3, 2002, Tokyo, Japan, October 29-30, 2002, Materials Research Society, pp. 161-67
1038	U.S. Patent No. 6,215,189 to Toyoda <i>et al.</i> (“Toyoda”)

Petition for *Inter Partes* Review
Patent No. 7,439,623

Exhibit No.	Description
1039	U.S. Patent No. 6,238,850 to Bula et al. (“Bula”)

LIST OF CHALLENGED CLAIMS

Claim Element	Claim Language
[1.pre]¹	A semiconductor device comprising:
[1.a]	a semiconductor substrate;
[1.b]	a first interconnect formed on the semiconductor substrate;
[1.c]	a first insulating film formed on the first interconnect;
[1.d]	a second interconnect formed on the first insulating film;
[1.e]	a via formed through the first insulating film and connecting between the first and second interconnects; and
[1.f]	a dummy via connected to the second interconnect,
[1.g]	wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough;
[1.h]	the second interconnect and the via form a dual damascene structure, and
[1.i]	the second interconnect and the dummy via form a dual damascene structure.
[2.a]	The semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,

¹ Claims 1, 2, and 45 are not challenged in this petition, but are listed here because various challenged claims depend therefrom.

[2.b]	wherein the first interconnect is formed on the second insulating film, and
[2.c]	the dummy via is connected to a first dummy interconnect formed on the second insulating film.
[5.a]	The semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view, and
[5.b]	a diameter of the dummy via is substantially equal to a width of the first dummy interconnect.
[6.a]	The semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square, and
[6.b]	a side of the dummy via is substantially equal to a width of the first dummy interconnect.
[10.a]	The semiconductor device of claim 2, wherein a planar shape of the dummy via is substantially a square, and
[10.b]	a side of the dummy via is smaller than a width of the first dummy interconnect.
19	The semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square.

20	The semiconductor device of claim 19, wherein a length of a side of the via and a length of a side of the dummy via are substantially equal to each other.
[23.a]	The semiconductor device of claim 1, wherein the via is substantially circular in a plan view, and
[23.b]	a diameter of the via is substantially equal to a width of the first interconnect.
[24.a]	The semiconductor device of claim 1, wherein a planar shape of the via is substantially a square, and
[24.b]	a side of the via is substantially equal to a width of the first interconnect.
27	The semiconductor device of claim 1, wherein the distance between the via and the dummy via is substantially equal to a minimum interconnect width.
[29.a]	The semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view, and
[29.b]	a diameter of the dummy via is smaller than a diameter of the via.
[30.a]	The semiconductor device of claim 1, wherein a planar shape of each of the via and the dummy via is substantially a square, and

[30.b]	a side of the dummy via is smaller than a side of the via.
[31.a]	The semiconductor device of claim 1, wherein the dummy via is substantially rectangular in a plan view, and
[31.b]	a longer side of the dummy via in a plan view and a shorter side of the second interconnect are provided along a same direction.
33	The semiconductor device of claim 1, wherein the dummy via is connected to the upper surface of the second interconnect.
34	The semiconductor device of claim 33, wherein the dummy via is formed in a third insulating film formed on the second interconnect.
35	The semiconductor device of claim 34, wherein the third insulating film has a multilayer structure including a SiN film and a SiO ₂ film.
36	The semiconductor device of claim 33, wherein the dummy via includes a second barrier film and a second conductive film.
37	The semiconductor device of claim 36, wherein the second conductive film includes copper.

38	The semiconductor device of claim 33, wherein a second dummy interconnect is provided on the dummy via so as to come in contact with a top of the dummy via.
41	The semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end surrounded by a second insulating film.
43	The semiconductor device of claim 1, wherein a bottom of the dummy via is located deeper than a bottom of the via
[44.a]	The semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,
[44.b]	wherein the first interconnect is formed on the second insulating film, and
[44.c]	a bottom of the dummy via is located in the second insulating film.
[45.a]	The semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and
[45.b]	the via is connected to the second interconnect portion.

[48.a]	The semiconductor device of claim 45, wherein the dummy via is substantially rectangular in a plan view, and
[48.b]	a longer side of the dummy via and a longer side of the first interconnect portion are provided along a same direction.

I. RELIEF REQUESTED

Applying the following grounds, Petitioner petitions for *Inter Partes* Review (“IPR”) of U.S. Patent No. 7,439,623 (“the ’623 patent”) and cancellation of claims 5-6, 10, 19-20, 23-24, 27, 29-31, 33-38, 41, 43-44, and 48:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	10, 19-20, 24, 27	102	Watanabe
1B	27	103	Watanabe
2	23	103	Watanabe + Iizuka
3	5	103	Watanabe + Iizuka + Kurashima
4	6	103	Watanabe + Kurashima
5	29-30	103	Watanabe + Nasu
6	31	103	Watanabe + Fujii
7	48	103	Watanabe + Kamoshima + Fukazawa
8	23, 27, 41, 43-44	102	Hasunuma
9	5	103	Hasunuma + Kurashima
10	6	103	Hasunuma + Kurashima + Iizuka
11	19-20	103	Hasunuma + Watanabe

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
12	24	103	Hasunuma + Iizuka
13	29-30	103	Hasunuma + Nasu
14	33-38	103	Hasunuma + Kamoshima

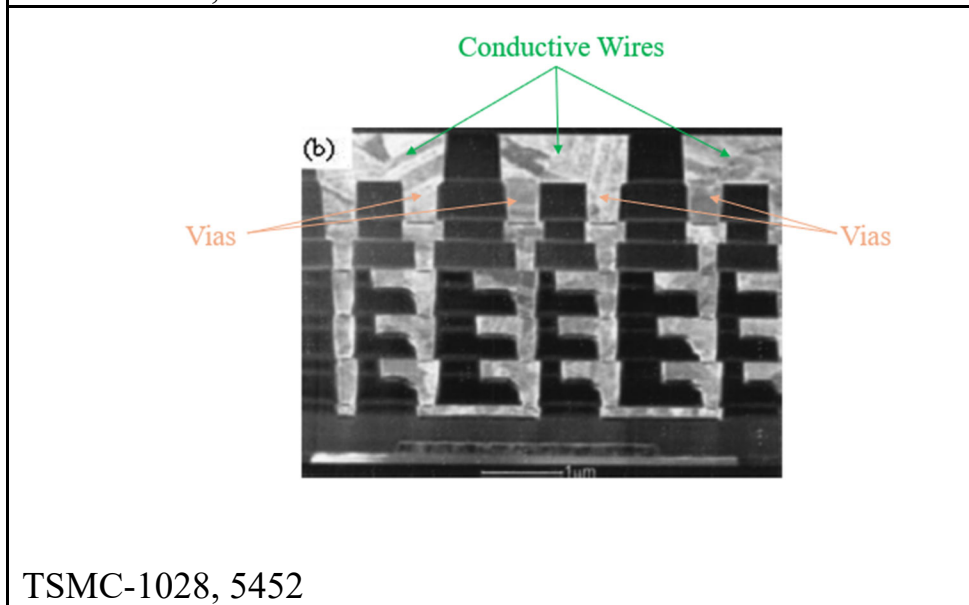
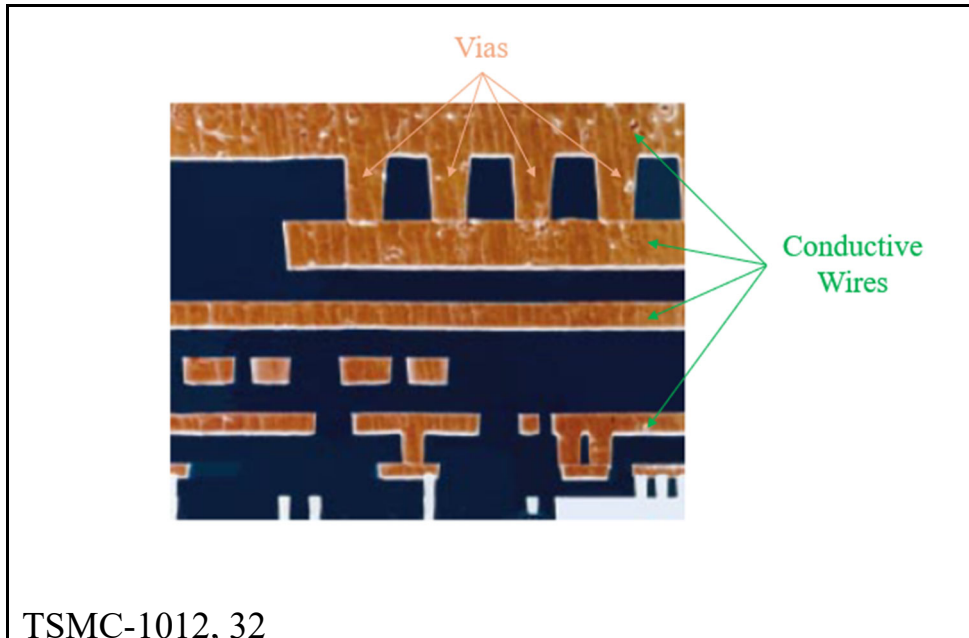
Independent claim 1 and dependent claims 2 and 45 are formally challenged in IPR2025-01212. This petition addresses further dependent claims that merely add conventional features that were well-known prior to the '623 patent. This petition is supported by the declaration of Dr. Reinhold Dauskardt, an expert in the field of interconnect technology. TSMC-1003, ¶¶1-39.

II. STATE OF THE ART

The '623 patent describes the use of dummy structures to reduce stress-induced void formation in interconnect structures. Such dummy structures, for the same purposes, were already well-known. TSMC-1003, ¶¶40-46.

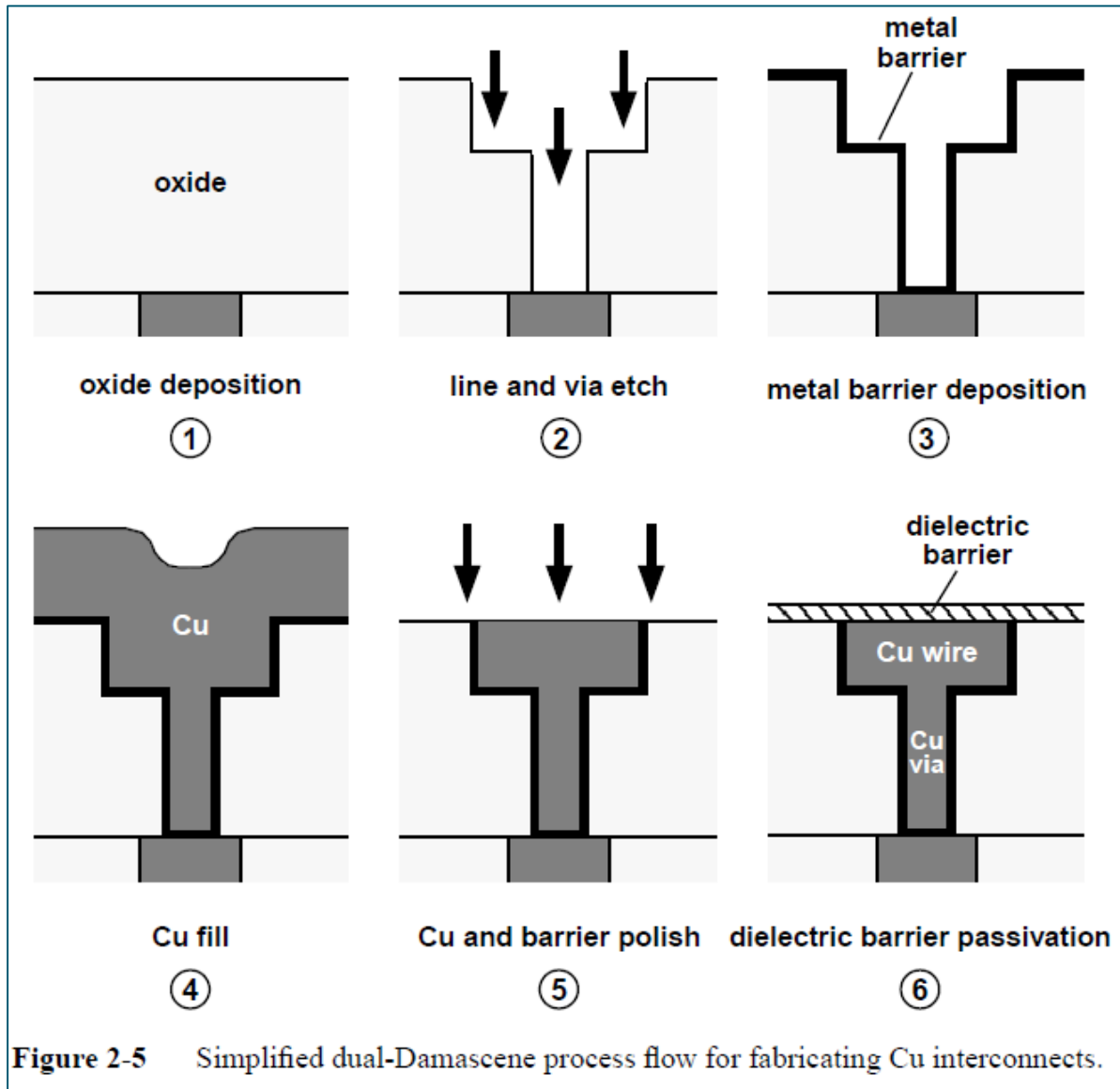
A. Interconnects and Dual Damascene

Semiconductor chips have multiple levels of conductive wires (“interconnects”) for controlling chip operation, with vias connecting wires between different levels when needed; such interconnect structures are commonly made of aluminum or copper. TSMC-1015, 1:13-24; *see also* TSMC-1012, 32; TSMC-1017, 2:53-58. Exemplary interconnect structures are shown below:



Dual damascene is a manufacturing process where patterns of trenches and underlying via holes are filled with conductive metal(s) to simultaneously form the interconnects on a given level and the vias below that level. TSMC-1015, 4:20-23;

TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract; TSMC-1034, 671-76. This process is illustrated below:



TSMC-1027, 25. Steps ④→⑤ are typically performed using chemical mechanical polishing (“CMP”). TSMC-1034, 322-34, 675.

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength

Stress migration and electromigration involve the movement of metal atoms and vacancies within the interconnect structure; because vacancies tend to aggregate in/under vias, voids can form and cause electrical disconnects. TSMC-1029, 207; TSMC-1028, 5455-56, 5458-59; TSMC-1015, 1:32-37, 2:61-63. In addition, insulating films, especially low-k materials, can have poorer mechanical strength and adhesion, making them susceptible to damage during CMP. TSMC-1016, 1:53-2:7; TSMC-1026, 583.

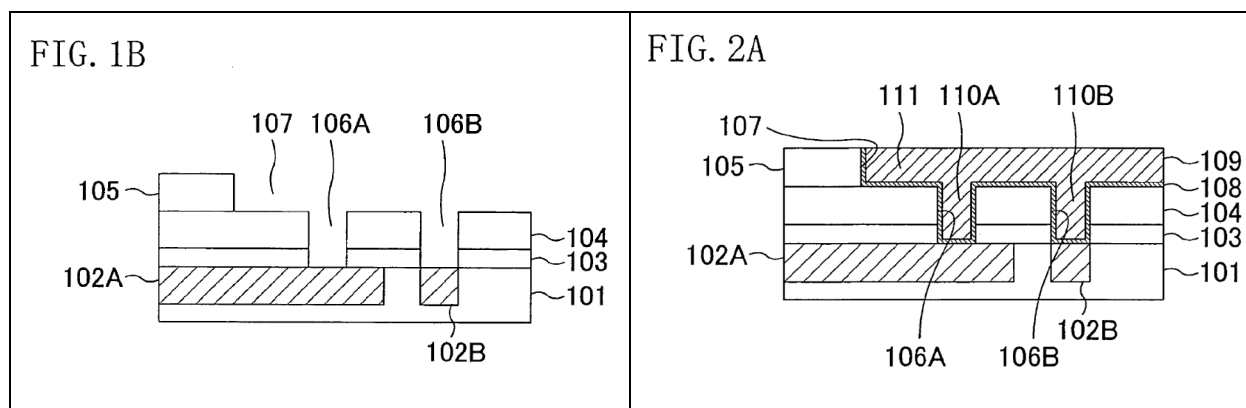
Dummy structures were used long before the '623 patent for addressing these problems. For example, dummy vias have been added near active vias to arrest stress-induced vacancy migration and void formation. TSMC-1029, Abstract, 208; TSMC-1015, 2:64-3:14. Dummy structures were also known to alleviate electromigration concerns, acting as reservoirs for metallic ions. *See* TSMC-1015, 1:66-2:11; TSMC-1032, ¶¶[0012]-[0016]. Migrating vacancies/microvoids get distributed between vias and dummy vias, reducing their concentration in/under active vias. TSMC-1029, 208; TSMC-1009, ¶[0088]. Dummy vias also improve mechanical strength, preventing damage during CMP. TSMC-1016, 4:42-47; TSMC-1026, 584-85.

Similar to dummy vias, dummy wirings/interconnects also improve mechanical properties, helping adhesion across multiple insulating layers and improving the CMP process by reducing dishing. TSMC-1020, Abstract; TSMC-1024, 2:55-58; TSMC-1025, Abstract; TSMC-1026, 584-85. Connecting dummy wirings to dummy vias was well-known to increase the mechanical strength of the combined insulating layer and upper-level wiring, as well as enhance the durability of multi-layered insulating films. TSMC-1011, 8:35-54.

III. THE '623 PATENT

A. Overview

The '623 patent relates to a semiconductor device having multilevel interconnection structures. TSMC-1001, 7:47-50. A first interconnect 102A (and optionally a dummy interconnect 102B) is formed in insulating film 101. *Id.*, 10:56-63, Figs. 1A, 2B. After forming intermediate insulating layers 103-105, the dual damascene process is used to form second interconnect 111 on/in the insulation layer stack, which is connected to first interconnect 102A by via 110A:



Id., 11:5-21; 6:38-40, Figs. 1B-1C, 2A-2B. Dummy via 110B, formed in dummy hole 106B simultaneously with via 110A and interconnect 111, connects dummy interconnect 102B with second interconnect 111. *Id.*, 11:15-21; Figs. 2A-2B.

First interconnect 102A, via 110A and second interconnect 111 constitute part of a closed-circuit during device operation, while neither dummy interconnect 102B nor dummy via 110B does. *Id.*, 10:24-28. That is, the device remains operable even if dummy interconnect 102B and dummy via 110B are omitted from the structure. *Id.*, 10:28-32.

According to the '623 patent, vacancies in copper film 109 of second interconnect 111 are divided and respectively flow into via 110A and dummy via 110B, thereby reducing vacancies flowing into via 110A and reducing the associated stress gradient. *Id.*, 11:36-42. The '623 patent says this suppresses occurrences of voids in via hole 106A. *Id.*, 11:38-45.

B. Prosecution History

The '623 application was filed on December 2, 2004, claiming priority to a Japanese application filed December 3, 2003. Following the addition of claims 27-86 in a restriction response, the USPTO issued multiple Office Actions rejecting the claims over U.S. Patent No. 6,919,637 to He. TSMC-1002, 237-47, 285-97. The Examiner also rejected dependent claims reciting relative interconnect widths, via diameters, and their spacing, stating that "one of ordinary skill in the art would

have been led to the recited shapes, sizes and dimensions through routine experimentation and optimization.” *Id.*, 244-45, 295-96. Applicant responded first by requiring that the dummy via be conductive, then adding “dual damascene” limitations, but later deleted these limitations and instead required that the dummy via be incapable of current flow. *Id.*, 266, 301, 331. The NOA re-added the dual-damascene limitations, while stating that the prior art did not teach the “dummy via made of a conductive film and being arranged as in the context of claim 27.” *Id.*, 354-55.

C. Claim Construction

The Board construes claims under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For purposes of this proceeding, Petitioner does not believe that any claim terms need construction to resolve the unpatentability issues presented in this Petition. TSMC-1003, ¶57.

IV. ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. TSMC-1003, ¶37. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. *Id.*

V. PRIOR ART²

Reference	Filed	Published	Pre-AIA Prior Art Qualification
Watanabe	12/4/2002 (USPTO)	6/26/2003	§§102(a),(b),(e)
Hasunuma	9/3/2003 (USPTO)	6/17/2004	§102(e)
Iizuka	1/24/1992 (USPTO)	10/5/1993	§§102(a),(b),(e)
Kurashima	8/14/2003 (USPTO)	5/9/2006	§102(e)
Nasu	6/24/1998 (JPO)	1/14/2000	§§102(a),(b)
Fujii	10/8/1997 (JPO)	8/11/1998	§§102(a),(b)
Kamoshima	9/9/2003 (USPTO)	9/9/2004	§102(e)
Fukazawa	3/29/2001 (JPO)	10/11/2002	§§102(a),(b)

VI. DETAILED EXPLANATION OF GROUNDS

A. Ground 1A: Watanabe Anticipates Claims 10, 19-20, 24, and 27

Watanabe anticipates claims 10, 19-20, 24, and 27. TSMC-1003, ¶¶106-194.

² All references are prior art regardless of any priority claim to the Japanese application filed December 3, 2003. Petitioner does not acquiesce that any claims are so entitled.

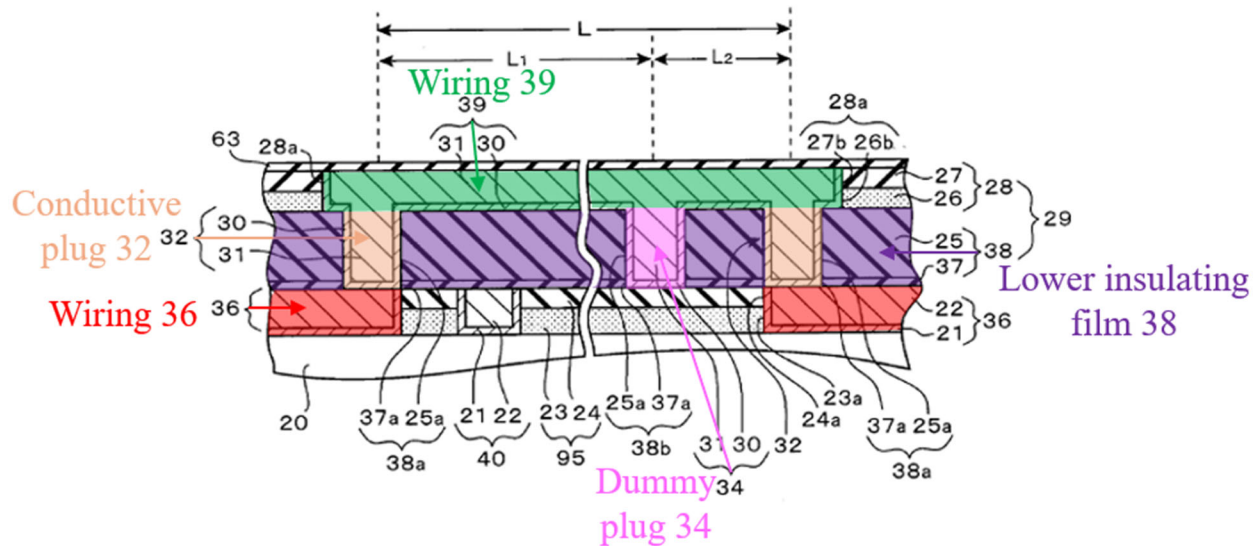
1. Watanabe

Because Watanabe is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Watanabe is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1004, ¶¶[0005], [0016]-[0018]; TSMC-1003, ¶¶59-77. Indeed, Watanabe recognized the same problem and proposed the same solution before the '623 patent. TSMC-1003, ¶59.

Watanabe discloses semiconductor devices having multilevel dual-damascene interconnect structures that address reliability problems caused by stress-induced void migration and electromigration. TSMC-1004, ¶¶[0012]-[0019], [0022]-[0024], [0077]. Watanabe incorporates non-functional dummy vias and dummy interconnects formed concurrently with the functional structures. *Id.*, Abstract, ¶¶[0026]-[0028]; TSMC-1003, ¶59.

Watanabe's first embodiment (Figures 1-2) discloses wiring 36, overlying insulating film 29, and wiring 39 formed along with conductive plug 32 and dummy conductive plug 34 using dual damascene:

FIG. 1

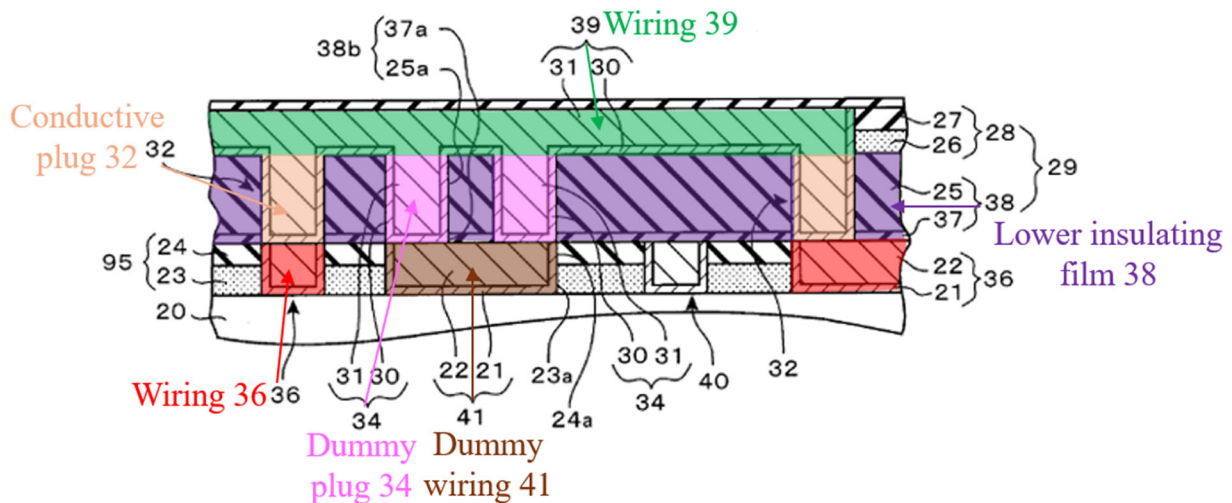


Id., ¶¶[0065]-[0074], Fig. 1; TSMC-1003, ¶65.

Conductive plug 32 connects wiring 36 and wiring 39. Dummy plug 34 connects to wiring 39 but its other end extends to a “non-forming region” of insulating film 95. TSMC-1004, ¶¶[0067], [0079]; TSMC-1003, ¶66. Watanabe teaches that dummy plug 34 reduces stress migration problems, provides a source of copper atoms to mitigate electromigration, and enhances support for insulating film 29/wiring 39. *Id.*, ¶¶[0026], [0070]-[0079], [0091]; TSMC-1003, ¶66.

Watanabe’s second embodiment (Figures 3-4) adds dummy wiring 41:

FIG. 3



Id., ¶¶[0028], [0090]; TSMC-1003, ¶67. Dummy wiring 41 resides in the same insulating film 95 as wiring 36, and adds mechanical strength and uniformity during CMP. *Id.*, ¶¶[0028]-[0029], [0090]-[0091]; TSMC-1003, ¶68.

Watanabe discloses multiple embodiments, including:

- a “first embodiment” in Figures 1-2 (*see* TSMC-1004, ¶¶[0059]-[0087]);
- a “second embodiment” in Figures 3-4 (*see id.*, ¶¶[0088]-[0092]);
- a “third embodiment” in Figures 5A-5C (*see id.*, ¶¶[0093]-[0108]);
- a “fifth embodiment” in Figures 8-11 (*see id.*, ¶¶[0115]-[0133]); and
- a more generic embodiment in Figure 14 (*see id.*, ¶¶[0171]-[0181]).

See, e.g., *id.*, ¶¶[0038]-[0049], [0051]; TSMC-1003, ¶60.

Watanabe's Figs. 12A-12N show a method of manufacturing for the foregoing embodiments. TSMC-1004, ¶[0049] ("...method of manufacturing the

semiconductor device **according to the embodiments of the present**

invention”)³; *see also id.*, ¶¶[0072], [0134]-[0170]; TSMC-1003, ¶64. The first-fifth embodiments (Figures 1-9) and Figures 12A-12N use common reference numerals. TSMC-1004, ¶¶[0089], [0116], [0135]; TSMC-1003, ¶74. Watanabe also discloses that the method can be repeated to obtain any number of wirings. TSMC-1004, ¶¶[0171]-[0173]; TSMC-1003, ¶75.

2. Claim 1⁴

Watanabe’s first embodiment is applied to claim 1 below, and subsequent sections apply Watanabe’s other embodiments.

a) First Embodiment

(1) [1.pre]

Watanabe discloses “a semiconductor device” as shown in Figures 1, 12A-12N, and 14. TSMC-1004, Title, Abstract, ¶¶[0003], [0038], [0051], [0135]-[0136], [0170]-[0173]; TSMC-1003, ¶¶108-09.

(2) [1.a]

Watanabe discloses underlying layer 20 that includes a “silicon wafer (semiconductor substrate)”:

³ All emphases have been added unless otherwise noted.

⁴ *See* List of Challenged Claims for all claim language. Claims 1, 2, and 45 are addressed herein given dependencies of Challenged Claims.

FIG. 1

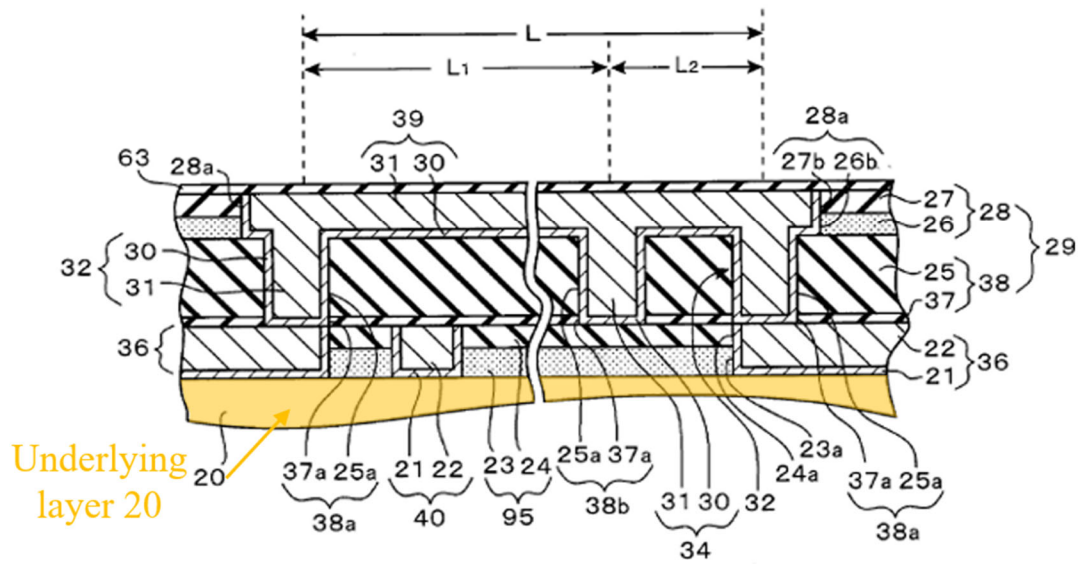
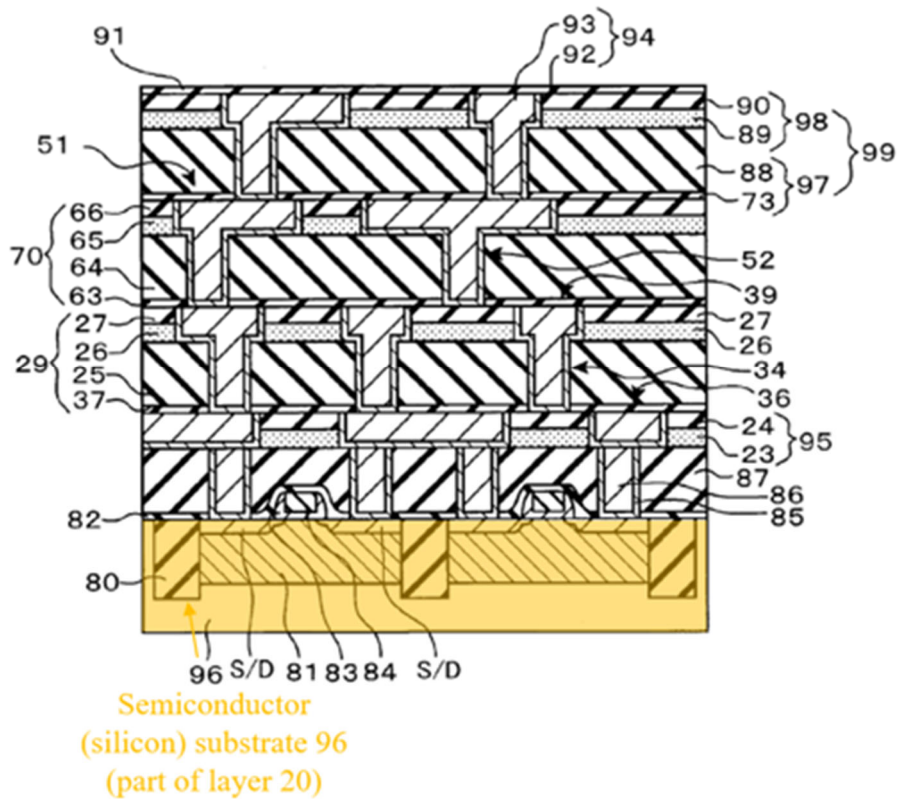


FIG. 14

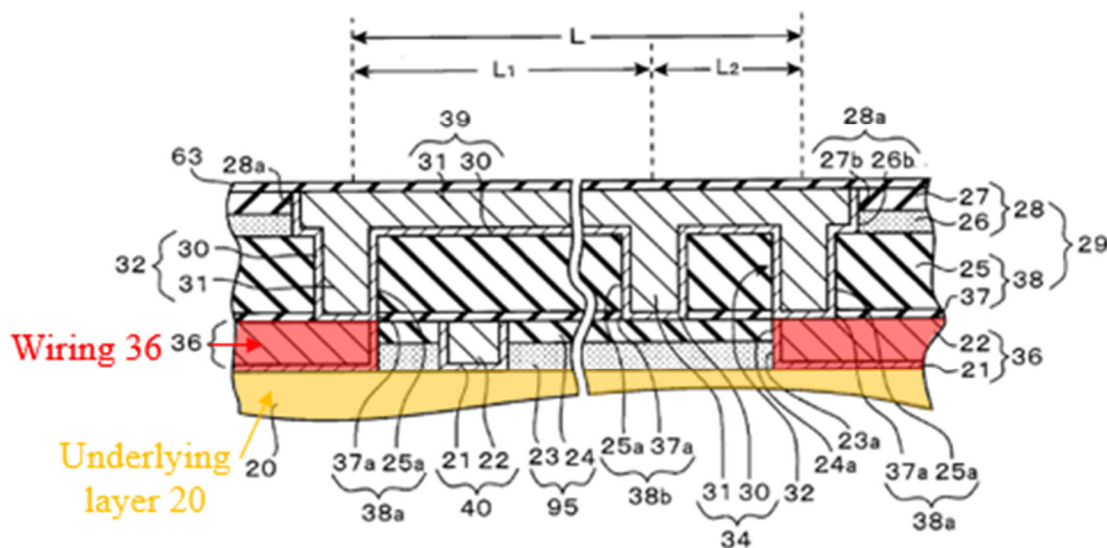


TSMC-1004, ¶¶[0061]; *see also id.*, ¶¶[0051], [0135]-[0136], [0172]-[0173], Figs. 1, 12A, 14; TSMC-1003, ¶¶110-11.

(3) [1.b]

Watanabe discloses a first interconnect (e.g., “wiring 36”) formed on underlying layer 20 (having a semiconductor substrate):

FIG. 1

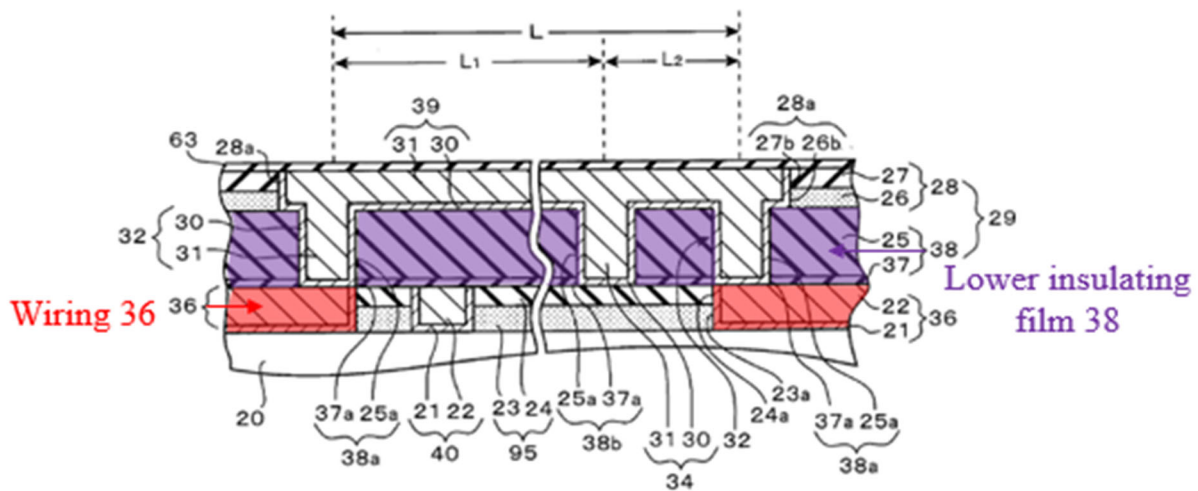


TSMC-1004, $\sqrt{3}\sqrt{3}$ [0051], [0061], [0064]-[0065], [0136]-[0144], [0174], Figs. 1, 12A-12D, 14; TSMC-1003, $\sqrt{3}\sqrt{3}$ 112-13.

(4) [1.c]

Watanabe discloses a first insulating film (e.g., “lower insulating film 38”) formed on the first interconnect:

FIG. 1

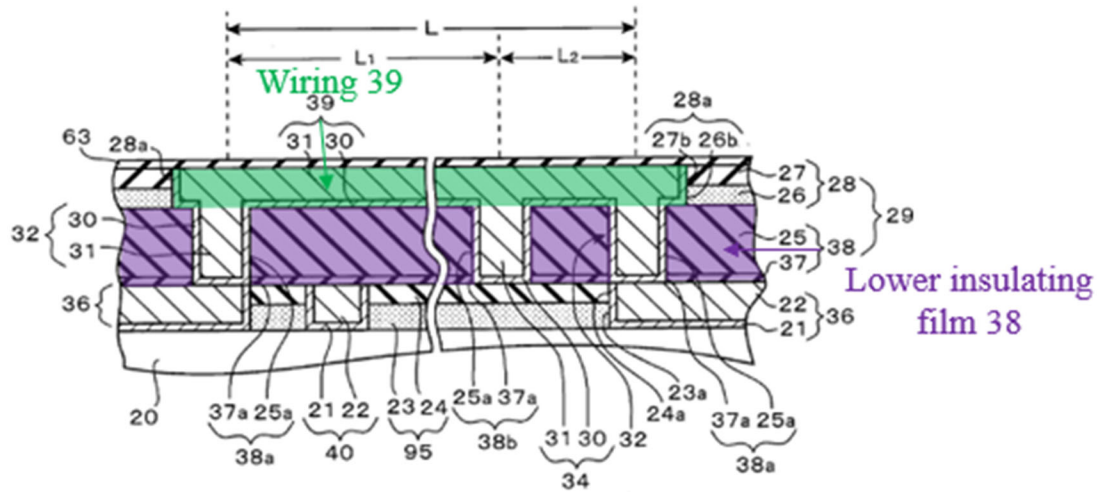


TSMC-1004, ¶¶[0066], [0149]-[0150], [0175], Figs. 1, 3, 12E, 12M, 14; TSMC-1003, ¶¶114-15. Additionally, for purposes of applying Watanabe to the challenged claims, the “first insulating film” could also be read on Watanabe’s entire insulating film stack 29, which includes upper and lower insulating films 28 and 38. TSMC-1004, ¶¶[0149]-[0152]; TSMC-1003, ¶116.

(5) [1.d]

Watanabe discloses a second interconnect (e.g., “wiring 39”) formed on first insulating film (“lower insulating film 38”):

FIG. 1



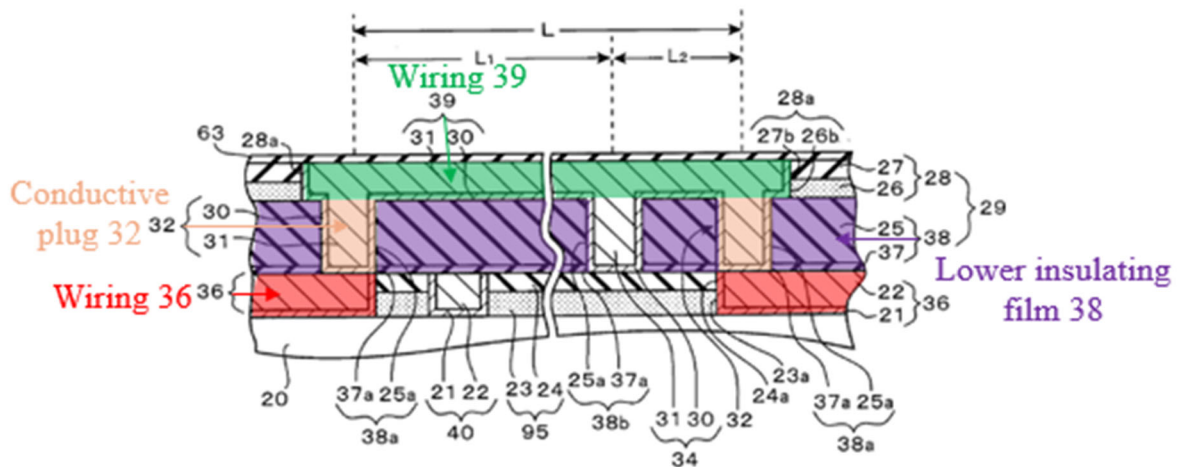
TSMC-1004, ¶¶[0067], [0069], [0153]-[0168], [0175], Figs. 1, 12E-12M, 14;

TSMC-1003, ¶¶117-18.

(6) [1.e]

Watanabe discloses a via (e.g., “conductive plug 32”) formed in via hole 38a through the lower first insulating film, and connecting first and second interconnects (wirings 36, 39):

FIG. 1



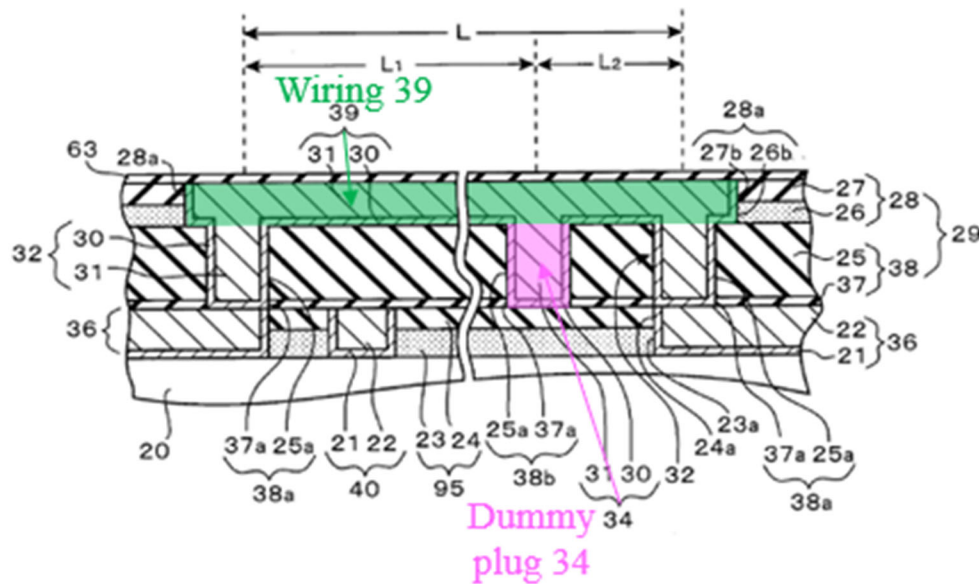
TSMC-1004, ¶¶[0067]-[0070], [0155]-[0168], [0173], Figs. 1, 12G-12M, 14;

TSMC-1003, ¶¶119-120.

(7) [1.f]

Watanabe discloses a dummy via (e.g., “dummy plug 34”) connected to the second interconnect (e.g., “wiring 39”):

FIG. 1



TSMC-1004, ¶¶[0067]-[0072], [0079], [0164]-[0168], Figs. 1, 12G-12M, 14;

TSMC-1003, ¶¶121-22.

(8) [1.g]

Watanabe’s dummy via (“dummy plug 34”) comprises a conductive film and is arranged to be incapable of having current flow therethrough. TSMC-1003, ¶¶123-29. Watanabe’s dummy plug 34 includes conductive barrier metal layer 30

and conductive copper film 31. TSMC-1004, ¶¶[0067]-[0072], [0164]-[0168], [0185], Figs. 1, 12K-12M, 14; TSMC-1003, ¶¶123-29.

The '623 specification states that dummy vias and dummy interconnects “do not constitute a closed circuit in actual use of a device with an interconnection structure including these via and interconnect (i.e., no current flows therein during actual use of the device),” and the circuit is operable even if the dummy vias and dummy interconnects are omitted. TSMC-1001, 3:14-18; 10:26-32.

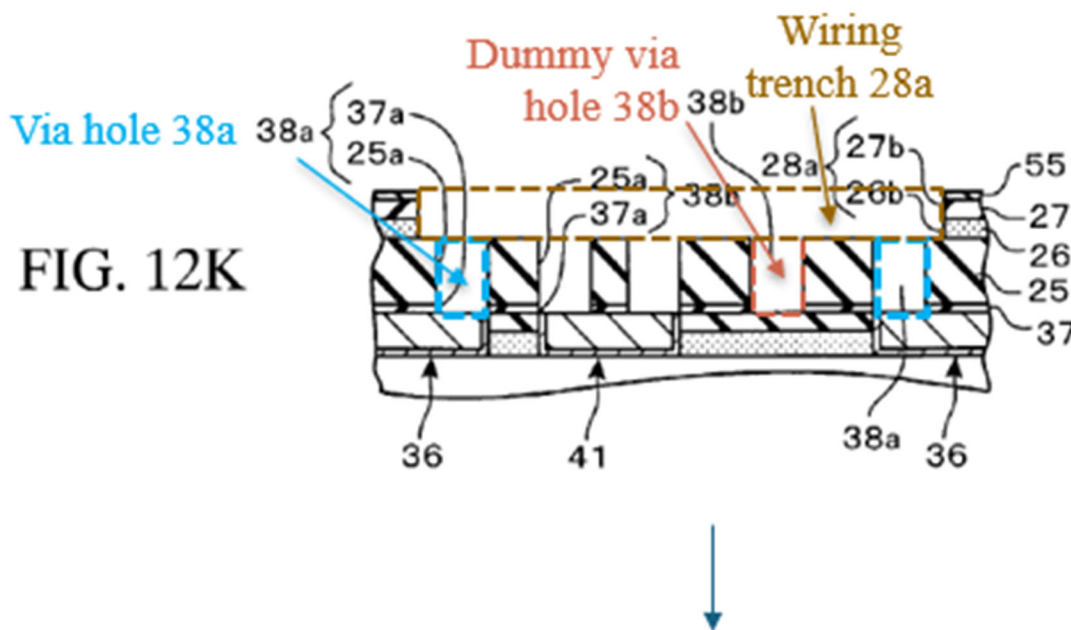
Watanabe's dummy plug 34 extends to a “non-forming region” of insulating film 95. TSMC-1004, ¶¶[0061], [0067], [0079], [0165], Figs. 1, 12K-12M, 14; TSMC-1003, ¶125. Watanabe's dummy plugs 34 do not constitute part of a closed circuit in actual use of the device as no current flows therethrough during actual device use. TSMC-1003, ¶128. A POSITA would recognize that no current flows through dummy plugs 34 due to this lack of connection to a second active circuit element. *Id.*

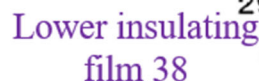
Instead, current flows between wirings 36 and 39 through conductive plugs 32, forming a closed circuit for operation of the device. *See* TSMC-1004, ¶[0073], Figs. 1, 14; TSMC-1003, ¶129. Watanabe's device remains operable without dummy plugs 34, because current would still flow between wirings 36 and 39 through plugs 32 during device use. TSMC-1003, ¶129.

(9) [1.h]/[1.i]

Watanabe discloses forming the second interconnect (“wiring 39”), via (“plug 32”), and dummy via (“dummy plug 34”) using a “dual damascene process,” thus forming dual-damascene structures. TSMC-1004, ¶¶[0067]-[0072], [0135], [0153]-[0168], Figs. 1, 12E-12M, 14; TSMC-1003, ¶¶76, 130-36, 150.

Watanabe fills wiring trench 28a, via hole 38a, and dummy via hole 38b with barrier metal layer 30 and copper film 31, simultaneously forming wiring 39, plug 32, and dummy plug 34:





as well as wiring 39 and dummy plug 34 forming dual damascene structures:



TSMC-1003, ¶¶76, 135-36. The same applies to the structures of Figure 14. *Id.*,
¶136.

b) Second Embodiment

Watanabe's second embodiment (Figures 3-4) also discloses claim 1, including the same components as the first embodiment. *See supra*, §VI.A.2.(a) (discussing underlying layer 20, wiring 36, lower insulating film 38, wiring 39, plug 32, and dummy plug 34). TSMC-1004, ¶¶[0088]-[0092], Figs. 3-4; TSMC-1003, ¶¶137-38, 142.

Further, dummy plugs 34 are connected to a dummy interconnect (“dummy wiring 41”):

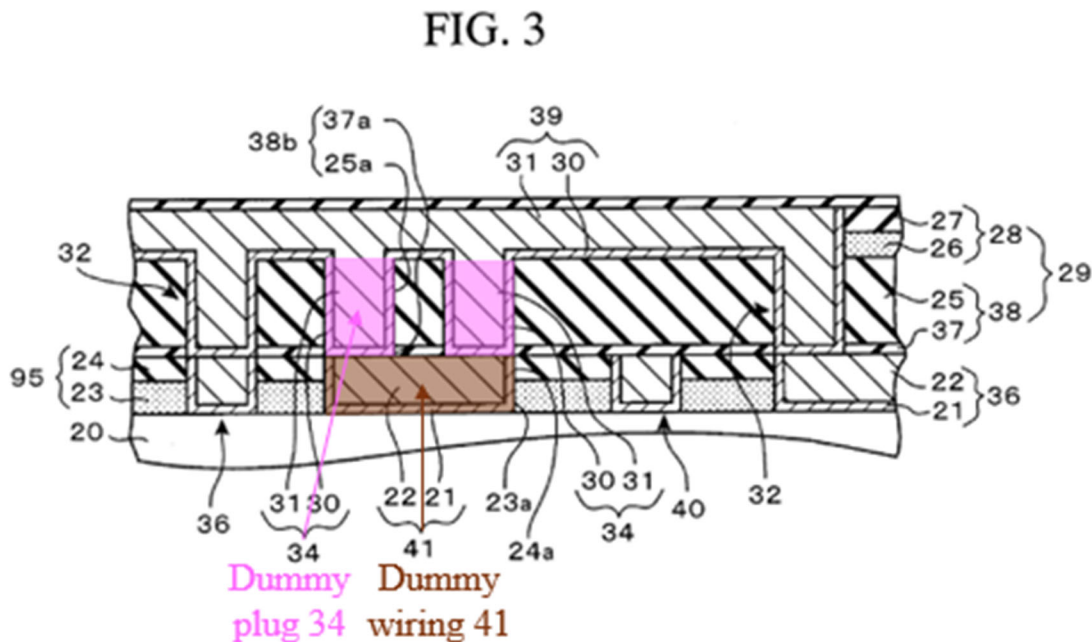
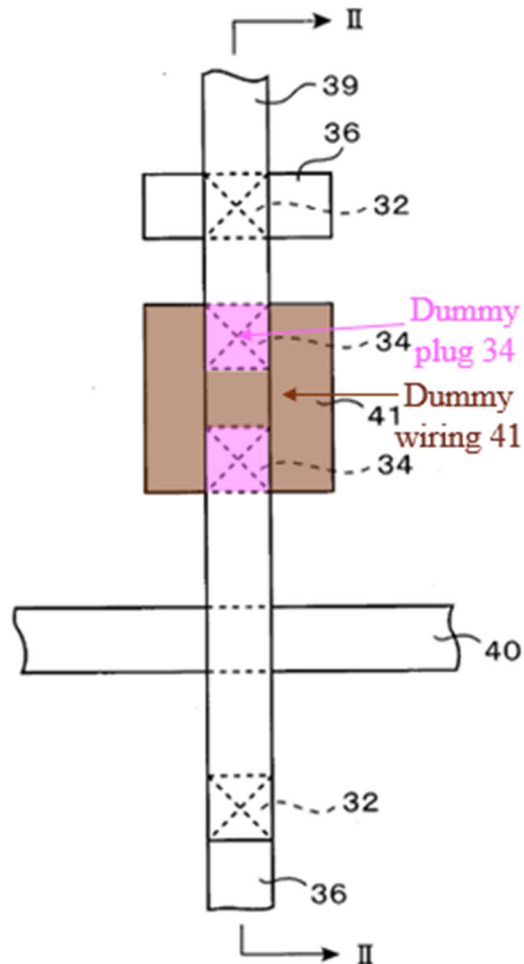


FIG. 4



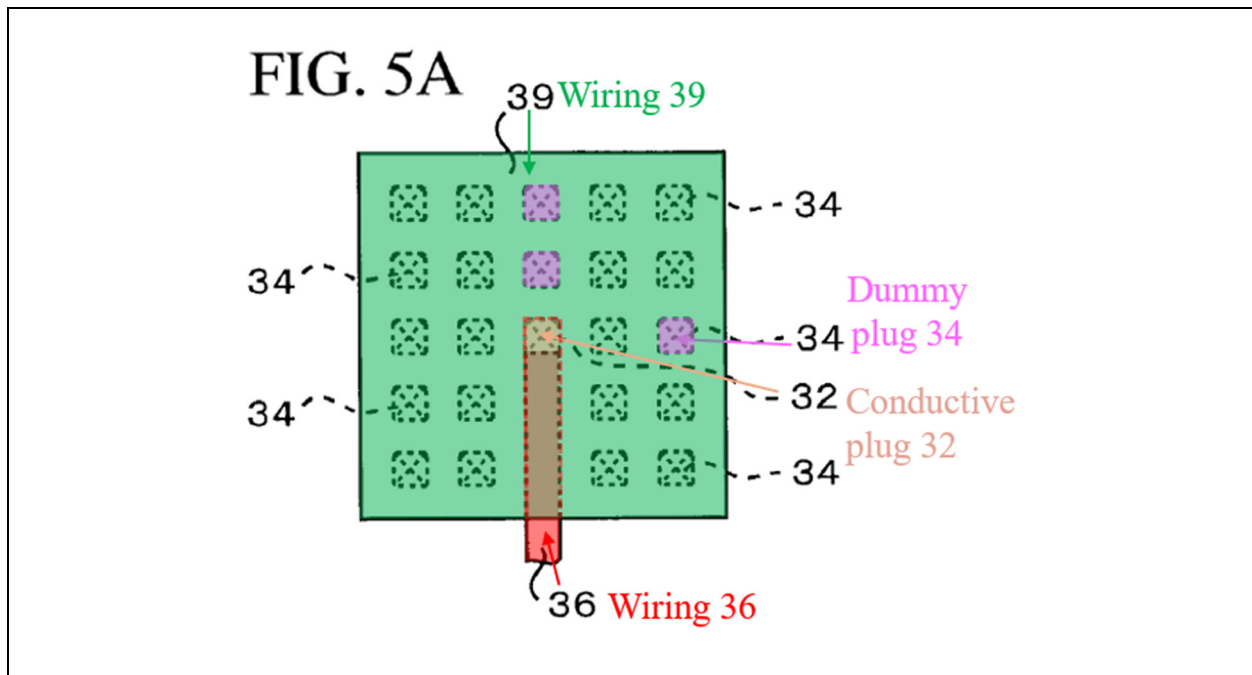
TSMC-1004, ¶¶[0090]-[0092], [0165], [0186], Figs. 12E, 12K-12M; TSMC-1003, ¶¶139-40.

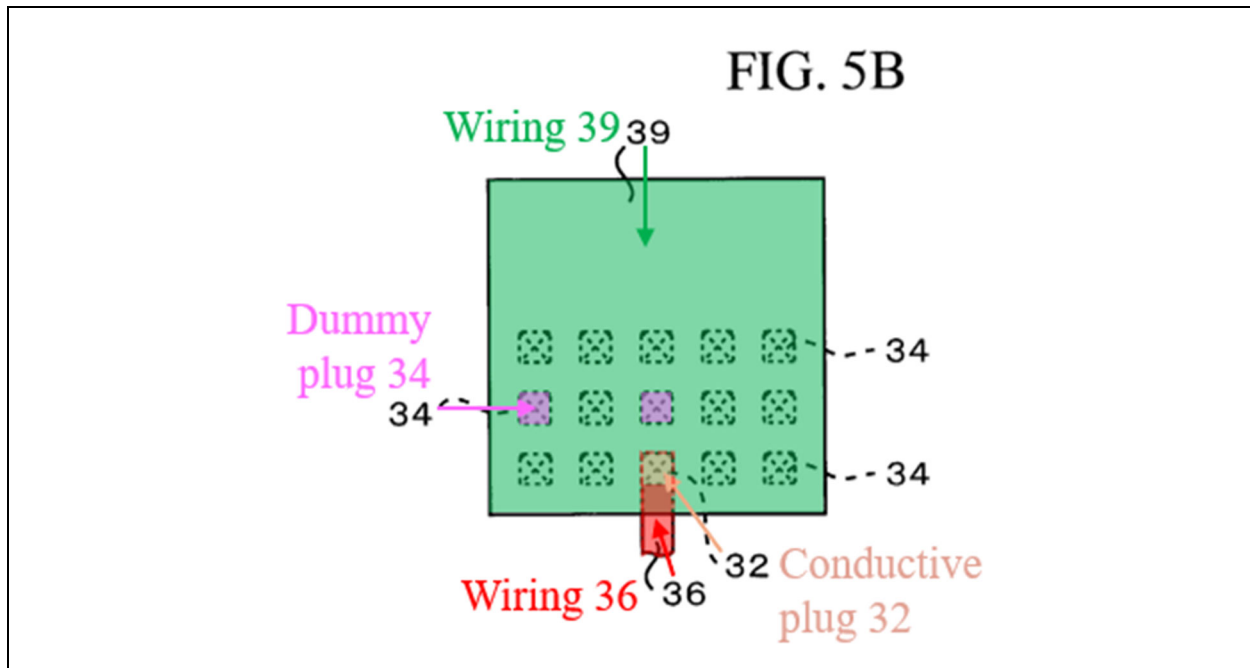
Like Watanabe's first embodiment, "dummy plugs 34" in Watanabe's second embodiment are "incapable of having current flow therethrough" because dummy wiring 41 does not connect to any other active circuit element or form part of a closed circuit during actual use. TSMC-1004, ¶¶[0089], [0135], [0166]-

[0168], [0186]; TSMC-1003, ¶140. And, even with omitting dummy plugs 34 and dummy wiring 41, the device would still be operable because wirings 36, 39 and plugs 32 form a closed circuit for operation of the device. *Id.*, ¶¶140-41.

c) Third Embodiment

Watanabe's third embodiment discloses claim 1, matching the first and second embodiments in relevant respects, while providing an alternative shape/configuration for wiring 39 and dummy plugs 34 in various locations:

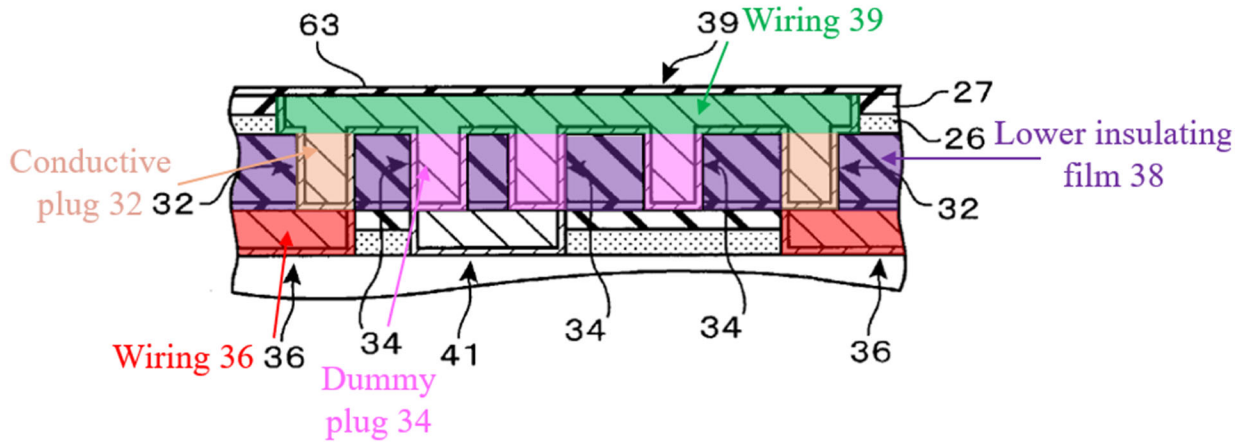




TSMC-1004, ¶¶[0093]-[0099], Figs. 5A-5C; TSMC-1003, ¶143.

Also given Watanabe’s express statement that Figure 12 represents “sectional views showing a method of manufacturing the semiconductor device according to the embodiments of the present invention,” a POSITA understood that the cross-section of Figure 12N discloses the basic structure of Watanabe’s third embodiment (e.g., Figures 5A-5C):

FIG. 12N

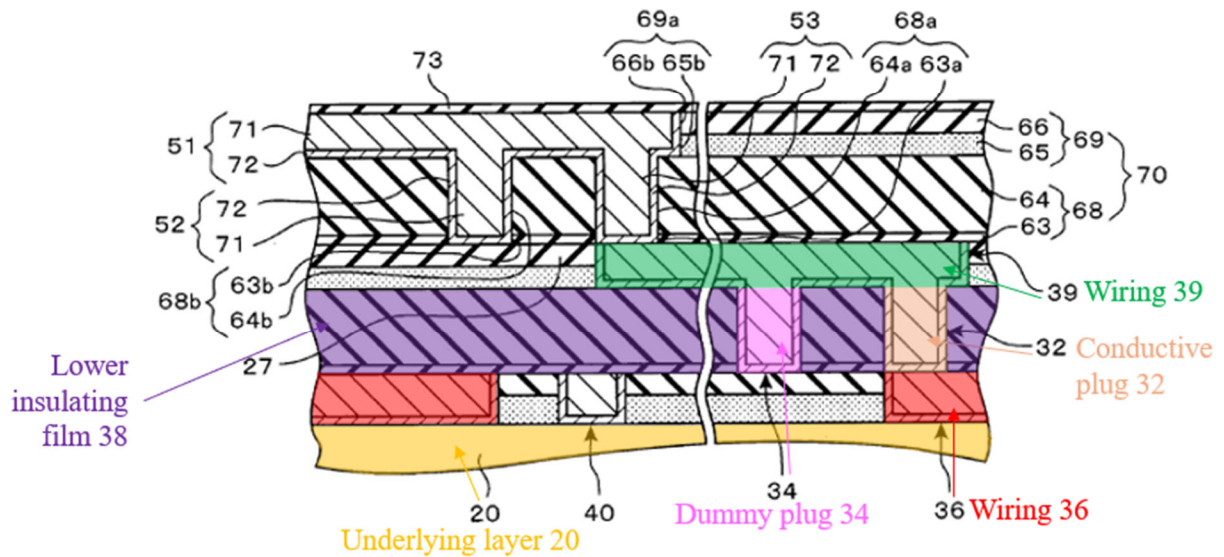


TSMC-1004, ¶¶[0049], [0135], Fig. 12; TSMC-1003, ¶143. Thus, Watanabe's third embodiment similarly discloses claim 1 for the same reasons as Watanabe's first embodiment. *Supra*, §VI.A.2.(a); TSMC-1003, ¶¶143-44.

d) Fifth Embodiment

Watanabe's fifth embodiment (Figures 8-9) discloses a three-level interconnect structure that discloses claim 1 in multiple ways. TSMC-1004, ¶¶[0115]-[0133]; TSMC-1003, ¶¶145-51. First, Watanabe's fifth embodiment includes the same structure and meets claim 1 in the same way as the first embodiment, shown in Figure 8 below (a first mapping):

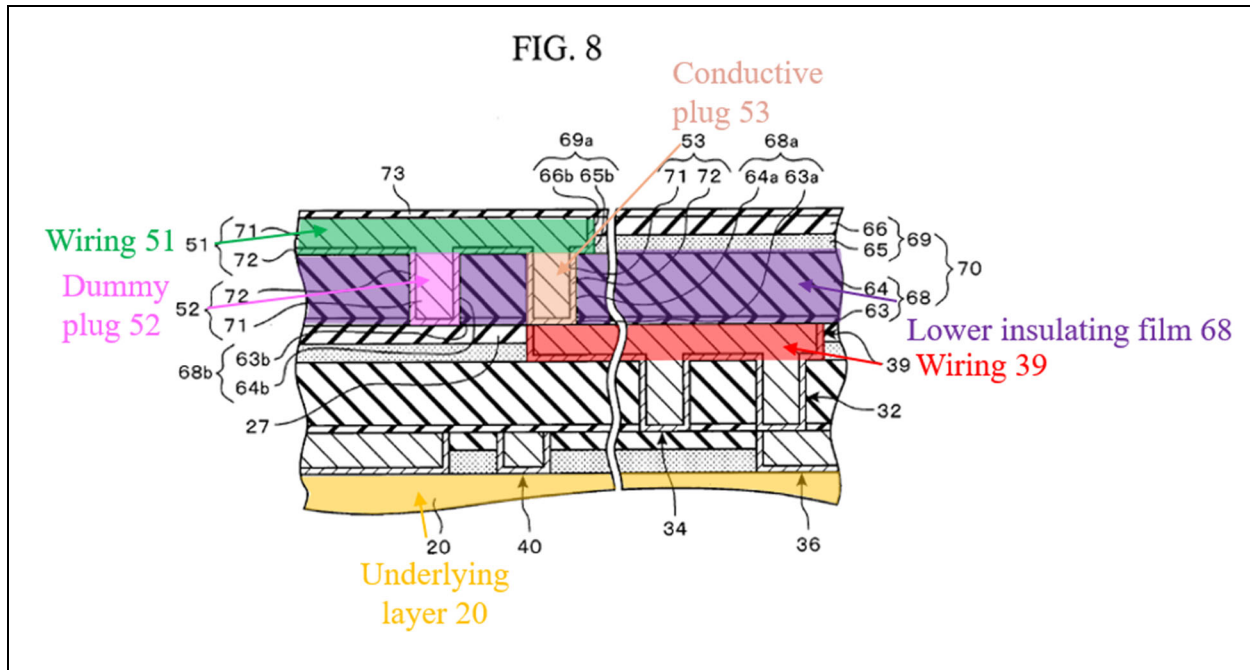
FIG. 8



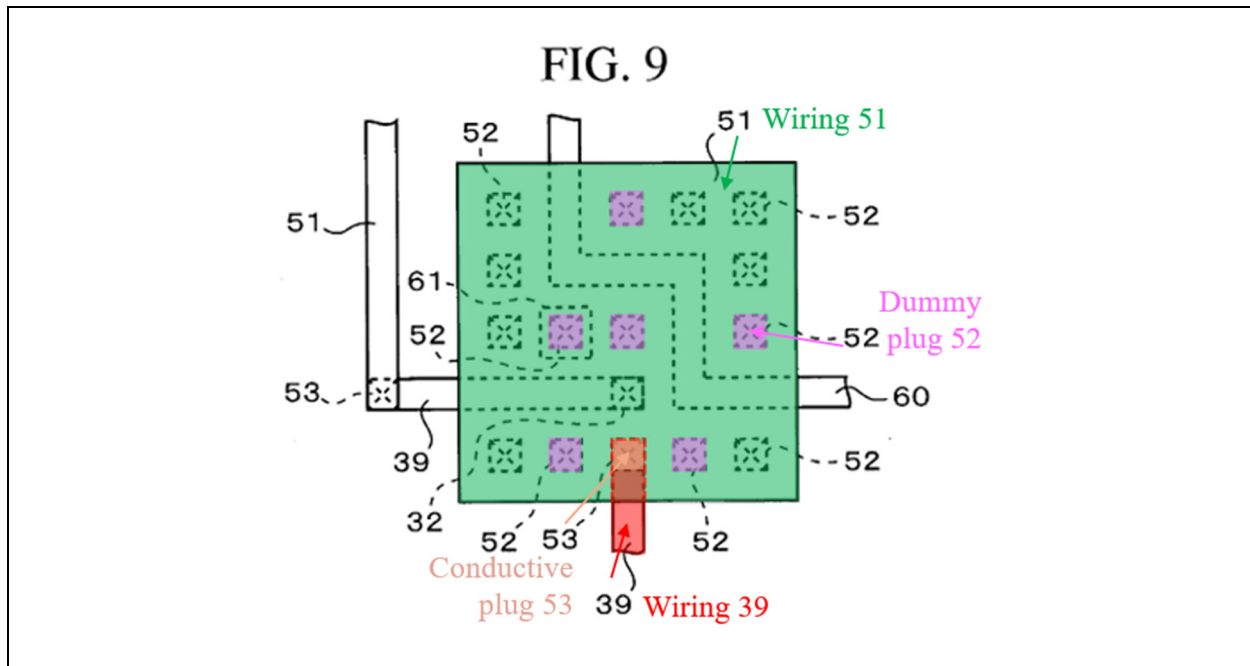
Supra, §VI.A.2.(a); TSMC-1003, ¶146.

As another mapping, Watanabe’s fifth embodiment discloses claim 1 based on wirings 39, 51; thus, wiring 39 is the “first interconnect,” insulating film 68 is the “first insulating film,” and wiring 51 is the “second interconnect.” TSMC-1004, ¶¶[0117]-[0122], Fig. 8; *see also id.*, ¶¶[0172]-[0178], Fig. 14; TSMC-1003, ¶¶147-48. Watanabe’s conductive plug 53 is a “via,” formed within via hole 68a through insulating film 68 and connecting wirings 39, 51. TSMC-1004, ¶¶[0120]-[0122], Figs. 8-9. And Watanabe’s dummy plug 52 is a “dummy via,” connected

to wiring 51. *Id.*, ¶[0122], Figs. 8-9. Figures 8-9 below show this second mapping⁵:



⁵ When Watanabe's first embodiment of Figures 1-2 is applied against a claim, the first mapping of Watanabe's fifth embodiment of Figures 8-9 applies equally and is not separately discussed hereinafter. Further discussions of Watanabe's fifth embodiment below apply the second mapping from Figures 8-9.



TSMC-1003, ¶148.

Dummy plug 52, comprising the same barrier metal layer 72 and copper film 71 as wiring 51, is conductive, but is arranged to be incapable of having current flow therethrough because it extends to and terminates in a “non-forming region” of insulating film 27 (i.e., where there is no wiring 39) or toward dummy wiring 61. TSMC-1004, ¶¶[0118]-[0122], [0127], [0185]-[0186], Figs. 8-9; TSMC-1003, ¶149. The same rationale as for dummy plugs 34 applies to dummy plugs 52. *See supra*, §§VI.A.2.(a).(7)-(8); TSMC-1003, ¶149.

Watanabe’s same “dual damascene” manufacturing process from Figures 12A-12N applies to Figure 8. TSMC-1004, ¶¶[0049], [0118]-[0123], [0134]-[0171], Figs. 12A-12N. Wiring 51 thus forms a dual-damascene structure with

plug 53 and with dummy plug(s) 52, analogous to wiring 39, plug 32, and dummy plug(s) 34. *Id.*, ¶¶[0072], [0171]; *supra*, §VI.A.2.(a).(9); TSMC-1003, ¶150.

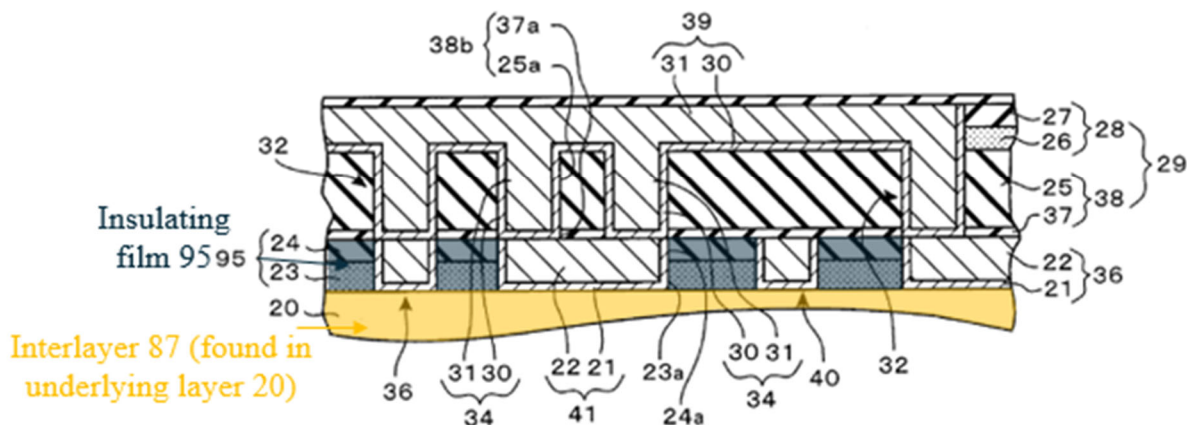
3. Claim 2

Watanabe's second and fifth embodiments meet claim 2. TSMC-1003, ¶¶152-63.

a) [2.a]

Watanabe's second embodiment (Figures 3-4) discloses a "second insulating film" (e.g., constituted by "insulating film 95" and "interlayer insulating film 87" of underlying layer 20, collectively, or optionally insulating film 87 alone). TSMC-1004, ¶¶[0061], [0089], [0172]-[0174], Figs. 3, 14; TSMC-1003, ¶¶153-54. For each embodiment, underlying layer 20 includes components shown in Figure 14, such as interlayer insulating film 87:

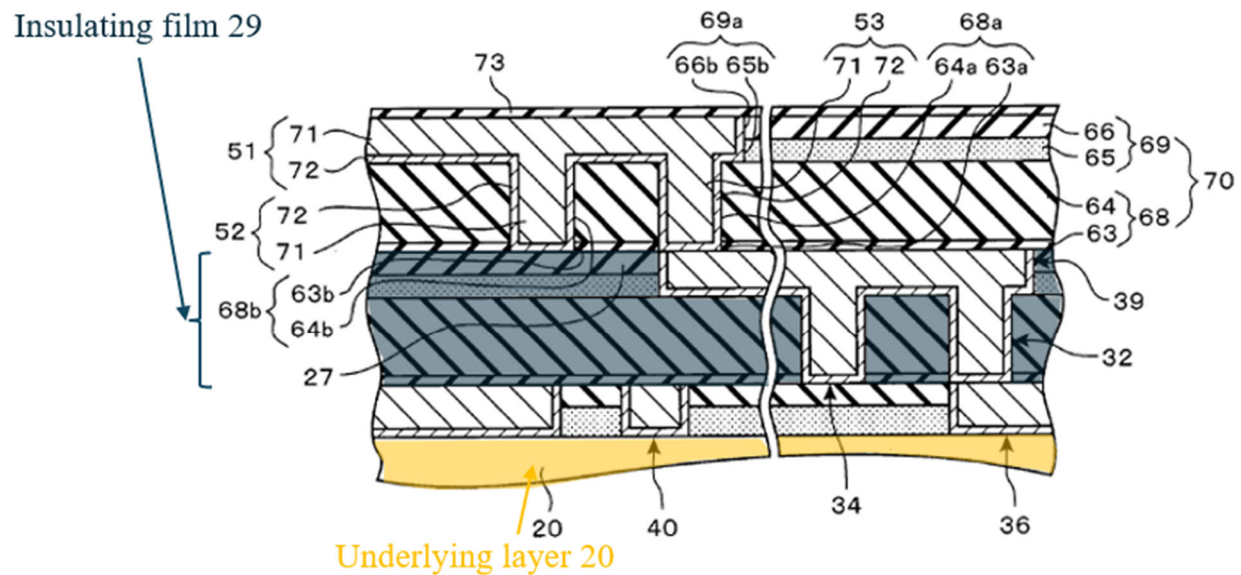
FIG. 3



TSMC-1004, ¶¶[0173]-[0174], [0061], [0089], [0094], [0116]; TSMC-1003, ¶154.

Watanabe's fifth embodiment (Figures 8-9) discloses a "second insulating film" (e.g., "insulating film 29" constituted by upper insulating film 28 and lower insulating film 38; or alternatively just lower insulating film 38). TSMC-1004, ¶¶[0066]-[0067], [0116]-[0117], [0172]-[0175], Figs. 1, 8, 12, 14; TSMC-1003, ¶155. Insulating film 29 is formed on a semiconductor substrate (which is part of underlying layer 20; "silicon substrate 96" in Figure 14):

FIG. 8

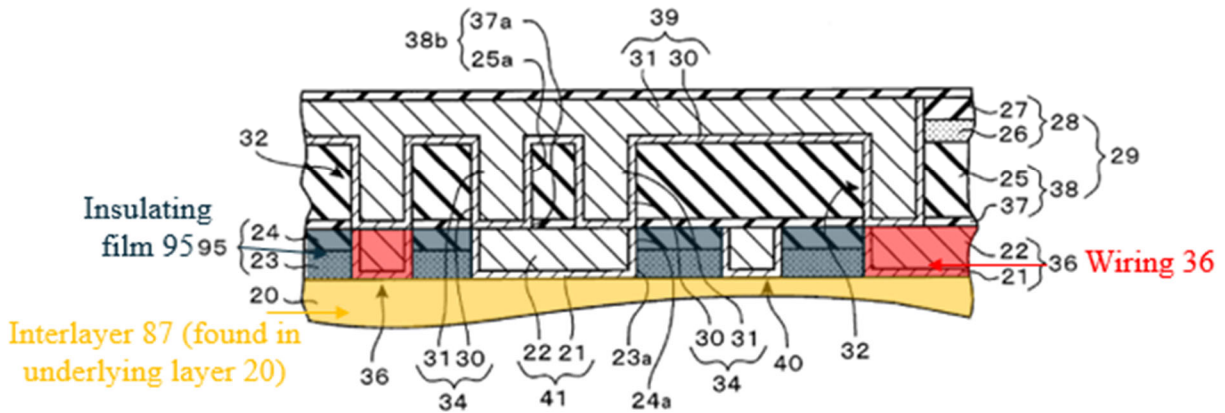


TSMC-1004, ¶¶[0061], [0172]-[0175]; Figs. 1, 8, 12, 14; TSMC-1003, ¶155.

b) [2.b]

Watanabe's second embodiment includes wiring 36 ("first interconnect") formed on interlayer insulating film 87/insulating film 95 ("second insulating film"):

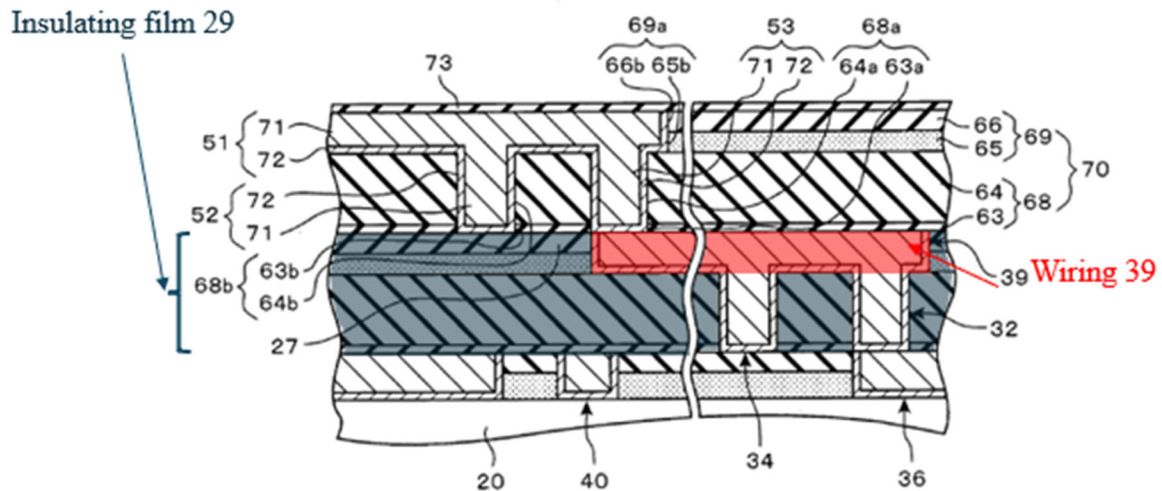
FIG. 3



TSMC-1004, ¶¶[0061], [0089], [0172]-[0174], Figs. 3, 14; TSMC-1003, ¶¶156-57.

Watanabe's fifth embodiment includes wiring 39 ("first interconnect") formed on insulating film 29 ("second insulating film"):

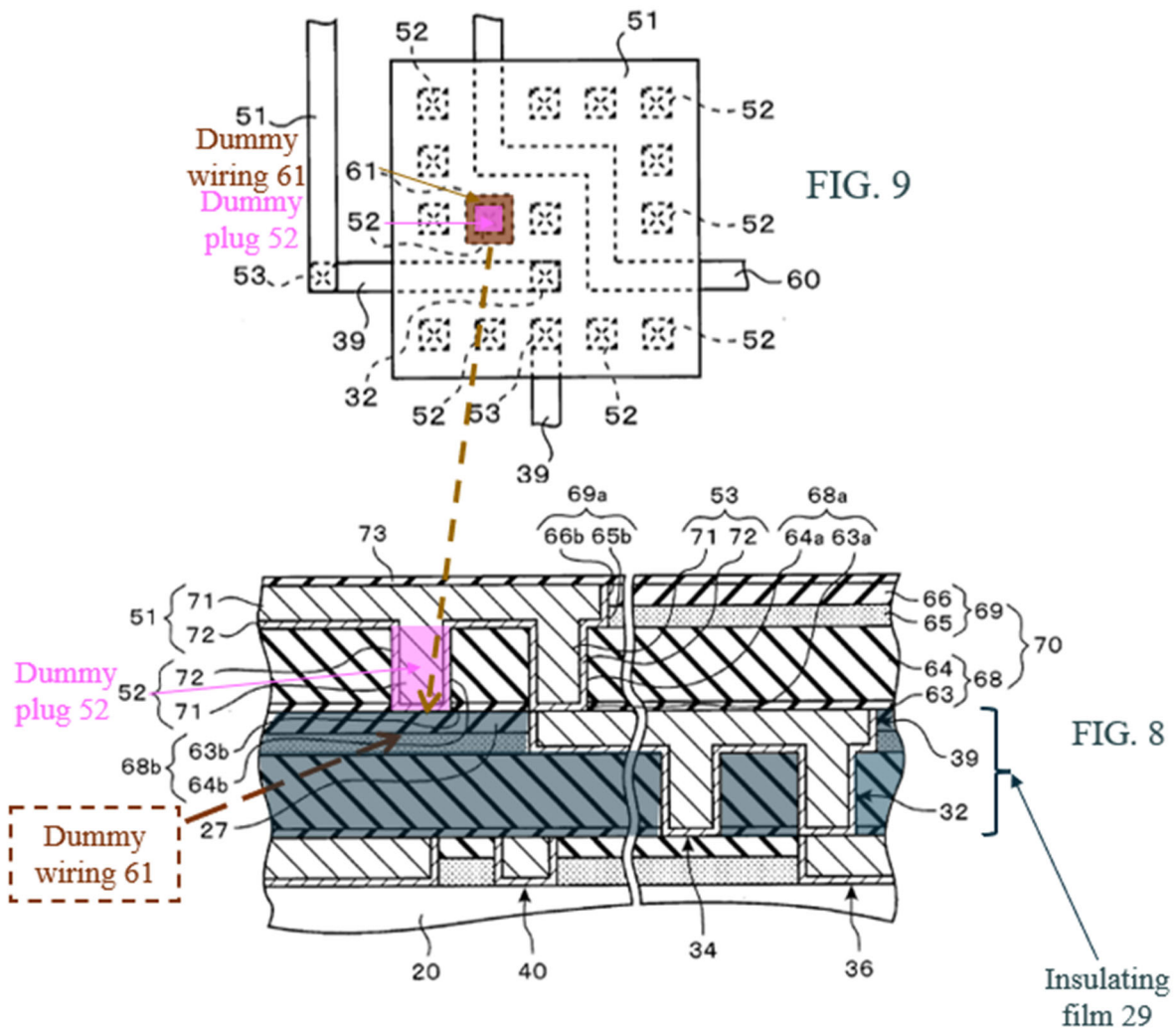
FIG. 8



Watanabe's second embodiment discloses a first dummy interconnect ("dummy wiring 41"), formed on the second insulating film (e.g., insulating film 87/insulating film 95) and connected to a dummy via (e.g., "dummy plug 34"):

Watanabe's fifth embodiment (Figures 8-9) discloses a first dummy interconnect ("dummy wiring 61") formed on insulating film 29 (or lower insulating film 38) ("second insulating film"). TSMC-1004, ¶[0127], Figs. 1, 8-9;

TSMC-1003, ¶¶162-63. Dummy wiring 61 and wiring 39 are at the same level and on the same insulating film (e.g., insulating film 29). TSMC-1004, ¶[0127]; *supra*, VI.A.2.(a).(5); TSMC-1003, ¶¶162-63. Annotated Figures 8-9 disclose the approximate location of dummy wiring 61 when Figure 8 accounts for dummy wiring 61, demonstrating that dummy wiring 61 is on insulating film 29 (or lower insulating film 38):



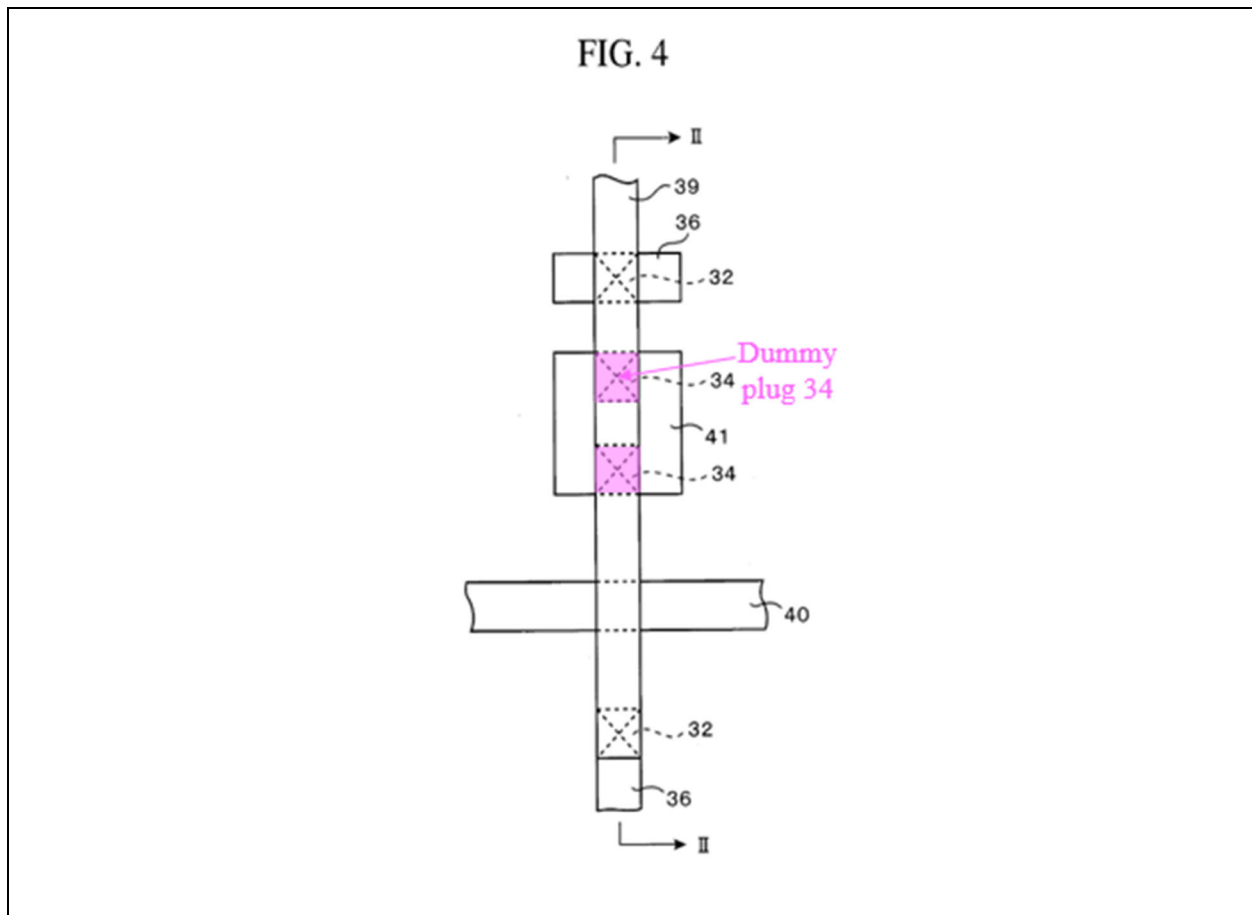
TSMC-1003, ¶162. Dummy plug 52 (“dummy via”) is connected to dummy wiring 61 as shown. TSMC-1004, ¶[0127]; TSMC-1003, ¶163.

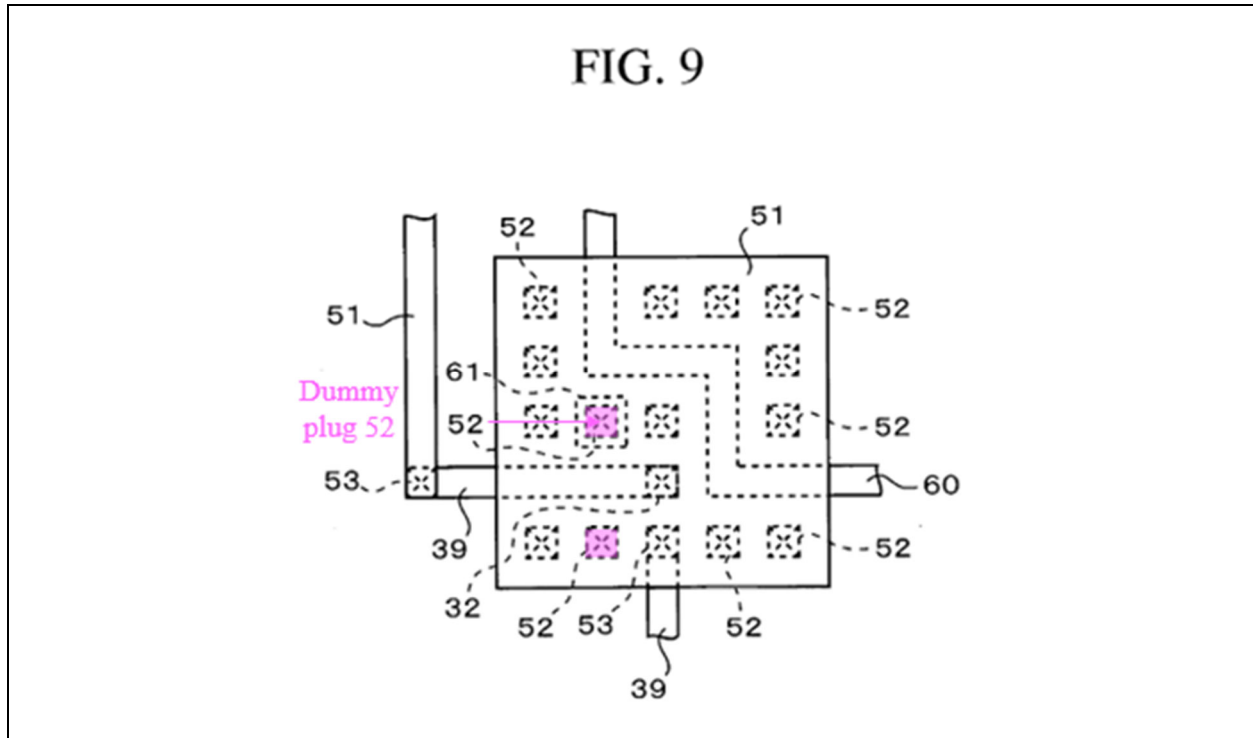
4. Claim 10

At least Watanabe’s second and fifth embodiments meet claim 10. TSMC-1003, ¶¶164-69.

a) [10.a]

For Watanabe’s second and fifth embodiments, Figures 4 and 9 disclose dummy plugs 34 and 52 (“dummy vias”) having a substantially square planar shape:





TSMC-1004, Figs. 4, 9; TSMC-1003, ¶¶165-66. And square shapes for vias were known. *Id.*; see also TSMC-1008, 9:45-47 (“[T]he opening of the via-hole may have any configuration, such as a square....”), 10:8-11; TSMC-1013, 9:45-49; TSMC-1039, 5:27-32 (noting the greater contact area achieved with square vias); TSMC-1003, ¶167.

b) [10.b]

For Watanabe’s second and fifth embodiments, Figures 4 and 9 disclose the side of dummy plug 34/dummy plug 52 (“dummy via”) being smaller than a width of dummy wiring 41/dummy wiring 61 (“first dummy interconnect”):

FIG. 4

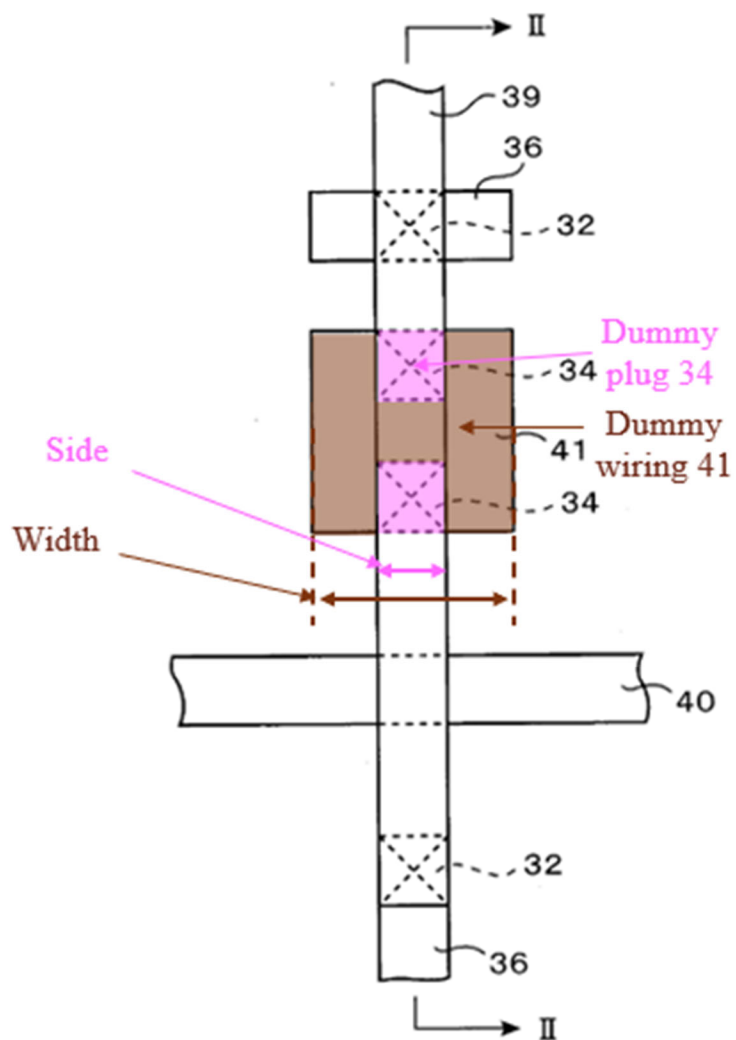
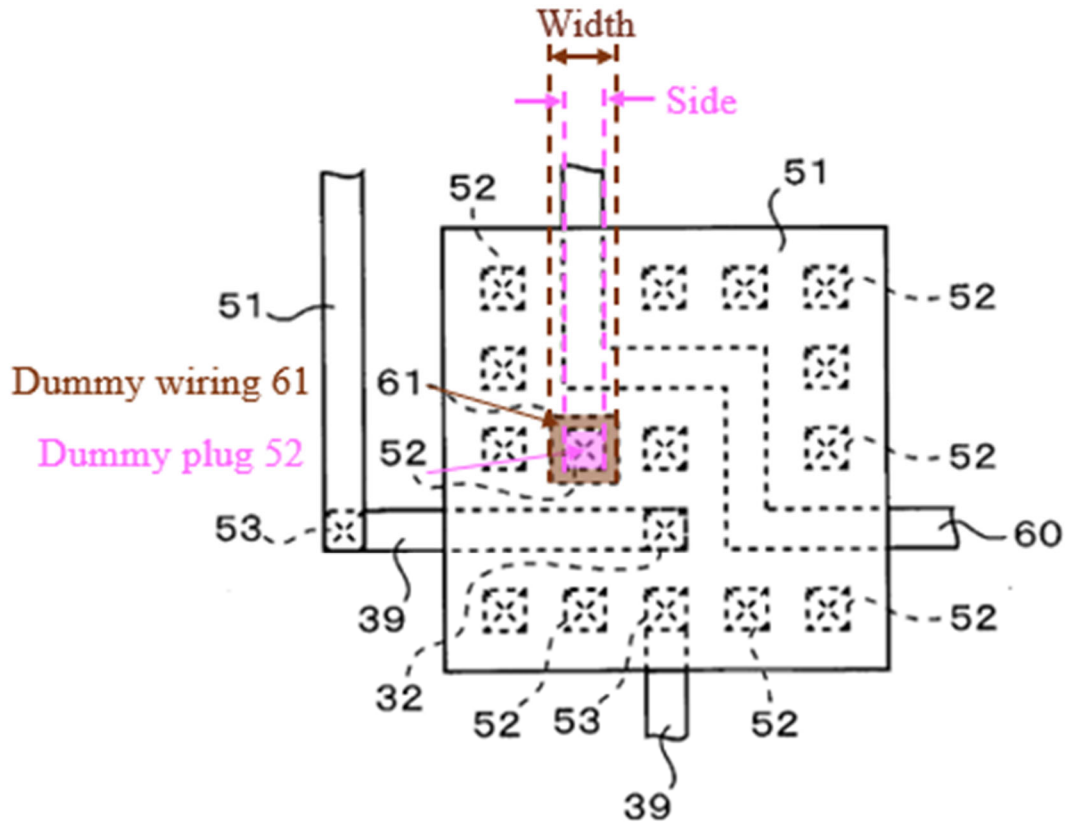


FIG. 9



TSMC-1004, Figs. 4, 9; TSMC-1003, ¶¶168-69.

5. Claim 19

For each of its first-to-third and fifth embodiments, Watanabe discloses that plugs 32/53 and dummy plugs 34/52 each have a planar shape that is substantially square, exemplified in Figures 2, 5A, and 9:

FIG. 2

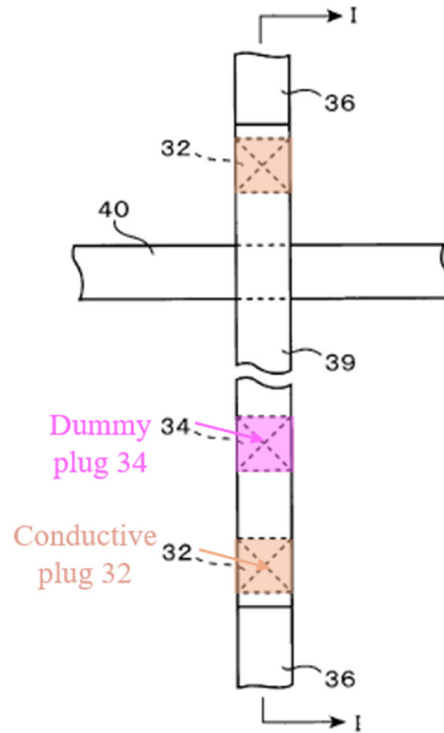


FIG. 5A

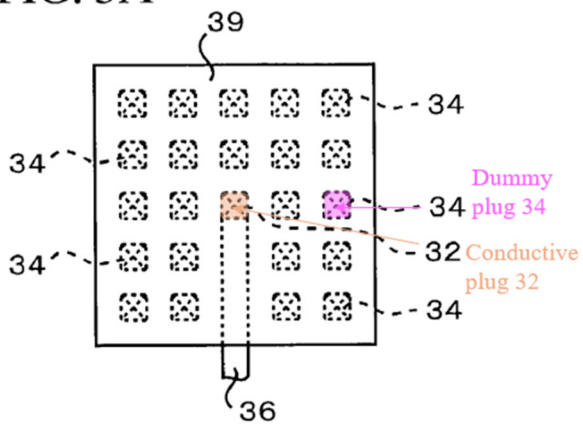
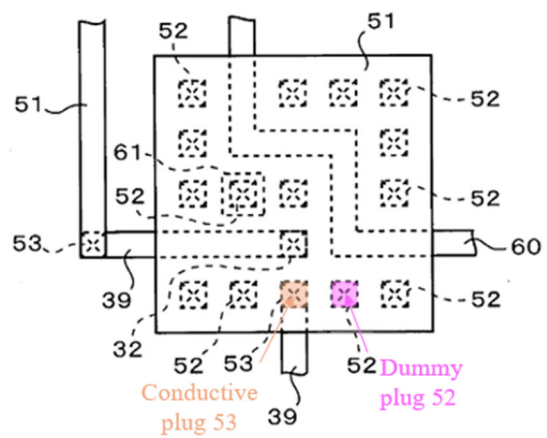


FIG. 9



TSMC-1003, ¶¶170-73; *see also* TSMC-1004, ¶¶[0070], [0096]-[0098], [0124]-[0127], Figs. 2, 4, 5A-5C, and 9. Indeed, square vias were a well-known, common option for via shape. TSMC-1008, 9:45-47 (“[T]he via-hole may have any configuration, such as a square....”), 10:8-11; TSMC-1013, 9:45-49; TSMC-1039, 5:27-32 (noting greater contact area achieved with square vias); TSMC-1003, ¶174.

6. Claim 20

For each of the first-to-third and fifth embodiments, Watanabe discloses that the square vias and dummy vias (discussed for claim 19, above) have side lengths/dimensions that are substantially equal to each other, such as illustrated in Figures 2, 4, 5A, and 9:

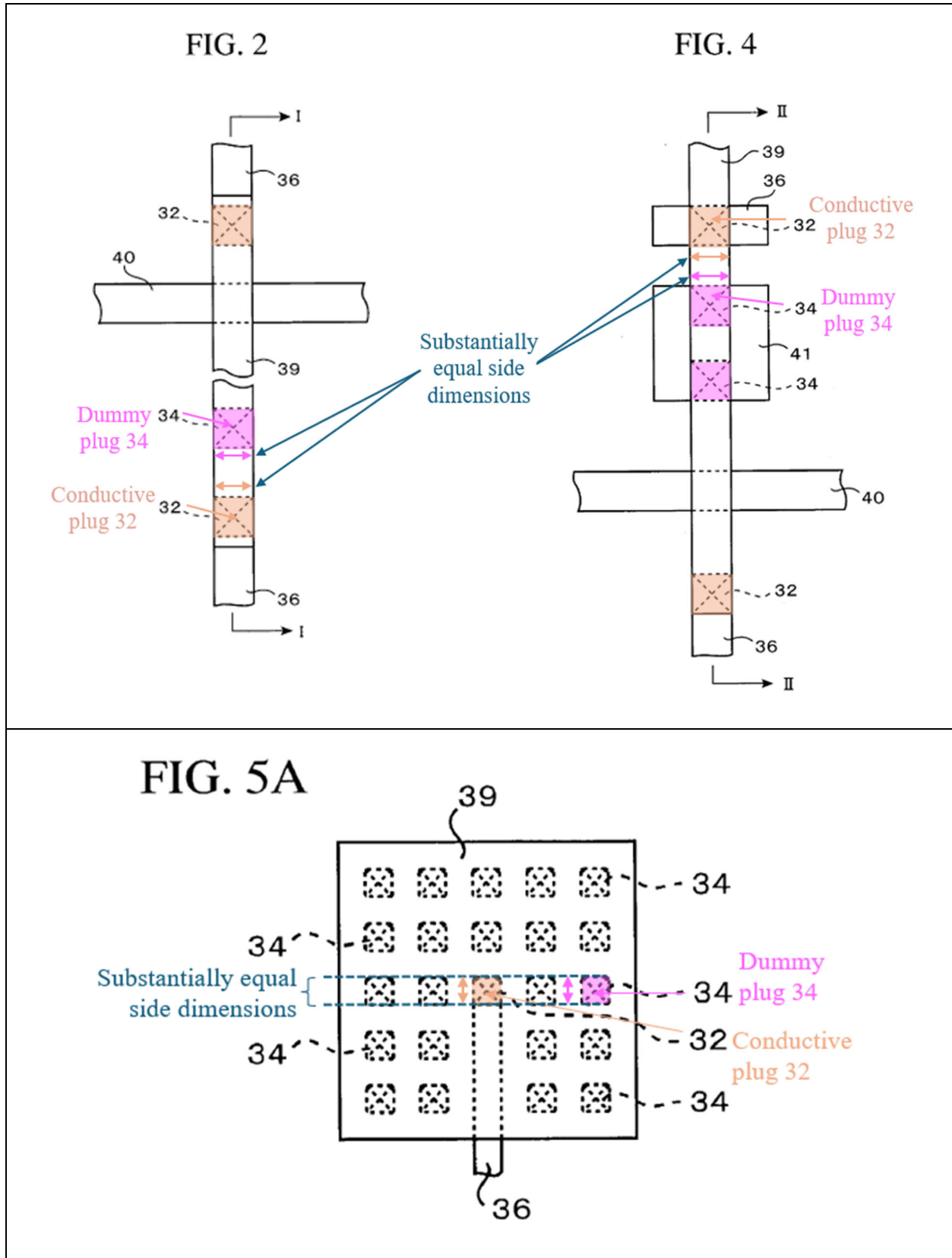
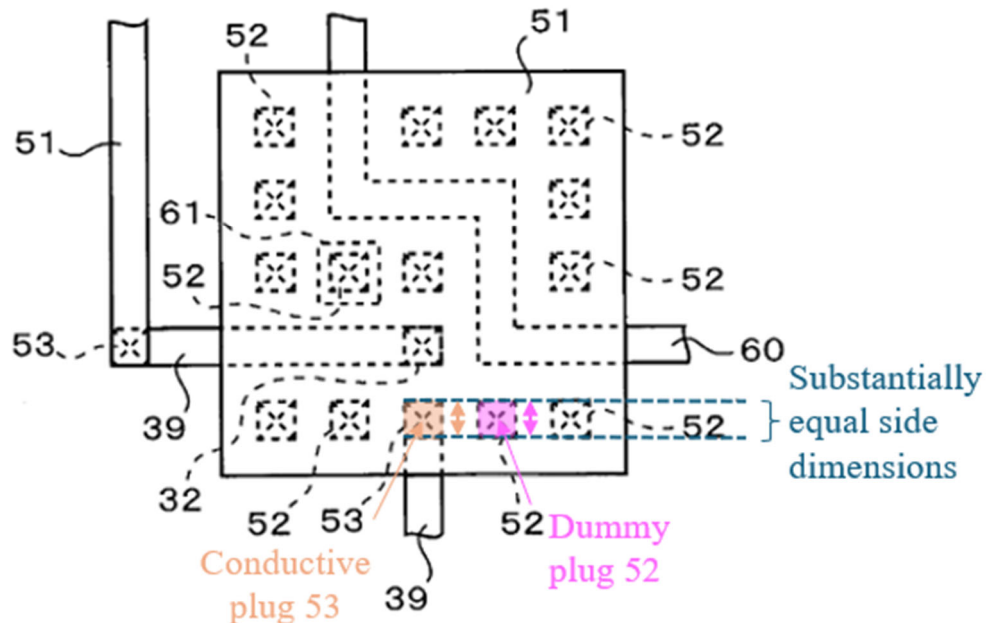


FIG. 9



TSMC-1003, ¶¶175-78.

7. Claim 24

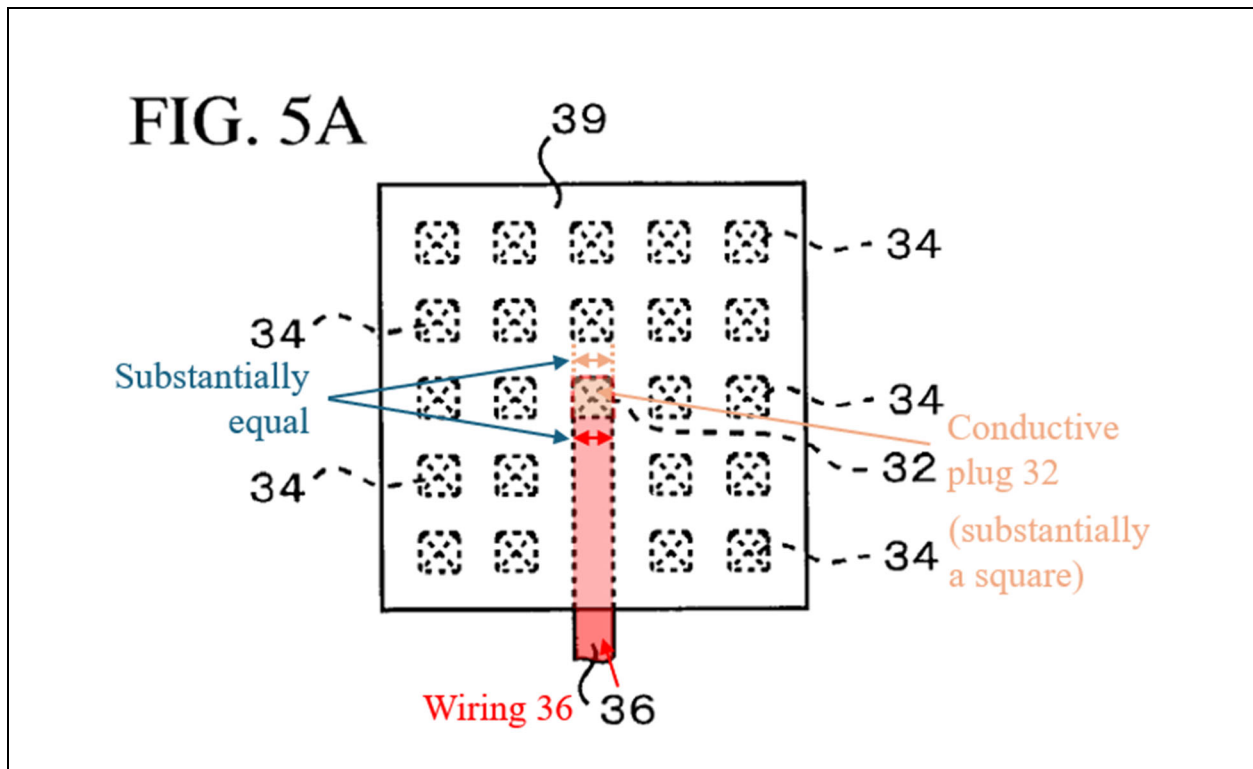
At least Watanabe's first-to-third and fifth embodiments satisfy claim 24.

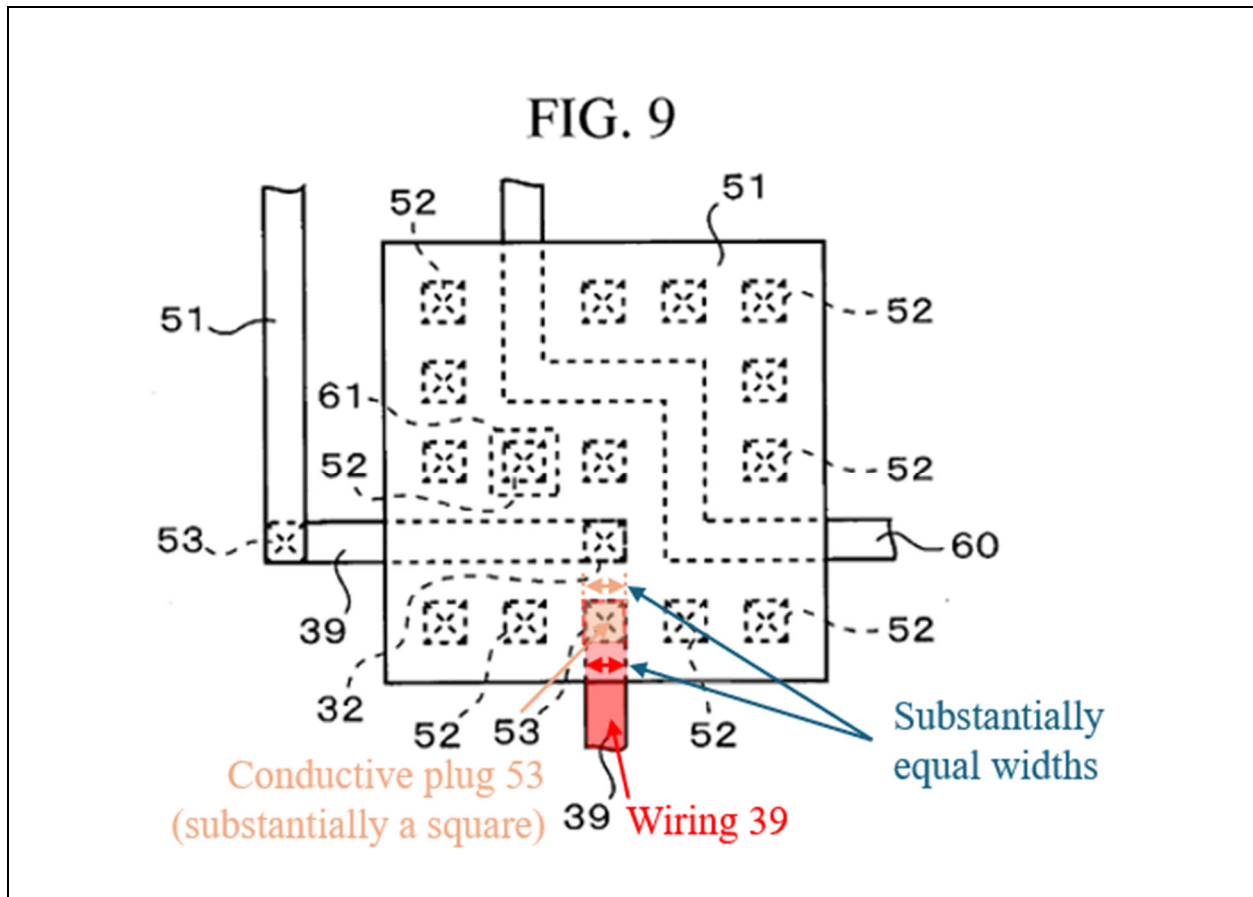
a) [24.a]

For each of its first-to-third and fifth embodiments, Watanabe discloses vias (e.g., plugs 32, 53) having a substantially square shape, as shown in Figures 2, 4, 5A-5C, and 9. *Supra*, §§VI.A.3-5; TSMC-1003, ¶¶179-183.

b) [24.b]

Watanabe's Figures 2, 4, 5A-5C, and 9 disclose conductive plugs 32 and 53 having side dimensions equal to the width of "first" wirings 36 and 39 (in first-to-third and fifth embodiments, respectively). TSMC-1004, Figs. 2, 4, 5A-5C, 9; TSMC-1003, ¶¶184-87. Figures 5A and 9 are shown below:





TSMC-1003, ¶¶186.

8. Claim 27

Applicable to its first-to-third and fifth embodiments, Watanabe discloses that the via-to-dummy via spacing is substantially equal to a minimum interconnect width. TSMC-1003, ¶¶188-194. Figure 14 discloses wiring 36 as the first interconnect layer above the MOSFET devices, and a POSITA understood that the wiring layer closest to the MOSFET devices needs to be spaced at the minimum interconnect width to maximize wiring density and minimize parasitic capacitance. See TSMC-1012, 34 (“[T]he lower wiring levels are at a minimum possible pitch

and thickness to minimize capacitance and maximize wiring density.”); TSMC-1003, ¶192.

Watanabe's Figures 4 and 17 disclose conductive plugs 32 on wiring 36, where the wiring 36 width (representing a minimum interconnect width, as noted above) is equal to the spacing between conductive plug 32 and adjacent dummy plug 34, as illustrated below:

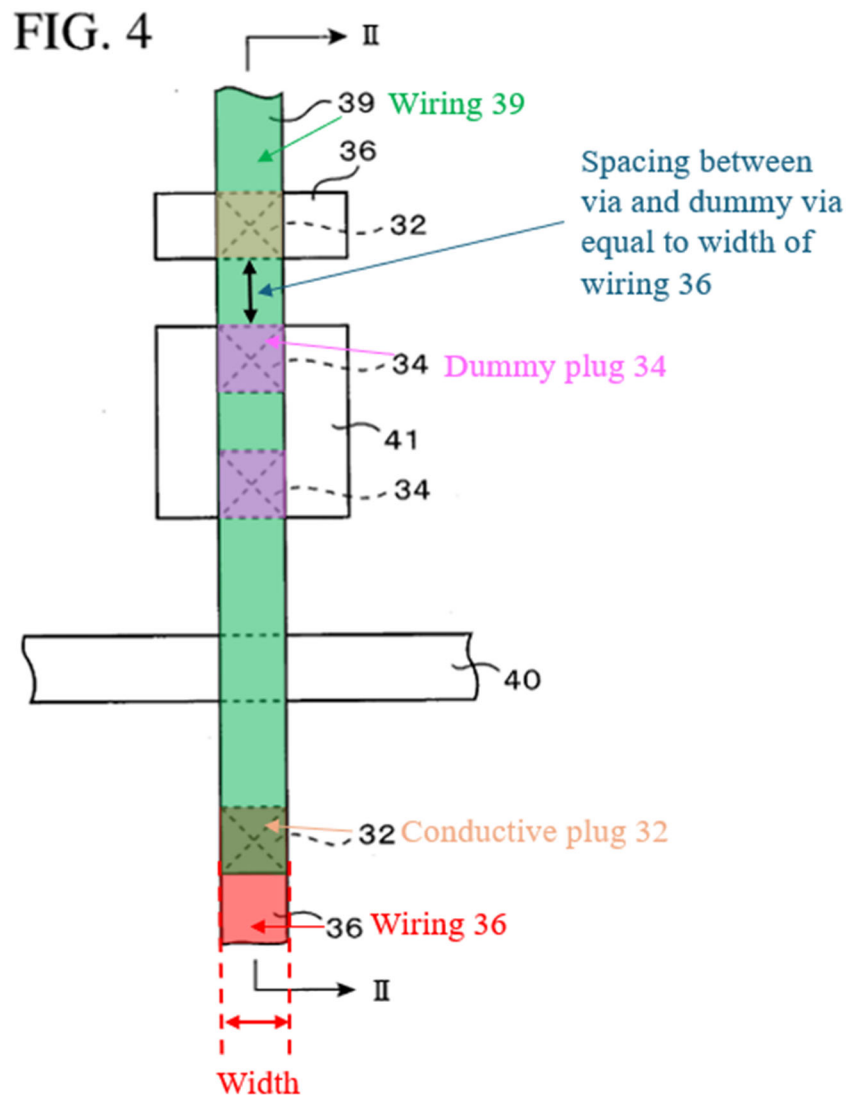
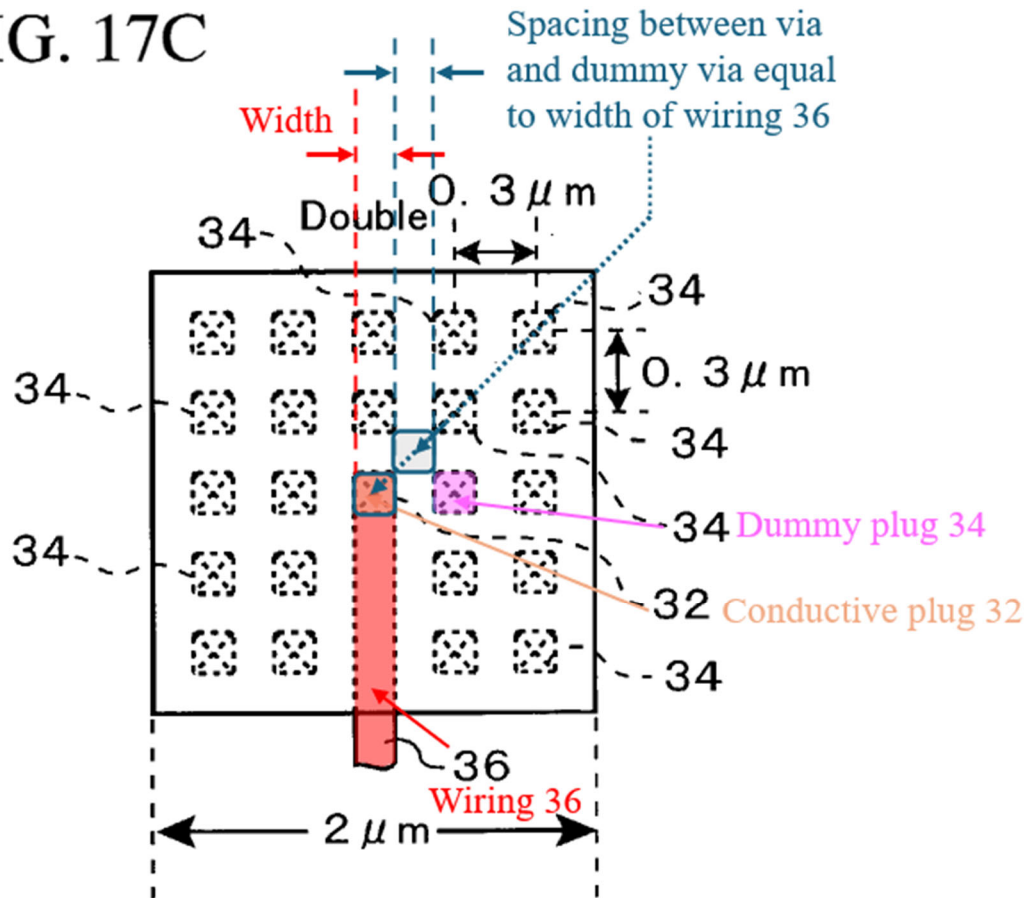


FIG. 17C



TSMC-1003, ¶¶193-194. A POSITA would thus have understood that Watanabe teaches a distance between vias (e.g., plugs 32) and dummy vias (e.g., dummy plugs 34) that is substantially equal to a minimum interconnect width. *Id.*

B. Ground 1B: Claim 27 Is Obvious over Watanabe

In addition to being anticipated, claim 27 is also obvious over Watanabe. TSMC-1003, ¶¶195-204.

1. Claim 27

Watanabe teaches that reducing the pitch (p_2) between conductive plug 32 and adjacent dummy conductive plug 34 to the minimum amount is desirable for

improving stress migration resistance. TSMC-1004, ¶¶[0032]-[0033], [0086]-[0087], [0190]-[0191], Figs. 15A-18; TSMC-1003, ¶197. Specifically, Watanabe's simulations teach that the stress difference ($\Delta\sigma$)—which is indicative of stress-migration susceptibility—generally decreases as the pitch p_2 decreases, with good results shown below 1 μm , and especially below 0.6 μm . *Id.*

Furthermore, Watanabe recognizes the general trend and requirement for miniaturization and increasing integration density in semiconductor devices, as well as maintaining adequate mechanical strength of the device, which are likewise achieved by minimizing the spacing between elements, such as between vias and dummy vias. TSMC-1004, ¶¶[0015], [0028]-[0033], [0186]; TSMC-1003, ¶¶197-200. The edge-to-edge spacing of conductive plug 32 to adjacent dummy conductive plug 34 is reduced as the pitch (center-to-center spacing) is reduced. TSMC-1003, ¶¶197-200.

A POSITA designing a semiconductor device, motivated by Watanabe's teaching to minimize the via-to-dummy-via pitch (p_2) for improved reliability and mechanical strength, and simultaneously driven by the standard industry goal of maximizing layout density (as acknowledged by Watanabe (TSMC-1004, ¶[0005]; *see also* TSMC-1012, 34)), would place dummy plug 34 as close as possible to conductive plug 32. TSMC-1003, ¶201.

The minimum possible spacing between vias in a semiconductor layout is dictated by the design rules for the specific manufacturing process technology node being used. *Id.*, ¶202. These design rules define minimum feature sizes and minimum spacing requirements to ensure manufacturability and avoid electrical shorts, other failures, and undesirable “crosstalk” resulting from parasitic capacitances and the like. *Id.*; see TSMC-1034, 585 (discussing arranging multilevel interconnect structures in tiers and using finest metal-pitch allowed by design rules being employed for the tiers). Therefore, it was obvious when seeking to implement Watanabe’s stress-reducing and mechanically-enhancing dummy vias in the most space-efficient manner while maximizing their effectiveness (by minimizing the pitch/effective interconnect length (*see* TSMC-1004, ¶¶[0020]-[0022], [0026]-[0028], [0074]-[0076], [0083]-[0092], [0108])) to place dummy conductive plug 34 adjacent to conductive plug 32 at the minimum spacing allowed by the applicable design rules. TSMC-1003, ¶202.

A POSITA knew that design rules for minimum spacing between features (like vias) and minimum widths of features (like interconnects) are intrinsically linked within a given technology node; they typically scale together since they are dictated by the resolution implementable at a given interconnect level and/or for a given planarization uniformity. *Id.*, ¶203. Placing the dummy via at the minimum allowed spacing would naturally result in a distance “substantially equal to” the

minimum interconnect width for that technology generation at that interconnect level, especially given that the limits for both are typically limited by the lithography resolution for a given level/surface planarization. *Id.*

A POSITA would have had a reasonable expectation of success in achieving improved stress migration resistance (which Watanabe teaches as a result of closer spacing/lower “effective wiring lengths”), as well as improved processing and high layout density, by employing this minimum design rule spacing. *Id.*, ¶204. By definition, this is the minimum spacing that could be reliably implemented and achieved for a given manufacturing process, ensuring that it could be attained. *Id.*

C. Ground 2: Claim 23 Is Obvious Over Watanabe and Iizuka

Watanabe and Iizuka render claim 23 obvious. TSMC-1003, ¶¶205-21.

1. Iizuka

Because Iizuka is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the ’623 patent purports to address (e.g., interconnect reliability), Iizuka is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1008, 1:7-14; 2:39-45; TSMC-1003, ¶¶85-87.

Iizuka describes methods for manufacturing semiconductor devices, focused on improving the filling of small-diameter via holes to form reliable conductive plugs between interconnect layers. TSMC-1008, Abstract, 1:7-14, 2:39-45. Iizuka teaches common via-hole planar shapes: “the opening of the via-hole may have

any configuration, such as a **square**, rectangle or **circle**.” *Id.*, 9:45-47; *see also id.*, 6:60-63, Fig. 5A (disclosing “diameter” of via). Iizuka thus confirms that vias/dummy vias can have various planar shapes, and that selecting a specific shape (e.g., as between square and circular) was a simple design choice. TSMC-1008, 9:45-47; TSMC-1003, ¶85. Circular (or square) via holes result in vias having substantially circular (or square) cross-sections. TSMC-1003, ¶¶85-86.

2. Claim 23

a) [23.a]

Watanabe’s simulation model describes conductive plugs 32 (vias) as a “circular cylinder,” thus disclosing circular vias. TSMC-1004, ¶[0083]; TSMC-1003, ¶209.

Iizuka confirms that vias can have various planar shapes, such as square, rectangle, or **circle**, and that selecting a specific shape was a simple design choice. TSMC-1008, 9:45-47; TSMC-1003, ¶210. Iizuka’s description of via-hole 6 having a “diameter” (TSMC-1008, 6:60-63) similarly discloses a circular via shape. TSMC-1003, ¶210.

It was obvious to implement Watanabe’s conductive plugs 32/53 with a substantially circular shape given Iizuka’s teaching that circular vias were a known, interchangeable design alternative, as well as the widespread knowledge of

circular-shaped vias at the time. *Infra*, §VI.C.3; TSMC-1003, ¶211; TSMC-1005, Figs. 19A, 22A; TSMC-1013, 8:48-52; TSMC-1014, ¶[0091].

b) [23.b]

Watanabe's plan-view figures consistently disclose vias (conductive plugs 32, 53) that span the full width of the first interconnect (e.g., first wirings 36, 39) to which the bottom end of the via connects. TSMC-1004, Figs. 2, 4, 9; TSMC-1003, ¶213. A POSITA, having found it obvious to implement vias with a circular shape (as discussed for element [23.a]), would further have found it obvious to maintain this full-width contact by making the diameter of circular conductive plugs 32, 53 substantially equal to the width of the underlying wiring (e.g., wirings 36, 39). TSMC-1003, ¶¶214-15. Such sizing is a standard design practice that maximizes the electrical contact area of circular vias and ensures a robust connection between a via and an underlying interconnect line. *Id.*

The expectation of success in achieving such a dimensionally-matched connection would have been high, as this represents a routine design for reliable via-to-line interconnections. *Id.*, ¶215. A POSITA would simply have specified the vias to have the same size as the underlying interconnect line, and the standard manufacturing process would then build them as such. *Id.*

3. Combination of Watanabe and Iizuka

Watanabe's simulation model describes its vias and dummy vias as "circular cylinders," thereby disclosing vias having circular cross-sections as alternatives to the square vias in Watanabe's figures. TSMC-1004, ¶[0083]; *supra*, §VI.C.2.(a). Iizuka's teaching that vias can be circular, square, or rectangular confirms that a POSITA viewed these shapes as a finite number of readily interchangeable design choices given Iizuka's express teaching to this effect and a POSITA's general understanding. TSMC-1008, 9:45-47; *supra*, §VI.C.2.(a). It was thus obvious to implement Watanabe's conductive plugs 32/53 (as well as dummy plugs 34/52) with a substantially circular shape. TSMC-1003, ¶¶216-221.

Motivations for selecting a circular shape included simple design choice, advantages in manufacturing process control (e.g., more uniform etching and filling characteristics), more favorable stress distribution around a circular opening, design simplicity, and consistency with Watanabe's own simulation models. *Id.*, ¶¶217-18; TSMC-1038, 7:61-67.

A POSITA would have recognized that neither the electrical connection function of Watanabe's functional vias, nor the fundamental stress-relieving function of Watanabe's dummy vias, would be materially altered by adopting a circular cross-section versus a square. TSMC-1003, ¶¶218-20. The '623 patent

also does not teach any criticality as to the via/dummy via shape. *Id.*; *see also* TSMC-1002, 292-96 (Examiner noting no criticality for via shapes).

A POSITA would have expected success in implementing Watanabe's vias (both functional and dummy) with circular shapes. TSMC-1003, ¶221. Circular vias were standard in the industry, and Iizuka itself teaches circular vias and methods for successfully filling such via holes. *Id.* The choice of via shape was a routine design parameter, subject to routine optimization as noted by the Examiner during prosecution (TSMC-1002, 244-45, 292-96), and modifying Watanabe's square vias (or implementing its modeled circular vias) to be circular would not have involved any inventive step while being readily achievable using known fabrication techniques at the time. TSMC-1003, ¶221.

D. Ground 3: Claim 5 Is Obvious Over Watanabe, Iizuka, and Kurashima

Watanabe, Iizuka, and Kurashima render claim 5 obvious. TSMC-1003, ¶¶222-40.

1. Kurashima

Because Kurashima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Kurashima is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1011, 1:15-22, 1:49-67; TSMC-1003, ¶¶83-84.

Kurashima enhances durability of insulating films, particularly low-relative-dielectric-constant films, against CMP-related stresses to prevent film peeling.

TSMC-1011, 1:15-22, 1:49-67. Kurashima teaches forming in parallel Cu-wire 9 and Cu-dummy wire 10 in insulating film 4. *Id.*, 4:50-6:32, Figs. 1B-1D, 3A-3B.

Then a second-layer Cu-wire 16 is formed connecting to first-layer Cu-wire 9. *Id.*, 6:58-8:35, Figs. 2A-3A. Concurrently, a second-layer Cu-dummy wire 17 is formed in contact with first-layer Cu-dummy wire 10, providing a reinforcing effect and enhancing interfacial adhesion and CMP durability, to reduce peeling of layers. *Id.*, 6:11-32; 6:58-8:54, 9:16-23, Figs. 2C, 3A. Kurashima teaches forming functional wires and dummy wires with substantially the same width:

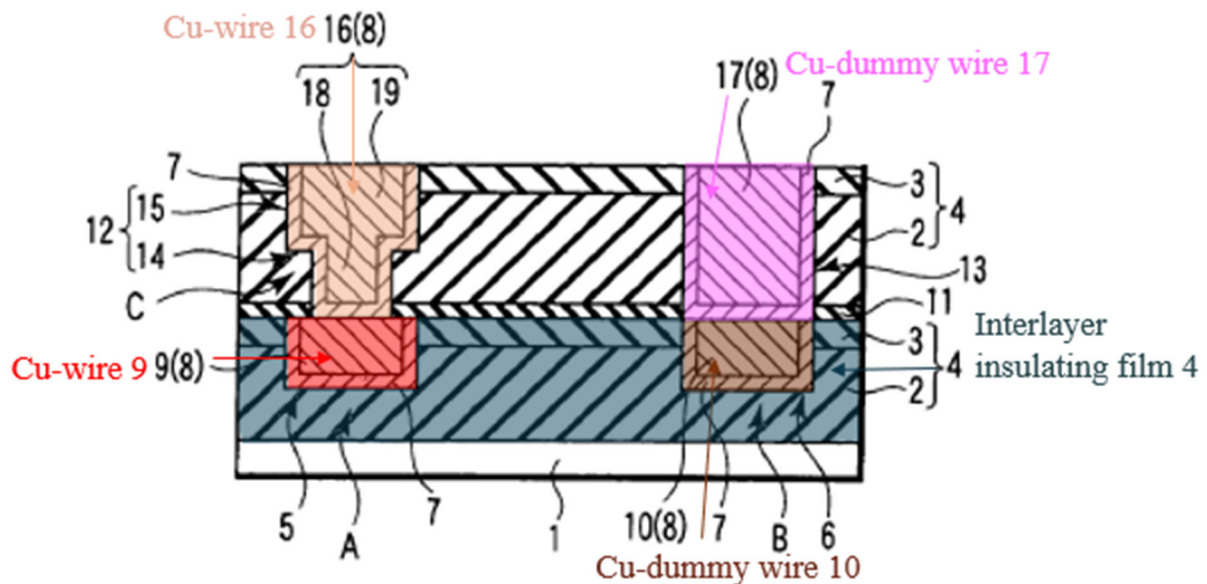


FIG. 3A

Id., 4:50-63, Figs. 1D, 3A-3B; TSMC-1003, ¶83.

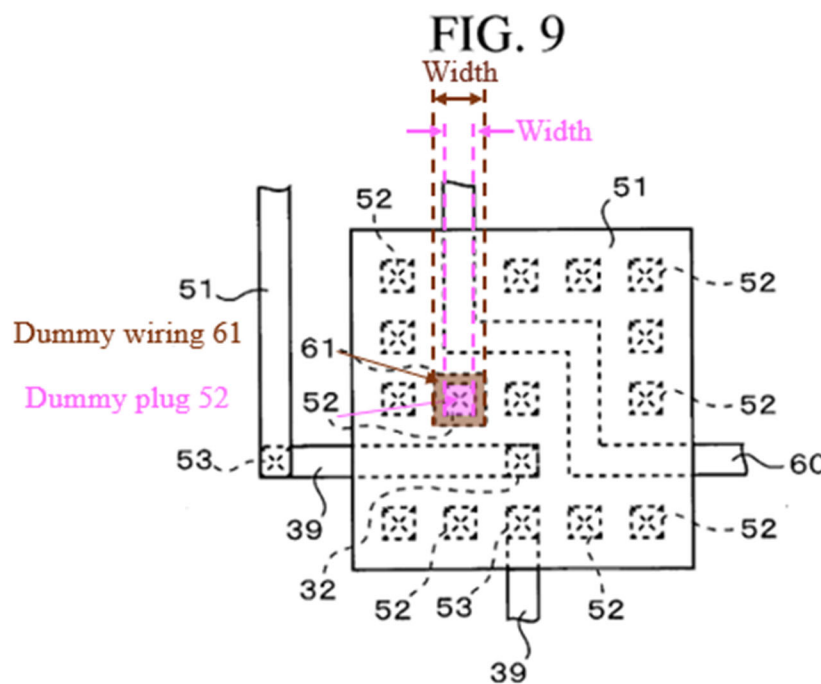
2. Claim 5

a) [5.a]

For the same reasons discussed for claim 23 regarding conductive plugs 32/53, it was obvious, based on Watanabe's own simulation model and Iizuka's teaching that via shapes (circular, square, rectangular) were interchangeable design options, to form Watanabe's dummy plugs 34/52 (i.e., dummy vias) with a substantially circular shape in a plan view. *Supra*, §§VI.C.2-3; TSMC-1003, ¶¶224-27.

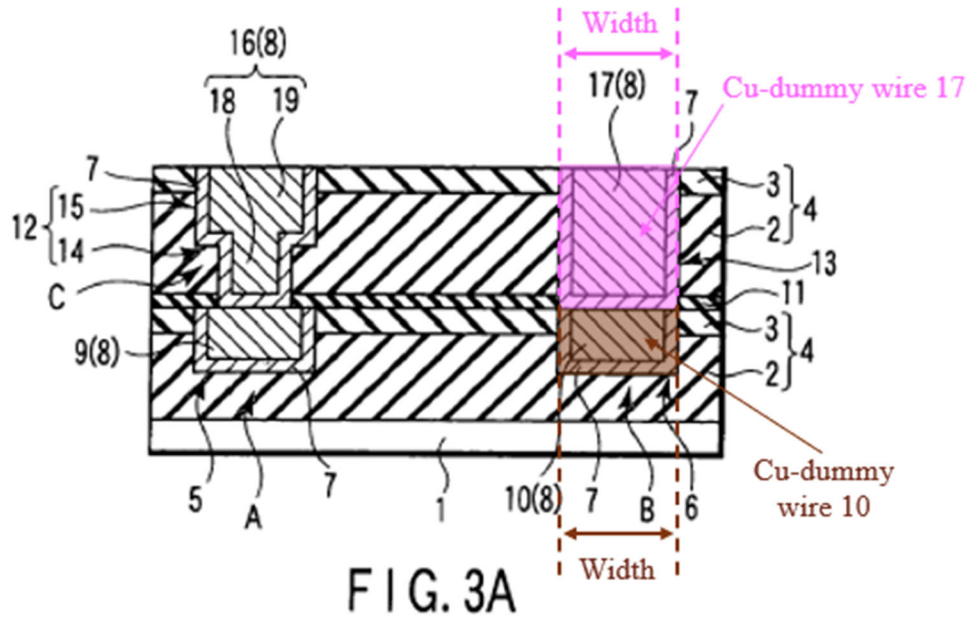
b) [5.b]

Watanabe’s fifth embodiment discloses dummy plug 52 (“dummy via”) having a width slightly smaller than a width of dummy wiring 61 (“first dummy interconnect”) to which it connects:



TSMC-1004, ¶[0127], Fig. 9; TSMC-1003, ¶229.

Kurashima teaches dummy wire 17 (dummy via) and underlying Cu-dummy wire 10 (dummy interconnect) having the same width (TSMC-1011, Fig. 3A; TSMC-1003, ¶¶230):



For the reasons discussed below, it was obvious, in view of Kurashima, for Watanabe's dummy plug 52 ("dummy via") to have a diameter/width matching the width of underlying dummy wiring 61 ("first dummy interconnect"). *Infra*, §VI.D.3.

3. Combination of Watanabe, Iizuka, and Kurashima

A POSITA was motivated to implement circular dummy vias in Watanabe with a diameter that matches a width of an underlying dummy interconnect to ensure a secure connection between the dummy via and dummy interconnect while

minimizing the dummy interconnect/wiring footprint and undesired parasitic capacitance and cross-talk with adjacent, active interconnects/wirings. TSMC-1003, ¶¶231-37. For example, the desire to reduce parasitic capacitance and crosstalk motivated reducing dummy wiring 61's width to match that of wirings 39 and 60 to thereby increase the spacing between dummy wiring 61 and wiring 60. TSMC-1004, ¶[0034]; TSMC-1003, ¶¶232-34. Doing so would result in wiring 61's width also matching that of dummy plugs 52 since Watanabe teaches dummy plugs having the same width as wirings 39 and 60. TSMC-1003, ¶234.

As another approach, dummy plug 52 could be widened to match the larger dimension of dummy wiring 61 shown in Watanabe's Figure 9. This modification would improve the interfacial adhesion between the two by increasing their contact area, as taught by Kurashima. TSMC-1011, 6:11-32; 6:58-8:54, 9:16-23, Figs. 2C, 3A; TSMC-1003, ¶235.

Either approach described above (widening dummy plug 52 to match wiring 61's width, or reducing wiring 61's width to match dummy plug 52) avoids sharp corners where the dummy plug connects to the dummy wiring, having the benefit of reducing stress concentration at their junction. TSMC-1003, ¶236.

With Watanabe and Iizuka both teaching circular vias (TSMC-1004, ¶[0083]; TSMC-1008, 9:45-47), the resulting combination would be a circular-

shaped dummy via (dummy plug 52) having a diameter equal to the width of the dummy interconnect (dummy wiring 61). TSMC-1003, ¶237.

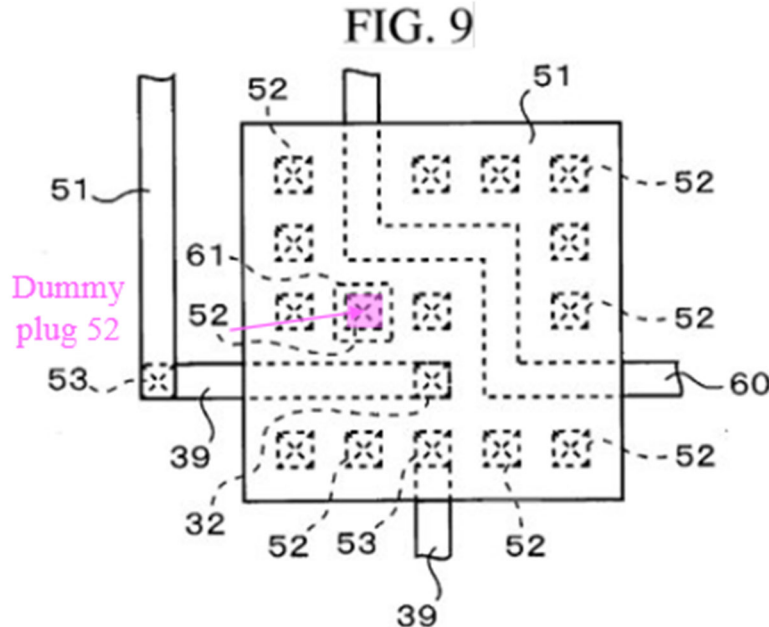
A POSITA would have expected success when implementing Watanabe's dummy vias with circular shapes. *Supra*, §VI.C.3; TSMC-1003, ¶238. Slightly modifying the diameter of the resulting circular via to be equal to a width of the dummy interconnect would have merely involved routine, known changes as demonstrated by Kurashima which were achievable with Watanabe's existing manufacturing processes. TSMC-1003, ¶¶238-40. Indeed, such via/interconnect sizing was a standard design practice and thus would have been expected to succeed. *Id.*

E. Ground 4: Claim 6 Is Obvious Over Watanabe and Kurashima

Watanabe and Kurashima render claim 6 obvious. TSMC-1003, ¶¶241-52.

1. [6.a]

Watanabe's Figure 9 (fifth embodiment) discloses dummy plug 52 ("dummy via") with a square planar shape:



TSMC-1004, Fig. 9; TSMC-1003, ¶243. Moreover, a POSITA understood the common nature of square-shaped vias. TSMC-1003, ¶243.

2. [6.b]

As discussed *supra*, §VI.D.2.(b), Watanabe's Figure 9 discloses dummy plug 52 ("dummy via") having a width slightly smaller than a width of dummy wiring 61 ("first dummy interconnect") (TSMC-1004, ¶[0127], Fig. 9), and Kurashima teaches dummy wire 17 ("dummy via") and underlying Cu-dummy wire 10 ("first dummy interconnect") having the same width (TSMC-1011, Fig. 3A; TSMC-1003, ¶¶245-46).

FIG. 9

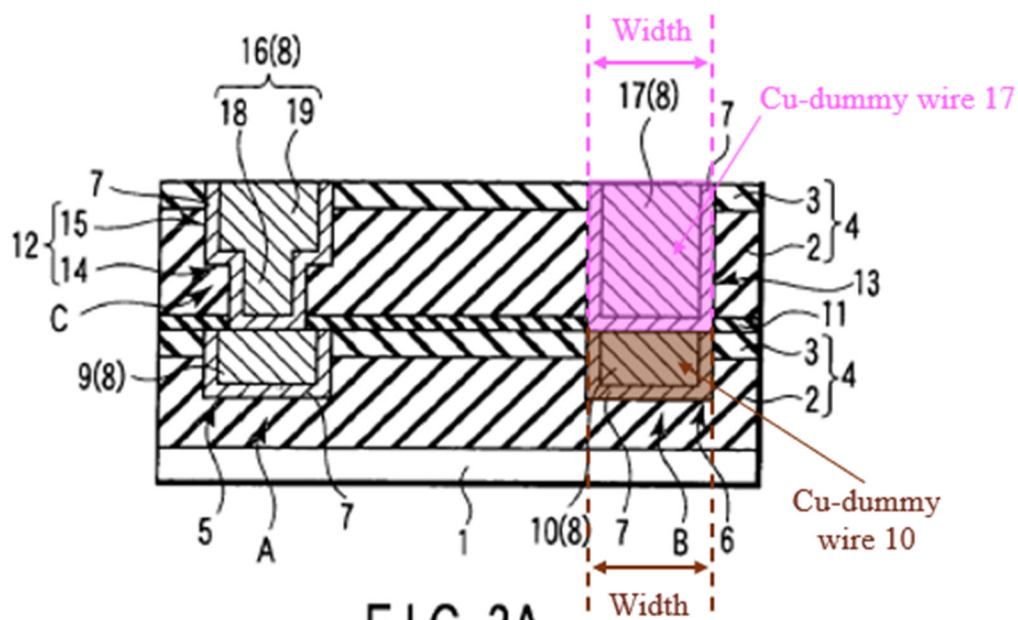
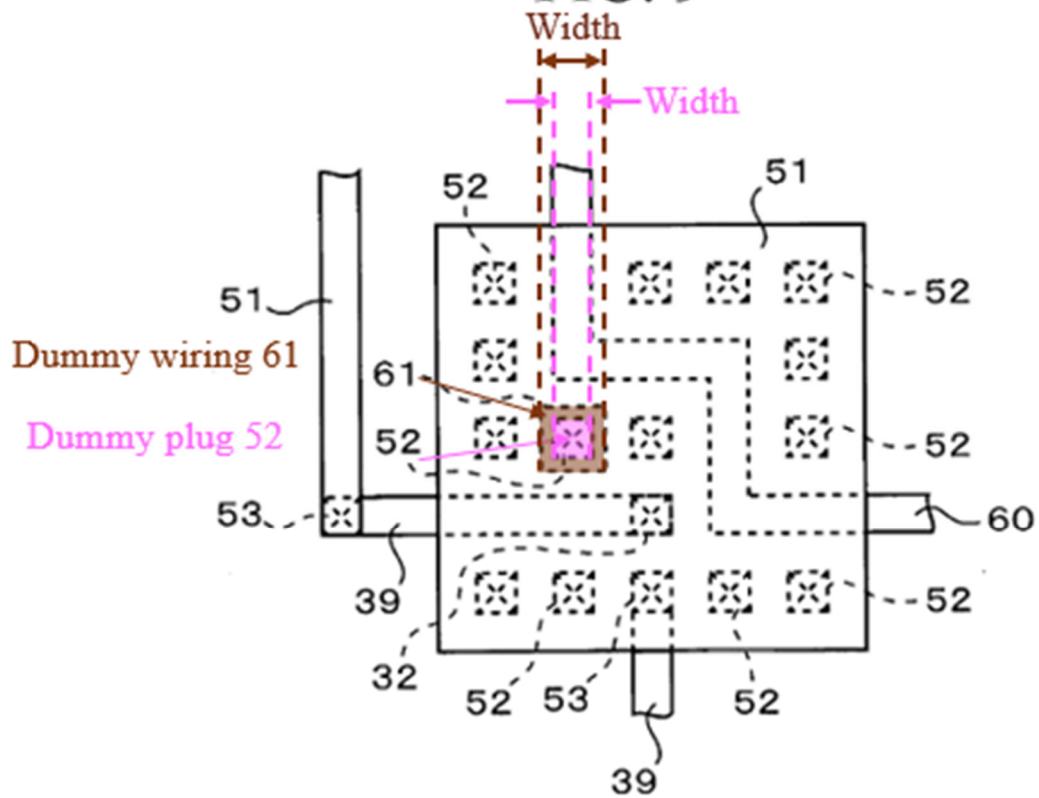


FIG. 3A

For the same reasons discussed for claim 5, it was obvious, based on Kurashima, for Watanabe's dummy plug 52 to have a width matching that of underlying dummy wiring 61 (e.g., to ensure a secure connection while minimizing the dummy wiring footprint and undesired parasitic capacitance and cross-talk with adjacent, active wirings), and there would have been a reasonable expectation of success for doing so. *Supra*, §VI.D.3; TSMC-1003, ¶¶247-52.

F. Ground 5: Claims 29-30 Are Obvious Over Watanabe and Nasu

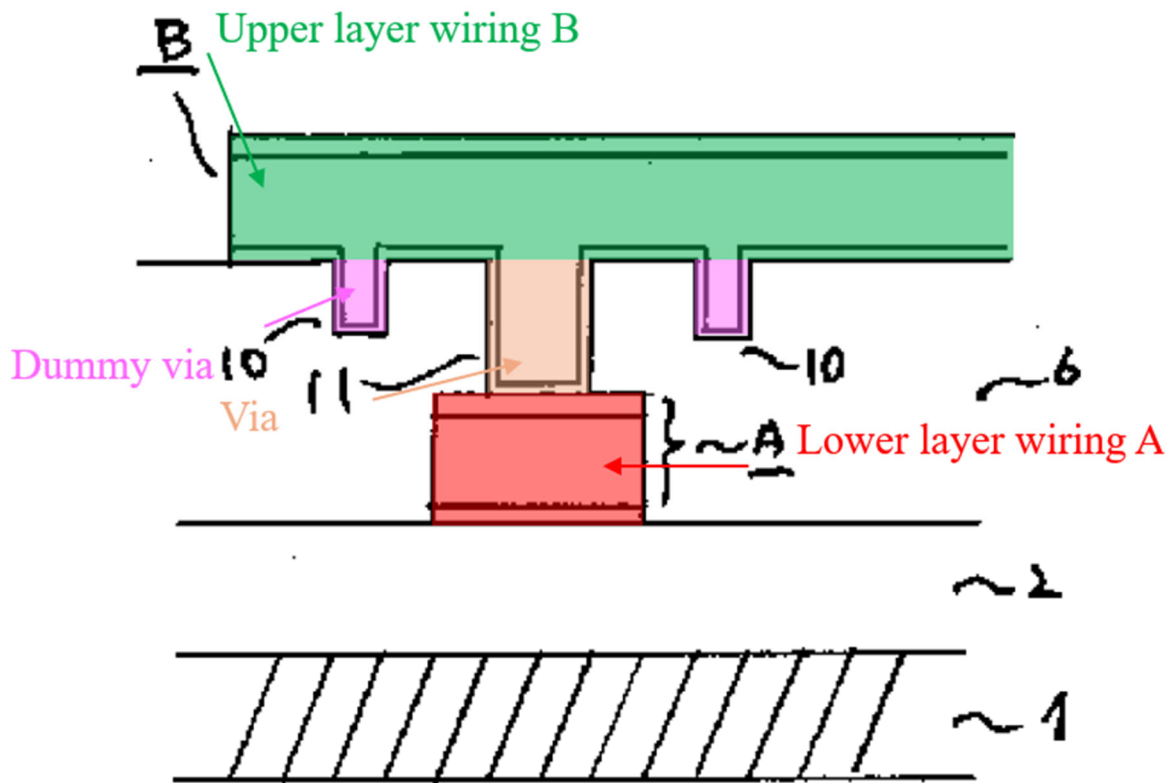
Watanabe and Nasu render claims 29-30 obvious. TSMC-1003, ¶¶253-75.

1. Nasu

Because Nasu is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Nasu is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1032, Abstract, ¶¶[0001]-[0002], [0013]; TSMC-1003, ¶¶88-93.

Nasu discloses a wiring structure that includes lower and upper wirings, where upper layer wiring B connects to lower wiring A through the via in via hole 11. TSMC-1032, ¶¶[0022]-[0028], Figs. 1, 5. To address electromigration, Nasu teaches forming one or more dummy vias in dummy holes 10 near via hole 11, to serve as a supply source for Al or Cu atoms, thereby enhancing EM resistance. *Id.*, Abstract, ¶¶[0012]-[0013], Figs. 2-3; TSMC-1003, ¶88.

Nasu forms dummy via holes 10 with a smaller diameter than via hole 11 using typical photoresist patterning. TSMC-1032, ¶¶[0023] (e.g., dummy hole pattern 8 having a diameter of 0.30 μm or less, and hole pattern 9 having a diameter of 0.45 μm), Fig. 2; TSMC-1003, ¶¶89-91. Simultaneously etching insulating layer 6 through photoresist hole patterns 8 and 9 results in dummy holes 10 and via hole 11, where dummy holes 10 are shallower (less deep) due to the micro-loading effect, as seen in Figure 5:



TSMC-1032, ¶¶[0024], [0027]-[0028], Figs. 2-3, 5; TSMC-1003, ¶¶91-92. The dummy vias in holes 10 do not reach lower wiring A. *Id.*

2. Claim 29

a) [29.a]

Watanabe discloses vias (conductive plug 32) and dummy vias (dummy plugs 34). TSMC-1004, Figs. 1, 3; *supra*, §§VI.A.2.(a).(6)-(7). Watanabe’s simulation model teaches circular vias and dummy vias. *Supra*, §§VI.C.2.(a), VI.D.2.(a); TSMC-1003, ¶255.

Nasu also describes vias and dummy vias having specific “diameters.” TSMC-1032, ¶[0023]; TSMC-1003, ¶256. Nasu’s consistent reference to the “diameter” of both via hole pattern 9 and dummy hole pattern 8 indicates that these via openings, and thus the vias formed within them, are circular in their planar shape. *Id.*

Given Watanabe’s own use of circular models, Nasu’s teaching of circular vias, and the art’s general recognition of circular-shaped vias (TSMC-1008, 9:45-47), it was obvious to implement both the functional via and the dummy via of Watanabe with substantially circular planar shapes. *Supra*, §§VI.C.3; TSMC-1003, ¶¶255, 257. The motivation would be design choice, manufacturing and stress benefits, and/or consistency with Watanabe’s simulation models, with a high expectation of success as circular vias were standard. *Id.*

b) [29.b]

Nasu teaches forming dummy hole pattern 8 with diameters (e.g., 0.30 μm or less) smaller than the diameter of via hole pattern 9 (e.g., 0.45 μm). TSMC-1032, ¶¶[0023], [0028]; TSMC-1003, ¶¶258-60. The obviousness of applying this teaching to Watanabe's structure is explained *infra*, §VI.F.4. TSMC-1003, ¶¶261-62.

3. Claim 30

a) [30.a]

Watanabe's plan view figures (e.g., Figures 2, 4, 5A-5C, 9) consistently disclose square vias and dummy vias. TSMC-1004, Figs. 2, 4, 5A-5C, 9; TSMC-1003, ¶264. Nasu also discloses square-shaped via holes 11 and square dummy holes 10:

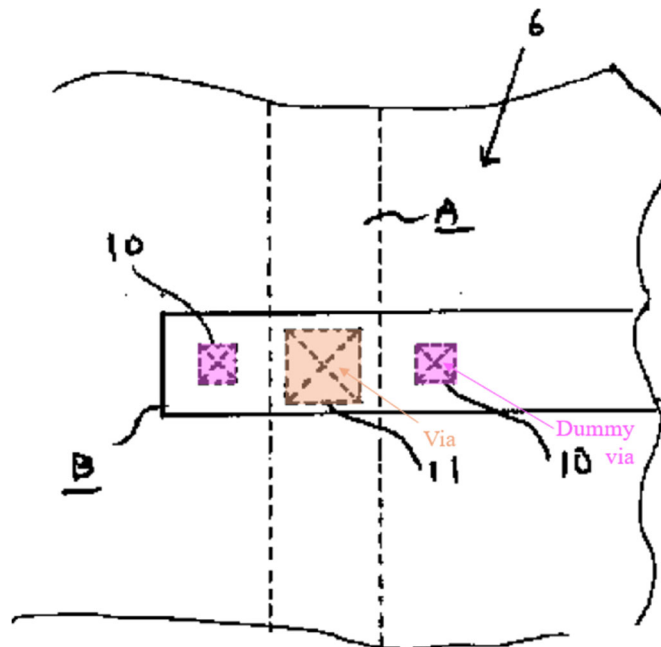


FIG. 6

TSMC-1032, Fig. 6, TSMC-1003, ¶265. And square vias and dummy vias were well-known. *Supra*, §§VI.A.4-5, VI.C.1-3.

b) [30.b]

Nasu discloses dummy vias 10 smaller than via 11:

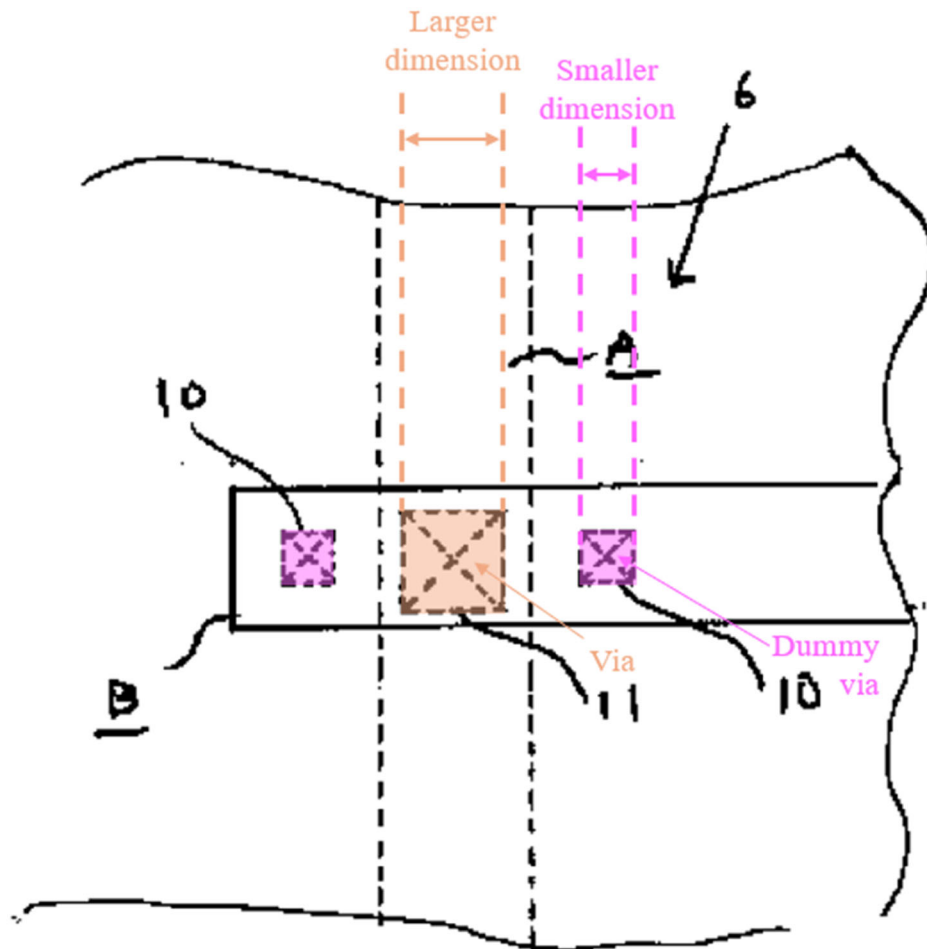


FIG. 6

TSMC-1032, ¶¶[0023], [0028], Fig. 6; TSMC-1003, ¶267. Nasu's teachings on relative sizing applied regardless of whether the via is circular or square. TSMC-1003, ¶267.

If both the via and dummy via are square as in Watanabe, and the dummy via is made dimensionally smaller than the functional via per Nasu's teaching, then a side of the dummy via would necessarily be smaller than a side of the functional via. *Id.*, ¶268.

4. Combination of Watanabe and Nasu

A POSITA would have been motivated to combine the teachings of Watanabe and Nasu to enhance the reliability of multilayer interconnect structures. TSMC-1003, ¶269. Both references address reliability issues by incorporating dummy vias near functional vias. *Id.*; *supra*, §§VI.A.1, VI.F.1.

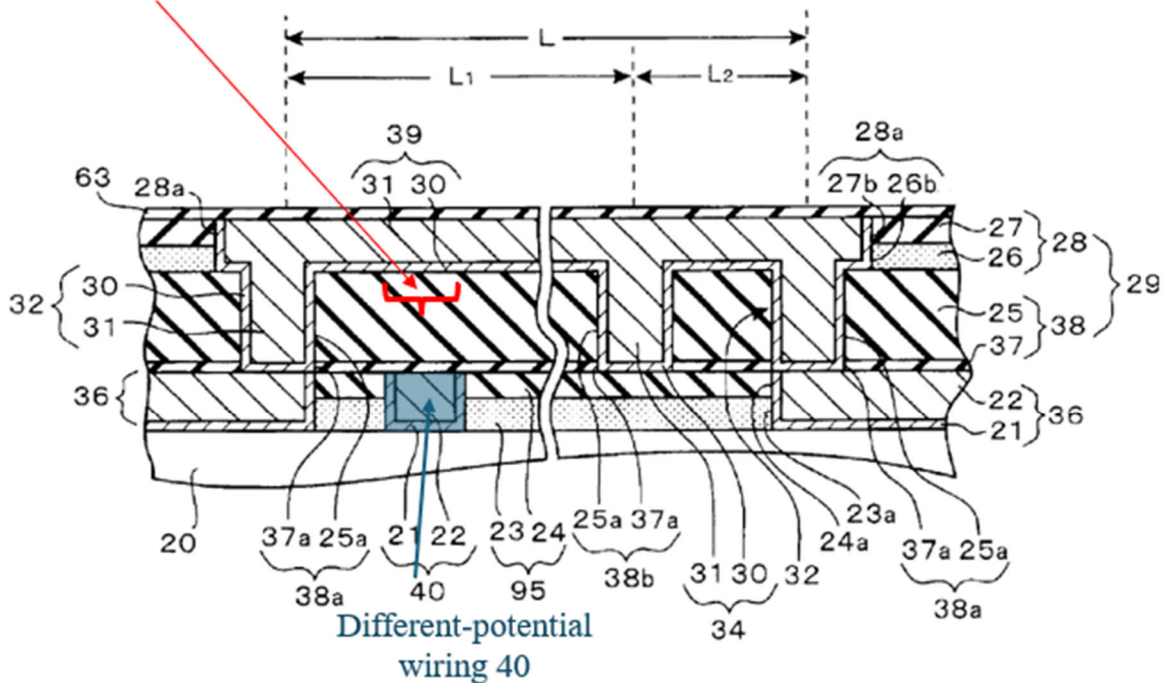
Regarding Nasu's smaller-diameter dummy vias as compared to functional vias, Nasu explains that a smaller dimension for the dummy via hole(s) results in shallower dummy features when the holes for the vias and dummy vias are simultaneously etched. TSMC-1032, ¶¶[0024], [0028], Fig. 3; TSMC-1003, ¶270. Due to the slower etching, the dummy vias do not reach the lower wiring while still serving as "material reservoirs." *Id.*

It was obvious to implement Nasu's smaller-sized dummy vias (whether circular or square) in Watanabe's structure. TSMC-1003, ¶271. Nasu's approach helps optimize layout density, since dummy vias having a shallower depth can be formed/placed in areas over lower-level interconnects that cannot be electrically connected to the upper-level interconnect from which the dummy vias depend.

Watanabe's Figure 1 is illustrative, where lower interconnect 40 is intended to be electrically isolated from interconnects 36 and 39 (TSMC-1004, ¶[0079]):

Shallower dummy vias
formed per Nasu (over but
not connecting to wiring 40)

FIG. 1



TSMC-1003, ¶271. A similar benefit can be achieved in Watanabe's Figure 9 embodiment by allowing dummy plugs to be located over underlying interconnect 60. *Id.*

As further motivation, smaller-diameter dummy vias better attract vacancies from the interconnect due to the higher stress gradient generated from the smaller dummy via diameter/width. *Id.*, ¶¶272-74; TSMC-1009, ¶[0088]; TSMC-1029, 208; TSMC-1036, 315, 319; TSMC-1037, 163, 165, Figs. 8, 14. Thus, Nasu's approach would have benefited Watanabe's device by expanding the ability to

create reservoir structures as taught by Nasu both to provide a source of metal atoms and to collect vacancies. TSMC-1003, ¶274.

Because dummy vias by definition carry no current, they are free to be made smaller than the active vias. *Id.*, ¶272. Fabricating vias/dummy vias of different, controlled sizes and shapes in the same device was a known capability as demonstrated by Nasu and Watanabe, leading to a high expectation of success in implementing such a combination to arrive at claims 29-30. *Id.*, ¶275.

G. Ground 6: Claim 31 Is Obvious Over Watanabe and Fujii

Watanabe and Fujii render claim 31 obvious. *Id.*, ¶¶276-89.

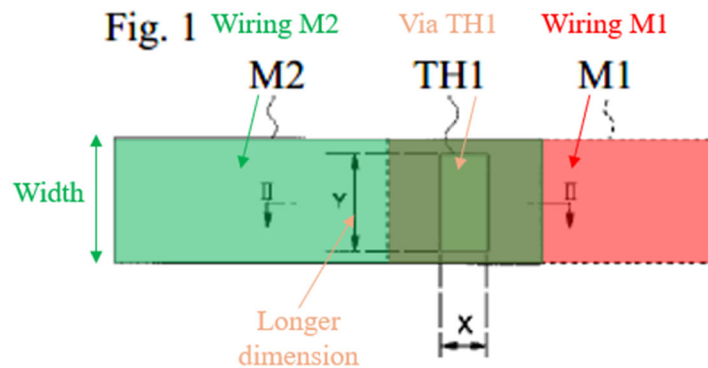
1. Fujii

Because Fujii is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Fujii is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1030, Abstract, ¶¶[0001], [0009]-[0012]; TSMC-1003, ¶¶94-96.

Fujii improves electromigration (“EM”) resistance in connection holes (TH1, TH2) (i.e., vias) for interlayer wiring. TSMC-1030, Abstract. Specifically, Fujii teaches rectangular-shaped vias having a longer dimension in the direction orthogonal to current flow (i.e., parallel to the interconnect width), so that current approaches the longer side dimension of the vias. *Id.*, ¶¶[0016], [0064]-[0066]; TSMC-1003, ¶94. This configuration allows current to be dispersed across the

longer width of the via, thereby suppressing local high-current density. *Id.* The larger surface perpendicular to the current flow direction distributes the current across connection hole TH1 and reduces metal atom movement out of connection hole TH1, thus preventing void formation around the connection hole/via. *Id.*

Fujii's Figure 1 discloses via TH1 having a rectangular plan view, with its longer dimension (Y) parallel to the width of upper-level wiring M2:



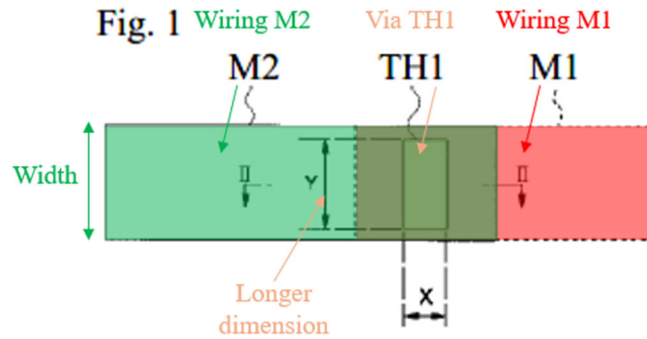
TSMC-1003, ¶95.

2. Claim 31

a) [31.a]

Watanabe's Figures 2, 4, and 9 (first, second and fifth embodiments) disclose dummy plugs 34/52 ("dummy via") having a substantially square planar shape. TSMC-1004, Figs. 2, 4, 9; TSMC-1003, ¶278.

Fujii teaches forming a rectangular connection hole/via having its longer dimension (Y) oriented along the upper-level wiring (M2)/second interconnect's width (i.e., its shorter side):



TSMC-1030, ¶¶[0016], [0052], Fig. 1; TSMC-1003, ¶279.

Moreover, demonstrating their known nature, both Iizuka and Yamaha disclose rectangular vias. TSMC-1008, 9:45-47; TSMC-1013, 8:48-52; TSMC-1003, ¶280.

b) [31.b]

Watanabe's Figures 2 and 9 disclose an elongated wiring 39 (second interconnect) and dummy plugs 34/52 (dummy vias). TSMC-1004, Figs. 2, 9; TSMC-1003, ¶282.

Watanabe's dummy vias not only mitigate stress migration, but also electromigration by providing a source of copper atoms to replace those swept away by the electric current traveling through the interconnect. TSMC-1004, ¶¶[0012]-[0019], [0022]-[0024], [0075], [0077]; *see also* TSMC-1015, 1:25-41, 1:66-2:11; TSMC-1003, ¶283. Fujii teaches improving electromigration resistance at a via by having an elongated via (e.g., rectangular) with the longer side in the

direction of the wiring width (orthogonal to the main wiring length). TSMC-1030, Abstract, ¶¶[0016], [0064]-[0066]; TSMC-1003, ¶283.

A POSITA was motivated to modify Watanabe's dummy vias to take advantage of Fujii's teachings, specifically orienting known rectangular-shaped dummy vias perpendicular to the interconnect length to more effectively replace copper atoms across the entire width of the interconnect in response to electromigration. TSMC-1003, ¶¶284-87. Just as in Fujii, the larger surface perpendicular to the current flow direction provides a more even distribution of copper atoms across the interconnect, thus mitigating void formation due to electromigration, while simultaneously capturing migrating vacancies across the interconnect width. *Id.*

Moreover, given that rectangular vias were one of several commonly-recognized shapes (TSMC-1008, 9:45-47 (noting that standard via shapes include rectangular cross-sections); TSMC-1013, 8:48-52 (same)), and given Fujii's teachings regarding the importance of rectangular via orientation relative to the interconnection direction, a POSITA would have arrived at claim 31's limitation through simple, routine optimization of the dummy via shape and orientation. TSMC-1003, ¶288.

A POSITA would have expected success in making Watanabe's dummy vias 34/52 rectangular and oriented relative to the second interconnect as taught by

Fujii, given Fujii's recognition of their standard nature. *Id.*, ¶289. Additionally, configuring dummy vias/interconnects with such shapes/orientations would have merely required patterning of correspondingly shaped and located via holes/interconnect trenches, which was easily achievable with Watanabe's manufacturing processes. *Id.*

H. Ground 7: Claim 48 is Obvious Over Watanabe, Kamoshima, and Fukazawa

Watanabe, Kamoshima, and Fukazawa render Claim 48 obvious. TSMC-1003, ¶¶290-316.

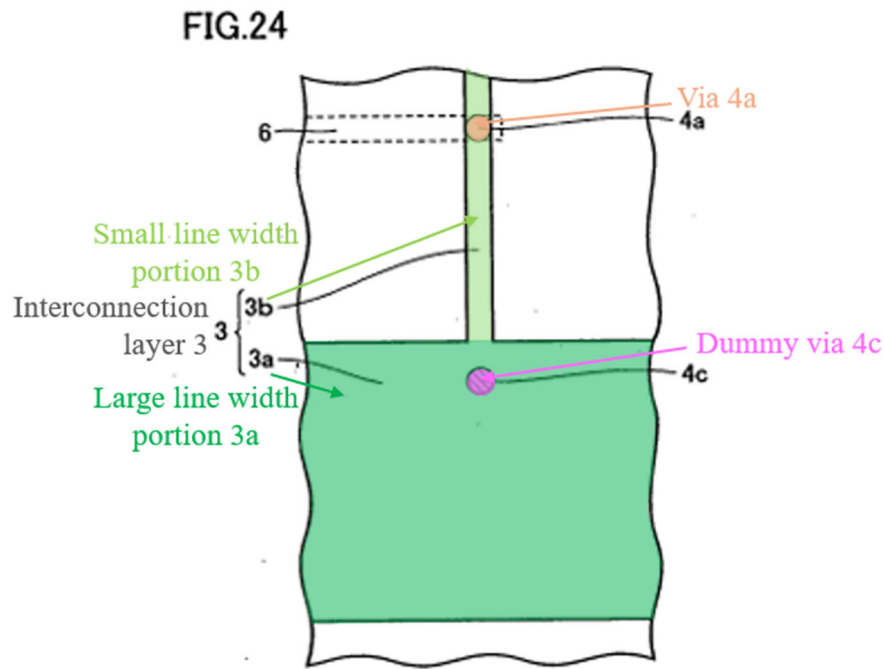
1. Kamoshima

Because Kamoshima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Kamoshima is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1009, ¶¶[0002], [0004]-[0007]; TSMC-1003, ¶¶97-100.

Kamoshima discloses interconnection structures that "suppress concentration of voids in an interconnection under a via due to stress migration." TSMC-1009, ¶¶[0002], [0008]. Kamoshima uses dummy vias so that microvoids are distributed between a via and dummy via, thereby suppressing concentration of microvoids under the via. *Id.*, ¶¶[0088], [0097]-[0098].

Interconnection layer 3 can have different shapes, including having a constant width (Figure 15), and having an interconnection portion with a small line

width 3b branching off an interconnection portion with a large line width 3a (Figures 23-27). *Id.*, ¶¶[0094]-[0103], Figs. 23-27. Kamoshima teaches arranging via 4a along small line width portion 3b and dummy via 4c in the vicinity of a “connection portion” between interconnection portions 3a, 3b. *Id.*, ¶¶[0095], [0099].



Id., Fig. 24; TSMC-1003, ¶¶98-99.

2. Fukazawa

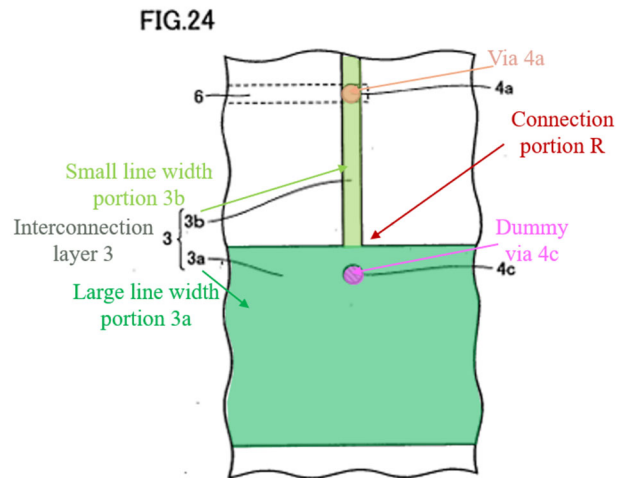
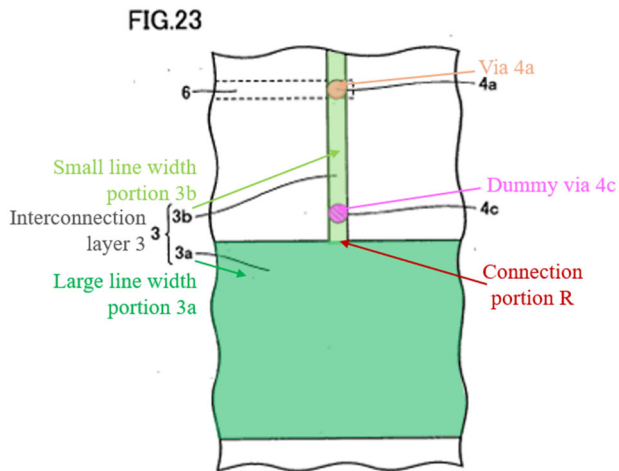
Because Fukazawa is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Fukazawa is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1010, Abstract, ¶¶[0001], [0004]-[0007]; TSMC-1003, ¶¶101-04.

Fukazawa's dummy contact 43, which is a dummy via, is connected to an upper layer interconnect (e.g., "upper layer Cu wiring 41"), and not connected to a lower layer interconnect. TSMC-1010, ¶¶[0017], Fig. 7; TSMC-1003, ¶¶101-02. To enhance mechanical strength, Fukazawa's dummy contact 43 is rectangularly shaped. TSMC-1010, ¶¶[0017]-[0018] ("the dummy contacts are column-shaped"), Fig. 7; TSMC-1003, ¶¶102-03. Thus, Fukazawa provides the additional teaching of a rectangularly-shaped via positioned such that its longer side parallels a longer side of an interconnect portion to which it is connected.

3. Claim 45

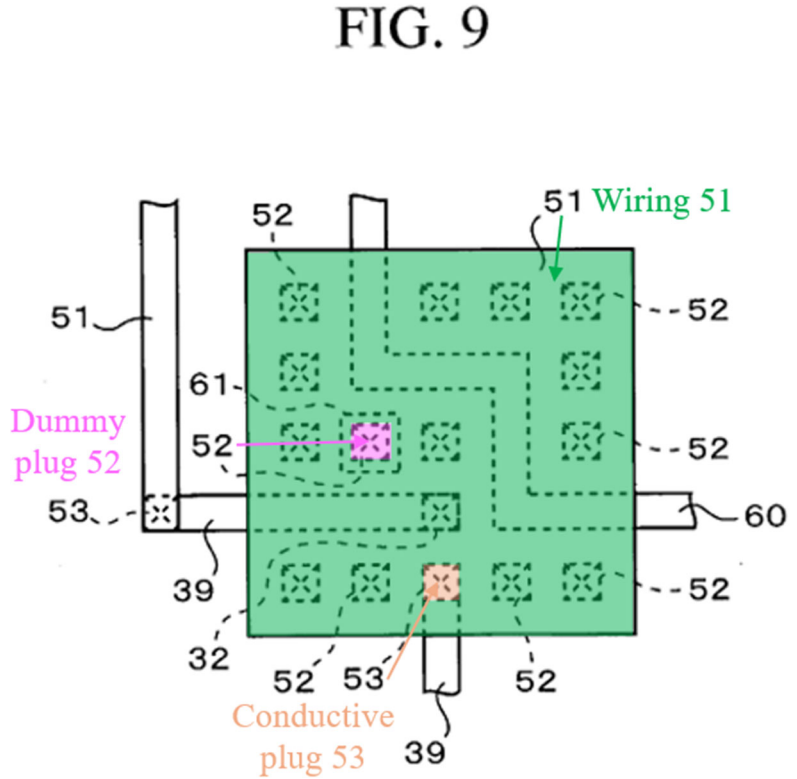
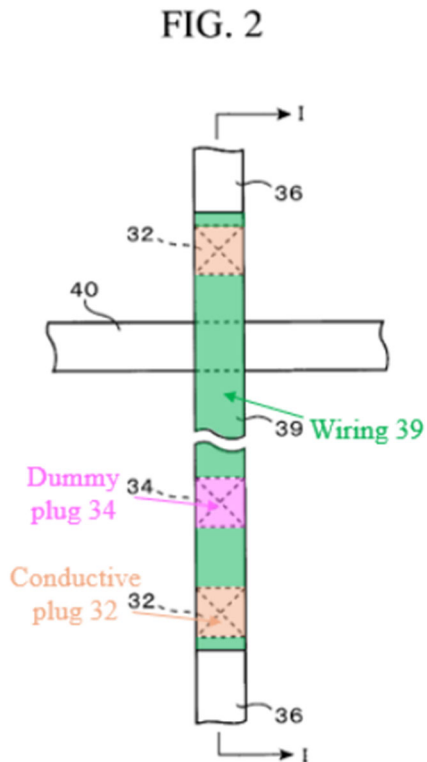
a) [45.a]

Kamoshima discloses an interconnection layer shape with large line width portion 3a and small line width portion 3b. TSMC-1009, ¶¶[0002], [0094]-[0103], Abstract, Figs. 23-27; TSMC-1003, ¶¶291-93. Moreover, Kamoshima teaches having via 4a in small line width portion 3b and dummy via 4c in the vicinity of "connection portion R" between interconnection portions 3a, 3b (*see* TSMC-1009, Figs. 23-24; TSMC-1003, ¶¶292-93):



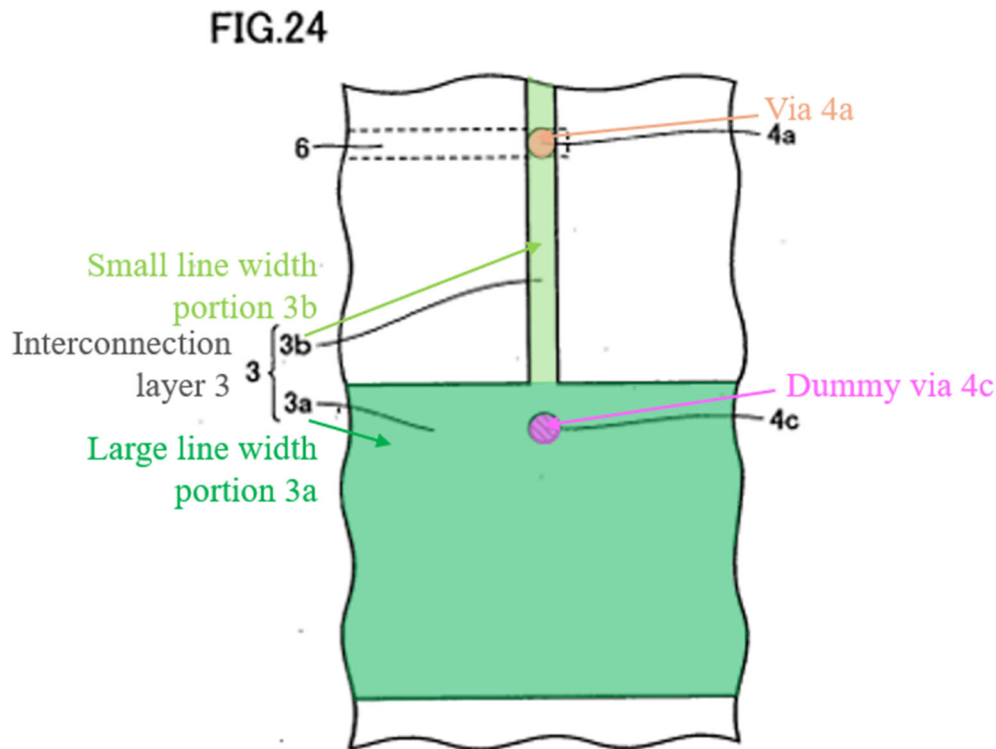
b) [45.b]

Watanabe's vias (conductive plugs 32, 53) and dummy vias (dummy plugs 34, 52) are connected to the second interconnect (wirings 39, 51):



TSMC-1004, ¶¶[0067]-[0073], [0118]-[0122], [0159]-[0165], Figs. 1-3, 8-9, 12J-12M; TSMC-1003, ¶295.

Kamoshima's via 4a and dummy via 4c are similarly connected to interconnection layer 3 (TSMC-1009, Figs. 23-24; *supra*, §VI.H.1; TSMC-1003, ¶296):



c) Combination of Watanabe and Kamoshima

Kamoshima motivates a POSITA to use an interconnection layer with large and small width portions, and positioning the via (for connection to another interconnect) along the small line width portion and dummy via in vicinity of the connection portion between these interconnect portions. TSMC-1003, ¶¶297-302.

Such an interconnect configuration causes microvoids that would otherwise

distribute between the via and the dummy via to further concentrate under the dummy via before reaching the via. *Id.*; see TSMC-1009, ¶¶[0088], [0097]-[0099]. Kamoshima thus teaches a known design choice for suppressing microvoids. TSMC-1003, ¶300.

Following Kamoshima's teachings, a POSITA would update Watanabe's second interconnect 39/51 to include a large line width portion and a small line width portion branched therefrom, analogous to Kamoshima's interconnection layer 3 from Figures 23-24. *Id.*, ¶¶301-02. Watanabe's plug 32/53 would be connected to the small line width portion and dummy plug 34/52 would be connected to the large line width portion. *Id.* This branched interconnect shape further enhances the suppression of microvoids in addition to Watanabe's design in any of its first-to-third and fifth embodiments. *Id.*; see also TSMC-1033, ¶¶[0056]-[0057], [0112]-[0114]; TSMC-1037, 162-63, 165, Figs. 9, 14.

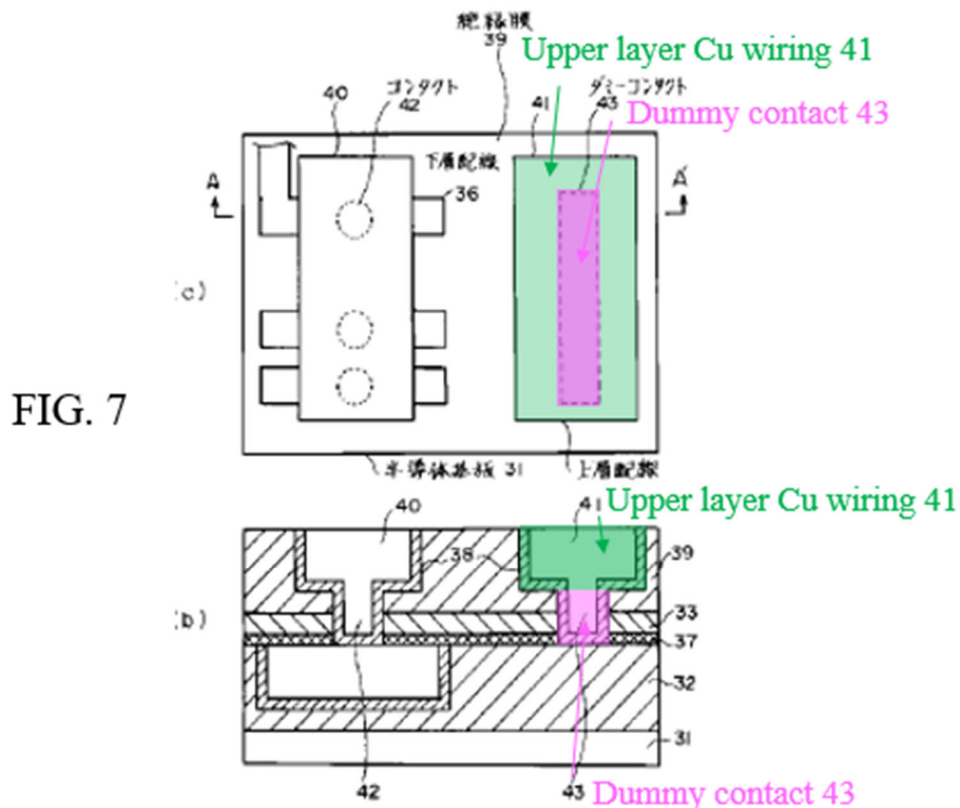
A POSITA would have expected success when modifying Watanabe in this manner. Both Watanabe and Kamoshima relate to forming an interconnect connected to both a via (to connect to another interconnect) and dummy via, where the dummy via is present to suppress voids from concentrating in the via. TSMC-1004, ¶¶[0012]-[0019], [0070]-[0073], [0075], [0117]-[0122], Figs. 1-5C, 8-9; TSMC-1009, ¶¶[0085]-[0086], [0088], [0094]-[0099], Figs. 15-16, 23-27; TSMC-1003, ¶¶303-04. The modification would be readily achieved with Watanabe's

manufacturing process by using appropriate trench portion widths/shapes. TSMC-1003, ¶¶303-04.

4. Claim 48

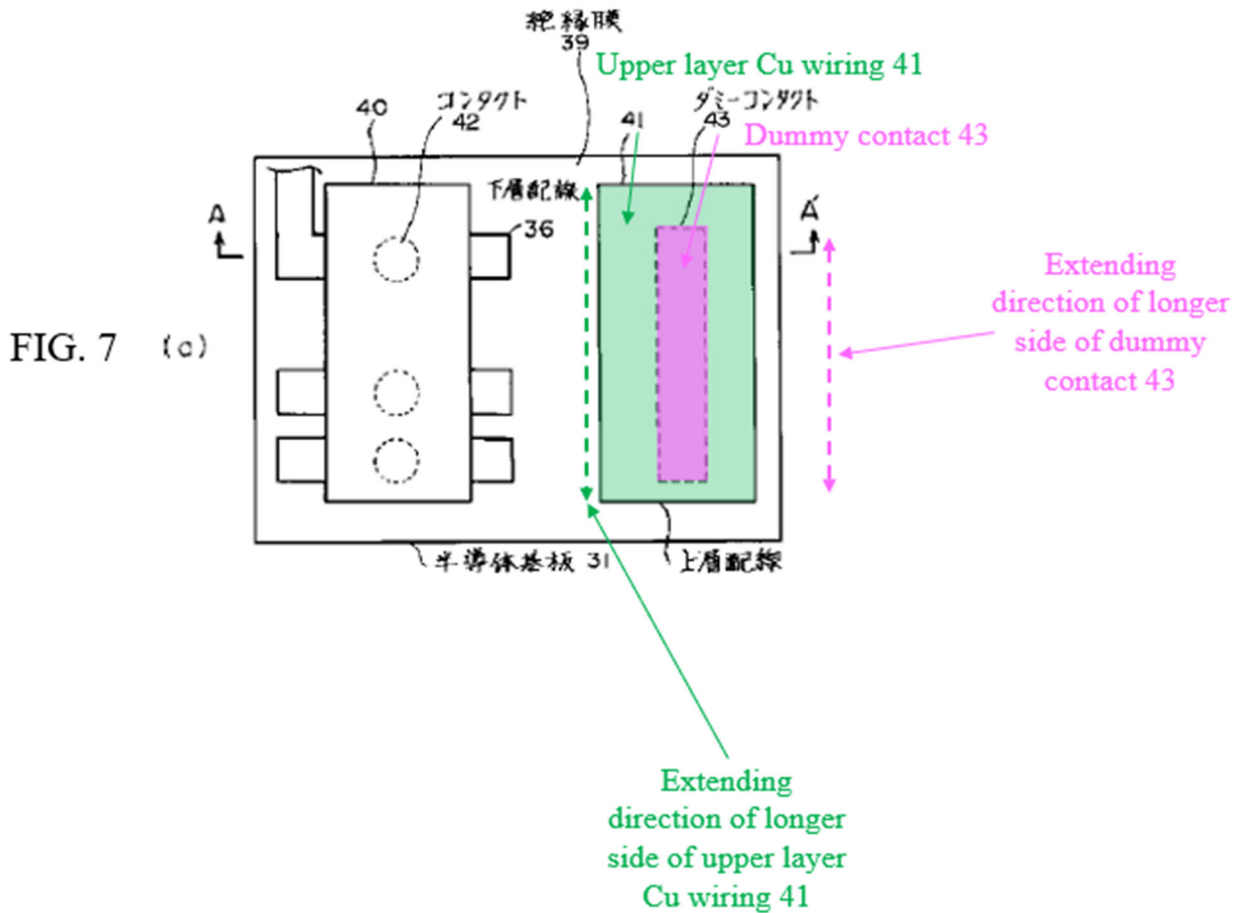
a) [48.a]

Fukazawa discloses a dummy via (e.g., “dummy contact 43” and “barrier metal layer 38,” hereafter collectively “dummy contact 43”) connected to an upper layer interconnect (e.g., “upper layer Cu wiring 41” and “barrier metal layer 38,” hereafter collectively “upper layer Cu wiring 41”). TSMC-1010, ¶[0017], Fig. 7. Fukazawa’s “dummy contact 43” has a substantially rectangular shape in a plan view (*see id.*, ¶¶[0017]-[0018], Fig. 7; TSMC-1003, ¶308):



b) [48.b]

A longer side of dummy contact/via 43 is provided along a same direction as a longer side of a correspondingly rectangular interconnect (“upper layer Cu wiring 41”) (TSMC-1010, ¶¶[0017]-[0018], Figure 7; TSMC-1003, ¶¶[309-10]):

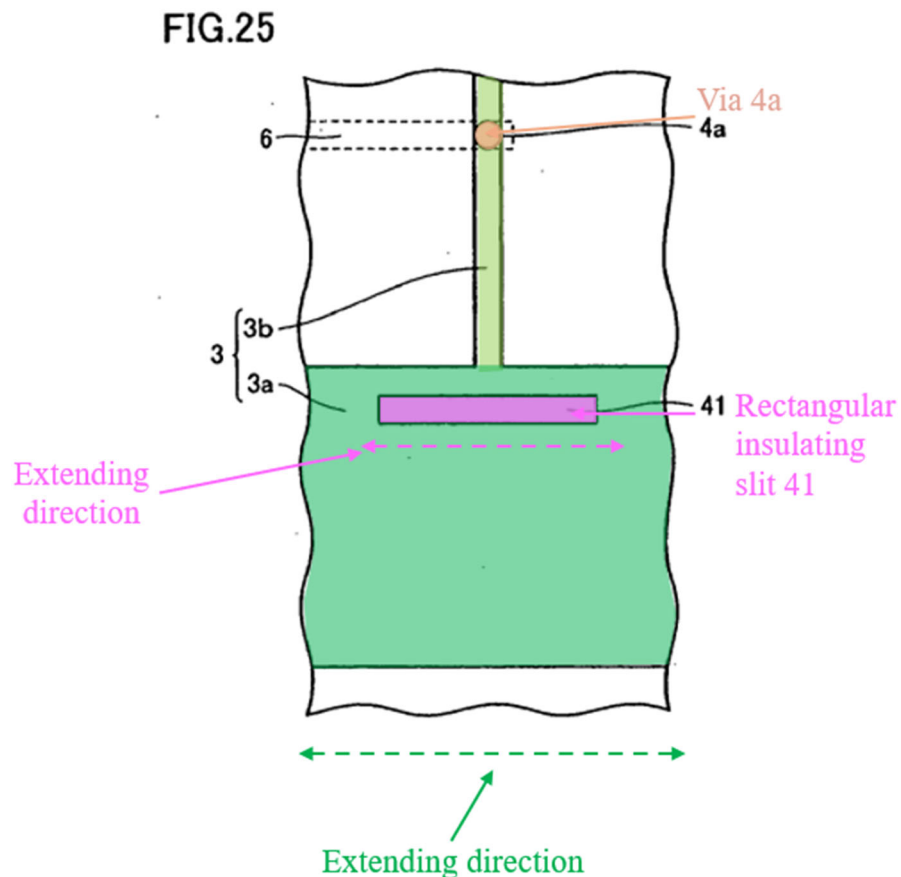


c) **Combination of Watanabe, Kamoshima, and Fukazawa**

In view of Fukazawa, it was obvious to use a rectangularly-shaped dummy via in the wider interconnect portion of Watanabe’s second interconnect (after modified in view of Kamoshima to have a branched interconnect structure – *supra*,

§VI.H.3). TSMC-1003, ¶¶305-316. A POSITA was motivated to use a rectangularly-shaped dummy via and to position it along a longer side of the wider portion of the branched interconnect to further reduce vacancy migration to (and thus void formation within) a real via positioned on the narrow branch of the interconnect. *Id.*, ¶311.

Indeed, Kamoshima teaches using a rectangular structure (e.g., insulating slit 41) positioned in such a manner (such that a longer side of the rectangular structure extends in a same direction as a longer side of the wider interconnect portion) to suppress vacancy migration to via 4a:



TSMC-1009, ¶¶[0102]-[0105], Fig. 25; TSMC-1003, ¶312.

Positioning a rectangular dummy via in the same position as insulating slit 41 would have similarly suppressed vacancy migration (similar to dummy vias 4c in Kamoshima's Figure 23-24 embodiments), with the added benefit of providing a larger area of vacancy interception due to the rectangular shape and its position along a length of the wider portion of the interconnect (and thus perpendicular to the narrow branch portion). TSMC-1003, ¶313.

Additionally, a POSITA was motivated by the increased mechanical strength afforded to the overall wiring structure by the rectangular dummy via, as taught by Fukazawa. *Id.*, ¶314; TSMC-1010, ¶[0018] (“[T]he contacts are column-shaped.... Because of this structure, sufficient mechanical strength is ensured..., thereby improving the strength of the wiring structure.”).

Such a modification had a reasonable expectation of success. TSMC-1003, ¶315. As described previously, a POSITA was capable of creating a branched interconnect. *Id.* Claim 48 merely adds that the dummy via has a rectangular shape and is connected to the wider interconnect portion analogous to the position of insulating slit 41 in Kamoshima's Figure 25 embodiment. *Id.* This would have been reliably accomplished using standard processing techniques at the time. *Id.* Indeed, other references demonstrate that rectangular vias were known and used

and that positioning them where desired was easily achieved. *Id.*; TSMC-1008, 9:45-47; TSMC-1013, 9:45-49, 10:1-4.

I. Ground 8: Hasunuma Anticipates Claims 23, 27, 41, and 43-44

Hasunuma anticipates Claims 23, 27, 41, and 43-44. TSMC-1003, ¶¶317-79.

1. Hasunuma

Because Hasunuma is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Hasunuma is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1005, ¶¶[0003], [0005]-[0006], [0079]-[0088]; TSMC-1003, ¶¶78-82.

Hasunuma addresses reliability problems arising from stresses inherent in interconnect structures. TSMC-1005, ¶¶[0079]-[0086]. Like the '623 patent, Hasunuma's solution for mitigating stress-related problems involves incorporating non-functional, concurrently formed dummy vias ("reinforcing plugs 28") extending from a second interconnect ("conductive layer 26") that is separately connected to a first interconnect ("conductive layer 14") by a functional via ("conductive plug 27") formed through a first insulating film (e.g., films 3, 4, 2):

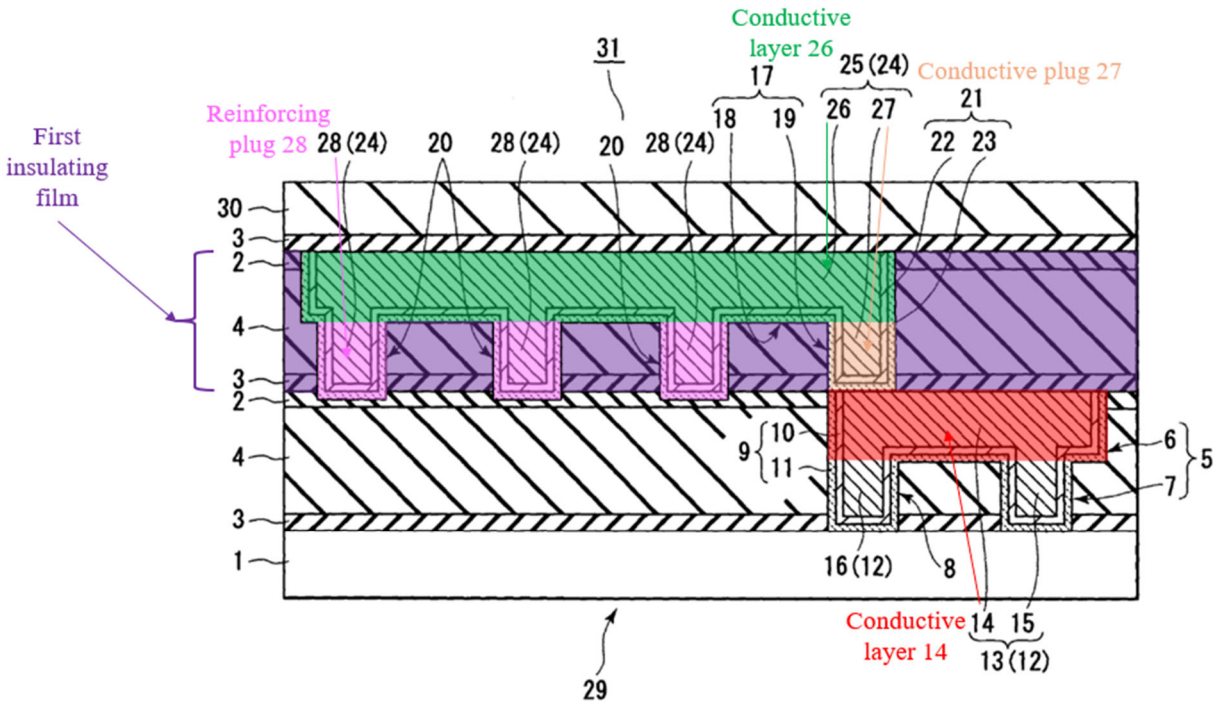


FIG. 8

Id., ¶¶[0090]-[0111], Fig. 8; *see also id.* Fig. 14 (same); TSMC-1003, ¶¶78-81.

Hasunuma forms these structures using a dual damascene process that is repeated for each interconnect-plus-via level. TSMC-1005, ¶[0103].

2. Claim 1⁶

a) [1.pre]

Hasunuma's Figure 8⁷ discloses semiconductor device 31. TSMC-1005,

⁶ Hasunuma is applied to claim 1 given the dependencies of the challenged claims.

⁷ Hasunuma’s Figure 14 embodiment meets the challenged claims just like the first embodiment that includes Figure 8. TSMC-1003, ¶319 n.6.

Abstract, ¶¶[0021], [0111]; TSMC-1003, ¶¶318-19.

b) [1.a]

Hasunuma’s Figure 8 discloses silicon substrate 1 (i.e., a “semiconductor substrate”). TSMC-1005, ¶¶0090, Figs. 1A-8; TSMC-1003, ¶¶320-21.

c) [1.b]

Hasunuma discloses a first interconnect (e.g., “Cu conductive layer 14” and “barrier layer 9,” hereinafter collectively “conductive layer 14” or “first interconnect”) formed on the semiconductor substrate. TSMC-1005, ¶¶[0095], [0098], Figs. 3A, 8. Conductive layer 14 is formed within an insulating film deposited over substrate 1:

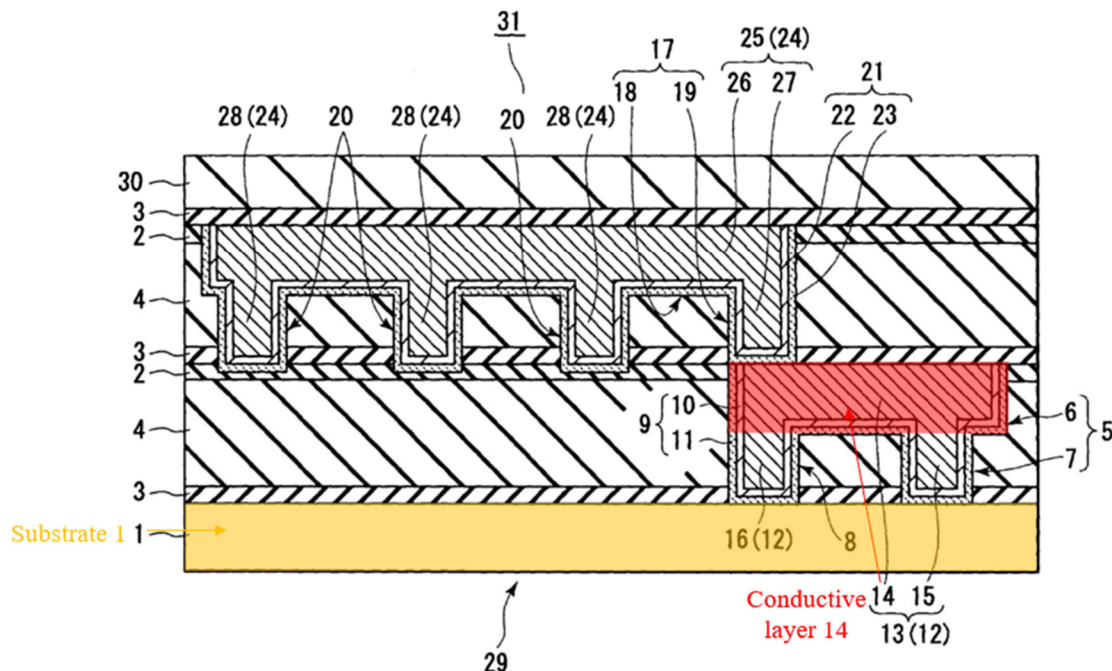


FIG. 8

TSMC-1003, ¶¶322-23.

d) [1.c]

Hasunuma discloses a first insulating film comprising insulating films 3, 4, and 2 stacked on the first interconnect:

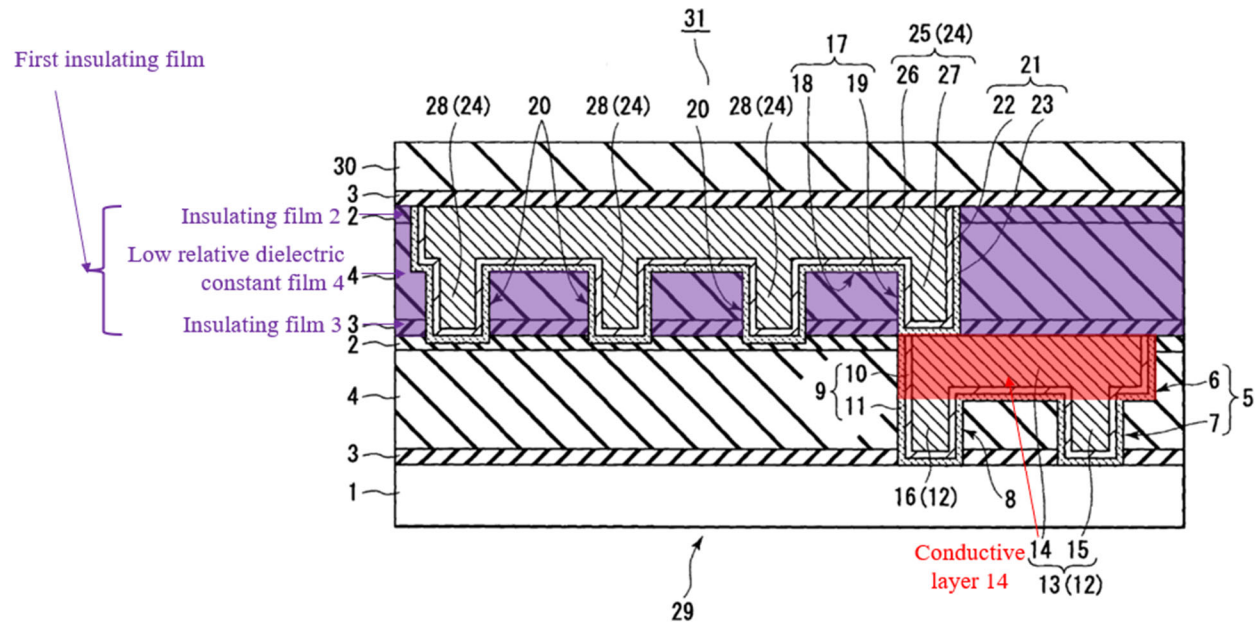


FIG. 8

TSMC-1005, ¶¶[0100], [0090]-[0091], Figs. 3A-8; TSMC-1003, ¶¶324-25. Either the combination of films 3, 4, and 2, or either or both of films 3 and 4, can constitute the “first insulating film.” *Id.*, ¶326.

e) [1.d]

Hasunuma discloses a second interconnect, formed by filling recess 18 in the “first insulating film” with barrier metal film 21 and copper film 24 to form, collectively “conductive layer 26”:

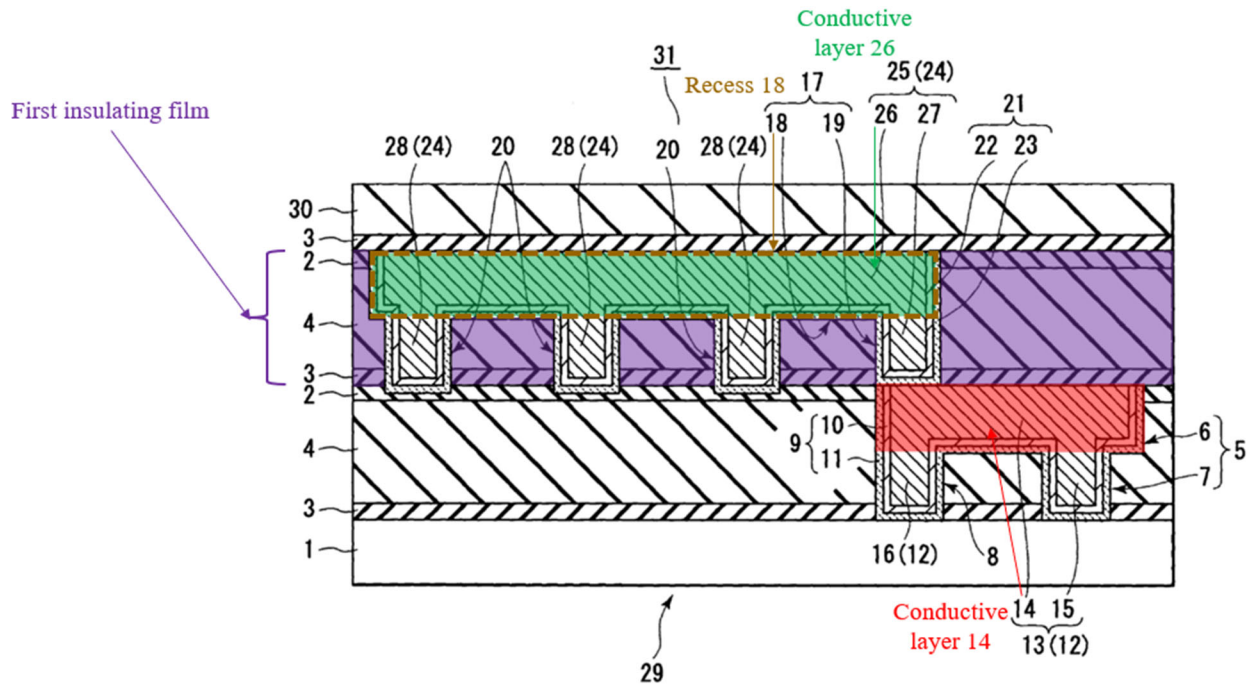


FIG. 8

TSMC-1005, ¶¶[0101], [0105]-[0108], [0110], Figs. 4-8; TSMC-1003, ¶¶327-28.

The second interconnect is formed on the first insulating film, regardless of whether the first insulating film comprises all of insulating films 3, 4, and 2, or either or both of films 3 and 4. *Id.*, ¶329.

f) [1.e]

Hasunuma discloses a via, formed by filling recess 19 with barrier metal layer 21 and copper film 24 to form, collectively “conductive plug 27,” that extends through the first insulating film from the second interconnect (conductive layer 26) to the first interconnect (conductive layer 14):

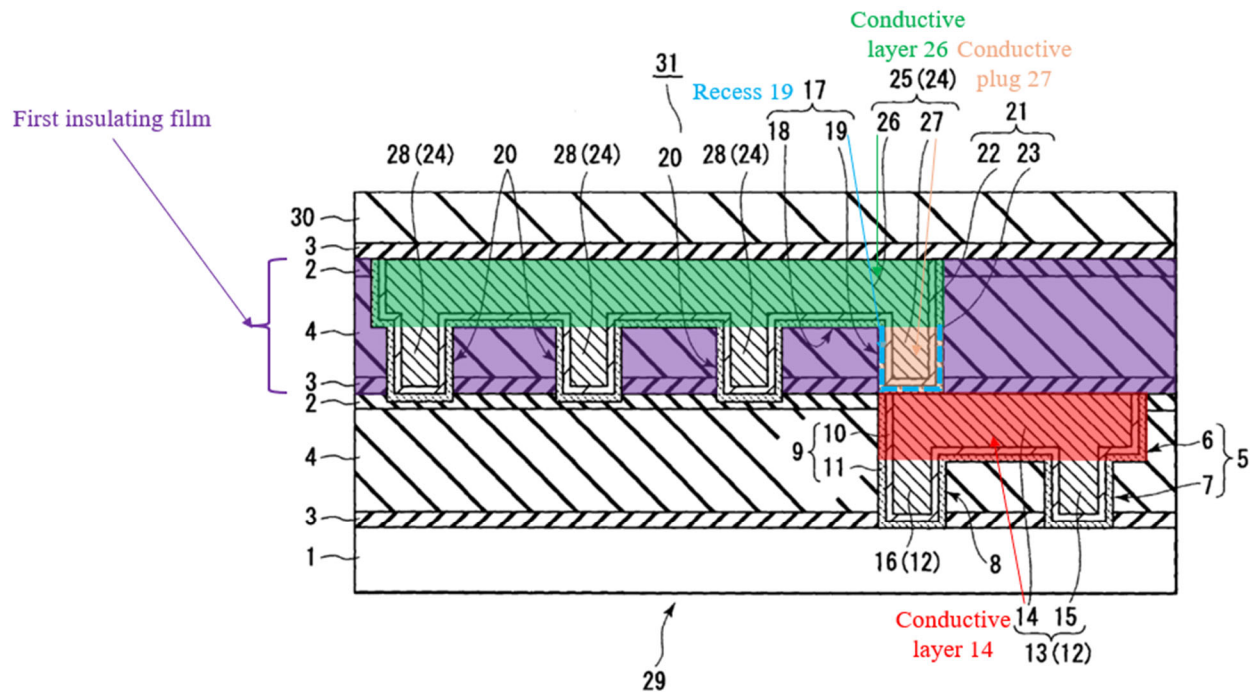


FIG. 8

TSMC-1005, ¶¶[0101]-[0103], [0105]-[0108], Figs. 4-8; TSMC-1003, ¶¶330-31.

Conductive plug 27 connects the first and second interconnects through the first insulating film, regardless of whether insulating films 3, 4, and 2, or either or both of films 3 and 4, constitute the first insulating film. *Id.*, ¶332.

g) [1.f]

Hasunuma discloses dummy vias, formed by filling recesses 20 with barrier metal film 21 and copper film 24 to form, collectively “reinforcing plugs 28,” that extend from the second interconnect:

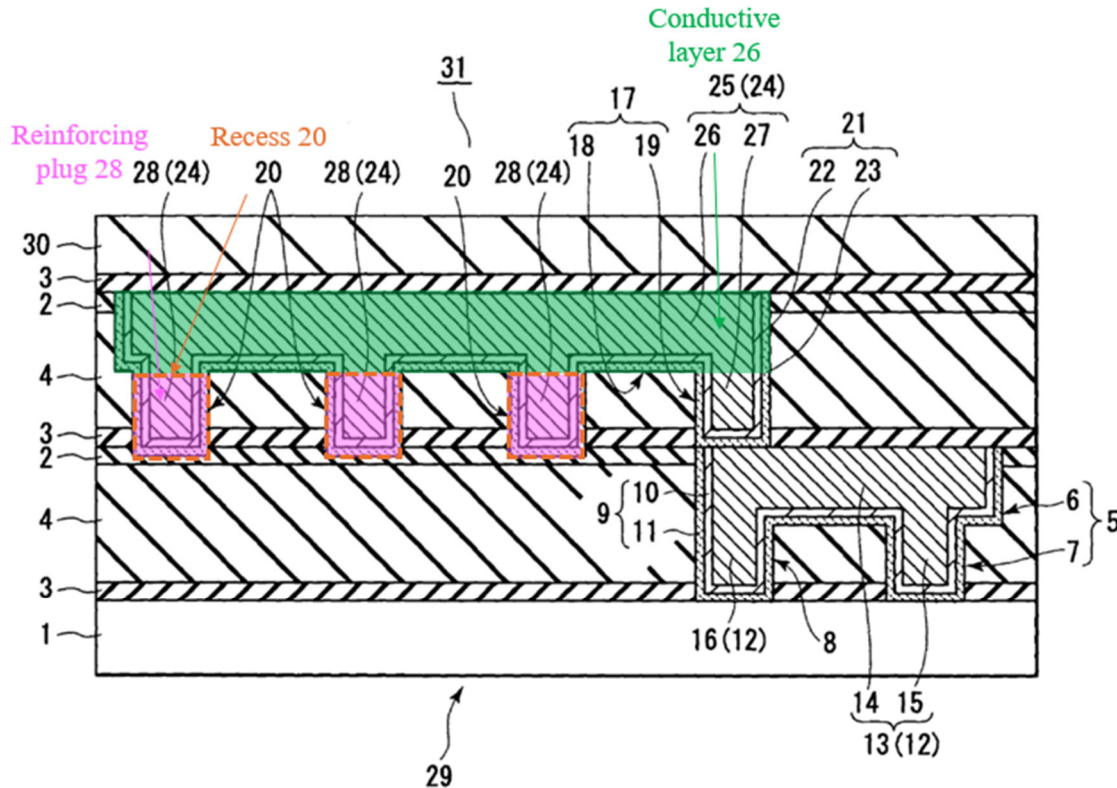


FIG. 8

TSMC-1005, ¶¶[0103]-[0108], Figs. 4-8; TSMC-1003, ¶¶333-37.

h) [1.g]

Hasunuma's dummy vias (reinforcing plugs 28) are formed from barrier metal film 21 and copper film 24 (*supra*, §VI.I.2.(g)), which are “conductive films.” TSMC-1003, ¶¶338-39. The lower ends of reinforcing plugs 28 are connected only to insulating films 2 and 3, and Hasunuma explicitly describes reinforcing plug 28 as a non-functional “dummy plug (sacrifice plug)” which does not function as the wiring. TSMC-1005, ¶¶[0104], [0109], Fig. 8. Reinforcing plugs 28 thus do not conduct current as part of active device operation, could be

omitted from the structure without any impact on the device's circuit diagram, and are incapable of having current flow therethrough in the context of the device's operational circuitry. TSMC-1003, ¶¶340-45. Moreover, Hasunuma's device would still be operable if reinforcing plugs 28 were omitted, because current would still flow through the active circuit elements (i.e., conductive layers 14 and 26 and conductive plug 27) during actual use of the device. *Id.*

i) [1.h]/[1.i]

Hasunuma's wiring layer 25 (which comprises the second interconnect (conductive layer 26) and via (conductive plug 27)) is "formed in the dual damascene structure." TSMC-1005, ¶¶[0101], [0108]. Hasunuma's second interconnect (conductive layer 26) and dummy vias (reinforcing plugs 28) are similarly "formed in the dual damascene structure." *Id.*, ¶[0103]; TSMC-1003, ¶¶346-47.

This is consistent with Hasunuma forming the second interconnect, via, and dummy vias integrally when recesses 18-20 are simultaneously filled with barrier metal film 21 and then copper film 24. TSMC-1005, ¶¶[0101], [0103], [0105]-[0109], Figs. 4-8. Thus, Hasunuma's second interconnect and via forms a dual damascene structure, as does its second interconnect and dummy vias:

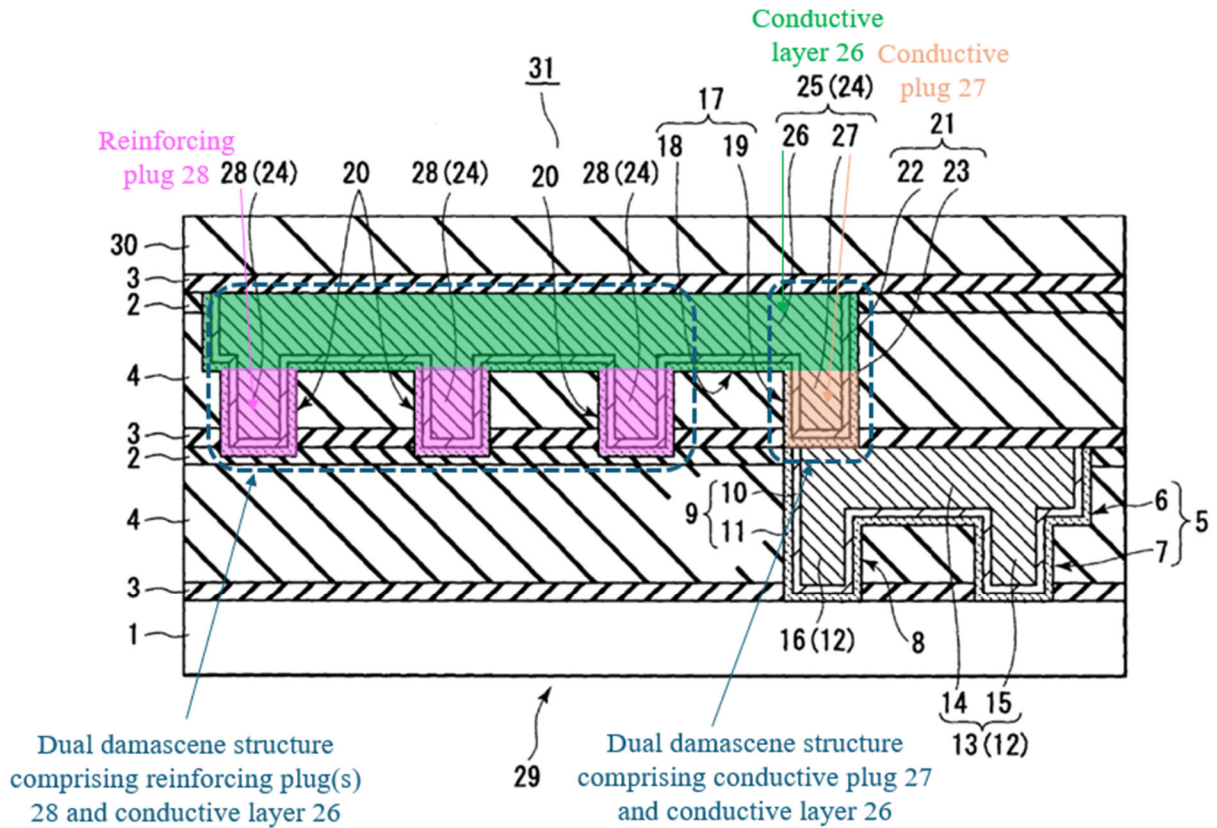


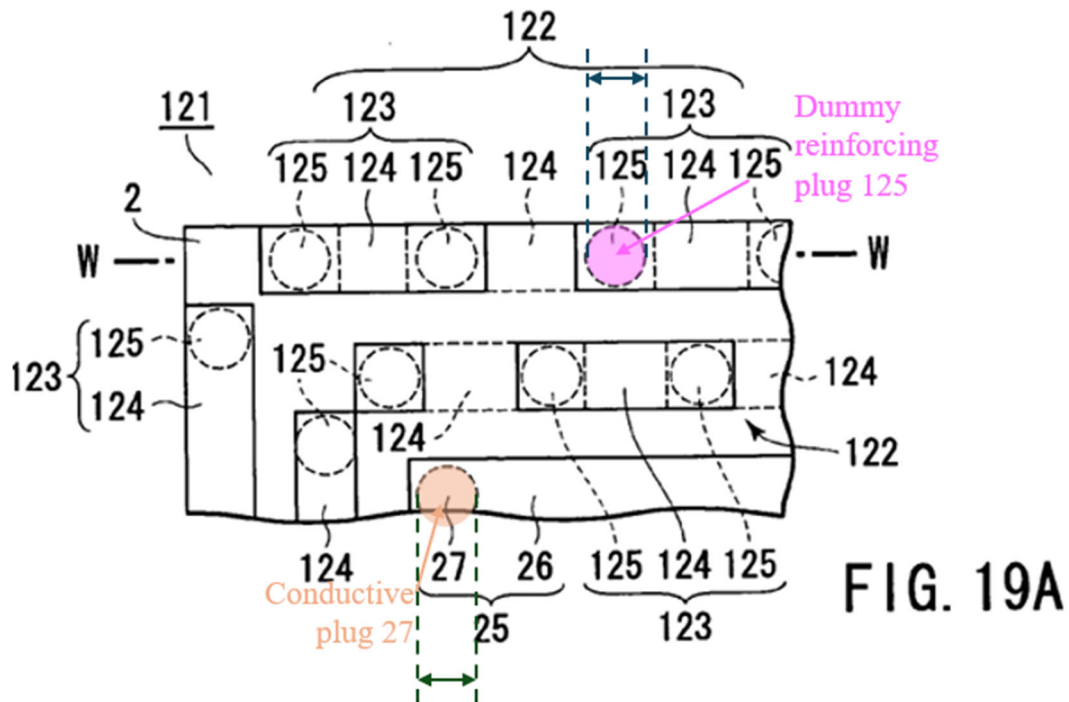
FIG. 8

TSMC-1003, ¶348.

3. Claim 23

a) [23.a]

Hasunuma discloses via structures with circular plan views, for example in Figure 19A, which shows various dummy reinforcing plugs 125 and conductive plugs 27 as circular:



TSMC-1005, ¶[0200]; *see also id.*, Figs. 22A-22C, 24A-27C; TSMC-1003, ¶350.

Further, when describing tests performed on structures including Hasunuma’s vias (conductive plugs 27) and dummy vias (reinforcing plugs 28), Hasunuma refers to their diameter: “each **diameter** of...conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 μm .” TSMC-1005, ¶¶[0127], [0133], [0201], [0216], [0010]; TSMC-1003, ¶351. This use of “diameter” discloses a circular shape for both conductive plug 27 and reinforcing plug 28, since “diameter” is the standard dimensional term for circular features. TSMC-1003, ¶352. The express disclosure of circular vias in, *inter alia*, Figure 19A, reinforces that Hasunuma’s reference to the “diameters” of its vias and

dummy vias teaches structures having a substantially circular cross section in plan view, just as in Figure 19A. *Id.*

b) [23.b]

Hasunuma discloses a via diameter of “about 0.13 μm ,” and in the same paragraph teaches that the interconnects (as part of wirings 13 and 25, respectively) also have widths of “about 0.13 μm .” TSMC-1005, ¶[0127]. Hasunuma’s via diameter and first interconnect width (as part of wiring 13) are therefore substantially equal. TSMC-1003, ¶¶353-54.

4. Claim 27

Hasunuma’s Figure 9⁸ and Tables 1-3 provide values for the “Plug interval” between conductive plug 27 and an adjacent reinforcing plug 28, labeled as “B” and seen below in Figure 9:

⁸ Figure 9 depicts the same device of Hasunuma’s first embodiment/Figure 8, adding various heat stress illustrations. TSMC-1005, ¶¶[0022], [0112]; TSMC-1003, ¶357 n.7.

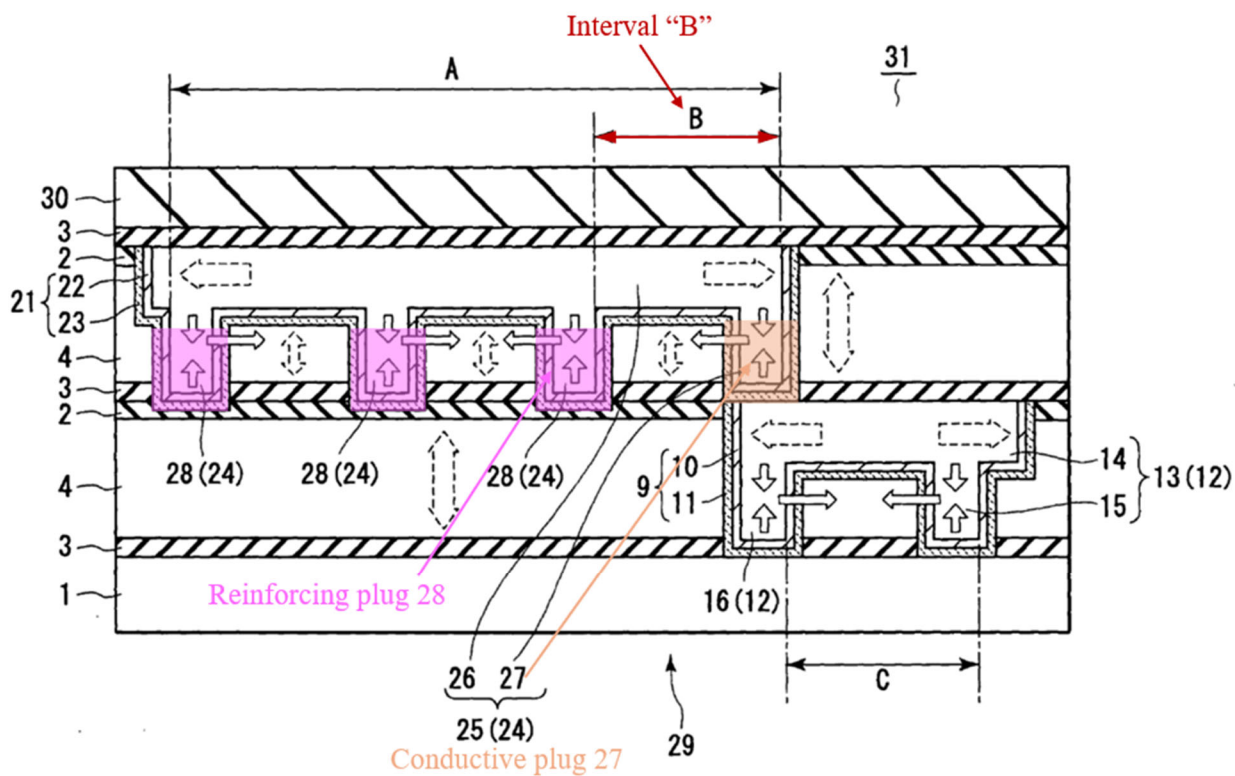


FIG. 9

TSMC-1005, ¶¶[0127], [0130]-[0137]; TSMC-1003, ¶¶357-58. As seen above, interval “B” is effectively equal to the center-to-center spacing between the via and dummy via, which is larger than the edge-to-edge spacing between the via and dummy via (e.g., the spacing between the right edge of reinforcing plug 28 and the adjacent left edge of conductive plug 27). TSMC-1003, ¶¶358-59.

The smallest value for B from Table 1 that was successful with 3 plugs is 0.26 μm . TSMC-1005, Table 1. The edge-to-edge spacing between the via and dummy via can be calculated as interval B (0.26 μm) minus the via diameter

(=0.13 μm (*id.*, ¶[0127])), which results in an edge-to-edge spacing of 0.13 μm .

TSMC-1003, ¶360.

Hasunuma teaches a wiring width for wiring layer 13 (which includes the first interconnect (conductive layer 14)) and wiring layer 25 (which includes the second interconnect (conductive layer 26)) of about 0.13 μm , establishing this as “a minimum interconnect width.” TSMC-1005, ¶[0127]; TSMC-1003, ¶356.

Therefore, Hasunuma discloses a distance between the via and dummy via of 0.13 μm , equal to the minimum interconnect width of 0.13 μm . TSMC-1003, ¶360.

5. Claim 41

Hasunuma discloses dummy vias (e.g., “reinforcing plugs 28”) with first and second ends, the first end connected to the second interconnect (e.g., “conductive layer 26”) and the second end surrounded by insulating film 2 (alone or as part of the combination with film 4):

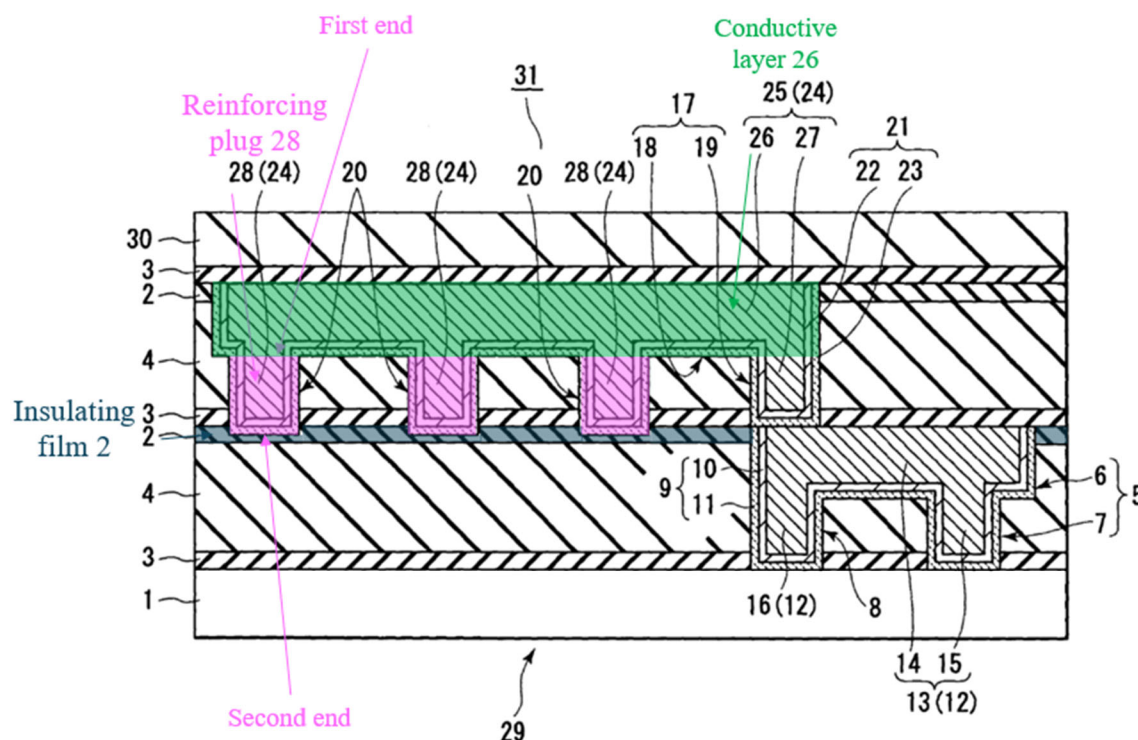
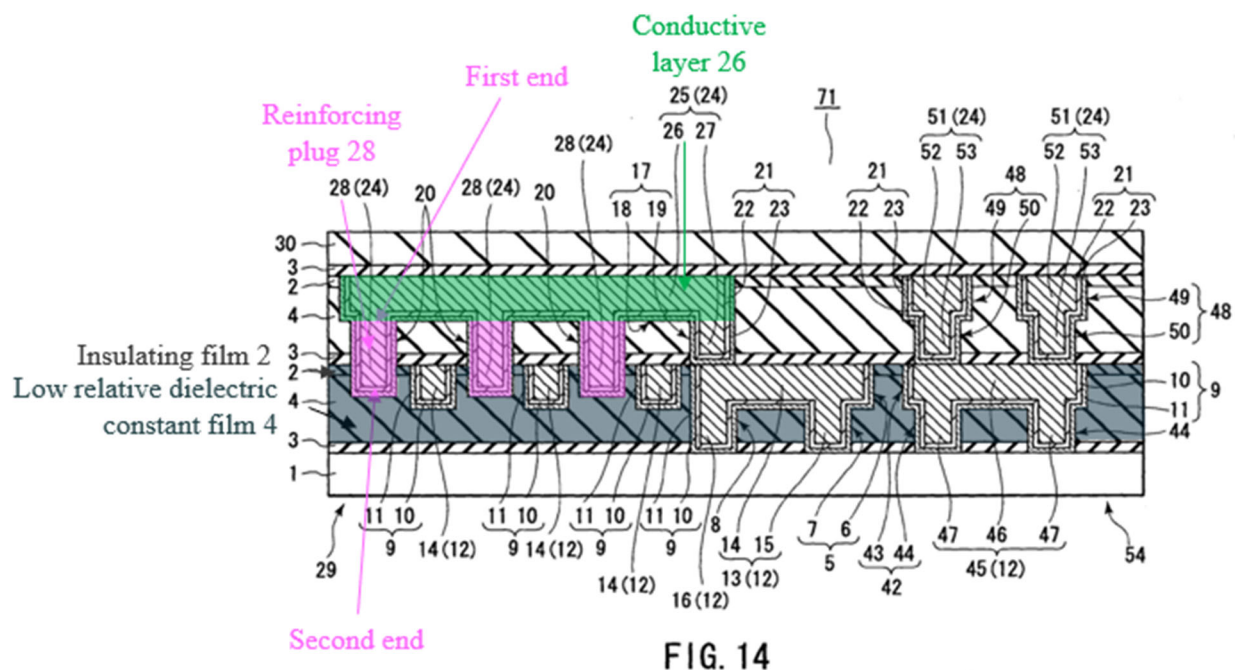


FIG. 8

TSMC-1005, ¶¶[0103]-[0104], [0109], Figs. 4, 8; TSMC-1003, ¶¶361-66.

Additionally, Figure 14 (an embodiment having the same relevant components as Hasunuma's Figures 1-8 embodiment)⁹ (TSMC-1005, ¶[0176]) discloses "the lower end of each Cu reinforcing via plug 28 project[ing] into the low relative dielectric constant film...4 of the first layer," (*id.*, ¶[0177]), such that the second ends of reinforcing plugs 28 are surrounded by film 4:

⁹ As noted above, the same analysis described herein for Figures 1-8 applies equally to Figure 14 throughout this Petition. TSMC-1003, ¶367.



TSMC-1003, ¶¶365-67.

6. Claim 43

Hasunuma teaches that a bottom of its dummy vias (reinforcing plugs 28) is deeper than a bottom of its vias (conductive plug 27). TSMC-1005, ¶¶[0104], [0109], [0176]-[0178], Fig. 8, 14; TSMC-1003, ¶¶368-71. Figure 8 discloses “reinforcing plug 28” extending into underlying “SiC film 2” while “conductive plug 27” extends only to the upper surface of “conductive layer 14”:

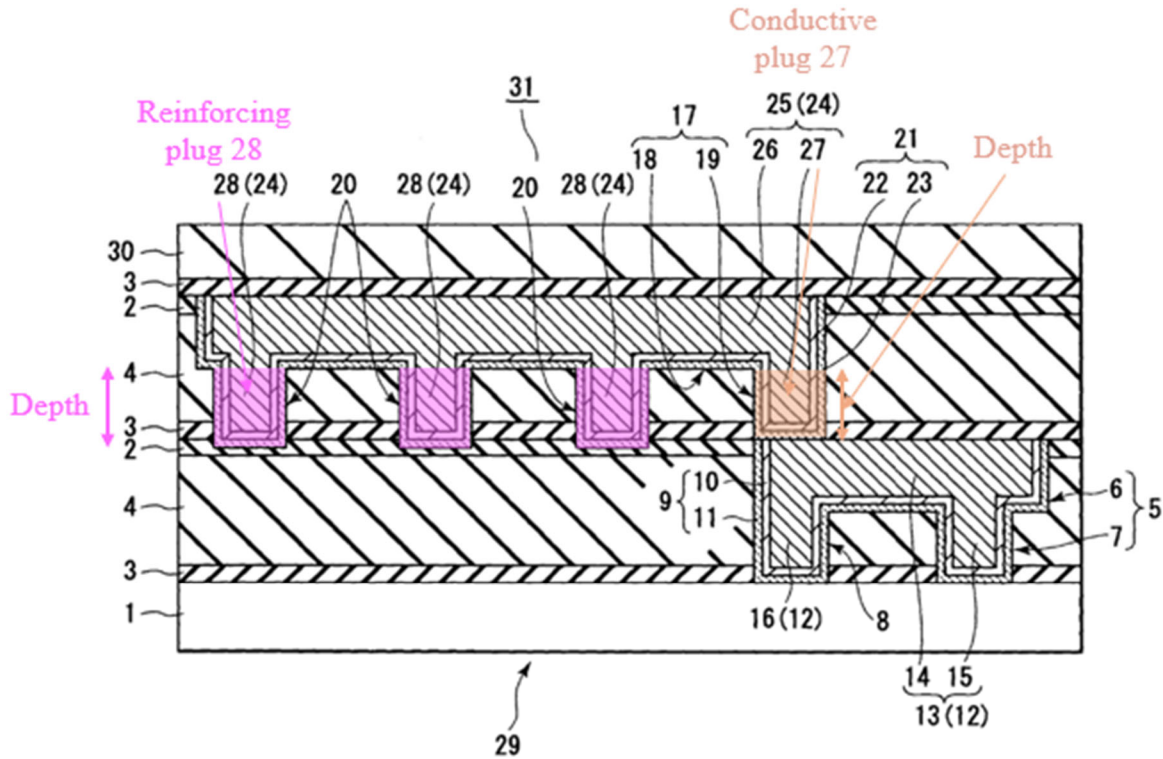


FIG. 8

TSMC-1005, Fig. 8, ¶¶[0109], [0104]; TSMC-1003, ¶369.

Additionally, Figure 14 (*supra* §VI.I.5) discloses “reinforcing plugs 28” extending into underlying film 4 while “conductive plug 27” only extends to the upper surface of “conductive layer 14”:

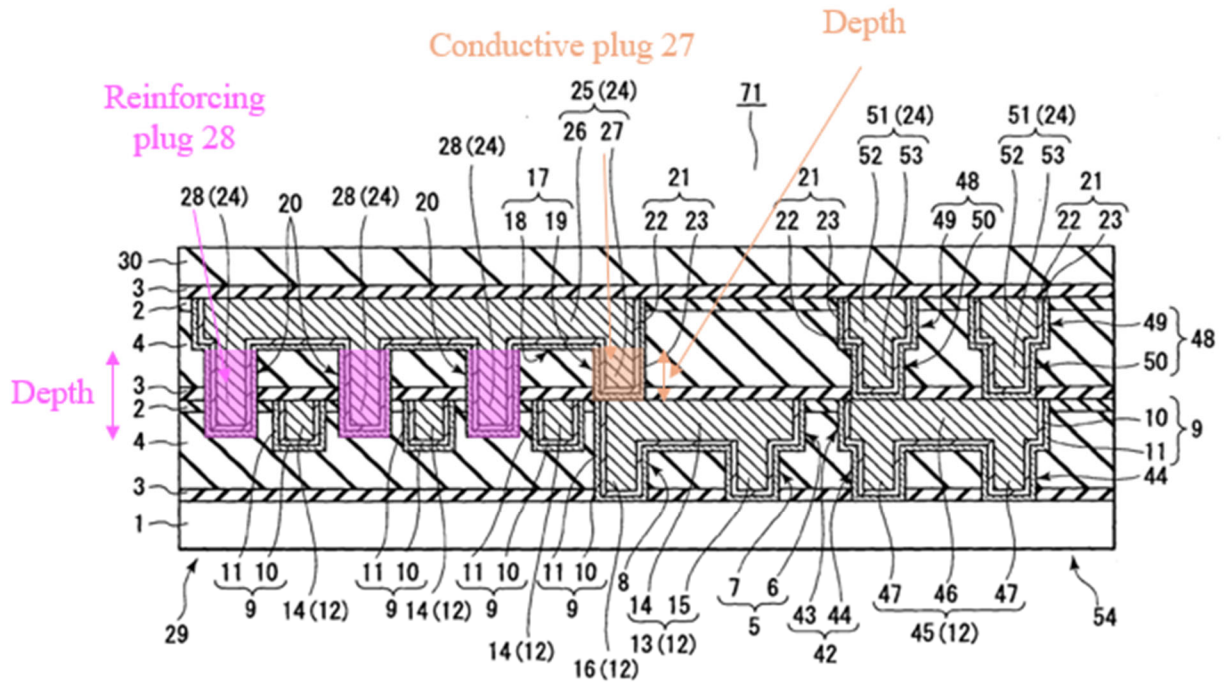


FIG. 14

TSMC-1005, Fig. 14, ¶[0176]; TSMC-1003, ¶370.

7. Claim 44

a) [44.a]

Hasunuma discloses a “second insulating film” (e.g., insulating films 3, 4, and 2) on substrate 1:

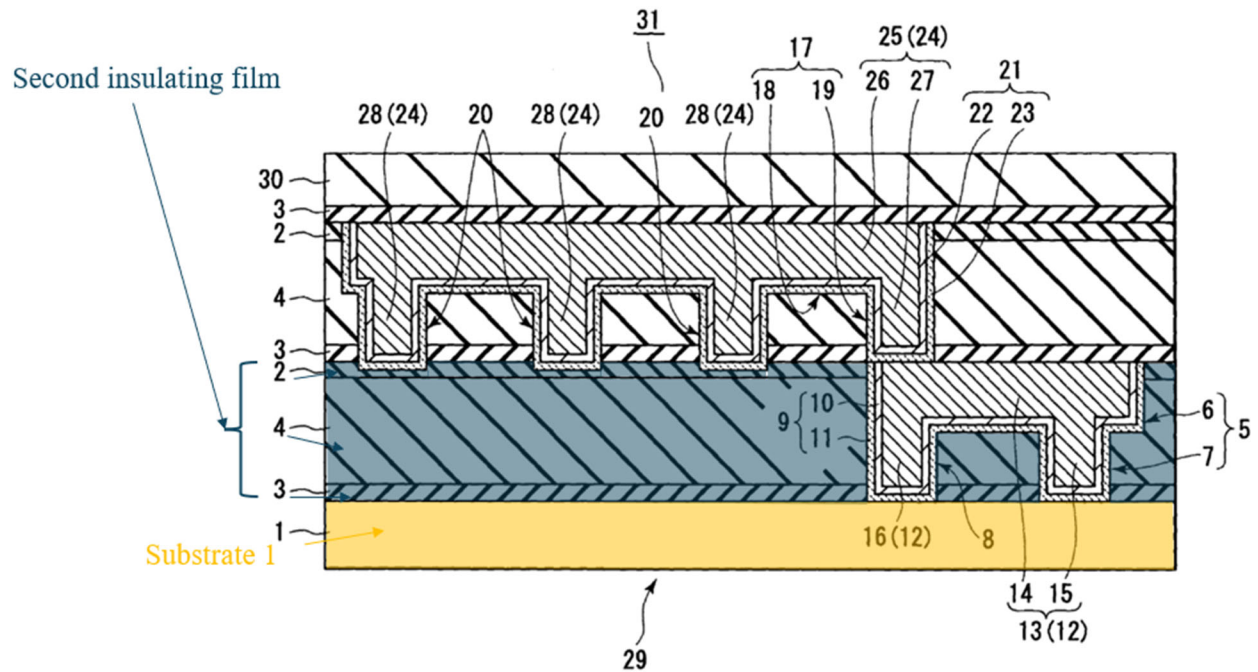


FIG. 8

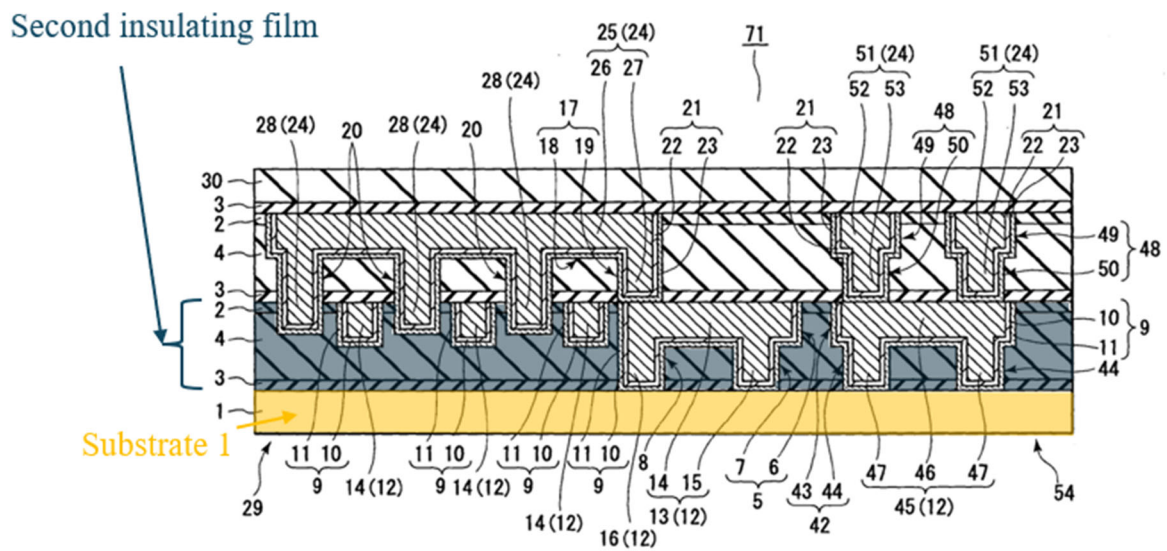
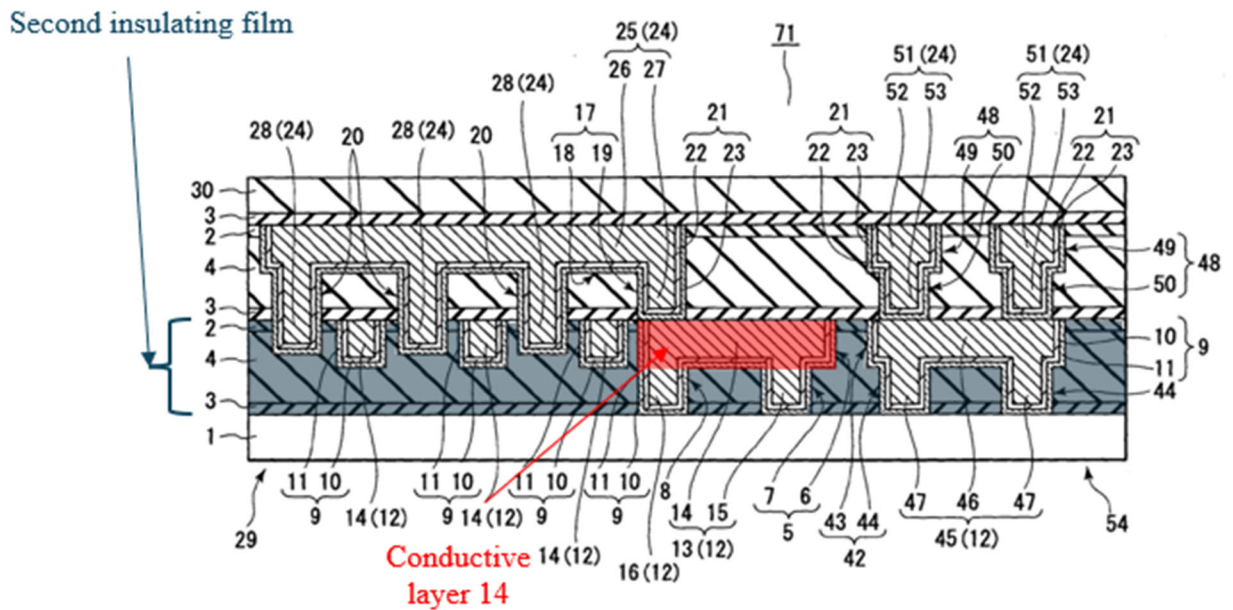
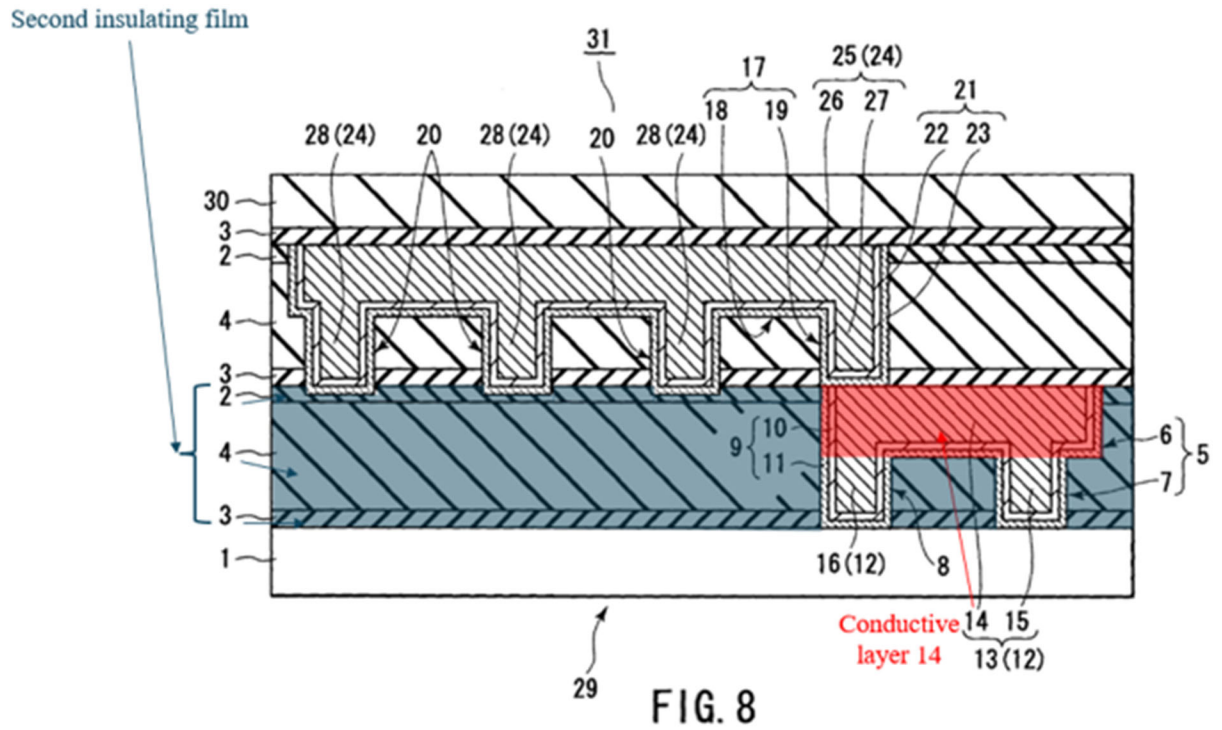


FIG. 14

TSMC-1005, ¶¶[0090]-[0091], Figs. 1A, 8, 14; TSMC-1003, ¶¶372-73.

b) [44.b]

Hasunuma's first interconnect (conductive layer 14) is formed on the second insulating film:



As explained above (*supra*, §VI.I.5), a bottom of Hasunuma's dummy vias (reinforcing plugs 28) extends into the second insulating film (e.g., insulating films 3, 4, 2):



101

Second insulating film

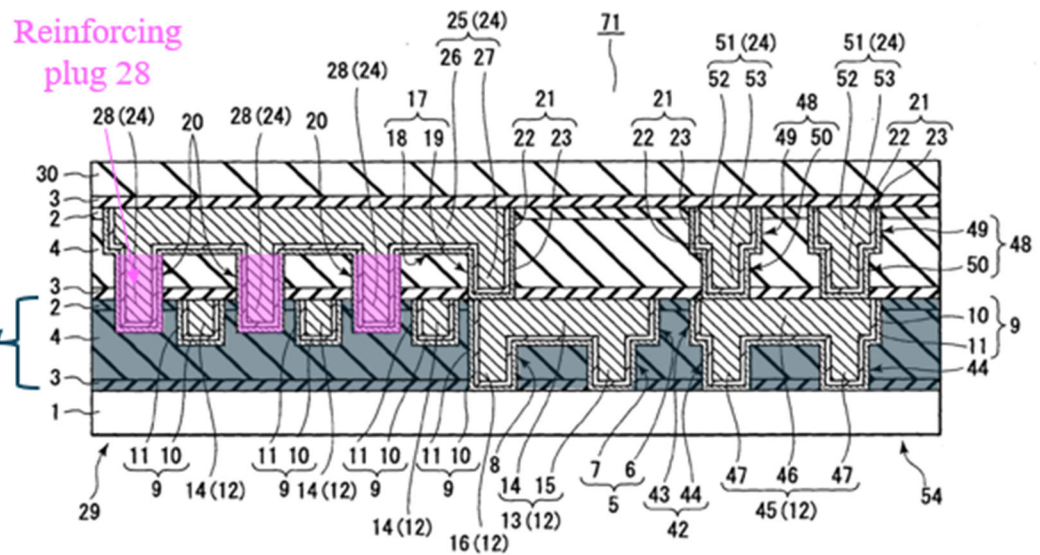


FIG. 14

TSMC-1005, ¶¶[0176]-[0178], Fig. 14; TSMC-1003, ¶¶378-79. The Figure 14 embodiment also meets claims 1 and 44 with the “second insulating film” being, e.g., Hasunuma’s lower films 4 and 2, or lower films 4 and 3. *Id.*

J. Ground 9: Claim 5 Is Obvious Over Hasunuma and Kurashima

Hasunuma and Kurashima render claim 5 obvious. TSMC-1003, ¶¶380-403.

1. Claim 2¹⁰

a) [2.a]

Hasunuma discloses a second insulating film (e.g., the stack of insulating films 3, 4, and 2 in Figure 3A)¹¹, on silicon substrate 1:

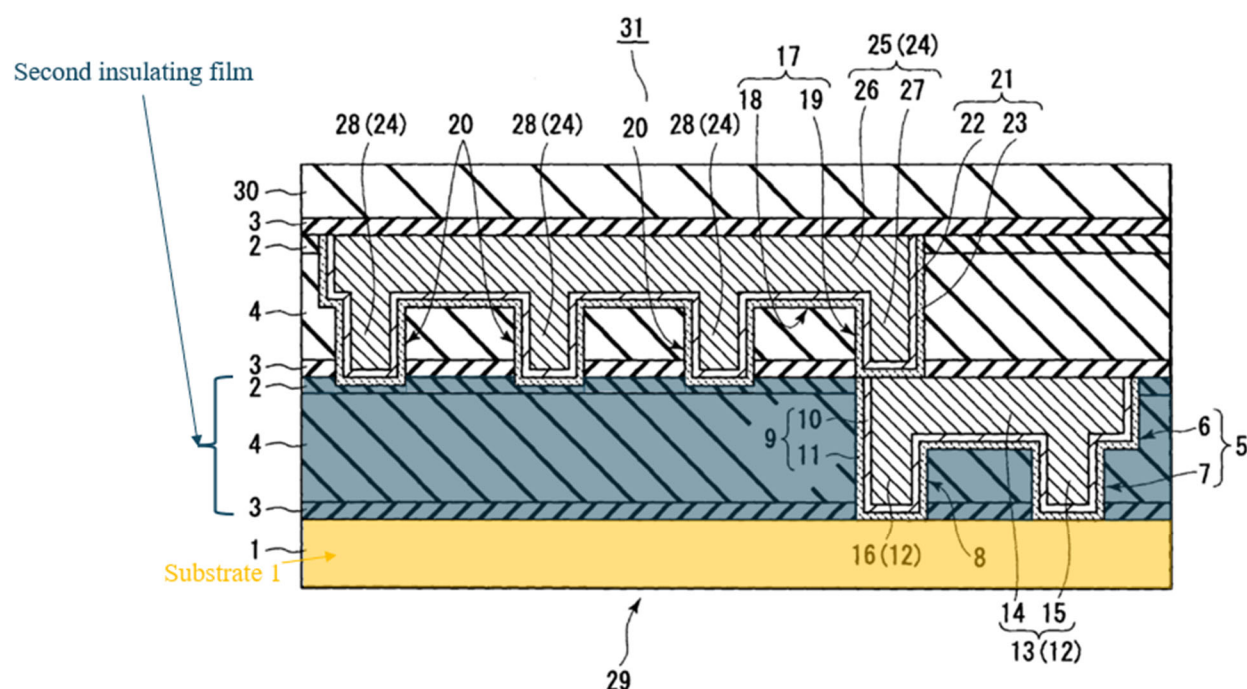


FIG. 8

TSMC-1005, §§[0090]-[0091], Figs. 8, 14; TSMC-1003, §§381-82.

¹⁰ Claim 2 is addressed due to the dependencies of the challenged claims.

¹¹ In the alternative, any or both of films 3 and 4 also satisfies the “second insulating film” element. TSMC-1003, ¶382 n.9.

b) [2.b]

Hasunuma discloses first interconnect (e.g., conductive layer 14) on the second insulating film:

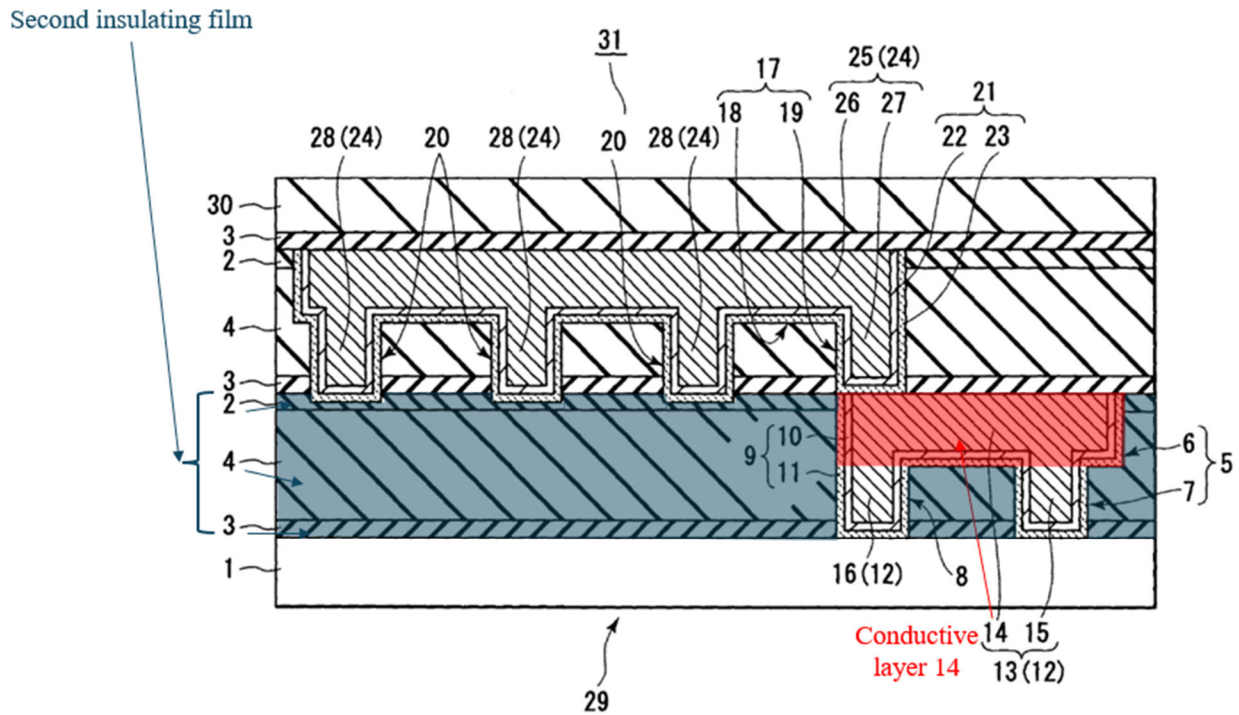


FIG. 8

TSMC-1005, ¶¶[0092]-[0098], Figs. 3A, 8, 14; TSMC-1003, ¶¶383-84.

c) [2.c]

Hasunuma discloses dummy vias (e.g., “reinforcing plugs 28”):

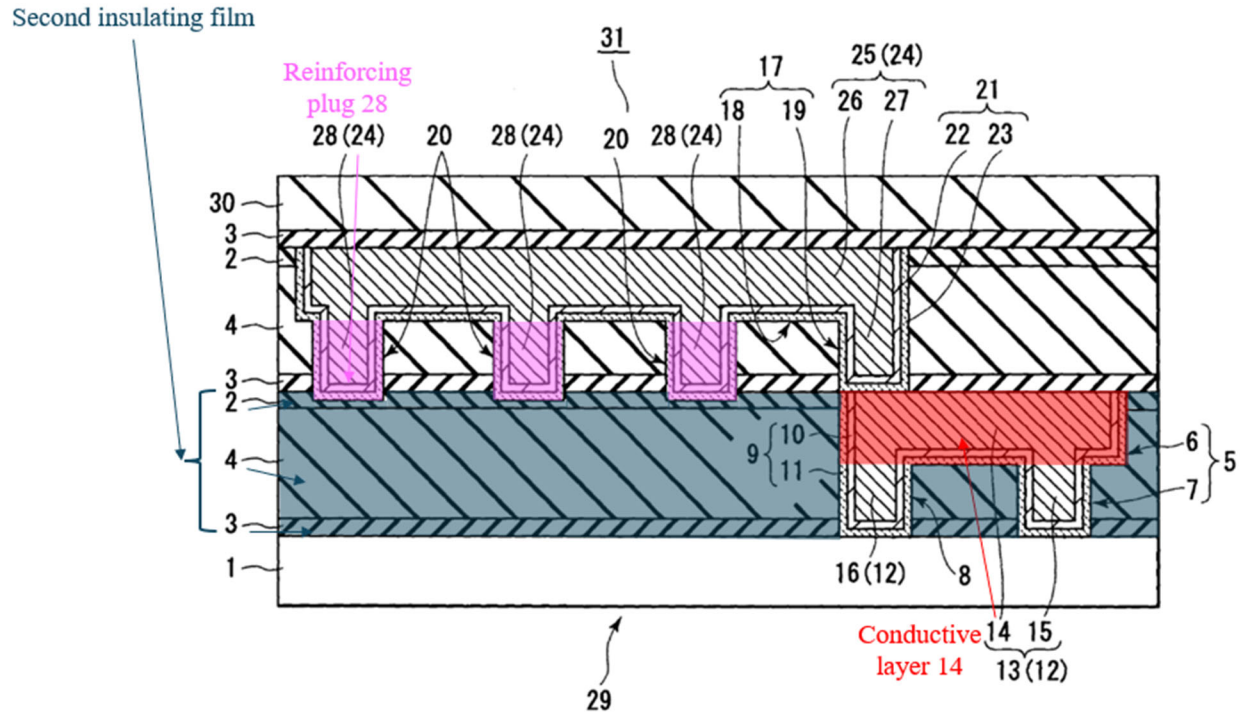


FIG. 8

Supra, §§VI.I.2.(g)-(h); TSMC-1003, ¶¶385-86.

Kurashima likewise teaches forming dummy wire 10 in first interlayer insulating film 4, and then dummy wire/via 17 is formed connecting to dummy wire 10:

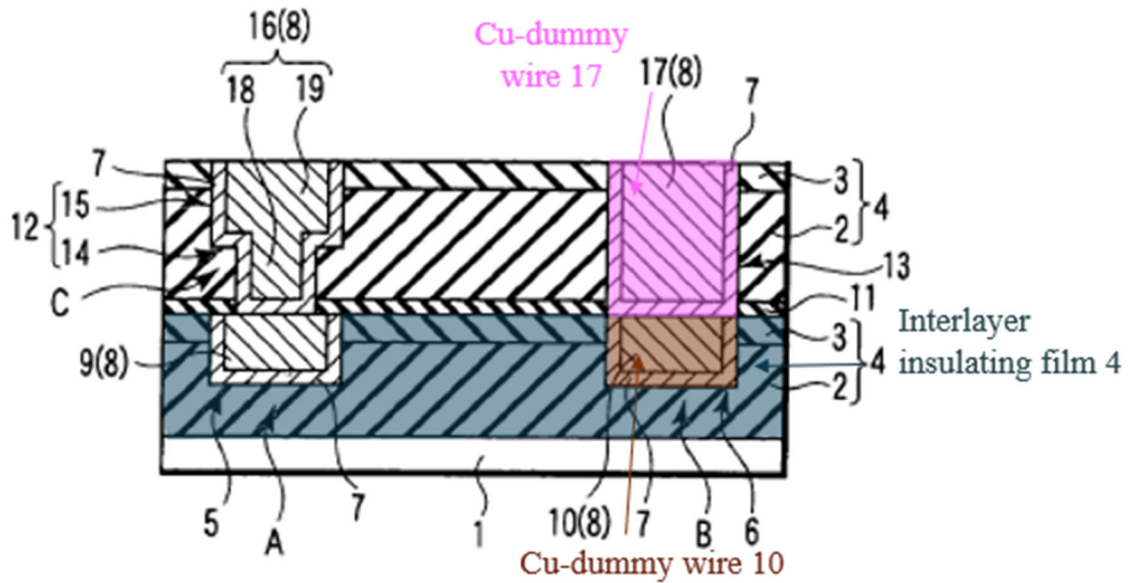
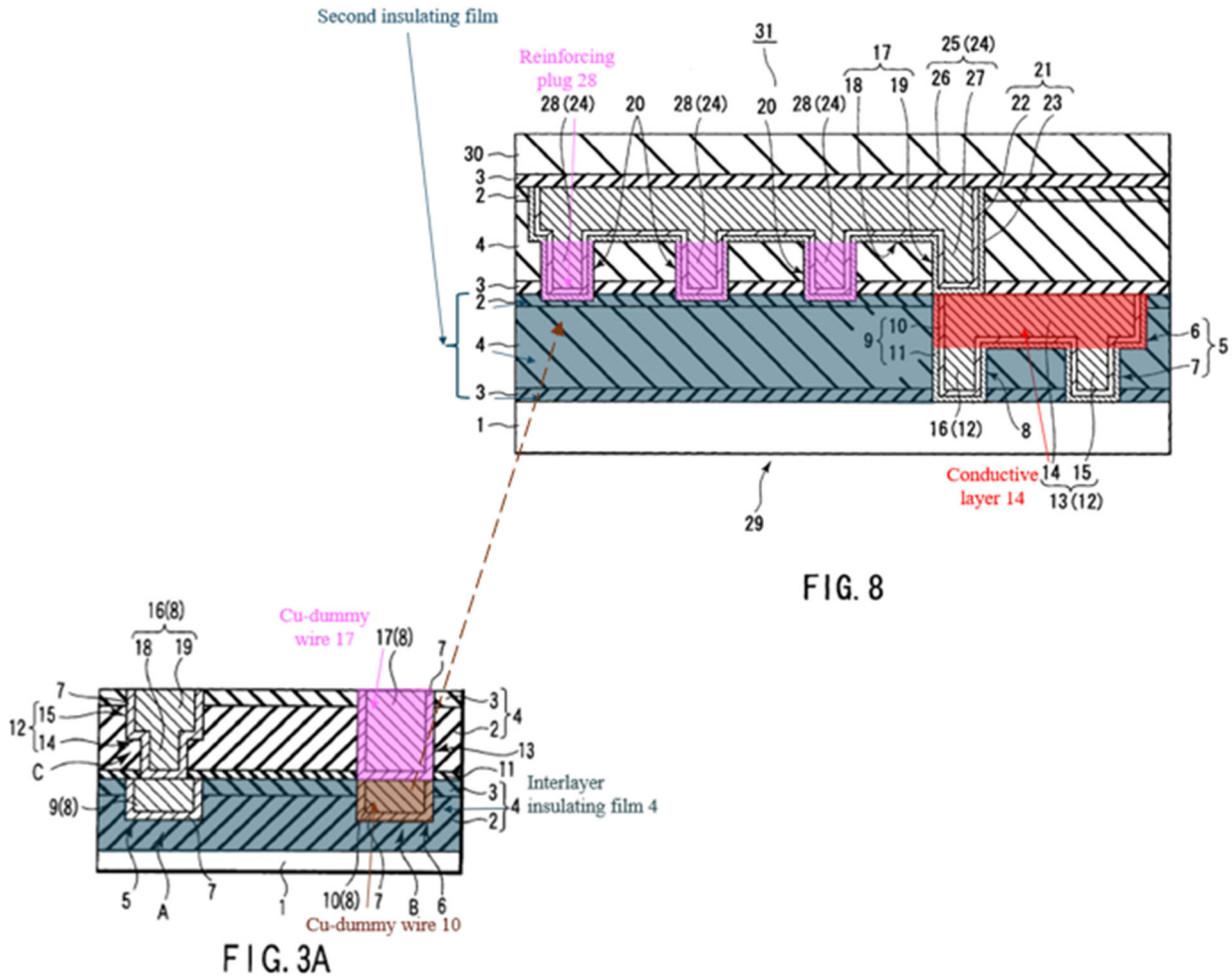


FIG. 3A

Supra, §VI.D.1; TSMC-1003, ¶¶387-88. The connection between dummy wire 10 and dummy wire 17 enhances the adhesion between insulating layers and improves durability against CMP-induced stress. *Id.*

d) Combining Hasunuma and Kurashima

A POSITA was motivated to improve the mechanical strength of Hasunuma's structure by applying Kurashima's teaching to connect Hasunuma's reinforcing plug(s) 28 to a dummy interconnect beneath them. TSMC-1003, ¶389. This suggested addition from Kurashima's Figure 3A to Hasunuma's Figure 8 structure is illustrated below:



Id.

A POSITA was motivated to incorporate Kurashima's dummy interconnect(s) into Hasunuma's device to increase the interlayer strength and reduce the likelihood of peeling or delamination between Hasunuma's lower films 4 and 2. See TSMC-1011, 5:63-6:32, 8:14-34, Figs. 5A-5B; TSMC-1003, ¶¶390-92. Kurashima's dummy plug-dummy interconnect structure also provided additional structural support and uniformity during the polishing step to reduce

dishing. *See* TSMC-1011, 5:63-6:32; TSMC-1007, 4:12-44; TSMC-1003, ¶¶393-94.

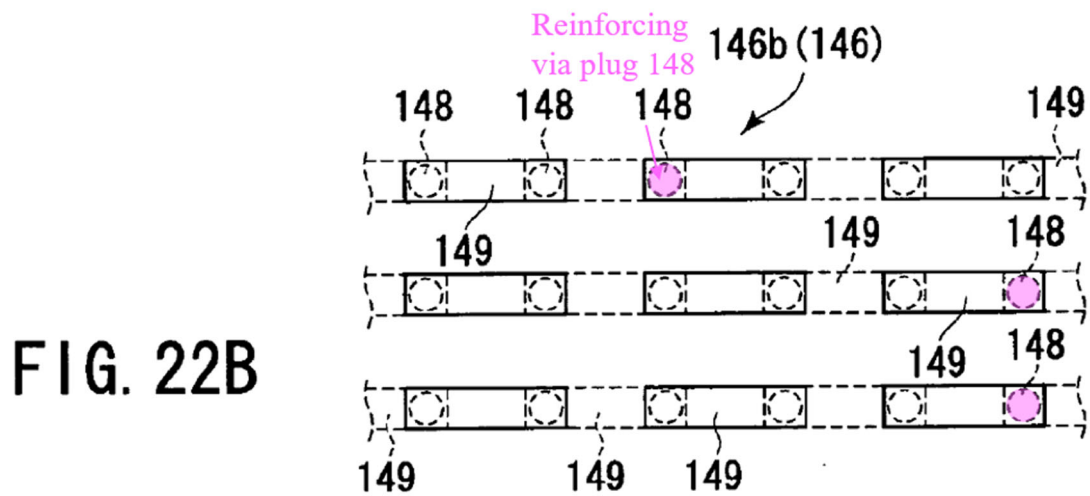
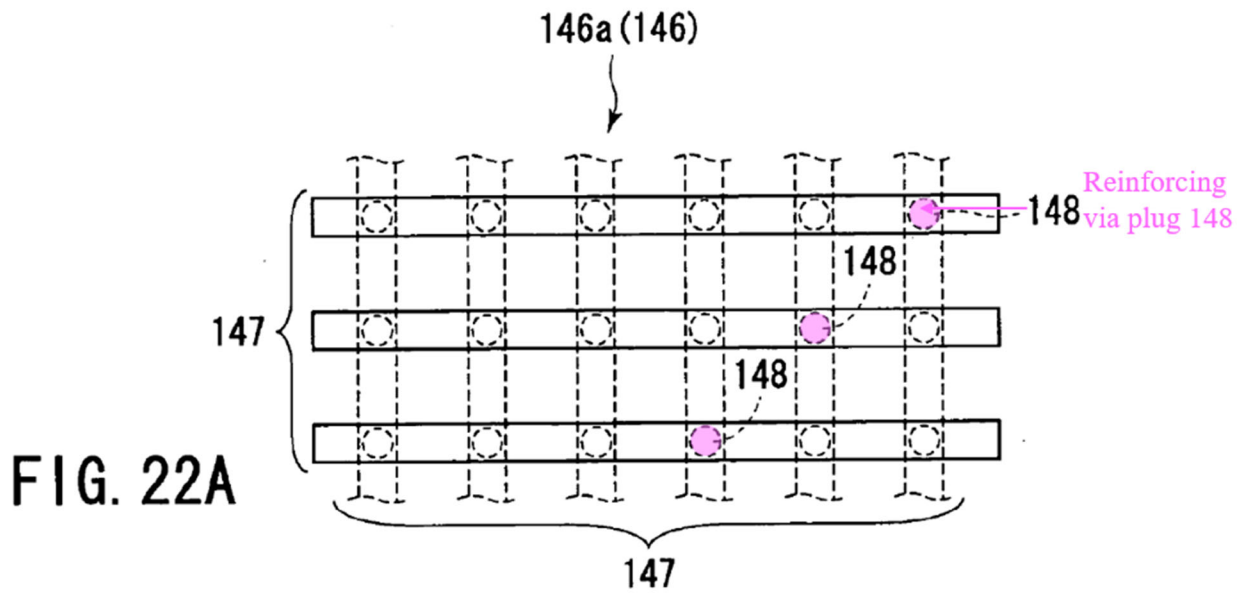
A POSITA would have expected success when incorporating Kurashima's dummy plug-dummy interconnect structure into Hasunuma's device, which entailed only the positioning of a dummy interconnect beneath one or more of Hasunuma's dummy vias/reinforcing plugs 28. TSMC-1003, ¶395. Creation of the dummy interconnect would have been easily accomplished using the same processing steps Hasunuma uses to create its conductive layer 14, with a reinforcing plug 28 connected thereto as part of building the next level in Hasunuma's Figure 8 structure. *Id.*

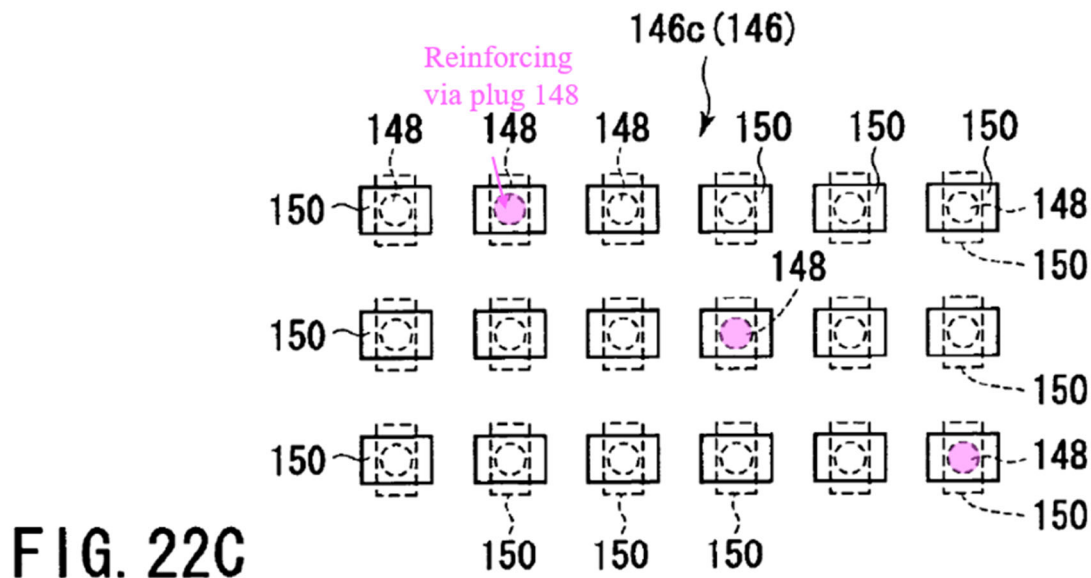
2. Claim 5

As discussed *supra*, §VI.J.1, Kurashima suggests adding a dummy interconnect to Hasunuma.

a) [5.a]

Hasunuma discloses that its dummy vias ("reinforcing via plugs") can be circular, such as in Figures 19A, 22A-22C and 24A-27C.





TSMC-1003, ¶397. Hasunuma also discusses their “diameter.” TSMC-1005, ¶[0127].

Circular vias were an obvious, easily-achieved design choice for Figure 8, being both well-known and easier to process. TSMC-1003, ¶¶398-99; *supra*, §§VI.C.2.(a), C.3.

b) [5.b]

Hasunuma’s reinforcing plug 28 (“dummy via”) has a diameter of 0.13 μm , substantially equal to the width of its reinforcing layers, such as shown in Figures 22A and 24A. TSMC-1005, ¶[0127], Figs. 22A, 24A; *supra*, §VI.J.2.(a).

The combination of Hasunuma and Kurashima results in the width of Hasunuma’s reinforcing plug 28 (“dummy via”) being substantially equal to the width of the first dummy interconnect, as disclosed by Kurashima. TSMC-1003,

¶¶400-03. Accordingly, when combined for the reasons discussed *supra*,

§VI.J.1.(d), Hasunuma and Kurashima render claim 5 obvious. *Id.*

K. Ground 10: Claim 6 Is Obvious Over Hasunuma, Kurashima and Iizuka

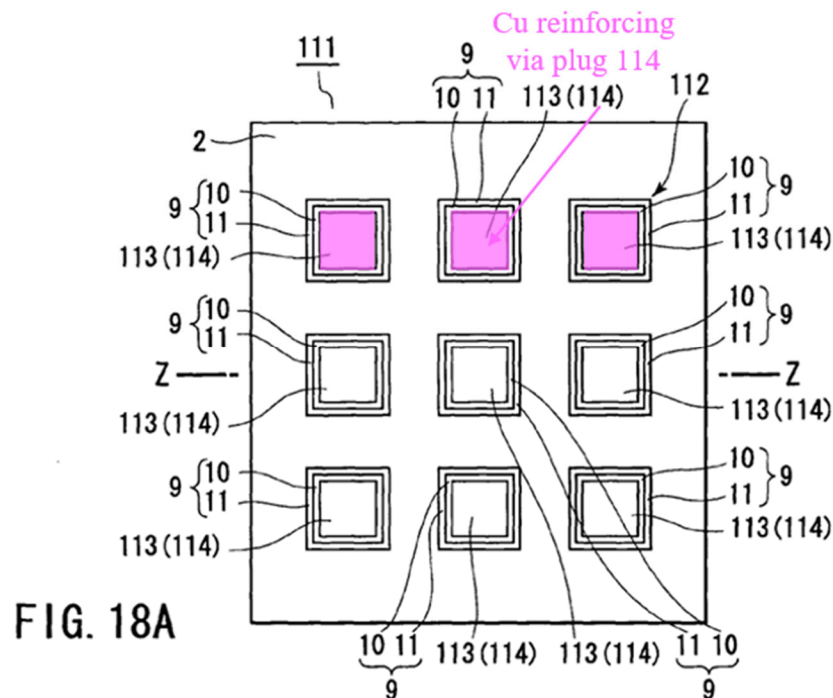
Hasunuma, Kurashima, and Iizuka render claim 6 obvious. TSMC-1003,

¶¶404-13.

1. Claim 6

a) [6.a]

Hasunuma discloses dummy vias (e.g., “Cu reinforcing via plug 114”) that are square:



TSMC-1005, Fig. 18A; TSMC-1003, ¶406.

Iizuka likewise teaches square-shaped vias. TSMC-1008, 9:45-47. Square dummy vias were a well-known design option that could be easily implemented. TSMC-1004, Figs. 2, 5, 9; TSMC-1013, 9:45-49; TSMC-1014, ¶[0092], Figs. 8, 14; TSMC-1003, ¶407. Additionally square-shaped vias provided the added advantage of increased contact area with interconnects above and/or below the vias and implementation of a more compact area with better space utilization. *Id.*; TSMC-1039, 5:27-32.

Thus, it was obvious to implement Hasunuma's vias (conductive plugs 27) and dummy vias (reinforcing plugs 28) with a square shape, as disclosed by Hasunuma and taught by Iizuka, which would have been easily achieved. TSMC-1003, ¶¶408-09; *see also supra*, §§VI.C.1, C.3; *infra*, §§VI.L.1, L.3.

b) [6.b]

Hasunuma teaches vias having a dimension of “about 0.13 μm ,” and wiring layer 13 (which includes the first interconnect (conductive layer 14)) also having a width of “about 0.13 μm .” TSMC-1005, ¶[0127].

It was obvious, when implementing square dummy vias as taught by Iizuka and Hasunuma, to utilize dummy via side dimensions equal to the width of the dummy interconnect (as suggested by both Hasunuma (*id.*) and Kurashima (*supra*, §§VI.D.2-3)), given that both Hasunuma and Kurashima teach equal sizes/widths for their vias and interconnects. TSMC-1003, ¶¶410-13. Such sizing ensured

secure connections while minimizing the dummy wiring footprint and undesired parasitic capacitance and cross-talk with adjacent wirings. *Supra*, §VI.D.3; TSMC-1003, ¶413.

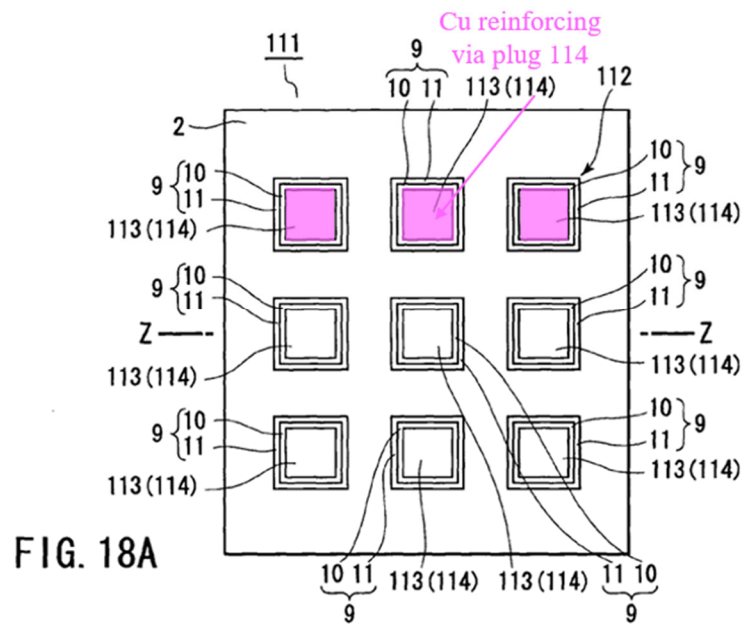
A POSITA would have expected success given that square vias were common, and that sizing the landing wire/interconnect relative to the via was a standard design consideration, as confirmed by Hasunuma teaching a via having a same size (0.13 μm) as the width (0.13 μm) of the interconnect connected to it (TSMC-1005, ¶[0127]). TSMC-1003, ¶413.

L. Ground 11: Claims 19-20 Are Obvious Over Hasunuma and Watanabe

Hasunuma and Watanabe render claims 19-20 obvious. TSMC-1003, ¶¶414-32.

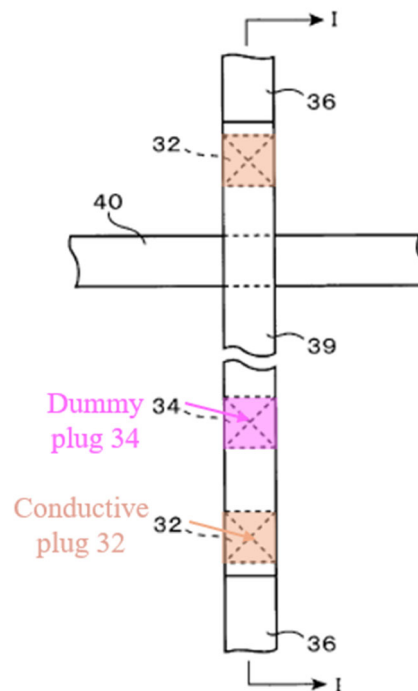
1. Claim 19

Hasunuma discloses square-shaped dummy vias as a known design option (*supra*, §VI.K.1.(a); TSMC-1003, ¶¶416-17):



Additionally, Watanabe discloses square-shaped vias and dummy vias, as seen for example in Watanabe's Figure 2:

FIG. 2



Supra, §VI.A.5; TSMC-1003, ¶418.

Prior to the '623 patent, both vias and dummy vias were commonly designed and fabricated with square cross-sections. TSMC-1008, 9:45-47 (“[T]he via-hole may have any configuration, such as a **square**, rectangle or circle.”), 10:8-11; TSMC-1013, 9:45-49; TSMC-1039, 5:27-32. Thus, square vias were an obvious design option that could have been easily implemented with a reasonable expectation of success. TSMC, 1003, ¶¶419-24; *supra*, §§VI.A.5, VI.F.3-4. Additionally, square-shaped vias provided the added advantage of increased contact area with interconnects above and below the vias. TSMC-1039, 5:27-32; TSMC-1003, ¶421.

Accordingly, it was obvious in view of Hasunuma’s and Watanabe’s disclosures of square vias and the state of the art at the time to make both Hasunuma’s vias and dummy vias substantially square in a planar shape. TSMC-1003, ¶¶419-24.

2. Claim 20

Hasunuma describes its vias and dummy vias as having identical widths (TSMC-1005, ¶[0127]), and Watanabe’s plan view figures (e.g., Figures 2, 4, 9) also consistently disclose square vias and dummy vias having identical side lengths. *Supra*, §§VI.A.5-6; TSMC-1003, ¶¶426-28. Watanabe’s simulation model likewise assigns identical dimensions (0.15 μm) to its functional and

dummy vias (TSMC-1004, ¶[0083]), further suggesting that the vias and dummy vias have identical side dimensions. TSMC-1003, ¶428.

In implementing Hasunuma's vias and dummy vias as squares (*supra*, §VI.L.1), it was obvious to make the vias and dummy vias substantially the same size (i.e., substantially the same side lengths), especially for design consistency and process commonality, as suggested by Watanabe's figures and modeling. TSMC-1003, ¶429.

3. Combination of Hasunuma and Watanabe

Both Hasunuma and Watanabe address similar problems (reliability in damascene-built interconnect structures) with similar foundational solutions (dummy vias extending from the interconnects). It would have been nothing more than a simple substitution to adopt Watanabe's specific via/dummy via sizes and shapes in Hasunuma's device. TSMC-1003, ¶430. For example, choosing specific shapes (e.g., square) and dimensional relationships (via and dummy via sizes) as taught by Watanabe would have been routine design choices to meet particular layout or process requirements within Hasunuma's framework. *Id.*

Furthermore, it was obvious to combine specific advantageous embodiments or features from one known approach (Watanabe) into another (Hasunuma) if it led to an improved or more optimized overall design. *Id.*, ¶431. The underlying physics of stress migration, electromigration, and mechanical reinforcement in

both Watanabe's and Hasunuma's devices are similar or the same (see, e.g., TSMC-1004, ¶¶[0016]-[0019], [0022]-[0033], [0071]-[0078], [0087], [0091]; TSMC-1005, ¶¶[0084]-[0089], [0103], [0115]-[0125]), such that a POSITA would have appreciated that dummy via geometry helps with both stress migration issues and mechanical stability for the interconnect structure. TSMC-1003, ¶431. Accordingly, it would have been at most routine optimization for a POSITA to determine the beneficial shape (e.g., square) and relative sizes (e.g., square side dimensions) of the vias and dummy vias. *Id.*; *see also* TSMC-1002, 244-45, 292-96.

There would have been a high expectation of success in combining these teachings. TSMC-1003, ¶432. Both references describe conventional semiconductor materials and dual-damascene manufacturing processes. Incorporating Watanabe's specific via/dummy via shapes and dimensional relationships into Hasunuma's device would involve standard layout/patterning modifications using identical process steps, all well within a POSITA's capabilities. *Id.* Indeed, the functions of Hasunuma's and Watanabe's dummy vias are congruent, making their features readily combinable. *Id.*

M. Ground 12: Claim 24 Is Obvious Over Hasunuma and Iizuka

Hasunuma and Iizuka render claim 24 obvious. TSMC-1003, ¶¶433-47.

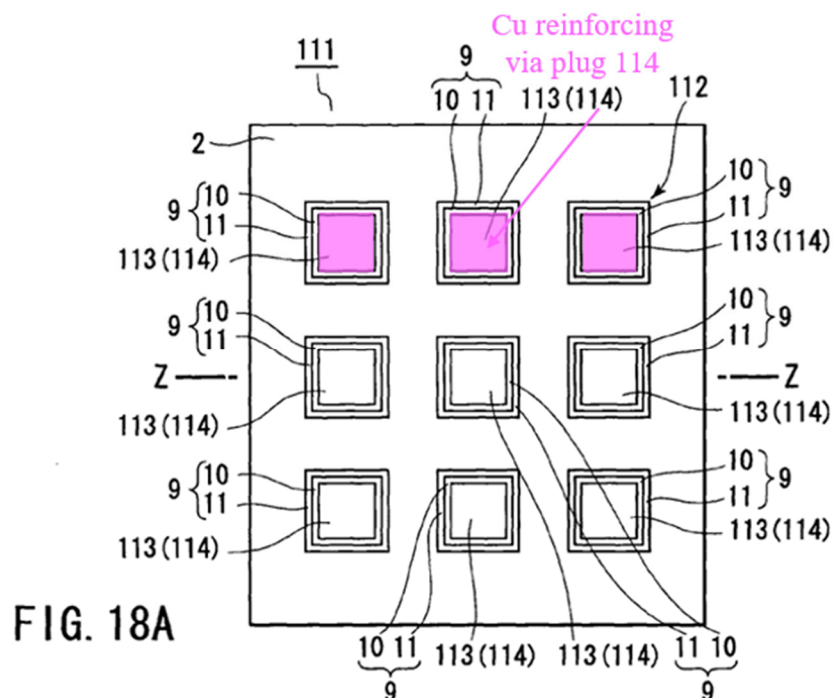
1. Claim 24

a) [24.a]

Iizuka teaches square-shaped vias. TSMC-1008, 9:45-47 (“the opening of the via-hole may have any configuration, such as a square, rectangle or circle.”).

It was obvious to implement Hasunuma’s vias (i.e., conductive plugs 27) with this common square shape. TSMC-1003, ¶¶434-43.

For the same reasons discussed *supra*, §§VI.L.1-3, square-shaped vias were a simple design choice, which Hasunuma itself discloses in plan-view figures, such as Figure 18A:



Id., ¶¶437-42. A POSITA would have expected success in implementing square vias in Hasunuma's Figure 8 embodiment because it was a known substitution option and was known to work. *Id.*, ¶¶440-43; *supra*, §§VI.K-VI.L.

b) [24.b]

Hasunuma teaches vias having a dimension of "about 0.13 μm ," and in the same paragraph, teaches that wiring layer 13 (which includes the first interconnect (conductive layer 14)) also has a width of "about 0.13 μm ." TSMC-1005, ¶[0127]; TSMC-1003, ¶445.

A POSITA, implementing the square via shape taught by Iizuka and in Hasunuma's Figure 18A, would have found it obvious to utilize square vias having side dimensions equal to the width of the first interconnect, especially given that Hasunuma expressly taught equal sizes for its via and first interconnect. TSMC-1003, ¶446. Furthermore, it was common practice to design vias with the same width as the underlying "first" interconnect. *See, e.g.*, TSMC-1004, Figs. 2, 4, 9 (disclosing square vias having the same side dimension as the underlying interconnect); TSMC-1003, ¶446. This ensures that the vias make robust, full-width contact for good electrical connection with the underlying interconnect. TSMC-1003, ¶446. It was therefore obvious to apply this standard design practice to Hasunuma's vias and underlying interconnect. *Id.*

It was at most routine optimization to determine the beneficial shape (e.g., square) and relative sizes (e.g., square side dimensions) of the vias and interconnect. *Id.*; *see also* TSMC-1002, 244-45, 292-96. A POSITA would have had a reasonable expectation of success, since square shapes and matching via and interconnect sizes were readily achievable using known fabrication techniques. TSMC-1003, ¶¶446-47.

N. Ground 13: Claims 29-30 Are Obvious Over Hasunuma and Nasu

Hasunuma and Nasu render claims 29-30 obvious. TSMC-1003, ¶¶448-71.

1. Claim 29

a) [29.a]

Hasunuma discloses vias and dummy vias having circular cross sections. *Supra*, §VI.I.3.(a); TSMC-1003, ¶450. Nasu also refers to the “diameter” of its via openings (TSMC-1032, ¶[0023]), thus disclosing circular cross sections. TSMC-1003, ¶451. Moreover, the choice of via shape was a mere design choice, with circular shapes well-known as illustrated by Iizuka. *See, e.g.*, TSMC-1008, 9:45-47. Circular-shaped vias also had manufacturing and stress benefits. TSMC-1038, 7:62-67; TSMC-1003, ¶452; *supra*, §VI.C.3.

b) [29.b]

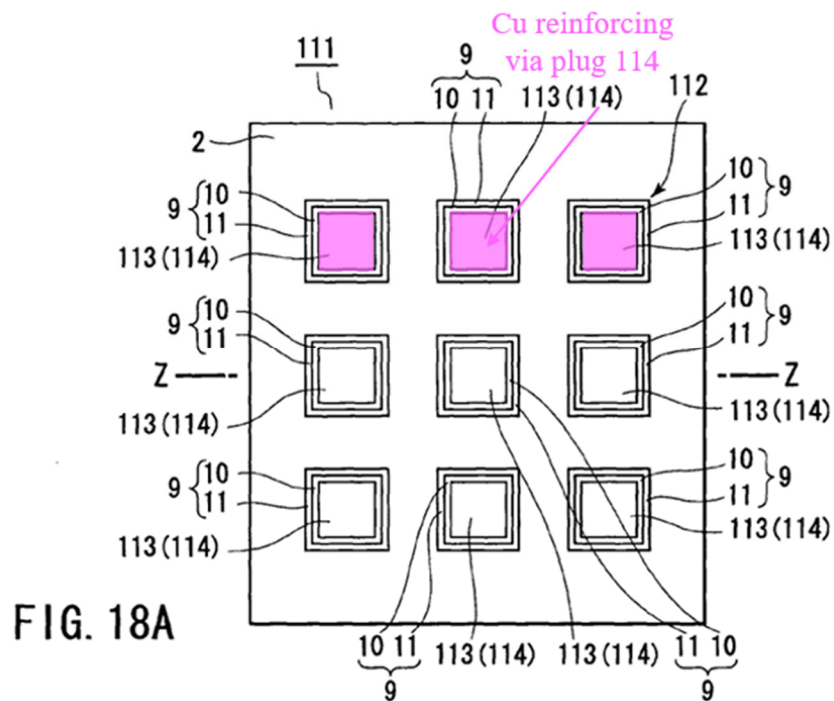
As noted previously, Nasu teaches dummy vias having smaller cross sections than the regular vias. *Supra*, §§VI.F.1-2. The obviousness of applying

this teaching to Hasunuma's structure is explained *infra*, §VI.N.3. TSMC-1003, ¶¶453-56.

2. Claim 30

a) [30.a]

Hasunuma discloses square-shaped dummy vias as a known design option:



Supra, §VI.K.1.(a); TSMC-1003, ¶¶457-58. Nasu also discloses square-shaped via holes 11 and square dummy holes 10:

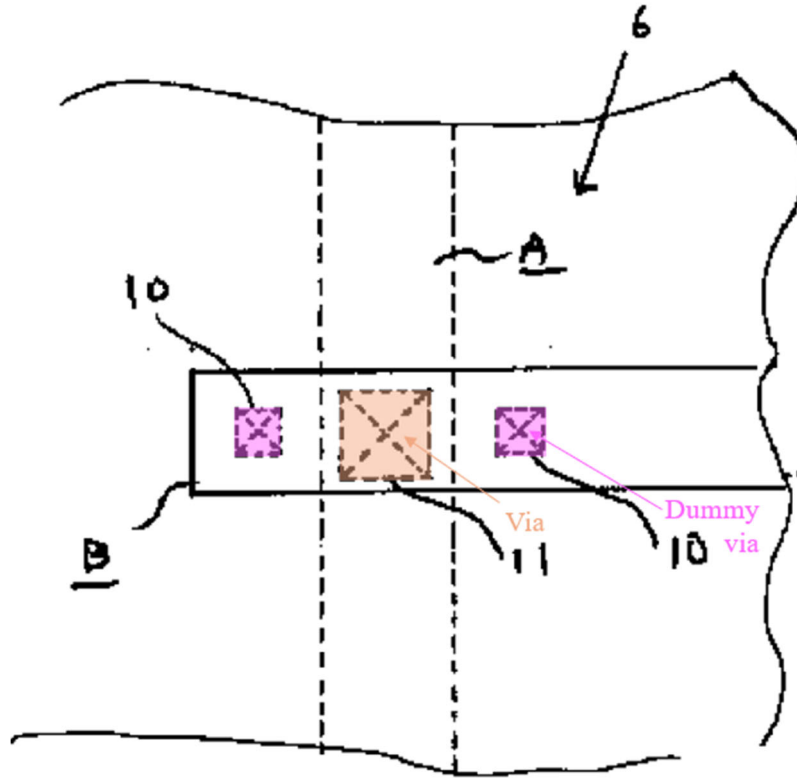


FIG. 6

TSMC-1032, Fig. 6; TSMC-1003, ¶459. Square-shaped vias/dummy vias were well-known and obvious. *Supra*, §§VI.C.1-3, VI.K.1.(a), VI.L.1-3; TSMC-1003, ¶¶460-61.

b) [30.b]

As previously discussed (*supra*, §§VI.F.3, VI.N.1.(b)), Nasu's dummy holes 10 have a smaller side dimension than via hole 11:

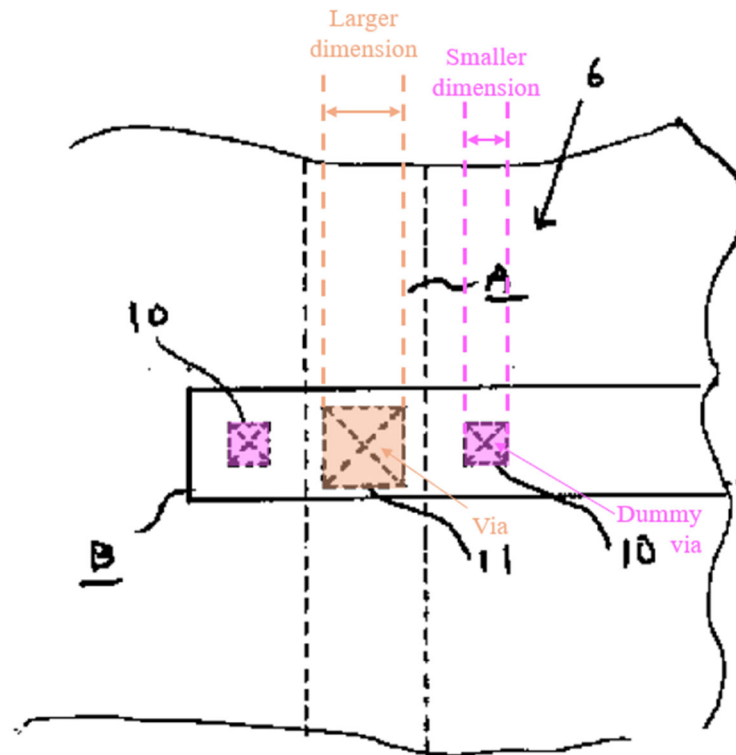


FIG. 6

TSMC-1032, ¶¶[0024], [0028], Fig. 6; TSMC-1003, ¶¶462-64.

3. Combination of Hasunuma and Nasu

Whether implemented as circles or squares, a POSITA would have been motivated to incorporate into Hasunuma smaller dummy vias compared to the functional vias as taught by Nasu to enhance the reliability of multilayer interconnect structures. TSMC-1003, ¶¶465-70. Such dummy vias address reliability issues by providing excess metal atoms and better collecting vacancies, while being locatable over underlying interconnect layers when an electrical connection must be avoided. *Id.*; *see supra*, §VI.F.4.

Because dummy vias by definition carry no current, they are free to be made smaller than the active vias. TSMC-1003, ¶468. Fabricating vias/dummy vias of different, controlled sizes and shapes in the same device was a known capability as demonstrated by Nasu and Hasunuma, leading to a high expectation of success in implementing such a combination to arrive at claims 29-30. *Id.*, ¶471.

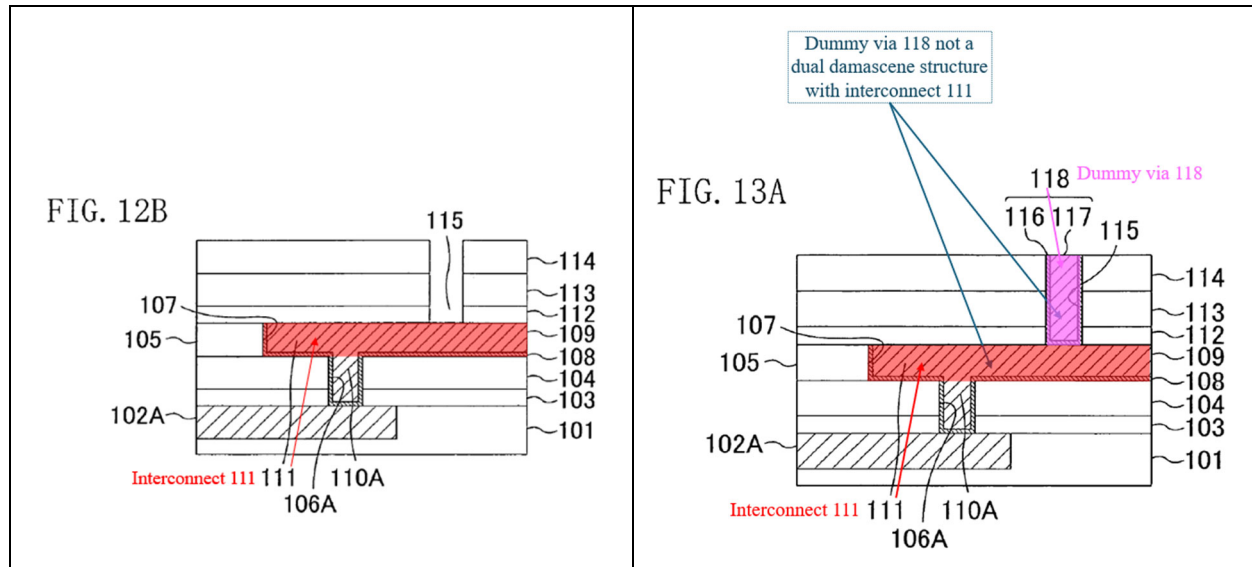
O. Ground 14: Claims 33-38 Are Obvious over Hasunuma and Kamoshima

1. Lack of Written Description Support

The '623 patent lacks written description support for claim 33 and, thus, also claims 34-38 that depend from claim 33. TSMC-1003, ¶¶477-79. Claim 33 requires the dummy via be connected to the “upper surface” of the second interconnect. The only embodiment in the '623 patent that shows a dummy via connected to a second interconnect upper surface is Embodiment 5 of Figure 13B, which is made according to the method of Figures 11-13. TSMC-1001, 22:27-24:6. Because claim 33 depends on claim 1, it inherits the limitation that “the second interconnect and the dummy via form a dual damascene structure.”

Embodiment 5, however, forms dummy via 118 only after forming second interconnect 111 and, thus, second interconnect 111 and dummy via 118 do not form a dual damascene structure (*supra*, §II.A), which is in conflict with claim 1's requirement. TSMC-1001, 22:47-23:2, Figs. 12A-13B. The lack of a dual

damascene structure is understood from Figures 12B and 13A, which show dummy via 118 made in a different step from second interconnect 111:



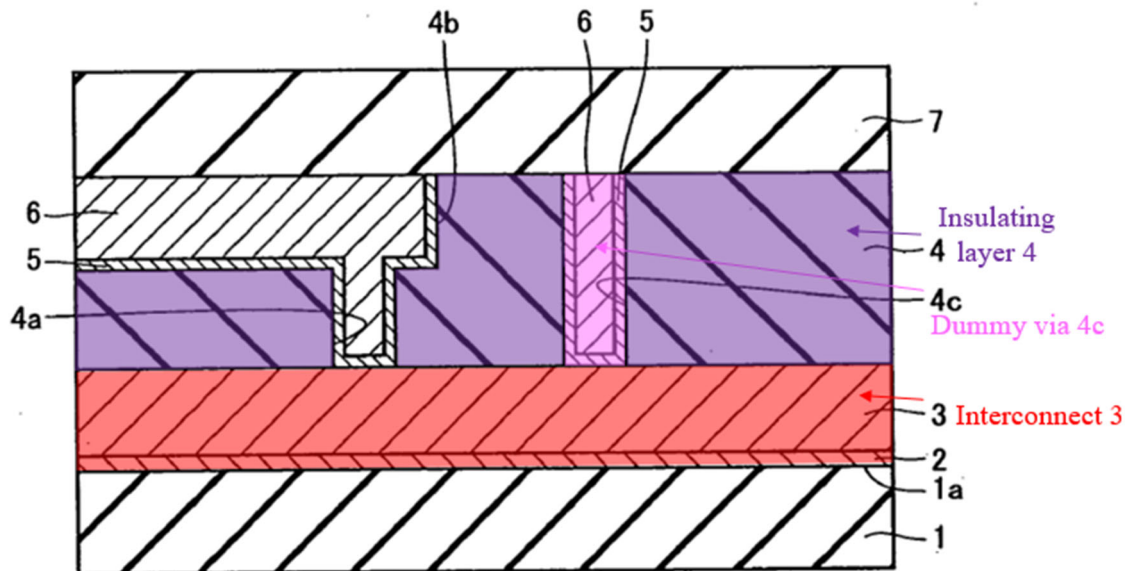
Id., Figs. 12B, 13A; TSMC-1003, ¶¶473-76, 478. Consequently, the '623 patent specification fails to describe a device satisfying both claim 1's dual-damascene limitation and claim 33's top-surface-connection limitation for the dummy via. TSMC-1003, ¶478.

If claim 33 is interpreted as reading on Embodiment 5/Figure 13A in the '623 patent (despite the irreconcilable conflict between claims 1 and 33), then claims 33-38 are obvious over Hasunuma and Kamoshima, as explained below. *Id.*, ¶¶472, 479-507.

2. Kamoshima

Kamoshima discloses dummy vias extending from an interconnect top surface:

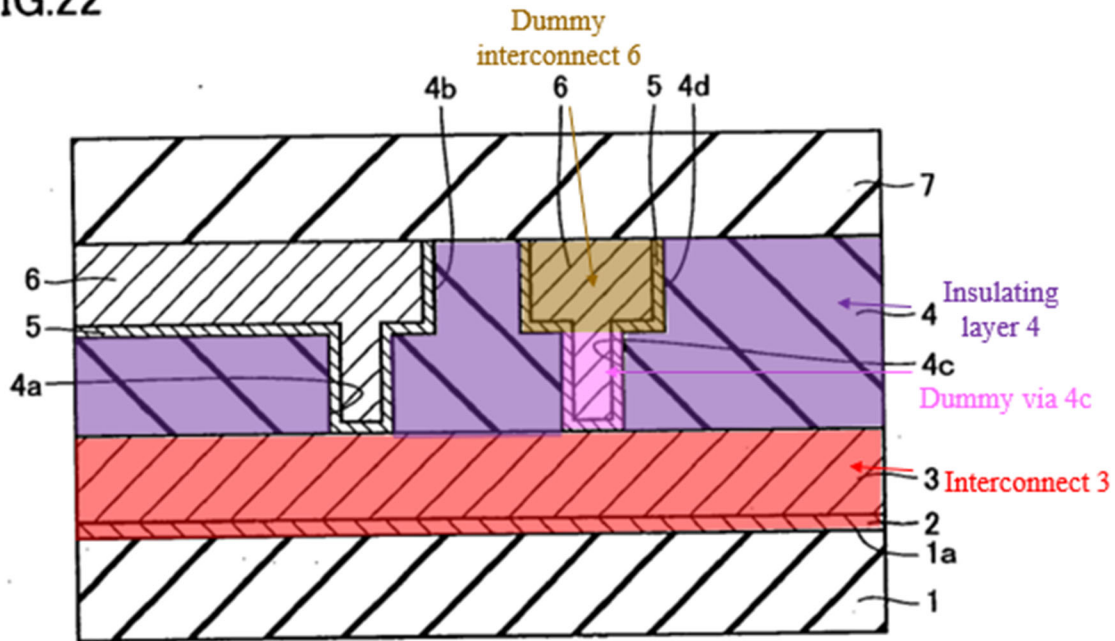
FIG.16



TSMC-1009, ¶¶[0085]-[0086], Fig. 16; TSMC-1003, ¶480.

Kamoshima further discloses a dummy interconnect 6 on and in contact with the top of upwardly-directed dummy via 4c:

FIG.22



TSMC-1009, ¶¶[0090]-[0092], Fig. 22; TSMC-1003, ¶¶481-82.

3. Claim 33

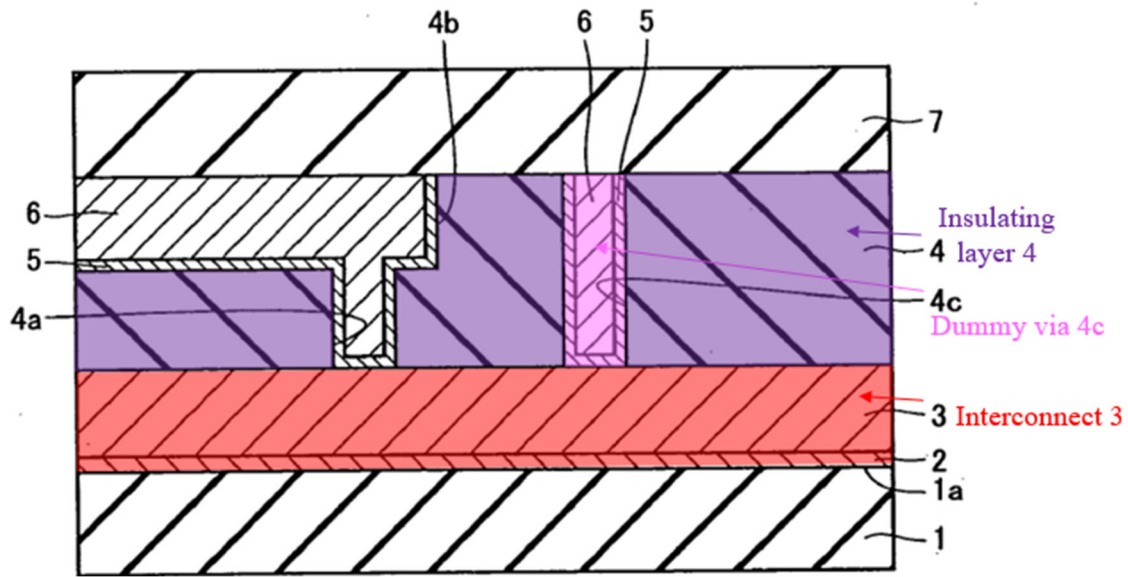
In Hasunuma's Figure 8, the dummy via (reinforcing plug 28) is connected to a bottom surface of the second interconnect (conductive layer 26). TSMC-1005, Fig. 8; TSMC-1003, ¶485. However, Hasunuma discloses additional options for all embodiments that "can appropriately be combined, used, or carried out."

TSMC-1005, ¶[0290]. One of these is for "the reinforcing plug to be connected to the upper surface of the conductive layer or the reinforcing metal layer may separately be provided so as to be connected to the reinforcing material provided above." *Id.*, ¶[0291]. In other words, Hasunuma teaches an alternative where the reinforcing plug (dummy via) extends from the upper surface of the interconnect,

such as Hasunuma's conductive layer 26, which satisfies claim 33 (when read on the '623 patent's Embodiment 5/Figure 13A). *Id.*, ¶¶[0290]-[0291], Fig. 8; TSMC-1003, ¶485.

Kamoshima likewise discloses dummy via 4c on a top surface of interconnection layer 3 for collecting microvoids:

FIG.16



TSMC-1009, ¶¶[0017], [0085]-[0088], Fig. 16; TSMC-1003, ¶486.

Thus, Hasunuma teaches having the reinforcing plug (dummy via) on the upper surface of the second interconnect, and Kamoshima teaches how (and why) to include a dummy via extending from an interconnect's top surface. It was obvious to implement Hasunuma's paragraph [0291] teaching, per Kamoshima's additional disclosure, to so modify Hasunuma's Figure 8 embodiment:

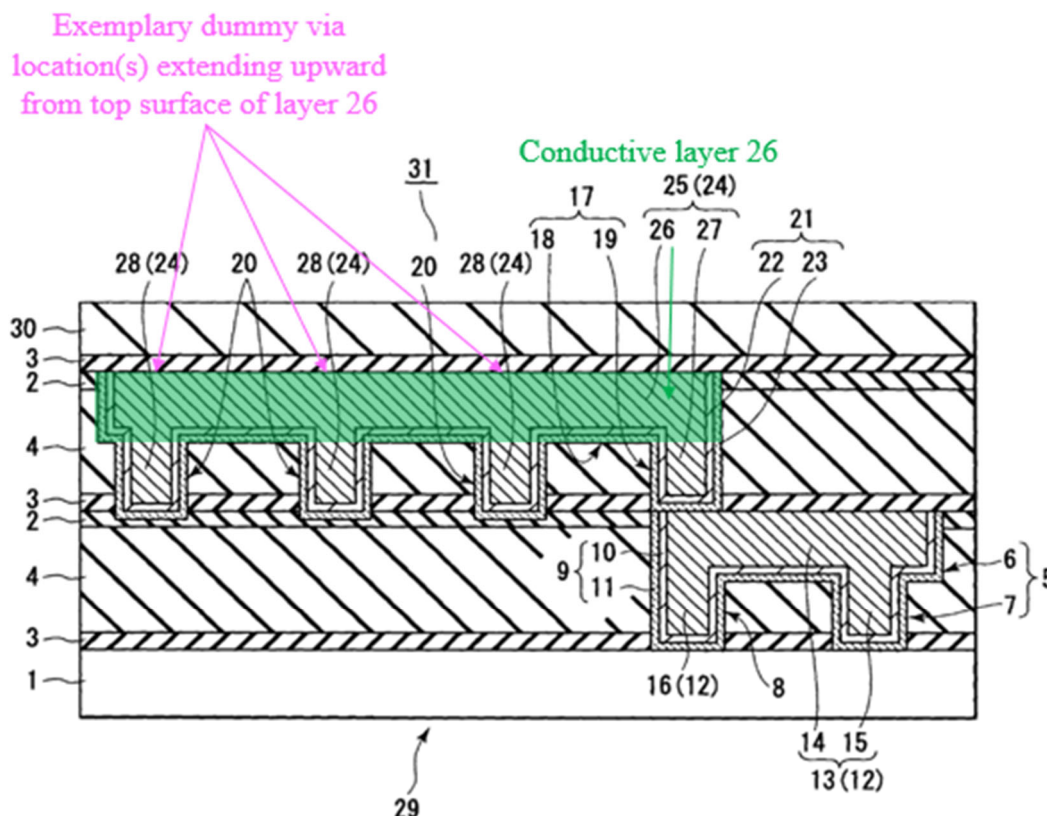


FIG. 8

TSMC-1003, ¶487.

4. Claim 34

Hasunuma discloses a third insulating film (e.g., film 3) formed on top of conductive layer 26. TSMC-1005, ¶[0111], Fig. 8; TSMC-1003, ¶489. Hasunuma also explains that the number of layers in the Figure 8 embodiment is not limited, and that more layers may be stacked on top. TSMC-1005, ¶¶[0297]-[0298]. When building additional interconnect and via layers atop the Figure 8 embodiment, another low relative dielectric constant film 4 and insulating film 2 would be stacked atop the topmost film 3 to form a “third insulating film” on top of the

second interconnect as indicated below, because films 3, 4, and 2 are provided for each interconnect/via layer:

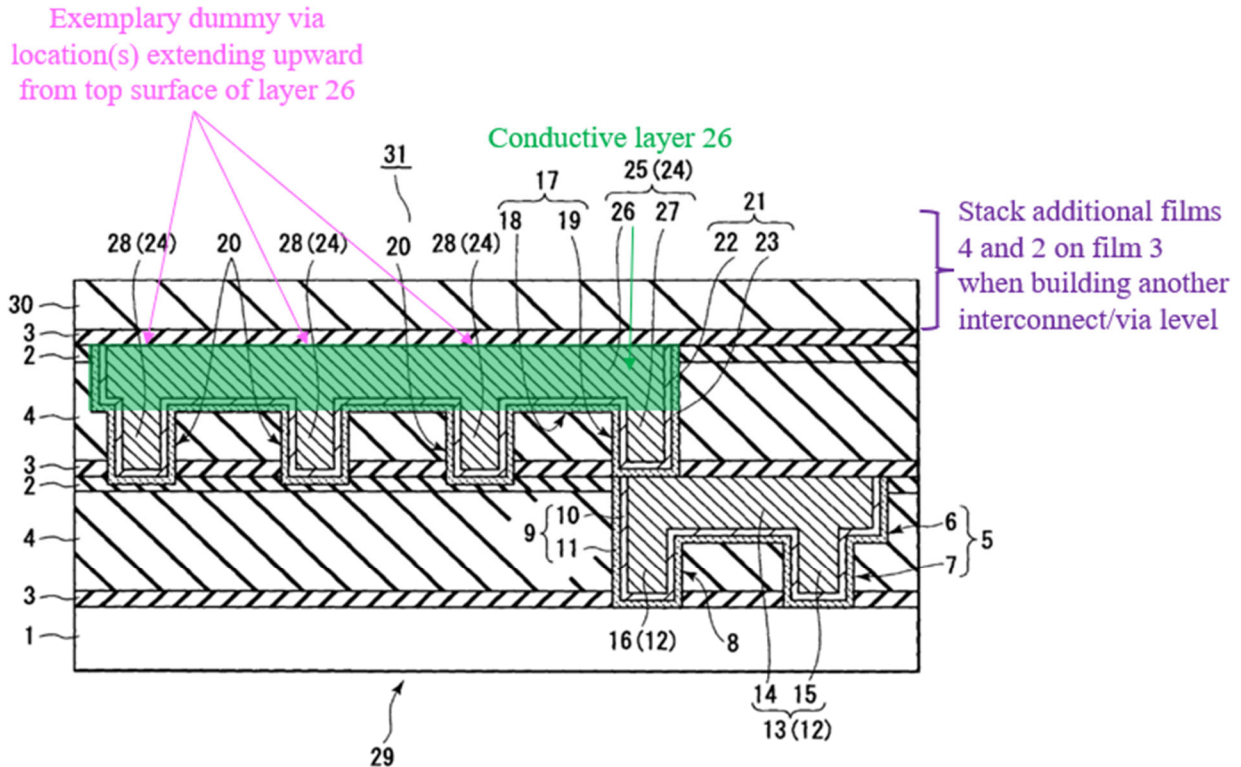
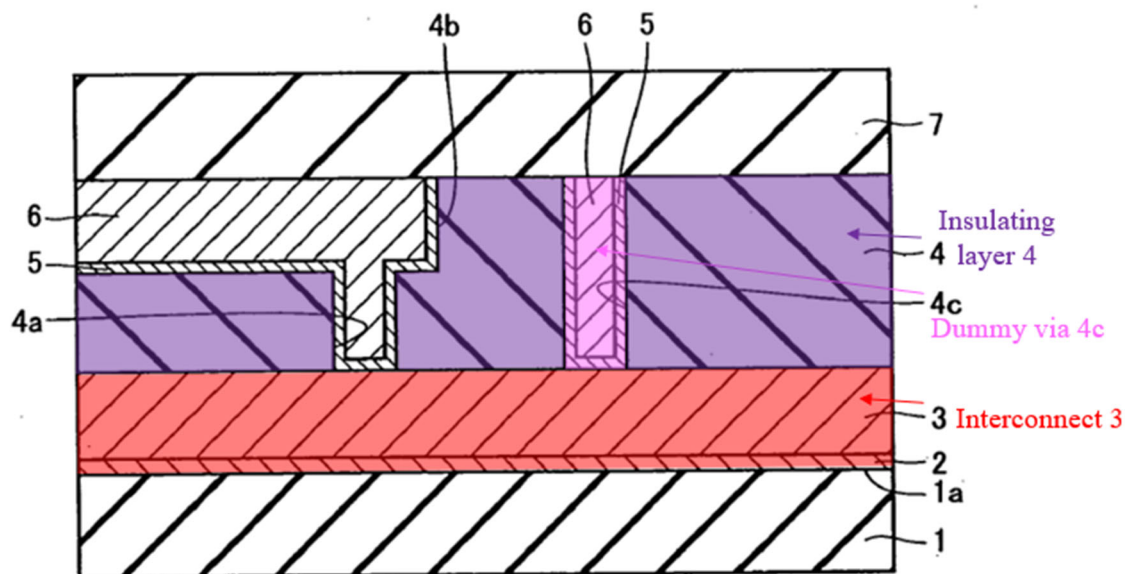


FIG. 8

TSMC-1003, ¶489.

Dummy vias (reinforcing plugs) extending upward from the second interconnect (conductive layer 26) surface would be formed in the additional 3-4-2 insulating film stack added onto conductive layer 26, such that the resulting dummy via is formed in a third insulating film on the second interconnect. *Id.*, ¶490. This arrangement is analogous to Kamoshima's formation of dummy via 4c in insulating layer 4, which is formed on interconnection layer 3:

FIG.16



Id.

Thus, when a dummy via is connected to and extends upward from the upper surface of a second interconnect, such as Hasunuma's conductive layer 26, it was obvious for the dummy via to be formed in a third insulating film formed on the second interconnect. *Id.*, ¶491.

5. Claim 35

As noted for claim 34, when adding additional levels to Hasunuma's Figure 8 embodiment, another film 4 and film 2 would be stacked atop the topmost film 3 in Figure 8. *Id.*, ¶493. Thus, the third insulating film would have a multilayer structure of films 3-4-2. *Id.*

Hasunuma's film 3 can be a SiN film, and film 2 can be a SiO₂ film.

TSMC-1005, ¶¶[0293], [0299]. Thus, Hasunuma's multilayer insulating film structure including films 2 and 3 can be formed with a SiN film and a SiO₂ film.

TSMC-1003, ¶494. It was obvious to use these materials because Hasunuma explicitly lists them as materials that can be used for those films 2 and 3 (as part of the repeating 3-4-2 film structure), and they are commonly used in interconnect structures. *Id.*, ¶¶492-94.

6. Claim 36

Hasunuma's reinforcing plugs 28 (dummy vias) include barrier metal film 21 and Cu film 24, which are conductive. TSMC-1005, ¶¶[0105]-[0108], Fig. 8. Likewise, Kamoshima's dummy plug 4c comprises barrier metal layer 5 and copper layer 6 (TSMC-1009, ¶[0086], Fig. 16), identical to the barrier film and conductive film depicted in the '623 patent's Figure 13B. TSMC-1003, ¶496.

It was therefore obvious for a dummy via extending from the top surface of Hasunuma's interconnect layer 26 to comprise a barrier film and conductive film ("second barrier film" and "second conductive film"), just as with Hasunuma's other dummy vias, and as in Kamoshima's Figure 16 for dummy via 4c and other prior art. *Id.*, ¶497.

7. Claim 37

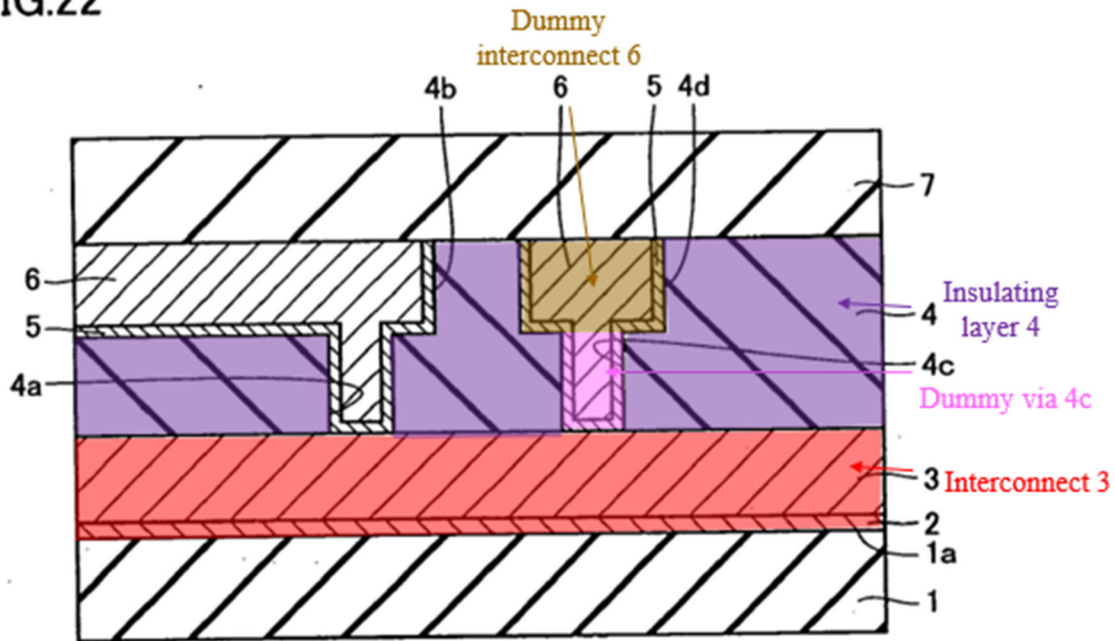
Both Hasunuma's and Kamoshima's dummy vias include copper. TSMC-1005, ¶¶[0105]-[0108], Fig. 8; TSMC-1009, ¶[0086], Figs. 1, 16. A POSITA would have understood and found it obvious that Hasunuma's dummy via (reinforcing plug) includes copper even when extending from the top surface of the interconnect, and as taught by Kamoshima regarding its dummy via 4c. TSMC-1003, ¶¶498-99.

8. Claim 38

Hasunuma teaches that “the reinforcing plug to be connected to the upper surface of the conductive layer...may separately be provided so as to be connected to the reinforcing material provided above.” TSMC-1005, ¶[0291]. Thus, Hasunuma teaches that the reinforcing plug (dummy via) is connected at its top end to a second dummy interconnect (“reinforcing material provided above”). TSMC-1003, ¶501.

Kamoshima also teaches a dummy interconnect (dummy interconnection layer 6) on top of upward-extending dummy via 4c, as illustrated in Figure 22:

FIG.22



TSMC-1009, ¶[0090] (noting that “dummy interconnection layer 6 does not electrically connect interconnection layer 3 to another element”), Figs. 1-8; TSMC-1003, ¶502.

Thus, both Hasunuma and Kamoshima teach the limitation of claim 38. Its implementation into Hasunuma's Figure 8 embodiment was obvious given Kamoshima's express illustration of such a structure. TSMC-1003, ¶¶500-03.

9. Combination of Hasunuma with Kamoshima

A POSITA was motivated to add a reinforcing plug (dummy via) to the top surface of Hasunuma's conductive layer 26 to achieve better resistance to mechanical stresses. *Id.*, ¶504. Adding one or more reinforcing plugs extending upwards into the third insulating film, including attachment to a reinforcing metal

layer (i.e., dummy interconnect) above when present, would clamp conductive layer 26 between two mechanically strong layers. *Id.*; TSMC-1011, 8:35-54.

Additionally, as taught by Kamoshima, dummy vias attached to the top surface of an interconnect help protect against microvoid aggregation at adjacent active vias. TSMC-1009, ¶¶[0017], [0085]-[0088]; TSMC-1003, ¶505.

Specifically, when another level of vias and interconnects are added atop Hasunuma's Figure 8 embodiment (TSMC-1005, ¶¶[0291], [0297]-[0298]), Hasunuma's interconnect layer 26 will have one or more active vias connecting it to the interconnect level above. TSMC-1003, ¶505. Dummy vias extending upward from the top surface of interconnect layer 26 would thus achieve Kamoshima's stated benefit of reducing void aggregation under such active vias, including when a dummy interconnect contacts the top of the dummy via, as in Kamoshima's Figure 22. TSMC-1009, ¶¶[0085]-[0092]; TSMC-1003, ¶505.

Incorporating Kamoshima's dummy interconnect, as seen in its Figure 22, into Hasunuma's structure would have also provided better, more uniform CMP processing. *Supra*, §II.B; TSMC-1003, ¶506.

A POSITA would have expected success in implementing dummy vias connected to a top surface of the conductive layer as in Hasunuma (along with dummy interconnects on top of the dummy vias, when desired) given Hasunuma's disclosure of such structures (TSMC-1005, ¶[0291]) and given Kamoshima's

teachings and figures showing how to make such structures. TSMC-1003, ¶507.

Hasunuma explains that more layers may be stacked atop the Figure 8 embodiment (TSMC-1005, ¶¶[0297]-[0298]), and so modifying Hasunuma's device would have involved no more than pattern adjustments when building dummy vias and dummy interconnects simultaneously with corresponding active vias and interconnects.

TSMC-1003, ¶507.

VII. GROUNDS FOR STANDING

Petitioner certifies that the '623 patent is available for review, and Petitioner is not barred/estopped from requesting review on the grounds identified herein.

VIII. MANDATORY NOTICES

A. Real Party-In-Interest

The real party-in-interest here is Taiwan Semiconductor Manufacturing Company Limited.

B. Related Matters

The '623 patent is asserted in *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Case No. 2:25-cv-00324 (E.D. Tex.).

C. Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3) and 42.10(a), Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. §42.10(b), a Power of Attorney accompanies this Petition.

Lead Counsel	Back-Up Counsel
Michael Houston Reg. No. 58,486 FOLEY & LARDNER LLP 321 North Clark Street, Suite 3000 Chicago, Illinois 60654 312-832-4500 mhouston@foley.com	Pavan Agarwal Reg. No. 40,888 FOLEY & LARDNER LLP 3000 K Street N.W., Suite 600 Washington, DC 20008 202-672-5300 pagarwal@foley.com Nicholas Lagerwall Reg. No. 63,272 FOLEY & LARDNER LLP 150 East Gilman Street, Suite 5000 Madison, Wisconsin 53703 608-257-5035 nlagerwall@foley.com

Petitioner consents to electronic service directed to the following email address: Foley_TSMC_623-2_IPR2025-01211@foley.com.

IX. PAYMENT OF FEES

The Office is authorized to charge fees for this Petition to Deposit Account No. 19-0741. Any additional fees that might be due are also authorized.

X. CONCLUSION

For the reasons given above, Petitioner requests IPR be instituted for the challenged claims.

Respectfully submitted,

Dated: July 25, 2025

By: /Michael R. Houston/

Michael R. Houston
Reg. No. 58,486
FOLEY & LARDNER LLP
Counsel for Petitioner

**CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME
LIMITATION, TYPEFACE REQUIREMENTS, AND TYPE STYLE
REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,966 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. §42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. §42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

Respectfully submitted,

Date: July 25, 2025

By: /Michael R. Houston/

Michael R. Houston
Reg. No. 58,486
FOLEY & LARDNER LLP
Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on July 25, 2025, true and correct copies of the foregoing document and supporting materials were served in its entirety on the Patent Owner at the following address of record listed on the USPTO's Patent Center via overnight service:

Michael J. Cherskov
Szymon M. Gurda
903 Commerce Dr.
Suite 310
Oak Brook, IL 60523

Courtesy copies of the same documents were served electronically on prosecution counsel and Patent Owner's litigation counsel by email at the following addresses:

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Respectfully submitted,

Date: July 25, 2025

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