IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

IPR2025-01212

U.S. Patent No. 7,439,623

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,439,623

TABLE OF CONTENTS

EXHIBIT LIST vi

LIST OF CHALLENGED CLAIMS x

I. RELIEF REQUESTED 1

II. STATE OF THE ART 2

A. Interconnects and Dual Damascene 2

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength 4

III. THE '623 PATENT 6

A. Overview 6

B. Prosecution History 7

C. Claim Construction 8

IV. ORDINARY SKILL 8

V. PRIOR ART 9

VI. DETAILED EXPLANATION OF GROUNDS 9

A. Ground 1: Watanabe Anticipates Claims 1-3, 7, 11-16, 21-22, 25-26, 28, 32, 39-40, and 42 9

1. Watanabe 10

2. Claim 1 13

3. Claim 2 30

4. Claim 3 35

5. Claim 7 35

6. Claim 11 37

7. Claim 12 39

8. Claim 13 40

9. Claim 14 40

10. Claim 15 42

11. Claim 16 43

12. Claim 21 44

13. Claim 22 46

14. Claim 25 48

15. Claim 26 50

16. Claim 28 50

17. Claim 32 51

18. Claim 39 53

19. Claim 40 53

20. Claim 42 54

B. Ground 2: Claims 4 and 8 Are Obvious Over Watanabe and Kurashima 56

1. Kurashima 56

2. Claim 4 58

3. Claim 8 61

C. Ground 3: Claims 9 and 17-18 Are Obvious Over Watanabe and Iizuka 65

1. Iizuka 65

2. Claim 9 66

3. Claim 17 67

4. Claim 18 67

5. Combination of Watanabe and Iizuka 68

D. Ground 4: Claims 45-47 Are Obvious Over Watanabe and Kamoshima 70

1. Kamoshima 70

2. Claim 45 71

3. Claim 46 75

4. Claim 47 76

E. Ground 5: Hasunuma Anticipates Claims 1, 11-15, 17-18, 21-22, 25-26, 28, 32, and 39-40 77

1. Hasunuma 77

2. Claim 1 79

3. Claim 11 86

4. Claim 12 87

5. Claim 13 87

6. Claim 14 87

7. Claim 15 88

8. Claim 17 89

9. Claim 18 90

10. Claim 21 91

11. Claim 22 92

12. Claim 25 93

13. Claim 26 94

14. Claim 28 94

15. Claim 32 94

16. Claim 39 96

17. Claim 40 97

F. Ground 6: Claims 2 and 8 Are Obvious Over Hasunuma and Kurashima 97

1. Claim 2 97

2. Claim 8 102

G. Ground 7: Aoyagi renders obvious Claims 1, 16, and 45-46 104

1. Aoyagi 104

2. Claim 1 108

3. Claim 16 118

4. Claim 45 119

5. Claim 46 121

H. Ground 8: Claim 47 Is Obvious Over Aoyagi and Hasunuma 122

I. Ground 9: Kunikiyo Renders Claims 1-2, 4, 7, 14, and 42 Unpatentable 124

1. Kunikiyo 124

2. Claim 1 124

3. Claim 2 135

4. Claim 4 139

5. Claim 7 140

6. Claim 14 142

7. Claim 42 143

J. Ground 10: Claims 9 and 17 Are Obvious Over Kunikiyo and Iizuka 144

1. Claims 9, 17 144

K. Ground 11: Claim 3 Is Obvious Over Kunikiyo and Watanabe 147

VII. GROUNDS FOR STANDING 149

VIII. MANDATORY NOTICES 150

A. Real Party-In-Interest 150

B. Related Matters 150

C. Counsel and Service Information 150

IX. PAYMENT OF FEES 151

X. CONCLUSION 151

EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,439,623
1002	File History of U.S. Patent No. 7,439,623 ("the '623 File History")
1003	Declaration of Dr. Reinhold Dauskardt
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. ("Watanabe")
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. ("Hasunuma")
1006	U.S. Patent Publication No. 2001/0019180 to Aoyagi et al. ("Aoyagi")
1007	U.S. Patent No. 6,717,267 to Kunikiyo ("Kunikiyo")
1008	U.S. Patent No. 5,250,465 to Iizuka et al. ("Iizuka")
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. ("Kamoshima")
1010	Reserved
1011	U.S. Patent No. 7,042,099 to Kurashima ("Kurashima")
1012	P. Andricacos, "Copper On-Chip Interconnections," *Interface*, *The Electrochemical Society*, pp. 32-37, 1999
1013	U.S. Patent No. 5,885,857 to Yamaha et al. ("Yamaha")

Exhibit No.	Description
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi et al. ("Igarashi")
1015	U.S. Patent No. 6,717,268 to Hau-Riege ("Hau-Riege")
1016	U.S. Patent No. 6,468,894 to Yang ("Yang")
1017	U.S. Patent No. 6,022,808 to Nogami ("Nogami")
1018	AICP'S P.R. 3-1 Disclosure of Asserted Claims and Infringement Contentions and P.R. 3-2 Document Production Against TSMC (cover document only)
1019	Kaanta et al., "Dual Damascene: A ULSI Wiring Technology," *VMIC Conference*, IEEE, June 11-12, 1991, pp. 144-152
1020	U.S. Patent No. 5,032,890 to Ushiku ("Ushiku")
1021	Reserved
1022	U.S. Patent No. 6,582,976 to Watanabe ("Watanabe'976")
1023	S. Middleman et al., *Process Engineering Analysis in Semiconductor Device Fabrication*, pp. 260-61 (excerpted), McGraw-Hill, 1993 ("Middleman")
1024	U.S. Patent No. 6,156,660 to Liu et al. ("Liu")
1025	U.S. Patent No. 5,798,298 to Yang ("Yang 2")
1026	T. I. Bao et al., "90 nm Generation Cu/CVD Low-k ($k < 2.5$) Interconnect Technology," *Digest. International Electron Devices Meeting*, San Francisco, CA, USA, 2002, pp. 583-586

Exhibit No.	Description
1027	A. Loke, "Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects," Dissertation, Stanford University (1999)
1028	K.N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *Applied Physics Review – Focused Review, Journal of Applied Physics*, Vol. 94, No. 9 (November 1, 2003), pp. 5451-5473
1029	T. C. Huang, *et al*., "Numerical Modeling and Characterization of the Stress Migration Behaviour Upon Various 90 nanometer Cu/Low k Interconnects," *Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)*, Burlingame, CA, USA, 2003 (added to IEEE Xplore 8-11-2003), pp. 207-209
1030	Reserved
1031	JP2000277609 to Narita ("Narita") and Certified Translation of Narita with Certification of Translation
1032	JP2000012688 to Nasu ("Nasu") and Certified Translation of Nasu with Certification of Translation
1033	U.S. Patent Publication No. 2001/0030365 to Otsuka et al. ("Otsuka")
1034	Wolf, Stanley, *Silicon Processing for the VLSI Era: Deep-Submicron Process Technology*, Lattice Press, 2002 (excerpted) ("Wolf")
1035	Reserved
1036	Reserved
1037	A. von Glasow et al., "Geometrical Aspects of Stress-Induced Voiding in Copper Interconnects," *Proceedings of the Advanced Metallization Conference 2002* (AMC 2002), San

Exhibit No.	Description
	Diego, CA, October 1-3, 2002, Tokyo, Japan, October 29-30, 2002, Materials Research Society, pp. 161-67
1038	U.S. Patent No. 6,215,189 to Toyoda et al. ("Toyoda")

LIST OF CHALLENGED CLAIMS

Claim Element	Claim Language
[1.pre]	A semiconductor device comprising:
[1.a]	a semiconductor substrate;
[1.b]	a first interconnect formed on the semiconductor substrate;
[1.c]	a first insulating film formed on the first interconnect;
[1.d]	a second interconnect formed on the first insulating film;
[1.e]	a via formed through the first insulating film and connecting between the first and second interconnects; and
[1.f]	a dummy via connected to the second interconnect,
[1.g]	wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough;
[1.h]	the second interconnect and the via form a dual damascene structure, and
[1.i]	the second interconnect and the dummy via from a dual damascene structure.
[2.a]	The semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,
[2.b]	wherein the first interconnect is formed on the second insulating film, and

[2.c]	the dummy via is connected to a first dummy interconnect formed on the second insulating film.
3	The semiconductor device of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect.
4	The semiconductor device of claim 2, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other.
7	The semiconductor device of claim 2, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film.
8	The semiconductor device of claim 2, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle.
[9.a]	The semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view, and
[9.b]	a diameter of the dummy via is smaller than a width of the first dummy interconnect.

11	The semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO_2 film.
12	The semiconductor device of claim 1, wherein the second interconnect includes a first barrier film and a first conductive film.
13	The semiconductor device of claim 12, wherein the first conductive film includes copper.
14	The semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode.
[15.a]	The semiconductor device of claim 1, wherein the first interconnect, the second interconnect and the via constitute part of a closed circuit, and
[15.b]	the dummy via does not constitute a closed circuit.
16	The semiconductor device of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect.

17	The semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view.
18	The semiconductor device of claim 17, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other.
21	The semiconductor device of claim 1, wherein the first interconnect and the second interconnect extend in a same direction.
22	The semiconductor device of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends.
25	The semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less.
26	The semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 1 μm or less.
28	The semiconductor device of claim 1, wherein the dummy via is provided in plural.

32	The semiconductor device of claim 1, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect and shorter than a distance between the via and the other end of the second interconnect.
39	The semiconductor device of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film.
40	The semiconductor device of claim 1, wherein the dummy via and the second interconnect include a Cu film.
42	The semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film.
[45.a]	The semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and
[45.b]	the via is connected to the second interconnect portion.

46	The semiconductor device of claim 45, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions.
47	The semiconductor device of claim 45, wherein a width of the second interconnect portion is 0.2 μm or less.

I. RELIEF REQUESTED

Applying the following grounds, Petitioner petitions for *Inter Partes* Review ("IPR") of U.S. Patent No. 7,439,623 ("the '623 patent") and cancellation of claims 1-4, 7-9, 11-18, 21-22, 25-26, 28, 32, 39-40, 42, and 45-47:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1	1-3, 7, 11-16, 21-22, 25-26, 28, 32, 39-40, 42	102	Watanabe
2	4, 8	103	Watanabe, Kurashima
3	9, 17-18	103	Watanabe, Iizuka
4	45-47	103	Watanabe, Kamoshima
5	1, 11-15, 17-18, 21-22, 25-26, 28, 32, 39-40	102	Hasunuma
6	2, 8	103	Hasunuma, Kurashima
7	1, 16, 45-46	103	Aoyagi
8	47	103	Aoyagi, Hasunuma
9	1, 2, 4, 7, 14, 42	102/103	Kunikiyo
10	9, 17	103	Kunikiyo, Iizuka
11	3	103	Kunikiyo, Watanabe

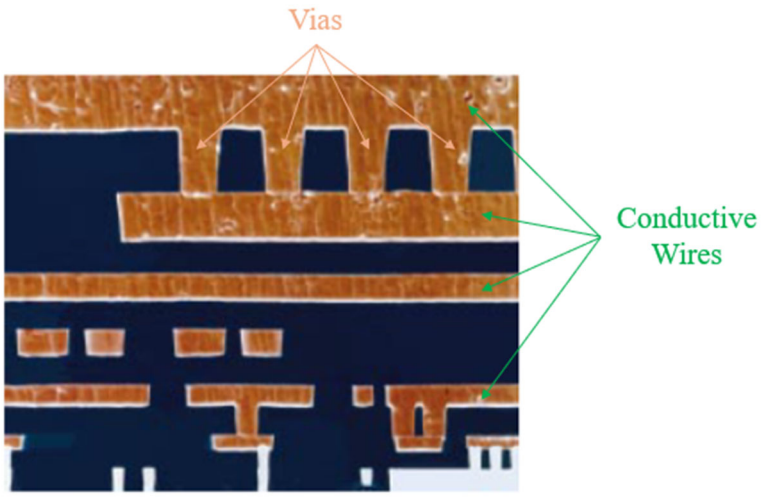
This petition is supported by the declaration of Dr. Reinhold Dauskardt, an expert in the field of interconnect technology. TSMC-1003, ¶¶1-39.

II. STATE OF THE ART

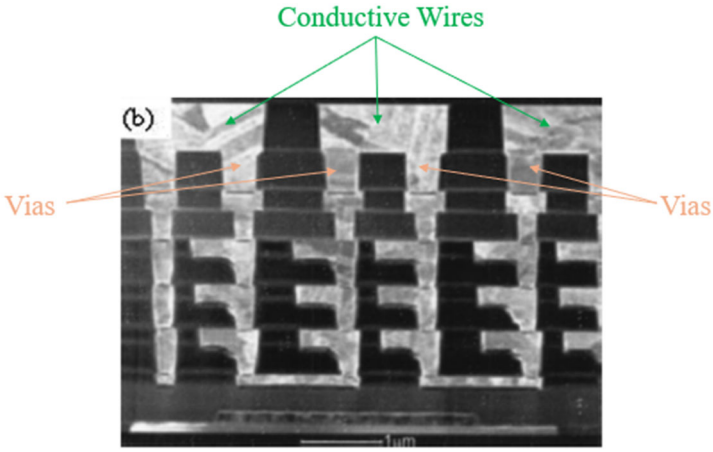
The '623 patent describes using dummy structures to reduce stress-induced void formation in interconnect structures. Such dummy structures, for the same purposes, were already well-known. TSMC-1003, ¶¶40-46.

A. Interconnects and Dual Damascene

Semiconductor chips have multiple levels of conductive wires ("interconnects") for controlling chip operation, with vias connecting wires between different levels when needed; such interconnect structures are commonly made of aluminum or copper. TSMC-1015, 1:13-24; *see also* TSMC-1012, 32; TSMC-1017, 2:53-58. Exemplary interconnect structures are shown below:



TSMC-1012, 32



TSMC-1028, 5452

Dual damascene is a manufacturing process where patterns of trenches and underlying via holes are filled with conductive metal(s) to simultaneously form the interconnects on a given level and the vias below that level. TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract; TSMC-1034, 671-76. This process is illustrated below:

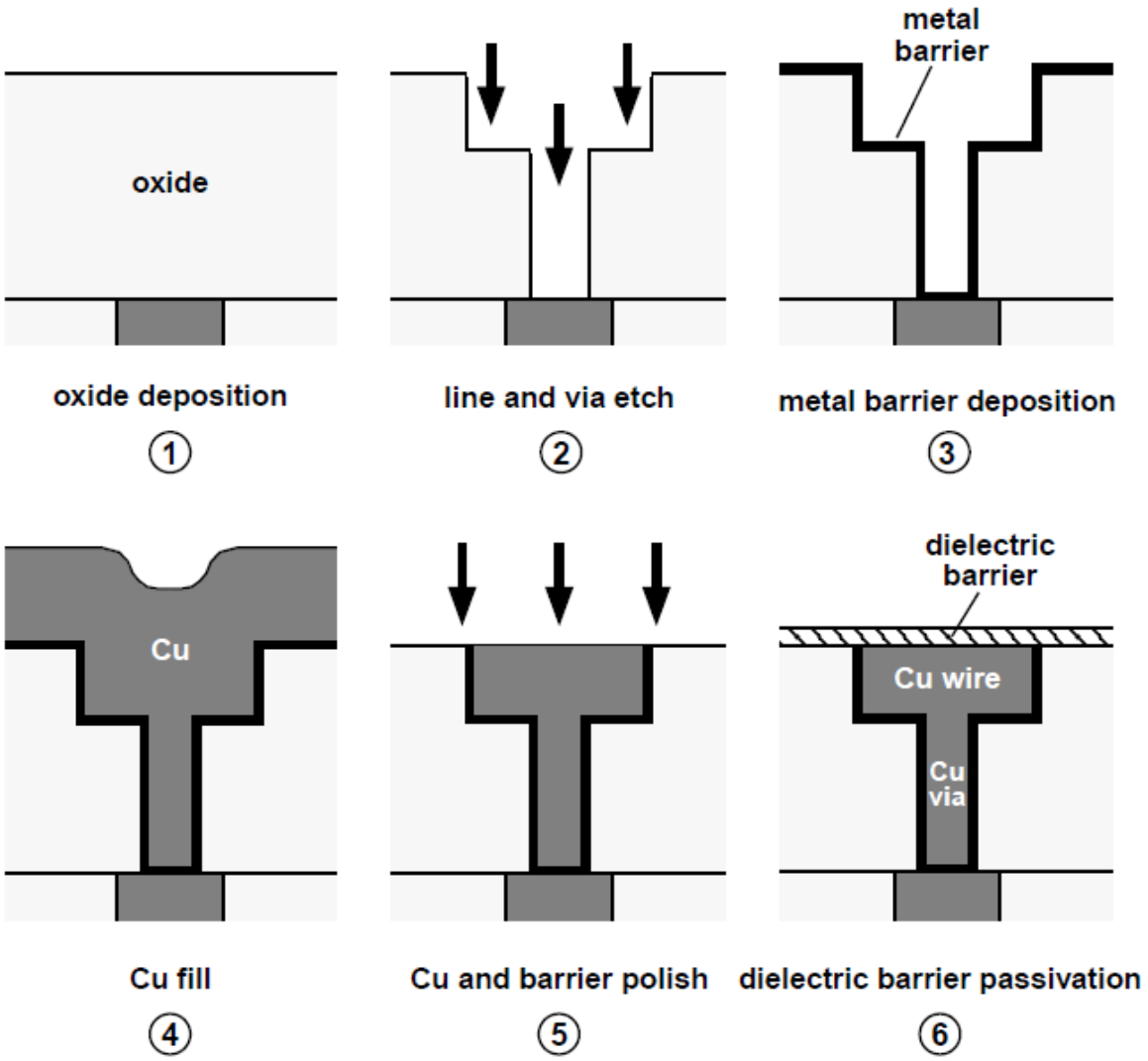


Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects.

TSMC-1027, 25. Steps ④→⑤ are typically performed using chemical mechanical polishing ("CMP"). TSMC-1034, 322-34, 675.

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength

Stress migration and electromigration involve the movement of metal atoms and vacancies within the interconnect structure; because vacancies tend to

aggregate in/under vias, voids can form and cause electrical disconnects. TSMC-1029, 207; TSMC-1028, 5455-56, 5458-59; TSMC-1015, 1:32-37, 2:61-63. In addition, insulating films, especially low-k materials, can have poorer mechanical strength and adhesion, making them susceptible to damage during CMP. TSMC-1016, 1:53-2:7; TSMC-1026, 583.

Dummy structures were used long before the '623 patent for addressing these problems. For example, dummy vias have been added near active vias to arrest stress-induced vacancy migration and void formation. TSMC-1029, Abstract, 208; TSMC-1015, 2:64-3:14. Dummy structures were also known to alleviate electromigration concerns, acting as reservoirs for metallic ions. *See* TSMC-1015, 1:66-2:11; TSMC-1032, ¶¶[0012]-[0016]. Migrating vacancies/microvoids get distributed between vias and dummy vias, reducing their concentration in/under active vias. TSMC-1029, 208; TSMC-1009, ¶[0088]. Dummy vias also improve mechanical strength, preventing damage during CMP. TSMC-1016, 4:42-47; TSMC-1026, 584-85.

Similar to dummy vias, dummy wirings/interconnects also improve mechanical properties, helping adhesion across multiple insulating layers and improving the CMP process by reducing dishing. TSMC-1020, Abstract; TSMC-1024, 2:55-58; TSMC-1025, Abstract; TSMC-1026, 584-85. Connecting dummy wirings to dummy vias was well-known to increase the mechanical strength of the

combined insulating layer and upper-level wiring, as well as enhance the durability of multi-layered insulating films. TSMC-1011, 8:35-54.

III. THE '623 PATENT

A. Overview

The '623 patent relates to a semiconductor device having multilevel interconnection structures. TSMC-1001, 7:47-50. A first interconnect 102A (and optionally a dummy interconnect 102B) is formed in insulating film 101. *Id.*, 10:56-63, Figs. 1A, 2B. After forming intermediate insulating layers 103-105, the dual damascene process is used to form second interconnect 111 on/in the insulation layer stack, which is connected to first interconnect 102A by via 110A:

FIG. 1B

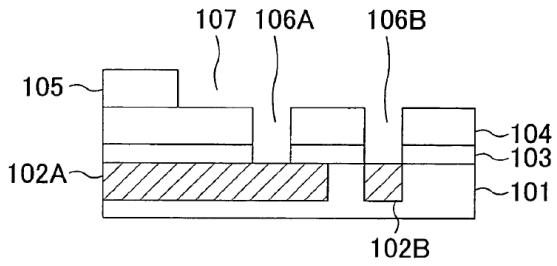
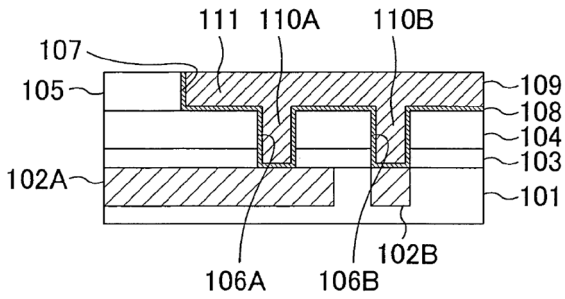


FIG. 2A



Id., 11:5-21; 6:38-40, Figs. 1B-1C, 2A-2B. Dummy via 110B, formed in dummy hole 106B simultaneously with via 110A and interconnect 111, connects dummy interconnect 102B with second interconnect 111. *Id.*, 11:15-21; Figs. 2A-2B.

First interconnect 102A, via 110A and second interconnect 111 constitute part of a closed-circuit during device operation, while neither dummy

interconnect 102B nor dummy via 110B does. *Id.*, 10:24-28. That is, the device remains operable even if dummy interconnect 102B and dummy via 110B are omitted from the structure. *Id.*, 10:28-32.

According to the '623 patent, vacancies in copper film 109 of second interconnect 111 are divided and respectively flow into via 110A and dummy via 110B, thereby reducing vacancies flowing into via 110A and reducing the associated stress gradient. *Id.*, 11:36-42. The '623 patent says this suppresses occurrences of voids in via hole 106A. *Id*., 11:38-45.

B. Prosecution History

The '623 application was filed on December 2, 2004, claiming priority to a Japanese application filed December 3, 2003. Following the addition of claims 27-86 in a restriction response, the USPTO issued multiple Office Actions rejecting the claims over U.S. Patent No. 6,919,637 to He. TSMC-1002, 237-47, 285-97. The Examiner also rejected dependent claims reciting relative interconnect widths, via diameters, and their spacing, stating that "one of ordinary skill in the art would have been led to the recited shapes, sizes and dimensions through routine experimentation and optimization." *Id.*, 244-45, 295-96. Applicant responded first by requiring that the dummy via be conductive, then adding "dual damascene" limitations, but later deleted these limitations and instead required that the dummy via be incapable of current flow. *Id.*, 266, 301, 331. The NOA re-added the dual-

damascene limitations, while stating that the prior art did not teach the "dummy via made of a conductive film and being arranged as in the context of claim 27." *Id.*, 354-55.

C. Claim Construction

The Board construes claims under the standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For purposes of this proceeding, Petitioner does not believe that any claim terms need construction to resolve the unpatentability issues presented in this Petition. TSMC-1003, ¶57.

IV. ORDINARY SKILL

A person of ordinary skill in the art ("POSITA") had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. TSMC-1003, ¶37. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. *Id.*

V. PRIOR ART[1]

Reference	Filed	Published	Pre-AIA Prior Art Qualification
Watanabe	12/4/2002 (USPTO)	6/26/2003	§§102(a),(b),(e)
Hasunuma	9/3/2003 (USPTO)	6/17/2004	§102(e)
Aoyagi	3/20/2001 (USPTO)	9/6/2001	§§102(a),(b),(e)
Kunikiyo	7/7/2000 (USPTO)	4/6/2004	§102(e)
Kurashima	8/14/2003 (USPTO)	5/9/2006	§102(e)
Iizuka	1/24/1992 (USPTO)	10/5/1993	§§102(a),(b),(e)
Kamoshima	9/9/2003 (USPTO)	9/9/2004	§102(e)

VI. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: Watanabe Anticipates Claims 1-3, 7, 11-16, 21-22, 25-26, 28, 32, 39-40, and 42

Watanabe anticipates claims 1-3, 7, 11-16, 21-22, 25-26, 28, 32, 39-40, and 42. TSMC-1003, ¶¶103-241.

[1] All references are prior art regardless of any priority claim to the Japanese application filed December 3, 2003. Petitioner does not acquiesce that any claims are so entitled.

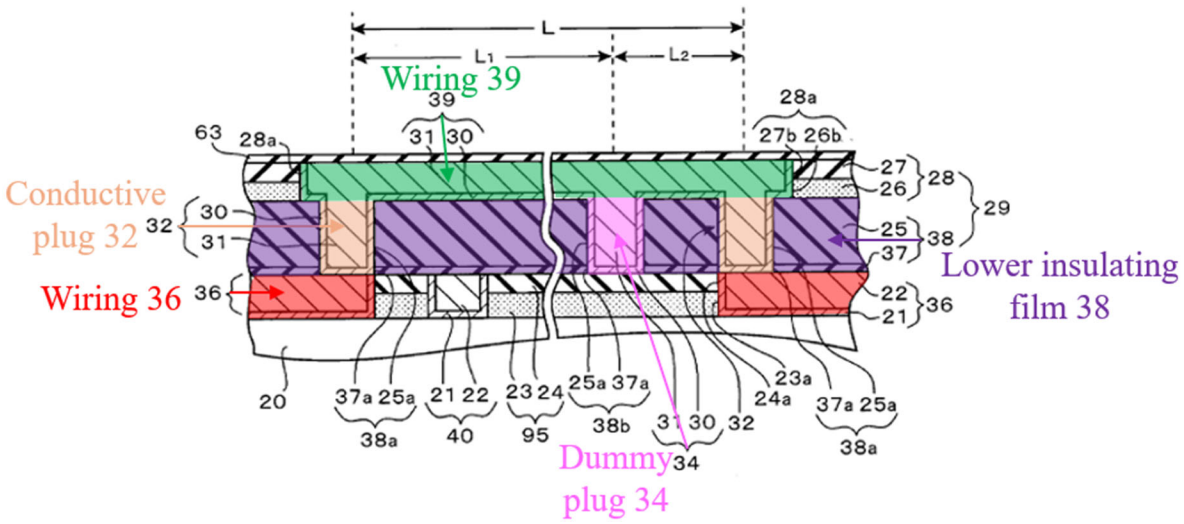
1. Watanabe

Because Watanabe is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Watanabe is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1004, ¶¶[0005], [0016]-[0018]; TSMC-1003, ¶¶59-77. Indeed, Watanabe recognized the same problem and proposed the same solution before the '623 patent. TSMC-1003, ¶59.

Watanabe discloses semiconductor devices having multilevel dual-damascene interconnect structures that address reliability problems caused by stress-induced void migration and electromigration. TSMC-1004, ¶¶[0012]-[0019], [0022]-[0024], [0077]. Watanabe incorporates non-functional dummy vias and dummy interconnects formed concurrently with the functional structures. *Id*., Abstract, ¶¶[0026]-[0028]; TSMC-1003, ¶59.

Watanabe's first embodiment (Figures 1-2) discloses wiring 36, overlying insulating film 29, and wiring 39 formed along with conductive plug 32 and dummy conductive plug 34 using dual damascene:

FIG. 1

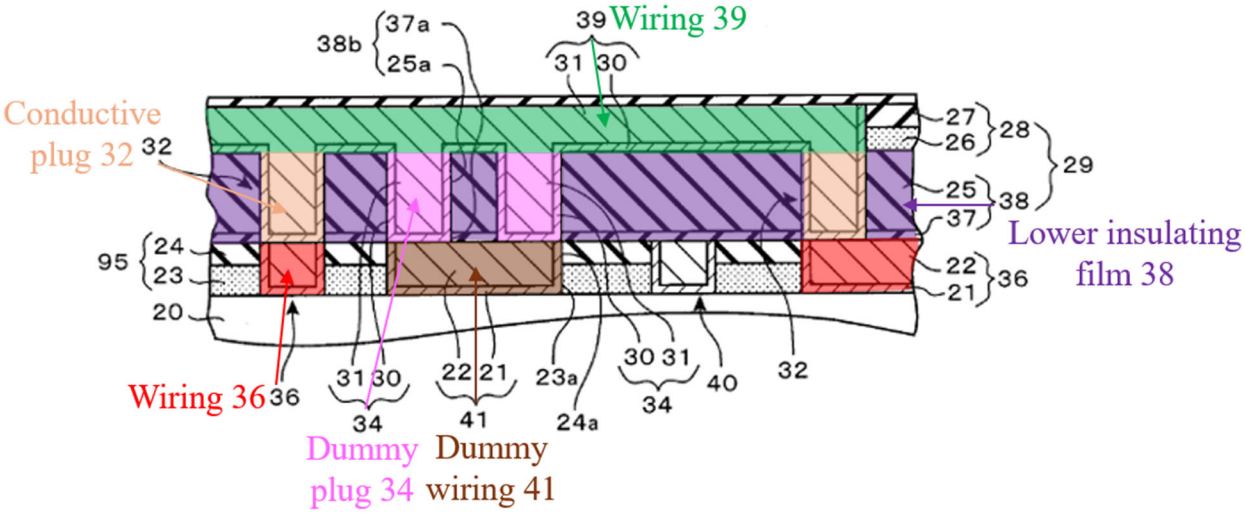


Id., ¶¶[0065]-[0074], Fig. 1; TSMC-1003, ¶65.

Conductive plug 32 connects wiring 36 and wiring 39. Dummy plug 34 connects to wiring 39 but its other end extends to a "non-forming region" of insulating film 95. TSMC-1004, ¶¶[0067], [0079]; TSMC-1003, ¶66. Watanabe teaches that dummy plug 34 reduces stress migration problems, provides a source of copper atoms to mitigate electromigration, and enhances support for insulating film 29/wiring 39. *Id.*, ¶¶[0026], [0070]-[0079], [0091]; TSMC-1003, ¶66.

Watanabe's second embodiment (Figures 3-4) adds dummy wiring 41:

FIG. 3



Id., ¶¶[0028], [0090]; TSMC-1003, ¶67. Dummy wiring 41 resides in the same insulating film 95 as wiring 36, and adds mechanical strength and uniformity during CMP. *Id.*, ¶¶[0028]-[0029], [0090]-[0091]; TSMC-1003, ¶68.

Watanabe discloses multiple embodiments, including:

- a "first embodiment" in Figures 1-2 (*see* TSMC-1004, ¶¶[0059]-[0087]);
- a "second embodiment" in Figures 3-4 (*see id.*, ¶¶[0088]-[0092]);
- a "third embodiment" in Figures 5A-5C (*see id.*, ¶¶[0093]-[0108]);
- a "fifth embodiment" in Figures 8-11 (*see id.*, ¶¶[0115]-[0133]); and
- a more generic embodiment in Figure 14 (*see id.*, ¶¶[0171]-[0181]).

See, e.g., *id.*, ¶¶[0038]-[0049], [0051]; TSMC-1003, ¶60.

Watanabe's Figs. 12A-12N show a method of manufacturing for the foregoing embodiments. TSMC-1004, ¶[0049] ("…method of manufacturing the

semiconductor device **according to the embodiments of the present invention**")[2]; *see also id*., ¶¶[0072], [0134]-[0170]; TSMC-1003, ¶64. The first-fifth embodiments (Figures 1-9) and Figures 12A-12N use common reference numerals. TSMC-1004, ¶¶[0089], [0116], [0135]; TSMC-1003, ¶74. Watanabe also discloses that the method can be repeated to obtain any number of wirings. TSMC-1004, ¶¶[0171]-[0173]; TSMC-1003, ¶75.

2. Claim 1[3]

Watanabe's first embodiment is applied to claim 1 below, and subsequent sections apply Watanabe's other embodiments.

a) First Embodiment

(1) [1.pre]

Watanabe discloses "a semiconductor device" as shown in Figures 1, 12A-12N, and 14. TSMC-1004, Title, Abstract, ¶¶[0003], [0038], [0051], [0135]-[0136], [0170]-[0173]; TSMC-1003, ¶¶106-07.

(2) [1.a]

Watanabe discloses underlying layer 20 that includes a "silicon wafer (semiconductor substrate)":

[2] All emphases have been added unless otherwise noted.

[3] *See* List of Challenged Claims for all claim language.

FIG. 1

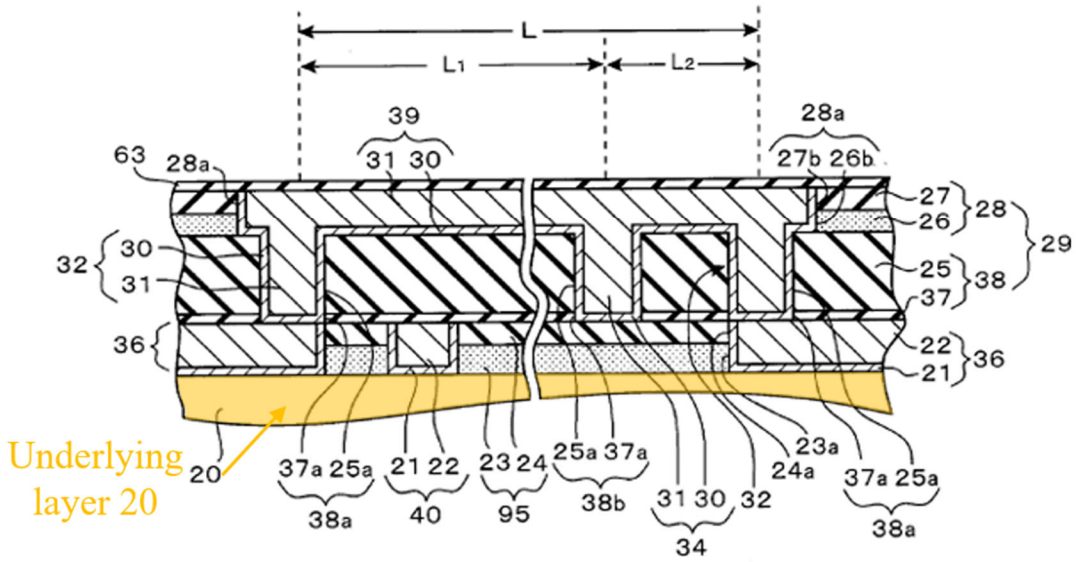
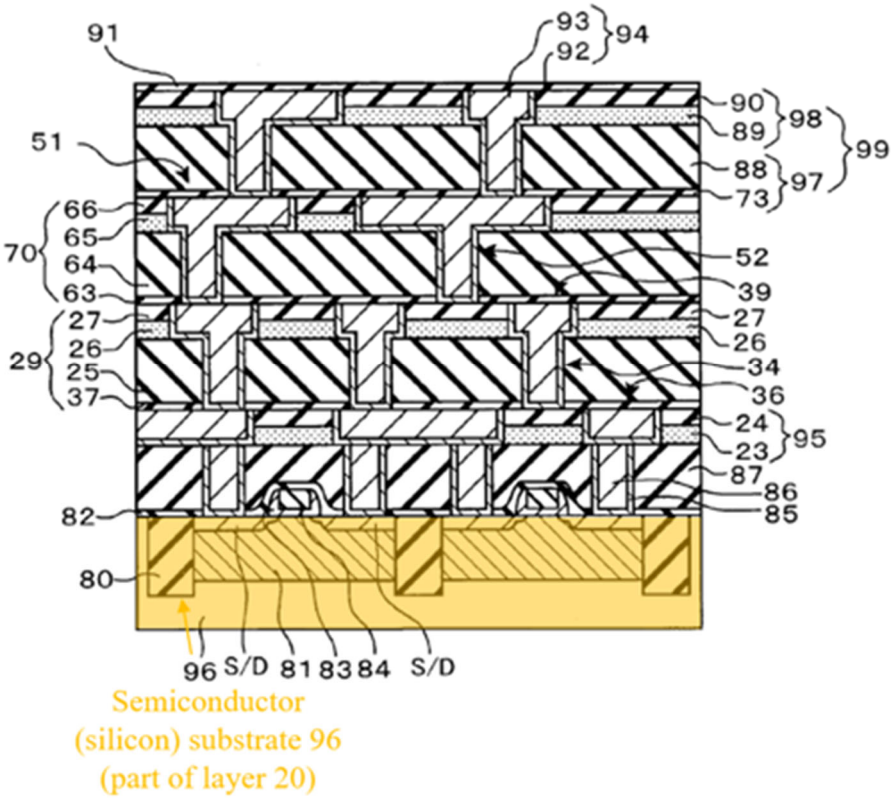

L
L1
L2
39
31 30
28a
27b 26b
63
28a
27
26
28
29
30
32
31
25
37
38
36
22
21
36
Underlying layer 20
20
37a 25a
38a
21 22
40
23 24
95
25a 37a
38b
31 30 32
34
23a
24a
37a 25a
38a

FIG. 14

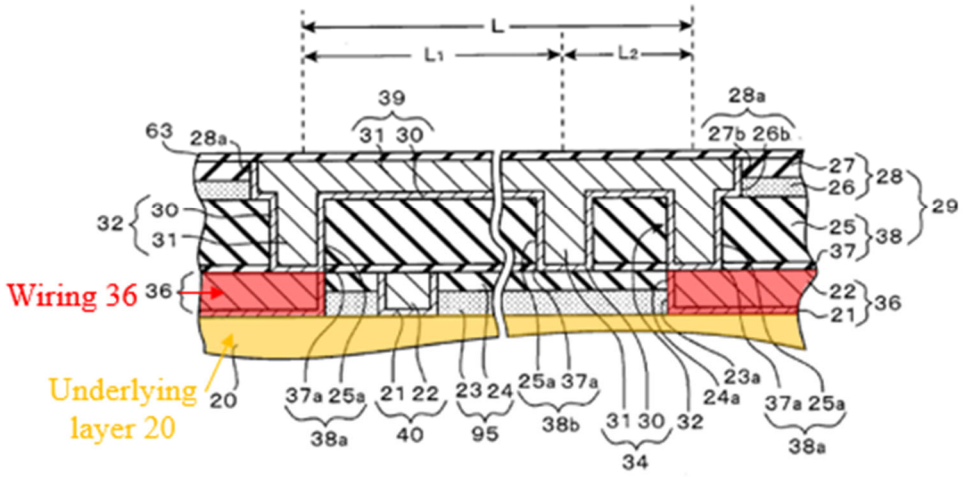

91
93
92
94
90
89
98
99
88
97
73
51
66
65
64
63
70
52
39
27
26
29
25
37
34
36
24
23
95
87
86
85
82
80
96
S/D
81
83
84
S/D
Semiconductor (silicon) substrate 96 (part of layer 20)

TSMC-1004, ¶¶[0061]; *see also id*., ¶¶[0051], [0135]-[0136], [0172]-[0173], Figs. 1, 12A, 14; TSMC-1003, ¶¶108-09.

(3) [1.b]

Watanabe discloses a first interconnect (e.g., "wiring 36") formed on underlying layer 20 (having a semiconductor substrate):

FIG. 1

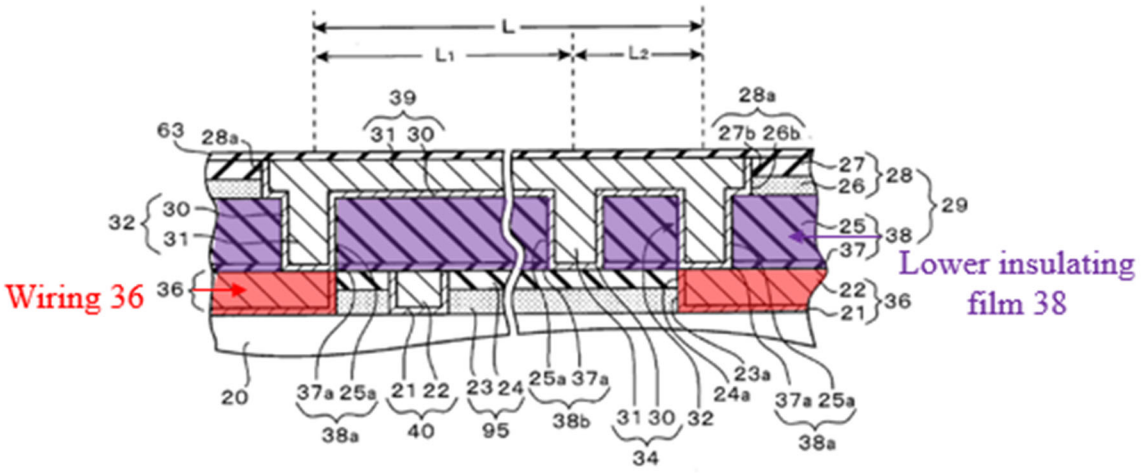


TSMC-1004, ¶¶[0051], [0061], [0064]-[0065], [0136]-[0144], [0174], Figs. 1, 12A-12D, 14; TSMC-1003, ¶¶110-11.

(4) [1.c]

Watanabe discloses a first insulating film (e.g., "lower insulating film 38") formed on the first interconnect:

FIG. 1

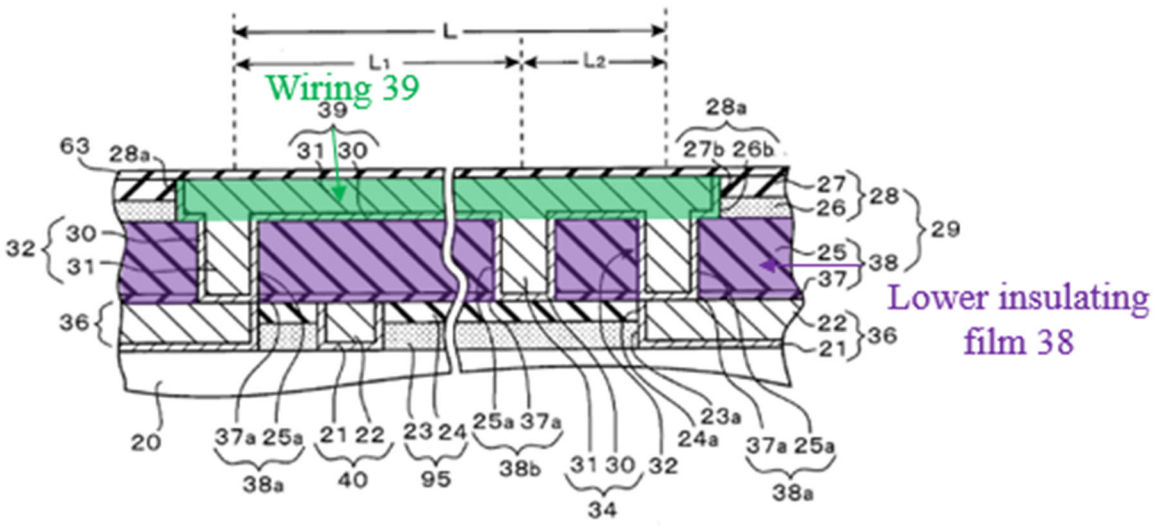


TSMC-1004, ¶¶[0066], [0149]-[0150], [0175], Figs. 1, 3, 12E, 12M, 14; TSMC-1003, ¶¶112-13. Additionally, for purposes of applying Watanabe to the challenged claims, the "first insulating film" could also be read on Watanabe's entire insulating film stack 29, which includes upper and lower insulating films 28 and 38. TSMC-1004, ¶¶[0149]-[0152]; TSMC-1003, ¶114.

(5) [1.d]

Watanabe discloses a second interconnect (e.g., "wiring 39") formed on first insulating film ("lower insulating film 38"):

FIG. 1

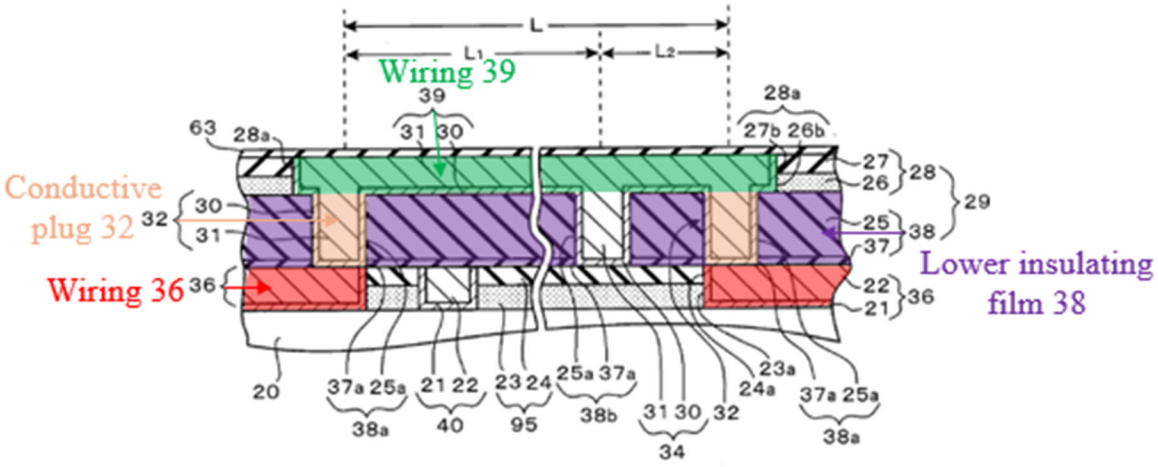


TSMC-1004, ¶¶[0067], [0069], [0153]-[0168], [0175], Figs. 1, 12E-12M, 14; TSMC-1003, ¶115-16.

(6) [1.e]

Watanabe discloses a via (e.g., "conductive plug 32") formed in via hole 38a through the lower first insulating film, and connecting first and second interconnects (wirings 36, 39):

FIG. 1

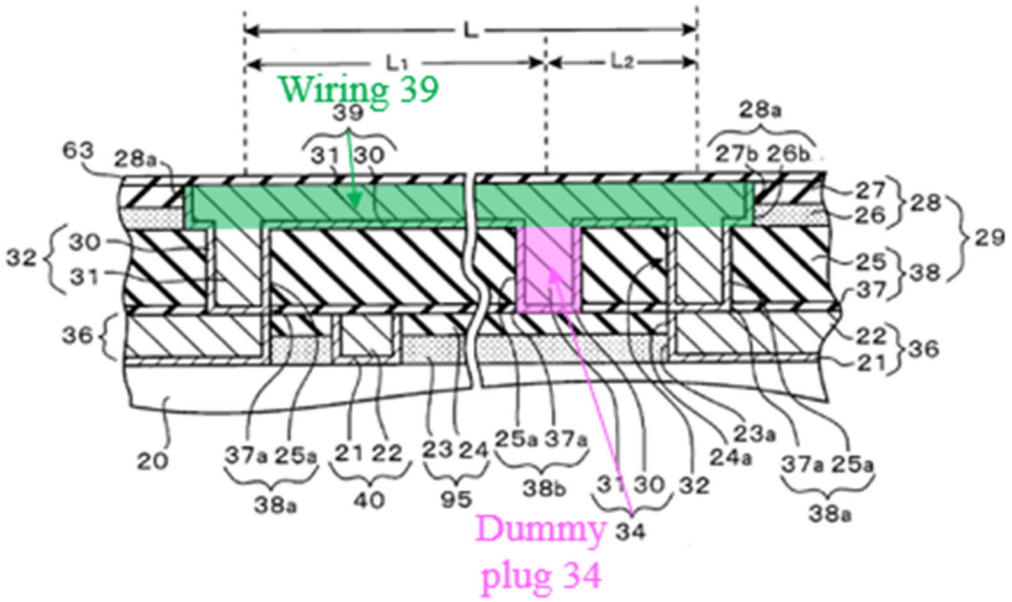


TSMC-1004, ¶¶[0067]-[0070], [0155]-[0168], [0173], Figs. 1, 12G-12M, 14; TSMC-1003, ¶¶117-18.

(7) [1.f]

Watanabe discloses a dummy via (e.g., "dummy plug 34") connected to the second interconnect (e.g., "wiring 39"):

FIG. 1



TSMC-1004, ¶¶[0067]-[0072], [0079], [0164]-[0168], Figs. 1, 12G-12M, 14; TSMC-1003, ¶¶119-20.

(8) [1.g]

Watanabe's dummy via ("dummy plug 34") comprises a conductive film and is arranged to be incapable of having current flow therethrough. TSMC-1003, ¶¶121-27. Watanabe's dummy plug 34 includes conductive barrier metal layer 30 and conductive copper film 31. TSMC-1004, ¶¶[0067]-[0072], [0164]-[0168], [0185], Figs. 1, 12K-12M, 14; TSMC-1003, ¶¶121-27.

The '623 specification states that dummy vias and dummy interconnects "do not constitute a closed circuit in actual use of a device with an interconnection structure including these via and interconnect (i.e., no current flows therein during

actual use of the device)," and the circuit is operable even if the dummy vias and dummy interconnects are omitted. TSMC-1001, 3:14-18; 10:26-32.

Watanabe's dummy plug 34 extends to a "non-forming region" of insulating film 95. TSMC-1004, ¶¶[0061], [0067], [0079], [0165], Figs. 1, 12K-12M, 14; TSMC-1003, ¶123. Watanabe's dummy plugs 34 do not constitute part of a closed circuit in actual use of the device as no current flows therethrough during actual device use. TSMC-1003, ¶126. A POSITA would recognize that no current flows through dummy plugs 34 due to this lack of connection to a second active circuit element. *Id*.

Instead, current flows between wirings 36 and 39 through conductive plugs 32, forming a closed circuit for operation of the device. *See* TSMC-1004, ¶[0073], Figs. 1, 14; TSMC-1003, ¶127. Watanabe's device remains operable without dummy plugs 34, because current would still flow between wirings 36 and 39 through plugs 32 during device use. TSMC-1003, ¶127.

(9) [1.h]/[1.i]

Watanabe discloses forming the second interconnect ("wiring 39"), via ("plug 32"), and dummy via ("dummy plug 34") using a "dual damascene process," thus forming dual-damascene structures. TSMC-1004, ¶¶[0067]-[0072], [0135], [0153]-[0168], Figs. 1, 12E-12M, 14; TSMC-1003, ¶¶76, 128-34, 149.

Watanabe fills wiring trench 28a, via hole 38a, and dummy via hole 38b with barrier metal layer 30 and copper film 31, simultaneously forming wiring 39, plug 32, and dummy plug 34:

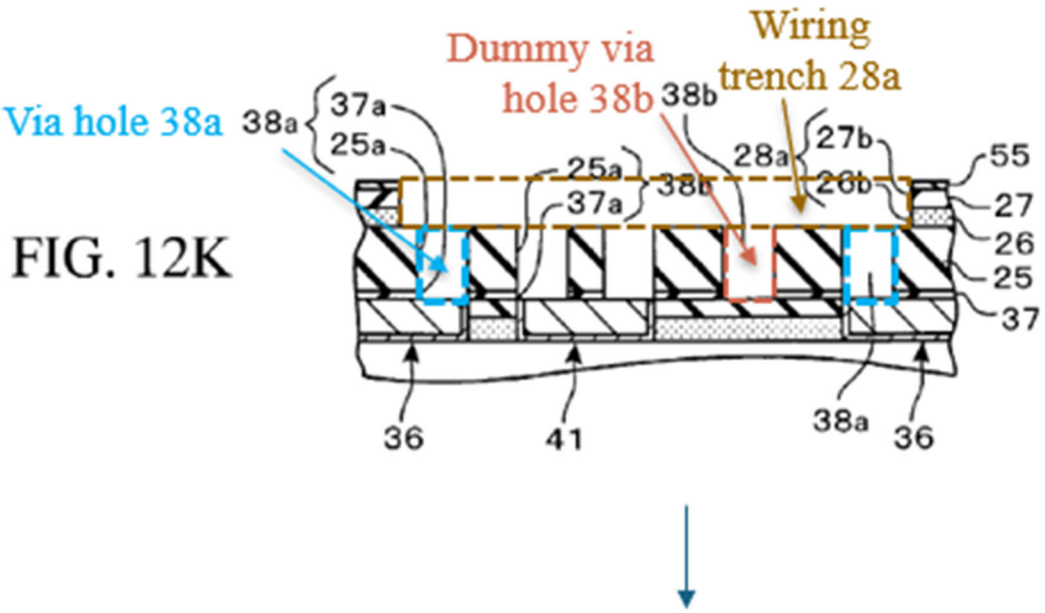


FIG. 12K

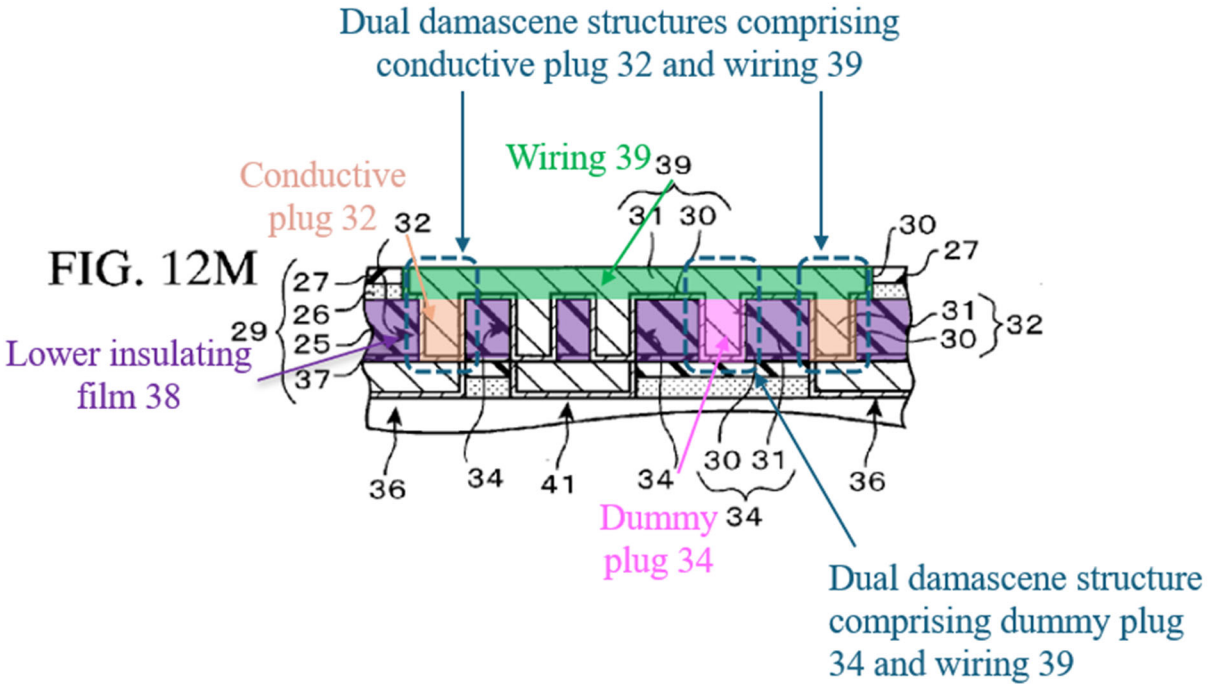
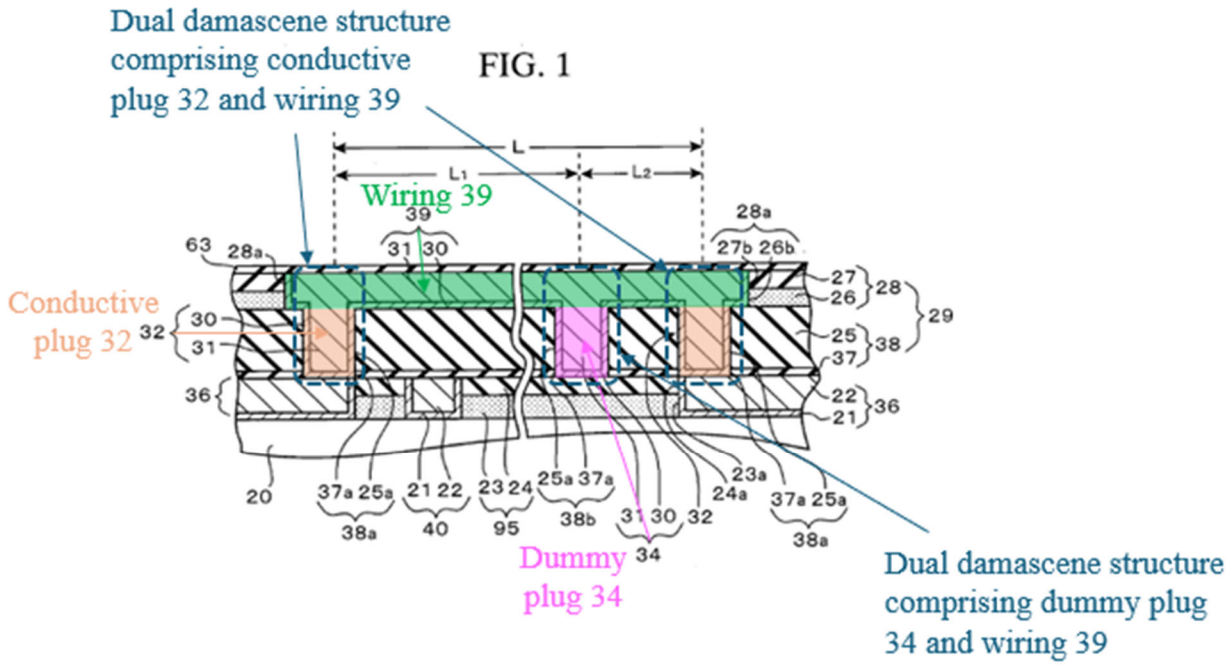


FIG. 12M

TSMC-1004, ¶¶[0067]-[0068], [0072], [0166]-[0168], Figs. 12E-12M; TSMC-1003, ¶129. Figure 1 discloses the completed device, with wiring 39 and plug 32, as well as wiring 39 and dummy plug 34 forming dual damascene structures:



TSMC-1003, ¶¶76, 133-34. The same applies to the structures of Figure 14. *Id.*, ¶134.

b) Second Embodiment

Watanabe's second embodiment (Figures 3-4) also discloses claim 1, including the same components as the first embodiment. *See supra*, §§VI.A.2.(a) (discussing underlying layer 20, wiring 36, lower insulating film 38, wiring 39, plug 32, and dummy plug 34). TSMC-1004, ¶¶[0088]-[0092], Figs. 3-4; TSMC-1003, ¶¶135-36, 141.

Further, dummy plugs 34 are connected to a dummy interconnect ("dummy wiring 41"):

FIG. 3

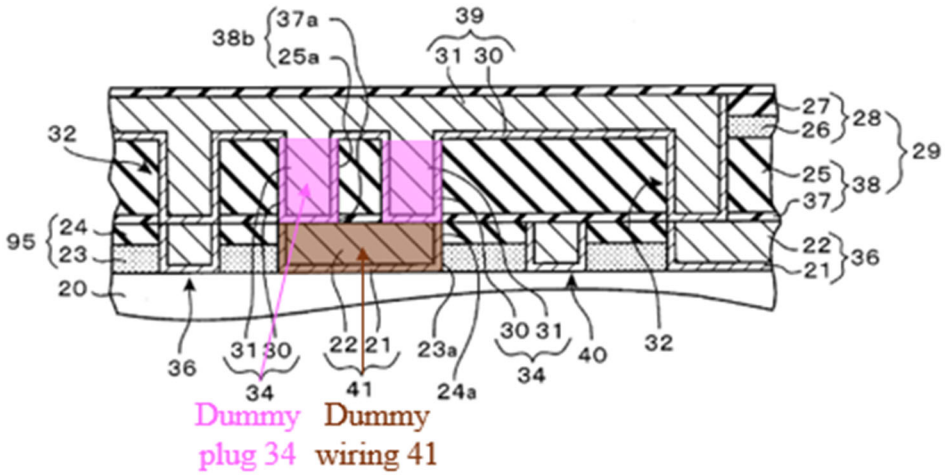
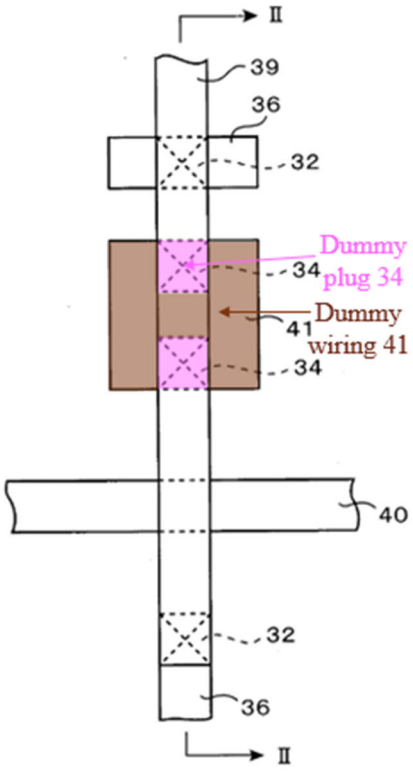


FIG. 4

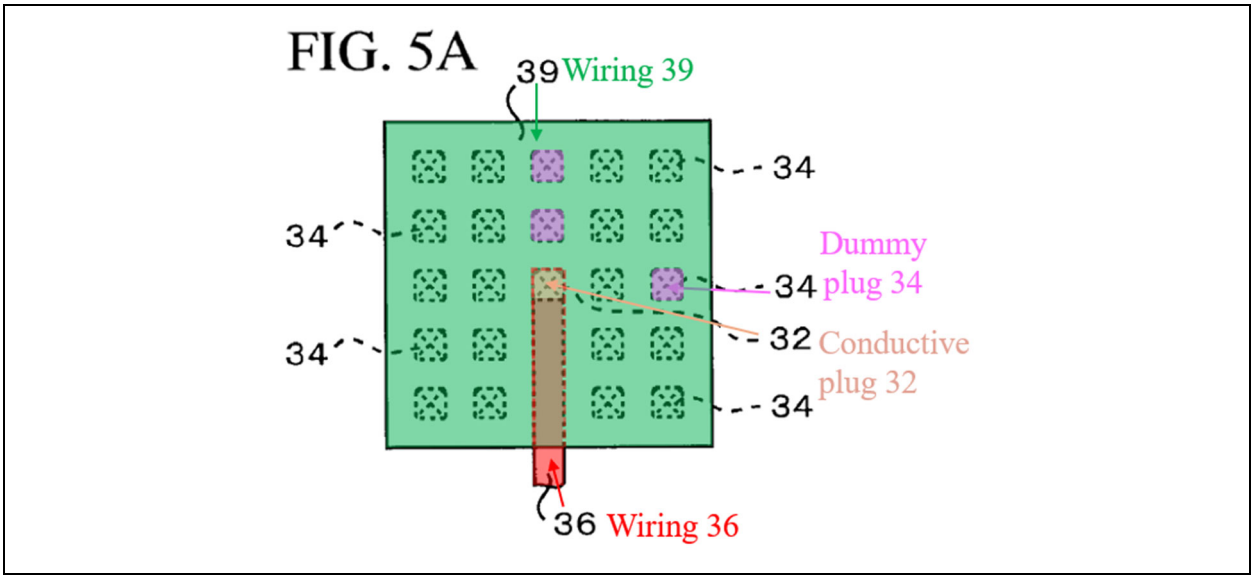


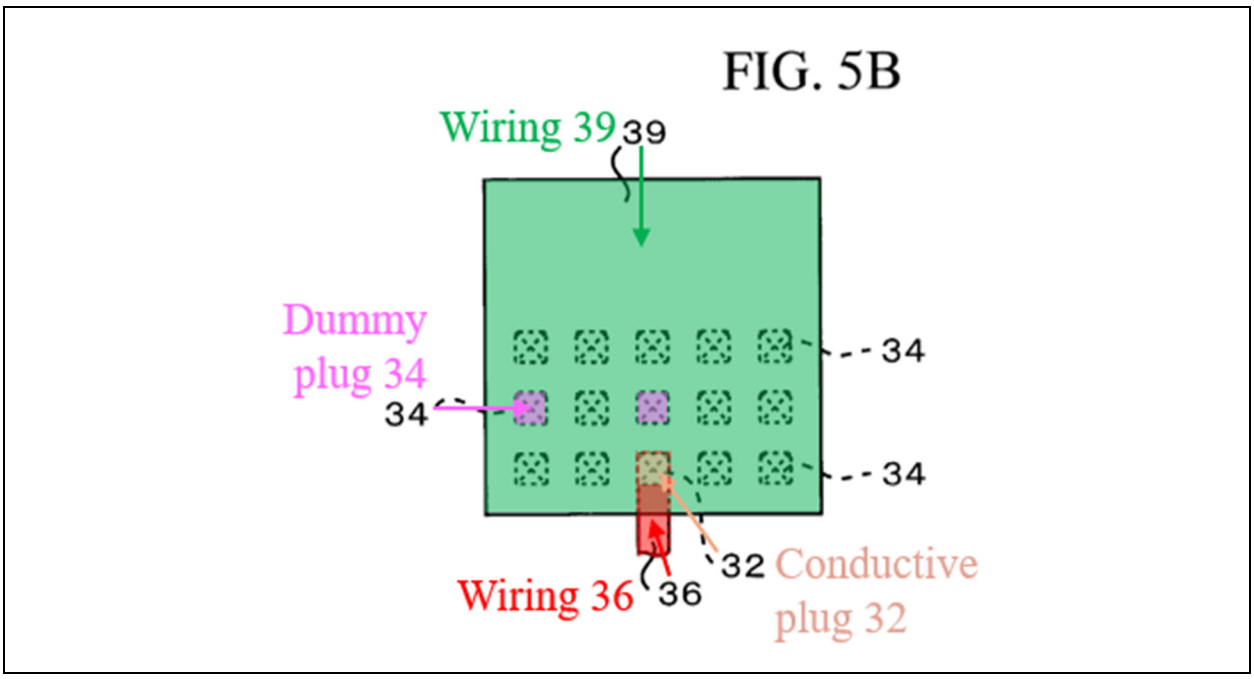
TSMC-1004, ¶¶[0090]-[0092], [0165], [0186], Figs. 12E, 12K-12M; TSMC-1003, ¶¶137-38.

Like Watanabe's first embodiment, "dummy plugs 34" in Watanabe's second embodiment are "incapable of having current flow therethrough" because dummy wiring 41 does not connect to any other active circuit element or form part of a closed circuit during actual use. TSMC-1004, ¶¶[0089], [0135], [0166]-[0168], [0186]; TSMC-1003, ¶139. And, even with omitting dummy plugs 34 and dummy wiring 41, the device would still be operable because wirings 36, 39 and plugs 32 form a closed circuit for operation of the device. TSMC-1003, ¶¶139-40.

c) Third Embodiment

Watanabe's third embodiment discloses claim 1, matching the first and second embodiments in relevant respects, while providing an alternative shape/configuration for wiring 39 and dummy plugs 34 in various locations:

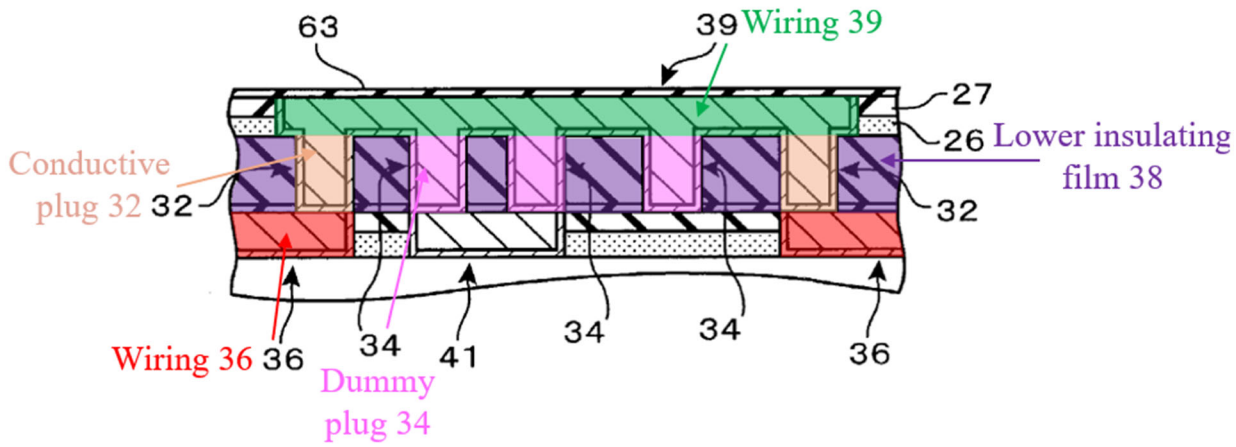




TSMC-1004, ¶¶[0093]-[0099], Figs. 5A-5C; TSMC-1003, ¶142.

Also given Watanabe's express statement that Figure 12 represents "sectional views showing a method of manufacturing the semiconductor device according to the embodiments of the present invention," a POSITA understood that the cross-section of Figure 12N discloses the basic structure of Watanabe's third embodiment (e.g., Figures 5A-5C):

FIG. 12N

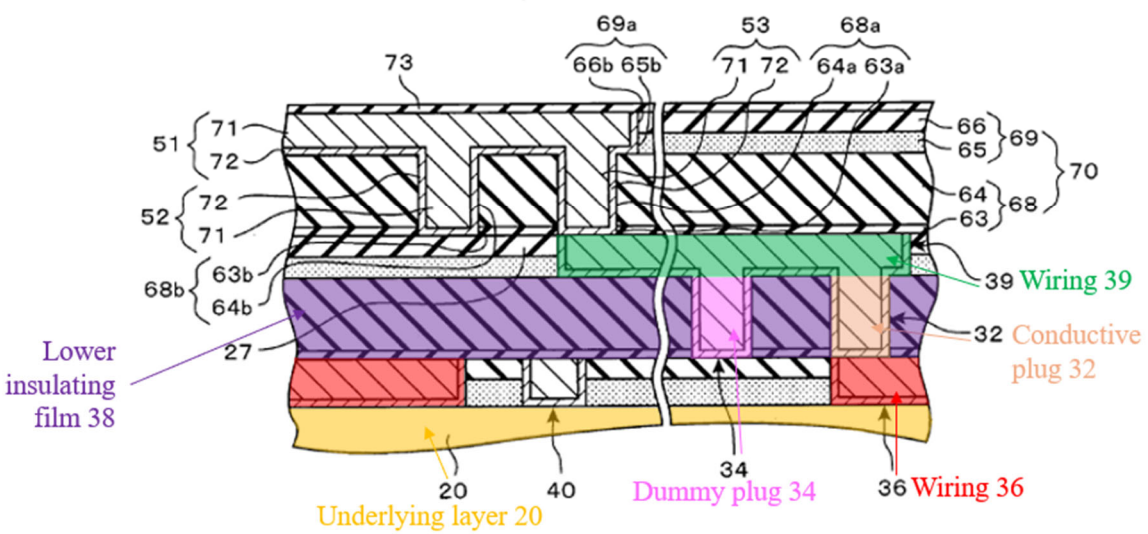


TSMC-1004, ¶¶[0049], [0135], Fig. 12; TSMC-1003, ¶142. Thus, Watanabe's third embodiment similarly discloses claim 1 for the same reasons as Watanabe's first embodiment. *Supra*, §VI.A.2.(a); TSMC-1003, ¶¶142-43.

d) Fifth Embodiment

Watanabe's fifth embodiment (Figures 8-9) discloses a three-level interconnect structure that discloses claim 1 in multiple ways. TSMC-1004, ¶¶[0115]-[0133]; TSMC-1003, ¶¶144-50. First, Watanabe's fifth embodiment includes the same structure and meets claim 1 in the same way as the first embodiment, shown in Figure 8 below (a first mapping):

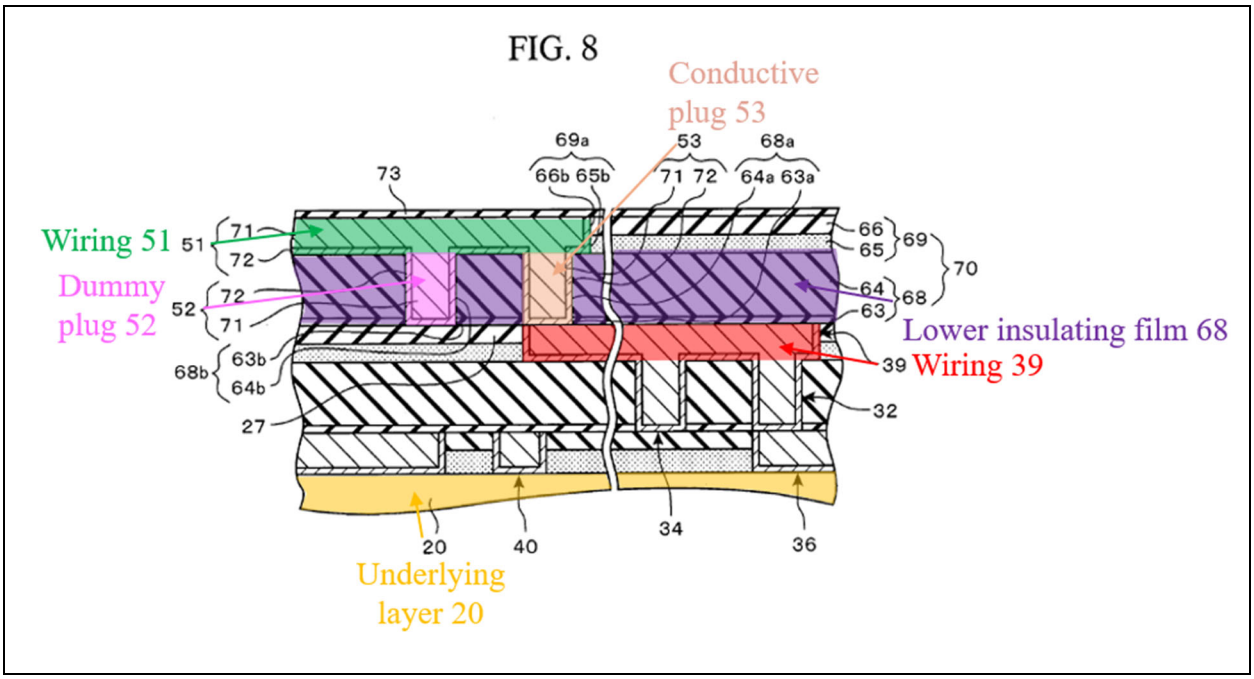
FIG. 8



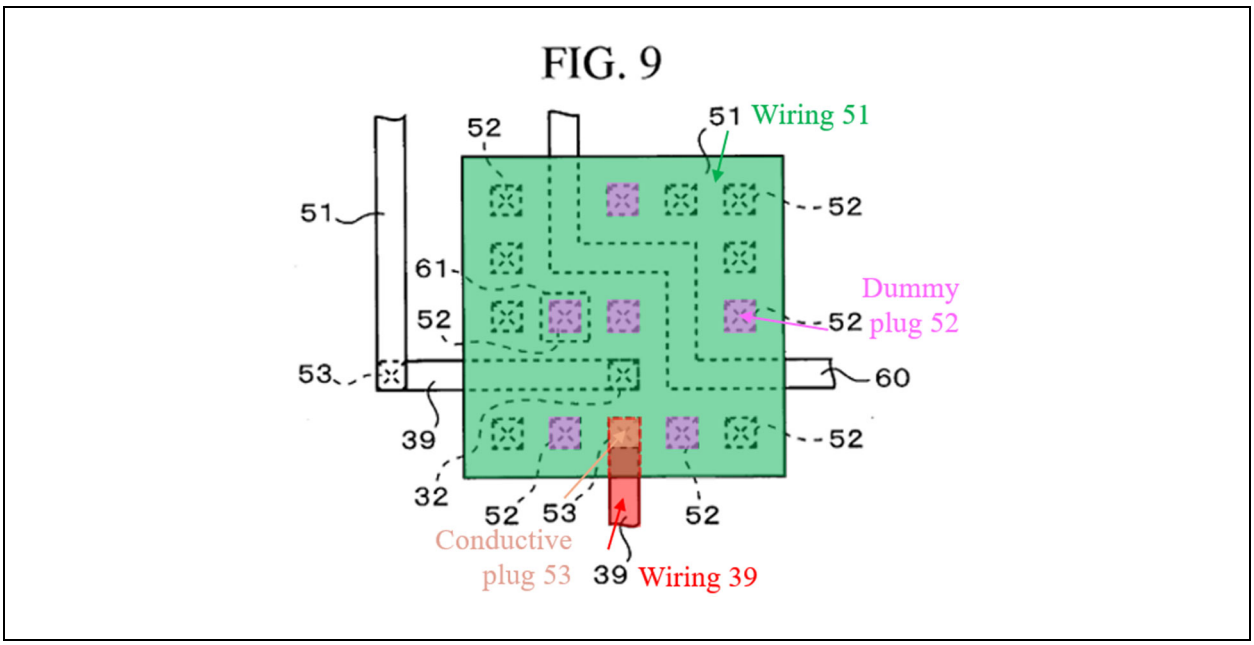
Supra, §VI.A.2.(a); TSMC-1003, ¶145.

As another mapping, Watanabe's fifth embodiment discloses claim 1 based on wirings 39, 51; thus, wiring 39 is the "first interconnect," insulating film 68 is the "first insulating film," and wiring 51 is the "second interconnect." TSMC-1004, ¶¶[0117]-[0122], Fig. 8; *see also id.*, ¶¶[0172]-[0178], Fig. 14; TSMC-1003, ¶¶146-47. Watanabe's conductive plug 53 is a "via," formed within via hole 68a through insulating film 68 and connecting wirings 39, 51. TSMC-1004, ¶¶[0120]-[0122], Figs. 8-9. And Watanabe's dummy plug 52 is a "dummy via," connected

to wiring 51. *Id.*, ¶[0122], Figs. 8-9. Figures 8-9 below show this second mapping[4]:



[4] When Watanabe's first embodiment of Figures 1-2 is applied against a claim, the first mapping of Watanabe's fifth embodiment of Figures 8-9 applies equally and is not separately discussed hereinafter. Further discussions of Watanabe's fifth embodiment below apply the second mapping from Figures 8-9.



TSMC-1003, ¶147.

Dummy plug 52, comprising the same barrier metal layer 72 and copper film 71 as wiring 51, is conductive, but is arranged to be incapable of having current flow therethrough because it extends to and terminates in a "non-forming region" of insulating film 27 (i.e., where there is no wiring 39) or toward dummy wiring 61. TSMC-1004, ¶¶[0118]-[0122], [0127], [0185]-[0186], Figs. 8-9; TSMC-1003, ¶148. The same rationale for dummy plugs 34 applies to dummy plugs 52. *See supra*, §§VI.A.2.(a).(7)-(8); TSMC-1003, ¶148.

Watanabe's same "dual damascene" manufacturing process from Figures 12A-12N applies to Figure 8. TSMC-1004, ¶¶[0049], [0118]-[0123], [0134]-[0171], Figs. 12A-12N. Wiring 51 thus forms a dual-damascene structure with

plug 53 and with dummy plug(s) 52, analogous to wiring 39, plug 32, and dummy plug(s) 34. *Id*., ¶¶[0072], [0171]; *supra*, §VI.A.2.(a).(9); TSMC-1003, ¶149.

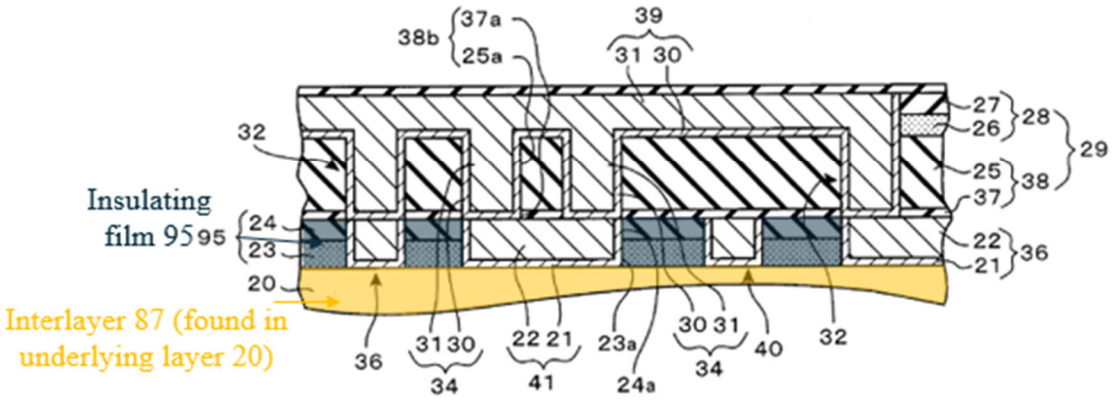
3. Claim 2

At least Watanabe's second and fifth embodiments meet claim 2. TSMC-1003, ¶¶151-62.

a) [2.a]

Watanabe's second embodiment (Figures 3-4) discloses a "second insulating film" (e.g., constituted by "insulating film 95" and "interlayer insulating film 87" of underlying layer 20, collectively, or optionally insulating film 87 alone). TSMC-1004, ¶¶[0061], [0089], [0172]-[0174], Figs. 3, 14; TSMC-1003, ¶¶152-53. For each embodiment, underlying layer 20 includes components shown in Figure 14, such as interlayer insulating film 87:

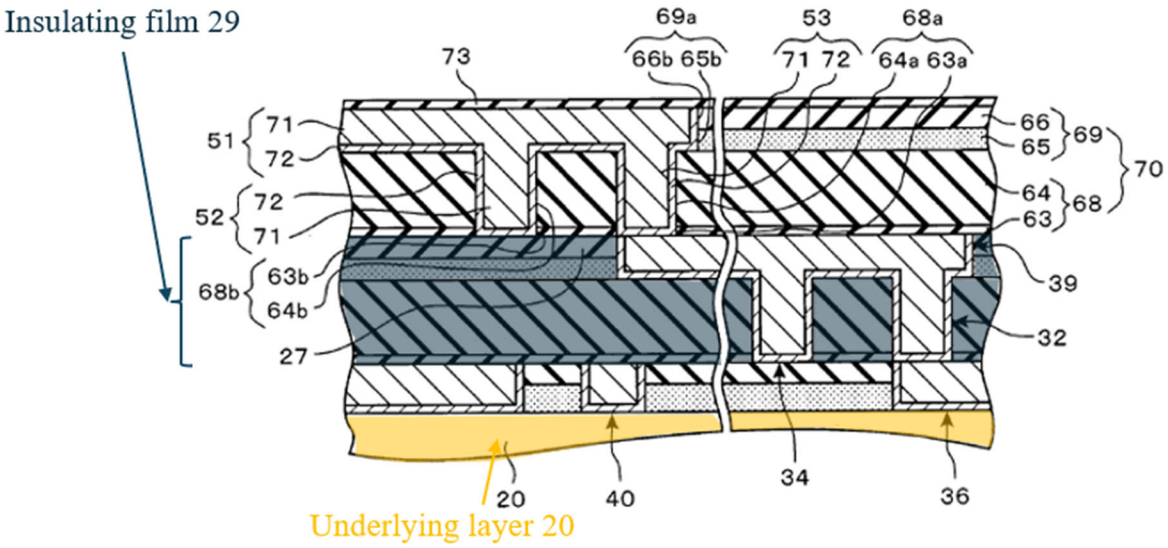
FIG. 3



TSMC-1004, ¶¶[0173]-[0174], [0061], [0089], [0094], [0116]; TSMC-1003, ¶153.

Watanabe's fifth embodiment (Figures 8-9) discloses a "second insulating film" (e.g., "insulating film 29" constituted by upper insulating film 28 and lower insulating film 38; or alternatively just lower insulating film 38). TSMC-1004, ¶¶[0066]-[0067], [0116]-[0117], [0172]-[0175], Figs. 1, 8, 12, 14; TSMC-1003, ¶154. Insulating film 29 is formed on a semiconductor substrate (which is part of underlying layer 20; "silicon substrate 96" in Figure 14):

FIG. 8

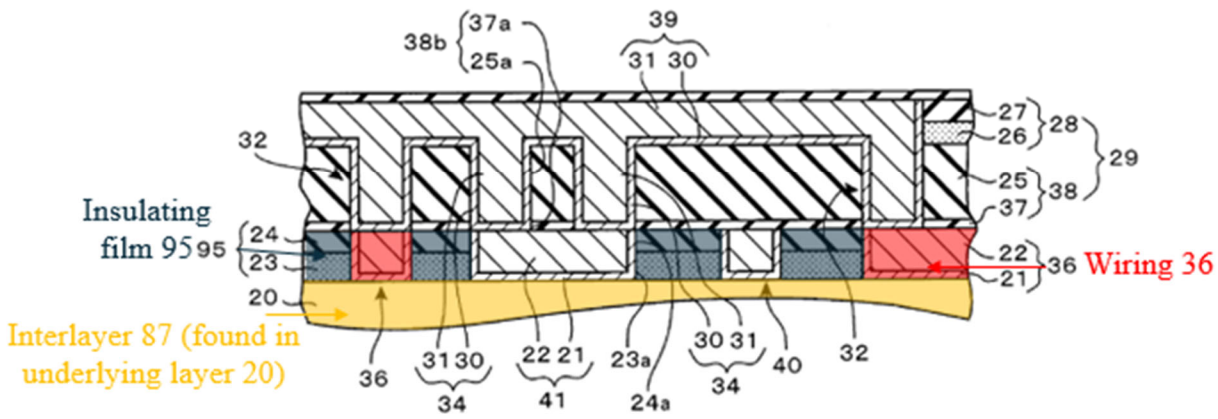


TSMC-1004, ¶¶[0061], [0172]-[0175]; Figs. 1, 8, 12, 14; TSMC-1003, ¶154.

b) [2.b]

Watanabe's second embodiment includes wiring 36 ("first interconnect") formed on interlayer insulating film 87/insulating film 95 ("second insulating film"):

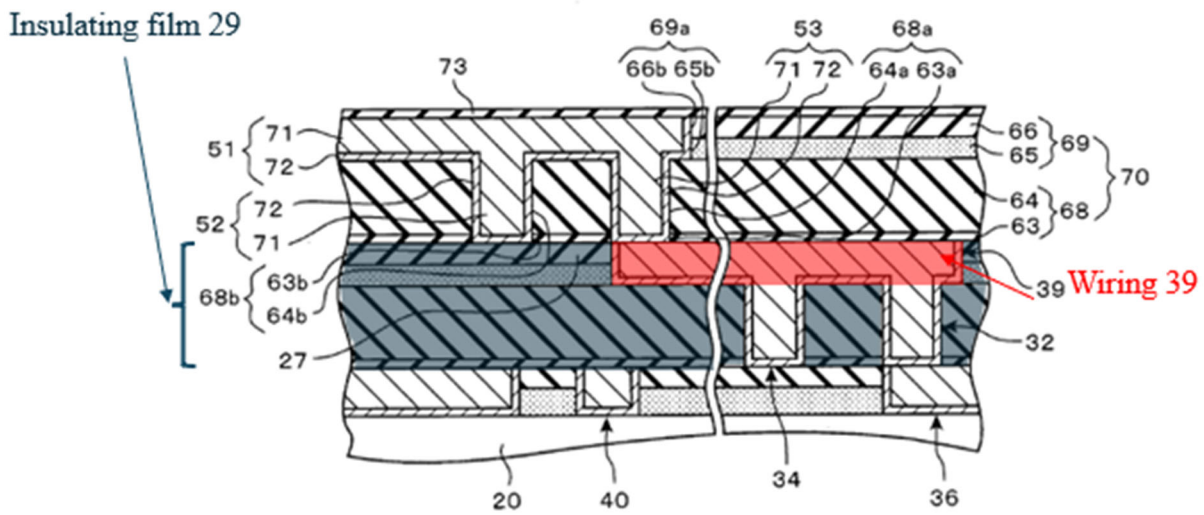
FIG. 3



TSMC-1004, ¶¶[0061], [0089], [0172]-[0174], Figs. 3, 14; TSMC-1003, ¶¶155-56.

Watanabe's fifth embodiment includes wiring 39 ("first interconnect") formed on insulating film 29 ("second insulating film"):

FIG. 8

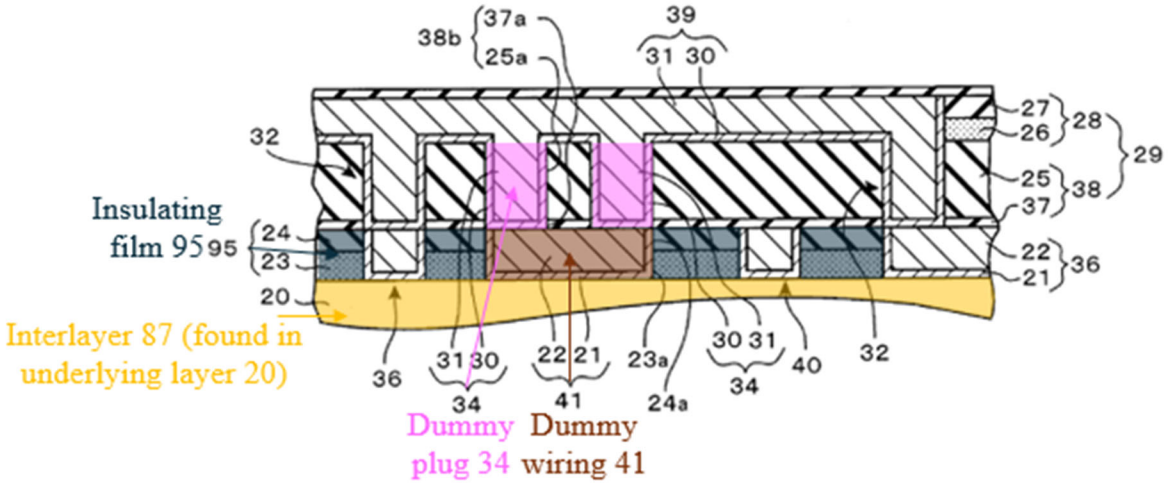


TSMC-1004, ¶¶[0066]-[0069], [0116]-[0117], [0172]-[0175], Figs. 1, 8, 12, 14; TSMC-1003, ¶157 (further noting alternative of lower insulating film 38 as second insulating film for fifth embodiment).

c) [2.c]

Watanabe's second embodiment discloses a first dummy interconnect ("dummy wiring 41"), formed on the second insulating film (e.g., insulating film 87/insulating film 95) and connected to a dummy via (e.g., "dummy plug 34"):

FIG. 3



TSMC-1004, ¶¶[0061], [0089]-[0091], [0144]-[0149], [0165], [0172]-[0174], Figs. 3, 12A-12M, 14; TSMC-1003, ¶¶158-60.

Watanabe's fifth embodiment (Figures 8-9) discloses a first dummy interconnect ("dummy wiring 61") formed on insulating film 29 (or lower insulating film 38) ("second insulating film"). TSMC-1004, ¶[0127], Figs. 1, 8-9;

TSMC-1003, ¶¶161-62. Dummy wiring 61 and wiring 39 are at the same level and on the same insulating film (e.g., insulating film 29). TSMC-1004, ¶[0127]; *supra*, VI.A.2.(a).(5); TSMC-1003, ¶¶161-62. Annotated Figures 8-9 disclose the approximate location of dummy wiring 61 when Figure 8 accounts for dummy wiring 61, demonstrating that dummy wiring 61 is on insulating film 29 (or lower insulating film 38):

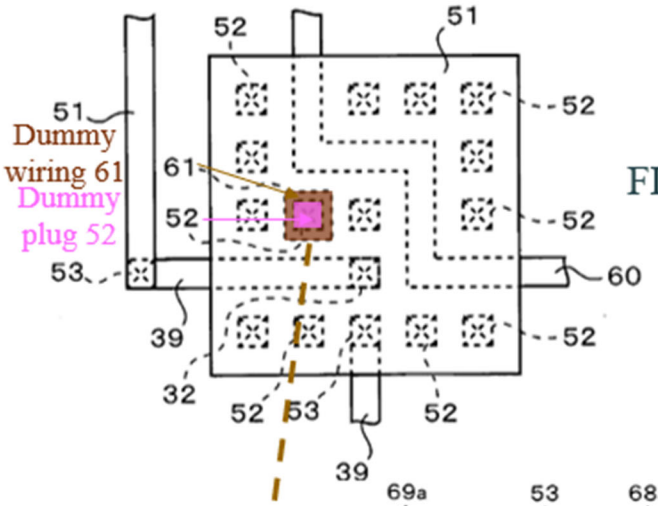


FIG. 9

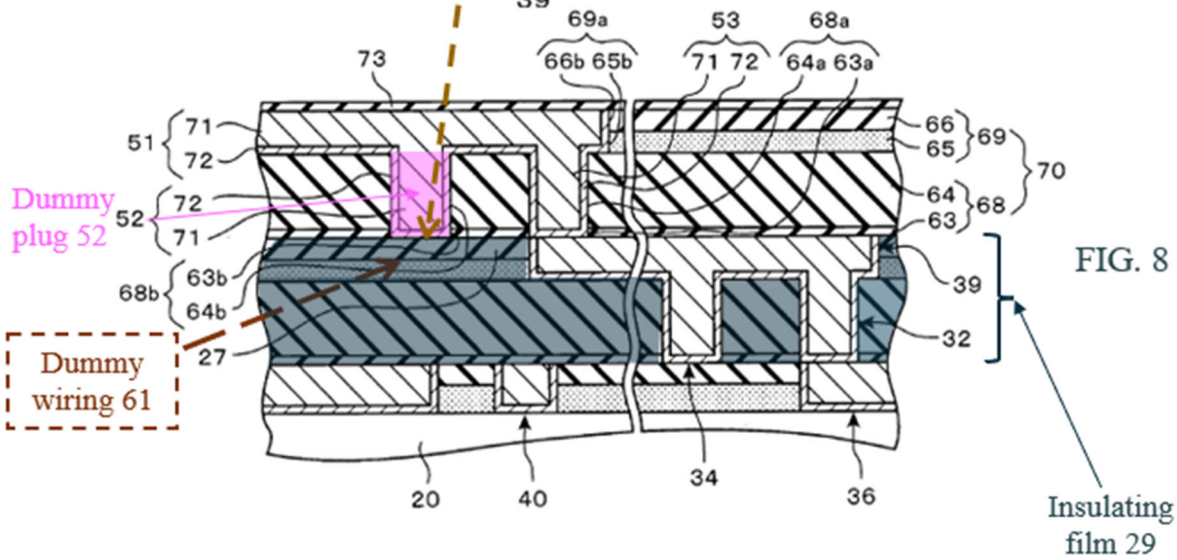


FIG. 8

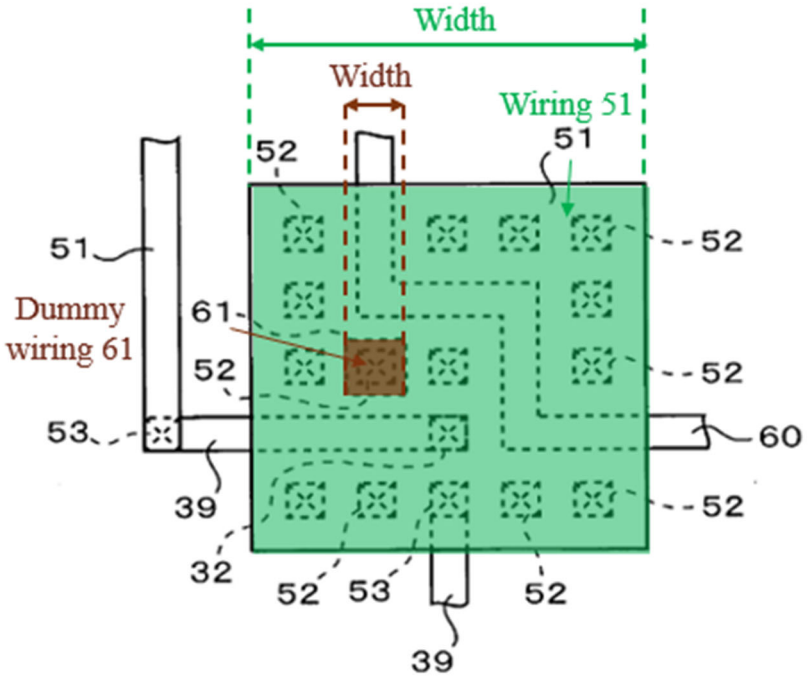
TSMC-1003, ¶161. Dummy plug 52 ("dummy via") is connected to dummy wiring 61 as shown. TSMC-1004, ¶[0127]; TSMC-1003, ¶162.

4. Claim 3

At least Watanabe's fifth embodiment meets claim 3.

In Watanabe's fifth embodiment, dummy wiring 61 ("first dummy interconnect") has a smaller width than wiring 51 ("second interconnect"):

FIG. 9



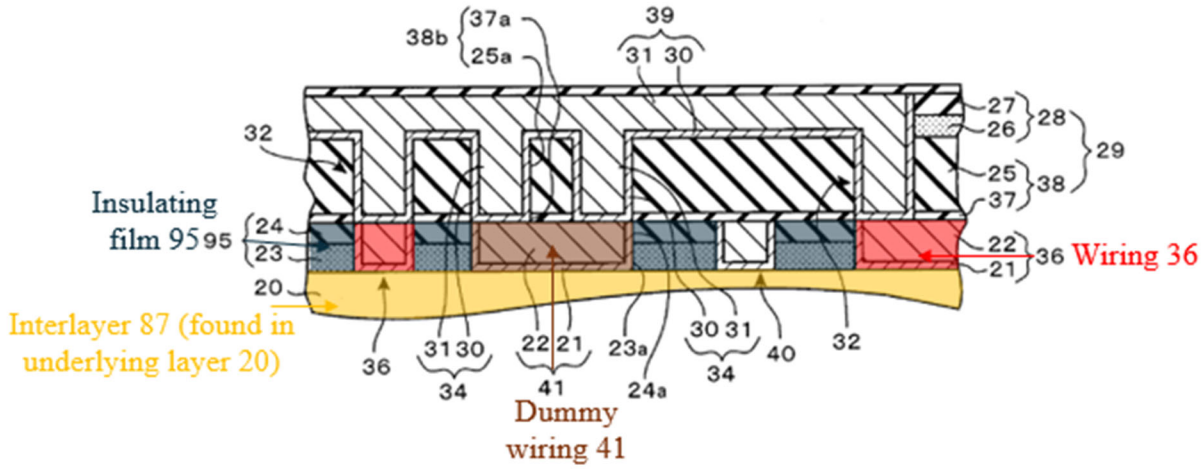
TSMC-1004, ¶¶[0116]-[0117], [0125], [0127], Fig. 9; TSMC-1003, ¶¶163-64.

5. Claim 7

At least Watanabe's second and fifth embodiments meet claim 7. TSMC-1003, ¶¶165-69.

In Watanabe's second embodiment (Figures 3-4, together with Fig. 14), wiring 36 ("first interconnect") and dummy wiring 41 ("first dummy interconnect") are buried in insulating film 95, an upper portion of "second insulating film" (collective insulating film 95/interlayer insulating film 87):

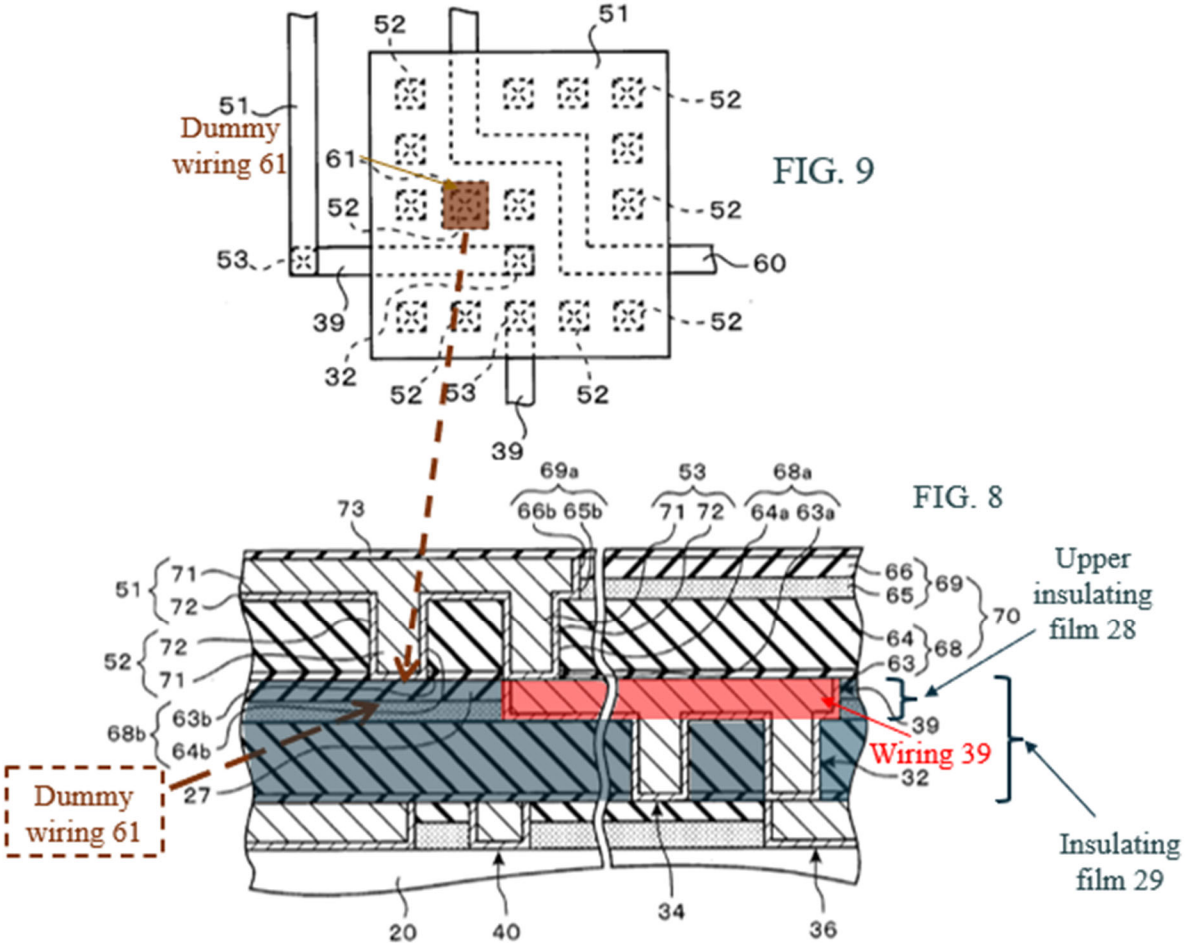
FIG. 3



TSMC-1004, ¶¶[0061]-[0065], [0089], [0172]-[0174], Figs. 3, 12, 14; TSMC-1003, ¶166.

In Watanabe's fifth embodiment (Figures 8-9), wiring 39 ("first interconnect") and dummy wiring 61 ("first dummy interconnect") are buried in insulating film 28, i.e., an upper portion of insulating film 29 ("second insulating film"). *Id*., ¶¶[0066]-[0070], [0116]-[0117], [0127], [0172]-[0175], Figs. 1, 8-9, 12, 14; TSMC-1003, ¶¶167-69.

As outlined above, dummy wiring 61 and wiring 39 are in the same layer. *Id.*, ¶[0127]; *supra*, §VI.A.2.(a).(5); TSMC-1003, ¶168. Annotated Figures 8-9 show the approximate location of dummy wiring 61, demonstrating that dummy wiring 61 is in upper insulating film 28 of insulating film 29:



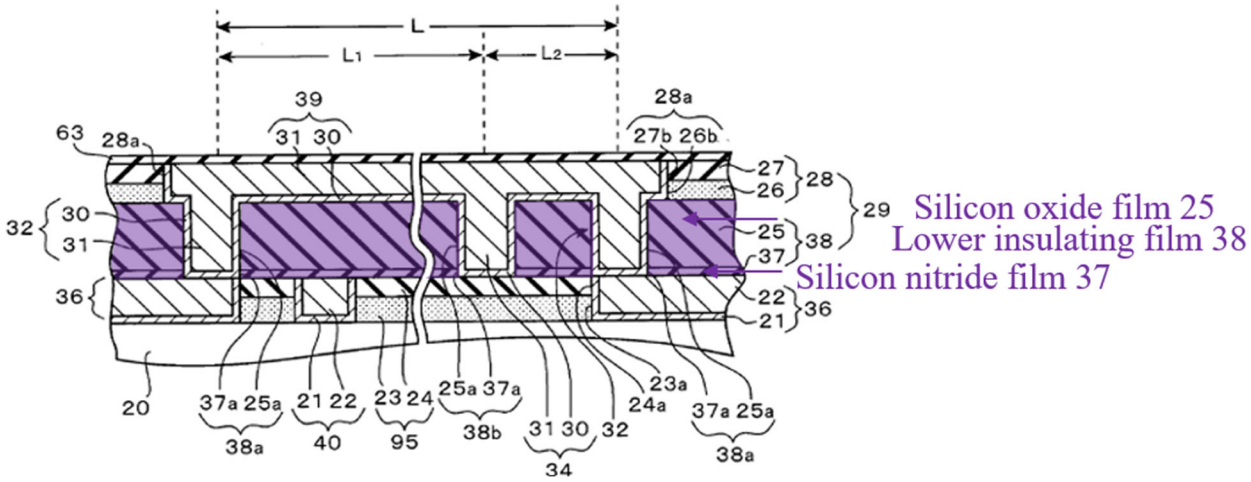
TSMC-1003, ¶167.

6. Claim 11

At least Watanabe's first-to-third and fifth embodiments satisfy claim 11.

In the first-to-third embodiments, Watanabe's first insulating film ("lower insulating film 38") includes a multilayer structure constituted by a SiN film ("silicon nitride film 37") and a SiO_2 film ("silicon oxide film 25"), as demonstrated in Figure 1:

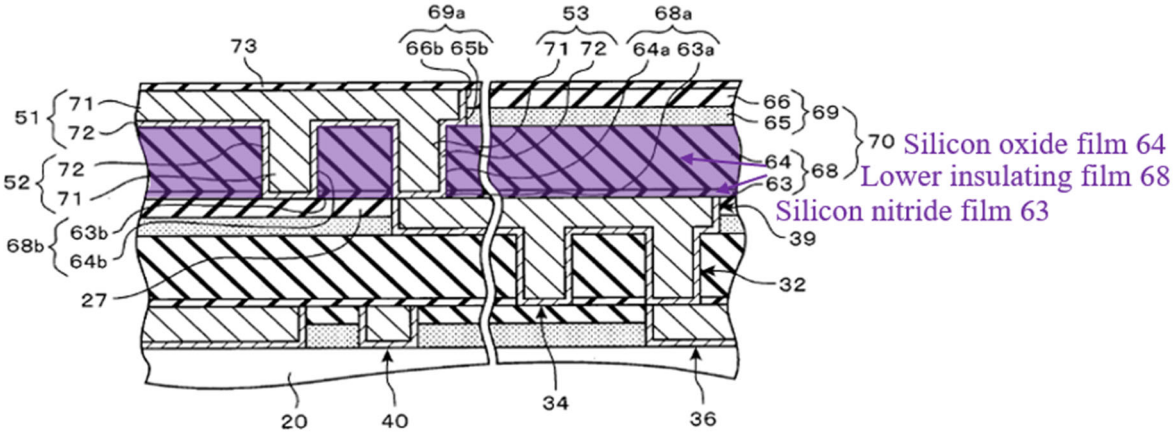
FIG. 1



TSMC-1004, ¶¶[0066], [0089], [0094], [0150], [0184], Figs. 1, 3, 5A-5C, 12E, 12M; TSMC-1003, ¶¶170-71.

In Watanabe's fifth embodiment, the first insulating film ("lower insulating film 68") has a multilayer structure having a SiN film ("silicon nitride film 63") and a SiO_2 film ("silicon oxide film 64"), as seen in Figure 8:

FIG. 8



TSMC-1004, ¶[0119], Fig. 8; TSMC-1003, ¶172.

7. Claim 12

In its first-to-third embodiments, Watanabe discloses a second interconnect (wiring 39) having a double-layered structure with a first barrier film (e.g., "barrier metal layer 30") and a first conductive film (e.g., "copper film 31"). TSMC-1004, ¶¶[0068]-[0069], [0089], [0094], [0166]-[0168], Figs. 1, 3, 5A-5C, 12L-12M; TSMC-1003, ¶¶173-174. In Watanabe's fifth embodiment, the second interconnect (wiring 51) likewise has a double-layered structure with a first barrier film (e.g., "barrier metal layer 72") and a first conductive film (e.g., "copper film 71"). *Id*., ¶[0118], Fig. 8; TSMC-1003, ¶¶173-74.

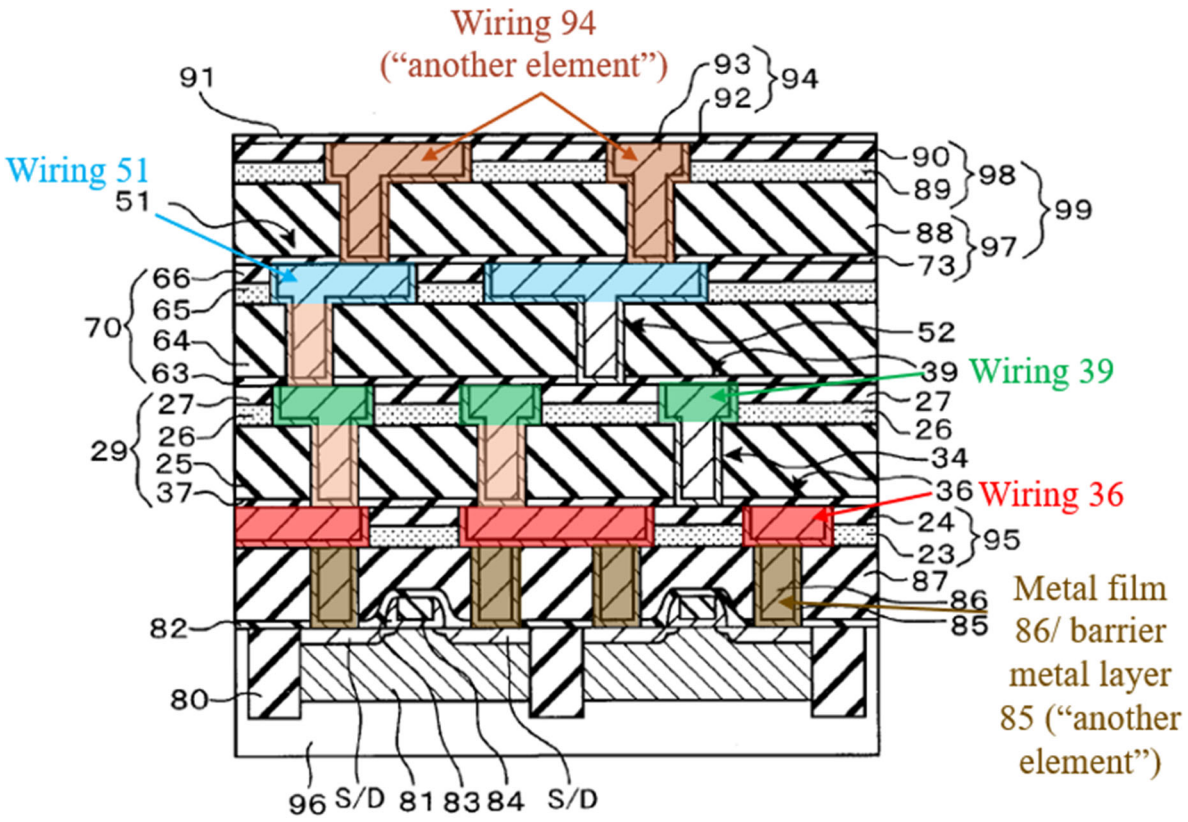
8. Claim 13

Watanabe discloses that its "first conductive films" in the first-to-third and fifth embodiments include copper, e.g., copper film 31 and copper film 71. *Supra*, §VI.A.7; TSMC-1003, ¶¶175-77.

9. Claim 14

In Watanabe's first-to-third and fifth embodiments, each of the first and second interconnects (e.g., wirings 36, 39, and 51) are connected to another element or an external electrode. TSMC-1003, ¶¶178-86. Watanabe explains that, while a two-wiring structure (wirings 36 and 39) is disclosed, any number of wiring layers can be laminated by repeating the same method (of Figures 12A-12M). TSMC-1004, ¶[0171]; TSMC-1003, ¶180. Watanabe's Figure 14 illustrates a structure having four layers of wirings (including wirings 36, 39, and 51), which are each connected to other elements. *See id.*, ¶¶[0051], [0172]-[0181], Fig. 14. For the first-to-third embodiments, wiring 36 is connected to metal film 86 and wiring 39 is connected to wiring 51 by a conductive plug. *Id.* For the fifth embodiment, wiring 39 is connected to wirings 36 and 51 by conductive plugs, and wiring 51 is connected to wiring 94 by another conductive plug, which constitute "other elements," as seen in Figure 14:

FIG. 14



TSMC-1003, ¶180.

Additionally, in each embodiment, underlying layer 20 includes semiconductor transistors as seen in Figure 14, including gate electrodes 84, source/drain regions S/D on silicon substrate 96, and conductive plugs (having barrier metal layer 85 and metal film 86), which are connected to wirings 36, 39, 51 as shown above. TSMC-1004, ¶¶[0173]-[0178]; *see also id.*, ¶¶[0061] (underlying layer 20 has a structure with MOSFET formed in active region of silicon wafer), [0089], [0094], [0116]; TSMC-1003, ¶¶181-85. Accordingly, given

that wirings 36, 39 and wirings 39, 51 are the first and second interconnects for the first-to-third, and fifth embodiments, respectively (*supra*, §§VI.A.2.(a).(3), (5), VI.A.2.(b)-(d)), each of these wirings/interconnects is connected to another element or external electrode. TSMC-1003, ¶¶184-86.

10. Claim 15

At least Watanabe's first-to-third and fifth embodiments satisfy claim 15. TSMC-1003, ¶¶187-96.

a) [15.a]

Watanabe discloses that the first interconnect, second interconnect, and the via constitute part of a closed circuit. For the first-to-third embodiments, wiring 36, wiring 39, and conductive plug 32 form a functional electrical path. TSMC-1004, ¶[0073], Figs. 1, 3, 5A-5C, 8; TSMC-1003, ¶¶188-91. In Watanabe's fifth embodiment, wiring 39, wiring 51, and conductive plug 53 similarly form a functional electrical path. *Id*., ¶[0122], Figs. 8, 14; TSMC-1003, ¶¶188-91.

b) [15.b]

Watanabe discloses that the dummy via ("dummy plug 34" or "dummy plug 52") does not constitute a closed circuit. *Supra*, §§VI.A.2.(a).(7)-(8), VI.A.2.(d); TSMC-1003, ¶¶192-96.

11. Claim 16

At least Watanabe's third and fifth embodiments meet claim 16. TSMC-1003, ¶¶197-201. Figures 5A (third embodiment) and 9 (fifth embodiment) disclose first interconnects (wirings 36, 39) having a smaller width than the second interconnects (wirings 39, 51):

FIG. 5A

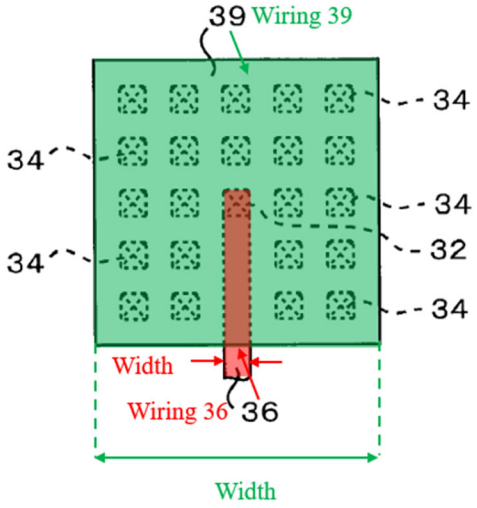
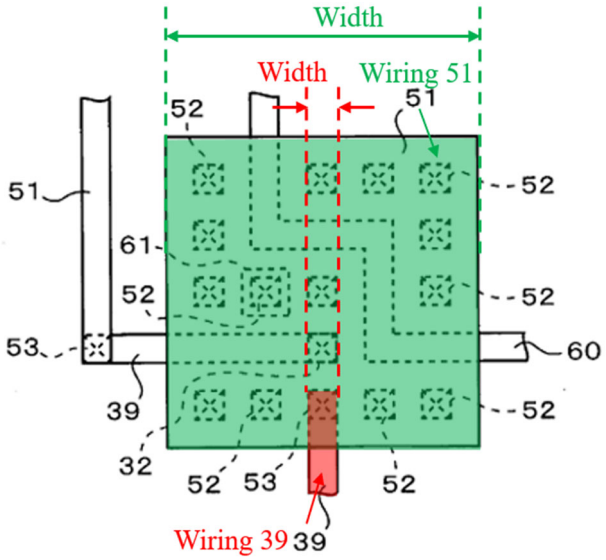


FIG. 9



TSMC-1004, ¶¶[0094]-[0095], [0124]-[0125]; TSMC-1003, ¶¶197-201.

12. Claim 21

For each of the first-to-third and fifth embodiments, Watanabe discloses that the first interconnect (e.g., wiring 36, 39) and the second interconnect (e.g., wiring 39, 51) extend in a same direction (i.e., along "L" direction):

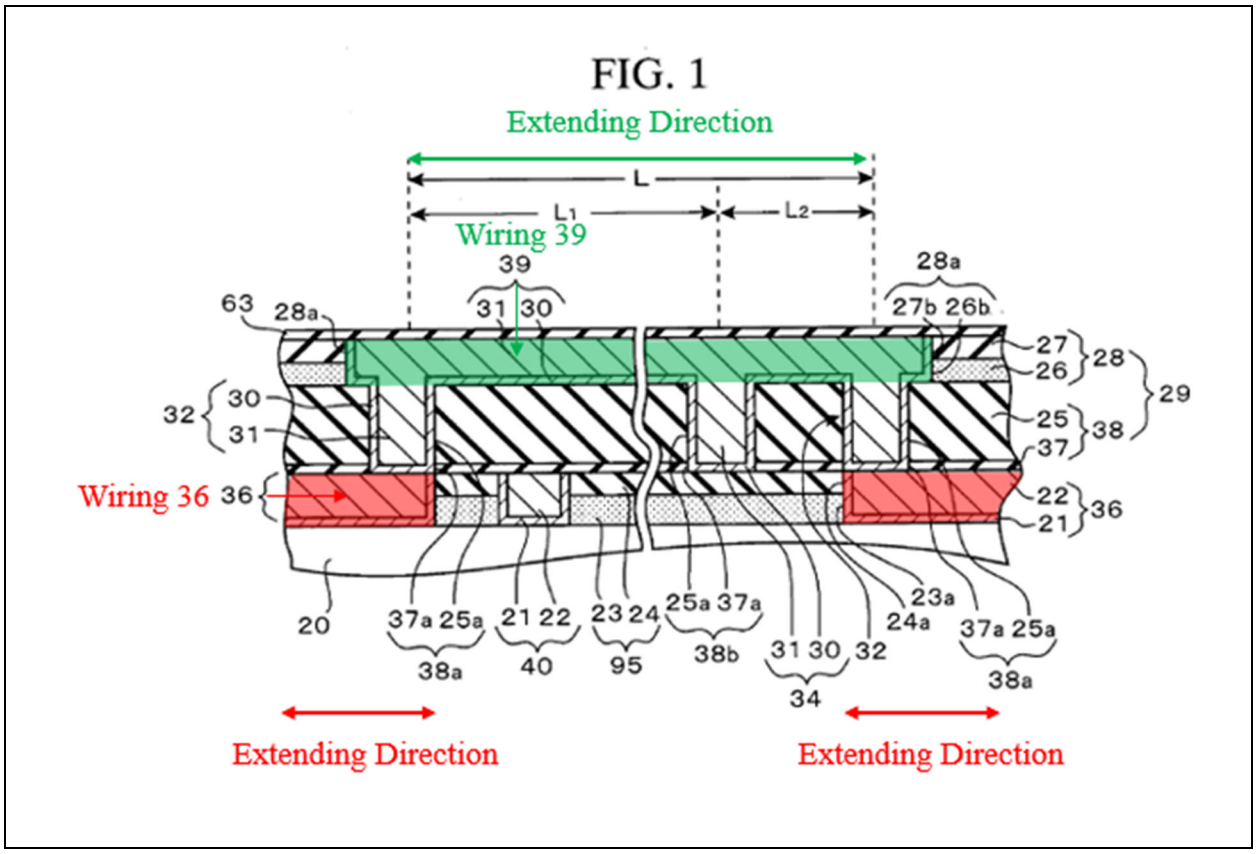


FIG. 2

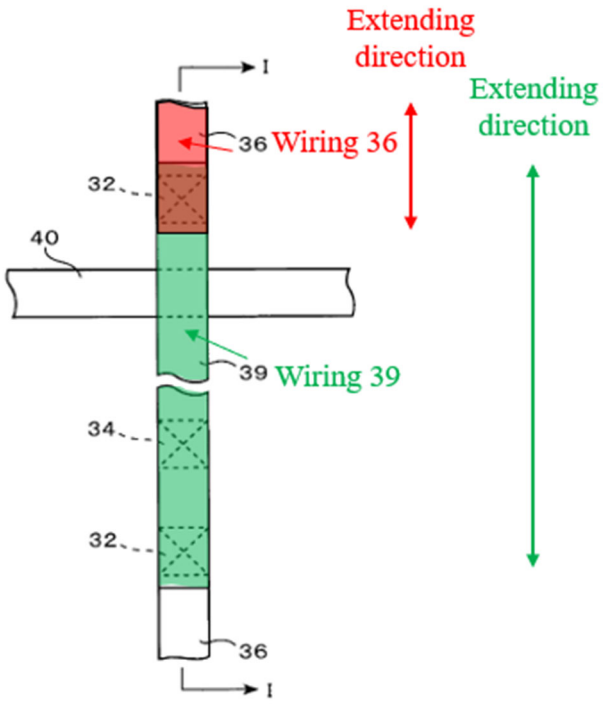

Extending direction
Extending direction
I
36 Wiring 36
32
40
39 Wiring 39
34
32
36
I

FIG. 5A

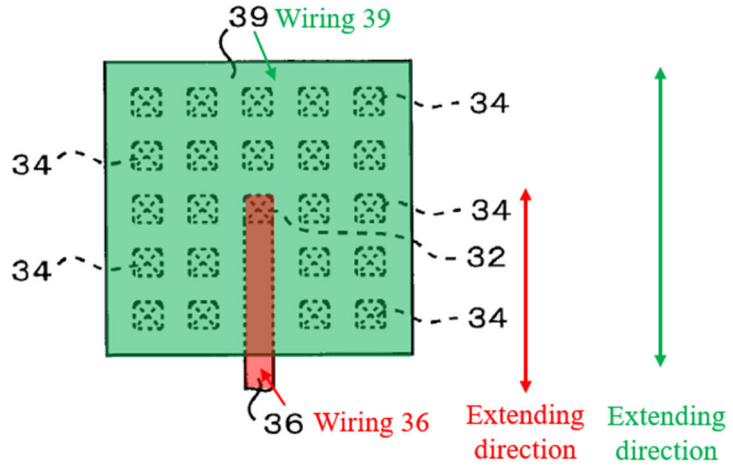
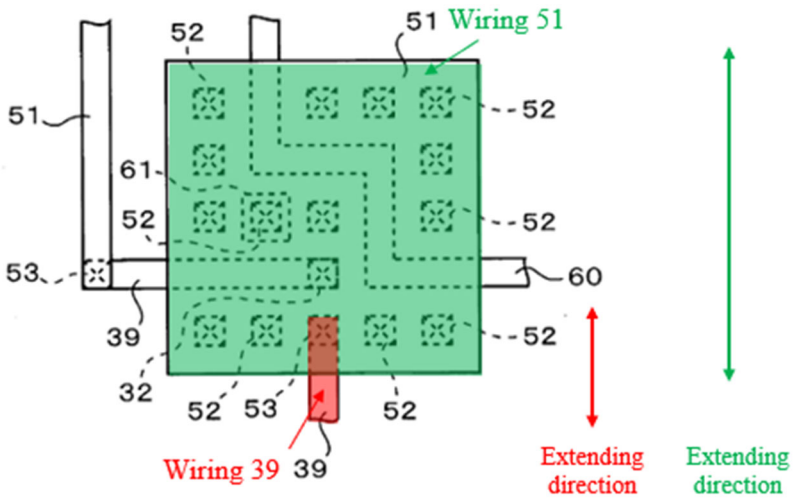

39 Wiring 39
34
34
34
34
32
34
36 Wiring 36
Extending direction
Extending direction

FIG. 9



TSMC-1004, ¶¶[0095], [0111], Figs. 1-2, 4, 5A-5C, 9; TSMC-1003, ¶¶202-05.

13. Claim 22

Watanabe's first-to-third and fifth embodiments provide at least one dummy via (e.g., dummy plug 34) on an extended line along which the first interconnect (e.g., wiring 36) extends, as shown in Figures 2, 4, 5A, and 9:

FIG. 2

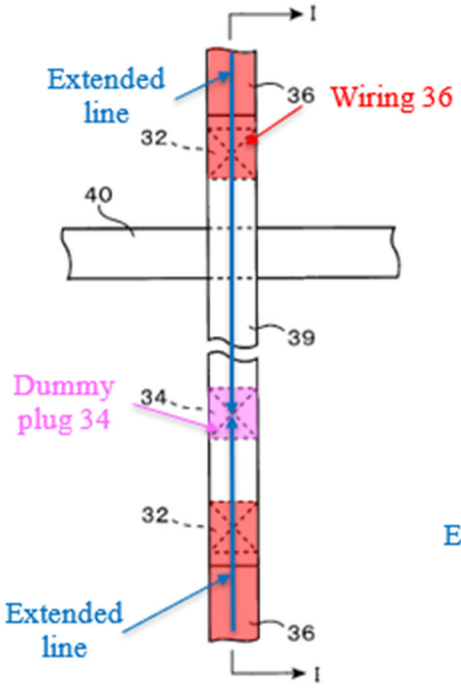


FIG. 4

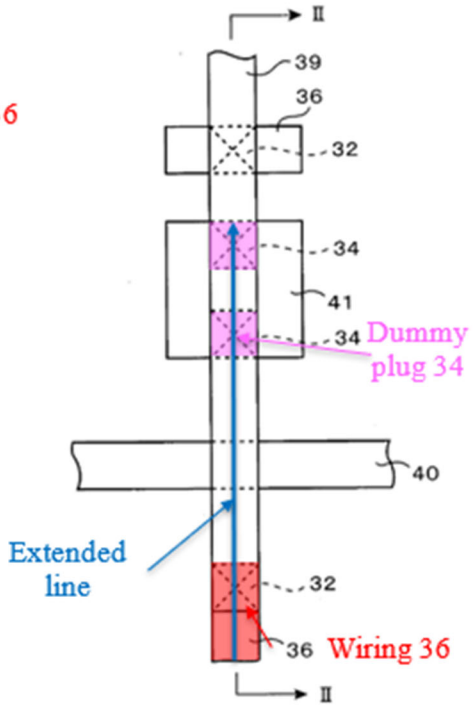


FIG. 5A

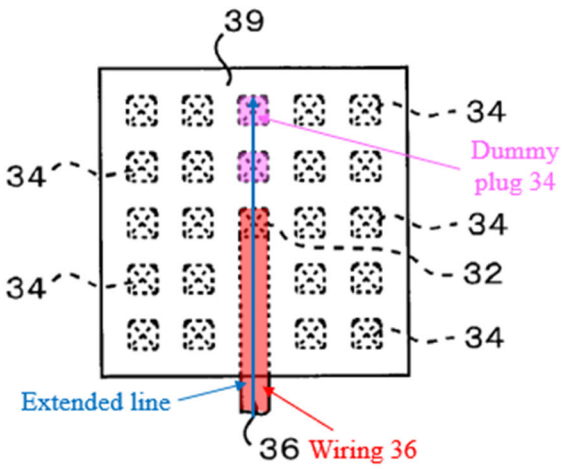
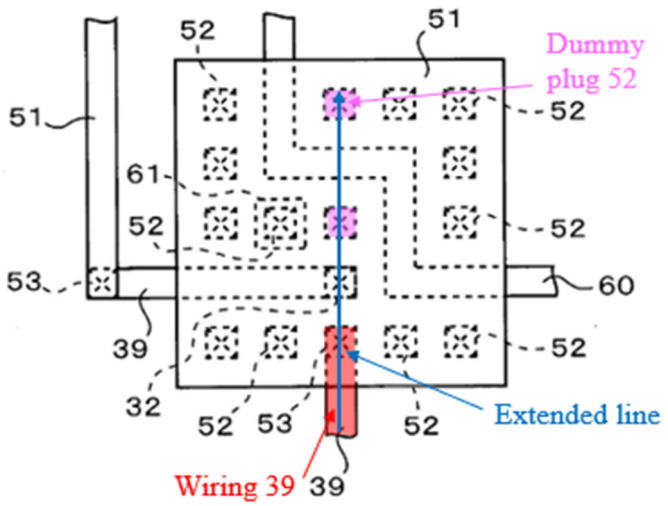


FIG. 9



TSMC-1003, ¶¶206-08.

14. Claim 25

The '623 patent refers to the "space" between a via and dummy via as corresponding to the distance from an edge of the via and the closest edge of an adjacent dummy via. TSMC-1001, 4:18-22.

Applicable to its first-to-third and fifth embodiments, Watanabe discloses that its via (e.g., plug 32) and dummy via (e.g., dummy plug 34) are spaced at a distance of 25 μm or less, teaching, for example, that the interval between the neighboring plugs (including plug 32 and dummy plug 34) was fixed to **0.3 μm**. TSMC-1004, ¶¶[0100]-[0105], [0081], [0086]-[0087], Figs. 15A-17C; TSMC-1003, ¶¶209-14. This interval/pitch "p_2" is shown below:

FIG. 16B

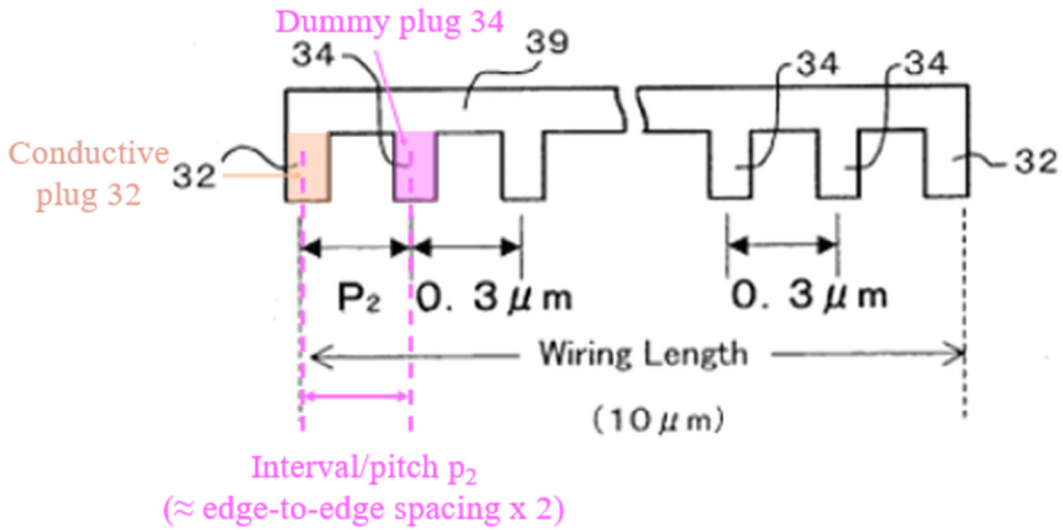
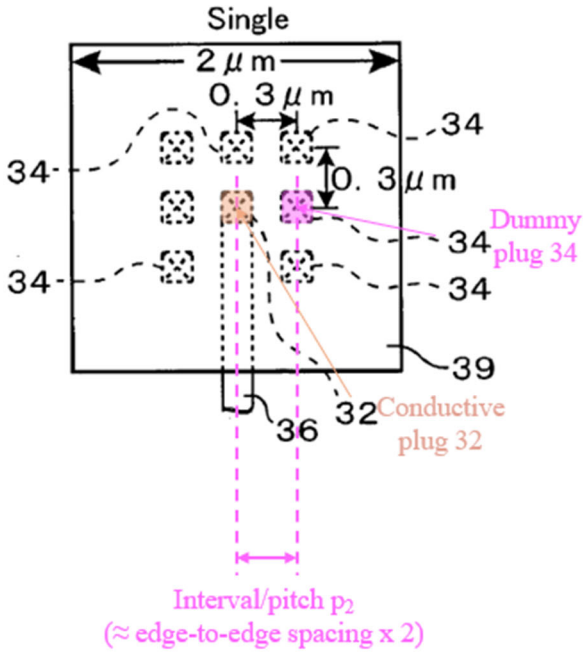


FIG. 17B



TSMC-1003, ¶211.

As shown above, the interval/pitch "p_2" in Watanabe is the center-to-center distance between a via and an adjacent dummy via; thus, the spacing from a right

edge of the annotated conductive plug 32 to a left edge of the adjacent annotated dummy plug 34 is necessarily less than the interval/pitch p_2—in Watanabe's case, the edge-to-edge spacing is approximately half the pitch interval. *Id*., ¶¶211-212.

Watanabe teaches that to prevent stress-migration, it is preferable that pitch p_2 is less than 1 μm, and more preferably less than 0.6 μm. TSMC-1004, ¶¶[0032]-[0033], [0053], [0086]-[0087], [0190]-[0191], [0193], Fig. 16A; TSMC-1003, ¶¶213-14. Thus, Watanabe discloses vias and dummy vias spaced at a distance of 0.3 μm or less, well below 25 μm. *Id*.

15. Claim 26

Applicable to its first-to-third and fifth embodiments, Watanabe discloses a via-to-dummy-via interval/pitch of 1 μm or less, disclosing a spacing of less than 1.0 μm, less than 0.6 μm, and 0.3 μm. *Supra*, §VI.A.14. As discussed for claim 25, the spacing between the via and dummy via is necessarily less than (approximately half of) the interval/pitch, so Watanabe discloses the claimed spacing of 1 μm or less. TSMC-1003, ¶¶215-17.

16. Claim 28

At least Watanabe's second, third, and fifth embodiments all disclose a plurality of dummy vias (dummy plugs 34 and 52), such as seen in Figures 3-4 (second embodiment), 5A-5C (third embodiment), and 8-9 (fifth embodiment). TSMC-1004, ¶¶[0108], [0114]; TSMC-1003, ¶¶218-20.

17. Claim 32

Applicable to its first-to-third and fifth embodiments, Watanabe discloses in Figures 2, 4, 5B, and 9 that a distance ("D1") between the via (plugs 32 or 53) and one end of the second interconnect (wiring 39 or 51) is shorter than a distance ("D2") between the dummy via (dummy plug 34 or 52) and the one end of the second interconnect, and shorter than a distance ("D3") between the via and the other end of the second interconnect. TSMC-1003, ¶¶221-26. These features are illustrated below:

FIG. 2

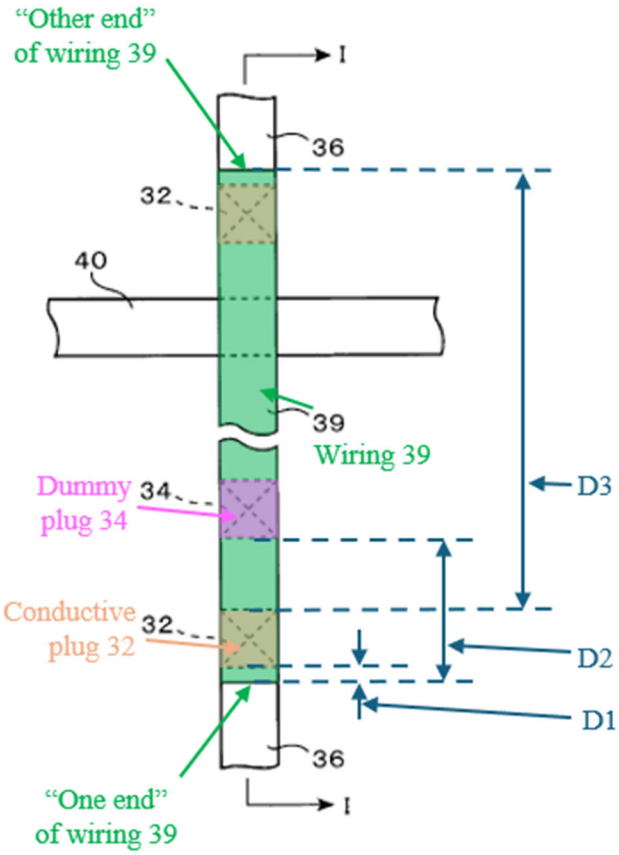


FIG. 5B

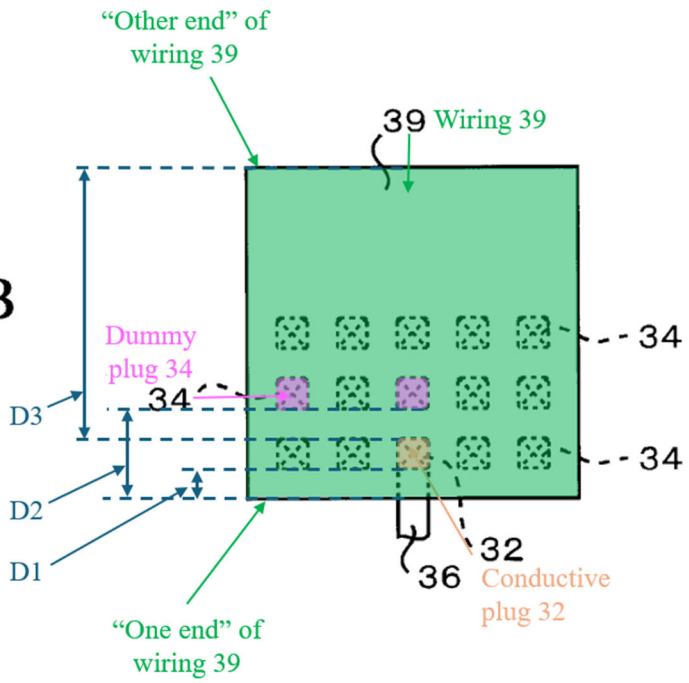
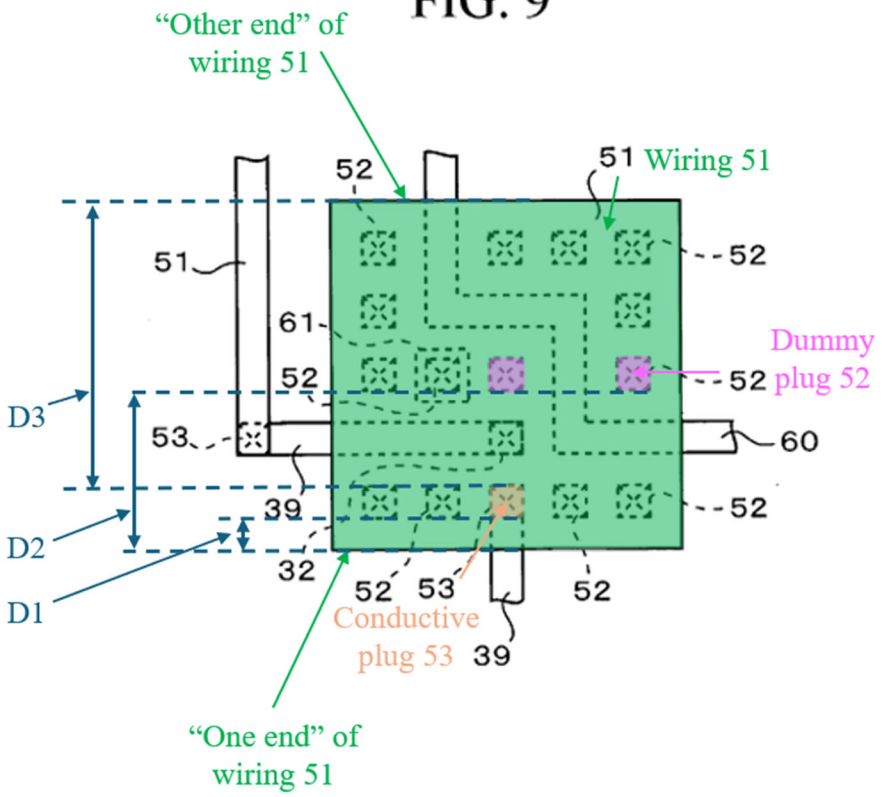

"Other end" of wiring 39
39 Wiring 39
34
34
Dummy plug 34
34
D3
D2
D1
32
36
Conductive plug 32
"One end" of wiring 39

FIG. 9


"Other end" of wiring 51
52
51 Wiring 51
51
52
61
52
Dummy plug 52
52
D3
53
60
39
52
D2
32
52
53
52
D1
Conductive plug 53
39
"One end" of wiring 51

Id., ¶225. Thus, Watanabe discloses plug 32/plug 53 positioned closer to one end of wiring 39/wiring 51 than an adjacent dummy plug 34/dummy plug 53, and plug 32/plug 53 is closer to that end than opposite end of the wiring 39/wiring 51. *Id*., ¶226.

18. Claim 39

In each of its first-to-third and fifth embodiments, Watanabe's dummy via(s) (e.g., dummy plugs 34, 52) and second interconnect(s) (e.g., wirings 39, 51) are made of the same conductive film (e.g., copper film 31, barrier metal layer 30). TSMC-1004, ¶¶[0067]-[0070], [0072], [0166]-[0168], Figs. 12L-12M; TSMC-1003, ¶¶227-32. "The barrier metal layer 30 and the copper film 31…constitute the second wiring 39" and "the portion of the second wiring 39...in the dummy via hole 38b [is] the dummy plug." TSMC-1004, ¶[0168]; *see also id.*, ¶¶[0118], [0122] (wiring buried in dummy via hole 68b is dummy plug 52); TSMC-1003, ¶¶231-32.

19. Claim 40

Applicable to its first-to-third and fifth embodiments, Watanabe's dummy via(s) (dummy plugs 34, 52) and second interconnect(s) (wiring 39, 51) include a Cu film; specifically, dummy plug 34 and wiring 39 include copper film 31, and dummy plug 52 and wiring 51 include copper film 71. TSMC-1004, ¶¶[0067]-

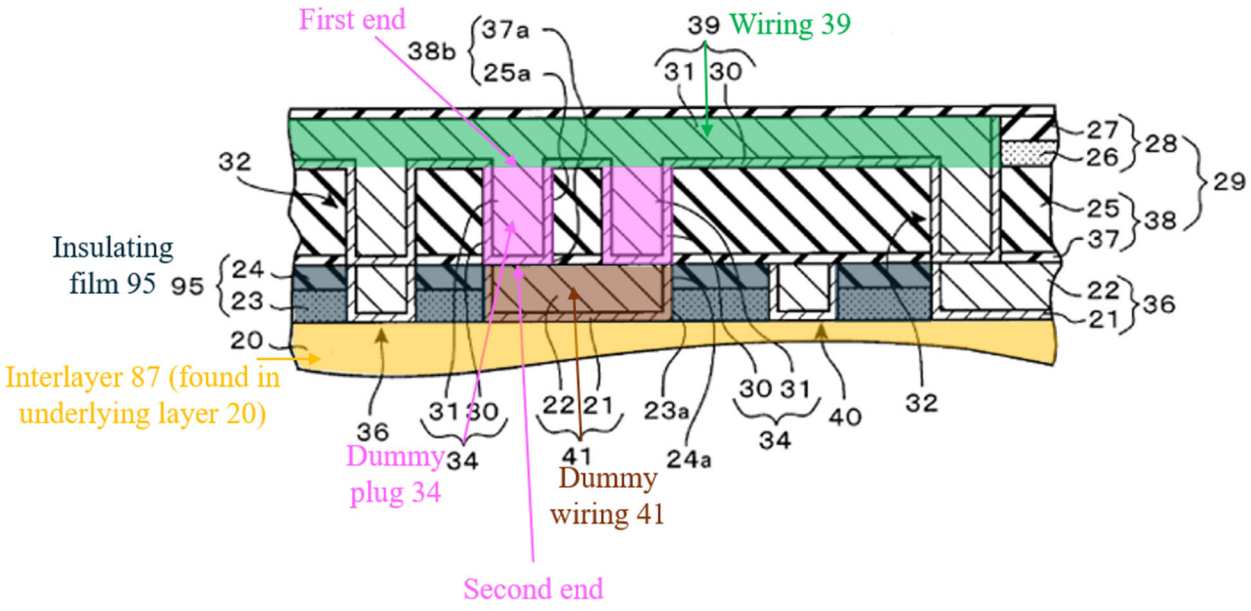
[0070], [0072], [0118], [0121]-[0122], [0166]-[0167]; *supra*, §§VI.A.7-8; TSMC-1003, ¶¶233-36.

20. Claim 42

At least Watanabe's second and fifth embodiments meet claim 42. TSMC-1003, ¶¶237-41.

Watanabe's second embodiment discloses that a dummy via (e.g., dummy plug 34) includes a first end connected to the second interconnect (e.g., wiring 39) and a second end connected to a first dummy interconnect (e.g., dummy wiring 41), the first dummy interconnect is surrounded by insulating film 95:

FIG. 3



TSMC-1004, ¶¶[0089]-[0090], [0140]-[0144], [0172]-[0174], Figs. 3, 12B-12D, 12M; TSMC-1003, ¶¶238-39. Underlying layer 20 also includes interlayer

insulating film 87 beneath dummy wiring 41 (TSMC-1004, ¶[0173], Fig. 14), thus further surrounding dummy wiring 41 with an insulating film (i.e., interlayer insulating film 87 and insulating film 95, collectively). TSMC-1003, ¶¶238-39.

In Watanabe's fifth embodiment, dummy via (e.g., dummy plug 52) has a first end connected to second interconnect (e.g., wiring 51) and a second end connected to a first dummy interconnect (e.g., dummy wiring 61). TSMC-1004, ¶¶[0127], [0116]-[0123], [0140]-[0144], [0172]-[0175], Figs. 8-9, 12B-12D, 12M; TSMC-1003, ¶¶240-41.

Dummy wiring 61 is formed in the same layer as wiring 39, and is connected to dummy plug 52. *Id*., ¶[0127]. As explained *supra* §§VI.A.3, 5, dummy wiring 61 and wiring 39 are formed in the same insulating film (e.g., insulating film 29). Dummy wiring 61 is surrounded by insulating film 29:

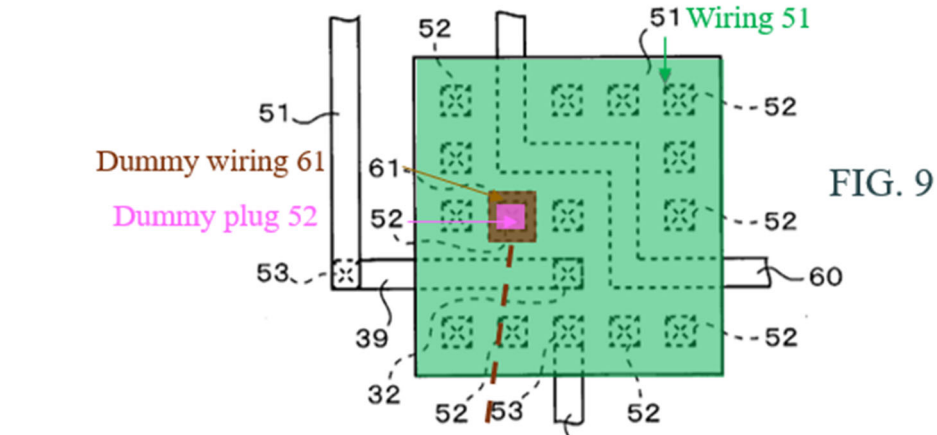


FIG. 9

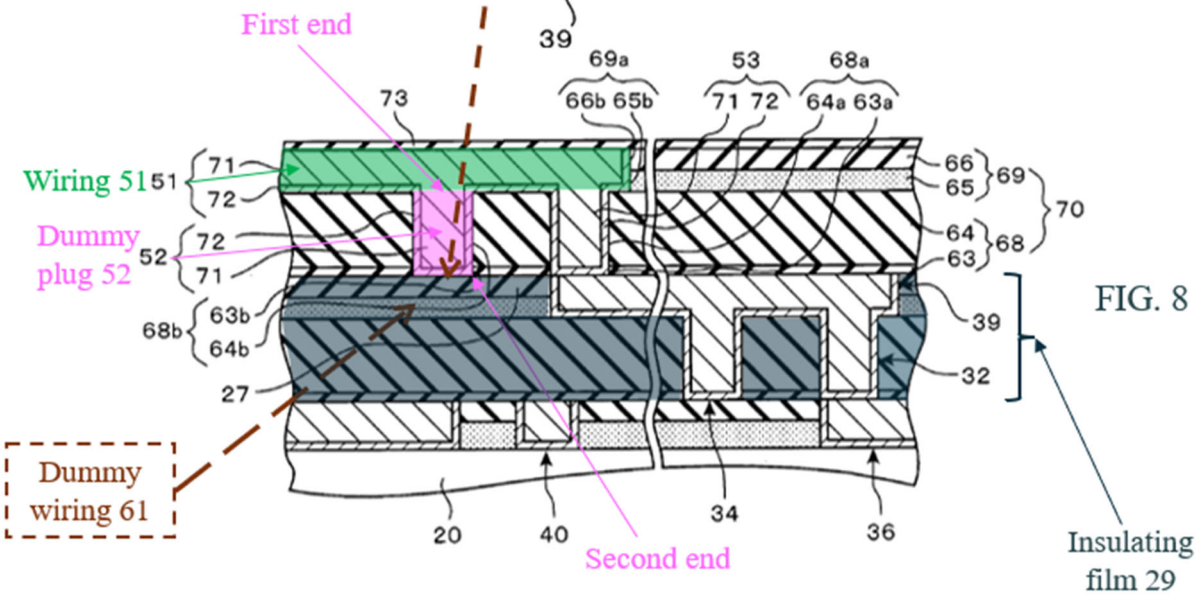


FIG. 8

TSMC-1004, Figs. 8-9; TSMC-1003, ¶¶240-41.

B. Ground 2: Claims 4 and 8 Are Obvious Over Watanabe and Kurashima

Watanabe and Kurashima render claims 4 and 8 obvious. TSMC-1003, ¶¶242-60.

1. Kurashima

Because Kurashima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g.,

interconnect reliability), Kurashima is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1011, 1:15-22, 1:49-67; TSMC-1003, ¶¶94-95.

Kurashima enhances durability of insulating films, particularly low-relative-dielectric-constant films, against CMP-related stresses to prevent film peeling. TSMC-1011, 1:15-22, 1:49-67. Kurashima teaches forming in parallel Cu-wire 9 and Cu-dummy wire 10 in insulating film 4. *Id*., 4:50-6:32, Figs. 1B-1D, 3A-3B. Then a second-layer Cu-wire 16 is formed connecting to first-layer Cu-wire 9. *Id*., 6:58-8:35, Figs. 2A-3A. Concurrently, a second-layer Cu-dummy wire 17 is formed in contact with first-layer Cu-dummy wire 10, providing a reinforcing effect and enhancing interfacial adhesion and CMP durability, to reduce peeling of layers. *Id*., 6:11-32; 6:58-8:54, 9:16-23, Figs. 2C, 3A. Kurashima teaches forming functional wires and dummy wires with substantially the same width within the same layer:

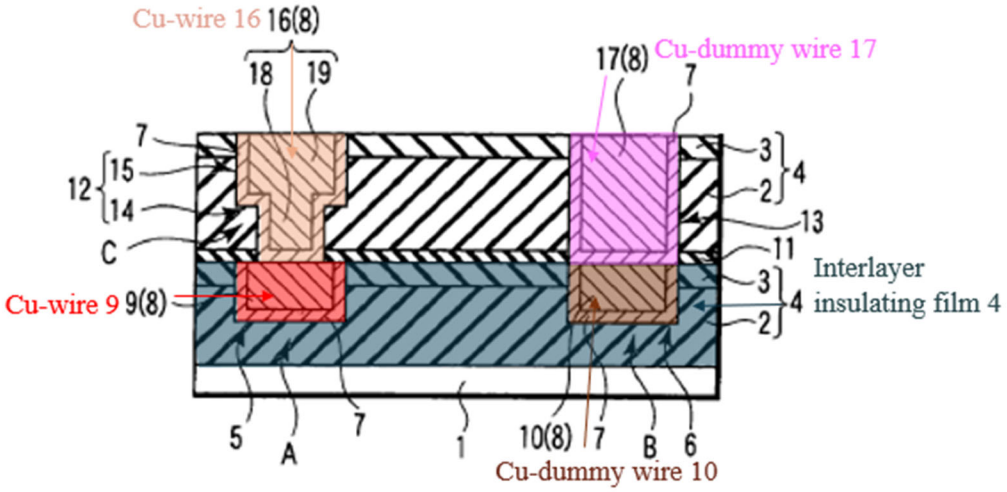
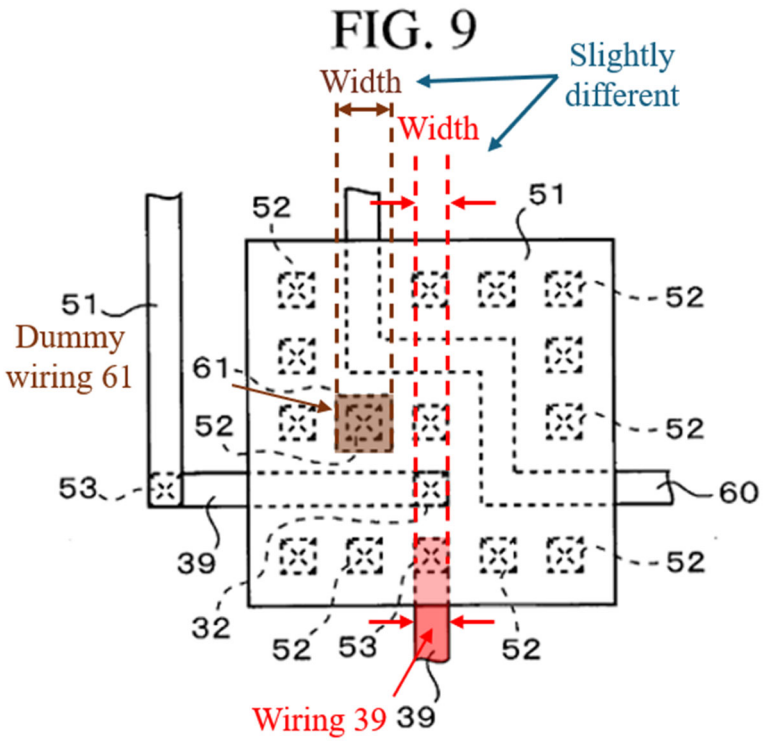


FIG. 3A

Id., 4:50-63, Figs. 1D, 3A-3B; TSMC-1003, ¶94.

2. Claim 4

In Watanabe's fifth embodiment, Figure 9 discloses dummy wiring 61 ("first dummy interconnect") with a slightly larger width than wiring 39 ("first interconnect"):



TSMC-1004, ¶[0127], Fig. 9; TSMC-1003, ¶¶243-44.

Kurashima teaches a functional wire ("Cu-wire 9" and "TaN-film 7," collectively "Cu-wire 9") and a dummy wire ("Cu-dummy wire 10" and "TaN-film 7," collectively "Cu-dummy wire 10") with substantially equal widths:

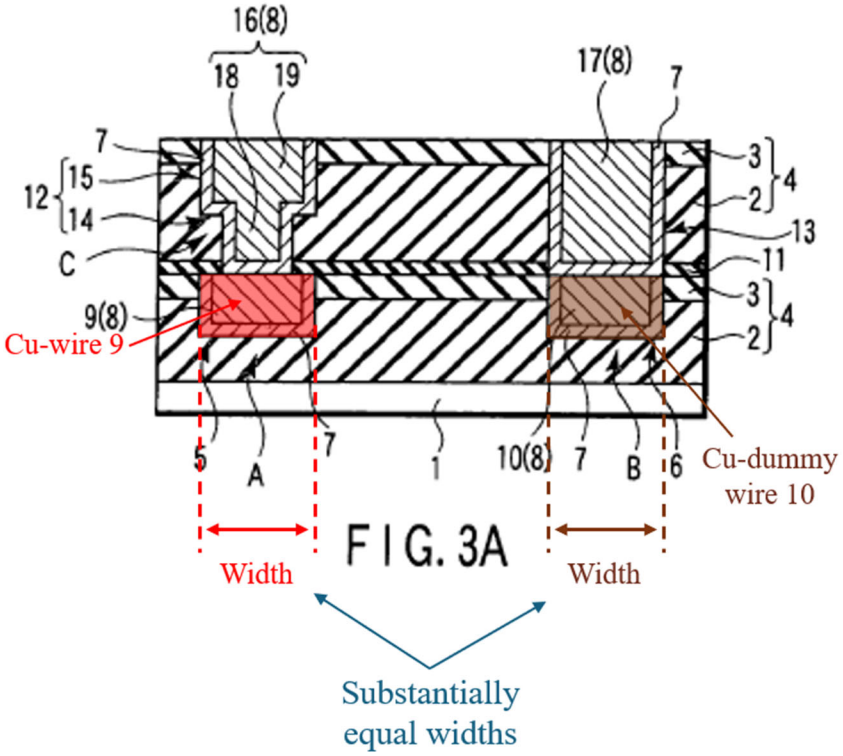
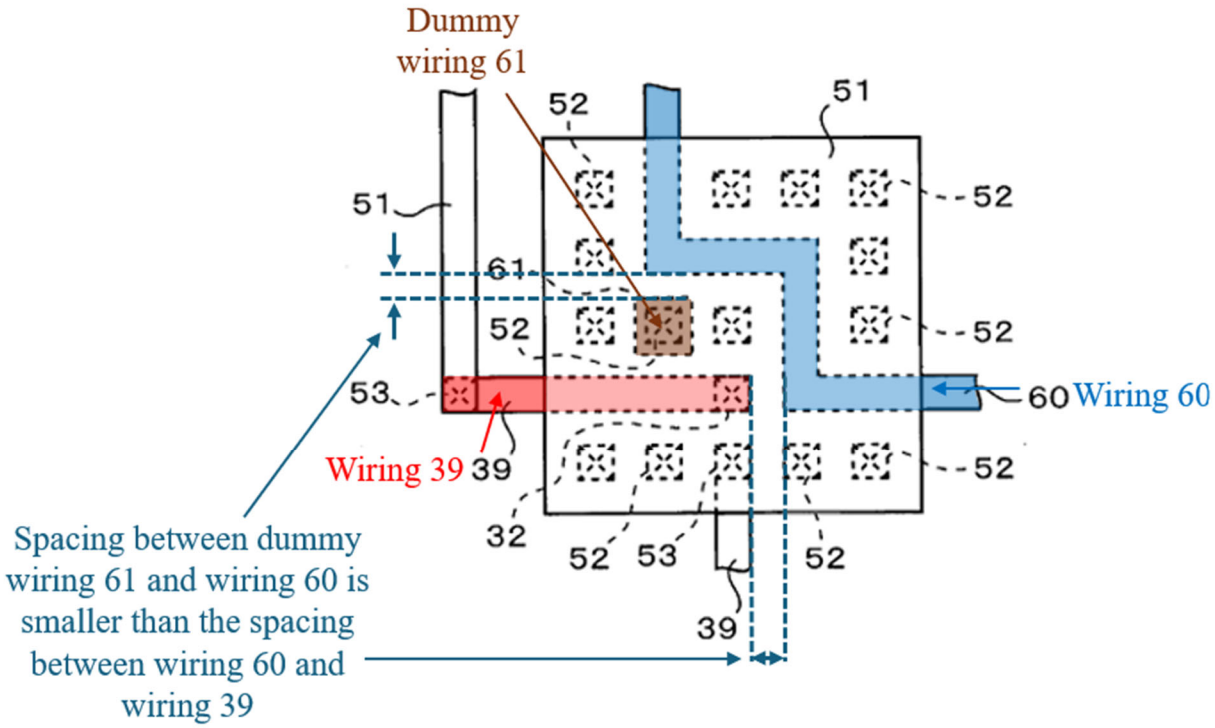


FIG. 3A

TSMC-1011, 4:38-41, 5:22-31, 7:57-8:3, Figs. 1D, 3A-3B; TSMC-1003, ¶¶245-46.

Kurashima demonstrates that slightly adjusting Watanabe's dummy wiring 61 to have a width equal to wiring 39 was a known design choice; further, Kurashima teaches that dummy wire 10's width matching that of dummy plug 17 secures the connection between them. *See* TSMC-1011, 4:38-41, 5:22-31, 7:57-8:3, Figs. 1D, 3A-3B; TSMC-1003, ¶246. Reducing the width of dummy wiring 61 to match wiring 39's width would also beneficially increase the spacing between dummy wiring 61 (which is at the potential of wiring 51) and adjacent wiring 60 (which is at a different potential):

FIG. 9



TSMC-1004, ¶[0126]; TSMC-1003, ¶¶248-49. Making Watanabe's dummy wiring 61 the same width as the first-level interconnects (i.e., wirings 39 and 60) to matching the spacing between wirings 39 and 60 would reduce parasitic capacitance and crosstalk between dummy wiring 61 and wiring 60. TSMC-1004, ¶[0034]; TSMC-1003, ¶¶248-49. Because Watanabe's dummy plugs are the same width as wiring 60, dummy wiring 61 so-modified would have the same width as the dummy plug 52 it is connected to, thus ensuring a secure connection between dummy via/dummy interconnect as taught by Kurashima. TSMC-1003, ¶¶248-50.

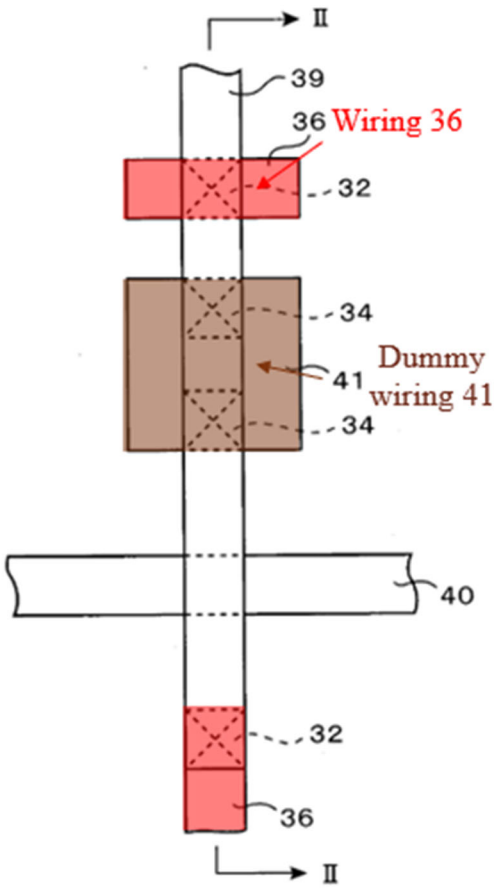
Modifying Watanabe's dummy interconnect to have substantially the same width as an adjacent first interconnect is just a simple substitution adopting

Kurashima's disclosed configuration, involving no criticality; a POSITA was motivated to adopt this configuration to reduce unwanted parasitic capacitances and crosstalk, and would have been able to easily achieve it by simply adjusting the device dimensions during manufacture. TSMC-1003, ¶¶247-51.

3. Claim 8

Watanabe's Figure 4 discloses a horizontally extending wiring 36 ("first interconnect") and a vertically extending wiring 36, both connected to wiring 39 ("second interconnect") through respective plugs 32 ("via"). TSMC-1004, Fig. 4. Watanabe thus exemplifies wiring that extends in various directions, sometimes as a single wiring (e.g., wiring 60 in Figure 9) and at other times as separate wires as with wirings 36 in Figure 4:

FIG. 4



TSMC-1003, ¶253.

Kurashima teaches Cu-dummy wire 10 (analogous to Watanabe's dummy wiring 61) having numerous shapes with one overall side longer than another to reduce CMP stress and the possibility of film peeling. TSMC-1011, 3:25-33, 6:11-32, 10:4-21, 10:58-67, 12:49-52; Figs. 3B, 6A, 6E, 6G, 6M. Kurashima's Fig. 6G discloses an exemplary shape for dummy wire 10 (TSMC-1003, ¶254):

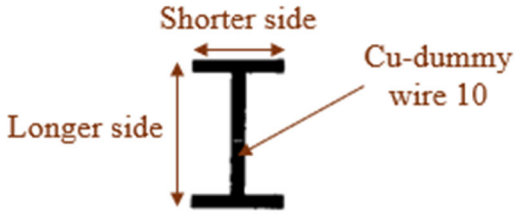


FIG. 6G

Some shapes (*see* Figures 3B, 6A, 6M) have an overall longer side from top to bottom, while other shapes (*see* Figures 7D, 7G-7H, 8C, 9C) have an overall longer side from left to right. *See id*., Figs. 3B, 6-9; TSMC-1003, ¶255. Similarly, if the "longer side" of the dummy wire is simply considered to be the direction orthogonal to its width, Kurashima's dummy wires have "longer sides" running both up-down and side-to-side. TSMC-1003, ¶255. Under either reading, Kurashima's Figure 6 teaches dummy interconnect patterns having "longer sides" in both orthogonal directions (i.e., top-to-bottom and side-to-side). *Id*.

It was obvious to extend Watanabe's dummy wiring 41 in one direction or another (i.e., other than a square) based on Kurashima's teaching of a multitude of beneficial dummy wiring designs such as Figure 6G above. Implementing one of these known shapes for Watanabe's dummy wiring 41 results in a longer side of dummy wiring 41 forming a right angle with a longer side of **one of** wirings 36 ("first interconnect"), as illustrated below:

FIG. 4

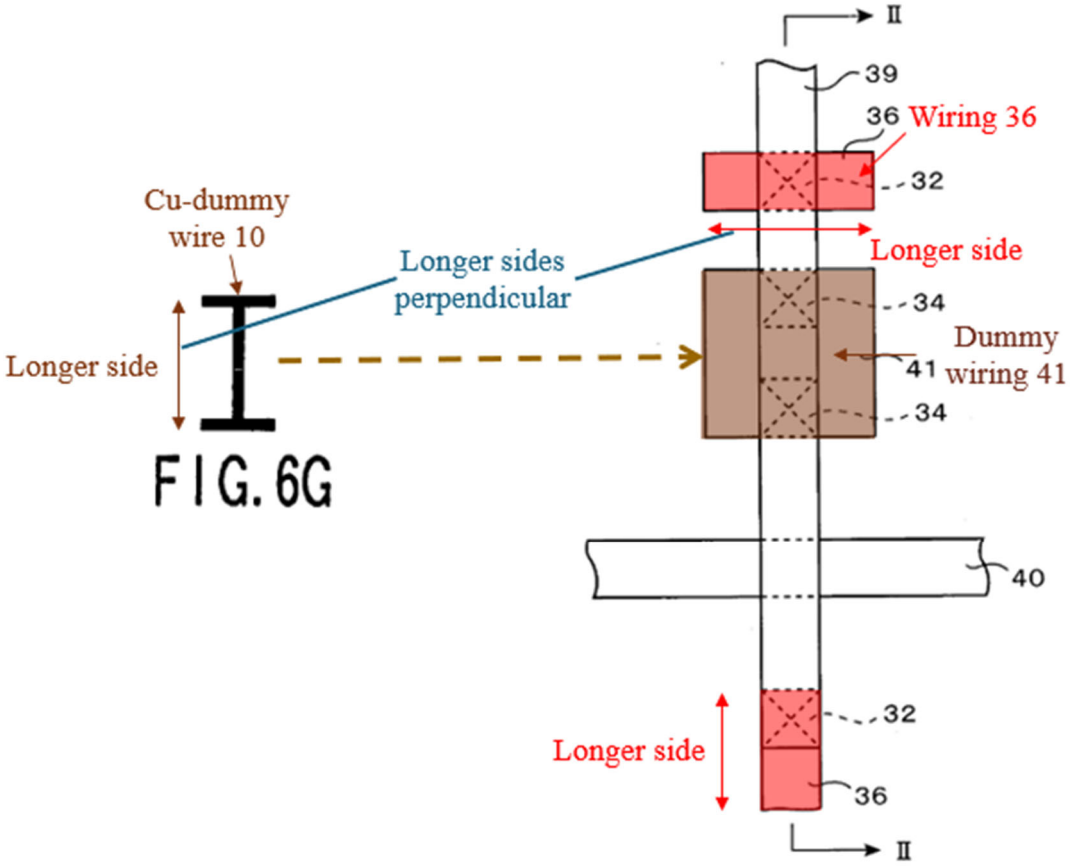


FIG. 6G

TSMC-1003, ¶¶256-57.

A POSITA was motivated to adopt Kurashima's dummy interconnect shapes because they can better bear and dissipate larger stresses from CMP. TSMC-1011, 10:4-21, 10:58-67; TSMC-1003, ¶258. A POSITA appreciated that utilizing Kurashima's dummy wiring shapes for Watanabe's dummy wiring 41 would better alleviate/dissipate CMP stresses placed on the dummy wiring and insulating film 23 in which it is formed. TSMC-1003, ¶258.

Moreover, because Kurashima teaches that the dummy wiring shape (i.e., ones having various "longer side" orientations) impacts device reliability and manufacturability (TSMC-1011, 3:25-33, 6:11-32; 10:4-21, 10:58-67, 12:49-52; Figs. 3B, 6A, 6E, 6G, 6M), it would have been routine optimization for a POSITA to determine the optimal orientation and longer-side dimension of Watanabe's dummy wirings 41 (Figure 4) and 61 (Figure 9) relative to the lower-level interconnect direction. TSMC-1003, ¶259.

A POSITA would have expected success in implementing such interconnect shapes, because extending Watanabe's dummy wiring 61 in one direction or another as shown by Kurashima involved a mere design choice that could be readily implemented with Watanabe's existing manufacturing process. *Id*., ¶260. Implementing such interconnect shapes and orientations merely required that the trenches defining such interconnects be patterned as desired, which was easily accomplished with standard techniques at the time. *Id*.

C. Ground 3: Claims 9 and 17-18 Are Obvious Over Watanabe and Iizuka

Watanabe and Iizuka render claims 9 and 17-18 obvious. TSMC-1003, ¶¶261-82.

1. Iizuka

Because Iizuka is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g.,

interconnect reliability), Iizuka is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1008, 1:7-14; 2:39-45; TSMC-1003, ¶¶96-98.

Iizuka describes methods for manufacturing semiconductor devices, focused on improving the filling of small-diameter via holes to form reliable conductive plugs between interconnect layers. TSMC-1008, Abstract, 1:7-14, 2:39-45. Iizuka teaches common via-hole planar shapes: "the opening of the via-hole may have any configuration, such as a square, rectangle or **circle**." *Id*., 9:45-47; *see also id*., 6:60-63, Fig. 5A (disclosing "diameter" of via). Iizuka thus confirms that vias/dummy vias can have various planar shapes, and that selecting a specific shape (e.g., as between square and circular) was a simple design choice. TSMC-1008, 9:45-47; TSMC-1003, ¶¶265-67. Iizuka's description of via-hole 6 having a "diameter" (TSMC-1008, 6:60-63) similarly discloses a circular via shape, since the geometrical term "diameter" corresponds with circular shapes. TSMC-1003, ¶265. Circular via holes result in vias having substantially circular cross-sections. TSMC-1003, ¶¶96-97.

2. Claim 9

Watanabe discloses vias/dummy vias having circular cross-sections through its simulation model (TSMC-1004, ¶[0083]), and Iizuka further teaches that circular vias were a known, interchangeable design alternative to square vias (*supra*, §VI.C.1). TSMC-1003, ¶¶264-66.

Watanabe's dummy plugs 34/52 ("dummy via") have a smaller cross-sectional dimension than dummy wirings 41/61 ("first dummy interconnect") (TSMC-1004, ¶¶[0090]-[0091], [0127], Figs. 2, 4, 9), such that the diameter of a circular dummy via in Watanabe will be smaller than the dummy interconnect width. *Id*.; TSMC-1003, ¶¶272-74. It was thus obvious to incorporate circular dummy vias having a diameter smaller than the width of the dummy interconnect into Watanabe's device. *Infra*, §VI.C.5; TSMC-1003, ¶¶266-71, 274-75.

3. Claim 17

Watanabe discloses vias (conductive plugs 32) and dummy vias (dummy plugs 34) (*supra*, §§VI.A.2.(a).(6)-(7), VI.A.2.(b)-(d)), and both Watanabe and Iizuka teach that such vias can be circular in cross-section (*supra*, §§VI.C.1-2). TSMC-1003, ¶¶276-278. Thus, it was obvious to incorporate circular vias and dummy vias into Watanabe's device. *Infra*, §VI.C.5; TSMC-1003, ¶¶276-78.

4. Claim 18

Watanabe's simulation model assigns identical diameters (0.15 μm) to both its vias (e.g., conductive plug 32) and dummy vias (e.g., dummy plug 34). TSMC-1004, ¶[0083]; TSMC-1003, ¶280. Thus, in implementing Watanabe's vias/dummy vias with circular cross sections (as rendered obvious by Iizuka), it would have been further obvious to make their diameters substantially equal, as taught by Watanabe's own modeling parameters. TSMC-1003, ¶¶279-82.

This choice would have been motivated by simple design choice, design simplicity, process commonality for etching and filling these features, and to ensure consistent relative behavior as between the via and dummy via, for example with respect to the effects on mechanical properties. *Id*., ¶281.

The expectation of success in implementing vias and dummy vias with substantially equal diameters would be high, as Watanabe's own simulation model demonstrates this configuration, and Watanabe consistently discloses same-sized vias and dummy vias. *Id*., ¶282. A POSITA would simply have specified the vias and dummy vias as having the same size, and the standard manufacturing process would build them as such. *Id*.

5. Combination of Watanabe and Iizuka

Watanabe's simulation model describes its vias and dummy vias as "circular cylinders," thereby disclosing vias having circular cross-sections as alternatives to the square vias in Watanabe's figures. TSMC-1004, ¶[0083]; *supra*, §§VI.C.1-2. Iizuka's teaching that vias can be circular, square, or rectangular confirms that a POSITA would have viewed these shapes as a finite number of readily interchangeable design choices given Iizuka's express teaching to this effect and a POSITA's general understanding. TSMC-1008, 9:45-47; TSMC-1003, ¶¶265-66.

The motivation to use circular vias, as known from Iizuka and general practice, includes advantages in manufacturing process control (e.g., more uniform

etching and filling for circular shapes compared to sharp-cornered squares), more favorable stress distribution around circular openings, design simplicity, and consistency with Watanabe's own models. TSMC-1003, ¶¶267-68; TSMC-1038, 7:61-67.

A POSITA would have recognized that neither the fundamental stress-relieving function of Watanabe's dummy vias, nor the electrical-connection function of Watanabe's functional vias, would be materially altered by adopting a circular cross-section. TSMC-1003, ¶¶268-69. The '623 patent also does not teach any criticality to the via/dummy via shape. *Id.*, ¶270; *see also* TSMC-1002, 292-96 (Examiner noting no criticality for via shapes).

A POSITA would have expected success in implementing Watanabe's vias and dummy vias with circular shapes. *Id*., ¶¶271, 275. Circular vias were standard in the industry, and Iizuka teaches methods for successfully filling small-diameter via holes. *Id*. The choice of via shape as a routine design parameter, subject to routine optimization as noted by the Examiner during prosecution (TSMC-1002, 244-45, 292-96), and modifying Watanabe's square vias (or implementing its modeled circular vias) to be circular would have been readily achievable using known fabrication techniques. TSMC-1003, ¶¶271, 275.

D. Ground 4: Claims 45-47 Are Obvious Over Watanabe and Kamoshima

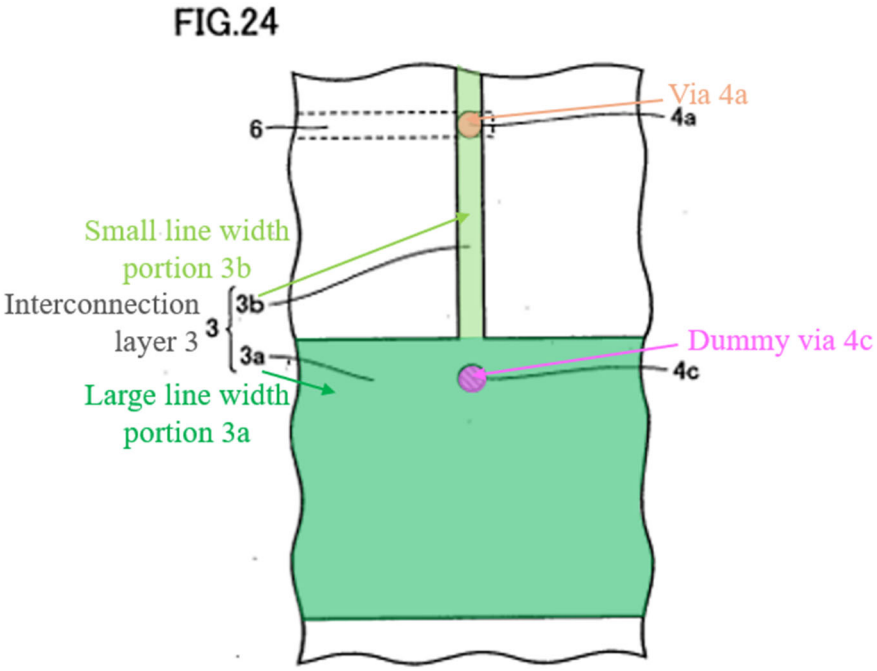
Watanabe and Kamoshima render claims 45-47 obvious. TSMC-1003, ¶¶283-307.

1. Kamoshima

Because Kamoshima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Kamoshima is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1009, ¶¶[0002], [0004]-[0007]; TSMC-1003, ¶¶99-102.

Kamoshima discloses interconnection structures that "suppress concentration of voids in an interconnection under a via due to stress migration." TSMC-1009, ¶¶[0002], [0008]. Kamoshima uses dummy vias so that microvoids are distributed between a via and dummy via, thereby suppressing concentration of microvoids under the via. TSMC-1009, ¶¶[0088], [0097]-[0098].

Interconnection layer 3 can have different shapes, including having a constant width (Figure 15), and having an interconnection portion with a small line width 3b branching off an interconnection portion with a large line width 3a (Figures 23-27). *Id.*, ¶¶[0094]-[0103], Figs. 23-27. Kamoshima teaches arranging via 4a along small line width portion 3b and dummy via 4c in the vicinity of a "connection portion" between interconnection portions 3a, 3b. *Id.*, ¶¶[0095], [0099].



Id., Fig. 24; TSMC-1003, ¶¶99-100.

2. Claim 45

a) [45.a]

Kamoshima discloses an interconnection layer shape with large line width portion 3a and small line width portion 3b. TSMC-1009, ¶¶[0002], [0094]-[0103], Abstract, Figs. 23-27; TSMC-1003, ¶¶284-86. Moreover, Kamoshima teaches having via 4a in small line width portion 3b and dummy via 4c in the vicinity of "connection portion R" between interconnection portions 3a, 3b (*see* TSMC-1009, Figs. 23-24; TSMC-1003, ¶¶286-87):

FIG.23

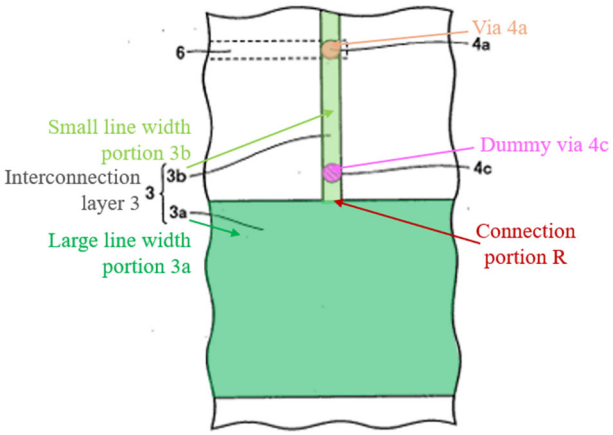
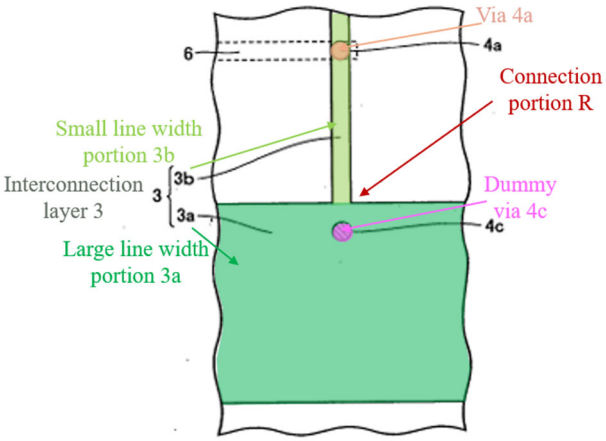


FIG.24



b) [45.b]

Watanabe's vias (conductive plugs 32, 53) and dummy vias (dummy plugs 34, 52) are connected to the second interconnect (wirings 39, 51):

FIG. 2

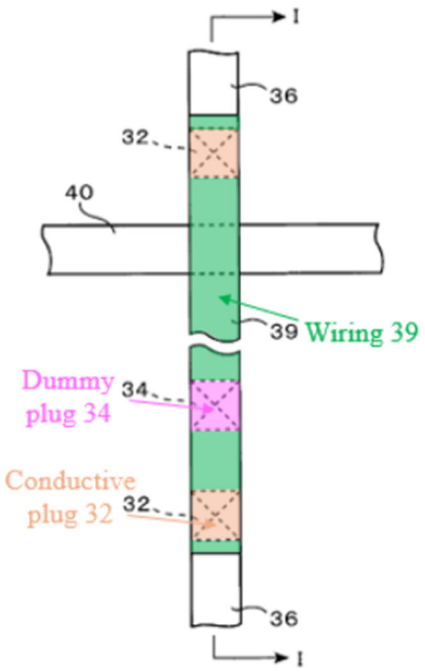
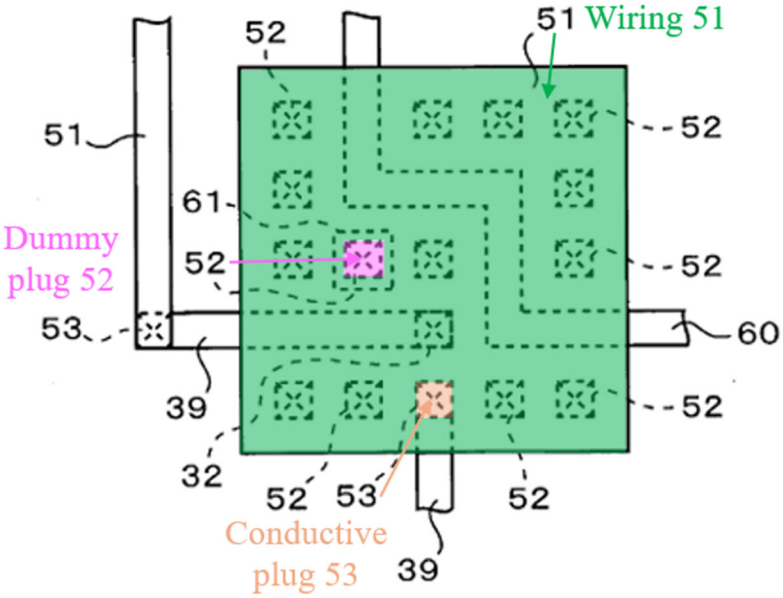
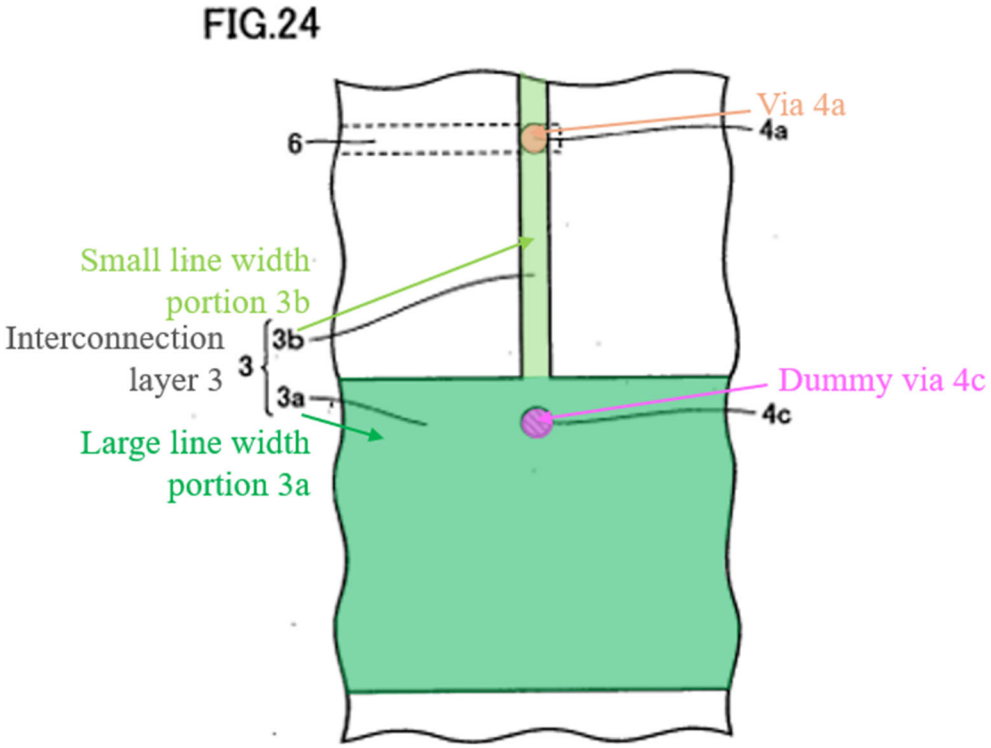


FIG. 9



TSMC-1004, ¶¶[0067]-[0073], [0118]-[0122], [0159]-[0165], Figs. 1-3, 8-9, 12J-12M; TSMC-1003, ¶289.

Kamoshima's via 4a and dummy via 4c are similarly connected to interconnection layer 3 (TSMC-1009, Figs. 23-24; *supra*, §VI.D.1; TSMC-1003, ¶290):



c) Combination of Watanabe and Kamoshima

Kamoshima motivates a POSITA to use an interconnection layer with large and small width portions, and positioning the via (for connection to another interconnect) along the small line width portion and dummy via in vicinity of the connection portion between these interconnect portions. TSMC-1003, ¶¶292-94. Such an interconnect configuration causes microvoids that would otherwise

distribute between the via and the dummy via to further concentrate under the dummy via before reaching the via. *Id*.; *see* TSMC-1009, ¶¶[0088], [0097]-[0099]. Kamoshima thus teaches a known design choice for suppressing microvoids. TSMC-1003, ¶294.

Following Kamoshima's teachings, a POSITA would update Watanabe's second interconnect 39, 51 to include a large line width portion and a small line width portion branched therefrom, analogous to Kamoshima's interconnection layer 3 from Figures 23-24. *Id*., ¶¶291-296. Watanabe's plug 32/53 would be connected to the small line width portion and dummy plug 34/52 would be connected to the large line width portion. *Id*. This branched interconnect shape further enhances the suppression of microvoids in addition to Watanabe's design in any of its first-to-third and fifth embodiments. *Id*.; *see also* TSMC-1033, ¶¶[0056]-[0057], [0112]-[0114]; TSMC-1037, 162-63, 165, Figs. 9, 14.

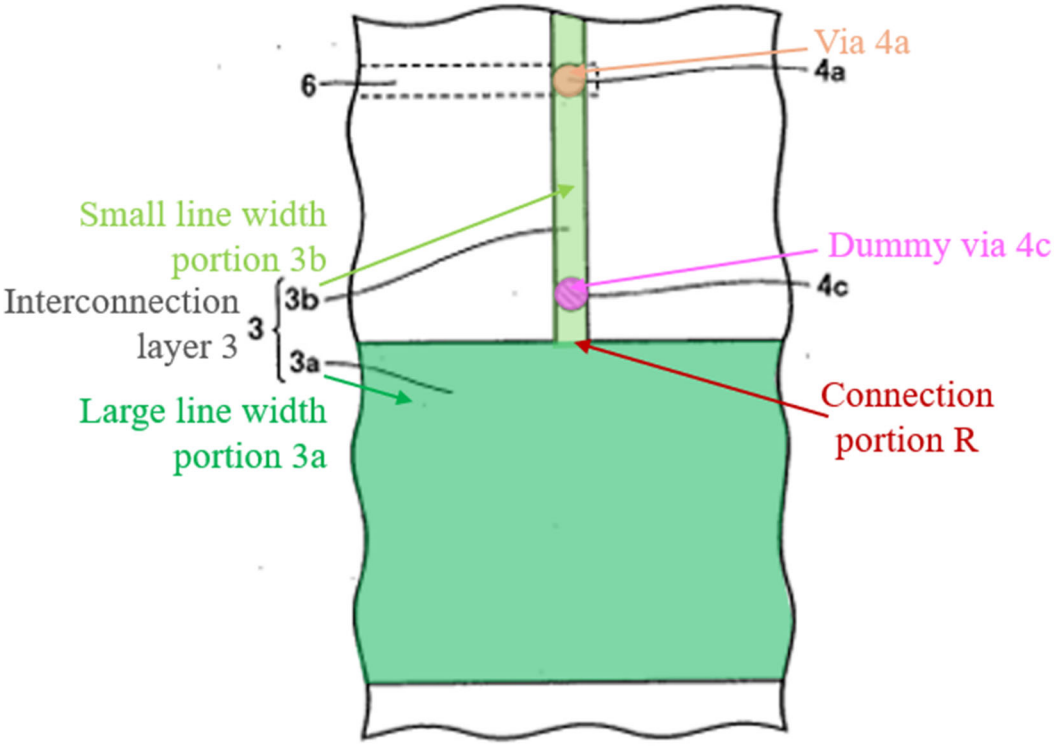
A POSITA would have expected success when modifying Watanabe in this manner. Both Watanabe and Kamoshima relate to forming an interconnect connected to both a via (to connect to another interconnect) and dummy via, where the dummy via is present to suppress voids from concentrating in the via. TSMC-1004, ¶¶[0012]-[0019], [0070]-[0073], [0075], [0117]-[0122], Figs. 1-5C, 8-9; TSMC-1009, ¶¶[0085]-[0086], [0088], [0094]-[0099], Figs. 15-16, 23-27; TSMC-1003, ¶¶297-98. The modification would be readily achieved with Watanabe's

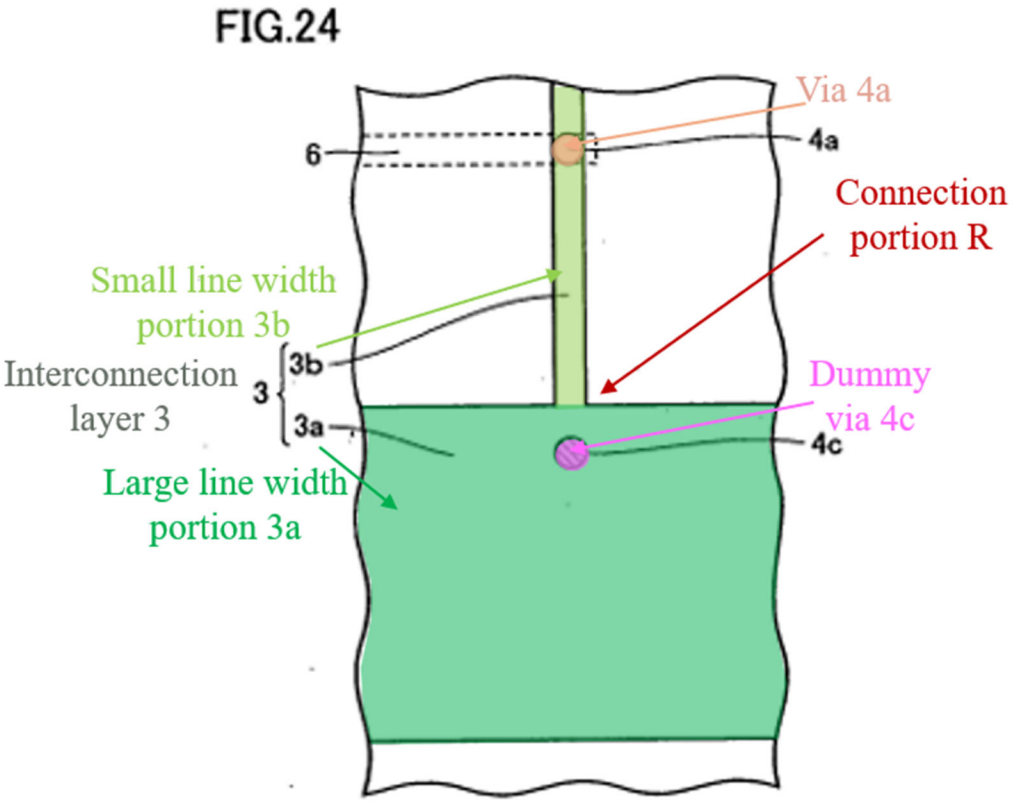
manufacturing process by using appropriate trench portion widths/shapes. TSMC-1003, ¶¶297-98.

3. Claim 46

Kamoshima teaches placing dummy via 4c at or near the branch point between first and second interconnect portions 3a, 3b (e.g., "connection portion R"):

FIG.23





TSMC-1009, ¶¶[0094]-[0095], [0099], Figs. 23-24; TSMC-1003, ¶¶299-300.

It was obvious to combine these teachings of Kamoshima and Watanabe for the reasons discussed above. *Supra*, §VI.D.2.(c); TSMC-1003, ¶¶301-03.

4. Claim 47

Kamoshima describes interconnection portion 3b as having "a small line width." TSMC-1009, ¶[0095]; Figs. 23-24; TSMC-1003, ¶305. Watanabe discloses vias (e.g., plugs 32) simulated as having a 0.15 μm diameter, and that their interconnects (e.g., wires 36, 39) could have the same widths. TSMC-1004, ¶[0083], Figs. 2, 4-5, 9; TSMC-1003, ¶305. Interconnect line widths of "0.2 μm or

less" are a routine design parameter for interconnects, e.g., Hasunuma teaches 0.13 μm for interconnect and via widths. TSMC-1005, ¶[0127]; TSMC-1003, ¶305.

Given Watanabe's teaching of 0.15 μm plugs ("vias"), and shown to match the width of interconnects (e.g. Figs. 2, 4), it was obvious to implement the small-line-width portion accordingly. TSMC-1003, ¶¶304-07; *see also* TSMC-1033, ¶¶[0056]-[0057], [0112]-[0114].

A POSITA would have expected success, because modifying Watanabe's interconnect shape and having the stated line width was well within the capabilities of a POSITA, and readily achieved with Watanabe's existing manufacturing process. TSMC-1003, ¶307; *see also* TSMC-1005, ¶[0127] (disclosing wiring layer widths of 0.13 μm).

E. Ground 5: Hasunuma Anticipates Claims 1, 11-15, 17-18, 21-22, 25-26, 28, 32, and 39-40

Hasunuma anticipates claims 1, 11-15, 17-18, 21-22, 25-26, 28, 32, and 39-40. TSMC-1003, ¶¶308-97.

1. Hasunuma

Because Hasunuma is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Hasunuma is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1005, ¶¶[0003], [0005]-[0006], [0079]-[0088]; TSMC-1003, ¶¶78-82.

Hasunuma addresses reliability problems arising from stresses inherent in interconnect structures. TSMC-1005, ¶¶[0079]-[0086]. Like the '623 patent, Hasunuma's solution for mitigating stress-related problems involves incorporating non-functional, concurrently formed dummy vias ("reinforcing plugs 28") extending from a second interconnect ("conductive layer 26") that is separately connected to a first interconnect ("conductive layer 14") by a functional via ("conductive plug 27") formed through a first insulating film (e.g., films 3, 4, 2), as exemplified in Figure 8:

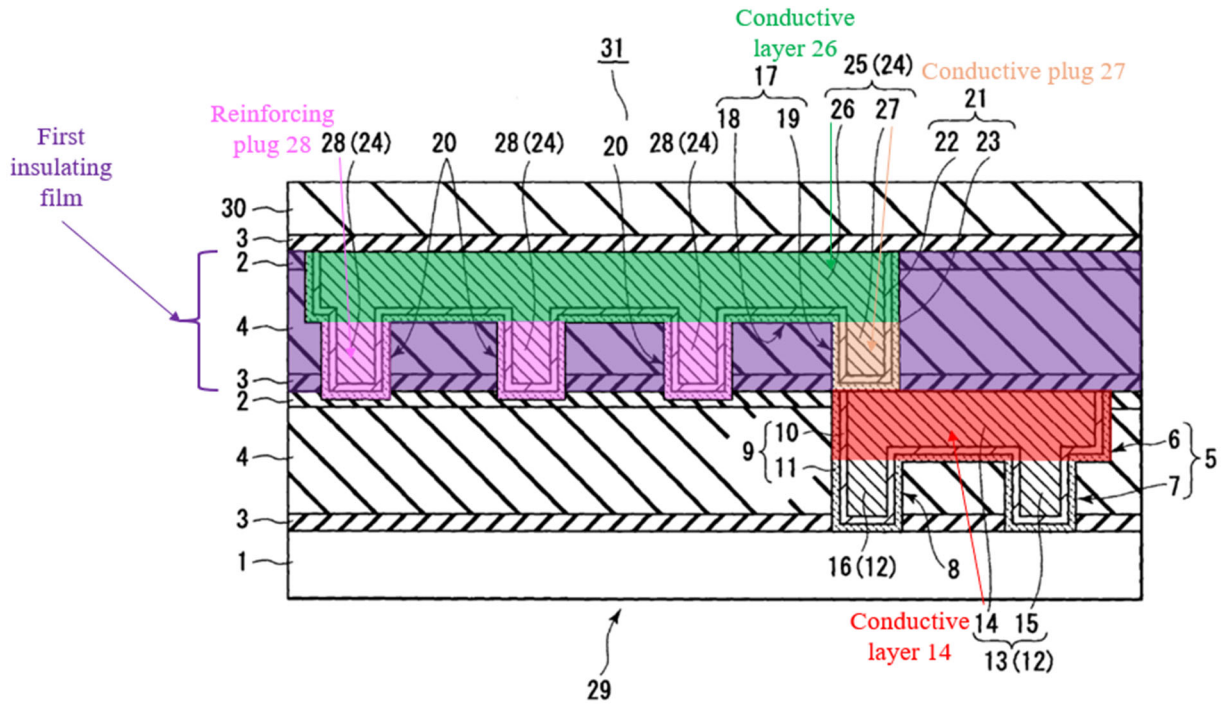


FIG. 8

Id., ¶¶[0090]-[0111]; *see also id*. Fig. 14 (same); TSMC-1003, ¶¶78-81. Hasunuma forms these structures using a dual damascene process that is repeated for each interconnect-plus-via level. TSMC-1005, ¶[0103].

2. Claim 1

a) [1.pre]

Hasunuma's Figure 8[5] discloses semiconductor device 31. TSMC-1005, Abstract, ¶¶[0021], [0111]; TSMC-1003, ¶¶309-10.

b) [1.a]

Hasunuma's Figure 8 discloses silicon substrate 1 (i.e., a "semiconductor substrate"). TSMC-1005, ¶[0090], Figs. 1A-8; TSMC-1003, ¶¶311-12.

c) [1.b]

Hasunuma discloses a first interconnect (e.g., "Cu conductive layer 14" and "barrier layer 9," hereinafter collectively "conductive layer 14" or "first interconnect") formed on the semiconductor substrate. TSMC-1005, ¶¶[0095], [0098], Figs. 3A, 8. Conductive layer 14 is formed within an insulating film deposited over substrate 1:

[5] Hasunuma's Figure 14 embodiment meets the challenged claims just like the first embodiment that includes Figure 8. TSMC-1003, ¶310 n.6.

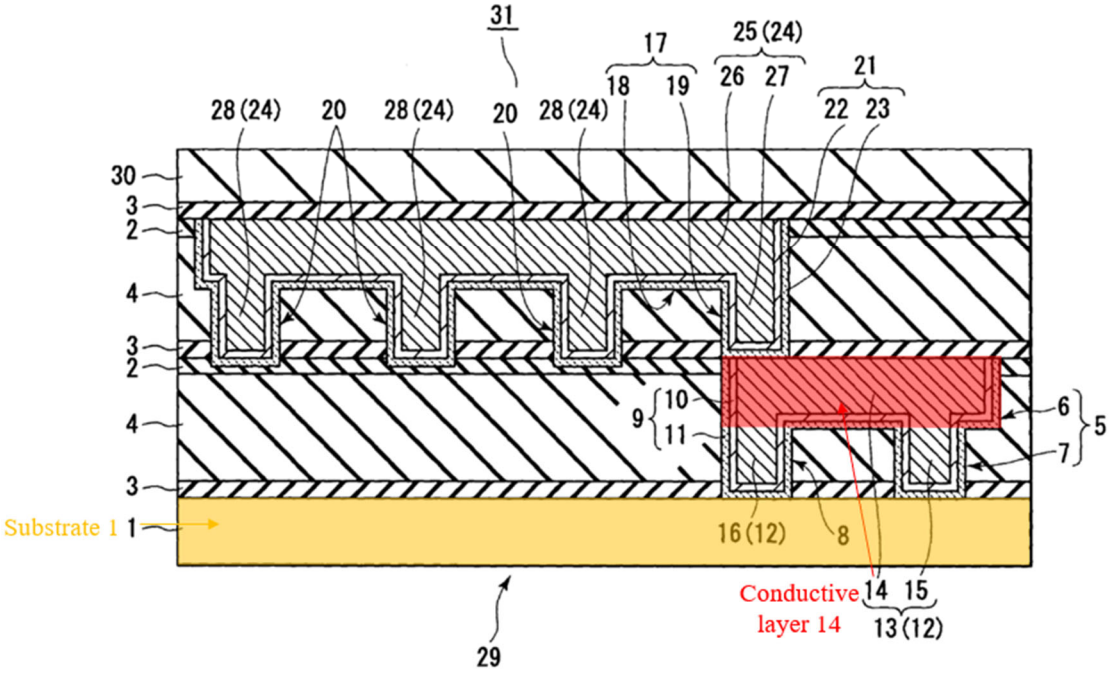


FIG. 8

TSMC-1003, ¶¶313-15.

d) [1.c]

Hasunuma discloses a first insulating film comprising insulating films 3, 4, and 2 stacked on the first interconnect:

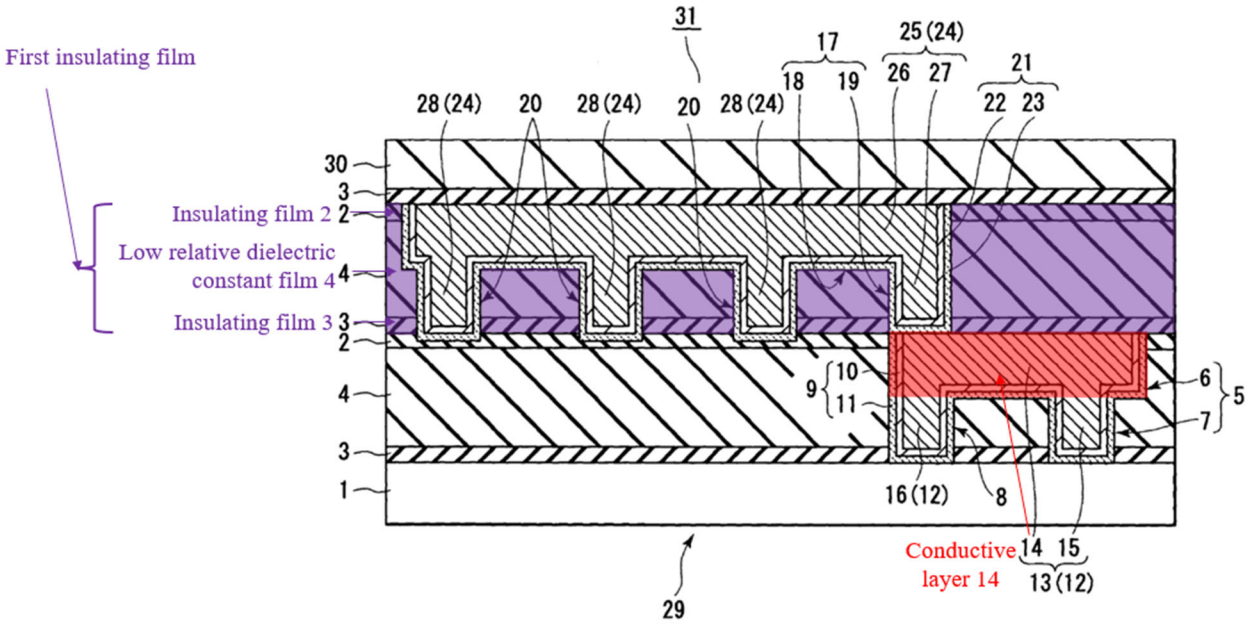


FIG. 8

TSMC-1005, ¶¶[0100], [0090]-[0091], Figs. 3A-8; TSMC-1003, ¶¶316-17. Either the combination of films 3, 4, and 2, or either or both of films 3 and 4, can constitute the "first insulating film." *Id.*, ¶318.

e) [1.d]

Hasunuma discloses a second interconnect, formed by filling recess 18 in the "first insulating film" with barrier metal film 21 and copper film 24 to form, collectively "conductive layer 26":

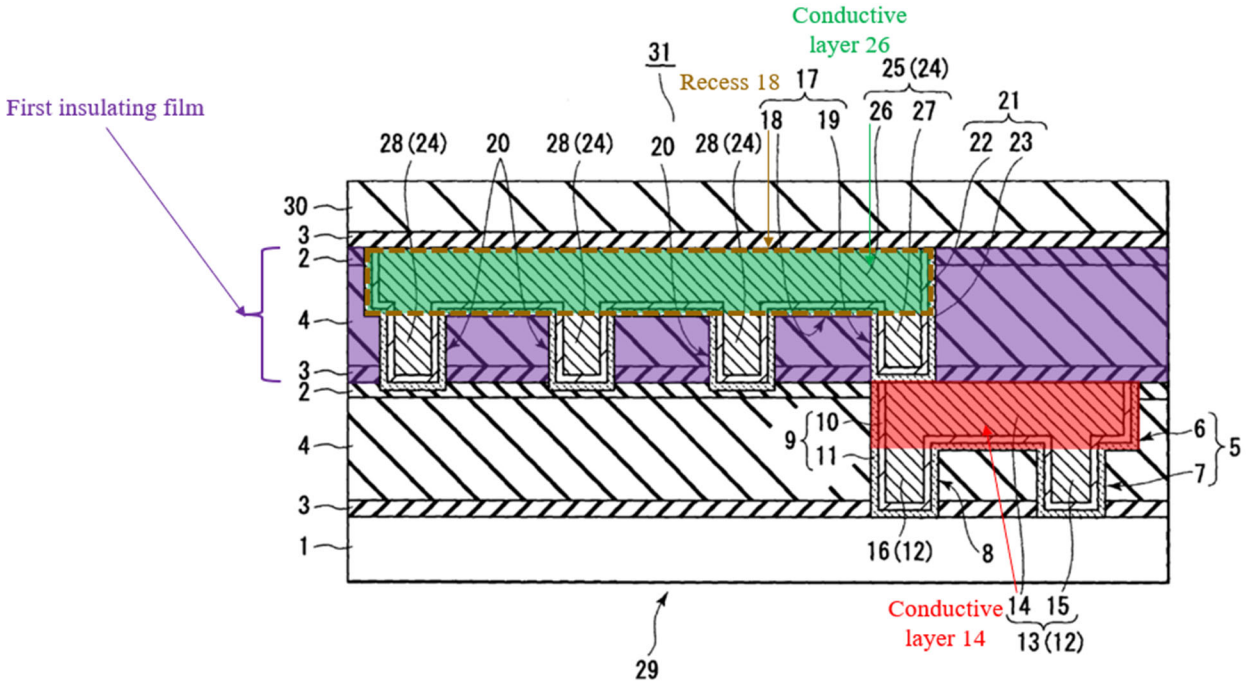


FIG. 8

TSMC-1005, ¶¶[0101], [0105]-[0108], [0110], Figs. 4-8; TSMC-1003, ¶¶319-20. The second interconnect is formed on the first insulating film, regardless of whether the first insulating film comprises all of insulating films 3, 4, and 2, or either or both of films 3 and 4. *Id.*, ¶321.

f) [1.e]

Hasunuma discloses a via, formed by filling recess 19 with barrier metal layer 21 and copper film 24 to form, collectively "conductive plug 27," that extends through the first insulating film from the second interconnect (conductive layer 26) to the first interconnect (conductive layer 14):

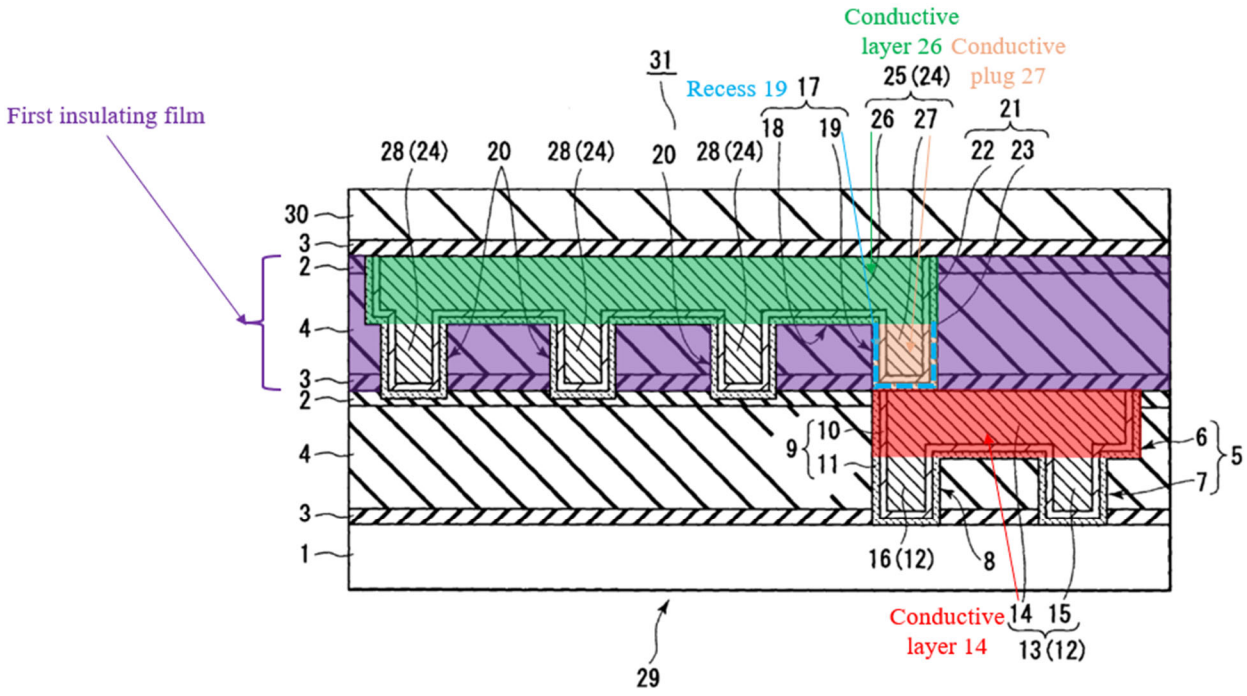


FIG. 8

TSMC-1005, ¶¶[0101]-[0103], [0105]-[0108], Figs. 4-8; TSMC-1003, ¶¶322-23. Conductive plug 27 connects the first and second interconnects through the first insulating film, regardless of whether insulating films 3, 4, and 2, or either or both of films 3 and 4, constitute the first insulating film. *Id*., ¶324.

g) [1.f]

Hasunuma discloses dummy vias, formed by filling recesses 20 with barrier metal film 21 and copper film 24 to form, collectively "reinforcing plugs 28," that extend from the second interconnect:

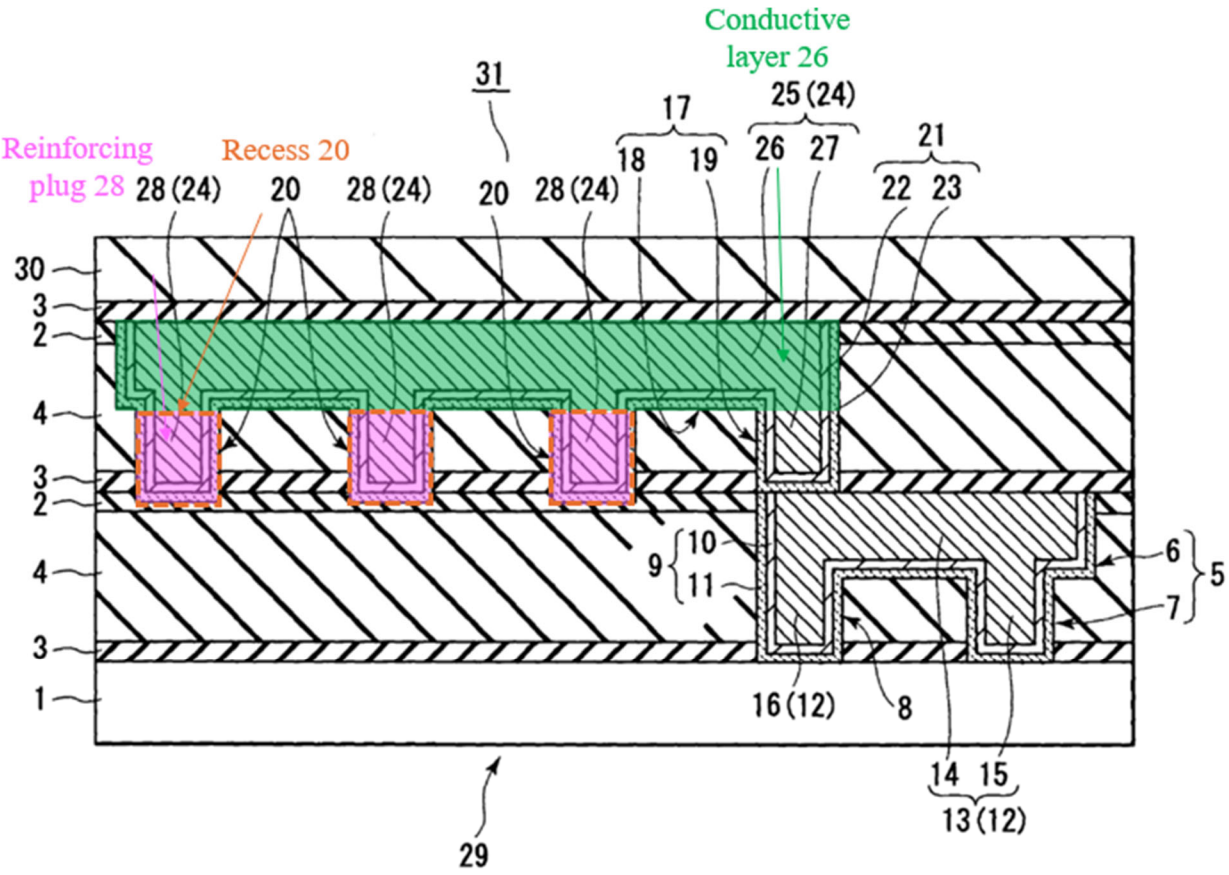


FIG. 8

TSMC-1005, ¶¶[0103]-[0108], Figs. 4-8; TSMC-1003, ¶¶325-29.

h) [1.g]

Hasunuma's dummy vias (reinforcing plugs 28) are formed from barrier metal film 21 and copper film 24 (*supra*, §VI.E.2.(g)), which are "conductive films." TSMC-1003, ¶¶330-31. The lower ends of reinforcing plugs 28 are connected only to insulating films 2 and 3, and Hasunuma explicitly describes reinforcing plug 28 as a non-functional "dummy plug (sacrifice plug)" which does not function as the wiring. TSMC-1005, ¶¶[0104], [0109], Fig. 8. Reinforcing

plugs 28 thus do not conduct current as part of active device operation, could be omitted from the structure without any impact on the device's circuit diagram, and are incapable of having current flow therethrough in the context of the device's operational circuitry. TSMC-1003, ¶¶332-37. Moreover, Hasunuma's device would still be operable if reinforcing plugs 28 were omitted, because current would still flow through the active circuit elements (i.e., conductive layers 14 and 26 and conductive plug 27) during actual use of the device. *Id.*

i) [1.h]/[1.i]

Hasunuma's wiring layer 25 (which comprises the second interconnect (conductive layer 26) and via (conductive plug 27)) is "formed in the dual damascene structure." TSMC-1005, ¶¶[0101], [0108]. Hasunuma's second interconnect (conductive layer 26) and dummy vias (reinforcing plugs 28) are similarly "formed in the dual damascene structure." *Id*., ¶[0103]; TSMC-1003, ¶¶338-39.

This is consistent with Hasunuma forming the second interconnect, via, and dummy vias integrally when recesses 18-20 are simultaneously filled with barrier metal film 21 and then copper film 24. TSMC-1005, ¶¶[0101], [0103], [0105]-[0109], Figs. 4-8. Thus, Hasunuma's second interconnect and via forms a dual damascene structure, as does its second interconnect and dummy vias:

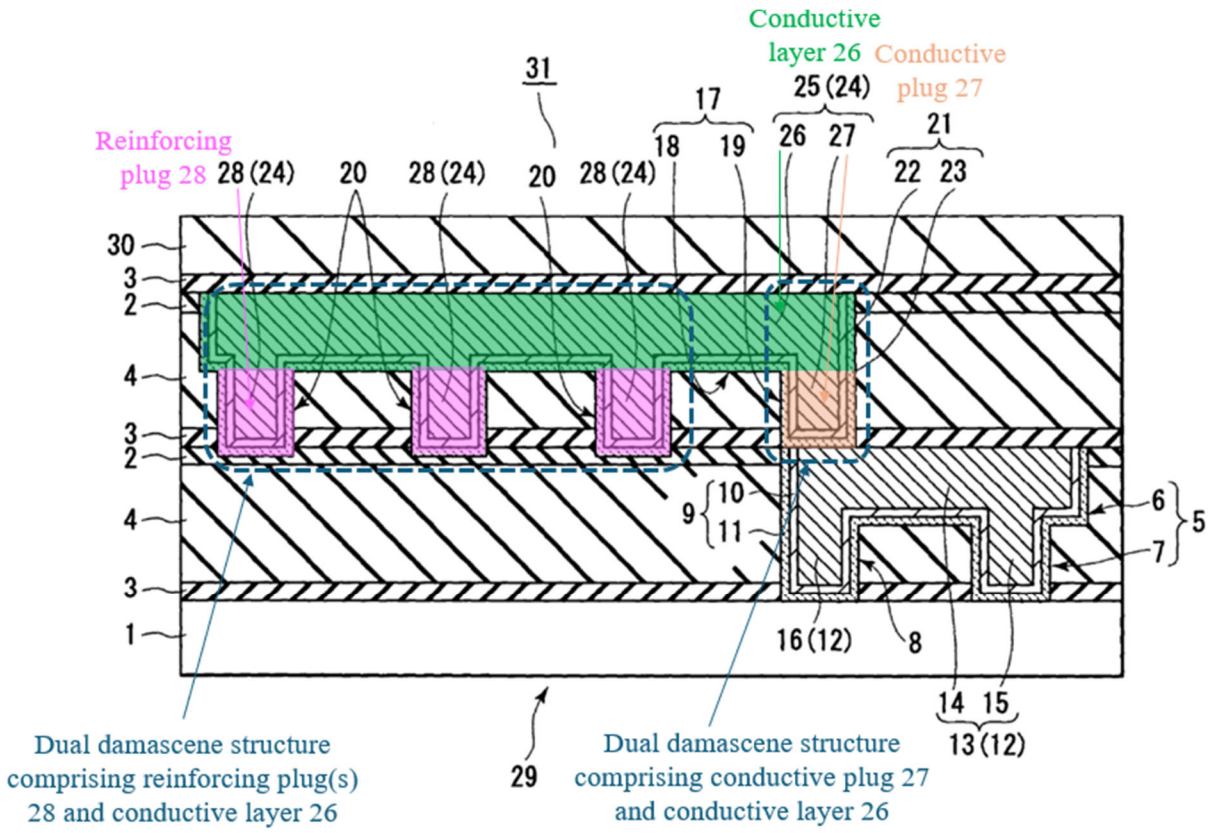


FIG. 8

TSMC-1003, ¶¶340.

3. Claim 11

Hasunuma teaches a first insulating film (e.g., combination of layers 3, 4, 2) having a SiN film and a SiO2 film. TSMC-1005, ¶[0299] ("instead of the SiC film 2, an **SiO_2 film** may also be used"; "instead of the SiCN film 3, an **SiN film** may also be used"); *see also id.*, ¶¶[0091]-[0092], [0100], [0293] (explaining that insulating films 2 and 3 can constitute SiO_2 and SiN films); TSMC-1003, ¶¶341-43.

4. Claim 12

Hasunuma's second interconnect (conductive layer 26) includes a first barrier film (e.g., "barrier metal film 21") and a first conductive film (e.g., "copper film 24"). *Supra*, §VI.E.2.(e); TSMC-1005, ¶¶[0105]-[0108], Figs. 4-8; TSMC-1003, ¶¶344-45.

5. Claim 13

The "first conductive film" corresponds to Hasunuma's copper film 24 (*supra*, §VI.E.4), which includes copper. TSMC-1003, ¶346.

6. Claim 14

Hasunuma's first interconnect (conductive layer 14) is formed on a semiconductor (silicon) substrate that includes active electronic circuits, where conductive plug 15 of the first interconnect secures "the conduction to the electronic circuit formed in the Si substrate 1." TSMC-1005, ¶¶[0091]-[0093], Fig. 3A; TSMC-1003, ¶¶347-49.

Hasunuma's second interconnect (conductive layer 26) is connected to the first interconnect by the via/conductive plug 27, and thus to the "electronic circuits." *Supra*, §VI.E.2.(f); TSMC-1003, ¶350. Furthermore, Hasunuma's second interconnect is part of a functional multi-level wiring scheme that creates a circuit by virtue of connection to other elements (e.g., other wiring layers, vias, or circuit components) or external electrodes (e.g., electrodes connected/bonded to Al

pad 136). *Id*.; TSMC-1005, ¶¶[0089], [0128], [0209]-[0212], [0298], Figs. 3A, 21A. Thus, Hasunuma's first and second interconnects are connected to other elements and/or external electrodes. TSMC-1003, ¶¶347-351.

7. Claim 15

a) [15.a]

As explained above (*supra*, §VI.E.6), Hasunuma's first and second interconnects (conductive layers 14 and 26) are connected to each other by via/conductive plug 27 and to other active elements within the semiconductor device such as "electronic circuits." TSMC-1005, ¶¶[0092]-[0093]; TSMC-1003, ¶¶348-53. A POSITA would have therefore understood that the structure comprising the via and the first and second interconnects constitutes part of a functional, closed electrical circuit in an operating semiconductor device. TSMC-1003, ¶¶354-56.

b) [15.b]

Hasunuma describes dummy via (reinforcing plug 28) as a non-functional "dummy plug (sacrifice plug)," which does not function as the wiring. TSMC-1005, ¶[0109], Fig. 8; TSMC-1003, ¶¶357-58. The top of reinforcing plug 28 connects to conductive layer 26 (second interconnect), but its bottom end terminates in an insulating material (e.g., films 2 and 3), without connecting to an underlying conductive path to complete a circuit. TSMC-1005, ¶¶[0104], [0109],

Fig. 8; TSMC-1003, ¶358. Because it does not function as wiring and does not complete a path for current flow between two distinct active points in an operational circuit, Hasunuma's dummy via does not constitute part of a closed circuit. *Supra*, §§VI.E.2.(g)-(h); TSMC-1003, ¶¶357-59.

8. Claim 17

Hasunuma discloses many via structures with circular plan views, for example in Figure 19A, which shows various dummy reinforcing plugs 125 and conductive plugs 27 as circular:

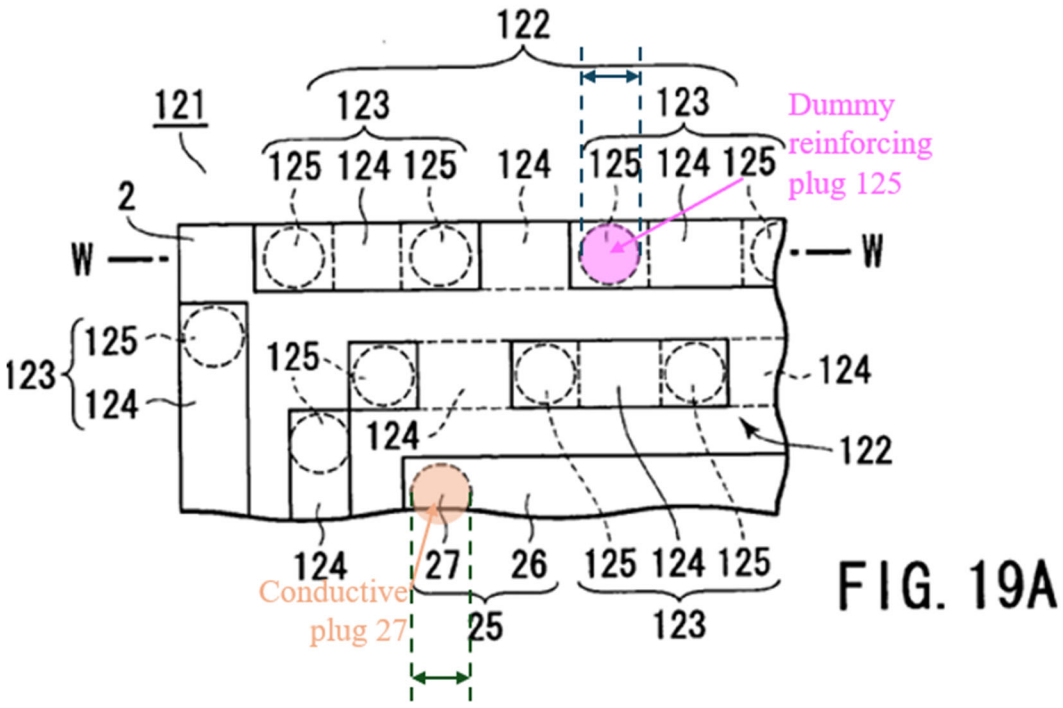


FIG. 19A

TSMC-1005, ¶[0200]; *see also id.*, Figs. 22A-22C, 24A-27C; TSMC-1003, ¶¶360-61.

Further, when describing tests performed on structures including Hasunuma's vias (conductive plugs 27) and dummy vias (reinforcing plugs 28), Hasunuma refers to their diameter: "each **diameter** of…conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 μm." TSMC-1005, ¶¶[0127], [0133], [0201], [0216], [0010]; TSMC-1003, ¶362.

Use of "diameter" in this context discloses a circular shape for both conductive plug 27 and reinforcing plug 28 (i.e., via and dummy via), since "diameter" is the standard dimensional term for circular features. TSMC-1003, ¶362. The express disclosure of circular vias in, *inter alia*, Figure 19A, reinforces that Hasunuma's reference to the "diameters" of its vias and dummy vias teaches structures likewise having a substantially circular cross section in plan view, just as shown in Figure 19A. *Id*., ¶¶362-64.

9. Claim 18

As noted for claim 17 above, Hasunuma expressly assigns the same dimension for the diameter of both its vias (conductive plugs 27) and its dummy vias (reinforcing plugs 28), stating: "each diameter of…conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 μm." TSMC-1005, ¶[0127]. Therefore, Hasunuma discloses circular vias and dummy vias having substantially the same diameter. TSMC-1003, ¶¶365-66.

10. Claim 21

Figure 8 discloses Hasunuma's first interconnect (e.g., "conductive layer 14") extends in a same direction as Hasunuma's second interconnect (e.g., "conductive layer 26"):

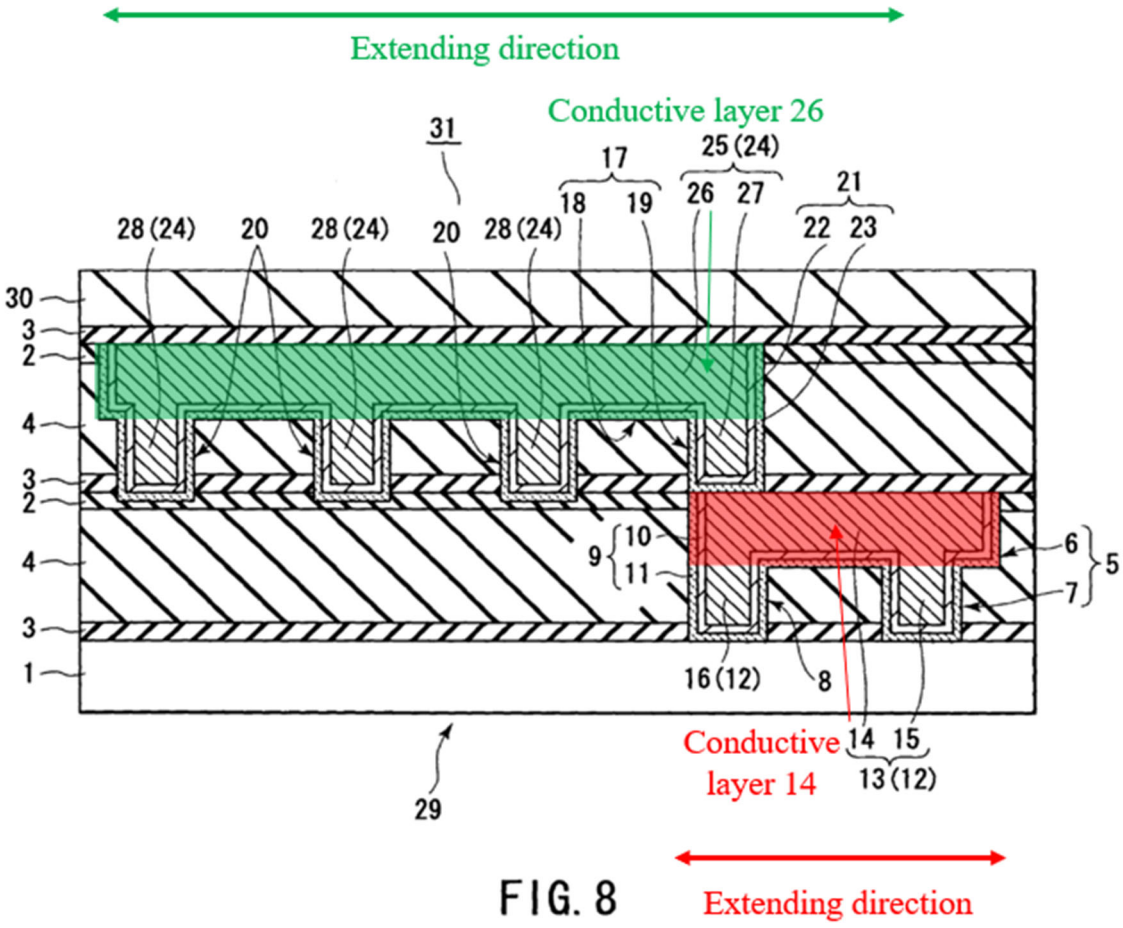


FIG. 8

TSMC-1003, ¶¶367-68. Hasunuma's interconnects are described as having identical widths matching the width of the vias (TSMC-1005, ¶[0127]; *see also* Fig. 14), such that Figure 8's first and second interconnects must extend across the

page in the same lengthwise direction. TSMC-1003, ¶¶369-71. Additionally, both interconnects extend in a same direction into/out of the page of Figure 8. *Id.*, ¶372.

11. Claim 22

Hasunuma's dummy via (e.g., reinforcing plug 28) is provided on an extended line along which the first interconnect (conductive layer 14) extends, as seen in Figure 8:

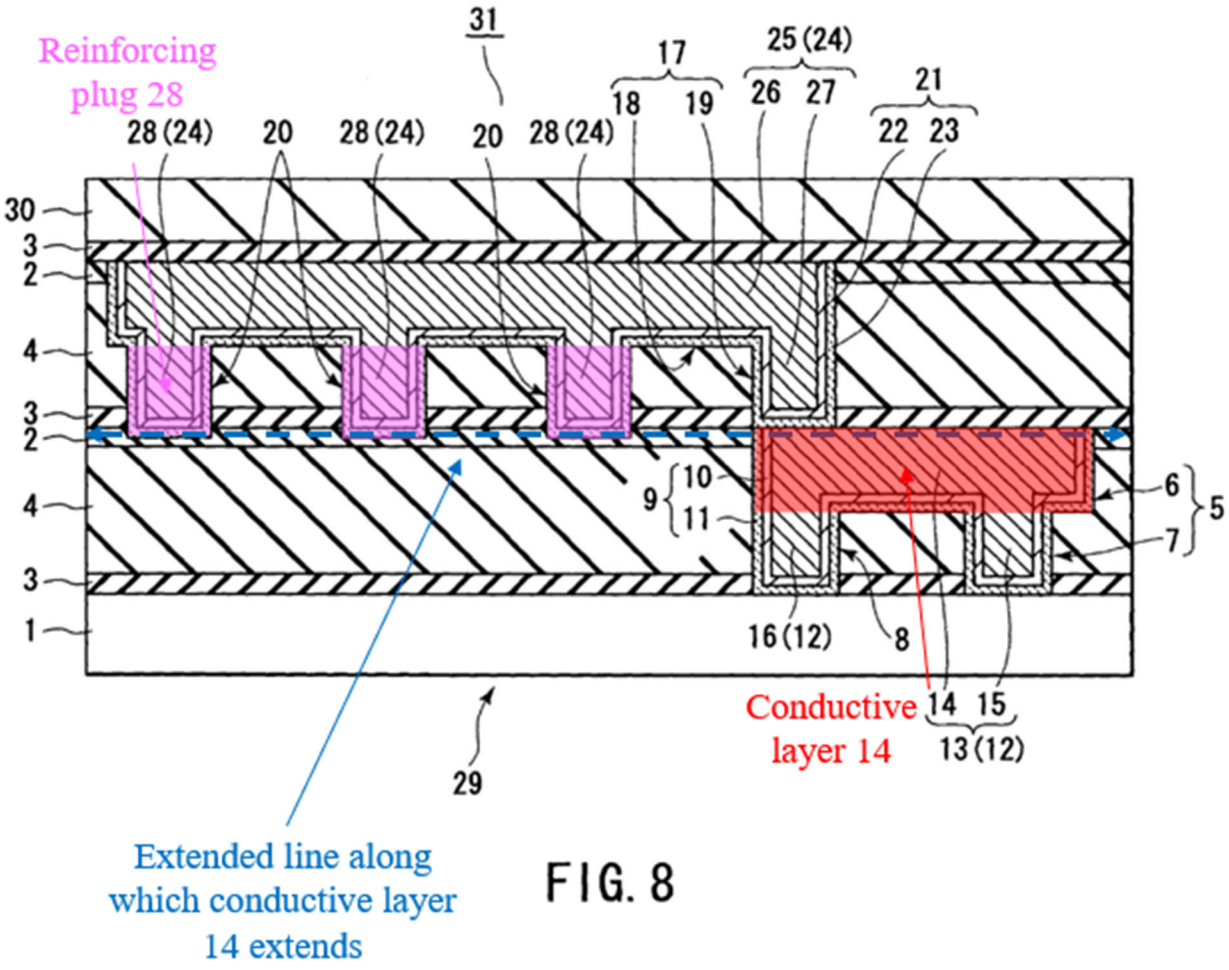


FIG. 8

TSMC-1003, ¶¶374-76.

12. Claim 25

Hasunuma's Figure 9[6] and Tables 1-3 provide values for the "Plug interval" between conductive plug 27 and an adjacent reinforcing plug 28, labeled as "B" and seen below in Figure 9:

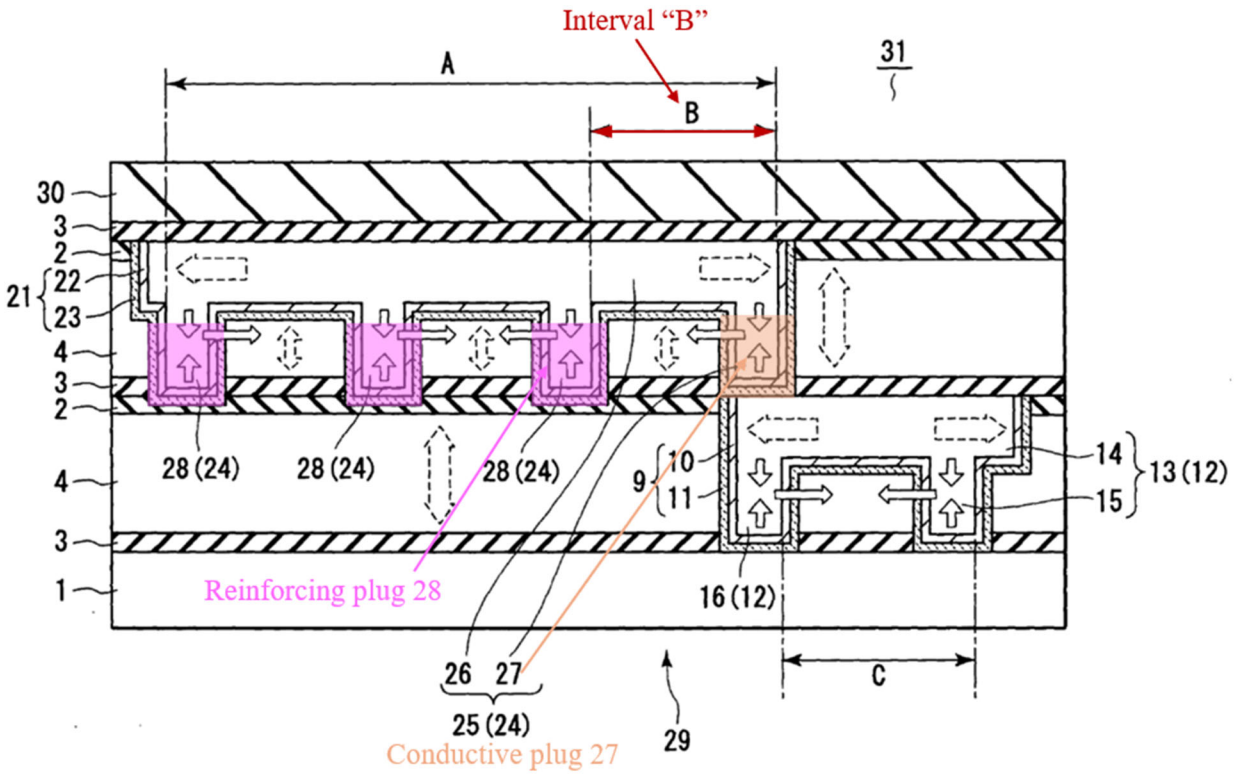


FIG. 9

TSMC-1005, ¶¶[0127], [0130]-[0137]; TSMC-1003, ¶¶377-78. As seen above, interval "B" is effectively equal to the center-to-center spacing between the via and

[6] Figure 9 depicts the same device of Hasunuma's first embodiment/Figure 8, adding various heat stress illustrations. TSMC-1005, ¶¶[0022], [0112]; TSMC-1003, ¶378 n.7.

dummy via, which is larger than the edge-to-edge spacing between the via and dummy via (e.g., the spacing between the right edge of reinforcing plug 28 and the adjacent left edge of conductive plug 27). TSMC-1003, ¶379.

Hasunuma teaches that a preferred interval B is about 1 μm or less, and shows such values in Tables 1-3. TSMC-1005, ¶[0137], Tables 1-3. Since B represents an even greater distance than the edge-to-edge spacing between the via and dummy via, this teaching for B satisfies the claim limitation of 25 μm or less. TSMC-1003, ¶¶380-81.

13. Claim 26

As noted for claim 25 above, Hasunuma teaches a preferred plug interval B of about 1 μm or less, thus satisfying claim 26 since the edge-to-edge spacing is smaller than the interval B spacing. TSMC-1005, ¶[0137], Tables 1-3; TSMC-1003, ¶¶382-85.

14. Claim 28

Hasunuma consistently shows and describes the use of multiple dummy vias (reinforcing plugs 28), with Figure 8 disclosing three such dummy vias, for example. TSMC-1005, ¶¶[0103], [0137], Fig. 8; TSMC-1003, ¶¶386-87.

15. Claim 32

Hasunuma teaches that the via (conductive plug 27) is preferably provided at an end-most portion of the wiring layer, as illustrated in Figure 8, where the via is

shown at one end (e.g., the rightmost end as disclosed) of the second interconnect (conductive layer 26). TSMC-1005, ¶[0171], Fig. 8; TSMC-1003, ¶390. Using the same definitions as previously described (*supra*, §VI.A.17), the dummy vias (reinforcing plugs 28) are located further along the second interconnect from that same end, as seen in Figure 8:

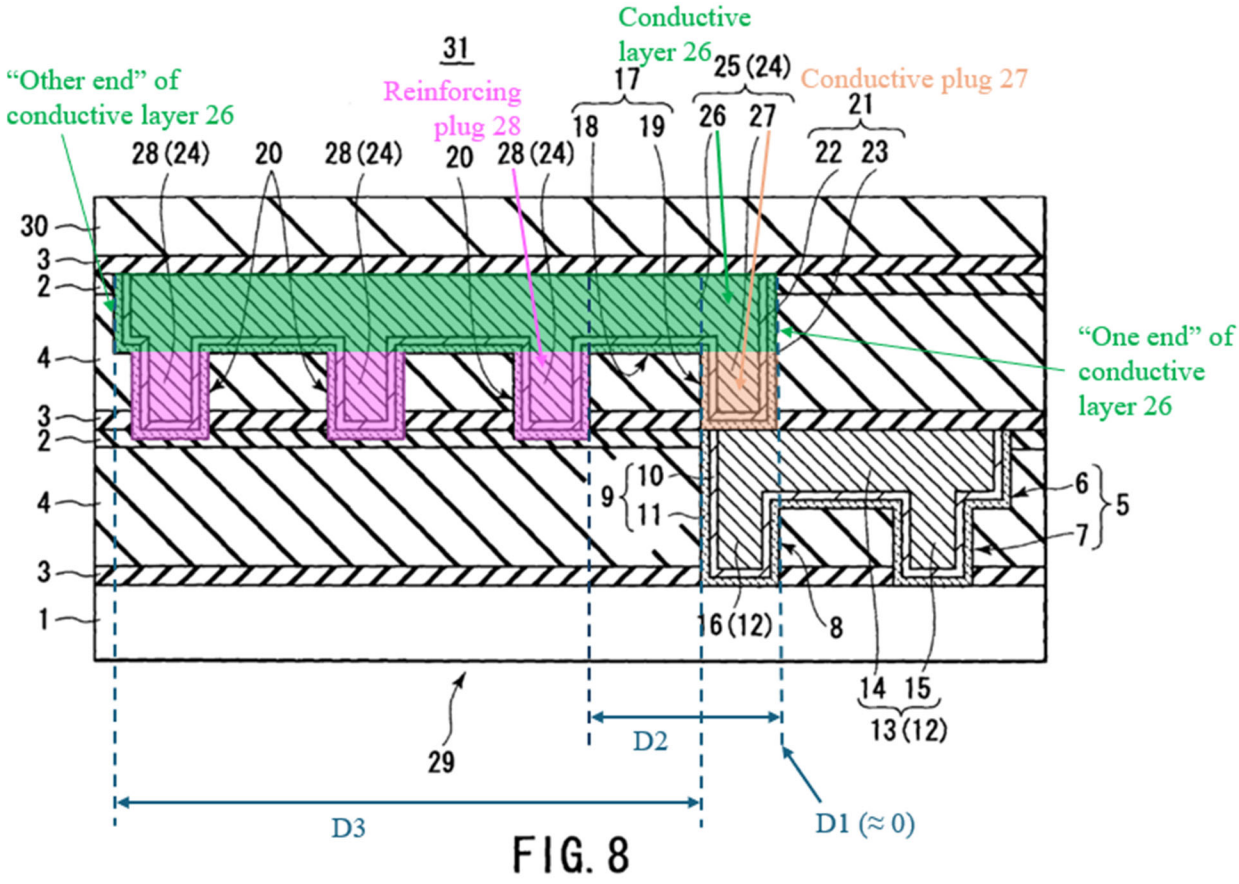


FIG. 8

TSMC-1003, ¶¶388-90.

In Figure 8, the distance D1 between the via and the proximate end of the second interconnect is minimal (essentially zero). *Id.*, ¶391. This minimal distance is shorter than the distance D2 from any dummy via to that same

proximate end. *Id*. Furthermore, this minimal distance from the via to the proximate end is also shorter than the distance D3 from the via to the opposite end of the second interconnect (e.g., the left end as disclosed in Figure 8). *Id*.

16. Claim 39

Hasunuma's dummy via (e.g., "reinforcing plug 28") and second interconnect (e.g., "conductive layer 26") are both made from the same conductive film (e.g., "Cu film 24" and/or "barrier metal film 21"), as illustrated in Figure 8 below:

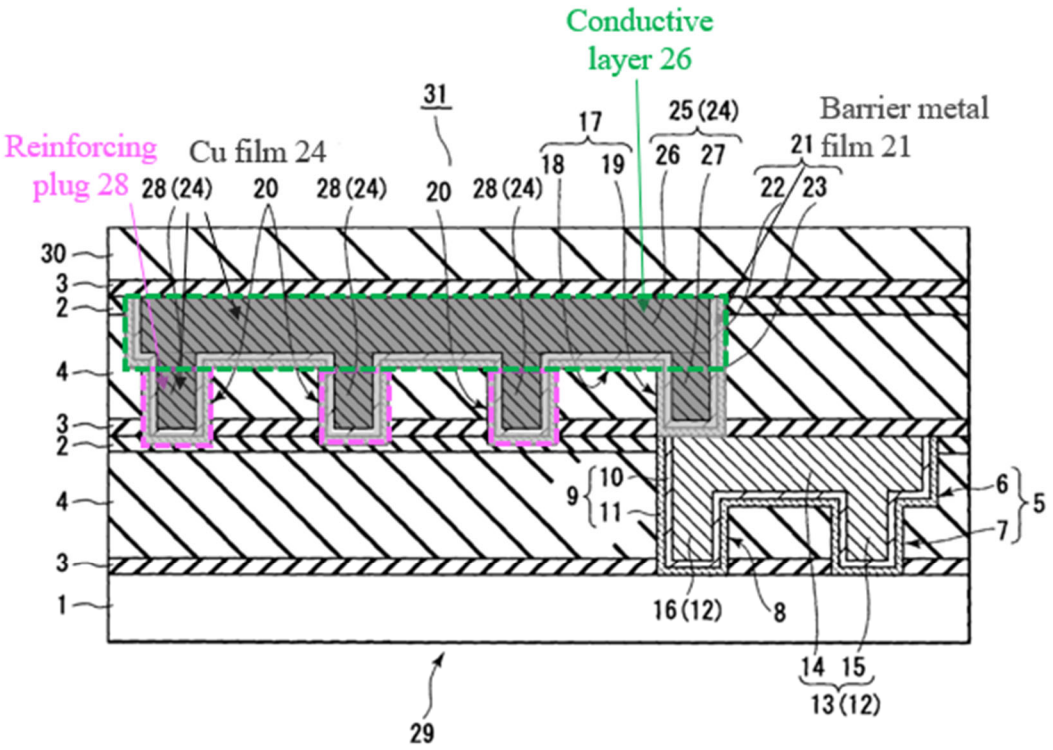


FIG. 8

TSMC-1005, ¶¶[0105]-[0108]; *supra*, §§VI.E.2.(h)-(i); TSMC-1003, ¶¶392-93.

Hasunuma's dual damascene process simultaneously forms the dummy via (reinforcing plug 28) and the second interconnect (conductive layer 26) by filling recesses (recess 20, recess 18) first with the same barrier metal film 21 and then with the same bulk Cu film 24, such that they are made of the same conductive film. *See* TSMC-1005, ¶¶[0105]-[0108]; TSMC-1003, ¶¶394-95.

17. Claim 40

As noted for claim 39, Hasunuma's dummy via and second interconnect both include copper film 24. *Supra*, §VI.E.16; TSMC-1003, ¶¶396-97.

F. Ground 6: Claims 2 and 8 Are Obvious Over Hasunuma and Kurashima

Hasunuma and Kurashima renders claims 2 and 8 obvious. TSMC-1003, ¶¶398-421.

1. Claim 2

a) [2.a]

Hasunuma discloses a second insulating film (e.g., the stack of insulating films 3, 4, and 2 in Figure 3A)[7], on silicon substrate 1:

[7] In the alternative, any or both of films 3 and 4 also satisfies the "second insulating film" element. TSMC-1003, ¶400 n.8.

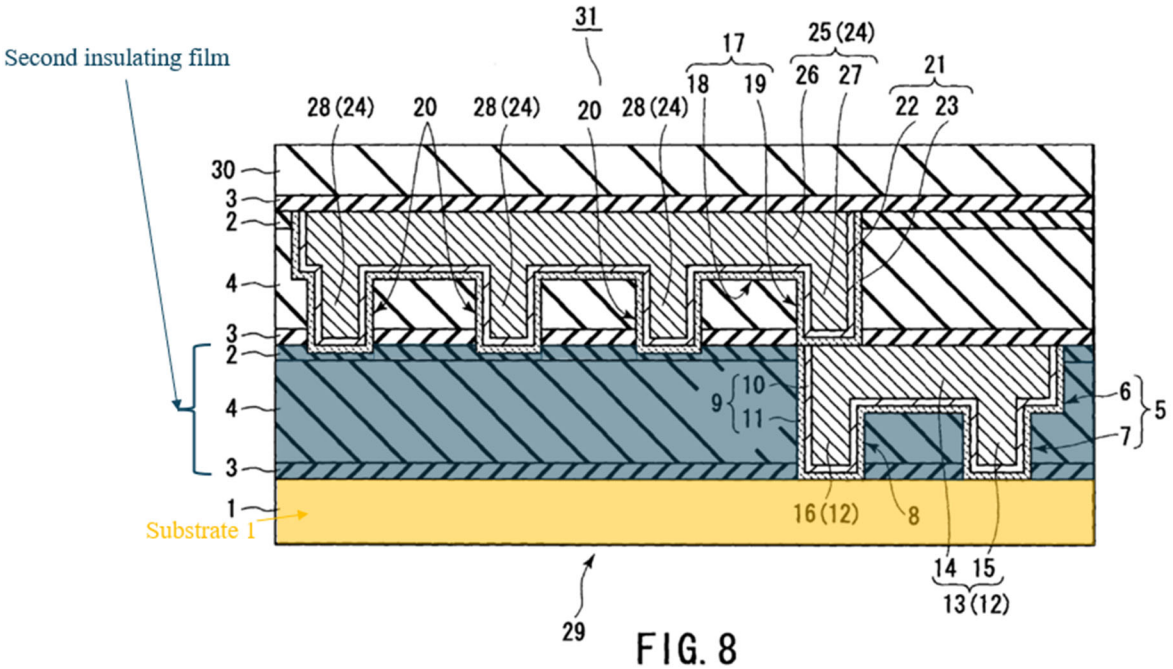


FIG. 8

TSMC-1005, ¶¶[0090]-[0091], Figs. 8, 14; TSMC-1003, ¶400.

b) [2.b]

Hasunuma discloses first interconnect (e.g., conductive layer 14) on the second insulating film:

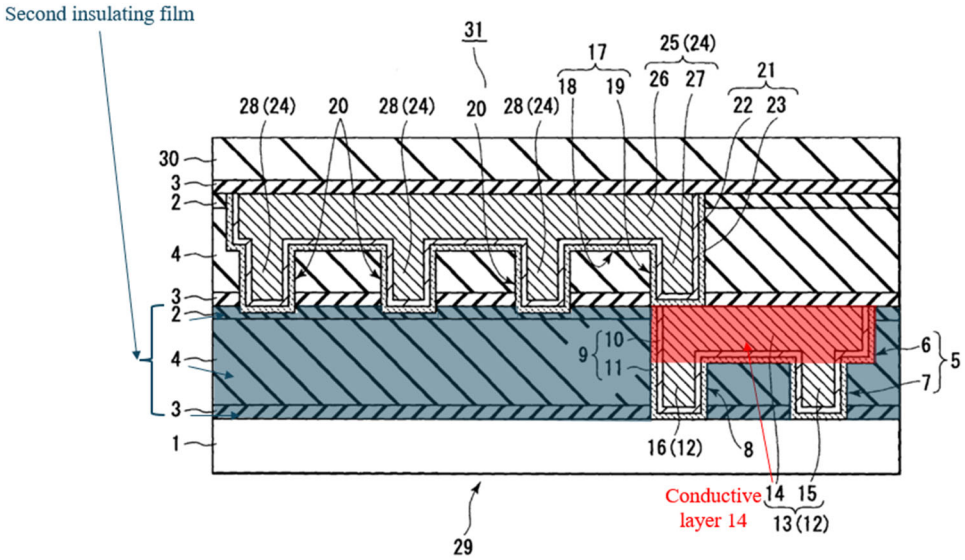


FIG. 8

98

TSMC-1005, ¶¶[0092]-[0098], Figs. 3A, 8, 14; TSMC-1003, ¶¶401-02.

c) [2.c]

Hasunuma discloses dummy vias (e.g., "reinforcing plugs 28"):

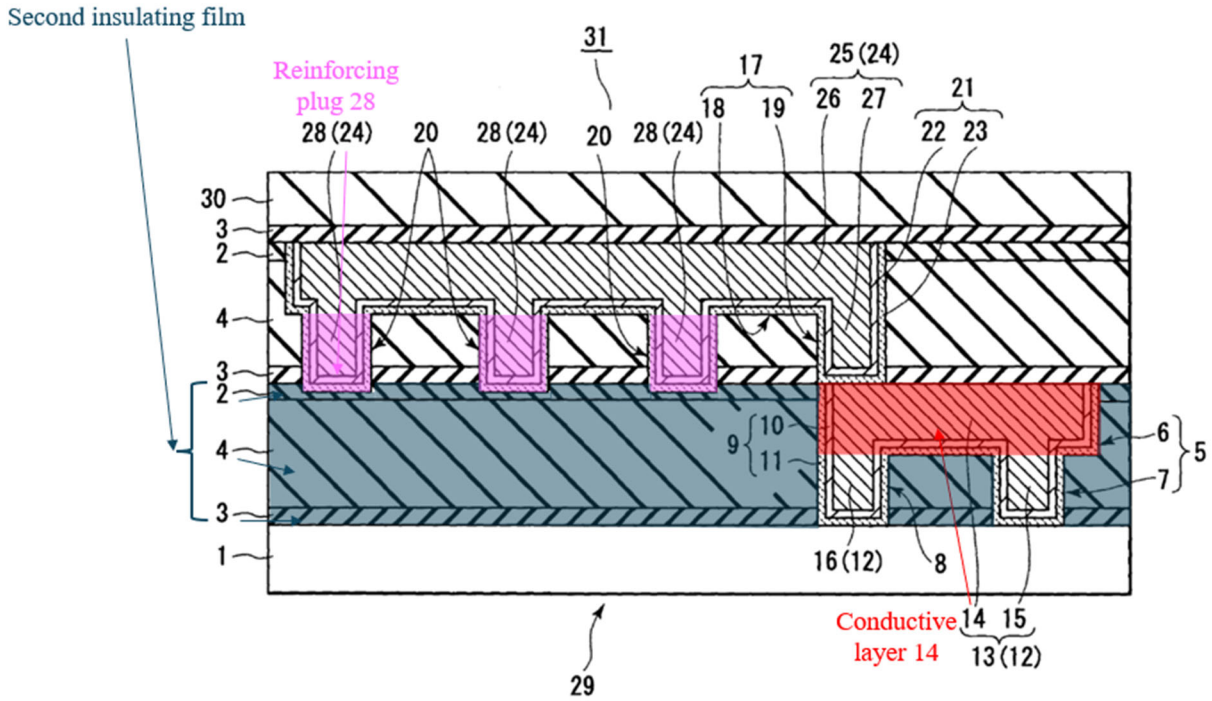


FIG. 8

Supra, §§VI.E.2.(g)-(h); TSMC-1003, ¶403-04.

Kurashima likewise teaches forming dummy wire 10 in first interlayer insulating film 4, and then dummy wire/via 17 is formed connecting to dummy wire 10:

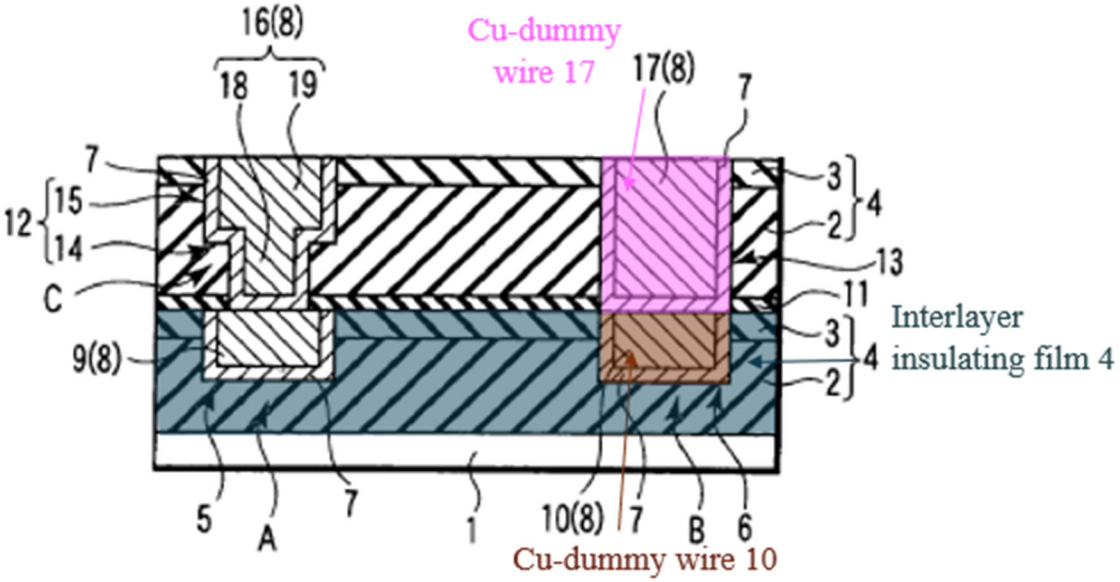


FIG. 3A

Supra, §VI.B.1; TSMC-1003, ¶¶405-06. The connection between dummy wire 10 and dummy wire 17 enhances the adhesion between insulating layers and improves durability against CMP-induced stress. *Id*.

d) Combining Hasunuma and Kurashima

A POSITA was motivated to improve the mechanical strength of Hasunuma's structure by applying Kurashima's teaching to connect Hasunuma's reinforcing plug(s) 28 to a dummy interconnect beneath them. TSMC-1003, ¶407. This suggested addition from Kurashima's Figure 3A to Hasunuma's Figure 8 structure is illustrated below:

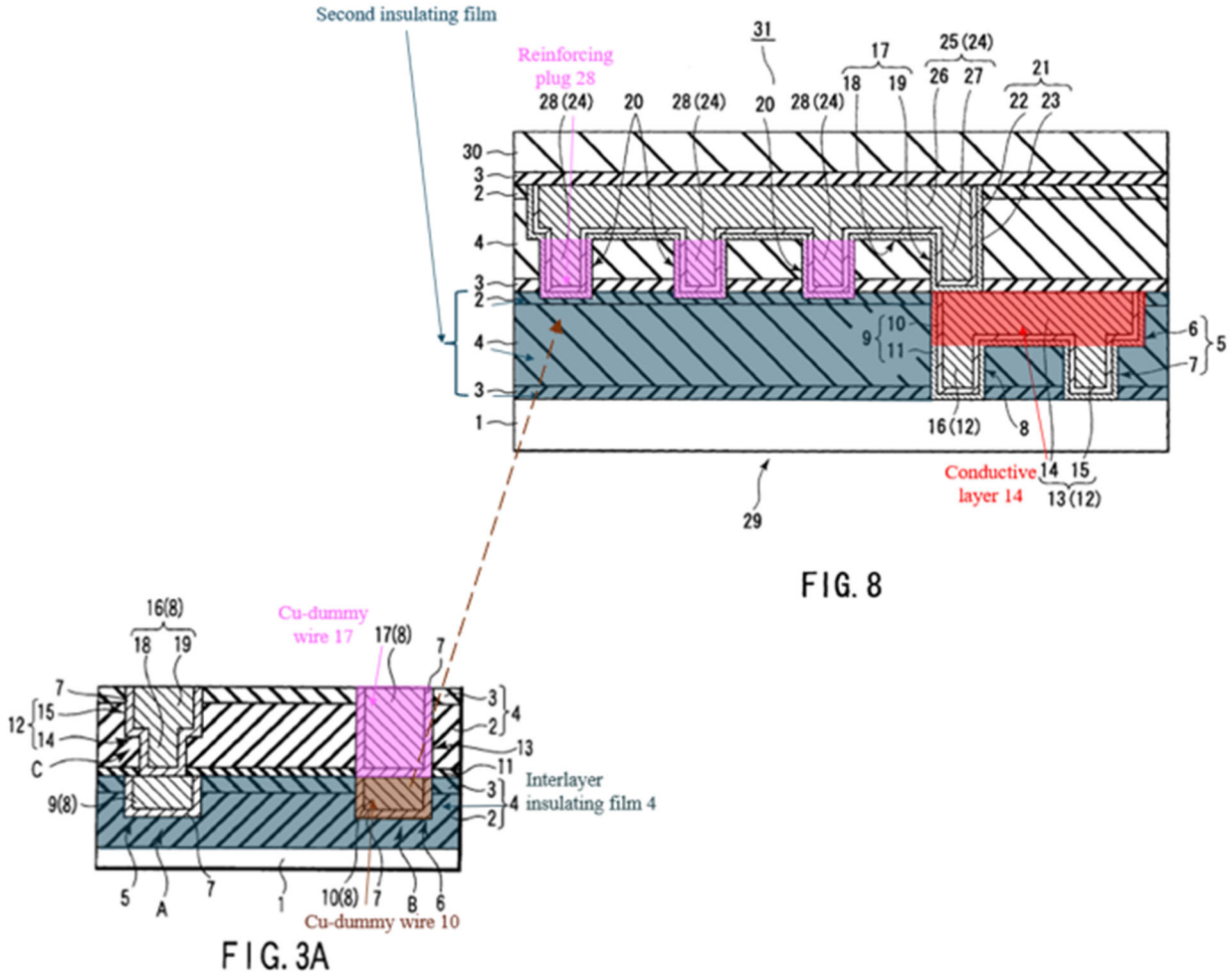


FIG. 8

FIG. 3A

Id.

A POSITA was motivated to incorporate Kurashima's dummy interconnect(s) into Hasunuma's device to increase the interlayer strength and reduce the likelihood of peeling or delamination between Hasunuma's lower films 4 and 2. *See* TSMC-1011, 5:63-6:32, 8:14-34, Figs. 5A-5B; TSMC-1003, ¶¶408-10. Kurashima's dummy plug-dummy interconnect structure also provided additional structural support and uniformity during the polishing step to reduce

dishing. *See* TSMC-1011, 5:63-6:32; TSMC-1007, 4:12-44; TSMC-1003, ¶¶411-12.

A POSITA would have expected success when incorporating Kurashima's dummy plug-dummy interconnect structure into Hasunuma's device, which entailed only the positioning of a dummy interconnect beneath one or more of Hasunuma's dummy vias/reinforcing plugs 28. TSMC-1003, ¶413. Creation of the dummy interconnect would have been easily accomplished using the same processing steps Hasunuma uses to create its conductive layer 14, with a reinforcing plug 28 connected thereto as part of building the next level in Hasunuma's Figure 8 structure. *Id*.

2. Claim 8

As discussed *supra*, §VI.F.1, Kurashima motivates a POSITA to add a dummy interconnect to Hasunuma.

The shapes of functional and dummy interconnects were a mere design choice, the selection of which was dictated by design parameters including establishing desired wire connections while optimizing density, managing crosstalk, and/or achieving specific CMP objectives. TSMC-1003, ¶¶414-16; *see, e.g.*, TSMC-1004, Fig. 9 (showing an exemplary routing for interconnect 60). This is exemplified by Kurashima, which discloses many different dummy wiring

shapes having "longer sides" oriented in either/both orthogonal direction(s), one of which is exemplified in Figure 6G:

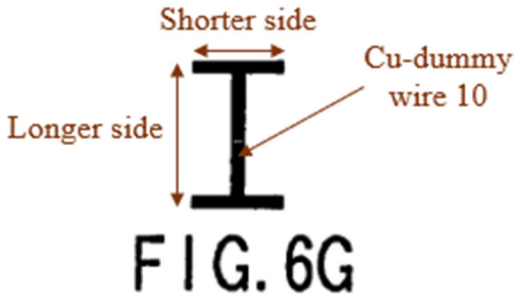


FIG. 6G

Supra, §VI.B.3; TSMC-1011, Figs. 3B, 6A-9C; TSMC-1003, ¶¶416-17.

Interconnects, including dummy interconnects and functional interconnects such as Hasunuma's conductive layer 14, will often have turns (including 90-degree corners) similar to Kurashima's Cu-dummy wire 10 and Watanabe's interconnect 60. TSMC-1003, ¶418. It was typical to have several such interconnects extending in different directions and around other elements, according to design requirements. *Id*.

Accordingly, when adding dummy interconnect(s) as taught by Kurashima into Hasunuma's device, each of Kurashima's foregoing dummy interconnect shapes were known, obvious design options, which would have been selected based on design requirements for the specific device being designed, and optimized for achieving improved adhesion between layers. *Id*., ¶419.

When choosing one of Kurashima's "longer side" shapes, it was obvious to position Hasunuma's conductive layer 14 ("first interconnect") such that its longer side was perpendicular to a longer side of an added dummy interconnect. *Id*., ¶420. For example, when choosing a dummy interconnect shape such as in Kurashima's Figure 6G, the dummy interconnect would be positioned with a longer side perpendicular to a longer side of Hasunuma's conductive layer 14 (or another similar interconnect in the same wiring level). *Id*.

A POSITA would have expected success when implementing such interconnect shapes and orientations, which merely requires that the trenches defining such interconnects be patterned in the desired shapes and orientations, which was easily accomplished with standard patterning and etching techniques. *Id*., ¶421.

G. Ground 7: Aoyagi renders obvious Claims 1, 16, and 45-46

1. Aoyagi

Because Aoyagi is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Aoyagi is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1006, Abstract, ¶¶[0001], [0004]-[0005]; TSMC-1003, ¶¶83-90.

Aoyagi discloses in Figures 2-12 and 19, and their supporting description, a semiconductor device and method of fabricating the device. Figures 3-4 disclose various parts of the device:

FIG. 3

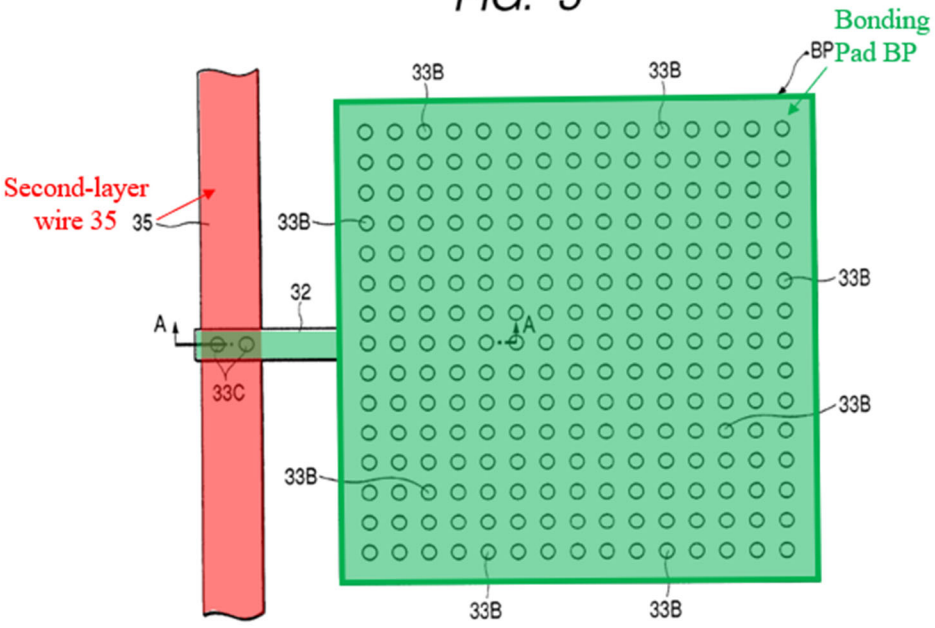
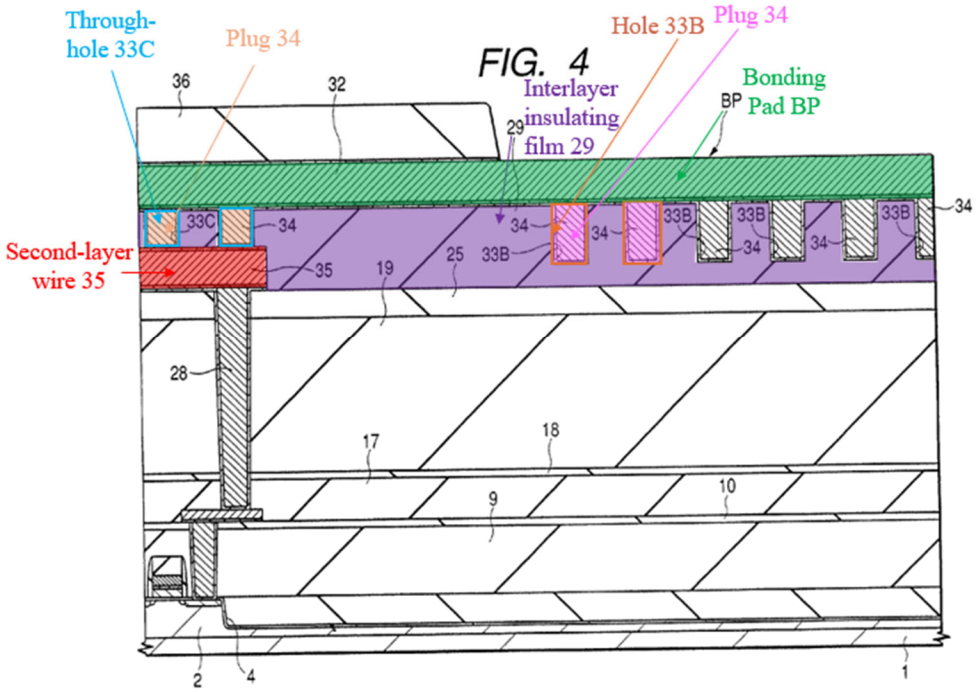


FIG. 4

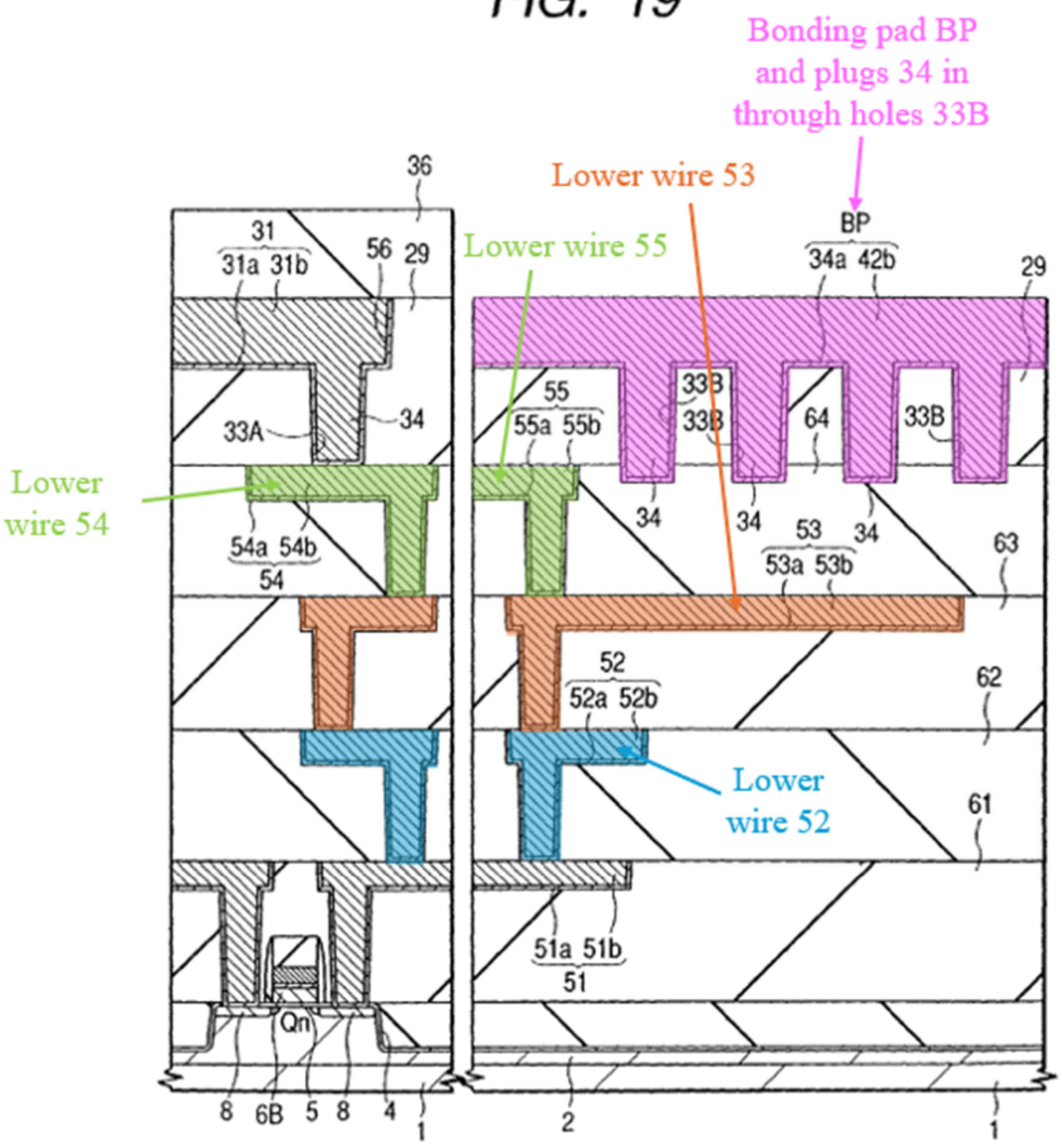


These figures show second-layer wire 35, interlayer insulating film 29, and bonding pad BP with lead wire 32 connected at one side.[8] TSMC-1006, ¶¶[0049], [0053]-[0056]. Vias (plugs 34 formed in through-holes 33C) connect bonding pad BP and second-layer wire 35, and dummy vias (plugs 34 formed in holes 33B) extend from bonding pad BP into insulating film 29 to improve adhesion. *Id*., ¶¶[0050]-[0055], [0079].

Aoyagi teaches a first process (e.g., Figures 5-12 (*id*., ¶¶[0058]-[0067])) and a dual damascene process (e.g., Fig. 19 (*id.*, ¶[0077])) for forming interconnects and vias. Figure 19 discloses dual-damascene-formed structures using common cross-hatching for the simultaneously-formed interconnects and the vias/dummy vias directly underneath:

[8] "Bonding pad BP" and "lead wire 32" together form a single, integral component, and thus discussion of "bonding pad BP" herein includes "lead wire 32" unless specified otherwise. *See* TSMC-1006, Figs. 3-4.

FIG. 19



The respective, common cross-hatching in each layer indicates that each wiring layer and the vias extending downward therefrom form dual damascene structures. TSMC-1003, ¶87. This dual-damascene teaching likewise applies to the interconnects (e.g., wire 35, bonding pad BP) and various functional and dummy

vias (e.g., plugs 34 in holes 33C, 33B) in Figures 3-4. *Id*. Specifically, Aoyagi's dual-damascene process may be used to create the interconnects, functional vias, and dummy vias in Figures 3-4. *Id*.

Given Aoyagi's discussion of using dual damascene to form wire 31/bonding pad BP and deposit conductive material in holes 33A and 33B and upper wire groove 56, it was obvious to use the dual damascene process to form bonding pad BP and the vias in through-holes 33C in the structure of Figures 3-4. TSMC-1003, ¶¶89, 423-27. A POSITA was motivated to use dual damascene to simplify manufacturing, increase efficiency, reduce costs, and increase reliability, and could have easily implemented such a process given its widespread use (including in Aoyagi). *Id*.; *supra*, §II.A; *see also* TSMC-1034, 583-84, 671-76, 718, 723-26; TSMC-1019, 145-151; TSMC-1027, 25; TSMC-1028, 5458-59.

Accordingly, Aoyagi renders claims 1, 16, and 45-46 obvious. TSMC-1003, ¶¶422-64.

2. Claim 1

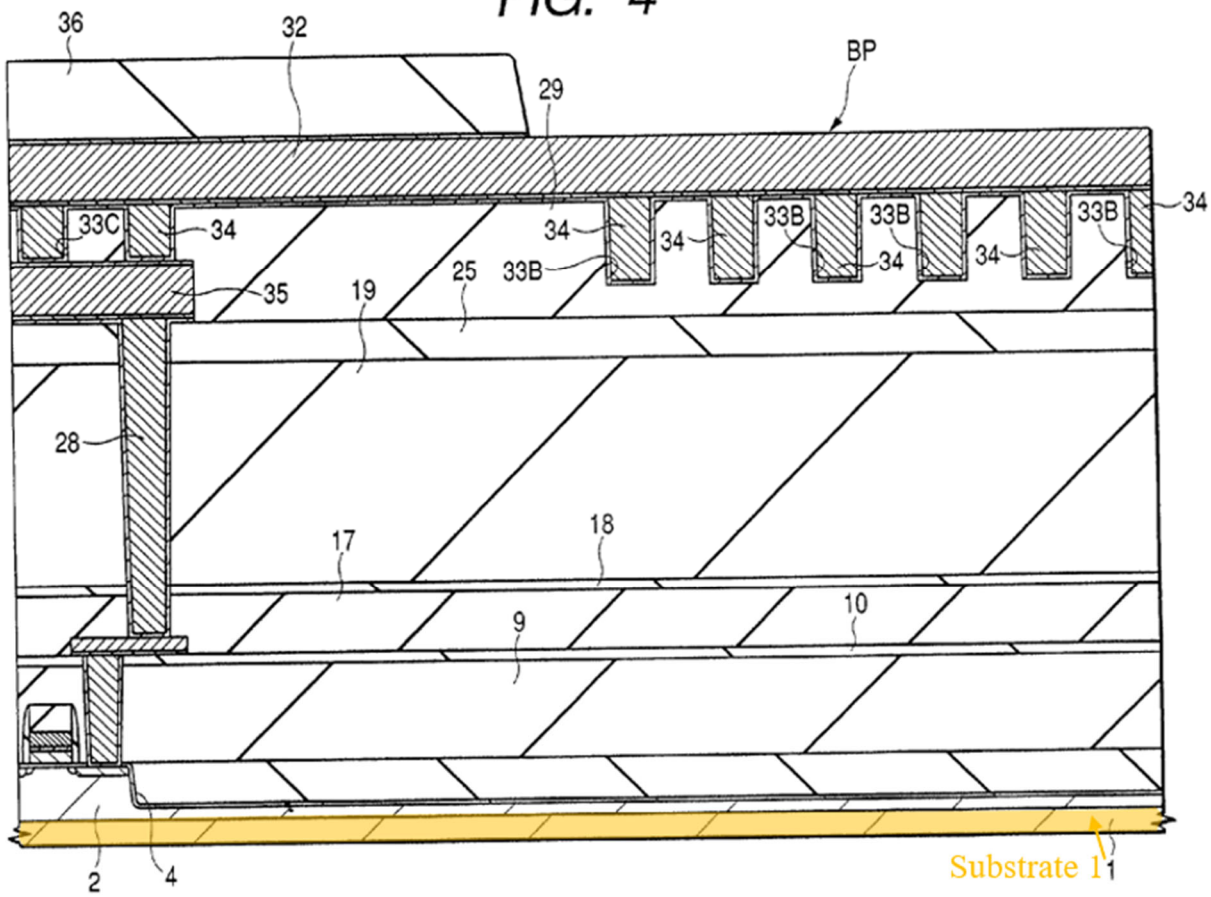
a) [1.pre]

Aoyagi discloses a "semiconductor integrated circuit device." TSMC-1006, Abstract, ¶[0001], Figs. 1-4, 19; TSMC-1003, ¶428.

b) [1.a]

Aoyagi discloses a semiconductor substrate 1:

FIG. 4

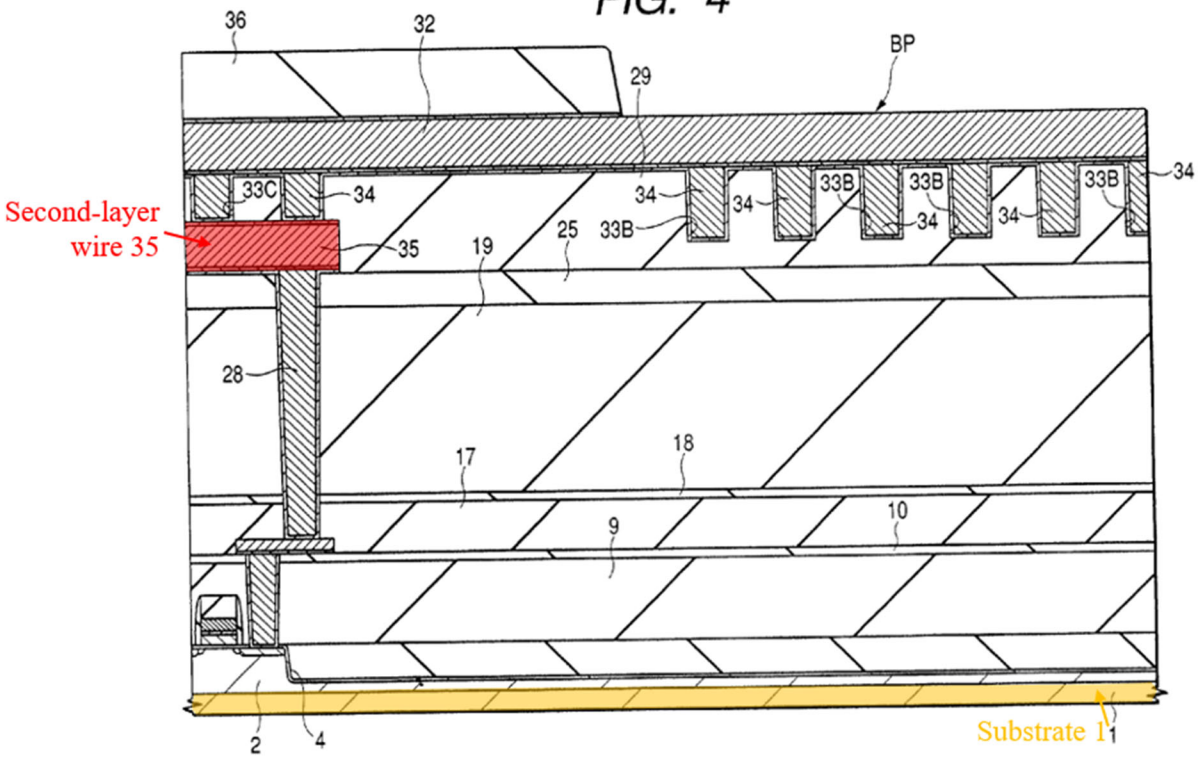


TSMC-1006, ¶¶[0040], [0043], [0057], [0061], Figs. 2, 4; TSMC-1003, ¶429.

c) [1.b]

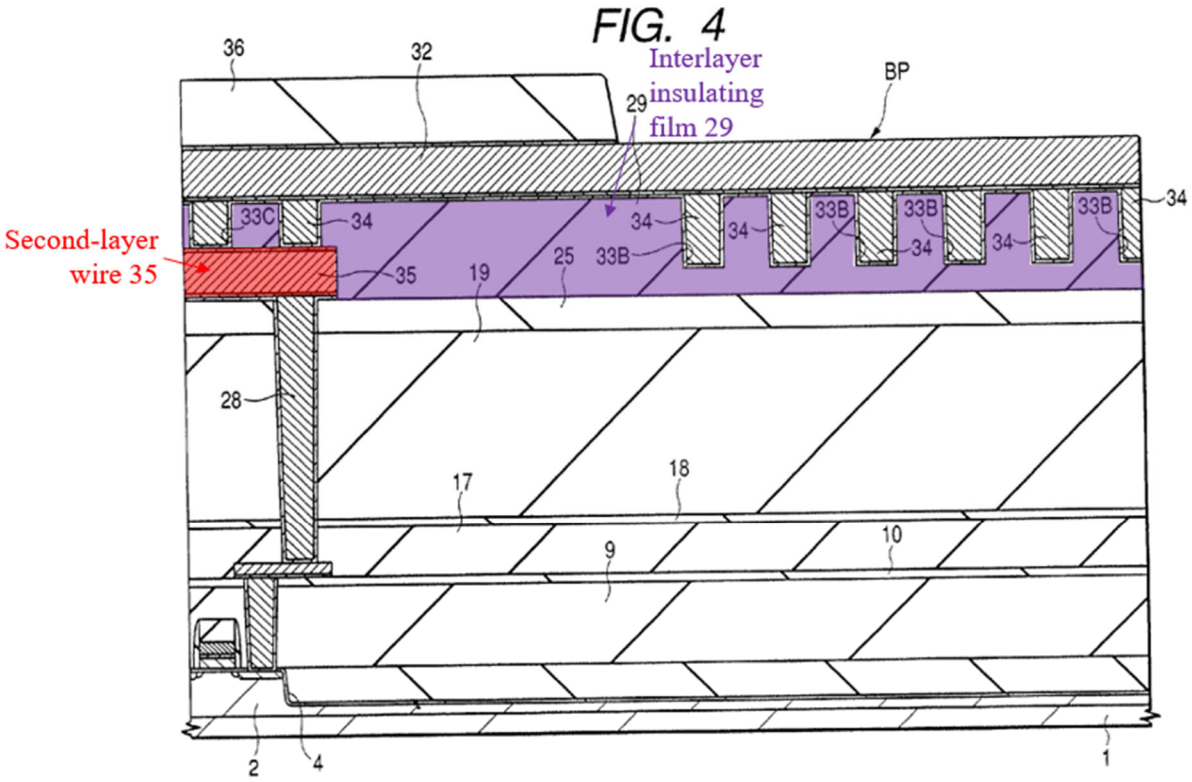
Aoyagi discloses a first interconnect (e.g., "second-layer wire 35") formed on substrate 1 (TSMC-1006, ¶¶[0055], [0061], Figs. 4, 7; TSMC-1003, ¶¶430-31):

FIG. 4



d) [1.c]

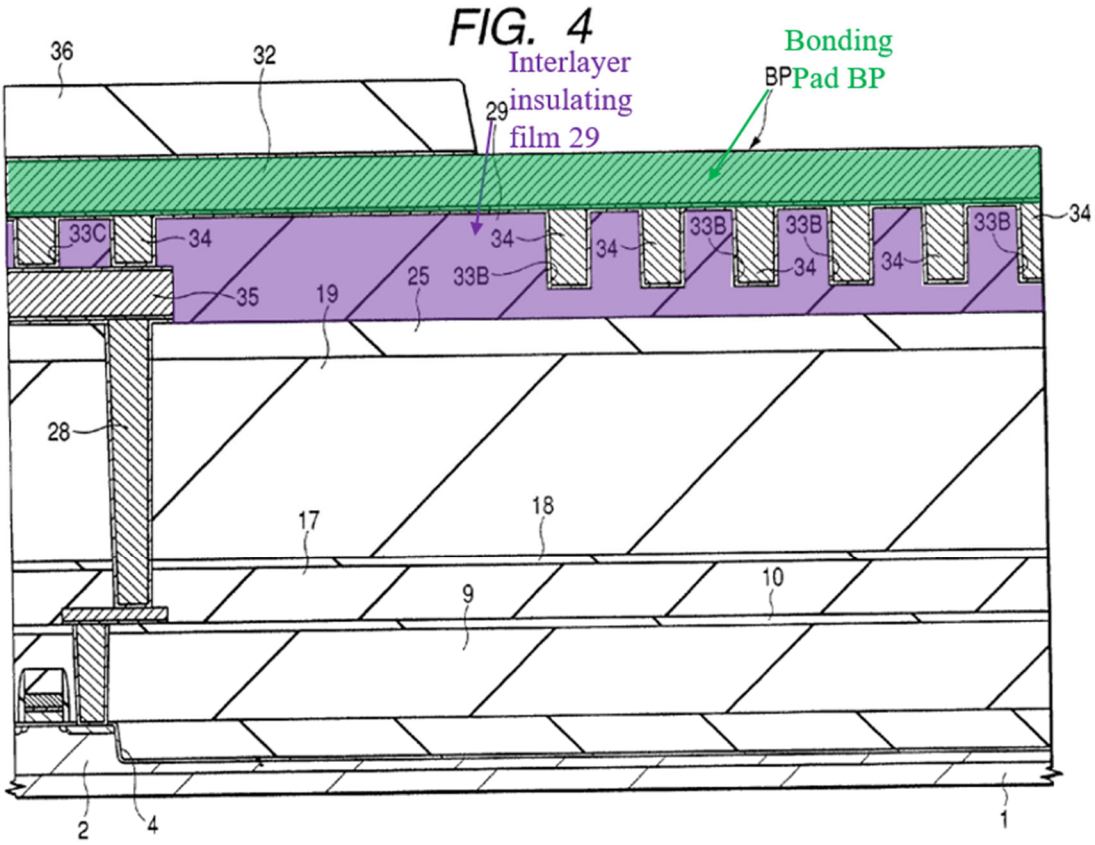
Aoyagi discloses interlayer insulating film 29 formed on second-layer wire 35 (TSMC-1006, ¶¶[0049], [0062], Figs. 4, 8; TSMC-1003, ¶¶432-33):



Aoyagi's "insulating film (first interlayer insulating film) 29…is formed over the second-layer wires…." TSMC-1006, ¶[0049].

e) [1.d]

Aoyagi discloses a second interconnect (e.g., "bonding pad BP") formed on insulating film 29:

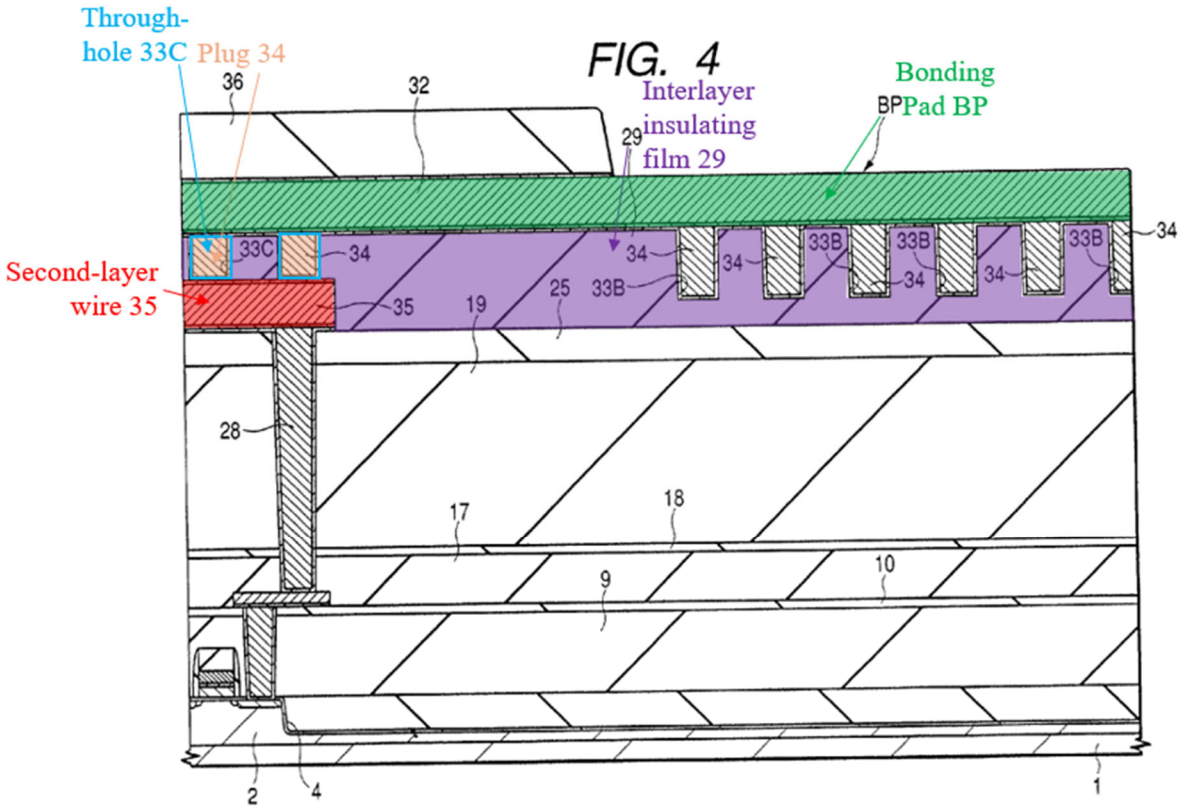


TSMC-1006, ¶¶[0049]-[0055], [0077], Figs. 2-4, 19; TSMC-1003, ¶¶434-36.

When employing dual damascene, bonding pad BP is formed by depositing "barrier metal film 34a" and then "Al alloy film 31b (42b)" onto interlayer insulating film 29. TSMC-1006, ¶[0077]; Fig. 19; TSMC-1003, ¶436.

f) [1.e]

Aoyagi discloses a via (e.g., "plug 34" in "through-hole 33C") formed through insulating film 29 that connects the first and second interconnects (e.g., "second-layer wire 35" and "bonding pad BP," respectively).

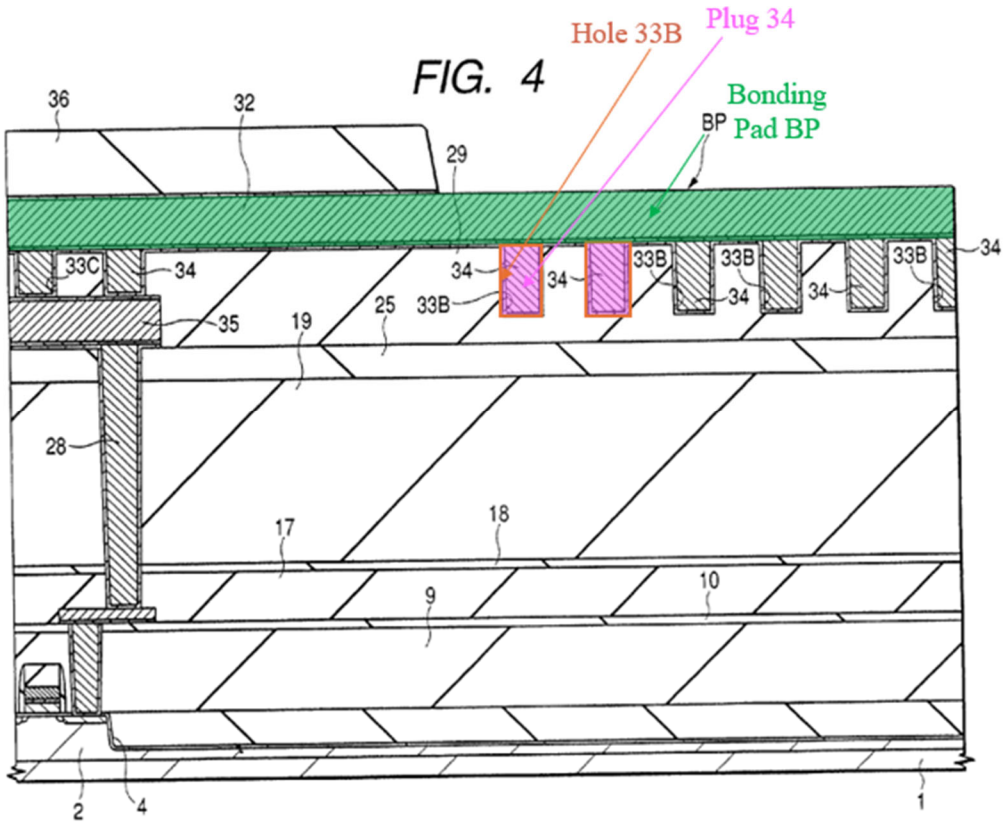


TSMC-1006, ¶¶[0049]-[0055], [0077], Figs. 2-4, 19; TSMC-1003, ¶¶437-40.

When formed using dual damascene, plugs 34 (within holes 33C) are formed by depositing barrier metal film 34a in holes 33C formed through insulating film 29, and then depositing "Al alloy film 31b (42b)" on the barrier metal film. TSMC-1006, ¶[0077]; TSMC-1003, ¶440.

g) [1.f]

Aoyagi discloses dummy vias (e.g., "plugs 34" formed in "holes 33B") connected to the second interconnect (e.g., "bonding pad BP"):



TSMC-1006, ¶¶[0050]-[0056], [0077], Figs. 2-4, 19; TSMC-1003, ¶¶441-42.

h) [1.g]

Aoyagi teaches using a dual damascene process to form wire 31/bonding pad BP and deposit conductive material in holes 33A and 33B, thereby forming vias and dummy vias, respectively. TSMC-1006, ¶[0077]. It was obvious to apply this dual damascene process to form bonding pad BP together with the vias/plugs 34 in holes 33C and the "dummy" vias/plugs 34 in holes 33B in the structure of Figures

3-4. *Supra*, §VI.G.1; TSMC-1003, ¶¶423-27; *see also* TSMC-1006, ¶[0036] (stating "like reference numerals indicate like parts or members" across its figures and embodiments). A POSITA was motivated to do so by the simplified manufacturing, increased efficiency, reduced cost, and increased reliability of dual damascene, and could have easily implemented such a process given its widespread use. TSMC-1003, ¶¶426, 445; *supra*, §§II.A, VI.G.1.

When formed by dual damascene, "dummy" plugs 34 in holes 33B are formed by successively depositing a barrier metal film and Al alloy film (i.e., a conductive film) in holes 33B. TSMC-1006, ¶[0077]; TSMC-1003, ¶¶444-45.

Additionally, these dummy plugs 34/dummy vias in holes 33B are "incapable of having current flow therethrough." TSMC-1003, ¶¶446-51. As disclosed in Figures 4 and 19, holes 33B and plugs 34 therein are formed entirely within one or more insulating films. These "dummy" holes 33B/"dummy" plugs 34 are only connected on one end to an active circuit element (i.e., "bonding pad BP"), while the other end is not connected to a second active circuit element. Dummy plugs 34 improve "adhesion" between bonding pad BP and insulating film 29. TSMC-1006, ¶¶[0053], [0079]; Fig. 4. Thus, no current flows through Aoyagi's dummy plugs 34 due to this lack of connection to a second active circuit element. TSMC-1003, ¶¶448-51. Instead, current flows between Aoyagi's second-layer wire 35 and bonding pad BP through plugs in holes 33C, which

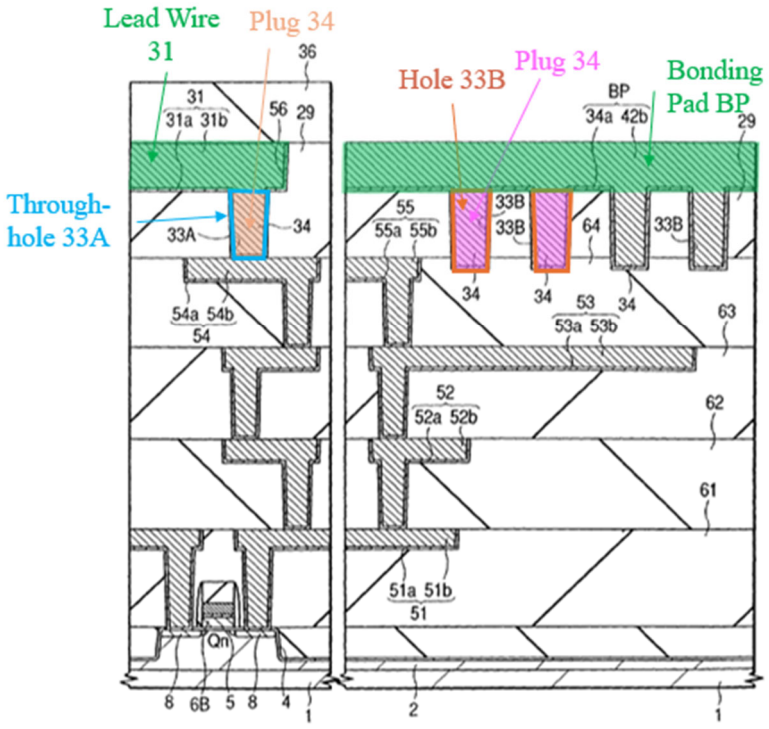
constitute parts of a closed circuit in actual use of the device. TSMC-1006, ¶[0055], Figs. 3-4; TSMC-1003, ¶450.

Moreover, Aoyagi's device would still be operable if dummy plugs 34 were omitted, because current would flow through the active circuit elements (i.e., bonding pad BP, holes 33C/plugs 34 therein, and second-layer wiring 35) during actual use of the device. TSMC-1003, ¶451.

i) [1.h]/[1.i]

Aoyagi teaches integrally forming its second interconnect (bonding pad BP), functional vias (plugs 34 in holes 33A), and dummy vias (plugs 34 in holes 33B) by dual damascene:

FIG. 19



TSMC-1006, ¶[0077]; Fig. 19; TSMC-1003, ¶¶453-55.

It was obvious to form bonding pad BP and the vias/dummy vias in holes 33B and 33C of the device in Figures 3-4 using this same process:

FIG. 19

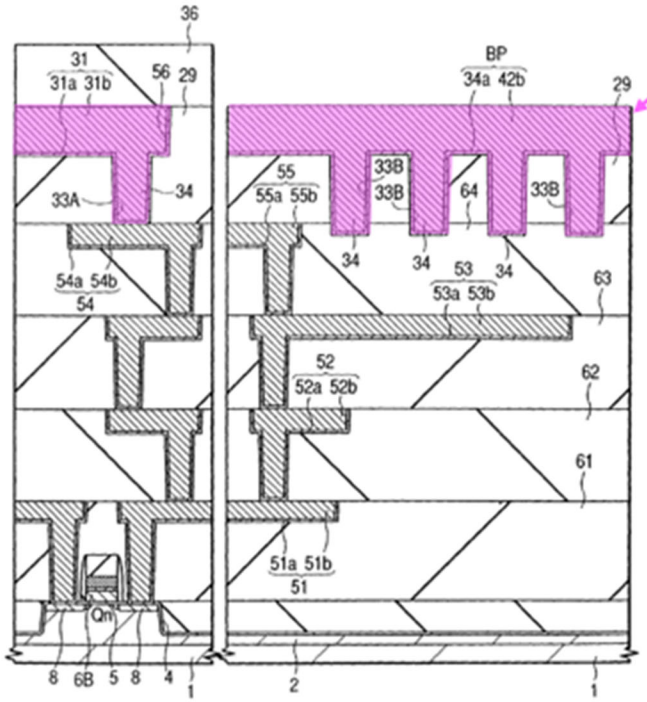
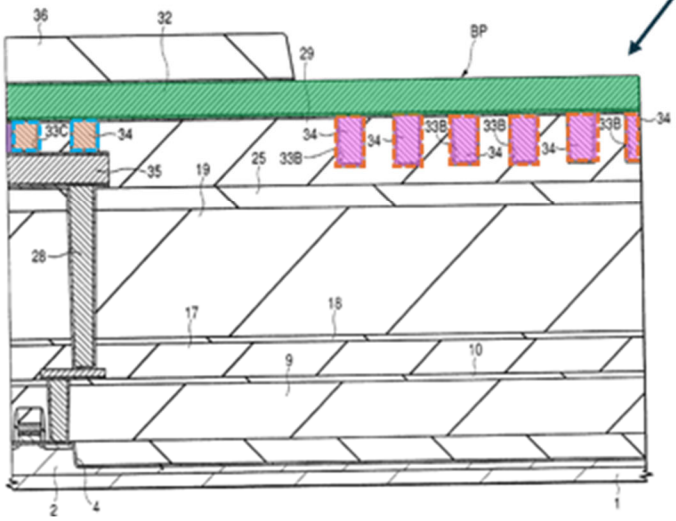


FIG. 4



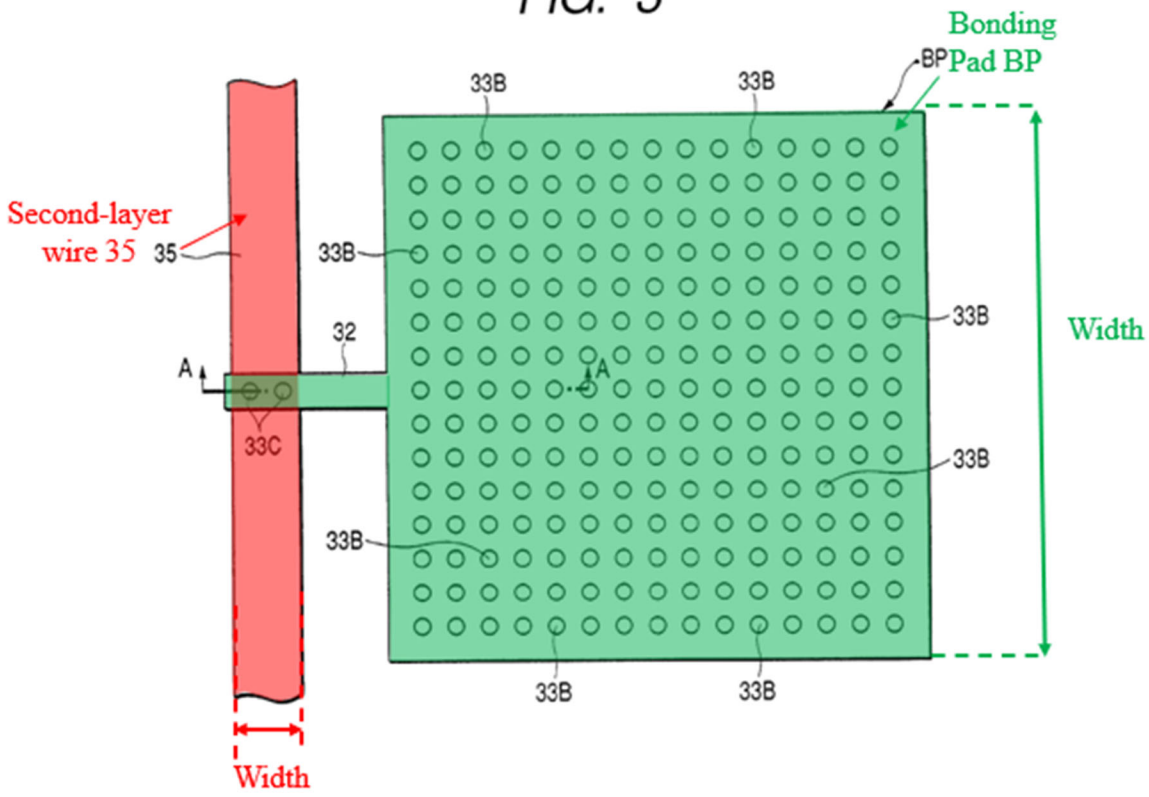
Supra, §§VI.G.1, VI.G.2.(h); TSMC-1003, ¶¶456-57.

A POSITA was motivated to apply Aoyagi's dual damascene process for the well-known associated benefits including simplified manufacturing, increased efficiency, reduced cost, and increased reliability. TSMC-1003, ¶¶424-27, 456; *supra*, §§II.A, VI.G.1, VI.G.2.(h). Dual damascene was commonly used for such interconnect structures and easily implemented given its widespread use, as evidenced by Aoyagi's own teachings. *Id*. Using dual damascene, a given interconnect structure is formed in its entirety and simultaneously with its associated vias/dummy vias. TSMC-1003, ¶457. Accordingly, when applying Aoyagi's dual damascene process to the embodiment of Figures 2-4, Aoyagi's bonding pad BP (second interconnect) forms dual damascene structures with the vias/dummy vias in holes 33C/33B, respectively. *Id*.

3. Claim 16

Aoyagi's first interconnect (e.g., "second-layer wire 35") has a width smaller than that of the second interconnect (e.g., "bonding pad BP"):

FIG. 3



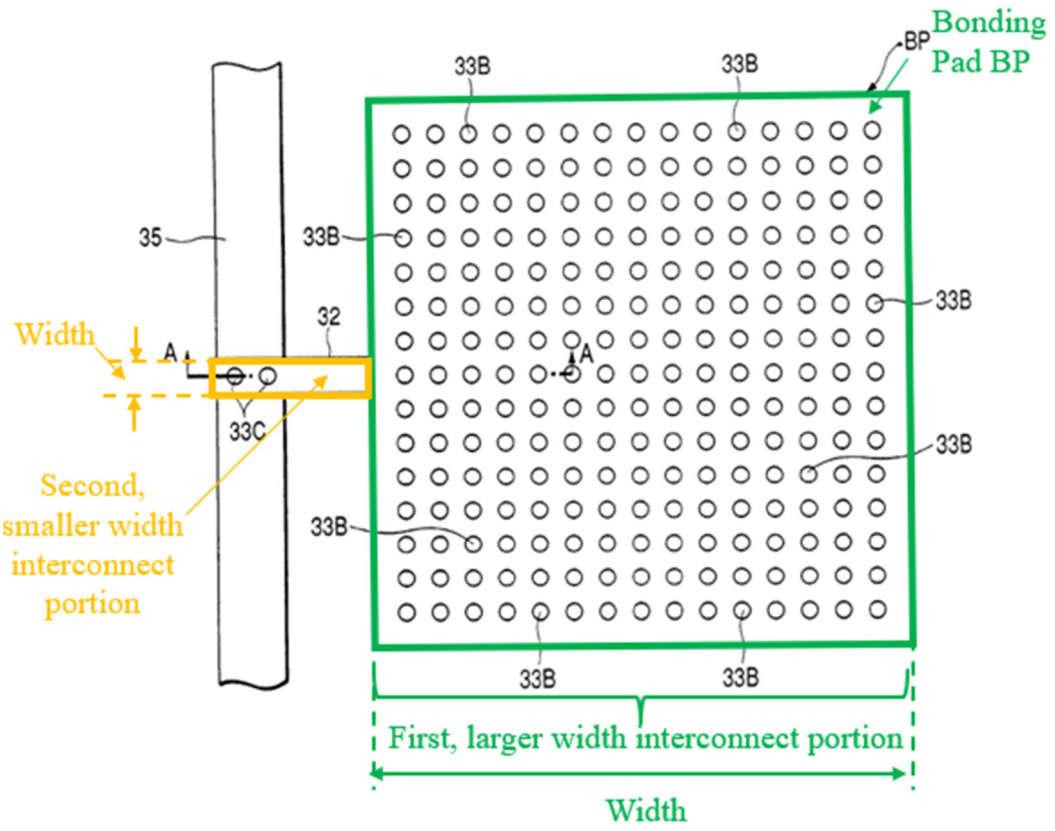
TSMC-1006, Fig. 3; TSMC-1003, ¶¶458-59.

4. Claim 45

a) [45.a]

Aoyagi discloses a second interconnect (e.g., "bonding pad BP" with "lead wire 32") having a first interconnect portion (wider portion of "bonding pad BP") and a second interconnect portion with a smaller width and branching from the first interconnect portion ("lead wire 32" portion of "bonding pad BP"):

FIG. 3

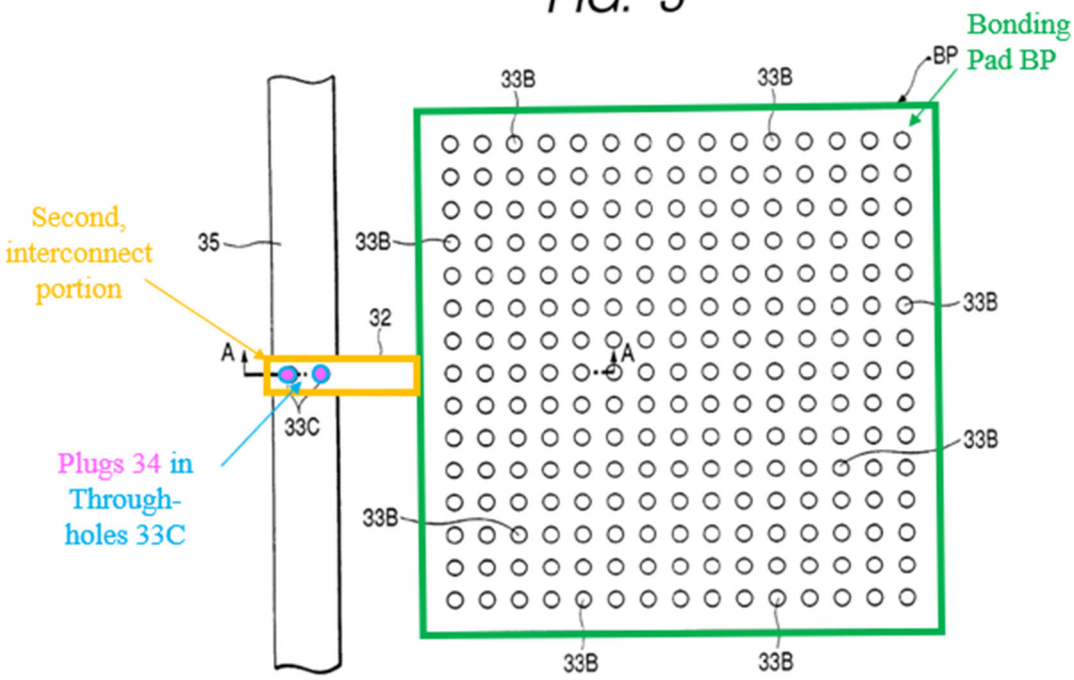


TSMC-1003, ¶¶461-62; TSMC-1006, ¶[0055], Fig. 3.

b) [45.b]

Aoyagi's vias (e.g., plugs 34 in holes 33C) are connected to the second interconnect portion (e.g., lead wire 32 portion of bonding pad BP):

FIG. 3

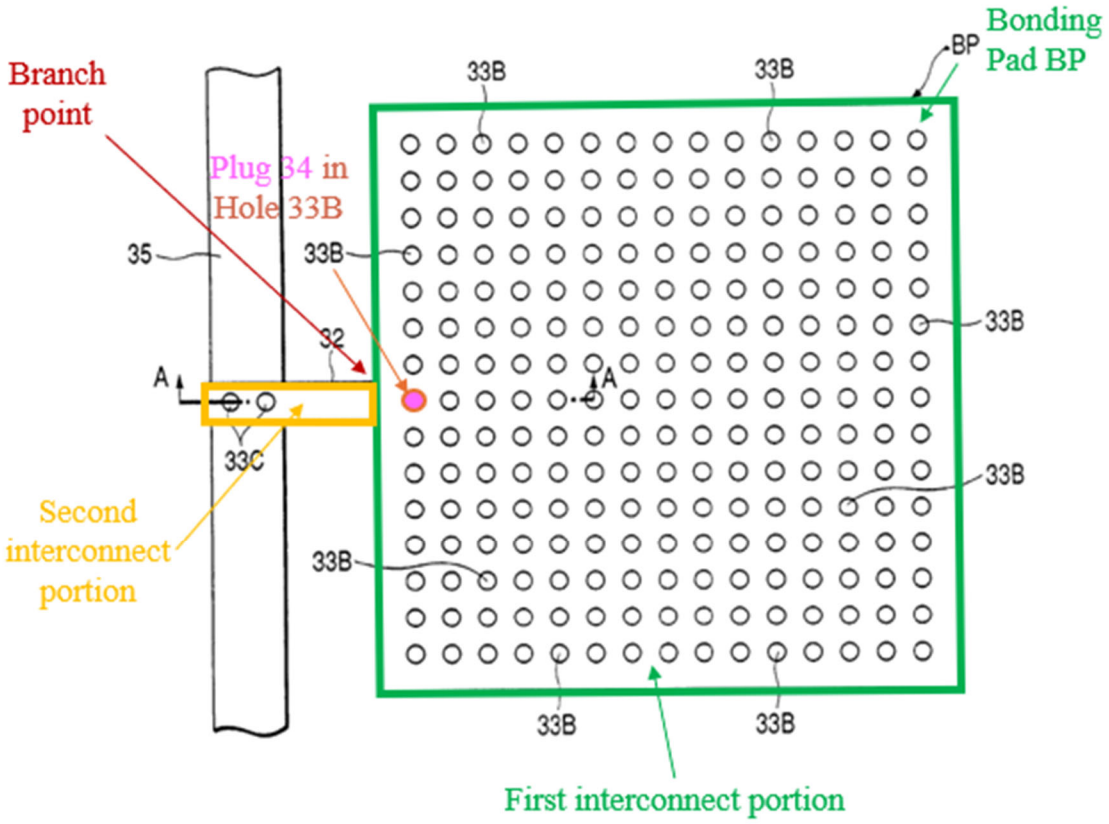


TSMC-1006, ¶¶[0054]-[0055], Fig. 3; TSMC-1003, ¶463.

5. Claim 46

Dummy hole 33B and plug 34 therein is formed near the branch point between the first and second portions (wider bonding pad BP portion, lead wire 32 portion) of the second interconnect (bonding pad BP):

FIG. 3



TSMC-1003, ¶464; TSMC-1006, Fig. 3.

H. Ground 8: Claim 47 Is Obvious Over Aoyagi and Hasunuma

Claim 47 is obvious over Aoyagi and Hasunuma. TSMC-1003, ¶¶465-70. Hasunuma teaches fabricating and using wiring layers with dimensions of 0.13 µm. TSMC-1005, ¶[0127] (teaching an interconnect wiring width of "about 0.13 µm").

It was obvious to utilize Hasunuma's width dimension for Aoyagi's lead wire 32. TSMC-1003, ¶¶468-70. Specific sizing (including widths of 0.2 µm or less) of Aoyagi's "lead wire 32" was a predictable design choice as evidenced, for

example, by Hasunuma's disclosed 0.13 μm width. *Id*. A POSITA was motivated to minimize the width as much as reasonably possible. *Id*., ¶469. For example, Kamoshima discusses benefits associated with a narrow-width interconnect branch, including creating a narrow path to restrict vacancy flow to active vias (such as Aoyagi's holes 33C/plugs 34). *See* TSMC-1009, ¶¶[0094]-[0109]. Narrow widths of 0.2 μm or less would have improved the mitigation of such vacancy flow. TSMC-1003, ¶469.

Moreover, a POSITA would have had a reasonable expectation of success. *Id*., ¶470. Both Hasunuma and Aoyagi disclose manufacturing interconnects by dual damascene, and a POSITA recognizes that the minimum interconnect width depends on the capabilities of the etching process to form trenches. TSMC-1005, ¶¶[0098], [0101]; TSMC-1006, ¶[0077]; TSMC-1003, ¶470. Hasunuma discloses that such widths are viable, and that its conductive layer and plugs and reinforcing plugs can be aluminum. TSMC-1005, ¶[0294]. Additionally, Aoyagi's bonding pad BP/lead wire 32 is an aluminum alloy film. TSMC-1006, ¶¶[0050], [0074], [0077]. Narita describes similar aluminum alloy interconnects with widths less than 0.2 μm (e.g., 0.175 μm), confirming that such dimensions are achievable for Aoyagi's lead wire 32. TSMC-1031, ¶¶[0016], [0029]-[0030]; TSMC-1003, ¶470.

I. Ground 9: Kunikiyo Renders Claims 1-2, 4, 7, 14, and 42 Unpatentable

Kunikiyo anticipates and renders obvious claims 1-2, 4, 7, 14, and 42. TSMC-1003, ¶¶471-516.

1. Kunikiyo

Because Kunikiyo is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Kunikiyo is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1007, Abstract, 1:9-15, 6:34-7:7, 12:31-41, 20:4-14; TSMC-1003, ¶¶91-93.

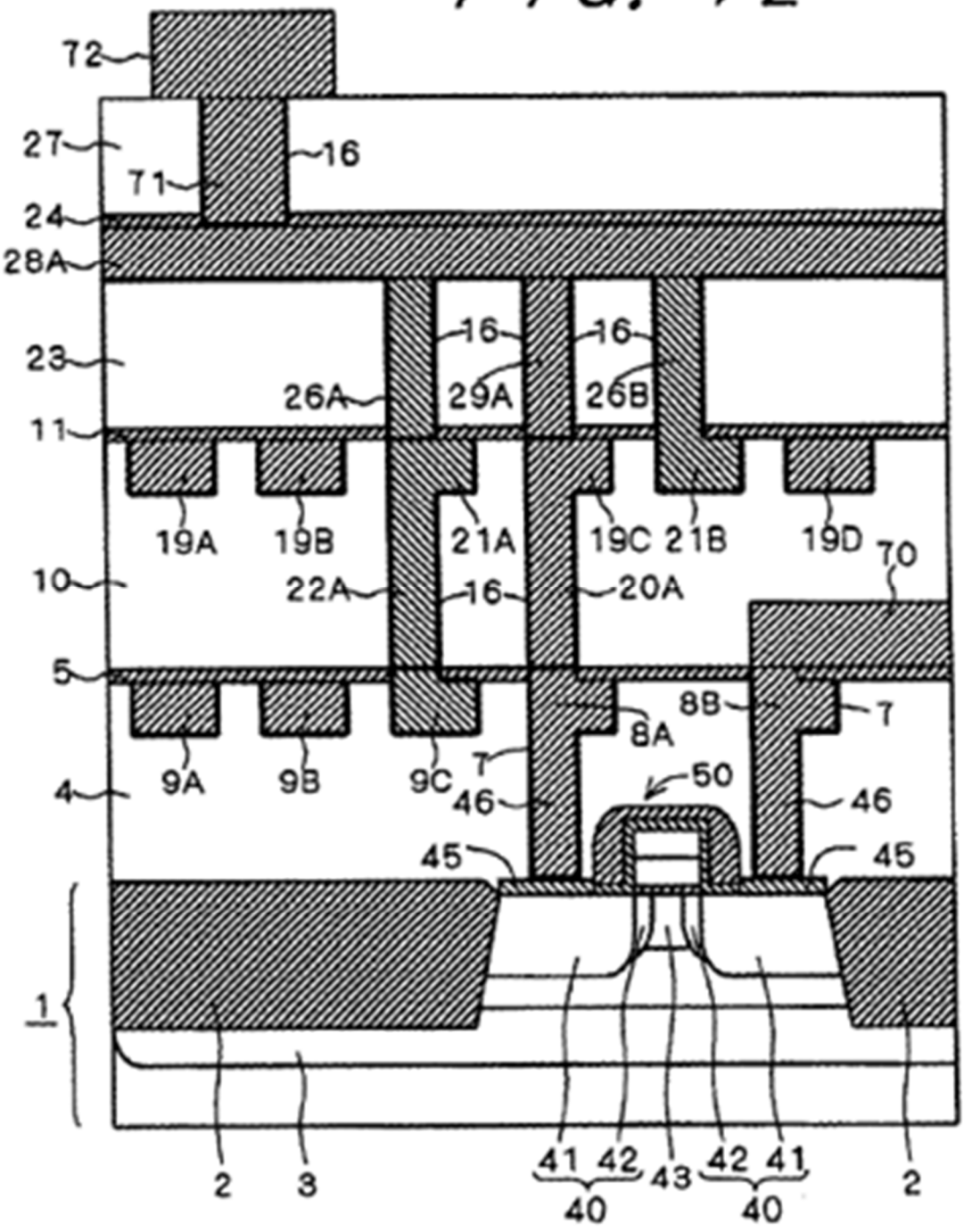
Kunikiyo's Figure 12 embodiment discloses a semiconductor device featuring a multilayered interconnect structure, with additional features and connections beyond the Figure 7 embodiment. TSMC-1007, 20:4-49. In addition to the active interconnects and vias essential for device operation, Figure 12 adds dummy vias attached to active interconnects, including dummy interconnects attached to the dummy vias. *Id*. Kunikiyo teaches incorporating such dummy structures to enhance the uniformity of interconnection density and reduce electronic noise. *Id*., 5:46-56, 12:31-36, 14:31-36, 15:62-67, 25:54-26:9.

2. Claim 1

a) [1.pre]

Kunikiyo's Figure 12 discloses a semiconductor device:

FIG. 12

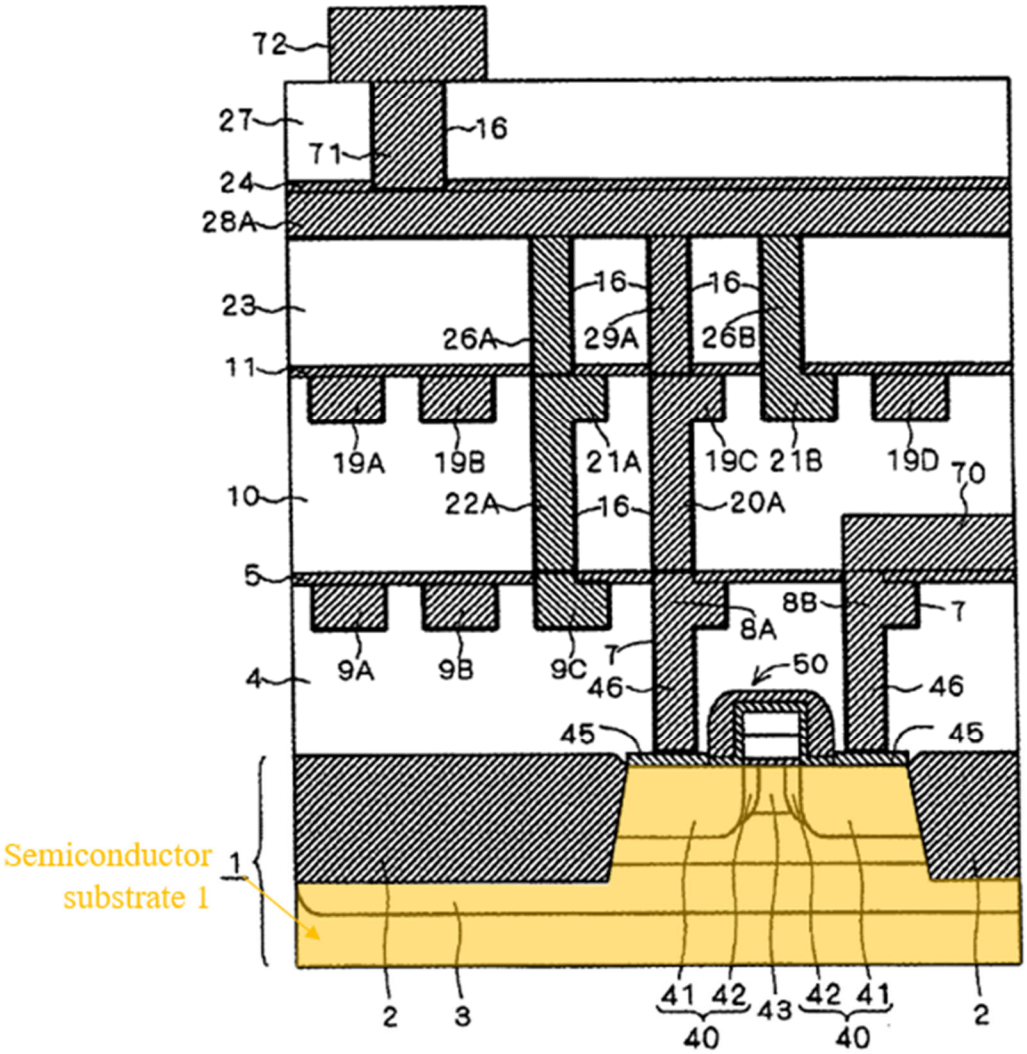


TSMC-1007, 10:50-55, 20:4-24; TSMC-1003, ¶472.

b) [1.a]

Figure 12 discloses semiconductor (silicon) substrate 1:

FIG. 12

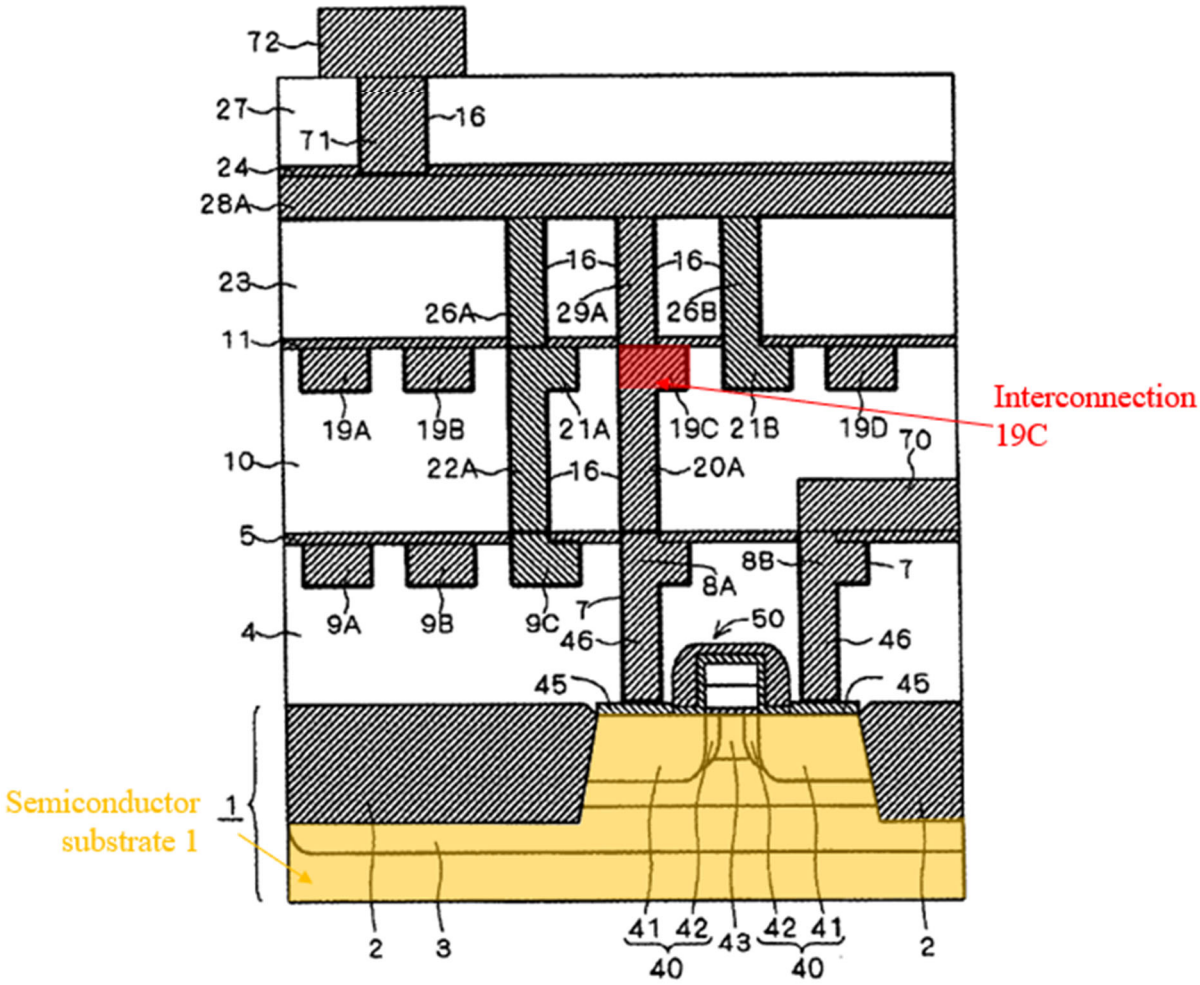


TSMC-1007, 10:50-55, 20:9-11; TSMC-1003, ¶473.

c) [1.b]

Figure 12 discloses a first interconnect (e.g., "interconnection 19C") formed on semiconductor substrate 1:

FIG. 12

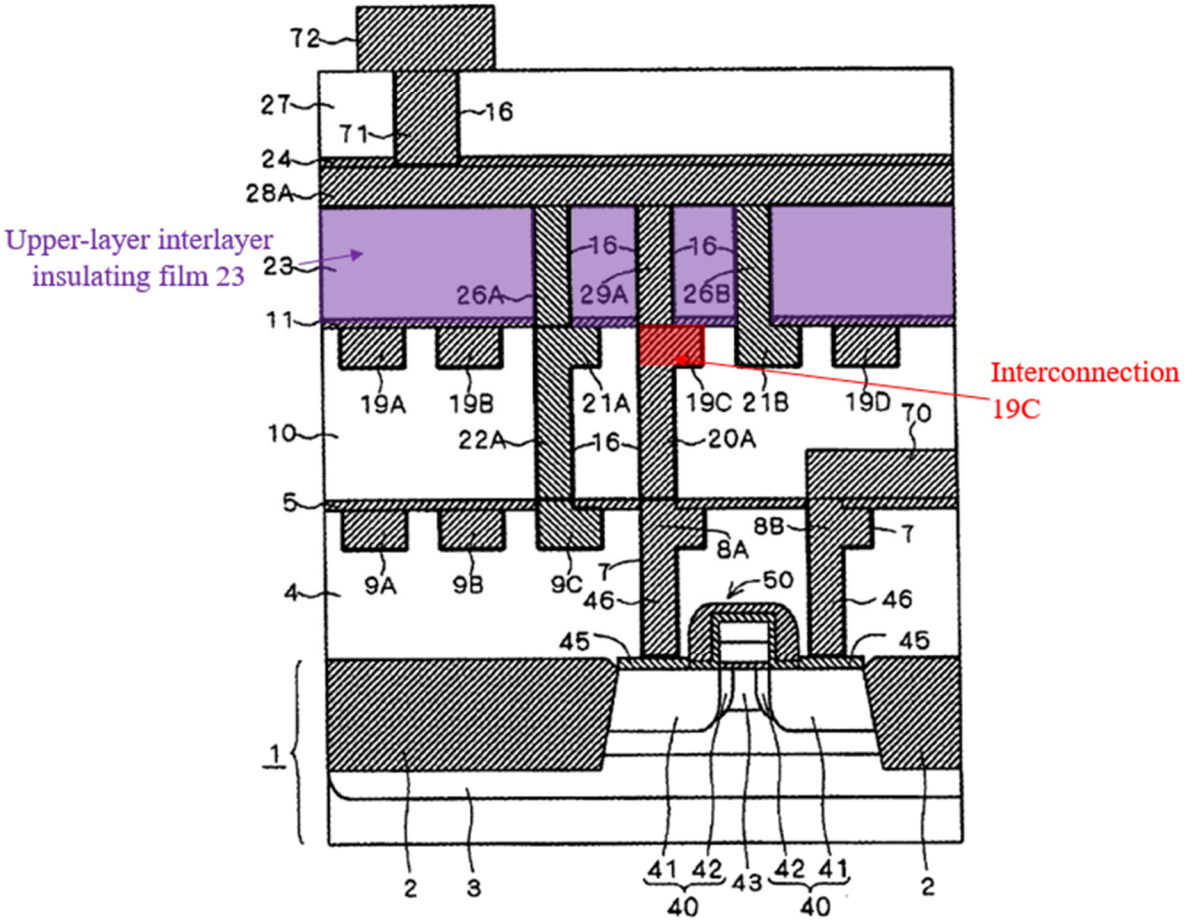


TSMC-1007, 20:15-49; TSMC-1003, ¶¶474-75.

d) [1.c]

Figure 12 discloses a first insulating film (e.g., "upper-layer interlayer insulating film 23") formed on first interconnect 19C:

FIG. 12

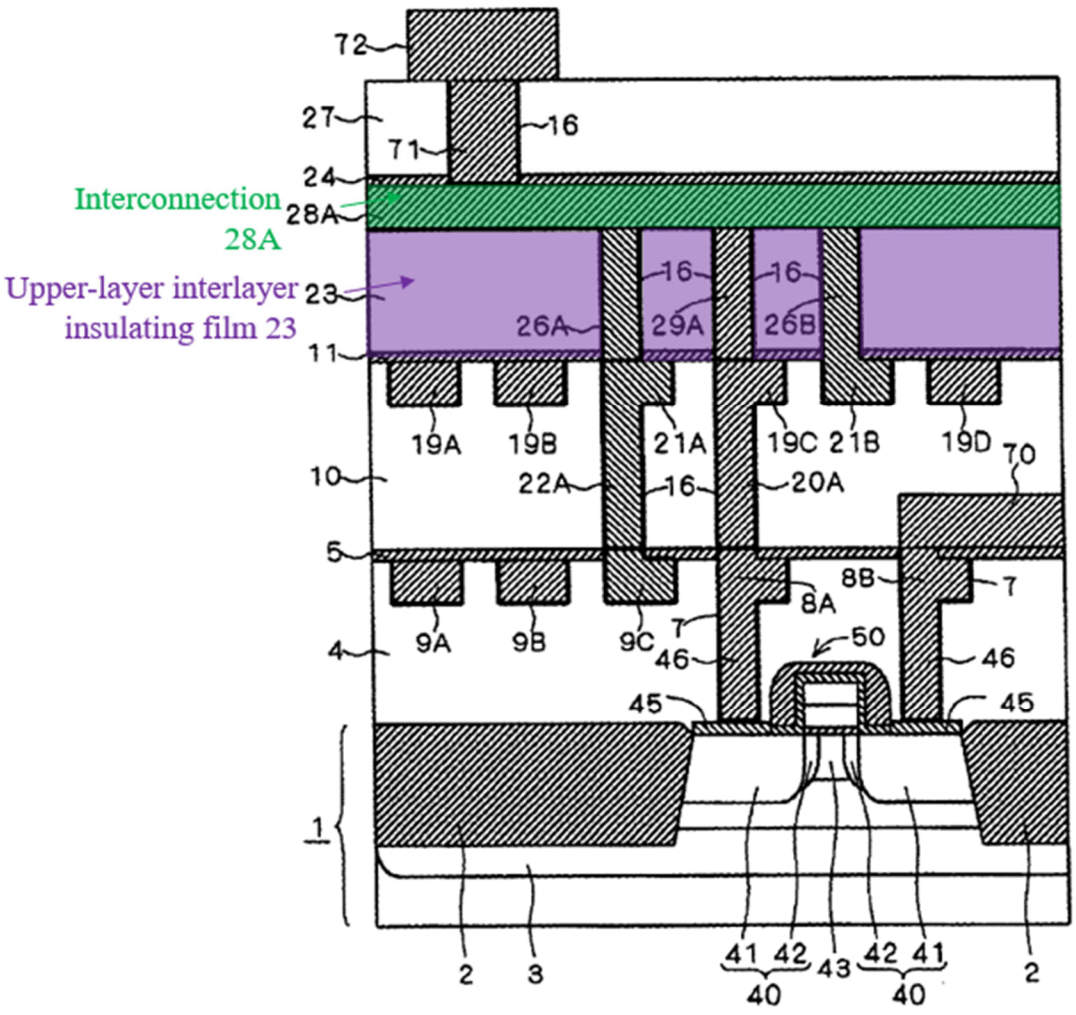


TSMC-1007, 12:47-51, 20:9-11; TSMC-1003, ¶¶476-77. The "first insulating film" can include or omit insulating film 11 lying just below film 23. *Id.*, ¶477.

e) [1.d]

Figure 12 discloses a second interconnect (e.g., "interconnection 28A") formed on insulating film 23:

FIG. 12

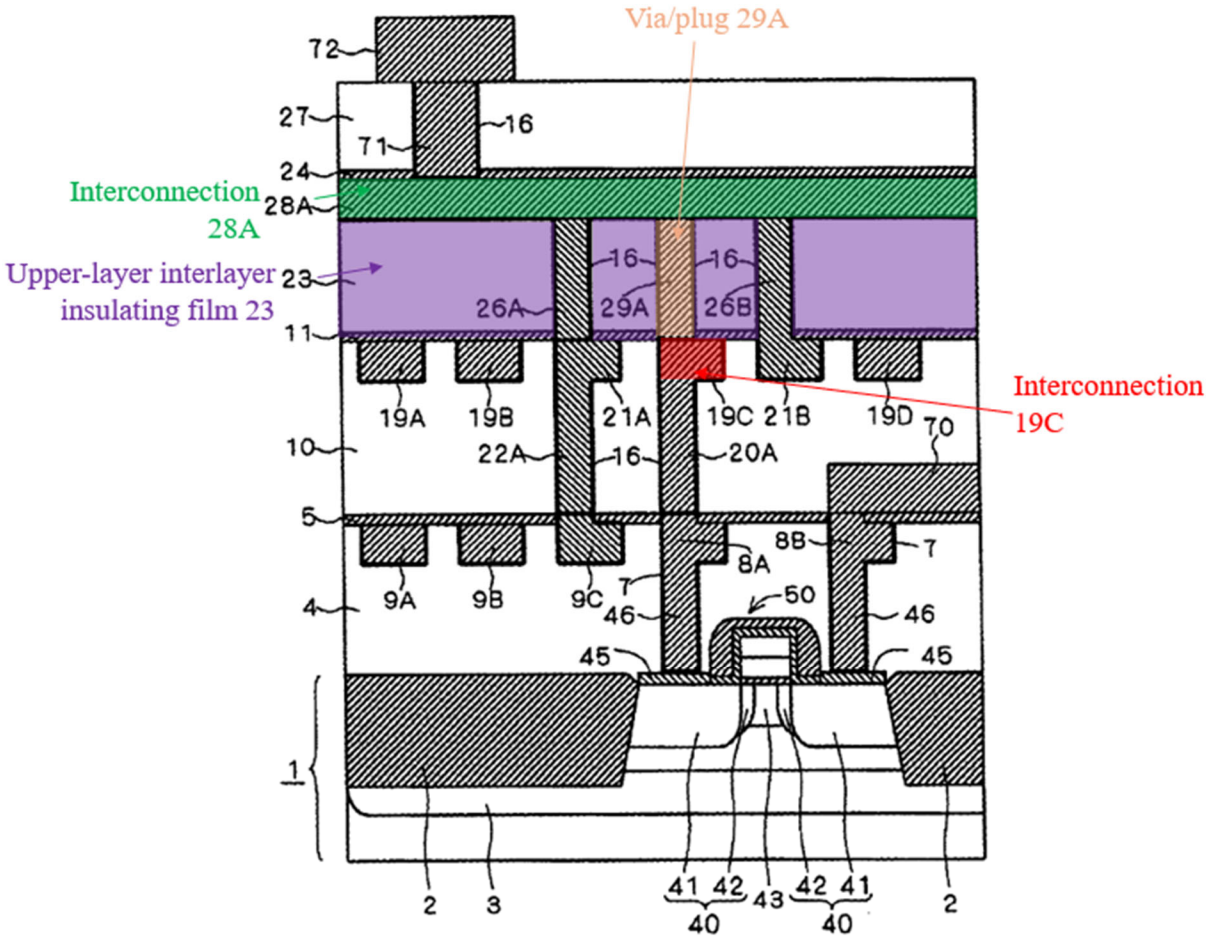


TSMC-1007, 12:47-51, 20:9-24; TSMC-1003, ¶¶478-80.

f) [1.e]

Figure 12 discloses a via (e.g., "plug 29A") formed through insulating film 23, and connecting first interconnect 19C and second interconnect 28A:

FIG. 12

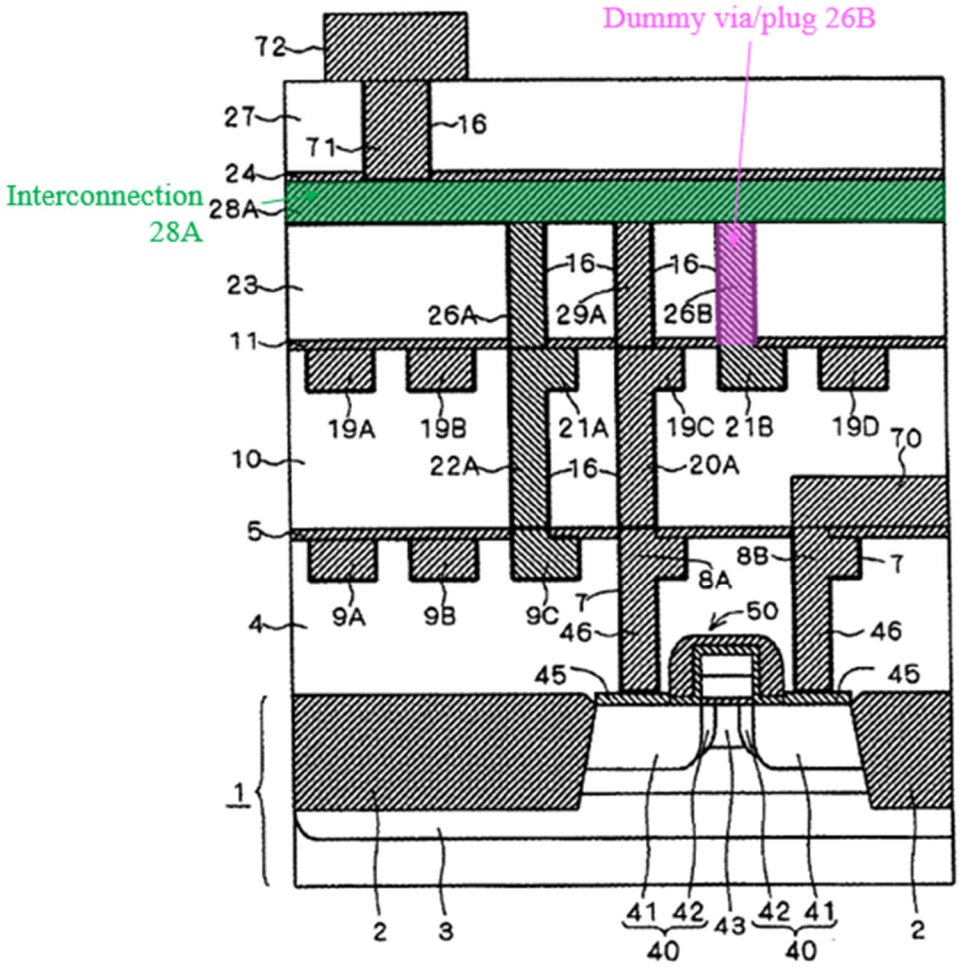


TSMC-1007, 12:47-51, 20:9-19; TSMC-1003, ¶¶481-82.

g) [1.f]

Figure 12 discloses a dummy via (e.g., "dummy plug 26B") connected to second interconnect 28A:

FIG. 12



TSMC-1007, 12:47-51, 20:32-34; TSMC-1003, ¶¶483-87. Figure 12's dummy plug 26A is another dummy via connected to second interconnect 28A. TSMC-1003, ¶484.

h) [1.g]

Kunikiyo's dummy vias 26A, 26B are each made of copper, a conductive film. TSMC-1007, 12:7-51, 20:9-11, Figs. 4-6, 12. Kunikiyo's Figures 3-6 illustrate a dual damascene process, where through holes 12, interconnect trenches 14, and dummy interconnect trenches 15 are filled with barrier metal 16 and then copper 17. *Id*., 5:42-46, 11:37-12:41. Kunikiyo teaches that "the dual damascene method is performed again, thus forming upper-layer interconnections 25 (25a, 25b)…and plugs 26 (26a to 26c)…in the upper-layer interlayer insulating film 23." *Id*., 12:47-51. Dummy plugs 26A and 26B ("dummy vias") are made of copper ("conductive film") when the dual damascene method "is performed again." TSMC-1003, ¶¶488-89.

Kunikiyo's dummy structures, including dummy vias 26A and 26B, do not contribute to the function of the MOSFET device, as both ends never connect to elements that actively participate in circuit operation. TSMC-1007, 5:51-59, 11:53-56, 13:63-14:3, 14:31-33, 20:29-37, 25:54-26:9. Kunikiyo explains:

> A dummy interconnection is an interconnection which is not directly related to the circuit operation of the semiconductor device and whether they are present or absent makes no difference on the circuit diagram of the semiconductor device.

Id., 25:59-63. Kunikiyo's device would be operable even if Kunikiyo's dummy vias/dummy interconnects were omitted. *Id*.; *cf.* TSMC-1001, 3:14-18; 10:26-32.

Such dummy structures, by their stated definition and purpose in Kunikiyo, do not carry current to operate the semiconductor device. TSMC-1003, ¶¶490-93. Thus, Kunikiyo's dummy vias are arranged so as to be incapable of having current flow therethrough. *Id*.

i) [1.h]/[1.i]

Kunikiyo discloses using the dual damascene process for forming its interconnects and vias/dummy vias. TSMC-1007, 11:48-12:51, 20:9-24, Figs. 3-7, 12. Figures 3-6 detail the process steps for an earlier/lower level, showing the formation of through-holes 12 and interconnection trenches 14, which are then filled with barrier metal 16 and copper 17:

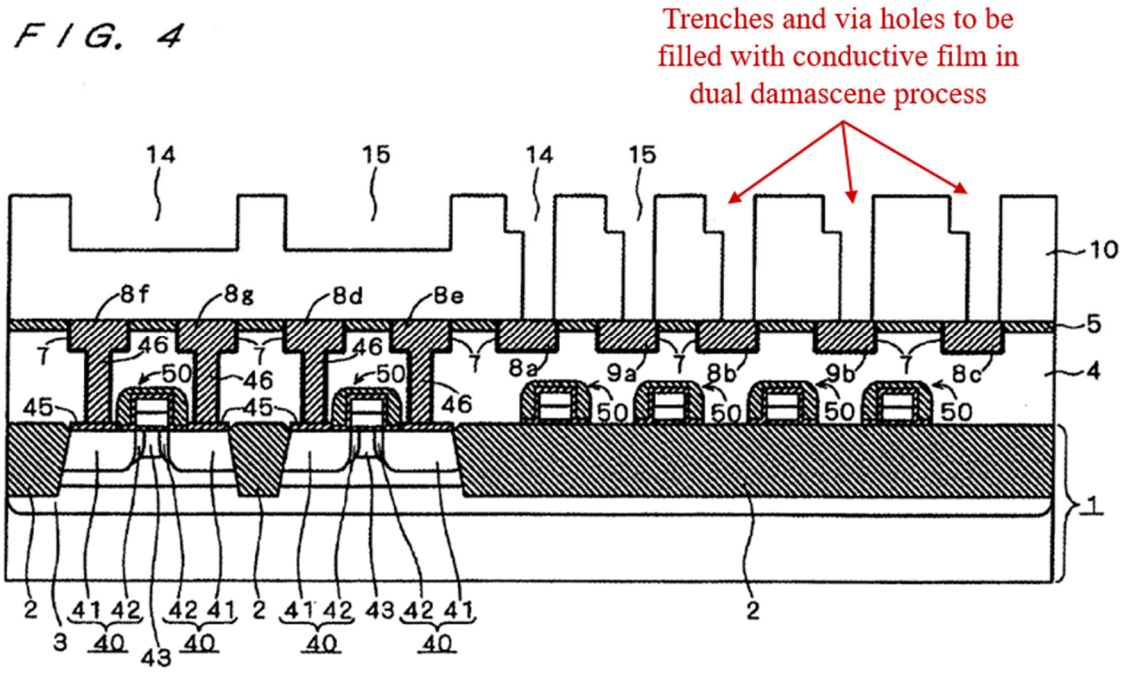
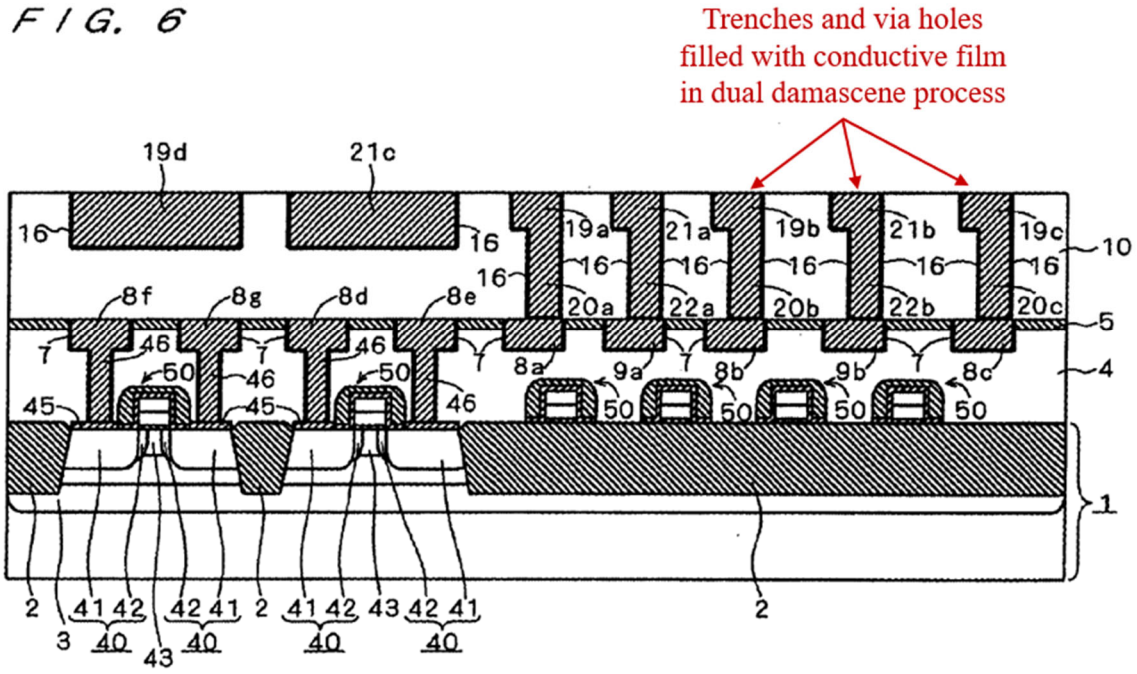


FIG. 6



Id.; TSMC-1003, ¶¶494-95. Kunikiyo then states, "[i]n the process step of FIG. 7, the dual damascene method is performed again, thus forming upper-layer interconnections 25 (25a, 25b), 28 (**28a** to 28d) and plugs 26 (**26a to 26c**), 29 (**29a** to 29c) in the upper-layer interlayer insulating film 23." TSMC-1007, 12:47-51. Figure 12's via 29A, dummy vias 26A and 26B, and second interconnect 28A are among the listed upper-layer structures formed by this dual damascene process. *Id.*, 12:47-51, 20:9-24, Figs. 12, 22.

Accordingly, via 29A, dummy vias 26A and 26B, and second interconnection 28A in the Figure 12 embodiment are formed simultaneously using the dual damascene technique, where the trench for second interconnect 28A and the holes for via 29A and dummy vias 26A and 26B are patterned in insulating

film 23 and then filled with conductive material (barrier metal 16, copper 17) in the same deposition and planarization steps. TSMC-1003, ¶¶495-99.

Thus, Kunikiyo's Figure 12 device discloses second interconnect 28A and via 29A, and second interconnect 28A and dummy vias 26A and 26B, as dual damascene structures. *Id*.

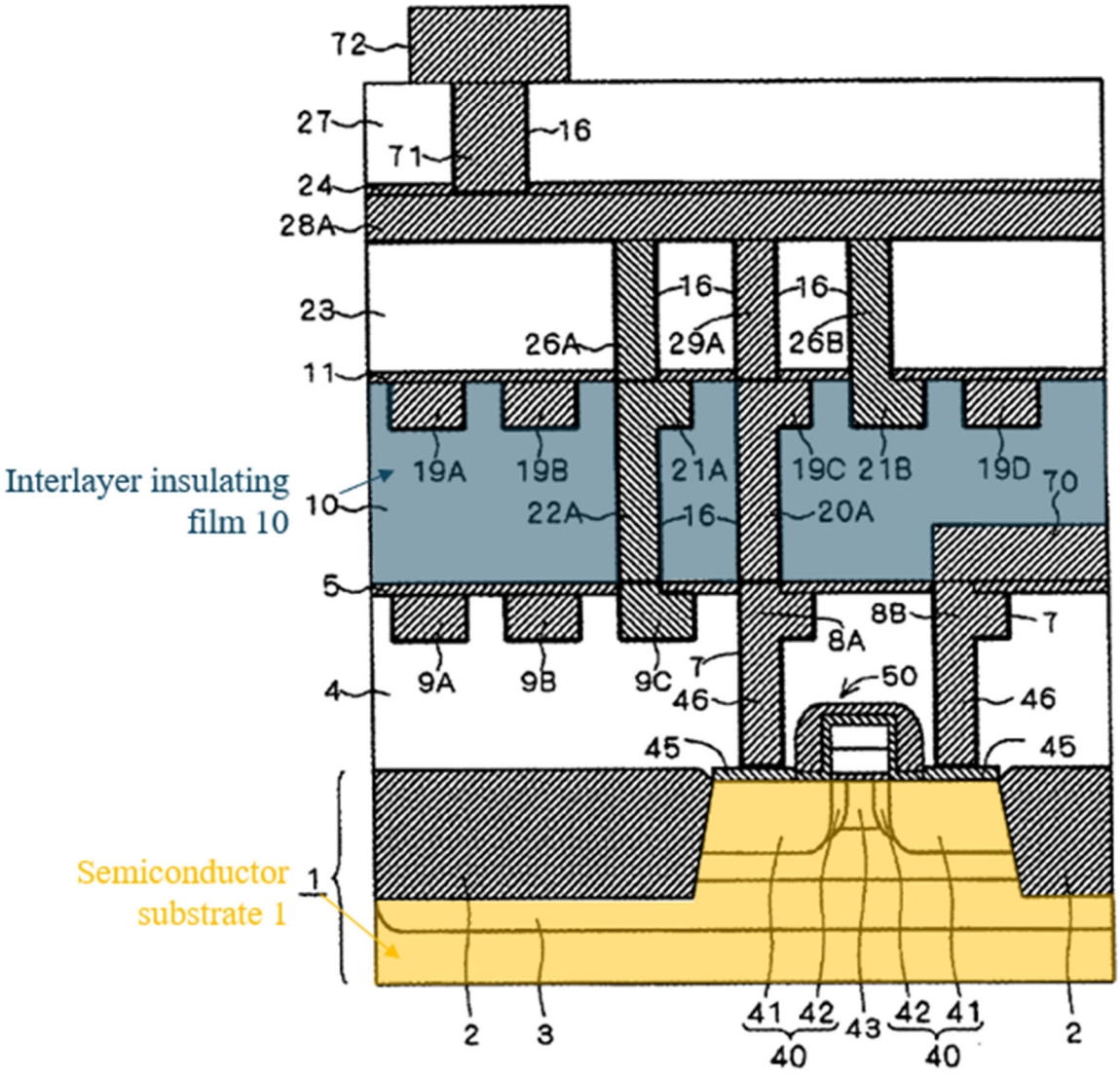
Additionally, it was obvious to form the vias and dummy vias as dual damascene structures with the second interconnect, for the reasons previously explained. *Supra*, §§VI.G.1, VI.G.2.(i); TSMC-1003, ¶500. A POSITA would have expected success because the dual-damascene process was well-known, widely used, and taught in Kunikiyo. *Id*.; TSMC-1007, 11:48-12:51, 20:9-24, Figs. 3-6.

3. Claim 2

a) [2.a]

Kunikiyo's Figure 12 discloses a second insulating film (e.g., "interlayer insulating film 10") formed on semiconductor substrate 1:

FIG. 12

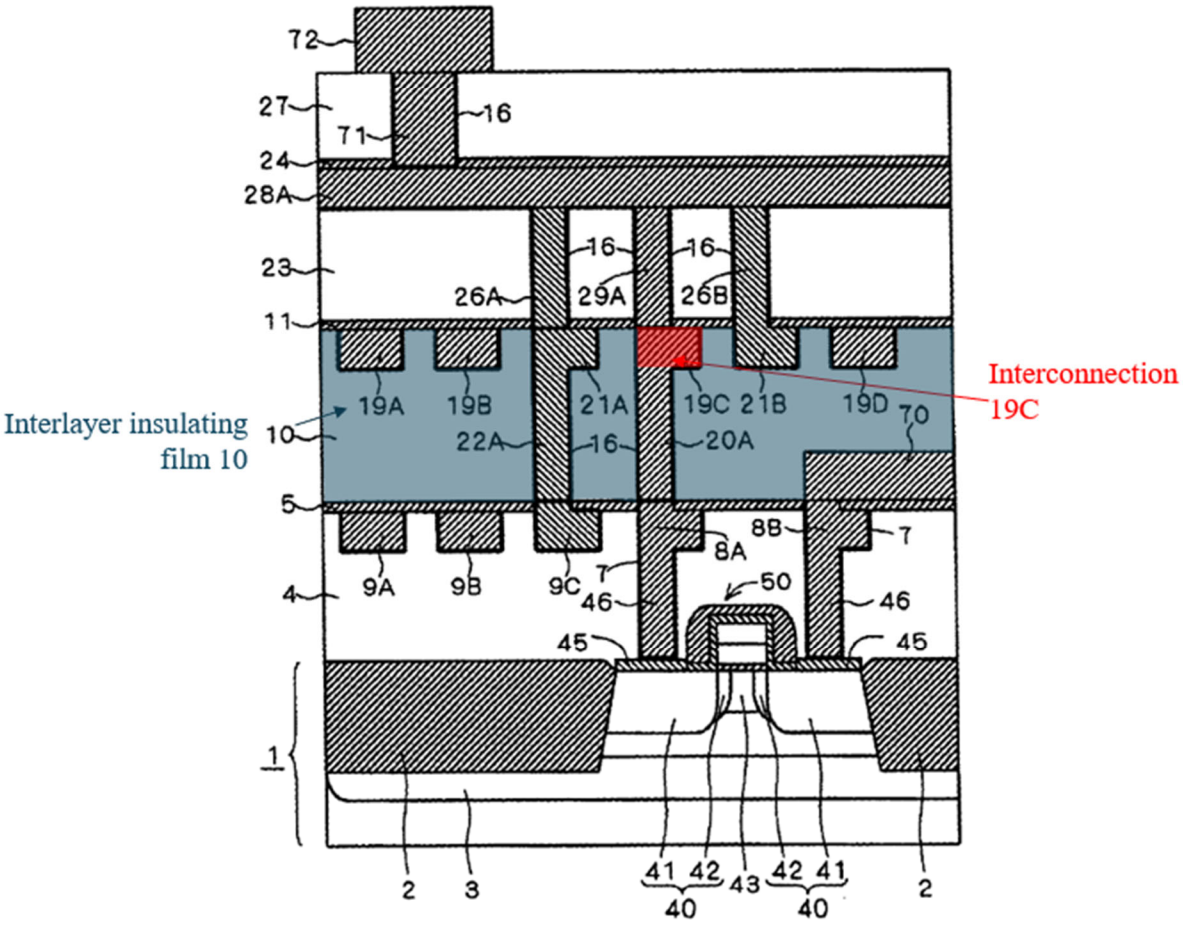


TSMC-1007, 10:50-55, 11:36-37; TSMC-1003, ¶¶501-02.

b) [2.b]

Kunikiyo's Figure 12 discloses that the first interconnect (e.g., interconnection 19C) is formed on the second insulating film (interlayer insulating film 10):

FIG. 12

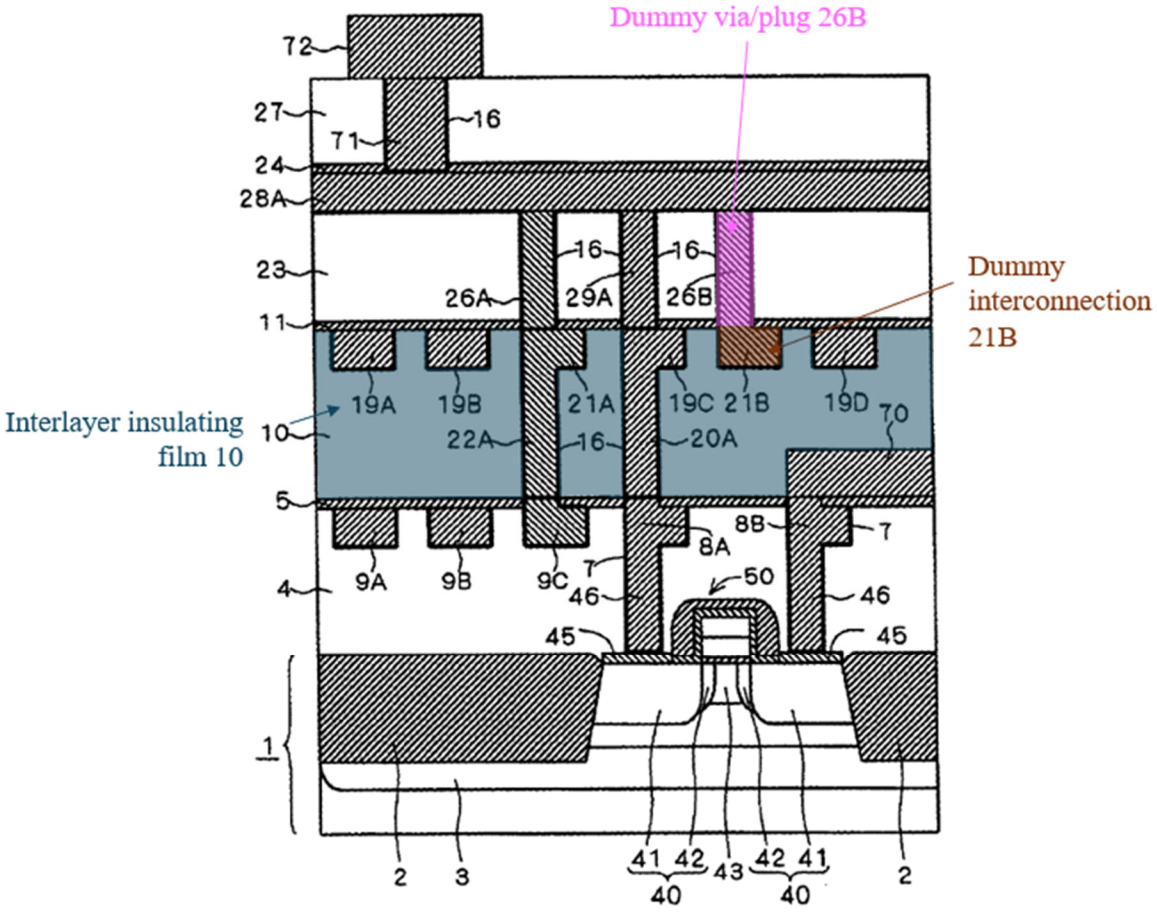


TSMC-1007, 11:38-12:30, 20:15-24: TSMC-1003, ¶¶503-04.

c) [2.c]

Kunikiyo's dummy via 26B is connected to first dummy interconnection 21B which is formed on second insulating film (interlayer insulating film 10):

FIG. 12



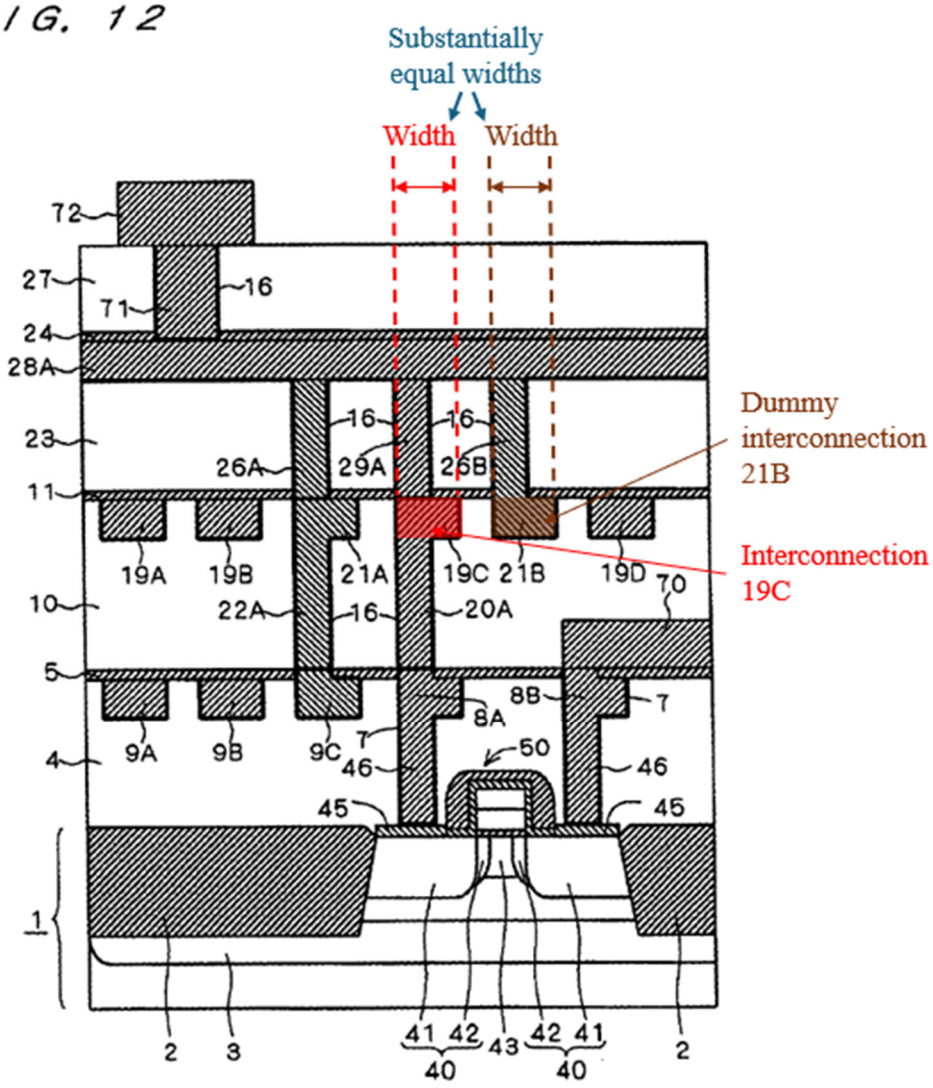
TSMC-1007, 11:38-12:30, 20:25-37, Fig. 12; TSMC-1003, ¶¶505-06. Dummy via 26A is likewise connected to dummy interconnection 21A formed on second insulating film 10. *Id.*

Kunikiyo's structures 21A and 21B are "dummy" interconnects for the same reasons as explained for dummy vias 26A, 26B. *Supra*, §VI.I.2.(h); TSMC-1003, ¶507.

4. Claim 4

Kunikiyo's Figure 12 shows first interconnect (interconnection 19C) and first dummy interconnect (dummy interconnection 21B), with each having identical widths:

FIG. 12

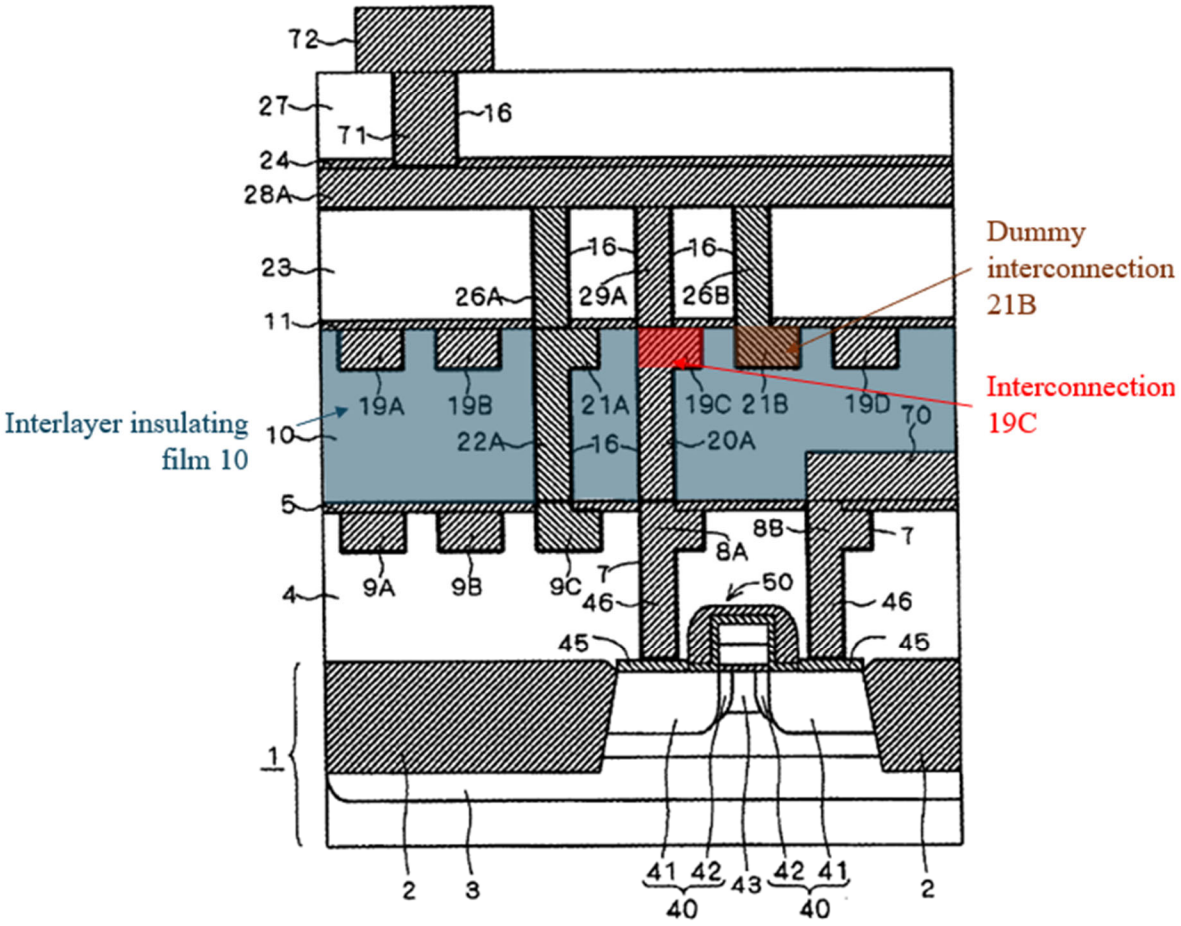


TSMC-1007, 11:48-56, 20:7-34; TSMC-1003, ¶¶508-09. Kunikiyo's figures are intended to show the relative widths of the structures shown therein, as evidenced by Kunikiyo's recognition of Figure 9 specifically discloses the alternating widths of interconnect 25B. *Id*., 15:11-35; TSMC-1003, ¶510. Thus, when Kunikiyo wanted to show structures having different widths, it showed them as such, which reinforces that Kunikiyo's structures having identical widths were intended to convey exactly that. TSMC-1003, ¶510.

5. Claim 7

Kunikiyo's Figure 12 shows the first interconnect (interconnection 19C) and the first dummy interconnect (dummy interconnection 21B) buried in an upper portion of the second insulating film (interlayer insulating film 10):

FIG. 12

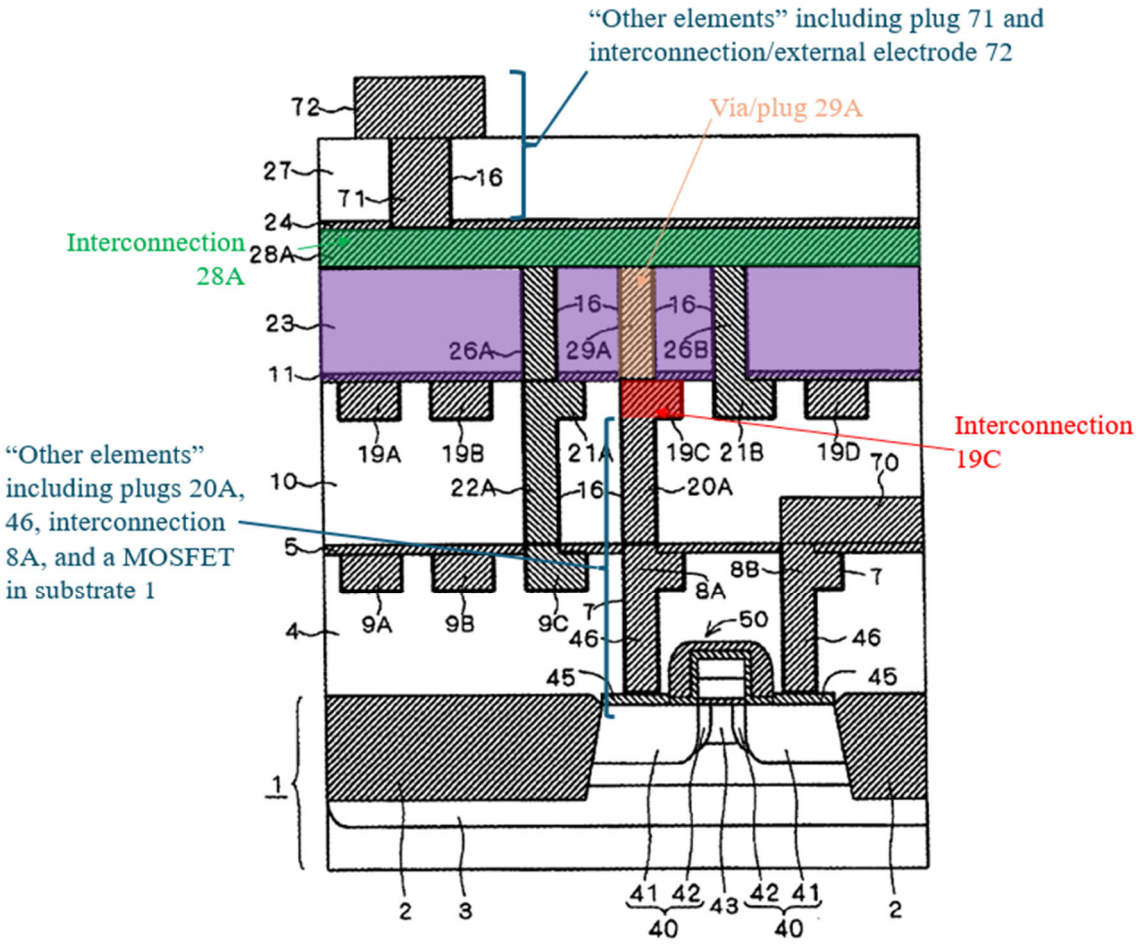


TSMC-1007, 11:48-56, 20:7-34; TSMC-1003, ¶¶511-12. They are positioned at the top of this film, directly beneath the next layer, which places them in the "upper portion" of interlayer insulating film 10. *Id.*, 11:36-12:30, 20:7-34, Fig. 12; TSMC-1003, ¶512.

6. Claim 14

Kunikiyo's Figure 12 shows the first interconnect (interconnection 19C) and the second interconnect (interconnection 28A) connected to another element or an external electrode, which include plugs 20A, 46, and 71, interconnection 8A, interconnection/external electrode 72, and the MOSFET device built into the semiconductor substrate:

FIG. 12

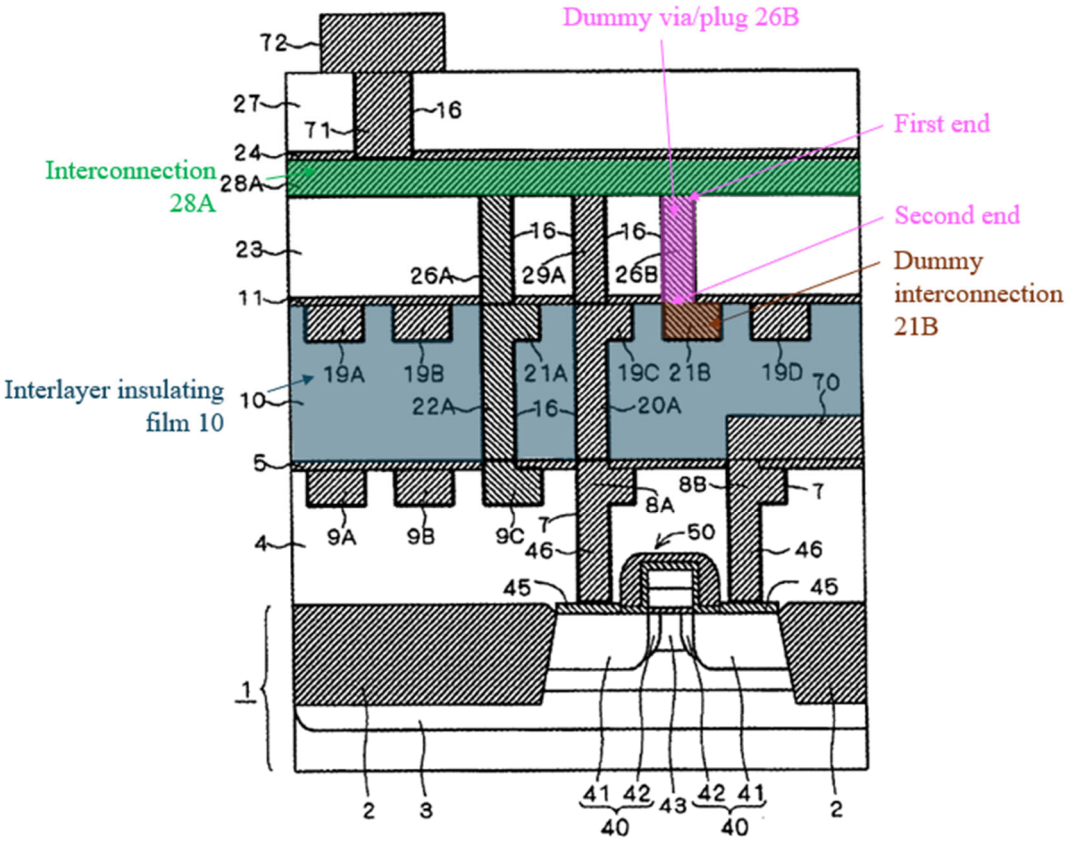


TSMC-1007, 10:50-14:67, 20:4-21:21, Figs, 12, 14; TSMC-1003, ¶¶513-14.

7. Claim 42

Kunikiyo's Figure 12 shows the dummy via (dummy plug 26B) as a vertical conductive structure with a top (first) end and a bottom (second) end. TSMC-1007, Fig. 12. Dummy plug 26B's top end is connected to the second interconnect (interconnection 28A), and the bottom end is connected to the first dummy interconnect (dummy interconnection 21B). *Id*. Further, dummy interconnect 21B is buried within, and therefore surrounded by, the second insulating film (interlayer insulating film 10):

FIG. 12



TSMC-1003, ¶¶515-16.

J. Ground 10: Claims 9 and 17 Are Obvious Over Kunikiyo and Iizuka

Kunikiyo and Iizuka render claims 9 and 17 obvious. TSMC-1003, ¶¶517-36.

1. Claims 9, 17

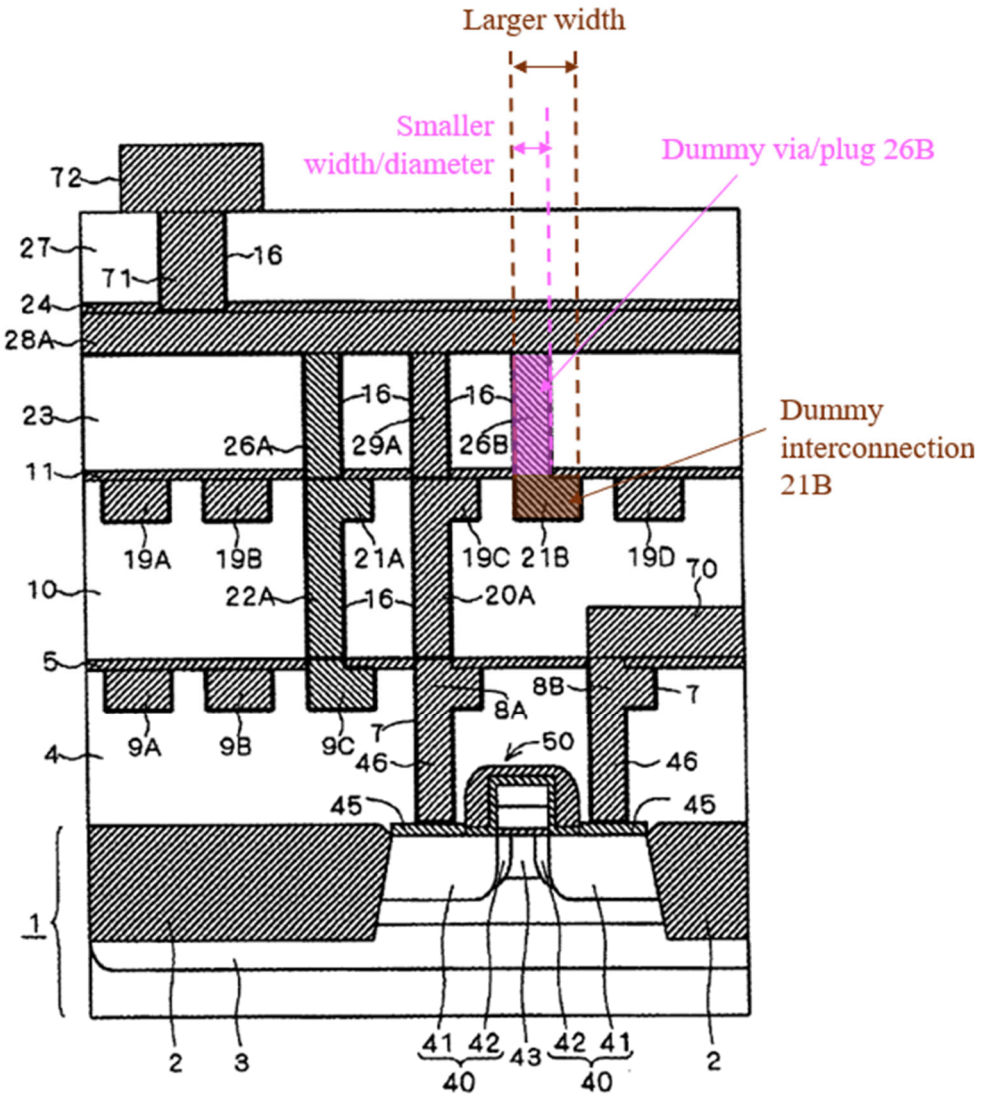
a) [9.a]/17

Vias/dummy vias with circular cross-sectional shapes were well-recognized in the art, as expressly taught by Iizuka. *Supra*, §VI.C.1; *see also* TSMC-1005, Figs. 19A, 22A (showing circular dummy vias); TSMC-1013, 8:47-52 (recognizing circular dummy-via shapes); TSMC-1014, ¶[0091] (designating circular vias as a default shape); TSMC-1003, ¶¶518-20. Kunikiyo also teaches that its dummy structures may be built with various shapes. TSMC-1007, 25:67-26:4.

b) [9.b]

Kunikiyo's dummy via (e.g., dummy plugs 26B, 26A) has a smaller diameter than the first dummy interconnect (e.g., dummy interconnections 21B, 21A):

FIG. 12



TSMC-1007, 20:25-34, Fig. 12; TSMC-1003, ¶¶525-29. Dummy plug 26A also has a width smaller than the width of dummy interconnection 21A. *Id.*

As explained previously, Kunikiyo's Figure 12 portrays the relative width of dummy interconnection 21B in relation to dummy via 26B (and similar for dummy interconnection 21A/dummy via 26A) along the cross-section shown. *Supra*, §VI.I.4.

Accordingly, when dummy plug 26B (or dummy plug 26A) is made circular per Iizuka's teaching, the diameter of dummy plug 26B would be smaller than a width of the first dummy interconnect ("dummy interconnection 21B"). TSMC-1003, ¶¶528-29.

2. Combination of Kunikiyo and Iizuka

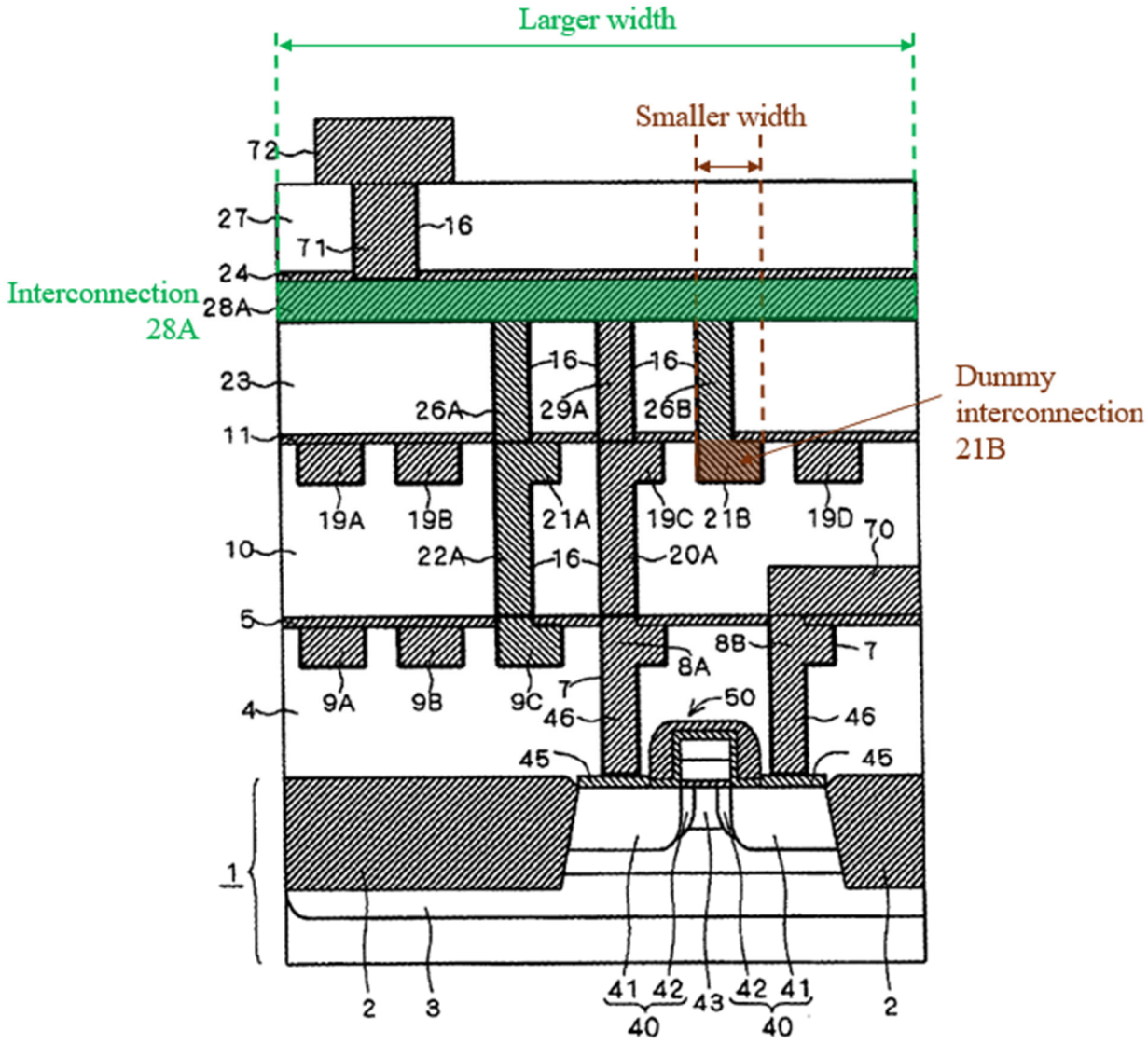
A circular via shape was a well-known design choice, subject to routine optimization as noted by the Examiner (TSMC-1002, 244-45, 292-96). TSMC-1005, Figs. 19A, 22A; TSMC-1013, 8:47-52; TSMC-1014, ¶[0091]; TSMC-1003, ¶¶519-20, 523-24. Circular shapes also have potential advantages. *Supra*, §§VI.C.5; TSMC-1038, 7:61-67; TSMC-1003, ¶¶521-22. This applies equally to vias and dummy vias. *Id*.

Moreover, a circular via/dummy via shape does not alter the fundamental function of Kunikiyo, and forming Kunikiyo's vias/dummy vias as circular was readily achievable with known fabrication techniques. TSMC-1003, ¶¶522, 524. Therefore, a POSITA would have expected success when implementing Kunikiyo's vias/dummy vias with a circular cross-sectional shape having a diameter smaller than Kunikiyo's dummy interconnect. *Id*.

K. Ground 11: Claim 3 Is Obvious Over Kunikiyo and Watanabe

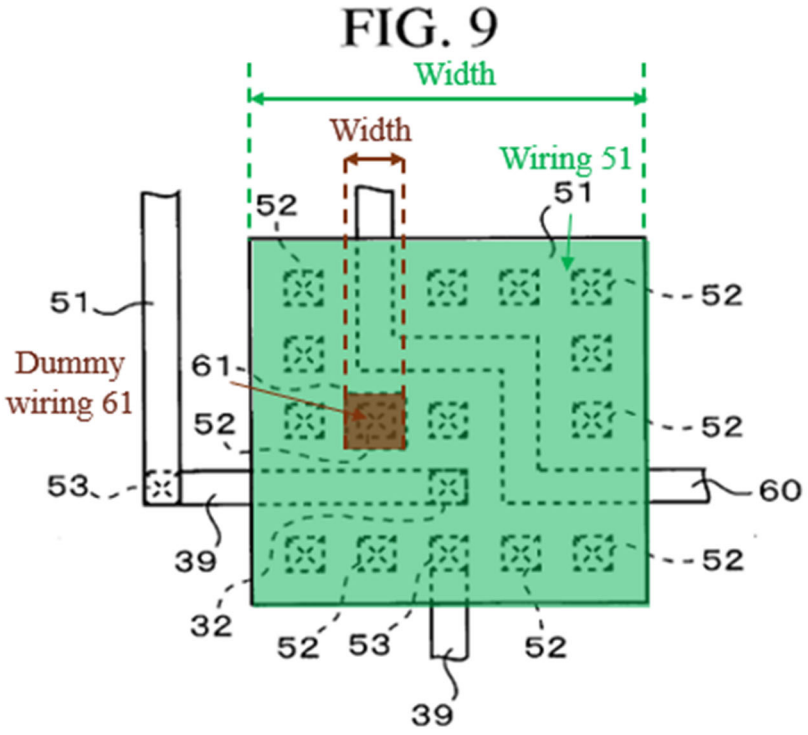
Kunikiyo and Watanabe render claim 3 obvious. TSMC-1003, ¶¶537-47. Kunikiyo teaches a dummy interconnect 21B having a smaller width than the second interconnect 28A:

FIG. 12



TSMC-1003, ¶¶537-39.

Additionally, Watanabe teaches second interconnect widths larger than dummy interconnect widths, as exemplified in Watanabe's Figure 9:



Supra, §VI.A.4. Watanabe demonstrates that dummy interconnects having smaller widths than the second interconnects was a mere design choice, and a simple substitution to implement in Kunikiyo's device. TSMC-1003, ¶¶540-42. Indeed, the '623 patent teaches no criticality associated with these relative widths. *Id*.

A POSITA was motivated to use such relative widths to provide more space on the second interconnect for vias connecting to other circuit elements, as illustrated in Watanabe's Figure 9. *Id*., ¶¶543-46. Kunikiyo's Figure 12 shows the same, with second interconnect 28A connected to via 29A and dummy vias 26A,

26B. *Id*. A POSITA was further motivated because smaller-width dimensions are generally required at lower levels in the interconnect structure to achieve a greater concentration/density of wiring. *Id*.; TSMC-1034, 585-86, 591, Figs. 12-17, 12-18. Dummy interconnects and active wires at lower levels should maintain the same dimensions to maintain pitch requirements and allow for efficient routing and wiring density. TSMC-1003, ¶545. In contrast, higher-level interconnects typically carry more current and must dissipate more heat, requiring relatively wider interconnects. *Id*.; TSMC-1012, 34; TSMC-1034, 594. Accordingly, it was a simple design choice—one encouraged by existing design parameters for widths of lower-level wirings (including dummy interconnects)—for dummy interconnects to have a smaller width than the second interconnect. TSMC-1003, ¶¶541, 546.

A POSITA would have expected success because this modification merely required adjusting the relative sizes of the dummy and second interconnects, which was easily achievable using then-standard processing techniques. *Id*., ¶547; *see also* TSMC-1016, 6:14-29; TSMC-1028, 5458.

VII. GROUNDS FOR STANDING

Petitioner certifies that the ’623 patent is available for review, and Petitioner is not barred/estopped from requesting review on the grounds identified herein.

VIII. MANDATORY NOTICES

A. Real Party-In-Interest

The real party-in-interest here is Taiwan Semiconductor Manufacturing Company Limited.

B. Related Matters

The '623 patent is asserted in *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Case No. 2:25-cv-00324 (E.D. Tex.).

C. Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3) and 42.10(a), Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. §42.10(b), a Power of Attorney accompanies this Petition.

Lead Counsel	Back-Up Counsel
Michael Houston Reg. No. 58,486 **FOLEY & LARDNER LLP** 321 North Clark Street, Suite 3000 Chicago, Illinois 60654 312-832-4500 mhouston@foley.com	Pavan Agarwal Reg. No. 40,888 **FOLEY & LARDNER LLP** 3000 K Street N.W., Suite 600 Washington, DC 20008 202-672-5300 pagarwal@foley.com Nicholas Lagerwall Reg. No. 63,272 **FOLEY & LARDNER LLP** 150 East Gilman Street, Suite 5000 Madison, Wisconsin 53703 608-257-5035

Lead Counsel	Back-Up Counsel
	nlagerwall@foley.com

Petitioner consents to electronic service directed to the following email address: Foley_TSMC_623-1_IPR2025-01212@foley.com.

IX. PAYMENT OF FEES

The Office is authorized to charge fees for this Petition to Deposit Account No. 19-0741. Any additional fees that might be due are also authorized.

X. CONCLUSION

For the reasons given above, Petitioner requests IPR be instituted for the challenged claims.

Respectfully submitted,

Dated: July 25, 2025 By: */Michael R. Houston/*

Michael R. Houston
Reg. No. 58,486
FOLEY & LARDNER LLP
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS, AND TYPE STYLE REQUIREMENTS

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,991 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. §42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. §42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

Respectfully submitted,

Date: July 25, 2025 By: /*Michael R. Houston*/

Michael R. Houston
Reg. No. 58,486
FOLEY & LARDNER LLP
Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on July 25, 2025, true and correct copies of the foregoing document and supporting materials were served in its entirety on the Patent Owner at the following address of record listed on the USPTO's Patent Center via overnight service:

Michael J. Cherskov
Szymon M. Gurda
903 Commerce Dr.
Suite 310
Oak Brook, IL 60523

Courtesy copies of the same documents were served electronically on prosecution counsel and Patent Owner's litigation counsel by email at the following addresses:

ksrinivasan@susmangodfrey.com; jnelson@susmangodfrey.com;
igore@susmangodfrey.com; kdiehl@susmangodfrey.com;
brey@susmangodfrey.com; nloaiza@susmangodfrey.com;
anassar@susmangodfrey.com; rbhalla@susmangodfrey.com;
gfisk@susmangodfrey.com; andrea@millerfairhenry.com;
claire@millerfairhenry.com

Respectfully submitted,

Date: July 25, 2025 By: /*Michael R. Houston*/

Michael R. Houston
Reg. No. 58,486
FOLEY & LARDNER LLP
Counsel for Petitioner