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(54) INTERCONNECTION STRUCTURE

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(57) **ABSTRACT**

An interconnection structure includes a lower interconnection layer formed on a substrate and composed of a copper layer, an interlayer insulating layer formed on the lower interconnection layer and having a via reaching the lower interconnection layer, an upper interconnection layer electrically connected to the lower interconnection layer through the via, and composed of a copper layer formed in the interlayer insulating layer, and a barrier metal layer formed between the upper interconnection layer and the interlayer insulating layer. The barrier metal layer has an opening in a bottom portion of the via, and through that opening, the upper interconnection layer comes in direct contact with the lower interconnection layer in the bottom portion of the via. Thus, an interconnection structure suppressing concentration of voids in an interconnection under a via due to stress migration can be attained.

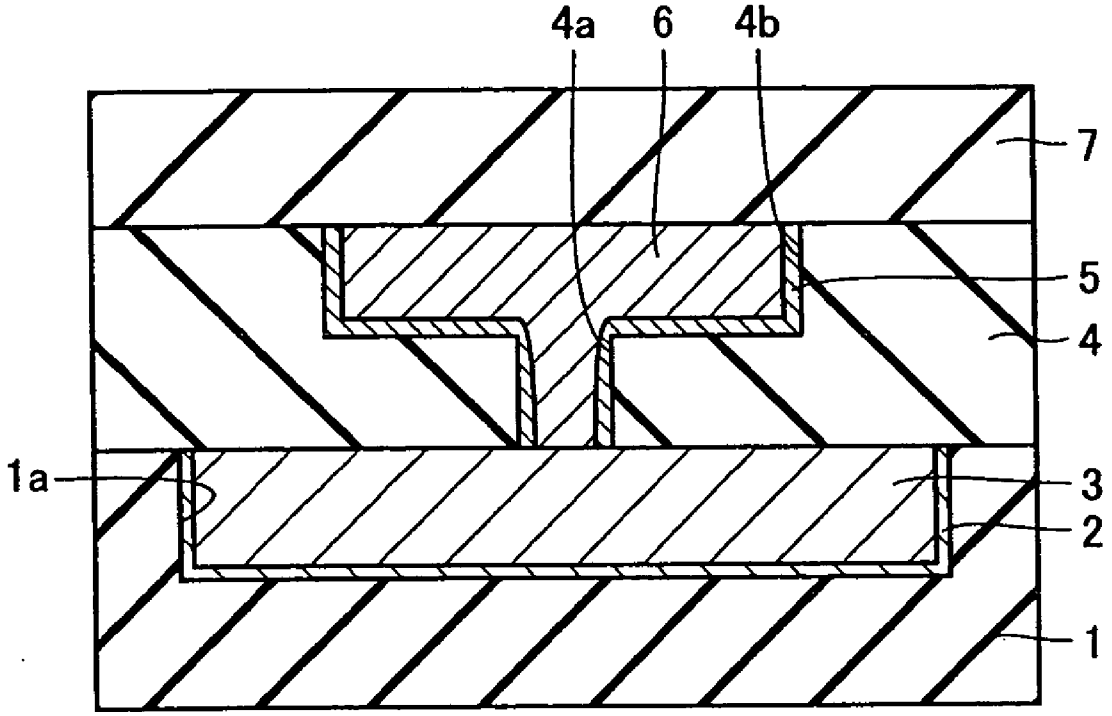


FIG.1

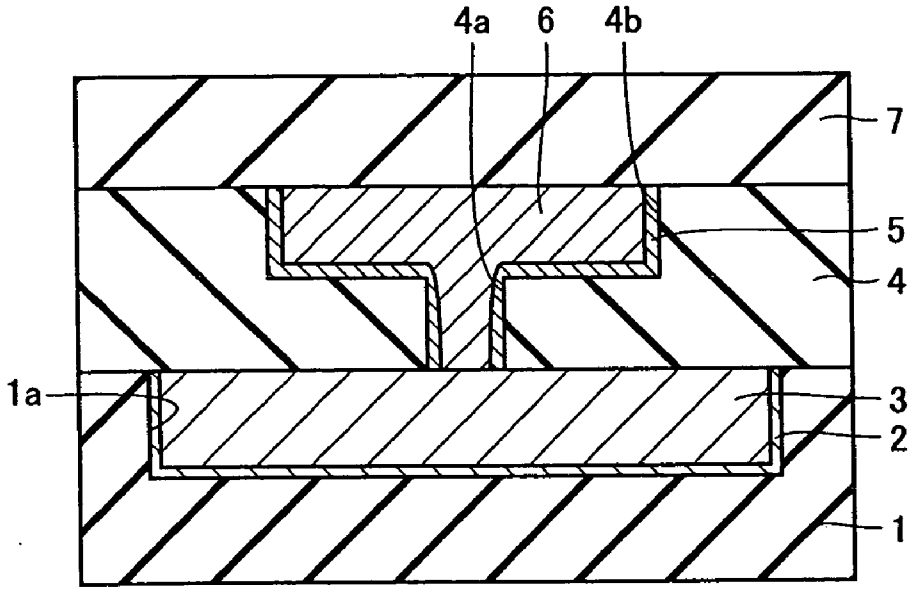


FIG.2

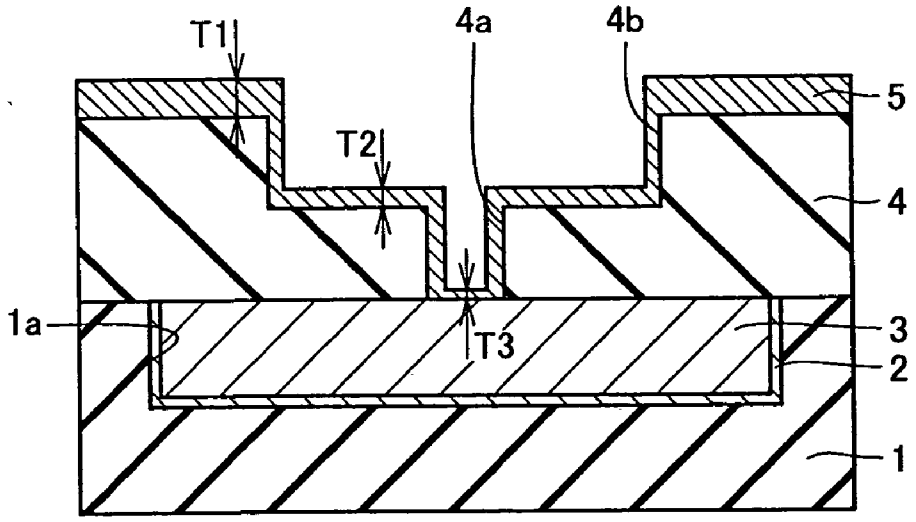


FIG.3

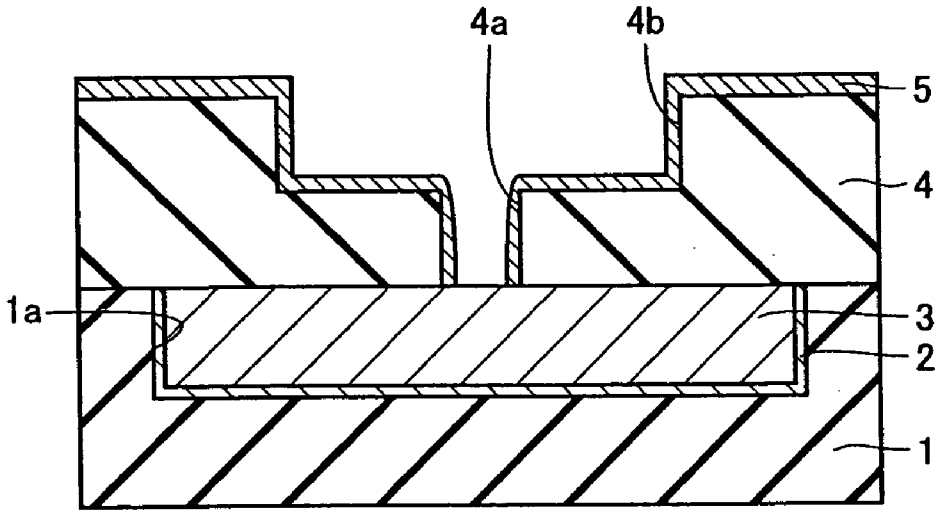


FIG.4

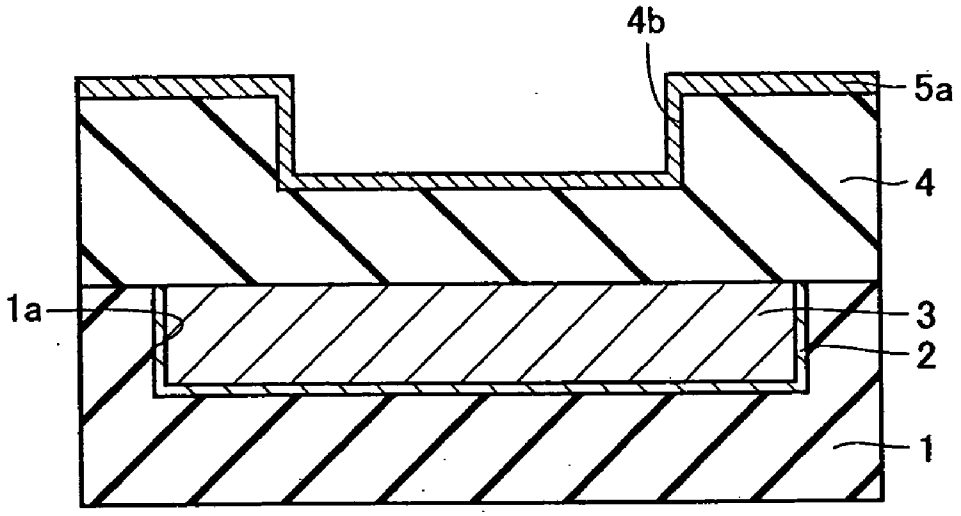


FIG.5

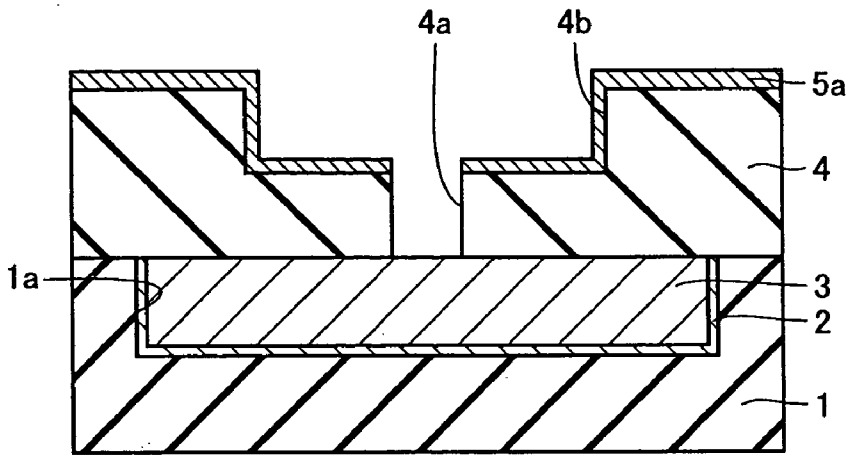


FIG.6

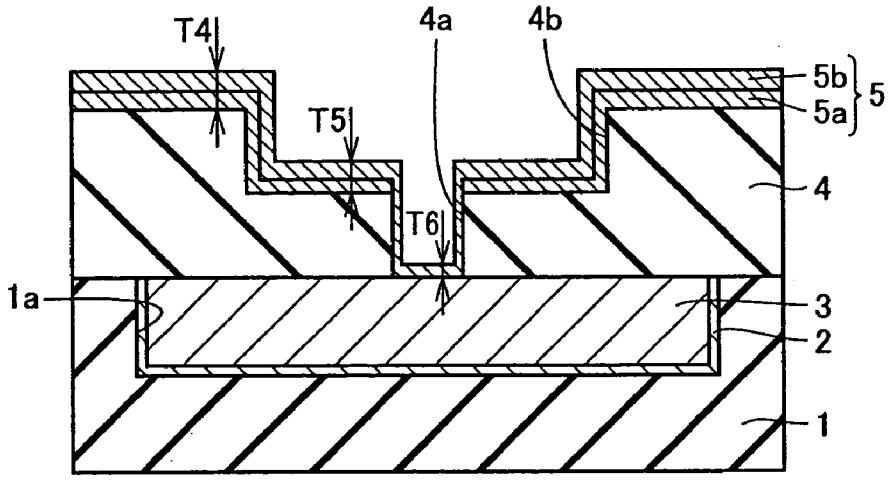


FIG.7

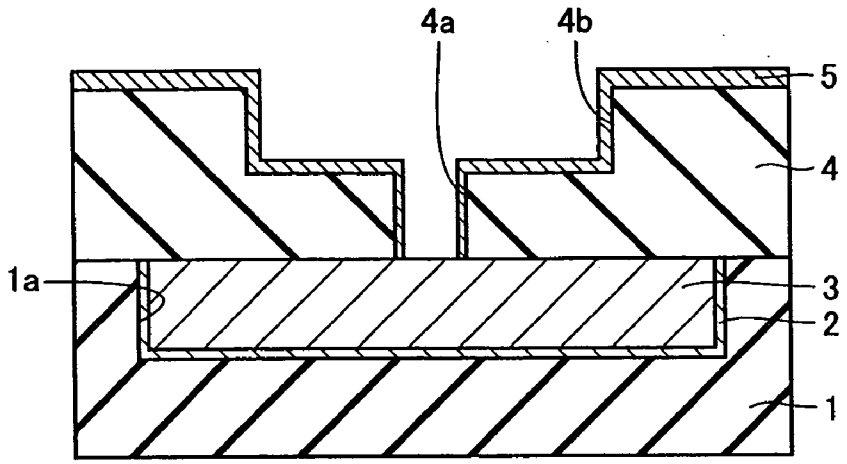

4a
4b
5
4
1a
3
2
1

FIG.8

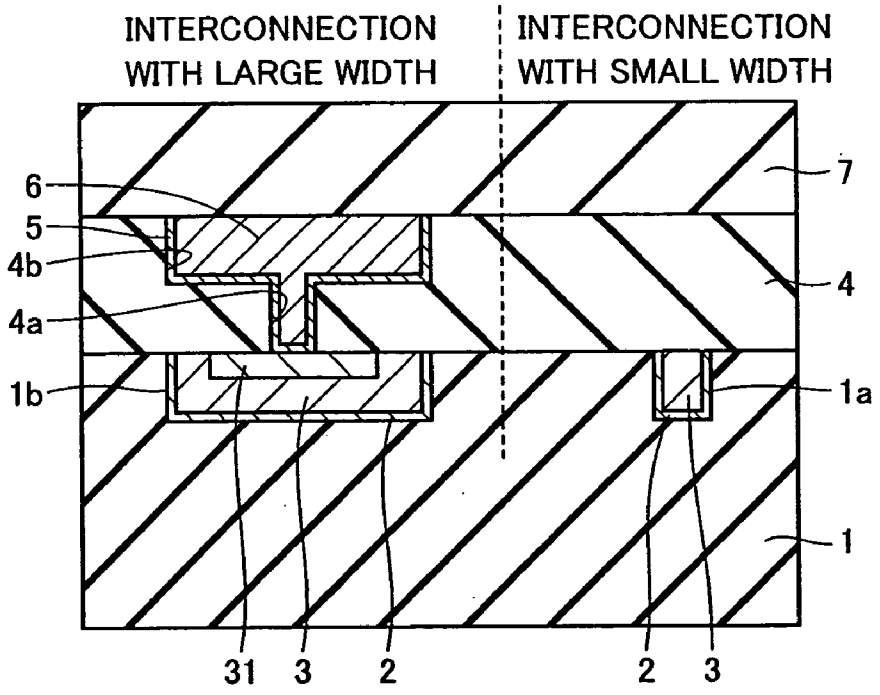

INTERCONNECTION WITH LARGE WIDTH
INTERCONNECTION WITH SMALL WIDTH
6
5
4b
4a
1b
7
4
1a
1
31
3
2
2
3

FIG.9

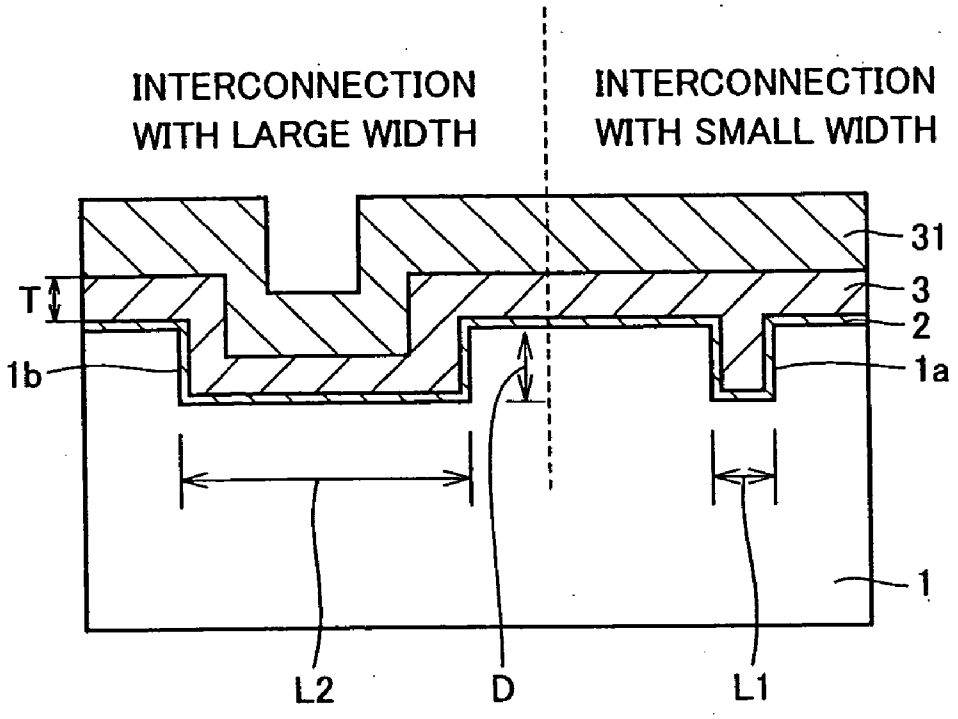

INTERCONNECTION WITH LARGE WIDTH
INTERCONNECTION WITH SMALL WIDTH
31
3
2
1a
1b
T
1
L2
D
L1

FIG.10

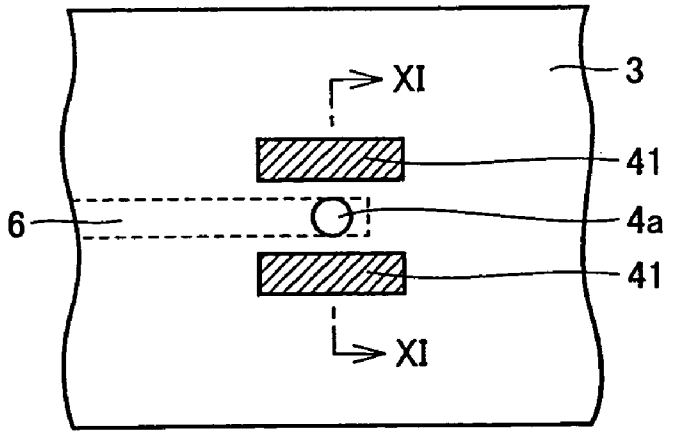

XI
3
41
6
4a
41
XI

FIG.11

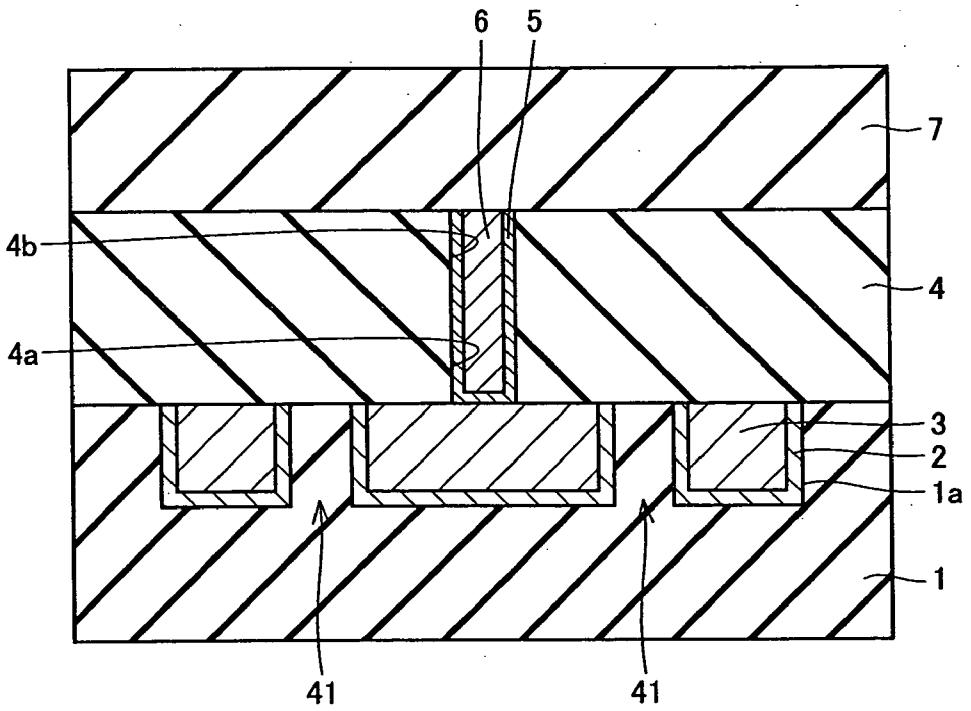


FIG.12

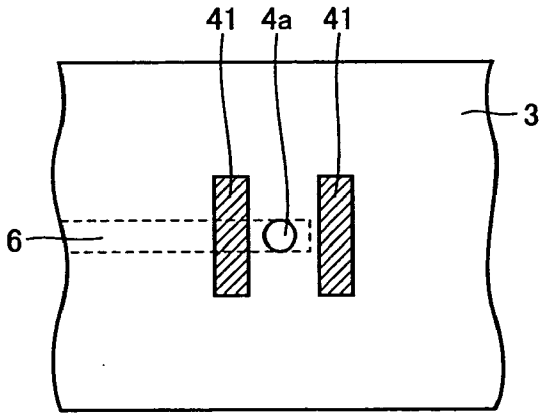


FIG.13

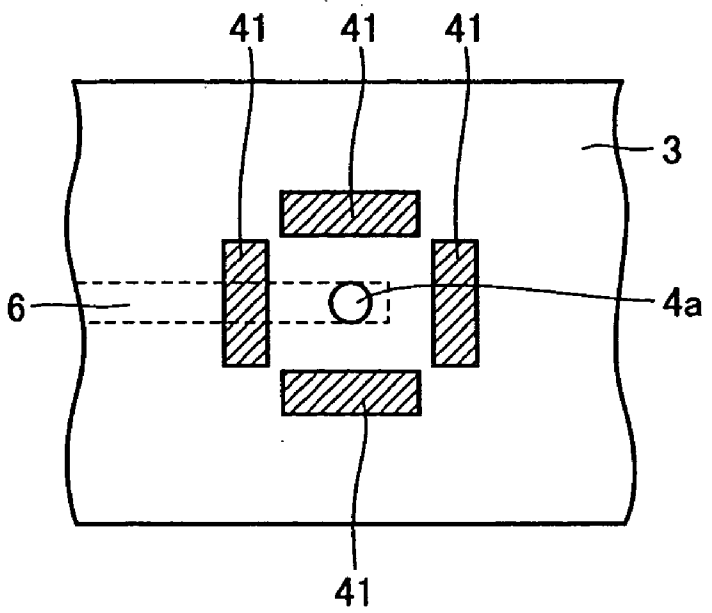


FIG.14

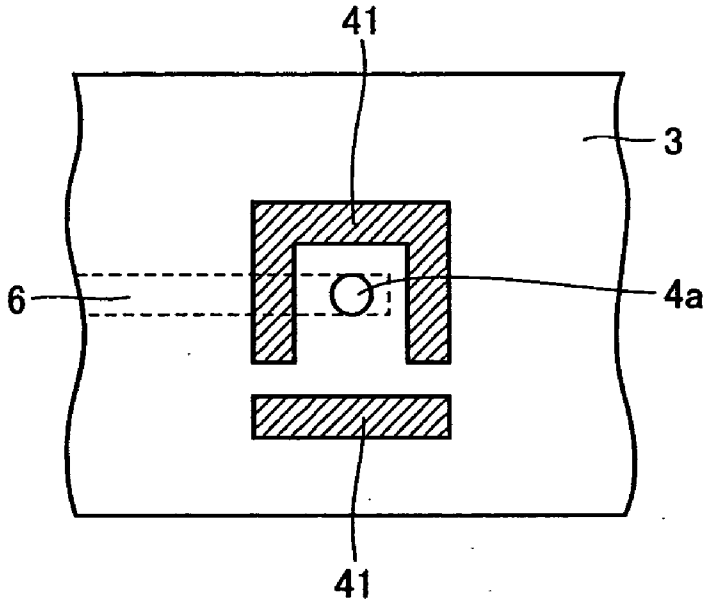


FIG.15

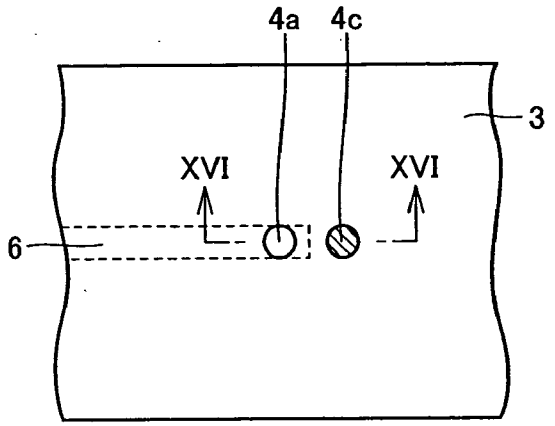


FIG.16

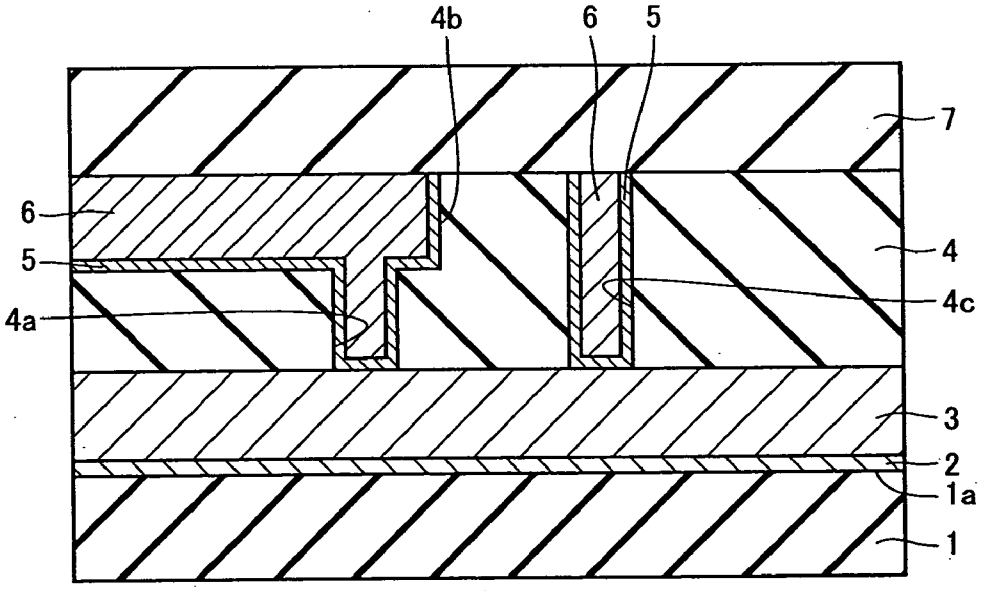


FIG.17

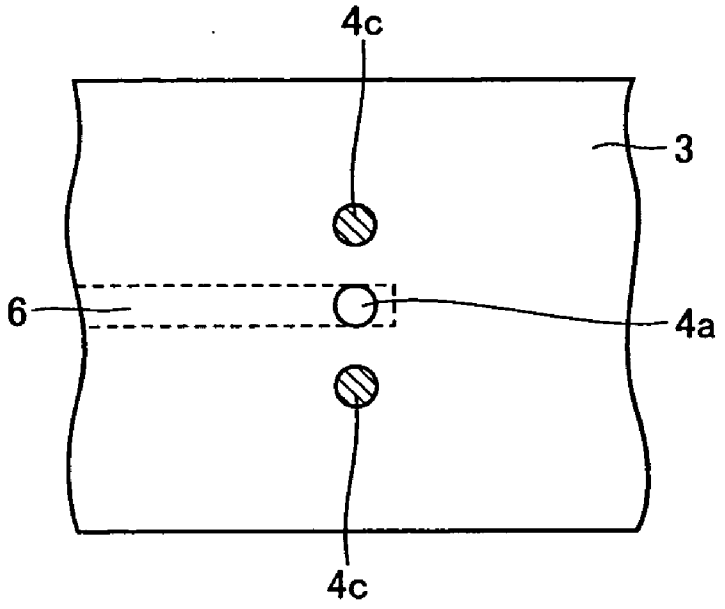


FIG.18

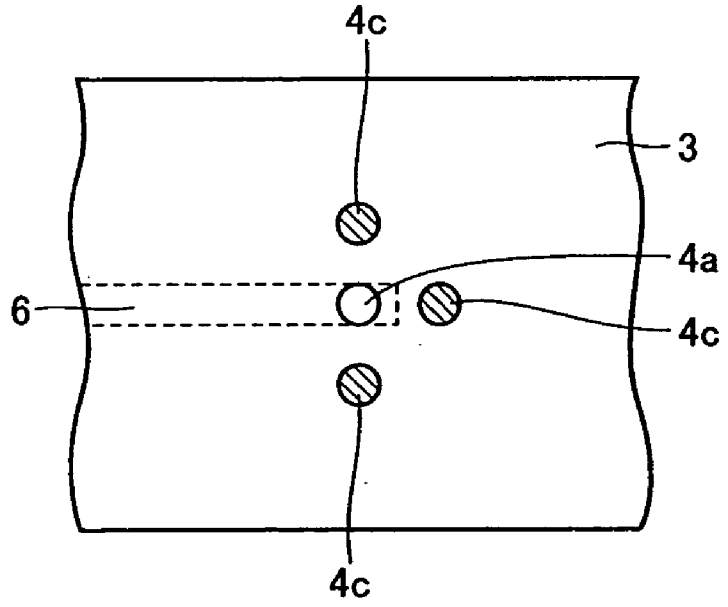


FIG.19

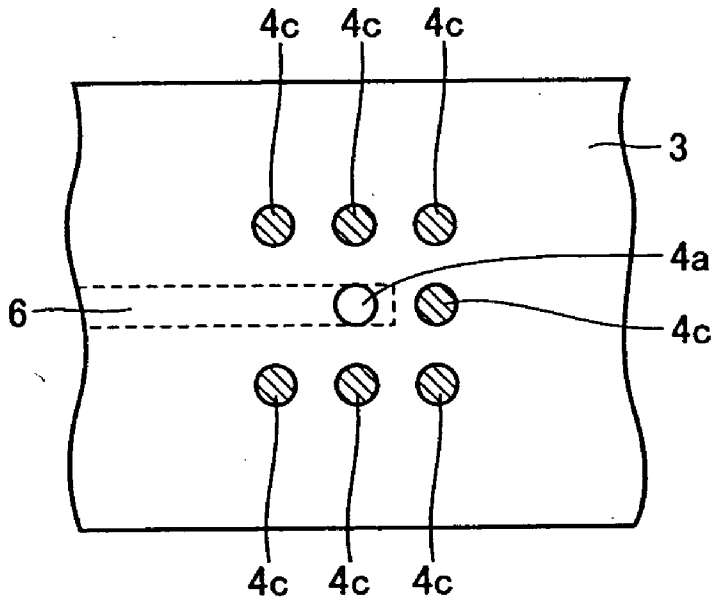


FIG.20

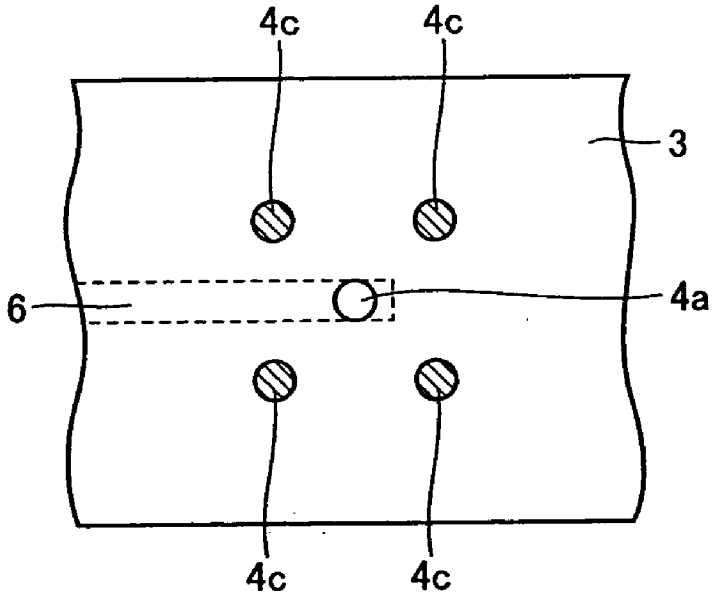


FIG.21

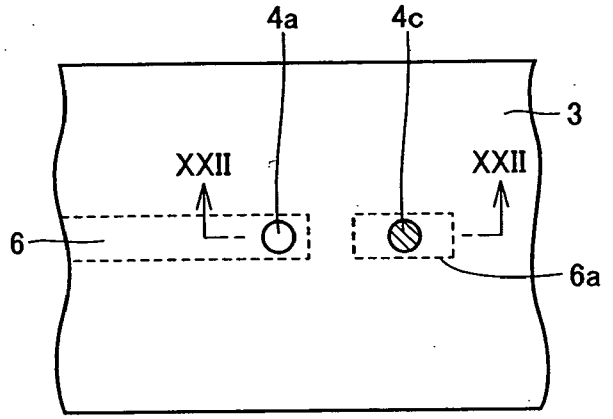


FIG.22

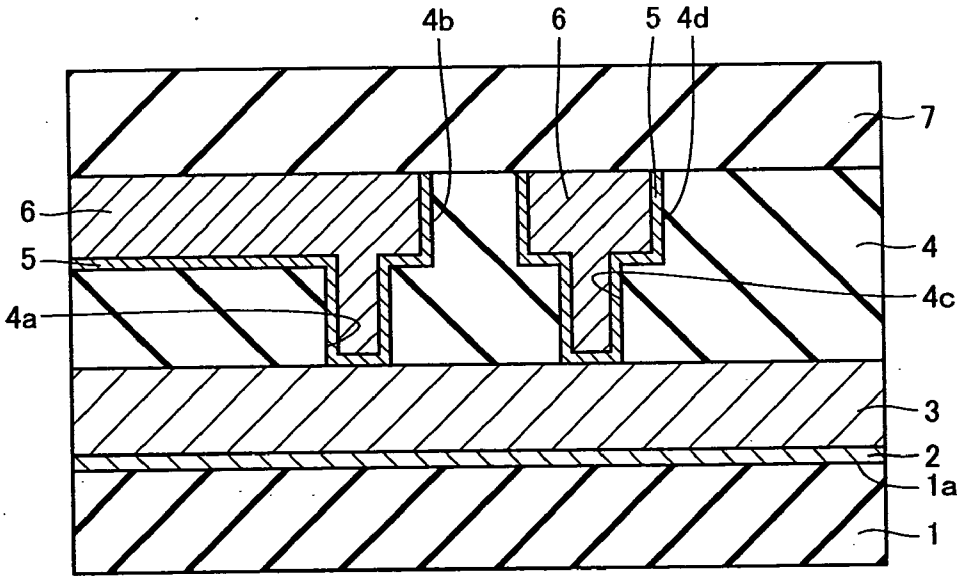


FIG.23

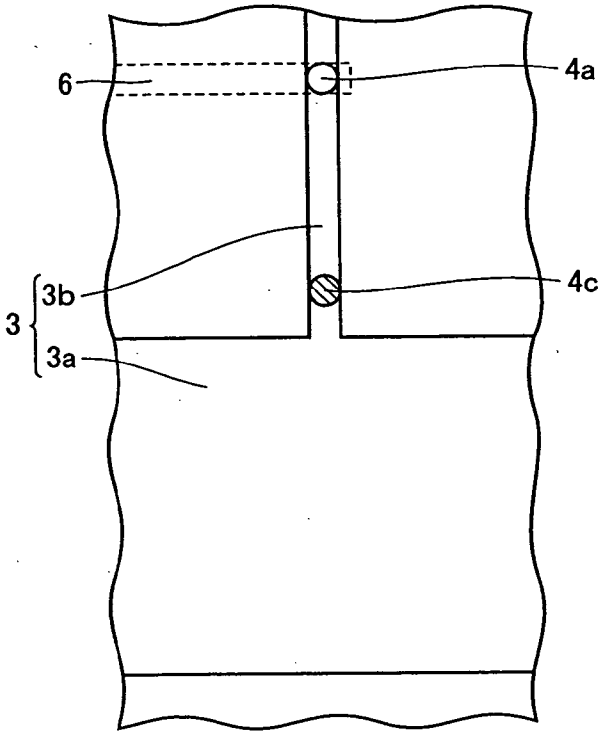


FIG.24

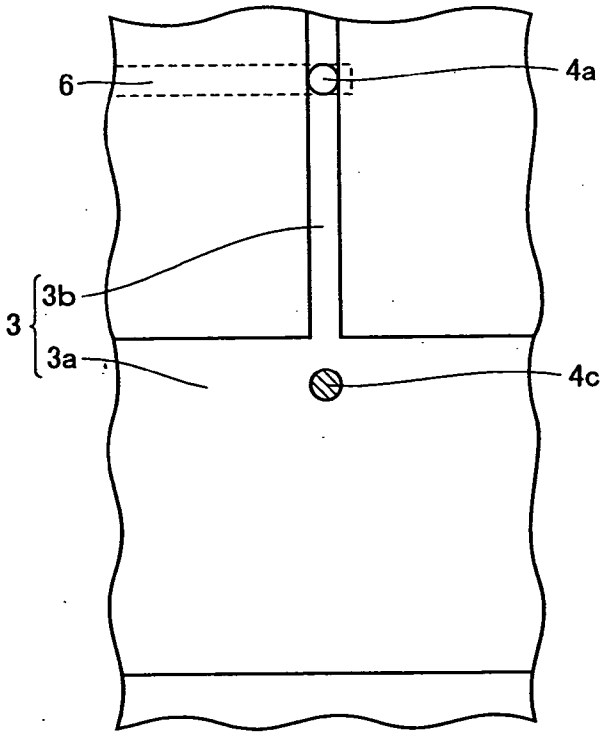


FIG.25

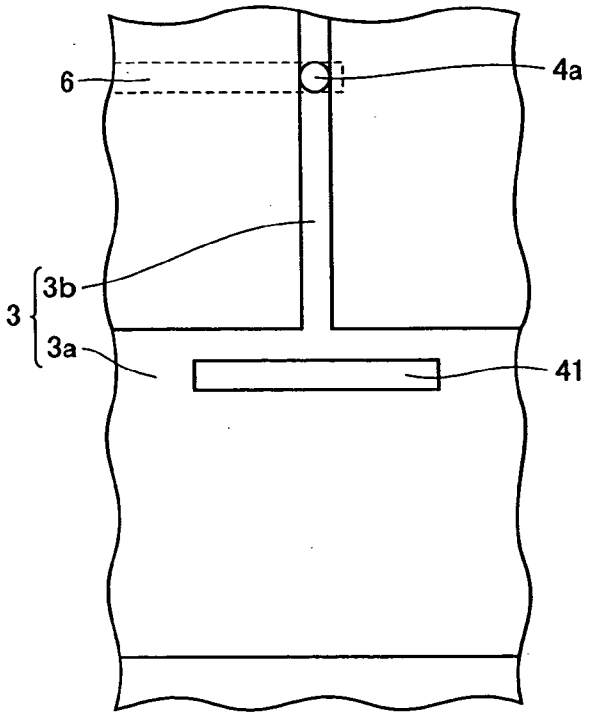


FIG.26

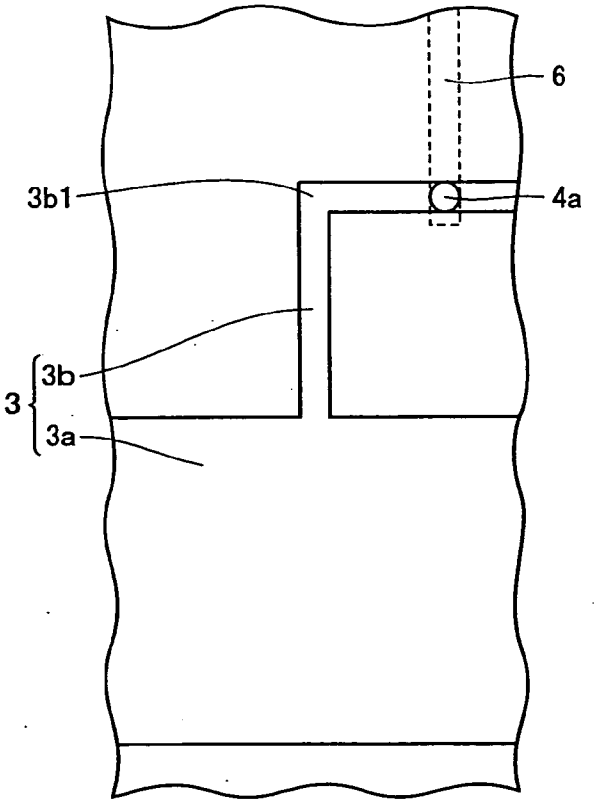
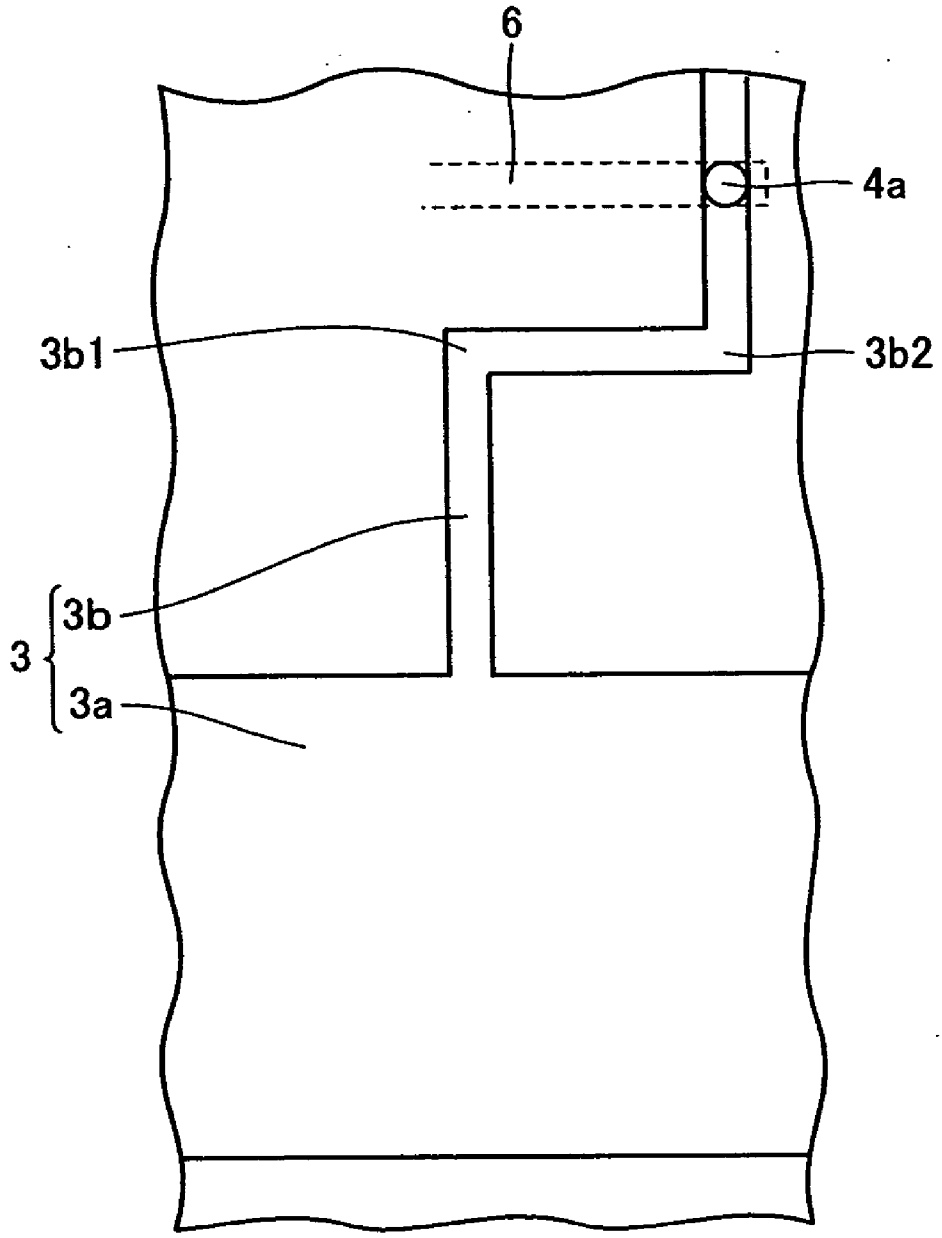


FIG.27



INTERCONNECTION STRUCTURE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an interconnection structure, and more particularly to an interconnection structure for an electronic device such as a semiconductor device or a liquid crystal device.

[0003] 2. Description of the Background Art

[0004] For a metal interconnection in an integrated circuit in a conventional semiconductor device, an aluminum (Al) alloy has mainly been employed. Meanwhile, for a state-of-the-art device, a copper (Cu) interconnection with lower resistance and excellent electromigration characteristic is employed. A semiconductor device with such a Cu interconnection is disclosed, for example, in Japanese Patent Laying-Open No. 2001-156073, and E. T. Ogawa et al., "Stress-Induced Voiding Under Vias Connected To Wide Cu Metal Leads" IEEE 02CH37320 40th Annual International Reliability Physics Symposium, Dallas, Tex., 2002, pp.312-321.

[0005] A manufacturing flow of the semiconductor device with such a Cu interconnection includes a dual damascene method and a single damascene method. In the dual damascene method, a via and a groove in an interconnection portion are formed by dry etching. Then, a barrier metal and a Cu seed film are formed, and a Cu film is formed by electrolytic plating. Thereafter, the quality of the Cu film is stabilized by heat treatment, and a Cu interconnection is formed by CMP (Chemical Mechanical Polishing).

[0006] On the other hand, in the single damascene method, first, a via is formed. Then, a barrier metal and a Cu seed film are formed, and a Cu film is formed by electrolytic plating. Thereafter, the quality of the Cu film is stabilized by heat treatment, and only the via is filled with the Cu film by CMP. Thereafter, an interlayer insulating film is formed, and an interconnection groove is formed by photolithography and dry etching. Then, the barrier metal and the Cu seed film are formed, and the Cu film is formed by electrolytic plating. After the quality of the Cu film is stabilized by heat treatment, only the interconnection groove is filled with the Cu film by metal CMP.

[0007] Cu plating is usually used in those two methods, however, it is known that the Cu plated film includes a large number of microvoids therein. In addition, it is considered that the voids are diffused in the film due to thermal stress, and are concentrated in an area under the via, if a stress migration test is conducted under a condition of 100° C. to 250° C. In particular, when an interconnection under a via has a large width, that is, a width not smaller than 1 μm, a defect tends to occur. If voids are concentrated in such a manner, a defect such as an increase in a via resistance, an open state, an increase in interconnection resistance, or disconnection may take place.

SUMMARY OF THE INVENTION

[0008] The present invention was made to solve the above-described problems. An object of the present invention is to provide an interconnection structure suppressing concentration of voids in an interconnection under a via due to stress migration.

[0009] An interconnection structure according to one aspect of the present invention includes a first conductive layer, an insulating layer, a second conductive layer, and a barrier metal layer. The first conductive layer is formed on a substrate, and composed of a copper layer. The insulating layer is formed on the first conductive layer, and has a hole reaching the first conductive layer. The second conductive layer is formed within the insulating layer, and composed of a copper layer electrically connected to the first conductive layer through the hole. The barrier metal layer is formed between the second conductive layer and the hole, and the insulating layer. The barrier metal layer has an opening in a bottom portion of the hole, and the second conductive layer comes in direct contact with the first conductive layer through the opening.

[0010] In the interconnection structure according to one aspect of the present invention, the first conductive layer and the second conductive layer are in direct contact with each other through the opening provided in the barrier metal layer in the bottom portion of the hole. The first conductive layer and the second conductive layer are both copper layers. In other words, connection between the first conductive layer and the second conductive layer is established between metals of the same type. Therefore, concentration of voids under the hole due to connection between different metals, caused when a barrier metal is interposed between the first conductive layer and the second conductive layer, can be suppressed.

[0011] An interconnection structure according to another aspect of the present invention includes a first interconnection portion, a second interconnection portion, an insulating layer, and a conductive layer. The first interconnection portion is formed on a substrate. The second interconnection portion is formed on the substrate, and has a line width larger than that of the first interconnection portion. The insulating layer is formed on the first and second interconnection portions, and has a hole reaching the second interconnection portion. The conductive layer is electrically connected to the second interconnection portion through the hole, and formed within the insulating layer. The first interconnection portion is composed of a copper layer formed by plating. The second interconnection portion has a two-layered structure of a copper layer and a metal layer, which is positioned at least in a region directly under the hole.

[0012] In the interconnection structure according to another aspect of the present invention, the second interconnection portion connected to the hole has a two-layered structure of the copper layer and the metal layer, which is connected to the hole. Thus, as a portion connected to the hole is not a copper layer including a large number of microvoids, concentration of voids in an area under the hole due to stress migration can be suppressed.

[0013] In addition, as the first interconnection portion is composed only of the copper layer, interconnection resistance in the first interconnection portion with a small line width can be maintained to a low level, and deterioration of performance due to an increase in resistance will not occur.

[0014] An interconnection structure according to yet another aspect of the present invention includes a first conductive layer, an insulating layer, and a second conductive layer. The first conductive layer is formed on a substrate, and composed of a copper layer. The insulating layer is

formed on the first conductive layer, and has a hole reaching the first conductive layer. The second conductive layer is formed within the insulating layer, and electrically connected to the first conductive layer through the hole. A slit is formed in the vicinity of the hole of the first conductive layer.

[0015] In the interconnection structure according to yet another aspect of the present invention, the slit is formed in the vicinity of the hole. Therefore, the slit serves as a wall when microvoids in the first conductive layer concentrate in a portion connected to the hole. Thus, since the microvoids cannot reach an area under the hole without going around the slit serving as the wall, concentration of microvoids in the area under the hole due to stress migration can be suppressed.

[0016] An interconnection structure according to yet another aspect of the present invention includes a first conductive layer, an insulating layer, and a second conductive layer. The first conductive layer is formed on a substrate, and composed of a copper layer. The insulating layer is formed on the first conductive layer, and has a first hole and a second hole reaching the first conductive layer. The second conductive layer for establishing electrical connection to another element is electrically connected to the first conductive layer through the first hole, and formed within the insulating layer. The second hole is used as a dummy hole which does not electrically connect the first conductive layer to another element.

[0017] In the interconnection structure according to yet another aspect of the present invention, a dummy hole is provided in addition to the first hole for connecting the first conductive layer to the second conductive layer. Therefore, microvoids in the first conductive layer do not concentrate solely in the first hole, but are distributed to the first hole and the second, dummy hole. Thus, concentration of microvoids in the area under the first hole due to stress migration can be suppressed.

[0018] An interconnection structure according to yet another aspect of the present invention includes a first conductive layer, an insulating layer, and a second conductive layer. The first conductive layer is formed on a substrate, has a first interconnection portion with a large line width and a second interconnection portion with a small line width, and is composed of a copper layer. The insulating layer is formed on the first conductive layer, and has a hole reaching the second interconnection portion with a small line width. The second conductive layer is electrically connected to the first conductive layer through the hole, and formed within the insulating layer. The second interconnection portion with a small line width is bent between a junction of the second interconnection portion and the first interconnection portion, and the hole.

[0019] In the interconnection structure according to yet another aspect of the present invention, a bend portion is disposed between a connection portion of the second interconnection portion and the first interconnection portion, and the hole. Therefore, a large number of microvoids within the first interconnection portion with a large line width are less likely to reach an area under the hole. Thus, concentration of voids in the area under the hole due to stress migration can be suppressed.

[0020] The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] **FIG. 1** is a schematic cross-sectional view showing a configuration of a semiconductor device in Embodiment 1 of the present invention.

[0022] **FIGS. 2 and 3** are schematic cross-sectional views illustrating, in the order of process steps, a first method of manufacturing a semiconductor device in Embodiment 1 of the present invention.

[0023] FIGS. **4** to **7** are schematic cross-sectional views illustrating, in the order of process steps, a second method of manufacturing a semiconductor device in Embodiment 1 of the present invention.

[0024] **FIG. 8** is a schematic cross-sectional view showing a configuration of a semiconductor device in Embodiment 2 of the present invention.

[0025] **FIG. 9** is a schematic cross-sectional view illustrating a method of manufacturing a semiconductor device in Embodiment 2 of the present invention.

[0026] **FIG. 10** is a schematic plan view showing a configuration of a semiconductor device in Embodiment 3 of the present invention.

[0027] **FIG. 11** is a schematic cross-sectional view along the line XI-XI in **FIG. 10**.

[0028] **FIG. 12** is a schematic plan view showing another configuration of the semiconductor device in Embodiment 3 of the present invention.

[0029] **FIGS. 13 and 14** are schematic plan views showing yet other configurations of the semiconductor device in Embodiment 3 of the present invention.

[0030] **FIG. 15** is a schematic plan view showing a configuration of a semiconductor device in Embodiment 4 of the present invention.

[0031] **FIG. 16** is a schematic cross-sectional view along the line XVI-XVI in **FIG. 15**.

[0032] **FIG. 17** is a schematic plan view showing another configuration of the semiconductor device in Embodiment 4 of the present invention.

[0033] FIGS. **18** to **20** are schematic plan views showing yet other configurations of the semiconductor device in Embodiment 4 of the present invention.

[0034] **FIG. 21** is a schematic plan view showing a configuration in which a dummy interconnection is provided in the semiconductor device in Embodiment 4 of the present invention.

[0035] **FIG. 22** is a schematic cross-sectional view along the line XXII-XXII in **FIG. 21**.

[0036] **FIG. 23** is a schematic plan view showing a configuration of a semiconductor device in Embodiment 5 of the present invention.

[0037] **FIG. 24** is a schematic plan view showing another configuration of the semiconductor device in Embodiment 5 of the present invention.

[0038] **FIG. 25** is a schematic plan view showing a configuration of a semiconductor device in Embodiment 6 of the present invention.

[0039] **FIG. 26** is a schematic plan view showing a configuration of a semiconductor device in Embodiment 7 of the present invention.

[0040] **FIG. 27** is a schematic plan view showing another configuration of the semiconductor device in Embodiment 7 of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0041] In the following, embodiments of the present invention will be described with reference to the figures.

[0042] (Embodiment 1)

[0043] Referring to **FIG. 1**, an interlayer insulating layer **1** is formed on a semiconductor substrate (not shown). A groove **1***a* is formed on the surface of interlayer insulating layer **1**. A barrier metal layer **2** is formed along an inner wall of groove **1***a*, and an interconnection layer (a first conductive layer) **3** composed of a copper layer is formed so as to fill groove **1***a*.

[0044] An interlayer insulating layer **4** is formed on interconnection layer **3**, and a via (hole) **4***a* reaching interconnection layer **3** and a groove **4***b* are formed in interlayer insulating layer **4**. Via **4***a* is formed in a bottom portion of groove **4***b*. A barrier metal layer **5** is formed along the wall surface of via **4***a* and groove **4***b*. An interconnection layer (a second conductive layer) **6** composed of a copper layer is formed so as to fill via **4***a* and groove **4***b*, and so as to electrically connect to interconnection layer **3** through via **4***a*. Interconnection layer **6** is thus formed in interlayer insulating layer **4**.

[0045] Barrier metal layer **5** described above has an opening in the bottom portion of via **4***a*, and interconnection layer **6** is in direct contact with interconnection layer **3** through that opening. An insulating layer **7** is formed on interlayer insulating layer **4** so as to cover interconnection layer **6**.

[0046] Here, barrier metal layer **2**, **5** is of a single-layer structure consisting of any of tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), and tungsten nitride (WN), for example, or of a multi-layered structure consisting of any combination of such materials.

[0047] Next, two manufacturing methods in the present embodiment will be described.

[0048] Referring to **FIG. 2**, interlayer insulating layer **1** is formed on the semiconductor substrate (not shown). Groove **1***a* is formed in interlayer insulating layer **1**. Barrier metal layer **2** is formed on the entire surface of interlayer insulating layer **1** where groove **1***a* is formed, and thereafter, copper layer **3** is formed so as to fill groove **1***a*. Copper layer **3** is formed, by forming a copper seed layer followed by forming a copper plated layer by plating. Then, barrier metal layer **2** and copper layer **3** are polished and removed by CMP until the surface of interlayer insulating layer **1** is exposed. Thus, barrier metal layer **2** and copper layer **3** are left only in groove **1***a*, to form interconnection layer **3** composed of a copper plated layer (a copper layer formed by plating).

[0049] Interlayer insulating layer **4** is formed on interlayer insulating layer **1** so as to cover interconnection layer **3**. Via **4***a* and groove **4***b* are formed on the surface of interlayer insulating layer **4** by dry etching. Via **4***a* is formed so as to extend from the bottom portion of groove **4***b* and to expose the surface of interconnection layer **3**.

[0050] Barrier metal layer **5** is formed on the surface of interlayer insulating layer **4** where via **4***a* and groove **4***b* are formed, for example, by sputtering. When barrier metal layer **5** is formed by sputtering, film thickness of barrier metal layer **5** attains a relation of T1>T2>T3, due to a difference in the aspect ratio (depth/bottom size) of the opening. In other words, film thickness T1 of barrier metal layer **5** on the upper surface of interlayer insulating layer **4** is larger than film thickness T2 in the bottom portion of groove **4***b*, while film thickness T2 in the bottom portion of groove **4***b* is larger than film thickness T3 in the bottom portion of via **4***a*. Thereafter, the whole surface of barrier metal layer **5** is subjected to dry etching.

[0051] Referring to **FIG. 3**, film thickness of barrier metal layer **5** is smaller in the bottom portion of via **4***a*. Therefore, barrier metal layer **5** in the bottom portion of via **4***a* is removed by dry etching described above. Thus, an opening is formed in barrier metal layer **5** in the bottom portion of via **4***a*, and the surface of interconnection layer **3** is exposed through the opening.

[0052] Referring to **FIG. 1**, copper layer **6** is formed so as to fill via **4***a* and groove **4***b*. Copper layer **6** is formed, by forming a copper seed layer followed by forming a copper plated layer by plating. Then, barrier metal layer **5** and copper layer **6** are polished and removed by CMP intil the surface of interlayer insulating layer **4** is exposed. Thus, barrier metal layer **5** and copper layer **6** are left only in via **4***a* and groove **4***b*, to form interconnection layer **6** composed of a copper plated layer. Thereafter, insulating layer **7** is formed on interlayer insulating layer **4** so as to cover interconnection layer **6**.

[0053] Referring to **FIG. 4**, interlayer insulating layer **1**, groove **1***a*, barrier metal layer **2**, and interconnection layer **3** are formed in a manner similar to the first manufacturing method as described above.

[0054] Interlayer insulating layer **4** is formed on interlayer insulating layer **1** so as to cover interconnection layer **3**. Groove **4***b* is formed on the surface of interlayer insulating layer **4** by dry etching. A barrier metal layer **5***a* is formed on the surface of interlayer insulating layer **4** where groove **4***b* is formed, for example, by sputtering.

[0055] Referring to **FIG. 5, a** resist pattern is formed on barrier metal layer **5***a* by photolithography. Thereafter, using the resist pattern as a mask, barrier metal layer **5***a* and interlayer insulating layer **4** are selectively removed by dry etching. Via **4***a* is thus formed in the bottom portion of groove **4***b*, and the surface of interconnection layer **3** is exposed on the bottom portion of via **4***a*. After the dry etching, the resist pattern is removed, for example, by ashing.

[0056] Referring to **FIG. 6, a** barrier metal layer **5***b* is formed on via **4***a* and barrier metal layer **5***a*. Film thickness of barrier metal layer **5** attains a relation of T4, T5>T6. In other words, barrier metal layers **5***a* and **5***b* are both formed on the upper surface of interlayer insulating layer **4** and on

the bottom portion of groove **4***b*, while only barrier metal layer **5***b* is provided in the bottom portion of via **4***a*. Therefore, film thickness T4, T5 of barrier metal layer **5** on the upper surface of interlayer insulating layer **4** and on the bottom portion of groove **4***b* is larger than film thickness T6 of barrier metal layer **5** in the bottom portion of via **4***a*. Thereafter, the whole surface of barrier metal layer **5** is subjected to dry etching.

[**0057**] Referring to **FIG. 7**, film thickness of barrier metal layer **5** is smaller in the bottom portion of via **4***a*. Therefore, barrier metal layer **5** in the bottom portion of via **4***a* is removed by dry etching described above. Thus, an opening is formed in barrier metal layer **5** in the bottom portion of via **4***a*, and the surface of interconnection layer **3** is exposed through the opening.

[**0058**] Referring to **FIG. 1**, copper layer **6** is formed so as to fill via **4***a* and groove **4***b*. Copper layer **6** is formed, by forming a copper seed layer followed by forming a copper plated layer by plating. Then, barrier metal layer **5** and copper layer **6** are polished and removed by CMP until the surface of interlayer insulating layer **4** is exposed. Thus, barrier metal layer **5** and copper layer **6** are left only in via **4***a* and groove **4***b*, to form interconnection layer **6** composed of a copper layer. Thereafter, insulating layer **7** is formed on interlayer insulating layer **4** so as to cover interconnection layer **6**.

[**0059**] According to the present embodiment, interconnection layer **3** and interconnection layer **6** are in direct contact with each other through the opening provided in barrier metal layer **5** in the bottom portion of via **4***a*, as shown in **FIG. 1**. Interconnection layer **3** and interconnection layer **6** are both copper layers. In other words, connection between interconnection layer **3** and interconnection layer **6** is established between metals of the same type. Therefore, concentration of microvoids under via **4***a* due to connection between different metals, caused when barrier metal layer **5** is interposed between interconnection layer **3** and interconnection layer **6**, can be suppressed.

[**0060**] Unlike a conventional example, barrier metal layer **5** is not in contact with interconnection layer **3** on the entire bottom of via **4***a*, though it is in contact with interconnection layer **3** in a peripheral portion of the bottom portion of via **4***a*. Therefore, in the present embodiment, voids will not diffuse as far as a central area of the bottom portion of via **4***a*, and stress distribution can be made smaller. Thus, as described above, concentration of microvoids under via **4***a* can be suppressed, compared to the conventional example.

[**0061**] (Embodiment 2)

[**0062**] Referring to **FIG. 8**, interlayer insulating layer **1** is formed on the semiconductor substrate (not shown). Groove **1***a* for an interconnection with a small line width (narrow interconnection) and a groove **1***b* for an interconnection with a large line width (wide interconnection) are formed on the surface of interlayer insulating layer **1**. Barrier metal layer **2** is formed along each inner wall of grooves **1***a*, **1***b*. Interconnection layer (a first interconnection portion) **3** with a small width, composed of a copper layer formed by plating, is formed so as to fill groove **1***a*. In addition, an interconnection layer (a second interconnection portion) with a large width, having a two-layered structure of copper layer **3** formed by plating and a metal layer **31** is formed so as to fill groove **1***b*. The interconnection layer with a large width has a line width larger than that of the interconnection layer with a small width.

[**0063**] Interlayer insulating layer **4** is formed on interlayer insulating layer **1**, so as to cover the interconnection layer with a small width and the interconnection layer with a large width. Via (hole) **4***a* reaching the interconnection layer with a large width and groove **4***b* are formed in interlayer insulating layer **4**. Via **4***a* is formed in the bottom portion of groove **4***b*. Metal layer **31** of the interconnection layer with a large width is positioned at least in a region directly under via **4***a*, and comes in contact with barrier metal layer **5** in the bottom portion of via **4***a*.

[**0064**] Barrier metal layer **5** is formed along the wall surface of via **4***a* and groove **4***b*. Interconnection layer (a conductive layer) **6** composed of a Cu layer is formed so as to fill via **4***a* and groove **4***b*, and so as to electrically connect to the interconnection layer with a large width through via **4***a*. Interconnection layer **6** is thus formed in interlayer insulating layer **4**. Insulating layer **7** is formed on interlayer insulating layer **4** so as to cover interconnection layer **6**.

[**0065**] Here, metal layer **31** is a single-layer structure consisting of any of tantalum, tantalum nitride, titanium, titanium nitride, and tungsten nitride, for example; a multi-layered structure consisting of any combination of such materials; an aluminum alloy layer; or a copper layer formed by sputtering.

[**0066**] In addition, barrier metal layer **2**, **5** is of a single-layer structure consisting of any of tantalum, tantalum nitride, titanium, titanium nitride, and tungsten nitride, for example, or of a multi-layered structure consisting of any combination of such materials.

[**0067**] Next, a manufacturing method in the present embodiment will be described.

[**0068**] Referring to **FIG. 9**, interlayer insulating layer **1** is formed on the semiconductor substrate (not shown). Groove **1***a* for the interconnection with a small line width (narrow interconnection) and groove **1***b* for the interconnection with a large line width (wide interconnection) are formed in the interlayer insulating layer **1** by dry etching. Barrier metal layer **2** is formed on the entire surface of interlayer insulating layer **4** along each inner wall of grooves **1***a*, **1***b*. Copper layer **3** is formed on barrier metal layer **2**. Copper layer **3** is formed, by forming a copper seed layer followed by forming a copper plated layer by plating. Metal layer **31** is formed on copper layer **3**.

[**0069**] Here, copper layer **3** is formed to a film thickness so as to completely fill groove **1***a*, as well as to a film thickness so as not to completely fill groove **1***b*. More specifically, copper layer **3** is formed such that film thickness T is smaller than depth D of groove **1***b*, not smaller than half the dimension of width L1 of groove **1***a* (L1/2), and less than half the dimension of width L2 of groove **1***b* (L2/2). In other words, in order to completely fill groove **1***a* with copper layer **3**, copper layer **3** should have film thickness T not smaller than L1/2. In order not to completely fill groove **1***b* with copper layer **3**, copper layer **3** should have film thickness T smaller than depth D of groove **1***b* and less than L2/2.

[**0070**] Thereafter, metal layer **31** and copper layer **3** are polished and removed by CMP until the surface of interlayer

insulating layer **1** is exposed. Thus, as shown in **FIG. 8**, only copper layer **3** is left in groove **1***a*, to form the interconnection layer with a small width, while both metal layer **31** and copper layer **3** are left in groove **1***b*, to form the interconnection layer with a large width.

[**0071**] Thereafter, interlayer insulating layer **4** is formed on interlayer insulating layer **1** so as to cover the interconnection layer with a small width and the interconnection layer with a large width. Via **4***a* and groove **4***b* are formed on the surface of interlayer insulating layer **4** and on the interconnection layer with a large width by dry etching. Via **4***a* is formed so as to extend from the bottom portion of groove **4***b* and so as to expose the surface of metal layer **31**.

[**0072**] Barrier metal layer **5** is formed on the surface of interlayer insulating layer **4** where via **4***a* and groove **4***b* are formed, and copper layer **6** is formed so as to fill via **4***a* and groove **4***b*. Copper layer **6** is formed, by forming a copper seed layer followed by forming a copper plated layer by plating. Then, barrier metal layer **5** and copper layer **6** are polished and removed by CMP until the surface of interlayer insulating layer **4** is exposed. Thus, barrier metal layer **5** and copper layer **6** are left only in via **4***a* and groove **4***b*, to form interconnection layer **6** composed of a copper layer. Thereafter, insulating layer **7** is formed on interlayer insulating layer **4** so as to cover interconnection layer **6**. According to this manufacturing method, the interconnection layer with a small width, composed of copper layer **3**, and the interconnection layer with a large width, having a two-layered structure of metal layer **31** and copper layer **3**, can easily be formed.

[**0073**] According to the present embodiment, the interconnection layer with a large width connected to via **4***a* has a two-layered structure of copper layer **3** and metal layer **31**, to which via **4***a* is connected. Thus, as a portion connected to via **4***a* is not a copper plated layer including a large number of microvoids, concentration of voids in an area under via **4***a* due to stress migration can be suppressed.

[**0074**] In addition, as the interconnection layer with a small width can be composed only of copper layer **3**, interconnection resistance in the interconnection layer with a small width can be maintained to a low level, and deterioration of performance due to an increase in resistance will not occur.

[**0075**] Here, though junction between metal layer **31** and copper layer **3** is established between metals of a different type, a contact area of metal layer **31** and the copper layer can readily be increased. Therefore, by increasing the contact area, local concentration of microvoids present in copper layer **3** in the junction between different metals can be suppressed.

[**0076**] Though **FIG. 8** shows a configuration formed with the dual damascene method, the present embodiment can also be adapted to a semiconductor device formed with the single damascene method.

[**0077**] Further, even if a copper layer formed by sputtering is employed as metal layer **31**, an effect as described above can be attained, because the copper layer formed by sputtering has the smaller number of microvoids than the copper layer formed by plating. It is to be noted that the copper layer formed by plating includes a large amount of impurity, such as chlorine (Cl), carbon (C), sulfur (S), or the like, contained in a chemical.

[**0078**] (Embodiment 3)

[**0079**] Referring to **FIGS. 10 and 11**, a configuration in the present embodiment is different from that in Embodiment 1 primarily in that a slit **41** is provided in interconnection layer (first conductive layer) **3** instead of forming an opening in barrier metal layer **5** in the bottom portion of via **4***a*.

[**0080**] Accordingly, barrier metal layer **5** is in contact with interconnection layer **3** on the entire surface of the bottom portion of via **4***a*. Slit **41** represents a region where groove **1***a* is not formed in interconnection layer **3** with a large width, and where interlayer insulating film **1** still remains, as shown in **FIG. 11**. For example, two such slits **41** are formed in the vicinity of via **4***a*, so as to interpose a portion connected to via **4***a*.

[**0081**] Configuration is otherwise approximately the same as that in Embodiment 1 described above. Therefore, same reference characters refer to same components, and description therefor will not be repeated.

[**0082**] According to the present embodiment, slit **41** is formed so as to interpose the portion connected to via **4***a*. Therefore, slit **41** serves as a wall when microvoids in interconnection layer **3** concentrate in the portion connected to via **4***a*. Thus, since the microvoids cannot reach an area under via **4***a* without going around the slit serving as the wall, concentration of microvoids in the area under via **4***a* due to stress migration can be suppressed.

[**0083**] Though an example in which slit **41** is formed so as to extend in a direction the same as interconnection layer **6** (horizontal direction in the figure) has been described with reference to **FIG. 10**, it is to be noted that slit **41** may extend in a direction intersecting interconnection layer **6** (longitudinal direction in the figure, for example), as shown in **FIG. 12**. In addition, slit **41** may be provided so as to surround four sides around the portion connected to via **4***a*, as shown in **FIG. 13**. Further, slit **41** may be implemented by slit **41** in an inverted U shape surrounding three sides around the portion connected to via **4***a*, and by straight slit **41** arranged on remaining one side, as shown in **FIG. 14**.

[**0084**] (Embodiment 4)

[**0085**] Referring to **FIGS. 15 and 16**, a configuration in the present embodiment is different from that in Embodiment 1 primarily in that a dummy via (dummy hole) **4***c* is provided in interlayer insulating layer **4** instead of forming an opening in barrier metal layer **5** in the bottom portion of via **4***a*.

[**0086**] Accordingly, barrier metal layer **5** is in contact with interconnection layer **3** on the entire surface of the bottom portion of via **4***a*. In addition, dummy via **4***c* does not electrically connect interconnection layer **3** to another element. Barrier metal layer **5** is formed along the inner wall of dummy via **4***c*, and copper layer **6** is formed so as to fill dummy via **4***c*. Copper layer **6** is not electrically connected to other interconnection layer other than interconnection layer **3**.

[**0087**] Configuration is otherwise approximately the same as that in Embodiment 1 described above. Therefore, same reference characters refer to same components, and description therefor will not be repeated.

[0088] According to the present embodiment, dummy via **4***c* is provided in addition to via **4***a* for connecting interconnection layer **3** to interconnection layer **6**. Therefore, microvoids in interconnection layer **3** do not concentrate solely in via **4***a*, but are distributed to a via **4***a* side and a dummy via **4***c* side. Thus, concentration of microvoids in the area under via **4***a* due to stress migration can be suppressed.

[0089] Though **FIG. 15** shows a configuration in which one dummy via **4***c* is disposed, two or more dummy vias **4***c* may be provided, as shown in FIGS. **17** to **20**. More specifically, two dummy vias **4***c* may be arranged so as to interpose via **4***a*, as shown in **FIG. 17**, or alternatively, three dummy vias **4***c* may be arranged so as to surround three sides around via **4***a*, as shown in **FIG. 18**. In addition, seven dummy vias **4***c*, for example, may be arranged so as to surround via **4***a*, as shown in **FIG. 19**, or alternatively, four dummy vias **4***c* may be arranged, as shown in **FIG. 20**.

[0090] Dummy via **4***c* may electrically connect interconnection layer **3** to dummy interconnection layer **6**, as shown in **FIGS. 21 and 22**. In such a case, a groove **4***d* for a dummy interconnection is formed on dummy via **4***c* of interlayer insulating layer **4**. Barrier metal layer **5** is formed on the inner wall of dummy via **4***c* and groove **4***d* for the dummy interconnection, and dummy interconnection layer **6** composed of a copper layer is formed so as to fill dummy via **4***c* and groove **4***d* for the dummy interconnection. Here, dummy interconnection layer **6** does not electrically connect interconnection layer **3** to another element.

[0091] Configuration is otherwise approximately the same as that shown in **FIGS. 15 and 16** described above. Therefore, same reference characters refer to same components, and description therefor will not be repeated.

[0092] As described above, when dummy via **4***c* and dummy interconnection **6** are provided as well, an effect similar to that in **FIGS. 15 and 16** can be attained.

[0093] (Embodiment 5)

[0094] Referring to **FIG. 23, a** configuration in the present embodiment is different from that in Embodiment 4 primarily in a position where dummy via **4***c* is arranged.

[0095] Interconnection layer **3** includes an interconnection portion with a large line width **3***a*, and an interconnection portion with a small line width **3***b*. Interconnection layer **6** is electrically connected to interconnection portion with a small line width **3***b* of interconnection layer **3** through via **4***a*. Dummy via **4***c* is positioned on interconnection portion with a small line width **3***b* between a connection portion R of interconnection portion with a large line width **3***a* and interconnection portion with a small line width **3***b*, and via **4***a*.

[0096] Configuration is otherwise approximately the same as that in Embodiment 4 described above. Therefore, same reference characters refer to same components, and description therefor will not be repeated.

[0097] According to the present embodiment, dummy via **4***c* is provided in addition to via **4***a* for connecting interconnection layers **3** and **6**. Therefore, microvoids in interconnection layer **3** do not concentrate only in via **4***a*, but are distributed to the via **4***a* side and the dummy via **4***c* side. Thus, concentration of voids in the area under via **4***a* due to stress migration can be suppressed.

[0098] A large number of microvoids in interconnection layer with a large line width **3***a* tend to concentrate in the area under dummy via **4***c* before reaching the area under via **4***a*. Therefore, concentration of voids in the area under via **4***a* can further be suppressed.

[0099] Even when dummy via **4***c* is arranged on interconnection layer with a large line width **3***a* as shown in **FIG. 24**, an effect as described above can be attained, so long as dummy via **4***c* is arranged in the vicinity of connection portion R of interconnection portion with a large line width **3***a* and interconnection portion with a small line width **3***b*.

[0100] In the present embodiment as well, the dummy interconnection layer may electrically be connected to interconnection layer **3** through dummy via **4***c*, or alternatively, the dummy interconnection layer does not need to be provided.

[0101] (Embodiment 6)

[0102] Referring to **FIG. 25, a** configuration in the present embodiment is different from that in Embodiment 3 in a position where slit **41** is arranged.

[0103] Interconnection layer **3** includes interconnection portion with a large line width **3***a*, and interconnection portion with a small line width **3***b*. Interconnection layer **6** is electrically connected to interconnection portion with a small line width **3***b* of interconnection layer **3** through via **4***a*. Slit **41** is positioned on interconnection portion with a large line width **3***a* in the vicinity of connection portion R of interconnection portion with a large line width **3***a* and interconnection portion with a small line width **3***b*.

[0104] Configuration is otherwise approximately the same as that in Embodiment 3 described above. Therefore, same reference characters refer to same components, and description therefor will not be repeated.

[0105] According to the present embodiment, slit **41** is formed in the vicinity of connection portion R. Therefore, a large number of microvoids in interconnection layer with a large line width **3***a* cannot reach an area under via **4***a* without going around slit **41** serving as the wall. Thus, concentration of voids in the area under via **4***a* due to stress migration can be suppressed.

[0106] (Embodiment 7)

[0107] Referring to **FIG. 26, a** configuration in the present embodiment is different from that in Embodiment 5 in that interconnection portion with a small line width **3***b* is once bent at a bend portion **3***b***1** instead of providing a dummy via. Bend portion **3***b***1** is arranged between connection portion R and via **4***a*.

[0108] Configuration is otherwise approximately the same as that in Embodiment 5 described above. Therefore, same reference characters refer to same components, and description therefor will not be repeated.

[0109] According to the present embodiment, bend portion **3***b***1** is disposed between connection portion R and via **4***a*. Therefore, a large number of microvoids within interconnection layer with a large line width **3***a* are less likely to reach an area under via **4***a*. Thus, concentration of voids in the area under via **4***a* due to stress migration can be suppressed.

[0110] Though an example in which one bend portion **3b1** is provided has been described above, two or more bend portions (two bend portions **3b1**, **3b2**, for example) may be arranged between connection portion R and via **4a**, as shown in **FIG. 27**.

[0111] By arranging two or more bend portions, a large number of microvoids in interconnection layer with a large line width **3a** are further less likely to reach the area under via **4a**. Accordingly, concentration of voids in the area under via **4a** due to stress migration can further be suppressed.

[0112] In the above-described embodiments, a copper layer represents a layer composed of a material consisting essentially of copper, and includes a layer composed of copper containing unavoidable impurities, a copper alloy layer, or the like.

[0113] The configurations in the above-described embodiments may be combined, as desired. In addition, though an interconnection structure for a semiconductor device has been described above, the present invention is widely applicable to an interconnection structure for an electronic device, such as a liquid crystal device, in addition to the semiconductor device.

[0114] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. An interconnection structure, comprising:

a first conductive layer formed on a substrate and composed of a copper layer;

an insulating layer formed on said first conductive layer and having a hole reaching said first conductive layer;

a second conductive layer formed within said insulating layer and composed of a copper layer electrically connected to said first conductive layer through said hole; and

a barrier metal layer formed between said second conductive layer and said hole, and said insulating layer; wherein

said barrier metal layer has an opening in a bottom portion of said hole, and said second conductive layer comes in direct contact with said first conductive layer through said opening.

2. An interconnection structure, comprising:

a first interconnection portion formed on a substrate;

a second interconnection portion formed on said substrate and having a line width larger than that of said first interconnection portion;

an insulating layer formed on said first and second interconnection portions and having a hole reaching said second interconnection portion; and

a conductive layer electrically connected to said second interconnection portion through said hole and formed within said insulating layer; wherein

said first interconnection portion is composed of a copper layer formed by plating, and

said second interconnection portion has a two-layered structure of a copper layer and a metal layer positioned at least in a region directly under said hole.

3. The interconnection structure according to claim 2, wherein

said metal layer is a copper layer formed by sputtering.

4. The interconnection structure according to claim 2, wherein

said metal layer is an aluminum alloy layer.

5. An interconnection structure, comprising:

a first conductive layer formed on a substrate and composed of a copper layer;

an insulating layer formed on said first conductive layer and having a first hole and a second hole reaching said first conductive layer; and

a second conductive layer for electrical connection to another element, electrically connected to said first conductive layer through said first hole and formed within said insulating layer; wherein

said second hole is used as a dummy hole which does not electrically connect said first conductive layer to another element.

6. The interconnection structure according to claim 5, further comprising a dummy interconnection layer which is electrically connected to said first conductive layer through said second hole and does not electrically connect said first conductive layer to another element.

7. The interconnection structure according to claim 5, further comprising a third conductive layer filling said second hole, wherein

said third conductive layer is not electrically connected to other interconnection layer other than said first conductive layer.

8. The interconnection structure according to claim 5, wherein

said first conductive layer has a first interconnection portion with a large line width, and said second conductive layer has a second interconnection portion with a small line width, and

said first interconnection portion with a large line width is connected to said second interconnection portion with a small line width through said hole.

9. The interconnection structure according to claim 5, wherein

said first conductive layer has a first interconnection portion with a large line width, and a second interconnection portion with a small line width,

said second conductive layer has a third interconnection portion with a small line width, and

said second interconnection portion with a small line width is connected to said third interconnection portion with a small line width through said hole.

10. The interconnection structure according to claim 9, wherein

said second hole used as said dummy hole is formed so as to reach said first interconnection portion with a large line width.

11. The interconnection structure according to claim 9, wherein

said second hole used as said dummy hole is formed so as to reach said second interconnection portion with a small line width.

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