DUAL DAMASCENE: A ULSI WIRING TECHNOLOGY

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ABSTRACT

Escalating density, performance, and (perhaps most importantly) manufacturing requirements associated with ULSI semiconductor wiring, necessitate a metamorphosis in interconnection technology. To meet these needs, an inlaid fully integrated wiring technology called Dual Damascene has been designed and demonstrated at IBM's Essex Junction, Vermont, facility. A subset of the technology's features has been successfully implemented in the manufacture of IBM's 4-Mb DRAM. The Dual Damascene structure achieved is a planar, monolithic-metal interconnect, comprising a vertical metal stud and horizontal metal interconnect, both embedded in an insulator matrix. The complete Dual Damascene technology features a unique process sequence, chemical-mechanical insulator planarization, stacked photolithographic masks, clustered stud and interconnect etch, concurrent stud and interconnect metal fill, and chemical-mechanical metal etchback. In full production, IBM's 4-Mb 200-mm manufacturing implementation uses key elements of this new technology; i.e., chemical-mechanical insulator planarization, concurrent stud and interconnect metal fill, and chemical-mechanical metal etchback. These elements improve manufacturability while maintaining excellent reliability. More progressive Dual Damascene process features such as clustered photolithography and clustered etch, which facilitate self-aligned stud to interconnect structures, are expected to become ULSI necessities as scaling and defect density requirements become still more demanding.

INTRODUCTION

Interconnection is arguably the most demanding component of ULSI technologies. Historically, the semiconductor industry has utilized either subtractive etch or liftoff as the primary metal-patterning technique. But these techniques (and associated processing) have limitations, including non-planarity, poor metal step coverage, and residual metal shorts which, along with other fabrication problems, often result in inconsistent manufacturability, low yields, uncertain reliability, and poor ULSI extendibility. To address these problems, a new interconnect technology called Dual Damascene has been designed and demonstrated.

The art of damascene has been used for centuries in the fabrication of jewelry; we have now adapted the basic damascene concept for application in the semiconductor industry. This paper describes the full wiring technology called Dual Damascene. It extends the state of the art by providing a streamlined method for fabricating ULSI interconnections for applications such as DRAM, SRAM and multilevel logic. This complete process has been demonstrated in IBM's development laboratory at Essex Junction and key aspects have been implemented its manufacturing facilities. Each Dual Damascene wiring level consists of a single planar insulator with embedded vertical studs and horizontal interconnects. The laboratory and manufacturing wiring structures achieved are identical except that the manufacturing stud and interconnect structures are not self-aligned. Figure 1 shows a schematic cross section of the technology's elements as applied to high-density logic. All wiring levels can reasonably be pushed to the minimum-dimension pitch limit for a given ground-rule set (minimum line / minimum space, with vertical stud). Similar fabricating operations are clustered throughout the process and planarization is maintained to improve manufacturability and lessen the risk of process- induced defects.

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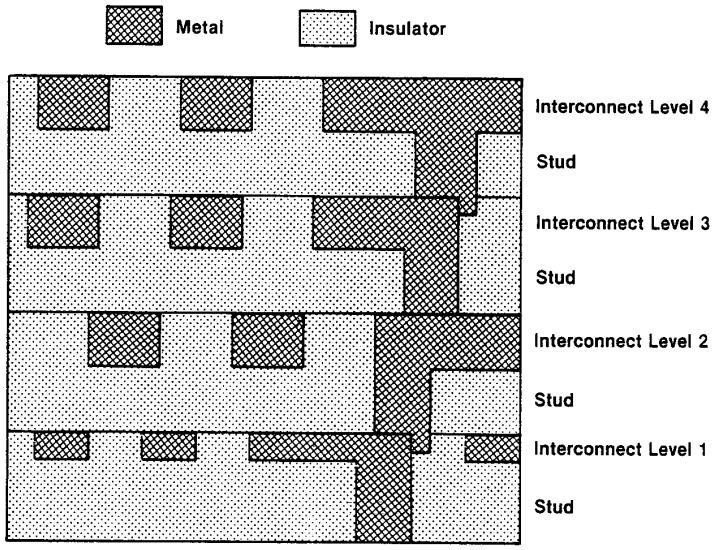

Figure 1. Dual Damascene technology key features: "automatic" reoccurring planarity; monolithic stud/interconnect structure; embedded metal; self-alignment of the interconnect and stud; extendibility to additional levels.

PROCESS SEQUENCE

In the simplest ULSI Damascene implementation, grooves are reactively ion-etched (RIE) into a pre-planarized dielectric and filled with metal. The metal overburden is then selectively removed, re-exposing the planar dielectric surface, and leaving embedded metal in the desired wiring pattern. The selective metal etchback is accomplished by using a technique called chemical-mechanical polish (CMP)[1].

Dual Damascene is a more manufacturable technology. The complete process sequence as demonstrated in the Essex Junction Laboratory (Figure 2) begins on an insulator surface that has been planarized by either chemical-mechanical polish or by other means. Once achieved, this critically important insulator planarity is maintained through successive wiring levels and need not be re-established. An insulator is then deposited in one extended deposition. Its thickness is equal to the combined thickness of the planned interlevel dielectric and the metal interconnect. Photolithographic operations for studs and interconnect are accomplished in succession with their mask images stacked one on top of the other (Figure 2a).

The stacked mask images are sequentially transferred into the insulator during the in situ RIE operations. The intersection of the two mask openings defines the self-aligned stud. The stud shape is etched almost to completion (Figure 2b). In situ RIE reagents are then changed so that the interconnect pattern can be selectively opened through the stud-masking material (e.g., photoresist), exposing the insulator in the desired circuit pattern (Figure 2c). Again in situ, the RIE reagents are changed and the interconnect pattern is recessed into the insulator. As the interconnect pattern is transferred, the stud is simultaneously being deepened, completing its etch to the required depth and providing the necessary over-etch, assuring contact to the underlying level. The last in situ etch strips all residual masking material from the insulator's top surface (Figure 2d).

Suitable metal deposition is now required to fill the high-aspect-ratio stud and interconnect cavities. An excellent process choice is low-pressure chemical-vapor-deposited tungsten (LPCVD-W), but other lower resistivity options are also becoming available[2]. After metal deposition, an appropriate anneal can be performed.

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Chemical-mechanical etchback is then used to remove the excess metal from the insulator's top surface (Figure 2f). At the same time, the composite structure is automatically returned to a planar surface, ready to receive another wiring level. From this point on, the process repeats for each additional wiring level, to build a multilevel stack.

Generalized process flows for a conventional RIE process, IBM's manufacturing implementation of Dual Damascene, and a full Dual Damascene process are shown in Table I. For each case, it is assumed that a stud and an interconnect are formed beginning on a planar surface. The complete Dual Damascene process uses fewer steps, orders the steps for clustering and returns a planar surface. Figure 3 shows a completed CVD-W Dual Damascene structure.

MANUFACTURING LEVERAGE

Dual Damascene technology offers the unification of density, performance, reliability, and manufacturability in a fully integrated wiring technology. The features that enhance density and performance also promote excellent reliability and improve manufacturability.

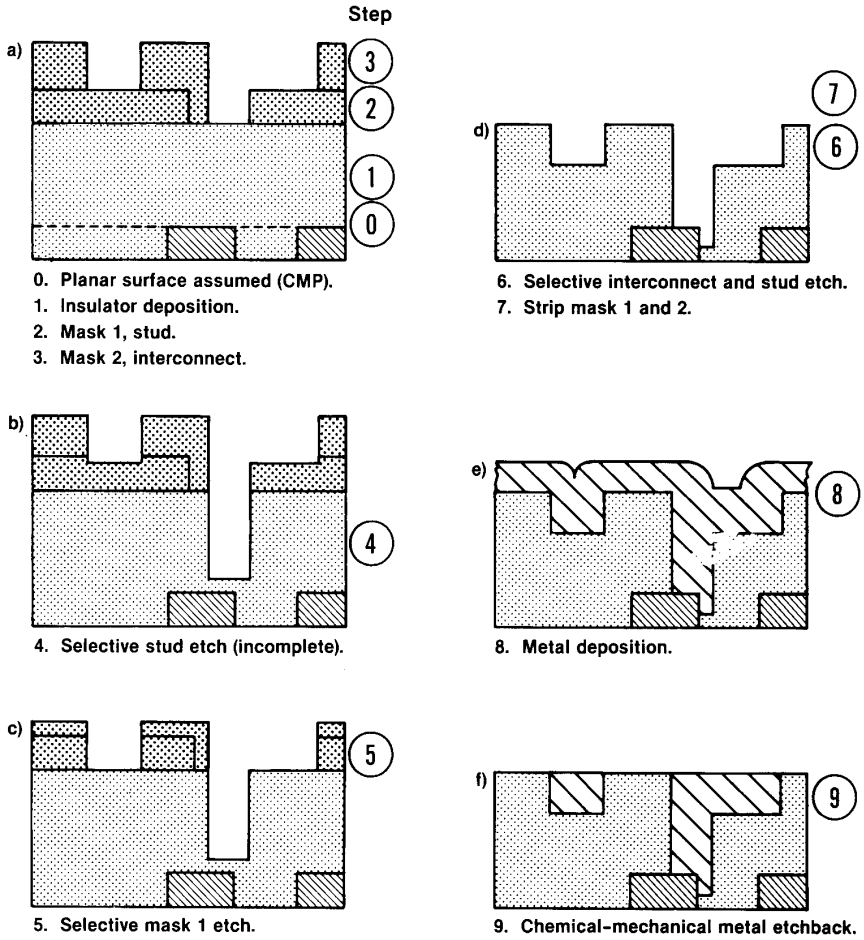

Figure 2. Process sequence.

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Table I. Process sequence comparison for wiring technologies. Each sequence is assumed to begin on a planar surface. For both Dual Damascene implementations, note that there are fewer total operations and that insulator replanarization is avoided. For the complete implementation, note that similar operations are ordered (clustered process) and that three future tool clusters are suggested.

Conventional RIE	Dual Damascene		
	4-Mb Manufacturing Implementation	Complete Implementation	Tool Clusters
Insulator Deposition	Insulator Deposition	Insulator Deposition	
Contact Lithography	Contact Lithography	Contact Lithography	C1
Insulator RIE (Contact)	Insulator RIE (Contact)	Interconnect Lithography	
Photoresist Strip	Photoresist Strip	Insulator RIE (Contact)	
Metal Fill (Stud)	Interconnect Lithography	Insulator RIE (Interconnect)	
Metal Etchback (RIE)	Insulator RIE (Interconnect)	Photoresist Strip	C2
Metal Deposition	Photoresist Strip	Metal Depostition	
Interconnect Lithography	Metal Deposition	Anneal	
Metal RIE (Interconnect)	Anneal	Metal Etchback (CMP)	C3
Photoresist Strip	Metal Etchback (CMP)		
Anneal			
Insulator Deposition			
Insulator Planarization			

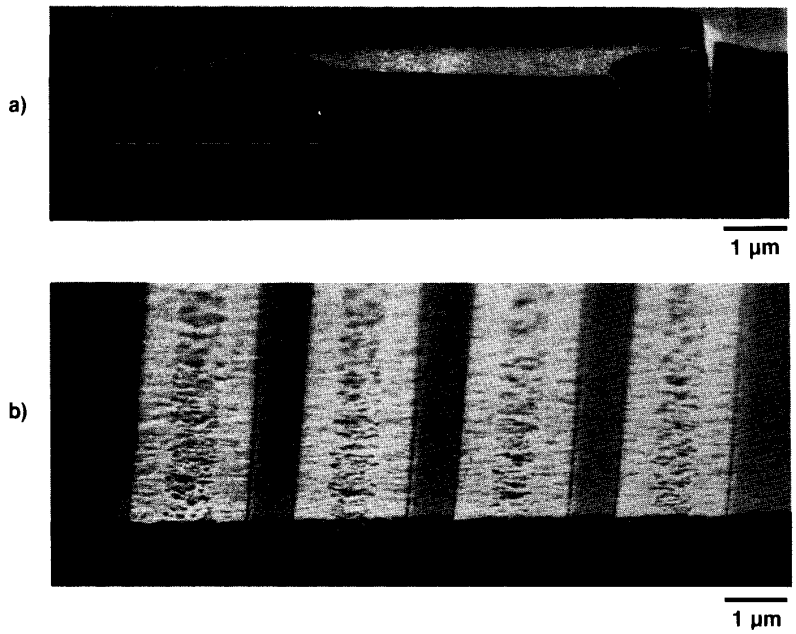

Figure 3. SEM micrographs showing Dual Damascene: a) insulator structure prior to metal fill; note that interconnect is self-aligned to stud (upper right corner); b) tungsten interconnects following CMP etchback.

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Manufacturing Yield

Enhanced manufacturing yield is the central motivation for choosing to practice Dual Damascene. Overall manufacturing yield is improved by optimizing the conductor-to-stud structure, simplifying the process, maximizing the process window, and controlling process-induced defects. Relative data comparing manufacturing yields and other selected electrical parameters are shown in Table II; the results are for a subset of Dual Damascene features implemented in production of IBM's 200-mm 4-Mb DRAM; they are compared to high-volume parts manufactured using a previously reported IBM manufacturing wiring technology[3]. The Dual Damascene technology elements included in the 4-Mb DRAM program are chemical-mechanical insulator planarization, concurrent stud and interconnect metal fill, and chemical-mechanical metal etchback.

Defect density control. Dual Damascene's persistent planarity is ideal for defect control. As each wiring level is completed, the planar surface re-emerges, free from all projecting topography (including defects), ready to receive another wiring level. Any foreign material residues embedded during fabrication are truncated during the CMP metal etchback operation (Figure 4). CMP also aggressively removes any residual metal, giving direct control over otherwise troublesome metal shorts.

The stacked photolithographic mask structure provides a built-in redundancy, reducing susceptibility to RIE transfer of pin holes and other mask defects.

Process window. Planarity widens the process window for subsequent operations and film thickness variations are minimized. For example, the interlevel metal-to-metal distance remains uniform, so the required via over-etch is minimized. Photolithographic exposure can be optimized with a uniform resist thickness and consistent focus depth. Compounding level-to-level topography variations no longer cause unwanted metal RIE stringers and unacceptably sharp etch profiles.

Table II. Relative parametric comparison. Normalized data comparing key RIE and Dual Damascene manufacturing results. Data generated during high volume production of IBM's 4-Mbit DRAM.

Parameter	RIE	Dual Damascene
Overall Final Test Yield	1.0	2.0X *
Defect Density	1.0	0.2X
Metal Opens × Shorts Yield	1.0	1.1X
R_c Distribution	Variable	Tight
FET Threshold Stability	1.0	1.0X
Device Integrity	1.0	1.0X
Reliability	Excellent	Excellent

* Function of timing and toolset.

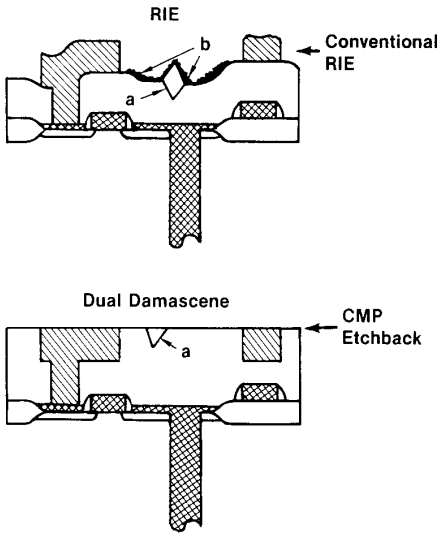

Figure 4. Defect density control. (a) Embedded foreign material residues are truncated by chemical-mechanical etchback; (b) residual metal aggressively removed, giving direct control of metal shorts.

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Etch. The etch process window used to define the wiring pattern is significantly improved by etching the insulator instead of the metal. Insulators are easier to etch than metals. RIE metal-process yields often suffer, particularly from residual metal shorts and corrosion. Table II compares RIE metal opens and shorts with damascene-patterned metal.

Self-alignment. The Dual Damascene masking sequence provides orthogonal self-alignment between a contact or via stud and its overpassing interconnect (Figure 5), reducing the possibility for intralevel shorts from stud top to adjacent metal line. The worst-case space between these two structures is effectively increased by one overlay, compared to more conventional wiring technologies.

Another, more subtle, advantage is that the stud image can now be made oversized, orthogonal to the interconnect, by a distance approaching the space width. This opens the photolithographic process window and reduces stepper exposure time.

Manufacturing Cost

The Dual Damascene concept addresses manufacturing cost issues such as cost-effective planarization, process simplification, process clustering, and tool clustering. The 4-Mb DRAM implementation takes full advantage of cost-effective planarization. Limited process simplification (fewer metal depositions and CMP operations) and process/tool clustering (consolidated metal depositions) are also practiced in the 4-Mb manufacturing process.

Cost-effective planarization. Topographic planarization offers important ULSI advantages, as listed above, but it is an expensive and demanding process. Any planarization process, including chemical-mechanical polish, should be applied with some restraint and, where possible, with finesse. Once a planar surface has been achieved, the Dual Damascene sequence eliminates the need for subsequent

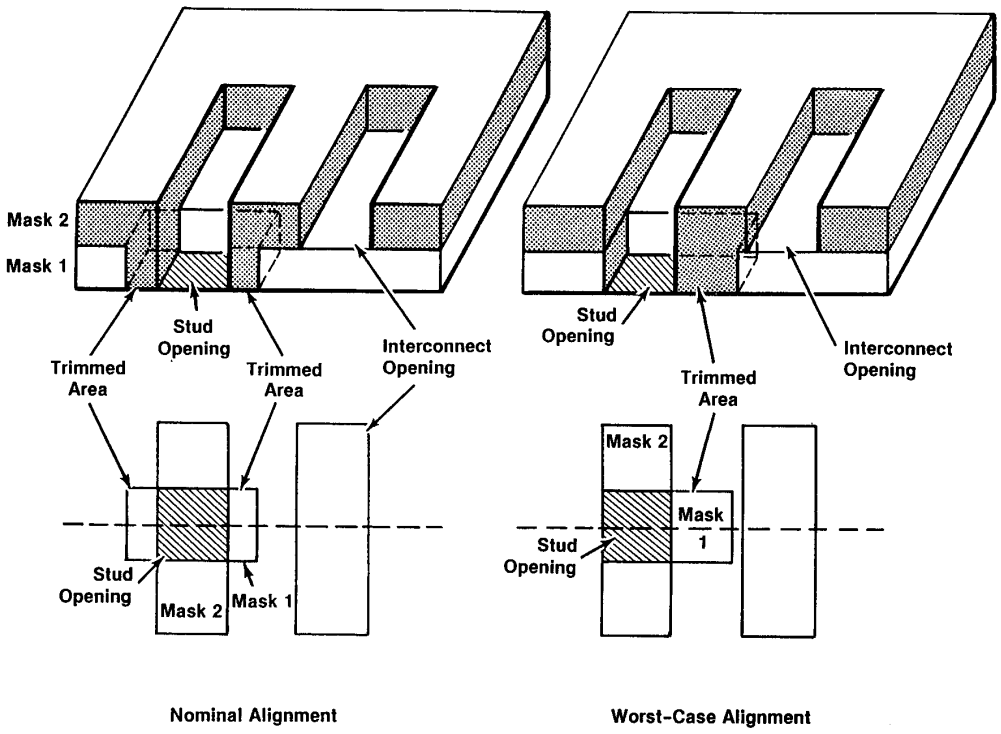

Figure 5. Self-alignment features.

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replanarization. In the process sequence shown (Figure 2), planarity is won prior to the contact / bit-line level (metal-1). Thereafter, an insulator replanarization operation is avoided at each successive wiring level. When chemical-mechanical processing is invoked, it is not used for insulator replanarization; it is used in its far less stringent and more controllable metal etchback mode. As chemical-mechanical etchback clears the metal overburden, its etch is largely arrested by the insulator matrix, which serves as an etch stop. After CMP etchback, the metal wiring level is complete and the substrate has been "automatically" returned to its original planar state, ready to accept further processing without topographical complications (Figure 2f).

Simplification - reduced process steps. The Dual Damascene process sequence has potentially 30% fewer operations than a more traditional planarized technology with vertical studs (Table I). This simplification has important ramifications for startup tool cost, process turnaround time, and defects. For example, an RIE technology requires 13 major operations to produce a planar wiring level with vertical stud and horizontal interconnect. Dual Damascene requires as few as nine major operations; the process steps avoided are an insulator deposition, an insulator planarization, a resist strip, and a metal deposition.

Improved process-line logistics - process cluster. The unique process sequence shown in Figure 2 clusters similar operations. *Process clustering* minimizes product handling between manufacturing sectors, reduces the possibility for handling damage, smooths product flow and eases product tracking.

Tool cluster. It will soon become practical for one manufacturing tool to accomplish several dissimilar fabricating operations. Only process-clustered technologies like Dual Damascene will readily facilitate these future *tool clusters*. Potential advantages are reduced handling for defect-density control and improved production cycle time (turnaround time). A full Dual Damascene wiring level could be fabricated in three clustered operations (Table II). The first cluster would be photolithographic, where both contact/via and interconnect resist patterns would be applied in sequence; the second cluster would provide contact/via and interconnect etch, resist strip, and metal depositions; and a third cluster would provide chemical-mechanical etchback and post-cleaning operations.

RELIABILITY

Interconnect reliability results continue to be excellent for 4-Mb manufacturing parts fabricated with either RIE or Dual Damascene; the new technology adds reliability margin for step coverage, electromigration, and corrosion.

Electromigration / Step Coverage

Both current-crowding and step-coverage concerns, at the transition from vertical stud to horizontal line, are mitigated by the Dual Damascene's self-alignment and monolithic metal structure. A single-metal deposition forms both stud and interconnect and eliminates the normal stud-to-interconnect interface. Self-alignment maximizes the metal cross-sectional area, virtually eliminating step-coverage concerns at this critical reliability juncture (Figure 5).

Corrosion

Chemical-mechanical metal etchback avoids corrosive RIE process residues. The Dual Damascene sequence also confines chemical attack to a single metal surface -- the top -- which is easily accessible for cleaning and any required chemical quench. These features combine to reduce both in-process and future susceptibility to corrosion failure.

PERFORMANCE

RC Losses

Dual Damascene performance benefits from planarization and vertical studs in the same way as a previously reported technology where a performance gain of 24% was reported,[4, 5] compared to a technology where the interconnects must traverse topography disrupted by underlying features. Vertical

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studs provide increased flexibility in the optimization of the interlevel dielectric thickness for minimum capacitive loss and increase wirability, allowing more wiring flexibility and better performance.

Contact Resistance

The number of metal interfaces for a multilevel wiring technology is reduced by 50% when compared to a more conventional stud technology. Within each level, Dual Damascene's monolithic structure eliminates the stud-to-interconnect, contact interface, and all related contact resistance issues. The "interface" becomes a continuum of bulk material, molded by the concurrent deposition of stud and interconnect metal into the insulator grooves (Figures 3, 5). Of course, level-to-level contact resistance issues persist.

EXTENDIBILITY

Increased Metallurgical Options

Damascene patterning with CMP provides increased metallurgical options unconstrained by RIE requirements. Increased flexibility is gained for optimizing resistivity and electromigration resistance, and process integration. Additional material options include Au, Cu, and tailored Al alloys. This metallurgical freedom stems from the fundamental difference between the RIE and chemical-mechanical etch processes. To remove unwanted metal, reactive-ion etch requires the production of volatile metal species; CMP does not. CMP can effectively remove a wider assortment of materials.

Density

The Dual Damascene mask-and-etch sequence provides self-aligned, fully covered contact/vias by overpassing metal. This desirable situation minimizes interconnect-to-adjacent stud shorts, which makes it practical to tighten wired pitch (interconnect pitch with vertical stud) to just two times the minimum photolithographic image. At the same time, the contact area of stud-to-overpassing interconnect is maintained. (Bias and tolerance complications are ignored here.) This represents a ground-rule improvement of one overlay, compared to other known wiring technologies (Figure 5). As we approach 256-Mb and 1-Gb DRAMs and their logic counterparts, these features can be expected to become common technology goals.

Other density-enhancing features are offered by the Dual Damascene technology; these features include compatibility with stacked via studs, unlanded vias, and multilevel aggressive-pitch structures.[3]

TECHNOLOGY CHALLENGES

The Dual Damascene technology challenges include metal gap-fill, interconnect etch-depth control, ground-rule restrictions and soft-metal CMP. All these problems have been successfully addressed or avoided in the 4-Mb manufacturing implementation, which uses a CVD-W metallurgy.

Metal gap-fill required by Dual Damascene is a demanding operation. Depth-to-width aspect ratios >5:1 must be filled in future technologies. Conformal CVD depositions are ideal, but other methods like electroplating[6], selective CVD, and collimated sputtering[7] are possible. Controlling the interconnect recess depth is another challenge, partially offset by the increasing sophistication of today's insulator etch tools, and can be avoided completely with the addition of an etch-stop material laminated within the insulator stack[8] .

Ground-rule restrictions on metal line width result from CMP's tendency to dish down into the center of wide metal features (Figure 6). Another ground-rule constraint is the relative ratio of the conductor to the surrounding insulator. There must be a sufficiently large insulator surface area relative to the metal pattern to avoid unacceptable thinning; it is not solely sufficient for the CMP metal-to-insulator etch-rate ratio to be very large (>200:1).

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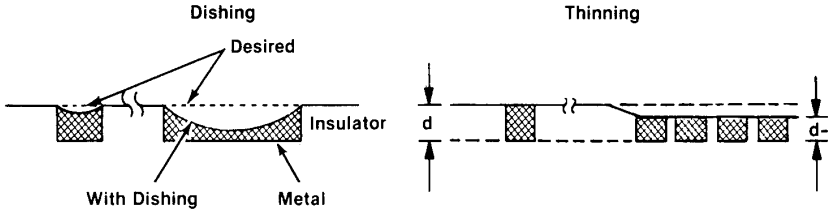

Figure 6. CMP dishing/thinning.

Anisotropic attack of the stacked stud and interconnect masks can contribute to unacceptable bias during the in situ insulator etch. This effect can be mitigated with a judicious choice of etch processes, mask pre-treatments, masking materials and insulator materials. Finally CMP scratching and smearing of soft metals conductors can occur.

SUMMARY

A new wiring technology called Dual Damascene has been described. It offers a unique process sequence and structure for multiple wiring levels (each with inherent planarity). The planarity, structure, and defect density control are the key elements used to improve manufacturing yield, cost, reliability, and future extendibility. A subset of the described technology features have been successfully implemented in the 200-mm volume production of IBM's 4-Mb DRAM. The more advanced scaling features offered, e.g., absolute minimum-wired pitch (minimum line / minimum space, with stud) with maximum stud-to-interconnect cross-sectional area, are expected to become a necessity as integration requirements for the 256-Mb DRAM and its successors are designed.

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