PROCESS INTEGRATION ISSUES OF LOW-PERMITTIVITY DIELECTRICS WITH COPPER FOR HIGH-PERFORMANCE INTERCONNECTS

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To Papa, Mummy, Alan, and Selene...

Abstract

The relentless drive toward high-speed and high-density silicon-based integrated circuits (IC's) has necessitated significant advances in interconnect technology. In current process technologies, transistors are interconnected by multilevel aluminum and tungsten conductors encased in silicon dioxide (oxide) insulators. Continued scaling of IC features exacerbates performance limitations and chip reliability due to interconnects, thus heightening the need to replace the existing interconnect system with lower resistivity conductors and lower permittivity insulators. Copper integrated with oxide has recently been announced as the next interconnect technology to enter IC manufacturing. The switch to copper reduces wire delay, improves electromigration reliability, and lowers manufacturing cost. Substantial improvements can further be achieved by incorporating low-permittivity (low-κ) dielectrics for capacitance reduction to mitigate wire delay, power dissipation, and crosstalk noise issues. The integration of low-κ dielectric with copper remains a very active process development effort in the semiconductor industry.

This dissertation explores process integration issues that dictate the design, performance, and reliability of low-κ polymer dielectric implementation with copper. In particular, the electrical isolation between interconnects is examined to identify potential sources of leakage conduction. Moisture as well as leakage along interfaces between the low-κ polymer and dielectric liners contribute detrimentally to electrical leakage. Next, the anisotropy in dielectric constant is investigated and a novel technique to measure the lateral dielectric constant is demonstrated. The lateral dielectric constant of a blanket dielectric film is determined to assess the effect of anisotropy on crosstalk noise. Finally, an extensive study of copper drift in various low-κ polymers is presented to address barrier requirements. An oxide-sandwiched low-κ dielectric capacitor structure was developed to facilitate the investigation. Copper ion penetration in low-κ polymers is accelerated by bias-temperature stressing and detected by capacitance–voltage and dielectric time-to-failure measurements. The copper drift properties in various families of low-κ polymers were evaluated and compared.

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Table of Contents

Abstract vii
Acknowledgments ix
List of Tables xvii
List of Figures xix

Chapter 1 Introduction 1
1.1 Limitations with Interconnect Scaling 3
1.1.1 Interconnect Delays 4
1.1.2 Reliability 6
1.1.3 Capacitance Issues 6
1.2 Interconnect Materials Options 8
1.3 Arrival of Copper Metallization 11
1.4 Marching Towards Low-Permittivity Dielectrics 13
1.5 Organization of Dissertation 16

Chapter 2 Review of Interconnect Integration 17
2.1 Conventional Technology 18
2.1.1 Fabrication of Tungsten Vias 18
2.1.2 Fabrication of Aluminum Alloy Wires 21
2.2 Dual-Damascene Copper Technology 23
2.2.1 Dielectric Etch 26
2.2.2 Metal Barrier Deposition 28
2.2.3 Copper Deposition 30
2.2.4 Chemical-Mechanical Polishing 33
2.2.5 Dielectric Barrier Passivation 35
2.3 Summary 35

Chapter 3 Low-Permittivity Dielectrics 37
3.1 Strategies for Dielectric Constant Reduction 37
3.2 Survey of Available Materials 39
3.3 Investigated Dielectrics 43
3.3.1 Polyarylene Ether 43
3.3.2 Aromatic Hydrocarbon 45
3.3.3 Fluorinated Polyimide 45

3.3.4 Benzocyclobutene 46
3.3.5 Parylene-F 47
3.4 Summary 48

Chapter 4 Interconnect Isolation 49
4.1 Dielectric Liners 50
4.2 Dielectric Interface Leakage 51
4.2.1 Fabrication of Test Structures 52
4.2.2 Electrical Testing 55
4.2.3 Experimental Results 58
4.2.3.1 Moisture Instability 58
4.2.3.2 Leakage Comparison 59
4.2.3.3 Leakage Path Determination 61
4.2.3.4 Analysis of Electrical Results 63
4.2.3.5 Metal/Polyimide Interfacial Stability 63
4.2.4 Implications on Process Integration 64
4.3 Summary 66

Chapter 5 Dielectric Constant Anisotropy 67
5.1 Conventional Measurement Techniques and their Limitations 68
5.1.1 Optical Prism Coupler 69
5.1.2. Crosstalk Capacitance of Gapfilled Interdigitated Lines 70
5.2 Electrical Anisotropy of a Blanket Dielectric 72
5.2.1 Theory of Measurement 72
5.2.2 Fabrication of Test Structures 74
5.2.3 Electrical Testing 75
5.2.4 Experimental Results 76
5.2.5 Simulations and Modeling 77
5.2.6 Extraction of In-plane Dielectric Constant 80
5.2.7 Measurement Issues 81
5.3 Summary 84

Chapter 6 Copper Drift in Dielectrics 85
6.1 Detection of Copper Drift 87
6.1.1 Capacitance–Voltage Analysis 87
6.1.2 Dielectric Time-to-failure Measurements 95
6.2 Copper Drift in Low-Permittivity Polymers 97

6.2.1 Fabrication of Test Structures 98
6.2.2 Electrical Testing 101
6.2.3 Interface Instabilities 104
6.2.4 Capacitance–Voltage Analysis 107
6.2.5 Model of Copper Drift Kinetics 109
6.2.6 Extraction of Copper Drift Rates 113
6.2.7 Dielectric Time-to-failure Measurements 115
6.2.8 Discussion 118
6.3 Summary 121

Chapter 7 Conclusion 123
7.1 Summary 123
7.2 Suggestions for Future Work 125

Appendix Capacitor Process Flow 127

Bibliography 135

List of Related Publications 147

List of Tables

Chapter 1 Introduction

Table 1-1: Roadmap for Interconnect Technology (Logic) [24] 8

Table 1-2: Candidate Metals for Advanced Interconnects 9

Table 1-3: Families of Candidate Low-κ Dielectrics for Advanced Interconnects 10

Table 1-4: Current Status of Copper Technology in Semiconductor Industry [30] ... 13

Chapter 2 Review of Interconnect Integration

Table 2-1: Interconnect Design Rules for 0.25-µm Technology [18] 23

Table 2-2: Comparison of Dual-Damascene Dielectric Etch Approaches [48] 28

Chapter 3 Low-Permittivity Dielectrics

Table 3-1: Property Requirements of Low-κ Dielectrics 39

Table 3-2: Families of Candidate Low-κ Dielectrics for Advanced Interconnects 40

Table 3-3: Investigated Low-κ Dielectrics 43

Chapter 5 Dielectric Constant Anisotropy

Table 5-1: Anisotropy in FPI-136M Fluorinated Polyimide 81

Chapter 6 Copper Drift in Dielectrics

Table 6-1: Low-κ Polymer Dielectrics for Evaluation of Copper Drift 99

Table 6-2: Trends between Copper Drift Rate and Polymer Properties 118

List of Figures

Chapter 1 Introduction

Figure 1-1 Trends in the semiconductor industry [4]–[7]. 2

Figure 1-2 Cross-sectional scanning electron micrograph of state-of-the-art 0.25-µm CMOS multilevel interconnect technology for high-performance logic. Courtesy of Motorola. 3

Figure 1-3 Intrinsic gate and interconnect delays as a function of minimum feature size [10]. 4

Figure 1-4 Impact of line-to-ground and line-to-line coupling on total interconnect capacitance [19]. 7

Figure 1-5 Number of metal layers for various interconnect materials options [9]. .. 11

Figure 1-6 Scanning electron micrographs of interconnect architecture with six levels of Cu lines/vias, W contacts/local interconnects, and SiO_2 ILD. Demonstrations by (a) IBM [27] and (b) Motorola. Lower figure provided courtesy of Motorola. 12

Figure 1-7 Cross-sectional scanning electron micrographs of industry demonstrations of Cu integration with various low-κ dielectrics: (a) polyimide (κ = 2.9) [31], (b) silsesquioxane (κ = 2.2) [32], and (c) xerogel (κ = 1.8) [33]. 14

Figure 1-8 Cross-sectional scanning electron micrograph of multilevel integration of hydrogen silsesquioxane (κ = 3.0) with Al metallization [35]. The low-κ dielectric is embedded between adjacent interconnects in the same level primarily for reducing lateral crosstalk capacitance. 15

Chapter 2 Review of Interconnect Integration

Figure 2-1 Cross-sectional scanning electron micrograph of state-of-the-art 0.25-µm CMOS multilevel interconnect technology for high-performance logic. Courtesy of Motorola. 18

Figure 2-2 Process flow for fabrication of tungsten vias. 20

Figure 2-3 Process flow for fabrication of aluminum alloy wires. 22

Figure 2-4 Scanning electron micrograph of manufacturable copper interconnect architecture demonstrated by IBM [27]. 24

Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects. 25

Figure 2-6 Dual-Damascene variations for defining wire trenches and via holes: (a) buried etch stop, (b) clustered, (c) partial via first, (d) full via first, and (e) line first approaches. 26–27

Figure 2-7 Comparison of ideal and typical step coverages of a metal barrier deposited by PVD [57]. 30

Figure 2-8 Schematic of a Cu electroplating system. 32

Figure 2-9 Schematic of a typical chemical-mechanical polishing system. 34

Chapter 3 Low-Permittivity Dielectrics

Figure 3-1 Frequency response of dielectric mechanisms [69]. 38

Figure 3-2 Structural formula of a hydrogen silsesquioxane spin-on glass..... 41

Figure 3-3 Structural formula of two polyarylene ethers: (a) Schumacher PAE-2 [77] and (b) Asahi Chemical ALCAP-E [78]. Ar, Ar', and Ar'' are proprietary aromatic groups. 44

Figure 3-4 Structural formula of DuPont FPI-136M fluorinated polyimide [82]..... 45

Figure 3-5 Structural formula of Dow Chemical Cyclotene™ 5021 benzocyclobutene (BCB) monomer [83]. 46

Figure 3-6 Structural formula of Novellus AF-4 parylene-F [85]. 47

Chapter 4 Interconnect Isolation

Figure 4-1 Cross-section of Damascene Cu and low-κ polymer dielectric integration scheme illustrating incorporation of thin oxide liners. The nitride liner passivates the top Cu surface to prevent Cu diffusion and drift from the inter-

connect into a low-κ polymer with poor Cu barrier property. 50

Figure 4-2 Use of oxide hard mask for patterning low-κ dielectric. 51

Figure 4-3 Plan view schematic of interdigitated metal test structure. 52

Figure 4-4 Cross-sectional schematic of experimental splits: (a) polyimide-passivated Damascene Al(Cu), (b) unpassivated Damascene Al(Cu), (c) oxide-passivated Damascene Al(Cu), and (d) oxide-gapfilled RIE Al(Cu). The metal lines have the same line width and spacing of 0.5 µm..... 53

Figure 4-5 Scanning electron micrograph of polyimide-passivated Damascene Al(Cu) after polyimide etch illustrating polished Al(Cu) lines and polyimide sidewall..... 54

Figure 4-6 Electrical setup to measure intralevel leakage current at 100–275°C. 55

Figure 4-7 High-frequency (1 MHz) *C–V* measurements demonstrating that Si surface is in accumulation at zero gate bias. *Comb1*, *serpentine*, and *comb2* were shorted together as the common gate electrode. 56

Figure 4-8 Typical *I–V* characteristics of intralevel leakage at 150°C for (a) polyimide-passivated Damascene Al(Cu), (b) unpassivated Damascene Al(Cu), (c) oxide-passivated Damascene Al(Cu), and (d) oxide-gapfilled RIE Al(Cu). The I_{comb} regression slopes are used for comparisons. 57

Figure 4-9 Moisture-related leakage instability at 150°C. 58

Figure 4-10 Residual gas analysis of fluorinated polyimide film heated to 200°C in vacuum. 59

Figure 4-11 Leakage conductance at 150°C after 24-hour bake at 150°C. 60

Figure 4-12 Arrhenius plot of leakage conductance after a 24-hour bake at 150°C. .. 60

Figure 4-13 Experiment to distinguish between (a) interfacial and (b) bulk leakage paths in polyimide film. 61

Figure 4-14 $I_{serp} / I_{comb2} \approx C_{serp} / C_{comb2} \approx 5$ for bulk polyimide conduction. Simulated equipotentials are shown. 62

Figure 4-15 I_{serp} and I_{comb2} after (a) 0.1-hour and (b) 25-hour bake at 150°C with *ser-*

pentine and *comb2* grounded. 62

Figure 4-16 Rutherford backscattering spectra of fluorinated polyimide on Al(Cu), as-deposited and after 30-minute anneals at 150–400°C. 64

Figure 4-17 (a) Cross-sectional scanning electron micrograph illustrating Al(Cu)/parylene-F comb capacitor structure demonstrated by Texas Instruments. (b) Corresponding comb-to-comb leakage current with and without oxide liner encapsulation of interconnects [97]. 65

Chapter 5 Dielectric Constant Anisotropy

Figure 5-1 Cross-sectional scanning electron micrograph of Cu/polyimide interconnect system demonstrated by IBM. The polyimide has $\kappa_{\perp}$ and $\kappa_{||}$ of 2.9 and 3.7 respectively [47]. 68

Figure 5-2 Schematic of prism coupler technique for measuring n_{TM} and n_{TE}..... 70

Figure 5-3 (a) Measurement of $\kappa_{||}$ from crosstalk capacitance between metal lines gap-filled with polymer dielectric. (b) Technique is limited in part by poor dielectric gapfill [103]. 71

Figure 5-4 Cross-section of interdigitated Al(Cu) test structure, inlaid in oxide and passivated by a blanket dielectric. 73

Figure 5-5 Linear interpolation to extract κ_{top}, the effective dielectric constant of the polyimide passivation. 73

Figure 5-6 Plan view schematic of interdigitated metal test structure. *Comb1* and *comb2* are externally connected together to be a common *comb* electtrode. 74

Figure 5-7 Cross-section of experimental splits: (a) unpassivated Damascene Al(Cu), (b) polyimide-passivated Damascene Al(Cu), and (c) oxide-passivated Damascene Al(Cu). 74

Figure 5-8 Electrical setup to measure lateral crosstalk capacitance between *serpentine* and *comb*. 76

Figure 5-9 Effective dielectric constant of DuPont FPI-136M fluorinated polyimide. 77

Figure 5-10 *Serpentine* resistance at 150°C showing agreement with variations in capacitance resulting from process nonuniformity. 77

Figure 5-11 Confirmation of extraction technique by capacitance simulations. 78

Figure 5-12 Simulated (a) potential contours for polyimide passivation and (b) electric field rolloff along half-plane midway between adjacent metal lines. 79

Figure 5-13 Simulated dependence of $C_{crosstalk}$ on passivation dielectric thickness. Minimum thickness for accurate extraction is 1.0 µm. The metal line spacing is 0.5 µm. 80

Figure 5-14 (a) Fringing fields traverse through both in-plane and out-of-plane directions. (b) Measurement of $\kappa_{\perp}$ from a parallel-plate capacitor with large area. A known $\kappa_{\perp}$ is required to extract $\kappa_{\parallel}$ from κ_{top} in capacitance simulations. 81

Figure 5-15 Distributed *RC* model of *comb1/serpentine/comb2* test structure. 82

Figure 5-16 Simulations illustrating effect of number of distributed *RC* elements, *n*, on modeling crosstalk capacitance measurements of the unpassivated *comb1*/*serpentine*/*comb2* structure. 83

Figure 5-17 Simulations illustrating effect of substrate resistance, R_{sub}, on measured crosstalk capacitance of unpassivated lines. 84

Chapter 6 Copper Drift in Dielectrics

Figure 6-1 Cross-section of potential Cu and low-κ polymer dielectric integration scheme illustrating encapsulation of copper interconnects with metal and dielectric barriers. 86

Figure 6-2 Bias-temperature stressing of Cu-insulator-Si capacitors to accelerate penetration of Cu^{+} ions into a dielectric. 87

Figure 6-3 Effect of trapped charges in the dielectric on the high-frequency *C–V* behavior. 88

Figure 6-4 Effect of interface charge traps at the Si interface on the high-frequency *C–V* behavior. Electron traps are assumed. 89

Figure 6-5 Capacitor structure for evaluating Cu drift in PECVD dielectric: oxide ($\kappa = 4.1$) and oxynitride ($\kappa = 5.1$). Gate area is 1 mm^2. 90

Figure 6-6 *C–V* characteristics of PECVD oxide capacitors at 20°C after stressing under +20 V gate bias (+1.0 MV/cm) at 175°C for 0, 1, 2, and 3 hours... 91

Figure 6-7 Negative bias-temperature instabilities in PECVD oxide capacitors stressed under -20 V gate bias (-1.0 MV/cm). 92

Figure 6-8 ΔV_{FB} as a function of stress time and temperature for PECVD oxynitride capacitors stressed at +20 V (+1.0 MV/cm). 93

Figure 6-9 SIMS analysis of Cu capacitors with oxide and oxynitride dielectrics. Capacitors were stressed at +20 V (+1.0 MV/cm) and 250°C for one hour. The Cu gates were stripped by wet-etching prior to analysis. 94

Figure 6-10 (a) Cu-gate thermal oxide capacitors. (b) Typical I_{gate} transient of capacitor stressed to breakdown at 200°C under +10 V bias (+2 MV/cm). Gate area is 2 mm^2. 96

Figure 6-11 Arrhenius plot of time-to-failure of Cu-gate thermal oxide capacitors stressed at various gate biases corresponding to 2.0–3.5 MV/cm. 97

Figure 6-12 Oxide-sandwiched low-κ polymer capacitor for evaluating Cu drift in low-κ polymer. Gate area is 1 mm^2. 98

Figure 6-13 Effect of forming gas anneal at 350°C for one hour on *C–V* characteristics. PECVD oxide capacitors with Al electrodes are used for the illustration. 100

Figure 6-14 Experimental setup for electrical testing. To prevent moisture uptake in the polymer, all measurements and stressing were conducted without breaking the N_2 ambient. 101

Figure 6-15 $\kappa_{polymer}$ transient demonstrating moisture uptake in low-κ polymer after exposure to 40% RH air at 20°C. Prior to exposure, the capacitors were heated to 200°C. PI is abbreviated for DuPont PI-2556 PMDA-ODA (pyromellitic dianhydride — oxydianiline) polyimide. 102

Figure 6-16 Leakage current characteristics of raised probe tips (I_{tip}) and hot chuck (I_{chuck}) in the N_2-purged probe station. The hot chuck was maintained at

300°C during the measurement. 103

Figure 6-17 *C–V* characteristics demonstrating interface-related instabilities at the polymer/Si interface. Virgin capacitors were stressed at ±35V and 20°C for various durations preceding the *C–V* sweeps. 104

Figure 6-18 *C–V* characteristics showing no interface-related instability at both Al/oxide and oxide/Si interfaces. Virgin capacitors were stressed at -35 V and 20°C for various durations preceding the *C–V* sweeps..... 105

Figure 6-19 *C–V* characteristics demonstrating interface-related instabilities at the Al/polymer interface. Virgin capacitors were stressed at 300°C for one hour under various gate biases. 106

Figure 6-20 *C–V* characteristics of oxide-sandwiched (a) PAE, (b) FPI, and (c) BCB capacitors stressed at 200°C for one hour under various gate biases..... 108

Figure 6-21 *C–V* characteristics of nitride control capacitors stressed at 200°C for one hour under various gate biases. 109

Figure 6-22 I_{gate}–V_{gate} sweeps of oxide-sandwiched PAE, FPI, and BCB capacitors at 200°C under +20-V gate bias..... 110

Figure 6-23 I_{gate}–t characteristics of oxide-sandwiched PAE, FPI, and BCB capacitors at 200°C. The I_{gate}–V_{gate} traces were obtained using a relatively quick V_{gate} sweep time of 1.0 minute to minimize dielectric charging. 110

Figure 6-24 Energy band diagram illustrating proposed kinetics of Cu^+ penetration under positive V_{gate} stress. Cu atoms ionize, penetrate into the dielectric, and then accumulate in the dielectric as Cu^+ space charge. For the purpose of illustration, the band structure of the low-*K* polymer is assumed to match that of oxide. 111

Figure 6-25 Measured ΔV_{FB} transients (○) compared to model predictions (-----) for Cu-gate (a) PAE and (b) FPI capacitors. 112

Figure 6-26 Arrhenius plot of initial Cu^+ drift rates and corresponding activation energies in various dielectrics. Drift rates were extracted from I_{gate}–V_{gate} measurements at an electric field of 0.8 MV/cm, except for PECVD oxynitride which was extracted at a field of 1.0 MV/cm. 114

Figure 6-27 *C–V* characteristics of deposited oxide control capacitors stressed at 200°C for one hour under various gate biases..... 115

Figure 6-28 Time-dependent dielectric breakdown (TDDB) experiments of Cu-gate capacitors stressed at 250°C under +60-V bias. (a) Typical I_{gate} transients, and (b) capacitor time-to-failure (*TTF*) distribution. *TTF* was defined as stressing time required for I_{gate} to reach 10 µA..... 116

Figure 6-29 Correlation between median *TTF*'s and initial drift rates at 250°C. 117

Chapter 1 Introduction

It began with the inventions of the transistor in 1947 [1] and the integrated circuit (IC) in 1958 [2]. Fifty years later, the IC industry bears little resemblance to its innocent beginnings [3]. Today's IC's are orders of magnitude smaller, faster, cheaper, and more reliable than their early counterparts. Modern IC fabs with pricetags exceeding US$1 billion are already commonplace. Yet, the corporations that finance these enormous investments are actively speculated to grow well in excess of current profit levels. Though maturing, the dynamic IC sector remains a hotbed of lucrative opportunities and future potential.

The exponential growth in IC production has been fueled by ever increasing demand for high-performance, low-power, and compact silicon-based microelectronic products that are relatively inexpensive and extremely reliable. To date, the industry continues to meet this demand because of ongoing advances in silicon (Si) wafer growth and semiconductor manufacturing technologies, enabling more and more transistors to be packed onto a single chip. The increased level of integration is realized primarily through reductions in the physical size of the transistor and a concurrent growth in chip size. These trends are summarized in Figure 1-1 [4]–[7].

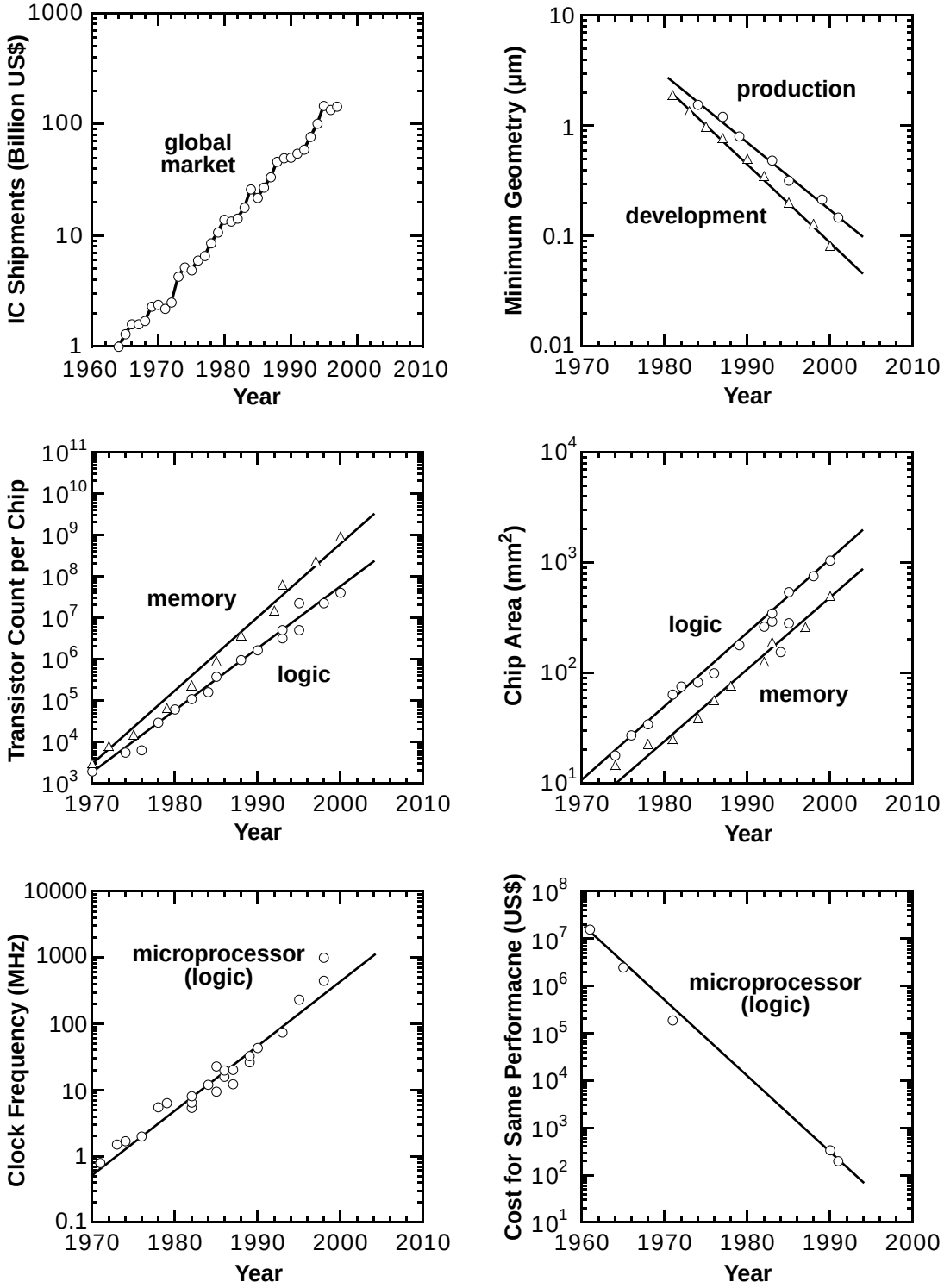


Figure 1-1 Trends in the semiconductor industry [4]–[7].

1.1 Limitations with Interconnect Scaling

IC performance is dictated by the delays arising from propagation of electrical signals through the circuit. These delays have traditionally been associated with transistor switching. Performance improvements have thus been achieved primarily through reductions in the size of transistor geometries, most notably the gate length in MOS technology [8]. With this paradigm, the industry has enjoyed continual improvements in IC performance until only recent years.

The scaling of transistors has necessitated an increase in wiring density to accommodate increasing transistor densities over larger chip areas [9]. This has been made possible by advances in interconnect technology enabling continued miniaturization of interconnects as well as stacking of additional levels of metallization. Figure 1-2 illustrates a state-of-the-art interconnect architecture for the 0.25-µm technology generation.

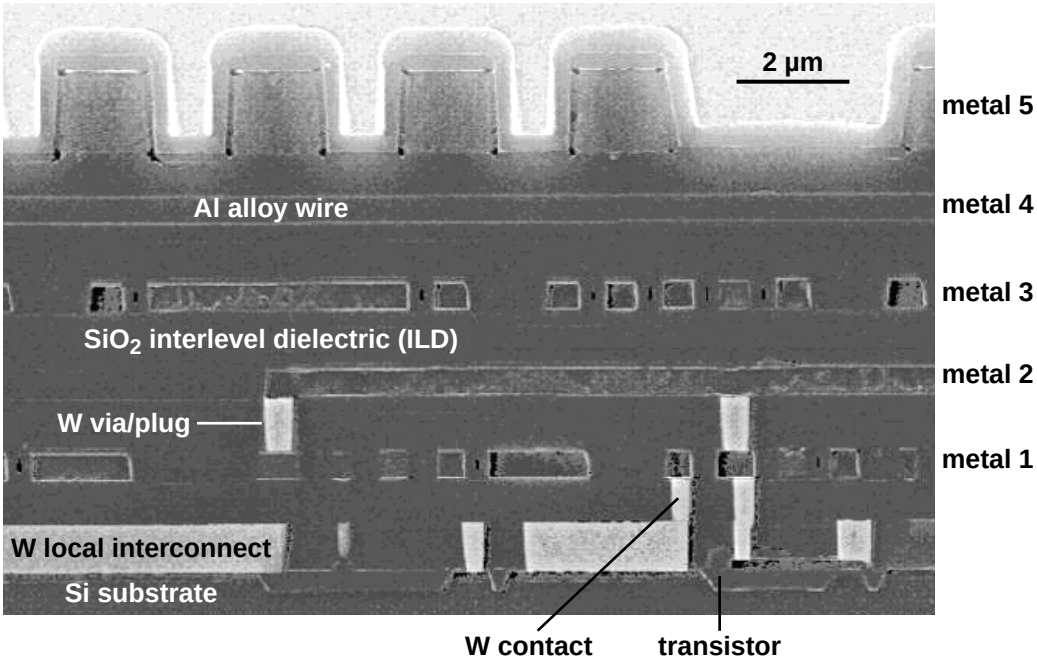


Figure 1-2 Cross-sectional scanning electron micrograph of state-of-the-art 0.25-µm CMOS multilevel interconnect technology for high-performance logic. Courtesy of Motorola.

1.1.1 Interconnect Delays

Although signals propagate faster through transistors as dimensions are scaled down, propagation through interconnects unfortunately becomes slower. In fact, in submicron logic technologies, interconnects have become the performance limiter (Figure 1-3) [10]. Moreover, the increasing complexity of multilevel wiring architectures has escalated the cost of interconnect manufacture to comprise over half of the total wafer processing cost [11]. For these reasons, the industry continues to invest large-scale efforts to develop cost-effective technological and design solutions which can overcome the pending interconnect problem.

The interconnect delay can be estimated by the *RC* delay— the product of interconnect line resistance, *R*, and the parasitic capacitance coupling the interconnect to adjacent lines and underlying Si substrate, *C*.

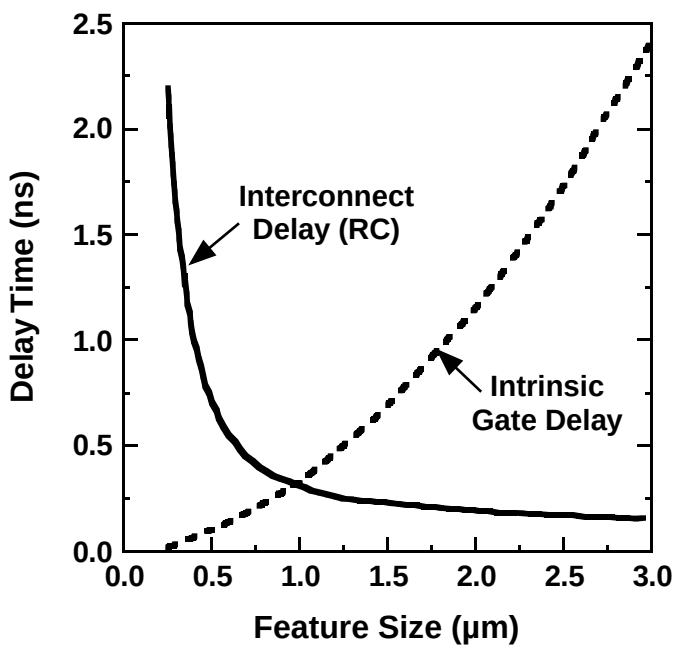


Figure 1-3 Intrinsic gate and interconnect delays as a function of minimum feature size [10].

$$RC \approx \rho\varepsilon \frac{L^2}{t_M t_{ILD}} \tag{1-1}$$

In Eq. (1-1), ρ, L, and t_M, are respectively the resistivity, length, and thickness of the interconnect, while ε and t_{ILD} are respectively the permittivity and thickness of the interlevel dielectric (ILD). For convenience, ε is usually cited in terms of the dielectric constant, κ, defined as $\varepsilon/\varepsilon_0$ where ε_0 is the permittivity of free space.

Various options exist to reduce *RC* delays. In some cases, the length of an interconnect in a critical path can be reduced if additional levels of wiring were available [12]. However, this solution provides little benefit to designs already optimized for maximum wiring and transistor densities. Moreover, extending any process flow will invariably increase cost and reduce chip yield. The *RC* delay can also be reduced by dividing long interconnects into shorter segments and inserting repeaters (inverter stages) between consecutive segments [13]. Repeaters sharpen slowly rising and falling transitions of a logic stage output, hence shortening the time required to trigger the input of subsequent logic stages. Repeaters are effective provided they can significantly reduce the effective *RC* load driven by the preceding stage. The penalty though is increased power consumption, chip area, and design cost. Yet another attempt to minimize interconnect delay is to lower the IC operating temperature where both interconnect propagation and device switching are faster [14]. Unfortunately, the added complexity and cost of cooling the chip can only be justified in niche applications where performance is the only objective.

The technological solution for *RC* delay reduction is to replace the existing conductors and insulators that comprise the interconnect system with lower ρ and κ materials. As shown in Figure 1-2, the conventional architecture consists of aluminum (Al) alloy conductors ($\rho \approx 3.0$–3.3 $\mu\Omega$-cm) isolated by silicon dioxide (SiO_2) or oxide ($\kappa = 4.0$–4.5) with adjacent storeys of Al wires connected by tungsten (W) vias ($\rho \approx 5.7$ $\mu\Omega$-cm). Candidate metal and dielectric replacements are discussed in Section 1.2.

1.1.2 Reliability

Interconnect reliability is also compromised by scaling and is arguably a more pressing concern than *RC* delays in many IC products [15]–[17]. Since supply voltages are not reduced as aggressively as the interconnect dimensions, interconnects must support higher current densities and are consequently prone to earlier electromigration failure. Electromigration is thermally activated atomic diffusion induced by an electron current. At current densities as high as those used in IC's, there is enough transfer of momentum from the electrons to the atoms of the conductor to cause a net atomic self-diffusion in the direction of electron transport. This mass movement changes the atomic density along the interconnect and consequently builds up mechanical stresses. Tensile stresses in the line eventually lead to formation of voids that ultimately cause open-circuit failures while compressive stresses lead to formation of hillocks that protrude through the encapsulating ILD and cause short-circuit failures with adjacent interconnects or interconnects in a different level.

Pure aluminum exhibits poor resistance against electromigration. To overcome this shortcoming, the industry has invested exhaustive efforts to improve the reliability of aluminum metallization, incorporating optimized microstructures, alloying with impurities, and cladding the interconnect with hard liner materials [18]. These sophistications have markedly prolonged the lifetime of Al interconnects to the point that failures are now concentrated to the intermetallic interfaces between the Al wires and W vias. With continued scaling though, it is questionable that extending an optimized Al interconnect technology can meet future reliability requirements. Alternative conductor systems with superior electromigration resistance are therefore under strong consideration.

1.1.3 Capacitance Issues

With minimum interconnect feature sizes now in the submicron regime, interconnect capacitance increases from continued scaling because of dominating line-to-line coupling between adjacent wires of the same metal level. See Figure 1-4. Besides the *RC* delay,

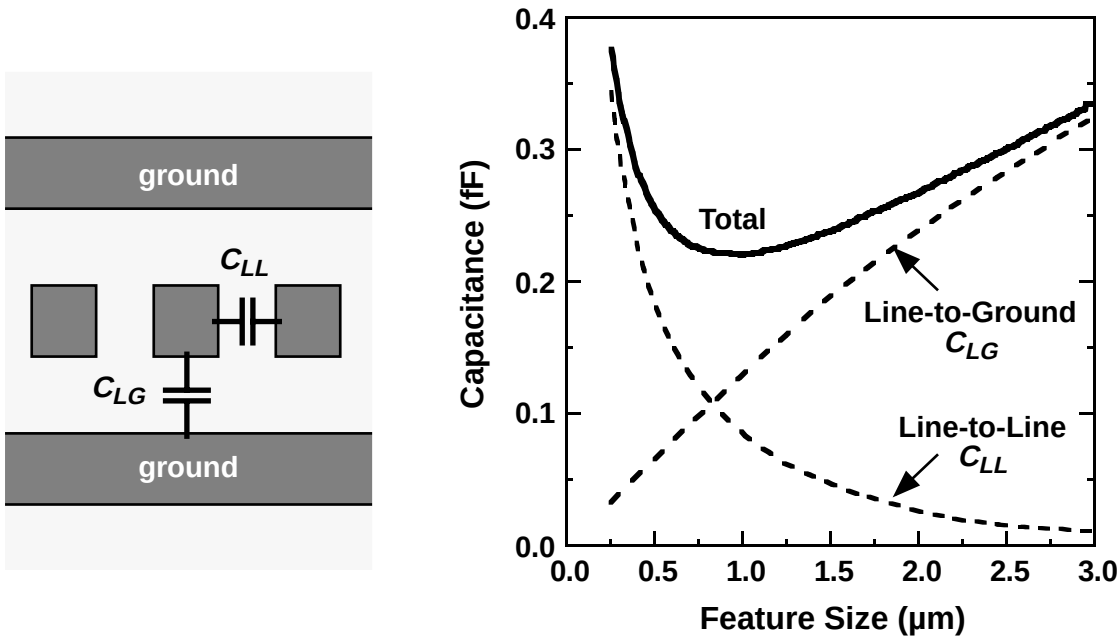


Figure 1-4 Impact of line-to-ground and line-to-line coupling on total interconnect capacitance [19].

capacitive parasitics also present other limitations on IC performance— dynamic power dissipation and crosstalk noise [19]–[22]. Continued scaling of interconnects will only exacerbate these issues and heighten the urgency to incorporate low-κ ILD's.

With increasing device densities and operating frequencies, the density of power that is generated on-chip also increases. Chips today operate at 85–120°C due to device and interconnect heating. This issue imposes increasing demands on already expensive packaging solutions to transport heat away from the chip in order to prevent quiescent temperatures from escalating even further. Otherwise, chip performance and reliability will degrade. On-chip power dissipation consists of both static and dynamic components. In MOS technology, static power dissipation is primarily due to transistor junction leakage. Dynamic power is dissipated during the switching transients in digital circuits and is estimated by Eq. (1-2).

$$P_{dynamic} = \frac{1}{2}\alpha C V^2 f \tag{1-2}$$

Here, C is the capacitive load at a circuit node, V is the power supply voltage, f is the clock frequency, and α represents the probability that the node transitions in a given clock cycle. Clearly, lower κ ILD's have a direct impact on dynamic power reduction.

Crosstalk noise is another undesirable consequence of interconnect scaling, most seriously affecting wires of minimum spacing. A propagating voltage transient in an interconnect will capacitively couple voltage transients into adjacent interconnects; the smaller the metal line separation, the larger the crosstalk peak voltage that is induced [23]. Therefore, for circuits to be resilient to crosstalk, supply voltages cannot be lowered too aggressively in order to maintain adequate noise margins. Lateral coupling can be minimized by manipulating the geometries (aspect ratios) of the lines and spaces, but altering aspect ratios only trades line-to-line for line-to-ground capacitance [20]. The robust answer to crosstalk minimization is still capacitance reduction with a low-κ ILD.

1.2 Interconnect Materials Options

To develop a perspective for evaluating low-ρ and low-κ candidates, it is prudent to examine the projected requirements for future IC's. See Table 1-1. Projections for logic

Table 1-1: Roadmap for Interconnect Technology (Logic) [24]

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Clock frequency (MHz)	750	1250	1500	2100	3500	6000	10000
Number of metal levels	6	6–7	7	7	7–8	8–9	9
Maximum interconnect length (m)	820	1480	2160	2840	5140	10000	24000
Minimum metal dimension (nm)	250	180	150	130	100	70	50
Metal aspect ratio (height/width)	1.8	1.8	2.0	2.1	2.4	2.7	3.0
Via aspect ratio	2.2	2.2	2.4	2.5	2.7	2.9	3.2
Metal effective resistivity ($\mu\Omega$-cm)	3.3	2.2	2.2	2.2	2.2	< 1.8	< 1.8
Barrier/cladding thickness (nm)	100	23	20	16	11	8	6
ILD effective dielectric constant	3.0–4.1	2.5–3.0	2.0–2.5	1.5–2.0	1.5–2.0	≤ 1.5	≤ 1.5

products are considered since high-performance logic, as opposed to memory (DRAM), is the driving force behind advanced interconnect development.

Several conductors have been actively researched as possible replacements for Al alloys. Unfortunately, only three elements exhibit lower resistivity than Al, namely gold (Au), silver (Ag), and copper (Cu). Among these metals, whose properties are listed in Table 1-2, Au has the highest resistivity. Although Ag has the lowest resistivity, it has poor resistance against electromigration. Cu exhibits an excellent combination of good electrical and mechanical properties, offering a resistivity 40% better than that of Al and the lowest self-diffusivity which translates to improved reliability. Based on these comparisons, Cu is the most promising choice for deep submicron interconnects.

Selecting a low-κ dielectric to replace SiO_2 is not as obvious. Table 1-3 summarizes the families of available dielectric materials most suitable for ILD integration. Unfortunately, these new materials impose integration constraints which are unfamiliar to an

Table 1-2: Candidate Metals for Advanced Interconnects

Property		Al	Au	Cu	Ag
Resistivity (μΩ-cm)		2.66	2.35	1.67	1.59
Self-diffusivity at 100°C (cm^2/s)		2.1×10^{-20}	2.2×10^{-27}	2.1×10^{-30}	1.1×10^{-26}
Electromigration resistance		low	high	high	very low
Availability of deposition and etching technique	sputtering	√	√	√	√
	evaporation	√	√	√	√
	CVD	√	√	√	?
	plating	?	√	√	√
	wet etching	√	√	√	√
	dry etching	√	?	?	?

Table 1-3: Families of Candidate Low-κ Dielectrics for Advanced Interconnects

Dielectric Materials	Dielectric Constant	Deposition Method
undoped plasma SiO_2	4.0–4.5	CVD
fluorinated SiO_2	3.5	CVD
spin-on glasses (silsesquioxanes)	2.2–3.0	spin-on
organic polymers (e.g., polyimides, parylenes, aromatic ethers)	2.0–3.9	spin-on / CVD
fluorinated amorphous carbon (α-C:F)	2.1–2.3	CVD
nanoporous dielectrics (e.g., xerogels)	1.2–2.2	spin-on

industry that understands primarily oxide ILD's. This shortcoming has stimulated a strong synergy between chipmakers and chemical vendors to co-develop better low-κ materials. Not surprisingly, the processing difficulties associated with each low-κ dielectric are commensurate with the corresponding permittivity advantage. Hence, traditionally conservative manufacturing practices will dictate progressive reductions in κ as outlined in the roadmap.

If successfully implemented, Cu and low-κ dielectrics can provide benefits illustrated in Figure 1-5. By achieving a higher wiring density with Cu and low-κ dielectrics, the required number of metal layers can be reduced, resulting in a potentially simpler process flow with enhanced yield and ultimately reduced cost.

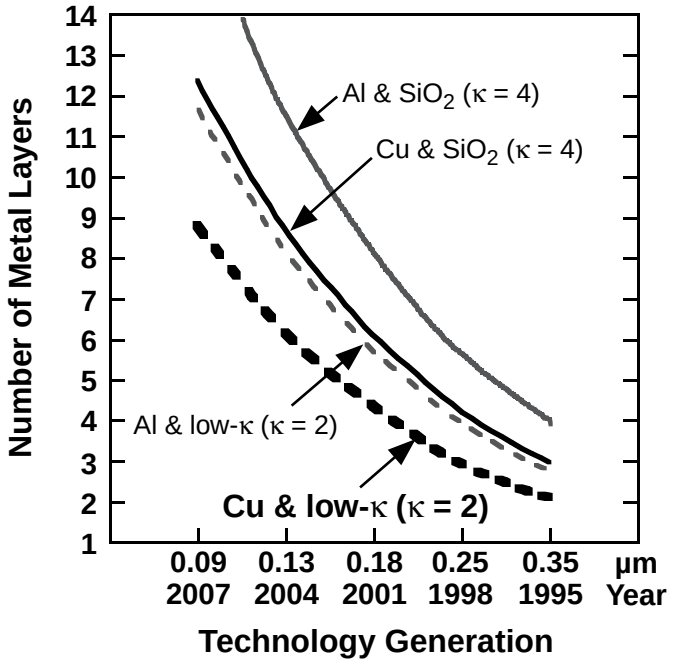
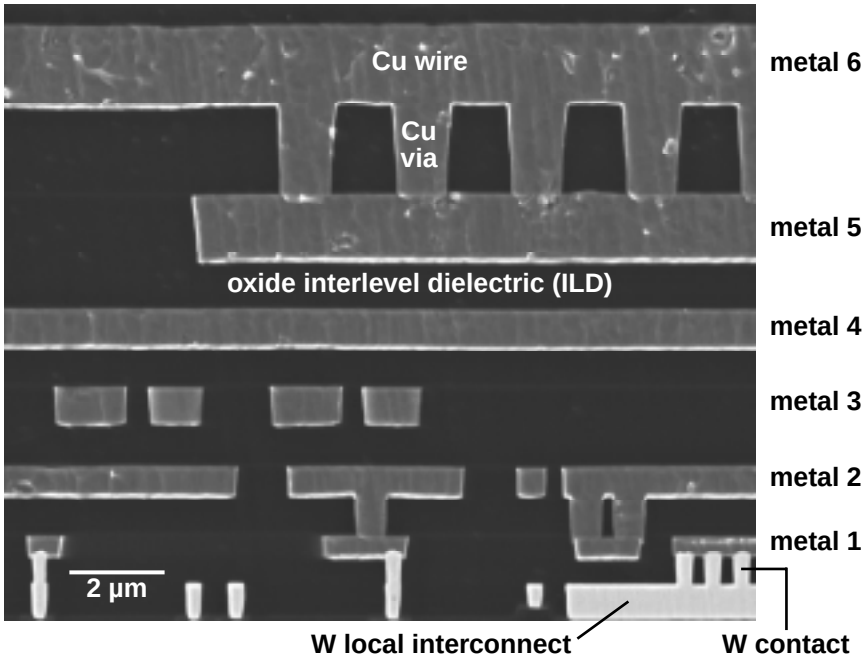


Figure 1-5 Number of metal layers for various interconnect materials options [9].

1.3 Arrival of Copper Metallization

Although Cu is a very promising interconnect material and has been actively explored for over a decade [25], [26], only recently has it been demonstrated as a feasible production technology. In September 1997, IBM and Motorola declared their intentions to incorporate Cu with oxide (SiO_2) in their next generation CMOS logic technologies (Figure 1-6) [27], [28]. Shortly after, the performance advantage of Cu interconnects was demonstrated in high-speed microprocessors [29]. What comes as a surprise is the claim that this performance improvement is achieved at a lower cost [27]. This attraction has energized an industry of conservative and reluctant chipmakers to accelerate their copper development programs. Many vendors of equipment and process consumables are now channeling significant efforts to provide the enormous manufacturing infrastructure that must support the new technology. Semiconductor manufacturers worldwide are anticipated to adopt Cu as the mainstream interconnect conductor by the turn of the century. See Table 1-4 [30].

(a)



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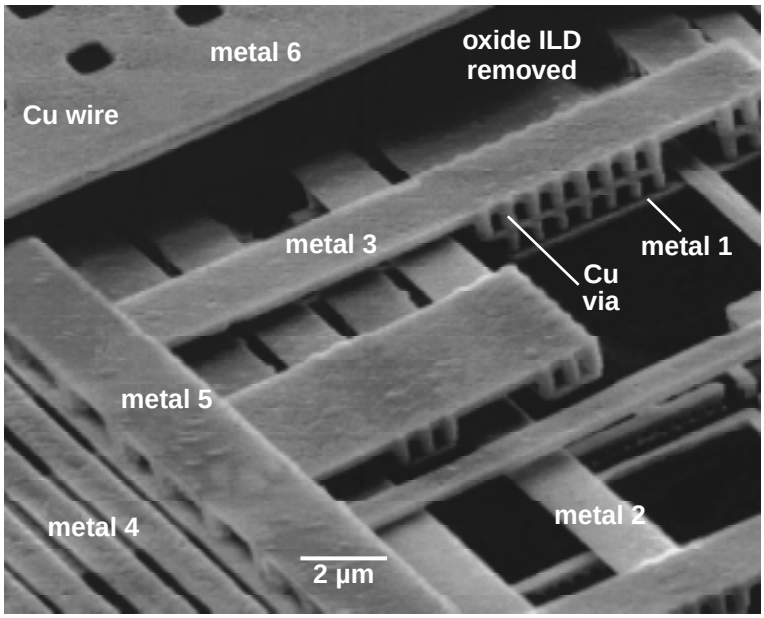


Figure 1-6 Scanning electron micrographs of interconnect architecture with six levels of Cu wires/vias, W contacts/local interconnects, and SiO_2 ILD. Demonstrations by (a) IBM [27] and (b) Motorola. Lower figure provided courtesy of Motorola.

Table 1-4: Current Status of Copper Technology in Semiconductor Industry [30]

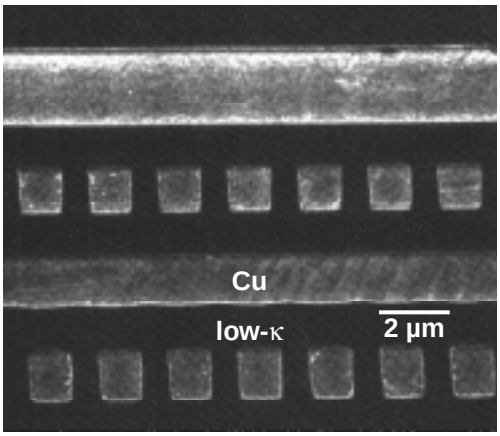
Chipmaker	Target for copper	Technology	Initial products
AMD	introducing in 2000	0.18 µm	microprocessors
IBM	ramping production now	0.20 µm	microprocessors, ASIC's
Intel	in production by 2001	0.13 µm	microprocessors
Motorola	sampling prototypes now	0.15 µm	microprocessors, SRAM's
NEC	introducing at end of 1999	0.15 µm	ASIC's
Philips	introducing in 2000	—	to be determined
Texas Instruments	in production in 2000	0.18 µm	microprocessors, DSP's
Samsung	in production by mid-1999	0.18 µm	microprocessors
Siemens	introducing in 2000	—	high-speed IC's
TSMC	offering in 2nd half 1999	0.18 µm	foundry designs
VLSI Technology	launching in 1999	0.15 µm	ASIC's
UMC	offering in 2nd half 1999	0.18 µm	foundry designs

The main integration challenges are patterning Cu lines and preventing potential device contamination. Discussed in Chapter 2, these issues are overcome respectively by using the Damascene process and by cladding the Cu interconnects with diffusion barriers.

1.4 Marching Towards Low-Permittivity Dielectrics

With the industry now committing to Cu, the natural extension for further performance improvements is to replace the oxide ILD with low-κ dielectrics. In fact, the combination of Cu and low-κ dielectric has been demonstrated by IBM as early as 1993 [31]. The integrated ILD was a polyimide with $\kappa = 2.9$. Very recently, an increasing number of companies are demonstrating capabilities to integrate Cu with other low-κ materials such as silsesquioxane [32] and xerogel [33]. Figure 1-7 illustrates a few examples. However,

(a)



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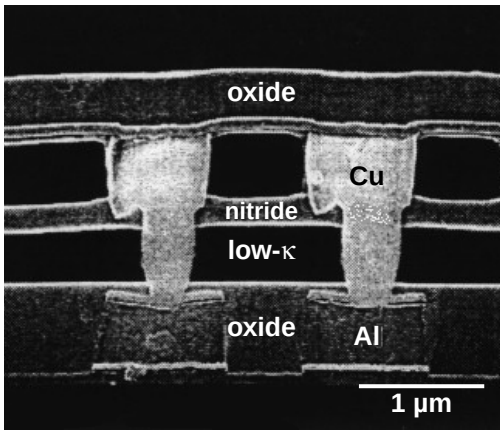

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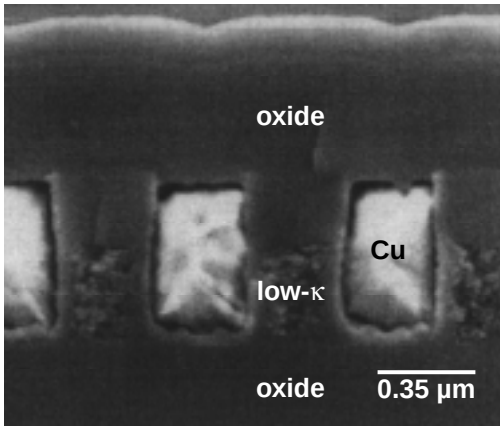


Figure 1-7 Cross-sectional scanning electron micrographs of industry demonstrations of Cu integration with various low-κ dielectrics: (a) polyimide (κ = 2.9) [31], (b) silsesquioxane (κ = 2.2) [32], and (c) xerogel (κ = 1.8) [33].

much work remains to demonstrate the cost-effectiveness of these new technologies to the point of justifying volume production.

Implementation of low-κ dielectrics with Damascene Cu represents only one approach. Extensive interconnect simulations have shown that in many IC's, low-κ ILD's alone offer more significant performance benefits than Cu [34]. This insight has motivated strong development efforts, concurrent with the development of Damascene Cu with oxide, to extend Al metallization to include low-κ dielectrics. The simplest extension is to incorporate fluorine in conventional oxide ILD's [21]. Fluorinating oxide films can reduce κ to as low as 3.5 before significant integration issues arise. More aggressive integration of low-κ dielectrics with Al alloys and W vias has also been successfully demonstrated with hydrogen silsesquioxane (κ = 3.0) [35], parylene-F (κ = 2.3) [36], and fluorinated amorphous carbon (κ = 2.3) [37]. Products with silsesquioxane ILD's are now available (Figure 1-8).

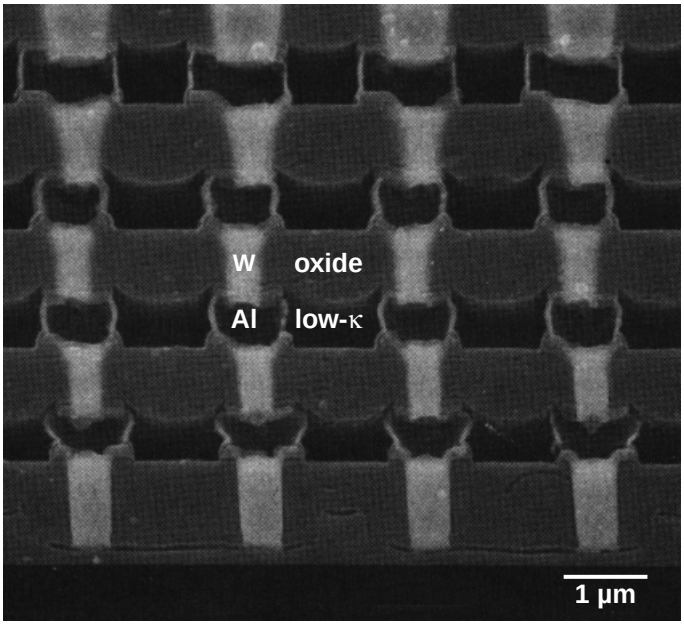


Figure 1-8 Cross-sectional scanning electron micrograph of multilevel integration of hydrogen silsesquioxane (κ = 3.0) with Al metallization [35]. The low-κ dielectric is embedded between adjacent interconnects in the same level primarily for reducing lateral crosstalk capacitance.

1.5 Organization of Dissertation

The development of Cu and low-κ dielectric interconnects is a significant industry-wide effort with much progress anticipated in the near future. This thesis explores some of the challenges associated with integrating both materials, focussing on organic polymers with dielectric constants of 2.4 to 2.8.

Having presented the motivations behind this work, the organization of this document is now outlined. Chapter 2 reviews the process integration of conventional and advanced interconnects, summarizing the salient features of conventional Al alloy and W metallization as well as the rapidly emerging Damascene Cu technology. Chapter 3 provides a brief overview of low-κ dielectric materials, concentrating on the organic polymers that were studied. These introductory chapters lay the foundation for understanding the context and applicability of three specific investigations that were explored in this dissertation. These areas of research, discussed in Chapters 4 to 6, address integration issues important in a successful implementation of Cu and low-κ polymer dielectrics. Finally, conclusions and suggestions for future research are offered in Chapter 7.

Chapter 2 Review of Interconnect Integration

The investigations to be presented in subsequent chapters assume a basic command of interconnect process technologies. This chapter provides an overview of interconnect integration, emphasizing key features in both conventional Al and Damascene Cu technologies. It is hoped that with this review, the less familiar reader will have acquired some relevant background information for comprehending the context of the work to follow.

In conventional silicon IC technologies, the interconnects are incorporated after frontend processing. Frontend processing refers to the sequence of fabrication steps, typically at very high temperatures (700–1100°C), that form the MOS transistors in the active regions, the pockets of thick isolation in the field regions that separate adjacent transistors, and the silicidation of the transistor terminals for low-resistance contacts. The reader is directed to [38]–[40] for a representative flavor of manufacturable advanced frontend technologies.

The backend, referring to the interconnection of transistors, is subsequently formed by contacting the transistor terminals and then vertically stacking alternating layers of metal wires and vias encased in dielectric. Backend process temperatures typically do not exceed 450°C to avoid melting of the metals and to control stress.

2.1 Conventional Technology

The state-of-the-art 0.25-µm backend, shown in Figure 2-1, is revisited to illustrate the integration of conventional Al metallization. The example consists of five levels of aluminum (Al) alloy wires and tungsten (W) vias (also called plugs or studs) embedded in oxide (SiO_2). Integration success is largely attributed to the processes that maintain excellent planarity after fabricating each and every via and wire level. The absence of topography helps to mitigate the fundamental depth-of-focus limitation of high-resolution lithography and avoid reliability problems such as metal line breaks over dielectric steps.

2.1.1 Fabrication of Tungsten Vias

The process sequence for forming tungsten vias is summarized in Figure 2-2 [40]. First, a thick blanket oxide film is deposited on a planar surface, typically by PECVD

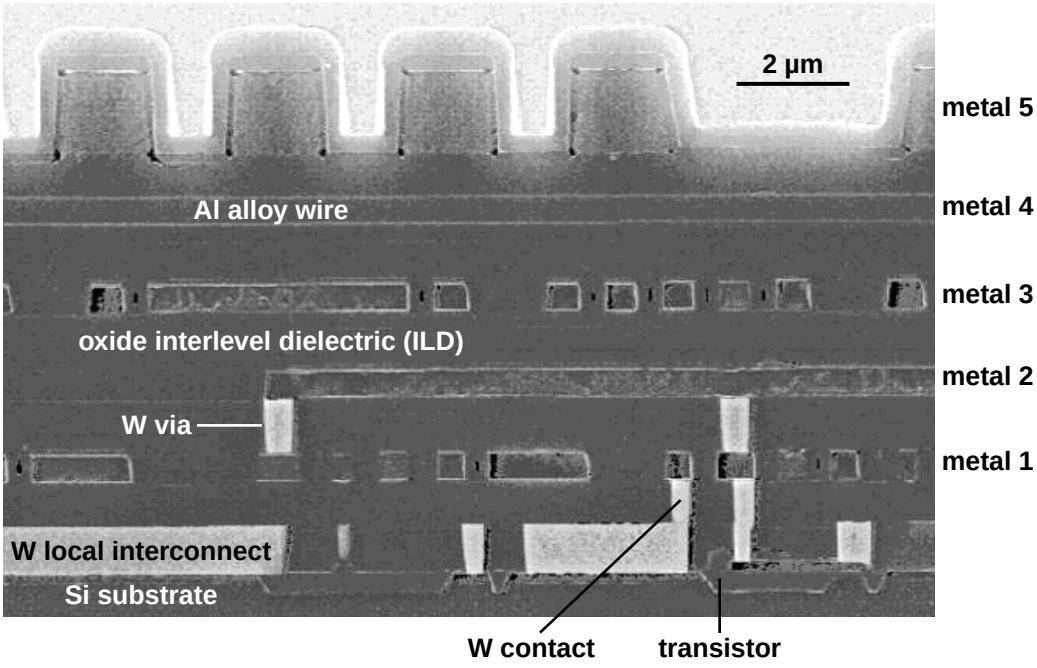


Figure 2-1 Cross-sectional scanning electron micrograph of state-of-the-art 0.25-µm CMOS multilevel interconnect technology for high-performance logic. Courtesy of Motorola.

(plasma-enhanced chemical vapor deposition) with a TEOS (tetraethyl orthosilicate) precursor at 350–400°C. The oxide ILD is patterned by photoresist and then etched to expose the underlying metal layer or contact level silicide. After the resist is stripped, the via opening is cleaned and then lined with a thin PVD titanium (Ti) layer. In modern CMOS technologies, PVD (physical vapor deposition) exclusively refers to sputtering. The Ti film serves as an adhesion layer and also decreases contact resistance to underlying conductors by reducing interfacial oxides. Titanium nitride (TiN) is subsequently deposited *in situ* either by sputtering or by CVD. Following that, the remaining part of the hole is conformally filled void-free with CVD tungsten at 425–450°C by SiH_4 reduction of WF_6. Here, the TiN barrier layer protects the CVD by-products from attacking the underlying Ti adhesion layer and oxide. The excess W, TiN, and Ti in the field regions are finally removed by chemical-mechanical polishing (CMP), making the top of the W via thus formed coplanar with the flat oxide surface. This method of embedding metal structures in dielectrics is known as the *Damascene* process, paying tribute to an ancient art that originated in Damascus. Jewellers then would inlay soft metals, such as gold, in precious stones by boring into the gem, filling the opening with metal, and polishing away the excess metal.

Tungsten via technology has matured to the point where void-free and untapered vias with aggressive aspect ratios exceeding 3:1 are routinely formed, thus enabling increases in wiring density and reduction of capacitive parasitics to under- and overlying wires. Advances in lithography alignment have also enabled borderless vias to be formed, thereby permitting even further improvements in wiring density. In addition, Damascene tungsten has been adapted as planar local interconnects for strapping source/drain and gate contacts [41]. Although this process is more difficult to control, successful implementation of tungsten local interconnects can reduce the cell size of SRAM's used as microprocessor cache memories by 20–30%.

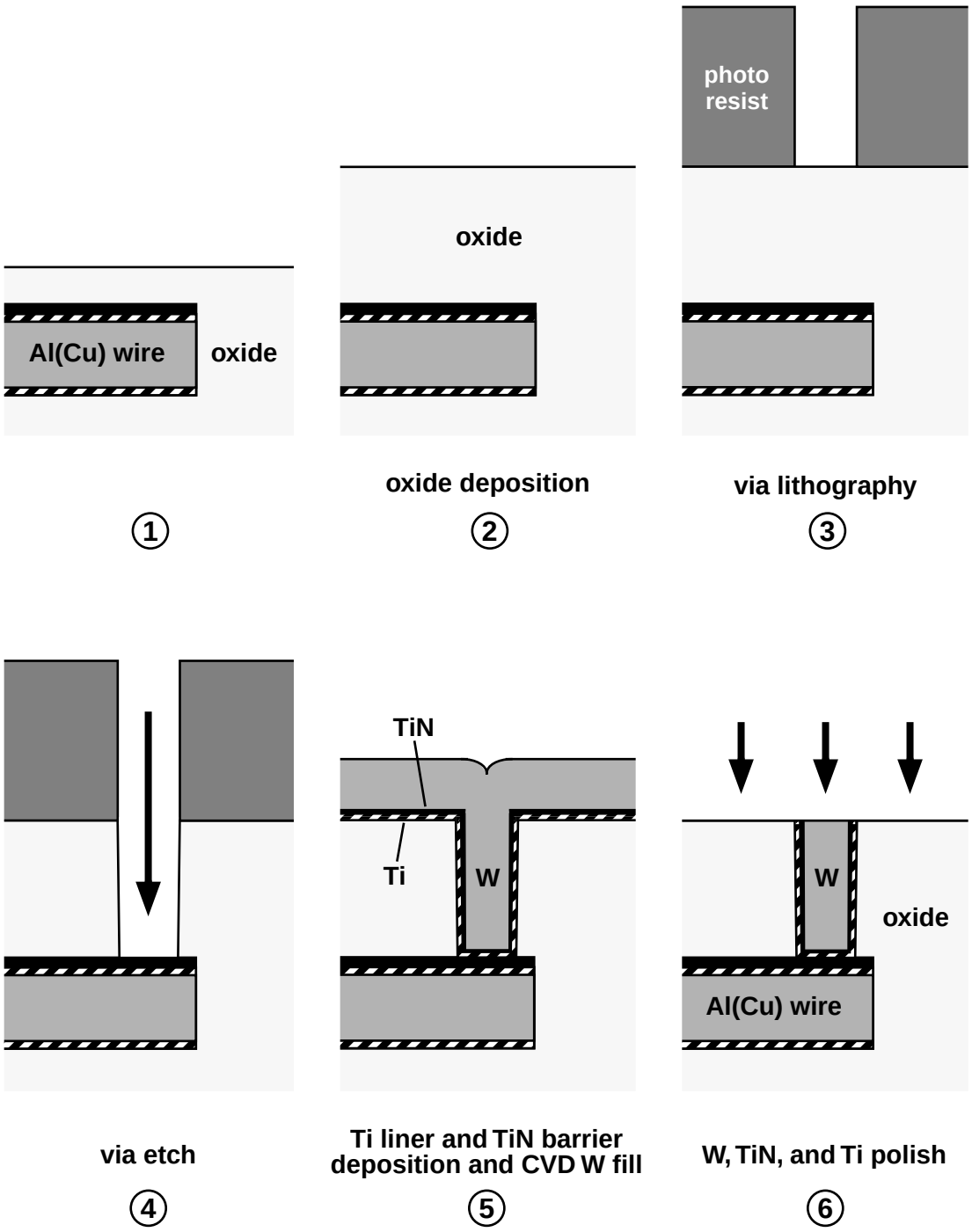


Figure 2-2 Process flow for fabrication of tungsten vias.

The chief drawback of tungsten via technology is cost. Furthermore, processing of tungsten, a brittle refractory metal, is notorious for introducing particles and defects on the wafer and compromising yield. Before CMP was employed, these problems were even more severe when the excess W was removed by etching. Cost alone continues to motivate the development of cheaper via technologies.

2.1.2 Fabrication of Aluminum Alloy Wires

The conventional process for forming Al alloy wires, also known as the *cloisonné* process, is summarized in Figure 2-3 [40]. After via or contact CMP, metal is sputtered over a planarized surface. The metal deposition typically consists of a sequence of Ti, Al(Cu), Ti, and TiN depositions without breaking vacuum. The Al layer is alloyed with 0.5% Cu which segregates to the Al grain boundaries for improved electromigration resistance [42]. This "Ti-over-and-under" wiring uses Ti as a base layer for good adhesion, low contact resistance to underlying vias, and a seed for (111)-textured Al(Cu) grains which have better electromigration resistance. The Al(Cu) layer is sandwiched by thin Ti layers because subsequent thermal treatment forms $TiAl_3$, a hard refractory intermetallic that further improves electromigration reliability as well as mechanical stability against stress-induced void and hillock formation. Finally, the reactively sputtered TiN film caps the metal stack to minimize the reflectivity of the stack and thus facilitate photolithographic control of fine features. The process flow continues with the metal lithography and etch. The vertical reactive ion etch (RIE) of the metal stack is becoming increasingly difficult for very aggressive line geometries. After the metal is patterned, the photoresist is removed and the metal spaces are subsequently filled by a conformal oxide deposition. Void-free dielectric gapfill remains an integration challenge, but can be achieved with high-density plasma (HDP) CVD oxide processes for 0.18-µm technologies. The residual oxide topography is removed with oxide CMP, leaving a planar oxide surface as the starting point for fabricating the next level of vias.

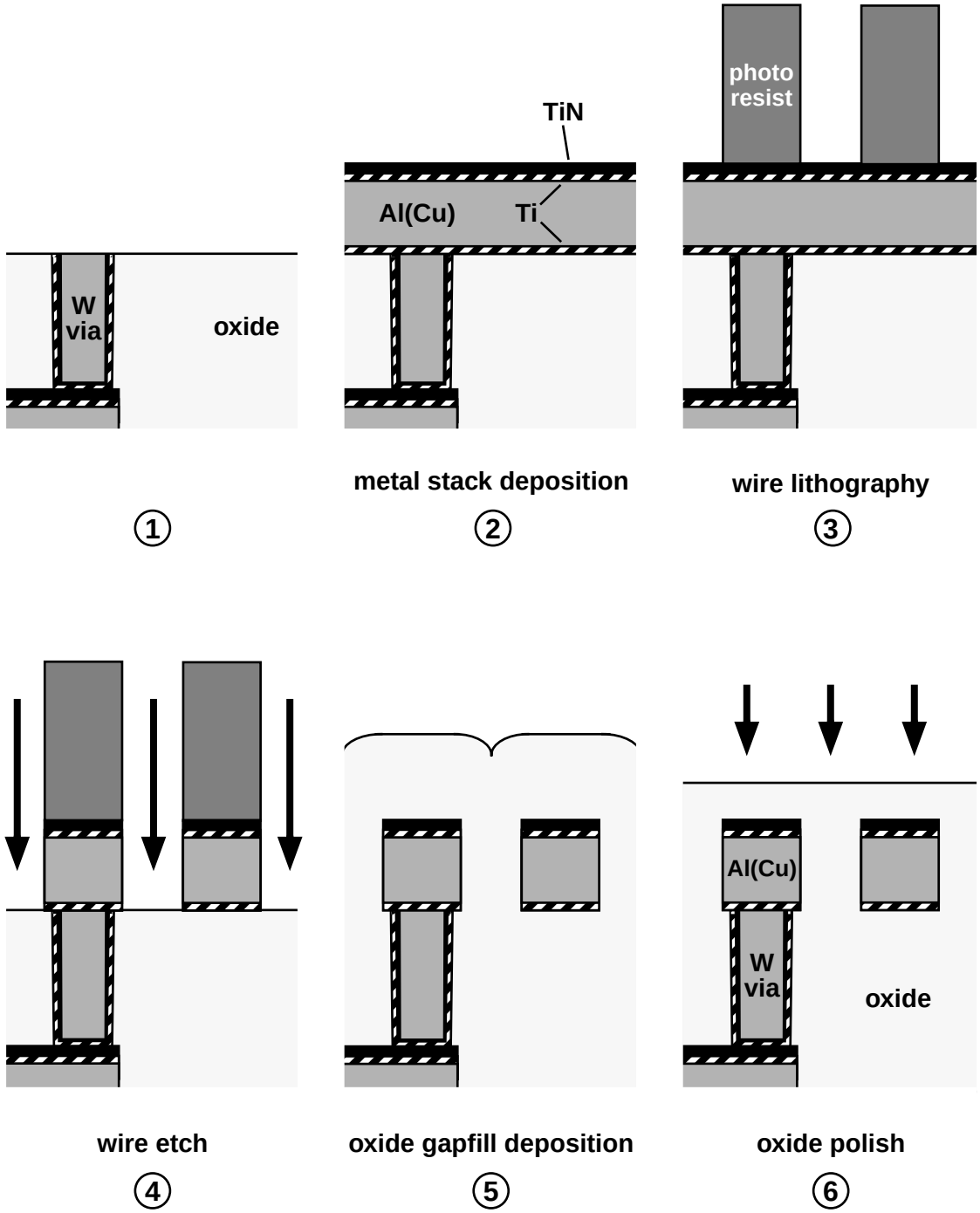


Figure 2-3 Process flow for fabrication of aluminum alloy wires.

The interconnects in high-performance logic IC's typically obey a hierarchical wiring scheme. As seen in Table 2-1, the metal pitch (sum of line width and spacing) and thickness become progressively larger for interconnects further away from the transistors. The lower layers of interconnection close to the transistors are designed for maximum wiring density. On the other hand, the uppermost layer(s) of thick interconnects (also called *fat* wires) are generally reserved for long connections as well as power and ground distribution.

Table 2-1: Interconnect Design Rules for 0.25-µm Technology [18]

Layer	Minimum Pitch	Thickness	Wire Aspect Ratio
metal 1	0.48 µm	0.48 µm	1.5 : 1
metal 2	0.93 µm	0.90 µm	1.9 : 1
metal 3	0.93 µm	0.90 µm	1.9 : 1
metal 4	1.60 µm	1.33 µm	1.7 : 1
metal 5	2.56 µm	1.90 µm	1.5 : 1

2.2 Dual-Damascene Copper Technology

The cross-section of a manufacturable copper interconnect technology is shown in Figure 2-4. In this example, W local interconnects and contacts are fabricated first using the Damascene process described in Section 2.1.1. Then, six levels of Cu wiring are integrated with Cu vias between successive metal layers. Oxide is both the via- and wire-level dielectric. As mentioned in Chapter 1, the main technical issues with Cu integration are Cu line patterning and potential device contamination.

Deep submicron copper interconnects cannot be formed using the conventional cloisonné approach that is ubiquitous in Al metallization. Cu halide compounds, e.g., chlorides and fluorides, that form during plasma etching are hardly volatile at low temperatures [43], rendering the etch prohibitively slow. Unfortunately, photoresist can-

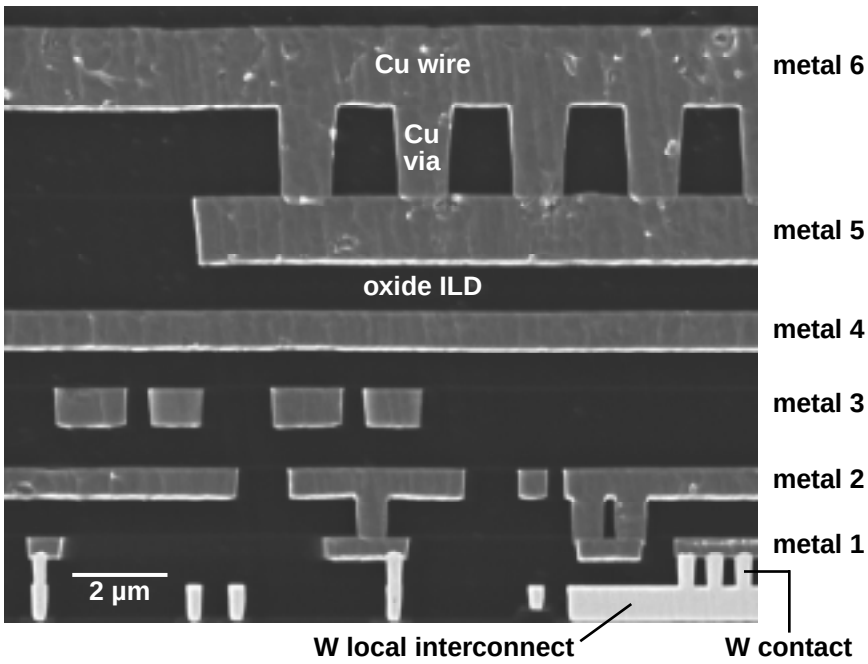


Figure 2-4 Scanning electron micrograph of manufacturable copper interconnect architecture demonstrated by IBM [27].

not withstand the temperatures required for practical Cu etch rates (> 200°C). Dielectrics such as polyimide, oxide, and nitride have been explored as alternative masking materials but they complicate the lithography process. Wet etching and lift-off approaches have also been attempted [44]. However, line width control of deep submicron features is essentially impossible with these techniques.

Cu is known to be a fast diffuser in silicon where it can act as a deep level acceptor in the silicon bandgap [45]. Deep level states degrade minority carrier lifetimes, causing high junction leakage in transistors and short retention times in DRAM's. Cu also diffuses through silicon dioxide, especially under electrical bias [46]. These facts have raised serious concerns about device contamination should Cu be introduced into the backend. Successful implementation of Cu interconnects must consequently prevent any trace amounts of Cu from migrating to the Si substrate. This will not only involve added process complexity but also influence wafer handling and tool designs.

The preceding obstacles are overcome by the dual-Damascene process with diffusion barriers surrounding the Cu interconnects [47]. Illustrated in Figure 2-5, dual-Damascene is a modified single-Damascene process where incorporating a second lithography step defines both wire trenches and via holes before they are backfilled with Cu. Hence, Cu wires and vias are formed with only one metal fill and one CMP step. Otherwise, two complete single-Damascene flows will be required: one for the vias and the second for the overlying wires. This process simplification results in reduced cost and improved manufacturability. The Cu interconnects are isolated from the surrounding oxide by metal barrier materials on the interconnect side and bottom interfaces, and by a dielectric barrier

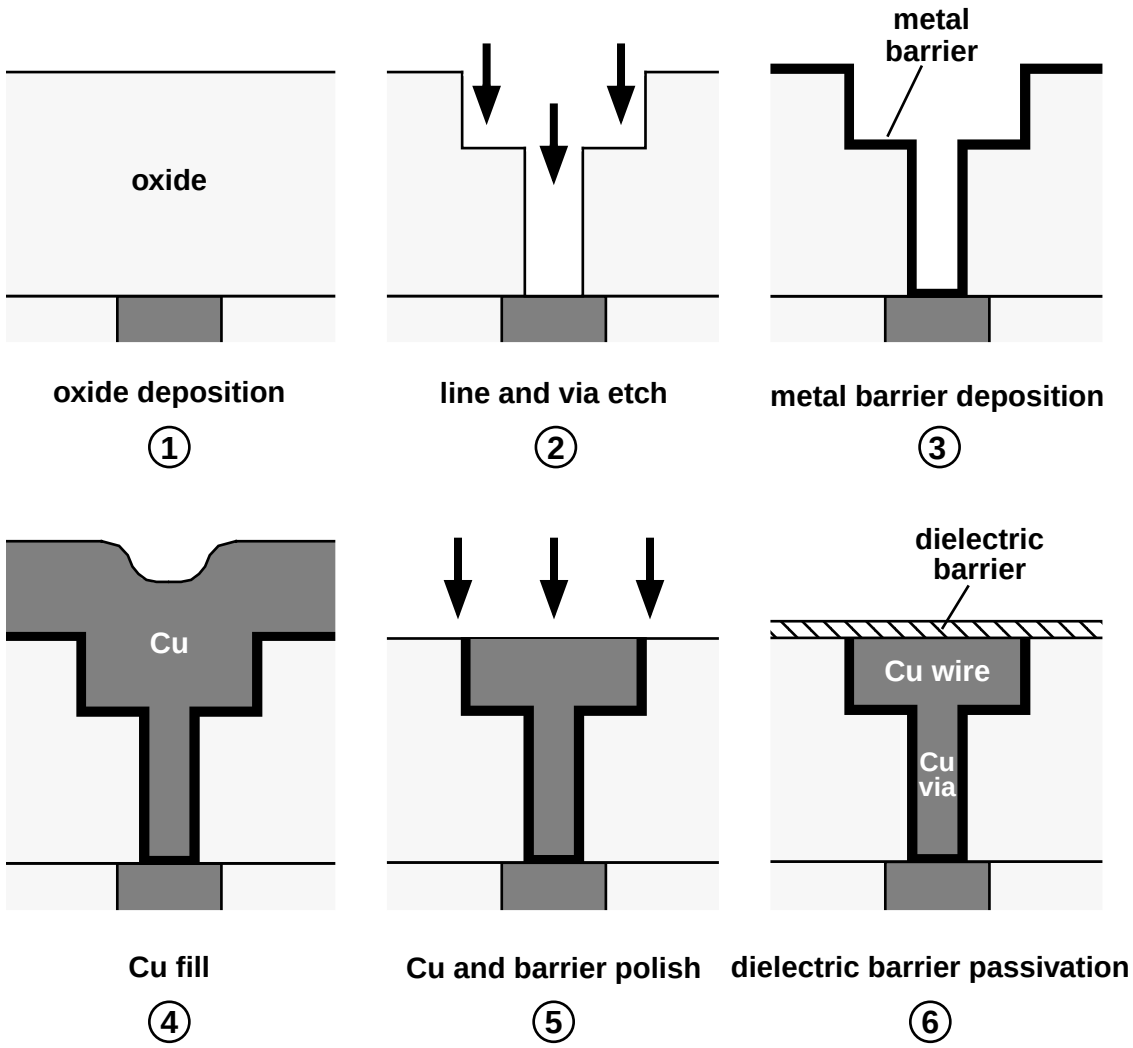


Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects.

above the interconnect. The individual steps in the dual-Damascene flow and the complex considerations in choosing barrier materials are elaborated in the subsections to follow.

2.2.1 Dielectric Etch

In a dual-Damascene flow, there are various methods of forming wire trenches and via holes to the underlying conductor [48]. Five approaches are summarized in Figure 2-6 [49]–[53]. Their merits and issues are listed in Table 2-2. The specific flow that is ultimately implemented in manufacturing will vary from company to company and depends on the process strengths in lithography and etch within a corporation.

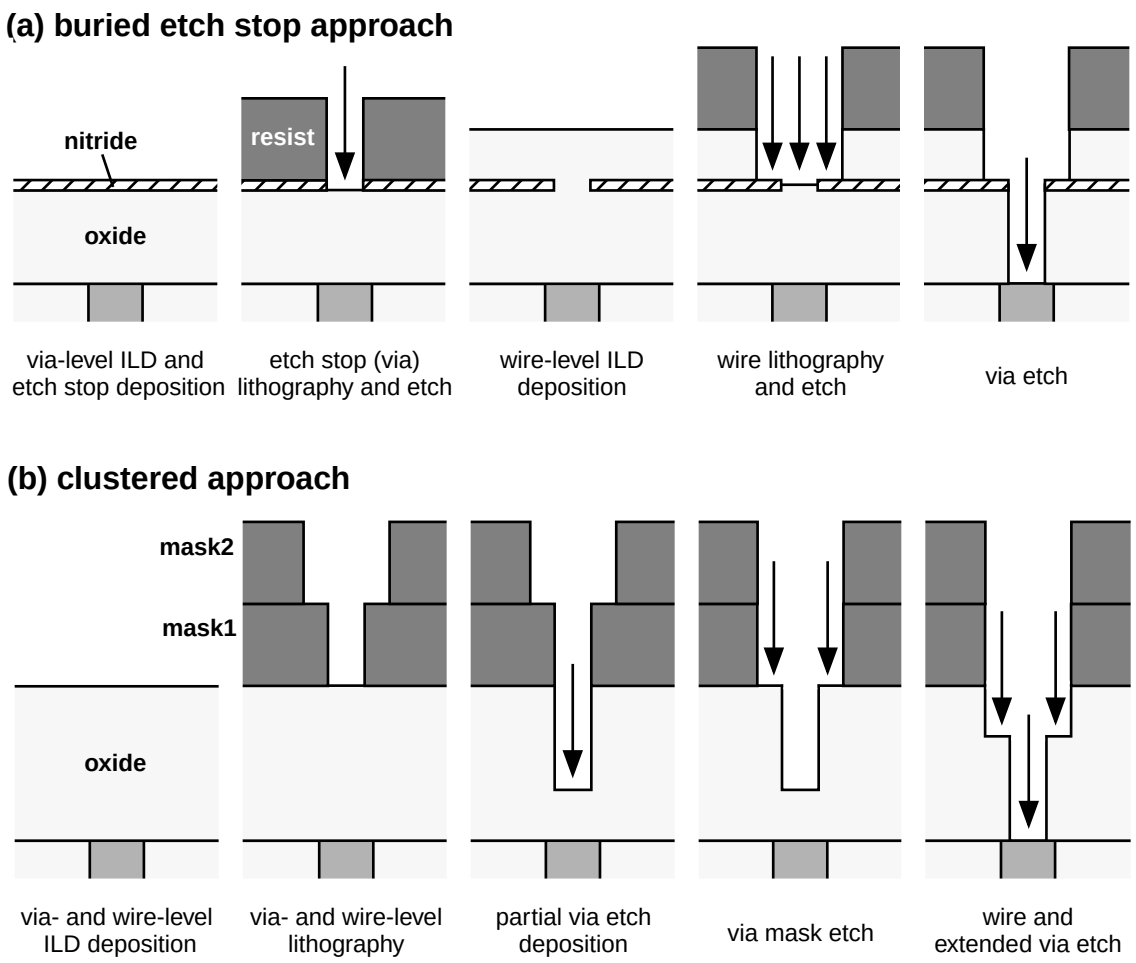


Figure 2-6 Dual-Damascene variations for defining wire trenches and via holes: (a) buried etch stop and (b) clustered approaches.

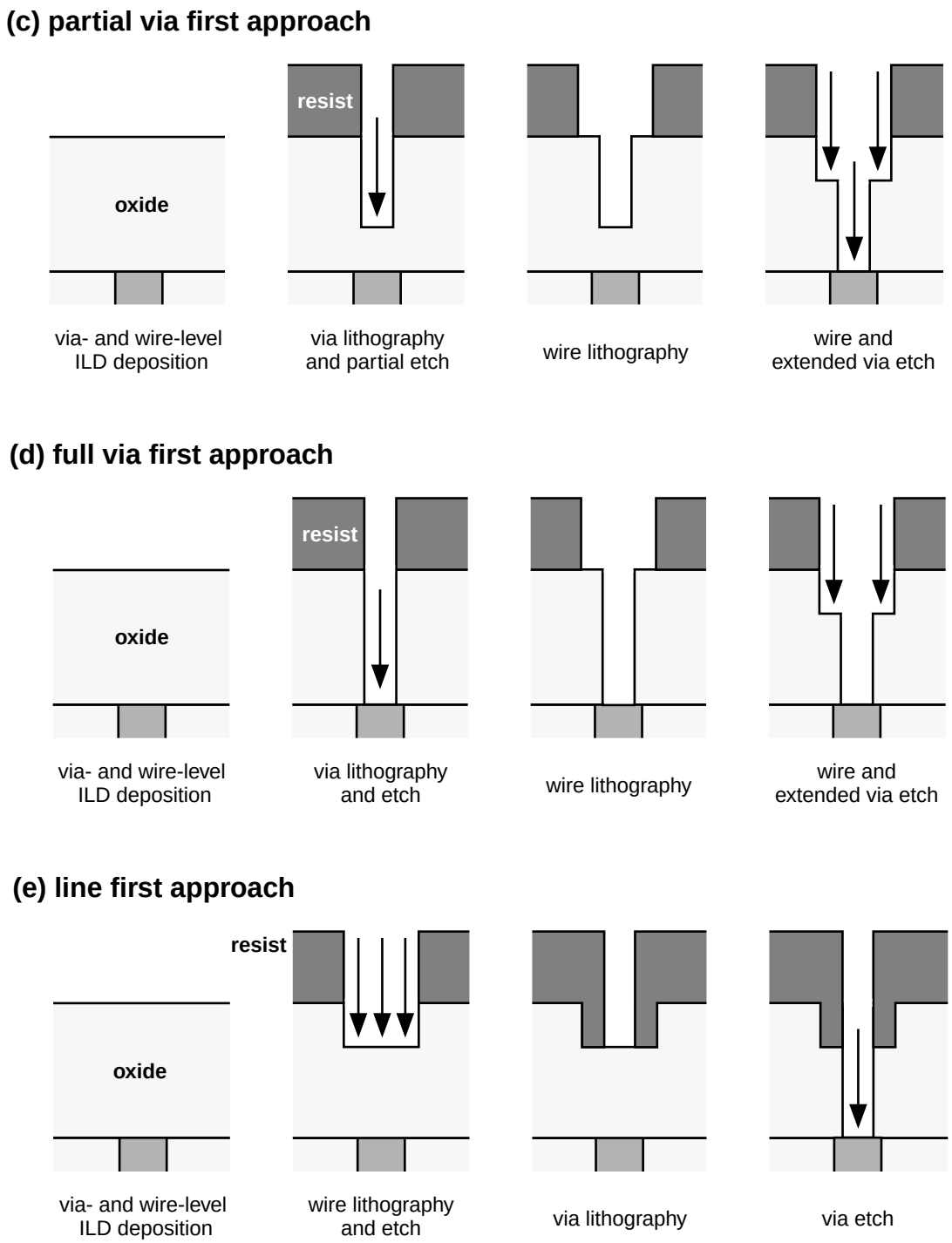


Figure 2-6 Dual-Damascene variations for defining wire trenches and via holes: (c) partial via first, (d) full via first, and (e) line first approaches.

Table 2-2: Comparison of Dual-Damascene Dielectric Etch Approaches [48]

Process Flow	Advantages	Disadvantages
buried etch stop [49]	topography minimized	etch process selectivity and control are critical
clustered [50]	process types grouped	resist adhesion, pattern transfer
partial via first [51]	cleaner structure, less critical etching	lithography process difficulty increased
full via first [52]	lithography and etch processes slightly easier; stacked via trivial	lithography rework and resist cleaning process difficult
line first [53]	easier etch process, less topography for lithography	resist cleaning process critical

2.2.2 Metal Barrier Deposition

Barrier encapsulation of Cu interconnects is required to ensure that even trace levels of Cu do not diffuse through the surrounding dielectrics into the Si substrate. As illustrated in Figure 2-5, both metal and dielectric barriers will be needed for dual-Damascene integration of Cu with oxide.

Following the dielectric etch, the wire trenches and via holes must be lined with a conductive barrier material to clad the side and bottom boundaries of the Cu interconnects. Since barrier materials are generally very resistive compared to Cu, barrier thickness must be kept to a minimum in order to preserve the effective conductivity advantage of Cu over Al alloys. Minimum barrier thicknesses in the 20–30 nm range are expected for 0.18-µm technologies [24]. Besides possessing superior barrier property, metal barriers should additionally exhibit low contact resistance to Cu. This requires an effective clean of the via holes following the dielectric etch. Since the via etch will expose underlying Cu wires, the clean must not redeposit any Cu onto the via hole sidewalls [54]. The barrier layers should also have low stress and good adhesion to oxide. In addition, barriers play an

important role in determining the microstructure of Cu films that are subsequently deposited. Similar to that of Al alloys, the electromigration reliability of Cu interconnects depends on Cu film texture [55]. The texture and roughness of the barrier layer are only two factors affecting the texture that develops in Cu films [56]. Finally, for integration feasibility, it is critical that metal barriers be deposited conformally into high aspect-ratio holes with low particle counts and be easy to planarize [57].

The above requirements have generated much interest to evaluate the barrier properties of refractory metals, primarily Ti, W, tantalum (Ta), and their nitrides [58]. With the wealth of experience gained from W via technology, the industry would ideally like to extend the use of Ti/TiN liners in Damascene Cu integration. However, it appears that TiN may be inadequate as a barrier against Cu diffusion. Ta and TaN have shown great promise. Amorphous materials are also being considered. Ternary films of TaSiN as thin as 5 nm have been shown to exhibit excellent barrier properties, presumably by removing fast Cu diffusion paths along the grain boundaries present in polycrystalline films [57]. These advanced barrier materials will draw more attention as barrier thickness scales with interconnect dimension.

There exists a strong concurrent effort to develop deposition technologies capable of providing conformal coverage of barrier materials in very high aspect-ratio holes. Conformal coverage of the dielectric openings is essential because failure is expected to occur where the barrier is thinnest, usually at the lower corners and sidewalls of a via. Conventional dc magnetron sputtering cannot meet the stringent conformality requirements because the large angular distribution of sputtered atomic flux will result in more deposition along the top corners of the trenches before there is adequate barrier coverage along the via bottom and sidewalls. This cusping will also increase the difficulty of the subsequent Cu fill. See Figure 2-7. Sputtering technology has thus been modified to improve vertical flux directionality. Long-throw, collimated, and ionized metal plasma (IMP) sputtering technologies provide better but not completely conformal step coverage. Inherently a conformal process, CVD also has been actively investigated but is an expensive technol-

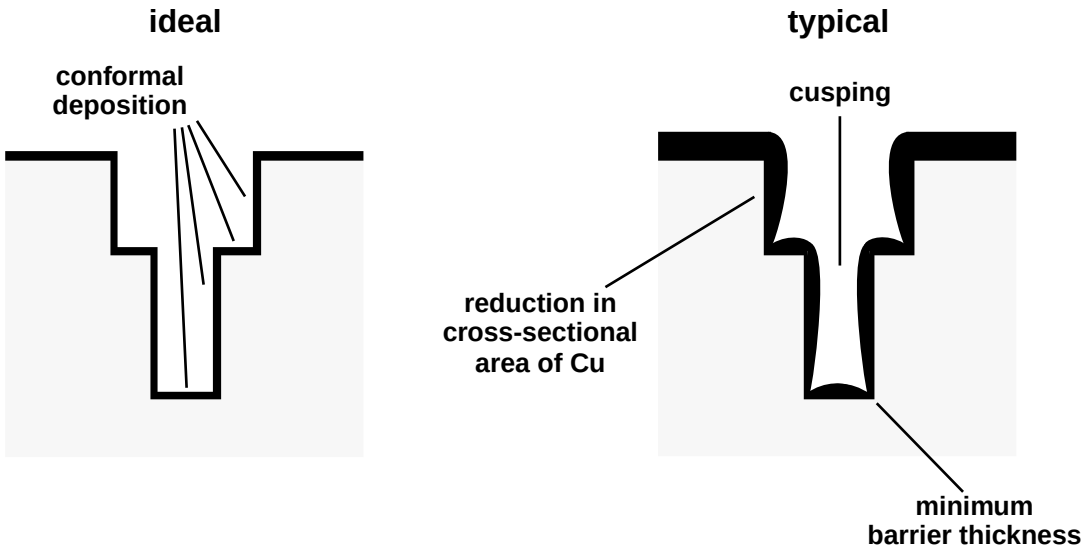


Figure 2-7 Comparison of ideal and typical step coverages of a metal barrier deposited by PVD [57].

ogy. The potential of CVD will depend on the extendability of cheaper sputtering technologies for more aggressive geometries [54].

The development of a metal barrier technology is key to successful integration of Cu with oxide. Although many implementation details remain undisclosed by companies involved, there is growing concensus in the industry to employ Ta liners and TaN barriers deposited by IMP sputtering.

2.2.3 Copper Deposition

After metal barrier deposition, the trenches and vias are filled with Cu. Many technologies have been explored to identify a cost-effective solution capable of high aspect-ratio and void-free Cu fill. Four are described in this discussion: PVD, CVD, electroless plating, and electroplating.

PVD techniques, even with improved flux directionality, are incapable of achieving void-free Cu fill. Revisiting Figure 2-7, the cusping that develops during sputtering will eventually pinch off the Cu film near the top of the trench and form a keyhole. However,

good trench filling has been demonstrated through reflow after sputtering [59]–[60]. First, the trench is partially filled by sputtering. In a subsequent *in situ* heat treatment, typically at 450°C for 30 minutes, the metal atoms redistribute from the field region into the trench, thereby completing the fill. The reflow process is thermodynamically driven by surface diffusion which minimizes the surface energy of the Cu film. It is very sensitive to the purity of the ambient gas during anneal, microstructural inhomogeneities in the Cu film, the wetability of the barrier underlayers, and the density of trench features. Moreover, the relatively high thermal budget incurred by the reflow anneal may unnecessarily impose stricter barrier requirements. The limited process latitude renders sputter reflow inadequate for manufacturing.

Due to its superior step coverage over PVD, CVD has naturally received much attention. CVD Cu films are deposited by thermal decomposition of organometallic (OMCVD) precursors at 150 to 200°C [61]. The most extensively investigated precursor is Cu(hfac)(tmvs), abbreviated for copper (I) hexafluoroacetylacetonate trimethylvinylsilane. Although excellent trench fill in aggressive geometries have been demonstrated, the main bottleneck preventing widespread use of CVD Cu is cost. The price of the Cu precursor will remain prohibitively high until cheaper alternative fill technologies can no longer accommodate the fill requirements as interconnects continue to scale.

Electroless plating, a cheap and simple means of selectively depositing thin Cu films, was also considered [62]. Wafers are immersed in a heated bath of aqueous Cu ions. Cu atoms are then supplied to the wafer surface by catalytic reduction of the Cu ions, but only at exposed conductive surfaces of the wafer. Electroless plating was a serious contender during the early stages of Cu process development. Unfortunately, its primary drawback is lack of process control during deposition. Deposition will proceed spontaneously and depend primarily on the plating solution chemistry and the seed layer. Moreover, the microstructure of electroless Cu films generally consists of very fine grains, implying poor electromigration reliability. For these reasons, electroless Cu is not considered feasible for production.

Recently, electroplating has emerged as the most promising and cost-effective Cu deposition technology [63], having already been demonstrated for manufacturability [27]. In electrochemical deposition of copper, the wafer is coated with a thin seed layer of Cu, typically by sputtering, and immersed in a solution containing Cu^{2+} ions. Although the wafer will have already been lined with a conductive barrier and a thin Cu seed layer, the Cu seed layer is needed because electroplating may not occur on some barriers. Electrical contact is made to the seed layer which serves as the cathode. An electrical current is supplied to the cathode to reduce Cu ions at the wafer, thereby depositing atomic Cu on the Cu seed. As Cu ions are plated out of the solution onto the wafer, the Cu anode simultaneously undergoes oxidation to replenish the supply of Cu ions in the solution. See Figure 2-8.

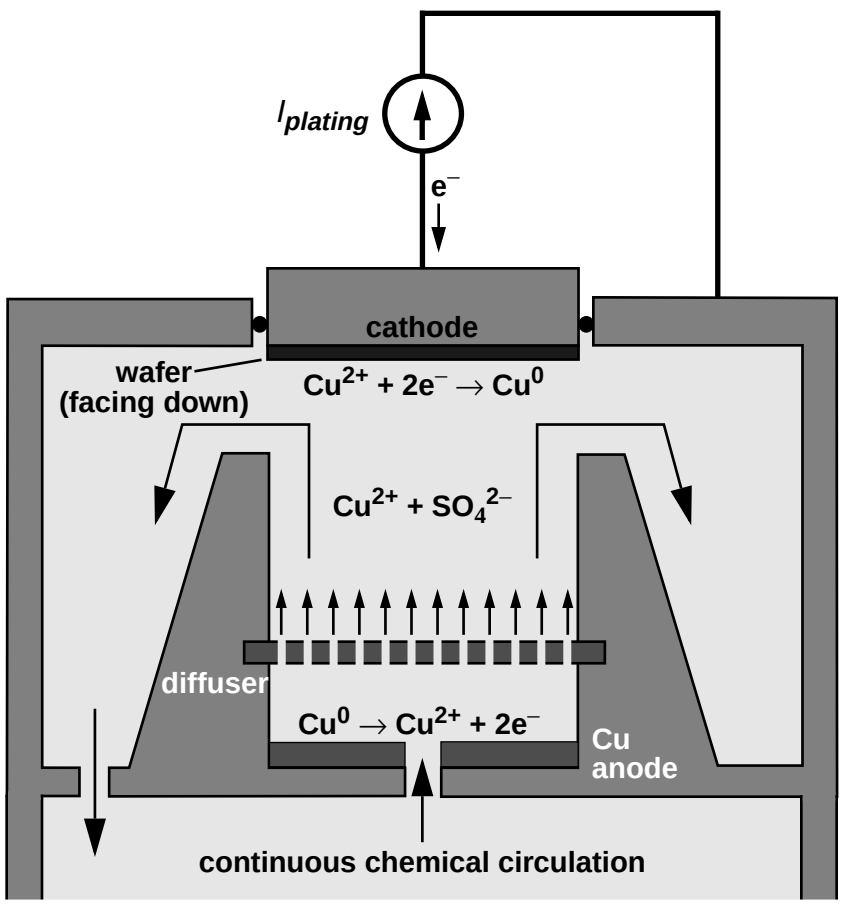


Figure 2-8 Schematic of a Cu electroplating system.

In principle a relatively simple technology, Cu electroplating in practice is fairly complex. A manufacturable process must demonstrate good fill capability, step coverage, film morphology, across-wafer and wafer-to-wafer uniformities, and practical deposition rates. To achieve void-free fill, the contents of the electroplating solution and the way in which the electrical current is applied must be optimized. Otherwise, keyholes may form in the trench since the plating rate is higher at the trench shoulders, where the current density is highest, than at the trench bottom. The plating bath primarily consists of aqueous copper sulfate ($CuSO_4$) and sulfuric acid (H_2SO_4) but also contains trace quantities of organic additives (e.g., thiourea, disulfides, and polyamines). These additives improve the quality of the deposited Cu film by, for example, enhancing deposition at the bottom of trenches, serving as wetting agents for good film nucleation, and relieving deposited film stress [64]. The trench and via filling capability of electroplating is also improved by modulating the magnitude and direction of the electrical current. Reversing the polarity of the applied current causes oxidation or etching of Cu to occur at the wafer surface. Since the etching rate is also a direct function of current density, a deposition/etch sequence is employed to remove copper from the trench shoulder more quickly than from the trench bottom during the etch cycle, resulting in more conformal coverage.

With both *pulsed* plating waveform and bath chemistry optimized, high aspect-ratio trenches and vias can be successfully filled [65]. Given the appropriate barrier and Cu seed layers and microstructures, plated Cu films with large grain sizes and a near-bamboo microstructure can be obtained. These factors are believed to be responsible for the good electromigration resistance of plated Cu [66].

2.2.4 Chemical-Mechanical Polishing

After the trenches and vias are filled with Cu, the excess Cu in the field region is removed by chemical-mechanical polishing (CMP). Pioneered by IBM, CMP is unquestionably the key enabling technology in Damascene integration [67]. Figure 2-9 illustrates a typical CMP system. Both chemical reactivity and mechanical abrasion play important roles in the selective removal of a film from the wafer surface. Chemicals in the slurry

react with the film surface, typically forming a thin oxidized layer. This layer is subsequently removed by mechanical abrasion due to fine particles in the slurry under the pressure of the polishing pad. The wafer surface becomes progresssively planar with polishing time since the removal or polishing rate increases with local pad pressure.

In metal CMP, a good balance must exist between chemical and mechanical components to achieve optimum planarization. If the mechanical component is too dominant, surface scratches and nonuniform polishing may result. On the other hand, if the chemical component is too dominant, overpolishing can result in severe surface topography due to the selectivity of the slurry chemistry against dielectric removal. Mechanical abrasion depends on the size and concentration of slurry particles, hardness and surface roughness of the pad, pad pressure, and the rotational speeds of the pad and wafer. The chemical component is controlled by the chemistry, concentration, and pH of the slurry. The CMP process must also minimize pattern density and feature size effects in order to avoid dielectric erosion and metal dishing.

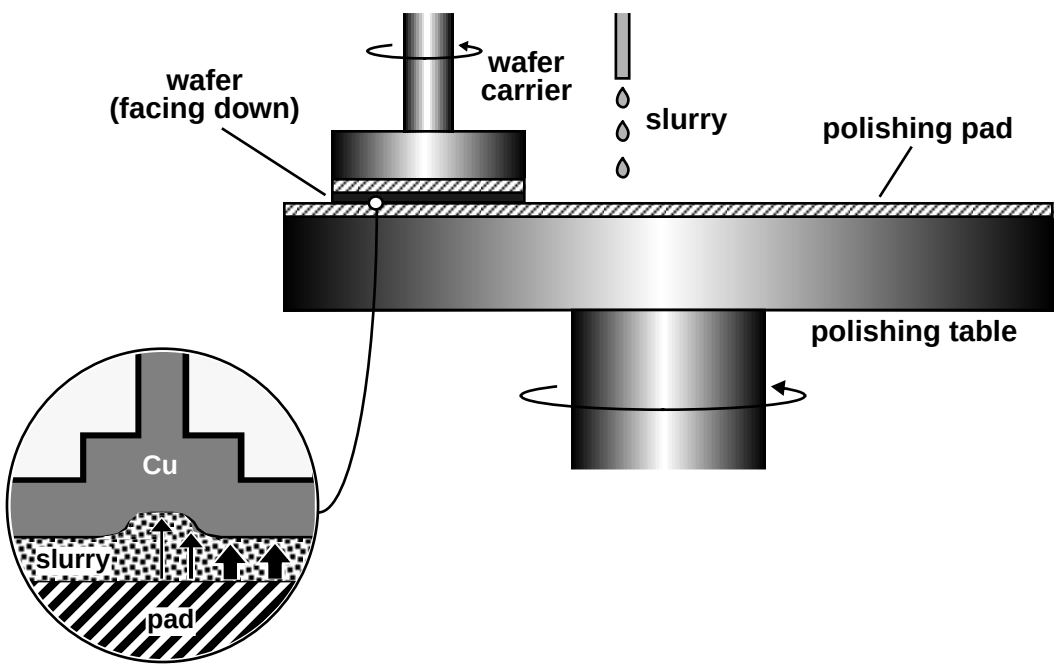


Figure 2-9 Schematic of a typical chemical-mechanical polishing system.

Compared to W CMP, there are several additional challenges unique to Cu CMP [63]. Unlike W, Cu is a relatively soft metal which is easily corroded and is prone to scratches and embedded particles. In addition, Cu CMP is complicated by the underlying conductive barrier layers which must also be removed. Like any CMP process, the post-CMP clean is critical in removing traces of slurry from the polished surface. However, since Cu CMP is inherently a wet process that will liberate Cu^{2+} by-products, the post-CMP clean has the additional burden of removing these ions from the wafer surface in order to minimize the potential of device contamination.

The development of a manufacturable Cu CMP process is arguably the most challenging aspect of Cu integration. Cu CMP process recipes will largely remain proprietary for the few years to come while they provide successful companies with a competitive technology edge.

2.2.5 Dielectric Barrier Passivation

Following Cu CMP, the Cu interconnects must be capped by a dielectric barrier such as PECVD silicon nitride. The nitride is typically deposited at 350–400°C using SiH_4 and NH_3 precursors. Since copper readily oxidizes at these temperatures, certain procedures must be followed to protect the exposed Cu surfaces. For example, in cluster tools, a wafer is loaded into the nitride deposition chamber after being evacuated in the common buffer chamber. The nitride passivation completes the fabrication of one level of Cu wires and vias.

2.3 Summary

This chapter reviewed the process integration of conventional Al and dual-Damascene Cu interconnects. First, Al metallization technology was described with an outline of Al alloy wire and W via fabrication. Next, the dual-Damascene Cu technology was presented. Key technical issues in the various aspects of both integration schemes were highlighted as they pertain to manufacturing. This background information establishes the

context for understanding Damascene Cu integration with low-κ dielectrics. Low-κ polymer materials are the subject of the following chapter.

Chapter 3 Low-Permittivity Dielectrics

Interlevel dielectrics (ILD's) currently incorporated in IC manufacturing are deposited oxides with dielectric constants (κ's) ranging from 4.0 to 4.5. As explained in Chapter 1, substituting the oxide ILD's with lower κ materials improves the performance of interconnects through reduction of parasitic capacitance. Capacitance reduction mitigates crosstalk noise, dynamic power dissipation, and interconnect propagation delay issues as interconnects continue to scale.

This chapter focusses on the chemistry and materials aspects of low-permittivity (low-κ) dielectrics, starting with a brief discussion of the physical properties that make a dielectric low-κ. A survey of materials that are developed as prospective future ILD materials is then presented. Emphasis is placed on the six low-κ polymer dielectrics that are studied in this dissertation.

3.1 Strategies for Dielectric Constant Reduction

The dielectric constant, κ, is a physical measure of the electric polarizability of a material [68]. Electric polarizability is the tendency of a material to allow an externally applied electric field to induce electric dipoles (separated positive and negative charges) in the material. Shown in Eq. (3-1), κ can be expressed as

$$\kappa = \frac{\varepsilon}{\varepsilon_0} = \frac{\varepsilon_0(1+\chi_e)}{\varepsilon_0} = 1 + \chi_e \tag{3-1}$$

where ε and ε_0 are the permittivities of the dielectric and free space respectively, and χ_e is the electric susceptibility of the dielectric. χ_e is the unitless constant of proportionality relating the induced dipole moment per unit volume of dielectric, $\vec{P}$, to the applied electric field, $\vec{E}$.

$$\vec{P} = \varepsilon_0 \chi_e \vec{E} \tag{3-2}$$

In a perfect vacuum, there are are no atoms to polarize, making $\chi_e = 0$ and $\kappa = 1$. In solid-state matter, there are three polarization mechanisms: electronic, atomic, and dipolar [69]. Electronic polarization occurs in neutral atoms when an electric field displaces the nucleus with respect to the electrons that surround it. Atomic polarization occurs when adjacent positive and negative ions stretch under an applied electric field. Dipolar or orientational polarization occurs when permanent dipoles in asymmetric molecules respond to the applied electric field. Each polarization mechanism has an associated response time and therefore will not contribute to κ beyond some corresponding frequency. Figure 3-1 illustrates a typical κ dependence on the frequency of the applied field. All three mechanisms respond to GHz or lower frequencies where IC's operate.

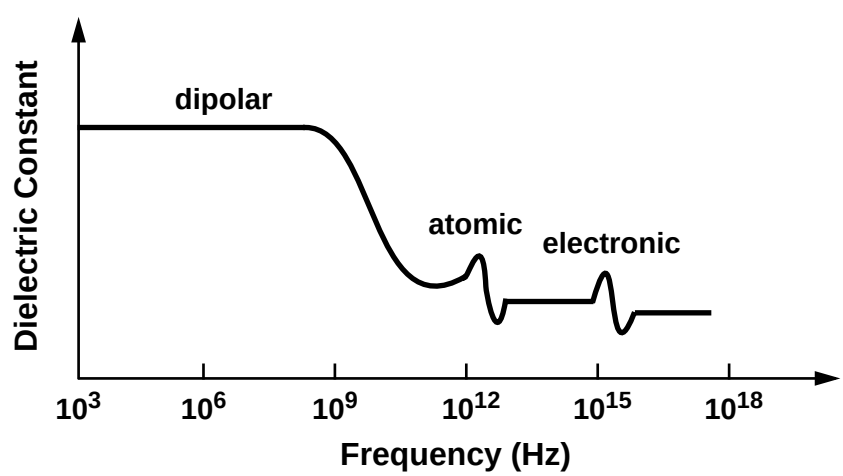


Figure 3-1 Frequency response of dielectric mechanisms [69].

A low-κ dielectric is an insulating material that exhibits weak polarization when subjected to an externally applied electric field. There are many guidelines employed to design low-κ materials. A few practical approaches are briefly mentioned. The most obvious one is to choose a nonpolar dielectric system. For example, polarity is weak in materials with few polar chemical groups and with symmetry to cancel the dipoles of chemical bonds between dissimilar atoms. Since $\kappa_{air} \approx 1$, dielectrics can also have lower effective κ's with the incorporation of some porosity into the chemical structure. Another approach is to minimize the moisture content in the dielectric or alternatively design a dielectric with minimum hydrophilicity. Since $\kappa_{water} \approx 80$, a low-κ dielectric needs to absorb only very small traces of water before losing its permittivity advantage.

3.2 Survey of Available Materials

Strictly speaking, air has the lowest κ, exhibiting more than 75% permittivity improvement over conventional oxide ILD's. Unfortunately, many reliability concerns exist with the implementation of air as the ILD, the obvious one being the structural integrity of the interconnects. Some of these issues can be mitigated by deliberately integrating air voids, for example, using an unconformal oxide deposition during gapfill [70]. However, the manufacturability of these approaches remain to be demonstrated. For a low-κ

Table 3-1: Property Requirements of Low-κ Dielectrics

Electrical	Chemical	Mechanical	Thermal
Dielectric constant Anisotropy Low dissipation Low leakage current Low charge trapping High electric-field strength High reliability	Chemical resistance Etch selectivity Low moisture uptake Low solubility in H_2O Low gas permeability High purity No metal corrosion Long storage life Enviromentally safe	Thickness uniformity Good adhesion Low stress High hardness Low shrinkage Crack resistance High tensile modulus	High thermal stability Low coefficient of thermal expansion Low thermal shrinkage Low thermal weight loss High thermal conductivity

dielectric to be considered suitable for backend integration, it must satisfy a multitude of electrical, chemical, mechanical, and thermal requirements summarized in Table 3-1. These requirements invariably introduce compromises which must be carefully considered in order to engineer feasible low-κ materials for the ILD application.

The families of dielectric materials currently available for ILD integration are listed in Table 3-2. These dielectrics are deposited on the wafer either by CVD or by spin-on deposition. CVD offers the advantages of being a dry process, capable of producing films with excellent uniformity and conformality [71]. However, CVD is generally restricted to dielectrics with relatively simple chemistries. A larger variety of materials can be deposited by spin-on deposition [72], much like photoresist. Dissolved in a solvent, spin-on low-κ precursors are first dispensed onto the wafer in liquid form. The coating is subsequently cured to expel the solvent and induce polymerization and crosslinking of the precursors in order to form a solvent-resistant dielectric with desirable electrical, mechanical, chemical, and thermal properties.

Fluorinated oxide shares many integration similarities as undoped plasma oxides and is extensively developed as the next generation ILD with $\kappa = 3.5$ [21]. Fluorinating a

Table 3-2: Families of Candidate Low-κ Dielectrics for Advanced Interconnects

Dielectric Materials	κ	Deposition Method
undoped plasma SiO_2	4.0–4.5	CVD
fluorinated SiO_2	3.5	CVD
spin-on glasses (silsesquioxanes)	2.2–3.0	spin-on
organic polymers (e.g., polyimides, parylenes, aromatic ethers)	2.0–3.9	spin-on / CVD
fluorinated amorphous carbon (α-C:F)	2.1–2.3	CVD
nanoporous dielectrics (e.g., xerogels)	1.2–2.2	spin-on

dielectric is a common means of reducing κ provided that the fluorine atoms are incorporated correctly. Fluorine is the most electronegative atom and forms chemical bonds that are not easily perturbed by external electric fields and hence not readily polarizable. However, since fluorine is also highly reactive, excessive fluorination raises concerns of metal and dielectric corrosion. Even though κ as low as 3.2 can be attained, excessive fluorination of oxide additionally introduces moisture uptake and thermal stability issues.

Below κ of 3.5, spin-on glasses (SOG's) have been actively investigated and are already used in production [35]. Before CMP was introduced in manufacturing, SOG's were considered primarily because of their ability to planarize the topography of Al lines and spaces for multilevel integration. Common SOG's are hydrogen silsesquioxane (HSQ) and methyl silsesquioxane (MSQ). Silsesquioxanes or siloxane-based dielectrics are caged silica structures, shown in Figure 3-2, which enclose empty pores for low κ. They are thermodynamically unstable and upon heating at 450°C or beyond, will transform into more densified amorphous SiO_2, thereby losing its permittivity advantage [72].

Organic polymers have also received significant consideration as ILD materials. Polyimides were first considered because they possess good mechanical strength, thermal stability, and chemical resistance [73] as well as have an established usage in printed cir-

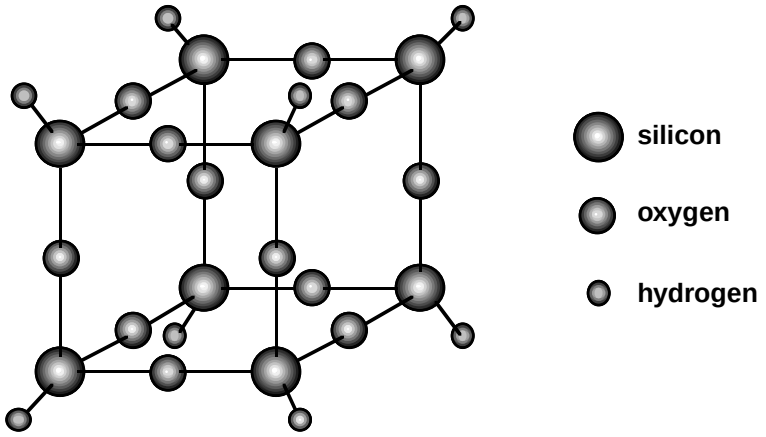


Figure 3-2 Structural formula of a hydrogen silsesquioxane spin-on glass.

cuit board manufacturing. However, with κ values typically exceeding 3.0, polyimides cannot meet future ILD requirements. Moreover, polyimides readily absorb ambient moisture and exhibit significant anisotropy in the dielectric constant. The polyimide system can be modified to mitigate these limitations, but the improvements are only incremental. These shortcomings have stimulated the chemical industry to develop completely different families of low-κ polymer dielectrics specifically tailored for ILD integration. Some of the spin-on varieties include polyarylene ethers, derivatives of cyclobutane, polynorbornenes, amorphous Teflon™, and phase-separated inorganic-organic hybrids. CVD alternatives include parylene-N, parylene-F, polynaphthalene, and polytetrafluoroethylene (Teflon™). Some of these materials will be further discussed in Section 3.3.

Other dielectrics receiving recent attention include diamond-like carbon [74] and fluorinated amorphous carbon [75]. These materials are attractive primarily because they are deposited by CVD using existing tools. Diamond-like carbon exhibits thermal stability and adhesion issues although it has been successfully incorporated in a single-Damascene demonstration [74]. κ can be reduced to as low as 2.1 by introducing fluorine although fluorination further degrades thermal stability and adhesion.

Nanoporous dielectrics are among the few materials options with ultralow κ (< 2.0). They include xerogels, aerogels, and organic nanofoams [76]. To date, the most active integration effort is with xerogel, a spin-on porous silica matrix. Unlike the previously described families of low-κ dielectrics, κ of xerogel is tunable depending on the degree of porosity that is incorporated during processing. Process integration of porous materials is very challenging because these dielectrics are mechanically weak and have large internal surface areas which can absorb moisture. The pores also degrade dielectric breakdown strength as well as increase the difficulty of depositing continuous films on these dielectric surfaces. Nevertheless, Damascene Cu integration with oxide-encapsulated xerogel has been demonstrated [33]. The potentially significant capacitance advantage of xerogel remains to be shown.

3.3 Investigated Dielectrics

Six low-κ organic polymer dielectrics were studied in this dissertation. As listed in Table 3-3, they consist of five spin-on polymers and one CVD polymer. The chemistries of these materials share some similarities which are incorporated to meet the ILD integration requirements. In designing carbon-based low-κ materials, the most challenging requirement to meet is thermal stability. At temperatures of 400–450°C and beyond, the polymer network begins to disintegrate as there is sufficient thermal energy to break chemical bonds. Thermal stability is improved in polymers which are highly crosslinked and have rigid backbones, aromatic structures, and highly polar groups. Crosslinking additionally increases mechanical strength and solvent resistance. However, aromaticity and polarity increase both κ and water absorption.

Table 3-3: Investigated Low-κ Dielectrics

Low-κ Polymer Family	Specific Variety	κ
polyarylene ether	Schumacher PAE-2 [77]	2.8
	Asahi Chemical ALCAP-E [78]	2.8
aromatic hydrocarbon	Dow Chemical SiLK™ polymer [79]	2.7
fluorinated polyimide	DuPont FPI-136M [82]	2.6
benzocyclobutene	Dow Chemical Cyclotene™ 5021 BCB [83]	2.6
parylene-F	Novellus Systems AF-4 [85]	2.4

3.3.1 Polyarylene Ether

Polyarylene ethers consist of aromatic groups (Ar) connected by ether oxygen linkages in a linear fashion. Compared to other functional groups (e.g., carboxylic acids, aldehydes, esters, and ketones), ether linkages provide strong C–O bonds for improved thermal stability while introducing relatively weak polarity for low κ. Two varieties of polyarylene ether were studied: Schumacher PAE-2 [77] (also known as Lo-κ™ 2000) and Asahi Chemical ALCAP-E [78]. Both materials have very isotropic κ's of 2.8. See

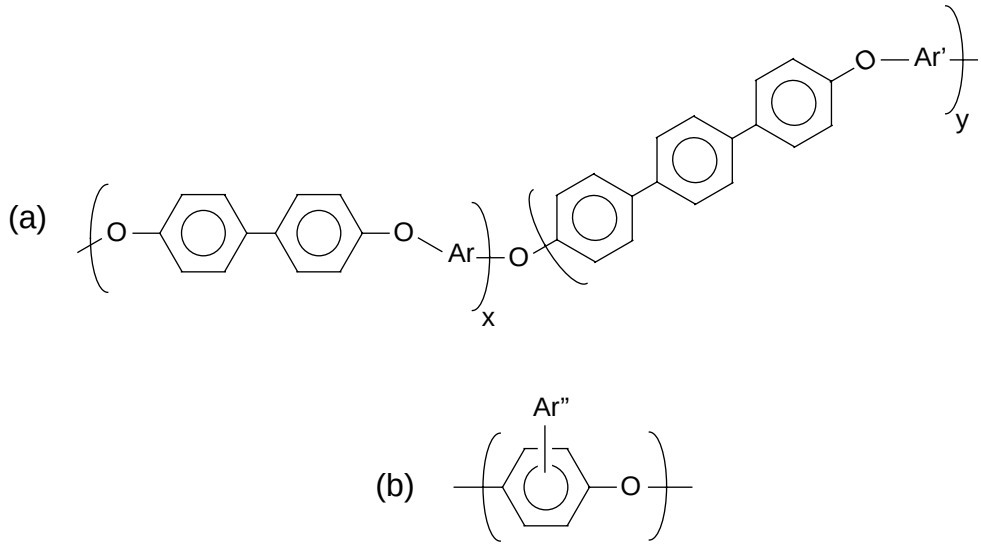
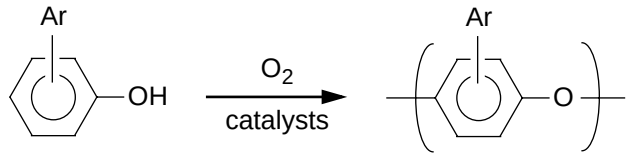


Figure 3-3 Structural formula of two polyarylene ethers: (a) Schumacher PAE-2 [76] and (b) Asahi Chemical ALCAP-E [78]. Ar, Ar', and Ar'' are proprietary aromatic groups.

Figure 3-3. Polyarylene ethers are essentially fully polymerized when spin-coated and can be synthesized by a few approaches. One example is oxidative coupling of phenols, which is employed to synthesize ALCAP-E.



(3-3)

Polyarylene ethers possess many desirable properties for ILD integration but require extensive crosslinking for good thermal stability and solvent resistance. Curing the polymer in oxygen improves crosslinking, but high-temperature exposure to oxygen may not be suitable for Cu integration. Fluorinated polyarylene ether, which exhibit lower κ (κ = 2.5–2.6) than nonfluorinated counterparts, has also been synthesized. However, the instability of fluorine in this polymer has resulted in severe metal corrosion, thus rendering integration to be unfeasible.

3.3.2 Aromatic Hydrocarbon

SiLK™ polymer, an aromatic hydrocarbon capable of withstanding temperatures in excess of 500°C, was recently developed by Dow Chemical [79]. Since the chemistry of this polymer is yet to be disclosed, SiLK™ polymer will be generically classified as an aromatic hydrocarbon. This material is an isotropic thermoset resin that becomes highly crosslinked in all dimensions upon curing. Although integration of SiLK™ polymer is very sensitive to processing conditions (e.g., cannot withstand exposure to oxygen at high temperatures) [80], the material is under strong consideration by many companies.

3.3.3 Fluorinated Polyimide

Although conventional polyimides do not meet the κ requirements of future ILD's, fluorinated polyimides are potentially suitable candidates [81], [82]. The specific example that was studied is a copolymer called DuPont FPI-136M (Figure 3-4).

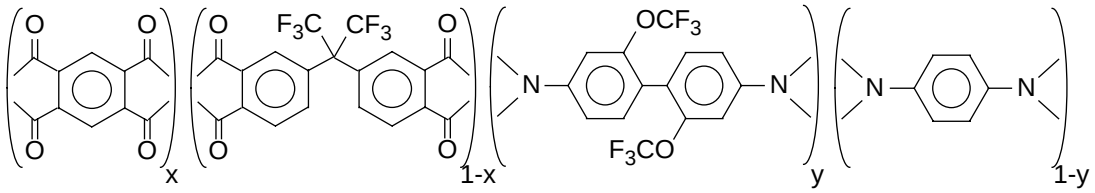
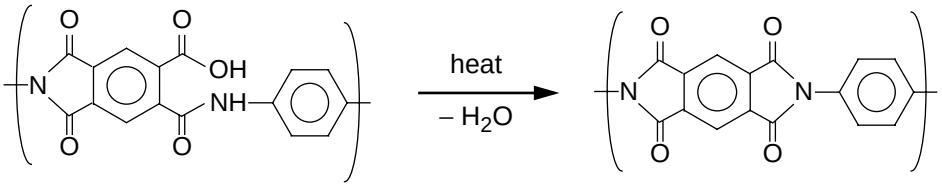


Figure 3-4 Structural formula of DuPont FPI-136M fluorinated polyimide [82].

Fluorinated polyimide exhibits lower κ, lower moisture uptake, and better isotropy than conventional counterparts. Like other linear polyimides, FPI-136M is formed by cyclization of polyamic acid precursors in the curing step after spin-on deposition. A simplified cyclization reaction is illustrated below.



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3.3.4 Benzocyclobutene

Divinylsiloxane-benzocyclobutane (DVS-BCB), commonly known as benzocyclobutene (BCB), is a thermoset resin derivative of cyclobutane deliberately designed to crosslink when heated [83]. The BCB monomer is shown in Figure 3-5.

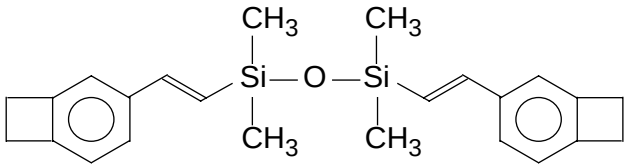
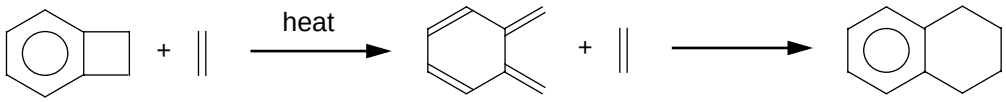


Figure 3-5 Structural formula of Dow Chemical Cyclotene™ 5021 benzocyclobutene (BCB) monomer [83].

Polymerization occurs during the cure step following spin-on deposition. The BCB monomer undergoes a ring opening reaction to give a diene that will react with a C=C to finally give a cyclohexane ring fused to a benzene. Since the BCB monomer has four active sites (two C=C and two cyclobutane rings) for this reaction to occur, the monomer will crosslink into a three-dimensional network, resulting in an isotropic κ of 2.7.



(3-5)

The crosslinking of BCB does not liberate any by-products although the cure must be performed in a non-oxidizing ambient. Otherwise, the polymer will degrade as carbonyl groups (C=O) form. BCB possesses other attractive qualities, such as hydrophobicity, that makes it an attractive and processable low-κ ILD. In fact, Damascene Cu integration with BCB has been demonstrated [84]. Unfortunately, the main drawback of BCB is its limited thermal stability. BCB is stable up to only 350°C and is consequently incompatible with many existing backend processes.

A similar derivative of cyclobutane, also developed by Dow Chemical, is perfluorocyclobutane (PFCB) with $\kappa = 2.4$. However, similar to other dielectrics having fluorine content, the adhesion of PFCB to common backend films is poor.

3.3.5 Parylene-F

Poly(tetrafluoro-*p*-xylylene) or parylene-F is a vapor-deposited crystalline polymer with κ of 2.3–2.4 [85]. See Figure 3-6.

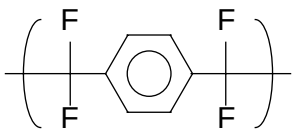
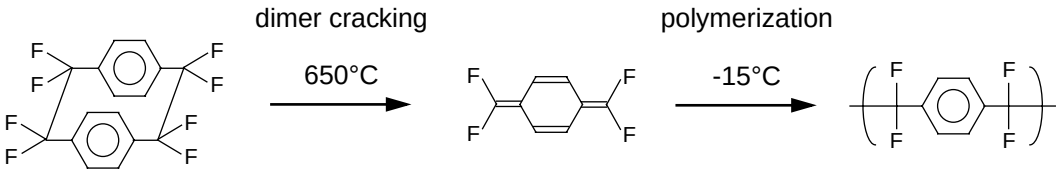


Figure 3-6 Structural formula of Novellus AF-4 parylene-F [85].

Dielectric deposition occurs via a sequence of steps [71]. The process involves first the vaporization (or sublimation) of the di-tetrafluoro-*p*-xylylene dimer at about 150°C. The dimer is led into a reactor where it is cracked, or cleaved, at 650°C to form two reactive tetrafluoro-*p*-xylylene monomers. The monomers are led to a vacuum chamber, condense on the wafer surface which is maintained at -15°C, diffuse into the bulk of the parylene-F film, and then polymerize by reacting with the ends of the free-radical polymer chains. The deposition process is surface-reaction-limited. Therefore, the deposition rate can be dramatically increased by lowering the substrate temperature and increasing the surface absorption rate. After deposition, the film must undergo a vacuum anneal at 350°C to stabilize its properties.



(3-6)

Because parylene-F is deposited from the vapor phase, good conformality can be achieved. Parylene-F has been successfully integrated with conventional Al and W metallization. It is yet to be demonstrated in a Damascene Cu scheme where good gapfill ability is not important. The feasibility of parylene-F for Cu integration is questionable considering the thermal, mechanical, adhesion and dimer cost issues associated with this material.

3.4 Summary

This chapter reviewed basic properties of low-κ dielectrics and surveyed the families of low-κ dielectrics currently evaluated by the industry. The syntheses and chemistries of the six low-κ dielectrics investigated in this thesis were described. This chapter and the previous chapter presented the prerequisite information for comprehending specific process integration issues of Cu and low-κ polymers— the subjects of the following three chapters. Electrical leakage and anisotropy of fluorinated polyimide are examined in Chapters 4 and 5 respectively while the Cu drift behaviors of the six low-κ polymers of Section 3.3 are evaluated in Chapter 6.

Chapter 4 Interconnect Isolation

A functional integrated circuit typically contains many million interconnections, each of which must communicate an electrical signal from one part of a chip to another without being interfered by nearby interconnects. A successful interconnect process architecture must therefore demonstrate good electrical isolation between adjacent interconnects to ensure that signal integrity is maintained for all wiring. Because the materials properties of low-κ polymer dielectrics are substantially different from those of silicon dioxide, process integration of these polymers will necessarily require unique solutions which subsequently introduce unique interconnect isolation issues. For example, the use of inorganic dielectric liners will be ubiquitous in any low-κ polymer integration flow.

This chapter explores electrical leakage issues associated with the integration of a low-κ polymer dielectric, fluorinated polyimide in particular, to address the impact of inorganic dielectric liners. The experiments to follow are aimed to identify leakage paths and sources of electrical conduction between isolated interconnects. The importance of moisture-induced leakage and leakage along the interface between the low-κ polymer and dielectric liner as potential integration issues will be demonstrated.

4.1 Dielectric Liners

Implementation of low-κ polymer dielectrics in a manufacturable multilevel interconnection scheme will almost invariably require inorganic dielectric liners such as silicon dioxide (oxide) and silicon nitride (nitride) to be incorporated [86]–[88]. Figure 4-1 illustrates a potential Damascene integration scenario where thin oxide liners have been inserted to cap the via-level and wire-level low-κ dielectric layers.

The dielectric liners serve a variety of functions in a Damascene integration. First, they are employed as hard masks for defining the wire-level and via-level low-κ dielectric etches. Since both photoresist and low-κ polymer are carbon-based, the oxygen plasma that etches the low-κ polymer will also attack the photoresist mask during the low-κ polymer etch. Conversely, the oxygen plasma in the subsequent photoresist strip is not selective against etching the low-κ polymer. This poor etch selectivity can be overcome by capping the low-κ polymer with a thin hard mask prior to etching the polymer and then performing the low-κ polymer etch and photoresist strip simultaneously. As explained in

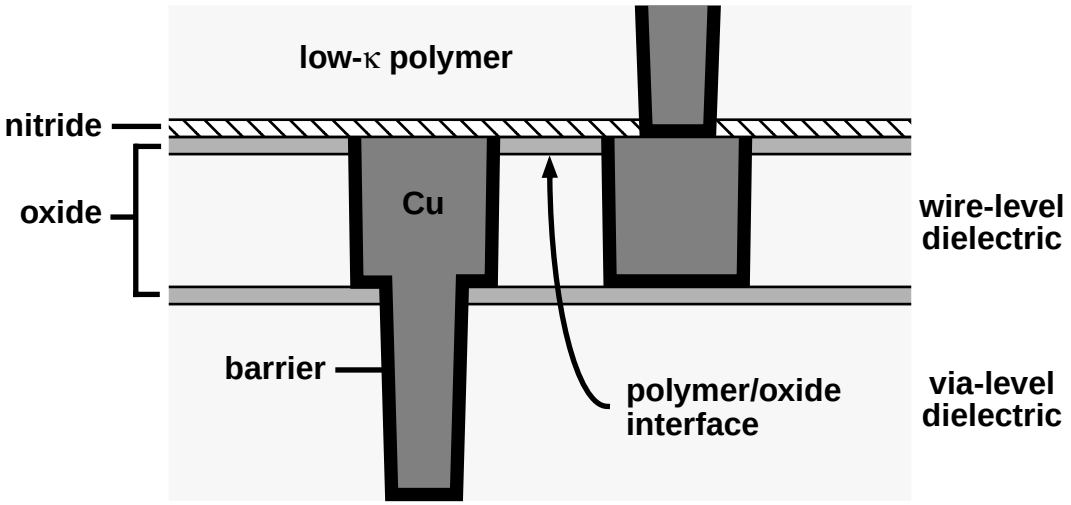


Figure 4-1 Cross-section of Damascene Cu and low-κ polymer dielectric integration scheme illustrating incorporation of thin oxide liners. The nitride liner passivates the top Cu surface to prevent Cu diffusion and drift from the interconnect into a low-κ polymer with poor Cu barrier property.

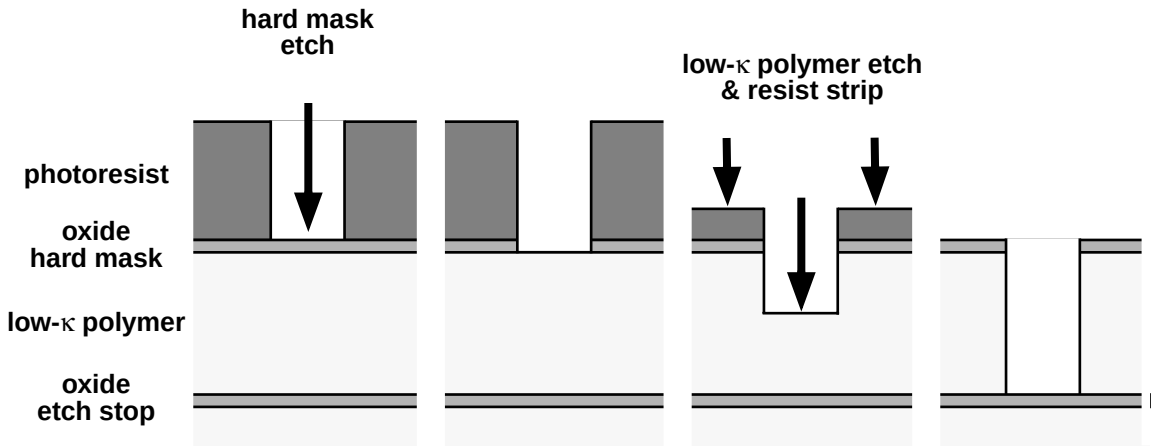


Figure 4-2 Use of oxide hard mask for patterning low-κ dielectric.

Figure 4-2, the hard mask is first patterned by the photoresist mask using a freon chemistry that is selective against etching the low-κ polymer. If the thickness of the hard mask is carefully optimized, the liner may possibly serve as an anti-reflection layer for photoresist exposure, enabling more aggressive interconnect geometries to be attained. The hard mask pattern is transferred to the exposed low-κ polymer in an oxygen plasma during which the photoresist is also stripped. The thicknesses of photoresist and low-κ polymer must be carefully optimized so that following the etch, the photoresist is completely removed. In addition to its roles in patterning the low-κ polymer, the dielectric liner can also be utilized as an etch stop in a dual-Damascene integration that employs a buried etch stop [49]. A third role of the dielectric liner is as a stop layer for chemical-mechanical polishing that follows copper deposition. Since low-κ polymers are relatively soft and mechanically weak compared to oxide, the polymers may not be able to withstand the abrasive shear forces present during the polishing process after the metal in the field regions has been cleared.

4.2 Dielectric Interface Leakage

Employing dielectric liners such as oxide will inadvertently introduce additional dielectric interfaces between these liners and the low-κ polymer. As illustrated in

Figure 4-1, the low-κ polymer/oxide interface may be a possible path for additional electrical leakage between adjacent interconnects since the interface may be intrinsically prone to electrical conduction. Moreover, since low-κ polymers are not completely impervious to moisture uptake, traces of moisture uptake by the low-κ polymer may induce additional bulk and interface leakage currents. Moisture is notorious for increasing surface and bulk electrical leakage in dielectrics [89]–[91].

4.2.1 Fabrication of Test Structures

Damascene Al(Cu) interconnects inlaid in oxide and passivated by fluorinated polyimide were studied to examine leakage issues along the low-κ polymer/oxide interface. Specifically, the interdigitated *comb1*/*serpentine*/*comb2* structure, consisting of three independent electrodes, was fabricated for intralevel leakage current measurements. See Figure 4-3. The Damascene Al(Cu) process was developed at Motorola's Advanced Process Research and Development Laboratory [92]. Al interconnects were used instead of Cu interconnects to avoid complications stemming from Cu drift in the dielectrics. Cu drift in dielectrics introduces additional leakage current and will cause dielectric failure [84].

The processing sequence commenced with a 6.8-nm gate oxidation on 200-mm, 10-Ω•cm n-type Si substrates followed by a 1.6-µm PECVD TEOS oxide deposition. The

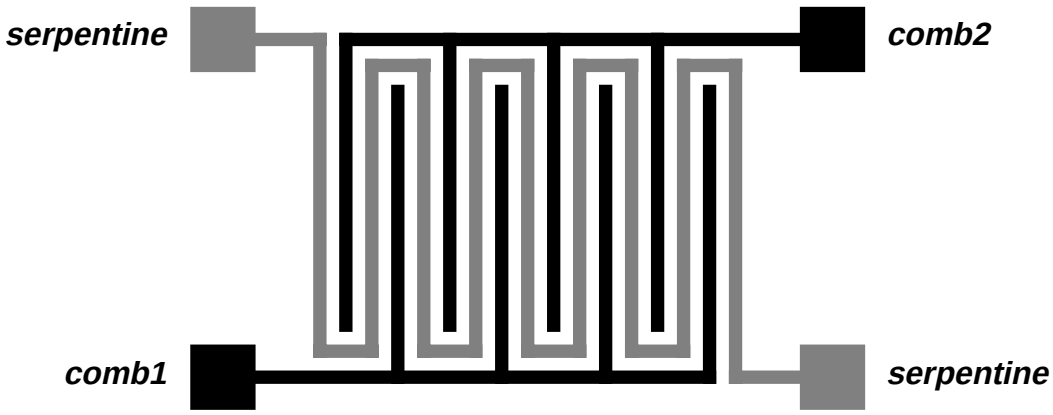


Figure 4-3 Plan view schematic of interdigitated metal test structure.

oxide grown on the wafer backside was then stripped. Subsequently, the front oxide surface was patterned to form 0.5-µm deep trenches in a timed etch. The resulting trenches were filled by a conformal Al(0.5%Cu) process sequence consisting of 20 nm PVD (i.e., sputtered) Ti at 200°C, 0.1 µm collimated PVD Al at 200°C, 0.8 µm CVD Al at 265°C, and 0.6 µm PVD Al(1%Cu) at 400°C. The CVD Al precursor was DMAH (dimethyl aluminum hydride). The PVD Al(1%Cu) was sputtered at 400°C to alloy the underlying Al with 0.5% Cu for electromigration resistance. Following the metal fill, the excess metal was immediately removed by chemical-mechanical polishing, resulting in planarized Damascene metal lines with equal line width and spacing of 0.5 µm, and a *serpentine* length of 1.7 m.

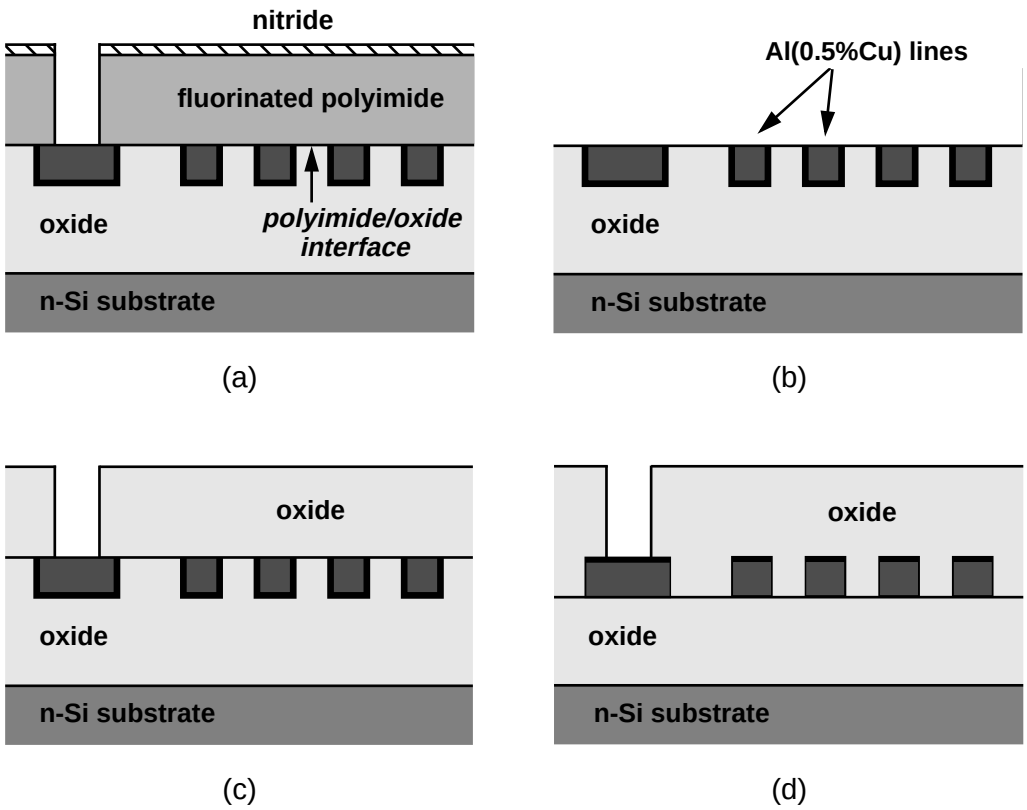


Figure 4-4 Cross-sectional schematic of experimental splits: (a) polyimide-passivated Damascene Al(Cu), (b) unpassivated Damascene Al(Cu), (c) oxide-passivated Damascene Al(Cu), and (d) oxide-gapfilled RIE Al(Cu). The metal lines have the same line width and spacing of 0.5 µm.

The Damascene metal wafers comprised three experimental splits. In the first split [Figure 4-4(a)], a DuPont VM651 adhesion promoter was applied and 1.2 µm DuPont FPI-136M fluorinated polyimide [82] was subsequently spun over the Damascene lines, cured at 400°C for 30 minutes, and capped by a 0.18-µm PECVD nitride hard mask. The nitride/polyimide stack was then etched to expose metal pads for test probing (Figure 4-5). The second and third splits (experimental controls) had no passivation [Figure 4-4(b)] and 1.2-µm TEOS oxide passivation respectively [Figure 4-4(c)].

A fourth split, consisting of oxide-gapfilled RIE metal (0.5-µm thick Ti/TiN/Al(0.5%Cu)/Ti/TiN stack) on 1.1 µm TEOS, was fabricated using Motorola's baseline 0.35-µm process for a technology comparison [Figure 4-4(d)]. In this non-Damascene process, the metal line spaces were filled by a conformal ozone-TEOS process followed by a standard PECVD TEOS oxide deposition. The oxide was then planarized by chemical-mechanical polishing down to a height of 1.2 µm above the metal. The metal lines in this split also have the same line width, line spacing, and serpentine length as the Damascene splits. All wafers were annealed in a forming gas ambient at 390°C for 30 minutes prior to electrical testing.

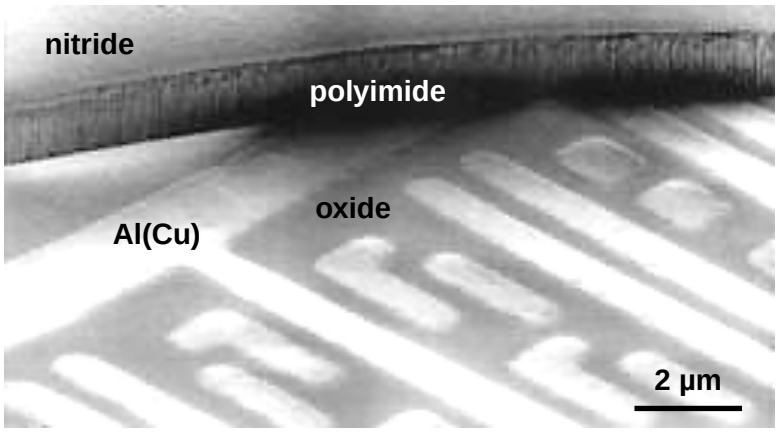


Figure 4-5 Scanning electron micrograph of polyimide-passivated Damascene Al(Cu) after polyimide etch illustrating polished Al(Cu) lines and polyimide sidewall.

4.2.2 Electrical Testing

Intralevel leakage currents between the *serpentine* and *comb* (*comb1* + *comb2*) electrodes were measured in the 100 to 275°C range using an HP4156A Precision Semiconductor Parameter Analyzer. With both *comb* and substrate grounded, a voltage ramp starting from zero bias was applied to the *serpentine* to force current into the other electrodes via possible leakage paths indicated in Figure 4-6. As confirmed by capacitance–voltage (*C*–*V*) measurements in Figure 4-7, positive V_{serp} conditions ensured the Si surface remained in deep accumulation to behave essentially as a grounded plate during the current–voltage (*I*–*V*) sweep. Since no potential difference existed between the *comb* and the substrate, the current returning to the *comb* electrode (I_{comb}) was measured to decouple parasitic leakage to the substrate. Otherwise, measurement of I_{serp} would include both lateral and substrate leakage components. Electrical noise at elevated temperatures, primarily originating from the hot chuck, was suppressed by grounding the substrate. Finally, dielectric charging was minimized by applying a relatively fast *I*–*V* sweep.

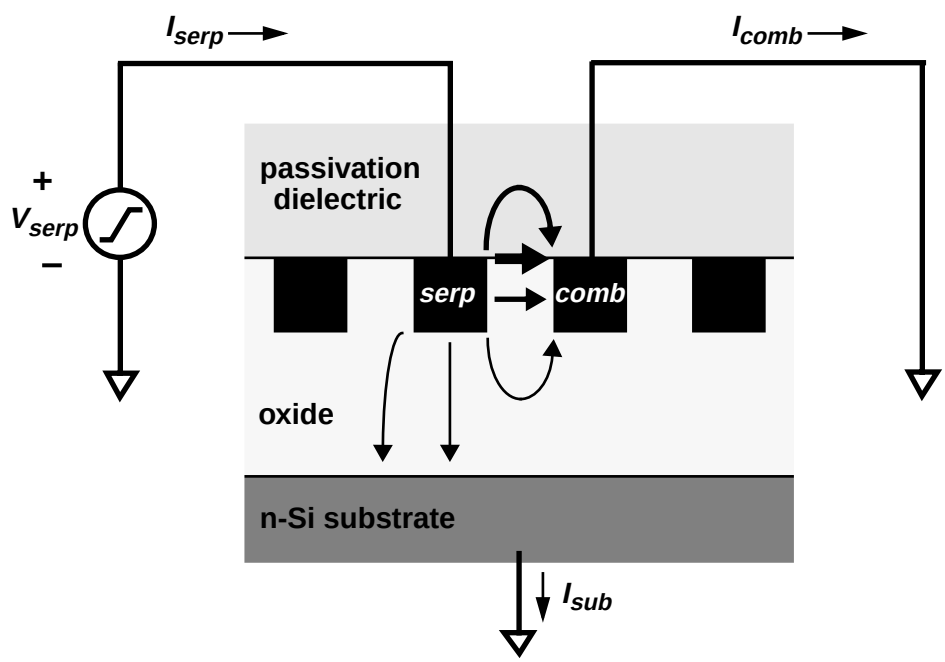


Figure 4-6 Electrical setup to measure intralevel leakage current at 100–275°C.

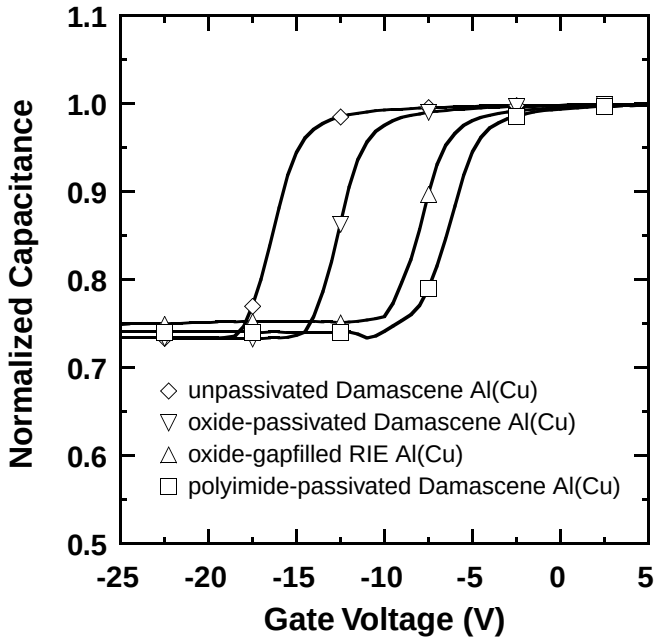


Figure 4-7 High-frequency (1 MHz) *C–V* measurements demonstrating that Si surface is in accumulation at zero gate bias. *Comb1*, *serpentine*, and *comb2* were shorted together as the common gate electrode.

Figure 4-8 shows linear *I–V* characteristics at low electric fields (< 0.1 MV/cm). The low-field leakage conductance (slope of *I–V* trace) was used as a representative measure in leakage comparisons. At these current levels, the resistance of the *serpentine*, averaged to be about 0.4 MΩ from *I–V* measurements across the two ends of the *serpentine*, was too small to produce an appreciable voltage gradient along the length of the *serpentine*. Consequently, the distributed resistance along the *serpentine* was neglected.

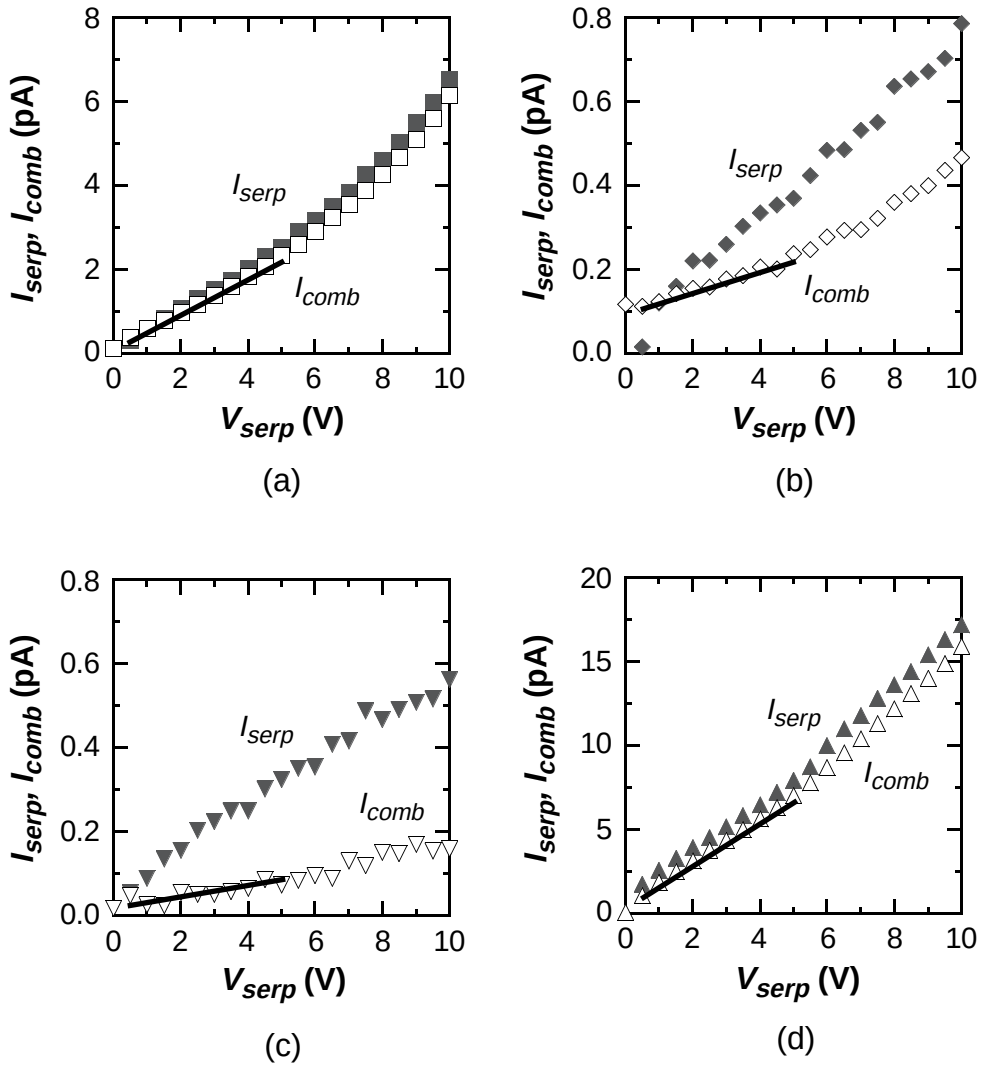


Figure 4-8 Typical *I–V* characteristics of intralevel leakage at 150°C for (a) polyimide-passivated Damascene Al(Cu), (b) unpassivated Damascene Al(Cu), (c) oxide-passivated Damascene Al(Cu), and (d) oxide-gapfilled RIE Al(Cu). The I_{comb} regression slopes are used for comparisons.

4.2.3 Experimental Results

4.2.3.1 Moisture Instability

A moisture-induced leakage instability was first examined (Figure 4-9). At 150°C, the leakage in polyimide-passivated lines was over three orders of magnitude higher than those in the others before falling asymptotically after many hours of baking. When the polyimide films re-equilibrated to ambient humidity at 20°C, the same leakage transient was observed upon heating. This transient behavior is attributed to outgassing of moisture from the polyimide, as confirmed by residual gas analysis (RGA) of an unpassivated 0.5-µm thick blanket fluorinated polyimide film heated to 200°C in vacuum (Figure 4-10). The nitride hard mask is believed to be responsible for the long outgassing time since nitride is a good moisture barrier. Similar behavior was observed in unpassivated lines on which surface moisture could reside prior to heating. However, leakages in the two splits of metal lines completely sealed in TEOS oxide remain unchanged with heating. This

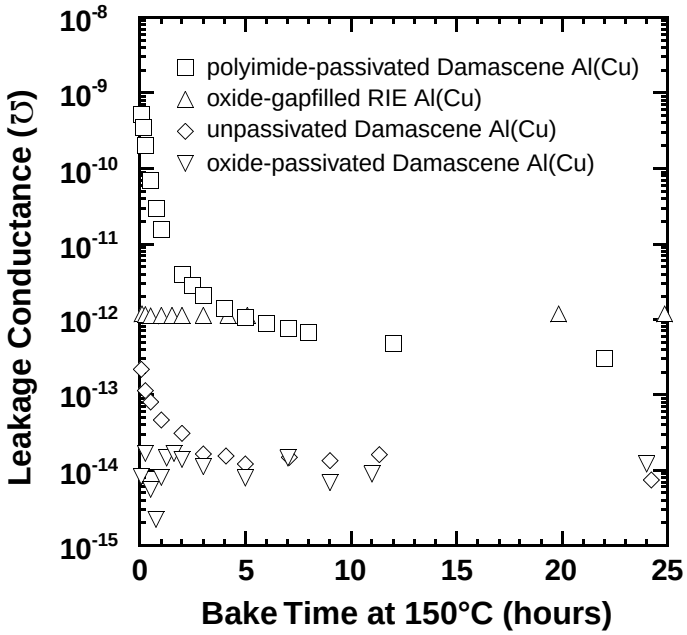


Figure 4-9 Moisture-related leakage instability at 150°C.

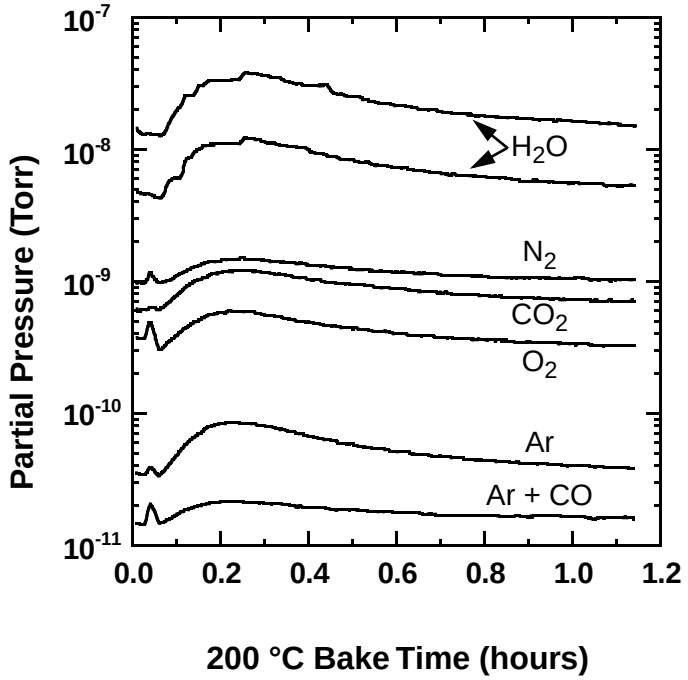


Figure 4-10 Residual gas analysis of fluorinated polyimide film heated to 200°C in vacuum.

observation is consistent with [93] reporting the absence of moisture uptake in TEOS oxide films.

4.2.3.2 Leakage Comparison

After a 24-hour bake to remove the moisture, leakage conductances were compared at 150°C. Figure 4-11 illustrates that the polyimide-passivated lines exhibit statistically more than an order of magnitude increase in leakage current over the unpassivated and oxide-passivated lines. Since the three Damascene splits are structurally identical except for the passivation dielectric, there must be additional leakage paths in the polyimide layer. All Damascene Al(Cu) structures, even with polyimide passivation, exhibited smaller intralevel leakage than the RIE Al(Cu) structure, which demonstrated a potential benefit of this inlaid process technology. Similar results were obtained at other temperatures (Figure 4-12).

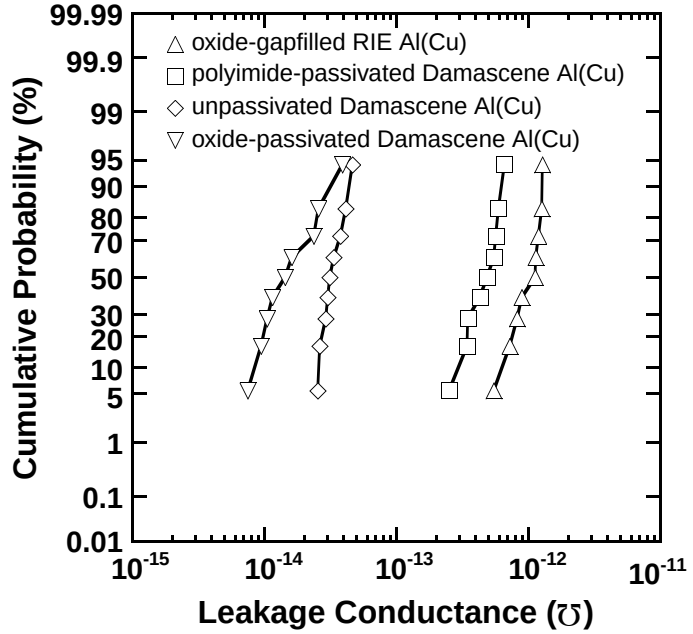


Figure 4-11 Leakage conductance at 150°C after 24-hour bake at 150°C.

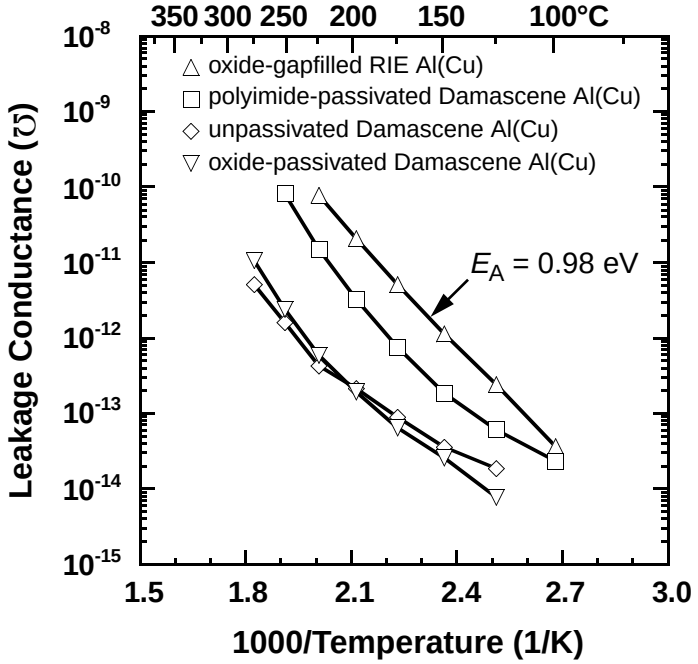


Figure 4-12 Arrhenius plot of leakage conductance after a 24-hour bake at 150°C.

4.2.3.3 Leakage Path Determination

Since additional leakage was observed only in the polyimide-passivated samples, the experiment depicted in Figure 4-13 was conducted to deduce the primary leakage path. Two conduction paths were considered— the polyimide/oxide interface and the polyimide bulk. A voltage ramp was applied to the *comb1* electrode to force leakage currents into the *serpentine* and *comb2* electrodes, both of which were grounded. Should interfacial leakage be dominant, I_{comb1} would concentrate along the polyimide/oxide interface into the *serpentine*, leaving $I_{comb2} \approx 0$ since $V_{serp} = V_{comb2}$ [Figure 4-13(a)]. On the other hand, should bulk polyimide conduction dominate, some current would traverse from *comb1* to *comb2* via fringing fields in the polyimide [Figure 4-13(b)]. In this case, $I_{comb2} \neq 0$ and I_{serp}/I_{comb2} would be similar to C_{serp}/C_{comb2} where C_{serp} and C_{comb2} are crosstalk capacitances above the Damascene metal (Figure 4-14). Here, the permittivity and bulk conductivity of polyimide are assumed to be relatively isotropic such that $C_{serp} / C_{comb2} \approx G_{serp}/G_{comb2}$ where G_{serp} and G_{comb2} are conductances associated with C_{serp} and C_{comb2} respectively. Simulations predict that $C_{serp} / C_{comb2} \approx 5$ [94] but experimental results show that $I_{serp} / I_{comb2} \gg 5$ (Figure 4-15). Therefore, the polyimide/oxide interface is indeed the dominant leakage path.

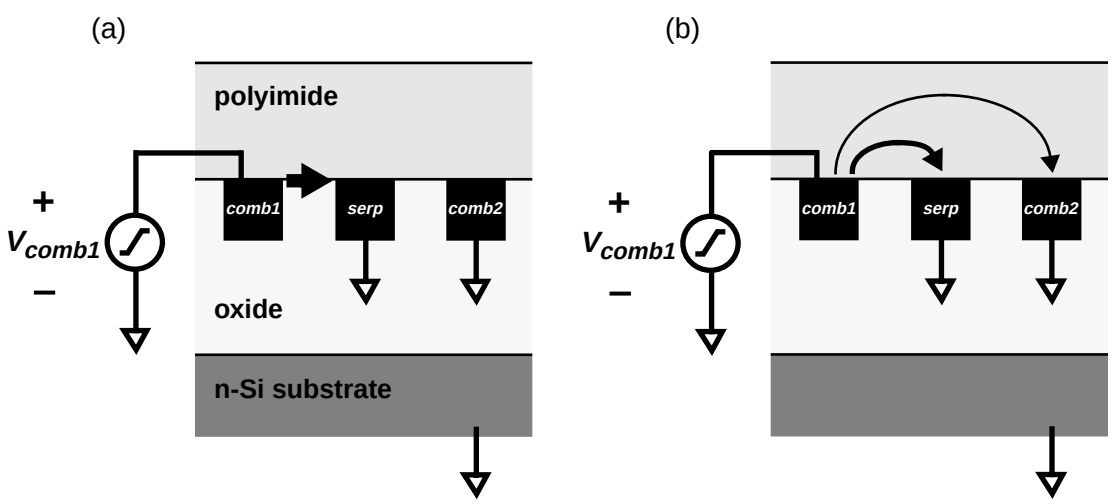


Figure 4-13 Experiment to distinguish between (a) interfacial and (b) bulk leakage paths in polyimide film.

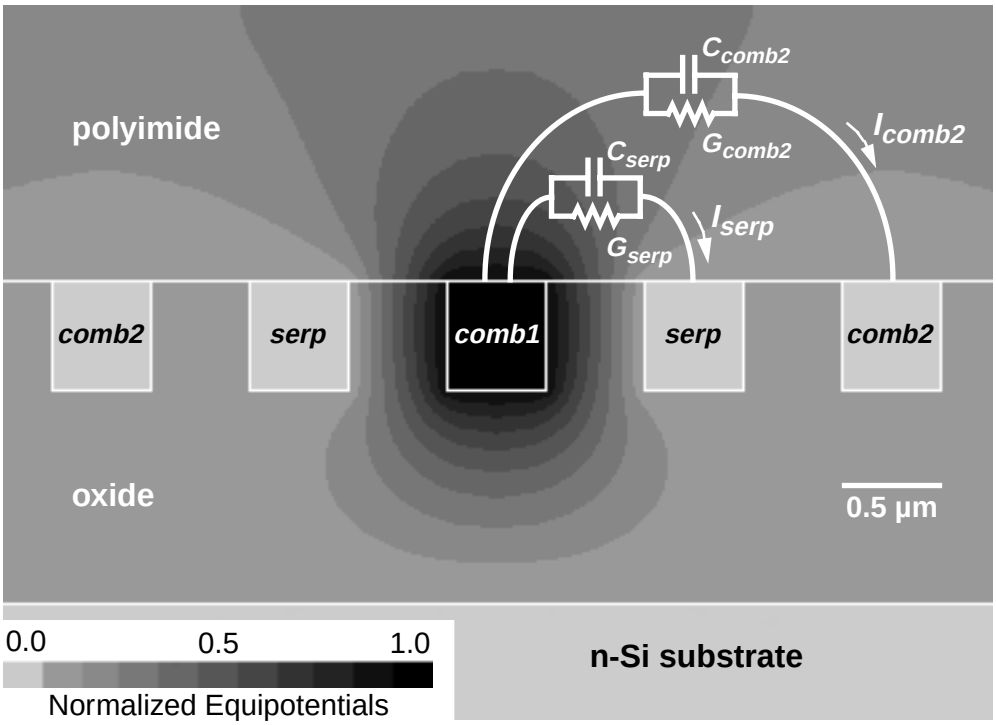


Figure 4-14 $I_{serp} / I_{comb2} \approx C_{serp} / C_{comb2} \approx 5$ for bulk polyimide conduction. Simulated equipotentials are shown.

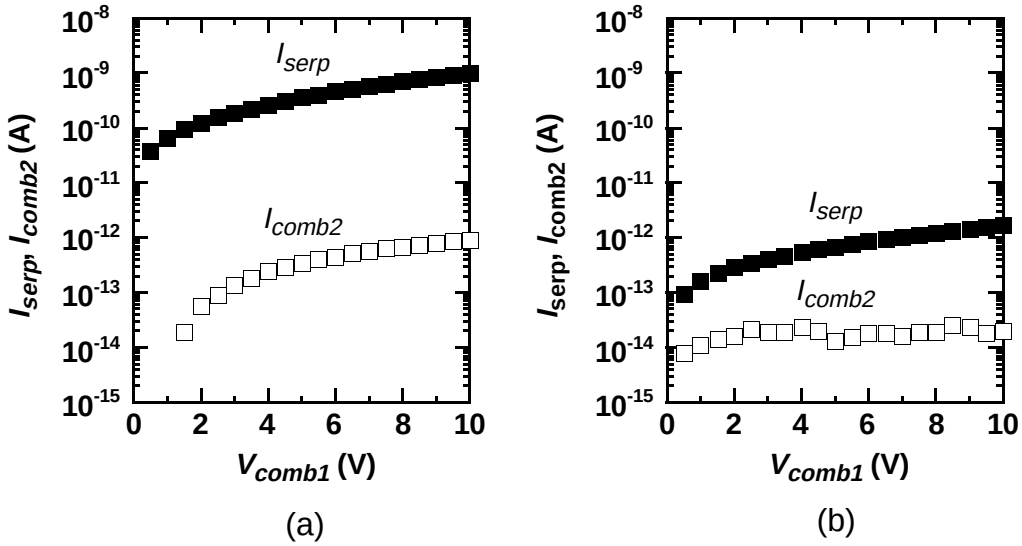


Figure 4-15 I_{serp} and I_{comb2} after (a) 0.1-hour and (b) 25-hour bake at 150°C with *serpentine* and *comb2* grounded.

4.2.3.4 Analysis of Electrical Results

It is clear from the reduction in I_{serp} with bake time that moisture impacts the interfacial leakage significantly. The corresponding reduction in I_{comb2} indicates that the bulk polyimide leakage is also degraded by moisture absorption. The linear *I–V* characteristics in Figure 4-8 and approximately exponential dependence of leakage on temperature in Figure 4-12 suggest that an ohmic-type conduction mechanism along the polyimide/oxide interface could be in effect. According to [95], the current flow associated with this dielectric conduction mechanism consists of thermally excited electrons hopping from one isolated state to the next, presumably along the polyimide/oxide interface. However, this hypothesis is speculatory. When moisture is present at the interface, the conduction mechanism could be entirely different. A previous study of moisture effects on electrical conductivity in Kapton™ polyimide [91] attributes the moisture-induced leakage to trace ionic salt impurities. The water dissolved in the polyimide film is thought to act as the aqueous phase in which salt impurities can dissociate, thus liberating ions which are free to move under an externally applied electric field and comprise an electrical current.

Further investigation is required to explain physically why polyimide passivation increases electrical leakage by an order of magnitude even after a 150°C bake to remove the moisture. In the next section, the possibility of interactions between fluorinated polyimide and Al(Cu) is evaluated. Other potential causes including the interactions of fluorinated polyimide and adhesion promoter with polished TEOS oxide surfaces remain to be examined.

4.2.3.5 Metal/Polyimide Interfacial Stability

The stability of the Al(Cu)/polyimide interface was confirmed by Rutherford backscattering (RBS) to address concerns that chemical reactivity between Al(Cu) and the deposited polyimide, potentially from the fluorine or acidity of the polyimide precursor or from the adhesion promoter, might be responsible for the observed electrical leakage behavior. As shown in Figure 4-16, blanket Al(Cu) films of the same thickness and depo-

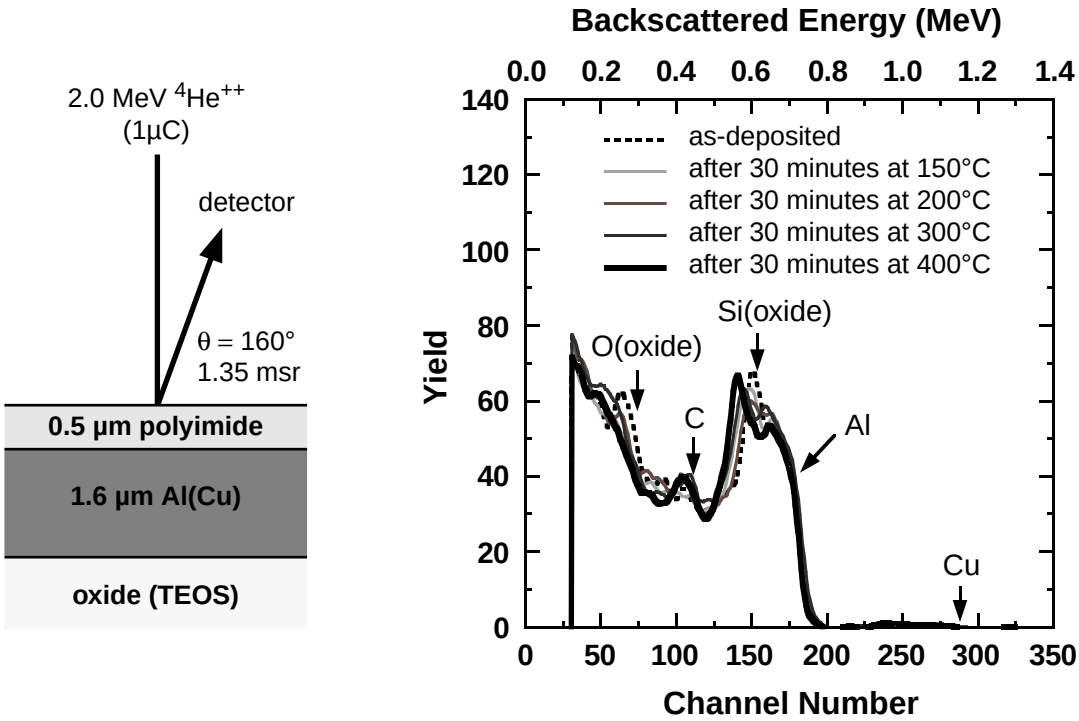


Figure 4-16 Rutherford backscattering spectra of fluorinated polyimide on Al(Cu), as-deposited and after 30-minute anneals at 150–400°C.

sition conditions as the Damascene metal films were prepared. Adhesion promoter and polyimide precursor were subsequently spun over the Al(Cu) films and baked at 130°C to evaporate the precursor solvent. The wafers were then subjected to one of the following temperatures for 30 minutes: 150, 200, 300, and 400°C. The resulting RBS spectra of the as-deposited and annealed films are found to be independent of the various heat treatments. Specifically, the slope of the Al edge remains unchanged, demonstrating that the Al(Cu)/polyimide interface is stable and no significant reaction has occurred [96].

4.2.4 Implications on Process Integration

The preceeding experiments have demonstrated that using dielectric liners to integrate fluorinated polyimide raises additional interconnect isolation concerns. The interface between dielectric liner and low-κ polymer introduces additional paths of electrical leakage. For dry polyimide films, the additional order of magnitude increase in leakage may

be tolerable since the leakage is comparable to a baseline oxide-gapfilled process that was used in manufacturing. However, this is not the case when moisture is present in polyimide. Minimizing the moisture content of polyimide during processing is thus critical to ensure good interconnect isolation. To isolate the metal lines from the leaky dielectric interfaces, oxide liner encapsulation of the interconnects will likely be required which unfortunately adds process complexity. Moreover, since κ_{oxide} typically ranges from 4.0 to 4.5, the challenge is to incorporate very thin, high-quality liners so that effective capacitance advantage of the low-κ polymer will not be compromised.

This work focuses on the impact of liners for Damascene architectures. Similar findings have been reported by workers at Texas Instruments in a thorough effort to integrate parylene-F with conventional RIE Al(Cu) interconnects [97]. See Figure 4-17. Although

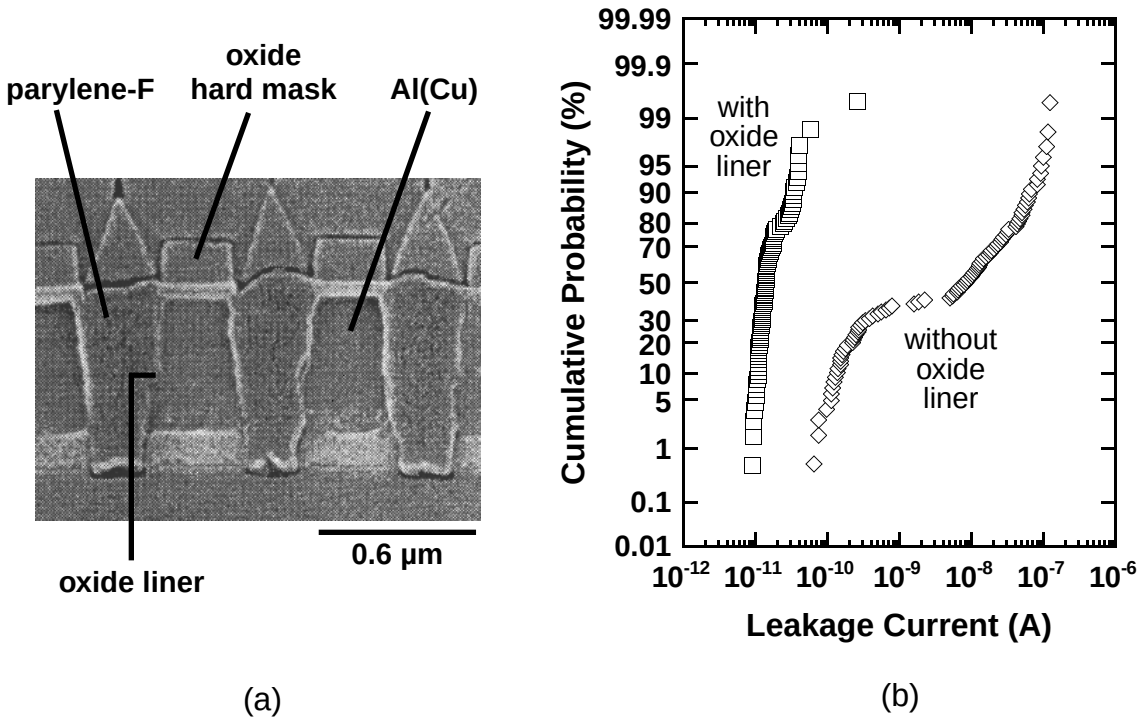


Figure 4-17 (a) Cross-sectional scanning electron micrograph illustrating Al(Cu)/parylene-F comb capacitor structure demonstrated by Texas Instruments. (b) Corresponding comb-to-comb leakage current with and without oxide liner encapsulation of interconnects [97].

the leakage paths were not identified, the absence of liner encapsulation of interconnects increased the intralevel or comb-to-comb leakage by a few orders of magnitude. Dielectric liners are therefore required in this integration scheme.

Despite the added process complexity, dielectric liners encapsulation also offer many other benefits [98]. They serve as a barrier to prevent reaction between the metal and potentially unstable low-κ materials such as those fluorinated varieties. Oxide liners also increase the low-κ dielectric breakdown strength by limiting bulk electrical conduction through the polymer. They may improve adhesion between metal and polymer. Electromigration resistance is also enhanced since the relatively harder oxide liner suppresses hillock formation. Finally, oxide is a more efficient thermal conductor than low-κ polymers and can thus dissipate interconnect Joule heating more effectively [99].

4.3 Summary

This chapter addressed the electrical isolation of low-κ polymer dielectric integration with Damascene interconnects. The use and impact of inorganic dielectric liners that will be needed in manufacturable Damascene architectures was examined. The investigation focussed on the effect of fluorinated polyimide passivation on electrical leakage current to examine dielectric interface leakage. Polyimide directly over Al(Cu) interconnects inlaid in oxide increases the intralevel leakage current mainly along the polyimide/oxide interface. Moisture absorbed in the polyimide further increases the interfacial as well as bulk leakages. These findings emphasize the importance of separating interconnects from direct contact with polyimide/oxide interfaces and minimizing moisture content of polyimide during processing to ensure good electrical isolation between interconnects. Complete liner encapsulation of interconnects is a potential solution provided that process complexity is minimized and that the capacitance advantage of the low-κ polymer is not severely compromised.

Chapter 5 Dielectric Constant Anisotropy

The capacitance advantage gained from low-κ polymer integration will be compromised not only by the incorporation of inorganic liners, as discussed in the previous chapter, but also by a large anisotropy in the polymer dielectric constant. Since many low-κ polymers are structurally very anisotropic, the electrical properties may exhibit strong directional dependences. In particular, the wafer in-plane (lateral) dielectric constant, $\kappa_{||}$, can be much larger than the wafer out-of-plane (vertical) dielectric constant, $\kappa_{\perp}$. This consideration is often undermined since $\kappa_{\perp}$, being most easily measured, is typically reported instead of $\kappa_{||}$. In fact, $\kappa_{||}$ can exceed $\kappa_{\perp}$ by as much as 30% in some polyimides, as seen in Figure 5-1 [47], [100]. The larger $\kappa_{||}$ can significantly impact the interconnect density as adjacent metal lines must be adequately spaced apart to mitigate coupling of crosstalk noise. Also, large anisotropies may render certain low-κ candidates inadequate for integration considering that the effective dielectric constant of interlevel dielectrics is targeted for 20–30% reduction with the introduction of every new technology generation [24].

This chapter presents an electrical technique for estimating $\kappa_{||}$ of a blanket low-κ polymer film. The technique is intended for evaluation of dielectrics considered for Damascene integration and is demonstrated using fluorinated polyimide. Common techniques for measuring $\kappa_{||}$ will be reviewed along with a discussion of their limitations.

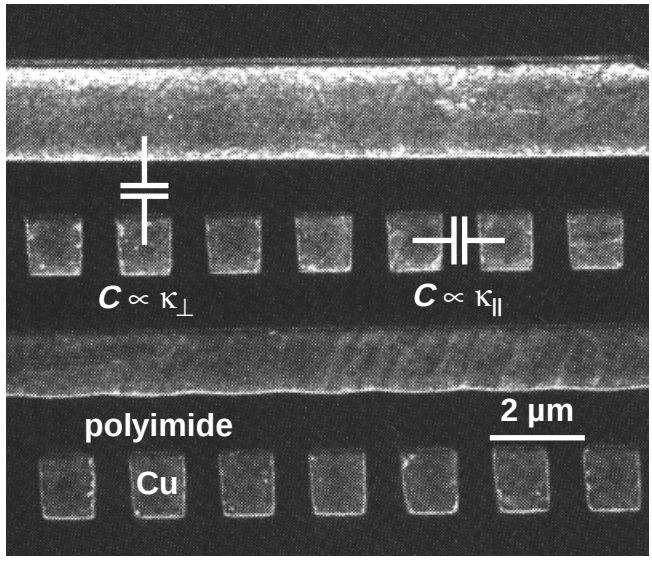


Figure 5-1 Cross-sectional scanning electron micrograph of Cu/polyimide interconnect system demonstrated by IBM. The polyimide has $\kappa_\perp$ and $\kappa_{||}$ of 2.9 and 3.7 respectively [47].

5.1 Conventional Techniques and their Limitations

The wafer out-of-plane dielectric constant, $\kappa_\perp$, is obtained by measuring the capacitance, typically at 1 MHz, of a parallel-plate capacitor with known area, *A*, and dielectric thickness, *d*, as given by Eq. (5-1).

$$C = \kappa_\perp \varepsilon_0 \frac{A}{d} \tag{5-1}$$

The capacitor area must be large in order to minimize the contribution from perimeter fringing fields. The structure typically fabricated for this measurement is a planar metal-insulator-silicon (MIS) capacitor. Although the principle of measurement is trivial, an accurate evaluation of $\kappa_\perp$ requires that the dielectric thickness be accurately determined, a good contact to the wafer backside be formed, and that the capacitance be measured at a bias where the silicon surface is in deep accumulation. The latter two considerations, if ignored, often lead to underestimation of $\kappa_\perp$ arising from neglected series capacitances.

The techniques for obtaining the wafer in-plane dielectric constant, $\kappa_{||}$, are not as straightforward as that for obtaining $\kappa_{\perp}$. Both optical and electrical methods are reviewed.

5.1.1 Optical Prism Coupler

$\kappa_{\perp}$ and $\kappa_{||}$ of a blanket dielectric film can be extracted optically using a prism coupler. The prism coupler measures the out-of-plane (transverse magnetic) index of refraction, n_{TM}, and in-plane (transverse electric) index of refraction, n_{TE}, of the dielectric film. Eqs. (5-2) and (5-3) are then applied to calculate $\kappa_{\perp}$ and $\kappa_{||}$ respectively.

$$\kappa_{\perp} = n_{TM}^2 \tag{5-2}$$

$$\kappa_{||} = n_{TE}^2 \tag{5-3}$$

The principle of measurement is illustrated in Figure 5-2 [101], [102]. The thin film sample to be measured is brought into contact with the base of a prism by means of a pneumatic coupling head, creating a small air gap between the film and the prism. A laser beam strikes the base of the prism and is normally totally reflected at the prism base onto a photodetector. At certain discrete values of the incident angle, called mode angles, the laser beam can penetrate across the air gap into the film and enter into a guided optical propagation mode. This coupling of energy into the film will subsequently cause a sharp drop in the intensity of reflected light reaching the detector. The angular location of the first mode approximately determines the film index, while the angular separation between the modes determines the film thickness. By controlling the polarization of the laser beam incident to the prism, both n_{TM} and n_{TE} can be measured, thus allowing the optical anisotropy or birefringence to be determined.

The prism coupler is a convenient means of measuring $\kappa_{\perp}$ and $\kappa_{||}$. However, estimates of dielectric constant at optical frequencies are optimistic since dielectrics are generally less polarizable at optical frequencies (THz range) than at lower electrical frequencies (MHz range) [69].

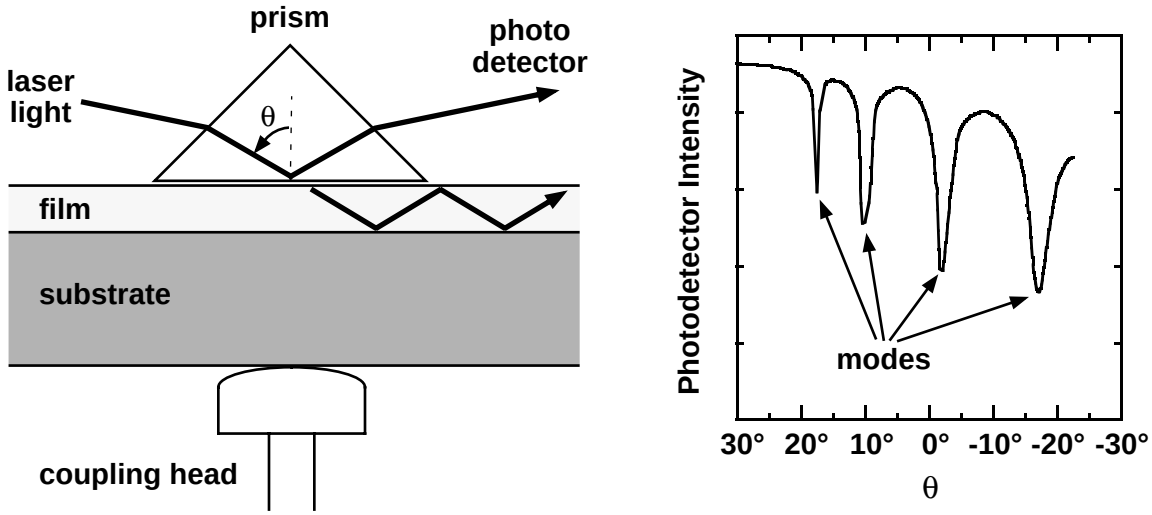


Figure 5-2 Schematic of prism coupler technique for measuring n_{TM} and n_{TE}.

5.1.2 Crosstalk Capacitance of Gapfilled Interdigitated Lines

$\kappa_{||}$ is estimated electrically by measuring the lateral crosstalk capacitance, $C_{crosstalk}$, between interdigitated metal lines [103], [104]. In a conventional RIE metal technology, the common test structure consists of closely spaced, etched metal lines that are gapfilled with the low-κ dielectric of interest as shown in Figure 5-3(a). The metal spaces should have a large cross-sectional aspect ratio so that the sidewall component of $C_{crosstalk}$, equivalently the influence of $\kappa_{||}$, is maximized. Once $C_{crosstalk}$ is measured, capacitance simulations are performed to model the fringing electric fields in order to decouple the effect of $\kappa_{\perp}$ and determine $\kappa_{||}$ [105]. A good estimate of $\kappa_{||}$ requires modeling the fringing fields above and below the metal lines since these fields contribute substantially to the total crosstalk. An independent measurement of $\kappa_{\perp}$ from planar capacitors is required.

The metal gapfill approach, unfortunately, has limited utility in evaluating dielectrics intended for Damascene applications. First, the feasibility of the test structure hinges on a successful high aspect-ratio dielectric gapfill. Some dielectrics, such as fluorinated polyimide, exhibit poor gapfill ability as shown in Figure 5-3(b), yet possess attractive quali-

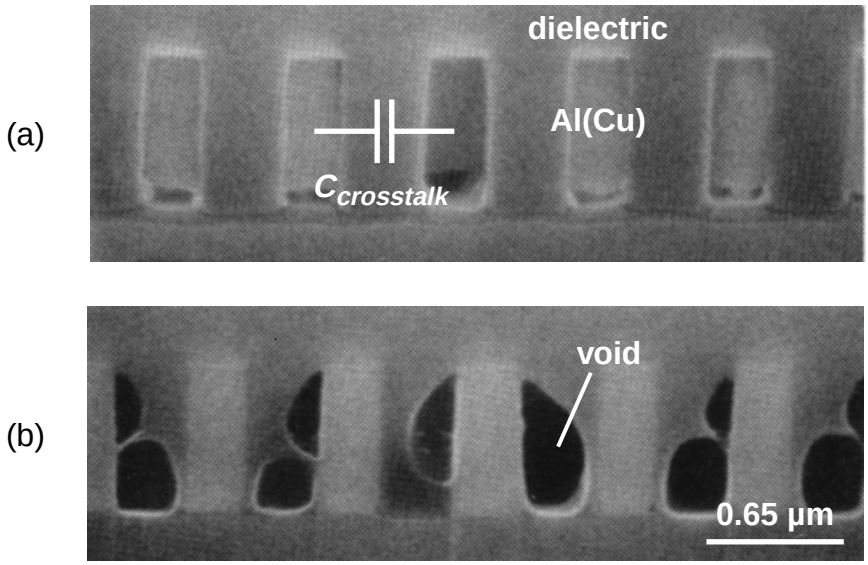


Figure 5-3 (a) Measurement of $\kappa_{||}$ from crosstalk capacitance between metal lines gapfilled with polymer dielectric. (b) Technique is limited in part by poor dielectric gapfill [103].

ties for Damascene metallization where only blanket low-κ polymer deposition is required. The gapfill ability of fluorinated polyimide could be improved by modifying the low-κ polymer precursor chemistry [96]. However, this endeavor compromises other material properties, such as the mechanical strength of the polymer. Another potential drawback of the gapfill approach occurs for very aggressive line geometries. Even if dielectric fill is successful in very narrow gaps, the extracted $\kappa_{||}$ for this test structure may not be representative of $\kappa_{||}$ in a Damascene integration. In the Damascene scheme, $\kappa_{||}$ reflects the lateral polarizability of a blanket low-κ polymer film deposited on a planar surface. One can envision that especially for linear polymers, the gapfilling process requires the polymer chains to conform to the topography of the metal lines and spaces. For conformal depostion along the vertical metal sidewalls, horizontal electric fields in the $C_{crosstalk}$ measurement would probe the in-plane as well as the unintended out-of-plane character of the polymer chains, rendering subsequent extraction of $\kappa_{||}$ to be inaccurate.

5.2 Electrical Anisotropy of a Blanket Dielectric

The following electrical technique eliminates the limitations associated with the preceeding techniques. A blanket low-κ dielectric film, fluorinated polyimide in this demonstration, is deposited over interdigitated Damascene Al(Cu) lines and the crosstalk capacitance is measured. The fringing electric fields in the overlying dielectric are then examined in order to extract $\kappa_{\parallel}$.

5.2.1 Theory of Measurement

Consider the cross-section of interdigitated Damascene metal lines passivated by a thick dielectric as illustrated in Figure 5-4. The lateral crosstalk capacitance between adjacent lines, $C_{crosstalk}$, is the sum of one sidewall (C_{side}) and two fringe components (C_{bottom} and C_{top}):

$$C_{crosstalk} = C_{bottom} + C_{side} + C_{top} \tag{5-4}$$

Provided the passivation dielectric is sufficiently thick to contain essentially all the electric field lines fringing above the metal,

$$C_{top} \propto \kappa_{top} \tag{5-5}$$

where κ_{top} is the effective (isotropic) dielectric constant of the passivation dielectric. The value of κ_{top} will be intermediate between $\kappa_{\perp}$ and $\kappa_{\parallel}$ of the passivation dielectric. For identical structures passivated by other dielectrics, that is, a different κ_{top}, ($C_{bottom} + C_{side}$) remains invariant. Hence, it follows that $C_{crosstalk}$ is a linear function of κ_{top}. This line is defined by measuring $C_{crosstalk}$ of structures passivated by two isotropic dielectrics with *known* dielectric constants. The unknown κ_{top} of polyimide ($\kappa_{polyimide}$) can then be interpolated from the measured $C_{crosstalk}$ of a polyimide-passivated structure, as illustrated in Figure 5-5, using Eq. (5-6). In this example, air ($\kappa_{air} = 1.0$) and TEOS oxide ($\kappa_{oxide} = 4.2$) were the two reference passivation dielectrics. After extracting κ_{top} and additionally

obtaining $\kappa_{\perp}$ from planar capacitors, interconnect capacitance simulations are performed to determine the $\kappa_{\parallel}$–$\kappa_{\perp}$ combination that is equivalent to the measured κ_{top}.

$$\frac{\kappa_{polyimide} - \kappa_{air}}{C_{polyimide} - C_{air}} = \frac{\kappa_{oxide} - \kappa_{air}}{C_{oxide} - C_{air}} \tag{5-6}$$

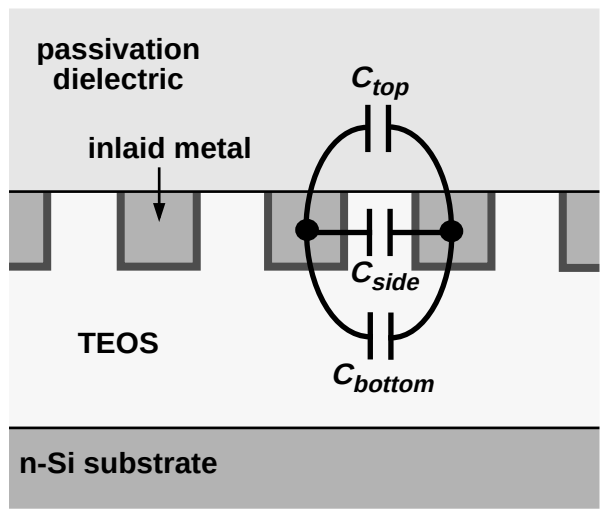


Figure 5-4 Cross-section of interdigitated Al(Cu) test structure, inlaid in oxide and passivated by a blanket dielectric.

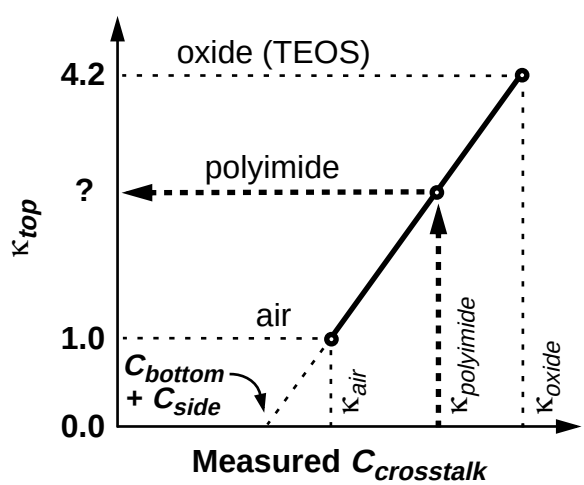


Figure 5-5 Linear interpolation to extract κ_{top}, the effective dielectric constant of the polyimide passivation.

5.2.2 Fabrication of Test Structures

The interdigitated Damascene metal test structures fabricated for the interconnect isolation studies in the previous chapter, shown in Figure 5-6, were used for the crosstalk capacitance measurements. Processing details are found in Section 4.2.1 of Chapter 4 but are summarized here. Processing commenced with a thin gate oxidation followed by a

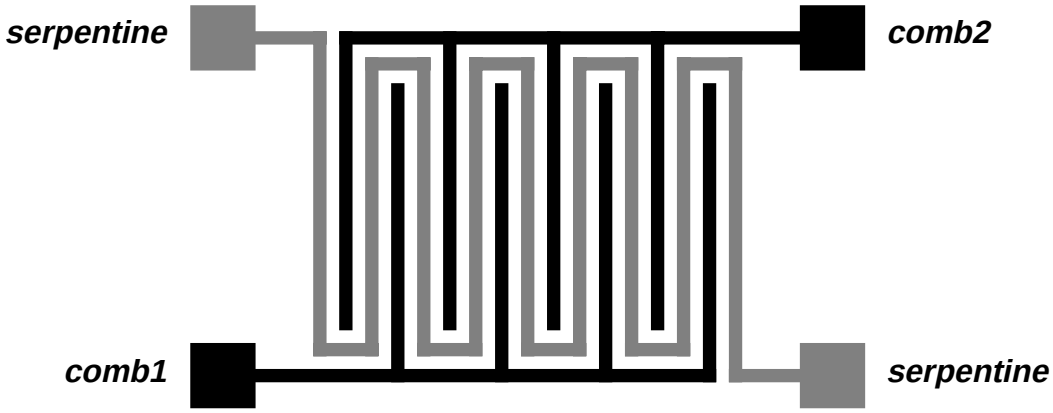


Figure 5-6 Plan view schematic of interdigitated metal test structure. *Comb1* and *comb2* are externally connected together to be a common *comb* electrode.

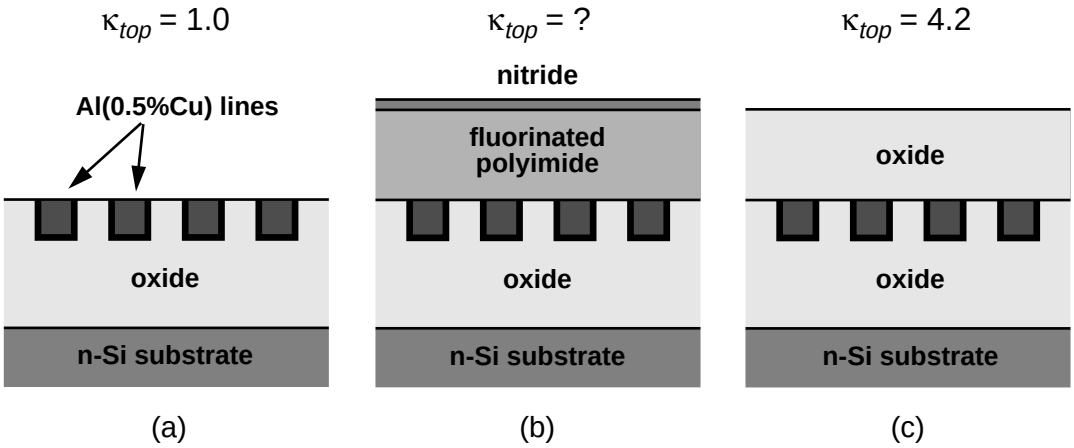


Figure 5-7 Cross-section of experimental splits: (a) unpassivated Damascene Al(Cu), (b) polyimide-passivated Damascene Al(Cu), and (c) oxide-passivated Damascene Al(Cu).

blanket 1.6-µm oxide deposition on n-type Si substrates. After backside oxide removal, trenches were formed by a 0.5-µm deep oxide etch and subsequently filled by a conformal Al(Cu) deposition. Following chemical-mechanical polishing of the excess metal to form the inlaid lines, the wafers were divided into three splits, respectively passivated by (1) air, (2) 1.2-µm oxide, and (3) 1.2-µm DuPont FPI-136M fluorinated polyimide [82]. See Figure 5-7. In the latter two splits, the passivation dielectric was etched to expose metal pads for test probing. A thin nitride film was deposited on the polyimide as a hard mask to pattern the polyimide. All wafers were annealed in a forming gas ambient prior to electrical testing. The resulting Damascene metal lines are 0.5 µm wide, with 0.5 µm separation between adjacent lines. The *serpentine* is 1.7 m long.

5.2.3 Electrical Testing

$C_{crosstalk}$ was measured at 1 kHz using an HP4194A Impedance/Gain-Phase Analyzer. The schematic of the measurement configuration is illustrated in Figure 5-8. The impedance between the HI and LO terminals was modeled by the HP4194A as a series connection of capacitor and resistor. The HI terminal of the test instrument, which applies the test voltage oscillation, was connected to the *serpentine* while the LO terminal, which measures the magnitude and phase of the resulting ac current with respect to the applied sinusoid, was connected to *comb1* and *comb2*. The two comb electrodes were shorted together to be the common *comb* electrode. Similarly, both ends of the *serpentine* were connected together. The dc level of the HI terminal was zero with respect to the LO terminal which was maintained at the instrument ground. To minimize noise and parasitic coupling between metal lines via the Si substrate, the wafer substrate was grounded. This substrate connection was not made to the LO terminal so as to avoid including any line-to-substrate coupling in the measured capacitance. In addition, a relatively large sinusoidal amplitude of 1 V was applied to maximize the ac signal current and to overcome the possible presence of trapped charge in the polymer. From capacitance–voltage (C–V) measurements (refer to Figure 4.7), the n-type Si surface was found to be in deep accumulation under these biases. This condition ensured that the entire Si substrate behaved as a

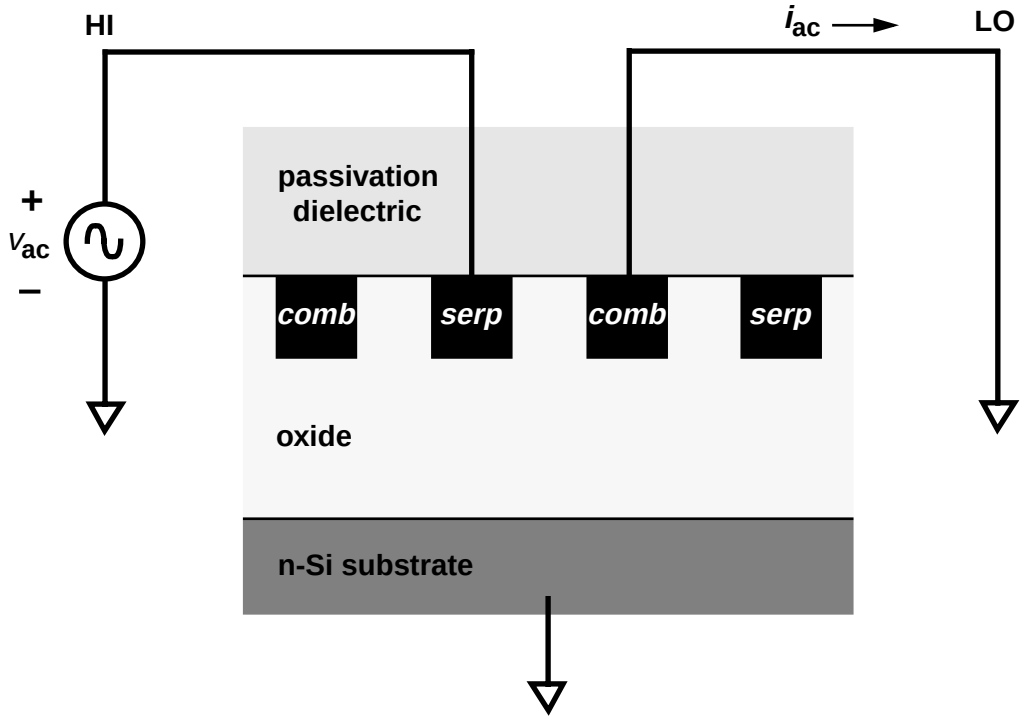


Figure 5-8 Electrical setup to measure lateral crosstalk capacitance between *serpentine* and *comb.*

grounded equipotential plane. Otherwise, series substrate resistance effects would degrade the integrity of the measured capacitance. $C_{crosstalk}$ was also measured at 1 kHz because at frequencies higher than 20 kHz, resistive shielding due to the *serpentine* line resistance would cause the measured capacitance to roll off regardless of the passivation dielectric [106]. These parasitic resistance effects are further examined in Section 5.2.7.

5.2.4 Experimental Results

Results of the extraction technique are shown in Figure 5-9. Fluorinated polyimide equilibrated to 40% relative humidity at 25°C is observed to have $\kappa_{top} = 3.3$. The same extraction at 150°C after a 24-hour bake at 150°C yields $\kappa_{top} = 2.8$, a value which remains unchanged with subsequent heating. The difference is attributed to moisture in the polyimide bulk and at the polyimide/oxide interface.

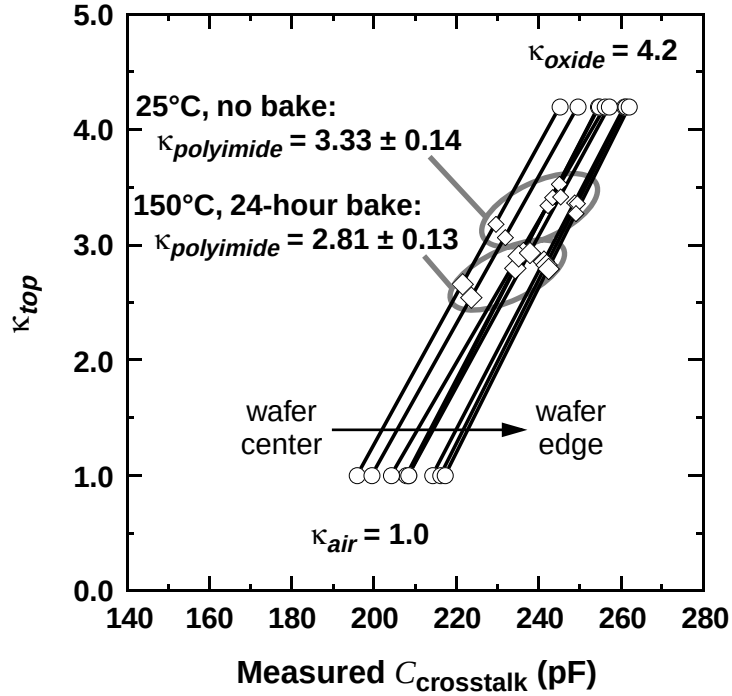


Figure 5-9 Effective dielectric constant of DuPont FPI-136M fluorinated polyimide.

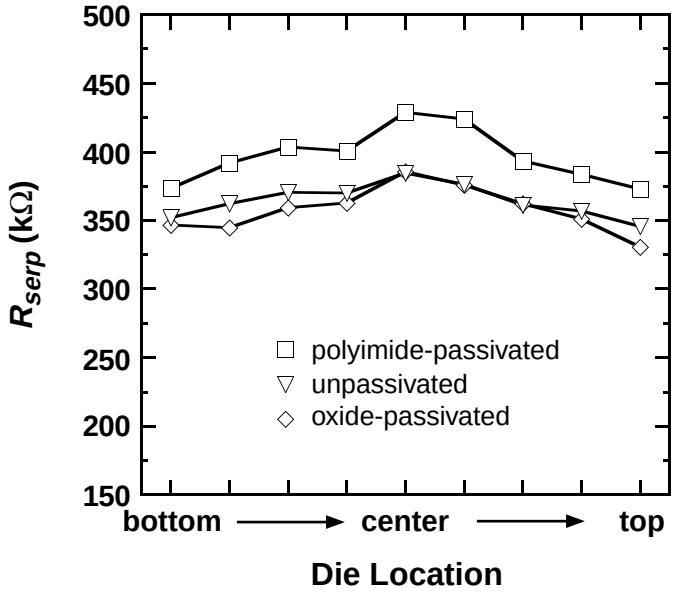


Figure 5-10 *Serpentine* resistance at 150°C showing agreement with variations in capacitance resulting from process nonuniformity.

Processing nonuniformities were considered by applying the extraction to the same die locations among the three wafer splits. The principal nonuniformity was due to Al(Cu) polishing. The polishing rate was preferentially higher at the wafer center and led to some oxide erosion near the wafer center, resulting in C_{side} variations. These variations are consistent with the higher *serpentine* line resistance, R_{serp}, near the wafer center. See Figure 5-10.

5.2.5 Simulations and Modeling

The κ_{top} extraction technique was confirmed by MEDICI™ two-dimensional interconnect capacitance simulations [94] where $C_{crosstalk}$ was simulated for Figure 5-7 cross-sections with κ_{top} values of 1.0, 2.8, and 4.2. As shown in Figure 5-11, simulation results demonstrate the expected linearity between $C_{crosstalk}$ and κ_{top} as well as verify good agreement between the measured and simulated values of $C_{crosstalk}$.

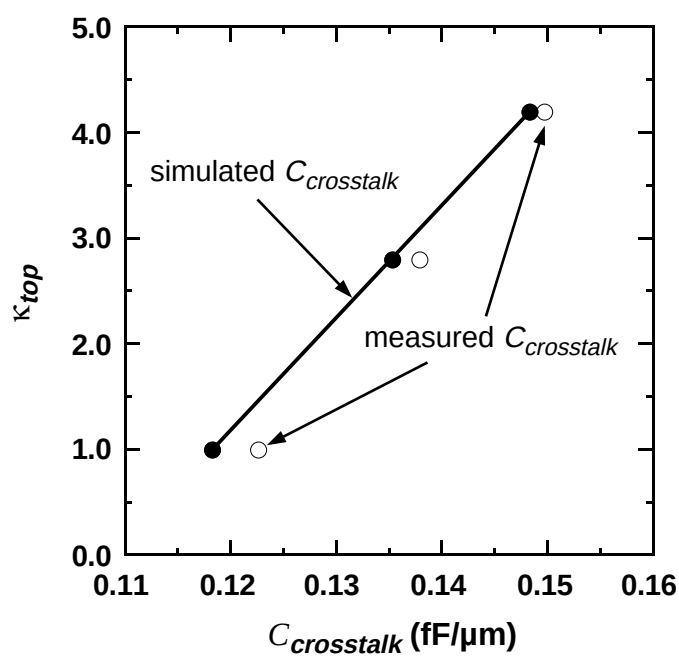


Figure 5-11 Confirmation of extraction technique by capacitance simulations.

The validity of the technique is also based on a sufficiently thick passivation dielectric to ensure that fringing electric fields do not spread above the passivation dielectric. Simulations show that in the absence of trapped charge in the dielectric, the fringe profile is insensitive to the dielectric material and field lines are essentially confined to the first 1.0 µm above the Damascene metal lines (Figure 5-12). For passivation dielectrics thinner than 1.0 µm, $C_{crosstalk}$ no longer remains constant since fringing fields now spread beyond the passivation layer into the dielectric above— air for oxide passivation and 0.18 µm nitride ($\kappa_{nitride} = 7.4$) for polyimide passivation. Hence, the passivation layer should be at least twice the intrametal spacing. In the fabricated structures, the passivation thickness was 1.2 µm. See Figure 5-13.

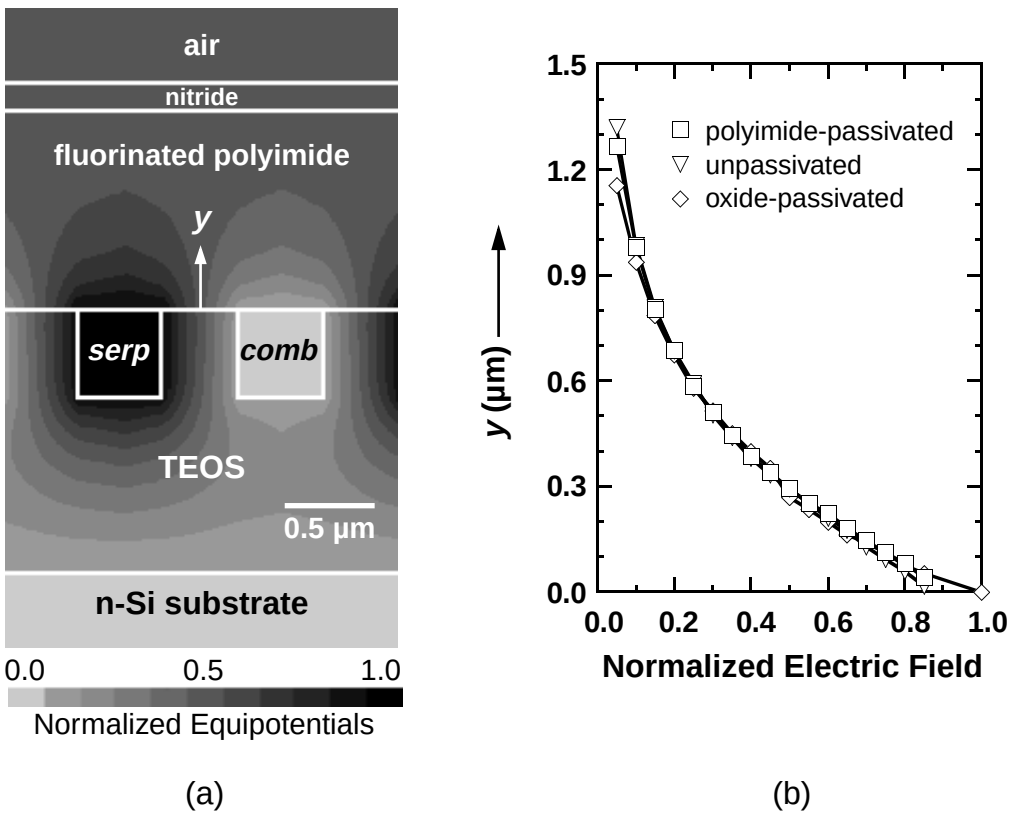


Figure 5-12 Simulated (a) potential contours for polyimide passivation and (b) electric field rolloff along half-plane midway between adjacent metal lines.

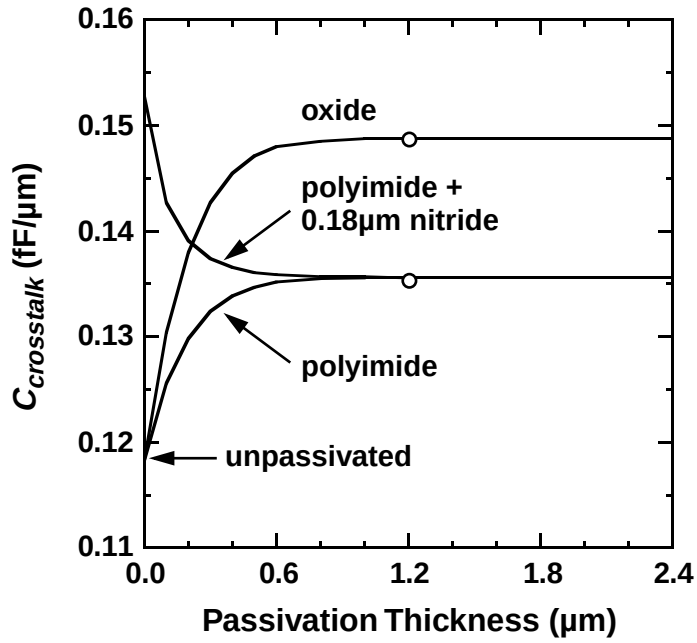


Figure 5-13 Simulated dependence of $C_{crosstalk}$ on passivation dielectric thickness. Minimum thickness for accurate extraction is 1.0 µm. The metal line spacing is 0.5 µm.

5.2.6 Extraction of In-plane Dielectric Constant

After extraction of κ_{top}, MEDICI™ simulations were performed to decouple the effect of $\kappa_{\perp}$ and extract $\kappa_{\parallel}$. As illustrated in Figure 5-14, the fringing fields traverse in both out-of-plane and in-plane directions. Given a fixed $\kappa_{\perp}$, the goal was to determine the $\kappa_{\parallel}$–$\kappa_{\perp}$ combination equivalent to the measured κ_{top}. This, in effect, would numerically solve the anisotropic Laplace's equation [Eq. (5-7)].

$$\kappa_{\parallel}\,\varepsilon_0\frac{\partial^2 V}{\partial x^2} + \kappa_{\perp}\varepsilon_0\frac{\partial^2 V}{\partial y^2} = 0 \qquad (5\text{-}7)$$

From planar capacitance measurements, $\kappa_{\perp}$ was found to be 2.6. This resulted in $\kappa_{\parallel}$ of 3.0, corresponding to an anisotropy of 15%.

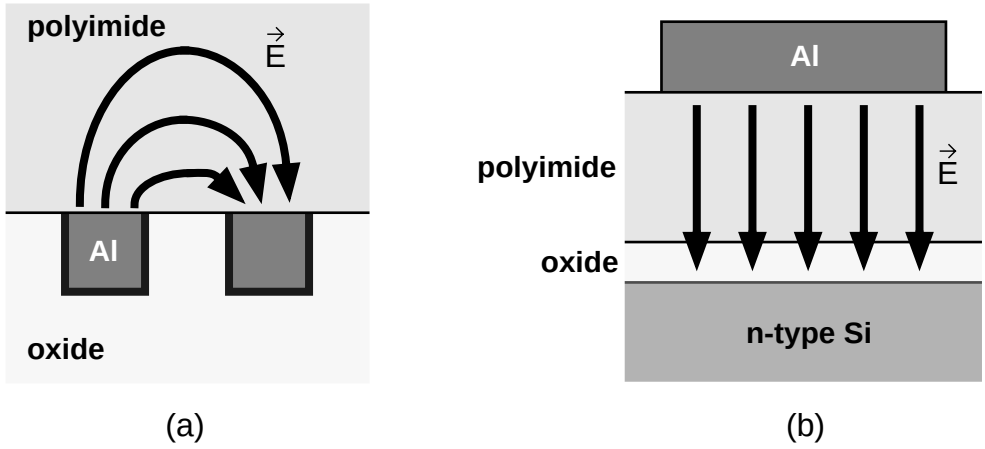


Figure 5-14 (a) Fringing fields traverse through both in-plane and out-of-plane directions. (b) Measurement of $\kappa_{\perp}$ from a parallel-plate capacitor with large area. A known $\kappa_{\perp}$ is required to extract $\kappa_{||}$ from κ_{top} in capacitance simulations.

The results are compared to published optical data [82] in Table 5-1.

Table 5-1: Anisotropy in FPI-136M Fluorinated Polyimide

Measurement	Frequency	$\kappa_{\perp}$	$\kappa_{||}$
crosstalk capacitance	1 kHz	2.6	3.0
prism coupler	475 THz (632 nm)	2.3	2.6

5.2.7 Measurement Issues

Two practical measurement considerations which impact the accuracy of $C_{crosstalk}$ and ultimately the accuracy of $\kappa_{||}$, are the effects of metal line and substrate resistances which are intrinsic to any interdigitated metal test structure. The parasitic resistances give rise to frequency dependences in $C_{crosstalk}$, since the vector impedance meter approximates the distributed impedances of the test structure as lumped elements, in this case, a

series capacitor–resistor (C_{series}–R_{series}) combination. $C_{crosstalk}$ must therefore be measured at a sufficiently low frequency to alleviate the frequency dependences.

Recall that $C_{crosstalk}$ was measured at 1 kHz because at higher frequencies, the measured C_{series} would roll off owing to the large *serpentine* resistance, R_{serp}, in the *comb1*/*serpentine*/*comb2* structure. HSPICE™ circuit simulations were performed to verify this hypothesis [107]. The exact measurement configuration detailed in Section 5.2.3 was simulated. Illustrated in Figure 5-15, the *serpentine*/*comb* structure was modeled as a ladder network with R_{serp} distributed along the *serpentine* and $C_{crosstalk}$ distributed between *comb* and *serpentine*. The *comb* resistance was neglected since the length of the *comb* segments was insignificant compared to the *serpentine* length. The substrate was modeled as a conductive plane representing the Si surface, which was connected to the substrate contact at the wafer backside via a lumped substrate resistance, R_{sub}. Coupling between the metal lines and Si surface was modeled by distributed capacitances estimated from *C*–*V* measurements. Figure 5-16 demonstrates that as the number of distributed *RC*

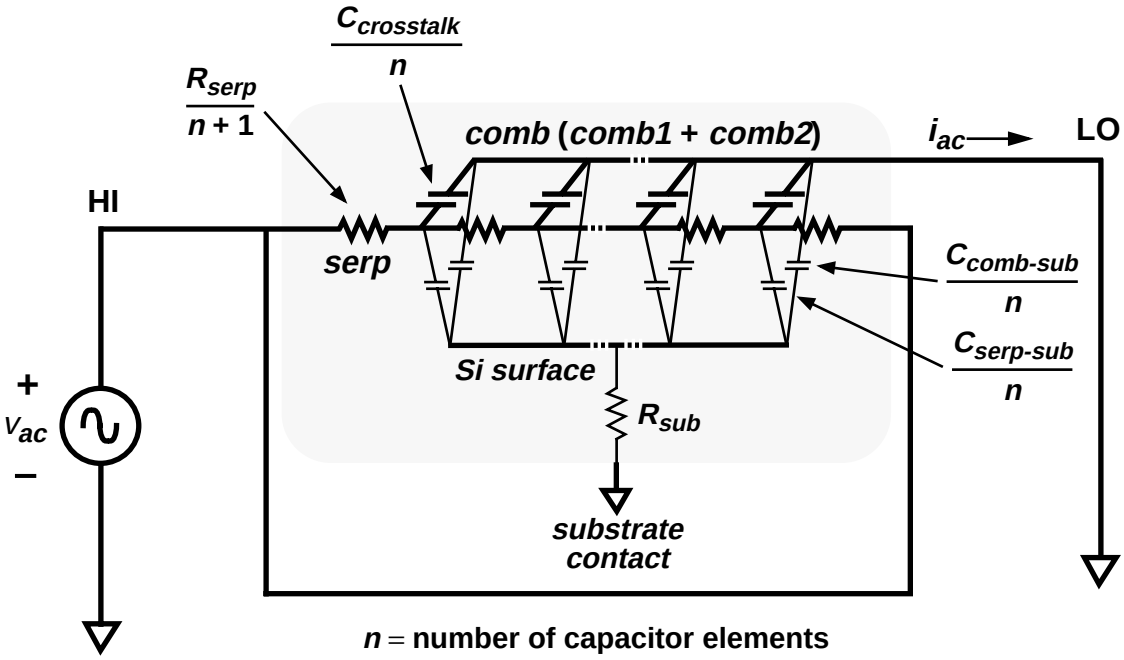


Figure 5-15 Distributed *RC* model of *comb1/serpentine/comb2* test structure.

elements increase, the simulated C_{series} approaches the measured C_{series} with excellent agreement. In this simulation, substrate effects were neglected by removing $C_{comb\text{-}sub}$, $C_{serp\text{-}sub}$, and R_{sub}. Hence, the observed rolloff in C_{series} is indeed attributed to the distribution of R_{serp} along the distributed $C_{crosstalk}$. For crosstalk measurements at higher frequencies, *comb1*/*comb2* is the more appropriate test structure.

Another frequency-limiting factor is R_{sub}. In the measurement configuration, the Si surface was assumed to be a grounded conductive plane. However, provided that R_{sub} is sufficiently large, the Si surface could establish a significant nonzero potential, being a floating intermediate node for capacitive coupling between *serpentine* and *comb.* The resulting increase in C_{series} is simulated for a range of R_{sub} values and illustrated in Figure 5-17. Simulations indicate that the effect of R_{sub}, estimated to be 150 Ω for the fabricated test structures, was negligible in the measurement at 1 kHz. It is worthy to note that a large R_{sub} could result from a poor backside contact or a depleted Si surface.

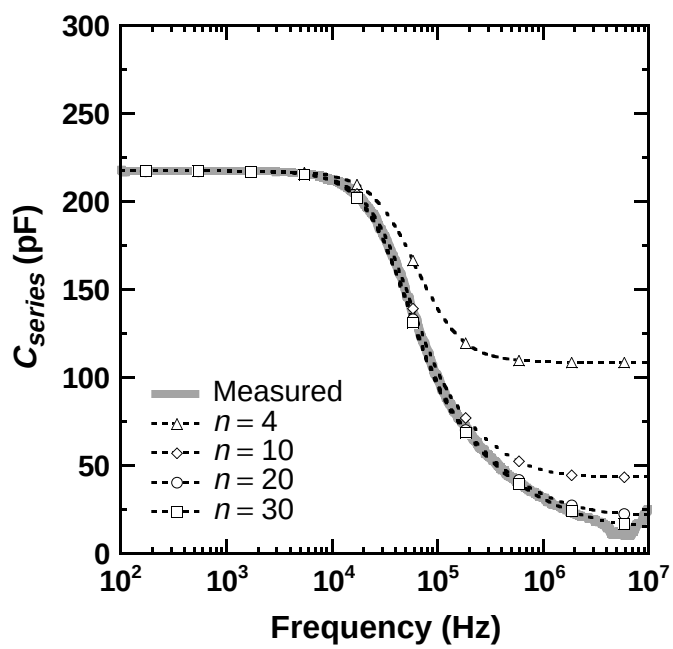


Figure 5-16 Simulations illustrating effect of number of distributed *RC* elements, *n*, on modeling crosstalk capacitance measurements of the unpassivated *comb1*/*serpentine*/*comb2* structure.

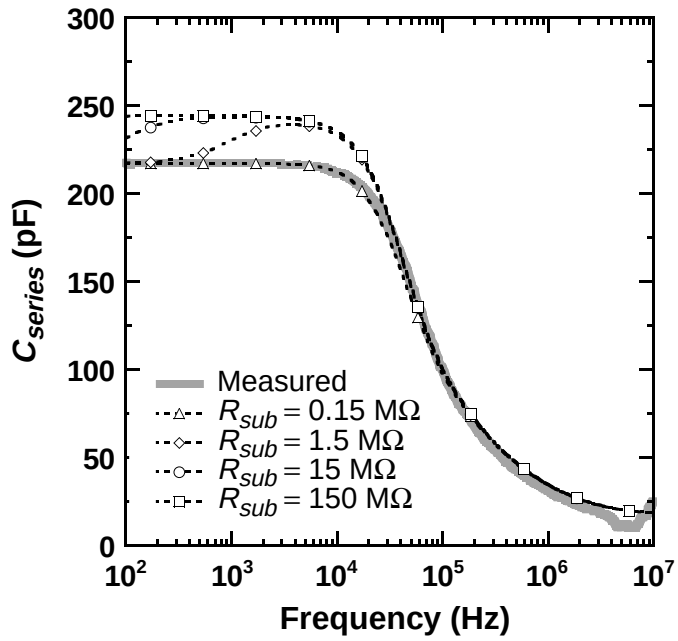


Figure 5-17 Simulations illustrating effect of substrate resistance, R_{sub}, on measured crosstalk capacitance of unpassivated lines.

5.3 Summary

This chapter presented a generic electrical technique to extract the in-plane dielectric constant, $\kappa_{||}$, of a blanket dielectric film for Damascene applications. The technique is based on measuring the fringe capacitance between interdigitated Damascene metal lines passivated by the dielectric film of interest. First, the effective dielectric constant of the passivating dielectric is obtained by interpolating the measured capacitance using reference structures passivated by two isotropic dielectrics with known dielectric constants. Following this extraction, a two-dimensional interconnect simulator is employed to decouple the effect of the out-of-plane dielectric constant, $\kappa_{\perp}$, in order to extract $\kappa_{||}$. The technique was demonstrated using fluorinated polyimide, with the reference dielectrics being air and oxide.

Chapter 6 Copper Drift in Dielectrics

Manufacturable integration of Cu interconnects with oxide requires an effective barrier technology. This added process complexity and cost to clad the Cu wires stem from the concern that copper can diffuse through oxide, especially in the presence of electric fields [46], [108]–[111]. Although thermal diffusion of Cu in oxide may be negligible at metallization process temperatures (≤ 450°C), positive Cu ions (Cu^+) drift rapidly through oxide at much lower temperatures. The electrical bias that assists the diffusion arises not only during operation of the integrated circuit but also during wafer processing where, for example, wafer charging may result from plasma etching [112].

The drift of Cu ions in dielectrics raises many reliability concerns. Cu^+, or any charge, in interlevel dielectrics shifts the threshold voltage of parasitic transistors in field regions with overlying interconnects, potentially resulting in poor device isolation. Extended penetration of Cu^+ has been shown to cause interlevel dielectric failure [110]. Moreover, the eventual migration of Cu^+ to the underlying Si substrate degrades carrier lifetime which leads to high junction leakage currents [111]. To identify the barrier requirements for integrating Cu with low-κ polymer dielectrics, the extent of Cu^+ penetration in these dielectrics must be determined. If these materials are inadequate dielectric

barriers against Cu^+ migration, complete barrier encapsulation of Damascene Cu interconnects will be required as depicted in Figure 6-1.

This chapter investigates the drift of Cu ions in low-κ polymer dielectrics. Cu^+ penetration into the dielectrics is accelerated by applying bias-temperature stress (BTS) to planar Cu/insulator/Si capacitors as illustrated in Figure 6-2. Typical stressing conditions are biases correponding to electric fields of 0.1–2.0 MV/cm at temperatures of 125–300°C. The resulting penetration is detected by capacitance–voltage (*C–V*) analysis and dielectric time-to-failure (*TTF*) measurements. In the industry, the *C–V* method is frequently employed to monitor trace mobile ions in gate oxides (Na^+ and K^+) in order to control the threshold voltage (V_T) of MOS transistors [113] while *TTF* measurements are performed to determine the reliability of gate oxides [114]. Principles of both techniques are first reviewed and then extended in a detailed investigation of Cu drift in six low-κ polymers, namely parylene-F, benzocyclobutene, fluorinated polyimide, an aromatic hydrocarbon, and two varieties of polyarylene ether.

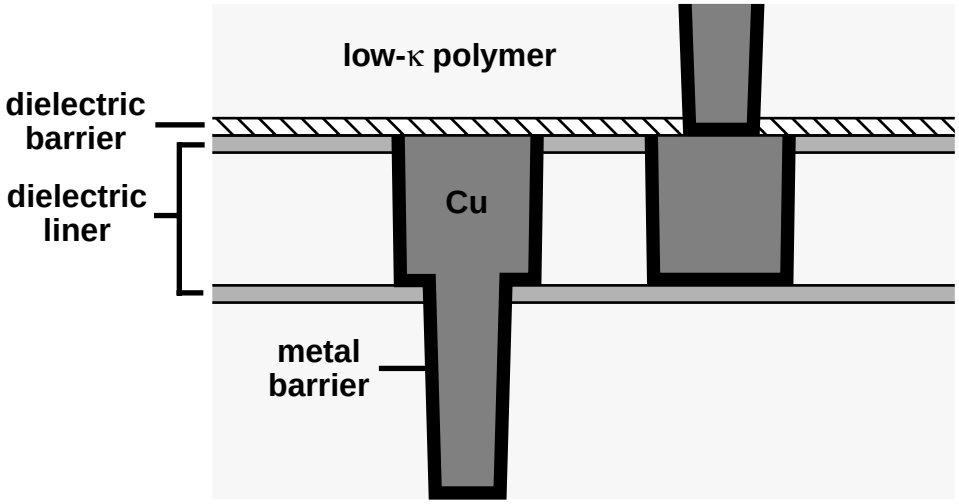


Figure 6-1 Cross-section of potential Cu and low-κ polymer dielectric integration scheme illustrating encapsulation of copper interconnects with metal and dielectric barriers.

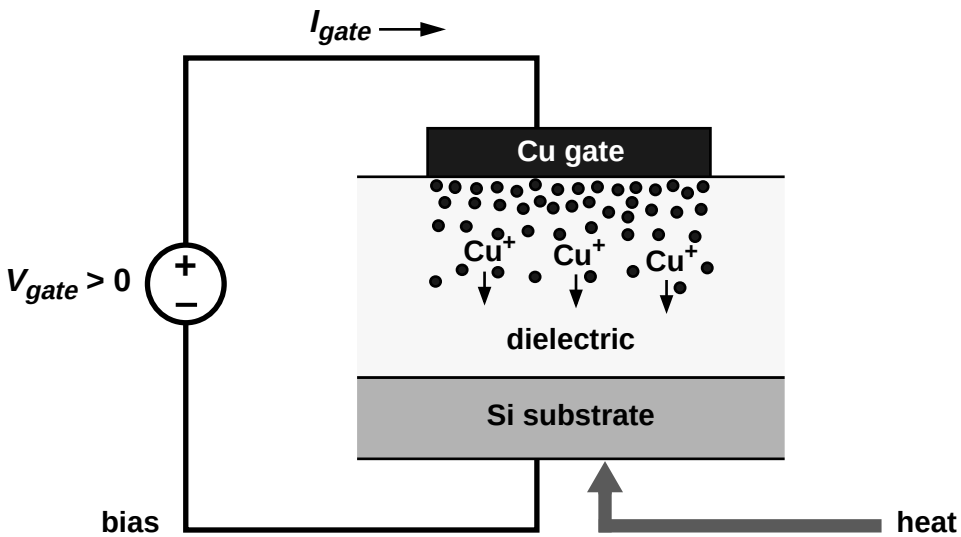


Figure 6-2 Bias-temperature stressing of Cu-insulator-Si capacitors to accelerate penetration of Cu^+ ions into a dielectric.

6.1 Detection of Copper Drift

Electrical techniques are employed to detect penetration of Cu ions resulting from BTS. They are applied to examine Cu drift in oxide and oxynitride, and provide the foundation for similar experiments involving the low-κ polymer dielectrics.

6.1.1 Capacitance–Voltage Analysis

The high-frequency *C–V* measurement, typically performed at 100 kHz to 1 MHz, is capable of quantifying dielectric charges in metal-insulator-semiconductor (MIS) systems with high sensitivity. Dielectric bulk and interface charges affect surface inversion in the semiconductor substrate and thus modify the *C–V* behavior. The room-temperature *C–V* characteristic is generally affected by BTS in two ways.

Introducing charge into the dielectric bulk causes a lateral shift in the *C–V* trace as quantified by the flatband voltage shift, ΔV_{FB}. V_{FB} is the gate bias at which no charge

resides in the Si substrate and marks the transition between accumulation and depletion of carriers at the Si surface. Uncompensated positive charge in the dielectric, Cu^+ for example, makes V_{FB} more negative because it induces negative image charge in the Si surface. To cancel this image charge and restore the flatband condition, negative charge must be added on the gate. Hence, V_{FB} becomes increasingly negative as more positive charge is introduced into the dielectric. Similarly, as more negative charge is introduced into the dielectric, V_{FB} becomes increasingly positive. As shown in Figure 6-3, for a distribution of charge in the dielectric (oxide on n-Si for example), the resulting ΔV_{FB}, is given by Eq. (6-1) [115],

$$\Delta V_{FB} = -\frac{1}{\varepsilon_{ox}} \int_0^{x_{ox}} x\ \rho(x)\, dx \tag{6-1}$$

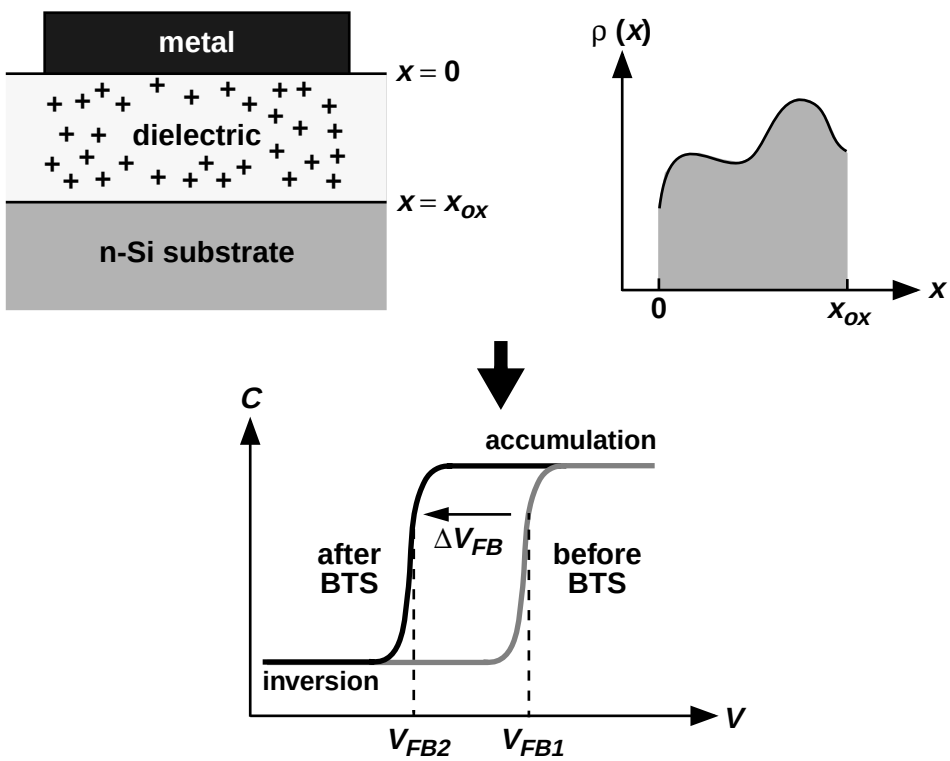


Figure 6-3 Effect of trapped charges in the dielectric on the high-frequency *C–V* behavior.

where ε_{ox} is the dielectric permittivity and $\rho(x)$, $0 \le x \le x_{ox}$, is the volumetric charge density. Charge near the gate interface ($x \approx 0$) has little effect on ΔV_{FB} whereas the same charge near the substrate interface ($x \approx x_{ox}$) has maximum effect on ΔV_{FB} . Under BTS, Cu penetrate into oxide as uncompensated positive charge in the dielectric. The magnitude of ΔV_{FB} reflects the quantity of Cu^+ that has drifted into the dielectric.

Another change in the *C–V* characteristic that is sometimes observed is *C–V* spread-out illustrated in Figure 6-4 [116]. This gradual transition between inversion and accumulation is typically the result of charge traps generated at the substrate interface from high-field stressing. When the n-Si surface shifts from inversion to accumulation, gate charge that would otherwise be balanced by depleted bulk Si charge (exposed donor atoms) is balanced by charge populating the interface traps. Hence, additional gate charge is

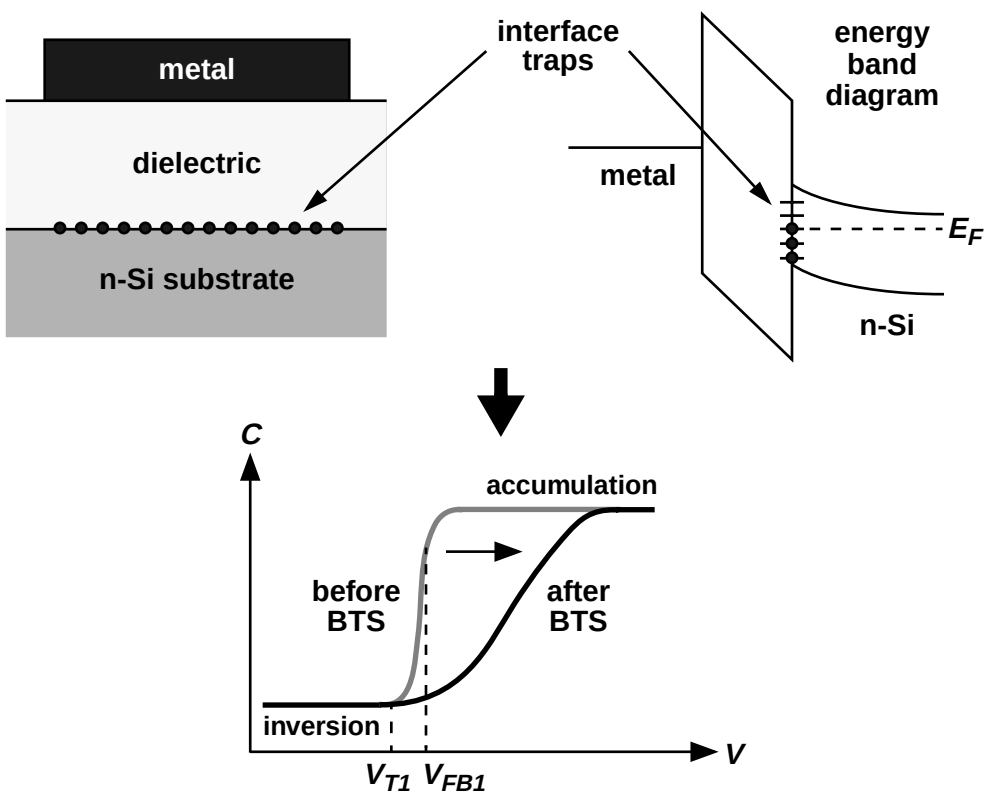


Figure 6-4 Effect of interface charge traps at the Si interface on the high-frequency *C–V* behavior. Electron traps are assumed.

required to move the Si surface Fermi level, E_F, through the interface states and a larger voltage span is thus needed for the transition. *C–V* spreadout need not be generated by BTS and is often an indication of a poor quality or damaged Si interface that results from processing. Both V_{FB} and V_T may change depending on the substrate type and whether the interface traps capture electrons or holes. A less common cause of *C–V* spreadout is gross nonuniform charging of the dielectric bulk across the capacitor area [117]. In this scenario, the capacitor can be viewed as a summation of many small capacitors in parallel that independently do not exhibit spreadout but collectively span a broad range of ΔV_{FB}'s.

The *C–V* technique is now applied to evaluate Cu drift in Si oxide and oxynitride. As an example, consider the drift of Cu^+ in a Cu-gate PECVD oxide capacitor shown in Figure 6-5. The thermal oxide layer provides a good dielectric-to-substrate interface with low interface trap density (D_{it}) and fixed interface charge (Q_f) for well-behaved *C–V* characteristics while the bottom Al layer provides a good substrate contact. To confidently interpret changes or instabilities in *C–V* behavior resulting from BTS, it is important to ensure that these changes are indeed due to migration of Cu^+. Consequently, a proper analysis additionally requires that capacitors with Al electrodes be tested as an experimental control. Al does not drift into oxide since it forms a stable interface with oxide, specifically reducing the SiO_2 leaving free Si and Al_2O_3 to form a stable Al–Al_2O_3–Si–SiO_2

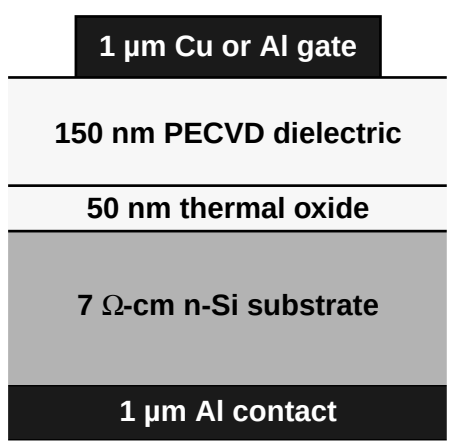


Figure 6-5 Capacitor structure for evaluating Cu drift in PECVD dielectric: oxide ($\kappa = 4.1$) and oxynitride ($\kappa = 5.1$). Gate area is 1 mm^2.

interface about 1 nm thick [118], [119]. With Al control capacitors, comparisons between the Al and Cu capacitor BTS results can more readily differentiate between metal-related *C–V* instabilities, such as Cu^+ migration, and dielectric-related instabilities. Examples of BTS dielectric-related instabilities include electron trapping in the dielectric bulk or interface [115], [120], polarization of dielectric interfaces [121], and movement of trace alkali impurities introduced during dielectric deposition. These phenomena are unrelated to Cu^+ migration and should they occur, they will be present regardless of the gate electrode metal.

Typical 20°C high-frequency *C–V* results after BTS of PECVD oxide are shown in Figure 6-6. Thermal stressing alone does not affect the *C–V* behavior. However, for the Cu capacitors, a positive gate voltage (V_{gate}) shifts the *C–V* curve horizontally in the negative V_{gate} direction; the longer the applied stress is maintained, the larger the shift. The *C–V* characteristics of corresponding Al control capacitors do not change after BTS. Hence, the observed instabilities in the Cu-gate capacitors are attributed to positive charge

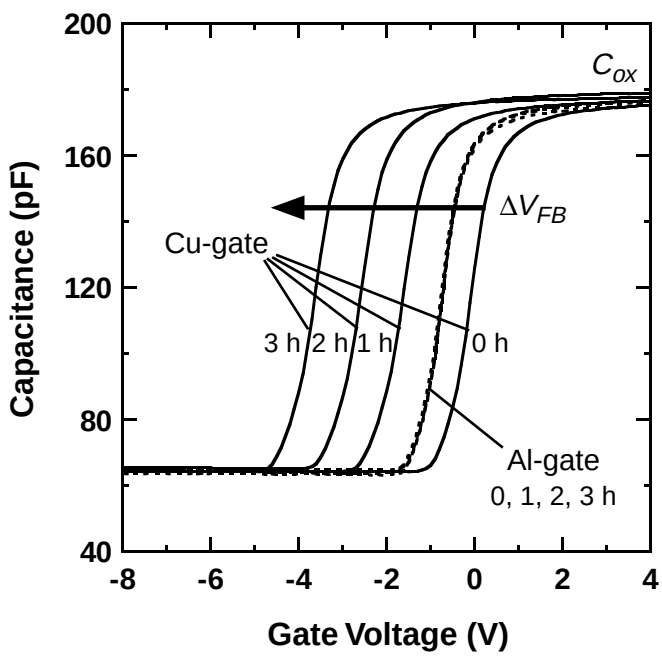


Figure 6-6 *C–V* characteristics of PECVD oxide capacitors at 20°C after stressing under +20 V gate bias (+1.0 MV/cm) at 175°C for 0, 1, 2, and 3 hours.

injected by the Cu gate (Cu^+) as opposed to alkali ion impurities or other trapped or induced charge in the dielectric. In addition, the absence of *C–V* spreadout indicates that interface traps can be neglected. The Cu ion polarity is verified by considering BTS results under negative gate bias. Although BTS at -20 V introduces small quantities of positive charge in the dielectric, the similar *C–V* shifts in both Cu- and Al-gate capacitors confirm that a dielectric-related instability is observed [122] and that the mobile Cu ions are positively charged. See Figure 6-7. The negative-bias temperature instability is believed to originate from hydrogen-related instabilities in deposited oxides [123] and can be overcome with a forming gas anneal.

The amount of Cu^+ charge drifted into the dielectric can be estimated from the measured ΔV_{FB}. Assuming that the Cu ions drift to the thermal-oxide/Si interface, the Cu^+ concentration per unit area, $[Cu^+]$, is given by Eq. (6-2).

$$[Cu^+] = -\frac{C_{ox}}{q}(\Delta V_{FB}) \tag{6-2}$$

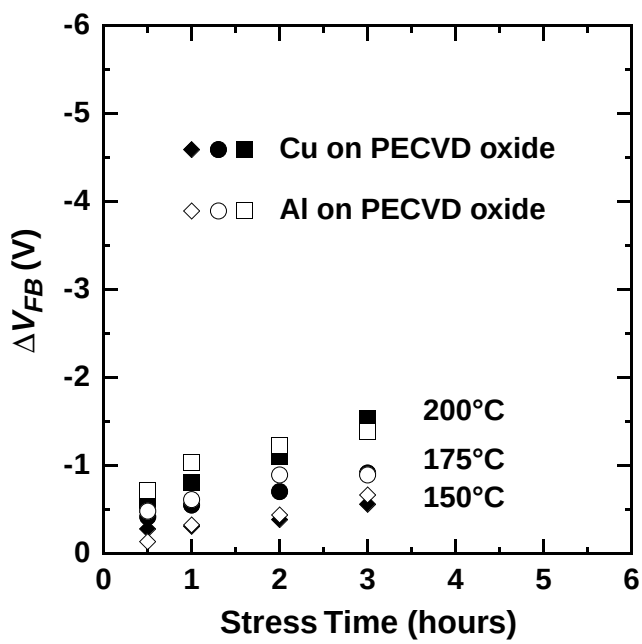


Figure 6-7 Negative bias-temperature instabilities in PECVD oxide capacitors stressed under -20 V gate bias (-1.0 MV/cm).

C_{ox} is the dielectric stack capacitance per unit area and q is the electronic charge. Only singly ionized Cu ions (Cu^+) are considered since the diffusivity and solid solubility of Cu^{2+} in oxide are insignificant compared to that of Cu^+ in oxide [124]. The Cu^+ drift rate in the dielectrics and its activation energy can be obtained by tracking ΔV_{FB} as functions of time and temperature. As an illustration, the ΔV_{FB} transients for PECVD oxynitride are shown in Figure 6-8. Since oxynitride is a much better Cu drift barrier than oxide, higher stress temperatures are required in order to observe similar ΔV_{FB}'s seen in Figure 6-6. The Cu^+ drift rate, DR_0, calculated from Eq. (6-3), can finally be extrapolated down to typical circuit operating conditions (85–120°C) to assess the magnitude of the reliability concern.

$$DR_0 = \frac{d}{dt}[Cu^+] = -\frac{C_{ox}}{q}\frac{d}{dt}(\Delta V_{FB}) \tag{6-3}$$

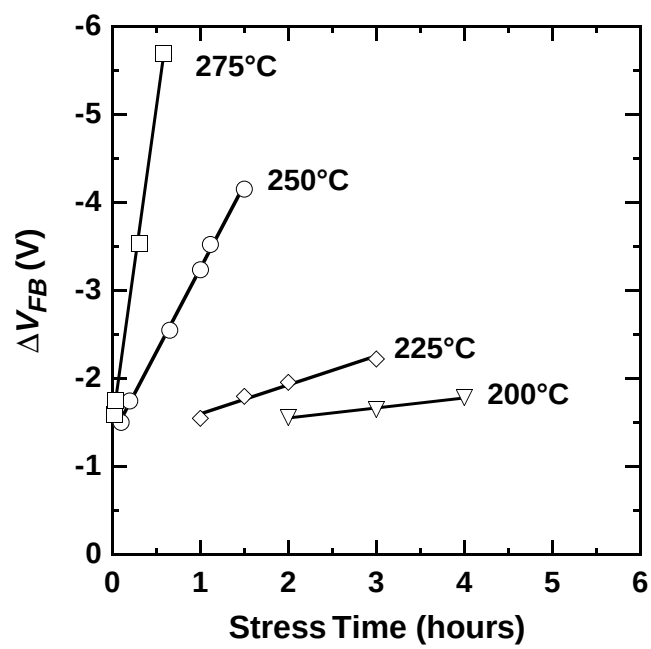


Figure 6-8 ΔV_{FB} as a function of stress time and temperature for PECVD oxynitride capacitors stressed at +20 V (+1.0 MV/cm).

The initial rapid change in ΔV_{FB} is believed to be due to trace alkali impurities originating from the Cu electrode during metal deposition. The effect of these faster moving alkali ions saturates when the limited ions accumulate at the substrate interface, leaving subsequent increase in ΔV_{FB} to be due to the slower Cu ions. For example, the best-fit lines clearly extrapolate back to a common ΔV_{FB}-intercept of about -1.3 V. However, since the drift rate is obtained from a slope, this effect need not be considered.

The presence of Cu in the dielectric was confirmed by secondary ion mass spectrometry (SIMS) [125] with results shown in Figure 6-9. Consistent with the observed ΔV_{FB}'s, the SIMS profiles show a large quantity of Cu reaching the thermal-oxide/substrate interface in the case of oxide, with very little Cu in the case of oxynitride. This observation of Cu accumulating near the substrate interface validates Eq. (6-2) as a reasonable estimate of $[Cu^+]$.

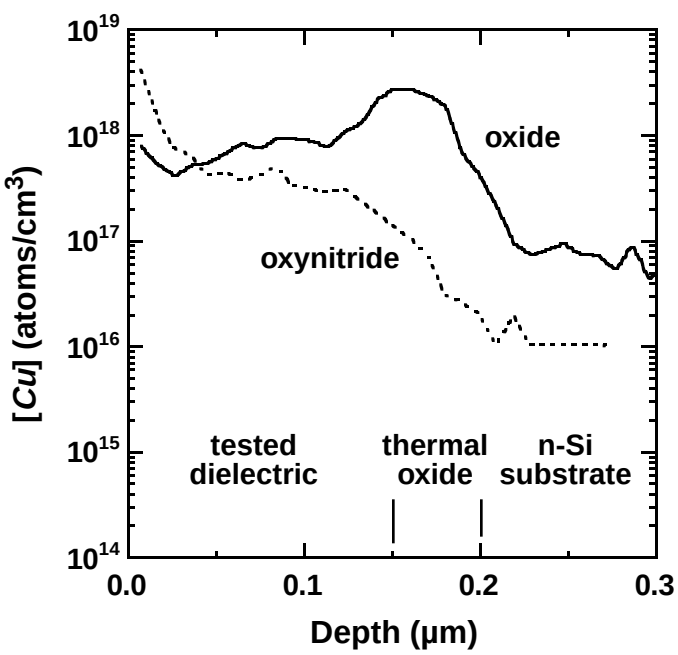


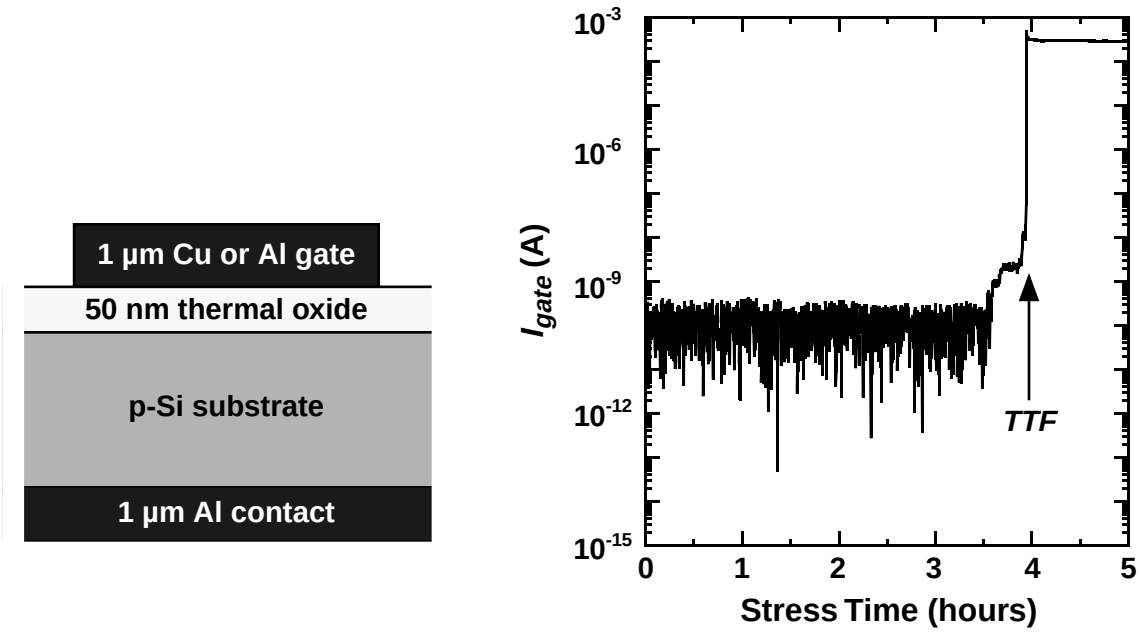
Figure 6-9 SIMS analysis of Cu capacitors with oxide and oxynitride dielectrics. Capacitors were stressed at +20 V (+1.0 MV/cm) and 250°C for one hour. The Cu gates were stripped by wet-etching prior to analysis.

6.1.2 Dielectric Time-to-failure Measurement

An alternative technique to detect migration of Cu^+ ions is based on time-dependent dielectric breakdown (TDDB) [114]. TDDB results from prolonged high-field stressing of a dielectric until the dielectric irreversibly loses its insulating property. The applied stress transports charges through the dielectric, via Fowler-Nordheim tunneling, which spawn regions of local damage that propagate through the dielectric network. The damage is physically manifested as broken bonds that trap charges in the dielectric bulk and at the dielectric interfaces [126]. Increased charging in the dielectric results in regions of electric field enhancement which further accelerate the damage creation process. Breakdown occurs after passage of some critical charge-to-breakdown, Q_{bd}.

Extended penetration of Cu^+ in a dielectric under constant voltage stress will also evetually lead to dielectric failure [110]. This phenomenon was investigated at Texas Instruments to evaluate Cu drift in thermal oxide. Figure 6-10 illustrates a typical constant voltage stress measurement of thermal oxide capacitors with Cu electrodes. These capacitors fail after some time-to-failure, *TTF*, marked by a sudden dramatic increase in dielectric current. It is believed that the penetration of uncompensated Cu^+ ions into the dielectric raises the electric field near the Si substrate [127], [128]. The increasing electric field will transport more electrons from the Si substrate through the dielectric until failure occurs. Hence, *TTF* reflects the kinetics of Cu^+ penetration in the dielectric such that longer failure times indicate lower drift rates of Cu ions.

Attributing capacitor failure to Cu^+ migration and not to intrinsic dielectric wearout requires examination of experimental controls. Consider that the *TTF* of a Cu capacitor stressed at +15 V, which corresponds to a field of +3.0 MV/cm, typically fails in 5 minutes at 200°C. When the polarity is reversed, failure is not observed even after 24 hours. In addition, in capacitors with Al electrodes, failure is not observed after a 24-hour period under +15-V stress. These observations are consistent with *C–V* results that only positive Cu ions drift.



(a) (b)

Figure 6-10 (a) Cu-gate thermal oxide capacitors. (b) Typical I_{gate} transient of capacitor stressed to breakdown at 200°C under +10 V bias (+2 MV/cm). Gate area is 2 mm^2.

To extrapolate *TTF* down to circuit operating conditions, *TTF* must be obtained for a range of temperatures and biases. Results for the thermal oxide capacitors are shown in Figure 6-11. Compared to the *C–V* analysis, the dielectric *TTF* measurement is particularly suited for extrapolating dielectric reliability, such as confirming if a 10-year lifetime criterion can be met. However, the technique is prone to a few key weaknesses. First, since dielectric failure is a stochastic event that is linked to defects, the measurement is very sensitive to dielectric quality which prompts the need to collect statistics. Also, the validity of *TTF* extrapolation may be questionable since these tests are performed under fairly high fields, typically over an order of magnitude higher than in actual operation (≤0.1 MV/cm), such that observed *TTF*'s are not unreasonably long. On the contrary, *C–V* measurements are very reproducible and provide more averaged behaviors. Nevertheless, dielectric *TTF* is frequently employed as a reliability metric in evaluating the Cu drift

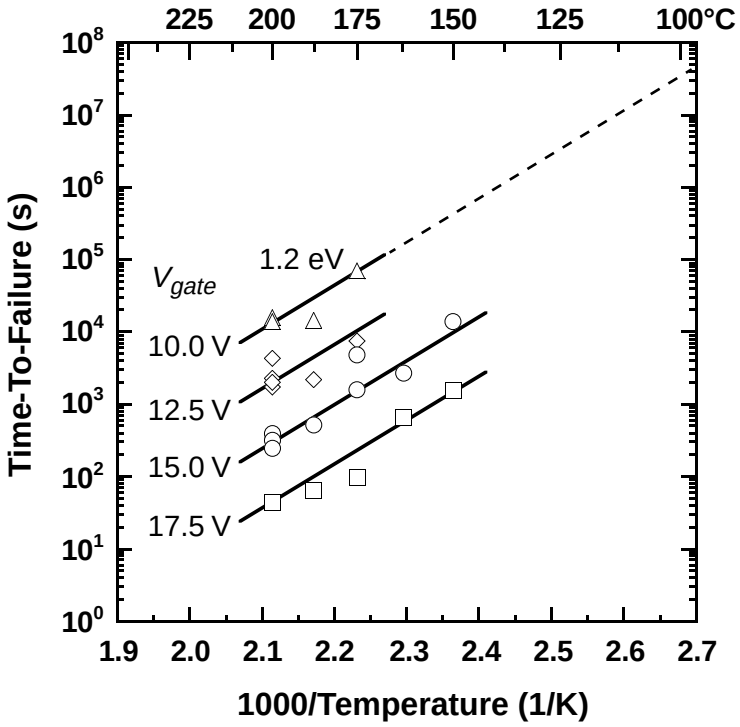


Figure 6-11 Arrhenius plot of time-to-failure of Cu-gate thermal oxide capacitors stressed at various gate biases corresponding to 2.0–3.5 MV/cm.

property of dielectrics as well as effectiveness of metal diffusion barriers inserted between the dielectric and Cu electrode [129].

6.2 Copper Drift in Low-Permittivity Polymers

This section extends the electrical techniques developed in the previous section to examine the drift of Cu ions in low-κ polymer dielectrics. It contains a thorough discussion of the development, fabrication, and measurement of a capacitor test structure suitable for the evaluation. Emphasis is placed on experimental difficulties associated with processing and testing low-κ polymers and on the solutions employed to overcome them. These issues include ambient moisture absorption [87], poor interface quality with metals [130]–[133] and Si [134], and dielectric charge instabilities [135]–[138].

The primary method of evaluation is *C–V* analysis before and after BTS. For additional insight into the Cu^+ drift process, these findings are complemented by current-time (*I–t*), current-voltage (*I–V*), and dielectric time-to-failure (*TTF*) measurements during BTS, enabling a physical model to be formulated to explain the kinetics of Cu^+ penetration.

6.2.1 Fabrication of Test Structures

Cu and Al MIS capacitors, illustrated in Figure 6-12, were fabricated with six industrially relevant low-κ polymers, listed in Table 6-1, belonging to five families of carbon-based polymers: polyarylene ether, aromatic hydrocarbon, fluorinated polyimide, benzocyclobutene, and parylene-F. Once again, since Al does not drift into oxide, Al capacitors are fabricated as experimental controls which, when compared to the Cu capacitor results, differentiate between metal- and dielectric-related instabilities.

The processing sequence is outlined below. Refer to the Appendix for a complete process flow. A thin thermal oxide layer was first grown on (100) n-type Si wafers in a dry ambient at 1000°C to form a stable, high-quality interface with the Si substrate. N-type

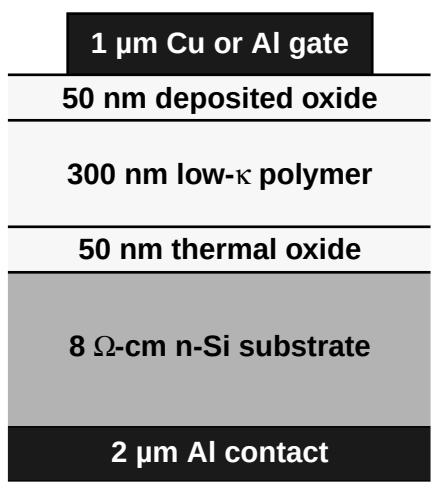


Figure 6-12 Oxide-sandwiched low-κ polymer capacitor for evaluating Cu drift in low-κ polymer. Gate area is 1 mm^2.

Table 6-1: Low-κ Polymer Dielectrics for Evaluation of Copper Drift

Low-κ Polymer	$\kappa_{\perp}$	Deposition Method	T_{cure} (ambient)
polyarylene ether Schumacher PAE-2 [77]	2.8	spin-on deposition	425°C (air)
polyarylene ether Asahi Chemical ALCAP-E [78]	2.8	spin-on deposition	400°C (N_2)
aromatic hydrocarbon Dow Chemical SiLK™ polymer [79]	2.7	spin-on deposition	450°C (N_2)
fluorinated polyimide DuPont FPI-136M [82]	2.6	spin-on deposition	375°C (N_2)
benzocyclobutene Dow Chemical BCB [83]	2.6	spin-on deposition	350°C (N_2)
parylene-F Novellus Systems AF-4 [85]	2.4	chemical vapor deposition	350°C (vacuum)

substrates were selected so that the Si surface would be in accumulation under a positive gate bias during BTS. Next, 300 nm of low-κ polymer was deposited over the thermal oxide. PAE-2 was cured in air (20% O_2), AF-4 was annealed in vacuum, whereas the other polymers were cured in N_2. Specific polymer processing conditions are detailed in the Appendix and in [77]–[79], [82], [83], [85]. A 50-nm oxide cap was subsequently deposited at 300°C after an *in situ* 300°C bake to degas residual moisture in the polymer. A SiH_4/N_2O chemistry instead of a SiH_4/O_2 chemistry was chosen to prevent the polymer surfaces from oxidizing during the deposition. After the oxide cap deposition, 1 µm of either pure Al or Cu was sputtered, patterned, and wet-etched to define gate electrodes with an area of 1 mm^2. Prior to metal depostion, the wafers underwent an *in situ* bake to remove moisture in the dielectric that could later cause metal blistering during testing. Also, a relatively thick gate was deposited as a precautionary measure to prevent test probes from penetrating the thin oxide cap and the underlying soft polymer film [139]. After the backside thermal oxide was stripped, 2 µm of pure Al was sputtered on the wafer backside to form a good substrate contact. The wafers were finally annealed in a forming

gas ambient at 350°C for one hour. Demonstrated in Figure 6-13, this final procedure restores the quality of the thermal-oxide/Si interface after plasma exposure during dielectric deposition and gate sputtering. The thermal cycle also causes the backside Al to alloy with Si for a better contact.

A salient feature of this capacitor structure is the pair of thin oxide layers that sandwich the low-κ polymer. The oxide layers overcome interface-related charge instabilities while allowing movement of Cu^+ under electrical bias. To be demonstrated later, polymers in direct contact with either the gate metal or Si substrate are prone to injection of electrons and holes across either interface. These interface-related instabilities are unrelated to Cu^+ drift and complicate the interpretation of results since the *C–V* technique cannot differentiate the different types of charges. The deposited oxide liner also alleviates Cu/polymer interface quality issues such as poor adhesion, thermal diffusion of Cu into the polymer, and Cu clustering in the polymer during metallization [130]–[133].

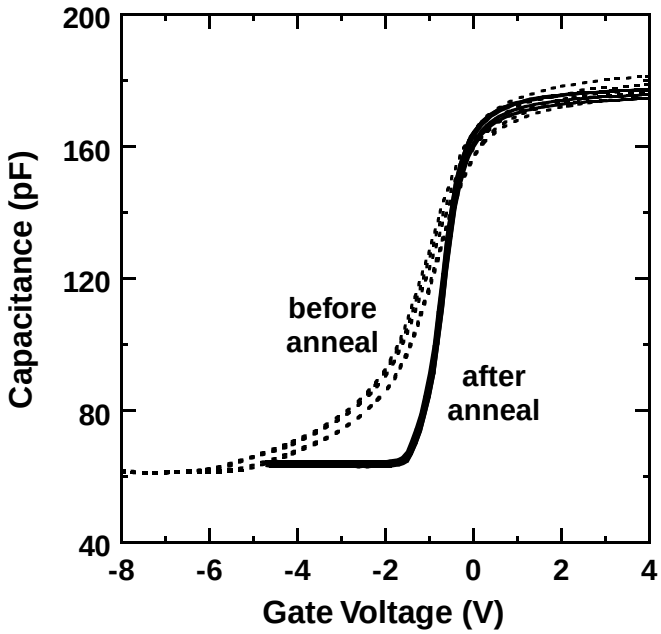


Figure 6-13 Effect of forming gas anneal at 350°C for one hour on *C–V* characteristics. PECVD oxide capacitors with Al electrodes are used for the illustration.

6.2.2 Electrical Testing

The electrical test setup, illustrated in Figure 6-14, consists of a probe station situated inside a sealed plexiglas™ enclosure which is continuously purged with N_2 to displace O_2 and moisture. The grounded probe station is furnished with an electrically isolated, water-cooled thermal chuck capable of quenching from 300°C to 50°C within one minute. The plexiglas™ box is surrounded by a lightproof metal enclosure which is also grounded to minimize electrical noise [140], resulting in probe tip leakage currents of less than 10 fA. Capacitor samples are vacuum-mounted onto the thermal chuck which serves as the connection to the sample substrates. Multiple capacitor gate electrodes are contacted by manual probers which are connected to the test instruments via low-leakage triaxial connections. The bias during BTS is provided by a HP4156A precision semiconductor parameter analyzer while the room-temperature *C–V* characteristic is measured with a HP4275A vector impedance meter.

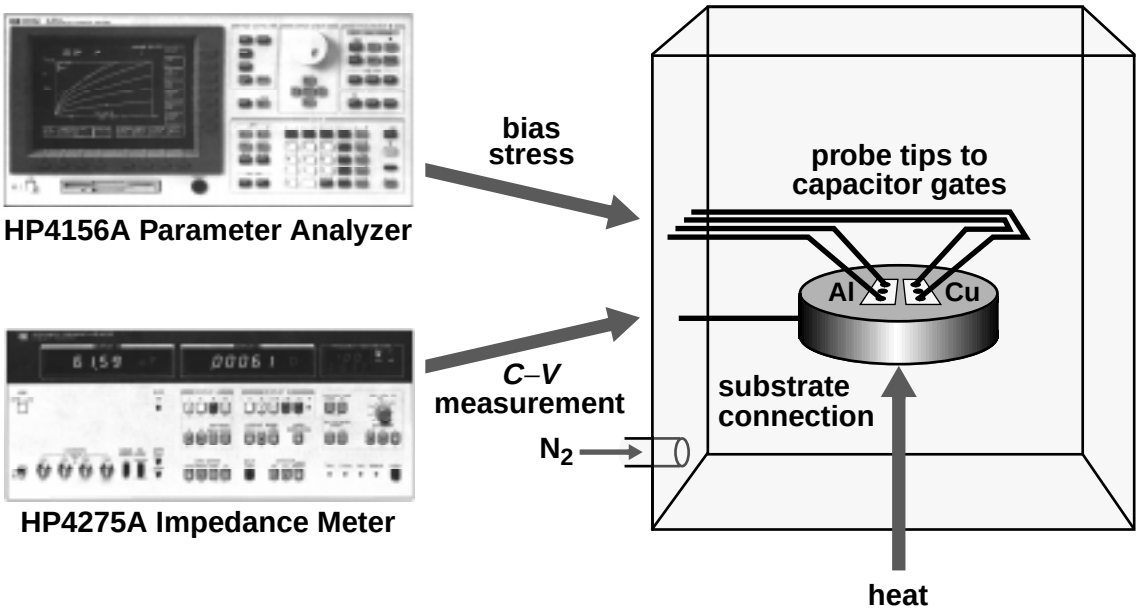


Figure 6-14 Experimental setup for electrical testing. To prevent moisture uptake in the polymer, all measurements and stressing were conducted without breaking the N_2 ambient.

All BTS experiments and *C–V* measurements are conducted without breaking the N_2 ambient. This ensures that the exposed Cu electrodes do not oxidize during heating and that the polymer films do not take up moisture throughout the testing sequence. As demonstrated in Figure 6-15, ambient moisture can readily be absorbed by a low-κ polymer film to increase polarization in the dielectric and give rise to anomalous *C–V* hysteresis [141] and increased capacitance [142]. For this reason, the capacitors are annealed at 200°C for 12 hours after being loaded into the test enclosure to dehydrate the low-κ polymer prior to any measurement or stressing.

Cu and correponding Al capacitors concurrently undergo BTS at 150–275°C with constant dc gate biases, V_{gate}, of 0–60 V corresponding to initial electric fields of 0.0–1.5 MV/cm in the polymer. Samples are heated to the test temperature and bias is subse-

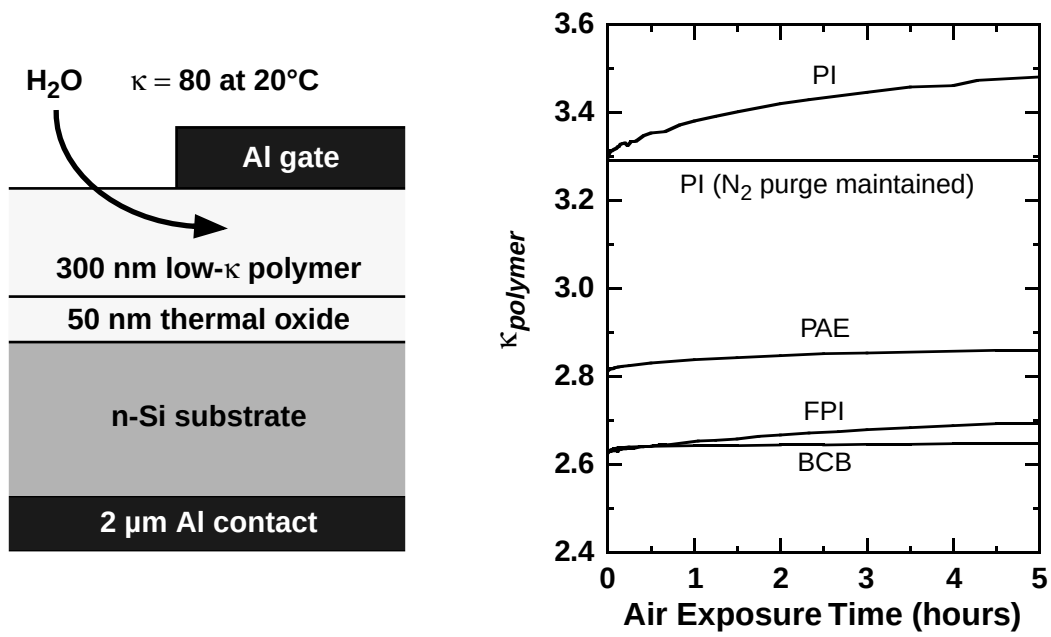


Figure 6-15 $\kappa_{polymer}$ transient demonstrating moisture uptake in low-κ polymer after exposure to 40% RH air at 20°C. Prior to exposure, the capacitors were heated to 200°C. PI is abbreviated for DuPont PI-2556 PMDA-ODA (pyromellitic dianhydride — oxydianiline) polyimide.

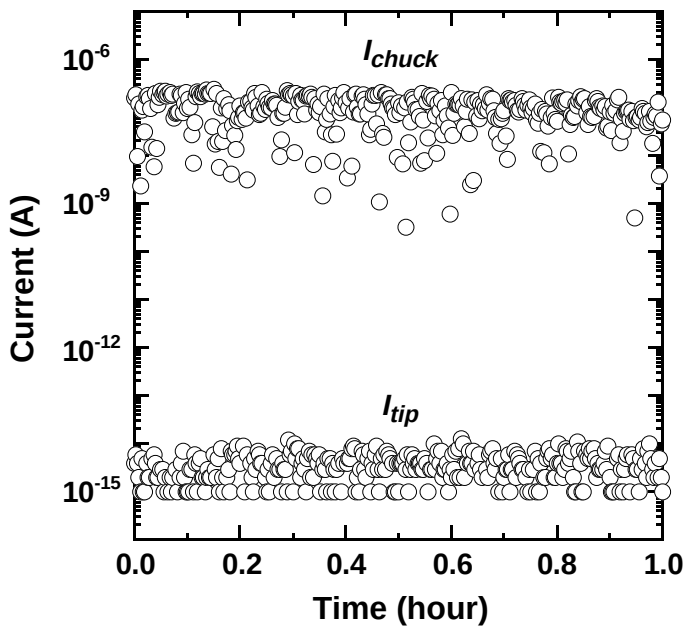


Figure 6-16 Leakage current characteristics of raised probe tips (I_{tip}) and hot chuck (I_{chuck}) in the N_2-purged probe station. The hot chuck was maintained at 300°C during the measurement.

quently applied for durations ranging from a few minutes to many hours. The gate current, I_{gate}, is monitored during BTS. The substrate current, however, is too noisy to be measured due to the chuck heater. See Figure 6-16. When the stress period expires, the capacitors are immediately quenched to room temperature to prevent backdrift of Cu^+ ions. The probe tips are raised during cooling to prevent damage to the polymer.

High frequency *C–V* sweeps from inversion to accumulation are obtained at 20°C before and after stressing. Typically, V_{gate} is swept from -35 V to +35 V in 1.0 minute using a 1-MHz sinusoid with an amplitude of 0.1 V. The primary measurement issue is electrical noise coupled from the chuck heater element and its power supply circuitry which interferes with the impedance meter signal. To alleviate this problem, the heater element is physically disconnected from its power supply during *C–V* sweeps.

6.2.3 Interface Instabilities

Interface-related charge instabilities occur when the low-κ polymer is in direct contact with either the gate metal or Si substrate. Because the *C–V* technique is very sensitive to any types of charges in the dielectric and at the interfaces, it is imperative that the test structure used for evaluation of Cu drift does not allow motion of charges other than Cu^+. Otherwise, it could become impossible to interpret the measurement results. An understanding of these interface issues is important in order to develop a suitable test structure.

To demonstrate these instabilities at the polymer/Si interface, virgin Al/oxide/polymer/n-Si capacitors are held at V_{gate} of ±35 V, which corresponds to an electric field of approximately ±0.9 MV/cm, for various durations before V_{gate} is swept to obtain the *C–V*. See Figure 6-17. Since Al forms an electrically stable interface with oxide, the deposited

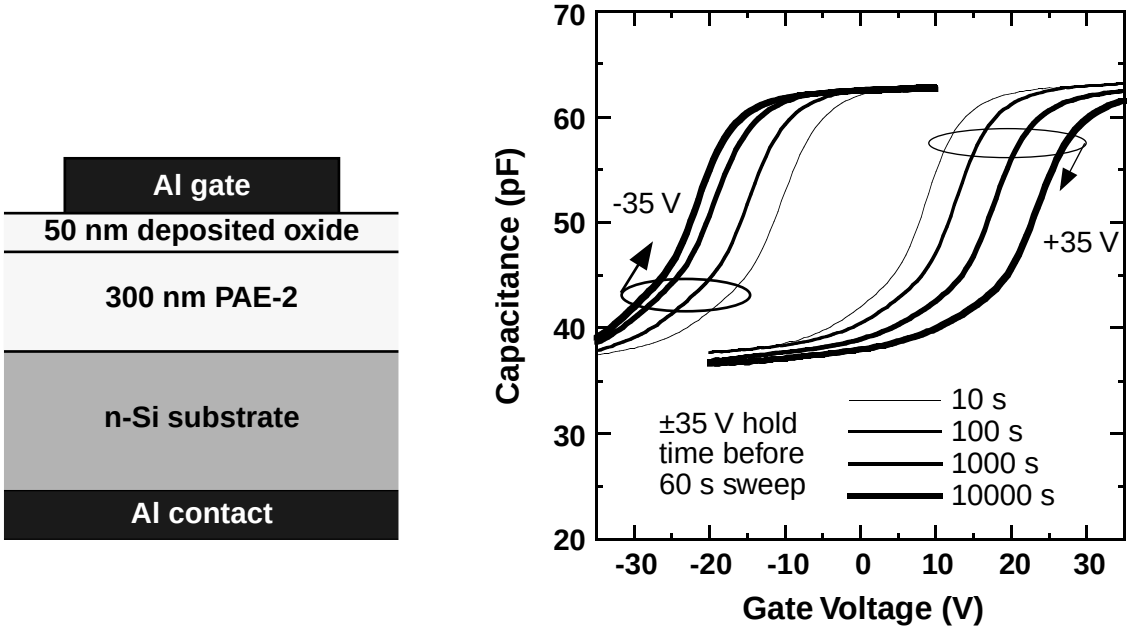


Figure 6-17 *C–V* characteristics demonstrating interface-related instabilities at the polymer/Si interface. Virgin capacitors were stressed at ±35V and 20°C for various durations preceding the *C–V* sweeps.

oxide layer electrically insulates the polymer from the Al gate, thus allowing the polymer/Si interface to be examined. The resulting *C–V* shifts prove that holding V_{gate} at -35 V introduces positive charge in the dielectric while holding V_{gate} at +35 V introduces negative charge; the longer the hold time, the larger the shift. The shifts correspond to charge densities of 10^{11}–10^{12} cm^{-2}. Since these instabilities occur at room temperature, it is believed that electrons and holes injected from the Si substrate are responsible for the phenomenon. From the spreadout between accumulation and inversion, the *C–V* characteristics also indicate that the Si surface is poorly passivated by the polymer and has a high density of interface traps (~10^{12} cm^{-2}). As an experimental control, the same experiment was performed on Al/oxide/n-Si capacitors. The absence of instabilities in Figure 6-18 confirms that as expected, both Al/oxide and oxide/Si interfaces are stable.

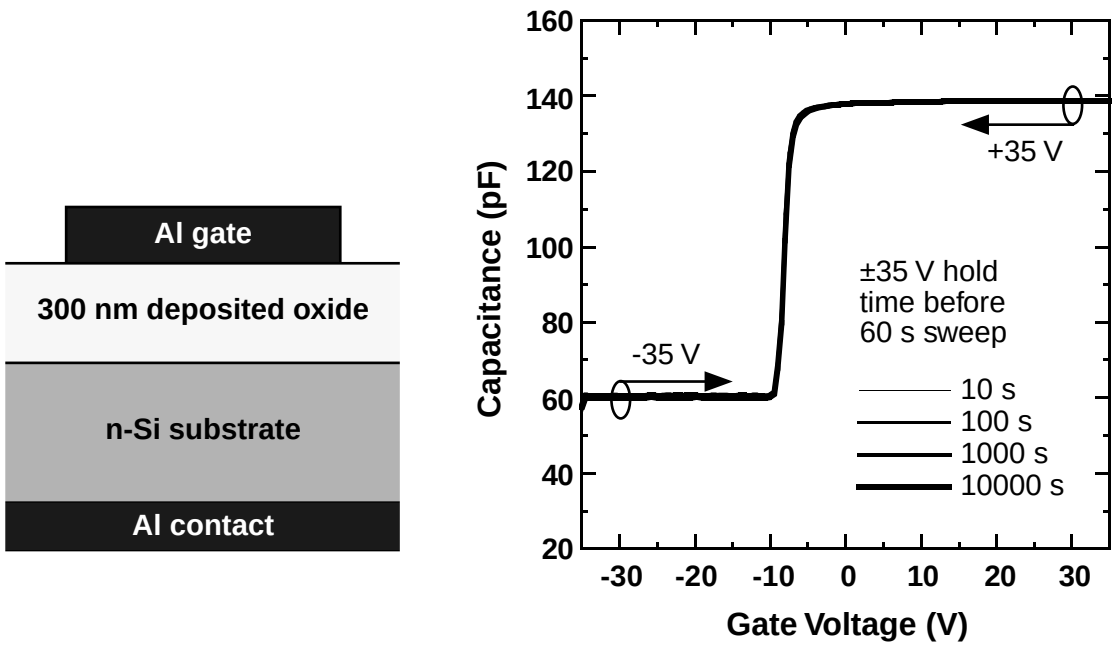


Figure 6-18 *C–V* characteristics showing no interface-related instability at both Al/oxide and oxide/Si interfaces. Virgin capacitors were stressed at -35 V and 20°C for various durations preceding the *C–V* sweeps.

Similar interface-related instabilities also occur at the gate/polymer interface. In the Al/polymer/oxide/n-Si capacitors shown in Figure 6-19, the polymer is electrically insulated from the substrate by the thermal oxide layer, thus allowing the Al/polymer interface to be inspected. Compared to polymer/Si instabilities, gate interface instabilities are more difficult to detect since the *C–V* measurement is much less sensitive to charge located near the gate interface. Hence, to demonstrate these instabilities, charge injection is accelerated by applying BTS at 300°C for one hour before examining the room-temperature *C–V* behaviors. Results show that regardless of polarity, very small gate biases introduce charge with the same polarity as V_{gate}, in this case originating from the gate electrode, deep into the dielectric. Similar charge instabilities, although with different magnitudes, are observed in other low-κ polymers.

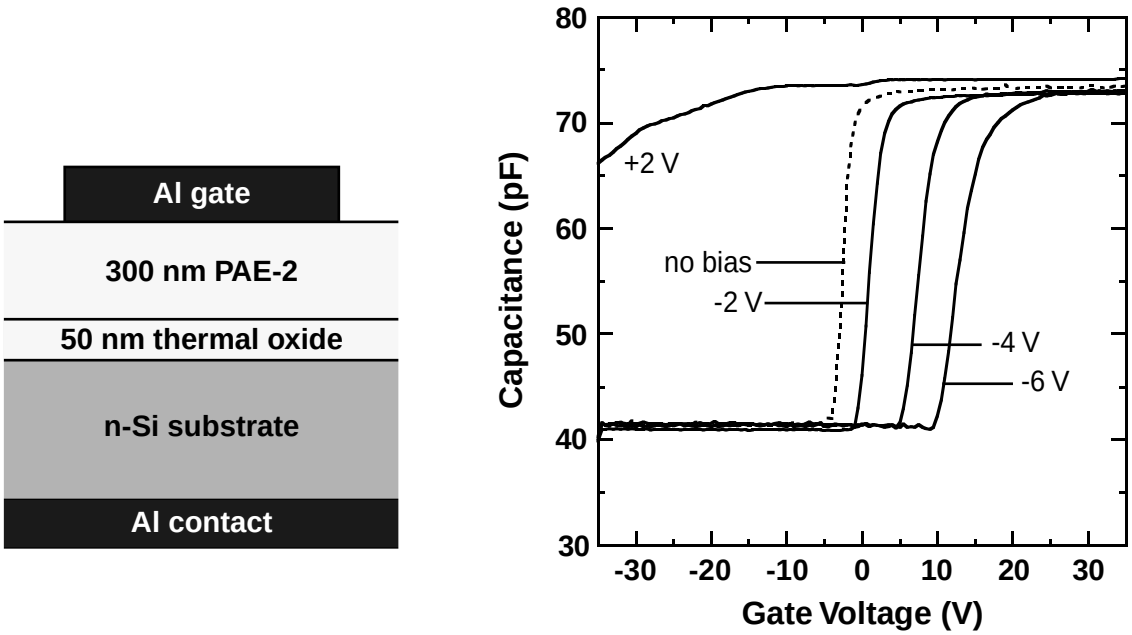


Figure 6-19 *C–V* characteristics demonstrating interface-related instabilities at the Al/polymer interface. Virgin capacitors were stressed at 300°C for one hour under various gate biases.

6.2.4 Capacitance–Voltage Analysis

The aforementioned charge instabilities motivate using the oxide-sandwiched low-κ polymer capacitor structure (Figure 6-12) to detect the penetration of Cu^+ into the low-κ polymer. Figure 6-20 shows examples of *C–V* results for PAE-2 (PAE), FPI-136M (FPI), and BCB capacitors subjected to BTS at 200°C for one hour. The *C–V* behavior is unaffected by the thermal cycles if no bias is applied. For PAE and FPI capacitors with positive V_{gate} stress, the negative flatband voltage shifts (ΔV_{FB}'s) in capacitors with Cu electrodes are much larger than those with Al electrodes, demonstrating that positive Cu^+ ions have penetrated into both PAE and FPI. The small shifts in Al capacitors, which eventually saturate with continued BTS, are attributed to trace alkali ions which are limited in quantity. For negative V_{gate} stress, negligible ΔV_{FB}'s are observed in PAE capacitors, implying that the applied bias during BTS is insufficient to induce bound polarization charge at the polymer/oxide interfaces [121]. In FPI, some polarization is observed and is believed to be attributed to the more polar chemical groups in the polyimide structure. For BCB capacitors, the *C–V* behavior is independent of gate metal and is weakly affected by a positive V_{gate} stress. This indicates that Cu^+ drift is significantly less in BCB than in PAE or FPI. The negative charge introduced by negative V_{gate} stress may be associated with dielectric wearout but is not due to Cu^+ drift since similar shifts are observed in Al capacitors.

To verify that Cu^+ is responsible for the large ΔV_{FB}'s in the PAE and FPI capacitors, BTS was performed on capacitors with PECVD silicon nitride, a good Cu^+ barrier [110], replacing the deposited oxide cap as shown in Figure 6-21. The nitride layer was deposited at 300°C using SiH_4/NH_3. Indeed, the absence of *C–V* shifts confirms that Cu^+ penetration is prevented by the 75-nm nitride layer. For this experiment, it is imperative that the polymer be adequately dehydrated prior to BTS to avoid complications with moisture polarization. Nitride is an excellent moisture barrier, proven for example by its use as a mask against steam diffusion in local oxidation of silicon (LOCOS).

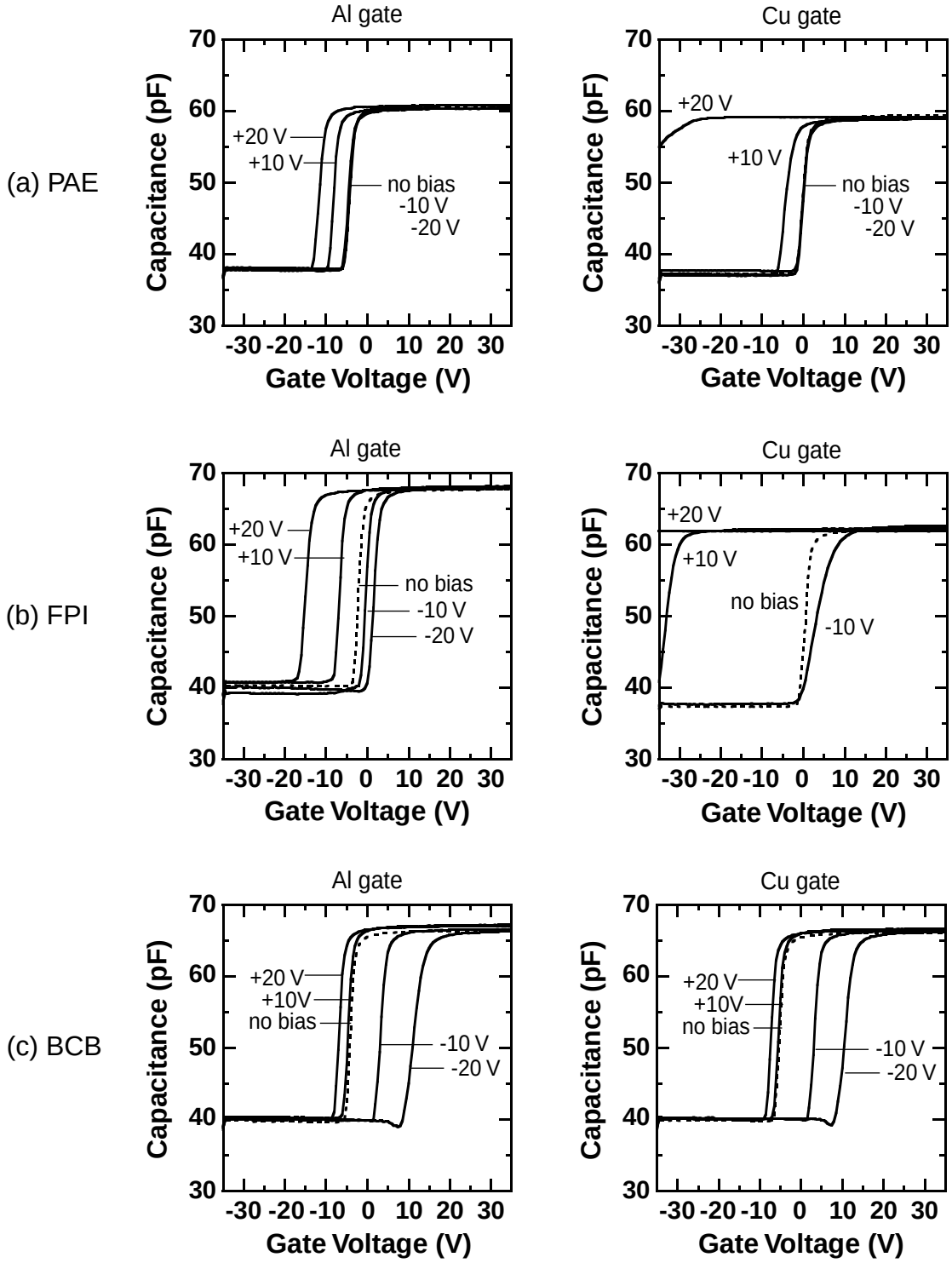


Figure 6-20 *C–V* characteristics of oxide-sandwiched (a) PAE, (b) FPI, and (c) BCB capacitors stressed at 200°C for one hour under various gate biases.

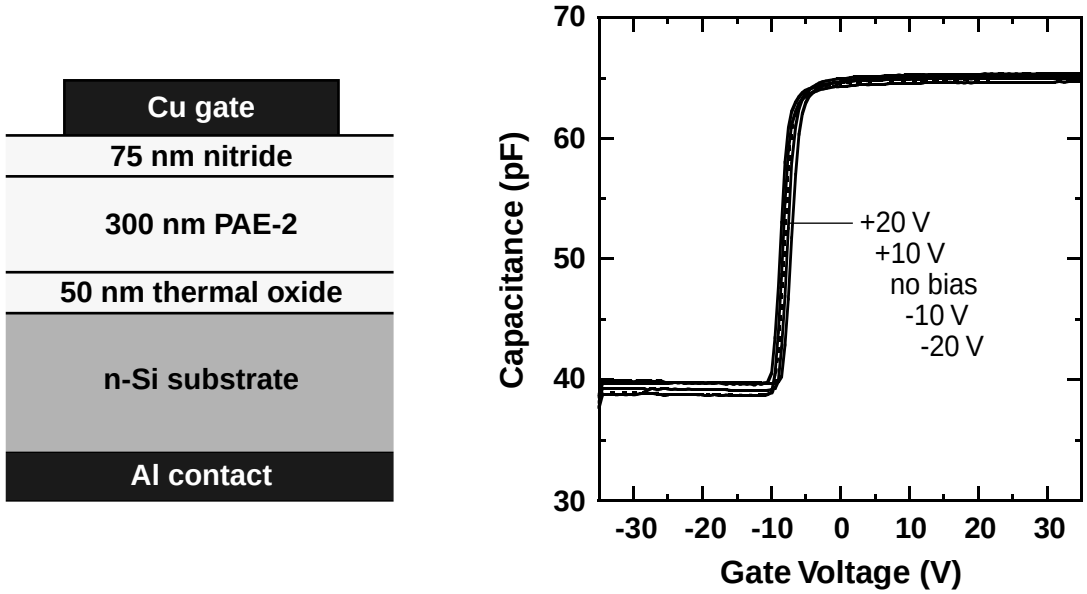


Figure 6-21 *C–V* characteristics of nitride control capacitors stressed at 200°C for one hour under various gate biases.

6.2.5 Model of Copper Drift Kinetics

Additional insight into the drift kinetics of Cu^+ is gained by measuring the I_{gate}–V_{gate} characteristics (Figure 6-22) and I_{gate}–t transients during BTS (Figure 6-23) of the Cu capacitors. These results are compared to the *C–V* characteristics to reveal two key observations. First, a good correlation exists between the magnitudes of ΔV_{FB} and I_{gate}, suggesting that I_{gate} is related to the quantity of Cu^+ penetration. Second, the decreasing I_{gate} with time under constant V_{gate} stress further implies that the electric field governing Cu^+ injection into the dielectric is decreasing with time in a manner described by the I_{gate}–V_{gate} measurement. These observations suggest that Cu^+ drift kinetics are governed by the physical model depicted in Figure 6-24. A positive V_{gate} first ionizes neutral Cu atoms into singly ionized Cu ions at the gate interface and then injects the resulting Cu^+ into the oxide cap, leaving behind electrons to be collected by the external instrument as I_{gate}. The detailed thermodynamics governing this process is modeled in [46].

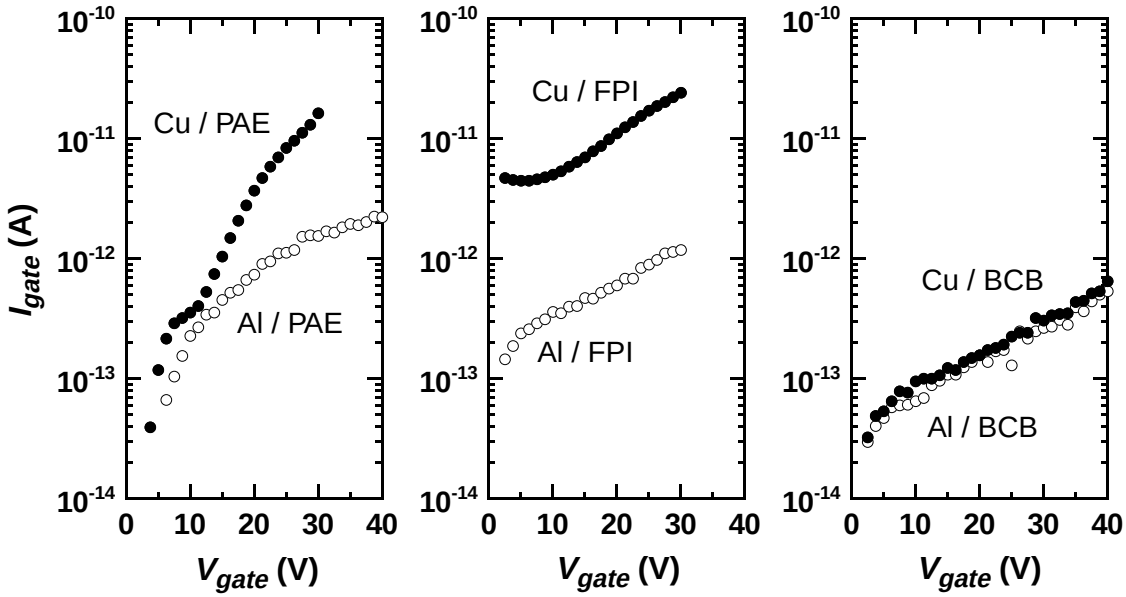


Figure 6-22 I_{gate}–V_{gate} sweeps of oxide-sandwiched PAE, FPI, and BCB capacitors at 200°C under +20-V gate bias.

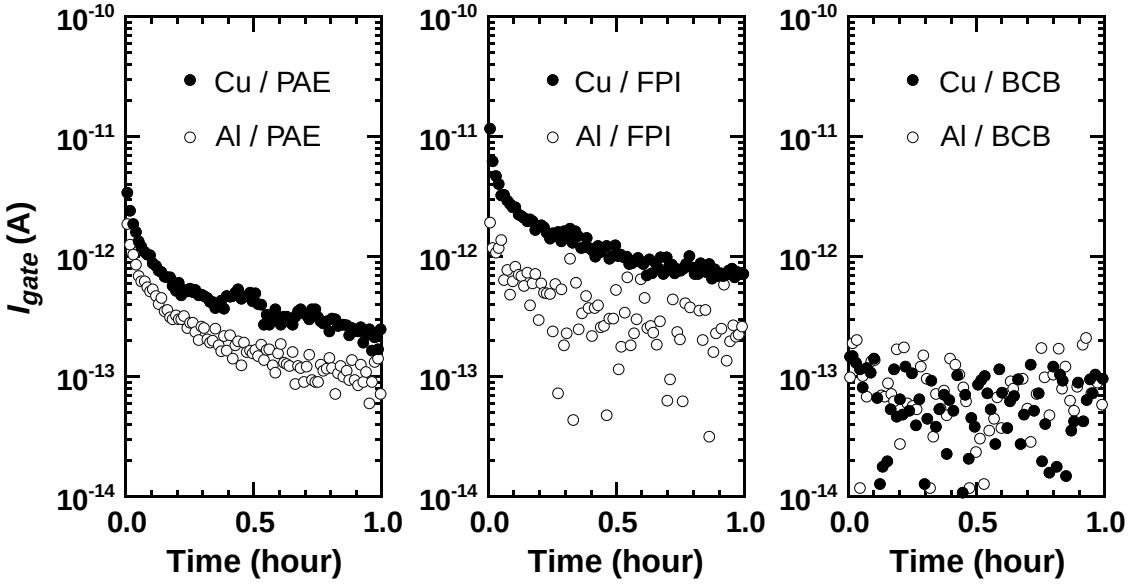


Figure 6-23 I_{gate}–t characteristics of oxide-sandwiched PAE, FPI, and BCB capacitors at 200°C. The I_{gate}–V_{gate} traces were obtained using a relatively quick V_{gate} sweep time of 1.0 minute to minimize dielectric charging.

Should Cu^+ ions penetrate readily into the polymer (PAE and FPI), they will accumulate at the thermal-oxide/Si interface, establishing an uncompensated positive space charge near the Si substrate as evidenced by the negative shift in *C–V* (Figure 6-20). Electric field divergence from this space charge will lower the electric field at the gate interface and reduce the rate of Cu^+ injection (Figure 6-22), consistent with the observed reduction of I_{gate} with time (Figure 6-23). On the other hand, should Cu^+ be unable to penetrate into the polymer (BCB), the accumulation of Cu^+ space charge in the oxide cap will quickly reduce the gate interface electric field to cease further injection of Cu^+. In this case, since the charge is located near the gate, the *C–V* behavior will be negligibly affected.

The proposed model equates J_{gate} (I_{gate} per unit area) to the rate of Cu^+ injection from the gate electrode into the dielectric. Given this hypothesis, $\Delta V_{FB}(t)$ can be predicted

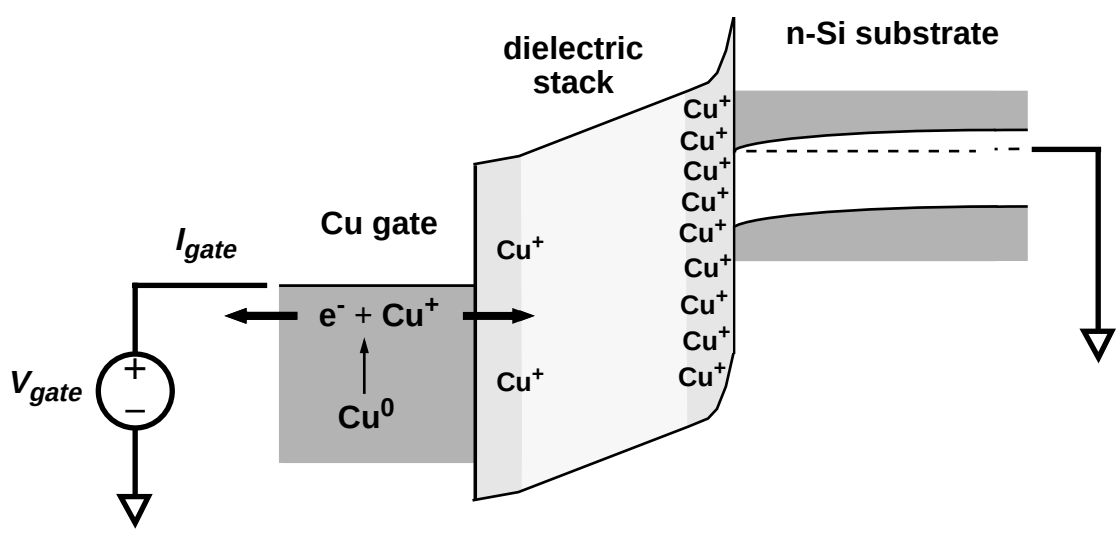


Figure 6-24 Energy band diagram illustrating proposed kinetics of Cu^+ penetration under positive V_{gate} stress. Cu atoms ionize, penetrate into the dielectric, and then accumulate in the dielectric as Cu^+ space charge. For the purpose of illustration, the band structure of the low-κ polymer is assumed to match that of oxide.

using Eq. (6-4) assuming that the injected positive Cu^+ ions, $Q_{Cu}(t)$, migrate to and accumulate at the thermal-oxide/Si interface.

$$\Delta V_{FB}(t) = -\frac{Q_{Cu}(t)}{C_{ox}} \approx -\frac{1}{C_{ox}} \int_0^t J_{gate}(\tau)\, d\tau \tag{6-4}$$

Here, C_{ox} is the capacitance per unit area of the dielectric stack and $Q_{Cu}(t)$ is the time integral of J_{gate} assuming that intrinsic dielectric conduction is negligible. As demonstrated in Figure 6-25, the model predicts the measured ΔV_{FB} transients reasonably well over a range of BTS temperatures and biases. There is some overestimation since not all the charges migrate exactly to the thermal-oxide/Si interface as assumed.

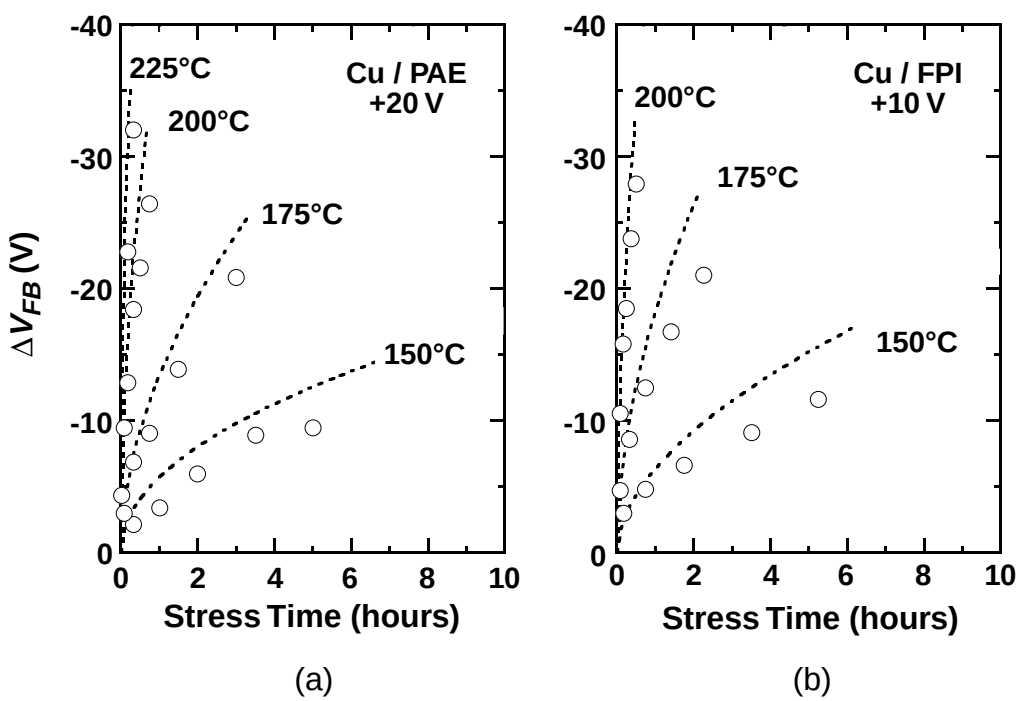


Figure 6-25 Measured ΔV_{FB} transients (○) compared to model predictions (-----) for Cu-gate (a) PAE and (b) FPI capacitors.

6.2.6 Extraction of Copper Drift Kinetics

Cu^+ drift rates in dielectrics are extracted to compare the barrier properties of various dielectrics to Cu^+ penetration but more importantly, to assess the magnitude of the reliability concern. One estimate of the Cu^+ drift rate is the rate of change of V_{FB}. Since the electric field in the dielectric evolves with time due to Cu^+ accumulation, the highest drift rate at the initial part of the transient is compared. However, this method is cumbersome as it requires many BTS experiments and C–V measurements. Alternatively, since I_{gate} reflects the quantity of injected Cu^+, a more convenient estimate of the initial Cu^+ drift rate is expressed in Eq. (6-5) using values from the I_{gate}–V_{gate} sweep at a bias level of interest.

$$DR_0 = J_{Cu-gate}(V_{gate}) - J_{Al-gate}(V_{gate}) \tag{6-5}$$

J_{gate} of the corresponding Al capacitor is subtracted to account for intrinsic dielectric conduction since ionic currents are assumed to be negligible in these Al capacitors. This correction is particularly important for dielectrics with slower drift rates, such as BCB and AF-4. For dielectrics with fast Cu^+ drift rates, such as PAE-2 and FPI-136M, intrinsic electronic conduction can be neglected since J_{gate} of the Cu capacitor is essentially attributed to Cu^+. In every I_{gate}–V_{gate} measurement, a fresh sample must be used and V_{gate} must be ramped from zero bias at a sufficiently fast rate to ensure that the rate of voltage increase is significantly faster than the rate of Cu^+ accumulation at the thermal-oxide/Si interface. Otherwise, J_{gate} will be underestimated. Initial Cu^+ drift rates estimated from the I_{gate}–V_{gate} measurements are shown in Figure 6-26. The Cu^+ drift rate into PECVD oxynitride and LPCVD SiH_4/O_2 deposited oxide are included for comparison.

The Cu^+ drift properties of various low-κ polymers have been evaluated using the oxide-sandwiched low-κ polymer capacitor. The effectiveness of this test structure hinges on the premise that the oxide layer capping the low-κ polymer is very permeable to Cu^+ migration. The kinetics of Cu^+ drift in silicon oxides from *TTF* results have been reported

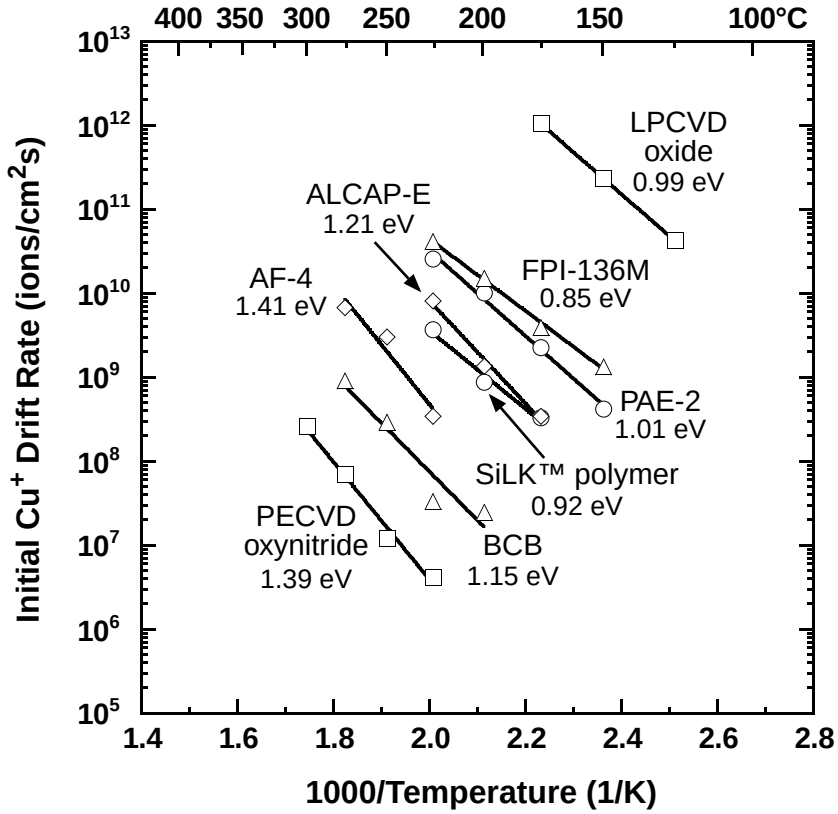


Figure 6-26 Arrhenius plot of initial Cu^+ drift rates and corresponding activation energies in various dielectrics. Drift rates were extracted from I_{gate}–V_{gate} measurements at an electric field of 0.8 MV/cm, except for PECVD oxynitride which was extracted at a field of 1.0 MV/cm.

to vary by as many as four orders of magnitude depending on film quality and growth method [110]. That study showed that thermal oxide exhibits better resistance against Cu drift compared to deposited varieties such as TEOS oxide, an unsurprising result considering that interstitial Cu ions should be less constrained to move in a porous undoped SiO_2 matrix (TEOS oxide for example) containing many more non-bridging oxygen atoms than thermal oxide [143], [144]. In this work, Figure 6-27 confirms that the deposited oxide layer did not act as a barrier for Cu^+ penetration into the low-κ polymer. Otherwise, a few orders of magnitude differences in Cu^+ drift rates from polymer to polymer would not have been observed. The oxide cap simply served as a barrier against injection of electrons and holes from the gate that would complicate *C*–*V* interpretation.

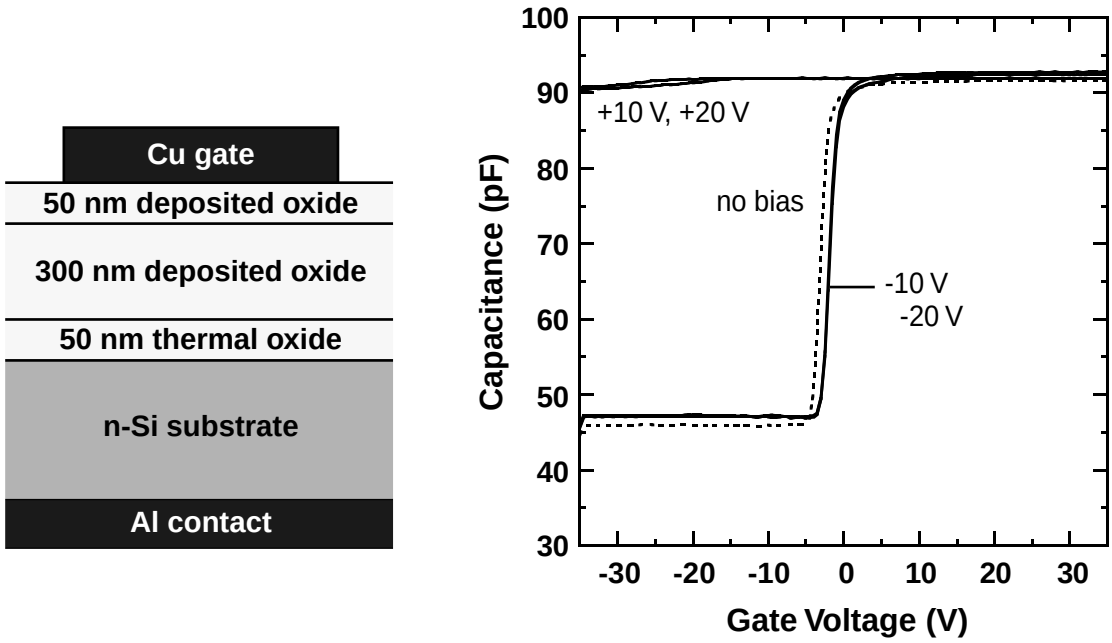
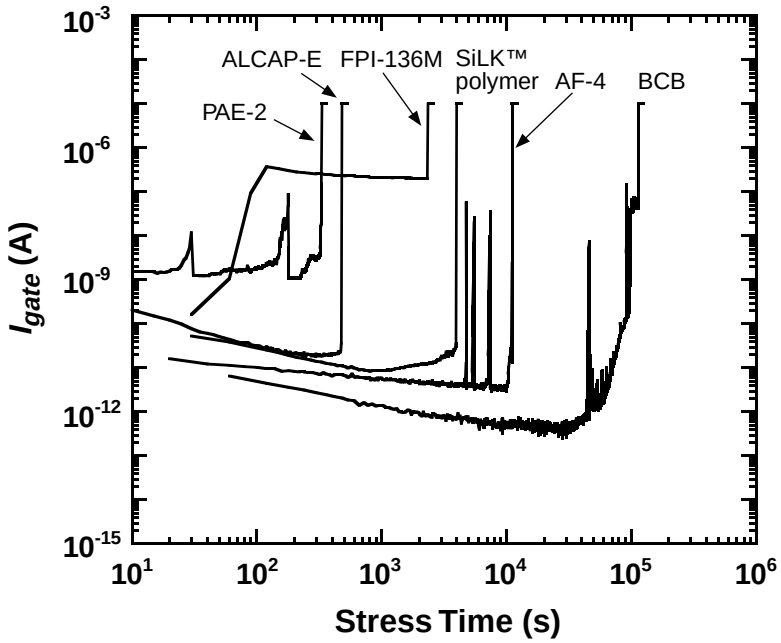


Figure 6-27 *C–V* characteristics of deposited oxide control capacitors stressed at 200°C for one hour under various gate biases.

6.2.7 Dielectric Time-to-failure Measurements

During BTS, the reduction of I_{gate} with time would seem to imply that Cu^+ drift in dielectrics is a self-limiting process with limited impact on reliability. However, as demonstrated in Section 6.1.2, Cu^+ drift will eventually lead to increased electrical leakage and ultimately dielectric breakdown given enough time for substantial penetration. Such dielectric time-to-failure experiments were performed on the oxide-sandwiched low-κ capacitors under more severe BTS conditions than in the *C–V* experiments, namely under +60 V bias (1.5 MV/cm) at 250°C, to yield more practical failure times. Figure 6-28 shows that indeed, all Cu capacitors eventually fail catastrophically. Furthermore, there is a reasonable correlation between the observed median time-to-failure and the extracted Cu^+ drift rates as summarized in Figure 6-29. Failures were not observed in corresponding Al capacitors.

(a)



(b)

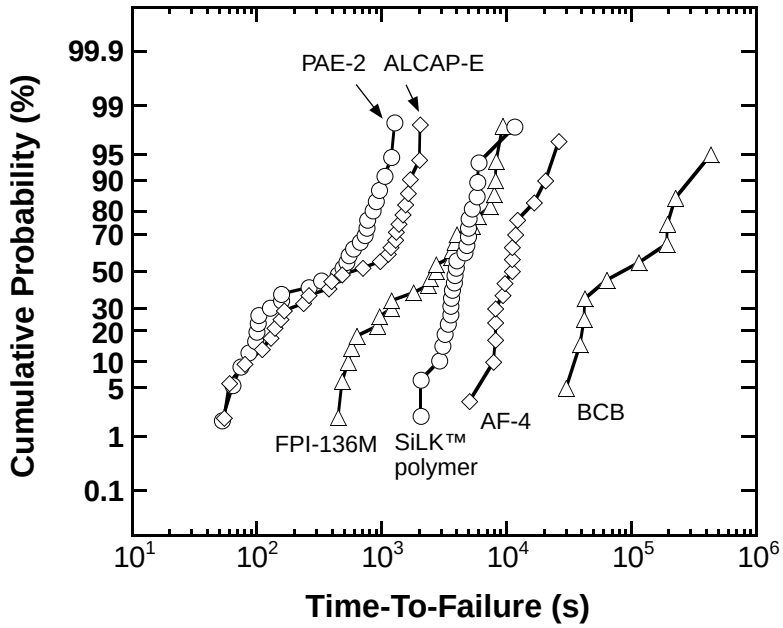


Figure 6-28 Time-dependent dielectric breakdown (TDDB) experiments of Cu-gate capacitors stressed at 250°C under +60-V bias. (a) Typical I_{gate} transients, and (b) capacitor time-to-failure (*TTF*) distribution. *TTF* was defined as stressing time required for I_{gate} to reach 10 µA.

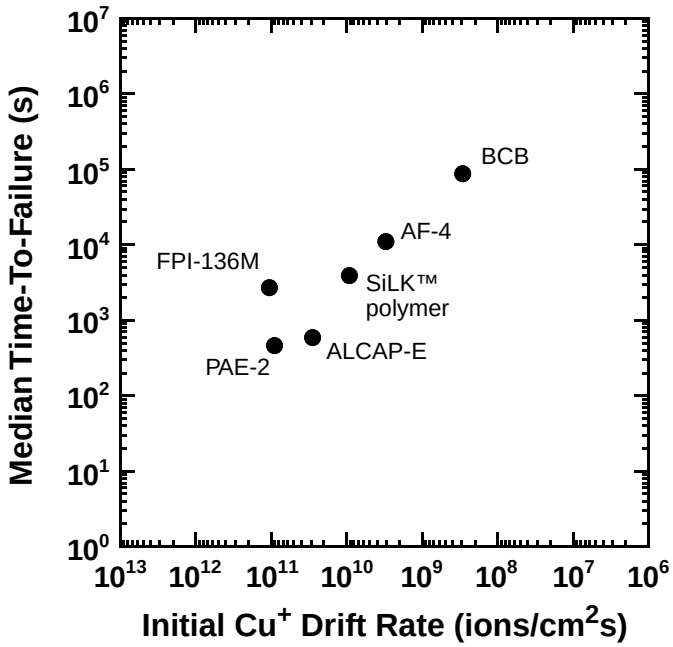


Figure 6-29 Correlation between median *TTF*'s and initial drift rates at 250°C.

Capacitor failure is believed to be a consequence of dielectric wearout induced by Cu^+ ions accumulating in the dielectric, similar to the explanation proposed in [127]. Revisiting Figure 6-24, recall that the penetration of uncompensated Cu^+ ions into the dielectric raises the electric field near the Si substrate. This increase in field will facilitate transport of electrons from the Si substrate across the thermal oxide layer via Fowler-Nordheim tunneling. The transit of charge through the dielectric will create regions of local damage which propagate through the dielectric network with continued stressing, eventually leading to capacitor failure. Observed variations in the spread of *TTF* distributions are believed to reflect structural defects and compositional inhomogeneities in the low-κ polymers.

6.2.8 Discussion

Combining the *C–V*, I_{gate}–V_{gate}, and *TTF* findings, this study shows that Cu^+ ions drift readily in fluorinated polyimide and in polyarylene ether, but less readily in parylene-F and in benzocyclobutene. Similar polymer chemistries exhibit similar behaviors as indicated by the drift rates in polyarylene ether materials (PAE-2 and ALCAP-E). The differences in observed Cu drift rates amongst the various low-κ polymer chemistries obviously reflect interactions between Cu^+ ions and the local chemical environments of the polymer. A good understanding of these interactions is difficult to grasp especially since the tested dielectrics belong to very distinct families of polymers. Moreover, the structural formulae for a few tested materials have not been disclosed. Nevertheless, some qualitative trends are suggested to speculate possible correlations between the Cu^+ drift rates and polymer properties. The properties to be examined are summarized qualitatively in Table 6-2.

Table 6-2: Trends between Copper Drift Rate and Polymer Properties

Low-κ Polymer	Relative Copper Drift Rate	Polymer Property	
		Degree of Crosslinking	Relative Aromaticity
fluorinated polyimide DuPont FPI-136M	very fast	none	high
polyarylene ether Schumacher PAE-2	very fast	moderate	high
polyarylene ether Asahi Chemical ALCAP-E	fast	moderate	high
aromatic hydrocarbon Dow Chemical SiLK™ polymer	moderate	heavy	high
parylene-F Novellus Systems AF-4	slow	crystalline	moderate
benzocyclobutene Dow Chemical BCB	very slow	heavy	moderate

To begin, Cu should already be in ionic form in the polymer since Cu must penetrate through the oxide cap in order to reach the polymer interface. Hence, the mechanism of how Cu reduces the polymer interface to percolate through the matrix as an ion need not be resolved since the oxide cap is essentially a catalyst for Cu ionization [145].

Results from this study suggest that the percolation of Cu ions through the polymers is retarded by increased crosslinking in the polymer network [80], [146], [147]. For example, SiLK™ polymer, a highly crosslinked aromatic hydrocarbon suspected to be a close relative of polyarylene ether, performs better as a Cu barrier than less crosslinked counterparts (PAE-2 and ALCAP-E). BCB, an excellent Cu barrier, is also highly crosslinked. It is speculated that highly crosslinked polymers reduce the kinetics of Cu^+ drift by minimizing the free volume in the polymer that is facilitating the interstitial migration of Cu ions. Free volume is also reduced in crystalline as opposed to amorphous polymers. This hypothesis perhaps explains the relatively good Cu barrier property of AF-4, the only crystalline polymer evaluated. One might speculate that the free volume argument can be substantiated with a correlation to mass density. However, since the chemistries of the compared polymers are so different, such an attempt will prove inconclusive.

The mobility of Cu ions in the polymer could be enhanced by polar groups in the polymer [80], [146]–[148] behaving as centers of strong negative partial charge (δ^-) that can attract Cu^+ ions electrostatically. For instance, consider the polarity of oxygen atoms incorporated in the polymers. A specific example is the the carbonyl group (C=O) present in FPI-136M. Often linked with moisture absorption, the carbonyl oxygen atom is very polar [149] and may be responsible for the high drift rate in FPI-136M. The presence of oxygen could also be responsible for the poor performance of PAE's compared to polymers with much less oxygen content, such as BCB and AF-4. The ether oxygen linkage in PAE is also polar since both bonds are not diametrically opposed. In contrast, the oxygen atoms in BCB are weakly electronegative since the attached silicon atoms are electropositive. Extending this polarity argument, the fluorine atoms of AF-4 are electronegative and may participate in Cu^+ interaction, thus admitting more Cu^+ penetration than BCB.

Strong partial negative charges also occur in aromatic rings. Electron delocalization in the conjugated bonds of the phenyl (benzene) ring results in negative charge regions (π clouds) above and below the plane of the ring [150]. Polymers with relatively strong aromatic character, such as PAE and SiLK™ polymer, exhibit poor Cu^+ barrier property compared to polymers with weaker aromatic character. This trend suggests that polymers with strong aliphatic character, that is, with abundance of carbon atoms having only single bonds, should have better Cu barrier characteristics. However, since aromaticity is deliberately incorporated in the polymer backbone in order to meet the thermal requirements of existing interconnect processing, purely aliphatic polymers cannot be considered for this application. The presence of partial charges may also be dictated by the concentration and homogeneity of defects in the polymer matrix, such as density and composition of polymer chain ends. The quality of the polymer will influence dielectric *TTF* results and could be an issue related to the maturity of the low-κ materials development.

For reliable incorporation of Cu with fluorinated polyimide or polyarylene ether, barrier encapsulation of the Cu interconnects is required. Dielectric barriers such as PECVD nitride or oxynitride will likely serve as a topside barrier to passivate the polished Cu interconnects. However, since $\kappa_{nitride} \approx 7$–$8$, the nitride thickness must be minimized to preserve the low-κ advantage of the polymer without compromising barrier integrity. Cu integration with benzocyclobutene and possibly parylene-F may relax barrier requirements but BCB will impose a limited thermal budget on process options.

These experiments were performed on planar low-κ polymer films. Barrier requirements not only depend on the intrinsic Cu barrier property of the polymer but even more importantly, on the integration scheme. For instance, in certain Damascene structures, weak interfaces may exist between the low-κ polymer and liner dielectrics. Despite the excellent Cu^+ drift barrier property of BCB and nitride, interconnect failures due to Cu^+ migration have been observed along the BCB/nitride interface [84].

6.3 Summary

This chapter addressed the barrier requirements of Cu and low-κ polymer integration with an electrical evaluation of Cu drift in these dielectrics. Bias-temperature stressing, capacitance–voltage measurements, current–voltage characteristics, and dielectric time-to-failure experiments were employed. The oxide-sandwiched low-κ polymer capacitor was developed to evaluate the Cu^+ drift behavior of low-κ polymers. This test structure circumvents interface instabilities existing when the low-κ polymer comes into direct contact with either Si or a metal. Cu drifts readily into flourinated polyimide and polyarylene ether, more slowly into parylene-F, and even more slowly into benzocyclobutene. A physical model was formulated to explain the observed kinetics of Cu^+ drift in the low-κ polymers and justify the use of current–voltage measurements to estimate Cu drift$^+$ rates. Cu integration with polymers having poor Cu^+ barrier property will require dielectric or metal barrier encapsulation. Nitride or oxynitride liners are effective dielectric barriers provided they are sufficiently thin to preserve the low-κ advantage of the polymer.

Chapter 7 Conclusion

7.1 Summary

The scaling of integrated circuit features for higher performance and density has arguably made the impact of interconnects on performance, reliability, and cost the paramount concern in the semiconductor industry. This problem has pressed the need to replace the existing interconnect system with lower resistivity conductors and lower permittivity insulators. Dual-Damascene copper integrated with conventional oxide dielectrics is now at the forefront of interconnect technology. Semiconductor companies worldwide are expected to introduce copper in high volume manufacturing within the next few years. Substantial performance gains can be further achieved through reduction of wiring capacitance. Consequently, the integration of low-κ dielectrics with Damascene copper has gained increasing attention. This dissertation concentrated on key process integration issues faced during implementation of low-κ dielectrics with Damascene copper. The dielectrics that were studied include spin-on and CVD low-κ organic polymers with dielectric constants of 2.4 to 2.8.

The electrical isolation of low-κ polymer integration was studied. Specifically, the impact of inorganic dielectric liners was examined to evaluate dielectric interface leakage

currents. Polyimide passivation over Al(Cu) interconnects inlaid in oxide increases the intralevel leakage current mainly along the polyimide/oxide interface. Moisture absorbed in the polyimide further increases the interfacial as well as bulk leakages. These findings emphasize the importance of separating interconnects from direct contact with polyimide/oxide interfaces and minimizing moisture content of polyimide during processing and use to ensure good electrical isolation between interconnects. Complete liner encapsulation of interconnects is a potential solution provided that process complexity is controlled and that the capacitance advantage of the low-κ polymer is not severely compromised.

A generic electrical technique was developed to extract the in-plane dielectric constant, $\kappa_{||}$, of a blanket dielectric film for Damascene applications. Since some low-κ polymers are structurally very anisotropic, the anisotropy in permittivity may adversely affect crosstalk noise. The technique is based on measuring the fringe capacitance between interdigitated Damascene metal lines passivated by the dielectric film of interest. The effective dielectric constant of the passivating dielectric is first obtained by interpolating the measured capacitance using reference structures passivated by two isotropic dielectrics with known dielectric constants. Following this extraction, a two-dimensional interconnect simulator is employed to decouple the effect of the out-of-plane dielectric constant, $\kappa_{\perp}$, in the fringe fields in order to extract $\kappa_{||}$. The technique was demonstrated using fluorinated polyimide, with the reference dielectrics being air and oxide.

Finally, the barrier requirements of copper and low-κ polymer integration were determined through an electrical evaluation of copper drift in the polymer dielectrics. Bias-temperature stressing, capacitance–voltage measurements, current–voltage characteristics, and dielectric time-to-failure experiments were employed. An oxide-sandwiched low-κ polymer capacitor was developed to evaluate the Cu^+ drift behavior of low-κ polymers. Copper drifts readily into flourinated polyimide and poly(arylene ether), more slowly into parylene-F, and even more slowly into benzocyclobutene. A physical model was formulated to explain the observed kinetics of Cu^+ drift in the low-κ polymers and justify the use of current–voltage measurements to estimate copper drift$^+$ rates. Copper

integration with polymers having poor Cu^+ barrier property will require dielectric or metal barrier encapsulation. Nitride or oxynitride liners are effective dielectric barriers provided they are sufficiently thin to preserve the low-κ advantage of the polymer without compromising barrier integrity.

7.2 Suggestions for Future Work

This dissertation touched on a few of many technical challenges that must be resolved before low-κ polymer dielectrics are successfully integrated with Damascene copper. The suggestions that follow are extensions of this work whose results should hopefully be relevant and complementary to industrial research.

Since IC's benefitting from high-performance interconnects will invariably operate at frequencies exceeding 1 GHz, it is important that the dielectric constant and its anisotropy be carefully characterized at these frequencies. In this work, the electrical measurements were performed at much lower frequencies where on-chip and test setup parasitics could be neglected. However, the same measurements at GHz frequencies are greatly complicated by issues such as test setup impedance mismatches and on-chip parasitics. At these frequencies, dielectric loss (imaginary component of κ) of these low-κ materials may be significant, similar to silicon dioxide. Since many low-κ polymers absorb some moisture, there is the concern that even trace levels of absorption may greatly impact both dielectric constant and dielectric loss.

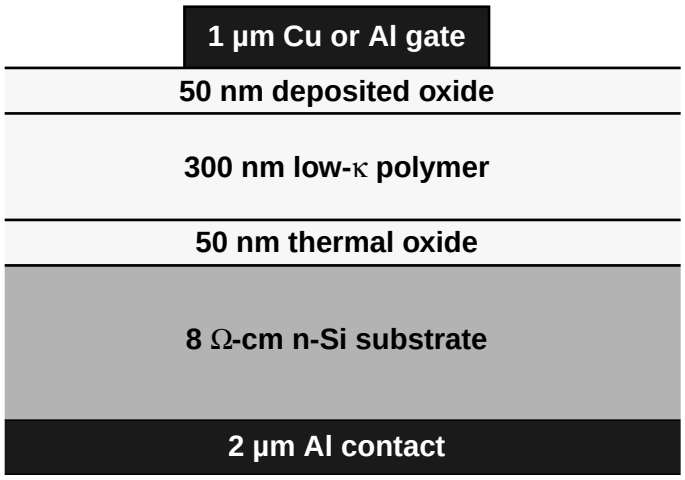
There are ample opportunities for further investigations of copper drift in low-κ dielectrics. The low-κ polymers that were tested did not exhibit drift barrier properties as good as silicon oxynitride. As new and innovative low-κ materials emerge, it is conceivable that there exists a suitable low-κ dielectric with excellent resistance against copper drift. Evaluating the drift properties of new low-κ dielectrics can also solidify the limited existing understanding of how dielectric chemistry impacts copper drift. Since low-κ polymers are structurally anisotropic, the copper drift behavior may be quite different in the wafer in-plane direction as compared to the evaluated out-of-plane behavior. Interdig-

itated structures will be required for this investigation. Some insight must be developed in order to identify whether copper drift occurs primarily through the dielectric bulk or along dielectric interfaces. In addition to the electrical findings, physical confirmation of copper drift in low-κ dielectrics is important. The challenge is to develop a technique suitable for profiling copper ions in the polymers. There has been a substantial collaborative effort with Motorola to employ SIMS for such an investigation. Unfortunately, preliminary attempts were inconclusive as there are measurement artifacts due to the charged sputtering beam that are convoluting the depth profiling.

The development of interconnects with copper and low-κ dielectrics remains an industry-wide effort with much progress expected in the few years to come. It is hoped that the findings in this work have contributed somewhat to the growing pool of knowledge that will ultimately direct the industry to achieve the inevitable.

Appendix Capacitor Process Flow

This appendix details the process flow for fabricating the oxide-sandwiched low-κ polymer capacitors described in Section 6.2.1 of Chapter 6. The capacitors were processed entirely in the clean room facility at the Center for Integrated Systems at Stanford University except for the low-κ polymer films which were processed by the respective low-κ materials suppliers.



1 Wafer Preparation

1.1 Starting material.

4-inch (100) Silicon prime wafer, n-type (phosphorus), 5–10 Ω-cm.

1.2 Measure wafer sheet resistivity (Sonogage rt^2).

1.3 Scribe wafer ID on wafer backside near primary flat.

1.4 Initial clean at nonmetal wetbench (wbnonmetal)— fresh chemicals.

H_2O rinse (× 2).
H_2SO_4/H_2O (9:1) at 120°C for 00:20:00.
H_2O rinse. Spin dry

2 Thermal Oxidation

2.1 Pre-diffusion clean at diffusion wetbench (wbdiff)— fresh chemicals.

H_2O rinse.
H_2SO_4/H_2O_2 (4:1) at 90°C for 00:10:00.
H_2O rinse.
$H_2O/HCl/H_2O_2$ (5:1:1) at 70°C for 00:10:00.
H_2O rinse. Spin dry.

2.2 Grow thermal oxide in furnace (tylan1–tylan4).

Immediate load after pre-diffusion clean.
Recipe = dry1000
Ambient = O_2
Temperature = 1000°C
Time = 00:54:00
Target thickness = 50 nm

2.3 Measure oxide thickness (Nanospec).

Program #7 (thin oxide on silicon, use n = 1.45).

3 Low-κ Polymer Deposition

3.1 Deposit low-κ polymer (materials supplier location).

Target thickness = 300 nm
Schumacher PAE-2 (Schumacher, Carlsbad, CA)

1. Deposit ~4 mL of 5% PAE-2 at 300 rpm (cyclohexanone solvent).
2. Spin at 1000 rpm for 00:00:20.
3. Heat at 80°C for 00:02:00.
4. Heat at 250°C for 00:02:00.
5. Repeat steps 1–4.
6. Heat at 425°C in 15 s/m N_2 ambient for 00:30:00.
7. At 425°C, flow 3 s/m O_2 & 12 s/m N_2 for 00:20:00 (crosslinking step).

Asahi Chemical ALCAP-E (Asahi Chemical Company Industry, Fuji, Japan)

1. Deposit ~4 mL of 12% ALCAP-E at 500 rpm for 00:00:05
   (mesitylene & PGMEA solvent mixture).
2. Spin at 1500 rpm for 00:00:30.
3. Heat at 120°C for 01:00:00 in air.
4. Heat at 400°C for 01:00:00 in pure N_2.

Dow Chemical SiLK (Dow Chemical Company, Midland, MI)

Temperature/humidity (T/H) control critical (27°C, 26% RH)

1. Apply 2–3 mL AP8000 siline-based adhesion promoter
   (MTI Flexifab spin coater with SemiFab Model CD200 T/H controller).
   Let stand for 00:00:02.
   Spin at 3000 rpm for 00:00:10.
2. Apply 2–3 mL SiLK™ prepolymer solution (NMP solvent).
   Spin at 2000 rpm for 00:00:20.
   Apply continuous stream of mesitylene to backside for 00:00:05.
3. Bake at 70°C for 00:00:20.
4. Remove 2–5 mm edge bead with mesitylene at 2000 rpm.
5. Hot plate bake at 325°C for 00:01:30 under N_2 blanket.
6. Cure at 450°C for 00:06:00 (YES Model PB-6 polymer bake oven).

DuPont FPI-136M (HD MicroSystems, Wilmington, DE)

1. Dehydration bake at 150°C for 00:02:00, vacuum contact on hot plate.
2. Prime with 0.5% VM651 adhesion promoter in H_2O.
   Flood H_2O for 00:00:20.
   Spin VM651 (γ-aminopropyl-triethoxysilane) at 2000 rpm for 00:00:30.
   Bake in vacuum contact with 90°C hot plate for 00:01:00.
3. Dispense ~2 g FPI-136M (9.2 wt. %, 675 cps, NMP solvent).
   Spin wafer at 1000 rpm for 00:00:05.
   Then spin at 7000 rpm for 00:02:00.
4. Proximity bake for 00:01:00, gap 15 over 90°C hot plate.
5. Vacuum contact bake for 00:01:00 on 90°C hot plate.
6. Vacuum contact bake for 00:01:00 on 150°C hot plate.
7. Cool for 00:00:10.
8. Cure at 375°C for 01:00:00.

Dow Chemical BCB (Dow Chemical Company, Midland, MI)

1. Dispense 2–3 mL of prepolymer solution, Cyclotene™ 5021
   (CEE Model 100 bench top spinner).
2. Spin at 2000 rpm for 00:00:20.
3. Dry bake.
4. Remove 2–5 mm edge bead with mesitylene at 2000 rpm.
5. Bake at 70°C for 00:00:20.
6. Cure at 300°C for 00:30:00 in N_2 (YES Model PB-6 polymer bake oven).

Novellus AF-4 (Novellus Systems, San Jose, CA)

Pyrolyzer temperature = 650–680°C

Vaporizer temperature = 100°C

Deposition conditions: -15°C at 25 mTorr

Deposition rate = 0.1 µm/minute

Post-deposition vacuum anneal in pecvd furnace at CIS.

Cool tube to room temperature for cold load.

Heat tube to 350°C in vacuum (01:00:00).

Anneal at 350°C for 00:01:00 (2.0 mTorr).

Cool tube to room temperature (12:00:00) for cold unload.

Optical microscope inspection (dark field).

3.2 Measure low-κ polymer thickness (Nanospec).

Customized dual-layer programs (polymer on oxide on silicon).

Cauchy coefficients obtained from materials supplier.

4 Oxide Cap Deposition

4.1 Pre-deposition clean at metal wetbench (wbmetal)— fresh chemicals.

Blank Si dummy wafers included for oxide thickness measurement.

PRS-1000 Clean at 40°C for 00:10:00 (loaded dry).

Composition of PRS-1000

1-methyl-2-pyrrolidinone (NMP)

Thiophene, tetrahydro-,1,1-dioxide

Diethylene glycol monoethyl ether

Ethanolamine

H_2O rinse. Spin dry. H_2O rinse. Spin dry.

4.2 Deposit oxide cap on front side (Strataglass).

Target thickness = 50 nm

Boat clean immediately before oxide runs.

Cold tube load at 100°C (specify clean tweezers).

Evacuate tube.

Wafer surface pre-clean with argon RF sputter (omit for AF-4).

1 Torr, 50 sccm Ar flow, 60 W, 00:03:00

Heat to 300°C and soak at 300°C for 01:00:00 for moisture degas (critical).

Oxide deposition

0.8 Torr, 800 sccm N_2O flow, 40 sccm SiH_4 flow, 60 W, 00:01:36

Important to prevent prolonged wafer exposure to oxidizing precursor gases.

Boat pull at 150°C.

Optical microscope inspection (dark field).

4.3 Measure oxide thickness of dummy wafers (Nanospec)

Program #7 (thin oxide on silicon, use n = 1.55).

5 Gate Metal Deposition

5.1 Pre-deposition clean at metal wetbench (wbmetal)— fresh chemicals.

PRS-1000 Clean at 40°C for 00:10:00 (loaded dry).

H_2O rinse. Spin dry. H_2O rinse. Spin dry.

5.2 Deposit 100% aluminum or copper on front side.

Target thickness = 1 µm

Immediate load after pre-deposition clean.

Aluminum wafers

- DC magnetron sputtering system (gryphon)
- Lock Program #2 (moisture degas) (ciritical)
  - 00:02:00 at ~ 200°C ($\times$ 2)
- Process Program #6 (aluminum sputtering)
  - Base pressure $\leq 1 \times 10^{-7}$ Torr
  - Process pressure = 2.3 mTorr
  - 00:10:00 at 40°C ($\times$ 2)
  - Power = 7.5 kW

Copper wafers

- DC sputtering system (Center for Materials Research)
- Bake at 200°C for 30 minutes for moisture degas (critical).
- Copper sputtering
  - Base pressure $\leq 6\text{–}8 \times 10^{-6}$ Torr (~8–12 hour wait)
  - Process pressure = 2.3 mTorr
  - 00:20:00 at room temperature (+ 00:02:00 target pre-sputter)
  - Power = 0.2 kW

5.3 Measure metal sheet resistance (prometrix).

6 Gate Metal Definition

6.1 Apply photoresist to front side (svgcoat).

Omit singe at 150°C.

Coat 1.0 µm Shipley 1813 photoresist (coat recipe #1).

Pre-bake photoresist at 105°C (bake recipe #1).

6.2 Expose photoresist (ultratech).

Reticle: JAMESCAP.JB (Field #1)

Dose: 100 mJ/cm^2 (aluminum), 120 mJ/cm^2 (copper)

Runmode 1: first level lithography (no alignment)

6.3 Develop photoresist (svgdev).

Develop with Microposit MF-319 (TMAH) (develop recipe #1).

Omit developer track post-bake.

Omit post-bake at 110°C.

Optical microscope inspection.

6.4 Wet-etch gate metal— fresh chemicals.

Immediate etch after photoresist develop.

Aluminum wafers (wbmetal)

H_2O soak.

Aluminum Etch II at 40°C for ~5 minutes.

Composition of Aluminum Etch II

Phosphoric acid, H_3PO_4	91.47%
Nitric acid, HNO_3	1.38%
Acetic acid, CH_3COOH	7.15%

H_2O rinse ($\times$ 2). Spin dry.

Copper wafers (wbgeneral)

Copper etch at room temperature for ~3–5 minutes (loaded dry).

Composition of copper etch

Ammonium persulfate, $(NH_4)_2S_2O_8$	90 g
Ammonium chloride, NH_4Cl	6 g
Deionized H_2O	1 L

H_2O rinse. Blow dry.

Optical microscope inspection (check undercut).

6.5 Strip frontside photoresist— fresh chemicals.

Immediate photoresist strip after metal etch.

Aluminum wafers (wbmetal)

PRS-1000 Clean at 40°C for 00:20:00 (loaded dry).

H_2O rinse. Spin dry. H_2O rinse. Spin dry.

Copper wafers (wbgeneral)

PRS-1000 Clean at room temperature for 00:20:00 (loaded dry).

H_2O rinse. Blow dry. H_2O rinse. Blow dry.

Inspect to ensure that photoresist is completely stripped.

7 Backside Oxide Removal

7.1 Apply photoresist to front side (svgcoat).

Omit singe at 150°C.

Coat 1.6 µm Shipley 1813 photoresist (coat recipe #2, omit HMDS prime).

Pre-bake photoresist at 105°C (bake recipe #1).

7.2 Strip backside oxide.

Aluminum wafers (wbmetal)

Buffered oxide etch (20:1 BOE) for 00:04:00 (loaded dry).

H_2O rinse. Spin dry.

Copper wafers (wbgeneral)

Buffered oxide etch (20:1 BOE) for 00:04:00 (loaded dry).

H_2O rinse. Blow dry.

7.3 Strip frontside photoresist— fresh chemicals.

Aluminum wafers (wbmetal)

PRS-1000 Clean at 40°C for 00:20:00 (loaded dry).

H_2O rinse. Spin dry. H_2O rinse. Spin dry.

Copper wafers (wbgeneral)

PRS-1000 Clean at room temperature for 00:20:00 (loaded dry).

H_2O rinse. Blow dry. H_2O rinse. Blow dry.

8 Backside Metal Deposition

8.1 Pre-deposition clean— fresh chemicals.

Immediate clean after backside oxide strip.

Aluminum wafers (wbmetal)

PRS-1000 Clean at 40°C for 00:20:00 (loaded dry).

H_2O rinse. Spin dry. H_2O rinse. Spin dry.

Copper wafers (wbgeneral)

PRS-1000 Clean at room temperature for 00:20:00 (loaded dry).

H_2O rinse. Blow dry. H_2O rinse. Blow dry.

8.2 Deposit 100% Al on wafer backside.

Target thickness = 2 µm

DC magnetron sputtering system (gryphon)

Immediate load after pre-deposition clean.

Lock Program #2 (moisture degas)

00:02:00 at ~ 200°C ($\times$ 2)

Process Program #6 (aluminum sputtering)

Base pressure $\leq 2 \times 10^{-7}$ Torr

Process pressure = 2.3 mTorr

00:10:00 at 40°C ($\times$ 2)

Power = 7.5 kW

9 Forming Gas Anneal

9.1 Forming gas anneal (pecvd)

Cool tube from 300°C idle to room temperature for cold load (12:00:00).

Load at room temperature.

Heat tube to 350°C in N_2 (01:00:00).

Flow forming gas for 1 hour (2 Torr).

Cool tube to room temperature for cold unload (12:00:00).

Unload at room temperature.

9.2 Final inspection.

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List of Related Publications

[1] A. L. S. Loke, C. Ryu, C. P. Yue, J. S. H. Cho, and S. S. Wong, "Kinetics of copper drift in PECVD dielectrics," *IEEE Electron Device Letters*, vol. 17, no. 12, pp. 549–551, Dec. 1996.

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