Numerical Modeling and Characterization of the Stress Migration Behavior Upon Various 90 nanometer Cu/Low k Interconnects

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Abstract

Stress migration (SM) behavior found on various Cu/Low k interconnects is analyzed in this article. The simulation results demonstrate that the minimum stresses always occur on/near via bottom, which makes the dummy via insertion an effect way relieving SM induced circuit failure. A numerical index reflecting the bulk vacancy density evolution is developed from the simulated stress distribution and aimed at predicting the destination of the migrating vacancies driven by the thermally generated stress gradient of the interconnect system. Though still in its burgeoning stage, the simulated SM behavior using the index compared well against those experimentally collected data.

Keywords: stress-migration, SM

Introduction

Stress migration phenomenon has been a critical reliability concern for various Cu/Low k interconnects. Its mechanism is well described and can be found elsewhere. [1~3] One of its major aspect tells that the thermally generated stress gradients of various three-dimensional (3D) interconnects, due in part to the material mismatch among various existing interfaces, drive the saturated vacancies within Cu diffuse through the pathways towards certain locations and accumulate to form electrically detrimental voids (Fig. 1). These voids deteriorate the performance of the circuits fabricated using Cu/Low k material system with the explicit symptom of unstable even fatal electrical properties. Thus, these voiding sites or the destination of the migrating vacancies are important to the circuit designers or the set-up of design rules so as to implement SM-resistant circuit designs and avoid their accumulation. Numerical method, particularly finite element method (FEM), is a good tool to obtain the thermally generated stress profiles of the versatile circuit designs and assess the most probable sites for the vacancy accumulation before the actual and costly mask tape-out, especially for the 90 nanometer technology node and beyond. In this article, a 3D FEM simulation analysis was conducted to study the SM behavior of Cu/Low k interconnects, both local and semi-global approaches are reported. In addition, a numerical index that reflects the time dependent vacancy density distribution is developed and aimed at predicting the destination of the migrating vacancies in the interconnect system. Though still in its burgeoning stage, the simulated SM behavior using the index compared well against those experimentally collected data.

Experimental

Two levels of Cu/Low k interconnect plus one level top metal layer and one passivation layer were fabricated for the current SM studies. Single damascene wafer processing was applied to the bottom metal layer and dual-damascene techniques to the upper metal layers and the linking vias. After the multi-level process flow and the passivation, the processed wafers were subjected to an unbiased thermal-stressing environment (with an ambient temperature specified at 175℃) for a continuous time period of 168 and 500 hours. The resistance of test patterns was measured and recorded before and after the thermal stressing, and the resistance shift of all samples were analyzed to obtain their statistic significance.

Numerical Simulations

Test structures

Various test circuits used as part of process development and reliability-monitoring vehicles were selected and numerically simulated to characterize their SM performance for the current studies. Fig. 2(a) ~ Fig. 2(f) illustrates the unit pattern of these circuits. A quarter of the symmetrical 3D physical model was constructed for each of the unit pattern of the studied circuits. The finite element simulations were carried out using the commercial package ANSYS to obtain their stress profiles for further analysis. The initial stress free temperature and the final thermal stressing temperature were specified at 275℃ and 175℃, respectively.

Numerical index reflecting the vacancy concentration

It is aforementioned that the thermally generated stress gradient of the copper interconnect drives the saturated vacancies towards the low stress regions through the pathways of either the copper grain boundaries or the liner/copper interfaces. Since the stress states are lower for the copper near/along the liner/Cu interface as compared with those regions in the bottom of a metal lead (Fig. 3), the vacancies will be driven from the film bulk towards the liner/Cu interfaces. Moreover, along the liner/Cu interfaces (the fast and easiest pathways for vacancy migration,) the bottom regions of the linking via are always the ones having the lowest stresses along the interfaces (Fig. 3), and thus, are prone to become the destination of the traveling vacancies.

To numerically mimic the physics of vacancy migration, a concept of the vacancy concentration or vacancy density is introduced. The vacancy concentration and its movement can be described as follow (4):

$$\frac{\partial C}{\partial t} = -\nabla\left[-\frac{D_p}{\Omega kT}\left(\Omega kT\nabla C - \Omega\nabla\sigma_H\right)\right] \qquad (1)$$

where D_p is the diffusion constant, C the atomic concentration, Ω the atomic volume, k the Boltzmann's constant, T the absolute temperature and σ_H the hydrostatic stress. Eqn (1) states that the evolution of vacancy density (per unit volume) at different time equals the preexisting vacancy concentration plus its variation over various spatial distances while stressed by σ_H. For our modeling scheme, a numerical index reflecting the vacancy density is developed to emulate the vacancy concentration evolution within each material volume/element, in which each finite element of the constructed FEM model is considered to be a unit volume with a specified pre-existing vacancy density. With the stress profiles simulated using FEM simulation, the vacancy movement along each spatial direction can be calculated and

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the index number or the simulated vacancy density of each location at various time thus obtained accordingly. It is noted that the stress evolution is considered negligible for the studied test structures.

Results and Discussions

Fig. 4 shows the circuit resistance shifts of the patterns shown in Fig. 1(a) and Fig. 1(c). It is shown that the case with via landing upon the metal lead center results in worse SM performance. The electrical properties of the test circuits having single via and dual via landed upon the center of the larger metal leads are shown in Fig. 5. It demonstrates that the case with double vias result in better SM-resistance than the test patterns having single via after the thermal stressing. It is thus interesting to elucidate the role the second via play. According to the SM mechanism there exist two possibilities. One is the stress gradient reduction effects leading to a reduced vacancy migration rate and it can be justified looking into a localized stress profile of the domains near the via bottom (Fig. 6); or it purely serves as another vacancy collector and shares the load of vacancy accumulation. From a semi-global viewpoint, the stress profiles clearly shows that the stress profiles hardly change for the bulk of the test patterns (Fig. 6) except the minor variation close to via area. Moreover, via bottom area is always the one having the lowest stress and the large metal lead center is the area where the maximum stresses occur. These results imply that the stress reduction effect is quite minor as compared with the stress distributions in the area from which the vast vacancy supply. Therefore, it is more likely that the second via share the vacancy only. It also points out the necessity of looking into the stress profiles of the whole patterns. Fig. 3 shows the stress profiles with and without a dummy via addition where most of the stress profiles unchanged except the area close to the inserted second via bottom. This result makes the dummy via addition an effect way reducing the SM induced interconnect reliability concerns (5) because the dummy via provides another destination for the migrating vacancies to go.

Fig. 7~9 shows the numerical indexes evolution of various test patterns calculated using their simulated stress profiles (Fig. 10). It is found that the index numbers reflecting the vacancy density upon via bottom is always higher for the pattern having single via than those having dual vias. And their difference is enlarged as the time step of the numerical simulation goes higher or for the longer thermal stressing time. The vacancy density index contours for all the 6 test patterns are illustrated in Fig. 11 where the high vacancy density areas are found near via bottom and the second via shares the arriving vacancies. Therefore, the second via addition reduces the probability of resulting in a significant resistance shift or open via. These results correlate with those experimentally collected electrical data after the thermal stressing.

Conclusions

Stress migration (SM) behavior found on various Cu/Low k interconnects is analyzed and the FEM simulation results obtained, which demonstrate that the minimum stresses always occur on/near via bottom, and it makes the dummy via insertion an effect way relieving SM induced circuit failure. A numerical index reflecting the bulk vacancy density evolution is developed from the simulated stress distribution. Though still in its burgeoning stage, the simulated SM behavior using the index compared well against those experimentally collected data.

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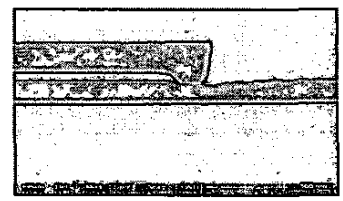

Fig. 1 Focused Ion-beam picture of a typical vacancy accumulation site upon/near the via bottom regions

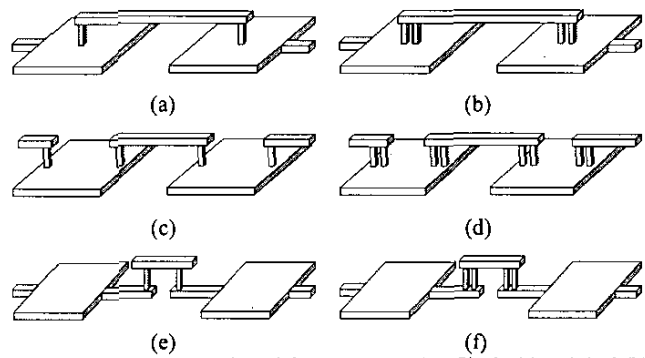

Fig. 2 Various patterns adopted for current studies. Single (a) and dual (b) via landing upon center of the large metal lead center; single (c) and dual (d) via landing upon edge of the large metal lead; single (e) and dual (f) via landing upon both ends of line extension.

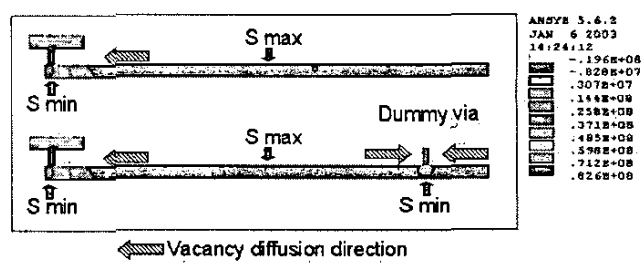

Fig. 3 Simulated stress profiles of a Cu/Low k interconnect. Maximum and minimum stresses occur in the center of the metal and via bottom area

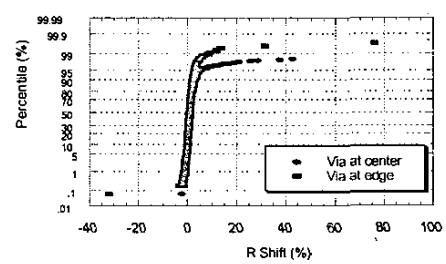

Fig. 4 Probability plots of the resistance shifts for the patterns having single via landing upon large metal lead center (Fig. 2(a)) and edge (Fig. 2(c)) after 168 hours of thermal stressing.

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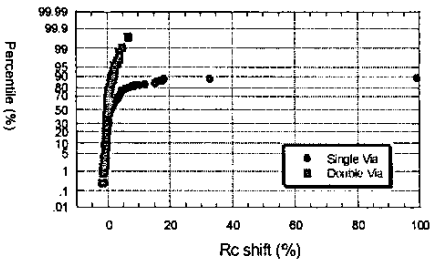
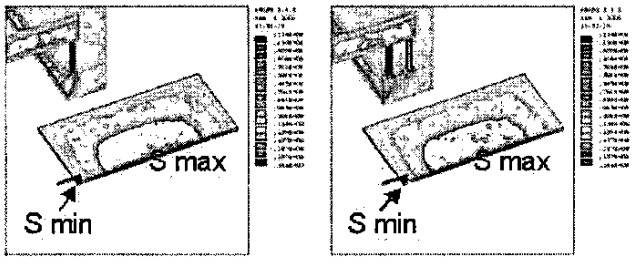


Fig. 5 Probability plots of the resistance shifts for the patterns having single via (Fig. 2(a)) and dual vias (Fig. 2(b)) landing upon the center of the large metal lead after 500 hours of thermal stressing.



(a) (b)

Fig. 6 Locally and semi-globally simulated stress profiles (a) single via, (b) double vias landing upon edge of the metal lead

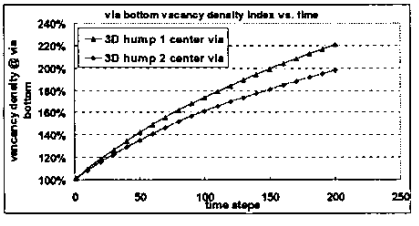


Fig. 7 Numerical index for vacancy density evolution of patterns having single via (Fig. 2(a)) and dual vias (Fig. 2(b)) landing upon large metal lead

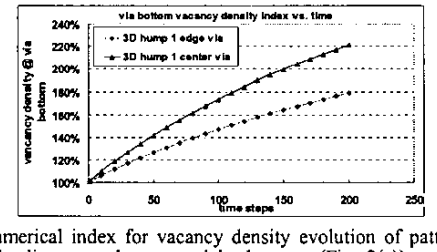


Fig. 8 Numerical index for vacancy density evolution of patterns having single via landing upon large metal lead center (Fig. 2(a)) and edge (Fig. 2(c))

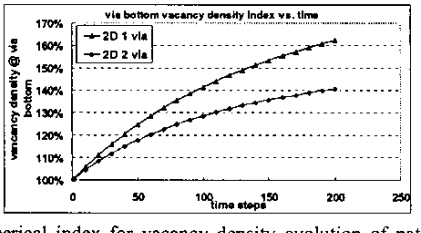


Fig 9 Numerical index for vacancy density evolution of patterns having single via (Fig. 2(e)) and dual vias (Fig. 2(f)) landing upon line extension

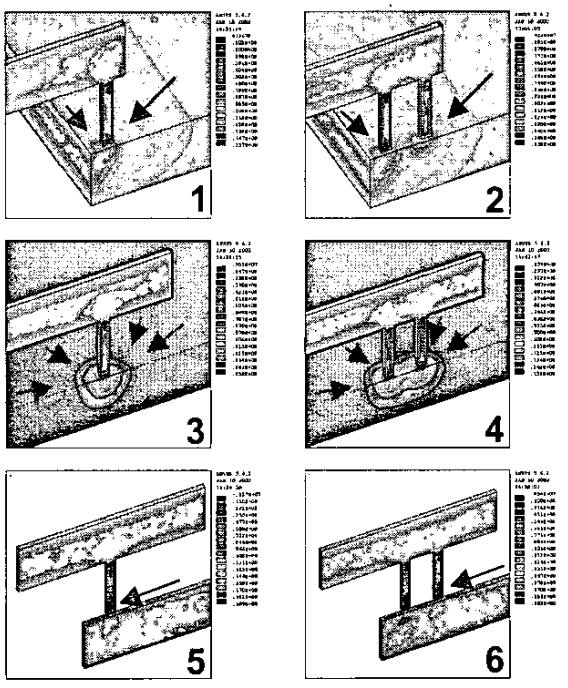


Fig. 10 Local stress distribution of various patterns. (1) single via upon metal edge, (2) dual vias upon metal edge, (3) single via upon metal center, (4) dual vias upon metal center, (5) single via upon line extension, (6) dual vias upon line extension

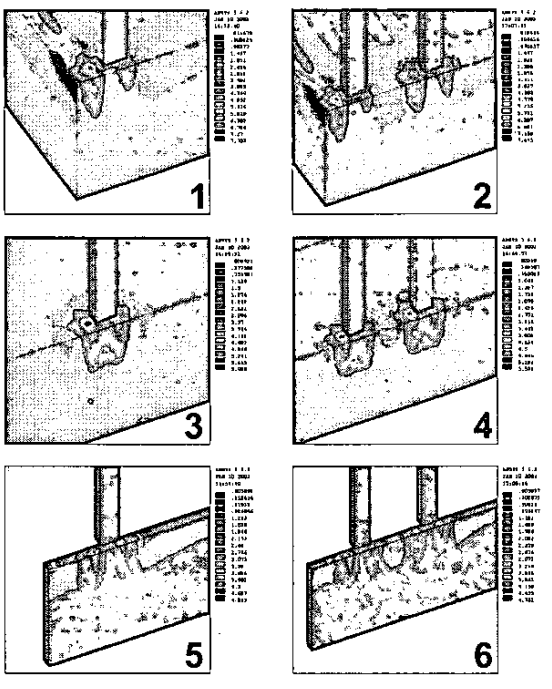


Fig. 11 Contours of the numerical index reflecting the vacancy density. (1) single via upon metal edge, (2) dual vias upon metal edge, (3) single via upon metal center, (4) dual vias upon metal center, (5) single via upon line extension, (6) dual vias upon line extension

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