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INTERFACE

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FROM THE EDITOR

Not Really Farewell Just an (Electro)Migration

This is my farewell message as Editor of *Interface*. I am relinquishing my editorship in order to fully assume my duties as a vice-president of ECS. I have edited 15 issues of Interface including this one featuring the Electrodeposition Division—one for each of the twelve Divisions and one Group; plus two special issues, one in which the 50th anniversary of the transistor was commemorated, and one to celebrate the first five years of *Interface*. I have enjoyed working with all the authors who have contributed to *Interface* and enjoyed learning the latest science and technology of interest to the featured Division/Group. I have learned much about the publishing of a magazine, particularly from Mary Yess, the ECS Director of Publications and *Interface's* Managing Editor. It is Mary's expertise that makes you want to turn the pages from the stunning cover artwork (from O&Y Design), through the articles, to the back cover. I certainly have had some fun writing these columns.

It seems fitting that my last issue of *Interface* features the Electrodeposition Division. This is a Division in which I have been very involved as an ad hoc member of its Executive Committee for a number of years and as a co-chair of several symposia sponsored by the Division. It's an exciting time for us electroplaters, particularly when you see the type of interesting materials and applications for the "old art" of electrodeposition. The articles in this issue highlight several new developments, such as the electroplating of dual Damascene copper interconnections for integrated circuitry; the electrodeposition of nanostructures such as multilayers, nanowires, and single electron transistors; and use of scanning tunneling microscopy to monitor electrodeposition and even to structure surfaces. As a member of this community, I found the advances made by my colleagues to be astounding. It's indeed an exciting and surprising time for electrodeposition!

Now the excitement comes from learning my new job as an ECS vice-president. Presently, I am actively involved in the planning of the two ECS meetings over which I will preside: the next joint meeting with ISE in San Francisco in September 2001 and the Centennial meeting in May 2002 in Philadelphia. So my face may yet appear in *Interface* in Meeting Highlights or in 2001 in the "From the President" column.

This is not a farewell really, but more of an "electromigration" for me. As I leave my editorship, my friends and other members of the ECS need not fear finding something they said to me in my column in *Interface!* This doesn't preclude passing on those items to the new Editor of *Interface*. I know the members of the Society will join me in welcoming the new Editor, Krishnan "Raj" Rajeshwar; and I hope he enjoys the experience as much as I have.

Jan B. Talbot

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Editor

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Fax (609) 737-2743
E-mail: publications@electrochem.org
ECS Home Page: http://www.electrochem.org

Editor: Jan B. Talbot
e-mail: jtalbot@ucsd.edu

Contributing Editor: Vicki Edwards

Managing Editor: Mary E. Yess
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Copper On-Chip Interconnections

A Breakthrough in Electrodeposition to Make Better Chips

by Panos C. Andricacos

On-chip interconnections comprise a multilevel structure of fine wiring located on the top of the transistor circuitry of logic or memory chips, whose role is to connect circuits together as shown in Fig. 1. To avoid significant degradation of circuit speed, on-chip interconnections should permit rapid signal transmission among the various parts of the circuitry. Ever since the development of the integrated circuit about 40 years ago, the most pervasively used materials for the fabrication of the wiring structure have been aluminum as the conductor (or more recently an aluminum-copper alloy for better reliability)[1] and silicon dioxide as the insulator. The transition to copper as the conductor and to a better insulator[2] began with IBM's announcement in September 1997[3] and product shipment since June 1998. This signals one of the most important changes in materials that the semiconductor industry has experienced since its creation. Copper metallization was implemented first since significant gains can be obtained by copper alone.

It is often stated that the three major challenges in the implementation of copper have been: (1) the method of depositing; (2) patterning the metal; and (3) finding a suitable barrier material that prevents the copper metal from diffusing into the insulator material. Although this generalization neglects the enormous integration and manufacturing challenges, it serves to highlight the fact that a combination, equivalent to blanket sputter deposition and reactive ion etching (RIE) technology used to deposit and pattern aluminum, was not available for copper. It is precisely this technological challenge that was met by electrodeposition used in a process-integration approach called Damascene[4] because of its resemblance to an ancient method of metal inlaying.

Thus, electrodeposition, a technology frequently considered to be more of an art than a science, has been able to serve successfully the needs of one of the most technologically advanced areas.

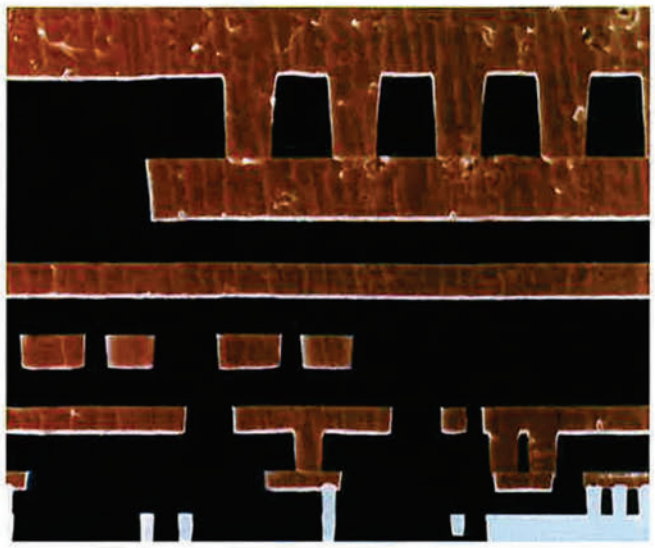


FIG. 1. Cross section of a 6-level copper wiring structure fabricated by IBM showing wiring hierarchy.

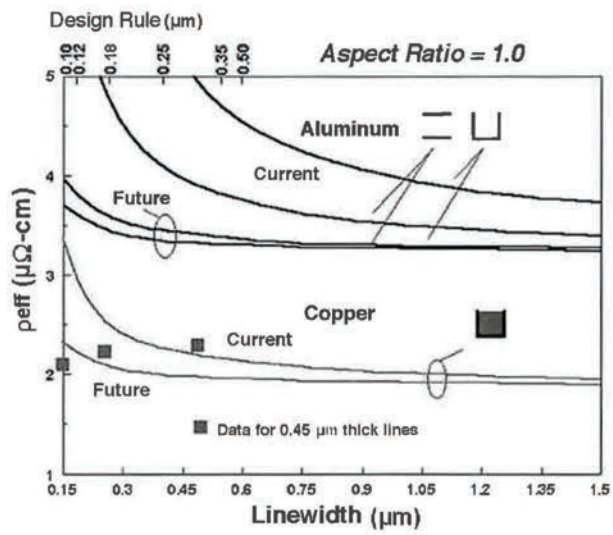


FIG. 2. Effective resistivities for aluminum and copper interconnects as functions of linewidth and design-rule generation; computational results (solid lines) have been obtained for various combinations of conductor material and barrier location shown in the right side of the figure; experimental points correspond to published results from real structures. (Copyright 1995 International Business Machines Corporation. Reprinted with permission of the IBM Journal of Research and Development, *Volume 39, Number 4.)*

History of Technology Development

Although it is indeed very early for one to discuss the history of an event whose initial phases are just unfolding, sufficient information has been published[5] to warrant a brief review of the events that lead to the announcement in September 1997.

At IBM, various forms of physical vapor deposition (including sputtering, dep-etch, electron cyclotron resonance, reflow), chemical vapor deposition (CVD), and electroless plating, were all being examined initially as potential methods of depositing copper. Electrolytic copper was simply not on the horizon. It only existed as a possibility in the minds of a very small group of researchers who had conceptualized the phenomenon of superfilling, a phenomenon that makes it possible to fill

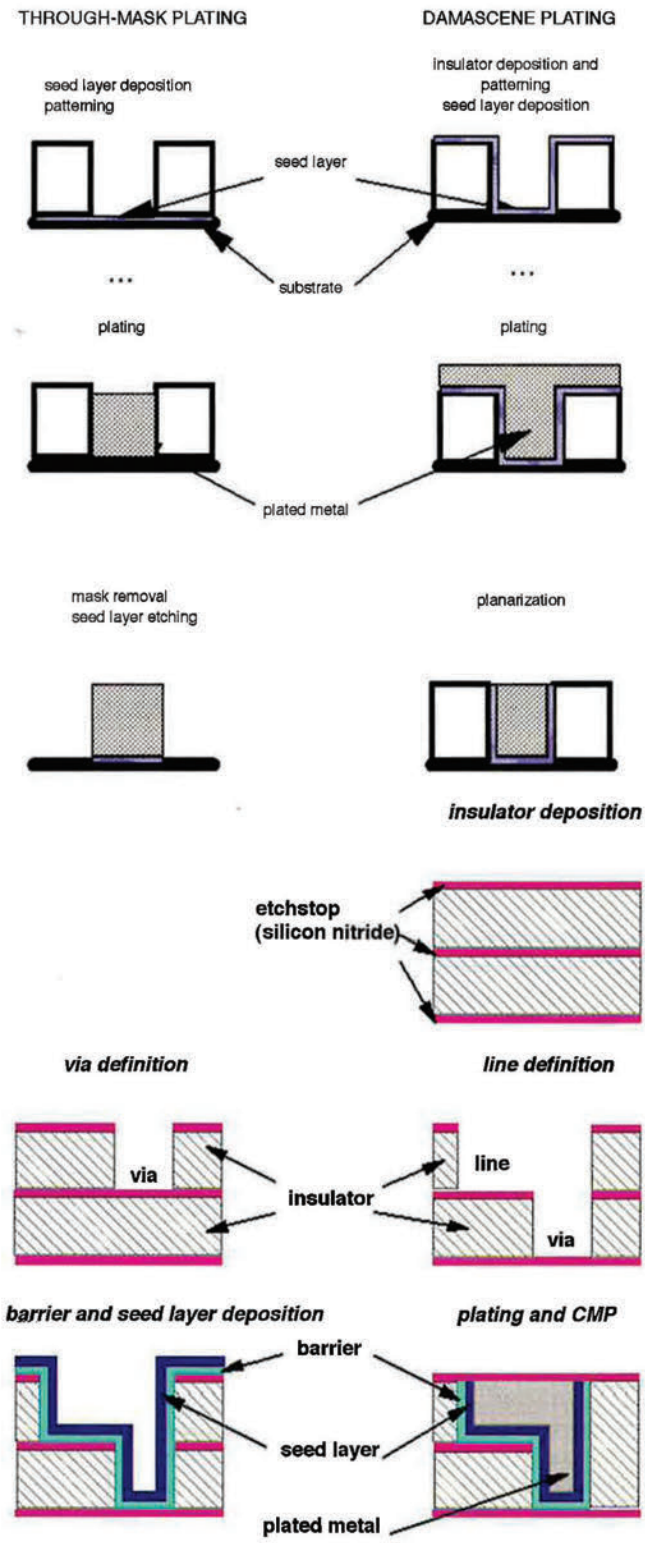


FIG. 3. Comparison of through-mask-plating and Damascene-plating integration steps (top); dual Damascene step sequence (bottom). (Copyright 1998 International Business Machines Corporation. Reprinted with permission of the IBM Journal of Research and Development, *Volume 42, Number 5.)*

submicron Damascene structures without defects.[6] It turns out that superfilling is an attribute unique to electrodeposition and thus played the key role in the success of the technology. The first Damascene-copper wafers were electroplated toward the end of 1989 and the beginning of 1990. It only took a few months for the copper integration team to realize that electroplated copper was the way to go because it delivered the best quality copper of all methods that were being evaluated at the time. It also offered potential for throughput improvement and cost reduction. The summer of 1991 was a period of intense plating effort; this led to the formal adoption of plating later that year as the fabrication method of a bipolar device that was part of IBM's semiconductor product plans at the time.

Copper chip interconnect technology went through a period of near extinction two years later as a result of several direct and indirect factors that were at play in the 1993-1994 timeframe. For one thing, the focus of research was on the use of polyimide as the insulator with copper, adopted in an effort to change both conductor and insulator simultaneously. Results of a 4-level copper/polyimide wiring structure were published in 1994[7] without specifying that the method of copper deposition was electroplating. Despite the scientific accomplishment of fabricating the 4-level structure, the prospect of its implementation in manufacturing was bleak because of the softness of the polyimide material and other reliability and manufacturability issues. At the same time, IBM was experiencing a fundamental change in orientation away from bipolar devices and toward CMOS chip technology. These factors, together with the adverse business environment that prevailed in the company at the time, cast a shadow on the copper program; and were it not for the value of the technology, it might have been extinguished.

The program was revived in 1994 and adapted to CMOS manufacturing. By then, the need for polyimide was rescinded in favor of the more reliable and better understood SiO_2. A hierarchical scaling strategy was developed to better optimize the interconnect resistance and capacitance for CMOS by leveraging the copper properties. Dual-Damascence integration was adopted for cost reduction, manufacturability, and extensibility. In the same timeframe, the project was moved from research to development, design rules were devised and released, and chip design with copper started in earnest. As a direct result of the success of the first reliability stressing of prototype Cu/SiO_2 dual-Damascene chips, copper was adopted as the plan of record for the next CMOS generation. These events caused a continued effort in electroplating development focusing on: (1) the infrastructure for a plating tools capable of handling a

high throughput of 200 mm wafers, and (2) the detailed integration of electroplating technology together with all other fabrication technologies to produce high reliability interconnect structures. Both were successful. Fabrication of copper/silicon dioxide wiring structures and performance of resulting devices were described in detail in 1997.[8] Copper on-chip interconnection technology entered high-volume manufacturing in 1998 at IBM's plant at Burlington, Vermont.

Advantages of Copper Interconnections

The advantages of copper interconnections have been described in detail by Edelstein.[9-11] The factors that contribute to logic gate delay were examined. The need for *"hierarchical wiring"* structures was indicated where the lower wiring levels are at a minimum possible pitch and thickness to minimize capacitance and maximize wiring density, while the higher wiring levels are scaled horizontally and vertically to maintain a constant capacitance while reducing resistance. In addition to the low capacitance (C) and low resistance (R) wires, the hierarchy allows for low-RC wires of intermediate dimensions. Typical width for the low-lying wires is about 0.25 micrometers, while it can increase by an order of magnitude for high-lying wires.

A reduction in the wiring resistance by as much as 45% can be accomplished when the interconnect metallurgy uses copper as the core material. This has a significant impact not only on the resistance of the "fat" wiring, but also (indirectly) on the capacitance of the "thin" wiring whose dimensions can be scaled smaller. This allows an additional benefit in reduction of crosstalk, which is difficult to quantify in general, but has already led to significant benefits in noise-related chip design and performance results.

It is important to note that wire resistance must take into account not only the core material of the interconnect (Al(Cu) or Cu), but also any other (usually higher resistivity) materials used to surround the core material. Edelstein makes the comparison (as shown in Fig. 2) between Al(Cu) wires made by RIE that have bottom and top Ti layers (which, during sintering, produce $TiAl_3$ with a resistivity of about 35 μΩ-cm and 3.5 times the original Ti thickness), and Cu wires made by a Damascene process (described below) that leaves cladding on the bottoms and the sides of the lines. The cladding also has high resistivity but does not react with Cu and serves as a diffusion barrier and an adhesion layer. It is clear from Fig. 2 that copper offers a very significant reduction in the effective resistivity for both current and future scenarios over aluminum.

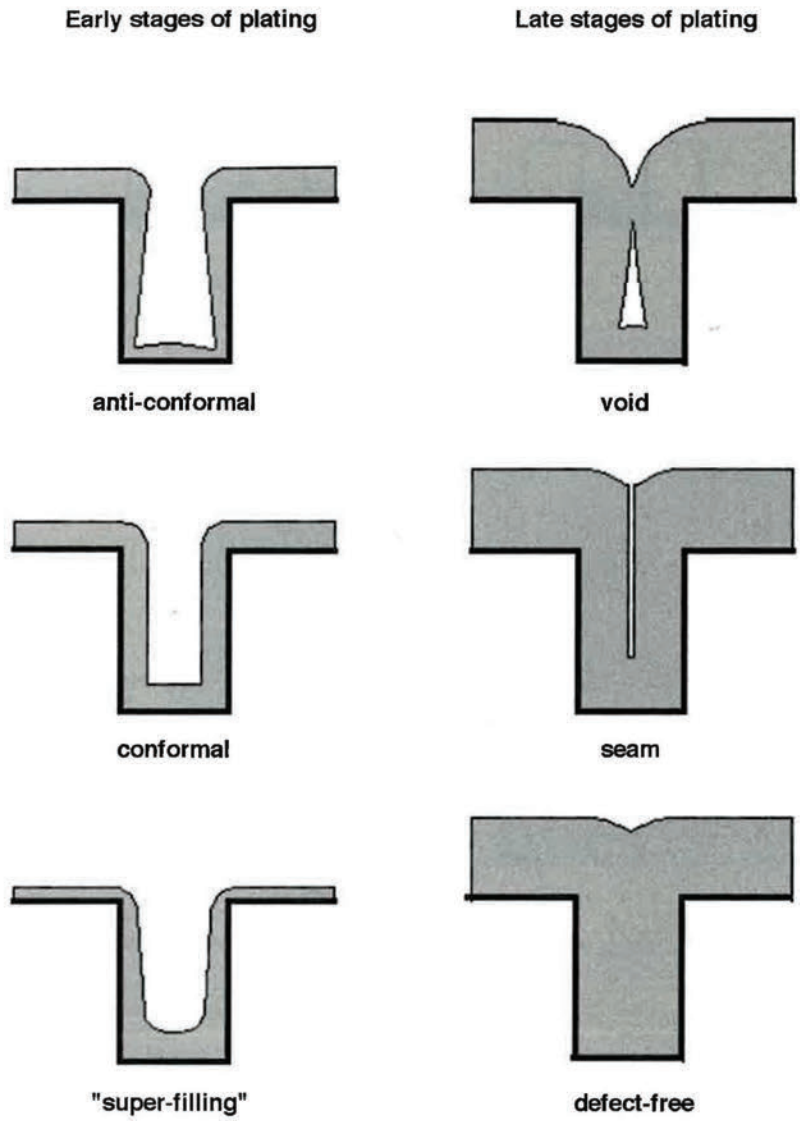
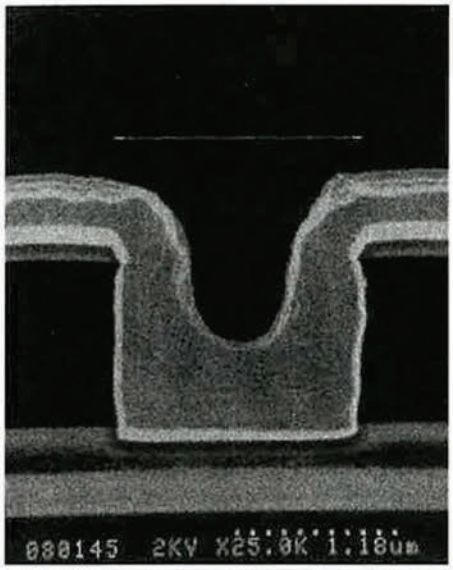


FIG. 4. Types of profile evolution in Damascene plating (Copyright 1998 International Business Machines Corporation. Reprinted with permission of the IBM Journal of Research and Development, *Volume 42, Number 5.)*

In addition to resistance reduction, Edelstein cites two other primary advantages of copper interconnection technology: high electromigration resistance and amenability to dual Damascene processing. Electromigration causes the diffusive transport of conductive material as a result of the momentum transfer by the passage of extremely high electron current densities. Atoms are being driven in the direction of the *"electron wind"* causing the cathodic end of the wire to become depleted and ultimately resulting in the formation of voids. Scaling of low-lying wires to reduce capacitance and to increase wiring density as mentioned above, as well as the inexorable trend to higher performance and transistor current-drives, leads to increased current densities. For this reason, an extendible conductor metallurgy must survive stringent electromigration tests. In addition to electromigration, stress voiding, mass transport resulting from thermally-induced stress gradients, is another reliability concern. Electromigration tests of 0.3 μm lines conducted at an elevated temperature (295°C) and a stress current of 2.5 million A/cm^2 showed a T_{50} lifetime (the time interval needed for 50% of the devices tested to fail) that was more than 100 times longer for Cu than Ti/Al(Cu)/Ti lines. Excellent results were obtained for stress migration testing.[8] Both sets of



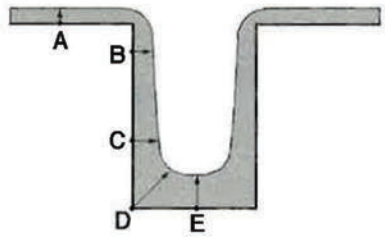


FIG. 5. (left) Cross-section of a partially-filled line showing the profile of electroplated copper that exhibits the superfilling phenomenon (Copyright 1998 International Business Machines Corporation. Reprinted with permission of the IBM Journal of Research and Development, *Volume 42, Number 5); (right) variation of electrodeposition rate along the line profile.*

results argue strongly in favor of the extendibility of copper interconnections to higher usable current densities and better overall performance.

The other primary advantage of copper interconnections in Edelstein's analysis, namely amenability to dual Damascene processing, relates to the manner that electroplating is integrated with other deposition, removal, patterning, and lithographic processes used in the fabrication of the device. Integration places tremendous requirements on the way electrodeposition is carried out.

Integration of Electroplating Processes

Because current must be conducted to the entire wafer surface for electroplating to occur at all points, a seed layer is usually deposited in a blanket fashion prior to the electroplating step by a process such as sputtering (Fig. 3). In Damascene processing, the seed layer is deposited on top of the patterned substrate and therefore, electroplating occurs everywhere, inside and outside features, from the bottom upward and from the sides inward. There are good reasons for adopting a Damascene process of integration. A barrier is usually required to prevent interaction between the conductor and the insulator and to provide good adhesion between the two. A via level and a trench level can be metallized and planarized simultaneously (dual Damascene process), thus saving in fabrication costs (Fig. 3). The requirement of a barrier layer and amenability to dual-level fabrication are some of the advantages of a Damascene process of integration.

Damascene electroplating as applied to the process of making copper on-chip interconnections, represents a deviation from another popular method of integrating electroplating called "through-mask plating." Here, the seed layer is deposited again over the wafer surface prior to patterning. Electroplating occurs only in those lithographic areas that are not covered by the masking material. Through-mask plating has been used extensively in the fabrication of inductive recording heads and in other applications.[12-14]

Both through-mask and Damascene electroplating require post-electrodeposition steps for the metallization process to be completed. In through-mask plating, the seed layer remains in place after completion of the plating step and must be removed by a dry or wet etching process. In a Damascene process, excess material is deposited on top of the useful wiring structure (called "overburden") and must be removed by a planarization process called chemical mechanical planarization (CMP).

The foremost challenge in Damascene plating is to fill vias, holes, trenches, and their combinations completely, without voids or seams. Figure 4 shows possible ways for the profile of plated copper to evolve in time. In conformal plating, a deposit of equal thickness at all points of a feature leads to the creation of a seam, or if the shape of the feature is reentrant, a void. Subconformal plating leads to the formation of a void even in straight-walled features. Subconformal plating results when substantial depletion of the cupric ion in the plating solution inside the feature leads to significant concentration overpotentials which, in turn, cause the current to flow preferentially to more accessible locations outside the feature. Also, if the feature depth is large (say in excess of 50 μm), the ohmic drop in the electrolyte may cause nonuniformity in the distribution of the current in favor of external feature locations. For defect-free filling, an increasing deposition rate along the sides and the bottom of the feature is desired.

As early as 1990, at IBM, we discovered that plating from certain plating solutions that contain additives leads to this superconformal deposition behavior that eventually produces void-free and seamless structures (Fig. 5). We call this behavior "superfilling."[6]

Superfilling

Superfilling can be understood by comparing deposition rates at different points along the feature profile, as shown in Fig. 5. The most noticeable difference may occur between points A and E. However, we consider the difference between points B and C, i.e., two points at different elevations on the side wall, to be a more fundamental determinant of superfilling, especially in high-aspect-ratio cavities. Since any two points are electrically shorted by the seed layer in the solid phase, the difference in total overpotential, $\Delta\eta = \eta^B - \eta^C$, must be equal to 0. The difference in total overpotential can be written as the sum of the difference in ohmic drop in the electrolyte, $\Delta\phi_\Omega$, plus the differences in concentration and surface overpotentials, $\Delta\eta_C$ and $\Delta\eta_S$, respectively. Thus, $\Delta\phi_\Omega + \Delta\eta_C + \Delta\eta_S = 0$. Because the feature is small (typically submicron), the difference in ohmic drop in the electrolyte $\Delta\phi_\Omega$ is negligible (on the order of one microvolt). The situation here is very different from the one that prevails in through-hole plating, where the ohmic drop in the electrolyte is substantial because the holes are typically tens of micron in depth. Assuming further that the difference in the cupric ion concentration is negligible (an assumption whose validity obviously diminishes with increasing aspect ratio and decreasing feature size), the difference in concentration overpotential becomes negligible, $\Delta\eta_C \sim 0$. One finally obtains that $\Delta\eta_S \sim 0$. Writing the surface overpotential in terms of a Tafel expression, it follows that $RT/\alpha F \ \ln \ i^B/i^B_0 = RT/\alpha F \ \ln \ i^C/i^C_0$, where i_0 is the exchange current density, α is the cathodic transfer coefficient, and, i is the current density (proportional to the rate of copper

deposition by Faraday's law). Assuming that the exchange current density is lower with a higher flux of additives, it follows that $i^B_0 < i^C_0$ simply because point B is more accessible to additive diffusion than point C. It follows that $i^B < i^C$, i.e. the rate of copper deposition is higher at point C.

We have developed a rigorous numerical model for superfilling.[6] Three coupled differential equations (the Laplace equation for the potential in the plating solution and the diffusion equations for the concentrations of the cupric ion and the additive) are solved numerically under the assumption that the additive in under mass-transport control. It is further assumed that the additive flux inhibits the kinetics of the copper-deposition reaction according to an empirical expression. A comparison of model predictions with experimental results have been published.[6] Extensibility of electroplating has been demonstrated down to 0.1 μm trenches.[15] It appears that superfilling is operational over a wide range of dimensions. (Note that superfilling is distinctly different from leveling. Leveling reduces the surface roughness and smooths defects such as scratches; superfilling produces void-free and seamless deposits inside lithographically defined cavities with vertical walls and high aspect ratios.)

Material Properties of Electroplated Copper

The material properties of electroplated copper have been the subject of extensive investigation (see, for example, Ref. 16). Recent discussions (especially at the 1998 Advanced Metallization Conference in Colorado Springs) have been centered around a peculiar metallurgical property of thin (on the order of 1 micron) films of electroplated copper whose resistivity after plating is about 20 to 25% higher than the expected resistivity of the metal (about 1.7 μΩ cm). Moreover the resistivity evolves in time decreasing even at room temperature to the expected value over a period of several hours. Although this phenomenon has been observed in the past,[17] renewed interest in it is of course due to the special significance of the conductor resistivity in a wiring structure.

Stress and microstructural measurements in unpatterned films revealed that the decrease in film resistance is accompanied by an increase in grain size by an order of magnitude and by a decrease in compressive stress to near zero values,[18]

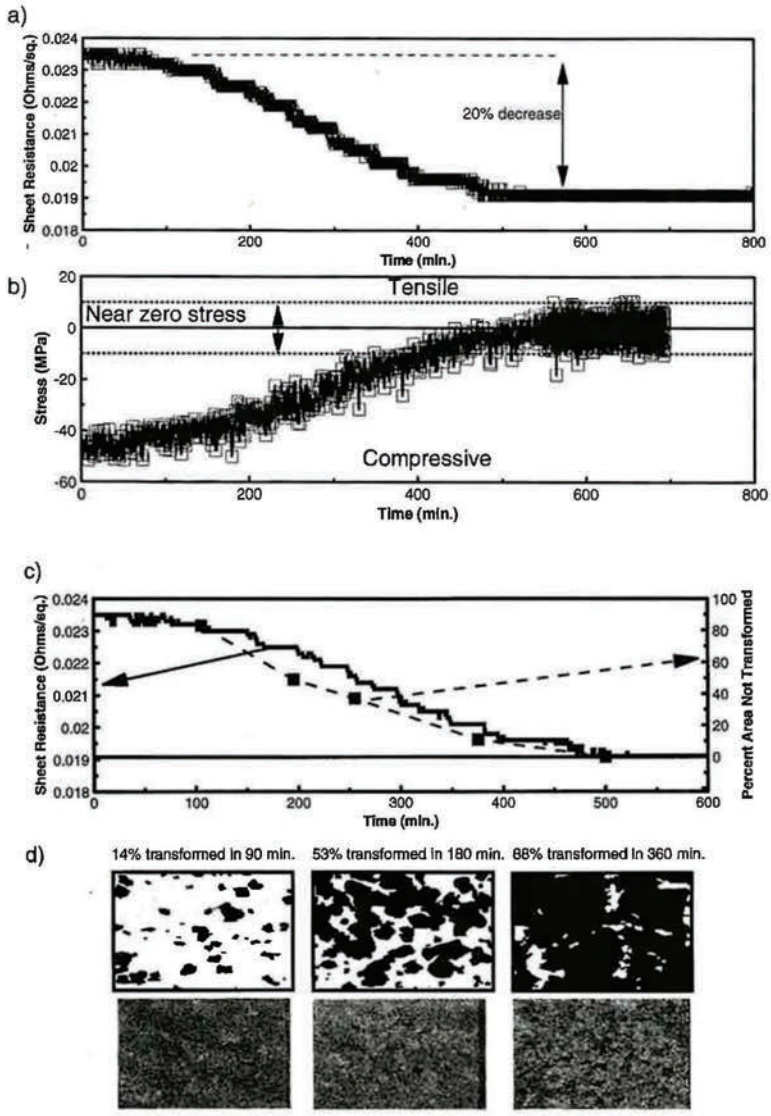


FIG. 6. Variation of (a) sheet resistance and (b) stress of electroplated copper as function of time elapsed since the end of plating at room temperature. These phenomena correlate with an increase in grain size; (c) the percentage of non-recrystallized copper as a function of time; (d) focus ion beam images and maps showing the areas of recrystallization. (Reprinted, with permission, from The Materials Research Society Conference Proceedings *V-14, p. 81).*

as shown in Fig. 6. Observation of grain growth in patterned films revealed that points of initiation are found close to the edges of features, where defect density and stress are probably the highest.[19] The high resistance of the as-deposited film is probably due to grain boundary electron scattering; stress relaxation is also consistent with grain boundary elimination. Elimination of defects has also been proposed to play a role in the reduction of the resistivity and stress. The activation energy for the grain growth and defect elimination processes has been found to be about 0.92 eV, comparable to the value measured for copper grain boundary diffusion.

It is expected that research in this area will continue, because the room-temperature microstructural transformation of electroplated copper may have direct bearing on the most significant material and reliability properties of the copper conductor. Research in other properties of the materials involved in chip interconnections is also expected to intensify in the near future as the technology implementation advances.

Electroless Plating

No discussion of the role of electrochemistry on copper on-chip interconnections can be complete without reference to the role electroless plating has played in the development of the technology. Electroless copper plating,

a technology already used in electronic packaging, has been used in the fabrication of copper on-chip interconnects to fill features.[20-25] Although potentially a low cost process because of its batch nature, it lost ground to electrolytic plating because of concerns due to hydrogen evolution, complexity in process control, low deposition rates, and potentially adverse environmental impact. Electroless plating of CoWP alloys (on sputtered Co) followed by electroless Cu plating has also been reported;[26] the Co alloy acts as a diffusion barrier/adhesion layer and the electroless Cu metal is the conductor. By combining these electroless steps, a potentially simpler process with fewer steps and simpler tools may result. It is possible that electroless plating processes will offer significant advantages for future wiring structures with improvements in sophistication and understanding.

Summary

Copper on-chip interconnections represent not only a change in materials but also new ways of integration and depositing the conductor metal. Copper interconnections are superior to Al(Cu) interconnections because of the decreased resistance, improved reliability and reduced process complexity. Electrodeposition has played a key role in making implementation of the technology possible because it can deposit copper in Damascene structures without defects such as seams or voids. This unique property of electrodeposition is due to a phenomenon called "superfilling," in which the rate of the copper deposition reaction increases down into a feature as a result of the differential inhibition of the reaction kinetics by the additives present in the plating solution. Because of its unique advantages and superior performance, electrodeposition is being adopted by the entire semiconductor industry as the method of choice for depositing the copper conductor for on-chip interconnections. ■

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References

1. C.- K. Hu, K. P. Rodbell, T. D. Sullivan, K. Y. Lee, and D. P. Boulder, *IBM J. Res. Develop.*, **39**, 465 (1995); I. Ames, F. M. d'Heurle, and R. E. Horstman, *IBM J. Res. Develop.*, **14**, 461 (1970).
2. See for example B. Zhao, D. Feiler, V. Ramanathan, Q. Z. Liu, M. Brongo, J. Wu, H. Zhang, J. C. Kuei, D. Young, J. Brown, C. Vo, W. Xia, C. Chu, J. Zhou, C. Nguyen, L. Tsau, D. Dornisch, L. Camilletti, P. Ding, G. Lai, B. Chin, N. Krishna, M. Johnson, J. Turner, T. Ritzdorf, G. Wu, and L. Cook, *Electrochemical and Solid-State Letters*, **1**, 276 (1998).
3. L. Zuckerman, *"IBM to Make Smaller and Faster Chips - Second Breakthrough in a Week Has Wide Uses," The New York Times*, D1, Monday, September 22 ,1997.
4. M. M. Chow, J. E. Cronin, W. L. Guthrie, W. Kaanta, B. Luther, W. J. Patrick, K. A. Perry, and C. L. Standley, U.S. Pat. No. 4,789,648 (1988).
5. P. Gwynne, *IBM Research*, **4**, 17 (1997).
6. P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, *IBM J. Res. Develop.*, **42**, 567 (1998).
7. B. Luther, J. F. White, C. Uzoh, T. Cacouris, J. Hummel, W. Guthrie, N. Lustig, S. Greco, N. Greco, S. Zuhoski, P. Agnello, E. Colgan, S. Mathad, L. Saraf, E. J. Weitzman, C. K. Hu, F. Kaufman, M. Jaso, L. P. Buchwalter, S. Reynolds, C. Smart, D. Edelstein, E. Baran, S. Cohen, C. M. Knoedler, J. Malinowski, J. Horkans, H. Deligianni, J. Harper, P. C. Andricacos, J. Paraszczak, D. J. Pearson, and M. Small, *Proceedings of the 10th International IEEE VLSI Multilevel Interconnection Conference*, p. 15 (1993).
8. D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt, W. Motsiff, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz, L. Su, S. Luce, and J. Slattery, *Tech. Digest IEEE Int. Electron Devices Mtg.*, p. 773, (1997).
9. D. C. Edelstein, G. A. Sai-Halasz, and Y. -J. Mii, *IBM J. Res. Develop.*, **39**, 383 (1995).
10. D. C. Edelstein, *Proceedings of the 12th International IEEE VLSI Multilevel Interconnection Conference*, p. 301 (1995).
11. D. C. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt, A. Stamper, W. Motsiff, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, P. McLaughlin, T. Katsetos, R. Schulz, L. Su, N. Rohrer, and S. Luce, *Realize Inc.*, Tokyo, p. 207 (1998).
12. P. C. Andricacos and L. T. Romankiw, *in Advances in Electrochemical Science and Engineering*, Vol. 3, H. Gerischer and C. W. Tobias, Eds., p. 227, VCH, New York (1993).
13. M. Datta, R. V. Shenoy, C. Jahnes, P. C. Andricacos, J. Horkans, J. O. Dukovic, L. T. Romankiw, J. Roeder, H. Deligianni, H. Nye, B. Agarwala, H. M. Tong, and P. Totta, *J. Electrochem. Soc.*, **142**, 3779 (1995).
14. P. C. Andricacos, J. H. Comfort, A. Grill, D. E. Kotecki, V. V. Patel, K. L. Saenger, A. G. Schrott, U.S. Pat. No. 5,789,320 (1998).
15. C.-K. Hu, K. Y. Lee, L. Gignac, S. M. Rossnagel, C. Uzoh, K. Chan, P. Roper, and J. M. E. Harper, in *Advanced Interconnects and Contact Materials and Processes for Future Integrated Circuits, Materials Research Society Symposium Proceedings Volume*, **514**, p. 287 (1998).
16. W. H. Safranek, *The Properties of Electrodeposited Metals and Alloys*, Second Edition, The American Electroplaters and Surface Finishers Society, Orlando, Florida (1986).
17. A. Gangulee, *J. Appl. Phys.*, **43**, 867 (1972).
18. C. Cabral, Jr., P. C. Andricacos, L. Gignac, I. C. Noyan, K. P. Rodbell, T. M. Shaw, R. Rosenberg, and J. M. E. Harper, *Room Temperature Evolution of Microstructure and Reactivity in Electroplated Copper Films*, Abstracts of the Advanced Metallization Conference (AMC), Colorado Springs, Colorado, October 6-8, 1998.
19. C. Lingk and M. E. Gross, *J. Appl. Phys.*, **84**, 5547 (1998).
20. C. H. Ting and M. Paunovic, U.S. Pat. 5,169,680 (1998).
21. M. Paunovic, in *Electrochemistry in Transition*, O. J. Murphy, S. Srinivasan, and B. E. Conway, Eds., p. 479, Plenum Press, New York (1992).
22. R. Jagannathan and M. Krishnan, *IBM J. Res. Develop.*, **37**, 117 (1993).
23. Y. Shacham-Diamand, in *Proceedings of the Second Symposium on Electrochemically Deposited Thin Films II*, M. Paunovic, Ed., PV 94-31, p. 295, The Electrochemical Society Proceedings Series, Pennington, NJ (1994).
24. M. Paunovic and M. Schlesinger, *Fundamentals of Electrochemical Deposition*, John Wiley, New York (1998).
25. S. Lopatin, Y. Shacham-Diamand, V. Dubin, P. K. Vasudev, J. Pellerin, and B. Zhao, in *Electrochemical Synthesis and Modification of Materials*, P. C. Andricacos, S .G. Corcoran, J-L. Delplancke, T. P. Moffat, and P. C. Searson, Eds., Volume 452, p. 463, Materials Research Society Symposium Proceedings Volume (1997).
26. S. Lopatin, Y. Shacham-Diamand, V. Dubin, P. K. Vasudev, J. Pellerin, and B. Zhao, in *Electrochemical Synthesis and Modification of Materials*, P. C. Andricacos, S. G. Corcoran, J-L. Delplancke, T. P. Moffat, and P. C. Searson, Eds., Materials Research Society Symposium Proceedings Volume **451**, p. 463 (1997).

About the Author

***Panos C. Andricacos** is manager of the Plating Technology and Materials group at IBM Thomas J. Watson Research Center. He has worked on the application of electrochemical processes in logic, memory storage, packaging and C4 technology, and has played a key role in the development of copper electroplating for chip metallization.*