

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

IPR2025-01212

U.S. Patent No. 7,439,623

**DECLARATION OF DR. REINHOLD DAUSKARDT IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,439,623**

TABLE OF CONTENTS

I.	INTRODUCTION	11
II.	BACKGROUND AND QUALIFICATIONS	12
	A. Education and Career	12
	B. Publications	16
	C. Compensation	18
III.	MATERIALS REVIEWED	19
IV.	LEGAL STANDARDS	19
	A. Anticipation	19
	B. Obviousness	20
V.	LEVEL OF ORDINARY SKILL IN THE ART	25
VI.	TECHNOLOGY BACKGROUND	25
	A. Interconnects and Dual Damascene	26
	B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength	29
VII.	THE '623 Patent	30
	A. Overview	30
	B. Prosecution History	32
	C. Claim Construction	33
VIII.	PRIOR ART	33
IX.	SUMMARY OF PRIOR ART REFERENCES	34
	A. Watanabe – U.S. Patent App. Pub. No. 2003/0116852	34
	B. Hasunuma – U.S. Patent App. Pub. No. 2004/0113238	47
	C. Aoyagi – U.S. Patent App. Pub. No. 2001/0019180	50

D.	Kunikiyo – U.S. Patent No. 6,717,267.....	57
E.	Kurashima – U.S. Patent No. 7,042,099	59
F.	Iizuka – U.S. Patent No. 5,250,465	61
G.	Kamoshima – U.S. Patent App. Pub. No. 2004/0173905	62
X.	CLAIMS 1-4, 7-9, 11-18, 21-22, 25-26, 28, 32, 39-40, 42, and 45-47 ARE UNPATENTABLE.....	64
A.	Ground 1: Watanabe Anticipates Claims 1-3, 7, 11-16, 21-22, 25-26, 28, 32, 39-40, 42	65
1.	Claim 1	65
2.	Claim 2.....	90
3.	Claim 3 – “semiconductor device of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect”	98
4.	Claim 7 – “semiconductor device of claim 2, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film”	99
5.	Claim 11 - “semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO ₂ film”	102
6.	Claim 12 – “semiconductor device of claim 1, wherein the second interconnect includes a first barrier film and a first conductive film”	105
7.	Claim 13 - “semiconductor device of claim 12, wherein the first conductive film includes copper”	106

8.	Claim 14 - “semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode”	106
9.	Claim 15	111
10.	Claim 16 – “semiconductor device of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect”	114
11.	Claim 21 – “semiconductor device of claim 1, wherein the first interconnect and the second interconnect extend in a same direction”	115
12.	Claim 22 – “semiconductor device of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends”	118
13.	Claim 25 – “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less”	121
14.	Claim 26 – “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 1 μm or less”	124
15.	Claim 28 – “semiconductor device of claim 1, wherein the dummy via is provided in plural”	125
16.	Claim 32 – “semiconductor device of claim 1, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect	

	<i>and shorter than a distance between the via and the other end of the second interconnect”</i>	126
17.	Claim 39 – “ <i>semiconductor device of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film</i> ”	130
18.	Claim 40 – “ <i>semiconductor device of claim 1, wherein the dummy via and the second interconnect include a Cu film</i> ”	131
19.	Claim 42 – “ <i>semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film</i> ”	132
B.	Ground 2: Claims 4 and 8 Are Obvious Over Watanabe and Kurashima	136
1.	Claim 4 – “ <i>semiconductor device of claim 2, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other</i> ”	137
2.	Claim 8 – “ <i>semiconductor device of claim 2, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle</i> ”	142
C.	Ground 3: Claims 9 and 17-18 Are Obvious Over Watanabe and Iizuka	147
1.	Claim 9	148

2.	Claim 17 – “ <i>semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view</i> ”	154
3.	Claim 18 – “ <i>semiconductor device of claim 17, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other</i> ”	156
D.	Ground 4: Claims 45-47 Are Obvious Over Watanabe and Kamoshima.....	157
1.	Claim 45	158
2.	Claim 46 – “ <i>semiconductor device of claim 45, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions</i> ”	169
3.	Claim 47 – “ <i>semiconductor device of claim 45, wherein a width of the second interconnect portion is 0.2 μm or less</i> ”	172
E.	Ground 5: Hasunuma Anticipates Claims 1, 11-15, 17-18, 21-22, 25-26, 28, 32, and 39-40	174
1.	Claim 1	174
2.	Claim 11 – “ <i>semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film</i> ”	188
3.	Claim 12 – “ <i>semiconductor device of claim 1, wherein the second interconnect includes a first barrier film and a first conductive film</i> ”	190

4.	Claim 13 – “semiconductor device of claim 12, wherein the first conductive film includes copper”	190
5.	Claim 14 – “semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode”	191
6.	Claim 15	193
7.	Claim 17 – “semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view”	195
8.	Claim 18 – “semiconductor device of claim 17, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other”	197
9.	Claim 21 – “semiconductor device of claim 1, wherein the first interconnect and the second interconnect extend in a same direction”	198
10.	Claim 22 – “semiconductor device of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends”	201
11.	Claim 25 – “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less”	202
12.	Claim 26 – “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 1 μm or less”	205

13.	Claim 28 – “ <i>semiconductor device of claim 1, wherein the dummy via is provided in plural</i> ”	206
14.	Claim 32 – “ <i>semiconductor device of claim 1, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect and shorter than a distance between the via and the other end of the second interconnect</i> ”	207
15.	Claim 39 – “ <i>semiconductor device of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film</i> ”	209
16.	Claim 40 – “ <i>semiconductor device of claim 1, wherein the dummy via and the second interconnect include a Cu film</i> ”	211
F.	Ground 6: Claims 2 and 8 Are Obvious Over Hasunuma and Kurashima	211
1.	Claim 2	211
2.	Claim 8 – “ <i>semiconductor device of claim 2, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle</i> ”	221
G.	Ground 7: Aoyagi Renders Obvious Claims 1, 16, and 45-46.....	224
1.	Aoyagi’s Dual Damascene Teaching	224
2.	Claim 1	227

3.	Claim 16 – “ <i>semiconductor device of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect</i> ”	246
4.	Claim 45	247
5.	Claim 46 – “ <i>semiconductor device of claim 45, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions</i> ”	250
H.	Ground 8: Claim 47 Is Obvious Over Aoyagi and Hasunuma.....	251
1.	Claim 47 – “ <i>semiconductor device of claim 45, wherein a width of the second interconnect portion is 0.2 μm or less</i> ”	251
I.	Ground 9: Claims 1-2, 4, 7, 14, and 42 are Anticipated and Rendered Obvious by Kunikiyo	253
1.	Claim 1	253
2.	Claim 2	270
3.	Claim 4 – “ <i>semiconductor device of claim 2, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other</i> ”	274
4.	Claim 7 – “ <i>semiconductor device of claim 2, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film</i> ”	276
5.	Claim 14 – “ <i>semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode</i> ”	278

6.	Claim 42 – “ <i>semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film</i> ”	280
J.	Ground 10: Claims 9 and 17 Are Obvious Over Kunikiyo and Iizuka	282
1.	Claim 9	282
2.	Claim 17 – “ <i>semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view</i> ”	288
K.	Ground 11: Claim 3 Is Obvious Over Kunikiyo and Watanabe.....	291
1.	Claim 3 – “ <i>semiconductor device of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect</i> ”	292
XI.	Conclusion	299
	EXHIBIT LIST	303
	LIST OF CHALLENGED CLAIMS	307

I, Dr. Reinhold Dauskardt, declare as follows:

I. INTRODUCTION

1. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in connection with a petition for *inter partes* review of U.S. Patent No. 7,439,623 (“’623 patent”), which I understand is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-4, 7-9, 11-18, 21-22, 25-26, 28, 32, 39-40, 42, and 45-47 of the ’623 patent (“Challenged Claims”). These claims of the ’623 patent are included in attached Appendix B.

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the basis for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the ’623 patent is unpatentable for at least the reasons I discuss below.

II. BACKGROUND AND QUALIFICATIONS

A. Education and Career

5. I have summarized in this section my educational background, career history, and other relevant qualifications.

6. My technical background and experience are summarized in my curriculum vitae and listing of publications included below in Appendix C.

7. I am currently the Ruth G. and William K. Bowes Professor of Materials Science and Engineering in the Department of Materials Science and Engineering at Stanford University. I have additional appointments as Professor in the Department of Mechanical Engineering, the Biodesign Institute and in the Department of Surgery, Stanford School of Medicine. I am also a Visiting Professor in the School of Materials Science and Engineering at the Nanyang Technological University in Singapore.

8. I earned a B.Sc. (1980) and M.Sc. (1983) in Physics, Mathematics and Materials from the University of the Witwatersrand, South Africa. Thereafter, I earned a Ph.D. in Materials Science and Engineering from the University of California at Berkeley / University of the Witwatersrand in 1988.

9. Based on my 28 years of experience in the field of materials science, particularly in connection with the thermomechanical reliability and manufacturing processes of microelectronic devices, and based on the acceptance of my

publications and professional recognition by societies in this field, I believe that I am an expert in the technology at issue in this proceeding and am qualified to provide an opinion in this declaration.

10. I have extensive experience in integrating new materials into emerging microelectronic devices and I am an internationally recognized expert on the design and thermomechanical reliability of engineering structures and semiconductor device technologies. My experience includes semiconductor device and packaging processing operations and processing environments (including plasma processing, chemical mechanical planarization, and a wide range of deposition techniques) and their effects on device materials, structures and their properties.

11. I teach several undergraduate and graduate classes in the School of Engineering at Stanford University on materials science topics. These classes include detailed discussions of structure-property relationship of materials, semiconductor device structures, their manufacturing processes and reliability.

12. My interdisciplinary research includes interaction with researchers in academia and industry. I have served as an editor and reviewer for a number of journals and books including Nature, Science, Acta Materialia, the Journal of Applied Physics, and the Journal of Microelectronics and Electronic Packaging. I am a frequent reviewer of proposals for U.S. federal and international funding agencies, I have organized international conferences and symposia in the area of

materials and electronic devices, and have published over 350 articles in the scientific literature.

13. I am a named inventor on over 30 provisional and granted United States patents. I have served as the research advisor of 67 doctoral students who have graduated under my supervision and mentorship and currently have 14 doctoral graduate students in my research group and 2 postdoctoral scholars. I have also supervised the research programs of more than 26 master's students and mentored more than 46 post-doctoral fellows, medical residents and medical fellows along with several visiting scientists and engineers.

14. I am an internationally recognized expert on the semiconductor devices and their manufacturing processes for which I was awarded the prestigious Semiconductor Industry Association University Researcher Award in 2010 for "research which has provided substantive and sustained contributions to semiconductor industry science and technology." This research includes studies of the adhesion and cohesion of interfaces and layers in materials, and the causes and mechanisms of fracture, delamination, stress migration, voiding, fatigue and mechanical reliability of microelectronic devices and their packages, and similar studies of the materials used in the manufacture of electronic device technologies. For my research directed to CMP processing, I was awarded the VLSI/ULSI

Multilevel Interconnection (VMIC) International Conference Award in 2008 for “Optimized Curing and CMP of Nanostructured Ultra-low-k Films,” Fremont, CA.

15. My research group is well known internationally for pioneering studies of the synergistic effects of mechanical forces, chemical environments, temperature and other forms of degradation on thermomechanical stresses and the processes of fracture and defect evolution that determine the reliability of materials and devices. Our experimental studies are complimented with a range of computational and theoretical modelling capabilities.

16. I have won a number of awards including the U.S. Dept. of Energy Outstanding Scientific Accomplishment Award (1989), the Alexander von Humboldt Research Award (2002), the ASM International Silver Medal (2003), an IBM Faculty Award (2006), the TMS Structural Materials Distinguished Scientist/Engineer Award (2010), the Semiconductor Industry Association University Researcher Award (2010), the H. Maso Award for fundamental contributions to skin science (2011), and the IBM Shared University Research Award (2011).

17. I have contributed significantly to leadership in Stanford's multidisciplinary materials and microelectronic device efforts which spans several schools and the Stanford Hospital. I am also a Fellow of ASM International and a Fellow of the American Ceramic Society

B. Publications

18. I have authored over 300 peer-reviewed academic journal publications, and I am a named inventor on at least 7 granted U.S. patents. Some examples of relevant publications to the technology at issue in this proceeding are:

- a) M. Lane, N. Krishna, I. Hashim, and R. H. Dauskardt, “Adhesion and Reliability of Copper Interconnects with Ta and TaN Barrier Layers,” *Journal of Materials Research*, 15 [1] 203-211, 2000.
- b) D. M. Gage, A.D.W. Thiel, R. H. Dauskardt, M. K. Haas, L.M. Matz, M. L. O’Neill, T. M. Wieder, G. Banerjee and M. B. Rao, “Impact of CMP polish and pCMP Cleaning on adhesion of SiCN capping layer on PECVD-derived Porous OSG and Copper” *Solid State Phenomena*, 145-146, 377-380, 2009.
- c) Ryan Birringer, Roey Shaviv, Roy H. Geiss, David Read, and Reinhold Dauskardt, “Effects of Barrier Composition and Electroplating Chemistry on Adhesion and Voiding in Copper / Dielectric Diffusion Barrier Films,” *Journal of Applied Physics*, 110, 044312, 2011.
- d) Qiran Xiao, Brian Watson and Reinhold H. Dauskardt, “Organothioliol-Based Hybrid-Layer Strategy for High-Performance Copper Adhesion and Stress-Migration via Simultaneous Oxide Reduction,” *Advanced Materials Interfaces*, 3, 14, 2016.

- e) Michael T. Barako, Scott G. Isaacson, Feifei Lian, Eric Pop, Reinhold H. Dauskardt, Kenneth E. Goodson, and Jesse Tice, “Dense Vertically Aligned Copper Nanowire Composites as High Performance Thermal Interface Materials,” *ACS Applied Materials and Interfaces*, 9 (48), pp 42067–42074, 2017. DOI: 10.1021/acsami.7b12313.
- f) Markus D. Ong, Vincent Jousseau, Sylvain Maitrejean, Reinhold H. Dauskardt: “Fracture Properties of Porous MSSQ Films: Impact of Porogen Loading and Burnout, in *Materials, Technology and Reliability of Low-k Dielectrics and Copper Interconnects*,” edited by Ting Y. Tsui, Young-Chang Joo, Lynne Michaelson, Michael Lane, Alex A. Volinsky (Mater. Res. Soc. Symp. Proc. 914, Warrendale, PA, 2006), 0914-F04-07.
- g) Ryan Birringer, Roey Shaviv, Tom Mountsier, Jon Reid, Jian Zhou, Roy H. Geiss, David Read, and Reinhold Dauskardt, “Adhesion, Cu Voiding, and Debonding Kinetics of Copper / Dielectric Diffusion Barrier Films,” *Advanced Metallization Conference*, Baltimore, 2009.
- h) M. Lane, W. Ni, R. H. Dauskardt, Q. Ma, H. Fujimoto and N. Krishna, “Effects of Interface Nonplanarity on the Interface Fracture Energy on the TiN/SiO₂ System,” in *Thin Film Stresses and Mechanical Properties VII*, vol. 516, Editors: T. Marieb, J. Bravman, M.A. Korhonen, J.R. Lloyd, *Proceedings of MRS Annual Meeting*, Boston, MA, pp. 357 – 362, 1998.

- i) Taek-Soo Kim, Qiping Zhong, Maria Peterson, Halbert Tam, Tomohisa Konno, and Reinhold H. Dauskardt, “Stress and Slurry Chemistry Effects on CMP Damage of Ultra-Low-k Dielectrics,” IEEE International Interconnect Technology Conference Proceedings, June 2007.
- j) Reinhold H. Dauskardt, Taek-Soo Kim, Qiping Zhong, Maria Peterson, Halbert Tam, and Tomohisa Konno, “Stress and Slurry Chemistry Effects on Cracking and Damage Evolution during CMP: Implications for Next Technology Nodes,” Twelfth International Conference on Chemical-Mechanical Polish (CMP) Planarization for ULSI Multilevel Interconnection (CMP-MIC), Fremont, California, 2006.
- k) M. Lane, A. Vainchtein, H. Gao, and R. H. Dauskardt, “Plasticity Contributions to Interface Adhesion in Thin-Film Interconnect structures,” Journal of Materials Research, 15 [12], 2758-2769, 2000.
- l) Ryan Birringer, Roey Shaviv, Paul Besser and Reinhold Dauskardt, “Environmentally Assisted Debonding of Copper / Barrier Interfaces,” Acta Materialia, 60, 2219–2228, 2012.

C. Compensation

19. I am being compensated for services provided in this matter at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of my work in this matter. My compensation is not contingent upon the

results of my study or analysis, the substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '623 patent.

III. MATERIALS REVIEWED

20. In forming my opinions regarding the '623 patent, I reviewed the materials discussed in this declaration, including the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

IV. LEGAL STANDARDS

21. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '623 patent are patentable, I understand that I am obliged to follow existing law.

A. Anticipation

22. I understand the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I understand that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

23. I understand that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

24. I understand that under 35 U.S.C. §103(a), “[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in §102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I understand that, in inter partes review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

25. When considering the issues of obviousness, I understand that I am to do the following:

- a. Determine the scope and content of the prior art;
- b. Ascertain the differences between the prior art and the claims at issue;
- c. Resolve the level of ordinary skill in the pertinent art; and
- d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

26. I understand that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have been asked to assume is just before the earliest claimed priority date of the '623 patent (i.e., December 3, 2003).

27. I understand that obviousness is a determination of law based on underlying determinations of fact. I understand that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of obviousness or non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the '623 patent).

28. I understand that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also understand that a person of ordinary skill in the art is presumed to know all relevant prior art. I understand that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

29. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I understand

that the following principles may be considered, and I have been asked to consider them:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

30. I understand that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I understand that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I understand that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

31. I understand the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I understand that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I understand it would be improper to consider only the specific problem the patentee was trying to solve.

32. I understand that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I understand that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I understand that in many fields, there

may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I understand that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

33. I understand that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine them. But I also understand that any “teaching, suggestion, or motivation” present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I understand this “teaching, suggestion, or motivation” test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

34. I understand that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

35. I understand that when there is a known technique to address a known problem using prior art elements according to their established functions, then a person of ordinary skill in the art would have had a motivation to combine.

36. I understand that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I understand that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. LEVEL OF ORDINARY SKILL IN THE ART

37. A person of ordinary skill in the art (hereinafter “POSITA”) had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

38. I understand that I am to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

39. I have not analyzed the priority date of the ’623 patent, but I note that the earliest claim of priority listed on the face of the ’623 patent is December 3, 2003. I have also treated this date as the date from which to assess the knowledge available to a person of ordinary skill in the art.

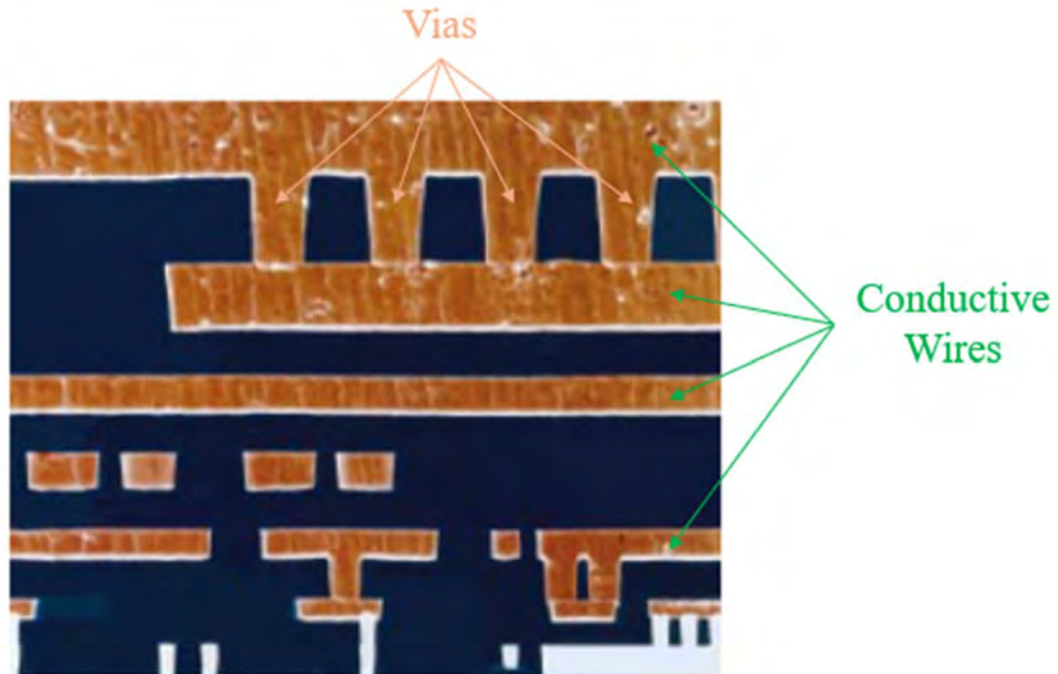
VI. TECHNOLOGY BACKGROUND

40. In my opinion, all the elements of the claims in the '623 patent were well known before December 3, 2003.

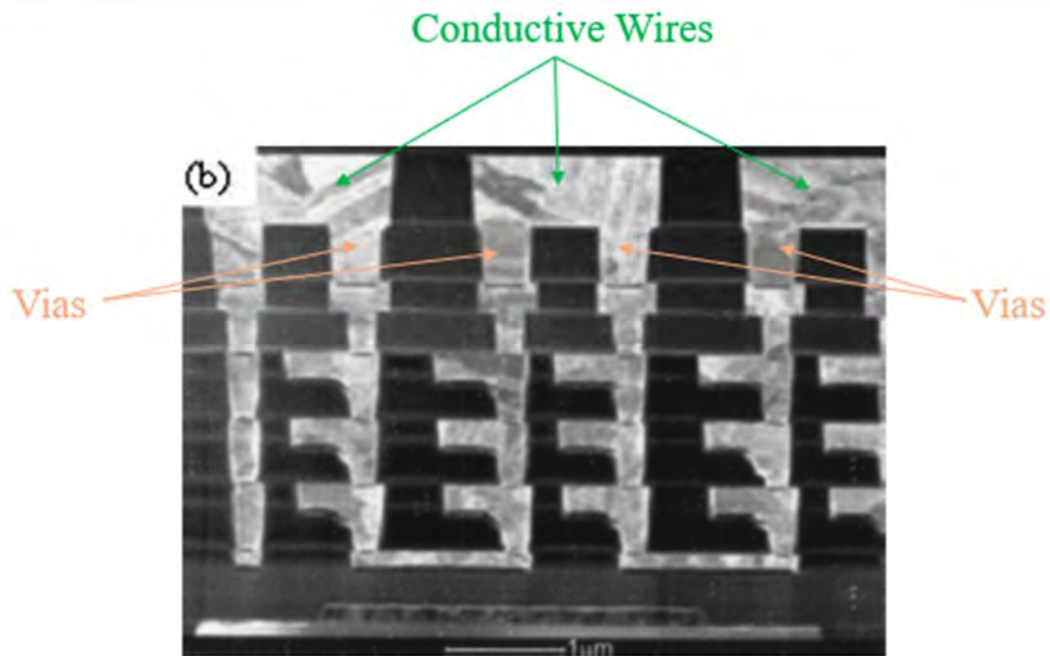
41. A person of ordinary skill in the art in the timeframe relevant to the '623 patent would have been familiar with the background information described below.

A. Interconnects and Dual Damascene

42. Semiconductor chips have multiple levels of conductive wires (“interconnects”) for controlling chip operation, with vias connecting wires between different levels when needed. TSMC-1015, 1:13-24; *see also* TSMC-1012, 32. Aluminum and copper are known interconnect materials, with copper commonly used in VLSI interconnect metallizations. TSMC-1015, 1:13-24; TSMC-1012, 32; TSMC-1017, 2:53-58. Exemplary multi-level copper wiring structures are shown below:



TSMC-1012, 32



TSMC-1028, 5452

43. Introduced by the early 1990s, dual damascene is a manufacturing process where patterns of trenches and underlying via holes are filled with conductive metal(s) to simultaneously form the interconnects on a given level and the vias below that level. TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract; TSMC-1034, 671-76. Dual damascene is illustrated below:

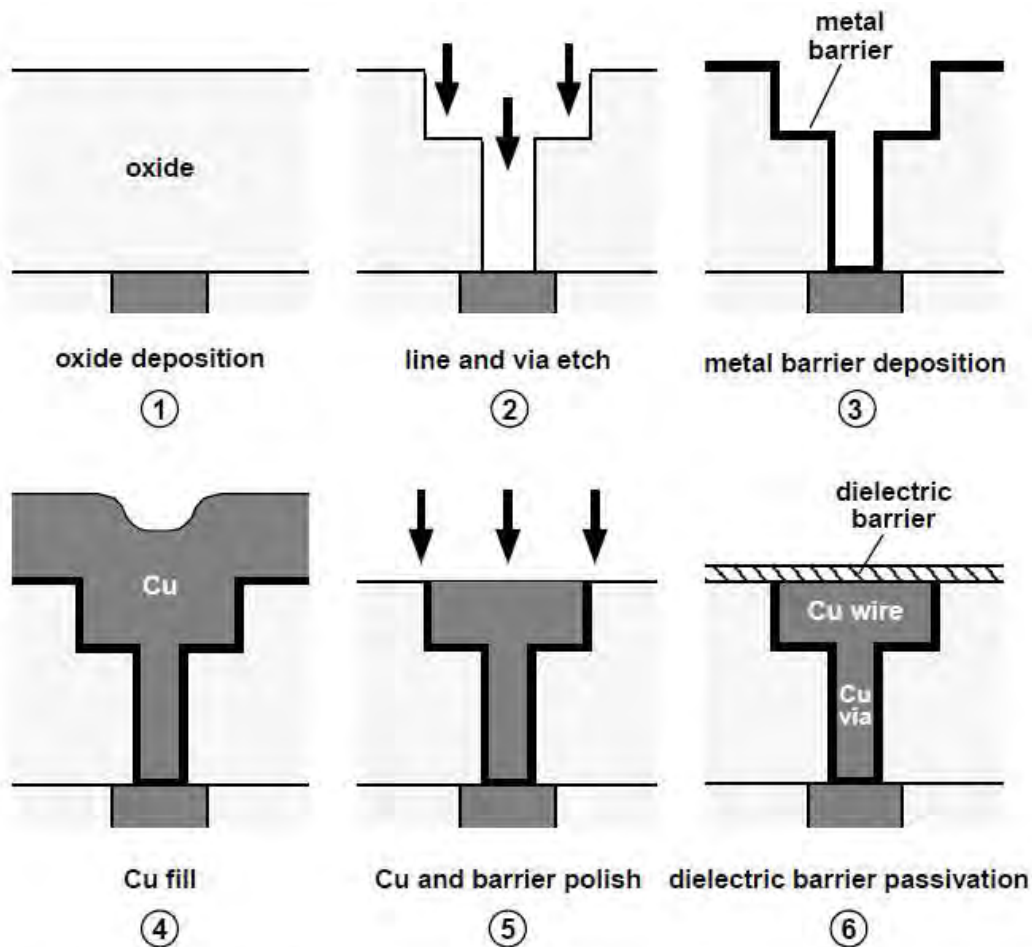


Figure 2-5 Simplified dual-Damascene process flow for fabricating Cu interconnects.

TSMC-1027, 25. In the above process flow, step 4→5 is typically accomplished using Chemical Mechanical Polishing (“CMP”). TSMC-1034, 322-34, 675.

B. Dummy Structures for Reducing Stress-Induced Voiding, and Improving Strength

44. Stress migration and electromigration involve the movement of metal atoms and vacancies within the interconnect structure; because vacancies tend to aggregate in/under vias, voids can form and cause electrical disconnects. TSMC-1029, 207; TSMC-1028, 5455-56, 5458-59; TSMC-1015, 1:32-37, 2:61-63. In addition, insulating films, especially low k materials, can have lower mechanical strength and poorer adhesion that makes them susceptible to damage, for example during CMP. TSMC-1016, 1:53-2:7; TSMC-1026, 583.

45. As replete in the art, dummy structures have been used well before the '623 patent for addressing these problems. For example, dummy vias have been added near active vias to arrest stress-induced vacancy migration and void formation. TSMC-1029, Abstract, 208; TSMC-1015, 2:64-3:14. Dummy structures have been known to address electromigration reliability concerns, including dummy plugs that act as reservoirs for metallic ions and reduce mechanical stress caused by electromigration. *See* TSMC-1015, 1:66-2:11; TSMC-1032, ¶¶[0012]-[0016]. Migrating vacancies/microvoids get distributed between vias and dummy vias, reducing their concentration in/under the vias. TSMC-1029, 208; TSMC-1009,

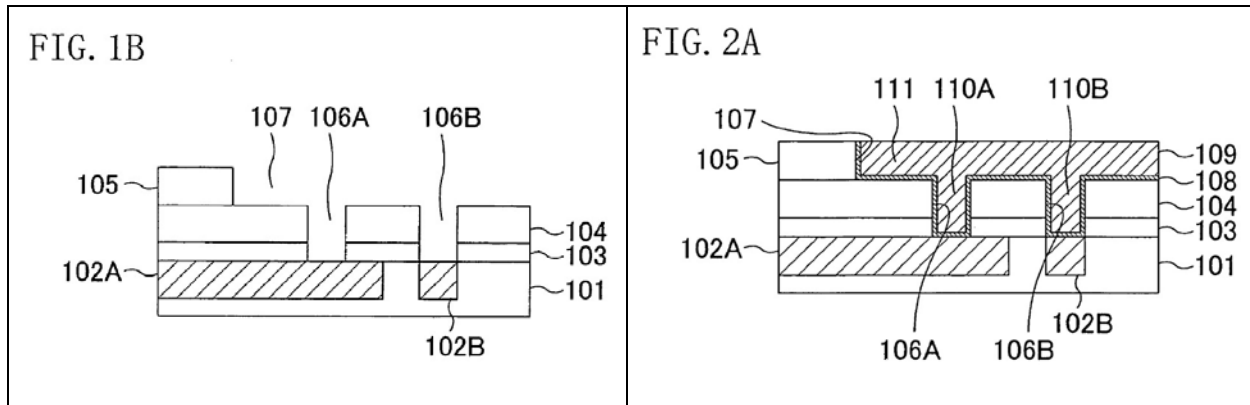
¶[0088]. Dummy vias were also well-known to improve mechanical strength, such as to prevent damage during CMP. TSMC-1016, 4:42-47; TSMC-1026, 584-85.

46. Similar to dummy vias, dummy wirings also improve mechanical properties, helping adhesion across multiple insulating layers and leading to improved planarization after CMP by reducing dishing. TSMC-1020, Abstract; TSMC-1024, 2:55-58; TSMC-1025, Abstract; TSMC-1026, 584-85. Connecting dummy wirings to dummy vias was well known to increase the mechanical strength of the combined insulating layer and upper-level wiring, as well as enhancing the durability of multi-layered insulating films during CMP and other manufacturing steps. TSMC-1011, 8:35-54.

VII. THE '623 PATENT

A. Overview

47. The '623 patent relates to a semiconductor device having multilevel interconnection structures. TSMC-1001, 7:47-50. A first interconnect 102A is formed in an insulating film 101, along with an optional dummy interconnect 102B. *Id.*, 10:56-63, Figs. 1A, 2B. After applying insulating layers 103, 104, and 105 on top of 102A and 102B, the dual damascene process is used to form second interconnect 111 on/in the insulation layer stack, which is connected to first interconnect 102A by via 110A:



Id., 11:5-21; 6:38-40, Figs. 1B-1C, 2A-2B. A dummy via 110B, formed in dummy hole 106B simultaneously with via 110A and interconnect 111, connects dummy interconnect 102B with second interconnect 111. *Id.*, 11:15-21; Figs. 2A-2B.

48. The first interconnect 102A, via 110A and second interconnect 111 constitute part of a closed-circuit during device operation, while neither the dummy interconnect 102B nor dummy via 110B does. *Id.*, 10:24-28. That is, the device remains operable even if the dummy interconnect 102B and dummy via 110B are omitted from the structure. *Id.*, 10:28-32.

49. According to the '623 patent, vacancies in the copper film 109 of second interconnect 111 are divided and respectively flow into the via 110A and dummy via 110B, thereby reducing vacancies flowing into the via 110A and reducing the associated stress gradient. *Id.*, 11:36-42. The '623 patent says this suppresses occurrences of voids in the via hole 106A. *Id.*, 11:38-45.

B. Prosecution History

50. The '623 application was filed in the USPTO on December 2, 2004, claiming priority to a Japanese application filed December 3, 2003.

51. After a restriction and election requirement (01/05/2007), Applicant elected the figure 2B species (03/05/2007), canceled claims 1-26, and added and elected new claims 27-86 (of which claim 27 was independent). TSMC-1002, 207-19.

52. In a non-final Office Action (05/22/2007), the Examiner withdrew claims 55-56, and rejected claim 27 as anticipated by He (U.S. Patent No. 6,919,637), identifying He's dielectric pillar 55 as the claimed dummy via. *Id.*, 240. The Examiner further rejected other claims reciting interconnect widths and via diameters and their spacing, stating that "one of ordinary skill in the art would have been led to the recited shapes, sizes and dimensions through routine experimentation and optimization." *Id.*, 244-45.

53. Applicant responded (08/22/2007) by amending claim 27 to recite that the dummy via be made of a conductive film. *Id.*, 266. In a Final Office Action (10/12/2007), the Examiner maintained the rejections, asserting that He's copper via 68 met the recited "dummy" feature. *Id.*, 285-97. Through an RCE (01/11/2008), Applicant amended claim 27 to require that the second interconnect form a dual damascene structure with each of the via and the dummy via. *Id.*, 301.

54. After another non-final Office Action (02/11/2008) maintained the rejections over He (*id.*, 320-29), Applicant's response (06/11/2008) amended claim 27 by removing the dual damascene limitations, and adding that the dummy via be "arranged so as to be incapable of having current flow therethrough." *Id.*, 331. Applicant argued that He's via 68 is arranged to allow current to flow therethrough as part of a closed circuit. *Id.*, 340-41.

55. A Notice of Allowance (08/01/2008) followed, including an Examiner's Amendment re-inserting the dual damascene limitations into claim 27. The reasons for allowance states that the prior art "does not disclose or suggest all of the claimed elements in the present application wherein, amongst other limitations, the formed dummy vis made of a conductive film and being arranged as in the context of claim 27." *Id.*, 354-55.

56. The '623 patent issued on October 21, 2008.

C. Claim Construction

57. I have not been made aware of any specific claim construction to apply to the claims. I will apply the plain and ordinary understanding of the claims to a POSITA.

VIII. PRIOR ART

58. I have been informed that the following references are prior art as follows:

Reference	Filed	Published
Watanabe	12/4/2002 (USPTO)	6/26/2003
Hasunuma	9/3/2003 (USPTO)	6/17/2004
Aoyagi	3/20/2001 (USPTO)	9/6/2001
Kunikiyo	7/7/2000 (USPTO)	4/6/2004
Kurashima	8/14/2003 (USPTO)	5/9/2006
Iizuka	1/24/1992 (USPTO)	10/5/1993
Kamoshima	9/9/2003 (USPTO)	9/9/2004

IX. SUMMARY OF PRIOR ART REFERENCES

A. Watanabe – U.S. Patent App. Pub. No. 2003/0116852

59. Watanabe identifies the same problem of stress-related via failures in dual damascene interconnects later addressed by the '623 patent, specifically citing stress migration leading to via lift-off (i.e., void formation) and connection failure. TSMC-1004, ¶¶[0012]-[0019], [0022]-[0024], Fig. 20 (showing voids formed by lifting up of the metal film). To address stress migration, Watanabe also proposed the same solution proposed in the '623 patent: incorporating non-functional dummy vias formed concurrently with the functional structures using the dual damascene process. *Id.*, Abstract, ¶¶[0026]-[0028]. Watanabe further teaches that such dummy

structures provide a source of copper atoms to mitigate electromigration, and enhance support for insulating film 29/second wiring 39. *Id.*, ¶¶[0026], [0070]-[0079].

60. Watanabe discloses several embodiments of semiconductor devices, and discloses a method of manufacturing (Figures 12A-12N) that applies to the device embodiments. Watanabe discloses the following embodiments:

- a “first embodiment” in Figures 1-2 (*see* ¶¶[0059]-[0087]);
- a “second embodiment” in Figures 3-4 (*see* ¶¶[0088]-[0092]);
- a “third embodiment” in Figures 5A-5C (*see* ¶¶[0093]-[0108]);
- a “fourth embodiment” in Figures 6-7 (*see* ¶¶[0109]-[0114]);
- a “fifth embodiment” in Figures 8-11 (*see* ¶¶[0115]-[0133]); and
- a more generic embodiment in Figure 14 (*see* ¶¶[0171]-[0181]).

See, e.g., TSMC-1004, ¶¶[0038]-[0049], [0051].

61. As understood by a POSITA and as stated by Watanabe, like reference numbers in Watanabe’s figures refer to the same structures in the first to fifth embodiments, and each figure does not necessarily show all the components. In describing the second embodiment, Watanabe states that “[i]n FIG. 3, the same reference numerals as those in FIG. 1 are affixed to the members explained in FIG. 1 and their explanation will be omitted hereunder.” *Id.*, ¶[0089]. In describing the third embodiment (Figs. 5A-5C), Watanabe notes that “[i]n these figures, in order to

make the planar arrangement of each plugs and the planar shape of the second wiring 39 easy to see, the underlying layer 20 (see FIGS. 1 and 3) and each insulating films are omitted.” *Id.*, ¶[0094]. Regarding the method of manufacturing in Figures 12A-12N, Watanabe states that the method is applicable for manufacturing “the semiconductor device according to the embodiments of the present invention.” *Id.*, ¶[0135]. Regarding the embodiment of the semiconductor device in Figure 14, Watanabe states regarding its members that “[t]he underlying layer 20 in the present embodiment and each embodiments of the present invention is constructed by above members, for example.” *Id.*, ¶[0173]. The POSITA understands, therefore, that the same underlying layer 20 and insulating films as illustrated Figures 1, 3, and 14 exist in the Figure 5A-5C device structure, but are not shown in Figures 5A-5C figures.

62. Watanabe says the same for the fifth embodiment shown in Figs. 8 and 9: “In FIG. 8, reference numerals similar to those in the above are affixed to the members explained already in the above, and thus their explanation will be omitted here under.” *Id.*, ¶[0116].

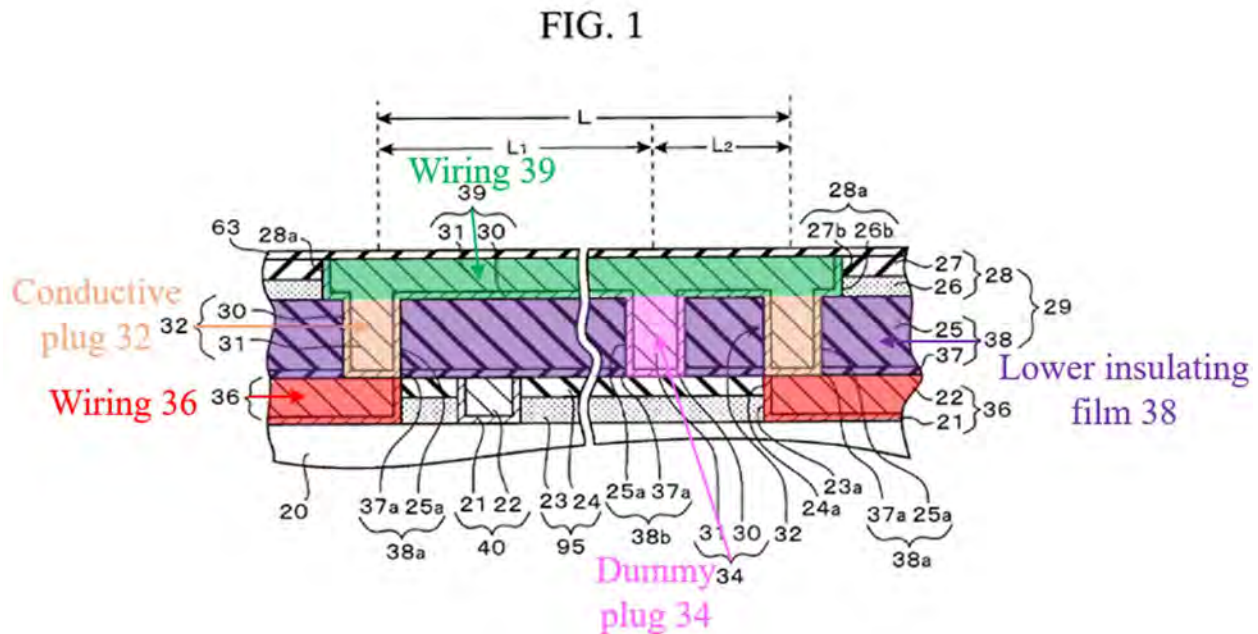
63. Watanabe teaches that the Figure 14 embodiment includes further layers built using the same manufacturing process. In introducing Figure 14, Watanabe explains that: “Although the structure of two wiring layers (the first wiring 36 and the wiring 39) is obtained in the above, any number of wirings can be

laminated by repeating the method same to described above. The case where four layers are laminated will be explained in the following.” *Id.*, ¶[0171].

64. Watanabe describes a method of manufacturing in Figures 12A-12N, which applies to the first to fifth embodiments. Watanabe states that “a method of manufacturing the above semiconductor device will be explained with reference to FIGS. 12A to 12N hereunder. FIGS. 12A-12N are sectional views showing the method of manufacturing the semiconductor devices according to the embodiments of the present invention.” *Id.*, ¶[0135]; *see id.*, ¶[0049]. This method of manufacturing is referenced earlier when Watanabe describes the first embodiment: “[a]s will be described later, this semiconductor device is manufactured by the dual damascene process.” *Id.*, ¶[0072]. Further, Figures 12A-12N use the same reference numerals as earlier figures. While the specific device shown in Figures 12A-12N matches the second embodiment, the POSITA would recognize that the same overall process applies to the other embodiments – indeed, Watanabe states that “This manufacturing method is the so-called dual damascene process in which the wirings and the plugs are formed integrally.” *Id.*, ¶[0135]. Watanabe also discloses that the method can be repeated to obtain any number of wirings. *Id.*, ¶[0171].

65. Figures 1-2 show Watanabe’s first embodiment. It discloses a structure directly analogous to that claimed in the ’623 patent. The interconnect structure includes a wiring 36 (an interconnect), an insulating film 29 (which is made of

multiple films), and a wiring 39 (another interconnect) connected to the wiring 36 by a conductive plug 32, which is a functional via. *Id.*, ¶¶[0065]-[0074], Figs. 1, 2. Crucially, it also includes a dummy via (Watanabe’s dummy conductive plug 34), where the wiring 39, plug 32, and dummy plug 34 are simultaneously formed by a dual damascene process. *Id.*, ¶¶[0070], [0072], Fig. 1. See annotated Figure 1 below:

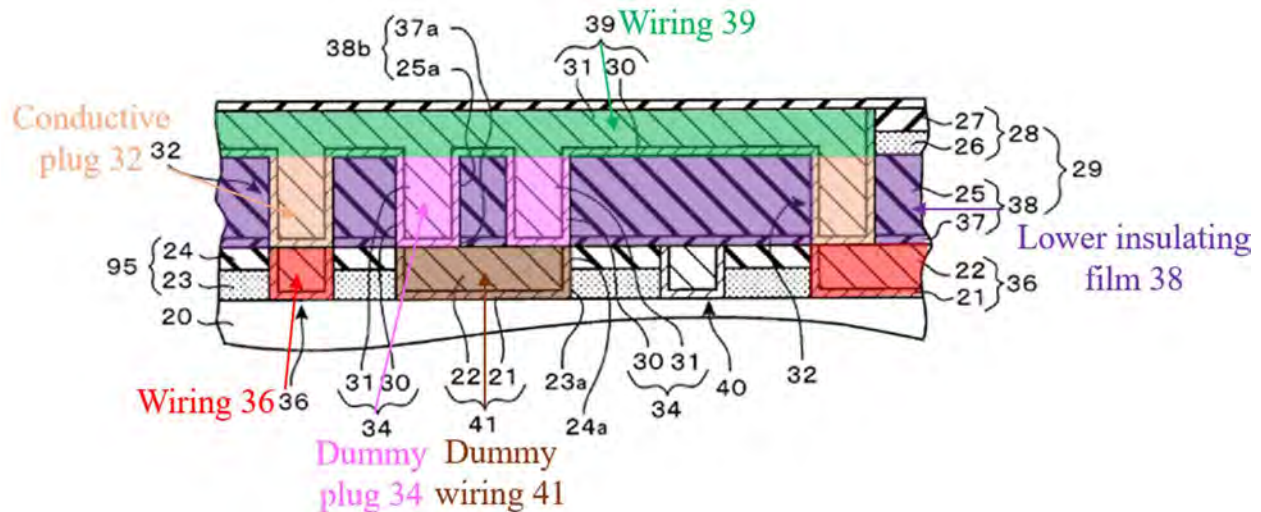


66. Conductive plug 32 connects wiring 36 and wiring 39. Like the '623 patent's dummy via 110A, Watanabe's dummy via 34 connects to the second interconnect (39) above but lands on the lower insulating layer (Watanabe's first insulating film 95) in a "non-forming region" below, rendering it incapable of carrying functional current. *Id.*, Fig. 1, ¶¶[0067], [0079]. Watanabe teaches that the dummy plugs 34 reduce stress migration problems, provide a source of copper atoms

to mitigate electromigration, and enhance support for insulating film 29/wiring 39. *Id.*, ¶¶[0026], [0028], [0070]-[0079], [0091]. Watanabe describes its interconnects using the term “wiring” (e.g., “wiring 36,” “wiring 39,” “wiring 51”). A POSITA understood that such wirings constitute “interconnects” as those terms are understood in the art because a wiring is a structure formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:20-27. Wiring/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:36-38.

67. Figures 3-4 disclose Watanabe’s second embodiment, which adds, among other structure, a dedicated, isolated dummy wiring 41. TSMC-1004, ¶¶[0028], [0090]-[0091], Fig. 3. See annotated Figure 3 below:

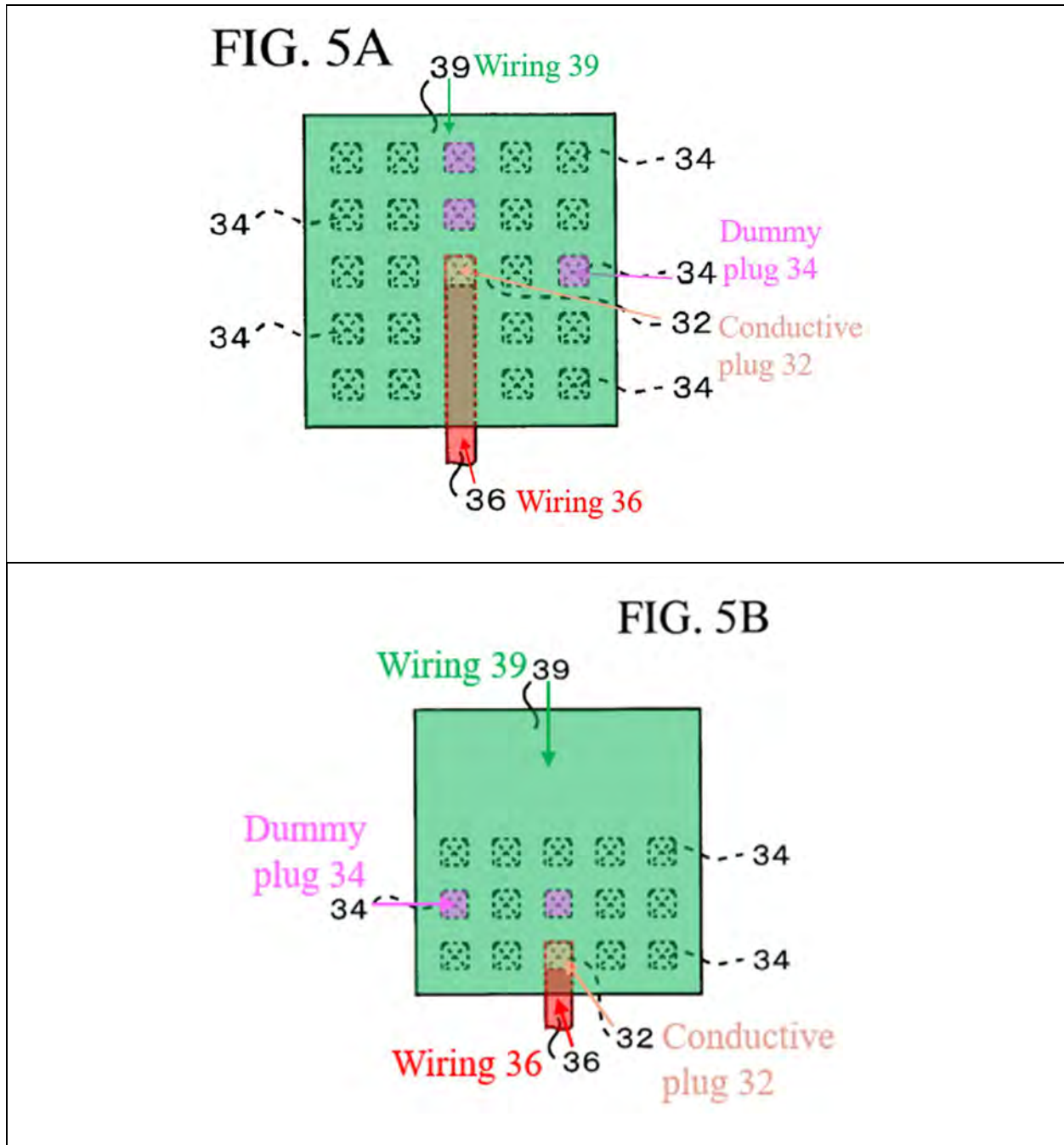
FIG. 3



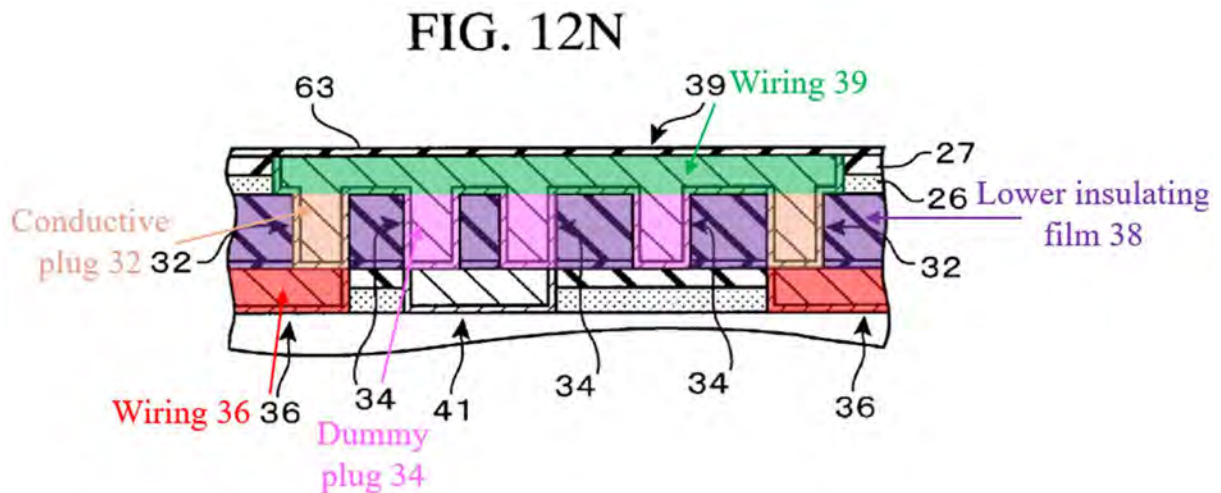
68. The dummy wiring 41 resides in the same insulating film 95 as wiring 36. *Id.*, Fig. 3. Watanabe teaches that this structure adds mechanical strength and uniformity during CMP. *Id.*, ¶¶[0028]-[0029], [0090]-[0091]; Figs. 3-4. Watanabe's dummy wiring 41 is directly analogous to the '623 patent's "first dummy interconnect" and resides in the same lower insulating layer (Watanabe's insulating film 95) as the functional first interconnect (36). *Id.*, Fig. 3. Watanabe teaches that this structure adds mechanical support and uniformity during CMP. *Id.*, ¶¶[0028]-[0029], [0091].

69. Figures 5A-5C disclose Watanabe's third embodiment. Watanabe's third embodiment is the same as Watanabe's first and second embodiments in relevant part, with Watanabe's third embodiment showing that the shape of the wiring 39 can be varied, along with the position of plug 32 and the positions and number of dummy plugs 34. *Id.*, ¶¶[0093]-[0099], Figs. 5A-5C. Watanabe's third

embodiment is the same in relevant respects as the first and second embodiments, with the third embodiment showing an alternative shape for the wiring 39 and different positions of plug 32 and different positions and numbers of dummy plugs 34, as exemplified in Figures 5A and 5B below:



Id., ¶¶[0093]-[0099], Figs. 5A-5C. In Watanabe's Figures 5A-5C, a POSITA would have understood that each of the hatched squares not otherwise labeled as a conductive plug 32 constitutes a dummy plug 34, even though I highlight only a few exemplary dummy plugs 34 in the above annotations. *Id.*, ¶¶[0096]-[0098]. Also, given Watanabe's express statement that Figure 12 represents "sectional views showing the method of manufacturing the semiconductor device according to the embodiments of the present invention," (*id.*, ¶¶[0049], [0135] (emphasis added); *see also id.*, ¶[0094] (noting the omission of various layers in Figure 5 for easier understanding)), a POSITA understood that the cross-section of Figure 12N discloses the basic structure of Watanabe's third embodiment (e.g., Figure 5B):

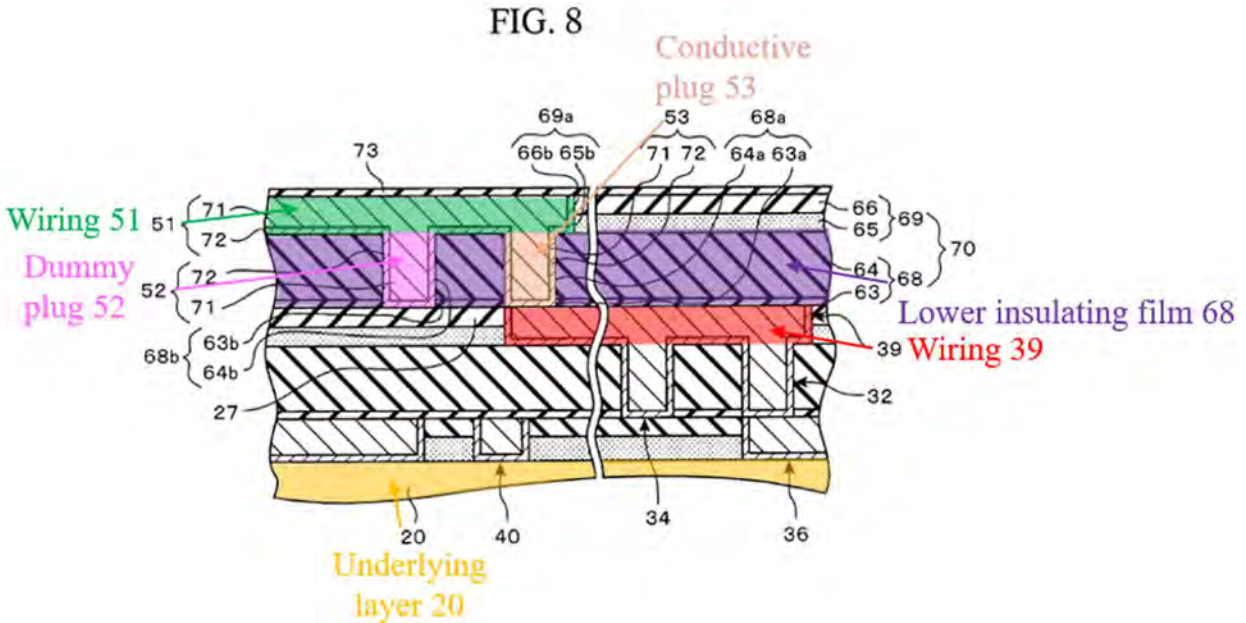


70. Figures 8 and 9 show Watanabe's fifth embodiment. Watanabe's fifth embodiment illustrates a semiconductor device having a three-level interconnect structure, as disclosed in Figure 8 (cross-section) and Figure 9 (plan view). *Id.*,

¶¶[0115]-[0133], Figs. 8-9. In Watanabe's fifth embodiment, the same numbers identifying the same elements as previously described with respect to Figures 1-5 are applicable to Figures 8-9.

71. As with the first-through-third embodiments, Watanabe's fifth embodiment structure is formed on a semiconductor substrate that is part of the underlying layer 20. *Id.*, ¶[0136], Fig. 8; *see also id.* ¶¶[0172]-[0173], Fig. 14 (showing the actual semiconductor devices formed in the semiconductor (silicon) substrate 96).

72. Moreover, Watanabe's fifth embodiment includes an additional interconnect level. *Id.*, Fig. 8. Watanabe's fifth embodiment includes the wiring 39, the lower insulating film 68 and the wiring 51. *Id.* Watanabe's conductive plug 53 is a "via," formed within via hole 68a through the lower insulating film 68 and connects the wiring 51 to the wiring 39. *Id.*, ¶¶[0120], [0122], Figs. 8-9; *see also id.*, ¶¶[0172]-[0178], Fig. 14. Watanabe's dummy plug 52 is connected to the wiring 51. *Id.*, ¶[0122], Figs. 8-9. See annotated Figure 8 below:



73. The dummy plug 52 is conductive, being composed of the same barrier metal layer 72 and copper film 71 as the wiring 51, yet is arranged to be incapable of having current flow therethrough because it terminates between insulating layers 27 and 68 in a non-forming region (i.e., where there is no wiring 39) or toward an isolated dummy wiring 61. *Id.*, ¶¶[0121], [0126]-[0127], [0185]-[0186], Figs. 8-9. The dummy wiring 61 is not shown in Figure 8, but it is shown in Figure 9, and Watanabe explains that the dummy wiring 61 is formed in the same layer as the wiring 39 and that the dummy plug 52 may be connected to this dummy wiring. *Id.* Consistent with Watanabe's overall manufacturing approach using a dual damascene process, the wiring 51 forms a dual damascene structure simultaneously with both the conductive plug 53 and the dummy plug 52. *Id.*, ¶[0135], Fig. 8.

74. Figures 12A-12N disclose Watanabe's method of manufacturing a semiconductor device that is applicable to all the embodiments. *Id.*, ¶¶[0049], [0072], [0134]-[0170], Figs. 12A-12N. The method uses the dual damascene process to form the wiring and the plugs integrally. *Id.* The first-fifth embodiments (Figs. 1-9) use common reference numerals as Figures 12A-12N. *Id.*, ¶¶[0089], [0116], [0135].

75. Figure 14 discloses a four wiring layer embodiment, where the initial structure is like that shown in Figure 1, and then further wiring layers are formed by repeating the method from Figure 12. *See id.*, ¶¶[0171]-[0181]. When introducing Figure 14, Watanabe discloses that the method can be repeated to obtain any number of wirings. *Id.*, ¶¶[0171]-[0173]. Figure 14 further discloses members in the underlying layer 20. *Id.*, ¶[0173], Fig. 14. The underlying layer 20 includes the gate electrode 84 and corresponding source/drain (S/D) regions, the interlayer insulating film 87, and conductive plugs formed from the barrier metal layer 85 and a metal film 86. *Id.* Watanabe explains that those members in the underlying layer 20 in Figure 14 apply to the other embodiments as well. *Id.*

76. Each of the disclosed first to third and fifth embodiments discloses a dual damascene structure of the interconnect with the active via and with the dummy via, respectively. Along with Watanabe's disclosure, this is evidenced by Watanabe's figures themselves. In each of cross-sectional Figures 1, 3, and 8, the

wiring 39,51 is a dual damascene structure with conductive plugs 32,53 and dummy plugs 34,52, respectively. A POSITA would appreciate that Watanabe's barrier metal layer 30,72 conformally coats the outer sides of the plugs 32,53, dummy plugs 34,52, and wiring 39,51, all a single, continuous layer. With this conformal barrier layer coating, copper film 31,71 is added to fill the recesses for the plugs 32,53, dummy plugs 34,52, and trench for wiring 39,51 to form a single, unitary copper structure. A POSITA would have recognized this configuration shown in Figures 1, 3, and 8 as a dual-damascene structure, especially in view of Watanabe's description (*e.g.*, *id.*, ¶¶[0072], [0135], [0161]-[0171], Figs. 12K-12M). A POSITA well understood the dual damascene process and its widespread general use at the time, along with motivations such as increased efficiency and reduced cost benefits. *See* TSMC-1034, 583-84, 671-76, 718, 723-26; TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-147; TSMC-1027, 25; TSMC-1028; 5458.

77. Because Watanabe is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (*e.g.*, interconnect reliability), Watanabe is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1004, ¶¶[0005], [0016]-[0018].

B. Hasunuma – U.S. Patent App. Pub. No. 2004/0113238

78. Hasunuma addresses reliability problems arising from stresses inherent in interconnect structures by incorporating non-functional, concurrently formed reinforcing plugs 28, which are dummy vias. TSMC-1005, ¶¶[0079]-[0086], [0103], [0108]-[0109], [0114], [0121]-[0125], Figs. 8-9, 14. Similar to the '623 patent, Hasunuma's solution for mitigating stress-related problems involves incorporating non-functional, concurrently formed Cu reinforcing plugs 28 ("dummy vias") extending from a given interconnect. *Id.*, Figs. 8, 14.

79. In Figure 8, Hasunuma discloses a semiconductor device having silicon substrate 1, first interconnect comprising a conductive layer 14, a first insulating film including film 3, film 4, and film 2 on the conductive layer 14, and second interconnect conductive layer 26. *Id.*, ¶¶[0090]-[0111], Fig. 8. Hasunuma describes its interconnects using the term "conductive layer" (e.g., "conductive layer 14," "conductive layer 26"). A POSITA understood that such conductive layers constitute "interconnects" as those terms are understood in the art because Hasunuma's conductive layers are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:20-27. Conductive layers/interconnects on different levels can be electrically connected by vias, which

are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:36-38. A conductive plug 27, which is a functional via, connects the two interconnects through the insulating film (TSMC-1005, ¶¶[0101], [0108], Fig. 8), and the reinforcing plugs 28 extend from the conductive layer 26 and are each described by Hasunuma as a “dummy plug (sacrifice plug)” that do not function as wiring (*id.*, ¶¶[0106]-[0109]). *Id.*, Fig. 8. Hasunuma utilizes a dual damascene process for forming the conductive layer 26, plug 27, and reinforcing plugs 28. *Id.*, ¶¶[0101]-[0103], [0106]-[0109]; Figs. 5-8, 14. Hasunuma uses a dual damascene process for each level, as seen in annotated Figure 8 below:

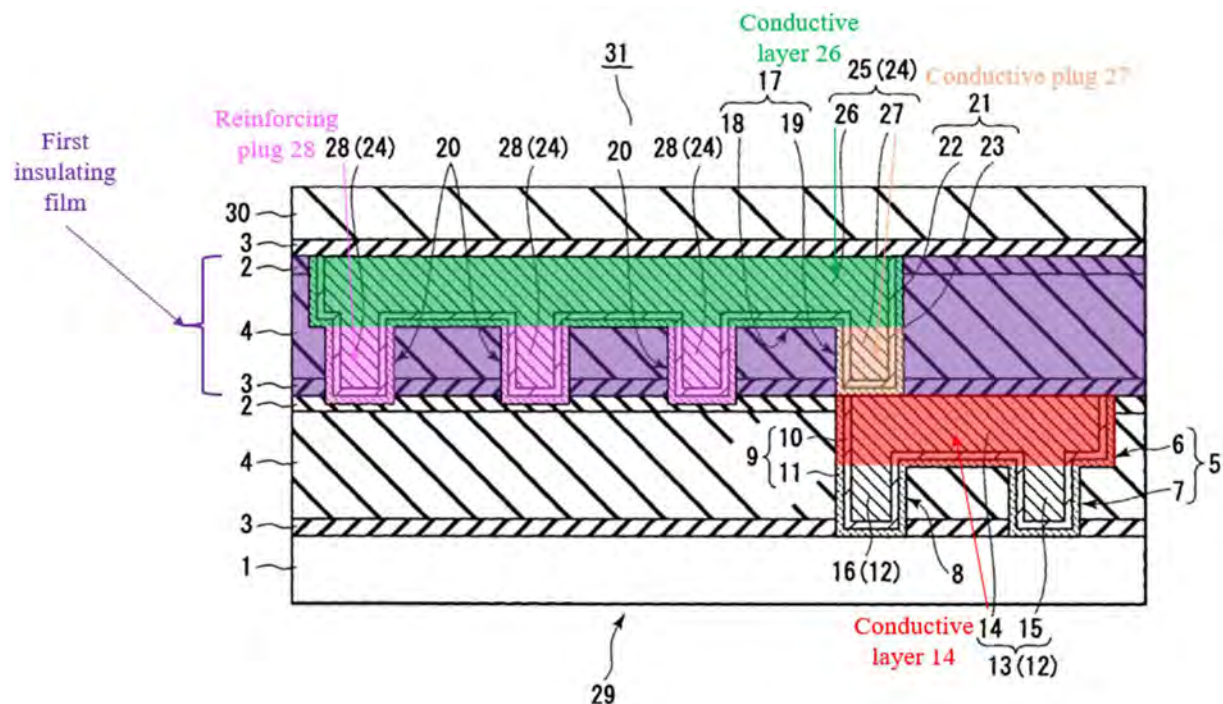


FIG. 8

Id. While not shown, Figure 14 shows similar relevant features as Figure 8.

80. Hasunuma describes forming the recess 18 for the conductive layer 26 and the recess 19 for the conductive via plug 27 together, and explicitly forms the recesses 20 for the reinforcing plugs 28 “integrally with the recess 18” for the conductive layer 26. *Id.*, ¶¶[0101]-[0104], Fig. 4. All these recesses (18, 19, and 20) are then filled simultaneously with the same barrier metal film 21 (including Ta film 22 and TaN film 23) and Cu film 24. *Id.*, ¶¶[0101]-[0103], [0105]-[0108], Figs. 4-6. This directly teaches the dual damascene formation of the conductive layer 26 together with the conductive plug 27 and the reinforcing plugs 28. *Id.*

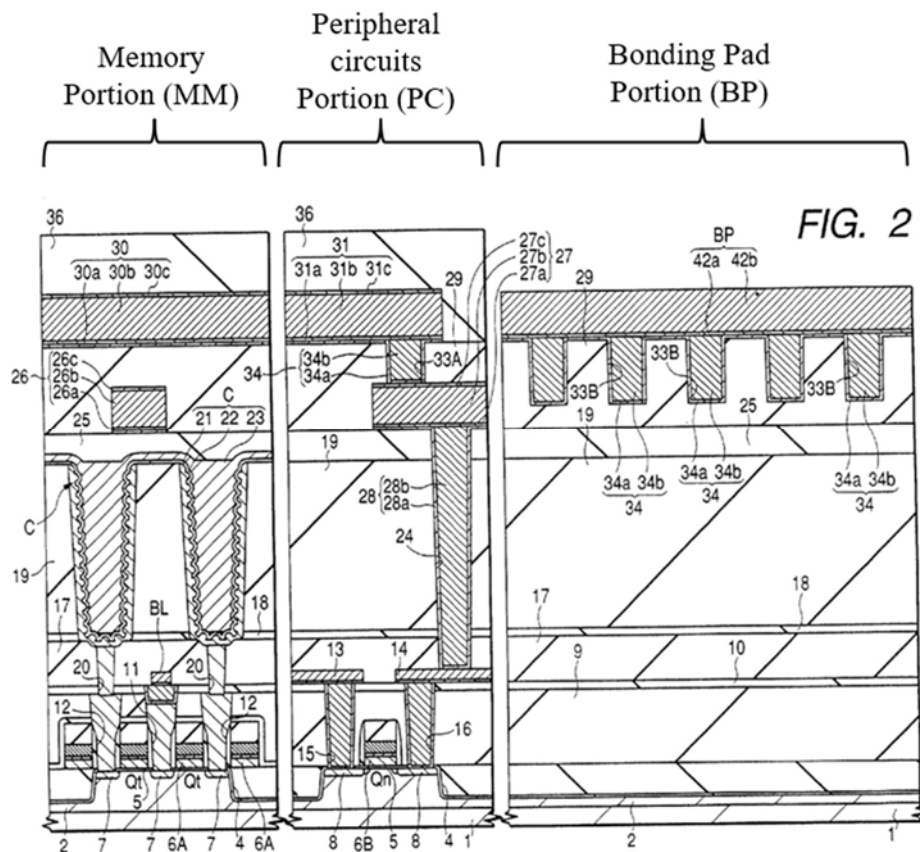
81. Like the purported problem mentioned in the '623 patent, Hasunuma addresses reliability problems arising from stresses inherent in interconnect structures. *Id.*, ¶¶[0079]-[0086]; TSMC-1001, 2:19-38. Hasunuma's solution for mitigating these stress-related issues, just as was later discussed in the '623 patent, involved incorporating the non-functional, concurrently formed reinforcing plugs 28, which are dummy vias, adjacent to the functional conductive via plug 27. TSMC-1005, ¶¶[0114], Fig. 8. This structure was designed by Hasunuma to manage mechanical stresses and to address stress-induced phenomena. *Id.*, ¶¶[0114], [0121]-[0125].

82. Because Hasunuma is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address

(e.g., interconnect reliability), Hasunuma is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1005, ¶¶[0003], [0005], [0079]-[0086].

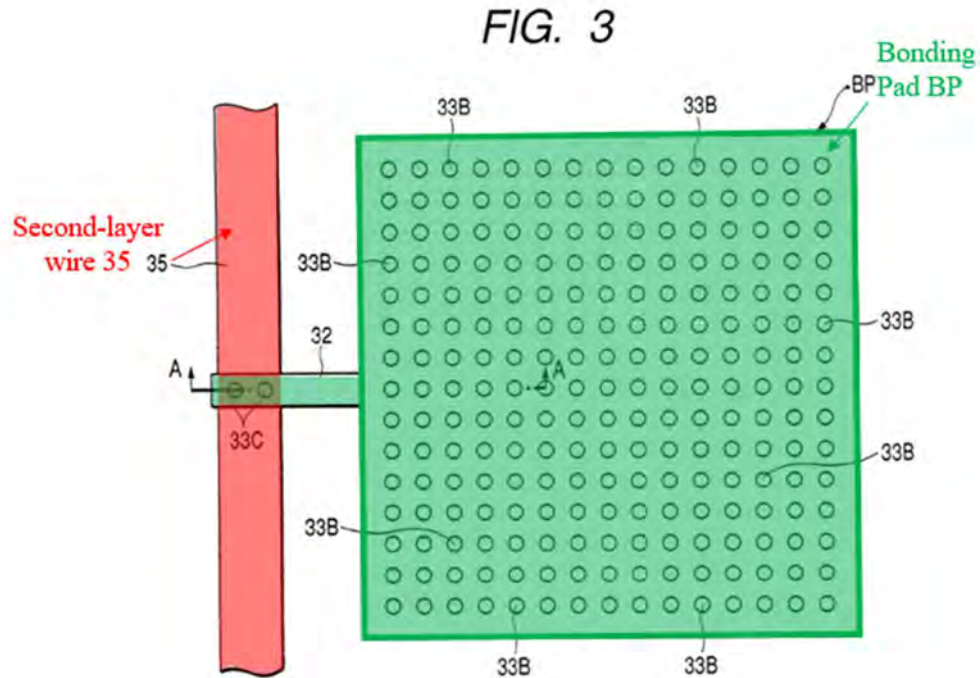
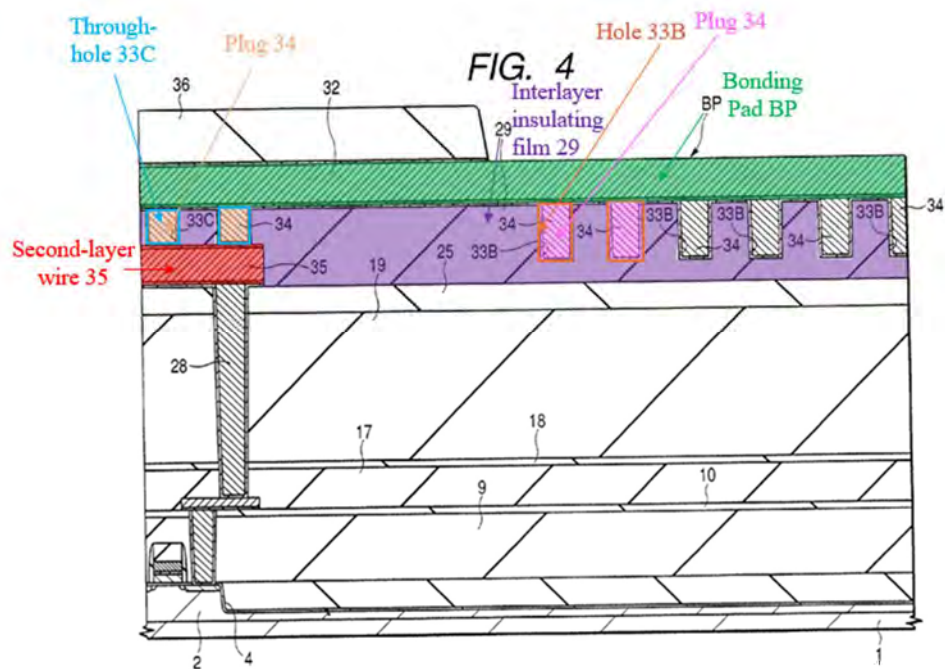
C. Aoyagi – U.S. Patent App. Pub. No. 2001/0019180

83. Aoyagi discloses in Figures 2-12 and 19, and their supporting description, a method of fabricating a semiconductor device and the resulting device. Aoyagi’s annotated Figure 2 discloses a semiconductor device, including “memory portion” (MM) (left), “peripheral circuits portion PC” (center), and bonding pad BP (right):



TSMC-1006, ¶¶[0038]-[0039].

84. Figures 3 and 4 of Aoyagi provide further details for part of peripheral circuit portion and bonding pad portion. *Id.*, Figs. 3-4.



85. These figures show second-layer wire 35, interlayer insulating film 29, and bonding pad BP with lead wire 32 from one end of the bonding pad and connecting to the second-layer wire.¹ *Id.*, ¶¶[0049], [0053]-[0056]. A POSITA would understand the bonding pad and Aoyagi's various "wires" to be "interconnects." Indeed, throughout Aoyagi, its interconnects are described using the term "wire" or "bonding pad" (e.g., "first-layer wire," "second-layer wire," "third-layer wire," "bonding pad BP"). A POSITA understood that such wires and bonding pad BP of Aoyagi constitute "interconnects" as those terms are understood in the art because both Aoyagi's wires and bonding pad BP are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:20-27. Wires/bonding pads/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:36-38. Vias (plugs 34 formed in through-holes 33C) connect

¹ As demonstrated by Figures 3-4, "bonding pad BP" and "lead wire 32" together form a single, integral component, and as such discussion of "bonding pad BP" herein is generally intended to include "lead wire 32" unless specified otherwise. *See* TSMC-1006, Figs. 3-4.

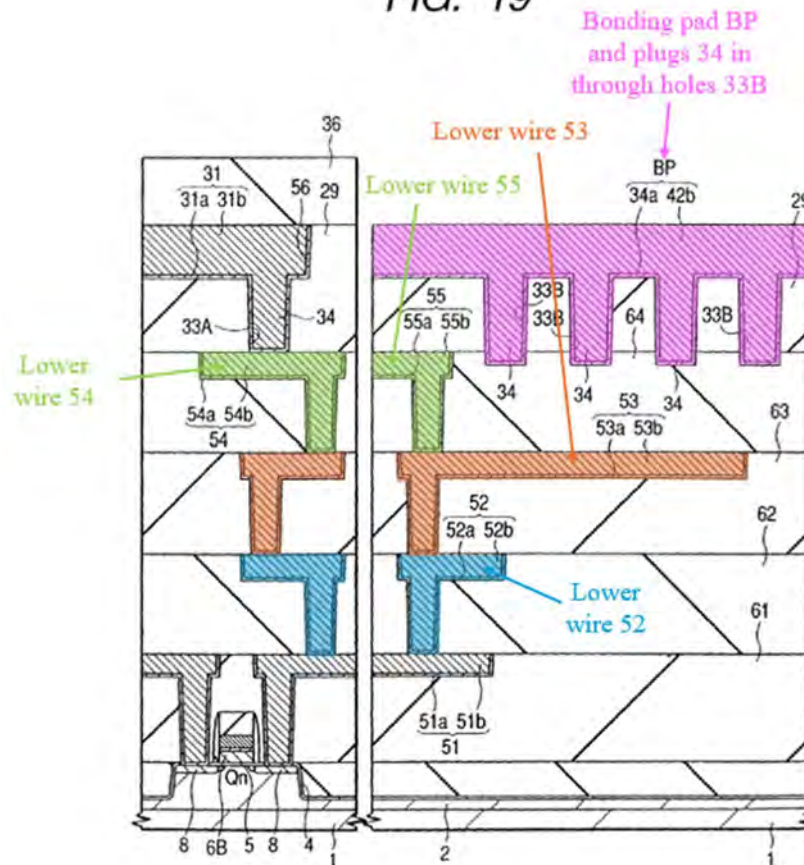
lead wire 32 and second-layer wire 35, and dummy vias (plugs 34 formed in through holes 33B) extend from bonding pad BP into insulating film 29 for promoting adhesion between bonding pad BP and insulating film 29, not for operational current flow to underlying layers for promoting adhesion between bonding pad BP and insulating film 29, not for operational current flow to underlying layers. TSMC-1006, ¶¶[0050]-[0055], [0079].

86. By their labeling and the disclosures in the figures, the “second-layer” wires 26, 27, and 35 are formed at the same level, in the same insulating film 29 in Figures 2-4. Further, third-layer wires 30, 31 are formed over the insulating film 29. *Id.*, ¶[0050]. The bonding pad is formed “by use of the wire formed in the same step as the third-layer wires 30, 31.” *Id.*, ¶[0051].

87. Figures 5-12 disclose a manufacturing process, and Figure 19 discloses an alternative dual damascene process for wiring formation that is applicable to the device shown in Figures 2-4. *Id.*, ¶¶[0050]-[0055], [0077], [0079]. In the case of dual damascene, as shown in Figure 19 and discussed below, second-layer wires are formed into the insulating film that is underneath the insulating film 29, and the third-layer wires such as third-layer wire 31, which includes the bonding pad BP, are formed in the insulating film 29. *Id.*, ¶[0077]. This dual damascene process applies equally to forming the interconnects (e.g., second-layer wire 35 and third-layer wire 31 that includes bonding pad BP) and the functional and dummy vias

(e.g., plugs 34 in holes 33C, 33B) of Figures 3-4. Annotated Figure 19 below shows dual-damascene-formed structures using common cross-hatching for the simultaneously-formed interconnects and the vias/dummy vias directly underneath:

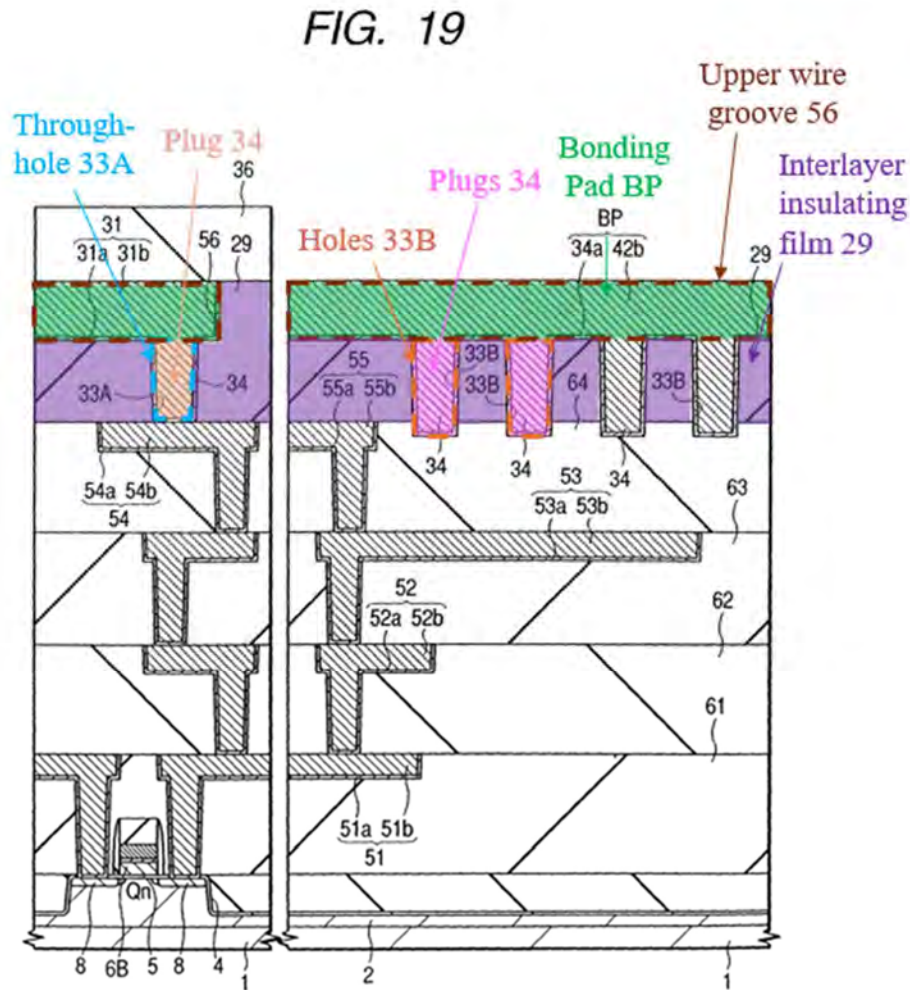
FIG. 19



The respective, common cross-hatching in each layer indicates that each wiring layer and the vias extending downward therefrom form dual damascene structures. This dual-damascene teaching likewise applies to the interconnects (e.g., wire 35, bonding pad BP) and various functional and dummy vias (e.g., plugs 34 in holes 33C, 33B) in Figures 3-4. Specifically, Aoyagi's dual-damascene process may be used to create the interconnects, functional vias, and dummy vias in Figures 3-4. For

example, Aoyagi notes that “upper wire 31 (including the bonding pad BP)” may be formed by depositing conductive material into holes 33A, 33B and wire groove 56. *Id.*, ¶[0077], Fig. 19.

88. Another annotated version of Figure 19 is shown below, disclosing a variety of components of the semiconductor device including components common to the device of Figures 3-4, demonstrating the applicability of the dual damascene process to the device of Figures 3-4:



89. Additionally, given Aoyagi's discussion of using a dual damascene process to form wire 31/bonding pad BP and to deposit conductive material in holes 33A and 33B and upper wire groove 56, a POSITA would have found it obvious to use the dual damascene process to form bonding pad BP/lead wire 32 and the vias formed in through-holes 33C in the structure of Figures 3-4. A POSITA would have been motivated to use the dual damascene process in order to increase efficiency and reduce costs of manufacturing as was well-known at the time. The nature of and advantages associated with dual damascene were well understood in the art. See, e.g., TSMC-1019, 146-147 (stating that dual damascene enhances density and performance and promotes reliability and improves manufacturability, including manufacturing yield); TSMC-1027, 25 (noting dual damascene forms Cu wires and vias with one metal fill and one CMP step, providing process simplification allowing for reduced cost and improved manufacturability); TSMC-1028, 5458-59 (discussing that, with making one level of lines and one level of vias together, can build more levels of Cu interconnects with same number of processing steps); *see also* TSMC-1034, 583-84, 671-76, 718, 723-26. Additionally, a POSITA could have easily implemented such a process given its already disclosed use in Aoyagi and its widespread use in industry at the time. *See* TSMC-1034, 583-84, 671-76, 723-26; TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-151.

90. Because Aoyagi is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Aoyagi is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1006, Abstract, ¶¶[0001], [0004]-[0005].

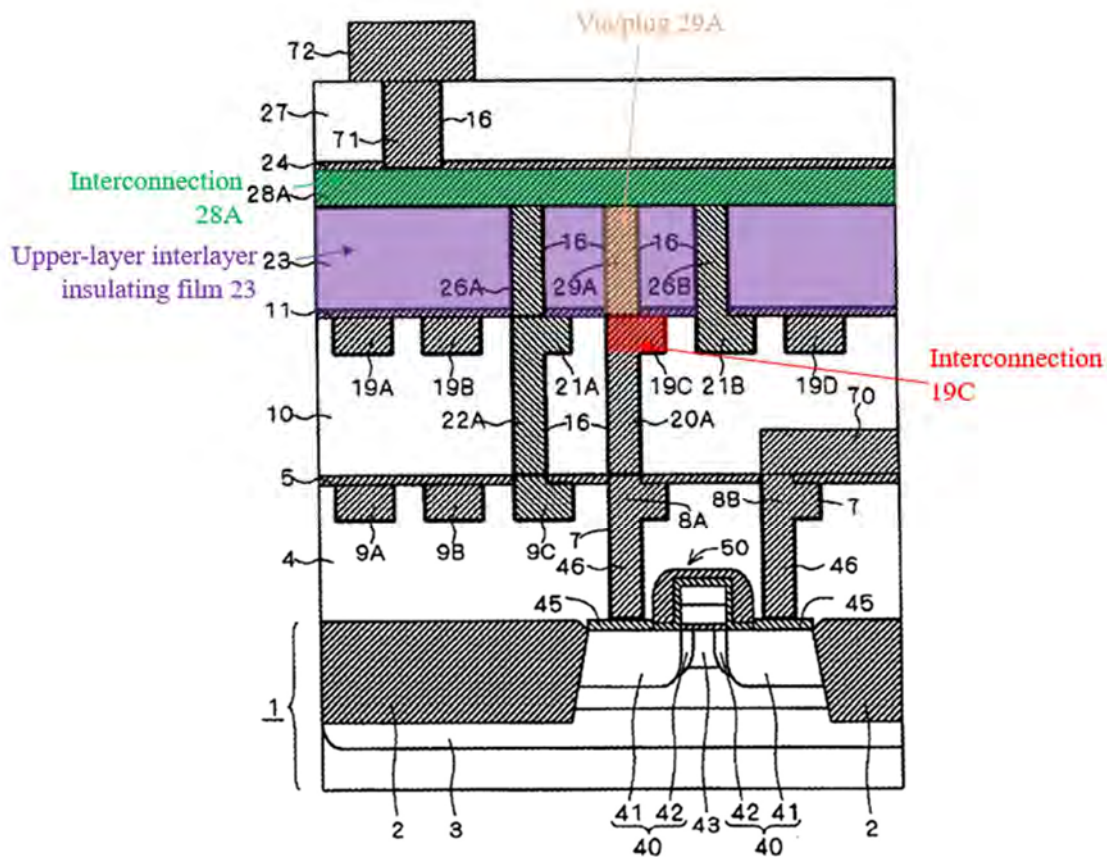
D. Kunikiyo – U.S. Patent No. 6,717,267

91. Kunikiyo discloses in Figure 12 a semiconductor device featuring a multilayered interconnect structure. TSMC-1007, 20:4-49, Fig. 12. Kunikiyo explains that the Figure 12 embodiment adds connections beyond sharing some elements with the Figure 7 embodiment, which are made from the process steps of Figures 3-6. *Id.*, 9:39-43, 20:4-49. Along with active interconnections and vias essential for the device's circuit operation, Kunikiyo adds dummy vias attached to the active interconnections, including dummy interconnections attached to the dummy vias. *Id.* Kunikiyo's dummy structures (i.e., its dummy vias and dummy interconnects) are not related to circuit operation, rather they are added to, *inter alia*, enhance the uniformity of interconnection density and manufacturability, such as improving surface flatness for processing steps like CMP, and suppress noise. *Id.*, 5:46-56, 12:31-36, 14:31-36, 15:62-67, 25:54-26:9.

92. Figure 12 of Kunikiyo illustrates the structural elements of that embodiment. The semiconductor device is built upon a semiconductor substrate 1. *Id.*, 10:52-55, 20:4-24, Fig. 12. Formed above this substrate is interlayer insulating

film 10. *Id.*, 10:50-55, 11:36-37, Fig. 12. On this interlayer insulating film 10, active interconnection 19C and dummy interconnection 21A are present. *Id.*, 11:38-12:30, 20:15-37, Fig. 12. Overlying interlayer insulating film 10 and these interconnections is the upper-layer interlayer insulating film 23. *Id.*, 12:47-51, 20:9-11, Fig. 12. Another, second interconnection layer is formed on this film 23, featuring active interconnection 28A. *Id.*, 12:47-51, 20:9-34, Fig. 12. Interconnection 28A is connected to interconnection 19C through plug (via) 29A, which passes through upper-layer interlayer insulating film 23. *Id.* Interconnection 28A also connects to dummy plug 26A, and this dummy plug 26A, in turn, connects down to dummy interconnection 21A. *Id.*, 11:38-12:30, 20:25-37. Interconnection 28A is formed together with plug 29A and dummy plug 26A in a dual damascene process. *Id.*, 11:48-12:51, 20:9-24, Figs. 3-7, 12. Annotated Figure 12 is below:

FIG. 12



93. Because Kunikiyo is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Kunikiyo is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1007, Abstract, 1:9-15, 6:34-7:7, 12:31-41, 20:4-14.

E. Kurashima – U.S. Patent No. 7,042,099

94. Kurashima enhances durability of insulating films, particularly low-relative-dielectric-constant films, against Chemical Mechanical Polishing (CMP) stresses to prevent film peeling in multi-layered wiring structures. TSMC-1011,

1:15-22, 1:49-67. In its first embodiment (Figs. 1A-1D, 2A-2C, 3A-3B), Kurashima teaches forming a Cu-wire 9 and a Cu-dummy wire 10 simultaneously in spaced-apart areas in a first layer interlayer insulating film 4. *Id.*, 4:50-6:32, Figs. 1B-1D, 3A-3B. Then a second-layer Cu-wire 16 is formed connecting to the first-layer Cu-wire 9. *Id.*, 6:58-8:35, Figs. 2A-3A. Concurrently, a second-layer Cu-dummy wire 17 is formed in contact with first-layer Cu-dummy wire 10, providing a reinforcing effect and enhancing interfacial adhesion and CMP durability, thereby reducing peeling of layers during CMP. *Id.*, 6:11-32; 6:58-8:54, 9:16-23, Figs. 2C, 3A. Kurashima teaches forming functional wires and dummy wires with substantially the same width within the same layer. *Id.*, 4:50-63, Figs. 1D, 3A, 3B. Annotated Figure 3A discloses these features, where each feature is colored to include barrier metal film 7:

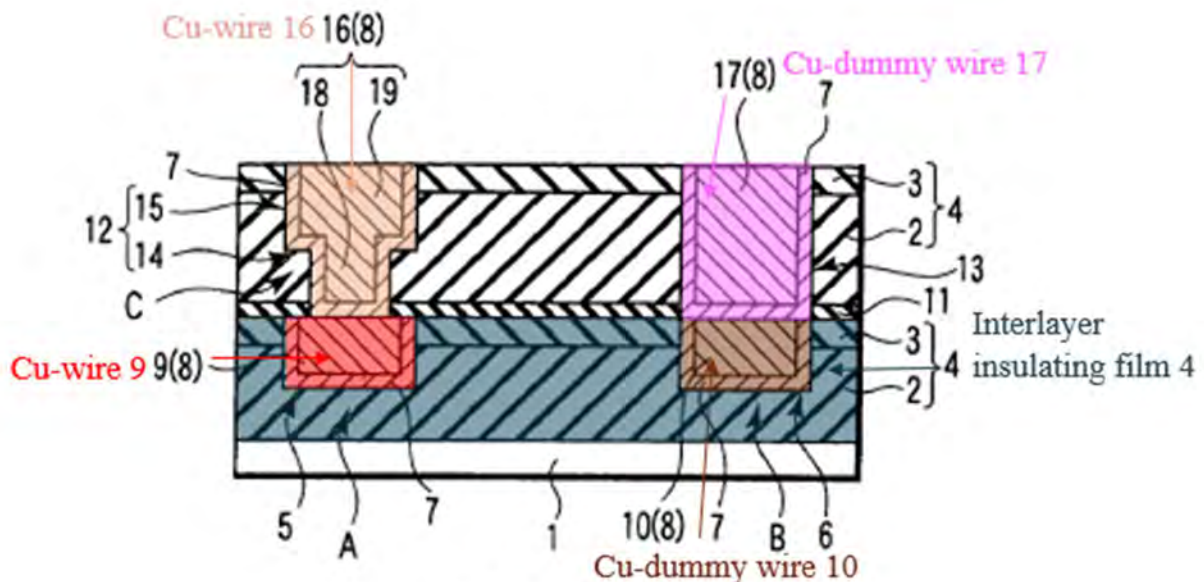


FIG. 3A

95. Because Kurashima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Kurashima is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1011, 1:15-22, 1:49-67.

F. Iizuka – U.S. Patent No. 5,250,465

96. Like the '623 patent, Iizuka describes methods for manufacturing semiconductor devices, specifically focused on improving the filling of small diameter via-holes (e.g., not greater than 0.6 μm) to form reliable conductive plugs between interconnect layers. TSMC-1008, Abstract, 1:7-14, 2:39-45. Iizuka explicitly acknowledges that via-holes can have various planar configurations, stating “It will also be understood that the opening of the via-hole may have any configuration, such as a square, rectangle or circle.” *Id.*, 9:45-47; *see also id.*, 10:17-22. A POSITA would have understood this teaching in Iizuka to refer to the shape of the via-hole viewed in plan view (i.e., from above) or as a cross-section, which then dictates the shape of the resulting via when the via-hole is filled (typically with a conductive metal such as aluminum or copper).

97. Thus, Iizuka teaches that via-holes themselves can be manufactured having various planar configurations, such as a square, rectangle or circle. *Id.* Iizuka’s Example 1 describes forming a “via-hole 6 having a diameter of 0.5 micrometers” (*id.*, 6:60-63), which a POSITA would have understood as disclosing

and resulting in a via with a circular shape (*see also id.*, Fig. 5A (showing a circular via)). Iizuka demonstrates that circular, square, and rectangular vias were known and interchangeable design alternatives, thereby teaching obvious via-shape alternatives for similar prior art structures. *Id.*, 9:41-47.

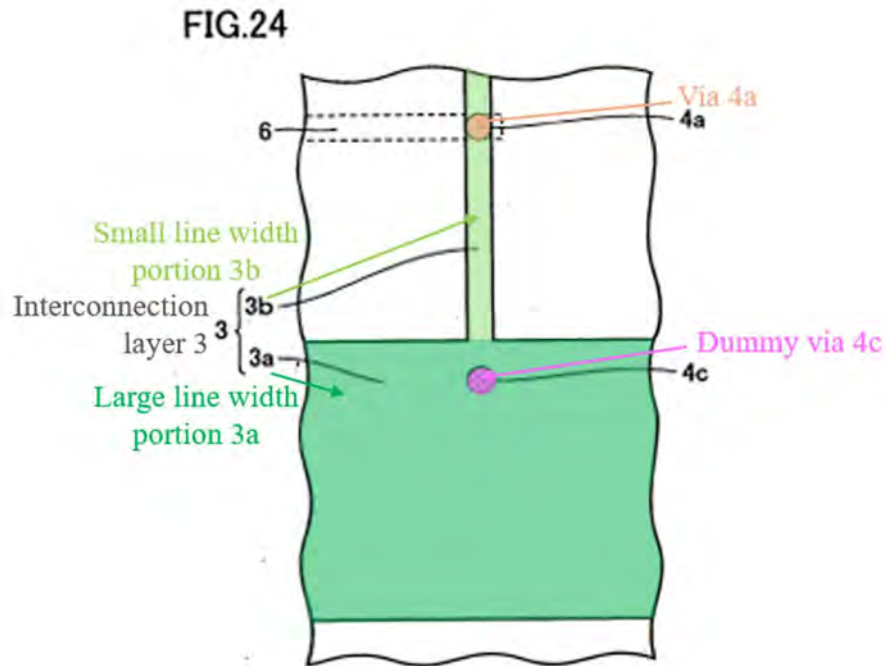
98. Because Iizuka is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Iizuka is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1008, 1:7-14; 2:39-45.

G. Kamoshima – U.S. Patent App. Pub. No. 2004/0173905

99. Kamoshima discloses interconnection structures for semiconductor devices that “suppress concentration of voids in an interconnection under a via due to stress migration.” TSMC-1009, ¶¶[0002], [0008]. Kamoshima teaches interconnect structures having multiple copper interconnect levels separated by an insulator, vias connecting the interconnect layers, and one or more dummy vias. *Id.*, ¶¶[0043]-[0044], [0088]-[0090]; Figs. 16, 22. The dummy vias cause microvoids in interconnection layer 3 to distribute between a via and dummy via, suppressing the concentration of microvoids in the area under the via due to stress migration. *Id.*, ¶¶[0088], [0097]-[0098].

100. The interconnection layer 3 can have different shapes, with Figure 15 disclosing a constant width interconnection layer 3, and Figures 23-27 disclosing

interconnection layer 3 having a first interconnection portion with a small line width 3b branching off a second interconnection portion with a large line width 3a. *See id.*, ¶¶[0094]-[0103], Figs. 23-27. Kamoshima teaches having via 4a (for connection to another interconnect layer) arranged along small line width portion 3b and dummy via 4c arranged in vicinity of a “connection portion” between the two interconnection portions. *Id.*, ¶¶[0095], [0099]. Annotated Figure 24 discloses these features:



101. Kamoshima further discloses that the dummy vias can be connected to the top surface of an interconnect, and that the dummy vias can be further connected at their upper end to a dummy interconnect. *Id.*, ¶[0090], Figs. 16, 22. Kamoshima shows in Figure 22 that the dummy via 4c can be connected to a top surface of the

interconnection layer 3, and that a top of the dummy via 4c can be connected to the dummy interconnection layer 6. *Id.*, ¶[0090], Fig. 22. Kamoshima confirms that dummy interconnection layer 6 “does not electrically connect interconnection layer 3 to another element.” *Id.*

102. Because Kamoshima is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the '623 patent purports to address (e.g., interconnect reliability), Kamoshima is analogous art. TSMC-1001, 1:14-15, 2:39-42; TSMC-1009, ¶¶[0002], [0004]-[0007].

X. CLAIMS 1-4, 7-9, 11-18, 21-22, 25-26, 28, 32, 39-40, 42, AND 45-47 ARE UNPATENTABLE

103. In my opinion, claims 1-4, 7-9, 11-18, 21-22, 25-26, 28, 32, 39-40, 42, and 45-47 are unpatentable on the grounds outlined below:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1	1-3, 7, 11-16, 21-22, 25-26, 28, 32, 39-40, 42	102	Watanabe
2	4, 8	103	Watanabe, Kurashima
3	9, 17-18	103	Watanabe, Iizuka
4	45-47	103	Watanabe, Kamoshima
5	1, 11-15, 17-18, 21-22, 25-26, 28, 32, 39-40	102	Hasunuma

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
6	2, 8	103	Hasunuma, Kurashima
7	1, 16, 45-46	103	Aoyagi
8	47	103	Aoyagi, Hasunuma
9	1, 2, 4, 7, 14, 42	102/103	Kunikiyo
10	9, 17	103	Kunikiyo, Iizuka
11	3	103	Kunikiyo, Watanabe

A. Ground 1: Watanabe Anticipates Claims 1-3, 7, 11-16, 21-22, 25-26, 28, 32, 39-40, 42

104. I believe that Watanabe anticipates Claims 1-3, 7, 11-16, 21-22, 25-26, 28, 32, 39-40, and 42 as detailed below. I previously summarized Watanabe. *Supra*, §IX.A. I first address claim 1, which is the independent claim, and then address each of the noted dependent claims.

1. Claim 1²

105. Watanabe's first embodiment is applied to the elements of claim 1 immediately below, and then the subsequent sections apply Watanabe's other embodiments to claim 1 thereafter.

² See Appendix B for all claim language.

a) **Watanabe's First Embodiment Discloses Claim 1**

(1) [1.pre] – “*A semiconductor device*”

106. The preamble of claim 1 calls for a “semiconductor device,” which Watanabe discloses. As examples, Figures 1, 12A-12N, and 14 each disclose a semiconductor device. TSMC-1004, Title, Abstract, ¶¶[0003], [0038], [0051], [0135]-[0136], [0170]-[0173].

107. Figures 1 and 14 of Watanabe, showing a semiconductor device, are reproduced below:

FIG. 1

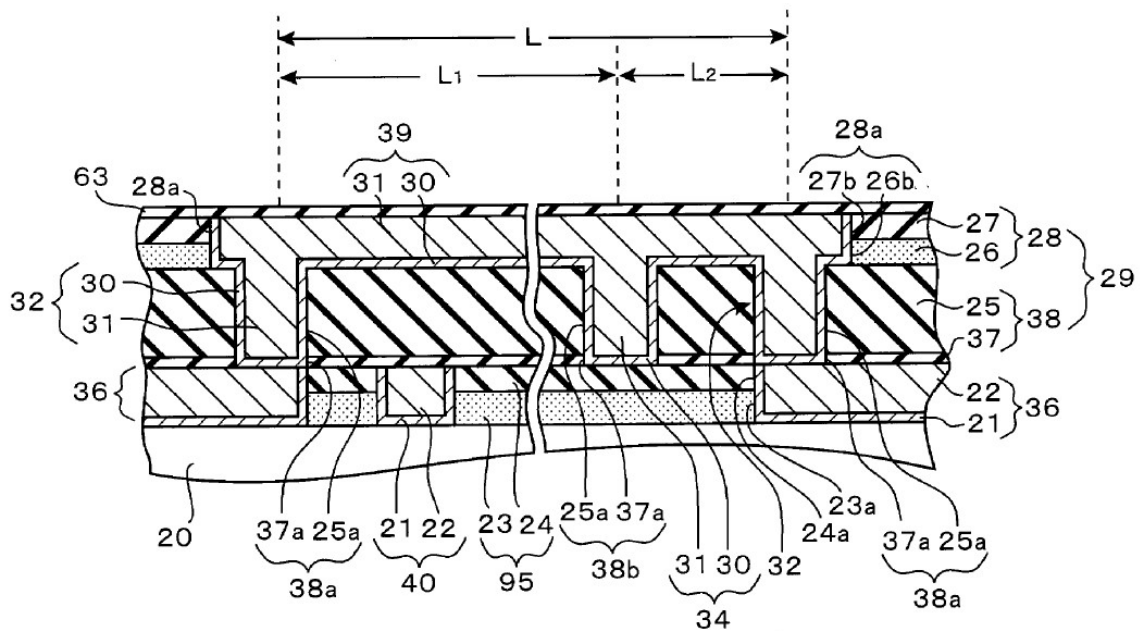
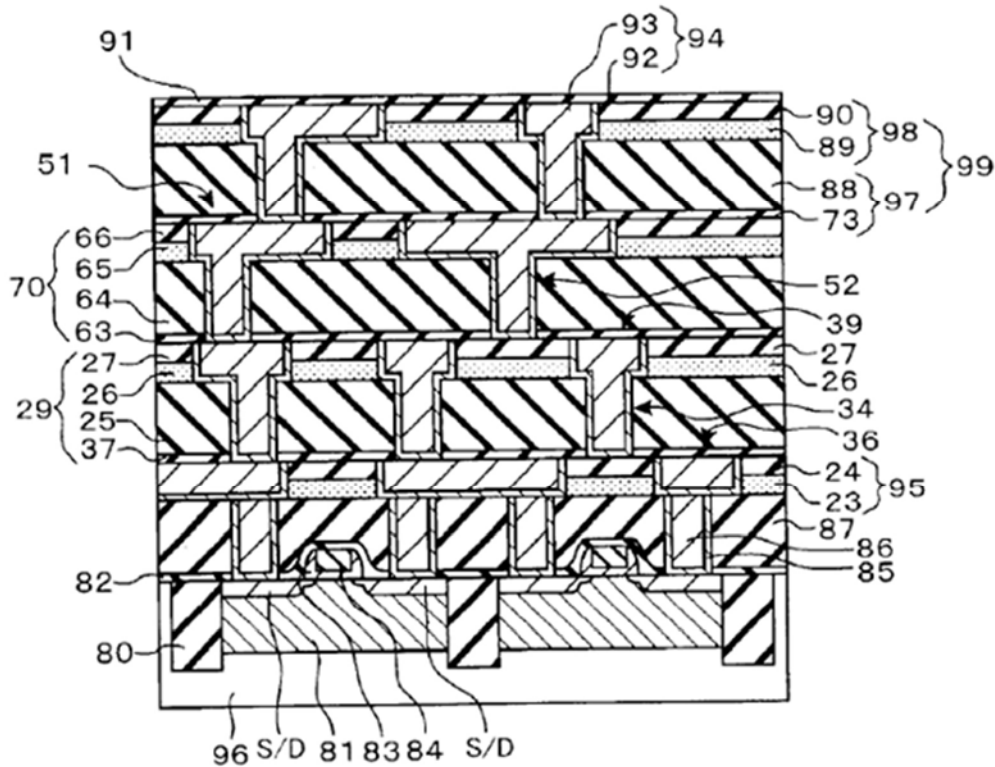


FIG. 14



See *id.*, ¶¶[0172]-[0173] (explaining that “layer 20” in the disclosed embodiments represents or includes the devices fabricated in/on semiconductor (silicon) substrate 96, as disclosed in more detail in Figure 14).

(2) [1.a] – “a semiconductor substrate”

108. Element [1.a] calls for a “semiconductor substrate,” which Watanabe discloses.

109. Watanabe’s Figure 1 discloses structures formed upon underlying layer 20 that includes a “silicon wafer (semiconductor substrate).” TSMC-1004, ¶¶[0061], Fig. 1; see also *id.* ¶¶[0051], [0135]-[0136], [0172]-[0173], Figs. 12A, 14. Annotated Figures 1 and 14 each disclose this feature:

FIG. 1

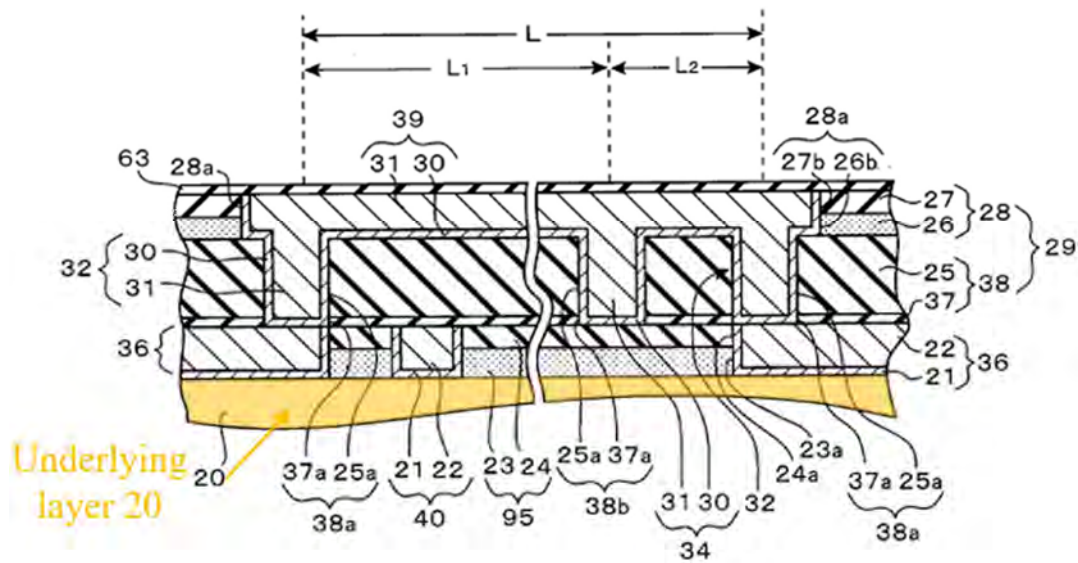
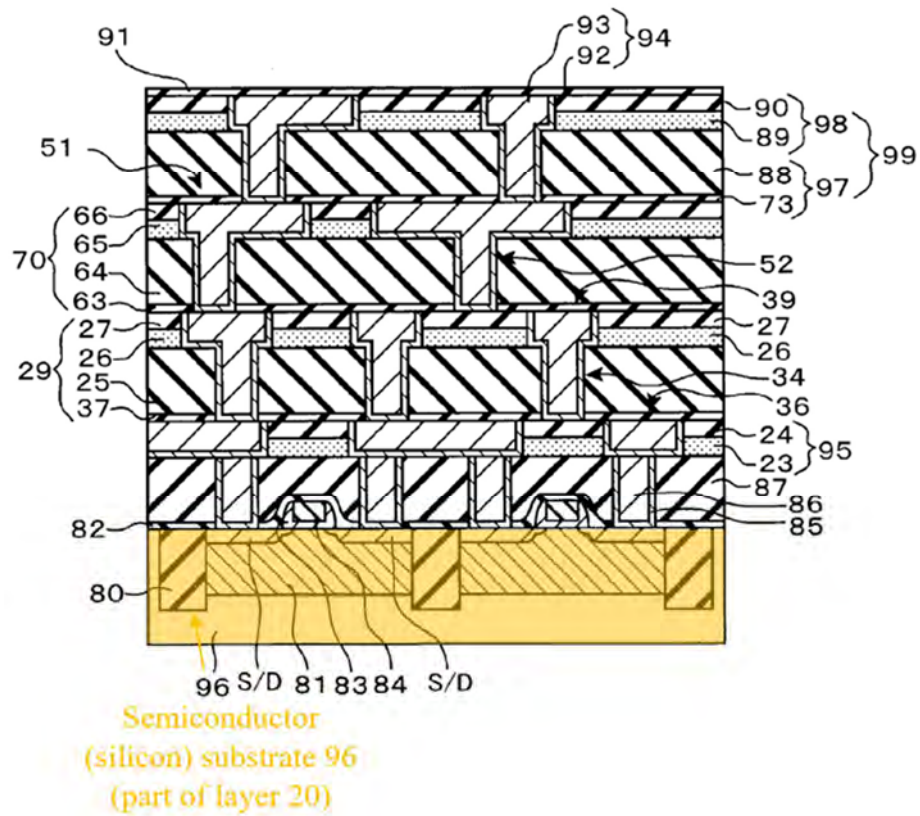


FIG. 14



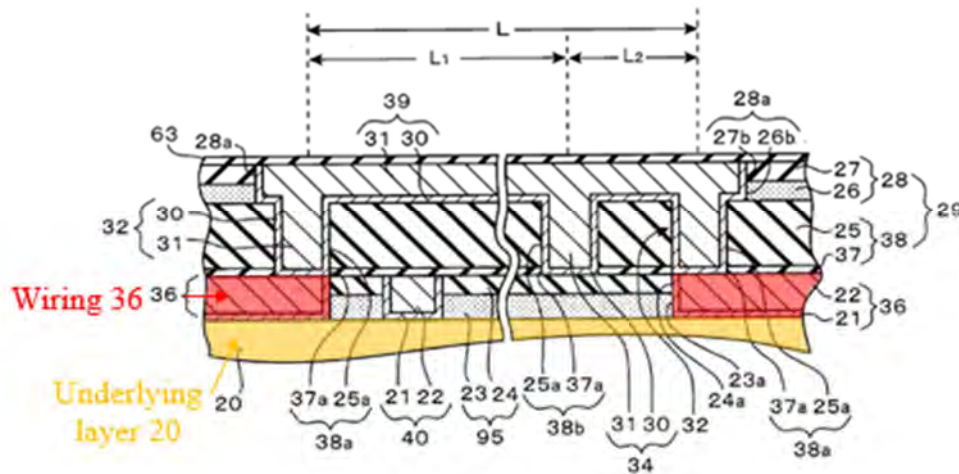
Id., Figs. 1, 14 (annotated).

(3) [1.b] – “a first interconnect formed on the semiconductor substrate”

110. Element [1.b] calls for “a first interconnect formed on the semiconductor substrate,” which Watanabe discloses with its wiring 36.

111. Watanabe describes its interconnects using the term “wiring” (e.g., “wiring 36,” “wiring 39,” “wiring 51”). A POSITA understood that such wirings constitute “interconnects” as those terms are understood in the art because a wiring is a structure formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:20-25. Wiring/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:36-38. Watanabe’s wiring 36 is formed within insulating film 95, which rests on the underlying layer 20 that includes the semiconductor substrate, so the wiring 36 is an interconnect formed on the semiconductor substrate. TSMC-1004, ¶¶[0051], [0061], [0064]-[0065], [0136]-[0144], [0174], Figs. 1-9, 12A-12D, 14. Annotated Figure 1 shows these features:

FIG. 1



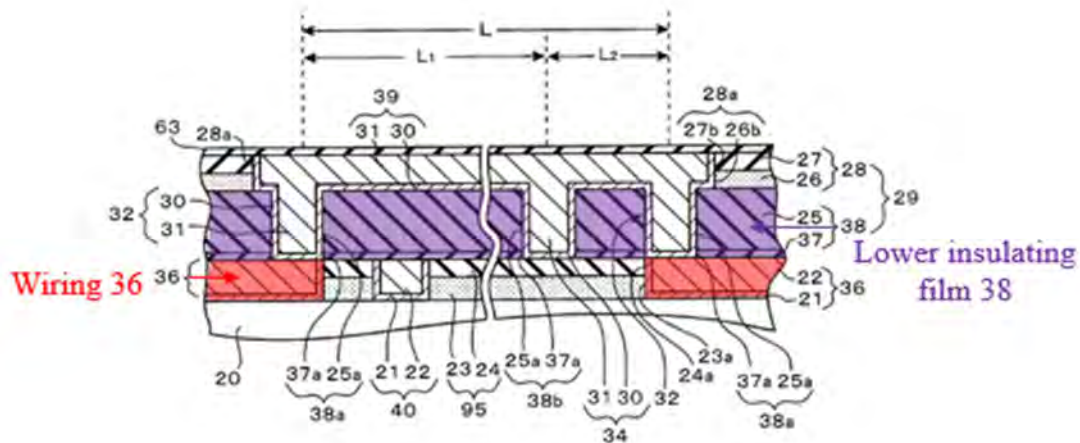
Id., Fig. 1 (annotated).

(4) [1.c] – “a first insulating film formed on the first interconnect”

112. Element [1.c] calls for “a first insulating film formed on the first interconnect,” which Watanabe discloses with its lower insulating film 38 as one example.

113. Watanabe’s lower insulating film 38 is formed on the wiring 36, as seen in Figures 1 and 14. TSMC-1004, ¶¶[0066], [0149]-[0150], [0175], Figs. 1, 3, 12E, 12M, 14. This lower insulating film 38 includes a silicon nitride film 37 and a silicon oxide film 25. It is formed on the wiring 36. *Id.* Annotated Figure 1 below shows these features:

FIG. 1



Id., Fig. 1 (annotated).

114. Additionally, for purposes of applying Watanabe to the challenged claims, the “first insulating film” could also be read on Watanabe’s entire insulating film stack 29, which includes upper and lower insulating films 28 and 38. *Id.*, ¶¶[0149]-[0152].

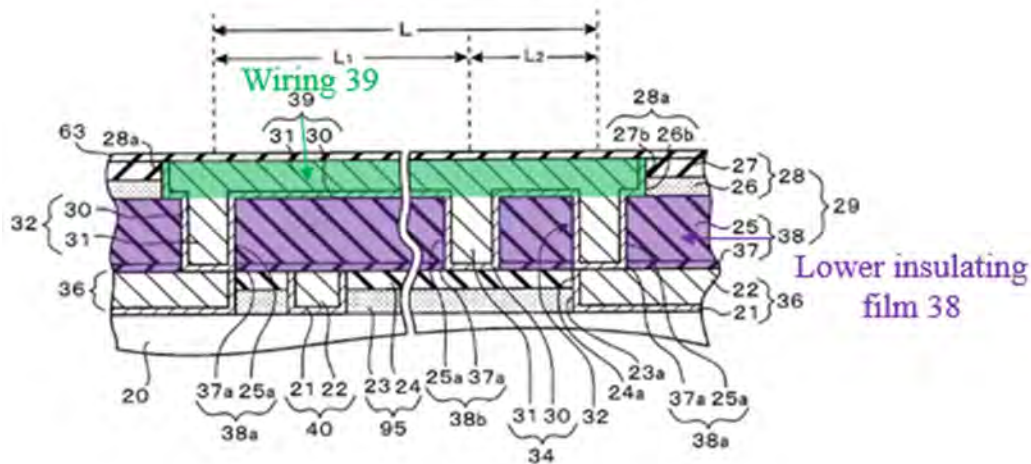
(5) [1.d] - *“a second interconnect formed on the first insulating film”*

115. Element [1.d] calls for “a second interconnect formed on the first insulating film,” which Watanabe discloses with its wiring 39.

116. The wiring 39 is formed on Watanabe's lower insulating film 38 (corresponding to the claimed "first insulating film"). TSMC-1004, ¶¶[0067], [0069], [0153]-[0168], [0175], Figs. 1, 12E-12M, 14. An annotated version of

Figure 1 highlighting the wiring 39 on lower insulating film 38 (the claimed “first insulating film”) is reproduced below:

FIG. 1



Id., Fig. 1 (annotated).

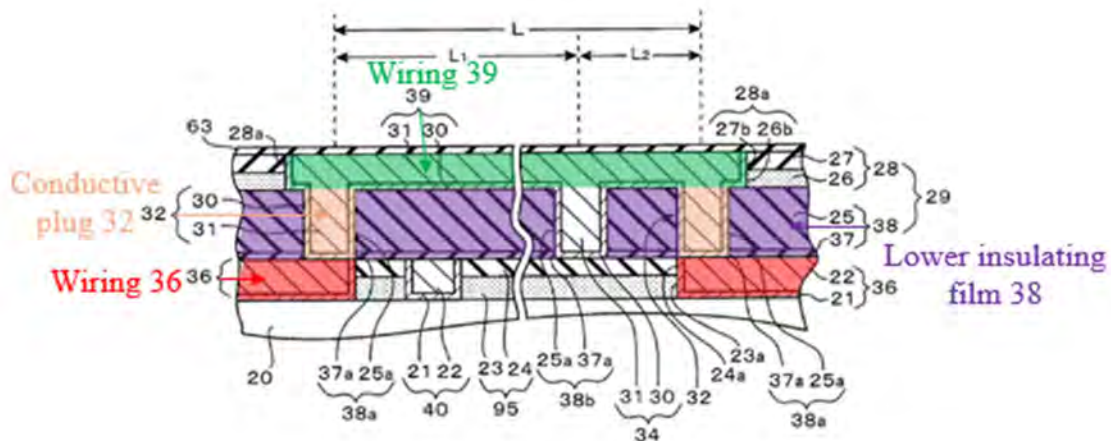
(6) [1.e] - *“a via formed through the first insulating film and connecting between the first and second interconnects”*

117. Element [1.e] calls for “a via formed through the first insulating film and connecting between the first and second interconnects,” which Watanabe discloses with its conductive plug 32 formed within via hole 38a.

118. Watanabe's via hole 38a extends through the lower insulating film 38 in via hole 38a, and is filled with conductive metal to form conductive plug 32. TSMC-1004, ¶¶[0067]-[0070], [0173], [0155]-[0168], Figs. 1, 12G-12M, 14. Conductive plug 32 is thus a "via" that is through the claimed "first insulating film"

(i.e. lower insulating film 38), and this conductive plug electrically connects the wiring 36 and the wiring 39 (which are the “first interconnect” and “second interconnect,” respectively). *Id.*, ¶¶[0073], [0168]. An annotated version of Figure 1 highlighting this structure is reproduced below.

FIG. 1



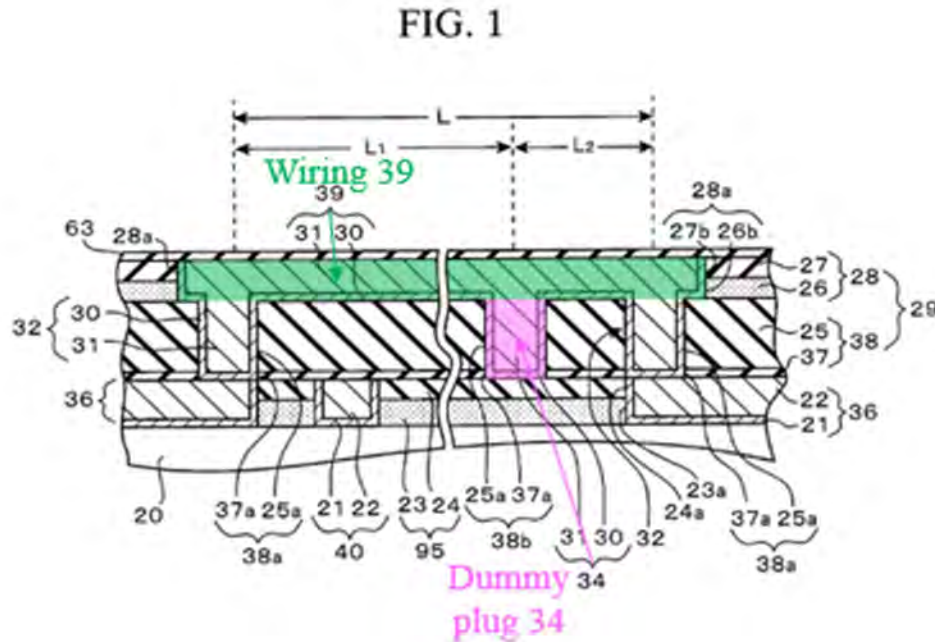
Id., Fig. 1 (annotated).

(7) [1.f] - “*a dummy via connected to the second interconnect*”

119. Element [1.f] calls for “a dummy via connected to the second interconnect,” which Watanabe discloses with its dummy plug 34 formed within dummy via hole 38b.

120. Dummy via hole 38b extends through the lower insulating film 38 (which are constituted by films 37 and 25). TSMC-1004, ¶¶[0067]-[0072], [0079], [0164]-[0168], Figs. 1, 12G-12M, 14. Dummy via hole 38b is filled with conductive

metal to form dummy plug 34, which is formed integrally with the wiring 39 (using dual damascene) and thus connected to the claimed “second interconnect.” *Id.* An annotated version of Figure 1 highlighting the dummy plug 34 connected to the wiring 39 is reproduced below.



Id., Fig. 1 (annotated).

(8) [1.g] - “*wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough*”

121. Element [1.g] calls for “wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough,” which Watanabe discloses with its dummy plug 34.

122. Watanabe's dummy plug 34 is formed integrally with the wiring 39 (using dual damascene) and includes a conductive barrier metal layer 30 and conductive copper film 31. TSMC-1004, ¶¶[0067]-[0072], [0164]-[0168], [0185], Figs. 1, 12K-12M, 14. The dummy plug 34, therefore, plainly made of conductive film. *Id.*

123. Watanabe's dummy via hole 38b extends to a "non-forming region of the first wiring 36." *Id.*, ¶¶[0067], [0079], Figs. 1, 12K-12M, 14. The dummy plug 34 extends to and terminates in a "non-forming region" of insulating film 95, i.e., it is not connected to a second active circuit element such as wiring 36 or wiring 40. *Id.*, ¶¶[0061], [0067], [0079], [0165], Figs. 1, 12K-12M, 14.

124. A POSITA would understand that Watanabe's "dummy plugs 34" are "arranged so as to be incapable of having current flow therethrough." In this regard, the '623 patent specification states:

A dummy via and a dummy interconnect herein means a pseudo via or a pseudo interconnect which do not constitute a closed circuit in actual use of a device with an interconnection structure including these via and interconnect (i.e., **no current flows therein** during actual use of the device.)

TSMC-1001, 3:14-18 (emphasis added).

125. The '623 patent goes on to explain that:

[N]either the dummy interconnect 102B nor the dummy via 110B constitutes a closed circuit in actual use. That is, even if the dummy interconnect 102B and the dummy via 110B are omitted in the interconnection structure shown in FIG. 2B, a device with this interconnection structure is operable at least immediately after fabrication.

Id., 10:26-32 (emphasis added).

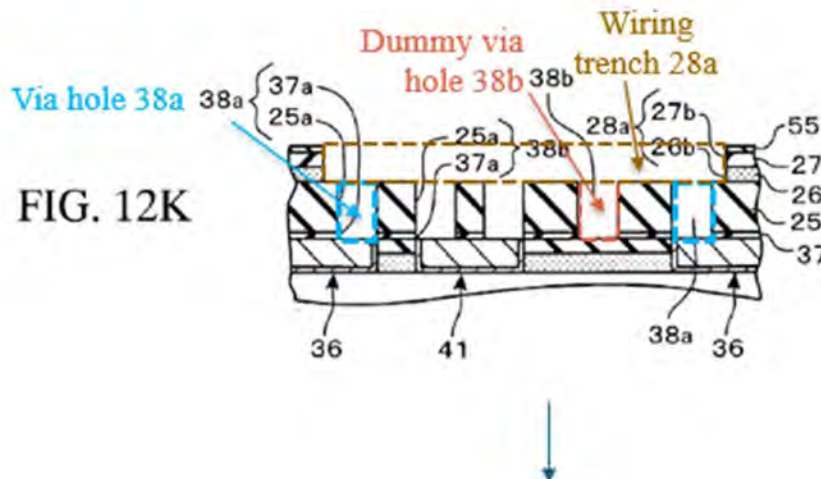
126. Watanabe’s “dummy” plugs 34 do not constitute part of a closed circuit in actual use of the device, i.e., no current flows through dummy plugs 34 during actual use of the device. As seen in Figure 1, these “dummy” plugs 34 are only connected at one end to an active element (i.e., “wiring 39”), while the other end is not connected to a second active circuit element (it instead ends at insulating film 95). A POSITA would recognize that no current flows through the dummy plugs 34 due to this lack of connection to a second active circuit element.

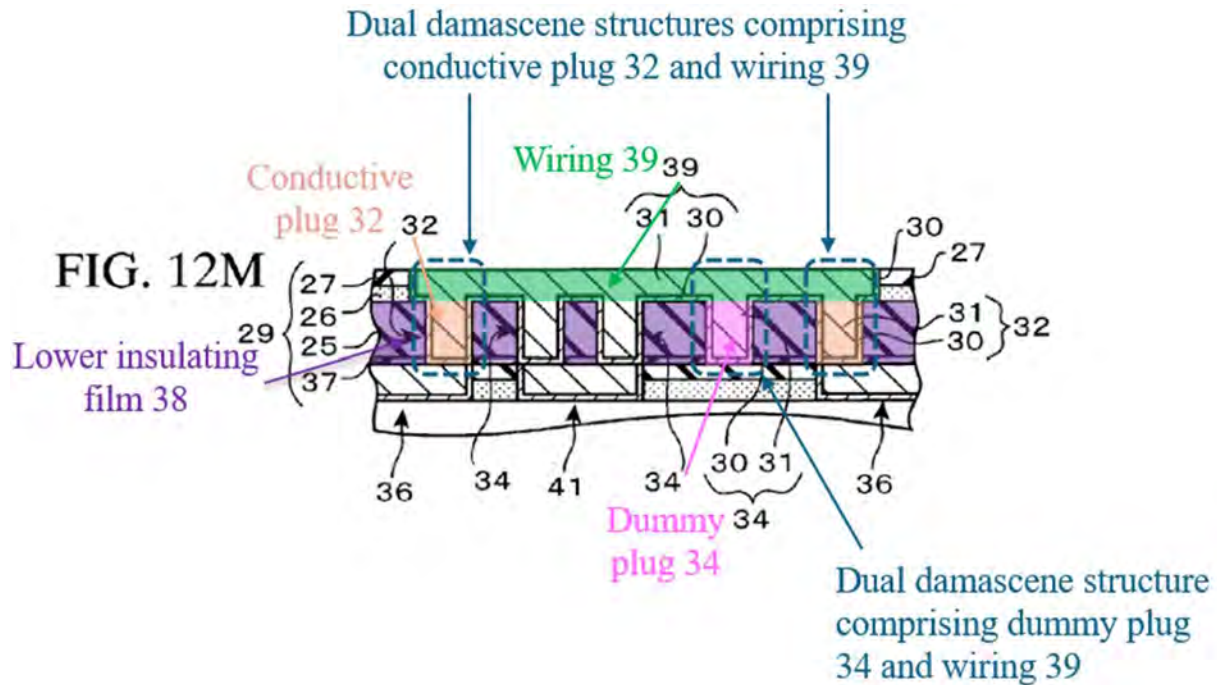
127. Also, Watanabe’s device would still be operable if dummy plugs 34 were omitted because dummy plugs 34 do not carry current/signals as part of a closed circuit during actual use of the device. Instead, current flows between the wiring 36 and wiring 39 through conductive plugs 32, forming a closed circuit for operation of the device. TSMC-1004, ¶[0073], Figs. 1, 14.

(9) [1.h] - *“the second interconnect and the via form a dual damascene structure”*

128. Element [1.h] calls for “the second interconnect and the via form a dual damascene structure,” which Watanabe discloses.

129. Watanabe discloses that the wiring 39 (which is the claimed “second interconnect”) and the conductive plug 32 (which is the claimed “via”) are formed using a “dual damascene process” and, thus, they form a dual damascene structure. TSMC-1004, ¶¶[0067]-[0072], [0135], [0153]-[0168], Figs. 1, 12E-12M, 14. Watanabe specifically describes the simultaneous, integral formation of the wiring 39 (“second interconnect”) and the plug 32 (“via”) by filling the wiring trench 28a and the via hole 38a with the barrier metal layer 30 and the copper film 31, as disclosed in Figures 12K-12M. See annotated Figure 12K, 12M below:





Id., ¶¶[0067]-[0068], [0072], [0166]-[0168], Figs. 12K-12M.

130. Accordingly, a POSITA would understand that Watanabe’s second wiring layer 39 and conductive plug 32 (the claimed second interconnect and via, respectively) form a dual damascene structure. The same applies to the structures in Figure 14. *Id.*, Fig. 14.

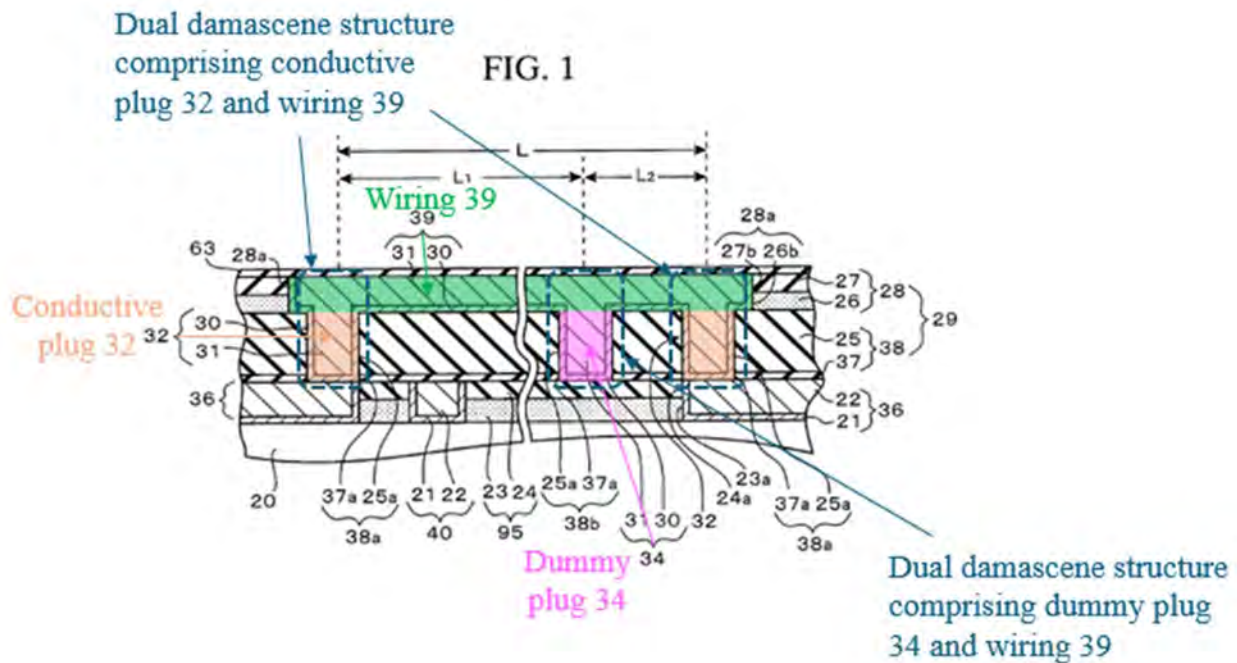
(10) [1.i] - “the second interconnect and the dummy via from a dual damascene structure”

131. Element [1.i] calls for “the second interconnect and the dummy via from a dual damascene structure,” which Watanabe discloses.

132. The same dual damascene process already described above, in connection with element [1.h], also forms the dummy plug 34 (which is the claimed “dummy via”) simultaneously and integrally with the wiring 39 (which is the

claimed “second interconnect”), by filling the wiring trench 28a and the dummy via hole 38b with the barrier metal layer 30 and the copper film 31, as illustrated above in annotated Figures 12K,12M above. TSMC-1004, ¶¶[0067]-[0072], [0135], [0153]-[0168], Figs. 1, 12E-12M, 14.

133. Annotated Figure 1 discloses the completed device, with wiring 39 and plug 32, as well as wiring 39 and dummy plug 34 forming dual damascene structures (see also *supra*, ¶76):



134. Accordingly, a POSITA would understand that Watanabe’s second wiring layer 39 and dummy plug 34 (the claimed second interconnect and dummy via) form a dual damascene structure. The same applies to the structures in Figure 14. *Id.*, Fig. 14.

b) Watanabe's Second Embodiment Discloses Claim 1

135. Watanabe's second embodiment, shown in Figure 3 (cross-section) and Figure 4 (plan view) and described at paragraphs ¶¶[0088]-[0092], also discloses all limitations of claim 1.

136. Just as with the first embodiment, Watanabe's second embodiment includes a semiconductor substrate (the substrate of underlying layer 20), a first interconnect (the wiring 36), a first insulating film (the lower insulating film 38), a second interconnect (the wiring 39), a functional via (the plug 32), and a dummy via (the dummy plug 34). TSMC-1004, ¶¶[0089]-[0092], Figs. 3-4; *supra*, §§X.A.1.(a).(1)-(a).(10). Thus, these common features in the second embodiment meet their respective claim elements like the first embodiment.

137. In Watanabe's second embodiment, instead of the lower end of dummy plug 34 terminating at insulating layer 95 as in the first embodiment, there is an added feature that at least some of the dummy plugs 34 connect to an isolated "dummy wiring 41" at their lower end.

138. This is seen in annotated Figures 3 and 4:

FIG. 3

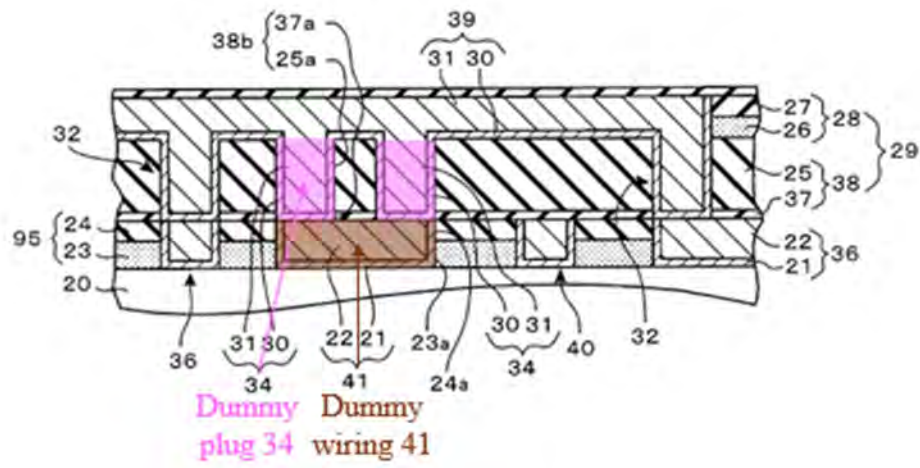
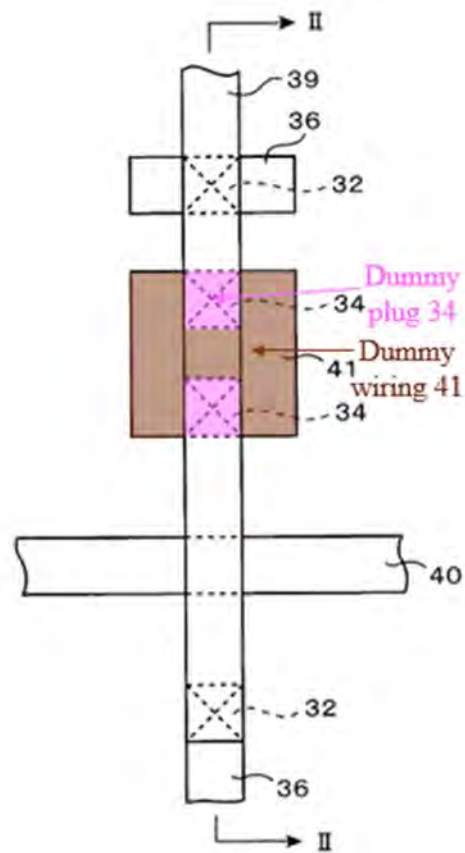


FIG. 4



Id., ¶¶[0090]-[0092], [0165], [0186], Figs. 3-4, 12E, 12K-12M.

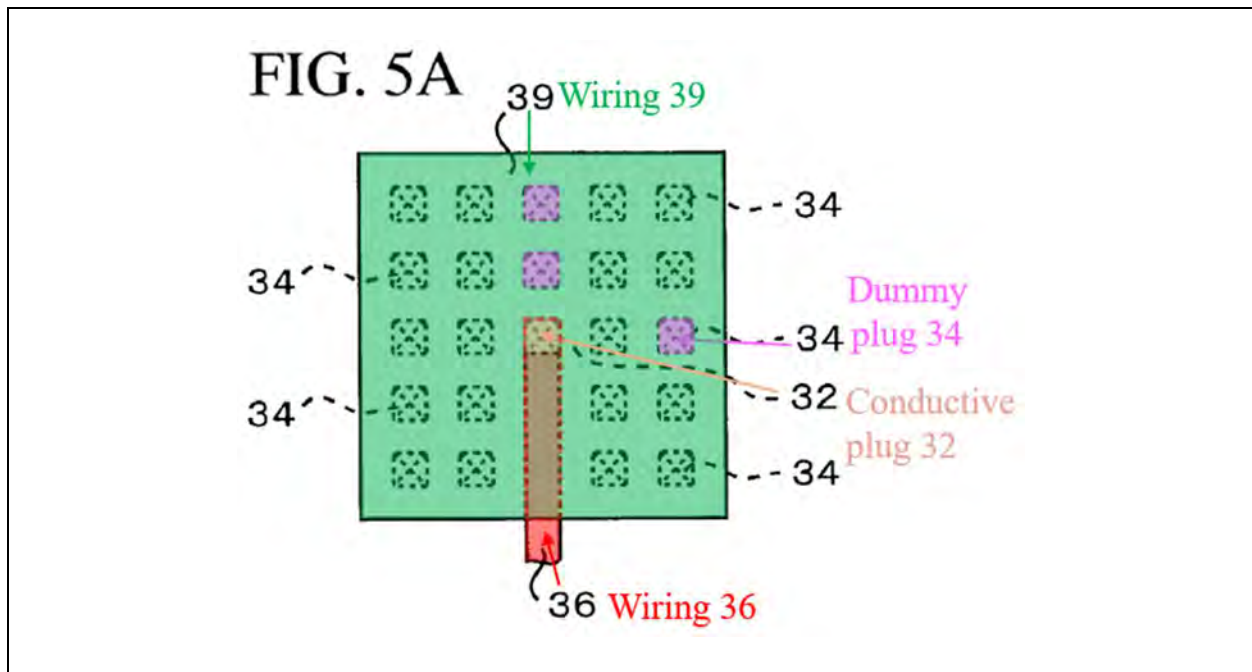
139. Just like Watanabe's first embodiment, a POSITA would understand that the "dummy plugs 34" in Watanabe's second embodiment are likewise "arranged so as to be incapable of having current flow therethrough." In this regard, the wiring 41 is itself "dummy" wiring that does not connect to any other active circuit element to form part of a closed circuit during actual device use. *Id.*, ¶¶[0089], [0135], [0166]-[0168], [0186]. As Watanabe explains, "the dummy wiring is provided in the non-forming region of the first wiring." *Id.*, ¶¶[0028]-[0029], [0090], [0186]. The dummy wiring 41 is for enhancing mechanical strength. *Id.*, ¶¶[0091], [0186]-[0187].

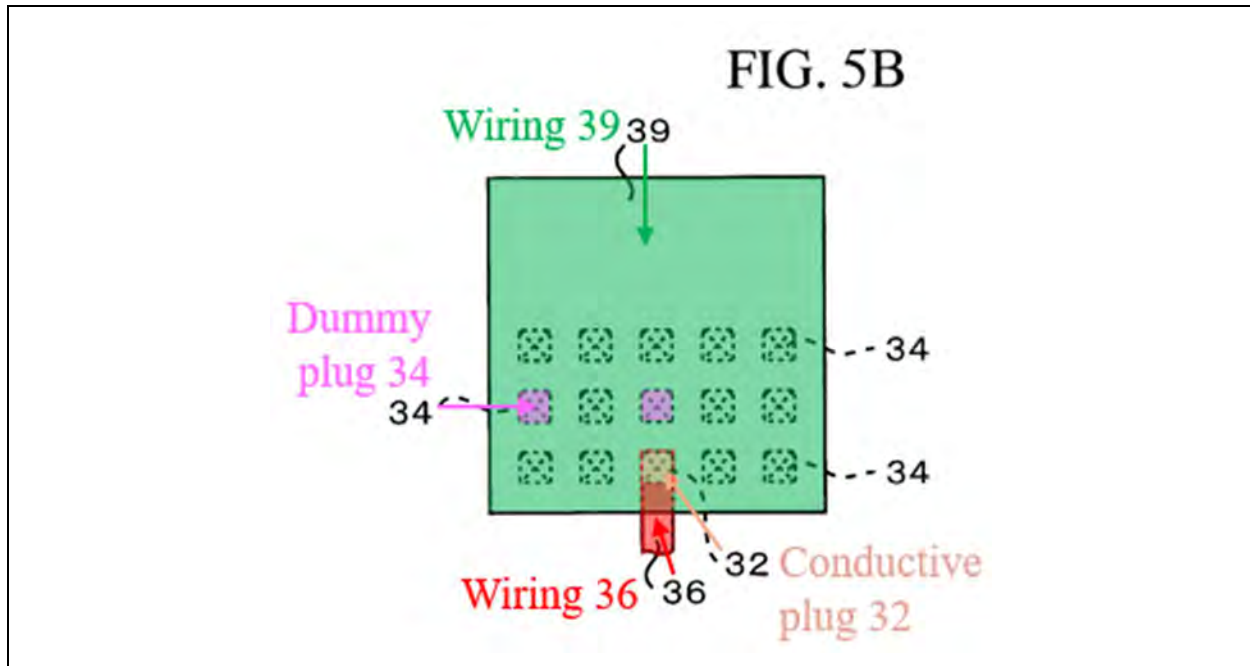
140. Additionally, both the dummy plugs 34 and dummy wiring 41 could be omitted from Watanabe's structure without affecting device operation, since the current/signals are carried between wirings 36 and 39 through conductive plugs 32 as part of a closed circuit during actual device use. *Id.*

141. Also, the second embodiment uses the same dual damascene process as with the first embodiment, resulting in integral formation of the second interconnect (the wiring 39) with both the functional vias (plugs 32) and the dummy vias (dummy plugs 34). *Id.*, Fig. 3, ¶¶[0089], [0135], [0166]-[0168].

c) Watanabe's Third Embodiment Discloses Claim 1

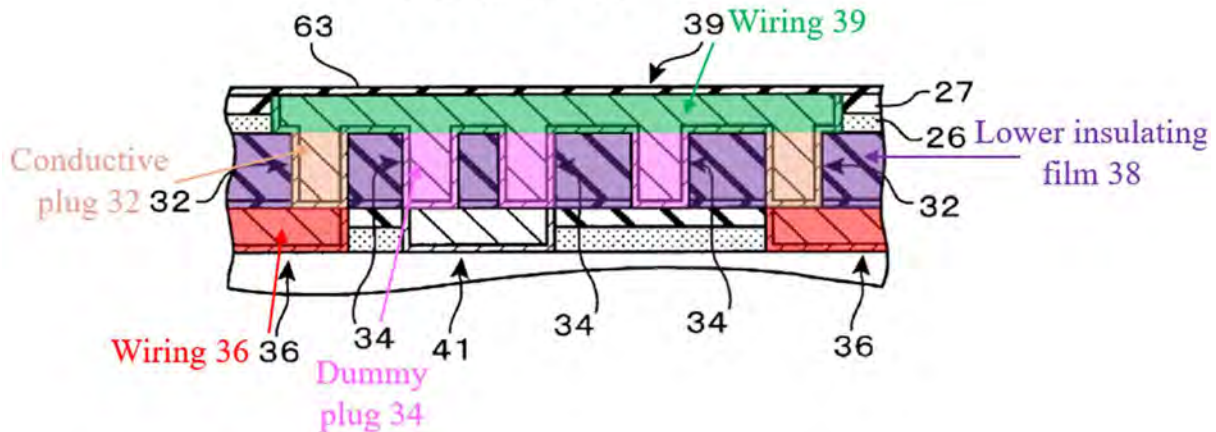
142. Watanabe's third embodiment is the same in relevant aspects as the first and second embodiments, with the third embodiment showing an alternative shape for the wiring 39 and different positions of plug 32 and different positions and numbers of dummy plugs 34, as exemplified in Figures 5A and 5B below:





TSMC-1004, ¶¶[0093]-[0099], Figs. 5A-5C. In Watanabe’s Figures 5A-5C, a POSITA would have understood that each of the hatched squares not otherwise labeled as a conductive plug 32 constitutes a dummy plug 34, even though I highlight only a few exemplary dummy plugs 34 in the above annotations. *Id.*, ¶¶[0096]-[0098]. Also, given Watanabe’s express statement that Figure 12 represents “sectional views showing a method of manufacturing the semiconductor device according to the embodiments of the present invention,” (*id.*, ¶¶[0049], [0135] (emphasis added); *see also id.*, ¶[0094] (noting the omission of various layers in Figure 5 for easier understanding)), a POSITA understood that the cross-section of Figure 12N discloses the basic structure of Watanabe’s third embodiment (e.g., Figure 5B):

FIG. 12N



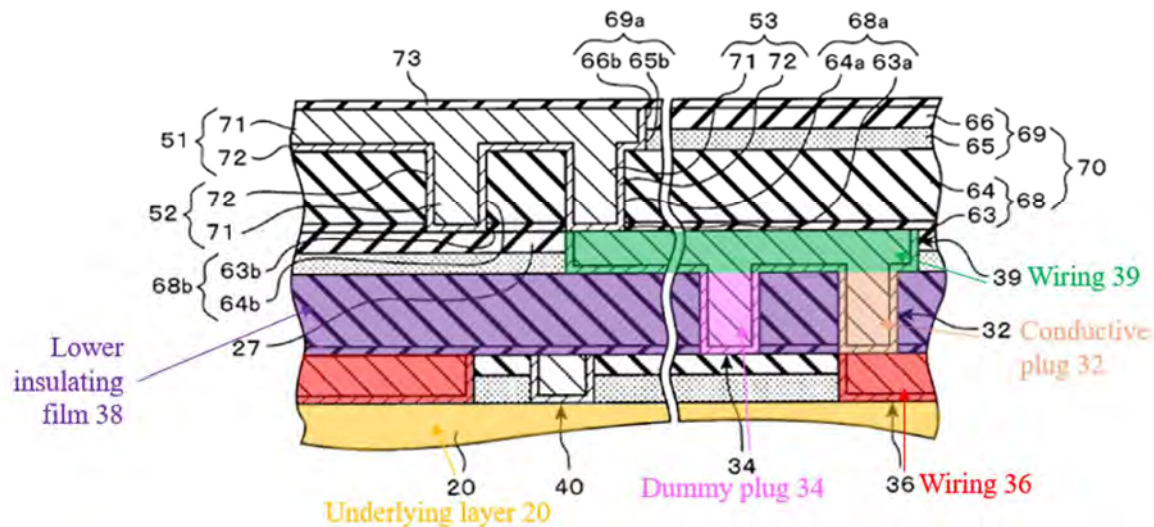
143. For the third embodiment (Figures 5A-5C), Watanabe intentionally omits depicting the underlying layer 20 and insulating films, while referencing Figures 1 and 3. *Id.*, ¶[0094]. As the foregoing figures confirm, Watanabe's third embodiment similarly discloses claim 1 for the same reasons as Watanabe's first and second embodiments.

d) Watanabe's Fifth Embodiment Discloses Claim 1

144. Watanabe's fifth embodiment illustrates a semiconductor device having a three-level interconnect structure, as disclosed in Figure 8 (cross-section) and Figure 9 (plan view). TSMC-1004, ¶¶[0115]-[0133], Figs. 8-9. The fifth embodiment also discloses claim 1.

145. Watanabe's fifth embodiment includes the same structure as shown in Figure 1. Therefore, as one basis, the fifth embodiment discloses claim 1 based on the same analysis that I laid out above for claim 1, as shown in Figure 8 below (a first mapping). *See supra*, §§X.A.1.(a).(1)-(a).(10).

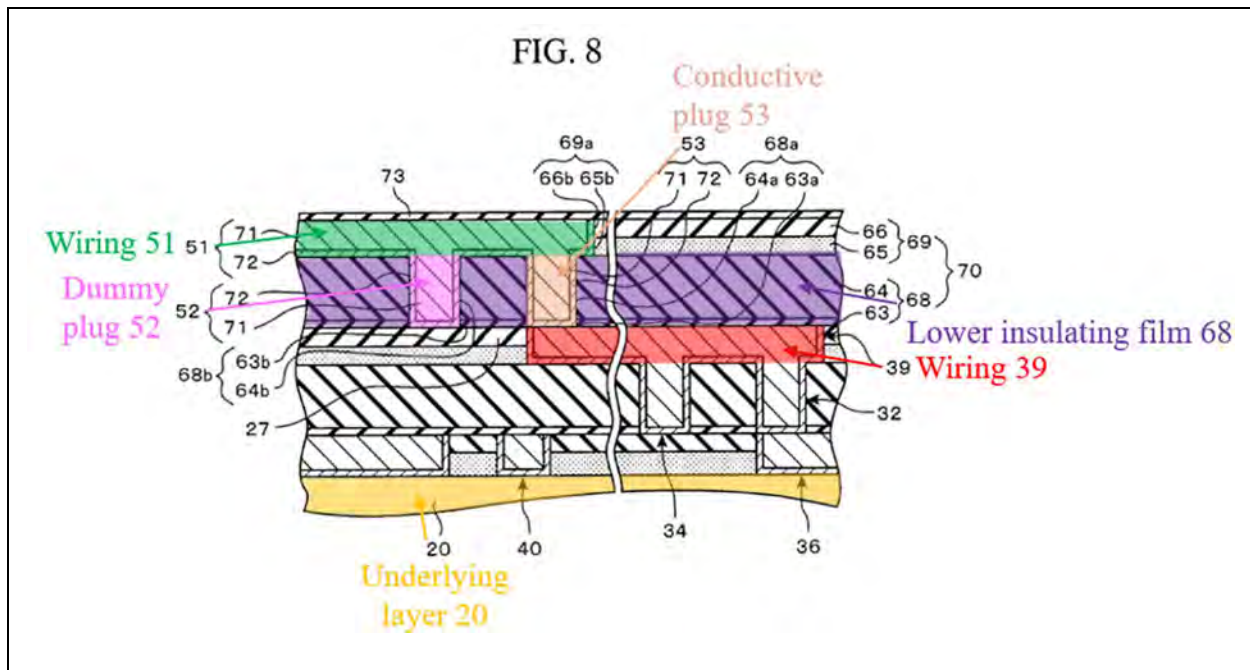
FIG. 8



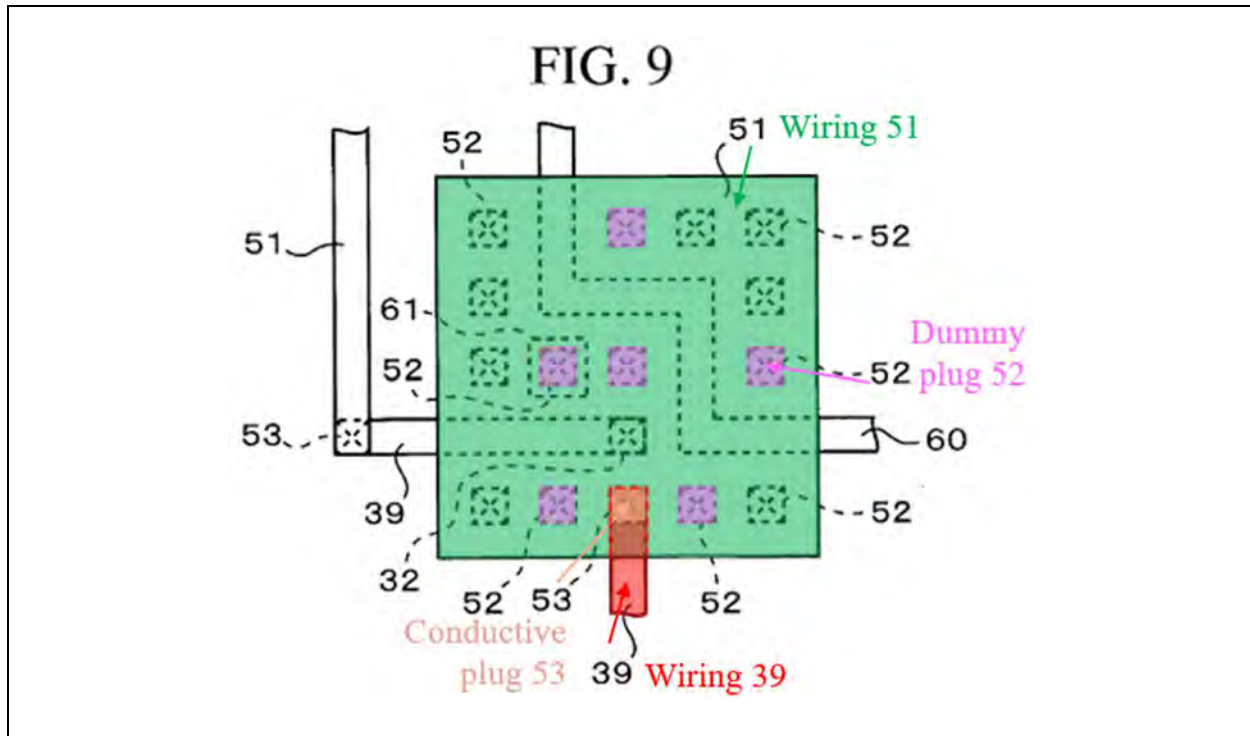
146. In addition, Watanabe's fifth embodiment includes an additional interconnect level, and the second and third level interconnect structure also discloses claim 1 as follows. To start with, Watanabe's fifth embodiment structure is formed on a semiconductor substrate that is part of the underlying layer 20. *Id.*, ¶[0136], Fig. 8; *see also id.* ¶¶[0172]-[0173], Fig. 14 (showing the actual semiconductor devices formed in the semiconductor (silicon) substrate 96).

147. In this alternative mapping, the claimed “first interconnect” corresponds to Watanabe’s wiring 39; the claimed “first insulating film” corresponds to Watanabe’s lower insulating film 68; and the claimed “second interconnect” corresponds to Watanabe’s wiring 51. TSMC-1004, ¶¶[0117]-[0122], [0172]-[0178], Figs. 8-9, 14. Similarly, Watanabe’s conductive plug 53 is the claimed “via,” formed within via hole 68a through the lower insulating film 68 and

connecting the wiring 51 to the wiring 39. *Id.*, ¶¶[0120]-[0122], Figs. 8-9. Further, dummy plug 52 is a “dummy via,” and is connected to the wiring 51. *Id.*, ¶[0122], Figs. 8-9. Annotated versions of Figures 8 and 9 highlighting this alternative, second mapping³ is illustrated below (appreciating that I have only highlighted some exemplary dummy plugs 52 in Figure 9 below):



³ When Watanabe's first embodiment of Figures 1-2 is applied against a claim, the first mapping of Watanabe's fifth embodiment of Figures 8-9 applies equally and is not separately discussed hereinafter. Further discussions of Watanabe's fifth embodiment below apply the second mapping from Figures 8-9.



148. The dummy plug 52 is conductive, being composed of the same barrier metal layer 72 and copper film 71 as the wiring 51. *Id.*, ¶¶[0118], [0122]. It is arranged to be incapable of having current flow therethrough because it extends to and terminates in a “non-forming region” of the insulating film 27 (i.e., where there is no wiring 39) or toward an isolated dummy wiring 61. *Id.*, ¶¶[0118]-[0122], [0127], [0185]-[0186], Figs. 8-9. A POSITA would have understood Watanabe’s dummy plugs 52 (whether or not connected to dummy wiring 61) to constitute the claimed “dummy plug” for the same reasons that I explained previously. *See supra*, §§X.A.1.(a).(7)-(a).(8). Thus, the dummy plugs 52 do not constitute part of a closed circuit in actual use of the device, and the device would still be operable if they were

omitted. Instead, current flows between wiring 39 and wiring 51 through conductive plug 53, which constitute parts of a closed circuit during device operation.

149. Consistent with Watanabe's overall manufacturing approach using a dual damascene process (¶[0135]), the wiring 51 forms a dual damascene structure simultaneously with both the plug 53 and the dummy plug 52. *Id.*, ¶[0135], Fig. 8,12A-12N, ¶¶[0049], [0118]-[0123], [0134]-[0171]. Thus, a POSITA would have understood that the wiring 51 and conductive plug 53 (i.e., the claimed "first interconnect" and "via") form a dual damascene structure, as do wiring 51 and dummy plug(s) 52 (i.e., the claimed "first interconnect" and "dummy via"). *Id.*, ¶¶[0072], [0171]. Indeed, each of the disclosed first to third and fifth embodiments discloses a dual damascene structure of the interconnect with the active via and with the dummy via, respectively. Along with Watanabe's disclosure, this is evidenced by Watanabe's figures themselves. In each of cross-sectional Figures 1, 3, and 8, the wiring 39,51 is a dual damascene structure with conductive plugs 32,53 and dummy plugs 34,52, respectively. A POSITA would appreciate that Watanabe's barrier metal layer 30,72 conformally coats the outer sides of the plugs 32,53, dummy plugs 34,52, and wiring 39,51, all a single, continuous layer. With this conformal barrier layer coating, copper film 31,71 is added to fill the recesses for the plugs 32,53, dummy plugs 34,52, and trench for wiring 39,51 to form a single, unitary copper structure. A POSITA would have recognized this configuration

shown in Figures 1, 3, and 8 as a dual-damascene structure, especially in view of Watanabe's description (*e.g., id.*, ¶¶[0072], [0135], [0161]-[0171], Figs. 12K-12M).

150. Accordingly, Watanabe's fifth embodiment discloses claim 1. *Id.*

2. Claim 2

151. At least each of Watanabe's second and fifth embodiments discloses claim 2.

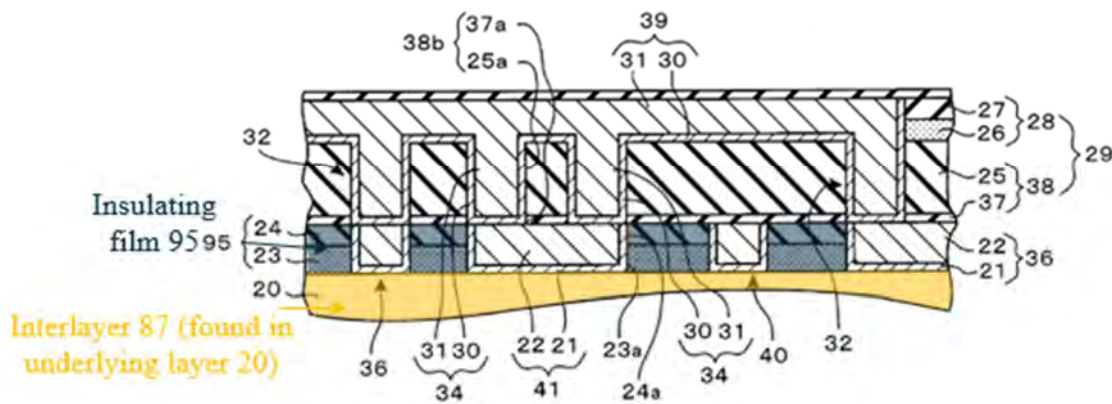
a) [2.a] – “semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate”

152. Element [2.a] recites the “semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,” which Watanabe discloses with its insulating film 95 and interlayer insulating film 87, collectively (or optionally insulating film 87 alone) (second embodiment) and insulating film 29 (fifth embodiment).

153. Watanabe's second embodiment (Figures 3-4) discloses an insulating film 95 that includes a low-dielectric insulating film 23 and silicon oxide film 24. TSMC-1004, ¶¶[0061], [0089], Fig. 3. Further, in connection with Figure 14, Watanabe discloses that the underlying layer 20 includes certain components, including the interlayer insulating film 87 underneath the insulating film 95, and then states that “[t]he underlying layer 20 in the present embodiment and each

embodiments of the present invention is constructed by above members, for example.” *Id.*, ¶¶[0172]-[0174], Fig. 14. Therefore, the Figure 3 embodiment includes an interlayer insulating film 87 and an insulating film 95 which, collectively constitute the claimed “second insulating film,” or optionally interlayer insulating film 87 alone, that is on the semiconductor substrate. See annotated Figure 3 below:

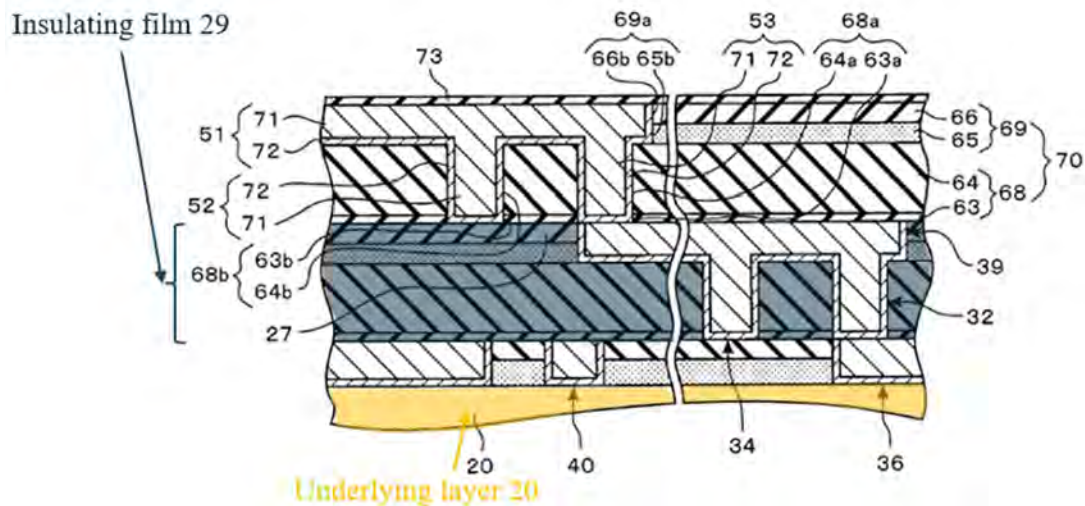
FIG. 3



Id., ¶¶ [0173]-[0174], [0061], [0089], [0094], [0116].

154. Watanabe's fifth embodiment (Figures 8-9), which builds on Figures 1-2, discloses insulating film 29, which includes the upper insulating film 28 and the lower insulating film 38 (together "second insulating film"; alternatively just lower insulating film 38). *Id.*, ¶¶[0066]-[0067], [0116]-[0117], [0172]-[0175], Figs. 1, 8, 14. Insulating film 29 is formed on a semiconductor substrate (which is part of underlying layer 20; and which is expressly shown as "silicon substrate 96" in Figure 14). *Id.* ¶¶[0061], [0172]-[0175]; Figs. 1, 8, 14. Insulating film 29 is indicated in annotated Figure 8 below:

FIG. 8



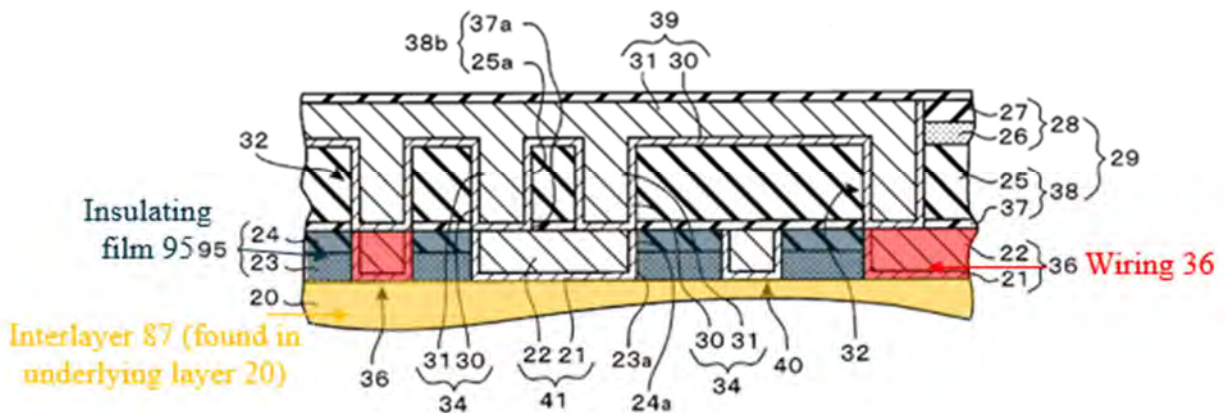
Along with film 27 of insulating film 29 being expressly labeled in Watanabe's Figure 8, a POSITA would understand that insulating film 29 comprises films 37, 25, 26, and 27 based on the common hatching, film thicknesses, and consistency with Figures 1, 3, 12, and 14, which all show the constituent sub-layers of insulating film 29. Additionally, for purposes of claim 2 and Watanabe's fifth embodiment, the "first insulating film" could be comprised of either or both of the films 37 and 25 residing directly above wiring 36 (e.g., lower insulating film 38 as described and annotated in the context of Figure 1 at *supra*, §X.A.1.(a).(4)).

b) [2.b] – “wherein the first interconnect is formed on the second insulating film”

155. Element [2.b] calls for “wherein the first interconnect is formed on the second insulating film,” which Watanabe discloses.

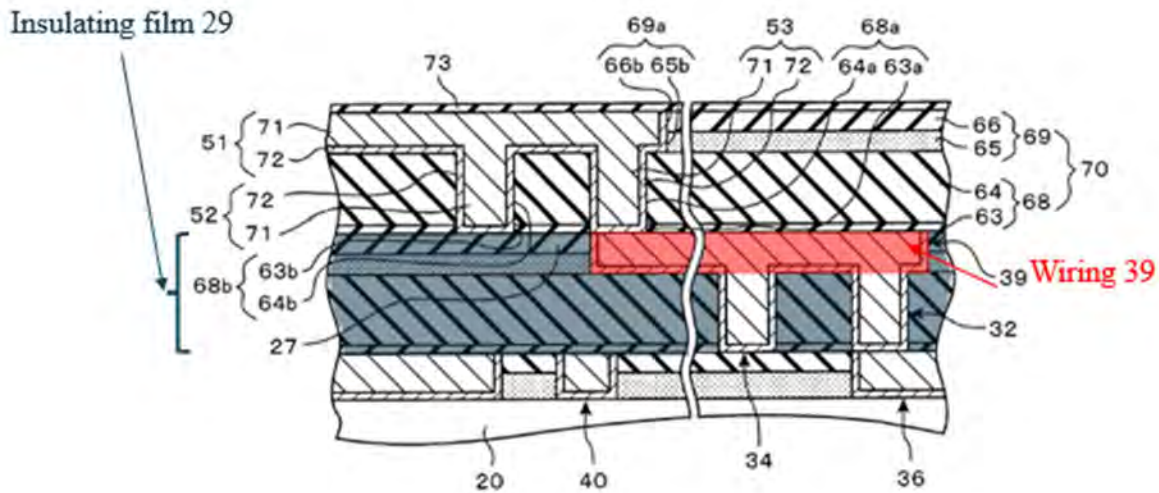
156. In Watanabe's second embodiment (Figures 3-4), the wiring 36 (the "first interconnect") is formed on the insulating film 95/interlayer insulating film 87 (the "second insulating film"; or optionally interlayer insulating film 87). TSMC-1004, ¶¶[0061], [0089], [0172]-[0174], Figs. 3, 14. See annotated Figure 3 below:

FIG. 3



157. In Watanabe's fifth embodiment (Figures 8-9), the wiring 39 (which is the "first interconnect") is formed on the insulating film 29, or the sublayers 37 and 25 (together, lower insulating film 38), with either film 29 or 38 being the "second insulating film." *Id.*, ¶¶[0066]-[0069], [0116]-[0117], [0172]-[0175], Figs. 1, 3, 8, 12, 14. Insulating film 29 is highlighted in the annotations to Figure 8 below:

FIG. 8



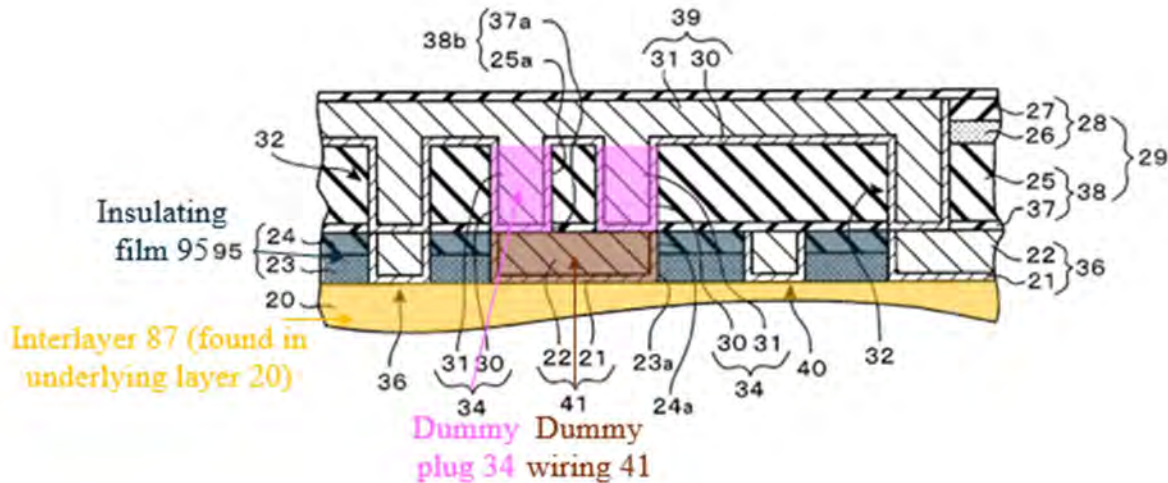
c) [2.c] – *“the dummy via is connected to a first dummy interconnect formed on the second insulating film”*

158. Element [2.c] calls for “the dummy via is connected to a first dummy interconnect formed on the second insulating film,” which Watanabe discloses with its dummy wiring 41 (second embodiment) or dummy wiring 61 (fifth embodiment).

159. In the second embodiment, Figure 3 illustrates a dummy wiring 41 (which is the “first dummy interconnect”). TSMC-1004, ¶¶[0090]-[0091], Fig. 3. The dummy wiring 41 is formed on the interlayer insulating film 87/insulating film 95, which is the “second insulating film”; or alternatively interlayer insulating film 87 alone. *Id.*, ¶¶[0061], [0089]-[0091], [0144]-[0149], [0165], [0172]-[0174], Figs. 3, 12A-12M, 14. The dummy plug 34 (which is the claimed “dummy via”) is

connected to the dummy wiring 41. *Id.*, ¶¶[0090]-[0091], Fig. 3. See annotated Figure 3 below:

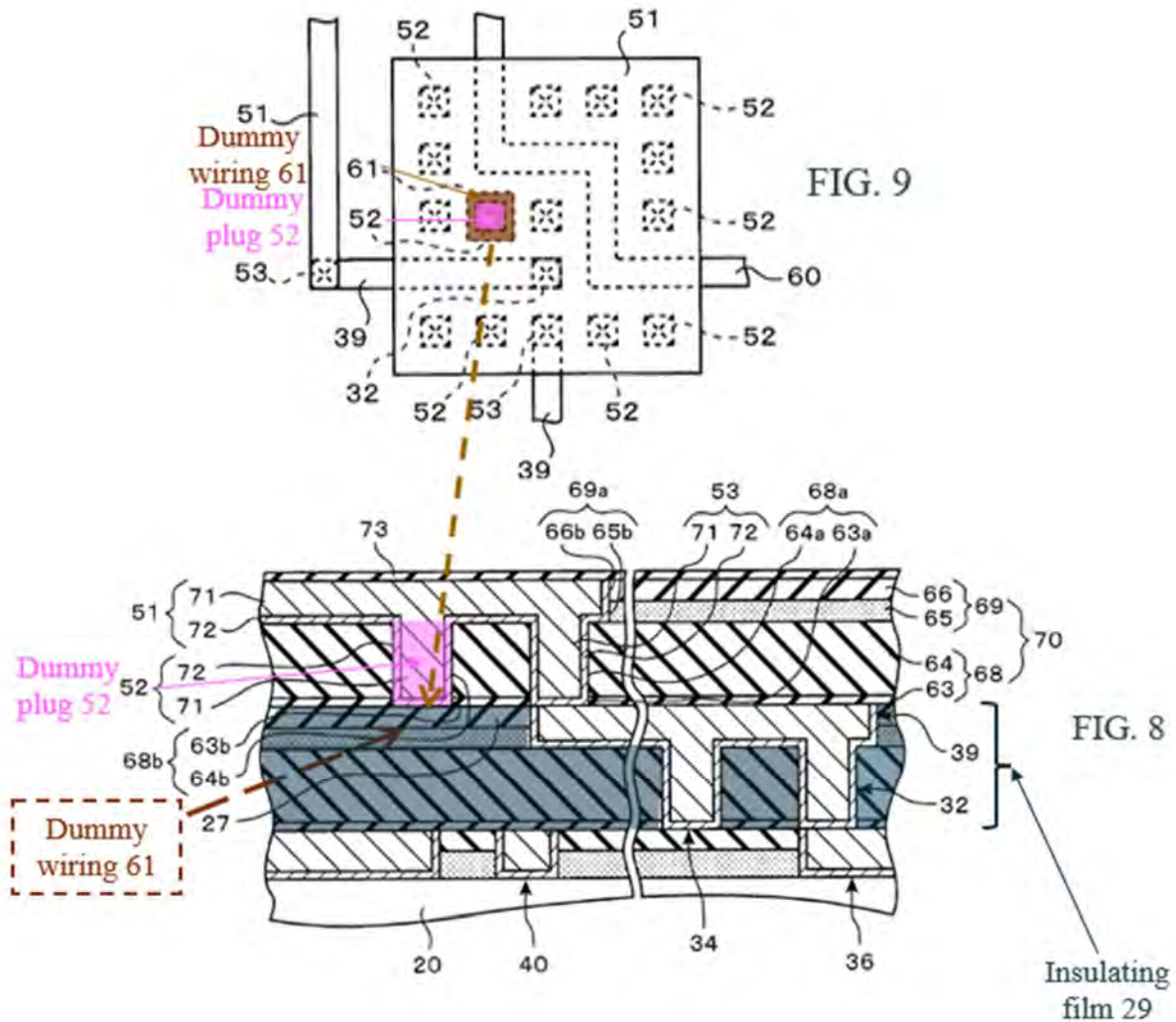
FIG. 3



160. A POSITA would understand that “dummy wiring 41” is a “dummy interconnect” both because of its description as a “dummy” and its structure, which is consistent with the ’623 patent’s description of a “dummy interconnect.” Specifically, a POSITA would recognize that dummy wiring 41 does not constitute part of a closed circuit during actual use of the device, i.e., no current flows therein during use, and Watanabe’s device would still be operable if dummy wiring 41 was omitted. As discussed previously, the purpose of Watanabe’s dummy wiring 41 is merely to add additional structural support/strength to the overall device, not to serve as active circuitry or otherwise conduct current flow. Indeed, Watanabe states that “as shown in FIG. 3, a dummy wiring 41 is provided *in the non-forming region* of

the first wiring 36,” further demonstrating to a POSITA that the dummy wiring cannot pass current. *See* TSMC-1004, ¶[0090] (emphasis added).

161. In the fifth embodiment, Figures 8-9 illustrate a dummy wiring 61 (which is the claimed “first dummy interconnect”) formed on the insulating film 29, as well as on lower insulating film 38 (comprising films 37 and 25 per §X.A.2.(a), *supra*), with either film 29 or 38 being the “second insulating film.” *Id.*, ¶[0127], Figs. 1, 3, 8, 9, 12, 14. In particular, dummy wiring 61 and wiring 39 are in the same layer and are on the same insulating film (e.g., insulating film 29). *Id.*, ¶[0127]; *supra*, X.A.1.(a).(5). Annotated Figures 8-9 disclose the approximate location of dummy wiring 61 when Figure 8 accounts for dummy wiring 61, demonstrating that dummy wiring 61 is on insulating film 29 (or insulating film 38 (not annotated)):

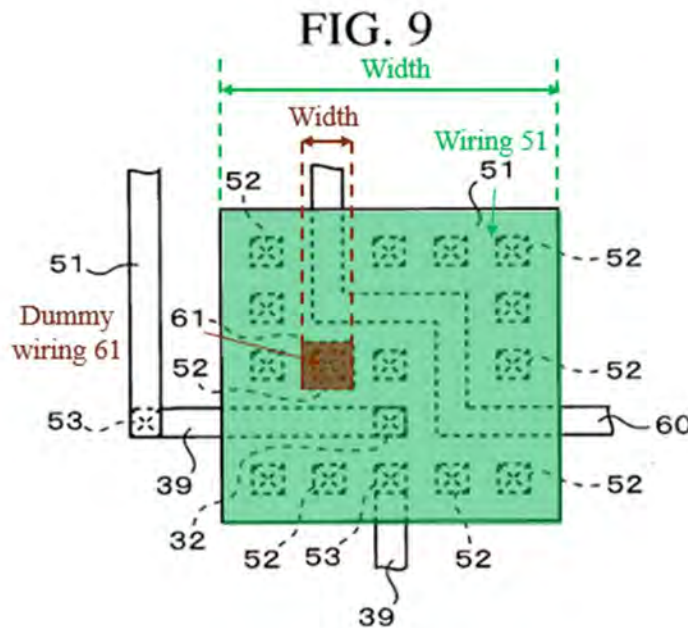


162. The dummy plug 52 (which is the claimed “dummy via”) is connected to the dummy wiring 61. TSMC-1004, ¶[0127]. Just like the “dummy wiring 41” and for the same reasons discussed above with respect to the second embodiment for this claim limitation, a POSITA would understand that “dummy wiring 61” is a “dummy interconnect.”

3. Claim 3 – “semiconductor device of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect”

163. Claim 3 recites the “semiconductor device of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect,” which at least Watanabe’s fifth embodiment discloses.

164. As described for claims 1 and 2, Watanabe’s fifth embodiment discloses a first dummy interconnect (e.g., “dummy wiring 61”) and a second interconnect (e.g., “wiring 51”). *Supra*, §§X.A.1.(d), X.A.2. In Watanabe’s fifth embodiment, the dummy wiring 61 (the “first dummy interconnect”) has a smaller width than wiring 51 (the “second interconnect”), as shown in the plan view in annotated Figure 9 below:



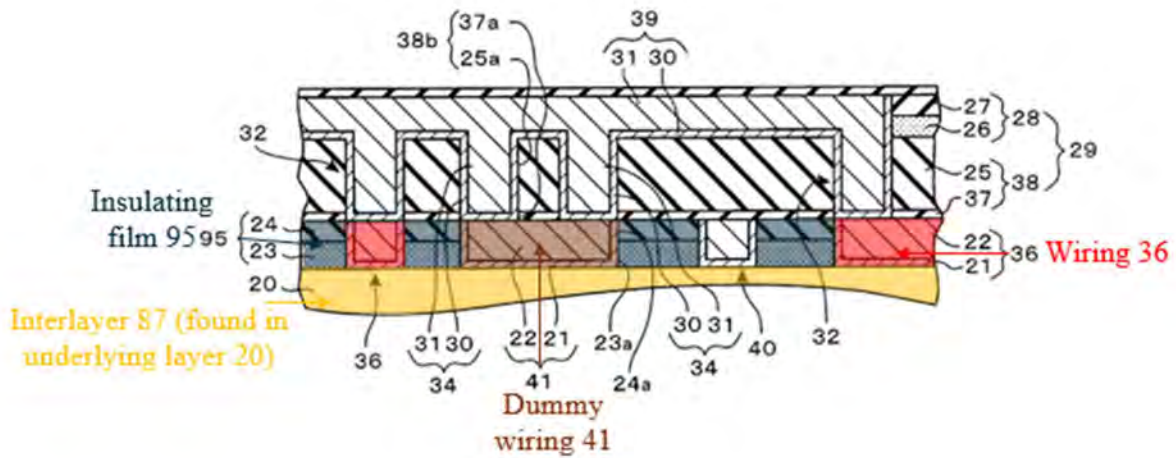
TSMC-1004, ¶¶[0116]-[0117], [0125]-[0127], Fig. 9.

4. Claim 7 – “semiconductor device of claim 2, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film”

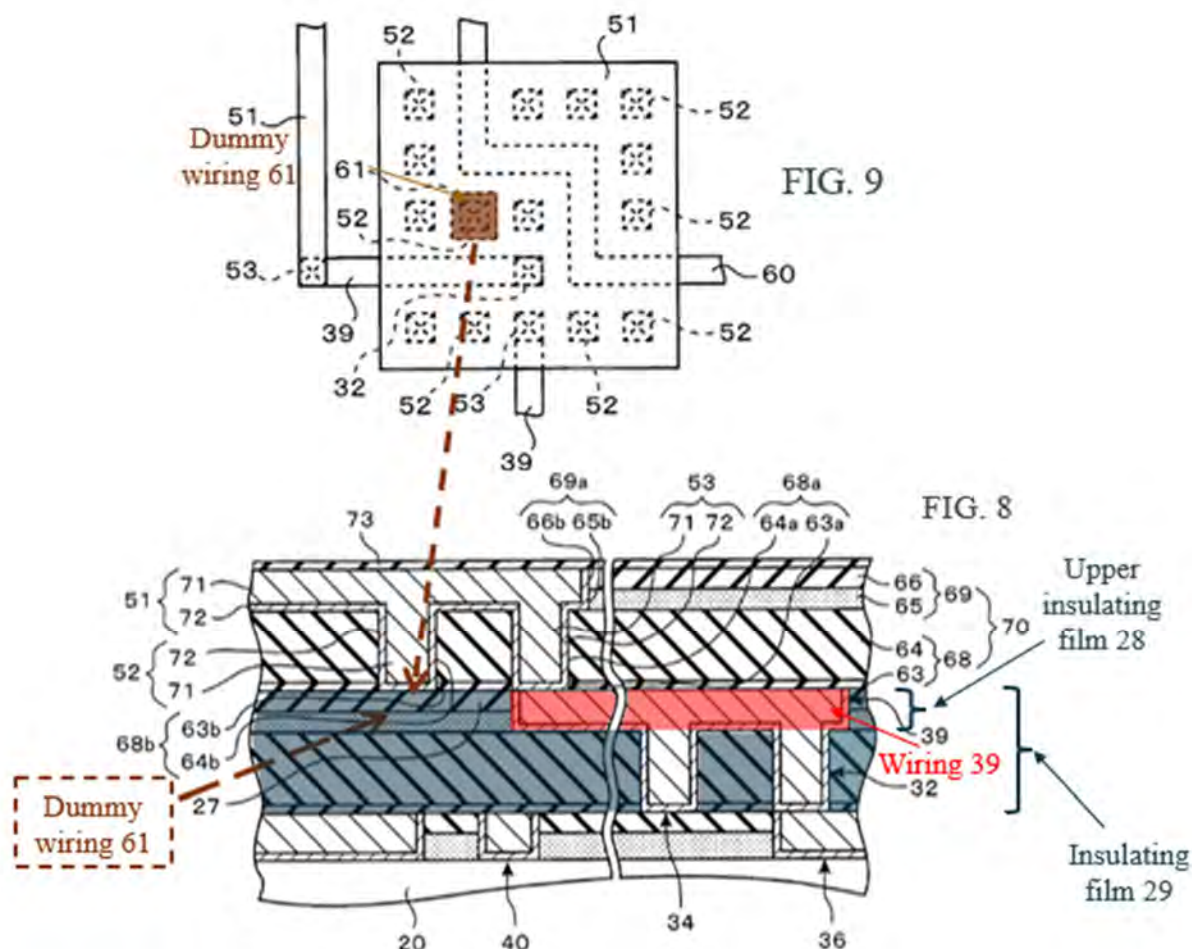
165. Claim 7 recites the “semiconductor device of claim 2, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film,” which at least each of Watanabe’s second and fifth embodiments discloses.

166. In Watanabe’s second embodiment in Figures 3-4 (and taking into account Fig. 14), the combined insulating film 95/interlayer insulating film 87 are together the “second insulating film.” The insulating film 95 is an upper portion of the “second insulating film.” The wiring 36 (the “first interconnect”) and the dummy wiring 41 (the “first dummy interconnect”) are buried in that upper portion (i.e. within the insulating film 95). TSMC-1004, ¶¶[0061]-[0065], [0089], [0172]-[0174], Figs. 3, 14. See annotated Figure 3 below:

FIG. 3



167. In Watanabe's fifth embodiment (Figures 8-9), the insulating film 29 is a "second insulating film." An upper portion of this "second insulating film" is upper insulating film 28 (comprising films 26 and 27, as seen in Watanabe's Figure 14, for example). The wiring 39 ("first interconnect") and dummy wiring 61 ("first dummy interconnect") are buried within upper insulating film 28, and are thus buried in an upper portion of the insulating film 29 (i.e., the "second insulating film"). *Id.*, ¶¶[0066]-[0070], [0116]-[0117], [0127], [0172]-[0175], Figs. 1, 8, 9, 14. This is shown in annotated Figures 8 and 9 of Watanabe:



168. Watanabe explains that the dummy wiring 61 is formed in the same layer as the wiring 39, and it is below the dummy plug 52 as shown in Figure 9, so the above annotated Figure 8 shows the approximate location for the dummy wiring 61 when this figure accounts for the dummy wiring 61. *Id.*, ¶[0127], Figs. 8, 9. The dummy wiring 61, found in the same layer as the wiring 39, would be located within the upper insulating film 28 (including films 26 and 27) of the insulating film 29 (“second insulating film”). *Id.*, ¶[0127], Figs. 1, 8, 9. Annotated Figures 8 and 9

above disclose the approximate location of dummy wiring 61, demonstrating that dummy wiring 61 is in upper insulating film 28.

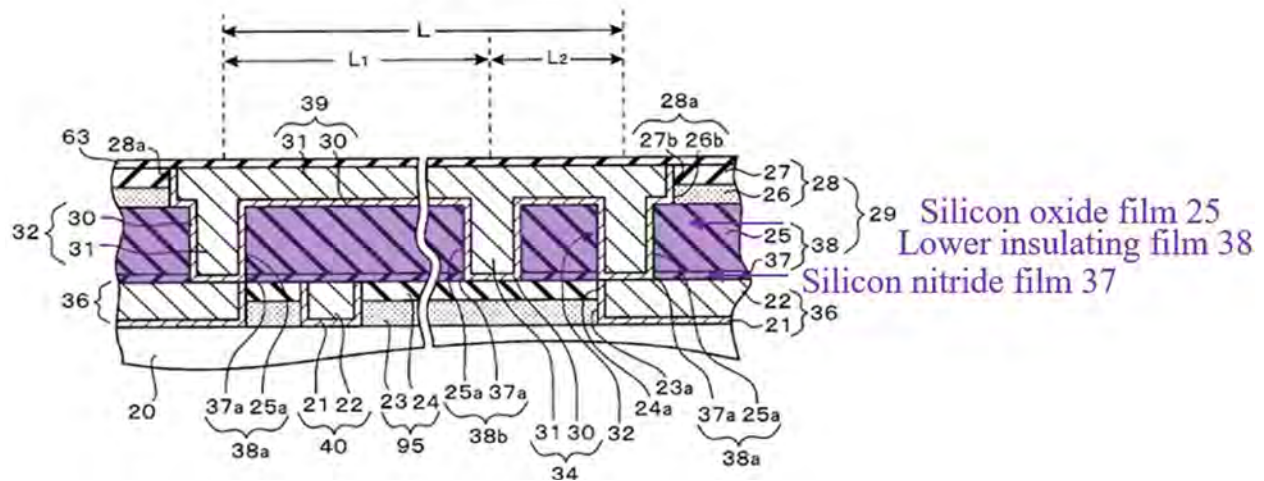
169. Watanabe explains that by having the dummy wiring 61 and connecting the dummy plug 52 to the dummy wiring 61, the mechanical strength of the laminated body is enhanced. *Id.*

5. Claim 11 - “semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film”

170. Claim 11 recites the “semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

171. The disclosure of claim 1 by Watanabe is established above. For the first to third embodiments, the “first insulating film” is the lower insulating film 38. Additionally, the “first insulating film” may be considered to be Watanabe’s “insulating film 29,” of which lower insulating film 38 is a sub-layer. The lower insulating film 38 includes multiple layers, including a silicon nitride film 37 (SiN film) and a silicon oxide film 25 (SiO₂ film). TSMC-1004, ¶¶[0066], [0089], [0094], Figs. 1, 3, 5A-5C, 12E, 12M; *see also id.*, ¶¶[0150], [0184]. See annotated Fig. 1 below:

FIG. 1



A POSITA would have understood that “SiN” refers to “silicon nitride.” A POSITA would also have understood that “SiO₂” encompasses “silicon oxide” because “silicon oxide” is a common term of art used in this field to refer to SiO₂ films, or at least films comprising predominantly SiO₂. For example, in another contemporaneous patent of his, Watanabe’976⁴, Watanabe expressly equates “silicon nitride” to “SiN” and “silicon oxide” to “SiO₂.” TSMC-1022, 2:48-49 (describing “a silicon nitride (SiN) film” and “a silicon oxide (SiO₂) film”).

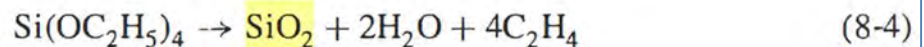
⁴ Watanabe’976 is directed to a semiconductor device and manufacturing method relating to the formation of vias/via holes to be formed through an insulating film on a wiring layer. TSMC-1022, 1:15-21. Because Watanabe’976 is in the same field (interconnection/wiring structures) and reasonably pertinent to a problem the ’623 patent purports to address (e.g., interconnect manufacture and reliability), Watanabe’976 is analogous art. TSMC-1001, 1:14-16, 2:39-42; TSMC-1022, Title, 1:15-21, 3:15-30, 9:33-39, 10:25-32, 12:25-32, Fig. 11.

Contemporaneous textbooks likewise show that the term “silicon oxide” was commonly used to refer to SiO₂:

Silicon oxide is also produced by chemical vapor deposition (CVD). In this method the silicon is supplied along with an oxygen-bearing compound, and the oxide is grown *on* the wafer rather than within the wafer, as in thermal oxidation. Various chemical systems have been used in oxide growth. Two examples are the dichlorosilane–nitrous oxide system



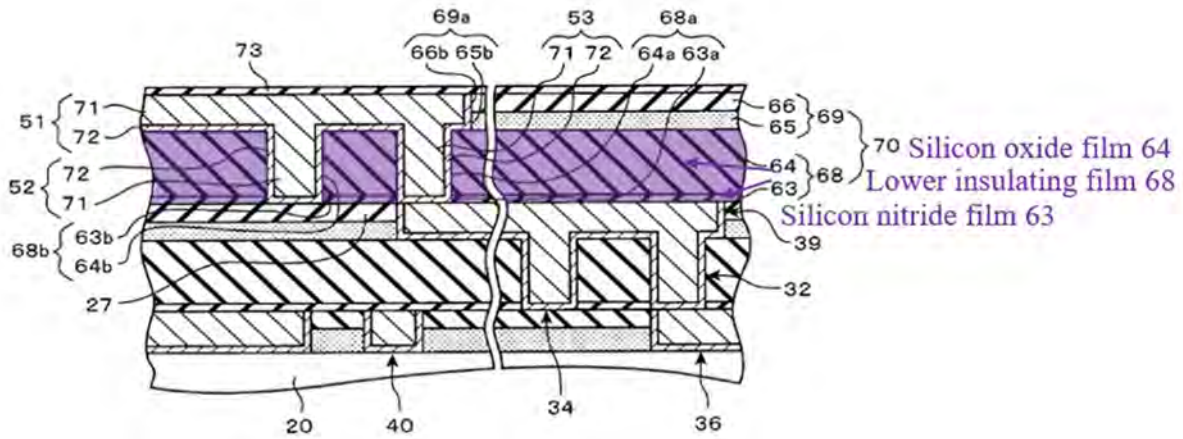
and the TEOS (tetraethylorthosilicate) system



TSMC-1023, 261. Thus, a POSITA would have understood Watanabe’s disclosures of silicon nitride and silicon oxide films as part of lower insulating film 38 to disclose the limitations of claim 11.

172. For the fifth embodiment, the “first insulating film” is the lower insulating film 68. Additionally, the “first insulating film” may be considered to be Watanabe’s “insulating film 70,” of which lower insulating film 68 is a sub-layer. The lower insulating film 68 is a multilayer structure including a silicon nitride film 63 and a silicon oxide film 64. *Id.*, ¶¶[0119], Fig. 8. See annotated Fig. 8 below:

FIG. 8



6. Claim 12 – “*semiconductor device of claim 1, wherein the second interconnect includes a first barrier film and a first conductive film*”

173. Claim 12 recites the “semiconductor device of claim 1, wherein the second interconnect includes a first barrier film and a first conductive film,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

174. The disclosure of claim 1 by Watanabe is established above. In its first-to-third embodiments, Watanabe discloses a second interconnect (wiring 39) having a double-layered structure with a first barrier film (e.g., barrier metal layer 30) and a first conductive film (e.g., copper film 31). TSMC-1004, ¶¶[0068]-[0069], [0089], [0094], [0166]-[0168], Figs. 1, 3, 5A-5C, 12L-12M. In Watanabe’s fifth embodiment, the second interconnect (wiring 51) likewise has a double-layered

structure with a first barrier film (e.g., barrier metal layer 72) and a first conductive film (e.g., copper film 71). *Id.*, ¶[0118], Fig. 8.

7. Claim 13 - “semiconductor device of claim 12, wherein the first conductive film includes copper”

175. Claim 13 recites the “semiconductor device of claim 12, wherein the first conductive film includes copper,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

176. The disclosure of claim 1 by Watanabe is established above. For the first to third embodiments, the “first conductive film” is the copper film 31, which plainly includes copper. TSMC-1004, ¶[0069], Figs. 1, 3.

177. For the fifth embodiment, the “first conductive film” is the copper film 71, which plainly includes copper. *Id.*, ¶[0118], Fig. 8.

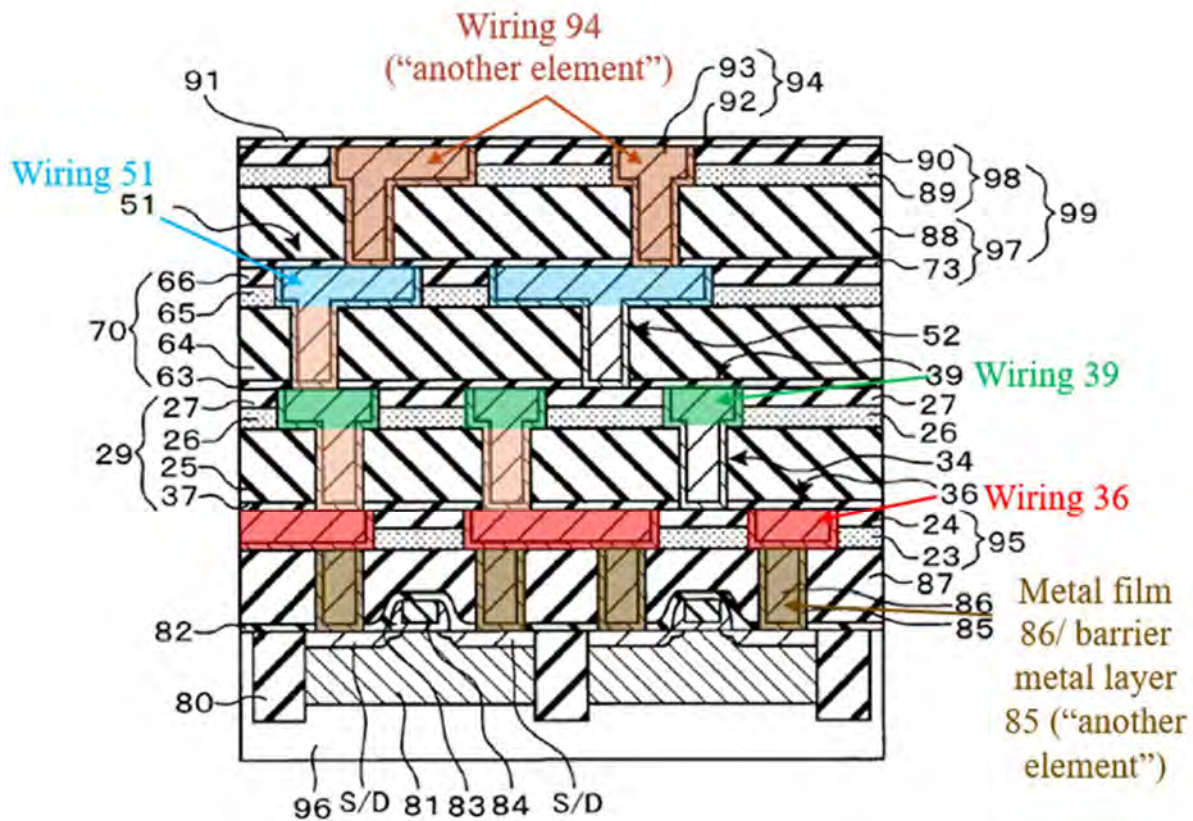
8. Claim 14 - “semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode”

178. Claim 14 recites the “semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

179. The disclosure of claim 1 by Watanabe is established above. For the first-to-third embodiments, the wiring 36 and wiring 39 correspond to the claimed “first interconnect” and “second interconnect,” respectively. For the fifth embodiment, the wiring 39 and wiring 51 correspond to the claimed “first interconnect” and “second interconnect,” respectively.

180. A POSITA would understand that each of Watanabe’s first and second interconnects (e.g., “wiring 36,” “wiring 39,” “wiring 51”) is connected to another element or an external electrode. Watanabe explains that, while a two-wiring structure (wiring 36 and wiring 39) is disclosed, any number of wiring layers can be laminated by repeating the same method (of Figures 12A-12M). TSMC-1004, ¶[0171]. Watanabe’s Figure 14 illustrates a structure having four layers of wirings (including wirings 36, 39, and 51), which are each connected to other elements. *Id.*, ¶¶[0051], [0172]-[0181], Fig. 14. For example, for the first to third embodiments, wiring 36 is connected to a metal film 86 and wiring 39 is connected to wiring 51 by a conductive plug (which a POSITA would understand to be conductive plugs 32/53). *Id.* For the fifth embodiment, wiring 39 is connected to wirings 36 and 51 by conductive plugs (e.g., conductive plugs 32/53), and wiring 51 is connected to wiring 94 by another conductive plug, each of which constitute “other elements.” *Id.* These connections are shown for example in annotated Figure 14 below:

FIG. 14



181. A POSITA would understand that each of the first to third and fifth embodiments provides a semiconductor device where wirings 36, 39, and 51 form a circuit to convey electrical signals/current to other elements. The specific components and connection/wiring configurations would depend on the design criteria/objectives for the device, which a POSITA would have readily and easily customized as required to meet such objectives.

182. Additionally, in describing its various embodiments, Watanabe states that the structures (like wiring 36, wiring 39, and wiring 51) are formed upon an underlying layer 20. *Id.*, ¶[0061], Figs. 1, 3, 8. Watanabe explains that the

underlying layer can include a MOSFET formed on a semiconductor substrate and conductive plugs through an insulating film. *Id.*, ¶¶[0089], [0094], [0116], [0173]. While Figures 1, 3, and 8 disclose this underlying layer 20 generically, Watanabe later shows the detailed composition of the underlying layer 20 in Figure 14 when discussing the broader applicability of its manufacturing method and resulting structures. *Id.*, ¶[0173].

183. Specifically, Watanabe states that the underlying layer 20 in each of the embodiments include the semiconductor transistor components shown in Figure 14, such as gate electrodes 84, source/drain regions S/D on a silicon substrate 96, and conductive plugs (comprising barrier metal layer 85 and metal film 86) connecting to these active device components. *Id.*, ¶¶[0061], [0089], [0094], [0016], [0173]-[0178]. These transistor components expressly shown in Figure 14 are representative of example circuit connections for all the embodiments discussed, including the first, second, third, and fifth embodiments. Thus, while Figures 1, 3, and 8 disclose this underlying layer 20 generically, Watanabe later shows the detailed composition of the underlying layer 20 in Figure 14 when discussing the broader applicability of its manufacturing method and resulting structures. *Id.*, ¶[0173].

184. Thus, for embodiments like the first, second, and third, Watanabe's wiring 36 is formed on this underlying layer 20 and connects to its elements, such

as the metal film 86 of the conductive plugs that connect to the S/D regions for the gate electrodes 84. *Id.*, ¶[0173]-[0174], Fig. 14. The wiring 39 is formed above and connected to the wiring 36 via conductive plug 32. *Id.*, Figs. 1, 3, 8, 14. Watanabe further discloses that any number of wiring layers can be stacked, and Figure 14 discloses a multi-level structure where the wiring 36 is connected to underlying device elements, and the wiring 39 is connected to the wiring 36 and can be connected to further elements like a wiring 51. *Id.*, ¶[0173]-[0178], Fig. 14.

185. Thus, the wiring 39 is connected downwards to the wiring 36 via conductive plug 32; the wiring 36, in turn, connects to the underlying active members in underlying layer 20 as described above; and the wiring 51 is connected downwards to the wiring 39 via conductive plug 53. *Id.* These connections demonstrate that each of these interconnects is connected to another element (another wiring layer or underlying device members). In addition, a POSITA would understand that, in a semiconductor device, it is necessary that the functional wiring layers ultimately must be connected to other circuit elements or to external electrodes for the device to operate. *Id.*, ¶[0006], [0073].

186. Therefore, in the first-to-third and fifth embodiments, each of the first and second interconnects (e.g., wiring 36, wiring 39, wiring 51) are connected to another element or an external electrode. Figure 14 illustrates a structure with four

layers of wirings, which incorporates wiring 36, 39, and 51, each connected to other elements. *See id.*, ¶¶[0051], [0172]-[0181], Fig. 14.

9. Claim 15

187. At least each of Watanabe’s first-to-third and fifth embodiments meet claim 15.

a) [15.a] – “*semiconductor device of claim 1, wherein the first interconnect, the second interconnect and the via constitute part of a closed circuit*”

188. Element [15.a] recites the “semiconductor device of claim 1, wherein the first interconnect, the second interconnect and the via constitute part of a closed circuit,” which Watanabe discloses.

189. The disclosure of claim 1 by Watanabe is established above. In Watanabe’s first, second, and third embodiments, the wiring 36 (“first interconnect”), the wiring 39 (“second interconnect”), and the conductive plug 32 (“via”) form a functional electrical path. TSMC-1004, ¶[0073], Figs. 1, 3, 5A-5C. Indeed, Watanabe explicitly states that the conductive plug 32 is electrically connected to the wiring 36 and functions to connect the wiring 36 to the wiring 39 electrically. *Id.* As established in the above analysis for claim 14, these interconnects are connected to other active elements and, therefore, the path formed

by the wiring 36, conductive plug 32, and wiring 39 constitutes part of a closed electrical circuit essential for device operation. *Id.*, ¶[0173], Figs. 1, 3, 14.

190. In Watanabe’s fifth embodiment, the wiring 39 (“first interconnect”), the wiring 51 (“second interconnect”), and the conductive plug 53 (“via”) similarly form a functional electrical path. *Id.*, ¶[0122], Fig. 8. The wiring 39, in turn, connects to the wiring 36 and ultimately to underlying active device components as explained in the analysis for claim 14. *Id.*, ¶[0173], Figs. 8, 14. This configuration forms part of a closed circuit.

191. Therefore, Watanabe discloses that the first interconnect, second interconnect, and the via constitute part of a closed circuit. For the first-to-third embodiments, wiring 36, wiring 39, and the conductive plug 32 form a functional electrical path. *Id.*, ¶[0073], Figs. 1, 3, 8. In Watanabe’s fifth embodiment, the wiring 39, the wiring 51, and the conductive plug 53 similarly form a functional electrical path. *Id.*, ¶[0122], Figs. 8, 14.

b) [15.b] – “*the dummy via does not constitute a closed circuit*”

192. Element [15.b] calls for “the dummy via does not constitute a closed circuit,” which Watanabe discloses.

193. In Watanabe’s first embodiment, the dummy plug 34 (“dummy via”) extends from the wiring 39 to a “non-forming region of the first wiring 36.” TSMC-

1004, ¶[0067], Fig. 1. The dummy plug 34 connects to the wiring 39 at its upper end but its lower end terminates at an insulating region (insulating film 95) without connecting to an active conductive element that would constitute a closed circuit. *Id.*, ¶[0067], [0079], Fig. 1. Watanabe explicitly states that the purpose of the dummy plug 34 is to suppress stress migration (*see id.*, [0074]-[0079]); it is not for forming an electrical connection for device operation. *See supra*, §X.A.1.(a).(8).

194. In Watanabe's second embodiment, some dummy plugs 34 connect to an isolated dummy wiring 41 at their lower end. TSMC-1004, ¶[0090], Figs. 3, 4. This dummy wiring 41 is itself described as being in the non-forming region of the wiring 36 and is not shown to connect to any other active circuit elements. *Id.* Therefore, in this configuration, the dummy plug 34 (and the associated dummy wiring 41) does not constitute part of a closed circuit for device operation.

195. In Watanabe's fifth embodiment, the dummy plug 52 ("dummy via") connects from the wiring 51 to "the non-forming region of the second wiring 39" or to an isolated dummy wiring 61. *Id.*, ¶[0121]-[0122], [0127], Figs. 8, 9. In either case, the dummy plug 52 does not complete a path for current flow in an active circuit.

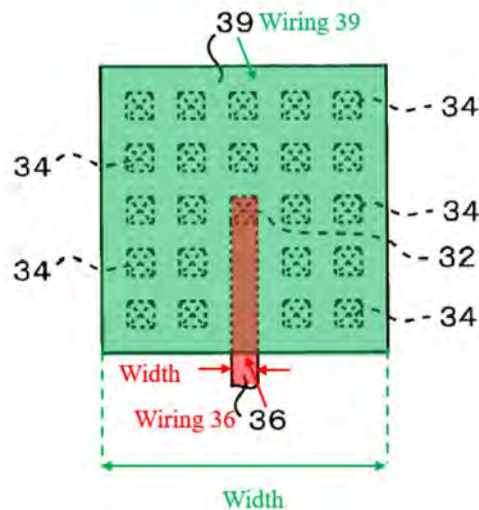
196. Therefore, Watanabe discloses that the dummy vias ("dummy conductive plugs 34" or "dummy conductive plugs 52") do not constitute a closed circuit.

10. Claim 16 – “semiconductor device of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect”

197. Claim 16 calls for “semiconductor device of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect,” which at least each of Watanabe’s third and fifth embodiments discloses.

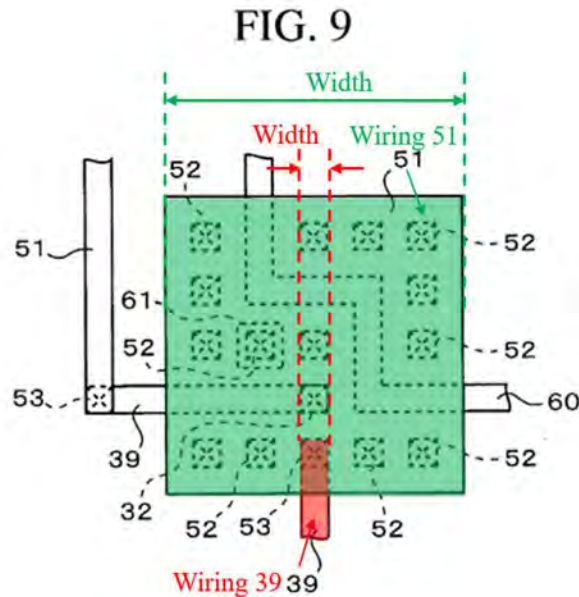
198. Annotated Figure 5A (third embodiment) discloses the first interconnect (e.g., “wiring 36”) as having a width smaller than that of the second interconnect (e.g., “wiring 39”). TSMC-1004, ¶¶[0094]-[0095], Figs. 5A-5C.

FIG. 5A



199. In the third embodiment, “wiring 39” may have a wider planar shape as opposed to the generally “linear shape” of the first and second embodiments. *See also id.*, ¶¶[0042], [0049], [0094].

200. Similarly, the first interconnect (e.g., “wiring 39”) of Watanabe’s fifth embodiment has a width smaller than that of the second interconnect (e.g., “wiring 51”) as disclosed in annotated Figure 9 below (*id.*, ¶¶[0125], Fig. 9):



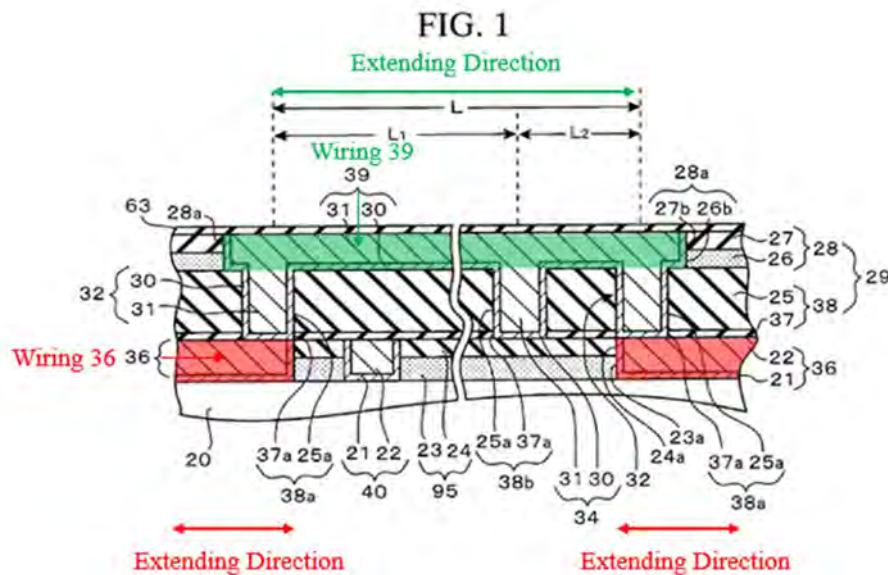
201. Like the third embodiment, the fifth embodiment similarly describes a narrower, linear first interconnect on a layer below a wider, planar second interconnect. *Id.*, ¶¶[0124]-[0125]. Thus, each of at least the third and fifth embodiments of Watanabe satisfies claim 16.

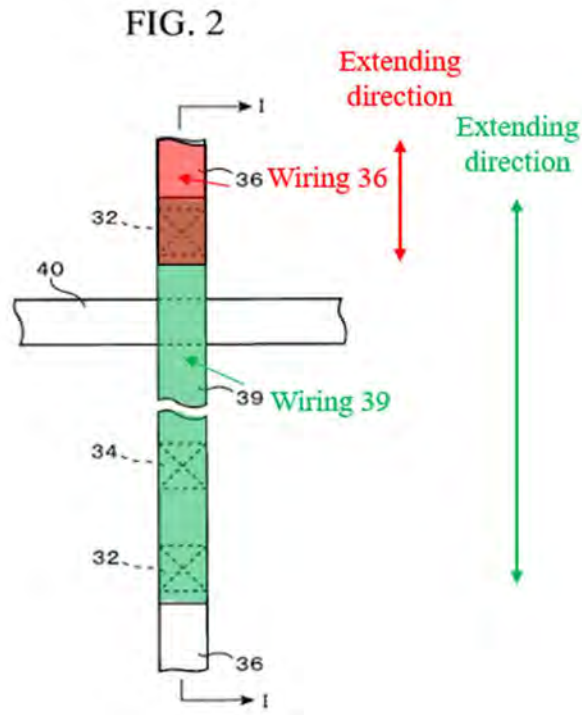
11. Claim 21 – “semiconductor device of claim 1, wherein the first interconnect and the second interconnect extend in a same direction”

202. Claim 21 recites the “semiconductor device of claim 1, wherein the first interconnect and the second interconnect extend in a same direction,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

203. The disclosure of claim 1 by Watanabe is established above. In Watanabe's first, second, and third embodiments, the wiring 36 ("first interconnect") and the wiring 39 ("second interconnect") are disclosed extending in the same direction.

204. As shown for example in each of annotated Figures 1 and 2 below, Watanabe discloses that the first interconnect (e.g., "first wiring 36") and the second interconnect (e.g., "second wiring 39") extend in a same direction (e.g., along the "L" direction in Fig. 1). TSMC-1004, Figs. 1-4, ¶[0095]. For example, the cross-sectional views in Figures 1 and 3 (as well as 8) show both first wiring 36 and second wiring 39 as parallel interconnects extending across the page (i.e., the "same direction" "L"), as confirmed in the corresponding plan views in Figures 2 and 4. Annotated Figures 1 and 2 below show the show wirings 36 and 39 extending in the same direction:





205. Figure 5A also shows first wiring 36 and second wiring 39 extending in the same direction (*id.*, Figs. 5A-5C, ¶¶[0095], [0111]), as does Figure 9 for wirings 39 and 51, as shown in the annotated figures below:

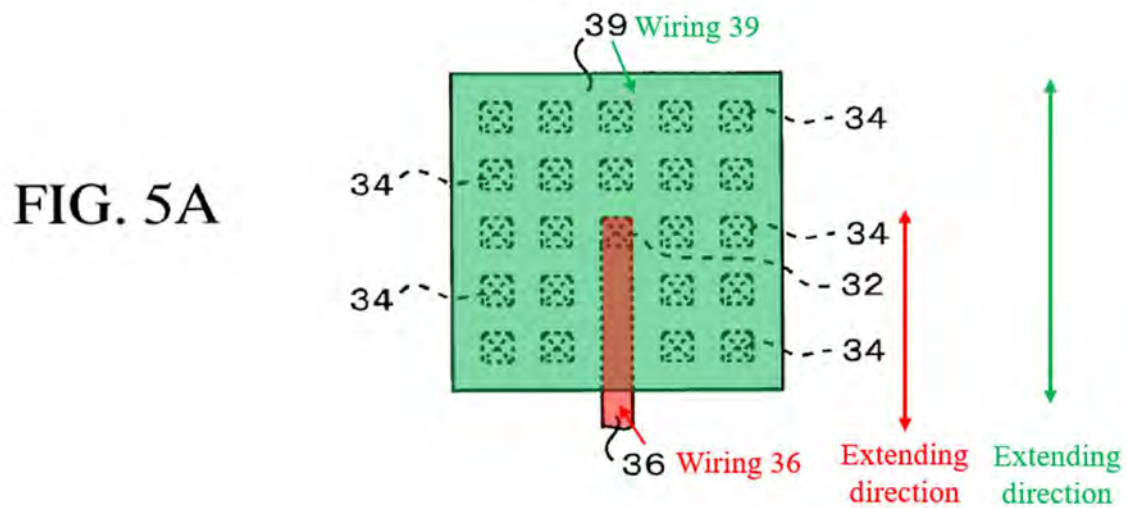
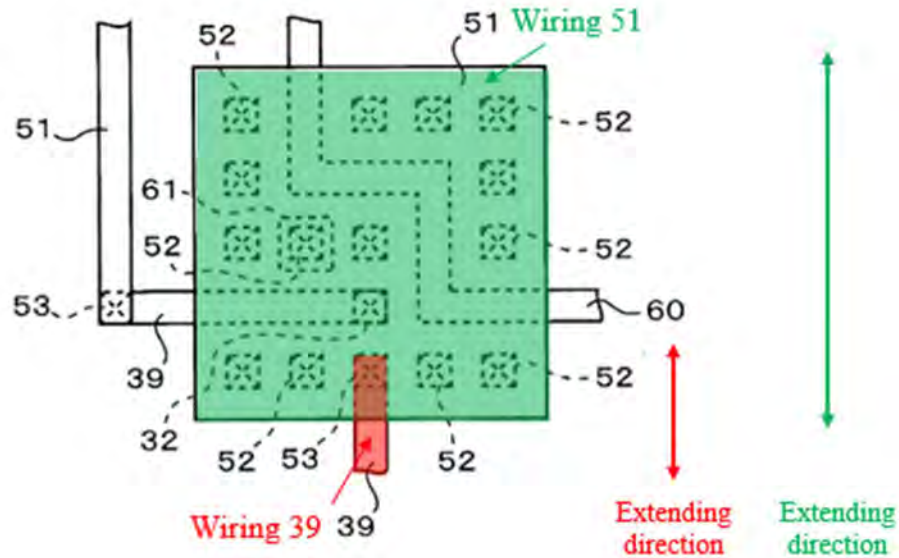


FIG. 9



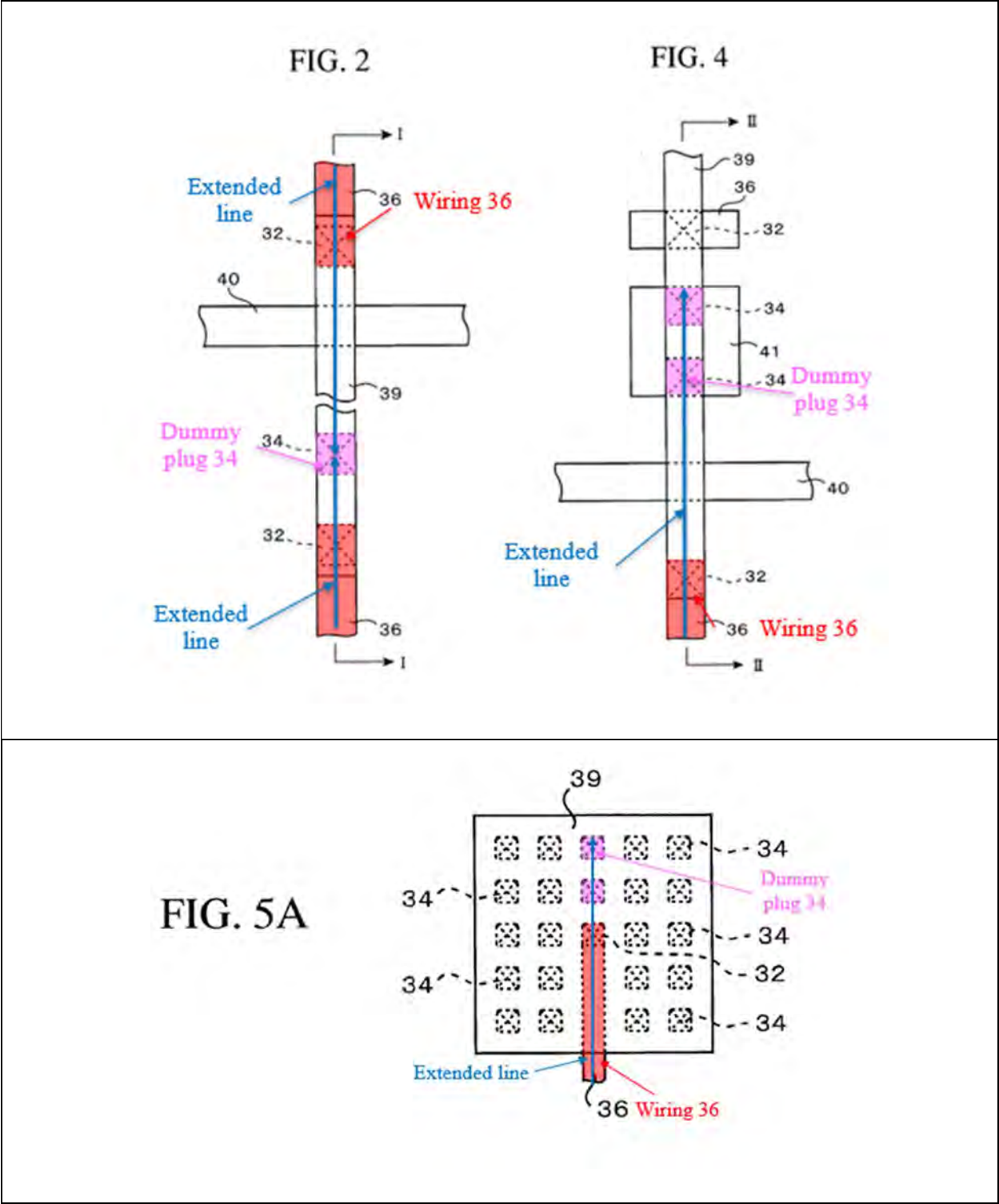
12. Claim 22 – “*semiconductor device of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends*”

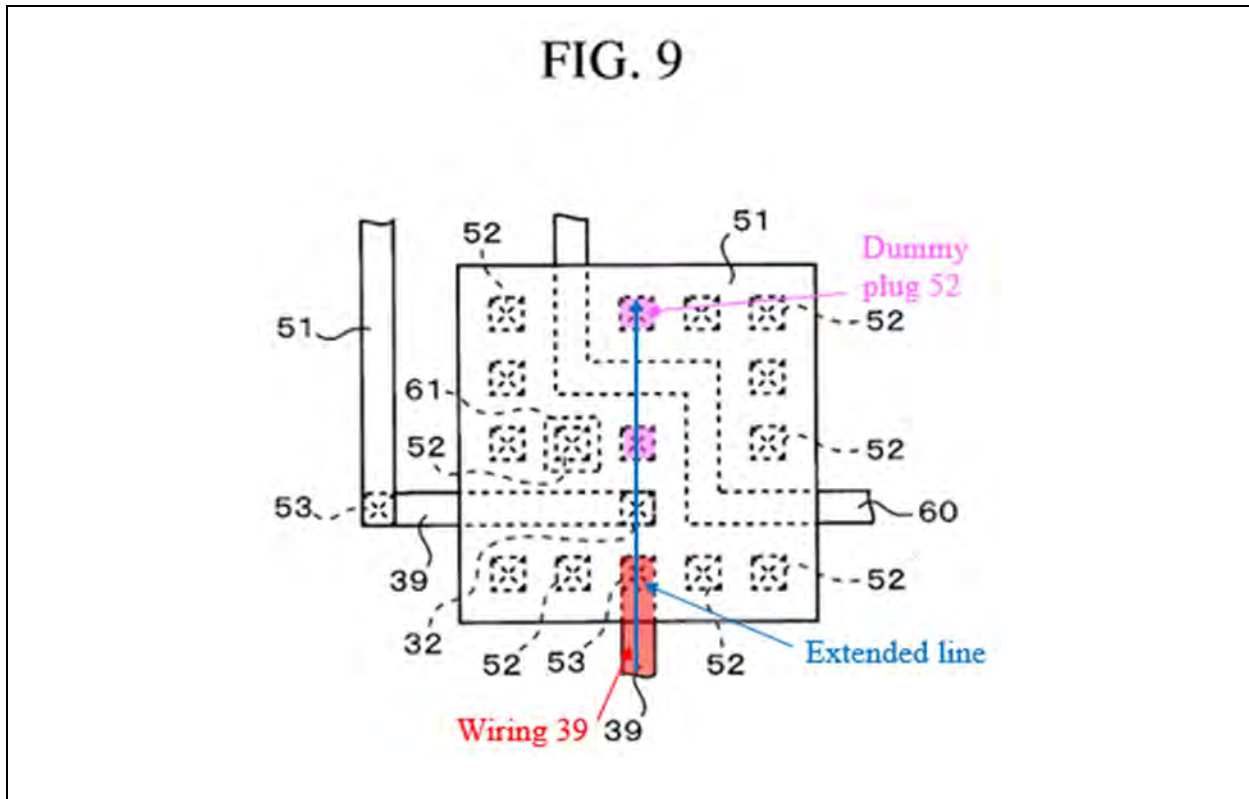
206. Claim 22 recites the “semiconductor device of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

207. The disclosure of claim 1 by Watanabe is established above. Watanabe's plan view figures show the dummy plug 34, 52 ("dummy via" in each instance) positioned along an extended line along which the wiring 36, wiring 39

(i.e., the claimed “first interconnect” in each instance) extends. TSMC-1004, Figs. 2, 4, 5A-5C, 9. For instance, Figure 2 of Watanabe illustrates the dummy plug 34 is provided on an extended line along which the wiring 36 extends. *Id.*, Fig. 2. Similarly, Figure 4 of Watanabe shows dummy plugs 34 provided on an extended line along which the wiring 36 extends. *Id.*, Fig. 4. Figure 9 of Watanabe shows dummy plugs 52 provided on an extended line along which the wiring 39 extends. *Id.*, Fig. 9.

208. Therefore, for each of Watanabe’s first-to-third and fifth embodiments, at least one dummy via (e.g., dummy plug 34) is provided on an extended line along which the first interconnect (e.g., wiring 36) extends, as shown in annotated Figures 2, 4, 5A, and 9:





13. Claim 25 – “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less”

209. Claim 25 recites the “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less,” which at least each of first-to-third and fifth embodiments discloses.

210. The '623 patent refers to the “space” between a via and dummy via as corresponding to the distance from an edge of the via and a closest edge of an adjacent dummy via. TSMC-1001, 4:18-22. Watanabe expressly discusses and analyzes the distances between the conductive plug 32 (“via”) and the dummy plug 34 (“dummy via”). TSMC-1004, ¶¶[0081], [0086]-[0087], [0100]-[0105], Figs.

15A-17C. Specifically, Watanabe discloses that the via (e.g., plug 32) and the dummy via (e.g., dummy plug 34) are spaced at a distance of 25 μm or less (e.g., 0.3 μm). *Id.*, ¶[0105] (“the interval between the neighboring plugs (including the plug 32 and the dummy plug 34) was fixed to 0.3 μm .”), Figs. 15A-17C.

211. Watanabe provides an example where the interval between the neighboring plugs (including the plug 32 and the dummy plug 34) was fixed to 0.3 μm for simulations involving the models shown in Figures 17B-17C. *Id.*, ¶[0105], Figs. 17B-17C. This interval/pitch “ p_2 ” is disclosed in the annotated Figures 16B and 17B below:

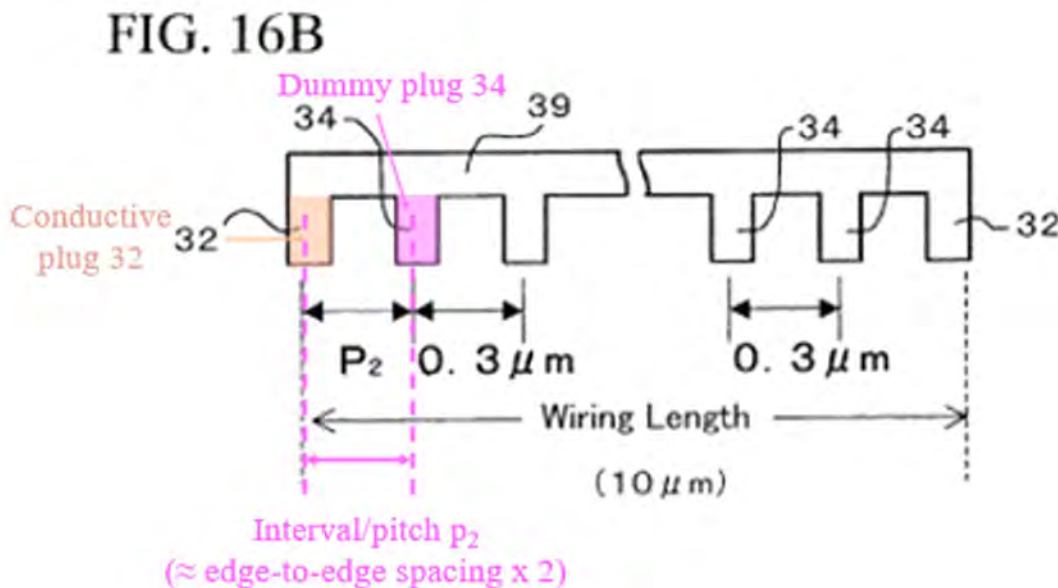
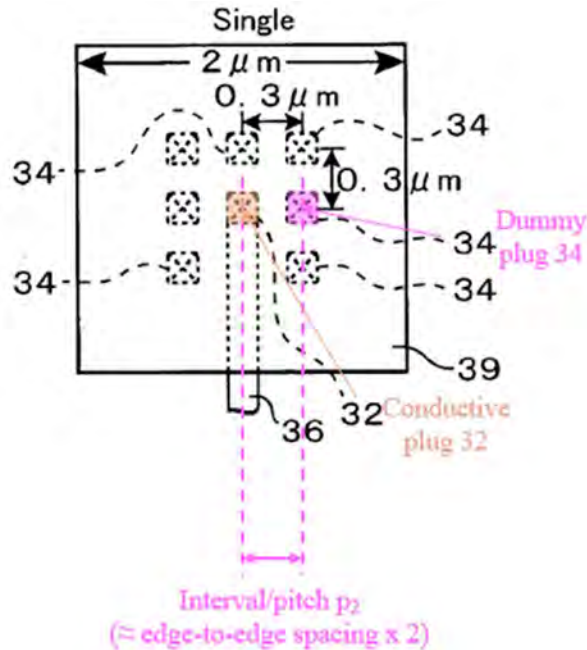


FIG. 17B



212. As shown in annotated Figure 16B above, the interval/pitch “ p_2 ” in Watanabe is the interval from a center of a via to a center of an adjacent dummy via, so the spacing from an edge of the via to an edge of the adjacent dummy plug is necessarily less than the interval/pitch p_2 —in Watanabe’s case, the edge-to-edge spacing is approximately half the pitch interval. So as an example, the spacing distance between the right side of the conductive plug 32 annotated above in Figures 16B and 17B and the left side of the nearest dummy plug 34 is less than the interval or pitch between those same plugs. Thus, because this $0.3\ \mu\text{m}$ interval/pitch between plugs 32 and 34 satisfies the $25\ \mu\text{m}$ or less requirement of claim 13, the edge-to-edge spacing between the same plugs necessarily satisfies this requirement as well.

213. Indeed, Watanabe explicitly discusses and analyzes the spacing between the conductive plug 32 (“via”) and the dummy conductive plug 34

(“dummy via”). *Id.*, ¶¶[0032]-[0033], [0053], [0086]-[0087], [0100]-[0105], [0190]-[0191], [0193], Figs. 16A, 17B, 17C. In the simulation results shown in Figure 16A, Watanabe investigates the effect of varying the pitch p_2 (an interval between the conductive plug 32 and the adjacently arranged dummy conductive plug 34) on stress migration. *Id.*, ¶¶[0086]-[0087], Fig. 16A. All data points evaluated in Figure 16A entail a pitch p_2 of 1.0 μm or less. *Id.* Watanabe concludes that in order to prevent the stress-migration, it is preferable that the first pitch p_2 is less than 1 μm , and more preferably less than 0.6 μm . *Id.*, ¶[0087]. A spacing of less than 1 μm or 0.6 μm satisfies the condition of being 25 μm or less.

214. A POSITA would have interpreted these teachings from Figures 16 and 17 as applying to the arrangements in Watanabe’s first-to-third and fifth embodiments, as disclosed in Figures 1-5 and 8-9.

14. Claim 26 – “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 1 μm or less”

215. Claim 26 recites the “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 1 μm or less,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

216. The disclosure of claim 1 by Watanabe is established above. The same discussion as outlined for claim 25 above applies to claim 26. As discussed, Watanabe concludes that in order to prevent the stress-migration, it is preferable that

the first pitch p_2 is less than 1 μm and more preferably less than 0.6 μm . TSMC-1004, ¶¶[0032]-[0033], [0053], [0086]-[0087], [0190]-[0191], [0193], Fig. 16A. As discussed for claim 25, the spacing between the via and dummy via is necessarily less than (approximately half of) the interval/pitch, so Watanabe discloses the claimed spacing of 1 μm or less. These teachings apply to the first-to-third and fifth embodiments.

217. Therefore, Watanabe discloses a via-to-dummy-via spacing of 1 μm or less, disclosing a spacing of less than 1.0 μm , less than 0.6 μm , and 0.3 μm .

15. Claim 28 – “*semiconductor device of claim 1, wherein the dummy via is provided in plural*”

218. Claim 28 recites the “semiconductor device of claim 1, wherein the dummy via is provided in plural,” which at least each of Watanabe’s second, third, and fifth embodiments discloses.

219. The disclosure of claim 1 by Watanabe is established above. Watanabe explicitly shows multiple dummy plugs 34 (“dummy via”) in several of its embodiments and figures. TSMC-1004, Figs. 4, 5A-5C. For example, Figures 3 and 4, showing the second embodiment, illustrate a plurality of dummy plugs 34. *Id.*, ¶[0090], Figs. 3, 4. Watanabe’s third embodiment, shown in Figures 5A-5C, is specifically focused on various arrangements of a plurality of dummy plugs 34 around a conductive plug 32. *Id.*, ¶¶[0096]-[0098], Figs. 5A-5C. The simulation

model in Figure 16B explicitly shows multiple dummy plugs 34 on one side of the conductive plug 32. *Id.*, Fig. 16B. In Watanabe's fifth embodiment, where dummy plug 52 is the claimed "dummy via," Figure 9 shows multiple dummy plugs 52 connected to the wiring 51. *Id.*, Fig. 9.

220. Therefore, Watanabe discloses plural dummy vias (dummy plugs 34 and 53), such as illustrated Figures 3-5 and 8-9. The same is true for the simulation models in Figures 15-17 (see dummy plugs 34). *Id.*, ¶¶[0108], [0114].

16. Claim 32 – “semiconductor device of claim 1, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect and shorter than a distance between the via and the other end of the second interconnect”

221. Claim 32 recites the “semiconductor device of claim 1, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect and shorter than a distance between the via and the other end of the second interconnect,” which at least each of Watanabe's first-to-third and fifth embodiments discloses.

222. The disclosure of claim 1 by Watanabe is established above. Watanabe discloses in Figures 2, 4, 5B, and 9 that a distance (“D1”) between the via (conductive plugs 32 or 53) and one end of the second interconnect (wiring 39 or

51) is shorter than a distance (“D2”) between the dummy via (dummy plug 34 or 52) and the one end of the second interconnect, and shorter than a distance (“D3”) between the via and the other end of the second interconnect. Note, for defining the distances D1, D2, and D3, I have used the via/dummy via edge that is closest to the end of the interconnect in question; one could map these distances to the centerline of each via/dummy via, and the outcome of my analysis would not change.

223. Watanabe’s plan view figures disclose this asymmetric placement of the conductive plug 32 (“via”) relative to the dummy plug 34 (“dummy via”) and the ends of the wiring 39 (“second interconnect”). TSMC-1004, Figs. 2, 5B, 5C. For example, Figure 2 of Watanabe shows that a conductive plug 32 is positioned closer to one end of the wiring 39 than an adjacent dummy plug 34 is to that same end, and the conductive plug 32 is also closer to that one end than to the opposite end of the wiring 39. *Id.*

224. An asymmetric placement is also clearly illustrated in Watanabe’s third embodiment. *Id.*, Figs. 5B-5C. Figure 5B of Watanabe shows the conductive plug 32 provided at one edge portion of the solid wiring 39, with many dummy plugs 34 located further from that edge, one of which is highlighted in an annotated version of Figure 5B. *Id.*, Fig. 5B. In this configuration, the distance from the conductive plug 32 to the proximate end (edge) of the wiring 39 is shorter than the distance from the dummy plug 34 to that same end. *Id.* Furthermore, this distance from the

conductive plug 32 to the proximate end is also shorter than the distance from the conductive plug 32 to the opposite end of the wiring 39. *Id.* A similar relationship is shown in Fig. 5B. *Id.*, Fig. 5B.

225. Therefore, as exemplified in annotated Figures 2, 5B, and 9, Watanabe discloses that a distance between the via (conductive plug 32 or 53) and one end of the second interconnect (wiring 39 or 51) (“D1” below) is shorter than a distance between the dummy via (dummy plug 34 or 52) and the one end of the second interconnect (“D2” below), and shorter than a distance between the via and the other end of the second interconnect (“D3” below):

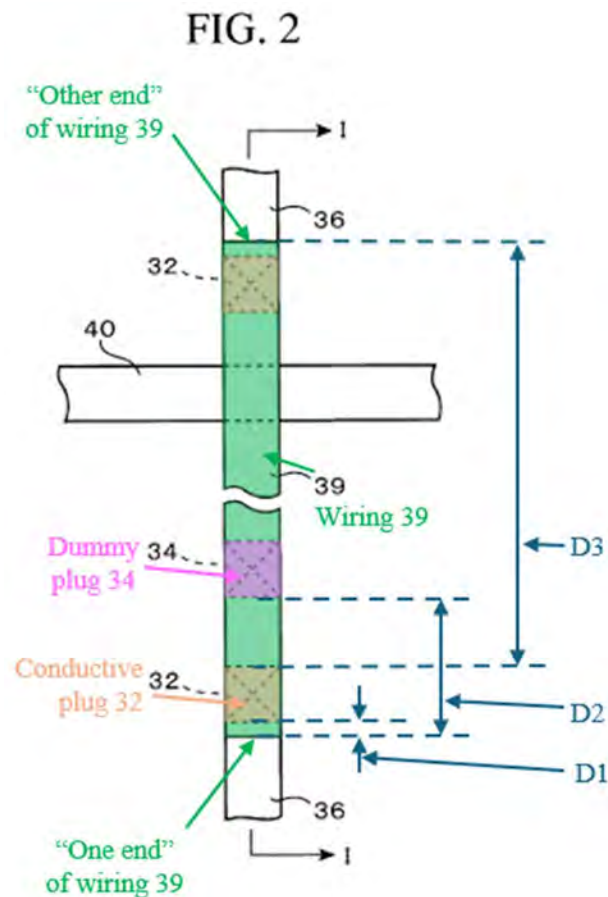


FIG. 5B

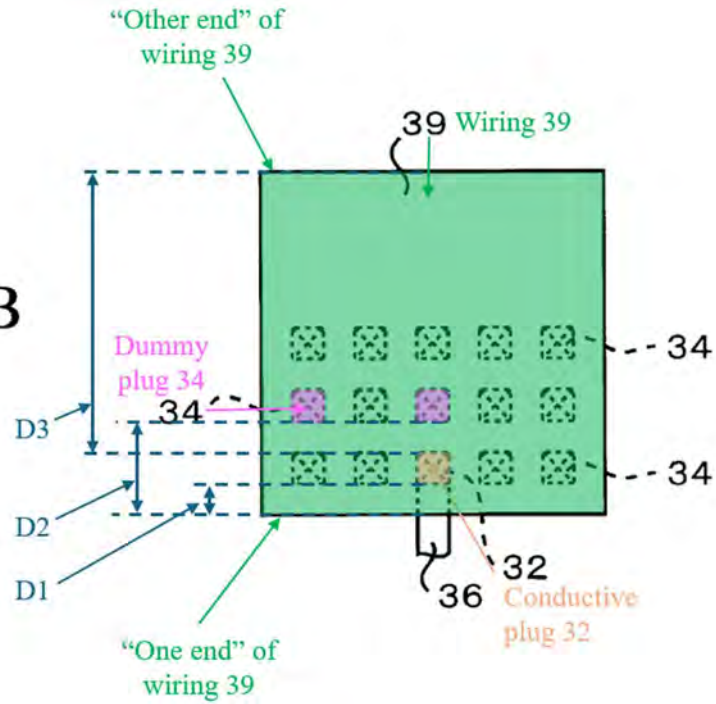
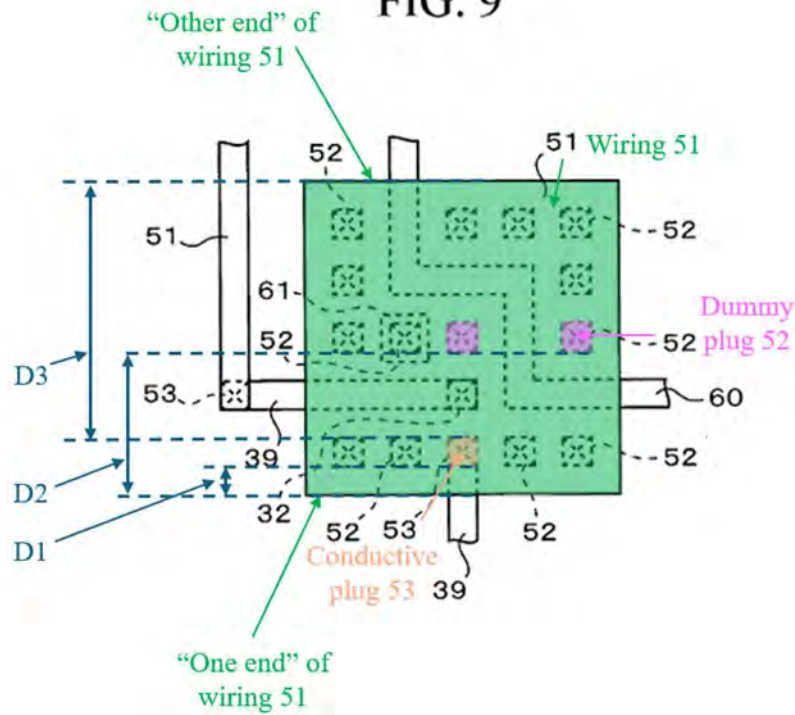


FIG. 9



226. Thus, Watanabe discloses conductive plug 32/plug 53 positioned closer to one end of wiring 39/wiring 51 than an adjacent dummy plug 34/dummy plug 53, and conductive plug 32/plug 53 is closer to that end than opposite end of the wiring 39/wiring 51. *Id.*

17. Claim 39 – “semiconductor device of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film”

227. Claim 39 recites the “semiconductor device of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

228. Watanabe discloses claim 1, including the dual damascene formation.

229. Watanabe’s dummy via (e.g., “dummy plugs 34” in the first through third embodiments and “dummy plugs 52” in the fifth embodiment) and the second interconnect (e.g., “wiring 39” in the first through third embodiments; “wiring 51” in the fifth embodiment) are made of the same conductive film (e.g., “copper film 31,” “barrier metal layer 30”). TSMC-1004, ¶¶[0067]-[0070], [0072], [0166]-[0168], Figs. 12L-12M.

230. The dummy via and the second interconnect being made of the same conductive film is a result of the dual damascene process disclosed by Watanabe. *Id.*, ¶¶[0072], [0135]; Figs. 1, 3, 12J-M. The same conductive film (copper film 31)

simultaneously fills the trench for the second interconnect 39 and the hole for the dummy via 34. *Id.* Watanabe states the dummy plug is a portion of the second wiring. *Id.*, ¶[0070].

231. Watanabe discloses that the dummy via (e.g., dummy plug 34) and the second interconnect (e.g., wiring 39) are made of the same conductive film (e.g., “copper film 31,” “barrier metal layer 30”). *Id.*, ¶[0168], Figs. 1, 3, 12L-12M. Watanabe explains “The barrier metal layer 30 and the copper film 31...constitute the second wiring 39. Then, the portion of the second wiring 39, which is buried in the via hole 38a, is served as the plug, and the portion of the second wiring 39, which is buried in the dummy via hole 38b, is served as the dummy plug.” *Id.*, ¶[0168].

232. In Watanabe’s fifth embodiment, the same principle applies. The dummy plug 52 (“dummy via”) and the third wiring 51 (“second interconnect”) are also formed from the same conductive film (i.e. barrier metal layer 72 and copper film 71). *Id.*, ¶¶[0118]-[0122] (wiring buried in dummy via hole 68b is dummy plug 52), Fig. 8.

18. Claim 40 – “semiconductor device of claim 1, wherein the dummy via and the second interconnect include a Cu film”

233. Claim 40 recites the “semiconductor device of claim 1, wherein the dummy via and the second interconnect include a Cu film,” which at least each of Watanabe’s first-to-third and fifth embodiments discloses.

234. Watanabe discloses claim 1, as established in Ground 1A.

235. Watanabe explicitly identifies the conductive film 31, which forms both the wiring 39 (second interconnect) and the dummy plug 34 (dummy via), as “copper film 31”. TSMC-1004, ¶¶[0068]-[0070], Fig. 1, 3.

236. Indeed, Watanabe’s dummy via(s) (dummy plugs 34, 52) and second interconnect(s) (wiring 39, 51) include a Cu film; specifically, dummy plug 34 and wiring 39 include copper film 31, and dummy plug 52 and wiring 51 includes copper film 71. *Id.*, ¶¶[0067]-[0070],[0072],[0118],[0121]-[0122],[0166]-[0167].

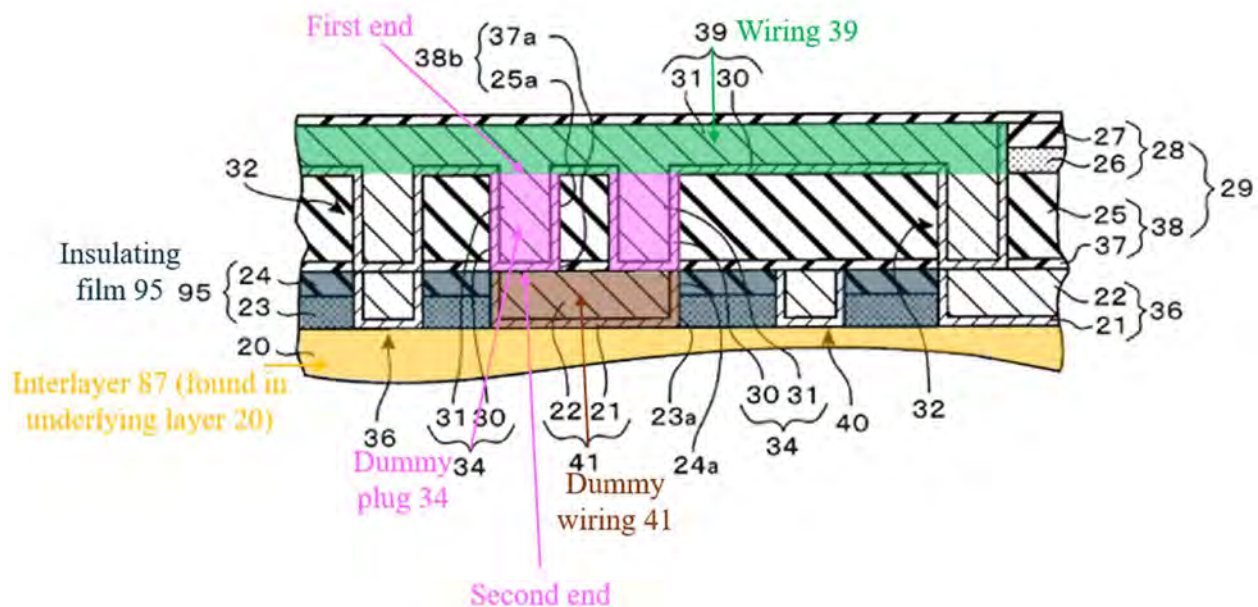
19. Claim 42 – “*semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film*”

237. Claim 42 recites “semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film, which at least each of Watanabe’s second and fifth embodiments discloses.

238. Watanabe’s second embodiment discloses that a dummy via (e.g., dummy plug 34) includes a first and second end, the first end connected to the second

interconnect (e.g., wiring 39) and the second end connected to a first dummy interconnect (e.g., dummy wiring 41), where the first dummy interconnect is surrounded by a second insulating film, e.g., insulating film 95, optionally including interlayer insulating film 87. TSMC-1004, ¶¶[0089]-[0090], [0140]-[0144], [0172]-[0174], Figs. 3, 12B-12D, 12M, 14. This is shown in annotated Fig. 3 below:

FIG. 3



239. As illustrated above, insulating film 95 surrounds a periphery of the second, lower end of dummy 41. More specifically, the first end of dummy plug 34 is connected to the wiring 39 (the claimed “second interconnect”), as they are formed integrally in a dual damascene process. *Id.*, ¶¶[0072], [0167]-[0168], Figs. 3, 12K-12M. The second (bottom) end of dummy plug 34 is connected to a dummy wiring 41 (the claimed “first dummy interconnect”). *Id.*, ¶[0090], Figs. 3, 12M. This dummy wiring 41 is formed within a trench in the first insulating film 95 (comprising

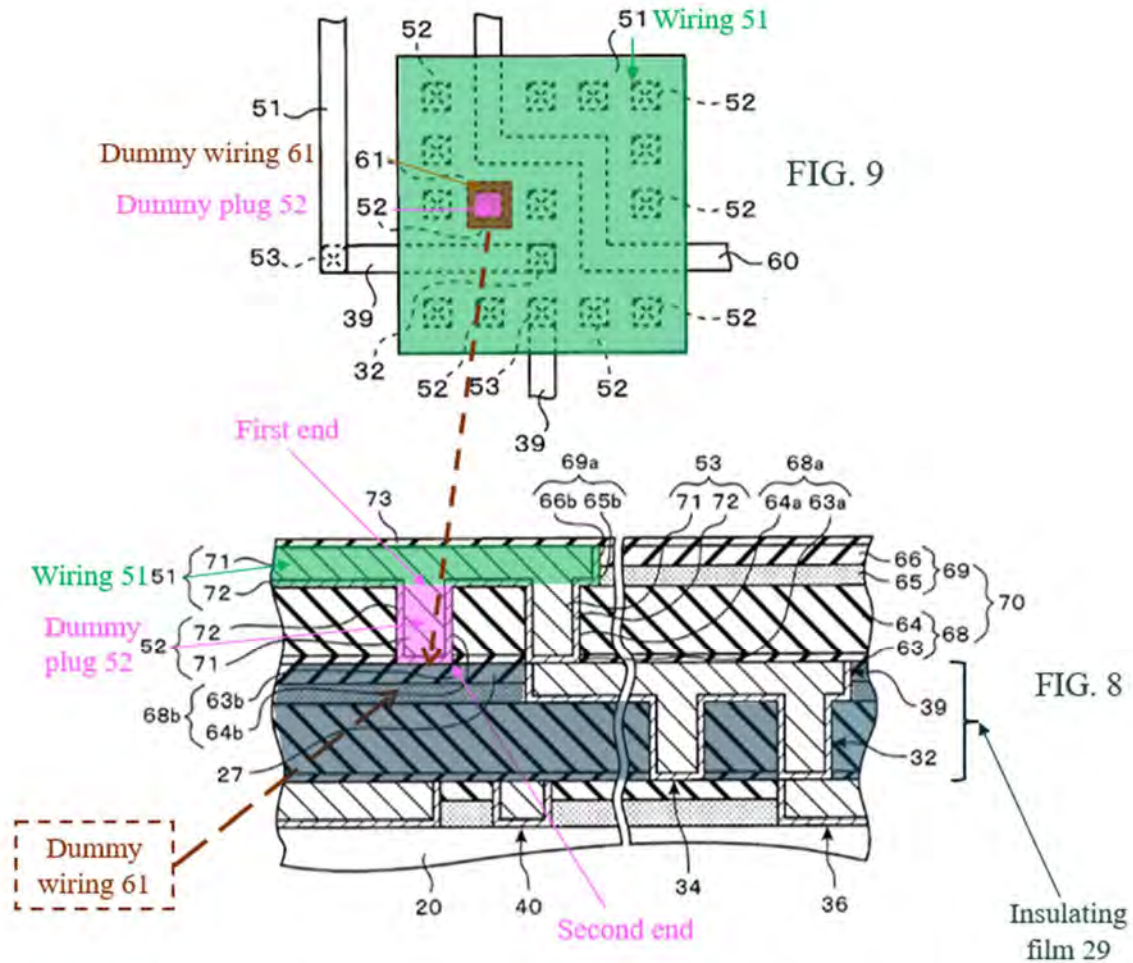
low-dielectric insulating film 23 and silicon oxide film 24), which corresponds to the claimed “second insulating film” in the context of claim 42. *Id.*, Figs. 12B-12D. The dummy wiring 41 is also on the underlying layer 20, which is described as including an insulating film, shown in Figure 14 as including an interlayer insulating film 87. *Id.*, ¶¶[0061], [0173], Figs. 3, 12D, 14. Thus, interlayer insulating film 87 of the underlying layer 20 could also be considered part of the claimed “second insulating film” in the context of claim 42. The dummy wiring 41 is thus laterally confined by the insulating material of first insulating film 95 and supported underneath by the interlayer insulating film 87 of the underlying layer 20, meaning it is surrounded by a “second insulating film” collectively comprising insulating films 95 and 87. *Id.*, Figs. 3, 12d, 14.

240. In Watanabe’s fifth embodiment, dummy via (e.g., dummy plug 52) has a first end connected to second interconnect (e.g., wiring 51) and a second end connected to a first dummy interconnect (e.g., dummy wiring 61), the first dummy interconnect surrounded by a second insulating film (e.g., insulating film 29). TSMC-1004, ¶¶[0127], [0116]-[0123], [0140]-[0144], [0172]-[0175], Figs. 8-9, 12B-12D, 12M.

241. As also outlined above, dummy wiring 61 would be formed in the same layer as wiring 39, and dummy plug 52 is connected to dummy wiring 61. Watanabe explains that “dummy wiring [61] [is] formed in the same layer as the second

wiring 39. The dummy plug 52 may be connected to this dummy wiring 61.” *Id.*, ¶[0127] (emphasis added). Together with Watanabe’s method of manufacturing (*see id.*, [0144], Figs. 12A-12D), a POSITA would understand that “dummy wiring 61” is formed in the same insulating film (e.g., “insulating film 29”)⁵ as “wiring 39” in Figure 8. Annotated Figures 8 and 9 below disclose the approximate location of “dummy wiring 61” when the cross-sectional view otherwise in Figure 8 is drawn through dummy wiring 61. As demonstrated, dummy wiring 61 is surrounded by insulating film 29 (*id.*, Figs. 8-9):

⁵ Watanabe explains that Figure 8 is similar to the first to fourth embodiments, and adds third wiring layer 51. *See* TSMC-1004, ¶¶[0116]-[0117]. Films 25 and 26 are labeled in the first and second embodiments (e.g., Figures 1 and 3) and the manufacturing process figures (e.g., Figures 12A-12M). *See id.*, ¶¶[0066]-[067], [0150]-[0152], *supra*, §X.A.1.(a).(3).



As illustrated above, insulating film 29 in the fifth embodiment as disclosed in Figures 8-9 of Watanabe surrounds a second, lower end of dummy wiring 61.

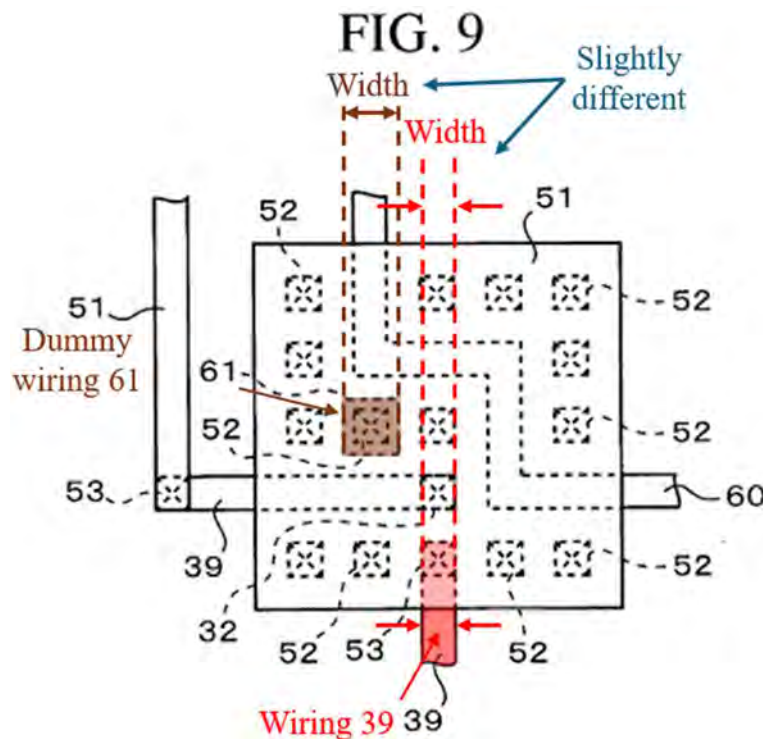
B. Ground 2: Claims 4 and 8 Are Obvious Over Watanabe and Kurashima

242. I believe that claims 4 and 8 are obvious to a POSITA in view of Watanabe and Kurashima. Watanabe discloses claims 1 and 2, outlined above.

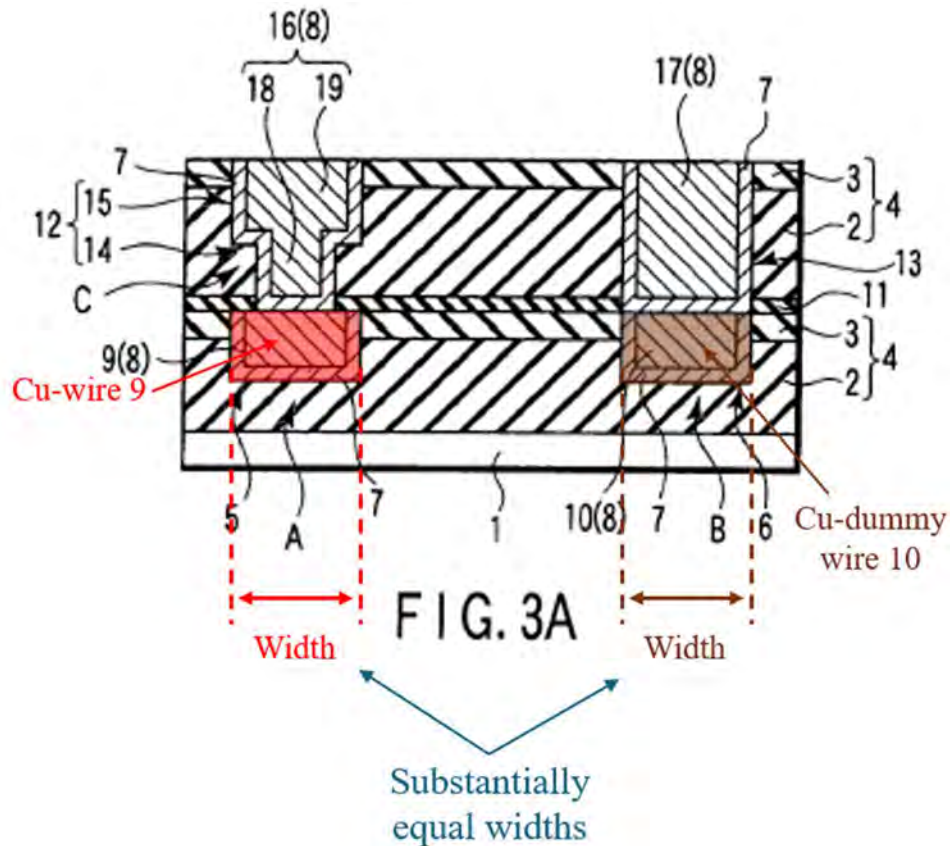
1. Claim 4 – “*semiconductor device of claim 2, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other*”

243. Claim 4 recites the “semiconductor device of claim 2, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other,” which Watanabe and Kurashima render obvious.

244. In Watanabe’s fifth embodiment, Figure 9 discloses dummy wiring 61 (“first dummy interconnect”) with a slightly larger width than wiring 39 (“first interconnect”). TSMC-1004, ¶[0127], Fig. 9. Annotated Figure 9 discloses this relationship:



245. Kurashima teaches simultaneously forming a functional wire (Cu-wire 9 and TaN-film 7, hereafter collectively “Cu-wire 9”) and a dummy wire (Cu-wire 10 and TaN-film 7, hereafter collectively “Cu-wire 10”) that have substantially equal widths. TSMC-1011, 4:38-41, 5:22-31, 7:57-8:3, Figs. 1D, 3A-3B. Annotated Figure 3A of Kurashima discloses these features:



246. Kurashima’s disclosures show that having Cu-wire 9 and Cu-dummy wire 10 be the same width is a known design choice; therefore, slightly adjusting Watanabe’s dummy wiring 61 to have a width equal to wiring 39 was a known design choice. Furthermore, Kurashima teaches that the width of dummy wire 10 matching that of dummy plug 17 ensures a secure adhesive connection between

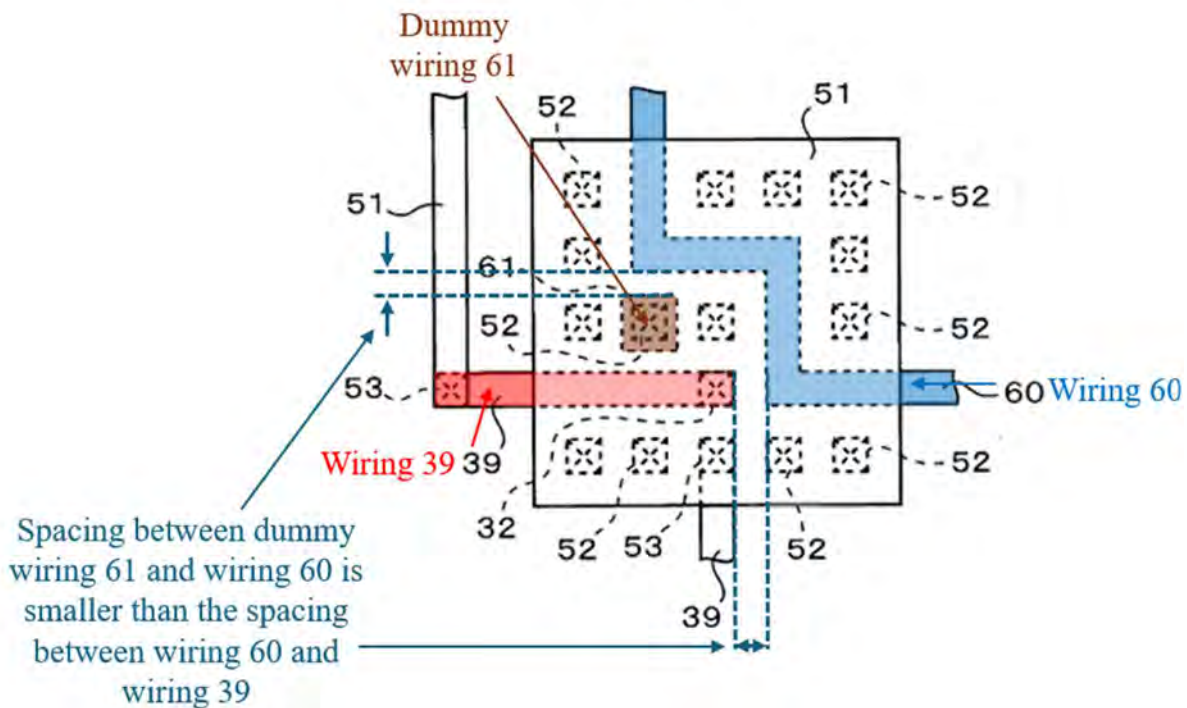
them. *See* TSMC-1011, 4:38-41, 5:22-31, 7:57-8:3, Figs. 1D, 3A-3B. And Watanabe similarly discloses that its conductive plug 53, dummy plug 52, and wirings 39, 51 (the left-hand-most wiring 51 in Watanabe's Figure 9) and have equal widths. This suggests that these features are at a standard feature width for that design level, and that it would be straight forward to provide the dummy wiring 61 with a width equal to the other elements.

247. A POSITA would have recognized that using a dummy interconnect and adjacent first interconnect with substantially the same width, in light of Kurashima's equal dimensions substituted for the nearly similar dimensions in Watanabe, is just a simple substitution involving no criticality. Such a uniform width would have been commonplace, and, I further note that the '623 patent teaches no criticality or surprising or unexpected results with respect to the matching widths of the active interconnect and dummy interconnect in the same level, reinforcing my opinion that such matching dimensions were nothing more than a matter of routine design choice.

248. Moreover, an affirmative motivation for designing Watanabe's dummy wiring 61 to have the same plan-view width as the dummy vias and first interconnect(s), is to ensure adequate spacing (i.e., edge-to-edge distance) between adjacent features—as is seen, for example, with the spacing between interconnects 39 and 60—to reduce unwanted parasitic capacitance and crosstalk. In Watanabe's

Figure 9, dummy wiring 61 and interconnect 60 are not shown to be electrically connected to each other, such that a POSITA would presume they are not so connected and experience different potentials during device operation. However, as Figure 9 shows, the upper edge of dummy wiring 61 is actually closer to interconnect 60 as compared to the spacings of all other features shown, such as the spacing between interconnects 39 and 60, for example, which are also not electrically connected:

FIG. 9



249. This closer spacing between the upper edge of dummy wiring 61 (which is at the same potential as active interconnect 51 (underneath which dummy wiring 61 resides) given their connection to each other from dummy plug 52) and

interconnect 60 would lead to more parasitic capacitance and crosstalk between them as compared to two structures held at a greater spacing apart, such as at the spacing between wirings 39 and 60. Watanabe itself expressly acknowledges this problem of inter-wiring capacitance. TSMC-1004, ¶[0034]. A POSITA would have been motivated to reduce the size of dummy wiring 61 to have the same dimension of dummy plug 52 (and thereby the same dimension as the first interconnect 39) so that a uniform spacing is achieved between dummy wiring 61 and interconnect 60, i.e., the same spacing as seen between interconnect 39 and interconnect 60.

250. A POSITA understood that a dummy interconnect width matching that of the dummy vias as well as an active interconnect in the same level would have allowed for a greater and more uniform spacing between components, yet while still ensuring a secure adhesive connection between dummy via/dummy interconnect as taught by Kurashima by maintaining the dummy via and dummy interconnect at the same dimension. If a POSITA desired even greater mechanical stability, this would be easily achieved by adding more dummy wirings under dummy plugs like dummy wiring 61 shown in Figure 9, but with the dummy wiring dimensions matching those of the dummy plugs 52.

251. A POSITA would have had a reasonable expectation of success because the POSITA would employ the same manufacturing process already found in Watanabe. Matching the widths of dummy wiring 61 with the wiring 39 is readily

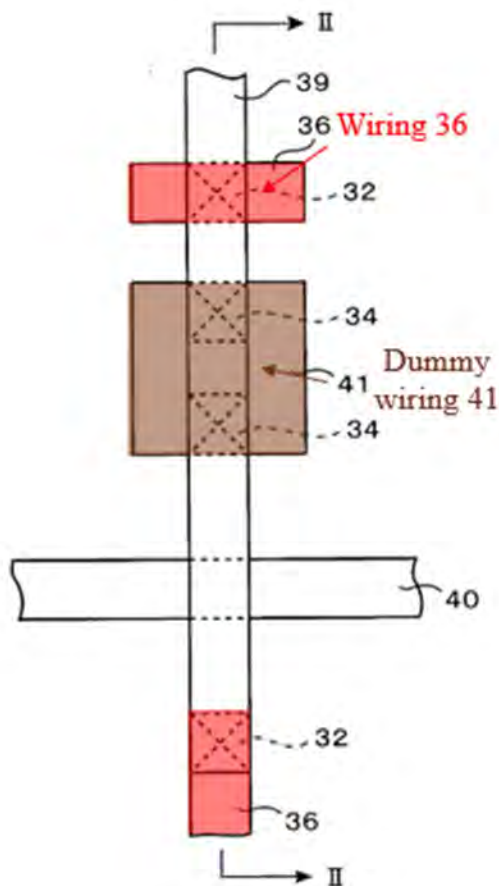
achieved simply by adjusting the dimensions of the dummy wiring features, while still using the same patterning steps and materials.

2. Claim 8 – “semiconductor device of claim 2, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle”

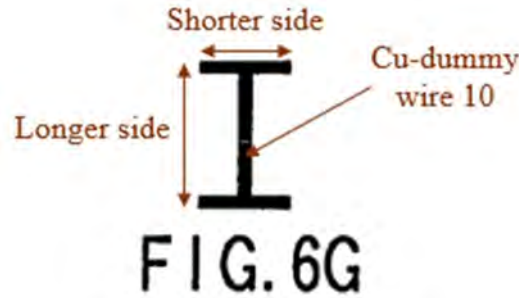
252. Claim 8 recites the “semiconductor device of claim 2, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle,” which Watanabe and Kurashima render obvious.

253. Watanabe’s Figure 4 (second embodiment) includes a horizontally extending wiring 36 (“first interconnect”) and a vertically extending wiring 36, both connected to wiring 39 (“second interconnect”) through respective plugs 32 (“via”). TSMC-1004, Fig. 4. A POSITA would recognize that Watanabe’s Figure 4 exemplifies wiring that extends in various directions, sometimes as a single wiring (see, e.g., wiring 60 in Figure 9) and at other times as separate wires as with wirings 36 in Figure 4. Considering either side of dummy wiring 41 (“first dummy interconnect”) as longer, that longer side will form substantially a right angle with one of the wirings 36. *See id.* Annotated Figure 4 showing wirings 36 and dummy wiring 41 is disclosed below:

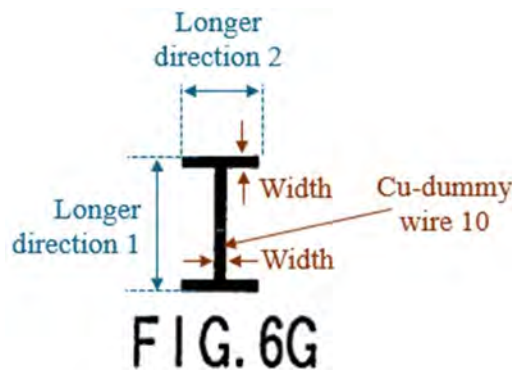
FIG. 4



254. Moreover, Kurashima teaches Cu-dummy wiring 10 (analogous to Watanabe's dummy wiring 61) having numerous shapes with one overall side longer than another to reduce CMP stress and the possibility of film peeling. TSMC-1011, 3:25-33, 6:11-32, 10:4-21, 10:58-67, 12:49-52; Figs. 3B, 6A, 6E, 6G, and 6M. Annotated Figure 6G of Kurashima, which discloses an exemplary shape for dummy wire 10, is shown below:



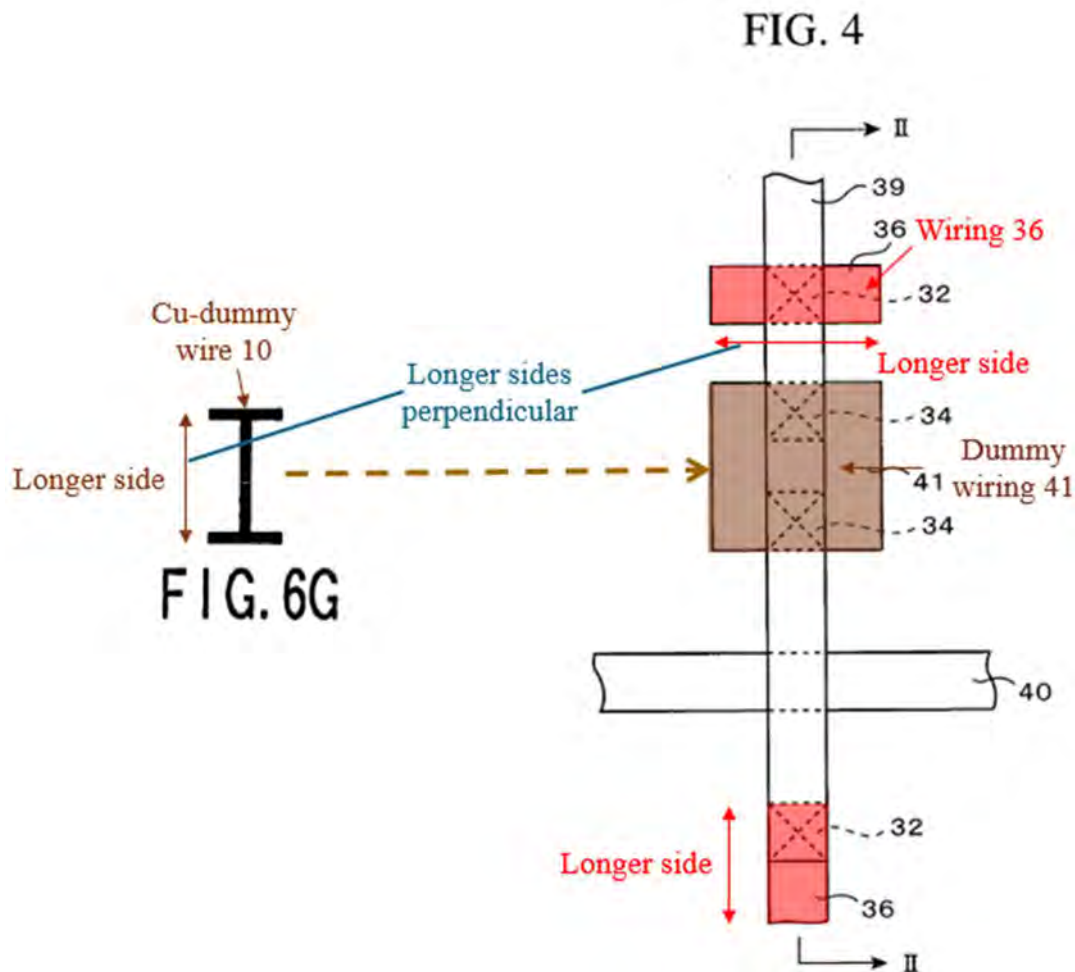
255. Other shapes in Kurashima's Figures 3B, 6A, 6M, etc. have an overall longer side from top to bottom, while the shapes in Figures 7D, 7G-7H, 8C, and 9C have an overall longer side from left to right. *Id.*, Figs. 3B, 6-9. Similarly, if the "longer side" of the dummy wire is simply considered to be the direction orthogonal to its width, Kurashima's dummy wires have "longer sides" running both up-down and side-to-side:



Under either reading, Kurashima's Figure 6 teaches dummy interconnect patterns having "longer sides" in both orthogonal directions (i.e., top-to-bottom and side-to-side).

256. It would have obvious to a POSITA to extend dummy wiring 41 in Watanabe in one direction or another (i.e., other than a square) based on Kurashima's

teachings to use any of a multitude of beneficial dummy wiring designs such as Figure 6G, and either results in the longer side of dummy wiring 41 forming a right angle with a longer side of one of the second wirings 39 (“first interconnect”). Thus, implementing such an alternative, well-known design for dummy wiring 41 in Watanabe results in a longer side of dummy wiring 41 that forms a right angle with a longer side of one of the two wirings 36 (“first interconnect”):



257. I have outlined one possible combination, and Kurashima teaches a multitude of shapes that, as used for dummy wiring 41, would each result in a longer

side of dummy wiring 41 that forms a right angle with a longer side of one of the two wirings 36. The same idea also applies to Figure 9 (fifth embodiment) of Watanabe, just accounting for spacing requirements between components. The POSITA would recognize to layout the interconnects (including active and dummy) according to needed parameters for a given situation, and the dummy wiring 61 can be shaped with Kurashima's teachings while accounting for necessary spacing.

258. Kurashima further provides rationale for its alternative shapes that would provide suggestion to the POSITA for using its noted shapes, such as Fig. 6G. Kurashima teaches such an alternative shape for the dummy interconnect can bear large stresses such as mechanical stress from CMP, including enhancing a bearing force for the CMP stress generated in various directions. TSMC-1011, 10:4-21. Kurashima further teaches to avoid confined dielectric film areas in favor of low-relative dielectric constant films inside the dummy wire that are contiguous with low-relative-dielectric constant film outside the dummy wire (i.e., non-confined), whereby CMP stress added to dummy wire and low-relative-dielectric-constant film inside the wire can be released to outside the dummy wire. *Id.*, 10:58-67. A POSITA would have been motivated by Kurashima, appreciating that utilizing the dummy wiring shapes taught by Kurashima for Watanabe's dummy wiring 41 would better alleviate/dissipate CMP stresses placed on the dummy wiring and insulating film 23 in which dummy wiring 41 is formed. As stated by Kurashima, "the CMP stress

added to the dummy wire and the low-relative-dielectric-constant film inside the wire can be released to the outside of the dummy wire.” *Id.*

259. Moreover, because Kurashima teaches that the dummy wiring shape (i.e., ones having various “longer side” orientations) impacts device reliability and manufacturability (TSMC-1011, 3:25-33, 6:11-32; 10:4-21, 10:58-67, 12:49-52; Figs. 3B, 6A, 6E, 6G, 6M), it would have been routine optimization for a POSITA to determine the optimal orientation and longer-side dimension of Watanabe’s dummy wirings 41 (Figure 4) and 61 (Figure 9) relative to the lower-level interconnect direction.

260. A POSITA would have had a reasonable expectation of success in implementing such interconnect shapes, because extending Watanabe’s dummy wiring 61 in one direction or another as shown by Kurashima involved a mere design choice that could be readily implemented with Watanabe’s existing manufacturing process. Implementing such interconnect shapes and orientations merely required that the trenches defining such interconnects be patterned as desired. This was readily accomplished with standard techniques at the time.

C. Ground 3: Claims 9 and 17-18 Are Obvious Over Watanabe and Iizuka

261. I believe that claims 9 and 17-18 are obvious to a POSITA in view of Watanabe and Iizuka. I previously summarized Iizuka. *Supra*, §IX.F.

1. Claim 9

a) [9.a] - “semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view”

262. Element [9.a] recites the “semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view,” which Watanabe in view of Iizuka renders obvious.

263. Watanabe discloses claims 1 and 2 from which claim 9 depends.

264. Watanabe further discloses a simulation model with plug 32 (“via”) and dummy plug 34 (“dummy via”) as a “circular cylinder,” i.e., disclosing them to the POSITA as substantially circular in plan view. TSMC-1004, ¶[0083], Figs. 1, 3. A POSITA would recognize that the same applies to dummy plugs 52 in all of Watanabe’s embodiments. *E.g., id.*, Fig. 9. Disclosing the circular cylinder shape for its simulation model teaches circular vias to a POSITA for Watanabe’s devices, since this is the shape on which Watanabe’s modeling was done. A POSITA would thus interpret Watanabe as disclosing vias having circular cross-sections in plan view, in addition to the square vias disclosed in the figures.

265. Like Watanabe, Iizuka is directed to a “semiconductor device” in which “via-holes” are formed. *See* TSMC-1008, Abstract. Iizuka demonstrates that it was well-known prior to the ’623 patent that vias could have many polygonal cross-sectional shapes and that the selection of a specific shape was simply a design choice.

For example, Iizuka teaches the common nature of circular via-holes and the interchangeability with other common shapes such as squares: “the opening of the via-hole may have any configuration, such as a square, rectangle or circle.” *Id.*, 9:45-47 (emphasis added). Iizuka’s description of via-hole 6 as having a “diameter” similarly discloses a circular via shape, since the geometrical term “diameter” corresponds with circular shapes. *Id.*, 6:60-63, Fig. 5A.

266. Thus, a POSITA understood that circular shaped vias were common and standard in the industry, as evidenced by Iizuka, and would have understood that the dummy plugs 34 and 52 in Watanabe could be made to be substantially circular in a plan view. This is further evidenced, for example, by Hasunuma, which shows circular vias/dummy vias in various embodiments. *See, e.g.*, TSMC-1005, ¶[0200], Fig. 19A (showing circular-shaped dummy vias 125); *see also* TSMC-1013, 8:47-52 (noting that circular vias may be used, among other shapes). Also, Igarashi teaches circular vias as the default shape for all via connections, except where square vias or other shapes are needed for a given overlap of the upper and lower interconnects. TSMC-1014, ¶¶[0091]-[0092], Figs. 8, 14 (teaching circular vias as a default shape, and square vias as preferred for certain interconnect junctions). Thus, a POSITA understood that square and circular shapes are among a finite number of common, interchangeable design choices for via/dummy via shapes, and circular vias were well-known, as expressly taught by Iizuka, among others.

267. In addition, particular via shapes, such as square or circular, each provide known advantages applicable to a given situation. *See, e.g.*, TSMC-1014, ¶¶[0091]-[0092], Figs. 8, 14 (disclosing the use of circular and square vias, depending on the specifics of the interconnect junction). More specifically, circular vias can provide for greater manufacturing process control (e.g., more uniform etching and filling characteristics for circular shapes compared to sharp-cornered squares), more favorable stress distribution around a circular opening, and design simplicity. *See, e.g.*, TSMC-1038, 7:61-67 (teaching that vias having circular cross-sections benefit from more precisely controlled etching, improved coverage of barrier metal in the via opening, and easier fill-in of the via opening with a metal film). Circular-shaped vias also provide improved reliability due to the lack of sharp corners that can concentrate stress and cause damage in the form of dielectric cracking and the like.

268. While there can sometimes be operational or design considerations that lead to a preference for circular or square vias, a POSITA nonetheless recognized that the fundamental stress-relieving function of Watanabe's dummy via (or the electrical connection function of Watanabe's via) in terms of attracting and sequestering vacancies, preventing void formation, and providing a surplus of copper atoms, would be roughly the same with both circular and square dummy vias. That is because these functions do not generally depend on the exact cross-sectional

shape of the dummy via. To the extent some minor differences in performance exist, implementing circular vias would have promoted greater consistency with Watanabe's simulation results which were based on circular-shaped vias. A POSITA would have further recognized that the structural strengthening functions of Watanabe's dummy via would not be materially altered by adopting a circular cross-section versus a square. Indeed, both circular and square vias would still strengthen the overall layers of Watanabe's device and reduce the mechanical stress exhibited at the functional vias.

269. Further, because a POSITA was aware of these shapes, and was aware of the role of the dummy vias in mitigating stress-induced voiding and electromigration problems as taught, for example, by Watanabe (*supra*, §IX.A), it would have been a matter of routine optimization to choose the via shape that works best for a given overall design. I understand that the Examiner suggested the same during prosecution. TSMC-1002, 244-45, 292-96. With a few basic shapes to choose from (e.g., circular, square, rectangular), it would not have required an undue amount of experimentation to arrive at the optimal via shape.

270. A POSITA understood that there was no criticality associated with having a circular via or dummy via shape and that such circular-shaped vias would have operated substantially the same as other shapes. That is, there was no surprising or unexpected performance benefit associated with circular vias as opposed to other

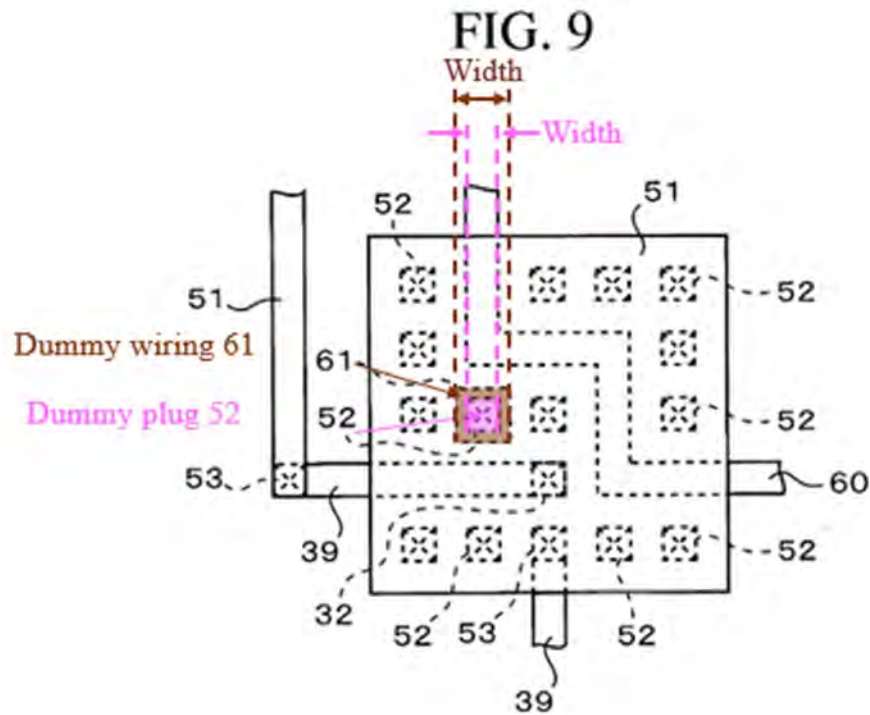
shaped-vias. Any difference in performance was well understood and something that a POSITA would have balanced with other considerations (such as manufacturing limitations, costs, etc.) when choosing the appropriate shape for the functional and dummy vias for a given application. In this regard, I note that the '623 patent teaches no criticality or surprising or unexpected results with respect to the cross-sectional shape of its vias or dummy vias, reinforcing my opinion that such shapes were nothing more than a matter of routine design choice.

271. A POSITA would have had a reasonable expectation of success in implementing such circularly-shaped dummy vias. Indeed, as demonstrated by Iizuka (and other references at the time) as well as the modeling of Watanabe, circular vias (including dummy vias) were routinely used in semiconductor devices and thus their fabrication and associated techniques was well understood. *See* TSMC-1005, Fig. 19A; TSMC-1014, ¶[0091]; TSMC-1013, 8:47-52; TSMC-1038, 7:62-67. Thus, a POSITA would not have expected any significant hurdles or problems when implementing such a shape for Watanabe's dummy vias.

b) [9.b] – “a diameter of the dummy via is smaller than a width of the first dummy interconnect”

272. Element [9.b] recites “a diameter of the dummy via is smaller than a width of the first dummy interconnect,” which Watanabe discloses.

273. Watanabe discloses, including in Figure 4 (second embodiment) and Figure 9 (fifth embodiment), dummy plug 34 or 52 (“dummy via”) having a smaller width than dummy wiring 41 or 61 (“first dummy interconnect”). TSMC-1004, ¶¶[0090]-[0091], [0127], Figs. 2, 4, 9. For example, as shown in annotated Figure 9 below, Watanabe’s fifth embodiment discloses dummy plug 52 (“dummy via”) with a width that is smaller than a width of the dummy wiring 61 (“first dummy interconnect”) to which it connects:



Id., ¶[0127], Fig. 9.

274. A POSITA would understand that, with a circular dummy plug 34 or 52, the diameter of the dummy plug 34/52 will be smaller than a width of dummy wiring 41/61. That is, the shape of the dummy plug 34/52 would become circular,

and its diameter would be analogous to the width of the original square shape. This is consistent with Watanabe's Figure 17B showing that the side dimension of the square dummy vias is 0.15 μm , and Watanabe's modelling of the dummy vias as cylinders with a diameter of 0.15 μm . *Id.*, ¶[0083], Fig. 17B. Thus, with the width of the dummy wiring 41/61 as disclosed in Figures 4 and 9 relative to the dummy vias, the circular-shaped dummy via will have a diameter smaller than the dummy interconnect.

275. A POSITA would have expected success in implementing Watanabe's dummy vias with circular shapes having diameters smaller than the dummy interconnect width, as this configuration would have been easily accomplished using the standard patterning and manufacturing techniques used to make the interconnect structure in general. It was well known how to pattern via holes having circular cross-sections using masks, photolithography, and etching, and such round patterns subsequently result in circular vias when conductive material is deposited into the patterned vias holes.

2. Claim 17 – “*semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view*”

276. Claim 17 recites the “semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view,” which Watanabe in view of Iizuka renders obvious.

277. As discussed above, Watanabe discloses both vias (e.g., plugs 32/53) and dummy vias (e.g., dummy plugs 34/52). *Supra*, §X.A.1. Watanabe's plan view figures disclose square vias and dummy vias. Watanabe also discloses a simulation model with conductive plug 32 ("via") and dummy plug 34 ("dummy via") as a "circular cylinder," i.e., disclosing them to the POSITA as substantially circular in plan view. TSMC-1004, ¶[0083], Figs. 1, 3. A POSITA would recognize that the same applies to conductive plugs 53 and dummy plugs 52 in all of Watanabe's embodiments. *E.g., id.*, Fig. 9. Disclosing the circular cylinder shape for its simulation model teaches circular vias to a POSITA for Watanabe's devices, since this is the shape on which Watanabe's modeling was done. A POSITA would thus interpret Watanabe as disclosing vias and dummy vias having circular cross-sections in plan view, in addition to the square vias and dummy vias disclosed in the figures.

278. As discussed for claim 9, Iizuka demonstrates that it was well-known prior to the '623 patent that vias could have many polygonal cross-sectional shapes and that the selection of a specific shape, including a circular shape, was simply a design choice. *Supra*, X.C.1.(a). For the same reasons discussed for claim 9, it was obvious to use circular shapes for Watanabe's vias (e.g., conductive plugs 32, 53) and dummy vias (e.g., dummy plugs 34, 52). *Id.*

3. Claim 18 – “semiconductor device of claim 17, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other”

279. Claim 18 recites the “semiconductor device of claim 17, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other,” which Watanabe in view of Iizuka renders obvious.

280. Watanabe’s own simulation model, which, as discussed for claim 17, utilizes circular vias and dummy vias, assigns the identical diameter (0.15 μm) to both its functional conductive plug 32 (“via”) and its dummy plug 34 (“dummy via”). TSMC-1004, ¶[0083] (“In the simulations in FIGS. 15A, 15B, 16A, and 16B, the distance between the centers of the neighboring plugs 32, 32 (i.e., the wiring length) was fixed to 10 μm . Then, as the model of the plug 32 and the dummy plug 34 a circular cylinder whose diameter is 0.15 μm and whose height is 0.42 μm was employed.”). Thus, with a POSITA implementing Watanabe’s vias and dummy vias as circular (as rendered obvious by Iizuka), it would have been further obvious to a POSITA to further make the diameters of both the vias and the dummy vias substantially equal, as directly suggested by Watanabe’s own modeling parameters.

281. This choice would have been motivated by design simplicity, process commonality for etching and filling these features, and to ensure consistent relative

behavior if the dummy via's effectiveness is linked to its size relative to the functional via, for example with respect to the effects on mechanical properties. For example, having the same shape and size vias and dummy vias makes processing much easier relative to design in which the shape and sizes vary. Indeed, a POSITA recognize that the same patterning, etching, and filling parameters could be reused across all vias and dummy vias having common sizing and shapes. Reusing the same patterning technique and parameters would improve consistency and reliability across the vias and dummy vias.

282. The expectation of success in implementing vias and dummy vias with substantially equal diameters would be high, as Watanabe's own simulation model demonstrates this configuration, and Watanabe consistently discloses same-sized vias and dummy vias. A POSITA would simply have designated the vias and dummy vias as having the same size, and the standard manufacturing process would then build them as such.

D. Ground 4: Claims 45-47 Are Obvious Over Watanabe and Kamoshima

283. I believe that claims 45-47 are obvious to a POSITA in view of Watanabe and Kamoshima. I previously summarized Kamoshima. *Supra*, §IX.G. I first outline the disclosures of these references relative to claims 45-47, and then provide motivation to combine their teachings for these claims.

1. Claim 45

a) [45.a] – *“semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion”*

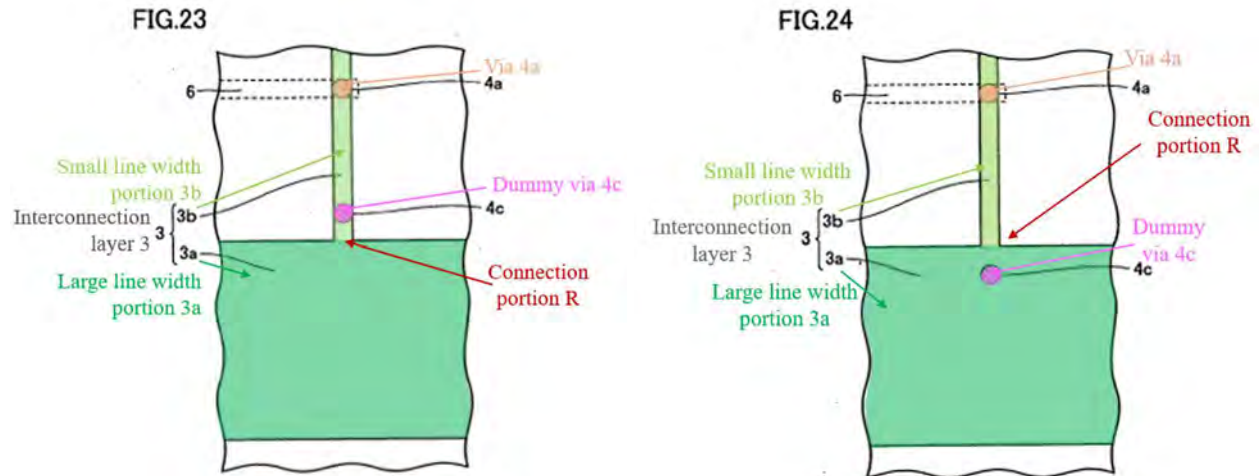
284. Element [45.a] recites the “semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion,” which Watanabe and Kamoshima render obvious.

285. Kamoshima discloses interconnections having a constant width, such as interconnection layer 3 (Figure 3), Kamoshima also discloses an interconnection with a branched shape including a large line width portion 3a and a small line width portion 3b. TSMC-1009, ¶¶[0002], [0062], [0068]-[0069], [0094]-[0103], Abstract, Figs. 8-9, 23-27.

286. For example, in Figures 23-27, Kamoshima discloses a second interconnect (e.g., “interconnection layer 3) that is comprised of a first interconnect portion (e.g., “large line width portion 3a”) and a second interconnect portion (e.g., “small line width portion 3b”) whose interconnect width is smaller than that of the

first interconnect portion and which branches from the first interconnect portion.

See annotated Figures 23 and 24 below (*see id.*, ¶¶[0094]-[0103], Figs. 23-27):



287. Kamoshima teaches having via 4a in small line width portion 3b and dummy via 4c in the vicinity of the “connection portion R” between the two interconnection portions 3a, 3b (*see id.*, Figs. 23-24). Kamoshima’s approach provides a local, targeted protection for the most vulnerable point—the functional via—by creating a bottleneck with the small line width portion 3b to prevent voids from reaching it.

b) [45.b] – “the via is connected to the second interconnect portion”

288. Element [45.b] calls for “the via is connected to the second interconnect portion,” which Watanabe and Kamoshima render obvious.

289. Watanabe's vias (plugs 32, 53) are likewise connected to the second interconnect (e.g., wirings 36, 39). TSMC-1004, ¶¶[0067]-[0073], [0118]-[0122], [0159]-[0165], Figs. 1, 3, 8-9, 12J-12K. See annotated Figures 2 and 9 below:

FIG. 2

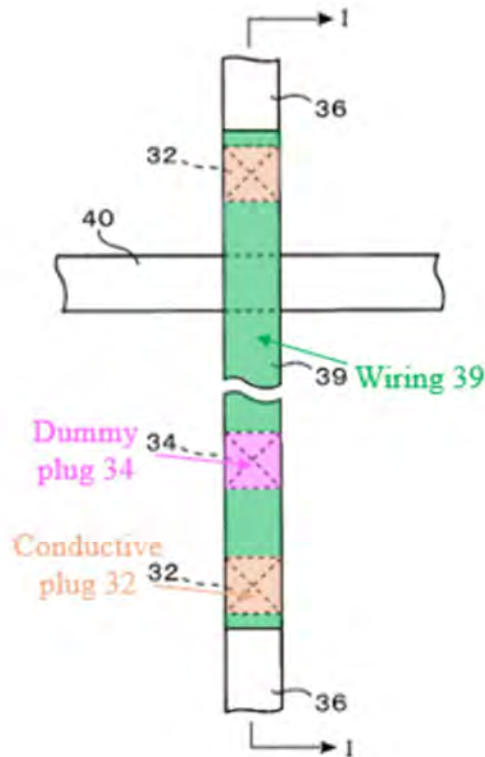
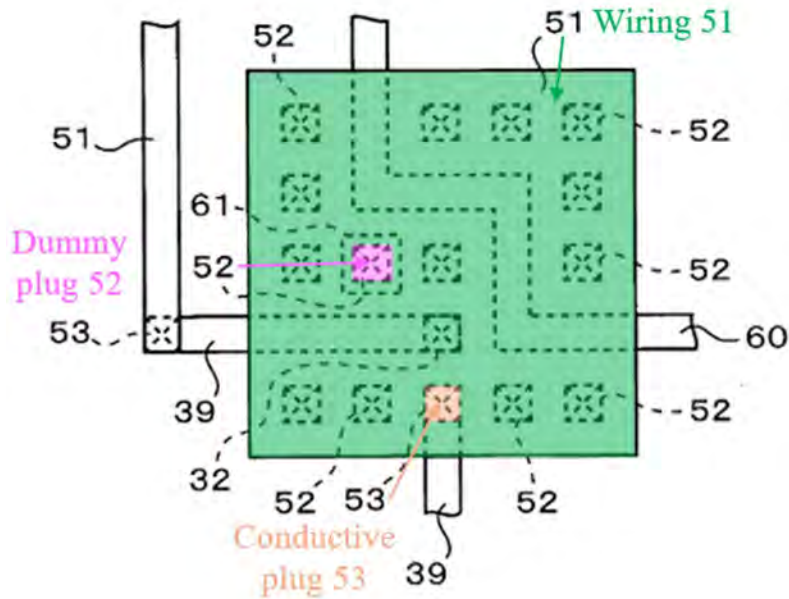


FIG. 9



290. Kamoshima discloses that the via (e.g., “via 4a”) is connected to the second interconnect portion (e.g., “interconnection portion with a small line width 3b”). TSMC-1009, ¶¶[0095] (“Interconnection layer 3 includes an interconnection portion with a large line width 3a, and an interconnection portion with a small line width 3b. Interconnection layer 6 is electrically **connected to interconnection portion with a small line width 3b of interconnection layer 3 through via 4a.**”), [0098], Figs. 23-24. See annotated Figures 23-24:

FIG.23

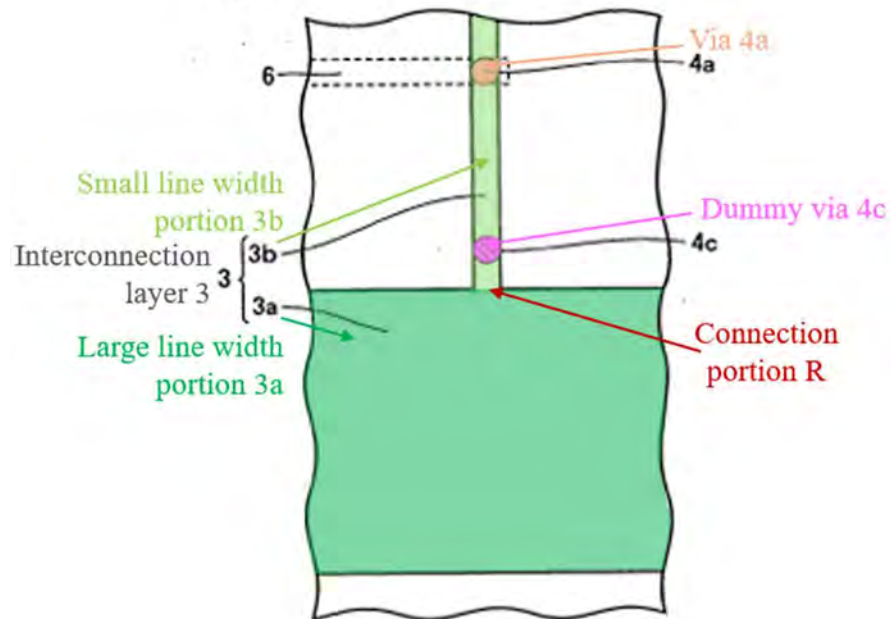
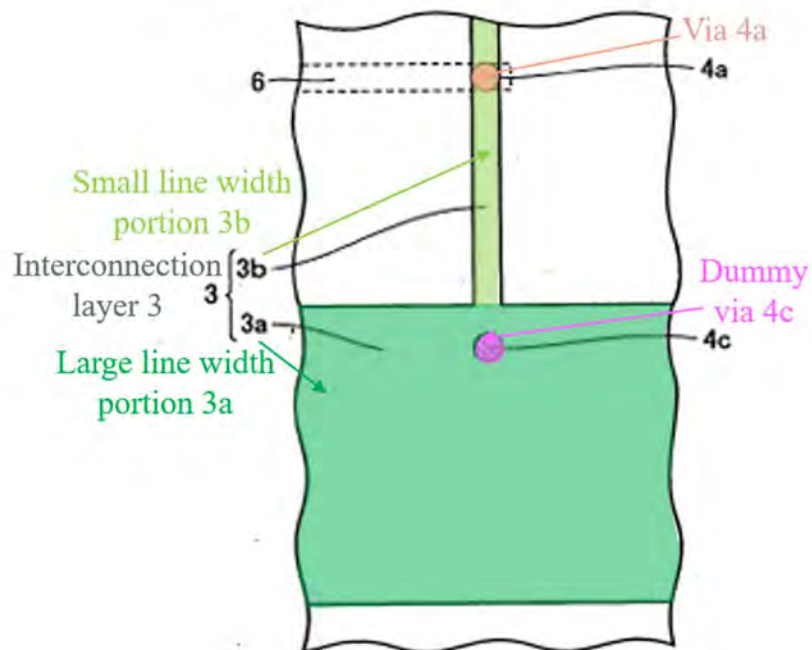


FIG.24



c) Obviousness of Combining Watanabe and Kamoshima

291. As discussed previously, the first through third and fifth embodiments of Watanabe disclose a second interconnect (e.g., “wiring 39,” “wiring 51”). *Supra*, §§X.A.1.(a).(5), X.A.1.(b)-(d). As examples, annotated Figure 1 (first embodiment) discloses wiring 39 and Figure 8 (fifth embodiment) discloses wiring 51:

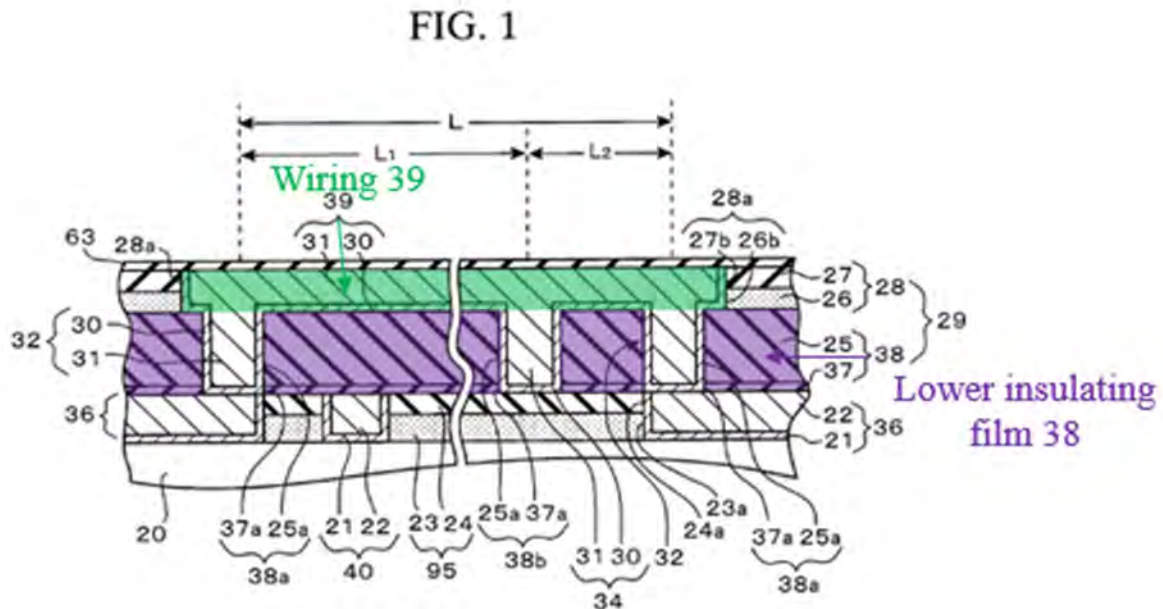
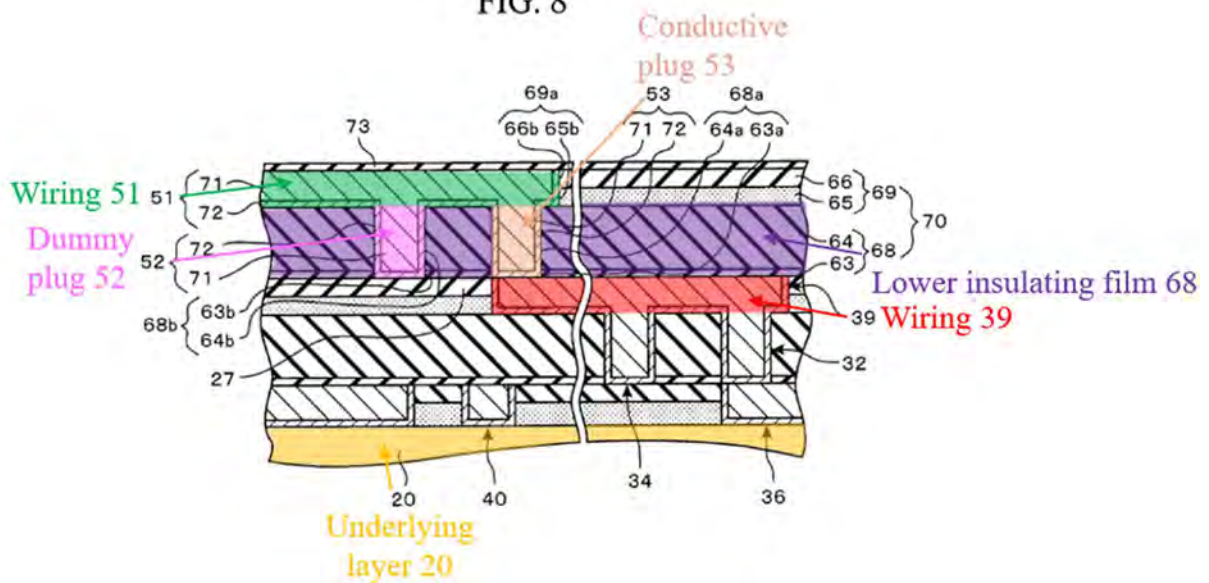


FIG. 8



292. In view of Kamoshima (e.g., Figures 23-24), a POSITA would have understood the claimed branched shape (with a narrower portion extending from a wider portion) was a known design option for the shape of any of Watanabe's wirings that correspond to the claimed "second interconnect" (e.g., "wiring 39," "wiring 51"). Thus, it was obvious to a POSITA for Watanabe's second interconnects (e.g., wiring 39, wiring 51) (in any of the first-to-third and fifth embodiments) to be similarly shaped so as to create an interconnect having a branched configuration similar to Kamoshima's "interconnection layer 3" of Figures 23-24. Doing so would simply involve changing Watanabe's "wiring trench 28a" (or "wiring trench 69a") in "insulating film 29" (or "insulating film 70") so that the wiring trenches 28a (or 69a) included a similar shape as Kamoshima's interconnection layer 3 from Figures 23-24.

293. Moreover, because Kamoshima's interconnection layer 3 is connected to both a real via (i.e., via 4a) and a dummy via (i.e., via 4c) (see, e.g., TSMC-1009, Figs 22-24), a POSITA would have understood that the shape of Kamoshima's "interconnection layer 3" was an option for Watanabe's upper layer wirings (e.g., "second wiring 39" and "third wiring 51"), which likewise are common interconnects that are connected to both a real via (e.g., "conductive plug 32") and a dummy via (e.g., "dummy plug 34"). TSMC-1004, ¶¶[0070]-[0073], [0117]-[0122], Figs. 1-5C, 8-9. Accordingly, when considering potential shapes for Watanabe's "second wiring 39" and "third wiring 51," a POSITA would have considered the shapes of Kamoshima's "interconnection layer 3" as potential options given their similarity in connections (e.g., to both real and dummy vias).

294. Given that such a shape was a known design option, a POSITA would have been motivated to select that shape wherever the design objectives for the corresponding device would have found that shape advantageous. For example, Kamoshima motivates a POSITA to use an interconnection layer with large and small width portions, and positioning the via (for connection to another interconnect) along the small line width portion and dummy via in vicinity of the connection portion between these interconnect portions, to cause microvoids that would otherwise distribute between the via and the dummy via to further concentrate under the dummy via before reaching the via. *See* TSMC-1009, ¶¶[0088], [0097]-[0099].

Such an interconnect design thus further suppresses the concentration of voids under the real via positioned on the narrow portion/branch. Kamoshima expressly notes that such an interconnect design offered the foregoing benefit of further suppressing void concentrations in the narrower branch, where the real via could be located. *See Id.*, ¶[0098] (“A large number of microvoids in interconnection layer with a large line width $3a$ tend to *concentrate in the area under dummy via 4c before reaching the area under via 4a*. **Therefore, concentration of voids in the area under via 4a can further be suppressed.**”); *see also id.*, ¶¶[0088],[0097]-[0099]. Thus, Kamoshima teaches a known design choice of an interconnect shape that has the added benefit of further suppressing microvoids under functional vias. Kamoshima motivates the design to suppress the concentration of voids due to stress migration. *See id.*, ¶¶[0097]-[0098], [0105], [0109], [0111].

295. Following Kamoshima’s teachings, a POSITA would update Watanabe’s second interconnect 39, 51 to include a large line width portion and a small line width portion branched therefrom, analogous to Kamoshima’s interconnection layer 3 from Figures 23-24. Watanabe’s plug 32/53 would be connected to the small line width portion and dummy plug 34/52 would be connected to the large line width portion. This branched interconnect shape would further enhance suppression of the microvoids in Watanabe’s design in any of its first-to-third and fifth embodiments. *See also* TSMC-1033, ¶¶[0056]-[0057], [0112]-[0114]

(“A sample without the narrow wiring and a sample having the narrow wiring length of 2 μm was checked.... The sample without the narrow wiring showed the defective factor of about 1%. The sample with the narrow wiring of about 2 μm in length showed the defective factor of about 0%.”); TSMC-1037, 162-63, 165, Figs. 9, 14. Watanabe already teaches address stress migration, and the POSITA would recognize that incorporating Kamoshima’s interconnect shape and corresponding via/dummy via configuration teaching would further enhance the suppression of microvoids.

296. A POSITA would have been motivated to combine the teachings of Watanabe and Kamoshima because the references address the identical problem of stress-induced voiding with complementary solutions that operate on different scales. Watanabe teaches a global approach, using dummy conductive plugs to reduce overall stress across the interconnect area. Kamoshima’s use of a small line width portion (3b) provides a local, targeted protection for the most vulnerable point—the functional via—by creating a bottleneck to prevent voids from reaching it. Kamoshima identifies the issue migration of microvoids from a large area interconnect portion, which acts as a large reservoir for such defects. The solution taught by Kamoshima is to physically isolate the functional via from this large reservoir. Therefore, placing Watanabe’s functional via on this narrow portion directly applies Kamoshima’s protective teaching, using the geometry to starve the

critical area under the via from the main source of failure-causing voids. A POSITA would have found it obvious to apply Kamoshima's geometric protection to Watanabe's structure to create a more robust design that benefits from both the global stress relief of Watanabe and the targeted via protection of Kamoshima. The benefits would be seen as additive; a POSITA would expect Watanabe's dummy plugs to continue to provide global stress relief in the wide interconnect portion, while simultaneously expecting Kamoshima's narrow bottleneck to effectively isolate the functional via from void migration.

297. A POSITA would have found this modification easy to implement and thus would have had a reasonable expectation of success when doing so. Both Watanabe and Kamoshima relate to forming an interconnect connected to both a via (to connect to another interconnect) and dummy via, where the dummy via is present to suppress voids from concentrating in the via. *See* TSMC-1004, ¶¶[0012]-[0019], [0070]-[0073], [0075], [0117]-[0122], Figs. 1-5C, 8-9; TSMC-1009, ¶¶[0085]-[0086], [0088], [0094]-[0099], Figs. 15-16, 23-27.

298. The foregoing modification to Watanabe would merely involve selecting the location of the via/plug such that it was located in the narrow interconnect portion, and forming the via/plug using the same processes already taught in Watanabe. Indeed, implementing the foregoing interconnect configuration would have merely involved etching the wiring trench in the desired branched shape

with appropriate trench portion widths and then filling such trenches with appropriate conductive material (e.g., barrier metal layer and bulk copper layer) to form the interconnect and via holes, which was well within the capabilities of a POSITA at the time of the alleged invention. The modification would be readily achieved with Watanabe's manufacturing process by using appropriate trench portion widths/shapes.

2. Claim 46 – “*semiconductor device of claim 45, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions*”

299. Claim 46 recites “wherein the dummy via is formed at or near the branch point between the first and second interconnect portions,” which Watanabe and Kamoshima render obvious.

300. Kamoshima discloses that the dummy via (e.g., dummy via 4c) is formed at or near the branch point (e.g., “connection point R”) between the first and second interconnect portions (e.g., point at the intersection of “interconnection portion with a large line width 3a” and “interconnection portion with a small line width 3b”). TSMC-1009, ¶[0099] (“Even when dummy via 4c is arranged on interconnection layer with a large line width 3a as shown in FIG. 24, an effect as described above can be attained, **so long as dummy via 4c is arranged in the vicinity of connection portion R of interconnection portion with a large line**

width $3a$ and interconnection portion with a small line width $3b$.), Figs. 23-24.

Annotated Figures 23 and 24 below disclose the dummy via 4c at or near the branch point (e.g., “connection portion R”):

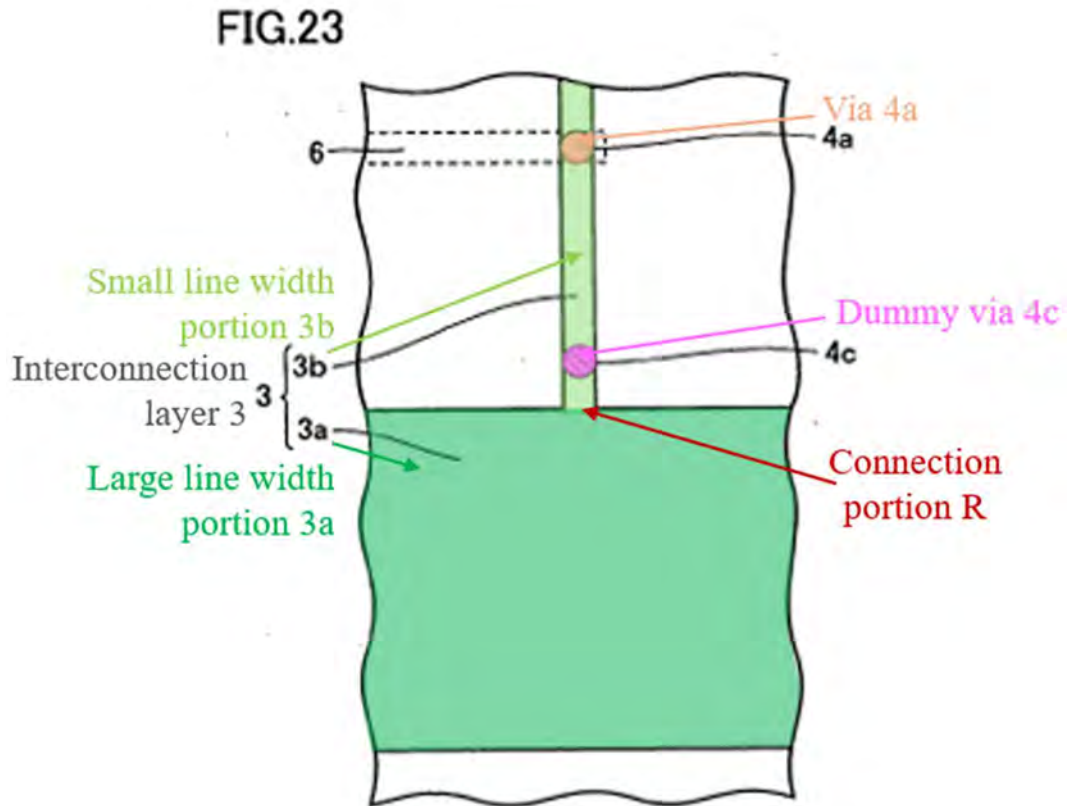
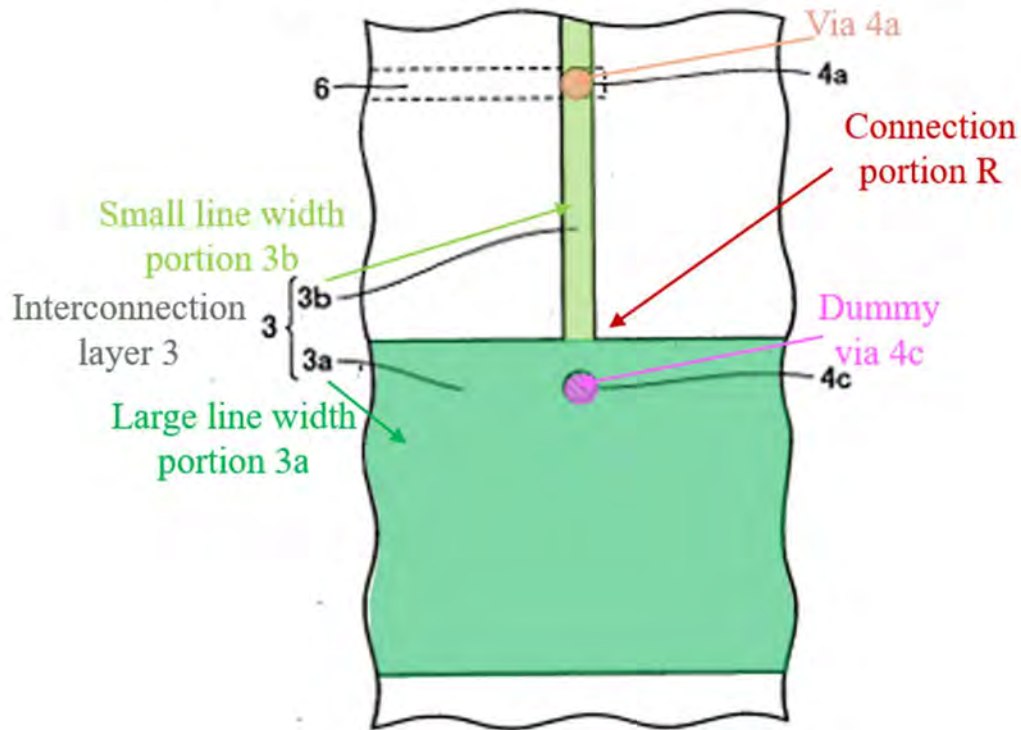


FIG.24



Id., ¶¶[0094]-[0095], [0099].

301. I have explained that it would have been obvious to combine these teachings of Watanabe and Kamoshima in connection with claim 45 above. *Supra*, §X.D.1.(c). That rationale and combination, with the same underlying motivation, applies to claim 46 to render it obvious too. For example, a POSITA would have been motivated to place the dummy via (and thus associated dummy hole) in this location to suppress the concentration of voids in the area under the real via that is due to stress migration.

302. Kamoshima explains a technical reason for placing the dummy via at or near the branch point, teaching that a large number of microvoids from the wide

interconnect (3a) will concentrate under the dummy via (4c) before they can reach the functional via (4a), thereby improving reliability of the device. This establishes the dummy via's role as a "void trap." A POSITA, having already combined Watanabe and Kamoshima to arrive at the structure of claim 45, would then look to Kamoshima for guidance on optimizing the placement of Watanabe's dummy via (dummy plug 34 or 52) and would be directly taught to place it at or near the branch point to achieve this specific void-trapping benefit. A POSITA would have found locating the dummy vias in this location simple and routine as discussed above as it would simply utilize standard processing techniques at the time including those already disclosed in Watanabe, and, thus, would have expected success.

303. Accordingly, when modified to include the interconnect and via configuration of taught in Kamoshima, Watanabe would satisfy claim 46. Thus, a POSITA would have found claim 46 obvious in view of the combination of Kamoshima and Watanabe.

3. Claim 47 – “semiconductor device of claim 45, wherein a width of the second interconnect portion is 0.2 μm or less”

304. Claim 47 recites the “semiconductor device of claim 45, wherein a width of the second interconnect portion is 0.2 μm or less,” which Watanabe and Kamoshima render obvious.

305. Kamoshima expressly describes its interconnection portion 3b as having “a small line width.” TSMC-1009, ¶[0095]; Figs. 23-24. Watanabe discloses via (e.g., plugs 32) simulated to having 0.15 μm diameter, and their underlying interconnects (e.g., wires 36) have the same widths. TSMC-1004, ¶[0083], Figs. 2, 4-5, 9. Watanabe demonstrates the well known nature of interconnect widths under 0.2 μm at the time. Interconnect line widths of “0.2 μm or less” are a routine design parameter for interconnects, as further demonstrated by other art at the time, such as Hasunuma teaching 0.13 μm for interconnect and via widths. TSMC-1005, ¶[0127].

306. Given Watanabe’s teaching of 0.15 μm cylinders and with the same width for its interconnects, it would have been obvious that a POSITA would have implemented the small-line-width portion accordingly. *See also* TSMC-1033, ¶¶[0056]-[0057], [0112]-[0114]. That is, such line widths were well known in the art at the time, and the POSITA would have known to apply such a line width of 0.2 μm or less to the portion of the interconnect with the small width.

307. A POSITA would have had a reasonable expectation of success, because modifying Watanabe’s interconnect shape and having the stated line width was well within the capabilities of a POSITA and indeed already disclosed by Watanabe, and readily achieved with Watanabe’s existing manufacturing process. Indeed, such line widths were well known at the same, such as discussed by Hasunuma. *See* TSMC-1005, ¶[0127] (disclosing wiring layer widths of 0.13 μm).

E. Ground 5: Hasunuma Anticipates Claims 1, 11-15, 17-18, 21-22, 25-26, 28, 32, and 39-40

308. I believe that Hasunuma anticipates claims 1, 11-15, 17-18, 21-22, 25-26, 28, 32, and 39-40 as detailed below. I summarized Hasunuma's teachings previously. *Supra*, §IX.B.

1. Claim 1

a) [1.pre] – “semiconductor device”

309. The preamble of claim 1 calls for a “semiconductor device,” which Hasunuma discloses.

310. Hasunuma's Figure 8 discloses semiconductor device 31, and thus satisfies claim 1's preamble. TSMC-1005, ¶¶Abstract, [0021], [0111].⁶

b) [1.a] – “a semiconductor substrate”

311. Element 1[a] calls for “a semiconductor substrate,” which Hasunuma discloses.

312. Hasunuma's Figure 8 discloses silicon substrate 1 (i.e., a “semiconductor substrate”) for its semiconductor device 31. TSMC-1005, ¶[0090], Figs. 1-8.

⁶ Hasunuma's Figure 14 embodiment meets the challenged claims just like the first embodiment that includes Figure 8. Although my analysis here focuses primarily on Figure 8, the same analysis would apply to Hasunuma's Figure 14.

c) [1.b] – “*a first interconnect formed on the semiconductor substrate*”

313. Element 1[b] calls for “a first interconnect formed on the semiconductor substrate,” which Hasunuma discloses.

314. Hasunuma discloses a first interconnect (e.g., “Cu conductive layer 14” and “barrier layer 9,” hereinafter collectively referred to as “conductive layer 14” or “first interconnect”) formed on the semiconductor substrate. TSMC-1005, ¶¶[0094], [0098], Figs. 3A, 8. Hasunuma describes its interconnects using the term “conductive layer” (e.g., “conductive layer 14,” “conductive layer 26”). A POSITA understood that such conductive layers constitute “interconnects” as those terms are understood in the art because Hasunuma’s conductive layers are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:20-27. Conductive layers/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:36-38.

315. Hasunuma's conductive layer 14, comprising barrier metal film 9 and copper film 12, is formed within an insulating film deposited over substrate 1, as seen in annotated Figure 8 below:

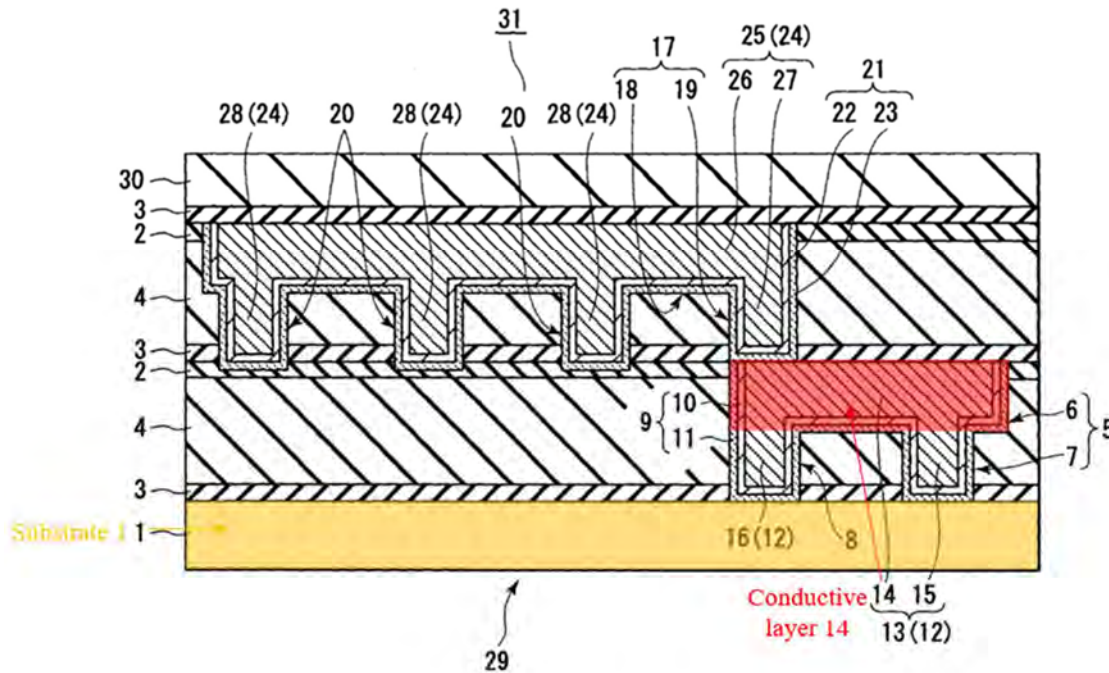


FIG. 8

TSMC-1005, Fig. 3A, 8.

d) [1.c] – “a first insulating film formed on the first interconnect”

316. Element 1[c] calls for “a first insulating film formed on the first interconnect,” which Hasunuma discloses.

317. Hasunuma discloses a second-level insulating film comprising insulating films 3, 4 (a low dielectric constant film), and 2 stacked on the first interconnect, as shown in annotated Figure 8 below:

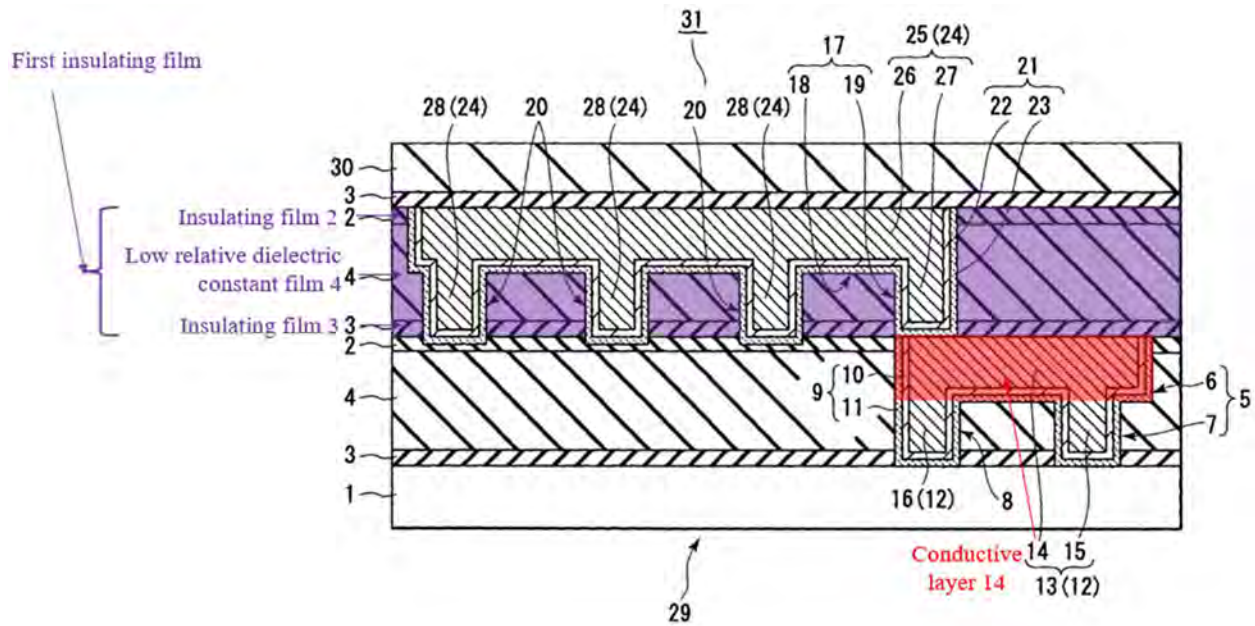


FIG. 8

TSMC-1005, ¶[0100], Figs. 3A-8.

318. As shown in Figure 8 above, Hasunuma discloses depositing an insulating stack over the Cu conductive layer 14, which insulating stack includes an insulating film 3, a low relative dielectric film 4, and an insulating film 2. *Id.*, Figs. 3B, 8, ¶[0100]. Hasunuma explains that “on the SiC film 2 and Cu wiring layer 13 of the first layer, the SiCN film 3, the low relative dielectric constant film 4, and the SiC film (capping layer of a second layer) 2 of the second layer are successively stacked.” *Id.*, ¶[0100]. A POSITA would understand each of SiCN film 3, the low relative dielectric constant film 4, and the SiC film (capping layer of a second layer) 2 (as well as any films that may be substituted for these particular films) to be insulating films. Indeed, Hasunuma expressly refers to films 2, 3, and 4 as

“insulating films.” *See id.*, ¶¶[0090]-[0091] (“as shown in FIG. 1A, on a silicon substrate (semiconductor substrate) 1 in which an active area and underlayer wiring comprising various electronic circuits (not shown) are formed, an insulating film 3, interlayer insulating film (inter-level dielectrics: ILD) 4, and another insulating film 2 are successively stacked. Concretely, first on the surface of the Si substrate 1, for example, a CVD process is used to deposit the insulating film 3 whose Young's modulus is about 30 GPa or more in a film thickness of about 50 nm. This insulating film 3 functions as a first reinforcing film (reinforcing material), and in the present embodiment, for example, an SiCN film is employed as the insulating film 3. Subsequently, on the surface of this SiCN film 3, the CVD process is used to deposit the interlayer insulating film 4....”). A POSITA would understand that the combination of films 3, 4, and 2, or either or both of films 3 and 4, can constitute the “first insulating film.”

e) [1.d] – “*a second interconnect formed on the first insulating film*”

319. Element 1[d] calls for “a second interconnect formed on the first insulating film,” which Hasunuma discloses.

320. Hasunuma discloses a second interconnect, formed by filling recess 18 in the “first insulating film” with barrier metal film 21 and copper film 24 (having

“Cu plating seed layer 24a” and “Cu plating film 24b”) to form, collectively “conductive layer 26,” as seen in annotated Figure 8 below:

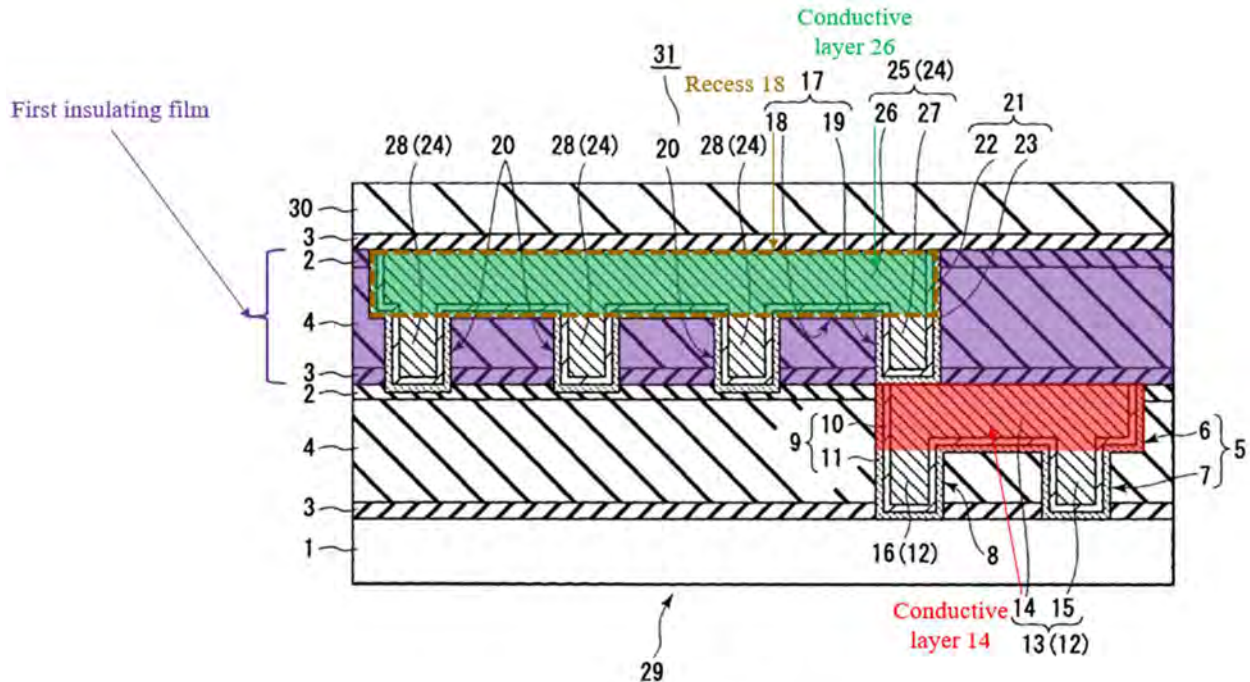


FIG. 8

TSMC-1005, $\{111\}$, $[0101]$, $[0105]$ - $[0108]$, $[0110]$, Figs. 4-8.

321. A POSITA would recognize that the second interconnect is formed on the first insulating film, regardless of whether the first insulating film comprises all of insulating films 3, 4, and 2, or either or both of films 3 and 4. For example, the first insulating film could be considered to be the combination of insulating films 3 and 4 or either film 3 or 4 individually, on each of which the conductive layer 26 is formed.

f) [1.e] – “a via formed through the first insulating film and connecting between the first and second interconnects”

322. Element 1[e] calls for “a via formed through the first insulating film and connecting between the first and second interconnects,” which Hasunuma discloses.

323. Hasunuma discloses a via, formed by filling recess 19 with barrier metal layer 21 and copper film 24 to form, collectively “conductive plug 27,” that extends through the first insulating film from the second interconnect (conductive layer 26) to the first interconnect (conductive layer 14). TSMC-1005, ¶¶[0101]-[0110], Figs. 4-8. This is shown below in annotated Figure 8:

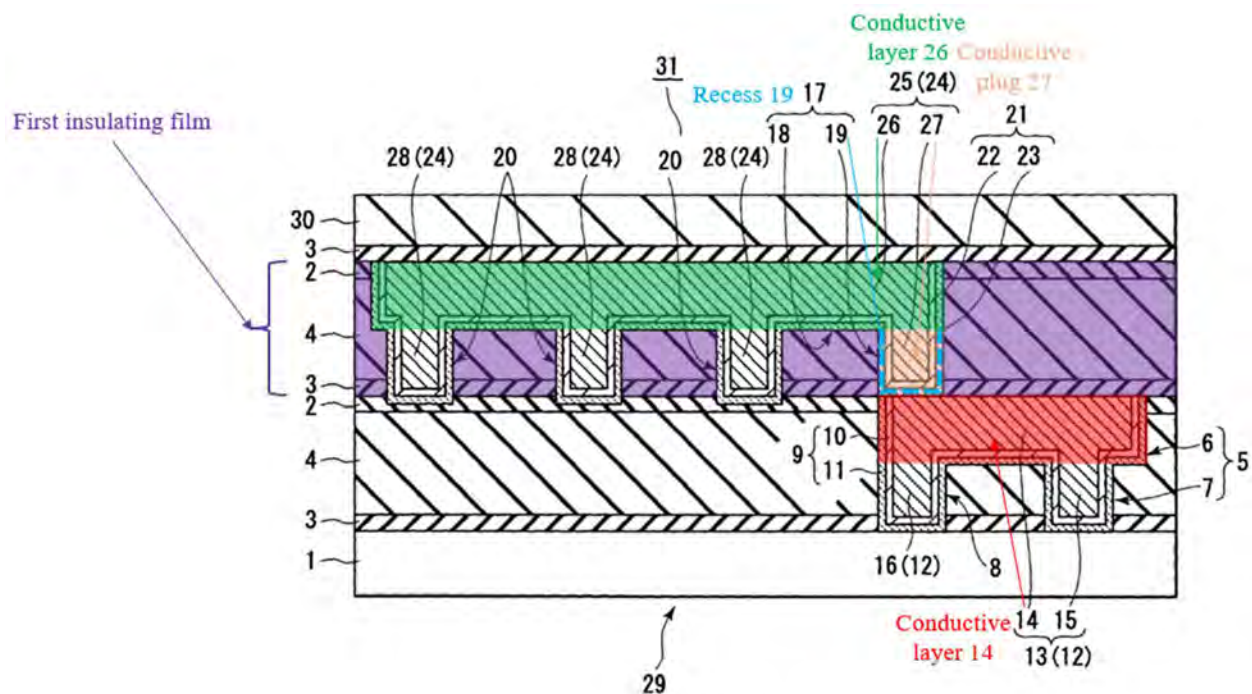


FIG. 8

Id.

324. The conductive plug 27 constitutes the claimed “via.” The conductive plug 27 connects the conductive layer 14 (first interconnect) and the conductive layer 26 (second interconnect). *Id.*, ¶¶[0101], [0110], Fig. 8. Conductive plug 27 connects the first and second interconnects through the first insulating film, regardless of whether insulating films 3, 4, and 2, or either or both of films 3 and 4, constitute the first insulating film.

g) [1.f] – “a dummy via connected to the second interconnect”

325. Element 1[f] calls for “a dummy via connected to the second interconnect,” which Hasunuma discloses.

326. For example, Hasunuma discloses dummy vias (e.g., reinforcing plugs 28) connected to the second interconnect (e.g., conductive layer 26). Hasunuma’s dummy vias/reinforcing plugs 28, formed by filling recesses 20 with barrier metal film 21 and copper film 24 to form, that extend from the second interconnect (conductive layer 26), as seen in annotated Figure 8:

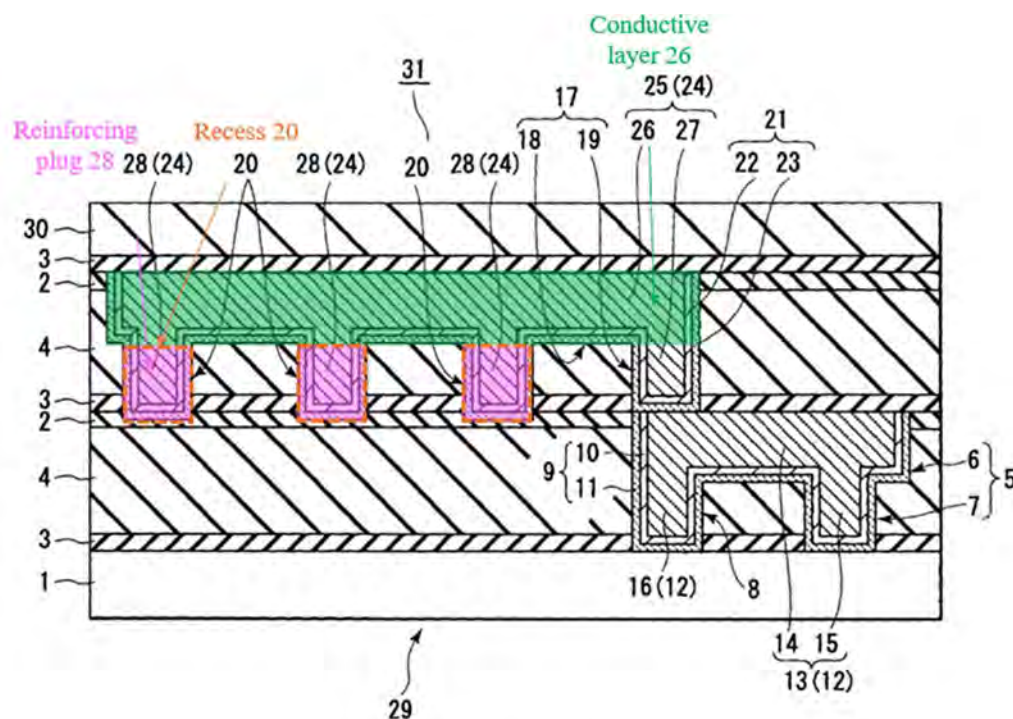


FIG. 8

TSMC-1005, $\{0103\}$ - $\{0108\}$, Figs. 4-8.

327. Regarding its dummy vias/reinforcing plugs 28, Hasunuma discloses forming multiple recesses 20 integrally with the recess 18, and at the same time as recess 19. *Id.*, ¶[0103]. Thus, using a RIE process, recess 20 is formed extending down through SiCN film 3 to expose the surface of SiC film 2 of the insulating stack. *See id.* Hasunuma notes that, with the RIE process used, the bottom portions of the recesses 20 may extend below the SiC film 2. *Id.*, ¶[0104]. Thus, in this embodiment the first reinforcing plugs 28 extend through the SiCN film 3 to contact the SiC film 2 via the barrier metal film 21. *Id.*, ¶[0109].

328. The first reinforcing plugs 28 are connected to the conductive layer 26. *Id.*, Figs 7, 8. Indeed, Hasunuma explains that “the Cu wiring layer 25 of the second layer including the Cu conductive layer 26 and Cu conductive plug (Cu conductive contact plug) 27, and three Cu first reinforcing plugs 28 of the second layer are formed. The Cu wiring layer 25 is a so-called Cu dual damascene wiring.” *Id.*, ¶[0108].

329. Each of the first reinforcing plugs 28 constitutes a “dummy via” as explained further in connection with the next limitation [1.g] below.

h) [1.g] – “*wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough*”

330. Element 1[g] calls for “wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough,” which Hasunuma discloses.

331. Hasunuma’s dummy vias (reinforcing plugs 28) are formed from barrier metal film 21 and copper film 24, which are “conductive films.” TSMC-1005, ¶¶[0103]-[0109]. Thus, a POSITA would recognize that the dummy vias/reinforcing plugs 28 are made of a conductive film.

332. Additionally, a POSITA would recognize that the dummy vias/reinforcing plugs 28 are arranged so as to be incapable of having current flow

therethrough. For example, the lower end of reinforcing plugs 28 are connected only to insulating films 2 and 3, and Hasunuma explicitly describes reinforcing plug 28 as a non-functional “**dummy** plug (sacrifice plug)” which does not function as the wiring. *Id.*, ¶¶[0104] (“[T]here is no problem as long as each the recess 20 has a depth to such an extent that the first reinforcing plug 28 of the second layer formed in the recess 20 **is not electrically connected** to the essential wiring layer (not shown) provided below the plug.”), [0109], Fig. 8; *see also id.* Fig. 14 (locating reinforcing plugs 28 in between and not in contact with conductive layers 14). Hasunuma further describes the Cu first reinforcing plug 28 as a non-functional “dummy plug (sacrifice plug) which does not substantially function as the wiring.” *Id.*, ¶[0109]. Hasunuma also states that “the Cu first reinforcing plug 28 of the second layer may also be referred to as the Cu reinforcing via plug or Cu sacrifice via plug.” *Id.*

333. A POSITA would thus understand that reinforcing plugs 28 do not conduct current as part of active device operation, and that they could be omitted from the structure without any impact on the device’s circuit diagram. Indeed, because they serve no purpose with respect to the current flow associated with any operational circuits of the device, the omission of reinforcing plugs 28 would not impact circuit operation. Thus, the first reinforcing plugs 28 are “incapable of having current flow therethrough” as claimed.

334. As previously outlined, the '623 patent specification states:

A dummy via and a dummy interconnect herein means a pseudo via or a pseudo interconnect which do not constitute a closed circuit in actual use of a device with an interconnection structure including these via and interconnect (i.e., **no current flows therein** during actual use of the device.)

TSMC-1001, 3:14-18 (emphasis added).

335. The '623 patent goes on to explain that:

[N]either the dummy interconnect 102B nor the dummy via 110B constitutes a closed circuit in actual use. That is, even if the dummy interconnect 102B and the dummy via 110B are omitted in the interconnection structure shown in FIG. 2B, a device with this interconnection structure is operable at least immediately after fabrication.

Id., 10:26-32 (emphasis added).

336. As understood by the POSITA, Hasunuma's "first reinforcing plugs 28" do not constitute part of a closed circuit in actual use of the device, i.e., no current flows through the first reinforcing plugs 28 during actual use of the device. As seen in Figures 7-8, these "first reinforcing plugs 28" are only connected at their upper end to an active element (i.e., "conductive layer 26"), while the other end is not connected to another active circuit element. TSMC-1005, Figs. 7-8. A POSITA

would recognize that no current flows through the first reinforcing plugs 28 due to this lack of connection to a second active circuit element.

337. Also, Hasunuma's device would still be operable if first reinforcing plugs 28 were omitted because they do not carry current/signals as part of a closed circuit during actual use of the device. On the other hand, current flows occur between the conductive layer 14 and conductive layer 26 through conductive plug 27, which do constitute a closed circuit for operation of the device. A POSITA would readily understand the similarity between this configuration and that of interconnect 111 and via 110A (and corresponding recess in which via 110A is formed) in the '623 patent. See TSMC-1001, 10:10-48, Figs. 2A-2B.

i) [1.h]/[1.i] – *“the second interconnect and the via form a dual damascene structure”/“the second interconnect and the dummy via from a dual damascene structure”*

338. Element [1.h] calls for “the second interconnect and the via form a dual damascene structure” and element [1.i] calls for “the second interconnect and the dummy via from a dual damascene structure,” both of which Hasunuma discloses.

339. Hasunuma states that wiring layer 25 (which comprises the second interconnect (conductive layer 26) and via (conductive plug 27)) is “formed in the dual damascene structure.” TSMC-1005, ¶¶[0101], [0108], Fig. 8. Hasunuma

similarly states that its second interconnect (conductive layer 26) and dummy vias (reinforcing plugs 28) are “formed in the dual damascene structure.” *Id.*, ¶[0103].

340. This is consistent with Hasunuma forming the second interconnect, via, and dummy vias integrally when recesses 18-20 are simultaneously filled with barrier metal film 21 and copper film 24. *Id.*, ¶¶[0101], [0103], [0105]-[0109], Figs. 4-8. Thus, Hasunuma’s second interconnect (conductive layer 26) and via (conductive plug 27) forms a dual damascene structure. Additionally, Hasunuma’s second interconnect (conductive layer 26) and the dummy vias (reinforcing plugs 28). This is shown in annotated Figure 8 below:

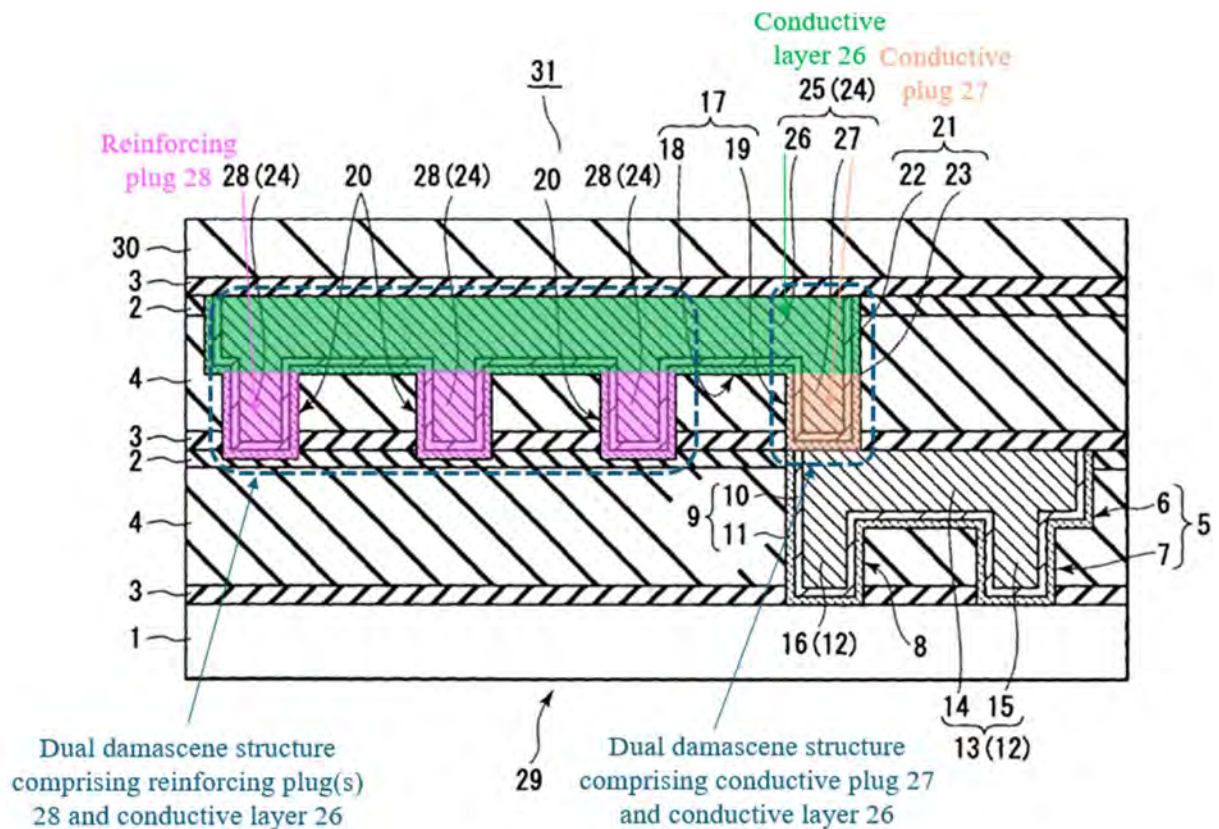


FIG. 8

That Hasunuma's second interconnect (conductive layer 26) and via (conductive plug 27) form a dual damascene structure, as does Hasunuma's second interconnect and its dummy vias (reinforcing plugs 28), is further evidenced by Figure 8 itself. Specifically, a POSITA would appreciate that Hasunuma's barrier metal film 21 conformally coats the outer sides of the conductive film 26, the plug 27 and the reinforcing plugs 28, all as one single, continuous layer. Within this conformal barrier layer coating, copper film 24 is added to fill the recesses for the vias and dummy vias and trench for the interconnect to form the vias, dummy vias, and interconnect from a single, unitary copper structure. A POSITA would have recognized this configuration shown in Figure 8 as a dual-damascene structure, especially in conjunction with Hasunuma's description (*e.g.*, *id.*, ¶¶[0105]-[0108], Figs. 4-7.

2. Claim 11 – “semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film”

341. Claim 11 recites the “semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO₂ film,” which Hasunuma discloses.

342. Hasunuma's first insulating film (*e.g.*, combination of layers 2, 3, 4) has a multilayer structure including a SiN film and a SiO₂ film, thus satisfying claim

11. TSMC-1005, ¶[0299] (“instead of the SiC film 2, an SiO₂ film may also be used”; “instead of the SiCN film 3, an SiN film may also be used”).

343. Hasunuma explicitly teaches that the materials for layers 2, 3, 4 can be substituted. *See id.*, ¶¶[0091], [0293], [0299]. Specifically, Hasunuma states that “instead of the SiC film 2, an SiO₂ film may also be used” and “instead of the SiCN film 3, an SiN film may also be used.” *Id.*, ¶[0299]. Hasunuma also discloses those substitutions in paragraph [0293], teaching that for the films having a Young’s modulus of 30 GPa or more, such as the SiCN film or SiC film, other materials can be used including SiN and SiO₂. *Id.*, ¶[0293]. Those films having a Young’s modulus of 30 GPa or more are the SiCN film 3 and the SiC film 2, which are described by Hasunuma as having the Young’s modulus of 30 GPa or more. *Id.*, ¶¶[0091]-[0092], [0100]. Applying the explicitly taught substitutions, the second-level insulating stack comprising layers 2, 4 and 3 (the “first insulating film” (*supra*, X.E.1.(d))) would comprise a SiN film (substituted for SiCN film 3) and an SiO₂ film (substituted for SiC film 2). *Id.*, ¶¶[0293], [0299]. This resulting multilayer stack serving as the claimed “first insulating film” thus includes both a SiN film and a SiO₂ film, thereby satisfying claim 11.

3. Claim 12 – “*semiconductor device of claim 1, wherein the second interconnect includes a first barrier film and a first conductive film*”

344. Claim 12 recites the “semiconductor device of claim 1, wherein the second interconnect includes a first barrier film and a first conductive film,” which Hasunuma discloses.

345. Hasunuma forms its second interconnect (conductive layer 26) by first lining recess 18 with barrier metal film 21, i.e., “a first barrier film.” TSMC-1005, ¶¶[0105]-[0108], Figs. 4-5. Hasunuma then fills the lined recess 18 with copper film 24 (i.e., “a first conductive film”) to form conductive layer 26. *Id.*, ¶¶[0106]-[0108], Figs. 5-8. Thus, Hasunuma’s second interconnect includes a first barrier film (barrier metal film 21) and a first conductive film (copper film 24).

4. Claim 13 – “*semiconductor device of claim 12, wherein the first conductive film includes copper*”

346. Claim 13 recites the “semiconductor device of claim 12, wherein the first conductive film includes copper,” which Hasunuma discloses. As noted for claim 12 above, the “first conductive film” is the copper film 24, which obviously includes copper. TSMC-1005, ¶¶[0106]-[0108].

5. Claim 14 – “*semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode*”

347. Claim 14 recites the “semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode,” which Hasunuma discloses.

348. A POSITA would understand that each of Hasunuma’s first and second interconnects (e.g., “conductive layer 14” and “conductive layer 26”) is connected to another element (e.g., “contact plug 15,” “electronic circuit on substrate 1,” and other active components of the active circuit formed together with the first and second interconnects) or an external electrode. TSMC-1005, ¶[0092]. Together “wiring layer 13” (which includes first interconnect/“conductive layer 14”) and “wiring layer 25” (which includes second interconnect/“conductive layer 26”) form an “effective wiring area 29” that “actually functions as the wiring” of Hasunuma’s device. *Id.*, ¶[0110]. A POSITA understood that the wiring in such a semiconductor device includes a multitude of circuit elements connected together to form the wiring/circuit, including transistors or other devices on the substrate and external electrodes or connections for facilitating electrical connection of the wiring/circuit to an external component.

349. Hasunuma's first interconnect ("conductive layer 14") is indeed formed on a semiconductor (silicon) substrate that includes active electronic circuits, e.g., where conductive plug 15 of the first interconnect secures "the conduction to the electronic circuit formed in the Si substrate 1." *See id.*, ¶¶[0090], [0092]-[0093] ("It is to be noted that the conductive plug 15 of the first layer is formed as the contact plug 15 for securing the conduction to the electronic circuit formed in the Si substrate 1.>").

350. Hasunuma's second interconnect ("conductive layer 26") is connected to the first interconnect by the via/conductive plug 27, and thus to the "electronic circuits." Furthermore, a POSITA would recognize that Hasunuma's second interconnect ("conductive layer 26") is part of a functional multi-level wiring scheme that creates a circuit by virtue of a connection to other elements (e.g., other wiring layers, vias, or circuit components) or external electrodes (e.g., electrodes connected/bonded to Al pad 136). *Id.*, ¶¶[0089], [0128], [0209]-[0212], [0298], [0005], Fig. 21A. In addition, a POSITA understood that, in a semiconductor device, it is necessary that such functional wiring layers, such as Hasunuma's first and second interconnects, be connected to other circuit elements and/or to external electrodes for the device to operate. Indeed, without connections to other circuit elements, no circuit is created and the active interconnects would serve no purpose and the overall device itself would be useless.

351. Thus, Hasunuma satisfies claim 14.

6. Claim 15

a) [15.a] – “*semiconductor device of claim 1, wherein the first interconnect, the second interconnect and the via constitute part of a closed circuit*”

352. Element 15[a] recites the “semiconductor device of claim 1, wherein the first interconnect, the second interconnect and the via constitute part of a closed circuit,” which Hasunuma discloses.

353. Hasunuma’s first and second interconnects (conductive layers 14 and 26) are connected to each other by via/conductive plug 27 and to other active elements within the semiconductor device such as “electronic circuits.” TSMC-1005, ¶¶[0092]-[0093]. A POSITA would have therefore understood that the structure comprising the via and the first and second interconnects constitutes part of a functional, closed electrical circuit in an operating semiconductor device. *Id.*

354. Hasunuma describes conductive layer 14 as follows: “That is, the conductive layer 14 and conductive plug 15 comprise a wiring layer (effective wiring layer) 13 which is actually energized to function as a primary wiring.” *Id.*, ¶[0092]. Hasunuma further describes conductive layer 26 as also functioning as a primary wiring: “In the same manner as the conductive layer 14 and conductive plug 15 of the first layer, the conductive plug 27 of the second layer is formed to be electrically

connected to the conductive layer 26 of the second layer, and comprises the conduction path to be actually energized together with the conductive layer 26.” *Id.*, ¶[0101]. Hasunuma explains that the conductive plug 15 is for conduction (i.e., electrical connection) to the electronic circuit. *Id.*, ¶¶[0092]-[0093].

355. Moreover, Hasunuma explains that the recess 19 is formed “to expose the surface of the wiring layer 13 of the first layer so that the conduction of the via plug 27 to the wiring layer 13 of the first layer.” *Id.*, ¶[0102]. The conductive plug 27 is integrally formed with the conductive layer 26 (*see id.*, ¶[0101]), and connected to the conductive layer 14, such as shown in Figs. 7-8.

356. In short, the conductive layer 14, the conductive layer 26, and the conductive plug 27, during actual device use, form a closed circuit.

b) [15.b] – “*the dummy via does not constitute a closed circuit*”

357. Element 15[b] calls for “the dummy via does not constitute a closed circuit,” which Hasunuma discloses.

358. Hasunuma describes dummy via (reinforcing plug 28) as a non-functional “dummy plug (sacrifice plug),” which does not function as the wiring. TSMC-1005, ¶[0109], Fig. 8; *see also supra*, §X.E.1.(h). The top of reinforcing plug 28 connects to conductive layer 26 (the claimed “second interconnect”), but its bottom end terminates in an insulating material (e.g., film 2), without connecting to

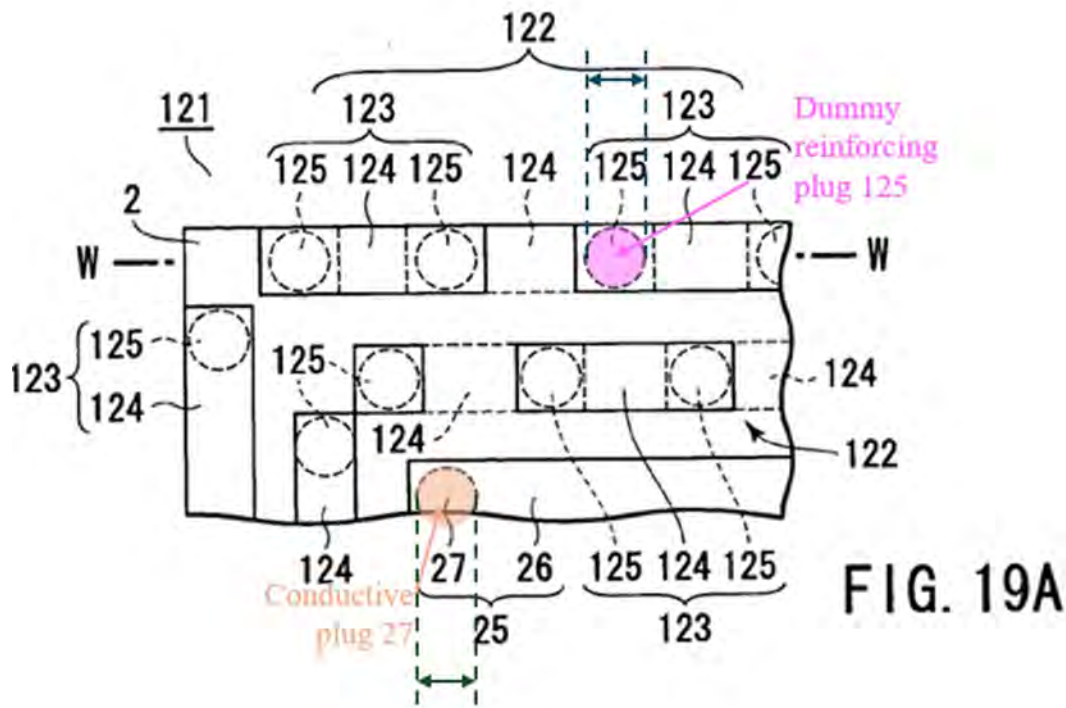
an underlying functional conductive path to complete a circuit. *Id.*, ¶¶[0104], [0109], Fig. 8. Because it does not function as wiring and does not complete a path for current flow between two distinct active points in an operational circuit, Hasunuma's dummy via does not constitute part of a closed circuit.

359. Accordingly, Hasunuma discloses claim 15.

7. Claim 17 – “*semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view*”

360. Claim 17 recites the “semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view,” which Hasunuma discloses.

361. Hasunuma discloses circular vias (in plan view) in various figures, including Figure 19A as annotated below:



TSMC-1005, Fig. 19A; *see also id.* ¶[0200], Figs. 22A-22C, 24A-27C.

362. Additionally, when describing tests performed on such structures, Hasunuma discusses the “diameter” of both conductive and reinforcing plugs, further demonstrating Hasunuma’s disclosure of a circular shape for both its vias and dummy vias. *See id.*, ¶¶[0127] (“[E]ach diameter of the Cu conductive contact plug 15, Cu reinforcing contact plug 16, Cu conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 μm .”), [0133], [0201], [0216], [0010]. A POSITA would have understood that describing the vias’ “diameter” in this context discloses a circular shape for both conductive plug 27 and reinforcing plug 28 (i.e., via and dummy via), since “diameter” is the standard dimensional term for circular features.

363. The express disclosure of circular vias in, *inter alia*, Figure 19A, reinforces that Hasunuma's reference to the "diameters" of its vias and dummy vias discloses that these structures likewise have a substantially circular cross section in plan view, just as shown in Figures 19A, 22A, etc. In view of the foregoing, a POSITA would have readily understood Hasunuma to disclose substantially circular-shaped vias for any of its vias or dummy vias.

364. Accordingly, Hasunuma discloses claim 17.

8. Claim 18 – “semiconductor device of claim 17, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other”

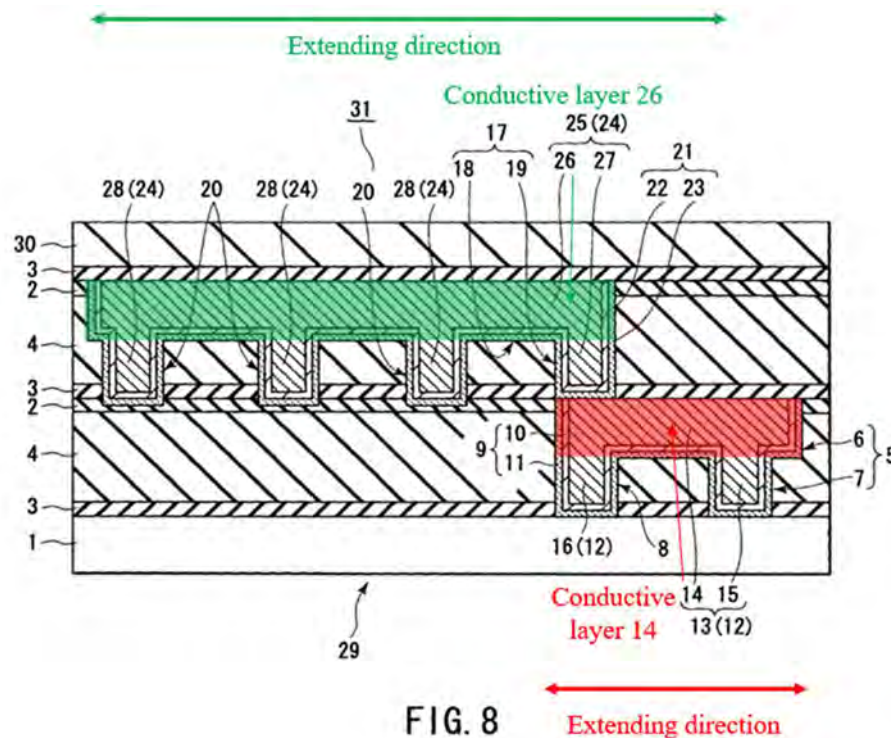
365. Claim 18 recites the “semiconductor device of claim 17, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other,” which Hasunuma discloses. Claim 17 is addressed immediately above.

366. As noted for claim 17, Hasunuma expressly assigns the same dimension for the diameter of both its vias (conductive plugs 27) and its dummy vias (reinforcing plugs 28), stating: “each diameter of...conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 μm .” TSMC-1005, ¶[0127], Figs. 8-9. Therefore, Hasunuma discloses circular vias and dummy vias having a substantially equal/same diameter.

9. Claim 21 – “semiconductor device of claim 1, wherein the first interconnect and the second interconnect extend in a same direction”

367. Claim 21 recites the “semiconductor device of claim 1, wherein the first interconnect and the second interconnect extend in a same direction,” which Hasunuma discloses.

368. A POSITA would understand that Hasunuma’s first interconnect (e.g., “conductive layer 14”) and second interconnect (e.g., “conductive layer 26”) each extend in multiple directions that are the same. For example, in Figure 8, Hasunuma’s first interconnect (e.g., “conductive layer 14”) extends in a same lengthwise direction (e.g., across the page) as Hasunuma’s second interconnect (e.g., “conductive layer 26”), as shown in annotated Figure 8:



TSMC-1005, Fig. 8.

369. A POSITA would further recognize and discern between these lengthwise and widthwise directions based on the description in Hasunuma's specification of the dimensions of the vias and conductive layers as well as Hasunuma's figures. For example, both conductive layers 14 and 26 (which are part of Cu wiring layers 13, 25) are described as having a same width as conductive plug 27 and reinforcing plugs 28. *See id.*, ¶[0127] ("Additionally, each diameter of the Cu conductive contact plug 15, Cu reinforcing contact plug 16, Cu conductive via plug 27, and Cu reinforcing via plug 28 was formed in about 0.13 um.... Furthermore, each of the Cu wiring layers 13, 25 was formed as a single wiring. In this case, a wiring width of a wiring pattern of each of the Cu wiring layers 13, 25 was set to about 0.13 um...."). This further demonstrates to a POSITA that the cross-sectional views in Figure 8 of Hasunuma disclose a length of both conductive layer 26 and conductive layer 14, because the distances of these layers across the page are both different from each other, and different from and much greater than the width of the individual plugs 27 and 28 (which are described as having a same width). This confirms that Figure 8's cross section must be showing the lengthwise direction of conductive layers 14 and 26, and that these lengthwise directions extend in the same direction across the page.

370. Additionally, Figure 14 discloses multiple first conductive layers 14, one extending in a lengthwise direction across the page and the other three extending in a lengthwise direction into/out of the page:

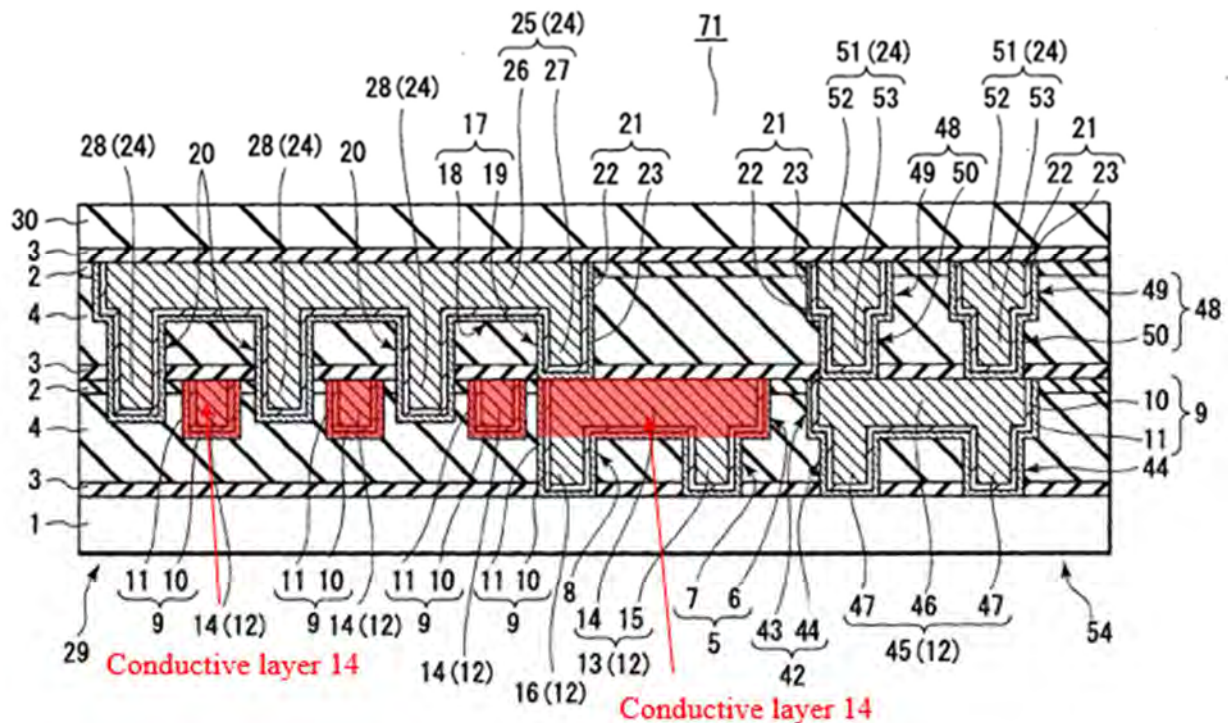


FIG. 14

371. As shown in Figure 14, the three conductive layers 14 on the left side of Figure 14 extend a same distance across the page as the reinforcing plugs 28 and conductive plug 27, and thus a POSITA would recognize that dimension of the conductive layers 14 to be the width (since it is approximately equal to that of reinforcing plugs 28 and conductive plug 27 just as called for in paragraph 127). In contrast, the conductive layer 14 on the right would be recognized by a POSITA to

extend in a lengthwise direction across the page given its much greater extent across the page as compared to that of the other conductive layers 14 and the conductive plug 27 and reinforcing plugs 28.

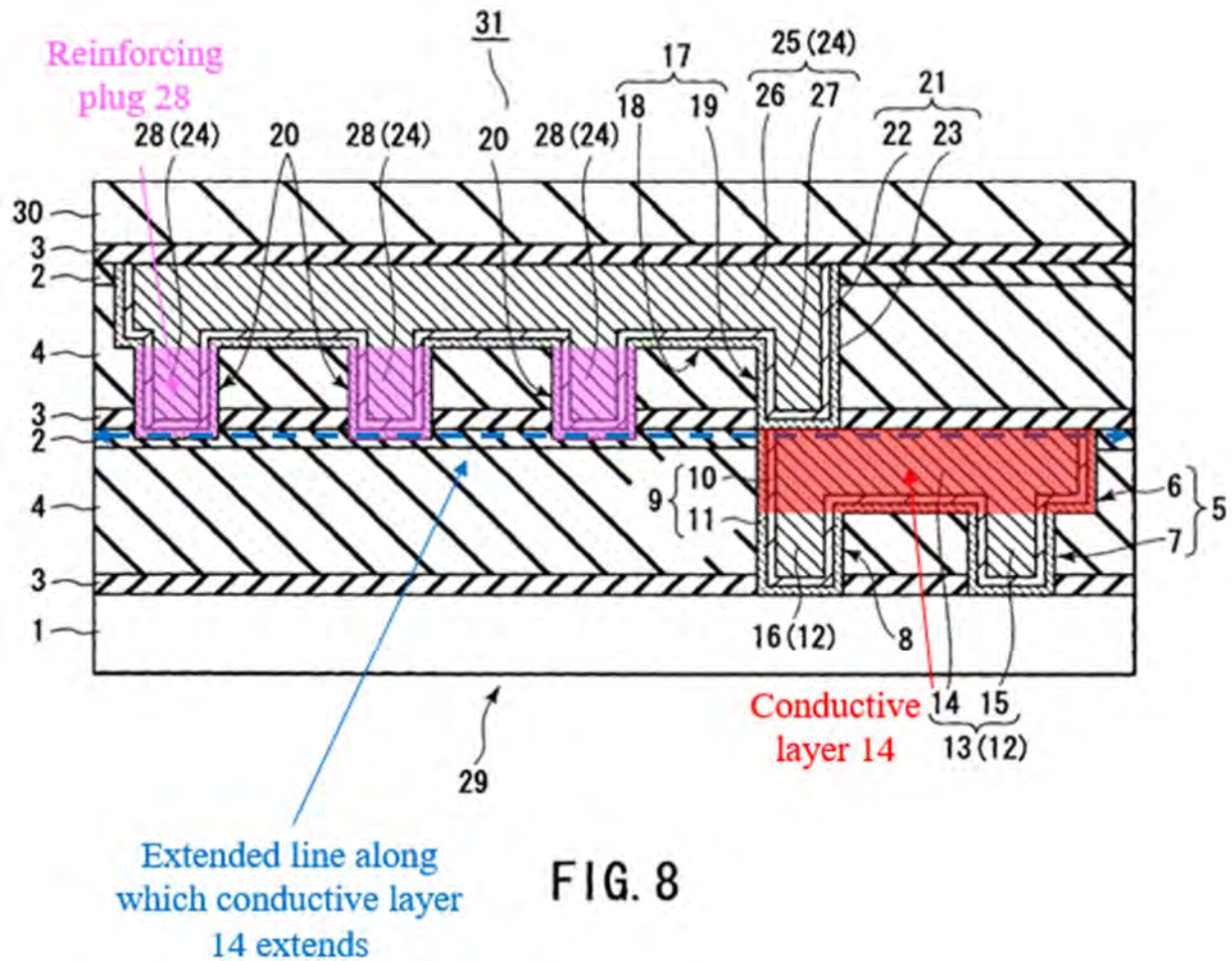
372. Additionally, a POSITA would understand that both interconnects extend in a same widthwise direction into/out of the page.

373. Accordingly, Hasunuma satisfies claim 21.

10. Claim 22 – “*semiconductor device of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends*”

374. Claim 22 recites the “semiconductor device of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends,” which Hasunuma discloses.

375. In Hasunuma’s cross-sectional views, such as Figure 8, the first interconnect (conductive layer 14) is disclosed as a generally horizontal layer, shown to extend across the page (e.g., from right to left). Hasunuma’s dummy via (e.g., “reinforcing plug 28”) is provided on an extended line along which the first interconnect (e.g., “conductive layer 14”) extends. This is shown below in annotated Figure 8:



TSMC-1005, Fig. 8.

376. Accordingly, Hasunuma satisfies claim 22.

11. Claim 25 – “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less”

377. Claim 25 recites the “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less,” which Hasunuma discloses.

378. Hasunuma's Figure 9⁷ and Tables 1-3 provide values for "plug interval" between conductive plug 27 and an adjacent reinforcing plug 28, labeled as "B" in Figure 9:

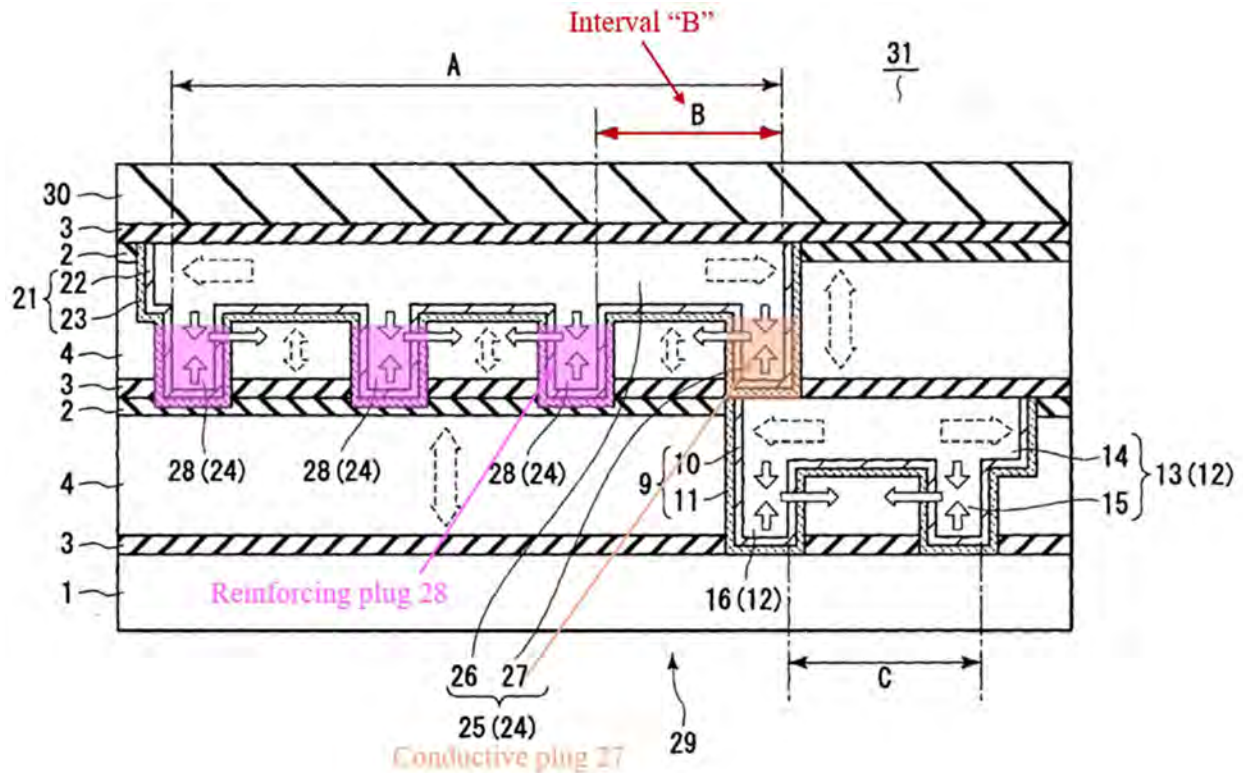


FIG. 9

TSMC-1005, ¶¶[0127], [0130]-[0137].

379. As seen from Figure 9, interval "B" is portrayed as the right edge-to-right edge spacing, which is effectively equal to the center-to-center spacing between

⁷ A POSITA would recognize that Hasunuma's Figure 9 discloses the same device as in Hasunuma's first embodiment and Figure 8, but adds illustrations of various stresses (e.g., thermal stresses) within the device. TSMC-1005, ¶¶[0022], [0112].

the via and dummy via. As clearly seen from Figure 9, this right edge-to-right edge or center-to-center spacing is larger than the adjacent edge-to-adjacent edge spacing between the via and dummy via (e.g., the spacing between the right edge of reinforcing plug 28 and the adjacent left edge of conductive plug 27).

380. Hasunuma discloses a preferred interval B of less than 1 μm or of less than 5 μm or less, and tested intervals up to 20 μm , each of which is less than 25 μm for the larger right edge-to-right edge or center-to-center spacing. *Id.*, ¶¶[0137] (“Cu conductive plugs 15, 27 and Cu reinforcing plugs 16, 28 are preferably provided so that the plug interval B, C is about 1 μm or less”), [0159] (“[I]t has been found that the plug interval B provided in the Cu wiring layer 25 is preferably about 5 μm or less”), Tables 1-3 (disclosing plug intervals of 0.26 μm , 0.39 μm , etc.). As noted above, the spacing distance between the right side of the reinforcing plug 28 annotated above in Figure 9 and the left side of the adjacent conductive plug 27 is less than the plug interval B between those same plugs. Since B represents an even greater distance than the claimed right edge-to-left edge spacing between the via (conductive plug 27) and dummy via (reinforcing plug 28), this teaching for B satisfies the claim limitation of 25 μm or less.

381. Accordingly, Hasunuma satisfies claim 25.

12. Claim 26 – “*semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 1 μm or less*”

382. Claim 26 recites the “semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 1 μm or less,” which Hasunuma discloses.

383. Hasunuma’s Figure 9 and Tables 1-3 provide values for the “Plug interval” between conductive plug 27 and an adjacent reinforcing plug 28, labeled as “B” and seen in annotated Figure 9:

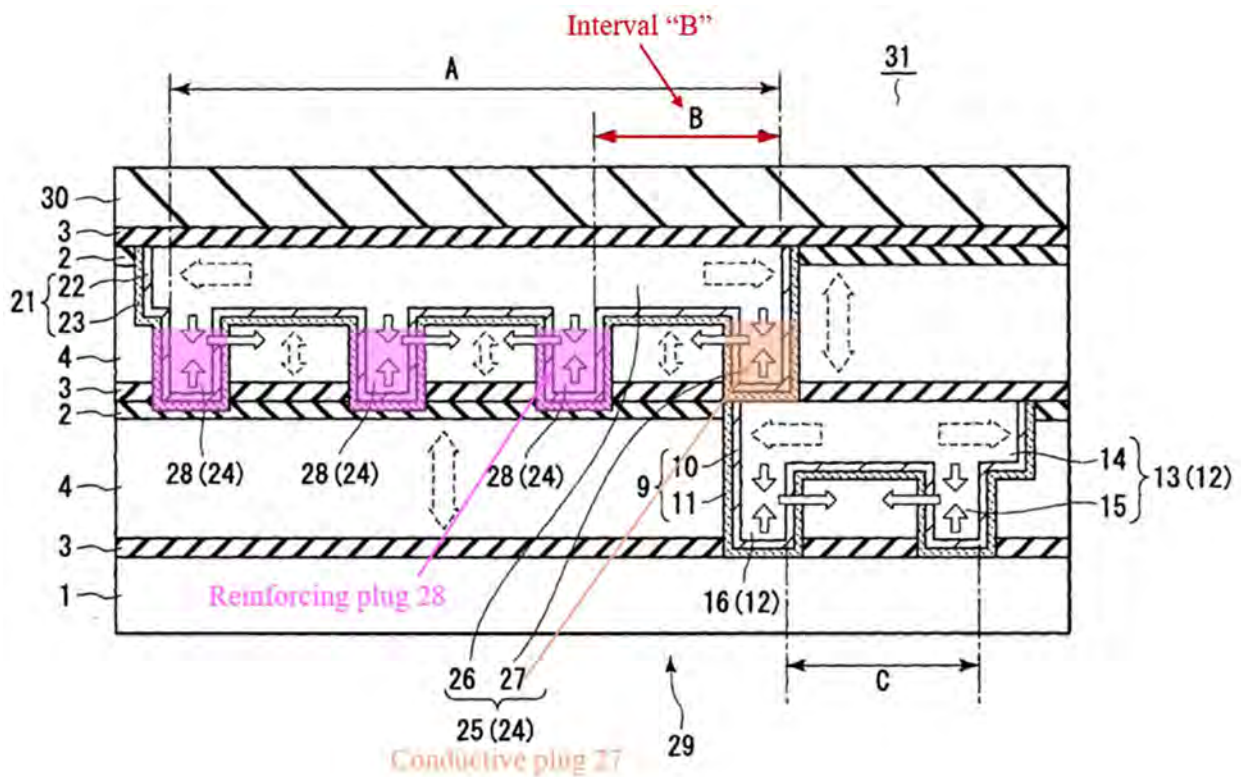


FIG. 9

TSMC-1005, $\text{P}^{\text{II}}[0127]$, $[0130]$ - $[0137]$, Fig. 9.

384. As seen from Figure 9, interval “B” is portrayed as the right edge-to-right edge spacing, which is effectively equal to the center-to-center spacing between the via and dummy via. As clearly seen from Figure 9, this right edge-to-right edge or center-to-center spacing is larger than the adjacent edge-to-adjacent edge spacing between the via and dummy via (e.g., the spacing between the right edge of reinforcing plug 28 and the adjacent left edge of conductive plug 27).

385. Hasunuma teaches that a preferred interval B is about **1 μm or less**, and shows such values in Tables 1-3. *Id.*, ¶[0137], Tables 1-3; *see also supra*, §X.E.11. As noted above, the spacing distance between the right side of the reinforcing plug 28 annotated above in Figure 9 and the left side of the adjacent conductive plug 27 is less than the plug interval B between those same plugs. Since B represents an even greater distance than the claimed right edge-to-left edge spacing between the via (conductive plug 27) and dummy via (reinforcing plug 28), this teaching for B satisfies the claim limitation of 1 μm or less. *Id.*

13. Claim 28 – “semiconductor device of claim 1, wherein the dummy via is provided in plural”

386. Claim 28 recites the “semiconductor device of claim 1, wherein the dummy via is provided in plural,” which Hasunuma discloses.

387. The “dummy vias” in Hasunuma are the Cu first reinforcing plugs 28. *Supra*, §X.E.1.(g). Hasunuma consistently shows and describes using multiple Cu

first reinforcing plugs 28. TSMC-1005, ¶¶[0103], [0137], Fig. 8. For example, Figure 8 discloses three separate dummy vias (reinforcing plugs 28). A POSITA would further recognize Hasunuma as teaching other plural numbers of reinforcing plugs 28 could be included. Therefore, Hasunuma consistently shows and describes the use of a plurality of dummy vias (reinforcing plugs 28), with Figure 8 disclosing three such dummy vias, as just one example. Hasunuma thus satisfies claim 28.

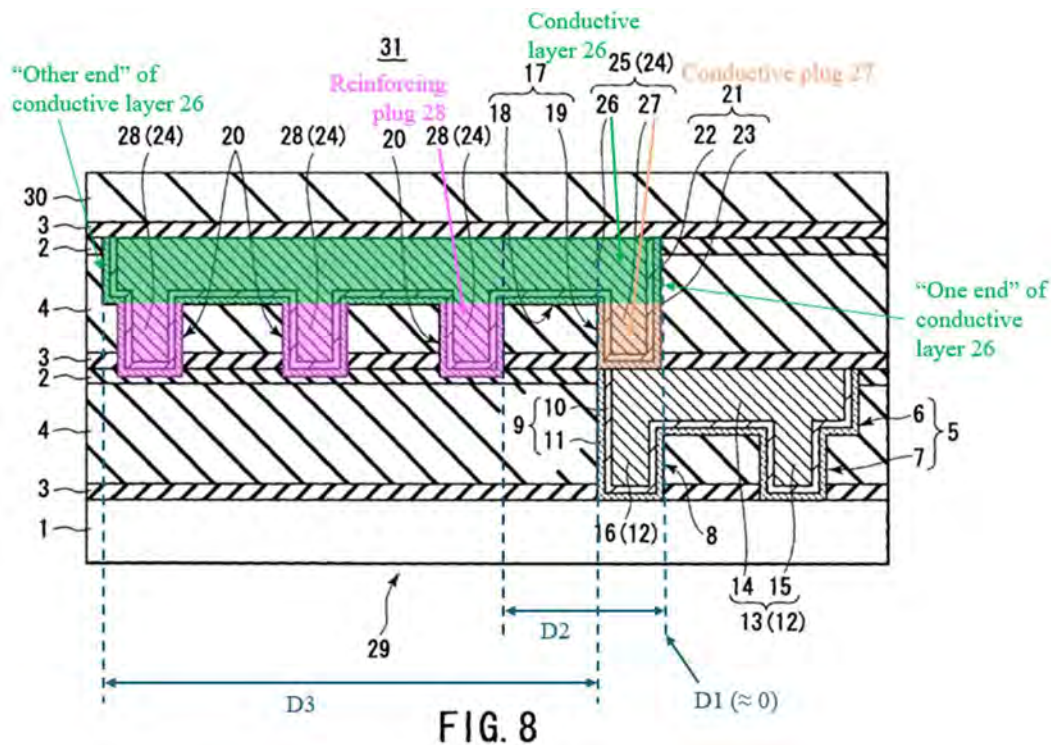
14. Claim 32 – “semiconductor device of claim 1, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect and shorter than a distance between the via and the other end of the second interconnect”

388. Claim 32 recites the “semiconductor device of claim 1, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect and shorter than a distance between the via and the other end of the second interconnect,” which Hasunuma discloses.

389. As discussed above, and throughout my declaration, Hasunuma’s functional conductive plug (e.g., plug 27 in Fig. 8) constitutes the claimed “via,” its first reinforcing plug (e.g., reinforcing plug 28 in Fig. 8) constitutes the claimed

“dummy via,” and its upper conductive layer (e.g., 26 in Fig. 8) constitutes the claimed “second interconnect.” See TSMC-1005, Fig. 8; *supra*, §§X.E.1.(f)-(g).

390. Hasunuma teaches that the via (conductive plug 27) is preferably provided at an end-most portion of the wiring layer, as illustrated in Figure 8, where the via is shown at one end (e.g., the rightmost end in the cross-section of Figure 8) of the second interconnect (conductive layer 26). *Id.*, ¶[0171], Fig. 8. Using the same definitions as previously described (*supra*, §X.A.16), the dummy vias (reinforcing plugs 28) are located further along the second interconnect from that same end (e.g., further to the left in the cross-section), as seen in annotated Figure 8 below:



Id., Fig. 8.

391. In this configuration, the distance D1 between the via (conductive plug 27) and the proximate end of the second interconnect is minimal (essentially zero). Given that distance D1 is essentially zero, it is shown in annotated Figure 8 above with only an arrow pointing to the right edge of conductive plug 27. This minimal distance D1 is shorter than the distance D2 from any dummy via to that same proximate end. The distance D2 is shown above in annotated Figure 8 extending from the right side of conductive plug 27 to the right side of the nearest reinforcing plug 28. Furthermore, this minimal distance D1 from the via (conductive plug 27) to the proximate end is also shorter than the distance D3 from the via to the opposite end of the second interconnect (e.g., the left end of conductive layer 26 as shown above in annotated Figure 8). Thus, Hasunuma satisfies claim 32.

15. Claim 39 – “*semiconductor device of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film*”

392. Claim 39 recites the “semiconductor device of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film,” which Hasunuma discloses.

393. Hasunuma’s dummy via (e.g., “reinforcing plug 28”) and second interconnect (e.g., “conductive layer 26”) are both made from the same conductive film (e.g., “Cu film 24” and/or “barrier metal film 21”):

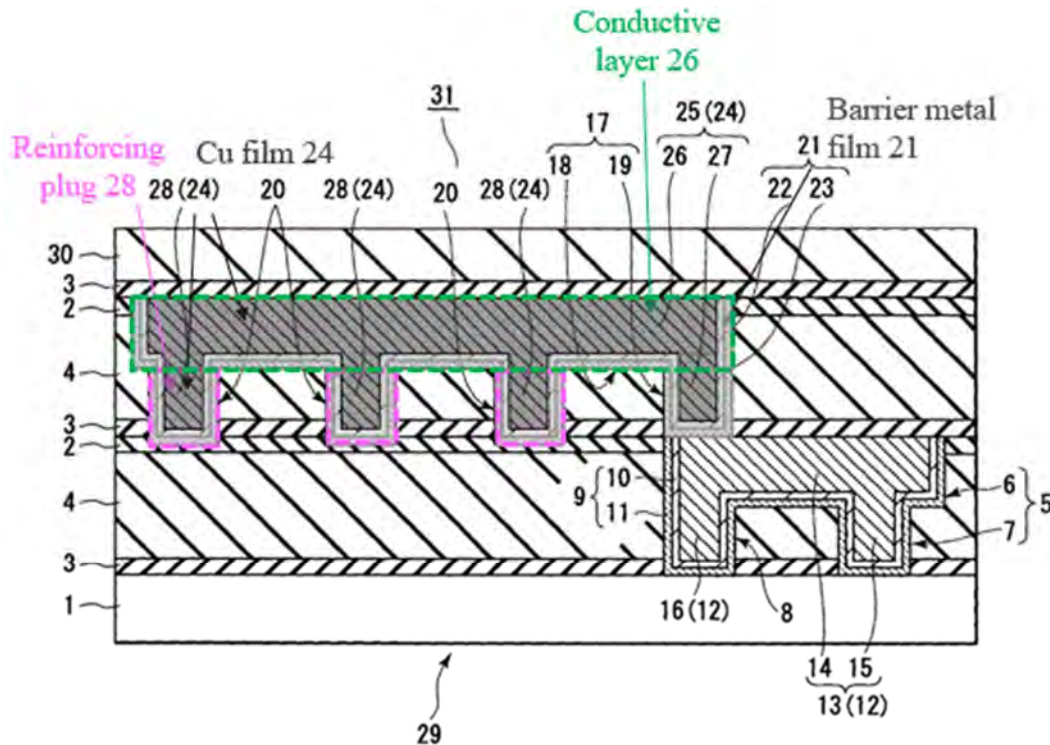


FIG. 8

TSMC-1005, ¶¶[0105]-[0108], Fig. 8.

394. Indeed, a POSITA would understand that Hasunuma's dual damascene simultaneously process for forming its interconnects and vias forms the dummy via (Cu reinforcing plug 28) and the second interconnect (Cu conductive layer 26) by filling integrally formed recesses (recess for the first reinforcing plug 20, recess for the conductive layer 18) first with the same barrier metal film 21 and then with the same bulk Cu film 24. *See id.*, FIGS. 4-7, ¶¶[0105]-[0108]. Thus, both the dummy via and the second interconnect are made of a same conductive film, namely the barrier metal film 21 and copper film 24.

395. Accordingly, Hasunuma satisfies claim 39.

16. Claim 40 – “semiconductor device of claim 1, wherein the dummy via and the second interconnect include a Cu film”

396. Claim 40 recites the “semiconductor device of claim 1, wherein the dummy via and the second interconnect include a Cu film,” which Hasunuma discloses.

397. Hasunuma identifies the Cu film 24, which forms both the dummy via (Cu first reinforcing plug 28) and the second interconnect (Cu conductive layer 26), as Copper (Cu). TSMC-1005, ¶¶[0106], [0107], Fig. 8. Therefore, Hasunuma’s dummy via and second interconnect both include copper film 24. *Id.*; *see also supra*, §X.E.15.

F. Ground 6: Claims 2 and 8 Are Obvious Over Hasunuma and Kurashima

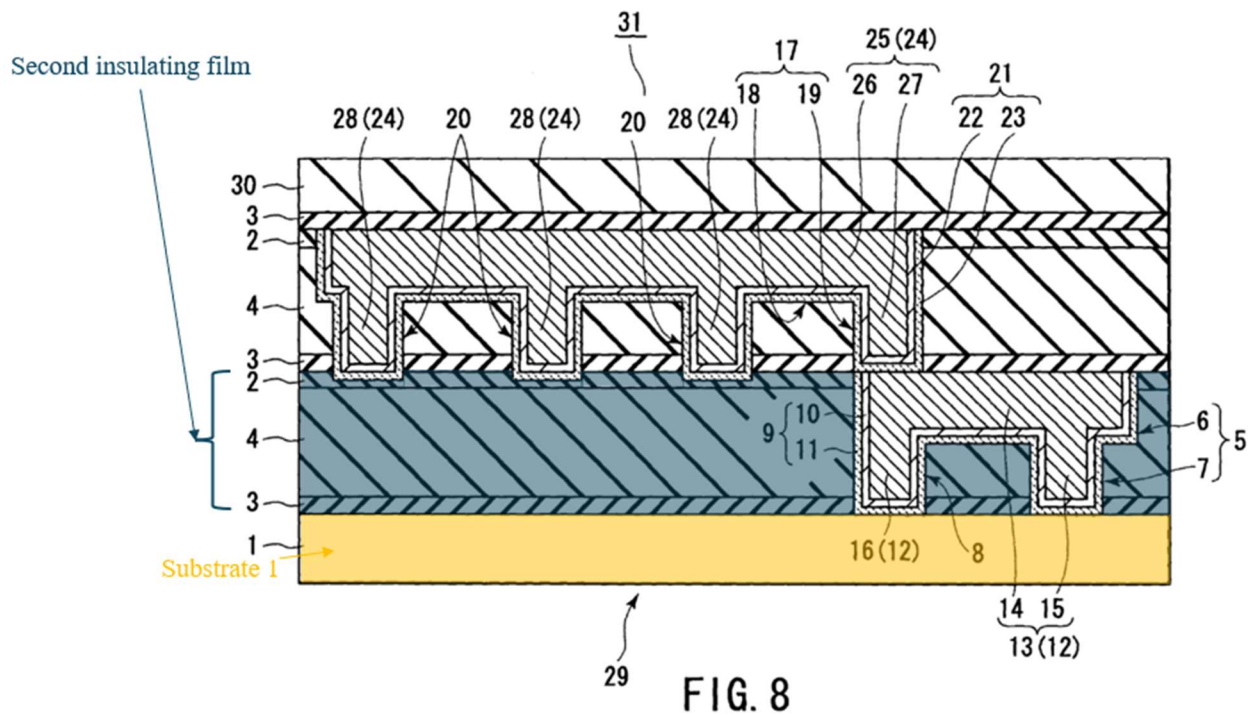
398. I believe that claims 2 and 8 are obvious over Hasunuma and Kurashima as discussed below. I summarized Kurashima’s teachings previously. *Supra*, §IX.E.

1. Claim 2

a) [2.a] – “semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate”

399. Element [2.a] recites the “semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,” which Hasunuma discloses.

400. Hasunuma discloses a second insulating film (e.g., the stack of insulating films 3, 4, and 2 in Figure 3A)⁸, on silicon substrate 1, as seen in annotated Figure 8:



TSMC-1005, ¶¶[0090]-[0091], Figs. 8, 14.

⁸ In the alternative, any or both of films 3 and 4 also satisfies the “second insulating film” element, as each of these films/combinations is on the substrate and otherwise satisfies the requirements of claim 2.

b) [2.b] – “wherein the first interconnect is formed on the second insulating film”

401. Element [2.b] calls for “wherein the first interconnect is formed on the second insulating film,” which Hasunuma discloses.

402. Hasunuma discloses first interconnect (e.g., conductive layer 14) on the second insulating film, as seen in annotated Figure 8:

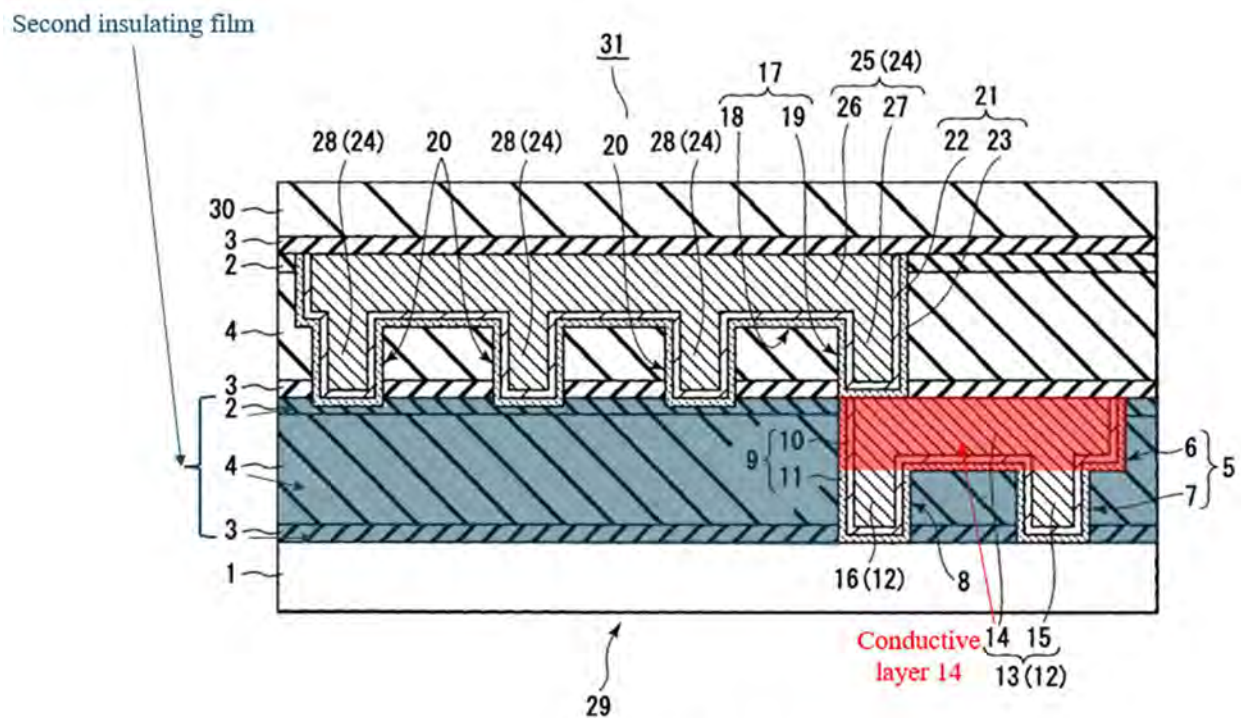


FIG. 8

TSMC-1005, ¶¶[0092]-[0098], Figs. 3A, 8, 14.

c) [2.c] – *“the dummy via is connected to a first dummy interconnect formed on the second insulating film”*

403. Element [2.c] calls for “the dummy via is connected to a first dummy interconnect formed on the second insulating film,” which Hasunuma and Kurashima disclose.

404. Hasunuma discloses dummy vias (e.g., “reinforcing plugs 28”), as seen in annotated Figure 8:

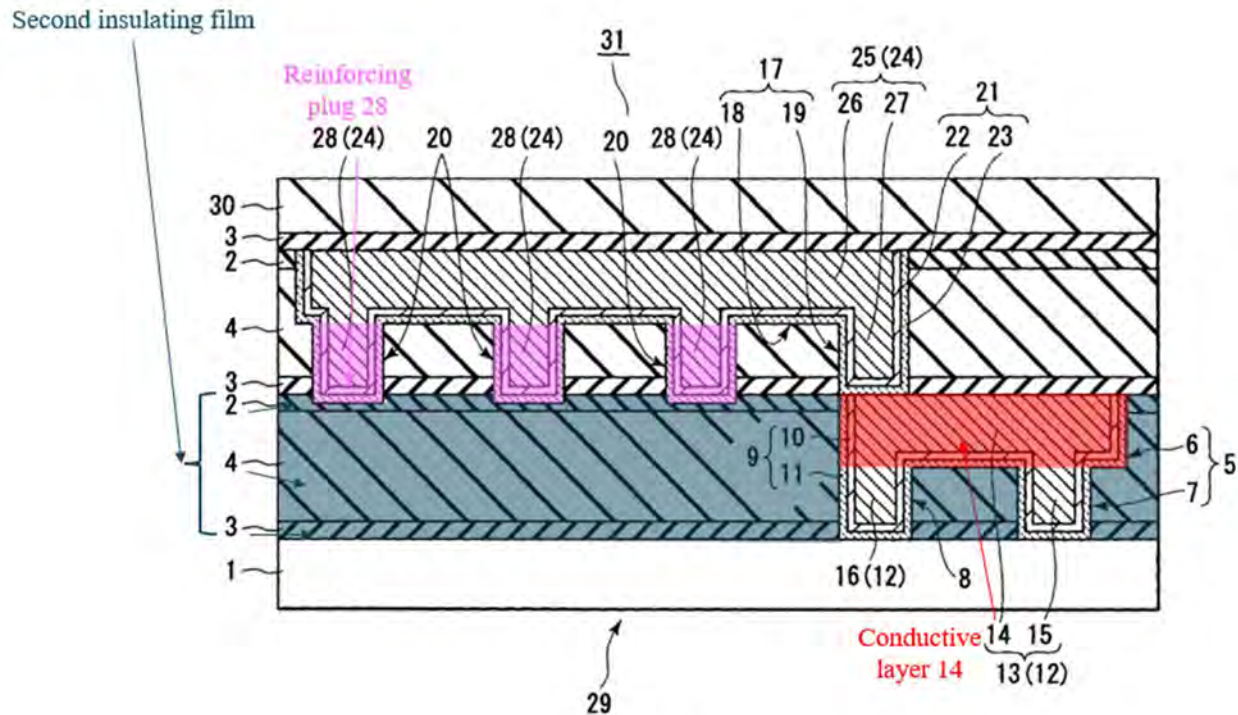
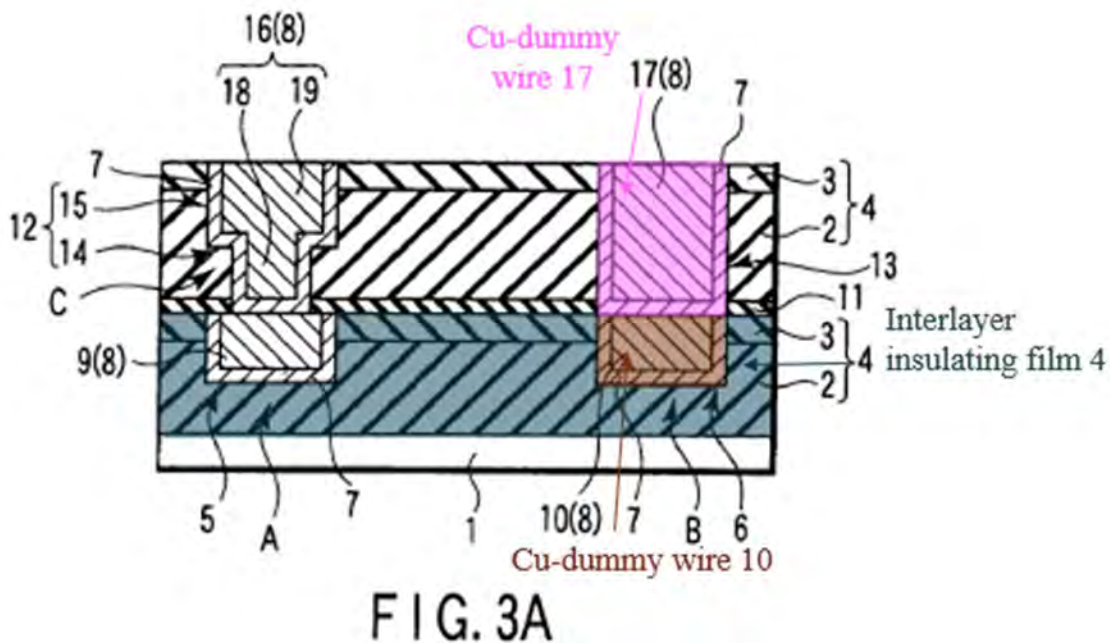


FIG. 8

TSMC-1005, Fig. 8.

405. Kurashima discloses simultaneously forming both a first interconnect (e.g., “Cu-wire 9” and “TaN-film 7,” hereafter collectively “Cu-wire 9”) and a first

dummy interconnect (e.g., “Cu-dummy wire 10” and “TaN-film 7,” hereafter collectively “Cu-dummy wire 10”) on a semiconductor substrate (e.g., “semiconductor substrate 1”). TSMC-1011, 4:12-21, 4:50-6:57, Figs. 1B-1D. For example, Kurashima teaches forming dummy wire 10 in first interlayer insulating film 4, and then dummy wire/via 17 is formed connecting to dummy wire 10, as seen in annotated Figure 3A:



Id., 4:7-21, Fig. 3A.

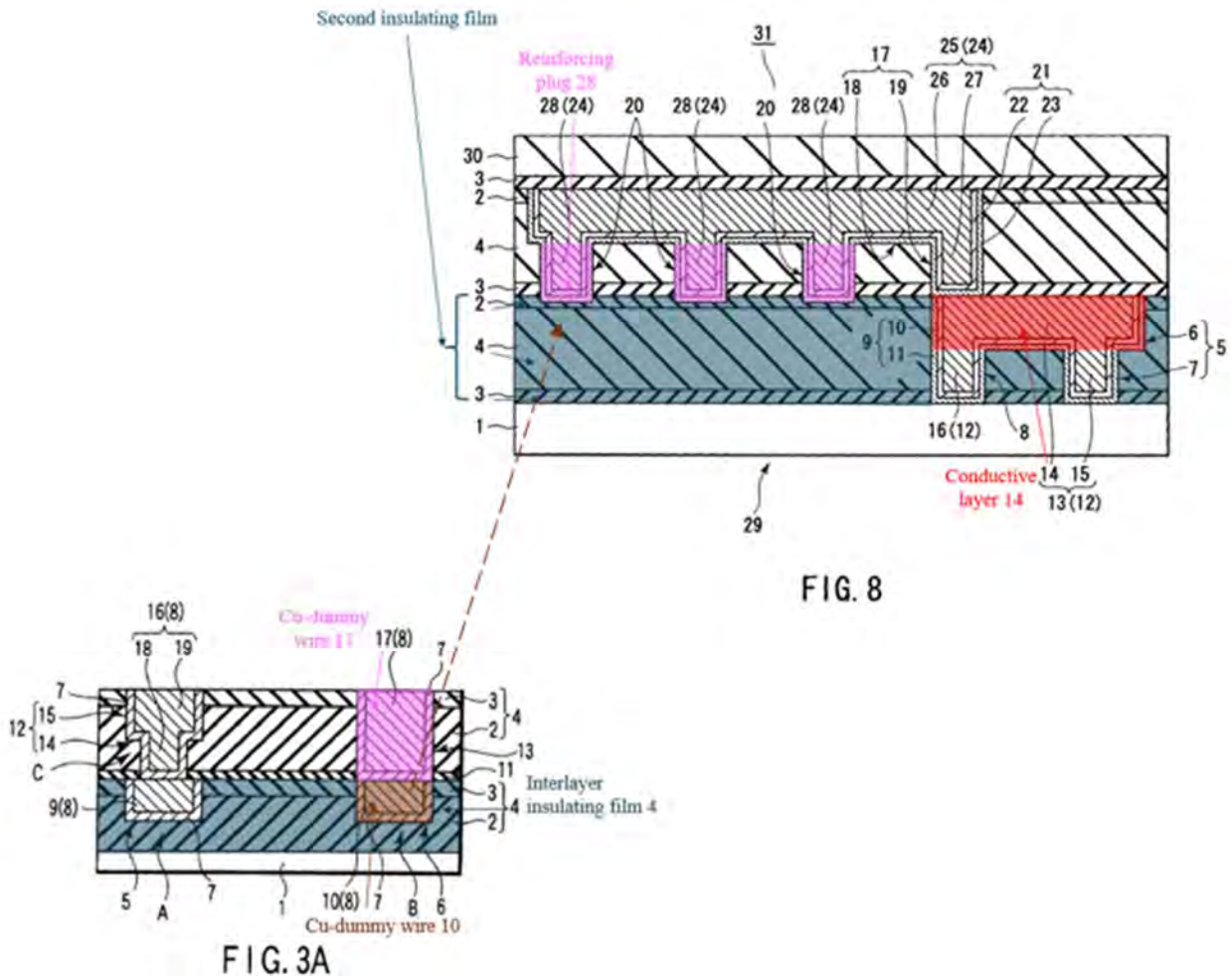
406. A POSITA would understand that dummy wire 10 is a dummy interconnect both because of its description as a “dummy” structure and its purpose (i.e., to add structural support to the device and prevent peeling of layers rather than as an active circuit element), which is consistent with the ’623 patent’s description of a “dummy interconnect.” Specifically, dummy wire 10 does not constitute part

of a closed circuit in actual use of the device, i.e., no current flows therein during use. *Id.*, 4:58-61. Rather, Kurashima uses dummy wire 10 (and its direct connection to a dummy via, i.e., “Cu-wire 9”) to add structural support to the device and thereby reduce film peels. *Id.*, 5:63-6:32 (“Therefore, the SiC film 3 is substantially connected to the low-relative-dielectric-constant film 2 via the Cu-dummy wire 10 and TaN-film 7. Accordingly, the adhesion at the interface between the SiC-film 3 and low-relative-dielectric-constant film 2 is enhanced to a size that can bear a physical load of CMP. That is, the durability of the interlayer insulating film 4 against the mechanical stress in the CMP process is enhanced in forming the Cu-wire 9 and Cu-dummy wire 10 of the first layer. Accordingly, the film peels in the layer are reduced.”). Thus, the connection between dummy wire 10 and dummy wire 17 enhances the adhesion between insulating layers (especially at the interface with a low-dielectric film like Kurashima’s low dielectric film 2) and improves durability against CMP-induced stress. Additionally, Kurashima’s device would still be operable if dummy wire 10 was omitted, because it serves no part in routing current flow as part of the actual operation of the device.

d) Obviousness of Combining Hasunuma and Kurashima

407. A POSITA was motivated to improve the mechanical strength of Hasunuma’s structure by applying Kurashima’s teaching to connect Hasunuma’s reinforcing plug(s) 28 to a dummy interconnect beneath them. Kurashima’s

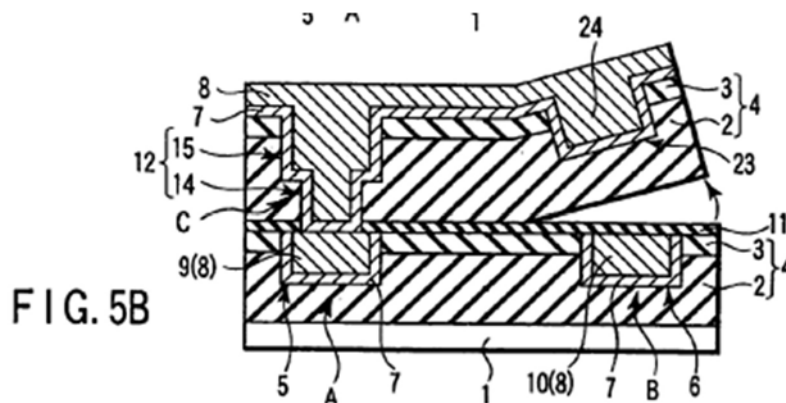
suggested addition from Figure 3A of dummy wire 10 to Hasunuma's Figure 8 structure is illustrated below:



408. A POSITA was motivated to incorporate Kurashima's dummy interconnect(s) into Hasunuma's device to increase the interlayer strength of the semiconductor device to reduce the likelihood of layer peeling or film separation between Hasunuma's lowermost insulating films 4 and 2 (i.e., its low-k film 4 and the overlying insulating film 2), as expressly discussed by Kurashima in regard to its low-k film 2 and overlying insulating film 3. See TSMC-1011, 5:63-6:32

(“According to experiments conducted by the present inventors, when the Cu-dummy wire 10 is not formed, as shown in FIG. 5A, during the first polishing, a film peel was generated at an interface between the low-relative-dielectric-constant film 2 and SiC-film 3. Additionally, in the present embodiment in which the Cu dummy wire 10 is formed, as shown in FIG. 1D, even when not only the first polishing but also the second polishing end, the film peel was hardly generated in the interface between the low-relative-dielectric-constant film 2 and SiC-film 3.”), 8:14-34, Figs. 5A-5B.

409. Kurashima expressly discusses the significance of extending the overlying dummy via such that it contacts the dummy interconnect, in discussing how film peel may still occur when the overlying dummy via is not extended to the dummy interconnect, as shown in Figure 5B:



Id., 8:14-34, Fig. 5B.

410. A POSITA would have readily recognized that implementing a dummy interconnect connected in Hasunuma such that it was connected to a dummy

reinforcing plug 28 would have helped prevent separation with the first insulating layer stack of Hasunuma's device (i.e., as between Hasunuma's low-dielectric constant film 4 and the insulating film 2 directly on top of it) similar to the corresponding structure of Kurashima.

411. Additionally, a POSITA would have been further motivated to incorporate such a dummy plug-dummy interconnect structure to establish additional structural support and uniformity during the polishing step to reduce dishing. *See* TSMC-1011, 5:63-6:32; TSMC-1007, 4:12-44. Use of dummy structures to prevent dishing was widely known and utilized prior to the '623 patent. As noted for example in Figure 8 of Hasunuma below, there is a large vacant space in the insulating film beside conductive layer 14:

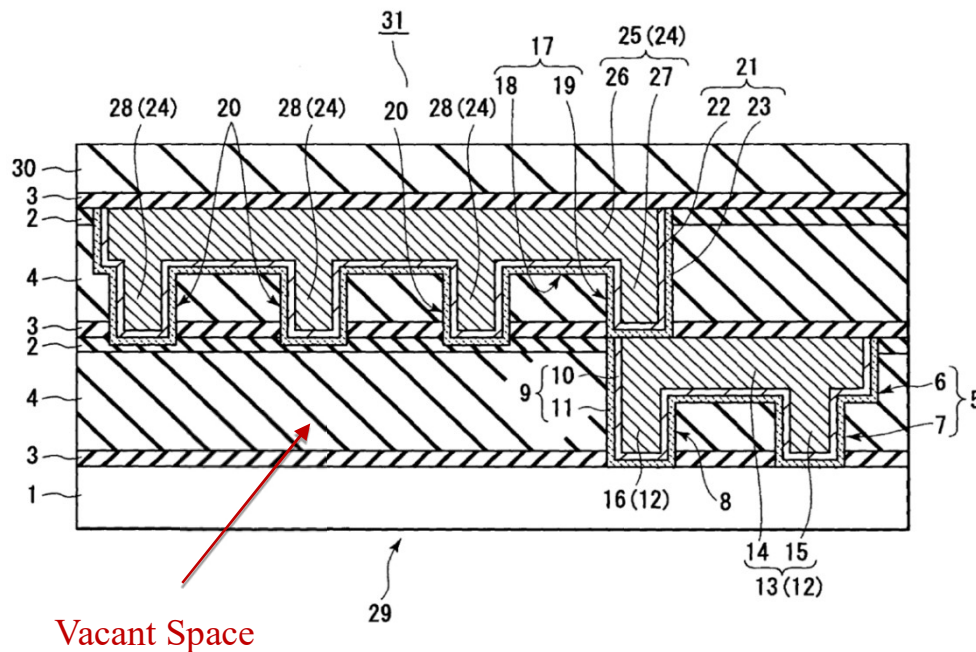


FIG. 8

412. A POSITA would have readily recognized that adding a dummy interconnect connected to dummy plugs 28 in this space would have helped prevent dishing that may otherwise occur during the polishing step (*see* TSMC-1005, Fig. 3A, ¶[0098]) for the formation of the conductive layer 14. *See also* TSMC-1024, 2:55-58 (“This application of dummy patterns results in better fill in bulk metal circuit lines with subsequent improved planarization after CMP and in the elimination of dishing or surface concavity after CMP of large open areas.”).

413. A POSITA would have expected success when incorporating Kurashima’s dummy plug-dummy interconnect structure into Hasunuma’s device, which entailed only the positioning of a dummy interconnect beneath one or more of the dummy vias/reinforcing plugs 28 of Hasunuma. Creation of the dummy interconnect could have been easily accomplished using the same processing steps already utilized in Hasunuma to create its first interconnect layer (“conductive layer 14”), with the dummy via (“first reinforcing plug 28”) connected thereto as part of building the next level in Hasunuma’s Figure 8 structure. *See, e.g.*, TSMC-1005, ¶¶[0090]-[0099], Figs. 1A-3A. For example, a POSITA would have readily recognized that the dummy interconnect need merely be patterned and created in the same layer and manner as conductive layer 14 using the same processing techniques already used in Hasunuma to create conductive layer 14. Reinforcing plug 28 could then have been easily connected to the dummy interconnect using the same

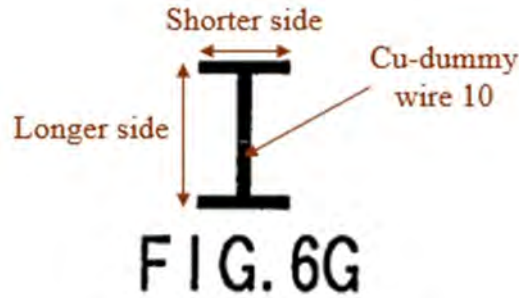
processing techniques already disclosed in Hasunuma as being used to create reinforcing plug 28 and conductive plug 27 (whereby conductive plug 27 is connected to conductive layer 14).

2. Claim 8 – “semiconductor device of claim 2, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle”

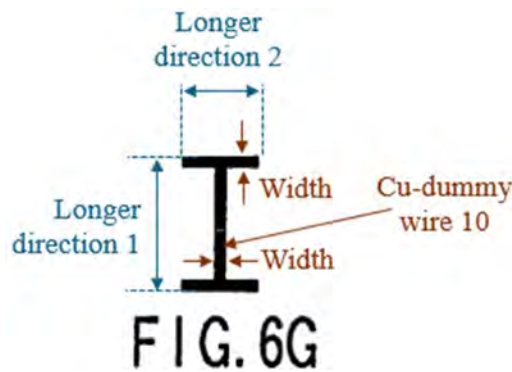
414. Claim 8 recites the “semiconductor device of claim 2, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle,” which Hasunuma and Kurashima render obvious.

415. As discussed *supra* §X.F.1.(c)-(d), Kurashima suggests adding a first dummy interconnect to Hasunuma.

416. As well-understood by a POSITA, the shapes of functional and dummy interconnects were a mere design choice, the selection of which was dictated by device design parameters including establishing desired wire connections while optimizing density, managing crosstalk, and/or achieving specific CMP objectives. *see, e.g.*, TSMC-1004, Fig. 9 (showing an exemplary routing for interconnect 60). This is exemplified by Kurashima, which discloses many different dummy wiring shapes having “longer sides” oriented in either/both orthogonal direction(s). *See* TSMC-1011, Figs. 3B, 6A-9C. Figure 6G of Kurashima is one such example:



417. Other shapes in Kurashima’s Figures 3B, 6A, 6M, etc. have an overall longer side from top to bottom, while the shapes in Figures 7D, 7G-7H, 8C, and 9C have an overall longer side from left to right. *Id.*, Figs. 3B, 6-9. Similarly, if the “longer side” of the dummy wire is simply considered to be the direction orthogonal to its width, Kurashima’s dummy wires have “longer sides” running both up-down and side-to-side:



Under either reading, Kurashima’s Figure 6 teaches dummy interconnect patterns having “longer sides” in both orthogonal directions (i.e., top-to-bottom and side-to-side).

418. A POSITA knew that interconnects, including dummy interconnects and functional interconnects such as Hasunuma’s conductive layer 14, will typically

have turns (including 90-degree corners) similar to Kurashima's disclosed Cu-dummy wire 10 and Watanabe's interconnect 60. It was also typical to have several such interconnects extending in different directions and around other elements, according to design requirements.

419. Accordingly, when adding dummy interconnect(s) as taught by Kurashima into Hasunuma's device as discussed above, a POSITA would have found each of Kurashima's foregoing dummy interconnect shapes to be known, obvious design options, which would have been selected based on design requirements for the specific device being designed, and optimized for achieving improved adhesion between layers.

420. When choosing one of Kurashima's "longer side" shapes discussed above, it was obvious to position Hasunuma's conductive layer 14 ("first interconnect") such that its longer side was perpendicular to a longer side of an added dummy interconnect. For example, when choosing a dummy interconnect shape such as shown in Kurashima's Figure 6G, the dummy interconnect would be positioned with a longer side perpendicular to a longer side of Hasunuma's conductive layer 14 (or another similar interconnect in the same wiring level). Such layouts would have been obvious, employed according to the design considerations mentioned above.

421. A POSITA would have expected success when implementing such interconnect shapes and orientations, which merely requires that the trenches defining such interconnects be patterned in the desired shapes and orientations. This was easily accomplished with standard patterning and etching techniques at the time.

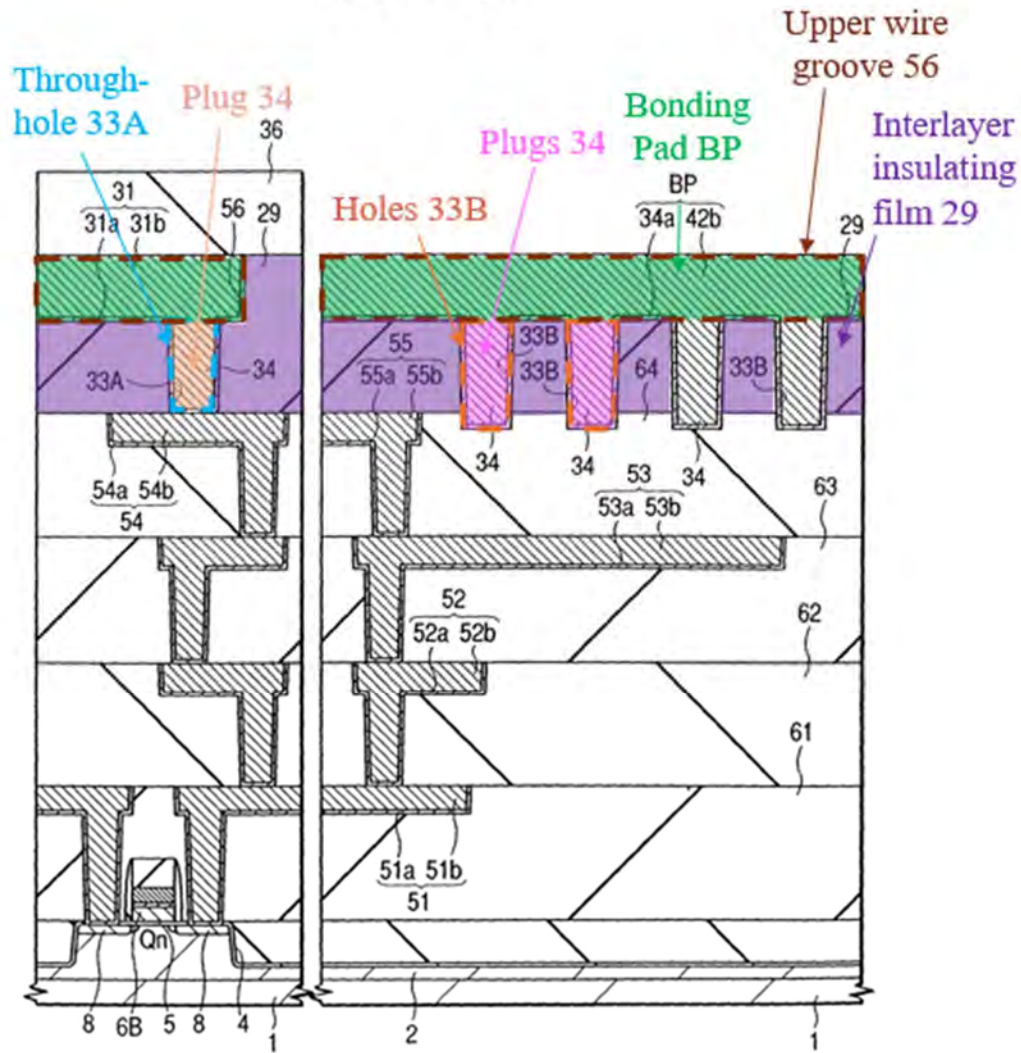
G. Ground 7: Aoyagi Renders Obvious Claims 1, 16, and 45-46

422. I believe that claims 1, 16, and 45-46 are obvious to a POSITA based on Aoyagi, as detailed below. I previously summarized Aoyagi. *Supra*, §IX.C.

1. Aoyagi's Dual Damascene Teaching

423. I discuss Figures 3 and 4 below for certain structural elements. Aoyagi's Figure 19 teaches using a dual damascene process for interconnect/via fabrication, noting that "upper wire 31 (including the bonding pad BP)" may be formed by depositing conductive material into the functional and dummy via holes 33A, 33B and wire groove 56. TSMC-1006, ¶[0077], Fig. 19. See annotated Figure 19 below:

FIG. 19



A POSITA would recognize that this dual damascene process applies to forming the interconnects (e.g., second-layer wire 35 and third-layer wire 31 that includes bonding pad BP) and the functional and dummy vias (e.g., plugs 34 in holes 33C, 33B) of Figures 3-4.

424. In addition, as discussed above, given Aoyagi's discussion of using a dual damascene process to form wire 31/bonding pad BP and to deposit conductive

material in holes 33A and 33B and upper wire groove 56, it was obvious to use a dual damascene process to form bonding pad BP/lead wire 32 and the vias formed in through-holes 33C in the structure of Figures 3-4. *Supra*, §IX.C; *infra*, §X.G.2.

425. A POSITA would have been motivated to do so by the well-known benefits associated with the dual damascene process, which include increased manufacturing simplicity and efficiency (afforded by forming the vias and interconnects simultaneously rather than serially), the resulting reduced cost, and improved reliability including a reduced risk of electromigration failure. *See* TSMC-1034, 583-84, 671-76, 695, 698, 718, 723-26; TSMC-1015, 4:20-23; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1019, Abstract, 145-151; TSMC-1027, 25; TSMC-1028; 5458-59.

426. Indeed, the nature of and advantages associated with dual damascene were well understood in the art. *See, e.g.*, TSMC-1019, 146-147 (stating that dual damascene enhances density and performance and promotes reliability and improves manufacturability, including manufacturing yield); TSMC-1027, 25 (noting dual damascene forms Cu wires and vias with one metal fill and one CMP step, providing process simplification allowing for reduced cost and improved manufacturability); TSMC-1028, 5458 (discussing that, with making one level of lines and one level of vias together, can build more levels of Cu interconnects with same number of processing steps). Regarding simplified and more efficient manufacturing, a

POSITA was aware that: “The dual-damascene process offers the advantage of reducing the number of process steps” (TSMC-1034, 673); “The reduction in the number of processing steps is another of the benefits that have driven the development of dual-damascene processes” (*id.*, 676). The foregoing benefits are easily recognized when compared to other manufacturing process (e.g., single damascene) where interconnect trenches and vias are independently formed one step at a time, a much more time consuming and thus oftentimes expensive process.

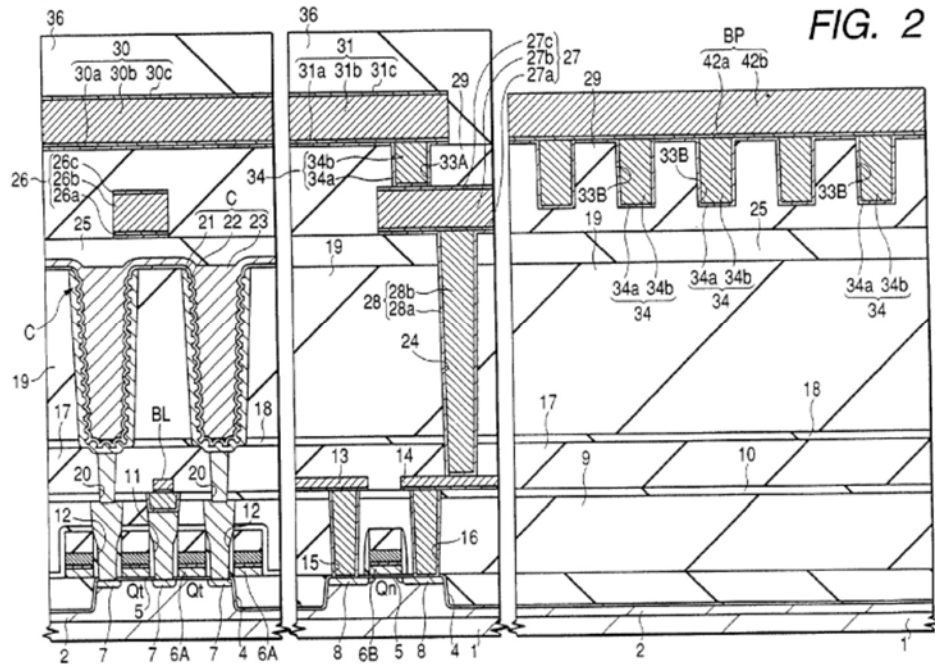
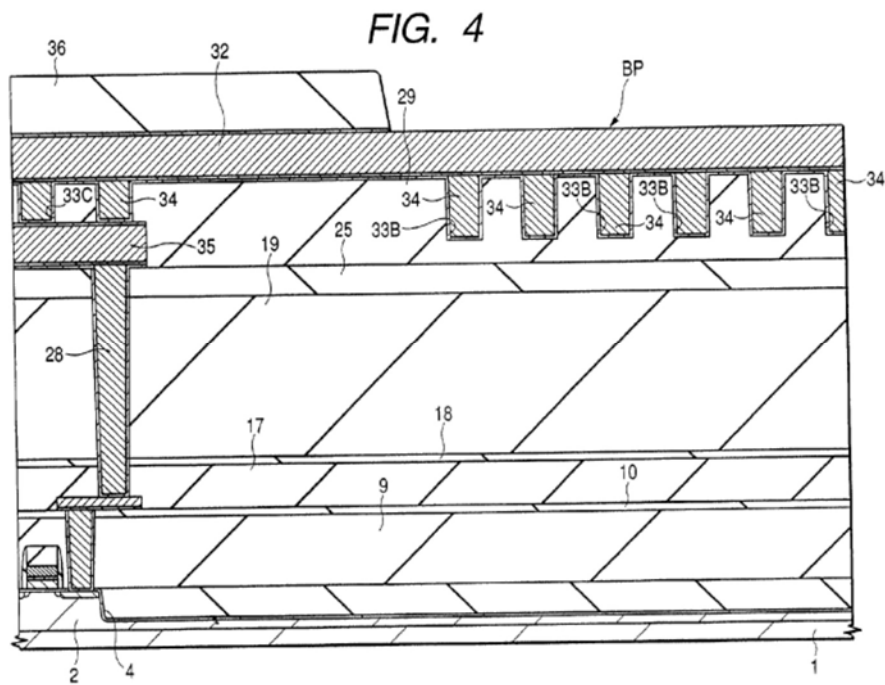
427. A POSITA would have further recognized that use of the dual damascene process in this manner could have been easily implemented given its already disclosed use in Aoyagi, and its general widespread use in industry at the time as widely recognized in the various contemporary references discussed above and, thus, would have expected success in the use of the dual damascene process in this manner. *See also* TSMC-1015, 3:63-4:22; TSMC-1034, 583-84, 671-76, 718, 723-26 (explaining development, implementation, and advantages of the dual-damascene process); *supra*, §VI.A.

2. Claim 1

a) [1.pre] – “*semiconductor device*”

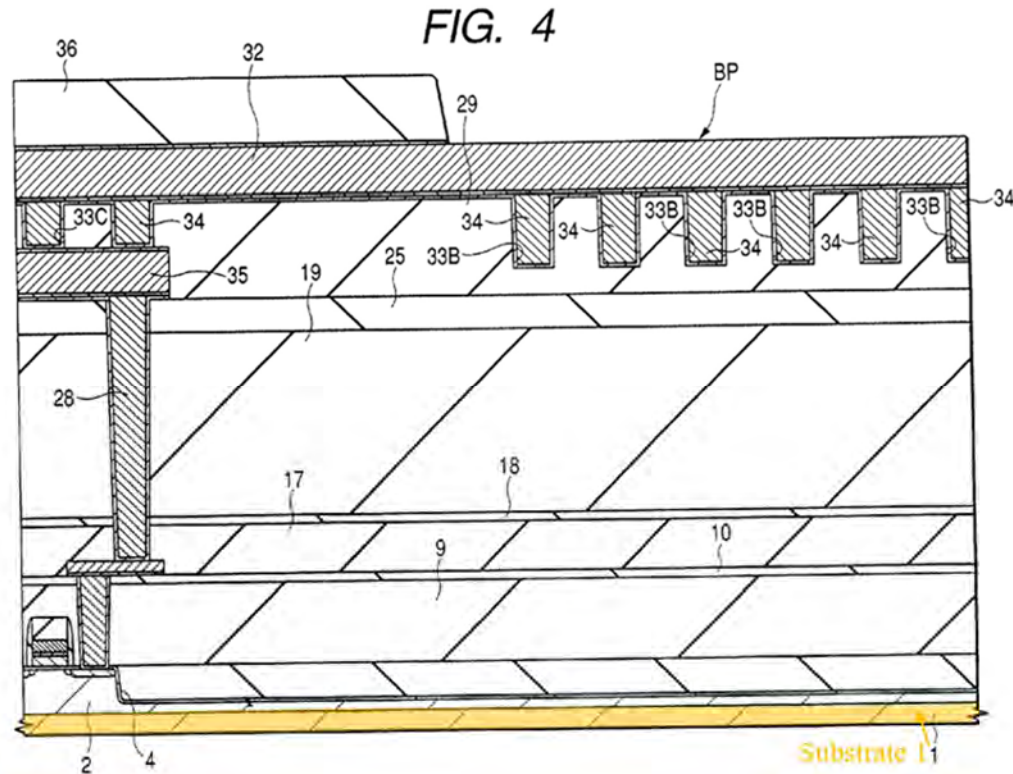
428. The preamble of claim 1 recites a “semiconductor device,” which Aoyagi discloses. For example, as shown throughout Aoyagi’s figures (including

Figures 2 and 4 reproduced below), Aoyagi discloses a “semiconductor integrated circuit device.” TSMC-1006, Abstract, ¶[0001], Figs. 2-4, 19.



b) [1.a] – “a semiconductor substrate”

429. Element 1[a] recites “a semiconductor substrate,” which Aoyagi discloses in the form of at least semiconductor substrate 1. Aoyagi’s semiconductor substrate 1 is shown in annotated Figure 4:

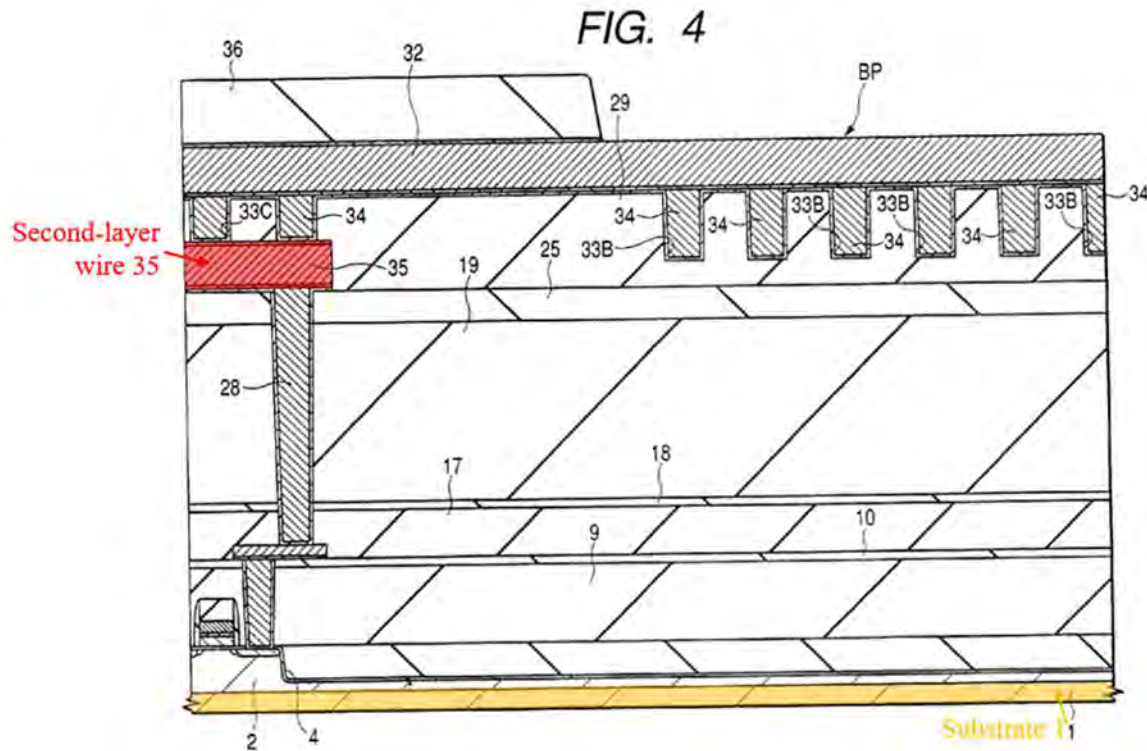


TSMC-1006, [0040], [0043], [0057], [0061], Figs. 2, 4.

c) [1.b] – “a first interconnect formed on the semiconductor substrate”

430. Element [1.b] recites “a first interconnect formed on the semiconductor substrate,” which Aoyagi discloses.

431. For example, Aoyagi discloses a first interconnect (e.g., “second-layer wire 35”) formed on substrate 1. TSMC-1006, ¶¶[0055], [0061], Figs. 4, 7. A POSITA would understand Aoyagi’s various wires and its bonding pad BP to be “interconnects.” Indeed, throughout Aoyagi, its interconnects are described using the term “wire” or “bonding pad” (e.g., “first-layer wire,” “second-layer wire,” “third-layer wire,” “bonding pad BP”). A POSITA understood that such wires and bonding pad BP of Aoyagi constitute “interconnects” as those terms are understood in the art because both Aoyagi’s wires and bonding pad BP are structures formed of conductive material (e.g., copper surrounded by a barrier metal to prevent diffusion of the copper into the surrounding insulator material), typically functioning to carry electrical signals from one point to another. *See, e.g.*, TSMC-1001, 1:20-27. Wires/bonding pads/interconnects on different levels can be electrically connected by vias, which are holes in the insulating film separating the interconnects that have been likewise filled with conductive material (e.g., copper surrounded by a barrier metal). *See, e.g., id.*, 1:36-38. Annotated Figure 4 discloses this feature:



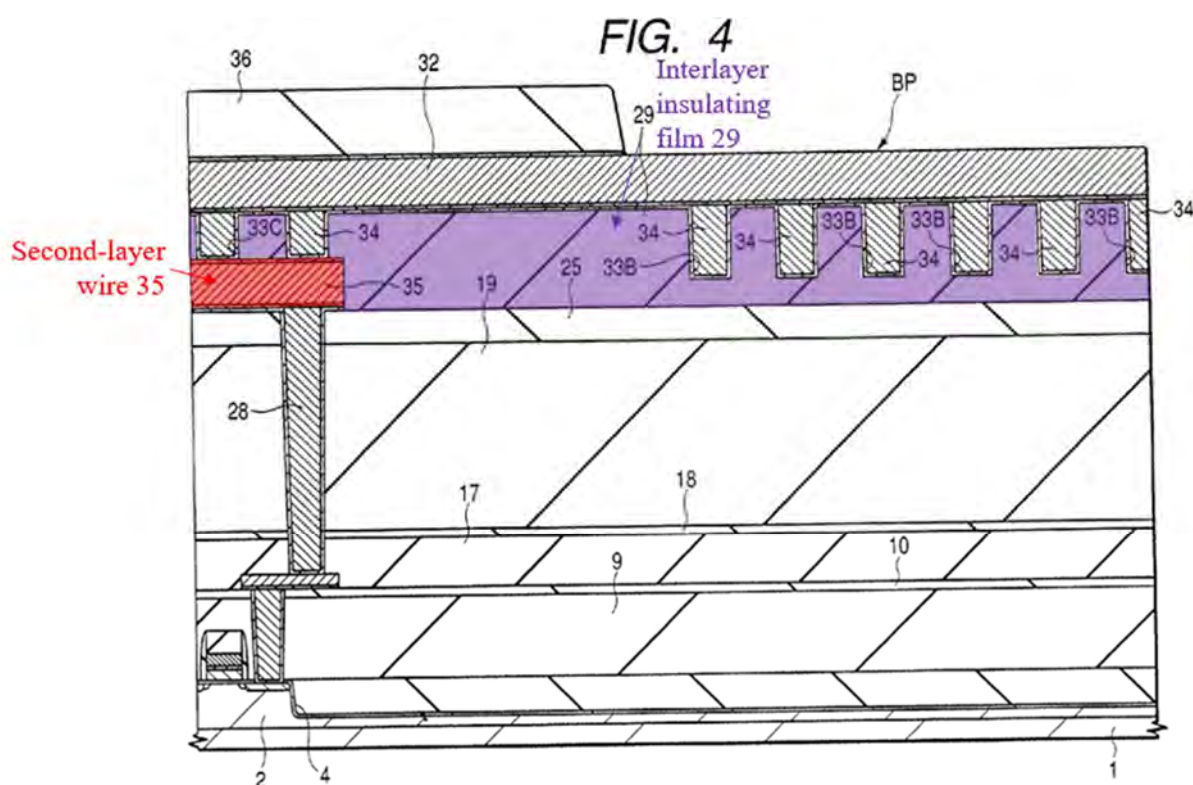
TSMC-1006, Fig. 4.

d) [1.c] – “a first insulating film formed on the first interconnect”

432. Element [1.c] recites “a first insulating film formed on the first interconnect,” which Aoyagi discloses.

433. For example, Aoyagi discloses interlayer insulating film 29 formed on second-layer wire 35, explaining that “insulating film (first interlayer insulating film) 29...is formed over the second-layer wires 26, 27.” TSMC-1006, ¶[0049] (emphasis added). Throughout its specification, Aoyagi uses common layer designations (e.g., “first-layer,” “second-layer,” “third-layer,” etc.). A POSITA would understand these common layer designations to indicate that the same

component types are formed in a same layer and formed in the same manner as other common components in that layer. In this regard, given the common layer disclosures in Aoyagi's figures and common designation "second-layer wire" for wires 26, 27, 35, "insulating film 29" is formed on "second-layer wire 35" just like "second-layer wires 26, 27." Thus, annotated Figure 4 discloses the interlayer insulating film 29 formed on the second-layer wire 35:

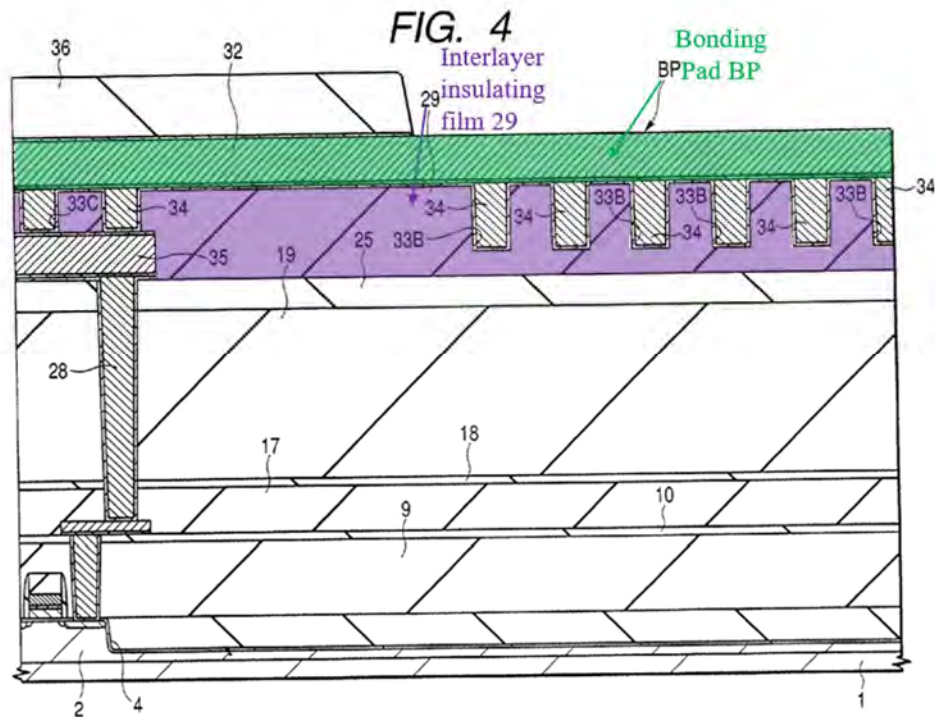


Id., ¶¶[0049], [0062], Figs. 4, 8.

e) [1.d] – “*a second interconnect formed on the first insulating film*”

434. Element [1.d] recites “a second interconnect formed on the first insulating film,” which Aoyagi discloses.

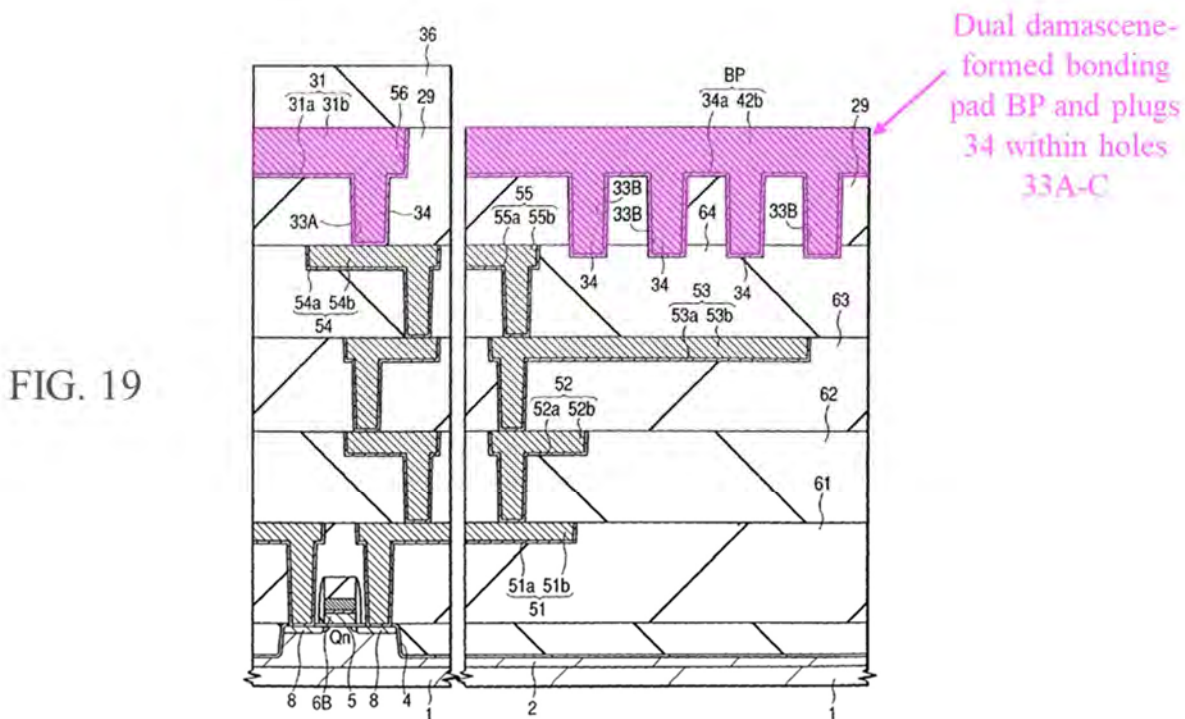
435. For example, Aoyagi discloses a second interconnect (e.g., “bonding pad BP” with “lead wire 32”)⁹ formed on insulating film 29 as shown below in annotated Figure 4:



⁹ As demonstrated by Figures 3-4, “bonding pad BP” and “lead wire 32” together form a single, integral component, and as such discussion of “bonding pad BP” herein includes “lead wire 32” unless indicated otherwise. *See* TSMC-1006, Figs. 3-4.

TSMC-1006, ¶¶[0049]-[0055], [0077], Figs. 2-4, 19.

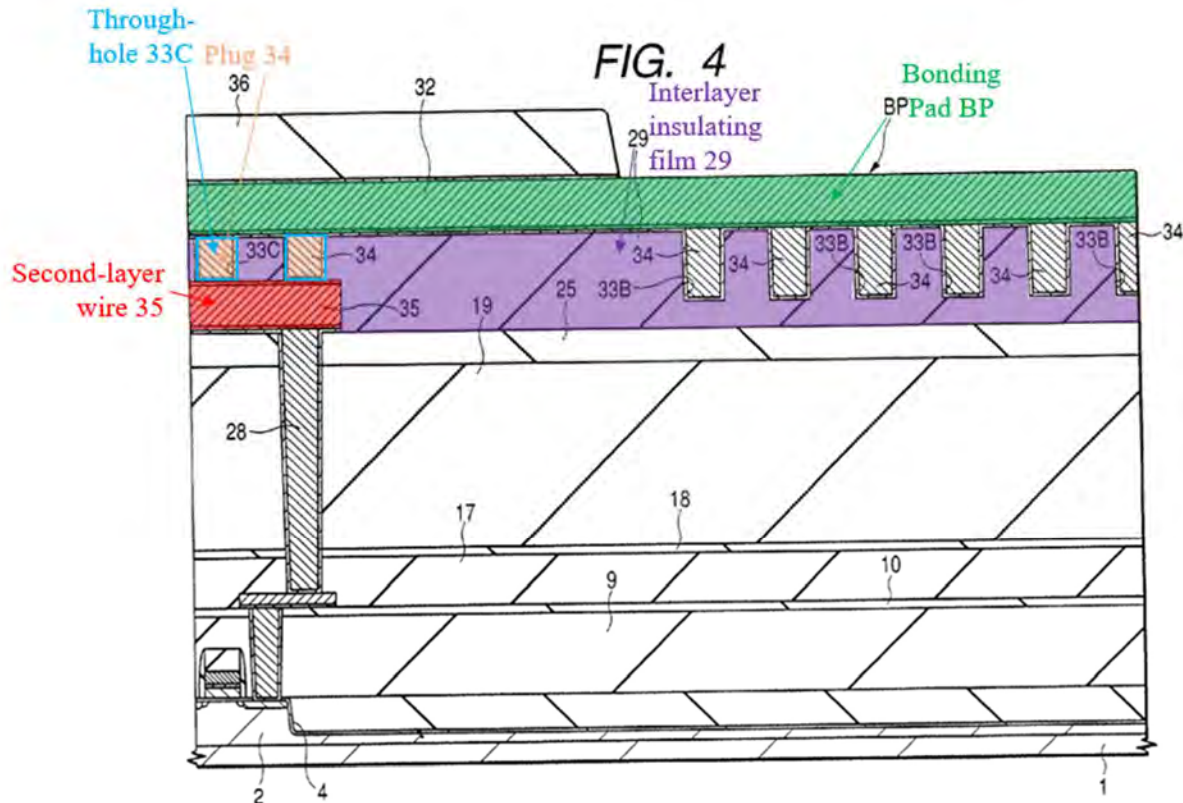
436. When formed using dual damascene, bonding pad BP is formed by depositing “barrier metal film 34a” and then “Al alloy film 31b (42b)” onto interlayer insulating film 29. *Id.*, ¶[0077]; Fig. 19. Annotated Figure 19 discloses the bonding pad BP when formed using a dual damascene process, which a POSITA would understand is equally applicable to the device of Figures 3-4:



f) [1.e] – “a via formed through the first insulating film and connecting between the first and second interconnects”

437. Element [1.e] recites “a via formed through the first insulating film and connecting between the first and second interconnects,” which Aoyagi discloses.

438. For example, Aoyagi discloses a via (e.g., “plug 34” in “through-hole 33C”) formed through insulating film 29 that connects first and second interconnects (e.g., “wire layer 35” and “bonding pad BP,” respectively). These elements are shown in annotated Figure 4 below:



TSMC-1006, ¶¶[0049]-[0055], [0077], Figs. 2-4, 19.

439. Regarding formation of via and dummy holes, Aoyagi discloses “[i]n...insulating film 29 beneath the bonding pad BP, a plurality of **holes 33B** are formed....” *Id.*, ¶[0052]. Also, “through-hole 33A” and “through-hole 33C” are “formed in the interlayer insulating film 29.” *Id.*, ¶¶[0050], [0055], Fig. 4. Thus, all through-holes 33A, 33B, 33C are formed in insulating film 29. Given Aoyagi’s

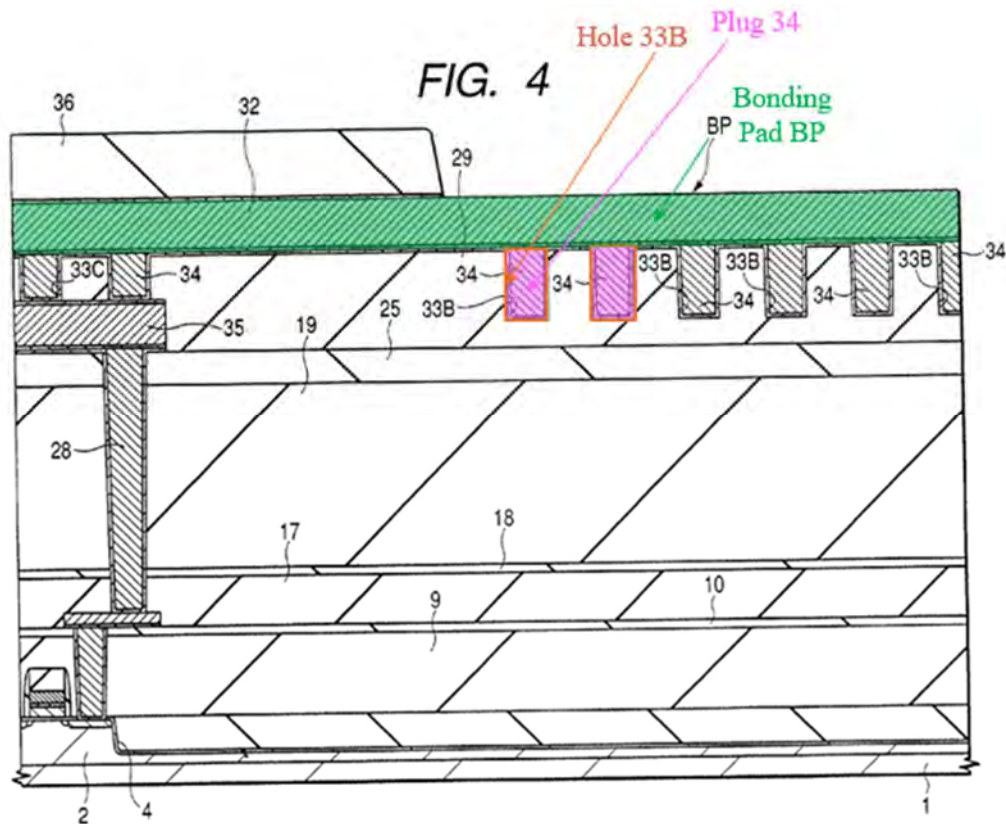
express discussion of using a dual damascene process to form wire 31/bonding pad BP and deposit conductive material in holes 33A and 33B, a POSITA would understand Aoyagi to teach and/or suggest using a dual damascene process to form each of bonding pad BP (with lead wire 32) as well as the vias formed in through-holes 33C and the dummy vias in through-holes 33B in the structure of Figures 3-4.

440. When formed using dual damascene (as was obvious as discussed *supra*, §X.G.1), bonding pad BP/lead wire 32 and plugs 34 (within holes 33C) are formed by depositing barrier metal film 34a in holes 33C formed through insulating film 29, and then depositing “Al alloy film 31b (42b)” on the barrier metal film. TSMC-1006, ¶[0077].

g) [1.f] – “a dummy via connected to the second interconnect”

441. Element [1.f] recites “a dummy via connected to the second interconnect,” which Aoyagi discloses.

442. Specifically, Aoyagi discloses dummy vias (e.g., “plugs 34” formed in “holes 33B”) connected to the second interconnect (e.g., “bonding pad BP”) as again shown in annotated Figure 4:



TSMC-1006, $\text{P}^+\text{P}^+[[0050]-[0056], [0077]]$, Figs. 2-4, 19.

h) [1.g] – “*wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough*”

443. Element [1.g] recites that “the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough,” which Aoyagi discloses.

444. For example, Aoyagi discloses forming dummy plugs 34 by successively depositing barrier metal film 34a and Al alloy film 42b in holes 33B, which are conductive. TSMC-1006, ¶[0077]. Thus, a POSITA would understand

that Aoyagi's dummy plugs (i.e., "dummy vias") are made of a conductive film (e.g., barrier metal film 34a and/or Al alloy film 42b). A POSITA would further understand that these films are deposited when the dual damascene process is utilized to create the dummy plugs 34/dummy vias together with bonding pad BP.

445. Regarding dual damascene, as discussed previously, Aoyagi teaches using a dual damascene process to form wire 31/bonding pad BP and deposit the conductive material (which includes the barrier metal film 34a and Al alloy film 42b from the previous paragraph) in holes 33A and 33B, thereby forming vias and dummy vias, respectively. *Id.*, ¶[0077]. Aoyagi further teaches using this dual damascene process to form bonding pad BP together with the vias/plugs 34 in holes 33C and the "dummy" vias/plugs 34 in holes 33B in the structure of Figures 3-4 as discussed above. *Supra*, §IX.C. A POSITA would further understand that Aoyagi's use of similar reference numerals/labels across common parts when discussing both the device of Figures 3-4 and the use of dual damascene with respect to Figure 19 evidences the applicability of dual damascene processing to the Figures 3-4 device. *See* TSMC-1006, ¶[0036] (stating "like reference numerals indicate like parts or members" across its figures and embodiments). Additionally, as discussed above, it was obvious to use dual damascene and a POSITA was motivated to do so by the increased efficiency and reduced cost of the dual damascene process, and could have

easily implemented such a process given its already disclosed use in Aoyagi. *Supra*, §§X.G.1., IX.C.

446. Holes 33B and dummy plugs 34 are “arranged so as to be incapable of having current flow therethrough.” As previously discussed above regarding incapability of current flow, the ’623 patent specification states:

A dummy via and a dummy interconnect herein means a pseudo via or a pseudo interconnect which do not constitute a closed circuit in actual use of a device with an interconnection structure including these via and interconnect (i.e., **no current flows therein** during actual use of the device.)

TSMC-1001, 3:14-18 (emphasis added).

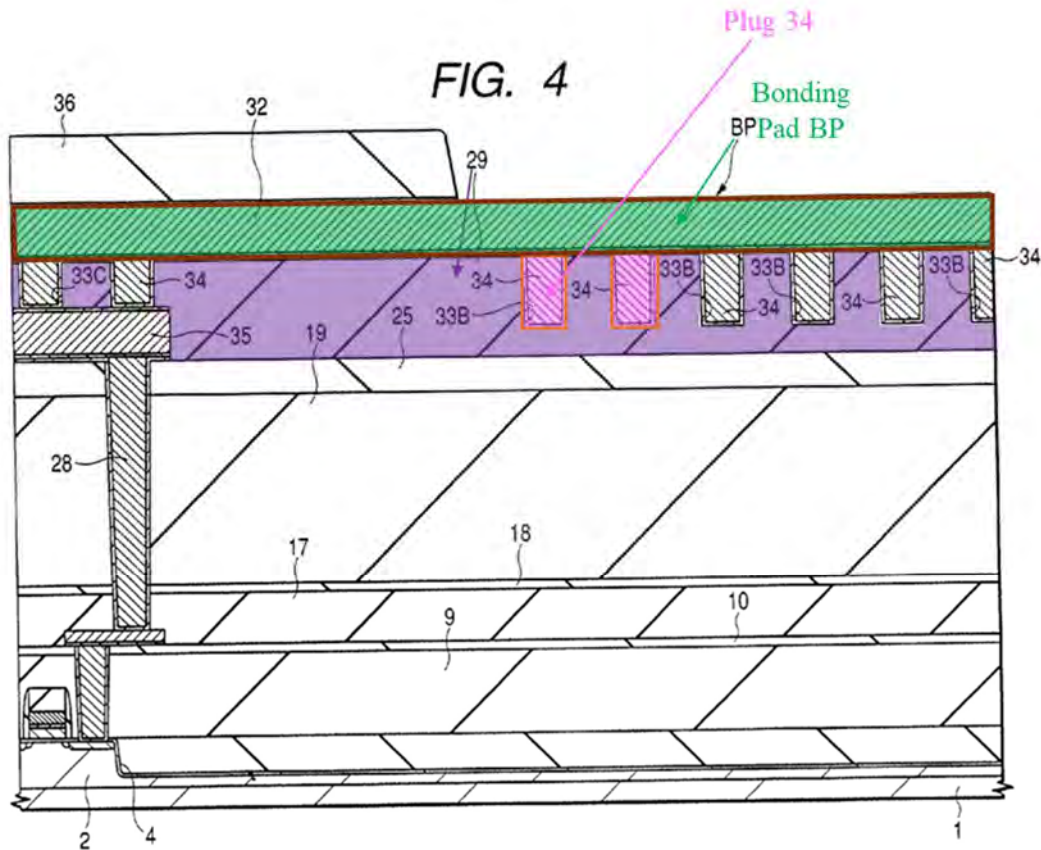
447. The ’623 patent goes on to explain that:

[N]either the dummy interconnect 102B nor the dummy via 110B constitutes a closed circuit in actual use. That is, even if the dummy interconnect 102B and the dummy via 110B are omitted in the interconnection structure shown in FIG. 2B, a device with this interconnection structure is operable at least immediately after fabrication.

Id., 10:26-32 (emphasis added).

448. As illustrated in Figures 4 and 19 below, holes 33B and dummy plugs 34 therein are formed entirely within one or more insulating films (e.g., insulating film 29 in Figure 4 and the combination of insulating films on the upper two layers

in Figure 19). Indeed, as exemplified in annotated Figure 4 below, one end of dummy plugs 34 are connected to bonding pad BP and the bottoms of dummy plugs 34 are formed within insulating film 29:



449. When formed by dual damascene as disclosed in annotated Figure 19, the bottom end of holes 33B and dummy plugs 34 are similarly formed in an insulating film and not connected to a conductive element:

FIG. 19

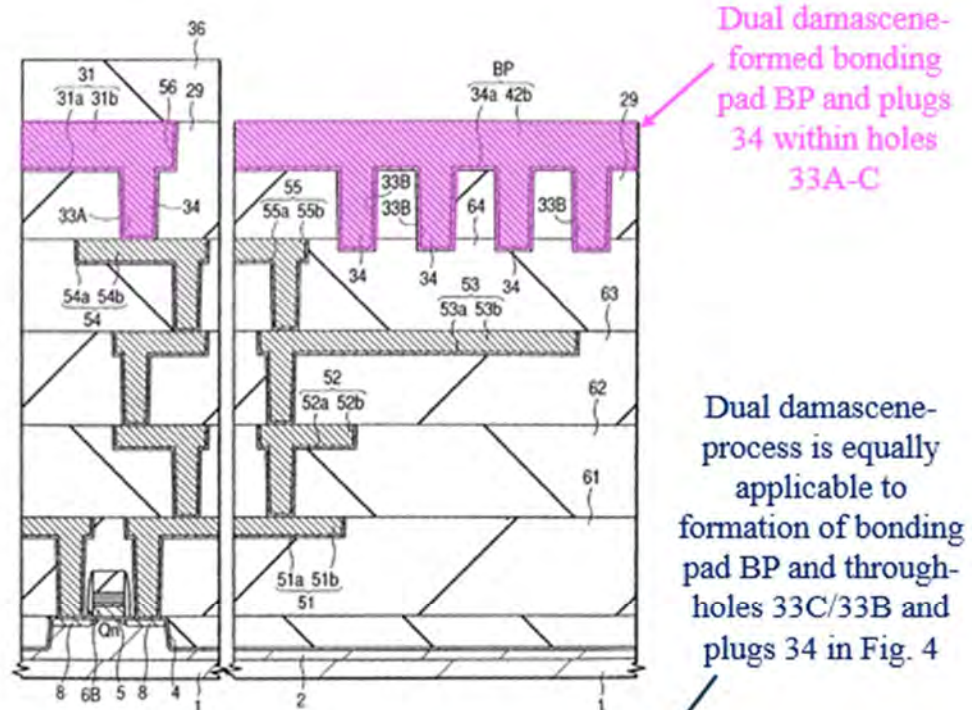
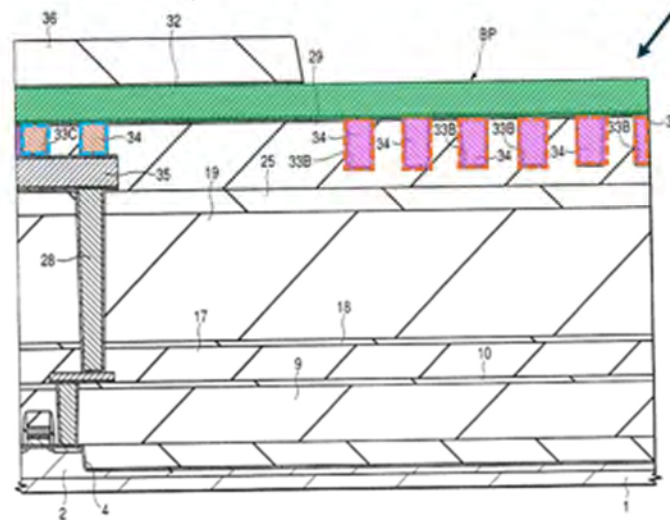


FIG. 4



450. These dummy plugs 34 in through-holes 33B are only connected on one end to an active circuit element (i.e., “bonding pad BP”), while the other end is not connected to a second active circuit element. As Aoyagi notes, its dummy plugs 34 are intended only to improve “adhesion” between bonding pad BP and insulating film 29. TSMC-1006, ¶¶[0053], [0079]; Fig. 4. Thus, no current flows through

Aoyagi's dummy plugs 34 due to this lack of connection to a second active circuit element. Instead, current flows between Aoyagi's second-layer wire 35 and bonding pad BP through plugs in holes 33C, which constitute parts of a closed circuit in actual use of the device. *Id.*, ¶[0055], Figs. 3-4.

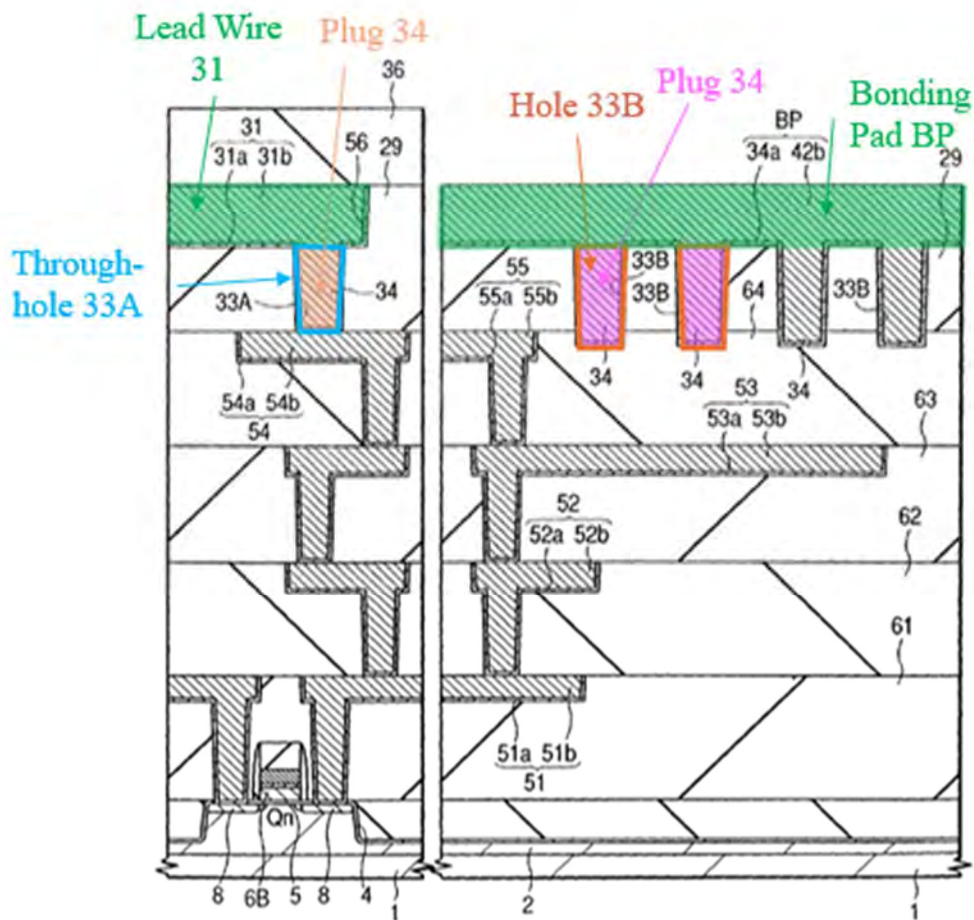
451. A POSITA would thus recognize that no current would flow through Aoyagi's dummy plugs 34 formed in holes 33B, that such plugs/holes do not constitute part of a closed circuit during actual use, and that these plugs/holes could be omitted and the device would still be operable. In Aoyagi, current instead flows through bonding pad BP interconnect and the plugs 34 formed in holes 33C, which constitute portions of a closed circuit in actual use of the device. Thus, omission of dummy plugs 34 in holes 33B would not render the device inoperable since current could still flow (and thus an active circuit still exists) through the plugs 34 in holes 33C.

i) [1.h]/[1.i] – “*the second interconnect and the via form a dual damascene structure*”/“*the second interconnect and the dummy via from a dual damascene structure*”

452. Element [1.h] recites “the second interconnect and the via form a dual damascene structure” and element [1.i] recites “the second interconnect and the dummy via from a dual damascene structure,” both of which Aoyagi discloses.

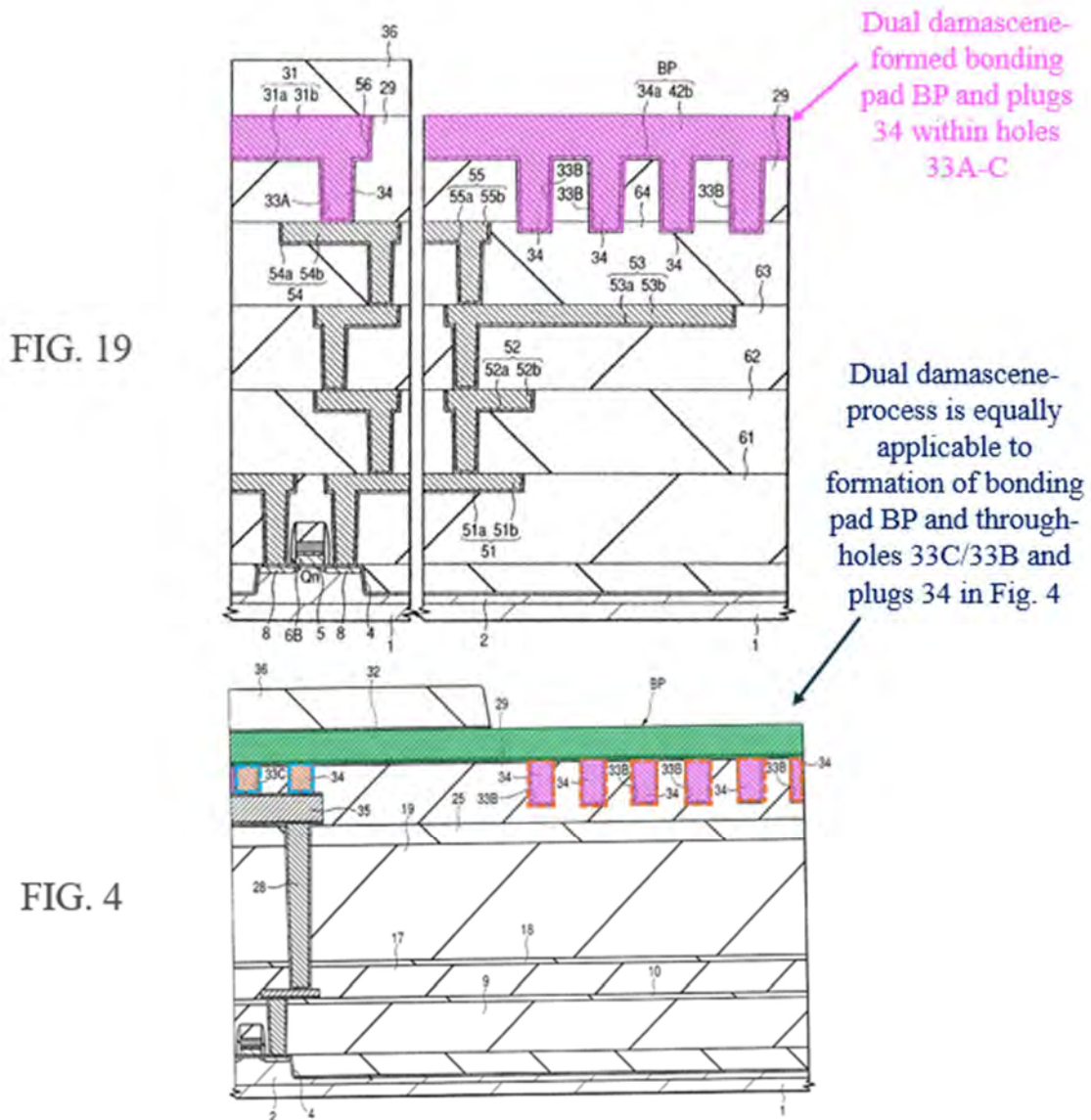
453. As described with respect to Figure 19, Aoyagi teaches integrally forming its second interconnect (bonding pad BP), functional vias (in through-holes 33A), and dummy vias (in holes 33B) using a dual damascene process. TSMC-1006, ¶[0077]. Annotated Figure 19 shows these components:

FIG. 19



454. A POSITA understands that this teaching of using a dual damascene process to form the bonding pad BP and underlying plugs 34 and corresponding holes (i.e., the underlying vias and dummy vias connected to bonding pad BP) also

applies to the corresponding features in Figures 3-4. *Id.*, ¶[0036] (stating that “like reference numerals indicate like parts or members” across its figures and embodiments). Indeed, a POSITA would have understood that Figure 4’s bonding pad BP/lead wire 32 and its associated vias in holes 33C are likewise integrally formed in the dual damascene process together with dummy vias (plugs 34) in holes 33B. This is illustrated in annotated Figures 4 and 19 below:



455. Indeed, a POSITA would understand that when employing Aoyagi's dual damascene process for the fabrication of such a device, a barrier metal film 34a and "Al alloy film 31b (42b)" is deposited in the upper groove 56, to form third-layer (upper) wire 31, bonding pad BP, and plugs 34 in holes 33B, 33C. TSMC-1006, ¶¶[0055], [0077]. Such a process would result in a similar final structure as shown in Figures 3-4 of Aoyagi except that there would be no thin film layer (e.g., layer 42a in Figs. 2, 4)) between the primary conductive materials in bonding pad BP and the various plugs 34.

456. Additionally, for the reasons discussed above, given Aoyagi's discussion of using a dual damascene process to form wire 31/bonding pad BP and to deposit conductive material in holes 33A and 33B and upper wire groove 56, it was certainly obvious to a POSITA to use the dual damascene process (described, for example with respect to Figure 19) to form bonding pad BP/lead wire 32 and the vias formed in through-holes 33C and 33B in the structure of Figures 3-4. *Supra*, §X.G.1. A POSITA would have been motivated to do so by the well-known benefits of dual damascene processing as discussed throughout my declaration, including increased fabrication/manufacturing efficiency and reduced cost afforded by forming the vias and interconnects simultaneously rather than serially. *Supra*, §§X.G.1, IX.C. Additionally, a POSITA would have easily implemented such a process and would have expected success given its already disclosed use in Aoyagi

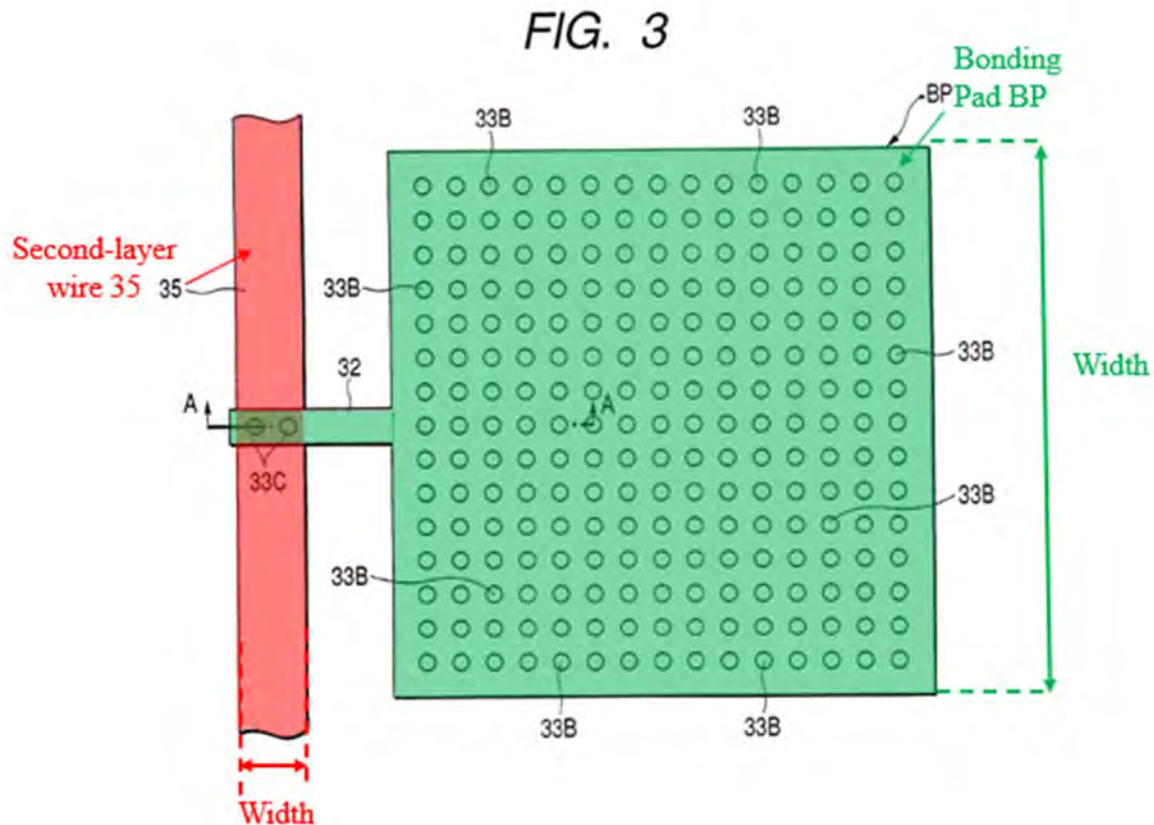
(and widespread use throughout industry at the time given its associated, well-known benefits). *See* TSMC-1015, 3:63-4:22; *supra*, §§X.G.1, IX.C; *see also* TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1018, 129; TSMC-1019, Abstract.

457. Using dual damascene processing, a given interconnect structure is formed in its entirety and simultaneously with its associated vias/dummy vias. *Supra*, §§VI.A; TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1018, 129. Accordingly, when applying Aoyagi's dual damascene process to the embodiment of Figures 2-4, Aoyagi's bonding pad BP (second interconnect) forms dual damascene structures with the vias/dummy vias in holes 33C/33B, respectively. Thus, a POSITA would understand that it was obvious for the bonding pad BP/lead wire 32 (second interconnect) and the vias formed in through-holes 33C, as well as bonding pad BP and the dummy vias formed in holes 33B, to form respective dual damascene structures, satisfying limitations 1.h and 1.i.

3. Claim 16 – “semiconductor device of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect”

458. Claim 16 recites that “the first interconnect has a width smaller than that of the second interconnect,” which Aoyagi discloses.

459. As demonstrated in annotated Figure 3 below, a POSITA would plainly recognize from this figure that Aoyagi's first interconnect (second layer wire 35) has a width smaller than either width of the second interconnect (bonding pad BP):



TSMC-1006, Fig. 3.

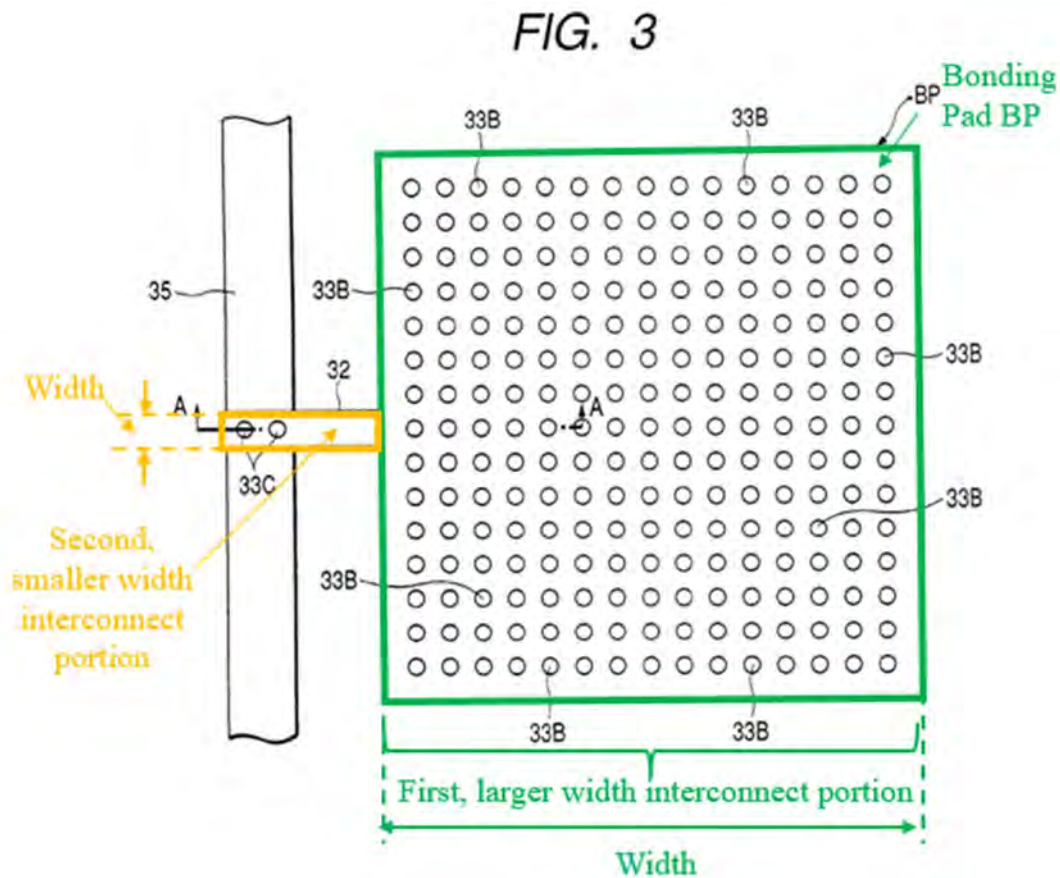
4. Claim 45

460. Aoyagi discloses the elements of claim 45.

- a) [45.a] – “semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion”

461. Element [45.a] recites that “the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion,” which Aoyagi discloses.

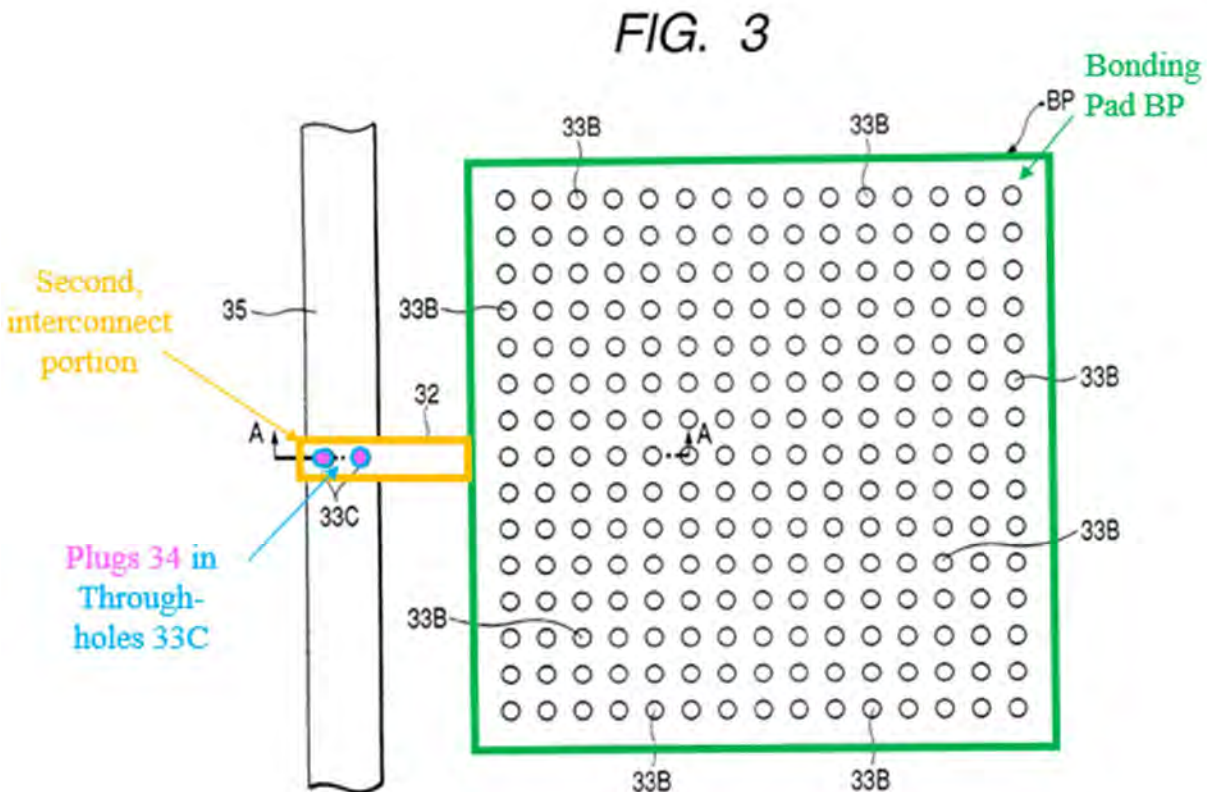
462. As shown in annotated Figure 3 below, Aoyagi discloses a second interconnect (e.g., “bonding pad BP” with “lead wire 32”) having a first interconnect portion (wider portion of “bonding pad BP”) and a second interconnect portion with a smaller width and branching from the first interconnect portion (“lead wire 32” portion of “bonding pad BP”) (TSMC-1006, Fig. 3):



TSMC-1006, ¶[0055], Fig. 3.

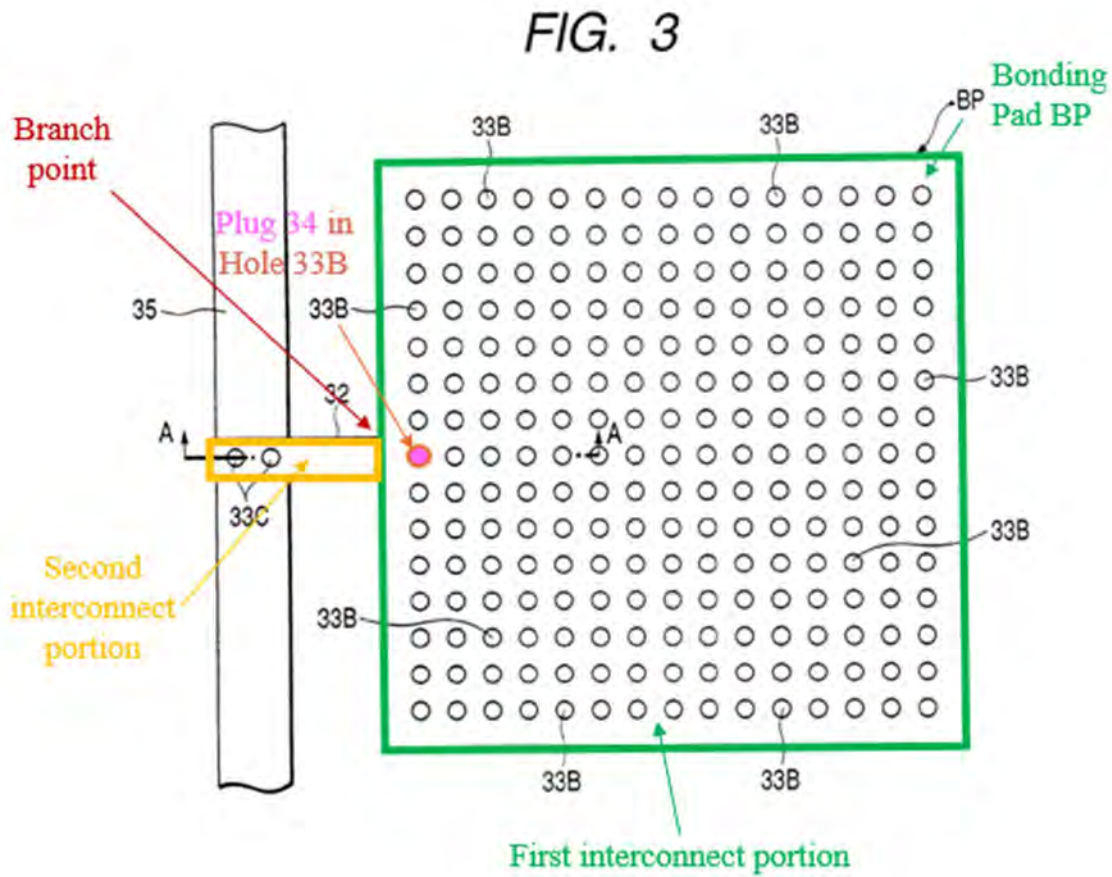
b) [45.b] – “the via is connected to the second interconnect portion”

463. Element [45.b] recites that “the via is connected to the second interconnect portion,” which Aoyagi discloses. As disclosed in annotated Figure 3 below, Aoyagi’s vias (e.g., “plugs 34” formed in “holes 33C”) are connected to the second interconnect portion (e.g., lead wire 32 portion of bonding pad BP) (TSMC-1006, ¶[0054]-[0055], Fig. 3):



5. Claim 46 – “semiconductor device of claim 45, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions”

464. Claim 46 recites that “the dummy via is formed at or near the branch point between the first and second interconnect portions,” which Aoyagi discloses. For example, as shown in annotated Figure 3 below, dummy hole 33B (and thus plug 34 therein) is formed near the branch point between the first and second portions (wider bonding pad BP portion, lead wire 32 portion, respectively) of the second interconnect (bonding pad BP), which satisfies claim 16 (TSMC-1006, Fig. 3):



H. Ground 8: Claim 47 Is Obvious Over Aoyagi and Hasunuma

465. I believe that claim 47 is obvious to a POSITA based on Aoyagi and Hasunuma.

1. Claim 47 – “semiconductor device of claim 45, wherein a width of the second interconnect portion is 0.2 μm or less”

466. Claim 47 recites that “a width of the second interconnect portion is 0.2 μm or less,” which the combination of Aoyagi and Hasunuma renders obvious.

467. Hasunuma teaches the fabrication and use of wiring layers with dimensions of 0.13 μm . TSMC-1005, ¶[0127] (teaching an interconnect wiring width of “about 0.13 μm ”). Hasunuma’s 0.13 μm dimension less than 0.2 μm .

468. A POSITA would have found it obvious to utilize Hasunuma’s width dimension for lead wire 32 of Aoyagi. A POSITA would have understood that the specific sizing (including widths of 0.2 μm or less) of Aoyagi’s “lead wire 32” was a predictable design choice as evidenced, for example, by Hasunuma’s disclosed 0.13 μm width. *Id.* Hasunuma teaches that line widths of less than 0.2 μm for interconnects were well known at the time.

469. Additionally, a POSITA was motivated to minimize the width as much as reasonably possible. For example, Kamoshima discusses benefits associated with a narrow-width interconnect branch, including creating a narrow path to restrict vacancy flow to the active vias (such as those in Aoyagi’s holes 33C). *See* TSMC-

1009, ¶¶[0094]-[0109]. Narrow widths of 0.2 μm or less for an active interconnect was a known way to mitigate such vacancy flow. Aoyagi already teaches a narrow width portion for the lead wire 32 part of bonding pad BP and Hasunuma provides a recognized width size that may be used. Additionally, as discussed above for Ground 4 *supra*, §§X.D, a POSITA understood the benefit of locating dummy vias at the branch point of a narrow interconnect so that the dummy vias would block flow of voids to a real via on the narrow interconnect. A POSITA further recognized that it was easy to block void migration using a dummy via at the branchpoint for interconnect branches with narrow widths of 0.2 μm or less (as compared to those with larger widths), thus further motivating a POSITA to use such a narrow width.

470. Moreover, a POSITA would have had a reasonable expectation of success. Both Hasunuma and Aoyagi disclose manufacturing interconnects using a dual damascene process, and the POSITA recognizes that the minimum width depends on the capabilities of the etching process to form trenches or holes. TSMC-1005, ¶¶[0098], [0101]; TSMC-1006, ¶[0077]. Hasunuma expressly discloses that such widths are viable, and discloses that its conductive layer and plugs and reinforcing plugs and layers can be Al. TSMC-1005, ¶[0294]. Additionally, Aoyagi's bonding pad BP/lead wire 32 is an Al alloy film. TSMC-1006, ¶¶[0050], [0074], [0077], Fig. 19. Narita describes similar Al alloy interconnects with widths less than 0.2 μm , successfully forming such interconnects (also with Ti/TiN layers)

having patterned widths of 0.175 μm . TSMC-1031, ¶¶[0016], [0029]-[0030]. Narita confirms that such dimensions are readily achievable for Aoyagi's lead wire 32 at the time. Thus, a POSITA recognized prior to the '623 patent that patterning an interconnect to have a width of 0.2 μm or less would have succeeded.

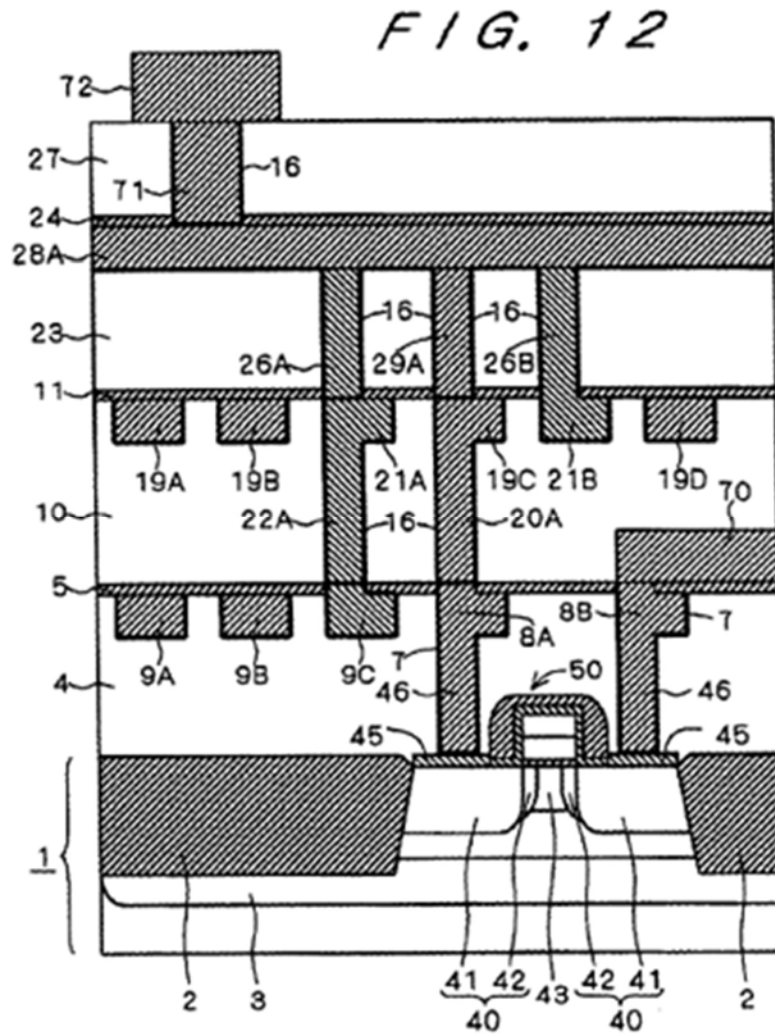
I. Ground 9: Claims 1-2, 4, 7, 14, and 42 are Anticipated and Rendered Obvious by Kunikiyo

471. I believe that Kunikiyo anticipates claims 1-2, 4, 7, 14, and 42, and renders them obvious, as detailed below. I summarized Kunikiyo's teachings previously. *Supra*, §IX.D.

1. Claim 1

a) [1.pre] – “semiconductor device”

472. The preamble of claim 1 calls for a “semiconductor device,” which Kunikiyo discloses, *inter alia*, in the embodiment disclosed by Figure 12:

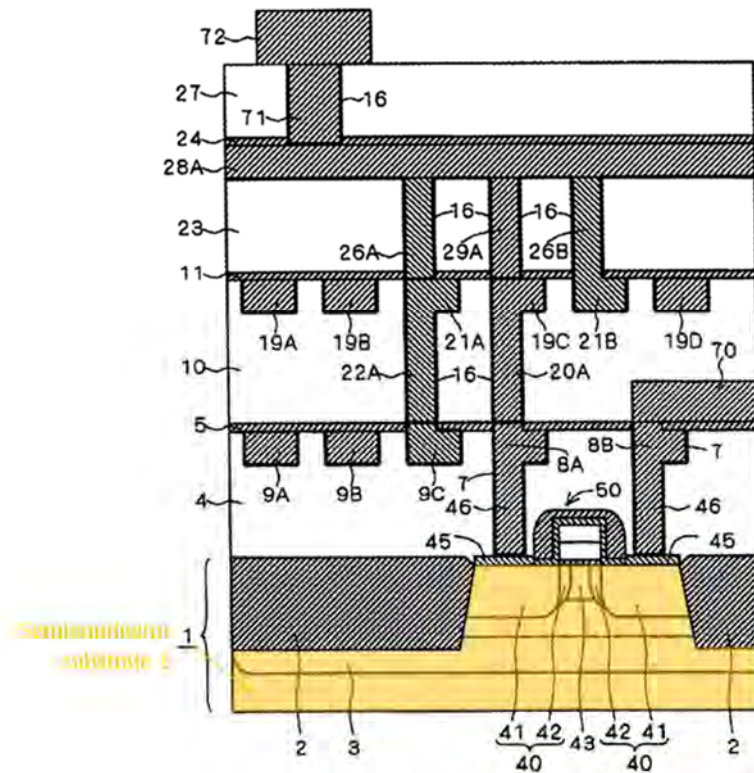


TSMC-1007, 10:50-55, 20:4-24.

b) [1.a] – “a semiconductor substrate”

473. Element 1[a] calls for “a semiconductor substrate,” which Kunikiyo discloses in the form of a silicon substrate, as seen in annotated Figure 12 below:

FIG. 12



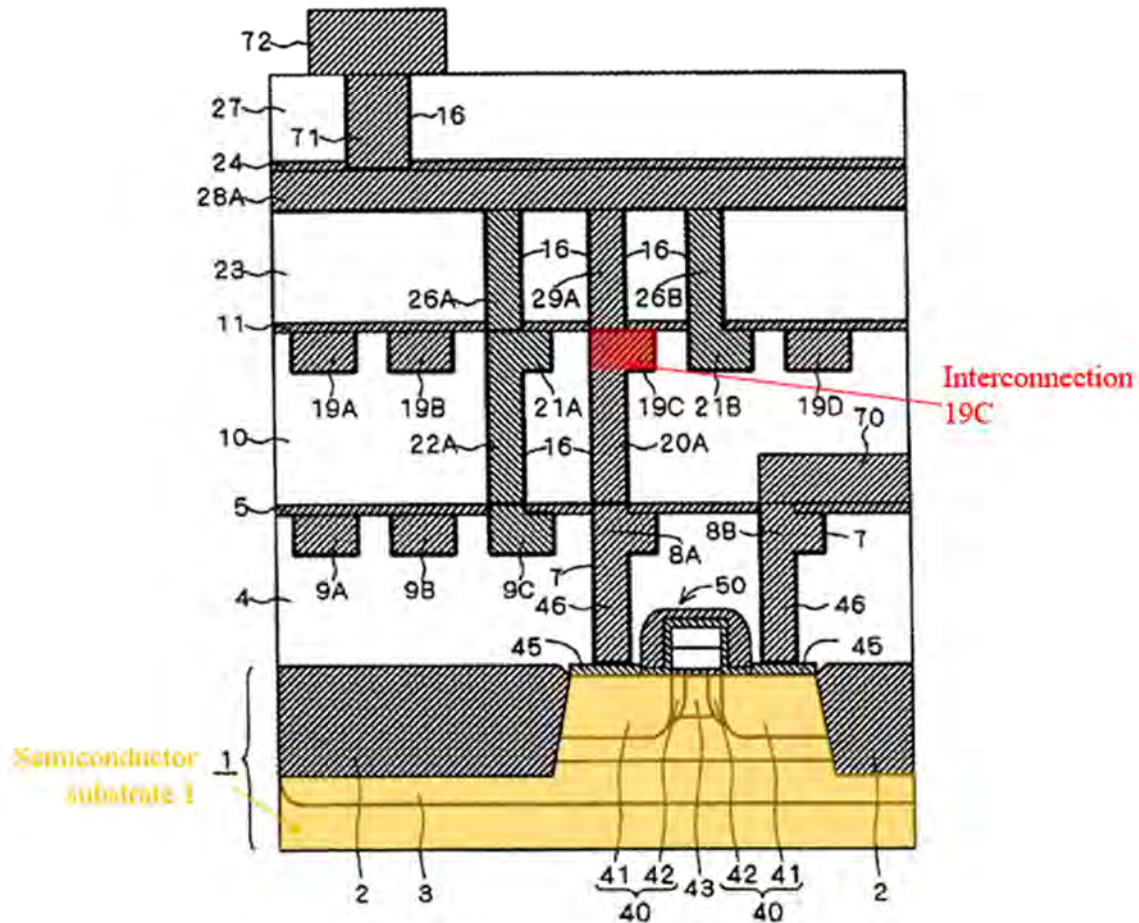
TSMC-1007, 10:50-55, 20:9-11. The shallow trench isolations (“STIs”) identified as item “2” in Figure 12 (*id.*, 10:50-60) could also be considered to be part of the semiconductor substrate, although not highlighted by the annotations herein.

c) [1.b] – “a first interconnect formed on the semiconductor substrate”

474. Element [1.b] calls for “a first interconnect formed on the semiconductor substrate,” which Kunikiyo discloses.

475. The annotations to Figure 12 below show a first interconnect (e.g., “interconnection 19C”) formed on the semiconductor substrate 1:

FIG. 12



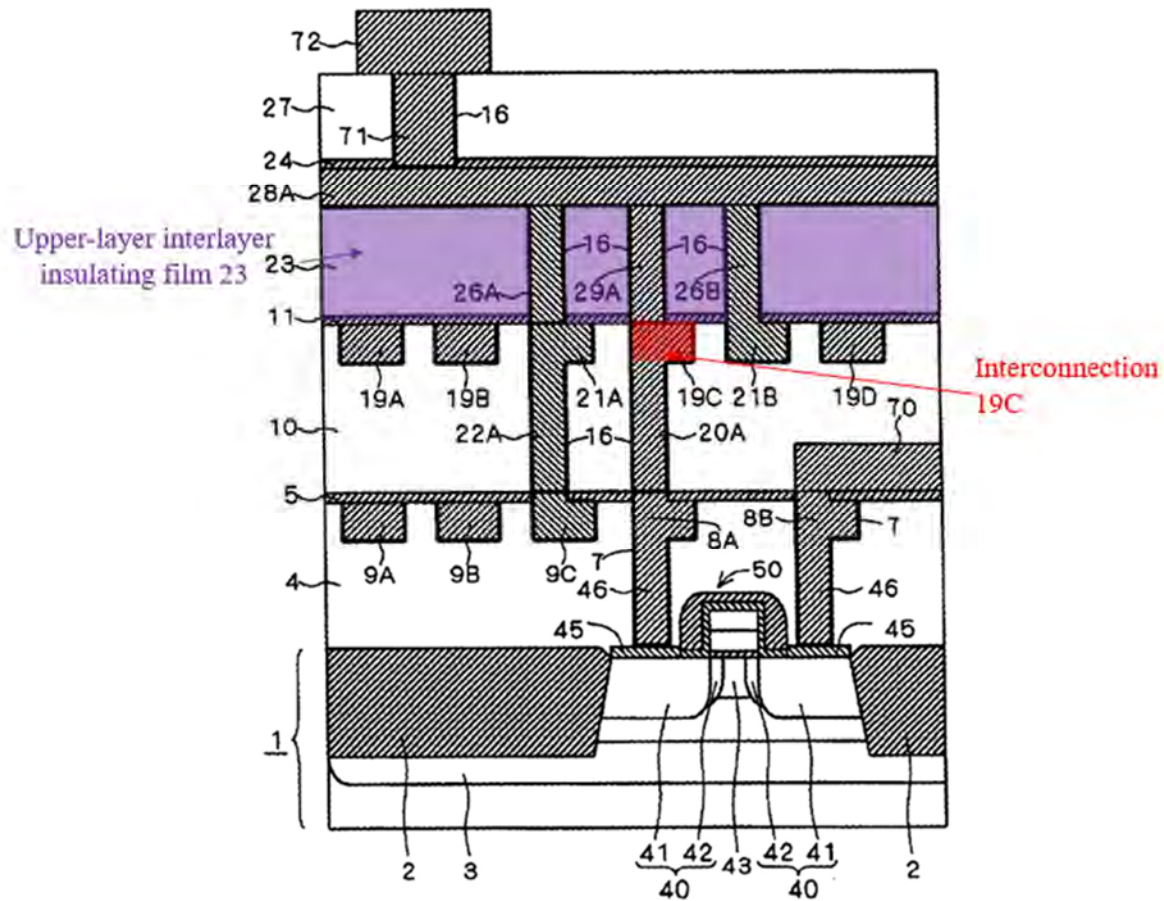
TSMC-1007, 20:15-49, Fig. 12.

d) [1.c] – “a first insulating film formed on the first interconnect”

476. Element [1.c] calls for “a first insulating film formed on the first interconnect,” which Kunikiyo discloses.

477. The annotations to Figure 12 below show a first insulating film (e.g., “upper-layer interlayer insulating film 23”) formed on the first interconnect 19C:

FIG. 12



TSMC-1007, 12:47-51, 20:9-11, Fig. 12. I note that Kunikiyo shows another film 11 right below insulating film 23. Kunikiyo does not expressly describe this film 11 that I can see, but nonetheless, a POSITA would understand that film 11 is another insulating film—if it were instead a conductive film, it would cause a short across all of the interconnects at that level (i.e., just underneath film 11). This is contrary to how a POSITA would understand and interpret Figure 12. A POSITA would understand that film 11 is another insulating film underlying film 11 (it is common

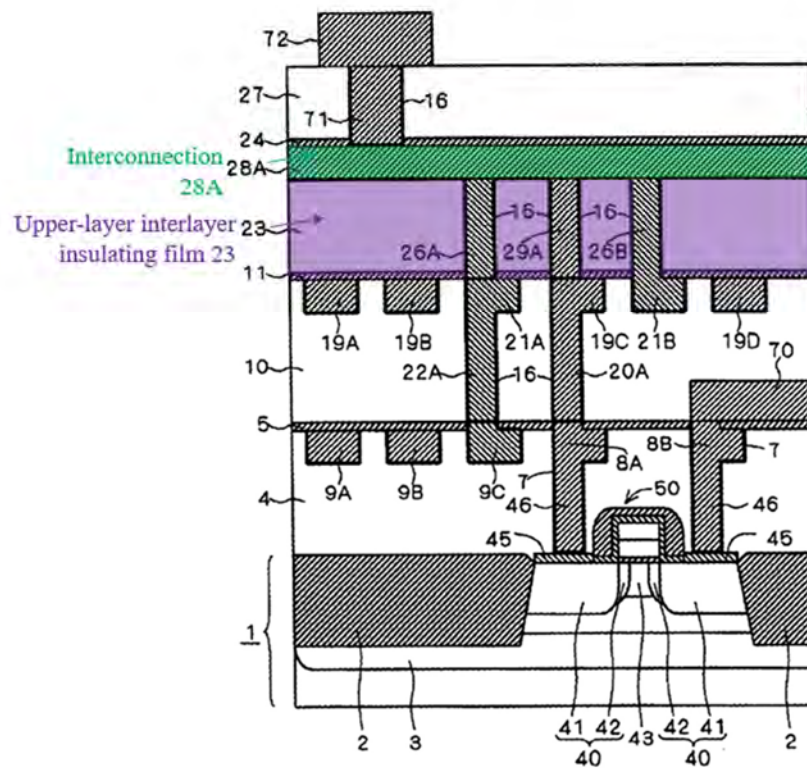
to build insulating films in multilevel stacks). As a result, the “first insulating film” of this claim limitation can include or omit insulating film 11 lying just below film 23.

e) [1.d] – “a second interconnect formed on the first insulating film”

478. Element [1.d] calls for “a second interconnect formed on the first insulating film,” which Kunikiyo discloses.

479. The annotations to Figure 12 below show a second interconnect (e.g., “interconnection 28A”) formed on the first insulating film 23:

FIG. 12



TSMC-1007, 12:47-51, 20:9-24.

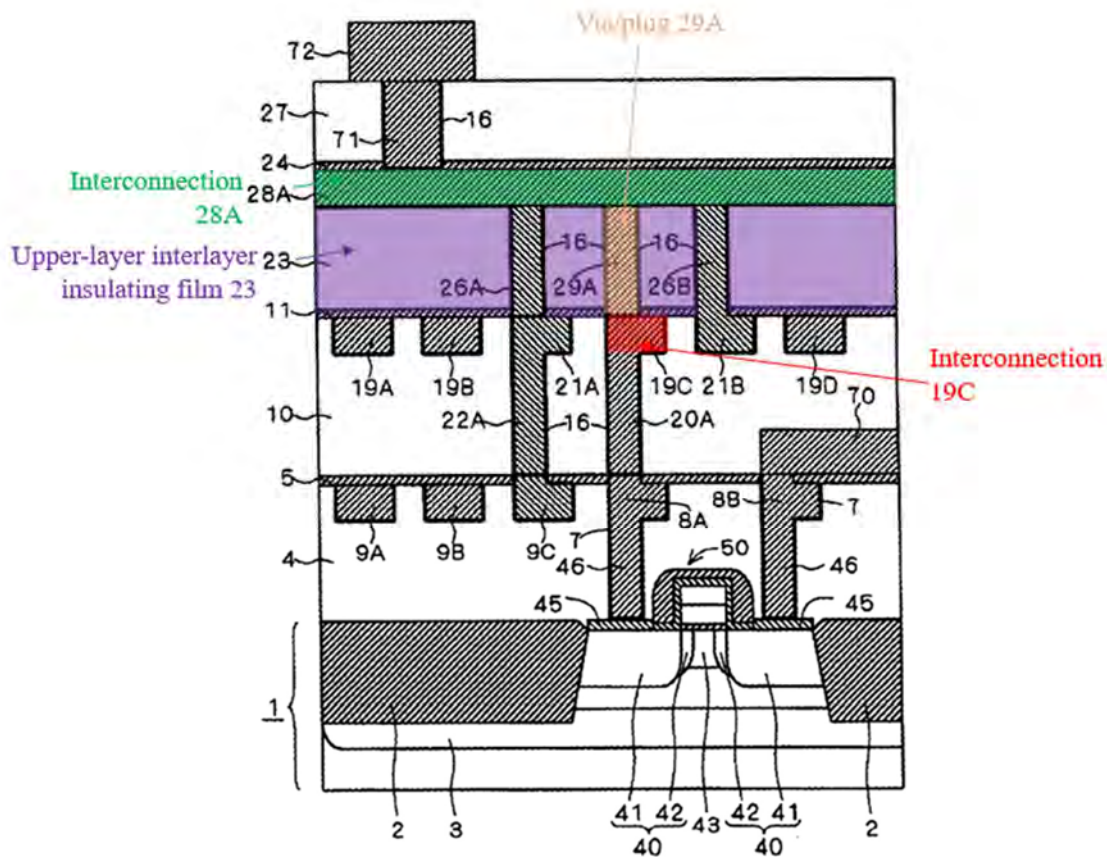
480. As I noted in regard to element [1.c] above, in the context of Figure 12, a POSITA would have understood film 11 to also be an insulating film, like film 23. This is because if film 11 were conductive, it would short together many of the interconnects and the device would not operate properly. Furthermore, it was common to employ multi-layered insulating films, such as films 11 and 23 shown here, in the manufacture of semiconductor devices. For example, a POSITA would find it very likely that film 11 is a SiN film, which is a common insulating film used for etch stops and other purposes, while film 23 is another insulating film chosen more so for its dielectric properties. While film 11 is included in the “first insulating film” annotations, film 11 could be omitted from the claimed “first insulating film” and my entire analysis regarding Kunikiyo herein would not change.

f) [1.e] – “*a via formed through the first insulating film and connecting between the first and second interconnects*”

481. Element [1.e] calls for “a via formed through the first insulating film and connecting between the first and second interconnects,” which Kunikiyo discloses.

482. The annotations to Figure 12 below show a via (e.g., “plug 29A”) formed through the first insulating film (e.g., layers 23 and 11), and connecting first interconnection 19C and second interconnection 28A:

FIG. 12



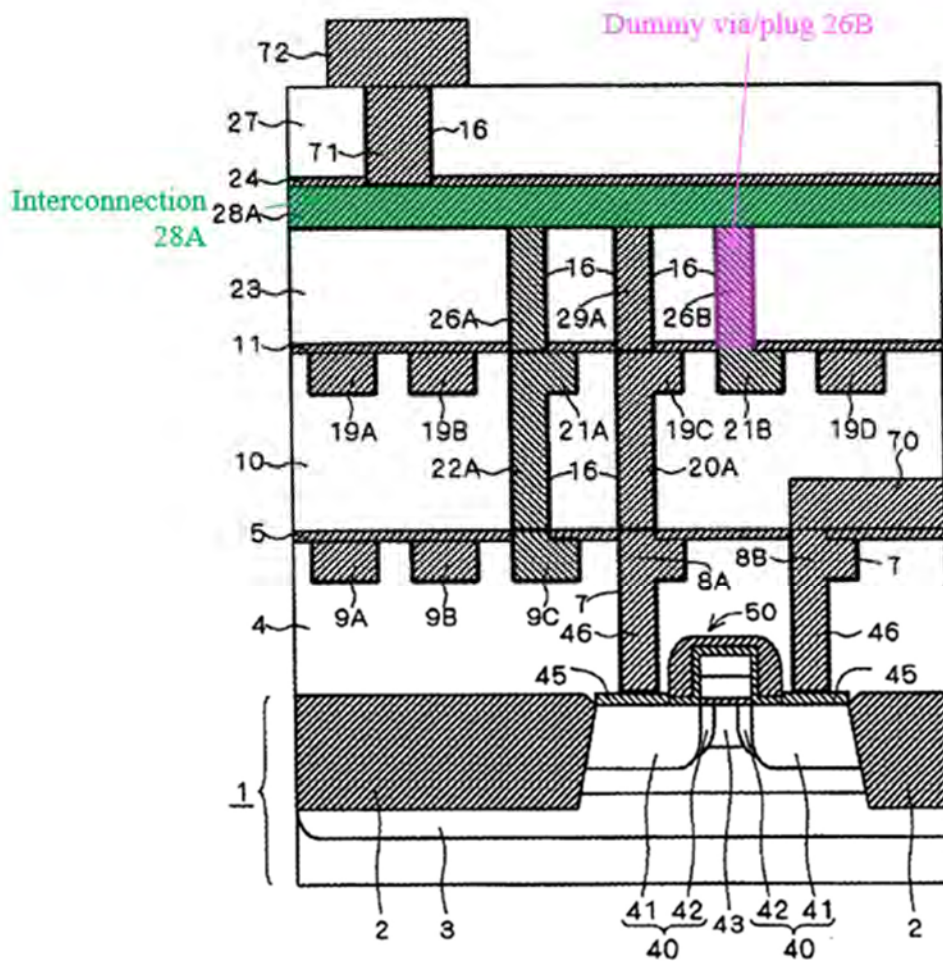
Id., 12:47-51, 20:9-19. Exemplifying the formation of a lower level of the semiconductor device, Kunikiyo's Figures 3-6 show the general process by which via holes are formed in an insulating layer and then filled with conductive material for form the vias (and interconnects). *Id.*, Figs. 3-6. A POSITA would have understood that via plug 29 is manufactured the same way as the via/plug formation is illustrated in Figures 3-6.

g) [1.f] – “a dummy via connected to the second interconnect”

483. Element [1.f] calls for “a dummy via connected to the second interconnect,” which Kunikiyo discloses.

484. The annotations to Figure 12 below show a dummy via (e.g., “dummy plug 26B”) connected to the second interconnect 28A:

FIG. 12



TSMC-1007, 12:47-51, 20:32-34. Figure 12 discloses other dummy vias as well, such as dummy via 26A, which is also connected to the second interconnect 28A.

Id.

485. A POSITA would have understood that the structures 26A and 26B represent “dummy” vias not only because Kunikiyo describes them as such, but also because they connect only to other dummy interconnects at one end. *Id.*, 20:25-37. For example, the lower end of dummy via 26B in Figure 12 connects to structure 21B, which Kunikiyo describes as a dummy interconnection. *Id.* Kunikiyo expressly teaches that:

A dummy interconnection is an interconnection which is not directly related to the circuit operation of the semiconductor device and whether they are present or absent makes no difference on the circuit diagram of the semiconductor device.

Id., 25:59-63.

486. Notably, just like Kunikiyo, the '623 patent's Figures 2A-2B show dummy via 102B connected to an active interconnect 111 at its upper end, and a dummy interconnect 102B at its lower end. Like Kunikiyo, the '623 patent explains:

[N]either the dummy interconnect 102B nor the dummy via 110B constitutes a closed circuit in actual use. That is, even if the dummy interconnect 102B and the dummy via 110B are omitted in the interconnection structure shown in FIG.2B, a device with this

interconnection structure is operable at least immediately after fabrication.

TSMC-1001, 9:66-10:32.

487. Thus, Kunikiyo's dummy vias, such dummy via 26B, are configured exactly the same as the "dummy vias" in the '623 patent.

h) [1.g] – *“wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough”*

488. Element [1.g] calls for “wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough,” which Kunikiyo discloses.

489. First, Kunikiyo's dummy vias 26A and 26B are each made of copper, which is a conductive film. TSMC-1007, 12:7-51, Figs. 3-6, 12. Specifically, Kunikiyo's Figures 4-6 illustrate a dual damascene process, where through holes 12, interconnect trenches 14, and dummy interconnect trenches 15 are filled with a barrier metal 16 and then copper 17. *Id.*, 11:37-12:41. Kunikiyo teaches that “the dual damascene method is performed again, thus forming upper-layer interconnections 25 (25a, 25b) ... and plugs 26 (26a to 26c) ... in the upper-layer interlayer insulating film 23.” *Id.*, 12:47-51. A POSITA would thus have

understood that dummy plugs 26A and 26B (“dummy vias”) are made of copper (i.e., “conductive film”) when the dual damascene method “is performed again.”

490. Second, Kunikiyo’s dummy structures, including dummy vias 26A and 26B, are arranged so as to be incapable of having current flow therethrough as part of the semiconductor device’s intended circuit operation. *Id.*, 5:46-50, 14:31-33, 25:54-26:9. Such dummy structures, by their stated definition and purpose in Kunikiyo, do not carry current for operating the semiconductor elements like MOSFETs. *Id.*, 5:46-50, 14:31-33, 25:54-26:9. For example, Kunikiyo explains that:

A dummy interconnection is an interconnection which is not directly related to the circuit operation of the semiconductor device and whether they are present or absent makes no difference on the circuit diagram of the semiconductor device.

Id., 25:59-63. This is exactly how the ’623 patent describes its dummy structures. TSMC-1001, 10:26-32.

491. A POSITA would have understood that Kunikiyo’s dummy vias do not contribute to the function of the MOSFET device, because one end always connects only to other dummy interconnects/dummy vias. Both ends of Kunikiyo’s dummy vias never connect to other elements that actively participate in circuit operation. As noted in the quote from Kunikiyo above, Kunikiyo’s device would be operable even

if Kunikiyo's dummy vias (or dummy interconnects) were omitted. TSMC-1007, 25:59-63; *cf.* TSMC-1001, 3:14-18; 10:26-32.

492. Moreover, plan #1 in Kunikiyo's Figure 13 describes an electrical configuration that maintains an equipotential state across dummy vias 26A and 26B, resulting in no current flow through them. TSMC-1007, 20:25-49, Figs, 12-13. This plan specifies that the main interconnection 19C and its adjacent dummy interconnections, 21A and 21B, are all held at the same higher power-supply potential, V_{DD} . *Id.* In the device structure of Figure 12, dummy via 26A connects dummy interconnection 21A to the common (active) interconnection 28A, and dummy via 26B connects dummy interconnection 21B to dummy vias 26A and 26B. *Id.* Since both dummy interconnections 21A and 21B, as well as interconnection 28A, are all at the V_{DD} potential, both ends of both dummy vias 26A and 26B are connected to points that are maintained at the identical V_{DD} potential. Because electrical current only flows when there is a potential difference, and because this difference is zero across the dummy plugs 26A and 26B in this arrangement, no current flows through them during operation.

493. For all of these reasons, a POSITA would understand that Kunikiyo's dummy vias, such as dummy vias 26A and 26B, are arranged so as to be incapable of having current flow through them. Simply put, they lead to "dead ends" in the interconnect structure (e.g., never forming connections between two active elements

such as an external electrode and a MOSFET source or drain, for example) such that there is no place for current to flow to or from. And they are also arranged identically to the dummy vias described in the '623 patent (e.g., dummy via 110B in the '623 patent's Figure 2A).

- i) [1.h]/[1.i] – *“the second interconnect and the via form a dual damascene structure”/“the second interconnect and the dummy via from a dual damascene structure”*

494. Element [1.h] calls for “the second interconnect and the via form a dual damascene structure,” and element [1.i] calls for “the second interconnect and the dummy via from a dual damascene structure.” Kunikiyo discloses dual damascene structures for both its second interconnect and via, and its second interconnect and dummy via.

495. Specifically, Kunikiyo discloses using the dual damascene process for forming its interconnects and vias/dummy vias. TSMC-1007, 11:48-12:51, 20:15-24, Figs. 3-7, 12. Figures 3-6 detail the steps in this process for an exemplary level lower in the overall interconnect structure, showing the formation of through holes 12 and interconnection trenches 14, which are then filled with barrier metal 16 and copper 17, as illustrated by the annotations below:

FIG. 4

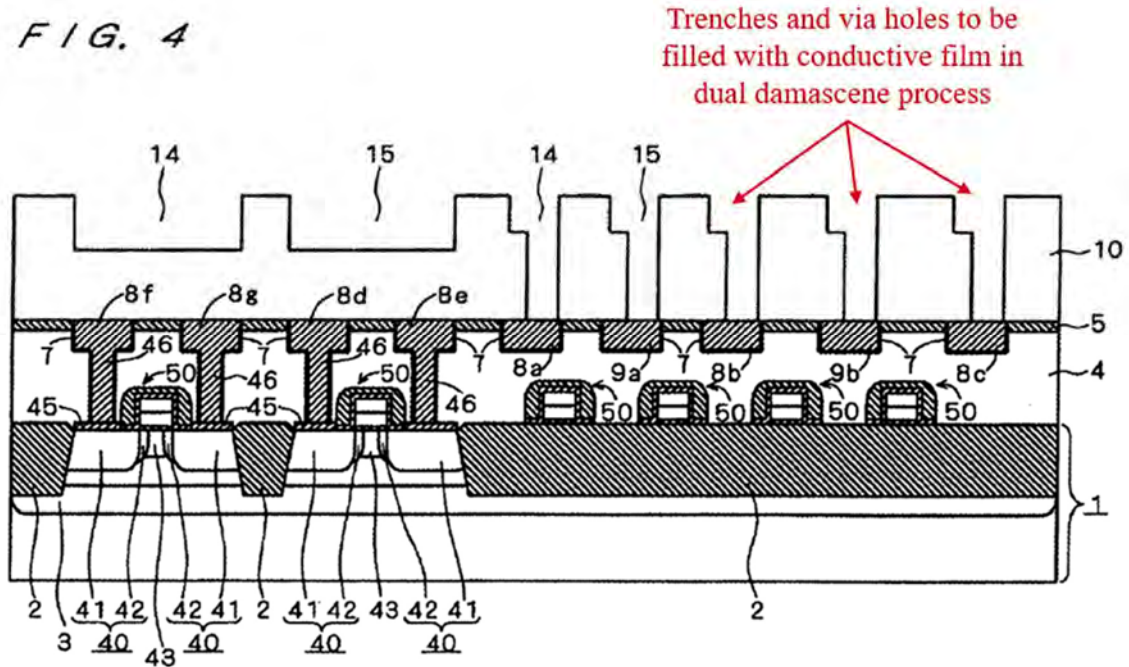
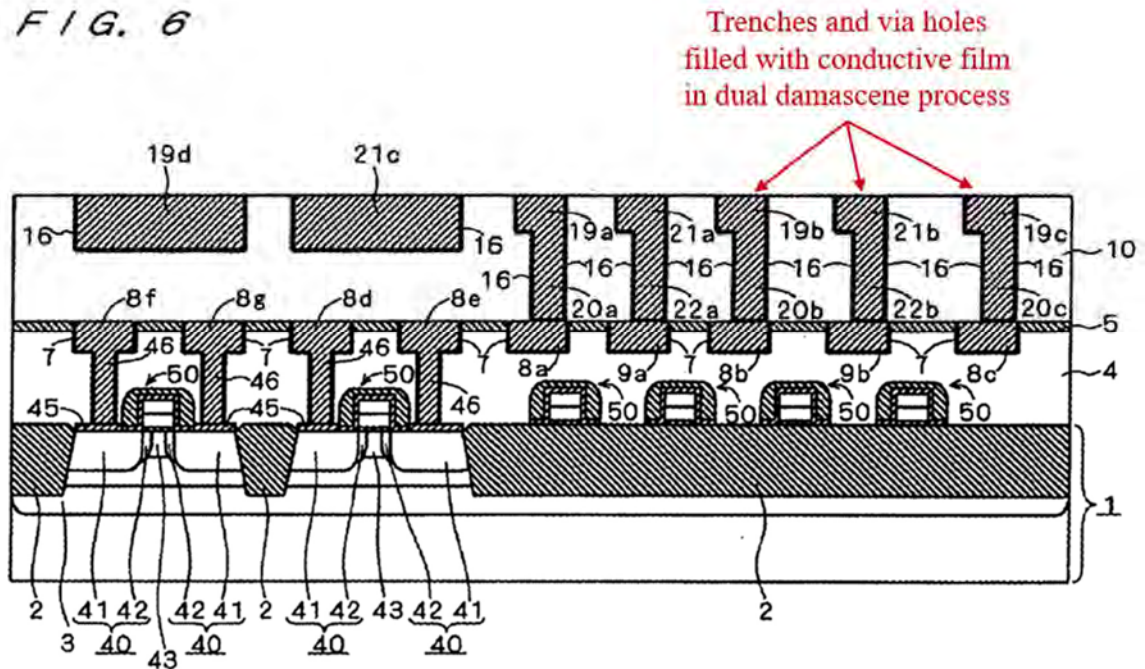


FIG. 6



Id.

496. Kunikiyo then states, “[i]n the process step of FIG. 7, the dual damascene method is performed again, thus forming upper-layer interconnections

25 (25a, 25b), 28 (**28a** to 28d) and plugs 26 (**26a to 26c**), 29 (**29a** to 29c) in the upper-layer interlayer insulating film 23.” *Id.*, 12:47-51.

497. In introducing its Figure 12 embodiment, Kunikiyo states that Figure 12 corresponds to the first embodiment but shows an additional connection between dummy conductors and a ground interconnection not included in the first embodiment of Figure 7. *Id.*, 20:4-14. Reading the passage regarding fabrication of the Figure 7 embodiment in conjunction with the introduction to the Figure 12 embodiment, a POSITA would have understood that Figure 12’s via 29A, dummy vias 26A and 26B, and second interconnect 28A are among the upper-layer structures formed by this “repeated” dual damascene process, as noted by the bold highlighting above showing the relevant numbering for the relevant features in the Figure 12 embodiment. *Id.*, 12:47-51, 20:15-24, Fig. 12. Indeed, structures 28A and 29A only appear in Kunikiyo’s Figure 12 and 14 embodiments, such that Kunikiyo’s passage at column 12, lines 47-51 quoted above must be inclusive of Figure 12.

498. A POSITA would thus have understood from Kunikiyo’s express description of its manufacturing process that via 29A, dummy vias 26A and 26B, and second interconnection 28A in the Figure 12 embodiment are formed simultaneously using this dual damascene technique, where the trench for second interconnect 28A and the holes for via 29A and dummy vias 26A and 26B are patterned in the first insulating film 23 and then filled with conductive material

(barrier metal 16 and copper 17) in the same deposition step, followed by a planarization/CMP step.

499. Kunikiyo's dual damascene fabrication process results in second interconnect 28A and via 29A forming a dual damascene structure, and second interconnect 28A and dummy via 26B (or dummy via 26A) likewise forming a dual damascene structure, thereby meeting Elements [1.h] and [1.i].

500. In addition, it would have been obvious to a POSITA to form Kunikiyo's second interconnect and via, and its second interconnect and dummy via, as copper-based dual damascene structures, just as it does for the interconnects and vias/dummy vias elsewhere in the structure. *See* TSMC-1007, 11:48-12:51, 20:9-24, Figs. 3-6. As I described previously in regard to Aoyagi (*supra*, §X.G.2.(i)), a POSITA would have been motivated to use the copper-based dual damascene process to form the second interconnect 28A, via 29A, and dummy vias 26A and 26B given the well-known benefits of dual damascene processing, including increased fabrication/manufacturing efficiency and reduced cost afforded by forming the vias/dummy vias and interconnects simultaneously rather than serially. *Supra*, §§VI.A, IX.C, X.G.1. Additionally, a POSITA would have easily implemented such a process and would have expected success given its already disclosed use in Kunikiyo (and widespread use throughout industry at the time given its associated, well-known benefits). *See* TSMC-1007, 11:48-12:51, 20:9-24, Figs.

3-6; *see also* TSMC-1016, 1:47-52; TSMC-1017, 1:52-57; TSMC-1018, 129; TSMC-1019, Abstract. Kunikiyo thus both anticipates claim 1 and renders it obvious.

2. Claim 2

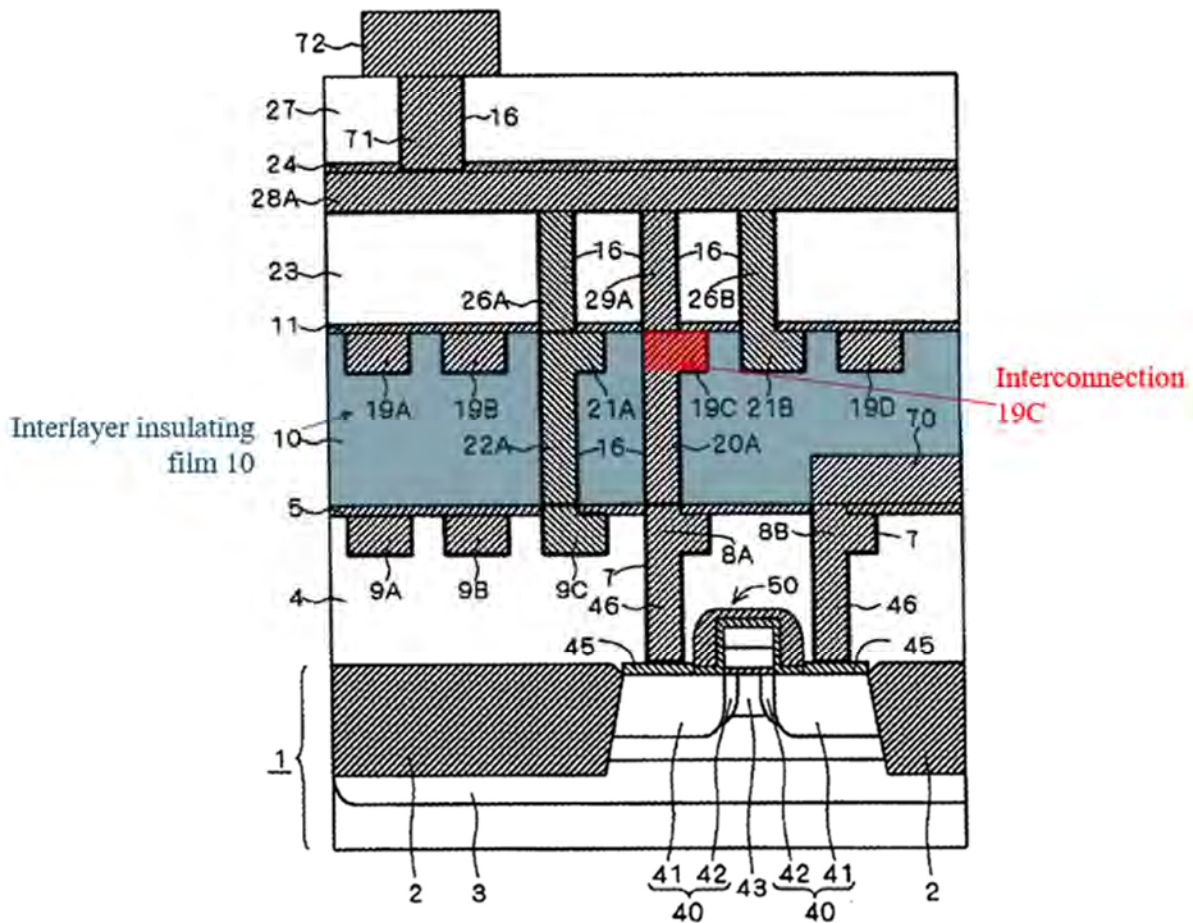
a) [2.a] – “*semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate*”

501. Element [2.a] recites the “semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,” which Kunikiyo discloses.

502. The annotations to Kunikiyo’s Figure 12 below show a second insulating film (e.g., “interlayer insulating film 10”) formed on semiconductor substrate 1:

504. The annotations to Kunikiyo's Figure 12 below show that the first interconnect (e.g., interconnection 19C) is formed on the second insulating film (interlayer insulating film 10):

FIG. 12



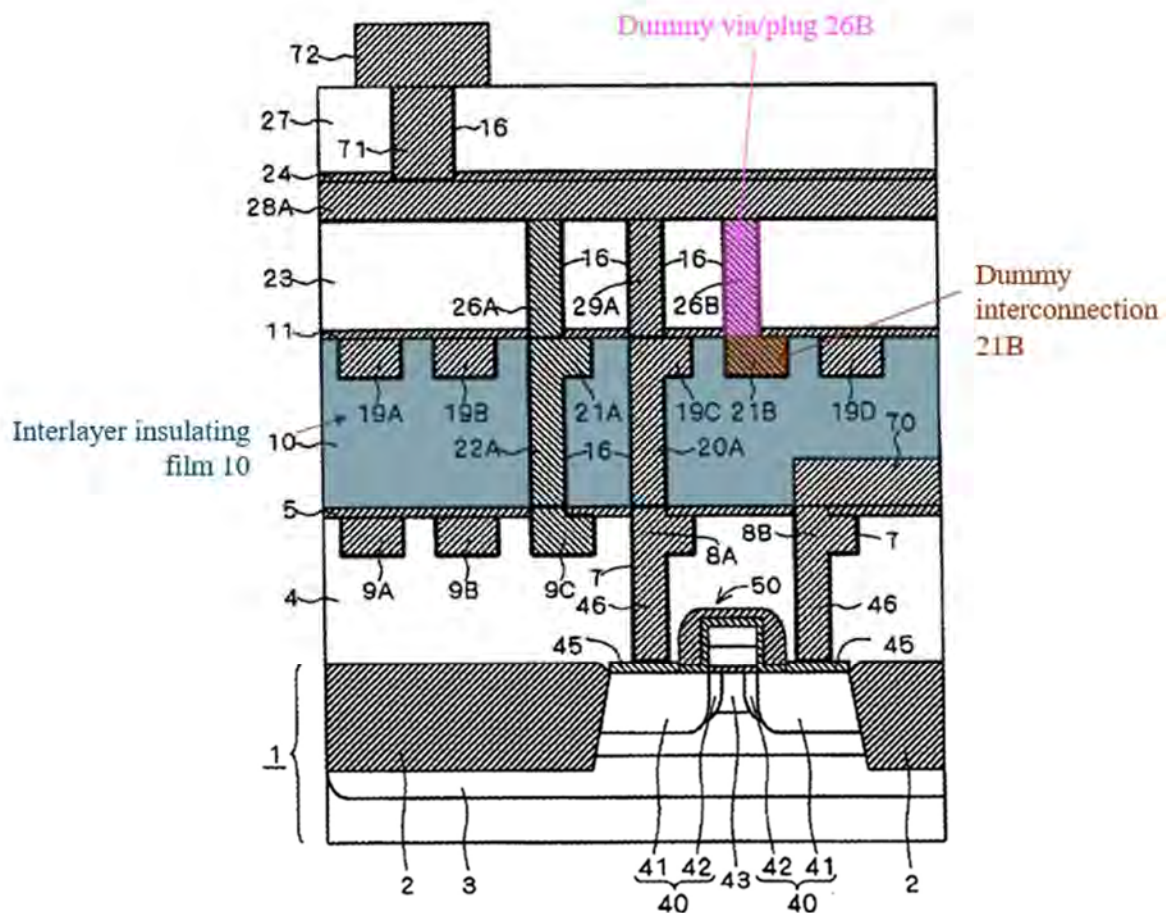
TSMC-1007, 11:38-12:30; 20:15-24.

c) [2c] – “*the dummy via is connected to a first dummy interconnect formed on the second insulating film*”

505. Element [2.c] calls for “the dummy via is connected to a first dummy interconnect formed on the second insulating film,” which Kunikiyo discloses.

506. The annotations to Figure 12 below show a first dummy interconnect 21B that is formed on second insulating film (interlayer insulating film 10), and that that dummy via 26B is connected to first dummy interconnect 21B:

FIG. 12



TSMC-1007, 20:25-37. Although not highlighted with annotations above, Figure 12 also shows that dummy via 26A is connected to dummy interconnection 21A formed on second insulating film 10.

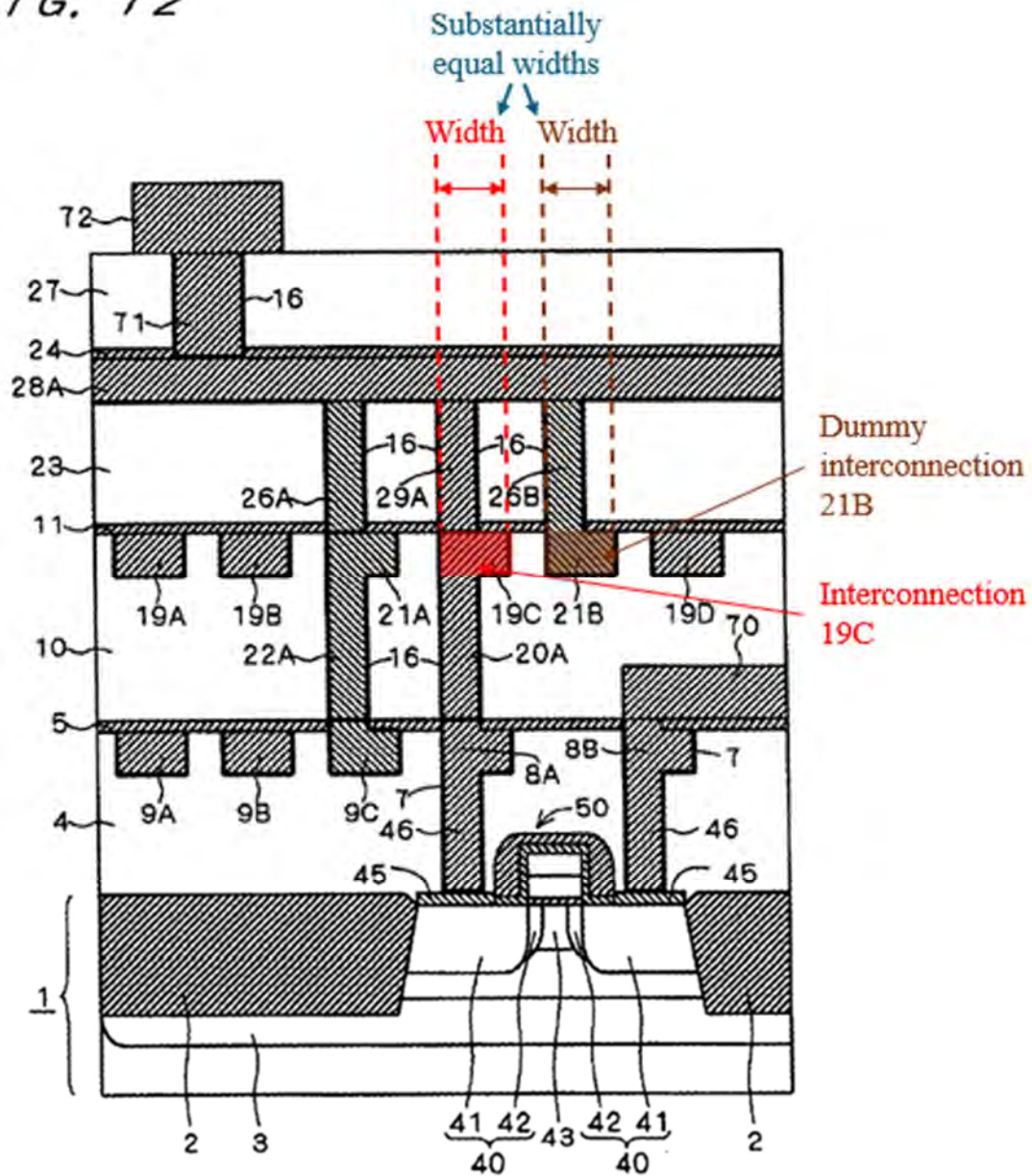
507. Kunikiyo describes structures 21A and 21B as “dummy interconnections” (*id.*, 20:29-32) and a POSITA would understand them to be “dummy” interconnects as called for in the claims of the ’623 patent for the same reasons as previously explained for dummy vias 26A and 26B (*supra*, §X.I.1.(g)-(h)).

3. Claim 4 – “semiconductor device of claim 2, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other”

508. Claim 4 recites the “semiconductor device of claim 2, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other,” which Kunikiyo discloses.

509. The annotations to Kunikiyo’s Figure 12 below show that the first interconnect (interconnection 19C) and the first dummy interconnect (dummy interconnection 21B) have identical widths:

FIG. 12



TSMC-1007, 11:48-56, 20:7-34, Fig. 12. Interconnection 19C and dummy interconnection 21B are shown as identically sized lines formed in the same layer (interlayer insulating film 10) and are only distinguished by their function. *Id.*, 20:7-34, Fig. 12.

510. A POSITA would have appreciated that Kunikiyo's figures are intended to show the relative widths of the structures shown therein. For example, Kunikiyo describes how its Figure 9 specifically shows the alternating widths of interconnect 25B. *Id.*, 15:11-35. Specifically calling out features that have different dimensions and showing them as such in the figures indicates to a POSITA that other features drawn with the same or different widths were intentionally drawn that way and intended to disclose such identical or different widths. Stated another way, when Kunikiyo wanted to show structures having different widths, as evidenced by certain discussions in the specification, it showed them as such in its figures. This reinforces a POSITA's understanding that Kunikiyo's structures having identical widths in the figures were intended to convey that the features did in fact have the same widths, as is the case with interconnect 19C and dummy interconnect 21B in Figure 12.

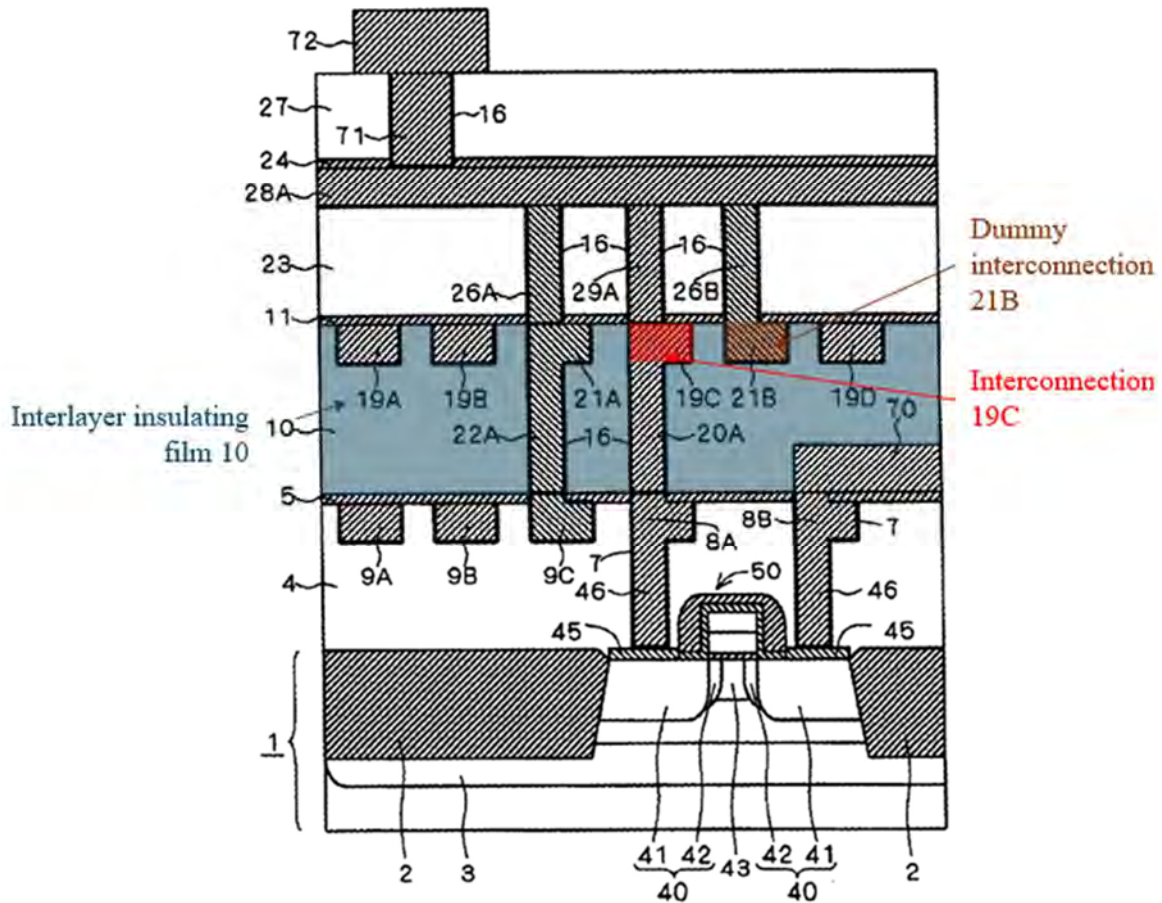
4. Claim 7 – “semiconductor device of claim 2, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film”

511. Claim 7 recites the “semiconductor device of claim 2, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film,” which Kunikiyo discloses.

512. The annotations to Kunikiyo's Figure 12 below show the first interconnect (interconnection 19C) and the first dummy interconnect (dummy

interconnection 21B) buried in an upper portion of the second insulating film (interlayer insulating film 10):

FIG. 12



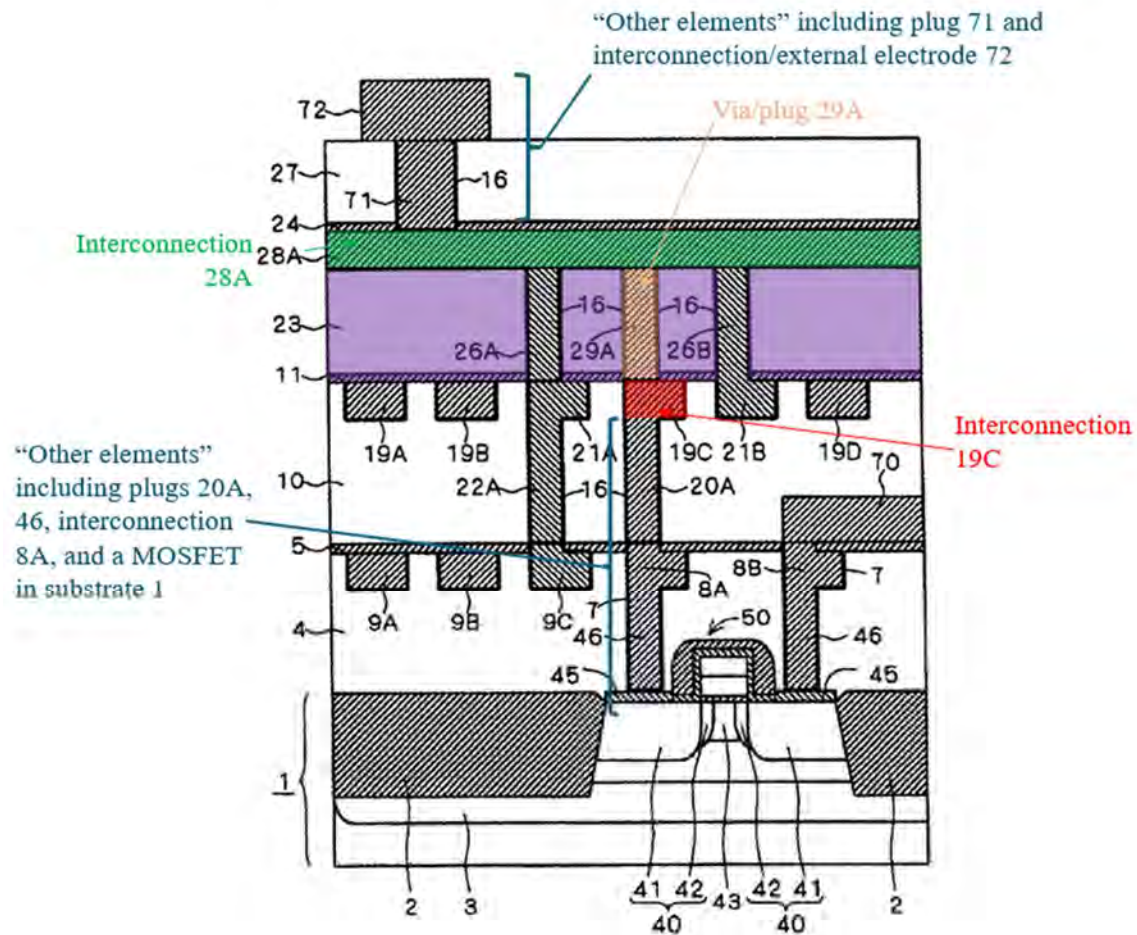
TSMC-1007, 11:48-56, 20:7-34, Fig. 12. The interconnection 19C and the dummy interconnection 21B are positioned at the top of the interlayer insulating film 10, directly beneath the next layer, which places them in the “upper portion” of interlayer insulating film 10. *Id.*, 11:36-12:30, 20:7-34, Fig. 12.

5. Claim 14 – “*semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode*”

513. Claim 14 recites the “semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode,” which Kunikiyo discloses.

514. Kunikiyo’s Figure 12 discloses a first interconnect (interconnection 19C) and a second interconnect (interconnection 28A) that are both connected to “another element or an external electrode.” Such “other elements” include plugs 20A, 46, and 71, and interconnections 8A and 72; interconnection 72 could also be considered an external electrode. The first and second interconnects are also connected to the MOSFET device built into the semiconductor substrate, e.g., elements 40, 41, 42, 43, 45, etc. The connections between Kunikiyo’s first and second interconnects and “other elements” can be seen in Kunikiyo’s Figure 12, as annotated below:

FIG. 12



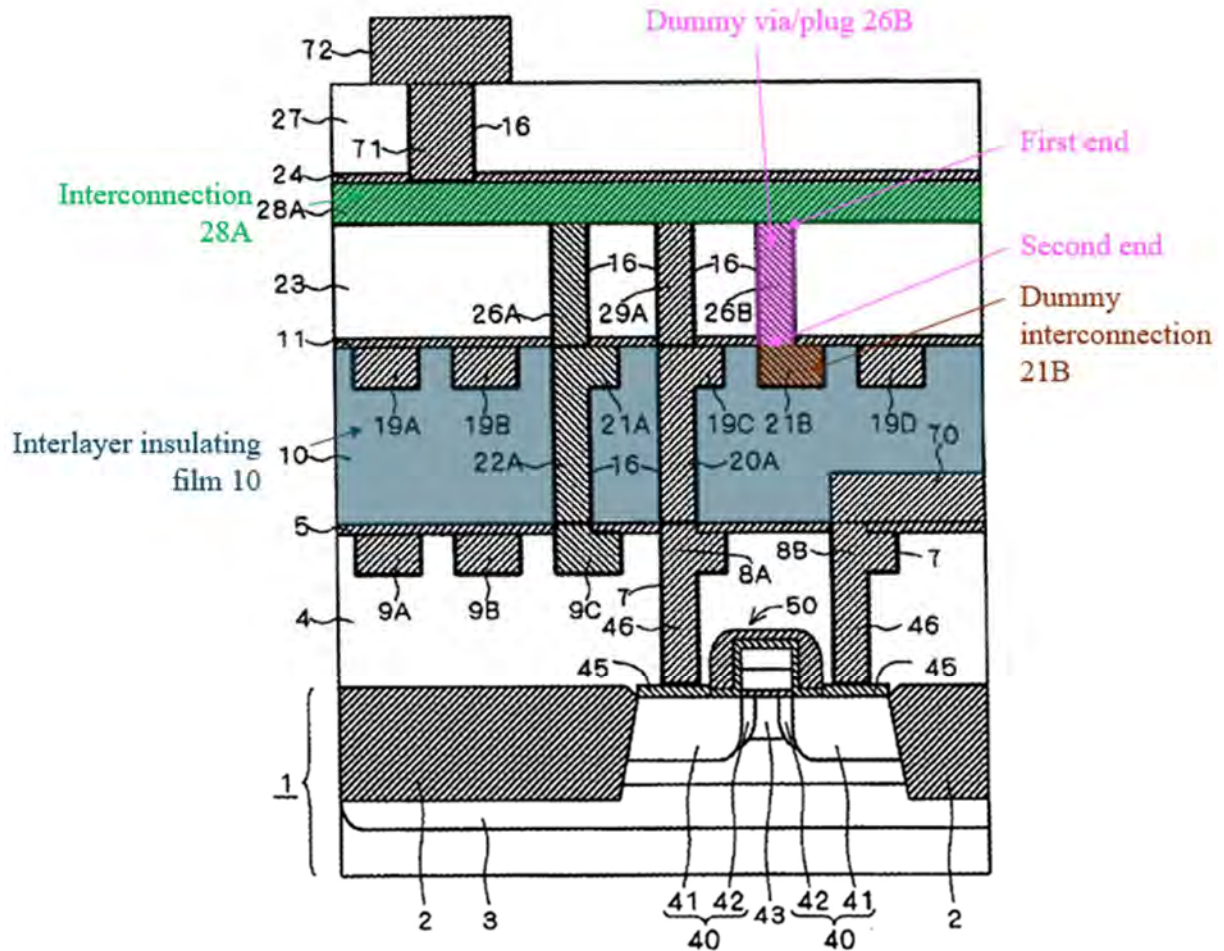
TSMC-1007, 10:50-14:67, 20:4-21:21, Figs, 12, 14. I note that if Kunikiyo's first and second interconnects were not connected to other elements, such as external electrodes and/or the MOSFETs or similar structures in the substrate, then the device would not function or have a purpose, so a POSITA would appreciate that these connections exist and have a purpose.

6. Claim 42 – “*semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film*”

515. Claim 42 recites the “semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film,” which Kunikiyo discloses.

516. The annotations to Kunikiyo’s Figure 12 below show the dummy via (dummy plug 26B) as a vertical conductive structure with a top (first) end and a bottom (second) end, where a top end of dummy plug 26B is connected to the second interconnect (interconnection 28A), and a bottom end is connected to the first dummy interconnect (dummy interconnection 21B):

FIG. 12



As shown above, dummy interconnection 21B is buried within, and therefore surrounded by, the second insulating film (interlayer insulating film 10). TSMC-1007, Fig. 12.

J. Ground 10: Claims 9 and 17 Are Obvious Over Kunikiyo and Iizuka

517. I believe that claims 9 and 17 are obvious to a POSITA in view of Kunikiyo and Iizuka. I discussed how Kunikiyo discloses claims 1 and 2, and Iizuka, previously. *Supra*, §§X.I.1-2.

1. Claim 9

a) [9.a] – “semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view”

518. Element [9.a] recites the “semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view,” which Kunikiyo and Iizuka render obvious.

519. Iizuka teaches common cross-sectional shapes for vias: “the opening of the via-hole may have any configuration, such as a square, rectangle or circle,” and a circular/square pattern means the resulting via formed in a circular/square hole would have a substantially circular/square shape. TSMC-1008, 9:44-47, 10:17-22. Consistent with Iizuka’s teachings, that vias would be manufactured with any of a variety of cross-sectional shapes, specifically including circular cross-sectional shapes, was well known to a POSITA at the time. *See, e.g.*, TSMC-1005, ¶¶[0200], [0209], Figs. 19A, 22A (disclosing circular dummy vias); TSMC-1013, 8:47-52 (noting that vias may have circular cross-sectional shapes); TSMC-1014, ¶¶[0091] (teaching circular vias as a default shape).

520. It would have been obvious based on the teaching in Iizuka to make the dummy plug 26B (“dummy via”) in Kunikiyo substantially circular in a plan view because Iizuka explains that a circular via was a known design option, as the other prior art cited in the preceding paragraph likewise confirms. A POSITA would have viewed a circular cross-sectional shape as among a finite number of common, interchangeable design choices, expressly taught by Iizuka and within a POSITA’s general understanding, as evidenced above. It would have been obvious based on this reasoning alone to make a planar cross-sectional shape of Kunikiyo’s dummy plug 26B (“dummy via”) circular because, as Iizuka confirms, circular-shaped vias were a known design option.

521. In addition, vias/dummy vias having a circular cross-sectional shape provided for greater manufacturing process control (e.g., more uniform etching and filling characteristics for circular shapes compared to sharp-cornered squares), more favorable stress distribution around a circular opening, and design simplicity. *See, e.g.,* TSMC-1038, 7:62-67 (teaching that vias with circular cross-sections benefit from more precisely controlled etching, improved coverage of barrier metal in the via opening, and easier fill-in of the via opening with a metal film). Circular-shaped vias also provide improved reliability due to the lack of sharp corners that can concentrate stress and cause damage in the form of dielectric cracking and the like.

522. While there can sometimes be operational or design considerations that lead to a preference for circular or square vias, a POSITA nonetheless recognized that the fundamental function of Kunikiyo's dummy vias (*see, e.g.*, TSMC-1007, 5:46-54, 12:31-36, 14:31-36, 25:54-26:9) in terms of enhancing the uniformity of interconnection density and manufacturability, improving surface flatness for processing steps like CMP, and providing electrical shielding, would all be realized using circular-shaped dummy vias (as would the electrical-connection function of Kunikiyo's active vias). This is because these functions do not depend on the exact cross-sectional shape of the via/dummy via. In this regard, I note that the '623 patent teaches no criticality or surprising or unexpected results with respect to the cross-sectional shape of its vias or dummy vias, reinforcing my opinion that such shapes were nothing more than a matter of routine design choice.

523. Further, because a POSITA was aware of the basic via shapes, and was aware of the role of the dummy vias in providing process uniformity (*supra*, §IX.D) as well as reducing stress-induced voiding and electromigration problems as taught, for example, by Watanabe (*supra*, §IX.A), it would have been a matter of routine optimization to choose the via shape that works best for a given overall design while optimizing characteristics like etching and filling characteristics, and the tendency to concentrate or dissipate mechanical stresses, for example. With a few basic shapes to choose from (e.g., circular, square, rectangular), it would not have required

an undue amount of experimentation to arrive at the optimal via shape – both for active vias and dummy vias.

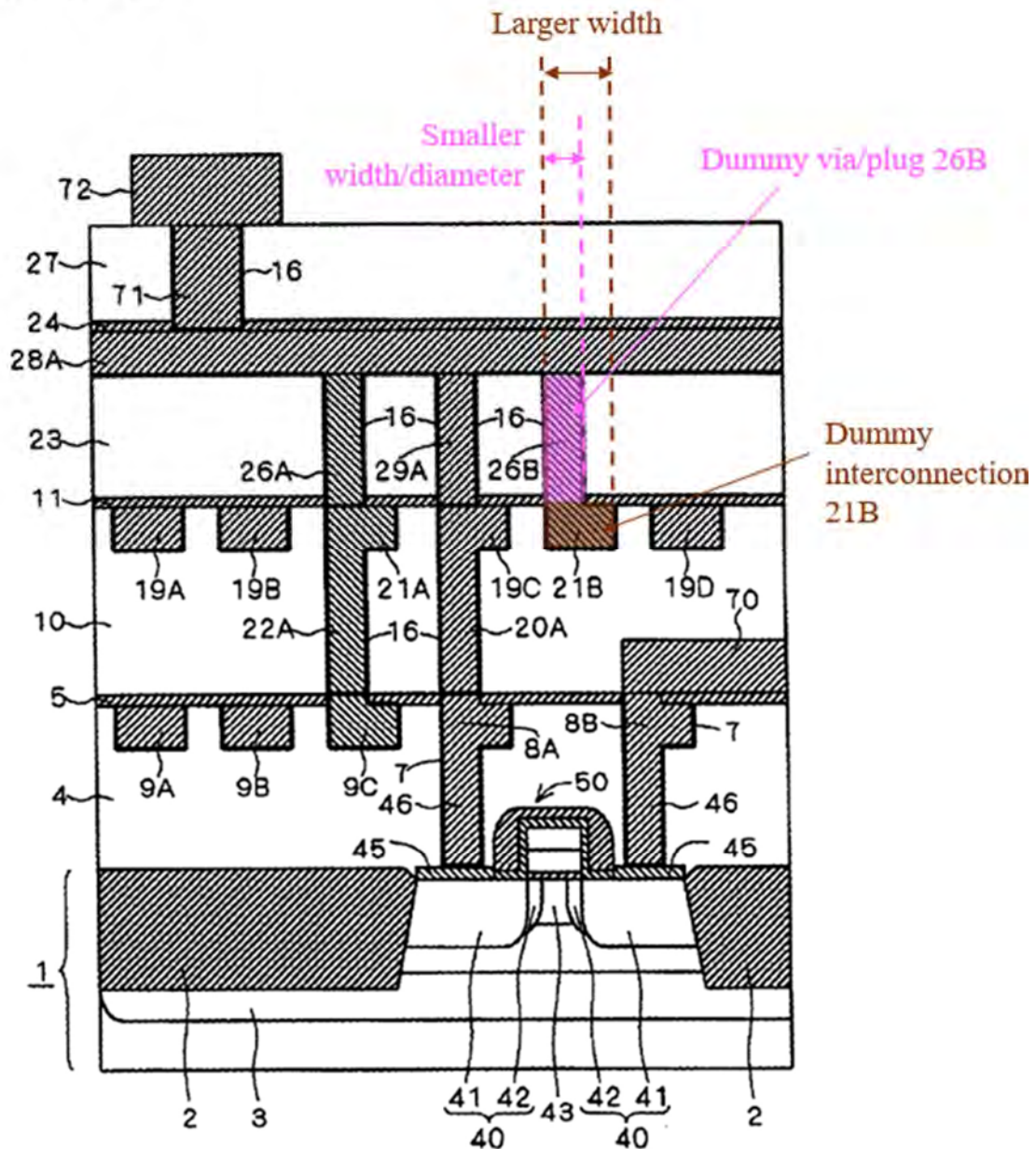
524. Because circular vias were well known, they could have been easily implemented as part of the standard patterning and manufacturing process of Kunikiyo and, thus, a POSITA would have expected success in doing so. Accordingly, it would have been obvious to a POSITA to manufacture Kunikiyo's dummy vias with a substantially circular planar shape.

b) [9.b] – “*a diameter of the dummy via is smaller than a width of the first dummy interconnect*”

525. Element [9.b] calls for “a diameter of the dummy via is smaller than a width of the first dummy interconnect,” which Kunikiyo and Iizuka render obvious.

526. As seen in annotated Figure 12, Kunikiyo shows that dummy plug 26B (“dummy via”) has a smaller width dimension than a width of the dummy interconnection 21B (“first dummy interconnect”):

FIG. 12



TSMC-1007, 20:25-34, Fig. 12. Similarly, I note that dummy plug 26A also has a smaller width dimension than a width of the dummy interconnection 21A. *See id.*

527. When the dummy plug 26B (or dummy plug 26A) is made circular in accordance with the teaching of, e.g., Iizuka, as discussed above, the diameter of the

dummy plug 26B will be smaller than a width of the dummy interconnection 21B (“first dummy interconnect”).

528. As I noted previously, a POSITA would have appreciated that Kunikiyo’s figures are intended to show the relative widths and contours of the structures shown therein. *Supra*, §X.I.3. For example, Kunikiyo describes how its Figure 9 specifically shows the alternating widths of interconnect 25B. TSMC-1007, 15:11-35. Thus, a POSITA would have reasonably interpreted Kunikiyo’s figures as showing different dimensioned features when they are drawn as such. A POSITA would therefore have interpreted Kunikiyo’s Figure 12 as portraying the relative width of dummy interconnection 21B as wider than the diameter of dummy via 26B (and similar for dummy interconnection 21A/dummy via 26A).

529. A POSITA would have had a reasonable expectation of success in implementing Kunikiyo’s vias (both functional and dummy) with a circular cross-sectional shape, and having a diameter less than the dummy interconnect as disclosed in Kunikiyo, as this would easily be accomplished using the standard patterning and manufacturing techniques used to make the interconnect structure in general. Certainly it was well known how to pattern via holes having circular cross-sections using masks, photolithography, and etching, and such round patterns subsequently result in circular vias when conductive material is deposited into the patterned vias holes. It would have been obvious, therefore, for a planar shape of

each of the dummy plugs 26A, 26B of Kunikiyo (“dummy vias”) to be substantially a circle, and they would have a smaller width dimension (diameter) than a width of the dummy interconnection 21A, 21B (“first dummy interconnect”) taught by Kunikiyo.

2. Claim 17 – “*semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view*”

530. Claim 17 recites the “semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view,” which Kunikiyo and Iizuka render obvious.

531. As discussed above for claim 9, Iizuka teaches common cross-sectional shapes for vias, demonstrating that circular vias and dummy vias were known design options: “the opening of the via-hole may have any configuration, such as a square, rectangle or circle,” and a circular pattern means the resulting via formed in a circular hole would have a substantially circular shape. TSMC-1008, 9:44-47, 10:17-22. Consistent with Iizuka’s teachings, that vias would be manufactured with any of a variety of cross-sectional shapes, including circular cross-sections, was well known to a POSITA at the time. *See, e.g.*, TSMC-1005, ¶¶[0200], [0209], Figs. 19A, 22A (disclosing circular dummy vias); TSMC-1013, 8:47-52 (noting that vias may have circular cross-sectional shapes); TSMC-1014, ¶¶[0091] (teaching circular vias as a default shape).

532. For the same reasons discussed above for claim 9, it would have been obvious based on the teaching in Iizuka to make both the plug 29A (“via”) and the dummy plug 26B (“dummy via”) in Kunikiyo substantially circular in a plan view because Iizuka explains that a circular via was a known design option, as the other prior art cited in the preceding paragraph likewise confirms. A POSITA would have viewed a circular cross-sectional shape as among a finite number of common, interchangeable design choices for both functional and dummy vias, expressly taught by Iizuka and within a POSITA’s general understanding, as evidenced above. It would have been obvious based on this reasoning alone to make a planar cross-sectional shape of Kunikiyo’s plug 29A (“via”) and dummy plug 26B (“dummy via”) circular because, as Iizuka confirms, circular-shaped vias were a known design option.

533. In addition, circular via shapes provide known advantages applicable to a given situation. For example, circular vias can provide for greater manufacturing process control (e.g., more uniform etching and filling characteristics for circular shapes compared to sharp-cornered squares), more favorable stress distribution around a circular opening, and design simplicity. *See, e.g.*, TSMC-1038, 7:62-67 (teaching that vias having circular cross-sections benefit from more precisely controlled etching, improved coverage of barrier metal in the via opening, and easier fill-in of the via opening with a metal film). Circular-shaped vias also

provide improved reliability due to the lack of sharp corners that can concentrate stress and cause damage in the form of dielectric cracking and the like.

534. While there can sometimes be operational or design considerations that lead to a preference for circular vias, a POSITA nonetheless recognized that the fundamental function of Kunikiyo's vias in terms of providing a conductive path between first and second interconnects (*see, e.g.*, TSMC-1007, 20:15-24) and dummy vias in terms of enhancing the uniformity of interconnection density and manufacturability, improving surface flatness for processing steps like CMP, and providing electrical shielding (*see, e.g.*, TSMC-1007, 5:46-54, 12:31-36, 14:31-36, 20:25-37, 25:54-26:9), would all be realized using circular-shaped vias and dummy vias. That is, these functions for Kunikiyo's vias and dummy vias do not depend on the exact cross-sectional shape of the via or dummy via. In this regard, I note that the '623 patent teaches no criticality or surprising or unexpected results with respect to the cross-sectional shape of its vias or dummy vias, nor did the Examiner view the via/dummy via shape as being critical (*see, e.g.*, TSMC-1002, 292-96), thus reinforcing my opinion that the cross-sectional via/dummy via shapes were nothing more than a matter of routine design choice.

535. Further, because a POSITA was aware of the basic via shapes, and was aware of the role of vias in providing conductive paths between interconnects and the dummy vias in providing process uniformity (*supra*, §IX.D) as well as reducing

stress-induced voiding and electromigration problems as taught, for example, by Watanabe (*supra*, §IX.A), it would have been a matter of routine optimization to choose the via shape that works best for a given overall design. With a few basic shapes to choose from (e.g., circular, square, rectangular) and known concerns regarding the ability of vias/dummy vias to be both formed and filled with conductive materials while avoiding stress-induced problems, it would not have required an undue amount of experimentation to arrive at the optimal via shape.

536. Given that circular-shaped vias were well known, they could have been easily implemented as part of the standard patterning and manufacturing process for Kunikiyo's vias and dummy vias and, thus, a POSITA would have expected success. Accordingly, it would have been obvious to a POSITA to manufacture Kunikiyo's vias and dummy vias with a substantially circular planar shape.

K. Ground 11: Claim 3 Is Obvious Over Kunikiyo and Watanabe

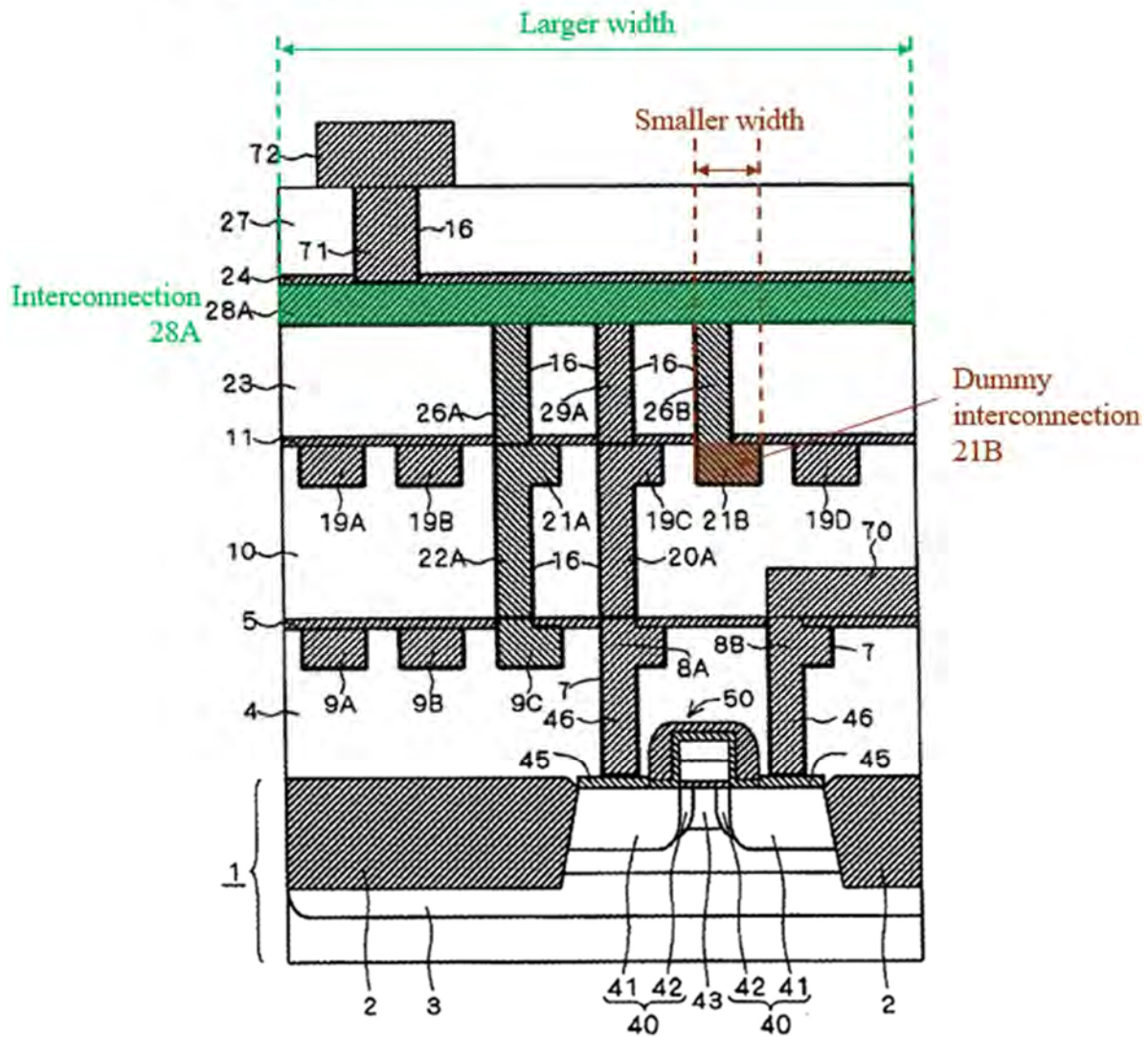
537. I believe claim 3 is obvious to a POSITA in view of Kunikiyo and Watanabe. I have previously discussed how both Kunikiyo and Watanabe disclose claims 1 and 2. *Supra*, §§X.A.1-2, X.I.1-2.

1. Claim 3 – “*semiconductor device of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect*”

538. Claim 3 recites the “semiconductor device of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect,” which Kunikiyo teaches and, additionally, Kunikiyo and Watanabe render obvious. Kunikiyo discloses claim 2 (from which claim 3 depends) as discussed above. *Supra*, §X.I.2.

539. As shown in annotated Figure 12 of Kunikiyo below, Kunikiyo discloses dummy interconnect 21B having a smaller width (along the cross-section captured in Figure 12) than the second interconnect 28A:

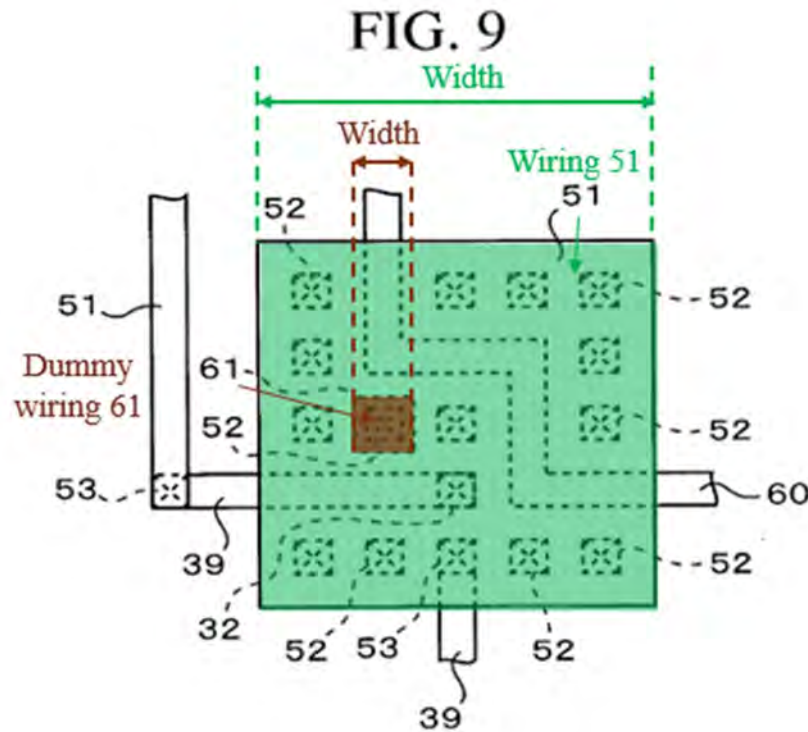
FIG. 12



A POSITA would have appreciated this relative sizing of the second interconnect as compared to the lower-level dummy interconnect because upper level interconnects, such as Kunikiyo's "second interconnect" 28A, often need to connect to a greater number of lower-level interconnects/dummy interconnects by vias/dummy vias. This can be seen, for example, in Kunikiyo's Figure 12 above, where "second interconnect" 28A is connected to each of lower-levels interconnect 19C and dummy

interconnects 21A and 21B by via 29A and dummy vias 26A and 26B, respectively. Given the greater number of connections that second interconnect 28A must make, a POSITA would appreciate that it would have a width greater than the width of the underlying dummy interconnect.

540. Watanabe expressly teaches this well-known understanding of a POSITA that interconnects and dummy interconnects can have a variety of sizes and shapes depending on the design requirements for the specific device at issue, including second (upper) interconnect widths larger than the width of dummy interconnects. *See* TSMC-1004, ¶[0127], Fig. 9. In particular, Watanabe teaches a dummy interconnect configured to have a smaller width than an upper level interconnect (such as the claimed “second interconnect”). *Supra*, §X.A.3. For example, Figure 9 of Watanabe discloses dummy interconnect (e.g., “dummy wiring 61”) having a smaller width than the second interconnect (e.g., “wiring 51”):



Id., Fig. 9, ¶[0125]; *see also id.*, ¶[0105].

541. Thus, as clearly shown in Figure 9 above, Watanabe teaches that the specific relative sizing (including relative widths) of dummy interconnects and functional upper level interconnects, including the functional upper level interconnect being larger than dummy interconnect such as in Figure 9, was a mere design choice that a POSITA was well aware of at the time. Indeed, a POSITA would have recognized that implementing such relative sizing of dummy interconnects and second interconnects into Kunikiyo's device would simply be accomplished by substituting interconnects having such relative sizes/widths into Kunikiyo's devices (including the device disclosed in Kunikiyo's Figure 12).

542. The '623 patent does not give any express reason for the relative sizing between the dummy interconnect and second interconnect or teach any surprising or unexpected results; thus a POSITA would not have gleaned any criticality or unexpected results associated with these relative feature sizes from the discussion in the '623 patent.

543. A POSITA would have been further motivated in certain instances to use a wider-width second interconnect (as compared to the dummy interconnect) to provide a relatively larger and wider “second interconnect” which would have provided more space for additional via connections and thus connections to other circuit elements above and below the “second interconnect.” It was common prior to the '623 patent for higher-level interconnects to be relatively larger than lower-level interconnects (including dummy interconnects) to accommodate more connections, carry more current, reduce resistance, and meet electromigration rules. TSMC-1034, 585-86, 591, Figs. 12-17, 12-18. This is because having a larger, wider second/upper interconnect enables connections to a greater number of functional vias and corresponding wirings, thus enabling more complex circuits and expanding the design options available to the circuit/device designer, as well as connections to more dummy vias and dummy interconnects.

544. Thus, in situations where the circuit design requires additional space for the second interconnect, a POSITA would have chosen such wider interconnects

for use in the semiconductor device. Figure 9 of Watanabe is one example disclosing such a larger second/upper interconnect, which is useful for additional connections through active vias and dummy vias. In addition, having a wider second/upper interconnect permits space for a much greater number of dummy vias, which will better accumulate vacancies as compared to smaller, narrower interconnects having fewer dummy vias, thus further mitigating vacancies from migrating to functional vias and causing stress migration problems. *See, e.g.*, TSMC-1004, ¶[0108] (noting the advantages of having multiple dummy vias).

545. Additionally, dummy interconnects on the same level as the first interconnect (i.e., closer to the semiconductor substrate) can more easily be made with relatively smaller widths than interconnects on the next level up. Smaller width dimensions are in fact desired at lower levels in the interconnect structure because a greater concentration/density of wiring is needed to connect to transistors in the semiconductor substrate, thus necessitating features having smaller widths to achieve the needed layout density at lower layers. *See, e.g.*, TSMC-1034, 585-86, 591, Figs. 12-17, 12-18. Dummy interconnects at the lower interconnect levels have to maintain the same general dimensions as the active wires at that same level to maintain pitch requirements (to reduce/avoid unwanted parasitic capacitance, for example (*see, e.g.*, TSMC-1004, ¶[0034] (noting problem of inter-wiring capacitance))). and allow for efficient routing and wiring density. In contrast, higher

levels typically connect to a greater number of elements and thus carry more current and need better heat dissipation, giving rise to relatively wider interconnect widths higher in the structure (e.g., “second interconnects”). *Id.*, Figs. 5A-5C, 9; TSMC-1012, 34; TSMC-1034, 594. This need to implement smaller features at the lower interconnect levels would have applied equally to the first interconnects as well as dummy interconnects to help maintain process uniformity and enable adequate routing options for the active interconnects.

546. It was also typical for interconnect widths to increase when moving up levels in an interconnect structure because as the levels build on top of each other, it can become more challenging for CMP to produce surfaces having the same level of smoothness as lower levels. Because surface smoothness impacts the lithography resolution that can be achieved, minimum interconnect widths are typically larger the higher up one is in the interconnect structure. The specific desired width for any given application would take into account known design considerations, and Watanabe provides one such example that demonstrates the known nature of an active interconnect (wiring 51) being wider than the dummy interconnect 61, showing that implementing the claimed relative dimensions was a simple design choice.

547. A POSITA would have considered such a modification likely to be successful, given that it merely requires changing the relative sizes of the dummy

and second interconnects, which would have been easily achieved using standard patterning and processing techniques at the time, as evidenced for example by Watanabe (*e.g.*, TSMC-1004, Fig. 9). For example, a POSITA would have understood that such second and dummy interconnects could be easily created by merely etching patterned trenches to the appropriate desired size in the insulating film in which the interconnects were formed, respectively. *See, e.g.*, TSMC-1016, 6:14-29; TSMC-1028, 5458. Tailoring the size, location, etc., of such trenches (and thus the resulting second/dummy interconnect formed in the trench) was routinely performed. Indeed, it was and is performed for the fabrication of every such semiconductor device.

XI. CONCLUSION

548. As discussed above, it is my opinion that the Challenged Claims of the '623 patent are unpatentable because they are anticipated by the prior art, because they would have been obvious to a person of ordinary skill in view of the prior art, or both.

549. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for

cross-examination within the United States during the time allotted for cross-examination.

550. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

551. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Declaration of Dr. Reinhold Dauskardt

Executed on this 24th day of July, 2025, in Stanford, CA.

By: _____  _____

Dr. Reinhold H. Dauskardt

Appendix A

EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,439,623
1002	File History of U.S. Patent No. 7,439,623 (“the ’623 File History”)
1003	Declaration of Dr. Reinhold Dauskardt
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. (“Watanabe”)
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. (“Hasunuma”)
1006	U.S. Patent Publication No. 2001/0019180 to Aoyagi et al. (“Aoyagi”)
1007	U.S. Patent No. 6,717,267 to Kunikiyo (“Kunikiyo”)
1008	U.S. Patent No. 5,250,465 to Iizuka et al. (“Iizuka”)
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. (“Kamoshima”)
1010	Reserved
1011	U.S. Patent No. 7,042,099 to Kurashima (“Kurashima”)
1012	P. Andricacos, “Copper On-Chip Interconnections,” <i>Interface</i> , The Electrochemical Society, pp. 32-37, 1999
1013	U.S. Patent No. 5,885,857 to Yamaha et al. (“Yamaha”)
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi et al. (“Igarashi”)

Exhibit No.	Description
1015	U.S. Patent No. 6,717,268 to Hau-Riege (“Hau-Riege”)
1016	U.S. Patent No. 6,468,894 to Yang (“Yang”)
1017	U.S. Patent No. 6,022,808 to Nogami (“Nogami”)
1018	AICP’S P.R. 3-1 Disclosure of Asserted Claims and Infringement Contentions and P.R. 3-2 Document Production Against TSMC (cover document only)
1019	Kaanta et al., “Dual Damascene: A ULSI Wiring Technology,” <i>VMIC Conference</i> , IEEE, June 11-12, 1991, pp. 144-152
1020	U.S. Patent No. 5,032,890 to Ushiku (“Ushiku”)
1021	Reserved
1022	U.S. Patent No. 6,582,976 to Watanabe (“Watanabe’976”)
1023	S. Middleman et al., <i>Process Engineering Analysis in Semiconductor Device Fabrication</i> , pp. 260-61 (excerpted), McGraw-Hill, 1993 (“Middleman”)
1024	U.S. Patent No. 6,156,660 to Liu et al. (“Liu”)
1025	U.S. Patent No. 5,798,298 to Yang (“Yang 2”)
1026	T. I. Bao <i>et al.</i> , “90 nm Generation Cu/CVD Low-k ($k < 2.5$) Interconnect Technology,” <i>Digest. International Electron Devices Meeting</i> , San Francisco, CA, USA, 2002, pp. 583-586
1027	A. Loke, “Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects,” Dissertation, Stanford University (1999)

Exhibit No.	Description
1028	K.N. Tu, “Recent advances on electromigration in very-large-scale-integration of interconnects,” <i>Applied Physics Review – Focused Review, Journal of Applied Physics</i> , Vol. 94, No. 9 (November 1, 2003), pp. 5451-5473
1029	T. C. Huang, <i>et al.</i> , “Numerical Modeling and Characterization of the Stress Migration Behaviour Upon Various 90 nanometer Cu/Low k Interconnects,” <i>Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)</i> , Burlingame, CA, USA, 2003 (added to IEEE Xplore 8-11-2003), pp. 207-209
1030	Reserved
1031	JP2000277609 to Narita (“Narita”) and Certified Translation of Narita with Certification of Translation
1032	JP2000012688 to Nasu (“Nasu”) and Certified Translation of Nasu with Certification of Translation
1033	U.S. Patent Publication No. 2001/0030365 to Otsuka et al. (“Otsuka”)
1034	Wolf, Stanley, <i>Silicon Processing for the VLSI Era: Deep-Submicron Process Technology</i> , Lattice Press, 2002 (excerpted) (“Wolf”)
1035	Reserved
1036	Reserved
1037	A. von Glasow et al., “Geometrical Aspects of Stress-Induced Voiding in Copper Interconnects,” <i>Proceedings of the Advanced Metallization Conference 2002 (AMC 2002)</i> , San Diego, CA, October 1-3, 2002, Tokyo, Japan, October 29-30, 2002, Materials Research Society, pp. 161-67
1038	U.S. Patent No. 6,215,189 to Toyoda et al. (“Toyoda”)

Appendix B

LIST OF CHALLENGED CLAIMS

Claim Element	Claim Language
[1.pre]	A semiconductor device comprising:
[1.a]	a semiconductor substrate;
[1.b]	a first interconnect formed on the semiconductor substrate;
[1.c]	a first insulating film formed on the first interconnect;
[1.d]	a second interconnect formed on the first insulating film;
[1.e]	a via formed through the first insulating film and connecting between the first and second interconnects; and
[1.f]	a dummy via connected to the second interconnect,
[1.g]	wherein the dummy via is made of a conductive film and is arranged so as to be incapable of having current flow therethrough;
[1.h]	the second interconnect and the via form a dual damascene structure, and
[1.i]	the second interconnect and the dummy via form a dual damascene structure.
[2.a]	The semiconductor device of claim 1 further comprising a second insulating film formed on the semiconductor substrate,
[2.b]	wherein the first interconnect is formed on the second insulating film, and

[2.c]	the dummy via is connected to a first dummy interconnect formed on the second insulating film.
3	The semiconductor device of claim 2, wherein the first dummy interconnect has a width smaller than that of the second interconnect.
4	The semiconductor device of claim 2, wherein a width of the first dummy interconnect and a width of the first interconnect are substantially equal to each other.
7	The semiconductor device of claim 2, wherein each of the first interconnect and the first dummy interconnect is buried in an upper portion of the second insulating film.
8	The semiconductor device of claim 2, wherein a longer side of the first interconnect and a longer side of the first dummy interconnect form substantially a right angle.
[9.a]	The semiconductor device of claim 2, wherein the dummy via is substantially circular in a plan view, and
[9.b]	a diameter of the dummy via is smaller than a width of the first dummy interconnect.

11	The semiconductor device of claim 1, wherein the first insulating film has a multilayer structure including a SiN film and a SiO ₂ film.
12	The semiconductor device of claim 1, wherein the second interconnect includes a first barrier film and a first conductive film.
13	The semiconductor device of claim 12, wherein the first conductive film includes copper.
14	The semiconductor device of claim 1, wherein each of the first and second interconnects is connected to another element or an external electrode.
[15.a]	The semiconductor device of claim 1, wherein the first interconnect, the second interconnect and the via constitute part of a closed circuit, and
[15.b]	the dummy via does not constitute a closed circuit.
16	The semiconductor device of claim 1, wherein the first interconnect has a width smaller than that of the second interconnect.

17	The semiconductor device of claim 1, wherein the via and the dummy via are substantially circular in a plan view.
18	The semiconductor device of claim 17, wherein a diameter of the via and a diameter of the dummy via are substantially equal to each other.
21	The semiconductor device of claim 1, wherein the first interconnect and the second interconnect extend in a same direction.
22	The semiconductor device of claim 1, wherein the dummy via is provided on an extended line along which the first interconnect extends.
25	The semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 25 μm or less.
26	The semiconductor device of claim 1, wherein the via and the dummy via are spaced at a distance of 1 μm or less.
28	The semiconductor device of claim 1, wherein the dummy via is provided in plural.

32	The semiconductor device of claim 1, wherein a distance between the via and one end of the second interconnect is shorter than a distance between the dummy via and the one end of the second interconnect and shorter than a distance between the via and the other end of the second interconnect.
39	The semiconductor device of claim 1, wherein the dummy via and the second interconnect are made of the same conductive film.
40	The semiconductor device of claim 1, wherein the dummy via and the second interconnect include a Cu film.
42	The semiconductor device of claim 1, wherein the dummy via includes a first and second end, the first end connected to the second interconnect and the second end connected to a first dummy interconnect, the first dummy interconnect being surrounded by a second insulating film.
[45.a]	The semiconductor device of claim 1, wherein the second interconnect is comprised of a first interconnect portion and a second interconnect portion whose interconnect width is smaller than that of the first interconnect portion and which branches from the first interconnect portion, and
[45.b]	the via is connected to the second interconnect portion.

46	The semiconductor device of claim 45, wherein the dummy via is formed at or near the branch point between the first and second interconnect portions.
47	The semiconductor device of claim 45, wherein a width of the second interconnect portion is 0.2 μm or less.

Appendix C

Reinhold H. Dauskardt, Ph.D.

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Reinhold Dauskardt is the Ruth G. and William K. Bowes Professor in the Department of Materials Science and Engineering and has additional appointments as Professor in Mechanical Engineering, the Biodesign Institute and the Department of Surgery, Stanford School of Medicine. Dauskardt is a member of Stanford Bio-X, the Cardiovascular Institute, the Wu Tsai Human Performance Alliance, and the Wu Tsai Neurosciences Institute, and an affiliate of the Precourt Institute for Energy and the Stanford Woods Institute for the Environment. He is also a Visiting Professor in the School of Materials Science and Engineering at the Nanyang Technological University in Singapore.

The underlying theme of his research is to enable innovation and design of high-performance materials and devices by exploiting the fundamental connection between device materials, design, and processing and resulting device performance, function and reliability under use conditions.

Dauskardt and his group have worked extensively on integrating new nano and molecular materials into emerging technologies that include semiconductor, nanoscience and energy technologies, high-performance laminates, biomaterials and soft tissues.

He is an internationally recognized expert on the design and thermomechanical reliability of engineering structures, solar, battery and electronic device technologies for which he was awarded the prestigious Semiconductor Industry Association University Researcher Award in 2010 for “research which has provided substantive and sustained contributions to semiconductor industry science and technology.” The Dauskardt Lab has a unique combination of internationally recognized materials and device processing capabilities, scalable manufacturing, reliability physics, high resolution characterization, accelerated testing and modeling capabilities. These capabilities include advanced sol-gel processing and open-air spray plasma deposition of semiconductor, solar and battery materials, along with accelerated testing and reliability modeling. He is also well known for his studies of the effects of semiconductor device and packaging processing operations and processing environments (including plasma processing, chemical mechanical planarization (CMP), and a wide range of deposition techniques) on device structures and their properties. Experimental studies are complimented with a range of multi-scale mechanics and molecular computational modeling capabilities.

His research on soft tissues and wound healing has concentrated on establishing a biomechanics framework to understand and control the biological processes that determine the effects of treatments and exposures on barrier function and the biomechanics of human skin and other soft tissues for which he was awarded the Henry Maso Award for fundamental contributions to the advancement of cosmetic and skin science, and scar formation in healing cutaneous wounds. A major theme in his labs current research involves wearable device technologies. The interdisciplinary nature of his research is reflected in his appointments in the Stanford Biodesign Institute and in the Department of Surgery, Stanford School of Medicine.

His interdisciplinary research includes interaction with researchers in academia, industry, and clinical practice. He has served as an editor and reviewer for a number of journals and books including Nature, Science, Energy and Environmental Sciences, Nanoletters, Acta Materialia, the Journal of Applied Physics, PANS and the New England Journal of Medicine. He has co-organized international technical conferences and symposia in his areas of research. He has published over

400 articles in the scientific literature and holds more than 30 U.S. and International Patents. Dauskardt has contributed significantly to leadership in Stanford's multidisciplinary materials efforts which spans several departments, schools, and the SSRL.

Education: B.Sc. (1980) and M.Sc. (1983) Physics, Mathematics and Materials – U. Witwatersrand, South Africa, Ph.D. Materials Science and Eng. - U.C. Berkeley/ U. Witwatersrand (1988).

Recognition and Awards: 2016: Visiting Professor, Nanyang Technological University. 2013: appointed the Ruth G. and William K. Bowes Professor in the School of Engineering, Stanford University. 2011: H. Maso Award for fundamental contributions to skin science, Int. Fed. Soc. Cos. Chem.; IBM Shared University Research Award. 2010: Semiconductor Industry Assoc. Univ. Researcher Award for substantive contributions to semiconductor industry sci. & tech.; TMS Struct. Mat. Distinguished Scientist Award; Fellow ASM Int. 2008: Fellow Am. Ceram. Soc.; VLSI/ULSI Multilevel Interconnection Int. Conf. Award for “Optimized Curing and CMP of Nanostructured Ultra-low-k Films”; Am. Vac. Soc. Thin-Film User Group Special Award. 2006: Distinguished Speaker Award, Dept. MSE, Penn State; IBM Faculty Award, Yorktown Heights. 2003: ASM Int. Silver Medal. 2002: Alexander von Humboldt Research Award. 1989: U.S. DoE Outstanding Sci. Accomplishment Award.

Advisory Boards and Board of Directors: Advisory Board, National Inst. Materials Science, Tsukuba, Japan; Advisory Board, School of Mat. Sci. Eng. Nanyang Tech. U., Singapore; Advisory Board, Singapore Institute of Manufacturing Technology (SimTech), A-Star, Singapore; Co-founder, Neodyne Biosciences Inc. (medical devices), Palo Alto, CA.

Professional Activities: Dauskardt has been involved in a range of university academic and materials research leadership roles at Stanford. He is an established international leader in the broader materials and device technical and scientific communities where he has managed several large multidisciplinary research activities. He has served as organizer of a range of international conferences and symposia.

He serves as a consultant and technical advisor to a range of leading international technology companies, materials suppliers, and equipment vendors. He is well known for his work providing technical expert services in trial, by declaration, and/or deposition for litigation and regarding both validity and infringement analysis in US and International patent cases.

Doctoral Students and Post Doctoral Fellows: Dauskardt has supervised 66 doctoral students and 48 post-doctoral fellows, medical residents and medical fellows. He currently has 16 doctoral students, 2 masters student, and 2 post docs in his research group along with visiting professors and industry researchers.

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