IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner,

v.

Advanced Integrated Circuit Process LLC,

Patent Owner.

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IPR2025-01212

U.S. Patent No. 7,439,623

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PETITIONER'S UPDATED EXHIBIT LIST

UPDATED EXHIBIT LIST

Exhibit No.	Description	Filed	Served
1001	U.S. Patent No. 7,439,623	X	X
1002	File History of U.S. Patent No. 7,439,623 ("'623 File History")	X	X
1003	Declaration of Dr. Reinhold Dauskardt	X	X
1004	U.S. Patent Publication No. 2003/0116852 to Watanabe et al. ("Watanabe")	X	X
1005	U.S. Patent Publication No. 2004/0113238 to Hasunuma et al. ("Hasunuma")	X	X
1006	U.S. Patent Publication No. 2001/0019180 to Aoyagi et al. ("Aoyagi")	X	X
1007	U.S. Patent No. 6,717,267 to Kunikiyo ("Kunikiyo")	X	X
1008	U.S. Patent No. 5,250,465 to Iizuka et al. ("Iizuka")	X	X
1009	U.S. Patent Publication No. 2004/0173905 to Kamoshima et al. ("Kamoshima")	X	X
1010	Reserved		
1011	U.S. Patent No. 7,042,099 to Kurashima ("Kurashima")	X	X
1012	P. Andricacos, "Copper On-Chip Interconnections," *Interface*, *The Electrochemical Society*, pp. 32-37, 1999	X	X

Exhibit No.	Description	Filed	Served
1013	U.S. Patent No. 5,885,857 to Yamaha et al. ("Yamaha")	X	X
1014	U.S. Patent Publication No. 2003/0005399 to Igarashi ("Igarashi")	X	X
1015	U.S. Patent No. 6,717,268 to Hau-Riege ("Hau-Riege")	X	X
1016	U.S. Patent No. 6,468,894 to Yang ("Yang")	X	X
1017	U.S. Patent No. 6,022,808 to Nogami ("Nogami")	X	X
1018	AICP'S P.R. 3-1 Disclosure of Asserted Claims and Infringement Contentions and P.R. 3-2 Document Production Against TSMC (cover document only)	X	X
1019	Kaanta et al., "Dual Damascene: A ULSI Wiring Technology," VMIC Conference, IEEE, Jun. 11-12, 1991, pp. 144-152	X	X
1020	U.S. Patent No. 5,032,890 to Ushiku ("Ushiku")	X	X
1021	Reserved		
1022	U.S. Patent No. 6,582,976 to Watanabe ("Watanabe'976")	X	X
1023	S. Middleman et al., *Process Engineering Analysis in Semiconductor Device Fabrication*, pp. 260-61 (excerpted), McGraw-Hill, 1993 ("Middleman")	X	X
1024	U.S. Patent No. 6,156,660 to Liu et al. ("Liu")	X	X

Exhibit No.	Description	Filed	Served
1025	U.S. Patent No. 5,798,298 to Yang ("Yang 2")	X	X
1026	T. I. Bao et al., "90 nm Generation Cu/CVD Low-k (k < 2.5) Interconnect Technology," *Digest. International Electron Devices Meeting*, San Francisco, CA, USA, 2002, pp. 583-586	X	X
1027	A. Loke, "Process Integration Issues of Low-Permittivity Dielectrics With Copper for High-Performance Interconnects, Dissertation," Stanford University (1999)	X	X
1028	K.N. Tu, "Recent advances on electromigration in very-large- scale-integration of interconnects," *Applied Physics Review – Focused Review*, *Journal of Applied Physics*, Vol. 94, No. 9, pp. 5451-5473 (November 1, 2003)	X	X
1029	T. C. Huang, et al., "Numerical Modeling and Characterization of the Stress Migration Behaviour Upon Various 90 nanometer Cu/Low k Interconnects," Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695), Burlingame, CA, USA, 2003 (added to IEEE Xplore 8-11-2003), pp. 207-209	X	X
1030	Reserved		
1031	JP2000277609 to Narita ("Narita") and Certified Translation of Narita with Certification of Translation	X	X
1032	JP2000012688 to Nasu ("Nasu") and Certified Translation of Nasu with Certification of	X	X

Exhibit No.	Description	Filed	Served
	Translation		
1033	U.S. Patent Publication No. 2001/0030365 to Otsuka et al. ("Otsuka")	X	X
1034	Wolf, Stanley, Silicon Processing for the VLSI Era: Deep- Submicron Process Technology, Lattice Press, 2002 (excerpted) ("Wolf")	X	X
1035	Reserved		
1036	Reserved		
1037	A. von Glasow et al., "Geometrical Aspects of Stress-Induced Voiding in Copper Interconnects," Proceedings of the Advanced Metallization Conference 2002 (AMC 2002), San Diego, CA, October 1-3, 2002, Tokyo, Japan, October 29-30, 2002, Materials Research Society, pp. 161-67	X	X
1038	U.S. Patent No. 6,215,189 to Toyoda et al. ("Toyoda")	X	X
1039	Reserved		
1040	STIPULATION: 7-31-2025 Letter from K. Wheatley (counsel for TSMC) to J. Nelson et al. (counsel for AICP)	X	X

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on August 21, 2025 a true and correct copy of **EXHIBIT 1040** and **PETITIONER'S UPDATED EXHIBIT LIST** was served in its entirety on the Patent Owner to the email addresses below:

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Dated: August 21, 2025

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